Product & Applications Handbook

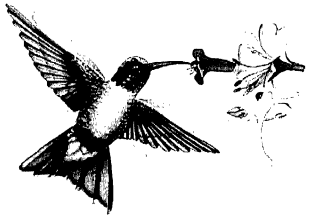
INTEGRATED CIRCUITS UNITRODE

Product & Applications Handbook 1993-94

INTEGRATED CIRCUITS UNITRODE

INTEGRATED CIRCUITS
UNITRODE

About the Cover



The Hummingbird is amazing. It's incredibly fast, astonishingly energetic, and phenomenally efficient.

It's remarkably versatile--it can even fly backwards. It can survive in any kind of environment.

And it's a tough little bird that masters every challenge and easily out performs much bigger competitors.

In fact, it's so much like UICC and our products that we've adopted it as our mascot.

So when you consider qualities like speed, efficiency, dependability, versatility, toughness, and top performance in a small package, remember the hummingbird...and UICC.

LIFE SUPPORT POLICY

U.I.C.C.'s products are not authorized for use as critical components in the life support devices or systems without express written approval.

Printed in U.S.A. - June, 1993

Introduction

Unitrode Integrated Circuits Corporation - U.I.C.C. - is a world leader in the design and manufacturing of high performance integrated circuits for power supplies, motor controls and power interface applications that demand high reliability, extraordinary quality and innovative technology.

Backed by a linear design team that we consider the best in the industry, by a total quality process designed and driven by our employees, by state-of-the-art manufacturing facilities, by a dynamic spirit of innovation and by the countless number of Continuous Improvement Teams passionately dedicated to customer satisfaction - the Company provides outstanding products and services globally. U.I.C.C serves customers around the world from:

- its recently expanded headquarters and principal manufacturing facility in Merrimack, New Hampshire;
- its design center in Raleigh, North Carolina;
- its extensive test, assembly subcontractor coordination and customer service facility in Singapore;
- and from its European distribution, quality and customer service facility in Ireland.

Process Capabilities

U.I.C.C.'s strengths include a number of production process capabilities that complement its design expertise and enhance its product offerings.

Its BIPOLAR process, optimized for both precision analog and power functions, is constantly updated to incorporate leading edge process options such as:

- Schottky and integrated injection logic;
- ion implant;
- thin film resistors with laser trimming;
- double-level metallization for high density, high current layouts;
- and buried zener reference.

Its BICMOS process is ideal for high density linear and mixed mode designs, especially where speed and low power are of primary importance. Process options include:

- 3-micron, N-well process with double poly;
- double level metallization;
- fully isolated, vertical NPN transistors;
- and thin film resistors with laser trim capability.

New process capabilities include a complementary bipolar process that dielectrically isolates substrates using a low cost proprietary technique for direct bonding of silicon wafers. It is an extremely cost effective way of replacing junction isolation with dielectric isolation, leading to dramatic size reductions and performance enhancements unobtainable with conventional IC technologies.

Many of U.I.C.C.'s new processes will be manufactured in its new Class 10 Wafer Fab that will be completed by mid-1993.

Introduction (Cont'd)

An ISO 9001 Firm

In October 1992, U.I.C.C. became one of the very few U.S. electronics companies to achieve IS/ISO 9001/EN29001 registration.

The ISO 9000 quality system was developed to establish an international standard of quality. In order to be registered, a company must pass a rigorous assessment of its quality systems -- from design of its product through shipment. Registration thus assures customers all over the world that the company is adhering to very high, precisely defined standards.

Meeting Demanding Market Needs

In the development of custom and semi-custom parts, U.I.C.C. design engineers work very closely with customer personnel. This close cooperation assures that all requirements are accurately understood, that all possibilities are fully explored, and that the resulting products meet and exceed specified needs.

U.I.C.C. pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that will satisfy them.

A Resource You Can Count On

Unitrode Integrated Circuits Corporation has earned its reputation for excellence in computer, communications, automotive, industrial, commercial and military markets. It is totally committed to continuing that excellence in everything it does.

With products and services that are among the most innovative in the industry, with proven quality and reliability, and with superb design engineering and the industry's best applications technical support, U.I.C.C. is a resource you can depend on.

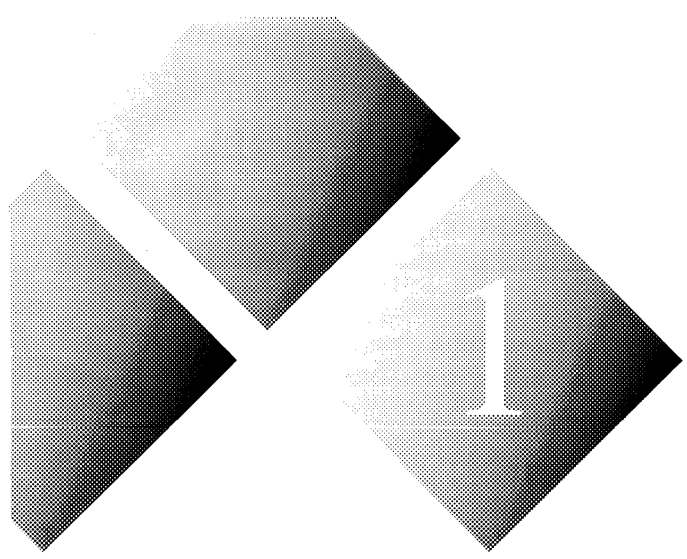
This databook describes new as well as previously introduced products, and it includes detailed applications information. We welcome your inquiries about our products and services, and we look forward to working with you.


INTEGRATED
CIRCUITS
UNITRODE

INDEX

TABLE OF CONTENTS


INTEGRATED
CIRCUITS
UNITRODE



Part Number Index


INTEGRATED
CIRCUITS
UNITRODE

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
6-6	L293	Push-Pull Four Channel Driver
6-6	L293D	Push-Pull Four Channel Driver
7-7	L295	Dual Switchmode Solenoid Driver
6-11	L298	Dual Full-Bridge Power Driver
6-15	L298D	Dual Full-Bridge Power Driver
*	UC117	1.5A, Three Terminal Adj. Voltage Regulator
*	UC137	1.5A, Three Terminal Adj. Negative Voltage Regulator
*	UC150	3A, Three Terminal Adj. Positive Voltage Regulator
5-15	UC161A	Micropower Quad Comparator
5-15	UC161B	Micropower Quad Comparator
5-15	UC161C	Micropower Quad Comparator
*	UC195	Smart Power Transistor
*	UC217	1.5A, Three Terminal Adj. Voltage Regulators
*	UC237	1.5A, Three Terminal Adj. Negative Voltage Regulator
*	UC250	3A, Three Terminal Adj. Positive Voltage Regulator
*	UC295	Smart Power Transistor
*	UC317	1.5A, Three Terminal Adj. Voltage Regulators
*	UC337	1.5A, Three Terminal Adj. Negative Voltage Regulator
*	UC350	3A, Three Terminal Adj. Positive Voltage Regulator
*	UC395	Smart Power Transistor
5-19	UC494A	Advanced Regulating Pulse Width Modulators
5-19	UC494AC	Advanced Regulating Pulse Width Modulators
5-19	UC495A	Advanced Regulating Pulse Width Modulators
5-19	UC495AC	Advanced Regulating Pulse Width Modulators
6-19	UC1517	Stepper Motor Drive Circuit
5-23	UC1524	Advanced Regulating Pulse Width Modulators
5-28	UC1524A	Advanced Regulating Pulse Width Modulators
5-34	UC1525A	Regulating Pulse Width Modulators
5-41	UC1525B	Regulating Pulse Width Modulators
5-47	UC1526	Regulating Pulse Width Monitor
5-54	UC1526A	Regulating Pulse Width Modulator
5-34	UC1527A	Regulating Pulse Width Modulators
5-41	UC1527B	Regulating Pulse Width Modulators

PAGE	PART NUMBER	DESCRIPTION
5-62	UC1543	Power Supply Supervisory Circuit
5-62	UC1544	Power Supply Supervisory Circuit
5-67	UC1575-5	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC1575-12	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC1575-15	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-73	UC1575-ADJ	Simple 1 Amp Step-Down Voltage Regulator
5-80	UC1576-5	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC1576-12	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC1576-15	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-87	UC1576-ADJ	Simple 3 Amp Step-Down Voltage Regulator
5-94	UC1577-12	Simple Step-Up Fixed Voltage Regulators
5-94	UC1577-15	Simple Step-Up Fixed Voltage Regulators
5-99	UC1577-ADJ	Simple Step-Up Voltage Regulator
6-26 & 5-106	UC1610	Dual Schottky Diode Bridge
6-28 & 5-108	UC1611	Quad Schottky Diode Array
6-31 & 5-111	UC1612	Dual Schottky Diode
6-33	UC1620	Switchmode Driver for 3-Ø Brushless DC Motors
6-39	UC1625	Brushless DC Motor Controller
6-50	UC1633	Phase Locked Frequency Controller
6-57	UC1634	Phased Locked Frequency Controller
6-61	UC1635	Phased Locked Frequency Controller
6-65	UC1637	Switched Mode Controller for DC Motor Drive
7-11	UC1705	High Speed Power Driver
7-14	UC1706	Dual Output Driver
7-19	UC1707	Dual Channel Power Driver
7-25	UC1708	Dual Non-Inverting Power Driver
7-29	UC1709	Dual High-Speed FET Driver
7-32	UC1710	High Current FET Driver
7-35	UC1711	Dual Ultra High-Speed FET Driver
6-71	UC1717	Stepper Motor Drive Circuit
7-37	UC1724	Isolated Drive Transmitter
7-40	UC1725	Isolated High Side FET Driver
7-44	UC1726	Isolated Drive Transmitter
7-49	UC1727	Isolated High Side IGBT Driver
7-55	UC1730	Thermal Monitor
5-113	UC1823	High Speed PWM Controller
5-119	UC1823A	High Speed PWM Controller

*Consult Factory

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
5-119	UC1823B	High Speed PWM Controller
5-127	UC1824	High Speed PWM Controller
5-134	UC1825	High Speed PWM Controller
5-119	UC1825A	High Speed PWM Controller
5-119	UC1825B	High Speed PWM Controller
5-141	UC1828	Current Mode PWM Controller IC
5-142	UC1832	Precision Low Dropout Linear Controllers
5-142	UC1833	Precision Low Dropout Linear Controllers
5-149	UC1834	High Efficiency Linear Regulator
5-155	UC1835	High Efficiency Regulator Controller
5-155	UC1836	High Efficiency Regulator Controller
5-159	UC1838A	Magnetic Amplifier Controller
5-163	UC1840	Programmable, Off-Line, PWM Controller
5-171	UC1841	Programmable, Off-Line, PWM Controller
5-179	UC1842	Current Mode PWM Controller
5-186	UC1842A	Current Mode PWM Controller
5-179	UC1843	Current Mode PWM Controller
5-186	UC1843A	Current Mode PWM Controller
5-179	UC1844	Current Mode PWM Controller
5-186	UC1844A	Current Mode PWM Controller
5-179	UC1845	Current Mode PWM Controller
5-186	UC1845A	Current Mode PWM Controller
5-192	UC1846	Current Mode PWM Controller
5-192	UC1847	Current Mode PWM Controller
5-199	UC1848	Average Current Mode PWM Controller
5-207	UC1851	Programmable, Off-Line, PWM Controller
5-213	UC1852	High Power-Factor Preregulator
5-218	UC1854	High Power Factor Preregulator
5-226	UC1854A	Enhanced High Power Factor Preregulator
5-226	UC1854B	Enhanced High Power Factor Preregulator
5-229	UC1856	Improved Current Mode PWM Controller
5-237	UC1860	Resonant Mode Power Supply Controller
5-245	UC1861	Resonant-Mode Power Supply Controllers
5-245	UC1862	Resonant-Mode Power Supply Controllers
5-245	UC1863	Resonant-Mode Power Supply Controllers
5-245	UC1864	Resonant-Mode Power Supply Controllers
5-245	UC1865	Resonant-Mode Power Supply Controllers
5-245	UC1866	Resonant-Mode Power Supply Controllers
5-245	UC1867	Resonant-Mode Power Supply Controllers
5-245	UC1868	Resonant-Mode Power Supply Controllers
5-251	UC1871	Resonant Fluorescent Lamp Driver
5-256	UC1875	Phase Shift Resonant Controller
5-256	UC1876	Phase Shift Resonant Controller
5-256	UC1877	Phase Shift Resonant Controller
5-256	UC1878	Phase Shift Resonant Controller
5-265	UC1891	Two Stage Power Factor Converter
5-265	UC1892	Two Stage Power Factor Converter
5-265	UC1893	Two Stage Power Factor Converter
5-265	UC1894	Two Stage Power Factor Converter
5-269	UC1901	Isolated Feedback Generator
5-274	UC1903	Quad Supply and Line Monitor
5-281	UC1904	Precision Quad Supply and Line Monitor
5-286	UC1907	Load Share Controller
5-23	UC2524	Advanced Regulating Pulse Width Modulators
5-28	UC2524A	Advanced Regulating Pulse Width Modulators
5-34	UC2525A	Regulating Pulse Width Modulators
5-41	UC2525B	Regulating Pulse Width Modulators
5-47	UC2526	Regulating Pulse Width Monitor
5-54	UC2526A	Regulating Pulse Width Modulator
5-34	UC2527A	Regulating Pulse Width Modulators
5-41	UC2527B	Regulating Pulse Width Modulators
5-62	UC2543	Power Supply Supervisory Circuit
5-62	UC2544	Power Supply Supervisory Circuit
5-67	UC2575-5	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC2575-12	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC2575-15	Simple 1 Amp Step-Down Fixed Voltage Regulators

*Consult Factory

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
5-73	UC2575-ADJ	Simple 1 Amp Step-Down Voltage Regulator
5-67	UC2575HV-5	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC2575HV-12	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-67	UC2575HV-15	Simple 1 Amp Step-Down Fixed Voltage Regulators
5-73	UC2575HV-ADJ	Simple 1 Amp Step-Down Voltage Regulator
5-80	UC2576-5	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC2576-12	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC2576-15	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-87	UC2576-ADJ	Simple 3 Amp Step-Down Voltage Regulator
5-80	UC2576HV-5	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC2576HV-12	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-80	UC2576HV-15	Simple 3 Amp Step-Down Fixed Voltage Regulators
5-87	UC2576HV-ADJ	Simple 3 Amp Step-Down Voltage Regulator
5-94	UC2577-12	Simple Step-Up Fixed Voltage Regulators
5-94	UC2577-15	Simple Step-Up Fixed Voltage Regulators
5-99	UC2577-ADJ	Simple Step-Up Voltage Regulator
6-50	UC2633	Phase Locked Frequency Controller
6-57	UC2634	Phased Locked Frequency Controller
6-61	UC2635	Phased Locked Frequency Controller
6-65	UC2637	Switched Mode Controller for DC Motor Drive
7-11	UC2705	High Speed Power Driver
7-14	UC2706	Dual Output Driver
7-19	UC2707	Dual Channel Power Driver
7-37	UC2724	Isolated Drive Transmitter
7-40	UC2725	Isolated High Side FET Driver
7-44	UC2726	Isolated Drive Transmitter
7-49	UC2727	Isolated High Side IGBT Driver
7-55	UC2730	Thermal Monitor
5-113	UC2823	High Speed PWM Controller
5-119	UC2823A	High Speed PWM Controller
5-119	UC2823B	High Speed PWM Controller
5-127	UC2824	High Speed PWM Controller
5-134	UC2825	High Speed PWM Controller
5-119	UC2825A	High Speed PWM Controller
5-119	UC2825B	High Speed PWM Controller
5-141	UC2828	Current Mode PWM Controller IC

PAGE	PART NUMBER	DESCRIPTION
5-142	UC2832	Precision Low Dropout Linear Controllers
5-142	UC2833	Precision Low Dropout Linear Controllers
5-149	UC2834	High Efficiency Linear Regulator
5-155	UC2835	High Efficiency Regulator Controller
5-155	UC2836	High Efficiency Regulator Controller
5-159	UC2838A	Magnetic Amplifier Controller
5-163	UC2840	Programmable, Off-Line, PWM Controller
5-171	UC2841	Programmable, Off-Line, PWM Controller
5-179	UC2842	Current Mode PWM Controller
5-186	UC2842A	Current Mode PWM Controller
5-179	UC2843	Current Mode PWM Controller
5-186	UC2843A	Current Mode PWM Controller
5-179	UC2844	Current Mode PWM Controller
5-186	UC2844A	Current Mode PWM Controller
5-179	UC2845	Current Mode PWM Controller
5-186	UC2845A	Current Mode PWM Controller
5-192	UC2846	Current Mode PWM Controller
5-192	UC2847	Current Mode PWM Controller
5-199	UC2848	Average Current Mode PWM Controller
5-207	UC2851	Programmable, Off-Line, PWM Controller
5-213	UC2852	High Power-Factor Preregulator
5-218	UC2854	High Power Factor Preregulator
5-226	UC2854A	Enhanced High Power Factor Preregulator
5-226	UC2854B	Enhanced High Power Factor Preregulator
5-229	UC2856	Improved Current Mode PWM Controller
5-237	UC2860	Resonant Mode Power Supply Controller
5-245	UC2861	Resonant-Mode Power Supply Controllers
5-245	UC2862	Resonant-Mode Power Supply Controllers
5-245	UC2863	Resonant-Mode Power Supply Controllers
5-245	UC2864	Resonant-Mode Power Supply Controllers
5-245	UC2865	Resonant-Mode Power Supply Controllers
5-245	UC2866	Resonant-Mode Power Supply Controllers
5-245	UC2867	Resonant-Mode Power Supply Controllers
5-245	UC2868	Resonant-Mode Power Supply Controllers

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
5-251	UC2871	Resonant Fluorescent Lamp Driver
5-256	UC2875	Phase Shift Resonant Controller
5-256	UC2876	Phase Shift Resonant Controller
5-256	UC2877	Phase Shift Resonant Controller
5-256	UC2878	Phase Shift Resonant Controller
5-265	UC2891	Two Stage Power Factor Converter
5-265	UC2892	Two Stage Power Factor Converter
5-265	UC2893	Two Stage Power Factor Converter
5-265	UC2894	Two Stage Power Factor Converter
5-269	UC2901	Isolated Feedback Generator
5-274	UC2903	Quad Supply and Line Monitor
5-281	UC2904	Precision Quad Supply and Line Monitor
5-292	UC2906	Sealed Lead-Acid Battery Charger
5-286	UC2907	Load Share Controller
7-59	UC2950	Half-Bridge Bipolar Switch
6-79	UC3173A	Full Bridge Power Amplifier
6-89	UC3174B	Full-Bridge Power Amplifier
6-89	UC3175B	Full-Bridge Power Amplifier
6-94	UC3176	Full Bridge Power Amplifier
6-94	UC3177	Full Bridge Power Amplifier
6-98	UC3178	Full Bridge Power Amplifier
6-19	UC3517	Stepper Motor Drive Circuit
5-23	UC3524	Advanced Regulating Pulse Width Modulators
5-28	UC3524A	Advanced Regulating Pulse Width Modulators
5-34	UC3525A	Regulating Pulse Width Modulators
5-41	UC3525B	Regulating Pulse Width Modulators
5-47	UC3526	Regulating Pulse Width Monitor
5-54	UC3526A	Regulating Pulse Width Modulator
5-34	UC3527A	Regulating Pulse Width Modulators
5-41	UC3527B	Regulating Pulse Width Modulators
5-62	UC3543	Power Supply Supervisory Circuit
5-62	UC3544	Power Supply Supervisory Circuit
6-26 & 5-106	UC3610	Dual Schottky Diode Bridge
6-28 & 5-108	UC3611	Quad Schottky Diode Array
6-31 & 5-111	UC3612	Dual Schottky Diode

PAGE	PART NUMBER	DESCRIPTION
6-33	UC3620	Switchmode Driver for 3-Ø Brushless DC Motors
6-103	UC3622	Switchmode Driver for 3-Ø Brushless DC Motors
6-107	UC3623	Low Noise Switchmode Driver for 3-Ø Brushless DC Motors
6-39	UC3625	Brushless DC Motor Controller
6-50	UC3633	Phase Locked Frequency Controller
6-57	UC3634	Phased Locked Frequency Controller
6-61	UC3635	Phased Locked Frequency Controller
6-65	UC3637	Switched Mode Controller for DC Motor Drive
6-110	UC3655	Low Saturation, Linear Brushless DC Motor Driver
7-61	UC3657	Triple Tri-State Power Driver
7-65	UC3704	Bridge Transducer Switch
7-11	UC3705	High Speed Power Driver
7-14	UC3706	Dual Output Driver
7-19	UC3707	Dual Channel Power Driver
7-25	UC3708	Dual Non-Inverting Power Driver
7-29	UC3709	Dual High-Speed FET Driver
7-32	UC3710	High Current FET Driver
7-35	UC3711	Dual Ultra High-Speed FET Driver
6-71	UC3717	Stepper Motor Drive Circuit
6-115*	UC3717A	Stepper Motor Drive Circuit
*	UC3722	Five-Channel Programmable Current Switch
7-37	UC3724	Isolated Drive Transmitter
7-40	UC3725	Isolated High Side FET Driver
7-44	UC3726	Isolated Drive Transmitter
7-49	UC3727	Isolated High Side IGBT Driver
7-55	UC3730	Thermal Monitor
6-123	UC3770A	High Performance Stepper Motor Drive Circuit
6-123	UC3770B	High Performance Stepper Motor Drive Circuit
5-113	UC3823	High Speed PWM Controller
5-119	UC3823A	High Speed PWM Controller
5-119	UC3823B	High Speed PWM Controller
5-127	UC3824	High Speed PWM Controller
5-134	UC3825	High Speed PWM Controller
5-119	UC3825A	High Speed PWM Controller
5-119	UC3825B	High Speed PWM Controller
5-141	UC3828	Current Mode PWM Controller IC
5-142	UC3832	Precision Low Dropout Linear Controllers
5-142	UC3833	Precision Low Dropout Linear Controllers
5-149	UC3834	High Efficiency Linear Regulator

*Consult Factory

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
5-155	UC3835	High Efficiency Regulator Controller
5-155	UC3836	High Efficiency Regulator Controller
5-159	UC3838A	Magnetic Amplifier Controller
5-163	UC3840	Programmable, Off-Line, PWM Controller
5-171	UC3841	Programmable, Off-Line, PWM Controller
5-179	UC3842	Current Mode PWM Controller
5-186	UC3842A	Current Mode PWM Controller
5-179	UC3843	Current Mode PWM Controller
5-186	UC3843A	Current Mode PWM Controller
5-179	UC3844	Current Mode PWM Controller
5-186	UC3844A	Current Mode PWM Controller
5-179	UC3845	Current Mode PWM Controller
5-186	UC3845A	Current Mode PWM Controller
5-192	UC3846	Current Mode PWM Controller
5-192	UC3847	Current Mode PWM Controller
5-199	UC3848	Average Current Mode PWM Controller
5-207	UC3851	Programmable, Off-Line, PWM Controller
5-213	UC3852	High Power-Factor Preregulator
5-218	UC3854	High Power Factor Preregulator
5-226	UC3854A	Enhanced High Power Factor Preregulator
5-226	UC3854B	Enhanced High Power Factor Preregulator
5-229	UC3856	Improved Current Mode PWM Controller
5-237	UC3860	Resonant Mode Power Supply Controller
5-245	UC3861	Resonant-Mode Power Supply Controllers
5-245	UC3862	Resonant-Mode Power Supply Controllers
5-245	UC3863	Resonant-Mode Power Supply Controllers
5-245	UC3864	Resonant-Mode Power Supply Controllers
5-245	UC3865	Resonant-Mode Power Supply Controllers
5-245	UC3866	Resonant-Mode Power Supply Controllers
5-245	UC3867	Resonant-Mode Power Supply Controllers
5-245	UC3868	Resonant-Mode Power Supply Controllers
5-251	UC3871	Resonant Fluorescent Lamp Driver
5-256	UC3875	Phase Shift Resonant Controller
5-256	UC3876	Phase Shift Resonant Controller
5-256	UC3877	Phase Shift Resonant Controller
5-256	UC3878	Phase Shift Resonant Controller
5-265	UC3891	Two Stage Power Factor Converter
5-265	UC3892	Two Stage Power Factor Converter
5-265	UC3893	Two Stage Power Factor Converter
5-265	UC3894	Two Stage Power Factor Converter
5-269	UC3901	Isolated Feedback Generator
5-274	UC3903	Quad Supply and Line Monitor
5-281	UC3904	Precision Quad Supply and Line Monitor
5-292	UC3906	Sealed Lead-Acid Battery Charger
5-286	UC3907	Load Share Controller
7-69	UC5170C	Octal Line Driver
7-73	UC5171	Octal Line Driver
7-77	UC5172	Octal Line Driver
7-81	UC5180C	Octal Line Receiver
7-84	UC5181C	Octal Line Receiver
7-87	UC5601	SCSI Active Terminator
7-91	UC5602	SCSI Active Terminator
7-96	UC5603	9-Line SCSI Active Terminator
7-101	UC5661	Ethernet Coaxial Impedance Monitor
5-299	UC7501	Primary Side Controller
5-300	UC7502	Error Signal Isolator
5-299	UC7503	Primary Side Controller
*	UC7805	Three Terminal Fixed Voltage Positive Regulators
*	UC7812	Three Terminal Fixed Voltage Positive Regulators
*	UC7815	Three Terminal Fixed Voltage Positive Regulators
*	UC7905	Three Terminal Fixed Voltage Negative Regulators
*	UC7912	Three Terminal Fixed Voltage Negative Regulators
*	UC7915	Three Terminal Fixed Voltage Negative Regulators
5-301	UC19431	Precision Adjustable Shunt Regulator
5-306	UC19432	Precision Analog Controller
5-301	UC29431	Precision Adjustable Shunt Regulator
5-306	UC29432	Precision Analog Controller
5-301	UC39431	Precision Adjustable Shunt Regulator
5-306	UC39432	Precision Analog Controller
5-312	UCC1570	Low Power Pulse Width Modulator
5-319	UCC1800	Low-Power BiCMOS Current-Mode PWM

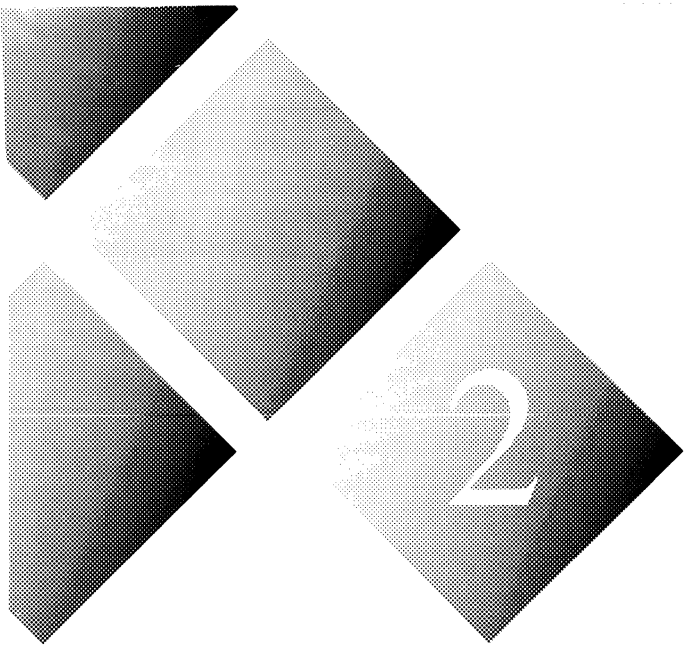
*Consult Factory

PART NUMBER INDEX

PAGE	PART NUMBER	DESCRIPTION
5-319	UCC1801	Low-Power BiCMOS Current-Mode PWM
5-319	UCC1802	Low-Power BiCMOS Current-Mode PWM
5-319	UCC1803	Low-Power BiCMOS Current-Mode PWM
5-319	UCC1804	Low-Power BiCMOS Current-Mode PWM
5-319	UCC1805	Low-Power BiCMOS Current-Mode PWM
5-323	UCC1806	Low Power, Dual Output, Current Mode PWM Controller
5-326	UCC1810	Low-Power BiCMOS Dual Current-Mode PWM
5-309	UCC183-0	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC183-3	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC183-5	Low Drop Out 3 Ampere Linear Regulator Family
5-327	UCC1883	Micropower Peak Current Mode Controller
5-337	UCC1885	Micropower Secondary Regulation IC
5-312	UCC2570	Low Power Pulse Width Modulator
5-319	UCC2800	Low-Power BiCMOS Current-Mode PWM
5-319	UCC2801	Low-Power BiCMOS Current-Mode PWM
5-319	UCC2802	Low-Power BiCMOS Current-Mode PWM
5-319	UCC2803	Low-Power BiCMOS Current-Mode PWM
5-319	UCC2804	Low-Power BiCMOS Current-Mode PWM
5-319	UCC2805	Low-Power BiCMOS Current-Mode PWM
5-323	UCC2806	Low Power, Dual Output, Current Mode PWM Controller

PAGE	PART NUMBER	DESCRIPTION
5-326	UCC2810	Low-Power BiCMOS Dual Current-Mode PWM
5-309	UCC283-0	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC283-3	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC283-5	Low Drop Out 3 Ampere Linear Regulator Family
5-327	UCC2883	Micropower Peak Current Mode Controller
5-337	UCC2885	Micropower Secondary Regulation IC
5-312	UCC3570	Low Power Pulse Width Modulator
5-319	UCC3800	Low-Power BiCMOS Current-Mode PWM
5-319	UCC3801	Low-Power BiCMOS Current-Mode PWM
5-319	UCC3802	Low-Power BiCMOS Current-Mode PWM
5-319	UCC3803	Low-Power BiCMOS Current-Mode PWM
5-319	UCC3804	Low-Power BiCMOS Current-Mode PWM
5-319	UCC3805	Low-Power BiCMOS Current-Mode PWM
5-323	UCC3806	Low Power, Dual Output, Current Mode PWM Controller
5-326	UCC3810	Low-Power BiCMOS Dual Current-Mode PWM
5-309	UCC383-0	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC383-3	Low Drop Out 3 Ampere Linear Regulator Family
5-309	UCC383-5	Low Drop Out 3 Ampere Linear Regulator Family
5-327	UCC3883	Micropower Peak Current Mode Controller
5-337	UCC3885	Micropower Secondary Regulation IC

*Consult Factory



General Information


INTEGRATED
CIRCUITS
UNITRODE

PRODUCT CLASSIFICATION STATUS

The following definitions apply to describe U.I.C.C.'s current product production status. U.I.C.C. also reserves the right to make changes without further notice in order to improve design performance, reliability, or manufacturability.

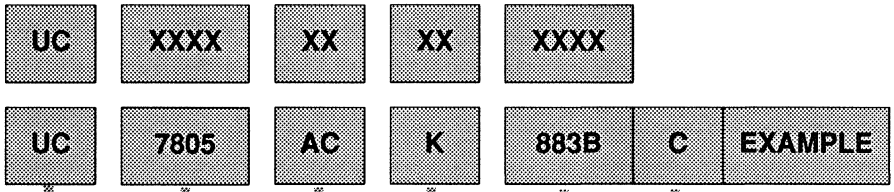
CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheet	First Production	Supplementary data may be published at a later date. U.I.C.C. reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product in Full Production

This databook contains complete data and applications information about Unitrode Linear Integrated Circuits for industrial and military applications. It includes all our latest new products including products that will be introduced throughout the year 1993.

For more information about any new products or any of U.I.C.C. service capabilities, please call, write or fax.

GENERAL INFORMATION

PART NUMBER DESIGNATORS



Compliant "C" Indicator Per MIL-STD-883.

PREFIX
"UC" Linear Integrated Circuits

SCREEN/PROCESSING OPTIONS
883 - MIL-STD-883 Class B
JAN - MIL-M-38510 (Integrated Circuits)
SMD - STD Military Drawing (DESC)

PART NUMBER
*Generic P/N's (See Data Sheets For Descriptions)
*5 Digit In-House Number To Spec. Control Drawings

PACKAGE OPTIONS

Letter Designator	Package Type
N	Plastic Molded Dip
J	Glass-Sealed Ceramic DIP
D	14 Pin Narrow Body SO (150 mL)
DP	16 Pin Narrow Body (150 mL) Power SO
DW	16/20 Pin Wide Body SO Surface Mount (300 mL)
DWP	28 Pin Wide Body Power SO
L	Ceramic Leadless Chip Carrier
Q, QP	Plastic Molded Quad PLCC
V, VH	15 Pin Power SIP
H	TO-39 Metal Can
K	TO-3 Steel-Base Power
T	TO-220 Plastic Power
SP	Ceramic Power
G	TO-257 Hermetic (TO-220 Style)
IG	TO-257 Hermetic Isolated Tab
Z	16 Pin Power ZIP

OPTIONAL GRADES
A - Improved Version
C- "Commercial " Temperature Range

For More Information See Packaging Section

INTEGRATED CIRCUITS
UNITRODE

QUALITY STATEMENT

Since its founding, Unitrode Integrated Circuits Corp. (U.I.C.C.) has structured its development to fully respond to customer requirements in areas of quality and overall product assurance, with particular emphasis on enhanced design and reliability.

As part of its total quality planning, U.I.C.C. has progressed through the traditional techniques of control by appraisal to a more mutually satisfying statistically based process monitoring. However, immature process nodes may still require the use of universally accepted sampling plans, such as those referenced in MIL-STD-105 and MIL-M-38510.

UNITRODE INTEGRATED CIRCUITS REGISTERED AS
ISO 9001 FIRM (Registration Number M667)

In the fall of 1992, Unitrode Integrated Circuits Corporation (U.I.C.C.) announced that it achieved IS/ISO 9001/EN 29001 Registration. Adopted in 1987 by the International Organization for Standardization in Geneva, Switzerland, the ISO 9000 quality system was developed in order to establish an international standard of quality systems--from design of its product through shipment. Therefore, when a firm is registered to meet ISO 9000, customers all over the world are assured that the firm is adhering to very specific quality standards.

U.I.C.C. attributes the ISO 9001 achievement in great part to its Total Quality Excellence (TQE) process, designed entirely by a team of employees representing all levels of the organization. The theme of U.I.C.C.'s quality program, "Building Customer Loyalty", focuses on internal and external customer satisfaction.

nsai

I.S./ISO 9001/EN 29001

TOTAL QUALITY EXCELLENCE

A key element of the Company's strategy and an important factor in its success has been its focus on customer satisfaction. Everything the Company does is aimed at providing its customers with the highest possible levels of quality, reliability and technical support.

Quality, Reliability and Innovation

Quality and reliability are the hallmarks of all U.I.C.C. products - standards of excellence are woven tightly into the Company's corporate fabric, implemented through a Total Quality Excellence process which permeates everything the Company does.

Total Quality Excellence - TQE - impacts each and every department, each and every activity, and each and every product — from initial concept to end-use installation and operation.

Continuous Improvement

The aim of the TQE process is continuous improvement — it is a never ending search for ways to improve everything the Company is and does, and a pledge to ultimately translate improvements into better products and services for customers. For example, goals include:

- improved designs that meet the broadest spectrum of application needs;
- improved translation of customer requirements into actual product performance characteristics;
- improved understanding of process capabilities to improve the product introduction process;
- higher productivity, less scrap and rework, and lower production costs, all which can be passed along to customers.

Employee Teams

To make continuous improvement a reality, through total involvement, there are more than 20 employee teams focused on product, process and service improvement. Using Statistical Process Control methods as the quantitative tools to facilitate the process, these teams help make it possible for the Company to attain the milestones on the road of continuous improvement.

The entire process was put together and is now operated by the employees; its initial structure was developed by an employee team; issues are identified by staff members and teams are formed by those who feel thay can make a contribution to the effort.

The concern for quality extends beyond the Company itself. Total Quality Excellence includes suppliers as well as U.I.C.C. employees. In fact, U.I.C.C. provides a TQE education program for vendors' personnel. Again, the focus is on the customer — the improvement of products and services in any and all ways possible.

A Living Process

TQE is a flexible, living process that was created and has been nurtured by the people who are the Company. It is an expression of their drive to be the best.

And for U.I.C.C. customers, it is an assurance of superior products; designed, made, sold and supported by people who care about them.

GENERAL INFORMATION

Quality

Process improvement has become an aggressive daily pursuit in manufacturing. Just meeting specification is no longer good enough. U.I.C.C.'s goal is to achieve a 6σ process.

Simply; many benefits to the customer have been realized in the form of on-time-delivery, superior quality and unprecedented levels of sustained reliability. Organizationally, a "total commitment" to quality has manifested itself in the form of:

- Improved customer satisfaction
- Improved designs
- Known process capabilities
- Increased yields
- Improved product flow
- Reduction in quality costs such as scrap and rework
- Prevention orientation and quality consciousness
- Reduction in operating costs

U.I.C.C.'s unique self-auditing approach makes certain quality ownership is an intrinsic part of the manufacturing community with no one faction having full responsibility. Documentation at U.I.C.C. has been developed to truly reflect a "Real Time" status through master matrixing and planning whereas design, fabrication, assembly and test and their many detailed process steps are tied together relationally.

Reliability assurance at U.I.C.C. has specific goals to demonstrate product reliability of the various functional families that make up this primarily bipolar product base. It is important to note the existence of feedback to design and process engineering that ensures all products receive continuing reviews, thus enhancing even the most mature family of products.

GENERAL INFORMATION

Quality

QUAL/QCI FLOW FOR JANB, 883B MIL-STD-883 METHOD 5005

GROUP A ELECTRICALS
-55°, +25°, +125°, +150°C

GROUP B

SUBGROUP 2
Resistance To Solvents

SUBGROUP 3
Solderability

SUBGROUP 5
Bond Strength

GROUP C

SUBGROUP 1
Steady State Life
End Point Electricals

GROUP D

SUBGROUP 1
Physical Dimensions

SUBGROUP 2
Lead Integrity
Seal (Fine And Gross)

SUBGROUP 3
Thermal Shock
Temperature Cycling
Moisture Resistance
Seal (Fine And Gross)
Visual Examination
End Point Electricals

SUBGROUP 4
Mechanical Shock
Vibration, Variable Frequency
Constant Acceleration
Seal (Fine And Gross)
Visual Examination
End Point Electricals

SUBGROUP 5
Salt Atmosphere
Seal (Fine and Gross)
Visual Examination

SUBGROUP 6
Internal Water Vapor Content

SUBGROUP 7
Adhesion of Lead Finish

SUBGROUP 8
Lid Torque

GROUP E
RADIATION HARDNESS ASSURANCE (WHEN APPLICABLE)

SUBGROUP 1
Neutron Irradiation
End Point Electricals

SUBGROUP 2
Steady State Total Dose Irradiation
End Point Electricals

SUBGROUP 3
Transient Ionizing Irradiation
End Point Electricals

Note: Unitrode Integrated Circuits also performs testing to source control drawings for Class S devices in accordance with MIL-STD-883

QUALIFICATION FLOW FOR COMMERCIAL - INDUSTRIAL DEVICES

Non-Hermetic

SUBGROUP 1
Group A Electricals -40°, 0°, +25°, +70°, +85° C, Visual Exam

SUBGROUP 2
Humidity Life (85°C/85%^{RH})
1000 Hours
Post Electricals

SUBGROUP 3
Temperature Cycling (1000 Cycles)
Post Electricals

SUBGROUP 4
Thermal Shock (500 cycles)
Post Electricals

SUBGROUP 5
Autoclave 96 Hours
2 Atmospheres
Post Electricals

SUBGROUP 6
Electrostatic Sensitivity Discharge
Post Electricals

Hermetic

SUBGROUP 1
Group A Electricals -55°, +25°, +125°C, Visual Exam

SUBGROUP 2
Thermal Shock (500 Cycles)
Seal (Fine and Gross)
Post Electricals
External Visual

SUBGROUP 3
Temperature Cycling (1000 Cycles)
Seal (Fine and Gross)
Post Electricals
External Visual

SUBGROUP 4
Steady State Life
1000 Hours

SUBGROUP 5
Constant Acceleration
Seal (Fine and Gross)
Post Electricals

SUBGROUP 6
Electrostatic Sensitivity Discharge

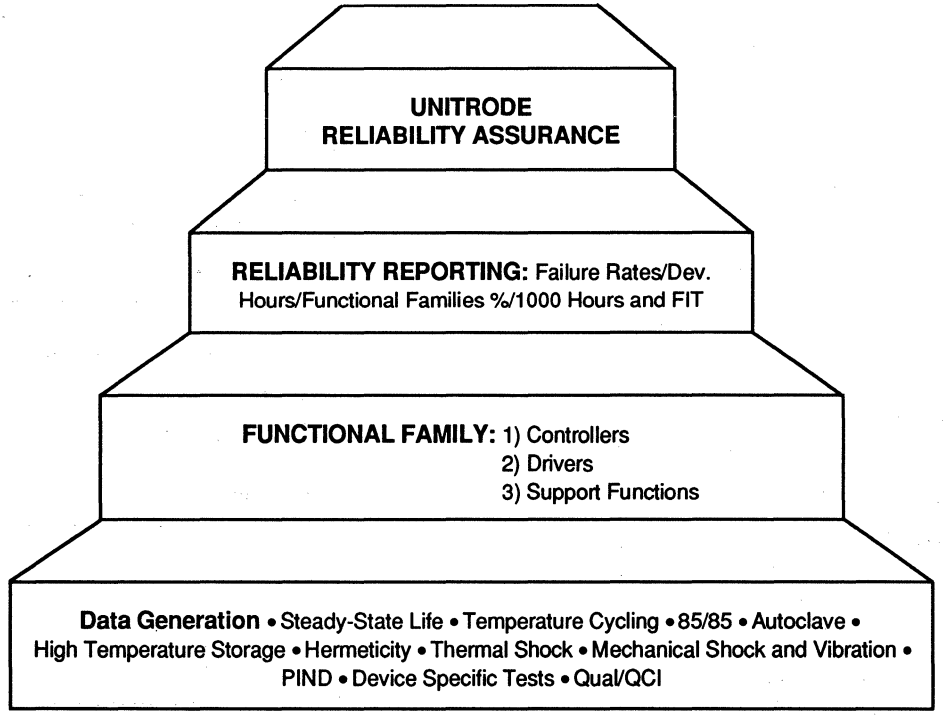
GENERAL INFORMATION

Quality

Should failure occur either in the field or during the course of reliability testing, in-depth failure analysis is performed to identify and understand the failure mechanism(s) involved. Immediate feedback to design or process for the purpose of corrective action is systematically accomplished.

Levels of long-term device reliability, through the accumulation of millions of hours of testing at accelerated temperatures have demonstrated 15 fit or lower failure rates within a functional family. With the ever-growing demand for greater system reliability, this is a major factor.

U.I.C.C. has planned and developed reliability goals for the decade of the 90's that realistically test the technology.



New Quality Products from U.I.C.C.

PULSE WIDTH MODULATORS

Part Number	Description	Page Number
UCC3570	High Performance Voltage Mode PWM	5-312
UCC3802	High Frequency BICMOS PWM 3842 Type	5-319
UCC3803	High Frequency BICMOS PWM 3842 Type	5-319
UCC3804	High Frequency BICMOS PWM 3842 Type	5-319
UCC3805	High Frequency BICMOS PWM 3842 Type	5-319
UCC3806	High Frequency BICMOS PWM 3846 Type	5-323
UCC3810	Dual BICMOS PWM	5-326
UC3824	Complementary Output UC1825	5-127
UC3828	Enhanced Current Mode PWM	5-141
UC3848	Average Current Mode PWM	5-199
UCC3856	High Performance Current Mode PWM	5-229
UCC3883	ISDN Micro Power PWM	5-327
UCC3885	ISDN Micro Power PWM	5-337

RESONANT CONTROLLERS

Part Number	Description	Page Number
UC3866	ZVS Resonant Controller	5-245
UC3875	Phase Shift Resonant PWM	5-256

SPECIAL FUNCTION CIRCUITS

Part Number	Description	Page Number
UC3612	Dual Schottky Diode Array	5-111, 6-31
UC3852	Electronic Ballast Power Factor	5-213
UC3871	Fluorescent Lamp Driver	5-251
UC5661	Ethernet Coaxial Impedance Monitor	7-101

Note: Only commercial part numbers are indicated - see military section for military versions

INTEGRATED CIRCUITS
UNITRODE

New Quality Products from U.I.C.C.

MOTOR CONTROLLERS/DRIVERS

INTERFACE CIRCUITS

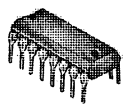
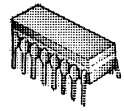
HIGH POWER DRIVERS

New Quality Products from U.I.C.C.

POWER SUPPLY SUPPORT CIRCUITS

General Information

PACKAGE CROSS-REFERENCE CHART

								
	PLASTIC DIP	**CERAMIC DIP**	**MULTIWATT**	**PLCC**	**LCC**	**SOIC**	**TO-3***	**TO-220**
UNITRODE	N	J	V	Q, QP	L	D, DP, DW, DWP	K	T
Linear Tech	N, N-8	J, J-8		--	L	S, S-8	K	T
Cherry	N	J	V	FN	--	D, DW	--	T
SGS - Thompson	B, N, P	--	V	--	--	D	K	--
Silicon General	M, N, W	J, Y		Q	L	D, DW, DWW	K	P
Texas Instruments	N, NT, NW, P	J, JG	V	FN	FK	D, DB, DW	K	KC, KV
Signetics	N	F, FE		A	G	D	--	U
National	N, N-8, N-14	J, J-8, J-14	V	Y	E	M	K	T
Motorola	N, P, P1, P2	J, J-8, L, U		FN	--	D, DW	K	KC
Fairchild	T, P	D, R		Q	L	S	K	U
Sprague	A, M, B	R		EP	EK, EL	L, LB, LW	V	Z
Micro Linear	P	J		Q	L	S	--	--
Samsung	N	J		PL	L	D	M	T
Philips	N	F		A	--	D	--	--
Seagate	N	J		--	--	D	K	T
Siliconix	J, N	K, Q		N, P	--	Y	--	--
Teledyne	P	J		L	N	O	--	--

*Consult factory for availability.

INTEGRATED CIRCUITS
UNITRODE

Die And Wafers

DESCRIPTION

Unitrode Integrated Circuits Corp., U.I.C.C., offers most of its products described in this data book in die and/or wafer form. Products include all Pulse Width Modulators (PWMs), Motor Controls, Low-Drop Regulators, fixed, and adjustable industry standard Voltage Regulators, Power Drivers and Switches, Active Terminators, and Special Function Circuits. Most U.I.C.C. products are designed with military temperature range operation capability.

U.I.C.C. die utilize linear bipolar technology featuring tight beta control and resistor matching techniques. Also, other enhancements used implement thin film resistor and Schottky process, as well as in-house epitaxial capability for unique voltage flexibility. All products are protected by CVD Oxide plus Nitride layers to make a sandwich passivation system that offers superior coverage over all junctions.

Die thicknesses vary by product type, however, they fall into the catagories; 12 mils ± 1 mil, or 15 mils ± 1 mil. Interconnects are an alloy of copper (2%) and aluminum (to reduce possibility of metal migration). Backside metallization is Titanium - Nickel - Silver, suitable with various common eutectic and thermal epoxy mount- down techniques used today.

TESTING

All products are tested at two separate points. 1) In-line probing and 2) Final test probing.

Final test probe utilizes state-of-the-art high speed/power ATE equipment. Die are 100% tested to low power DC limits.

INSPECTION

U.I.C.C. performs visual inspections on military grade die to MIL-STD-750B, Method, 2072 and to MIL-STD-883C Method 2010, condition A or B, or to customer supplied requirements.

Die can be supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils (generic 4 inch diameter).

ORDERING INFORMATION

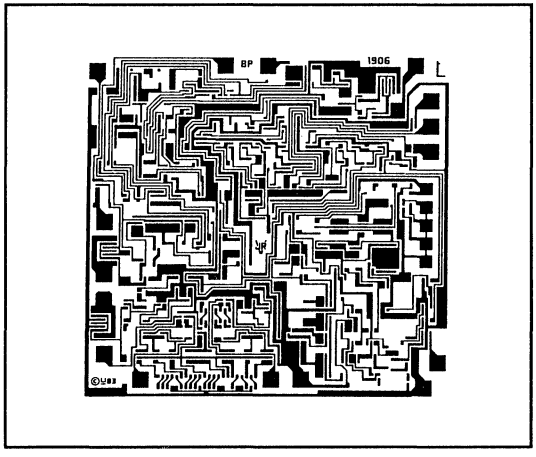
PART NUMBER = UCXXXX: CHIP WFR

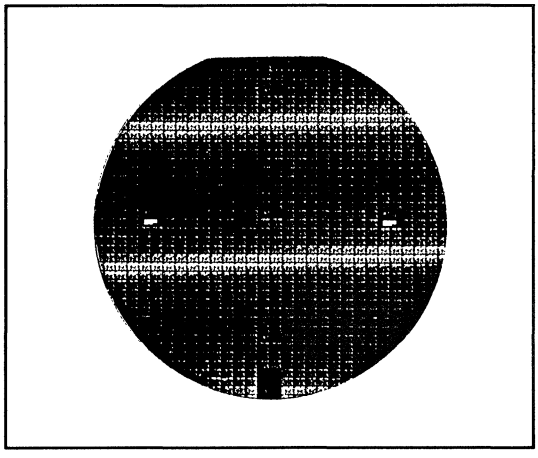
\+

CHIP ORDER

\+

WAFER ORDER





UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL (603) 424-2410 • FAX (603) 424-3460


INTEGRATED
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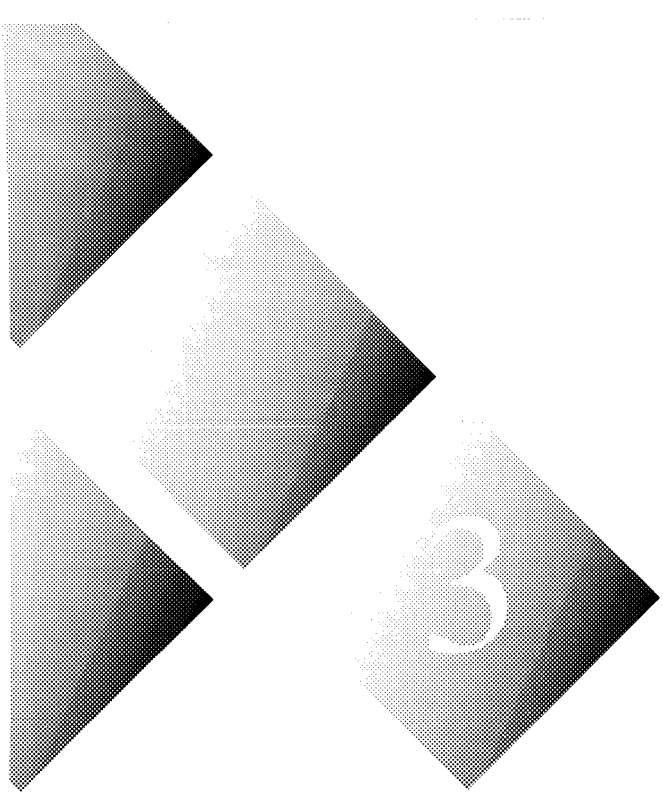
UNITRODE

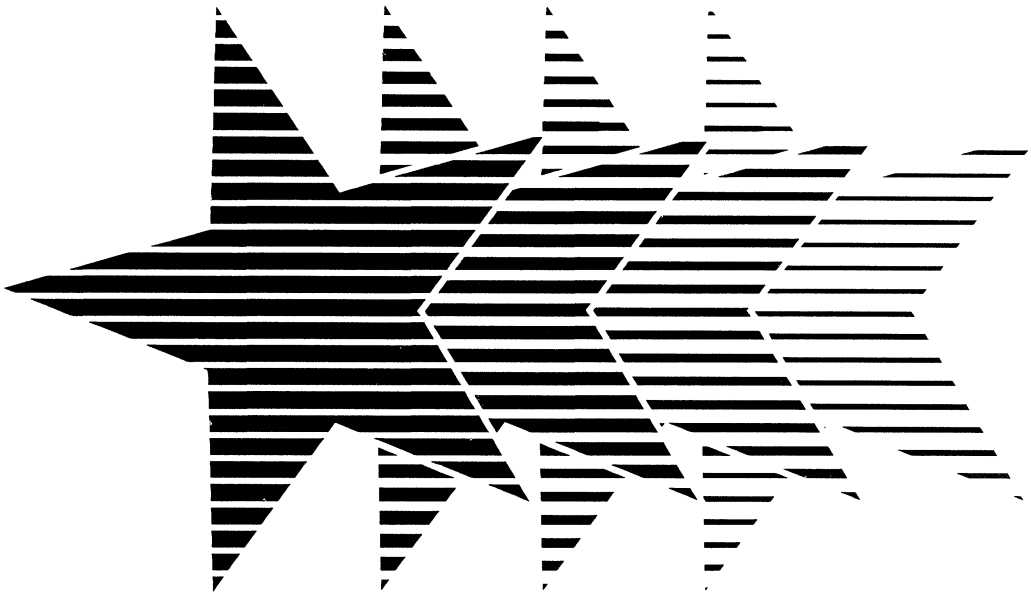


3

Military/Aerospace Products


INTEGRATED
CIRCUITS
UNITRODE

INTEGRATED CIRCUITS
UNITRODE



3

Military/Aerospace Products Selection Guide

MILITARY/AEROSPACE PRODUCTS

U.I.C.C. has been committed to producing military/aerospace and high reliability products for several years and continues to support this key market segment. Our product offering includes:

- STANDARD MILITARY DRAWING (SMD) - Conformance to Class B process requirements per the SMD selected item drawings.
- SCD-CLASS S - conformance to all Class S process requirements of MIL-STD-883 and individual customer source control documents.
- SCD - CLASS B - Conformance to Class B process requirements of MIL-STD-883 and individual customer source control documents
- JAN-LEVEL B - full compliance to MIL-M-38510 JAN program and QPL listings as published by DESC.

U.I.C.C. has had DESC facility certification continuously since November 1985. This certification allows us to produce JAN Class B linear microcircuits for the military marketplace.

U.I.C.C. has been a leader in producing linear ICs to customers' Class S specifications for the last several years. Our abilities in the area include all processing standards of Class S, as well as an extensive library of radiation data on our most popular devices. Our superior design support and customer service make us the best choice for customers with Class S requirements.

JAN PRODUCT LINE

Unitrode Integrated Circuits Corporation presently has DESC line certification to MIL-M-38510 to produce Jan Class B linear microcircuits. Unitrode is the originator of the 702 current mode PWM slash sheet (UC1846/UC1847) and in January of 1990 received JAN qualification.

In a continued effort to meet and produce the highest military grade devices, Unitrode Integrated Circuits reviews all existing slash sheets applicable to our product base in the effort to either add device types or develop new slash sheets for industry use.

Unitrode Integrated Circuits also has lab suitability to perform MIL-STD-883 method 5004 and 5005 screening/QUAL/QCI issued by DESC, with the exception of internal water vapor content and vibration variable frequency. In addition we have full self-auditing programs to ensure compliance to all specifications. Our SPC program has enhanced the process of all product through continuous improvement teams whose purpose is to reduce variation in the process.

Unitrode Integrated Circuits is committed to producing military grade linear monolithic devices in full compliance to MIL-M-38510. MIL-STD-883, SMD and SCD requirements and at all times focusing on quality and reliability enhancements.

Military/Aerospace Products

STANDARDIZED MILITARY DRAWINGS (SMDs) LISTING U.I.C.C. AS AN APPROVED SOURCE OF SUPPLY

LINEAR VOLTAGE REGULATORS*	GENERIC DEVICE	TYPE	SMD PART NUMBER
	117AG/883BC	Positive Adjustable Reg.	7703405TA
	117AH/883BC	Positive Adjustable Reg.	7703405XA
	117AIG/883BC	Positive Adjustable Reg.	7703405UA
	117AK/883BC	Positive Adjustable Reg.	7703405YA
	117G/883BC	Positive Adjustable Reg.	7703401TA
	117H/883BC	Positive Adjustable Reg.	7703401XA
	117IG/883BC	Positive Adjustable Reg.	7703401UA
	117K/883BC	Positive Adjustable Reg.	7703401YA
	117L/883BC	Positive Adjustable Reg.	77034012A
	137AG/883BC	Negative Adjustable Reg.	7703406TA
	137AH/883BC	Negative Adjustable Reg.	7703406XA
	137A3IG/883BC	Negative Adjustable Reg.	7703406UA
	137AK/883BC	Negative Adjustable Reg.	7703406YA
	137G/883BC	Negative Adjustable Reg.	7703403TA
	137H/883BC	Negative Adjustable Reg.	7703403XA
	137IG/883BC	Negative Adjustable Reg.	7703403UA
	137K/883BC	Negative Adjustable Reg.	7703403YA
	150AK/883BC	Positive Adjustable Reg.	5962-8767502XA
	150K/883BC	Positive Adjustable Reg.	5962-8767501XA
	1834J/883BC	Low Dropout Regulator	5962-8774201EA
	7805AG/883BC	Positive 5V Reg.	5962-8778201TA
	7805AIG/883BC	Positive 5V Reg.	5962-8778201UA
	7805AK/883BC	Positive 5V Reg.	5962-8778201YA
	7812AG/883BC	Positive 12V Reg.	5962-8777601TA
	7812AIG/883BC	Positive 12V Reg.	5962-8777601UA
	7812AK/883BC	Positive 12V Reg.	5962-8777601YA
	7815AG/883BC	Positive 15V Reg.	5962-8855301TA
	7815AIG/883BC	Positive 15V Reg.	5962-8855301UA
	7815AK/883BC	Positive 15V Reg.	5962-8855301YA

*Consult factory for availability

Military/Aerospace Products

STANDARDIZED MILITARY DRAWINGS (SMDs) LISTING U.I.C.C. AS AN APPROVED SOURCE OF SUPPLY (Cont'd)

LINEAR VOLTAGE REGULATORS*	GENERIC DEVICE	TYPE	SMD PART NUMBER
	7905AG/883BC	Negative 5V Reg.	5962-8874601TA
	7905AIG/883BC	Negative 5V Reg.	5962-8874601UA
	7905AK/883BC	Negative 5V Reg.	5962-8874601YA
	7912AG/883BC	Negative 12V Reg.	5962-8874701TA
	7912AIG/883BC	Negative 12V Reg.	5962-8874701UA
	7912AK/883BC	Negative 12V Reg.	5962-8874701YA
	7915AG/883BC	Negative 15V Reg.	5962-8874801TA
	7915AIG/883BC	Negative 15V Reg.	5962-8874801UA
	7915AK/883BC	Negative 15V Reg.	5962-8874801YA
PULSE WIDTH MODULATORS	1823J/883B	High Speed PWM	5962-8990501EA
	1823L/883B	High Speed PWM	5962-89905012A
	1524J/883B	PWM	7802801EA
	1524AJ/883BC	PWM	5962-8764502EA
	1525AJ/883BC	PWM	5962-8951103EA
	1527AJ/883BC	PWM	5962-8951104EA
	1525AJ/883BC	PWM	5962-8951101EA
	1527AJ/883BC	PWM	5962-8951102EA
	1526AJ/883BC	PWM	8551502VA
	1526AJ/883BC	PWM	8551501VA
	1825J/883BC	High Speed PWM	5962-8768101EA
	1825L/883BC	High Speed PWM	5962-87681012A
	1842J/883BC	Current Mode PWM	5962-8670401PA
	1843J/883BC	Current Mode PWM	5962-8670402PA
	1844J/883BC	Current Mode PWM	5962-8670403PA
	1845J/883BC	Current Mode PWM	5962-8670404PA
	1846J/883BC	Current Mode PWM	5962-8680601EA
	1847J/883BC	Current Mode PWM	5962-8680602EA

*Consult factory for availability

STANDARDIZED MILITARY DRAWINGS (SMDs) LISTING U.I.C.C. AS AN APPROVED SOURCE OF SUPPLY (Cont'd)

POWER SUPERVISORY CIRCUITS	GENERIC DEVICE	TYPE	SMD PART NUMBER
	1543J/883BC	Power Supply Supervisory	5962-8774001EA
	1544J/883BC	Power Supply Supervisory	5962-8774002VA
	1903J/883BC	Quad Supply + Line Monitor	5962-8869701VA
	1903L/883BC	Quad Supply + Line Monitor	5962-88697012A
POWER DRIVERS	L293DSP/883B	4-Channel Driver	5962-9235001MEA
	1706J/883BC	Dual Output Driver	5962-8961101EA
	1707J/883BC	Dual Channel Power Driver	5962-8761901EA
	195H/883BC	Smart Power Transistor	5962-8777801XA
	195K/883BC	Smart Power Transistor	5962-8777801XA
OTHER FUNCTIONS	1611J/883BC	Quad Schottky Array	5962-8995701EA
	1633J/883	Brushless DC Motor Cont.	5962-9168901MEX
	1625J/883	Phase Lock Controller	5962-9098701MEX
	1637J/883BC	PWM DC Servo Control	5962-8995701VA
	1838AJ/883B	Magnetic Amplifier Circuit	5962-8989901MEA
	1864J/883	Resonant Mode Cont.	5962-9203101MEX
	1901J/883B	Iso. Feedback Generator	5962-8944101CA

Military/Aerospace Products

PACKAGE AVAILABILITY

PART NO. DESIGNATOR	PACKAGE TYPE*	TYP. θJC, °C/W	TYPE θJA °C/W
G	TO-257 Non-Isolated	3.2 (1)	N/A
IG	TO-257 Isolated	3.7 (2)	N/A
H	TO-5	20	130
J	Ceramic DIL 8-pin 14-Pin 16-Pin 18-Pin	 40 30 30 30	 130 80 80 75
SP	Side-Brazed Power 16-pin 24-pin	 5 TBD	 65 45 (3) TBD
K	TO-3	3 (2) 6 (4)	35
L	Ceramic Leadless Chip Carrier (CLCC)	15	70

*Consult factory

NOTES:
1. This data is Junction to Tab
2. Junction to Bottom Plate
3. With finned heat sink
4. Junction to top plate

Military/Aerospace Products

Military Die Capability

Unitrode's military product offering includes all catalog circuits in unencapsulated form. Unencapsulated (chips) are supplied screened to MIL-STD-883B, method 2010, conditional A or B. Product is electrically tested at ambient room temperature. Shipment of this product is in individual waffle packs or as complete wafers.

Radiation Tolerant Products

Unitrode recognizes the increasing market demand for radiation tolerant and radiation hardened high reliability products. Because of this, we - in conjunction with customers - have characterized our key products. Full radiation data reports are available on the following products.

Pulse Width Modulators	Linear Regulators	Power FET Drivers
UC1524A	UC7805	UC1711
UC1526	UC7905	UC1707
UC1526A		
UC1825		
UC1842		
UC1843		Low Drop Regulators
UC1844		UC1834
UC1845		UC1835/36

Below is a summary of radiation data U.I.C.C. has collected:

Unitrode Bipolar Junction Isolated Process

Device	Total Dose Rad (si)	Neutron Damage N/cm2	Dose Rate Rad (si)/sec.
UC1707J		2.9E12	2.0E5
UC1711J		1E13	8.77E9
UC1825J	4E5	3E12	
UC1834J	1E6		
UC1836J	6E4		
UC1840J			1.7E10
UC1842J			1.7E10
UC1845J	1E6		
UC3825N	3E5		
UC7805K		2E13	
UC7815K		2E13	
UC7905K	1E6		

Note: Radiation levels represented are from independent customer test results.


INTEGRATED
CIRCUITS
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4

Automotive Products


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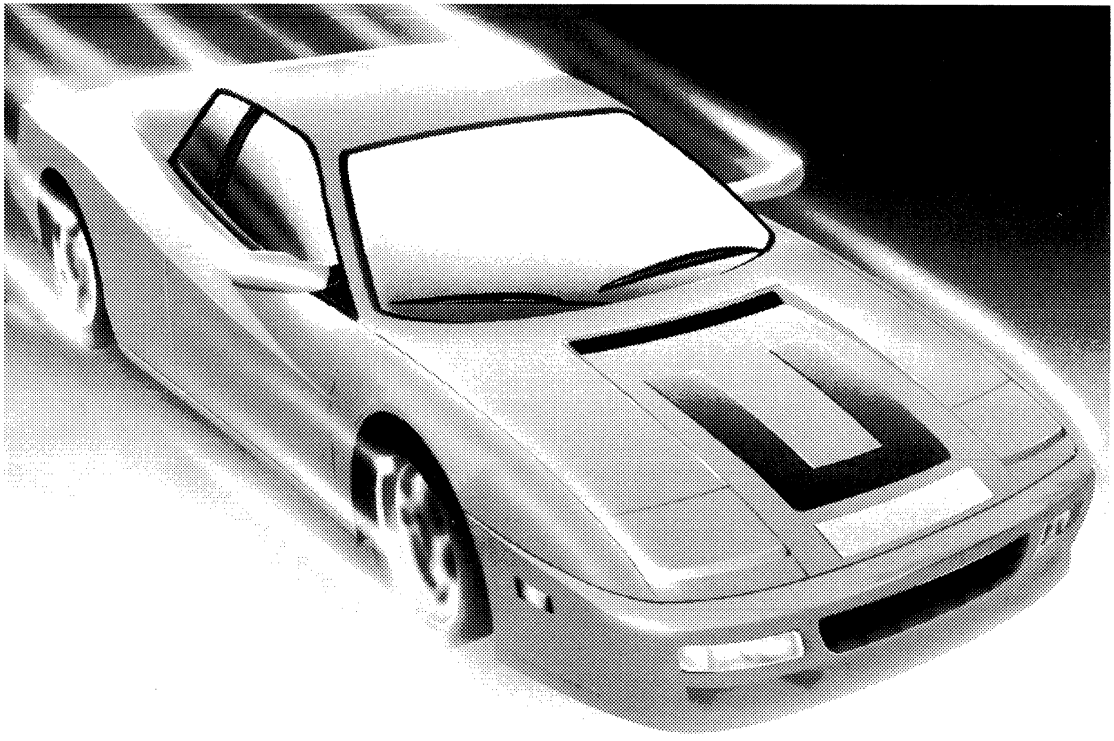

Automotive Products

A Dedication to Automotive Customers

Unitrode Integrated Circuits is a leader in innovative analog circuits that meet the needs of advanced automotive applications. **The circuits presented in this section are used in numerous automobile applications including: *systems multiplexing, electric vehicles, HID lighting, instrumentation, motor controls, fuel management and airbag systems.***

Unitrode is committed to the rigorous requirements of automotive customers. Utilizing a Total Quality Management (TQM) program based on the Baldridge model, maximum customer satisfaction is achieved. The TQM program includes twenty five continuous improvement teams. These teams are empowered to champion the process and to make changes which will enhance any facet of the operation. In order to ensure TQM techniques are employed by our vendors, Unitrode established Unitrode University. Unitrode University is an important element which enables the Unitrode TQM culture to be transferred to our vendor base. As a result of our dedication to Quality we have recently received ISO-9000 certification. Unitrode exceeds your Quality expectations.

Advanced Technologies

In order to maintain our leadership position we have a team of dedicated process development engineers who are working on the latest technologies. **Unitrode is very proud of our most recent process development, *Direct Wafer Bonding*. Developed in conjunction with Motorola as our partner, Direct Wafer Bonding will enable us to offer product utilizing junction isolation.** This will increase speed, power capabilities and integration densities. Technologies like Direct Wafer Bonding will enable Unitrode to be a leader in the automotive market.

Packaging

Unitrode offers a complete line of automotive package solutions. Packaging options include conventional 300 and 600 mil through-hole dual-in-line configurations as well as the latest surface mount solutions. Surface mount options include the plastic power leadless chip carrier (PLCC) and the 150 and 300 mil small outline (SO) packages. All packaged automotive circuits are supplied to operate over the full automotive temperature range (-40 degrees C to +105 degrees C).

Power Management

UC2842,3,4,5
Current Mode PWM Controller

- Low start-up current
- Optimized for offline and DC to DC converters
- Automatic feed forward compensation
- Pulse-by-pulse current limiting

NEW PRODUCT

UCC2802,3,4,5
Low Power BiCMOS (Current Mode) PWM

- 100µA typical starting supply current
- 500µA typical operating supply
- Internal soft start
- Internal leading edge blanking of the current sense signal

UC2846
Current Mode PWM Controller

- Programmable Pulse-by-Pulse current limiting
- Automatic symmetry correction in push-pull configuration
- Enhanced load response characteristics
- Parallel operation capability

UC2825
High Speed PWM Controller

- Compatible with voltage or current mode topologies
- 50ns propagation delay to output
- Practical operation at switching frequencies to 1.0 MHz
- High current dual totem pole outputs (1.5A Peak)

UC2852
High Power-Factor Preregulator

- Low cost power factor correction
- Power factor >.99
- Few external parts required
- Zero current switching

UC2854
High Power-Factor Preregulator

- Control boost PWM to .99 power factor
- Limit line current distortion to <5%
- World-wide operation without switches
- Feed forward line regulation

For more information on these products, refer to detailed data sheets.

INTEGRATED CIRCUITS
UNITRODE

Automotive Products

Power Management

NEW PRODUCT

UCC2806
Low Power BICMOS PWM

- 1.4MA max operating current
- 125 nsec delay to outputs
- 100mA start up current
- Simplified parallel operation

UC2575
Step-Down Voltage Regulator

- 5V output, ±3% max over line and load conditions
- Guaranteed 1A output current
- Voltage range 7V to 40V
- 4 external components required
- 2.5V precision reference

UC2576
Easy Switcher 1 Amp Step Down Voltage Regulator

- Adjustable output, reference voltage ± 2% max over line and load conditions
- Wide input and output voltage range
- Low power standby mode, Iq typically <200 μA
- Efficiency typically over 80%

UCC283-X
Low Drop Out 3A Positive Regulator

- Precision positive series pass voltage regulation
- 0.45V Drop out @ 3A
- Drop out under 2mV @ 10mA

Motor Control

L293
Push-Pull 4-Channel Driver

- Output current 1A per channel
- Peak output current 2A per switchmode channel
- Inhibit facility
- High noise immunity

UC2611
Quad Schottky Diode Array

- Matched, 4-diode monolithic array
- High peak current
- Low forward voltage

For more information on these products, refer to detailed data sheets.

INTEGRATED CIRCUITS
UNITRODE

Automotive Products

Motor Control

UC2637
Switched Mode Controller for DC Motor Drive

- Single or dual supply operation
- Pulse-by-pulse current limiting
- +/- 5% initial oscillator accuracy

UC2625
Brushless DC Motor Controller

- Drives power MOSFETS or power Darlingtons directly
- 50V open collector high side drivers
- Latched soft start

4

UC2717
Stepper Motor Drive Circuit

- Half-step and full-step capability
- Bipolar constant current motor drive
- Built-in fast recovery Schottky commutating diodes

UC2770
High Performance Stepper Motor Drive Circuit

- Full-step, half-step, and micro-step capability
- Bipolar output current up to 2A
- Low saturation voltage

Driver/Special Function

UC2722
Five-Channel Programmable Current Switch

- Five current-sinking switches
- Peak current-sinking switches
- Internal current sensing

UC2730
Thermal Monitor

- On-chip temperature transducer
- Temperature comparator gives threshold temperature alarm
- Precision 2.5V power reference

For more information on these products, refer to detailed data sheets.

INTEGRATED CIRCUITS
UNITRODE

Automotive Products

Driver/Special Function

UC2704
Bridge Transducer Switch

- Dual matched current sources
- High gain differential sensing circuit
- Wide common-mode input capability
- Externally programmable time

UC2705
High Speed Power Driver

- 1.5A source/sink drive
- 100 nsec delay
- 40 nsec rise and fall into 1000pF
- Inverting and non-inverting inputs

UC2707
Dual Channel Power Driver

- Two independent drivers
- 1.5A totem pole outputs
- 40nsec rise and fall into 1000pF
- High speed, power MOSFET Compatible

UC2708
Dual Non-Inverting Power Driver

- 3.0A peak current totem pole outputs
- 5 to 35V operation
- Wide 25 nsec Rise and Fall times

UC2709
Dual High-Speed FET Driver

- 1.5A source/sink drive
- Pin compatible with 0026 products
- 40nsec rise and fall into 1000pF
- Low quiescent current

UC2710
High Current FET Driver

- Totem pole output with 5A source/sink drive
- 35nsec delay
- 25nsec rise and fall time into 2.2 nF
- 85nsec rise and fall time into 30nF

For more information on these products, refer to detailed data sheets.

Driver/Special Function

UC2724
Isolated Drive Transmitter

- 500mA output drive, source or sink
- 8 to 35V operation
- Transmits logic signal instantly
- Programmable operating frequency

UC2725
Isolated High Side FET Driver

- Receives both power and signal across the isolation boundary
- 9 to 15V high level gate drive guaranteed
- Under-voltage lockout
- Output enable function

UC2726
Isolated Drive Transmitter

- 750mA output drive, source or sink
- 8 to 35V operation
- Transmits logic signal instantly
- Programmable operating frequency

UC2727
Isolated High Side IGBT Driver

- Receives power and signal from single isolation transformer
- Generates split rail for 4A peak bipolar gate drive
- 16V high level gate drive

NEW PRODUCT

UC2871
Synchronous Resonant Fluorescent Lamp Driver

- Complete drive and control circuitry for lamp and LCD
- Zero voltage switched topology
- Open lamp protection circuitry
- 4.5V to 20V operation

For more information on these products, refer to detailed data sheets.


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Indicates Application Note Available
See Section 9.

Power Supply Circuits


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Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs

Note: Most series available screened to /883B Rev. C

VOLTAGE MODE PWMs	PERFORMANCE CHARACTERISTICS																			
	Voltage Reference ±4%	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Osc.	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Osc. Sync Terminal	Adjustable Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package (Note 2)
Regulating PWMs																				
UC1524/2524/3524	X						X	100mA		300KHz	X								16 Pin N, J, *
Advanced Regulating PWMs																				
UC1524A/2524A/3524A		X		X	X	X	X	200mA		500KHz	X						X		16 Pin N, J, *
Advanced Regulating PWMs																				
UC1525A/2525A/3525A								100mA												
UC1527A/2527A/3527A		X	X	X	X		X	0.4A Pulse		500KHz			X	X	X				16 Pin N, J, *
Regulating PWMs																				
UC1526/2526/3526		X	X	X	X	X	X	100mA		400KHz			X	X	X		X		18 Pin N, J, *
Advanced Regulating PWMs																				
UC1526A/2526A/3526A		X	X	X	X	X	X	100mA		550KHz			X	X	X		X		18 Pin N, J, *
High Frequency PWM Controllers																				
UC1823/2823/3823		X	X	X	X	X		500mA 1.5A	X			X	X	X	X		X	X	
UC1825/2825/3825		X	X	X	X	X		Pulse		2MHz	X		X	X	X		X	X	16 Pin N, J, *
Regulating PWMs																				
UC494	X							200mA		300KHz	X				X		X		16 Pin N, J
Advanced Regulating PWMs																				
UC494A/UC494C																				16 Pin N, J
UC495A/UC495AC		X			X			200mA		300KHz	X				X		X			18 Pin N, J
Programmable Primary Side PWMs																				
UC1840/2840/3840		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J,*

Note 1: All Current Mode Control ICs can be used in "Voltage Mode" Also; Consult Current Mode PWM Selection Guide.

Note 2: N = Plastic Package
J = Ceramic Package
* = Surface Mount Available, Consult Factory

5

Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs (Cont'd)

Note: Most series available screened to /883B Rev. C

VOLTAGE MODE PWMs	PERFORMANCE CHARACTERISTICS																			
	Voltage Reference ±4%	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Osc.	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Osc. Sync Terminal	Adjustable Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package (Note 2)
Programmable Primary Side PWMs UC1841/2841/3841		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J,*
Advanced Programmable, Off-Line PWM UC1851/3851		X	X	X	X	X	X	200mA	X	500KHz		X	X		X	X	N/A	X	18 Pin N,J,*
Power Supply Control Systems* UC2850/3850	X		X	X	X	X	X	50mA		200KHz	X			X	X		X		24 Pin N, J, *
Enhanced Voltage Mode UCC3570 (BICMOS)		X	X	X	X	X	X	500mA	X	500KHz		X	X	X	X	X	N/A	X	14Pin N, J, D

Note 1: All Current Mode Control ICs can be used in "Voltage Mode" Also; Consult Current Mode PWM Selection Guide.
Note 2: N = Plastic Package
J = Ceramic Package
* = Surface Mount Available, Consult Factory

Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs

Note: Most series available screened to /883B Rev. C

CURRENT MODE PWMs	PERFORMANCE CHARACTERISTICS																			
	Accurate Osc. Discharge Current	Voltage Reference ±1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Osc.	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Osc. Sync Terminal	Accurate Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package (Note)
BICMOS High Frequency PWM Controllers																			
UCC1802/2802/3802																			
UCC1803/2803/3803								500mA											
UCC1804/2804/3804								1.0A											
UCC1805/2805/3805		X	X	X	X	X		Pulse	X	1MHz		X	X			X	X	X	8 Pin N, J, D *
BICMOS High Frequency PWM Controllers								500mA											
UCC1806/2806/3806		X	X	X	X	X	X	1.0A Pulse	X	1MHz	X		X	X		X	X	X	16 Pin N, J, DW
Dual BICMOS Current Mode																			
UC1810/2810/3810		X	X	X	X	X			X	1MHz		(2)X	X			X	X	X	16 Pin N, J, DW
High Frequency PWM Controllers								500mA											16 Pin N, J, *
UC1823/2823/3823		X	X	X	X	X		1.5A	X			X	X	X	X		X	X	
UC1825/2825/3825		X	X	X	X	X		Pulse		2MHz	X		X	X	X		X	X	
High Frequency PWM Controllers								500mA											
UC1823A/2823A/3823A	X	X	X	X	X	X		1.5A	X			X	X	X			X	X	
UC1825A/2825A/3825A	X	X	X	X	X	X		Pulse		2MHz	X		X	X	X		X	X	16 Pin N, J, *
Complementary Output PWM Controllers								500mA											
UC1824/2824/3824		X	X	X	X	X	X	1.5A Pulse	X		X		X	X	X	X	X	X	16 Pin N, J, DW
Programmable Primary Side PWMs																			
UC1840/2840/3840		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	16 Pin N, J, *
Programmable Primary Side PWMs																			
UC1841/2841/3841		X	X	X	X	X	X	200mA	X	500KHz		X			X	X	N/A	X	18 Pin N, J, *
Economy Primary Side PWMs																			
UC1842/2842/3842																			
UC1843/2843/3843								100mA											
UC1844/2844/3844								1A											
UC1845/2845/3845		X		X	X	X		Pulse	X	500KHz		X			X		N/A	X	8 Pin N, J, *

Note: N = Plastic Package
J = Ceramic Package
* = Surface Mount Available, Consult Factory

Power Supply Controls

PWM Performance Chart

SWITCHING REGULATOR CONTROL ICs (Cont'd)

Note: Most series available screened to /883B Rev. C

CURRENT MODE PWMs	PERFORMANCE CHARACTERISTICS																		
	Accurate Osc. Discharge Current	Voltage Reference ± 1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Osc.	Dual Outputs	Single-Ended Output	Totem Pole Outputs	Separate Osc. Sync Terminal	Accurate Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up	Package (Note)
Economy Primary Side PWMs UC1842A/2842A/3842A UC1843A/2843A/3843A UC1844A/2844A/3844A UC1845A/2845A/3845A		X		X	X	X		100mA 1A Pulse	X	500KHz		X			X		N/A	X	8 Pin N, J, *
Current Mode PWM Controllers UC1846/2846/3846 UC1847/2847/3847		X	X	X	X	X	X	200mA	X	500KHz			X	X	X	X	X	X	16 Pin N,J, *
Average Current Mode PWM UC1848/2848/3848	X	X	X	X	X			500mA 2.0 A Pulse		1MHz		X	X		X	X	X	X	16 Pin N, J, DW
Advanced Programmable, Off-line PWM UC1851/3851		X	X	X	X	X	X	200mA	X	500KHz		X	X		X	X	N/A	X	18 Pin N, J, *
Advanced High Performance PWM UC1856/2856/3856	X	X	X	X	X	X	X	500mA 1.5A Pulse		1MHz	X		X	X	X		X		16 Pin N, J, DW

Note: N = Plastic Package
J = Ceramic Package
* = Surface Mount Available, Consult Factory

Power Supply Controls

CURRENT MODE CONTROL IC APPLICATION GUIDE

	OFF LINE	DC/DC & BATTERY	POWER FACTOR CORRECTION	SYNCHRONOUS RECTIFIER	BUCK REGULATOR	BOOST CONVERTER	FORWARD (<50% MAX DUTY)	FLYBACK (<50% MAX DUTY)	FORWARD (>50% MAX DUTY)	FLYBACK (>50% MAX DUTY)	HALF-BRIDGE	FULL-BRIDGE	PUSH-PULL	CUK/SEPIC
UCC1800		■			■	■			■	■				■
UCC1801		■			■	■			■	■				■
UCC1802	■				■	■			■	■				■
UCC1803		■			■	■			■	■				■
UCC1804	■				■	■	■	■						■
UCC1805		■			■	■	■	■						■
UCC1806	■	■					■	■			■	■	■	
UCC1810	■	■			■	■	■	■	■	■				■
UC1823	■	■			■	■			■	■				■
UC1823A		■			■	■			■	■				■
UC1823B	■				■	■			■	■				■
UC1824	■	■		■		■	■	■	■	■				
UC1825	■	■					■	■			■	■	■	
UC1825A		■					■	■			■	■	■	
UC1825B	■						■	■			■	■	■	
UC1828	■	■			■	■	■	■	■	■				■
UC1840	■	■			■	■	■	■	■	■				■
UC1841	■	■			■	■	■	■	■	■				■
UC1842	■				■	■			■	■				■
UC1842A	■				■	■			■	■				■
UC1843		■			■	■			■	■				■
UC1843A		■			■	■			■	■				■
UC1844	■				■	■	■	■						■
UC1844A	■				■	■	■	■						■

Note: Most series available screened to /883B Rev. C

Power Supply Controls

Current Mode Application Guide

CURRENT MODE CONTROL IC APPLICATION GUIDE (Cont'd)

	OFF LINE	DC/DC BATTERY	POWER FACTOR CORRECTION	SYNCHRONOUS RECTIFIER	BUCK REGULATOR	BOOST CONVERTER	FORWARD (<50% MAX DUTY)	FLYBACK (<50% MAX DUTY)	FORWARD (>50% MAX DUTY)	FLYBACK (>50% MAX DUTY)	HALF-BRIDGE	FULL-BRIDGE	PUSH-PULL	CUK/SEPIC
UC1845		■			■	■	■	■						■
UC1845A		■			■	■	■	■						■
UC1846	■	■					■	■			■	■	■	
UC1847	■	■					■	■			■	■	■	
UC1848	■	■			■	■	■	■	■	■				■
UC1849	■	■									■	■	■	■
UC1851	■	■			■	■	■	■	■	■				■
UC1852	■		■		■	■		■		■				■
UC1854	■		■		■	■		■		■				■
UC1854A	■		■		■	■		■		■				■
UC1855	■		■		■	■		■		■				■
UC1856	■	■			■	■	■	■			■	■	■	
UC1871		■		■	■	■		■		■	■	■	■	■
UC1875	■	■										■		
UC1876	■							■				■		
UC1877		■						■				■		
UC1878	■							■				■		
UCC1883	■	■			■	■	■	■	■	■				■
UCC1885	■	■			■	■	■	■	■	■				■
UCC1891	■		■			■	■	■			■	■	■	
UCC1892	■	■	■			■	■	■			■	■	■	
UCC1893	■		■	■		■			■	■				■
UCC1894	■	■	■	■		■			■	■				■

Note: Most series available screened to /883B Rev. C

Power Supply Controls

RESONANT MODE CONTROLLERS

DEVICE	ZERO CURRENT SWITCHING (ZCS)	ZERO VOLTAGE SWITCHING (ZVS)	ZERO VOLTAGE TRANSITION (ZVT)	VARIABLE FREQUENCY	FIXED FREQUENCY	CONTROLLED PWM ON-TIME	CONTROLLED PWM OFF-TIME	ZERO DETECTION	SINGLE OUTPUT	DUAL OUTPUT - ALTERNATING	DUAL OUTPUT - COMPLEMENTARY	QUAD OUTPUTS - PHASE SHIFTED	OFF-LINE	DC/DC
UC1824			■		■	■					■		■	■
UC1852	■			■		■		■	■				■	■
UC1855			■		■	■					■		■	■
UC1860	■			■		■		■	■	■	■		■	■
UC1861		■		■			■	■		■			■	
UC1862		■		■			■	■	■				■	
UC1863		■		■			■	■		■				
UC1864		■		■			■	■	■					■
UC1865	■			■		■		■		■			■	
UC1866	■			■		■		■	■				■	
UC1867	■			■		■		■		■				■
UC1868	■			■		■		■	■					■
UC1875			■		■	■						■	■	■
UC1876	■							■				■		
UC1877		■						■				■		
UC1878	■							■				■		

Note: Most series available screened to /883B Rev. C

5

Power Supply Controls

POWER FACTOR CORRECTION ICs

	FIXED FREQUENCY	VARIABLE FREQUENCY	PFC & PWM (COMBO)	AVERAGE CURRENT MODE PFC	CONTROLLED ON-TIME PFC	ZERO VOLTAGE TRANSITION (ZVT)	ALTERNATING OUTPUTS - PWM	PARALLEL OUTPUTS - PWM
UC1852		■			■	1		
UC1854	■			■				
UC1854A	■			■				
UC1855	■			■		■		
UC1891	■		■	■			■	
UC1892	■		■	■			■	
UC1893	■		■	■				■
UC1894	■		■	■				■

1 can be obtained

LOW CURRENT BICMOS CONTROLLERS

	OFF-LINE APPLICATIONS	DC/DC APPLICATIONS	NOTEBOOK/BATTERY	ISDN (25mW RESTRICTED)	SINGLE PWM OUTPUT	DUAL OUTPUTS	5 VOLT OPERATION	INTERNAL LEADING-EDGE BLANKING	SOFT-START (I/E)	RESTART DELAY AFTER FAULT
UCC1800		■	■		■			■	I	I
UCC1801		■	■		■			■	I	I
UCC1802	■				■			■	I	I
UCC1803		■	■		■		■	■	I	I
UCC1804	■				■			■	I	I
UCC1805		■	■		■		■	■	I	I
UCC1806	■	■	■			■		■	E	E
UCC1810	■	■				■		■	I	I
UCC1883		■	■	■	■			■	E	E
UCC1885		■	■	■	■				E	E

1 can be obtained

Power Supply Controls

POWER SUPPLY SUPPORT FUNCTIONS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1891/2891/3891	Two Stage Power Factor Converter	• Single Chip Solution For Power Factor Corrected Power Systems • World Wide Voltage Operation Without Switches • Fixed Frequency PWM Drive for Both Pre and Post Regulators • Low Offset Analog Multiplier/Divider	28 Pin PLCC or 24 Pin DIL
UC1904/2904/3904	Enhanced Quad Supply and Line Monitor	• Inputs for Monitoring up to Four Supply Voltages • Two Inputs Preset for -5V and -12V Monitoring, or Programmable Positive Levels • Precision 2.5V Reference • Separate Inputs for Over-Current and Line Fault Sensing	18 Pin DIL or 20 Pin SO-IC
UC1612/3612	Dual Schottky Diode Array	• Monolithic Two Diode Array • Exceptional Efficiency • Low Forward Voltage • High Peak Current (3A) • Small Size	8 Pin SO-IC (Power PKG) or 8 Pin DIL
UC19431	Shunt Precision Reg./Opto Driver	• Multiple On-Chip Programmable Reference Voltages • 0.4% Initial Accuracy • 1.0% Overall Ref. Tolerance • 2.2V to 36V Operating Supply Voltage and User Programmable Reference • Known Linear Transconductance @ 5%Tolerance	8 Pin DIL or 8 Pin SO-IC
UC19432	Precision Analog Reg./Opto Driver	• Programmable Transconductance for Optimum Current Drive • Accessible 1.3V Precision Reference • Both Error Amplifier Inputs Available • 0.4% Initial Accuracy • 1.0% Overall Reference Tolerance • 2.2V to 36.0V Operating Supply Voltage • Reference Accuracy Maintained for Entire Range of Supply Voltage • Superior Accuracy and Easier Compensation for Opto-Isolator Application • Low Quiescent Current (0.55mA Typ.)	8 Pin DIL or 8 Pin SO-IC
UC1907/2907/3907	Load Share Controller	• Fully Differential High Performance Voltage Sensing • Accurate Current Amplifier for Precise Current Sharing • Opto Coupler Driving Capability • 1.25% Trimmed Reference	16 Pin DIL or 16 Pin SO-IC or 20 Pin PLCC
UC2575	EZ Switcher	• 1A Fixed or Adjustable Step Down Converter • Up to 60V Input • High Efficiency • Pin Compatible with LM2575	5 Pin TO-220

Product Selection Guide

POWER SUPPLY SUPPORT FUNCTIONS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC2576	EZ Switcher	• Same Features as UC2575 • 3A Output • Pin Compatible with LM2576	5 Pin TO-220
UC2577	EZ Switcher	• 1A Fixed or Adjustable Step Up Converter • Up to 60V Input • High Efficiency • Pin Compatible with LM2577	5 Pin TO-220
UCC1831, 2, 3, 5 UCC2831, 2, 3, 5 UCC3831, 2, 3, 5	Low Dropout 3A Positive Linear Regulator	• Drop Out < 0.6V @ 3A • Drop Out <2mV @ 10mA • Quiescent current < 250μA Irrespective of Load • Adjustable (5 Lead) Output Voltage Version • Fixed (3 Lead) Version @ 2.85V, 3.3V and 5V • Protection Features	5 Pin TO-220 or 3 Pin TO-220
UC1854A/2854A/3854A	Enhanced UC3854 Power Factor Controller	• Controls Boost PWM to Near Unity Power Factor • Limits Line Current Distortion to < 3% • Accurate Power Limiting • Enhanced Multiplier Improvements • High Bandwidth (5 MHz) Low Offset Current Amplifier • Faster/Improved Accuracy 'Enable Comparator'	16 Pin DIL or 16 Pin SO-IC or 20 Pin PLCC

Power Supply Controls

PRODUCT APPLICATIONS CIRCUITS

PRODUCT SERIES	TYPICAL APPLICATIONS
UC1611/2611/3611 Quad Schottky Array For other similar product refer to UC1610/3610 Schottky Array	• Matched, Four Diode Monolithic Array • High Peak Current • Low Cost MINIDIP Package • Low Forward Voltage • Parallelable for Lower V_F or Higher V_F • Fast Recovery Time • Military Temperature Range Available
UC3704 Bridge Transducer Switch	Any Analog to Digital monitoring system; coupled with any of a wide range of sensors almost any type of physical phenomena may be monitored. Samples: • Air-Flow Sensor Circuits • Liquid or Gas Flow Circuits • Passing Object Circuits
UC1906/2906/3906 Lead-Acid Battery Charger	"IC Circuitry that results in optimized charge cycles for specific battery applications." • Uninterruptable Power Supplies • Portable Electrical Equipment • Emergency Power and Light Systems • Volatile Data Handling Computers—Power Back-Up
UC1730/2730/3730 Temperature and Air Flow Sensor	By combining a temperature monitor and heater, this IC permits airflow velocity past the IC package to be monitored. • On-Chip Temperature Transducer • Temperature Comparator Gives Threshold Temp-Airflow Alarm • Low 2.5mA Quiescent Current
ISDN UCC1883/2883/3883 Primary Side Controller	• Can Function as a General-purpose Low-power Controller • Fully Synchronizing Oscillator • Synchronization to Secondary Side Logic • Leading Edge Blanking of Current Sense • 50% Maximum Duty Cycle • Undervoltage Lockout • Programmable Low Line Sensing • Programmable Softstart • Programmable Fault/Restart Delay **ISDN FEATURES** • Zero-power Startup Capability • Restricted Mode Detection • Frequency Agile PWM in Restricted Mode • Precision Programmable Quiescent Current • Very Low Quiescent Power for CCITT 25mW Restricted Mode • Accurate, Programmable Input Power Limit or Input Current Limit
ISDN UCC1885/2885/3885 Secondary Regulator	• Wide Operating Range • Fully Synchronized Oscillator • Temperature Stable Oscillator • Logic Level Synchronization Input • Precision Reference • Error Amplifier for Loop Regulation and Compensation • Undervoltage Lockout **ISDN FEATURES** • Low Line Logic Output • Restricted Mode Logic Output • Precision Programmable Quiescent Current • Very Low Quiescent Power for CCITT 25mW Restricted Mode


INTEGRATED
CIRCUITS
UNITRODE

UC161A
UC161B
UC161C

Micropower Quad Comparator

FEATURES

- Programmable Output Drive Capability
- Direct CMOS Logic Compatibility
- Low Power
- Direct Wire-OR of Outputs
- Wide Input Common Mode Range

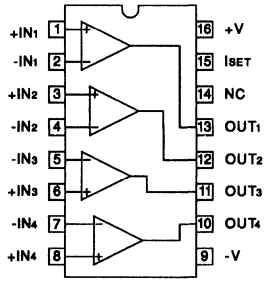
DESCRIPTION

The UC161 family of quad comparators feature programmable DC and AC parameters. A single external resistor can set the comparators to operate in the microwatt region for battery applications, or higher current levels can be set to obtain improved speed or drive capabilities. The outputs on these devices can be wire OR'd together, simplifying external logic requirements in some applications.

These devices are available in three temperature ranges, the UC161A is specified for the full military range, -55° C to +125°C, the UC161B for the industrial range, -25°C to +85°C, and the UC161C for the commercial range of 0°C to +70°C.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
N or J Package

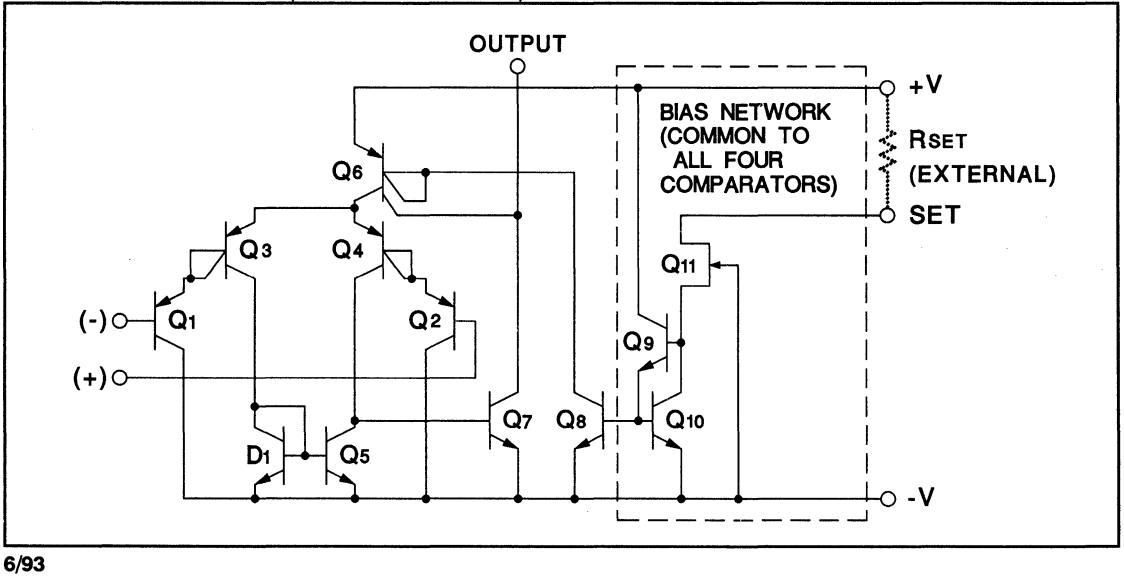


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V to -V)	36V
Differential Input Voltage	±30V
Input Voltage	-V–0.3V to +V
Power Dissipation at T_A = 25°C	1000 mW
Power Dissipation at Tc = 25°C	2000 mW
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+300°C

Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)



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ELECTRICAL CHARACTERISTICS: Temperature range is -55° to +125°C for the UC161A, -25°C to +85°C for the UC161B, and 0°C to +70°C for the UC161C.

LOW POWER ELECTRICAL CHARACTERISTICS: Unless Otherwise Stated: V_S = ±3V, I_{SET}[2] = 10µA, R_2 =10MΩ, C_L = 10pF, T_A = 25°C, T_A = T_J.

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1	3		1	6	mV
INPUT	Input Offset Current	I_{OS}			1	20		1	25	nA
INPUT	Input Bias Current	I_{BT}			20	100		20	200	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		20	30		10	30		V/mV
OUTPUT	Low Output Voltage[1]	V_{OL}	R_L = 20kΩ		-2.95	-2.6		-2.95	-2.6	V
OUTPUT	High Output Voltage[1]	V_{OH}	R_L = 200kΩ	2.5	2.9		2.5	2.9		V
DYNAMIC	Common Mode Range	CMR			+1.3/-3			+1.3/-3		V
DYNAMIC	Response Time	t	100mV Overdrive, C_L = 10pF		5			5		µs
DYNAMIC	CommonModeRejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	PowerSupplyRejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	SupplyCurrent	Is	AllInputsGrounded, R_L = ∞		210	300		210	300	µA
										T_A = Over Temperature Range
	Input Offset Voltage	V_{OS}				5				mV
	DC Open Loop Voltage Gain	A_{VOL}		10			5			V/mV
	Supply Current	Is	All Inputs Grounded, R_L = ∞			350			350	µA

HIGH POWER ELECTRICAL CHARACTERISTICS: Unless Otherwise Stated: V_S = ±15V, I_{SET}[2] = 100µA, R_L =2MΩ, C_L = 10pF, T_A = 25°C, T_A = T_J.

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1.5	3		1.5	6	mV
INPUT	Input Offset Current	I_{OS}			5	60		5	90	nA
INPUT	Input Bias Current	I_{BT}			100	400		100	800	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		50	100		30	100		V/mV
OUTPUT	Low Output Voltage1	V_{OL}	R_L = 20kΩ		-14.9	-14.6		-14.9	-14.6	V
OUTPUT	High Output Voltage1	V_{OH}	R_L = 200kΩ	14.5	14.9		14.5	14.9		V
DYNAMIC	Common Mode Range	CMR			+13/-15			+13/-15		V
DYNAMIC	Response Time	t	100mV Overdrive, C_L = 10pF		1			1		µs
DYNAMIC	Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	Supply Current	Is	All Inputs Grounded, R_L = ∞		2100	3500		2100	3500	µA

Note 1: The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

Note 2: Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} : I_{SUPPLY} = 21 \times I_{SET}.$$

HIGH POWER ELECTRICAL CHARACTERISTICS (Continued): $T_A = T_J$.

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
	Input Offset Voltage	V_{OS}				6				mV
	Input Bias Current	I_{BT}				500				nA
	DC Open Loop Voltage Gain	A_{VOL}		25			15			V/mV
	Supply Current	I_S	All Inputs Grounded $R_L = \infty$			4000			4000	µA

Note 1: The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

Note 2: Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} : I_{SUPPLY} = 21 \times I_{SET}.$$

APPLICATION AND OPERATION INFORMATION DESCRIPTION

The UC161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias, current slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations is possible. The UC161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The circuit (see Simplified Schematic) is composed of five major blocks–four comparators and a common bias network. Q_1-Q_6, and D_1 from a darlington differential amplifier with double-to-single ended conversion. Q_6 is a dual current source whose outputs are exactly twice the current flowing through Q_8. The collector current of Q_8 is a function of the current supplied externally to Q_9-Q_{10}, which in turn is known as the set current of I_{SET}. This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}$$

where +V is the voltage to which the control resistor is connected, -V is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship between I_{SET} and the total supply current:

I_{SUPPLY} = [I_{SET} *(current sourced by Q_6 to Q_8)*

+2 I_{SET} (current sourced to the differential amplifier by Q_6)

+2 I_{SET} (current sourced to the comparator output by Q_6)

× 4 (the total number of comparators)

+ I_{SET} (current sourced through Q_{11}, Q_{10}, and Q_9 to –V)

= [I_{SET} + 2 I_{SET} + 2 I_{SET}] × 4 + I_{SET}

= 21 I_{SET}

The output current pulldown capability (I_{OL}) of the UC161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6:

$$I_{OH} = 2 \times I_{SET}$$

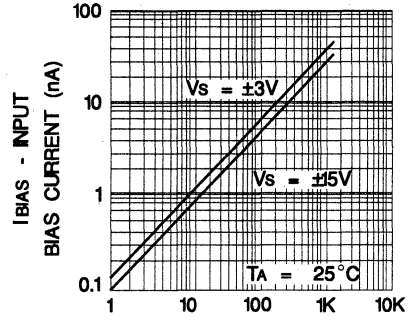
I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain Q_7:

$$I_{OL} = \beta (Q_7) \times 2\ I_{SET}$$

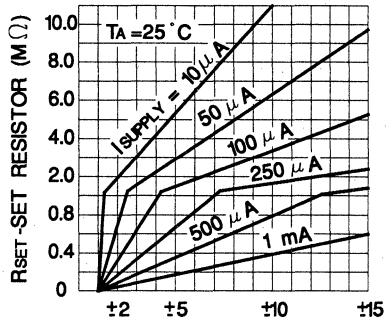
The beta of Q_7 is about 75–150.

APPLICATION AND OPERATION INFORMATION (Continued)

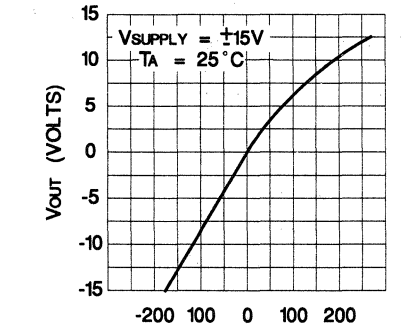
Input Bias Current vs Supply Current



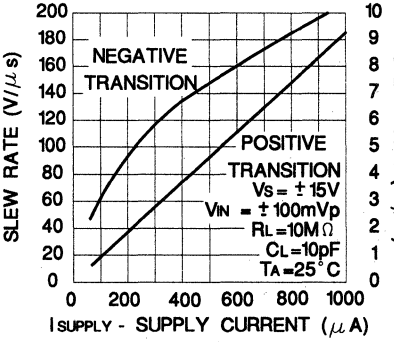
RSET vs VSUPPLY for Various Supplies



Transfer Characteristics



Slew Rate vs Supply Current



UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603)-424-3460

Advanced Regulating Pulse Width Modulators

FEATURES

- Dual Uncommitted 40V, 200mA Output Transistors
- 1% Accurate 5V Reference
- Dual Error Amplifiers
- Wide Range, Variable Deadtime
- Single-ended or Push-pull Operation
- Under-voltage Lockout With Hysteresis
- Double Pulse Protection
- Master or Slave Oscillator Operation
- UC495A: Internal 39V Zener Diode
- UC495A: Buffered Steering Control

DESCRIPTION

This entire series of PWM modulators each provide a complete pulse width modulation system in a single monolithic integrated circuit. These devices include a 5V reference accurate to ±1%, two independent amplifiers usable for both voltage and current sensing, an externally synchronizable oscillator with its linear ramp generator, and two uncommitted transistor output switches. These two outputs may be operated either in parallel for single-ended operation or alternating for push-pull applications with an externally controlled dead-band. These units are internally protected against double-pulsing of a single output or from extraneous output signals when the input supply voltage is below minimum.

The UC495A contains an on-chip 39V zener diode for high-voltage applications where Vcc would be greater than 40V, and a buffered output steering control that overrides the internal control of the pulse steering flip-flop.

The UC494A is packaged in a 16-pin DIP, while the UC495A is packaged in an 18 pin DIP. The UC494A, UC495A are specified for operation over the full military temperature range of -55°C to +125°C, while the UC494AC, UC495AC are designed for industrial applications from 0°C to +70°C.

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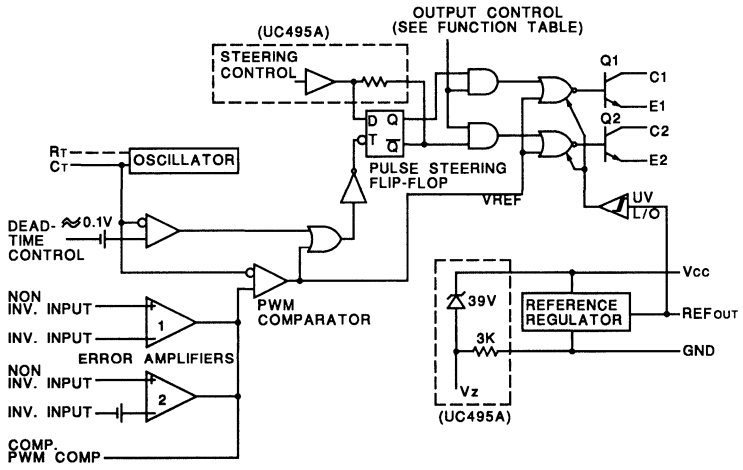
BLOCK DIAGRAM



FUNCTION TABLE	
Output Control Connected to:	Output Function
Ground	Single-Ended or Parallel Operation
VREF	Push-Pull Alternating Outputs

UC495A

Steering Control (Output Control at VREF)	Output Function
Vs < 0.4V	PWM Output at Q1
Vs > 2.4V	PWM Output at Q2

ABSOLUTE MAXIMUM RATINGS (Note 1, 2, 3)

Supply Voltage, Vcc (Note 2) 45V
Amplifier Input Voltages ..... Vcc + 0.3V
Collector Output Voltage 41V
Collector Output Current 250mA
Continuous Total Dissipation 1000mW
@ (or below) 25°C free air temperature range (Note 3)
Storage Temperature Range ..... -65° to +150°C
Lead Temperature 1/16" (1.6mm) from case for 60 seconds,
J Package ..... 300°C
Lead Temperature 1/16" (1.6mm) from case for 10 seconds,
N Package ..... 260°C

Note 1: Over operating free air temperature range unless otherwise noted.

Note 2: All voltage values are with respect to network ground terminal 3.

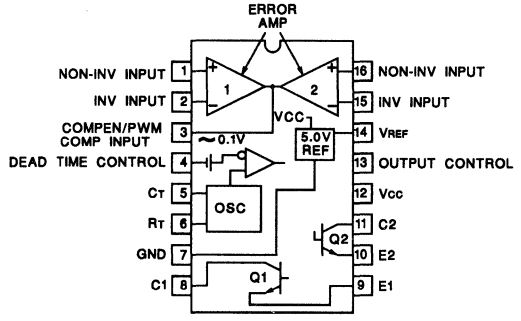
Note 3: Consult Packaging Section of Databook regarding thermal specifications and limitations of packages.

RECOMMENDED OPERATING CONDITIONS

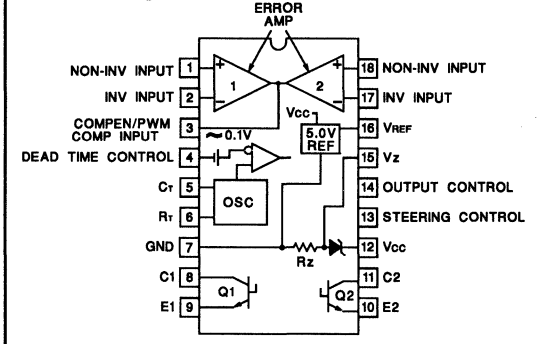
Supply Voltage Vcc ..... 7V to 40V
Error Amplifier Input Voltages ..... -0.3V to Vcc-2V
Collector Output Voltage 40V
Collector Output Current (each transistor) 200mA
Current into Feedback Terminal 0.3mA
Timing Capacitor, C_T ..... 0.47nF to 10,000nF
Timing Resistor, R_T ..... 1.8kΩ to 500kΩ
Oscillator Frequency ..... 1kHz to 300kHz
Operating Free Air Temperature
UC494A, UC495A ..... -55°C to +125°C
UC494AC, UC495AC ..... 0°C to +70°C

CONNECTION DIAGRAMS

DIL-18 (TOP VIEW) **UC494A/AC**
J or N Package



DIL-18 (TOP VIEW) **UC495A/AC**
J or N Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, over recommended operating free-air temperature range, Vcc = 15V, f = 10kHz, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage V_{REF}	Io = 1mA, T_A = 25°C	4.95	5	5.05	V
Input Regulation	Vcc = 7V to 40V		2	25	mV
Output Regulation	Io = 1mA to 10mA		1	15	mV
Output Voltage Over Temperature	ΔT_A = Min. to Max.	4.90		5.10	V
Short Circuit Output Current	V_{REF} = 0, T_A = 25°C (Note 1)	10	35	50	mA
Oscillator Section					
Frequency (Note 2)	C_T = 0.01μF, R_T = 12kΩ		10		kHz
Standard Deviation Of Frequency (Note 3)	All Values of Vcc, C_T, R_T, T_A Constant		10		%
Frequency Change With Voltage	Vcc = 7V to 40V, T_A = 25°C		0.1		%
Frequency Change With Temperature	C_T = 0.01μF, R_T = 12kΩ, ΔT_A = Min. to Max.			2	%
Deadtime Control Section (Output Control Connected to V_{REF})					
Input Bias Current (Pin 4)	$V_{(PIN\ 4)}$ = 0V to 5.25V		-2	-10	μA
Maximum Duty-Cycle (Each Output)	$V_{(PIN\ 4)}$ = 0V	45			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz, $T_A = T_J$.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
Deadtime Control Section (cont.) (Output Control Connected to V_{REF})							
Input Threshold Voltage (Pin 4)		Zero Duty-Cycle			3	3.3	V
		Maximum Duty-Cycle		0			V
Amplifier Section							
Input Offset Voltage		$V_{O\ (PIN\ 3)}$ = 2.5V			2	10	mV
Input Offset Current		$V_{O\ (PIN\ 3)}$ =2.5V			25	250	nA
Input Bias Current		$V_{O\ (PIN\ 3)}$ = 2.5V			-0.2	-1	µA
Common-Mode Input Voltage Range		V_{CC} = 7V to 40V		.03 to V_{CC} -2			V
Open Loop Voltage Gain		ΔVo = 3V, Vo = 0.5V to 3.5 V		70	95		dB
Unity Gain Bandwidth					800		kHz
Common-Mode Rejection Ratio		V_{CC} = 40V, T_A = 25°C		65	80		dB
Output Sink Current (Pin 3)		V_{ID} = -15mV to -5V, $V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Output Source Current (Pin 3)		V_{ID} = 15mV to 5V, $V_{(PIN\ 3)}$ = 3.5V		-2			mA
Output Section							
Collector Off-State Current		V_{CE} = 40V, V_{CC} = 40V			2	100	µA
Emitter Off-State Current		V_{CC} = V_C = 40V, V_E = 0				-100	µA
Collector - Emitter Saturation Voltage	Common-Emitter	V_E = 0, I_C = 200mA			1.1	1.3	V
	Emitter-Follower	V_C = 15V, I_E = -200mA			1.5	2.5	V
Output Control Input Current		V_I = V_{REF}				3.5	mA
PWM Comparator Section							
Input Threshold Voltage (Pin 3)		Zero Duty-Cycle			4	4.5	V
Input Sink Current (Pin 3)		$V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Steering Control (UC495A, See Function Table)							
Input Current		$V_{(PIN\ 13)}$ = 0.4V, Q_1 ACTIVE				-200	µA
		$V_{(PIN\ 13)}$ = 2.4V, Q_2 ACTIVE				300	µA
Deadband					500		mV
Zener Diode Circuit (UC495A)							
Breakdown Voltage		V_{CC} = 45V, I_Z = 2mA		36	39	45	V
Sink Current		$V_{(PIN\ 15)}$ = 1V		0.2	0.3	0.6	mA
Total Device							
Standby Supply Current		Pin 6 at V_{REF}, All other inputs and outputs open	V_{CC} = 15V		6	10	mA
			V_{CC} = 40V		9	15	mA
Under Voltage Lockout				3.5		6.5	V
Hysteresis					300		mV
Switching Characteristics (T_A = 25°C)							
Output Voltage Rise Time		Common-Emitter Configuration			100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L = 15pF			25	100	ns
Output Voltage Rise Time		Emitter-Follower Configuration			100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L=15pF			40	100	ns

Note 1: Duration of the short circuit should not exceed one second.

Note 2: Frequency for other values of C_T and R_T is approximately $f = \frac{1.1}{R_T C_T}$

Note 3: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum (X_n - X)^2}{\frac{n-1}{n-1}}}$$

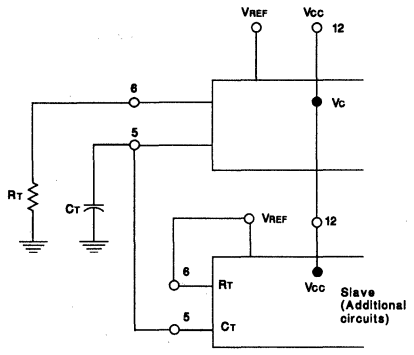


Figure 1. Slaving Two or More Control Circuits

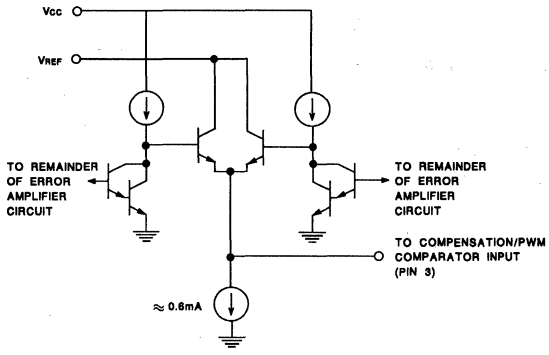
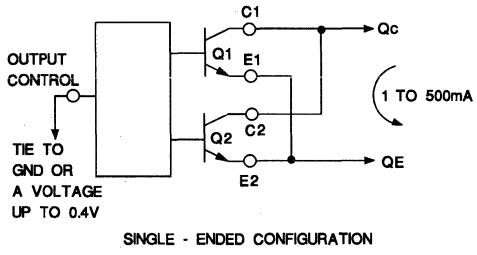


Figure 2. Output Circuit of Error Amplifiers



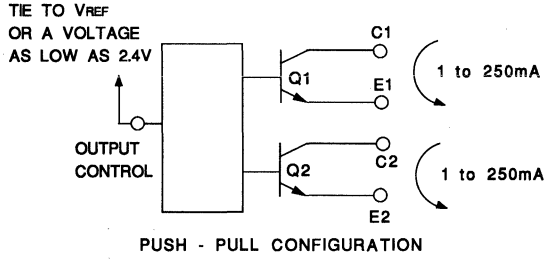


Figure 3. Output Connections for Single-Ended and Push-Pull Configurations

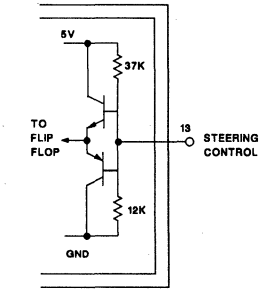


Figure 4. Internal Buffer with Deadband for Steering Control on UC495A

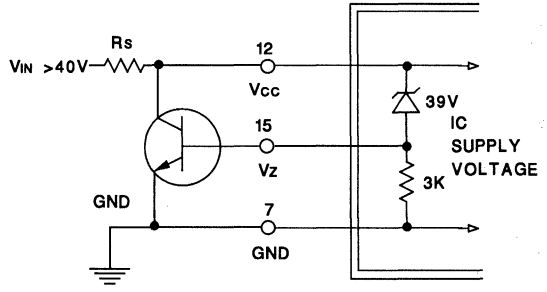


Figure 5. Operation with VIN > 40V Using Internal Zener

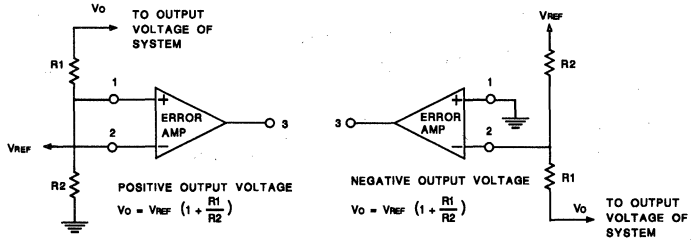


Figure 6. Error Amplifier Sensing Techniques

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UC1524
UC2524
UC3524

Advanced Regulating Pulse Width Modulators

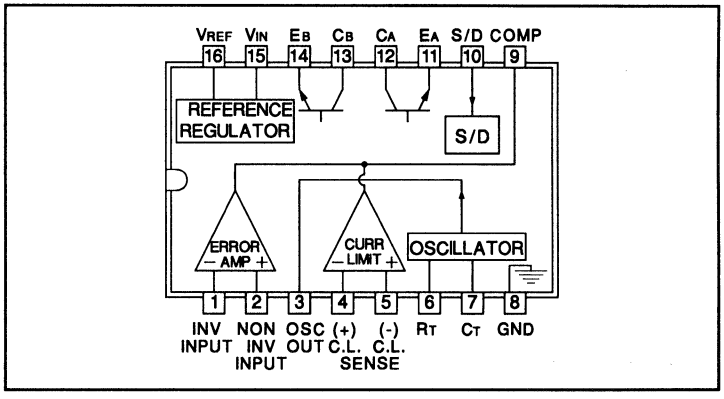
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current...8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

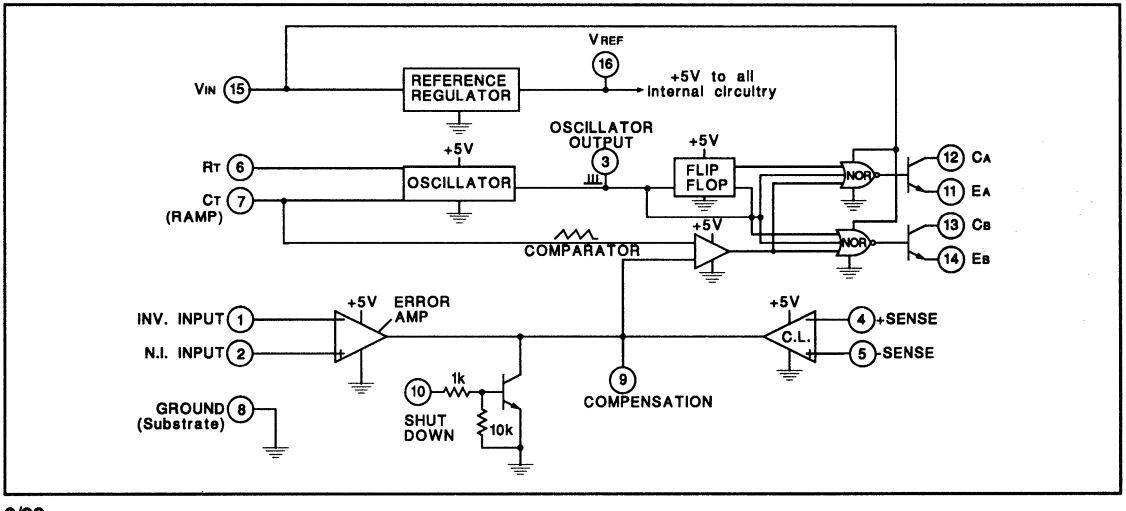
DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

CONNECTION DIAGRAM



BLOCK DIAGRAM



6/93

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1524, –25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T_J = 25°C		66			66		dB
Short Circuit Current Limit	V_{REF} = 0, T_J = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C_T = .001mfd, R_T = 2kΩ		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	V_{IN} = 8 to 40V, T_J = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			5			5	%
Output Amplitude	Pin 3, T_J = 25°C		3.5			3.5		V
Output Pulse Width	C_T = .01mfd, T_J = 25°C		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T_J = 25°C	1.8		3.4	1.8		3.4	V
Common Mode Rejection Ratio	T_J = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		3			3		MHz
Output Voltage	T_J = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		µA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_J = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage		-1		+1	-1		+1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	µA
Saturation Voltage	I_C = 50mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18		17	18		V
Rise Time	R_C = 2k ohm, T_J = 25°C		0.2			0.2		µs
Fall Time	R_C = 2k ohm, T_J = 25°C		0.1			0.1		µs
Total Standby Current	V_{IN} = 40V		8	10		8	10	mA
(Excluding oscillator charging current, error and current limit dividers, and with outputs open)								

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, Vcc (Notes 2 and 3) 40V
Collector Output Current 100mA
Reference Output Current 50mA
Current Through CT Terminal ..... -5mA
Power Dissipation at TA = +25°C (Note 4) 1000mW
Power Dissipation at TC = +25°C (Note 4) 2000mW
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C

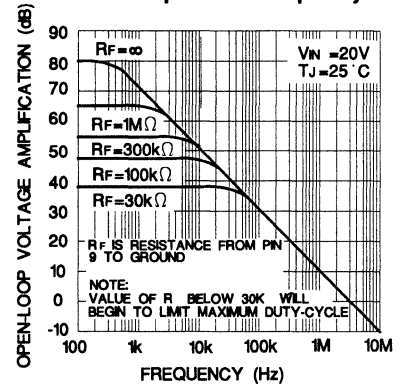
Note 1: Over operating free-air temperature range unless otherwise noted.
Note 2: All voltage values are with respect to the ground terminal, pin 8.
Note 3: The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the Vcc and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.
Note 4: Consult packaging section of databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

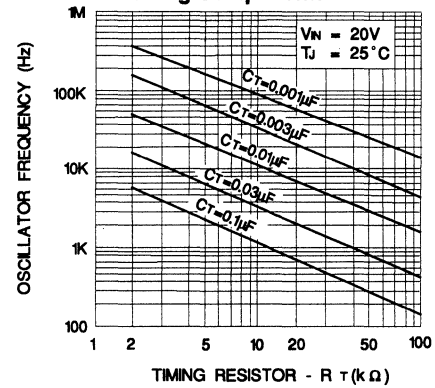
Supply Voltage, Vcc ..... 8V to 40V
Reference Output Current ..... 0 to 20mA
Current through CT Terminal ..... -0.03mA to -2mA
Timing Resistor, RT ..... 1.8kΩ to 100kΩ
Timing Capacitor, CT ..... 0.001μF to 0.1μF
Operating Ambient Temperature Range
UC1524 ..... -55°C to +125°C
UC2524 ..... -25°C to +85°C
UC3524 ..... 0°C to +70°C

TYPICAL CHARACTERISTICS

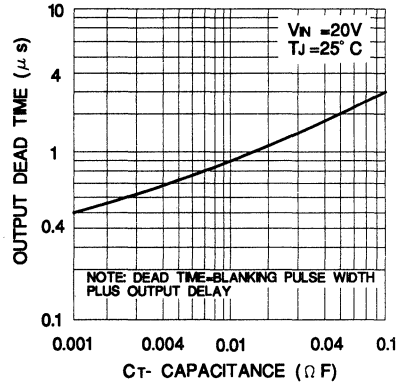
Open-Loop Voltage Amplification of Error Amplifier vs Frequency



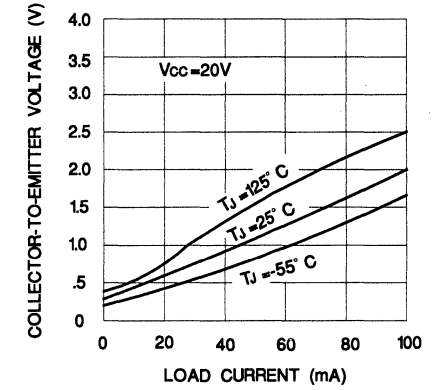
Oscillator Frequency vs Timing Components



Output Dead Time vs Timing Capacitance Value



Output Saturation Voltage vs Load Current



PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T), R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the valve of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

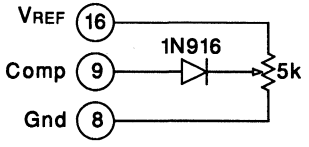
$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

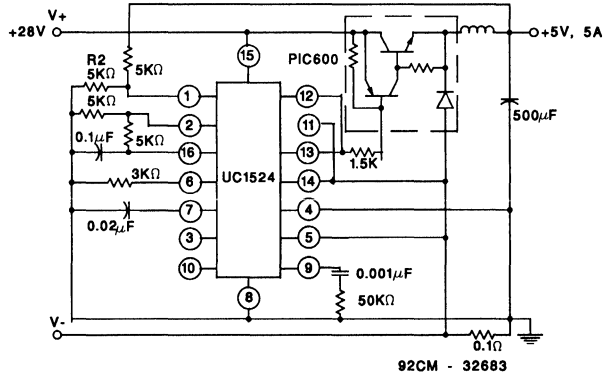


Synchronous Operation

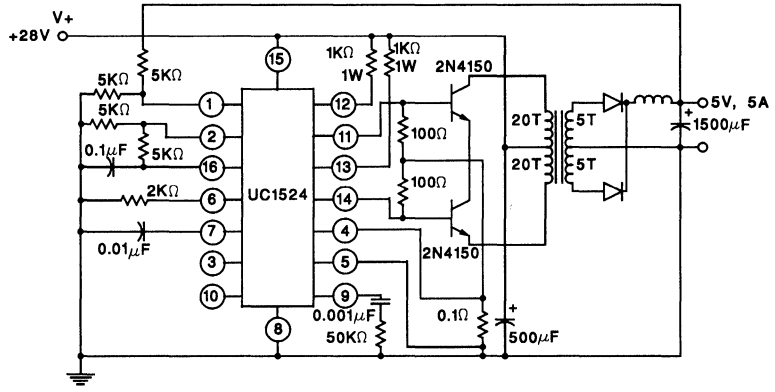
When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T, terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

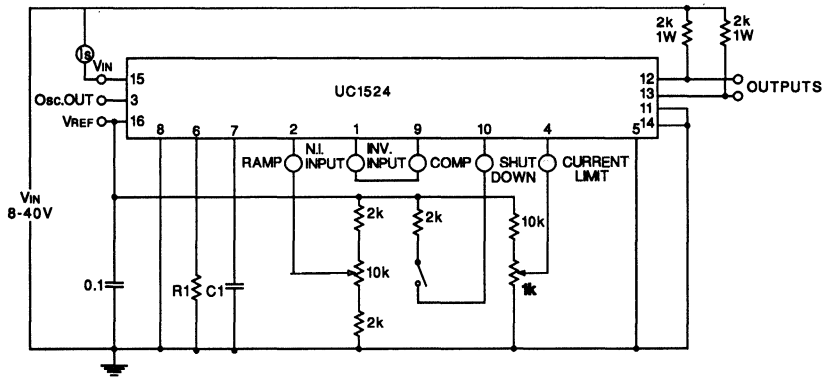
Single-Ended LC Switching Regulator Circuit



Push Pull Transformer Coupled Circuit



Open Loop Test Circuit



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Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family
- Precision Reference Internally Trimmed to ±1%
- High-Performance Current Limit Function
- Under-Voltage Lockout with Hysteretic Turn-on
- Start-Up Supply Current Less Than 4mA
- Output Current to 200mA
- 60V Output Capability
- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression Logic
- 200ns Shutdown through PWM Latch
- Guaranteed Frequency Accuracy
- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

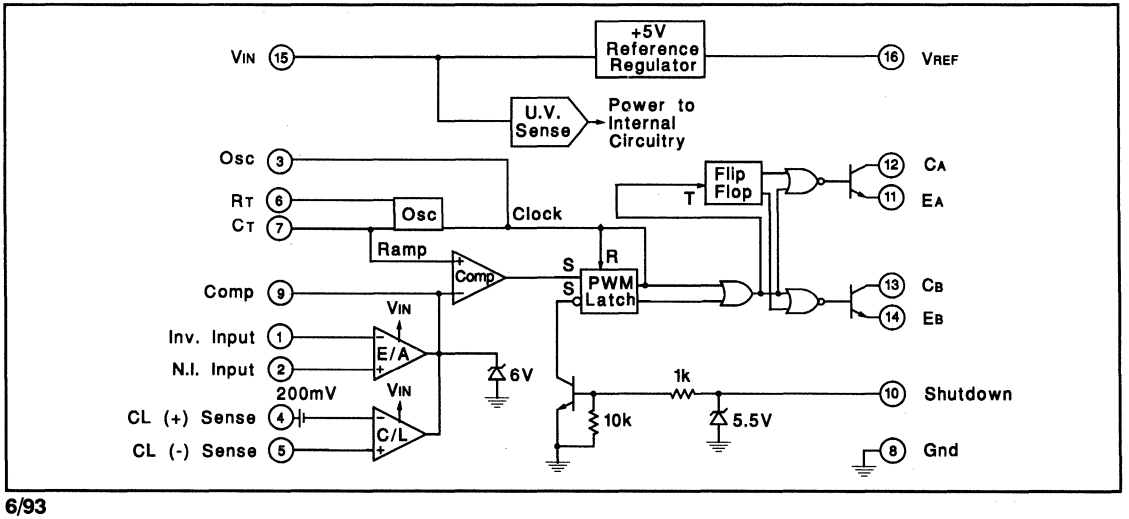
The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.

BLOCK DIAGRAM

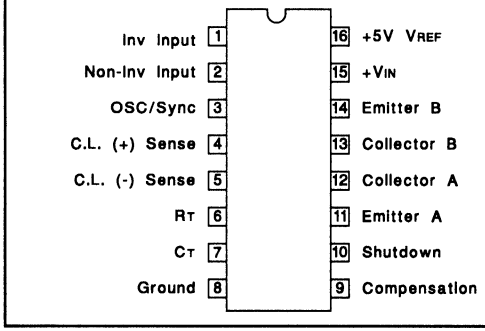


6/93

ABSOLUTE MAXIMUM RATINGS

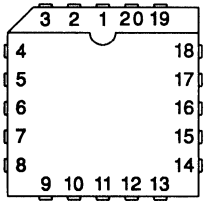
Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) ..... -3 to +5V
Maximum Forced Current (Pin 9, 10) ..... ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) ..... +300°C
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
RT	8
CT	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+VIN	19
+5V VREF	20

5

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T_J =25°C		40			40		μVrms
Long Term Stability*	T_J =125°C, 1000 Hrs.		20	50		20	50	mV

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq 10M\Omega$	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	$V_{(pin\ 5)}$ = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq 10M\Omega$	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

** These parameters are guaranteed by design but not 100% tested in production.*

§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to the common mode voltage.

The minimum g_M specification is used to calculate minimum Av when the error amplifier output is loaded.

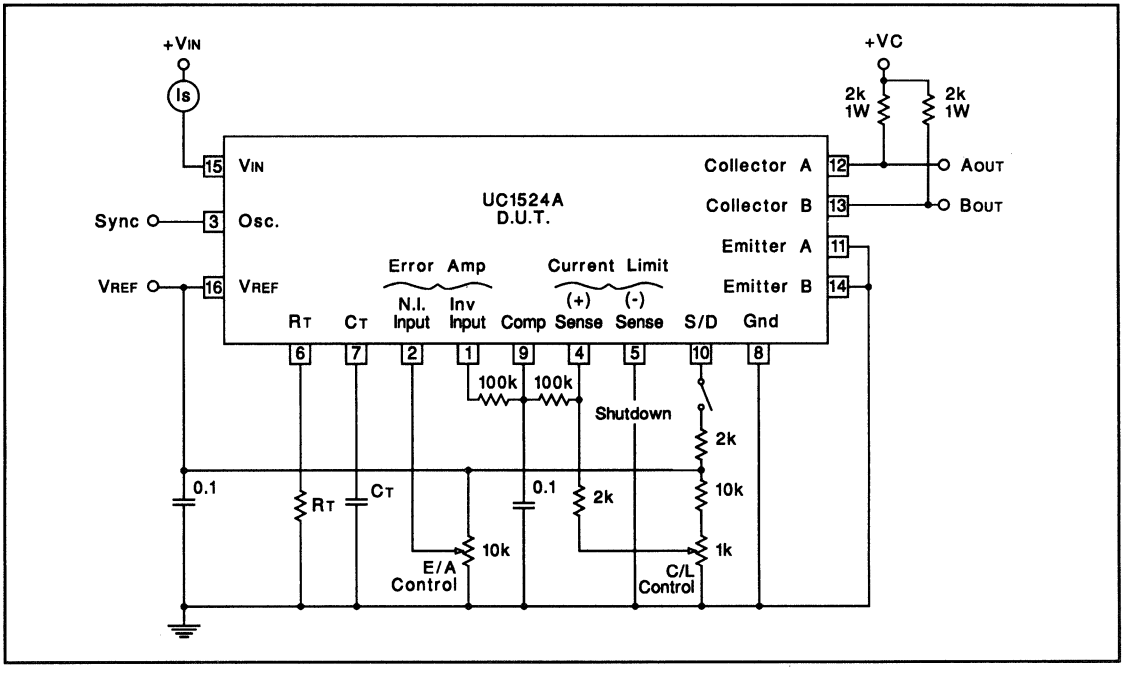
Note 1: Min Limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

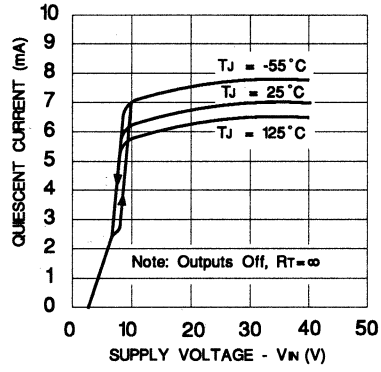
PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

** These parameters are guaranteed by design but not 100% tested in production.*

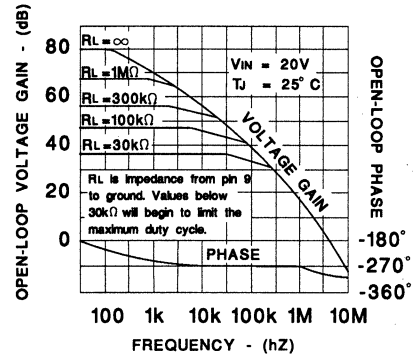
OPEN-LOOP CIRCUIT



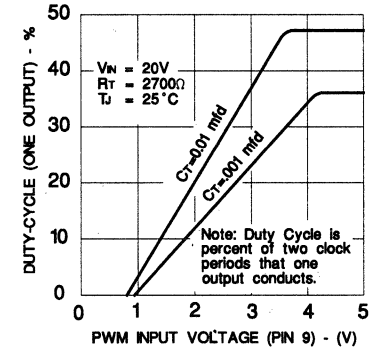
Supply Current vs Voltage



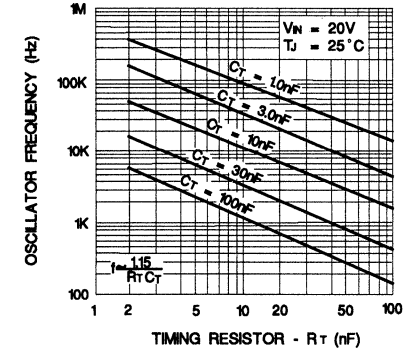
Error Amplifier Voltage Gain and Phase vs Frequency



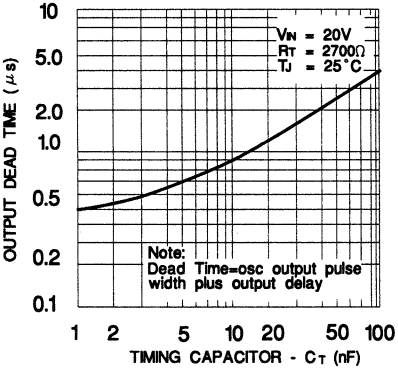
Pulse Width Modulator Transfer Function



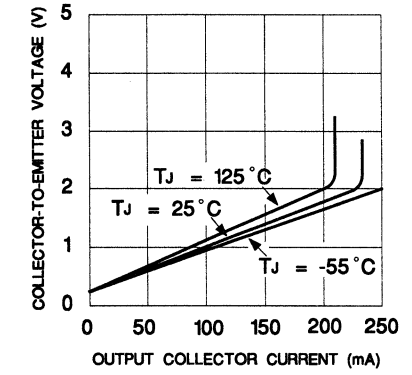
Oscillator Frequency vs Timing Components



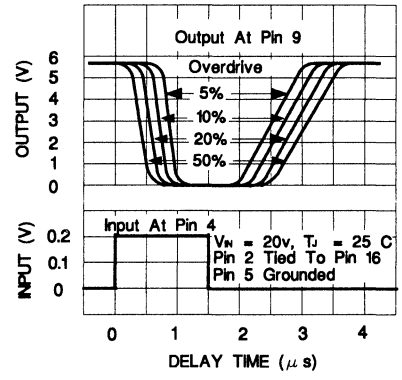
Output Dead Time vs Timing Capacitor Value



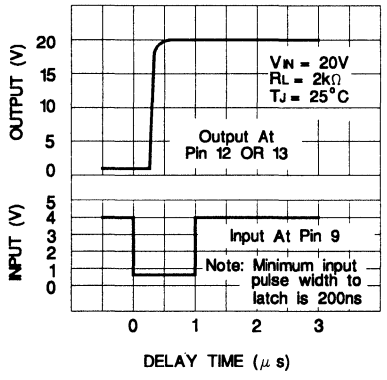
Output Saturation Voltage



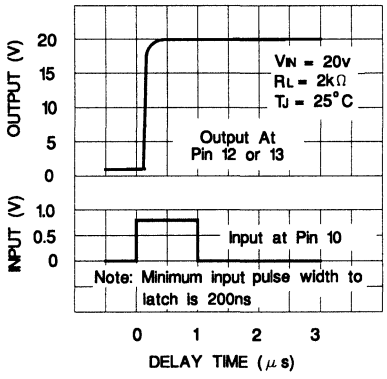
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator - Pin 9



Turn-Off Delay From Shutdown - Pin 10



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INTEGRATED CIRCUITS
UNITRODE

UC1525A/27A
UC2525A/27A
UC3525A/27A

Regulating Pulse Width Modulators

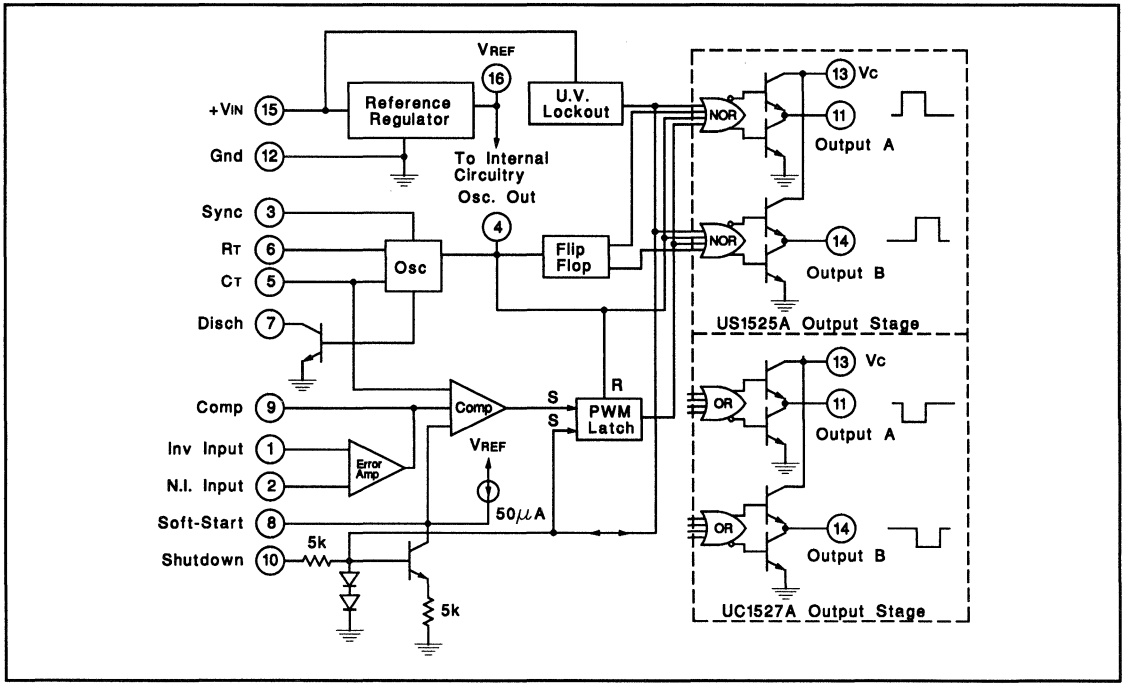
FEATURES

- 8 to 35V Operation
- 5.1V Reference Trimmed to ±1%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (+VIN) ..... +40V
Collector Supply Voltage (VC) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +VIN
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at TC = +25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.

Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

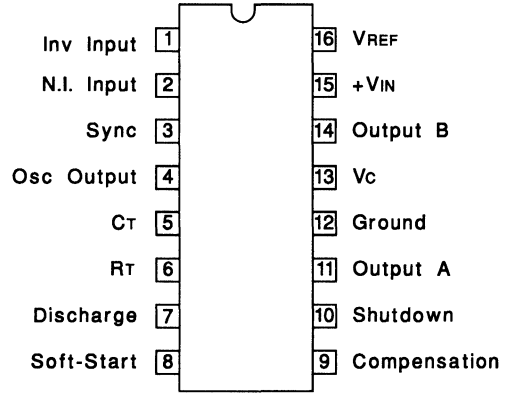
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage (+VIN) ..... +8V to +35V
Collector Supply Voltage (VC) ..... +4.5V to +35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... .001μF to 0.1μF
Dead Time Resistor Range ..... 0 to 500Ω
Operating Ambient Temperature Range
UC1525A, UC1527A ..... -55°C to +125°C
UC2525A, UC2527A ..... -25°C to +85°C
UC3525A, UC3527A ..... 0°C to +70°C

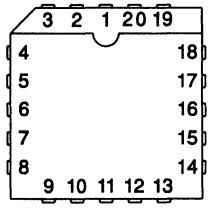
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
N.I. Input	3
SYNC	4
OSC. output	5
N/C	6
CT	7
RT	8
Discharge	9
Softstart	10
N/C	11
Compensation	12
Shutdown	13
Output A	14
Ground	15
N/C	16
VC	17
Output B	18
+VIN	19
VREF	20

5

ELECTRICAL CHARACTERISTICS: +V_{IN} = 20V, and over operating temperature, unless otherwise specified, T_A = T_J

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Shorter Circuit Current	V_{REF} = 0, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T_J = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T_J = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_J = 25°C		± 2	± 6		± 2	± 6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 to 35V		± 0.3	± 1		± 1	± 2	%
Temperature Stability (Note 5)	Over Operating Range		± 3	± 6		± 3	± 6	%
Minimum Frequency	R_T = 200kΩ, C_T = 0.1μF			120			120	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R_L ≥ 10MΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at fosc = 40kHz (R_T = 3.6kΩ, C_T = 0.01μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

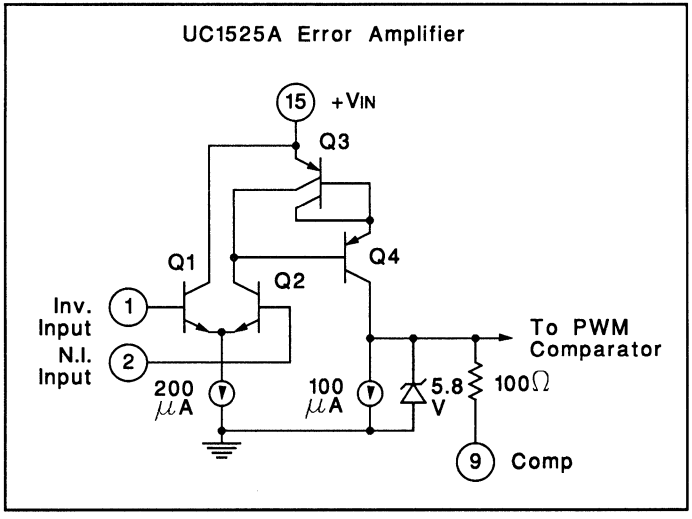
$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

Note 7: DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground..
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 20V, and over operating temperature, unless otherwise specified, T_A = T_J

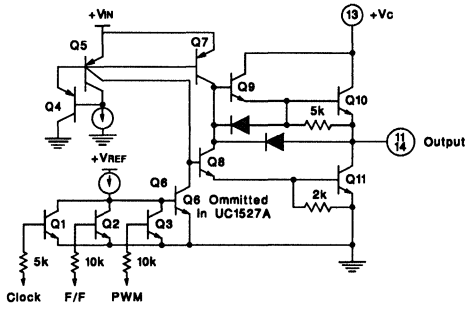
PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	µA
Shutdown Section								
Soft Start Current	V_{SD} = 0V, V_{SS} = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	V_{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V_{SS} = 5.1V, T_J = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V_{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V_{SD} = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Under-Voltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
V_C OFF Current (Note 7)	V_C = 35V			200			200	µA
Rise Time (Note 5)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 6: Tested at fosc = 40kHz (R_T = 3.6kΩ, C_T = 0.01µF, R_D = 0Ω).
Note 7: Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

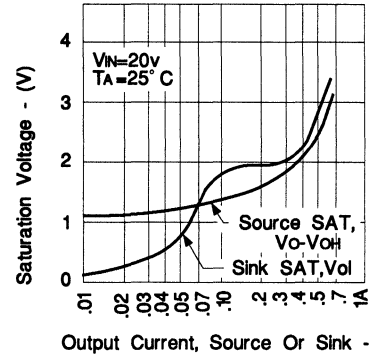


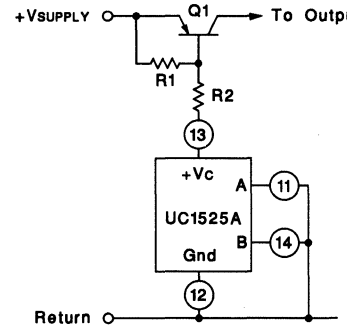
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A Output Circuit (1/2 Circuit Shown)

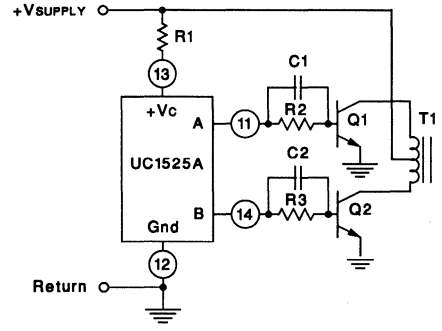


UC1525A Output Saturation Characteristics

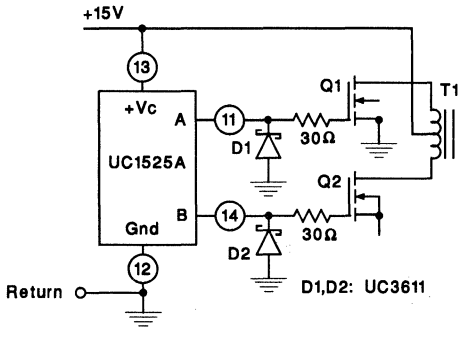




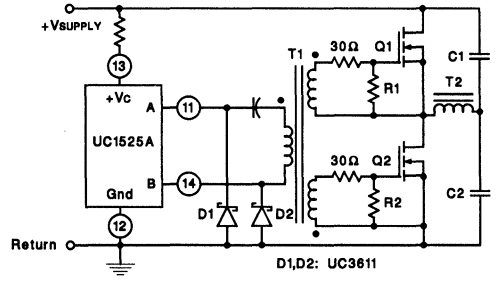
For single-ended supplies, the driver outputs are grounded. The Vc terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



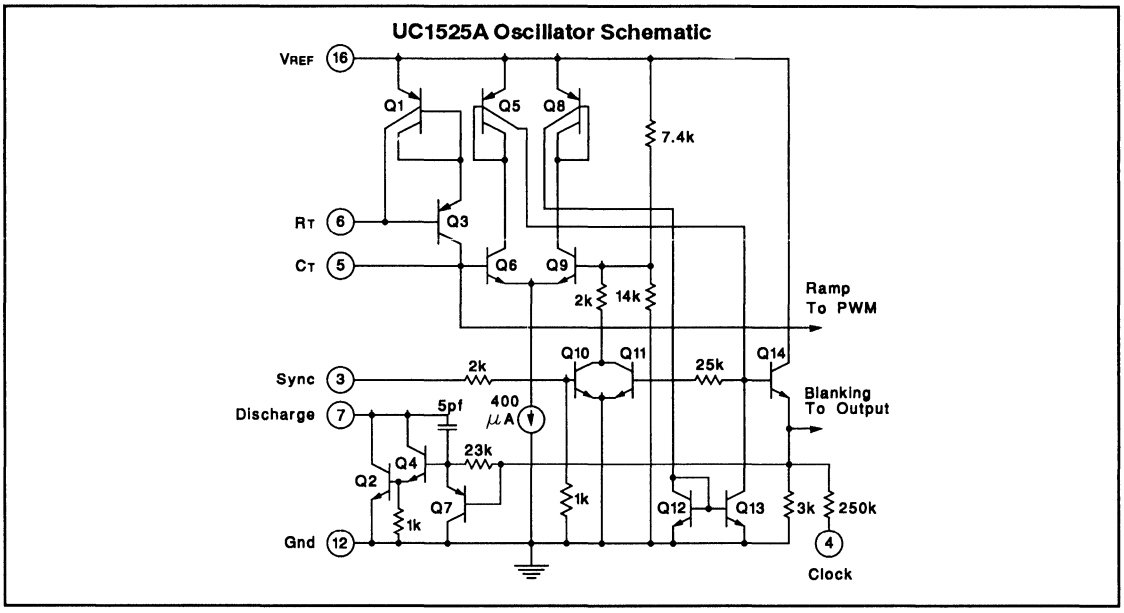
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.



The low source impedance of the output drivers provides rapid charging of power FET Input capacitance while minimizing external components.



Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.



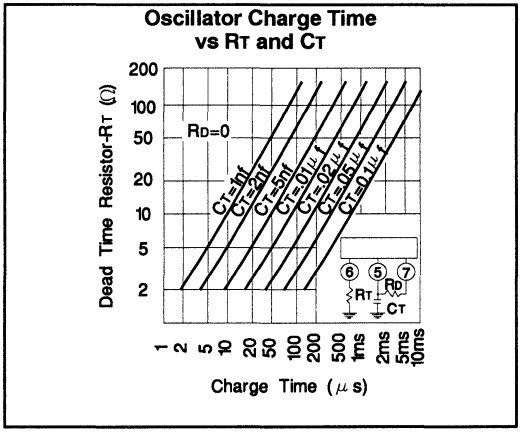
5

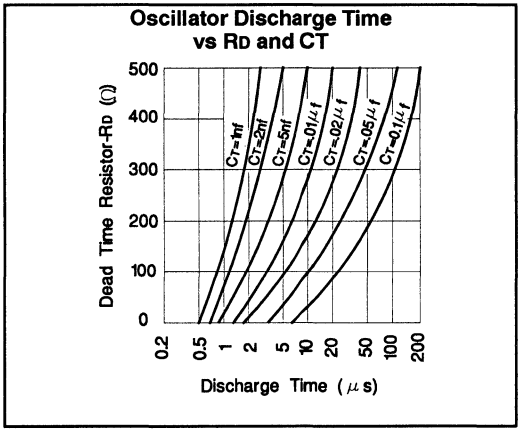
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTIC SHUTDOWN OPTIONS
(See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

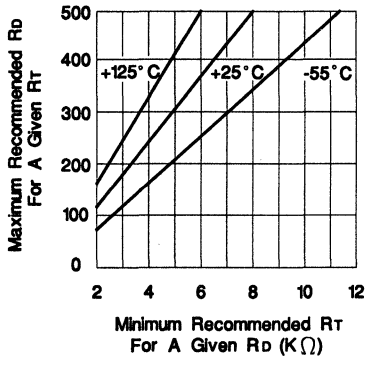
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150μA-current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

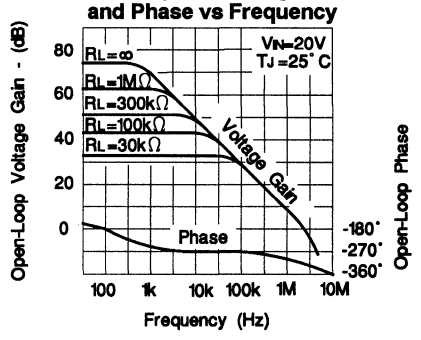




Maximum Value RD vs Minimum Value RT

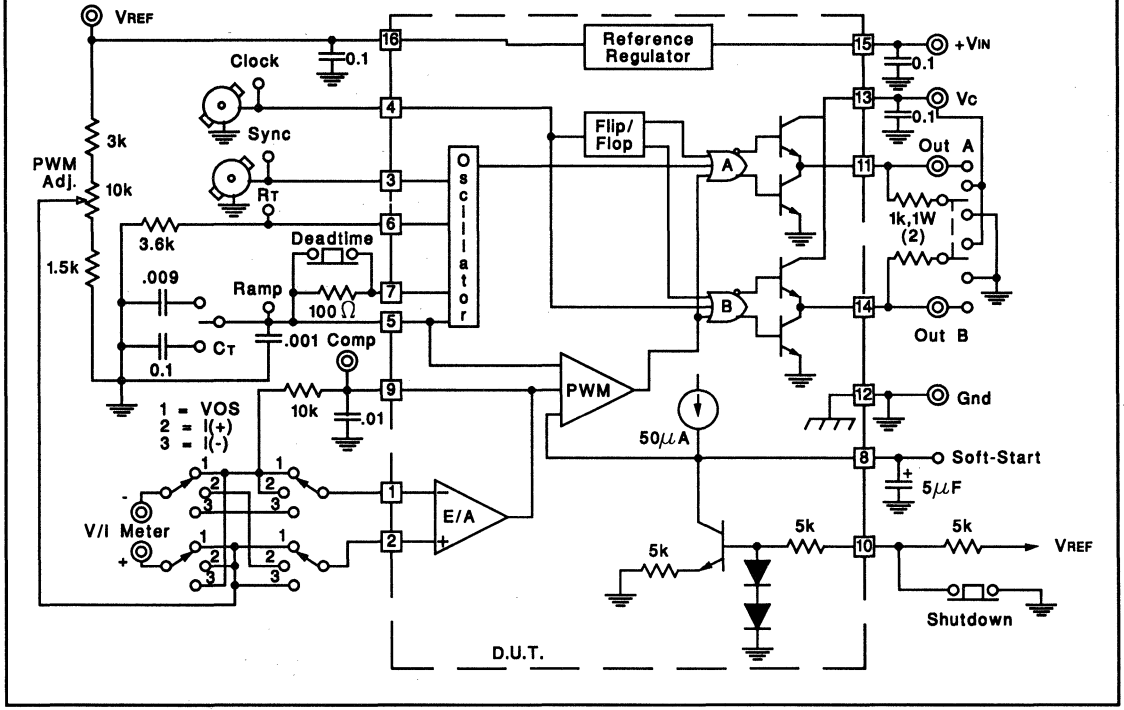


Error Amplifier Voltage Gain and Phase vs Frequency



RL is impedance from pin 9 to ground. Values below 30kΩ will begin to limit the maximum duty cycle.

LAB TEST FIXTURE



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INTEGRATED CIRCUITS
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Regulating Pulse Width Modulators

UC1525B UC1527B
UC2525B UC2527B
UC3525B UC3527B

FEATURES

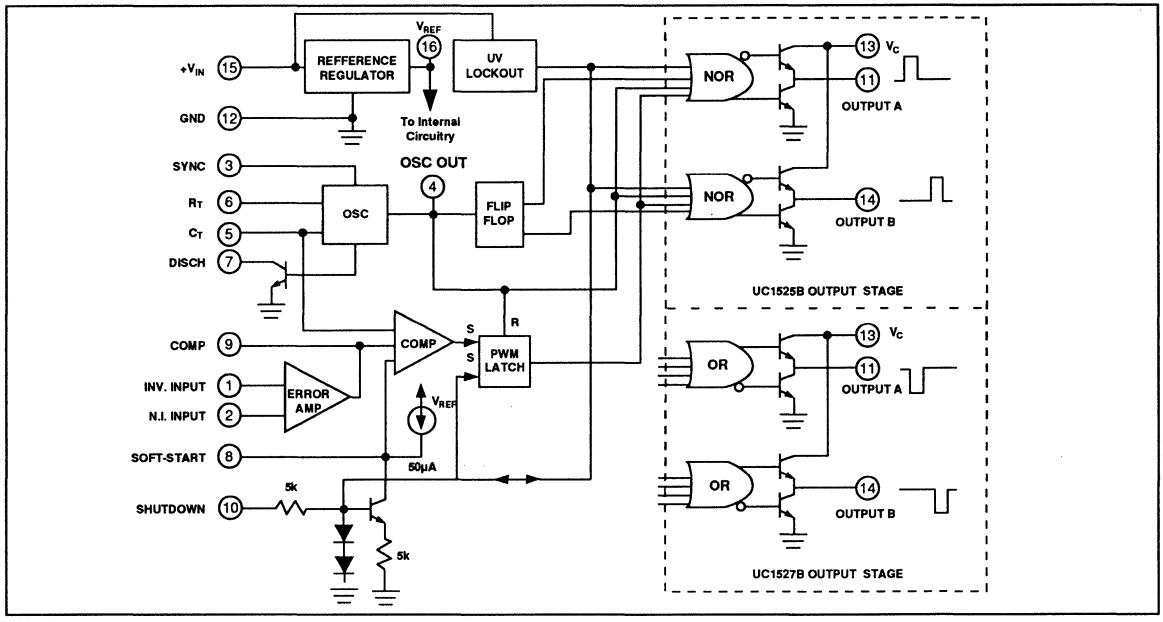
- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to ± .75%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

DESCRIPTION

The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to ±.75% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.

5

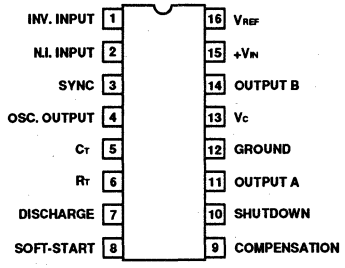
BLOCK DIAGRAM



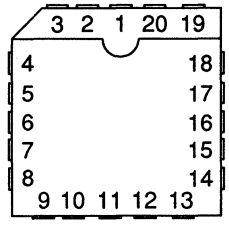
12/92

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N Package, DW Package



PLCC-20, LCC-20 (Top View)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV INPUT	2
N.I. INPUT	3
SYNC	4
OSC. OUTPUT	5
N/C	6
C_T	7
R_T	8
DISCHARGE	9
SOFT-START	10
N/C	11
COMPENISATION	12
SHUTDOWN	13
OUTPUT A	14
GROUND	15
N/C	16
V_C	17
OUTPUT B	18
$+V_{IN}$	19
V_{REF}	20

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, ($+V_{IN}$) ..... +40V
Collector Supply Voltage (V_C) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to $+V_{IN}$
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A= +25°C (Note 2) 1000mW
Power Dissipation at T_C= +25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Note 1: *Values beyond which damage may occur.*

Note 2: *Consult packaging section of databook for thermal limitations and considerations of package.*

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage ($+V_{IN}$) ..... +8V to +35V
Collector Supply Voltage (V_C) ..... +4.5V to +35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... .001µF to 0.1µF
Dead Time Resistor Range ..... 0 to 500Ω
Operating Ambient Temperature Range
UC1525B, UC1527B ..... -55°C to +125°C
UC2525B, UC2527B ..... -40°C to +85°C
UC3525B, UC3527B ..... 0°C to +70°C

Note 3: *Range over which the device is functional and parameter limits are guaranteed.*

ELECTRICAL CHARACTERISTICS: $+V_{IN}$ = 20V, and over operating temperature, unless otherwise specified

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.062	5.10	5.138	5.036	5.10	5.164	V
Line Regulation	V_{IN} = 8 to 35V		5	10		5	10	mV
Load Regulation	I_L = 0 to 20mA		7	15		7	15	mV
Temperature Stability (Note 5)	Over Operating Range		10	30		10	30	mV
Total Output Variation	Line, Load, and Temperature	5.036		5.164	5.024		5.176	V
Short Circuit Current	V_{REF} = 0, T_J =25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ f ≤ 10kHz, T_J = 25°C		40	200		40	200	µVrms
Long Term Stability (Note 5)	T_J = 125°C, 1000 Hrs.		3	10		3	10	mV

ELECTRICAL CHARACTERISTICS: $+V_{IN}$ = 20V, and over operating temperature, unless otherwise specified

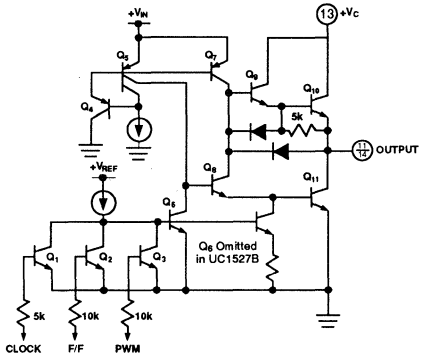
PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_J = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 TO 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 5)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	RT = 200kΩ, C_T = 0.1µF			120			120	Hz
Maximum Frequency	RT = 2kΩ, C_T= 470pF	400			400			kHz
Current Mirror	IRT = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (VCM = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	RL ≥10 Meg Ω	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cysle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 6)	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	µA
Shutdown Section								
Soft Start Current	V_{SD} = 0V, V_{SS} = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	V_{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V_{SS} = 5.1V, T_J=25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V_{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V_{SD} = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µS
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and V_{SS} = high	6	7	8	6	7	8	V
Collector Leakage	V_C= 35V			200			200	µA
Rise Time (Note 5)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Cross conduction charge	Per cycle, T_J = 25°C		30			30		nc
Total Standby Current								
Supply Current	V_{IN}= 35V		14	20		14	20	mA

Notes: 5. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

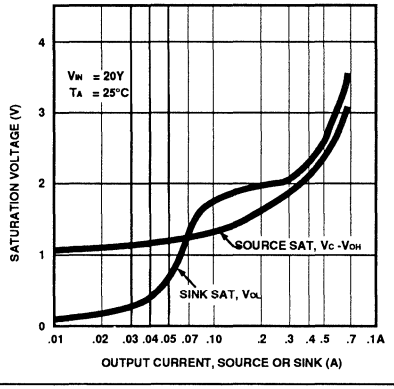
6. Tested at fosc= 40khz (R_T = 3.6Ω, C_T = .01µF, R_D = 0Ω). Approximate oscillator frequency is defined by: $f = \frac{1}{C_T(0.7R_T+3R_D)}$

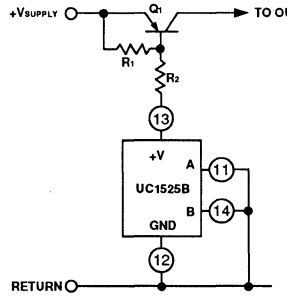
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525B OUTPUT CIRCUIT
(1/2 Circuit Shown)



UC1525B OUTPUT SATURATION CHARACTERISTICS





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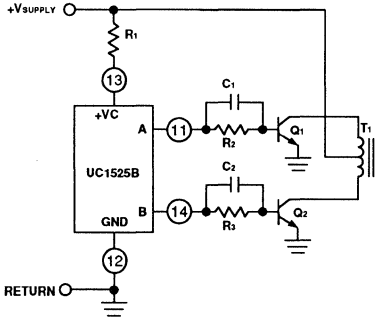

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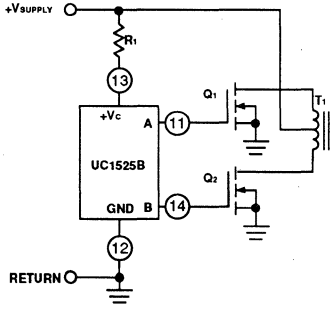

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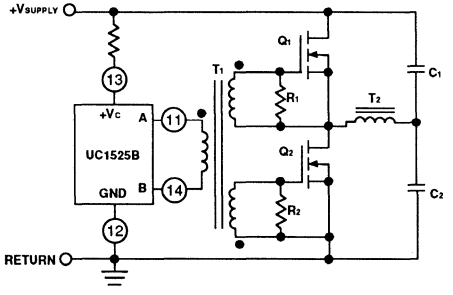

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PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

SHUTDOWN OPTIONS (See Block Diagram)

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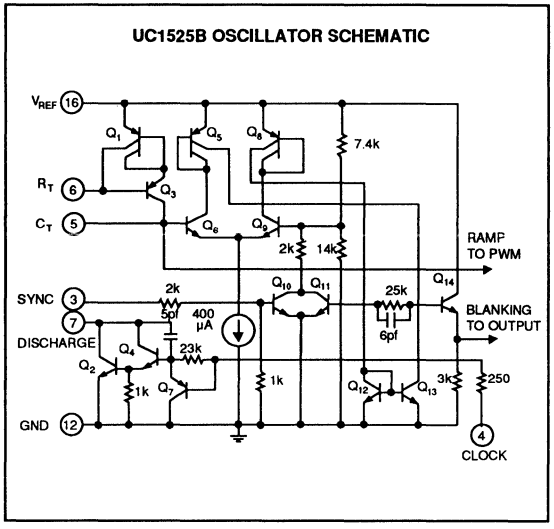
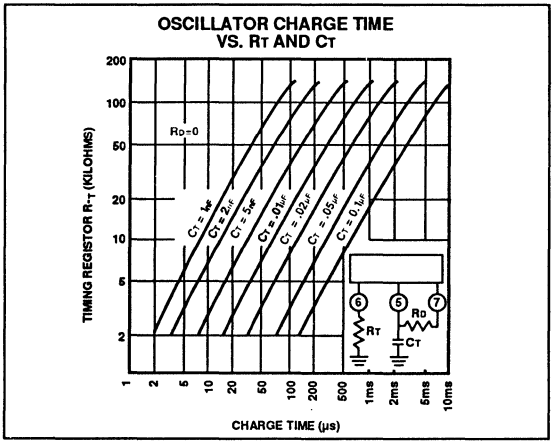
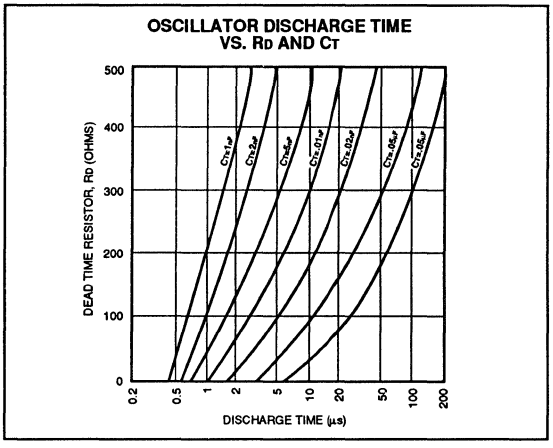
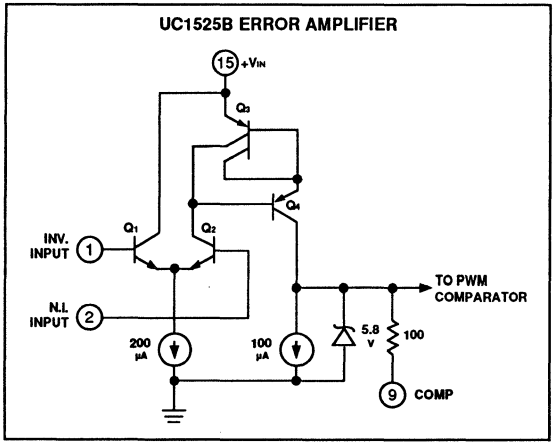
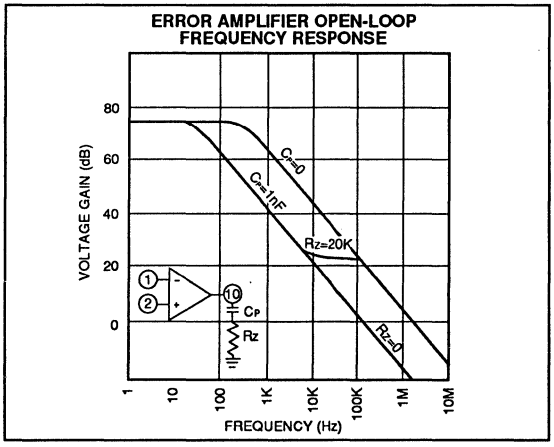




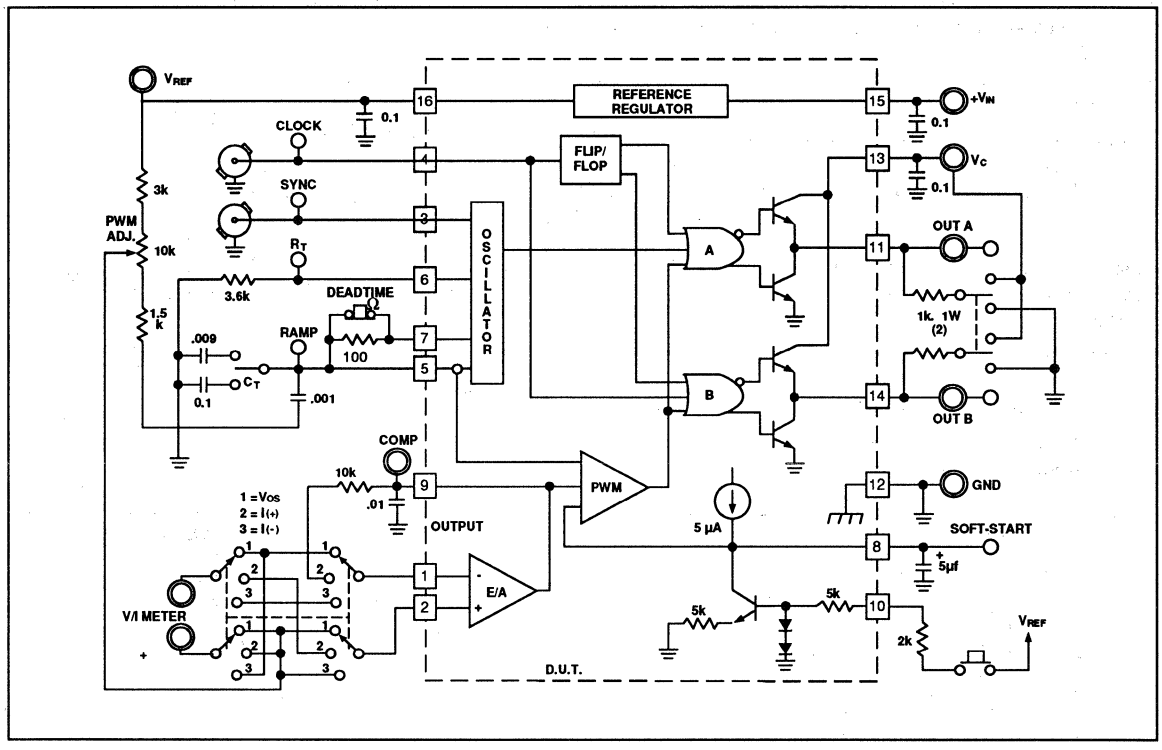






5

LAB TEST FIXTURE



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Regulating Pulse Width Monitor

FEATURES

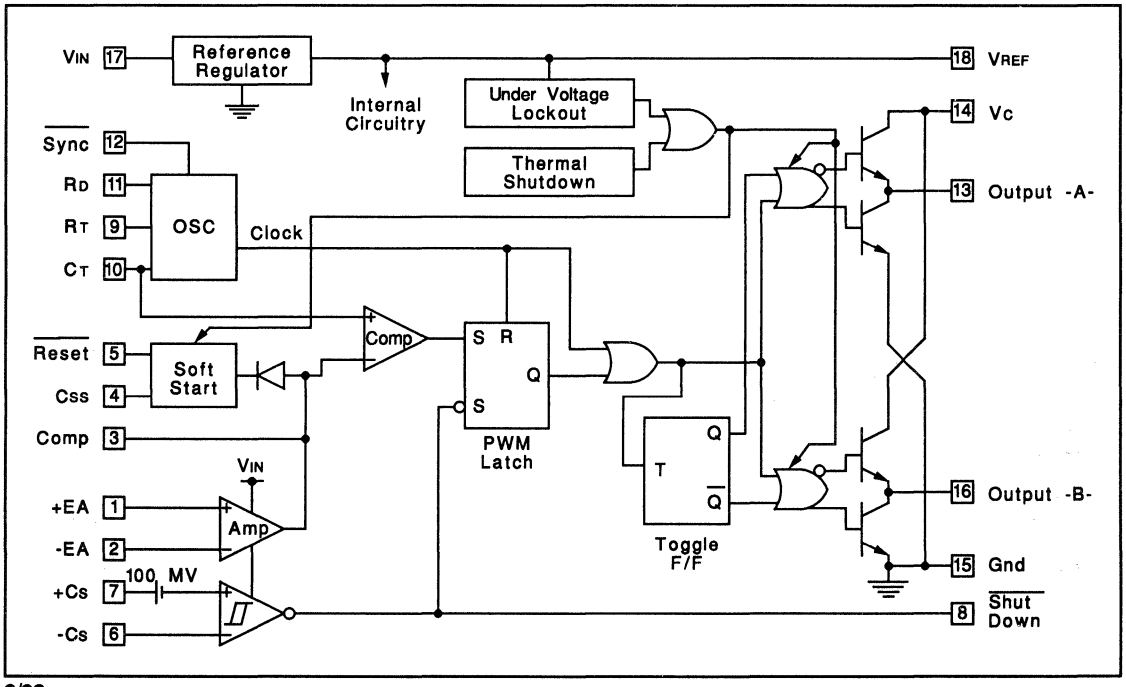
- 8 To 35V Operation
- 5V Reference Trimmed To ±1%
- 1Hz To 400kHz Oscillator Range
- Dual 100mA Source/Sink Outputs
- Digital Current Limiting
- Double Pulse Suppression
- Programmable Deadtime
- Under-Voltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- TTL/CMOS Compatible Logic Ports
- Symmetry Correction Capability
- Guaranteed 6 Unit Synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and setting logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2526 is characterized for operation from -25°C to +85°C, and the UC3526 is characterized for operation from 0° to +70°C.

5

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+VIN) ..... +40V
Collector Supply Voltage (+Vc) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +VIN
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at Tc = +25°C (Note 2) 3000mW
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging section of databook for thermal limitations and considerations of package.

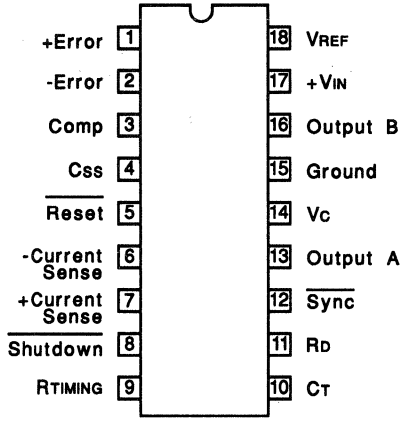
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage ..... +8V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 1nF to 20μF
Available Deadtime Range at 40kHz ..... 3% to 50%
Operating Ambient Temperature Range
UC1526 ..... -55°C to +125°C
UC2526 ..... -25°C to +85°C
UC3526 ..... -0°C to +70°C

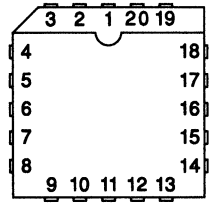
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+Error	2
-Error	3
Comp.	4
Css	5
Reset	6
- Current Sense	7
+ Current Sense	8
Shutdown	9
RTIMING	10
CT	11
RD	12
Sync	13
Output A	14
Vc	15
N/C	16
Ground	17
Output B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	TJ = + 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 8 to 35V		10	20		10	30	mV
Load Regulation	IL = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating TJ		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	VREF = 0V	25	50	100	25	50	100	mA
Under -Voltage Lockout								
RESET Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
	VREF = 4.8V	2.4	4.8		2.4	4.8		V

Note 4: IL = 0mA.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 5)								
Initial Accuracy	T_J = + 25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 6)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	V_{PIN1}-V_{PIN2} ≥ 150mV, I_{SOURCE} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V_{PIN2}-V_{PIN1} ≥ 150mV, I_{SINK} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 12kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 5)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} =40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA
Current Limit Comparator (Note 7)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ =+2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output) (Note 8)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	μA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	μs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	μs
Power Consumption (Note 9)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		18	30		18	30	mA

Note 4: I_L = 0mA.
Note 5: Fosc = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.1μF ± 1%, R_D = 0Ω)
Note 6: V_{CM} = 0 to +5.2V
Note 8: V_C = +15V
Note 9: +V_{IN} = +35V, R_T = 4.12kΩ

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

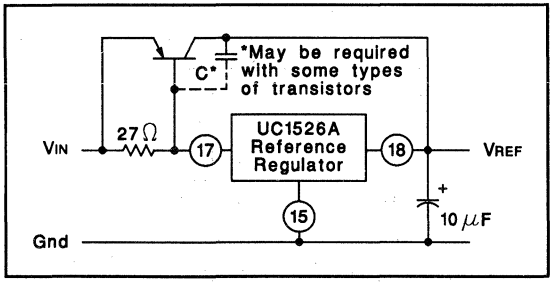


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

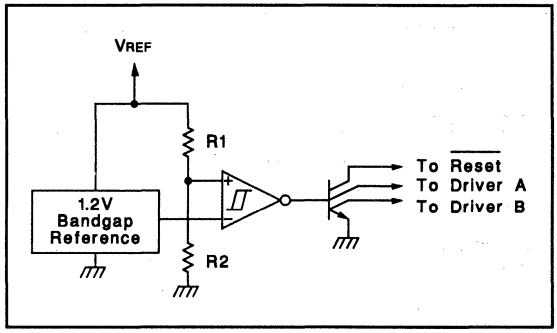


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100mA current source to charge Cs. Q2 clamps the error amplifier output to 1VBE above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

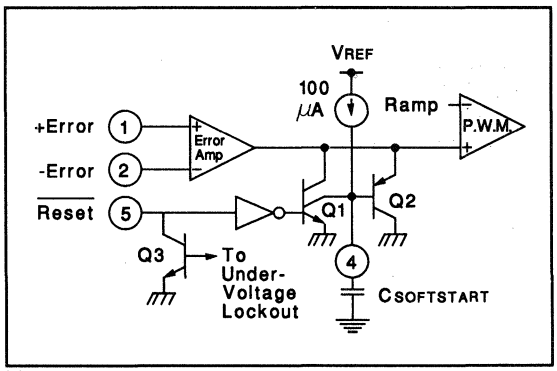


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector

APPLICATIONS INFORMATION (cont.)

TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

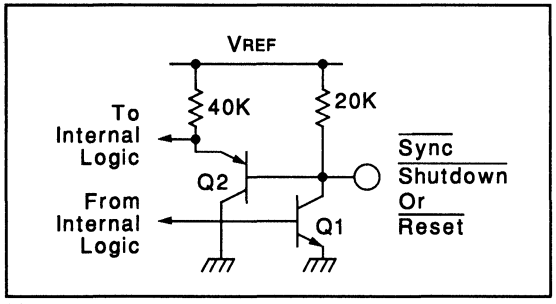


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD = 0 (pin 11 shorted to ground) select values for RT and CT from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.

2. If more dead time is required, select a large value of RD. At 40kHz dead time increases by 400ns/Ω .

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminals may be either left open or grounded.

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

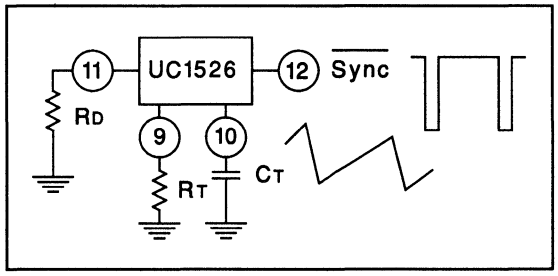


Figure 5. Oscillator Connections and Waveforms

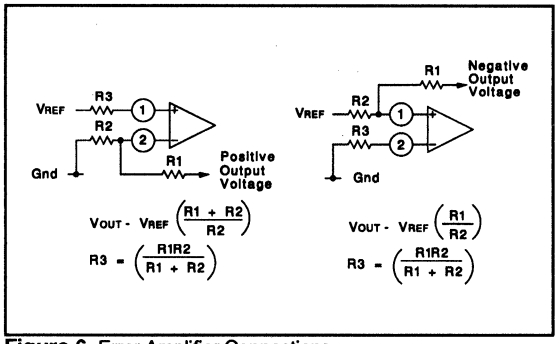


Figure 6. Error Amplifier Connections

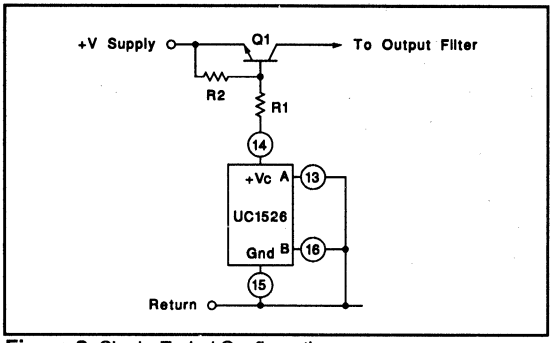


Figure 8. Single-Ended Configuration

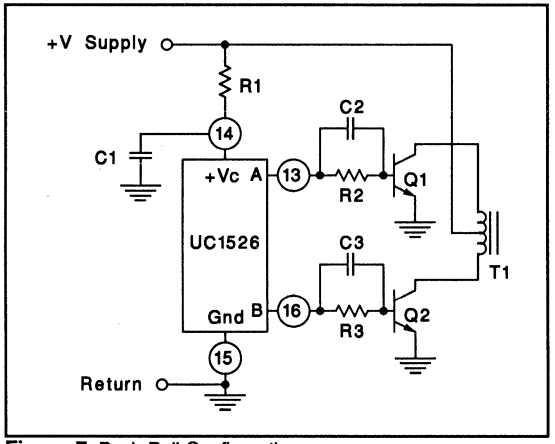


Figure 7. Push-Pull Configuration

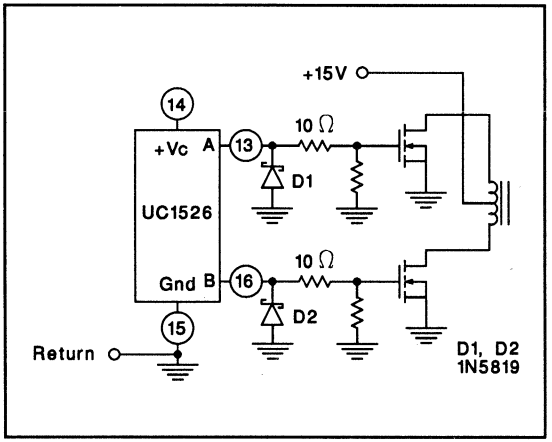
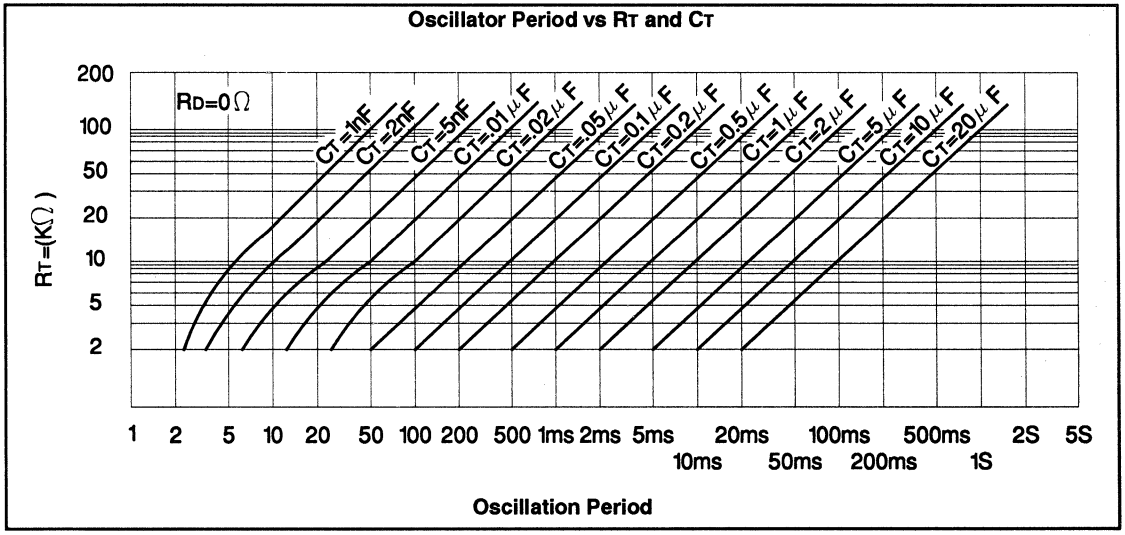


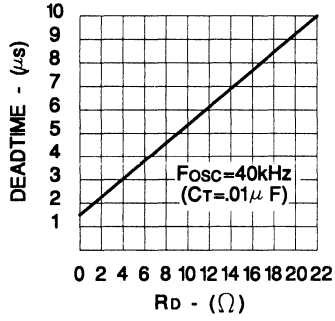
Figure 9. Driving N-channel Power Mosfets

TYPICAL CHARACTERISTICS

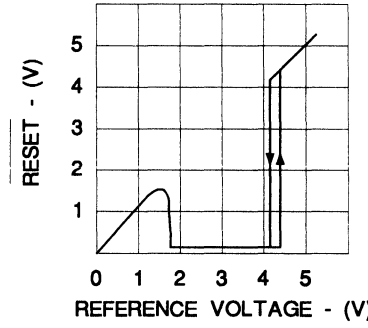


TYPICAL CHARACTERISTICS

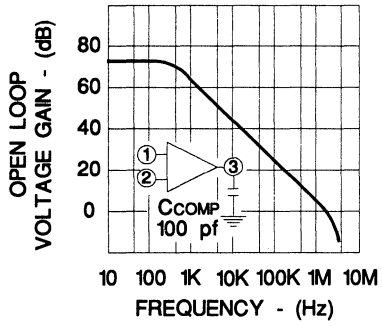
Output Driver Deadtime vs RD Value



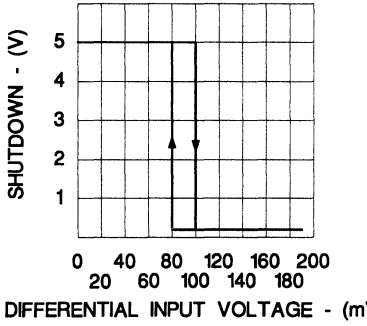
Under Voltage Lockout Characteristic



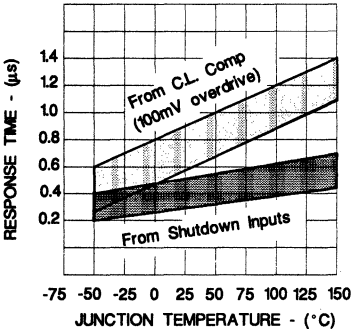
Error Amplifier Open Loop Gain vs Frequency



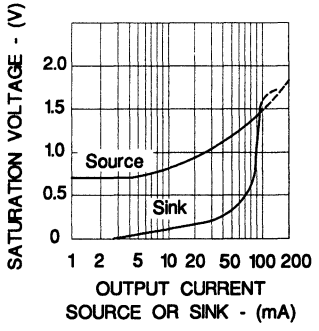
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



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UC1526A
UC2526A
UC3526A

Regulating Pulse Width Modulator

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation (V_{IN} = V_C = V_{REF} = 5.0V)

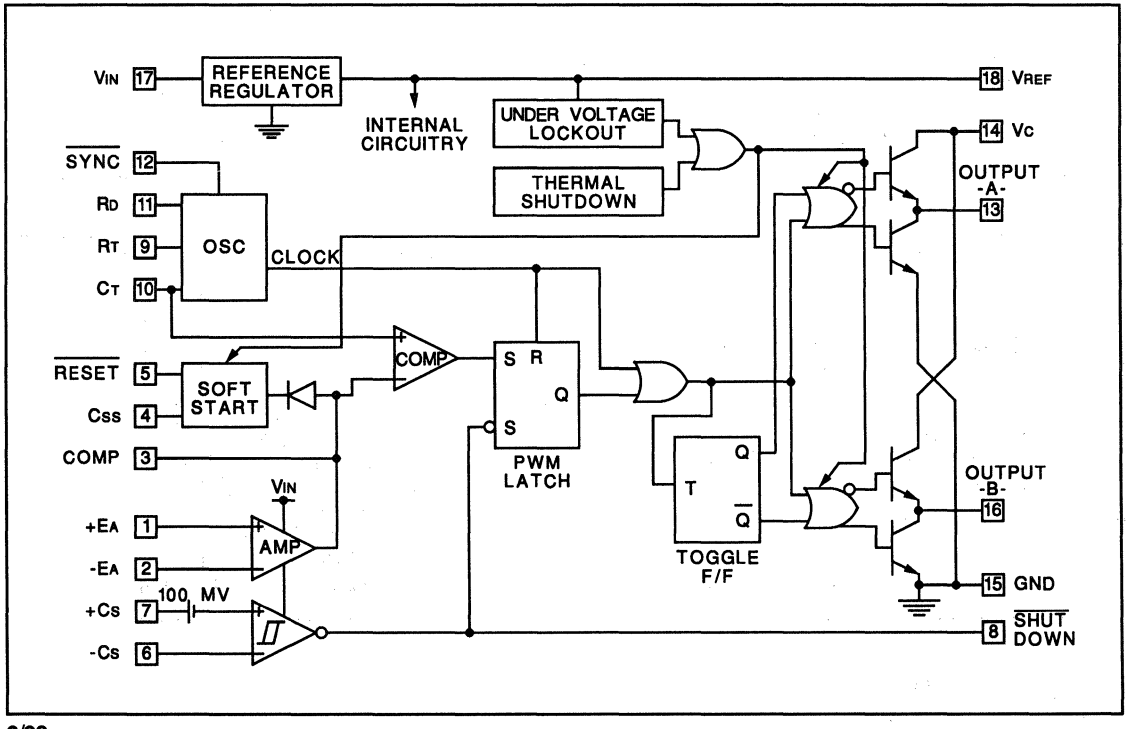
DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting V_{IN}, V_C and V_{REF} to a precision 5V input supply. Consult factory for additional information.

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+V_{IN}) ..... +40V
Collector Supply Voltage (+Vc) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Power Dissipation at T_C = +25°C (Note 2) 3000mW
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

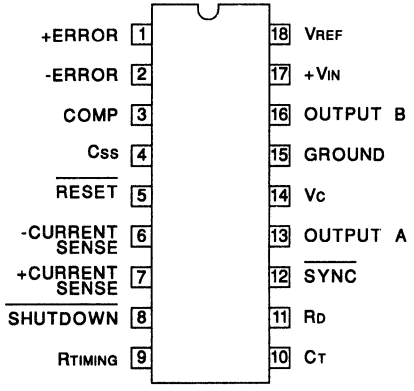
RECOMMENDED OPERATING CONDITIONS

(Note 3)
Input Voltage ..... +7V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 600kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 400pF to 20μF
Available Deadtime Range at 40kHz ..... 1% to 50%
Operating Ambient Temperature Range
UC1526A ..... -55°C to +125°C
UC2526A ..... -25°C to +85°C
UC3526A ..... 0°C to +70°C

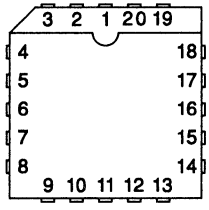
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+ERROR	2
-ERROR	3
COMP.	4
Css	5
RESET	6
- CURRENT SENSE	7
+ CURRENT SENSE	8
SHUTDOWN	9
RTIMING	10
CT	11
RD	12
SYNC	13
OUTPUT A	14
Vc	15
N/C	16
GROUND	17
OUTPUT B	18
+VIN	19
VREF	20

5

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1526A / UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T_J (Note 5)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
	V_{REF} = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J (Note 5)		2	6		1	3	%
Minimum Frequency	R_T = 150kΩ, C_T = 20μF (Note 5)			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} =7V	0.5	1.0		0.5	1.0		V
$\overline{\text{SYNC}}$ Pulse Width	T_J = 25°C, R_L = 2.7kΩ to V_{REF}		1.1			1.1		μs
Error Amplifier Section (Note 7)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	$V_{PIN\,1}$ - $V_{PIN\,2}$ ≥ 150mV, I_{SOURCE} = 100μA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	$V_{PIN\,2}$ - $V_{PIN\,1}$ ≥ 150mV, I_{SINK} = 100μA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{SOURCE} = 40μA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	μA
Shutdown Delay	From Pin 8, T_J = 25°C		160			160		ns
Current Limit Comparator (Note 8)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Delay	From pin 7, 100mV Overdrive, T_J = 25°C		260			260		ns

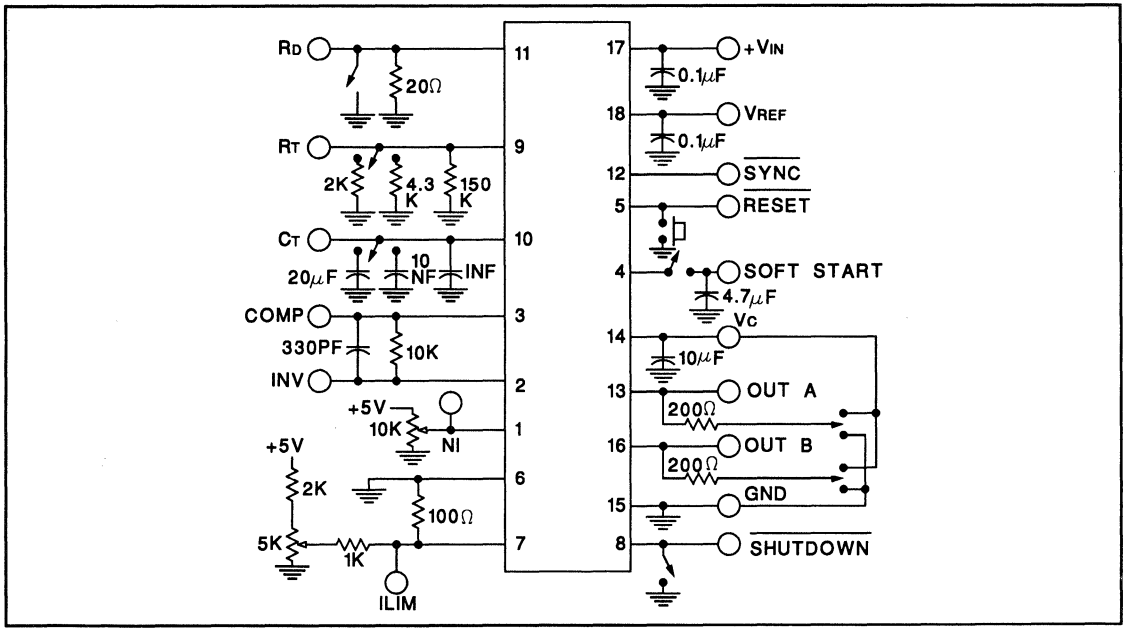
Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: F_{OSC} = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01μF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10: V_{IN} = +35V, R_T = 4.12kΩ.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526A UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF (Note 5)		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF (Note 5)		0.1	0.2		0.1	0.2	µs
Cross-Conduction Charge	Per cycle, T_J = 25°C		8			8		nC
Power Consumption (Note 10)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		14	20		14	20	mA

Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: Fosc = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01µF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10: V_{IN} = +35V, R_T = 4.12kΩ.

Open Loop Test Circuit UC1526A



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

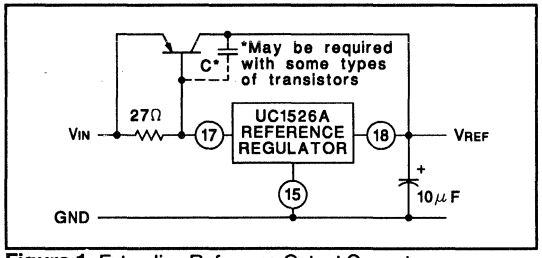


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

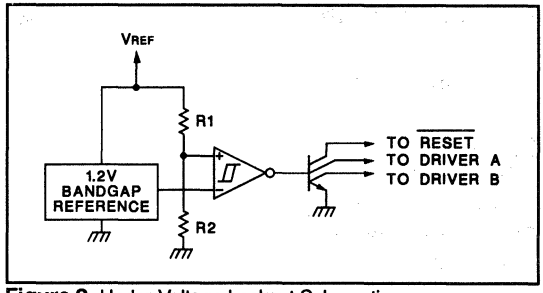


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100μA current source to charge Cs. Q2 clamps the error amplifier output to 1VBE above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

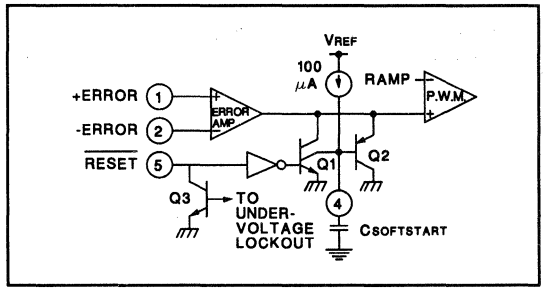


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start

APPLICATIONS INFORMATION (cont.)

capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2K pull-up resistor to +5V.

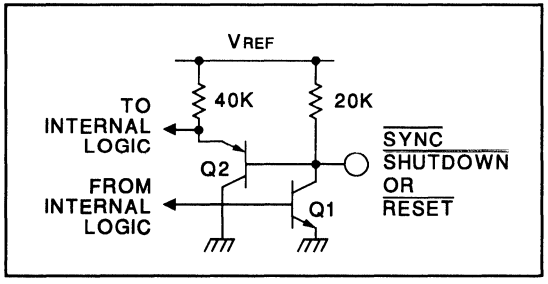


Figure 4. Digital Control Port Schematic

Oscillators

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD= 0Ω (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.

2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by 400ns/Ω.

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the $\overline{SYNC}$ frequency.

A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{SYNC}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all $\overline{SYNC}$ terminals are likewise connected to the $\overline{SYNC}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.

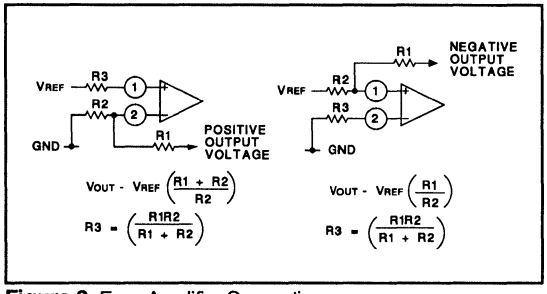


Figure 6. Error Amplifier Connections

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

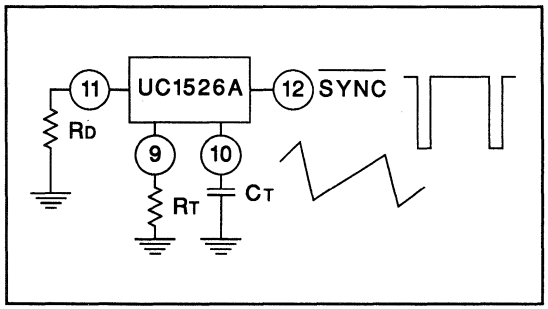


Figure 5. Oscillator Connections and Waveforms

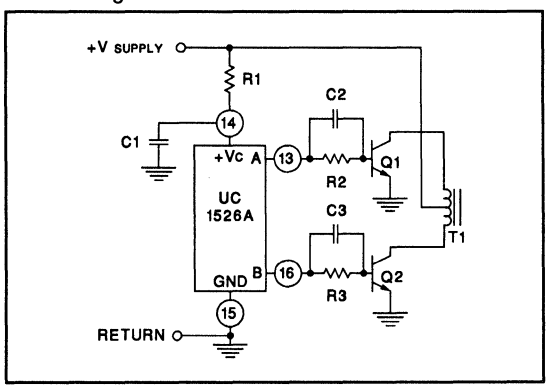


Figure 7. Push-Pull Configuration

APPLICATIONS INFORMATION (cont.)

Output Drivers

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

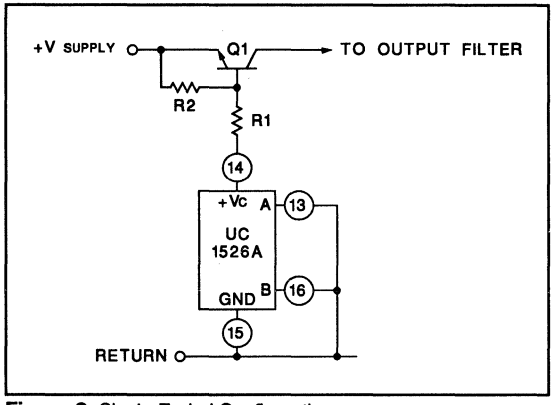


Figure 8. Single-Ended Configuration

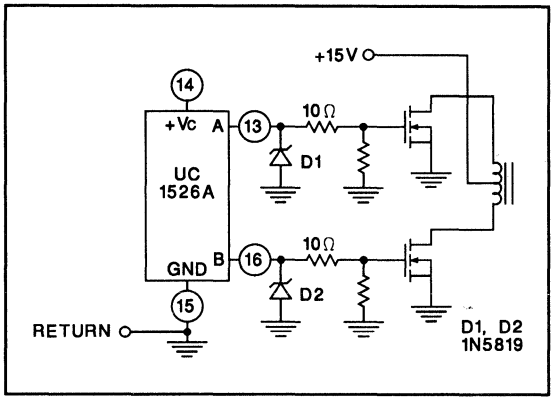
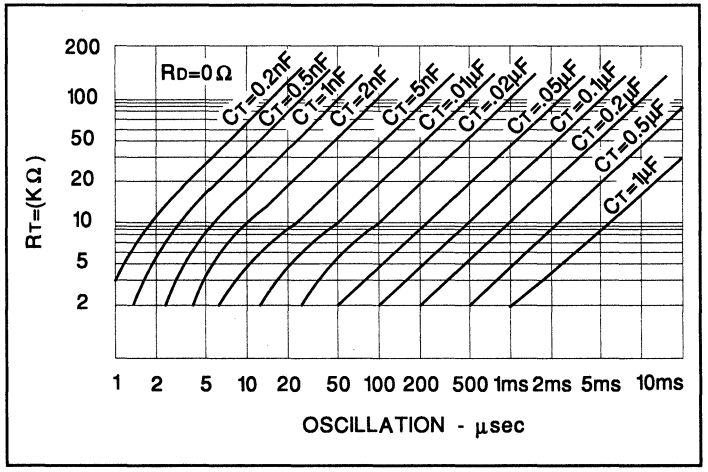


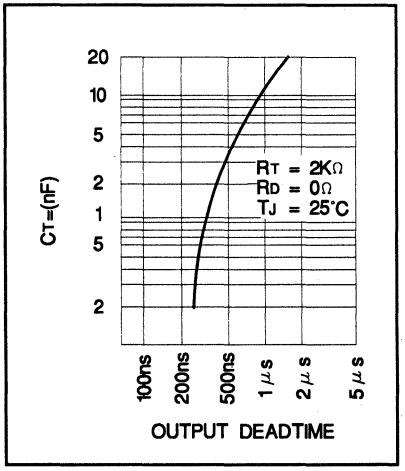
Figure 9. Driving N-Channel Power MOSFETs

TYPICAL CHARACTERISTICS

OSCILLATOR PERIOD vs RT and CT

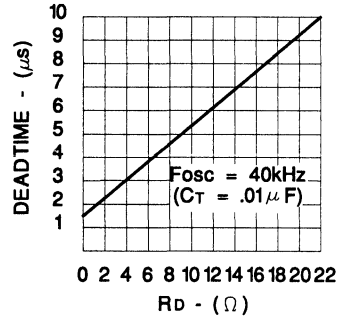


OUTPUT BLANKING

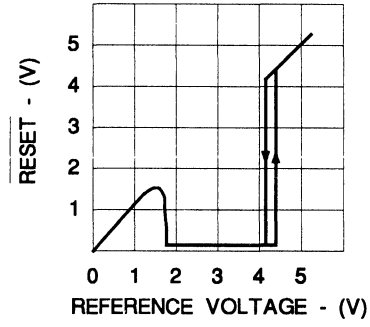


TYPICAL CHARACTERISTICS (Cont.)

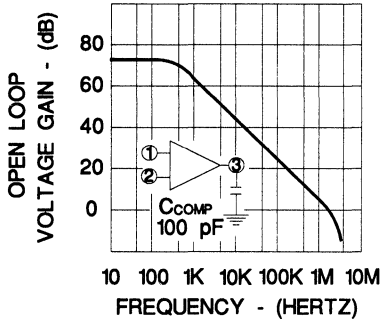
Output Driver Deadtime vs. RD Value



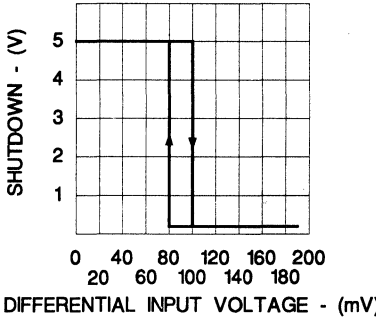
Under Voltage Lockout Characteristic



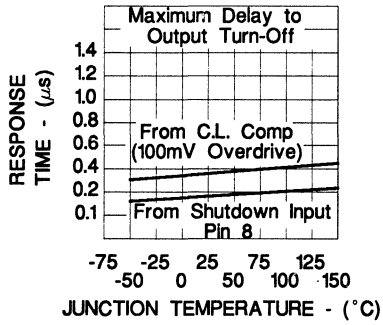
Error Amplifier Open Loop Gain vs. Frequency



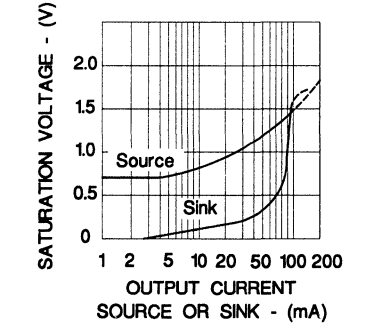
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



5

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INTEGRATED CIRCUITS
UNITRODE

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

Power Supply Supervisory Circuit

FEATURES

- Includes Over-voltage, Under-voltage, And Current Sensing Circuits
- Internal 1% Accurate Reference
- Programmable Time Delays
- SCR "Crowbar" Drive Of 300mA
- Remote Activation Capability
- Optional Over-voltage Latch
- Uncommitted Comparator Inputs For Low Voltage Sensing (UC1544 Series Only)

DESCRIPTION

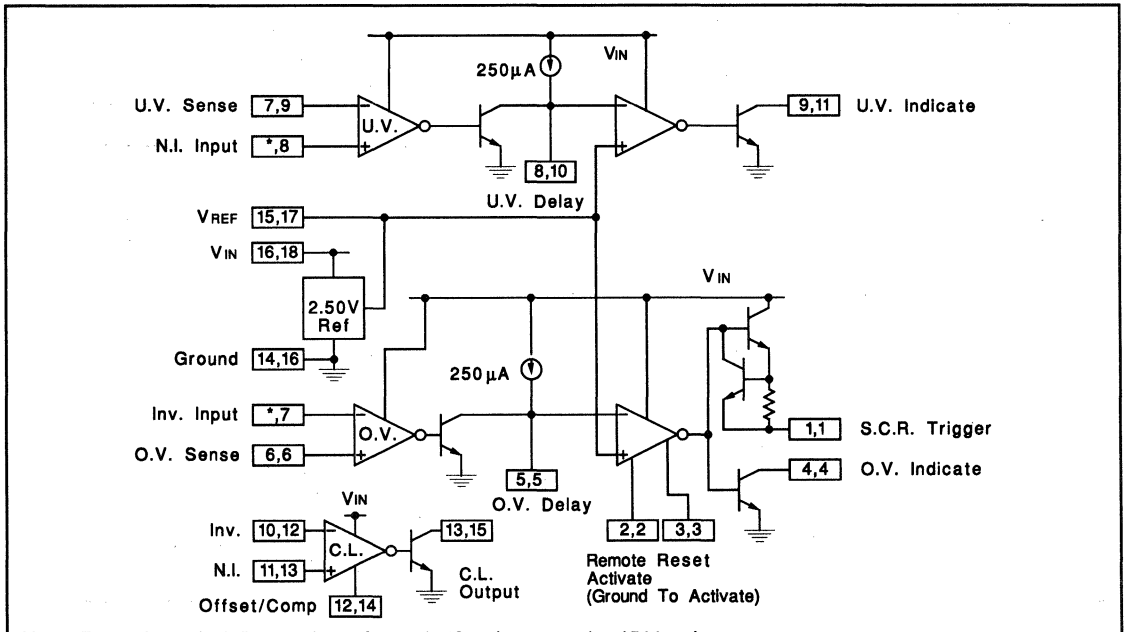
The monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2455/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage. The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

BLOCK DIAGRAM



Note: For each terminal, first number refers to 1543 series, second to 1544 series.
** On 1543 series, this function is internally connected to VREF.*

6/93

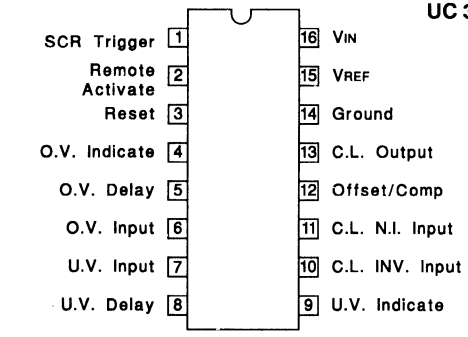
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN} 40V
Sense Inputs, Voltage Range . . . . . 0 to V_{IN}
SCR Trigger Current (Note 1) . . . . . -600mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Power Dissipation (Package Limitation) 1000mW
Operating Temperature Range
UC1543, UC1544 . . . . . -55°C to +125°C
UC2543, UC2544 . . . . . -25°C to +85°C
UC3543, UC3544 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C

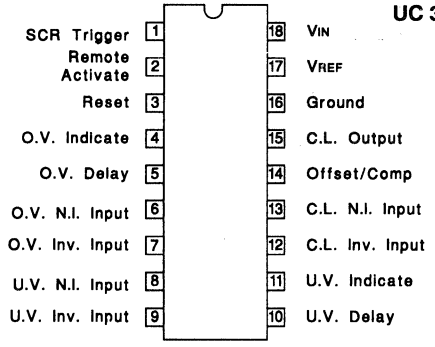
Note 1: At higher input voltages, a dissipation limiting resistor, RG, is required.
Note 2: Currents are positive-into, negative-out of the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

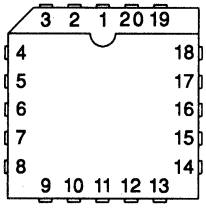
DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package
UC 1543
UC 2543
UC 3542



DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package
UC 1544
UC 2544
UC 3544

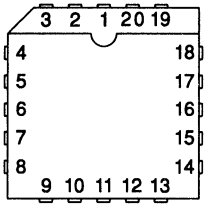


PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. Input	8
N/C	9
N/C	10
U.V. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
VREF	19
VIN	20

PLCC-20, LCC-20
(TOP VIEW)
Q or L Package

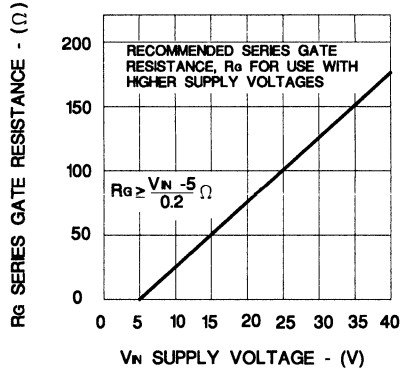


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. N.I. Input	8
O.V. INV. Input	9
U.V. N.I. Input	10
U.V. INV. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
VREF	19
VIN	20

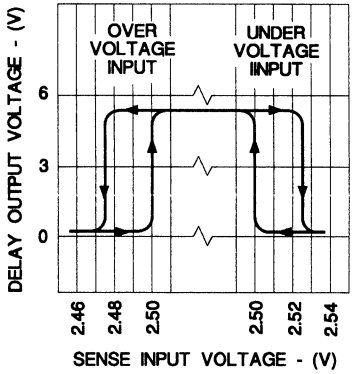
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1543 and UC1544; -25°C to +85°C for the UC2543 and UC2544; and 0°C to +70°C for the UC3543 and UC3544; and for V_{IN} = 5 to 35V. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1543/UC1544 UC2543/UC2544			UC3543/UC3544			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Output Open, T_J = 25°C		7	10		7	10	mA
	$T_{MIN} \le T_J \le T_{MAX}$			15			15	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	-12	-20	-40	-12	-20	-40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	-100	-300	-600	-100	-300	-600	mA
Peak Output Voltage	V_{IN} = 15V, I_O = -100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Reset Voltage	Reset open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from R/A	R_L = 50Ω, T_J = 25°C, C_D = 0		300			300		ns
Prop. Delay from O/V input	R_L = 50Ω, T_J = 25°C, C_D = 0		500			500		ns
Comparator Section								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		-0.3	-1.0		-0.3	-1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_O = 0	-200	-250	-300	-200	-250	-300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Propagation Delay	Input Over Drive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Over Drive = 200mV, T_J = 25°C, C_D = 1µF		10			10		ms
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		-0.3	-1.0		-0.3	-1.0	µA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVOL	Offset Pin Open, V_{CM} = 0V, R_L = 10k to 15kΩ, ΔV_{OUT} = 1 to 6V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

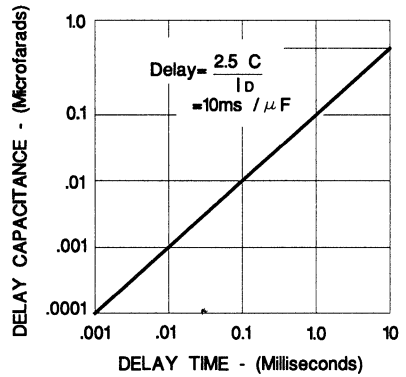
SCR Trigger Power Limiting



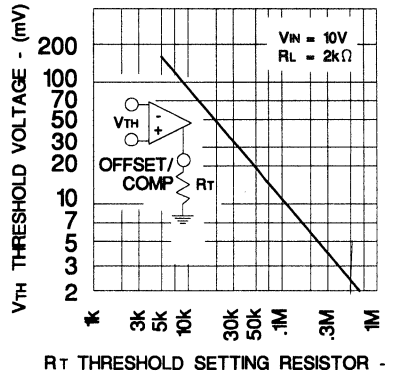
Comparator Input Hysteresis



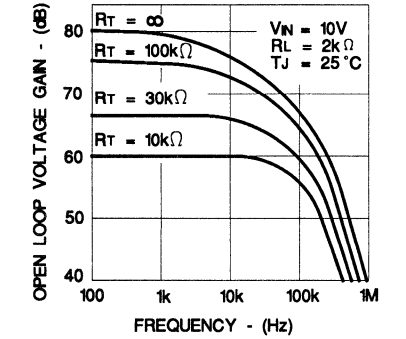
Activation Delay vs Capacitor Value



Current Limit Input Threshold

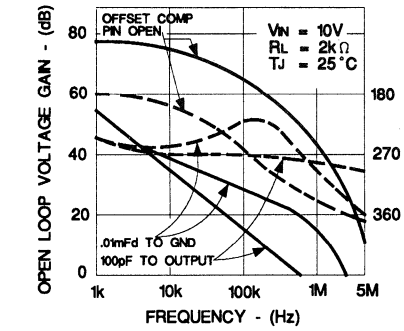


Current Limit Amplifier Gain



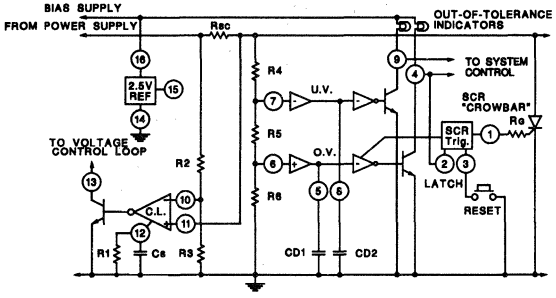
Note: RT is connected from Offset Pin to Gnd. Values of RT below 5.0k may cause Amplifier Cutoff at -55°C.

Current Limit Amplifier Frequency Response



APPLICATIONS (Pin numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} = \frac{1000}{R_1}$

CS is determined by the current loop dynamics

Peak current to load, $I_P \cong \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2 + R_3}\right)$

Short Circuit Current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

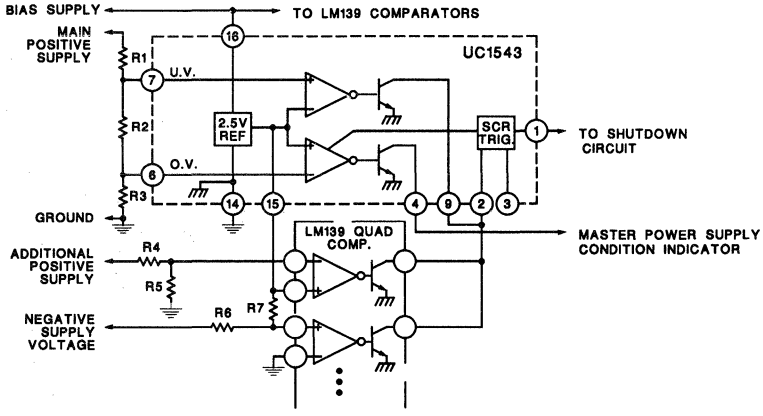
Low output voltage limit, $V_O\ (Low) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit, $V_O\ (High) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_6}$

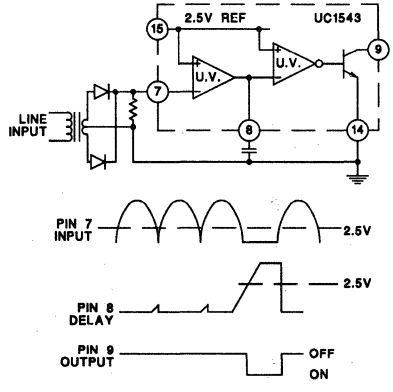
Voltage sensing delay, $t_D = 10{,}000C_D$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

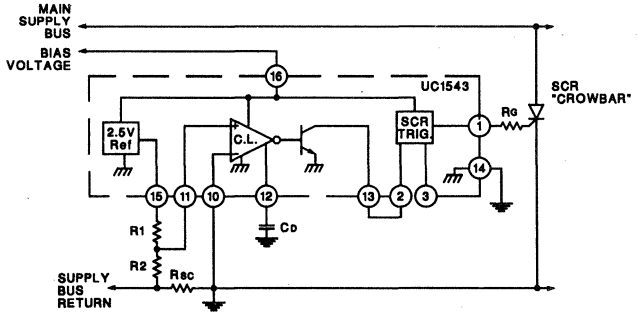
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



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Simple 1 Amp Step-Down Fixed Voltage Regulators

PRELIMINARY

FEATURES

- 5V, 12V and 15V Output, ±3% Max Over Line and Load Conditions
- Guaranteed 1A Output Current
- Wide Input Voltage Range From V_{OUT}+2V to 40V (60V for HV)
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- Low Power Standby Mode, I_Q Typically < 200 µA
- Efficiency Typically Over 80%
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- 100% Electrical Thermal Limit Burn-in
- Replacement for LM2575 Series

APPLICATIONS

- Simple High-Efficiency Step-Down (buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Inverting, Buck-Boost)
- Isolated Flyback Converter using Minimum Number of External Components
- Negative Boost Converter

DESCRIPTION

The UC1575/UC2575 family of devices provides all the active functions necessary to implement a simple step-down (buck) switching regulator. Utilizing a minimum number of external components, these regulators offer a simple, high efficiency replacement for popular three-terminal adjustable linear regulators, greatly reducing, and in many cases eliminating, the need for a heat sink.

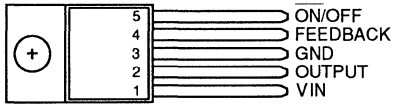
The UC1575/UC2575 series features an output voltage of 5V, 12V or 15V (see Table 1) and is capable of driving a 1A load while maintaining excellent line and load regulation. Other features include internal frequency compensation, an on-chip fixed frequency oscillator with a ±3% tolerance, and output voltage with ±2% tolerance within specified input voltages and output load conditions. External shutdown with a standby current of 200µA is provided. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

A standard series of inductors and capacitors are available from several manufacturers optimized for use with the UC1575/UC2575 series. This feature greatly simplifies the design of switched mode power supplies.

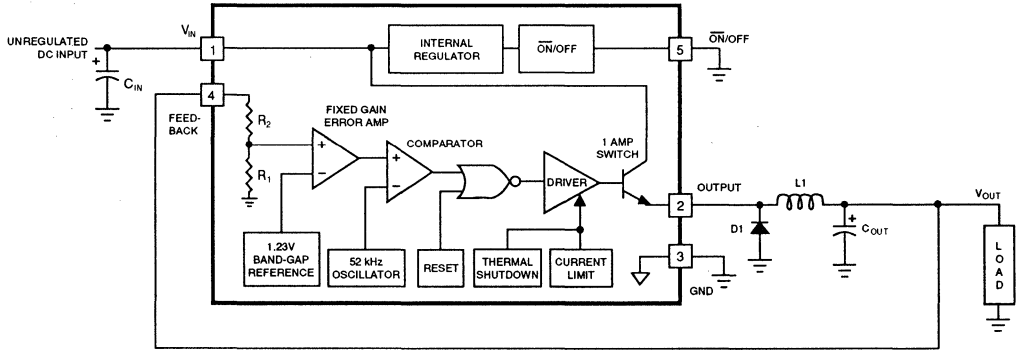
5

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-PACKAGE



BLOCK DIAGRAM



Note: Pin numbers are for the TO-220 package

5/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage
- UC1575/UC2575 ..... 45V
- UC2575HV 63V

ON/OFF Pin Input Voltage ..... -0.3 ≤ V ≤ +40V

Output Voltage to Ground (Steady State) ..... -1V

Power Dissipation ..... Internally Limited

Storage Temperature Range ..... -65°C to +150°C

Minimum ESD Rating
- (C = 100 pF, R = 1.5 kΩ) ..... 2 kV
- FB Pin (Pin 4) ..... 1 kV

Lead Temperature
- (Soldering, 10 sec.) ..... 260°C

OPERATING RATINGS

Maximum Junction Temperature ..... 150°C

Temperature Range
- UC1575 ..... -55°C ≤ T_J ≤ +150°C
- UC2575/UC2575HV ..... -40°C ≤ T_J ≤ +125°C

Supply Voltage
- UC1575/UC2575 ..... 40V
- UC2575HV 60V

Order Number For:		Output Voltage	Temperature Range
Standard Voltage Rating (40V)	High Voltage Rating (60V)		
UC2575T-5.0	UC2575HVT-5.0	5.0	-40°C≤TJ≤+125°C
UC2575T-12	UC2575HVT-12	12.0	
UC2575T-15	UC2575HVT-15	15.0	
UC1575K-5.0		5.0	-55°C≤TJ≤+150°C
UC1575K-12		12.0	
UC1575K-15		15.0	

TABLE 1

TEST CIRCUIT AND LAYOUT GUIDELINES *(Figure 1)*

C_{IN} ..... 100 µF, 75V Aluminum Electrolytic
C_{OUT} ..... 330 µF, 15V Aluminum Electrolytic
220 µF, 15V Aluminum Electrolytic for UC2575-5
D1 ..... Schottky, MBR360
L1 ..... 330 µH (PE-52627) for UC2575-5
470µH (AIE-430-0634) for UC2575-12
680µH (AIE-415-0935) for UC2575-15
5-Pin TO-220 Socket ..... 2936 (Loranger Mfg. Co.)
4-Pin TO-3 Socket ..... 8112-AG7 (Augat Inc.)

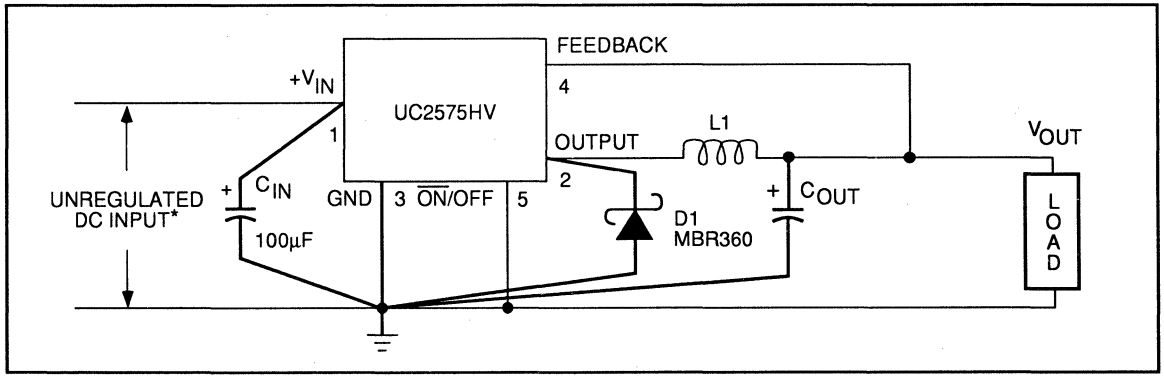


FIGURE 1

Note: *Pin numbers are for the TO-220 package*

** 7-40V (60HV) for-5, 15-35V (60HV) for-12, 17-40V (60HV) for-15*

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1575-12 and -40°C to +125°C for the UC2575-12/UC2575HV-12, T_A =T_J). Unless otherwise specified, V_{IN} = 25V, and I_{LOAD} = 200mA.

		UC1575-12			UC2575-12 UC2575HV-12			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Output Voltage	V_{IN} = 25V, I_{LOAD} = 0.2A Circuit of *Figure1*, T_J = 25°C	11.88	12.0	12.12	11.76	12.0	12.24	V
Output Voltage UC1575/UC2575	0.2A ≤ I_{LOAD} ≤ 1A,15V ≤ V_{IN} ≤ 40V Circuit of *Figure 1* T_J = 25°C	11.52 11.64	12.0	12.48 12.36	11.40 11.52	12.0	12.60 12.48	V
Output Voltage UC2575HV	0.2A ≤ I_{LOAD} ≤ 1A, 15V ≤ V_{IN} ≤ 60V Circuit of *Figure 1* T_J = 25°C				11.40 11.52	12.0	12.65 12.52	V
Efficiency	V_{IN} = 15V, I_{LOAD} = 1A, V_{OUT} = 12V		88			88		%
DEVICE PARAMETERS								
Oscillator Frequency	(Note 9) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 1A (Note 3) T_J = 25°		0.9	1.4 1.2		0.9	1.4 1.2	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	1.3 1.7	2.2	3.2 3.0	1.3 1.7	2.2	3.2 3.0	A
Output Leakage Current	V_{IN} = 40V, T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 6) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 6) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

5

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1575-15 and -40°C to +125°C for the UC2575-15/UC2575-15HV, T_A=T_J). Unless otherwise specified, V_{IN} = 30V, and I_{LOAD} = 200mA.

		UC1575-15			UC2575-15 UC2575HV-15			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Output Voltage	V_{IN} = 30V, I_{LOAD} = 0.2A Circuit of *Figure1*, T_J = 25°C	14.85	15.0	15.15	14.70	15.0	15.30	V
Output Voltage UC1575/UC2575	0.2A ≤ I_{LOAD} ≤ 1A,18V ≤ V_{IN} ≤ 40V Circuit of *Figure 1* T_J = 25°C	14.40 14.55	15.0	15.60 15.45	14.25 14.40	15.0	15.75 15.60	V
Output Voltage UC2575HV	0.2A ≤ I_{LOAD} ≤ 1A, 18V ≤ V_{IN} ≤ 60V Circuit of *Figure 1* T_J = 25°C				14.25 14.40	15.0	15.83 15.68	V
Efficiency	V_{IN} = 18V, I_{LOAD} = 1A, V_{OUT} = 15V		88			88		%
DEVICE PARAMETERS								
Oscillator Frequency	(Note 9) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 1A (Note 3) T_J = 25°		0.9	1.4 1.2		0.9	1.4 1.2	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	1.3 1.7	2.2	3.2 3.0	1.3 1.7	2.2	3.2 3.0	A
Output Leakage Current	V_{IN} = 40V,T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 6) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 6) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

Note 2: *External components such as the catch diode. Inductor, input and output capacitors can affect switching regulator system performance. When the UC1575/UC2575 Is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics*

Note 3: *Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.*

Note 4: *Feedback (pin 4) removed from output and connected to 0V.*

Note 5: *Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.*

Note 6: *Feedback (pin 4) removed from output and connected to 25V to force the output transistor OFF.*

Note 7: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/2 inch leads in a socket, or on a PC board with minimum copper area.*

Note 8: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/4 inch leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.*

Note 9: *The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which pulls the output lower than 3V for UC2575-5.0, or lower than 7.2V for UC2575-12 and lower than 9V for UC2575-15. This self protection features lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.*

Note 10: *Refer to RETS UC1575K For current revision of military RETS/SMD.*

Typical Performance Characteristics *(Circuit of Figure 1)*

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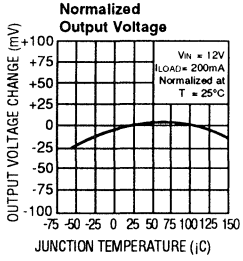
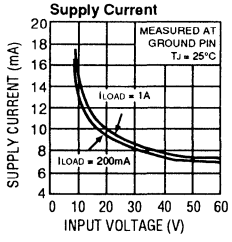
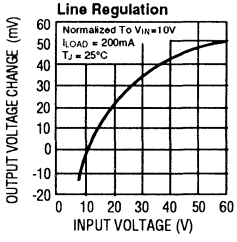
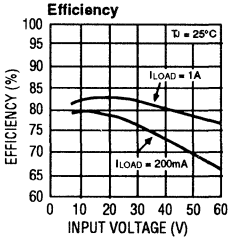
UC1575-5.0/UC2575-5.0

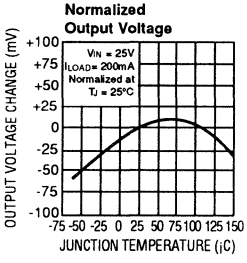


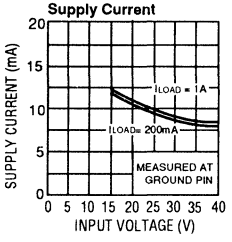


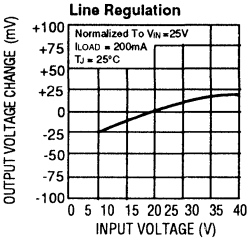


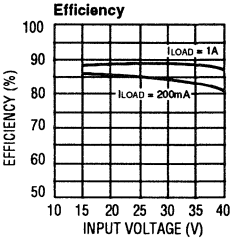


UC1575-12/UC2575-12

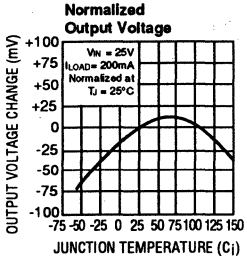


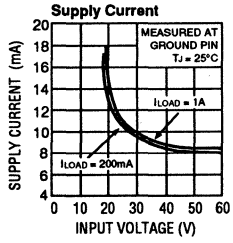


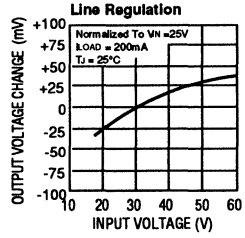


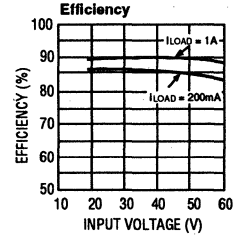


UC1575-15/UC2575-15

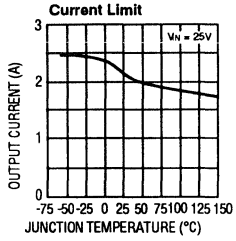


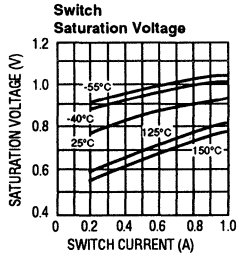


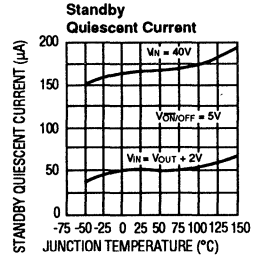




Other Characteristics:







UNITRODE INTEGRATED CIRCUITS
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UC1575-ADJ
UC2575-ADJ
UC2575HV-ADJ

Simple 1 Amp Step-Down Voltage Regulator

PRELIMINARY

FEATURES

- Adjustable Output
- Reference Voltage ±2% Max Over Line and Load Conditions
- Guaranteed 1A Output Current
- Wide Input Voltage Range, 4V to 40V (60V for HV)
- Wide Output Voltage Range, 1.23V to 37V (57V for HV)
- Requires Only 6 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- Low Power Standby Mode, I_Q Typically < 200 µA
- Efficiency Typically Over 80%
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- 100% Electrical Thermal Limit Burn-in
- Replacement for LM2575 Series

APPLICATIONS

- Simple High-Efficiency Step-Down (buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-card Switching Regulators
- Positive to Negative Converter (Inverting, Buck-Boost)
- Isolated Flyback Converter Using Minimum Number of External Components
- Negative Boost Converter

DESCRIPTION

The UC1575-ADJ family of devices provides all the active functions necessary to implement a simple step-down (buck) switching regulator. Utilizing a minimum number of external components, these regulators offer a simple, high efficiency replacement for popular three-terminal adjustable linear regulators, greatly reducing, and in many cases eliminating the need for a heat sink.

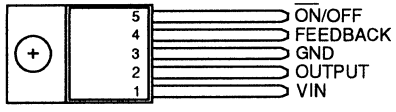
The UC1575-ADJ series features an output voltage which is adjustable from 1.23V to 37V (57V for the HV version) and is capable of driving a 1A load while maintaining excellent line and load regulation. Other features include internal frequency compensation, an on-chip fixed frequency oscillator with a ±10% tolerance, and output voltage with ±2% tolerance within specified input voltages and output load conditions. External shutdown with a standby current of 200µA is provided. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

A standard series of inductors and capacitors are available from several manufacturers optimized for use with the UC1575-ADJ series. This feature greatly simplifies the design of switched mode power supplies.

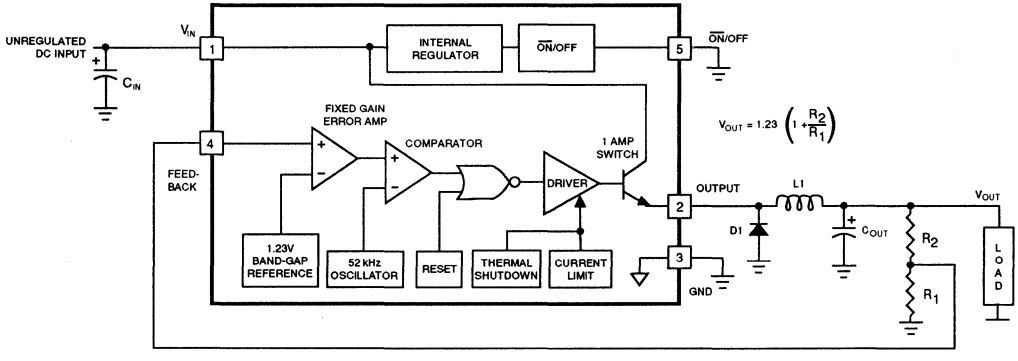
5

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-PACKAGE



BLOCK DIAGRAM



Note: Pin numbers are for the TO-220 package

5/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage
- UC1575/UC2575 ..... 45V
- UC2575HV 63V

ON/OFF Pin Input Voltage ..... $-0.3 \le V \le +40V$

Output Voltage to Ground (Steady State) ..... -1V

Power Dissipation ..... Internally Limited

Storage Temperature Range ..... -65°C to +150°C

Minimum ESD Rating
- (C = 100 pF, R = 1.5 kΩ) ..... 2 kV
- FB Pin (Pin 4) ..... 1 kV

Lead Temperature
- (Soldering, 10 sec.) ..... 260°C

OPERATING RATINGS

Maximum Junction Temperature ..... 150°C

Temperature Range
- UC1575 ..... $-55°C \le TJ \le +150°C$
- UC2575/UC2575HV ..... $-40°C \le TJ \le +125°C$

Supply Voltage
- UC1575/UC2575 ..... 40V
- UC2575HV 60V

TEST CIRCUIT AND LAYOUT GUIDELINES *(Figure 1)*

C_{IN} ..... 100 µF, 75V Aluminum Electrolytic
C_{OUT} ..... 470 µF, 15V Aluminum Electrolytic
D1 ..... Schottky, MBR360
L1 ..... 330 µH, 415-0926 (AIE)
R1 ..... 1k, 0.1%, R2 = 3.065k, 0.1%
5-Pin TO-220 Socket ..... 2936 (Loranger Mfg. Co.)
4-Pin TO-3 Socket ..... 8112-AG7 (Augat Inc.)

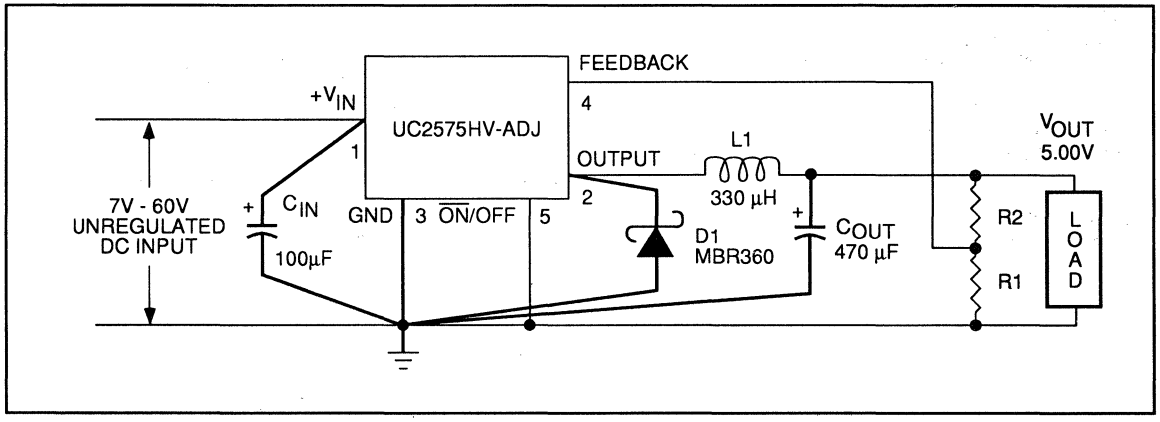


FIGURE 1

Note: *Pin numbers are for the TO-220 package*

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1575 and -40°C to +125°C for the UC2575/UC2575HV, T_A=T_J). Unless otherwise specified, V_{IN} = 12V and I_{LOAD} = 200 mA.

		UC1575-ADJ			UC2575-ADJ UC2575HV-ADJ			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Feedback Voltage	V_{IN}= 12V, I_{LOAD} = 0.2A V_{OUT} = 5V, T_J = 25°C Circuit of *Figure*1	1.217	1.230	1.243	1.217	1.230	1.243	V
Feedback Voltage UC1575/UC2575	0.2A ≤ I_{LOAD} ≤ 1A, 8V ≤ V_{IN} ≤ 40V V_{OUT} = 5V, Circuit of *Figure 1* T_J = 25°C	1.193 1.205	1.230	1.267 1.255	1.180 1.193	1.230	1.280 1.267	V
Feedback Voltage UC2575HV	0.2A ≤ I_{LOAD} ≤ 1A, 8V ≤ V_{IN} ≤ 60V V_{OUT} = 5V, Circuit of *Figure 1* T_J = 25°C				1.180 1.193	1.230	1.286 1.273	V
Efficiency	V_{IN} = 12V, I_{LOAD} = 1A, V_{OUT} = 5V		82			82		%
DEVICE PARAMETERS								
Feedback Bias Current	V_{OUT} = 5V T_J = 25°C		50	500 100		50	500 100	nA
Oscillator Frequency	(Note 8) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 1A (Note 3) T_J = 25°		0.9	1.4 1.2		0.9	1.4 1.2	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	1.3 1.7	2.2	3.2 3.0	1.3 1.7	2.2	3.2 3.0	A
Output Leakage Current	V_{IN} = 40V, T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 5) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 5) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 6) T Package, Junction to Ambient (Note 7) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

Note 2: *External components such as the catch diode. Inductor, input and output capacitors can affect switching regulator system performance. When the UC1575/UC2575 Is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.*

Note 3: *Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.*

Note 4: *Feedback (pin 4) removed from output and connected to 0V.*

Note 5: *Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.*

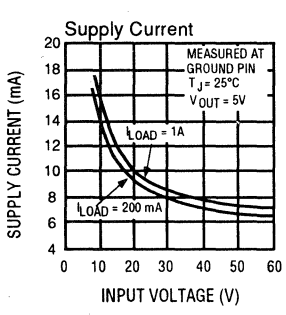
Note 6: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/2 inch leads in a socket, or on a PC board with minimum copper area.*

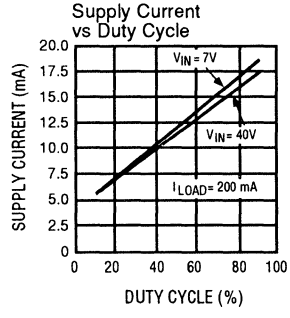
Note 7: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/4 inch leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.*

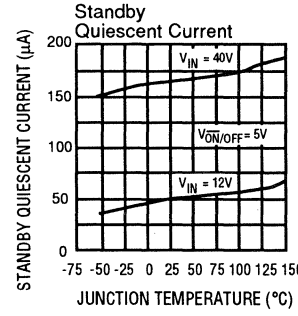
Note 8: *The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which pulls the feedback voltage lower than .7V. This self protection feature lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.*

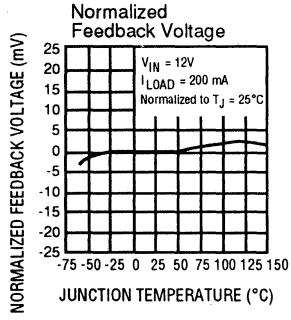
Note 9: *Refer to RETS UC1575K-ADJ For current revision of military RETS/SMD.*

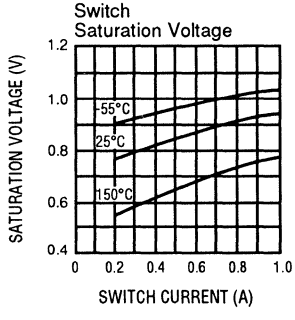
Typical Performance Characteristics *(Circuit of Figure 1)*

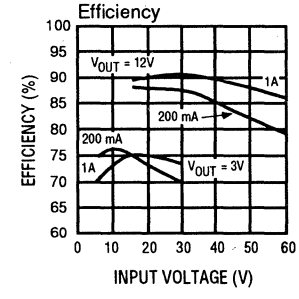












UC1575 Series Buck Regulator Design Procedure

PROCEDURE

Given:

V_{OUT} = Regulated Output Voltage
V_{IN} (max) = Minimum Input Voltage
I_{LOAD} (max) = Maximum Load Current
F = Switching Frequency (52kHz)

Example: V_{OUT} = 10V, V_{IN} (max) = 25V, I_{LOAD} (max) = 1A, F = 52kHz.

1. Programming Output Voltage (Selecting R1 and R2)

The following formula can be used to select the resistor values for a given voltage:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right)$$

And for a given R1 (between 1K and 10K),

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Example:

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right) \text{ select R1 = 1K:}$$

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{10V}{1.23V} - 1\right) = 7.13K, \text{ use closest 1\% value 7.15K.}$$

2. Inductor Selection (L1)

A. Calculate E•T(V•μS), from the following formula:

$$E \cdot T = (V_{IN} - V_{OUT}) \cdot \frac{V_{OUT}}{V_{IN}} \cdot \frac{1000}{F(\text{in kHz})} \quad (V \cdot \mu S)$$

B. Use the E•T value from above and match it with the E•T number on the vertical axis of the Inductor value selection guide shown in Figure 2.

C. On the horizontal axis, select the minimum load current. Find the region intersected by the E•T value and the maximum load current value and note the inductor code for the region.

D. Match the inductor code to the inductor value, using Fig. 3.

Example:

Calculating E•T (V•μS):

$$E \cdot T = (25 - 10) \cdot \frac{10}{25} \cdot \frac{1000}{52} = 115 \text{ V} \cdot \mu S$$

For I_{LOAD} = 1A and E•T = 115V•μS, Inductor code is H470 and the inductor value is 470μH.

3. Output Capacitor Selection (C_{OUT})

A. The dominant pole-pair of the switching regulator loop is defined by the value of the output capacitor and the inductor. In order to achieve stable operation the capacitor must satisfy the following requirement.

$$C_{OUT} > 7{,}785 \cdot \frac{V_{IN}\,(max)}{V_{OUT} \cdot L(\mu H)} \quad (\mu F)$$

Example:

$$C_{OUT} > 7{,}785 \cdot \frac{25}{10 \cdot 150} = 130\mu F$$

For acceptable ripple voltage, select C_{OUT} = 220μF electrolytic capacitor.

The ESR (Equivalent Series Resistance) of the output capacitor is the primary cause of the output ripple voltage and the value and the type of the output capacitor determine the amount of ESR and thus the output ripple voltage. In general lower capacitor values have higher ESR ratings.

Capacitor values larger than 680µF will produce an output ripple voltage of 35mV to 50mV, while smaller capacitors (220µF to 680µF) will typicaly cause a ripple of 50mV to 150mV. The following approximate relationship could be used in determining the output ripple:

$$V_{RIPPLE}\ p\text{-}p > 0.3 \times I_{LOAD}(max) \times ESR$$

It is possible to reduce the output ripple to 10mV-20mV by using several standard electrolytic capacitors in parallel or by using higher grade capacitors with low ESR and low inductance. However, ESR values lower than 0.05 Ohms can cause instability. The capacitor's ripple current rating at 52kHz should be at least 50% higher than the inductor current ripple:

$$I_{RIPPLE}(max) > 1.5 \times 0.3 \times I_{LOAD}(max)$$

B. The voltage rating of the output capacitor should be at least 1.2 times greater that the output voltage. For a 10V output, a rating of 15V is appropriate, and a 20V rating is recommended.

4. Catch Diode Selection (D1)

The current rating of the catch diode must be at least 1.2 times greater than the maximum load current, unless the diode is expected to withstand a continuous output short, in which case the current rating of the diode should be equal to the maximum current rating of UC2575.

A. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

B. Schottky diodes with fast switching speed and a low forward voltage drop are the most efficient. Some types of diodes with an abrupt turn-off characteristic may cause instability and EMI problems. Therefore in general, a fast-recovery diode with soft recovery characteristics is recommended.

See Figure 4 for Schottky and "soft" fast-recovery diode selection guide.

5. Input Capacitor (CIN)

To assure stability, the regulator input pin must be bypassed with a by-pass capacitor of at least 47µF, low ESR (electrolytic type). If an operation at low temperatures (for example -25°C) is intended, then addition of a ceramic or solid tantalum capacitor near the input pin may be required to maintain the capacitance value and low ESR at low temperature.

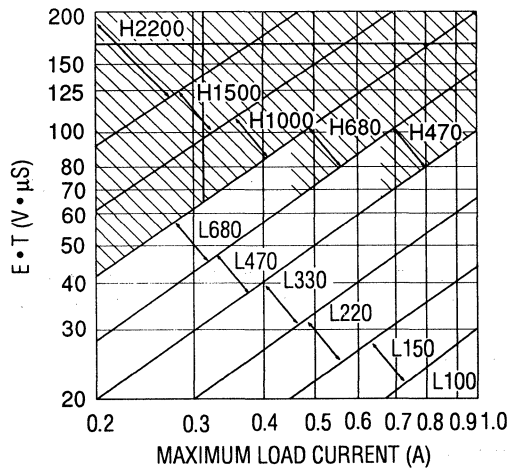


Figure 2. Inductor Value Selection Guide (for Continuous Mode Operation)

Inductor Code	Inductor Value	AIE (Note 1)	Pulse Eng. (Note 2)	Renco (Note 3)
L47	47 µH	415-0932	PE-53112	RL2442
L68	68 µH	415-0931	PE-92114	RL2443
L100	100 µH	415-0926	PE-52627	RL1952
L150	150 µH	415-0953	PE-53113	RL1954
L220	220 µH	415-0922	PE-52626	RL1953
L330	330 µH	415-0926	PE-52627	RL1952
L470	470 µH	415-0927	PE-53114	RL1951
L680	680 µH	415-0928	PE-52629	RL1950
H150	150 µH	415-0936	PE-53115	RL2445
H220	220 µH	430-0636	PE-53116	RL2446
H330	330 µH	430-0635	PE-53117	RL2447
H470	470 µH	430-0634	PE-53118	RL1961
H680	680 µH	415-0935	PE-53119	RL1960
H1000	1000 µH	415-0934	PE-53120	RL1959
H1500	1500 µH	415-0933	PE-53121	RL1958
H2200	2200 µH	415-0945	PE-53122	RL2448

Note 1: *AIE Magnetics, Div. Vernitron Corp. Passive Components Group, (813) 347-2181 2801 72nd Street North, St. Petersburg, FL 33710*

Note 2: *Pulse Engineering, (619) 268-2400 P.O. Box 12235, San Diego, CA 92112*

Note 3: *Renco Electronics Inc., 60 Jeffnyn Blvd. East, Deer Park, NY 11729 (516) 586-5566*

FIGURE 3. Inductor Selection by Manufacturer's Part Number

V_{IN} (max)	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P SR102	1N5820 MBR320P SR302	The following diodes are all rated to 100V 11DF1 MUR110 HER102	The following diodes are all rated to 100V 31DF1 MUR310 HER302
30V	1N5818 MBR130P 11DQ03 SR103	1N5821 MBR330 31DQ03 SR303		
40V	1N5819 MBR140P 11DQ04 SR104	1N5822 MBR340 31DQ04 SR304		
50V	MBR150 11DQ05 SR105	MBR350 31DQ05 SR305		
60V	MBR1601 11DQ06 SR106	MBR3603 31DQ06 SR306		

Figure 4. Diode Selection Chart

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Simple 3 Amp Step-Down Fixed Voltage Regulators

PRELIMINARY

FEATURES

- 5V, 12V and 15V Output, ±3% Max Over Line and Load Conditions
- Guaranteed 3A Output Current
- Wide Input Voltage Range, from V_{OUT}+2V to 40V (60V for HV)
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- Low Power Standby Mode, I_Q Typically < 200 µA
- Efficiency Typically Over 80%
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- 100% Electrical Thermal Limit Burn-in
- Replacement for LM2576 Series

APPLICATIONS

- Simple High-Efficiency Step-Down (buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Inverting, Buck-Boost)
- Isolated Flyback Converter using Minimum Number of External Components
- Negative Boost Converter

DESCRIPTION

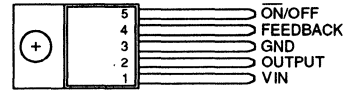
The UC1576/UC2576 family of devices provides all the active functions necessary to implement a simple step-down (buck) switching regulator. Utilizing a minimum number of external components, these regulators offer a simple, high efficiency replacement for popular three-terminal adjustable linear regulators, greatly reducing, and in many cases eliminating, the need for a heat sink.

The UC1576/UC2576 series features an output voltage of 5V, 12V or 15V (see Table 1) and is capable of driving a 3A load while maintaining excellent line and load regulation. Other features include internal frequency compensation, an on-chip fixed frequency oscillator with a ±10% tolerance and feedback voltage with ±3% tolerance within specified input voltages and output load conditions. External shutdown with a standby current of 200µA is provided. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

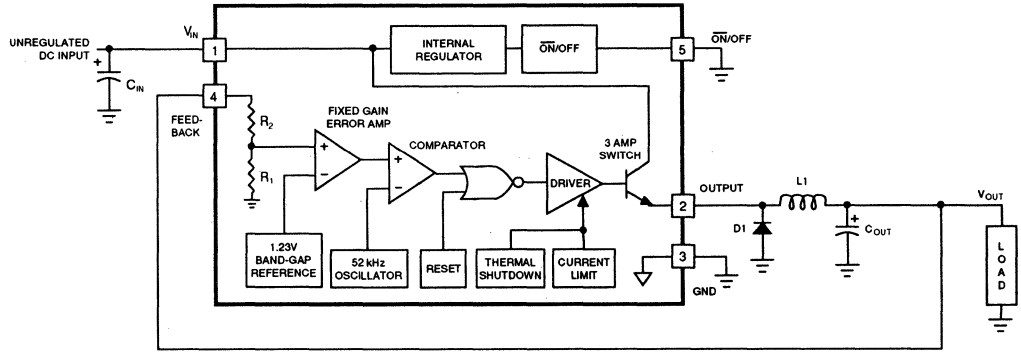
A standard series of inductors and capacitors are available from several manufacturers optimized for use with the UC1576/UC2576 series. This feature greatly simplifies the design of switched mode power supplies.

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-PACKAGE



BLOCK DIAGRAM



Note: Pin numbers are for the TO-220 package

5/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage
- UC1576/UC2576 ..... 45V
- UC2576HV 63V

ON/OFF Pin Input Voltage ..... -0.3 ≤ V ≤ +40V

Output Voltage to Ground (Steady State) ..... -1V

Power Dissipation ..... Internally Limited

Storage Temperature Range ..... -65°C to +150°C

Minimum ESD Rating
- (C = 100 pF, R = 1.5 kΩ) ..... 2 kV
- FB Pin (Pin 4) ..... 1 kV

Lead Temperature
- (Soldering, 10 sec.) ..... 260°C

OPERATING RATINGS

Maximum Junction Temperature ..... 150°C

Temperature Range
- UC1576 ..... -55°C ≤ TJ ≤ +150°C
- UC2576/UC2576HV ..... -40°C ≤ TJ ≤ +125°C

Supply Voltage
- UC1576/UC2576 ..... 40V
- UC2576HV 60V

TEST CIRCUIT AND LAYOUT GUIDELINES *(Figure 1)*

CIN ..... 100 µF, 75V Aluminum Electrolytic
COUT ..... 1000 µF, 15V Aluminum Electrolytic
D1 ..... Schottky, MBR360
L1 ..... 100 µH (PE-92108) for UC2576-5
220 µH (PE-53116) for UC2576-12, and UC2576-15
5-Pin TO-220 Socket ..... 2936 (Loranger Mfg. Co.)
4-Pin TO-3 Socket ..... 8112-AG7 (Augat Inc.)

Order Number For:		Output Voltage	Temperature Range
Standard Voltage Rating (40V)	High Voltage Rating (60V)		
UC2576T-5.0	UC2576HVT-5.0	5.0	-40°C≤TJ≤+125°C
UC2576T-12	UC2576HVT-12	12.0	
UC2576T-15	UC2576HVT-15	15.0	
UC1576K-5.0		5.0	-55°C≤TJ≤+150°C
UC1576K-12		12.0	
UC1576K-15		15.0	

TABLE 1

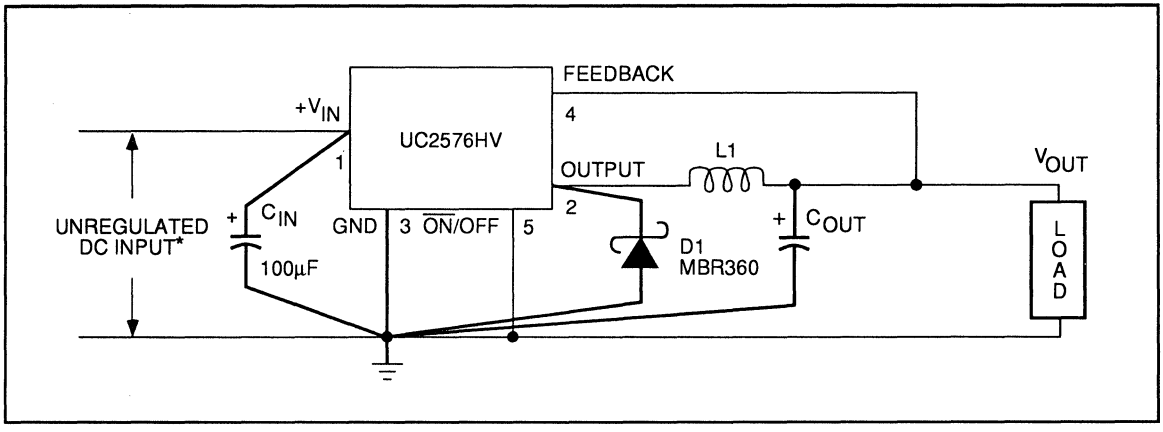


FIGURE 1

Note: *Pin numbers are for the TO-220 package*

** 7-40V (60HV) for-5, 15-35V (60HV) for-12, 17-40V (60HV) for-15*

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1576-5 and -40°C to +125°C for the UC2576-5/UC2576HV-5, T_A=T_J). Unless otherwise specified, V_{IN} = 12V and I_{LOAD} = 500mA.

		UC1576-5			UC2576-5 UC2576HV-5			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Output Voltage	V_{IN} = 12V, I_{LOAD} = 0.5A Circuit of *Figure 1*, T_J = 25°C	4.950	5.0	5.050	4.900	5.0	5.100	V
Output Voltage UC1576/UC2576	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 40V Circuit of *Figure 1* T_J = 25°C	4.800 4.850	5.0	5.200 5.150	4.750 4.800	5.0	5.250 5.200	V
Output Voltage UC2576HV	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 60V Circuit of *Figure 1* T_J = 25°C				4.750 4.800	5.0	5.275 5.225	V
Efficiency	V_{IN} = 12V, I_{LOAD} = 3A, V_{OUT} = 5V		77			77		%
DEVICE PARAMETERS								
Oscillator Frequency	(Note 9) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 3A (Note 3) T_J = 25°		1.4	2.0 1.8		1.4	2.0 1.8	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	3.5 4.2	5.8	7.5 6.9	3.5 4.2	5.8	7.5 6.9	A
Output Leakage Current	V_{IN} = 40V, (T_J = 25°C), Output = 0V V_{IN} = 60V for HV Output = -1V (Note 5) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 5) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V T_J = 25°C	24 2.2	1.5 1.4 	 0.8 1.0	2.4 2.2	1.5 1.4 	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1576-12 and -40°C to +125°C for the UC2576-12/UC2576HV-12, T_A=T_J). Unless otherwise specified, V_{IN} = 25V and I_{LOAD} = 500mA.

		UC1576-12			UC2576-12 UC2576HV-12			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Output Voltage	V_{IN} = 25V, I_{LOAD} = 0.5A Circuit of *Figure 1*, T_J = 25°C	11.88	12.0	12.12	11.76	12.0	12.24	V
Output Voltage UC1576/UC2576	0.5A ≤ I_{LOAD} ≤ 3A,15V ≤ V_{IN} ≤ 40V Circuit of *Figure 1* T_J = 25°C	11.52 11.64	12.0	12.48 12.36	11.40 11.52	12.0	12.60 12.48	V
Output Voltage UC2576HV	0.5A ≤ I_{LOAD} ≤ 3A, 15V ≤ V_{IN} ≤ 60V Circuit of *Figure 1* T_J = 25°C				11.40 11.52	12.0	12.65 12.52	V
Efficiency	V_{IN} = 15V, I_{LOAD} = 3A, V_{OUT} = 12V		88			88		%
DEVICE PARAMETERS								
Oscillator Frequency	(Note 9) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 3A (Note 3) T_J = 25°		1.4	2.0 1.8		1.4	2.0 1.8	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	3.5 4.2	5.8	7.5 6.9	3.5 4.2	5.8	7.5 6.9	A
Output Leakage Current	V_{IN} = 40V, T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 6) Output = -1V		7.5	2 30		7.5	2 30	A
Quiescent Current	(Note 6) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
ON/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 12V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

5

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1576-15 and -40°C to +125°C for the UC2576-15/UC2576HV-15, T_A=T_J). Unless otherwise specified, V_{IN} = 30V and I_{LOAD} = 500mA..

		UC1576-15			UC2576-15 UC2576HV-15			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Output Voltage	V_{IN} = 30V, I_{LOAD} = 0.5A Circuit of *Figure 1*, T_J = 25°C	14.85	15.0	15.15	14.70	15.0	15.30	V
Output Voltage UC1576/UC2576	0.5A ≤ I_{LOAD} ≤ 3A, 18V ≤ V_{IN} ≤ 40V Circuit of *Figure 1* T_J = 25°C	14.40 14.45	15.0	15.60 15.45	14.25 14.40	15.0	15.75 15.60	V
Output Voltage UC2576HV	0.5A ≤ I_{LOAD} ≤ 3A, 18V ≤ V_{IN} ≤ 60V Circuit of *Figure 1* T_J = 25°C				14.25 14.40	15.0	15.83 15.68	V
Efficiency	V_{IN} = 18V, I_{LOAD} = 3A, V_{OUT} = 15V		88			88		%
DEVICE PARAMETERS								
Oscillator Frequency	(Note 9) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 3A (Note 3) T_J = 25°		1.4	2.0 1.8		1.4	2.0 1.8	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	3.5 4.2	5.8	7.5 6.9	3.5 4.2	5.8	7.5 6.9	A
Output Leakage Current	V_{IN} = 40V, T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 6) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 6) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 7) T Package, Junction to Ambient (Note 8) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 12V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

Note 2: *External components such as the catch diode. Inductor, input and output capacitors can affect switching regulator system performance. When the UC1576/UC2576 Is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics*

Note 3: *Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.*

Note 4: *Feedback (pin 4) removed from output and connected to 0V.*

Note 5: *Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.*

Note 6: *Feedback (pin 4) removed from output and connected to 25V to force the output transistor OFF.*

Note 7: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/2 inch leads in a socket, or on a PC board with minimum copper area.*

Note 8: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/4 inch leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.*

Note 9: *The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which pulls the output lower than 3V for UC2576-5.0, or lower than 7.2V for UC2576-12 and lower than 9V for UC2576-15. This self protection features lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.*

Note 10: *Refer to RETS UC1576K For current revision of military RETS/SMD.*

Typical Performance Characteristics *(Circuit of Figure 1)*

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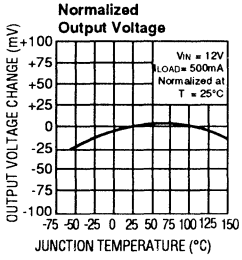
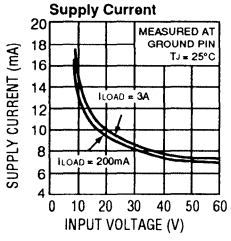
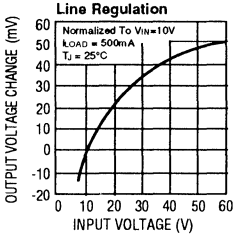
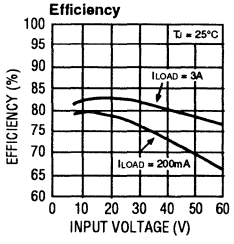
UC1576-5.0/UC2576-5.0

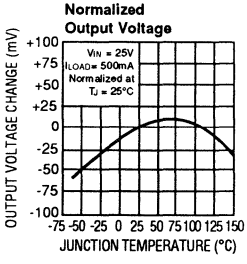


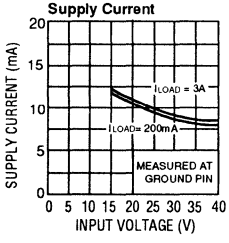


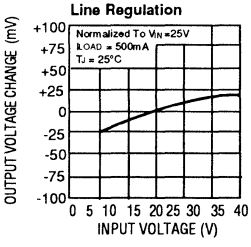


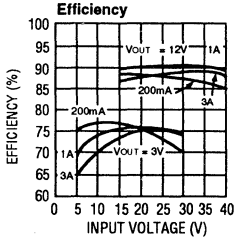


UC1576-12/UC2576-12

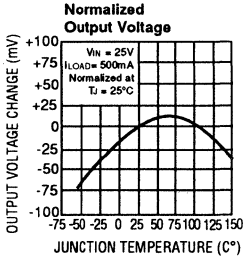


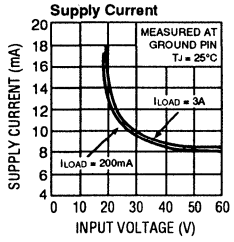


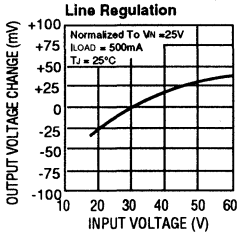


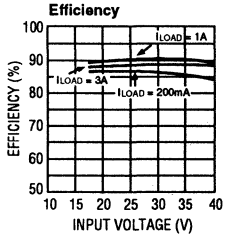


UC1576-15/UC2576-15

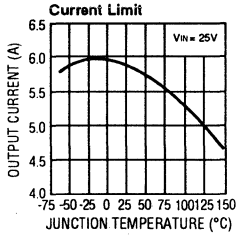


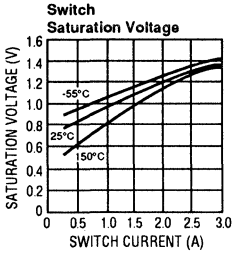


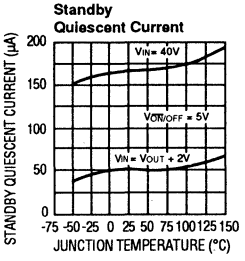




Other Characteristics:







UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

UC1576-ADJ
UC2576-ADJ
UC2576HV-ADJ

Simple 3 Amp Step-Down Voltage Regulator

PRELIMINARY

FEATURES

- Adjustable Output
- Reference Voltage ±2% Max Over Line and Load Conditions
- Guaranteed 3A Output Current
- Wide Input Voltage Range, 4V to 40V (60V for HV)
- Wide Output Voltage Range, 1.23V to 37V (57V for HV)
- Requires Only 6 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- Low Power Standby Mode, I_Q Typically < 200 µA
- Efficiency Typically Over 80%
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- 100% Electrical Thermal Limit Burn-in
- Replacement for LM2576 Series

APPLICATIONS

- Simple High-Efficiency Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Inverting, Buck-Boost)
- Isolated Flyback Converter Using Minimum Number of External Components
- Negative Boost Converter

DESCRIPTION

The UC1576-ADJ family of devices provides all the active functions necessary to implement a simple step-down (buck) switching regulator. Utilizing a minimum number of external components, these regulators offer a simple, high efficiency replacement for popular three-terminal adjustable linear regulators, greatly reducing, and in many cases eliminating, the need for a heat sink.

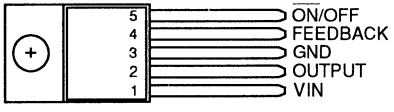
The UC1576-ADJ series features an output voltage which is adjustable from 1.23V to 37V (57V for the HV version) and is capable of driving a 3A load while maintaining excellent line and load regulation. Other features include internal frequency compensation, an on-chip fixed frequency oscillator with a ±10% tolerance, and output voltage with ±2% tolerance within specified input voltages and output load conditions. External shutdown with a standby current of 200µA is provided. The output switch includes cycle-by-cycle current limiting and thermal shutdown for full protection under fault conditions.

A standard series of inductors and capacitors are available from several manufacturers optimized for use with the UC1576-ADJ series. This feature greatly simplifies the design of switched mode power supplies.

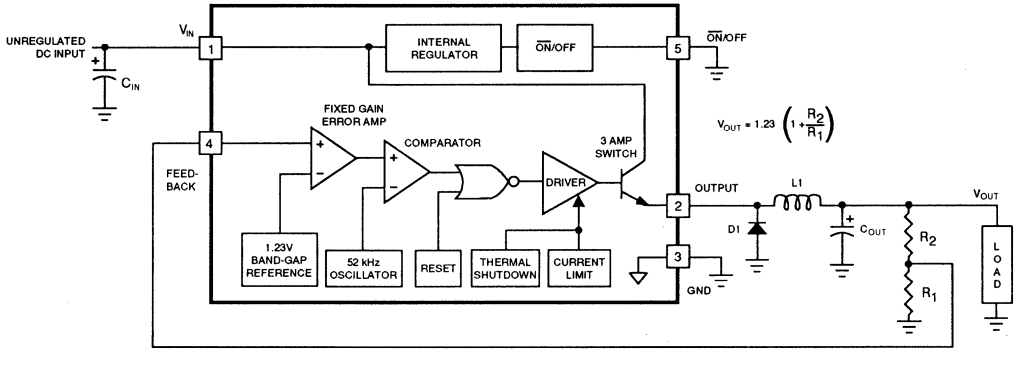
5

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-PACKAGE



BLOCK DIAGRAM



Note: Pin numbers are for the TO-220 package

5/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Maximum Supply Voltage
- UC1576/UC2576 ..... 45V
- UC2576HV 63V

ON/OFF Pin Input Voltage ..... $-0.3 \le V \le +40V$

Output Voltage to Ground (Steady State) ..... -1V

Power Dissipation ..... Internally Limited

Storage Temperature Range ..... -65°C to +150°C

Minimum ESD Rating
- (C = 100 pF, R = 1.5 kΩ) ..... 2 kV
- FB Pin (Pin 4) ..... 1 kV

Lead Temperature
- (Soldering, 10 sec.) ..... 260°C

OPERATING RATINGS

Maximum Junction Temperature ..... 150°C

Temperature Range
- UC1576 ..... $-55°C \le T_J \le +150°C$
- UC2576/UC2576HV ..... $-40°C \le T_J \le +125°C$

Supply Voltage
- UC1576/UC2576 ..... 40V
- UC2576HV 60V

TEST CIRCUIT AND LAYOUT GUIDELINES *(Figure 1)*

C_{IN} ..... 100 µF, 75V Aluminum Electrolytic

C_{OUT} ..... 1000 µF, 15V Aluminum Electrolytic

D1 ..... Schottky, MBR360

L1 ..... 100 µH, Pulse Eng. PE-92108

R1 ..... 1k, 0.1%, R2 = 3.065k, 0.1%

5-Pin TO-220 Socket ..... 2936 (Loranger Mfg. Co.)

4-Pin TO-3 Socket ..... 8112-AG7 (Augat Inc.)

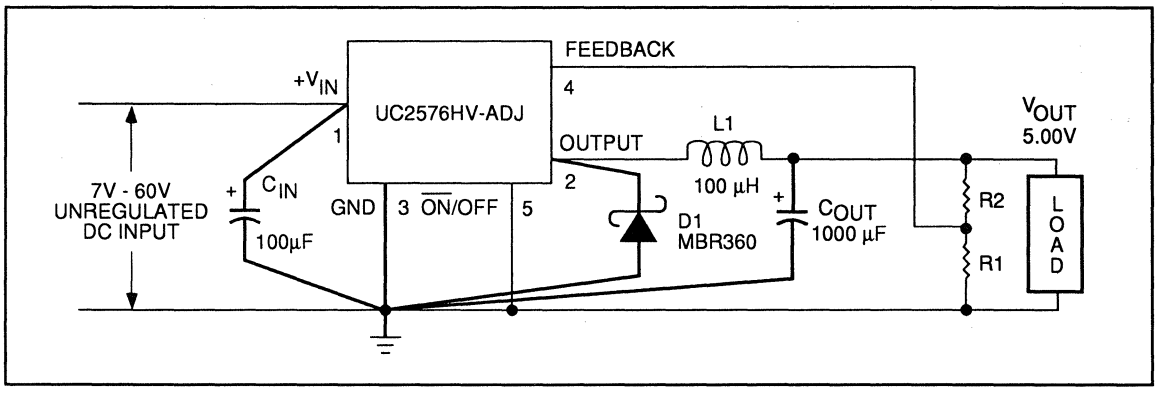


FIGURE 1

Note: Pin numbers are for the TO-220 package

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal stray inductance and ground loops, the length of the leads indicated by heavy lines should be kept as **short** as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results.

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A=-55°C to +150°C for UC1576 and -40°C to +125°C for the UC2576/UC2576HV, T_A=T_J). Unless otherwise specified, V_{IN} = 12V and I_{LOAD} = 500 mA.

		UC1576-ADJ			UC2576-ADJ UC2576HV-ADJ			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS (Note 2) Test Circuit *Figure 1*								
Feedback Voltage	V_{IN} = 12V, I_{LOAD} = 0.5A V_{OUT} = 5V, T_J = 25°C Circuit of *Figure1*	1.217	1.230	1.243	1.217	1.230	1.243	V
Feedback Voltage UC1576/UC2576	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 40V V_{OUT} = 5V, Circuit of *Figure 1* T_J = 25°C	1.193 1.205	1.230	1.267 1.255	1.180 1.193	1.230	1.280 1.267	V
Feedback Voltage UC2576HV	0.5A ≤ I_{LOAD} ≤ 3A, 8V ≤ V_{IN} ≤ 60V V_{OUT} = 5V, Circuit of *Figure 1* T_J = 25°C				1.180 1.193	1.230	1.286 1.273	V
Efficiency	V_{IN} = 12V, I_{LOAD} = 3A, V_{OUT} = 5V		82			82		%
DEVICE PARAMETERS								
Feedback Bias Current	V_{OUT} = 5V T_J = 25°C		50	500 100		50	500 100	nA
Oscillator Frequency	(Note 8) T_J = 25°C	43 47	52	62 58	42 47	52	63 58	KHz
Saturation Voltage	I_{OUT} = 3A (Note 3) T_J = 25°		1.4	2.0 1.8		1.4	2.0 1.8	V
Max Duty Cycle (ON)	(Note 4) T_J = 25°	93	98		93	98		%
Current Limit	Peak Current (Note 3) T_J = 25°C	3.5 4.2	5.8	7.5 6.9	3.5 4.2	5.8	7.5 6.9	A
Output Leakage Current	V_{IN} = 40V, T_J = 25°C, Output = 0V V_{IN} = 60V for HV Output = -1V (Note 5) Output = -1V		7.5	2 30		7.5	2 30	mA
Quiescent Current	(Note 5) T_J = 25°C		5	12 10		5	12 10	mA
Standby Quiescent Current	$\overline{ON}$/OFF Pin = 5V (OFF) T_J = 25°C		50	500 200		50	500 200	µA
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case T Package, Junction to Ambient (Note 6) T Package, Junction to Ambient (Note 7) T Package, Junction to Case		35 1.5			 65 45 2		°C/W
$\overline{ON}$/OFF CONTROL Test Circuit *Figure 1*								
$\overline{ON}$/OFF Pin Logic Input Level	V_{OUT} = 0V V_{OUT} = 5V T_J = 25°C	2.4 2.2	1.5 1.4	 0.8 1.0	2.4 2.2	1.5 1.4	 0.8 1.0	V
$\overline{ON}$/OFF Pin Input Current	$\overline{ON}$/OFF Pin = 5V (OFF) (T_J = 25°C)		12	30		12	30	µA
	$\overline{ON}$/OFF Pin = 0V (ON) (T_J = 25°C)		0	10		0	10	µA

5

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

Note 2: *External components such as the catch diode. Inductor, input and output capacitors can affect switching regulator system performance. When the UC1576/UC2576 Is used as shown in the Figure 1 test circuit, system performance will be as shown in system parameters section of Electrical Characteristics.*

Note 3: *Output (pin 2) sourcing current. No diode, inductor or capacitor connected to output.*

Note 4: *Feedback (pin 4) removed from output and connected to 0V.*

Note 5: *Feedback (pin 4) removed from output and connected to 12V to force the output transistor OFF.*

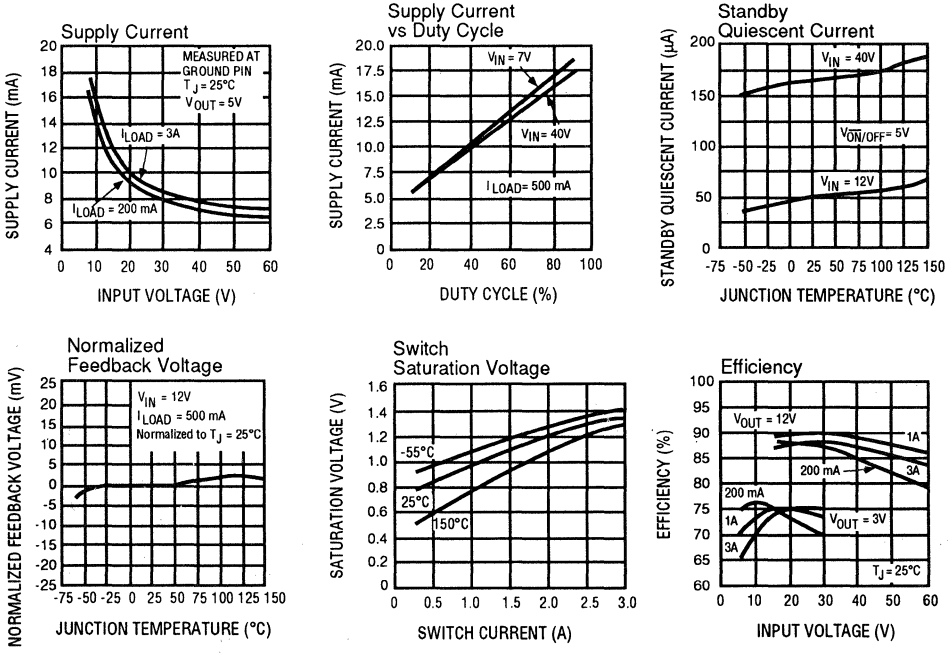
Note 6: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/2 inch leads in a socket, or on a PC board with minimum copper area.*

Note 7: *Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with 1/4 inch leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.*

Note 8: *The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which the feedback voltage lower than .7V. This self protection features lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.*

Note 9: *Refer to RETS UC1576K-ADJ For current revision of military RETS/SMD.*

Typical Performance Characteristics *(Circuit of Figure 1)*



UC1576 Series Buck Regulator Design Procedure

PROCEDURE

Given:

V_{OUT} = Regulated Output Voltage
V_{IN} (max) = Minimum Input Voltage
I_{LOAD} (max) = Maximum Load Current
F = Switching Frequency (52kHz)

Example: V_{OUT} = 10V, V_{IN} (max) = 25V, I_{LOAD} (max) = 3A, F = 52kHz

1. Programming Output Voltage (Selecting R1 and R2)

The following formula can be used to select the resistor values for a given voltage:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right)$$

And for a given R1 (between 1K and 10K),

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Example:

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right) \text{ select R1 = 1K:}$$

$$R2 = R1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{10V}{1.23V} - 1\right) = 7.13K, \text{ use closest 1\% value 7.15K.}$$

2. Inductor Selection (L1)

A. Calculate E•T(V•μS), from the following formula:

$$E{\bullet}T = (V_{IN} - V_{OUT}) \bullet \frac{V_{OUT}}{V_{IN}} \bullet \frac{1000}{F(\text{in kHz})} \quad (V{\bullet}\mu S)$$

B. Use the E•T value from above and match it with the E•T number on the vertical axis of the Inductor value selection guide shown in Figure 2.

C. On the horizontal axis, select the minimum load current. Find the region intersected by the E.T value and the maximum load current value and note the inductor code for the region.

D. Match the inductor code to the inductor value, using Fig. 3.

Example:

Calculating E•T (V•μS):

$$E{\bullet}T = (25 - 10) \bullet \frac{10}{25} \bullet \frac{1000}{52} = 115\ V{\bullet}\mu S$$

For I_{LOAD} = 3A and E•T = 115V•μS, Inductor code is H150 and the inductor value is 150μH.

3. Output Capacitor Selection (C_{OUT})

A. The dominant pole-pair of the switching regulator loop is defined by the value of the output capacitor and the inductor. In order to achieve stable operation, the capacitor must satisfy the following requirement.

$$C_{OUT} > 13{,}300 \bullet \frac{V_{IN}\ (max)}{V_{OUT} \bullet L(\mu H)} \quad (\mu F)$$

Example:

$$C_{OUT} > 13{,}300 \bullet \frac{25}{10 \bullet 150} = 221\mu F$$

For acceptable ripple voltage, select C_{OUT} = 680μF electrolytic capacitor.

The ESR (Equivalent Series Resistance) of the output capacitor is the primary cause of the output ripple voltage and the value and the type of the output capacitor determine the amount of ESR and thus the output ripple voltage. In general lower capacitor values have higher ESR ratings.

Capacitor values larger than 680µF will produce an output ripple voltage of 35mV to 50mV, while smaller capacitors (220µF to 680µF) will typicaly cause a ripple of 50mV to 150mV. The following approximate relationship could be used in determining the output ripple:

$$V_{RIPPLE}\ p\text{-}p > 0.3 \times I_{LOAD}(max) \times ESR$$

It is possible to reduce the output ripple to 10mV-20mV by using several standard electrolytic capacitors in parallel or by using higher grade capacitors with low ESR and low inductance. However, ESR values lower than 0.05 Ohms can cause instability. The capacitor's ripple current rating at 52kHz should be at least 50% higher than the inductor current ripple:

$$I_{RIPPLE}(max) > 1.5 \times 0.3 \times I_{LOAD}(max)$$

B. The voltage rating of the output capacitor should be at least 1.2 times greater that the output voltage. For a 10V output, a rating of 15V is appropriate, and a 20V rating is recommended.

4. Catch Diode Selection (D1)

The current rating of the catch diode must be at least 1.2 times greater than the maximum load current, unless the diode is expected to withstand a continuous output short, in which case the current rating of the diode should be equal to the maximum current rating of UC2576.

A. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.

B. Schottky diodes with fast switching speed and a low forward voltage drop are the most efficient. Some types of diodes with an abrupt turn-off characteristic may cause instability and EMI problems. Therefore in general, a fast-recovery diode with soft recovery characteristics is recommended.

See Figure 4 for Schottky and "soft" fast-recovery diode selection guide.

5. Input Capacitor (CIN)

To assure stability, the regulator input pin must be bypassed with a by-pass capacitor of at least 47 µF, low ESR (electrolytic type). If an operation at low temperatures (for example -25°C) is intended, then addition of a ceramic or solid tantalum capacitor near the input pin may be required to maintain the capacitance value and low ESR at low temperature.

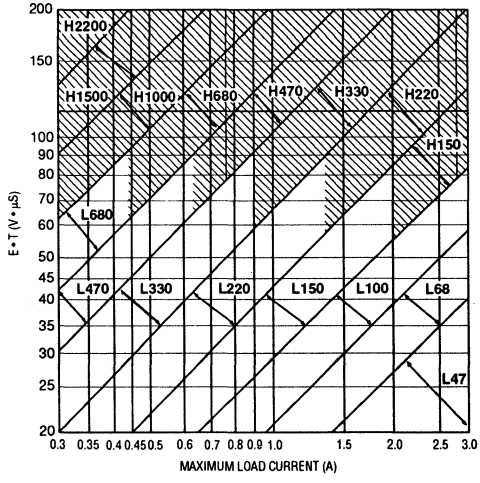


Figure 2. Inductor Value Selection Guide (for Continuous Mode Operation)

Inductor Code	Inductor Value	AIE (Note 1)	Pulse Eng. (Note 2)	Renco (Note 3)
L47	47 µH	415-0932	PE-53112	RL2442
L68	68 µH	415-0931	PE-92114	RL2443
L100	100 µH	415-0926	PE-52627	RL1952
L150	150 µH	415-0953	PE-53113	RL1954
L220	220 µH	415-0922	PE-52626	RL1953
L330	330 µH	415-0926	PE-52627	RL1952
L470	470 µH	415-0927	PE-53114	RL1951
L680	680 µH	415-0928	PE-52629	RL1950
H150	150 µH	415-0936	PE-53115	RL2445
H220	220 µH	430-0636	PE-53116	RL2446
H330	330 µH	430-0635	PE-53117	RL2447
H470	470 µH	430-0634	PE-53118	RL1961
H680	680 µH	415-0935	PE-53119	RL1960
H1000	1000 µH	415-0934	PE-53120	RL1959
H1500	1500 µH	415-0933	PE-53121	RL1958
H2200	2200 µH	415-0945	PE-53122	RL2448

Note 1: *AIE Magnetics, Div. Vernitron Corp. Passive Components Group, (813) 347-2181 2801 72nd Street North, St. Petersburg, FL 33710*

Note 2: *Pulse Engineering, (619) 268-2400 P.O. Box 12235, San Diego, CA 92112*

Note 3: *Renco Electronics Inc., 60 Jeffnyn Blvd. East, Deer Park, NY 11729 (516) 586-5566*

FIGURE 3. Inductor Selection by Manufacturer's Part Number

V_{IN} (max)	Schottky		Fast Recovery	
	3A	4A-6A	3A	4A-6A
20V	1N5820 MBR320P SR302	1N5823	The following diodes are all rated to 100V 31DF1 HER302	The following diodes are all rated to 100V 50WF10 MUR410 HER602
30V	1N5821 MBR330 31DQ03 SR303	50WQ03 31DQ03 1N5824		
40V	1N5822 MBR340 31DQ04 SR304	MBR340 31DQ04 50WQ04 1N5825		
50V	MBR350 31DQ05 SR305	50WQ05		
60V	MBR360 DQ06 SR306	50WQ06 50SQ060		

Figure 4. Diode Selection Chart

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ADVANCED INFORMATION

Simple Step-Up Fixed Voltage Regulators

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, Can Stand Off 65V
- Extended Input Voltage Range: 2.9V to 40V
- Current-Mode Operation for Improved Transient Response, Line Regulation and Current Limiting
- Sleep Mode Feature with Low Quiescent Current
- Soft Start Function Provides Controlled Start-up
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, Under-Voltage Lockout and Thermal Shutdown
- Improved Replacement for LM2577 Series

TYPICAL APPLICATIONS

- Simple Boost and Flyback Converters
- Transformer Coupled Forward Regulators
- Multiple-Output Designs

DESCRIPTION

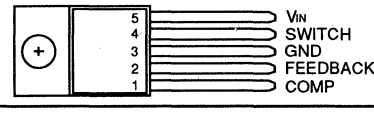
The UC1577 family of devices provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide fixed output voltages of 12V or 15V as step-up regulators.

The UC1577 series features a wide input voltage range of 2.9V to 40V. An on chip 3.0A NPN switch is included with undervoltage lockout and thermal protection circuitry and current limiting. A sleep mode is provided with low quiescent current, as well as soft-start mode operation to reduce current during start-up. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

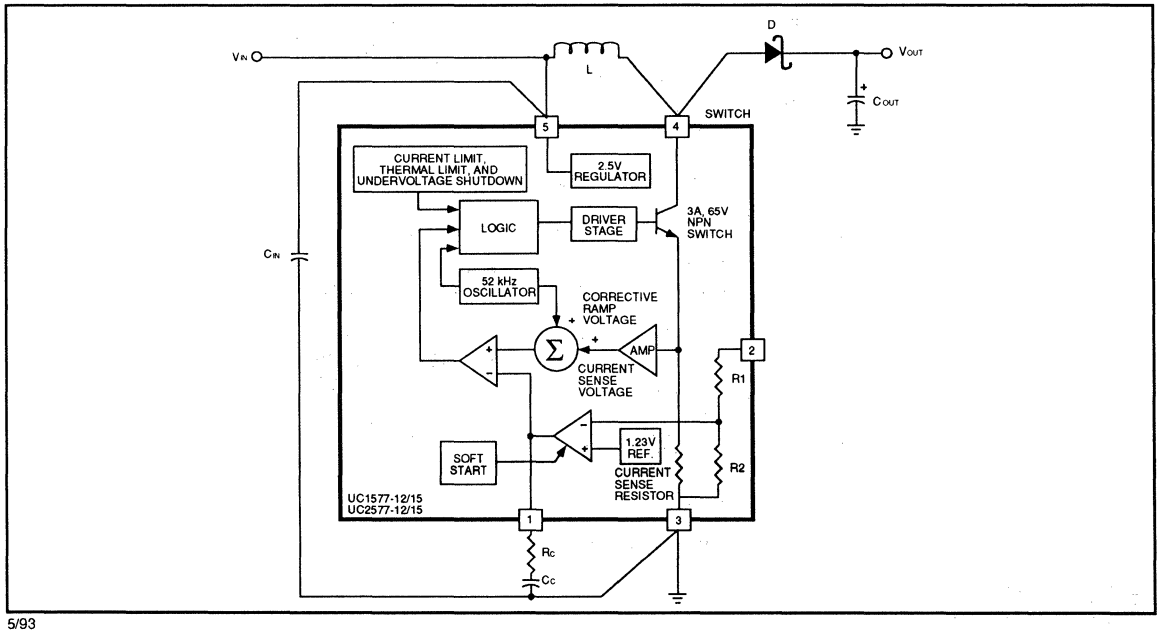
A standard series of inductors and capacitors are available from several manufacturers optimized for use with these regulators. (See specifications for UC1577-ADJ/UC2577-ADJ for part lists.)

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating
(C = 100 pF, R = 1.5 kΩ) ..... 2 kV

RECOMMENDED OPERATING RANGE

Supply Voltage ..... $2.9 \le V_{IN} \le 40V$
Output Switch Voltage ..... $0V \le V_{SWITCH} \le 60V$
Output Switch Current ..... $I_{SWITCH} \le 3.0A$
Junction Temperature Range
UC1577 ..... $-55°C \le T_J \le +150°C$
UC2577 ..... $-40°C \le T_J \le +125°C$

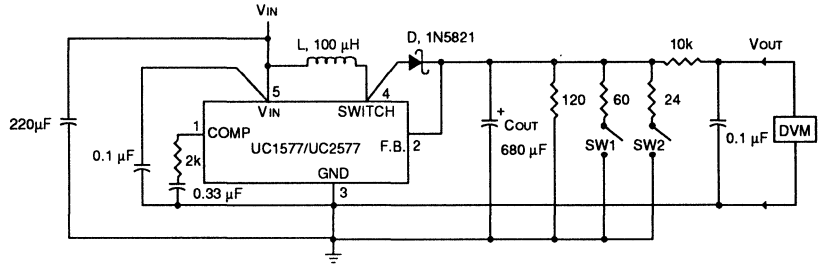
ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, $T_A = T_J$.) Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

		UC1577-12			UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS Circuit *Figure 1* (Note 3)								
Output Voltage	V_{IN} = 5V to 10V I_{LOAD} = 100 mA to 800 mA T_J = 25°C	11.40 11.60	12.0	12.60 12.40	11.40 11.60	12.0	12.60 12.40	V
Line Regulation	V_{IN} = 2.9V to 12V, I_{LOAD} = 300 mA T_J = 25°C		20	100 50		20	100 50	mV
Load Regulation	V_{IN} = 5V, I_{LOAD} = 100 mA to 800 mA T_J = 25°C		20	100 50			100 50	mV
Efficiency	V_{IN} = 5V, I_{LOAD} = 800 mA		80			80		%
DEVICE PARAMETERS								
Input Supply Current	$V_{FEEDBACK}$ = 14V (Switch Off) T_J = 25°C		7.5	14 10		7.5	14 10	mA
	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle) T_J = 25°C		25	85 50		25	85 50	mA
	V_{COMP} = 0, (Sleep), V_{IN}=5V, (Note 5)		250	400		250	400	µA
Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA T_J = 25°C	2.60 2.65	2.70	2.80 2.75	2.60 2.65	2.70	2.80 2.75	V
Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA T_J = 25°C	42 48	52	62 56	42 48	52	62 56	kHz
Output Reference Voltage	Measured at Feedback Pin V_{IN} = 2.9V to 40V, V_{COMP} = 1.0V T_J = 25°C	11.64 11.76	12	12.36 12.26	11.64 11.76	12	12.36 12.26	V
Reference Voltage Line Regulation	V_{IN} = 2.9V to 40V		7			7		mV
Feedback Pin Input Resistance			9.7			9.7		KΩ
Error Amp Transconductance	I_{COMP} = -30 µA to + 30 µA V_{COMP} = 1.0V T_J = 25°C	145 225	370	615 515	145 225	370	615 515	µmho
Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V, R_{COMP} = 1.0 MΩ (Note 4) T_J = 25°C	25 50	80		25 50	80		V/V
Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 10.0V T_J = 25°C	2.0 2.2	2.4		2.0 2.2	2.4		V
	Lower Limit $V_{FEEDBACK}$ = 15.0V T_J = 25°C		0.3	0.55 0.40		0.3	0.55 0.40	V

5

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, T_A = T_J.) Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

		UC1577-12			UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
DEVICE PARAMETERS Continued								
Error Amp Output Current	$V_{FEEDBACK}$ = 10.0V to 15.0V V_{COMP} = 10.0V T_J = 25°C	±90 ±130	±200	±400 ±300	±90 ±130	±200	±400 ±300	µA
Soft Start Current	$V_{FEEDBACK}$ = 10.0V V_{COMP} = 0.5V T_J = 25°C	1.5 2.5	5.0	9.5 7.5	1.5 2.5	5.0	9.5 7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100mA T_J = 25°C	90 93	95		90 93	95		%
Switch Transconductance			12.5			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 1.5V (Switch Off) T_J = 25°C		10	600 300		10	600 300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle) T_J = 25°C		0.5	0.9 0.7		0.5	0.9 0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V T_J = 25°C	3.0 3.7	4.3	6.0 5.3	3.0 3.7	4.3	6.0 5.3	A
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case		35 1.5					°C/W
	T Package, Junction to Ambient T Package, Junction to Case					65 2		
COMP Pin Sleep Threshold	V_{OUT} = 0 T_J = 25°C	110 130	150	190 170	110 130	150	190 170	mV
COMP Pin Current	V_{COMP} = 0 T_J =25°C	35 40	50	65 60	35 40	50	65 60	µA



L = 415-0930 (AIE)
D = Any Manufacturer

C_{OUT} = Spraque Type 673 D Electrolytic 680µF, 20V

Note: Pin numbers shown are for TO-220 (T) Package.

Figure 1. Circuit used for System Parameters Specifications

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating
(C = 100 pF, R = 1.5 kΩ) ..... 2 kV

RECOMMENDED OPERATING RANGE

Supply Voltage ..... $2.9 \le V_{IN} \le 40V$
Output Switch Voltage ..... $0V \le V_{SWITCH} \le 60V$
Output Switch Current ..... $I_{SWITCH} \le 3.0A$
Junction Temperature Range
UC1577 ..... $-55°C \le T_J \le +150°C$
UC2577 ..... $-40°C \le T_J \le +125°C$

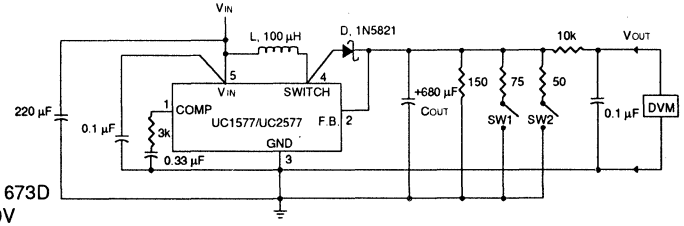
ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, $T_A = T_J$). Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

		UC1577-15			UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS Circuit *Figure 2* (Note 3)								
Output Voltage	V_{IN} = 5V to 12V I_{LOAD} = 100 mA to 600 mA T_J = 25°C	14.25 14.50	15.0	15.75 15.50	14.25 14.50	15.0	15.75 15.50	V
Line Regulation	V_{IN} = 2.9V to 12V, I_{LOAD} = 300 mA T_J = 25°C		20	100 50		20	100 50	mV
Load Regulation	V_{IN} = 5V, I_{LOAD} = 100 mA to 600 mA T_J = 25°C		20	100 50			100 50	mV
Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		80			80		%
DEVICE PARAMETERS								
Input Supply Current	$V_{FEEDBACK}$ = 1.5V (Switch Off) T_J = 25°C		7.5	14 10		7.5	14 10	mA
	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V(Max Duty Cycle) T_J = 25°C		25	85 50		25	85 50	mA
	V_{COMP} = 0, (Sleep), V_{IN} = 5V, (Note 5)		250	400		250	400	µA
Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA T_J = 25°C	2.60 2.65	2.70	2.80 2.75	2.60 2.65	2.70	2.80 2.75	V
Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA T_J = 25°C	42 48	52	62 56	42 48	52	62 56	kHz
Output Reference Voltage	Measured at Feedback Pin V_{IN} = 2.9V to 40V V_{COMP} = 1.0V, T_J = 25°C	14.55 14.70	15	15.44 15.30	14.55 14.70	15	15.44 15.30	V
Reference Voltage Line Regulation	V_{IN} = 2.9V to 40V		10			10		mV
Feedback Pin Input Resistance			12.2			12.2		KΩ
Error Amp Transconductance	I_{COMP} = -30 µA to + 30 µA V_{COMP} = 1.0V T_J = 25°C	110 170	300	500 420	110 170	300	500 420	µmho
Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V, R_{COMP} = 1.0 MΩ (Note 4) T_J = 25°C	20 40	65		20 40	65		V/V
Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 12.0V T_J = 25°C	2.0 2.2	2.4		2.0 2.2	2.4		V
	Lower Limit $V_{FEEDBACK}$ = 18.0V T_J = 25°C		0.3	0.55 0.40		0.3	0.55 0.40	V

5

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, T_A = T_J.) Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

		UC1577-15			UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
DEVICE PARAMETERS Continued								
Error Amp Output Current	$V_{FEEDBACK}$ = 12.0V to 18.0V V_{COMP} = 1.0V T_J = 25°C	±90 ±130	±200	±400 ±300	±90 ±130	±200	±400 ±300	µA
Soft Start Current	$V_{FEEDBACK}$ = 12.0V V_{COMP} = 0.5V T_J = 25°C	1.5 2.5	5.0	9.5 7.5	1.5 2.5	5.0	9.5 7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100mA T_J = 25°C	90 93	95		90 93	95		%
Switch Transconductance			12.5			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 1.5V (Switch Off) T_J = 25°C		10	600 300		10	600 300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle) T_J = 25°C		0.5	0.9 0.7		0.5	0.9 0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V T_J = 25°C	3.0 3.7	4.3	6.0 5.3	3.0 3.7	4.3	6.0 5.3	A
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case		35 1.5					°C/W
	T Package, Junction to Ambient T Package, Junction to Case					65 2		
COMP Pin Sleep Threshold	V_{OUT} = 0 T_J = 25°C	120 130	150	180 170	120 130	150	180 170	mV
COMP Pin Current	COMP = 0 T_J =25°C	35 40	50	65 60	35 40	50	65 60	µA



L = 415-0930 (AIE)
D = Any Manufacturer
C_{OUT} = Spraque Type 673D Electrolytic 680 µF, 20V

Note: Pin numbers shown are for TO-220 (T) package.

Figure 2. Circuit used for System Parameter Specifications

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

Note 2: *Output current cannot be internally limited when the UC1577/UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC1577/UC2577 is used as a flyback or forward converter regulator in accordance to the Application Hints.*

Note 3: *External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC1577/UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.*

Note 4: *A 1.0 MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥ 10 MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.*

Note 5: *Comp pin is externally forced to 0V. Supply current during sleep mode is tested at V_{IN} = 5V and could increase with increasing V_{IN}, however, it should typically be less than 500µA within the specified range of V_{IN}.*

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UC1577-ADJ
UC2577-ADJ

ADVANCED INFORMATION

Simple Step-Up Voltage Regulators

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, Can Stand Off 65V
- Extended Input Voltage Range: 2.9V to 40V
- Current-Mode Operation for Improved Transient Response, Line Regulation and Current Limiting
- Sleep Mode Feature with Low Quiescent Current
- Soft Start Function Provides Controlled Start-up
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, Under-Voltage Lockout and Thermal Shutdown
- Improved Replacement for LM2577-ADJ Series

DESCRIPTION

The UC1577-ADJ family of devices provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide up to 60V as a step-up regulator, and even higher as a flyback or forward converter regulator.

The UC1577-ADJ series feature a wide input voltage range of 2.9V to 40V and an adjustable output voltage. An on chip 3.0A NPN switch is included with undervoltage lockout and thermal protection circuitry and current limiting. A sleep mode is provided with low quiescent current, as well as soft-start mode operation to reduce current during start-up. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

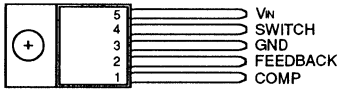
A standard series of inductors and capacitors are available from several manufacturers optimized for use with these regulators and are listed in this data sheet.

TYPICAL APPLICATIONS

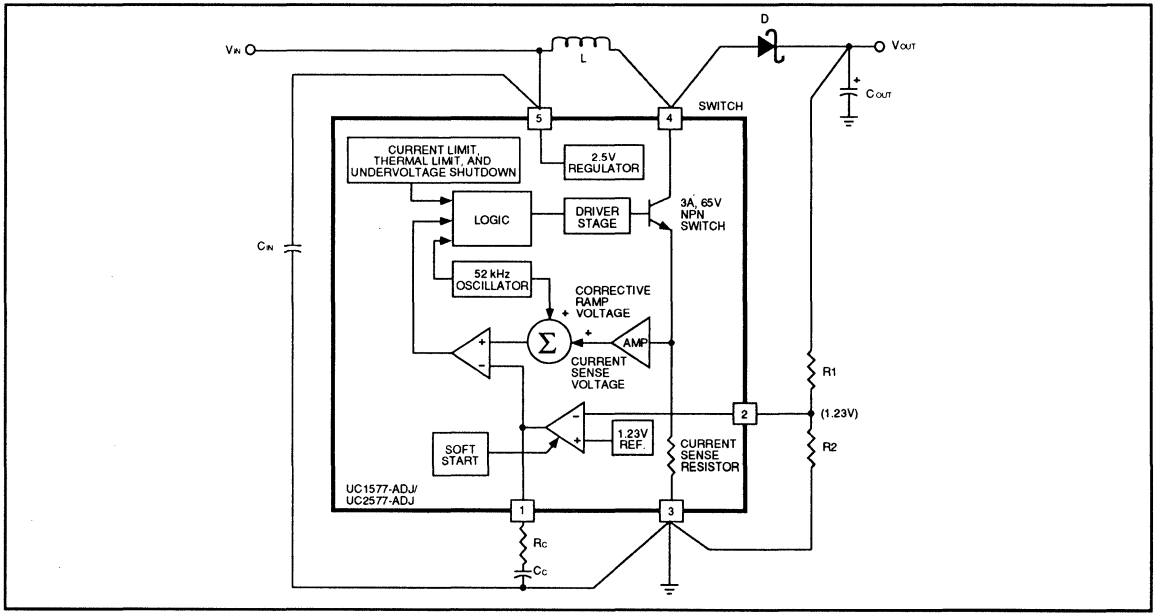
- Simple Boost and Flyback Converters
- Transformer Coupled Forward Regulators
- Multiple-Output Designs

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T-Package



BLOCK DIAGRAM



5/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

If Military/Aerospace specified devices are required, please contact the UICC Sales Office/Distributors for availability and specifications.

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating
(C = 100 pF, R = 1.5 kΩ) ..... 2 kV

RECOMMENDED OPERATING RANGE

Supply Voltage ..... $2.9V \le V_{IN} \le 40V$
Output Switch Voltage ..... $0V \le V_{SWITCH} \le 60V$
Output Switch Current ..... $I_{SWITCH} \le 3.0A$
Junction Temperature Range
UC1577 ..... $-55°C \le T_J \le +150°C$
UC2577 ..... $-40°C \le T_J \le +125°C$

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, $T_A = T_J$.) Unless otherwise specified, V_{IN} = 5V, $V_{FEEDBACK} = V_{REF}$, and I_{SWITCH} = 0.

		UC1577-ADJ			UC2577-ADJ			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
SYSTEM PARAMETERS Circuit *Figure 1* (Note 3)								
Output Voltage	V_{IN} = 5V to 10V I_{LOAD} = 100 mA to 800 mA T_J = 25°C	11.40 11.60	12.0	12.60 12.40	11.40 11.60	12.0	12.60 12.40	V
Line Regulation	V_{IN} = 2.9V to 10V, I_{LOAD} = 300 mA T_J = 25°C		20	100 50		20	100 50	mV
Load Regulation	V_{IN} = 5V, I_{LOAD} = 100 mA to 800 mA T_J = 25°C		20	100 50		20	100 50	mV
Efficiency	V_{IN} = 5V, I_{LOAD} = 800 mA		80			80		%
DEVICE PARAMETERS								
Input Supply Current	$V_{FEEDBACK}$ = 1.5V (Switch Off) T_J = 25°C		7.5	14 10		7.5	14 10	mA
	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle) T_J = 25°		25	85 50		25	85 50	mA
	V_{COMP} = 0 (Sleep), Vin = 5V, (Note 5)		250	400		250	400	µA
Input Supply Undervoltage Lockout	I_{SWITCH} = 100 mA T_J = 25°	2.60 2.65	2.70	2.80 2.75	2.60 2.65	2.70	2.80 2.75	V
Oscillator Frequency	Measured at Switch Pin I_{SWITCH} = 100 mA T_J = 25°C	42 48	52	62 56	42 48	52	62 56	kHz
Reference Voltage	Measured at Feedback Pin V_{IN} = 2.9V to 40V, V_{COMP} = 1.0V T_J = 25°C	1.206 1.214	1.230	1.254 1.246	1.206 1.214	1.230	1.254 1.246	V
Reference Voltage Line Regulation	V_{IN} = 2.9V to 40V		0.5			0.5		mV
Error Amp Input Bias Current	V_{COMP} = 1.0V T_J = 25°C		100	800 300		100	800 300	nA
Error Amp Transconductance	I_{COMP} = -30 µA to + 30 µA, V_{COMP} = 1.0V T_J = 25°C	1600 2400	3700	5800 4800	1600 2400	3700	5800 4800	µmho
Error Amp Voltage Gain	V_{COMP} = 1.1V to 1.9V, R_{COMP} = 1.0 MΩ (Note 4) T_J = 25°C	250 500	800		250 500	800		V/V
Error Amplifier Output Swing	Upper Limit $V_{FEEDBACK}$ = 1.0V T_J = 25°C	2.0 2.2	2.4		2.0 2.2	2.4		V
	Lower Limit $V_{FEEDBACK}$ = 1.5V T_J = 25°C		0.3	0.55 0.40		0.3	0.55 0.40	V

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for T_A = -55°C to +150°C for UC1577 and -40°C to +125°C for the UC2577, T_A =T_J.) Unless otherwise specified, V_{IN} = 5V, and I_{SWITCH} = 0.

		UC1577-ADJ			UC2577-ADJ			
PARAMETER	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
DEVICE PARAMETERS Continued								
Error Amp Output Current	$V_{FEEDBACK}$ = 1.0V to 1.5V V_{COMP} = 1.0V T_J = 25°C	±90 ±130	±200	±400 ±300	±90 +130	±200	±400 ±300	µA
Soft Start Current	$V_{FEEDBACK}$ = 1.0V V_{COMP} = 0.5V T_J = 25°C	1.5 2.5	5.0	9.5 7.5	1.5 2.5	5.0	9.5 7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V I_{SWITCH} = 100mA T_J = 25°C	90 93	95		90 93	95		%
Switch Transconductance			12.5			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V $V_{FEEDBACK}$ = 1.5V (Switch Off) T_J = 25°C		10	600 300		10	600 300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A V_{COMP} = 2.0V (Max Duty Cycle) T_J = 25°C		0.5	0.9 0.7		0.5	0.9 0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V T_J = 25°C	3.0 3.7	4.3	6.0 5.3	3.0 3.7	4.3	6.0 5.3	A
Thermal Resistance	K Package, Junction to Ambient K Package, Junction to Case		35 1.5					°C/W
	T Package, Junction to Ambient T Package, Junction to Case					65 2		
COMP Pin Sleep Mode Threshold	V_{OUT} = 0 T_J = 25°C	120 130	150	180 170	120 130	150	180 170	mV
COMP Pin Current	V_{COMP} = 0 T_J =25°C	35 40	50	65 60	35 40	50	65 60	µA

Note 1: *Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.*

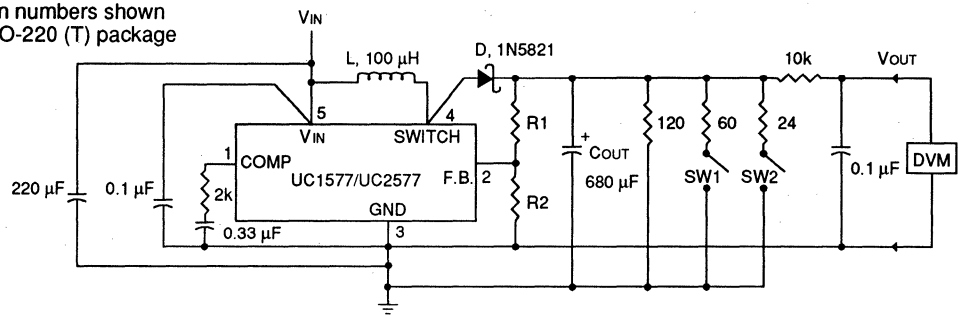
Note 2: *Output current cannot be internally limited when the UC1577/UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC1577/UC2577 is used as a flyback or forward converter regulator in accordance to the Application Hints.*

Note 3: *External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC1577/UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.*

Note 4: *A 1.0 MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥ 10 MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.*

Note 5: *Comp pin is externally forced to 0V. Supply current during sleep mode is tested at V_{IN} = 5V and could increase with increasing V_{IN}, however, it should typically be less than 500µA within the specified range of V_{IN}.*

Note: Pin numbers shown are for TO-220 (T) package



L = 415-0930 (AIE)
D = any manufacturer

COUT = Sprague Type 673D
Electrolytic 680 µF, 20V

R1 = 48.7k in series with 511Ω(1%)
R2 = 5.62k (1%)

Figure 1. Circuit Used to Specify System Parameters

STEP-UP (BOOST) REGULATOR

The Block Diagram shows a Step-Up switching Regulator utilizing the UC1577/UC2577. The regulator produces an output voltage higher than the input voltage when the UC1577 turns its switch on and off at a fixed frequency of 52kHz, thus storing energy in the inductor (L). When the NPN switch is on, the inductor current is charged at a rate of VIN/L. When the switch is turned off, the lower terminal of the inductor rises above Vin, discharging the stored current through the output diode (D) into the output capacitor (COUT) at a rate of (VOUT - VIN)/L. The energy stored in the inductor is thus transferred to the output.

The output voltage is controlled by the amount of energy transferred, which is controlled by modulating the peak inductor current. This modulation is done by feeding a portion of the output voltage to an error amplifier which amplifies the difference between the feedback voltage and an internal 1.23V precision reference voltage. The output of the error amplifier is than compared to a voltage proportional to the switch current, or the inductor current, during the switch on time. The comparator terminates the switch on time when the two voltages are equal and thus controlling the peak switch current to maintain a constant output voltage. Figure 2 shows voltage and current waveforms for the circuit. Formulas for calculation are shown in Figure 3.

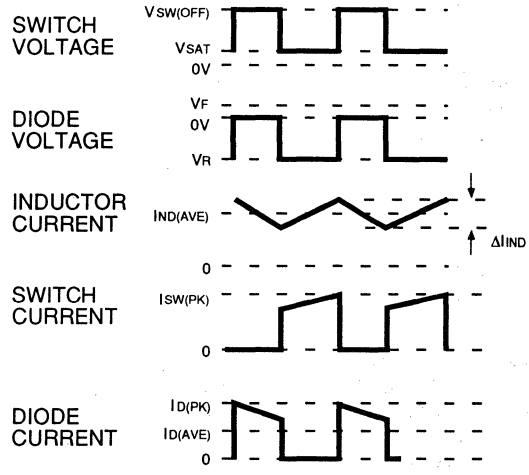


Figure 2. Step-Up Regulator Waveforms

Duty Cycle	D	$\frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F - V_{SAT}} \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$
Average Inductor Current	$I_{IND(AVE)}$	$\frac{I_{LOAD}}{1 - D}$
Inductor Current Ripple	ΔI_{IND}	$\frac{V_{IN} - V_{SAT}}{L} \frac{D}{52{,}000}$
Peak Inductor Current	$I_{IND(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Peak Switch Current	$I_{SW(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Switch Voltage When Off	$V_{SW(OFF)}$	$V_{OUT} + V_F$
Diode Reverse Voltage	V_R	$V_{OUT} - V_{SAT}$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1 - D} + \frac{\Delta I_{IND}}{2}$
Power Dissipation Of UC1577/2577	P_D	$0.25\Omega \left(\frac{I_{LOAD}}{1 - D}\right)^2 D + \frac{I_{LOAD}\, D\, V_{IN}}{50\,(1 - D)}$

VF = Forward Biased Diode Voltage LOAD = Output Load Current

Figure 3. Step-Up Regulator Formulas

STEP-UP REGULATOR DESIGN PROCEDURE

Given:

V_{IN} (min) = Minimum input supply voltage
V_{OUT} = Regulated output voltage
I_{LOAD} (max) = Maximum output load current

First, determine if the UC1577/ UC2577 can provide these values of V_{OUT} and I_{LOAD} (max) when operating with the minimum value of V_{IN}. The upper limits for V_{OUT} and I_{LOAD} (max) are given by the following equations.

$$V_{OUT} \leq 60V$$

and $V_{OUT} \leq 10 \times V_{IN}$ (min)

$$I_{LOAD(max)} \leq \frac{2.1A \times V_{IN}\,(min)}{V_{OUT}}$$

These limits must be greater than or equal to the values specified in this application.

1. Output Voltage Selection

Resistors R1 and R2 are used to select the desired output voltage. These resistors form a voltage divider and present a portion of the output voltage to the error amplifier which compares it to an internal 1.23V reference. Select R1 and R2 such that:

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

2. Inductor Selection (L)

A. *Preliminary Calculations:*

To select the inductor, the calculation of the following three parameters is necessary:

D(max), the maximum switch duty cycle ($0 \leq D \leq 0.9$):

$$D(max) \quad \frac{V_{OUT} + V_F - V_{IN}\,(min)}{V_{OUT} + V_F - 0.6V}$$

where V_F = 0.5V for Schottky diodes and 0.8V for fast recovery diodes (typically);

E•T, the product of volts x time that charges the inductor:

$$E \cdot T \quad \frac{D(max)\ (V_{IN}(min) - 0.6V)10^6}{52{,}000\ Hz} \quad (V \cdot \mu s)$$

$I_{IND,\,DC}$, the average inductor current under full load;

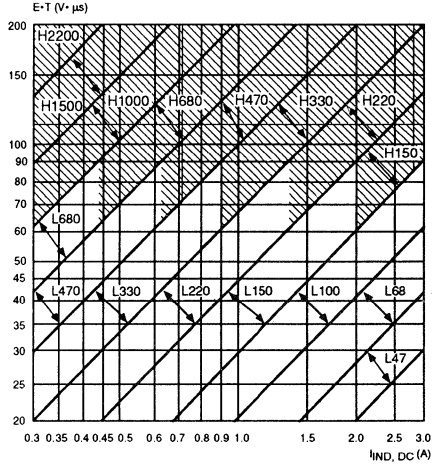
$$I_{IND,\,DC} = \frac{1.05 \times I_{LOAD(max)}}{1 - D(max)}$$

B. *Identify Inductor Value:*

1. From Figure 4, identify the inductor code for the region indicated by the intersection of E•T and $I_{IND,\,DC}$. This code gives the inductor value in microhenries. The L or H prefix signifies whether the inductor is rated for a maximum E•T of 90 V•µs (L) or 250 V•µs (H).
2. If $D < 0.85$, go on to step C. If $D \geq 0.85$, then calculate the minimum inductance needed to ensure the switching regulator's stability:

$$Lmin = \frac{6.4\ (V_{IN}(min) - 0.6V)\ (2D(max) - 1)}{1 - D(max)} \quad (\mu H)$$

If L_{MIN} is smaller than the inductor value found in step B1, go on to step C. Otherwise, the inductor value found in step B1 is too low; an appropriate inductor code should be obtained from the graph as follows:



Note: This chart assumes that the inductor ripple current inductor is approximately 20% to 30% of the average inductor current (when the regulator is under full load). Greater ripple current causes higher peak switch currents and greater ouput ripple voltage; lower ripple current is achieved with larger-value inductors. The factor of 20 to 30% is chosen as a convenient balance between the two extremes.

Figure 4. Inductor Selection Graph

5

1. Find the lowest value inductor that is greater than L_{MIN}.
2. Find where E•T intersects this inductor value to determine if it has an L or H prefix. If E•T intersects both the L and H regions, select the inductor with an H prefix.

C. *Select an inductor* from the table of *Figure 5* which cross references the inductor codes to the part numbers of three different manufacturers. Complete specifications for these inductors are available from the respective manufacturers. The inductors listed in this table have the following characteristics:

AIE: ferrite, pot-core inductors; Benefits of this type are low electro-magnetic interference (EMI), small physical size, and very low power dissipation (core loss). Be careful not to operate these inductors too far beyond their maximum ratings for E•T and peak current above rated value better than ferrite cores.

Pulse: powdered iron, torrid core inductors; Benefits are low EMI and ability to withstand E•T and peak current above rated value better than ferrite cores.

Renco: ferrite, bobbin-core inductors; Benefits are low cost and best ability to withstand E•T and peak current above rated value. Be aware that these inductors generate more EMI than the other types, and this may interfere with signals sensitive to noise.

Inductor Code	Manufacturer's Part Number		
	AIE	Pulse	Renco
L47	415 - 0932	PE - 53112	RL2442
L68	415 - 0931	PE - 92114	RL2443
L100	415 - 0930	PE - 92108	RL2444
L150	415 - 0953	PE - 53113	RL1954
L220	415 - 0922	PE - 52626	RL1953
L330	415 - 0926	PE - 52627	RL1952
L470	415 - 0927	PE - 53114	RL1951
L680	415 - 0928	PE - 52629	RL1950
H150	415 - 0936	PE - 53115	RL2445
H220	430 - 0636	PE - 53116	RL2446
H330	430 - 0635	PE - 53117	RL2447
H470	430 - 0634	PE - 53118	RL1961
H680	415 - 0935	PE - 53119	RL1960
H1000	415 - 0934	PE - 53120	RL1959
H1500	415 - 0933	PE - 53121	RL1958
H2200	415 - 0945	PE - 53122	RL2448

AIE Magnetics, div. Vernitron Corp., (813) 347-218
2801 72nd Street North, St. Petersburg, FL 33710
Pulse Engineering, (619) 268-2400
P.O. Box 12235, San Diego, CA 92112
Renco Electronics Inc., (516) 586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

Figure 5. Table of Standardized Inductors and Manufactuers' Part Numbers

3. Compensation Network (Rc, Cc) and Output Capacitor (C_{OUT}) Selection

The compensation network consists of resistor Rc and capacitor Cc which form a simple pole-zero network and stabilize the regulator. The values of Rc and Cc depend on voltage gain of the regulator, I_{LOAD}(max), the inductor L and output capacitance C_{OUT}. A procedure to calculate and select the values for Rc, Cc and C_{OUT} which ensures stability is described below. It should be noted, however, that this may not result in optimum compensation. To guarantee optimum compensation a standard procedure for testing loop stability is recommended, such as measuring V_{OUT} transient responses to pulsing I_{LOAD}.

A. First, calculate the maximum value for Rc.

$$Rc \leq \frac{750 \times I_{LOAD}(max) \times V_{OUT}^2}{V_{IN}(min)^2}$$

Select a resistor less than or equal to this value, and it should also be no greater than 3 kΩ.

B. Calculate the minimum value for C_{OUT} using the following two equations.

$$C_{OUT} \geq \frac{0.19 \times L \times Rc \times I_{LOAD}(max)}{V_{IN}(min) \times V_{OUT}}$$

and

$$C_{OUT} \geq \frac{V_{IN}(min) \times Rc \times (V_{IN}(min) + (3.74 \times 105 \times L))}{487{,}800 \times V_{OUT}^3}$$

The larger of these two values is the minimum value that ensures stability.

C. Calculate the minimum value of Cc.

$$Cc \geq \frac{58.5 \times V_{OUT}^2 \times C_{OUT}}{Rc^2 \times V_{IN}(min)}$$

The compensation capacitor is also used in the soft start function of the regulator. When input supply to the part is turned on, the switch duty cycle is increased slowly at a rate defined by the compensation capacitor and the soft start current, thus eliminating high input currents. Without the soft-start circuitry, the switch duty cycle would instantly rise to about 90% and draw large currents from the input supply. For proper soft-starting, the value for Cc should be equal or greater than 0.22μF.

Figure 6 lists several types of aluminum electrolytic capacitors which could be used for the output filter. Use the following parameters to select the right capacitor: *Working Voltage (WVDC):* Choose a capacitor with a working voltage at least 20% higher than the regulator output voltage.

Ripple Current: This is the maximum RMS value of current that charges the capacitor during each switching cycle. For step-up and flyback regulators, the formula for ripple current is.

$$I_{RIPPLE(RMS)} = \frac{I_{LOAD(max)} \times D(max)}{1 - D(max)}$$

Choose a capacitor that is rated at least 50% higher than this value at 52 kHz.

Equivalent Series Resistance (ESR): This is the primary cause of output ripple voltage, and it also affects the values of Rc and Cc needed to stabilize the regulator. As a result, the preceding calculations for Cc and Rc are only valid if ESR doesn't exceed the maximum value specified by the following equations.

$$ESR \leq \frac{0.01 \times 15V}{I_{RIPPLE(P-P)}} \text{ and } \leq \frac{8.7 \times (10) - 3 \times V_{IN}}{I_{LOAD(max)}}$$

where

$$I_{RIPPLE(P-P)} = \frac{1.15 \times I_{LOAD(MAX)}}{1 - D(MAX)}$$

Select a capacitor with ESR, at 52 kHz, that is less than or equal to the lower value calculated. Most electrolytic capacitors specify ESR at 120 kHz which is 15% to 30% higher than at 52 kHz. Also, be aware that ESR increases by a factor of 2 when operating at -20°C.

In general, low values of ESR are achieved by using large value capacitors (C ≥ 470 µF), and capacitors with high WVDC, or by paralleling smaller-value capacitors.

4. Input Capacitor Selection (C_{IN})

To reduce noise on the supply voltage caused by the switching action of a step-up regulator (ripple current noise), the Input Voltage pin should be bypassed to ground. A good quality 0.1µF capacitor with low ESR should provide sufficient decoupling. If the UC1577 is located far from the supply source filter capacitors, an extra electrolytic (47µF, for example) is required.

Cornell Dublier–Types 239, 250, 251, UFT, 300, or 350
P.O. Box 128, Pickens, SC 29671 (803) 878-6311

Nichicon–Types PF, PX, or PZ
927 East Parkway, Schaumburg, IL 60173 (708) 843-7500

Sprague–Types 672D, 673D, or 674D
Box 1, Sprague Road, Lansing, NC 28643 (919) 384-2551

United Chemi-Con–Types LX, SXF, or SXJ
9801 West Higgins Road, Rosemont, IL 60018
(708) 696-2000

Figure 6. Aluminum Electrolytic Capacitors Recommended for Switching Regulators

5. Output Diode Selection (D)

In the step-up regulator, the switching diode must withstand a reverse voltage and be able to conduct the peak output current of the UC2577. Therefore a suitable diode must have a minimum reverse breakdown voltage greater than the circuit output voltage, and should also be rated for average and peak current greater than I_{LOAD} (max) and $I_{D(PK)}$. Because of their low forward voltage drop (and thus higher regulator efficiencies,) schottky barrier diodes are often used in switching regulators. Refer to Figure 7 for recommended part numbers and voltage ratings of 1A and 3A diodes.

V_{OUT} (max)	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P	1N5820 MBR320P		
30V	1N5818 MBR130P 11DQ03	1N5821 MBR330P 31DQ03		
40V	1N5819 MBR140P 11DQ04	1N5822 MBR340P 31DQ04		
50V	MBR150 11DQ05	MBR350 31DQ05	1N4933 MUR105	
100V			1N4934 HER102 MUR110 10DL1	MR851 30DL1 MR831 HER302

Figure 7. Diode Selection Chart

6. Sleep Mode

The UC1577/2577 has a unique feature of Sleep Mode. When the COMP pin is externally forced below the Sleep Threshold of 150 mV, the internal regulator to the IC is disabled, thus substantially reducing Input Supply Quiescent current to 250µA typically, for V_{IN}=5V. This current, however, is dependent on the input supply voltage V_{IN} and will increase with increasing V_{IN}. For the specified range of V_{IN} (2.9V to 40V), the Input Supply Current should be typically less than 500µA.

5

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INTEGRATED CIRCUITS
UNITRODE

UC1610
UC3610

Dual Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to +70°C temperature range.

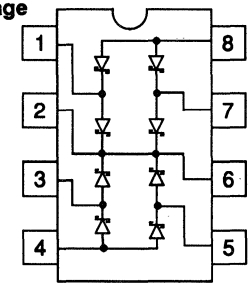
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 ..... 1A
  UC3610 ..... 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

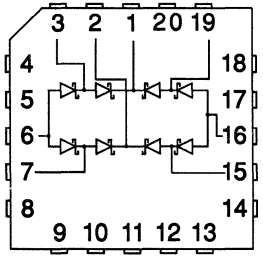
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

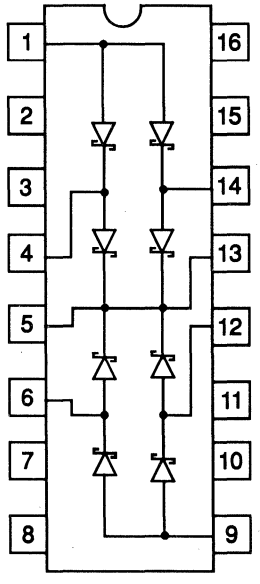
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



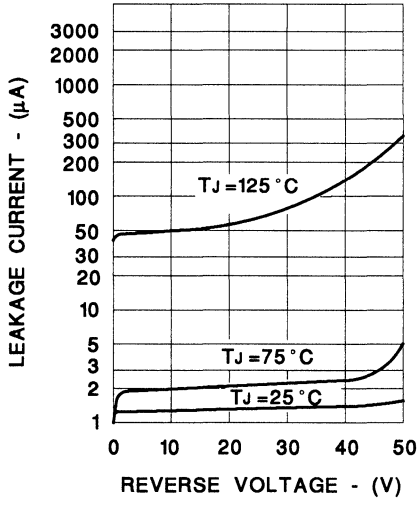
6/93

ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = 25°C except as noted. T_A = T_J.

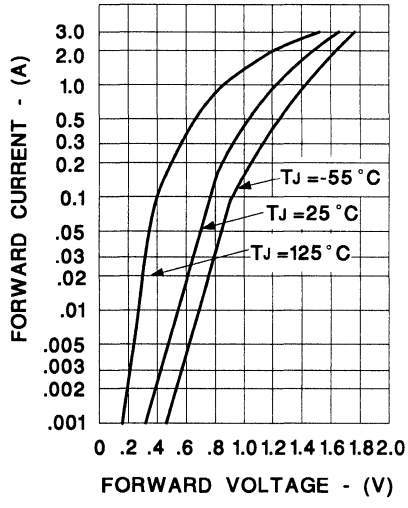
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA	0.4	0.5	0.7	V
	I_F = 1A	0.8	1.0	1.3	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A a parasitic current of approximately 10mA may be collected by adjacent diodes.

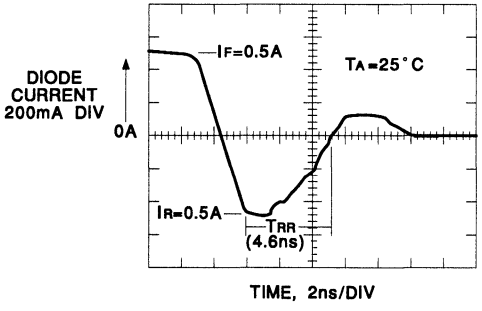
Reverse Current vs Voltage



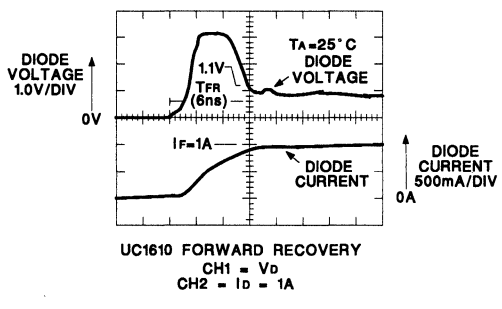
Forward Current vs Voltage



Reverse Recovery Characteristics



Forward Recovery Characteristics



5

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Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low-Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

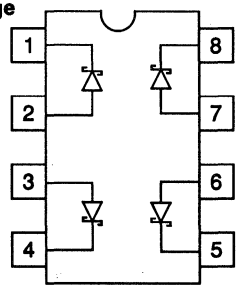
These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

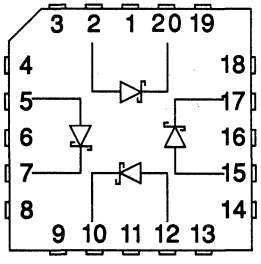
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1611 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

CONNECTION DIAGRAM

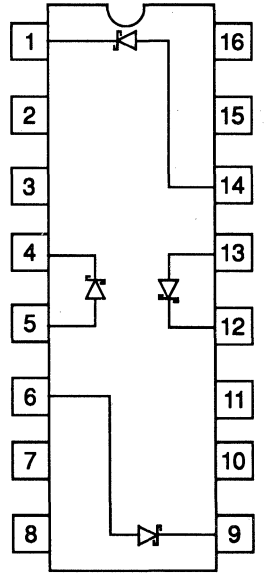
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



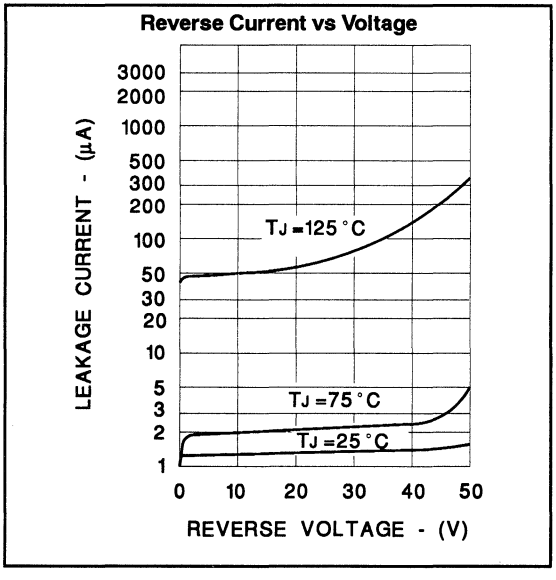
ABSOLUTE MAXIMUM RATINGS

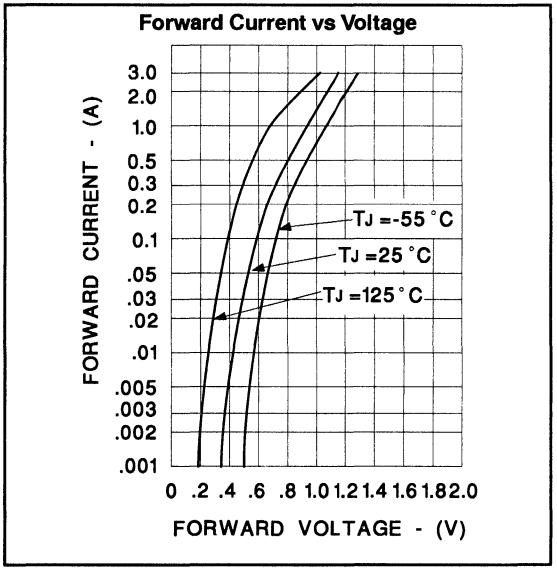
Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
UC1611 ..... 1A
UC3611 ..... 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C
Note: Please consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = +25°C except as noted. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA	0.3	0.4	0.7	V
	I_F = 1A		0.9	1.2	V
Leakage Current	V_R = 40V		0.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

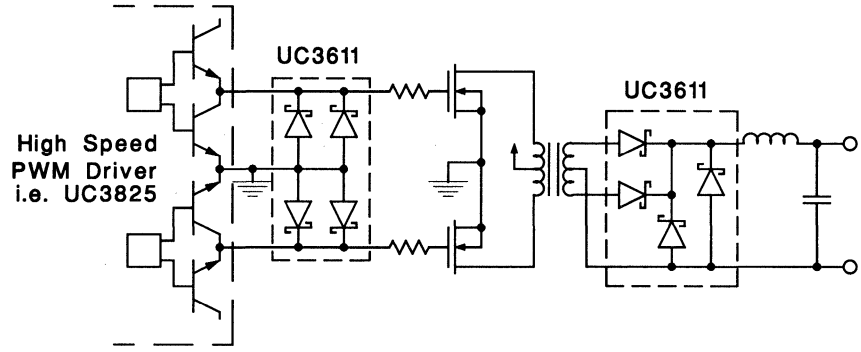
Note: At Forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.



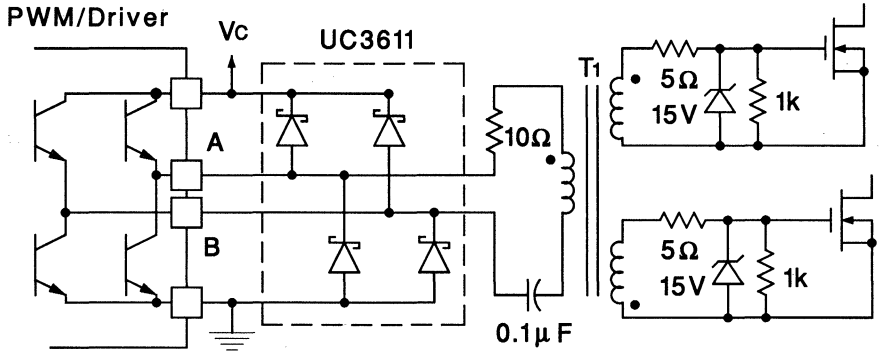


TYPICAL APPLICATIONS

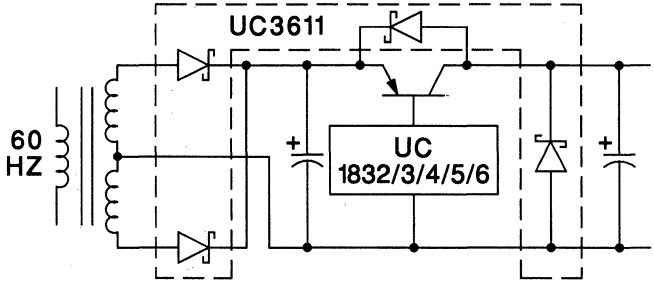
A. Clamp Diodes - PWMS and Drivers



B. Transformer Coupled Drive Circuits



C. Linear Regulations



UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Dual Schottky Diode

FEATURES

- Monolithic Two Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

The two-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in hermetic CERDIP as well as copper leaded plastic MINIDIP and SOIC surface mount power pack. The UC1612 in ceramic is designed for -55°C to +125°C environments, but with reduced peak current capability; while the UC3612 has higher current rating over a 0°C to +70°C ambient temperature range.

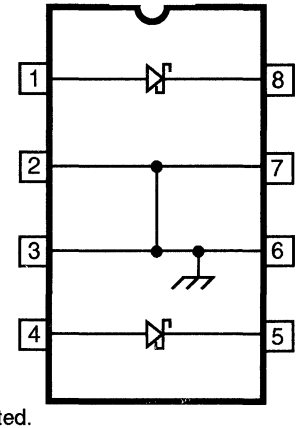
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current, UC3612 ..... 3A
Peak Forward Current, UC1612 ..... 1A
Power Dissipation at TA = 70°C 1W
  Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

5

CONNECTION DIAGRAM

J, N or DP PACKAGE
(TOP VIEW)



Pins 2,3,6,7 are connected to substrate and must be electrically isolated.

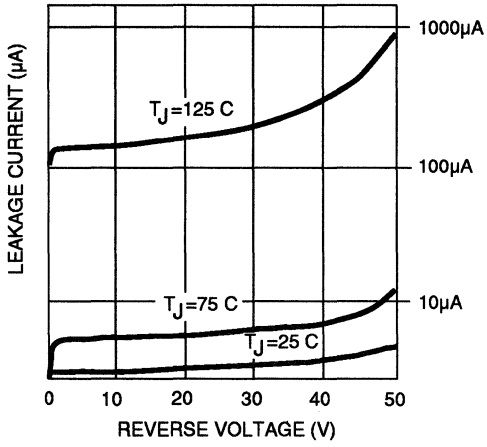
12/92

Electrical Characteristics (All specifications apply to each individual diode. T_J = 25°C except as noted).

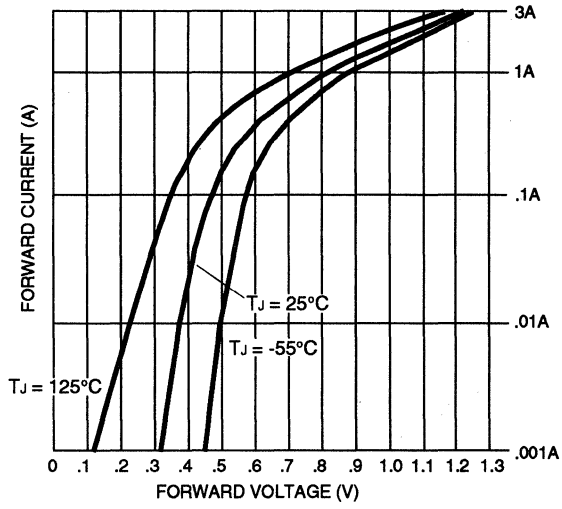
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA		0.49	.55	V
	I_F = 1A		0.90	1.0	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = 100°C		0.1	1.0	mA
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

Reverse Current vs Voltage



Forward Voltage vs Current



INTEGRATED CIRCUITS
UNITRODE

UC1823
UC2823
UC3823

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

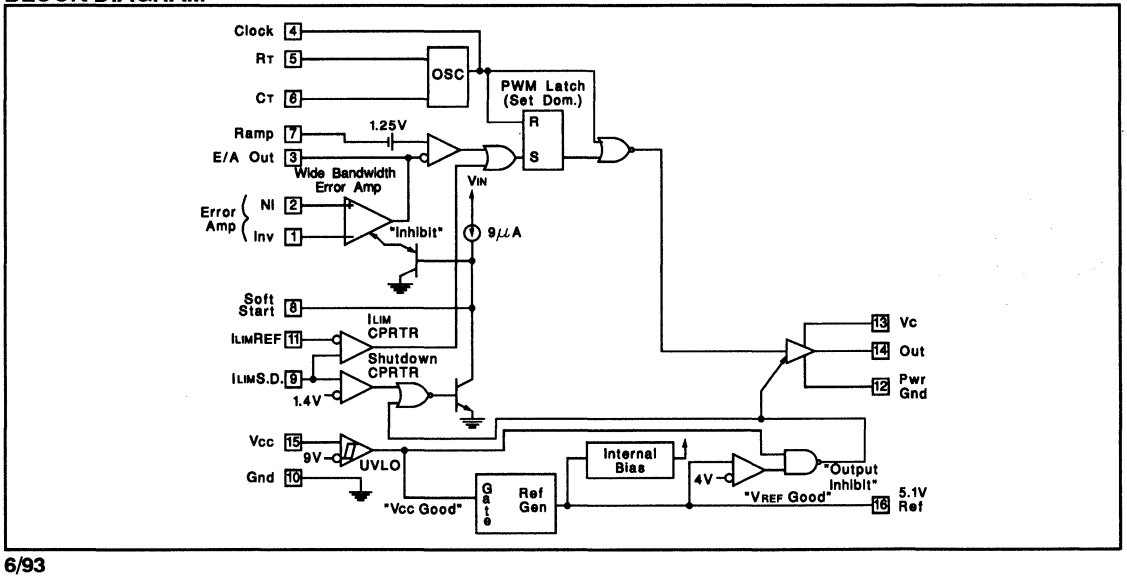
5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5μs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9) ..... -0.3V to +6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation at T_A = 60 °C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

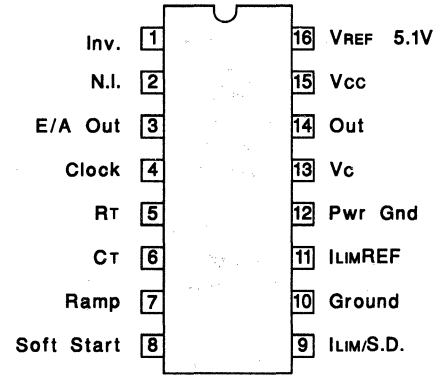
BLOCK DIAGRAM



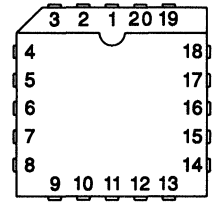
6/93

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv.	2
N.I.	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft start	10
N/C	11
ILIM/S.D.	12
Ground	13
ILIM REF	14
PWR Gnd	15
N/C	16
Vc	17
OUT	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, Vcc = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < Vcc < 30V		2	20		2	20	mV
Load Regulation	1 < Io < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF}=0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J=25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10 < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, Vcc = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	95		60	95		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10 < Vcc < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ =1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µS
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			±10			±10	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	Vc = 30V		100	500		100	500	µA
Rise/Fall Time*	C_L = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	Vcc = 8V		1.1	2.5		1.1	2.5	mA
Icc	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

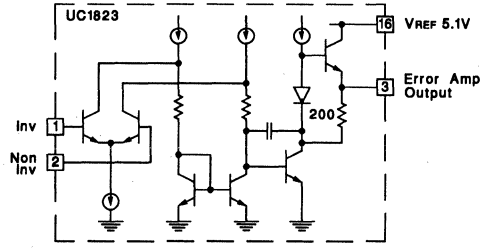
** These parameters are guaranteed by design but not 100% tested in production.*

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

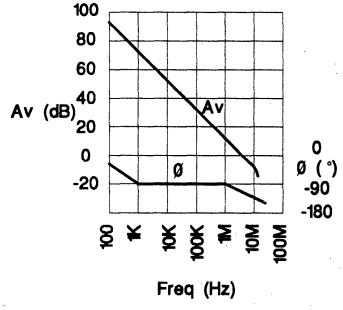
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass Vcc, Vc, and VREF. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

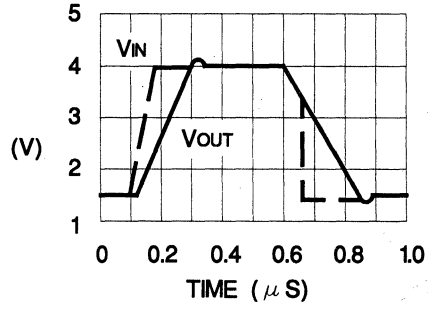
Simplified Schematic



Open Loop Frequency Response

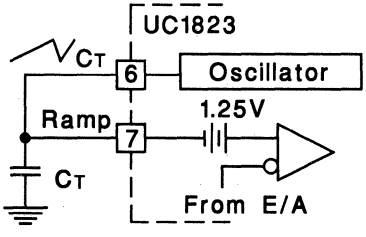


Unity Gain Slew Rate

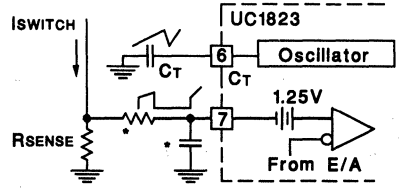


PWM APPLICATIONS

Conventional (Voltage Mode)

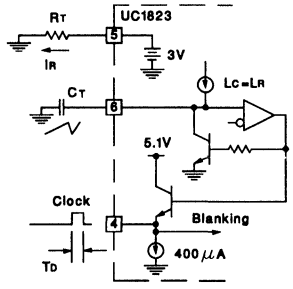


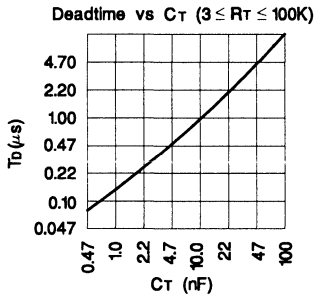
Current-Mode

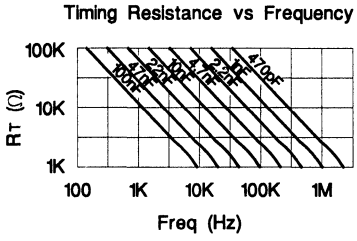


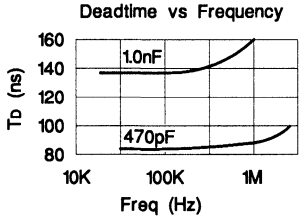
*** A small filter may be required to suppress switch**

OSCILLATOR CIRCUIT





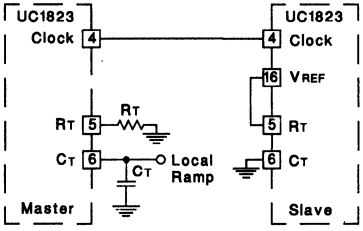




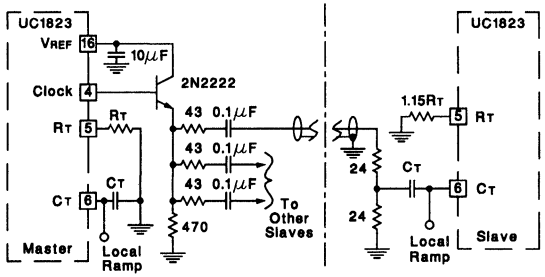
5

SYNCHRONIZED OPERATION

Two Units in Close Proximity

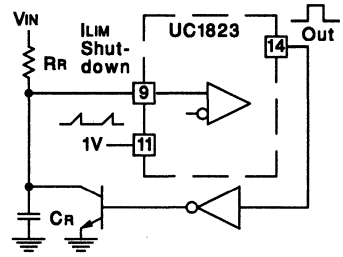


Generalized Synchronization



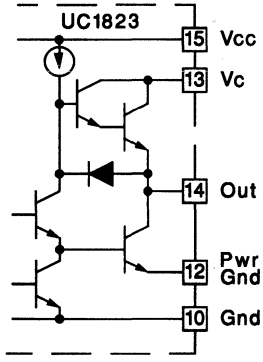
CONSTANT VOLT-SECOND CLAMP CIRCUIT

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

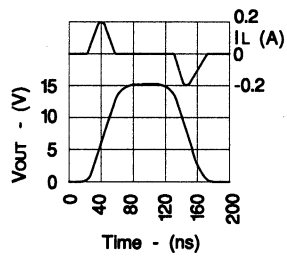


OUTPUT SECTION

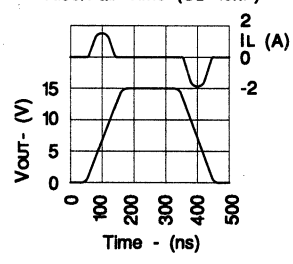
Simplified Schematic



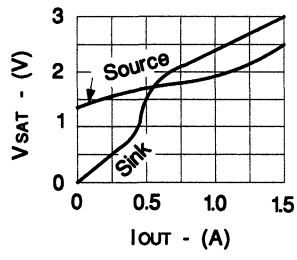
Rise/Fall Time (C_L=1NF)



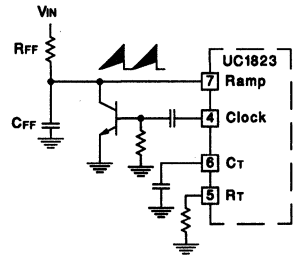
Rise/Fall Time (C_L=10NF)



Saturation Curves



FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



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INTEGRATED CIRCUITS
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UC1823A,B/1825A,B
UC2823A,B/2825A,B
UC3823A,B/3825A,B

High Speed PWM Controller

PRELIMINARY

FEATURES

"Bold Type" Denotes improved or new features

- **Improved versions of the UC3823/UC3825 PWMs**
- Compatible with Voltage or Current-Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- 50ns propagation delay to Output
- **High Current Dual Totem Pole Outputs (2A Peak)**
- **Wide Bandwidth Error Amplifier**
- **Trimmed Oscillator Discharge Current for Accurate Frequency & Dead Time Control**
- Fully Latched Logic with Double Pulse Suppression
- Soft Start Control
- **Pulse by Pulse Current Limiting Comparator**
- **Latched Over-Current Comparator With Full Cycle Restart**
- **Low Start Up Current — 100uA typ.**
- **Under Voltage Lock Out — 16V/10V On & Off ("B" versions)**
- **Outputs Active Low During UVLO**
- **Trimmed Bandgap Reference**
- **Adjustable Blanking For Leading Edge Noise Tolerance**

DESCRIPTION

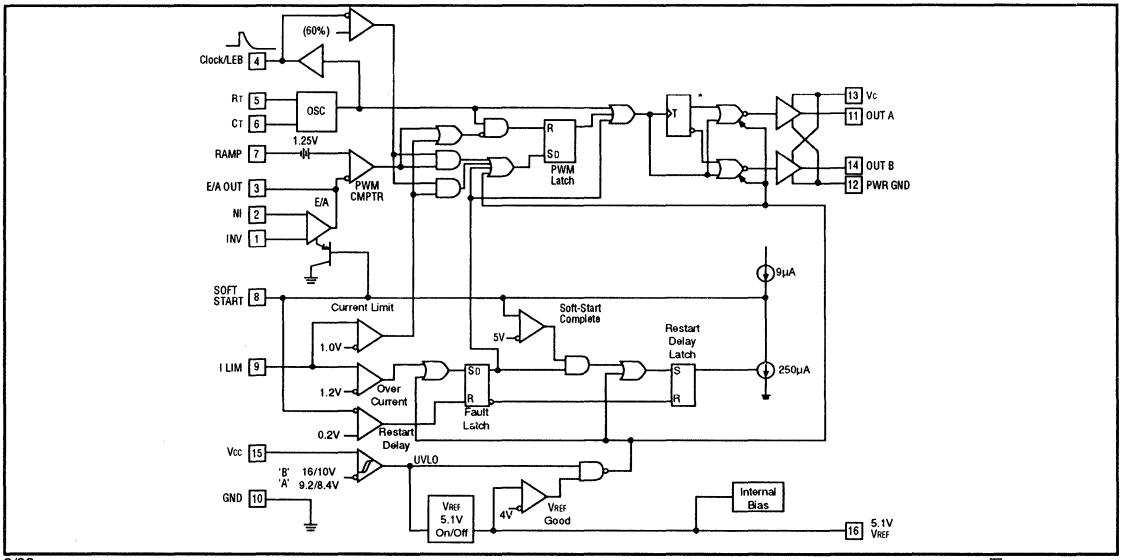
The UC3823A & B and the UC3825A & B family of PWM control ICs are improved versions of the standard UC3823 & UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12MHz while input offset voltage is 2mV. Current limit threshold is guaranteed to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Start up supply current, typically 100uA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the start up current specification. In addition each output is capable of 2A peak currents during transitions.

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed over-current comparator with a threshold of 1.2V. The over-current comparator sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 Clock pin has become Clk/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A,B has dual alternating outputs and the same pin configuration of the UC3825. The UC3823A,B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the '23A,B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823/25. The "B" versions have UVLO thresholds of 16 and 10V, intended for ease of use in off-line applications.

Consult Application Note U-128 for detailed technical and applications information. Contact the factory for further packaging and availability information.

Device	UVLO (V)	D(MAX)
UC3823A	9.2/8.4	< 100%
UC3823B	16/10	< 100%
UC3825A	9.2/8.4	< 50%
UC3825B	16/10	< 50%



6/93

*** Note:** 1823A,B Version Toggles Q and $\overline{Q}$ are always low

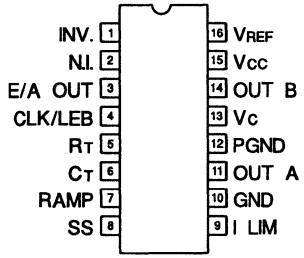
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 22V
Output Current, Source or Sink (Pins 11-14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground (Pin 12) ..... +/-0.2V
Analog Inputs
(Pins 1,2,7) ..... -0.3V to 7V
(Pin 9, 8) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error-Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation at T_A=60°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C

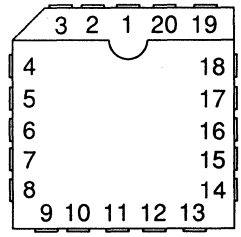
Note: All voltages are with respect to ground Pin 10
Currents are positive into the specified terminal.
Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

TOP VIEW
DIL-16 J or N Package; SOIC-16, DW Package



TOP VIEW
PLCC-20, LCC-20 Q&L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv.	2
N.I.	3
E/A Out	4
CIk/LEB	5
N/C	6
RT	7
CT	8
Ramp	9
SS	10
N/C	11
I LIM	12
GND	13
Out A	14
PGND	15
N/C	16
Vc	17
Out B	18
Vcc	19
VREF	20

Electrical Characteristics: Unless otherwise specified, these specifications apply for R_T = 3.65k, C_T = 1nF, Vcc = 12V, and -55° <T_A<125°C for the UC18xxX, -40°<T_A<85°C for the UC28xxX, 0° <T_A<70°C for the UC38xxX. T_J=T_A.

PARAMETER	TEST CONDITION	MIN	TYPE	MAX	UNITS
REFERENCE SECTION					
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.1	5.15	V
Line Regulation	12<Vcc<20V		2	15	mV
Load Regulation	1<Io<10mA		5	20	mV
Total Output Variation	Line, Load, Temp	5.03		5.17	V
Temperature Stability	T_{MIN}<T_A<T_{MAX}, (Note 1)		0.2	0.4	mV/°C
Output Noise Voltage	10Hz<f<10kHz, (Note 1)		50		µVRMS
Long Term Stability	T_J = 125°C, 1000 hours, (Note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	30	60	90	mA
OSCILLATOR SECTION					
Initial Accuracy	T_J = 25°C, (Note 1)	375	400	425	kHz
Total Variation	Line, Temp, (Note 1)	350		450	kHz
Voltage Stability	12<Vcc<20V			1	%
Temperature Stability	T_{MIN}<T_A<T_{MAX}, (Note 1)		5		%
Initial Accuracy	R_T = 6.6k, C_T = 220pF, T_A = 25°C, (Note 1)	0.9	1	1.1	MHz
Total Variation	R_T = 6.6k, C_T = 220pF, (Note 1)	0.85		1.15	MHz

Electrical Characteristics (Continued) Unless otherwise specified, these specifications apply for R_T = 3.65k, C_T = 1nF, Vcc = 12V, and -55° <T_A<125°C for the UC18xxX, -40°<T_A<85°C for the UC28xxX, 0° <T_A<70°C for the UC38xxX. T_J=T_A.

PARAMETER	TEST CONDITION	MIN	TYPE	MAX	UNITS
OSCILLATOR SECTION (CONTINUED)					
Clock Out High		3.7	4		V
Clock Out Low			0	0.2	V
Ramp Peak		2.6	2.8	3	V
Ramp Valley		0.7	1	1.25	V
Ramp Valley to Peak		1.6	1.8	2	V
Osc Discharge Current	R_T = open, V(C_T) = 2V	9	10	11	mA
ERROR AMPLIFIER SECTION					
Input Offset Voltage			2	10	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1<Vo<4V	60	95		dB
CMRR	1.5<V_{CM}<5.5V	75	95		dB
PSRR	12<V_{CC}<20V	85	110		dB
Output Sink Current	Vpin3 = 1V	1	2.5		mA
Output Source Current	Vpin3 = 4V	-0.5	-1.3		mA
Output High Voltage	I pin3 = -0.5mA	4.5	4.7	5	V
Output Low Voltage	I pin3 = 1mA	0	0.5	1	V
Gain Bandwidth Product	F = 200KHz	6	12		MHz
Slew Rate	(Note 1)	6	9		V/µs
PWM COMPARATOR SECTION					
Pin 7 Bias current	Vpin7 = 0V		-1	-8	µA
Minimum Duty Cycle				0	%
Maximum Duty Cycle		85			%
Leading Edge Blanking	R = 2k, C = 470pF	300	375	450	ns
LEB Resistor	Vpin4 = 3V	8.5	10	11.5	kohm
Pin 3 Zero D.C. Threshold	Vpin7 = 0V	1.1	1.25	1.4	V
Delay to Output *	Vpin3 = 2.1V, Vpin7 = 0 to 2V step, (Note 1)		50	80	ns
CURRENT LIMIT / START SEQUENCE / FAULT SECTION					
Soft Start Charge Current	Vpin8 = 2.5V	8	14	20	µA
Full Soft Start Threshold		4.3	5		V
Restart Discharge Current	Vpin8 = 2.5V	100	250	350	µA
Restart Threshold			0.3	0.5	V
Pin 9 Bias Current	0<Vpin9<2V			15	µA
Current Limit Threshold		0.95	1	1.05	V
Over Current Threshold		1.14	1.2	1.26	V
I LIM Delay to Output	Vpin9 = 0 to 2V step, (Note 1)		50	80	ns
OUTPUT SECTION					
Output Low Saturation	I_{OUT} = 20mA		0.25	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Saturation	I_{OUT} = 20mA		1.9	2.9	V
	I_{OUT} = 200mA		2	3	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Rise/Fall Time	C_L = 1nF, (Note 1)		20	45	ns

Electrical Characteristics (Continued): Unless otherwise specified, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 12V, and -55° <T_A<125°C for the UC18xxX, -40°<T_A<85°C for the UC28xxX, 0° <T_A<70°C for the UC38xxX. T_J=T_A.

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
UNDER VOLTAGE LOCKOUT					
Start Threshold	UCX823B and X825B only		16	17	V
Stop Threshold	UCX823B and X825B only	9	10		V
UVLO Hysteresis	UCX823B and X825B only	5	6	7	V
Start Threshold	UCX823A and X825A only	8.4	9.2	9.6	V
UVLO Hysteresis	UCX823A and X825A only	0.4	0.8	1.2	V
SUPPLY CURRENT					
Start Up Current	V_C = V_{CC} = V_{TH}(start) - 0.5V		100	300	µA
I_{CC}			28	36	mA

Note 1: This parameter is guaranteed by design but not 100% tested in production.

APPLICATIONS INFORMATION

OSCILLATOR

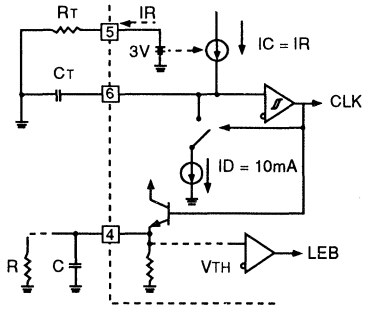
The 3823A,B/3825A,B oscillator is a saw tooth. The rising edge is governed by a current controlled by the R_T pin and value of capacitance at the C_T pin. The falling edge of the sawtooth sets dead time for the outputs. Selection of R_T should be done first, based on desired maximum Duty Cycle. C_T can then be chosen based on desired frequency, R_T, and D_{MAX}. The design Equations are:

$$R_T = \frac{3V}{(10mA)(1 - D_{MAX})}$$

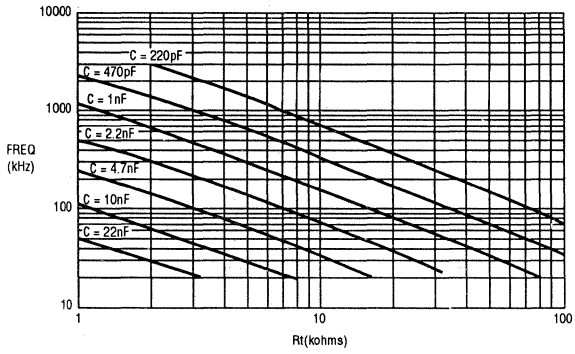
$$C_T = \frac{(1.6 \cdot D_{MAX})}{(R_T \cdot F)}$$

Recommended values for R_T range from 1K to 100K. Control of D_{MAX} less than 70% is not recommended.

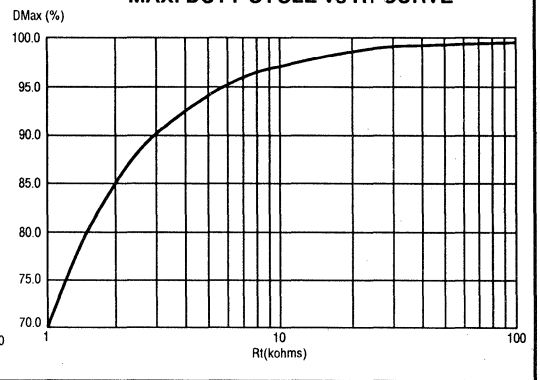
OSCILLATOR



OSC. FREQ vs R_T & C_T CURVE



MAX. DUTY CYCLE vs R_T CURVE



APPLICATIONS INFORMATION (Continued)

LEADING EDGE BLANKING

The UC3823A,B/3825A,B performs fixed frequency pulse width modulation control. The '23A,B outputs operate together at the switching frequency and can vary from 0 to some value less than 100%. The '25A,B outputs are alternately controlled. During every other cycle, one output will be off.Each output, then, switches a one-half oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the over current comparator.

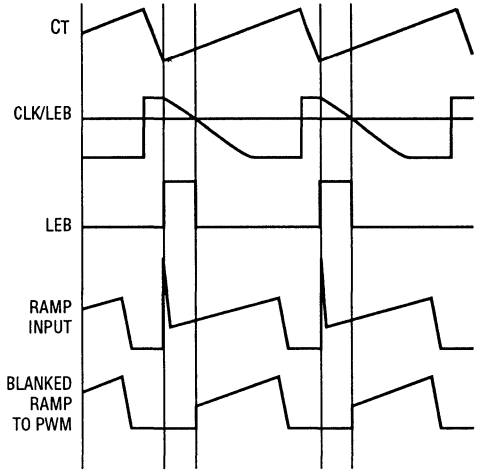
Normally the PWM comparator will sense a ramp crossing a control voltage (error amp output) and terminate the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking. After the LEB interval, the PWM comparator can terminate the pulse.

To program a Leading Edge Blanking period, connect a capacitor, C, to Clk/LEB. The discharge time set by C and the internal 10k resistor will determine the blanked interval. The 10k resistor has a 10% tolerance. For more accuracy, an external 2k 1% resistor, R, can be added, resulting in an equivalent resistance of 1.66k with a tolerance of 2.5% The design equation is:

$$t_{LEB} = 0.5 \cdot (R \,||\, 10k) \cdot C.$$

Values of R less than 2k should not be used.

LEB OPERATIONAL WAVEFORMS



Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the one volt threshold, the pulse is terminated. The over current comparator, however, is not blanked. It will catch catastrophic over current faults without a blanking delay. Any time the I LIM pin exceeds 1.2V, the fault latch will be set and the outputs driven low. For this reason, some noise filtering may be required on the I LIM pin.

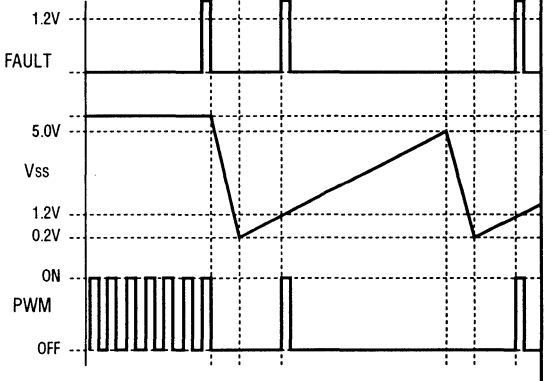
UVLO, SOFT START AND FAULT MANAGEMENT

Soft start is programmed by a capacitor on the SS pin. At power up, the SS pin is discharged. When the SS pin is low, the error amp output is forced to also be low. As the internal 9uA source charges the SS pin, the error amp output follows until closed loop regulation takes over.

Any time that the I LIM pin exceeds 1.2V, the fault latch will be set and the output pins will be driven low. The soft start cap is then discharged by a 250uA current sink. No more output pulses are allowed until soft start is fully discharged, and the I LIM pin is below 1.2V. At this point the fault latch will be reset and the chip will execute a soft start.

Should the fault latch be set during soft start, the outputs will be immediately terminated, but the soft start cap will not be discharged until it has been fully charged. This results in a controlled hiccup interval for continuous fault conditions.

SOFT START AND FAULT WAVEFORMS

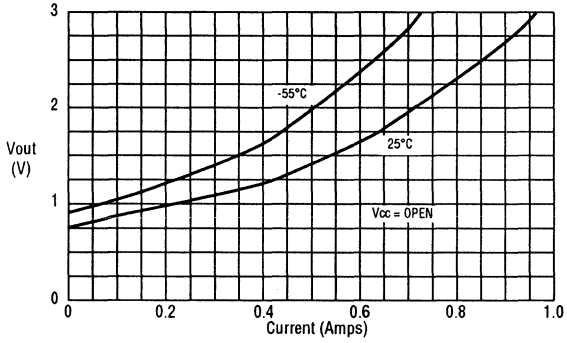


APPLICATIONS INFORMATION (Continued)

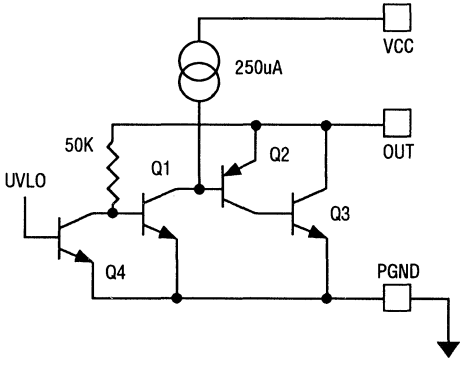
ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both Vcc and Vref before allowing the chip to operate.

OUTPUT V & I DURING UVLO



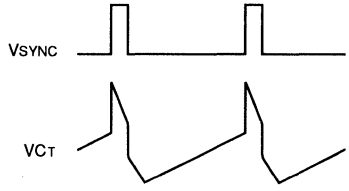
SIMPLIFIED SCHEMATIC



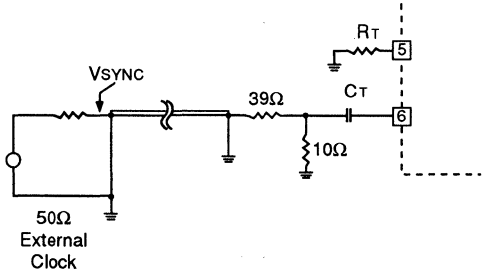
SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10 to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10ns and less than half the discharge time of the oscillator. The rising edge of the Clk/LEB pin can be used to generate a synchronizing pulse for other chips. Note that, the Clk/LEB pin will no longer accept an incoming synchronizing signal.

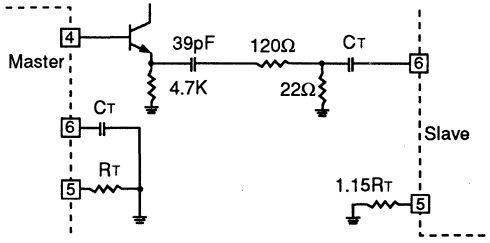
OPERATIONAL WAVEFORMS



GENERAL OSCILLATOR SYNCHRONIZATION



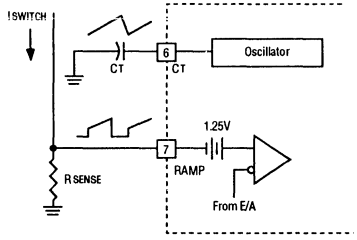
TWO UNITS



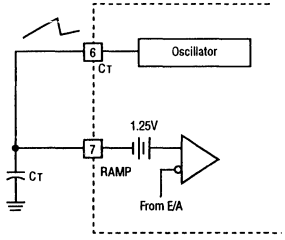
APPLICATIONS INFORMATION (Continued)

PWM APPLICATIONS

CURRENT MODE



VOLTAGE MODE

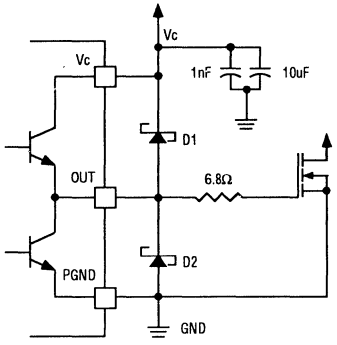


HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A,B and UC3825A,B can deliver a 2 amp peak current into a capacitive load. The output can slew a 1000pF capacitor 15 volts in approximately 20 nanoseconds. Separate collector supply (Vc) and power ground (PGND) pins help decouple the ICs analog circuitry from the high power gate drive noise. The use of 3 Amp SCHOTTKY diodes (1N5120, USD245 or equivalent) as shown in the figure from each output to both Vc and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. SCHOTTKY diodes must be used because a low forward voltage drop is required, and most 3 amp devices will suffice. DO NOT USE standard silicon diodes.

Although a "single ended" device, two output drivers are available on the UC3823A,B devices. These can be "paralleled" through a series one-half ohm (noninductive) resistor for a combined peak current of 4 amps.

POWER MOSFET DRIVE CIRCUIT

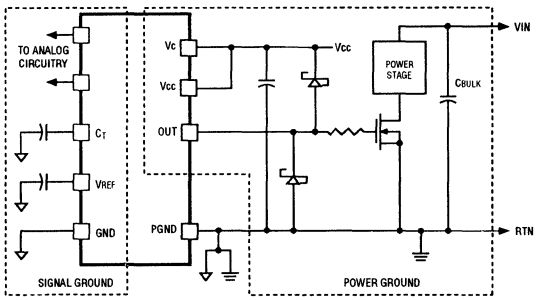


D1, D2, = 1N5820

GROUND PLANES

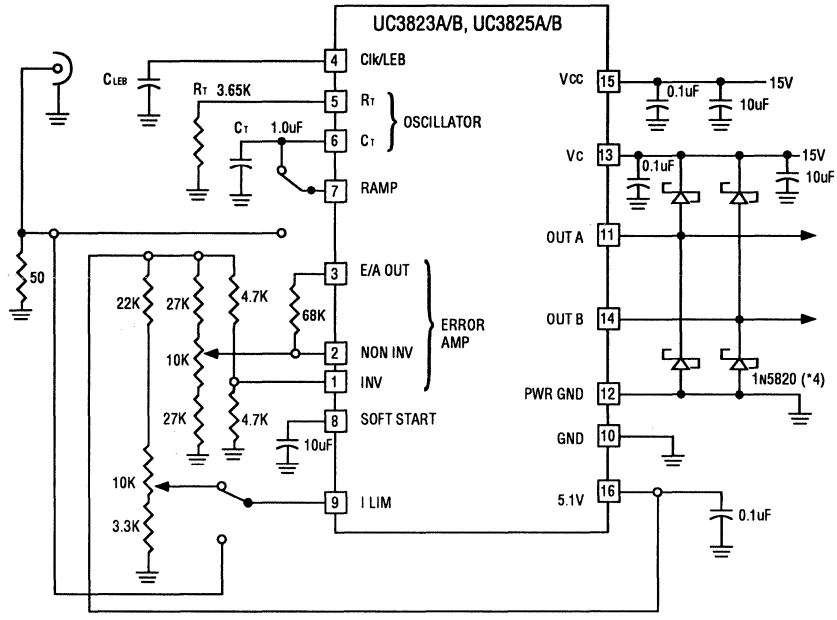
Each output driver of these devices is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. Vcc should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both Vcc and PGND. Nothing else should be connected to power ground.

Vref should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low esr/esl ceramic 1uF capacitors are recommended for both Vcc and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.



APPLICATIONS INFORMATION (Continued)

OPEN LOOP TEST CIRCUIT



This test fixture is useful for exercising many of the UC3823A,B, UC3825A,B functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

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High Speed PWM Controller

FEATURES

- Complimentary Outputs
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V ± 1%)

DESCRIPTION

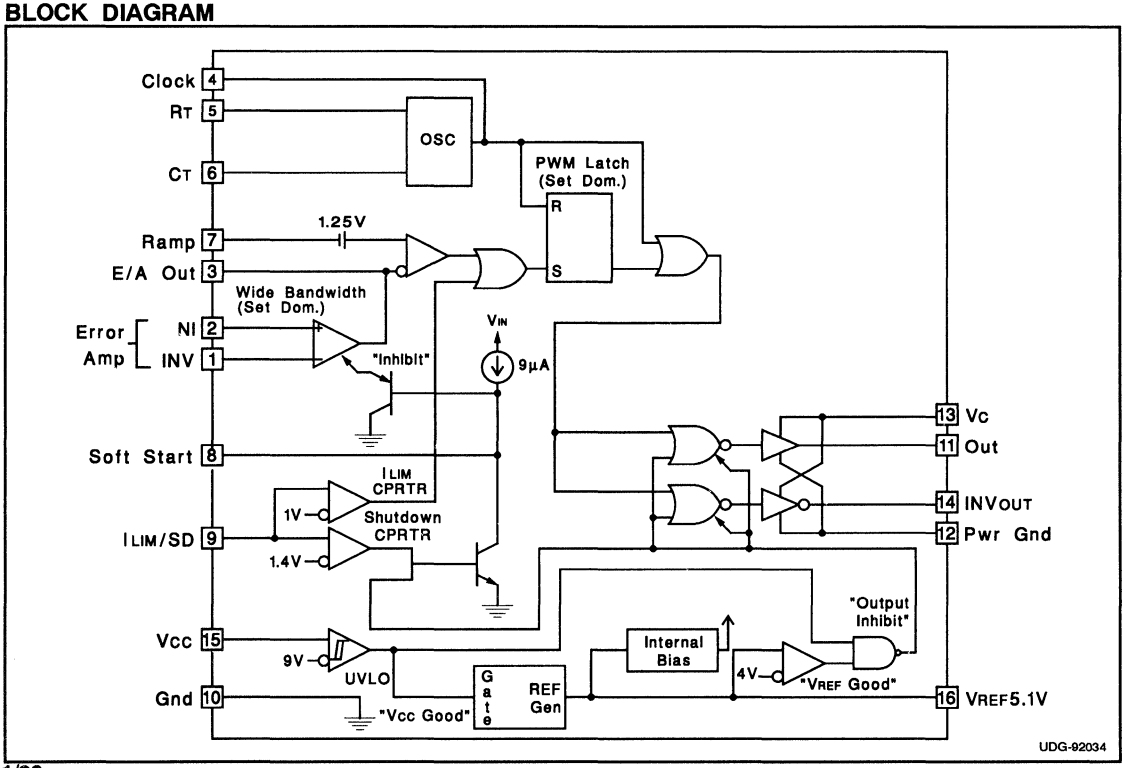
The UC1824 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

5

BLOCK DIAGRAM



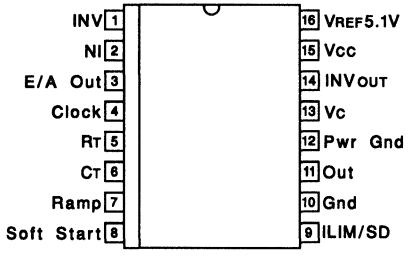
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5ms) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... -0.3V to 7V
(Pin 8, 9) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

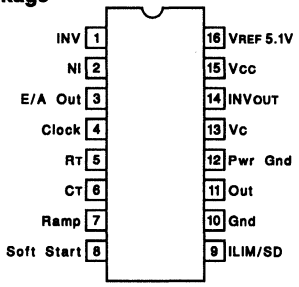
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

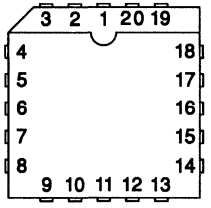


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
Vc	17
INVOUT	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated,these specifications apply for , RT = 3.65k, CT = 1nF, Vcc = 15V, -55°C<TA<125°C for the UC1824, –40°C<TA<85°C for the UC2824, and 0°C<TA<70°C for the UC3824, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	TJ = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1824, –40°C<T_A<85°C for the UC2824, and 0°C<T_A<70°C for the UC3824, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < Vo < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	mA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	Vc = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

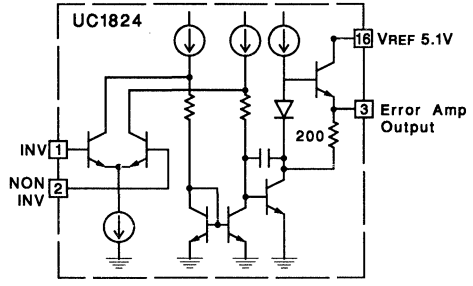
** This parameter not 100% tested in production but guaranteed by design.*

UC1824 Printed Circuit Board Layout Considerations

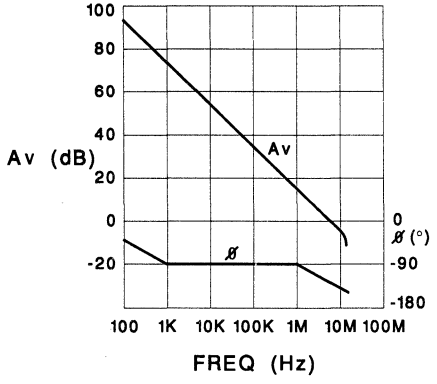
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor of a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

Error Amplifier Circuit

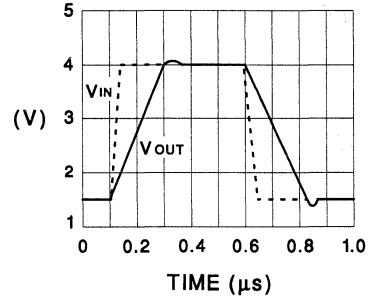
Simplified Schematic



Open Loop Frequency Response

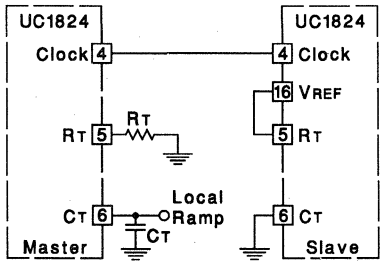


Unity Gain Slew Rate

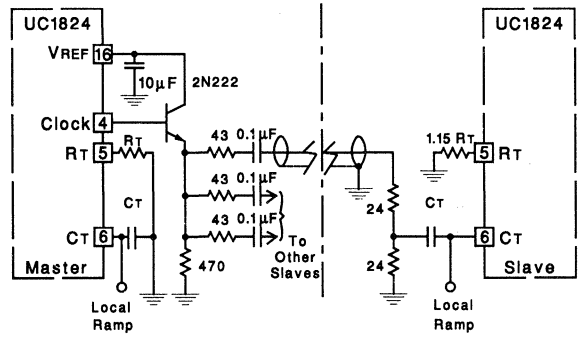


Synchronized Operation

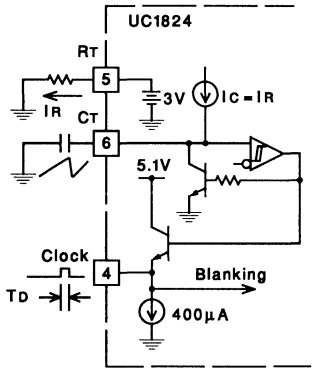
Two Units in Close Proximity



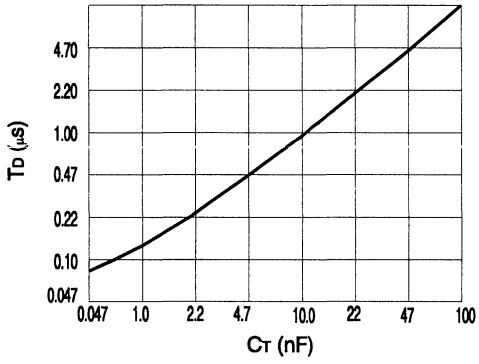
Generalized Synchronization



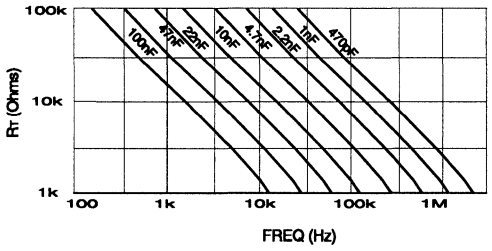
Oscillator Circuit



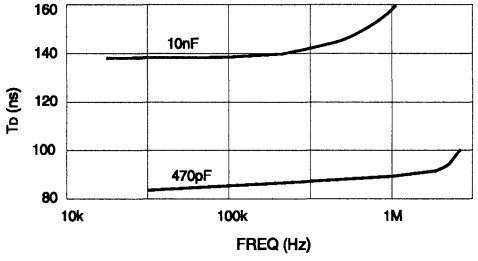
Primary Output Deadtime vs CT (3k ≤ RT ≤ 100k)



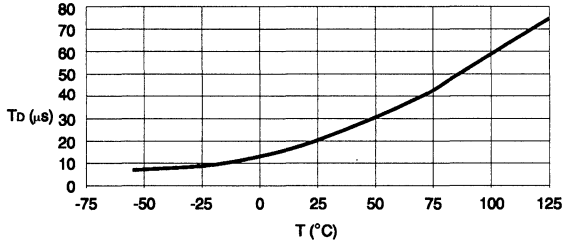
Timing Resistance vs Frequency



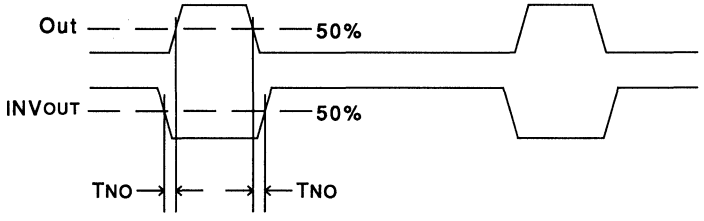
Primary Output Deadtime vs Frequency



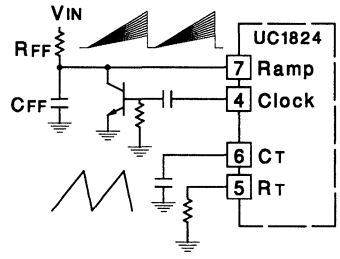
Typical Dead Time (TD) Over Temperature



Non-Overlap Time (TNO) Over Temperature

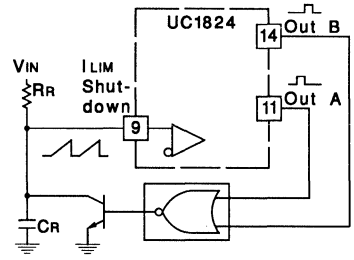


Forward Technique for Off-Line Voltage Mode Application



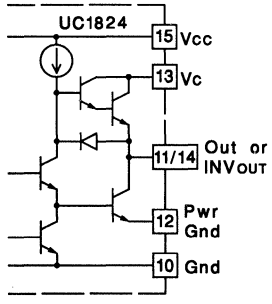
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

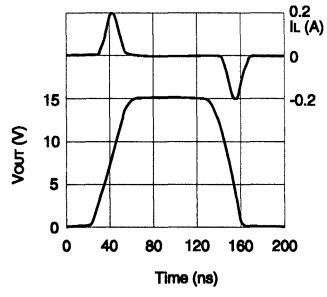


Output Section

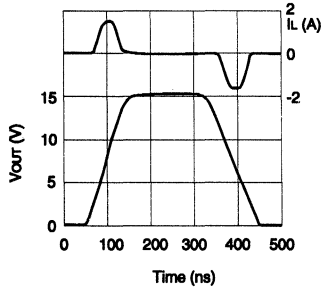
Simplified Schematic



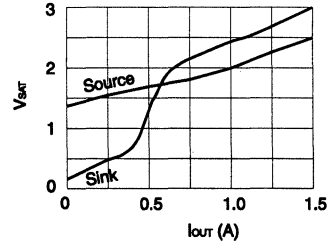
Rise/Fall Time (CL=1nF)



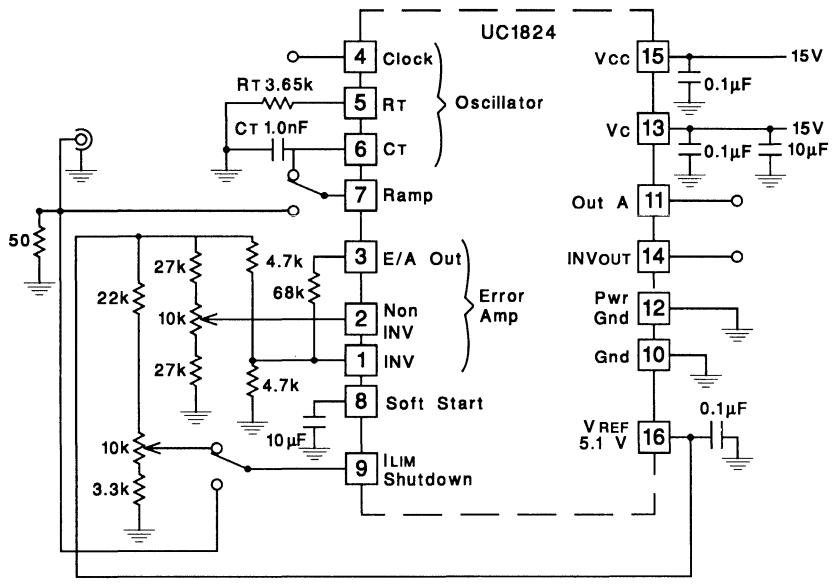
Rise/Fall Time (CL=10nF)



Saturation Curves



Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

5

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INTEGRATED CIRCUITS
UNITRODE

UC1825
UC2825
UC3825

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V ± 1%)

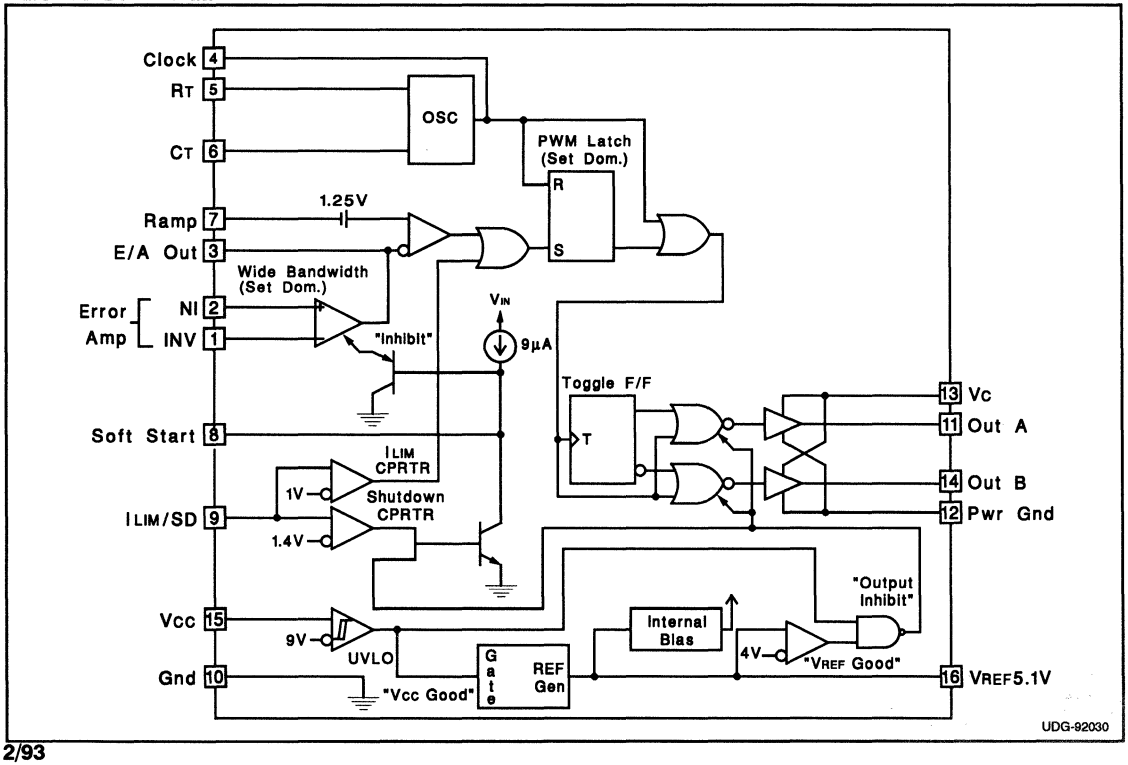
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM

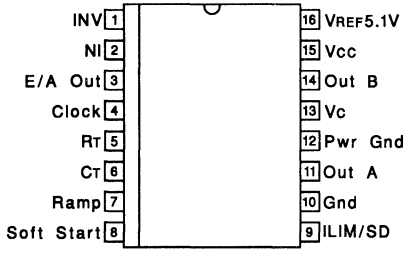


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5ms) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... -0.3V to 7V
(Pin 8, 9) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

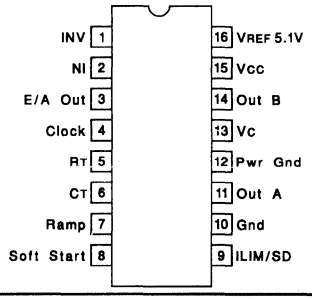
Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

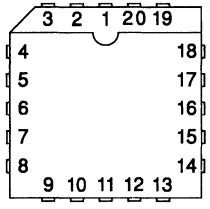


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out A	14
Pwr Gnd	15
N/C	16
Vc	17
Out B	18
Vcc	19
VREF 5.1V	20

5

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated,these specifications apply for , RT = 3.65k, CT = 1nF, Vcc = 15V, -55°C<TA<125°C for the UC1825, –40°C<TA<85°C for the UC2825, and 0°C<TA<70°C for the UC3825, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	TJ = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

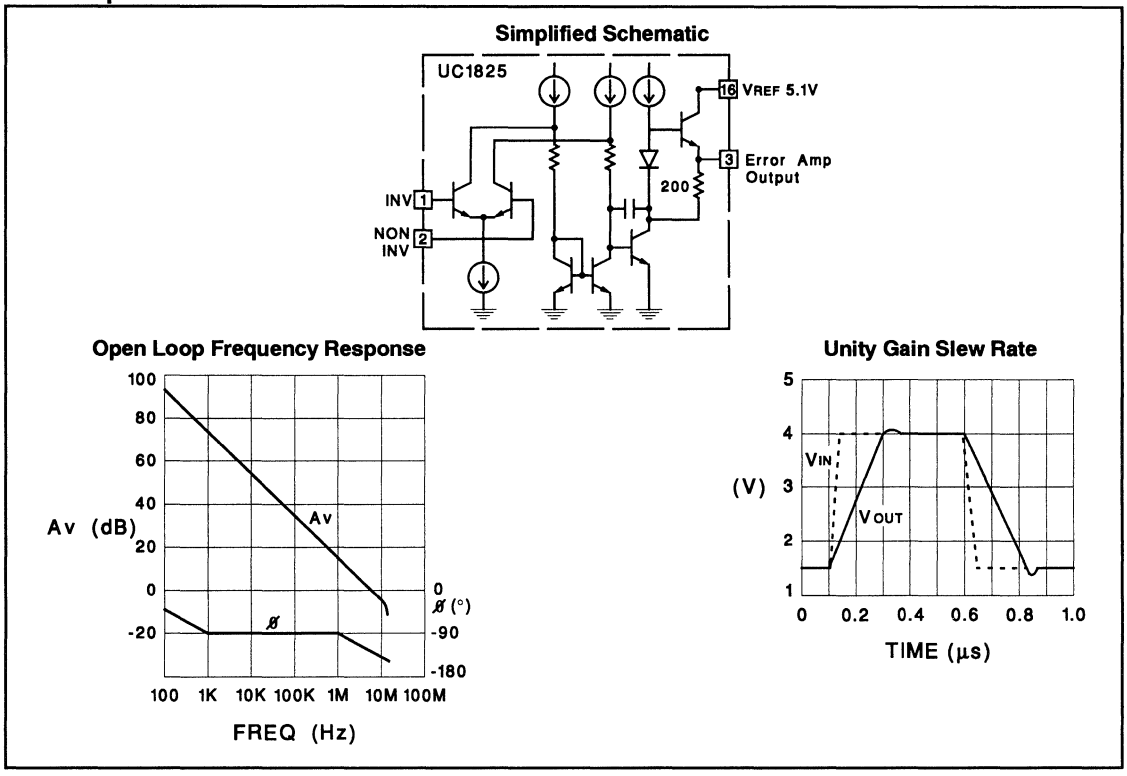
PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	mA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

** This parameter not 100% tested in production but guaranteed by design.*

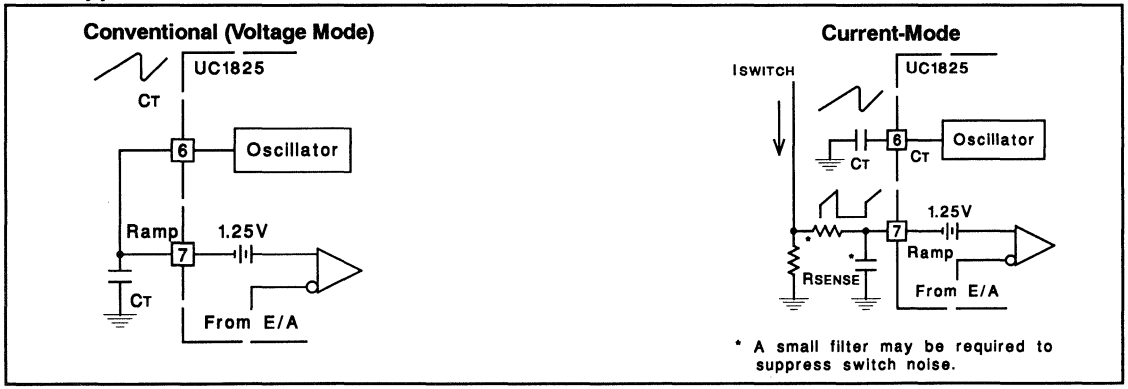
Printed Circuit Board Layout Considerations

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor of a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass Vcc, Vc, and VREF. Use 0.1μF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

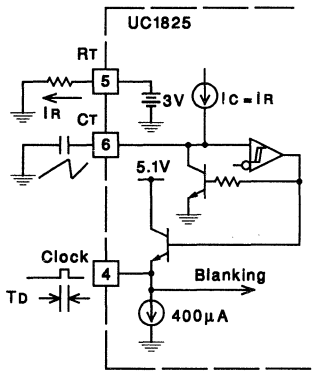
Error Amplifier Circuit

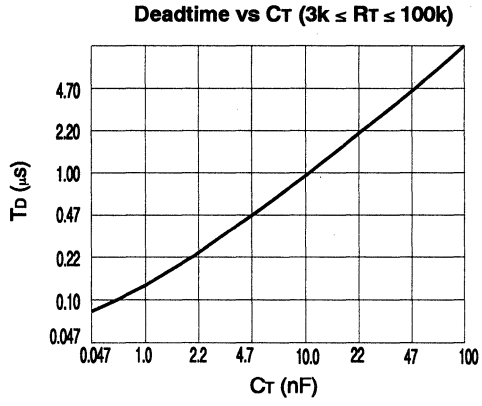


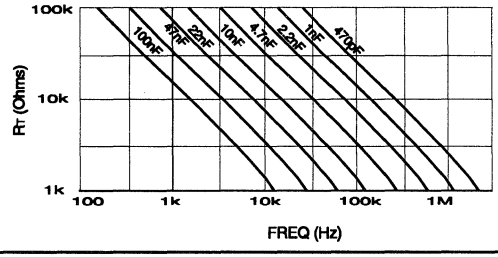
PWM Applications

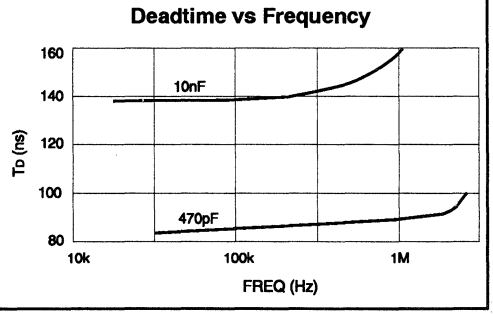


Oscillator Circuit



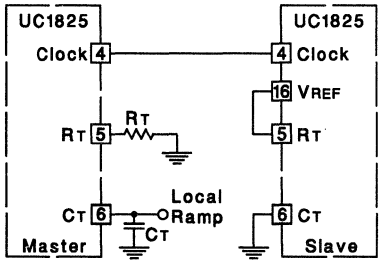




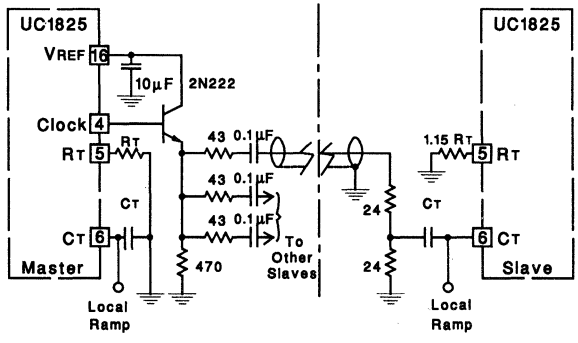


Synchronized Operation

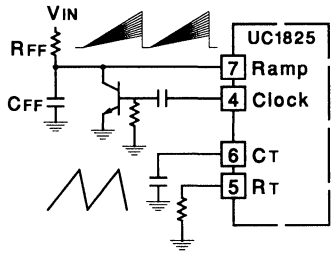
Two Units in Close Proximity



Generalized Synchronization

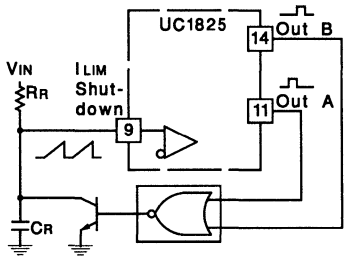


Forward Technique for Off-Line Voltage Mode Application



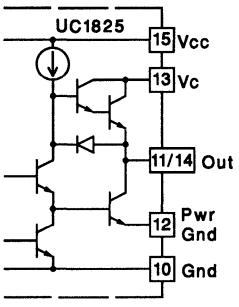
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

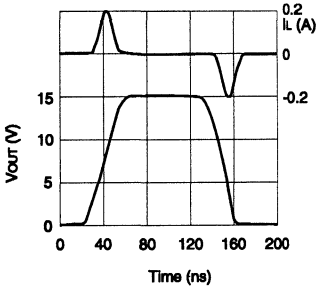


Output Section

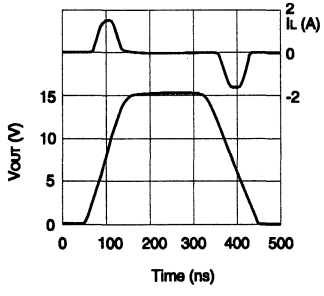
Simplified Schematic



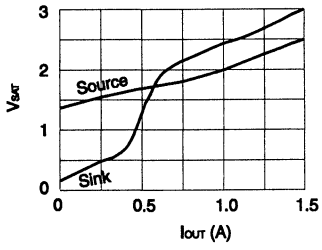
Rise/Fall Time (CL=1nF)



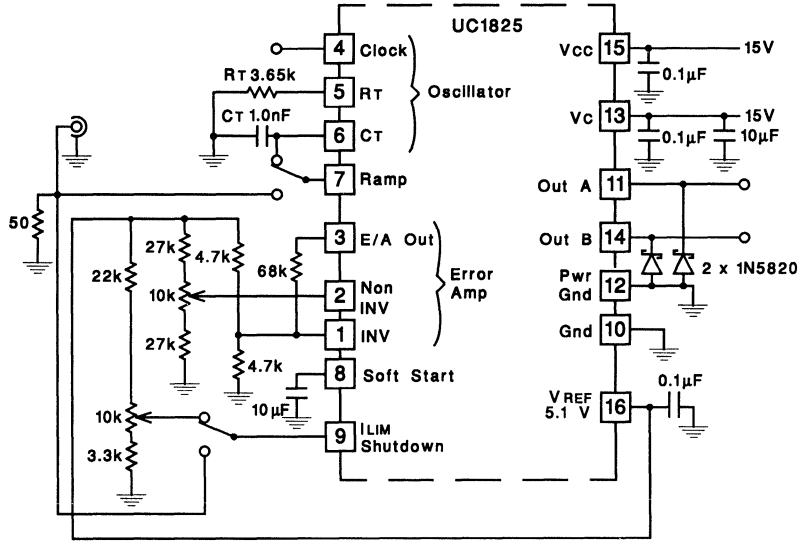
Rise/Fall Time (CL=10nF)



Saturation Curves



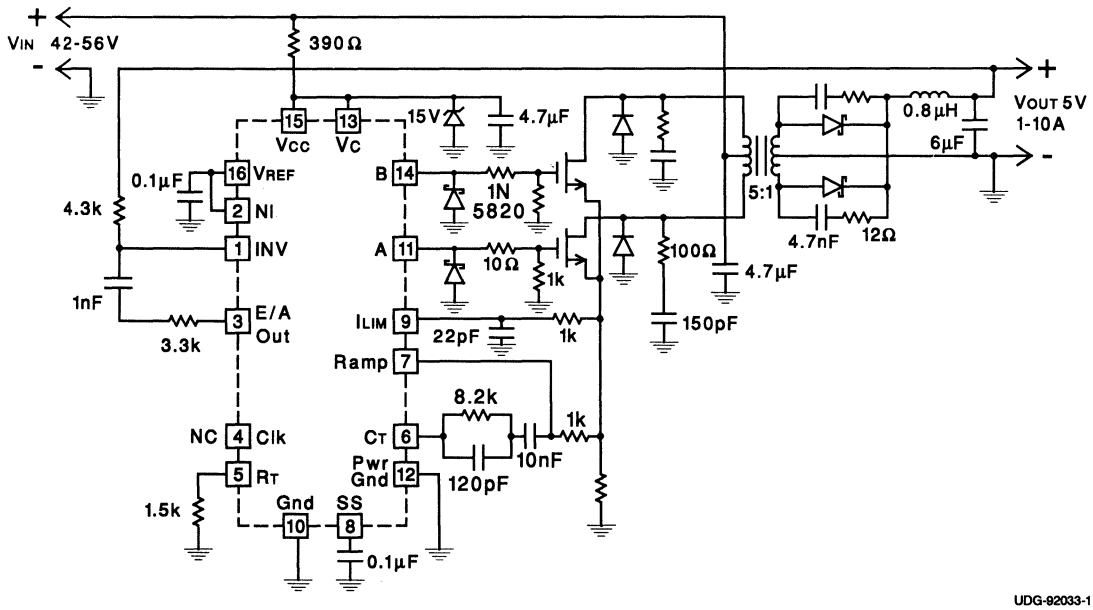
Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

Design Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency



UNITRODE INTEGRATED CIRCUITS
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TEL. (603) 424-2410 • FAX (603) 424-3460

UC1828
UC2828
UC3828

ADVANCED INFORMATION

Current Mode PWM Controller IC

FEATURES

- Wide Operating Range
- Programmable Triangle Wave Generator
- Low ISENSE Delay
- Low Start-up Current
- Built-in Programmable Blanking
- Latched Shutdown Pin
- Programmable Start-up Threshold with Default Setting
- Fully Synchronizing Oscillator
- Soft-Start Capability
- Open-collector Totem Pole Output can Drive High-Side Switch

DESCRIPTION

The UC1828 family of PWM controller ICs builds on the features offered in the UC1842 family. This new family has improved speed and accuracy, added functionality, and lower power requirements.

The oscillator is programmed by the user's selection of external resistors and a capacitor. One resistor accurately sets the charge current in the capacitor, while the other accurately sets the discharge current. This allows highly accurate frequency and duty cycle programming.

The S/D Latch pin, when given a high positive input command, will latch the output off until reset by the Enable pin. The S/D Latch function is designed to operate with very low delay times.

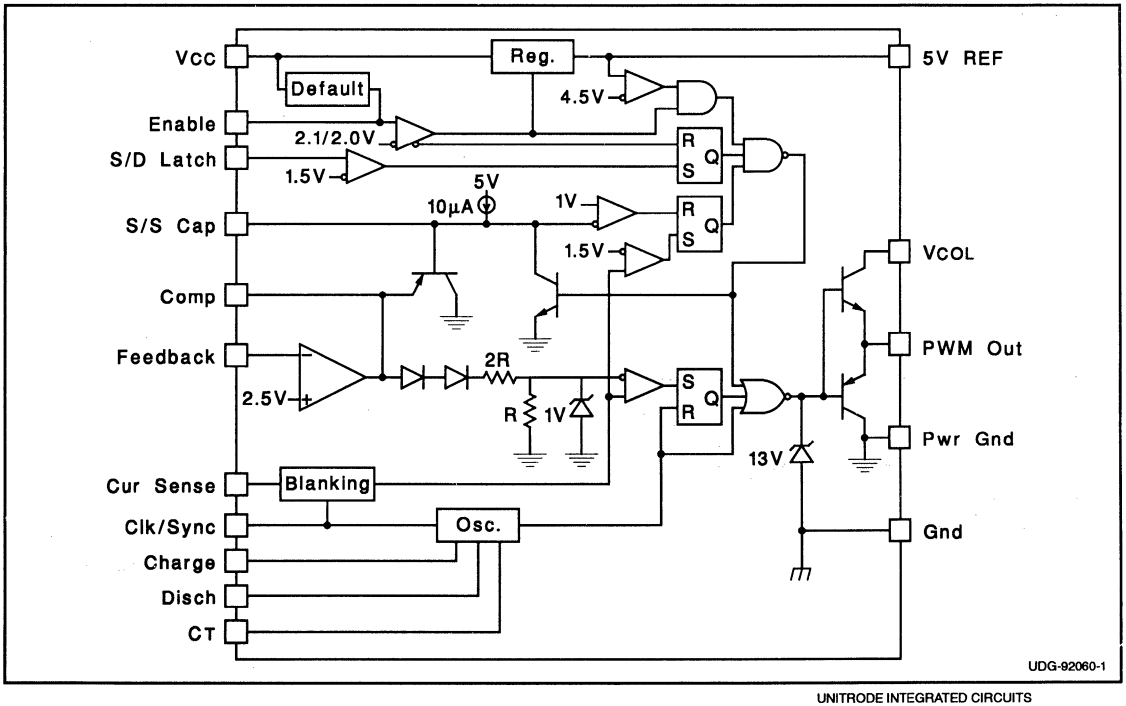
The Enable pin, when given a high positive input command, will reset the flip-flop set by the S/D Latch pin. If the Enable pin is connected directly to Vcc, the device will default to the settings of the internal UVLO circuitry.

The S/S Cap pin is used for programming soft-start capability. The user simply applies a small capacitor to this pin to set the soft start function. Each time the device is forced into a current-fault situation, it will go through a full soft start cycle, thus preventing current runaway.

The Clk/Sync pin can be used to easily synchronize two UC1828 devices to the same frequency.

5

BLOCK DIAGRAM



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INTEGRATED CIRCUITS
UNITRODE

UC1832/3
UC2832/3
UC3832/3

Precision Low Dropout Linear Controllers

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5V to 36V Operation
- 100mA Output Drive, Source or Sink
- Under-Voltage Lockout

Additional Features of the UC1832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate +VIN terminal
- Programmable Driver Current Limit
- Access to V_{REF} and E/A(+)
- Logic-Level Disable Input

DESCRIPTION

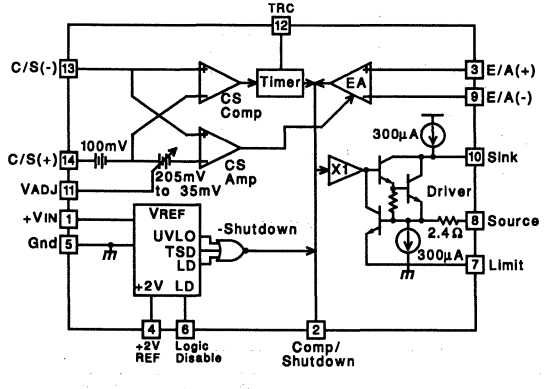
The UC1832 and UC1833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

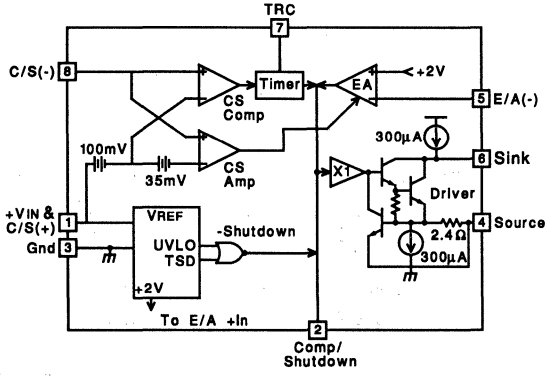
The UC1833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC1832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); industrial (–25°C to 85°C), order UC2832/3 (N or J); and military (–55°C to 125°C), order UC1832/3J. Surface mount packaging is also available.

BLOCK DIAGRAMS

UCx832



UCx833



UDG-92040

ABSOLUTE MAXIMUM RATINGS

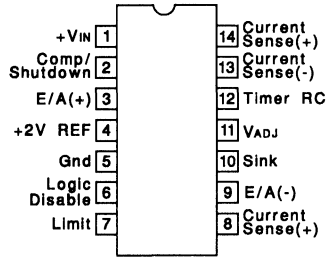
Supply Voltage +VIN 40V
Driver Output Current (Sink or Source) 450mA
Driver Sink to Source Voltage 40V
TRC Pin Voltage ..... –0.3V to 3.2V
Other Input Voltages ..... –0.3V to +VIN
Operating Junction Temperature (note 2) ... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

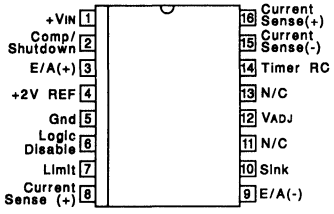
CONNECTION DIAGRAMS

UC1832

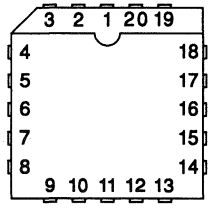
DIL-14 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



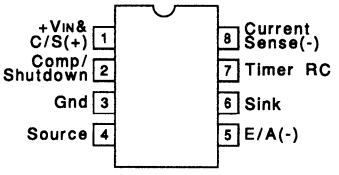
LCC-20 & PLCC-20
L & Q Package
(Top View)



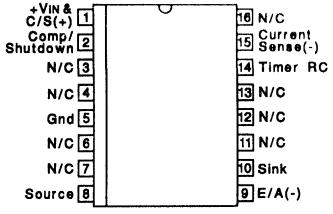
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
Comp/Shutdown	3
E/A(+)	4
+2V REF	5
N/C	6
Gnd	7
Logic Disable	8
Limit	9
Current Sense(+)	10
N/C	11
E/A(-)	12
Sink	13
VADJ	14
N/C	15-17
Timer RC	18
Current Sense(-)	19
Current Sense(+)	20

UC1833

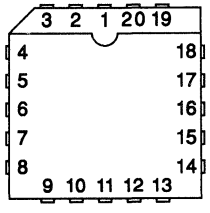
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



LCC-20 & PLCC-20
L & Q Package
(Top View)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN & C/S(+)	1
N/C	2
N/C	3
N/C	4
Comp/Shutdown	5
Gnd	6
N/C	7
N/C	8
N/C	9
Source	10
N/C	11
E/A(-)	12
N/C	13
N/C	14
Sink	15
Timer RC	16
Current Sense(+)	17
N/C	18-20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, $+V_{IN}$ = 15V, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 6V		6.5	10	mA
	$+V_{IN}$ = 36V		9.5	15	mA
	Logic Disable = 2V (UCx832 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	T_J = 25°C, I_{DRIVER} = 10mA	1.98	2.00	2.02	V
	over temperature, I_{DRIVER} = 10mA	1.96	2.00	2.04	V
Load Regulation (UCx832 only)	I_{OUT} = 0 to 10mA	-10	-5.0		mV
Line Regulation	$+V_{IN}$ = 4.5 to 36V, I_{DRIVER} = 10mA		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCx832 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Pin 6 = 0V	-5.0	-1.0		µA
Current Sense Section					
Comparator Offset		95	100	105	mV
	Over Temperature	93	100	107	mV
Amplifier Offset (UCx833 only)		110	135	170	mV
Amplifier Offset (UCx832 only)	V_{ADJ} = Open	110	135	170	mV
	V_{ADJ} = 1V	180	235	290	mV
	V_{ADJ} = 0V	250	305	360	mV
Input Bias Current	V_{CM} = $+V_{IN}$	65	100	135	µA
Input Offset Current (UCx832 only)	V_{CM} = $+V_{IN}$	-10		10	µA
Amplifier CMRR (UCx832 only)	V_{CM} = 4.1V to $+V_{IN}$+0.3V		80		dB
Transconductance	I_{COMP} = ±100µA		65		mS
V_{ADJ} Input Current (UCx832 only)	V_{ADJ} = 0V	-10	-1		µA
Timer					
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2V		0.25	1.0	µA
Active Pullup Current	C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN}$ - 0.4V; TRC pin = 0V	-345	-270	-175	µA
Duty Ratio (note 4)	ontime/period, R_T = 200k, C_T = .27µF		4.8		%
Period (notes 4,5)	ontime + offtime, R_T = 200k, C_T = .27µF		36		ms
Upper Trip Threshold (Vu)			1.8		V
Lower Trip Threshold (Vl)			0.9		V
Trip Threshold Ratio	Vu/Vl		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCx832 only)	V_{CM} = V_{COMP} = 2V	-8.0		8.0	mV
Input Bias Current	V_{CM} = V_{COMP} = 2V	-4.5	-1.1		µA
Input Offset Current (UCx832 only)	V_{CM} = V_{COMP} = 2V	-1.5		1.5	µA
AVOL	V_{COMP} = 1V to 13V	50	70		dB
CMRR (UCx832 only)	V_{CM} = 0V to $+V_{IN}$ - 3V	60	80		dB
PSRR (UCx832 only)	V_{CM} = 2V, $+V_{IN}$ = 4.5 to 36V		90		dB
Transconductance	I_{COMP} = ±10µA		4.3		mS
VOH	I_{COMP} = 0, Volts below $+V_{IN}$		.95	1.3	V
VOL	I_{COMP} = 0		.45	0.7	V
IOH	V_{COMP} = 2V	-700	-500	-100	µA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, $+V_{IN}$ = 15V, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (cont.)					
IOL	V_{COMP} = 2V, C/S(-) = $+V_{IN}$	100	500	700	µA
	V_{COMP} = 2V, C/S(-) = $+V_{IN}$ - 0.4V	2	6		mA
Driver					
Maximum Current	Driver Limit & Source pins common; T_J = 25°C	200	300	400	mA
	Over Temperature	100	300	450	mA
Limiting Voltage	Driver Limit to Source voltage at current limit, I_{SOURCE} = -10mA; T_J = 25°C (Note 6)		.72		V
Internal Current Sense Resistance	T_J = 25°C (Note 6)		2.4		Ω
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.4V; Driver Sink = $+V_{IN}$ - 1V	-800	-300	-100	µA
	Compensation/Shutdown = 0.4V, $+V_{IN}$ = 36V; Driver Sink = 35V	-1000	-300	-75	mA
Pull-Down Current at Driver Source	Compensation/Shutdown = 0.4V; Driver Source = 1V	150	300	700	µA
Saturation Voltage Sink to Source	Driver Source = 0V; Driver Current = 100mA		1.5		V
Maximum Source Voltage	Driver Sink = $+V_{IN}$, Driver Current = 100mA Volts below $+V_{IN}$		3.0		V
UVLO Sink Leakage	$+V_{IN}$ = C/S(+) = C/S(-) = 2.5V, Driver Sink = 15V, Driver Source = 0V, TA = 25°C		25		µA
Maximum Reverse Source Voltage	Compensation/Shutdown = 0V; I_{SOURCE} = 100µA, $+V_{IN}$ = 3V		1.6		V
Thermal Shutdown			160		°C

Note 3: On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving V_{SOURCE} to 2V.

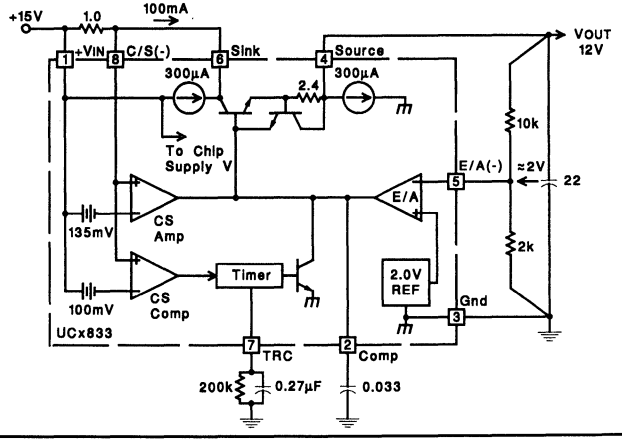
Note 4: These parameters are first-order supply-independent, however both may vary with supply for $+V_{IN}$ less than about 4V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

Note 5: With recommended R_T value of 200k, $T_{OFF} \approx R_T C_T * \ln(V_u/V_l)$ ±10%.

Note 6: The internal current limiting voltage has a temperature dependence of approximately -2.0mV/°C, or -2800ppm/°C. The internal 2.4 Ω sense resistor has a temperature dependance of approximately +1500ppm/°C.

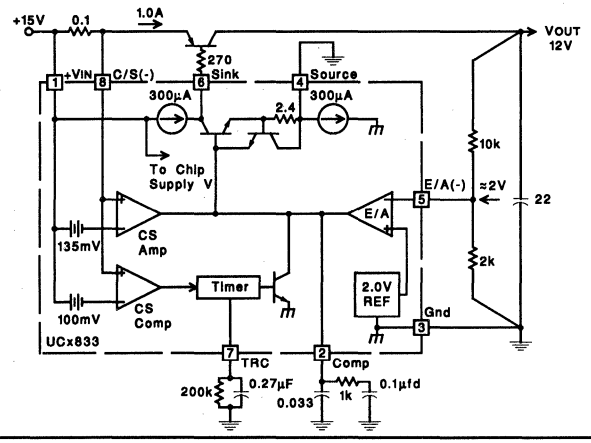
APPLICATION AND OPERATION INFORMATION

NPN Pass (Local 100mA Regulator) (UCx833)



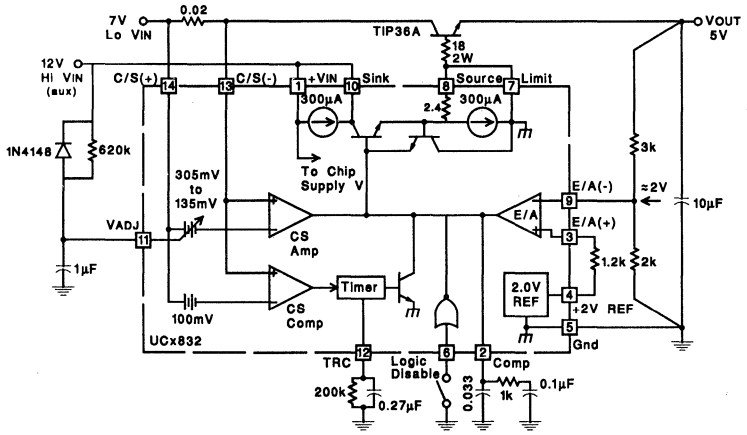
APPLICATION AND OPERATION INFORMATION (cont.)

PNP Pass (Low Drop-Out Regulator) (UCx833)



UDG-92042

NPN Pass (Medium Power, Low Drop-Out Regulator) (UCx832)



UDG-92043

Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current,

and $$K = \frac{Current\ Sense\ Amplifier Offset\ Voltage}{100mA}$$

≈1.35 for UCx833, and is variable from 1.35 to 3.05 with V_{ADJ} for the UCx832.

For a worst-case constant-current load of value just less than I_{TH}, C_{MAX} can be estimated from:

$$C_{MAX} = ((K-1)I_{TH})\left(\frac{T_{ON}}{V_{OUT}}\right),$$

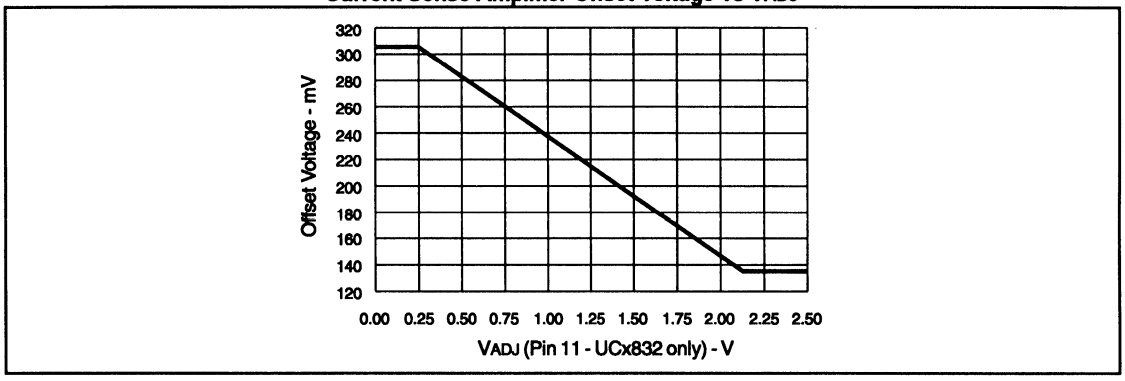
where V_{OUT} is the nominal regulator output voltage.

For a resistive load of value R_L, the value of C_{MAX} can be estimated from:

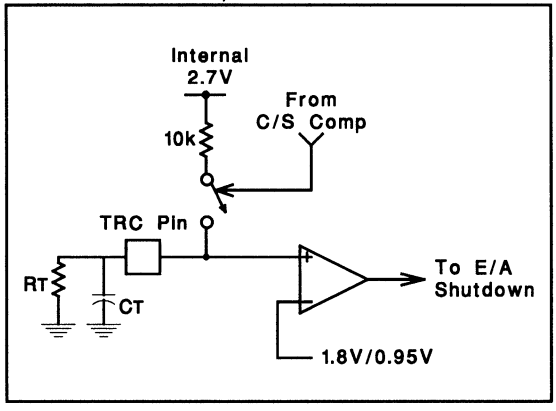
$$C_{MAX} = \frac{T_{ON}}{R_L} \bullet \frac{1}{ln\left[\left(1-\frac{V_{OUT}}{K \bullet I_{TH} \bullet R_L}\right)^{-1}\right]}.$$

APPLICATION AND OPERATION INFORMATION (cont.)

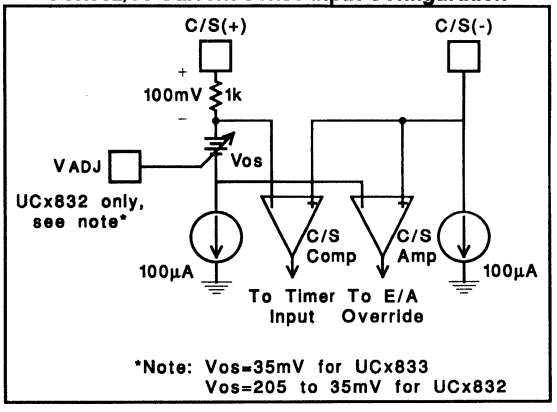
Current Sense Amplifier Offset Voltage vs VADJ



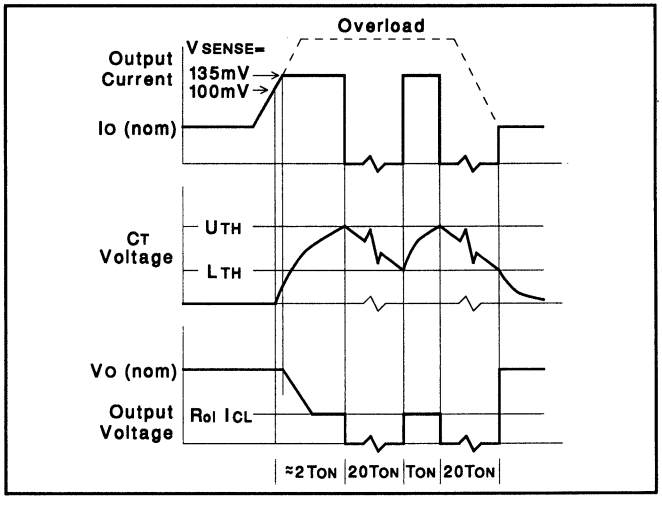
UCx832/33 Timer Function



UCx832/33 Current Sense Input Configuration



Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

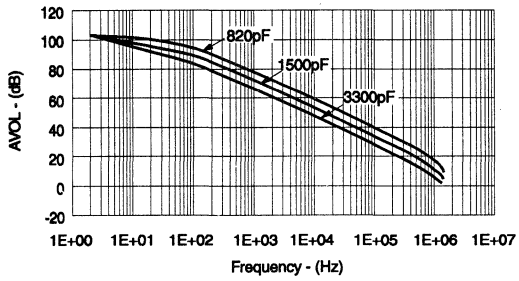


5

APPLICATION AND OPERATION INFORMATION (cont.)

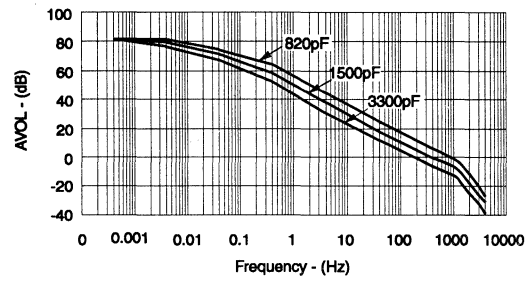
UCx832 Error Amplifier

AVOL vs Frequency and Cc



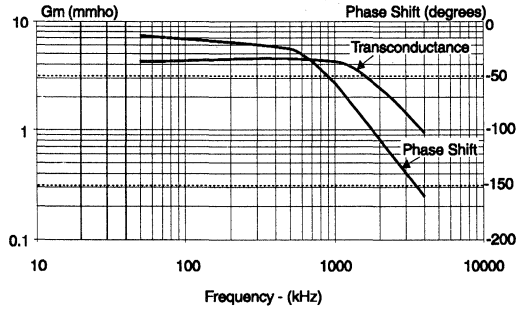
UCx832 Current Sense Amplifier

AVOL vs Frequency and Cc



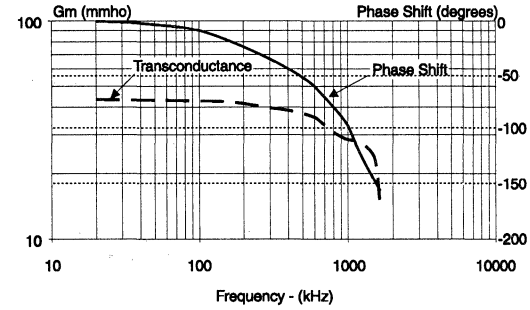
UCx832 Error Amplifier

Transconductance and Phase vs Frequency



UCx832 Current Sense Amplifier

Transconductance and Phase vs Frequency



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High Efficiency Linear Regulator

FEATURES

- Minimum VIN - VOUT Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

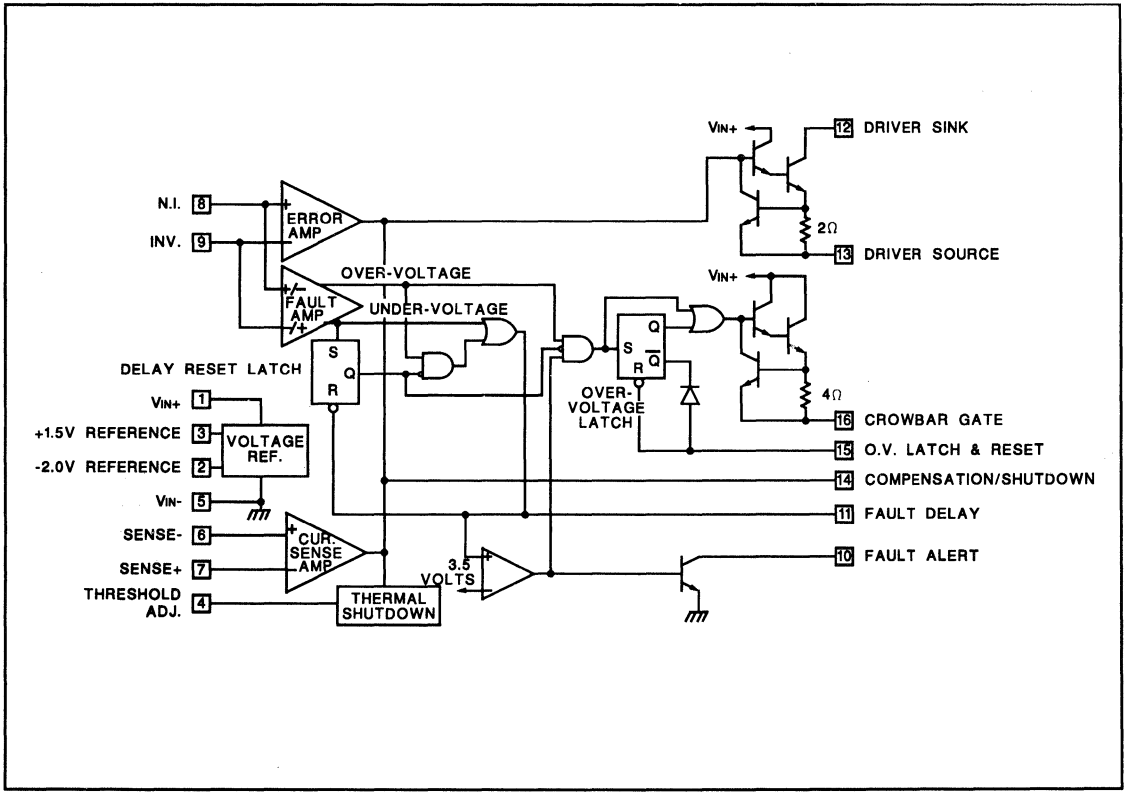
DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

5

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

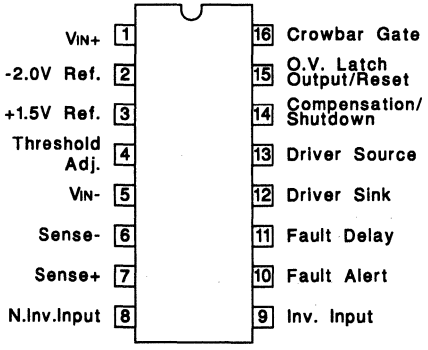
Input Supply Voltage, V_{IN} + ... 40V
Driver Current 400mA
Driver Source to Sink Voltage 40V
Crowbar Current ..... -200mA
+1.5V Reference Output Current ..... -10mA
Fault Alert Voltage 40V
Fault Alert Current 15mA
Error Amplifier Inputs ..... -0.5V to 35V
Current Sense Inputs ..... -0.5V to 40V
O.V. Latch Output Voltage ..... -0.5V to 40V
O.V. Latch Output Current 15mA

Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at Tc = 25°C 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

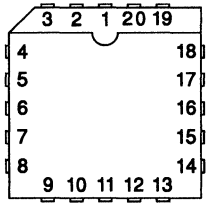
Note 1: Voltages are reference to V_{IN}-, Pin 5.
Currents are positive into, negative out of the specified terminals.
Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
V_{IN} +	2
-2.0V REF	3
+1.5V REF	4
Threshold Adjust	5
N/C	6
V_{IN}-	7
Sense-	8
Sense+	9
N.Inv. Input	10
N/C	11
Inv. Input	12
Fault Alert	13
Fault Delay	14
Driver Sink	15
N/C	16
Driver Source	17
Compensation/ Shutdown	18
O.V. Latch Output/Reset	19
Crowbar Gate	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for the UC1834, -40°C to +85°C for the UC2834, and 0°C to +70°C for the UC3834. V_{IN} = 15V, V_{IN} = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	1.47		1.53	1.455		1.545	
Line Regulation	V_{IN+} = 5 to 35V		1	10		1	15	mV
Load Regulation	I_{OUT} = 0 to 2mA		1	10		1	15	mV
-2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN}^+)	T_J = 25°C	2.04	-2	1.96	2.06	-2	1.94	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	2.06		1.94	2.08		1.92	
Line Regulation	V_{IN+} = 5 to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		kΩ
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 1.5V		1	6		1	10	mV
Input Bias Current	V_{CM} = 1.5V		-1	-4		-1	-8	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN+} Pin 13, 20Ω to V_{IN-}	50	65		50	65		dB
CMRR	V_{CM} = 0.5 to 33V, V_{IN+} = 35V	60	80		60	80		dB
PSRR	V_{IN+} = 5-35V, V_{CM} = 1.5V	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	I_{OUT} = 100mA		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V, Pin 13 = V_{IN-}, Pin 14 = V_{IN-}		0.1	50		0.1	50	µA
Shutdown Input Voltage at Pin 14	I_{OUT} = 100µA, Pin 13 = V_{IN-}, Pin 12 = V_{IN+}	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN-}, Pin 12 = V_{IN+} I_{OUT} = 100µA, Pin 13 = V_{IN-}		-100	-150		-100	-150	µA
Thermal Shutdown (Note 3)			165			165		°C
Fault Amplifier Section								
Under- and Over-Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	V_{IN+} = 35V, V_{CM} = 1.5 to 33V		-0.4	-0.8		-0.4	-1.0	%/v
Supply Sensitivity	V_{CM} = 1.5V, V_{IN+} = 5 to 35V		-0.5	-1.0		-0.5	-1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/µF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	I_{OUT} = 1mA		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	I_{OUT} = 1mA		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		-100	-175		-100	-175		mA
Crowbar Gate Leakage Current	V_{IN+} = 35V, Pin 16 = V_{IN-}		-0.5	-50		-0.5	-50	µA

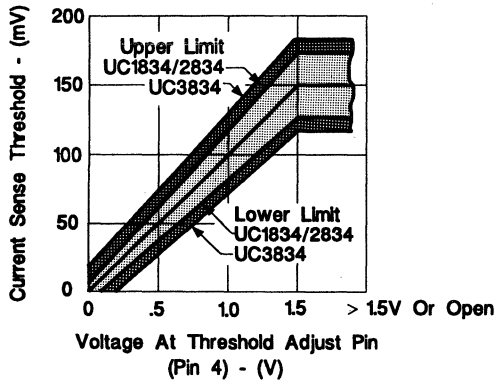
Note 2: When using both the 1.5V and -2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The -2.0V output will change -2.3mV per µA of imbalance.

Note 3: Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown) the O.V. Latch will be reset.

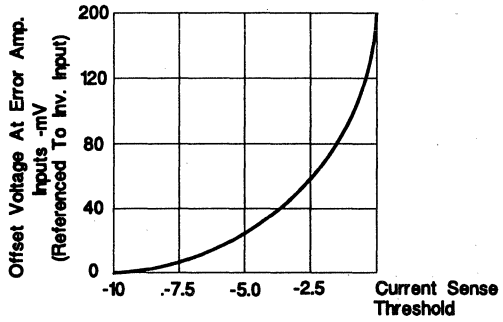
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for the UC1834, -40°C to +85°C for the UC2834, and 0°C to +70°C for the UC3834. V_{IN} = 15V, V_{IN} = 0V. T_A = T_J

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, V_{CM} = V_{IN+} or V_{IN-}	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, V_{CM} = V_{IN+} or V_{IN-}	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, V_{CM} = V_{IN-}, V_{IN+} = 5 to 35V		-0.1	-0.3		-0.1	-0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		-2	-10		-2	-10	µA
Sense Input Bias Current	V_{CM} = V_{IN+}		100	200		100	200	µA
	V_{CM} = V_{IN-}		-100	-200		-100	-200	

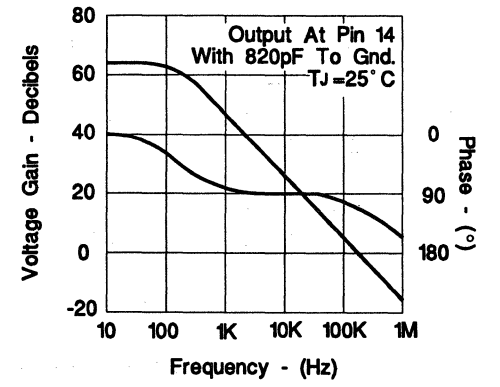
Current Sense Threshold Adjustment



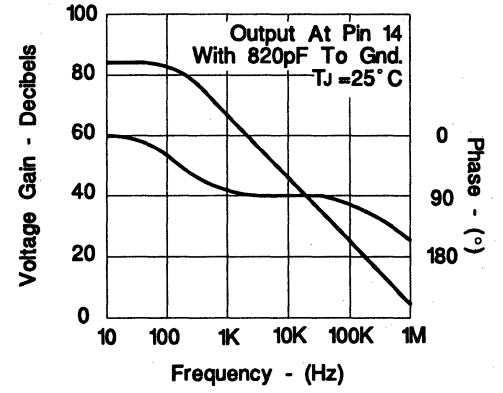
Current Limiting Knee Characteristics



Error Amplifier Gain and Phase Frequency Response

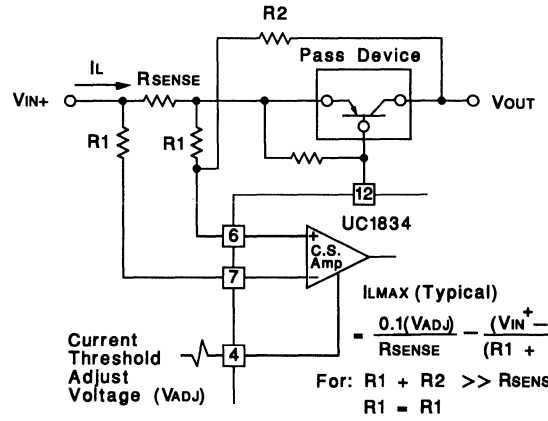


Current Sense Amplifier Gain and Phase Frequency Response



APPLICATION INFORMATION

Foldback Current Limiting



$$I_{LMAX}\ (Typical) = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN}^{+} - V_{OUT})\ R1}{(R1 + R2)\ R_{SENSE}},$$

For: $R1 + R2 >> R_{SENSE}$, $V_{ADJ} \leq 1.5V$, $R1 = R1$

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V\ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V\ C.S./A} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500kHz$ and $|Z_L(f)| \leq 1 M\Omega$

Where:

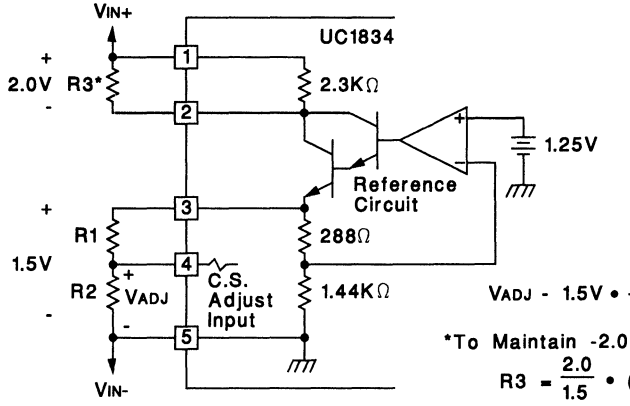
AV=Small Signal Voltage Gain to pin 14.

ZL(f) = Load Impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q- output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q- from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

Setting the Threshold Adjust Voltage (VADJ)



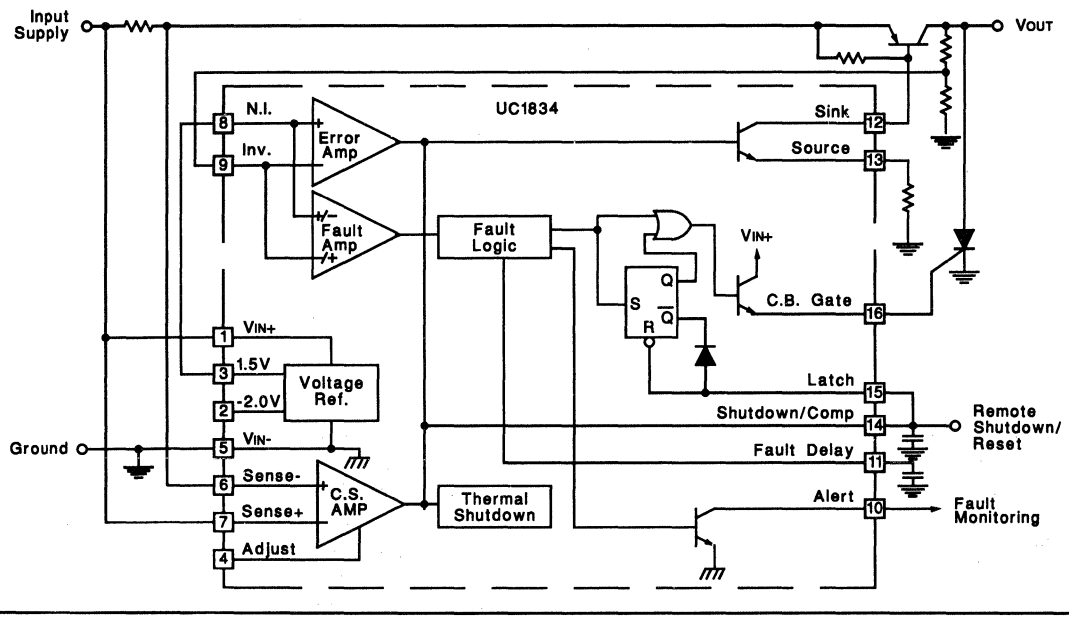
$$V_{ADJ} = 1.5V \bullet \frac{R2}{R1 + R2}$$

*To Maintain -2.0V Output

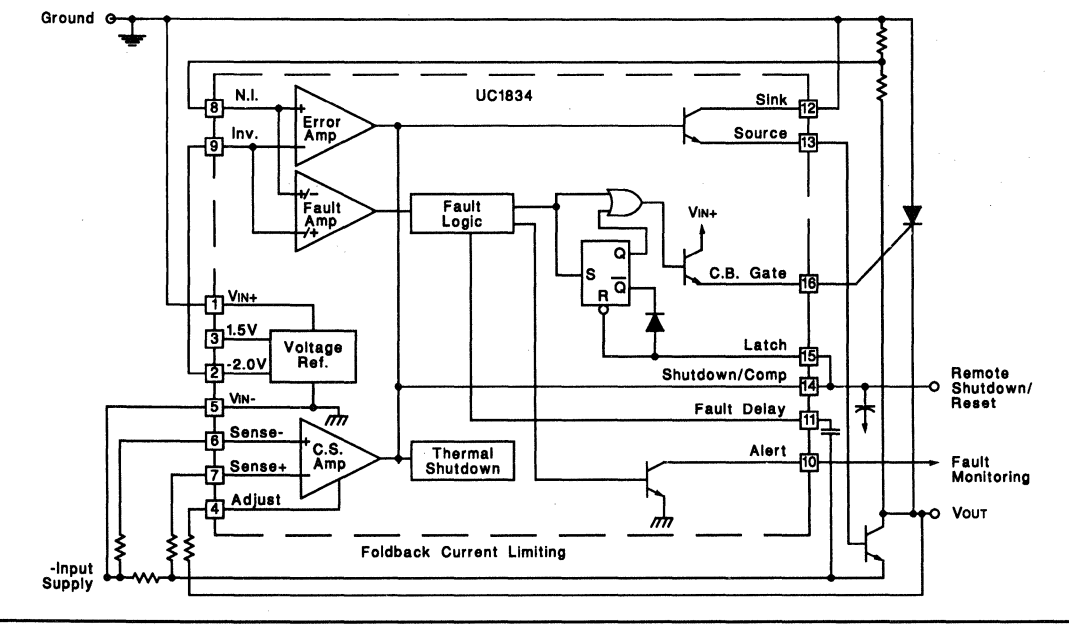
$$R3 = \frac{2.0}{1.5} \bullet (R1 + R2)$$

TYPICAL APPLICATIONS

5-10 Amp Positive Regulator



5-10 Amp Negative Regulator



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High Efficiency Regulator Controller

FEATURES

- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- 8 Pin Mini-Dip Package (Surface Mount also Available)

DESCRIPTION

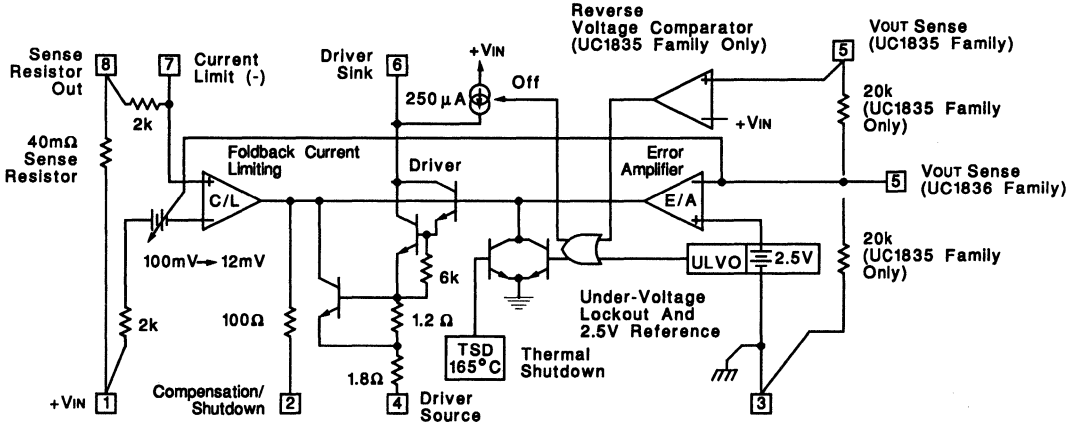
The UC1835/6 families of linear controllers are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained. These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (UC1835), or adjustable, (UC1836), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

5

BLOCK DIAGRAM



Note: Pin numbers refer to 8-Pin DIL Package

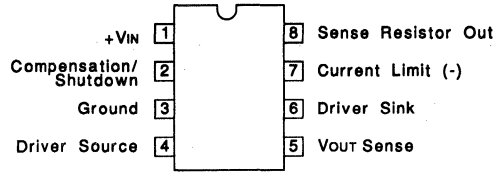
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (+VIN) ..... –1.0V to + 40V
Driver Output Current (Sink or Source) 600mA
Driver Source to Sink Voltage ..... + 40V
Maximum Current Through Sense Resistor..... 4A
VOUT Sense Input Voltage ..... –.3V to + 40V
Power Dissipation at TA = 25°C (Note 2) 1000mW
Power Dissipation at Tc = 25°C (Note 2)..... 2000mW
Operating Junction Temperature..... -55°C to +150°C
Storage Temperature..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)..... 300°C

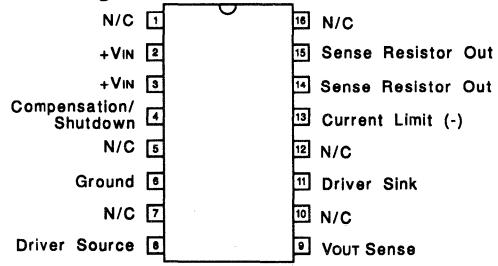
Note 1: Voltages are referenced to ground, (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal considerations and limitations of packages.

CONNECTION DIAGRAMS

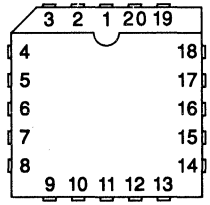
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
+VIN	3
N/C	4
Compensation/ Shutdown	5
N/C	6
Ground	7
N/C	8
N/C	9
Driver Source	10
N/C	11
VOUT Sense	12
N/C	13
N/C	14
Driver Sink	15
N/C	16
Current Limit (-)	17
N/C	18
Sense Resistor Out	19
Sense Resistor Out	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +VIN = 6V, Driver Source= 0V, Driver Sink = 5V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 6V		2.75	4.0	mA
	+VIN = 40V		3.75	6.0	mA
UVLO Threshold	+VIN Low to High, VOUT Sense = 0V	3.9	4.4	4.9	V
Threshold Hysteresis			0.1	0.35	V
Reverse Current	+VIN = -1.0V, Driver Sink Open		6.0	20	mA
Regulating Voltage and Error Amplifier (UC1835 Family Only)					
Regulating Level at VOUT Sense (VREG)	Driver Current = 10mA, TJ = 25°C	4.94	5.0	5.06	V
	Over Temperature	4.9		5.1	V
Line Regulation	+VIN = 5.2V + 35V		15	40	mV
Load Regulation	Driver Current = 0 to 250mA		6.0	25	mV
Bias Current at VOUT Sense	VOUT Sense = 5.0V	75	125	210	µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA

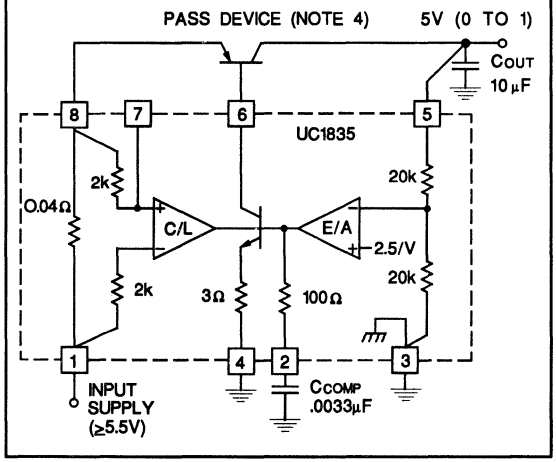
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +V_{IN} = 6V, Driver Source= 0V, Driver Sink = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Regulating Voltage and Error Amplifier (UC1836 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	2.47	2.5	2.53	V
	Over Temperature	2.45		2.55	V
Line Regulation	+V_{IN} = 5.2V to 35V		6.0	20	mV
Load Regulation	Driver Current = 0 to 250mA		3.0	15	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense =2.5V	-1.0	-0.2		µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Driver					
Maximum Current		250	500		mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	V
Pull-Up Current at Driver Sink	Compensation/Shutdown=0.45V	140	250	300	µA
Driver Sink Leakage	In UVLO			10	µA
	In Reverse Voltage (UC1835 Family Only)			10	µA
Thermal Shutdown			165		°C
Foldback Current Limit					
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	A
Current Limit Amp Tansconductance	±100µA at Compensation/Shutdown, V_{OUT} Sense = (0.9) V_{REG}	12	24	42	mS
Limiting Voltage at Current Limit (-) (Note 2)	V_{OUT} Sense = (0.9) V_{REG} Volts Below +V_{IN}, T_J = 25°C	80	100	140	mV
Sense Resistor Value (Note 3)	V_{OUT} Sense = (0.9) V_{REG}, I_{OUT} = I_A, T_J = 25°C		40		mΩ

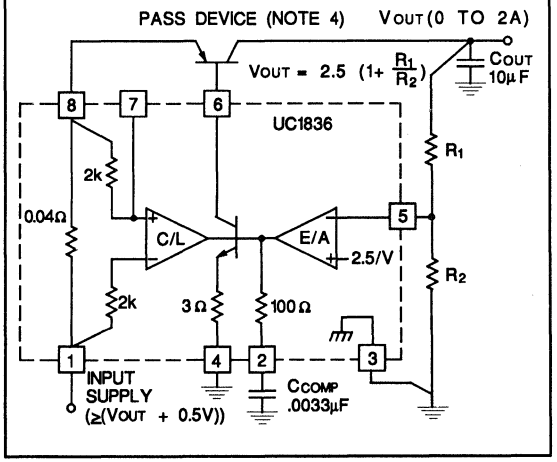
Note 2: This voltage has a positive temperature coefficient of approximately 3500ppm/°C.
Note 3: This resistance has a positive temperature coefficient of approximately 3500ppm/°C. The total resistance from Pin 1 to Pin 8 will include an additional 60 to 100mΩ of package resistance.

APPLICATION AND OPERATION INFORMATION

UC 1835 – Typical configurations for a 2A, Low Dropout 5V Regulator



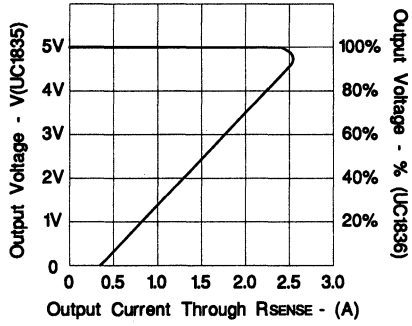
UC1836 – Typical Configuration for a 2A, Low Dropout Adjustable Regulator



Note 4: Suggested Pass devices are TIP 32B. (Dropout Voltage ≤0.75V) or, D45H, (Dropout Voltage ≤0.5V), or equivalents.

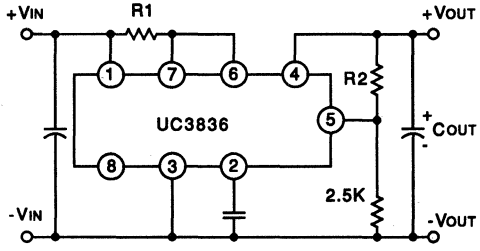
APPLICATION AND OPERATION INFORMATION (cont.)

UC1835/6 Foldback Current Limiting



UC3835/36 TYPICAL APPLICATIONS

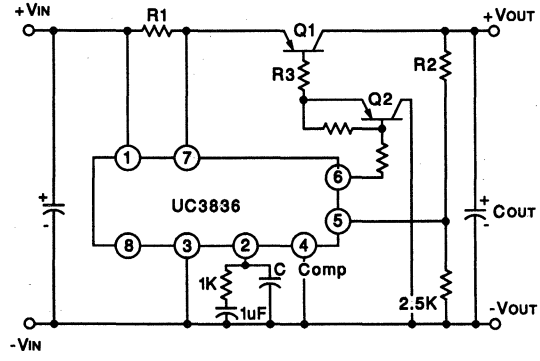
Low Current Application
using the UC3836 internal drive transistor



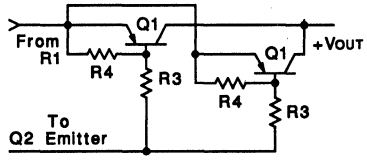
Typical Output Current vs VIN and VOUT
of the UC3836 internal drive transistor
for PDISS = 5.5W (approx.)

		VIN					
	Volts	5	9	12	15	18	24
VOUT	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

High Current Application
using drive transistor Q2 to increase Q1 base drive
and reduce UC3836 power dissipation



Parallel Pass Transistors
can be added for high current or
high power dissipation applications



EQUATIONS:

$R_1 = 0.100\ V/I_{OUT}$ (MAX)

$R_2 = (V_{OUT} - 2.5V/1mA)$

$R_3 = ((V_{IN} - V_{BE} - V_{SAT})*BETA(min))/I_{OUT}$ (max)

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INTEGRATED CIRCUITS
UNITRODE

UC1838A
UC2838A
UC3838A

Magnetic Amplifier Controller

FEATURES

- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with -120V Capability
- 5V to 40V Analog Operation
- 5W DIL Package

DESCRIPTION

The UC1838A family of magnetic amplifier controllers contains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source will provide the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2A to 20A.

By controlling the reset current to a magnetic amplifier, this device will define the amount of volt-seconds the magnetic amplifier will block before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width-modulated input voltage, a magnetic amplifier will block a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC1838A, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

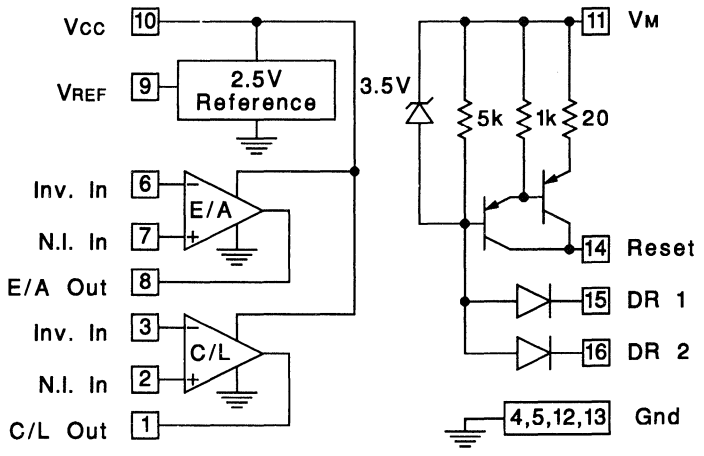
The UC1838A contains a precision 2.5V reference, two uncommitted high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of magnetic amplifier reset current and with -120 volt capability.

These devices are available in a plastic "bat-wing" DIP for operation over a -20°C to +85°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Surface mount versions are also available.

This improved "A" version replaced the non "A" version formerly introduced.

5

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS

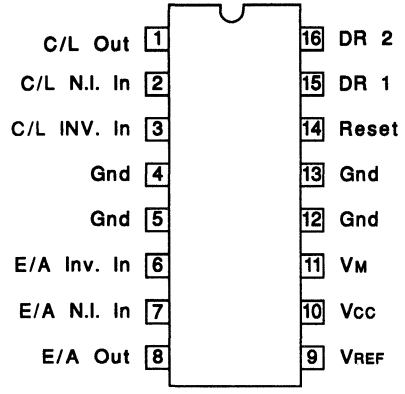
Supply Voltage, V_{CC} 40V
Magnetic Amp. Source Voltage, V_M 40V
Reset Output Voltage, V_R ..... -120V
Total Current Source Voltage, V_M - V_R ..... -140V
Amplifier Input Range ..... -0.3V to Vcc
Reset Input Current, I_{DR} ..... -10mA

	Q, N Package	J Package
Power Dissipation at T_A = 25°C	2W	1W
Power Dissipation at T (leads/case) = 25°C	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

Note: All voltages are with respect to ground pins.
All currents are positive into the specified terminal.
Consult Packaging section of Databook for thermal limitations and considerations of package.

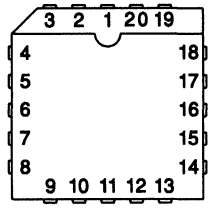
CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



Note: All four ground pins must be connected to a common ground

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L Out	2
C/L N.I. In	3
C/L Inv. In	4
GND	5
N/C	6
N/C	7
E/A Div. In	8
E/A N.I. In	9
E/A Out	10
N/C	11
V_{REF}	12
Vcc	13
V_M	14
GND	15
N/C	16
N/C	17
Reset	18
DR 1	19
DR 2	20

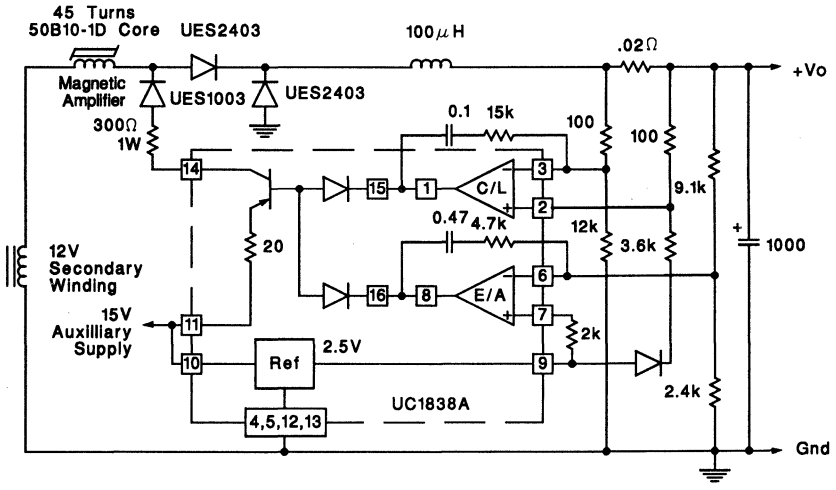
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1838A, -20°C to +85°C for the UC2838A, and 0°C to +70°C for the UC3838A, V_{CC} = 20V, V_M = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1838A / UC2838A			UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Supply Current	V_{CC} = V_M = 40V		4	8		4	8	mA
Reference Output	T_A = 25°C	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	V_{CC} = 5 to 30V		1	5		1	10	mV
Load Regulation	I_O = 0 to -2mA		5	20		5	20	mV
Short Circuit Current	V_{REF} = 0V		-30	-60		-30	-60	mA
Temperature Stability*	Over Operating Temp. Range		15	25		10	25	mV
Amplifier Section (Each Amplifier)								
Offset Voltage	V_{CM} = 2.5V			5			10	mV
Input Bias Current	V_{IN} = 0V			-1			-1	µA
Input Offset Current				100			100	nA
Minimum Output Swing		0.4		18	0.4		18	V
Output Sink Current	V_O = 5V	1	10	30	1	10	30	mA
Output Source Current	V_O = 0V	-1	-10	-20	-1	-10	-20	mA
A_{VOL}	V_O = 1 to 11V	100	120		100	120		dB
CMRR	V_{IN} = 1 to 11V	70	80		70	80		dB
PSRR	V_{CC} = 10 to 20V	70	100		70	100		dB
Gain Bandwidth*		0.6	0.8		0.6	0.8		MHz
Reset Drive Section								
Input Leakage	V_{DR} = 40V			10			10	µA
Output Leakage	V_R = -120V			-100			-100	µA
Input Current	I_R = -50mA		-1	-2		-1	-2	mA
Maximum Reset Current	I_{DR} = -3mA	-100	-120	-200	-100	-120	-200	mA
Transconductance	I_R = -10 to -50mA	.03	.042	.055	.03	.042	.055	A/V

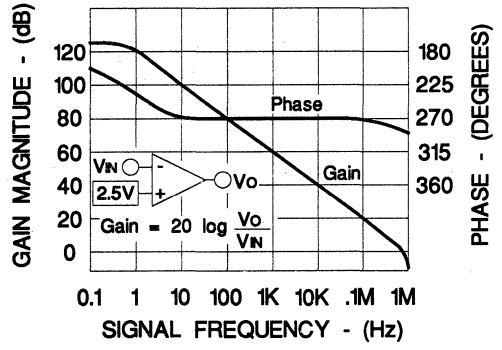
** These parameters are guaranteed by design but not 100% tested in production.*

TYPICAL APPLICATION

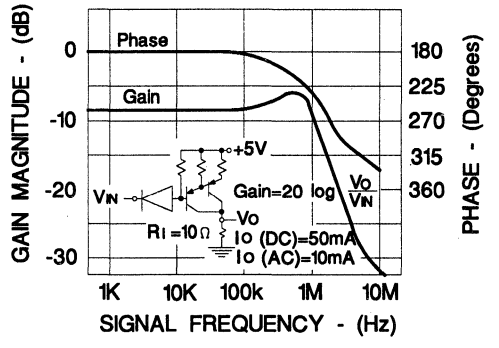
+12V, 4A Output With Switching Frequency = 50 kHz



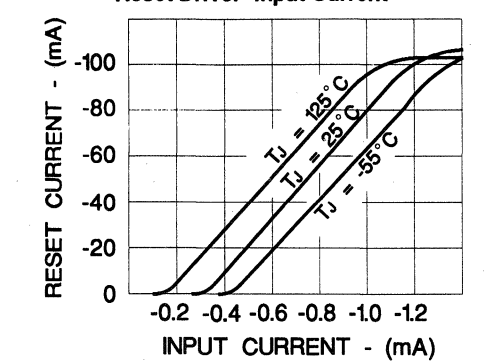
Amplifier Open Loop Response



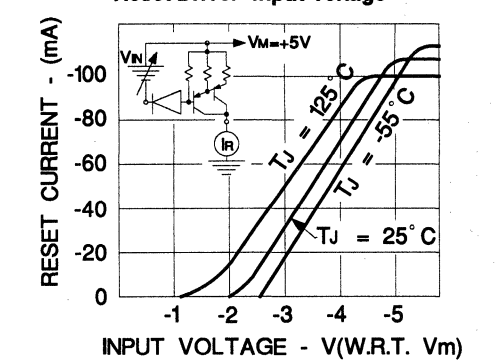
Reset Driver Response



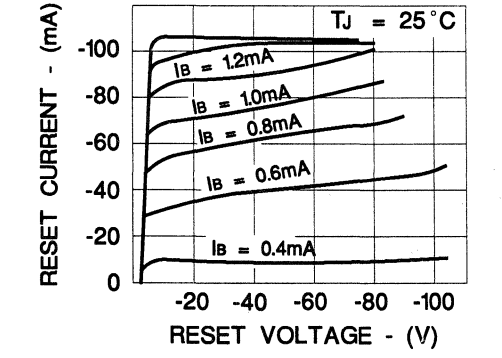
Reset Driver- Input Current



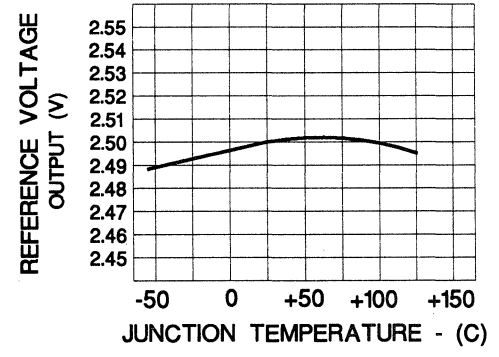
Reset Driver- Input Voltage



Reset Driver- Output Impedance



Reference Temperature Coefficient



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INTEGRATED CIRCUITS
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UC1840
UC2840
UC3840

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current, Off-Line Start Circuit
- Feed-Forward Line Regulation over 4 to 1 Input Range
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On and Maximum Duty-Cycle Clamp
- Shutdown Upon Over-or Under-Voltage Sensing
- Latch Off or Continuous Retry after Fault
- Remote, Pulse-Commandable Start/Stop
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18-pin DIL package

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operations over a wide input voltage range.

In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

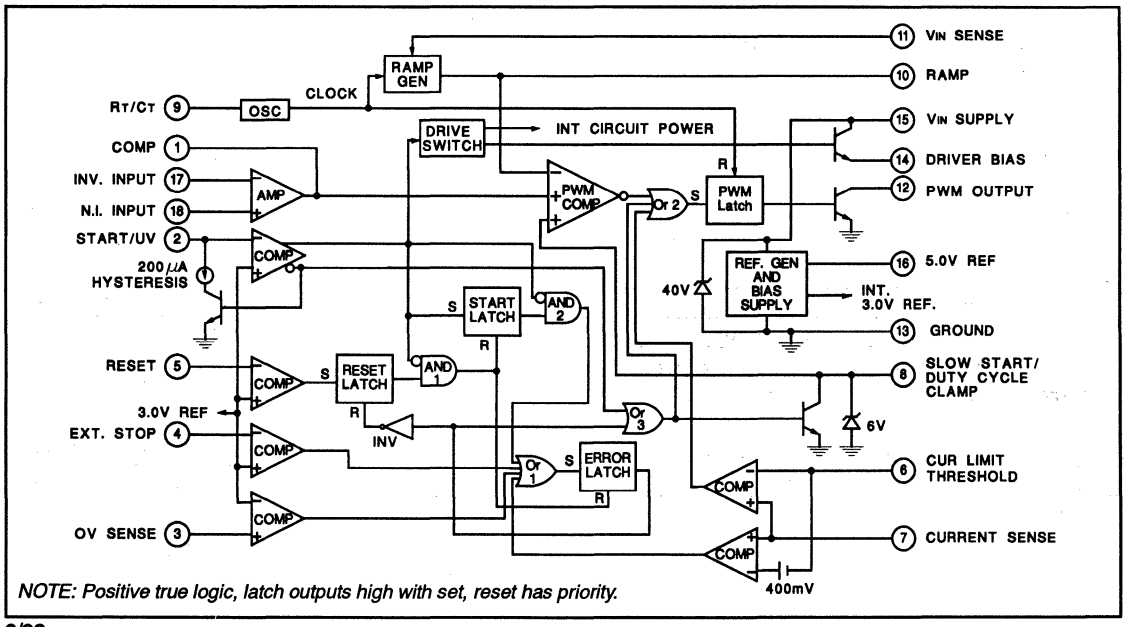
Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and high-speed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package. The UC1840 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2840 and UC3840 are designed for operation from -25°C to +85°C and 0°C to +70°C, respectively.

NOTE: THIS DEVICE NOT RECOMMENDED FOR NEW DESIGNS.

5

BLOCK DIAGRAM



NOTE: Positive true logic, latch outputs high with set, reset has priority.

6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

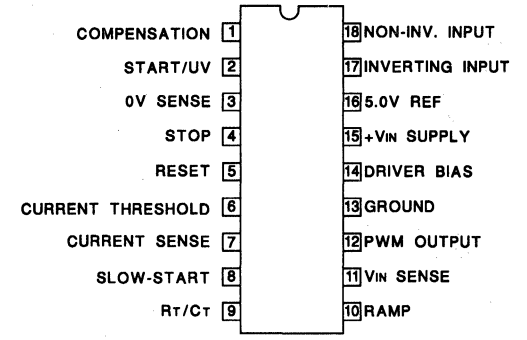
Supply Voltage, +VIN (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Comparator Inputs (Pins 2, 3, 4, 5, 17, 18) ..... -0.3 to +32V
Power Dissipation at TA = 25°C 1000mW
Power Dissipation at TC = 25°C 2000mW
Thermal Resistance, Junction to Ambient ..... 100°C/W
Thermal Resistance, Junction to Case ..... 60°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) ..... +300°C

Note: 1. All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.

CONNECTION DIAGRAM

DIL-18 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1840, -25°C to + 85°C for the UC2840, and 0°C to + 70°C for the UC3840; VIN = 20V, RT = 20k, CT = .001mfd, CR = .001mfd, Current Limit Threshold = 200mV, TA=TJ.

PARAMETER	TEST CONDITIONS	UC1840 / UC2840			UC3840			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	VIN = 30V, Pin 2 =2.5V, TJ = 25°C		4	5.5		4	5.5	mA
Start-Up Current T.C.*	VIN = 30V, Pin 2 = 2.5V		-0.1	-0.2		-0.1	-0.2	%/°C
Operating Current	VIN = 30V, Pin 2 = 3.5V	5	10	15	5	10	15	mA
Supply OV Clamp	IIN = 20mA	33	40	45	33	40	48	V
Reference Section								
Reference Voltage	TJ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 20mA		10	20		10	30	mV
Temperature Coefficient*	Over Operating Temperature Range			±0.4			±0.4	mV/°C
Short Circuit Current	VREF = 0, TJ = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	TJ = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Temperature Coefficient*	Over Operating Temperature Range			±.08			±.08	%/°C
Maximum Frequency	RT = 2kΩ, CT = 330pF	500			500			kHz
Ramp Generator								
Ramp Current, Minimum	ISENSE = -10µA	-14	-11		-14	-11		µA
Ramp Current, Maximum	ISENSE = 1.0mA		-.95	-0.9		-.95	-0.9	mA
Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to + 125°C for the UC1840, -25°C to + 85°C for the UC2840, and 0°C to + 70°C for the UC3840; V_{IN} = 20V, R_T = 20k, C_T = .001mfd, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

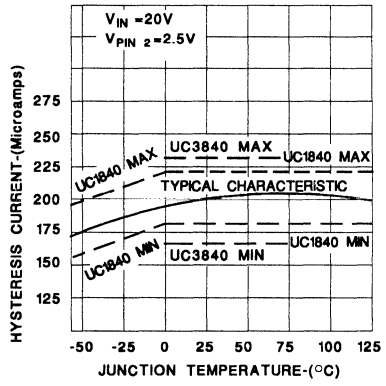
PARAMETER	TEST CONDITIONS	UC1840 / UC2840			UC3840			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range, Ramp Peak < 4.2V	5		95	5		95	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay*	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 4, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 4, 5 = 0V		-1.0	-3.0		-1.0	-3.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V, T_J = 25°C	180	200	220	170	200	230	µA
Input Leakage	Input V = 20V		0.1	10		0.1	10	µA
Driver Bias Saturation Voltage, V_{IN} - V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 2mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	Vs = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

** These parameters are guaranteed by design but not 100% tested in production.*

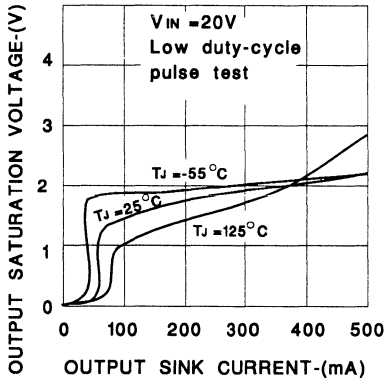
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where Kc is a first order correction factor ~ 0.3 log (C_T X 10^{12}).
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two possible inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense	This comparator performs three functions — With an increasing voltage, it generates a turn-on signal at a start threshold. With a decreasing voltage, it generates a UV fault signal at a lower level separated by a 200μA hysteresis current. At the UV threshold, it also resets the Error Latch if the Reset Latch has been set.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias off, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM off. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider $R_S R_{DC}$.
5. Start Latch	Keeps low input voltage at initial turn-on from being defined as a UV fault . Sets at start level to monitor for UV fault.
6. Reset Latch	When reset, this latch insures no reset signal to either Start or Error Latches so that first fault will lock the PWM off. When set, this latch resets the Start and and Error latches at the UV low threshold, allowing a restart.
PROTECTION FUNCTIONS	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. UV low (after turn-on) b. OV high c. Stop low d. Current Sense 400mV over threshold. Error Latch resets at UV threshold if Reset Latch is set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV above threshold, a shutdown signal is sent to error latch.

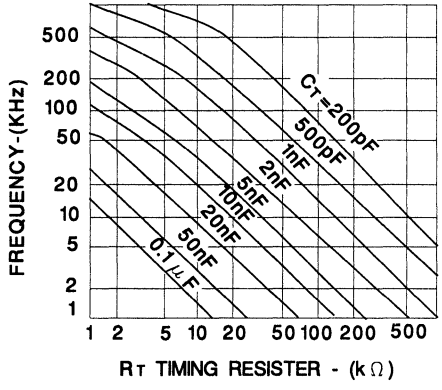
Start/UV Hysteresis Current



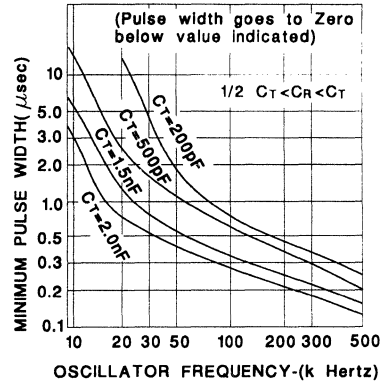
PWM Output Saturation Voltage



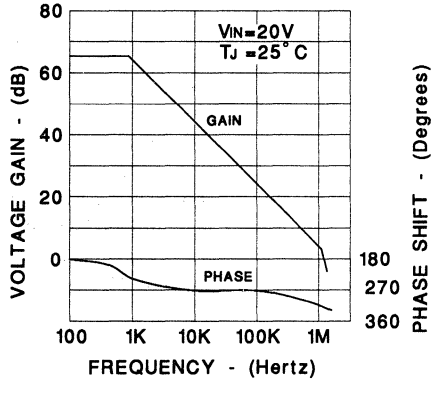
Oscillator Frequency



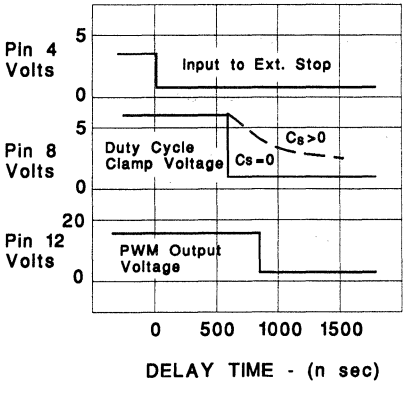
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Pulse



Shutdown Timing



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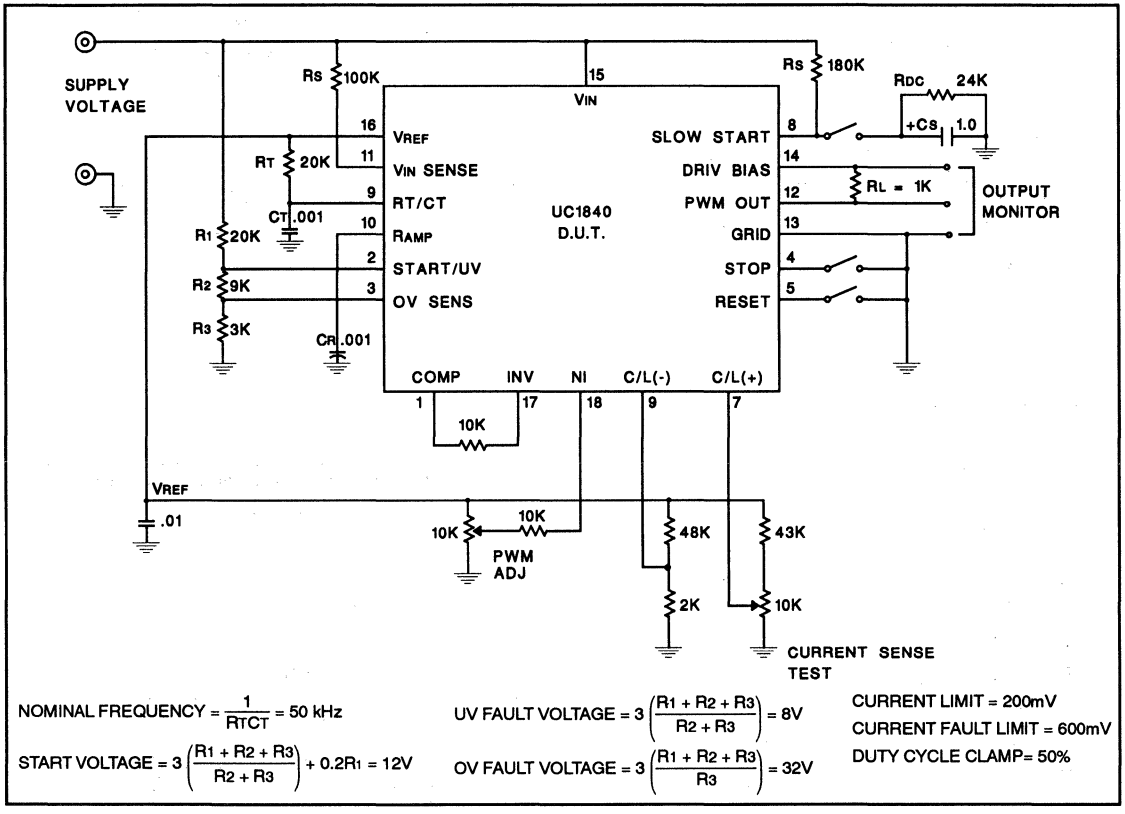
OPEN-LOOP TEST CIRCUIT



FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary- referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling — a task made even easier with the UC1840's feed-forward line regulation.

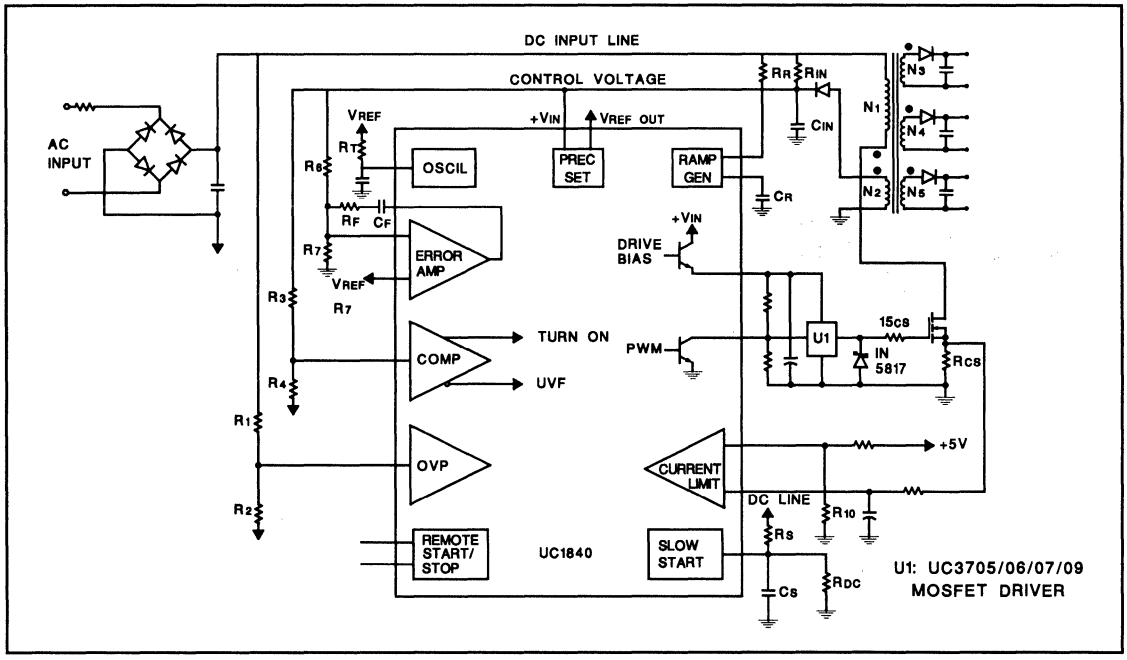
An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output. The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application.

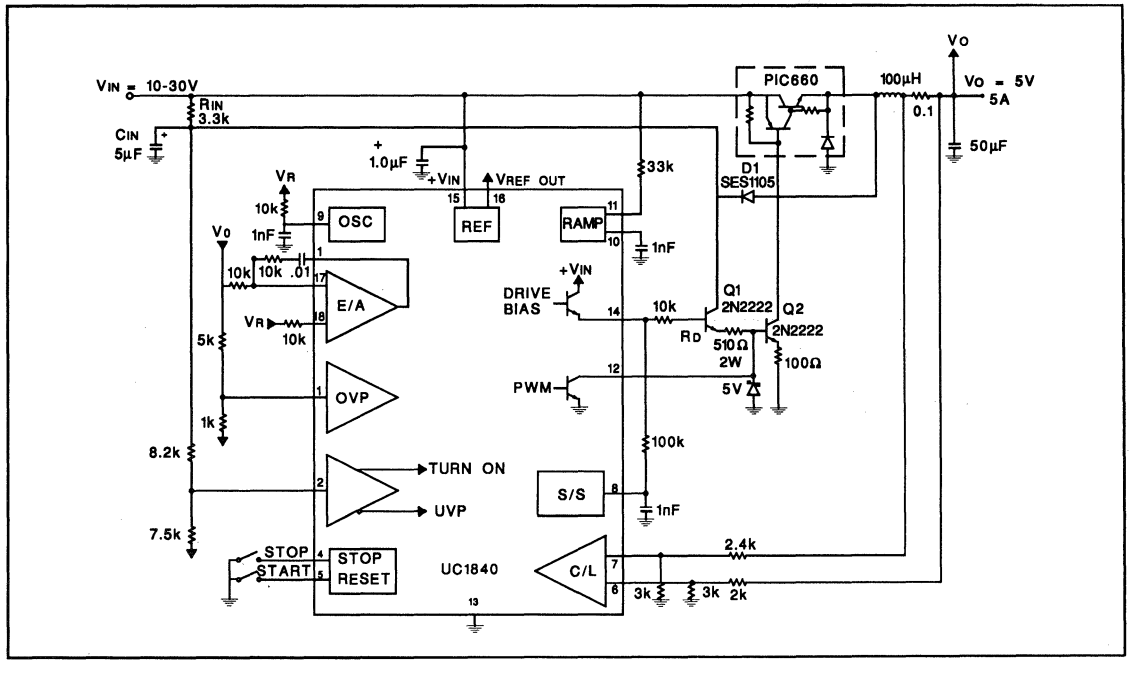
REGULATOR APPLICATION (B)

Although primarily intended for transformer-coupled power systems, the UC1840's advantages of feed-forward for high ripple-rejection, a fully contained fault monitoring system and remote start/stop capability make it worth considering for other types of regulators. Since the fault logic within the UC1840 requires recycling the voltage sensed by the Start/UV comparator to reset the error latch, a need for automatic restart must be addressed in a manner similar to that shown in Figure B (next page). In this simple, non-isolated, buck regulator; diode D1 provides a low-impedance bootstrapped drive power source after start-up is achieved through RIN and CIN. When a fault shutdown terminates switching action, the loading of Q1 and RD will lower the voltage on pin 2 to effect an automatic re-start attempt which will continuously recycle until the fault is removed.

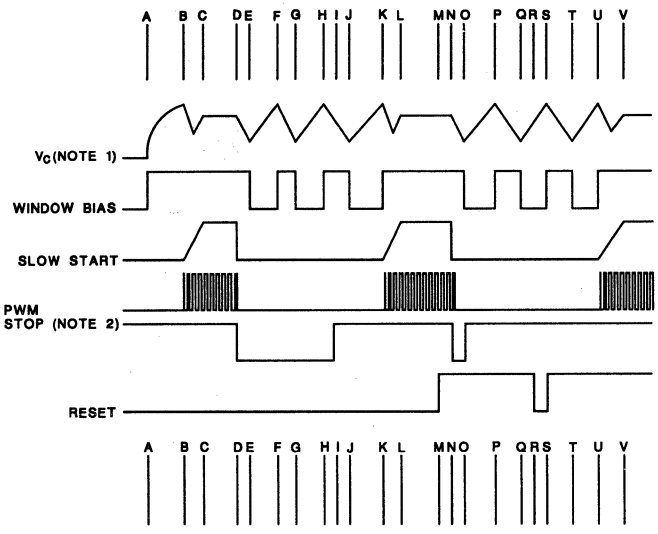
Uc1840 Programmable Pwm Controller in a Simplified Flyback Regulator (A)



UC1840 Controls a High-Current Non-Isolated Buck Regulator (B)



UC1840 POWER SEQUENCING FUNCTIONS

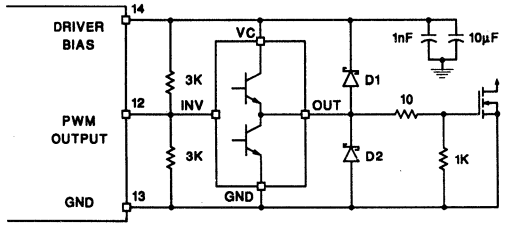


TIME	EVENT
A	Initial turn-on, Vc rises with load
B	Start threshold. Driver Bias loads Vc
C	Operating PWM regulates Vc
D	Stop input sets Error Latch turning off PWM
E	UV low threshold, Error Latch remains set
F	Start turns on Driver bias but Error Latch still set
G, H	Vc and Driver Bias continue to cycle
I	Stop command removed
J	Error Latch reset at UV low threshold
K	Start threshold now removes slow-start clamp
L	Return to normal run state
M	Reset Latch set signal removed
N	Error Latch set with momentary fault
O	Error Latch does not reset as Reset Latch is reset
P, Q	Vc and Driver Bias recycle with no turn-on.
R	Reset Latch set is set with momentary Reset signal
S	Vc must complete cycle to turn-on
T	Start and Error Latches reset
U	Normal start initiated
V	Return to normal run state

Notes 1: Vc represents an analog of the output voltage generated by a primary referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and, in most cases, is the supply voltage, VIN, for the UC1840.

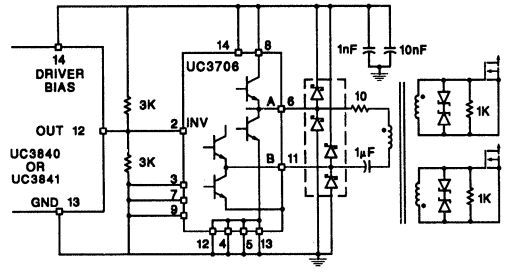
Note 2: Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

Power MOSFET Drive Circuit Using UC3705/3706/3707 or 3709 Drivers



D1, D2: UC3611 Schottky Diode

UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration



UC3611 Quad Schottky Diode Array

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INTEGRATED CIRCUITS
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UC1841
UC2841
UC3841

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-current, Off-line Start Circuit
- Voltage Feed Forward or Current Mode Control
- Guaranteed Duty Cycle Clamp
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-up or Shutdown Transients
- Slow Turn-on Both Initially and After Fault Shutdown
- Shutdown Upon Over- or Under-Voltage Sensing
- Latch Off or Continuous Retry After Fault
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL Package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

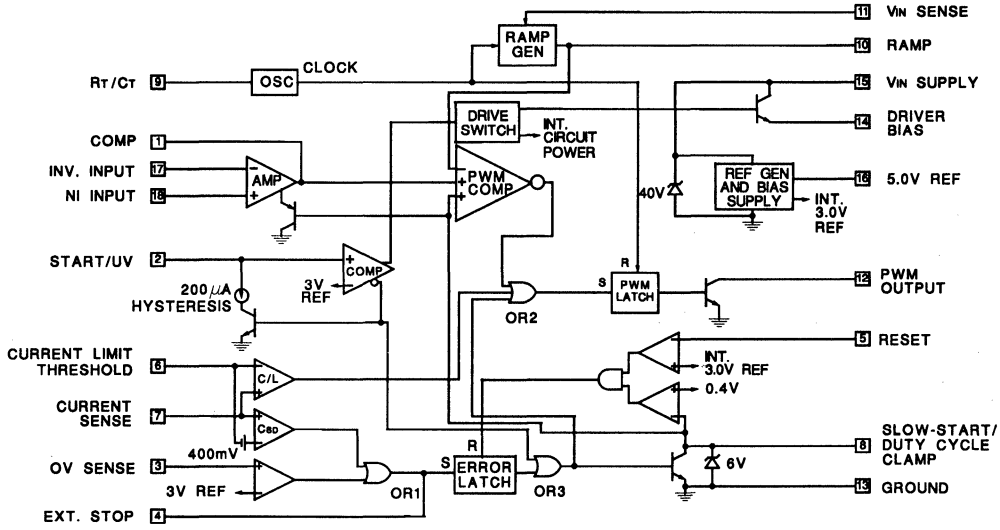
While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

The UC1841 is characterized for -55°C to +125°C operation while the UC2841 and UC3841 are designed for -25°C to +85°C and 0°to +70°C, respectively.

5

BLOCK DIAGRAM



Note: Positive true logic, latch outputs high with set, reset has priority.

6/93

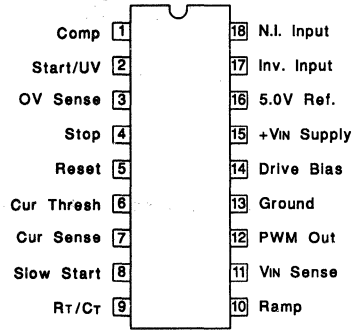
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V_{IN} (Pin 15) (Note 2)
  Voltage Driven ..... +32V
  Current Driven, 100mA maximum ..... Self-limiting
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Stop Input (Pin 4) ..... -0.3 to +5.5V
Comparator Inputs
  (Pins 1, 7, 9-11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

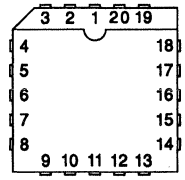
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTIONS	
FUNCTION	**PIN**
Comp	1
Start/UV	2
OV Sense	3
Stop	4
Reset	5
CUR Thresh	7
CUR Sense	8
Slow Start	9
RT/CT	10
Ramp	11
VIN Sense	12
PWM Out	13
Ground	14
Drive Bias	15
+VIN Supply	17
5.0V REF	18
Inv. Input	19
N.I. Input	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		10	14		10	14	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

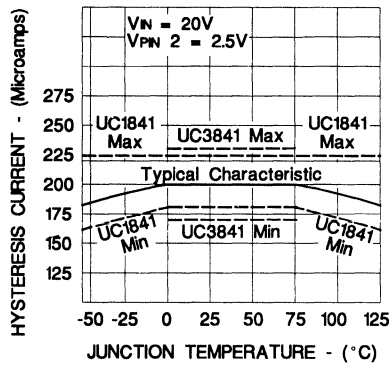
PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O= 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range, Ramp Peak < 4.2V	4		95	4		95	%
50% Duty Cycle Clamp	R_{SENSE} to V_{REF} = 10k	42	47	52	42	47	52	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay*	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN} - V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

** These parameters are guaranteed by design but not 100% tested in production.*

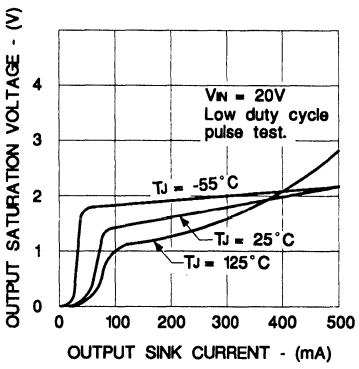
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where Kc is a first order correction factor ≈ 0.3 log (C_T X 10^{12}).
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense	With an increasing voltage, it generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by RsCs for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (typically 3V) b. Stop > 2.4V (typically 1.6V) c. Current Sense 400mV over threshold (typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a typical delay of 13ms/µF.

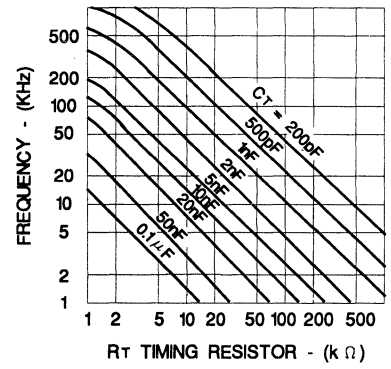
Start/UV Hysteresis



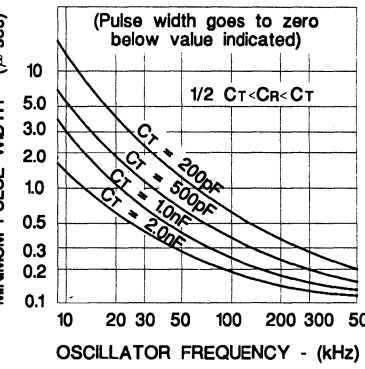
PWM Output-Saturation Voltage



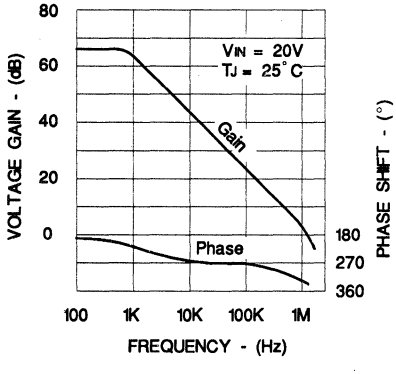
Oscillator Frequency



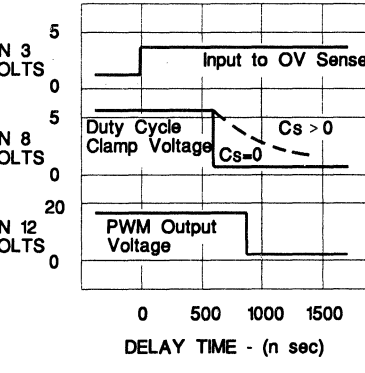
PWM Output Minimum Pulse Width



Error Amplifier Open Loop Gain and Phase

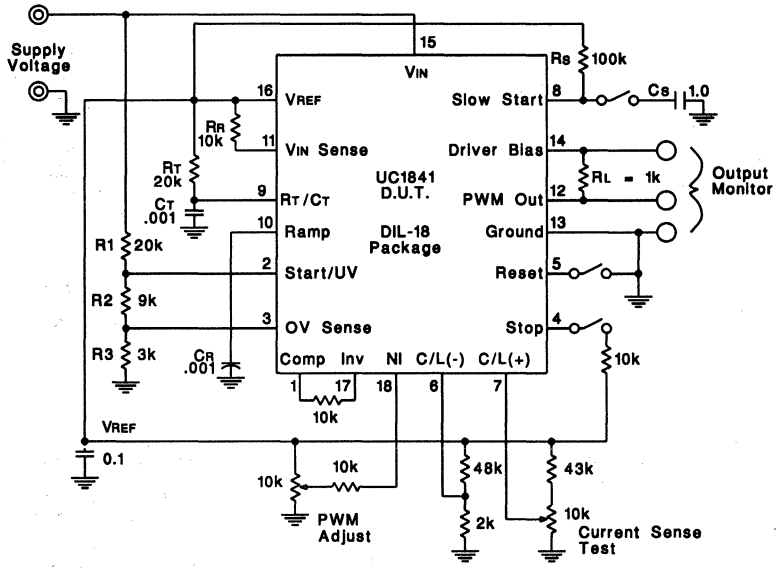


Shutdown Timing



5

OPEN-LOOP TEST CIRCUIT



$$\text{Nominal Frequency} = \frac{1}{R_T C_T} = 50\text{ kHz}$$

$$\text{Start Voltage} = 3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) + 0.2R1 = 12\text{V}$$

$$\text{UV Fault Voltage} = 3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) = 8\text{V}$$

$$\text{OV Fault Voltage} = 3\left(\frac{R1 + R2 + R3}{R3}\right) = 32\text{V}$$

Current Limit = 200mV

Current Fault Voltage = 600mV

Duty Cycle Clamp = 50%

FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1841's feed-forward line regulation.

An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to

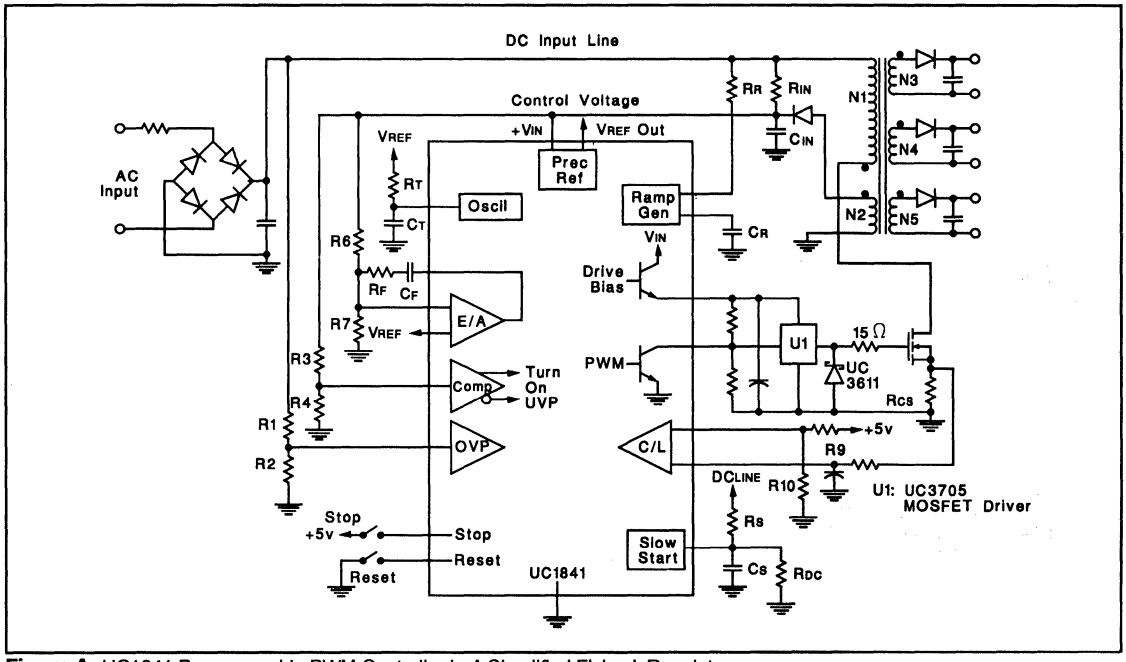


Figure A. UC1841 Programmable PWM Controller In A Simplified Flyback Regulator

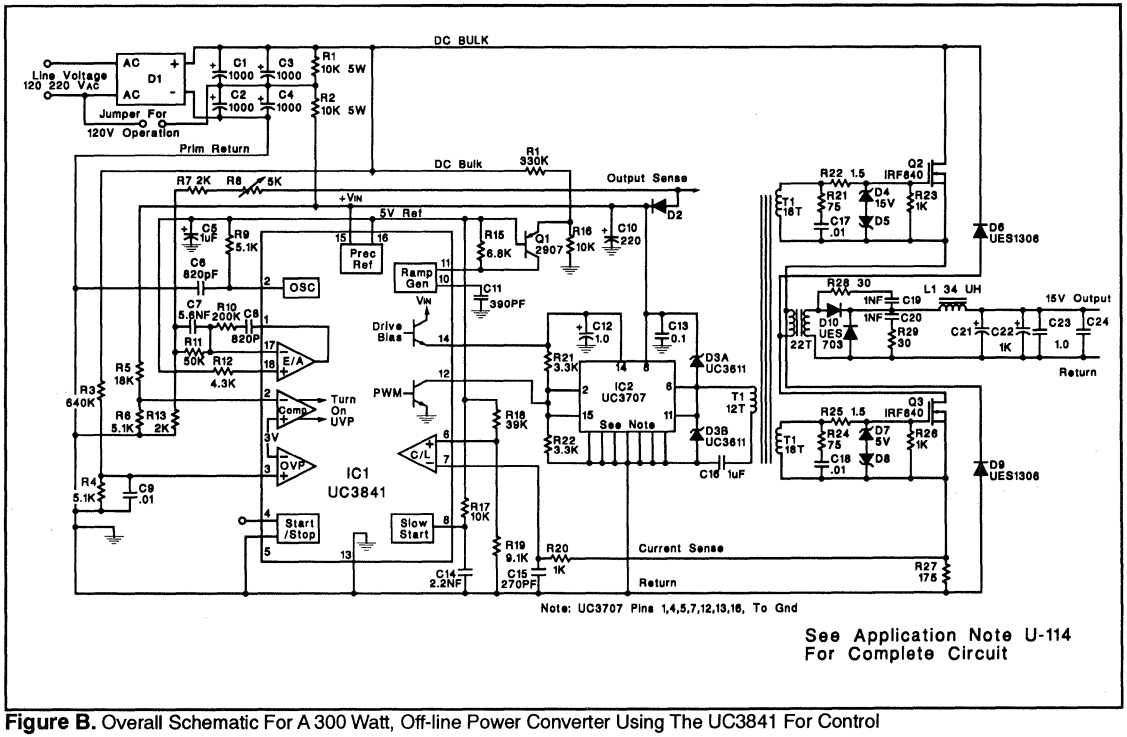
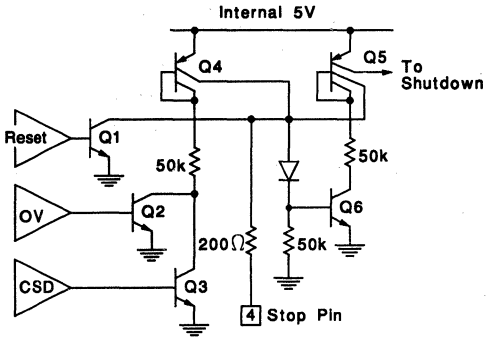


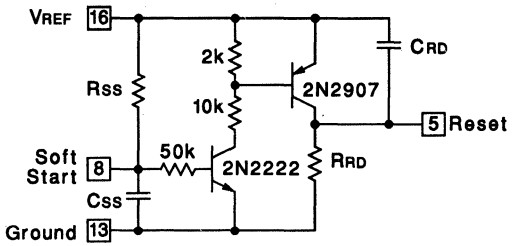
Figure B. Overall Schematic For A 300 Watt, Off-line Power Converter Using The UC3841 For Control

ERROR LATCH INTERNAL CIRCUITRY



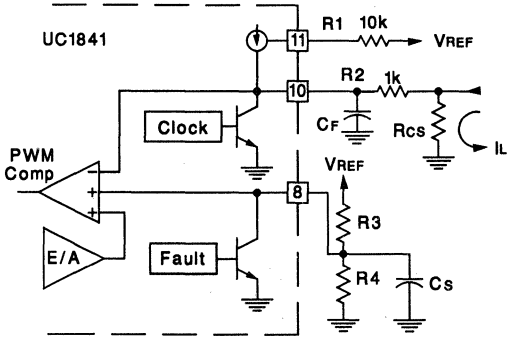
The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the ~ 100μA collector current from Q4.

PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT



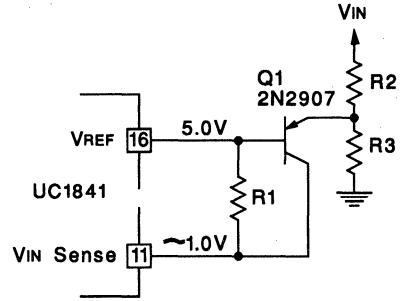
Restart Delay = (.51)(RRD)(CRD)

CURRENT MODE CONTROL



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through Rcs. Resistor R1 sets a 400mV offset across R2 (assuming R2 > Rcs) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with CF as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R1 is used in conjunction with CR (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing VIN.

The minimum ramp current is:

$$I_{R(MIN)} = \frac{V_{REF} - V_{IN\ SENSE}}{R1} \sim \frac{4V}{R1}$$

The threshold where VIN begins to add extra ramp current is:

$$V_{IN} \sim 5.6V\left(\frac{R2 + R3}{R3}\right)$$

Above the threshold, the ramp current will be:

$$I_R\ (VARIAB) \sim \frac{4}{R1} + \frac{V_{IN} - 5.6}{R2} - \frac{5.6}{R3}$$

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UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low Ro Error Amp

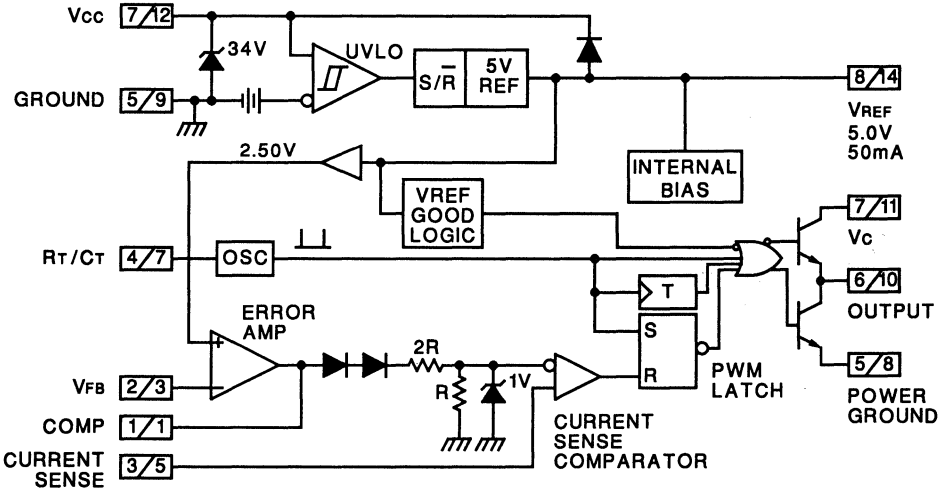
DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

5

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

6/93

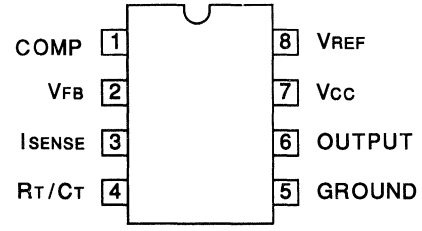
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc <30mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SOIC-14) 725mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

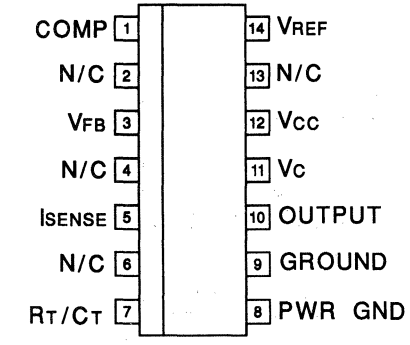
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

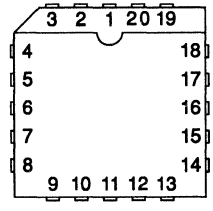
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D8 Package



SOIC-14 (TOP VIEW)
D Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
COMP	2
N/C	3
N/C	4
VFB	5
N/C	6
ISENSE	7
N/C	8
N/C	9
RT/CT	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C ≤ T_A ≤ 125°C for the UC184X; -40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T =3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2) (Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note2)		50			50		μV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\,4}$ peak to peak (Note 2)		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\,1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\,2}$ = 2.7V, $V_{PIN\,1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\,2}$ = 2.3V, $V_{PIN\,1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\,2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\,2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 and 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\,1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3) (Note 2)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	$V_{PIN\,3}$ = 0 to 2V (Note 2)		150	300		150	300	ns

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\,2}$ = 0.
Note 4: Gain defined as

$$A = \frac{\Delta\, VPIN1}{\Delta\, VPIN3},\ 0 \le VPIN3 \le 0.8V$$

Note 5: Adjust Vcc above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.
Note 7: Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp\ Stability = \frac{V_{REF}(max) - VREF(min)}{TJ(max) - TJ(min)}$$

V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55°C \le T_A \le 125°C$ for the UC184X; $-40°C \le T_A \le 85°C$ for the UC284X; $0°C \le T_A \le 70°C$ for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T =3.3nF, T_A=T_J.

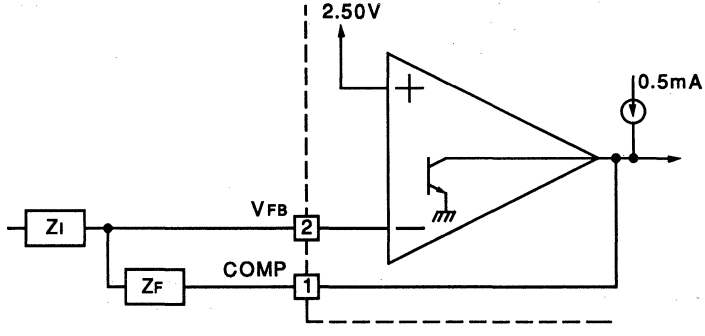
PARAMETER	TEST CONDITION	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Under-voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\,2}$ = $V_{PIN\,3}$ = 0V		11	17		11	17	mA
Vcc Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\,2}$ = 0.
Note 4: Gain defined as:

$$A = \frac{\Delta\, VPIN\,1}{\Delta\, VPIN\,3};\ 0 \le VPIN\,3 \le 0.8V.$$

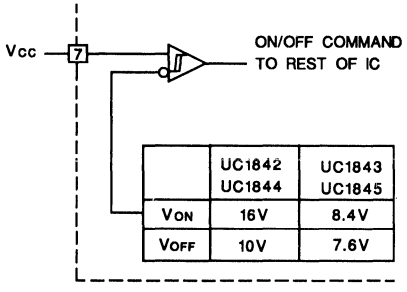
Note 5: Adjust Vcc above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

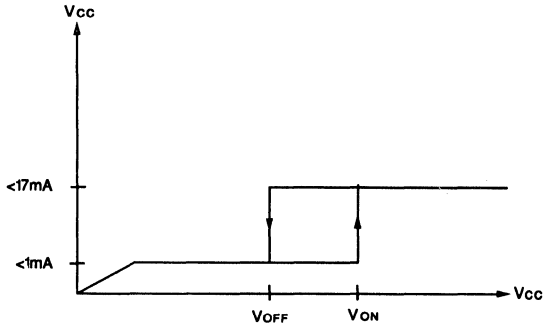


Error Amp can Source or Sink up to 0.5mA

UNDER-VOLTAGE LOCKOUT

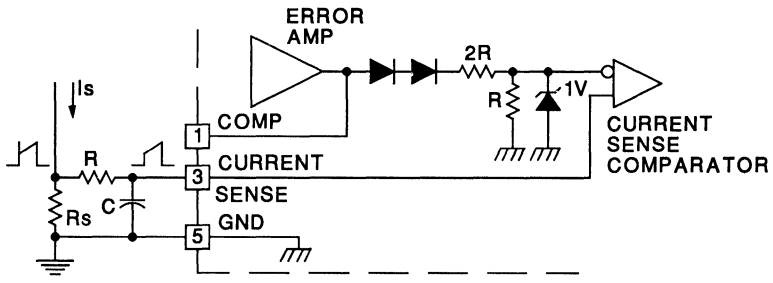


	UC1842 UC1844	UC1843 UC1845
VON	16V	8.4V
VOFF	10V	7.6V



During under-voltage lock-out, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

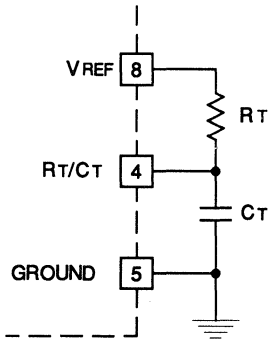


Peak Current (Is) is Determined By The Formula

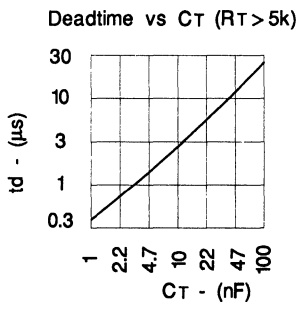
$$I_{SMAX} \approx \frac{1.0V}{Rs}$$

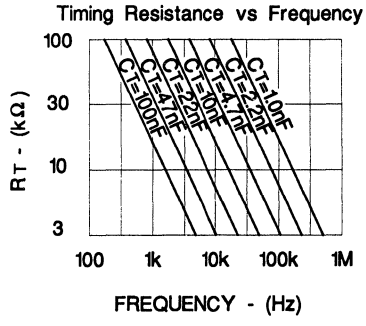
A small RC filter may be required to suppress switch transients.

OSCILLATOR SECTION

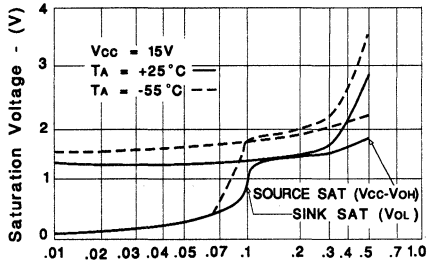


For $R_T > 5k$ $f \approx \frac{1.72}{R_T C_T}$

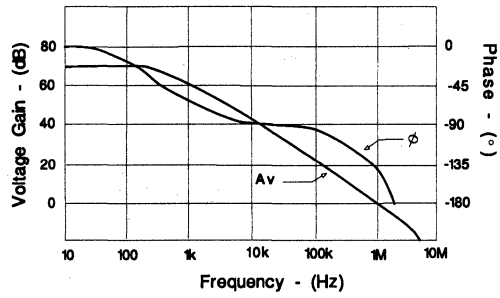




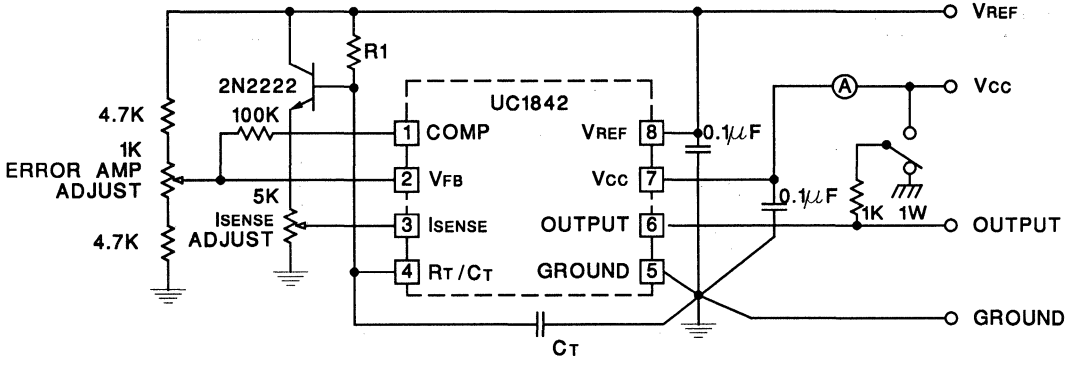
OUTPUT SATURATION CHARACTERISTICS



ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

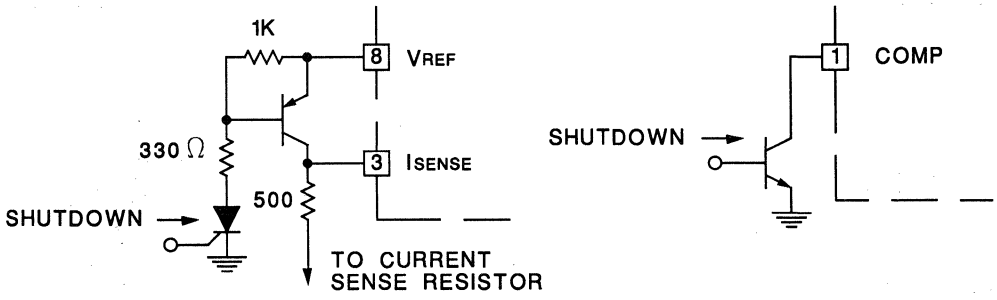


OPEN-LOOP LABORATORY FIXTURE



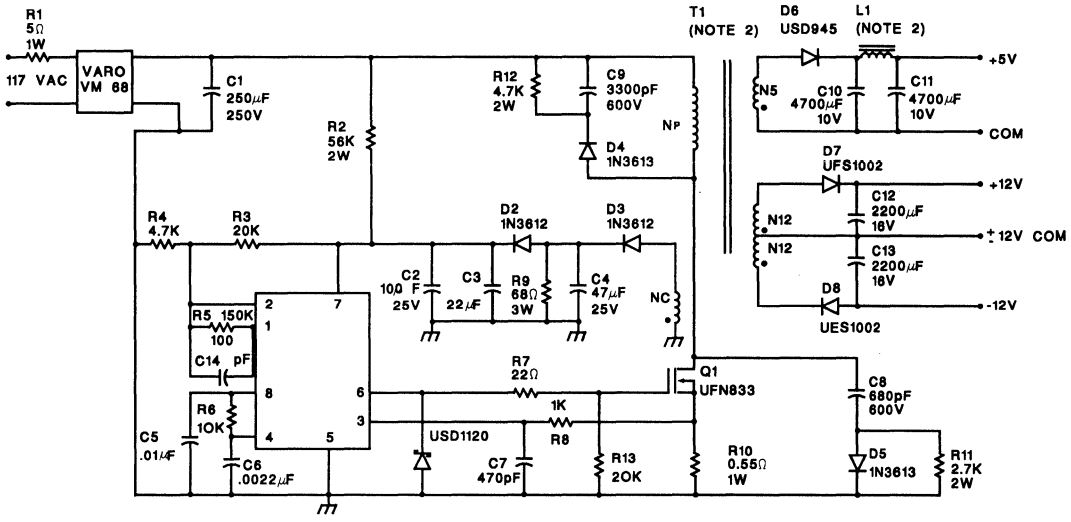
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUT DOWN TECHNIQUES



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

OFFLINE FLYBACK REGULATOR

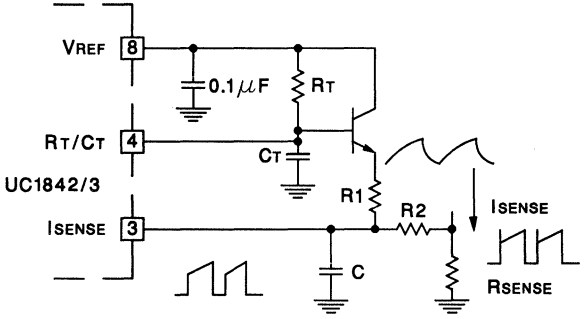


Power Supply Specifications

1. Input Voltage	95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation	3750V
3. Switching Frequency	40kHz
4. Efficiency @ Full Load	70%

5. Output Voltage:
   - A. +5V, ±5%; 1A to 4A load
     Ripple voltage: 50mV P-P Max
   - B. +12V, ±3%; 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max
   - C. -12V ,±3%; 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C_T forms a filter with R2 to suppress the leading edge switch spikes.

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

INTEGRATED CIRCUITS
UNITRODE

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

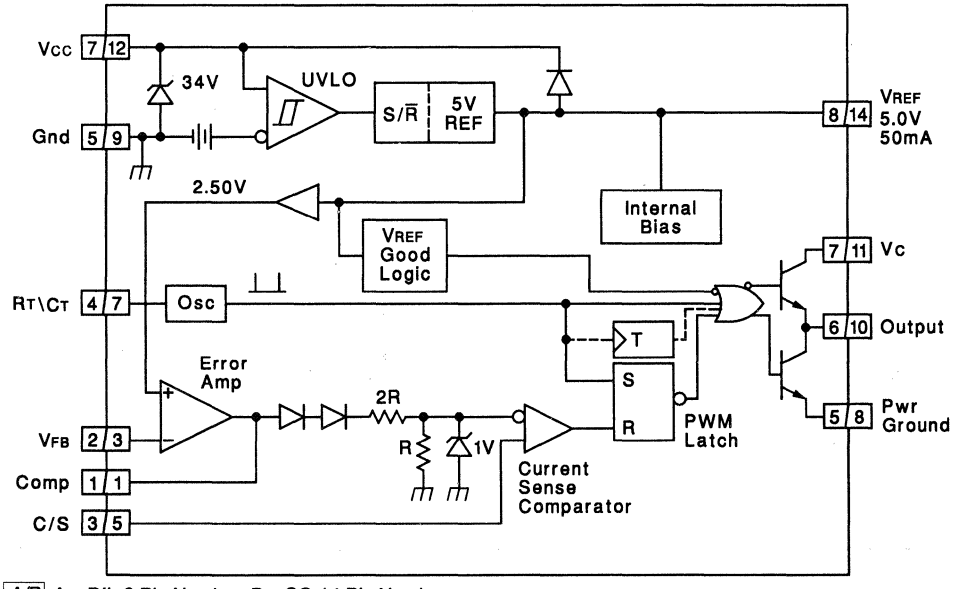
DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for Vcc over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

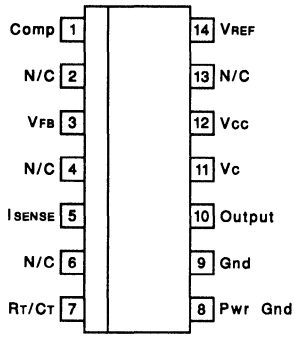
6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc mA)..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load)..... 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

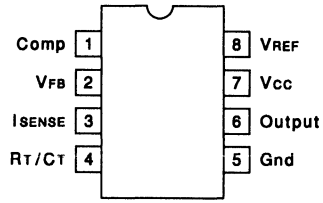
Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

SOIC-14 (TOP VIEW)
D Package

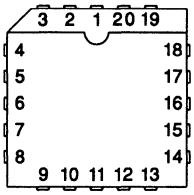


CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
J or N, D8 Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
VFB	5
N/C	6
ISENSE	7
N/C	8-9
RT/CT	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
Vc	17
Vcc	18
N/C	19
VREF	20

5

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq 125°C$ for the UC184xA; $-40°C \leq T_A \leq 85°C$ for the UC284xA; $0 \leq T_A \leq 70°C$ for the UC384xA; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF; $T_A = T_J$; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J = 25°C, Io = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25V$		6	20		6	20	mV
Load Regulation	$1 \leq Io \leq 20mA$		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz T_J = 25°C (Note 2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25V$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Discharge Current	T_J = 25°C, $V_{PIN\ 4}$ = 2V	7.8	8.3	8.8	7.8	8.3	8.8	mA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; VCC = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	VPIN 4 = 2V	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	VPIN 1 = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
AVOL	2 ≤ Vo ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	TJ = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ VCC ≤ 25V	60	70		60	70		dB
Output Sink Current	VPIN 2 = 2.7V, VPIN 1 = 1.1V	2	6		2	6		mA
Output Source Current	VPIN 2 = 2.3V, VPIN 1 = 5V	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	VPIN 2 = 2.3V, RL = 15k to ground	5	6		5	6		V
VOUT Low	VPIN 2 = 2.7V, RL = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	VPIN 1 = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ VCC ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	VPIN 3 = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	ISINK = 20mA		0.1	0.4		0.1	0.4	V
	ISINK = 200mA		15	2.2		15	2.2	V
Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
	ISOURCE = 200mA	12	13.5		12	13.5		V
Rise Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
Fall Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	VCC = 5V, ISINK = 10mA		0.7	1.2		0.7	1.2	V
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
TurnOn	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	VPIN 2 = VPIN 3 = 0V		11	17		11	17	mA

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with VPIN2 = 0.

Note 4: Gain defined as: $A = \frac{\Delta V_{PIN\,1}}{\Delta V_{PIN\,3}}$; $0 \le V_{PIN\,3} \le 0.8V$.

Note 5: Adjust Vcc above the start threshold before setting at 15V.

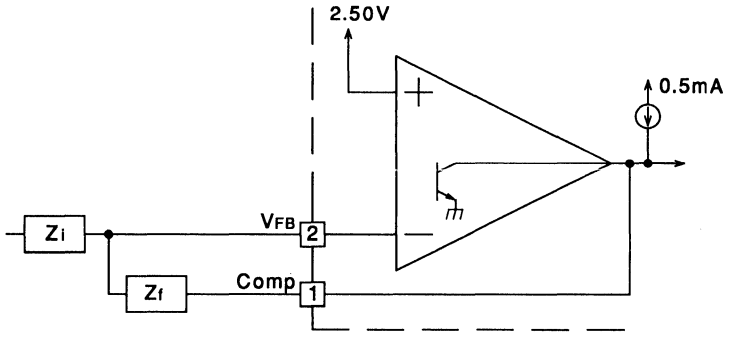
Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(max) - V_{REF}(min)}{T_J(max) - T_J(min)}.$$

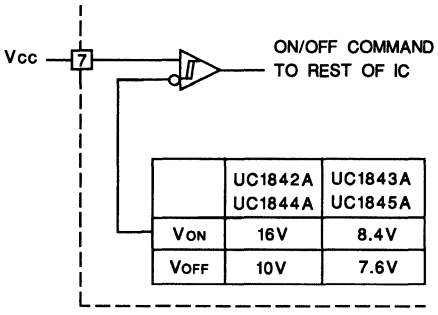
VREF (max) and VREF (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage

Error Amp Configuration

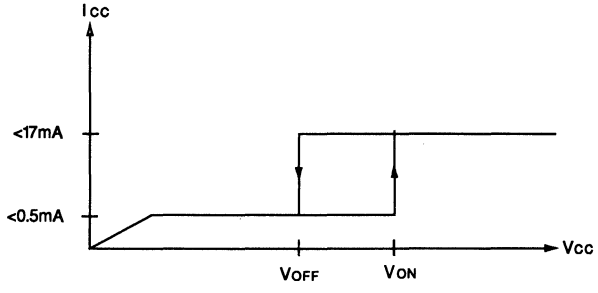


Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

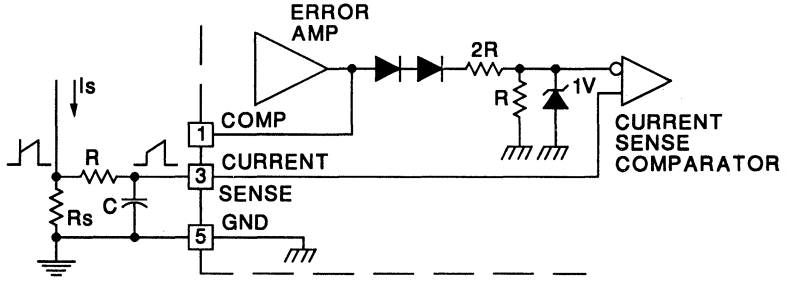


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

Current Sense Circuit



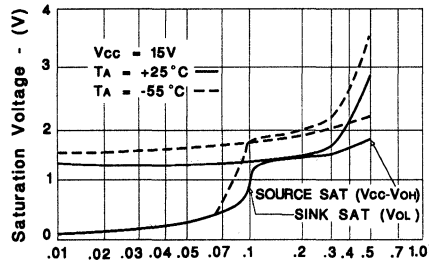
Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{Rs}$$

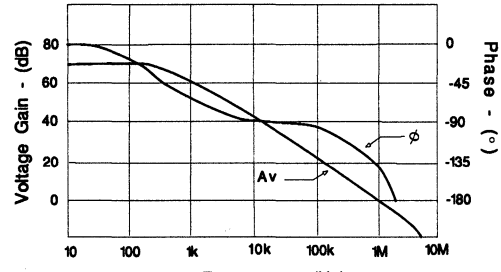
A small RC filter may be required to suppress switch transients.

APPLICATIONS DATA (cont.)

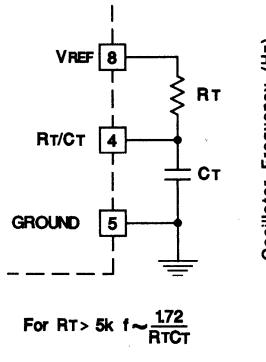
Output Saturation Characteristics



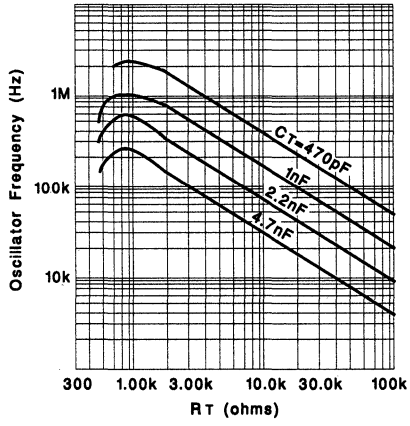
Error Amplifier Open-Loop Frequency Response



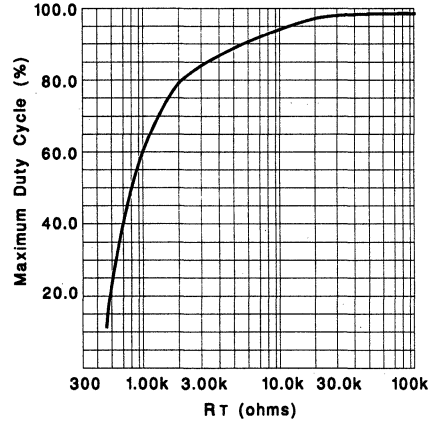
Oscillator Section



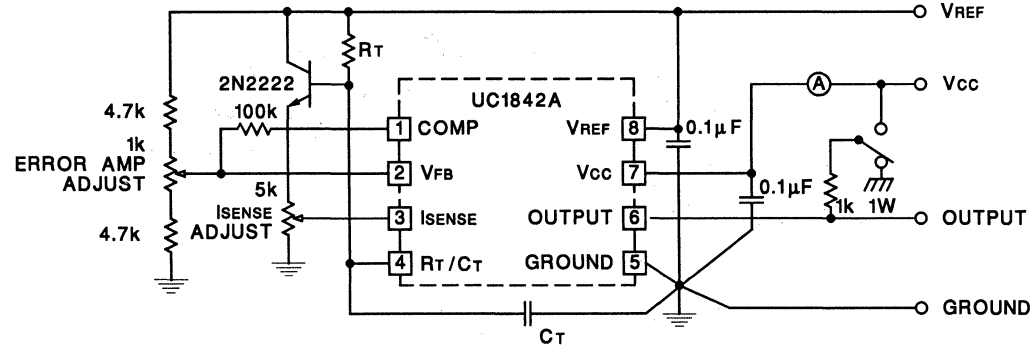
Oscillator Frequency vs Timing Resistance



Maximum Duty Cycle vs Timing Resistor



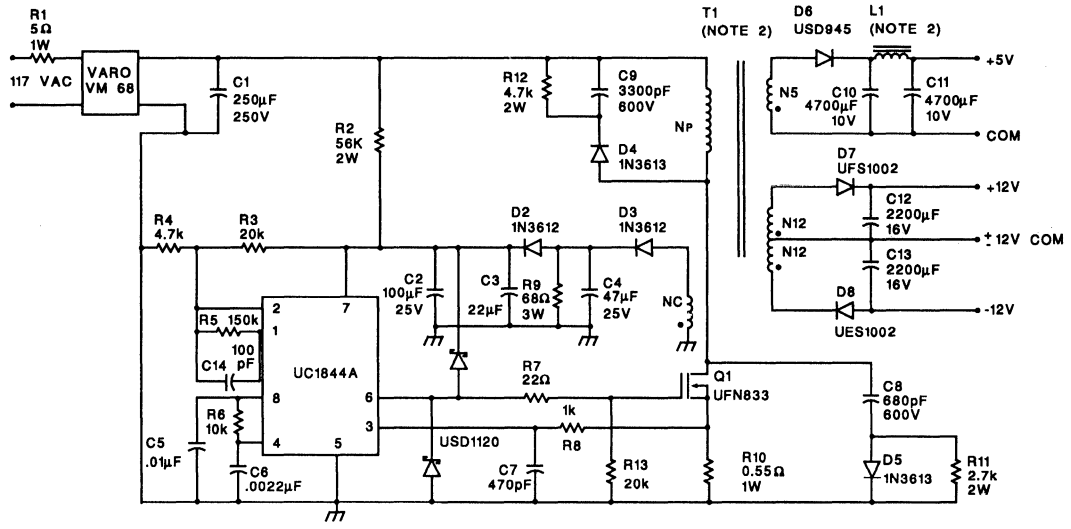
Open-Loop Laboratory Test Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

APPLICATIONS DATA (cont.)

Off-line Flyback Regulator

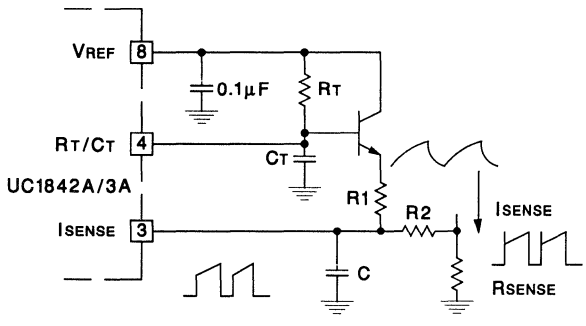


Power Supply Specifications

1. Input Voltage	95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation	3750V
3. Switching Frequency	40kHz
4. Efficiency @ Full Load	70%

5. Output Voltage:
A. +5V, ±5%; 1A to 4A load
Ripple voltage: 50mV P-P Max
B. +12V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
C. -12V ,±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max

Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

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INTEGRATED CIRCUITS
UNITRODE

Current Mode PWM Controller

UC1846/7
UC2846/7
UC3846/7

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- ±1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHZ Operation

DESCRIPTION

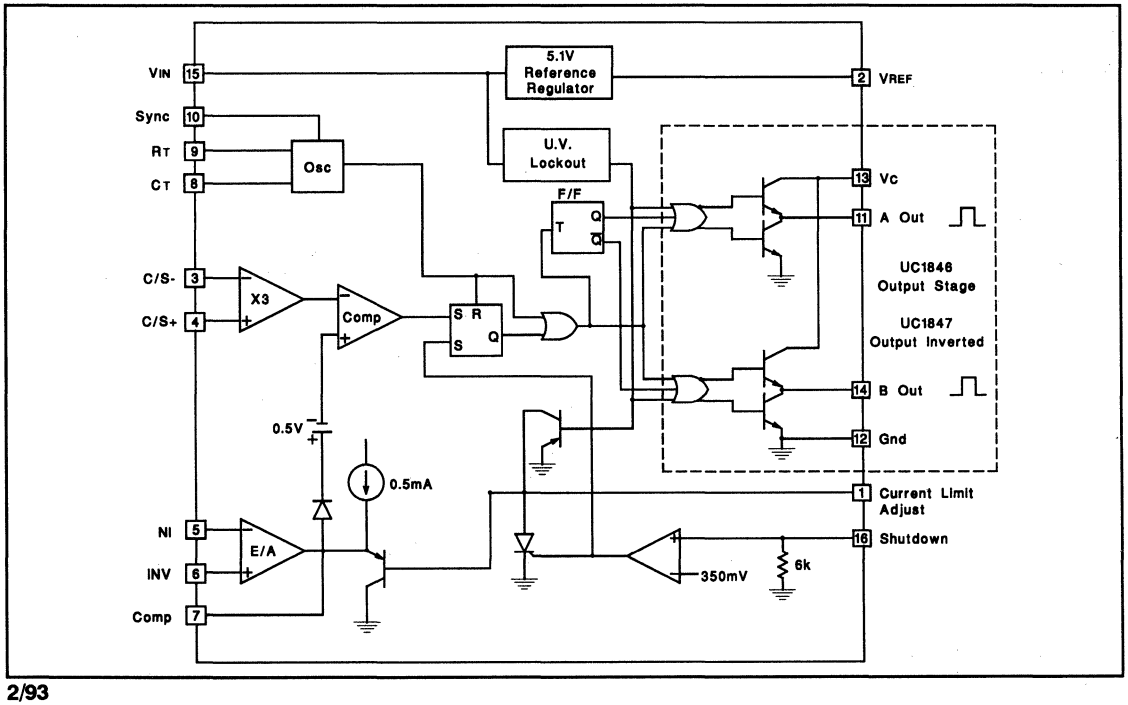
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



2/93

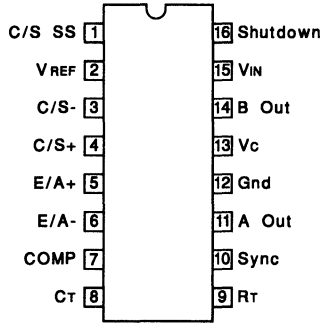
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... -0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... -30mA
Sync Output Current (Pin 10) ..... -5mA
Error Amplifier Output Current (Pin 7) ..... -5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=25°C 2000mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds ..... +300°C

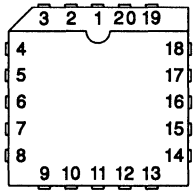
Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the speficied terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
V_{REF}	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
C_T	10
N/C	11
R_T	12
Sync	13
A Out	14
Gnd	15
N/C	16
Vc	17
B Out	18
V_{IN}	19
Shutdown	20

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J=25°C, I_O=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN}=8V to 40V		5	20		5	20	mV
Load Regulation	I_L=1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz≤ f ≤10kHz, T_J=25°C (Note 2)		100			100		μV
Long Term Stability	T_J=125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.) (Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	T_J=25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	ΔV_O=1.2 to 3V, V_{CM}=2V	80	105		80	105		dB
Unity Gain Bandwidth	T_J=25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		75	100		dB
PSRR	V_{IN}=8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		2	6		mA
Output Source Current	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM}=1V to 12V	60	83		60	83		dB
PSRR	V_{IN}=8V to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J=25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C=40V (Note 5)			200			200	µA
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=100mA	12	13.5		12	13.5		V
Rise Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

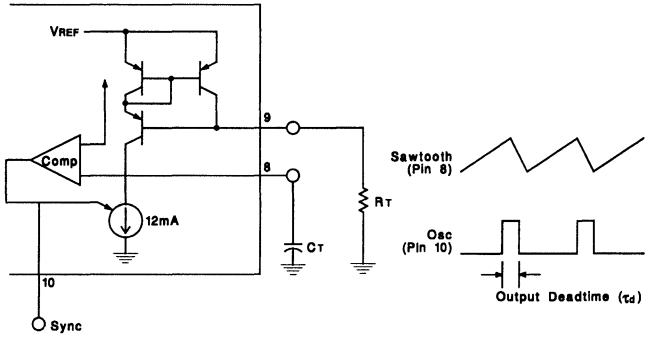
Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V.

Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$; $\Delta V_{PIN\ 4}$ = 0 to 1.0V.

Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



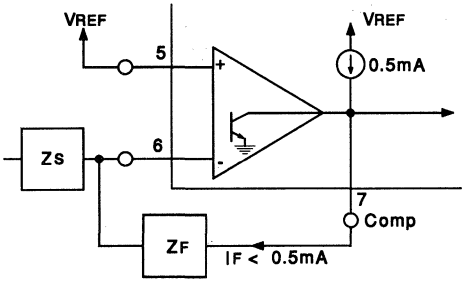
Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau_d\ (\mu s) = 145 C_T\ (\mu f) \left(\frac{12}{12 - \frac{3.6}{R_T\ (k\Omega)}} \right)$.

For large values of R_T: $\tau_d\ (\mu s) \approx 145 C_T\ (\mu f)$.

Oscillator frequency is approximated by the formula: $f_T\ (kHz) \approx \frac{2.2}{R_T\ (k\Omega) \cdot C_T\ (\mu f)}$.

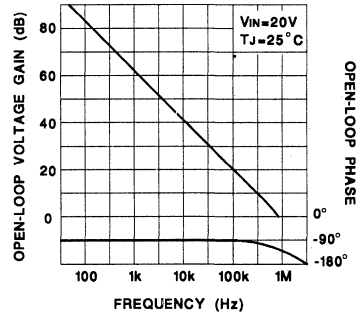
APPLICATIONS DATA (cont.)

Error Amp Output Configuration

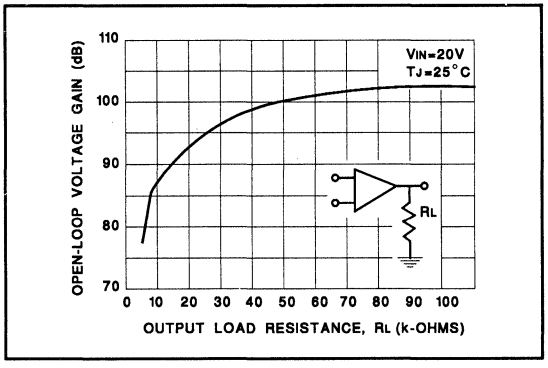


Error Amplifier can source up to 0.5mA.

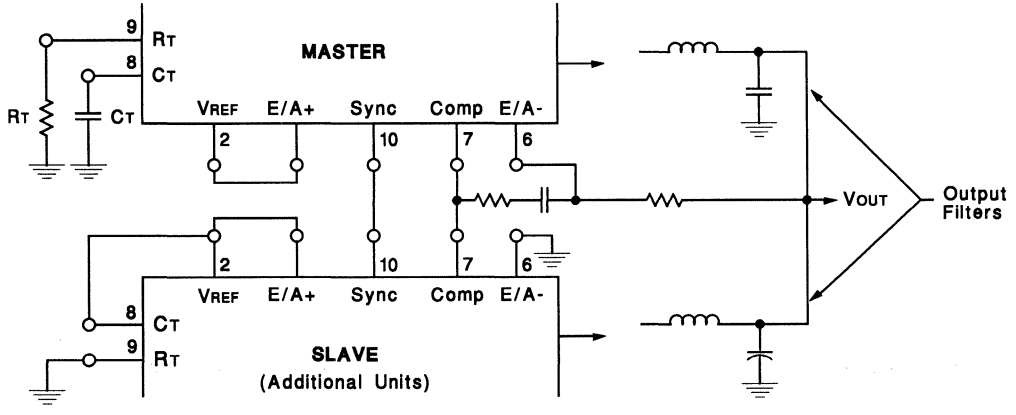
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance



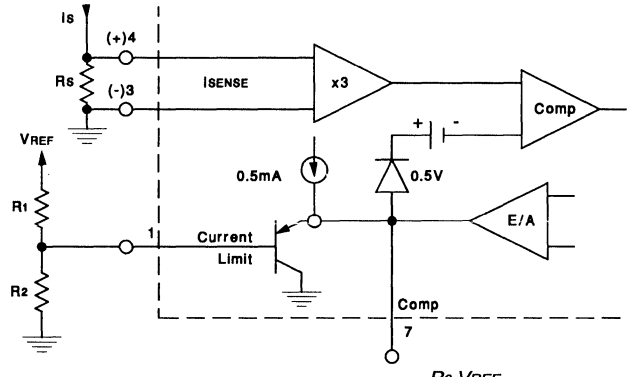
Parallel Operation



Slaving allows parallel operation of two or more units with equal current sharing.

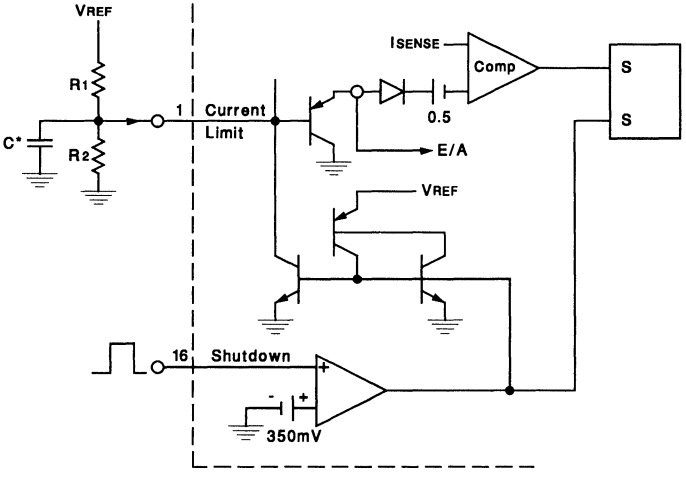
APPLICATIONS DATA (cont.)

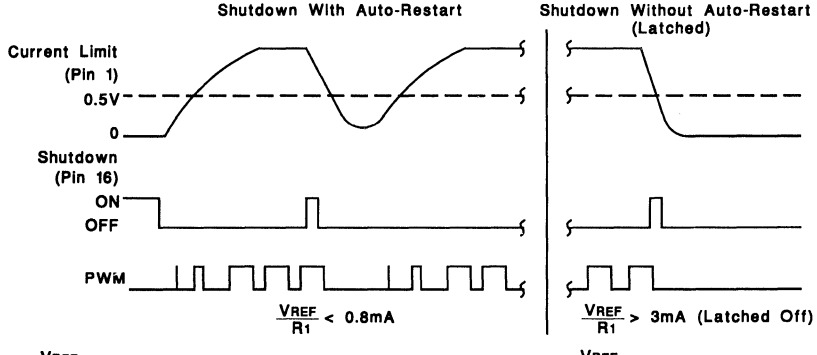
Pulse by Pulse Current Limiting



Peak Current (Is) is determined by the formula: $Is = \dfrac{\frac{R2\ VREF}{R1 + R2} - 0.5}{3Rs}$

Soft Start and Shutdown /Restart Functions





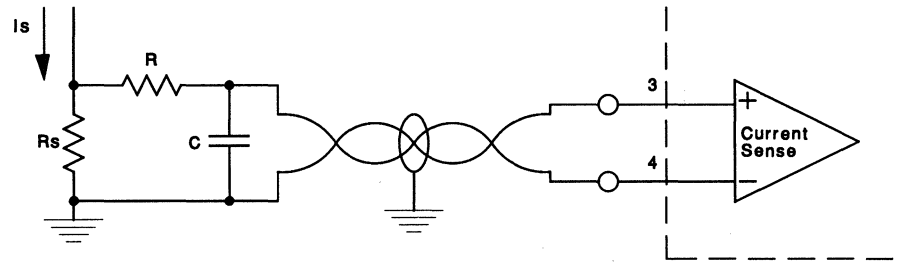
If $\frac{VREF}{R1}$ < 0.8mA, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{VREF}{R1}$ > 3mA, the device will latch off until power is recycled.

5

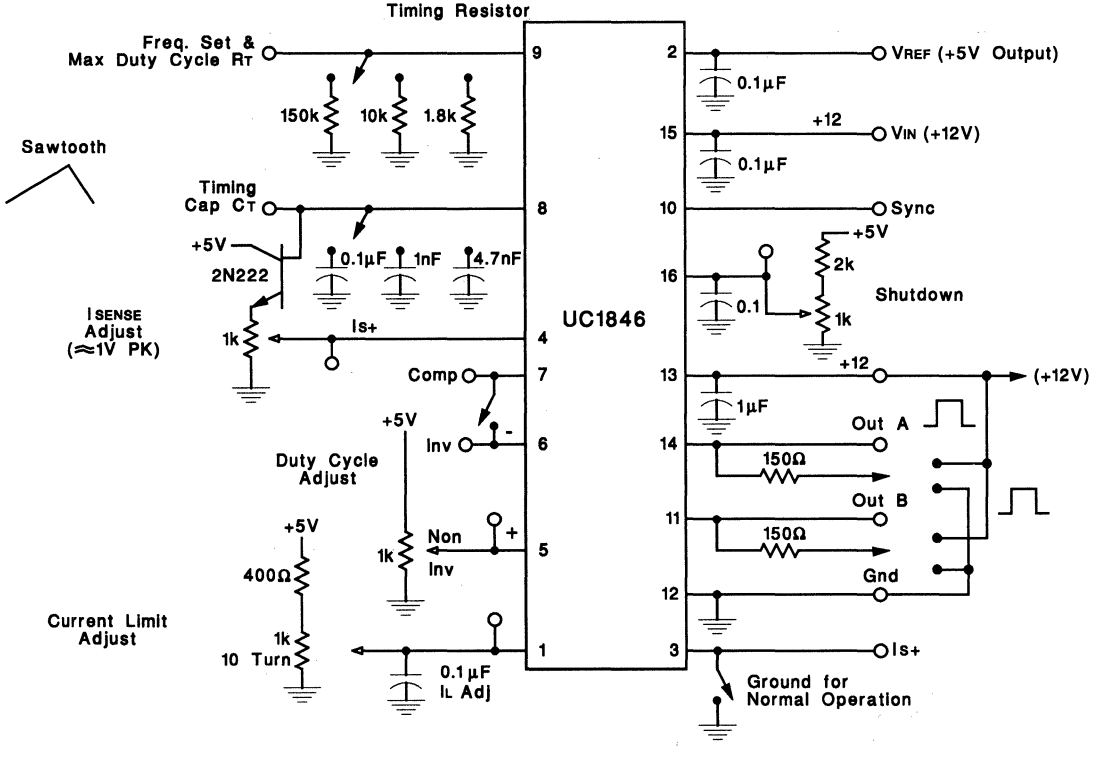
APPLICATIONS DATA (cont.)

Current Sense Amp Connection



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

UC1846 Open Loop Test Circuit



-Bypass Caps Should Be Low ESR & ESL Type
-Short Pins 6 & 7 for Unity Gain Testing

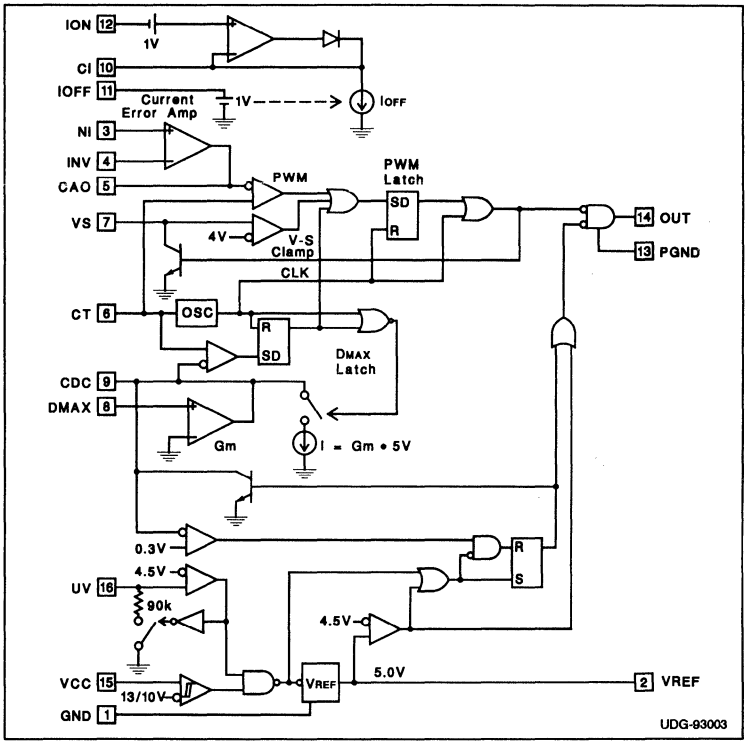
UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603)424-3460

Average Current Mode PWM Controller

FEATURES

- Practical Primary Side Control of Isolated Power Supplies with DC Control of Secondary Side Current
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second-Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Under Voltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Start-up Current (500μA)
- Precision 5V Reference (1%)

BLOCK DIAGRAM



DESCRIPTION

The UC1848 family of PWM control ICs makes primary side average current mode control practical for isolated switching converters. Average current mode control insures that both cycle by cycle peak switch current and maximum average inductor current is well defined and will not run away in a short circuit situation. The UC1848 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC1848 implements a patented technique of sensing secondary current in an isolated buck derived converter from the primary side. A Current Waveform Synthesizer monitors switch current and simulates the inductor current down slope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side allows for full DC control of output current.

The UC1848 circuitry includes a precision reference, a wide bandwidth Error Amplifier for average current control, an Oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current Output Driver. The Current Error Amplifier easily interfaces with an opto-isolator from a secondary side voltage sensing circuit.

A full featured Under Voltage Lockout (UVLO) circuit is contained in the UC1848. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500μA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second-product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

Both patents embodied in the UC1848 belong to Lambda Electronics Incorporated and are licensed for use in applications employing these devices.

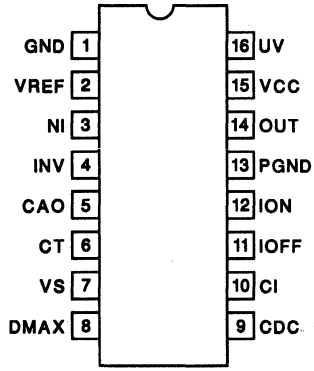
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15) 22V
Output Current, Source or Sink (Pin 14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground to Ground (Pin 1 to Pin 13) ..... ±0.2V
Analog Input Voltages
(Pins 3, 4, 7, 8, 12, 16) ..... -0.3 to 7V
Analog Input Currents, Source or Sink
(Pins 3, 4, 7, 8, 11, 12, 16) 1mA
Analog Output Currents, Source or Sink (Pins 5 & 10) ... 5mA
Power Dissipation at TA = 60°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

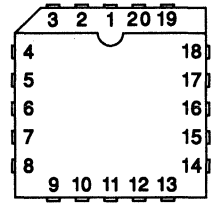
Notes: All voltages are with respect to ground (DIL and SOIC pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(Top View)
J or N, DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
GND	2
VREF	3
NI	4
INV	5
N/C	6
CAO	7
CT	8
VS	9
DMAX	10
N/C	11
CDC	12
CI	13
IOFF	14
ION	15
N/C	16
PGND	17
OUT	18
VCC	19
UV	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications are over the junction temperature range of -55°C to +125°C for the UC1848, -40°C to +85°C for the UC2848, and 0°C to +70°C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/µs
Iib			2	15	µA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	80		dB
Vio	12V ≤ VCC ≤ 20V, 0V ≤ VCM ≤ 5V			10	mV
Iib			0.5	3	µA
Voh	Io = -200µA	3	3.3		V
Vol	Io = 200µA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/µs

Note 1: Guaranteed by design, but not 100% tested in production.

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the junction temperature range of -55°C to +125°C for the UC1848, -40°C to +85°C for the UC2848, and 0°C to +70°C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100μA, CDC = 100nF, Cvs = 100pF, and Ivs = 400μA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency	T_A = 25°C	240	250	260	kHz
		225		275	kHz
Ramp Amplitude		1.6	1.8	2.0	V
Duty Cycle Clamp					
Max Duty Cycle	$V_{(DMAX)} = 0.75 \cdot V_{REF}$	72	75	78	%
Volt Second Clamp					
Max On Time		900		1100	ns
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.3	4.5	4.7	V
RHYSTERESIS	Vuv = 4.2V	77	90	103	kΩ
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	0 < Io < 10mA, 12 < VCC < 20	4.93		5.07	V
Line Regulation	12 < Vcc < 20V		2	10	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit Current	V_{REF} = 0V	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	CI = 1nF		20	45	ns
Output Low Saturation	Io = 20mA		0.25	0.4	V
	Io = 200mA		1.2	2.2	V
Output High Saturation	Io = -200mA		2.0	3.0	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Icc					
ISTART	VCC = 12V		0.3	0.5	mA
Icc (pre-start)	VCC = 15V, V(UV) = 0		0.5	1	mA
Icc (run)			22	27	mA

Note 1: Guaranteed by design, but not 100% tested in production.

UNDER VOLTAGE LOCKOUT

The Under Voltage Lockout block diagram is shown in Figure 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (500μA) and the output is low.

The UV comparator monitors input line voltage (V_{IN}). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$V_{IN(on)} = 4.5V \cdot (1 + Rv1/Rv2')$ and

$V_{IN(off)} = 4.5V \cdot (1 + Rv1/Rv2)$ where

$Rv2' = Rv2 | 190k$.

The resulting hysteresis is

$V_{IN(hys)} = 4.5V \cdot Rv1 / 90k$.

When the UV comparator is low, Icc is low (500μA) and the output is low.

UNDER VOLTAGE LOCKOUT (cont.)

When both the UV and VCC comparators are high, the internal bias circuitry for the rest of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

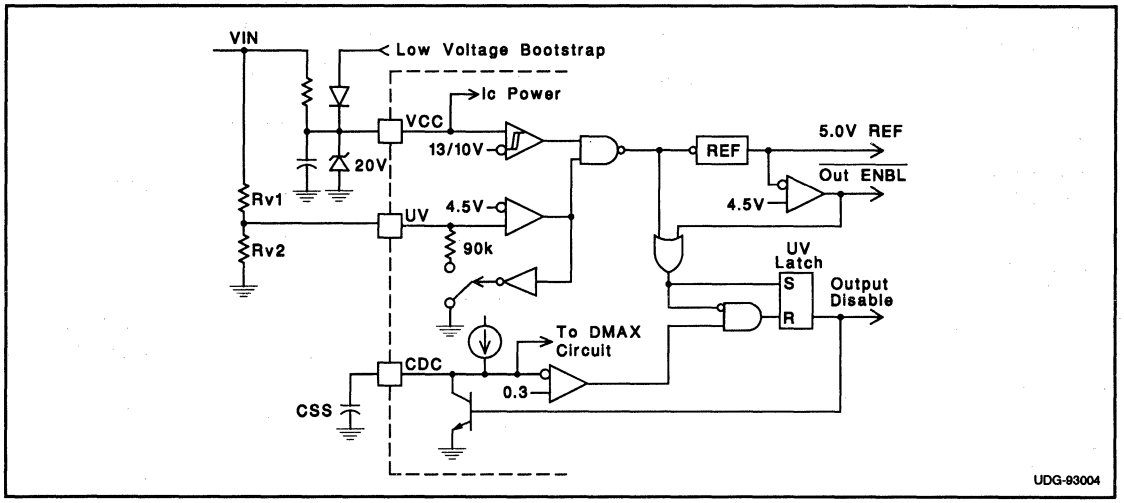


Figure 1: Under Voltage Lockout

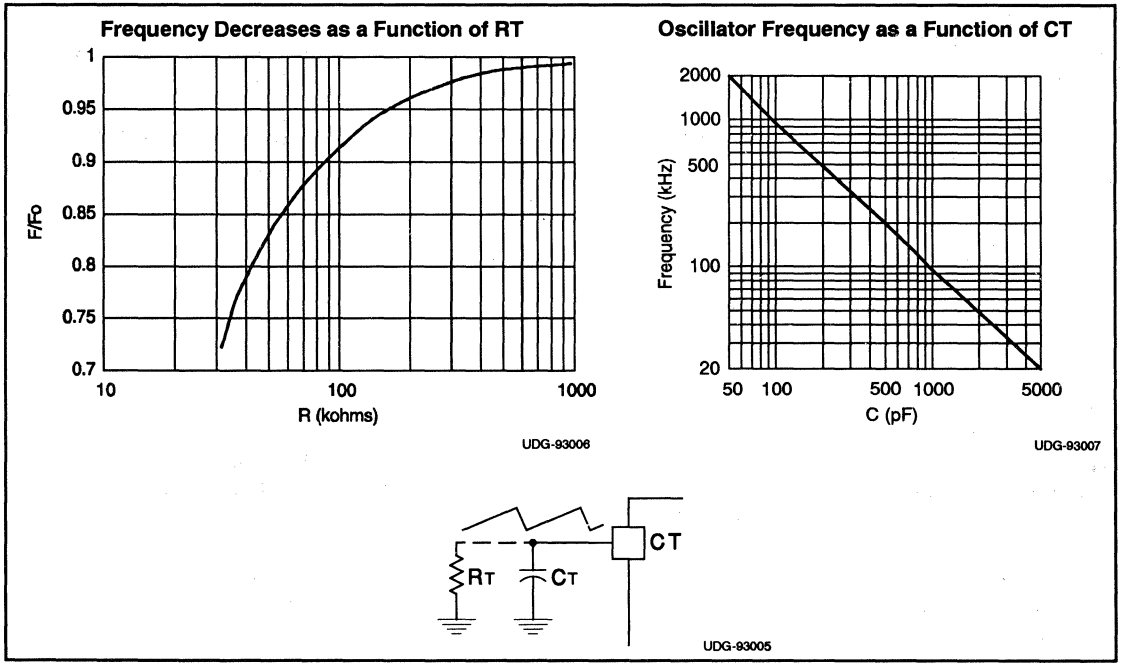


Figure 2: Oscillator Frequency

OSCILLATOR

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Figure 2. Frequency is determined by:

$$F = 1 / (10k \cdot CT).$$

The sawtooth wave shape is generated by a charging current of 200μA and a discharge current of 1800μA. The discharge time of the sawtooth is guaranteed dead time for the Output Driver. If maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If adjustment is required to overcome capacitor and chip tolerance, an additional trim resistor RT from CT to Ground can be used to adjust the oscillator frequency. RT should not be less than 40kohms. This will allow up to a 25% decrease in frequency.

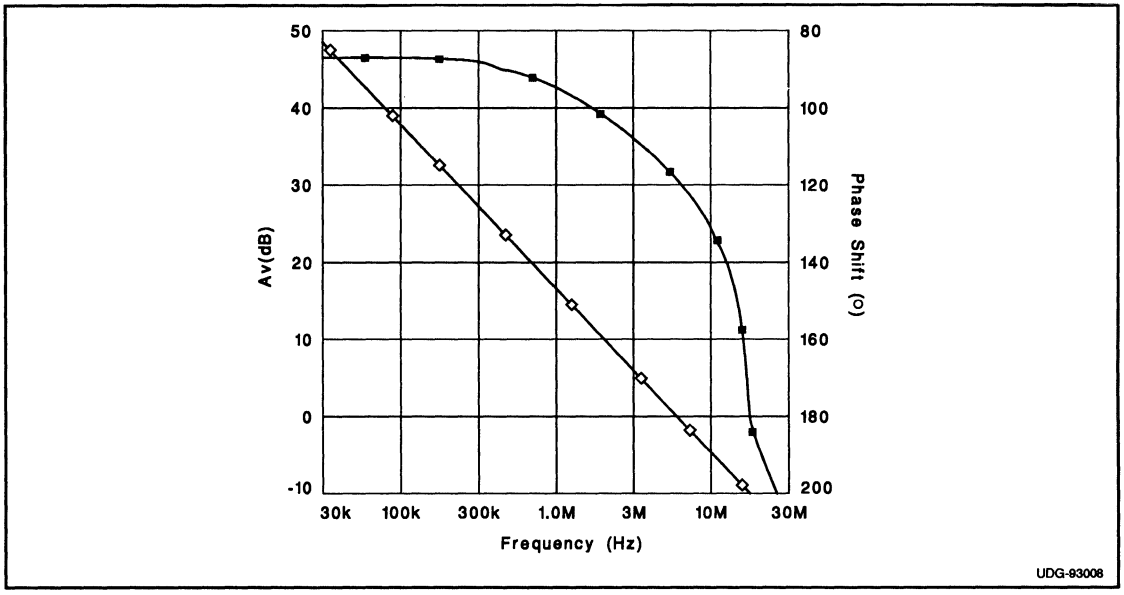


Figure 3: Error Amplifier Gain Phase Response over Frequency

INDUCTOR CURRENT WAVEFORM SYNTHESIZER

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope dIL/dt = –Vo/L. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented Current Waveform Synthesizer (Figure 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on-time switch current waveform. A programmable discharge current synthesizes the off-time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. Best utilization of the UC1848 is to translate maximum average inductor current to a 4 volt signal level. Given N and Ns (the turns ratio of the power and current sense transformers), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$Rs = 4V \cdot Ns \cdot N / IL(max).$$

Restated, the maximum average inductor current will be limited to:

$$IL(max) = 4V \cdot Ns \cdot N/Rs.$$

IOFF and CI need to be chosen so that the ratio of dV(CI)/dt to dIL/dt is the same during switch off-time as on-time. Recommended nominal off current is 100μA. This requires

$$CI = (100\mu A \cdot N \cdot Ns \cdot L) / (Rs \cdot Vo(nom))$$

INDUCTOR CURRENT WAVEFORM SYNTHESIZER (cont.)

where L is the output inductor value and Vo(nom) is the converter regulated output voltage.

IOFF can be programmed in several manners. If accurate average current control is required during short circuit operation, the IOFF must track output voltage. The method in Figure 4 derives a voltage proportional to VIN • D (Duty Cycle). (In a buck converter, output voltage is proportional to VIN • D.) A resistive loaded diode connection to the bootstrap winding yields a square wave that is proportional in amplitude to VIN and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated Vo. A single pole filter is shown, but in practice a two or three pole filter can do a better job of transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI down slope.

If the system is not sensitive to short circuit requirements, Figure 5 shows the simplest method of downslope generation: a single resistor (ROFF = 40k) from IOFF to VREF. The discharge current is then 100µA. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor down slope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Figure 6). When the power switch is off and inductor current is in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are it's inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining required isolation makes this a more costly solution. In the example, ROFF = Vo / 100µA. The 4 • ROFF resistor

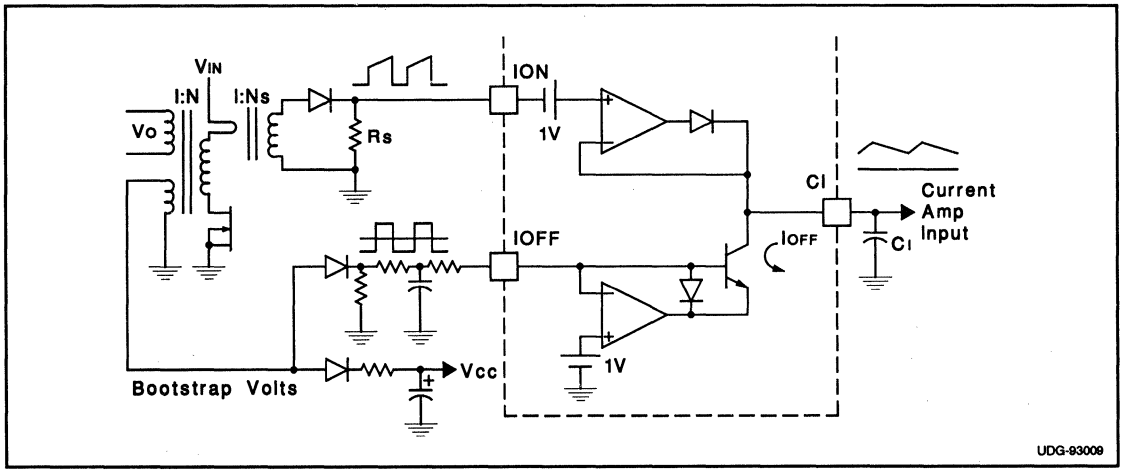


Figure 4: Inductor Current Waveform Synthesizer

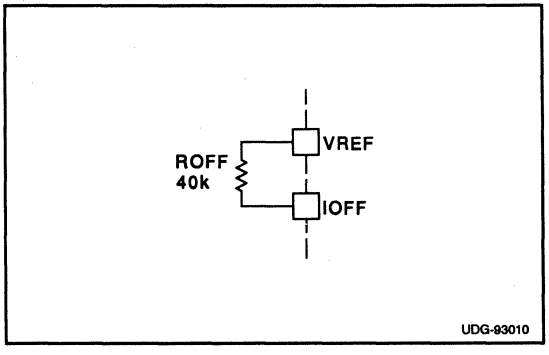


Figure 5: Fixed IOFF

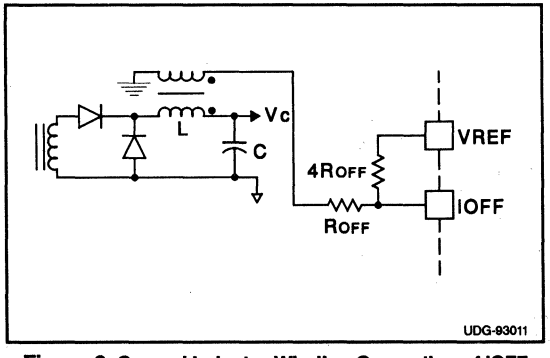


Figure 6: Second Inductor Winding Generation of IOFF

MAXIMUM VOLT-SECOND CIRCUIT

A maximum Volt-Second-Product can be programmed by a resistor (Rvs) from VS to VIN and a capacitor (Cvs) from VS to ground (Figure 7). VS is discharged while the switch is off. When the output turns on, VS is allowed to charge. Since the threshold of the VS comparator is much less than VIN, the charging profile at Vs will be essentially linear. If VS crosses the 4.0V threshold before the PWM turns the output off, the VS comparator will turn the output off for the remainder of the cycle. The maximum Volt-Second-Product is

$$V_{IN} \bullet T_{ON}(max) = 4.0V \bullet Rvs \bullet Cvs.$$

MAXIMUM DUTY CYCLE AND SOFT START

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Figure 7). The value programmed is:

$$D(max) = Rd1 / (Rd1 + Rd2).$$

For proper operation, the integrating capacitor, Cd, should be larger than Cd(min) > T(osc) / 80k, where T(osc) is the Oscillator period. Cd also sets the soft start time constant, so values of Cd larger than minimum may be desired. The soft start time constant is approximately:

$$I(ss) = 20k \bullet Cd.$$

GROUND PLANES

The output driver on the UC1848 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Figure 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which to PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low esr/esl ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, and CI should likewise be connected to the signal ground plane.

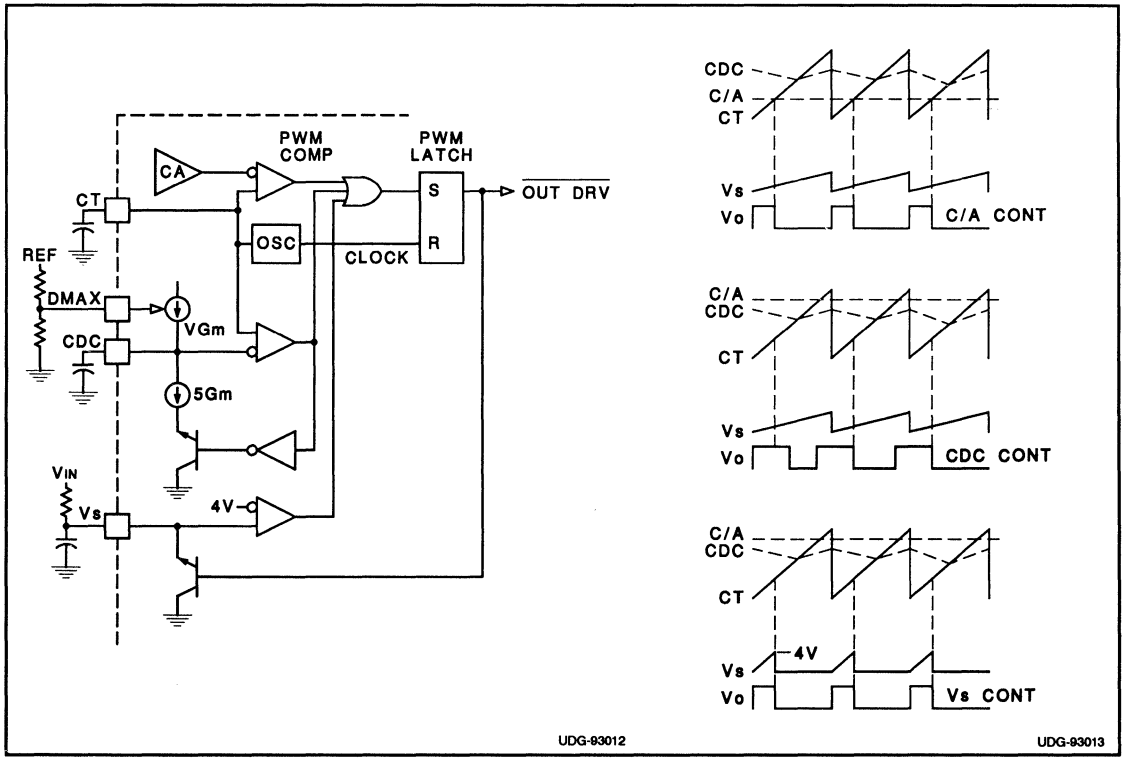


Figure 7: Duty Cycle Control

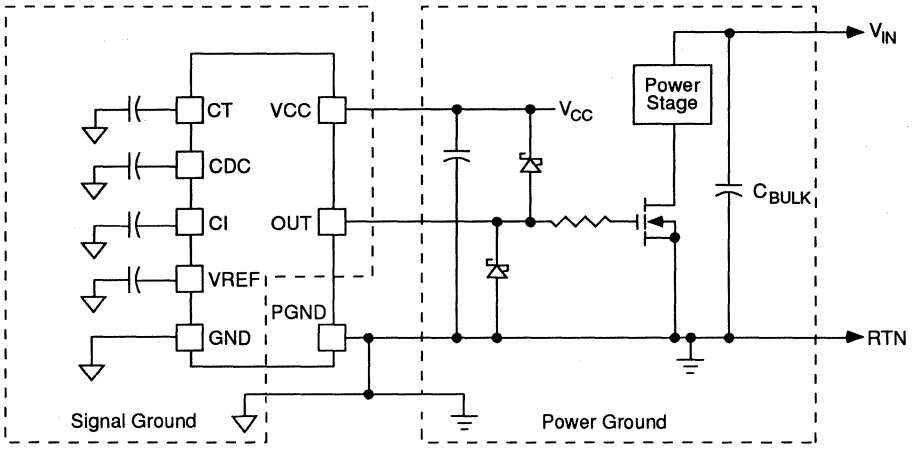


FIGURE 8: GROUND PLANE CONSIDERATIONS

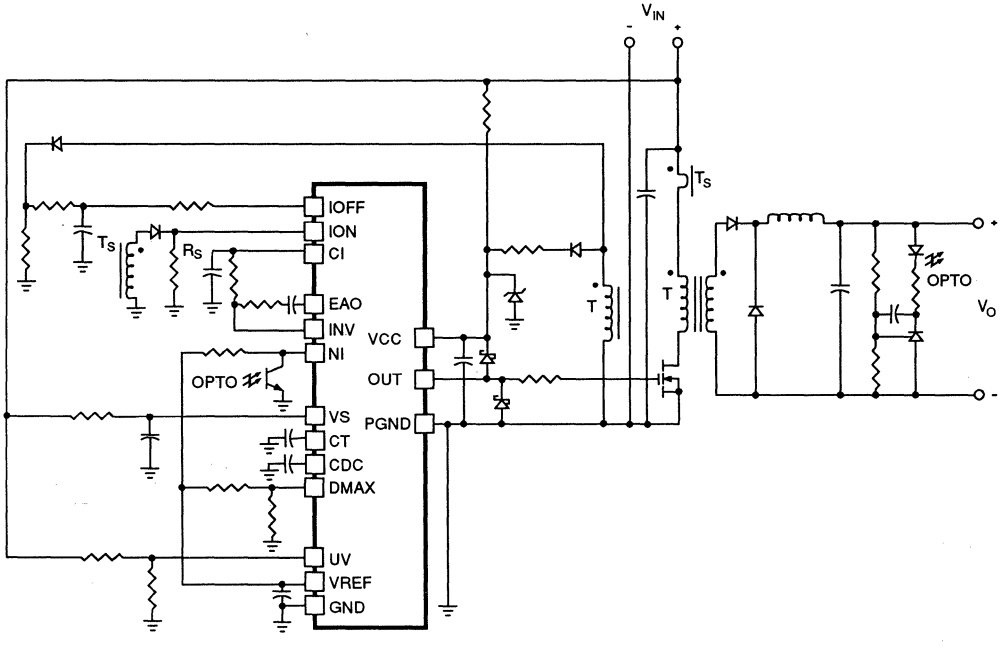


FIGURE 9: TYPICAL APPLICATION - AN AVERAGE CURRENT - MODE ISOLATED FORWARD CONVERTER

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INTEGRATED CIRCUITS
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UC1851
UC2851
UC3851

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

DESCRIPTION

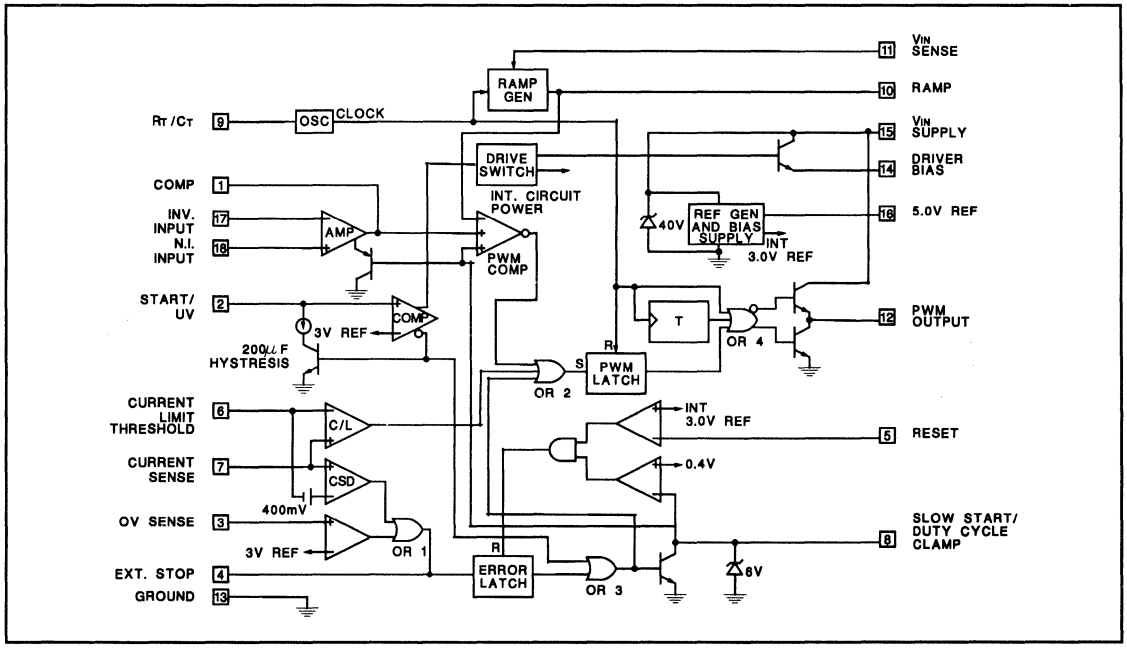
The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -25°C to +85°C and 0°C to +70°C, respectively.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +VIN (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

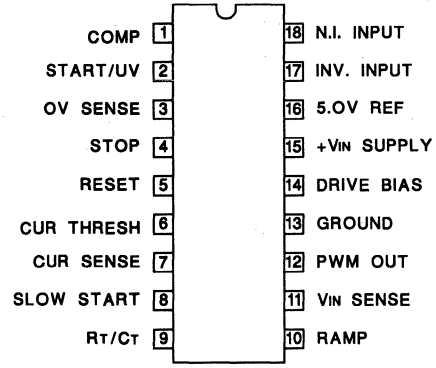
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20μJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Stop Input (Pin 4) ..... -0.3 to +5.5V

Comparator Inputs
(Pins 1–7, 9–11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

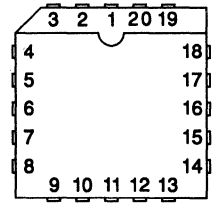
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L PACKAGE



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
COMP	1
START/UV	2
OV SENSE	3
STOP	4
RESET	5
CUR THRESH	7
CUR SENSE	8
SLOW START	9
RT/CT	10
RAMP	11
VIN SENSE	12
PWM OUT	13
GROUND	14
DRIVE BIAS	15
+VIN SUPPLY	17
5.0V REF	18
INV. INPUT	19
N.I. INPUT	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	V_{IN} = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

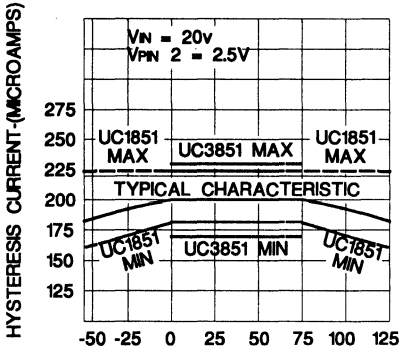
PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10μA		-11	-14		-11	-14	μA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	μA
Input Offset Current				0.5			0.5	μA
Open Loop Gain	ΔVo = 1 to 3V	60	66		60	66		dB
Output Swing (Max Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 1)	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate (Note 1)	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/μs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	I_{SOURCE} = 20mA	18	18.5		18	18.5		V
	I_{SOURCE} = 200mA	17	18.5		17	18.5		V
Rise Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Fall Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Comparator Delay (Note 1)	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	μA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	μA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	μA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	μA
Driver Bias Saturation Voltage, V_{IN}-V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	μA
Slow-Start Saturation	Is = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	Vs = 4.5V		0.1	2.0		0.1	2.0	μA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	μA
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 1)	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

Note 1:Guaranteed by design. Not 100% tested in production.

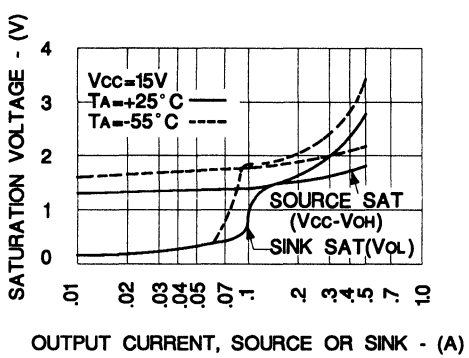
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{Kc}{R_T C_T}$ where Kc is a first-order correction factor ~ 0.3 log ($C_T \times 10^{12}$).
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dv}{dT} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley duty cycle. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200μA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by RsCs for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/μF.

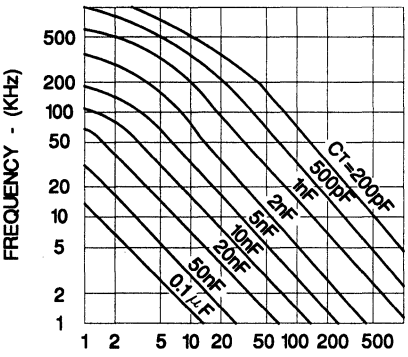
Start/UV Hysteresis Current



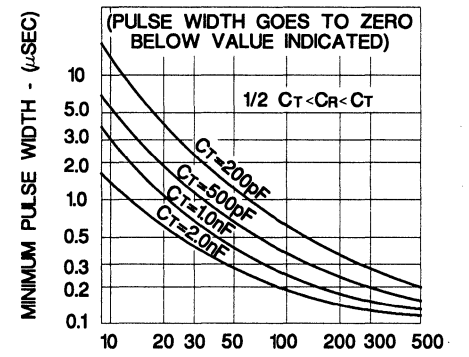
Output Saturation Characteristics



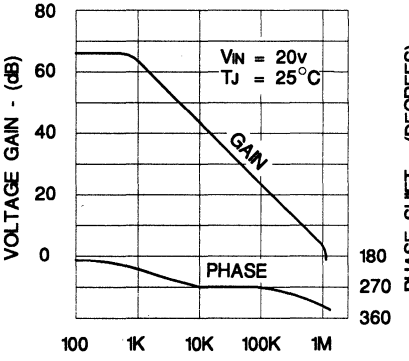
Oscillator Frequency



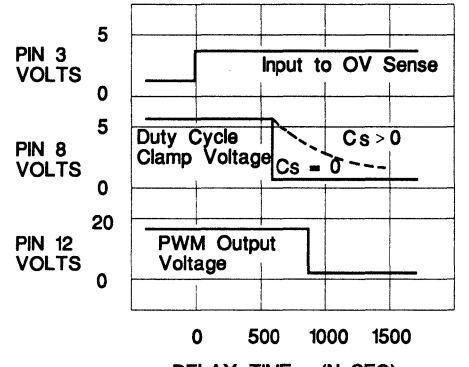
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



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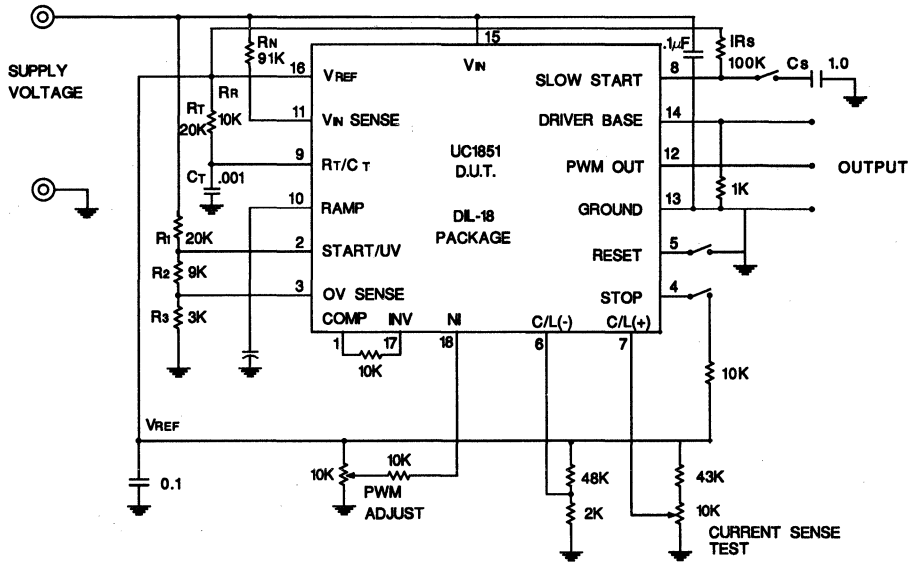
OPEN-LOOP CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50kHz

Start Voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$ +0.2R1 = 12V

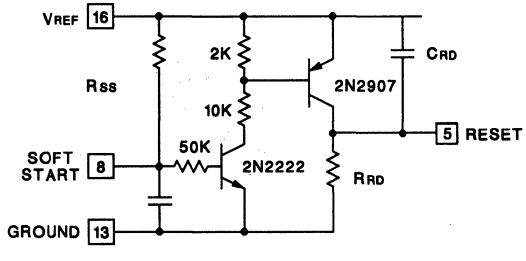
UV Fault Voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$ = 8V

OV Fault Voltage = $3\left(\frac{R1 + R2 + R3}{R3}\right)$ = 32V

Current Limit = 200mV
Current Fault Voltage = 600mV
Duty Cycle Clamp = 50%
@VIN = 15V, Duty Cycle = 48%
@VIN = 30V, Duty Cycle = 24%

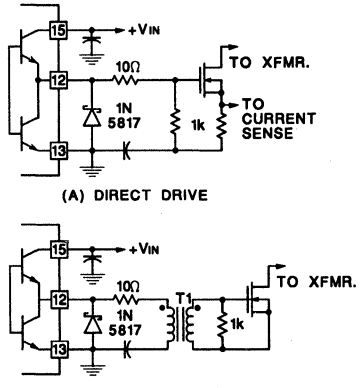
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Programmable Soft Start and Restart Delay Circuit



For further application information see UC1840/UC1841 Data Sheets

UC1851 Power MOSFET Drive Interface



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INTEGRATED CIRCUITS

UNITRODE

High Power-Factor Preregulator

UC1852
UC2852
UC3852

FEATURES

- Low-Cost Power Factor Correction
- Power Factor Greater Than 0.99
- Few External Parts Required
- Controlled On-Time Boost PWM
- Zero-Current Switching
- Limited Peak Current
- Min and Max Frequency Limits
- Starting Current Less Than 1mA
- High-Current FET Drive Output
- Under-Voltage Lockout

DESCRIPTION

The UC1852 provides a low-cost solution to active power-factor correction (PFC) for systems that would otherwise draw high peak current pulses from AC power lines. This circuit implements zero-current switched boost conversion, producing sinusoidal input currents with a minimum of external components, while keeping peak current substantially below that of fully-discontinuous converters.

The UC1852 provides controlled switch on-time to regulate the output bulk DC voltage, an off-time defined by the boost inductor, and a zero-current sensing circuit to reactivate the switch cycle. Even though switching frequency varies with both load and instantaneous line voltage, it can be maintained within a reasonable range to minimize noise generation.

While allowing higher peak switch currents than continuous PFCs such as the UC1854, this device offers less external circuitry and smaller inductors, yet better performance and easier line-noise filtering than discontinuous current PFCs with no sacrifice in complexity or cost. The ability to obtain a power factor in excess of 0.99 makes the UC1852 an optimum choice for low-cost applications in the 50 to 500 watt power range. Protection features of these devices include under-voltage lockout, output clamping, peak-current limiting, and maximum-frequency clamping.

The UC1852 family is available in 8-pin plastic and ceramic dual in-line packages, and in the 8-pin small outline IC package (SOIC). The UC1852 is specified for operation from -55°C to +125°C, the UC2852 is specified for operation from -40°C to +85°C, and the UC3852 is specified for operation from 0°C to +70°C.

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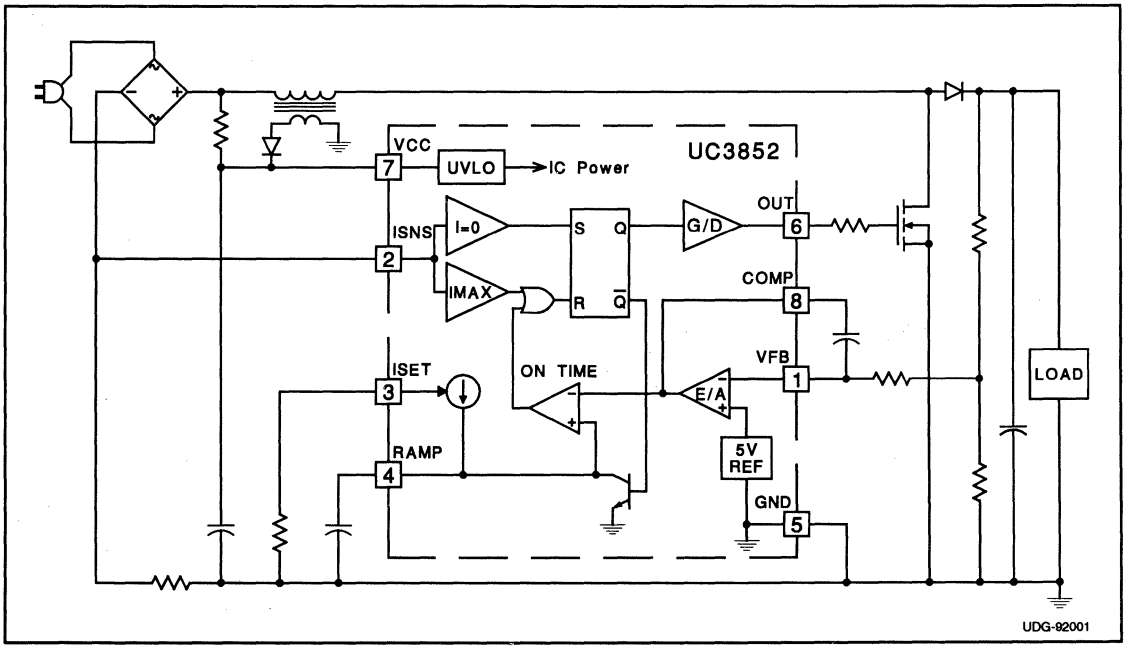
TYPICAL APPLICATION



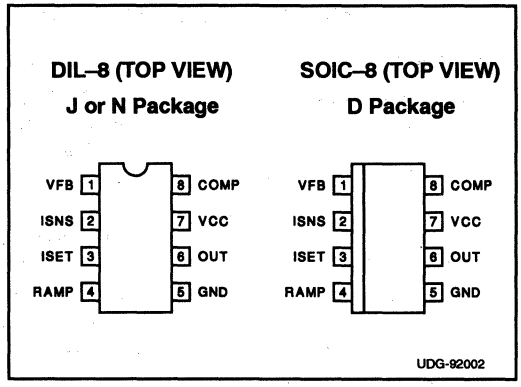
12/92

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low-impedance Source) 30.0V
Supply Current (High-impedance Source) 30.0mA
OUT Current, Peak ..... ±1.0A
OUT Energy, Capacitive Load 5.0µJ
Input Voltage, ISNS ..... ±5.0V
Input Voltage, VFB ..... –0.3V to +10.0V
COMP Current ..... ±10.0mA
ISET Current ..... –10.0mA
Power Dissipation at Ta≤25°C (Note 3) 1.0W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages with respect to GND (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: Refers to DIL-8 Package. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

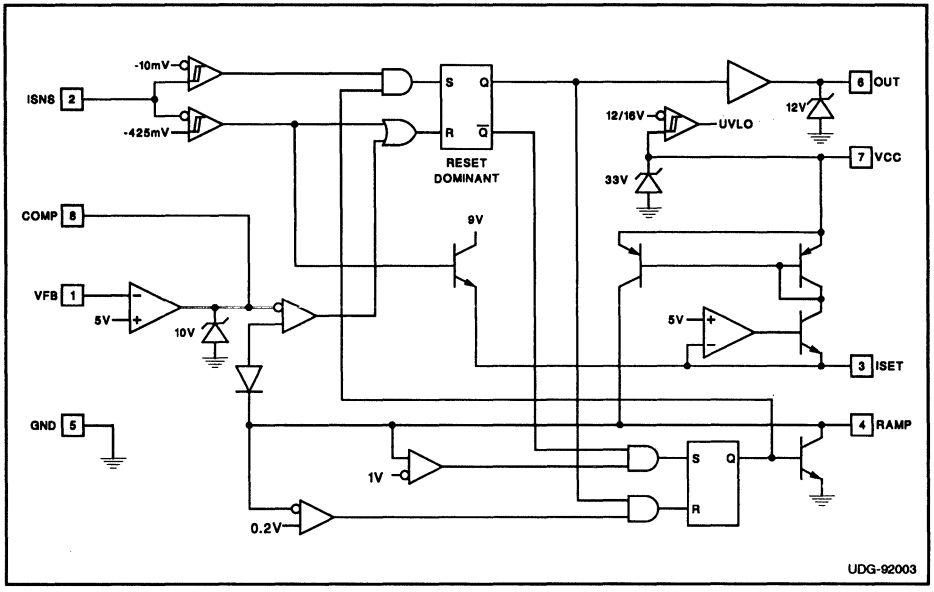


ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=24V, ISET=50kΩ to GND, RAMP=1nF to GND, ISNS= –0.1V, VFB connected to COMP, no load on OUT, –55°C<Ta<+125°C for the UC1852, –40°C<Ta<+85°C for the UC2852, and 0°C<Ta<+70°C for the UC3852, and Ta=Tj.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timer Section					
ISET Voltage		4.5	5.0	5.5	V
RAMP Charge Current	RAMP=2.5V	88	98	108	µA
RAMP Discharge Current	ISNS= –1.0V, RAMP=1.0V	12	28	50	mA
RAMP Saturation Voltage	ISNS= –1.0V, IRAMP=100µA		0.006	0.200	V
RAMP Threshold - Maximum Frequency	VFB=10V, COMP open	0.92	1.02	1.12	V
RAMP Threshold - PWM Comparator		3.9	4.3	4.8	V
Current Sense Comparator					
ISNS Restart Threshold		–18	–10	–4	mV
ISNS Fault Threshold		–550	–450	–350	mV
ISNS Input Current		–100	–30	100	µA
Error Amplifier Section					
VFB Input Voltage		4.6	5.0	5.3	V
VFB Input Bias Current		–5.00	–0.03	5.00	µA
COMP Sink Current	COMP=7.5V	10			mA
COMP Source Current	COMP=2.5V	–300	–175	–100	µA
COMP Clamp Voltage	VFB=0.0V, COMP open	9.2	10.0	10.6	V
OUT Output					
OUT Saturation Voltage High	VCC=13V, IOUT= –200mA, RAMP=2V	0.5	1.7	2.5	V
OUT Saturation Voltage Low	IOUT=200mA, ISNS= –1.0V	0.5	1.6	2.2	V
OUT Saturation Voltage Low @ 10mA	IOUT=10mA, ISNS= –1.0V		0.05	0.40	V
OUT Clamp Voltage	IOUT= –200mA, RAMP=2V	10.0	12.0	14.5	V
OUT Voltage during UVLO	IOUT=100mA, VCC=0V	0.5	1.0	2.2	V
Overall Section					
Inactive Supply Current	VCC=10V	0.2	0.4	1.0	mA
Active Supply Current		3.0	6.0	10.0	mA
VCC Clamp Voltage	ICC=25mA	30	33	36	V
VCC Turn-On Threshold		14.5	16.3	17.5	V
VCC Turn-Off Threshold		10.5	11.5	13.0	V
VCC Threshold Hysteresis		3	5	7	V

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. To limit PWM on-time, this pin is clamped to approximately 10V. To implement soft start, the COMP pin can be pulled low and ramped up with a PNP transistor, a capacitor, and a resistor.

GND: Ground for all functions is through this pin.

ISET: The dominant function is of this pin is to program RAMP charging current. RAMP charging current is approximately 5V divided by the external resistor placed from ISET to ground. Resistors in the range of 10kΩ to 50kΩ are recommended, producing currents in the range of 100μA to 500μA.

A second function of ISET is as reference output. The ISET pin is normally regulated to 5V ±10%. It is critical that this pin only see the loading of the RAMP programming resistor, but a high input-impedance comparator or amplifier may be connected to this pin or to a tap on the RAMP programming resistor if required.

The third function of the ISET pin is as a FAULT output. In the event of an over-current fault, the ISET pin is forced to approximately 9V by the fault comparator. This can be used to trip an external protection circuit which can disable the load or start a fault restart cycle.

ISNS: This input to the zero and over current comparators is specially built to allow operation over a ±5V dynamic range. In noisy systems or systems with very high Q inductors, it is desirable to filter the signal entering the ISNS input to prevent premature restart or fault cycles. For best accuracy, ISNS should be connected to a current sense resistor through no more than 200 ohms.

OUT: The output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±500mA. To prevent damage to the power MOSFET, the OUT pin is internally driven by a 12V supply. However, lead inductance between the OUT pin and the load can cause overshoot and ringing. External current boost transistors will increase this overshoot and ringing. If there is any significant distance between the IC and the MOSFET, external clamp diodes and/or series damping resistors may be required. OUT is actively held low when the VCC is below the UVLO threshold.

RAMP: A controlled on-time PWM requires a timer whose time can be modulated by an external voltage. The timer current is programmed by a resistor from ISET to GND. A capacitor from RAMP to GND sets the on time in conjunction with the voltage on COMP. Recommended values for the timer capacitors are between 100pF and 1nF.

VCC: VCC is the logic and control power connection for this device. VCC current is the sum of active device supply current and the average OUT current. Knowing the maximum operating frequency and the MOSFET gate charge (Qg), average OUT current can be estimated by:

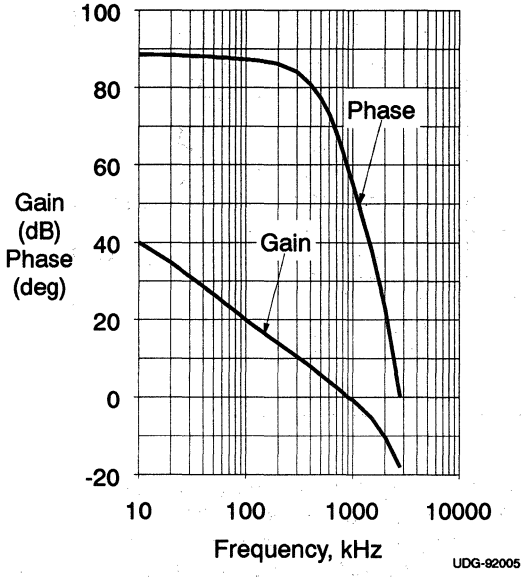
$$I_{OUT} = Q_g \times F$$

To prevent noise problems, bypass VCC to GND with both a ceramic and an electrolytic capacitor.

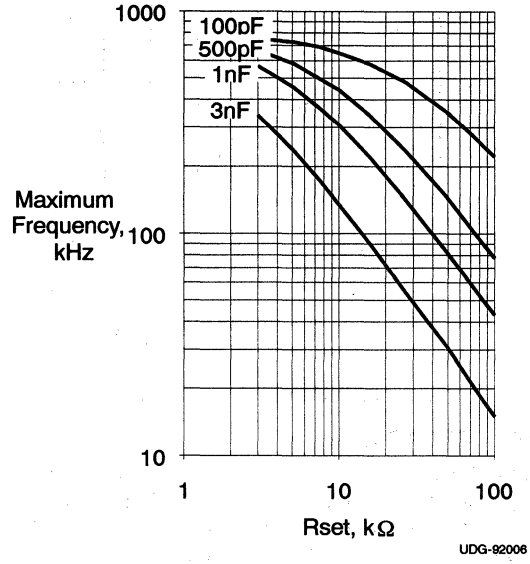
VFB: VFB is the error amplifier inverting input. This input serves as both the voltage sense input to the error amplifier and as the other compensation point for the error amplifier.

TYPICAL CHARACTERISTICS

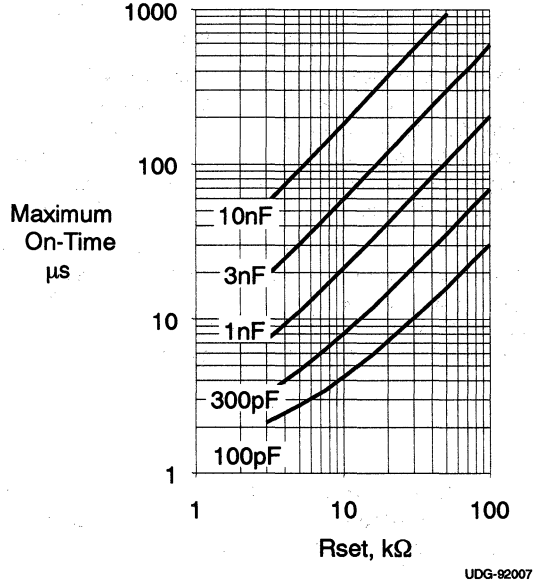
Error Amplifier Gain and Phase



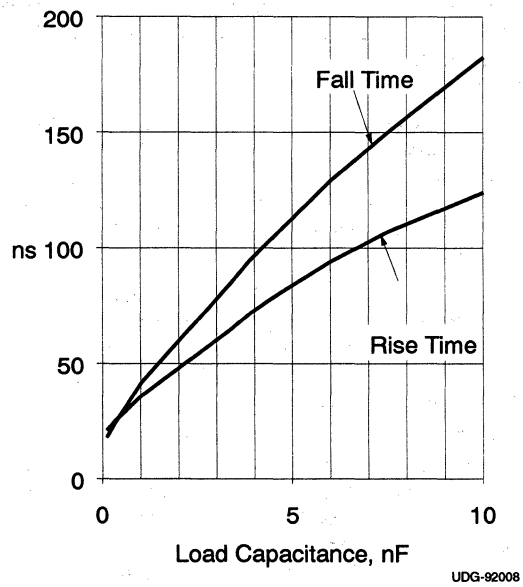
Max Frequency vs. Rset and Ct



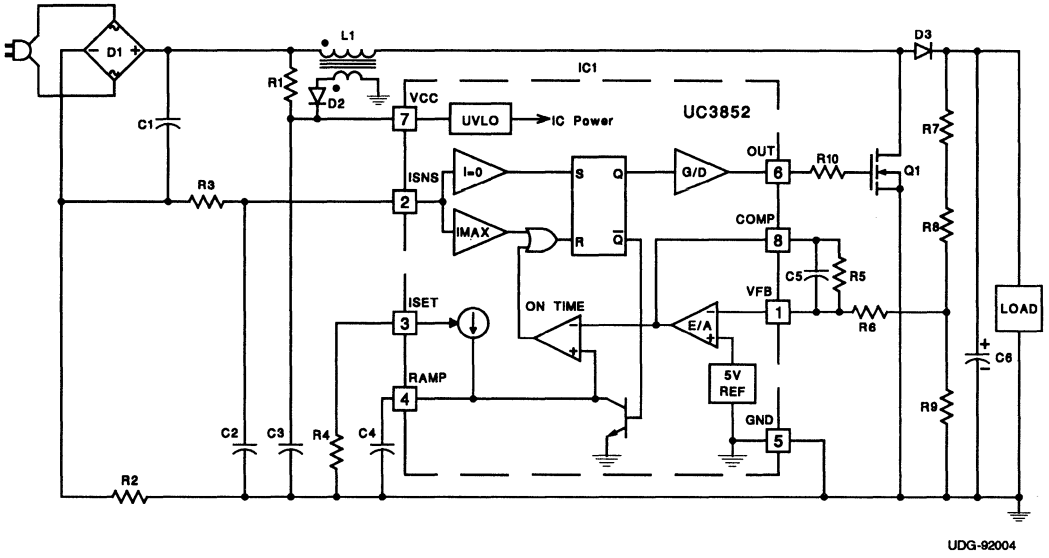
Max On-Time vs. Rset and Ct



OUT Rise and Fall Time



APPLICATION INFORMATION: A 100 Watt



This circuit demonstrates a complete power factor preregulator based on the UC3852. This preregulator will supply up to 100 watts at 400VDC and exhibit power factor greater than 0.995 with less than 10% total harmonic distortion. Operating input range is 90V to 160V RMS at 50Hz to 60Hz.

This design is intentionally simple, yet fully functional. The UC3852 can also be used in designs featuring soft start, over-voltage protection, wide power-line voltage operation, and fault latching. For more information on applying the UC3852, refer to Unitrode Application Note U–132.

PARTS LIST

C1	0.47µF/250VAC X2 Class Polyester
C2	1nF/16V Ceramic
C3	68µF/35V Aluminum Electrolytic
C4	180pF/16V Ceramic
C5	0.1µF/16V Polyester or Ceramic
C6	82µF/450V Aluminum Electrolytic
D1	2A/500V Bridge Rectifier (Collmer KBPC106 or Powertex MB11A02V60)
D2	100mA/50V Switching Diode (1N4148)
D3	2A/500V 250ns Recovery-Time Rectifier (Motorola MR856)
IC1	UC3852N Power Factor Controller IC
Q1	IRF830 4.5A/500V 1.5Ω Power FET
L1	680µH (Renco RL3792 with 10 Turn 24 AWG Secondary)
R1	150kΩ, ¼W
R2	0.2Ω, ½W Carbon Composition
R3	10Ω, ¼W
R4	13.3kΩ, ¼W
R5	1MΩ, ¼W
R6	20kΩ, ¼W
R7	200kΩ, ½W
R8	200kΩ, ½W
R9	5.1kΩ, ¼W
R10	12Ω, ¼W

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INTEGRATED CIRCUITS
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High Power Factor Preregulator

UC1854
UC2854
UC3854

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion To <5%
- World-Wide Operation Without Switches
- Feed-Forward Line Regulation
- Average Current-Mode Control
- Low Noise Sensitivity
- Low Start-Up Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier/Divider
- 1A Totem-Pole Gate Driver
- Precision Voltage Reference

DESCRIPTION

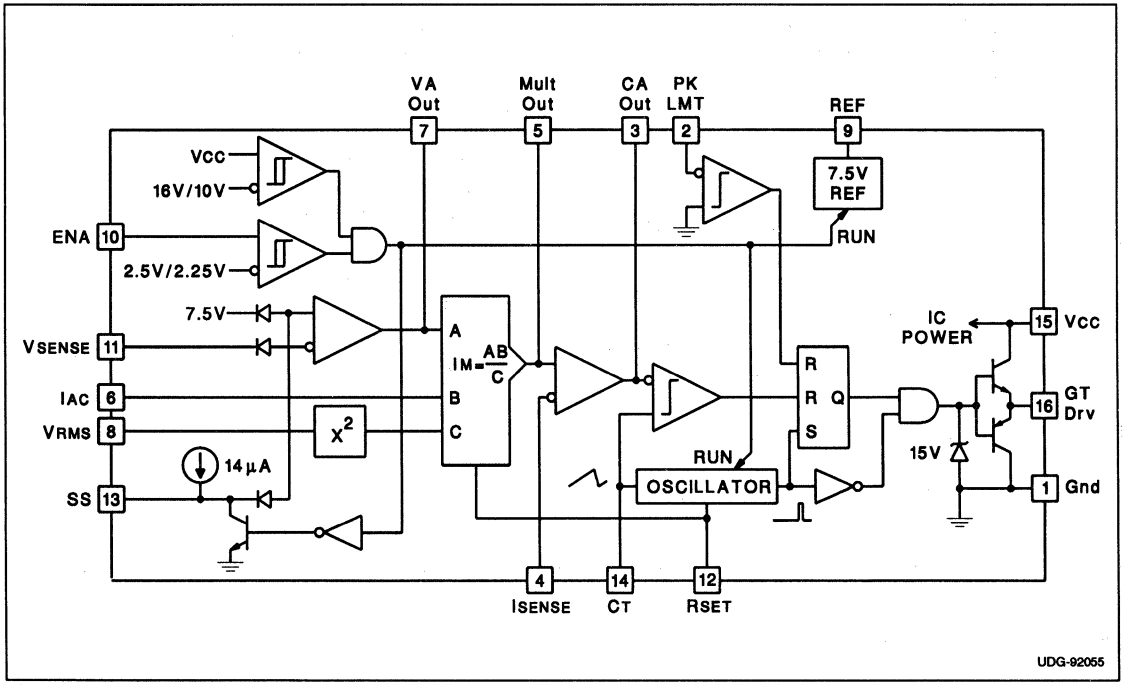
The UC1854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC1854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

The UC1854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The UC1854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC1854 can be used in single and three phase systems with line voltages that vary from 75 to 275 volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 features low starting supply current.

These devices are available packaged in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

BLOCK DIAGRAM



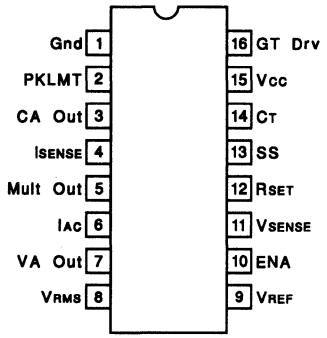
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc 35V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, VSENSE, VRMS 11V
Input Voltage, ISENSE, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, RSET, IAC, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

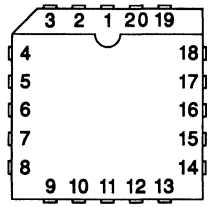
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA input is internally clamped to approximately 14V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAM

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
ISENSE	5
N/C	6
Mult Out	7
IAC	8
VA Out	9
VRMS	10
N/C	11
VREF	12
ENA	13
VSENSE	14
RSET	15
N/C	16
SS	17
CT	18
VCC	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=18V, RT=8.2k, CT=1.5nF, PKLMT=1V, VRMS=1.5V, IAC=100µA, ISENSE=0V, CA Out=4V, VA Out=3.5V, VSENSE=3V, –55°C<TA<125°C for the UC1854A/B, –40°C<TA<85°C for the UC2854A/B, and 0°C<TA<70°C for the UC3854A/B, and TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	ENA=0V		1.5	2.0	mA
Supply Current, On			10	16	mA
Vcc Turn-On Threshold		14.5	16	17.5	V
Vcc Turn-Off Threshold		9	10	11	V
ENA Threshold, Rising		2.4	2.55	2.7	V
ENA Threshold Hysteresis		0.2	0.25	0.3	V
ENA Input Current	ENA=0V	–5.0	–0.2	5.0	µA
VRMS Input Current	VRMS=5V	–1.0	–.01	1.0	µA
VOLTAGE AMPLIFIER					
Voltage Amp Offset Voltage	VA Out=3.5V	–8		8	mV
VSENSE Bias Current	VSENSE=0V	–500	–25	500	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Output Swing			0.5 to 5.8		V
Voltage Amp Short Circuit Current	VA Out=0V	–30	–12	–5	mA
SS Current	SS=2.5V	–20	–14	–6	µA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLMT=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GT Drv, –55°C<T_A<125°C for the UC1854, –40°C<T_A<85°C for the UC2854, and 0°C<T_A<70°C for the UC3854, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER					
Current Amp Offset Voltage		–4		4	mV
I_{SENSE} Bias Current		–500	–120	500	nA
Input Range, I_{SENSE}, Mult Out		–0.3 to 2.5			V
Current Amp Gain		80	110		dB
Current Amp Output Swing			0.5 to 16		V
Current Amp Short Circuit Current	CA Out=0V	–30	–12	–5	mA
Current Amp Gain-BW Product	T_A=25°C	400	800		kHz
REFERENCE					
Reference Output Voltage	I_{REF}=0mA, T_A=25°C	7.4	7.5	7.6	V
	I_{REF}=0mA, Over Temp.	7.35	7.5	7.65	V
V_{REF} Load Regulation	–10mA<I_{REF}<0mA	–15	5	15	mV
V_{REF} Line Regulation	15V<Vcc<35V	–10	2	10	mV
V_{REF} Short Circuit Current	REF=0V	–50	–28	–12	mA
MULTIPLIER					
Mult Out Current I_{AC} Limited	I_{AC}=100µA, R_{SET}=10k	–220	–200	–180	µA
Mult Out Current Zero	I_{AC}=0µA, R_{SET}=15k	–2.0	–0.2	2.0	µA
Mult Out Current R_{SET} Limited	I_{AC}=450µA, R_{SET}=15k	–280	–255	–220	µA
Mult Out Current	I_{AC}=50µA, V_{RMS}=2V, VA=4V	–50	–42	–33	µA
	I_{AC}=100µA, V_{RMS}=2V, VA=2V	–38	–27	–12	µA
	I_{AC}=200µA, V_{RMS}=2V, VA=4V	–165	–150	–105	µA
	I_{AC}=300µA, V_{RMS}=1V, VA=2V	–250	–225	–150	µA
	I_{AC}=100µA, V_{RMS}=1V, VA=2V	–95	–80	–60	µA
Multiplier Gain Constant	(Note 5)		–1.0		V
OSCILLATOR					
Oscillator Frequency	R_{SET}=15k	46	55	62	kHz
	R_{SET}=8.2k	86	102	118	kHz
C_T Ramp Peak-to-Valley Amplitude		4.8	5.2	5.6	V
C_T Ramp Valley Voltage		0.8	1.1	1.3	V
GATE DRIVER					
Maximum GT Drv Output Voltage	0mA load on GT Drv, 18V<Vcc<35V	13	14.5	18	V
GT Drv Output Voltage High	–200mA load on GT Drv, Vcc=15V	12	12.8		V
GT Drv Output Voltage Low, Off	Vcc=0V, 50mA load on GT Drv		0.9	1.5	V
GT Drv Output Voltage Low	200mA load on GT Drv		1.0	2.2	V
	10mA load on GT Drv		0.1	0.4	V
Peak GT Drv Current	10nF from GT Drv to Gnd		1.0		A
GT Drv Rise/Fall Time	1nF from GT Drv to Gnd		35		ns
GT Drv Maximum Duty Cycle			95		%
CURRENT LIMIT					
PKLMT Offset Voltage		–10		10	mV
PKLMT Input Current	PKLMT=–0.1V	–200	–100		µA
PKLMT to GT Drv Delay	PKLMT falling from 50mV to –50mV		175		ns

Note 5: Multiplier Gain Constant (k) is defined by: $I_{Mult\ Out} = \frac{k \times I_{AC} \times (VA\ Out - 1)}{V_{RMS}^2}$

PIN DESCRIPTIONS (Pin Numbers Refer to DIL Packages)

Gnd (Pin 1) (ground): All voltages are measured with respect to Gnd. Vcc and REF should be bypassed directly to Gnd with an 0.1μF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to Gnd should also be as short and as direct as possible.

PKLMT (Pin 2) (peak limit): The threshold for PKLMT is 0.0V. Connect this input to the negative voltage on the current sense resistor as shown in Figure 1. Use a resistor to REF to offset the negative current sense signal up to Gnd.

CA Out (Pin 3) (current amplifier output): This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to Gnd, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled. The current amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

ISENSE (Pin 4) (current sense minus): This is the inverting input to the current amplifier. This input and the non-inverting input Mult Out remain functional down to and below Gnd. Care should be taken to avoid taking these inputs below –0.5V, because they are protected with diodes to Gnd.

Mult Out (Pin 5) (multiplier output and current sense plus): The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at Mult Out. The cautions about taking ISENSE below –0.5V also apply to Mult Out. As the multiplier output is a current, this is a high impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject Gnd noise. Figure 1 shows an example of using the current amplifier differentially.

IAC (Pin 6) (input AC current): This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to Mult Out, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6V, so in addition to a resistor from IAC to rectified 60Hz, connect a resistor from IAC to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

VA Out (Pin 7) (voltage amplifier output): This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will stay active even if the IC is disabled with either ENA or Vcc. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8V to prevent overshoot. The voltage amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

VRMS (Pin 8) (RMS line voltage): The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the VRMS input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage should stay between 1.5V and 3.5V.

REF (Pin 9) (voltage reference output): REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when Vcc is low or when ENA is low. Bypass REF to Gnd with an 0.1μF or larger ceramic capacitor for best stability.

ENA (Pin 10) (enable): ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22k resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.

VSENSE (Pin 11) (voltage amplifier inverting input): This is normally connected to a feedback network and to the boost converter output through a divider network.

RSET (Pin 12) (oscillator charging current and multiplier limit set): A resistor from RSET to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from RSET to ground.

SS (Pin 13) (soft start): SS will remain at Gnd as long as the IC is disabled or Vcc is too low. SS will pull up to over 8V by an internal 14μA current source when both Vcc becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to Gnd, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

CT (Pin 14) (oscillator timing capacitor): A capacitor from CT to Gnd will set the PWM oscillator frequency according to this relationship:

$$F = \frac{1.25}{R_{SET} \times C_T}$$

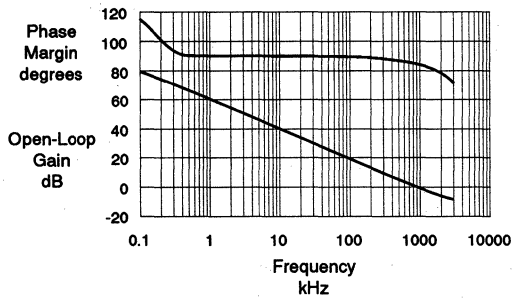
Vcc (Pin 15) (positive supply voltage): Connect Vcc to a stable source of at least 20mA above 17V for normal operation. Also bypass Vcc directly to Gnd to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GT Drv signals, these devices will be inhibited unless Vcc exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

PIN DESCRIPTIONS (cont.)

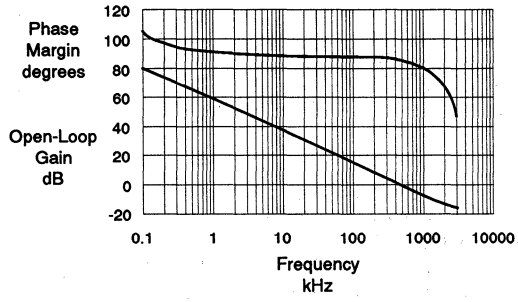
GT Drv (Pin 16) (gate drive): The output of the PWM is a totem pole MOSFET gate driver on GT Drv. This output is internally clamped to 15V so that the IC can be operated with Vcc as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT Drv output driver that might cause the GT Drv output to overshoot excessively. Some overshoot of the GT Drv output is always expected when driving a capacitive load.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

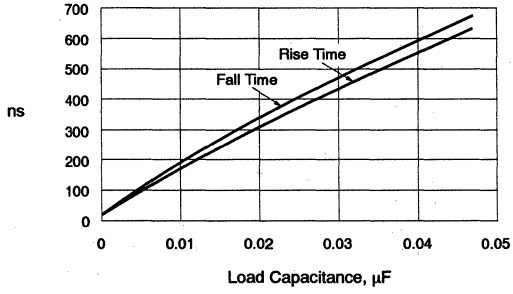
Current Amplifier Gain and Phase vs Frequency



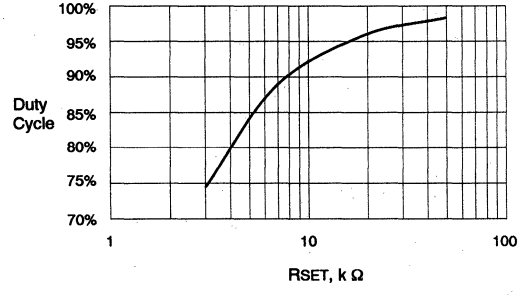
Voltage Amplifier Gain and Phase vs Frequency



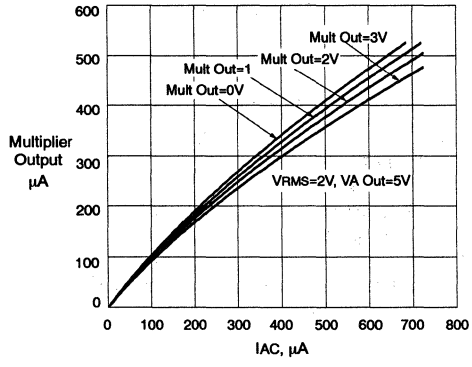
Gate Drive Rise and Fall Time



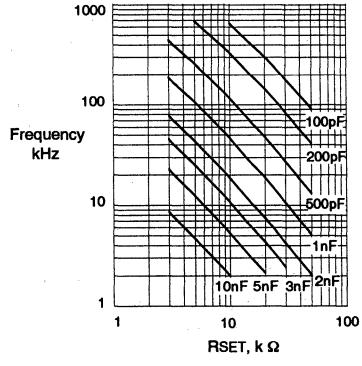
Gate Drive Maximum Duty Cycle



Multiplier Output vs Voltage on Mult

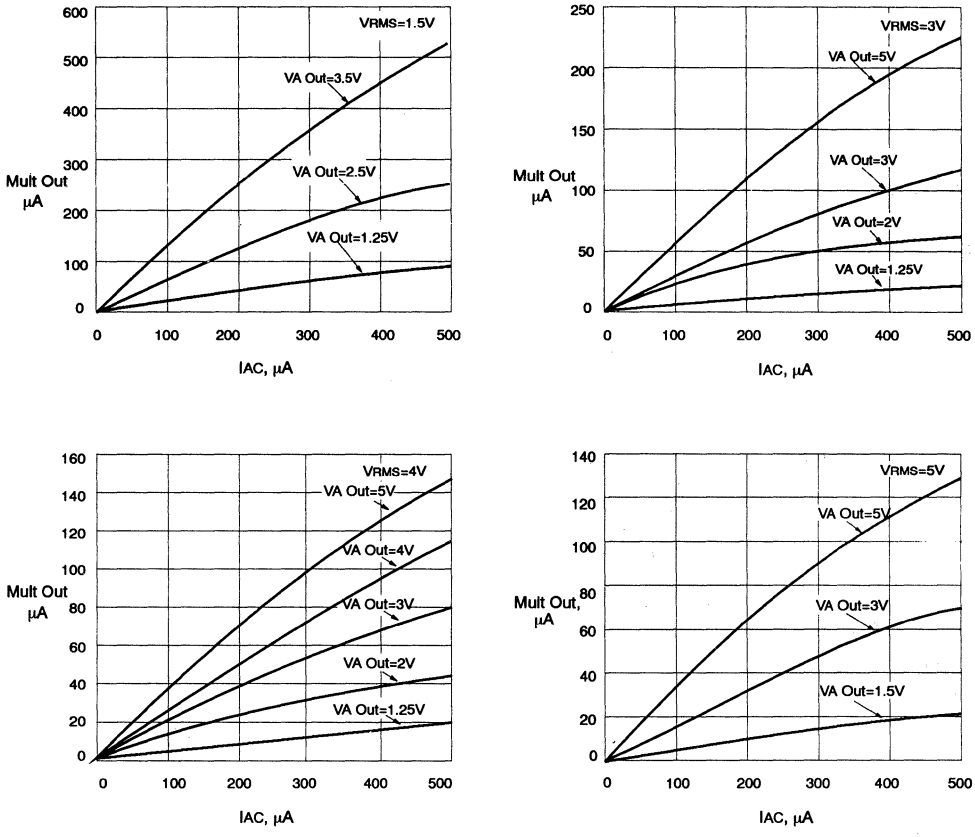


Oscillator Frequency vs R_{SET} and C_T



TYPICAL CHARACTERISTICS at $T_A = T_J = 25^{\circ}C$ (cont.)

Multiplier Output vs Multiplier Inputs with Mult Out=0V



5

APPLICATIONS INFORMATION

A 250W PREREGULATOR

The circuit of Figure 1 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the UC3854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the UC3854 provides PWM pulses (GT Drv, Pin 16) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN #	FUNCTION
V_{SENSE}	11	Output DC Voltage
I_{AC}	6	LineVoltage Waveform
I_{SENSE}/Mult Out	4/5	Line Current
V_{RMS}	8	RMS Line Voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions, as follows:

INPUT	PIN #	FUNCTION
ENA	10	Start-Up Delay
SS	13	Soft Start
PKLIM	2	Maximum Current Limit

APPLICATIONS INFORMATION (cont.)

PROTECTION INPUTS

ENA (Enable): The ENA input must reach 2.5 volts before the REF and GT Drv outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at pin 15, where the on/off thresholds are 16V and 10V. If the ENA input is unused, it should be pulled up to Vcc through a current limiting resistor of 100k.

SS (Soft start): The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically 7.5V. An internal current source delivers approximately -14μA from pin 13. Thus a capacitor connected between that pin and ground will charge linearly from zero to 7.5V in 0.54C seconds, with C expressed in microfarads.

PKLIM (Peak current limit): Use pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 1, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.25 ohm current sense resistor is 7.5V*2k/10k=1.5V, corresponding to 6A. A bypass capacitor from pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

VSENSE (Output DC voltage sense): The threshold voltage for the VSENSE input is 7.5V and the input bias current is typically 50nA. The values shown in Figure 1 are for an output voltage of 400V DC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 47nF feedback capacitor places a 15Hz pole in the voltage loop that prevents 120Hz ripple from propagating to the input current.

IAC (Line waveform): In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage in waveform is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.
This input is not a voltage, but a current (hence IAC). It is set up by the 220k and 910k resistive divider (see Figure 1). The voltage at pin 6 is internally held at 6V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400μA at the peak of the waveshape. The following formulas were used to calculate these resistors:

$$R_{AC} = \frac{V_{pk}}{I_{ACpk}} = \frac{260VAC \times \sqrt{2}}{400\mu A} = 910k$$

$$R_{REF} = \frac{R_{AC}}{4} = 220k$$

(where Vpk is the peak line voltage)

ISENSE/Mult Out (Line current): The voltage drop across the 0.25 ohm current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

VRMS (RMS line voltage): An important feature of the UC3854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in the US (85VAC) to high line in Europe (255VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the RMS value of the line voltage. The voltage applied to pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at pin 5, is a current that increases with the current at pin 6 and the voltage at pins 7, and decreases with the square of the voltage at pin 8.

PWM FREQUENCY: The PWM oscillator frequency in Figure 1 is 100kHz. This value is determined by CT at pin 14 and RSET at pin 12. RSET should be chosen first because it affects the maximum value of IMULT according to the equation:

$$I_{MULT_{MAX}} = \frac{-3.75V}{R_{SET}}$$

This effectively sets a maximum PWM-controlled current. With RSET=15k,

$$I_{MULT_{MAX}} = \frac{-3.75V}{15k} = -250\mu A$$

Also note that the multiplier output current will never exceed twice IAC.

With the 4k resistor from Mult Out to the 0.25 ohm current sense resistor, the maximum current in the current sense resistor will be

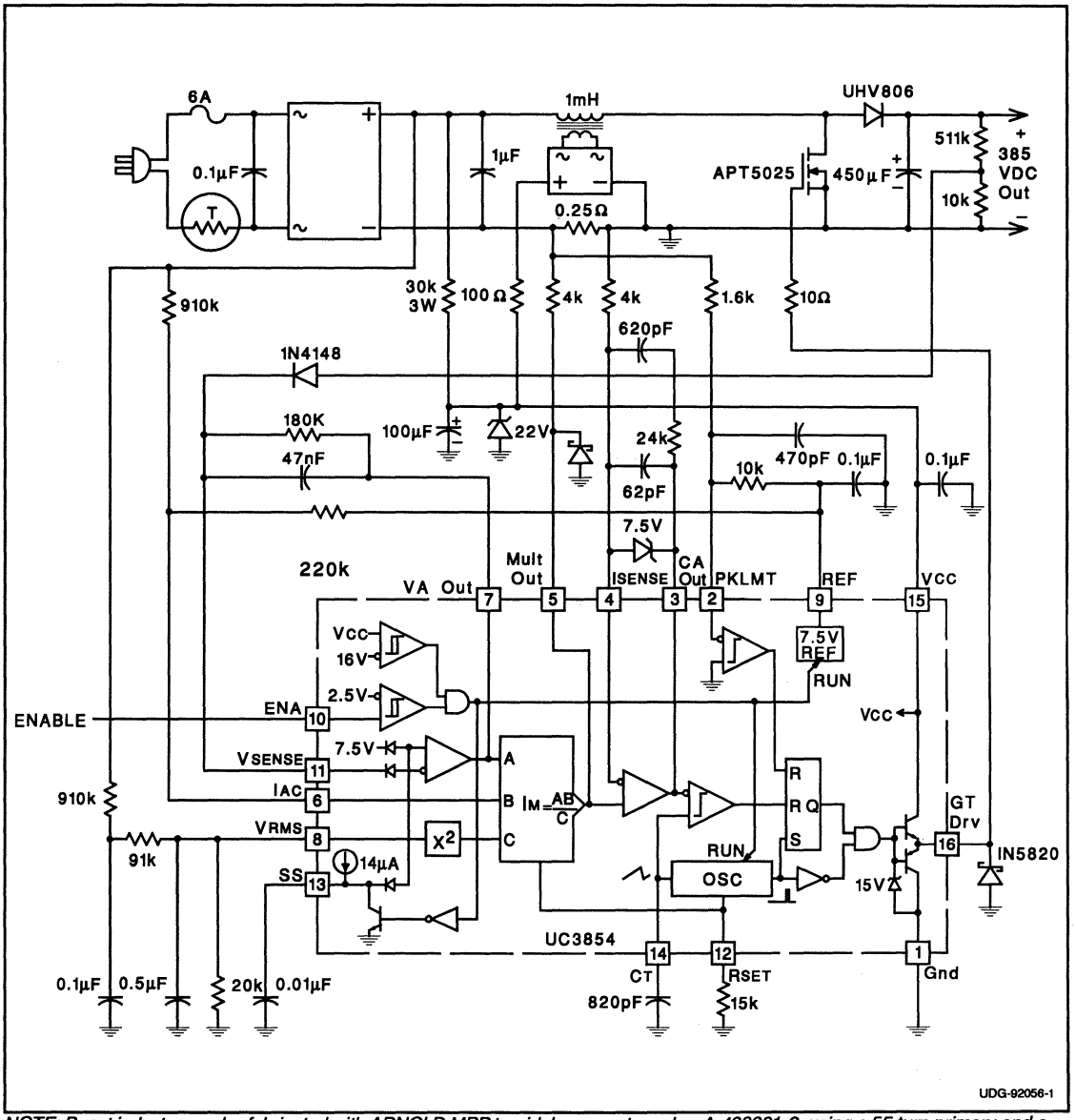
$$I_{MAX} = \frac{-I_{MULT_{MAX}} \times 4k}{0.25\Omega} = -4A$$

Having thus selected RSET, the current sense resistor, and the resistor from Mult Out to the current sense resistor, calculate CT for the desired PWM oscillator frequency from the equation

$$C_T = \frac{1.25}{F \times R_{SET}}$$

FIGURE 1 - Typical Application

This diagram depicts a complete 250 Watt Preregulator. At full load, this preregulator will exhibit a power factor of 0.99 at any power line voltage between 80 and 260 VRMS. This same circuit can be used at higher power levels with minor modifications to the power stage. See Design Note 39B and Application Note U-134 for further details.



NOTE: Boost inductor can be fabricated with ARNOLD MPP toroidal core part number A-438381-2, using a 55 turn primary and a 13 turn secondary.

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Enhanced High Power Factor Preregulator

PRELIMINARY

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Limits Line Current Distortion To <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed Frequency Average Current Mode Control
- High Bandwidth (5 mHz), Low Offset Current Amplifier
- Integrated Current and Voltage Amp Output Clamps
- Multiplier Improvements: Linearity, 500mV VAC Offset (eliminates external resistor), 0-5V Multout Common Mode Range
- VREF "GOOD" Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Threshold Options (16/10V / 10.5/10V)
- 300μA Startup Supply Current

	UVLO Turn on	UVLO Turn off
UC1854A	16V	10V
UC1854B	10.5V	10V

DESCRIPTION

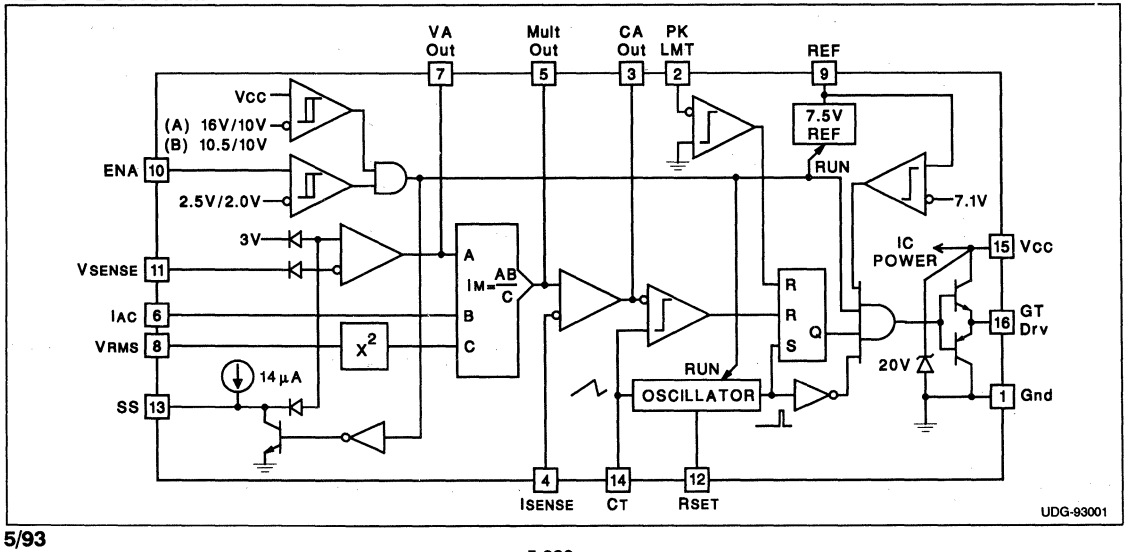
The UC1854A/B products are pin compatible enhanced versions of the UC1854. Like the UC1854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC1854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

The UC1854A/B products improve upon the UC1854 by offering a wide bandwidth, low offset Current Amplifier, a faster responding and improved accuracy enable comparator, a VREF "good" comparator, UVLO threshold options (16/10V for offline, 10.5/10V for startup from an auxiliary 12V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the Multiplier output/Current Amp input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, RSET controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 * IAC at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

A 1% 7.5V reference, fixed frequency oscillator, PWM, Voltage Amplifier with softstart, line voltage feedforward (VRMS squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16 pin N, DW, and J and 20 pin L and Q packages.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=4V, VA Out=3.5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	CAO, VAO = 0V, Vcc = UVLO - 0.3V		250	400	µA
Supply Current, On			12	18	mA
Vcc Turn-On Threshold	UC1854A		16	17.5	V
	UC1854B		10.5	10.8	V
Vcc Turn-Off Threshold	UC1854A / B	9	10		V
Vcc Clamp	I(Vcc) = Icc(on) + 5mA	18	20	22	V
VOLTAGE AMPLIFIER					
Input Offset Voltage		–8		8	mV
V_{SENSE} Bias Current		–500	–25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	70	100		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3	mA
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		1		mHz
CURRENT AMPLIFIER					
Input Offset Voltage	V_{CM} = 2.5V	–2		0	mV
Input Bias Current(sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, V_{OUT} = 2 to 6V	80	110		dB
V_{OUT} High	I_{LOAD} = –500µA		8		V
V_{OUT} Low	ILOAD = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3	mA
Common Mode Range		-0.3		5	V
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)	3	5		mHz
REFERENCE					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.425	7.5	7.575	V
	I_{REF} = 0mA	7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA	–15		15	mV
Line Regulation	Vcc = 12 to 18V	–10		10	mV
Short Circuit Current	V_{REF} = 0V	25	35	45	mA
OSCILLATOR					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	Vcc = 12 to 18V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Amplitude (p-p)		4.8		5.6	V
Ramp Valley Voltage		0.8		1.3	V
ENABLE / SOFTSTART / CURRENT LIMIT					
Enable Threshold		2.4	2.55	2.7	V
Enable Hysteresis	V_{FAULT} = 2.5V		500	600	mV
Propagation Delay to Disable	Enable overdrive = –100mV, (Note 1)		300		ns
SS Charge Current	$V_{SOFTSTART}$ = 2.5V	6	14	20	
PKLMT Offset Voltage		–10		10	mV
PKLMT Input Current	V_{PKLMT} = –0.1V	–200	–100		µA
PKLMT Propagation Delay	(Note 1)		150		ns

5

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=4V, VA Out=3.5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLIER					
Output Current - I_{AC} Limited	I_{AC}=100µA, V_{RMS} = 1V	–220	–200	–180	µA
Output Current - Zero	I_{AC}=0µA	–2.0	–0.2	2.0	µA
Output Current - Power Limited	V_{RMS} = 1.5V, Va = 6V	–220	–200	–180	µA
Output Current	V_{RMS} = 1.5V, Va = 2V		–22		µA
	V_{RMS} = 1.5V, Va = 5V		–156		µA
	V_{RMS} = 5V, Va = 2V		–2		µA
	V_{RMS} = 5V, Va = 5V		–14		µA
Gain Constant	(Note 2)	–1.1	–1.0	–0.9	A/A
GATE DRIVER					
Output High Voltage	I_{OUT} = –200mA, V_{CC} = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V
Output Rise / Fall Time	C_{LOAD} = 1nF, (Note 1)		35		ns
Output Peak Current	C_{LOAD} = 10nF, (Note 1)		1.0		A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \frac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^2 \times I_{MO}}$ *where* $1.5V \le V_{RMS} \le 5V$.

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Improved Current Mode PWM Controller

FEATURES

- Pin for pin compatible with the UC1846
- 65ns typical delay from shutdown to outputs, and 50ns typical delay from sync to outputs.
- Improved current sense amplifier with reduced noise sensitivity.
- Differential current sense with 3V common mode range.
- Trimmed oscillator discharge current for accurate deadband control.
- Accurate 1V shutdown threshold.
- High current dual totem pole outputs (1.5A peak).
- TTL compatible oscillator sync pin thresholds.
- 4kV ESD protection.

DESCRIPTION

The UC1856 is a high performance version of the popular UC1846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the Current Sense output is slew rate limited to reduce noise sensitivity. Fast 1.5 amp peak output stages have been added to allow rapid switching of power FET's.

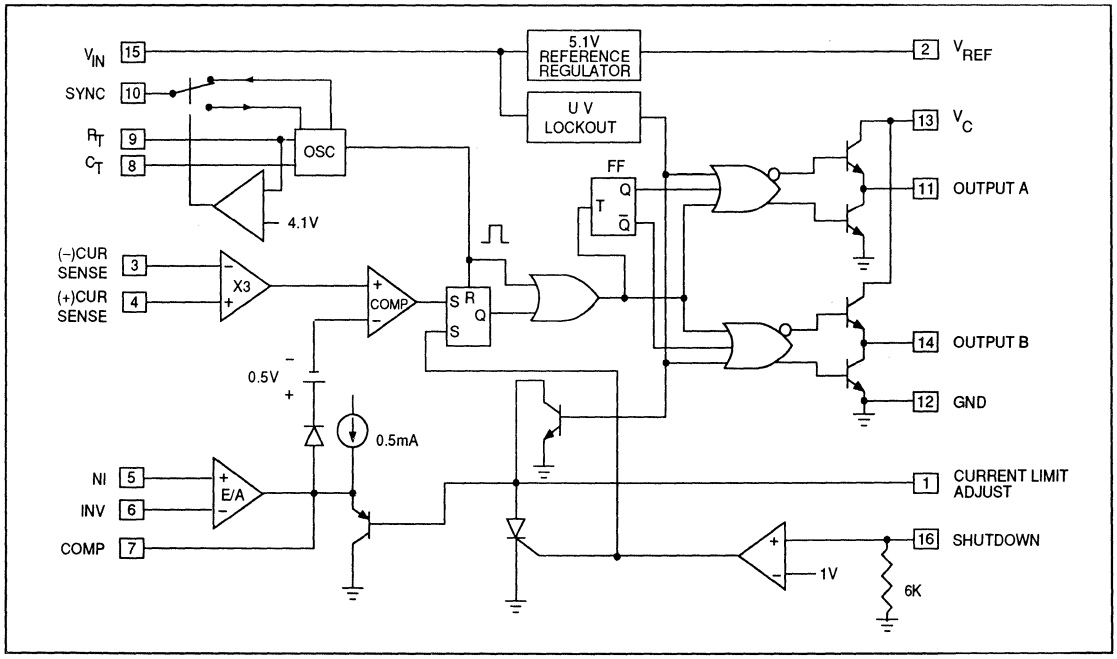
A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1 volt, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

5

BLOCK DIAGRAM



12/92

ABSOLUTE MAXIMUM RATINGS (Note 1)

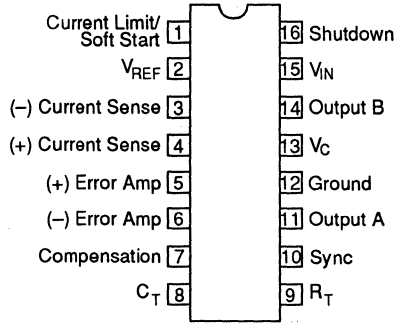
Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5µs) 2.0A
Error Amp Inputs (Pins 5, 6) ..... –0.3V to $+V_{IN}$
Shutdown Input (Pin 16) ..... -0.3V to +10V
Current Sense Inputs (Pins 3,4) ..... –0.3V to +3V
Sync Output Current (Pin 10) ..... ±10mA
Error Amplifier Output Current (Pin 7) ..... –5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A = 25°C (Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note: 1. All voltages are with respect to Ground, Pin 12.
Currents are positive into, negative out of the specified terminal.
Pin numbers and thermal ratings refer to the DIL-16 Package.

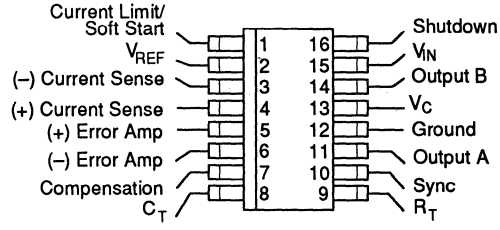
Note: 2. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL–16 (TOP VIEW)
J or N PACKAGE

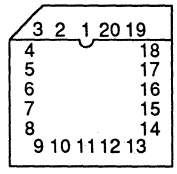


SOIC–16 (TOP VIEW)
DW PACKAGE



PLCC–Q PACKAGE (TOP VIEW)

1 - N/C
2 - Current Limit/Soft Start
3 - V_{REF}
4 - (–) Current Sense
5 - (+) Current Sense
6 - N/C
7 - (+) Error Amp
8 - (–) Error Amp
9 - Compensation
10 - C_T



20 - Shutdown
19 - V_{IN}
18 - Output B
17 - V_C
16 - N/C
15 - Ground
14 - Output A
13 - SYNC
12 - R_T
11 - N/C

OTHER PACKAGES AVAILABLE:

28-PIN QP
28-PIN L

ELECTRICAL CHARATERISTICS (Unless otherwise stated, these specifications apply for T_A = – 55°C to +125°C for UC1856; – 40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, V_{IN} =15V, R_T=10K, C_T=1nF) T_A=T_J, Pin No.'s Refer to DIL Package.

UC1856
UC2856
UC3856

PARAMETER	TEST CONDITIONS	UC1856 UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	Tj=25°C, Io=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	Vin=8 to 40V			20			20	mV
Load Regulation	Io=-1mA to -10mA			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz<f<10KHz, Tj=25°C		50			50		uV
Long Term Stability	Tj=125°C, 1000Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	Vref=0V	- 25	- 45	- 65	- 25	- 45	- 65	mA
Oscillator Section								
Initial Accuracy	Tj=25°C	180	200	220	180	200	220	KHz
	Over Operating Range	170		230	170		230	KHz
Voltage Stability	Vin= 8 to 40V			2			2	%
Discharge Current	Tj=25°C, Vpin8=2V	7.5	8.0	8.8	7.5	8.0	8.8	mA
	Vpin8=2V	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	Io=-1mA	2.4	3.6		2.4	3.6		V
Sync Output Low Level	Io=+1mA		0.2	0.4		0.2	0.4	V
Sync Input High Level	Pin 8=0V, Pin 9=Vref	2.0	1.5		2.0	1.5		V
Sync Input Low Level	Pin 8=0V, Pin 9=Vref		1.5	0.8		1.5	0.8	V
Sync Input Current	Pin 8=0V, Pin 9=Vref Vsync=5V		1	10		1	10	uA
Sync Delay to Outputs	Pin 8=0V, Pin 9=Vref Vsync=0.8V to 2V		50	100		50	100	ns
Error Amp Section								
Input Offset Voltage	Vcm=2V			5			10	mV
Input Bias Current				– 1			– 1	uA
Input Offset Current				500			500	nA
Common Mode Range	Vin=8 to 40V	0		Vin-2	0		Vin-2	V
Open Loop Gain	Vo=1.2 to 3V	80	100		80	100		dB
Unity Gain Bandwidth	Tj=25°C	1	1.5		1	1.5		MHz
CMRR	Vcm=0 to 38V, Vin=40V	75	100		75	100		dB
PSRR	Vin=8 to 40V	80	100		80	100		dB
Output Sink Current	Vid=– 15mV, Vpin7=1.2V	5	10		5	10		mA
Output Source Current	Vid=15mV, Vpin7=2.5V	– 0.4	– 0.5		– 0.4	– 0.5		mA
Output High Level	Vid=50mV, R_L (pin 7)=15K	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	Vid=-50mV, R_L (pin 7)=15K		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	Vpin3=0V, Pin1 Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal (Vpin4–Vpin3)	Pin 1 Open (Note 3) R_L (pin 7)=15K	1.1	1.2		1.1	1.2		V
Input Offset Voltage	Vpin1=0.5V Pin7 Open (Note 3)		5	35		5	35	mV
CMRR	Vcm= 0 to 3V	60			60			dB
PSRR	Vin= 8 to 40V	60			60			dB
Input Bias Current	Vpin1=0.5V, Pin 7 Open (Note 3)		– 1	– 3		– 1	– 3	uA

5

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for T_A = – 55°C to +125°C for UC1856; – 40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, V_{IN} =15V, R_T=10K, C_T=1nF) T_A=T_J Pin No.'s Refer to DIL Package.

UC1856
UC2856
UC3856

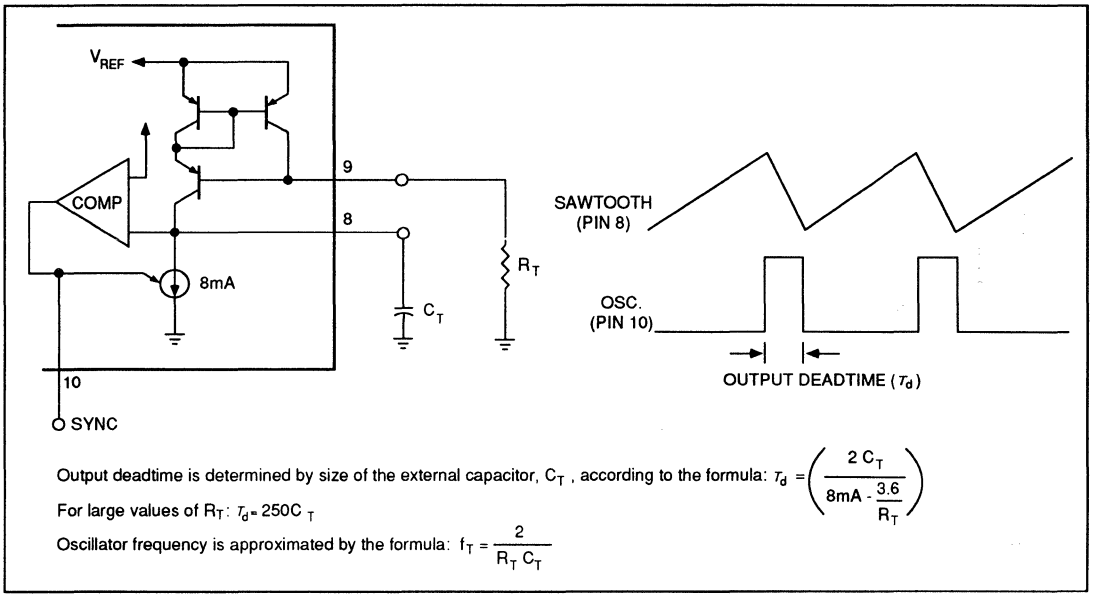
PARAMETER	TEST CONDITIONS	UC1856 UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Current Sense Amplifier Section (Continued)								
Input Offset Current	Vpin1=0.5V, Pin 7 Open (Note 3)			1			1	uA
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	Vpin5=Vref, Pin6=0V Pin4 – Pin3= 0 to 1.5V		120	250		120	250	ns
Current Limit Adjust Section								
Current Limit Offset	Vpin3=0V Vpin4=0V, Pin7=Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	Vpin5=Vref, Vpin6=0V		– 10	– 30		– 10	– 30	uA
Shutdown Terminal Section								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V
Minimum Latching Current (Ipin1)	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current (Ipin1)	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	Vpin16=0 to 1.3V		65	110		65	110	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	Vc=40V			250			250	uA
Output Low Level	Iout= 20mA		0.1	0.5		0.1	0.5	V
	Iout= 200mA		0.5	2.6		0.5	2.6	V
Output High Level	Iout= – 20mA	12.5	13.2		12.5	13.2		V
	Iout= – 200mA	12	13.1		12	13.1		V
Rise Time	C1= 1nF		40	80		40	80	ns
Fall Time	C1= 1nF		40	80		40	80	ns
UVLO Low Saturation	Vin=0V, Iout=20mA		0.8	1.5		0.8	1.5	V
PWM Section								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysterisis			0.7			0.7		V
Total Standby Current								
Supply Current			18	23		18	23	mA

NOTES:

1. All voltages are with respect to pin 12. Currents are positive into, negative out of the specified terminal.
2. This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.
3. Parameter measured at trip point of latch with Vpin5=Vref, Vpin6=0V.
4. Amplifier gain defined as: $G = \frac{\triangle Vpin7}{\triangle Vpin4}$; $\triangle Vpin4$=0 to 1.0V
5. Current into pin1 guaranteed to latch circuit into shutdown state
6. Current into pin 1 guaranteed not to latch circuit into shutdown state

APPLICATIONS DATA

Oscillator Circuit

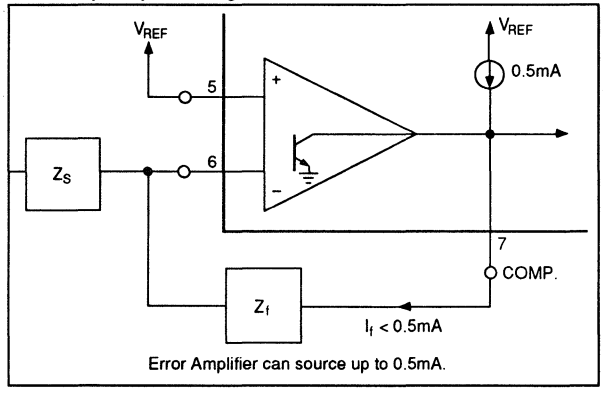


Output deadtime is determined by size of the external capacitor, C_T, according to the formula: $\tau_d = \left(\frac{2\,C_T}{8mA - \frac{3.6}{R_T}}\right)$

For large values of R_T: $\tau_d = 250C_T$

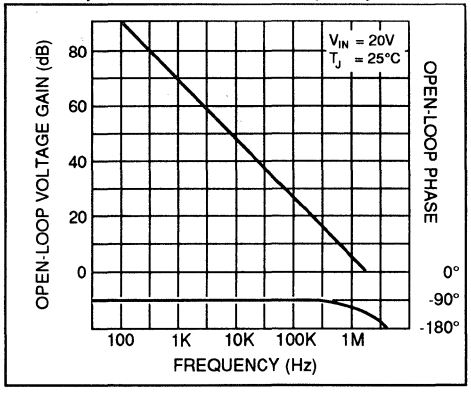
Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T\,C_T}$

Error Amp Output Configuration

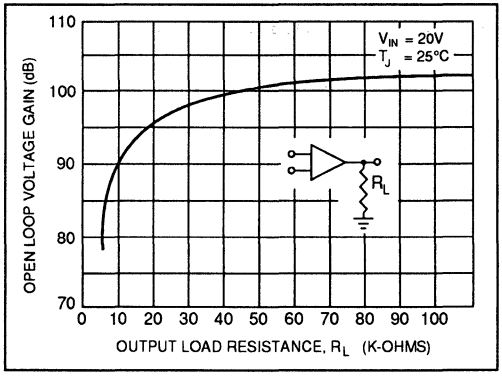


Error Amplifier can source up to 0.5mA.

Error Amp Gain and Phase vs Frequency

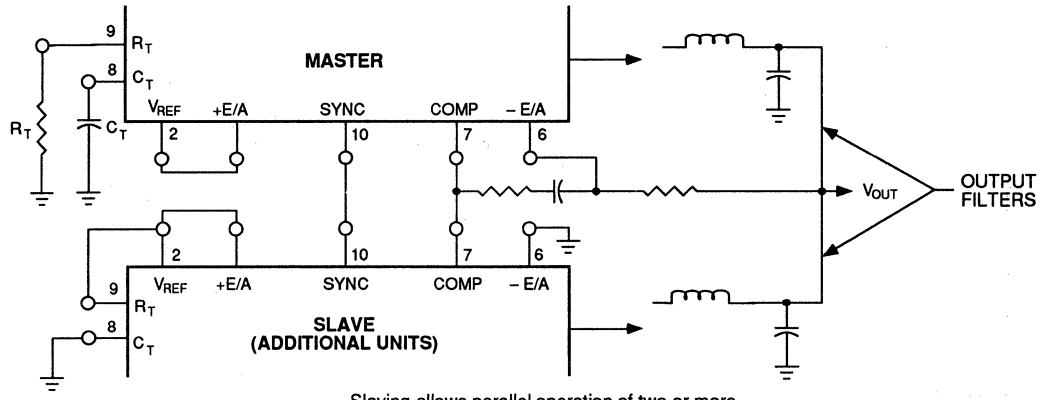


Error Amp Open-Loop D.C. Gain vs Load Resistance



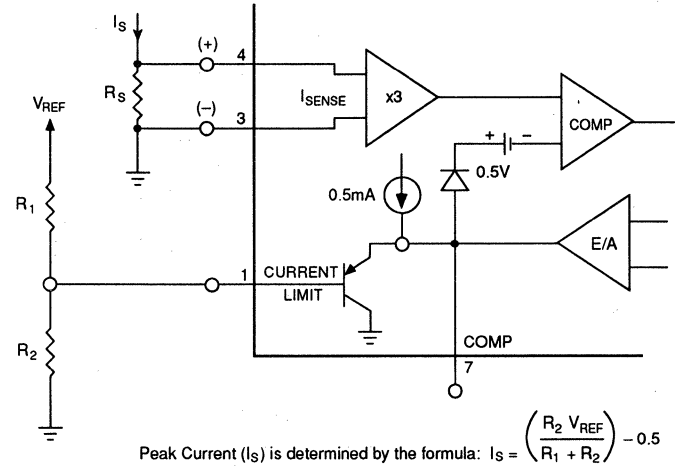
5

Parallel Operation



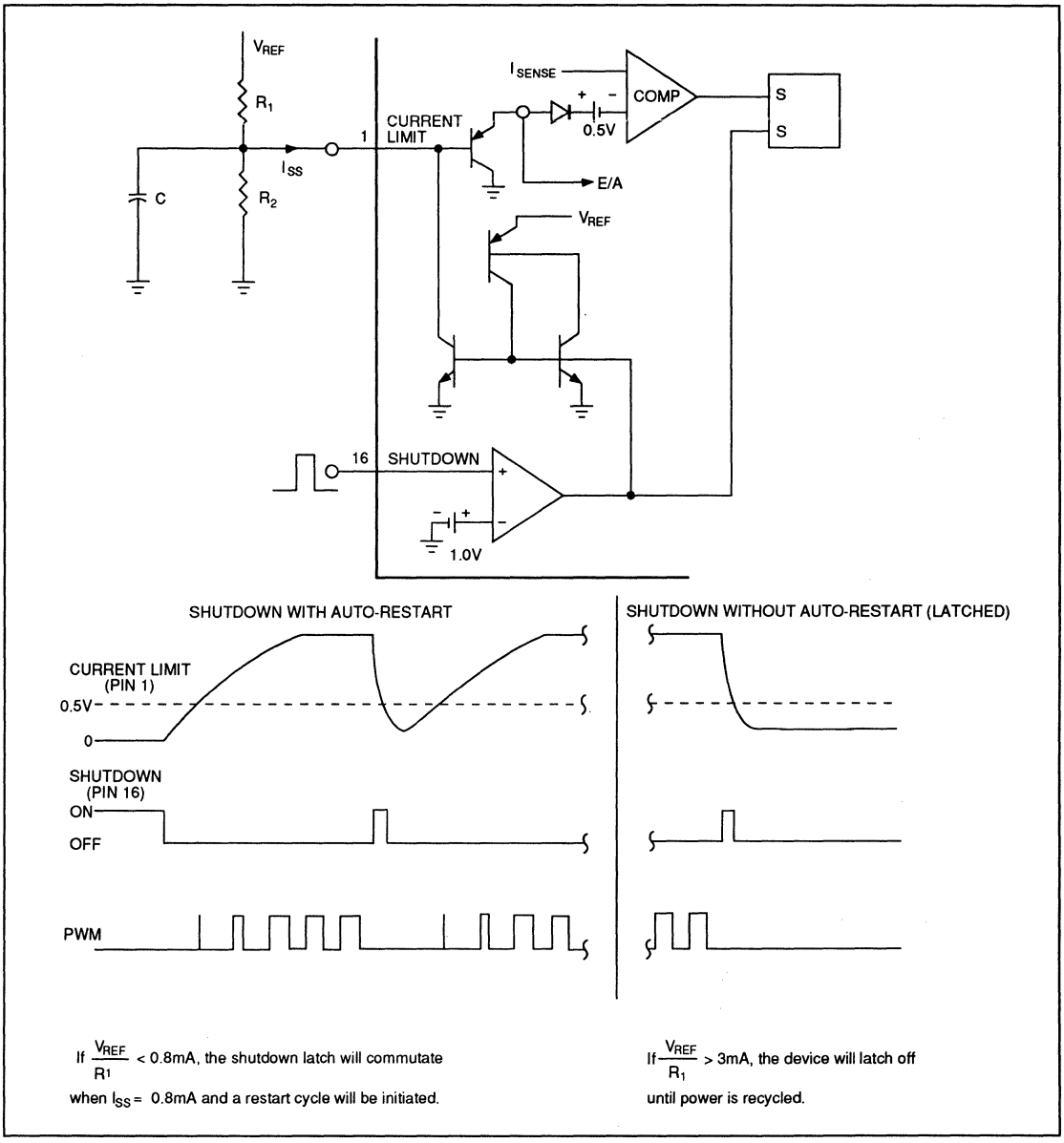
Slaving allows parallel operation of two or more units with equal current sharing.

Pulse by Pulse Current Limiting



Peak Current (I_S) is determined by the formula: $I_S = \dfrac{\left(\dfrac{R_2\ V_{REF}}{R_1 + R_2}\right) - 0.5}{3R_S}$

Soft Start and Shutdown/Restart Functions

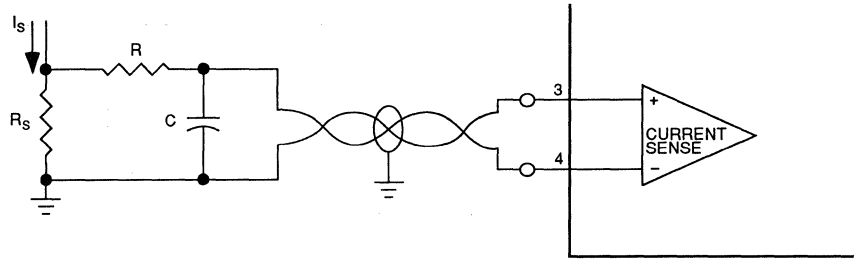


If $\frac{V_{REF}}{R1}$ < 0.8mA, the shutdown latch will commutate when I_{SS} = 0.8mA and a restart cycle will be initiated.

If $\frac{V_{REF}}{R_1}$ > 3mA, the device will latch off until power is recycled.

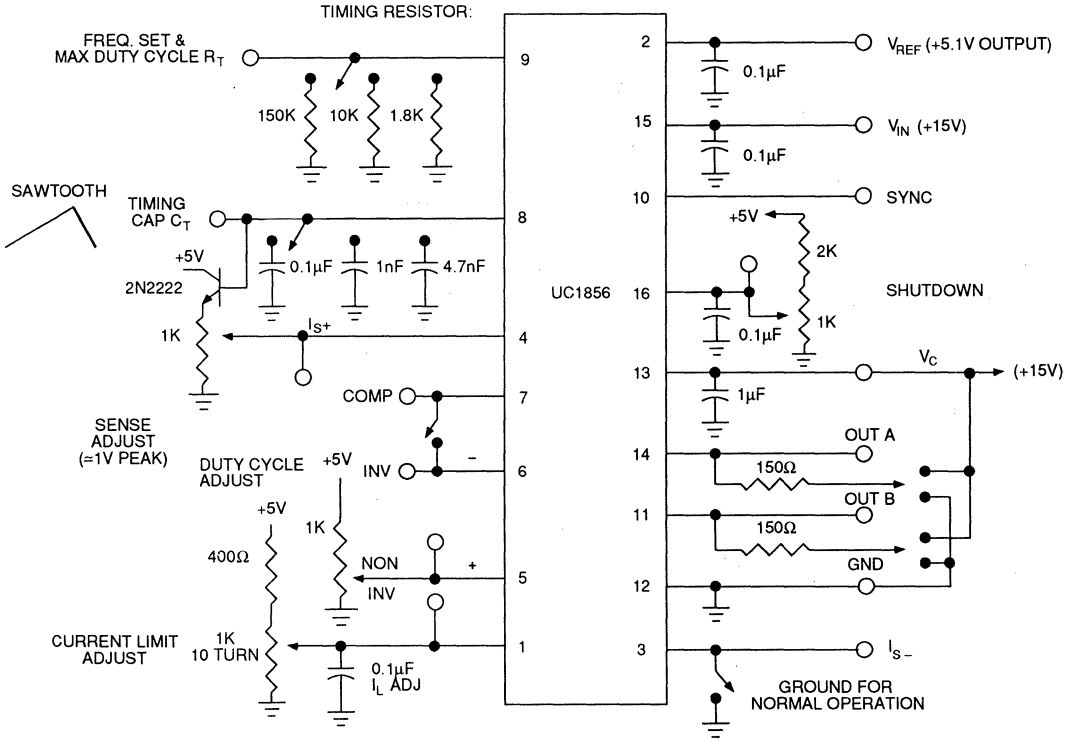
5

Current Sense Amp Connections



A small RC filter may be required in some applications to reduce switch transients.
Differential input allows remote, noise free sensing.

UC1856 Open Loop Test Circuit



-BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
-SHORT PINS 6 & 7 FOR UNITY GAIN TESTING

THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED

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INTEGRATED CIRCUITS
UNITRODE

Resonant Mode Power Supply Controller

UC1860
UC2860
UC3860

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant mode power supply control. This device easily implements frequency modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

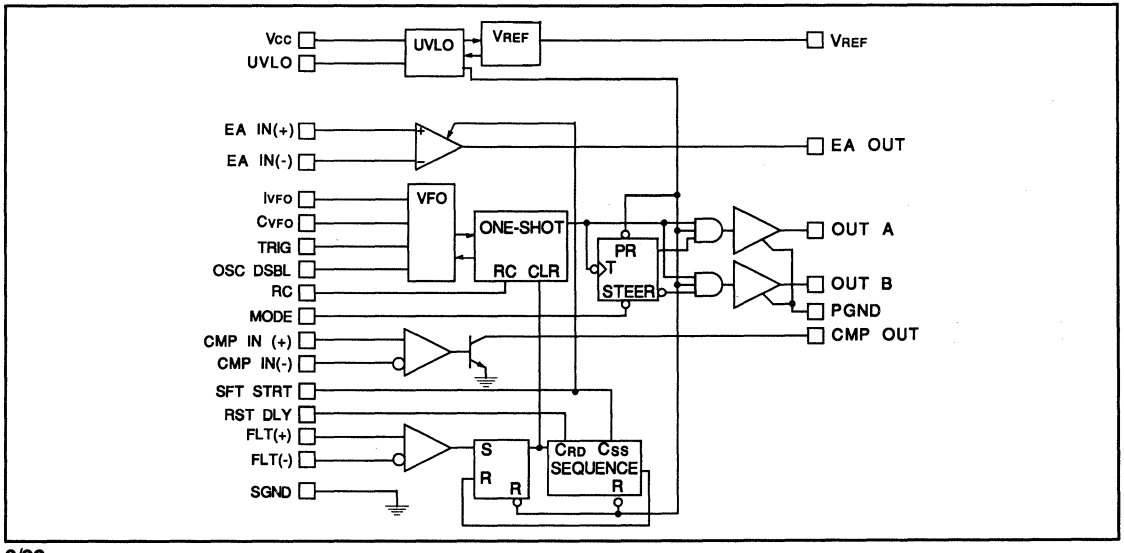
The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 19) 20V
Output Current, Source or Sink (pins 17 & 20)
DC 0.8A
Pulse (0.5µs) 3.0A
Power Ground Voltage ..... ±0.2V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12, 13, 14, 21, 22, 23 & 24) ..... -0.4 to 6V
Error Amp Output Current, Source or Sink (pin 5) 2mA
I_{VFO} Current (pin 7) 2mA
Comparator Output Current (pin 15) 5mA
Comparator Output Voltage (pin 15) 15V
Soft Start or Restart Delay Sink Current (pins 22 & 23) ... 5mA
Power Dissipation at T_A = 50°C (DIP) 1.25W
Power Dissipation at T_A = 50°C (PLCC) 1W
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the DIP. Refer to Packaging Section of Databook for thermal limitations and considerations of packages.

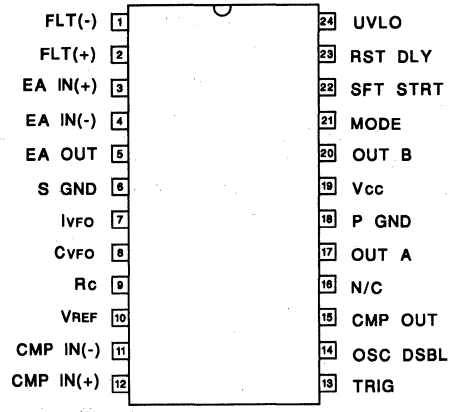
BLOCK DIAGRAM



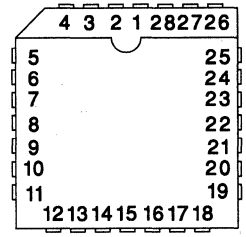
6/93

CONNECTION DIAGRAM

DIL - 24 (TOP VIEW)
J or N Package



PLCC-28, LCC-28
(TOP VIEW)
Q or L Package



PIN PACKAGE FUNCTION	
FUNCTION	PIN
S GND	1
IVFO	2
CVFO	3
RC	4
VREF	5
CMP IN (-)	6
CMP IN (+)	7
TRIG	8
OSC DSBL	9
CMP OUT	10
N/C	11, 12
OUT A	13
PGND	14
N/C	15
Vcc	16
OUT B	17
N/C	18, 19
MODE	20
SFT STRT	21
RST DLY	22
UVLO	23
FLT (-)	24
FLT (+)	25
EA IN (+)	26
EA IN (-)	27
EA OUT	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for -55°C ≤ TA ≤ 125°C for the UC1860, -25°C ≤ TA ≤ 85°C for the UC2860, 0 ≤ TA ≤ 70°C for the UC3860, Vcc = 12V, CVFO = 330pF, IVFO = 0.5mA, C = 330pF, and R = 2.7k, TA = TJ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TA = 25°C, Io = 0	4.95	5.00	5.05	V
	Io = 0, Over Temp	4.93		5.07	V
Line Regulation	10 ≤ Vcc ≤ 20V		2	15	mV
Load Regulation	0≤ Io ≤ 10mA		2	25	mV
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz		50		μVRMS
Short Circuit Current	VREF = 0V	-150		-15	mA
Error Amplifier Section					
Input Offset Voltage	2.8 ≤ VCM ≤ 4.5V		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	dVo = 1.5V	60	80		dB
PSRR	10 ≤ Vcc ≤ 20V	70	100		dB
Output Low (Vo-VIVFO)	-0.1 ≤ Io ≤ 0.1mA	-8	0	8	mV
Output High (Vo-VIVFO)	-0.5 ≤ Io ≤ 0.5mA	1.9	2	2.1	V
Unity Gain Bandwidth*	RIN = 2k	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dIosc*	100 ≤ IVFO ≤ 500μA	2	3	4	GHz/A

**Guaranteed by design but not 100% tested.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for -55°C ≤ T_A ≤ 125°C for the UC1860, -25° ≤ T_A ≤ 85°C for the UC2860, 0 ≤ T_A ≤ 70°C for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section (cont'd)					
Trig in Threshold		1.0	1.4	1.8	V
Trig in Open Circuit Voltage		0.7	0.9	1.1	V
Trig in Delta (V_{TH}-Voc)		0.3	0.5	0.7	V
Trig in Input Resistance	dV $_{TRIG}$ = Voc to V_{TH}	5	12	25	kΩ
Minimum Trig in Pulse Width*			3	10	ns
Osc. Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	I_{VFO} = 1.5mA	2.8	3.7	4.6	MHz
Dead Time*	I_{VFO} =1.5mA	35	70	100	ns
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	-20mA		1.5	2.0	V
	-200mA		1.7	2.5	V
Rise/Fall Time*	C_{LOAD} = 1nF		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
Vcc Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysteresis	0.2	0.4	0.6	V
UVLO Input Resistance	UVLO = 4/Vcc = 8	10	23	50	kΩ
V_{REF} Comparator Threshold	Vcc = UVLO = V_{REF}		4.5	4.9	V
Supply Current					
Icc	Vcc = 12V, Vosc DSBL = 3V		30	40	mA
I_{START}	UVLO pin open Vcc = Vcc (on) -0.3V		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	-0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Propagation Delay To Output*	±50mV input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	-0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Output Low Voltage	Io = 2mA		0.3	0.5	V
Propagation Delay To Sat*	±50mV input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	I_{SINK} = 100µA		0.2	0.5	V
Charge Current (2 pins)		2	5	10	µA
Restart Delay Threshold		2.8	3.0	3.2	V

**Guaranteed by design but not 100% tested.*

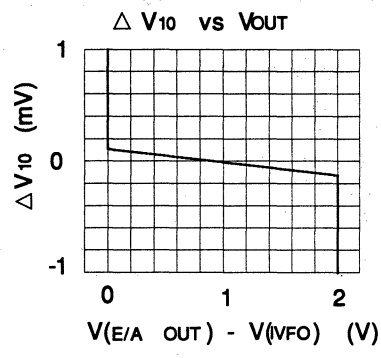
ERROR AMPLIFIER

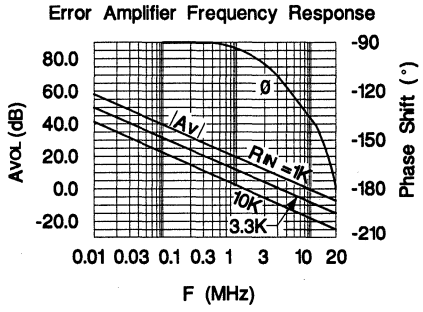
The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

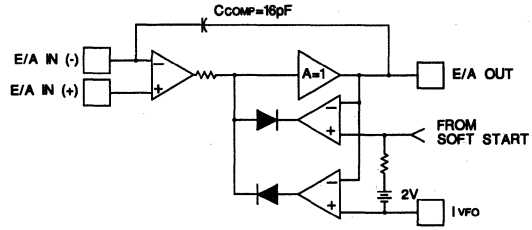
*Frequency (0dB) = 1/(2π * RIN (-) * CCOMP)*

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the IVFO pin is limited from zero to 2V. Note that pulling Sft Strt (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.





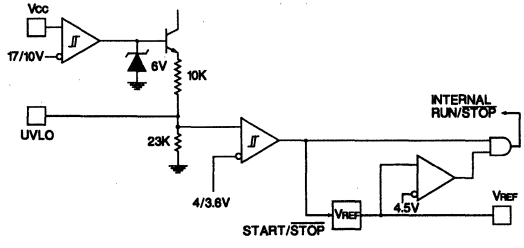


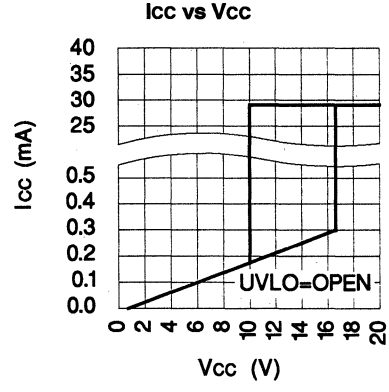
UNDER VOLTAGE LOCKOUT SECTION

The under voltage lockout consists of three comparators that monitor Vcc, UVLO and VREF. The VREF comparator makes sure that the reference voltage is sufficiently high before operation begins. When the UVLO comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The Vcc comparator is used for off-line applications by leaving the UVLO pin open. In this application the supply current is typically less than 0.3mA during start-up.

The UVLO comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, UVLO, Vcc, and VREF are tied together.





VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: C_{VFO}, I_{VFO}, Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

Frequency = $I_{VFO}/(C_{VFO} * 1V)$

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the I_{VFO} pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

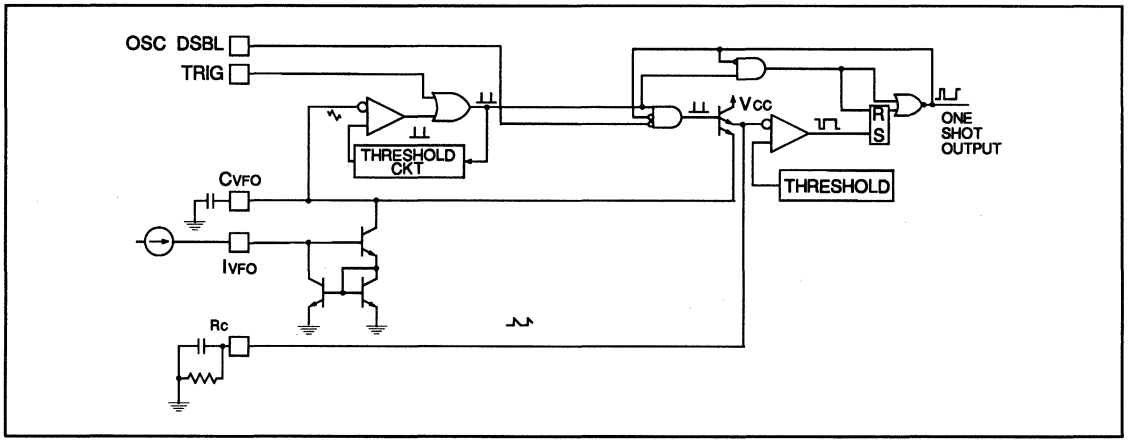
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

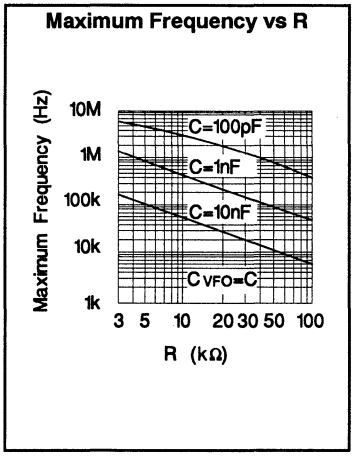
ONE SHOT TIMER

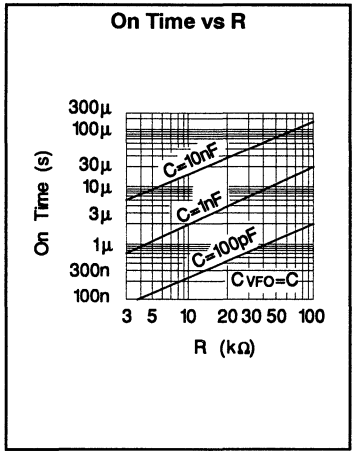
The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

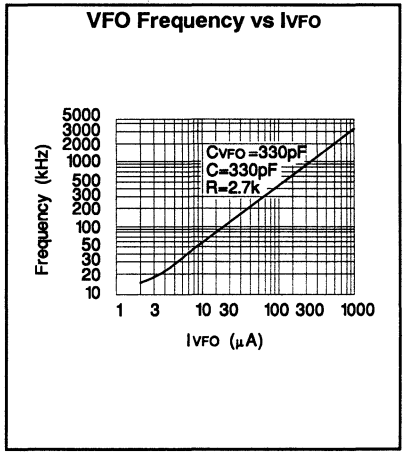
$t(on) = 0.2 * R * C$.

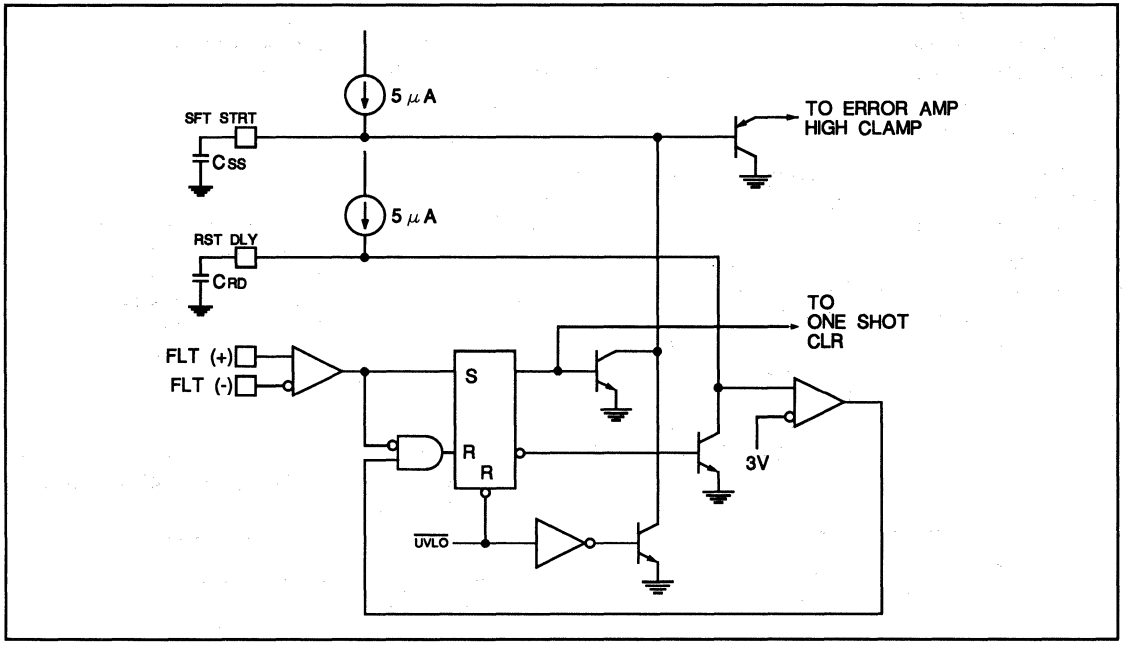
After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.











FAULT MANAGEMENT SECTION

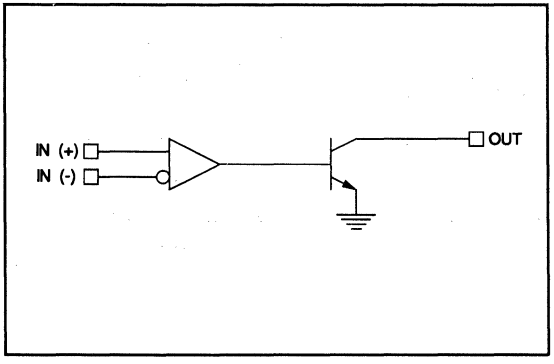
During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

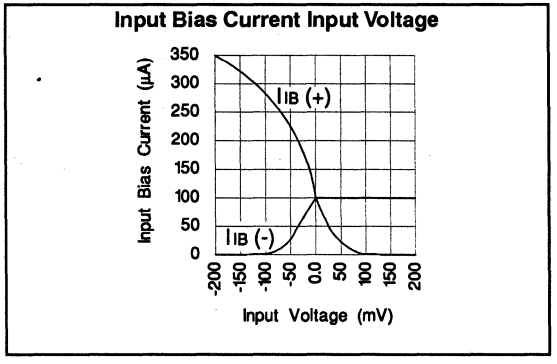
UNCOMMITTED COMPARATOR

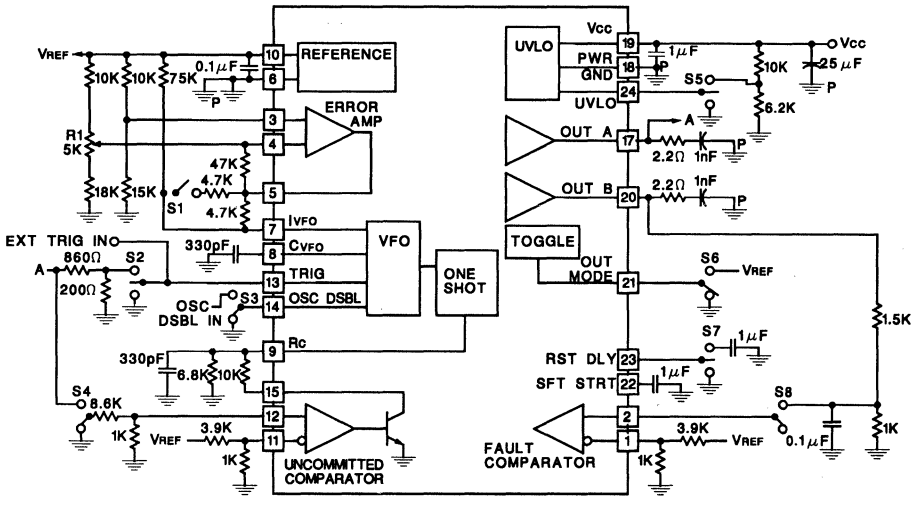
The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of -0.3 to 3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.

The high speed fault comparator will work over the input common mode range of -0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

*t (off) = 600 kohm * C(Rst Dly).*







NOTE: PIN NUMBERS REFER TO THE DIP

OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.

Open the IVFO resistor switch (S1).

Throw the Trig switch (S2) to ground.

Throw the Osc Dsbl switch (S3) to ground.

Throw the uncommitted comparator switch (S4) to ground.

Throw the UVLO switch (S5) to the resistive divider.

Throw the Out Mode switch (S6) to ground.

Open the restart delay switch (S7).

Throw the fault switch (S8)to ground.

In this configuration, the chip will operate for Vcc greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0 to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie: A,B, off,...)

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the Vcc start and stop thresholds are 17 and 10V. Switched to the resistive divider, the thresholds are approximately 12 and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, Vcc, or opening the switch. Connected to IμF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

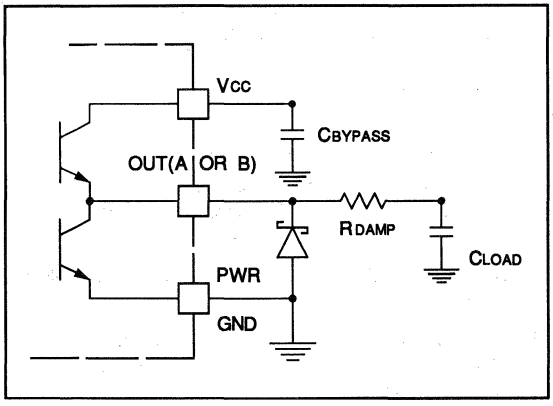
OUTPUT STAGE

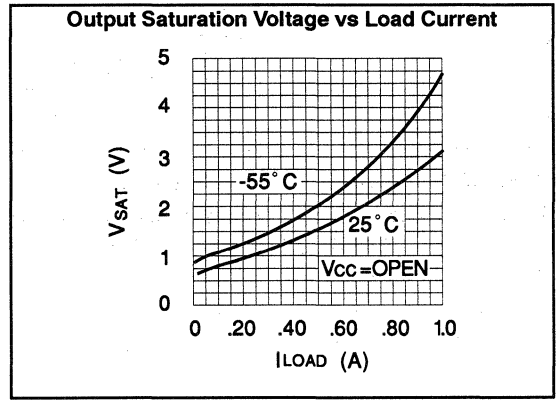
The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

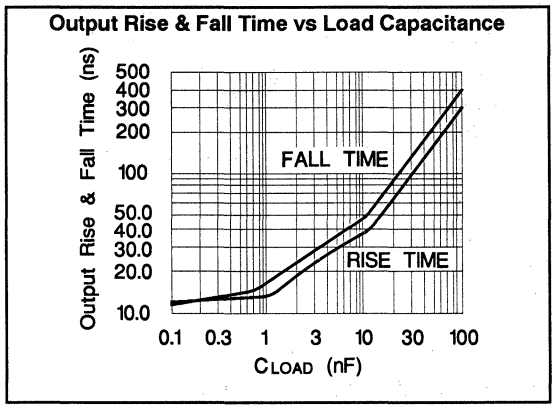
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of dI/dt. This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed ±0.2V from signal ground.

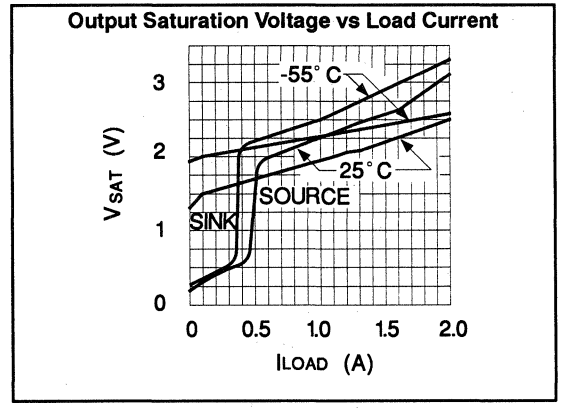
BYPASS NOTE

The reference should be bypassed with a 0.1μF ceramic capacitor from the VREF pin directly to the ground plane near the Signal Ground pin. The timing capacitors on CVFO and RC should be treated likewise. VCC, however, should be bypassed with a ceramic capacitor from the VCC pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.









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INTEGRATED CIRCUITS
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Resonant-Mode Power Supply Controllers

UC1861-1868
UC2861-2868
UC3861-3868

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10 kHz to 1 MHz
- Low Start-Up Current (150 µA typ.)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

Device	UVLO	Outputs	'Fixed'
1861	16.5/10.5	Alternating	Off Time
1862	16.5/10.5	Parallel	Off Time
1863	8/7	Alternating	Off Time
1864	8/7	Parallel	Off Time
1865	16.5/10.5	Alternating	On Time
1866	16.5/10.5	Parallel	On Time
1867	8/7	Alternating	On Time
1868	8/7	Parallel	On Time

DESCRIPTION

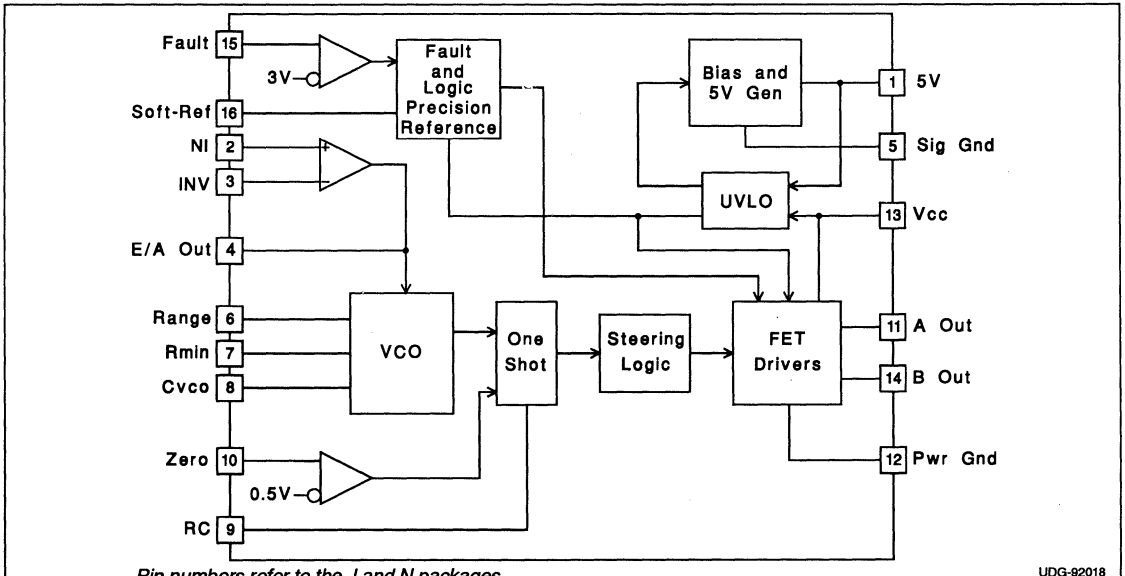
The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150 µA, and the outputs are actively forced to the low state. UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After Vcc exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage. (continued)

5

BLOCK DIAGRAM



Pin numbers refer to the J and N packages.

UDG-92018

DESCRIPTION (cont.)

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison alllowing a 2 Amp peak current.

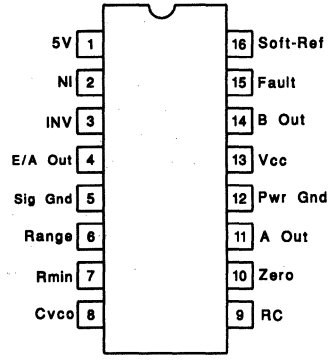
ABSOLUTE MAXIMUM RATINGS

Vcc 22V
Output Current, Source or Sink (Pins 11 & 14) DC 0.5A
Pulse (0.5µs) 1.5A
Power Ground Volage ..... ±0.2V
Inputs (Pins 2, 3, 10, & 15) ..... -0.4 to 7V
Error Amp Output Current ..... ±2mA
Power Dissipation 1W
Junction Temperature (Operating) ..... 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

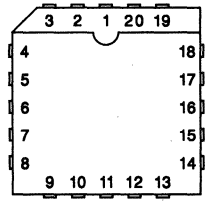
Note 1: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
Cvco	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
Vcc	17
B Out	18
NC	19
Fault	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications apply for -55°C≤TA≤125°C for the UC186x, -25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, Vcc=12V, Cvco=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and Csr=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	12V ≤ Vcc ≤ 20V, -10mA ≤ Io ≤ 0mA	4.8	5.0	5.2	V
Short Circuit Current	Vo = 0V	-150		-15	mA
Soft-Reference					
Restart Delay Current	V = 2V	10	20	35	µA
Soft Start Current	V = 2V	-650	-500	-350	µA
Reference Voltage	TJ = 25°C, Io = 0A	4.95	5.00	5.05	V
	12V ≤ Vcc ≤ 20V, -200µA ≤ Io ≤ 200µA	4.85		5.15	V
Line Regulation	12V ≤ Vcc ≤ 20V		2	20	mV
Load Regulation	-200µA ≤ Io ≤ 200µA		10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	VCM = 5V, Vo = 2V, Io = 0A	-10		10	mV
Input Bias Current	VCM = 0V	-2.0	-0.3		µA
Voltage Gain	Vcm = 5V, 0.5V ≤ Vo ≤ 3.7V, Io = 0A	70	100		dB
Power Supply Rejection Ratio	Vcm = 5V, Vo = 2V, 12V ≤ Vcc ≤ 20V	70	100		dB

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for -55°C≤TA≤125°C for the UC186x, -25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, Vcc=12V, CVCO=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and CSF=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	0V ≤ Vcm ≤ 6V, Vo = 2V	65	100		dB
VOUT Low	VID = -100mV, Io = 200µA		0.17	0.25	V
VOUT High	VID = 100mV, Io = -200µA	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	1.0		MHz
Voltage Controlled Oscillator					
Maximum Frequency	VID (Error Amp) = 100mV, TJ = 25°C	450	500	550	kHz
	VID (Error Amp) = 100mV	425		575	kHz
Minimum Frequency	VID (Error Amp) = -100mV, TJ = 25°C	45	50	55	kHz
	VID (Error Amp) = -100mV	42		58	kHz
One Shot					
Zero Comparator Vth		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	VZERO = 1V	850	1000	1150	ns
Maximum to Minimum Pulse	VZERO = 0V UCx861 - UCx864	2.5	4	5.5	
Width Ratio	VZERO = 0V UCx865 - UCx868	4	5.5	7	
Output Stage					
Rise and Fall Time	CLOAD = 1nF (Note 4)		25	45	ns
Output Low Saturation	Io = 20mA		0.2	0.4	V
	Io = 200mA		0.5	2.2	V
Output High Saturation	Io = -200mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	Io = 20mA		0.8	1.5	V
Fault Comparator					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns
UVLO					
Vcc Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
Vcc Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
Icc Start	Vcc = Vcc(on) - 0.3V		150	300	µA
Icc Run	VID = 100mV		25	32	mA

Note 1: Currents are defined as positive into the pin.
Note 2: Pulse measurement techniques are used to insure that TJ = TA.
Note 3: VID = V(NI) - V(INV).
Note 4: This parameter is not 100% tested in production but guaranteed by design.
Note 5: Vi = 0 to 4V tr(Vi) ≤ 10ns tpd = t(Vo = 6V) - t(Vi = 3V)

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300µA, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1µF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200µA, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1µF. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the

low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source.

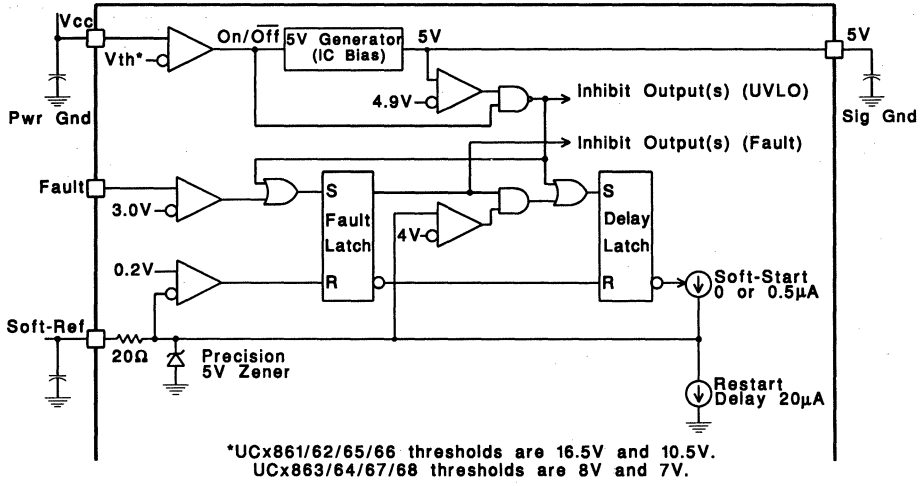
The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20µA. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20kΩ or larger resistor from Soft-Ref to ground.

A 100kΩ resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20µA current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

UVLO, 5V, Fault, and Soft-Ref



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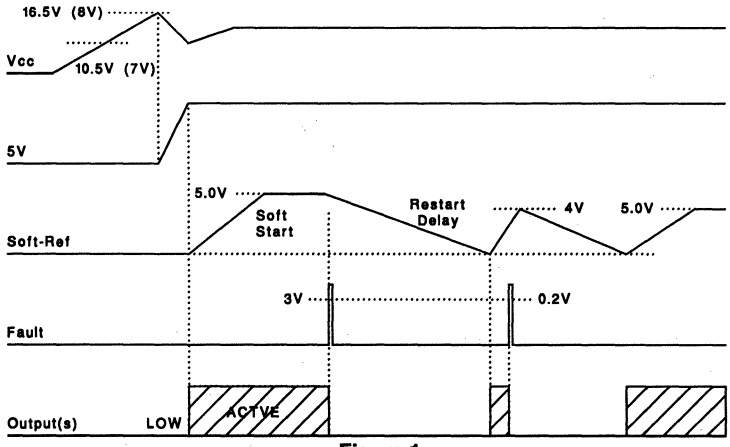

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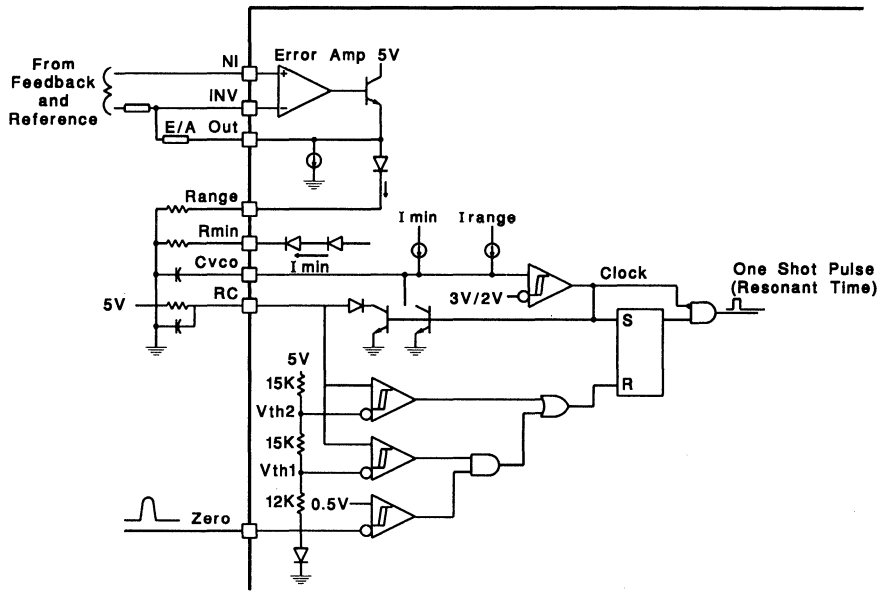
Figure 1

Error Amp, Voltage Controlled Oscillator, and One Shot



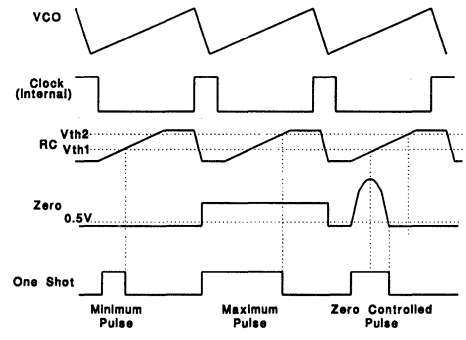


Figure 2

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{4.3}{R_{MIN} \bullet C_{VCO}}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.3}{(R_{MIN} \,||\, Range) \bullet C_{VCO}}$$

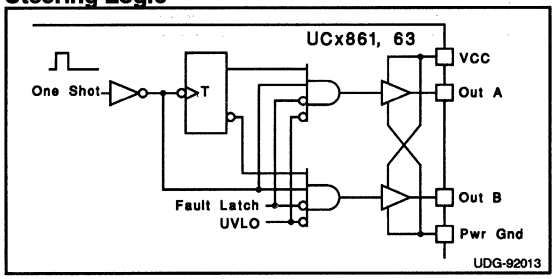
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tpw(min) \cong 0.3 \bullet R \bullet C.$$

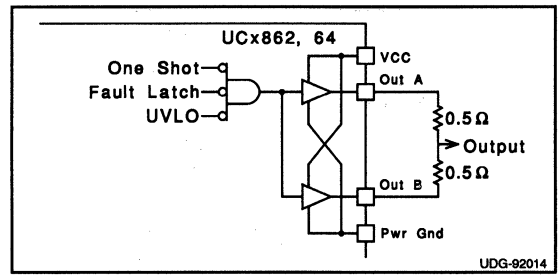
The maximum pulse width is approximately given by:

$$Tpw(max) \cong 1.2 \bullet R \bullet C.$$

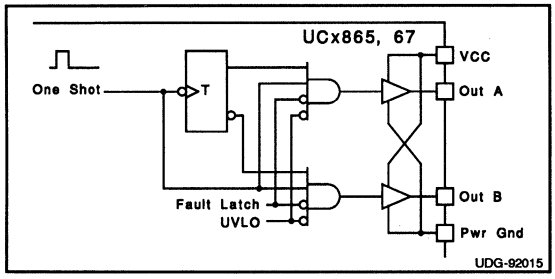
Steering Logic



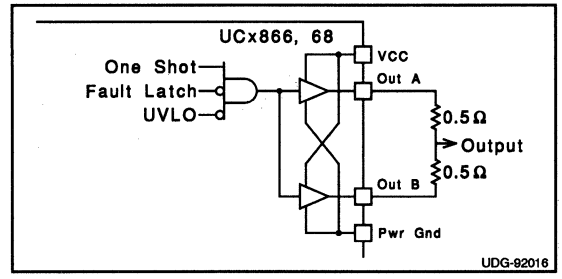
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

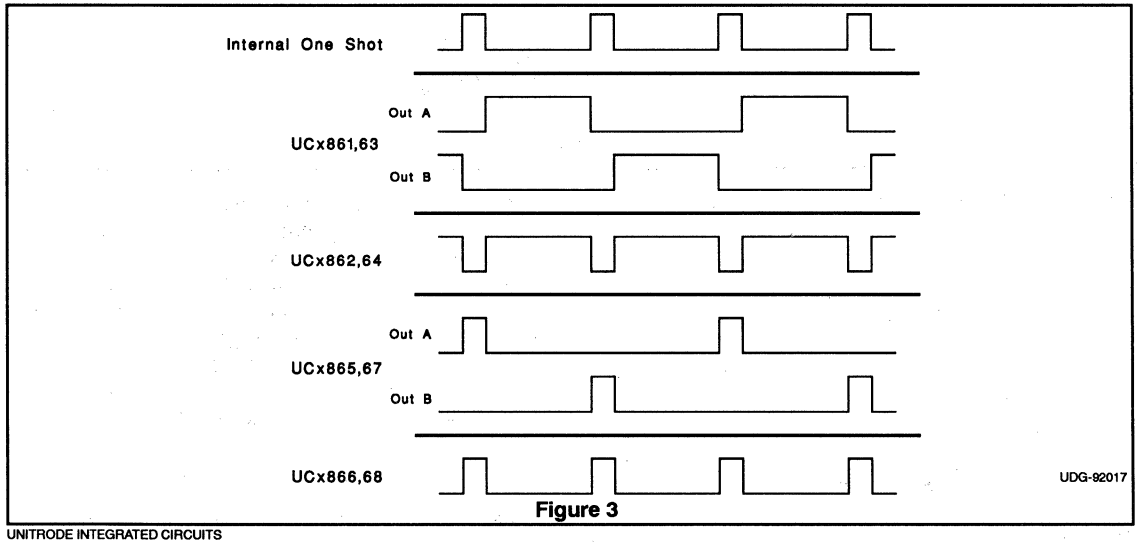


Figure 3

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Resonant Fluorescent Lamp Driver

FEATURES

- 1μA ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

DESCRIPTION

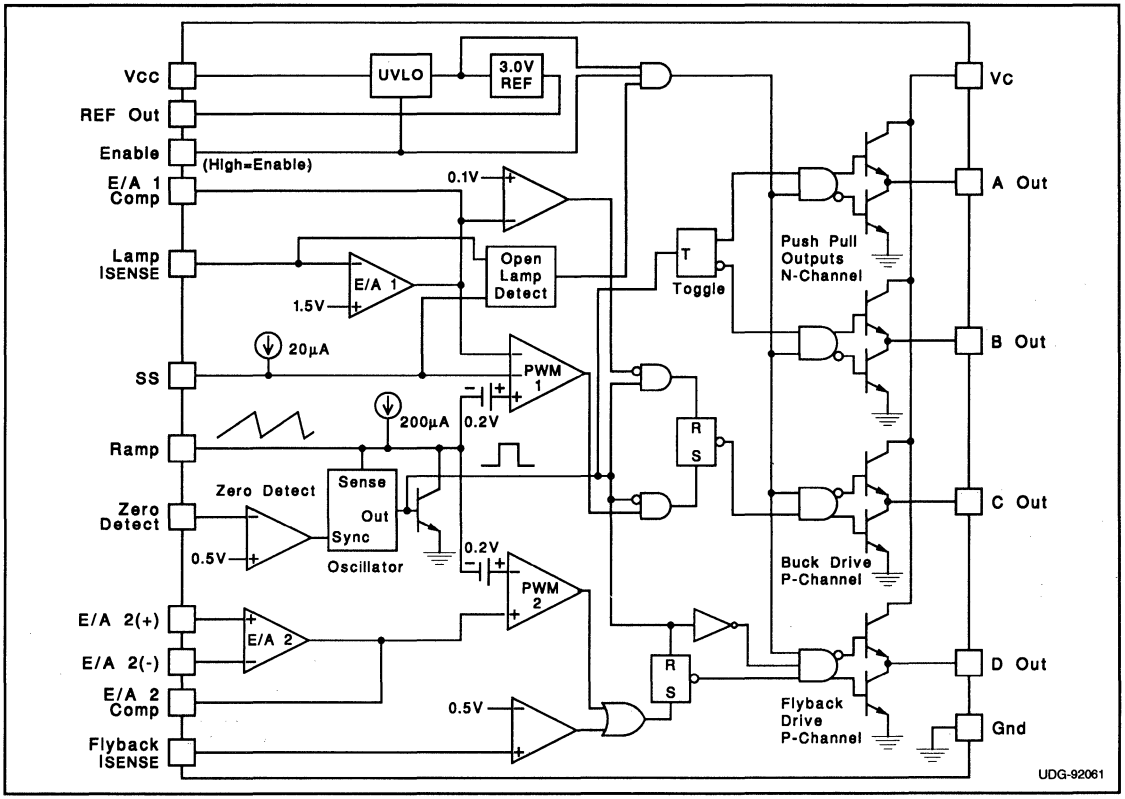
The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1μA, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



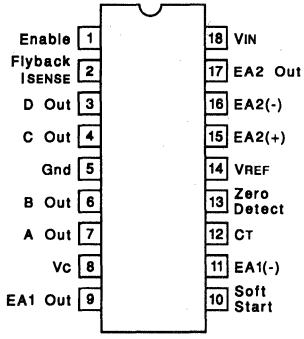
5/93

ABSOLUTE MAXIMUM RATINGS

Analog Inputs ..... +10V
Zero Detect ..... +20V
Power Dissipation at T_A = 25°C 1W
Storage Temperature ..... -65°C to +150°C
Lead Temperature ..... 300°C

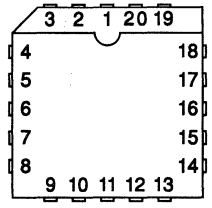
Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1
B Out	2
A Out	3
Vc	4
EA1 Out	5
Soft Start	6
EA1(-)	7
N/C	8
CT	9
Zero Detect	10
N/C	11
VREF	12
EA2(+)	13
EA2(-)	14
EA2 Out	15
VIN	16
Enable	17
Flyback ISENSE	18
D Out	19
C Out	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_J = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; Vcc = 5V, Vc = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J=25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	Vcc = 4.75V to 18V			10	mV
Load Regulation	Io=0 to -5mA			10	mV
Oscillator Section					
Free Running Freq	T_J=25°C	57	68	78	kHz
Max Sync Frequency	T_J=25°C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp 1 Section					
Input Voltage	Vo = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	µA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	V_{EA}(-) = 1.3V	3.1	3.5	3.9	V
Output Low	V_{EA}(-) = 1.7V		0.1	0.2	V
Output Source Current	V_{EA}(-) = 1.3V, Vo = 2V	-350	-500		µA
Output Sink Current	V_{EA}(-) = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}-1V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these parameters apply for T_J = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; Vcc = 5V, Vc = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Lamp Detect Section					
Soft Start Threshold	V_{EA}(-) = 0V	2.9	3.4	3.8	V
Error Amp Threshold	Vss = 4.2V	0.3	0.5	0.7	V
Soft Start Current	Vss = 2V	10	20	40	µA
Error Amp 2 Section					
Input Offset Voltage	Vo = 2V		0	10	mV
Input Bias Current			-0.2	-1	µA
Input Offset Current				0.5	µA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	V_{ID} = 100mV, Vo = 2V	3.6	4	4.4	V
Output Low	V_{ID} = -100mv, Vo = 2V		0.1	0.2	V
Output Source Current	V_{ID} = 100mV, Vo = 2V	-350	-500		µA
Output Sink Current	V_{ID} = -100mV, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}-2V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Isense Section					
Threshold		0.475	0.525	0.575	V
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Outputs C and D	14.7	14.9		V
	I_{OUT} = -10mA	13.5	14.3		V
	I_{OUT} = -100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{EA1}(-) = 1V	100			%
Out C Min Duty Cycle	V_{EA1}(-) = 2V			0	%
Out D Max Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = 100mV		92	96	%
Out D Min Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = -100mV			0	%
Under Voltage Lockout Section					
Start-Up Threshold		3.7	4.2	4.5	V
Hysterisis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	V_{ENABLE} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	Vcc = 20V		8	14	mA
VC Supply Current	Vc=20V		7	12	mA
ICC Disabled	Vcc = 20V, V_{ENABLE} = 0V		1	10	µA

Note 3: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.

Note 4: Guaranteed by design but not 100% tested in production.

TYPICAL APPLICATION

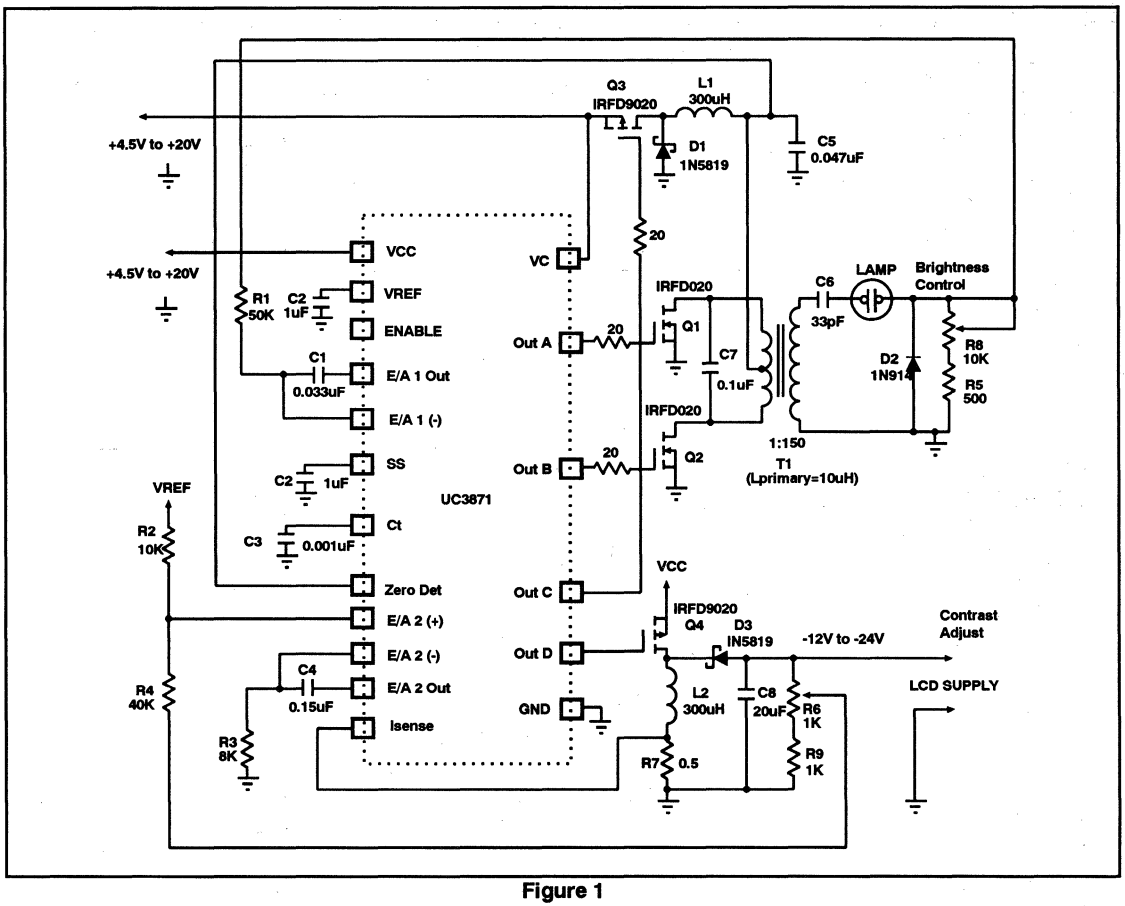


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

APPLICATION INFORMATION (cont.)

UC3871 OSCILLATOR SECTION

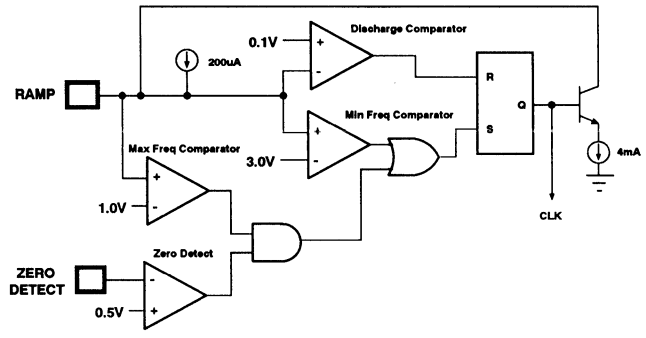


Figure 2

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shutdown, the IC typically draws less than 1μA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

5

UC1871 Open Lamp Detect Circuitry

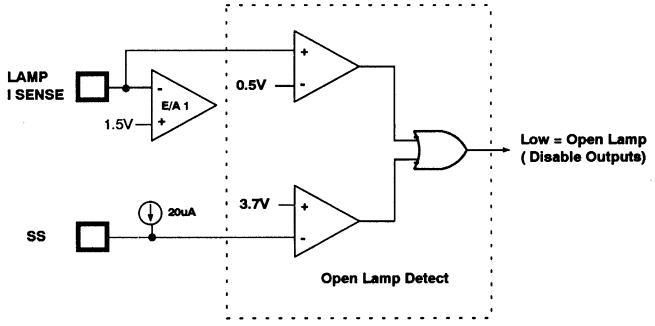


Figure 3

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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INTEGRATED CIRCUITS
UNITRODE

UC1875/6/7/8
UC2875/6/7/8
UC3875/6/7/8

Phase Shift Resonant Controller

FEATURES

- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation @ Switching Frequencies to 1MHz
- Four 2A Totem Pole Outputs
- 10MHz Error Amplifier
- Under Voltage Lockout
- Low Start-Up Current —150µA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Over-Current Comparator With Full Cycle Restart
- Trimmed Reference

Device	UVLO Turn-On	UVLO Turn-Off	Delay Set
UC1875	10.75	9.25V	Yes
UC1876	15.25V	9.25V	Yes
UC1877	10.75V	9.25V	No
UC1878	15.25V	9.25V	No

DESCRIPTION

The UC1875 family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

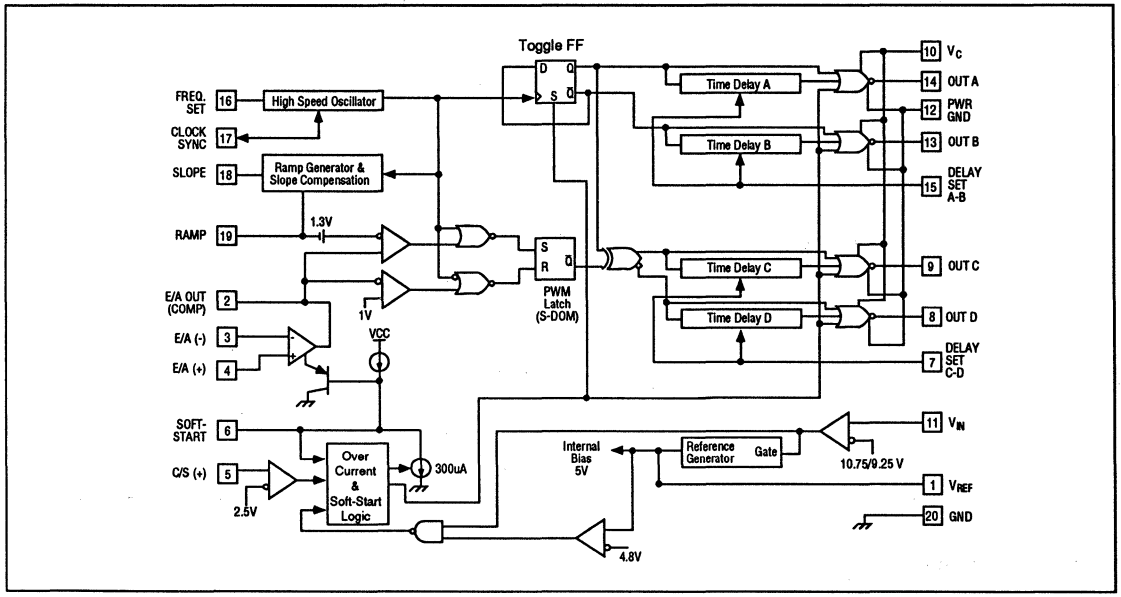
With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical . In addition to the standard free running mode, with the CLOCK/SYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an under-voltage lock-out which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold. 1.5V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided , and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

Additional features include an error amplifier with bandwidth in excess of 7MHz, a 5V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

These devices are available in 20-pin DIP, 28-pin "bat-wing" SOIC and 28 lead power PLCC plastic packages for operation over both 0°C to 70°C and -25°C to +85°C temperature ranges; and in hermetically sealed cerdip, and surface mount packages for -55°C to +125°C operation.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_C, V_{IN}) 20V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 3A
Analog I/Os (Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19) ..... -0.3 to 5.3V
Operating Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to + 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

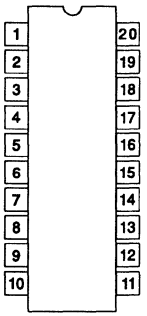
Note:
- Pin references are to 20 pin packages.
- All voltages are with respect to ground, DIL pin 20.
- Currents are positive into, negative out of, device terminals.
- Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

PACKAGE PIN FUNCTIONS

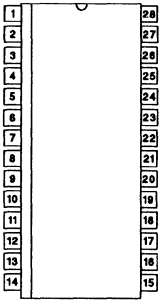
	PACKAGE TYPE and PIN NUMBER		
Function	**20-pin N, J**	**28-pin QP**	**28-pin DWP**
V_{REF}	1	19	1
E/A OUT (COMP)	2	20	2
E/A (-)	3	21	3
E/A (+)	4	22	4
C/S (+)	5	23	5
SOFT-START	6	24	6
DELAY SET C/D	7	25	10
OUT D	8	26	12
OUT C	9	27	13
V_C	10	28	14
V_{IN}	11	1	15
PWR GND	12	2	16
OUT B	13	3	17
OUT A	14	4	18
DELAY SET A/B	15	7	23
FREQ SET	16	8	24
CLOCK/SYNC	17	9	25
SLOPE	18	10	26
RAMP	19	11	27
GND	20	12-18	7-9,11,19-22, 28

CONNECTION DIAGRAMS

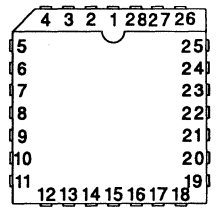
DIL-20 (TOP VIEW)
J or N PACKAGE



SOIC-28 (TOP VIEW)
DWP PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



Electrical Characteristics: Unless otherwise stated, V_C = V_{IN} = 12V, $R_{FREQ\ SET}$ = 12kΩ, $C_{FREQ\ SET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAY\ SET\ A-B}$ = $C_{DELAY\ SET\ C-D}$ = 0.01µF, $I_{DELAY\ SET\ A-B}$ = $I_{DELAY\ SET\ C-D}$ = -500µA, -55°C<T_A<125°C for the UC1875/6/7/8 -25°C<T_A<85°C for the UC2875/6/7/8 and 0°C<T_A<70°C for the UC3875/6/7/8 T_A=T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Under-Voltage Lockout					
Start Threshold	UC1875/UC1877		10.75		V
	UC1876/UC1878		15.25		V
UVLO Hysteresis	UC1875/UC1877		1.25		V
	UC1876/UC1878		6.0		V
Supply Current					
I_{IN} Startup	V_{IN} = 8V, V_C = 20V, R_{SLOPE} open, I_{DELAY} =0		150	600	µA
Ic Startup	V_{IN} = 8V, V_C = 20V, R_{SLOPE} open, I_{DELAY} =0		10	100	µA
I_{IN}			30	40	mA
Ic			15	30	mA

Electrical Characteristics: Unless otherwise stated, $V_C = V_{IN} = 12V$, $R_{FREQ\ SET} = 12k\Omega$, $C_{FREQ\ SET} = 330pF$, $R_{SLOPE} = 12k\Omega$, $C_{RAMP} = 200pF$, $C_{DELAY\ SET\ A-B} = C_{DELAY\ SET\ C-D} = 0.01\mu F$, $I_{DELAY\ SET\ A-B} = I_{DELAY\ SET\ C-D} = -500\mu A$, $-55°C<T_A<125°C$ for the UC1875/6/7/8, $-25°C<T_A<85°C$ for the UC2875/6/7/8, and $0°C<T_A<70°C$ for the UC3875/6/7/8, $T_A=T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Voltage Reference					
Output Voltage	T_J = + 25°C	4.95	5	5.05	V
Line Regulation	$11<V_{IN}<20V$		1	10	mV
Load Regulation	I_{VREF} = -10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.9		5.1	V
Noise Voltage	10Hz to 10kHz		50		μVrms
Long Term Stability	T_J = 125°C, 1000 hours		2.5		mV
Short Circuit Current	V_{REF} = 0V, T_J = 25°C		60		mA
Error Amplifier					
Offset Voltage			5	15	mV
Input Bias Current			0.6	3	μA
AVOL	$1 < V_{COMP} < 4V$	60	90		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		dB
PSRR	$11 < V_{IN} < 20V$	85	100		dB
Output Sink Current	V_{COMP}=1V	1	2.5		mA
Output Source Current	V_{COMP}=4V		-1.3	- 0.5	mA
Output Voltage High	I_{COMP} = -0.5mA	4	4.7	5	V
Output Voltage Low	I_{COMP} = 1mA	0	0.5	1	V
Unity Gain BW		7	11		MHz
Slew Rate		6	11		V/μsec
PWM Comparator					
Ramp Offset Voltage	T_J = 25°C, Note 3			1.3	V
Zero Phase Shift Voltage	Note 4	0.55	0.9		V
PWM Phase Shift	V_{COMP} > (Ramp Peak + Ramp Offset)	98	99.5	102	%
(Note 1)	V_{COMP} < Zero Phase Shift Voltage	0	0.5	2	%
Output Skew	V_{COMP} > Ramp Peak		5	±20	nsec
(Note 1)	V_{COMP} < 1V		5	±20	nsec
Ramp to Output Delay			50	100	nsec
Oscillator					
Initial Accuracy	T_J = 25°	0.85	1	1.15	MHz
Voltage Stability	$11 < V_{IN} < 20V$		0.2	2	%
Total Variation	Line, Temperature	0.80		1.20	MHz
Sync Pin Threshold	T_J = 25°C		3.8		V
Clock Out Peak	T_J = 25°C		4.3		V
Clock Out Low	T_J = 25°C		3.3		V
Clock Out Pulse Width	$R_{CLOCK/SYNC} = 3.9k\Omega$		30	100	nsec
Maximum Frequency	$R_{FREQSET} = 5k\Omega$	2			MHz
Ramp Generator/Slope Compensation					
Ramp Current, Minimum	$I_{SLOPE} = 10\mu A$, $V_{FREQ\ SET} = V_{REF}$		-11	-14	μA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQ\ SET} = V_{REF}$	-0.8	-0.95		mA
Ramp Valley			0		V
Ramp Peak - Clamping Level	$R_{FREQ\ SET} = 100k\Omega$	3.8	4.1		V
Current Limit					
Input Bias	VC/S+ = 3V		2	5	μA

Electrical Characteristics: Unless otherwise stated, $V_C = V_{IN} = 12V$, $R_{FREQ\ SET} = 12k\Omega$, $C_{FREQ\ SET} = 330pF$, $R_{SLOPE} = 12k\Omega$, $C_{RAMP} = 200pF$, $C_{DELAY\ SET\ A\text{-}B} = C_{DELAY\ SET\ C\text{-}D} = 0.01\mu F$, $I_{DELAY\ SET\ A\text{-}B} = I_{DELAY\ SET\ C\text{-}D} = -500\mu A$, $-55°C<T_A<125°C$ for the UC1875/6/7/8, $-25°C<T_A<85°C$ for the UC2875/6/7/8, and $0°C<T_A<70°C$ for the UC3875/6/7/8, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit (continued)					
Threshold Voltage		2.4	2.5	2.6	V
Delay to Output			70	125	nsec
Soft-Start/Reset Delay					
Charge Current	$V_{SOFT\text{-}START} = 0.5V$	-20	-9	-3	µA
Discharge Current	$V_{SOFT\ START} = 1V$	140	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level $I_{OUT} = 500mA$	$I_{OUT} = 50mA$		0.2	0.4	V
		1.2	2.6	V	
Output High Level $I_{OUT} = -500mA$	$I_{OUT} = -50mA$		1.5	2.5	V
		1.7	2.6	V	
Delay Set (UC1875 and UC1876 only)					
Delay Set Voltage	$I_{DELAY} = -500\mu A$	2.3	2.4	2.6	V
Delay Time	$I_{DELAY} = -250\mu A$ (NOTE 5)	150	250	400	nsec

Note 1: Phase shift percentage (0% = 0°, 100% = 180°) is defined as

$$\theta = \frac{200}{T}\ \Phi\ \%,$$

where θ is the phase shift, Φ and T are defined in Figure1.
At 0% phase shift, Φ is the output skew.

Note 2: Delay time is defined as

$$\text{delay} = T\left(\frac{1}{2} - (\text{duty cycle})\right),$$

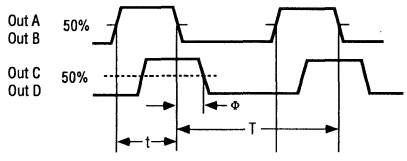
where T is defined in figure 1.

Note 3: Ramp offset voltage has a temperature coeffecient of about -4mV/°C.

Note 4: Zero phase shift voltage has a temperature coeffecient of about -2mV/°C.

Note 5: Delay time can be programmed via resistors from the delay set pins to ground. Delay time $\cong \frac{62.5 \times 10^{-12}}{I_{DELAY}}$ sec.

Where $I_{DELAY} = \frac{\text{Delay set voltage}}{R_{DELAY}}$ The recommended range for I_{DELAY} is $25\mu A \le I_{DELAY} \le 1mA$



Duty Cycle = $\frac{t}{T}$
Period = T
T_{DHL} (A to C) = T_{DHL} (B to D) = Φ

Phase Shift, Output Skew & Delay Time Definitions

FIGURE 1

PIN FUNCTIONAL DESCRIPTION

GND (signal ground):
All voltages are measured with respect to GND. The timing capacitor, on the FREQ SET pin, any bypass capacitor on the V_{REF} pin, bypass capacitors on V_{IN} and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

PWR GND (power ground):
V_C should be bypassed with a ceramic capacitor from the Vc pin to the section of the ground plane that is connected to PWR GND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

Vc (output switch supply voltage):
This pin supplies power to the output drivers and their associated bias circuitry. Connect Vc to a stable source above 3V for normal operation, above 12V for best performance. This supply should be bypassed directly to the PWR GND pin with low ESR, low ESL capacitors.

V_{IN} (primary chip supply voltage):
This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect V_{IN}

PIN FUNCTIONAL DESCRIPTION (CONTINUED)

to a stable source above 12V for normal operation. To ensure proper chip functionality, these devices will be inactive until V_{IN} exceeds the upper under-voltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When V_{IN} exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100uA to a current in excess of 20mA. If the UC1875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

FREQ SET (oscillator frequency set pin)
A resistor and a capacitor from FREQ SET to GND will set the oscillator frequency according to the following relationship:

$$f \approx \frac{4}{R_{FREQSET} \cdot C_{FREQSET}}$$

CLOCK/SYNC (bi-directional clock and synchronization pin):
Used as as output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCK/SYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

SLOPE (set ramp slope/slope compensation):
A resistor from this pin to Vcc will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

RAMP (voltage ramp):
This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{sense voltage}}{R_{SLOPE} \cdot C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation - see the applications information section for further information.
Because of the 1.3V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

E/A OUT (COMP) (Error amplifier output):
This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

E/A - (Error Amplifier inverting input):
This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

E/A+ (Error Amplifier non-inverting input):
This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A- pin.

SOFT-START:
SOFT-START will remain at GND as long as V_{IN} is below the UVLO threshold. SOFT-START will be pulled up to about 4.8V by an internal 9µA current source when V_{IN} becomes valid (assuming a non-fault condition). In the event of a current-fault (C/S+ voltage exceeding 2.5V), SOFT-START will be pulled to GND and them ramp to 4.8V. If a fault occurs during the SOFT-START cycle, the outputs will be immediately disabled and SOFT-START must charge fully prior to resetting the fault latch.
For paralleled controllers, the SOFT-START pins may be paralled to a single capacitor, but the charge currents will be additive.

C/S+ (current sense):
The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5V (separate from V_{REF}). When the voltage at this pin exceeds 2.5V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled from switching and held in a low state until the C/S+ pin is brought below 2.5V. The outputs may begin switching at 0 degrees phase shift before the SOFT-START pin begins to rise -- this condition will not prematurely deliver power to the load.

OUT A-OUT D (outputs A-D):
The outputs are 2A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with recpect to the A-B outputs.

DELAY SET A-B, DELAY SET C-D (output delay control):
The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

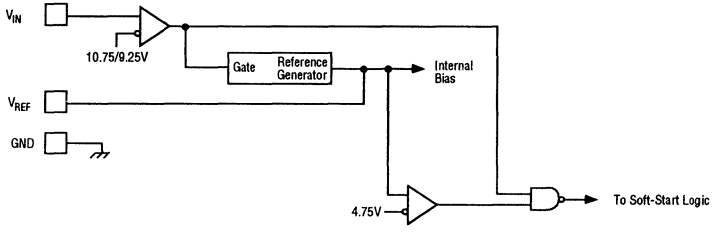
V_{REF}:
This pin is an accurate 5V voltage reference. This output is capable of delivering about 60mA to peripheral circuitry and is internally short circuit current limited. V_{REF} is disabled while V_{IN} is low enough to force the chip into UVLO. The circuit is also in UVLO until V_{REF} reaches approximately 4.75V. For best results bypass V_{REF} with a 0.1uF, low ESR, low ESL, capacitor to the GND pin.

APPLICATIONS INFORMATION

UNDER VOLTAGE LOCKOUT SECTION

When power is applied to the circuit and V_{IN} is below the upper UVLO threshold, I_{IN} will be below 600µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low.

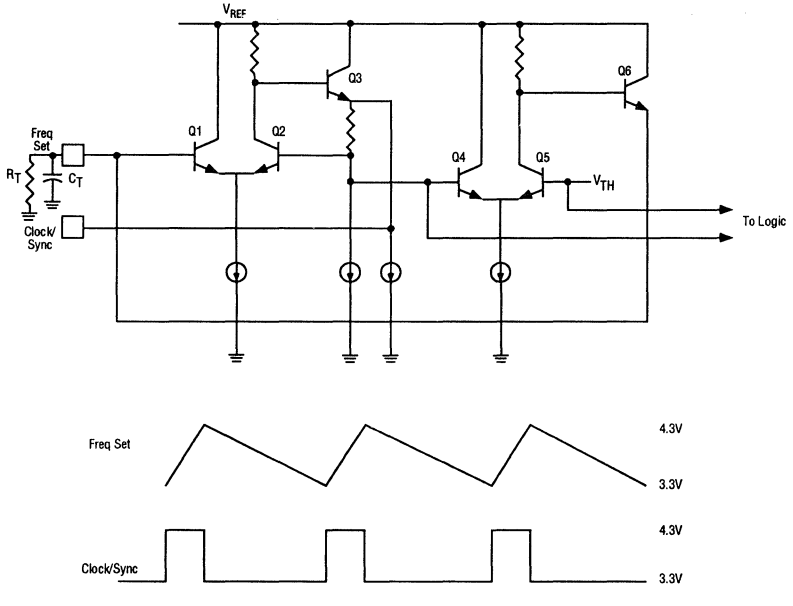
When V_{IN} exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, V_{REF}, exceeds 4.75V



OSCILLATOR

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQ. SET pin.

SIMPLIFIED OSCILLATOR SCHEMATIC

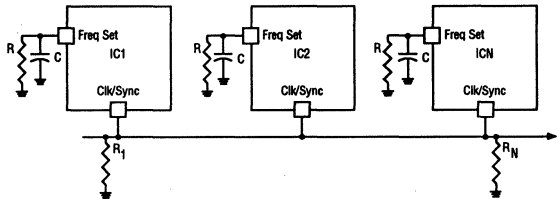


The CLOCK/SYNC pin of the oscillator may be used to synchronize multiple UC1875 devices simply by connecting the CLOCK/SYNC of each UC1875 to the others:

APPLICATIONS INFORMATION (CONTINUED)

SYNCHRONIZING THE OSCILLATOR

1875/6/7/8's only

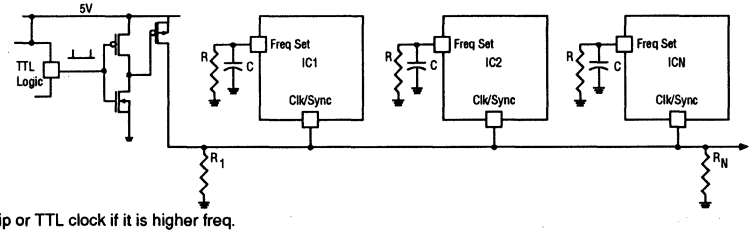


All ICs will sync to chip with the fastest local oscillator.

R_1 & R_N *may* be needed to keep sync pulse narrow due to capacitance on line.

R_1 & R_N *may* also be needed to properly terminate rsync line.

Syncing to external TTL/CMOS



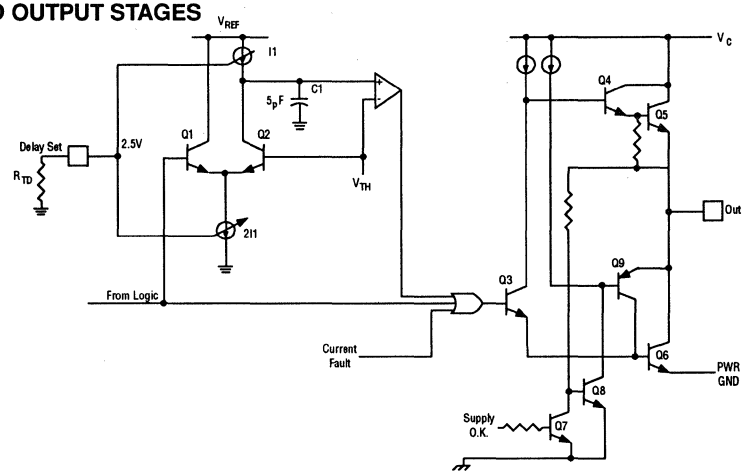
ICs will sync to fastest chip or TTL clock if it is higher freq.
R & R_N *may* be needed for same reasons as above

Although each UC1875/6/7/8 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCK/SYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.
Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in the previous figure. Capacitive loading on the CLOCK/SYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCK/SYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1,RN.

DELAY BLOCKS AND OUTPUT STAGES

In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.

SIMPLIFIED OUTPUT STAGES

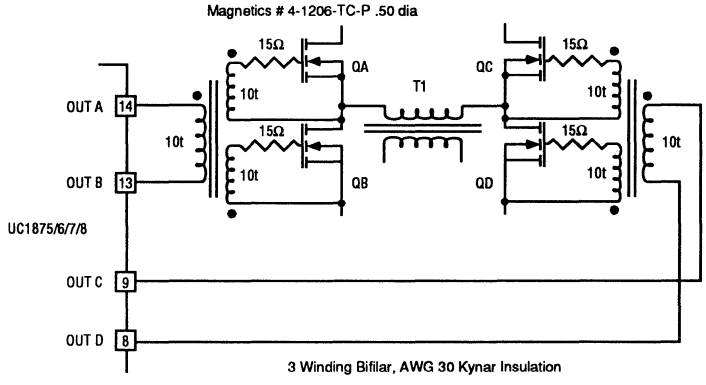


The delay providing the dead-time is accomplished with C1 which must discharge to Vth before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, RTD. The voltage on the Delay Set pins is internally regulated to 2.5V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuity, and the delay time must be programmed.

APPLICATIONS INFORMATION (CONTINUED)

OUTPUT SWITCH ORIENTATION

The four outputs of the UC1875/6/7/8 interace to the full bridge converter switches as shown below:



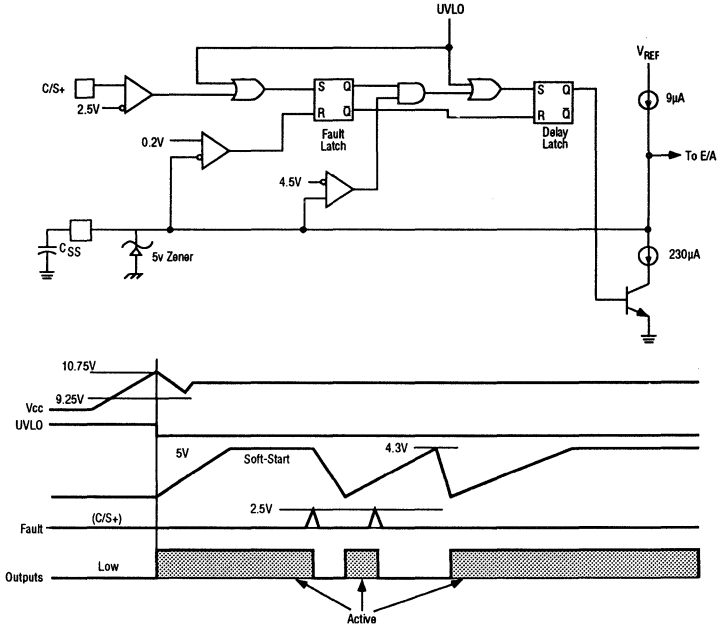
FAULT LOGIC

The fault control circuitry provides two forms of power shutdown:

- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFT-START pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.
The fault logic insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.

FAULT/SOFT-START



APPLICATIONS INFORMATION (CONTINUED)

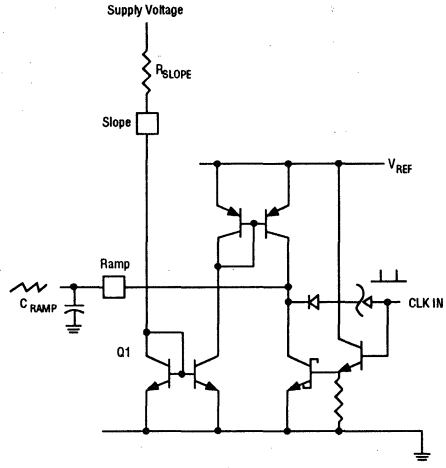
RAMP GENERATION

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

SLOPE/RAMP PINS

Voltage Mode Operation



1. Simple voltage mode operation achieved by placing RSLOPE between VIN & SLOPE

2. Voltage Feedforward achieved by placing RSLOPE between supply voltage and slope pin of UC1875.

Ramp

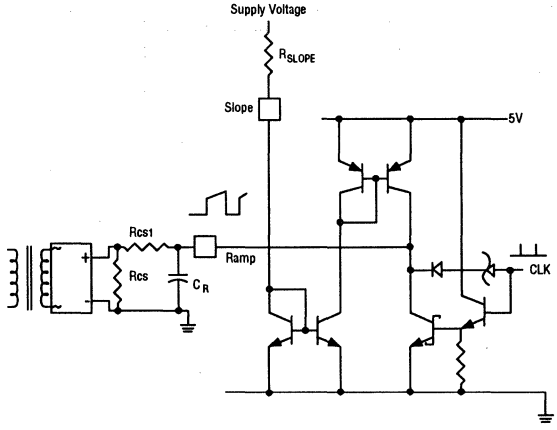
$$\frac{dV}{dT} \approx \frac{V_{RSLOPE}}{R_{SLOPE}\ C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator. Figure 7 shows a current-mode configuration with slope compensation. Rcs reconstructs the current wafeform from a current-sense transformer while the voltage across C_R adds a compensating ramp. Note that Rcs should be of a sufficiently low value to allow C_R to be fully discharged by the ramp circuitry.

Current Mode Slope Compensation/Operation

Added slope

$$\frac{dV}{dT} \approx \frac{V_{RSLOPE}}{R_{SLOPE}\ CR}$$



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UC1891/2/3/4
UC2891/2/3/4
UC3891/2/3/4

Two Stage Power Factor Converter

PRELIMINARY

FEATURES

- Single Chip Solution for Power Factor Corrected Power Systems
- Worldwide Operation Without Switches
- Fixed Frequency PWM Drive for Both Pre- and Post- Regulators
- Low Offset Analog Multiplier/Divider
- 5 MHz, Low Offset Current Amplifier
- Trimmed ±6% Oscillator Frequency
- Over Voltage Fault Comparator
- Low Icc Startup Current, 650µa Typical
- Trimmed ±1% 7.5V Reference
- Independent Maximum Multiplier Output Current Clamp
- 15/10V, 11/10V UVLO Thresholds
- Single-Ended or Double-Ended Post-Regulator Output Configurations
- 1A Totem Pole MOSFET Drivers

DESCRIPTION

The UC1891/2/3/4 family of power supply controller ICs combine an active Power Factor corrected boost pre-regulator with a Voltage mode PWM down converter for post regulation. Line voltage feedforward in the pre-regulator allows the converter to achieve near unity power factor over the full international range of line voltages. The post regulator is configurable for either single-ended or push-pull topologies providing a true single chip solution for PFC power systems.

The boost pre-regulator front end is implemented with line-compensated, average current mode control, for low distortion, continuous input current. Average current mode control accurately maintains sinusoidal line current without the need for slope compensation, unlike peak current mode control. The pre-regulator employs a low offset high bandwidth current amplifier, a separate voltage amplifier, an analog multiplier/divider, 1A totem pole MOSFET driver, and latched overvoltage and overcurrent comparators.

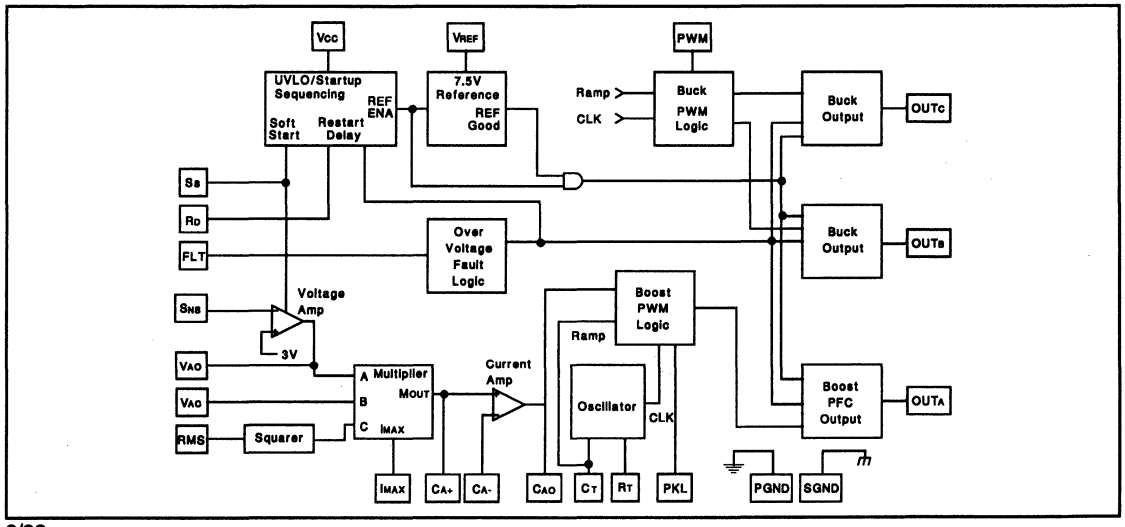
The PWM post-regulator section is configurable as either a single-ended or double-ended controller. A PWM comparator, PWM latch, toggle FF, and Dual 1A totem pole MOSFET drivers are included to realize the desired configurations. Voltage control can be implemented through an optical coupler from an isolated output.

An accurate fixed-frequency oscillator provides synchronization for both controllers. Restart delay and softstart circuits deliver highly predictable startup and fault management for the controllers. Part selectable UVLO thresholds provide the flexibility to start the controller from an auxiliary winding or a separate 12V regulator.

Additional features include low (1mA) startup current, a 1% trimmed 7.5V reference, and an independent multiplier maximum output current clamp.

These devices are available in the 28-pin QP package as well as the 24-pin J and 24-pin N packages.

BLOCK DIAGRAM

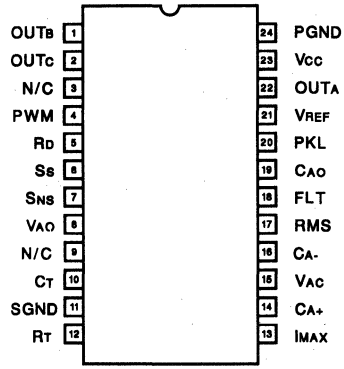


PRODUCT SCHEDULE

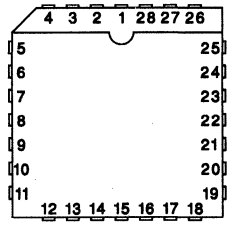
		Post Regulator Outputs	
		Alternating (Max DC < 50%)	Parallel (Max DC < 100%)
UVLO Thresholds	15V on, 10V off	1891	1893
	11V on, 10V off	1892	1894

CONNECTION DIAGRAM

DIL-24 (TOP VIEW)
N or J PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



PACKAGE PIN FUNCTIONS	
Function	Pin #
IMAX	1
CA+	2
VAC	3
CA-	4
RMS	5
FLT	6
CAO	7
PKL	8
VREF	9
OUTA	10
VCC	11
PGND	12-18
OUTB	19
OUTC	20
RD	22
SS	23
SNS	24
VAO	25
CT	26
SGND	27
RT	28

ELECTRICAL CHARACTERISTICS:

Unless specified V_{CC}=18V, R_T=15k, C_T=1.5nF, R_{IMAX}=15k, PKL=1V, V_{RMS}=1.5V, I_{VAC}=100µA, V_{CA-}=0V C_{AO}=3V, V_{AO}=5V, V_{SNS}=3.0V, -55°C < T_A < 125°C for the UC189X, -40°C < T_A < 85°C for the UC289X, and 0°C < T_A < 70°C for the UC389X, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Off	C_{AO}, V_{AO} = 0V, V_{CC} = UVLO-0.5V		600	1200	µA
Supply Current, On			25	30	mA
Vcc Turn-on Threshold	1891, 1893		15	16	V
Vcc Turn-off Threshold		9	10		V
Vcc Turn-on Threshold	1892, 1894		11	11.5	V
Vcc Turn-off Threshold		9	10		V
Voltage Amplifier					
Input Voltage	V_{AOUT} = 3.5V	2.9		3.1	V
V_{SENSE} Bias Current		-500	25	500	nA
Open Loop Gain	V_{AOUT}=2 to 6V	70	100		dB
V_{OUT} High	I_{LOAD} = -200µA		5.8		V
V_{OUT} Low	I_{LOAD} = 200µA		0.3	0.5	V
Output Short Circuit Current	V_{AOUT} = 0V		1.5	2.2	mA
Gain Bandwidth Product	F_{IN}=100kHz, 10mV p-p		1		mHz

ELECTRICAL CHARACTERISTICS (cont.): Unless specified V_{CC}=18V, R_T=15k, C_T=1.5nF, R_{IMAX}=15k, PKL=1V, V_{RMS}=1.5V, I_{VAC}=100µA, V_{CA}-=0V C_{AO}=3V, V_{AO}=5V, V_{SNS}=3.0V, -55°C < T_A < 125°C for the UC189X, –40°C < T_A < 85°C for the UC289X, and 0°C < T_A < 70°C for the UC389X, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amplifier					
Input Offset Voltage		-1		2	mV
Input Bias Current (sense)		-500		500	nA
Gain		80	110		dB
Output Swing	0.5 to 7.5V				
Short Circuit Current	CA_{OUT} = 0V		1.5	2	mA
PSRR	V_{CC} = 12 to 24V	65	85		dB
Common Mode Range		-0.3		4	V
Gain Bandwidth Product	F_{IN} = 100 kHz, 10mV p-p	2	3.5		mHz
Reference					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.425	7.5	7.575	V
	I_{REF} = 0mA	7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA	-15		15	mV
Line Regulation	V_{CC} = 15 to 35V	-10		10	mV
Short Circuit Current	V_{REF} = 0V	15	40	70	mA
Oscillator					
Initial Accuracy	T_A = 25°C	48		53	kHz
Voltage Stability	V_{CC} = 12 to 18V		1		%
Total Variation	Line, Temp	45		55	kHz
Ramp Amplitude (p-p)		4.8		5.6	V
Ramp Valley Voltage		0.8		1.3	V
Fault Management					
Fault Comparator V_{TH}		1.9	2	2.1	V
Fault Comp Input Bias	V_{FAULT} = 2.5V		0.3	3	µA
Fault Propagation Delay			250		ns
Ss Charge Current	$V_{SOFTSTART}$ = 2.5V	3	10	20	µA
PK Limit Offset Voltage		-10		10	mV
PK Limit Input Current	$V_{PKLIMIT}$ = -0.1V	-200	-100		µA
PK Limit Prop. Delay			200		ns
Multiplier					
Output Current - I_{AC} Limited	I_{AC} = 100µA, V_{RMS} = 1V	-220	-200	-180	µA
Output Current - Zero	I_{AC} = 0µA	-2	-0.2	2	µA
Output Current - R_{MULT} Limited	I_{AC} = 500µA	-280	-250	-220	µA
Output Current - Power Limited	I_{AC} = 100µA, V_{RMS} = 1.5V, V_A = 5.6V	-230	-205	-180	µA
Output Current	I_{AC} = 100µA, V_{RMS} = 1.5V, V_A = 2V	-55	-45	-35	µA
Output Current	I_{AC} = 100µA, V_{RMS} = 1.5V, V_A = 5V	-215	-180	-145	µA
Output Current	I_{AC} = 100µA, V_{RMS} = 5V, V_A = 2V	-20	-4	0	µA
Output Current	I_{AC} = 100µA, V_{RMS} = 5V, V_A = 5V	-25	-16	5	µA
Gain Constant	Refer to Note 1		-1		
Gate Drivers A, B, C					
Output High Clamp Voltage	No load, V_{CC} = 18 to 35V	14	15	16	V
Output High Voltage	I_{OUT} = -200mA, V_{CC} = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA	1.6	2.2		V
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V

ELECTRICAL CHARACTERISTICS (cont.): Unless specified V_{CC}=18V, R_T=15k, C_T=1.5nF, R_{IMAX}=15k, PKL=1V, V_{RMS}=1.5V, I_{VAC}=100µA, V_{CA}-=0V C_{AO}=3V, V_{AO}=5V, V_{SNS}=3.0V, –55°C < T_A < 125°C for the UC189X, –40°C < T_A < 85°C for the UC289X, and 0°C < T_A < 70°C for the UC389X, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drivers A, B, C (cont.)					
Output RISE/FALL Time	C_{LOAD} = 1nF		35		ns
Output Peak Current	C_{LOAD} = 10nF		1		A
Deadtime (B & C only)	C_T = 1nF		600		ns

Note 1. Gain Constant (k) = $\frac{I_{AC}(V_{AC} - 1V)}{V_{RMS}^2 \times I_{MO}}$

where: I_{MO} = *Multiplier Ouput Current*
$1.5V \le V_{RMS} \le 5.0V$
$2.0V \le V_{AO} \le 5.0V$

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INTEGRATED CIRCUITS
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UC1901
UC2901
UC3901

Isolated Feedback Generator

FEATURES

- An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal
- Low-Cost Alternative to Optical Couplers
- Internal 1% Reference and Error Amplifier
- Internal Carrier Oscillator Usable to 5mHz
- Modulator Synchronizable to an External Clock
- Loop Status Monitor

DESCRIPTION

The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

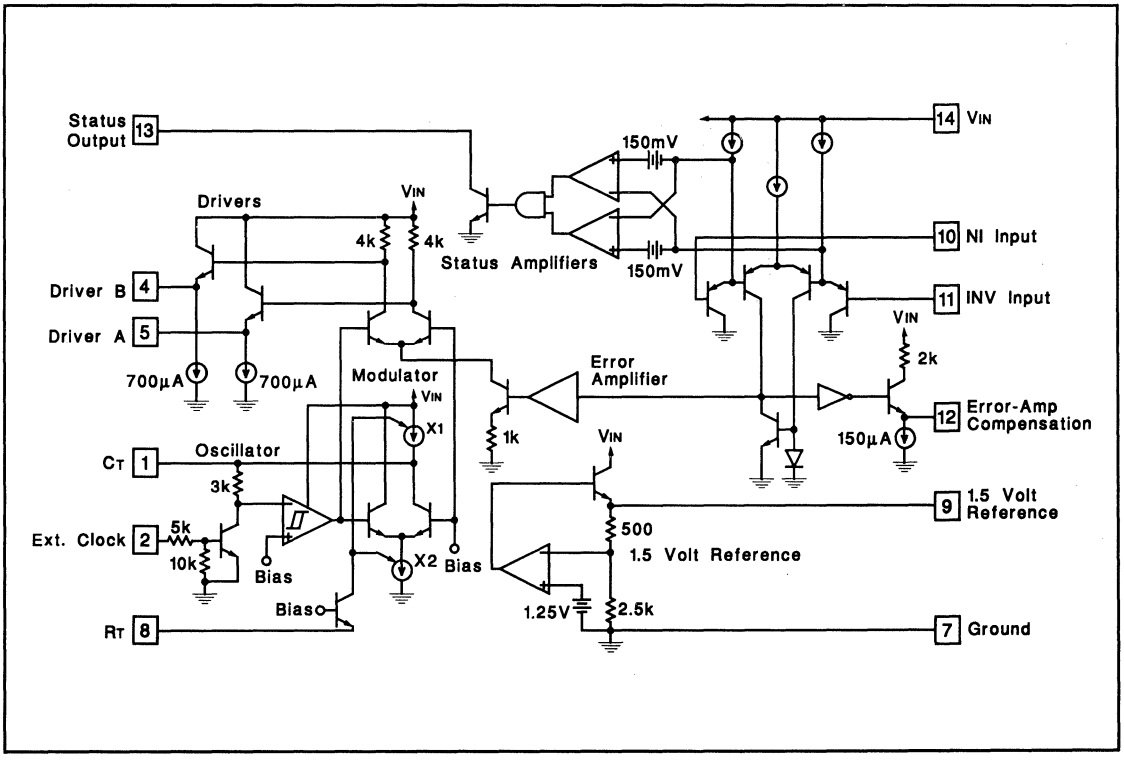
The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

5

UC1901 SIMPLIFIED SCHEMATIC



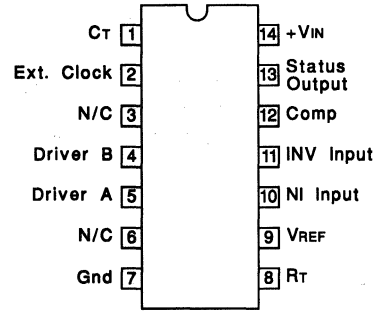
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN} 40V
Reference Output Current ..... -10mA
Driver Output Currents ..... -35mA
Status Indicator Voltage 40V
Status Indicator Current 20mA
Ext. Clock Input 40V
Error Amplifier Inputs ..... -0.5V to +35V
Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

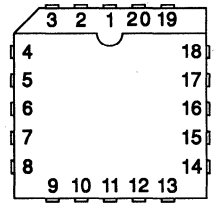
Note 1: Voltages are referenced to ground, Pin 7. Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (TOP VIEW)
J or N Package, D Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
CT	2
N/C	3
Ext. Clock	4
Driver B	5
N/C	6
Driver A	7
N/C	8
N/C	9
Gnd	10
N/C	11
RT	12
VREF	13
N/C	14
NI Input	15
N/C	16
INV Input	17
Comp	18
Status Output	19
+VIN	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 55°C to +125°C for the UC1901; -40°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, T_A = T_J.

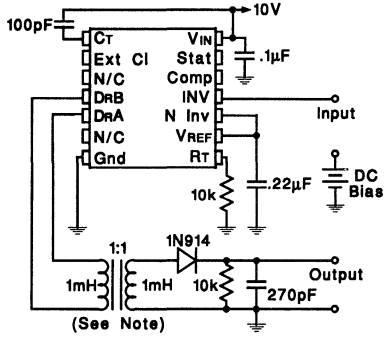
PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \le T_J \le T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_J = 25°C		-35	-55		-35	-55	mV
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		-1	-3		-1	-6	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 2 to 25V	80	100		80	100		dB
Output Swing, Δ Vo		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		µA
Maximum Source Current		-2	-3		-2	-3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/µS
Modulators/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V

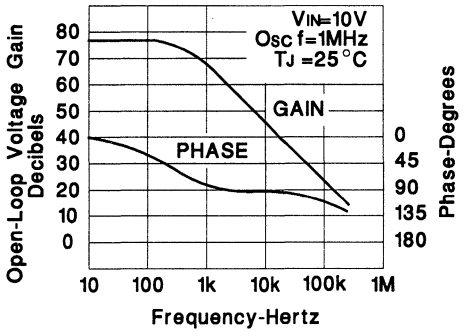
ELECTRICAL CHARACTERISTICS (cont.):

Unless otherwise stated, these specifications apply for T_A = 55°C to +125°C for the UC1901; -40°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, $T_A = T_J$.

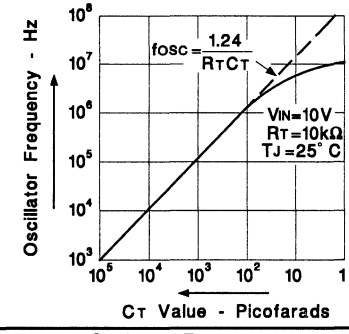
PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Modulators/Drivers Section (cont.)								
Driver Sink Current		500	700		500	700		µA
Driver Source Current		-15	-35		-15	-35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_J = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \le T_J \le T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10k, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A ΔInput = 0.2V		.05	1		.05	5	µA
Supply Current	V_{IN} = 35V		5	8		5	10	mA

Transformer Coupled Open Loop Transfer Function

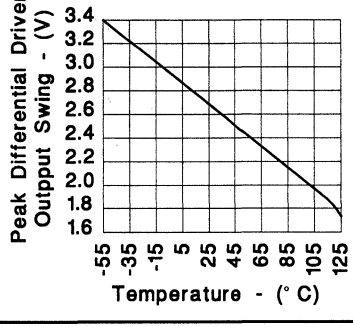




Transformer Data: N1 = N2 = 20TAWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O.D. toroid
Carrier Frequency = 1MHz



Oscillator Frequency



Typical Driver Output Swing vs Temperature

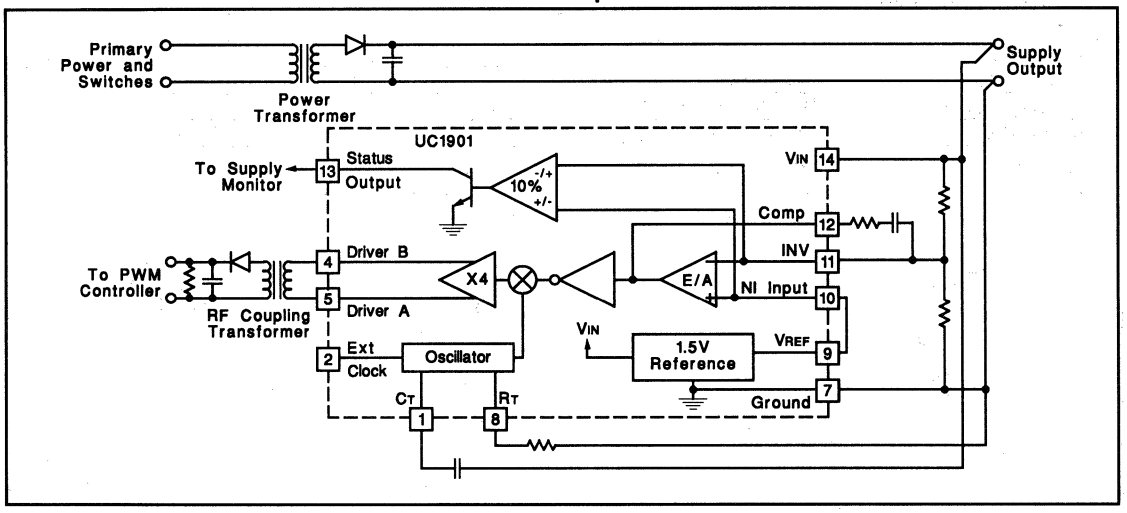
APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

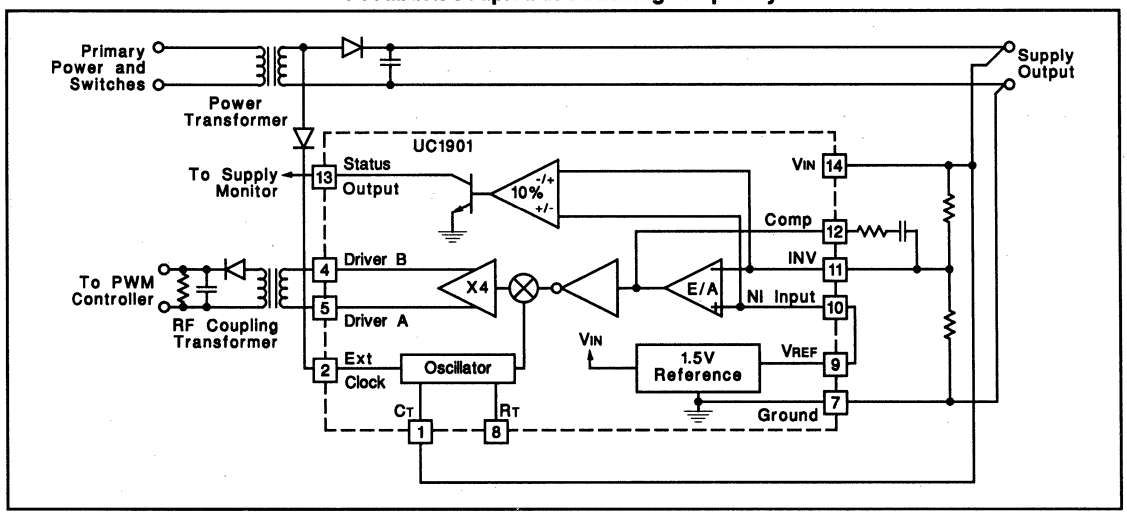
The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_R, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is not clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700μA, can be increased by adding resistors to ground at the driver outputs.

R.F. Transformer Coupled Feedback

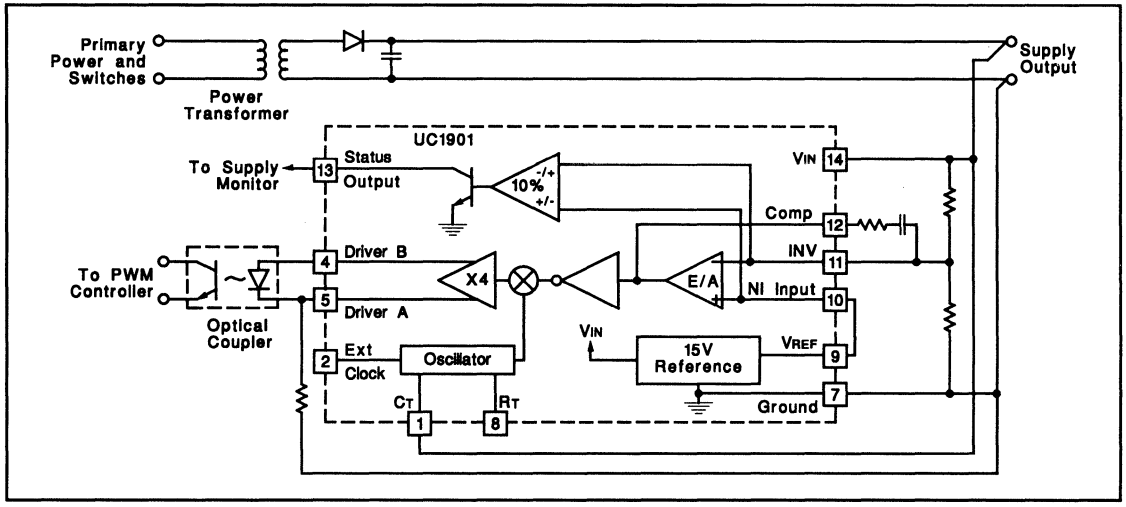


Feedback Coupled at Switching Frequency



TYPICAL APPLICATIONS

Optically Coupled DC Feedback



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INTEGRATED CIRCUITS
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UC1903
UC2903
UC3903

Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring up to Four Separate Supply Voltage Levels
- Internal Inverter for Sensing a Negative Supply Voltage
- Line/Switch Sense Input for Early Power Source Failure Warning
- Programmable Under- and Over-Voltage Fault Thresholds with Proportional Hysteresis
- A Precision 2.5V Reference
- General Purpose Op-Amp for Auxiliary Use
- Three High Current, >30mA, Open-Collector Outputs Indicate Over-Voltage, Under-Voltage and Power OK Conditions
- Input Supply Under-Voltage Sensing and Start-Latch Eliminate Erroneous Fault Alerts During Start-Up
- 8-40V Supply Operation with 7mA Stand-By Current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

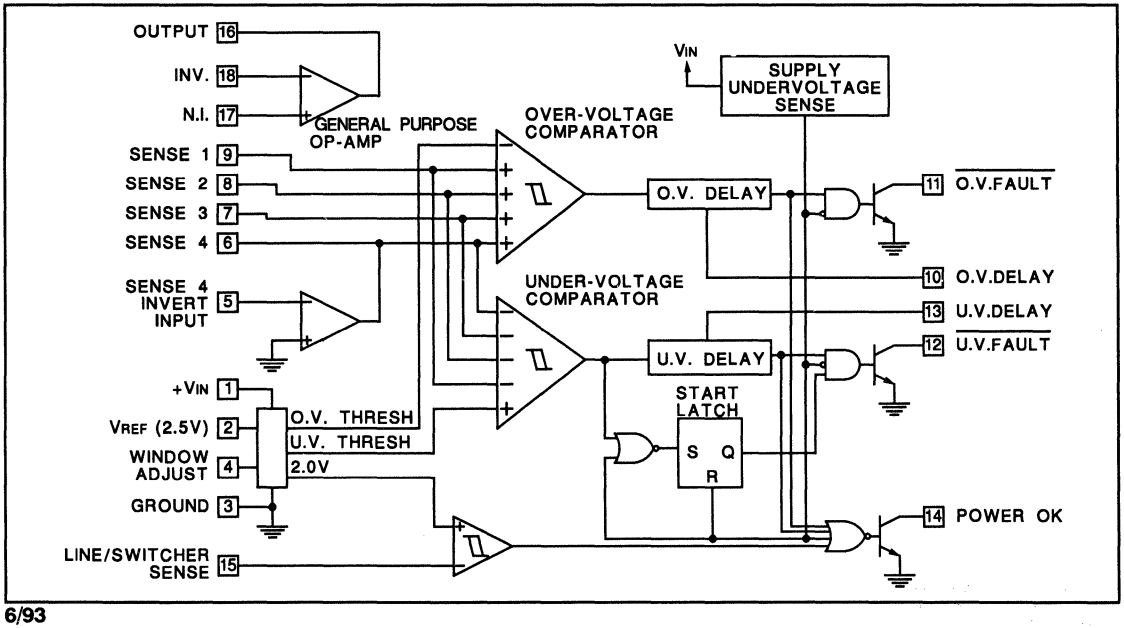
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8V to 40V input supply range and require a typical stand-by current of only 7mA.

BLOCK DIAGRAM



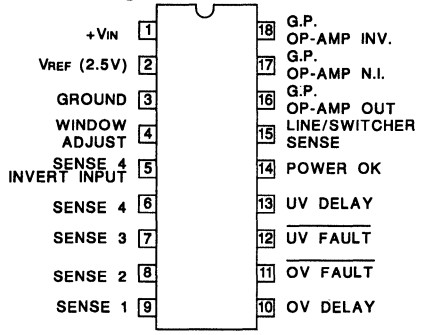
6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+VIN) ..... +40V
Open Collector Output Voltages ..... +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages ..... -0.3V to +20V
Line/Switcher Sense Input Voltage ..... -0.3V to +40V
Op-Amp and Inverter Input Voltages ..... -0.3V to +40V
Op-Amp and Inverter Output Currents ..... -40mA
Window Adjust Voltage ..... 0.0V to +10V
Delay Pin Voltages ..... 0.0V to +5V
Reference Output Current ..... -40mA
Power Dissipation at TA = 25°C (Note 1) 1000mW
Power Dissipation at TC = 25°C (Note 1) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

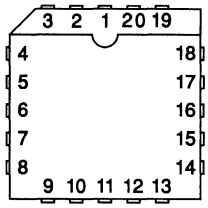
Note 1: Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20
(TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
VREF (2.5V)	2
GROUND	3
GROUND SENSE	4
WINDOW ADJUST	5
N/C	6
SENSE 4 INVERT INPUT	7
SENSE 4	8
SENSE 3	9
SENSE 2	10
SENSE 1	11
OV DELAY	12
$\overline{\text{OV FAULT}}$	13
$\overline{\text{UV FAULT}}$	14
UV DELAY	15
POWER OK	16
LINE/SWITCHER SENSE	17
G.P. OP-AMP OUT	18
G.P. OP-AMP N.I.	19
G.P. OP-AMP INV.	20

5

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TA = 55°C to +125°C for the UC1903; -40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; +VIN = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; VPIN 4 = 1.0V, TA = TJ.

PARAMETERS	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply								
Input Supply Current	No Faults		7	9		7	11	mA
	UV, OV and Line Fault		10	15		10	18	mA
Supply Under Voltage Threshold (VSUV)	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output			3.0	4.0		3.0	4.0	V
Reference								
Output Voltage (VREF)	TJ = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465		2.535	2.465		2.535	V
Load Regulation	IL = 0 to 10mA		1	10		1	15	mV
Line Regulation	+VIN = 8 to 40V		1	4		1	8	mV
Short Circuit Current	TJ = 25°C		40			40		mA
Fault Thresholds								
0V Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = Low to High, 0.5V ≤ VPIN 4 ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = High to Low, 0.5V ≤ VPIN 4 ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V

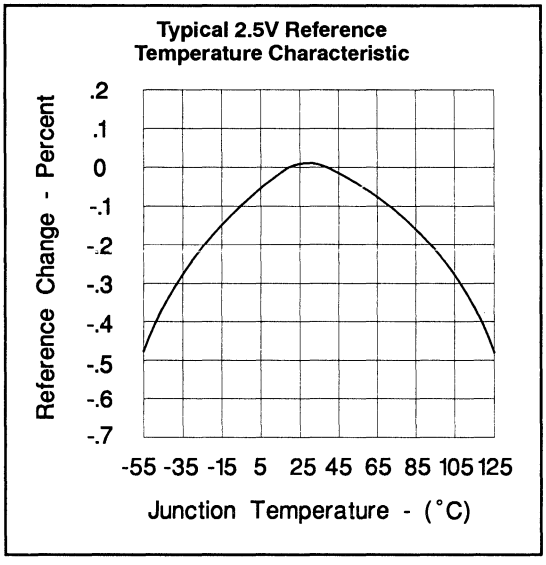
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 55°C to +125°C for the UC1903; -40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V, T_A = T_J.

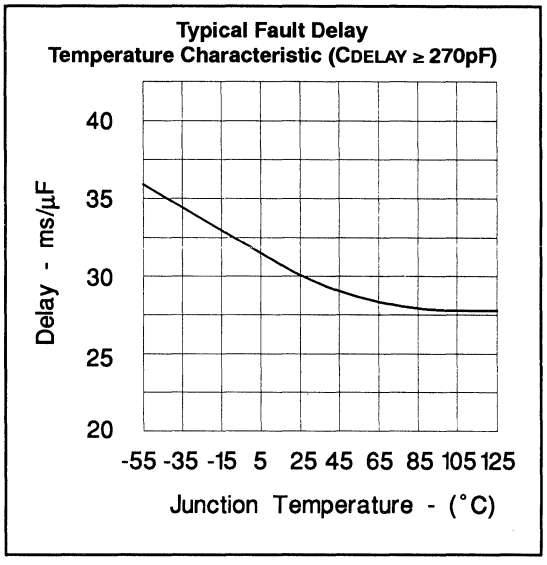
PARAMETERS	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Fault Thresholds (cont.)								
0V & UV Threshold Hyst.	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	10	20	30	10	20	30	mV/V
0V & UV Threshold Supply Sensitivity	$+V_{IN}$ = 8V to 40V		.002	.01		.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V		±1	±10		±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)		1	3		1	6	µA
	Input = 2.2 (Note 2)		-1	-3		-1	-6	µA
Line Sense Input Bias Current	Input = 2.3V (Note 2)		1	3		1	6	µA
0V and UV Fault Delay								
Charging Current			60			60		µA
Threshold Voltage	Delay Pin = Low to High		1.8			1.8		V
Threshold Hysteresis	T_J = 25°C		250			250		mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/µF
Fault Outputs ($\overline{0V}$, $\overline{UV}$, & Power 0K)								
Maximum Current	V_{OUT} = 2V	30	70		30	70		mA
Saturation Voltage	I_{OUT} = 12mA		.25	.40		.25	.40	V
Leakage Current	V_{OUT} = 40 V		3	25		3	25	µA
Sense 4 Inverter (Note 3)								
Input Offset Voltage			2	8		2	10	mV
Input Bias Current			.1	2		.1	4	µA
Open Loop Gain		65	80		65	80		dB
PSRR	$+V_{IN}$ = 8 to 40 V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA
G.P. Op-Amp (Note 3)								
Input Offset Voltage			1	5		1	8	mV
Input Bias Voltage			.1	2		.1	4	µA
Input Offset Current			.01	.5		.01	1.0	µA
Open Loop Gain		65	120		65	120		dB
CMRR	V_{CM} = 0 to $+V_{IN}$ = 2.0V	65	100		65	100		dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA

Note 2: These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

Note 3: When either the G.P. OP-Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤ 1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.

Note 4: Reference to pin numbers in this specification pertain to 18 pin DIL N and J packages.





5

OPERATION AND APPLICATION INFORMATION

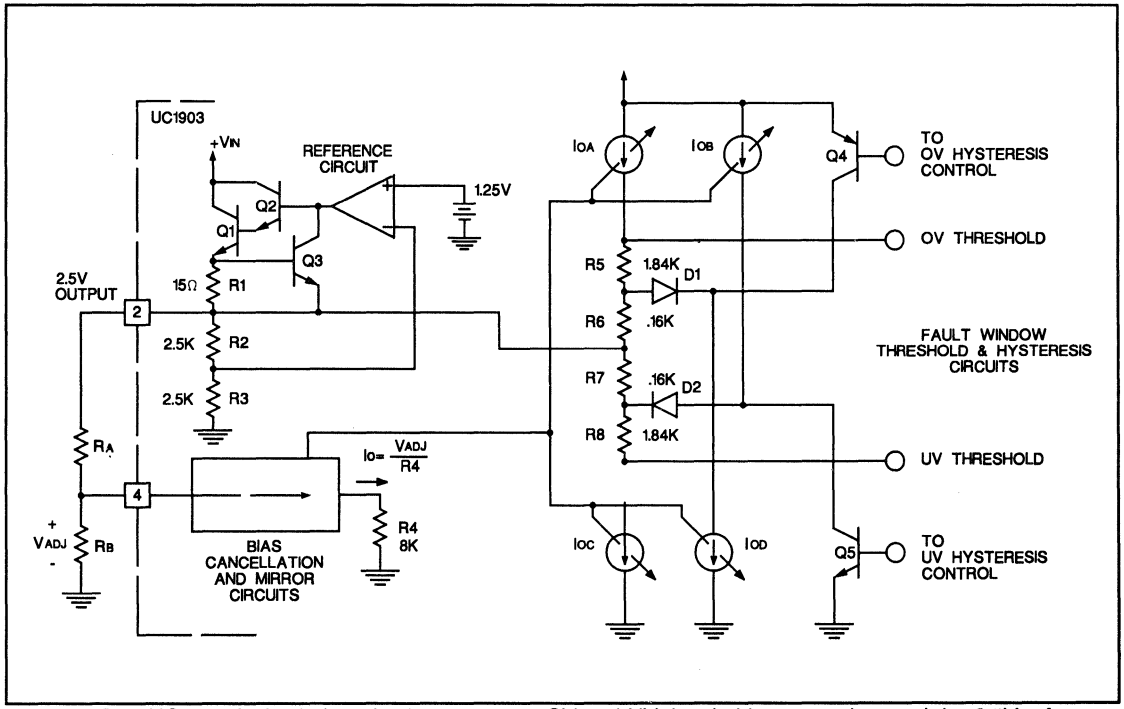


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, and an 8k resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_5 are turned on. In combination with D_1 and D_2 this prevents L_{OB} and L_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_8)$ respectively. The fault window can be expressed as:

$$(1) \qquad 2.5V \pm \frac{V_{ADJ}}{4}.$$

In terms of a sensed nominal voltage level, Vs, the window as a percent variation is:

$$(2) \qquad Vs \pm (10 \cdot V_{ADJ})\ \%.$$

When a sense input moves outside the fault window given in equation(1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

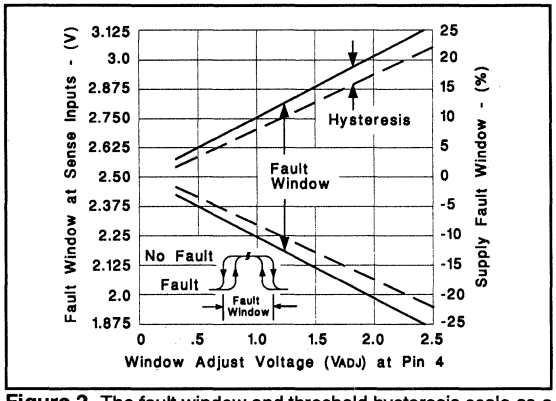


Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can Be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

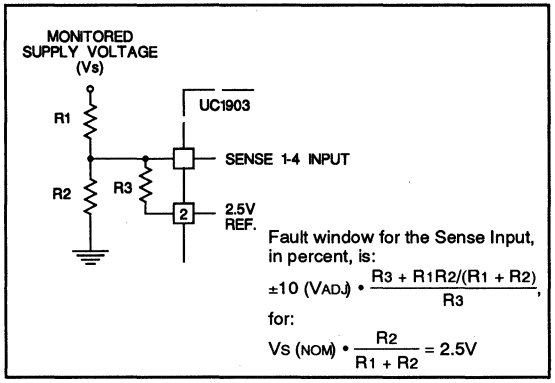


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

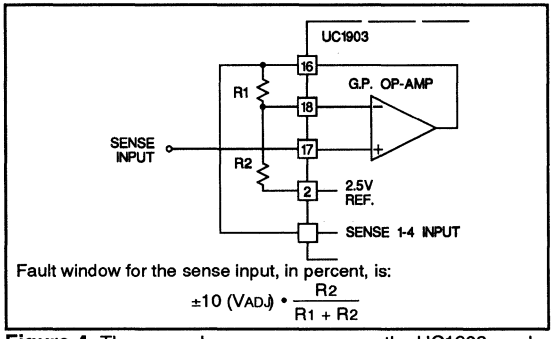


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability. ≥20mA while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

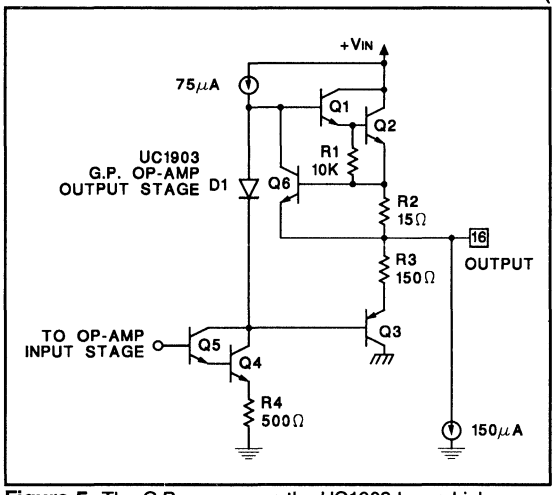
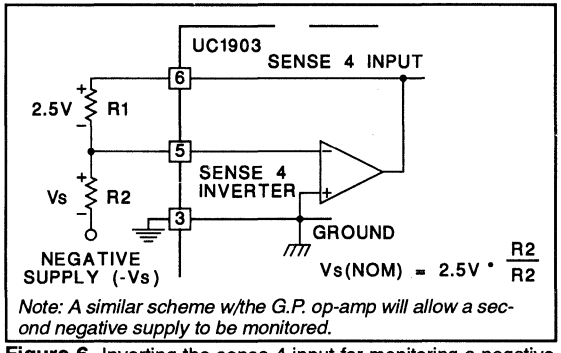


Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of the inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.



Note: A similar scheme w/the G.P. op-amp will allow a second negative supply to be monitored.

Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

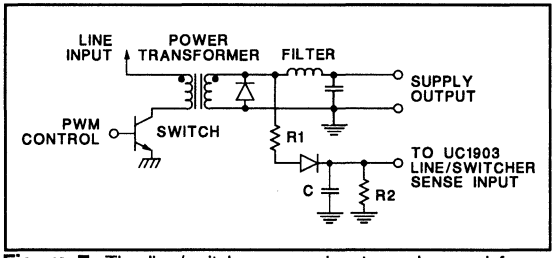


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2k resistor, R_1, and zener diode Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above -0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5k series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60μA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

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OPERATION AND APPLICATION INFORMATION (continued)

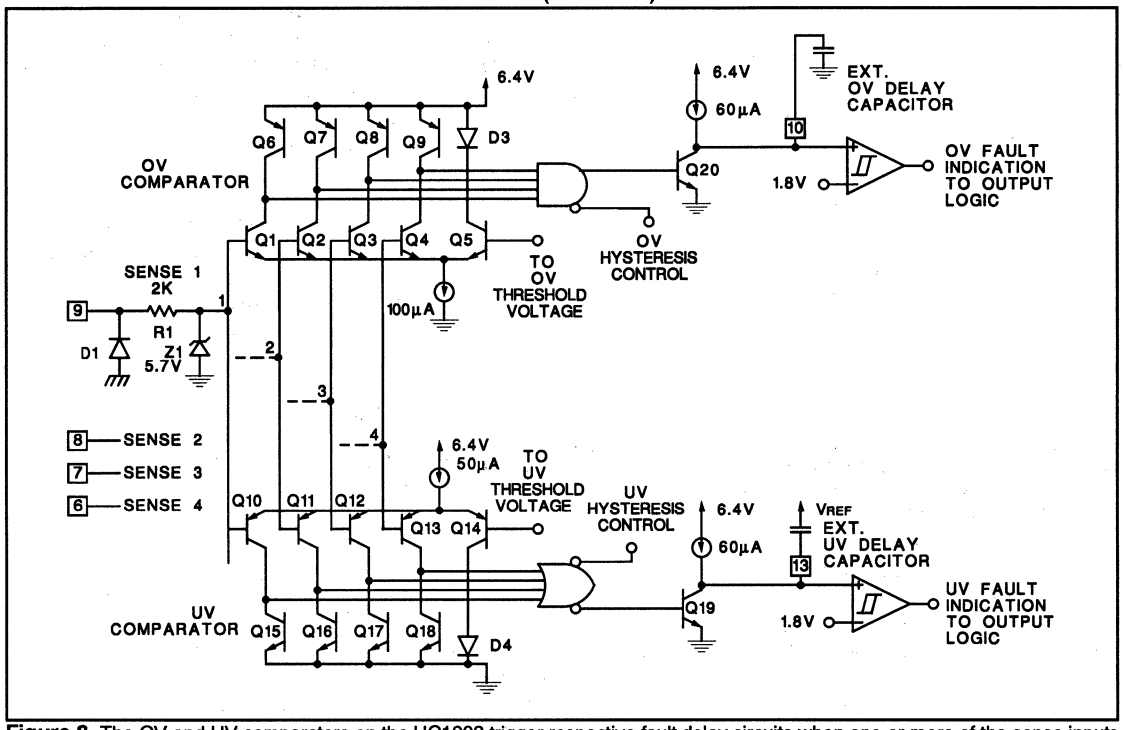

Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions. Terminating the UV delay capacitor to VREF assures correct logic at power up.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply (+VIN) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With +VIN below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

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UC1904
UC2904
UC3904

Precision Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring Up to Four Supply Voltages
- Two Inputs Preset for -5V and -12V Monitoring, or Programmable Positive Levels
- Precision 2.5V Reference
- Separate Inputs for Over-Current and Line Fault Sensing
- Adjustable Under- to Over-Voltage Fault Windows
- Latched Over-Voltage and Over-Current Output
- Power Good and Power Warning Outputs
- Auto Restart Function with ON/OFF Control, and Programmable Delay
- Programmable Pwr On Reset Delay

DESCRIPTION

The UC1904 Quad Supply Monitor will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. Four independent positive voltages can be monitored or, alternatively, two of the sense inputs are preset to monitor -5V and -12V supplies. The device also monitors Over-Current and Line Sense inputs, both with precision input thresholds.

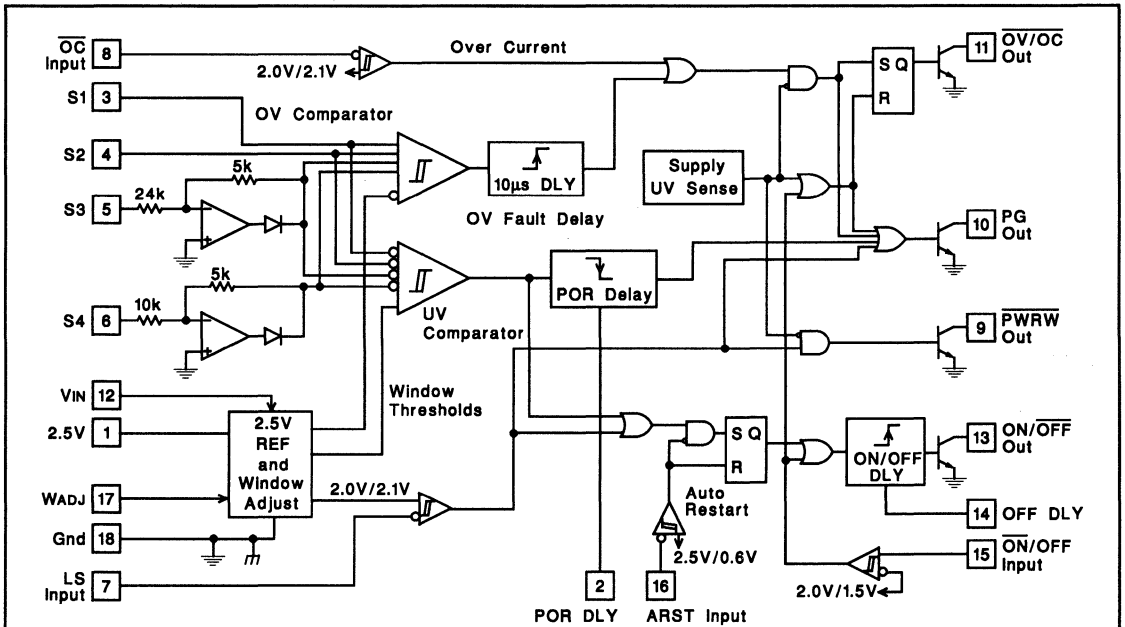
Four open collector outputs on the UC1904 give the following responses: 1. The $\overline{OV}/\overline{OC}$ output is a latched over-voltage, or over-current response. 2. A Power Good signal responds low with any fault detection – on power-up a programmable delay is used to hold this output low for a system Power On Reset signal. 3. The $\overline{PWRW}$ output responds only to a Line Sense input, for early warning of power failures. 4. The last open collector, the $ON/\overline{OFF}$ output, generates a delayed supply OFF control signal in response to an OFF input command, under-voltage condition, or line fault detection.

The OV-UV fault window is adjustable with a programming input. The thresholds are centered around the precision 2.5V reference, with a scaled hysteresis for precise, glitch free operation. In the positive mode of operation, the fault windows at each of the sense inputs can be independently scaled using external resistors and the 2.5V reference output. An Auto Restart function couples with the under-voltage and line sensing circuits to allow controlled power supply start-up and shutdown.

This device will operate over a supply range of 4.75V to 18V. The device is available in a DIP, SOIC, or PLCC outline. This device is ESD protected on all pins.

5

BLOCK DIAGRAM



Note: Pin Numbers refer to J, N, and DW Packages.

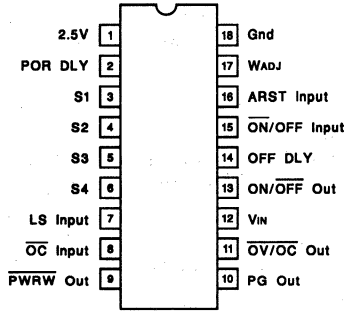
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage 20V
Sense Inputs, S1 And S2, Other Analog And Logic Inputs
  Maximum Forced Voltage ..... -0.3V to 10V
  Maximum Forced Current ..... ±10mA
Sense Input S3, (-12V Sense Input)
  Maximum Forced Voltage ..... -18V to 10V
  Maximum Forced Current ..... ±10mA
Sense Input S4, (-5V Sense Input)
  Maximum Forced Voltage ..... -10V to 10V
  Maximum Forced Current ..... ±10mA
Open Collector Outputs
  Maximum Voltage 20V
  Maximum Current 50mA
Reference Output Current ..... Internally Limited
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

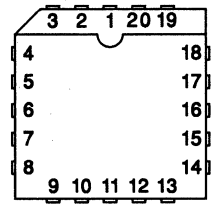
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N PACKAGE, DW PACKAGE



PLCC-20 (TOP VIEW)
Q PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
2.5V	1
POR DLY	2
N.C.	3
S1	4
S2	5
S3	6
S4	7
N.C.	8
LS Input	9
$\overline{OC}$ Input	10
$\overline{PWRW}$ Out	11
PG Out	12
$\overline{OV}/\overline{OC}$ Out	13
VIN	14
ON/$\overline{OFF}$ Out	15
OFF DLY	16
$\overline{ON}$/OFF Input	17
ARST Input	18
WADJ	19
Gnd	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +VIN = 15V, WADJ = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	VIN = 15V		3.2	4.5	mA
VIN UVLO Threshold	Low to High		4.5	4.75	V
UVLO Threshold Hysteresis			50		mV
Minimum VIN to Enable PG Out			0.8	1.5	V
Reference					
Output Voltage(VREF)	T_J = 25°C	2.475	2.5	2.525	V
	Over Temperature, UC3904	2.47		2.53	V
	Over Temperature, UC2904 & UC1904	2.465		2.535	V
Load Regulation	IOUT = 0 to 4mA			6	mV
Line Regulation	VIN = 4.75 to 18V			5	mV
Short Circuit Current	VREF = 0V		17		mA
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds					
Over-Voltage Thresholds S1, S2	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	140	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	270	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	540	mV
Over-Voltage Thresholds S3, S4 Positive Mode	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	145	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	280	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	550	mV

ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +V_{IN} = 15V, W_{ADJ} = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds (cont.)					
Under-Voltage Thresholds S1, S2	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-140	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-270	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-540	-500	-460	mV
Under-Voltage Thresholds S3, S4 Positive Mode	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-150	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-285	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-555	-500	-460	mV
OV and UV Threshold Hysteresis	As a Function of W_{ADJ}	30	50	70	mV/V
S3 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-13.52	-13.2	-12.88	V
	Under-Voltage, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-11.06	-10.8	-10.54	V
	Hysteresis, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	80	120	160	mV
S4 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-5.63	-5.5	-5.37	V
	Under-Voltage, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-4.61	-4.5	-4.39	V
	Hysteresis, W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	30	50	70	mV
W_{ADJ} Input Bias Current	0.25V < W_{ADJ} <1.0V	-5		5	µA/V
LS Threshold	Input = H to L	1.96	2	2.04	V
	Threshold hysteresis	65	100	125	mV
$\overline{OC}$ Threshold	Input = H to L	1.9	2	2.1	V
	Threshold hysteresis	50	100	150	mV
ARST Input Threshold	Input = L to H	2.25	2.5	2.75	V
	Input = H to L	0.56	0.625	0.69	V
$\overline{ON}$/OFF Input Threshold	Input high level		1.74	2.4	V
	Input low level	0.6	1.35		V
Sense and Logic Input Bias Currents					
Sense 1-4, Positive Mode	Input = 2.8V		250	800	nA
	Input = 2.2V	-1000	-250		nA
Sense 3 Negative Mode	Input = -12V	-700	-500	-300	µA
Sense 4 Negative Mode	Input = -5V	-700	-500	-300	µA
Line, and OC Inputs	Input = 2.2V		300	1000	nA
$\overline{ON}$/OFF Input	Input = 2.5V		150	600	nA
ARST Input	Input = 0.5	-2000	-700		nA
Open Collector Outputs ($\overline{OV}$/$\overline{OC}$ Out, PG Out, $\overline{PWRW}$ Out, ON/$\overline{OFF}$ Out)					
Saturation Voltage	I_{OUT} = 10mA		0.2	0.4	V
Leakage current	V_{OUT} = 20V			5	µA
POR Delay					
Delay		160	250	350	ms/µF
Internal Pullup Current			9		µA
Threshold Low to High			2.25		V
OFF Delay					
Delay		120	185	250	ms/µF
Internal Pullup current			12		µA
Threshold Low to High			2.25		V
OV Fault Delay					
Delay		10	20	50	µs

PIN FUNCTIONAL DESCRIPTION

2.5V: This is the output of the precision 2.5V reference.

ARST Input: This input, with a 4:1 hysteretic threshold, is used to sequence a power system through the **A**uto **R**e**S**tar**T** cycle. A delayed representation of a supply output voltage is used at this pin to provide adequate startup time for the power system, and a minimum power-off period.

Gnd: Reference point for the internal reference and all thresholds, as well as the return for the remainder of the device.

LS Input: The **L**ine **S**ense input is used to monitor a voltage that varies with the input line voltage to a system. The input is compared to a precision 2.0V level and is used to activate the $\overline{\text{PWRW}}$ and PG outputs, as well as triggering the Auto Restart sequence.

$\overline{\text{OC}}$ Input: The **O**ver-**C**urrent input can be used to respond to an inverted over-current signal. A low level signal at this input latches in a fault indication at the **$\overline{\text{OV}}$/$\overline{\text{OC}}$** output.

OFF DLY: This pin functions similarly to the POR DLY pin to delay the turn-on of the ON/$\overline{\text{OFF}}$ output transistor. The charging current and upper threshold are 12μA and 2.1V.

$\overline{\text{ON}}$/$\overline{\text{OFF}}$ Input: With a high level at this input the **ON/$\overline{\text{OFF}}$ Out** pin is activated after a user-programmable delay. A high level also activates the **PG Out** pin, and resets the **OV/OC** fault latch.

On/$\overline{\text{Off}}$ Out: This output is an open collector output that is activated by the **$\overline{\text{ON}}$/OFF Input**, or the Auto Restart circuitry. Saturation voltage on this and all the open collector outputs is rated at 10mA of current.

$\overline{\text{OV}}$/$\overline{\text{OC}}$ Out: In response to either an **O**ver-**V**oltage or **O**ver-**C**urrent situation this output is latched active low. There is nominal 20μs delay in the OV path to the fault latch, providing rejection to transient overshooting on the monitored voltages. The low condition is cleared when the fault latch is reset by the **$\overline{\text{ON}}$/OFF Input**, or a **UVLO** condition on the device.

POR DLY: This pin is used, with an external capacitor, to program a **P**ower-**O**n-**R**eset delay. This delay is reset whenever there is a UV condition at one of the S1-S4 inputs, and then triggered upon the clearing of the UV condition. When reset the voltage across the capacitor is quickly discharged to near zero volts, and the **PG Out** pin goes active low. Once triggered the capacitor is charged by a 9μA current source. The **PG Out** pin remains active low until the delay capacitor voltage reaches a 2.1V threshold.

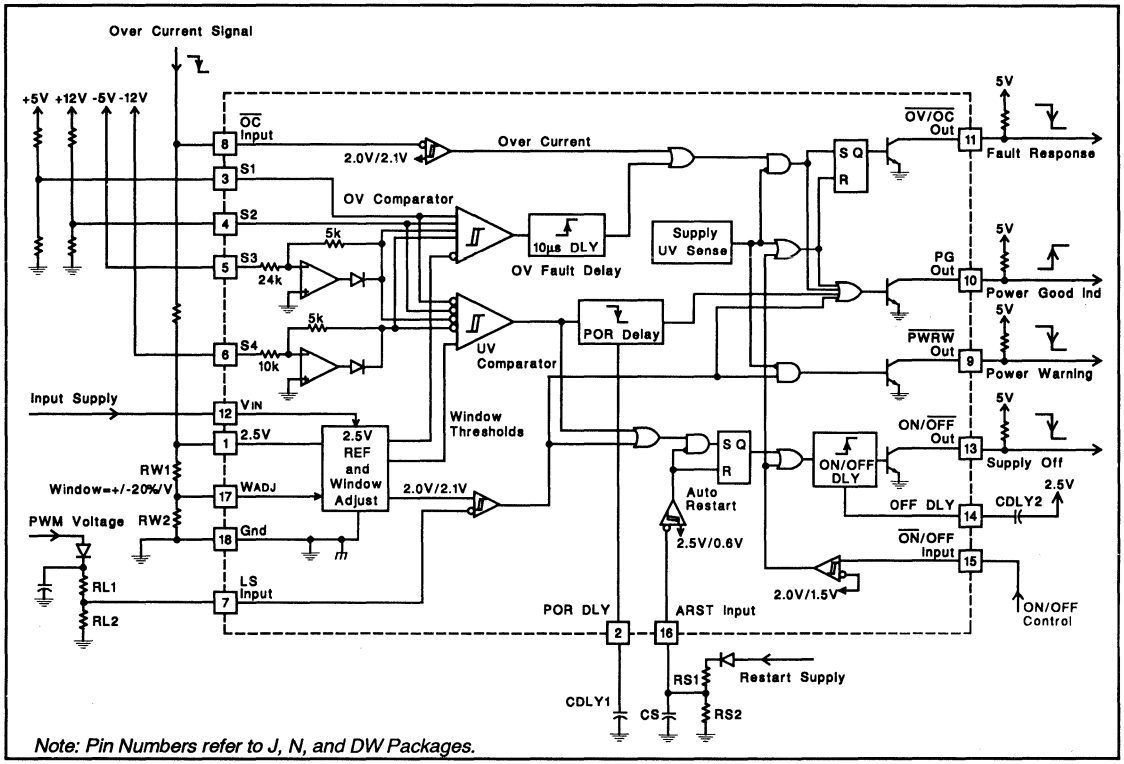
PG Out: During any fault, under-voltage, or UVLO condition this output is low. A **P**ower **G**ood indication (output off) is given when all supply conditions are within defined operating limits. During power-up the **PG** signal is delayed by a programmable **P**ower **O**n **R**eset delay. During **UVLO** the output is active low as long as the input supply, **VIN**, is above approximately 1.0V.

$\overline{\text{PWRW}}$ Out: When a low line condition is sensed by the LS Input this output goes low. This output is disabled (off) during a **UVLO** condition.

S1-S4: These are the sense inputs for OV and UV monitoring of external voltages. All four inputs can be used to sense positive voltages with a simple divider to scale the voltage level to the 2.5V centered window. The **S3** and **S4** inputs can also be used to sense -12V and -5V supplies respectively with no external components. This is done with internal precision resistor dividers and two source only op-amps that are disabled when the pins are used in the positive mode.

VIN: Input supply for the UC1904. The device is operational with 4.75V to 18V on this pin.

WADJ: The **WADJ** input is used to program the OV and UV window thresholds. The OV-UV window is centered around the 2.5V reference and is nominally ±20% per volt on the **WADJ** input pin.



Note: Pin Numbers refer to J, N, and DW Packages.

5

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INTEGRATED CIRCUITS
UNITRODE

UC1907
UC2907
UC3907

Load Share Controller

FEATURES

- Fully differential high impedance voltage sensing.
- Accurate current amplifier for precise current sharing.
- Opto coupler driving capability.
- 1.25% trimmed reference
- Master status indication
- Compatible with JIAWG 88-M7A specification
- 4.5V TO 35V operation.

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage .....+35V
Opto Out Voltage.....+35V
Opto Out Current.....+20mA
Status Indicate Sink Current.....+20mA
C/S Input Voltage .....+35V
Share Bus Voltage .....–0.3V to +35V
Other Analog Inputs and Outputs (Zener clamped)
Maximum Forced Voltage –0.3V to +10V
Maximum Forced Current.....±10mA
Ground Amp Sink Current.....+50mA
Pins 1, 9, 12, 15 Sink Current .....+20mA
Power Dissipation at T_A=25°C (Note 2)...1000mW
Power Dissipation at T_C=25°C (Note 2) ..2000mW
Storage Temperature Range .– 65°C to +150°C
Lead Temperature (Solder 10 Seconds)+300°C

NOTE 1: Pin Nos. refer to 16 Pin DIL Package
NOTE 2: Consult packaging section of databook for thermal limitations and considerations of package.

DESCRIPTION

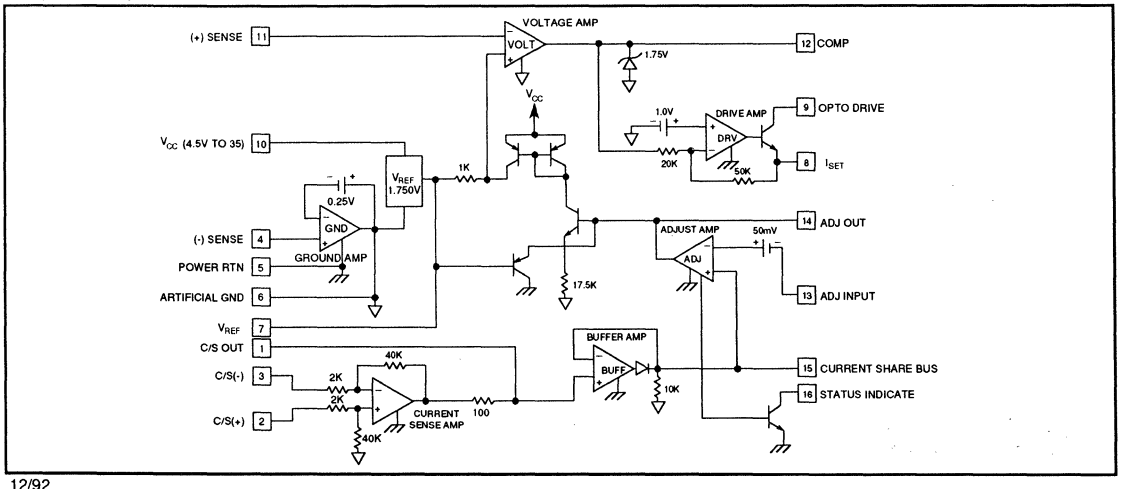
The UC3907 family of Load Share Controller IC's provides all the necessary features to allow multiple independent power modules to be paralleled such that each module supplies only its proportionate share to total load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage feedback amplifier whose reference can be independently adjusted in response to a common share bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the master, adjusts all the other modules to increase their output current to within 2.5% of that of the master.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an opto coupler or other isolated medium. The load sharing technique implemented with the UC3907 is compatible with the requirements of JIAWG 88-M7A specifications.

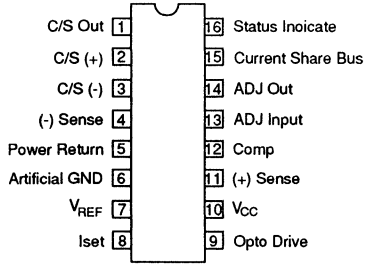
Other features of the UC3907 include 1.25% accurate reference: a low-loss, fixed gain current sense amplifier, a fully differential, high-impedance voltage sensing capability, and a status indicator to designate which module is performing as master.

BLOCK DIAGRAM

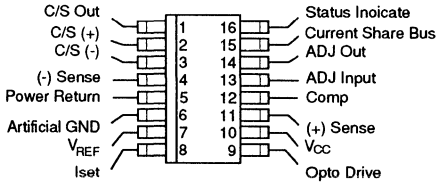


CONNECTION DIAGRAMS

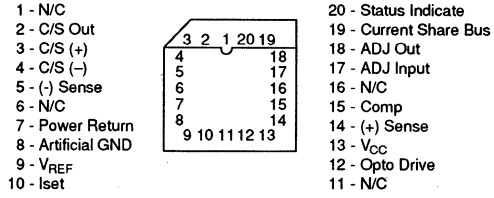
DIL-16 (TOP VIEW)
J or N PACKAGE



SOIC-16 (TOP VIEW)
DW PACKAGE



PLCC–20 Q PACKAGE (TOP VIEW)
LCC–20 L PACKAGE



Electrical Characteristics: Unless otherwise stated these specifications apply for $T_A = -55°C$ to $+125°C$ for UC1907; $-40°C$ to $+85°C$ for UC2907; and $0°C$ to $+70°C$ for UC3907; VIN = 15V, $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
VOLTAGE AMP SECTION					
Input Voltage	V/A out = 1V, $T_A = 25°C$	1.975	2.000	2.025	V
	V/A out = 1V, Over Temp	1.960	2.000	2.040	V
Line Regulation	Vin = 4.5V to 35V			15	mV
Load Regulation	I_L Reference = 0.0mA to – 10mA			10	mV
Long Term Stability	$T_A = 125°C$, 1000hrs (Note 2)		5	25	mV
Total Output Variation	Line, Load, Temp	1.960		2.040	
Input Adjust Range	A/A from max high to max low	85	100	115	mV
Input Bias Current		–1			uA
Open Loop Gain	V/A out = 0.75V to 1.5V	65			dB
Unity Gain Bandwidth	$T_A = 25°C$ (Note 2)	700			kHz
Output Sink Current	(+) Sense = 2.2V, V/A out = 1V	6	15		mA
Output Source Current	(+) Sense = 1.8V, V/A out = 1V	400	600		uA
Vout High	(+) Sense = 2.2V $I_L = -400ua$	1.85	2		V
Vout Low	(+) Sense = 1.8V $I_L = +1mA$		.15	.40	V
REFERENCE SECTION					
Output Voltage	$T_A = 25°C$	1.970	2.000	2.030	V
	Over Operating Temp	1.955	2.000	2.045	V
Short Circuit Current	$V_{REF} = 0.0V$	– 15	– 30	– 60	mA
GROUND AMP SECTION					
Output Voltage		200	250	300	mV
Common Mode Variation	(–) Sense from 0.0V to 2V			5	mV
Load Regulation	I_L = 0.0mA to 20mA, $T_A = 25°C$			10	mV
	I_L = 0.0mA to 20mA, Over Temp			15	mV

NOTE 1: Unless otherwise specified all voltages are with respect to (–) sense. Currents are positive into, negative out of the specified terminal.
NOTE 2: These parameters, although quaranteed over their recommended operating conditions are not 100% tested in production.

Electrical Characteristics: Unless otherwise stated these specifications apply for T_A = – 55°C to +125°C for UC1907; – 40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; VIN = 15V, T_A=T_J

PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNITS
ADJUST AMP SECTION						
Input Offset Voltage	A/A out = 1.5V, Vcm = 0.0V		40	50	60	mV
Input Bias Current			– 2			uA
Open Loop Gain	1.5V ≤ A/A out ≤ 2.25V		65			dB
Unity Gain Bandwidth	T_A = 25°C, Cout =1uF (Note 2)			500		Hz
Transconductance	Iout = – 10uA to +10uA, Vout = 1.5V		1.7	3	4.5	ms
Output Sink Current	Vid = 0.0V, A/A out = 1.5V		55	135	225	uA
Output Source Current	Vid = 250mV, A/A out = 1.5V		110	200	350	uA
Vout High	Vid = 250mV, Iout = – 50uA		2.20	2.70	2.90	V
Vout Low	Vid = 0.0V, Iout = 50uA		0.75		1.15	V
Common Mode Rejection Ratio	Vcm = 0.0 to 10V		70			dB
Output gain to V/A	Vout A/A = 1.5V to 2V		50	57	64	mV/V
	Δ (+) Sense/ ΔA/A out					
CURRENT AMP SECTION						
Gain	Vcm = 0.0V, Vid = 50mV to 100mV		19.2	19.6	20.1	V/V
Output Voltage	$V_{C/A}$ (+) = $V_{C/A}$ (-) = 0.0V	T_A = 25°C	210	250	290	mV
		Over Temp	180	250	330	mV
Input Offset Change with Common Mode Input					600	µV/V
Vout High	Vid = 1V		10	14.5		V
Vout Low	Vid = – 1V I_L = 1mA			350	450	mV
Power Supply Rejection Ratio	Vin = 4.5V to 35V, Vcm = 0.0V		60			dB
Slew Rate				0.4		V/us
DRIVE AMP SECTION Rset = 500 ohms to Artificial Gnd, Opto Drive = 15V						
Voltage Gain	V/A out = 0.5V to 1V		2.3	2.5	2.6	V/V
Iset Vout High	(+) sense = 2.2V		3.8	4.1	4.4	V
Iset Vout Low	(+) sense = 1.8V			270	300	mV
Opto out Voltage Range			4		35	V
Zero Current Input Threshold			1.55	1.65	1.75	V
BUFFER AMP SECTION						
Input Offset Voltage	Input = 1V				5	mV
Output Off Impedance	Input = 1V, Output = 1.5V to 2V		5	10	20	kΩ
Output Source Current	Input = 1V, Output = 0.5V		6	15		mA
Common Mode Rejection Ratio	Vcm = 0.3Vto 10V		70			dB
Power Supply Rejection Ratio	Vin = 4.5V to 35V		70			dB
UNDER VOLTAGE LOCKOUT SECTION						
Start-up Threshold				3.7	4.4	V
Threshold Hystesis				200		mV

NOTE 1: Unless otherwise specified all voltages are with respect to (–) sense. Currents are positive into, negative out of the specified terminal.
NOTE 2: These parameters, although guaranteed over their recommended operating conditions are not 100% tested in production.

STATUS INDICATE SECTION					
Vout Low	A/A– = Current Share Bus		0.2	0.5	V
Output Leakage	A/A out = 1V Vout = 35V		0.1	5	uA
TOTAL STAND BY CURRENT					
Start-Up Current	Vin = UVLO – 0.2V		3	5	mA
Operating Current	Vin = 35V		6	10	mA

NOTE 1: Unless otherwise specified all voltages are with respect to (–) sense. Currents are positive into, negative out of the specified terminal.
NOTE 2: These parameters, although guaranteed over their recommended operating conditions are not 100% tested in production.

PIN/BLOCK DESCRIPTIONS
(Pin Nos are for DIL-16 package)

NEGATIVE SENSE (Pin 4) - This is a high-impedance pin intended to allow remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. **This point should be considered as the "true" ground. Unless otherwise stated, all voltages are with respect to this point.**

ARTIFICIAL GROUND (Pin 6) - This is a low impedance circuit ground which is exactly 250 millivolts above the (–) Sense terminal. This offset allows the Ground Buffer Amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (–) Sense input.

POWER RETURN (Pin 5) - This should be the most negative voltage available and can range from zero to 5V below the (–) Sense terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current sensing impedances lie between this terminal and the (–) Sense point.

VREF (Pin 7) - The internal Voltage Reference is a band-gap circuit set at 2.0 Volts with respect to the (–) Sense input (1.75V above the Artificial Ground), and an accuracy of + / – 1.5%. This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5V to 35V allowing operation from unregulated DC, an auxiliary voltage, or the same output voltage that it is controlling. Under voltage lockout has been included to insure proper start-up by disabling internal bias currents until the reference rises into regulation.

VOLTAGE AMPLIFIER (Pins 11, 12) - This circuit is the feedback control gain stage for the power module's output voltage regulation, and overall loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal clamp of 2.0 Volts. The reference trimming is performed closed loop, and measured at pin 11, (+) sense. The value is trimmed to 2V ±1.25%.

DRIVE AMPLIFIER (Pins 8, 9, 12) - This amplifier is used as an inverting buffer between the Voltage Amplifier's output and the medium used to couple the feedback signal to the power controller. It has a fixed voltage gain of 2.5 and is usually configured with a current-setting resistor to ground. This establishes a current - sinking output optimized to drive optical couplers biased at any voltage from 4.5V to 35V, with current levels up to 20mA. The polarity of this stage is such that an increasing voltage at the Voltage Amplifier's sense input (as, for example, at turn on) will increase the opto's current. In a nonisolated application, a voltage signal ranging from 0.25V to 4.1V may be taken from the current-setting output but it should be noted that this voltage will also increase with increasing sense voltage and an external inverter may be required to obtain the correct feedback polarity.

CURRENT AMPLIFIER (Pins 1, 2, 3) - This amplifier has differential sensing capability for use with an external shunt in the power return line. The common-mode range of its input will accommodate the full range between the Power Return point and Vcc–2V which will allow undefined line impedances on either side of the current shunt. The gain is internally set at 20 giving the user the ability to establish the maximum voltage drop across the current sense resistor at any value between 50 and 500 millivolts. While the bandwidth of this amplifier may be reduced with the addition of an external output capacitor to ground, in most cases this is not required as the compensation of the Adjust Amplifier will typically form the dominant pole in the adjust loop.

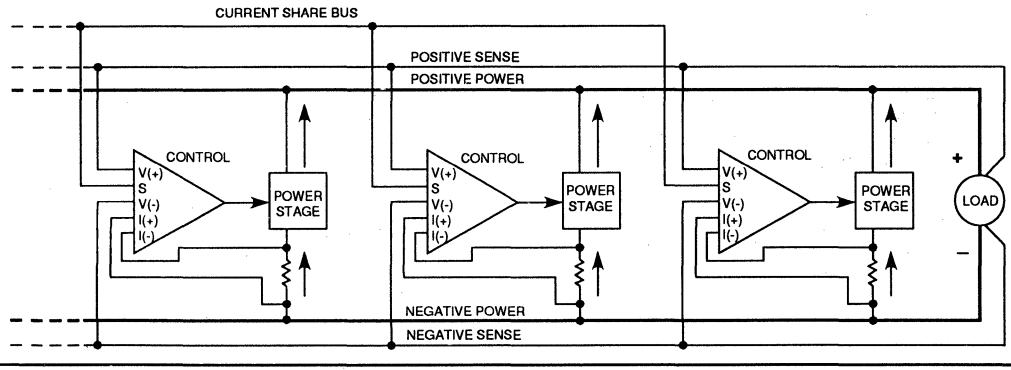
BUFFER AMPLIFIER (Pins 1, 15) - This amplifier is a unidirectional buffer which drives the Current Share Bus - the line which will interconnect all power modules paralleled for current sharing. Since the Buffer Amplifier will only source current, it insures that the module with the highest output current will be the master and drive the bus with a low-impedance drive capability. All other Buffer Amplifiers will be inactive with each exhibiting a 10 kohm load impedance to ground. The Share Bus terminal is protected against both shorts to ground and accidental voltages in excess of 50 Volts.

ADJUST AMPLIFIER (Pins 13, 14, 15) - This amplifier adjusts the individual module's reference voltage to maintain equal current sharing. It is a transconductance type in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to ground. The function of this amplifier is to compare its own module output current to the Share Bus signal - which represents the highest output current - and force an adjust command which is capable of increasing the reference voltage as seen by the voltage amplifier by as much as 100 millivolts. This number stems from the

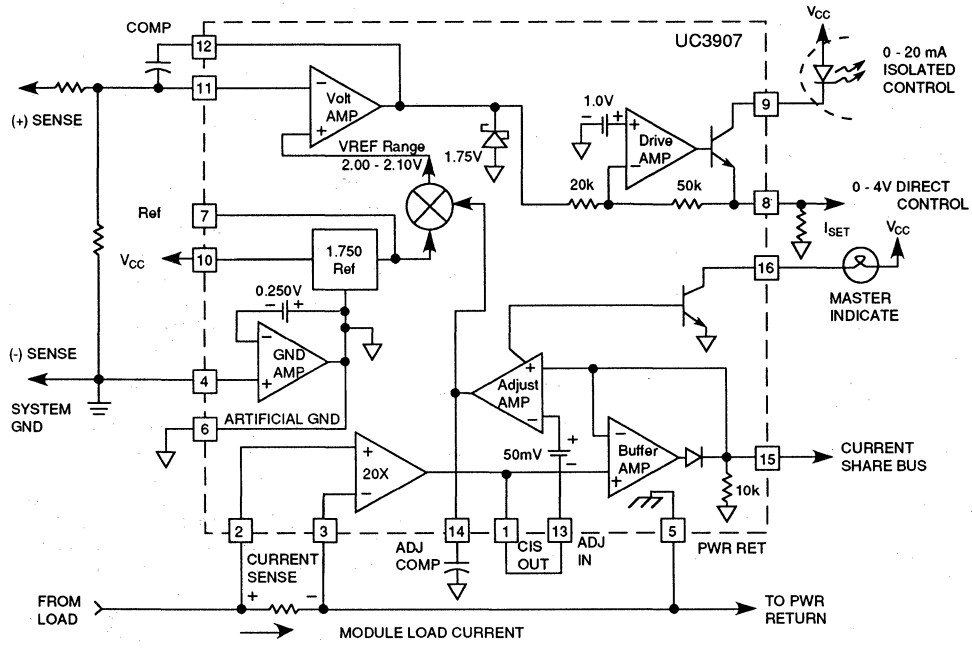
17.5:1 internal resistor ratio between the Adjust Amplifier's clamped output and the reference, and represents a 5% total range of adjustment - a value which should be adequate to compensate for unit-to -unit reference and external resistor tolerances. The Adjust Amplifier has a built-in 50 mV offset on its inverting input which will force the unit acting as the master to have a low output resulting in no change to the reference. While this 50 mV offset represents and error in current sharing, the gain of the current amplifier reduces it to only 2.5 mV across the current sense resistor. It should also be noted that when the module is acting independently with no connection to the Share Bus node, or when the Share Bus node is shorted to ground, its reference voltage will be unchanged. Since only the circuit acting as a master will have a low output from the Adjust Amplifier, this signal is used to activate a flag output to identify the master should some corrective action be needed.

STATUS INDICATE (Pin 16) - This pin is an open collector output intended to indicate the unit which is acting as the master. It achieves this by sensing when the adjust amp is in its low state and pulling the status indicate pin low.

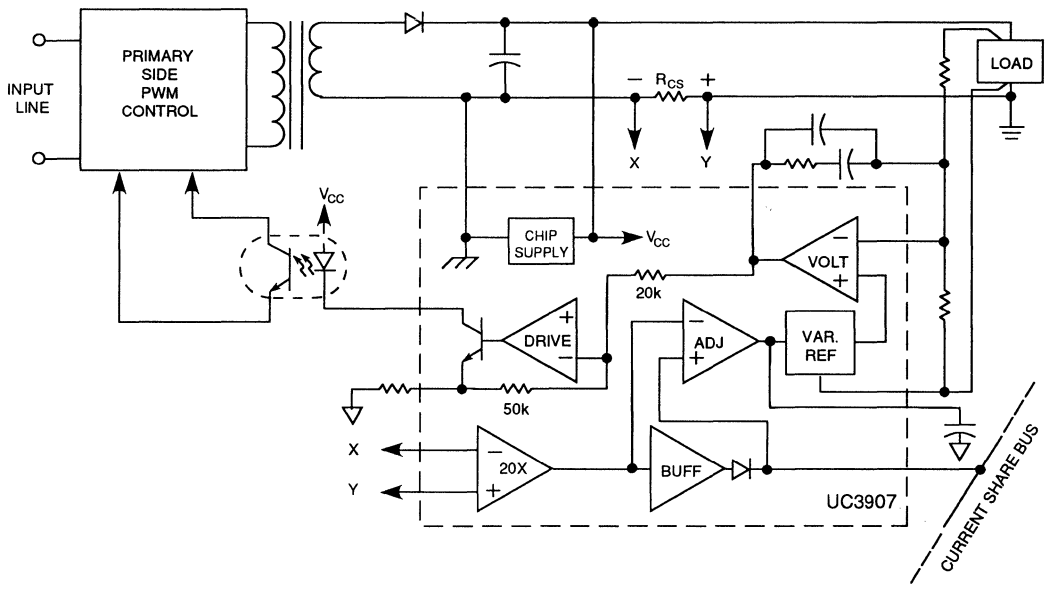
LOAD SYSTEM DIAGRAM



LOAD SHARE CONNECTION DIAGRAM



UC3907 IN A LOAD-SHARING FEEDBACK LOOP FOR AN OFF-LINE ISOLATED SUPPLY



5

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INTEGRATED CIRCUITS
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UC2906
UC3906

Sealed Lead-Acid Battery Charger

FEATURES

- Optimum Control for Maximum Battery Capacity and Life
- Internal State Logic Provides Three Charge States
- Precision Reference Tracks Battery Requirements Over Temperature
- Controls Both Voltage and Current at Charger Output
- System Interface Functions
- Typical Standby Supply Current of only 1.6mA

DESCRIPTION

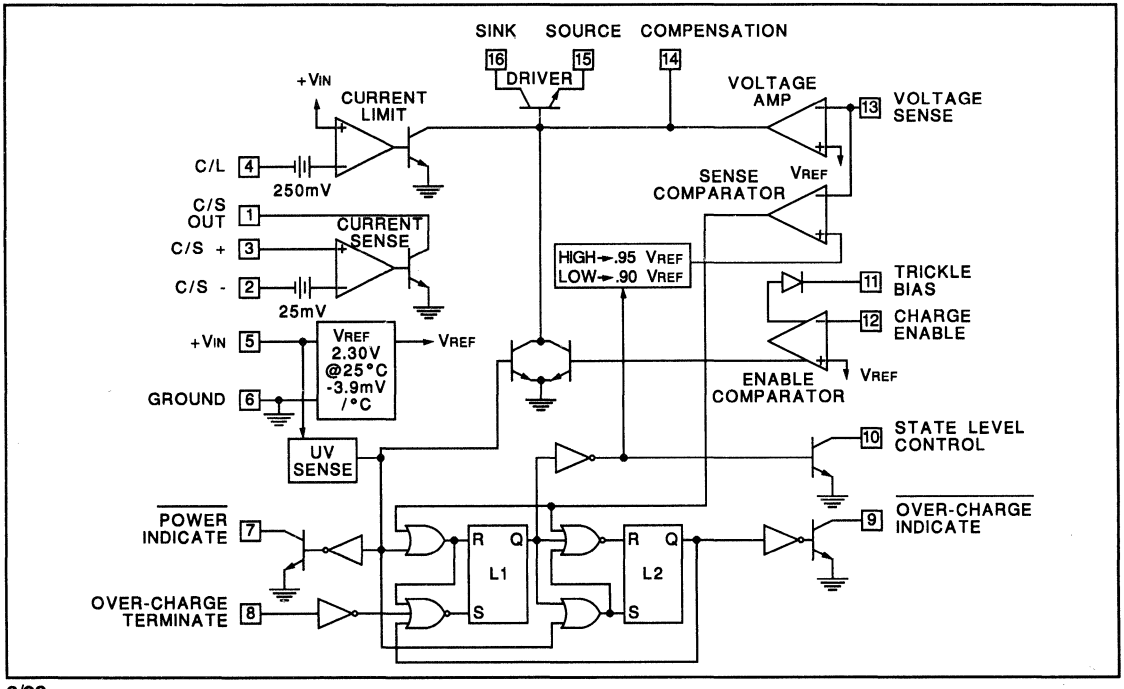
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply up to 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

BLOCK DIAGRAM



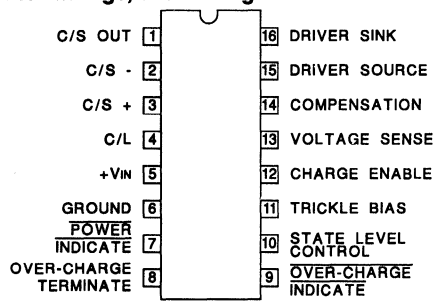
6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+VIN) 40V
Open Collector Output Voltages 40V
Amplifier and Comparator Input Voltages ... -0.3V to +40V
Over-Charge Terminate Input Voltage ..... -0.3V to +40V
Current Sense Amplifier Output Current 40mA
Other Open Collector Output Currents 5mA
Trickle Bias Output Current ..... -40mA
Driver Current 40mA
Power Dissipation at TA = 25°C(Note 2) 1000mW
Power Dissipation at Tc = 25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

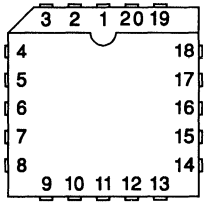
Note 1: Voltages are referenced to ground (Pin 6). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of packages.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/S OUT	2
C/S-	3
C/S+	4
C/L	5
N/C	6
+VIN	7
GROUND	8
POWER INDICATE	9
OVER CHARGE TERMINATE	10
N/C	11
OVER CHARGE INDICATE	12
STATE LEVEL CONTROL	13
TRICKLE BIAS	14
CHARGE ENABLE	15
N/C	16
VOLTAGE SENSE	17
COMPENSATION	18
DRIVER SOURCE	19
DRIVER SINK	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TA = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, +VIN = 10V, TA = TJ.

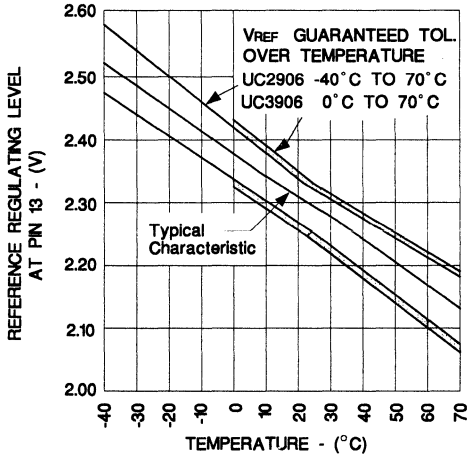
PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Supply								
Supply Current	+VIN = 10V		1.6	2.5		1.6	2.5	mA
	+VIN = 40V		1.8	2.7		1.8	2.7	mA
Supply Under-Voltage Threshold	+VIN = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			0.20	0.30		0.20	0.30	V
Internal Reference (VREF)								
Voltage Level (Note 2)	Measured as Regulating Level at Pin 13 w/ Driver Current = 1mA, TJ = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	+VIN = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			-3.9			-3.9		mV/°C
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	-0.5	-0.2		-0.5	-0.2		µA
Maximum Output Current	Source	-45	-30	-15	-45	-30	-15	µA
	Sink	30	60	90	30	60	90	µA
Open Loop Gain	Driver current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts above GND or below +VIN		0.2			0.2		V

Note 2. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, Io = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage			0.2	0.45		0.2	0.45	V
Current Limit Amplifier								
Input Bias Current			0.2	1.0		0.2	1.0	µA
Threshold Voltage	Offset below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.03	0.25		0.03	0.25	%/V
Voltage Sense Comparator								
Threshold Voltage	As a function of V_{REF}, L_1 = RESET	0.945	0.95	0.955	0.945	0.95	0.955	V/V
	As a function of V_{REF}, L_1 = SET	0.895	0.90	0.905	0.895	0.90	0.905	V/V
Input Bias Current	Total Input Bias at Thresholds	-0.5	-0.2		-0.5	-0.2		µA
Current Sense Comparator								
Input Bias Current			0.1	0.5		0.1	0.5	µA
Input Offset Current			0.01	0.2		0.01	0.2	µA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA	20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.05	0.35		0.05	0.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$		0.05	0.35		0.05	0.35	%/V
Maximum Output Current	V_{OUT} = 2V	25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA		0.2	0.45		0.2	0.45	V
Enable Comparator								
Threshold Voltage	As a function of V_{REF}	0.99	1.0	1.01	0.99	1.0	1.01	V/V
Input Bias Current		-0.5	-0.2		-0.5	-0.2		µA
Trickle Bias Maximum Output Current	$V_{OUT} = +V_{IN} - 3V$	25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts below $+V_{IN}$, I_{OUT} = 10mA		2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = -10µA	6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input								
Threshold Voltage		0.7	1.0	1.3	0.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold		10			10		µA
Open Collector Outputs (Pins 7, 9, and 10)								
Maximum Output Current	V_{OUT} = 2V	2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA		0.25	0.45		0.25	0.45	V
	I_{OUT} = 50µA		0.03	0.05		0.03	0.05	V
Leakage Current	V_{OUT} = 40V		1	3		1	3	µA

Internal Reference Temperature Characteristic and Tolerance



OPERATION AND APPLICATION INFORMATION

Dual Level Float Charger Operations

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn on mode. The output current of the charger is limited to a low-level until the battery reaches a specified voltage, preventing a high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor Rs.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, Voc, during state 1 and state 2. When the battery voltage reaches 95% of Voc, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, IOCT. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the $\overline{\text{OVER-CHARGE INDICATE}}$ signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual lever float charger is shown in Figure 3.

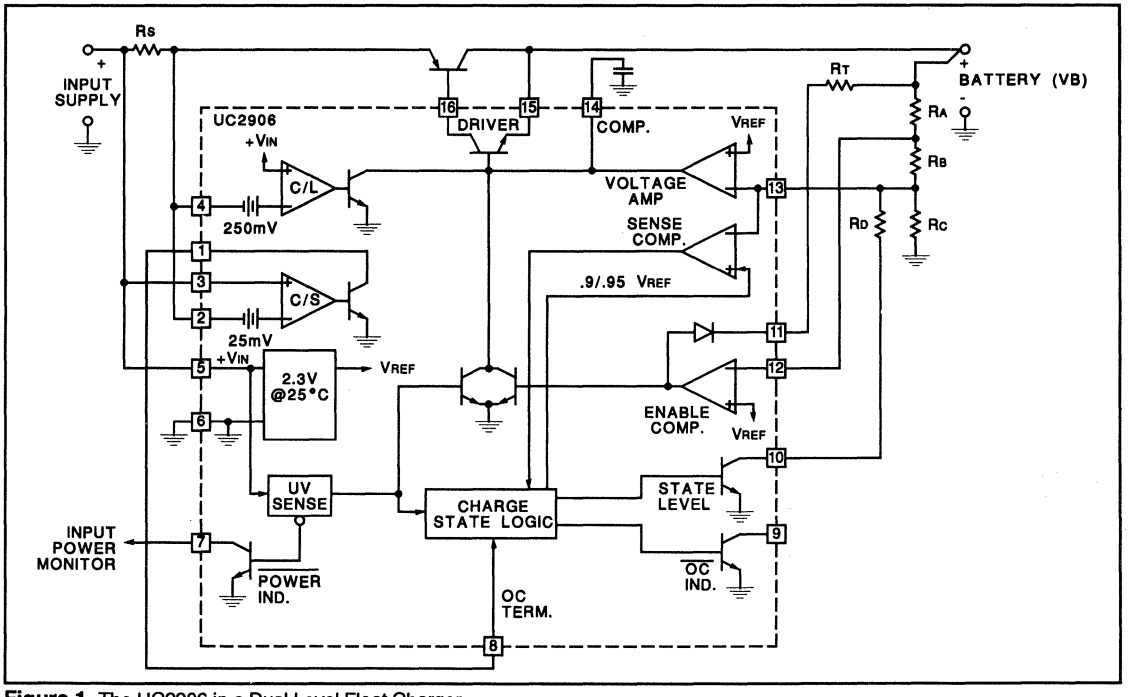
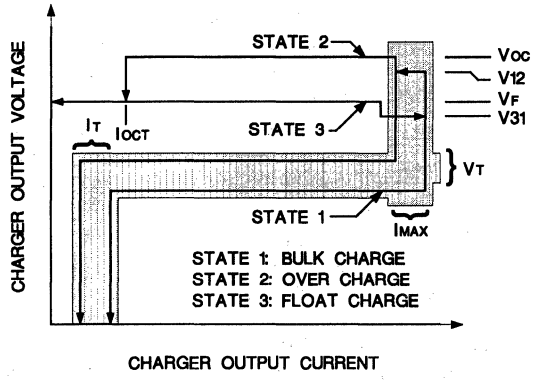


Figure 1. The UC2906 in a Dual Level Float Charger

OPERATION AND APPLICATION INFORMATION (continued)



Design procedure

1.) Pick divider current, I_D. Recommended value is 50μA to 100μA.

2.) $R_C = 2.3V/I_D$

3.) $R_A + R_B = R_{SUM} = (V_F - 2.3V)/I_D$

4.) $R_D = 2.3VR_{SUM}/(V_{OC} - V_F)$

5.) $R_A = (R_{SUM} + R_X)(1 - 2.3V/V_T)$
where: $R_X = R_CR_D/(R_C + R_D)$

6.) $R_B = R_{SUM} - R_A$

7.) $R_S = 0.25V/I_{MAX}$

8.) $R_T = (V_{IN} - V_T - 2.5V)/I_T$

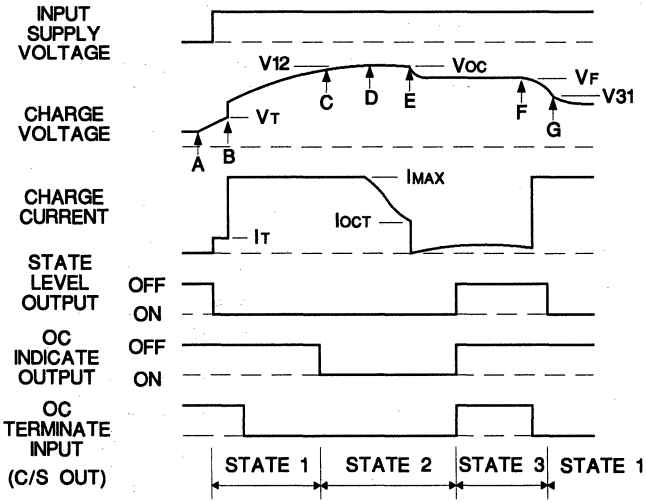
Note: $V_{12} = 0.95V_{OC}$

$V_{31} = 0.90V_F$

$I_{OCT} = \frac{I_{MAX}}{10}$

For further design and application information see UICC Application Note U-104

Figure 2. State Diagram and Design Equations for the Dual Level Float Charger



Explanation: Dual Level Float Charger

A. Input power turns on, battery charges at trickle current rate.

B. Battery voltage reaches VT enabling the driver and turning off the trickle bias output, battery charges at IMAX rate.

C. Transition voltage V12 is reached and the charger indicates that it is now in the over-charge state, state 2.

D. Battery voltage approaches the over-charge level VOC and the charge current begins to taper.

E. Charge current tapers to IOCT. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at VF.

F. Here a load (IMAX) begins to discharge the battery.

G. The load discharges the battery such that the battery voltage falls below V31. The charger is now in state 1, again.

Figure 3. Typical Charge Cycle: UC2906 Dual Level Float Charger

OPERATION AND APPLICATION INFORMATION (continued)

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, V_F. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum-charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, 1_H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V_{12} is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the $\overline{\text{POWER INDICATE}}$ pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

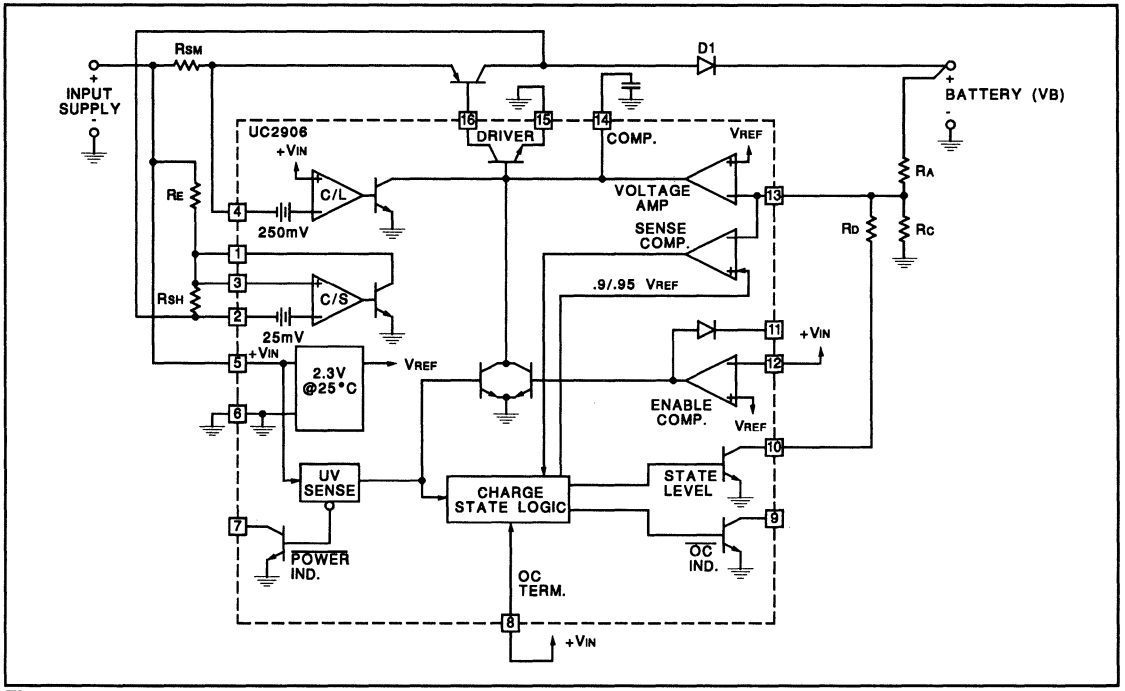


Figure 4. The UC2906 in a Dual Step Current Charger

OPERATION AND APPLICATION INFORMATION (continued)

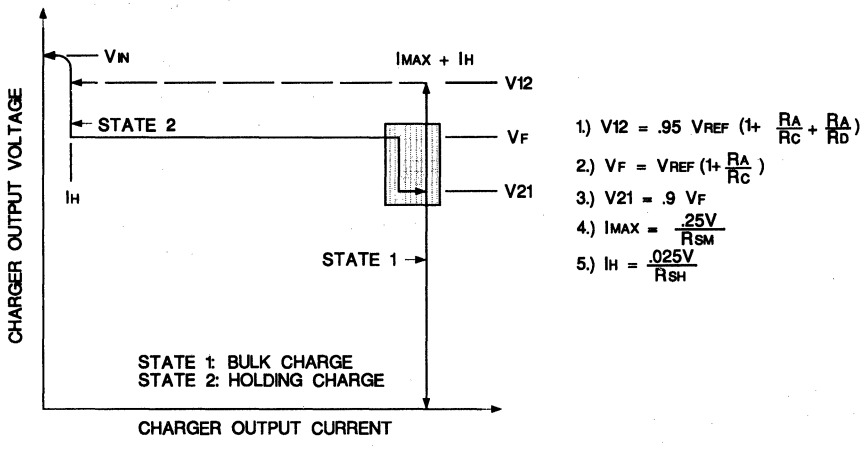
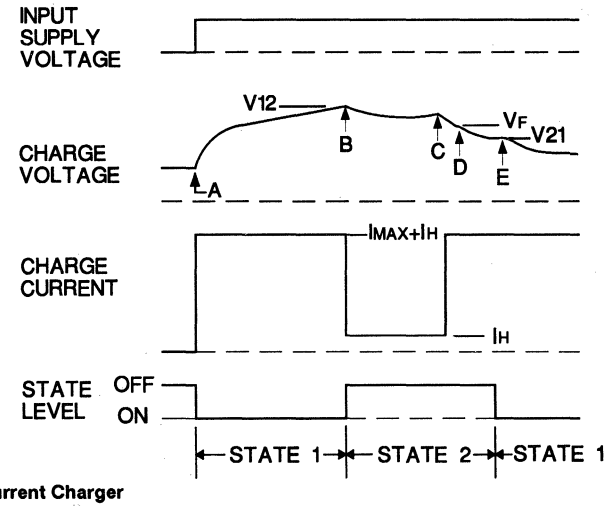


Figure 5. State Diagram and Design Equations for the Dual Step Current Charger



Explanation: Dual Step Current Charger

A. Input power turns on, battery charges at a rate of IH + IMAX.

B. Battery voltage reaches V12 and the voltage loop switches to the lower level VF. The battery is now fed with the holding current IH.

C. An external load starts to discharge the battery.

D. When VF is reached the charger will supply the full current IMAX + IH.

E. The discharge continues and the battery voltage reaches V21 causing the charger to switch back to state 1.

Figure 6. Typical Charge Cycle: UC2906 Dual Step Current Charger

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UC7501/7503
ADVANCED INFORMATION

Primary Side Controller

FEATURES

- Optimized for Offline Operation
- Toggle Option for 45% (UC7501)
- 90% Duty Cycle Limit (UC7503)
- Over-Current Protection via Frequency Reduction
- Low Standby Current for Current-Feed Startup
- Current-Mode or Voltage-Mode Control
- Built-in User-Adjustable Slope Compensation
- Functionally Integrated & Simplified 5-Pin Design
- Miniature Surface Mount U-PAK-5 (1 Watt) Package

DESCRIPTION

The UC7501/7503 is a primary side controller for switching mode power supplies. It is suitable for both voltage-mode and current-mode control and has advanced features not available in controllers with an even higher pin count. The key to full functionality in a 5-pin package is that the current signal and the error signal are added together and fed into the feedback pin. A sawtooth current flowing out of the feedback pin provides slope compensation, in proportion to the resistance terminating that pin. If the sum of the current signal and error signal exceeds the Over Current Detector threshold, indicating that the Current Control Detector loses control of the switch current, the charging current of the timing capacitor will be reduced to 25% for the remainder of the period. The reduced charge current leads up to a four-fold reduction in switching frequency, effectively preventing short-circuit current runaway.

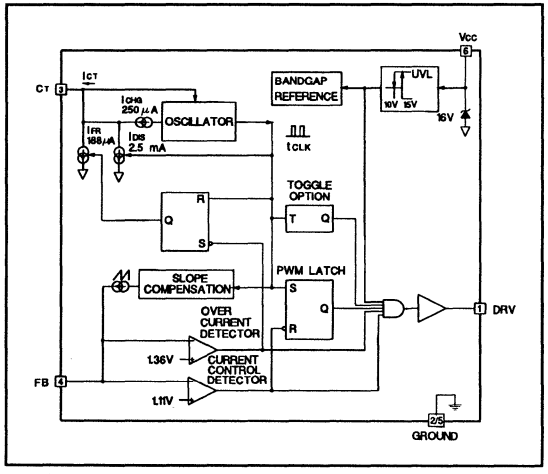
ABSOLUTE MAXIMUM RATINGS

Input Voltage VccMAX	17V
Power Dissipation	
UC7501/7503 U&D (Note 1)	1000mW
UC7501/7503J (Note 2)	825mW
Junction Temperature	150°C
Storage Temperature Range	-55 to +150°C
Lead Soldering Temp. (10 sec.)	300°C
Operating Temperature Range	
(Commercial)	0 to +70°C
(Industrial)	-40 to +85°C
(Military)	-55 to +125°C

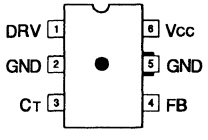
Note 1: Power dissipation must be derated at the rate of 8 mW/°C for operation at TA = 25°C and above.

Note 2: Power dissipation must be derated at the rate of 6.6 mW/°C for operation at TA = 25°C and above.

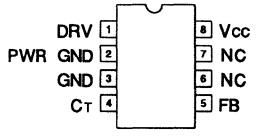
BLOCK DIAGRAM



U-PAK-5
J or N Package



DIL-8 (TOP VIEW)
J or N Package



Note: 8-Pin Power SOIC also available-Designated "DP" suffix.

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INTEGRATED CIRCUITS
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UC7502
ADVANCED INFORMATION

Error Signal Isolator

FEATURES

- Eliminates Opto-Coupler in Feedback Design
- Replaces UC431 and Eliminates Parasitic Zero
- Pulse Transformer Driver
- Same Transformer for Any Output Voltage
- Peak Current Controlled
- Automatic Volt-Second Balancing
- Self-Running Oscillator
- Hi-Performance Op Amp & Bandgap Reference
- Functionally Integrated & Simplified 5-pin Design
- Miniature Surface Mount U-PAK-5 (1 Watt) Package

DESCRIPTION

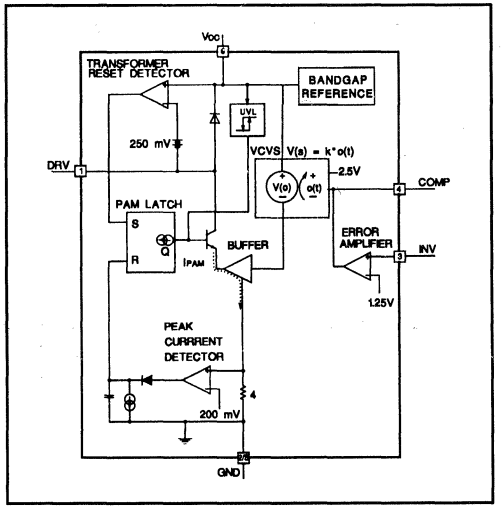
The UC7502 is designed to monitor the output voltage of a power supply, generate an error signal, and transmit the error signal through an isolation barrier using a small pulse transformer. In conjunction with the pulse transformer, it replaces the UC431/optocoupler combination and eliminates the undesirable zero created by that combination. The transformer is driven with pulse amplitude modulation in a free-running oscillator configuration. The period of oscillation is proportional to the pulse transformer inductance. The voltage pulse magnitude is internally limited so that the pulse transformer design need not be changed for various output voltages.

ABSOLUTE MAXIMUM RATINGS

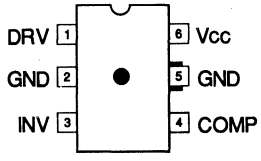
Input Voltage VccMAX. 17V
Power Dissipation (Note 1) 1W
Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . -55 to +150°C
Lead Soldering Temp. (10 sec.) . . . . . 300°C
Operating Temperature Range
(Commercial) . . . . . 0 to + 70°C
(Industrial) . . . . . -40 to +85°C
(Military) . . . . . -55 to +125°C

Note 1: Power dissipation must be derated at the rate of 8 mW/°C for operation at T_A = 25°C and above.

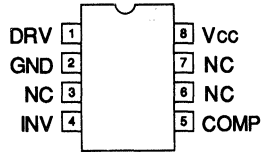
BLOCK DIAGRAM



U-PAK-5
J or N Package



DIL-8 (TOP VIEW)
J or N Package



Note: 8-Pin Power SOIC also available-Designated "DP" suffix.

6/93

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UC19431
UC29431
UC39431

Precision Adjustable Shunt Regulator

PRELIMINARY

FEATURES

- Multiple On-Chip Programmable Reference Voltages
- 0.4% Initial Accuracy
- 0.7% Overall Reference Tolerance
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- 36.0V Operating Supply Voltage
- Reference Accuracy Maintained For Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Opto-Isolator Application
- Improved Architecture Provides a Known Linear Transconductance with a + 5% Typical Tolerance

DESCRIPTION

The UC19431 is an adjustable shunt voltage regulator with 100mA sink capability. The architecture, comprised of an error amplifier and transconductance amplifier, gives the user separate control of the small signal error voltage frequency response along with a fixed linear transconductance. A minimum 3MHz gain bandwidth product for both the error and transconductance amplifiers assures fast response. In addition to external programming, the IC has three internal resistors that can be connected in six different configurations to provide regulated voltages of 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, and 12.24V. A sister device (UC19432) provides access to the non-inverting error ampilifer input and reference, while eliminating the three internal resistors.

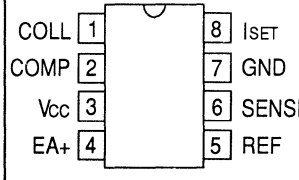
5

ABSOLUTE MAXIMUM RATINGS

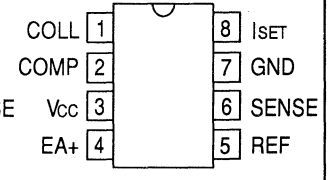
Supply Voltage: V 36V
Regulated Output: V 36V
Internal Resistors: R1, R2, R3 ..... 13V
E/A Input: SENSE 6V
E/A Compensation: COMP 6V
Output Sink Current: I 140mA
Power Dissapation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) .... +300°C
Note: All voltages are with respect to GND
All currents are positive into the specified terminal

CONNECTION DIAGRAMS

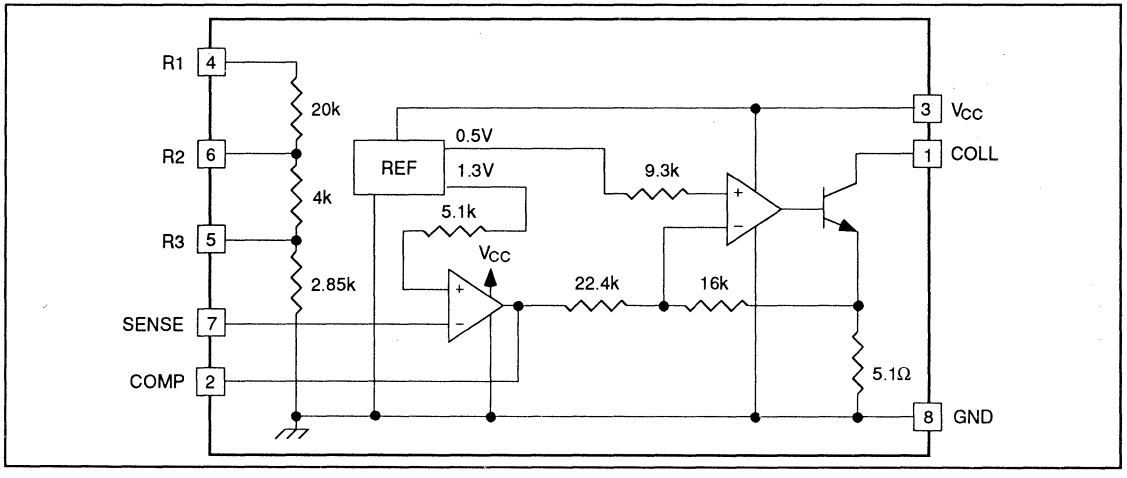
DIL-8 (TOP VIEW)
N or J Package



SOIC-8 (TOP VIEW)
D Package



BLOCK DIAGRAM



PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm•RL, where gm is designed to be -140mS ±10% and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frquency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.\

The SENSE pin is also used as the under-voltage lock out (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. Additional load current or a slower power turn-on than the error amplifier slew rate will be necessary to assure start-up. To increase the bandwidth and ensure start-up at low load current, it is recommended to create a zero along with the pole as shown in the shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

R1, R2, R3: Connection points to the three internal resistors.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

Electrical Characteristics: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C and Pin 1 Output = 2.4V to 36.0V for the UC19431, T_A = -25°C to +85°C and Pin 1 Output = 2.3V to 36.0V for the UC29431, and T_A = 0°C to +70°C and Pin 1 Output = 2.3V to 36.0V for the UC39431, V_{CC} = 15V, I_{COLL} = 10mA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	T_A = 25°C	1295	1300	1305	mV
Reference Temperature Tolerance	V_{COLL} = 5.0V	1291	1300	1309	mV
Reference Line Regulation	V_{CC} = 2.2V to 36.0V, V_{COLL} = 5V		1.2	10.0	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL}= 5V		1.2	10.0	mV
Sense Input Current	V_{CC} = 2.2V to 36.0V	0.2	0.5	uA	
Minimum Operating Current	V_{CC} = 36.0V, V_{COLL} = 5V		0.50	0.80	mA
Collector Current Limit	V_{COLL} = V_{CC} = 36.0V, Ref = 1.35V		130	140	mA
Collector Saturation	V_{CC} = 2.2V to 36.0V, I_{COLL} = 20mA	0.7	1.1	1.5	V
Transconductance (gm)	V_{CC} = 2.2V to 36.0V, V_{COLL} = 3V, I_{COLL} = 20mA	-153	-140	-127	mS
5.1V Reference	Internal Divider	5.05	5.10	5.15	V
12.24V Reference	Internal Divider	12.12	12.24	12.36	V
Error Amplifier A_{VOL}		60	90		dB
Error Amplifier GBW		3.0	5		MHz
Transconductance Amplifier GBW			3		MHz

Note: *The internal divider can be configured to give six unique references. These references are 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, 12.24V.*

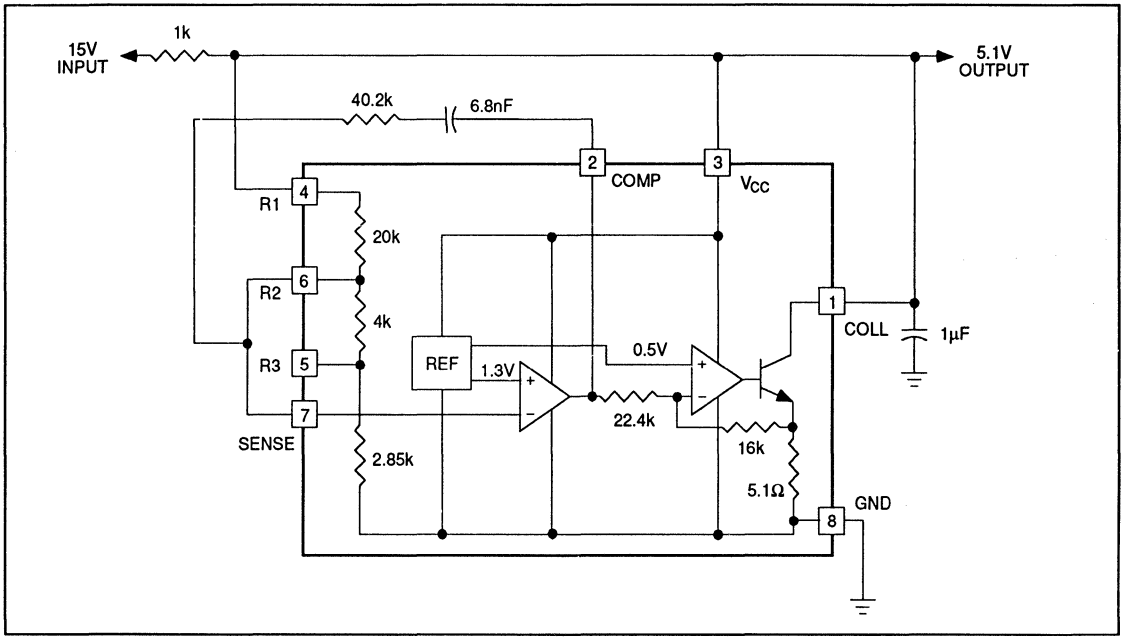


FIGURE 1: Typical 5.1V Shunt Regulator Application

MAG-AMP CONTROLLER APPLICATION

The 0.4% initial reference makes the UC19431 ideal as a programmable shunt regulator. By adding two external resistors, the on-chip 1.3V reference can be gained to any voltage between 2.2V (2.4V for the UC19431) and 36.0V. The input bias current is typically maintained at 0.2µA for the output voltage range. Since the non-inverting error amplifier input is not available, a 5.1k non-inverting input impedance is added to the input of the error amplifier. This allows the user to choose the SENSE pin input impedance to cancel the minimal offset voltage caused by the input bias current.

RESISTOR DIVIDER CONNECTION TABLE FOR SHUNT AND OPTO APPLICATIONS

To obtain the shunt regulated or opto-coupler sensed voltage specified in the left column, connect the internal resistors (R1, R2, R3) as indicated.

REGULATED VOLTAGE	CONNECT R1 TO:	CONNECT R2 TO:	CONNECT R3 TO:
2.82V	SENSE (pin 7)	COLL (pin 1)	SENSE (pin 7)
3.12V	open	COLL (pin 1)	SENSE (pin 7)
5.1V	COLL (pin 1	SENSE (pin 7)	open
7.8V	COLL (pin 1)	SENSE (pin 7)	GND (pin 8)
10.42V	COLL (pin 1)	SENSE (pin 7)	SENSE (pin 7)
12.24V	COLL (pin 1)	open	SENSE (pin 7)

FREQUENCY COMPENSATION

The UC19431 shunt regulator is designed with two independant gain stages. The error amplifier provides 90dB of gain with a typical gain bandwidth product of 5 MHz. The error amplifier provides sufficient gain in order for the sense voltage to be accurately compared to the 1.3V on-chip reference. Complete control of the frequency response of the error amplifier is accomplished with the COMP pin. By putting negative feedback across the error amplifier, either a pole or a pole-zero can be added.

The second gain stage is the transconductance (gm) amplifier. The gm amplifier is designed with a known linear - 140mS of transconductance. The voltage gain is consequently gm•Ro, where Ro is the output impedance at the collector pin. The frequency response of the transconductance amplifier is controlled with the COLL pin. The gain bandwidth product of the gm amplifier is typically 3MHz. A pole or pole-zero can be added to this stage by connecting a capacitor or a series capacitor and resistor between COLL and GND.

The compensation of a control loop containing the UC19431 is made easier due to the independant compensation capability of the error amplifier and gm amplifier. As shown in the applications information, a pole-zero is created with a series resistor and capacitor between SENSE and COMP. The pole created is dominant,while the zero is used to increase the bandwidth and cancel the effects of the pole created by the capacitor between the COLL and GND pins.

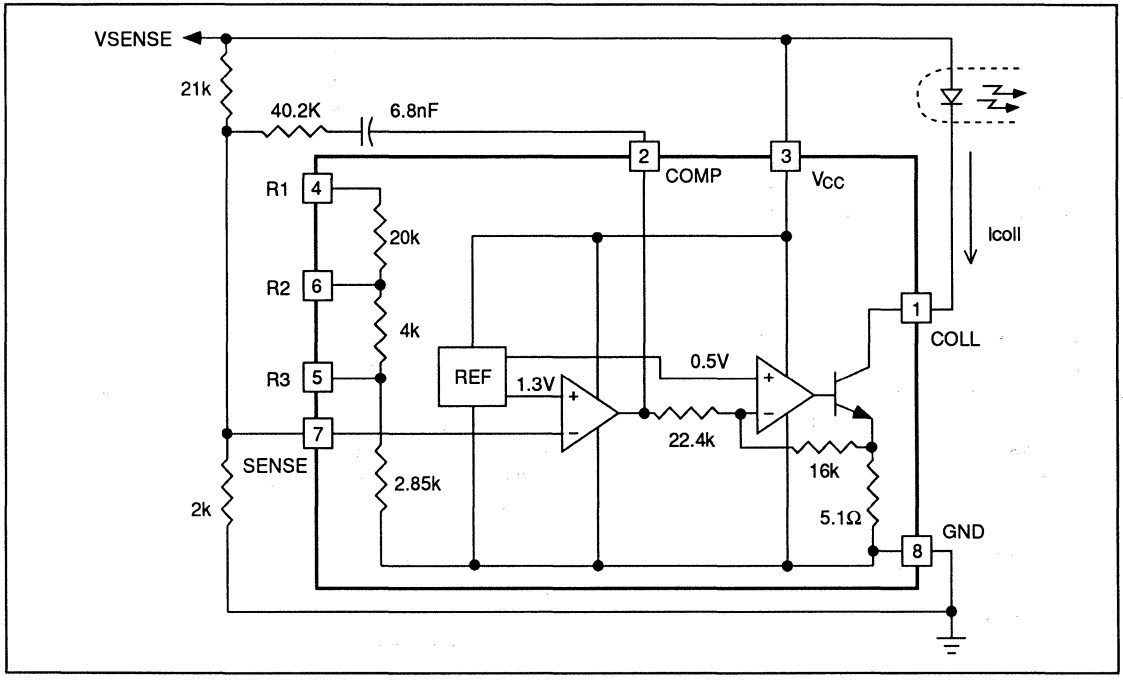


FIGURE 2: 15.0V Shunt Regulator Application

OPTOCOUPLER APPLICATION

The two amplifier circuit architecture employed in the UC19431 is most advantageous for the optocoupler application. The error amplifier provides a fixed open loop gain that is available to apply flexible loop compensation of either poles or zeroes. A fixed transconductance amplifier provides a linear current source compared to the typical transistor's exponential output characteristics. It also eliminates the traditional optocoupler's CTR variations with power supply and voltage, and the need to suffer the additional voltage drop of a series resistor.

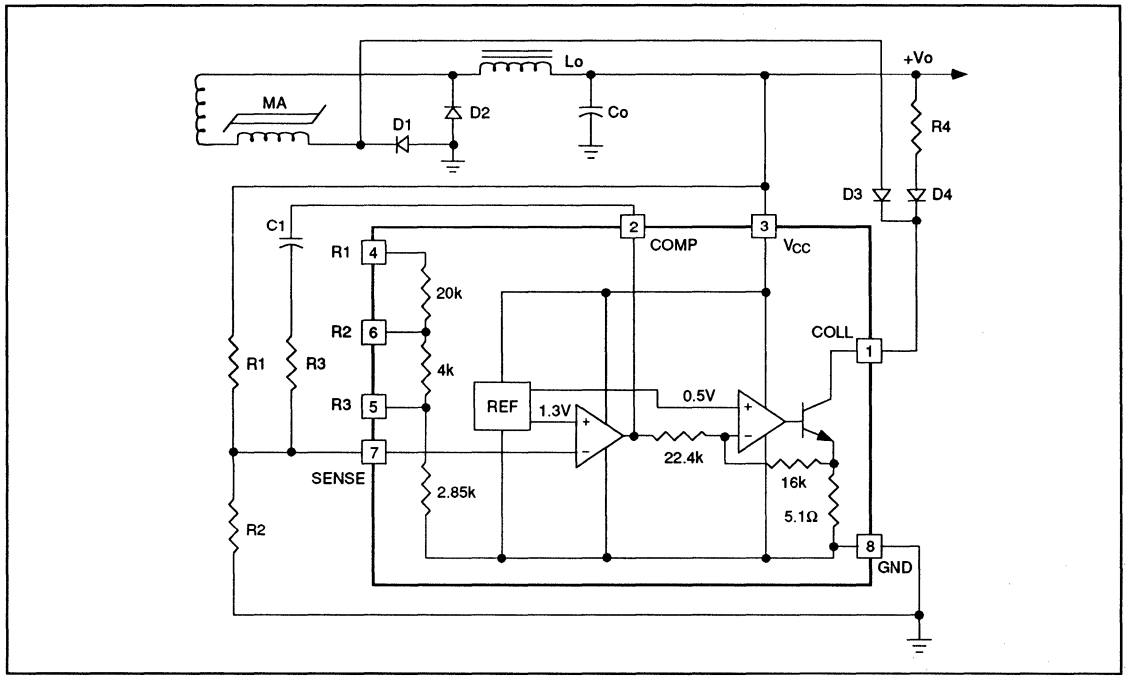


FIGURE 3: Mag Amp Controller Application

MAG-AMP CONTROLLER APPLICATION

The UC19431 makes an excellent controller for mag amp regulated outputs. Working from either a square wave drive or from a PWM signal controlled by another output, a saturable reactor provides highly efficient control, requiring only a reset current which can be generated from its own output.

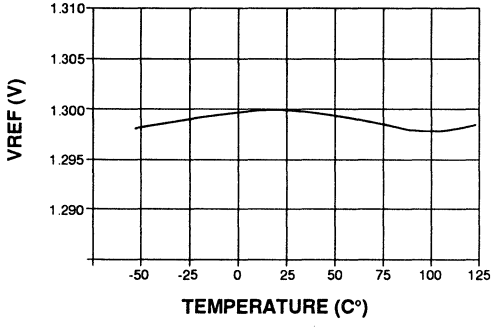


FIGURE 4: Internal 1.3V REF vs. Temperature

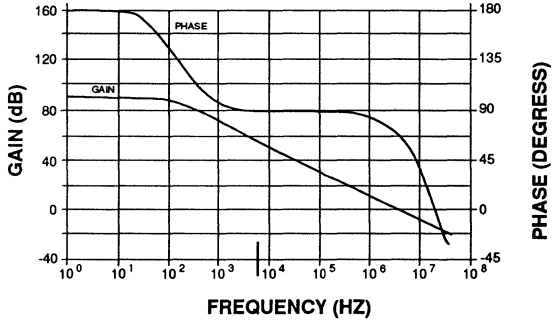


FIGURE 5: Error Amp Voltage Gain and Phase vs. Frequency

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UC19432
UC29432
UC39432
PRELIMINARY

Precision Analog Controller

FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.3V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Opto-Isolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC19432 is an adjustable precision analog controller with 100mA sink capability if the I_{SET} pin is grounded. A resistor between I_{SET} and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the opto-coupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configurations. A sister device, the UC19431 adjustable shunt regulator, has an on-board resistor network providing six pre-programmed voltage levels, as well as external programming capability.

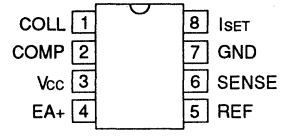
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V_{CC} 36V
Regulated Output: V_{COLL} 36V
E/A Input: SENSE, E/A+ 6V
E/A Compensation: COMP 6V
Reference Output: REF 6V
Output Sink Current: I_{COLL} 140mA
Output Source Current: I_{SET} ..... -140mA
Power Dissapation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) .. +300°C

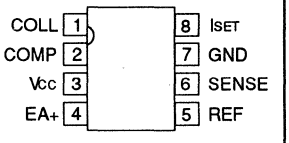
Notes: All voltages are with respect to GND
All currents are positive into the specified terminal

CONNECTION DIAGRAMS

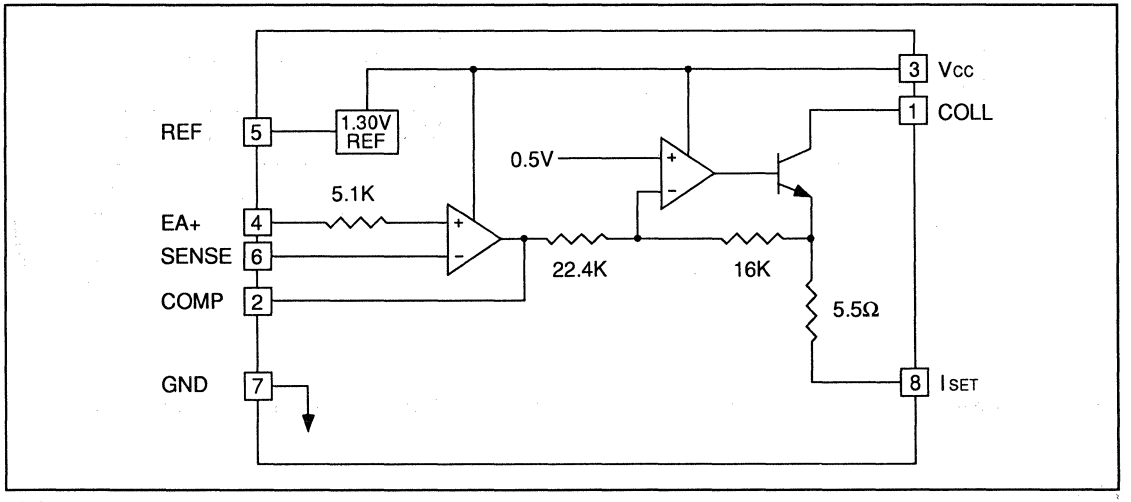
DIL-8 (TOP VIEW)
J or N Package



SOIC-8 (TOP VIEW)
D Package



BLOCK DIAGRAM



PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm•RL, where gm is designed to be -140mS ±10% and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frquency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the under-voltage lock out (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. Additional load current or a slower power turn-on than the error amplifier slew rate will be necessary to assure start-up. To increase the bandwidth and ensure start-up at low load current, it is recommended to create a zero along with the pole as shown in the shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

Vcc: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

ISET: The current set pin for the transconductance amplifier. The transconductance will be -140mS as specified in the electrical table if this pin is grounded. If a resistance RL is added to the ISET pin, the resulting new transconductance is calculated using the following equation: gm= -0.714/ (5.1 + RL). The maximum current will be approximately IMAX= 0.6V/ (5.1 + RL).

REF: The output of the trimmed precision reference. It can source or sink 10 mA and still maintain the 1% temperature specification.

E/A+: The non-inverting input to the error amplifier.

5

ELECTRICAL CHARACTERISTCS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C and Pin 1 Output = 2.4V to 36.0V for the UC19432, TA = -25°C to +85°C and Pin 1 Output = 2.3V to 36.0V for the UC29432, and TA = 0°C to +70°C and Pin 1 Output = 2.3V to 36.0V for the UC39432, Vcc = 15V, Icoll = 10mA, TA= TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	TA = 25°C	1295	1300	1305	mV
Reference Temperature Tolerance	Vcoll = 5.0V	1291	1300	1309	mV
Reference Line Regulation	Vcc = 2.2V to 36.0V, Vcoll = 5V		1.2	10.0	mV
Reference Load Regulation	Icoll = 10mA to 50mA, Vcoll = 5V		1.2	10.0	mV
Reference Sink Current				10	µA
Reference Source Current				-10	µA
E/A Input Bias Current	Vcc = 2.2V to 36.0V		0.2	0.5	µA
E/A Input Offset Voltage				2.0	mV
E/A Output Current Sink (Internally Limited)				16	µA
E/A Output Current Source				-1	mA
Minimum Operating Current	Vcc = 36.0V, Vcoll = 5V		0.50	0.80	mA
Collector Current Limit (Note 1)	Vcoll = Vcc = 36.0V, Ref = 1.35V, ISET = GND		130	140	mA
Collector Saturation	Vcc = 2.2V to 36.0V, Icoll = 20mA	0.7	1.1	1.5	V
Transconductance (gm) (Note 1)	Vcc = 2.2V to 36.0V, Vcoll = 3V, Icoll = 20mA, ISET = GND	-153	-140	-127	mS

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier AVOL		60	90		dB
Error Amplifier GBW		3.0	5		MHz
Transconductance Amplifier GBW			3		MHz

Note 1: *Programmed transconductance and collector current limit equations are specified in the ISET pin description.*

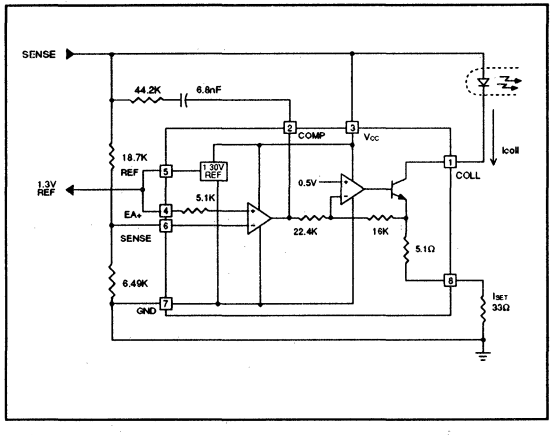


FIGURE 1: 5.0V Opto-coupler Application

OVER-VOLTAGE COMPARATOR APPLICATION:

The signal VIN senses the input voltage. As long as the input voltage is less than 5.5V, the output is equal to the voltage on VIN. During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3V. When VIN exceeds the over voltage threshold of 5.5V, the output is driven low. This forward biases the diode and creates hysteresis by changing the threshold to 4.5V.

OPTO-COUPLER APPLICATION:

The opto-coupler application shown takes advantage of the accessible pins REF and ISET. The ISET pin has a 33 ohm resistor to ground that protects the opto-coupler by limiting the current to about 20mA. This also lowers the transconductance to approximately 19mS. The ability to adjust the transconductance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

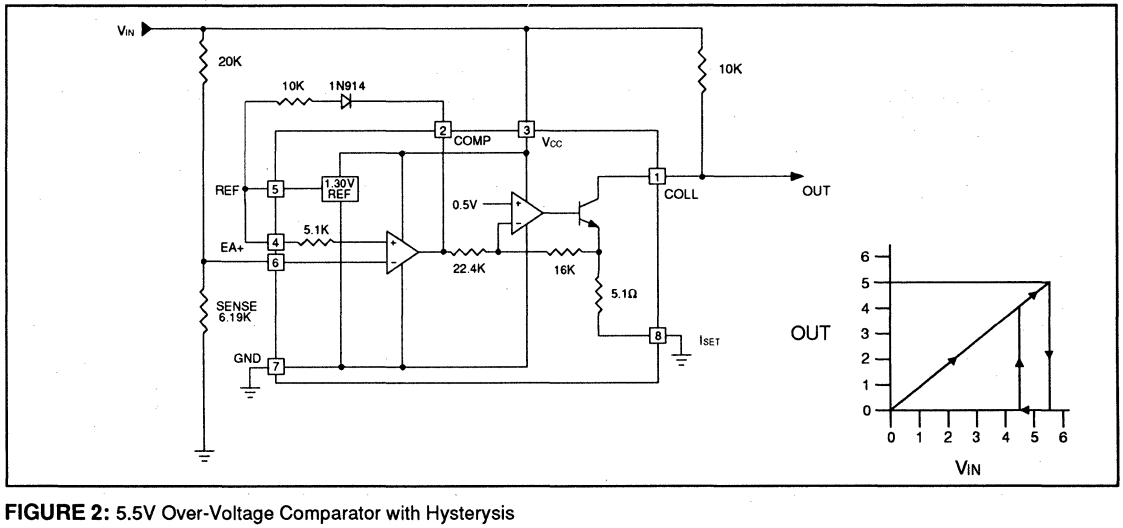


FIGURE 2: 5.5V Over-Voltage Comparator with Hysterysis

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Low Drop Out 3 Ampere Linear Regulator Family

ADVANCED INFORMATION

FEATURES

- Precision Positive Series Pass Voltage Regulation
- 0.45V Drop Out at 3A
- Drop Out Under 2mV at 10mA
- Quiescent Current Under 650µA Irrespective of Load
- Adjustable (5 Lead) Output Voltage Version
- Fixed (3 Lead) Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% • VIN • ISHORT
- Low VOUT to VIN Reverse Leakage
- Thermal Shutdown

DESCRIPTION

The UCC183-0/-3/-5 family of positive linear series pass regulators are tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC183-5 will pass 3A while requiring only 0.45V of typical input voltage headroom (guaranteed 0.6V drop out). These regulators include reverse voltage sensing that prevents current flow in the reverse direction. Quiescent current is always less than 650µA. These devices have been internally compensated in such a manner that the need for a minimum output capacitor has been eliminated.

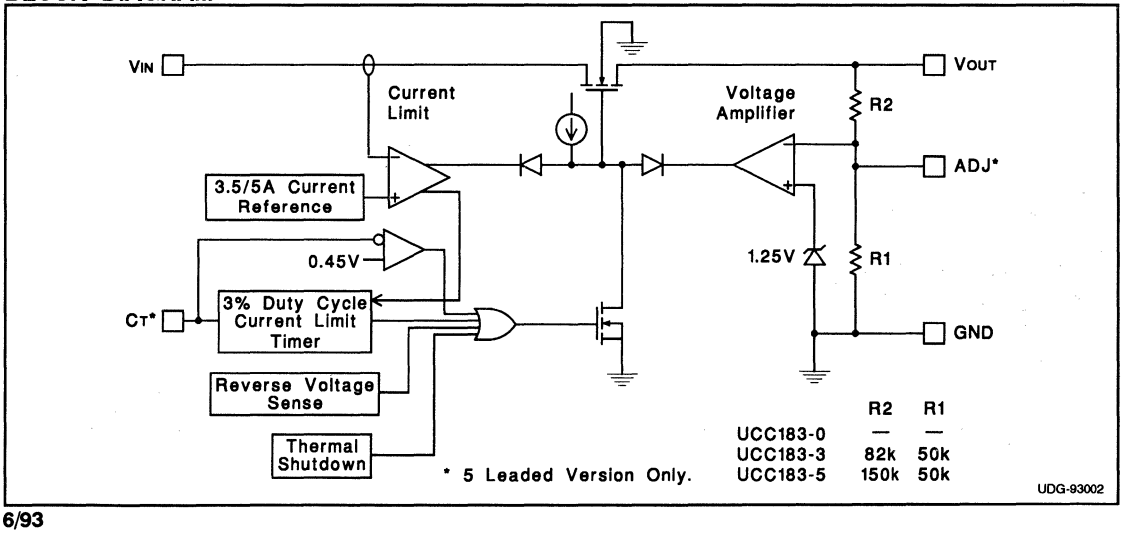
UCC183-3 and UCC183-5 versions are in 3 lead packages and have preset outputs at 3.3V and 5.0V respectively. The output voltage is regulated to 1.5% at room temperature. The UCC183-0 versions, in a 5 lead package, regulate the output voltage programmed by an external resistor ratio.

Short circuit current is internally limited. The device responds to a sustained over-current condition by turning off after a TON delay. The device then stays off for a period, TOFF, that is 32 times the TON delay. The device then begins pulsing on and off at the TON/TOFF duty-cycle of 3%. This drastically reduces the power dissipation during short circuit and means heat sinks need only accommodate normal operation. On the 3 leaded versions of the device TON is fixed at 500µs, on the adjustable 5 leaded versions an external capacitor sets the on time -- the off time is always 32 times TON. The external timing control pin, CT, on the five leaded versions also serves as a shutdown input when pulled low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 40°C.

The UCC183 series is specified for operation over the full military temperature range of -55°C to +125°C. The UCC283 series is specified for operation over the industrial range of -40°C to +85°C, and the UCC383 series is specified from 0°C to +70°C. These devices are available in 3 and 5 pin TO-220 power packages. For other packaging options please consult the factory.

BLOCK DIAGRAM



6/93

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, -40°C to +85°C for the UCC283-X, and -55°C to +125°C for the UCC183-X, V_{IN} = V_{OUT} + 1.5V, I_{OUT} = 0mA, C_{IN} = 10µF, C_{OUT} = 22µF, C_T = 1500pF for the UCC183-0, T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC183-5 Fixed 5V, 3A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	V_{IN} = 5.15V to 10V		2	10	mV
Load Regulation	I_{OUT} = 0mA to 3A		10	20	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Drop Out Voltage, V_{IN} - V_{OUT}	I_{OUT} 3A, V_{OUT} = 4.85V		0.45	0.6	V
	I_{OUT} 10mA, V_{OUT} = 4.85V		50	100	mV
Peak Current Limit	V_{OUT} = 0V	4.5	5	6	A
Over Current Threshold		3	3.5	4	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	TBD	%
Over Current Time Out, T_{ON}	V_{OUT} = 0V	330	500		µs
Ripple Rejection	f = 120Hz, V_{OUT} - V_{IN} > 1.5V, I_{LOAD} = 3A	60			dB
Quiescent Current			400	650	µA
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 5.1V, at V_{OUT}			50	µA
	0V < V_{IN} < V_{OUT}, V_{OUT} < 5.1V, at V_{IN}	-50			µA
UCC183-3 Fixed 3.3V, 3A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	mA
	Over Temperature	3.22		3.38	V
Line Regulation	V_{IN} = 3.45V to 10V		2	7	mV
Load Regulation	I_{OUT} = 0mA to 3A		7	15	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Drop Out Voltage, V_{IN} - V_{OUT}	I_{OUT} 3A, V_{OUT} = 3.15V		0.7	1	V
	I_{OUT} 1.5A, V_{OUT} = 3.15V		0.45	0.6	V
	I_{OUT} 10mA, V_{OUT} = 3.15V		50	100	mV
Peak Current Limit	V_{OUT} = 0V	4.5	5	6	A
Over Current Threshold		3	3.5	4	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	TBD	%
Over Current Time Out, T_{ON}	V_{OUT} = 0V	330	500		µs
Ripple Rejection	f = 120Hz, V_{OUT} - V_{IN} > 1.5V, I_{LOAD} = 3A	60			dB
Quiescent Current			400	650	µA
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 3.35V, at V_{OUT}			50	µA
	0V < V_{IN} < V_{OUT}, V_{OUT} < 3.35V, at V_{IN}	-50			µA
UCC183-0 Adjustable Output, 3A Family					
Regulating Voltage at ADJ Pin	T_J = 25°C	1.23	1.25	1.27	mA
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	V_{IN} = V_{OUT} + 150mV to 10V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 0mA to 3A		2	5	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Drop Out Voltage, V_{IN} - V_{OUT}	V_{IN} > 4V, I_{OUT} = 3A		0.45	0.6	V
	V_{IN} > 3V, I_{OUT} = 1.5A		0.45	0.6	V
	V_{IN} > 3V, I_{OUT} = 10mA		50	100	mV
Peak Current Limit	V_{OUT} = 0V, V_{IN} = 6.5V	4.5	5	6	A
Over Current Threshold	V_{IN} = 6.5V	3	3.5	4	A

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, -40°C to +85°C for the UCC283-X, and -55°C to +125°C for the UCC183-X, V_{IN} = V_{OUT} + 1.5V, I_{OUT} = 0mA, C_{IN} = 10µF, C_{OUT} = 22µF, C_T = 1500pF for the UCC183-0, T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC183-0 Adjustable Output, 3A Family (cont.)					
Current Limit Duty Cycle	V_{OUT} = 0V		3	TBD	%
Over Current Time Out, T_{ON}	V_{OUT} = 0V, C_T = 1500pF	TBD	660	TBD	µs
Ripple Rejection	f = 120Hz, V_{OUT} - V_{IN} > 1.5V, I_{LOAD} = 3A	60			dB
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 10V, at V_{OUT}			50	µA
	0V < V_{IN} < V_{OUT}, V_{OUT} < 10V, at V_{IN}	-50			µA
Bias current at ADJ Input			100	250	nA
Quiescent Current			400	650	µA
Shutdown Threshold	At C_T Input	0.25	0.45		V
Quiescent Current in Shutdown	V_{IN} = 10V		10	25	µA

5

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INTEGRATED CIRCUITS
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Low Power Pulse Width Modulator

UCC1570
UCC2570
UCC3570

PRELIMINARY

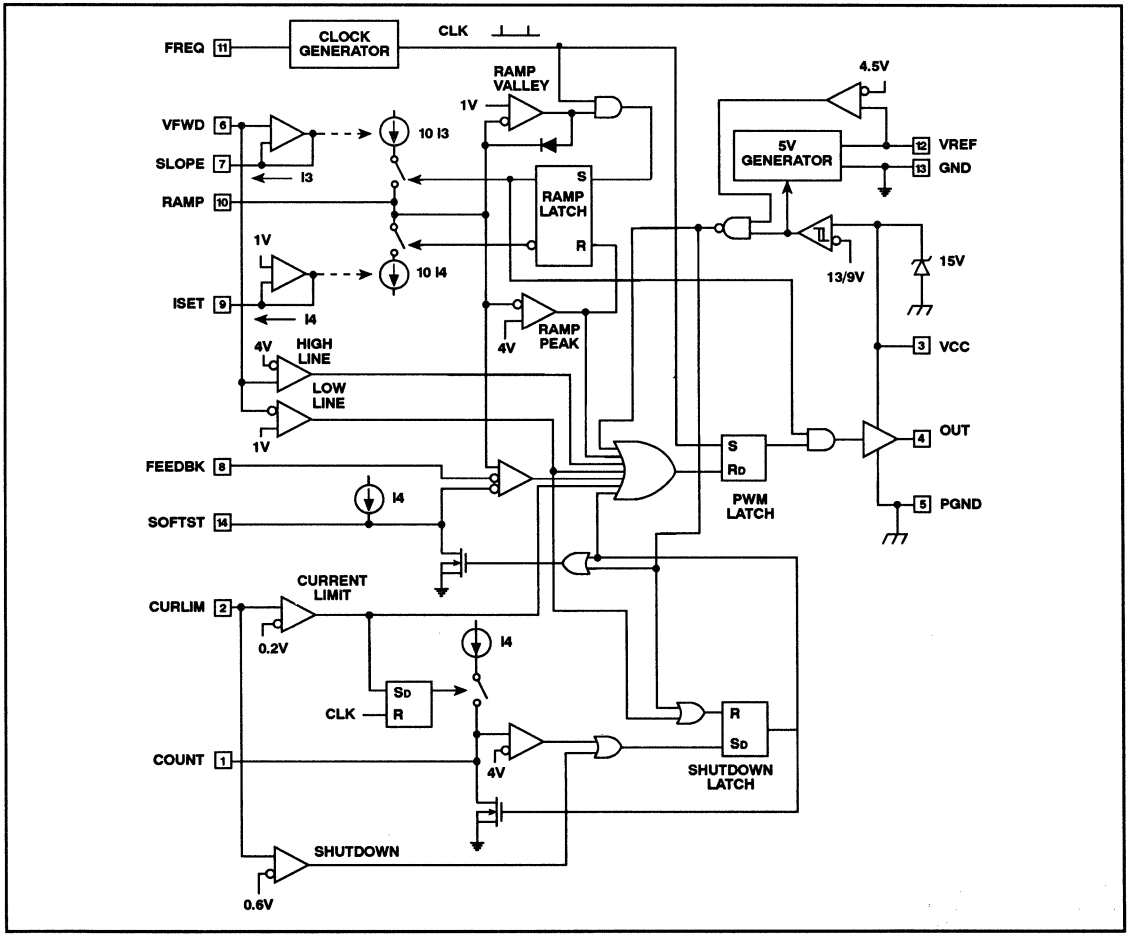
FEATURES

- Low Power BiCMOS Process
- 85µA Start-up Current
- 1mA Run Current
- 1A Peak Gate Drive Output
- Voltage Feed Forward
- Programmable Duty Cycle Clamp
- Opto Coupler Interface
- 500kHz Operation
- Soft Start
- Fault Counting Shutdown
- Fault Latch Off or Automatic Restart

DESCRIPTION

The UCC1570 family of pulse width modulator controllers is intended for application in isolated switching supplies using voltage mode feedback. Made with BiCMOS, this device features low start-up current for efficient bootstrap supply operation, while maintaining the ability to drive a power MOSFET gate at frequencies above 500kHz. Voltage feed-forward provides fast and accurate response to wide line voltage variations without the noise sensitivity of current-mode control. Fast current limiting is included with the ability to latch off after a programmable number of repetitive faults has occurred. Additional versatility is provided with a minimum duty-cycle clamp programmable within a 20% to 80% range.

BLOCK DIAGRAM



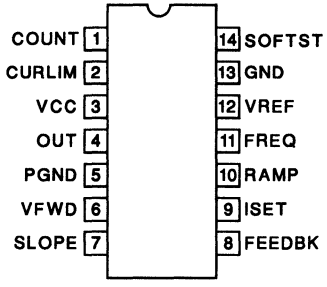
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Current Limited Supply 10mA) ..... Self Limiting
Supply Current 20mA
Analog Inputs (CURLIM, VFWD, FEEDBK) 6V
Programming Current (I (SLOPE), I(ISET)) ..... -1mA
Output Current (I(OUT)) ..... DC 180mA
..... Pulse (0.5μs) 1.2A

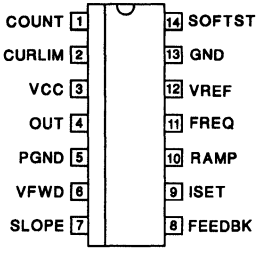
Note: *All voltages are with respect to GND. Currents are positive into the specified terminal.*

CONNECTION DIAGRAMS

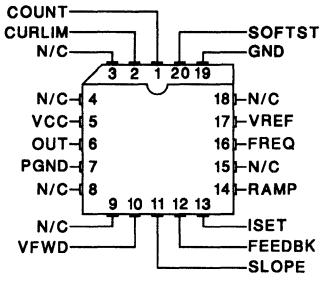
DIL-14 (TOP VIEW)
N or J PACKAGE



SOIC-14 (TOP VIEW)
D PACKAGE



PLCC-20 (TOP VIEW)
L Or Q PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=10V and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
VREF	VCC=10 to 13V, I(VREF)=0 to 2mA	4.9	5	5.1	V
Line Regulation	VCC=10 to 13V		2	10	mV
Load Regulation	I(VREF)=0 to 2mA		2	10	mV
Short Circuit Current	VREF=0V		10	50	mA
VCC					
Vth (On)		12	13		V
Vth (Off)		8	9	10	V
VCC	I(VCC)=10mA	13.5	15	16	V
I(VCC) Start	VCC=11V, VCC Comparator Off		85	150	μA
I(VCC) Run	VCC Comparator On		1	1.5	mA
Line Sense					
Vth High Line Comparator		3.8	4	4.2	V
Vth Low Line Comparator		0.95	1	1.05	V
Iib(VFWD)			0	100	nA
Oscillator					
Frequency		90	100	110	kHz
Ramp Generator					
I(RAMP)/(SLOPE)		9	10	11	A/A
-I(RAMP)/(ISET)		9	10	11	A/A
Peak Ramp Voltage		3.8	4	4.2	V
Valley Ramp Voltage		0.95	1	1.05	V
ISET		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=10V and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start					
Saturation	VCC=11V, VCC Comparator Off		25	100	mV
I(SOFTST)/I(ISET)		0.8	1	1.2	A/A
Pulse Width Modulator					
Iib(FEEDBK)			0	100	nA
FEEDBK	Zero Duty Cycle	0.9	1	1.1	V
	Maximum Duty Cycle, Note 1	3.8	4	4.2	V
Current Limit					
Iib(CURLIM)			0	100	nA
Vth Current Limit		180	200	220	mV
Vth Shutdown		500	600	700	mV
Fault Counter					
Vth		3.8	4	4.2	V
Vsat			0	100	mV
I(COUNT)/I(ISET)		0.8	1	1.2	A/A
Output Driver					
Vsat High	I(OUT)=-100mA		0.4	1	V
Vsat Low	I(OUT)=100mA		0.4	1	V
Rise/Fall Time	C(OUT)=1nF, Note 1		20	100	ns

Note 1: *This parameter guaranteed by design but not 100% tested in production.*

PIN DESCRIPTION

VCC: Chip supply voltage pin. Bypass to PGND with a low esl/esr 0.1µF capacitor. Lead lengths must be minimum.

PGND: Ground pin for the output driver. Keep connections less than 2cm. Carefully maintain low impedance path for high current return.

OUT: Gate drive output pin. Connect to the gate of a power MOSFET with a resistor greater than 2 ohms. Keep connection lengths under 2cm.

VFWD: Voltage Feed Forward and Line Sense pin. Connect to input DC line using a restive divider.

SLOPE: Program the charging current for RAMP with a resistor from this pin to GND. This pin will follow VFWD.

FEEDBK: Input to the pulse width modulation comparator. Drive this pin with an opto coupler and a resistor to VREF. Modulation input range is from 1 to 4V.

ISET: A Resistor from this pin to GND programs RAMP discharge current, FREQ current, SOFTST current, and COUNT Current.

RAMP: Ramp Pin. Connect a capacitor to GND. Rising slope is programmed by current in SLOPE. This slope is compared to FEEDBK for pulse width modulation. The failing slope is programmed by the current in ISET and used to limit maximum duty cycle.

FREQ: Oscillator pin. Program frequency with a capacitor to GND.

VREF: Precision 5V reference, and bypass point for internal circuitry. Bypass this pin with 0.1µF to GND.

GND: Chip ground. Connect to a low impedance ground plane containing all analog low current returns.

SOFTST: Soft start pin. Program with a capacitor to GND.

COUNT: Program the time that fault events will be tolerated before shut down occurs with a capacitor and resistor to GND.

CURLIM: Current Limit Sense pin. Terminates OUT gate drive pulse for inputs over 0.2V. Enables fault counting function (COUNT). For inputs over 0.6V, the chip is immediately shut down.

FUNCTIONAL DESCRIPTION

Power Sequencing

VCC normally connects through a high impedance (R5) to the rectified line, with an additional path (R6) to a low-voltage, bootstrap winding on the power transformer. VFWD normally connects to a divider (R1 and R2) from the rectified line. For circuit activation, the following conditions are all required:

1. VFWD between 1 and 4V
2. VCC has been under 9V (to reset the shutdown latch)
3. VCC over 13V
4. VREF over 4.5V

FUNCTIONAL DESCRIPTION (cont.)

At this time, the circuit will activate. I(VCC) will increase from its start up value of 85μA to its run value of 1mA. The capacitor on SOFTST is charged with a current determined by

$$-I(SOFTST) = 1V/R4.$$

When SOFTST rises above 1V, output pulses will begin and I(VCC) will further rise to a level dictated by gate charge requirements. With output pulses, the low voltage bootstrap winding should now power the controller. If VCC falls below 9V, the controller will turn off and the start sequence will reset and retry.

VCC Clamp

An internal shunt regulator clamps Vcc so that it will not exceed 15V.

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and back low when RAMP either crosses FEEDBK or equals 4V. If, however, any of the following occur, OUT is immediately driven low for the remainder of the clock period:

1. VFWD outside the range of 1 to 4V
2. CURLIM greater than 0.2V
3. FEEDBK or SOFTST less than 1V

Normal output pulses will not resume until the beginning of the next clock period free of the above conditions.

Current Limiting

CURLIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle providing pulse-by-pulse over-current control for excessive loads. This comparator also causes CF to be charged for the remainder of the clock cycle. The charging current is

$$-I(COUNT) = 1V/R4$$

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the Shutdown Latch is set. The COUNT integration delay feature can be bypassed by the Shutdown Comparator which has a 0.6V threshold. The Shutdown Comparator immediately sets the Shutdown Latch. RF in parallel with CF resets the COUNT integrator following transient faults. RF must be greater than 4 * R4.

Latched Shutdown

If CURLIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SOFTST and COUNT, and reduce I(VCC) to approximately 1 mA. When, and if, VCC falls below 9V, the shutdown latch will reset and I(VCC) will fall to 85μA, allowing the circuit to restart. If VCC remains above 9V, an alternate restart will occur if VFWD is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or CURLIM pins.

Deadtime Control

The voltage waveform on RAMP has independently controlled rising and falling edges. At the start of the clock period, RAMP is at 1V and rises to 4V. It then discharges back to 1V and awaits the next clock period. OUT can only be high during the rising part of the waveform, while it is positively blanked off during the falling portion. Setting the -dV/dt slope by R4 from ISET to GND establishes a minimum deadtime. The minimum deadtime is:

$$td = 0.3 * R4 * CR.$$

Choose R4 between 20k and 200k and CR greater than 50pF. In order to have a pulse at OUT in the next clock period, RAMP must fall to 1V prior to the end of the current period. If it does not, OUT will remain low for the entire next clock period.

Voltage Feed-Forward

The +dV/dt on RAMP is made proportional to line voltage. The slope is

$$dV/dt = 10 * VFWD / (R3 * CR),$$

where VFWD is line voltage scaled by R1 and R2. Therefore, a changing line voltage will accomplish an immediate proportionate pulse width change without any action from the feedback amplifier. This will result in constant volt-second drive to the power transformer providing both international voltage operation, and excellent dynamic line regulation. VFWD is intended to operate over a 4:1 range (1 to 4V) with under and over voltage sensors set to drive OUT low if this range is exceeded. Choose R3 between 20k and 200k.

Frequency Set

A capacitor from FREQ to GND will determine a constant clock frequency. Frequency is:

$$F = 1.8/(R4 * CT).$$

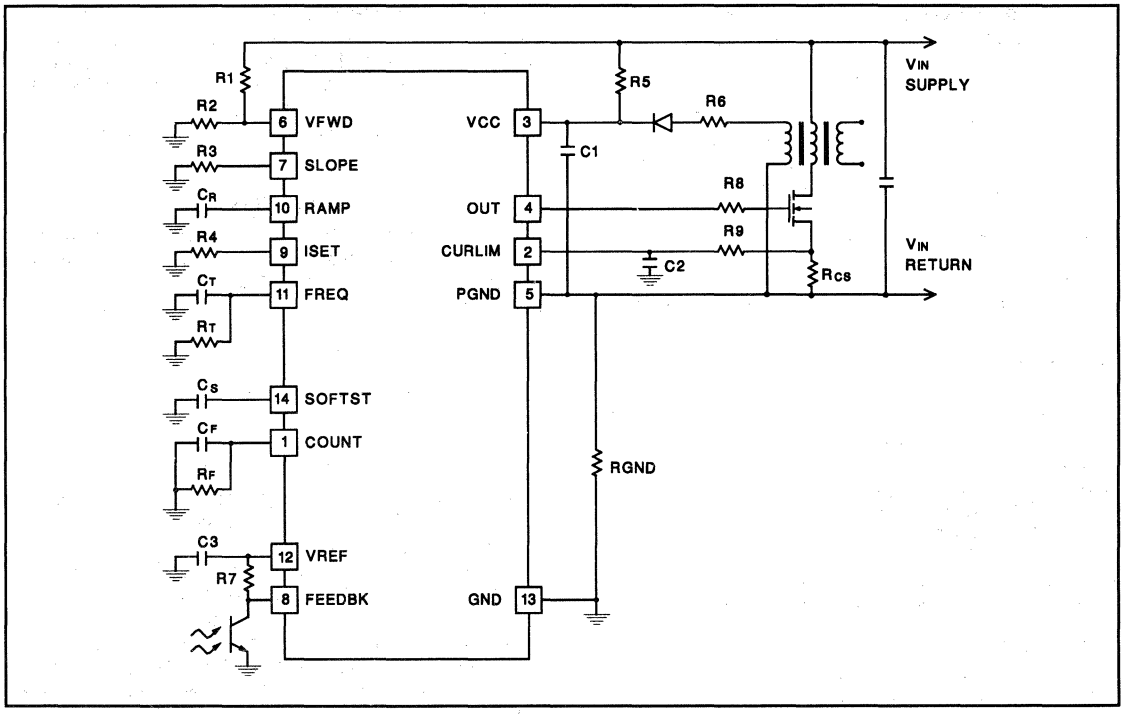
If required, frequency can be trimmed down from the above equation by the addition of RT from FREQ to GND. The reduction in frequency is a function of the ratio of RT/R4. RT should be greater than 2.4 * R4 for reliable operation.

External synchronization can be accomplished by coupling a sliver pulse into a small value series resistor in the ground side of CT. The pulse width should be less than 5% of the oscillator period.

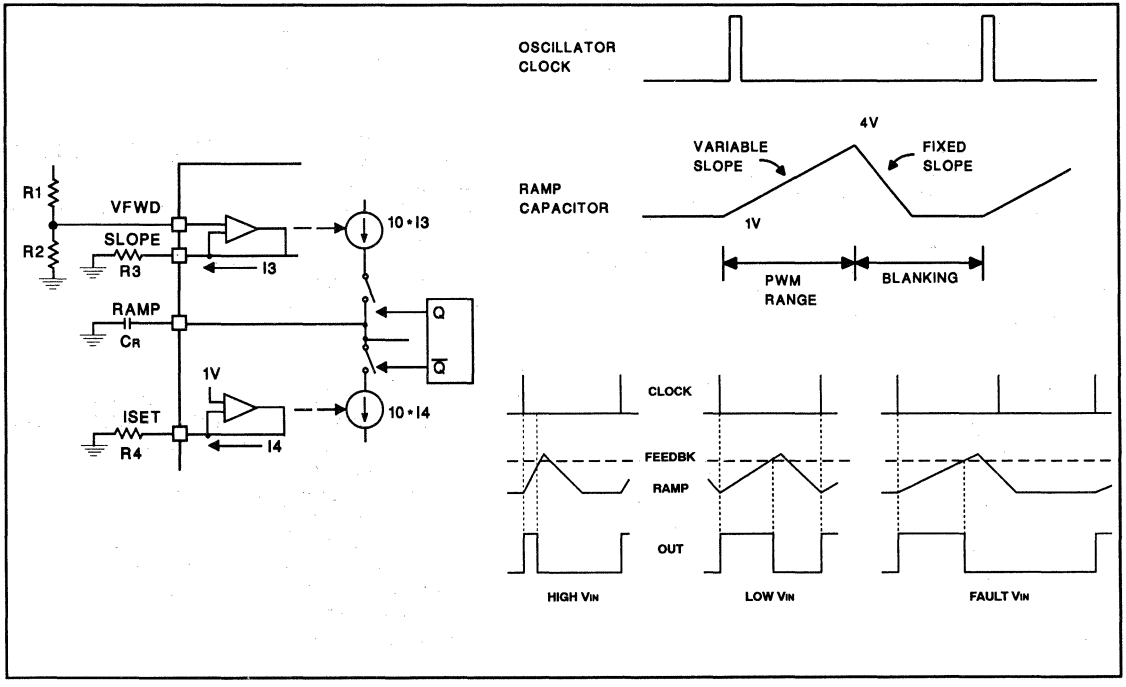
Gate Drive Output

The UCC1570 is capable of 1A peak output current. Bypass VCC with at least 0.1μF directly to PGND. Use a capacitor with low equivalent series resistance and inductance. The connection from OUT to the MOSFET gate should have a 2 ohm or greater damping resistor and the length should be minimized. A low impedance connection must be established between the MOSFET Source (or the bottom of the current sense resistor), the VCC bypass capacitor and PGND. PGND should then be connected by a single path (shown as RGND in the application) to GND.

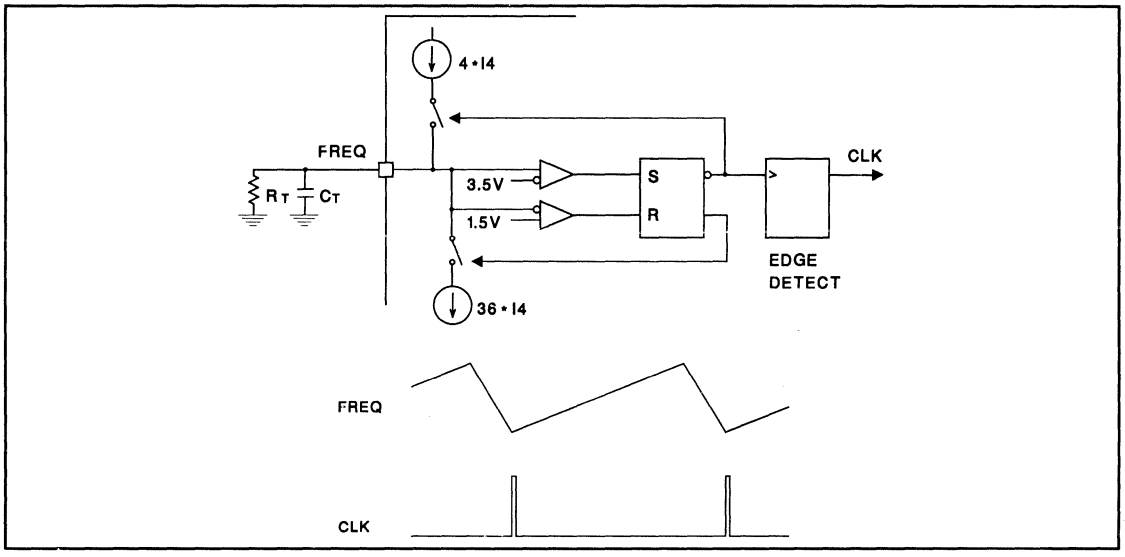
UCC1570 TYPICAL APPLICATION



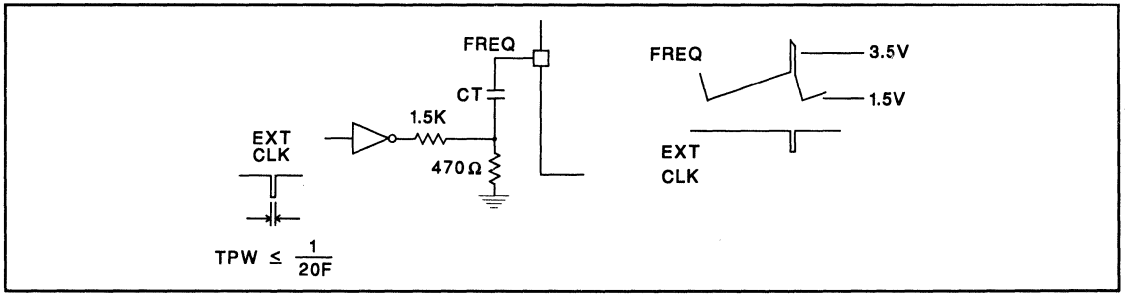
RAMP AND PWM WAVEFORMS



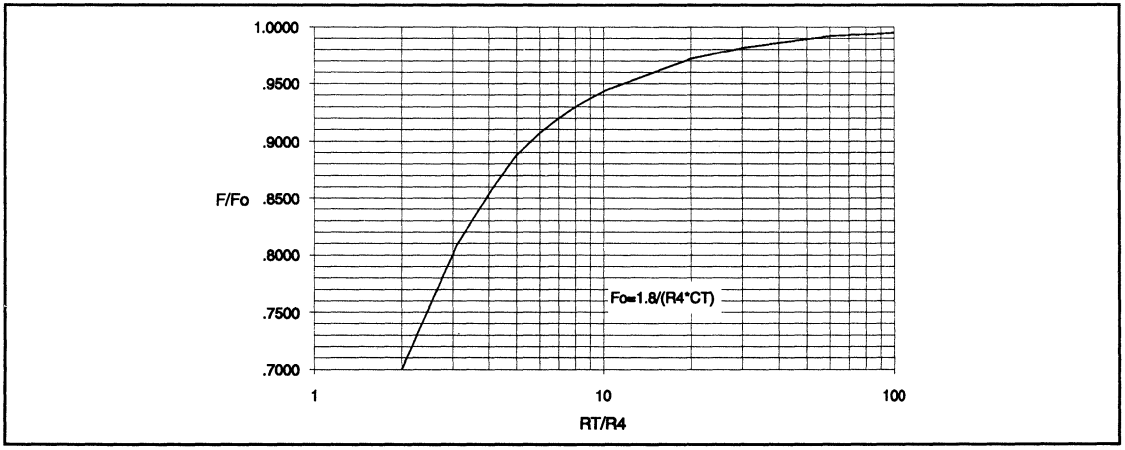
CLOCK GENERATOR



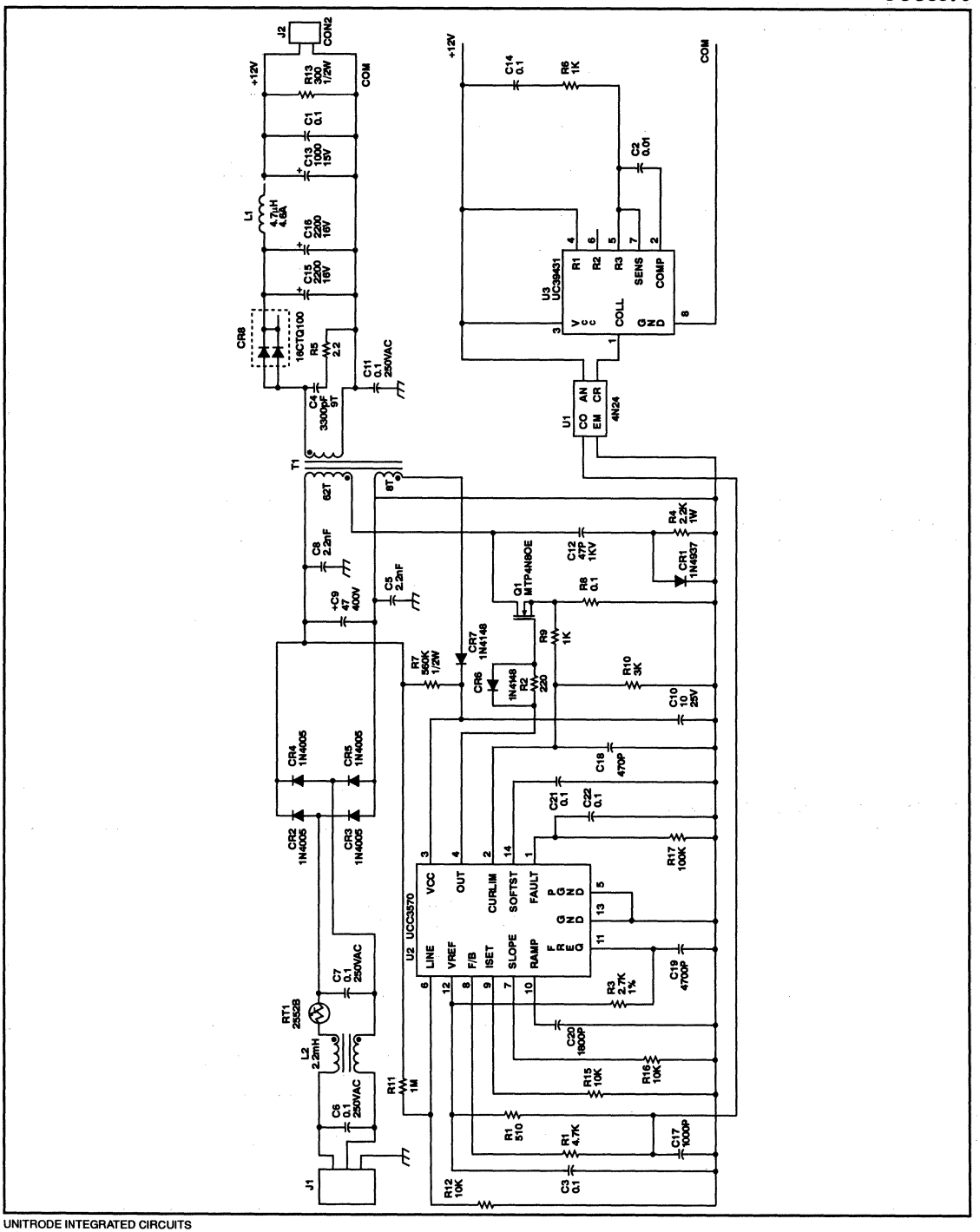
EXTERNAL CLOCK SYNCHRONIZATION



FREQUENCY DEPENDENCE ON RT/ R4 RATIO



TYPICAL APPLICATION



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INTEGRATED CIRCUITS
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UCC1800/1/2/3/4/5
UCC2800/1/2/3/4/5
UCC3800/1/2/3/4/5

Low-Power BiCMOS Current-Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 500µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

DESCRIPTION

The UCC1800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC1842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC1800/1/2/3/4/5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC1803 and UCC1805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC1802 and UCC1804 make these ideal choices for use in off-line power supplies.

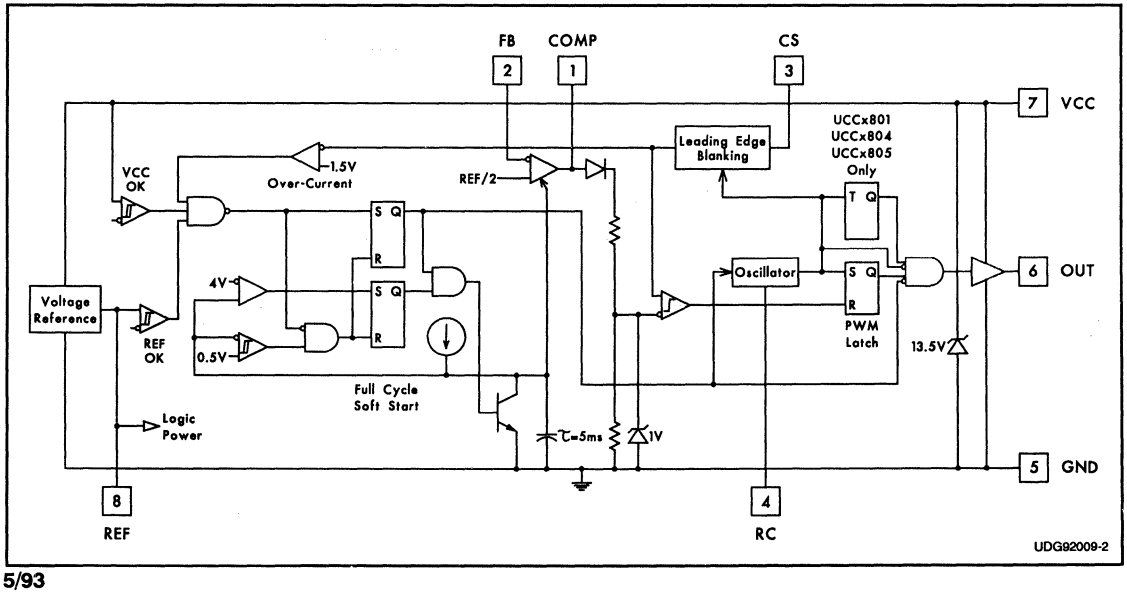
The UCC180x series is specified for operation from -55°C to +125°C, the UCC280x series is specified for operation from -40°C to +85°C, and the UCC380x series is specified for operation from 0°C to +70°C.

5

ORDERING INFORMATION

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx800	100%	5V	7.2V	6.9V
UCCx801	50%	5V	9.4	7.4V
UCCx802	100%	5V	12.5V	8.3V
UCCx803	100%	4V	4.1V	3.6V
UCCx804	50%	5V	12.5V	8.3V
UCCx805	50%	4V	4.1V	3.6V

BLOCK DIAGRAM

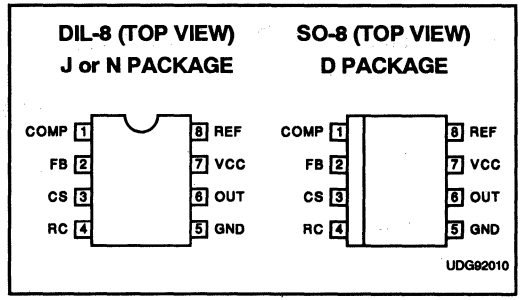


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 12.0V
Supply Current 30.0mA
OUT Current ..... ±1.0A
OUT Energy (Capacitive Load) 20.0µJ
Analog Inputs (FB, CS) ..... -0.3V to 6.3V
Power Dissipation at Ta < +25°C (N or J Package) 1.0W
Power Dissipation at Ta < +25°C (D Package) 0.65W
Storage Temperature Range ..... -65°C to +150°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal.
Note 2:Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAM



ELECTRICAL SPECIFICATIONS

Unless otherwise stated, these specifications apply for -55°≤Ta≤+125°C for UCC180x; -40°≤Ta≤+85°C for UCC280x; 0°C≤Ta≤+70°C for UCC380x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.01µF capacitor from VREF to GND. Ta=Tj.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	Tj=+25°C, I=0.2mA, UCCx800/1/2/4	4.925	5.00	5.075	4.925	5.00	5.075	V
	Tj=+25°C, I=0.2mA, UCCx803, UCCx805	3.94	4.00	4.06	3.94	4.00	4.06	
Load Regulation	0.2mA<I<5mA		10	30		10	25	mV
Total Variation	UCCx800/1/2/4, (Note 7)	4.88	5.00	5.10	4.88	5.00	5.10	V
	UCCx803, UCCx805, (Note 7)	3.90	4.00	4.08	3.90	4.00	4.08	V
Output Noise Voltage	10Hz≤f≤10kHz, Tj=+25°C (Note 9)		70			70		µV
Long Term Stability	Ta=+125°C, 1000 Hours (Note 9)		5			5		mV
Output Short Circuit		-5		-35	-5		-35	mA
Oscillator Section								
Oscillator Frequency	UCCx800, UCCx802, UCCx804, (Note 4)	40	46	52	40	46	52	kHz
	UCCx801, UCCx803, UCCx805, (Note 4)	26	31	36	26	31	36	
Temperature Stability	(Note 9)		2.5			2.5		%
Amplitude		2.30	2.45	2.50	2.30	2.45	2.50	V
Error Amplifier Section								
Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.44	2.50	2.56	2.44	2.50	2.56	V
	COMP=2.0V; UCCx803, UCCx805	1.95	2.0	2.05	1.95	2.0	2.05	
Input Bias Current		-1		1	-1		1	µA
Open Loop Voltage Gain		60	80		60	80		dB
COMP Sink Current	FB=2.7V, COMP=1.1V	0.3		3.5	0.4		2.5	mA
COMP Source Current	FB=1.8V, COMP=REF-1V	-0.2	-0.5	-0.8	-0.2	-0.5	-0.8	mA
PWM Section								
Maximum Duty Cycle	UCCx800, UCCx802, UCCx803	97	99	100	97	99	100	%
	UCCx801, UCCx804, UCCx805	48	49	50	48	49	50	
Minimum Duty Cycle	COMP=0V			0			0	%
Current Sense Section								
Gain	(Note 5)	1.10	1.65	1.80	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP=5V (Note 6)	0.9	1.0	1.1	0.9	1.0	1.1	V
Input Bias Current		-200		200	-200		200	nA

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, these specifications apply for -55°≤Ta≤+125°C for UCC180x; -40°≤Ta≤+85°C for UCC280x; 0°C≤Ta≤+70°C for UCC380x; VCC=10V (Note 3); RT=100K from REF to RC; CT=330pF from RC to GND; 0.1μF capacitor from VCC to GND; 0.01μF capacitor from VREF to GND. Ta=Tj.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Current Sense Section (cont.)								
CS Blank Time		50	100	150	50	100	150	ns
Over-Current Threshold		1.35	1.47	1.60	1.35	1.47	1.60	V
COMP to CS Offset	CS=0V	0.45	0.90	1.35	0.45	0.90	1.35	V
Output Section								
OUT Low Level	I=20mA, all parts		0.1	0.4		0.1	0.4	V
	I=200mA, all parts		0.35	0.90		0.35	0.90	
	I=50mA, VCC=5V, UCCx803, UCCx805		0.15	0.40		0.15	0.40	
	I=20mA, VCC=0V, all parts		0.7	1.2		0.7	1.2	
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, all parts		0.15	0.40		0.15	0.40	V
	I=-200mA, all parts		1.0	1.9		1.0	1.9	
	I=-50mA,VCC=5V, UCCx803, UCCx805		0.4	0.9		0.4	0.9	
Rise Time	C_L=1nF		41	70		41	70	ns
Fall Time	C_L=1nF		44	75		44	75	ns
Under-Voltage Lockout Section								
Start Threshold (Note 8)	UCCx800	6.6	7.2	7.8	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	8.6	9.4	10.2	
	UCCx802, UCCx804	11.5	12.5	13.5	11.5	12.5	13.5	
	UCCx803, UCCx805	3.7	4.1	4.5	3.7	4.1	4.5	
Minimum Operating Voltage after Start (Note 8)	UCCx1800	6.3	6.9	7.5	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8.0	6.8	7.4	8.0	
	UCCx802, UCCx804	7.6	8.3	9.0	7.6	8.3	9.0	
	UCCx803, UCCx805	3.2	3.6	4.0	3.2	3.6	4.0	
Hysteresis	UCCx800	0.12	0.3	0.48	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	1.6	2	2.4	
	UCCx802, UCCx804	3.5	4.2	5.1	3.5	4.2	5.1	
	UCCx803, UCCx805	0.2	0.5	0.8	0.2	0.5	0.8	
Soft Start Section								
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V		4			4		ms
Overall Section								
Start-up Current	VCC<Start Threshold		0.1	0.2		0.1	0.2	mA
Operating Supply Current	FB=0V, CS=0V		0.5	1.0		0.5	1.0	mA
VCC Zener Shunt Voltage	ICC=10mA (Note 8)	12	13.5	15	12	13.5	15	V
Shunt to Start Difference	UCCx802, UCCx804	0.5	1.0		0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.

Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.

Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.

Note 7: Total Variation includes temperature stability and load regulation.

Note 8: Start Threshold and Zener Shunt thresholds track one another.

Note 9: Although guaranteed by design not 100% tested in production.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3800 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

CS: CS is the input to the current sense comparators. The UCC3800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

UCCx800/1/2/4: $$F = \frac{1.5}{R \times C}$$

UCCx803, UCCx805: $$F = \frac{1.0}{R \times C}$$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750mA. OUT is actively held low when VCC is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

VCC: VCC is the power input connection for this device. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F$$

To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the chip as possible and an electrolytic capacitor.

REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When VCC is lower than the UVLO threshold, REF is actively held to GND. This means that REF can be used as a logic output indicating power system status.

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INTEGRATED CIRCUITS
UNITRODE

UCC1806
UCC2806
UCC3806
ADVANCED INFORMATION

Low Power, Dual Output, Current Mode PWM Controllers

FEATURES

- BiCMOS Version of UC1846 Families
- 1.4 mA Max Operating Current
- 100µA Max Start-up Current
- 1.0 A Peak Output Current
- 125 nSec Circuit Delay
- Easier Parallelability
- Improved Benefits of Current-Mode Control

DESCRIPTION

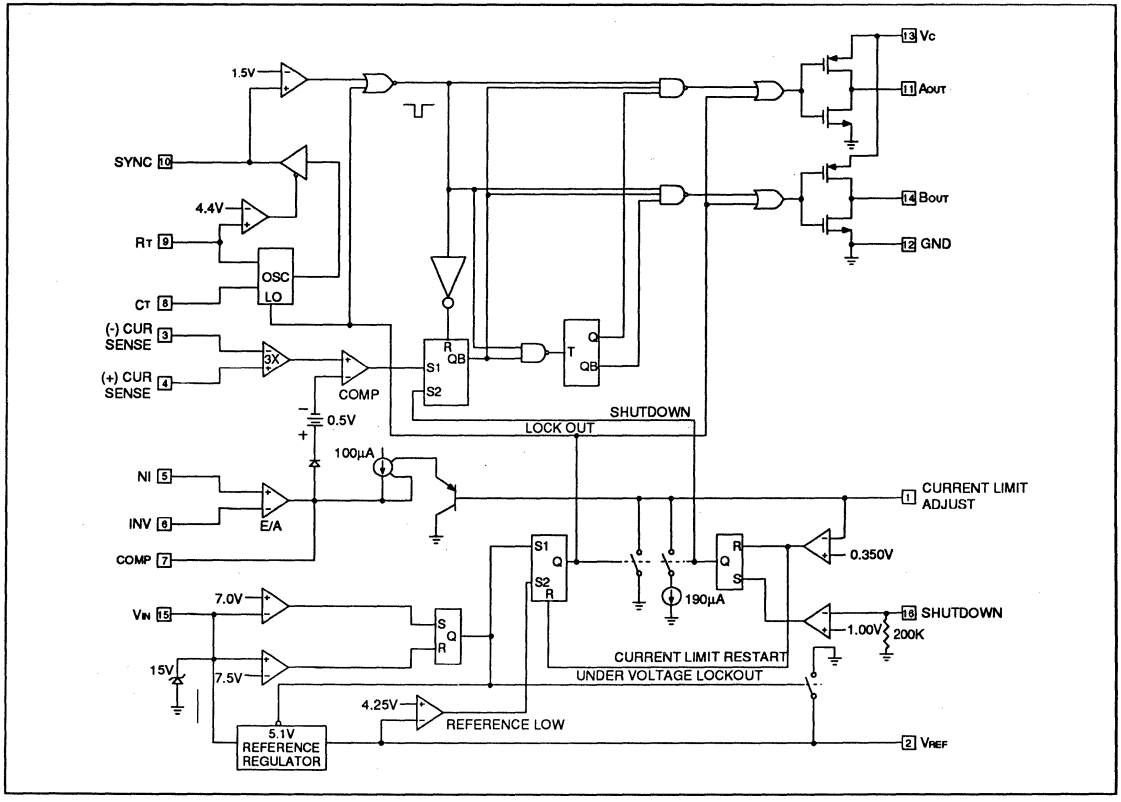
The UCC1806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC1846 series, the UCC1806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical start-up current of 50 µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high-current, FET-driving outputs and a fast current sense loop further enhance device versatility.

Of course, all the benefits of current-mode control including: simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push-pull symmetry correction are readily achievable with the UCC1806 series.

These devices will be available with multiple package options for both thru-hole and surface-mount applications; and in commercial, industrial, and military temperature ranges. Contact factory for availability.

5

BLOCK DIAGRAM



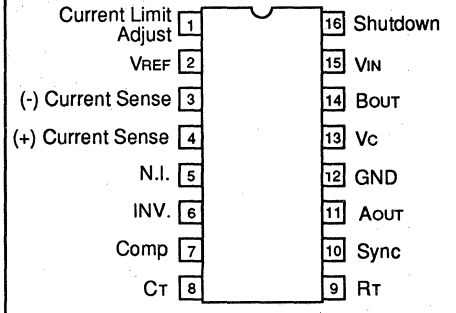
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Low Impedance (Pin 15) ..... +15V
Supply Current, High Impedance (Pin 15) ..... +25mA
Output Supply Voltage (Pin 13) ..... +18V
Output Current, Continuous Source or Sink ..... +/-200mA
Output Current, Gate Drive ..... +/-500mA
Analog Input Voltage (Pin 3,4,5,6,16) ..... -0.3V to +VIN + 0.3V
Sync Output Current (Pin 10) ..... +/-30mA
Error Amplifier Output Current (Pin 7) ..... +10mA/- is Self Limiting
Power Dissipation at Tc = 25°C (Note 3) 1000mW
Power Dissipation at Tc = 25°C (Note 3) 2000mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: All voltages are with respect to Ground, Pin 12.
Note 2: Currents are positive into, negative out of the specified terminal.
Note 3: Consult packaging section of databook for thermal limitations and considerations of package.
Note 4: Pin Numbers refer to DIL-16 pkg.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for UCC1806; -40°C to +85°C for the UCC2806 and 0°C to +70°C for the UCC3806; VIN = 12V, RT = 33k, CT = 330pF, CBYPASS on VREF = .01µF, TA = TJ.

PARAMETER	TEST CONDITION	UCC1806 UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage	TJ = 25°C, Io = 0.2mA	5.05	5.10	5.15	5.02	5.10	5.18	V
Load Regulation	0.2mA < Io < 5mA		3	25		3	25	mV
Temperature Stability	Note 5		0.2	0.6		0.2	0.6	mV/°C
Total Output Variation	Line, Load, Temperature	-150		150	-150		150	mV
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, TJ = 25°C (Note 5)		70			70		µV
Long Term Stability	TA = 125°C, 1000 Hours (Note 5)		5	25		5	25	mV
Output Short Circuit		-10		-30	-10		-30	mA
OSCILLATOR SECTION								
Initial Accuracy	TJ= 25°C	41	49	57	37	49	60	kHz
Temperature Stability	TMIN < TA < TMAX (NOTE 5)		5			5		%
Amplitude			2.35			2.35		V
Sync Delay to Outputs	Pin 8 = 0V, Pin 9 = VREF VSYNC = 0.8V to 2.0V		50	100		50	100	NS
Discharge Current	TJ = 25C, VPIN 8 = 2.0V		2			2		mA
Sync, Vol	IOUT = +1mA			0.4			0.4	V
Sync, VOH	IOUT = -5mA	2.4			2.4			V
Sync, VIL	Pin 8 = 0V, Pin 9 = VREF			0.8			0.8	V
Sync, VIH	Pin 8 = 0V, Pin 9 = VREF	2.0			2.0			V
Sync Input Current		-1		+1	-1		+1	µA
ERROR AMPLIFIER SECTION								
Input Offset Voltage				5			10	mV
Input Bias Current				-1			-1	µA
Input Offset Current				500			500	nA
Common Mode Range		0		VIN-2	0		VIN-2	V
Open Loop Gain	Vo = 1.0 to 4.0	80	100			80	100	dB
Unity Gain Bandwidth		1			1			MHz
Output Sink Current	VID < -20mV, VPIN 7 = 1.0V	1			1			mA
Output Source Current	VID < 20mV, VPIN 7 = 3.0V	-80	-120		-80	-120		µA
Output High Level	VID = 50 mV	4.5			4.5			V
Output Low Level	VID = -50mV			0.5			0.5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for UCC1806; -40°C to +85°C for the UCC2806; and 0°C to +70°C for the UCC3806; V_{IN}= 12V, R_T = 33k, C_T = 330p F, C_{BYPASS} on V_{REF} = .01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
CURRENT SENSE AMPLIFIER SECTION								
Amplifier Gain	V_{PIN3} = 0V, V_{PIN1} = V_{REF} (Notes 3,4)	2.7	3	3.3	2.7	3	3.3	V/V
Maximum Differential Input Signal (Vpin4-Vpin3)	V_{PIN1} = V_{REF}, V_{PIN5} = V_{REF}, V_{PIN6} = 0V	1.1			1.1			
Input Offset Voltage	V_{PIN1} = 0.5V, V_{PIN7} = open		10	30		10	50	mV
CMRR	V_{CM} = 0 to V_{IN} - 3.5	60			60			dB
PSRR		60			60			dB
Input Bias Current	V_{PIN1} = 0.5, Pin 7 open (Note 3)			-1			-1	µA
Input Offset Current	V_{PIN1} = 0.5V, Pin 7 open (Note 3)			1			1	µA
Delay to Outputs	V_{PIN5} = V_{REF}, Pin 6 = 0, Pin4-Pin 3 = 0 to 1.5V step (Note 6)		125	175		125	175	nS
CURRENT LIMIT ADJUST SECTION								
Current Limit Offset	V_{PIN3} = 0, V_{PIN4} = 0, Pin7 = open	0.40	0.5	0.60	0.40	0.5	0.60	mV
Input Bias Current				1			1	µA
SHUTDOWN TERMINAL SECTION								
Threshold Voltage		0.94	1.00	1.06	0.9	1.0	1.1	V
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current		300	200		300	200		µA
Maximum Non-Latching Current			200	80		200	80	µA
Delay to Outputs	V_{PIN16} = 0 to 1.3V		50	100		50	100	nS
OUTPUT SECTION								
Output Supply Voltage		2.5		15	2.5		15	V
Output Low Level	I_{SINK} = 20mA		100	200		100	200	mV
	I_{SINK} = 100mA		0.40	1.1		0.40	1.1	V
Output High Level	I_{SOURCE} = -20mA	11.8	11.9		11.8	11.9		V
	I_{SOURCE}= -100mA	11	11.6		11	11.6		V
Rise Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	nS
Fall Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	nS
UNDER VOLTAGE LOCKOUT SECTION								
Startup Current	V_{IN} < Start Threshold		50	100		50	100	µA
Operating Supply Current			1	1.4		1	1.4	mA
V_{IN} Shunt Voltage	I_{VIN} = 10mA	15		16.5	15		16.5	V
Startup Threshold		6.5	7.5	8	6.5	7.5	8	V
Threshold Hysteresis			0.75			0.75		V

Note 1: All voltages are with respect to Ground, Pin 12.

Note 2: Currents are positive into, negative out of the specified terminal.

Note 3: Parameters measured at trip point of latch with Vpin5 = Vref, Vpin6 = 0V.

Note 4: Amplifier gain defined as:

G = delta change at pin 7/delta change forced at pin 4
delta voltage at pin 4 = 0 to 1V.

Note 5: Not 100% tested in production.

Note 6: Current Sense amp output is slew rate limited to provide noise immunity.

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UCC1810
UCC2810
UCC3810

ADVANCED INFORMATION

Low-Power BiCMOS Dual Current-Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 750µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Outputs
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1% Tolerance Voltage Reference

DESCRIPTION

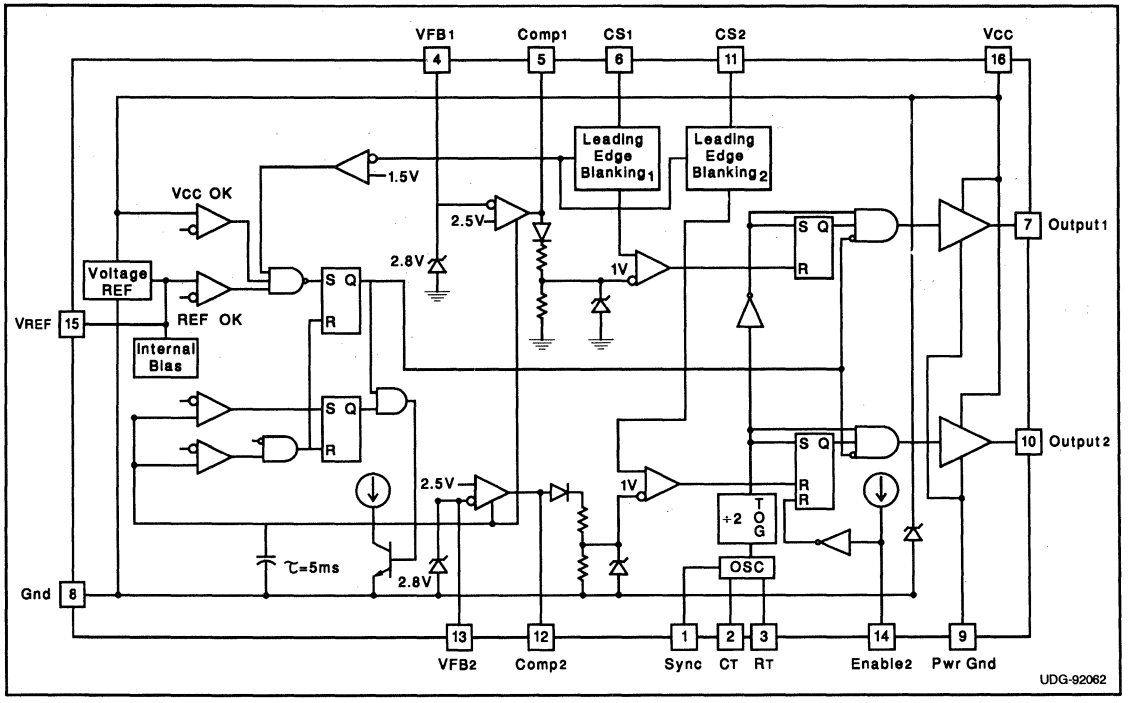
The UCCx810 high-speed dual PWM integrated circuits implement two synchronous pulse-width modulators for use in off-line and DC-to-DC power supplies.

These devices provide perfect synchronization between two PWMs by using the same oscillator. This oscillator also provides a slow-rise, fast-fall waveform which can be used for slope compensation if required.

Using a toggle flip flop to alternate between modulators, this IC ensures that one PWM will not slave, interfere, or otherwise affect the other PWM. This toggle flip flop also ensures that each PWM will be limited to 50% maximum duty cycle, so that in most applications, stable current mode control will not require slope compensation.

These ICs contain many of the same elements of the UC3842 current mode controller family, combined wiht the enhancements of the UCC3800 family so that power supply parts count can be minimized. These enhancements include leading edge blanking of the current sense signals, full-cycle internal soft start, CMOS output drivers, and outputs which remain low even when the supply voltage is removed.

BLOCK DIAGRAM



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Micropower Peak Current Mode Controller

ISDN I.430 RELATED FEATURES

- Zero-Power Startup Capability
- Restricted Mode Detection
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode
- Programmable Continuous Input Current Limit

GENERAL FEATURES

- Low-Power Peak Current Mode Controller
- Oscillator Synchronizes to Secondary Side Clock
- Leading Edge Blanking of Current Sense Waveform
- 50% Maximum Duty Cycle
- Undervoltage Lockout with Hysteresis
- 5V Vdd Logic Supply Regulator
- Programmable Low Line Sensing
- Programmable Soft Start
- Programmable Fault/Restart Delay
- Programmable Output Overload Fault Detection

DESCRIPTION

The UCC1883 is a peak current mode PWM controller designed to operate in conjunction with the UCC1885 secondary-side regulation IC. Together these devices provide the features to implement a fully isolated switch mode power supply with improved output regulation. In addition, this combination of ICs will allow a converter to meet the guidelines set forth in CCITT ISDN recommendation I.430. The chip set is intended mainly for use in DC/DC discontinuous flyback power converters, which are the most economical for developing multiple output voltages. Peak current mode control offers the advantages of pulse-by-pulse current limiting, automatic feed forward, and improved load response characteristics. The UCC1885 companion IC provides feedback control voltage and oscillator synchronization information to the UCC1883 via an isolation pulse transformer. The UCC1883 uses the feedback voltage and frequency information from the UCC1885 to determine the current loop control voltage, i.e. the voltage analog of the current commanded by the voltage loop. This internal control voltage is, in turn, used by the UCC1883 in a conventional peak current mode PWM circuit. Internal leading edge blanking of the current sense waveform eliminates the need for an external filtering network on the I_{SENSE} input. When in restricted mode or lightly loaded, the UCC1883 operates with a minimum pulse width determined by the leading edge blanking circuit. This eliminates the spurious EMI generated if arbitrarily short output pulses are produced by the PWM.

In addition to pulse-by-pulse current limiting, an over current threshold is maintained. A fault condition may also be triggered by repeated peak current limit conditions, through the use of the programmable output overload detector. If either of these faults is detected, OUT is immediately disabled, and a programmable restart period occurs before a soft start sequence is initiated.

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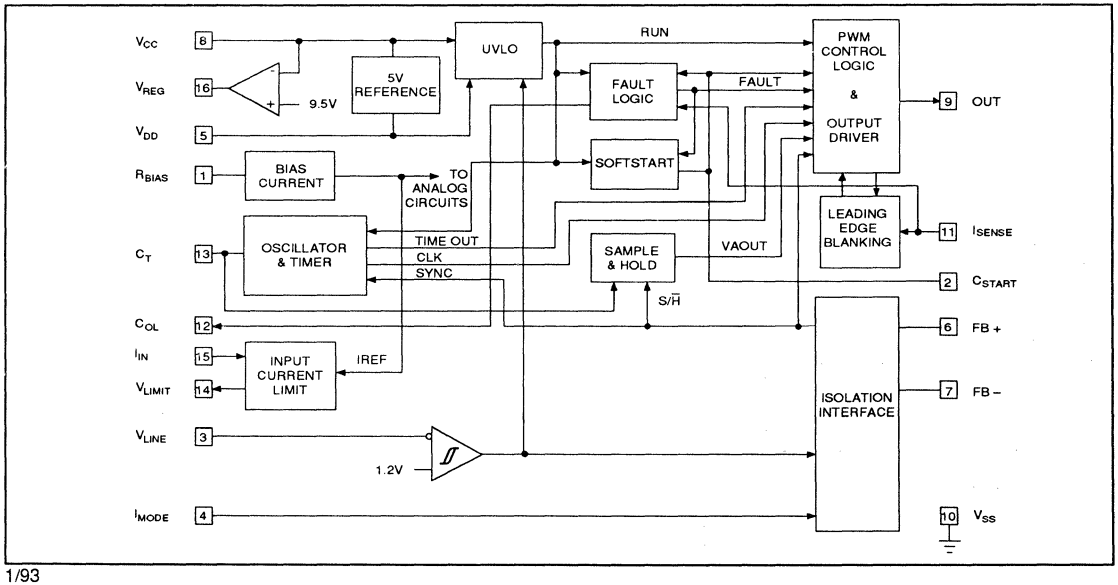
BLOCK DIAGRAM



1/93

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 16.5V
Maximum V_{CC} Slew Rate 10V/ms
Maximum Voltage:
R_{BIAS}, C_{START}, V_{LINE},
I_{MODE}, FB+, FB–, OUT, V_{REG} ..... V_{CC}+ 0.3V to 18V
V_{DD} 7V
C_{OL}, I_{SENSE}, C_T ..... V_{DD}+ 0.3V to 7V
V_{LIMIT}, I_{IN} 0.3V
Minimum Voltage:
V_{LIMIT} ..... – V_{CC}
All Other Pins ..... – 0.3V
Maximum DC Current, Any Pin, Source or Sink 100mA
Maximum Peak Current, Any Pin, Source or Sink ... 500mA
Total Package Dissipation (N package) 1W
Total Package Dissipation (D package) 725mW
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

DESCRIPTION (Continued)

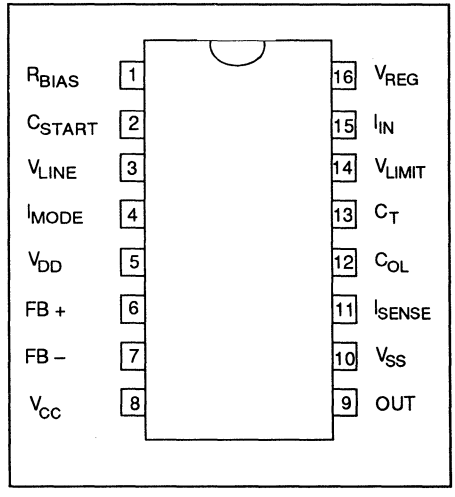
ISDN-specific features allow the UCC1883/UCC1885 combination to be compatible with CCITT recommendation I.430. The linear pre-regulator is intended to control a depletion-mode NMOS pass transistor, such as a BSS129. Startup power drawn from the line can be reduced to zero if a bootstrap winding provides power to the UCC1883 Vcc pin. An internal current comparator is provided to sense restricted mode directly from the input to the converter. Maximum input current may be accurately programmed and continuously limited with the use of an external PMOS pass transistor. Precision programming of the quiescent current used by the UCC1883 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1883 is fabricated in Unitrode's 3um BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1883.

Note 1: All voltages expressed with respect to pin 10, currents are positive into the specified terminal.
Note 2: All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified, with total package power dissipation at or below specified limits.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

Pin Number	Pin Name	Pin Type	Function
1	R_{BIAS}	Analog Program	Quiescent Bias Current Set
2	C_{START}	Analog Program	Soft Start and Restart Delay Timing Set
3	V_{LINE}	Analog Input	Input Line Voltage Sense
4	I_{MODE}	Analog Input	Input Line Polarity Sense
5	V_{DD}	Analog Output	5V Logic Regulator
6	FB +	Digital I/O	Differential Feedback Communication Signal (+)
7	FB –	Digital I/O	Differential Feedback Communication Signal (–)
8	V_{CC}	Power Supply	Positive Power Supply Input
9	OUT	Digital Output	Power Switch Control Voltage
10	V_{SS}	Power Supply	UCC1883 Ground Reference
11	I_{SENSE}	Analog Input	Primary Current Sense
12	C_{OL}	Analog Program	Output Overload Timing Set
13	C_T	Analog Program	Oscillator Frequency Set
14	V_{LIMIT}	Analog Output	Input Current Limit Control Voltage
15	I_{IN}	Analog Program	Input Current Limit Set
16	V_{REG}	Analog Output	9.5V Pre-regulator Control Voltage

CONNECTION DIAGRAM
DIL-16 J or N Package, SOIC-16 D Package



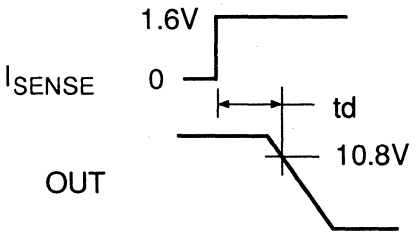
ELECTRICAL CHARACTERISTICS : (Unless otherwise noted, all specifications apply for Ta =0°C to + 70°C for the UCC3883, – 40°C to + 85°C for the UCC2883, – 55°C to + 125°C for the UCC1883; V_{CC} = 12V, V_{DD} = 5V, R_{BIAS} = 200Kohms, C_T = 100pF, Ta = Tj.)

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
UVLO SECTION					
V_{CC} Start Threshold		8.0	9.0	10.0	V
V_{CC} Threshold Hysteresis		1.5	2.0	2.5	V
LINEAR PRE-REGULATOR SECTION					
Regulated V_{CC} Voltage	(See Note 1)	8.6	9.5	10.3	V
Regulated V_{CC} to UVLO Delta		200	500	700	mV
V_{CC} Override Threshold		-	-	10.6	V
USER BIAS SECTION					
R_{BIAS} Voltage	Tj = 25°C	1.17	1.2	1.23	V
R_{BIAS} Voltage Line Regulation	10.0V<V_{CC}<13.5V	-	8	16	mV
Total R_{BIAS} Voltage Variation	Initial + Line + Temperature	1.15	-	1.25	V
INPUT CURRENT LIMIT SECTION					
I_{IN} Offset Voltage	V_{LIMIT} = – 3V	– 8	-	8	mV
Output Reference Current	Tj = 25°C, I_{IN} = 0V	1.6	1.9	2.1	uA
I_{REF} Line Regulation	10.0V<V_{CC}<13.5V	-	10	50	nA
Total I_{REF} Variation	Initial + Line + Temperature	1.5	-	2.2	uA
V_{LIMIT} Low Level	I_{IN} = 0.2V, |Iout| <10nA	– 10.5	– 9	-	V
V_{LIMIT} High Level	I_{IN} = -0.2V, |Iout| <10nA	-	0.6	1.0	V
V_{LIMIT} Output Current	I_{IN} = -0.2V, V_{LIMIT} = – 3V	3	6	14	mA
OSCILLATOR SECTION					
Initial Accuracy	Tj = 25°C	30	35	40	kHz
Voltage Stability	10.0V<V_{CC}<13.5V	-	1	3	%
Total Oscillator Variation	Initial + Line + Temperature	29.5	-	41.5	kHz
C_T Ramp Amplitude		2.35	2.5	2.65	V
SOFT START SECTION					
Soft Start Current (source)	C_{START} = 2.5V	17	30	43	uA
Restart Delay Current (sink)	C_{START} = 2.5V	0.5	1	2	uA
FAULT HANDLING SECTION					
Overload Current Source	C_{OL} = 0.5V	1.4	2.2	3.0	uA
Overload Current Sink	C_{OL} = 0.5V	1.4	2.2	3.0	uA
Overload Fault Threshold		1.4	1.5	1.6	V
Over Current Threshold		1.4	1.5	1.6	V
Over Current Delay	(See Figure 1) (Note 3)	-	100	200	ns
CURRENT SENSE SECTION					
Peak Current Limit Threshold		1.1	1.2	1.3	V
PWM LOGIC and OUTPUT SECTION					
Minimum Duty Cycle	I_{SENSE} = 0V	-	-	0	%
Maximum Duty Cycle	I_{SENSE} = 1.3V	49	50	51	%
OUT Low Level	Iout = 10mA	-	0.05	0.15	V
	Iout = 100mA	-	0.5	1.5	V
OUT High Level	Iout = -10mA	11.85	11.95	-	V
	Iout = -100mA	10.5	11.5	-	V
OUT Rise Time	Tj = 25°C, Cload = 1nF (See Figure 2)	-	25	75	ns
OUT Fall Time	Tj = 25°C, Cload = 1nF (See Figure 2)	-	25	75	ns

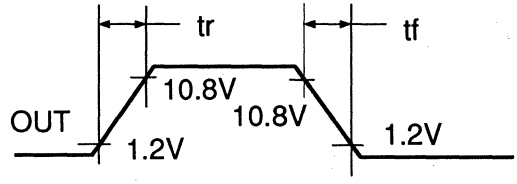
ELECTRICAL CHARACTERISTICS: (Unless otherwise noted, all specifications apply for Ta =0°C to + 70°C for the UCC3883, – 40°C to + 85°C for the UCC2883, – 55°C to + 125°C for the UCC1883; V_{CC} = 12V, V_{DD} = 5V, R_{BIAS} = 200Kohms, C_T = 100pF, Ta = Tj.)

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
ISOLATION INTERFACE SECTION					
FB Input High Voltage	V (FB+) - V (FB–), 0 < = FB < = V_{DD}	-	1.3	1.8	V
FB Input Low Voltage	V (FB+) - V (FB–), 0 < = FB < = V_{DD}	– 1.8	– 1.3	-	V
FB Input Pulse Width	(See Figure 3) (Note 3)	80	300	-	ns
FB Output Pulse Width	(See Figure 3) (Note 3)		75		ns
LOLINE Status Threshold		1.0	1.2	1.3	V
RSMODE Status Threshold		1	2	4	uA
V_{DD} REGULATOR					
V_{DD} Output Voltage	No External Load	4.75	5	5.25	V
V_{DD} Line Regulation	10.0V < V_{CC} < 13.5V	-	10	30	mV
V_{DD} Load Regulation	– 5mA < Iout < 0mA	-	100	200	mV
V_{DD} Short Circuit Current Limit	V_{DD} = 0V	10	50	80	mA
POWER SUPPLY					
DC Supply Current		-	200	250	uA
C_{PD}		-	150	-	pF

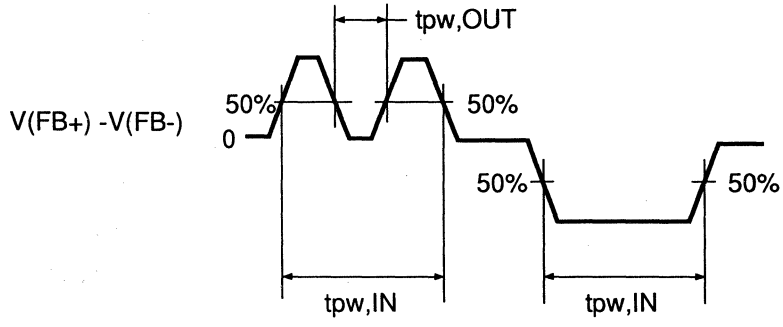
Note 1: BSS129 (or equivalent) External Pass Element, 1uF Ceramic Bypass; see Figure 6.
Note 2: Operating in Conjunction with UCCx885 Using Equal Valued R_{BIAS}.
Note 3: This Parameter Guaranteed but not 100% tested in production.



OVER CURRENT FAULT TIMING
FIGURE 1



OUTPUT RISE & FALL TIME
FIGURE 2



ISOLATION INTERFACE TIMING
FIGURE 3

APPLICATIONS INFORMATION

UNDERVOLTAGE LOCKOUT and SOFT START

When power is first applied to the UCC1883, C_{START} is held at V_{SS} until V_{CC} exceeds 9.0V and V_{DD} exceeds 4.4V. During this period of UVLO, the following state exists:

1) C_{START} is held low,
2) OUT is held low,
3) V_{REG} is forced to V_{CC} until V_{CC} > 4V, and
4) V_{LIMIT} becomes a high impedance output.

Once adequate operating voltages have been established, the input current limit function is enabled. C_{START} and OUT are still held low until the voltage on the V_{LINE} pin exceeds 1.2V, indicating ample voltage is stored on the converter's bulk filter capacitor. At that time, C_{START} is released and allowed to charge from an internal 25uA current source. The UCC1883 then begins to transfer energy to the secondary side of the converter by pulse width modulating the ramp voltage on C_T against the charging voltage on C_{START}. During this soft start period, all fault functions, pulse-by-pulse current limiting, and input current limiting are enabled. Note that the dV/dt established at the converter output by the positive dV/dt of C_{START} must be strictly less than the dV/dt established on the UCC1885 SOFTREF pin, if secondary-side soft start is utilized. The UCC1883 continues the blind soft start procedure until the first set of communication pulses is received from the secondary side via the isolation interface. At that time, all control of the power switch is effectively transferred to the secondary-side regulation IC. Should communication pulses never be received, or should they be discontinued during operation, blind PWM operation continues with the output pulse width limited by the internal 50% duty cycle clamp or pulse-by-pulse current limit with all fault processing enabled.

USER BIAS PROGRAMMING

The R_{BIAS} pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1883. A resistor from this pin to V_{SS} establishes a reference current according to the equation

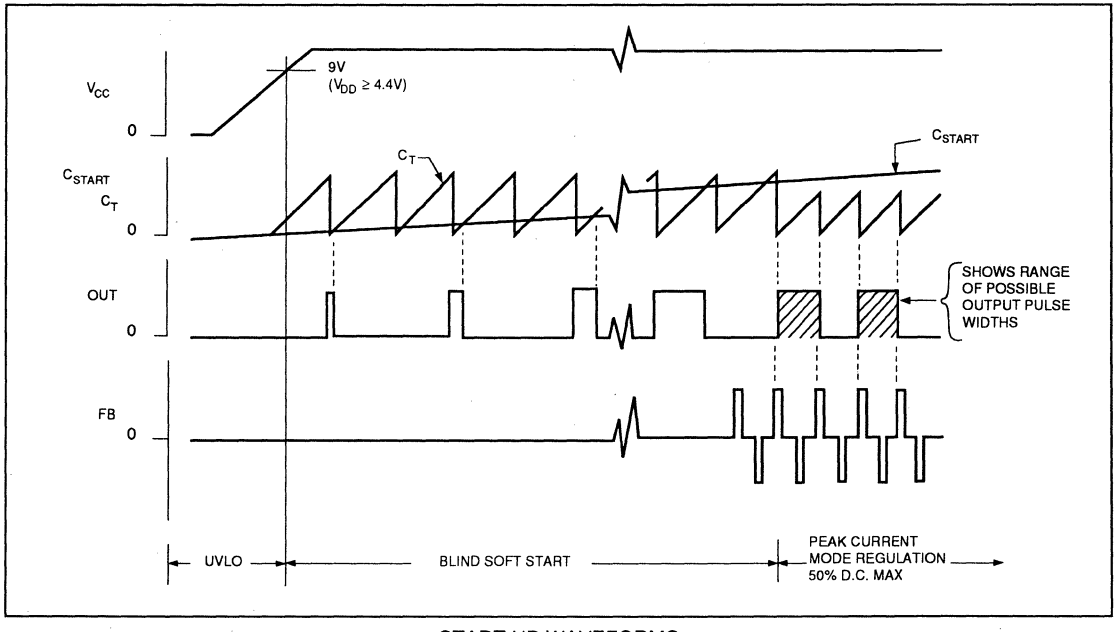
$$I_{BIAS} = \frac{1.2V}{R_{BIAS}}$$

Recommended range for R_{BIAS} is 39.2 KΩ to 392 KΩ. Internal circuits on the UCC1883 consume a total quiescent current of 9 • I_{BIAS}, plus some fixed currents amounting to about 85uA at room temperature. Additional dynamic current consumption may be calculated with C_{PD} (see specifications), given a certain oscillator frequency f_{OSC}, from the equation

$$I_{DYNAMIC} = C_{PD} \cdot V_{CC} \cdot f_{OSC}$$

9.5V LINEAR PRE-REGULATOR

The UCC1883 contains a control amplifier, which when used with a depletion-mode NMOS pass transistor such as the



START UP WAVEFORMS

FIGURE 4

BSS129, can provide a 9.5V linear pre-regulator to supply V_{CC} directly from the input line. The depletion-mode device guarantees the regulator is self-starting. Bypass values less than 3.3uF are recommended when the pre-regulator is utilized. The pre-regulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 10.6V to the V_{CC} pin. Note that the UCC1883 has 2V of UVLO hysteresis to allow use of more conventional startup circuitry, if the power consumption of such implementations can be tolerated. In these cases, any value of bypass capacitance is acceptable, although a minimum value of 0.01uF is recommended for all configurations.

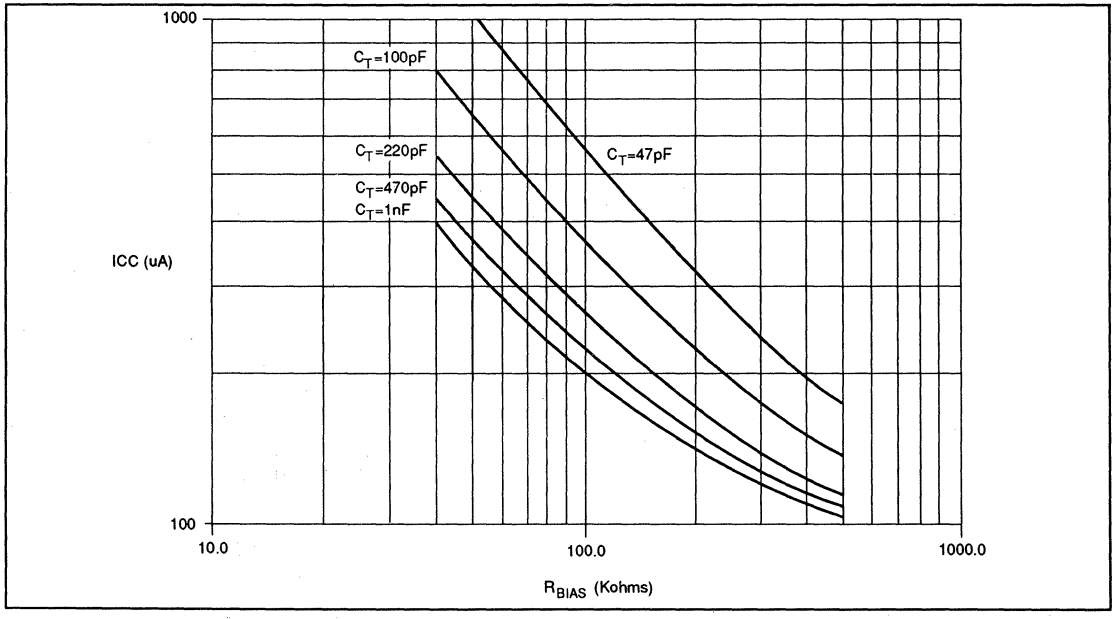
INPUT CURRENT LIMIT PROGRAMMING

The UCC1883 also incorporates the necessary control amplifier and current reference to implement a continuous input current limit mask conforming to CCITT recommendation I.430. When using this feature, the ratio of a sense and programming resistor determine the magnitude of the current passed by an external PMOS transistor. The PMOS device must be able to withstand the maximum input voltage seen by the converter, and its R_{ON} will cause some reduction in efficiency during normal operation, due to conduction losses. Referencing the application diagram of figure 7, the control amplifier programs a peak input current according to the equation

$$I_{LIMIT} = \left(\frac{R_P}{R_S} + 1\right) \cdot \frac{0.4}{R_{BIAS}}$$

by moving the gate of the external PMOS device until equal voltage is impressed across R_P and R_S. In addition to the input capacitance of the PMOS pass device, some compensation capacitance from V_{LIMIT} to V_{SS} may be required. However, too much capacitance on V_{LIMIT} will increase the inrush current response time beyond that allowed by recommendation I.430. A total capacitance of between 330pF and 2.2nF is recommended. A shunt bleeder resistor should be added across the PMOS pass transistor to facilitate converter startup. Due to the large values of resistance which will typically be encountered, a 10pF speedup capacitor across R_P is suggested to help maintain good phase margin in the control loop. A clamping diode across R_S improves transient response by preventing excessive error voltage from being stored on the R_P speedup capacitor during V_{LIMIT} slewing. Finally, a 12V zener clamp from V_{LIMIT} to V_{SS} is recommended to protect the gate of the PMOS device from over voltage and to limit the voltage slew which must occur before entering the current limit state. During normal converter operation, when less than the programmed current limit is being drawn from the line, the control loop opens and V_{LIMIT} moves to its maximum negative value, effectively turning the PMOS limit transistor into a series switch.

If a more accurate current reference than that supplied by the UCC1883 is desired, a precision resistor may be wired from an appropriate reference voltage to I_{IN}. Since I_{IN} is held at V_{SS}



AVERAGE DC CURRENT VS. R_{BIAS} (V_{CC}= 12V) NOT INCLUDING POWER SWITCH GATE CURRENT

FIGURE 5

(ground) by the current limit control amplifier, the additional current created in this case is equal to the reference voltage divided by the external resistor. A reference of at least 2V is recommended to decimate errors caused by the input offset voltage of the control amplifier. Because the reference current provided by the UCC1883 still sums into the I_{IN} pin, a minimum external reference current value of $4V/R_{BIAS}$ is recommended to minimize errors caused by the initial tolerance of the internal current reference.

FAULT HANDLING

Three fault conditions which immediately disable the output are detected by the UCC1883 housekeeping circuitry. These are:

1) UVLO,
2) 1.5V or higher on the I_{SENSE} pin, and
3) 1.5V or higher on the C_{OL} integrator pin.

Unlike the pulse-by-pulse current limit comparator, no leading edge blanking is applied to the over current fault comparator, which has a nominal 1.5V threshold. A capacitor to V_{SS} may be used on the C_{OL} pin to program the output overload fault integrator. The polarity of the 2.2uA current sourced by the internal circuitry driving the C_{OL} pin potentially changes on each falling edge of OUT. If the output pulse was terminated as the result of a peak current event, then current is sourced to C_{OL}, otherwise current is sunk from C_{OL} to V_{SS}. If the voltage on C_{OL} ever reaches 1.5V, a fault condition is set.

If any fault condition is detected once UVLO has ended, the fault is latched and a restart delay elapses before a soft start is attempted. This delay is normally controlled by an internal 1uA discharge of the C_{START} pin from V_{DD} to 0.2V. If a fault occurs during soft start, the output is immediately disabled, but C_{START} is fully charged (4.8V) before a restart delay begins. A fixed restart delay to soft start timing ratio of 25:1 may be obtained with only a capacitor from C_{START} to V_{SS}. This ratio may be decreased by adding an external resistor between C_{START} and V_{SS}. The value of this resistor should be greater than the value of the current programming resistor on the R_{BIAS} pin.

ISOLATION INTERFACE

In addition to receiving synchronization and duty cycle control information from the secondary side of the converter, the UCC1883 isolation interface also transmits digital status information to the secondary side. This digital information reflects the state of two internal analog comparators which monitor the V_{LINE} and I_{MODE} pins. A voltage of less than 1.2V on V_{LINE} is indicated by a true LOLINE bit, and an input current

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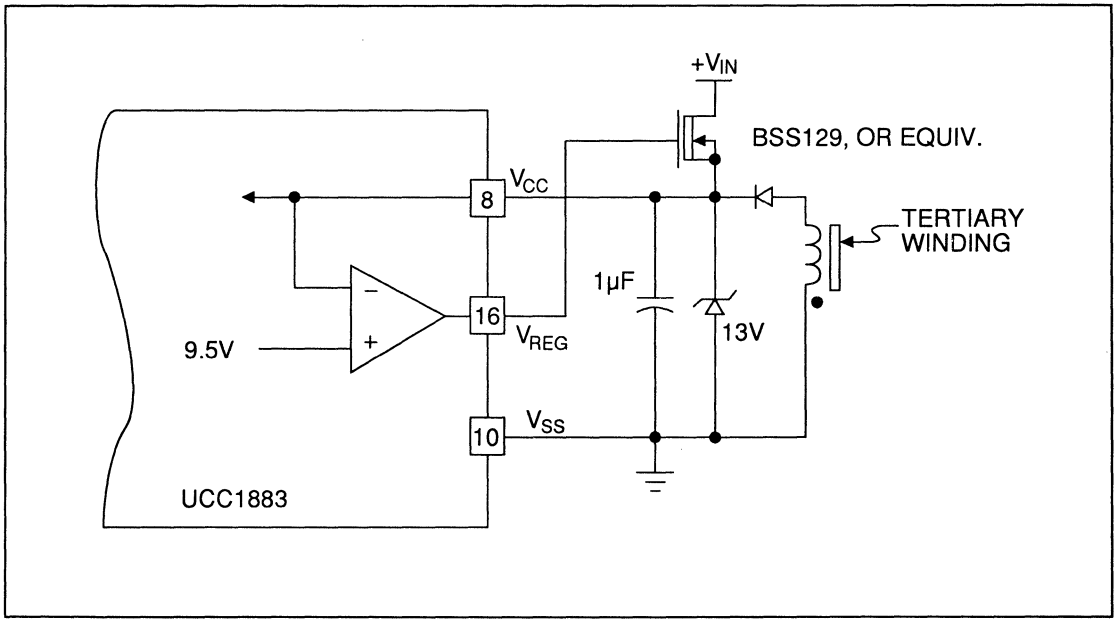


9.5V PRE-REGULATOR APPLICATION

FIGURE 6

of less than 2uA into the I_{MODE} pin is interpreted as a true RSMODE (restricted power mode) condition. These digital bits are transmitted across the isolation barrier and appear as outputs on the UCC1885 secondary-side regulation IC. Recall that no UCC1883 output will occur until a voltage greater than 1.2V is initially established on V_{LINE}.

V_{DD} LOGIC SUPPLY

The internal CMOS logic on the UCC1883 runs from a regulated 5V which is available externally at the V_{DD} pin. This pin should be bypassed to V_{SS} with a high quality ceramic capacitor having a value of at least 0.01uF. Values in excess of 10uF are not recommended.

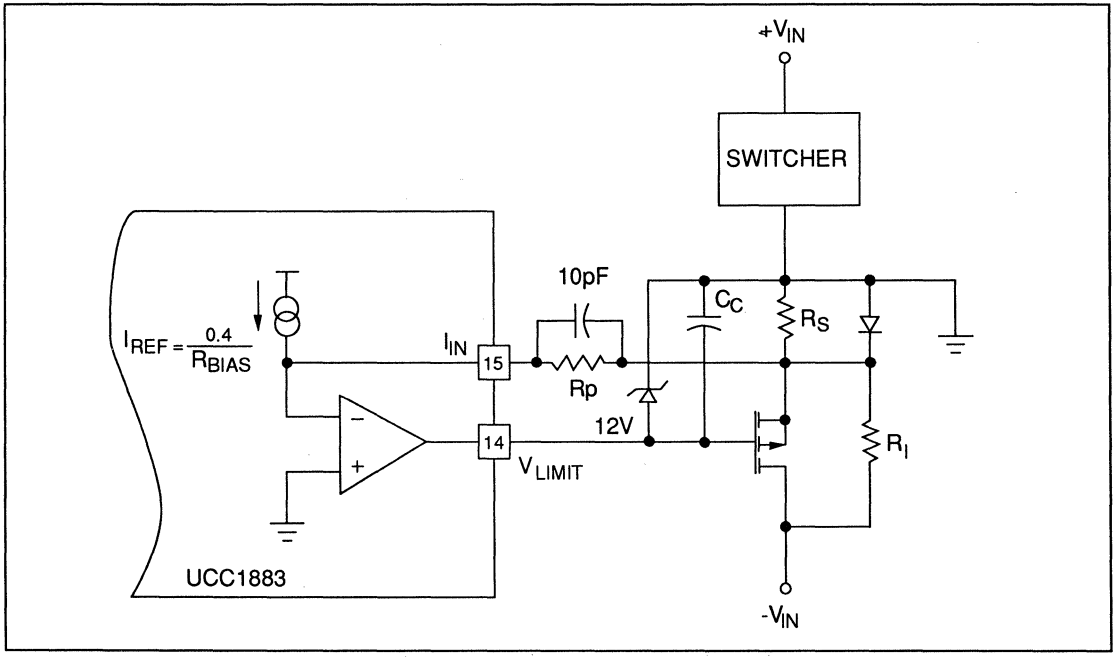
OSCILLATOR

A timing capacitor is connected between C_T and V_{SS} to program a natural oscillator frequency according to the equation

$$f_{OSC} = \frac{0.72}{C_T \cdot R_{BIAS}}$$

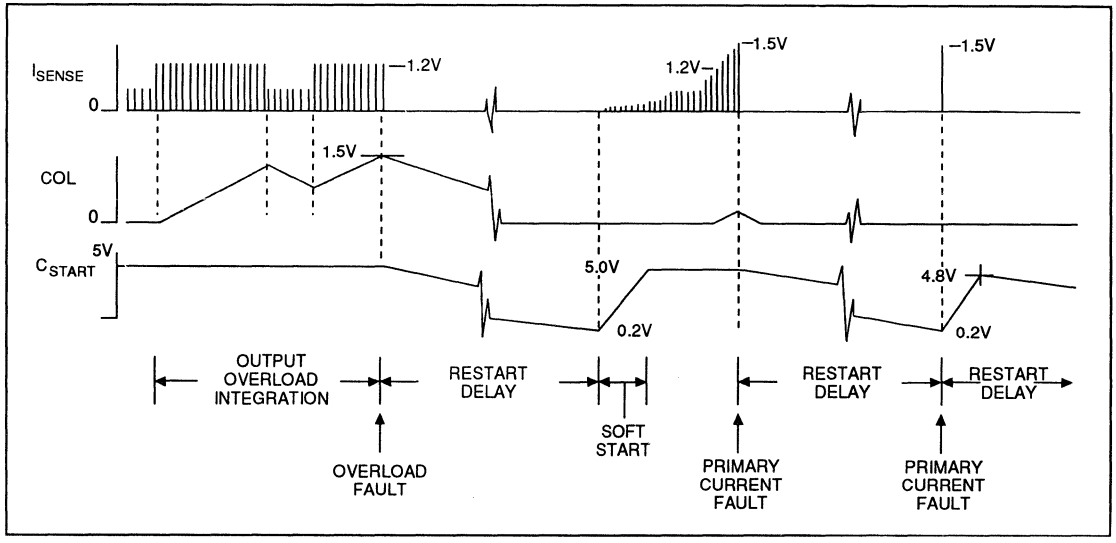
A ramp voltage running from V_{SS} to 2.5V is created on the C_T pin. This oscillator is automatically synchronized to the secondary-side clock frequency when data communication occurs across the isolation interface. Proper synchronization will only occur if the frequency of the secondary-side clock exceeds the natural frequency of the UCC1883 oscillator. A new oscillator cycle (ramp returns to V_{SS}) will be initiated on the rising edge of each positive isolation interface input pulse, with a corresponding decrease in ramp amplitude. The UCC1883 is designed so that the dV/dt established on its C_T pin will be nominally the same as that of the UCC1885 C_T pin, if equivalent components are used on the R_{BIAS} and C_T pins of both devices. However, the natural frequency of the UCC1883 oscillator will automatically be lower, to allow synchronization. Proper C_T ramp slope is important to the UCC1883, because it uses this information, along with the pulses received over the isolation interface, to reconstruct the analog output of the UCC1885 voltage error amplifier. This reconstructed voltage is in turn used to control the peak current mode PWM. The ratio of the slope of the UCC1883 timing ramp to the UCC1885 timing ramp sets the gain applied by the UCC1883 to the UCC1885 error amplifier output.

Other variations of the UCC1883 implementing voltage mode control, duty cycles greater than 50%, or faster natural oscillator frequencies may be available. Contact the factory for further information.

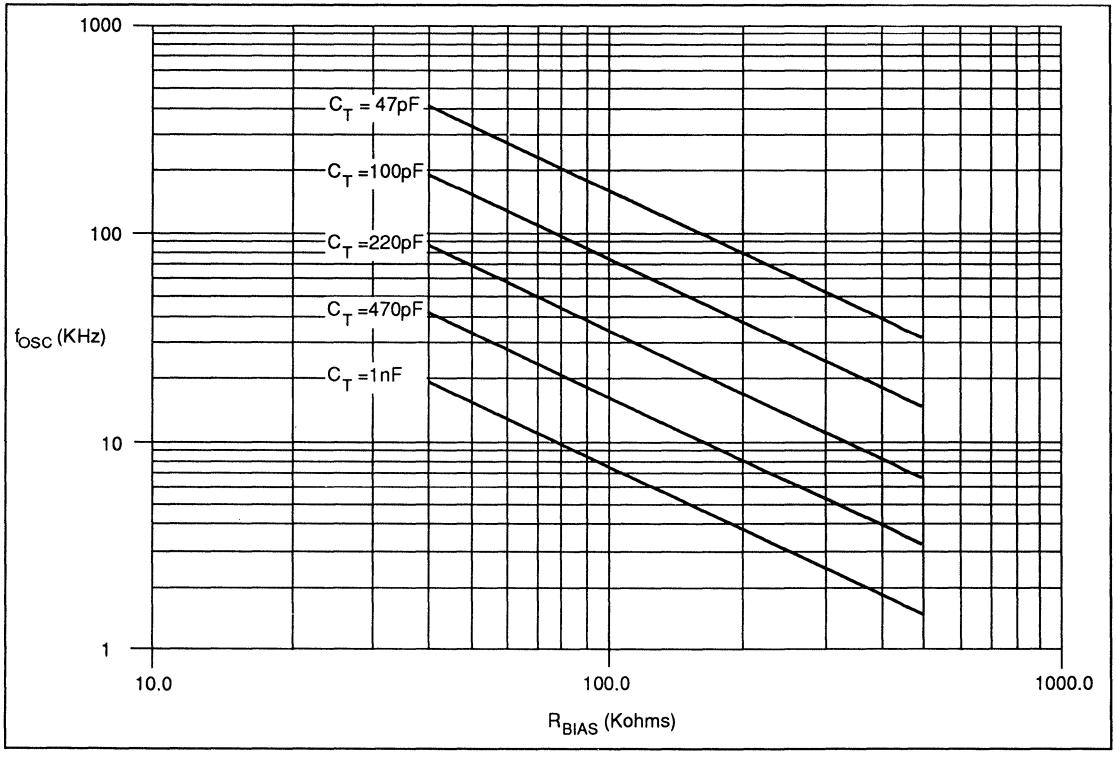


INPUT CURRENT LIMIT APPLICATION

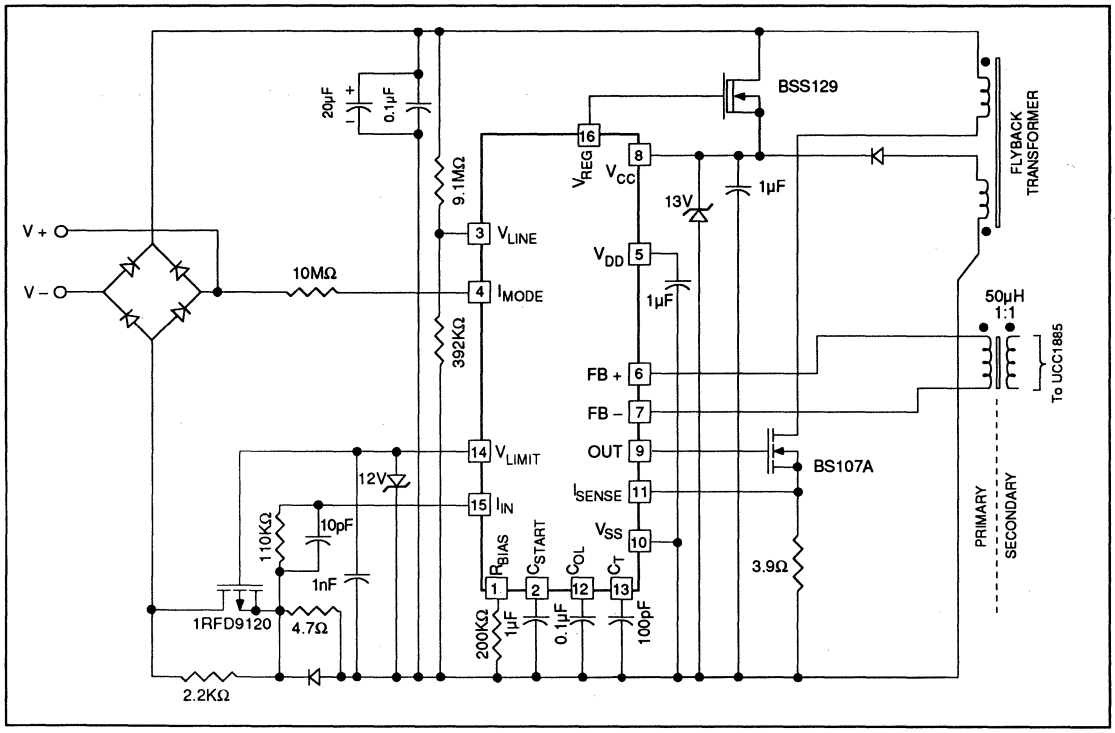
FIGURE 7



FAULT WAVEFORMS
FIGURE 8



OSCILLATOR FREQUENCY VERSUS R_{BIAS}
FIGURE 9



TYPICAL APPLICATION CIRCUIT
FIGURE 10

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL 603-424-2410 • FAX 603-424-3460

Micropower Secondary Regulation IC

ISDN I.430 RELATED FEATURES

- Secondary-Side Voltage Sense for Improved Regulation
- Restricted Mode Status Output
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode

GENERAL FEATURES

- Wide Supply Voltage Range
- Precision 2.0V Reference
- Low Offset, High Gain Error Amplifier
- Temperature Stable Oscillator
- Logic Level Oscillator Synchronization
- Low Line Status Output
- Under Voltage Lockout
- Programmable Secondary-Side Soft Start
- 5V Vdd Logic Supply Regulator

DESCRIPTION

The UCC1885 supplies the necessary functions to implement a fully isolated, ISDN compatible SMPS meeting the guidelines of CCITT recommendation I.430, when used in conjunction with the UCC1883 primary-side PWM controller. The UCC1885 secondary-side regulation IC provides improved regulation by allowing direct sensing of the output voltage on the secondary side of the DC/DC converter. The UCC1885 contains a precision system reference and a complete error amplifier. The output of the amplifier serves as the PWM control voltage and is provided to the primary-side via an isolation pulse transformer. The UCC1885 also sends synchronization information to the primary-side with this transformer. Under voltage lockout circuitry operates in combination with the user programmable soft start function to prevent transmission of data across the isolation barrier until adequate secondary-side operating conditions are established.

ISDN specific features allow the UCC1883/UCC1885 combination to be compatible with CCITT recommendation I.430. The UCC1885 receives two digital bits of status information from the UCC1883 via the isolation pulse transformer. These bits, which indicate restricted power mode and low input line voltage, are output on the secondary-side at CMOS logic levels. Precision programming of the quiescent current used by the UCC1885 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1885 is fabricated in Unitrode's 3µm BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1885.

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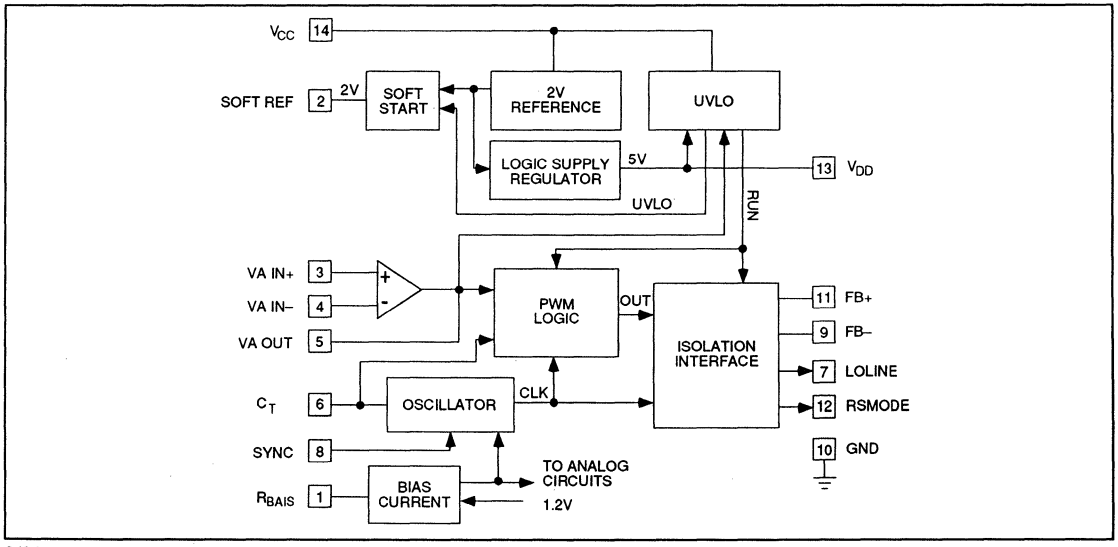
BLOCK DIAGRAM



3/93

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC}) 18V
Maximum V_{CC} Slew Rate 3V/mS
Digital Supply Voltage (V_{DD}) 7V
Maximum Voltage, All Signal Pins ..... V_{DD} + 0.3V to 7V
Minimum Voltage, All Pins ..... – 0.3V
Maximum DC Current, Any Pin, Source or Sink 100mA
Maximum Peak Current, Any Pin, Source or Sink 500mA
Total Package Dissipation (N package) 1W
Total Package Dissipation (D package) 800mW
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

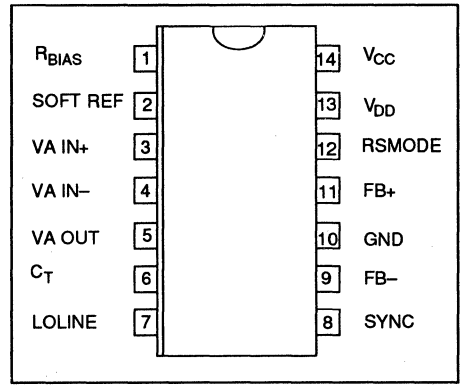
Note 1: All voltages expressed with respect to pin 10, currents are positive into the specified terminal.

Note 2: All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified, with total package power dissipation at or below specified limits.

Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-14, J or N Package, SOIC-14, D-Package



Pin Number	Pin Name	Pin Type	Function
1	R_{BIAS}	Analog Program	Quiescent Bias Current Set
2	SOFTREF	Analog Program & Output	Soft Start Timing Set and 2.0V Reference Output
3	VA IN +	Analog Input	Voltage Error Amplifier Non-Inverting Input
4	VA IN –	Analog Input	Voltage Error Amplifier Inverting Input
5	VA OUT	Analog Output	Voltage Error Amplifier Output
6	C_T	Analog Program	Oscillator Frequency Set
7	LOLINE	Digital Output	Low Primary-Side Line Voltage Status Bit (High = True)
8	SYNC	Digital Input	Oscillator SYNC (Positive-Edge Triggered)
9	FB –	Digital I/O	Differential Feedback Communication Signal (–)
10	GND	Supply Return	System Ground
11	FB +	Digital I/O	Differential Feedback Communication Signal (+)
12	RSMODE	Digital Output	CCITT Restricted Power Mode Status Bit (High = True)
13	V_{DD}	Logic Supply	5.0V Internal Regulator Output or Logic Supply Input
14	V_{CC}	Power Supply	Analog Power Supply Input

ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A -55°C to +125°C for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885 $V_{CC} = V_{DD} = 5V$, SYNC = OV, R_{BIAS} = 200Kohms, Ct = 100pF, and $T_J = T_A(min)$ to $T_A(max)$

UCC1885
UCC2885
UCC3885

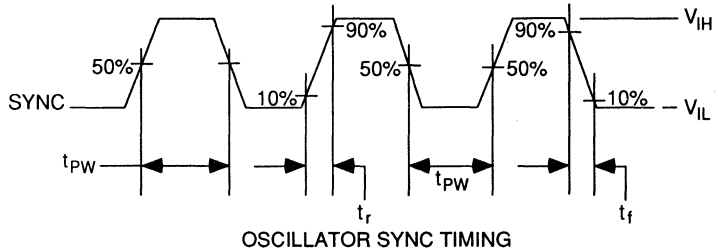
PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
UVLO Section					
V_{CC} Start Threshold	$V_{DD} = V_{CC}$	2.4	2.7	3.0	V
V_{CC} Threshold Hysteresis	$V_{DD} = V_{CC}$	260	400	600	mV
V_{DD} Start Threshold	$V_{DD} < V_{CC}$	2.0	2.4	2.9	V
VA OUT Run Threshold	VA OUT = VA IN(–)	1.0	1.15	1.3	V
Reference Section					
Reference Voltage	Tj = 25°C, Rload > 50Mohm	1.98	2	2.02	V
Line Regulation	3V < V_{CC} < 16.5V	–	2	10	mV
Load Regulation	–500nA < Iout < 500nA	–	12	35	mV
Total Reference Variation	Initial + Line + Temperature Rload > 50Mohm	1.96	–	2.04	V
Soft Start Current	SOFTREF = 0V	4	10	16	uA
External Override Threshold		–	–	2.45	V
Input Bias Current	SOFTREF = 5V	–	–	50	nA
User Bias Section					
R_{BIAS} Voltage	Tj = 25°C	1.17	1.2	1.23	V
R_{BIAS} Pin Line Regulation	3V < Vcc < 16.5V	–	8	30	mV
Total R_{BIAS} Pin Variation	Initial + Line + Temperature	1.15	–	1.25	V
Error Amplifier Section					
Input Common Mode Range	VA OUT = 1V	1	–	4.5	V
Input Offset Voltage	VA IN(+) = 2V, VA OUT = 1V	– 8	–	8	mV
Input Bias Current	VA IN(+) = 2V, VA OUT = 1V	-100	–	100	nA
VA OUT Low Level	Vdm = –10mV, Iout = 700uA	–	0.05	0.15	V
VA OUT High Level	R_{BIAS} = 200K, Vdm = 10mV, Iout = – 50uA	2.0	2.6	–	V
	R_{BIAS} = 39.2K, Vdm = 10mV, Iout = – 250uA	2.0	2.7	–	V
VA OUT Short Circuit Current	VA OUT = 0V, R_{BIAS} = 39.2 Kohms	– 0.4	– 1	– 5	mA
Open Loop Voltage Gain	Vcm = 2V, 0.1 < VA OUT = < 2.0V R_{BIAS} = 39.2 Kohms	80	110	–	dB
DC PSRR	Vcm = 2V, 0.1 < VA OUT = 1V R_{BIAS} = 39.2K, 3V < Vcc < 16.5V	70	110	–	dB
DC CMRR	VA OUT = 1V, R_{BIAS} = 39.2K 1V < Vcm < 4V	70	100	–	dB
Unity Gain Bandwidth	R_{BIAS} = 200 Kohms, Cout = 25pF (Note 1)	375	500	–	KHz
	R_{BIAS} = 39.2 Kohms, Cout = 25pF (Note 1)	1.6	2.2	–	MHz
Open Loop Output Impedance	R_{BIAS} = 200K (Note 1)	–	2.2	3.3	Kohms
	R_{BIAS} = 39.2K (Note 1)		450	675	ohms
VA OUT Slew Rate	R_{BIAS} = 200K, Cout = 25pF (Note 1)	140	250	–	mV/us
	R_{BIAS} = 39.2K, Cout = 25pF (Note 1)	0.7	1.25	–	V/us
Oscillator Section					
Initial Accuracy	T_J = 25°C	42	48	56	KHz
Voltage Stability	3V < $V_{CC} = V_{DD}$ < 7V	–	1	3	%
Total Oscillator Variation	Inital + Line + Temperature	41.5	–	58	KHz
C_T Ramp Amplitude		1.65	1.8	1.9	V
SYNC Input Low Voltage		–	–	1.5	V
SYNC Input High Voltage		3.5	–	–	V

5

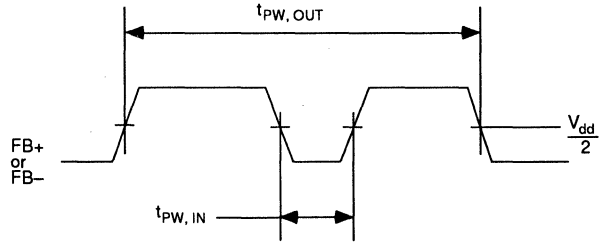
ELECTRICAL CHARACTERISTICS : Unless otherwise noted, all specifications apply for T_A -55°C to +125°C for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885 $V_{CC} = V_{DD} = 5V$, SYNC = OV, R_{BIAS} = 200Kohms, Ct = 100pF, and $T_J = T_A(min)$ to $T_A(max)$ UCC1885 UCC2885 UCC3885

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Oscillator Section (Continued)					
Maximum SYNC Rise, Fall Time	(See Figure 1 and Note 1)	500	–	–	nS
Minimum SYNC Pulse Width	(See Figure 1 and Note 1)	10	15	nS	
Isolation Interface Section					
FB Output High Voltage	Rload = 500 ohms	4.0	4.5	–	V
FB Output Low Voltage	Rload = 50 ohms to 5V	–	0.5	0.85	V
FB Output Pulse Width	R_{BIAS} = 200 Kohms (See Figure 2)	200	300	450	ns
	R_{BIAS} = 39.2 Kohms (See Figure 2)	–	100	–	ns
FB Output PW Matching		–	15	–	ns
Minimum FB Input Pulse Width	(See Figure 2 and Note 1)	–	10	–	ns
Digital Status Output High	LOLINE, RSMODE, Iout = – 200uA	4.85	4.95	–	V
Digital Status Output Low	LOLINE, RSMODE, Iout = 800µA	–	0.3	0.45	V
V_{DD} Regulator					
V_{DD} Output Voltage	$V_{DD} < V_{CC}$, No External Load	4.75	5	5.25	V
V_{DD} Line Regulator	$7V < V_{CC} < 16.5V$	–	10	50	mV
V_{DD} Load Regulation	– 3mA < Iout < 0mA	–	100	250	mV
V_{DD} Regulator Dropout	No External Load	–	0.9	1.7	V
V_{DD} Short Circuit Current	V_{DD} = 0V	8	30	70	mA
Power Supplies					
DC Supply Current		–	100	150	uA
Cpd	(Note 2)	–	150	–	pF

Notes: 1. This parameter not 100% tested in production, but guaranteed by design.
2. Total power dissipation will be determined by associated isolation pulse transformer characteristics. A pulse transformer with a low loss core and at least 50µH of magnetizing inductance is strongly recommended.



OSCILLATOR SYNC TIMING
FIGURE 1



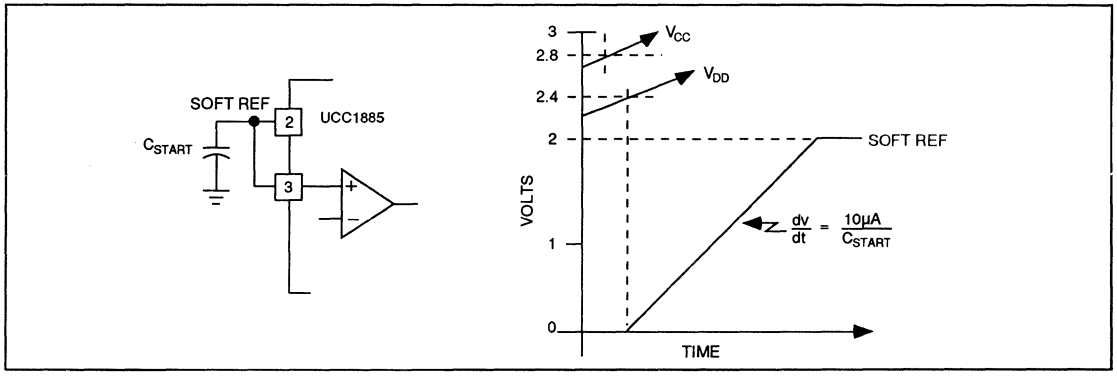
FEEDBACK I/0 TIMING
FIGURE 2

APPLICATIONS INFORMATION

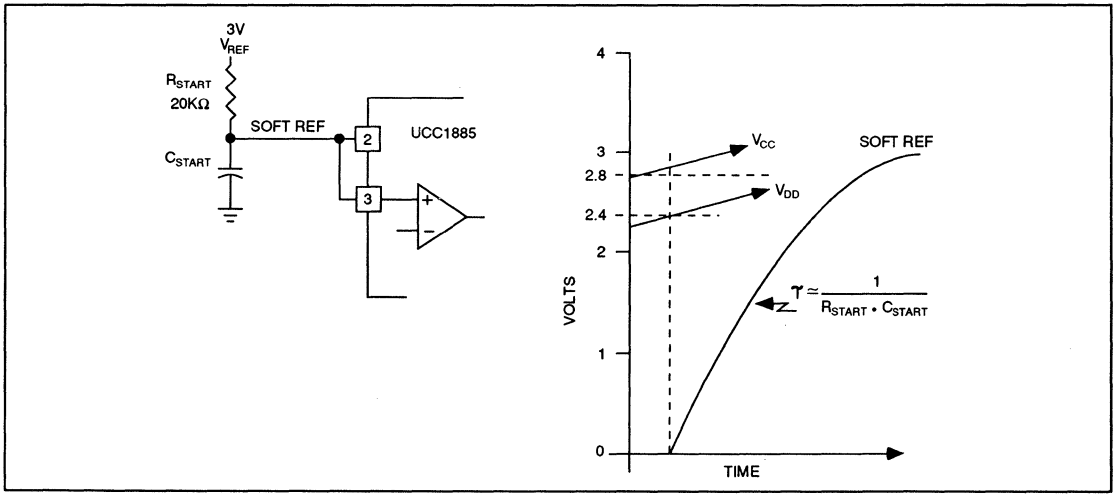
UNDER VOLTAGE LOCKOUT

When power is first applied to the UCC1885, SOFTREF is held at ground until V_{CC} exceeds 2.8V and V_{DD} exceeds 2.4V. Once adequate operating voltages have been established, SOFTREF is released and allowed to charge from an internal 10uA current source. A capacitor from this pin to ground may be used to continue an output soft start after the UCC1885 takes control of the SMPS with feedback communication to the UCC1883. In this case, the dV/dt established on SOFTREF must exceed the dV/dt established on the regulated output by the blind soft start being provided by the UCC1883. Normally the SOFTREF pin will charge to 2.0V, the value of the internal precision reference. Once the internal reference voltage is reached, the current source is disabled and the SOFTREF pin maintains an output impedance of 30KΩ, which, acting with any soft start capacitance, will then form a single-pole reference noise filter.

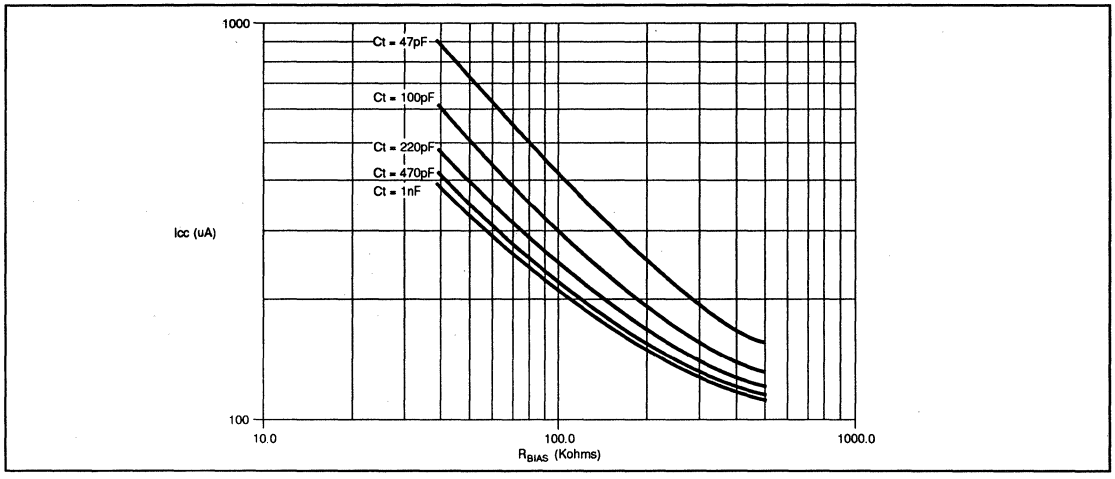
If the use of an external reference (V_{REF} > 2.5V) is desired, the soft start function can still be maintained on SOFTREF. In this case, the user must also supply a soft start resistor between the external reference and SOFTREF. The value of this resistor should be chosen such that the current sourced into the SOFTREF pin when the voltage reaches 2.0V is at least 20uA, which will allow the UCC1885 to sense the presence of an external reference. Once the external reference is sensed, the internal reference is disconnected from SOFTREF, making it high impedance and eliminating any DC error across the soft start resistor. The minimum value of the soft start resistor



SOFT START WITH INTERNAL REFERENCE
FIGURE 3



SOFT START WITH EXTERNAL REFERENCE
FIGURE 4



AVERAGE DC CURRENT VERSUS R_{BIAS} (Not including Pulse Transformer Loses)

FIGURE 5

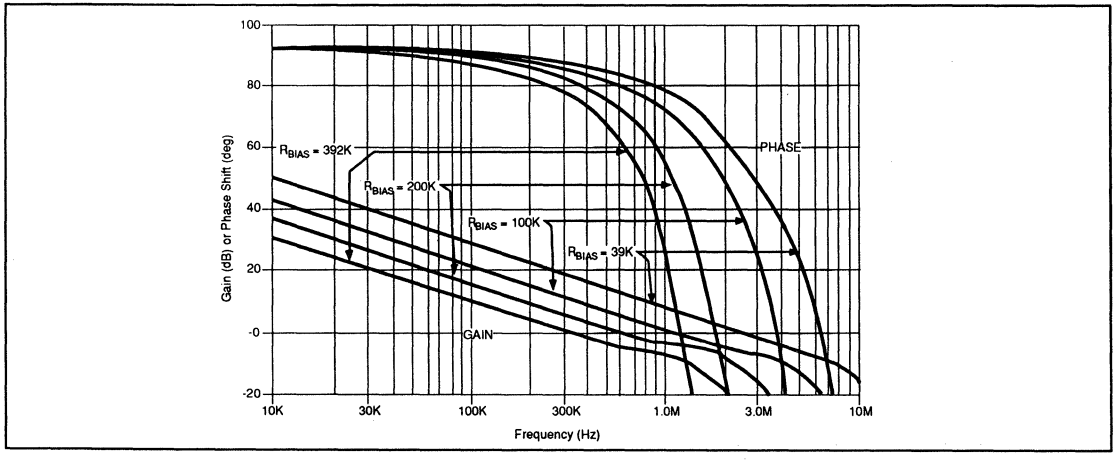
should be limited to allow SOFTREF to pull low during UVLO. The output impedance of SOFTREF during this phase of operation is about 300 ohms to ground.

The final portion of the UCC1885 UVLO sequence occurs when the output of the error amplifier increases above 1.15V. Normally this will not occur until the system reference has charged to some intermediate value. Assuming that adequate operating voltage has also been established, then the isolation interface on the UCC1885 begins transmitting output pulse width control information to the UCC1883 via an isolation pulse transformer. The 1.15V required on the output of the error amplifier guarantees that the UCC1885 will initially begin transmitting information to the primary-side PWM controller which keeps energy flowing to the secondary allowing the control loop to come into regulation. Once the isolation interface is enabled, the UVLO circuitry ignores all voltages appearing on the output of the error amplifier.

USER BIAS PROGRAMMING

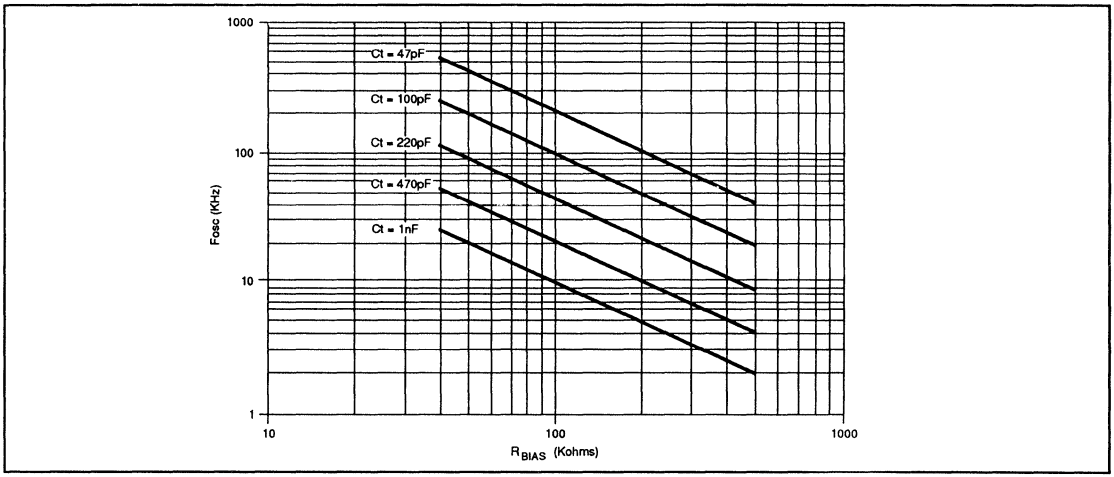
The R_{BIAS} pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1885. A resistor from this pin to ground establishes a user bias current according to the equation

$$I_{BIAS} = \frac{1.2V}{R_{BIAS}}$$



ERROR AMPLIFIER GBW VERSUS R_{BIAS}

FIGURE 6



OSCILLATOR FREQUENCY VERSUS R_{BIAS}
FIGURE 7

Recommended range for R_{BIAS} is 39.2 KΩ to 392 KΩ. Internal circuits on the UCC1885 consume a total quiescent current of 9 • I_{BIAS}, plus some fixed currents amounting to about 50uA at room temperature. Additional dynamic current consumption may be calculated with C_{PD} (see specifications), given a certain oscillator frequency f_{OSC}, from the equation

$$I_{DYNAMIC} = C_{PD} \cdot V_{DD} \cdot f_{OSC}$$

Also note from the specifications that the voltage on R_{BIAS} is well controlled and thus may be effectively used as another reference voltage in the system.

V_{DD} LOGIC SUPPLY

The internal CMOS logic on the UCC1885 requires a supply limited to 7V. If the value of V_{CC} is anticipated to be below 7V, then V_{DD} should be wired directly to V_{CC} and bypassed with at least 0.01uF. If V_{CC} exceeds 7V, the UCC1885 provides an internal 5V regulator to the V_{DD} pin for running the onboard CMOS logic. At these higher V_{CC} voltages, the V_{DD} pin should be disconnected and bypassed with at least 0.01uF. For this case of internal regulation, V_{DD} bypass capacitance should not exceed 10uF.

ERROR AMPLIFIER

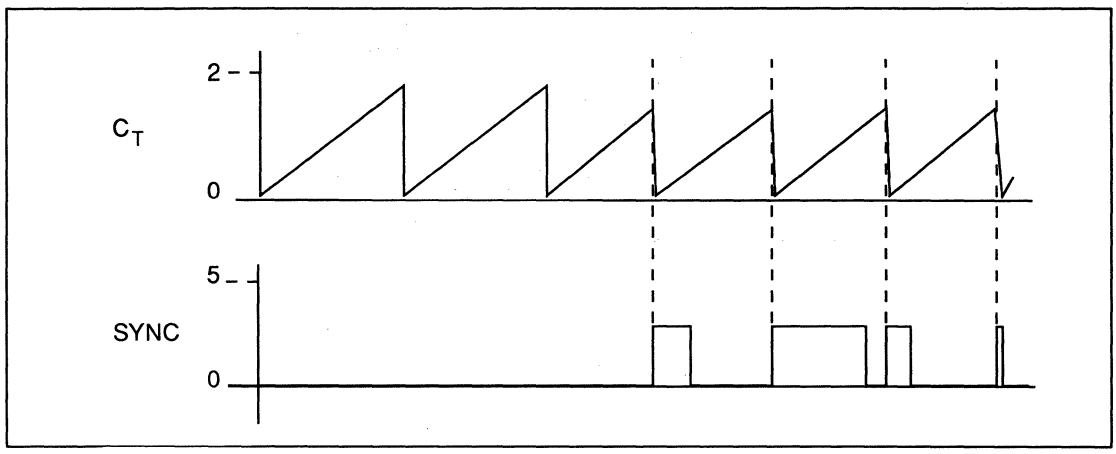
The UCC1885 error amplifier is intended to be the control amplifier for the voltage loop of the ISDN SMPS. It is a low offset, high gain design. Output swing is typically limited to a maximum of 2.7V. The GBW of the amplifier is controlled by the value of R_{BIAS} supplied by the user on pin 1. Input common mode range is between 1V and V_{CC} - 0.5V. If both inputs are beneath the common mode range during soft start, special circuitry on the UCC1885 guarantees VA out will be very near ground to insure proper startup.

OSCILLATOR

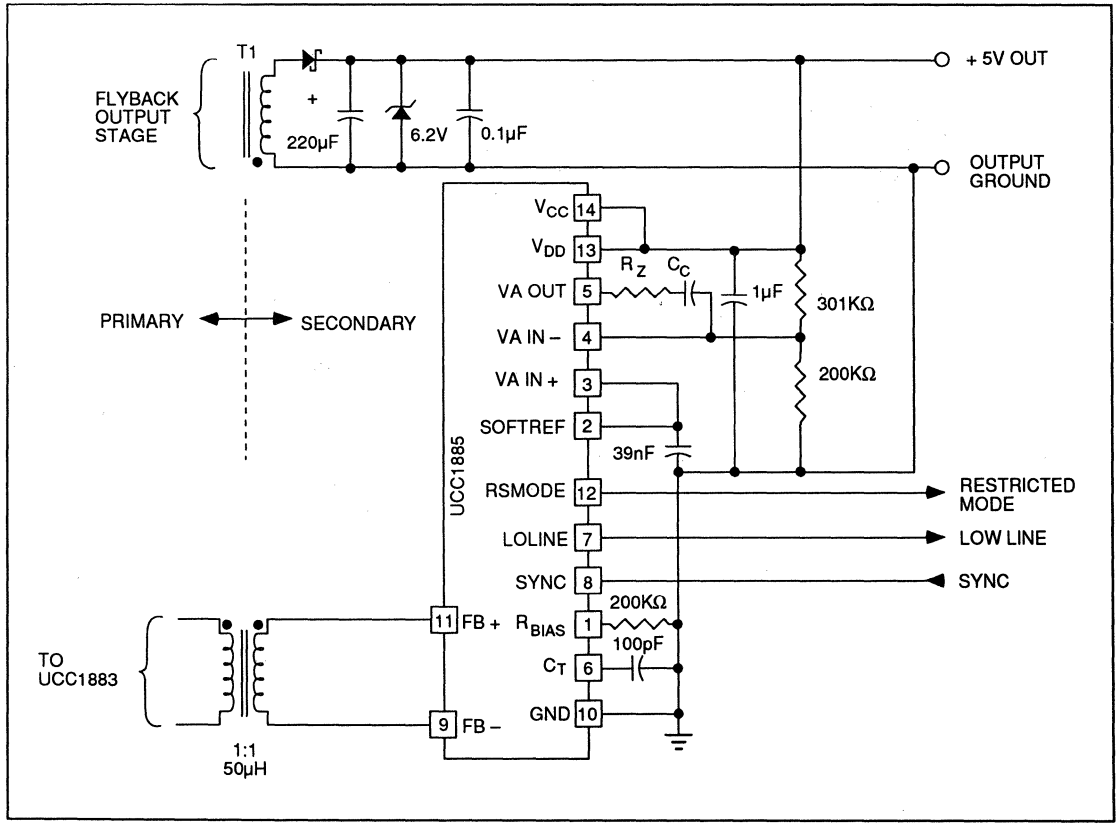
A timing capacitor is connected between C_T and ground to program a natural oscillator frequency according to the equation

$$f_{OSC} = \frac{1}{C_T \cdot R_{BIAS}}$$

A ramp voltage running from ground to 1.8V is created on the C_T pin. This oscillator may be synchronized to a system clock applied to SYNC. Proper synchronization will only occur if the frequency of the SYNC signal exceeds the natural frequency programmed into the oscillator. A new oscillator cycle (ramp returns to ground) will be initiated on each rising edge of SYNC, with a corresponding decrease in ramp amplitude. SYNC should be wired to ground if this feature is not used. The ramp amplitude represents the maximum value of error amplifier output voltage which may be passed over the isolation interface to the UCC1883. Thus a minimum synchronized ramp amplitude of 1.3V is recommended. The UCC1885 will accept a wide range of duty cycles on the SYNC pin, but rise and fall times of longer than 200ns are not recommended.



OSCILLATOR WAVEFORMS
FIGURE 8



TYPICAL APPLICATION
FIGURE 9

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

Indicates Application Note Available
See Section 9.

6

Intelligent Motion Circuits


INTEGRATED
CIRCUITS
UNITRODE

Product Selection Guide

INTELLIGENT CONTROLS AND MOTOR CONTROL DESIGNERS GUIDE

PERFORMANCE CHARACTERISTICS	UNITRODE PART NUMBER														
	L293	L293D	UC2950	UC3517	UC3625	UC3633	UC3634, 35	UC3637	UC1655	UC1657	UC1717/1717A	UC1720	UC1728	UC3770A/B	UC3174[C]
Linear				■						■					
PWM					■	■			■		■	■	■	■	■
Fixed off-time					■							■	■	■	■
Fixed Frequency						■			■		■				
Transconductance Ampl.				■	■	■			■	■	■				
Low Noise				■	■					■					
Number of Totem Pole Outputs	4	4	1	2	3				2	3	2	2			2
Over 0.5A Output	■	■	■	■	■					■	■	■	■	■	■
Includes Output Diodes		■	■		■							■			
Reversible Direction				■	■	■			■	■	■	■			■
Microstepping Capability				■					■		■	■			■
Hall Logic					■	■				■					
Full-Step/Half-Step Logic															
Phase-Lock Speed Control							■	■							
Four Quadrant Output						■					■				■
Current Sense Capability					■	■				■	■	■	■	■	■
Brake Function						■									
Tri-stable Outputs	■	■	■		■					■					
Thermal Protection	■	■	■	■	■	■				■	■	■	■	■	■
Undervoltage Lockout					■	■			■	■	■		■	■	
Driver Only: TTL Inputs	■	■	■												

Note C: Also includes 3175, 3176, 3177, 3178, 3173A

Product Selection Guide

INTELLIGENT CONTROLS AND MOTOR CONTROL DESIGNERS GUIDE (Cont'd)

PERFORMANCE CHARACTERISTICS	UNITRODE PART NUMBER														
	L293	L293D	UC2950	UC3517	UC3625	UC3633	UC3634, 35	UC3637	UC1655	UC1657	UC1717/1717A	UC1720	UC1728	UC3770A/B	UC3174[C]
APPLICATIONS[A]															
Unipolar Bilevel Stepper															
Bipolar Stepper	■	■	■	■					■		■				■
Three-Phase Brushless			■		■	■	■			■					
Two-Phase Brushless			■					■		■					
PWM Servo	■	■	■	■	■		■	■	■	■	■				■
Solenoid	■	■	■	■	■			■		■			■	■	
Relay	■	■	■	■	■			■		■			■	■	
Voice-Coil				■	■			■							■
STANDARD PACKAGE[B]															
16-Pin Batwing	■	■									■				■
16-Pin DIL							■	■							
18-Pin DIL									■						
20 Pin PLCC											■				■
24-Pin DIL															
28-Pin Power PLCC				■		■			■	■					■
28-Pin DIL						■								■	
5-Pin TO-220			■												
16-Pin Power Ceramic	■	■												■	
24-Pin Power Ceramic									■	■	■	■	■		
PHILLIPS STYLE PACKAGE (Power DIL)															
48QFP (Quad Flat PAC)															■
48QFP (Power)															■

Note A: See Application Section for more
Note B: Alternate Packaging Available
Note C: Also includes 3175, 3176, 3177, 3178, 3173A

Product Selection Guide

Intelligent Controls and Motor Control

CROSS APPLICATION CHART

NOTE: It is often possible — and advantageous — to fit into one application an IC that was originally designed for another. Here are a few hints:

UNITRODE PART#	BRUSH SERVOMOTOR	STEPPING MOTOR	MICRO-STEPPING	BRUSHLESS		VOICE COIL	SOLENOID
				1Ø	3Ø		
L293, 293D							
UC2950							
UC3173A, 4, 5,6,7,8							
UC3517							
UC3610,11,12							
UC3620,22,23							
UC3633,34							
UC1657							
UC3637							
UC3717,17A							
UC3770A,B							

Push-Pull Four Channel Driver

FEATURES

- Output Current 1A Per Channel (600mA for L293D)
- Peak Output Current 2A Per Channel (1.2A for L293D)
- Inhibit Facility
- High Noise Immunity
- Separate Logic Supply
- Over-Temperature Protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are packaged in 16-pin plastic and ceramic DIPs; both use the four center pins to conduct heat to the printed circuit boards. A 28-pin Power SOIC package is also available.

TRUTH TABLE

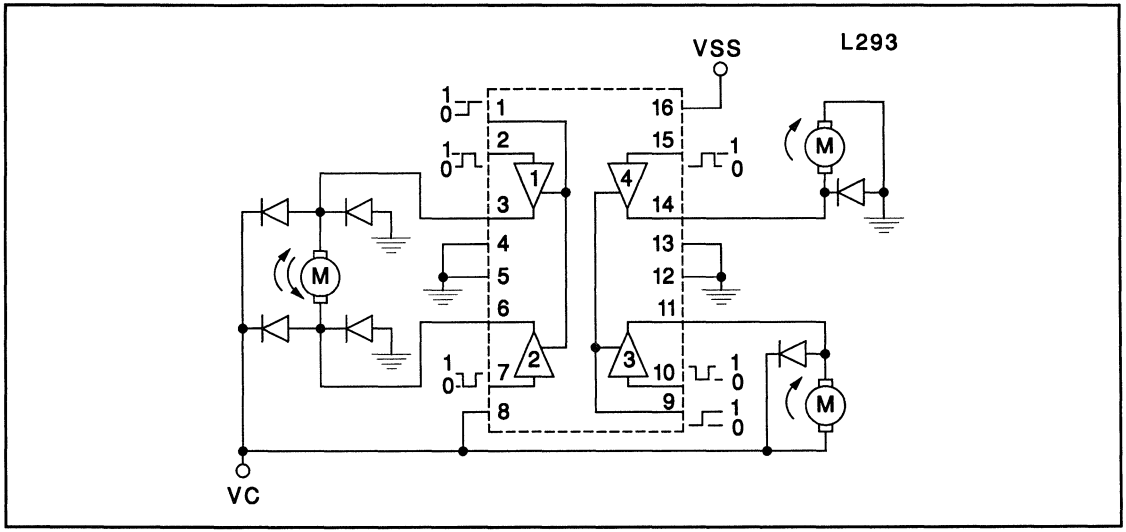
V_I (each channel)	V_{INH}*	V_O
H	H	H
L	H	L
H	L	X**
L	L	X**

**Relative to the considered channel*
***High output impedence*

ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, Vc 36V
Logic Supply Voltage, Vss 36V
Input Voltage, V_I 7V
Inhibit Voltage, V_{INH} 7V
Peak Output Current (Non-Repetitive), I_{OUT} (L293) 2A
I_{OUT} (L293D) 1.2A
Total Power Dissipation
at Tground-pins = 80°C, N pkg, (Note) 5W
Storage and Junction Temperature, Tstg, TJ ..... -40 to +150°C
Note:Consult packaging section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM

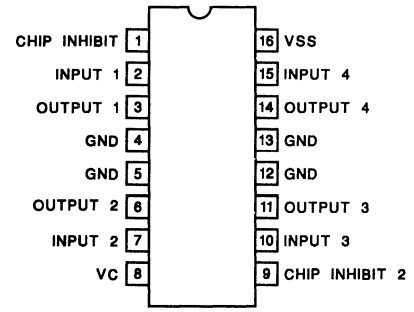


Note: Output diodes are internal in L293D.

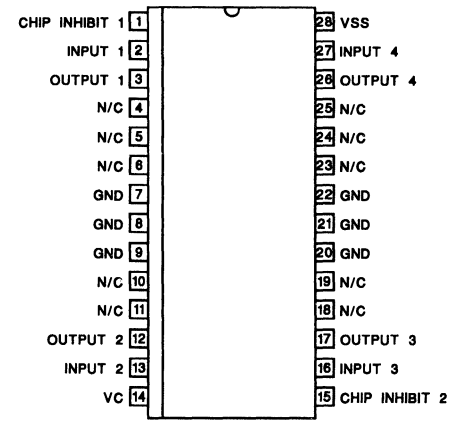
01/93

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



SOIC-28 (TOP VIEW)
J or N Package

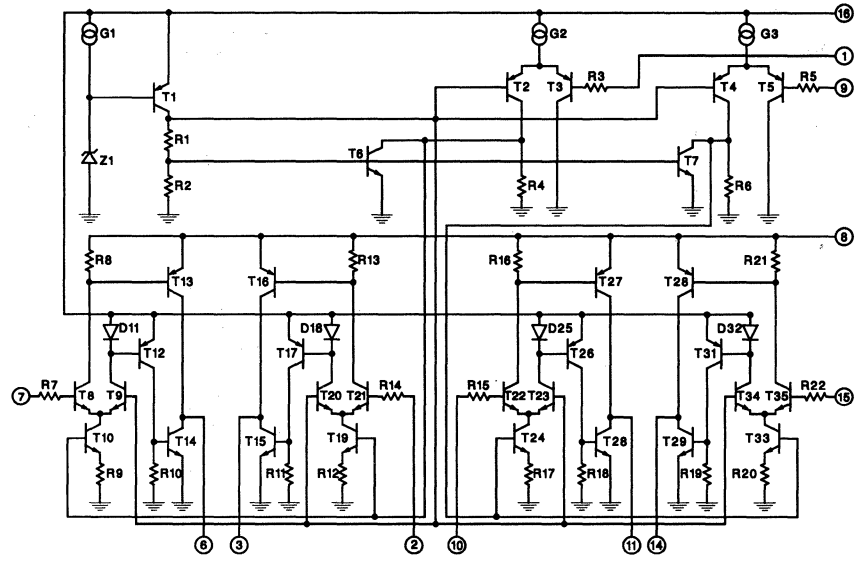


ELECTRICAL CHARACTISTICS: (For each channel, V_C = 24V, V_{SS} = 5V, T_{AMB} = 25°C, unless otherwise specified; $T_A = T_J$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_C				36	V
Logic Supply Voltage	V_{SS}		4.5		36	V
Collector Supply Current	I_C	V_I = L, I_O = 0, V_{INH} = H		2	6	mA
		V_I = H, I_O = 0, V_{INH} = H		16	24	mA
		V_{INH} = L			4	mA
Total Quiescent Logic Supply Current	I_{SS}	V_I = L, I_O = 0, V_{INH} = H		44	60	mA
		V_I = H, I_O = 0, V_{INH} = H		16	22	mA
		V_{INH} = L	-0.3	16	24	mA
Input Low Voltage	V_{IL}		2.3		1.5	V
Input High Voltage	V_{IH}	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		$V_{SS} \geq 7V$			7	V
Low Voltage Input Current	I_{IL}	V_I = 0V			-10	µA
High Voltage Input Current	I_{IH}	V_I = 4.5V		30	100	µA
Inhibit Low Voltage	$V_{INH, L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{INH, H}$	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		V_{SS} >7V	2.3		7	V
Low Voltage Inhibit Current	$V_{INH, L}$			-30	-100	µA
High Voltage Inhibit Current	$V_{INH, H}$				10	µA
Source Output Saturation Voltage	V_{CEsatH}	I_O = -1A (-0.6A for L293D)		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	I_O = 1A (0.6A for L293D)		1.2	1.8	V
Clamp Diode Forward Voltage (L293D only)	V_F	I_F = 0.6A		1.3		V
Rise Time	T_R	0.1 to 0.9 Vo (See Figure 1)		250		ns
Fall Time	T_F	0.9 to 0.1 Vo (See Figure 1)		250		ns
Turn-on Delay	T_{ON}	0. 5 V_I to 0.5 Vo (See Figure 1)		450		ns
Turn-off Delay	T_{OFF}	0. 5 V_I to 0.5 Vo (See Figure 1)		200		ns

6

SCHEMATIC DIAGRAM



APPLICATION INFORMATION

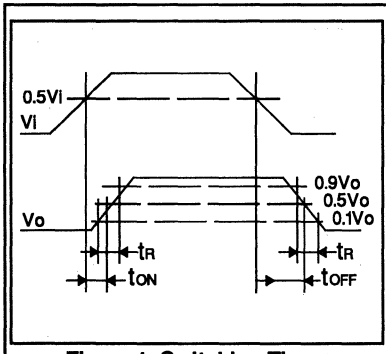


Figure 1: Switching Times

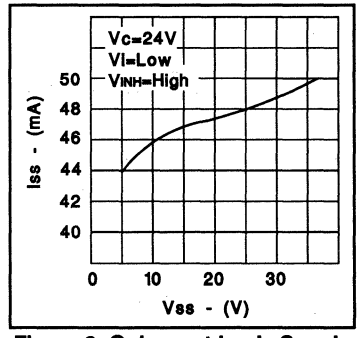


Figure 2: Quiescent Logic Supply Current vs Logic Supply Voltage

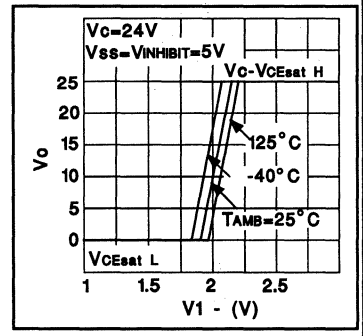


Figure 3: Output Voltage vs Input Voltage

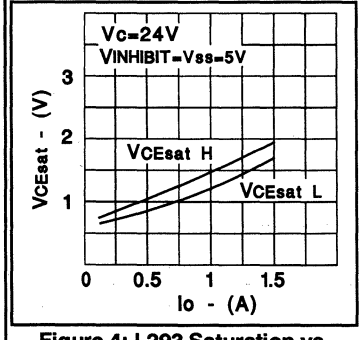


Figure 4: L293 Saturation vs Output Currrent

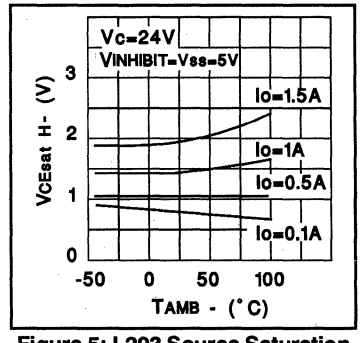


Figure 5: L293 Source Saturation vs Ambient Temperature

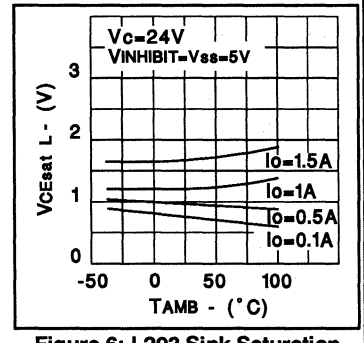


Figure 6: L293 Sink Saturation Voltage vs Ambient Temperature

NOTE: For L293D curves, multiply output current by 0.6.

APPLICATION INFORMATION (Cont.)

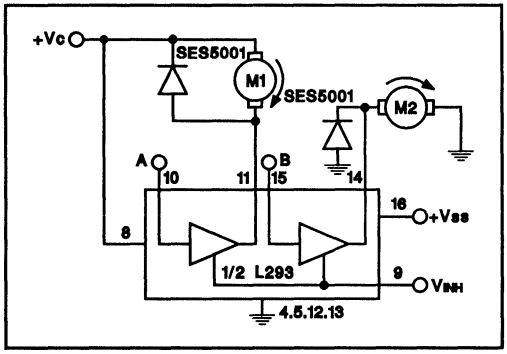


Figure 7: DC Motor Controls (with Connection to Ground and to Supply Voltage)

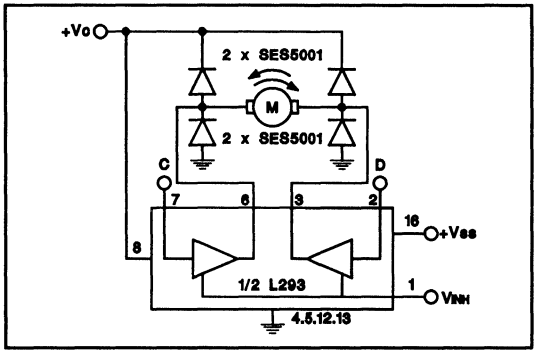


Figure 8: Bidirectional DC Motor Control

VINH	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't Care

INPUTS		FUNCTION
VINH = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
VINH = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't Care

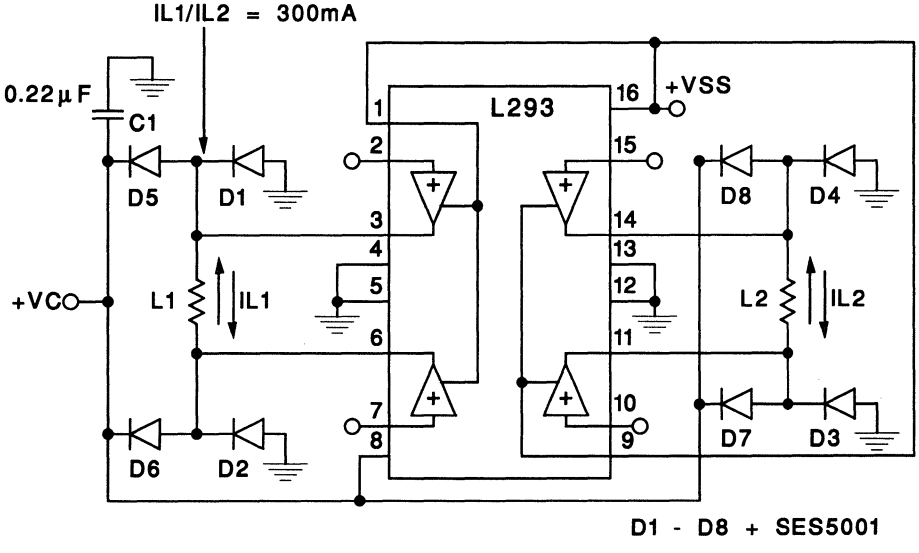


Figure 9: Bipolar Stepping Motor Control

MOUNTING INSTRUCTIONS

The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power Ptot and the θJA as a function of the side "l" of two equal square copper areas having a thickness of 35μ (see Figure 10). In addition, it is possible to use an external heatsink (see Figure 11).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

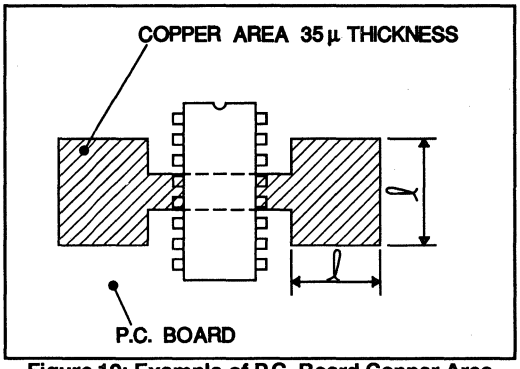


Figure 10: Example of P.C. Board Copper Area which is used as Heatsink

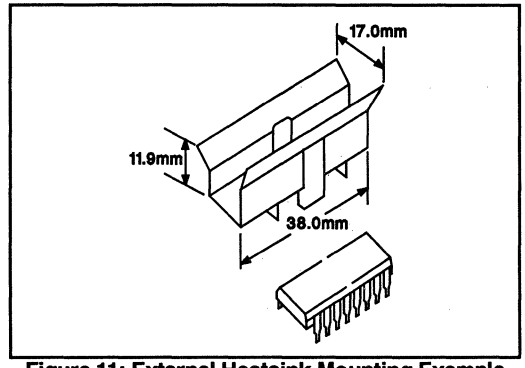


Figure 11: External Heatsink Mounting Example (θJA = 25°C/W)

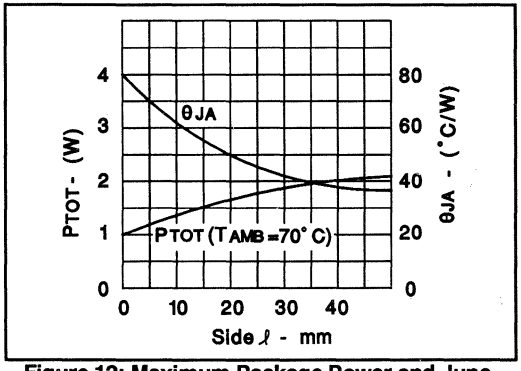


Figure 12: Maximum Package Power and Junction to Ambient Thermal Resistance

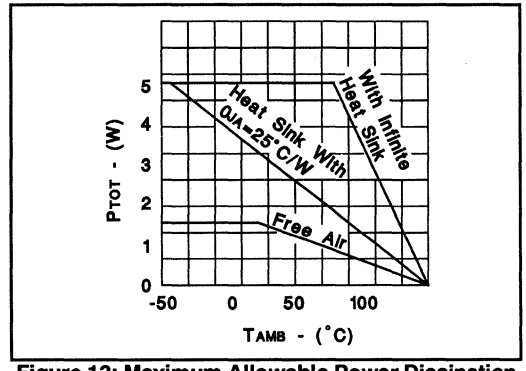


Figure 13: Maximum Allowable Power Dissipation vs Ambient Temperature

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L298

Dual Full-Bridge Power Driver

FEATURES

- Operating Supply Voltage up to 46V
- Total Saturation Voltage 3.4V max at 1A
- Overtemperature Protected
- Operates in Switched and L/R Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs

DESCRIPTION

The L298 is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 2A continuously.

Logic inputs to the L298 have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298 input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are separately available for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298 ideal for systems that require low standby current, such as portable or battery-operated equipment.

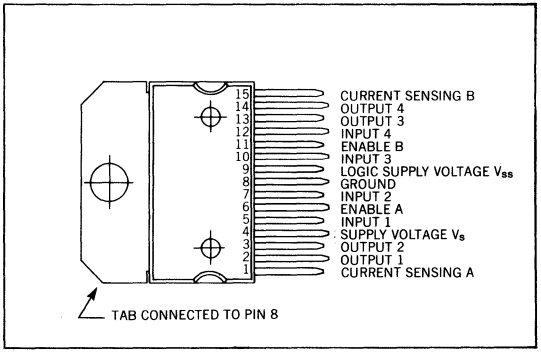
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_s 50V
Logic Supply Voltage, V_{ss} 7V
Input and Inhibit Voltage, V_i, $V_{inhibit}$ ..... -0.3V to +7V
Peak Output Current (each channel), I_o
Non-Repetitive (t = 100μs) 3A
Repetitive (80% on - 20% off; t_{ON} = 10ms) 2.5A
DC Operation 2A
Sensing Voltage, V_{sens} ..... -1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot} 25W
Storage and Junction Temperature, T_{stg}, T_j ..... -40°C to +150°C

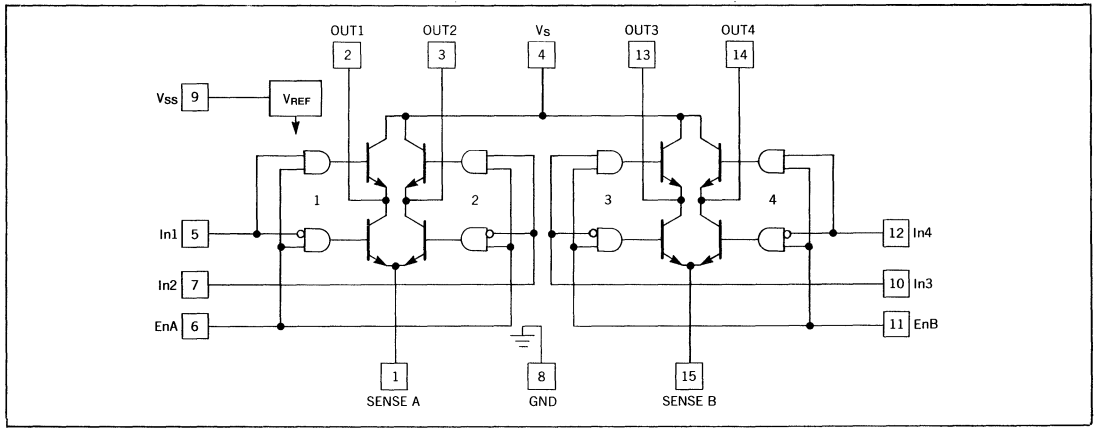
THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j\text{-}case}$ ..... 3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j\text{-}amb}$ ..... 35°C/W max.

CONNECTION DIAGRAM



BLOCK DIAGRAM



6

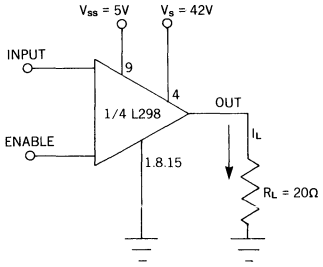
ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C) T_A=T_J

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operating Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	$V_{inh.}$ = H V_i = L		3	7	mA
	I_L = 0 V_i = H		15	20	
	$V_{inh.}$ = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	$V_{inh.}$ = H V_i = L		5	10	mA
	I_L = 0 V_i = H		1.5	3	
	$V_{inh.}$ = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\ L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\ H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ H}$	V_i = H		30	100	
Inhibit Low Voltage (Pins 6, 11), $V_{inh.\ L}$		-0.3		1.5	V
Inhibit High Voltage (Pins 6, 11), $V_{inh.\ H}$		2.3		7	
Low Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ L}$	$V_{inh.}$ = L			-10	μA
High Voltage Inhibit Current (Pins 6, 11), $I_{inh.\ H}$	$V_{inh.}$ = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\ sat(H)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.8	2.8	
Sink Saturation Voltage, $V_{CE\ sat(L)}$	I_L = 1A		1.2	1.8	V
	I_L = 2A		1.7	2.6	
Total Drop, $V_{CE\ sat}$	I_L = 1A			3.4	V
	I_L = 2A			5.2	
Sensing Voltage (Pins 1, 15), V_{sens}		-1 (1)		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L (2)		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L (2)		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L (2)		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L (2)		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L (3)		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L (3)		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L (3)		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L (3)		0.2		μs
Commutation Frequency, f_c	I_L = 2A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

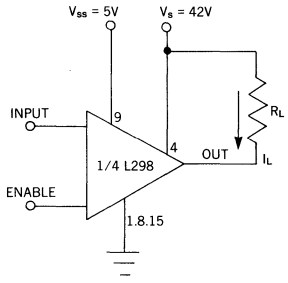
SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 2. Switching Times Test Circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input or Enable Chopper.

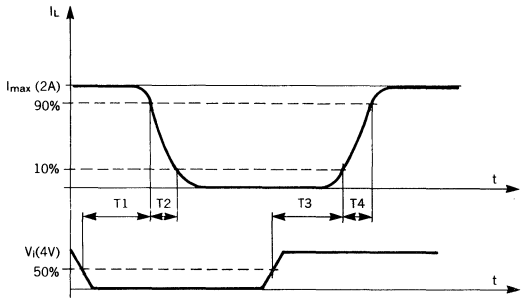
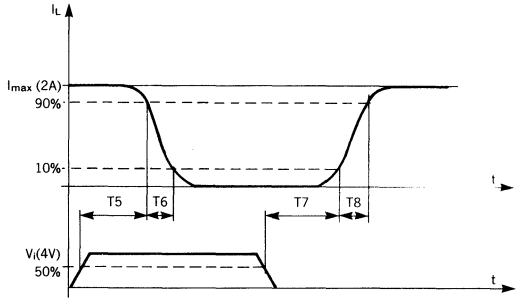


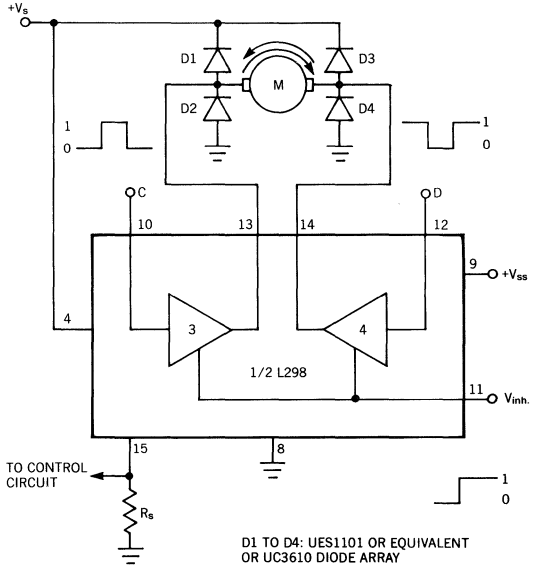
Figure 2a. Sink Current Delay Times vs. Input or Enable Chopper.



6

APPLICATIONS

Figure 3. Bi-Directional DC Motor Control.

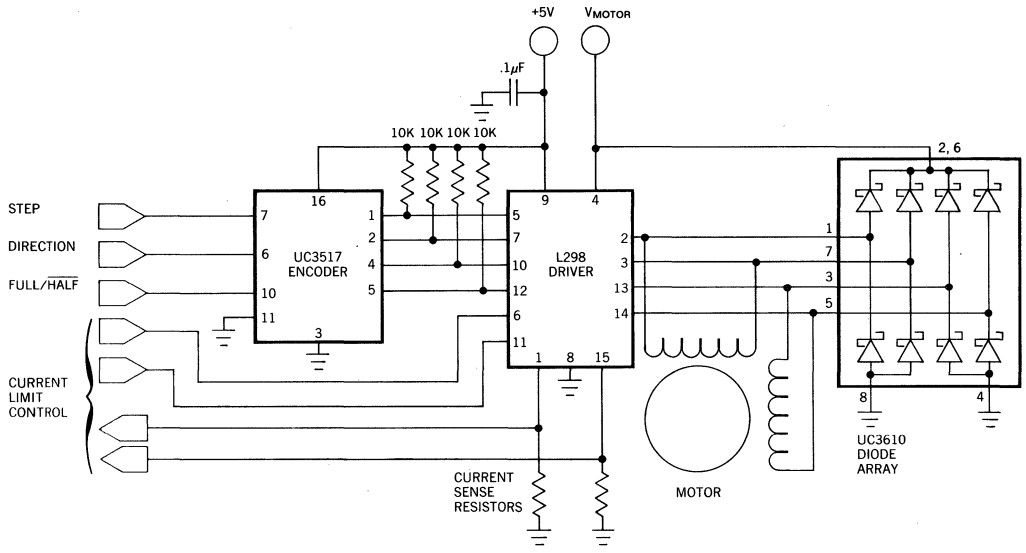


D1 TO D4: UES1101 OR EQUIVALENT
OR UC3610 DIODE ARRAY

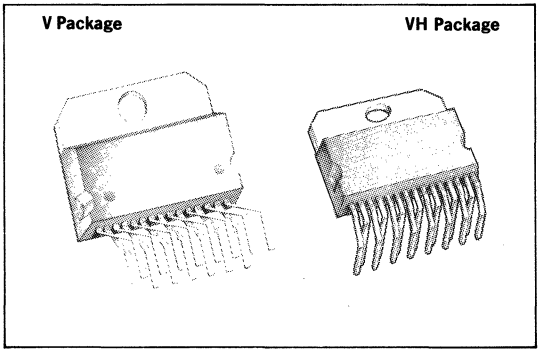
	INPUTS	FUNCTION
$V_{inh.}$ = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
$V_{inh.}$ = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

Figure 4. Bipolar Step Motor Driver.



STANDARD PACKAGES



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INTEGRATED CIRCUITS

UNITRODE

Dual Full-Bridge Power Driver

FEATURES

- Operating Supply Voltage up to 46V
- Overtemperature Protected
- Operates in Switched and L/R Current Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs
- Internal Diodes Minimize Parts Count

DESCRIPTION

The L298D is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 1A continuously.

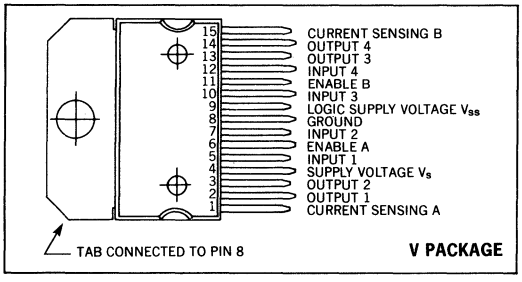
The L298D features internal diodes for clamping output excursions when driving inductive loads, such as motors and transmission lines. For most applications, these diodes can completely replace all external clamp diodes. In certain cases, however, additional output catch diodes may be valuable for reducing recovery time or power dissipation.

Logic inputs to the L298D have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298D input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

The emitters of the low-side power drivers are available in pairs for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298D ideal for systems that require low standby current, such as portable or battery-operated equipment.

CONNECTION DIAGRAM (TOP VIEW)



V PACKAGE

ABSOLUTE MAXIMUM RATINGS

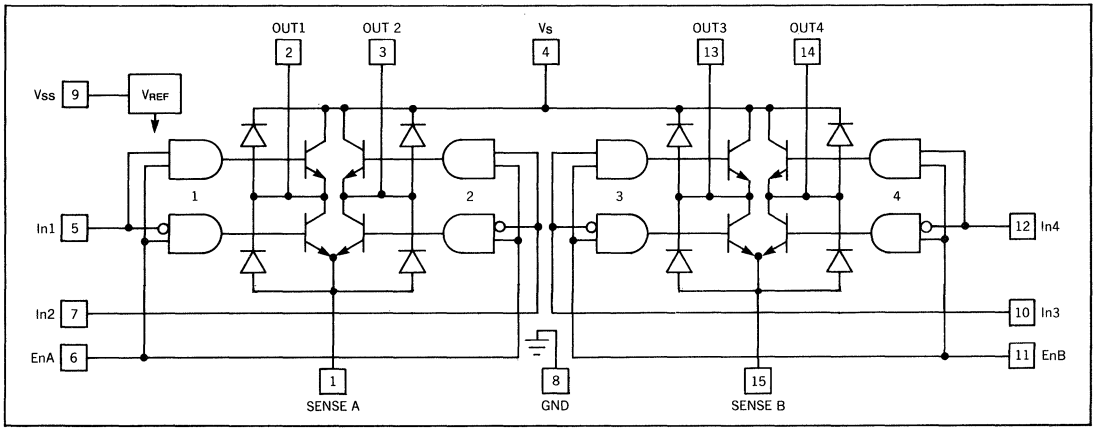
Power Supply, V_s 50V
Logic Supply Voltage, V_{ss} 7V
Input and Enable Voltage, V_i, V_{En} ..... -0.3V to +7V
Peak Output Current (each channel), I_o
- Non-Repetitive (t = 100μs) 1.5A
- Repetitive (80% on - 20% off; t_{ON} = 10ms) 1.2A
- DC Operation 1A

Sensing Voltage, V_{sens} ..... -1V to +2.3V
Total Power Dissipation (T_{case} = 75°C), P_{tot} 25W
Storage and Junction Temperature, T_{stg}, T_j ..... -40°C to +150°C

THERMAL DATA

Thermal Resistance Junction-Case, $R_{th\ j\text{-}case}$ ..... 3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th\ j\text{-}amb}$ ..... 35°C/W max.

BLOCK DIAGRAM



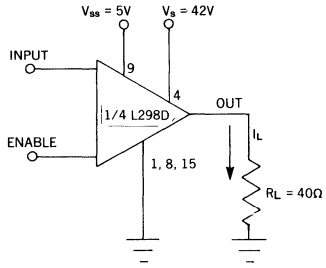
ELECTRICAL CHARACTERISTICS (for each channel, V_s = 42V, V_{ss} = 5V, T_j = 25°C) T_A=T_J

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), V_s	Operating Condition	V_{IH}+2.5		46	V
Logic Supply Voltage (Pin 9), V_{ss}		4.5		7	V
Quiescent Supply Current (Pin 4), I_s	V_{En} = H V_i = L		3	7	mA
	I_L = 0 V_i = H		15	20	
	V_{En} = L			1	
Quiescent Current from V_{ss} (Pin 9), I_{ss}	V_{En} = H V_i = L		5	10	mA
	I_L = 0 V_i = H		1.5	3	
	V_{En} = L		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_{i\ L}$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_{i\ H}$		2.3		V_{ss}	
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ L}$	V_i = L			-10	μA
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{i\ H}$	V_i = H		30	100	
Enable Low Voltage (Pins 6, 11), $V_{En\ L}$		-0.3		1.5	V
Enable High Voltage (Pins 6, 11), $V_{En\ H}$		2.3		7	
Low Voltage Enable Current (Pins 6, 11), $I_{En\ L}$	V_{En} = L			-10	μA
High Voltage Enable Current (Pins 6, 11), $I_{En\ H}$	V_{En} = H ≤ V_{ss} -0.6V		30	100	
Source Saturation Voltage, $V_{CE\ sat(H)}$	I_L = 1A		1.2	2.2	V
Sink Saturation Voltage, $V_{CE\ sat(L)}$	I_L = 1A		1.4	2.2	V
Total Drop, $V_{CE\ sat}$	I_L = 1A		2.6	4.2	V
High-Side Diode Voltage, $V_{D(H)}$	I_L = 1A		1.6	2.1	V
Low-Side Diode Voltage, $V_{D(L)}$	I_L = 1A		1.6	2.1	V
Sensing Voltage (Pins 1, 15), V_{sens}		-1[1]		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	0.5 V_i to 0.9 I_L[2]		1.7		μs
Source Current Fall Time, $T_2(V_i)$	0.9 I_L to 0.1 I_L[2]		0.2		μs
Source Current Turn-On Delay, $T_3(V_i)$	0.5 V_i to 0.1 I_L[2]		2.5		μs
Source Current Rise Time, $T_4(V_i)$	0.1 I_L to 0.9 I_L[2]		0.35		μs
Sink Current Turn-Off Delay, $T_5(V_i)$	0.5 V_i to 0.9 I_L[3]		0.7		μs
Sink Current Fall Time, $T_6(V_i)$	0.9 I_L to 0.1 I_L[3]		0.2		μs
Sink Current Turn-On Delay, $T_7(V_i)$	0.5 V_i to 0.1 I_L[3]		1.5		μs
Sink Current Rise Time, $T_8(V_i)$	0.1 I_L to 0.9 I_L[3]		0.2		μs
Commutation Frequency, f_c	I_L = 1A		25	40	KHz

1) Sensing voltage can be -1V for t ≤ 50μS; in steady state V_{sens} min ≥ -0.5V.
2) See figure 1a.
3) See figure 2a.

SWITCHING CHARACTERISTICS

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input.

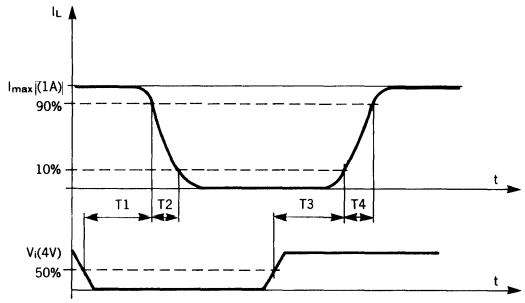
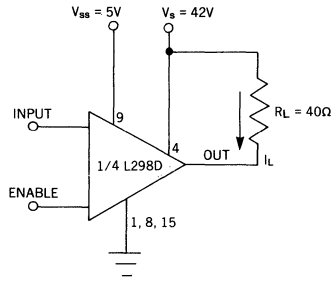
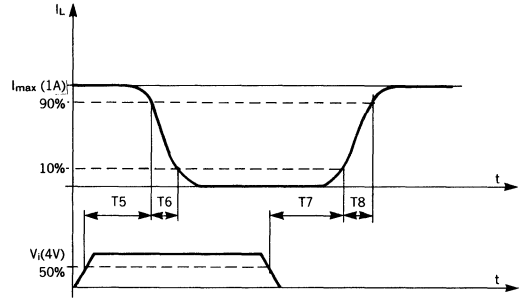


Figure 2. Switching Times Test Circuits.



NOTE: For INPUT chopper, set EN = H.

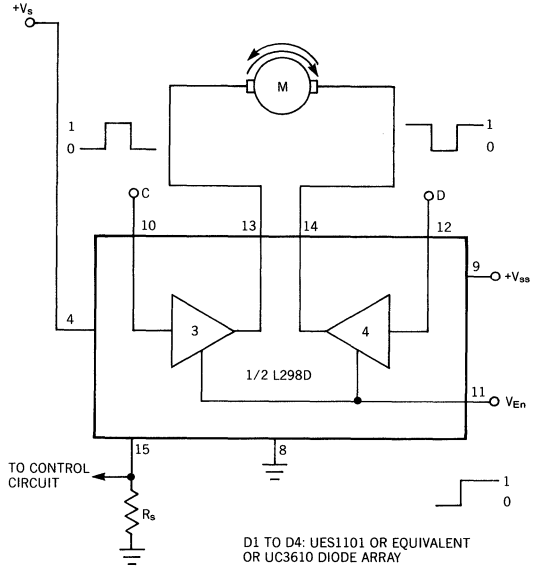
Figure 2a. Sink Current Delay Times vs. Input.



6

APPLICATIONS

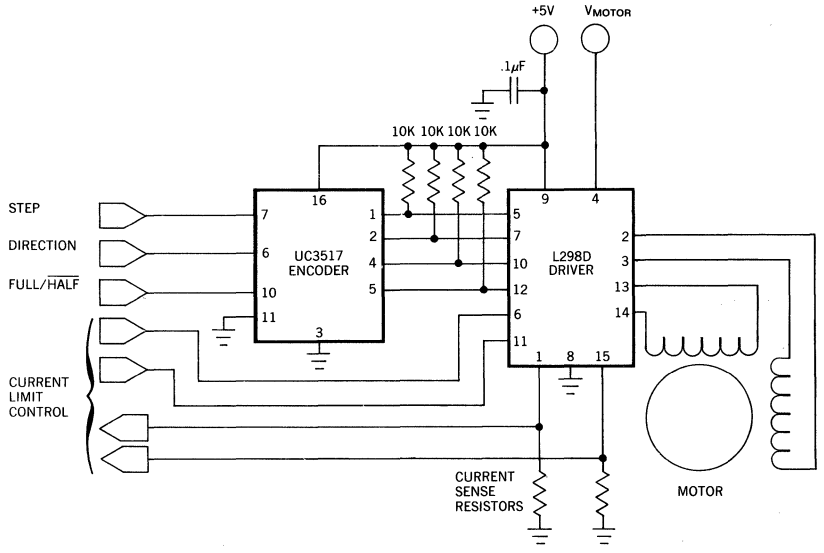
Figure 3. Bi-Directional DC Motor Control.



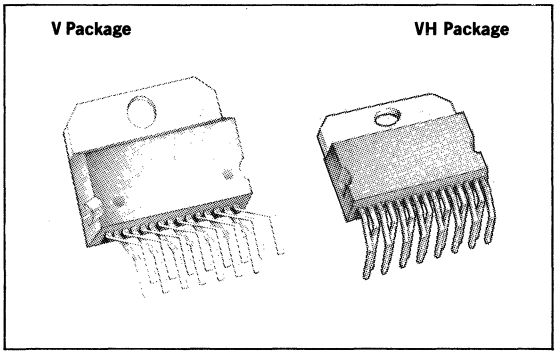
	INPUTS	FUNCTION
V_{En} = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V_{En} = L	C = X; D = C	Free running motor stop

L = Low
H = High
X = Don't Care

Figure 4. Bipolar Step Motor Driver.



STANDARD PACKAGES



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Stepper Motor Drive Circuit

FEATURES

- Complete Motor Driver and Encoder
- Continuous Drive Capability 350mA per Phase
- Contains all Required Logic for Full and Half Stepping
- Bilevel Operation for Fast Step Rates
- Operates as a Voltage Doubler
- Useable as a Phase Generator and/or as a Driver
- Power-On Reset Guarantees Safe, Predictable Power-Up

DESCRIPTION

The UC3517 contains four NPN drivers that operate in two-phase fashion for full-step and half-step motor control. The UC3517 also contains two emitter followers, two monostables, phase decoder logic, power-on reset, and low-voltage protection, making it a versatile system for driving small stepper motors or for controlling large power devices.

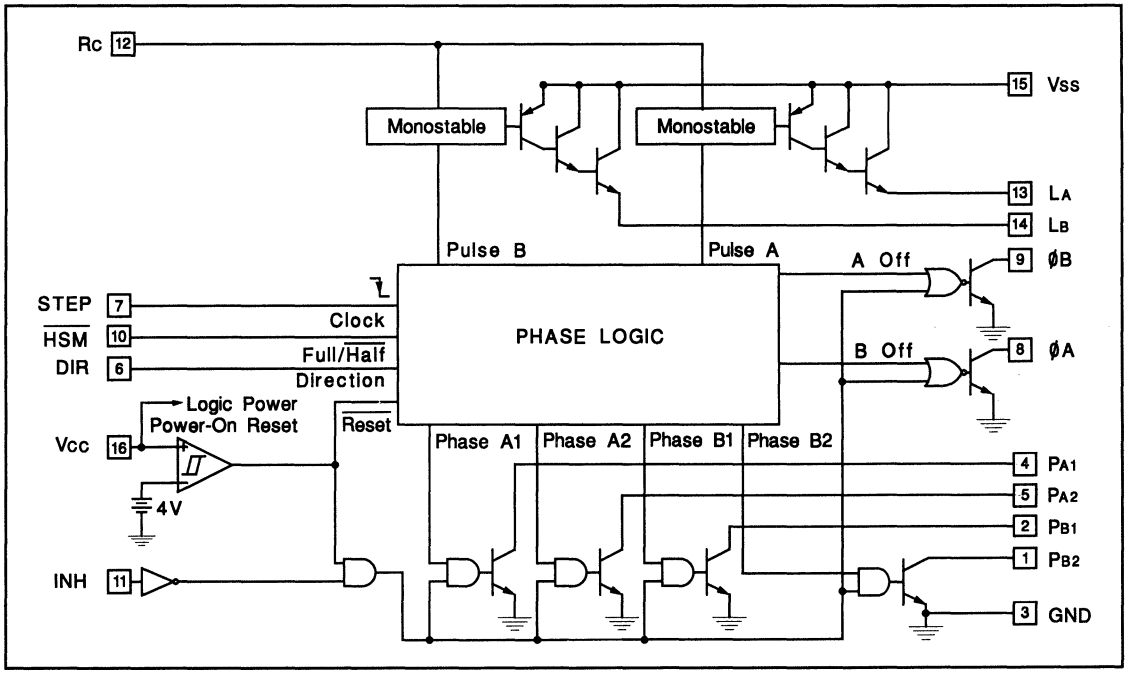
The emitter followers and monostables in the UC3517 are configured to apply higher-voltage pulses to the motor at each step command. This drive technique, called "Bilevel," allows faster stepping than common resistive current limiting, yet generates less electrical noise than chopping techniques.

ABSOLUTE MAXIMUM RATINGS

Second Level Supply, Vss 40V
Phase Output Supply, VMM 40V
Logic Supply, Vcc 7V
Logic Input Voltage ..... -.3V to +7V
Logic Input Current ..... ±10mA
Output Current, Each Phase 500mA
Output Current, Emitter Follower ..... -500mA
Power Dissipation, (Note) 1W
Power Dissipation, (Note) 2W
Junction Temperature ..... 150°C
Ambient Temperature, UC1517 ..... -55°C to +125°C
Ambient Temperature, UC3517 ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C

Note: Consult Packaging section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM



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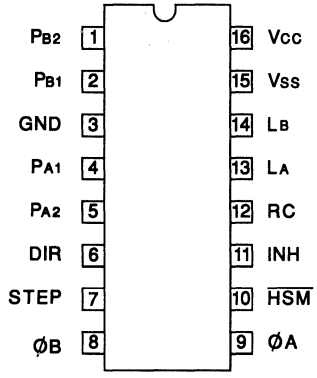
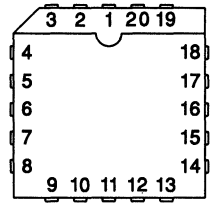
CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20
(TOP VIEW)
Q & L PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
P_{B2}	2
P_{B1}	3
GND	4
P_{A1}	5
N/C	6
P_{A2}	7
DIR	8
STEP	9
$Ø_B$	10
N/C	11
$Ø_A$	12
$\overline{HSM}$	13
INH	14
RC	15
N/C	16
L_A	17
L_B	18
V_{SS}	19
V_{CC}	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1517 and 0°C to +70°C for the UC3517, Vcc=5V, Vss = 20V, T_A=T_J. Pin numbers refer to DIL-16 package.

PARAMETER	TEST CONDITIONS	UC1517 / UC3517			UNITS
		MIN	TYP	MAX	
Logic Supply, Vcc	Pin 16	4.75		5.25	V
Second Supply, Vss	Pin 15	10		40	V
Logic Supply Current	V_{INH} = 0.4V		45	60	mA
	V_{INH} = 4.0V		12		mA
Input Low Voltage	Pins 6, 7, 10, 11			0.8	V
Input High Voltage	Pins 6, 7, 10, 11	2.0			V
Input Low Current	Pins 6, 7, 10, 11; V = 0V	-400			µA
Input High Current	Pins 6, 7, 10, 11; V = 5V			20	µA
Phase Output Saturation Voltage	Pins 1, 2, 4, 5; I = 350mA		0.6	0.85	V
Phase Output Leakage Current	Pins 1, 2, 4, 5; V = 39V			500	µA
Follower Saturation Voltage to Vss	Pins 13,14; I = 350mA			-2	V
Follower Leakage Current	Pins 13,14; V = 0V			500	µA
Output Low Voltage, $Ø_A$, $Ø_B$	Pins 8, 9; I = 1.6mA		0.1	0.4	V
Phase Turn-On Time	Pins 1, 2, 4, 5		2		µs
Phase Turn-Off Time	Pins 1, 2, 4, 5		1.8		µs
Second-Level On Time. T_{MONO}	Pins 13,14; Figure 3 Test Circuit	275	325	375	µs
Logic Input Set-up Time, ts	Pins 6, 10; Figure 4	400			ns
Logic Input Hold Time, th	Pins 6, 10; Figure 4	0			ns
STEP Pulse Width, tP	Pin 7; Figure 4	800			ns
Timing Resistor Value	Pin 12	1k		100k	Ω
Timing Capacitor Value	Pin 12	0.1		500	nF
Power-On Threshold	Pin 16		4.3		V
Power-Off Threshold	Pin 16		3.8		V
Power Hysteresis	Pin 16		0.5		V

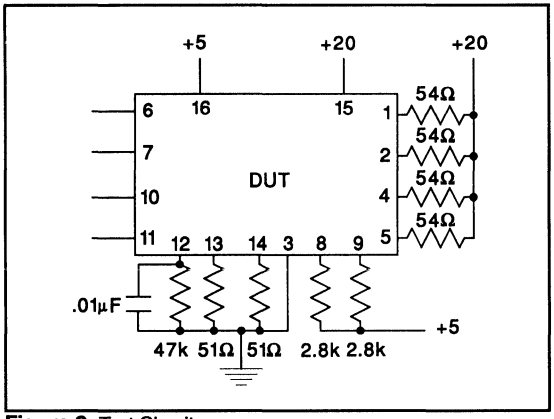


Figure 3. Test Circuit

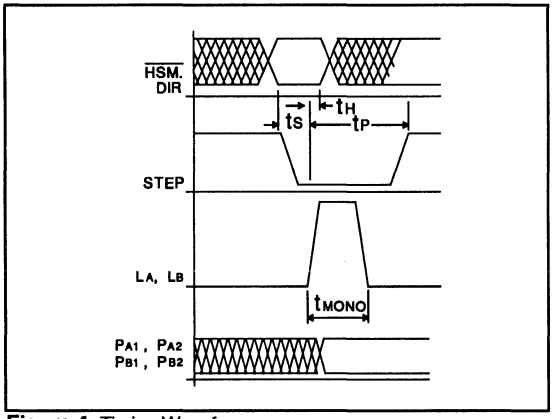


Figure 4. Timing Waveforms

PIN DESCRIPTION

VCC: VCC is the UC3517's logic supply. Connect to a regulated 5VDC, and bypass with a 0.1μF ceramic capacitor to absorb switching transients.

VMM: VMM is the primary motor supply. It connects to the UC3517 phase outputs through the motor windings. Limit this supply to less than 40V to prevent breakdown of the phase output transistors. Select the nominal VMM voltage for the desired continuous winding current.

VSS: VSS is the secondary motor supply. It drives the LA and LB outputs of the UC3517 when a monostable in the UC3517 is active. In the bilevel application, this supply is applied to the motor to charge the winding inductance faster than the primary supply could. Typically, VSS is higher in voltage than VMM, although VSS must be less than 40V. The VSS supply should have good transient capability.

GROUND: The ground pin is the common reference for all supplies, inputs and outputs.

RC: RC controls the timing functions of the monostables in the UC3517. It is normally connected to a resistor (R_T) and a capacitor (C_T) to ground, as shown in Figure 3. Monostable on time is determined by the formula $T_{ON} \approx 0.69\ R_T\ C_T$. To keep the monostable on indefinitely, pull RC to VCC through a 50k resistor. The UC3517 contains only one RC pin for two monostables. If step rates comparable to TON are commanded, incorrect pulsing can result, so consider maximum step rates when selecting RT and CT. Keep $T_{ON} \leq T_{STEP\ MAX}$.

ØA and ØB: These logic outputs indicate half-step position. These outputs are open-collector, low-current drivers, and may directly drive TTL logic. They can also drive CMOS logic if a pull-up resistor is provided. Systems which use the UC3517 as an encoder and use a different driver can use these outputs to disable the external driver, as shown in Figure 8. The sequencing of these outputs is shown in Figure 5.

PA1, PA2, PB1, and PB2: The phase outputs pull to ground sequentially to cause motor stepping, according to the state diagram of Figure 5. The sequence of stepping on these lines, as well as with the LA and LB lines is controlled by STEP input, the DIR input, and the $\overline{HSM}$ input. Caution: If these outputs or any other IC pins are pulled too far below ground either continuously or in a transient, step memory can be lost. It is recommended that these pins be clamped to ground and supply with high-speed diodes when driving inductive loads such as motor windings or solenoids. This clamping is very important because one side of the winding can "kick" in a direction opposite the swing of the other side.

LA and LB: These outputs pull to VSS when their corresponding monostable is active, and will remain high until the monostable time elapses. Before and after, these outputs are high-impedance. For detail timing information, consult Figure 5.

STEP: This logic input clocks the logic in the UC3517 on every falling edge. Like all other UC3517 inputs, this input is TTL/CMOS compatible, and should not be pulled below ground.

DIR: This logic input controls the motor rotation direction by controlling the phase output sequence as shown in Figure 5. This signal must be stable 400ns before a falling edge on STEP, and must remain stable through the edge to insure correct stepping.

$\overline{HSM}$: This logic input switches the UC3517 between half-stepping ($\overline{HSM}$ = low) and full-stepping ($\overline{HSM}$ = high) by controlling the phase output sequence as show in Figure 5. This line requires the same set-up time as the DIR input, and has the same hold requirement.

INH: When the inhibit input is high, the phase and θ outputs are inhibited (high impedance). STEP pulses received while inhibited will continue to update logic in the IC, but the states will not be reflected at the outputs until inhibit is pulled low. In stepper motor systems, this can be used to save power or to allow the rotor to move freely for manual repositioning.

OPERATING MODES

The UC3517 is a system component capable of many different operating modes, including:

Unipolar Stepper Driver: In its simplest form, the UC3517 can be connected to a stepper motor as a unipolar driver. L_A, L_B, RC and Vss are not used, and may be left open. All other system design considerations mentioned above apply, including choice of motor supply VMM, undershoot diodes and timing considerations.

Unipolar Bilevel Stepper Driver: If increased step rates are desired, the application circuit of Figure 6 makes use of the monostables and emitter followers as well as the configuration mentioned above to provide high-voltage pulses to the motor windings when the phase is turned on. For a given dissipation level, this mode offers faster step rates, and very little additional electrical noise.

The choice of monostable components can be estimated based on the timing relationship of motor current and voltage: V = Ldl/dt. Assuming a fixed secondary supply voltage (Vss), a fixed winding inductance (L_M), a desired winding peak current (Iw), and no back EMF from the motor, we can estimate that R_TC_T = 1.449 I_WL_M/Vss. In practice, these calculations should be confirmed and adjusted to accommodate for effects not modeled.

Voltage-Doubled Mode: The UC3517 can also be used to generate higher voltages than available with the system power supplies using capacitors and diodes. Figure 9 shows how this might be done, and gives some estimates for the component values.

Higher Current Operation: For systems requiring more than 350mA of drive per phase, the UC3717A can be used in conjunction with discrete power transistors or power driver ICs, like the L298. These can be connected as current gain devices that turn on when the phase outputs turn on.

Bipolar Motor Drive: Bipolar motors can be controlled by the UC3517 with the addition of bipolar integrated drivers such as the UC3717A (Figure 8) and the L298, or discrete devices. Care should be taken with discrete devices to avoid potential cross-conduction problems.

LOGIC FLOW GRAPH

The UC3517 contains a bidirectional counter which is decoded to generate the correct phase and Ø outputs. This counter is incremented on every falling edge of the STEP input. Figure 5 shows a graph representing the counter sequence, inputs that determine the next state (DIR and $\overline{HSM}$), and the outputs at each state. Each circle represents a unique logic state, and the four inside circles represent the half-step states.

The four bits inside the circles represent the phase outputs in each state (P_{A1}, P_{A2}, P_{B1}, and P_{B2}). For example, the circle labeled 1010 is immediately entered when the device is powered up, and represents P_{A1} off ("1" or high), P_{A2} on ("0" or low), P_{B1} off ("1" or high) and P_{B2} on ("0" or low). The $Ø_A$ and $Ø_B$ outputs are both low (unidentified).

The arrows in the graph show the state changes. For example, if the IC is in state 0110, DIR is high, $\overline{HSM}$ is high, and STEP falls, the next state will be 0101, and a pulse will be generated on the L_B line by the monostable.

Inhibit will not effect the logic state, but it will cause all phase outputs and both Ø outputs to go high (off). A falling edge on STEP will still cause a state change, but inhibit will have to toggle low for the state to be apparent.

A falling edge on STEP with $\overline{HSM}$ high will cause the counter to advance to the next full step state regardless of whether or not it was in a full step state previously.

No L_A or L_B pulses are generated entering half-states.

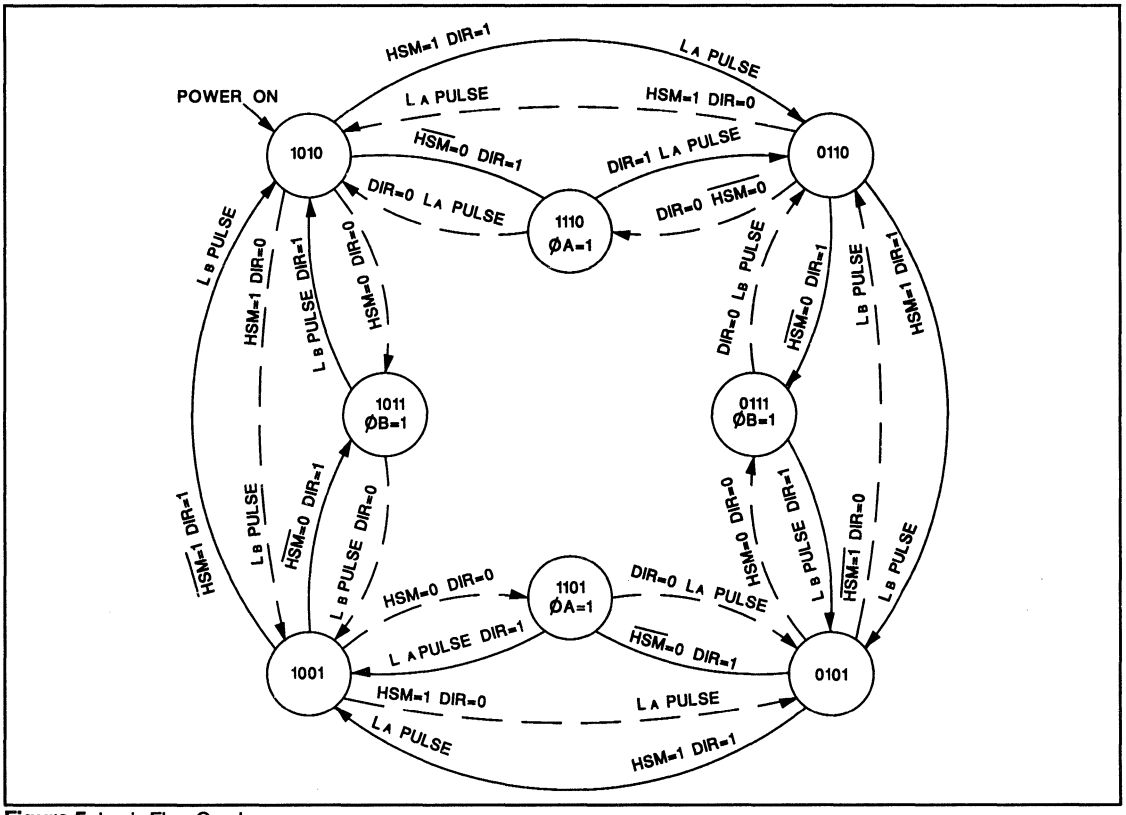
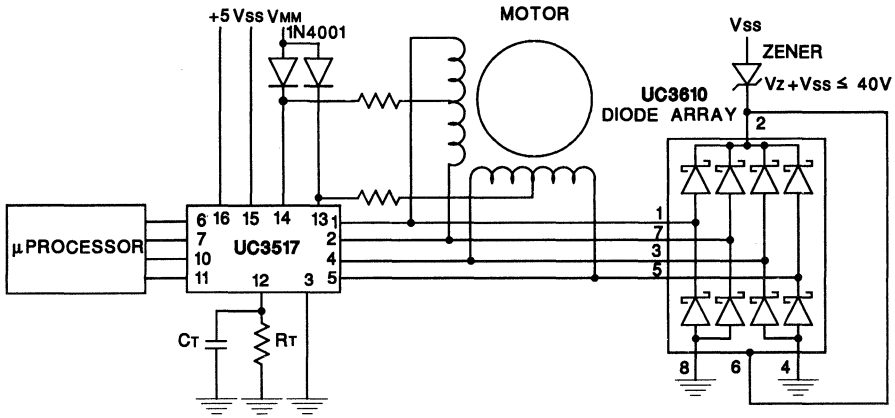
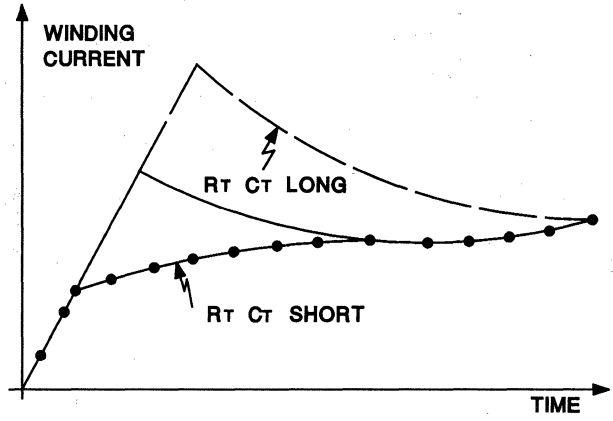


Figure 5. Logic Flow Graph



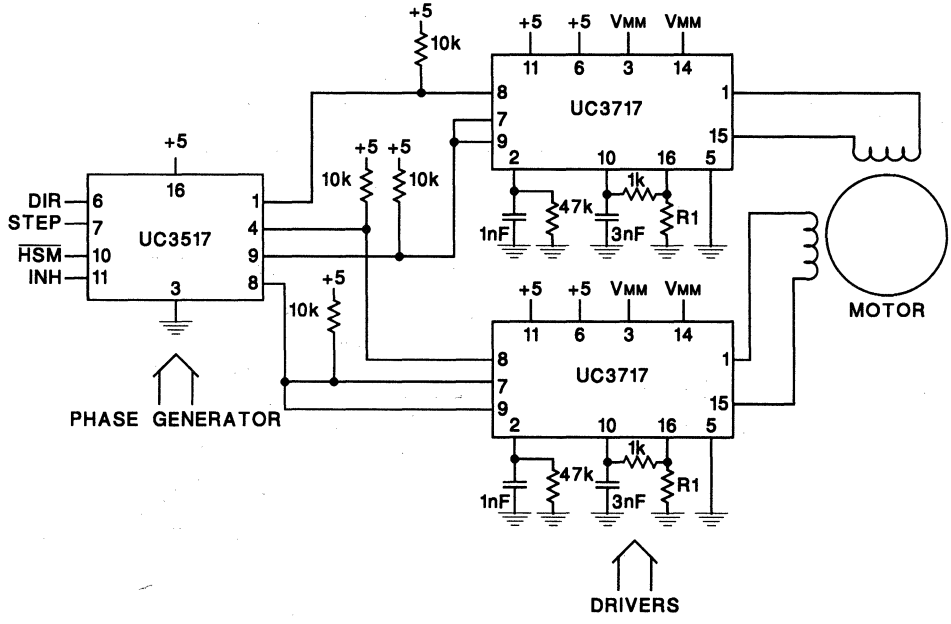
For applications requiring very fast step rates, a zener diode permits windings to discharge at higher voltages, and higher rates. Driver transistor breakdown must be considered when selecting Vss and zener voltage to insure that the outputs will not overshoot past 40V. If the zener diodes are not used and UC3610 pin 2 is connected directly to Vss then higher Vss can be used.

Figure 6. Bilevel Motor Driver



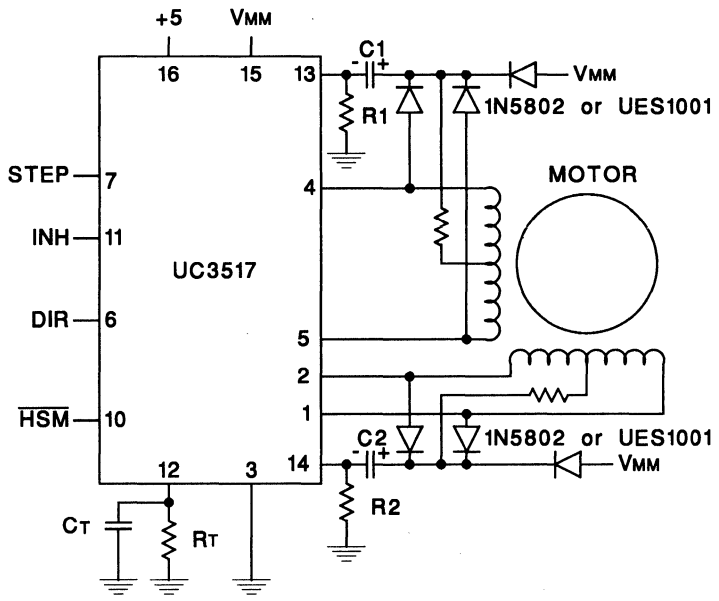
Experimental selection of RT and CT allow the designer to select a small amount of winding current overshoot, as shown above. Although the overshoot may exceed the continuous rated current of the winding and the drive transistors, the duration can be well controlled. Average power dissipation for the driver and motor must be considered when designing systems with intentional overshoot, and must stay within conservative limits for short duty cycles.

Figure 7. Effects of Different RT & CT on Bilevel Systems



In this application, the ØA and ØB outputs of the UC3517 are connected to the current program inputs of the UC3717. This allows the UC3517 inhibit signal to inhibit the UC3717, and also allows half-step operation of the UC3717. Peak motor winding current will be limited to approximately .42V/R1 by chopping.

Figure 8. Interface to UC3717 Bipolar Driver



Although component values can be best optimized experimentally, good starting values speed development. For this design, start with:

$R_T C_T = 3 L_W/R_W$
$C_1 = C_2 = L_W I_R/R_W$
$R_1 = R_2 = 2.9 T_{MIN}/C_1$

where:

L_W is winding inductance,
R_W is winding resistance,
I_R is rated winding current, and
T_{MIN} is minimum step period expected.

Figure 9. Using the UC3517 as a Voltage Doubler

6

UNITRODE INTEGRATED CIRCUITS
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Dual Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to +70°C temperature range.

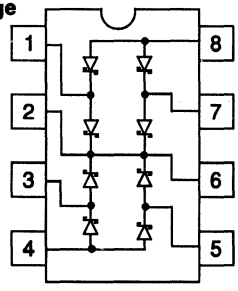
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 ..... 1A
  UC3610 ..... 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

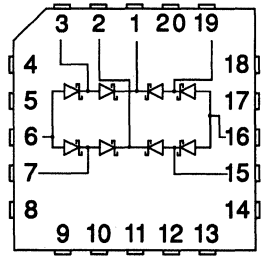
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

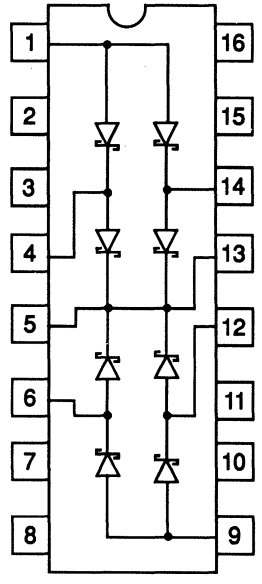
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package

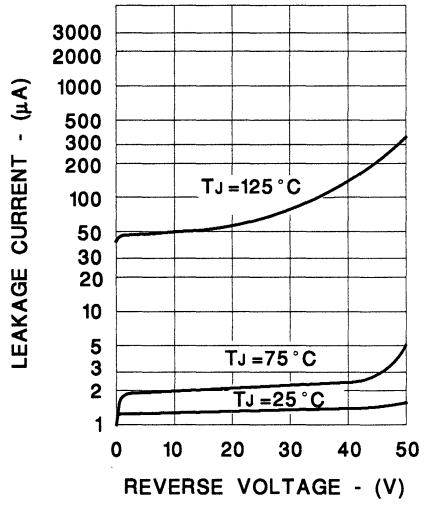


ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = 25°C except as noted. T_A = T_J.

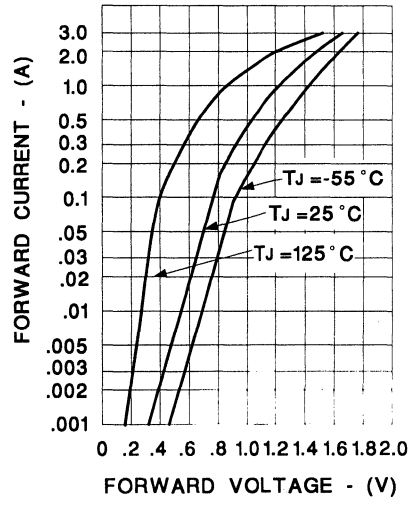
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA	0.4	0.5	0.7	V
	I_F = 1A	0.8	1.0	1.3	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A a parasitic current of approximately 10mA may be collected by adjacent diodes.

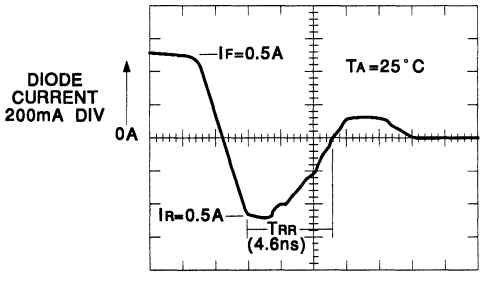
Reverse Current vs Voltage



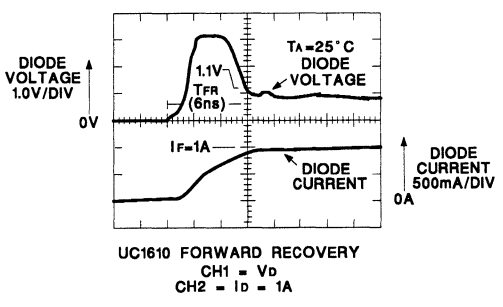
Forward Current vs Voltage



Reverse Recovery Characteristics



Forward Recovery Characteristics



UC1610 FORWARD RECOVERY
CH1 = V_D
CH2 = I_D = 1A

6

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Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low-Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

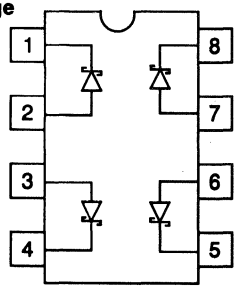
These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

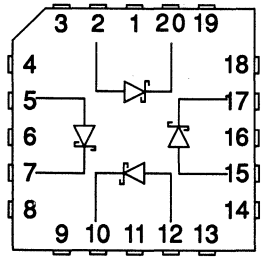
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1611 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

CONNECTION DIAGRAM

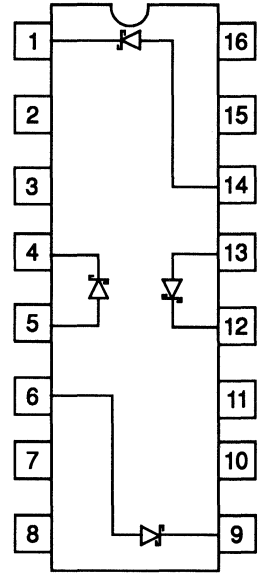
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



ABSOLUTE MAXIMUM RATINGS

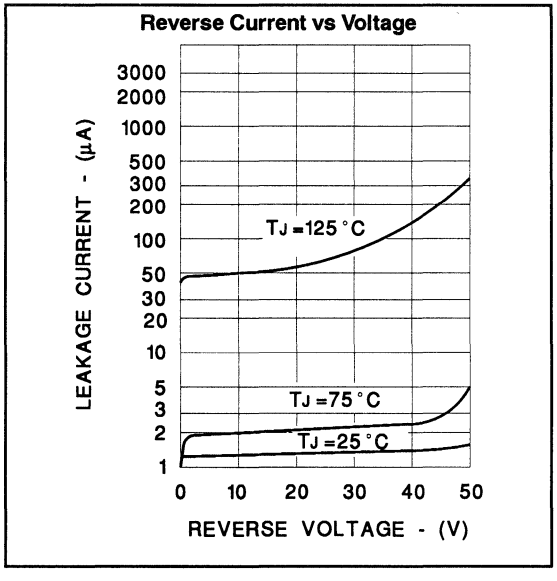
Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
UC1611 ..... 1A
UC3611 ..... 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C
Note: Please consult Packaging Section of Databook for thermal limitations and considerations of package.

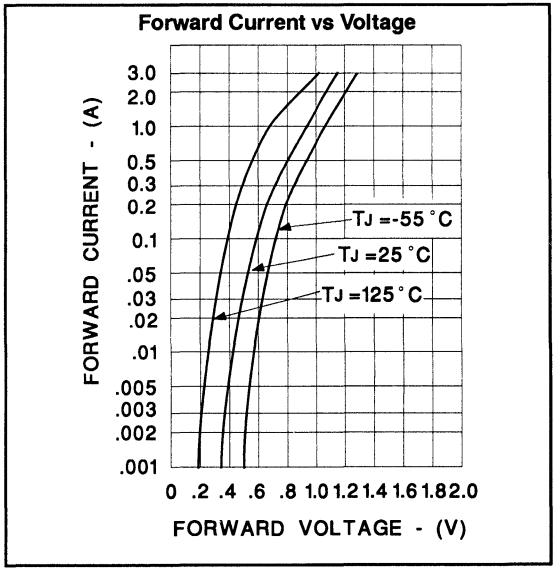
ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = +25°C except as noted. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA	0.3	0.4	0.7	V
	I_F = 1A		0.9	1.2	V
Leakage Current	V_R = 40V		0.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

Note: At Forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

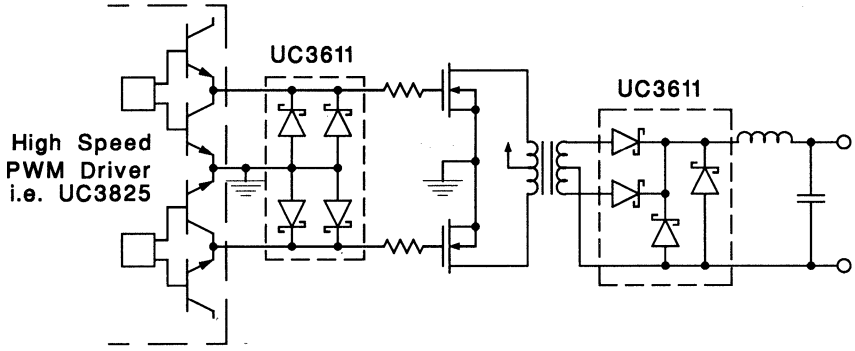
6



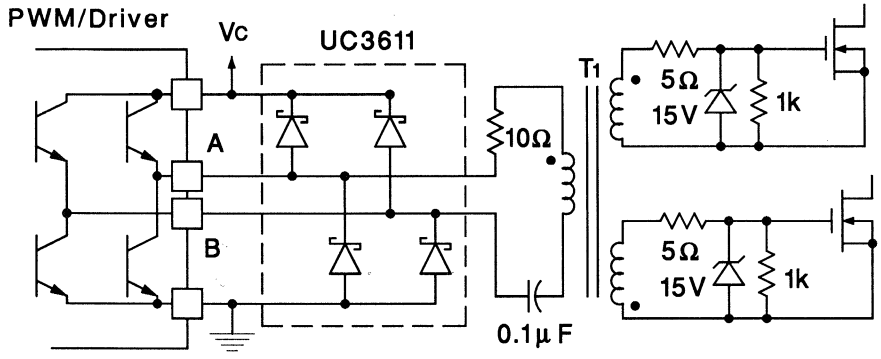


TYPICAL APPLICATIONS

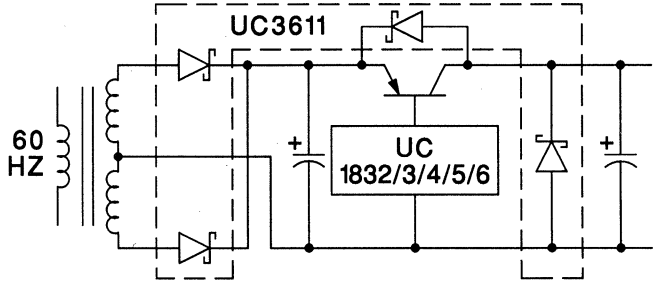
A. Clamp Diodes - PWMS and Drivers



B. Transformer Coupled Drive Circuits



C. Linear Regulations



UNITRODE INTEGRATED CIRCUITS
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Dual Schottky Diode

FEATURES

- Monolithic Two Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

The two-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

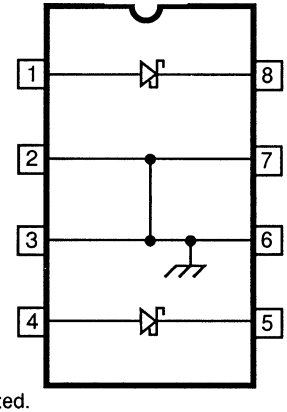
This single monolithic chip is fabricated in hermetic CERDIP as well as copper leaded plastic MINIDIP and SOIC surface mount power pack. The UC1612 in ceramic is designed for -55°C to +125°C environments, but with reduced peak current capability; while the UC3612 has higher current rating over a 0°C to +70°C ambient temperature range.

ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current, UC3612 ..... 3A
Peak Forward Current, UC1612 ..... 1A
Power Dissipation at TA = 70°C 1W
  Derate 12.5mW/°C above 70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

CONNECTION DIAGRAM

J, N or DP PACKAGE
(TOP VIEW)



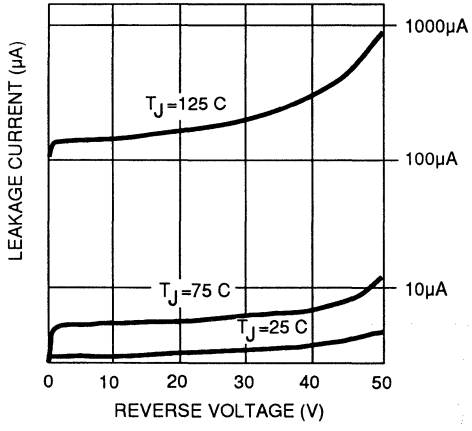
Pins 2,3,6,7 are connected to substrate and must be electrically isolated.

Electrical Characteristics (All specifications apply to each individual diode. T_J = 25°C except as noted).

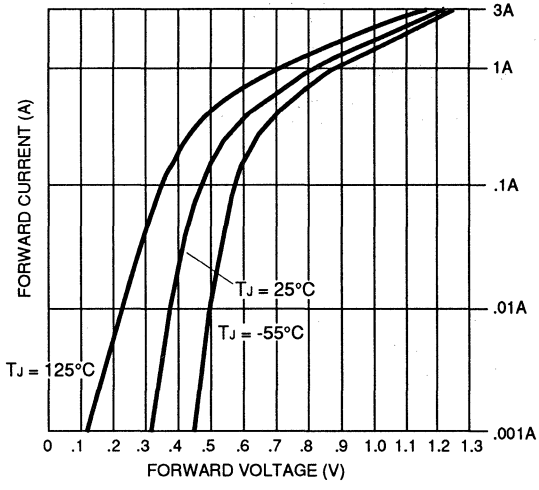
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA		0.49	.55	V
	I_F = 1A		0.90	1.0	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = 100°C		0.1	1.0	mA
Reverse Recovery	.5A Forward to .5A Reverse		15		nSec
Forward Recovery	1A Forward to 1.1V Recovery		30		nSec
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

Reverse Current vs Voltage



Forward Voltage vs Current



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Switchmode Driver for 3-∅ Brushless DC Motors

FEATURES

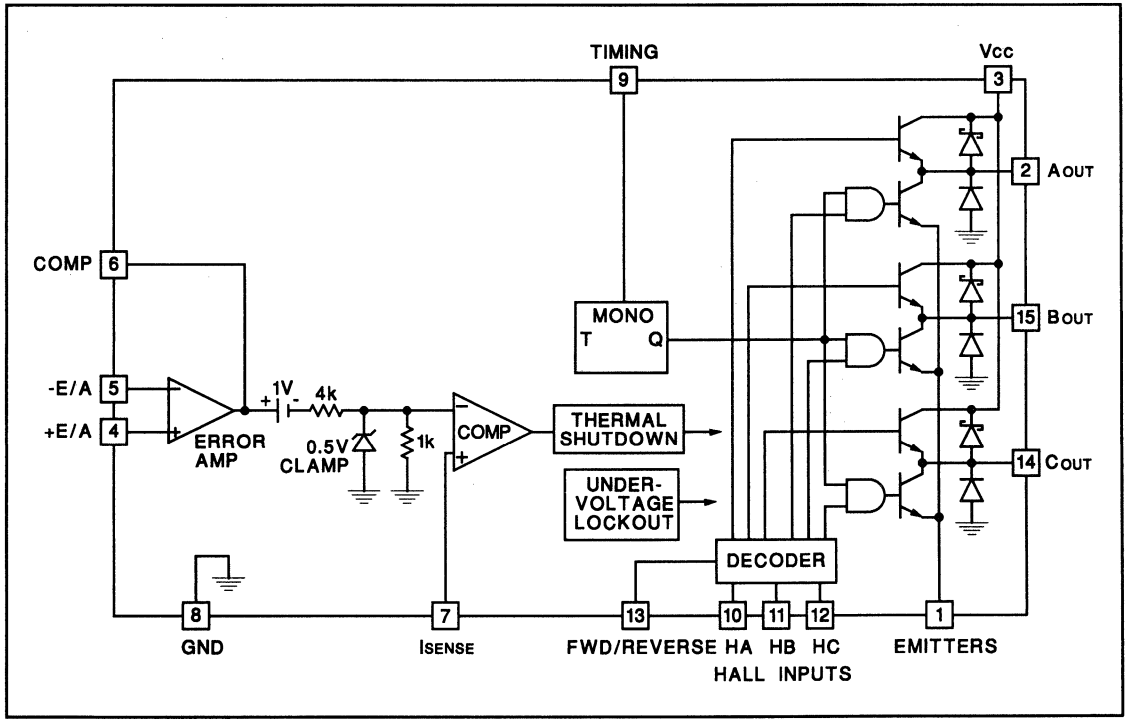
- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Velocity Control Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- Available in V, VH Multiwatt Plastic, and SP Hermetic Packages

DESCRIPTION

The UC3620 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/μs for any load condition.

The UC1620SP is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC3620SP is characterized for 0°C to +70°C. Surface mount versions are also available.

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

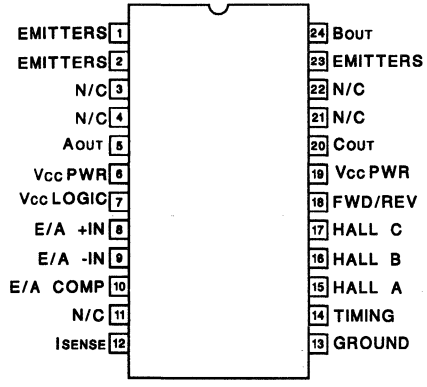
Supply Voltage, Vcc 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100µsec), Io 3A
  Repetitive (80% on - 20% off; tON = 10ms) 2.5A
  DC Operation 2A
Analog Inputs ..... -0.3 to +Vcc
Logic Inputs ..... -0.3 to +Vcc
Total Power Dissipation (at TCASE = 75° C)
  for SP Package (Note 2) 15W
Storage and Junction Temperature ..... -40°C to +150°C

Note 1: All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

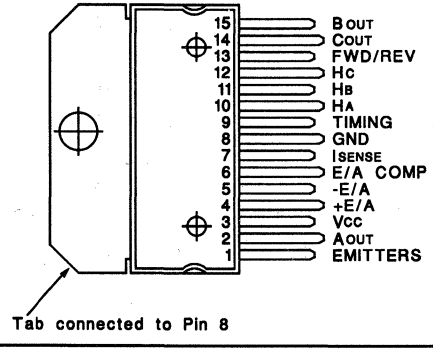
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

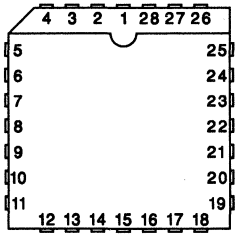
SP Hermetic Power DIL



V and VH Packages



28-PIN LCC and (TOP VIEW) L Package



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
N/C	1
EMITTERS	2
EMITTERS	3
N/C	4
N/C	5
AOUT	6
Vcc PWR	7
N/C	8
Vcc LOGIC	9
+E/A	10
-E/A	11
N/C	12
E/A COMP	13
ISENSE	14
GND	15
TIMING	16
HA	17
N/C	18
N/C	19
HB	20
HC	21
FWD/REV	22
Vcc PWR	23
COUT	24
N/C	25
N/C	26
EMITTERS	27
BOUT	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for 3620; T_A = 55°C to +125°C for UC1620; V_{CC} = 20V, R_T = 20V, R_T = 10k, C_T = -2.2nF. T_A=T_J.

PARAMETER	TEST CONDITIONS	UC3620			UC1620			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage			1.5	10		1.5	10	mV
Input Bias Current			-.25	-2.0		-.25	-2.0	µA
Input Offset Current			15	250		15	250	nA
Common Mode Range	V_{CC} = 8V to 40V	0		V_{IN}-2	0		V_{IN}-2	V
Open Loop Gain	ΔV_{PIN6} = 1V to 4V	80	100		75	100		dB
Unity Gain Bandwidth	T_J = 25°C, Note 2		0.8			0.8		MHz
Output Sink Current	V_{PIN6} = 1V		2			2		mA
Output Source Current	V_{PIN6} = 4V		8			8		mA
Current Sense Section								
Input Bias Current			-2.0	-5		-2.0	-5	µA
Internal Clamp		.425	0.5	.575	.405	0.5	.595	V
Divider Gain		.180	0.2	.220	.170	0.2	.230	V/V
Internal Offset Voltage		.8	1.0	1.2	.75	1.0	1.25	V
Timing Section								
Output Off Time		18	20	22	17	20	23	µs
Upper Mono Threshold			5.0			5.0		V
Lower Mono Threshold			2.0			2.0		V
Decoder Section								
High-Level Input Voltage		2.2			2.5			V
Low-Level Input Voltage				0.8			0.8	V
High-Level Input Current				10			10	µA
Low-Level Input Current		-10			-10			µA
Output Section								
Output Leakage Current	V_{CC} = 40V			500			1500	µA
VF1 Schottky Diode	I_O = 2A		1.5	2.0		1.5	2.0	V
VF1 Substrate Diode	I_O = 2A		2.2	3.0		2.2	3.0	V
Total Output Voltage Drop	I_O = 2A, Note 3		3.0	3.6		3.0	3.6	V
Output Rise Time	R_L = 44Ω		150			150		ns
Output Fall Time	R_L = 44Ω		150			150		ns
Under Voltage Lockout								
Startup Threshold				8.0			8.0	V
Threshold Hysteresis			0.5			0.5		V
Thermal Shutdown								
Junction Temperature		150		180	150		180	°C
Total Standby Current								
Supply Current			32	55		32	55	mA

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3: The total voltage drop is defined as the sum of both top and bottom side driver.

TABLE 1

STEP	FWD/ REV	Ha	Hb	Hc	AOUT	BOUT	COUT
1	1	1	0	1	H	L	O
2	1	1	0	0	H	O	L
3	1	1	1	0	O	H	L
4	1	0	1	0	L	H	O
5	1	0	1	1	L	O	H
6	1	0	0	1	O	L	H
1	0	1	0	1	L	H	O
2	0	1	0	0	L	O	H
3	0	1	1	0	O	L	H
4	0	0	1	0	H	L	O
5	0	0	1	1	H	O	L
6	0	0	0	1	O	H	L

H = HIGH OUTPUT
L = LOW OUTPUT
O = OPEN OUTPUT

CIRCUIT DESCRIPTION

The UC3620 is designed for implementation of a complete 3-Ø brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

Table 1 shows the decoding scheme used in the UC3620 to decode and drive each of three high current totem pole output stages. A forward/reverse signal, pin 13, is used to provide direction. At any point in time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by turning the sink driver off during the monostable reset time, producing a fixed off-time chop mode. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses. Hall lines require pull-up resistors.

CURRENT SENSING

Referring to Figure 1, emitter current is sensed across Rs and fed back through a low pass filter to the current sense pin 7. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1kΩ and 1000pF range.

TIMING

An R-C time constant on pin 9 is used by the monostable to generate a fixed off time at the outputs according to the formula:

$$T_{OFF} = .916R_TC_T$$

As the peak current in the emitters approaches the value at the minus (-) input of the on-board comparator, the monostable is triggered, causing the outputs to be turned off. On time is determined by the amount of time required for motor current to increase to the value required to re-trip the monostable. A timing sequence of these events is shown in Figure 2.

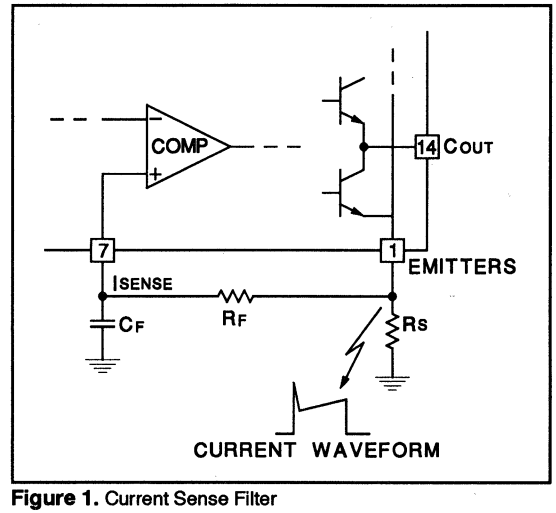


Figure 1. Current Sense Filter

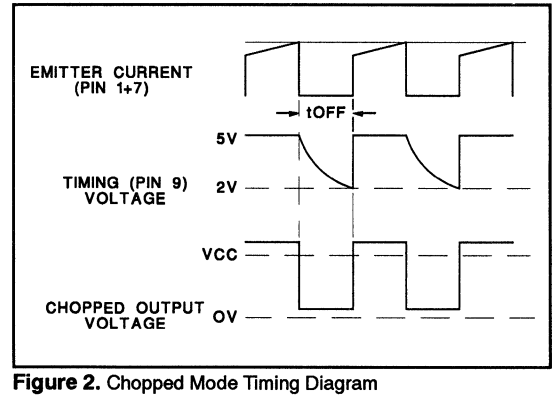


Figure 2. Chopped Mode Timing Diagram

CURRENT LIMIT

Since peak current is being controlled at all times by the internal comparator, a simple voltage clamp at its negative (-) input will limit peak current to a maximum value. A fixed 0.5V internal clamp has been included on the UC3620, and any current spike in the output which generates a sensed voltage greater than 0.5V will immediately shut down the outputs. Actual peak current values may be programmed by selecting the appropriate value of Rs according to the formula:

$$R_S = \frac{0.5}{I_{CURRENTLIMIT}}$$

CIRCUIT DESCRIPTION (cont.)

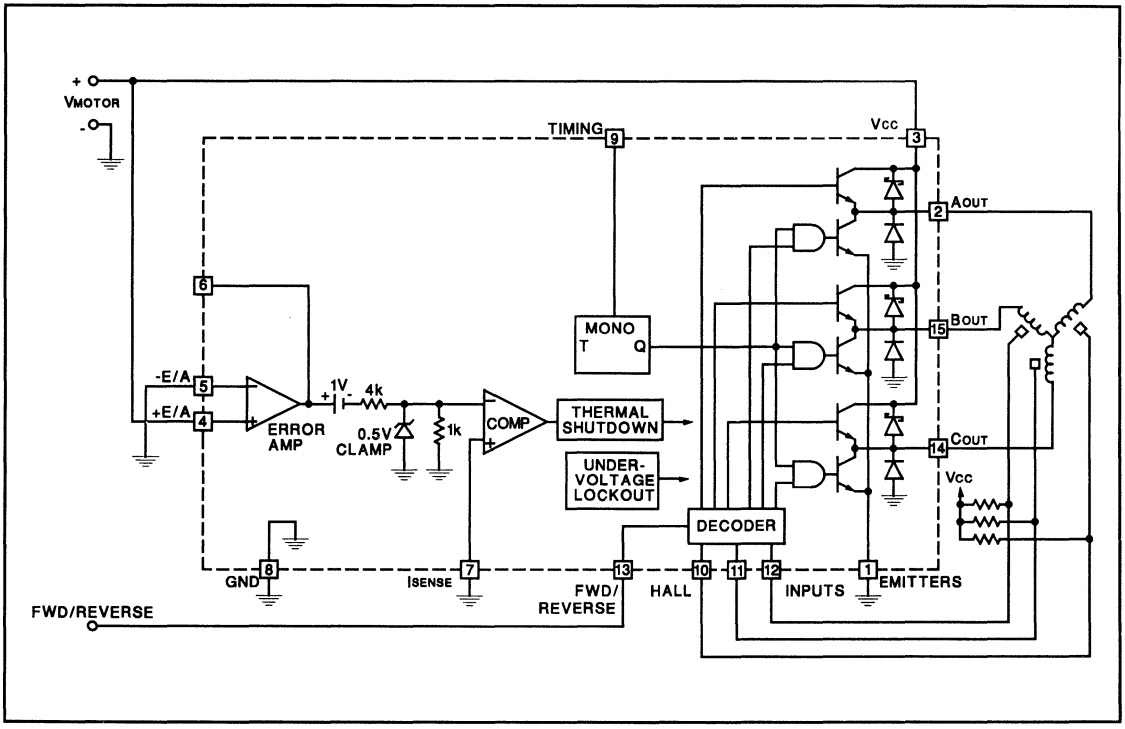
ERROR AMPLIFIER LIMIT

A high performance, on-board error amplifier is included to facilitate implementing closed loop motor control. Error voltage generation and loop compensation are easily accomplished by appropriately configuring the gain and feedback of this amplifier. To provide a larger dynamic signal range at the output of the error amplifier, a divide by 5 resistor network is used to reduce the error signal level before applying to the internal comparator. In addition, a one volt offset has been introduced at the output of the error amplifier to guarantee control down to zero current in the output stages. Since this offset is divided by the open loop gain of the feedback loop, it has virtually no effect on closed loop performance.

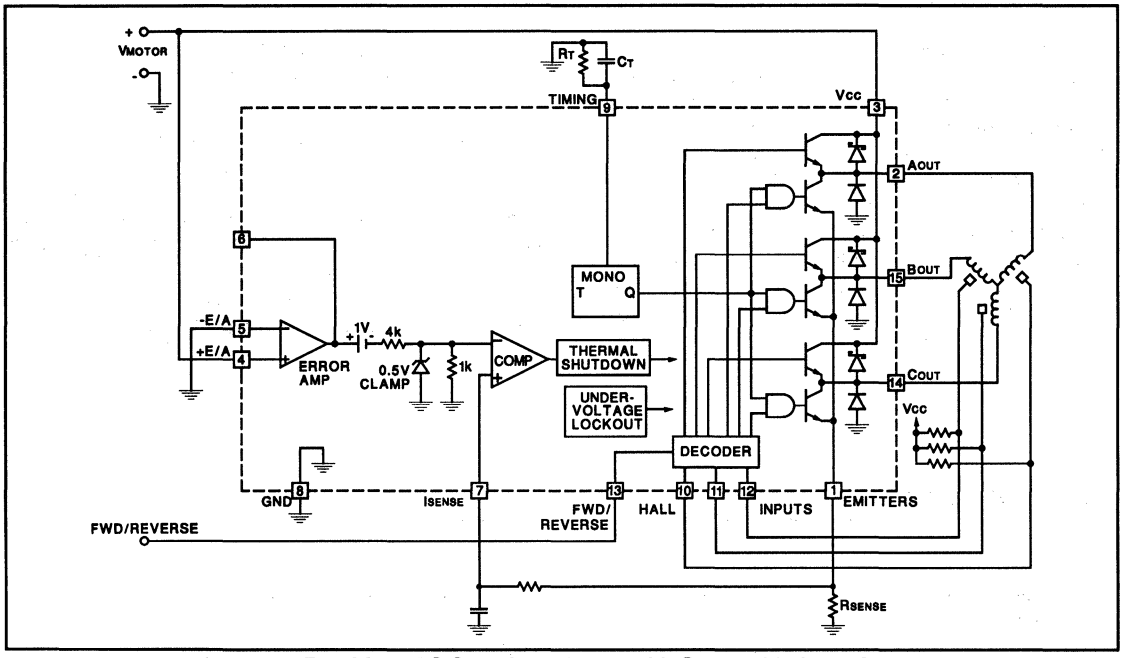
PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-slated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

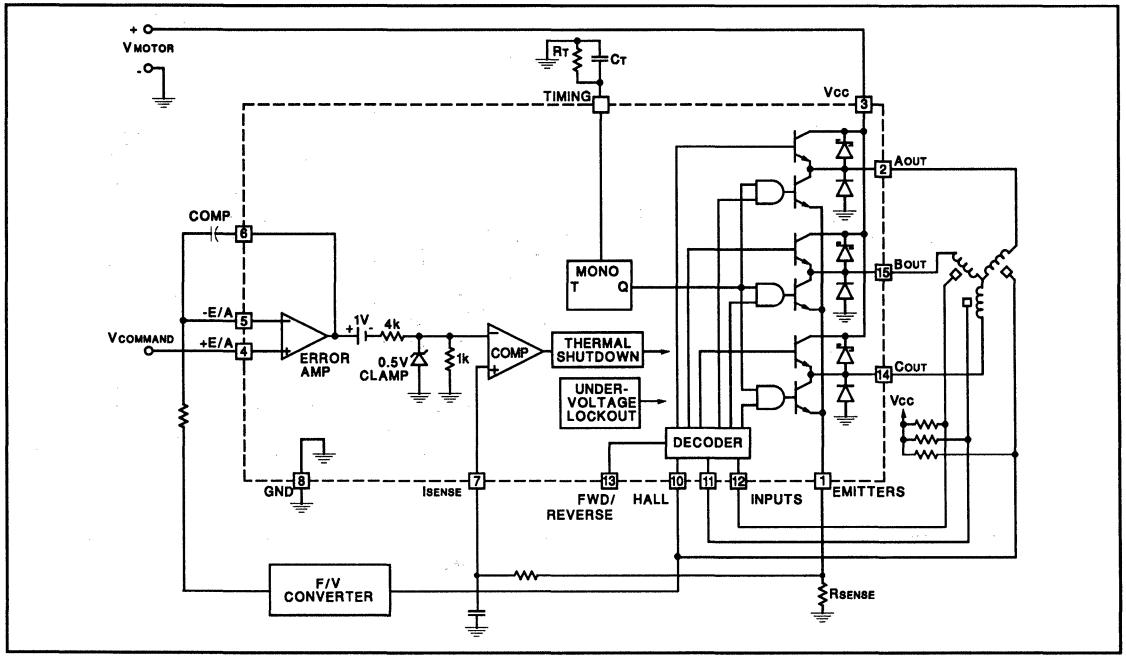
TYPICAL APPLICATIONS



3-∅ Brushless DC Open Loop Motor Drive



3-∅ Brushless DC Open Loop Motor with Current Limit at 2A.



Closed Loop Speed Control Servo

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Brushless DC Motor Controller

FEATURES

- Drives Power MOSFETs or Power Darlingtons Directly
- 50V Open Collector High-Side Drivers
- Latched Soft Start
- High-speed Current-Sense Amplifier with Ideal Diode
- Pulse-by-Pulse and Average Current Sensing
- Over-Voltage and Under-Voltage Protection
- Direction Latch for Safe Direction Reversal
- Tachometer
- Trimmed Reference Sources 30mA
- Programmable Cross-Conduction Protection
- Two-Quadrant and Four-Quadrant Operation

DESCRIPTION

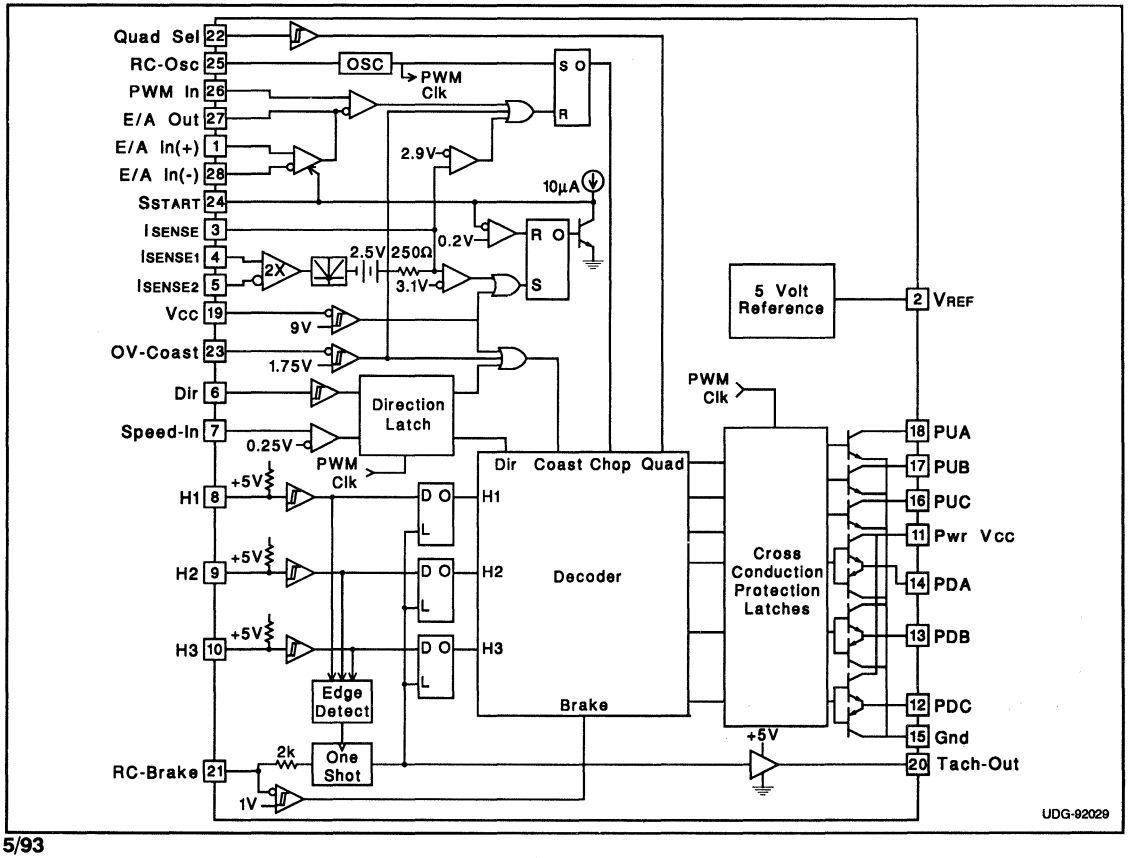
The UC1625 and UC3625 motor controller ICs integrate most of the functions required for high-performance brushless DC motor control into one package. When coupled with external power MOSFETs or Darlingtons, these ICs perform fixed-frequency PWM motor control in either voltage or current mode while implementing closed loop speed control and braking with smart noise rejection, safe direction reversal, and cross–conduction protection.

Although specified for operation from power supplies between 10V and 18V, the UC1625 can control higher voltage power devices with external level-shifting components. The UC1625 contains fast, high-current push-pull drivers for low-side power devices and 50V open-collector outputs for high-side power devices or level shifting circuitry.

The UC1625 is characterized for operation over the military temperature range of -55°C to +125°C, while the UC3625 is characterized from 0°C to 70°C.

NOTE: ESD Protection to 2kV

BLOCK DIAGRAM



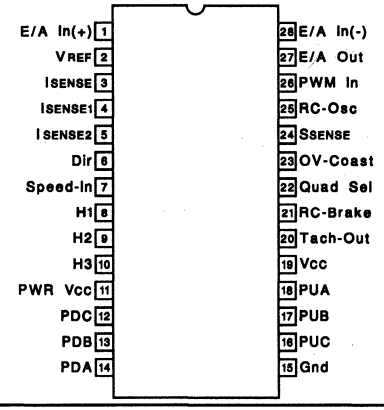
ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage ..... +20V
Pwr Vcc Supply Voltage ..... +20V
PWM In ..... -0.3 to 6V
E/A IN(+), E/A IN(–) ..... -0.3 to 12V
ISENSE1, ISENSE2 ..... -1.3 to 6V
OV–Coast, Dir, Speed-In, H1, H2, H3,
SSTART, Quad Sel ..... -0.3 to 8V
PU Output Voltage ..... -0.3 to 50V
PU Output Current ..... +200 mA continuous
PD Output Current ..... ±200 mA continuous
E/A Output Current ..... ±10 mA
I SENSE Output Current ..... -10 mA
Tach Out Output Current ..... ±10 mA
VREF Output Current ..... -50 mA continuous
Operating Temperature Range UC1625 ..... -55°C to 125°C
Operating Temperature Range UC3625 ..... 0°C to 70°C

Note 1: Currents are positive into and negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAM

DIL-28 (TOP VIEW)
J or N PACKAGE



Note 3: This pinout applies to the SOIC (DW), PLCC (Q), and LCC (L) packages (ie. pin 22 has the same function on all packages.)

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for: TA = 25°C; Pwr Vcc = Vcc = 12V; ROSC = 20k to VREF; COSC = 2nF; RTACH = 33k; CTACH = 10nF; and all outputs unloaded. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply current	Over Operating Range		14.5	30.0	mA
Vcc Turn-On Threshold	Over Operating Range	8.65	8.95	9.45	V
Vcc Turn-Off Threshold	Over Operating Range	7.75	8.05	8.55	V
Overvoltage/Coast					
OV-Coast Inhibit Threshold	Over Operating Range	1.65	1.75	1.85	V
OV-Coast Restart Threshold		1.55	1.65	1.75	V
OV-Coast Hysteresis		0.05	0.10	0.15	V
OV-Coast Input Current		-10	-1	0	µA
Logic Inputs					
H1, H2, H3 Low Threshold	Over Operating Range	0.8	1.0	1.2	V
H1, H2, H3 High Threshold	Over Operating Range	1.6	1.9	2.0	V
H1, H2, H3 Input Current	Over Operating Range, to 0V	-400	-250	-120	µA
Quad Sel, Dir Thresholds	Over Operating Range	0.8	1.4	2.0	V
Quad Sel, Dir Hysteresis			70		mV
Quad Sel Input Current		-30	50	150	µA
Dir Input Current		-30	-1	30	µA
PWM Amp/Comparator					
E/A In(+), E/A In(-) Input Current	To 2.5V	-5.0	-0.1	5.0	µA
PWM In Input Current	To 2.5V	0	3	30	µA
Error Amp Input Offset	0V < VCOMMON-MODE < 3V	-10		10	mV
Error Amp Voltage Gain		70	90		dB
E/A Out Range		0.25		3.50	V
SSTART Pull-up Current	To 0V	-16	-10	-5	µA
SSTART Discharge Current	To 2.5V	0.1	0.4	3.0	mA
SSTART Restart Threshold		0.1	0.2	0.3	V
Gain	ISENSE1 = .3V, ISENSE2 = .5V to .7V	1.75	1.95	2.15	V/V
Level Shift	ISENSE1 = .3V, ISENSE2 = .3V	2.4	2.5	2.65	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for: T_A = 25°C; PWR-Vcc = Vcc = 12V; Rosc = 20k to V_{REF}; Cosc = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amp (cont.)					
Peak Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.14	0.20	0.26	V
Over Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.26	0.30	0.36	V
I_{SENSE1}, I_{SENSE2} Input Current	To 0V	-850	-320	0	µA
I_{SENSE1}, I_{SENSE2} Offset Current	To 0V		±2	±12	µA
Range I_{SENSE1}, I_{SENSE2}		-1		2	V
Tachometer/Brake					
Tach-Out High Level	Over Operating Range, 10k to 2.5V	4.7	5	5.3	V
Tach-Out Low Level	Over Operating Range, 10k to 2.5V			0.2	V
On Time		170	220	280	µs
On Time Change With Temp	Over Operating Range		.1		%
RC-Brake Input Current	To 0V	-4.0	-1.9		mA
Threshold to Brake, RC-Brake	Over Operating Range	0.8	1.0	1.2	V
Brake Hysteresis, RC-Brake			0.09		V
Speed-In Threshold	Over Operating Range	220	257	290	mV
Speed-In Input Current		-30	-5	30	µA
Low-Side Drivers					
Voh, -1mA, Down From Vcc	Over Operating Range		1.60	2.1	
V Voh, -50mA, Down From Vcc	Over Operating Range		1.75	2.2	V
Vol, 1mA	Over Operating Range		0.05	0.4	V
Vol, 50mA	Over Operating Range		0.36	0.8	V
Rise/Fall Time	10% to 90% Slew Time, into 1nF		50		ns
High-Side Drivers					
Vol, 1mA	Over Operating Range		0.1	0.4	V
Vol, 50mA	Over Operating Range		1.0	1.8	V
Leakage Current	Output Voltage = 50V			25	µA
Fall Time	10% to 90% Slew Time, 50mA Load		50		ns
Oscillator					
Frequency		40	50	60	kHz
Frequency	Over Operating Range	35		65	kHz
Reference					
Output Voltage		4.9	5.0	5.1	V
Output Voltage	Over Operating Range	4.7	5.0	5.3	V
Load Regulation	0mA to -20mA Load	-40	-5		mV
Line Regulation	10V to 18V Vcc	-10	-1	10	mV
Short Circuit Current	Over Operating Range	50	100	150	mA
Miscellaneous					
Output Turn-On Delay			1		µs
Output Turn-Off Delay			1		µs

PIN DESCRIPTIONS:

Dir, Speed-In: The position decoder logic translates the Hall signals and the Dir signal to the correct driver signals (PUs and PDs). To prevent output stage damage, the signal on Dir is first loaded into a direction latch, then shifted through a two-bit register.

As long as Speed-In is less than 250mV, the direction latch is transparent. When Speed-In is higher than 250mV, the direction latch inhibits all changes in direction. Speed-In can be connected to Tach-Out through a filter, so that the direction latch is only transparent when the motor is spinning slowly, and has too little stored energy to damage power devices.

PIN DESCRIPTIONS (cont.):

Additional circuitry detects when the input and output of the direction latch are different, or when the input and output of the shift register are different, and inhibits all output drives during that time. This can be used to allow the motor to coast to a safe speed before reversing.

The shift register guarantees that direction can't be changed instantaneously. The register is clocked by the PWM oscillator, so the delay between direction changes is always going to be between one and two oscillator periods. At 40kHz, this corresponds to a delay of between 25µs and 50µs. Regardless of output stage, 25µs dead time should be adequate to guarantee no overlap cross-conduction.

E/A In(+), E/A In(-), E/A Out, PWM In: E/A In(+) and E/A In(-) are not internally committed to allow for a wide variety of uses. They can be connected to the ISENSE, to Tach-Out through a filter, to an external command voltage, to a D/A converter for computer control, or to another op amp for more elegant feedback loops. The error amplifier is compensated for unity gain stability, so E/A Out can be tied to E/A In(-) for feedback and major loop compensation.

E/A Out and PWM In drive the PWM comparator. For voltage-mode PWM systems, PWM In can be connected to RC-Osc. The PWM comparator clears the PWM latch, commanding the outputs to chop.

The error amplifier can be biased off by connecting E/A In(-) to a higher voltage than E/A In(+). When biased off, E/A Out will appear to the application as a resistor to ground. E/A Out can then be driven by an external amplifier.

GND: All thresholds and outputs are referred to the GND pin except for the PD and PU outputs.

H1, H2, H3: The three shaft-position sensor inputs consist of hysteresis comparators with input pull-up resistors. Logic thresholds meet TTL specifications and can be driven by 5V CMOS, 12V CMOS, NMOS, or open-collectors.

Connect these inputs to motor shaft position sensors that are positioned 120 electrical degrees apart. If noisy signals are expected, zener clamp and filter these inputs with 6V zeners and an RC filter. Suggested filtering components are 1k and 2nF. Edge skew in the filter is not a problem, because sensors normally generate modified Gray code with only one output changing at a time, but rise and fall times must be shorter than 20µs for correct tachometer operation.

Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals is inverted.

ISENSE1, ISENSE2, ISENSE: The current sense amplifier has a fixed gain of approximately two. It also has a built-in level shift of approximately 2.5 volts. The signal appearing on ISENSE is:

$$I_{SENSE} = 2.5V + (2 * ABS (I_{SENSE1} - I_{SENSE2}))$$

ISENSE1 and ISENSE2 are interchangeable and can be used as differential inputs. The differential signal applied can be as high as ±0.5V before saturation.

If spikes are expected on ISENSE1 or ISENSE2, they are best filtered by a capacitor from ISENSE to ground. Filtering this way allows fast signal inversions to be correctly processed by the absolute value circuit. The peak-current comparator allows the PWM to enter a current-limit mode with current in the windings never exceeding approximately 0.2V/RSENSE. The over current comparator provides a fail-safe shutdown in the unlikely case of current exceeding 0.3V/RSENSE. Then, soft start is commanded, and all outputs are turned off until the high current condition is removed.

It is often essential to use some filter driving ISENSE1 and ISENSE2 to reject extreme spikes and to control slew rate. Reasonable starting values for filter components might be 250Ω series resistors and a 5nF capacitor between ISENSE1 and ISENSE2. Input resistors should be kept small and matched to maintain gain accuracy.

OV-Coast: This input can be used as an over-voltage shutdown in put, as a coast input, or both. This input can be driven by TTL, 5V CMOS, or 12V CMOS.

PDA, PDB, PDC: These outputs can drive the gates of N-Channel power MOSFETs directly or they can drive the bases of power Darlingtons if some form of current limiting is used. They are meant to drive low-side power devices in high-current output stages. Current available from these pins can peak as high as 0.5A. These outputs feature a true totem-pole output stage. Beware of exceeding IC power dissipation limits when using these outputs for high continuous currents. These outputs pull high to turn a "low-side" device on (active high).

PUA, PUB, PUC: These outputs are open-collector, high-voltage drivers that are meant to drive high-side power devices in high-current output stages. These are active low outputs, meaning that these outputs pull low to command a high-side device on. These outputs can drive low-voltage PNP Darlingtons and P-channel MOSFETs directly, and can drive any high-voltage device using external charge-pump techniques, transformer signal coupling, cascode level-shift transistors, or opto-isolated drive. (See applications).

PWR Vcc: This supply pin carries the current sourced by the PD outputs. When connecting PD outputs directly to the bases of power Darlingtons, the PWR Vcc pin can be current limited with a resistor. Darlington outputs can also be "Baker Clamped" with diodes from collectors back to PWR Vcc. (See Applications)

PIN DESCRIPTIONS (cont.):

Quad Sel: The IC can chop power devices in either of two modes, referred to as "two-quadrant" (Quad Sel low) and "four-quadrant" (Quad Sel high). When two-quadrant chopping, the pull-down power devices are chopped by the output of the PWM latch while the pull-up drivers remain on. The load will chop into one commutation diode, and except for back-EMF, will exhibit slow discharge current and faster charge current. Two-quadrant chopping can be more efficient than four-quadrant.

When four-quadrant chopping, all power drivers are chopped by the PWM latch, causing the load current to flow into two diodes during chopping. This mode exhibits better control of load current when current is low, and is preferred in servo systems for equal control over acceleration and deceleration. The Quad Sel input has no effect on operation during braking.

RC-Brake: Each time the Tach-Out pulses, the capacitor tied to RC-Brake discharges from approximately 3.33V down to 1.67V through a resistor. The tachometer pulse width is approximately T = 0.67 R_T C_T, where R_T and C_T are a resistor and capacitor from RC-Brake to ground. Recommended values for R_T are 10k to 500k, and recommended values for C_T are 1nF to 100nF, allowing times between 5µs and 10ms. Best accuracy and stability are achieved with values in the centers of those ranges.

RC-Brake also has another function. If RC-Brake pin is pulled below the brake threshold, the IC will enter brake mode. This mode consists of turning off all three high-side devices, enabling all three low-side devices, and disabling the tachometer. The only things that inhibit low-side device operation in braking are low-supply, exceeding peak current, OV-Coast command, and the PWM comparator signal. The last of these means that if current sense is implemented such that the signal in the current sense amplifier is proportional to braking current, the low-side devices will brake the motor with current control. (See applications) Simpler current sense connections will result in uncontrolled braking and potential damage to the power devices.

RC-Osc: The UC3625 can regulate motor current using fixed-frequency pulse width modulation (PWM). The RC-Osc pin sets oscillator frequency by means of timing resistor R_{OSC} from the RC-Osc pin to V_{REF} and capacitor C_{OSC} from RC-Osc to Gnd. Resistors 10k to 100k and capacitors 1nF to 100nF will work best, but frequency should always be below 500kHz. Oscillator frequency is approximately:

$$F = 2 / R_{OSC} C_{OSC}$$

Additional components can be added to this device to cause it to operate as a fixed off-time PWM rather than a fixed frequency PWM, using the RC-Osc pin to select the monostable time constant.

The voltage on the RC-Osc pin is normally a ramp of about 1.2V peak-to-peak, centered at approximately 1.6V. This ramp can be used for voltage-mode PWM control, or can be used for slope compensation in current-mode control.

S_{START}: Any time that V_{CC} drops below threshold or the sensed current exceeds the over-current threshold, the soft-start latch is set. When set, it turns on a transistor that pulls down on S_{START}. Normally, a capacitor is connected to this pin, and the transistor will completely discharge the capacitor. A comparator senses when the NPN transistor has completely discharged the capacitor, and allows the soft-start latch to clear when the fault is removed. When the fault is removed, the soft-start capacitor will charge from the on-chip current source.

S_{START} clamps the output of the error amplifier, not allowing the error amplifier output voltage to exceed S_{START} regardless of input. The ramp on RC-Osc can be applied to PWM In and compared to E/A Out. With S_{START} discharged below 0.2V and the ramp minimum being approximately 1.0V, the PWM comparator will keep the PWM latch cleared and the outputs off. As S_{START} rises, the PWM comparator will begin to duty-cycle modulate the PWM latch until the error amplifier inputs overcome the clamp. This provides for a safe and orderly motor start-up from an off or fault condition.

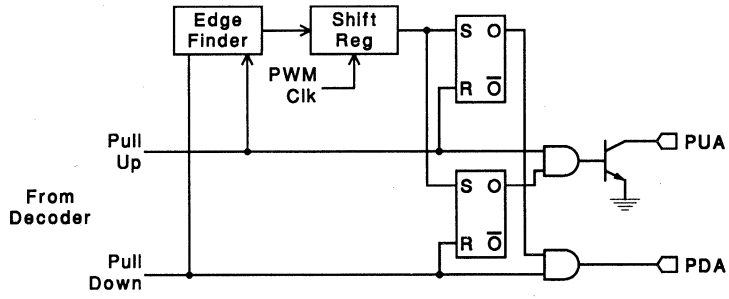
Tach-Out: Any change in the H1, H2, or H3 inputs loads data from these inputs into the position sensor latches. At the same time data is loaded, a fixed-width 5V pulse is triggered on Tach-Out. The average value of the voltage on Tach-Out is directly proportional to speed, so this output can be used as a true tachometer for speed feedback with an external filter or averaging circuit.

Whenever Tach-Out is high, the position latches are inhibited, such that during the noisiest part of the commutation cycle, additional commutations are not possible. Although this will effectively set a maximum rotational speed, the maximum speed can be set above the highest expected speed, preventing false commutation and chatter.

V_{CC}: This device operates with supplies between 10V and 18V. Under-voltage lockout keeps all outputs off below 7.5V, insuring that the output transistors never turn on until full drive capability is available. Bypass V_{CC} to ground with an 0.1µF ceramic capacitor. Using a 10µF electrolytic bypass capacitor as well can be beneficial in applications with high supply impedance.

V_{REF}: This pin provides regulated 5 volts for driving Hall-effect devices and speed control circuitry. V_{REF} will reach +5V before V_{CC} enables, ensuring that Hall-effect devices powered from V_{REF} will become active before the UC3625 drives any output. Although V_{REF} is current limited, operation over 30mA is not advised.

CROSS CONDUCTION PREVENTION



The UC3625 inserts delays to prevent cross conduction due to overlapping drive signals. However, some thought must always be given to cross conduction in output stage design because no amount of dead time can prevent fast slewing signals from coupling drive to a power device through a parasitic capacitance.

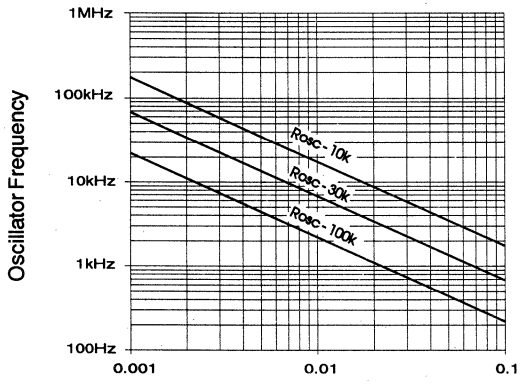
The UC3625 contains input latches that serve as noise blanking filters. These latches remain transparent through any phase of a motor rotation and latch immediately after an input transition is detected. They remain latched for two cycles of the PWM oscillator. At a PWM oscillator speed of 20kHz, this corresponds to 50µs to 100µs of blank time which limits maximum rotational speed to 100kRPM for a motor with six transitions per rotation or 50kRPM for a motor with 12 transitions per rotation.

This prevents noise generated in the first 50µs of a transition from propagating to the output transistors and causing cross–conduction or chatter.

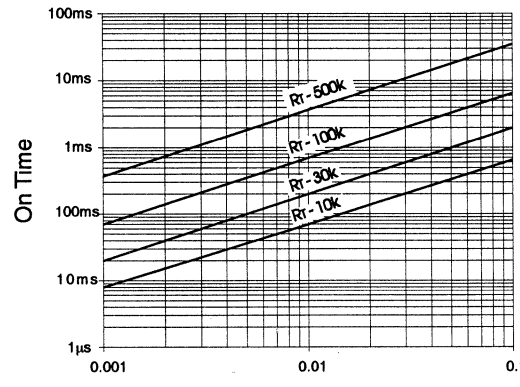
The UC3625 also contains six flip flops corresponding to the six output drive signals. One of these flip flops is set every time that an output drive signal is turned on, and cleared two PWM oscillator cycles after that drive signal is turned off. The output of each flip flop is used to inhibit drive to the opposing output. (see below) In this way, it is impossible to turn on driver PUA and PDA at the same time. It is also impossible for one of these drivers to turn on without the other driver having been off for at least two PWM oscillator clocks.

TYPICAL CHARACTERISTICS:

Oscillator Frequency vs Cosc and Rosc

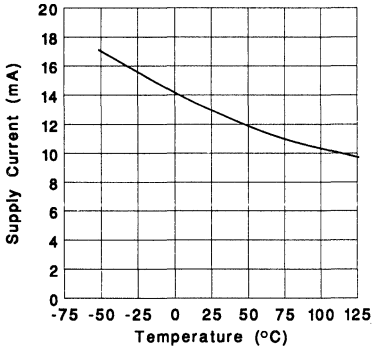


Tachometer On Time vs RT and CT

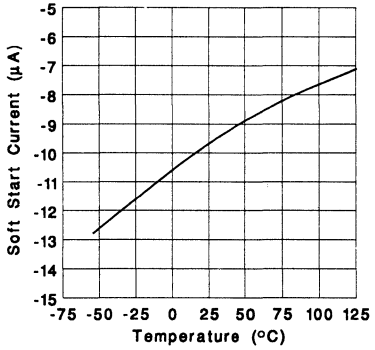


TYPICAL CHARACTERISTICS (cont.):

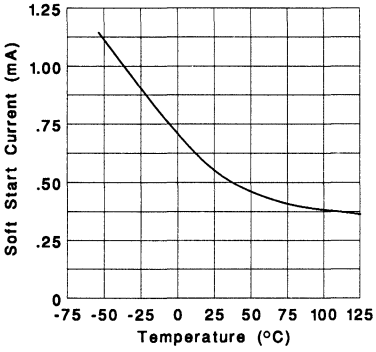
Supply Current vs Temperature



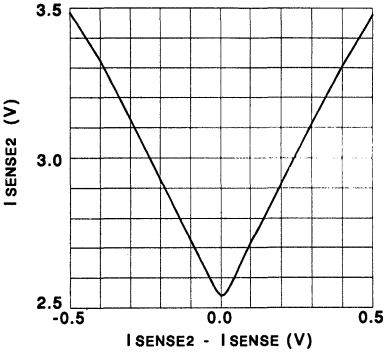
Soft Start Pull-Up Current vs Temperature



Soft Start Discharge Current vs Temperature



Current Sense Amplifier Transfer Function



POWER STAGE DESIGN:

The UC3625 is useful in a wide variety of applications, including high-power in robotics and machinery. The power output stages used in such equipment can take a number of forms, according to the intended performance and purpose of the system. Below are four different power stages with the advantages and disadvantages of each shown.

For high-frequency chopping, fast recovery circulating diodes are essential. Six are required to clamp the windings. These diodes should have a continuous current rating at least equal to the operating motor current, since diode conduction duty-cycle can be high. For low-voltage systems, Schottky diodes are preferred. In higher voltage systems, diodes such as Microsemi UHVP high voltage platinum rectifiers are recommended.

In a pulse-by-pulse current control arrangement, current sensing is done by resistor R_T, through which the transistor's currents are passed (Figures A, B, and C). In these cases, R_D is not needed. The low-side circulating diodes go to ground and the current sense terminals of the UC3625 (I_{SENSE1} and I_{SENSE2}) are connected to R_T through an R_C filter. The input bias current of the current sense amplifier will cause a common mode offset voltage to appear at both inputs, so for best accuracy, keep the filter resistors below 2k and matched.

The current that flows through R_T is discontinuous because of chopping. It flows during the on time of the power stage and is zero during the off time. Consequently, the voltage across R_T consists of a series of pulses, occurring at the PWM frequency, with a peak value indicative of the peak motor current.

To sense average motor current instead of peak current, add another current sense resistor (R_D in Figure D) to measure current in the low-side circulating diodes, and operate in four quadrant mode (pin 22 high). The negative voltage across R_D is corrected by the absolute value current sense amplifier. Within the limitations imposed by Table 1, the circuit of Figure B can also sense average current.

POWER STAGE DESIGN (cont.):

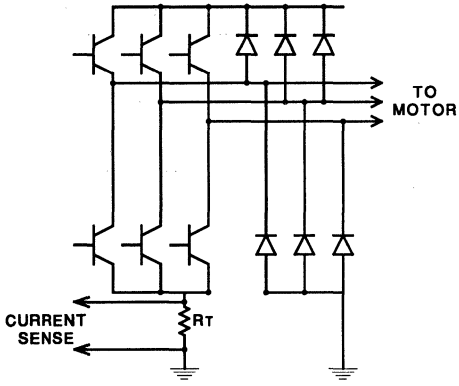


FIGURE A

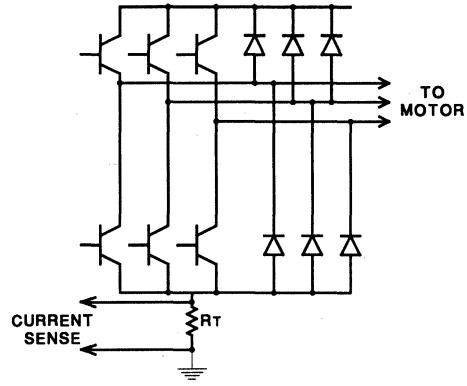


FIGURE B

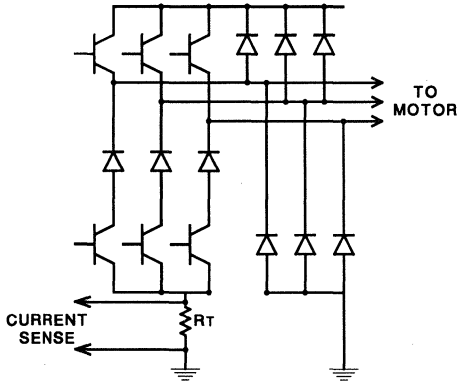


FIGURE C

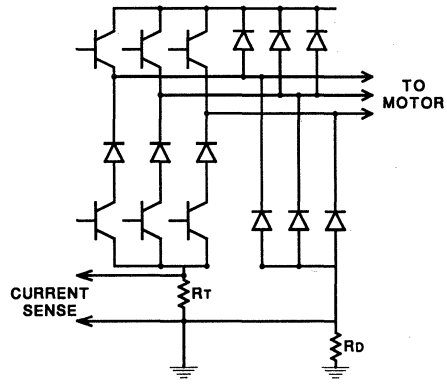
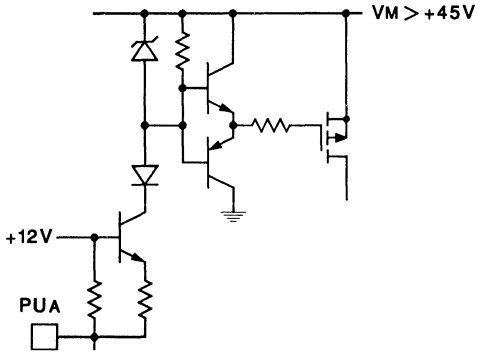


FIGURE D

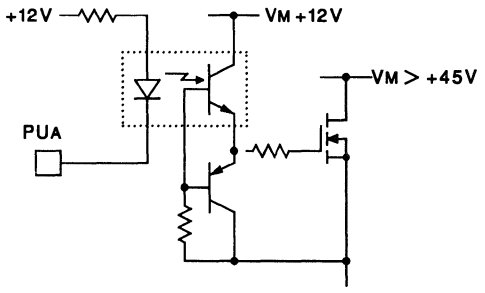
	2 QUADRANT	4 QUADRANT	SAFE BRAKING	POWER REVERSE	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
FIGURE A	YES	NO	NO	NO	YES	NO
FIGURE B	YES	YES	NO	IN 4QUAD MODE ONLY	YES	YES
FIGURE C	YES	YES	YES	IN 4QUAD MODE ONLY	YES	NO
FIGURE D	YES	YES	YES	IN 4QUAD MODE ONLY	YES	YES

Fast High-Side P-Channel Driver



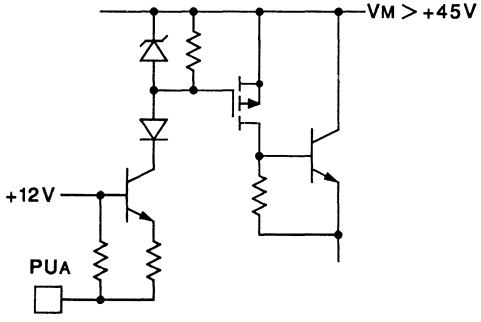
For drives where speed is critical, P-Channel MOSFETs can be driven by emitter followers. Here, both the level shift NPN and the PNP must withstand high voltages. A zener diode is used to limit gate-source voltage on the MOSFET. A series gate resistor is not necessary, but always advisable to control overshoot and ringing.

Optocoupled N-Channel High-Side Driver



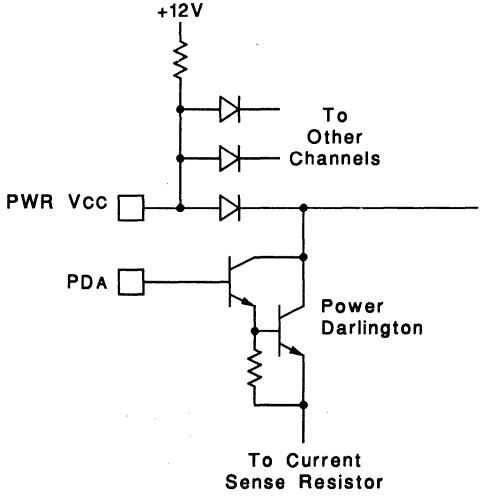
High-voltage optocouplers can quickly drive high-voltage MOSFETs if a boost supply of at least 10 volts greater than the motor supply is provided. To protect the MOSFET, the boost supply should not be higher than 18 volts above the motor supply.

Power NPN High-Side Driver



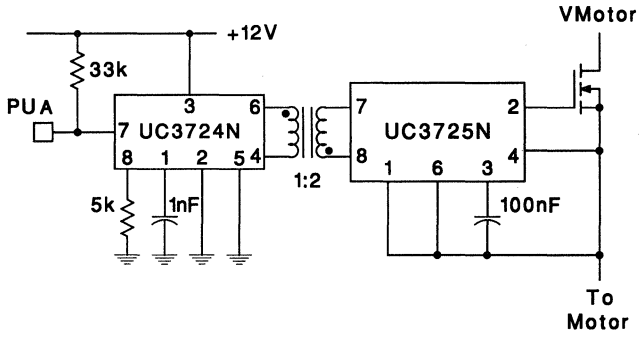
For under 200V 2-quadrent applications, a power NPN driven by a small P-Channel MOSFET will perform well as a high-side driver. A high voltage small-signal NPN is used as a level shift and a high voltage low-current MOSFET provides drive. Although the NPN will not saturate if used within its limitations, the base-emitter resistor on the NPN is still the speed limiting component.

Power NPN Low-Side Driver



This power NPN Darlington drive technique uses a clamp to prevent deep saturation. By limiting saturation of the power device, excessive base drive is minimized and turn-off time is kept fairly short. Lack of base series resistance also adds to the speed of this approach.

Fast High-Side N-Channel Driver with Transformer Isolation



A small pulse transformer can provide excellent isolation between the UC3625 and a high-voltage N-Channel MOSFET while also coupling gate drive power. In this circuit, a UC3724 is used as a transformer driver/encoder that duty-cycle modulates the transformer with a 150kHz pulse train. The UC3725 rectifies this pulse train for gate drive power, demodulates the signal, and drives the gate with over 2 amp peak current.

Both the UC3724 and the UC3725 can operate up to 500kHz if the pulse transformer is selected appropriately. To raise the operating frequency, either lower the timing resistor of the UC3724 (1k minimum), lower the timing capacitor of the UC3724 (500pF minimum) or both.

If there is significant capacitance between transformer primary and secondary, together with very high output slew rate, then it may be necessary to add clamp diodes from the transformer primary to +12V and ground. Signal diodes such as 1N4148 are normally adequate.

The UC3725 also has provisions for MOSFET current limiting. Consult the UC3725 data sheet for more information on implementing this.

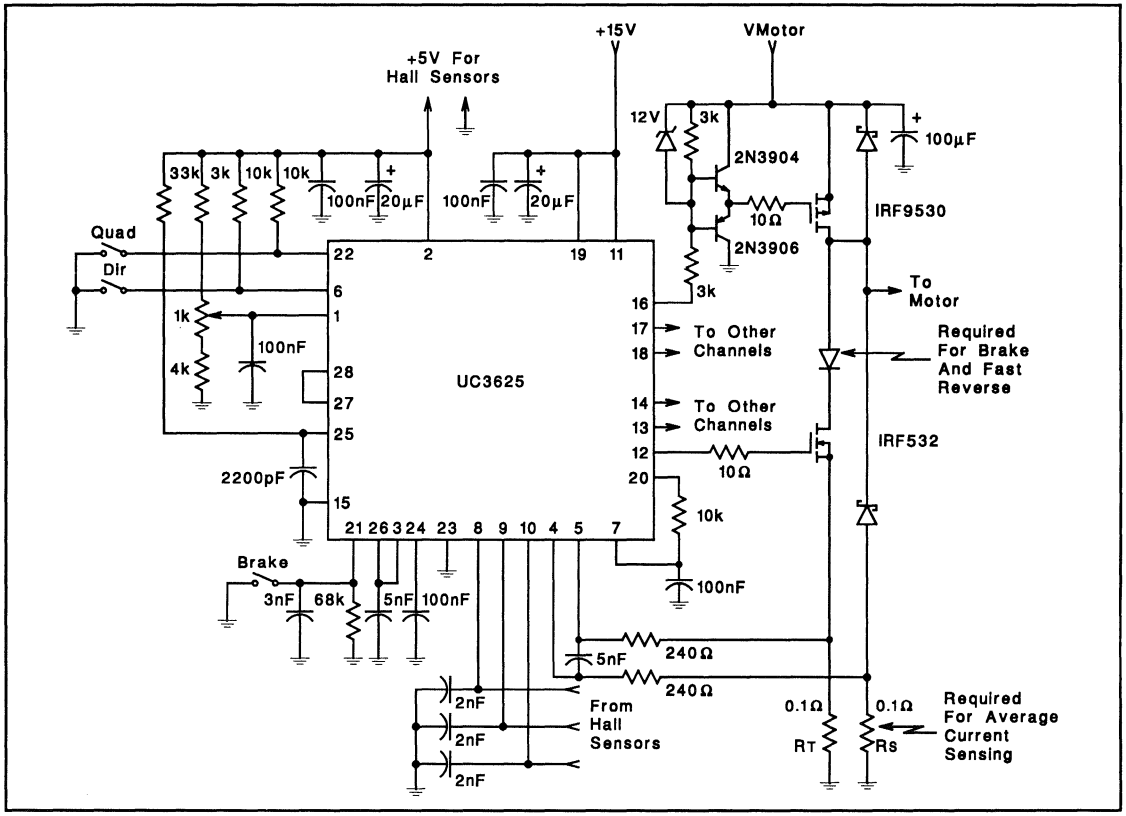
COMMUTATION TRUTH TABLE

This table shows the outputs of the gate drive and open collector outputs for given hall input codes and direction signals. Numbers at the top of the columns are pin numbers.

These ICs operate with position sensor encoding that has either one or two signals high at a time, never all low or all high. This coding is sometimes referred to as "120° Coding" because the coding is the same as coding with position sensors spaced 120 magnetic degrees about the rotor. In response to these position sense signals, only one low-side driver will turn on (go high) and one high-side driver will turn on (pull low) at any time.

INPUTS				OUTPUTS					
DIR	H1	H2	H3	Low-Side			High-Side		
6	8	9	10	12	13	14	16	17	18
1	0	0	1	L	H	L	L	H	H
1	0	1	1	L	L	H	L	H	H
1	0	1	0	L	L	H	H	L	H
1	1	1	0	H	L	L	H	L	H
1	1	0	0	H	L	L	H	H	L
1	1	0	1	L	H	L	H	H	L
0	1	0	1	L	L	H	H	L	H
0	1	0	0	L	L	H	L	H	H
0	1	1	0	L	H	L	L	H	H
0	0	1	0	L	H	L	H	H	L
0	0	1	1	H	L	L	H	H	L
0	0	0	1	H	L	L	H	L	H
X	1	1	1	L	L	L	H	H	H
X	0	0	0	L	L	L	H	H	H

TYPICAL APPLICATION: A 45V/8A Brushless DC Motor Drive Circuit



N–Channel power MOSFETs are used for low–side drivers, while P–Channel power MOSFETs are shown for high–side drivers. Resistors are used to level shift the UC3625 open–collector outputs, driving emitter followers into the MOSFET gate. A 12V zener clamp insures that the MOSFET gate–source voltage will never exceed 12V. Series 10Ω gate resistors tame gate reactance, preventing oscillations and minimizing ringing.

The oscillator timing capacitor should be placed close to pins 15 and 25, to keep ground current out of the capacitor. Ground current in the timing capacitor causes oscillator distortion and slaving to the commutation signal.

The potentiometer connected to pin 1 controls PWM duty cycle directly, implementing a crude form of speed control. This control is often referred to as "voltage mode" because the potentiometer position sets the average motor voltage. This controls speed because steady–state motor speed is closely related to applied voltage.

Pin 20 (Tach-Out) is connected to pin 7 (SPEED IN) through an RC filter, preventing direction reversal while the motor is spinning quickly. In two–quadrant operation, this reversal can cause kinetic energy from the motor to be forced into the power MOSFETs.

A diode in series with the low-side MOSFETs facilitates PWM current control during braking by insuring that braking current will not flow backwards through low–side MOSFETs. Dual current–sense resistors give continuous current sense, whether braking or running in four–quadrant operation, an unnecessary luxury for two–quadrant operation.

The 68k ohm and 3nF tachometer components set maximum commutation time at 140µs. This permits smooth operation up to 35,000 RPM for four–pole motors, yet gives 140µs of noise blanking after commutation.

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INTEGRATED CIRCUITS
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UC1633
UC2633
UC3633

Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

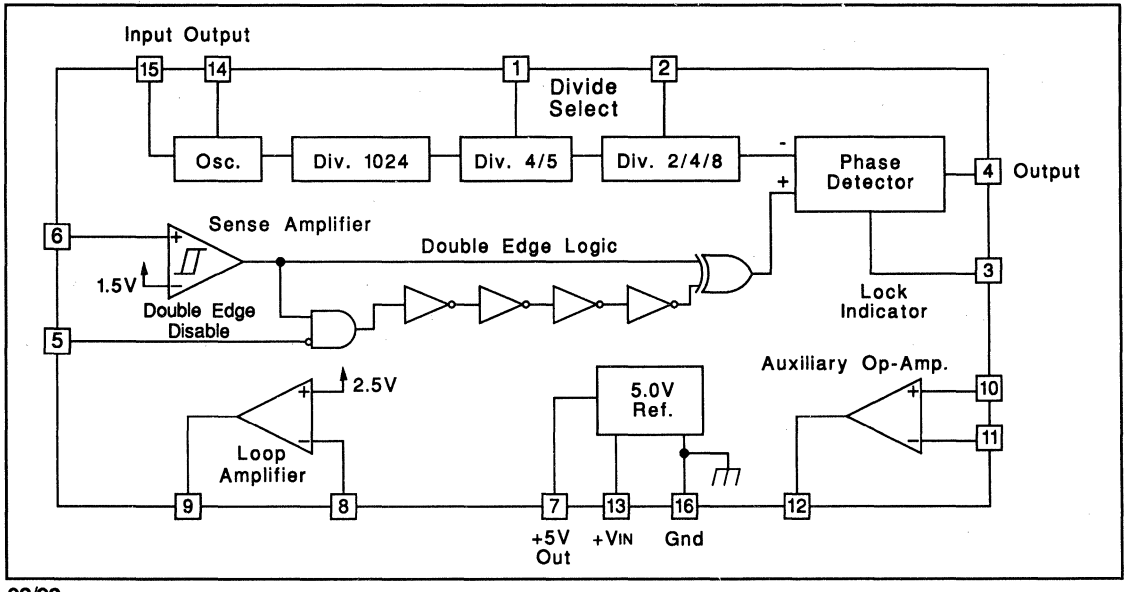
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output of other speed detection device. This signal is buffered by a sense ampilfier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of the op-amps will source or sink in excess of 16mA, so they can provide a low impedence control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM



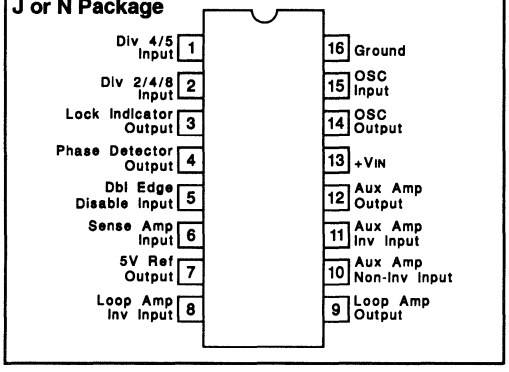
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltages ..... -.3V to +10V
Double Edge Disable Input Voltage ..... -.3V to +10V
Oscillator Input Voltage ..... -.3V to +5V
Sense Amplifier Input Voltage ..... .3V to +20V
Power Dissipation at TA = 25°C (Note 2 ..... 1000mW
Power dissipation at Tc = 25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

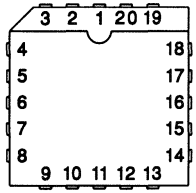
Note1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 4/5 Input	2
Div 2/4/8 Input	3
Lock Indicator Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for TA = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, +VIN = 12V; TA=TJ.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0V to 7mA		5.0	20	mV
Line Regulation	+VIN = 8V to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (VIB)	Oscillator Input Pin Open, TJ = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	VIN = VIB ±0.5V, TJ = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, TJ = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1VPP at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA
Div. 4/5 Threshold		0.5	1.6	2.2	V

Note 3: These impedence levels will vary with TJ at about 1700ppm/°C

ELECTRICAL CHARACTERISTICS (cont.): (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V; T_A=T_J.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dividers (cont.)					
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	v
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
CMRR	V_{CM} = 0V to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedence levels will vary with T_J at about 1700ppm/°C

APPLICATION AND OPERATING INFORMATION

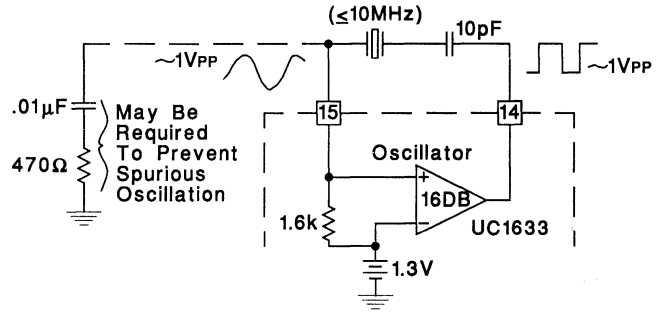
Determining the Oscillator Frequency

The frequency at the oscillator is determined by the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

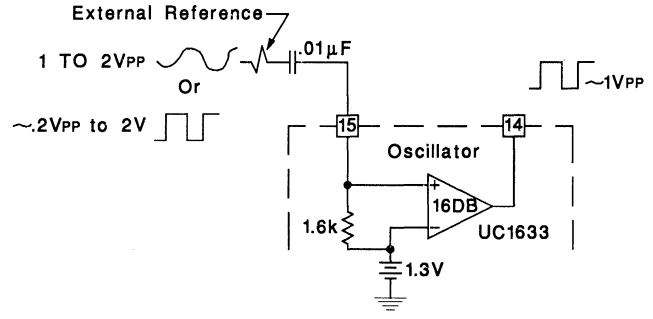
fosc(Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (x 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option, the loop reference frequency can be doubled for a given motor RPM.

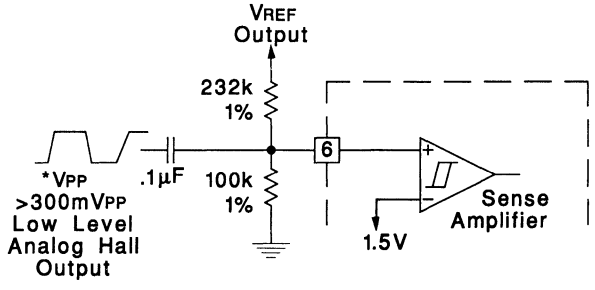
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method for Deriving Rotation Feedback Signal from Analog Hall Effect Device



**This signal may require filtering if chopped mode drive scheme is used.*

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

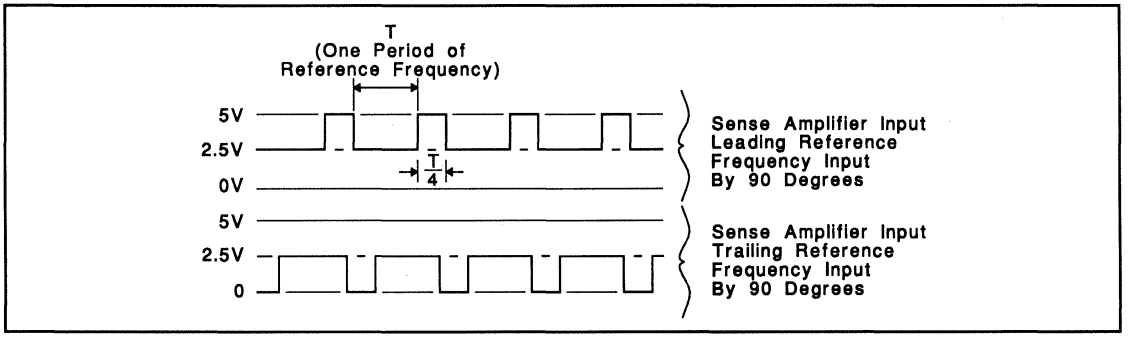
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low and the middle state output impedence is high, typically 6.0kΩ. When there is any static frequency difference between the inputs, the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal, the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level for the remainder of the period. If the phase relationship is reversed, then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector. kø, is $5V/4\pi$ radians or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

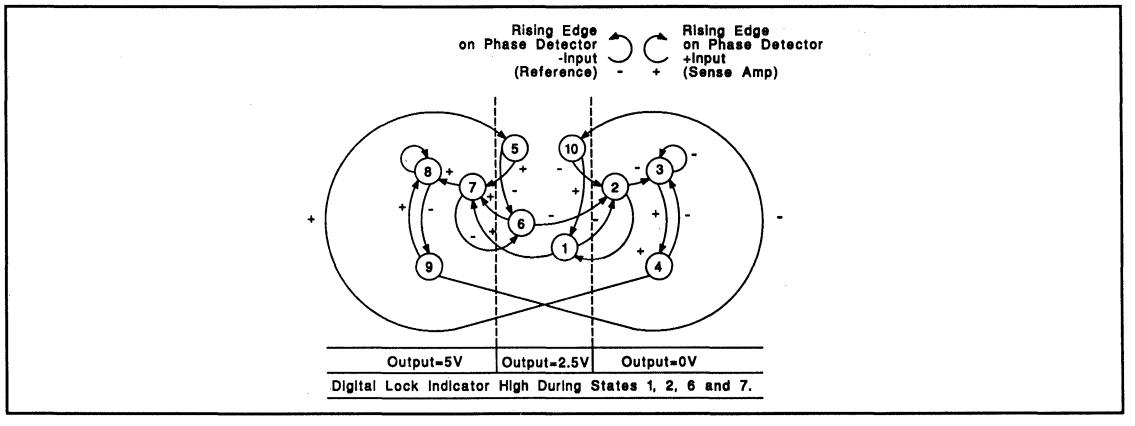
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic, and the connecting arrows represent the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge of the -input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from the frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

Typical Phase Detector Output Waveforms

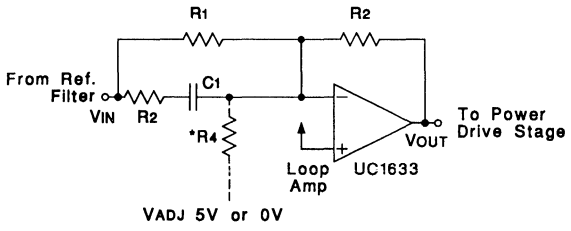


Phase Detector State Diagram



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{R_3}{R_1} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{R_2 C_1}$$

$$\omega_z = \frac{1}{(R_1 + R_2)\, C_1}$$

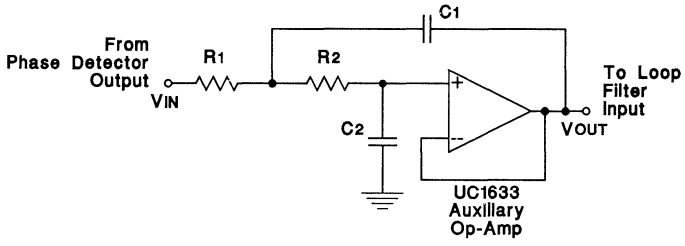
* The static phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R_4 = \frac{2.5V \cdot R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$, R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$, R4 Goes to 5.0V

Reference Filter Configuration



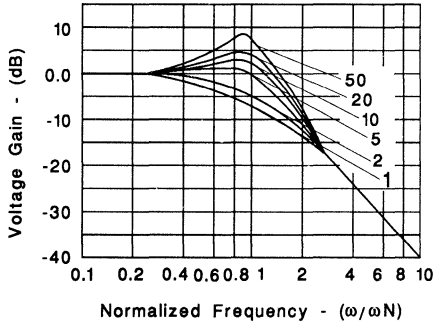
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s\,2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

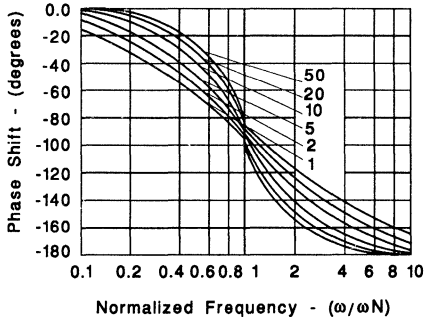
Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid - Gain Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

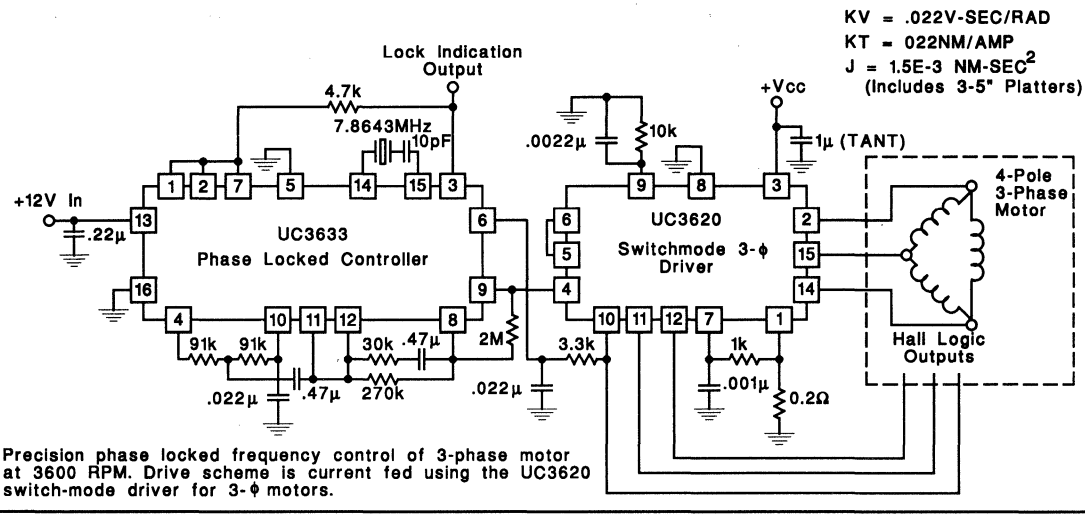
Reference Filter Design Aid - Phase Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

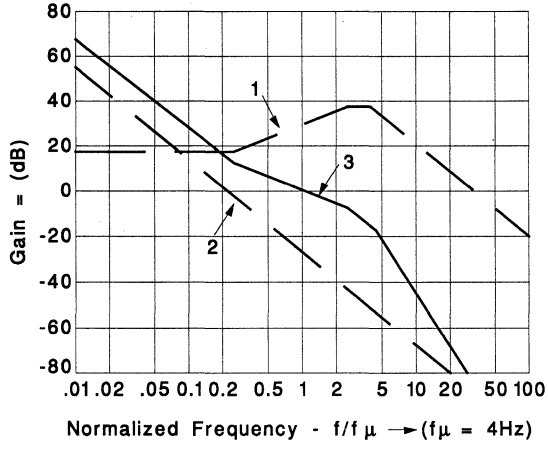
APPLICATION AND OPERATION INFORMATION

Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots - Design Example Open Loop Response



1.) $K_{LF}(s) \bullet K_{RF}(s)$

2.*) $\dfrac{N \bullet K\phi \bullet G_{PD} \bullet K_T}{s^2 \bullet J}$

3.) Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response
$K_{RF}(s)$ = Reference Filter Response
N = 4 (Using Double Edge Sensing With 4 Pole Motor)
$K\phi$ = Phase Detector Gain (.4V/RAD)
G_{PD} = Power Stage Transductance (1A/V)
K_T = Motor Torque Constant (.022NM/A)
J = Motor Moment of Inertia (.0015NM/A - SEC²)
s = 2πjf

Note: For a current mode driver the electrical time constant, L_M / R_M, of the motor does not enter into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2 above, can be approximated by:*

$$\frac{N \bullet K\phi \bullet K_{PD} \bullet K_T}{s^2 \bullet J \bullet R_M} \quad \text{if: } R_M > K_T\sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T{}^2}{2\pi \bullet J \bullet R_M} < f < \frac{R_M}{2\pi \bullet L_M}$$

Here: K_{PD} = Voltage gain of Driver Stage
R_M = Motor Winding Resistance
L_M = Motor Winding Inductance

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INTEGRATED CIRCUITS
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UC1634
UC2634
UC3634

Phase Locked Frequency Controller

FEATURES

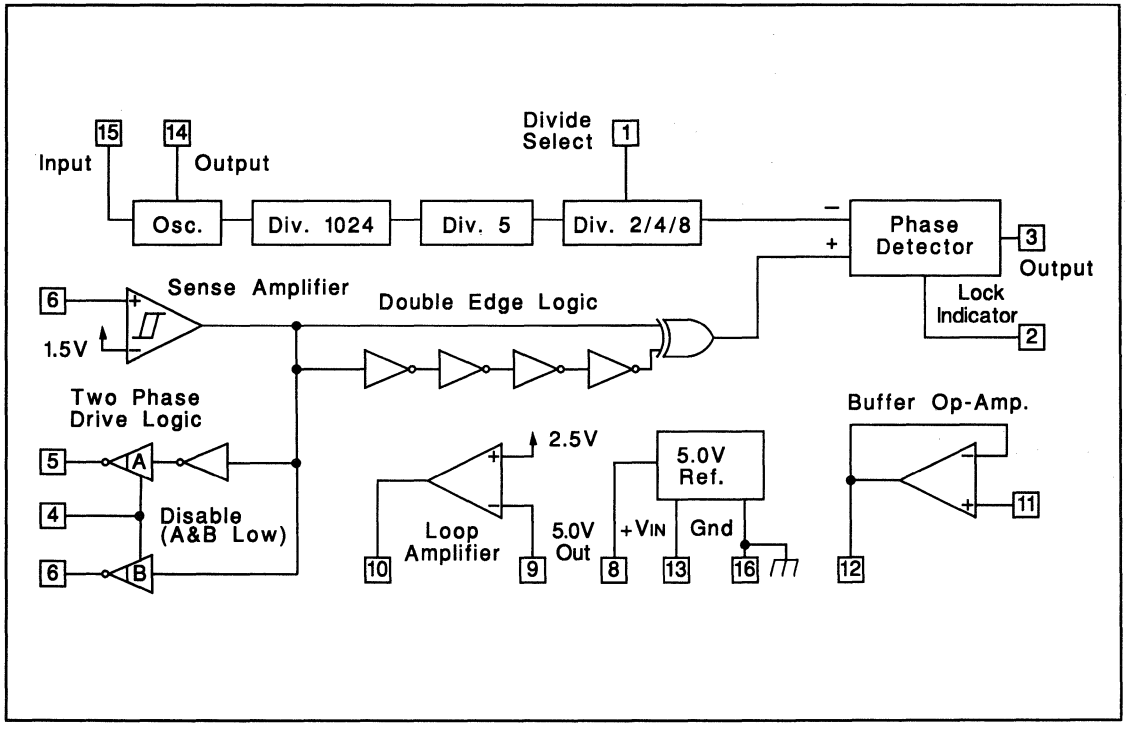
- Precision Phase Locked Frequency Control System
- Communication Logic for 2-Phase Motors
- Disable Input for Motor Inhibit
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

The UC1634 series of devices is optimized to provide precision phase locked frequency control for two phase DC brushless motors. These devices include most of the features of the general purpose UC1633 Phase Locked Control family and also provide the out-of-phase commutation signals required for driving two phase brushless motors. Only an external power booster stage is required for a complete drive and control system.

The two commutation outputs are open collector devices that can sink in excess of 16mA. A disable input allows the user to simultaneously force both of these outputs to an active low state. Double edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at Pin 7.

BLOCK DIAGRAM



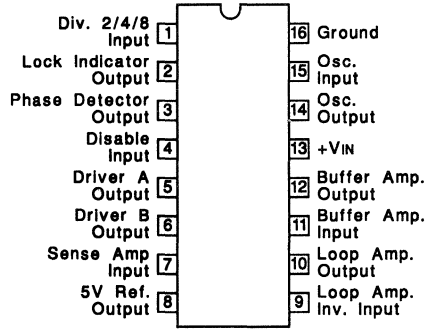
6

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltage ..... -.3V to +10V
Disable Input Voltage ..... -.3V to +10V
Oscillator Input Voltage ..... -.3V to +5V
Sense Amplifier Input Voltage ..... -.3V to +20V
Driver Output Currents ..... +30mA
Driver Output Voltages ..... +20V
Power Dissipation at T_A = 25°C(Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

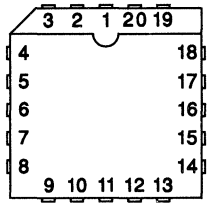
Note 1: Voltages are referenced to ground, (Pin 16, DIL Package). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
DIV 2/4/8	2
Lock Indicator Output	3
Phase Detector Output	4
Disable Input	5
N/C	6
Driver A Output	7
Driver B Output	8
Sense Amp Output	9
5V Ref Output	10
Loop Amp Inv input	11
Loop Amp Output	12
Buffer Amp Input	13
Buffer Amp Output	14
+VIN	15
N/C	16
OSC Output	17
OSC Input	18
Ground	19
DIV 4/5 Input	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, $+V_{IN}$ = 12V. T_A=T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$+V_{IN}$ = 15V		20	29	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0mA to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8V to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator In to Oscillator Out	12	16	20	dB
Input DC Level (V_{IB})	Oscillator In Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	V_{IN} = V_{IB} ± 0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator In Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1V_{PP} at Oscillator In	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
(Q Package Only, Note 4)	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, $+V_{IN}$ = 12V. T_A=T_J

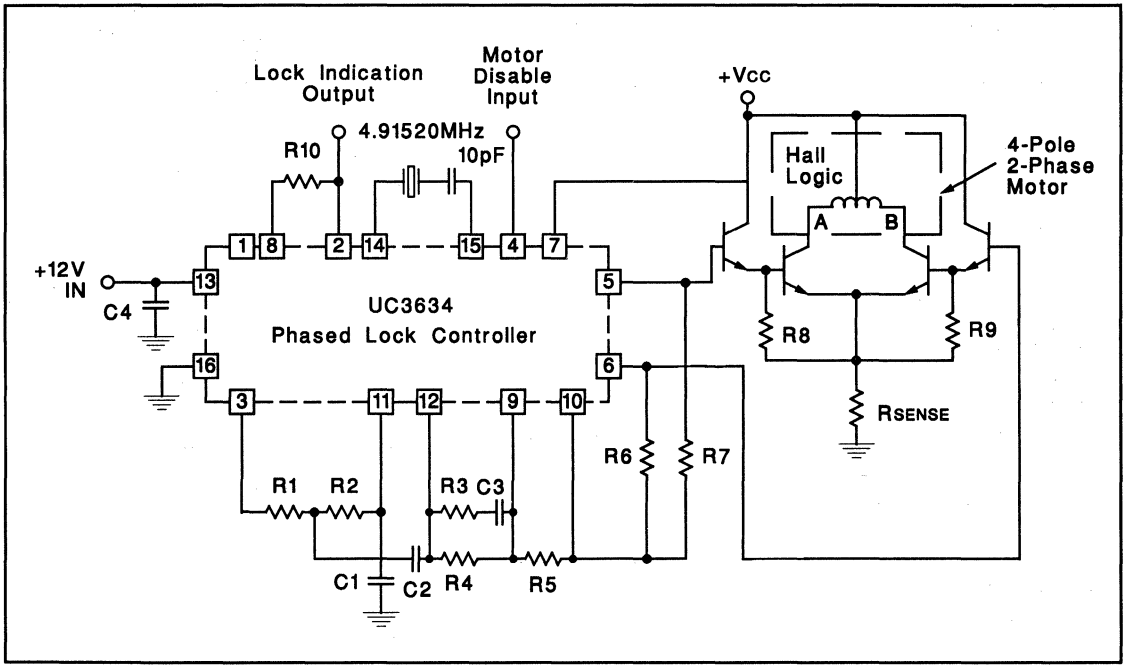
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dividers (cont.)					
Div. 4/5 Input Threshold (Q Package Only, Note 4)		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Current Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Two Phase Drive Outputs, A and B					
Saturation Voltage	I_{OUT} = 16mA		0.3	0.6	V
Leakage Current	V_{OUT} = 15V		0.1	5.0	µA
Disable Input					
Input Current	Input = 5V (Disabled, A and B Outputs Active Low)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase / Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase / Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase / Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
N INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Buffer Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.
Note 4: This part is also available in a 20 pin plastic leadless chip carrier, Q designator, where a divide by 4/5 select pin is available. Consult factory for details.

APPLICATION AND OPERATION INFORMATION (For additional information see UC1633 data sheet)

Design Example:

Precision phased locked frequency control of a 2-phase motor at 3600 RPM. Using the commutation logic on the UC3634, a simple discrete drive scheme is possible.



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Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Separate Divider Outputs and Phase Detector Input Pins
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op Amps
- 5V Reference Output

DESCRIPTION

The UC1635 family of integrated circuits was designed for use in precision speed control of DC motors. An extension to the UC1633 line of phase locked controllers, these devices provide access to both of the digital phase detector's inputs, and include a reference frequency divider output pin. With this added flexibility, this family of controllers can be used to obtain phase synchronization of multiple motors.

A reference frequency can be generated using the device's crystal oscillator and programmable dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

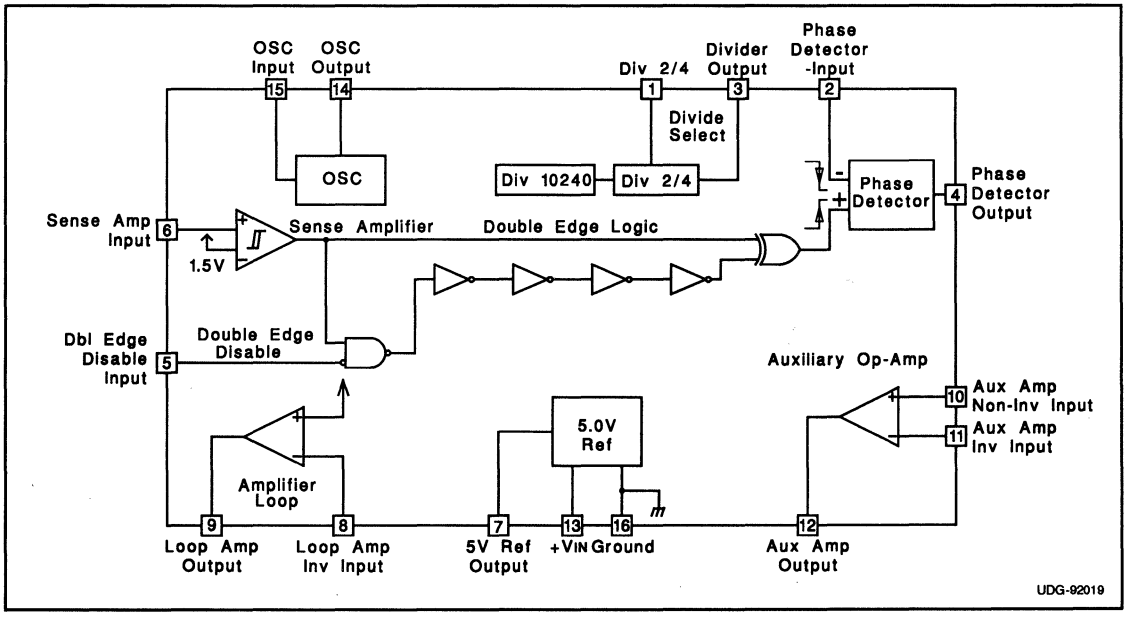
The phase detector responds proportionally to the phase error between the detector's minus input pin and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A 5V reference output can be used to accurately set DC operating levels.

6

BLOCK DIAGRAM



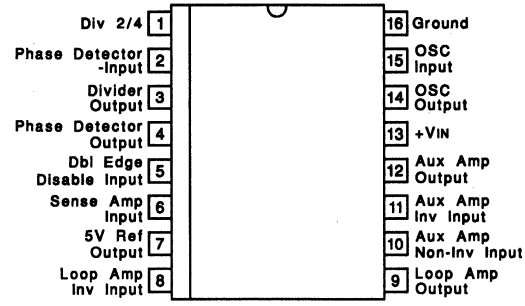
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -0.3 to +20V
Phase Detector Input Voltage ..... -0.3V to +5V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltages ..... -0.3V to +10V
Double Edge Disable Input Voltage ..... -0.3V to +10V
Oscillator Input Voltage ..... -0.3V to +5V
Sense Amplifier Input Voltage ..... -0.3V to +20V
Power Dissipation at TA = 25°C, (Note 2) 1000mW
Power Dissipation at Tc = 25°C, (Note 2) 2000mW
Operating Junction Temperature ..... -55° to 150°C
Storage Temperature ..... -65° to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

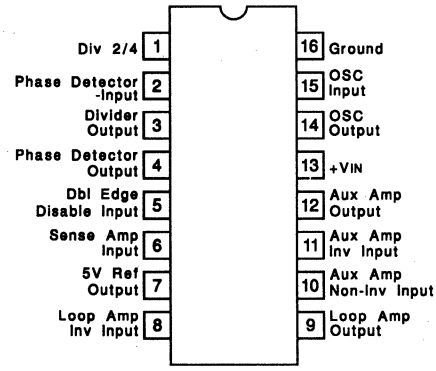
Note 1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

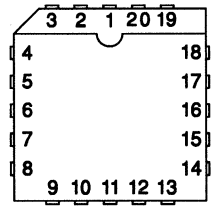
SOIC–16 (Top View)
DW Package



DIL–16 (Top View)
J & N Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 2/4	2
Phase Detector Input	3
Divider Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +VIN = 12V. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0 to 7mA		5.0	20	mV
Line Regulation	+VIN = 8 to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	15	35		mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (V_{IB})	Oscillator Input Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	V_{IN} = V_{IB} ±0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1Vpp at Oscillator Input	10			MHz
Div 2/4 Input Current	Input = 5V (Div. by 2)		150	500	µA
	Input = 0V (Div. by 4)	-5.0	0.0	5.0	µA
Div 2/4 Threshold		0.5	1.6	2.2	V
Divider Output	High Level (w/6.8k Load to GND)	4.0	4.5		V
	Low Level (Open Collector Leakage)			10	µA
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Sense Amplifier (cont.)					
Threshold Hysteresis			10		µV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
-Input Threshold	Detector Responds to Falling Edge	0.5	1.6	2.2	V
-Input Current	Input = 2.2V		100	250	µA
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Loop Amplifier					
Non-Inv Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	+V_{IN} = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

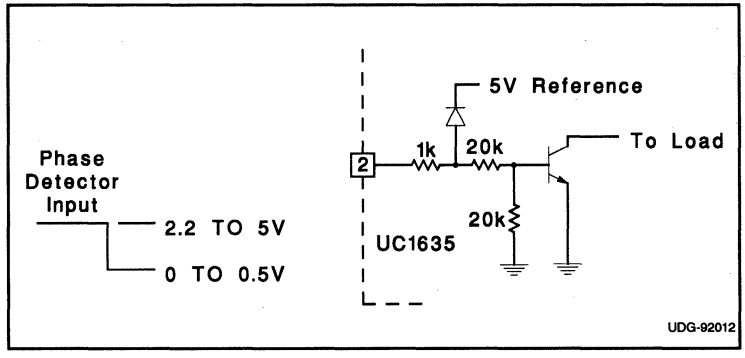
Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. $T_A = T_J$.

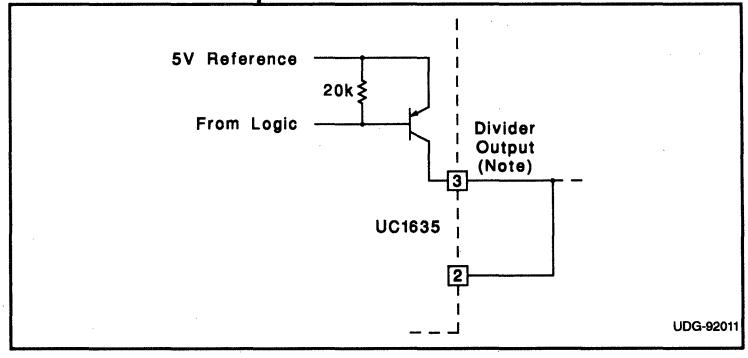
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	+V_{IN} = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Application and Operation Information
(For Additional Application Information see the UC1633 Data Sheet)
(Pin numbers refer to DIL and SOIC packages)

Phase Detector Input



Reference Divider Output Detail



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INTEGRATED CIRCUITS
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UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- ± 2.5V to ± 20V Input Supply Range
- ± 5% Initial Oscillator Accuracy; ± 10% Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

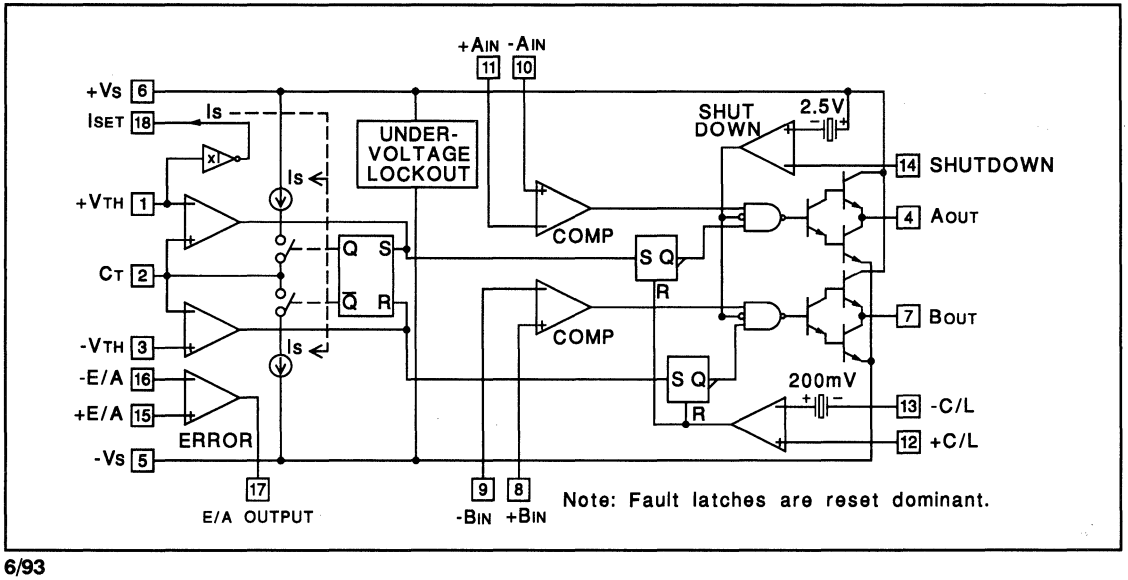
The UC1637 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC2637 and UC3637 are characterized for -25°C to +85°C and 0°C to +70°C, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (±Vs) ..... ±20V
Output Current, Source/Sink (Pins 4, 7) 500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11 12, 13, 14, 15, 16) ..... ±Vs
Error Amplifier Output Current (Pin 17) ..... ±20mA
Oscillator Charging Current (Pin 18) ..... -2mA
Power Dissipation at T_A = 25°C (Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

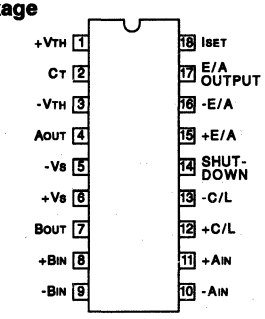
BLOCK DIAGRAM



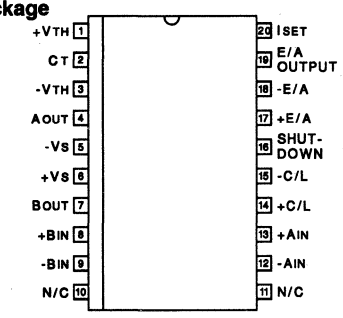
6/93

CONNECTION DIAGRAM

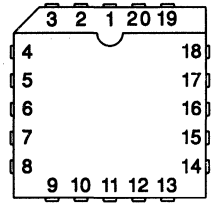
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
+VTH	1
CT	2
-VTH	3
AOUT	4
-VS	5
N/C	6
+VS	7
BOUT	8
+BIN	9
-BIN	10
-AIN	11
+AIN	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
ISET	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; +Vs = +15V, -Vs = - 15V, +VTH = 5V, -VTH = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C	9.4	10	10.6	9	10	11	kHz
Voltage Stability	Vs = ±5V to ±20V, $V_{PIN\,1}$ = 3V, $V_{PIN\,3}$ = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
+VTH Input Bias Current	$V_{PIN\,2}$ = 6V	-10	0.1	10	-10	0.1	10	µA
-VTH Input Bias Current	$V_{PIN\,2}$ = 0V	-10	-0.5		-10	-0.5		µA
+VTH, -VTH Input Range		+Vs-2		-Vs+2	+Vs-2		-Vs+2	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 0V		1.5	5		1.5	10	mV
Input Bias Current	V_{CM} = 0V		0.5	5		0.5	5	µA
Input Offset Current	V_{CM} = 0V		0.1	1		0.1	1	µA
Common Mode Range	Vs = ±2.5 to 20V	-Vs+2		+Vs	-Vs+2		+Vs	V
Open Loop Voltage Gain	R_L = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	Vs = ±2.5 to ±20V	75	110		75	110		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637: Vs = +15V, -Vs = - 15V, +VTH = 5V, -VTH = -5V, RT = 16.7kΩ, CT = 1500pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	VPIN 17 = 0V		-50	-20		-50	-20	mA
Output Source Current	VPIN 17 = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	VCM = 0V		20			20		mA
Input Bias Current	VCM = 0V		2	10		2	10	µA
Input Hysteresis	VCM = 0V		10			10		mV
Common Mode range	Vs = ±5V to ±40V	-Vs+1		+Vs-2	-Vs+1		+Vs-2	V
Current Limit								
Input Offset Voltage	VCM = 0V, T_J = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	Vs = ±2.5V to ±20V	-Vs		+Vs-3	-Vs		+Vs-3	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	VPIN 14 = +Vs to -Vs	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	ISINK = 20mA		-14.9	-13		-14.9	-13	V
	ISINK = 100mA		-14.5	-13		-14.5	-13	
Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
	ISOURCE = 100mA	12	13.5		12	13.5		
Rise Time	(Note 3) CL = Inf, T_J = 25°C		100	600		100	600	ns
Fall Time	(Note 3) CL = Inf, T_J = 25°C		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4: Parameter measured with respect to +Vs (Pin 6).
Note 5: Parameter measured at +Vs (Pin 6) with respect to -Vs (Pin 5).

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, ISET and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins +VTH and -VTH respectively. The +VTH terminal voltage is buffered internally and also applied to the ISET terminal to develop the capacitor charging current through RT. If RT is referenced to -Vs as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

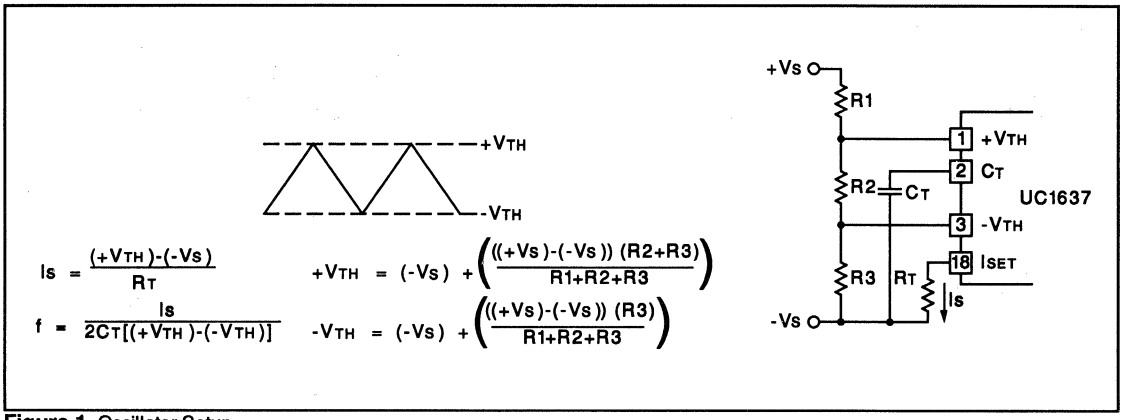


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)
In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)
A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)
With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

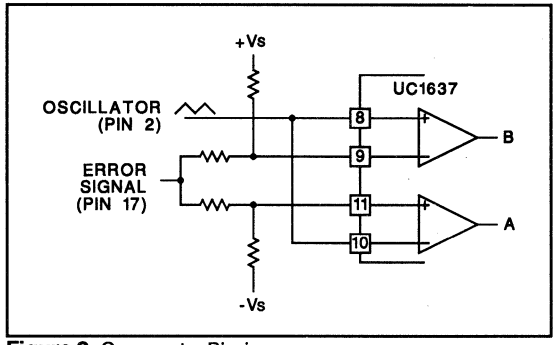


Figure 2. Comparator Biasing

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically -Vs + 0.2V @50mA low level and +Vs - 2.0V @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/μs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the ±Vs supply voltage, the common mode input range and the voltage output swing is within 2V of the Vs supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

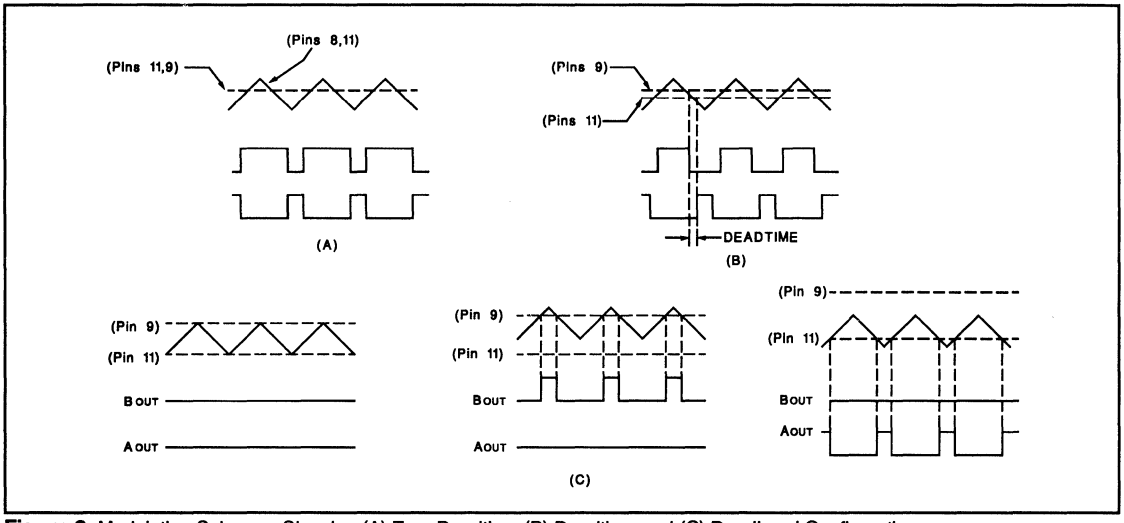


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below VIN, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

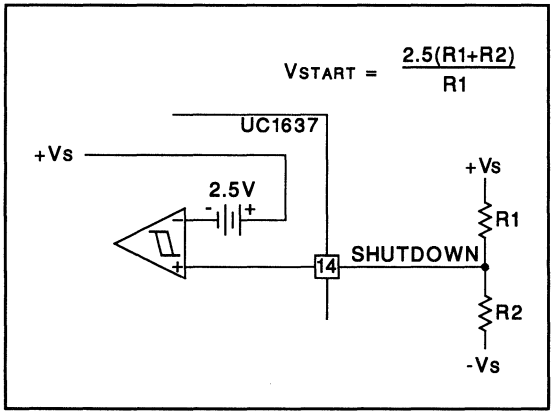


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from -Vs to within 3V of the +Vs supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

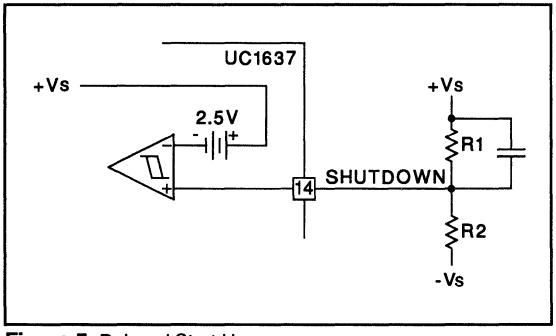


Figure 5. Delayed Start-Up

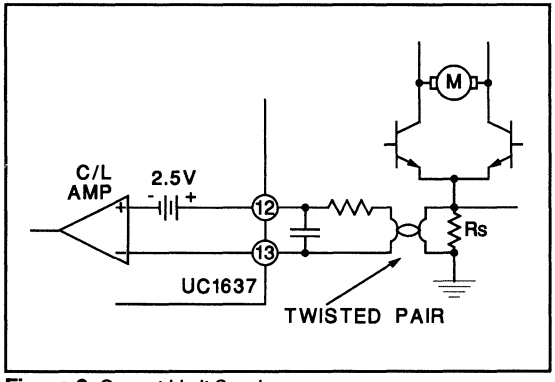


Figure 6. Current Limit Sensing

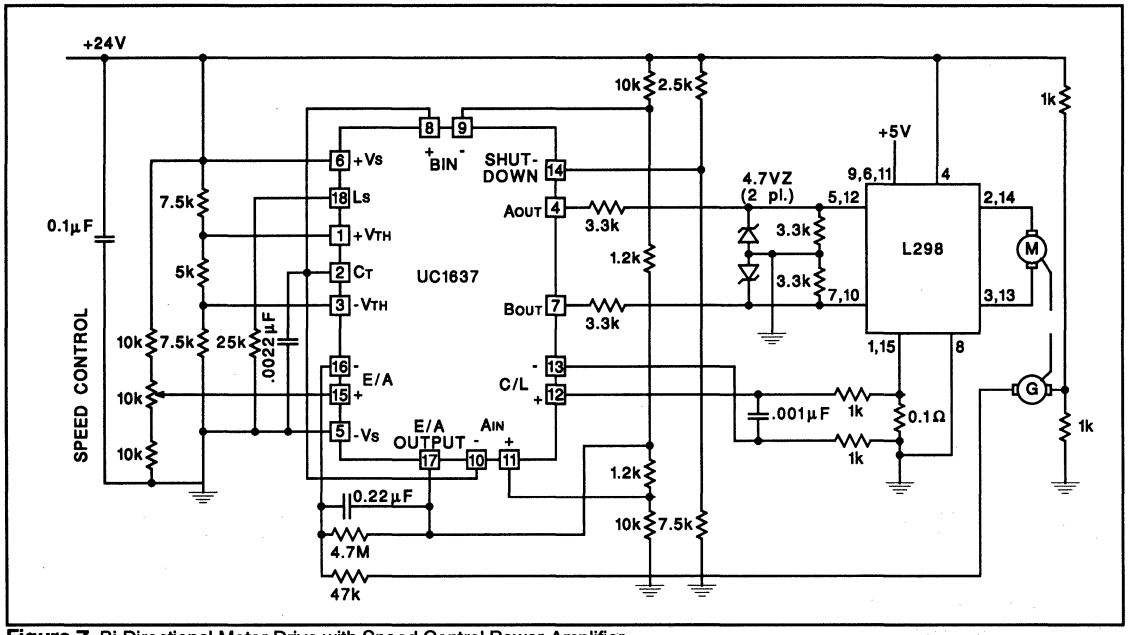


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

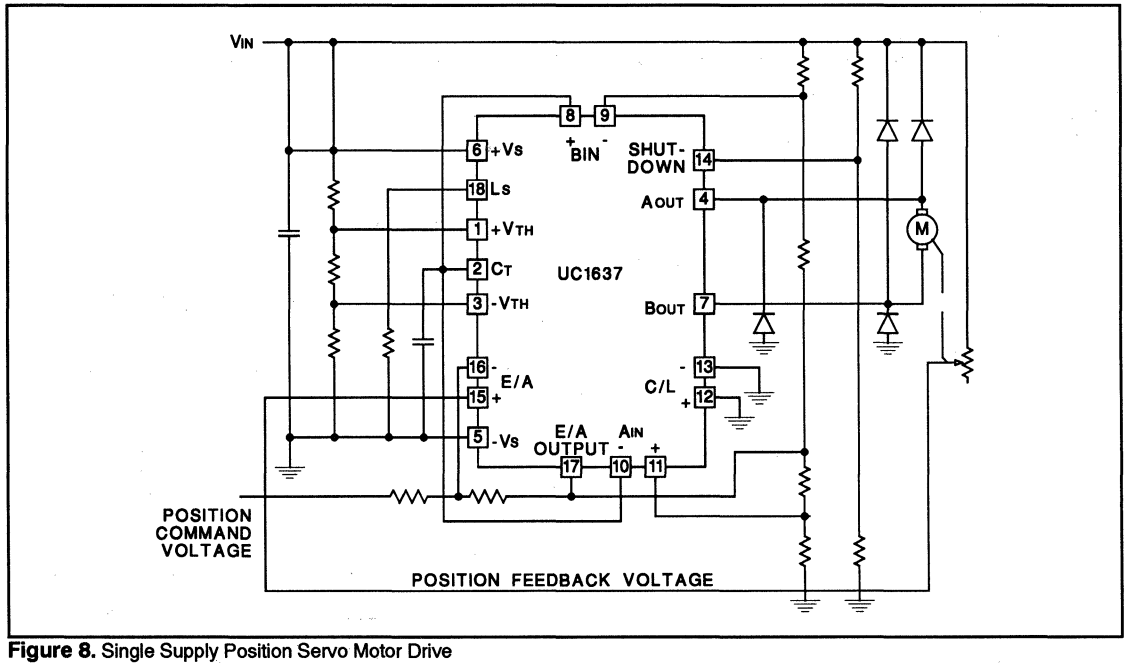


Figure 8. Single Supply Position Servo Motor Drive

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Stepper Motor Drive Circuit

UC1717
UC3717

FEATURES

- Half-step and Full-step Capability
- Bipolar Constant Current Motor Drive
- Built-in Fast Recovery Schottky Commutating Diodes
- Wide Range of Current Control 5-1000mA
- Wide Voltage Range 10-45V
- Designed for Unregulated Motor Supply Voltage
- Current Levels can be Selected in Steps or Varied Continuously
- Thermal Overload Protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717SP is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC3717 is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, Vcc 7V
- Output Supply, VM 45V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) Vcc
- Reference Input (Pin 11) 15V

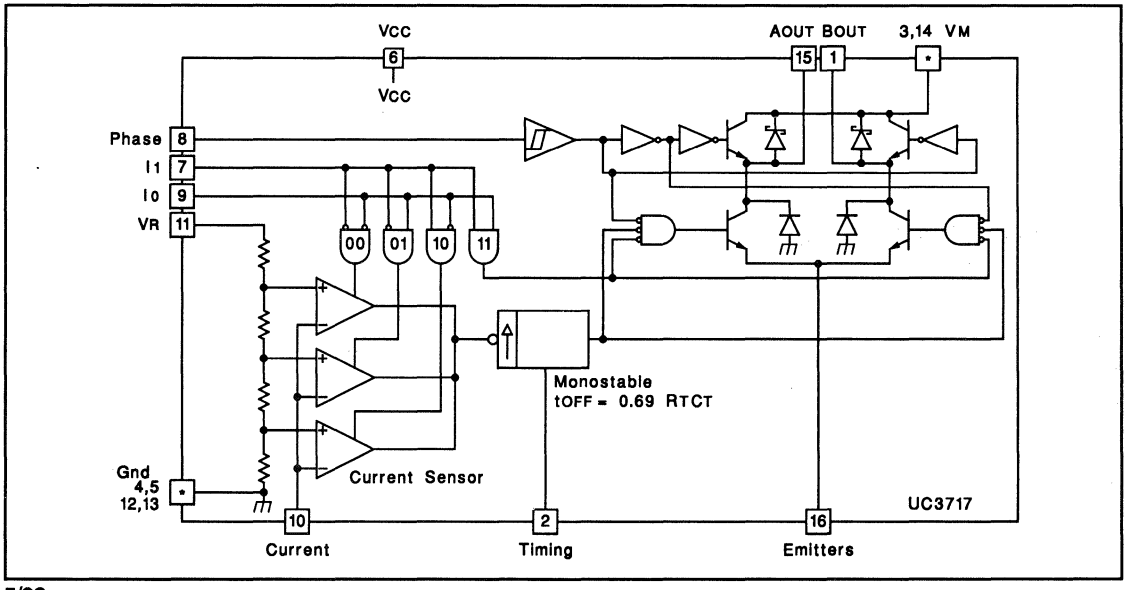
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1A
Junction Temperature, TJ ..... +150°C
Storage Temperature Range, Ts ..... -55°C to +150°C

Note 1: All voltages are with respect to ground, Pins 4,5, 12, 13. Pin numbers refer to DIL-16 package. Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for information on thermal limitations and considerations of package.

6

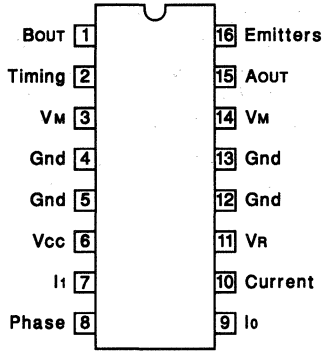
BLOCK DIAGRAM



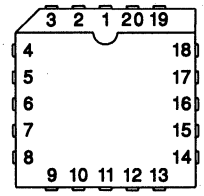
5/93

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
JP or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
VM	4
Gnd	5
N/C	6
Gnd	7
VCC	8
I1	9
Phase	10
N/C	11
Io	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage, Vcc	4.75	5	5.25	V
Supply Voltage, VM	10		40	V
Output Current. IM	20		800	mA
Rise Time Logic Inputs, tR			2	µs
Fall Time Logic Inputs, tF			2	µs
Ambient Temperature, TA				
UC1717	-55		125	°C
UC3717	0		70	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise specified, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Icc				25	mA
High-Level Input Voltage, Pins 7, 8, 9		2.0			V
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V
High-Level Input Current, Pins 7, 8, 9	VI = 2.4V			20	µA
Low Level Input Current, Pins 7, 8, 9	VI = 0.4V	-0.4			mA
Comparator Threshold Voltage	Io = 0, I1 = 0, VR = 5.0V	390	420	440	mV
	Io = 1, I1 = 0, VR = 5.0V	230	250	270	mV
	Io = 0, I1 = 1, VR = 5.0V	65	80	90	mV
Comparator Input Current		-20		20	µA
Output Leakage Current	Io = 1, I1 = 1, TA = +25°C			100	µA
Total Saturation Voltage Drop	IM = 500mA			4.0	V
Total Power Dissipation	IM = 500mA, fs = 30kHz		1.4	2.1	W
	IM = 800mA, fs = 30kHz		2.9	3.1	W
Cut Off Time, tOFF	VM = 10V, tON≥ 5µs (See Figure 5 and 6)	25	30	35	µs
Turn Off Delay, tD	TA = +25°C; dVc/dt ≥ 50mV/µs (See Figure 5 and 6)		1.6	2.0	µs
Thermal Shutdown Junction Temperature		+160		+180	°C

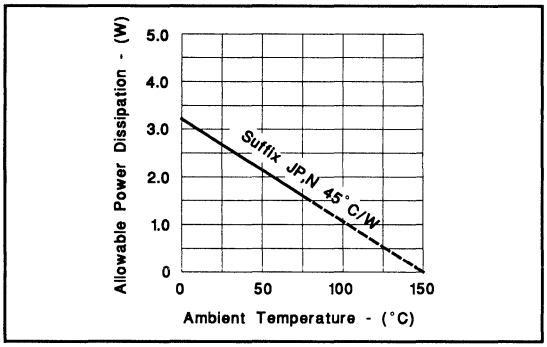


Figure 1

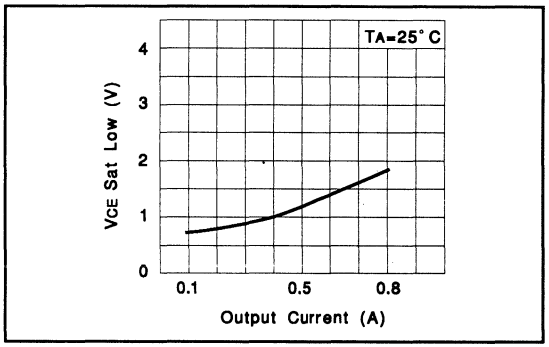


Figure 3: Typical Sink Saturation Voltage vs Output Current

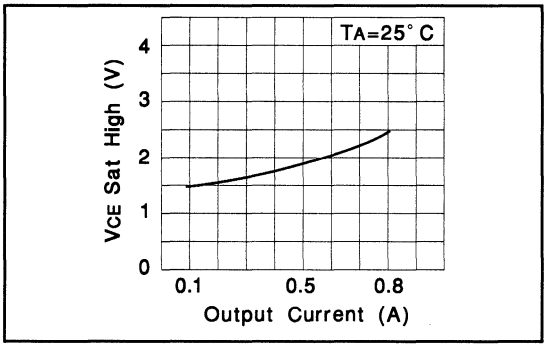


Figure 2: Typical Source Saturation Voltage vs Output Current

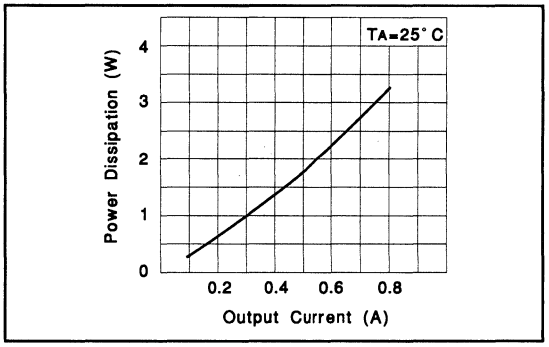


Figure 4: Typical Power Losses vs Output Current

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions:

(1) Phase Logic and H-Bridge Output Stage
(2) Voltage Divider with three Comparators for current control
(3) Two Logic inputs for Digital current level select
(4) Monostable for off time generation

Input Logic: If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input: The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage: The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used

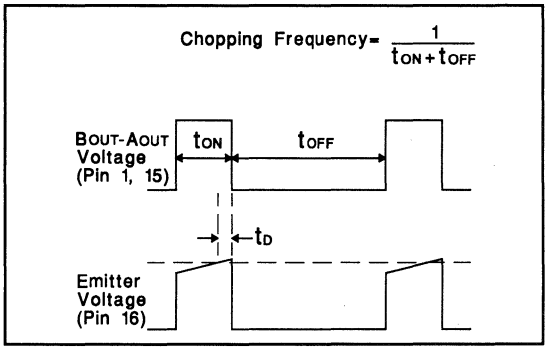


Figure 5: Connections and Component Values as in Figure 6.

across the source transistors. The Schottky diodes allow the current to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

PHASE INPUT	Q1, Q4	Q2, Q3
Low	Off	On
High	On	Off

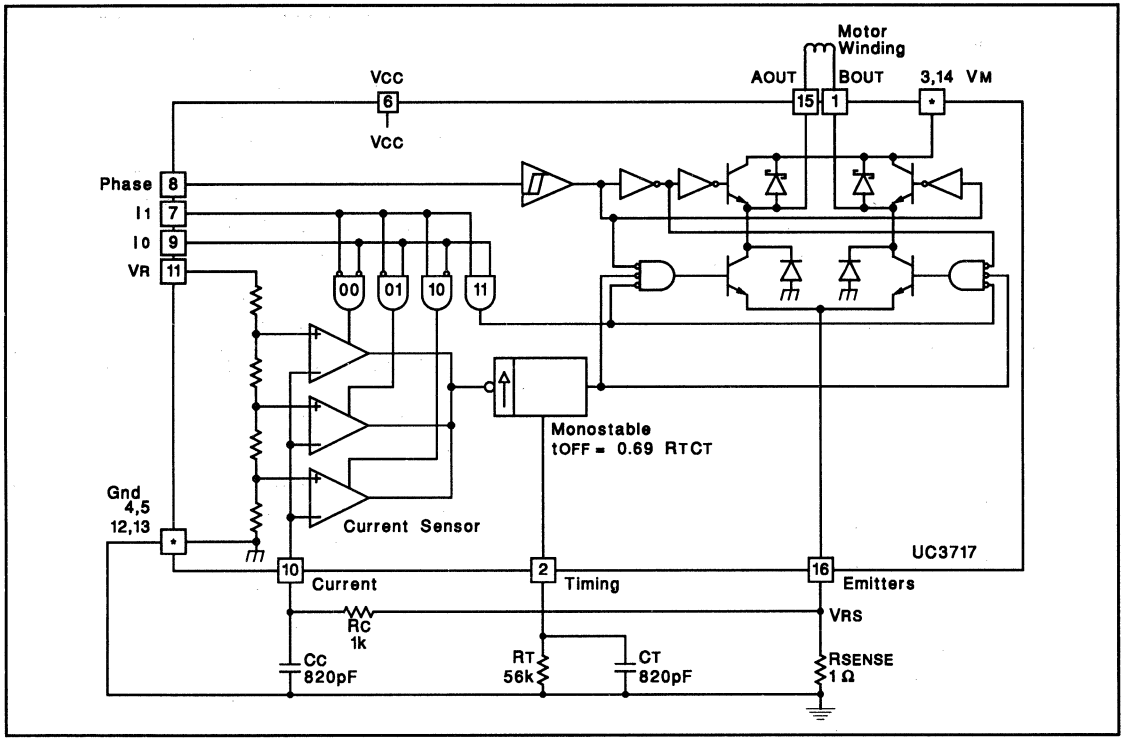


Figure 6

I0	I1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

Current Control: The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I0, I1) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by RT and CT connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and microstepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor Rs (pin 16).

Single-Pulse Generator: The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components RT and CT as:

$$T_{OFF} = 0.69\ R_T C_T$$

If a new trigger signal should occur during TOFF, it is ignored.

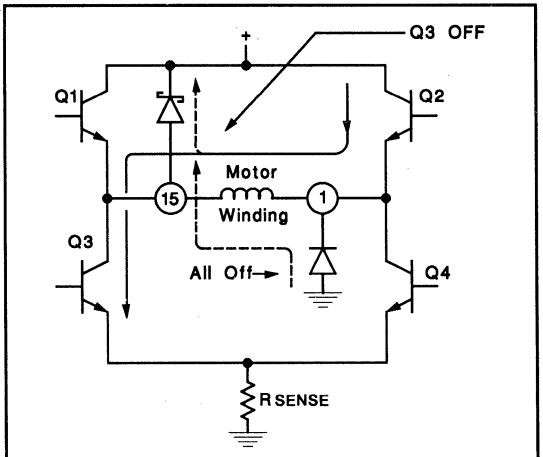


Figure 7: Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

Overload Protection: The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation: When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low pass filter Rc, Cc to the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistsor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noted at this time that the slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed at the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

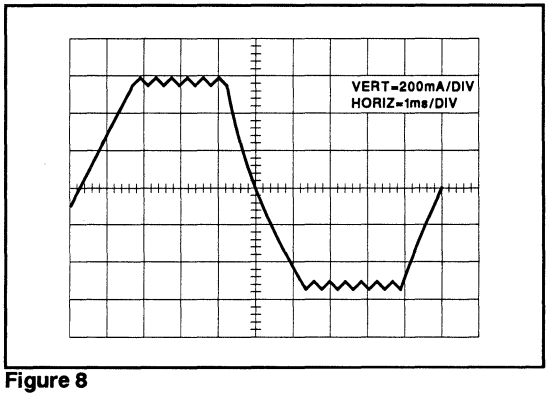


Figure 8

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

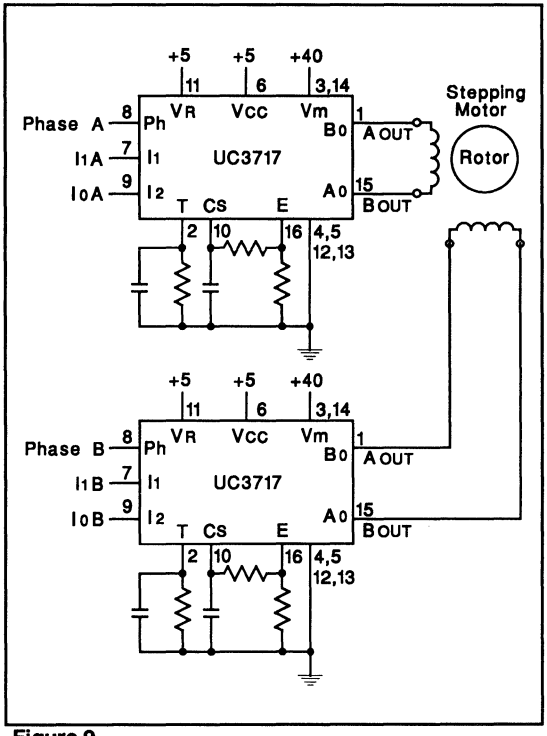


Figure 9

The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

Using the UC3717 to drive the L298 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

FUNCTIONAL DESCRIPTION (cont.)

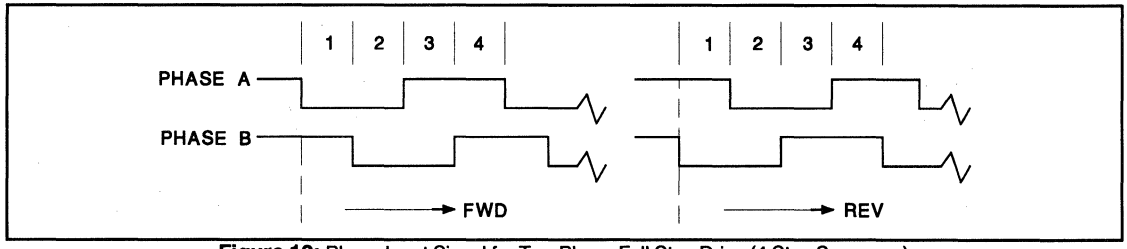


Figure 10: Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

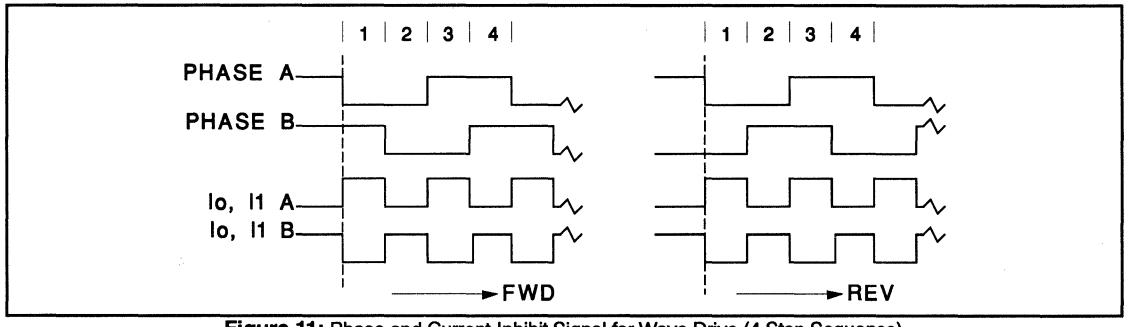


Figure 11: Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

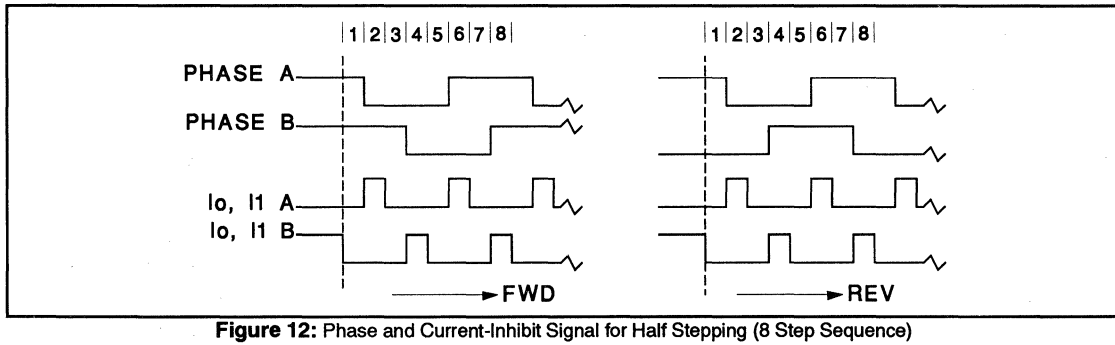


Figure 12: Phase and Current-Inhibit Signal for Half Stepping (8 Step Sequence)

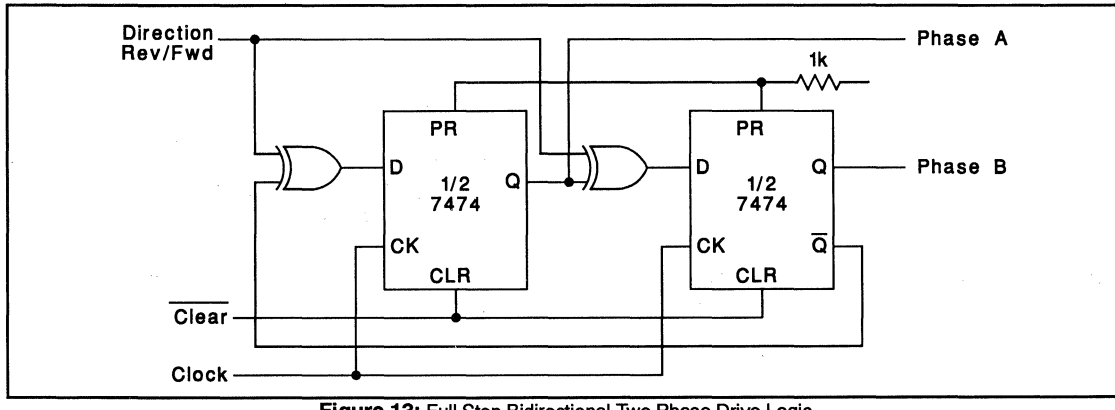


Figure 13: Full Step Bidirectional Two Phase Drive Logic

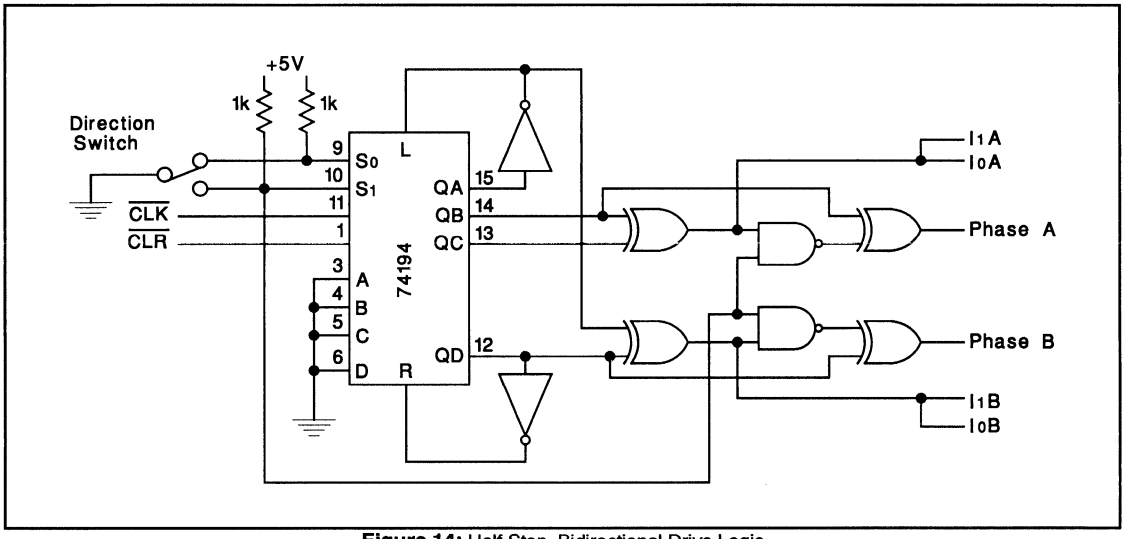


Figure 14: Half-Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping: In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

Ramping: Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors, torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses: Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponential manner as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

UNITRODE TYPE NUMBER
UC3717N - 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC1717JP - 16 Pin Dual-in-line Power Ceramic Package

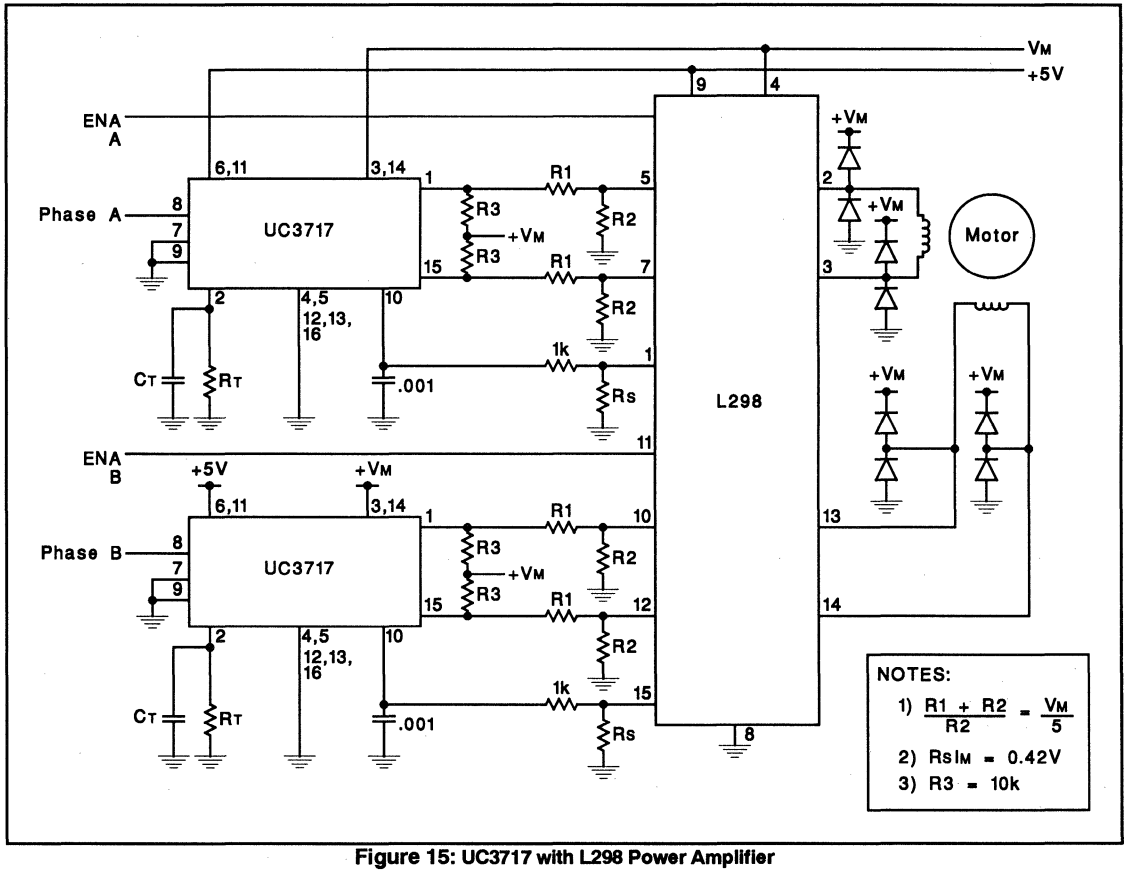


Figure 15: UC3717 with L298 Power Amplifier

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603)424-3460

Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- +/- 550mA Load Current
- 1.2V Typical Total Vsat at 450mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- 5V or 12V Operation
- 12mA Quiescent Supply Current
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

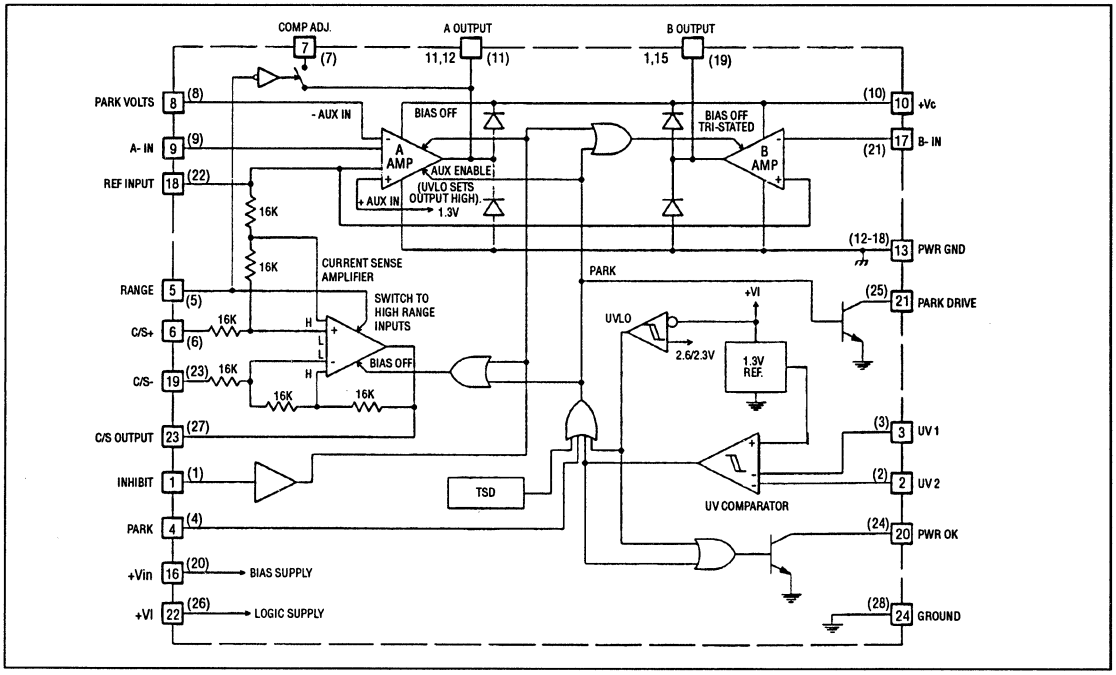
DESCRIPTION

This full-bridge power amplifier, rated for continuous output current of 0.55 Amperes, is intended for use in demanding servo applications such as head positioning for high-density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3173A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and activate the built-in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low-side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

6



Pin numbers shown are for "DW" PKG., ( ) numbers are for "QP" PKG.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+Vin, +Vc, +VI).....20V
UV Comparator, Logic Inputs, and Ref Input
maximum forced voltage.....-0.3V to 10V
maximum forced current.....+/- 10mA
B Amplifier Inverting Input.....-0.3V to +Vin + 1.0V
A Amplifier Inverting Inputs,(Aux. and normal).-0.3Vto +Vc + 1.0V
Open Collector Output Voltages.....20V
A and B Output Currents (continuous)
source.....Internally Limited
sink.....0.6A
Parking Drive Output Current
continuous.....150mA
pulsed.....1A
Output Diode Current (pulsed).....0.5A
Power OK Output Current(continuous).....30mA
Operating Junction Temperature.....- 55°C to +150°C
Storage Temperature.....- 65°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500uS.

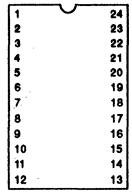
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
Thermal Resistance Junction to Leads, θjl .....15°C/W
Thermal Resistance Junction to Ambient, θja....30°-40°C/W
DW package:
Thermal Resistance Junction to Leads, θjl ..... 35°C/W
Thermal Resistance Junction to Ambient, θja....60°-70°C/W
FQ package:
Thermal Resistance Junction to Leads, θjl .....60°C/W
Thermal Resistance Junction to Ambient, θja .110-120°C/W

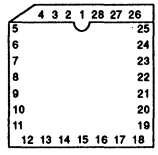
Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guide lines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAMS

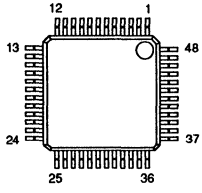
SOIC - 24 (TOP VIEW)
DW PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



TQFP-48 (TOP VIEW)
FQ PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DW	QP	FQ
INHIBIT	1	1	9
UV 2	2	2	10
UV 1	3	3	11
PARK	4	4	12
RANGE	5	5	13
C/S+	6	6	14
COMP ADJ	7	7	15
PARK VOLTS	8	8	16
A- IN	9	9	21
+Vc	10	10	22
A OUTPUT	11,12	11	26, 27
POWER GND	13	12-18	30, 31
B OUTPUT	14,15	19	34, 35
+Vin	16	20	39
B- IN	17	21	40
REF INPUT	18	22	45
C/S-	19	23	46
PWR OK	20	24	47
PARK DRIVE	21	25	48
+VI	22	26	2
C/S OUTPUT	23	27	3
GROUND	24	28	4

Electrical Characteristics:
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +VI, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+Vin Supply Current			10	13	mA
+Vc Supply Current	Iout = 0A		1.2	2.0	mA
+VI Supply Current			0.65	1.0	mA
Total Supply Current	Supplies = 5V, Iout = 0A		12	16	mA
	Supplies = 12V, Iout = 0A		13	18	mA
+VI UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysteresis			300		mV
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current	Max at either UV input	-1.0	-0.25		uA
UV Thresholds	low to high, other input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWR OK Vsat	Iout = 5mA, UV input low		0.15	0.45	V
PWR OK Leakage	Vout = 20V			5	uA

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER AMPLIFIERS A AND B					
Input Offset Voltage	A Amplifier, Vcm = 2.5V			4	mV
	B Amplifier, Vcm = 2.5V			12	mV
Input Bias Current	Vcm = 2.5V, Inverting inputs only	-500	-150		nA
Input Bias Current at Ref. Input	(Ref. Input - C/S+)/48Kohms, Tj = 25°C	15	21	27	uA/V
CMRR	Vcm = 1 to 10V, Supplies = 12V	70	90		dB
PSRR	+Vin = 4 to 15V, Vcm = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, Vout = 1V, Iout = 300mA to Vout = 11V, Iout = -300mA	3.0	15.0		V/mV
Gain Bandwidth Product	Note 1, A Amplifier		2.0		MHz
	Note 1, B Amplifier		1.0		MHz
Slew Rate	Note 1		1.0		V/uS
High-Side Current Limit		0.45	0.6		A
Output Saturation Voltage	High-Side, Iout = -100mA, Note 2		0.7		V
	High-Side, Iout = -300mA, Note 2		0.8		V
	High-Side, Iout = -550mA, Note 2		0.95		V
	Low-Side, Iout = 100mA		0.2		V
	Low-Side, Iout = 300mA		0.25		V
	Low-Side, Iout = 550mA		0.35		V
	Total Vsat, Iout = 100mA		0.9	1.2	V
	Total Vsat, Iout = 300mA		1.05	1.4	V
	Total Vsat, Iout = 550mA		1.3	1.7	V
+Vc to +Vin Headroom	Volts below +Vin, delta High-Side Vsat = 100mV, Iout = -450mA, Note 2	0.33	0.5		V
High-Side Diode, Vf	Id = 550mA		1.0		V
Low-Side Diode, Vf	Id = 550mA, Inhibit activated, B amplifer only		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	Vcm = 2.5V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change with Common Mode Input	Vcm = -1V to 13V, Supplies = 12V Low Range Mode			2000	uV/V
	High Range Mode			4000	uV/V
Voltage Gain	Vdiff = +1.0 to -1.0V, Vcm = 2.5V High range mode	0.485	0.50	0.515	V/V
	Low range mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, Iout = 1mA,		0.1	0.3	V
	High-Side, Iout = -1mA, Referenced to +Vin		0.1	0.3	V
PARKING FUNCTION					
Park Input Threshold Voltage		0.6	1.1	1.7	V
Park Input Threshold Current	Internal pull-up, Vin = 0.6V		50	75	uA
Park Drive Saturation Voltage	Iout = 50mA		0.15	0.35	V
Park Drive Leakage	Vout = 20V			50	uA
Regulating Voltage at Park Volts Input		1.275	1.30	1.325	V

Note 1: This specification not tested in production

Note 2: The high-side saturation performance of the UC3173A is referenced to the +Vin supply pin. The +Vc suppy pin can operate slightly below the +Vin supply input, about 400 mV, without affecting this performance.

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTION (CONTINUED)					
Amplifier A Auxiliary Input Bias Current		-750	-300		nA
Amplifier A Parking High-Side Saturation Voltage	Iout = -50mA, +Vin = 0V, +Vc = +Vl = 5V, Park Input Open, +Vc to Vout		0.8	0.95	V
Minimum Parking Supply	At +Vc and +Vl, +Vin = 0V, A Amplifier out - Vsat Parking Drive>0.5V Ipark = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At +Vl, +Vc = +Vin = 0V, Vsats < 0.5V, Iout Parking Drive = 50mA, Rl = 30ohms to 2V		1.1	1.4	V
	Iout Power OK = 5mA, Rl = 300ohms to 2V		1.2	1.6	V
+Vl Parking Supply Current	Park Input Open, +Vl = 5V, +Vc = 1.6V, +Vin = 0V Power OK Iout = 5mA, Parking Drive Iout = 50mA		1.6	3.0	mA
AUXILIARY FUNCTIONS					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		uA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	uA
Comp Adjust Pin Saturation Voltage	Range Input = 0V, Pin Current = +/-500uA Referenced to Aout		0.02	0.1	V
Comp Adjust Leakage Current	Range Input = 1.7V, Supplies = 12V Aout-V Comp Adj = +/-6V			5	uA
Total Supply Current when Inhibited	+Vin, +Vc, and +Vl currents		1.0	1.5	mA
Thermal Shutdown Temperature	Note 1		165		°C

Note 1: This specification not tested in production

PIN FUNCTIONAL DESCRIPTION

+Vin Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high-side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

+Vc +Vc supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A, or B amplifiers are to be activated. This pin can operate approximately 400mV below the +Vin supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

+Vl Logic portions of the UC3173A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PARKING DRIVE and POWER OK outputs. This pin is a low current supply that would normally be tied to the +Vc pin, or to a parking hold-up capacitor for extended parking operation with very low recovered back-emf.

GND Reference point for the internal reference, UV comparator, and other low-level circuitry.

PWR GND Current return for all high level circuitry, this pin should be connected to the same potential as **GND**.

A Out Output for the A power amplifier, providing one end of the differential drive to the load during normal operation, and during park. During a UVLO condition at the +Vin supply pin, this output is forced to a high, source only state.

B Out Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tri-stated.

A- In Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

B- In Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

Ref Input Reference for input control signals to the power amplifier, as well as, the non-inverting inputs to the A and B amplifiers, and the output level shift for the C/S amplifier.

C/S+ The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

Ref Input / 2 - 0.3V, in low range mode, and
2 • **Ref Input** - 0.9V, in high range mode.

C/S- The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

Range When this pin is open or at a logic **low** potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic **high**, the gain of the current sense amplifier will change into its **high** range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

Comp Adj The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

UV 1 & 2 Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the **Power OK** output to an active low state. If either of these inputs is not used it should be connected to a voltage greater than 1.3V.

Power OK Indicates with an active low condition that either of the **UV** inputs are low, or that the supply voltage at the **+VI** input to the UC3173A has dropped below the UVLO threshold. This output will remain active low until the **+VI** supply has dropped to below approximately 1.2V.

Park Volts The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3173A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-emf/velocity retract of the head. The park condition on the UC3173A is **always** activated by any one of the following four conditions, 1: a low condition on either of the **UV** inputs, 2: a high input level at the **Park** input, 3: a UVLO condition at the **+VI** supply pin, and 4: activation of the **TSD**, (thermal shutdown) protection circuit. During a UVLO condition at the **+VI** pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

Park Logic input that forces the park condition on the UC3173A. This input has an internal pull-up that will force the park condition if the pin is left open.

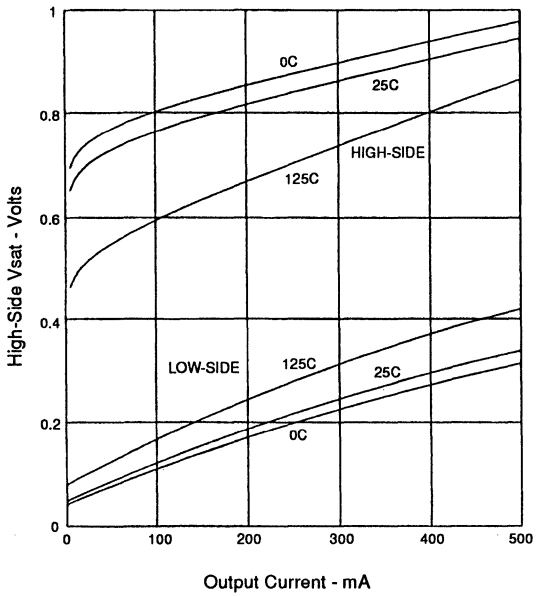
Park Drive A 100mA drive output that is active low during a park operation. This pin is normally used to supply the low-side drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

Inhibit A high impedence logic input that disables the A and B power amplifiers, as well as the Current Sense amplifier. The UV comparators and logic functions of the UC3173A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The **Inhibit** function is over-ridden by any condition that forces the park function to be activated.

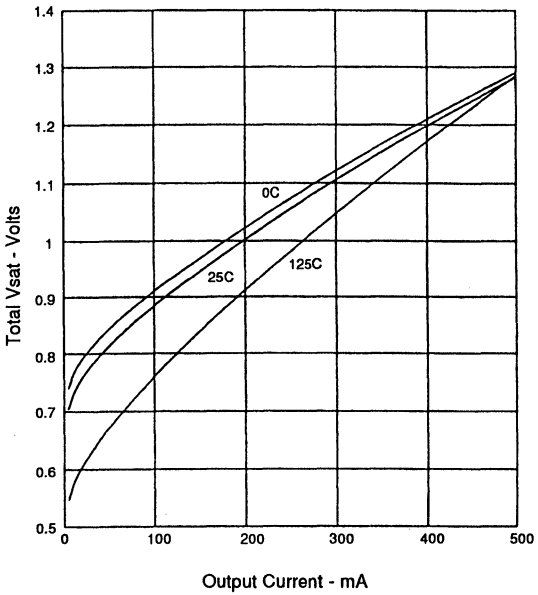
6

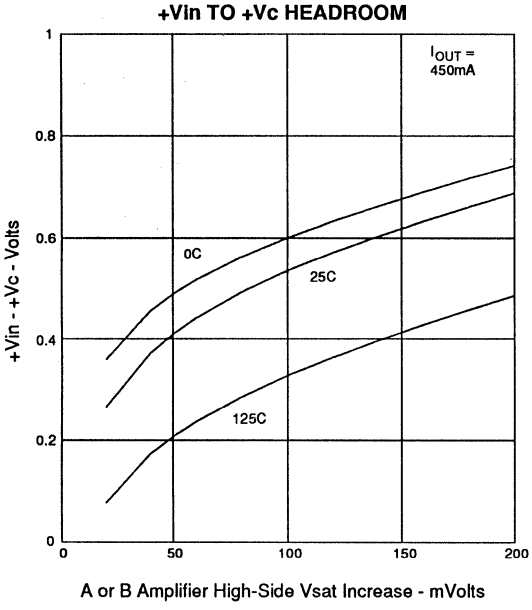
CHARACTERISTIC CURVES

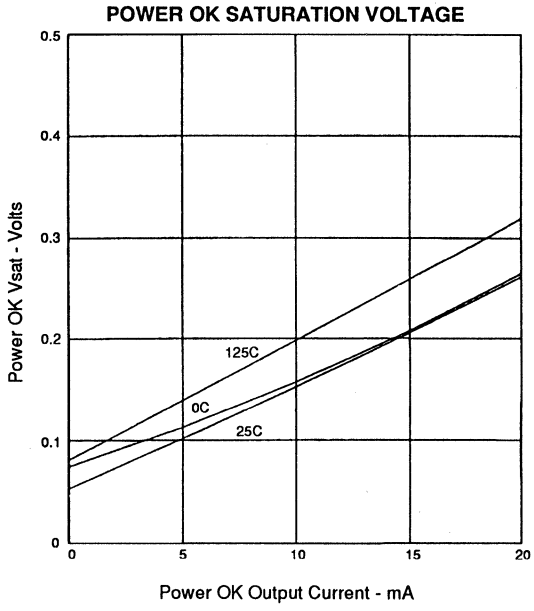
A AND B AMPLIFIER HIGH AND LOW VSATS

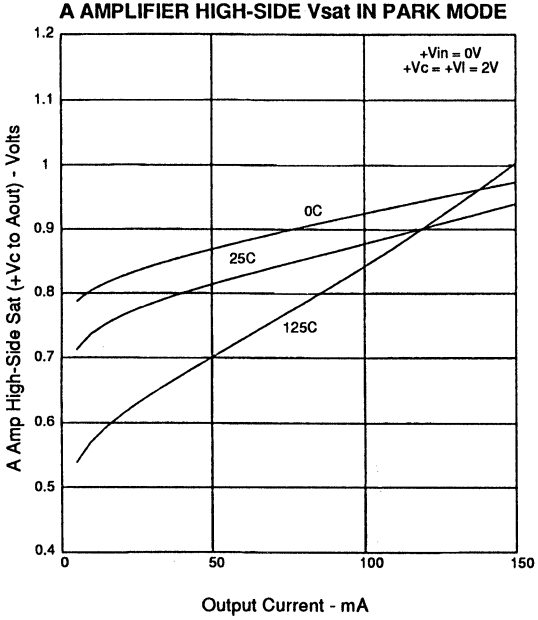


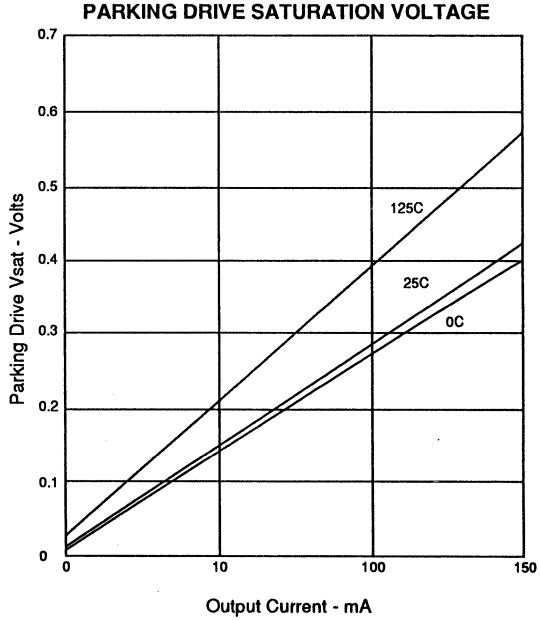
A AND B AMPLIFIER TOTAL VSAT



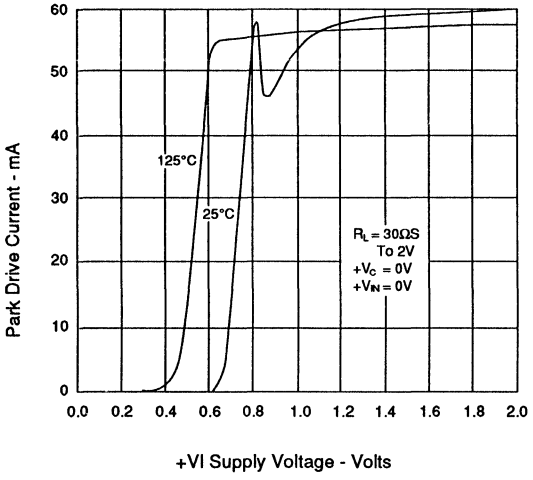

+Vin TO +Vc HEADROOM
I_{OUT} = 450mA
0C
25C
125C
+Vin - +Vc - Volts
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
A or B Amplifier High-Side Vsat Increase - mVolts


POWER OK SATURATION VOLTAGE
125C
0C
25C
Power OK Vsat - Volts
0.5
0.4
0.3
0.2
0.1
0
0
5
10
15
20
Power OK Output Current - mA

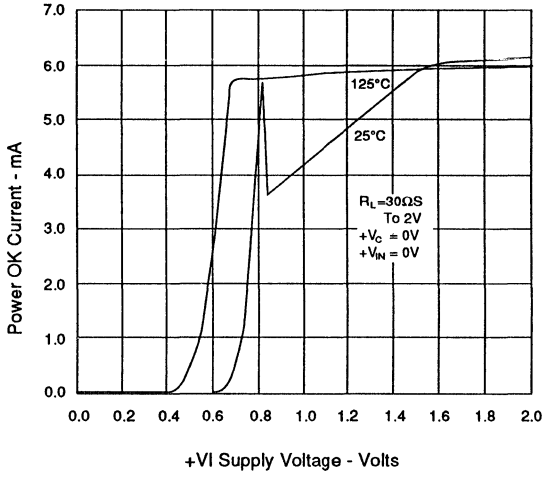

A AMPLIFIER HIGH-SIDE Vsat IN PARK MODE
+Vin = 0V
+Vc = +Vl = 2V
0C
25C
125C
A Amp High-Side Sat (+Vc to Aout) - Volts
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0
50
100
150
Output Current - mA


PARKING DRIVE SATURATION VOLTAGE
125C
25C
0C
Parking Drive Vsat - Volts
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
10
100
150
Output Current - mA

PARK DRIVE CURRENT vs. +V1 SUPPLY



POWER OK CURRENT vs. +VI SUPPLY



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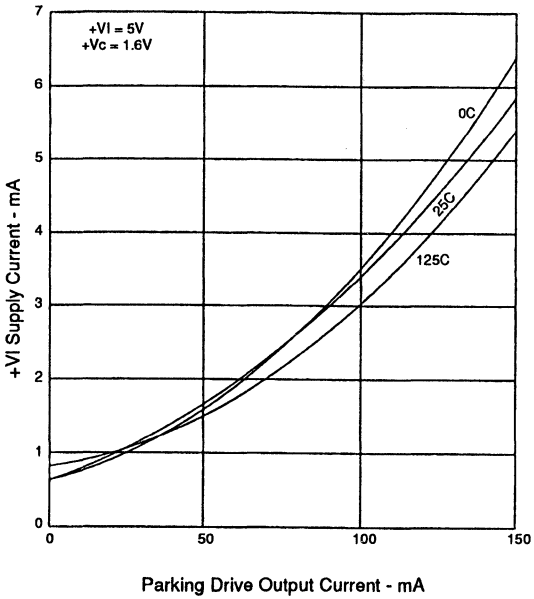
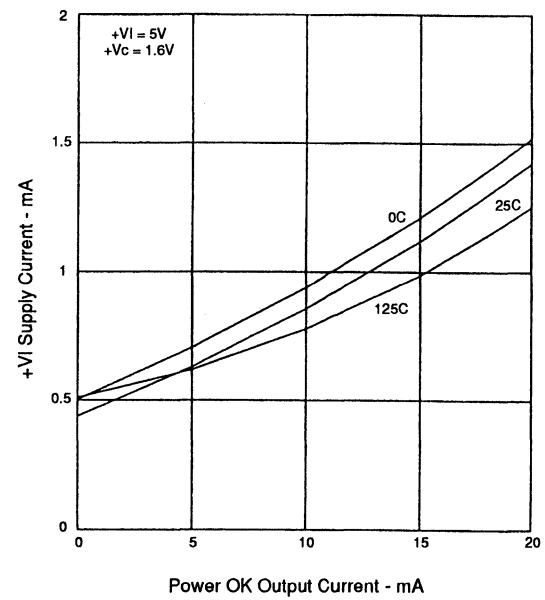
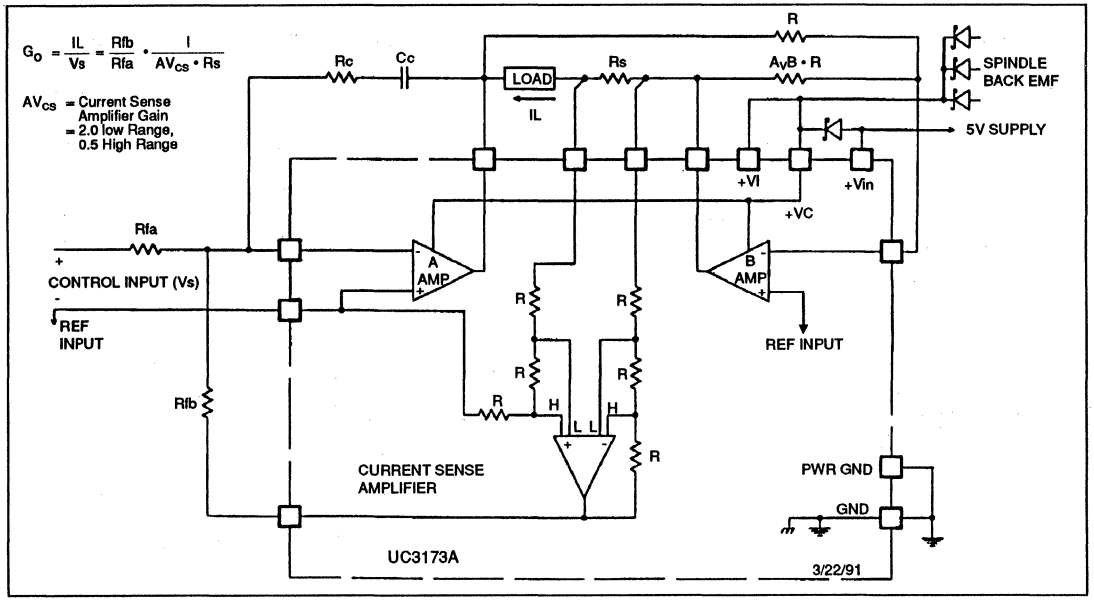
+VI CURRENT VERSUS PARK DR CURRENT



+VI CURRENT VERSUS PWR OK CURRENT



TYPICAL APPLICATION



Maximizing the Voltage to the Load

In order to assure that maximum voltage drive to the load is achievable there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the **Ref Input** and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the **Ref Input** voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (1).

$$(1)\, V_{ref(optimum)} = \frac{+Vin - Vhs_{sat} + Vls_{sat}}{2}$$

where: Vhs_{sat} = high-side V_{sat} at maximum load.
Vls_{sat} = low-side V_{sat} at maximum load.

Data for (1) can be taken off the characteristic curves showing Vsat performance versus output current. There will be a degree of temperature dependence to this solution since the low side Vsat of the power stages has a positive temperature dependence, and the high-side a negative. In some cases it might be worth interpolating between the 25°C and the 125°C curves to hit a typical junction temperature.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given **Ref Input** voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by,

$$(2)\, A_{VB} = \frac{+Vin - Vhs_{sat} + V_{ref}}{V_{ref} - Vls_{sat}}$$

or,

$$\frac{Vref - Vls_{sat}}{+Vin - Vhs_{sat} - V_{ref}}$$

whichever is greater than unity.

For a typical case, where Vref has been set at +Vin/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of $(A_{VB}+1)$.

Setting and Maximizing the Loop Bandwidth
The normal configuration for compensation of the power amplifier is shown in the ***Typical Application*** drawing. A simple RC network. RcCc time constant is typically chosen to correspond to the electrical time constant of the load, given by Rl/L. Where Rl is the total load and sense resistanace between the bridge outputs, and L is the load inductance.

The 3dB frequency(f_{3dB}) of the closed loop amplifier is given by the following expression:

$$(3)\ f_{3dB} = \frac{(1 + A_VB) \cdot A_VCS \cdot Rs \cdot Rc}{2\pi L \cdot Rfb}$$

assuming $f_{3dB} >> (2\pi Rc \cdot Cc)^{-1}$

where: A_VB is the voltage gain of the B amplifier.
A_VCS is the CS amplifier voltage gain.

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in the typical application drawing, the noise gain is given by the impedance ratio of the Rc-Cc series network, to the parallel combination of Rfa and Rfb. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product(GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

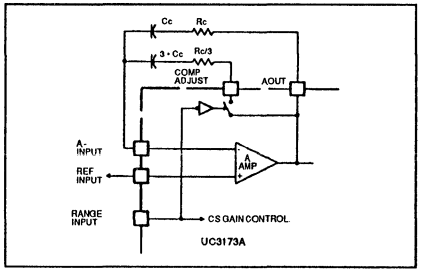
$$(4)\ f_{3dBmax} = \left(\frac{f_{gbw}A \cdot (1+A_VB) \cdot A_VCS \cdot Rs \cdot Rfa}{2\pi L \cdot (Rfa + Rfb)}\right)^{1/2}$$

where: $f_{gbw}A$ is the GBW of the A amplifier.

In the UC3173A, to accommodate wider power amplifier bandwidths, the GBW Product of the A amplifier has been extended to 2MHz. A loop compensated in this manner will have a second order closed response with the poles split around the 3dB frequency given in (3). The loop phase margin will be approximately 45°. The value of Rc required to set the above conditions is given by

$$(5)\ Rc_{max} = Rfb \cdot \left(\frac{f_{gbw}A \cdot 2\pi L \cdot Rfa}{(A_VB + 1) \cdot A_VCS \cdot Rs \cdot (Rfa + Rfb)}\right)^{1/2}$$

Range Change Bandwidth Control
When the range change feature of the UC3173A is used the closed loop bandwidth of the power amplifier will change according to (3). In other words, the bandwidth would be four times larger during the low range mode when AVCS is equal to 2, than during the high range mode when AVCS is equal to 0.5, unless the value of Rc is adjusted to compensate. The **Comp Adjust** pin on the UC3173A can be used to do this. The **Comp Adjust** pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.



The Comp Adjust pin switches in a parallel compensation network tostabilize the small signal bandwidth with range changes.

Head Parking
In the application figure, ***Controlled Velocity Head Parking,*** the UC3173A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by

$$(6)\ V_{park} = 1.3 \cdot \left(1 + \frac{R1}{R2}\right)$$

The B amplifier output is tri-stated during park, this side of the load is driven low by the **Park Drive** pin. A series resistor, Rp in the figure, can be inserted in series with the load to limit the peak current if required.

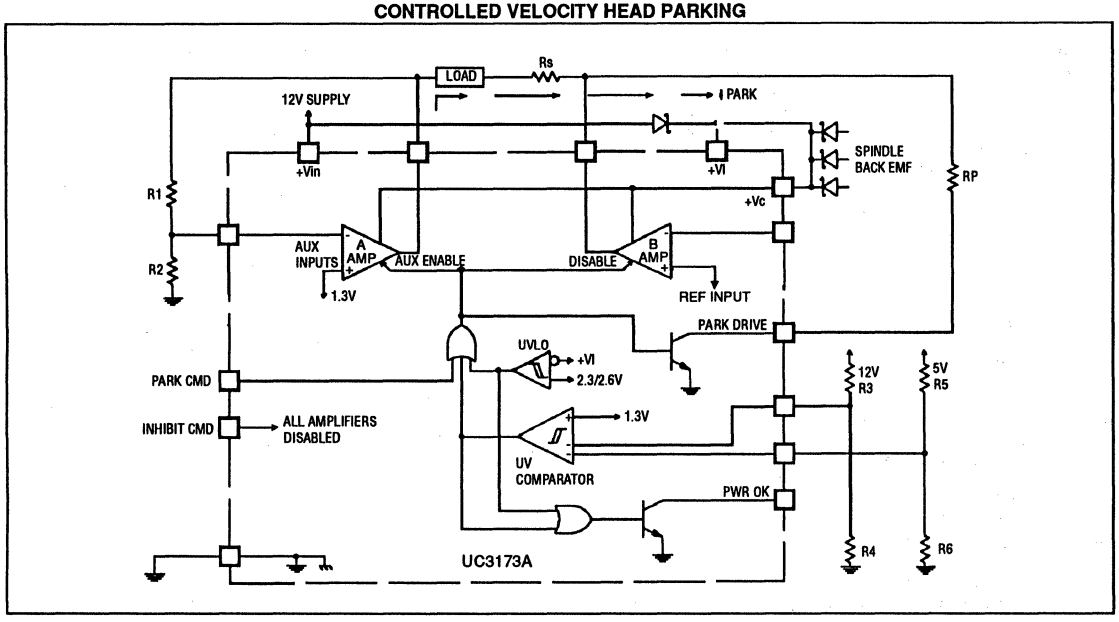
During park, supply to the load, and the UC3173A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the **+Vl** supply pin drops below the UVLO voltage,(2.3V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3173A will maintain drive to the load down to low supply levels. For example, with 1.5 Volts of recovered back EMF, the UC3173A can still deliver 50mA of drive to a 10 ohm load.

Parking With Very Low Back EMF
The UC3173 can also be configured to get parking drive to the load with very low recovered back EMF. The figure titled ***Head Parking with Low Back EMF*** illustrates how the **Power OK** pin can be used to drive an external PNP device to achieve very low parking drive Vsat losses. With this configuration, the UC3173A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

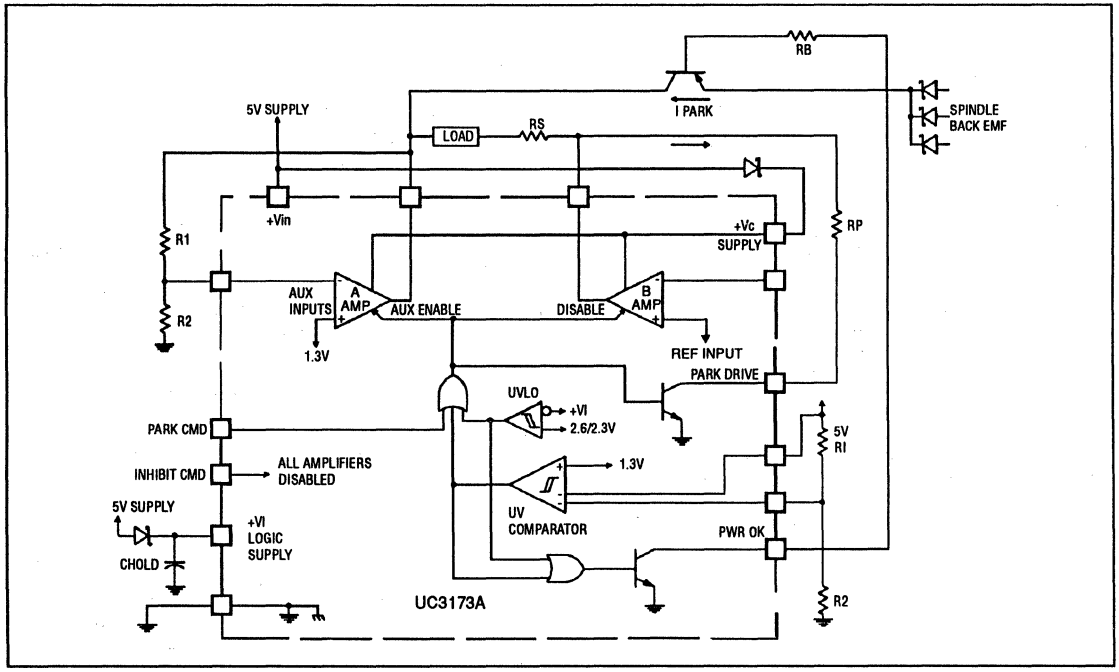
During system commanded parking with the supplies present, the **Park Volts** pin is still used to set the maximum voltage to the load. The logic function of the Power OK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the **Park Drive** and **Power OK** pins are provided by the **+Vl** supply pin. By using a hold up capacitor, CHOLD, the drive can be maintained to the load as the back EMF drops to below 1 volt. A variation on this approach is to add a connection between the +Vl pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V volt supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply drops below a certain level, is forcing a programmed voltage.

CONTROLLED VELOCITY HEAD PARKING



HEAD PARKING WITH LOW BACK EMF



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Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- ±800mA Load Current
- 1.25V Total V_{SAT} at 800mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Limit Input to Force Output Extremes
- Inhibit Input and UVLO
- 4V to 15V operation

DESCRIPTION

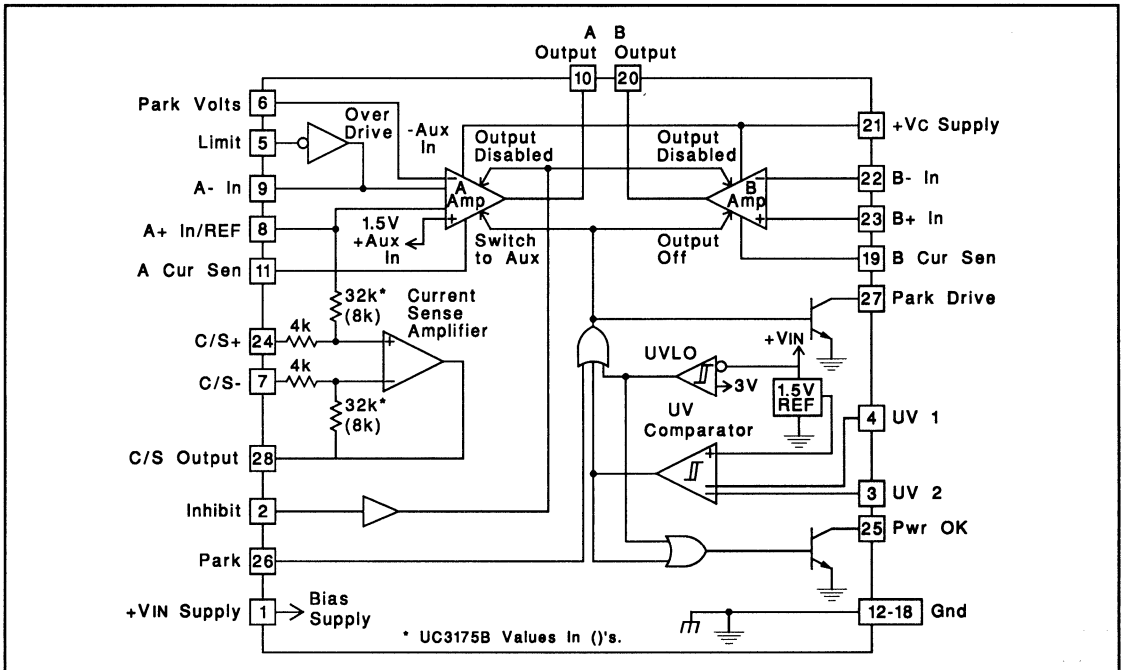
These full-bridge power amplifiers are rated for continuous output current of 0.8 Amperes and are intended for use in demanding servo applications such as head positioning for high-density disk drives. Both of these devices include a precision current sense amplifier that provides accurate control of load current. The UC3174B is designed for ground referenced current sensing using the device's Current Sense pins, while the UC3175B is optimized for sensing current with a single resistor in series with the load. These power amplifiers have a very low output saturation voltage and will operate down to 4V supply levels. Power output stage protection includes current limiting and thermal shutdown.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and force a built-in head park function when either is below minimum. When activated by either the UV comparator, or a command at the separate PARK input, the park circuitry will override the amplifier inputs to convert the power outputs to a programmable constant voltage source which will hold regulation as the supply voltage falls to below 3.0 Volts. Added features include a POWER OK flag output, a LIMIT input to force the drive output to its maximum level in either polarity, and a over-riding INHIBIT input to disable all amplifiers and reduce quiescent supply current.

This device is packaged in a power PLCC surface mount configuration which maintains a standard 28-pin outline, but with 7 pins along one edge allocated to ground for optimum thermal transfer. And is also available in a 24-pin surface mount SOIC package.

6

BLOCK DIAGRAM



Note: Pin numbers refer to PLCC package.

UDG-92054

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN,+Vc) 20V
UV Comparator, and Digital Inputs
  Maximum forced voltage ..... -0.3V to 10V
  Maximum forced current ..... ±10mA
C/S Inputs
  Maximum forced voltage ..... -0.3V to 20V
  A and B Amplifier Inputs ..... -0.3V to +VIN
Open Collector Output Voltages 20V
A and B Output Currents (continuous)
  Source ..... Internally Limited
  Sink 1.0A
Parking Drive Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (pulsed) 1A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

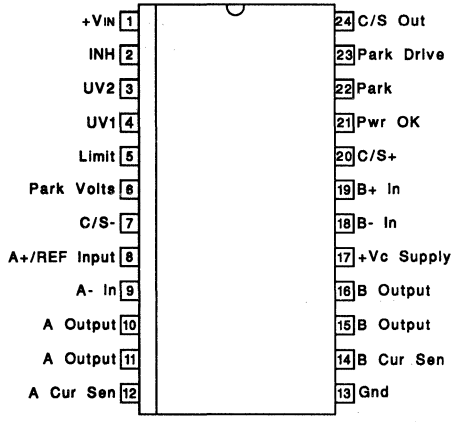
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals. "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Thermal Data

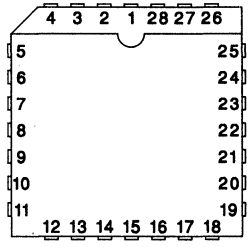
QP Package:
Thermal Resistance Junction to Leads,
  θJA ..... 15°C/W
Thermal Resistance Junction to Ambient,
  θJA ..... 40°C/W

CONNECTION DIAGRAMS

SOIC-24 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
INH	2
UV2	3
UV1	4
Limit	5
Park Volts	6
C/S-	7
A+/REF Input	8
A- In	9
A Output	10
A Cur Sen	11
Gnd (Heat Dissipation Pins)	12-18
B Cur Sen	19
B Output	20
+Vc Supply	21
B- In	22
B+ In	23
C/S+	24
Pwr OK	25
Park	26
Park Drive	27
C/S Out	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications apply for 0°C ≤ TA ≤ 70°C, +VIN = 12V, +Vc = +VIN, A+/REF Input = 6V. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+VIN Supply Current	All Amplifier Outputs = 6V		35	42	mA
+Vc Supply Current	IOUT = 0A		1		mA
+VIN UVLO Threshold	Low to High		2.8	3.0	V
UVLO Threshold Hysteresis			200		mV
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current		-1.5	-0.5		µA
UV Thresholds	Low to High, Other Input = 5V	1.48	1.50	1.52	V
UV Threshold Hysteresis		15	25	40	mV
Pwr OK VSAT	IOUT = 5mA			0.45	V
Pwr OK Leakage	VOUT = 20V			5	µA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated specifications apply for 0°C ≤ T_A ≤ 70°C, +V_{IN} = 12V, +Vc = +V_{IN}, A+/REF INPUT = 6V. T_A=T_J.

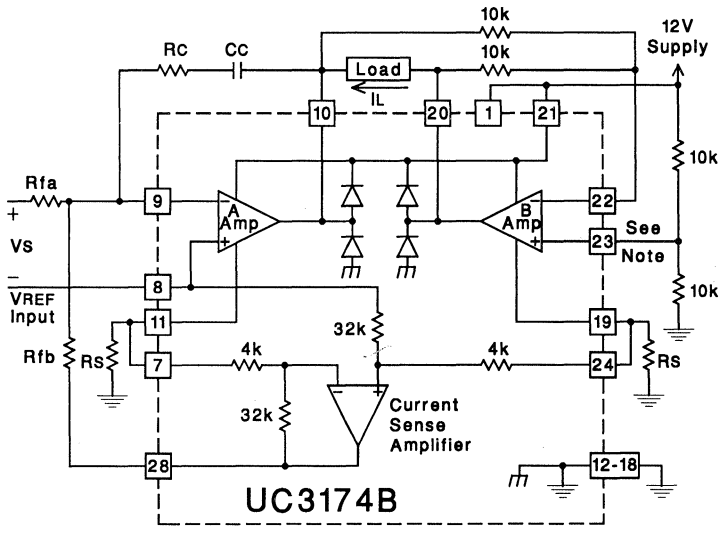
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER AMPLIFIERS A and B					
Input Offset Voltage	V_{CM} = 6V, A Amplifier			8	mV
	B Amplifier			12	mV
Input Offset Drift	Note 1, A Amplifier Only			25	µV/°C
Input Bias Current	V_{CM} = 6V, except A+/REF Input	-500	-150		nA
Input Offset Current	V_{CM} = 6V, B Amplifier Only			200	nA
Input Bias Current at A+/Ref Input	(A+/Ref–C/S+)/36k, T_J = 25°C, UC3174B Only	20	28	35	µA/V
	(A+/Ref–C/S+)/12k, T_J = 25°C, UC3175B Only	60	84	105	µA/V
Differential Sense Error Current	Note 2, I_L = 5mA	-500		500	µA
	I_L = 500mA		3	8	mA
CMRR	1V ≤ V_{CM} ≤ 10V	70	90		dB
PSRR	+V_{IN} = 4V to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	V_{OUT} = 1V, Sinking 500mA to V_{OUT} = 11V, Sourcing 500mA	3.0	15.0		V/mV
Slew Rate	1 to 13V, 13 to 1V, T_J = 25°C		1	2.1	V/µs
Unity Gain Bandwidth	Note 1, A Amplifier		2		MHz
	Note 1, B Amplifier		1		MHz
High-Side Current Limit		0.8	1.0		A
Output Saturation Voltage	High-Side, I_{SOURCE} = 250mA		0.7		V
	High-Side, I_{SOURCE} = 800mA		0.85		V
	Low-Side, I_{SINK} = 250mA		0.3		V
	Low-Side, I_{SINK} = 800mA		0.4		V
	Total, I_{OUT} = 250mA		1.0	1.2	V
	Total, I_{OUT} = 800mA		1.25	1.6	V
High Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
Low Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	V_{CM} = 6V			2.0	mV
	V_{CM} = 0V, UC3174B Only			5.0	mV
Input Offset Change with Ref Input	2V A+/Ref 10V, UC3174B Only			500	µV/V
Input Offset Change with Common Mode Input	0V ≤ V_{CM} ≤ 12V, UC3175B Only			1500	µV/V
Input Offset Drift	Note 1			8	µV/°C
Voltage Gain	-0.5V ≤ V_{DIFF} ≤ +0.5V, Vcm = 0V, UC3174B Only	7.8	7.9	8.0	V
	-1.0V ≤ V_{DIFF} ≤ +1.0V, V_{CM} = 6V, UC3175B Only	1.95	2.00	2.05	V
Output Saturation Voltage	Low-Side, I_{SINK} = 1.5mA		0.3	0.5	V
	High-Side, I_{SOURCE} = 1.5mA		0.4	0.7	V
Maximum A+/Ref Input	Volts Below +V_{IN}, C/S+ & C/S- = B_{OUTPUT} Max @ 10mA Output Current, +V_{IN} = 4.5V, UC3175B only, C/S VIO ≤ 5mV		2.6	3.0	V
PARKING FUNCTION					
Park Input Threshold		0.7	1.1	1.7	V
Park Input Current	Park Input = 1.7V		60	100	µA
Park Drive Saturation Voltage, PD_{VSAT}	I_{SINK} = 100mA		0.3	0.5	V
Parking Drive Leakage	V_{OUT} = 20V			100	µA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated specifications apply for 0°C ≤ T_A ≤ 70°C, $+V_{IN}$ = 12V, $+V_C$ = $+V_{IN}$, A+/REF Input = 6V. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTION (cont.)					
Amplifier A Aux Input Bias Current		-500	-150		nA
Amplifier A Saturation Voltage, A_{HVSAT}	I_{SOURCE} = 50mA, $+V_{IN}$ = 3V		0.65	0.8	V
Regulating Voltage at Park Volts		1.47	1.50	1.53	V
Minimum Parking Supply Voltage	A_{HVSAT} + PD_{VSAT} ≤ 1.3V @ 50mA		1.7	1.9	V
AUXILIARY FUNCTIONS					
Limit Input Low Voltage	A Output Forced Low	0.7	0.8		V
Limit Input High Voltage	A Output Forced High		2.2	2.3	V
Limit Inactive		1.2		1.8	V
Limit Open Circuit Voltage		1.45	1.50	1.55	V
Limit Input Resistance	1.2V ≤ Limit Input ≤ 1.8V		10		kΩ
Inhibit Input Threshold		0.7	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V		400	700	µA
Supply Current when Inhibited	The sum of $+V_{IN}$ and +Vc currents		2	6	mA
Thermal Shutdown Temperature			165		°C

Note 1: This specification not tested in production.
Note 2: This specification is a measure of the accuracy of the differential current sense scheme using the Current Sense pins of the UC3174B. The error current specified is defined as I_{CSA} - I_{CSB} - I_L, where I_{CSA} and I_{CSB} are respectively the currents out of the A and B current sense pins, with load current, I_L, flowing out of the B and into the A amplifier outputs. Similarly, the error current is measured as I_{CSB} - I_{CSA} - I_L, with I_L flowing from A into B.

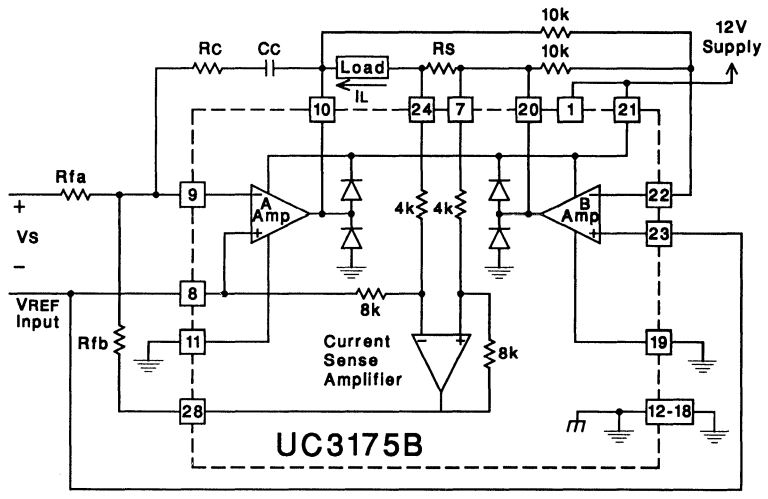
UC3174B Ground-Referenced Current Sensing



For maximum voltage swing, Pin 23 should see $+V_{IN}/2$. If V_{REF} at Pin 8 is at this level, then the divider is not necessary and Pin 23 can also be connected to the V_{REF} input.

$$Go = \frac{I_L}{Vs} = \frac{Rfb}{Rfa \bullet 8 \bullet Rs}$$

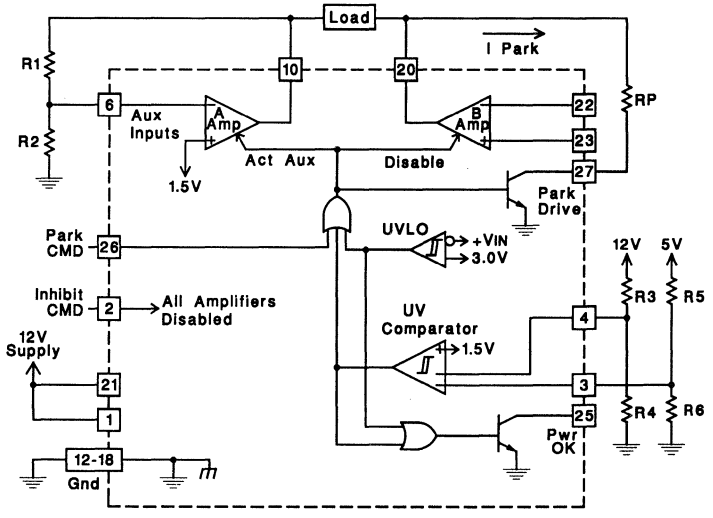
UC3175B Series Current Sensing



UDG-92058

$$Go = \frac{I_L}{Vs} = \frac{Rfb}{Rfa \bullet 2 \bullet Rs}$$

Parking Function



UDG-92059

Notes: Parking voltage = 1.5V • (R1 + R2) / R2 - (IL • RP)
RP is optional for current limiting.
Inhibit and Park Inputs are active high.
Pwr OK is low on power failure.

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Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

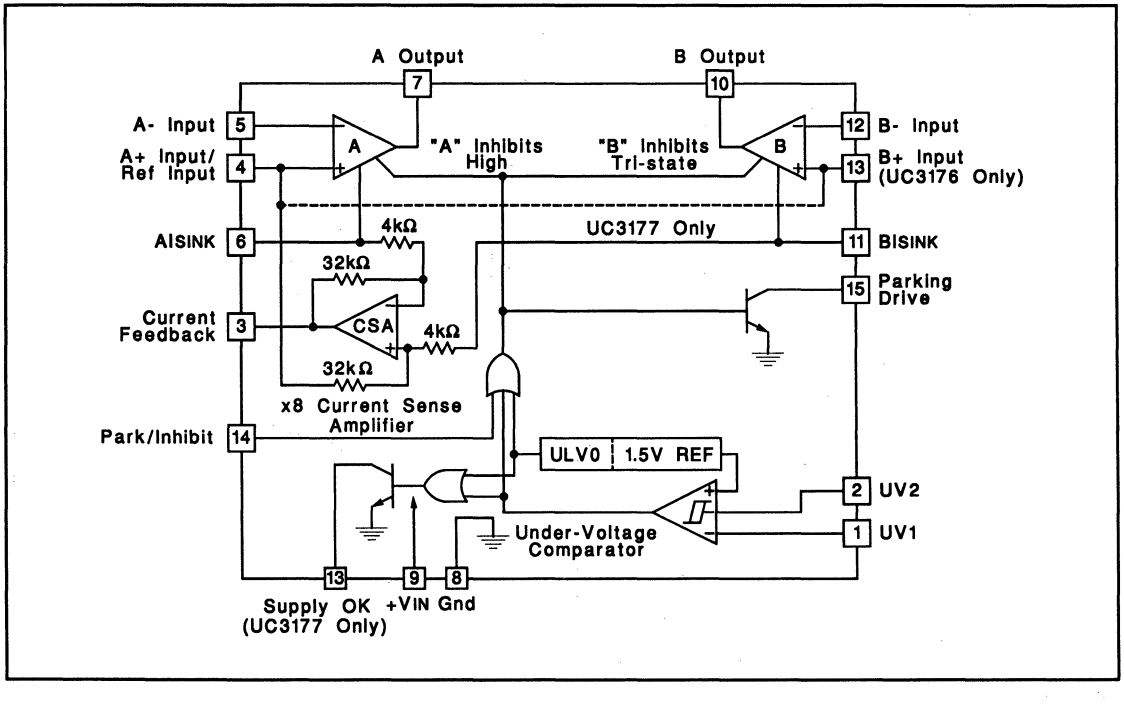
DESCRIPTION

The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit command input.

The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics. The parts are packaged in the 15 pin Multiwatt package with a maximum θJC of 3°C/Watt. For lower power applications a surface mount 28 pin PLCC package is available. Consult packaging section of databook for package details.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply voltage, (+VIN) 40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)
  Maximum forced voltage . . . . . -0.3V to 10V
  Maximum forced current . . . . . ±10mA
Other Input Voltages . . . . . -0.3V to +VIN
AISINK and BISINK Voltages . . . . . -0.3V to 6V
Open Collector Output Voltages 40V
A and B Output Currents (Continuous)
  Source . . . . . Internally Limited
  Sink 2.5A
Total Supply Current (Continuous) 4A
Parking Drive Output Current (Continuous) 200mA
Supply OK Output Current, UC3177 (Continuous) . . . 30mA
Operating Junction Temperature . . . . . -55°C to +150°C
Power Dissipation at TC = +75°C
  QP package 4W
Storage Temperature . . . . . -65°C to +150°C

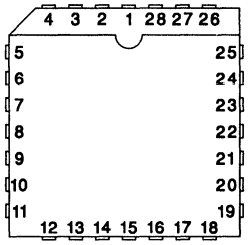
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

THERMAL DATA

QP package:
Thermal Resistance Junction to Leads, θJC . . . . . 15°C/W
Thermal Resistance Junction to Ambient, θJC . . . . . 50°C/W

CONNECTION DIAGRAM

PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
B Output	2
BISINK(Sense)	3
BISINK	4
N/C	5-7
B- Input	8
*	9
Park/Inhibit	10
Parking Drive	11
Gnd (Heat Flow Pins)	12-18
UV1	19
UV2	20
Current Feedback	21
A+ Input	22
A- Input	23
N/C	24
AISINK	25
AISINK(Sense)	26
A Output	27
Gnd	28

**Pin 9: UC3176, B+ Input*
UC3177, Supply OK

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0 to 70°C, +VIN = 12V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 12V		18	25	mA
	+VIN = 35V		21	30	mA
UVOL Threshold	+VIN low to high		2.8	3.0	V
	Threshold Hysteresis		220	300	mV
Power, Amplifier, A and B					
Input Offset Voltage	VCM = 6V, VOUT = 6V			8	mV
Input Bias Current	VCM = 6V, Except A+ Input	-500	-100		nA
Input Bias Current at A+/Reference Input	(A+/Ref - BISINK)/36kohms; TJ = 25°C	23	28	35	µA/V
Input Offset Current B Amp (UC3176 Only)	VCM = 6V			200	nA
CMRR	VCM = 1 to 33V, +VIN =35V, VOUT = 6V	70	100		dB
PSRR	+VIN = 5 to 35V, VCM = 2.5V	70	100		dB
Large Signal Voltage Gain	VOUT = 3V, w/IOUT = 1A to VOUT = 9V, w/IOUT = -1A	1.5	4		V/mV
Thermal Feedback	+VIN = 20V, Pd = 20W at opposite output		25	200	µV/W
Saturation Voltage	IOUT = -2A, High Side, TJ = 25°		1.9		V
	CIOUT = 2A, Low Side, TJ = 25°C		1.6		V
	Total VSAT at 2A, TJ = 25°C		3.5	3.7	V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/µs
Differential IOUT Sense Error Current	IOUT(A) = -IOUT(B), /IOUT/- /AISINK - BISINK/				
in Bridge Configuration	IOUT ≤200mA		3.0	6.0	mA
	IOUT ≤ 2A		5.0	10	mA
High Side Current Limiting	=VIN - VOUT < 12V		-2.7	-2.0	A

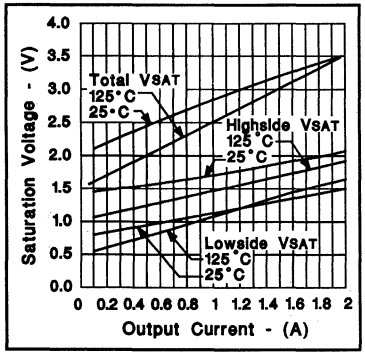
6

ELECTRICAL CHARACTERISTICS:

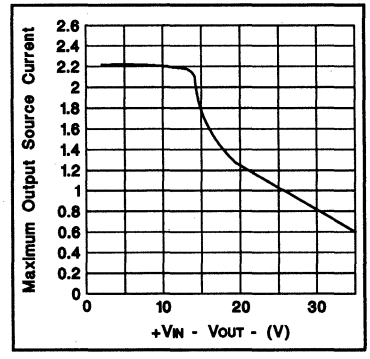
Unless otherwise stated, specifications hold for T_A = 0 to 70°C, $+V_{IN}$ = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 0V, A+/Ref at 6V			3	mV
	Ref = 2V to 20V, $+V_{IN}$ = 35, change with Ref input voltage			600	µV/V
Thermal Gradient Sensitivity	$+V_{IN}$ = 20V, Ref = 10V Pd = 20W @ A or B output		5.0	75	µV/W
PSRR	Ref = 2.5V, $+V_{IN}$ = 5 to 35V	70	100		dB
Gain	/AI_{SINK} - BI_{SINK}/ ≤ 0.5V	7.8	8	8.1	V/V
Slew Rate			2		V/µS
3dB Bandwidth			1		MHz
Max Output Current	I_{SOURCE} = $+V_{IN}$ - V_{OUT} = 0.5V	2.5	3.5		mA
Output Saturation Voltage	I_{SOURCE} = 1.5mA, High Side		0.15	0.30	V
	I_{SINK} = 5mA, Low Side		1.4	1.7	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold Hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	-2	-.05		µA
Supply OK V_{SAT} (UC3177 Only)	I_{OUT} = 5mA			0.45	V
Supply OK Leakage (UC3177 Only)	V_{OUT} = 35V			5	µA
Park/Inhibit					
Park/Inhibit Thl'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	µA
Parking Drive Saturation Voltage	I_{OUT} = 100mA		0.3	0.7	V
Parking Drive Leakage	V_{OUT} = 35V			15	µA
Thermal Shutdown					
Shutdown Temperature			165		°C

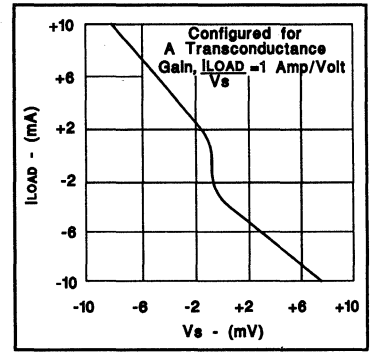
Output Saturation Voltage vs Current



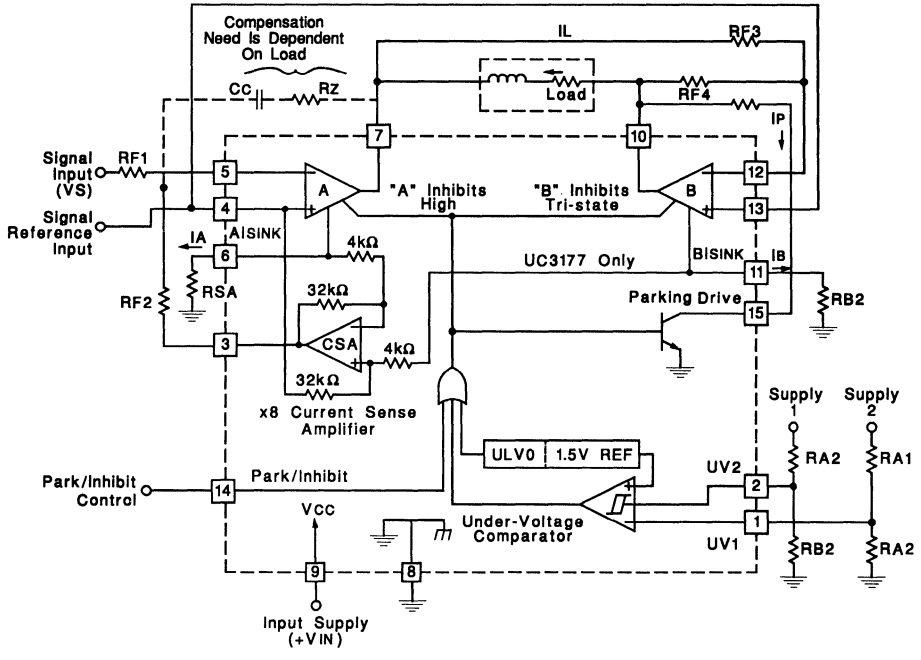
Maximum Source Current vs +VIN - VOUT



Crossover Current Error Characteristic

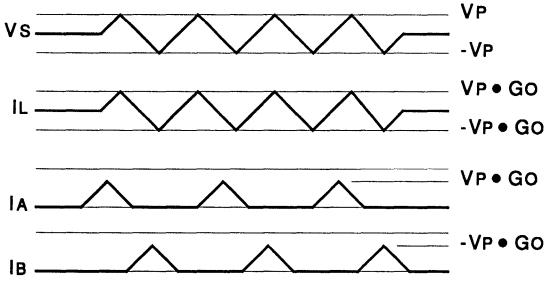


APPLICATION AND OPERATION INFORMATION



6

WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

Transconductance (GO) = $\frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \times \left(\frac{1}{8R_S}\right)$

with: $R_{SA} = R_{SB}$ and $R_{F3} = R_{F4}$

Parking Current (I_P) = $\frac{V_{IN} - 1.5}{R_P + R_L}$

where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
High to Low Threshold, (V_{LH}) = 1.425 (R_A + R_B)/R_B
Low to High Threshold, (V_{HL}) = 1.5 (R_A + R_B)/R_B

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Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- ±450mA Load Current
- 1.2V Typical Total Vsat at 450mA
- Programmable Over-Current Control
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Range Bandwidth Control
- Inhibit Input and UVLO
- 3V to 15V Operation
- 12mA Quiescent Supply Current

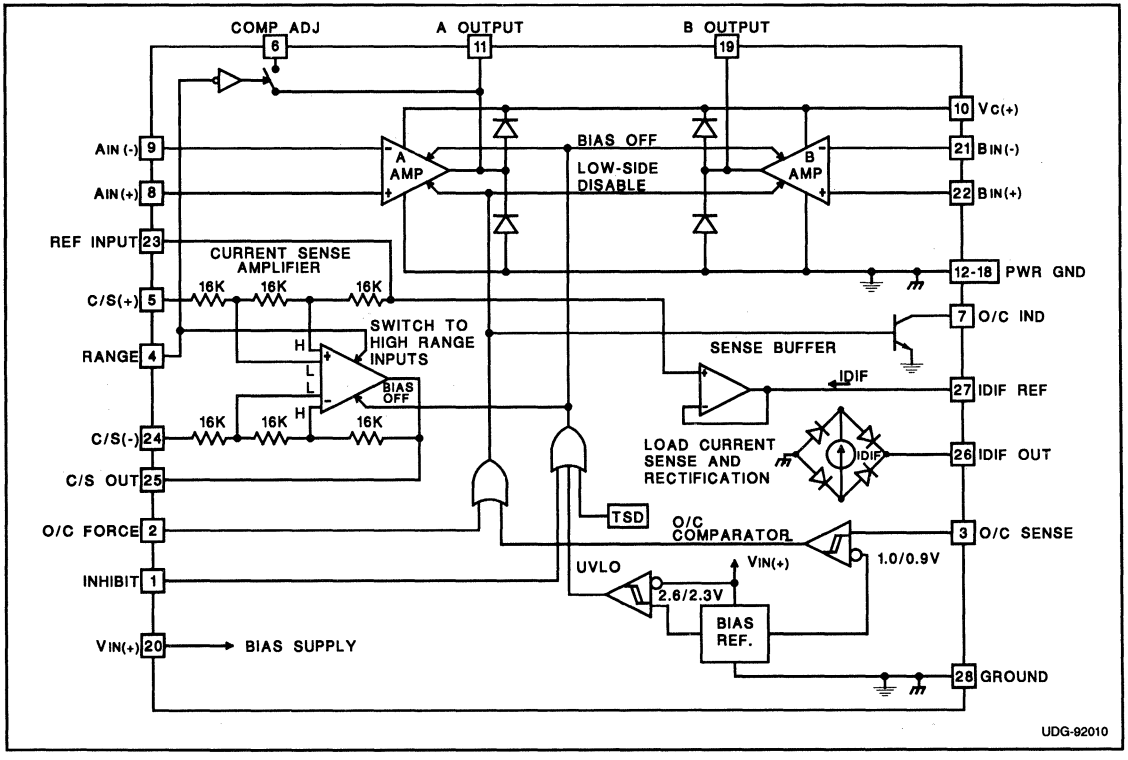
DESCRIPTION

The UC3178 full-bridge power amplifier, rated for continuous output current of 0.45 Amperes, is intended for use in demanding servo applications. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3178 is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited, the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a load current sensing and rectification function that can be configured with the device's over-current comparator to provide tight control on the maximum commanded load current. The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

This device is packaged a power PLCC, "QP" package which maintains a standard 28-pin outline, but with 7 pins along one edge directly tied to the die substrate for improved thermal performance.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (V_{IN}(+), Vc(+)) 20V
O/C Sense, Logic Inputs, and REF Input
  Maximum forced voltage ..... -0.3V to 10V
  Maximum forced current ..... ±10mA
A & B Amplifier Inputs ..... -0.3V to (V_{IN}(+) + 1.0V)
O/C Indicate Open Collector Output Voltage 20V
A and B Output Currents(continuous)
  Source ..... Internally Limited
  Sink 0.6A
Output Diode Current (pulsed)* 0.5A
O/C Ind Output Current(continuous) 20mA
Operating Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C

**Notes: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.*

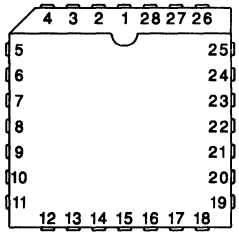
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
  Thermal Resistance Junction to Leads, θjl ..... 15°C/W
  Thermal Resistance Junction to Ambient, θja ... 30-40°C/W

Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAM

PLCC - 28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Inhibit	1
O/C Force	2
O/C Sense	3
Range	4
C/S(+)	5
Comp Adj	6
O/C Ind	7
A_{IN}(+)	8
A_{IN}(-)	9
Vc(+) Supply	10
A Output	11
Pwr Gnd	12
Pwr Gnd	13
Pwr Gnd	14
Pwr Gnd	15
Pwr Gnd	16
Pwr Gnd	17
Pwr Gnd	18
B Output	19
V_{IN}(+)	20
B_{IN}(-)	21
B_{IN}(+)	22
REF Input	23
C/S(+)	24
C/S Out	25
IDIF Out	26
IDIF REF	27
Ground	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications hold for T_A = 0°C to 70°C, Vc(+) = V_{IN}(+) = 12V, REF Input = V_{IN}(+)/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
V_{IN} (+)Supply Current			12	16	mA
Vc(+) Supply Current	I_{OUT} = OA		1.2	2.0	mA
Total Supply Current	Supplies = 5V,I_{OUT} = OA		12	16	mA
	Supplies = 12V,I_{OUT} = OA		13	18	mA
V_{IN}(+) UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysterisis			300		mV
Over-Current (O/C) Comparator					
Input Bias Current	V input = 0.8V	-1.0	-.01		µA
Thresholds	low to high	0.97	1.0	1.03	V
Threshold Hysterisis		85	100	115	mV
O/C IND Vsat	I_{OUT} = 5mA, V input low		0.2	0.45	V
O/C IND Leakage	V_{OUT} = 20V			5.0	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 6V			4.0	mV
	B Amplifier, V_{CM} = 6V			12.0	mV
Input Bias Current	V_{CM} = 6V	-500	-50		µA
CMRR	V_{CM} = 0.5 to 13V, Supplies = 15V	70	90		dB
PSRR	V_{IN}(+) = 4 to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA to V_{OUT} = 10.5V, I_{OUT} = -300mA	3.0	15.0		V/mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated specifications hold for T_A = 0°C to 70°C , Vc(+) = V_{IN}(+) = 12V, REF Input = V_{IN}(+)/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A & B (cont.)					
Gain Bandwith Product	A Amplifier		2.0		MHz
	B Amplifier		1.0		MHz
Slew Rate			1.0		V/µs
High-Side Current Limit		0.45	0.65		A
Output Saturation Voltage	High-Side, I_{OUT} = -100mA		0.75		V
	High-Side, I_{OUT} = -300mA		0.85		V
	High-Side, I_{OUT} = -450mA		0.9		V
	Low-Side, I_{OUT} = 100mA		0.2		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 450mA		0.30		V
	Total Vsat, I_{OUT} = 100mA		0.95	1.2	V
	Total Vsat, I_{OUT} = 300mA		1.05	1.4	V
	Total Vsat, I_{OUT} = 450mA		1.25	1.6	V
High-Side Diode, Vf	I_D = 450mA		1.30		V
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 6V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change	V_{CM} = -1V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
with Common Mode Input	V_{CM} = -1V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = -1mA, Referenced to = V_{IN}(+)		0.1	0.3	V
Input Bias Current at Ref. Input	(REF Input - C/S(+))/48kohms, Tj = 25°C	15	21	27	µA/V
Load Current Sense and Rectification					
Sense Buffer Offset Voltage	REF Input to IDIF REF, I_{OUT} = ±1mA			10	mV
Sense Buffer CMRR	I_{OUT} = ±1mA, REF Input = 2V to 10V	70	90		dB
IDIF REF to IDIF Out Current	IDIF = ± 100µA, IDIF Out = 1V	0.95	1.0	1.05	A/A
Ratio	IDIF = ±1mA, IDIF Out = 1V	0.94	1.0	1.06	A/A
IDIF Out Supply Sensitivity	IDIF Out = ± 1mA, V_{IN}(+) = 4V to 15V,REF Input = 2V		1.0	5.0	µA/V
IDIF Out Common Mode Sensitivity	I_{OUT} = ±1mA, REF Input = 2V to10V, IDIF Out = 1V				
(delta IDIF Out/delta REF Input)			1.0	5.0	µA/V
Auxiliary Functions					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		µA
O/C Force Input Threshold		0.6	1.1	1.7	V
O/C Force Input Current	O/C Force Input = 1.7V		50	100	µA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	µA
COMP ADJ Pin Saturation	Range Input = 0V, Pin Current = ±500µA, Referenced				
Voltage	to A_{OUT}		0.02	0.1	V
COMP ADJ Leakage Current	Range Input = 1.7V, Supplies = 12V				
	A_{OUT}-$V_{Comp\ Adj}$ = ±6V			5.0	µA
Total Supply Current When Inhibited	V_{IN}(+) and Vc(+) currents		1.0	1.5	mA
Thermal Shutdown Temperature			165		°C

PIN DESCRIPTIONS:

A & B OUT: Outputs for the A & B power amplifiers, providing differential drive to the load during normal operation. During a UVLO, Inhibit, or O/C condition both of these outputs will be in a high, source only state. High-side diodes are included to catch inductive load currents flowing into these pins, inductive kicks on the low-side are caught by the high-side output transistors.

AIN(+): Non-inverting input to the A amplifier. Normally tied to the REF Input when the current sense amplifier is used.

AIN(-): Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

BIN(+): Non-inverting input to the B amplifier. This pin normally sets the reference point for the differential voltage swing at the load.

BIN(-): Inverting input to the B amplifier. Used to program the gain of the B amplifier.

COMP ADJ: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

C/S(+): The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

(REF Input / 2) - 0.3V.

C/S(-): The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, O/C comparator, and other low-level circuitry.

IDIF OUT: Current source output pin. The value of the output current is nominally equal to the magnitude of the current through the IDIF REF pin.

IDIF REF: Output of the IDIF sense buffer. Voltage on this pin will track the applied voltage on the REF Input pin. Current through this pin is full wave rectified and appears as a current sourced from the IDIF OUT pin.

Inhibit : A high impedance logic input that disables the A and B power amplifiers, the IDIF sense buffer, and the Current Sense amplifier. This input has an internal pull-up that will inhibit the device if the input is left open.

O/C Force: Logic input that forces the O/C condition.

O/C IND: Open collector ouput that indicates, with an active low state, an O/C condition.

O/C Sense: Input to the Over Current Comparator. When this input is above its 1V threshold the low-side devices of both the A & B power amplifiers will be disabled forcing a high, source only, state at both outputs.

PWR GND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

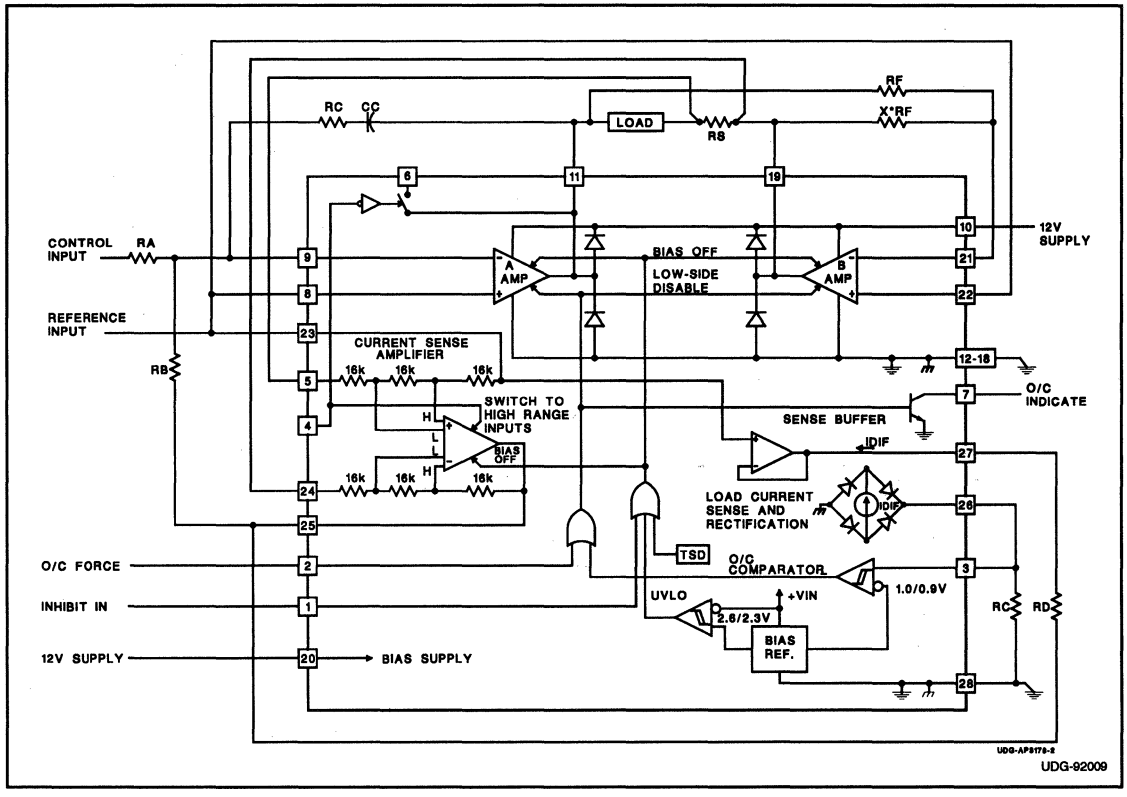
Range: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REF Input: Sets the Reference level at the C/S Output, and is normally tied to the system reference level for inputs to the power amplifier.

VIN(+): Provides bias supply to the device. The High-Side drive to the power stages on both the A and B amplifiers is referenced to this pin. The High-side saturation voltages, and UVLO are specified and measured with respect to this supply pin.

VC(+): This supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are to be activated. This pin can operate approximately 400mV below the VIN(+) supply without affecting the voltage available to the load.

TYPICAL APPLICATION



Power amplifier transconductance

$$Go = \frac{Il}{Vs} = \frac{RB}{RA} \bullet \frac{1}{AVCS \bullet RS}$$

Peak commanded load current

$$IlMAX = Vo/c \bullet \frac{RD}{RS \bullet AVCS \bullet RE}$$

where:

Il is the load current

Vs is the input command voltage

AVCS is the current sense amplifier gain

= 2.0 in low range mode

= 0.5 in high range mode

VO/C is the 1.0V over-current comparator threshold

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- Fixed-Frequency 4 Quadrant PWM for Servo Applications
- TTL Compatible Hall Inputs
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- 15 Lead, 25W Multiwatt Package

DESCRIPTION

The UC3622 is a brushless DC motor drive capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board oscillator and latched PWM comparator provide the necessary circuitry for implementing a fixed-frequency, pulse width modulated servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been reduced by limiting the output dv/dt to 150µs for any load condition.

The UC3622 will decode and drive all 3-phase motors with hall decode schemes compatible with Table 1. All other schemes can be decoded with the addition of a single external inverter. Consult factory for availability of military versions.

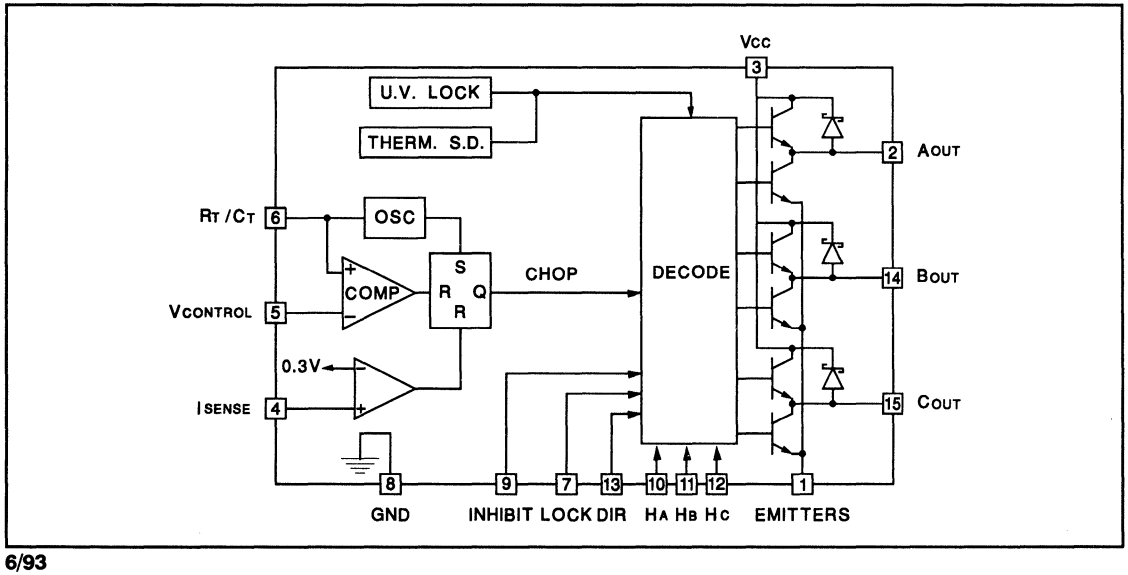
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, Vcc 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100µsec), Io 3A
  Repetitive (80% on - 20% off; tON = 10ms) 2.5A
  DC Operation 2A
Analog Inputs . . . . . -0.3 to +Vcc
Logic Inputs . . . . . -0.3 to +Vcc
Total Power Dissipation (at TCASE = 75°C) 25W
Storage and Junction Temperature . . . . . -40°C to +150°C

Note 1: All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

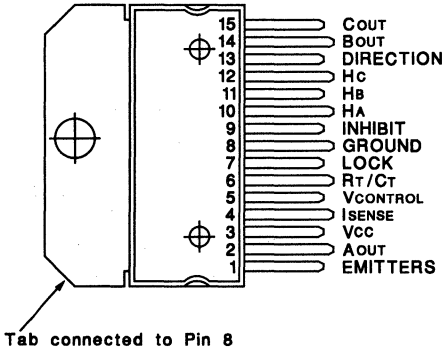
6

BLOCK DIAGRAM



CONNECTION DIAGRAM

(TOP VIEW)
V, VH PACKAGE



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; Vcc (PIN3) = 20V, R_T = 47k, C_T = .015µF, T_A = T_J.

PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PWM Comparator Section					
Input Offset Voltage				10	mV
Input Bias Current				5	µA
Current Sense Section					
Input Bias Current				5	µA
Internal Offset Voltage		.25	0.3	.35	V
Oscillator Section					
Initial Accuracy	T_J = 25°C	9	10	11	kHz
Temperature Stability	Over Operating Range		2		%
Ramp Peak			3.6		V
Ramp Valley			1.3		V
Decoder Section					
High-Level Input Voltage		2.5			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	µA
Low-Level Input Current		-10			µA
Output Section					
Output Leakage Current	Vcc = 40V			500	µA
V_F, Schottky Diode	Io = 2A		1.5	2.0	V
Total Output Voltage Drop	Io = 2A, Note 3		3.0	3.6	V
Output Rise Time	R_L = 44Ω		150		ns
Output Fall Time	R_L = 44Ω		150		ns
Under-Voltage Lockout					
Start-up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current			32	55	mA

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3: The total voltage drop is defined as the sum of both top and bottom side driver.

TABLE 1

STEP	INHIBIT	DIR	HA	HB	HC	LOCK	AOUT	BOUT	COUT
1	0	1	1	0	0	1	Ø	H	L
2	0	1	1	1	0	1	L	H	Ø
3	0	1	1	1	1	1	L	Ø	H
4	0	1	0	1	1	1	Ø	L	H
5	0	1	0	0	1	1	H	L	Ø
6	0	1	0	0	0	1	H	Ø	L
1	0	0	1	1	1	1	H	Ø	L
2	0	0	1	1	0	1	H	L	Ø
3	0	0	1	0	0	1	Ø	L	H
4	0	0	0	0	0	1	L	Ø	H
5	0	0	0	0	1	1	L	H	Ø
6	0	0	0	1	1	1	Ø	H	L
-	1	X	X	X	X	X	Ø	Ø	Ø
-	0	X	X	X	X	0	H	Ø	L

H = HIGH OUTPUT L = LOW OUTPUT Ø = OPEN (TRISTATE) OUTPUT

CIRCUIT DESCRIPTION

The UC3622 is designed for implementation of a complete 3-phase brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit function.

DECODER

Table 1 shows the logic scheme employed to decode and drive each of three high current, totem pole, output stages. A forward/reverse signal, Pin 13, is used to provide direction. At any time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by chopping all drivers during current control (fixed-frequency PWM), producing a four-quadrant, regenerative mode drive. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses.

HALL INPUTS

The Hall input pins (#10, 11, 12) are not provided with internal pull-up resistors. If these are required for the Hall devices, they must be added externally.

CURRENT LIMIT

Referring to Figure 1, emitter current is sensed across RLIMIT and fed back through a low pass filter to the current sense, Pin 4. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1k and 1000pF range. An internal 0.3V reference voltage limits the motor current to

$$I_{MAX} = \frac{0.3}{R_{LIMIT}}$$

TIMING

An RC circuit at Pin 6 is used to set the PWM frequency, as shown in Figure 2. The frequency is determined by the formula:

$$f \approx \frac{Vosc - 2.43}{2.27 R_T C_T} \; [Hz]$$

NOTE: RT should be chosen so that

$$50\mu A < \frac{Vosc - 2.27}{2.27 R_T} < 1\,mA$$

INHIBIT

The INHIBIT input (Pin 9) must be low during normal operation. A high level at this pin forces all three outputs to the open state, and can be used to allow the motor to coast.

LOCK

A low level at LOCK (Pin 7), together with a low level at INHIBIT sets the following output condition:

AOUT ..... HIGH
BOUT .... OPEN
COUT .... LOW

This can be used as part of a circuit intended to force the motor shaft to a desired parking position.

PROTECTION FUNCTIONS

Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-stated until Vcc is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

APPLICATION MATERIAL

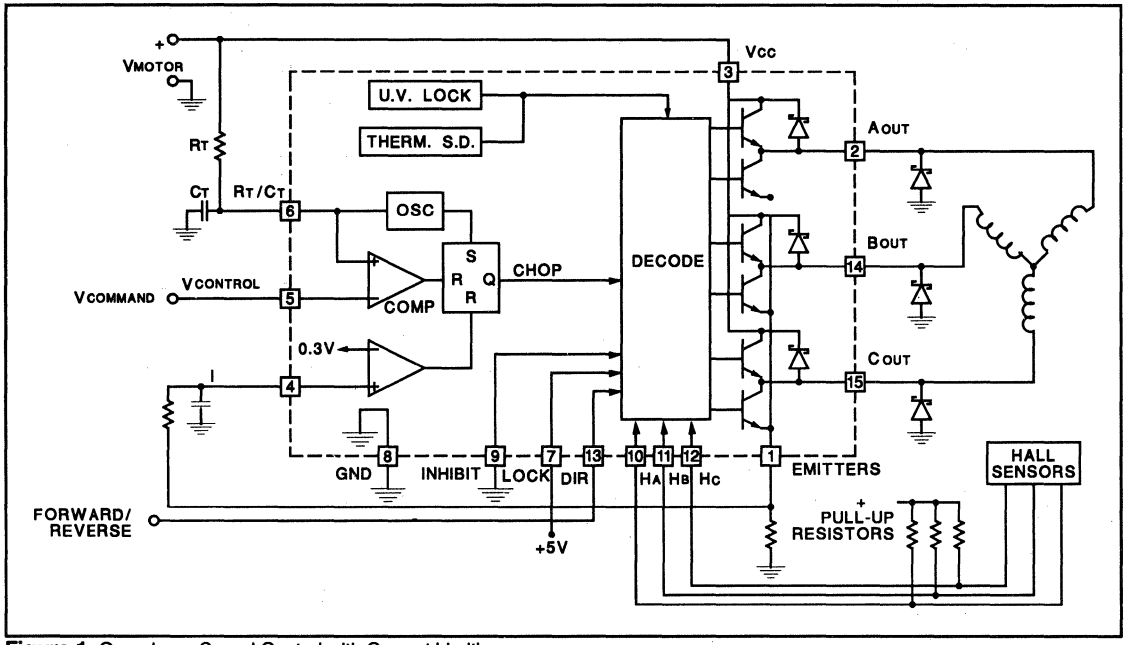


Figure 1. Open Loop Speed Control with Current Limiting

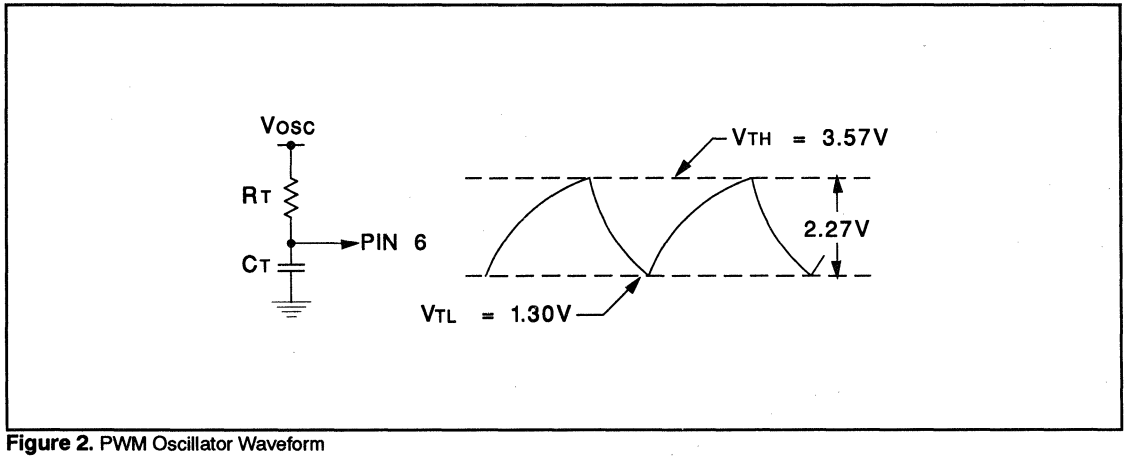


Figure 2. PWM Oscillator Waveform

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Low Noise Switchmode Driver for 3-∅ Brushless DC Motors

FEATURES

- 1A Continuous, 2A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Velocity Control Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection

DESCRIPTION

Designed specifically for noise-sensitive environments, the UC3623V monolithic driver IC offers the high efficiency of a chopper drive and the low EMI attainable with controlled output slew rates.

The UC3623 is a brushless DC motor drive capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/μs for any load condition.

The UC3623 offers standard 120 electrical degree. Hall decoding per Table 1. Consult factory for availability of military versions.

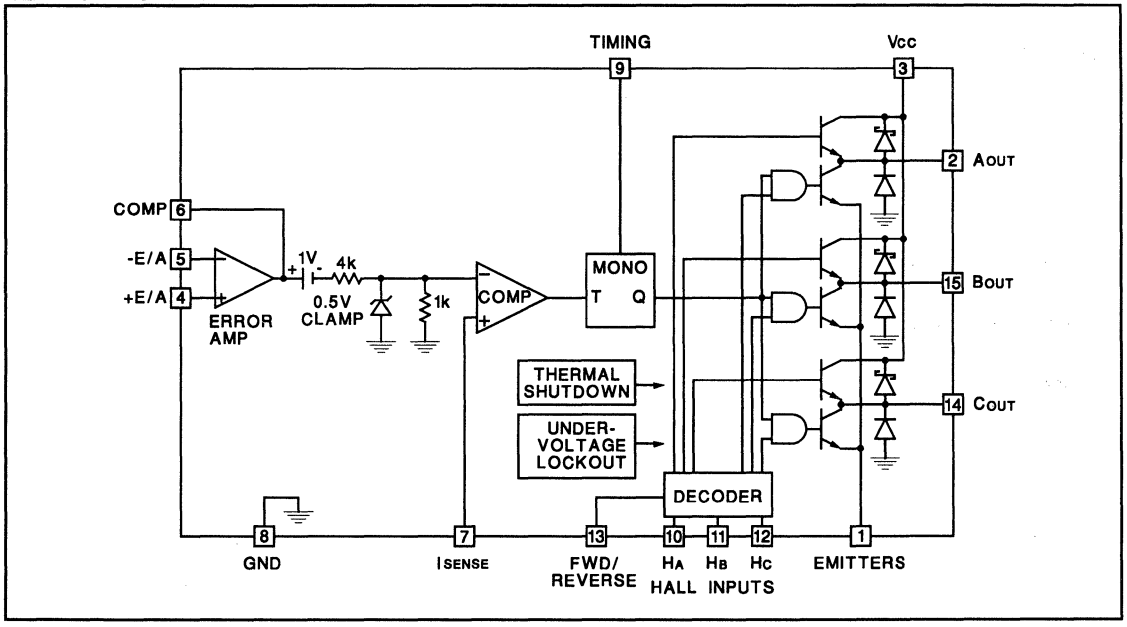
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, Vcc 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100μsec), Io 2A
  Repetitive (80% on - 20% off; TON = 10ms) 1.5A
  DC Operation 1A
Analog Inputs ..... -0.3 to +Vcc
Logic Inputs ..... -0.3 to +Vcc
Storage and Junction Temperature ..... -40°C to +150 °C

Note 1: All voltages are with respect to ground, pin 8. Currents are positive into, negative out of the specified terminal.

6

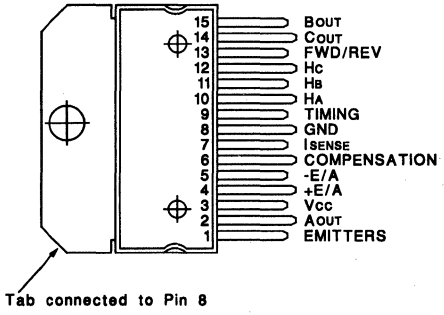
BLOCK DIAGRAM



6/93

CONNECTION DIAGRAM

V-VH PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; V_{CC} (PIN 3) = 20V, R_T = 10k, C_T = 2.2nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error Amplifier Section					
Input Offset Voltage			1.5	10	mV
Input Bias Current			-.25	-2.0	µA
Input Offset Current			15	250	nA
Common Mode Range	V_{CC} = 8V to 40V	0		V_{IN}-2	V
Open Loop Gain	ΔV_{PIN6} = 1V to 4V	80	100		dB
Unity Gain Bandwidth	T_J = 25°C, Note 2		0.8		MHz
Output Sink Current	V_{PIN6} = 1V		2		mA
Output Source Current	V_{PIN6} = 4V		8		mA
Current Sense Section					
Input Bias Current			-2.0	-5	µA
Internal Clamp		.425	0.5	.575	V
Divider Gain		.180	0.2	.220	V/V
Internal Offset Voltage		.8	1.0	1.2	V
Timing Section					
Output Off Time		18	20	22	µs
Upper Mono Threshold			5.0		V
Lower Mono Threshold			2.0		V
Decoder Section					
High-Level Input Voltage		2.2			V
Low-Level Input Voltage				0.8	V
High-Level Input Current				10	µA
Low-Level Input Current		-10			µA
Output Section					
Output Leakage Current	V_{CC} = 40V			500	µA
V_F, Schottky Diode	I_O = 1A		1.5	2.0	V
V_F, Substrate Diode	I_O = 1A		2.2	3.0	V
Total Output Voltage Drop	I_O = 1A, Note 3		3.0	3.6	V
Output Rise Time	R_L = 44Ω		350		ns
Output Fall Time	R_L = 44Ω		170		ns

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 3: The total voltage drop is defined as the sum of both top and bottom side driver.

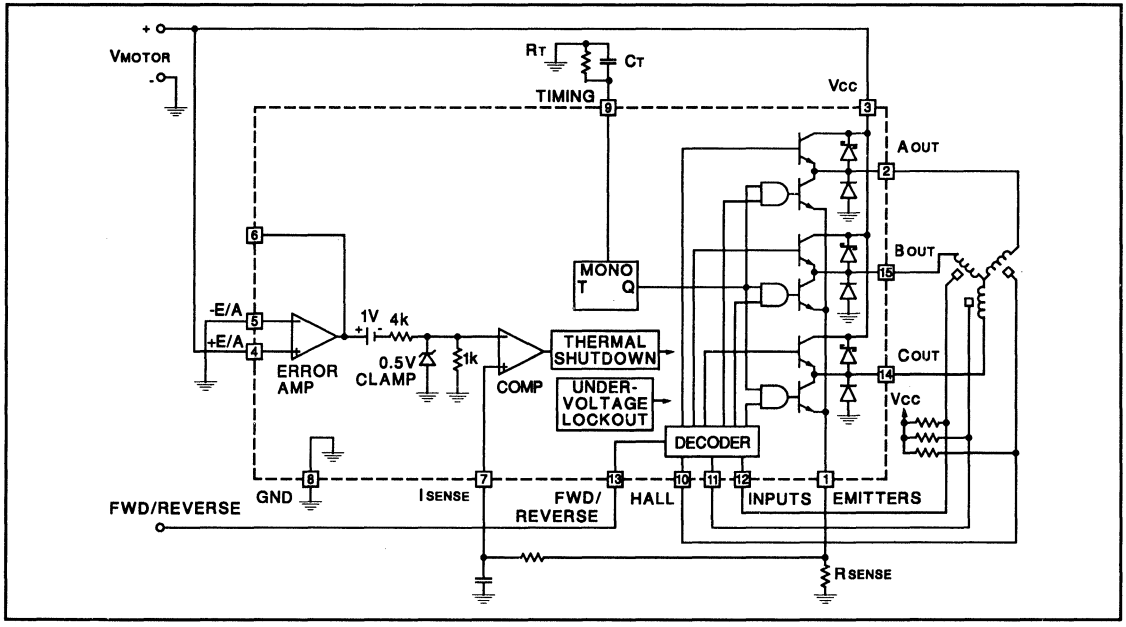
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C; V_{CC} (PIN 3) = 20V, R_T = 10k, C_T = 2.2nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Under-Voltage Lockout					
Start-Up Threshold				8.0	V
Threshold Hysteresis			0.5		V
Thermal Shutdown					
Junction Temperature		150		180	°C
Total Standby Current					
Supply Current			32	55	mA

TABLE 1

STEP	FWD/REV	H_A	H_B	H_C	A_{OUT}	B_{OUT}	C_{OUT}
1	1	1	0	1	H	L	O
2	1	1	0	0	H	O	L
3	1	1	1	0	O	H	L
4	1	0	1	0	L	H	O
5	1	0	1	1	L	O	H
6	1	0	0	1	O	L	H
1	0	1	0	1	L	H	O
2	0	1	0	0	L	O	H
3	0	1	1	0	O	L	H
4	0	0	1	0	H	L	O
5	0	0	1	1	H	O	L
6	0	0	0	1	O	H	L

TYPICAL APPLICATIONS



3-∅ Brushless DC Open Loop Motor Drive with Current Limit

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

Low Saturation, Linear Brushless DC Motor Driver

FEATURES

- Total Saturation Voltage of Less Than 1 Volt
- Sink Current Capability of up to 3 Amps
- Quiescent Current Less Than 10mA
- Single Supply 5 Volt Operation
- Motor Voltage of 5 to 40 Volts
- Full Decode for 3 Phase TTL Hall Sensors
- 120 Electrical Degree Logic
- Linear Closed-Loop Motor Current Control

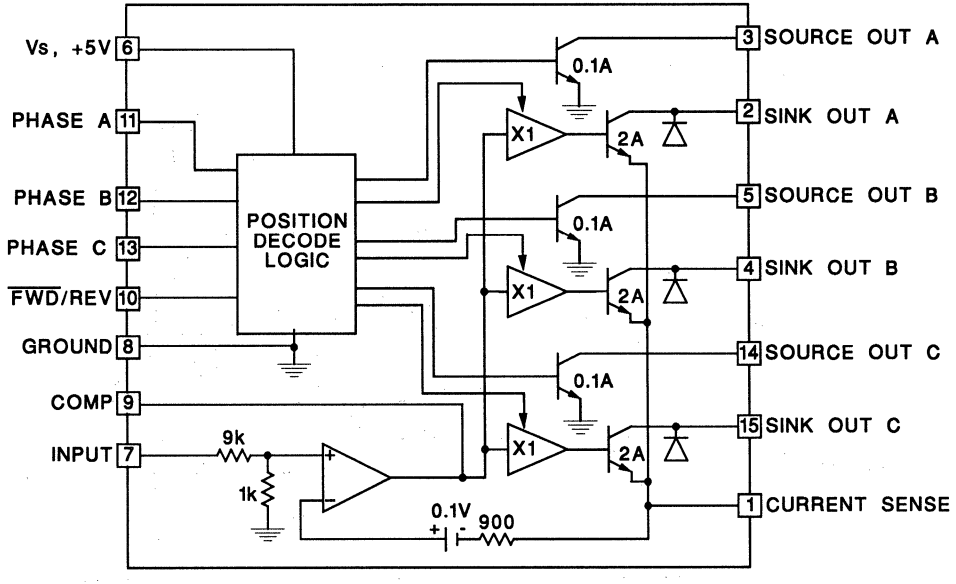
DESCRIPTION

The UC3655 DC motor driver achieves extremely efficient operation by using external PNP transistors selected for low saturation voltage as high side drivers. These are complemented with low side NPN drivers internal to the UC3655 which also have very low saturation losses. The PNP's can be low power devices as they are always switched into saturation by the action of internal 100mA base drivers, while the on-chip NPN's are driven linearly to control motor current. The result is a total source/sink saturation voltage drop of less than 1V at 1A load current.

This controller offers further efficiency by using only a 5V supply with a current requirement proportional to motor current. The quiescent supply current with the outputs off is less than 10mA.

In addition to the power output stages, the UC3655 contains 120 electrical degree hall logic decoding with forward, reverse, and inhibit functions selectable by a single pin. Also included in control amplifier to drive the sink output current linearly response to an input command voltage. Finally, full protection is offered with under-voltage lockout, current limiting, and thermal shutdown. The UC3655 is packaged in both a high-power 15-pin Multiwatt® plastic package and, for low power requirements, a 28-pin PLCC surface mount configuration.

BLOCK DIAGRAM



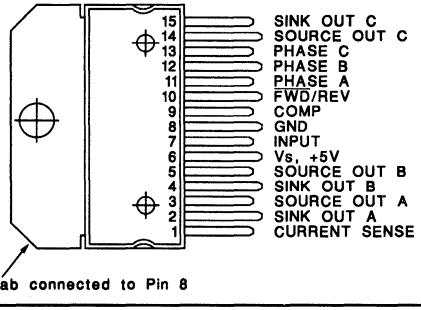
6/93

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, Vs 7V
Output Voltage, Vc (Source and Sink) 40V
Sink Output Current 3A
Source Drive Current ..... Internally Limited
Logic and Analog Inputs ..... -0.3 to 7V
Total Power Dissipation (At T_{TAB} = 75°C)
V Package 25W
QP Package 4.0W
Storage and Junction Temperature ..... -40°C to 150°C

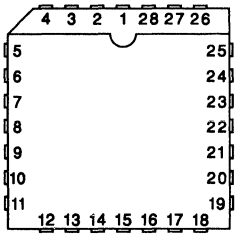
Note 1: All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

UC3655V(H)
(TOP VIEW)



CONNECTION DIAGRAMS

PLCC-28
(TOP VIEW)
QP Package



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
GND	1-2
COMP	3
FWD/REV	4
PHASE A	5
PHASE B	6
PHASE C	7
SOURCE OUT C	8
N/C	9
SINK OUT C	10
N/C	11
GND (HEAT FLOW)	12-18
CURRENT SENSE (SENSE)	19
CURRENT SENSE (FORCE)	20
SINK OUT A	21
SOURCE OUT A	22
N/C	23
SINK OUT B	24
SOURCE OUT B	25
Vs, +5V	26
N/C	27
INPUT	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, Vs = 5.0 Volts and R_{SENSE} = 0.2Ω, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sink Driver Section					
Collector Leakage	V_C = 40V			500	µA
Saturation Voltage	I_C = 2A, R_S = 0		0.8	1.0	V
	I_C = 1A, R_S = 0		0.4	0.5	V
Coll. Diode V_f	I_f = -1A			2.0	V
Source Driver Section					
Collector Leakage	V_C = 40V			100	µA
Saturation Voltage	I_C = 0.1A		1.9	2.3	V
Current Limit	V_C = 5V, T_A = 25°C	100	175	300	mA
Amplifier Section					
Input Low Voltage	Sink Current = 0A	0.8	1.0	1.2	V
Input High Voltage	Sink Current = 2A	4.5	5.0	5.5	V
Closed Loop Transconductance	Sink Current = 0-2A	0.45	0.5	0.55	S
Control Amp Transconductance	I_{COMP} = ± 50µA		0.2		mS
Voltage Gain to Current Sense	V_{IN} = 2-3V		-20		dB
Input Bias Current	V_{IN} = 5V		0.5	1.0	mA
Comp. Source Current	V_{IN} = 5V, V_{COMP} = .9V	-50	-100	-150	µA
Comp. Sink Current	V_{IN} = 0V, V_{COMP} = .9V	50	100	150	µA
Decoder Section					
High-level Input Voltage	Phase Input	2.2			V
Low-level Input Voltage	Phase Input			0.8	V
High-level Input Current	Phase Input			10	µA
Low-level Input Current	Phase Input	-10			µA

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, V_S = 5.0 Volts and R_{SENSE} = 0.2Ω, T_A = T_J.

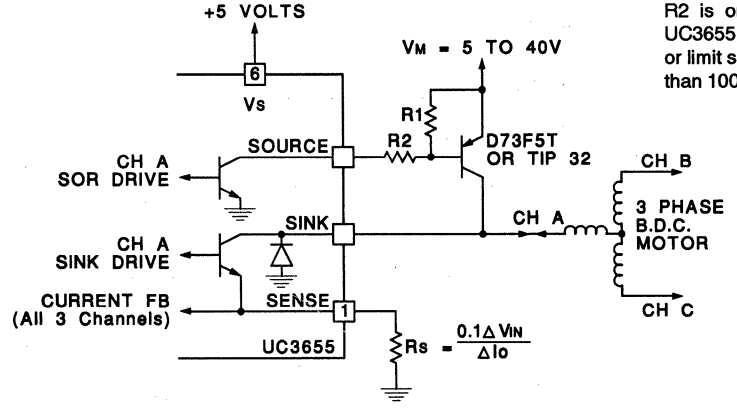
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Decoder Section (cont.)					
Input Voltage to Inhibit	$\overline{FWD}$/REV	1.8		3.2	V
Forward Command Input V	$\overline{FWD}$/REV			0.6	V
Reverse Command Input V	$\overline{FWD}$/REV	4.4			V
Supply Section					
Turn-on Threshold	Vs Low to High	3.5	4.0	4.7	V
Threshold Hysteresis			0.5		V
Supply Current	Outputs Inhibited		6.0	10	mA
Supply Current	Sink Current = 2A		25	100	mA
Thermal Shutdown	Junction Temperature		150		°C
Shutdown Hysteresis	Junction Temperature		5		°C

DECODE LOGIC TRUTH TABLE:

Inhibit	Phase Input			Source Drive			Sink Output			Motor Term		
$\overline{FWD}$/REV	A	B	C	A	B	C	A	B	C	A	B	C
X	0	0	0	Off	Off	Off	Off	Off	Off	0	0	0
X	1	1	1	Off	Off	Off	Off	Off	Off	0	0	0
Inhibit	X	X	X	Off	Off	Off	Off	Off	Off	0	0	0
L	1	0	1	On	Off	Off	Off	On	Off	H	L	0
L	1	0	0	On	Off	Off	Off	Off	On	H	0	L
L	1	1	0	Off	On	Off	Off	Off	On	0	H	L
L	0	1	0	Off	On	Off	On	Off	Off	L	H	0
L	0	1	1	Off	Off	On	On	Off	Off	L	0	H
L	0	0	1	Off	Off	On	Off	On	Off	0	L	H
H	1	0	1	Off	On	Off	On	Off	Off	L	H	0
H	1	0	0	Off	Off	On	On	Off	Off	L	0	H
H	1	1	0	Off	Off	On	Off	On	Off	0	L	H
H	0	1	0	On	Off	Off	Off	On	Off	H	L	0
H	0	1	1	On	Off	Off	Off	Off	On	H	0	L
H	0	0	1	Off	On	Off	Off	Off	On	0	H	L

(Note: X = Don't Care; Inh = 2.5 ±1V; H and L levels defined by applications; Motor Term O = High Impedance).

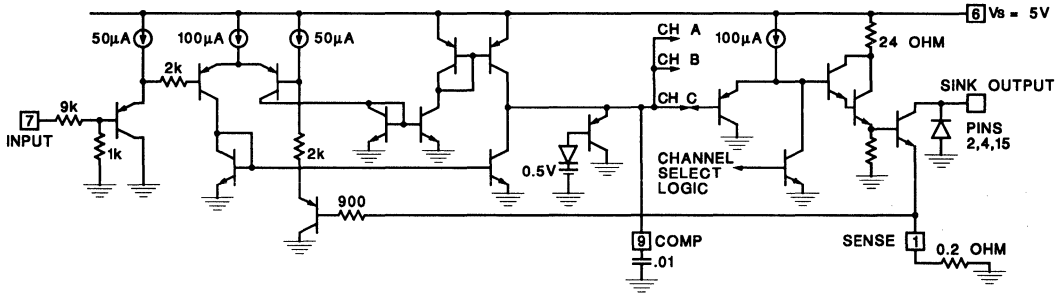
TYPICAL MOTOR DRIVE APPLICATION



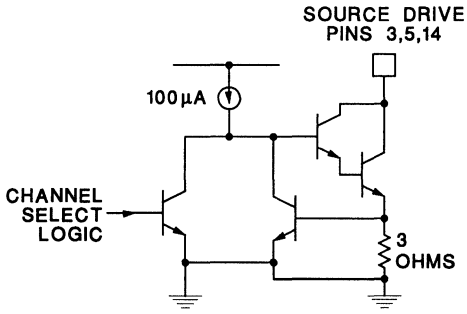
R2 is only used to reduce UC3655 power dissipation or limit source current to less than 100mA

Note: Rs must be non-inductive and located as close as possible to the UC3655 to avoid parasitic oscillations.

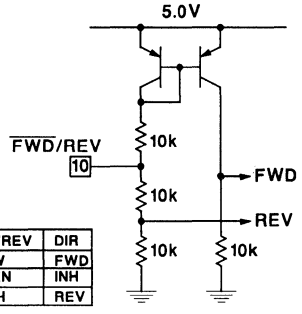
Linear Transconductance Amplifier



Source Drivers

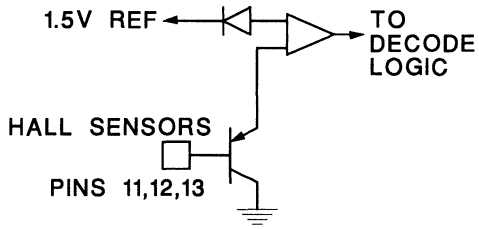


Forward/Reverse Input

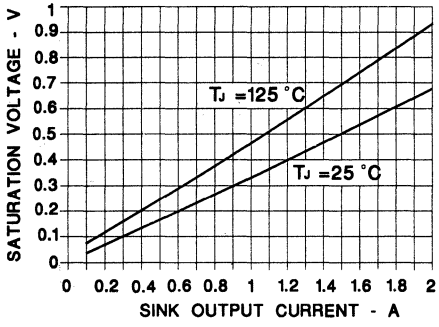


FWD/REV	DIR
LOW	FWD
OPEN	INH
HIGH	REV

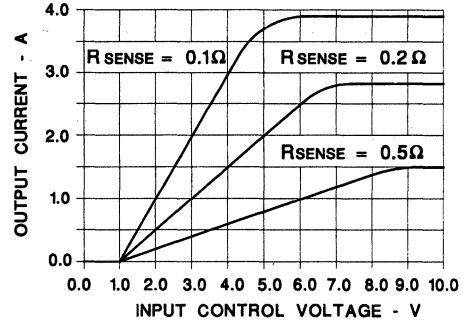
Phase Inputs



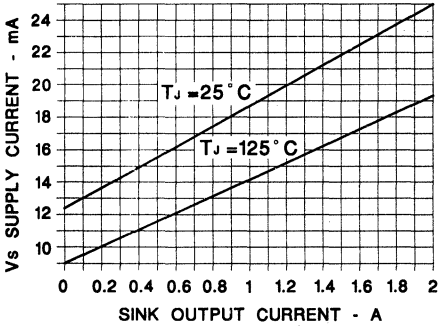
Sink Output Vsat vs Current



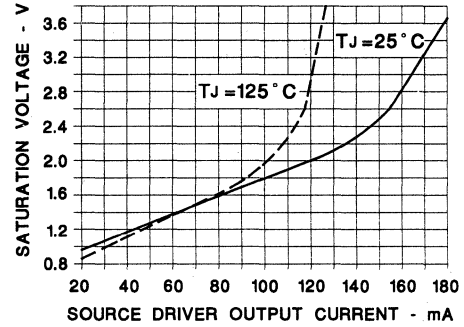
Control Transfer Characteristics



Vs Supply Current vs Sink Current



Source Driver Output Vsat vs Current



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Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability
- Bipolar Output Current up to 1A
- Wide Range of Motor Supply Voltage 10-46V
- Low Saturation Voltage with Integrated Bootstrap
- Built-In Fast Recovery Commutating Diodes
- Current Levels Selected in Steps or Varied Continuously
- Thermal Protection with Soft Intervention

DESCRIPTION

The UC3717A is an improved version of the UC3717, used to switch drive the current in one winding of a bipolar stepper motor. The UC3717A has been modified to supply higher winding current, more reliable thermal protection, and improved efficiency by providing integrated bootstrap circuitry to lower recirculation saturation voltages. The diagram shown below presents the building blocks of the UC3717A. Included are an LS-TTL compatible logic input, a current sensor, a monostable, a thermal shutdown network, and an H-bridge output stage. The output stage features built-in fast recovery commutating diodes and integrated bootstrap pull up. Two UC3717As and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC3717A is characterized for operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, Vcc 7V
- Output Supply, V_M 50V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) Vcc
- Reference Input (Pin 11) 15V

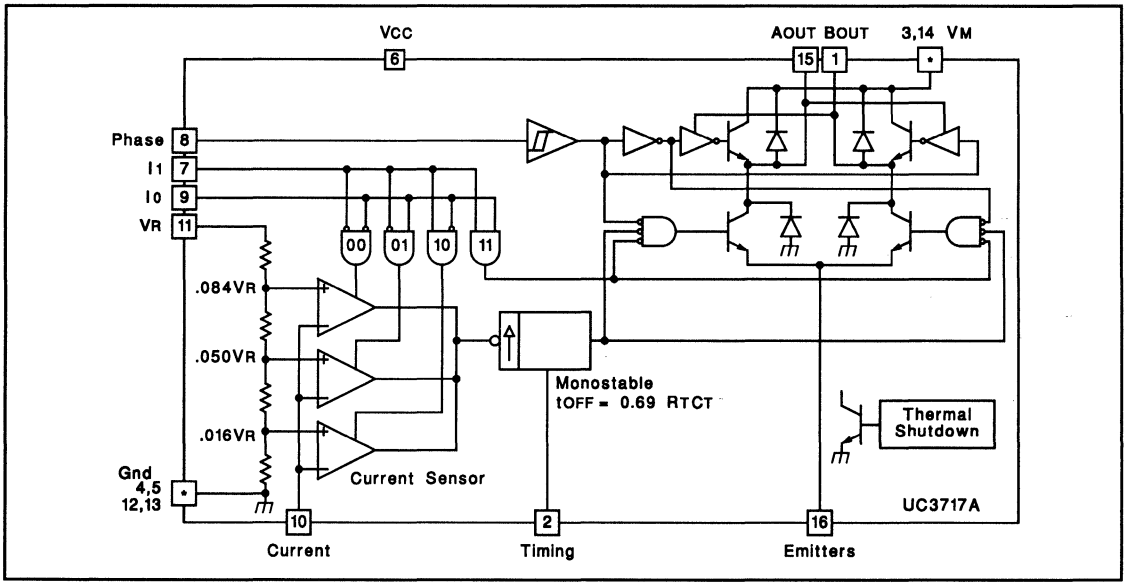
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1.2A
Junction Temperature, T_J ..... +150°C
Storage Temperature Range, Ts ..... -55°C to +150°C

Note 1: All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL-16 package.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

6

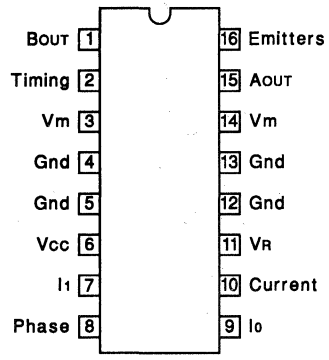
BLOCK DIAGRAM



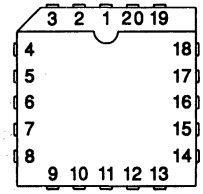
*Consult Factory

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
Vm	4
Gnd	5
N/C	6
Gnd	7
Vcc	8
I1	9
Phase	10
N/C	11
Io	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, Figure 6. V_m = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_m (Pins 3, 14)		10		46	V
Logic Supply Voltage, V_{CC} (Pin 6)		4.75		5.25	V
Logic Supply Current, I_{CC} (Pin 6)	I_O = I_1 = 0		7	15	mA
Thermal Shutdown Temperature		+160		+180	°C
Logic Inputs					
Input Low Voltage, (Pins 7, 8, 9)				0.8	V
Input High Voltage, (Pins 7, 8, 9)		2		V_{CC}	V
Low Voltage Input Current, (Pins 7, 8, 9)	V_I = 0.4V, Pin 8			-100	µA
	V_I = 0.4V, Pins 7 and 9			-400	µA
High Voltage Input Current, (Pins 7, 8, 9)	V_I = 2.4V			10	µA
Comparators					
Comparator Low, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = H	66	80	90	mV
Comparator Medium, Threshold Voltage (Pin 10)	V_R = 5V; I_O = H; I_1 = L	236	250	266	mV
Comparator High, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = L	396	420	436	mV
Comparator Input, Current (Pin 10)				±20	µA
Cutoff Time, t_{OFF}	R_T = 56kΩ, C_T = 820pF	25		35	µs
Turn Off Delay, t_D	(See Figure 5)			2	µs
Source Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -0.5A, Conduction Period		1.7	2.1	V
(See Figure 5)	I_m = -0.5A, Recirculation Period		1.1	1.35	V
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -1A, Conduction Period		2.1	2.8	V
(See Figure 5)	I_m = -1A, Recirculation Period		1.7	2.5	V
Leakage Current	V_m = 40V			300	µA
Diode Forward Voltage, V_F	I_m = -0.5A		1	1.25	V
	I_m = -1A		1.3	1.7	V

ELECTRICAL CHARACTERISTICS (cont.)

(Refer to the test circuit, Figure 6. V_M = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sink Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = 0.5A	8	1.1	1.35	V
	I_m = 1A		1.6	2.3	V
Leakage Current	V_m = 40V			300	µA
Diode Forward Voltage, V_F	I_m = 0.5A		1.1	1.5	V
	I_m = 1A		1.4	2	V

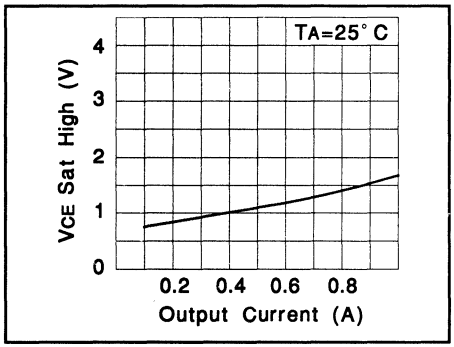


Figure 1: Typical Source Saturation Voltage vs Output Current (Recirculation Period)

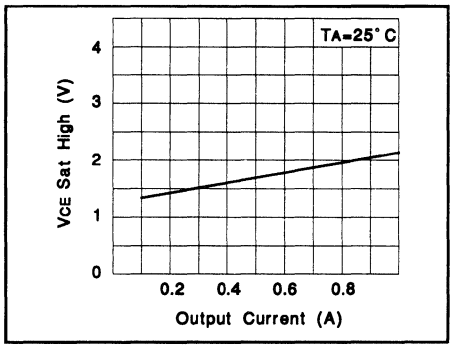


Figure 2: Typical Source Saturation Voltage vs Output Current (Conduction Period)

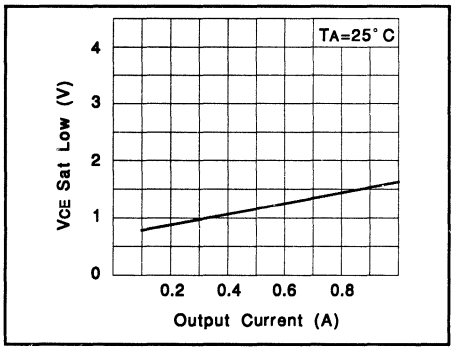


Figure 3: Typical Sink Saturation Voltage vs Output Current

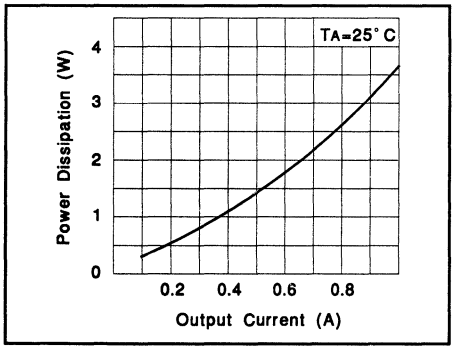


Figure 4: Typical Power Dissipation vs Output Current

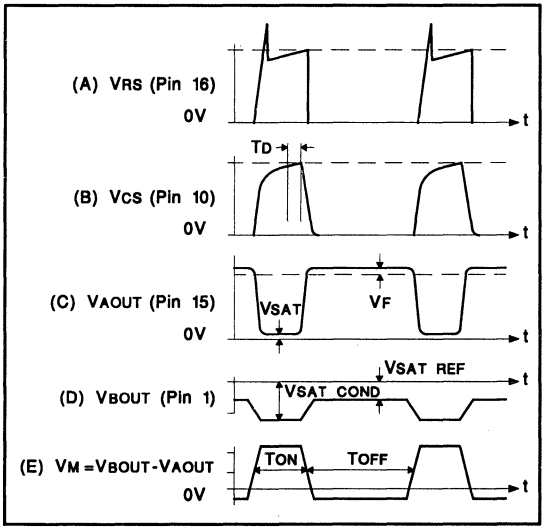


Figure 5: Typical Waveforms with MA Regulating (phase = 0)

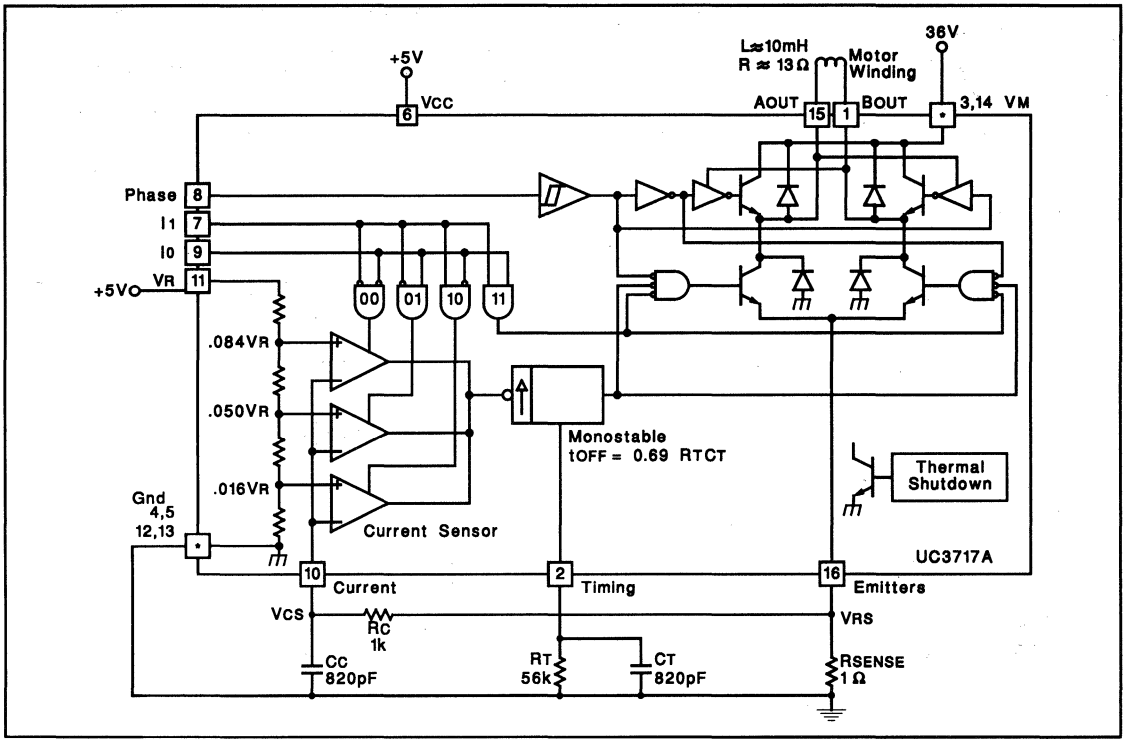


Figure 6: UC3717A Test Circuit

FUNCTIONAL DESCRIPTION

The UC3717A's drive circuit shown in the block diagram includes the following components.

(1) H-bridge output stage
(2) Phase polarity logic
(3) Voltage divider coupled with current sensing comparators
(4) Two-bit D/A current level select
(5) Monostable generating fixed off-time
(6) Thermal protection

OUTPUT STAGE

The UC3717A's output stage consists of four Darlington power transistors and associated recirculating power diodes in a full H-bridge configuration as shown in Figure 7. Also presented, is the new added feature of integrated bootstrap pull up, which improves device performance during switched mode operation. While in switched mode, with a low level phase polarity input, Q2 is on and Q3 is being switched. At the moment Q3 turns off, winding current begins to decay through the commutating diode pulling the collector of Q3 above the supply voltage. Meanwhile, Q6 turns on pulling the base of Q2 higher than its previous value. The net effect lowers the saturation voltage of source transistor Q2 during recirculation, thus improving efficiency by reducing power dissipation.

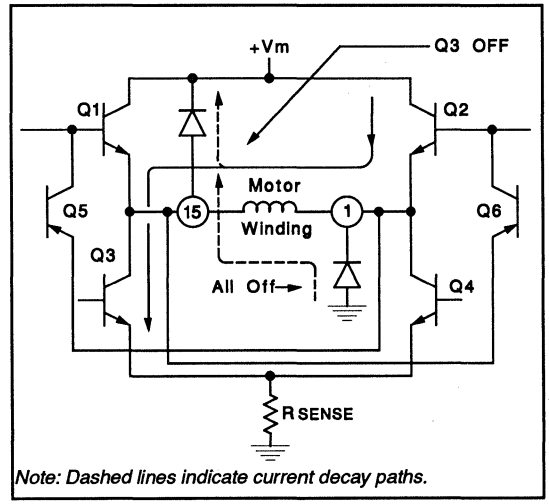


Figure 7: Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

PHASE POLARITY INPUT

The UC3717A phase polarity input controls current direction in the motor winding. Built-in hysteresis insures immunity to noise, something frequently present in switched drive environments. A low level phase polarity input enables Q2 and Q3 as shown in Figure 7. During phase reversal, the active transistors are both turned off while winding current delays through the commutating diodes shown. As winding current decays to zero, the inactive transistors Q1 and Q4 turn on and charge the winding with current of the reverse direction. This delay insures noise immunity and freedom from power supply current spikes caused by overlapping drive signals.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

CURRENT CONTROL

The voltage divider, comparators, monostable, and two-bit D/A provide a means to sense winding peak current, select winding peak current, and disable the winding sink transistors.

The UC3717A switched driver accomplishes current control using an algorithm referred to as "fixed off-time." When a voltage is applied across the motor winding, the current through the winding increases exponentially. The current can be sensed across an external resistor as an analog voltage proportional to instantaneous current. This voltage is normally filtered with a simple Rc low-pass network to remove high frequency transients, and then compared to one of the three selectable thresholds. The two bit D/A input signal determines which one of the three thresholds is selected, corresponding to a desired winding peak current level. At the moment the sense voltage rises above the selected threshold, the UC3717A's monostable is triggered and disables both output sink drivers for a fixed off-time. The winding current then circulates through the source transistor and appropriate diode. The reference terminal of the UC3717A provides a means of continuously adjusting the current threshold to allow microstepping. Table 1 presents the relationship between the two-bit D/A input signal and selectable current level.

TABLE 1

Io	I1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

OVERLOAD PROTECTION

The UC3717A is equipped with a new, more reliable thermal shutdown circuit which limits the junction temperature to a maximum of 180C by reducing the winding current.

PERFORMANCE CONSIDERATIONS

In order to achieve optimum performance from the UC3717A careful attention should be given to the following items.

External Components: The UC3717A requires a minimal number of external components to form a complete control and switch drive unit. However, proper selection of external components is necessary for optimum performance. The timing pin, (pin 2) is normally connected to an RC network which sets the off-time for the sink power transistor during switched mode. As shown in Figure 8, prior to switched mode, the winding current increases exponentially to a peak value. Once peak current is attained the monostable is triggered which turns off the lower sink drivers for a fixed off-time. During off-time winding current decays through the appropriate diode and source transistor. The moment off-time times out, the motor current again rises exponentially producing the ripple waveform shown. The magnitude of winding ripple is a direct function of off-time. For a given off-time T_{OFF}, the values of R_T and C_T can be calculated from the expression:

$$T_{OFF} = 0.69 R_T C_T$$

with the restriction that R_T should be in the range of 10-100k. As shown in Figure 5, the switch frequency Fs is a function of T_{OFF} and T_{ON}. Since T_{ON} is a function of the reference voltage, sense resistor, motor supply, and winding electrical characteristics, it generally varies during different modes of operation. Thus, Fs may be approximated nominally as:

$$Fs = 1/1.5\ (T_{OFF}).$$

Normally, Switch Frequency Is Selected Greater than 20kHz to prevent audible noise, and lower than 100kHz to limit power consumed during the switching cycle.

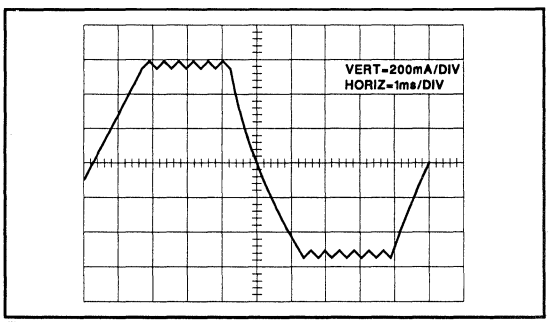


Figure 8: A typical winding current waveform. Winding current rises exponentially to a selected peak value. The peak value is limited by switched mode operation producing a ripple in winding current. A phase polarity reversal command is given and winding current decays to zero, then increases exponentially.

FUNCTIONAL DESCRIPTION (cont.)

Low-pass filter components Rc Cc should be selected so that all switching transients from the power transistors and commutating diodes are well smoothed, but the primary signal, which can be in the range of 1/TOFF or higher must be passed. Figure 5A shows the waveform which must be smoothed, Figure 5B presents the desired waveform that just smoothes out overshoot without radical distortion.

The sense resistor should be chosen as small as practical to allow as much of the winding supply voltage to be used as overdrive to the motor winding. V_{RS}, the voltage across the sense resistor, should not exceed 1.5V.

Voltage Overdrive: In many applications, maximum speed or step rate is a desirable performance characteristic. Maximum step rate is a direct function of the time necessary to reverse winding current with each step. In response to a constant motor supply voltage, the winding current changes exponentially with time, whose shape is determined by the winding time constant and expressed as:

$$I_m = \frac{V_m}{R\,[1-EXP\,(-R_{T/L})]}$$

as presented in Figure 9. With rated voltage applied, the time required to reach rated current is excessive when compared with the time required with over-voltage applied, even though the time constant L/R remains constant. With over-voltage however, the final value of current is excessive and must be prevented. This is accomplished with switch drive by repetitively switching the sink drivers on and off, so as to maintain an average value of current equal to the rated value. This results in a small amount of ripple in the controlled current, but the increase in step rate and performance may be considerable.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1μF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Half-Stepping: In half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90°. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the VR input can be used to boost the current of the single energized winding.

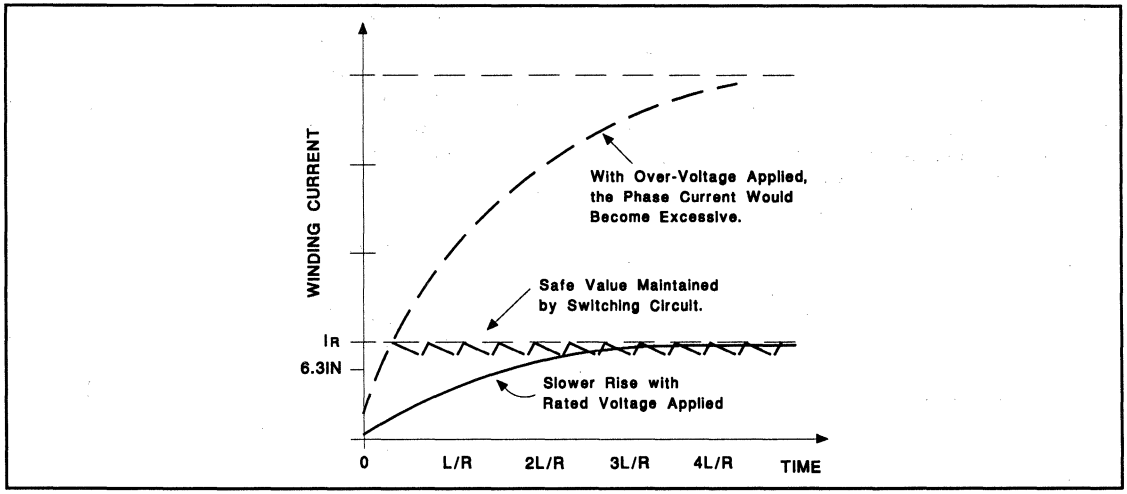


Figure 9: With rated voltage applied, winding current does not exceed rated value, but takes L/R seconds to reach 63% of its final value — probably too long. Increased performance requires an increase in applied voltage, of overdrive, and therefore a means to limit current. The UC3717A motor driver performs this task efficiently.

MOUNTING INSTRUCTIONS

The $R_{THJ-AMB}$ of the UC3717A can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink.

The diagram of Figure 11 shows the maximum package power P_{TOT} and the θ_{JA} as a function of the side " l " of two equal square copper areas having a thickness of 35µ (see Figure 10).

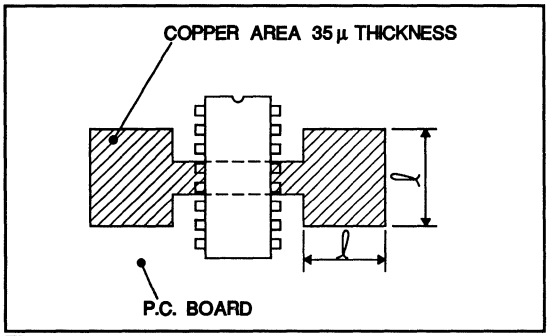


Figure 10: Example of P.C. Board Copper Area which is used as Heatsink.

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

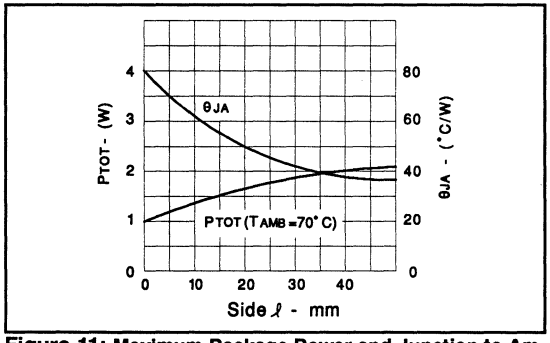


Figure 11: Maximum Package Power and Junction to Ambient Thermal Resistance vs Side "l".

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 12. The input can be controlled by a microprocessor, TTL, LS, or CMOS logic.

The timing diagram in Figure 13 shows the required signal input for a two phase, full step stepping sequence.

Figure 14 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 15 provides the signal shown in Figure 13, and in conjunction with the circuit shown in Figure 12 will implement a pulse-to-step two phase, full step, bi-directional motor drive.

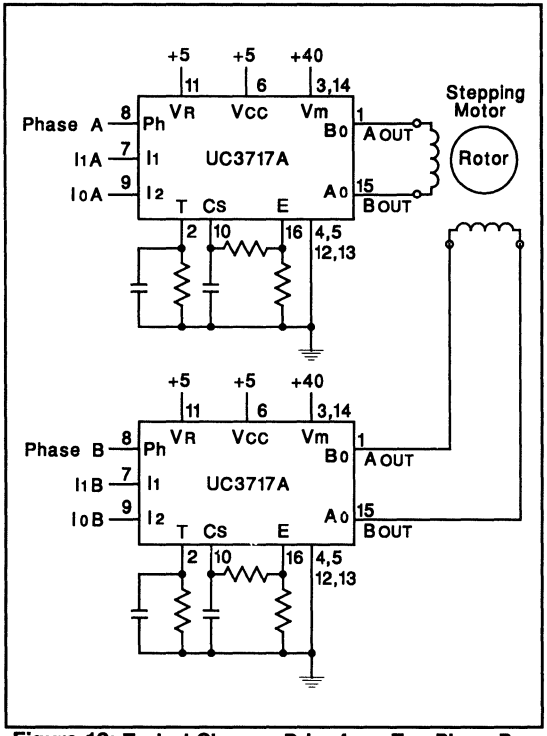


Figure 12: Typical Chopper Drive for a Two Phase Permanent Magnet Motor.

The schematic of Figure 16 shows a pulse to half step circuit generating the signal shown in Figure 14. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at high step rates.

ORDERING INFORMATION

UNITRODE TYPE NUMBER:

UC3717ANE - 16 Pin Dual-in-line (DIL) "Bat Wing" Package

3717AJ - 16 Pin Dual-in-line Ceramic Package

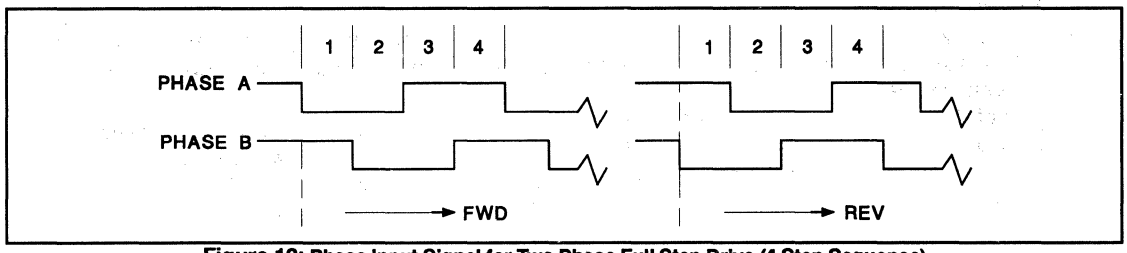


Figure 13: Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

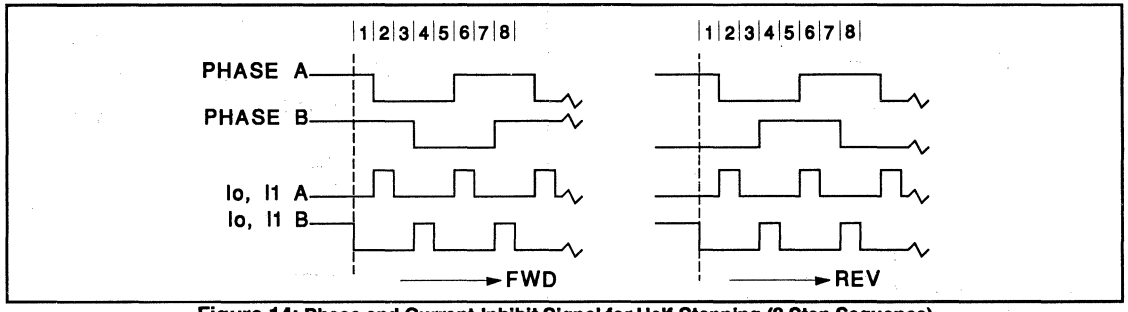


Figure 14: Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

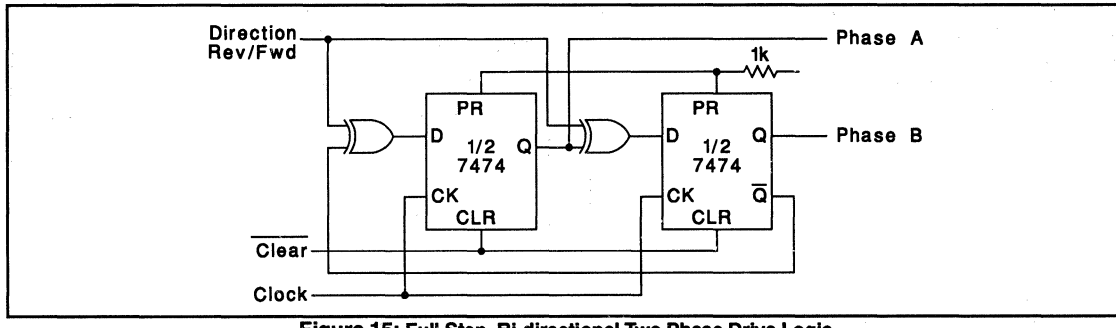


Figure 15: Full Step, Bi-directional Two Phase Drive Logic

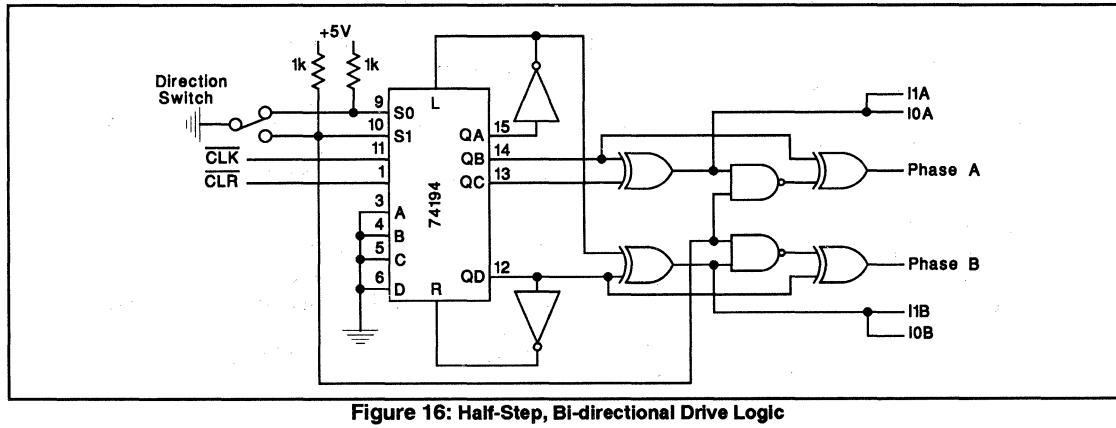


Figure 16: Half-Step, Bi-directional Drive Logic

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FEATURES

- Full-Step, Half-Step and Micro-Step Capability.
- Bipolar Output Current up to 2A.
- Wide Range of Motor Supply Voltage: 10–50V
- Low Saturation Voltage
- Wide Range of Current Control: 5mA–2A.
- Current Levels Selected in Steps or Varied Continuously.
- Thermal Protection and Soft Intervention.

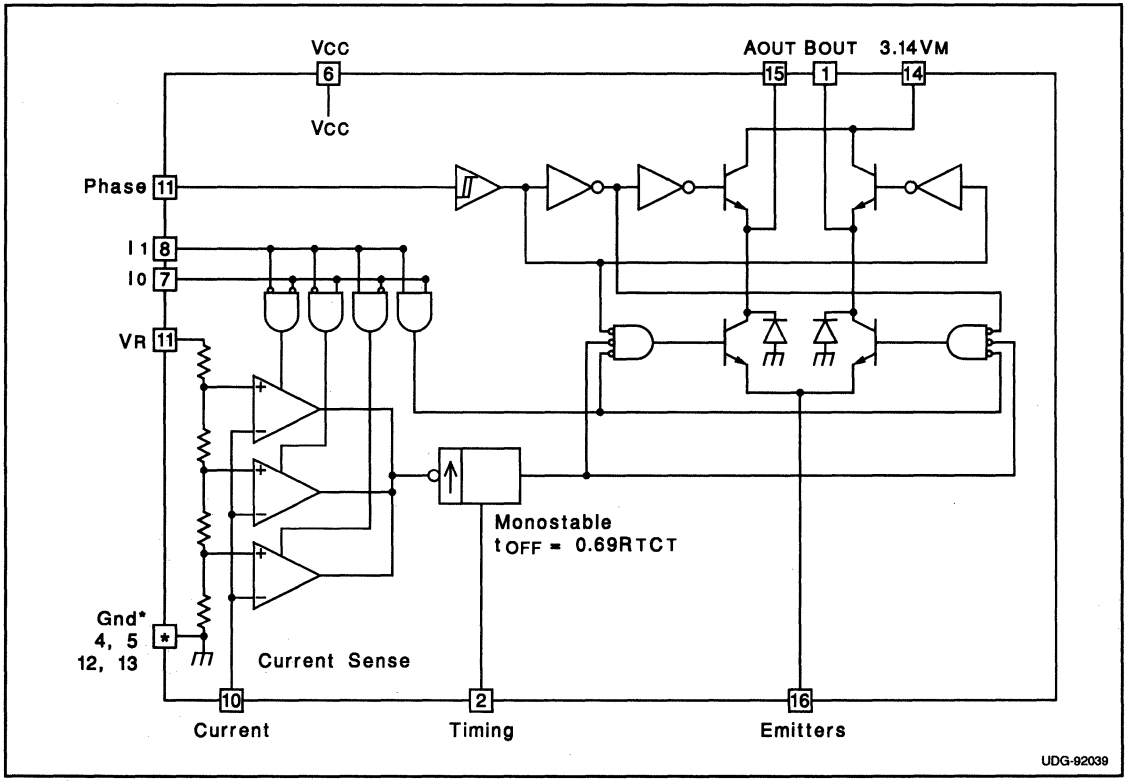
DESCRIPTION

The UC3770A and UC3770B are high-performance full bridge drivers that offer higher current and lower saturation voltage than the UC3717 and the UC3770. Included in these devices are LS-TTL compatible logic inputs, current sense, monostable, thermal shutdown, and a power H-bridge output stage. Two UC3770As or UC3770Bs and a few external components form a complete microprocessor-controllable stepper motor power system.

Unlike the UC3717, the UC3770A and the UC3770B require external high-side clamp diodes. The UC3770A and UC3770B are identical in all regards except for the current sense thresholds. Thresholds for the UC3770A are identical to those of the older UC3717 permitting drop-in replacement in applications where high-side diodes are not required. Thresholds for the UC3770B are tailored for half stepping applications where 50%, 71%, and 100% current levels are desirable.

The UC3770A and UC3770B are specified for operation from 0°C to 70°C ambient.

BLOCK DIAGRAM



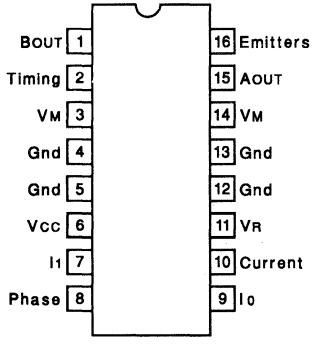
ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage, Vcc 7V
Output Supply Voltage, VMM 50V
Logic Input Voltage (Pins 7, 8, 9) 6V
Analog Input Voltage (Pin 10) Vcc
Reference Input Voltage (Pin 11) 15V
Logic Input Current (Pins 7, 8, 9) ..... -10mA
Analog Input Current (Pins 10, 11) ..... -10mA
Output Current (Pins 1, 15) ..... ± 2A
Junction Temperature, TJ ..... +150°C

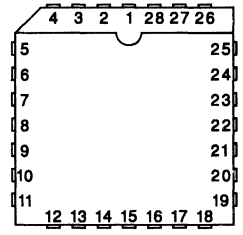
Note 1: All voltages are with respect to Gnd (DIL Pins 4, 5, 12, 13); all currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-28 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1-3
VM	4
N/C	5
AOUT	6
N/C	7
Emitters	8
Gnd	9
BOUT	10
Timing	11
VM	12
Gnd	13-17
Vcc	18
I1	19
Phase	20
Io	21
N/C	22
Current	23
VR	24
N/C	25-27
Gnd	28

ELECTRICAL CHARACTERISTICS:

(All tests apply with VM = 36V, Vcc = 5V, VR = 5V, No Load, and 0°C<TA<70°C, unless otherwise stated, TA = TJ.)

		UC3770A			UC3770B			
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Voltage VM (Pins 3, 14)		10		45	10		45	V
Logic Supply Voltage Vcc (Pin 6)		4.75	5	5.3	4.75	5	5.3	V
Logic Supply Current Icc (Pin 6)	Io = I1 = H, IM = 0		15	25		15	25	mA
	Io = I1 = L, IM = 0		18	28		18	28	mA
	Io = I1 = H, IM = 1.3A		33	40		33	40	mA
Thermal Shutdown Temperature			+170			+170		°C
Logic Threshold (Pins 7, 8, 9)		0.8		2.0	0.8		2.0	V
Input Current Low (Pin 8)	VI = 0.4V			-100			-100	µA
Input Current Low (Pins 7, 9)	VI = 0.4V			-400			-400	µA
Input Current High (Pins 7, 8, 9)	VI = 2.4V			10			10	µA
Comparator Threshold (Pin 10)	VR = 5V, Io = L, I1 = L	400	415	430	400	415	430	mV
	VR = 5V, Io = H, I1 = L	240	255	265	290	300	315	mV
	VR = 5V, Io = L, I1 = H	70	80	90	195	210	225	mV
Comparator Input Current (Pin 10)				±20			±20	µA
Off Time	RT = 56k, CT = 820pF	25	30	35	25	30	35	ms

ELECTRICAL CHARACTERISTICS (cont.):

(All tests apply with V_M = 36V, V_{CC} = 5V, V_R = 5V, No Load, and 0°C<T_A<70°C, unless otherwise stated, T_A = T_J.)

		UC3770A			UC3770B			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Turn Off Delay				2			2	ms
Sink Driver Saturation Voltage	I_M = 1.0A			0.8			0.8	V
	I_M = 1.3A			1.3			1.3	V
Source Driver Saturation Voltage	I_M = 1.0A			1.3			1.3	V
	I_M = 1.3A			1.6			1.6	V
Output Leakage Current	V_M = 45V			100			100	µA

Figure 1: Typical Source Saturation Voltages vs. Load Current

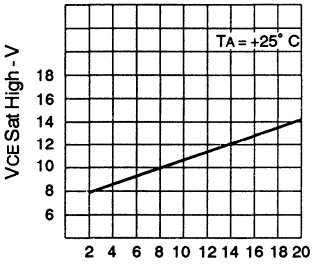


Figure 2: Typical Sink Saturation Voltages vs. Load Current

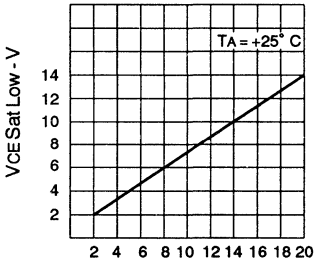
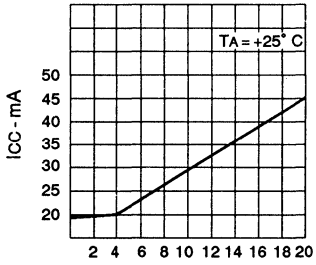


Figure 3: Typical Supply Current vs. Load Current



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Indicates Application Note Available
See Section 9.

7

Power Driver & Interface Circuits


INTEGRATED
CIRCUITS
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Product Selection Guide

POWER DRIVERS, SWITCHES AND INTERFACE CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC195/295/395	Smart Power Switch	These devices act as high gain power transistors and have on-chip, current limiting, power limiting, and thermal overload protection. • Greater than 1.0A Output • 3.0μA Typical Base Current (Adjustable) • 500ns Switching Time • 2.0V Saturation Voltage • Directly Interfaces with CMOS or TTL • Internal Thermal Limiting	TO-220
UC1728/3728	PWM Dual Driver	Load Control and Status monitoring for two inductive loads up to 1A each. • PWM Current Control • Dual Floating Switches • Supply Voltage up to 60V • Tri-State Status Outputs • Low Saturation Voltage	28 Pin DIL 28 PLCC
UC2950	Half-Bridge Bipolar Switch	• Source or Sink 4.0A • Supply Voltage to 35V • High-Current Output Diodes • Tri-State Operation • TTL and CMOS Input Compatability • Thermal Shutdown Protection • 300KHz Operation	5 Pin TO-220
UC1657/3657*	Triple Half-Bridge Power Driver	• Three 2A Drivers • On Board Clamp Diodes	24 Pin Power DIL
UC1720/3720*	Smart Switch	Independent high and low side switching, up to 2.5A capability • Full Protection • Over- and Under-Current Fault Indication • 50V Operation	24 Pin Power DIL
UC1722/3722*	Five Channel Programmable Current Switch	• Five Current-Sinking Switches • Programmable Currents from.5 to 2.5A • Internal Current Sensing • 40V Operation • Protection Features	24 Pin Power DIL
UC3724 UC3725 (Pair)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600KHz Carrier Capability • Local Current Limiting Feature	8 Pin DIL (Pair)
UC3726 UC3727 (Pair)	IGBT Driver Primary Side IGBT Driver Secondary Side	• Transmits to UC3727 • Able to Pass D.C. Information • Transmits Logic Signal Instantly • Receives Power and Signal Across Simple Pulse Transformer • +15V, -5V Gate Drive Voltage • 4Amp (PK) Output Current • De-Sat Detect with Programmable Fault Response	16 Pin DIL 28 Pin PLCC

* Consult Factory for Commercial 15 Pin Power Tab Package

Product Selection Guide

POWER DRIVERS, SWITCHES & INTERFACE CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC5170C	Octal Single Ended Line Driver	Suited for Data Transmission Systems • Eight Drivers in One Package • Meets EIA Standards • Single External Resistor Controls Slew Rate • Tri-State Outputs • Low Power Consumption • TTL Compatible	28 Pin DIL 28 PLCC
UC5171	Octal Single Ended Line Driver	• Single TTL Mode Select • Eight Drivers in One Package • Single External Resistor Controls Slew Rate • Tri-State Outputs	28-Pin DIL 28 PLCC
UC5172	Advanced Octal Single Ended Line Driver	Suited for Data Transmission Systems • Eight Drivers in One Package • Operates in EIA-423 Mode • Can Operate from Supplies up to ±15V • Can Withstand EDS of up to 40V (up to 1mS)	28 Pin DIL 28 Pin PLCC
UC5180C	Octal Line Receiver	Suited for Digital Communication Requirements • Eight Receivers in One Package • Meets EIA Standards • Single 5V Supply • Differential Inputs Withstand ± 25V • Low Noise Filter	28 Pin DIL 28 PLCC
UC5661	Ethernet Coaxial Impedance Monitor	• Detects Cable Impedance Errors • Detects Cable Termination Errors • Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT. • Preset and Adjustable Data Thresholds • Protects DTE from Spurious Data • Prevents Erroneous Transmission Through Repeaters • Acts as a FAST Receiver Squelch, even with RX Data Transformers as Small as 16μH. • Low Skew	8 Pin DIL

Product Selection Guide

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220 Power SO-IC
UC1706/3706	Dual High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion (1706 Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible	16 Pin DIL "Batwing"
UC1707/3707	Dual Uncommitted High Current MOSFET Compatible Output Driver	• Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	SMD Power SO-IC
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25nSec Rise and Fall Times • 25 nSec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8 Pin DIL 16 Pin DIL SMD Power SO-IC
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8 Pin DIL SMD Power SO-IC
UC1710/3710	High Current/Speed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8 Pin DIL 5 Pin TO-220 Power SO-IC
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 15nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8 Pin DIL SMD Power SO-IC

Product Selection Guide

SCSI BUS BOSS™ ACTIVE TERMINATORS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC5601	18 Line SCSI-2 Active Terminator	• Trimmed Regulator for Accurate Terminated Current • Logic Command Disconnects All Terminating Resistors • Provides Active Termination for 18 Lines • Negative Clamping On All Signal Lines • Low Supply Current in Disconnect Mode • Low Dropout Voltage Regulator • Low Thermal Resistance SMD Packages	28 Pin Pwr. PLCC 28 Pin Pwr. SO-IC
UC5602	18 Line SCSI-2 Active Terminator	• Provides Active Termination for 18 Lines • Engineered for High Volume Applications • 6% Trimmed Max. Termination Current • 6% Termination Impedance • Low Dropout Voltage Regulator	28 Pin Pwr. PLCC 28 Pin Pwr. SO-IC
UC5603	9 Line SCSI-2 Active Terminator	• Two New Power SMD Packages for 1.8 in. HDD or Cable Applications • Provides Active Termination for 9 Lines • Trimmed to Meet SCSI-3 Specifications • Low Capacitance • 300mA Source/Sink Current • 100μA Supply Current in Disconnect Mode • Negative Clamping on All Signal Lines	16 Pin Pwr. SO-IC 16 Pin Pwr. ZIP

Note: Look for other new SCSI product accouncements. Contact your UICC Representative

Dual Switchmode Solenoid Driver

FEATURES

- High current capability (up to 2.5A per channel)
- High voltage operation (up to 46V for power stage)
- High efficiency switchmode operation
- Regulated output current (adjustable)
- Few external components
- Separate logic supply
- Thermal protection

DESCRIPTION

The L295 is a monolithic integrated circuit in a 15 lead MULTIWATT® package; it incorporates all the functions for direct interfacing between digital circuitry and inductive loads. The L295 is designed to accept standard microprocessor logic levels and drive 2 independent solenoids. The output current is completely controlled by means of a switching technique allowing very efficient operation. Furthermore, it includes an enable input and separate power supply inputs for bilevel operation such as interfacing with peripherals running at higher voltage levels.

The L295 is particularly suitable for applications such as hammer driving in matrix printers, step motor driving and electromagnet controllers.

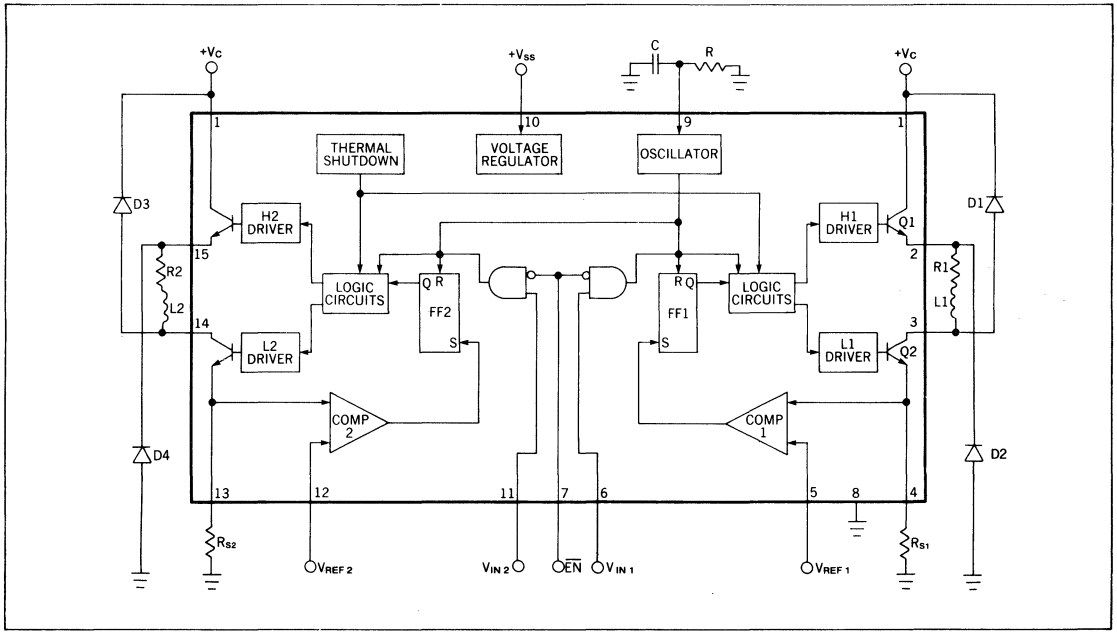
ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_C 50V
Logic Supply Voltage, V_{SS} 12V
Enable and Input Voltage, V_{EN}, V_i 7V
Reference Voltage, V_{REF} 7V
Peak Output Current (each channel)
Non-Repetitive, (t = 100μsec), I_o 3A
Repetitive (80% on −20% off; t_{ON} = 10ms) 2.5A
DC Operation 2A
Total Power Dissipation (at T_{case} = 75°C) 25W
Storage and Junction Temperature ..... −40 to +150°C

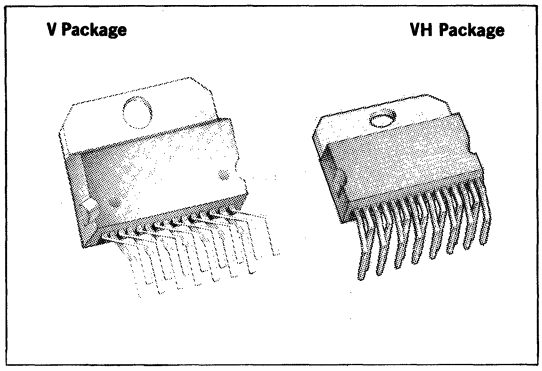
THERMAL DATA

Thermal Resistance Junction-Case, θ_{JC} ..... 3°C/W max
Thermal Resistance Junction-Ambient, θ_{JA} ..... 35°C/W max

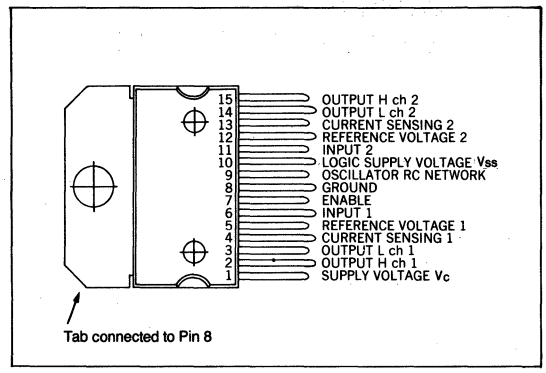
BLOCK DIAGRAM



MECHANICAL DATA



CONNECTION DIAGRAM (TOP VIEW)

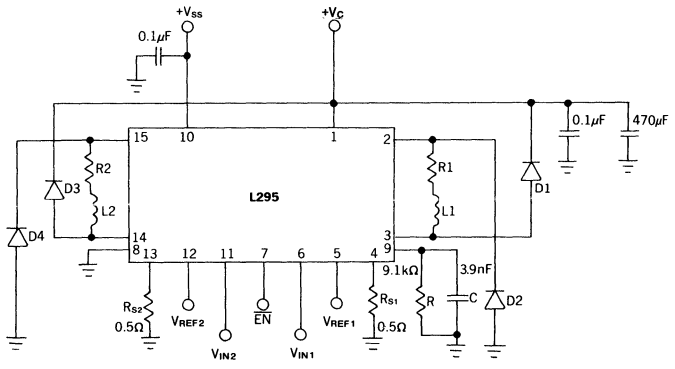


ELECTRICAL CHARACTERISTICS (Refer to the application circuit, V_{SS} = 5V, V_C = 36V, T_j = 25°C; unless otherwise specified, L = Low; H = High) $T_A = T_J$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_C		12		46	V
Logic Supply Voltage	V_{SS}		4.75		10	V
Quiescent Drain Current (from V_C)	I_C	V_C = 46V; V_{i1} = V_{i2} = V_{EN} = L			4	mA
Quiescent Drain Current (from V_{SS})	I_{SS}	V_{SS} = 10V			46	mA
Low Input Voltage	$V_{i1}L$, $V_{i2}L$		-0.3		0.8	V
High Input Voltage	$V_{i1}H$, $V_{i2}H$		2.2		7	V
Low Enable Input Voltage	$V_{EN}L$		-0.3		0.8	V
High Enable Input Voltage	$V_{EN}H$		2.2		7	V
Input Current	I_{i1}, I_{i2}	V_{i1} = V_{i2} = L			-100	μA
		V_{i1} = V_{i2} = H			10	
Enable Input Current	I_{EN}	V_{EN} = L			-100	μA
		V_{EN} = H			10	
Input Reference Voltage	V_{REF1}, V_{REF2}		0.2		2	V
Input Reference Current	I_{REF1}, I_{REF2}				-5	μA
Oscillation Frequency	f_{osc}	C = 3.9nF, R = 9.1KΩ		25		KHz
Transconductance (each channel)	$\frac{I_p}{V_{REF}}$	V_{REF} = 1V, R_s = 0.5Ω	1.9	2	2.1	A/V
Total Output Voltage Saturation (each channel)*	V_{sat}	I_o = 2A		2.8	3.6	V
External Sensing Resistors Voltage Drop	$V_{sens\ 1}$, $V_{sens\ 2}$				2	V

*$V_{sat} = V_{CEsatQ1} + V_{CEsatQ2}$.

APPLICATION CIRCUIT



D1, D4 = 2A HIGH SPEED DIODES (SES5001, or equivalent)

FUNCTIONAL DESCRIPTION

The L295 incorporates two independent driver channels with separate inputs and outputs, each capable of driving an inductive load (see block diagram).

The device is controlled by three microprocessor compatible digital inputs and two analog inputs. These inputs are;

$\overline{EN}$ chip enable (digital input, active low), enables both channels when in the low state.

V_{IN1},
V_{IN2} channel inputs (digital inputs, active high), enable each channel independently. A channel is activated when both $\overline{EN}$ and the appropriate channel input are active.

V_{REF1},
V_{REF2} reference voltages (analog inputs), used to program the peak load currents. Peak load current is proportional to V_{REF}.

Since the two channels are identical, only channel one will be described. The following description applies equally to channel two, replacing FF2 for FF1, V_{REF2} for V_{REF1} etc. When the channel is activated by a low level on the $\overline{EN}$ input and a high level on the channel input V_{IN1}, the output transistors Q1 and Q2 switch on and current flows in the load according to the exponential law:

$$I = \frac{V}{R1}\left(1 - e^{\frac{-R1t}{L1}}\right)$$

where: R1 and L1 are the resistance and inductance of the load and V is the voltage available on the load

The current increases until the voltage on the external sensing resistor, R_{S1}, reaches the reference voltage, V_{REF1}. This peak current, I_{p1}, is given by:

$$I_{p1} = \frac{V_{REF1}}{R_{S1}}$$

At this point the comparator output, Comp 1, sets the RS flip-flop, FF1, that turns off the output transistor, Q1. The load current flowing through D2, Q2, R_{S1}, decreases according to the law:

$$I = \left(\frac{V_A}{R1} + I_{P1}\right)e^{\frac{-R1\,t}{L1}} - \frac{V_A}{R1}$$

where: $V_A = V_{CEsat\ Q2} + V_{sense\ 1} + V_{D2}$

If the oscillator pin (9) is connected to ground the load current falls to zero as shown in Figure 1.

At time t_2, channel 1 is disabled by taking the inputs V_{IN1} low and/or $\overline{EN}$ high, and the output transistor Q2 is turned off. The load current flows through D2 and D1 according to the law:

$$I = \left(\frac{V_B}{R1} + I_{T2}\right)e^{\frac{-R1t}{L1}} - \frac{V_B}{R1}$$

where: $V_B = V_C + V_{D1} + V_{D2}$
I_{T2} = current value at the time t_2.

Figure 2 shows the current waveform obtained with an RC network connected between pin 9 and ground. From t_0 to t_1 the current increases as in Figure 1. A difference exists at the time t_2 because the current starts to increase again. At this time a pulse is produced by the oscillator circuit that resets the flip flop, FF1, and switches on the output transistor, Q1. The current increases until the drop on the sensing resistor R_{S1} is equal to V_{REF1} (t_3) and the cycle repeats.

The switching frequency depends on the values of R and C, as shown in Figure 4 and must be chosen in the range 10 to 30KHz.

It is possible with external hardware to change the reference voltage V_{REF} in order to obtain a high peak current I_p and a lower holding current I_h (see Figure 3).

The L295 is provided with a thermal protection that switches off all the output transistors when the junction temperature exceeds 150°C. The presence of a hysteresis circuit makes the IC work again after a fall of the junction temperature of about 20°C.

The analog input pins (V_{REF1}, V_{REF2}) can be left open or connected to V_{ss}; in this case the circuit works with an internal reference voltage of about 2.5V and the peak current in the load is fixed only by the value of R_s:

$$I_p = \frac{2.5}{R_s}$$

SIGNAL WAVEFORMS

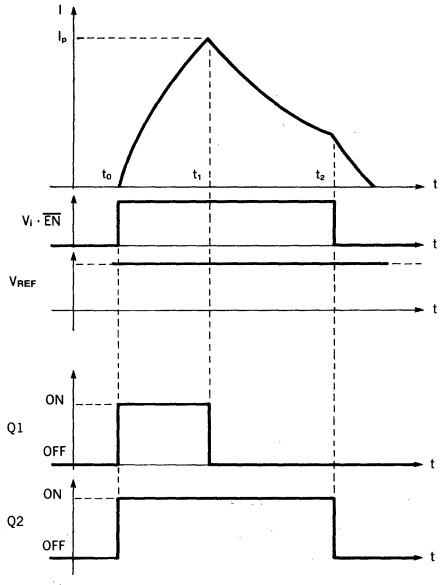


Figure 1. Load current waveform with pin 9 connected to GND

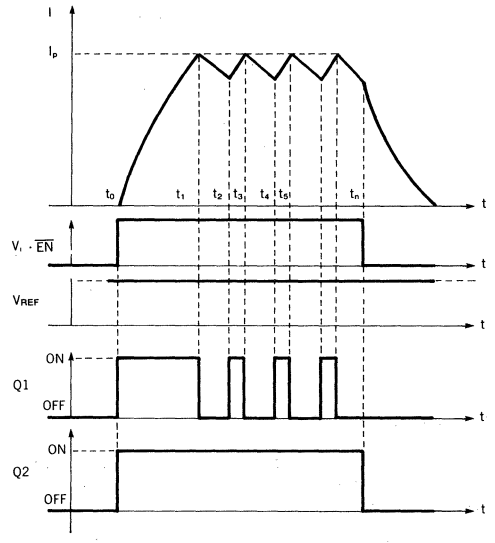


Figure 2. Load current waveform with external R-C network connected between pin 9 and ground

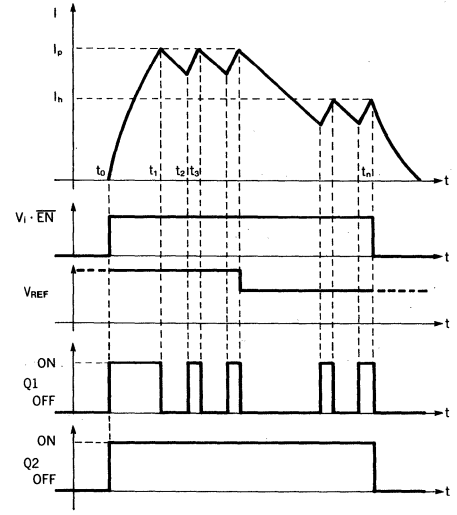


Figure 3. With V_{REF} changed by hardware

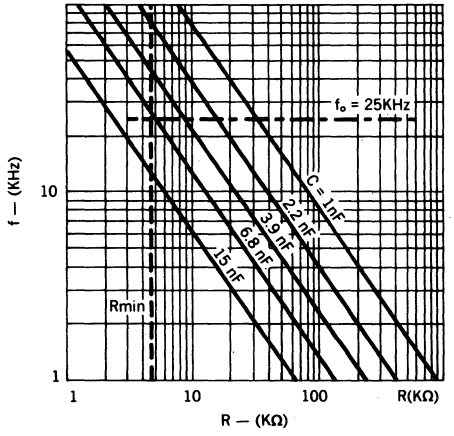


Figure 4. Switching frequency vs values of R and C

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INTEGRATED CIRCUITS
UNITRODE

UC1705
UC2705
UC3705

High Speed Power Driver

FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both Vs and Vc can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

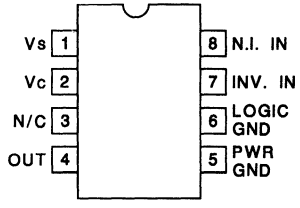
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

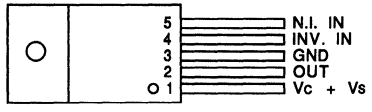
OUT = $\overline{\text{INV}}$ and N.I.
OUT = INV or $\overline{\text{N.I.}}$

CONNECTION DIAGRAMS

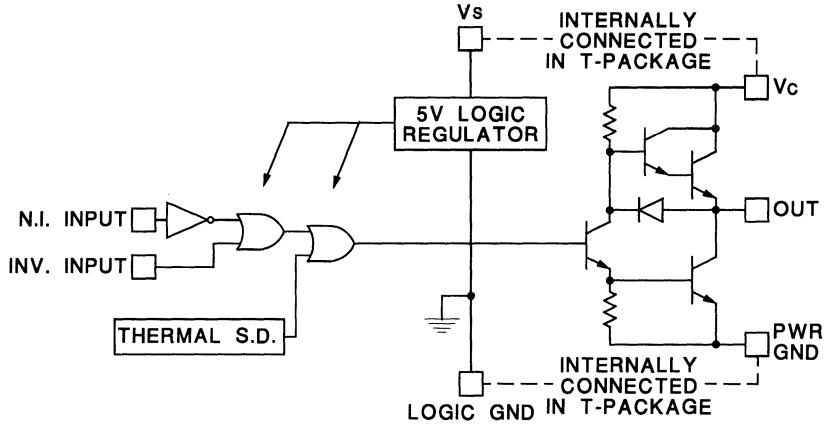
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N or J Package, D Package



5-PIN TO-220
(TOP VIEW)
T Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, Vc	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20µJ	15µJ	50µJ
Digital Inputs (See Note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C (See Note)	1W	1W	3W
Power Dissipation at T_A (Leads/Case) = 25°C (See Note)	3W	2W	25W
Operating Temperature Range	0°C to +70°C	-55°C to +125°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA
Consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1705, -25°C to +85°C for the UC2705, and 0°C to +70°C for the UC3705; Vs = Vc = 20V, T_A = T_J.

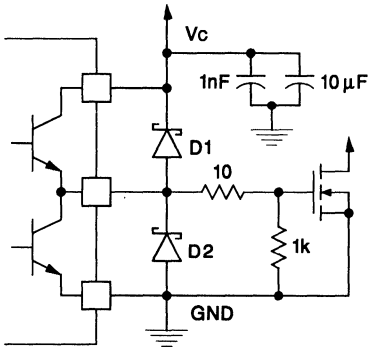
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Vs Supply Current	Vs = 40V, (Outputs High, T Pkg)		6	8	mA
	Vs = 40V, (Outputs Low, T Pkg)		8	12	mA
Vc Supply Current (N, J Only)	Vc = 40V, Outputs Low		2	4	mA
Vc Leakage Current (N, J Only)	Vs = 0, Vc = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.5	0.1	mA
Output High Sat., Vc-Vo	Io = -50mA			2.0	V
	Io = -500mA			2.5	V
Output Low Sat., Vo	Io = 50mA			0.4	V
	Io = 500mA			2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: Vs = Vc = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
Vc Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns

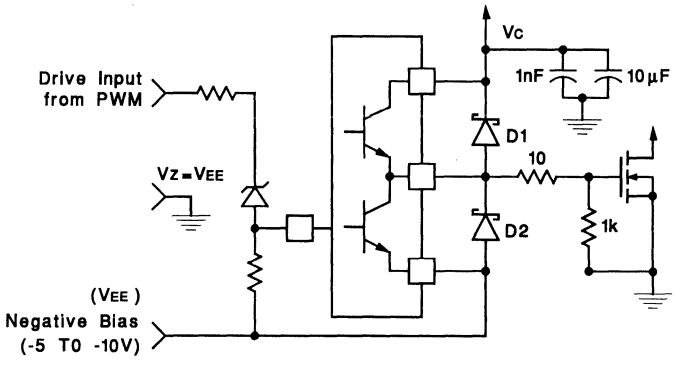
APPLICATIONS

Power MOSFET Drive Circuit



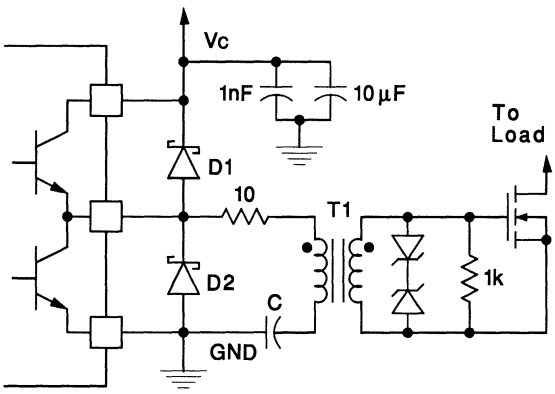
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



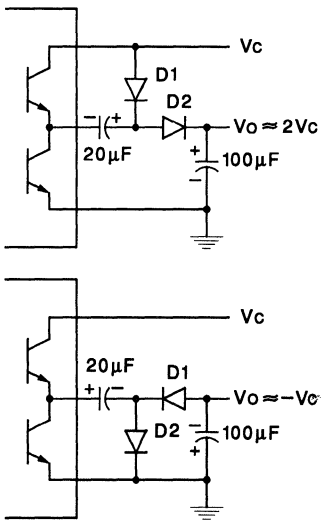
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



7

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INTEGRATED CIRCUITS
UNITRODE

UC1706
UC2706
UC3706

Dual Output Driver

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below.

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

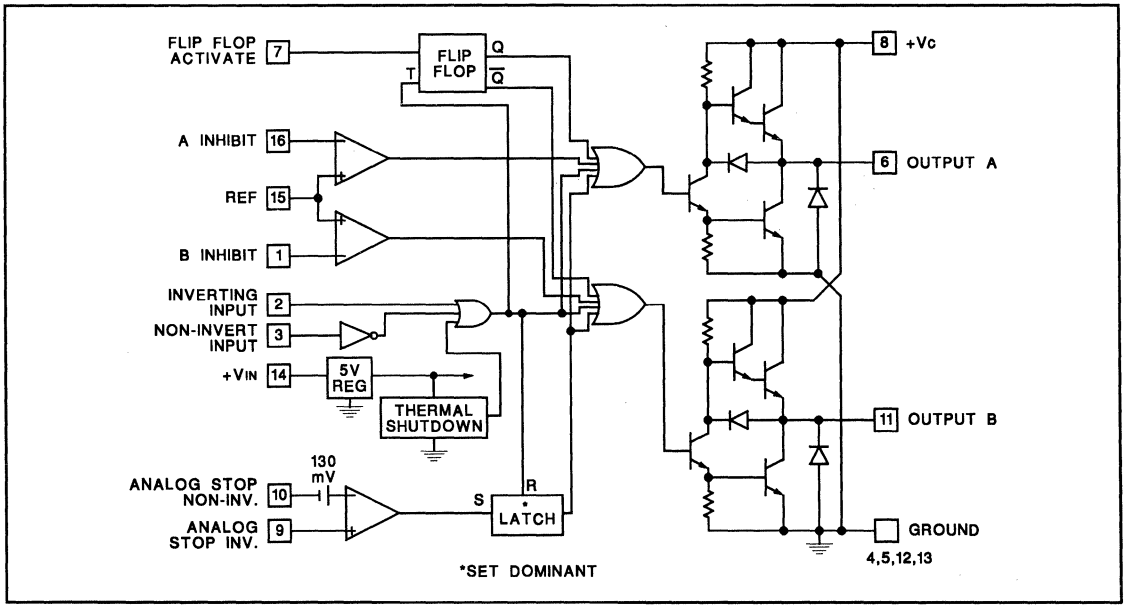
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

OUT = INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



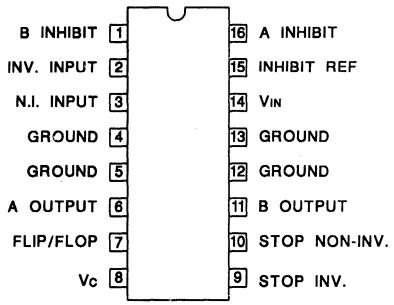
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, Vc	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

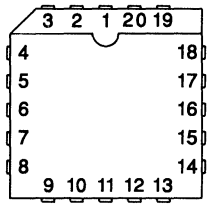
CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
B INHIBIT	2
INV INPUT	3
N.I. INPUT	4
GROUND	5
A OUTPUT	6
FLIP/FLOP	7
Vc	8
N/C	9
STOP INV.	10
STOP NON-INV.	11
B OUTPUT	12
GROUND	13
N/C	14
GROUND	15
N/C	16
GROUND	17
V_{IN}	18
INHIBIT REF	19
A INHIBIT	20

7

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1706, -25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = Vc = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
Vc Supply Current	Vc = 40V, Outputs Low		4	5	mA
Vc Leakage Current	V_{IN} = 0, Vc = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., Vc-Vo	Io = -50mA			2.0	V
	Io = -500mA			2.5	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1706, -25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Sat., Vo	Io = 50mA			0.4	V
	Io = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		-10	-20	µA
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	µA
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N. I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
Vc Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V, Inhibit Inv. = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V, Stop Inv. = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common Vc pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at last 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs--the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} - 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

CIRCUIT DESCRIPTION (cont.)

Supply Voltage

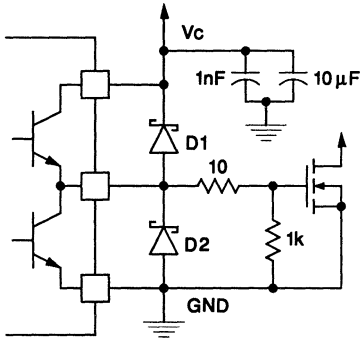
With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When VIN is low, the entire circuit is disabled and no current is drawn from Vc. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply VIN to the UC1706. VIN switching should be fast as if Vc is high, undefined operation of the outputs may occur with VIN less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

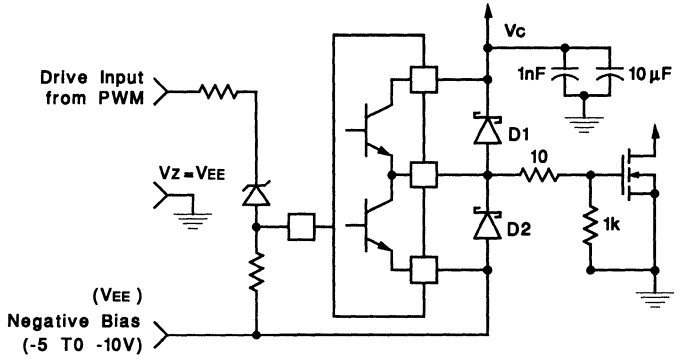
APPLICATIONS

Power MOSFET Drive Circuit



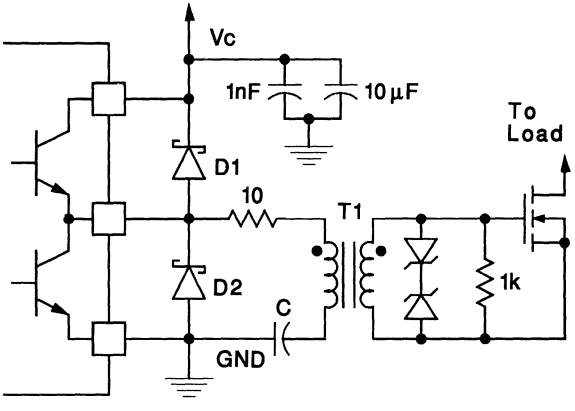
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



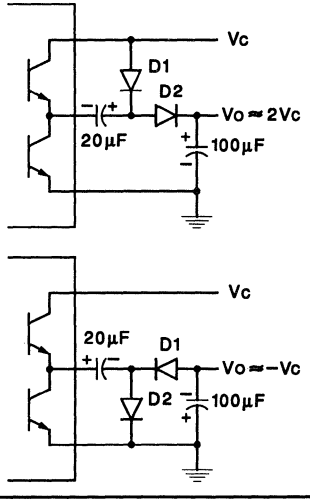
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



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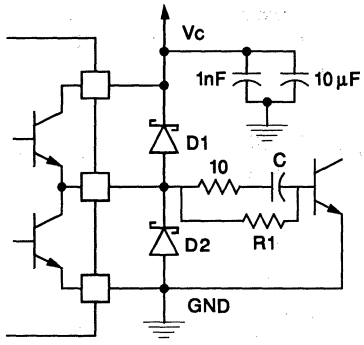
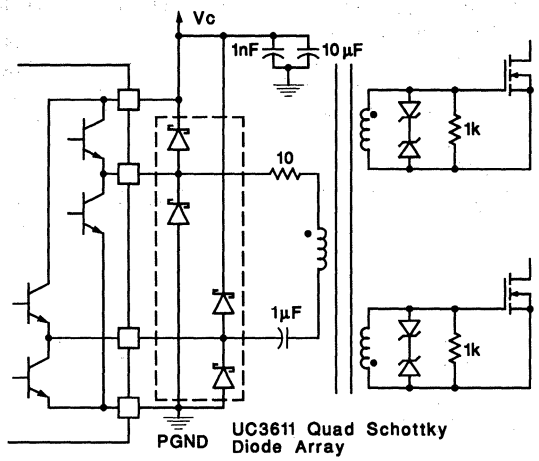
APPLICATIONS (cont'd)

Power Bipolar Drive Circuit



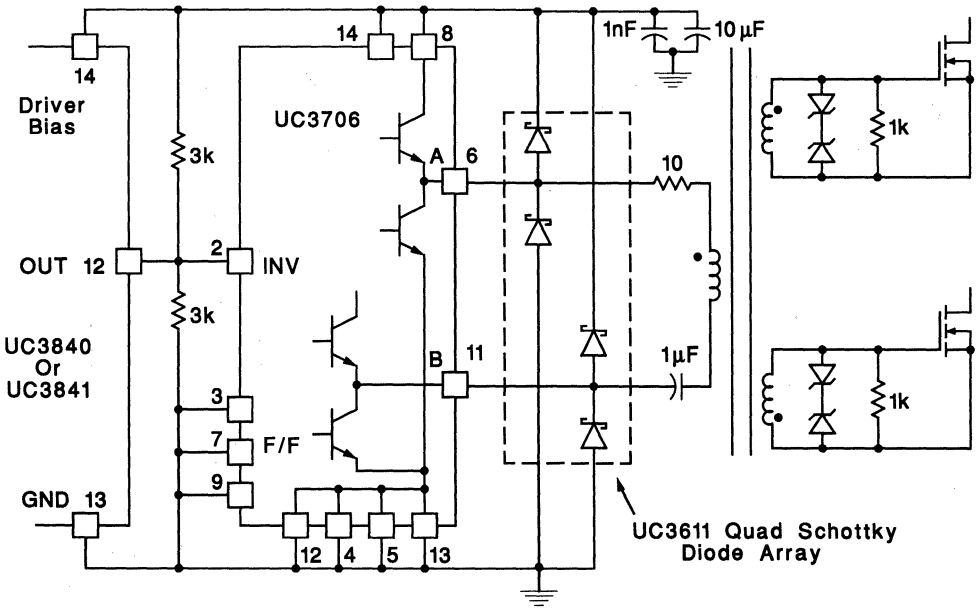
D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration



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INTEGRATED CIRCUITS
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Dual Channel Power Driver

UC1707
UC2707
UC3707

FEATURES

- Two Independent Drivers
- 1.5A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40ns Rise and Fall into 1000pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown with Optional Latch
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and Vc can independently range from 5V to 40V.

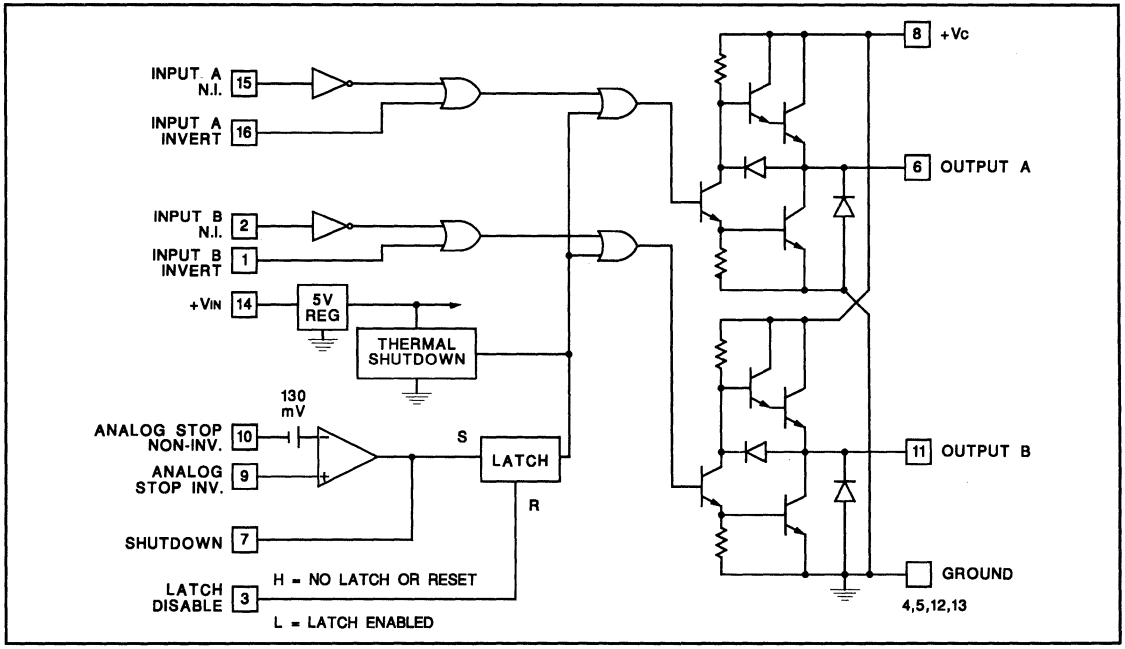
These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

TRUTH TABLE (Each Channel)

INV.	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{INV}$ and N.I.
OUT = INV or $\overline{N.I.}$

BLOCK DIAGRAM



5/93

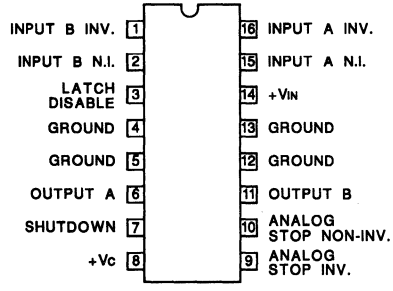
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, Vc	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs (See Note)	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.
Consult Packaging section of Databook for thermal limitations and considerations of package.

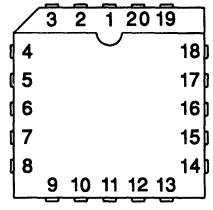
CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INPUT B INV.	2
INPUT B N.I.	3
LATCH DISABLE	4
GROUND	5
N/C	6
GROUND	7
OUTPUT A	8
SHUTDOWN	9
Vc	10
N/C	11
ANALOG STOP INV.	12
ANALOG STOP NON INV.	13
OUTPUT B	14
GROUND	15
N/C	16
GROUND	17
V_{IN}	18
INPUT A NON INV.	19
INPUT A INV.	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707, -25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = Vc = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		12	15	mA
Vc Supply Current	Vc = 40V, Outputs Low		5.2	7.5	mA
Vc Leakage Current	V_{IN} = 0, Vc = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., Vc-Vo	Io = -50mA			2.0	V
	Io = -500mA			2.5	V

ELECTRICAL CHARACTERISTICS (cont.):

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707, -25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Sat., Vo	Io = 50mA			0.4	V
	Io = 500mA			2.5	V
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	µA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

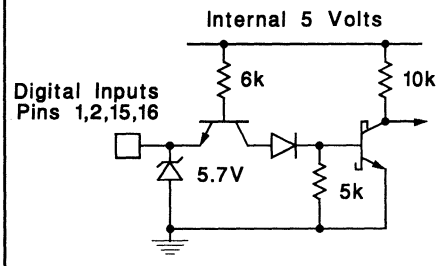
TYPICAL SWITCHING CHARACTERISTICS:

V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		40	50	60	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		30	40	50	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		30	40	50	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		45	55	65	ns
90% to 10% Fall		25	40	50	ns
Vc Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V Stop Inv. = 0 to 0.5V	180			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

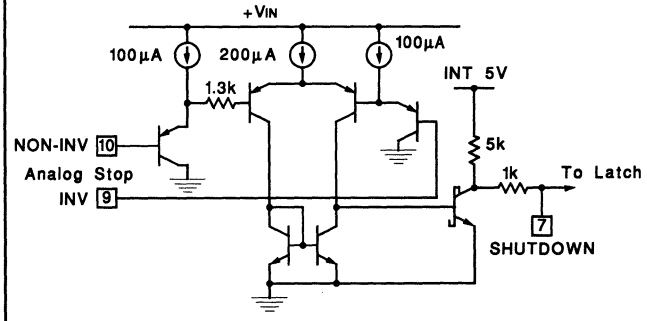
SIMPLIFIED INTERNAL CIRCUITRY

Typical Digital Input Gate



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

Analog Shutdown Comparator Circuit

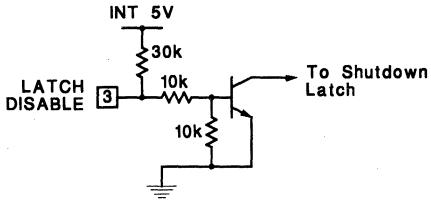


The input common-mode voltage range is from ground to (V_{IN}-3V). When not used both inputs should be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

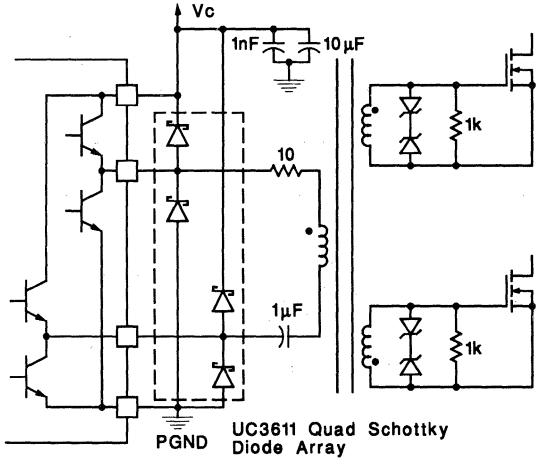
SIMPLIFIED INTERNAL CIRCUITRY (continued)

Latch Disable

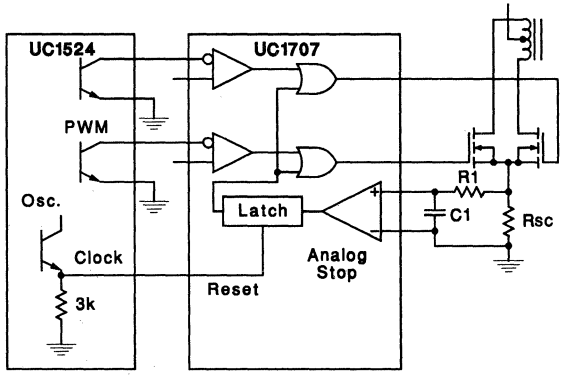
The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the V_{IN} supply or by momentarily (>200ns) raising pin 3 high.



Transformer Coupled Push-pull MOSFET Drive Circuit



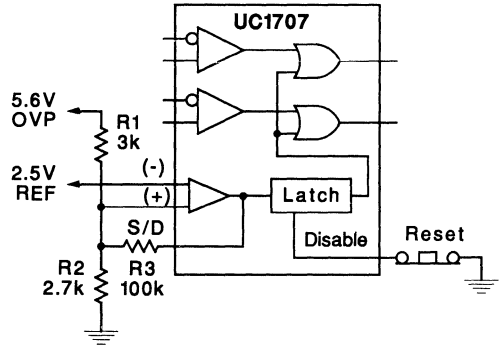
Current Limiting



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R1C1 is used to filter leading edge spikes.

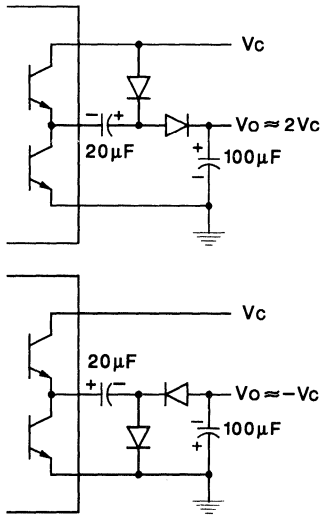
APPLICATIONS (continued)

Over-Voltage Protection



With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.

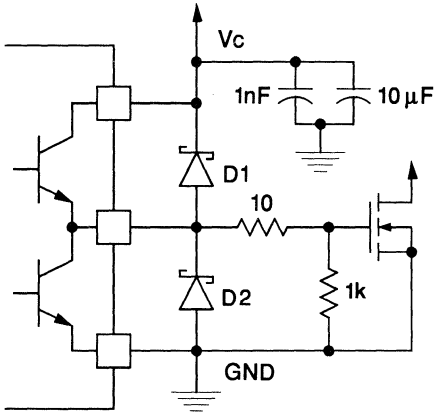
Charge Pump Circuits



When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

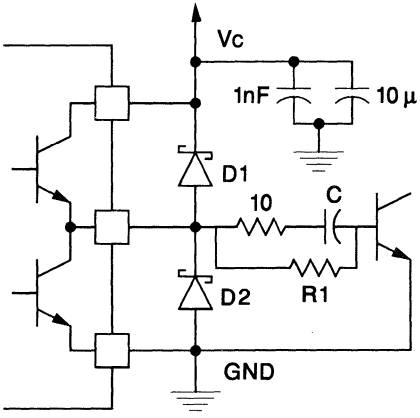
OUTPUT STAGE COUPLING

Power MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Power Bipolar Drive Circuit

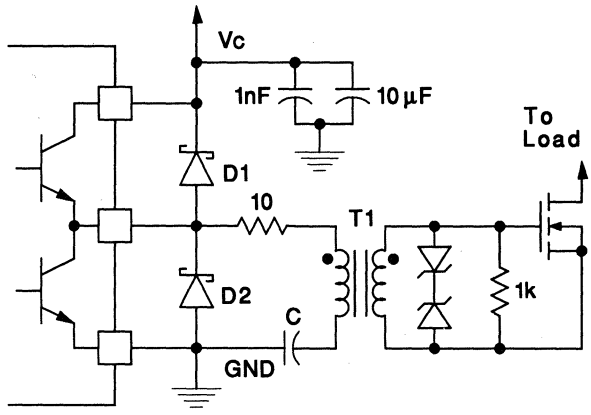


D1, D2: UC3611 Schottky Diodes

7

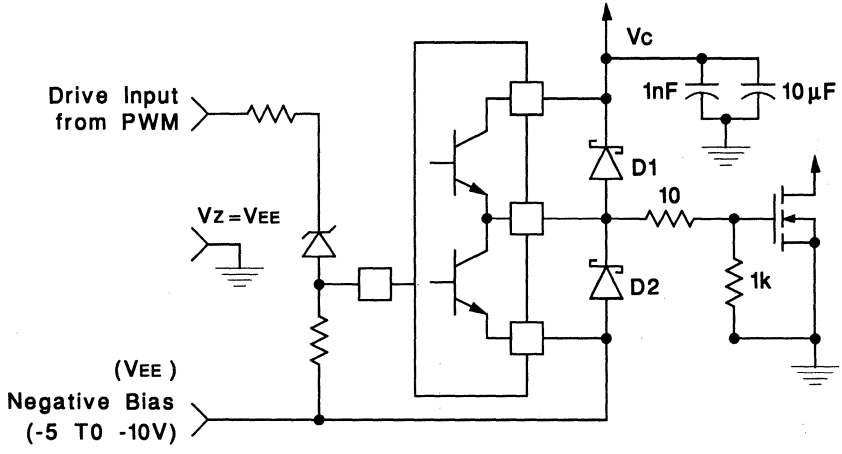
TRANSFORMER COUPLING

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottly Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Reference PWM



D1, D2: UC3611 Schottky Diodes

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INTEGRATED CIRCUITS
UNITRODE

Dual Non-Inverting Power Driver

UC1708
UC3708

FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25ns Rise and Fall Times
- 25ns Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

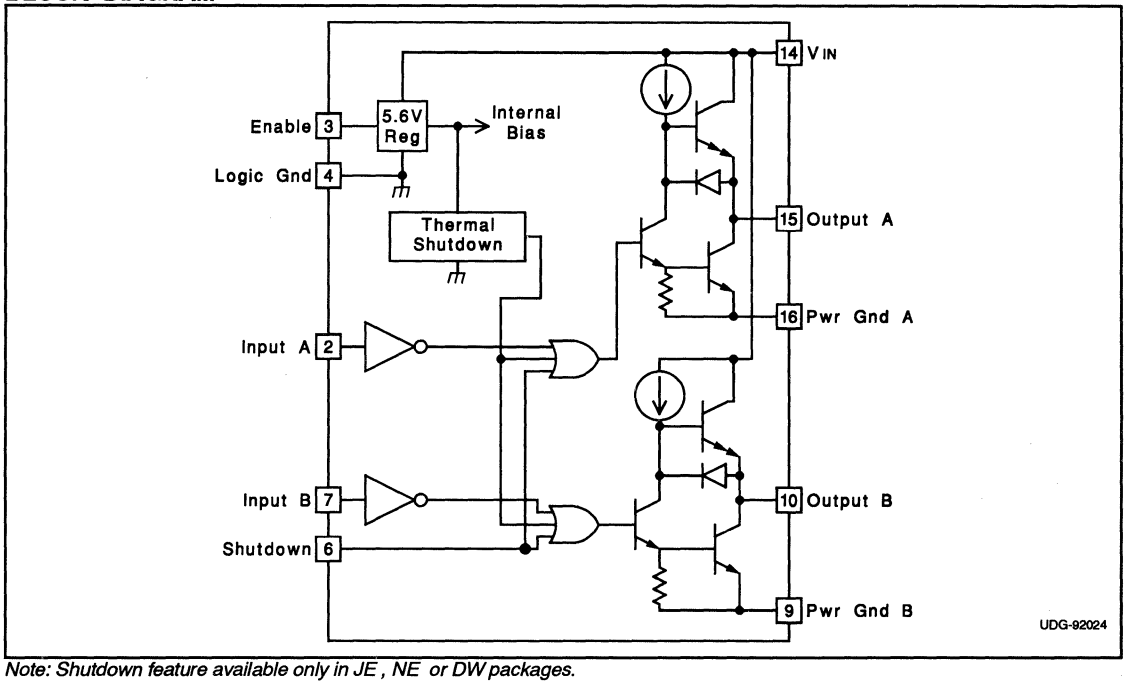
DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 to 35 volt supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as V_{IN}. Each output can source or sink up to 3A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

These devices are available in plastic 8-pin MINIDIP and 16-pin "bat-wing" DIP packages for operation over a 0°C to +70°C temperature range. For operation over a -55°C to +125°C temperature range, the device is available in hermetically sealed 8-pin MINIDIP and 16 pin DIP packages. Surface mount devices are also available.

BLOCK DIAGRAM



Note: Shutdown feature available only in JE, NE or DW packages.

12/92

7

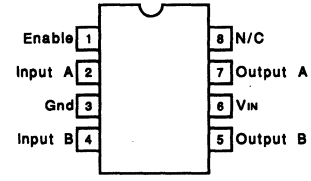
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{IN} 35V
Output Current (Each Output, Source or Sink)
  Steady-State 0.5A
  Peak Transient 3A
Ouput Voltage ..... -0.3 to (V_{IN} + 0.3)V
Enable and Shutdown Inputs ..... -0.3 to 6.2V
A and B Inputs ..... -0.3 to (V_{IN} + 0.3)V
Operating Junction Temperature (Note 2) ..... 150°
Storage Temperature Range ..... -65° to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

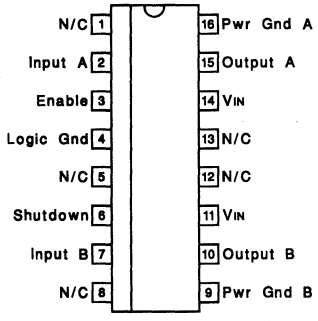
NOTE 1: All voltages are with respect to Logic Gnd pin. All currents are positive into, negative out of, device terminals.
NOTE 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

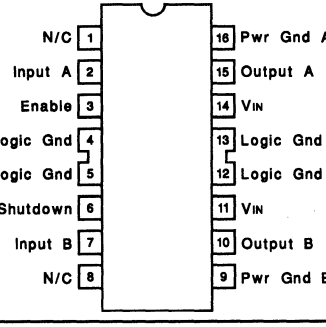
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE or NE Package



Note: In JE package Pin 4 is logic ground. Pins 5, 12, and 13 are N/C.

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, V_{IN}=10V to 35V, and these specifications apply for: –55°C<T_A<125°C for the UC1708 and 0°C<T_A<70°C for the UC3708. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	OutputsLow		18	26	mA
	Outputs High		14	18	mA
	Enable = 0V		1	4	mA
A, B and Shutdown Inputs Low Level				0.8	V
A, B and Shutdown Inputs High Level		2.0			V
A, B Input Current Low	$V_{A,B}$ = 0.4V	-1	-0.6		mA
A, B Input Current High	$V_{A,B}$ = 2.4V	-200		50	µA
A, B Input Leakage Current High	$V_{A,B}$ = 35.3V			200	µA
Shutdown Input Current Low	$V_{SHUTDOWN}$ = 0.4V		20	100	µA
Shutdown Input Current High	$V_{SHUTDOWN}$ = 2.4V		170	500	µA
	$V_{SHUTDOWN}$ = 6.2V		0.6	1.5	mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, V_{IN} = 10V to 35V, and these specifications apply for: $-55^{\circ}C<T_A<125^{\circ}C$ for the UC1708 and $0^{\circ}C<T_A<70^{\circ}C$ for the UC3708. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Input Current Low	V_{ENABLE} = 0V	-600	-460	200	µA
Enable Input Current High	V_{ENABLE} = 6.2V			200	µA
Enable Threshold Rising			2.8	3.6	V
Enable Threshold Falling			2.4	3.4	V
Output High Sat., V_{IN} - V_{OUT}	I_{OUT} = -50mA			2.0	V
	I_{OUT} = -500mA			2.5	V
Output Low Sat., V_{OUT}	I_{OUT} = 50mA			0.4	V
	I_{OUT} = 500mA			2.5	V
Thermal Shutdown			155		°C

SWITCHING CHARACTERISTICS (Figure 1) (V_{IN} = 20V, delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
From A,B Input to Output:					
Rise Time Delay (TPLH)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	40	ns
	CL = 2200pF		30	45	ns
10% to 90% Rise (TTLH)	CL = 0pF		55	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		35	50	ns
90% to 10% Fall (TTHL)	CL = 0pF		15	20	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
From Shutdown Input to Output					
Rise Time Delay (TPLH)	CL = 0pF		25	75	ns
	CL = 1000pF (Note 3)		30	65	ns
	CL = 2200pF		35	70	ns
10% to 90% Rise (TTLH)	CL = 0pf		50	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	45	ns
	CL = 1000pF (Note 3)		30	50	ns
	CL = 2200pF		35	55	ns
90% to 10% Fall (TTHL)	CL = 0pF		25	60	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Total Supply Current	F = 200kHz, 50% duty cycle, both channels; CL = 0pF		23	25	mA
	F = 200kHz, 50% duty cycle, both channels; CL = 2200pF		38	45	mA

NOTE 3: These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.

Figure 1: AC Test Circuit and Switching Time Waveforms

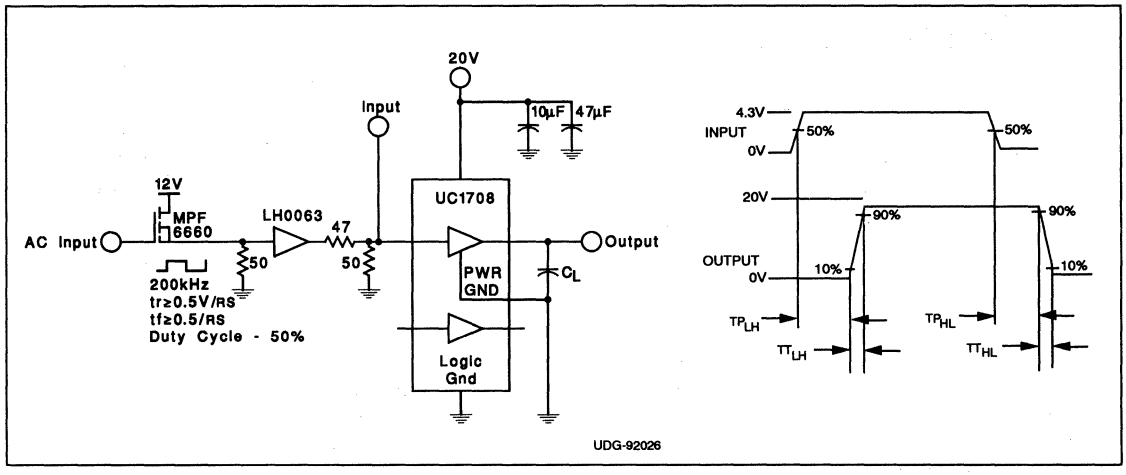
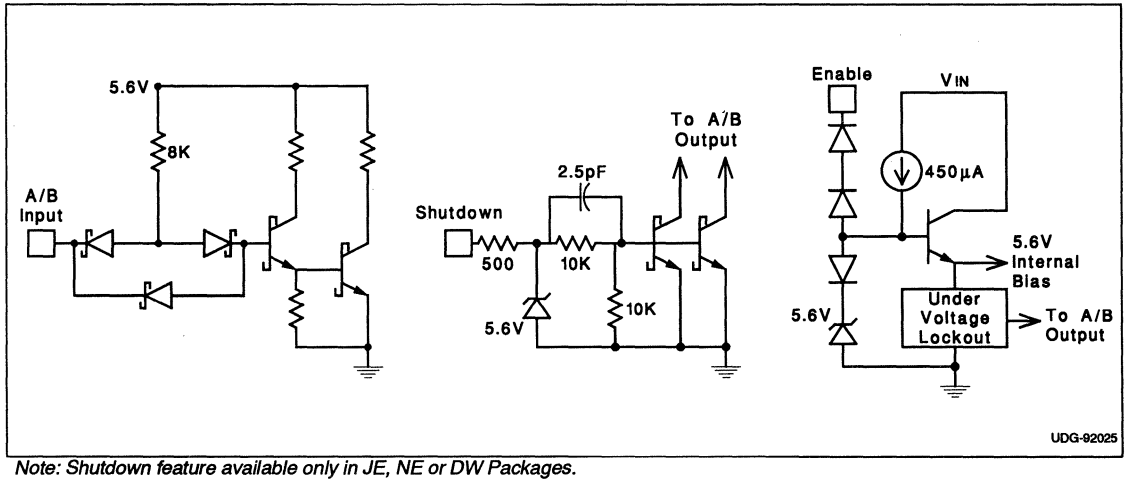


Figure 2: Equivalent Input Circuits



Note: Shutdown feature available only in JE, NE or DW Packages.

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Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection

DESCRIPTION

The UC1709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 amps of either source or sink current from a totem-pole output stage configured for minimal cross-conduction current spike.

The UC1709 (3709) is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

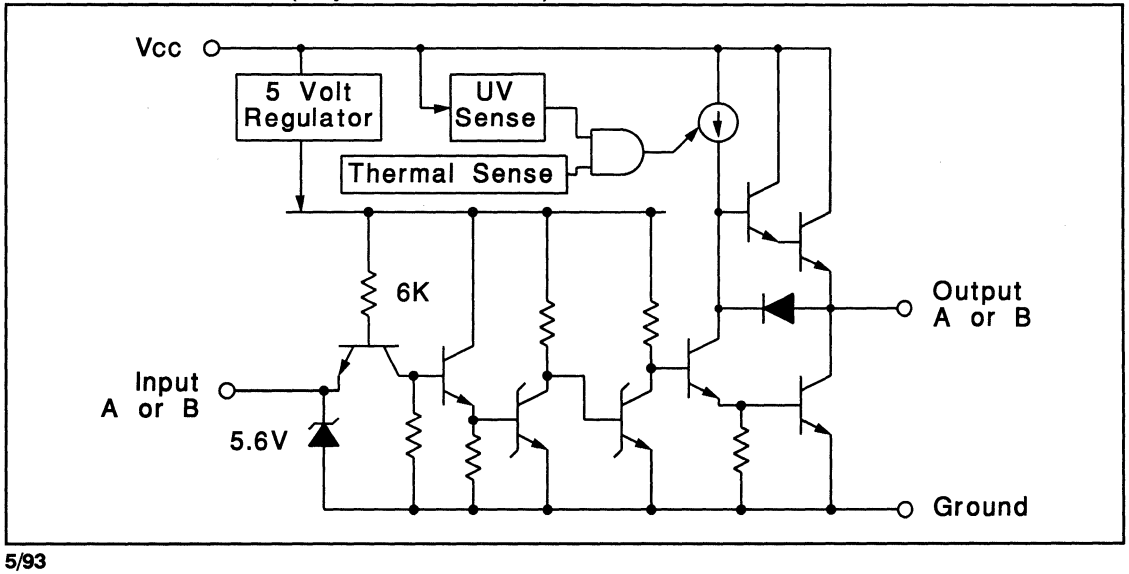
With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30V. This design also includes thermal shutdown protection and an under-voltage lockout circuit.

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40V	40V
Output Current (Source or Sink)		
Steady-State	±500	±500 mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20 µJ	15 µJ
Digital Inputs (See Note)	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W
Power Dissipation at T_C = 25°C	3W	2W
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C	300 °C

Note: All currents are positive into, negative out of the specified terminals. Digital drive can exceed 5.5V if input current is limited to 10mA. Consult Packaging section of Databook for thermal limitations and considerations of package.

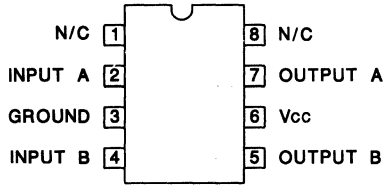
SIMPLIFIED SCHEMATIC (Only One Driver Shown)



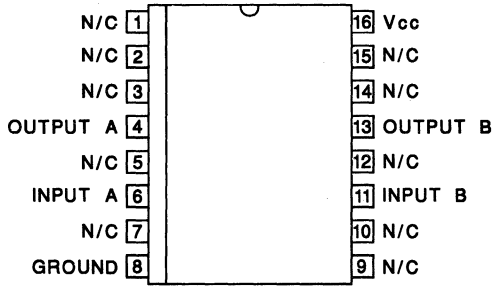
5/93

CONNECTION DIAGRAMS

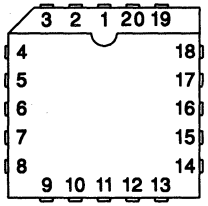
8 PIN DIL (TOP VIEW)
N or J Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
N/C	2
INPUT A	3
N/C	4
N/C	5
GROUND	6
N/C	7
N/C	8
INPUT B	9
N/C	10
N/C	11
OUTPUT B	12
N/C	13
N/C	14
N/C	15
Vcc	16
N/C	17
N/C	18
N/C	19
OUTPUT A	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1709 and 0°C to +70°C for the UC3709; Vcc = 20V, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Both Outputs High		10	12	mA
	Both Outputs Low		7	10	mA
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.05	0.1	mA
Output High Sat., Vcc-Vo	Io = -50mA		1.5	2.0	V
	Io = -500mA		2.0	2.5	V
Output Low Sat., Vo	Io = 50mA		0.1	0.4	V
	Io = 500mA		2.0	2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS:

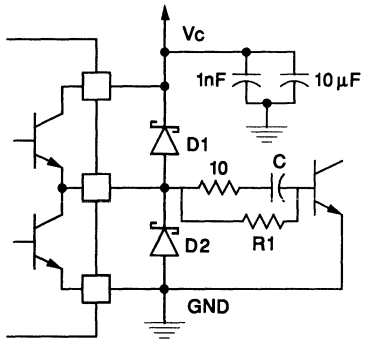
Vcc = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =		UNIT
		0 nF	2.2 nF	
Rise Time Delay		80	80	ns
10% to 90% Rise		20	40	ns
Fall Time Delay		60	80	ns
90% to 10% Fall		20	40	ns
Vcc Cross-Conduction Current Spike Duration	Output Rise	25		ns
	Output Fall	0		ns

Note: Refer to UC1705 specifications for further information

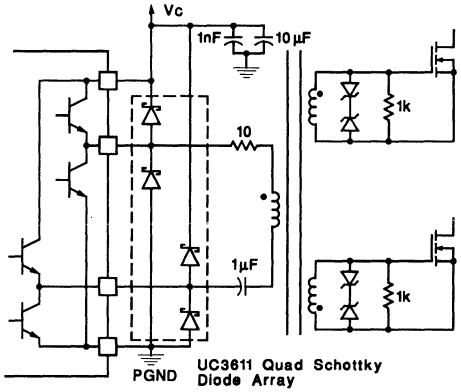
APPLICATIONS

Power Bipolar Drive Circuit



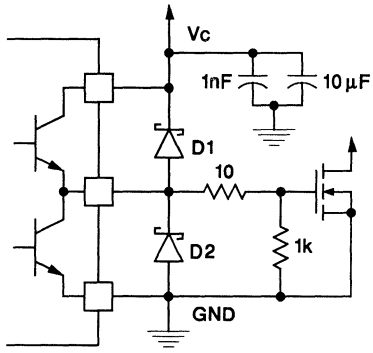
D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



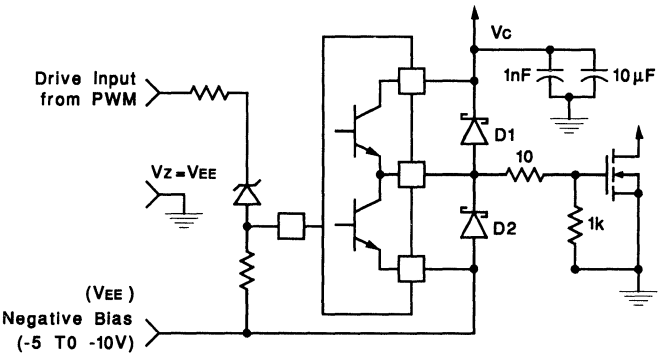
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit



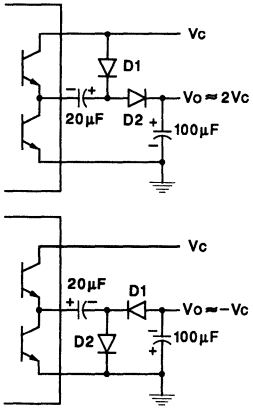
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS

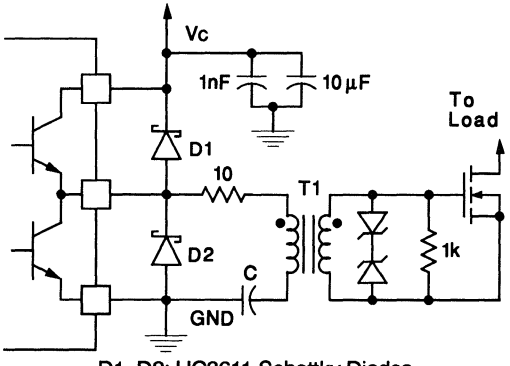


D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

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7

INTEGRATED CIRCUITS
UNITRODE

UC1710
UC3710

High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 5ns Delay
- 5ns Rise and Fall Time into 2.2nF
- 5ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and Vc can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

he UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to +125°C operation. The UC3710 is specified for a temperature range of 0°C to +70°C and is available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

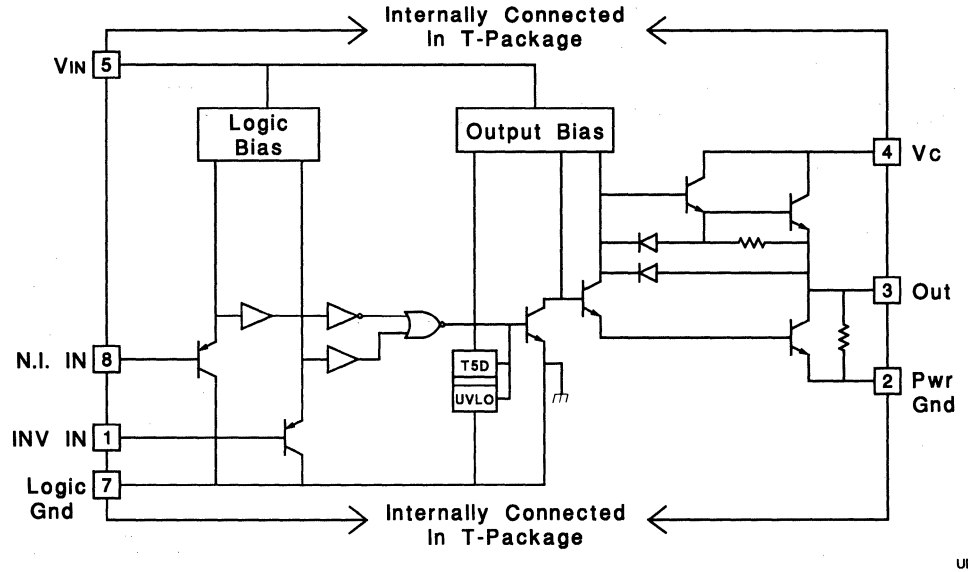
TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

OUT= $\overline{INV}$ and N.I.

$\overline{OUT}$= INV or $\overline{N.I.}$

BLOCK DIAGRAM



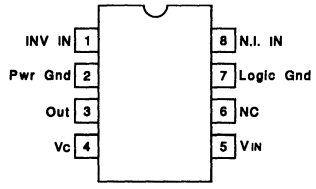
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, Vc	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1A
Digital Inputs	-0.3V-VIN	-0.3V-VIN	-0.3V-VIN
Power Dissipation at Ta=25°C	1W	1W	3W
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Operating Junction Temperature	-55°C-+150°C	-55°C-+150°C	-55°C-+150°C
Storage Temperature	-65°C-+150°C	-65°C-+150°C	-65°C-+150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

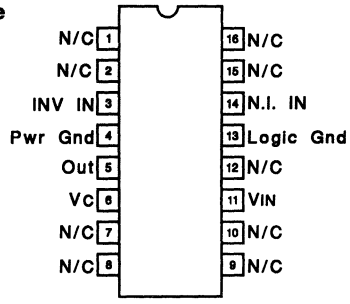
Note 1: All currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

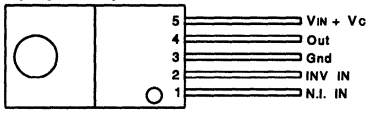
DIL-8 MINIDIP (Top View)
J or N Package



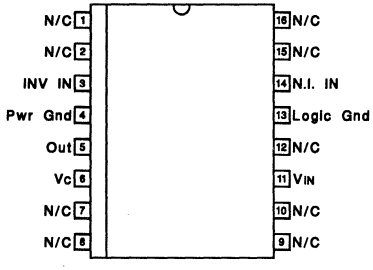
DIL-16 (Top View)
SP Package



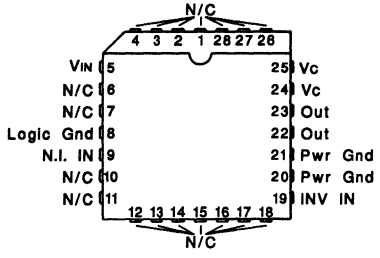
5-Pin TO-220 (Top View)
T Package



SOIC-16 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for TA =- 55°C to +125°C for the UC1710 and TA = 0 °C to +70°C for the UC3710; VIN = Vc = 15V, No load TA = TJ.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Supply Current	VIN=18V, Vc=18V, Output Low		26	35	mA
	VIN=18V, Vc=18V, Output High		21	30	mA
Vc Supply Current	VIN=18V, Vc=18V, Output Low		1.5	5.0	mA
	VIN=18V, Vc=18V,Output High		5.0	8	mA
UVLO Threshold	VIN High to Low	3.8	4.1	4.4	V
	VIN Low to High	4.1	4.4	4.8	V
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V

ELECTRICAL CHARACTERISTICS (cont.) (Unless otherwise stated, these specifications apply for T_A =- 55°C to +125°C for the UC1710 and T_A = 0 °C to +70°C for the UC3710; V_{IN} = Vc = 15V, No load. T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Current	Digital Input=0.0V	-70	-4.0		µA
Output High Sat., Vc-Vo	Io=-100mA		1.35	2.2	V
	Io=-6A		3.2	4.5	V
Output Low Sat., Vo	Io = 100mA		0.25	0.6	V
	Io = 6A		3.4	4.5	V
Thermal Shutdown			165		°C
From Inv.,Input to Output (Note 3, 4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 3,4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns

Note: 3. Delay measured from 50% input change to 10% output change.
Note: 4. Those parameters with CL = 30nF are not tested in production.
Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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INTEGRATED CIRCUITS
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UC1711
UC3711

Dual Ultra High-Speed FET Driver

FEATURES

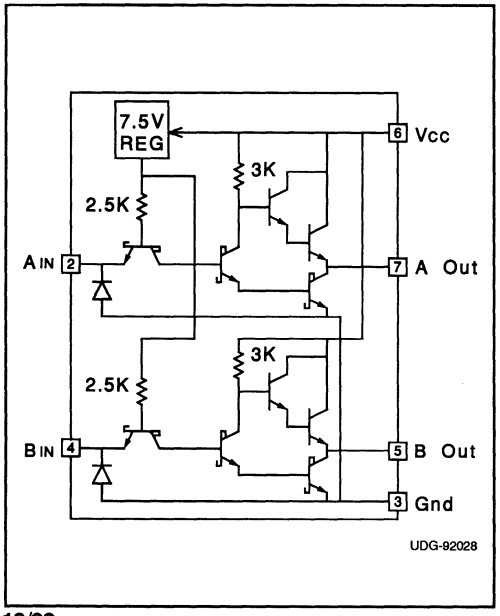
- 25ns Rise and Fall into 1000pF
- 15ns Propagation Delay
- 1.5A Source or Sink Output Drive
- Operation with 5V to 35V Supply
- High-Speed Schottky NPN Process
- 8-PIN MINIDIP Package

ABSOLUTE MAXIMUM RATINGS (note 1)

Input Supply Voltage, Vcc 40V
Output Current (Source or Sink)
  Steady State ..... +/-500mA
  Peak Transient ..... +/-1.5A
Inputs
Maximum Forced Voltage ..... -0.3V to 7V
Maximum Forced Current ..... +/- 10mA
Power Dissipation 1W
Operating Junction Temperature ..... -55°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. All reliability information for this device has been gathered at an ambient air temperature of 125°C, and a supply voltage of 25V.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

BLOCK DIAGRAM



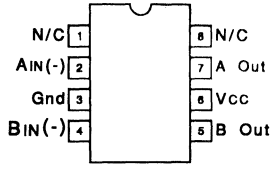
DESCRIPTION

The UC1711 family of FET drivers are made with an all-NPN Schottky process in order to optimize switching speed, temperature stability, and radiation resistance. The cost for these benefits is a quiescent supply current which varies with both output state and supply voltage. For lower power requirements, refer to the the UC1709 family which is both pin compatible with, and functionally equivalent to the UC1711.

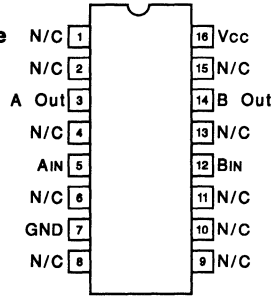
These devices implement inverting logic with TTL compatible inputs, and output stages which will either source, or sink in excess of 1.5A of load current with minimal cross-conduction charge. Due to their monolithic construction, the channels are well matched and can be paralleled for doubled output current capability.

CONNECTION DIAGRAMS

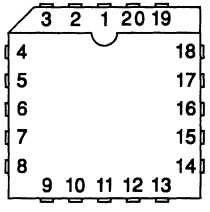
DIL-8 (Top View)
J or N Package



DIL-16 (Top View)
J E or NE Package



PLCC-20 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
AIN	2
N/C	3 - 5
GND	6
N/C	7 - 9
BIN	10
N/C	11 - 13
B Out	14
N/C	15
Vcc	16
N/C	17
A Out	18
N/C	19
N/C	20

7

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, Vcc = 15V. T_A =T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (Note 3)	Both inputs = 0V; Vcc = 15V		11	15	mA
	Both inputs = 5V; Vcc = 15V		20	27	mA
	Both inputs = 0V; Vcc = 35V		15	20	mA
	Both inputs = 5V; Vcc = 35V		41	56	mA
Logic Inputs					
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_{IN} = 0V	-5.0	-2.7		mA
	V_{IN} = 5V		0.5	2.0	mA
Output Stages					
Output High Level	I_{SOURCE} = 20mA, below Vcc		1.5	2.0	V
	I_{SOURCE} = 200mA, below Vcc		2.0	3.0	V
Output Low Level	I_{SINK} = 20mA		.25	0.4	V
	I_{SINK} = 200mA		0.4	1.0	V
Switching Characteristics (Note 4)					
Rise Time Delay, TPLH	C_{LOAD} = 0		10	40	ns
	C_{LOAD} = 1000pF, (Note 5)		15	50	ns
	C_{LOAD} = 2200pF		20	55	ns
Fall Time Delay, TPHL	C_{LOAD} = 0		3	20	ns
	C_{LOAD} = 1000pf, (Note 5)		5	20	ns
	C_{LOAD} = 2200pF		5	20	ns
Rise Time, TLH	C_{LOAD} = 0, (Note 5)		12	25	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Fall Time, THL	C_{LOAD} = 0, (Note 5)		7	15	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Total Supply Current	Freq = 200kHz, 50% Duty-cycle Both Channels Switching				
	C_{LOAD} = 0		17	23	mA
	C_{LOAD} = 2200pF		29	35	mA

Note 3: Supply currents at other input supply votages can be calculated by extrapolating the 15V and 35V supply currents. The impedance of the chip at the Vcc pin is linear for supply voltages from 8V to 35V, the approximate value of this impedance is 4.3k for both inputs low, 0.94k for both inputs high, and 1.54k for one input high and one low.

Note 4: Switching test conditions are, Vcc = 15V, Input voltage waveform levels are 0V and 5V, with transition times of <3ns. The timing terms are defined as : TPHL Propagation delay 50% V_{IN} to 90% V_{OUT}; TPLH Propogation delay 50% V_{IN} to 10% V_{OUT}; THL 90% V_{OUT} to 10% V_{OUT}; TLH 10% V_{OUT} to 90% V_{OUT}.

Note 5: This specification not tested in production.Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, Vcc = 15V. T_A = T_J.

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INTEGRATED CIRCUITS
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UC1724
UC2724
UC3724

Isolated Drive Transmitter

FEATURES

- 500mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Logic Signal Instantly
- Programmable Operating Frequency
- Under-Voltage Lockout
- Able To Pass DC Information Across Transformer
- Up To 600kHz Operation

DESCRIPTION

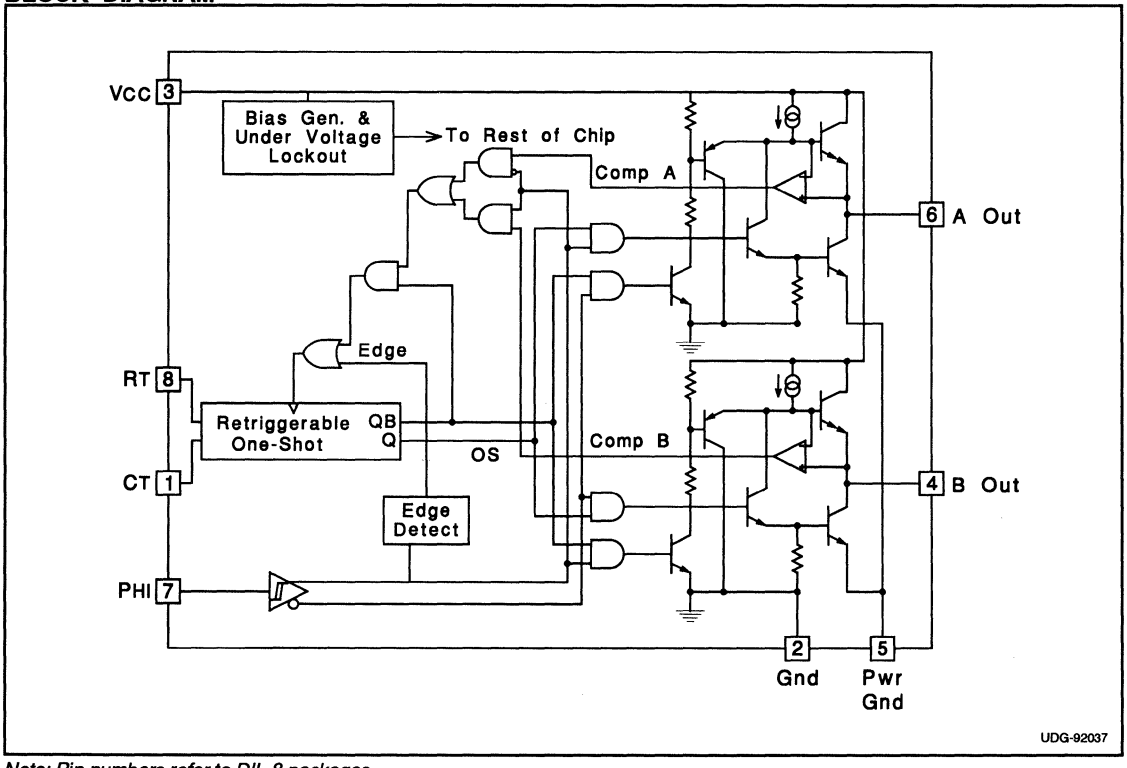
The UC1724 family of Isolated Drive Transmitters, along with the UC1725 Isolated Drivers, provide a unique solution to driving isolated power MOSFET gates. They are particularly suited to drive the high-side devices on a high-voltage H-bridge. The UC1724 devices transmit drive logic, and drive power, to the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty-cycle modulation technique that gives instantaneous response to the drive control transistions, and reliably passes steady-state, or DC, conditions. High frequency operation, up to 600kHz, allows the cost and size of the coupling transformer to be minimized.

These devices will operate over an 8 to 35 Volt supply range. The dual high current totem pole outputs are disabled by an uder-voltage lockout circuit to prevent spurious responses during startup or low voltage conditions.

These devices are available in 8-pin plastic or ceramic dual-inline packages, as well as surface mount packages.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-8 packages.

7

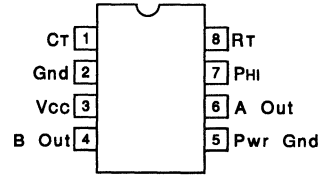
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} 40V
Source/Sink Current (Pulsed) 1A
Source/Sink Current (Continuous) 0.5A
Ouput Voltage (Pins 4, 6) ..... -0.3 to (V_{IN} +0.3)V
PHI, R_T, and C_T inputs (Pins 1, 7, and 8) ..... -0.3 to 6V
Operating Junction Temperature (Note 2) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

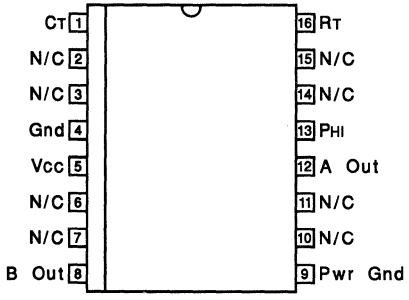
Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.
Note 2: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.
Note 3: Pin numbers refer to DIL-8 packages.

CONNECTION DIAGRAMS

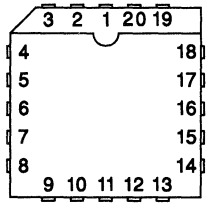
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Vcc	2
N/C	3-4
B Out	5
N/C	6
Pwr Gnd	7
N/C	8-9
A Out	10
N/C	11
PHI	12
N/C	13-14
RT	15
N/C	16
CT	17
N/C	18-19
Gnd	20

RECOMMENDED OPERATION CONDITIONS (Note 4)

Input Voltage ..... +9V to +35V
Sink/Source Load Current (each output) ..... 0 to 500mA
Timing Resistor ..... 2kΩ to 10kΩ
Timing Capacitor ..... 300pF to 3nF
Operating Temperature Range (UC1724) ..... -55°C<T_A<125°C
Operating Temperature Range (UC3724) ..... 0°C<T_A<70°C

Note 4: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, Vcc = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C<T_A<125°C for the UC1724, –25°C<T_A<85°C for the UC2724, and 0°C<T_A<70°C for the UC3724. T_A=T_J.

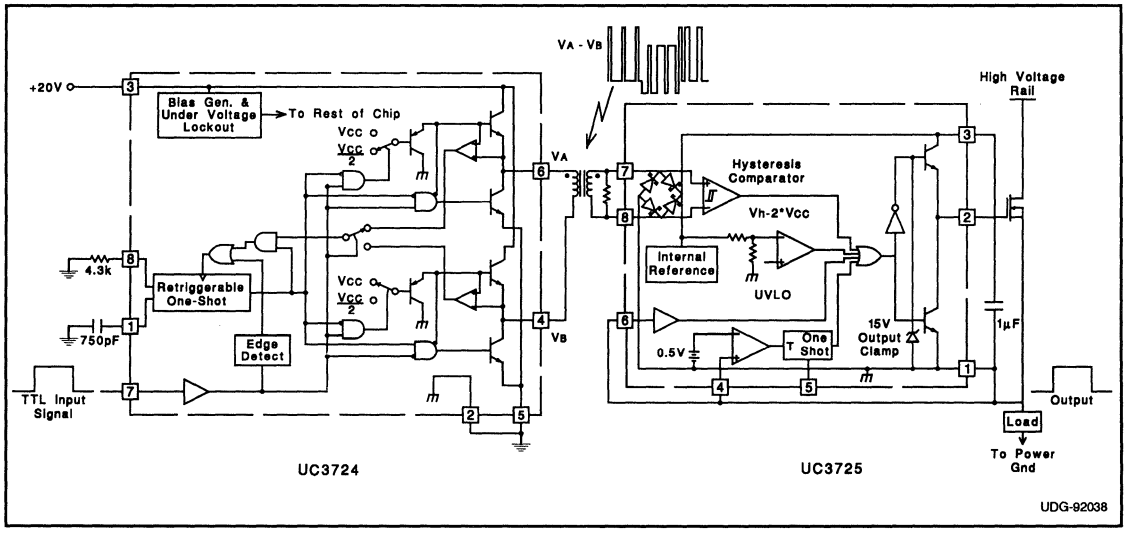
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Under-Voltage Lockout					
Start-Up Threshold	V_{IN} Rising		7.75	9.5	V
Threshold Hysteresis		0.4	1.0	1.5	V
Retriggerable One-Shot					
Initial Accuracy	T_J = 25°C	1.54	1.9	2.25	µs
Temperature Stability	Over Operating T_J	1.0		2.9	µs
Voltage Stability	V_{IN} = 10 to 35V		0.2	0.5	%/V
Operating Frequency	L_{LOAD} = 1.4mH	100	150	200	kHz
Minimum Pulse Width	RT = 2k CT = 300pF			500	ns
Operating Frequency	RT = 2k C_T = 300pF L_{LOAD} = 1.4mH	500	750	1100	kHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC} = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C<T_A<125°C for the UC1724, –25°C<T_A<85°C for the UC2724,and 0°C<T_A<70°C for the UC3724. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phi Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current	V_{IH} = +2.4V	-220	-130		mA
LOW Input Current	V_{IL} = +0.4V	-600	-300		µA
Delay to One-Shot				350	ns
Delay to Output				250	ns
Output Drivers					
Output Low Level	I_{SINK} = 500mA		0.3	0.4	V
	I_{SINK} = 250mA		0.5	2.1	V
Output High Level (Volts Below V_{CC})	I_{SOURCE} = 250 mA		1.5	2.1	V
	I_{SOURCE} = 250 mA		1.7	2.5	V
Rise/Fall Time	No load		30	90	ns
Total Supply Current					
Supply Current	C_T = 1.4V		15	30	mA

Typical Application



7

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Isolated High Side FET Driver

FEATURES

- Receives Both Power and Signal Across the Isolation Boundary
- 9 to 15 Volt High Level Gate Drive
- Under-voltage Lockout
- Programmable Over-current Shutdown and Restart
- Output Enable Function

DESCRIPTION

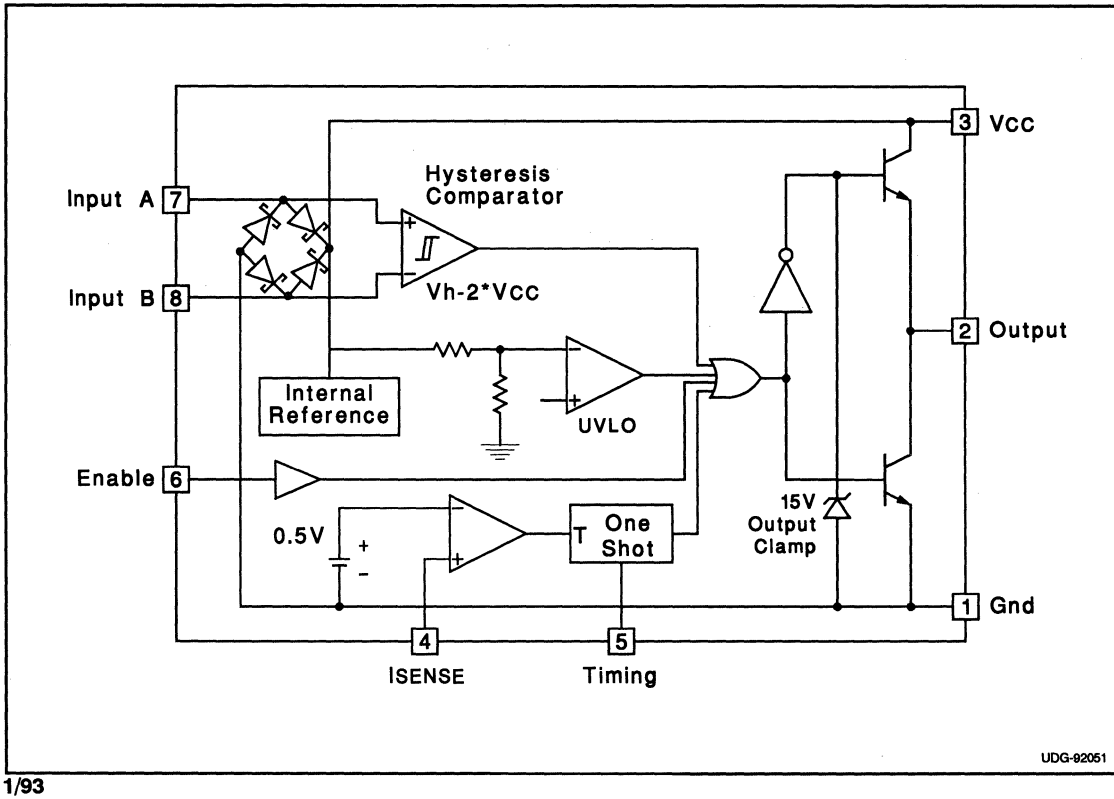
The UC1725 and its companion chip, the UC1724, provide all the necessary features to drive an isolated MOSFET transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signals across an isolation boundary with a minimum of external components.

Protection circuitry, including under-voltage lockout, over-current shutdown, and gate voltage clamping provide fault protection for the MOSFET. High level gate drive is guaranteed to be greater than 9 volts and less than 15 volts under all conditions.

Uses include isolated off-line full bridge and half bridge drives for driving motors, switches, and any other load requiring full electrical isolation.

The UC1725 is characterized for operation over the full military temperature range of -55°C to +125°C while the UC2725 and UC3725 are characterized for -25°C to +85°C and 0°C to +70°C respectively.

BLOCK DIAGRAM



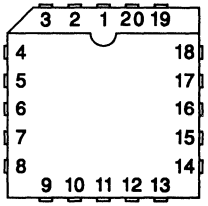
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 3) 30V
Power inputs (pins 7 & 8) 30V
Output current, source or sink (pin 2)
DC 0.5A
Pulse (0.5 us) 2.0A
Enable and Current limit inputs (pins 4 & 6) ..... -0.3 to 6V
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals (pin numbers refer to DIL-8 package).
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

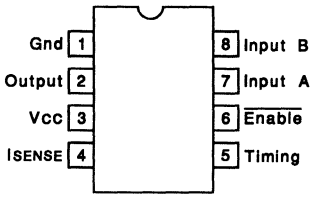
CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package

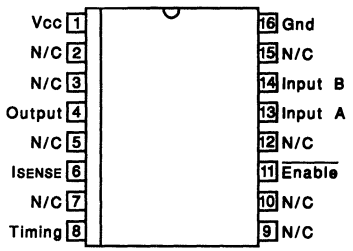


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
ISENSE	2
N/C	3-5
Timing	6
$\overline{\text{Enable}}$	7
N/C	8-9
Input A	11
N/C	12-14
Input B	15
Gnd	16
Vcc	17
N/C	18-19
Output	20

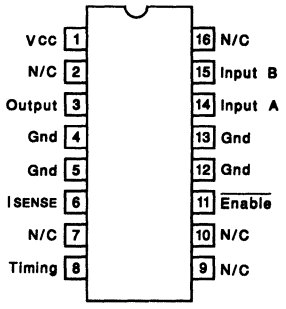
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE Or NE Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq +125°C$ for UC1725; $-25°C \leq T_A \leq +85°C$ for UC2725; $0°C \leq T_A \leq +70°C$ for UC3725; Vcc (pin 3) = 0 to 15V, R_T=10k, C_T=2.2nf, $T_A = T_J$, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT SECTION (PINS 7 & 8)					
Forward Diode Drop, Schottky Rectifier	I_F = 50ma		.55	.7	V
	I_F = 500ma		1.1	1.5	V
CURRENT LIMIT SECTION (PIN 4)					
Input bias current	V_{PIN4} = OV		-1	-10	µA
Threshold voltage		0.4	0.5	0.6	V
Delay to outputs	V_{PIN4} = 0 to 1V		100	250	ns
TIMING SECTION (PIN 5)					
Output Off Time		27	30	33	µs
Upper Mono Threshold		6.3	7.0	7.7	V
Lower Mono Threshold		1.9	2.0	2.3	V
HYSTERESIS AMPLIFIER (PINS 7 & 8)					
Input Open Circuit Voltage	Inputs (pins 7 & 8), Open Circuited, T_A= 25°C	7.0	Vcc/2	8.0	V
Input Impedance	T_A = 25°C	23	28	33	kΩ
Hysteresis		26.5	2*Vcc	30.5	V
Delay to Outputs	$V_{PIN7} - V_{PIN8}$ = Vcc + 1V		100	300	ns

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for -55°C≤TA≤+125°C for UC1725; -25°C≤TA≤+85°C for UC2725; 0°C≤TA≤+70°C for UC3725; Vcc (pin 3) = 0 to 15V, Rt=10k, CT=2.2nf, TA =TJ, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE SECTION (PIN 6)					
High Level Input Voltage		2.1	1.4		V
Low Level Input Voltage			1.4	.8	V
Input Bias Current			-250	-500	µA
OUTPUT SECTION					
Output Low Level	IOUT = 20mA		0.35	0.5	V
	IOUT = 200mA		0.6	2.5	V
Output High Level	IOUT = -20mA	13	13.5		V
	IOUT = -200mA	12	13.4		V
	Vcc = 30V, Iout = -20mA		14	15	V
Rise/Fall Time	CT = 1nf		30	60	ns
UNDER VOLTAGE LOCKOUT					
UVLO Low Saturation	20mA, Vcc = 8V		0.8	1.5	V
Start-up Threshold		11.2	12	12.6	V
Threshold Hysteresis		.75	1.0	1.12	V
TOTAL STANDBY CURRENT					
Supply Current			12	16	ma

APPLICATION AND OPERATION INFORMATION

INPUTS: Figure 1 shows the rectification and detection scheme used in the UC1725 to derive both power and signal information from the input waveform. Vcc is generated by peak detecting the input signal via the internal bridge rectifier and storing on a small external capacitor, C1. Note that this capacitor is also used to bypass high pulse currents in the output stage, and therefore should be placed direclty between pins 1 and 3 using minimal lead lengths.

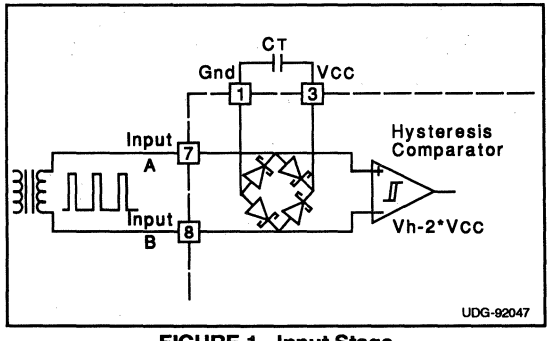


FIGURE 1 - Input Stage

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (resetting) the comparator only if the input signal exceeds Vcc (-Vcc). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis amplifier as shown in Figure 3.

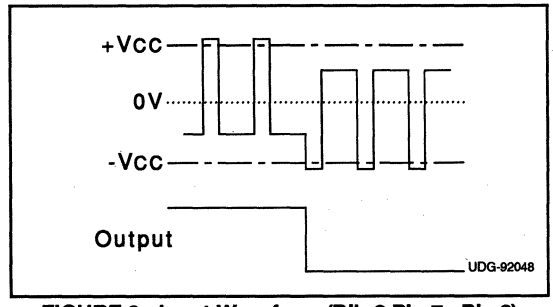


FIGURE 2 - Input Waveform (DIL-8 Pin 7 - Pin 8)

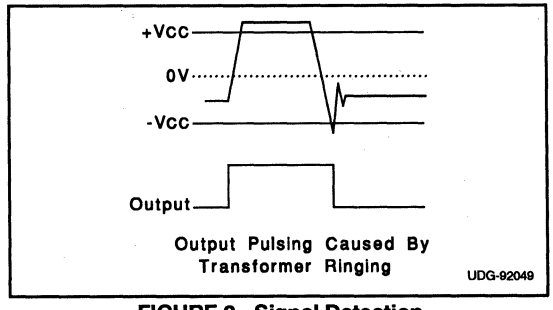


FIGURE 3 - Signal Detection

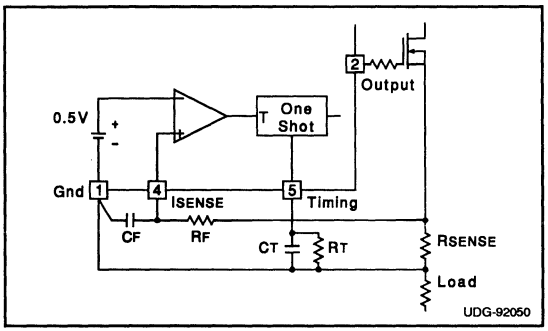


FIGURE 4 - Current Limit

CURRENT LIMIT AND TIMING: Current sensing and shutdown can be implemented directly at the output using the scheme shown in Figure 4. Alternatively, a current transformer can be used in place of RSENSE. A small RC filter in series with the input (pin 4) is generally needed to eliminate the leading edge current spike caused by parasitic circuit capacitances being charged during turn on. Due to the speed of the current sense circuit, it is very important to ground CF directly to Gnd as shown to eliminate false triggering of the one shot caused by ground drops.

One shot timing is easily programmed using an external capacitor and resistor as shown in Figure 4. This, in turn, controls the output off time according to the formula:

$$T_{OFF} = 1.28 \cdot RC.$$

If current limit feature is not required, simply ground pin 4 and leave pin 5 open.

OUTPUT: Gate drive to the power FET is provided by a totem pole output stage capable of sourcing and sinking currents in excess of 1 amp. The undervoltage lockout circuit guarantees that the high level output will never be less than 9 volts. In addition, during undervoltage lockout, the output stage will actively sink current to eliminate the need for an external gate to source resistor. High level output is also clamped to 15 volts. Under high capacitive loading however, the output may overshoot 2 to 3 volts, due to the drivers' inabitlity to switch from full to zero output current instantaneously. In a practical circuit this is not normally a concern. A few ohms of series gate resistance is normally required to prevent parasitic oscillations, and will also eliminate overshoot at the gate.

ENABLE: An enable pin is provided as a fast, digital input that can be used in a number of applications to directly switch the output. Figure 6 shows a simple means of providing a fast, high voltage translation by using a small signal, high voltage transistor in a cascode configuration. Note that the UC1725 is still used to provide power, drive and protection circuitry for the power FET.

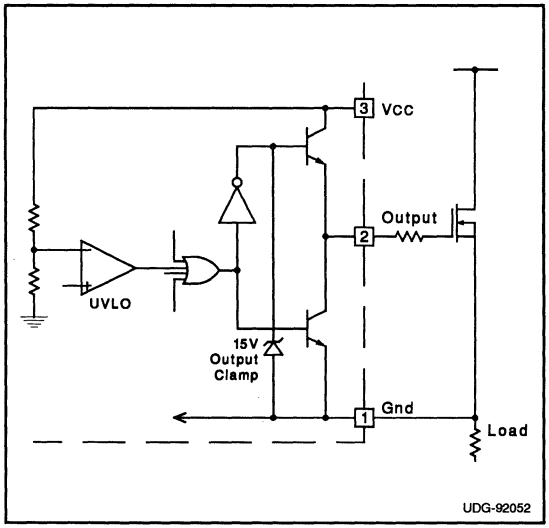


FIGURE 5 - Output Circuit

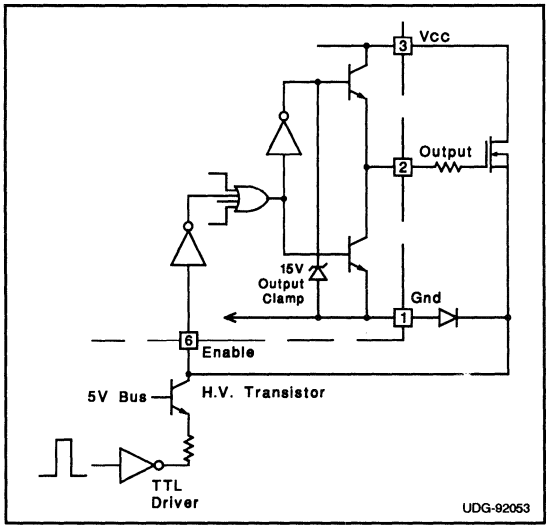


FIGURE 6 - Using Enable Pin as a High Speed Input Path

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INTEGRATED CIRCUITS
UNITRODE

Isolated Drive Transmitter

UC1726
UC2726
UC3726
PRELIMINARY

FEATURES

- 750mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Logic Signal Instantly
- Programmable Operating Frequency
- Able To Pass DC Information Across Transformer
- Up To 750kHz Operation
- Improved Output Control Algorithm Minimizes Output Jitter
- Fault Logic Monitors Isolated Driver IC (UC1727) for Faults
- User Programmable Fault Timing Screens False Fault Signals
- Shutdown Mode Disables On Chip Logic Reference for Low Standby Power
- Optional External Biasing of Logic Circuitry Can Reduce Overall Power Dissipation

DESCRIPTION

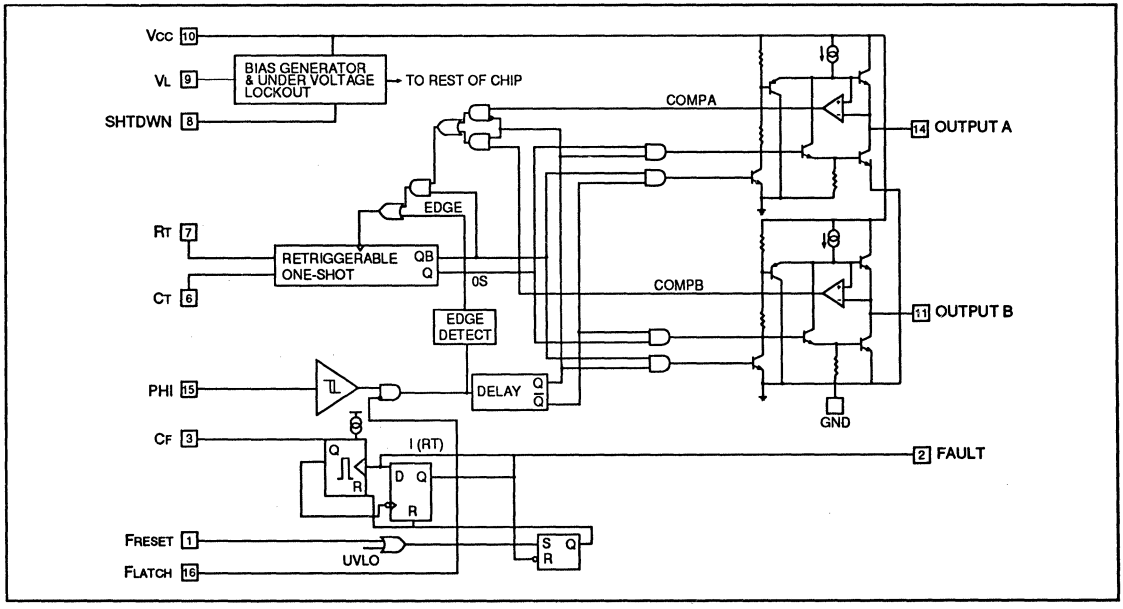
The UC1726 family of Isolated Drive Transmitters, along with the UC1727 Isolated Drivers, provide a unique solution to driving isolated power IGBTs. They are particularly suited to drive the high-side devices on a high-voltage H-bridge. The UC1726 device transmits the drive logic and drive power, along with transferring and receiving fault information with the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty-cycle modulation technique that gives instantaneous response to the drive control transitions, and reliably passes steady-state, or DC conditions. High frequency operation, up to 750kHz, allows the cost and size of the coupling transformer to be minimized.

The IC can be powered from a sole Vcc supply which internally generates a voltage reference for the logic circuitry. It can be placed into a low power, shutdown mode that will disable the internal reference. The IC's logic circuitry can be powered from an external supply to minimize overall power dissipation. The fault logic monitors the Isolated Driver IC (UC1727) for faults. Based on user defined timing, the IC distinguishes valid faults which it responds to by setting the fault latch pin. This will also disable the gate drive information until the fault reset pin is toggled to a logic one.

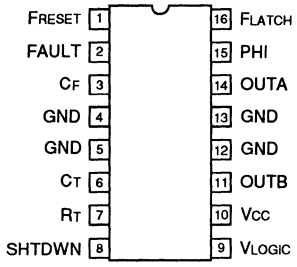
These devices will operate over an 8 to 35 volt supply range. The typical Vcc voltage will be above 28 volts to be compatible with the UC1727. The under voltage lock out circuitry of the Isolated Driver IC (UC1727) will effectively lock out the drive information during its under voltage lockout.

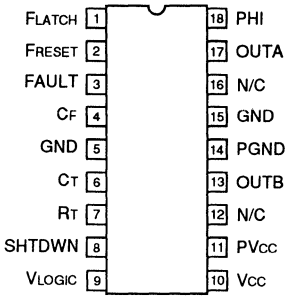
BLOCK DIAGRAM

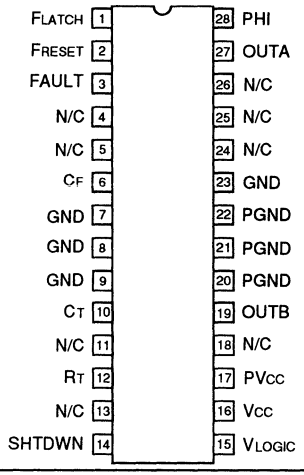


CONNECTION DIAGRAMS

DIL-16, 18 J, 28 DWP (TOP VIEWS)







ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 40V
Source/Sink Current (Pulsed) 1.5A
Source/Sink Current (Continuous) 1.0A
Output Voltage (pins 12, 14) ..... -0.3 to (V_{CC}+0.3)V
C_F, FRESET, FAULT, SHTDWN,
FLATCH, V_L, PHI, R_T ..... -0.3 to 6.0V
C_T ..... 1.0 to 6.0V
Operating Junction Temperature (Note 2) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.

RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage ..... +9 to +35.0V
Sink/Source Current (each output) ..... 0 to 750mA
Timing Resistor ..... 2.4k to 200kOhm
Timing Capacitor (C_T) ..... 75pF to 2.0nF
Timing Capacitor (C_F) ..... 75pF to 3.0nF

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Note 3: Range over which the device is functional and parameter limits are guaranteed.

PIN DESCRIPTIONS

FRESET: The input to the fault logic that resets the fault logic latch (FLATCH) and enables drive transmit data. This input should be powered up low and stay low until after the fault latch has been set.

FAULT: This input to the fault logic initiates the user programmable timer. This time interval specified by the capacitor on C_F determines the validity of the fault. The pin is tied to a low cost opto-coupler, and is high until the UC1727 powers up, and drives it low indicating proper power-up. The UC1726 sends drive information from the PHI pin through the transformer while the FAULT pin stays low. Once this pin goes high, it must stay high during the entire fault window to be accepted as a valid fault. A valid fault sets the FLATCH pin high and prevents the transmitting of gate drive information until the FRESET is toggled high.

C_F: The timing input to the fault logic. A capacitor is placed across the input of C_F and ground. The timing window is roughly determined by $t = C_F * R_T * 2.1$.

GND: The signal and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

C_T: The input of the timing capacitor that controls the operating frequency. A capacitor to ground is repetitively charged during the one shot pulse width. It is discharged when a comparator senses zero current in the primary side of the transformer. The one shot pulse width is consequently determined by the time it takes to charge the capacitor to a threshold voltage of VL/2. This pin is intended to be tied to a capacitor.

R_T: The input that sets the C_T and C_F capacitor currents with a resistor to ground. The voltage on R_T is approximately V_L* (0.3V). The resulting charge currents are: $I_{CT} = I_{CF} = V_L/(4 * R_T)$.

SHTDWN: This input shuts down the internal reference. A TTL logic one voltage will put the IC into a low standby current mode. This input has a pull down resistor on the chip to guarantee proper operation when left open. If an external logic voltage is applied to V_L, this shutdown feature cannot be used without bringing the external voltage source to zero volts.

V_L: The logic supply pin that biases all circuits except for the totem pole outputs. A bypass capacitor is recommended on this pin when left unconnected. The internal reference is approximately 4.4V. A 5.0V supply can be applied to this pin to assure minimum power dissipation. When an external supply higher than the V_L voltage is applied to this pin, the internal reference turns off.

Vcc: The input voltage that biases the outputs and the internal reference. It can vary between 8V to 35V. This supply pin will typically be above 28V to be compatible with the 1727 application.

OUTB: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output will toggle between Vcc-1.5V during the oneshot charge time and approximately Vcc*.6 during the rest of the period. When PHI is low the output will toggle between 0.3V during the oneshot charge time and approximately Vcc+0.4V during the remainder of the period.

OUTA: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output will toggle between 0.3V during the oneshot charge time and approximately Vcc+0.4 during the rest of the period. When PHI is low the output will toggle between Vcc-1.5V during the oneshot charge time and approximately Vcc*.6 during the remainder of the period.

PHI: A logic control input to the isolated gate driver that changes the outputs as described above. This will change the duty-cycle of the voltage wave form applied across the transformer. The isolated drive IC (UC1727) will sense the different duty-cycles as different drive commands.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC}=20V, R_T=4.32kΩ, C_T=330pF and C_F=2.2nF, no load on any output, and -55°C<T_A <125°C for the UC1726, -25°C<T_A<85°C for the UC2726 and 0°C<T_A<70°C for the UC3726, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RETRIGGERABLE ONE-SHOT					
Initial Accuracy	T_J = 25°C	1.250	1.350	1.450	µSec
Temperature Stability	Over Operating T_J	1.010		1.990	µSec
Voltage Stability	V_{CC} = 10 to 35V		0.2		%/V
Operating Frequency	L_{LOAD} = 1.5mH		200		kHz
PHI INPUT (CONTROL INPUT					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current			10		µA
LOW Input Current		-600	-300		µA
Delay to One-Shot			100	250	nSec
Delay to Output	C_T = 1.4V		250		nSec
OUTPUT DRIVERS					
Output Low Level	I_{SINK} = 50mA		0.3	0.4	V
	I_{SINK} = 750mA		1.5	2.1	V
Output High Level (volts below Vcc)	I_{SOURCE} = 50mA		1.5	2.1	V
	I_{SOURCE} = 750mA		1.7	2.1	V
Rise/Fall Time	No load		30	90	nSec
LOGIC VOLTAGE REF.					
VL-Logic Voltage	Internal Voltage	4.30	4.4	4.50	V
Logic Supply Current	V_L = 4.75V to 5.25V		12.0	18.0	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC}=20V, R_T=4.32kOhm, C_T=330pF and C_F=2.2nF, no load on any output, and -55°C<T_A<125°C for the UC1726, -25°C<T_A<85°C for the UC2726 and 0°C<T_A<70°C for the UC3726, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SHUT DOWN CIRCUIT					
Logic Voltage-Off			0.5		V
High Input Current	V_{IH} = 2.4	-100			µA
Low Input Current	V_{IL} = 0.4	-20			µA
FAULT LOGIC					
Fault Reset					
High Input Current	V_{IH} = 2.4	-5		5	µA
Low Input Current	V_{IL} = 0.4	-10			µA
Fault High Input Current	V_{IH} = 2.4	-5		5	µA
Fault Low Input Current	V_{IL} = 0.4	-10			µA
Supply Current	C_T = 1.4V, Shutdown = 5.0V		2.5		mA
Min Fault Pulse	C_F = 330pF		3.0		µS
Max Fault Pulse	C_F = 2.2nF		20.0		µS
Fault Latch, V_{OH}	I_{LOAD} = -1mA, Volts Below VL	1.7	1.3		V
Fault Latch, V_{OL}	I_{LOAD} = 1mA		0.25	0.4	V
Fault Latch, V_{OH}	I_{LOAD} = 0, Volts Below VL	0.3		V	
Fault Latch, V_{OL}	I_{LOAD} = 0		0.2		V
TOTAL SUPPLY CURRENT					
Supply Current	C_T = 1.4V		20	40	mA
Supply Current	C_T = 1.4V, VL = 5.0V		10	16	mA

OPERATING FREQUENCY:

The chip operating frequency is determined by both the R_T and C_T pins. A resistor between R_T and ground will set the charge current to I_{CT} = V_L/(R_T*4). The operating frequency varies slightly depending on the V_{CC} and V_L voltages. The following two equations are for V_{CC} = 20V.

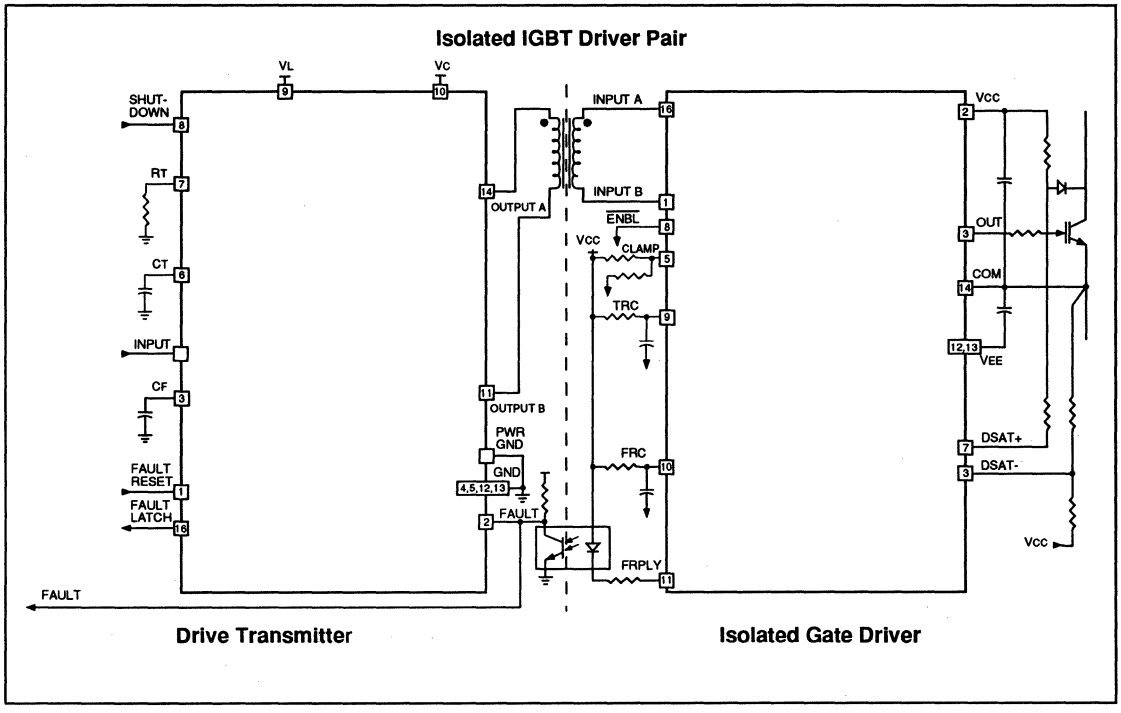
V_L = Internal Reference (4.4V)

$$F_O = 1/(R_T * C_T * (2.959) + 0.83 \times 10^{-6})$$

V_L = External Reference (5V)

$$F_O = 1/(R_T * C_T * (2.700) + 0.46 \times 10^{-6})$$

TYPICAL APPLICATION



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INTEGRATED CIRCUITS
UNITRODE

UC1727
UC2727
UC3727
PRELIMINARY

Isolated High Side IGBT Driver

FEATURES

- Receives Power and Signal from Single Isolation Transformer
- Generates Split Rail for 4A Peak Bipolar Gate Drive
- 16V High Level Gate Drive
- Low Level Gate Drive more Negative than -5V
- Under Voltage Lockout
- Desaturation Detection and Fault Processing
- Separate Output Enable Input
- Programmable Stepped Gate Drive for Soft Turn On
- Programmable Stepped Gate Drive for Soft Fault

DESCRIPTION

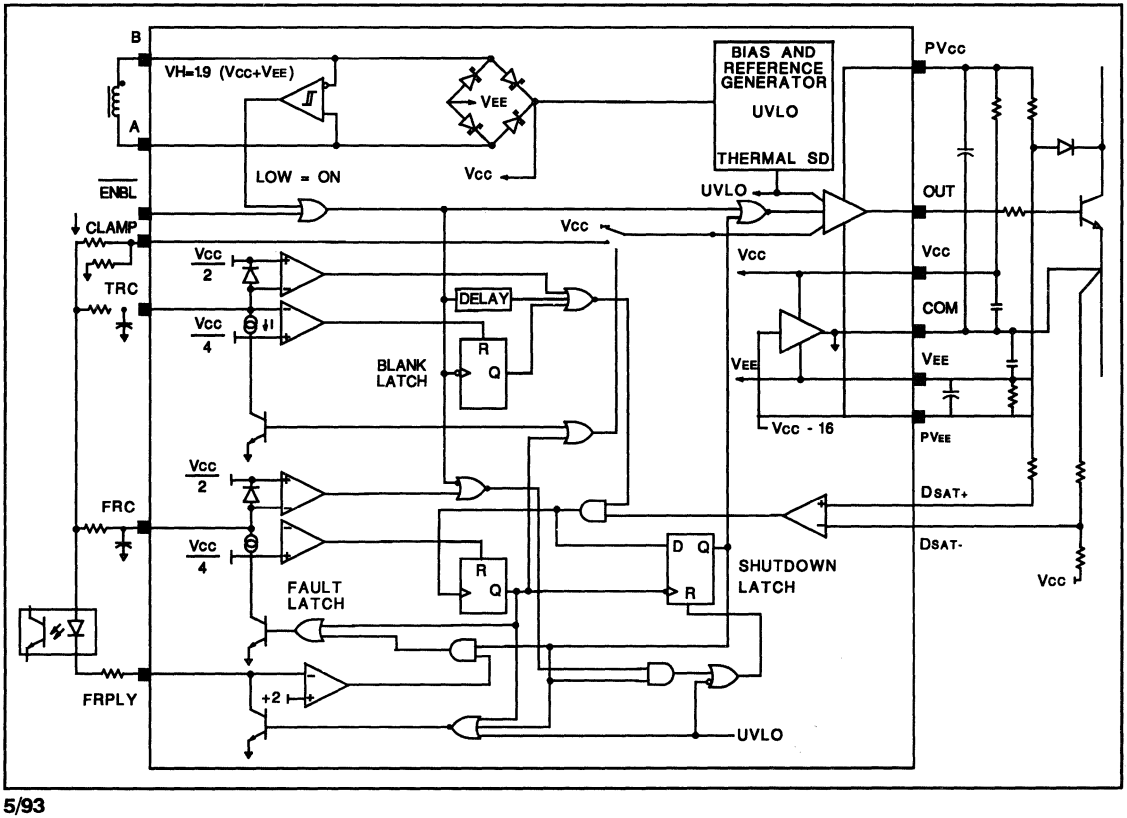
The UC1727 and its companion chip, the UC1726, provide all the necessary features to drive an isolated IGBT transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signal across an isolation boundary with a minimum of external components.

Protection features include under voltage lockout and desaturation detection. High level gate drive signals are guaranteed to be 16V. Intermediate high drive levels can be programmed for various periods of time to limit surge current at turn on and in the event of desaturation due to short circuit.

The chip generates a bipolar supply so that the gate can be driven to a negative voltage to insure the IGBT remains off in the presence of high common mode slew rates.

Uses include isolated off-line full bridge and half bridge drives for motors, switches, and any other load requiring full electrical isolation.

BLOCK DIAGRAM



5/93

7

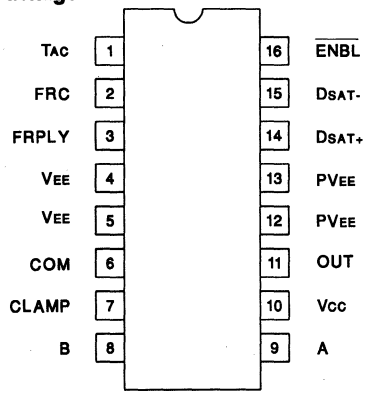
ABSOLUTE MAXIMUM RATINGS

Supply voltage (Vcc - VEE) 40V
Power Inputs (|A - B|) 45V
Analog Input Voltage ($\overline{ENBL}$, CLAMP) ..... -0.3 To Vcc+0.3
Analog Input Voltage (DSAT+, DSAT-) ..... VEE-0.3 to Vcc+0.3
Analog Input Current (DSAT+, DSAT-) ..... -10 to 10mA
Output Current, |(OUT)|
DC 0.8A
Pulse (0.5µs) 4A
FRPLY Output Current 30mA

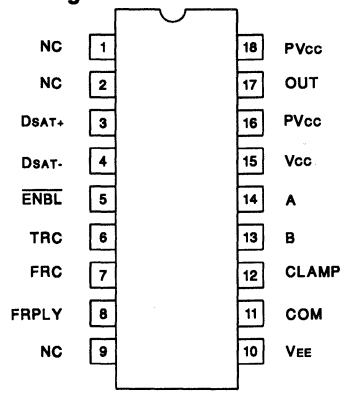
Note: All voltages are with respect to COM. Currents are positive into the specified terminal.

CONNECTION DIAGRAMS

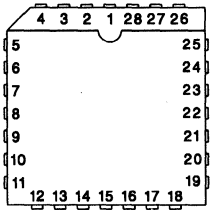
DIL-16 (Top View)
N or J Package



18 Pin Sidebrazed
Ceramic Package

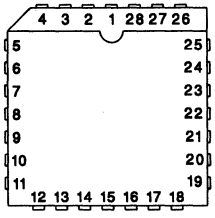


PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
VEE	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
VCC	9
PVCC	10
OUT	11
PVEE	12-18
DSAT+	19
DSAT-	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26
N/C	27
N/C	28

LCC-28 (TOP VIEW)
L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
VEE	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
VCC	9
PVCC	10
OUT	11
N/C	12-13
PVEE	14
N/C	15-18
DSAT+	19
DSAT-	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26-28

PIN FUNCTIONS

A & B: Signal and power input pins. Connect these pins to the secondary of the transformer driven by UC1726.

CLAMP: Analog Programming pin for intermediate drive level to be used at turn on or in response to a desaturation event. Requires a bypass capacitor to COM.

COM: Self generated common for bipolar supply. This pin will be 16.5V below Vcc.

DESAT+ & DESAT-: Inputs to the desaturation comparator. Desaturation is detected when $DE_{SAT+} > DE_{SAT-}$.

$\overline{ENBL}$: Negative-true enable input. Tie to Vcc to disable the chip. Short to COM to enable the Chip. If the $\overline{ENBL}$ pin is to be used as the primary input to the chip, short A to Vcc and B to V_{EE}.

FRC: Fault Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential during a desaturation event before it is driven fully low. Also sets the period of time that OUT will be held low before allowing it to be driven high again.

FRPLY: Fault Reply pin. Open collector output. Normally shorted to COM. When desaturation is detected, the pin will open.

OUT: Gate drive output. Connect to gate of IGBT with a damping resistor >3 ohms.

TRC: Timing Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential and the period of time the desaturation comparator will be ignored during the rising edge.

Vcc: Positive supply voltage. Bypass to COM.

V_{EE}: Negative supply voltage. Bypass to COM.

PVEE: Output driver negative supply. Connect to V_{EE} with 2.2 ohms and bypass to COM.

PVcc: Output driver positive supply. Connect to Vcc with 2.2 ohms and bypass to COM.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UC3727, T_A = -25 to 85°C for the UC2727, T_A = -55 to 125°C for the UC1727, R(TRC) = 54.9k, C(CTC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, Vcc - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT RECEIVERS					
Forward Diode Drop	I_F = 50mA		0.4	0.6	V
	I_F = 500mA		1.2	2	V
VCC REGULATOR					
Vcc	25 ≤ (Vcc - V_{EE}) ≤ 36V, |I(COM)| ≤ 15mA	15.5	16.5	17.5	V
HYSTERESIS COMPARATOR					
Input Open Circuit Voltage	(Measured with respect to V_{EE})		12.5		V
Input Impedance		50	100	180	kΩ
Hysteresis		45	47.5	50	V
ENABLE INPUT					
High Level Input Voltage				12	V
Low Level Input Voltage		5			V
Input Bias Current	$\overline{ENBL}$ = COM		-460	-900	µA
OUTPUT DRIVER					
Saturation to Vcc	I(OUT) = -20mA		1.7	2.3	V
Saturation to Vcc	I(OUT) = -500mA		2	2.5	V
Saturation to V_{EE}	I(OUT) = 20mA		2	3	V
Saturation to V_{EE}	I(OUT) = 500mA		2.4	3.4	V
Turn on Clamp Voltage	I(OUT) = -100mA	7	9	11	V
Fault Clamp Voltage	|I(OUT)| = 100mA	7	9	11	V
UVLO Saturation to V_{EE}	I(OUT) = 20mA,Vcc no connection		1.5	2	V
Rise/Fall Time	Cl = 1n, CLAMP = Vcc, R_{OUT} = 3Ω		75	150	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UC3727, T_A = -25 to 85°C for the UC2727, T_A = -55 to 125°C for the UC1727, R(TRC) = 54.9k, C(CTC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, Vcc - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TURN ON SEQUENCE TIMER					
Clamped Driver Time		0.5	1	1.5	µs
Blanking Time		3	5	7	µs
FAULT MANAGER					
Clamped Driver Time		0.5	1	1.5	µs
Fault Lock Off Time		15	25	35	µs
FRPLY Saturation	I(FRPLY) = 10mA		0.8	1.2	V
FRPLY Leakage	FRPLY = Vcc		0	10	µA
DESATURATION DETECTION COMPARATOR					
Input Offset Voltage (|vio|)	V_{CM} = V_{EE}+2, V_{CM} = Vcc-2		0	20	mV
Input Bias Current			-1.5	10	µA
Delay to Output	C(FRC) = 0		150		ns
UNDER VOLTAGE LOCK OUT					
Vcc Threshold		15	16	17	V
Vcc Hysteresis		0.5	1	1.5	V
V_{EE} Threshold		5	-5.5	-6	V
V_{EE} Hysteresis		0.2	0.5	0.8	V
THERMAL SHUTDOWN					
Threshold	Not tested		175		C
Hysteresis	Not tested		45		C
TOTAL STANDBY CURRENT					
I(Vcc)			24	30	mA

APPLICATION INFORMATION

Figure 1 shows the rectification and detection scheme used in the UC1727 to derive both power and signal information from the input waveform. Vcc-V_{EE} is generated by peak detecting the input signal via the internal bridge rectifier and storing on external capacitors. COM is generated by an internal amplifier that strives to maintain Vcc-C_{OM} = 16.5V. It is important to select Both Capacitors of equal value and large enough so that Vcc and V_{EE} ripple are small. Large ripple will cause the COM amplifier to dissipate excessive power.

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in figure 2. This is accomplished by setting (or resetting) the comparator only if the input signal exceeds 0.95*[Vcc-V_{EE}] (or 0.95*[V_{EE}-Vcc]). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator as shown in figure 3.

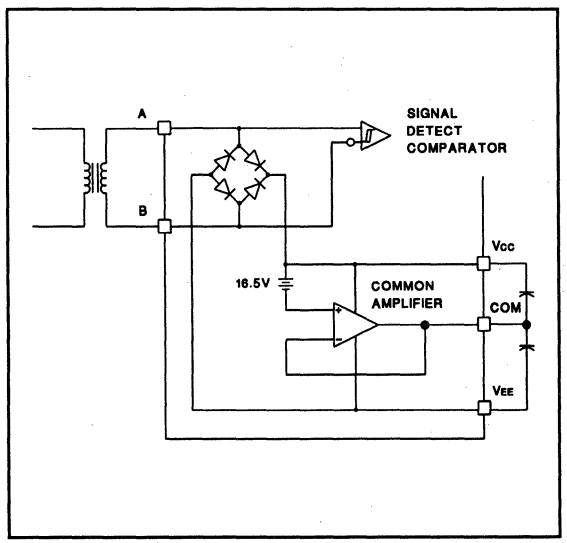


Figure 1. Input Stage & Bipolar Supply

APPLICATION INFORMATION (cont'd)

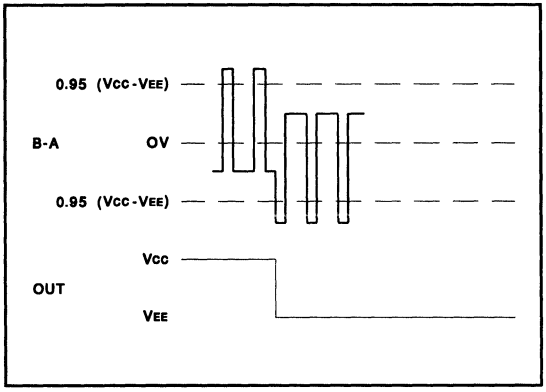


Figure 2. Input Waveform

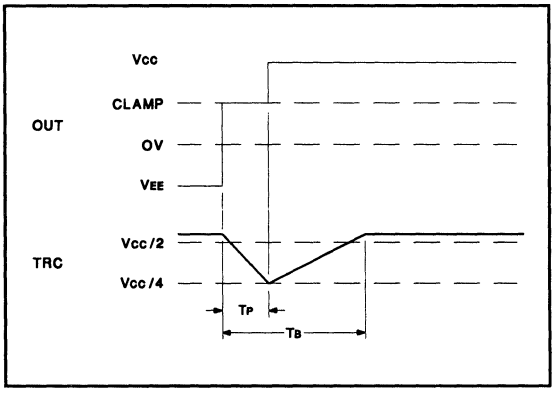


Figure 4. Rising Edge Waveform

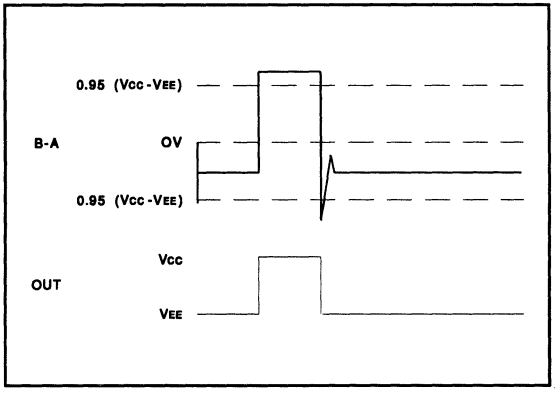


Figure 3. Output Pulsing Caused By Transformer Ringing

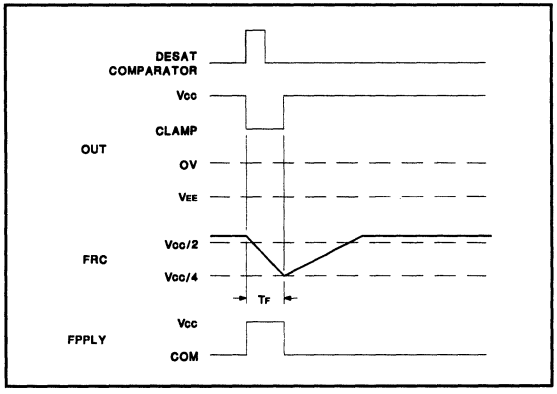


Figure 5. Transient Desaturation Response

GATE DRIVE WAVEFORM

The rising edge of OUT can be programmed for a two step sequence as shown in figure 4. The plateau voltage is programmed by a resistive divider from Vcc to COM applied at CLAMP. CLAMP must be bypassed to COM. The plateau voltage is approximately OUT = CLAMP. The plateau time is set by a resistor from TRC to Vcc and a capacitor to COM as:

*Tp = RC*ln((R-7.6k)/(R-12.4k)).*

TRC also programs a blanking time during which the chip ignores the desaturation comparator. The blanking time is:

*Tb = Tp + 0.4*RC.*

In the event that desaturation is detected outside the blanking interval, OUT will be driven back to the CLAMP plateau for a fault time set by a resistor from FRC to Vcc and a capacitor to COM as:

*Tf = RC*ln((R-7.6k)/(R-12.4k)).*

If the event is transient, OUT will return fully high at the end of Tf as shown in figure 5. During Tf, FRPLY is open. After Tf, FRPLY is shorted to COM.

Desaturation shown in figure 6 that persists longer than Tf will cause OUT to be driven fully low. The chip will not accept a command to drive OUT high for a delay period of

*Td = 0.4*RC*

FRPLY will be open during this entire period.

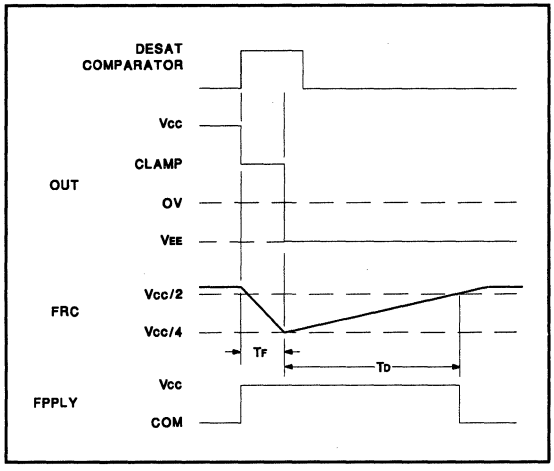


Figure 6. Rising Edge Waveform

ENABLE

$\overline{\text{ENBL}}$ provides an alternate means of controlling the output. If $\overline{\text{ENBL}}$ is to be used as the primary input, A should be connected to Vcc and B to VEE. $\overline{\text{ENBL}}$ can be driven by the output of an opto-isolator from $\overline{\text{ENBL}}$ to COM as shown in figure 7. If $\overline{\text{ENBL}}$ is not used, it should be shorted to COM.

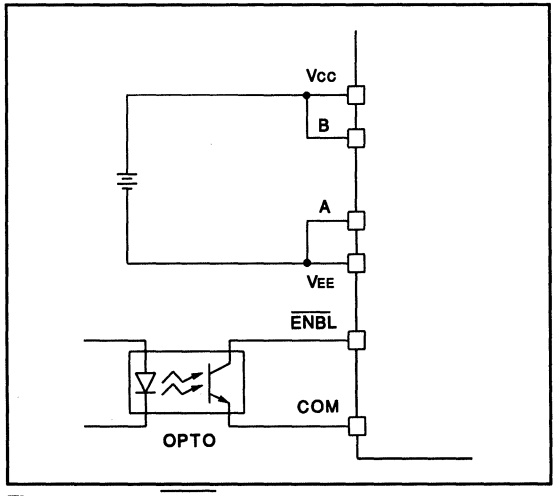


Figure 7. Using $\overline{\text{ENBL}}$ as Primary Input

EXTERNAL BIPOLAR SUPPLIES

If it is desired to drive an emitter grounded IGBT from external supplies, the configuration in figure 8 should be used. COM should never be connected to ground. Vcc must be ≥ 12V and Vcc-VEE must be ≥ 23.5V.

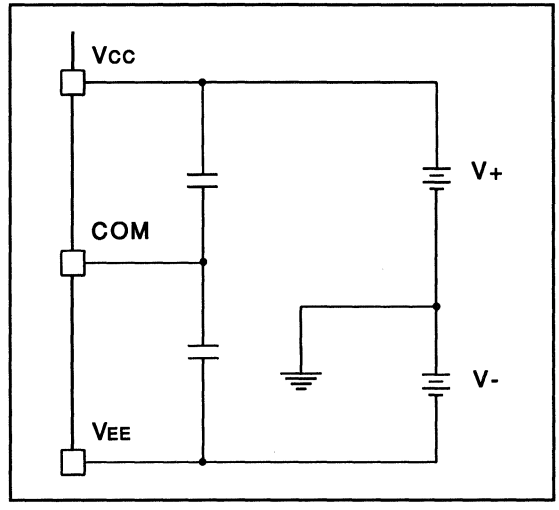


Figure 8. Using External Supplies

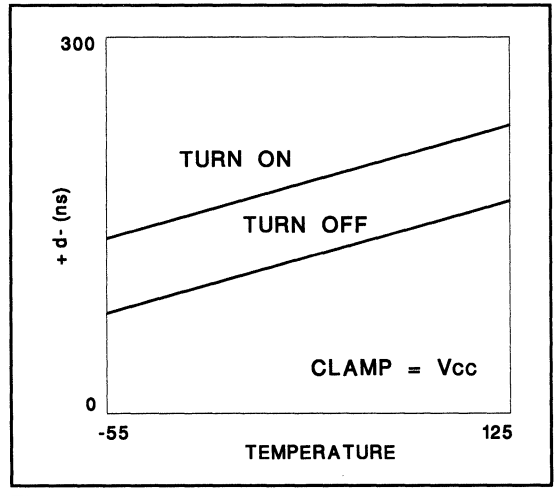


Figure 9. Input to Output Delay

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Thermal Monitor

FEATURES

- On-Chip Temperature Transducer
- Temperature Comparator Gives Threshold Temperature Alarm
- Power Reference Permits Airflow Diagnostics
- Precision 2.5V Power Reference Permits Airflow Diagnostics
- Transducer Output is Easily Scaled for Increased Sensitivity
- Low 2.5mA Quiescent Current

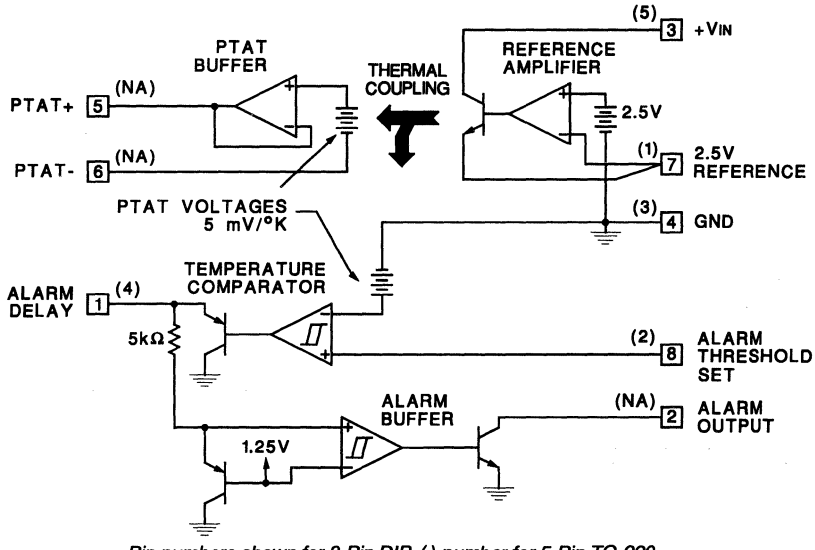
DESCRIPTION

The UC1730 family of integrated circuit devices are designed to be used in a number of thermal monitoring applications. Each IC combines a temperature transducer, precision reference, and temperature comparator allowing the device to respond with a logic output if temperatures exceed a user programmed level. The reference on these devices is capable of supplying in excess of 250mA of output current – by setting a level of power dissipation the rise in die temperature will vary with airflow past the package, allowing the IC to respond to airflow conditions

These devices come in an 8-Pin DIP, plastic or ceramic, a 5-Pin TO-220 or a PLCC-20 version. In the 8-Pin version, a PTAT (proportional to absolute temperature) output reports die temperature directly. This output is configured such that its output level can be easily scaled up with two external gain resistors. A second PTAT source is internally referenced to the temperature comparator. The other input to this comparator can then be externally programmed to set a temperature threshold. When this temperature threshold is exceeded an alarm delay output is activated. Following the activation of the delay output, a separate open collector output is turned on. The delay pin can be programmed with an external RC to provide a time separation between activation of the delay pin and the alarm pin, permitting shutdown diagnostics in applications where the open collector outputs of multiple parts are wire OR'ed together.

The 5-Pin version in the TO-220 package is well suited for monitoring heatsink temperatures. Enhanced airflow sensitivities can be obtained with this package by mounting the device to a small heatsink in the airstream. This version of the device does not include the PTAT output or the open collector alarm output.

BLOCK DIAGRAM



Pin numbers shown for 8-Pin DIP, ( ) number for 5-Pin TO-220.

5/93

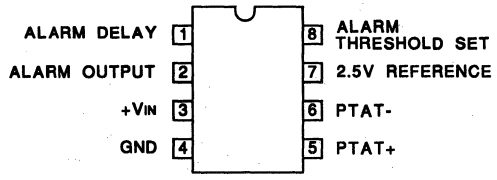
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN) 40V
Alarm Output Voltage (8-Pin Version Only) 40V
Alarm Delay Voltage 10V
Alarm Threshold Set Voltage 10V
2.5V Reference Output Current ..... -400 mA
Alarm Output Current (8-Pin Version Only) ..... 0 mA
Power Dissipation at TA = 25°C (Note 2) ..... 1000 mW
Power Dissipation at TC = 25°C (Note 2) ..... 2000 mW
Thermal Resistance Junction to Ambient
N, 8-Pin Plastic DIP ..... 110°C/W
J, 8-Pin Ceramic DIP ..... 110°C/W
T, 5-Pin Plastic DIP TO-220 ..... 65°C/W
Thermal Resistance Junction to Case
N, 8-Pin Plastic DIP ..... 60°C/W
J, 8-Pin Ceramic DIP ..... 40°C/W
T, 5-Pin Plastic TO-220 ..... 5°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

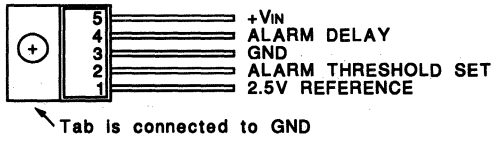
Note 1: Voltages are referenced to ground. Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

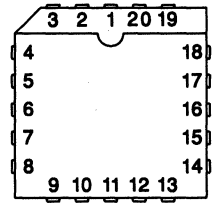
DIL-8 (TOP VIEW)
N or J Package



5-PIN TO-220 (TOP VIEW)
T Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1-3
ALARM DELAY	4
ALARM OUTPUT	5
+VIN	6
GND	7
N/C	8-13
PTAT+	14
PTAT-	15
2.5V REFERENCE	16
2.5V REFERENCE	17
ALARM THRESHOLD SET	18
N/C	19-20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TJ = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, +VIN = + 5V, and PTAT– = 0V. TA = TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	+VIN = 35V		2.8	4.0	mA
	+VIN = 5V		2.3	3.5	mA
REFERENCE					
Output Voltage	TJ = 25°C	2.475	2.5	2.525	V
	Over Temperature	2.46		2.54	V
Load Regulation	IOUT = 0 to 250mA		8.0	25	mV
Line Regulation	+VIN = 5 to 25V		1.0	5.0	mV
TEMPERATURE COMPARATOR					
Temperature Comparator Threshold	at 300°K (26.85°C), Nominally 5mV/°K, VINPUT High to Low	1.475	1.50	1.525	V
Temperature Error		-10		10	°C
Threshold Line Regulation	+VIN = 5 to 25V		0.005	0.02	%/V
Temperature Linearity	Note 2		2.0	5.0	°C
Threshold Hysteresis		3.0	8.0	15	mV
Input Bias Current	VINPUT at 1.5V	-0.5	-0.1		µA
Max Output Current	VOUT = 1V	1.2	3.0		mA
Output Sat Voltage	IOUT = 100µA		0.05	0.25	V

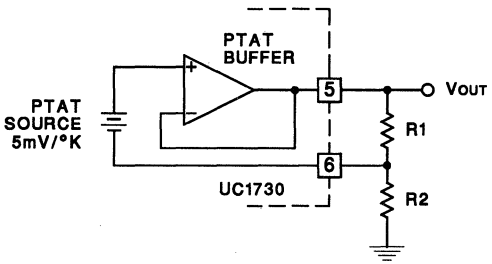
ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications apply for T_J = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, +V_{IN} = + 5V, and PTAT– = 0V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE COMPARATOR (cont.)					
Output Leakage Current	V_{OUT} = 1V		0.01	1.0	µA
PTAT BUFFER (8-Pin N, or J Version Only)					
Output Voltage	at 300°K (26.85°C), Nominally 5mV/°K	1.460	1.50	1.54	V
	In 10X Config. + V_{IN} = 25V	14.6	15	15.4	V
Temperature Error		-12		12	°C
Temperature Linearity (Note 2)			2.0	5.0	°C
Line Regulation	+V_{IN} = 5 to 25V		0.02	0.04	%/V
Load Regulation	I_{OUT} = 0 to 2mA		1.0	3.0	mV
Dropout Voltage	PTAT + TO +V_{IN}		1.9	2.5	V
Input Bias Current at PTAT– Input		-3.0	-1.0		µA
ALARM BUFFER COMPARATOR (8-Pin N, or J Version Only)					
Threshold Voltage (V_{TH})	Alarm Delay Input Low to High	1.1	1.2	1.3	V
Threshold Hysteresis Voltage	Alarm Delay Voltage > V_{TH}		100	250	mV
Input Bias Current	Alarm Delay Voltage < V_{TH}		0.1	0.5	µA
Max Output Current	V_{OUT} = 1V	7.0	15		mA
Output Sat Voltage	I_{OUT} = 3mA		0.25	0.45	V
Output Leakage	V_{OUT} = 35V		0.1	2.0	µA

Note 2: This parameter is guaranteed by design and is not tested in production.

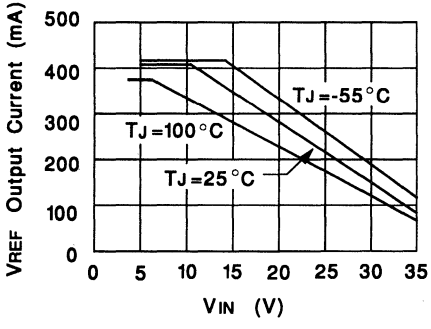
APPLICATIONS AND OPERATION INFORMATION

Scaling the PTAT Output (8 Pin Version Only)

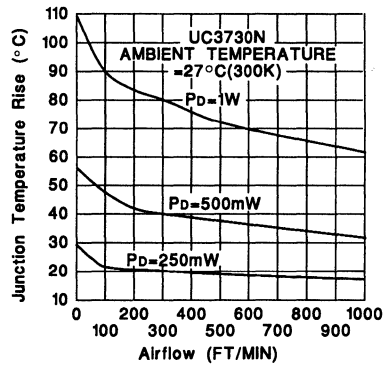


$$V_{OUT} = 5 \times \left(1 + \frac{R2}{R1}\right) mV/°K$$

(Recommended Range for R1 is 2k to 4k)



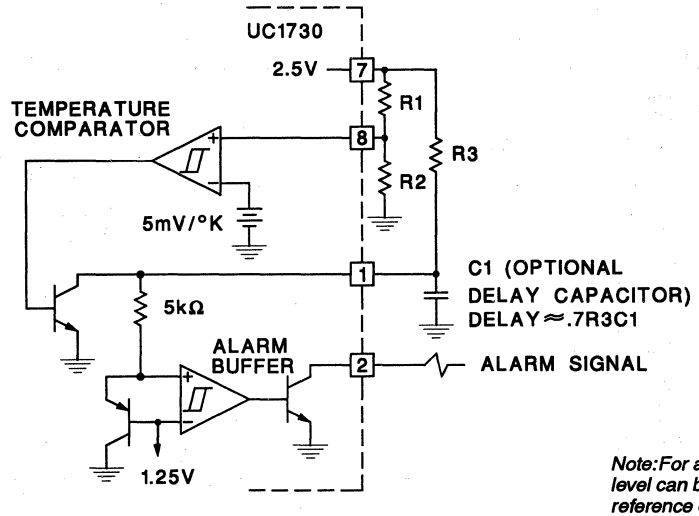
V_{REF} Maximum Output Current vs Input Supply



Junction Temperature Rise vs Airflow UC3730N (8-Pin Plastic Dip)

APPLICATIONS AND OPERATION INFORMATION (Cont.)

Setting a Temperature Threshold

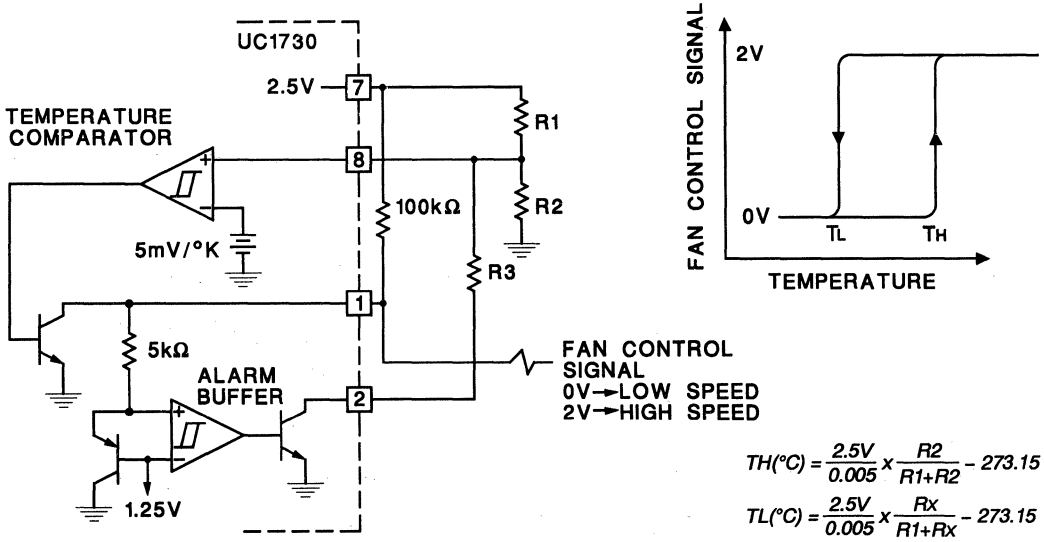


Temperature Threshold (°C)

$$= \left(\frac{2.5V}{0.005}\right) x \frac{R2}{R1+R2} - 273.15$$

Note: For airflow monitoring a power dissipation level can be set with a resistive load, R_L, on the reference output. $P_D = (+ V_{IN} - 2.5V)^2/R_L$.

Dual Speed Fan Control



$$TH(°C) = \frac{2.5V}{0.005} x \frac{R2}{R1+R2} - 273.15$$

$$TL(°C) = \frac{2.5V}{0.005} x \frac{Rx}{R1+Rx} - 273.15$$

$$\text{Where: } RX = R2 \times \frac{R3}{R2+R3}$$

UNITRODE INTEGRATED CIRCUITS
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TEL. (603) 424-2410 • FAX (603) 424-3460

Half-Bridge Bipolar Switch

FEATURES

- Source or Sink 4.0A
- Supply Voltage to 35V
- High-Current Output Diodes
- Tri-State Operation
- TTL and CMOS Input Compatibility
- Thermal Shutdown Protection
- 300kHz Operation
- Low-Cost TO-220 Package

DESCRIPTION

This device is a monolithic integrated circuit designed to provide high-current switching with low saturation voltages when activated by low-level logic signals. Source and sink switches may be independently activated without regard to timing as a built-in interlock will keep the sink off if the source is on.

This driver has the high current capability to drive large capacitive loads with fast rise and fall times; but with high-speed internal flyback diodes, it is also ideal for inductive loads. Two UC2950s can be used together to form a full bridge, bipolar motor driver compatible with high frequency chopper current control.

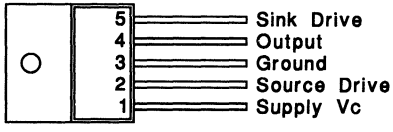
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Range, Vc	8V to 35V
Output Voltage Range, Vo	-3.0V to Vc+3V
Input Voltage Range, VIN	-0.3V to +7.0V
Peak Output Current (100 ms, 10% DC)	±4.0A
Continuous Output Current	±2.0A
Power Dissipation with Heat Sink	15W
Power Dissipation in Free Air	2W
Operating Temperature Range, TA	-20°C to +100°C
Storage Temperature Range, Ts	-55°C to +125°C

Note 1: Consult Packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T Package

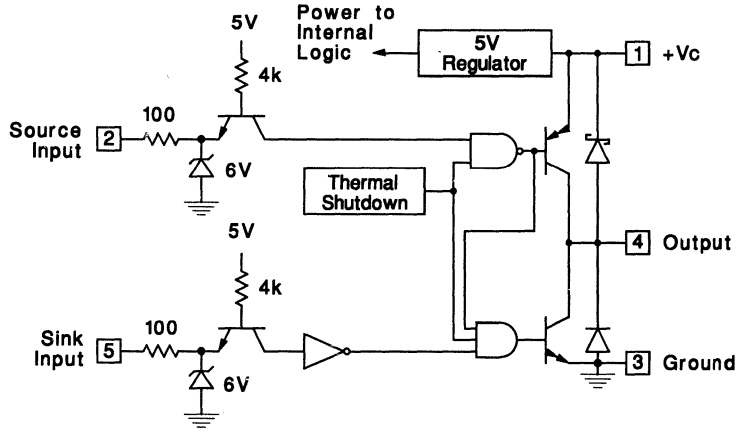


TRUTH TABLE

Source Drive Pin 2	Sink Drive Pin 5	Output Pin 4
Low	Low	Low
Low	High	Off
High	Low	High
High	High	High

Note: With no load, output voltage will be HIGH in the OFF state.

SIMPLIFIED SCHEMATIC



5/93

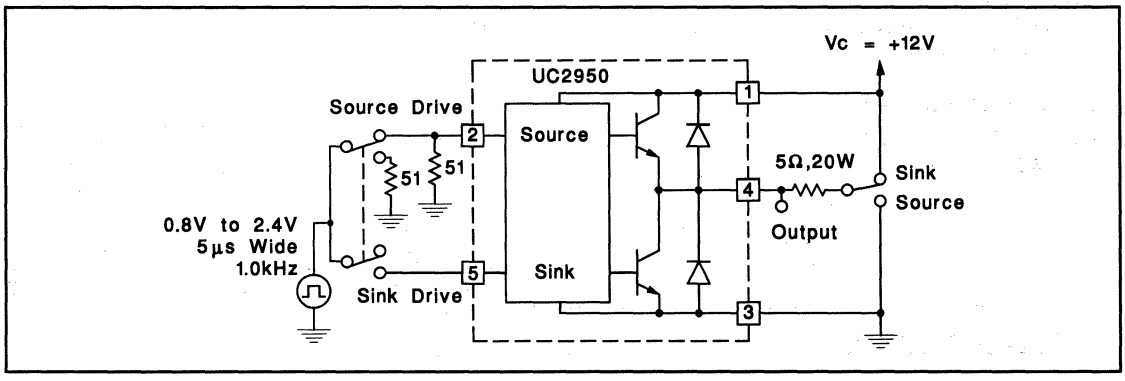
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_C = 35V, T_A = -20°C to +100°C, V_{IL} = 0.8V, V_{IH} = 2.4V for either input, T_A = T_J.

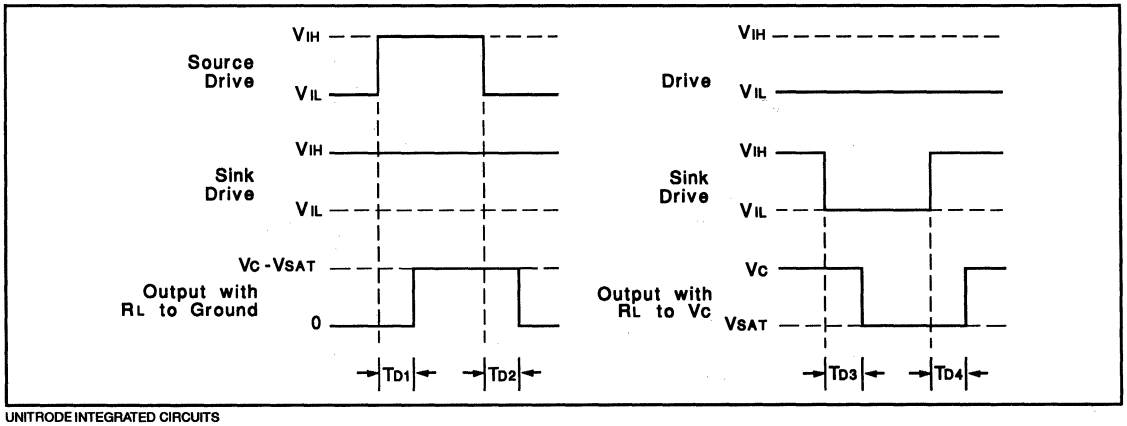
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage to V_C	Output Off		20	500	µA
Output Leakage to Ground	Output Off		-200	-500	µA
Output Sink Saturation	V_{OL}, I_L = 2.0A		1.2	2.0	V
Output Source Saturation	(V_C-V_{OL}), I_L = -2.0A		1.2	2.0	V
Sink Diode Forward Voltage	I_D = -2.0A		1.4	2.0	V
Source Diode Forward Voltage	I_D = 2.0A		1.4	2.0	V
Input Current	Either Input, V_I = 5V		20	100	µA
	Either Input, V_I = 0V		-1.0	-1.6	mA
Supply Current	Output High		20	30	mA
	Output Low		10	20	mA

SWITCHING CHARACTERISTICS: See Test Circuit. V_C = 12V, R_L = 5Ω, T_A = 25°C. Guaranteed by design, not 100% tested in production.

PARAMETERS	MIN	TYP	MAX	UNITS
Source Turn-On Delay, t_{D1}		300	500	ns
Source Turn-Off Delay, t_{D2}		1.0	2.0	µs
Sink Turn-On Delay, t_{D3}		200	400	ns
Sink Turn-Off Delay, t_{D4}		100	300	ns
Cross-Conduction Current Spike When Source and Sink are Activated Together		0.6	1.0	µs

SWITCHING TEST CIRCUIT





UNITRODE INTEGRATED CIRCUITS
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Triple Tri-State Power Driver

FEATURES

- Operating Supply Voltage to 32V
- Load Current Capability to 3A
- Built-In Thermal Protection
- Clamp Diodes Included for Driving Inductive Loads
- 25W Multiwatt® Power-Tab Package
- Individual Logic Inputs for Each Driver
- Master Inhibit Input for Power-Down and Coast
- TTL/CMOS Compatible Inputs

DESCRIPTION

The UC3657 triple power driver integrated circuit is well suited to driving three-phase motors, stepper motors, brush motors, inductors, incandescent lamps, resistive loads and long lines with controlled voltage slew rates. The UC3657 features minimum saturation voltage with light loads as well as low saturation voltage for loads in excess of 2A.

Each output contains two clamp diodes to conduct transient currents from inductive loads. The diode to Vcc is a fast, low voltage-drop Schottky type, while the diode to ground is a slower P-N junction device.

The UC3657 is completely safe from destruction due to incorrect combinations of logic inputs. For best performance, however, it is recommended that the inputs are driven with logic signals that have transition times faster than 100ns.

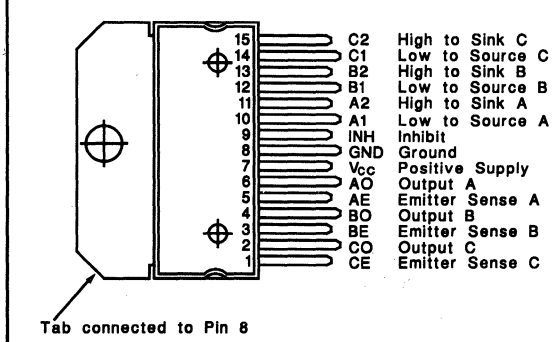
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage 35V
Logic Input Voltage ..... -0.3 to +35V
Peak Output Current (each channel)
  Non-Repetitive 100µs 3A
  Repetitive, 8ms on, 2ms off 2.5A
  Continuous 2A
Storage and Junction Temperature ..... -40°C to +150°C

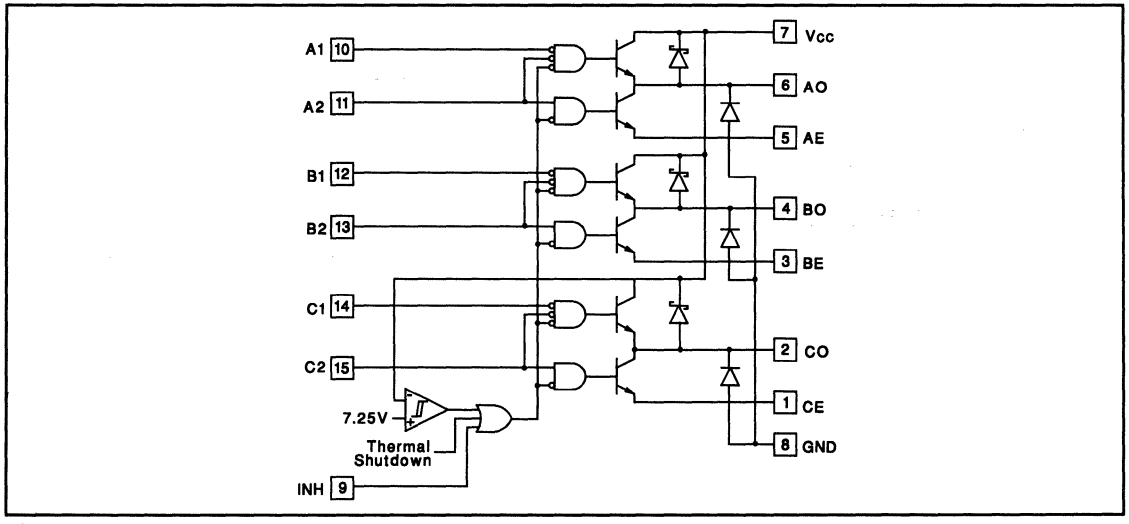
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

(TOP VIEW)



BLOCK DIAGRAM

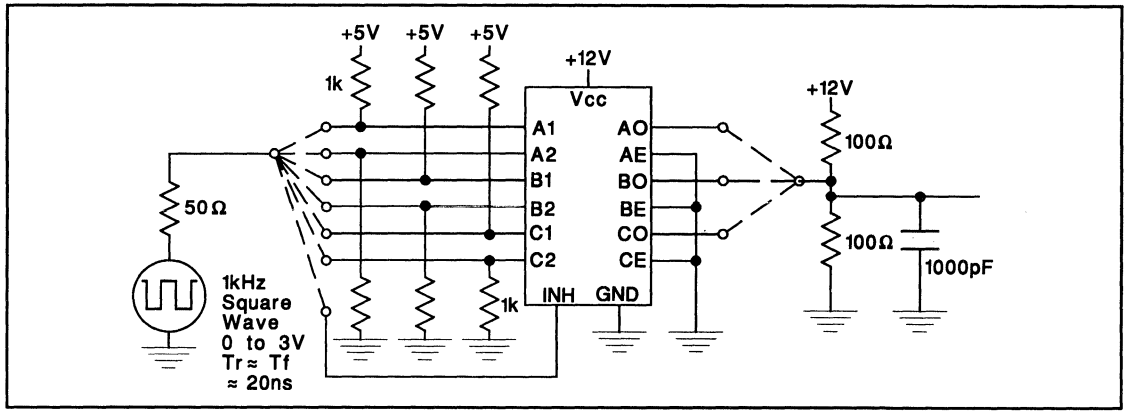


ELECTRICAL CHARACTERISTICS

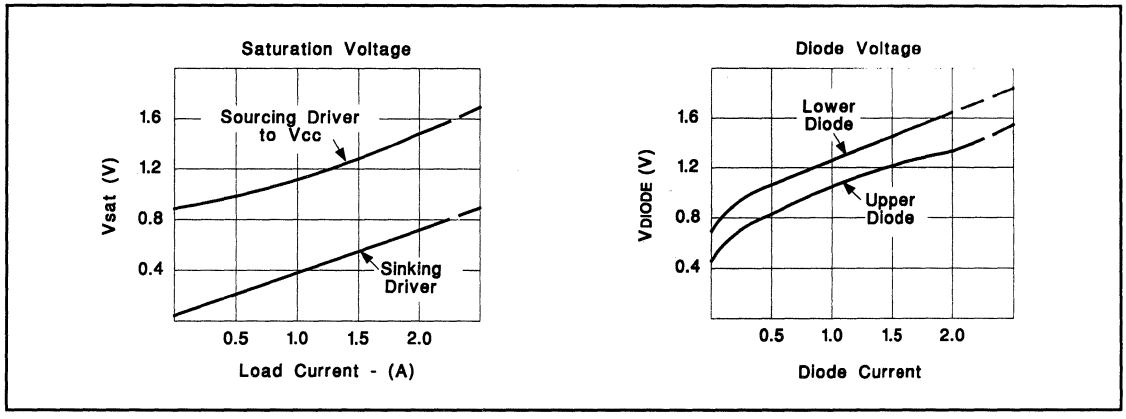
(0°C < T_A < 700°C, V_{CC} = 12V unless otherwise noted.) $T_A = T_J$

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Icc, Outputs Off	A1, B1, C1 = H A2, B2, C2 = L INH = L			10	25	mA
Icc, Outputs High	A1, B1, C1 = L A2, B2, C2 = L INH = L			10	28	mA
Icc, Outputs Low	A1, B1, C1, = L A2, B2, C2 = H INH = L			40	70	mA
Icc, Chip Inhibited	INH = H			0.5	5	mA
Icc, One Output Low 2A	A2, B2, C2 = H INH = L			100		mA
Vcc Range, Operating			8		32	V
Turn-On Threshold				7.5	8	V
Turn-Off Threshold				7.0		V
Thermal Shutdown Temperature				170		°C
Thermal Recovery Temperature				160		°C
Logic Input Threshold			0.8		2.0	V
Input Low Current; A1, A2, B1, B2, C1, C2	at 0.0V			4	20	µA
Inhibit Low Current, INH	at 0.0V				20	µA
Input High Current; A1, A2, B1, B2, C1, C2	at 3.0V				10	µA
Inhibit High Current; INH	at 3.0V			0.2	1	mA
Output Low Voltage	A2, B2, C2 = H INH = L	100mA		.07	.12	V
	AE, BE, CE Grounded	1A		.37	.75	V
		2A		.7	1.25	V
Output High Voltage, to Vcc	A1, B1, C1 = L INH = L	100mA		-.9	-1.3	V
	A2, B2, C2 = L	1A		-1.2	-1.5	V
		2A		-1.5	-1.9	V
Propagation Delay, Off-High	Test Circuit, Drive A1, B1, or C1			.1		µs
Propagation Delay, Off-Low	Test Circuit, Drive A2, B2, or C2			3.2		µs
Propagation Delay, High-Low	Test Circuit, Drive A1 + A2, B1 + B2, or C1 + C2			.25		ms
Propagation Delay, Low-High	Test Circuit, Drive A1 + A2, B1 + B2, or C1 + C2			.51		µs
Propagation Delay, High-Off	Test Circuit, Drive A1, B1, or C1			.4		µs
Propagation Delay, Low-Off	Test Circuit, Drive A2, B2, or C2			.35		µs
Propagation Delay, Low-Inhibit	Test Circuit, Drive INH			1.5		µs
Propagation Delay, Inhibit-Low	Test Circuit, Drive INH			.6		µs
Propagation Delay, High-Inhibit	Test Circuit, Drive INH			2.5		µs
Propagation Delay, Inhibit-High	Test Circuit, Drive INH			.5		µs
Output Slew Rate, Output Rising	100Ω Load to GND; Drive A1 + A2, B1 + B2, or C1 + C2			50		V/µs
Output Slew Rate, Output Falling	100Ω Load to Vcc; Drive A1 + A2, B1 + B2, or C1 + C2			50		V/µs
Output Leakage Current	INH = H, Vcc = 32V, 0V < 32V		-250		250	µA
High-Side Diode 2A Drop	INH = H			1.3	2	V
Low-Side Diode 2A Drop	INH = H			1.6	3	V

PROPAGATION DELAY TEST CIRCUIT (Connect only one channel at a time.)



TYPICAL CHARACTERISTICS, 25°C, 12V

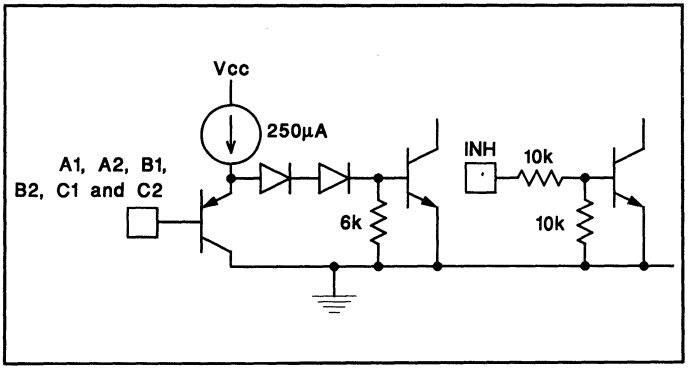


LOGIC TRUTH TABLE

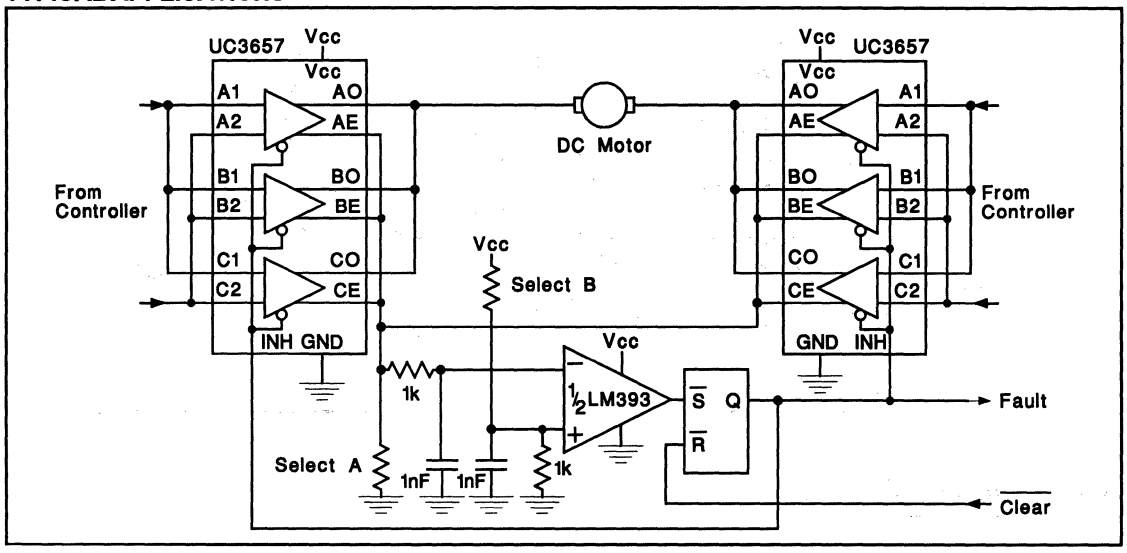
Input 1	Input 2	INH	Output
X	X	H	Off
H	L	X	Off
L	L	L	High
X	H	L	Low

L means input voltage < 0.8V.
H means input voltage > 2.0V.
Off means output is high impedance.
Low means output is low impedance to "E."
High means output is low impedance to "Vcc."
X means input voltage will not affect the output (don't care).

EQUIVALENT INPUT CIRCUIT



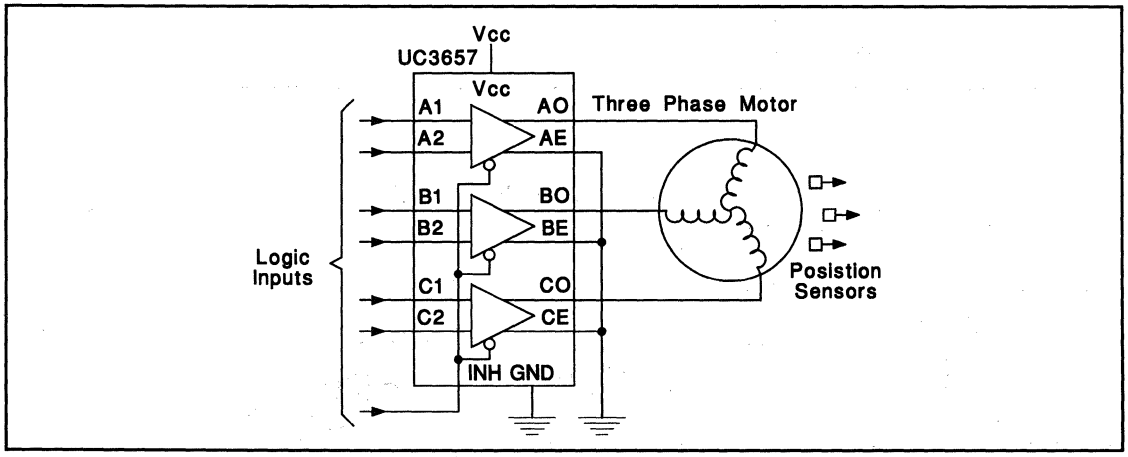
TYPICAL APPLICATIONS



This application features a fault latch to detect a shorted wire, stuck rotor, or other problem that can cause current to exceed some threshold. A single sense resistor is used with a voltage comparator to detect this fault. Emitter resistor "A" is used to sense total low-side current, and inhibit all devices in the event that current exceeds a threshold. Resistor "B" sets the comparator threshold, and a set-reset flip-flop latches the error signal to prevent oscillation. Matched RC filters on the comparator inputs allow operation close to threshold with good supply-noise rejection.

To achieve high currents, UC3657 outputs have been paralleled. This is practical within the device current and power ratings, according to the derating specification for the package.

BRUSHLESS MOTOR DRIVER



UNITRODE INTEGRATED CIRCUITS
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Bridge Transducer Switch

FEATURES

- Dual Matched Current Sources
- High-gain Differential Sensing Circuit
- Wide Common-mode Input Capability
- Complementary Digital Open-collector Outputs
- Externally Programmable Time Delay
- Optional Output Latch with Reset
- Built-in Diagnostic Activation
- Wide Supply Voltage Range
- High Current Heater Power Source Driver

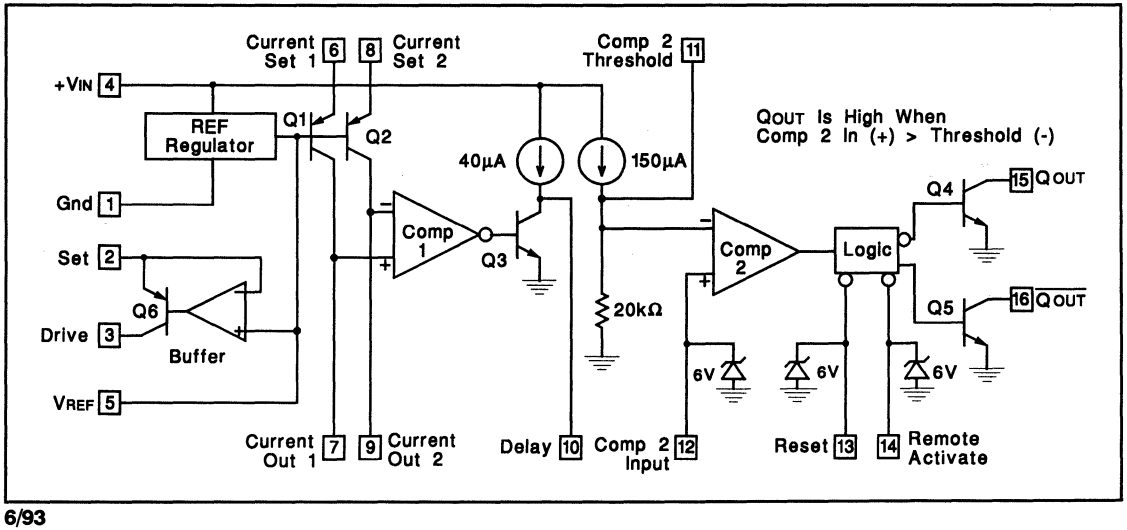
DESCRIPTION

This integrated circuit contains a complete signal conditioning system to interface low-level variable impedance transducers to a digital system. A pair of matched, temperature-compensated current sources are provided for balanced transducer excitation followed by a precision, high-gain comparator. The output of this comparator can be delayed by a user-selectable duration, after which a second comparator will switch complementary outputs separately activated for diagnostic operation and has an optional latch with external reset capability. An added feature is a high current power source useful as a heater driver in differential temperature sensing applications. The UC3704 is designed for 0°C to +70°C environments.

UC3704 COMPATIBLE SENSORS

SENSOR TYPE	ACTIVATION SOURCE						
	Temperature	Pressure	Force	Position	Displacement	Velocity	Shock
Thermistor	X					X	
Sensistor	X					X	
Thermocouple	X						
Semiconductor	X	X	X				
Photo Voltaic				X	X	X	
Photo Resistive				X	X	X	
Strain Gage		X	X	X	X	X	X
Piezoelectric		X	X		X	X	X
Magneto Resistive				X	X		
Inductive				X	X	X	X
Hall Effect				X	X		
Capacitive							X

BLOCK DIAGRAM



6/93

7

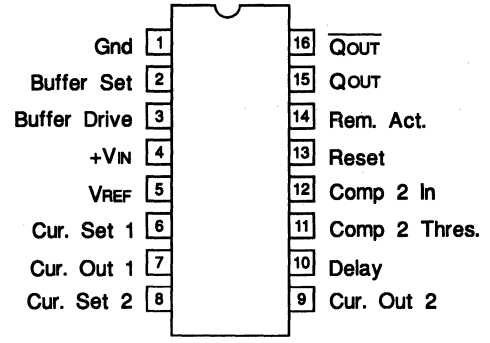
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V_{IN}) 40V
Output Current (each output) ..... 50 mA
Buffer Power Source Current 200mA
Comparator 1 Inputs ..... -0.5V to V_{REF}
Comparator 2 Inputs ..... 0 to 5.5V
Remote Activation and Reset Inputs ..... 0 to 5.5V
Power Dissipation at T_A = 25°C 1000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note: Unless otherwise specified, all voltages are with respect to ground (Pin 1).
Currents are positive into, negative out of the specified terminal.
Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704: V_{IH} = 15V, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Inputs					
Supply Voltage Range		4.2		36	V
Supply Current	V_{IN} = 36V		5	10	mA
Reference Section (with respect to V_{IN})					
V_{REF} Value $\|V_{IN} - V_{REF}\|$	T_J = 25°C	2.1	2.2	2.3	V
V_{REF} Temperature Coefficient	Note 1	-1	-2	-3	mV/°C
Line Regulation	ΔV_{IN} = 4.2 to 25V		2	10	mV
Load Regulation	ΔI_O = 0 to 4mA		2	10	mV
Short Circuit Current	V_{IN} = 36V, V_{REF} = V_{IN} or Ground			±25	mA
Current Source (Q1 and Q2)					
Output Current (Note 2)	Current Set = 10µA	-9	-9.5	-10	µA
	Current Set = 200µA	-180	-195	-200	µA
Output Offset Current	R_{E6} = R_{E8} = 20kΩ		0	±1	µA
Comparator One					
Input Offset Voltage			±1	±4	mV
Input Bias Current			-100	-300	nA
Input Offset Current				±60	nA
CMRR	V_{CM} = 0 to 12V	60	70		dB
Voltage gain	R_L>150kΩ	70	85		dB
Delay Current Source		34	40	52	µA
Output Rise Time	Overdrive = 10mV, C_D = 15pF, T_J = 20°C		2		V/µs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704: V_{IH} = 15V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Comparator Two (Q_{OUT} and $\overline{Q_{OUT}}$)						
Threshold Voltage			2.2	3.0	3.8	V
Threshold Resistance	To Ground		14	20	24	kΩ
Input Bias Current	V_{IN} (Pin 12) = 5V			1	3	µA
Remote Activate Current	Pin 14 = 0V			0.2	0.5	mA
Reset Current	Pin 13 = 0V			0.2	0.5	mA
Remote Activate Threshold	T_A = 25°C		0.8	1.2		V
Reset Threshold	T_A = 25°C		0.8	1.2		V
Output Saturation	I_{OUT} = 16mA			0.2	0.5	V
	I_{OUT} = 50mA			0.7	2.0	V
Output Leakage	V_{OUT} = 40V			0.2	10	µA
Output Response	Comp. Overdrive = 1V, R_L = 5k to V_{IN}	Turn-on		0.4		µs
		Turn-off		1.0		µs
Buffer						
Set Voltage (V_{IN} -Vs)	T_J = 25°C, Is = 100mA		1.9	2.1	2.3	V
Drive Current	T_J = 25°C, Rs = 200Ω, V_D = 0V		90	100	120	mA

Note 1: Parameter guaranteed by design, not tested in production.

Note 2: Collector output current $= \frac{V_{IN} - V_{REF} - V_{BE}}{R_E} \approx \frac{1.5V}{R_E}$

APPLICATIONS INFORMATION

Sensor Section

The input portion of the UC3704 provides both excitation and sensing for a low-level, variable impedance transducer. This circuitry consists of a pair of highly matched PNP transistors biased for operation as constant current sources followed by a high gain precision comparator.

The reference voltage at the bases of the PNP transistors has a TC to offset the base-emitter voltage variation of these transistors resulting in a constant voltage across the external emitter resistors and correspondingly constant collector currents for balancing, offsetting, or to provide unique temperature characteristic.

With the PNP transistor's optimum current ranging from 10 to 200µA, and the common-mode input voltage of the comparator usable from ground to (V_{IN} - 3V), a wide range of transducer impedance levels is possible.

The sensor comparator has a current source pull-up at the output so that an external capacitor from this point to ground can be used to provide a programmable delay before reaching the second comparator's threshold. The low-impedance on-state of Comp 1's output provides quick reset of this capacitor. This programmable delay function is useful for providing transient protection by requiring that Comp 1 remain activated for a finite period of time before Comp 2 triggers. Another application is in counting repetitive pulses where a missing pulse will allow Comp 1's output to rise to Comp 2's threshold. This time delay function is:

$$Delay = \frac{Comp\ 2\ Threshold}{Delay\ Current} \times C_D \approx 175ms/\mu F$$

If hysteresis is desired for Comparator 1, it may be accommodated by applying positive feedback from the delay terminal to the non-inverting input on Pin 7. This will aid in providing oscillation-free transitions for very slowly changing inputs.

APPLICATIONS INFORMATION (cont.)

Output Section

The output portion of the UC3704 is basically a second comparator with complimentary, open-collector outputs. This comparator has a built-in, ground-referenced threshold implemented with a high-impedance current source and resistor so that it may be easily overridden with an external voltage source if desired. Comp 2's input transistors are NPN types which require at least 1V of common-mode voltage for accurate operation and should not see a differential input voltage greater than 6V.

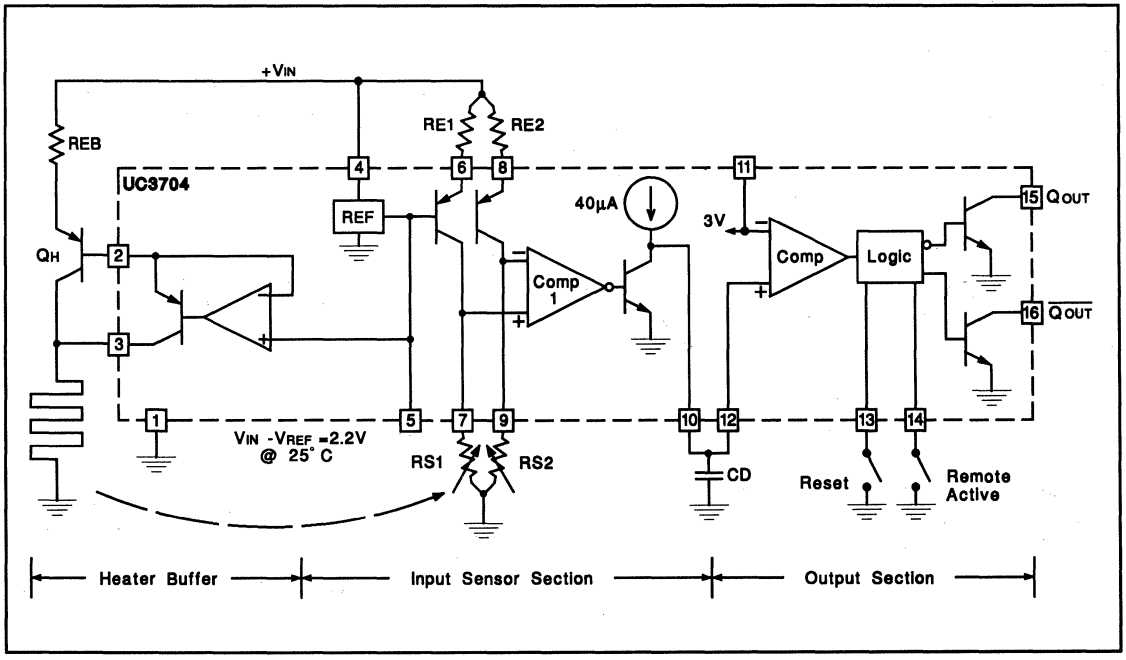
For diagnostic or latching purposes, the output logic is equipped with a Remote Activate and Reset function. These pins have internal pull-ups and are only active when pulled low below a threshold of approximately 1V. A low signal at the Remote Activate Pin causes the outputs to change state in exactly the same manner as if Comp 2's input is raised above the threshold on Pin 11. If Pin 16 is connected to Pin 14, positive feedback results and the outputs will latch once triggered by Comp 2's input. Pulling the Reset terminal low overrides the Remote Activate Pin releasing the latch.

Reference Buffer

This circuit is designed to provide up to 100mA to drive a high current external PNP transistor useful for powering a heater for differential temperature measurements. Care must be taken that power dissipation in Q6 does not cause excessive thermal gradients which will degrade the accuracy of the sensing circuitry.

Using a heating element attached to a temperature sensitive resistor, RS1, in one leg of the input bridge implements a flow sensor for either gasses or liquids. As long as there is flow, heat from the element is carried away and the sensor voltage remains below threshold. Using an identical sensor, RS2, without a heater to establish this threshold compensates for the ambient temperature of the flow.

TYPICAL APPLICATION FOR MONITORING LIQUID OR GAS FLOW



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Octal Line Driver

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards EIA232E/V.28, EIA423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection

DESCRIPTION

The UC5170C is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all eight drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is easily accomplished by taking the select pins (Ms+ and Ms-) to ground for low output mode (EIA232E/V.28 and EIA423A/V.10) or to their respective supplies for high mode (EIA232E/V.28). High mode should only by used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . -15V
PLCC Power Dissipation, T_A = 25°C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) . . . . . 1250 mW
Input Voltage . . . . . -1.5V to +7V
Output Voltage . . . . . -12V to +12V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . -65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of packages.

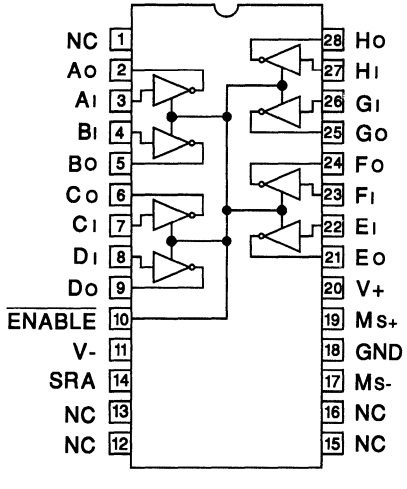
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
		HIGH	LOW
$\overline{EN}$	DATA	EIA-232E(2)	EIA423A+EIA232E
0	0	(V+)-3V	5V to 6V
0	1	(V-)-3V	-5V to -6V
1	X	High Z	High Z

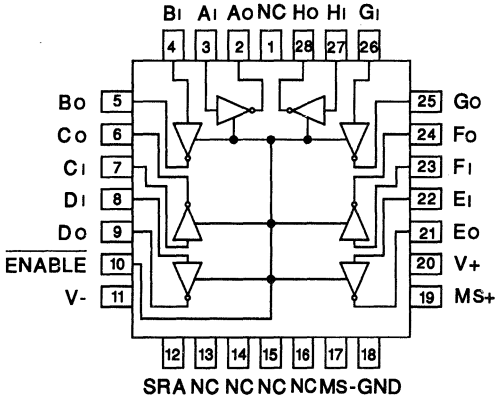
Note 2: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



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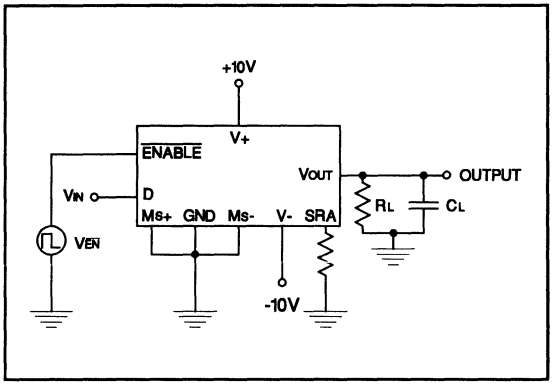
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $R_{SRA} = +10k$, $T_A = T_J$.

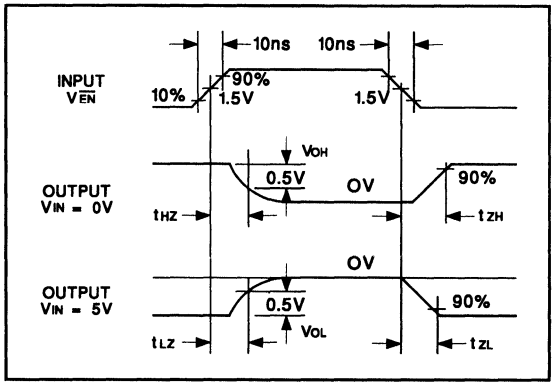
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			9		15	V
V- Range			-9		-15	V
V+ Supply Current	I_+	R_L = Infinite $\overline{En}$ = 0V		25	42	mA
V- Supply Current	I_-	R_L = Infinite $\overline{En}$ = 0V		-23	-42	mA
INPUTS						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA		-1.1	-1.8	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	-200	-8.0		µA
OUTPUTS						
High Level (Low Mode) Output Voltage (EIA423A/V.10, EIA232E/V.28)	V_{OH}	V_{IN} = 0.8V R_L = Inf.	5.0	5.3	6.0	V
		$\overline{En}$ = 0.8V R_L = 3k	5.0	5.3	6.0	V
		R_L = 450	4.5	5.2	6.0	V
Low Level (Low Mode) Output Voltage (EIA423A/V.10,EIA232E/V.28)	V_{OL}	V_{IN} = 2.0V R_L = Inf.	-5.0	-5.3	-6.0	V
		$\overline{En}$ = 0.8V R_L = 3k	-5.0	-5.3	-6.0	V
		R_L = 450	-4.5	-5.2	-6.0	V
Output Balance (EIA423A/V.10)	V_{BAL}	R_L = 450 $V_{OH} - V_{OL} = V_{BAL}$		0.2	0.4	V
High Level (High Mode) Output Voltage (EIA232E/V.28)	V_{OH}	V_{IN} = 0.8V R_L = Inf., M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
		$\overline{En}$ = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
Low Level (High Mode) Output Voltage (EIA232E, V.28)	V_{OL}	V_{IN} = 2.0V R_L = Inf., M_{S+} = V+, M_{S-} =V-	-7.0	-7.7	-10	V
		En = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	-7.0	-7.7	-10	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, V+ = 15V, V- = -15V	-100		100	µA
Short-Circuit Current	I_{OS}	V_{IN} = 0V, $\overline{En}$ = 0V	25	50		mA
		V_{IN} = 5V, $\overline{En}$ = 0V	25	40		mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $T_A = T_J$.

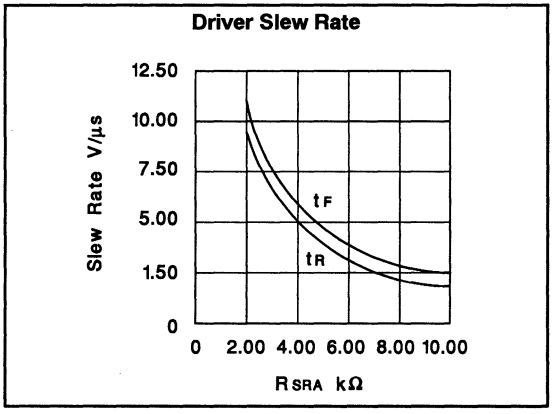
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to High Impedance	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to Output	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

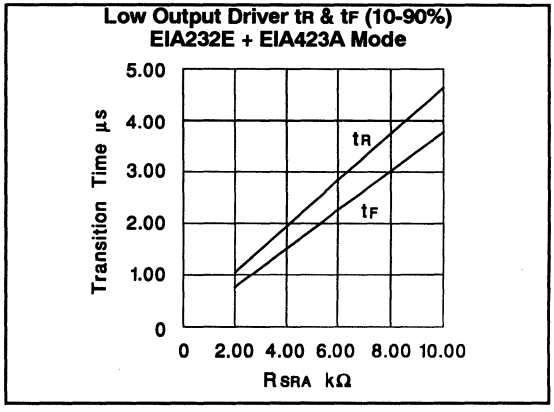
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATION INFORMATION

Slew Rate Programming

Slew rate for the UC5170C is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \; (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10k which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA423A +V.10. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

Output Voltage Programming

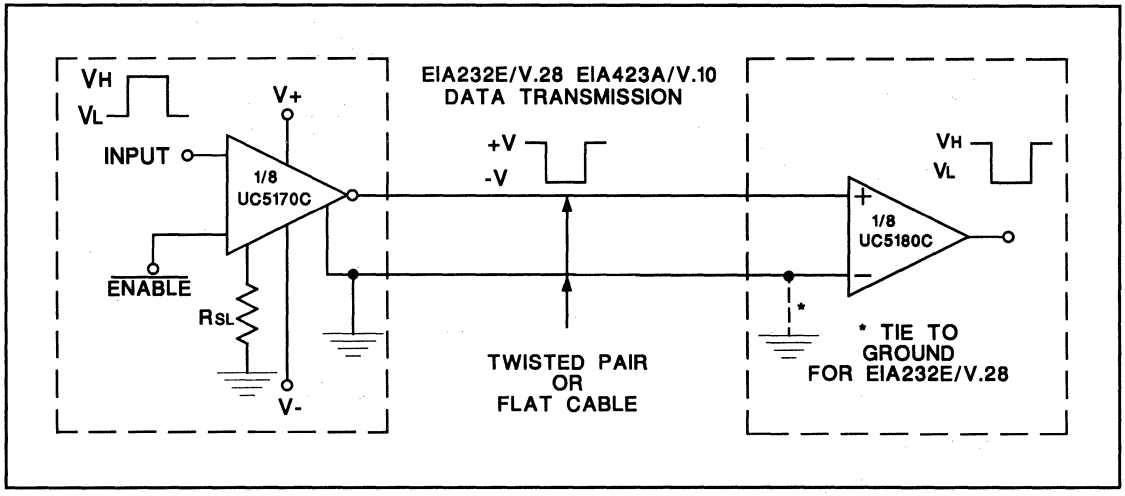
The UC5170C has two programmable output modes, either a low voltage mode which meets EIA423A, EIA232E/V.28/V.10 specifications, or the high output mode which meets the EIA232E, V.28 specifications.

The high output mode provides greater output swings, minimum of 3V below and supply rails for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supplies, Ms+ to V+ and Ms- to V-.

The low output mode provides a controlled output swing and is accomplished by connecting both mode select pins to ground.

7

APPLICATIONS



SPECIFIC LAYOUT NOTES

The UC5170C layout must have bulk bypassing close to the UC5170C, peak slew currents when all 8 drivers slew at once in the same direction is over 500mA. Some applications mount the UC5170C on a bulkhead, or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used the -10 volt supply has gone below 8.5 volts causing the slew rate control circuit to become unstable.

The UC5170C mode control leads must be kept short to prevent the chip from oscillating.

Power Sequence issue, if the +10 volts is applied before the -10 volts, the output will oscillate at 100kHz. This is a problem with some terminal designs where the +10 volts was derived from the power supply and the -10 volts was developed off of the flyback, a 500 millisec difference.

GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,00 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5170C is P6KEIOCA.

*Transzorb is a trademark of General Semiconductor Industries.

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Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Digital Selection of High Mode EIA232E/CCITT V.28 only, and Low Mode EIA232E/V.28 & EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins

DESCRIPTION

The UC5171 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is accomplished by the select pin Ms logic "low" for low output mode (EIA232E/V.28 & EIA423A/V.10) or pin Ms logic "high" for high mode (EIA232E/V.28). High mode should only be used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) ..... -15V
PLCC Power Dissipation, T_A = 25°C (Note 2) ..... 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) ..... 1250 mW
Input Voltage ..... -1.5V to +7V
Output Voltage ..... -12V to +12V
Slew Rate Resistor ..... 2k to 10kΩ
Storage Temperature ..... -65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

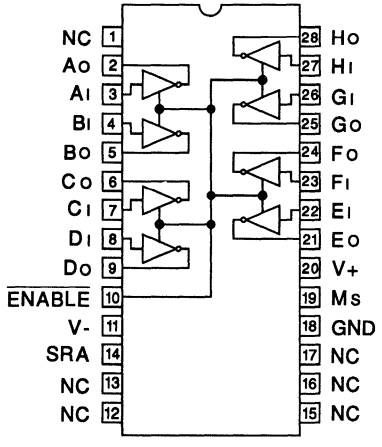
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
$\overline{EN}$	DATA	EIA-232E(3)	EIA-232E/EIA-423A
0	0	(V+)-3V	5V to 6V
0	1	(V-)+3V	-5V to -6V
1	X	High Z	High Z

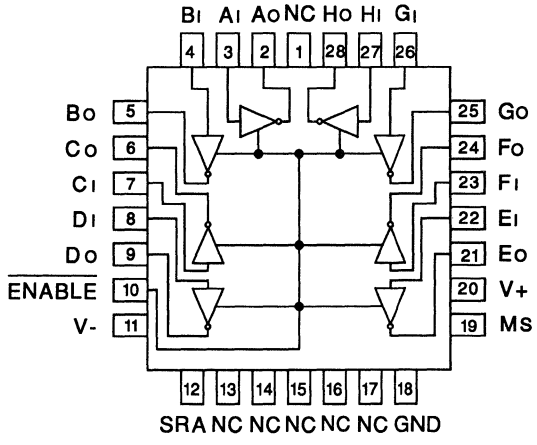
Note 3: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



6/93

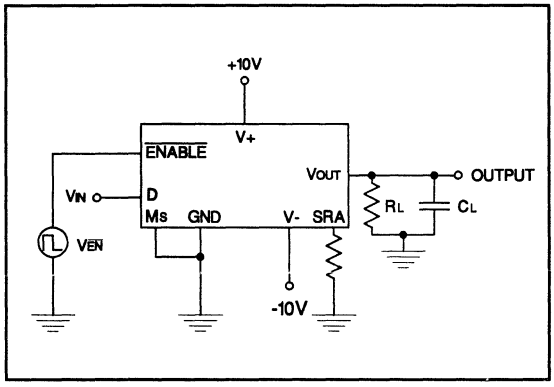
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = +10V$, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $R_{SRA} = +10k$, $T_A = T_J$.

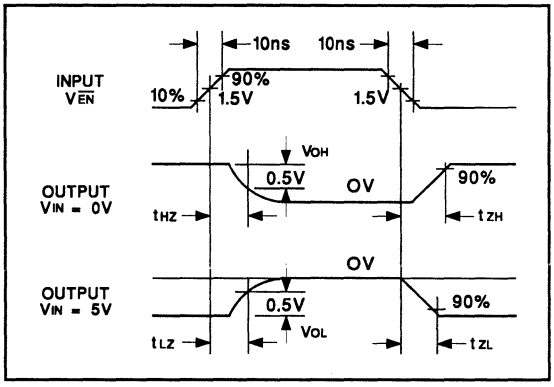
PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-9		-15	V
V+ Supply Current	I+	R_L = Infinite $\overline{En}$ = 0V			25	42	mA
V- Supply Current	I-	R_L = Infinite $\overline{En}$ = 0V			-23	-42	mA
INPUTS							
High Level Input Voltage	V_{IH}			2.0			V
Low Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA			-1.1	-1.8	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V			0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-200	-8.0		µA
OUTPUTS							
High Level	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA423A)			R_L = 450	4.5	5.2	6.0	V
Low Level	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-5.0	-5.3	-6.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-5.0	-5.3	-6.0	V
(EIA423A)			R_L = 450	-4.5	-5.2	-6.0	V
Output Balance (EIA423A)	V_{BAL}	R_L = 450	$V_{OH} + V_{OL} = V_{BAL}$		0.2	0.4	V
High Level	V_{OH}	V_{IN} = 0.8V, M_S = 2.0V	R_L = Inf.	7.0	7.6	10	V
Output Voltage (EIA232E)		$\overline{En}$ = 0.8V	R_L = 3k	7.0	7.6	10	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V, M_S = 2.0V	R_L = Inf.	-7.0	-7.7	-10	V
(EIA232E)		En = 0.8V	R_L = 3k	-7.0	-7.7	-10	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, Vo = ±6V, M_S = 2.0V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	50		mA
			V_{IN} = 5V	25	40		mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-|$ = +10V, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $T_A = T_J$.

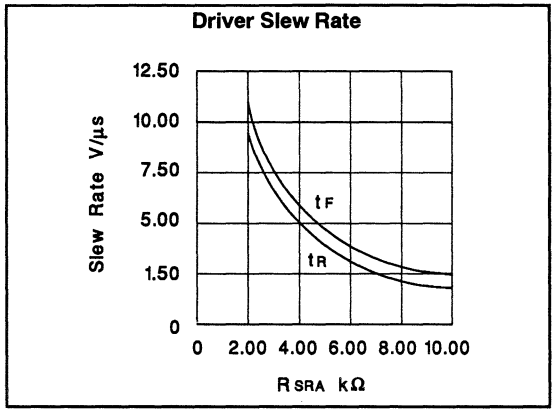
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
High Impedance	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
Output	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

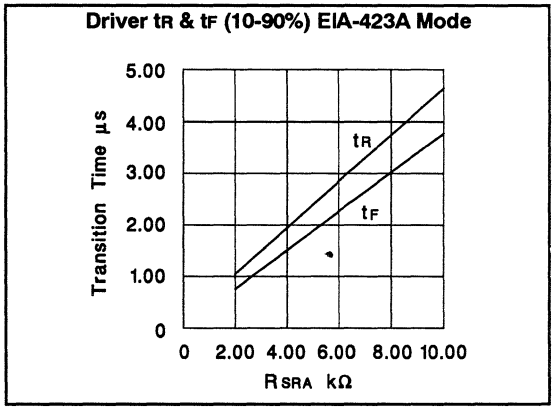
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5171 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \; (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate=300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet)=100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

Output Voltage Programming

The UC5171 has two programmable output modes, either a low voltage mode which meets EIA-423A operational specifications, or the high output voltage mode which meets the EIA-232E specifications.

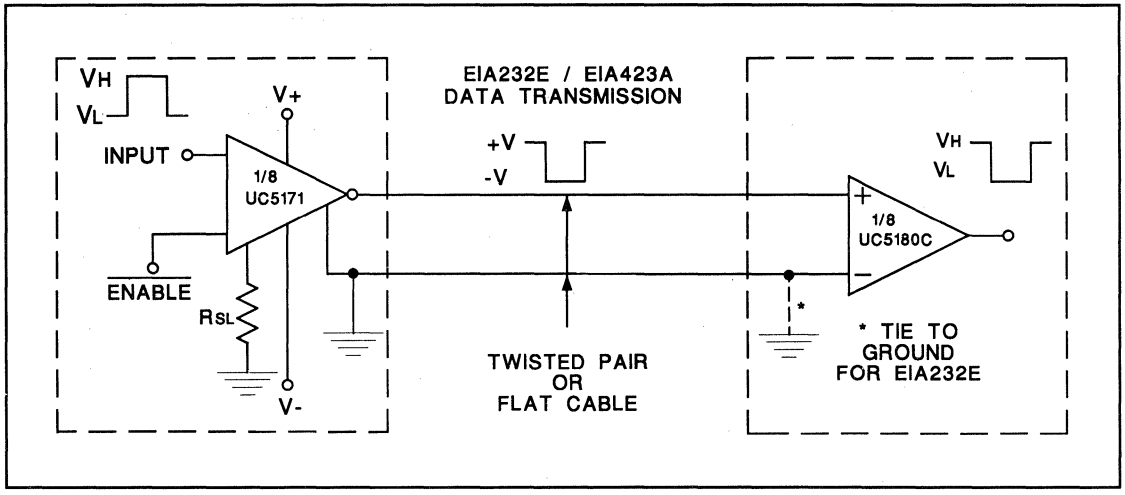
The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the modes select pin, (Ms), to a TTL "low" level. The low output mode provides a controlled output swing and is accomplished by connecting the mode select pin, (Ms), to a TTL "low level."

EIA Standards

The UC5171 meets or exceeds the EIA Standards for EIA-232E and EIA-423A modes of operation except under power down conditions. When powered down with the output attached to an active buss, the UC5171 has the potential to load the bus under transient conditions.

7

APPLICATIONS



UC5171 Specific Layout Notes

The UC5171 layout must have bulk bypassing close to the UC5171, peak slew currents when all 8 drivers slew at once in the same direction is over 500mA. Some applications mount the UC5171 on a bulkhead, or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used the -10 volt supply has gone below 8.5 volts causing the slew rate control circuit to become unstable.

Power sequence issue, if the +10 volts is applied before the -10 volts the output will oscillate at 100kHz. This is a problem with some terminal designs where the +10 volts was derived from the power supply and the -10 volts was developed off of the flyback, a 500 millisec difference.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal-to-metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5171 is P6KEIOCA

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Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Meets Standards EIA232E/CCITT V.28, and EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins
- EOS on all Output Pins 35V under all Output Conditions
- High Current Output for Long Line Drive, Exceeds Standards

DESCRIPTION

The UC5172 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels are independent of the power variations.

The UC5172 has high output current, and current balance for long line drive applications. EOS - Output parasitic SCRs powered on and off are 35V, well above signal levels, allowing protection devices to work.

Inputs are compatible TTL+MOS logic families and are diode protected against negative transients.

FUNCTIONAL TABLE

INPUTS		OUTPUT
$\overline{EN}$	DATA	EIA232E/EIA423A
0	0	5V to 6V
0	1	-5V to -6V
1	X	High Z

Note 2: Minimum output swings.

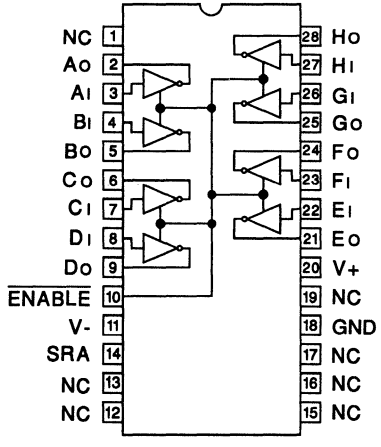
ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) ..... -15V
PLCC Power Dissipation, T_A=25°C (Note 3) ..... 1000 mW
DIP Power Dissipation, T_A=25°C (Note 3) ..... 1250 mW
Input Voltage ..... -1.5V to +7V
Output Voltage ..... -6V to +6V
Slew Rate Resistor ..... 2k to 10kΩ
Storage Temperature ..... -65°C to +150°C

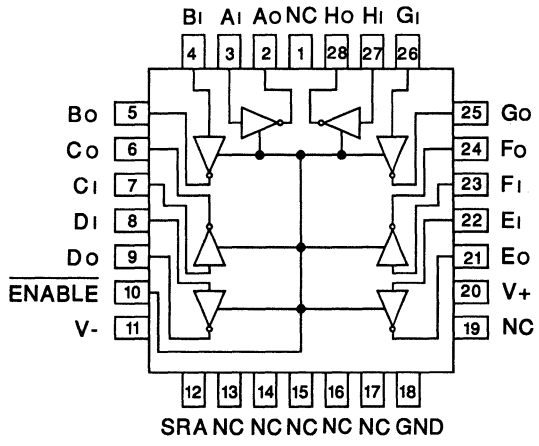
Note 1: All voltages are with respect to ground, pin 18.
Note 3: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



6/93

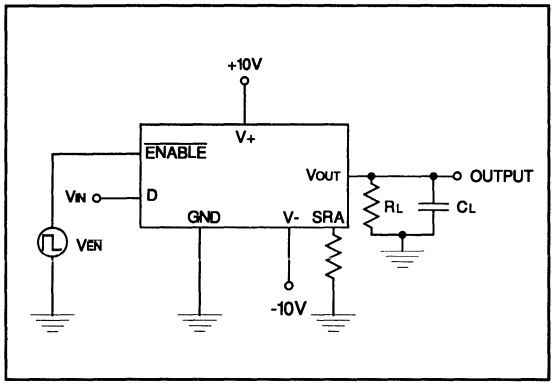
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0°C < T_A < +70°C$, $R_{SRA} = +10k$, $T_A = T_J$.

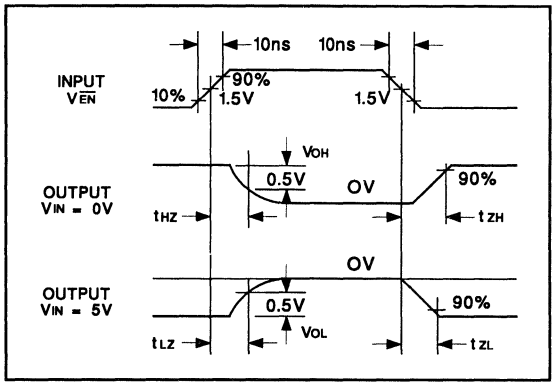
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-9		-15	V
V+ Supply Current	I+	R_L = Infinite $\overline{En}$ = 0V			15	25	mA
V- Supply Current	I-	R_L = Infinite $\overline{En}$ = 0V			-17	-25	mA
INPUTS							
High-Level Input Voltage	V_{IH}			2.0			V
Low-Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA			-1.1	-18	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		-2	0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-5	-8.0		
OUTPUTS							
High Level Output Voltage	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA-423A)			R_L = 450	4.5	5.2	6.0	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-5.0	-5.3	-6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-5.0	-5.6	-6.0	V
(EIA-423A)			R_L = 450	-4.5	-5.4	-6.0	V
Output Balance (EIA-423A)	V_{BAL}	R_L = 450, $V_{OH} - V_{OL} = V_{BAL}$			0.2	0.4	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, V+ = 15V, V– = -15V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	65		mA
			V_{IN} = 5V	25	70		mA
Power Off Output Current	I_{PO}	V_O = ±6V, V+ = V– = 0V		-100		100	mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-| = +10V$, $0°C < T_A < +70°C$, $T_A = T_J$.

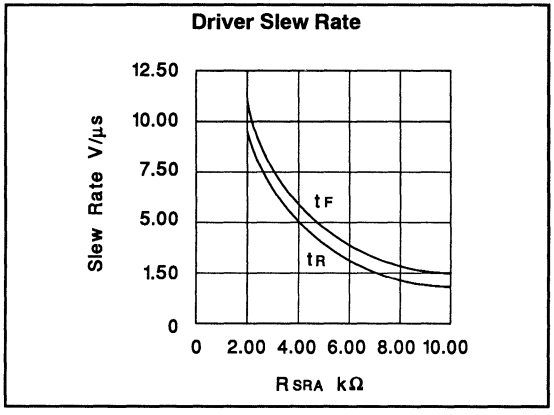
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	7.6	8.5	9.4	V/µs
	t_F	R_L = 450, C_L = 50pF	7.6	8.5	9.4	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.5	1.7	1.9	Vµs
	t_F	R_L = 450, C_L = 50pF	1.5	1.7	1.9	V/µs
Propagation Output to High Impedance	t_{HZ}	R_{SRA} = 10k		0.8	2.0	µs
	t_{LZ}	R_L = 450, C_L = 50pF		0.5	2.0	µs
Propagation High Impedance to Output	t_{ZH}	R_{SRA} = 10k		2.0	7.0	ms
	t_{ZL}	R_L = 450, C_L = 50pF		1.0	7.0	µs

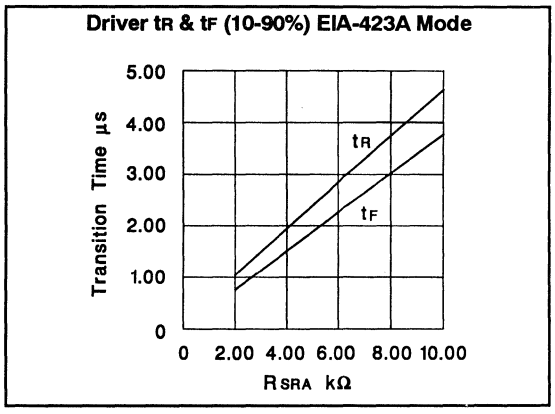
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





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APPLICATIONS

Slew Rate Programming

Slew rate for the UC5172 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \text{ (RSRA in k}\Omega\text{)}$$

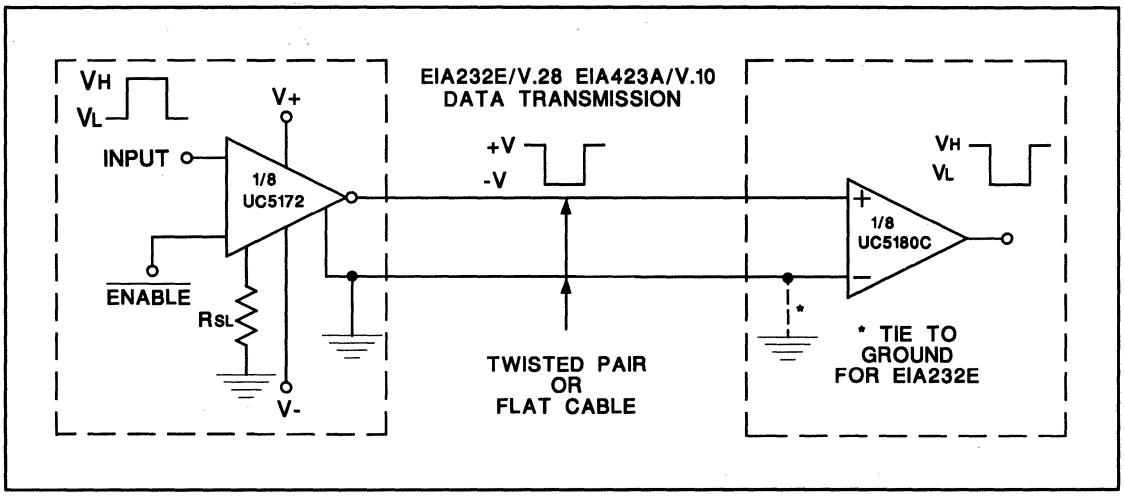
The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)
Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

APPLICATIONS



Specific Layout Notes

The UC5172 layout must have bulk bypassing close to the UC5172; peak slew currents when all 8 drivers slew at once in the same direction is over 500mA. Some applications mount the UC5172 on a bulkhead, or isolated place for RFI/FCC/VDE reasons. If bulk bypassing is not used the -10 volt supply has gone below 8.5 volts causing the slew rate control circuit to become unstable.

Power Sequence issue, if the +10 volts is applied before the -10 volts the output will oscillate at 100kHz. This is a problem with some terminal designs where the +10 volts was derived from the power supply and the -10 volts was developed off of the flyback, a 500 millisec difference.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5172 is P6KE10CA.

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Octal Line Receiver

FEATURES

- Meets EIA 232E/423A/422A and CCITT V.10,V.11, V.28, X.26, X.27
- Single +5V Supply--TTL Compatible Outputs
- Differential Inputs Withstand ± 25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current--35 mA Max
- Input Noise Filter
- Internal Hysteresis

DESCRIPTION

The UC5180C are octal line receivers designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA423A, EIA422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180C includes an input noise filter and is intended for applications employing data rates up to 200 KBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

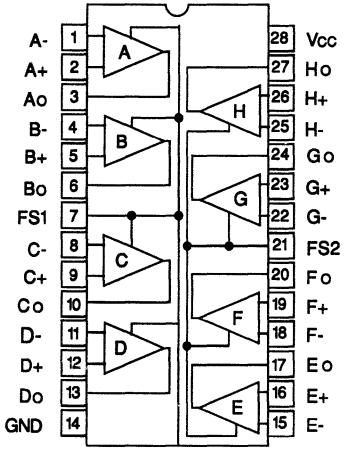
Supply Voltage, Vcc	7V
Output Sink Current	50 mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to Vcc
PLCC Power Dissipation, T_A = 25°C (Note 2)	1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2)	1200 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	-300°C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive into, negative out of the specified terminal

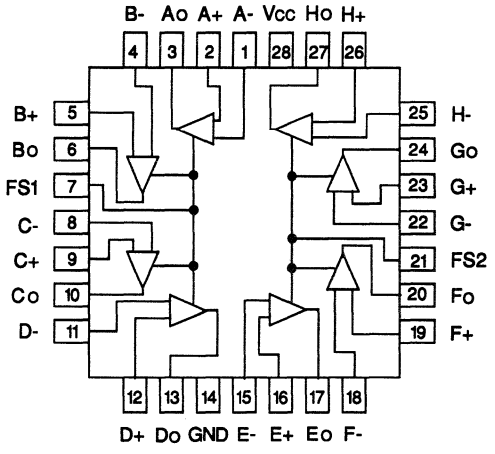
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



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DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, Input Common Mode Range ± 7V, T_A = T_J

PARAMETERS	SYMBOL	TEST CONDITIONS		UC5180C MIN	UC5180C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ | V_{IN} | ≤ 25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0 ≤ I_{OUT} ≤ 8mA, $V_{FAILSAFE}$ = 0V		0.45	V
			0 ≥ I_{OUT} ≥ - 400 µA, $V_{FAILSAFE}$ = V_{CC}	2.7		
Differential Input High Threshold	V_{TH}	V_{OUT} = 2.7V, I_{OUT} = 440 µA (See Figure 1)	R_S = 0 (Note 2)	50	200	mV
			R_S = 500 (Note 2)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 440 mA (See Figure 1)	R_S = 0 (Note 2)	-200	-50	mV
			R_S = 500 (Note 2)	-400		
Hysteresis	V_H	F_S = 0V or Vcc (See Figure 1)		50	140	mV
Open Circuit Input Voltage	V_{ICC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{CH}	V_{ID} = 1V, I_{OUT} = - 440µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 3)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 4		20	100	mA
Supply Current	I_{CC}	4.75V ≤ V_{CC} ≤ 5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IN} = -10V	-3.25		

Note 2: Rs is a resistor in series with each input.
Note 3: Measured after 100ms warm up (at 0°C)
Note 4: Only 1 output may be shorted at one time and then only for a maximum of 1 sec.

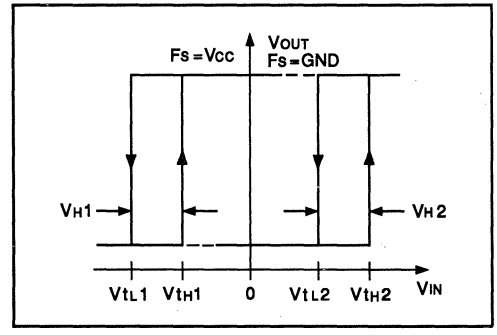


Figure 1. VtL, VtH, VH Definition

AC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C, Figure 2, T_A = T_J.

PARAMETERS	SYMBOL	TEST CONDITIONS	UC5180C MIN	UC5180C MAX	UNITS
Propagation Delay - Low to High	t_{PLH}	C_L = 50pH, V_{IN} = ± 500mV		550	ns
Propagation Delay - High to Low	t_{PHL}	C_L = 50pH, V_{IN} = ± 500mV		550	ns
Acceptance Input Frequency	f_A	Unused Input Grounded, V_{IN} = ± 200mV		0.1	MHz
Rejectable Input Frequency	f_R	Unused Input Grounded, V_{IN} = ± 500mV	5.5		MHz

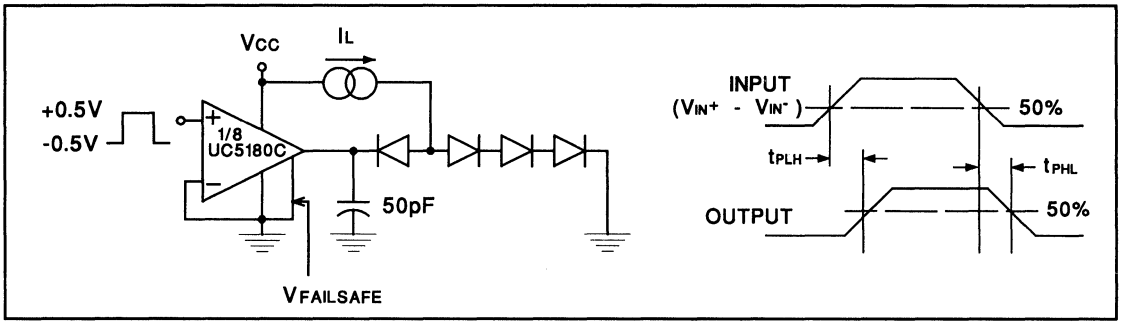


Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

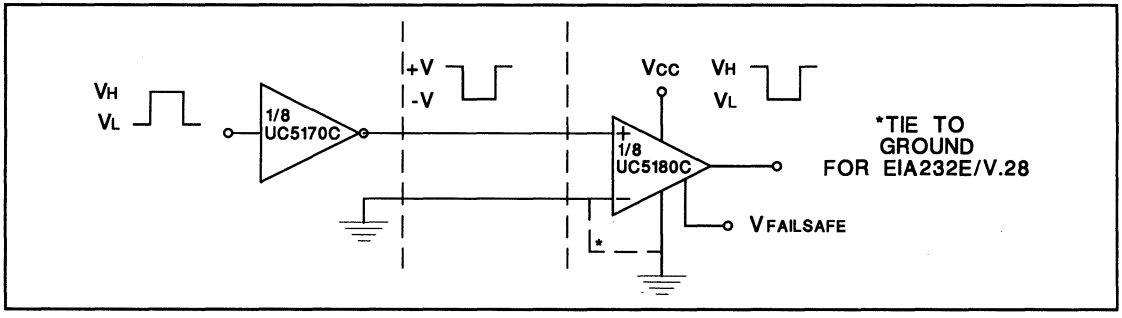
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) drive in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to Vcc or ground. A connection to Vcc provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5180C where each provides common failsafe control for four receivers.

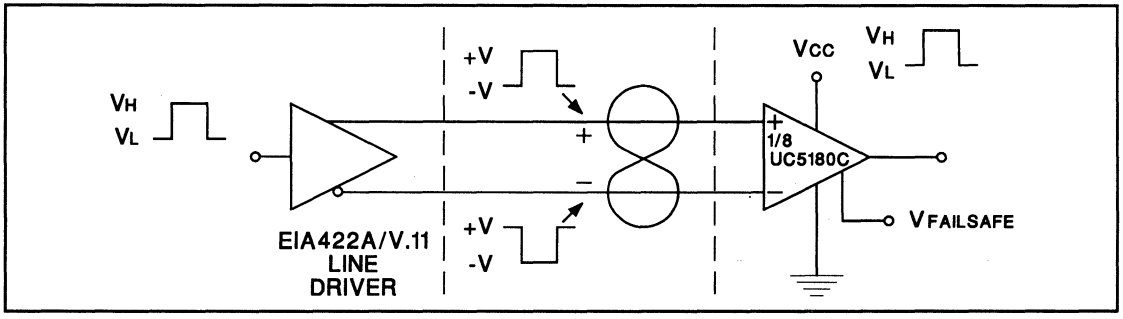
Input Filtering (UC5180C)

The UC5180C has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no charge of state occurs at the output.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



UNITRODE INTEGRATED CIRCUITS
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Octal Line Receiver

FEATURES

- Meets EIA232E/423A/422A and CCITT V.10, V.11, V.28, X.26, X.27
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35mA Max
- Internal Hysteresis

DESCRIPTION

The UC5181C are octal line receivers designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA422A, EIA423A and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5181C is similar to the UC5180C, but without the input filtering. Thus, it covers the entire range of data rates up to 10MBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

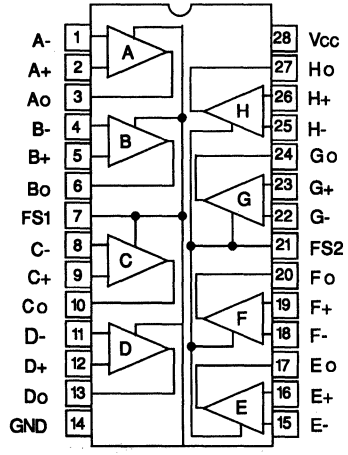
Supply Voltage, Vcc 7V
Output Sink Current 50mA
Output Short Circuit Time ..... 1 Sec
Common Mode Input Range 15V
Differential Input Range 25V
Failsafe Voltage ..... -0.3 to Vcc
PLCC Power Dissipation, T_A=25° C (Note 2) ..... 1000 mW
DIP Power Dissipation, T_A=25° C (Note 2) ..... 1200 mW
Storage Temperature Range ..... -65° C to +150° C
Lead Temperature (Soldering, 10 seconds) ..... -300° C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive in, negative out of the specified terminal.

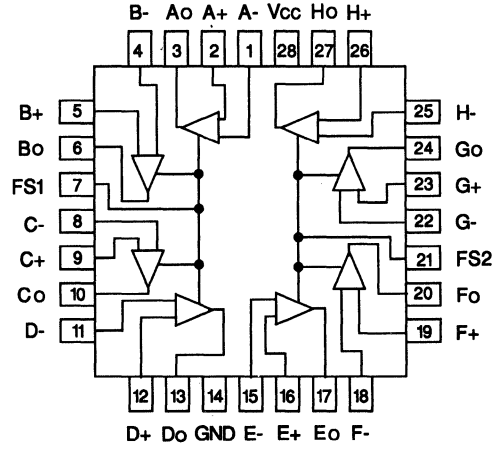
Note 2: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V, T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS		UC5181C MIN	UC5181C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ |V_{IN}|≤25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0≥I_{OUT}≥8mA $V_{FAILSAFE}$=0V		0.45	V
			0≥I_{OUT}≥-400µA, $V_{FAILSAFE}$=V_{CC}	2.7		
Differential Input High Threshold	V_{TL}	V_{OUT}= 0.45V, I_{OUT} = -440µA (See Figure 1)	R_S = 0 (Note3)	50	200	mV
			R_S = 500 (Note 3)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 3)	-200	-50	mV
			R_S = 500 (Note 3)	-400		
Hysteresis	V_H	F_S=0V or V_{CC} (See Figure 1)		45	140	mV
Open Circuit Input Voltage	V_{IOC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, I_{OUT} = -440 µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 4)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 5		20	100	mA
Supply current	I_{CC}	4.75V ≤V_{CC}≤5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IH} = -10V	-3.25		

Note 3: Rs is a resistor in series with each input.
Note 4: Measure after 100 ms warm up (at 0°C).
Note 5: Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
Note 6: The delays, either t_{PLH} or t_{PHL}, shall not vary from receiver to receiver by more than 35ns.

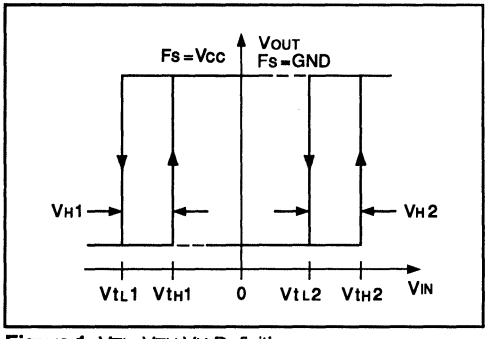


Figure 1. VTL, VTH,VH Definition

AC ELECTRICAL CHARACTERISTICS:

V_{CC}=5V ±5%. T_A=0°C to +70°C, Figure 2 T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS	UC5181C MIN	UC5181C MAX	UNITS
Propagation Delay–Low to High	t_{PLH}	C_L=50 pH, V_{IN}= ±500 mV (Note 6)		120	ns
Propagation Delay–High to Low	t_{PHL}	C_L=50 pH, V_{IN}= ±500 mV (Note 6)		120	ns
Acceptable Input frequency	f_A	Unused Input Grounded, V_{IN}= ±200 mV		5.0	MHz

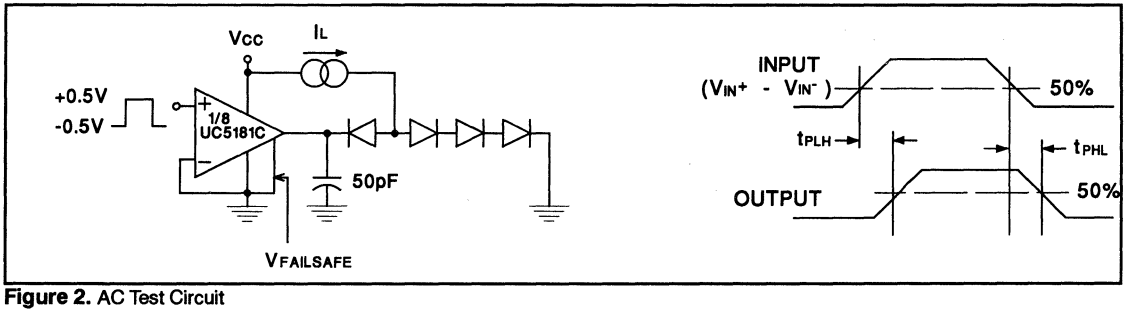


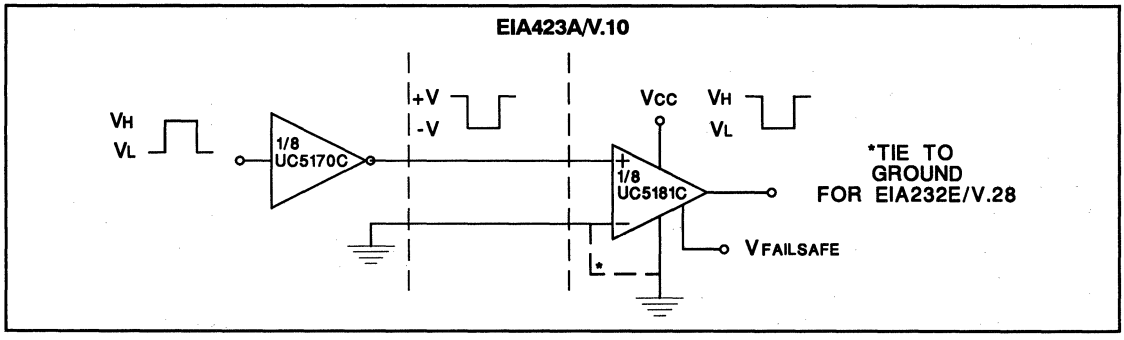
Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

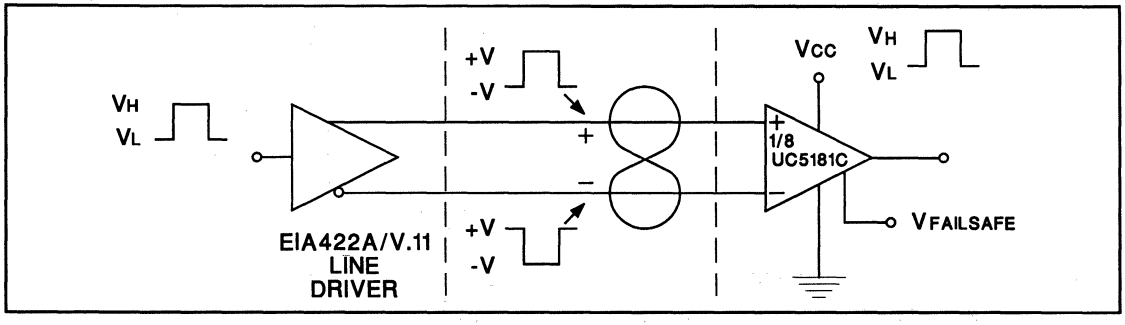
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to Vcc or ground. A connection to Vcc provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5181C where each provides common failsafe control for four receivers.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, and protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5180C and the UC5181C is P6KE22CA.

* Transzorb is a trademark of General Semiconductor Industries..

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SCSI Active Terminator

FEATURES

- Fully monolithic IC solution
- Complies with SCSI and SCSI-2 standards
- Provides active termination for 18 lines
- Logic command disconnects all terminating resistors
- Low supply current in disconnect mode
- Negative clamping on all signal lines
- Trimmed regulator for accurate termination current
- Current limit and thermal shutdown protection
- Low dropout voltage regulator
- Low thermal resistance surface mount packages

DESCRIPTION

The UC5601 provides precision resistive pull-up to a 2.9V reference for all 18 lines in a Small Computer Systems Interface (SCSI) bus cable. The SCSI-2 standard recommends active termination at both ends of every cable segment utilizing single ended drivers and receivers.

Internal circuit trimming is utilized, first to reduce resistor tolerances to +/– 3% and then to adjust the regulator's output voltage to insure termination current accuracy of +/– 3%.

The UC5601 provides a disconnect feature which, upon a logic command, disconnects all terminating resistors, and turns off the regulator; greatly reducing standby power.

Other features include negative clamping on all signal lines, 20mA of active negation sink current capability, regulator current limiting, and thermal shutdown protection.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

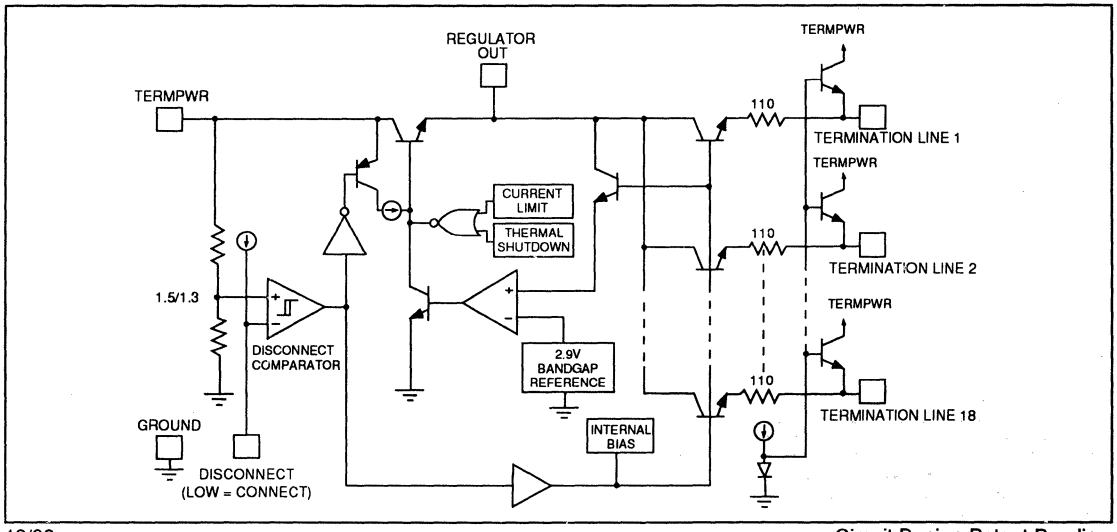
ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... + 7V
Signal Line Voltage ..... 0V to + 7V
Regulator Output Current 1A
Power Dissipation 2.5W
Operating Junction Temperature ... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

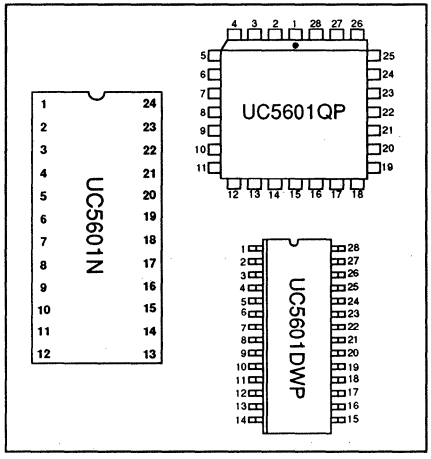
RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 4.0V to 5.25V
Signal Line Voltage ..... 0V to + 3V
Disconnect Input Voltage ..... 0V to Termpower

BLOCK DIAGRAM



CONNECTION DIAGRAM



UC5601 SCSI ACTIVE TERMINATOR PINOUT

PIN NAME	QP PKG PIN #	DWP PKG PIN #	N PKG PIN #	PIN NAME	QP PKG PIN #	DWP PKG PIN #	N PKG PIN #
TermPower	1	14	12	Termination Line 5	24	6	7
GND*	12	7	24	Termination Line 6	25	10	8
GND*	13	8		Termination Line 7	26	11	9
GND*	14	9		Termination Line 8	27	12	10
GND*	15	20		Termination Line 9	28	13	11
GND*	16	21		Termination Line 10	3	16	14
GND*	17	22		Termination Line 11	4	17	15
GND*	18	28		Termination Line 12	5	18	16
Reg Out	2	15	13	Termination Line 13	6	19	17
Disconnect	19	1	1	Termination Line 14	7	23	18
Termination Line 1	20	2	2	Termination Line 15	8	24	19
Termination Line 2	21	3	3	Termination Line 16	9	25	20
Termination Line 3	22	4	5	Termination Line 17	10	26	22
Termination Line 4	23	5	6	Termination Line 18	11	27	23

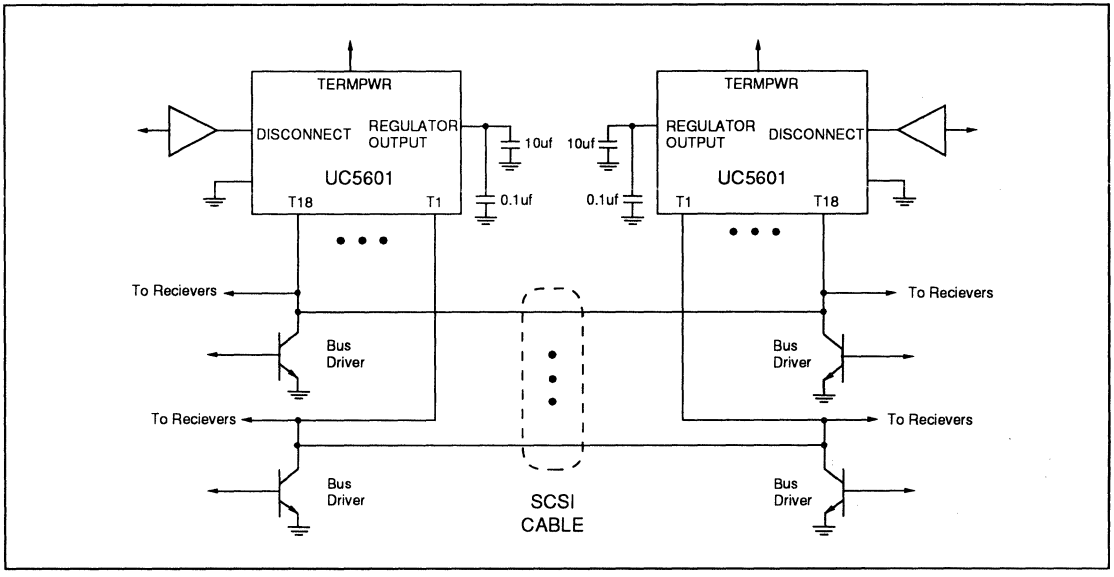
*On the QP package pins 12-18 serve as both heatsink, and electrical ground. On the DWP package only pin 28 serves as the electrical ground with pins 7-9, 20-22 as heatsink.

ELECTRICAL CHARACTERISTICS (Unless otherwise, stated these specifications apply for T_A = 0°C TO 70°C. Termpwr = 4.75V Disconnect = 0V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		17	25	mA
	All termination lines = 0.5V		400	430	mA
Power down Mode	Disconnect = Open		100	150	uA
Output Section (Termination Lines)					
Termination Impedance	Δ Iterm = – 5mA to – 15mA	107	110	113	Ohms
Output high voltage	Termpwr = 4V (Note2)	2.65	2.9		V
Max Output Current	Vout = 0.5V	-21.1	-21.7	-22.4	mA
	Vout = 0.5V, Termpwr = 4V (Note 2)	-19.8	-21.7	-22.4	mA
Output Clamp level	Iout = – 30mA	-0.2	-0.05	0.1	V
Output Leakage	Disconnect = Open, Vin = 0V to 5.25V		10	400	nA
Output Capacitance	Disconnect = Open (Note 3)		10		pF
Regulator Section					
Regulator output voltage		2.80	2.90	3.00	V
Line Regulation	Termpwr = 4V to 6V		10	20	mV
Load Regulation	I Reg = 0 to -400mA		20	50	mV
Drop out voltage	All Termination lines = 0.5V Δ Vout = 100mV		1.0	1.2	V
Short Circuit Current	Regulator output = 0V	-450	-650	-850	mA
Current Sink Capability	Vout = 3.5V	8	20		mA
Thermal Shutdown			170		°C
Disconnect Section					
Disconnect Threshold		1.3	1.5	1.7	V
Threshold hysterisis		100	160	250	mV
Input Current	Disconnect = 0V		10	15	uA

NOTE 1: Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
NOTE 2: Measuring each termination line while other 17 are low (0.5V).
NOTE 3: Guaranteed by design but not 100% tested in production.

TYPICAL SCSI BUS CONFIGURATION USING THE UC5601



A LOOK AT THE RESPONSE OF A SCSI-2 CABLE

Figure 1 shows a single line of a SCSI cable. The driver is an open collector type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage Vstep is defined as:

$$\mathbf{Vstep = Vol + Io\ Z0}$$

Vol = Driver Output Low Voltage
Io = Current from receiving terminator
Z0 = Cable characteristic impedance

$$\mathbf{Io} = \frac{\text{Vreg-Vol}}{110}$$

In the pursuit of higher data rates, sampling could occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5601 is trimmed so that the output current (Io) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

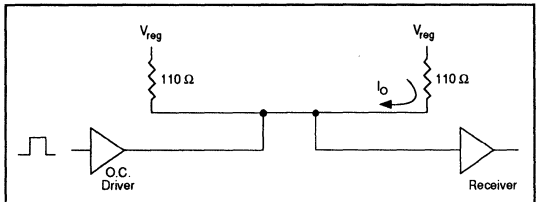


Figure 1. A Single Line of a SCSI Cable

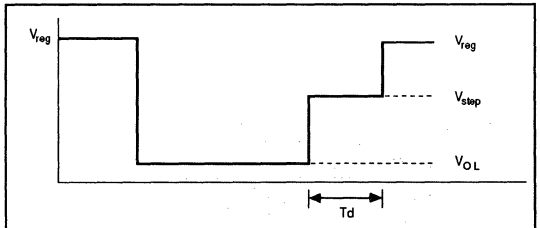


Figure 2. A Typical Response of a SCSI Cable

THERMAL DATA (see packaging section of UICC data book for more details on thermal performance)
QP package:

Thermal Resistance Junction to Leads, θjL ..... 15°C/W
Thermal Resistance Junction to Ambient, θja ..... 30°–40°C/W

DWP package:

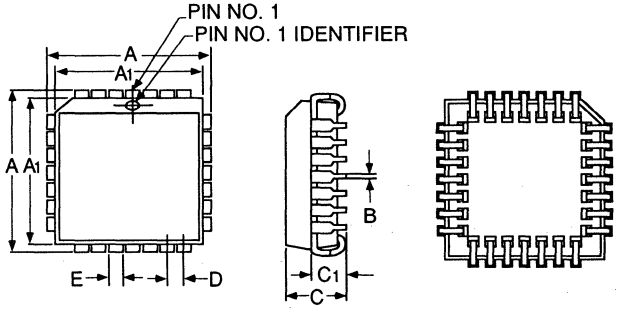
Thermal Resistance Junction to Leads, θjL ..... 18°C/W
Thermal Resistance Junction to Ambient, θja ..... 33°–43°C/W

NOTE: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

PACKAGE INFORMATION

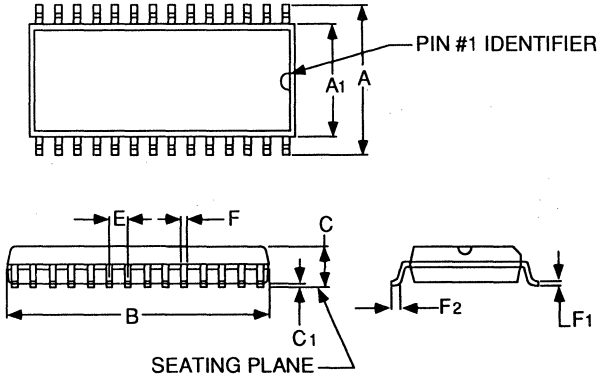
POWER PLCC PACKAGE (QP SUFFIX)

DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.485	.495	12.32	12.57
A1	.450	.454	11.43	11.53
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C1	.100	.110	2.54	2.79
D	.050		1.27	
E	.026	.032	0.66	0.51



POWER SOIC PACKAGE (DWP SUFFIX)

DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.398	.414	10.11	10.51
A1	.291	.299	7.40	7.60
B	.698	.706	17.73	17.93
C	.096	.104	2.44	2.64
C1	.004	.012	0.10	0.30
E	.050 BSC		1.27 BSC	
F	.013	.020	0.33	0.51
F1	.0091	.0125	0.23	0.32
F2	.020	.040	0.61	1.01



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SCSI Active Terminator

PRELIMINARY

FEATURES

- Fully Monolitic IC Solution
- Complies with SCSI and SCSI-2 Standards
- Provides Active Termination for 18 Lines
- Logic Command Disconnects all Terminating Resistors
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- Low Dropout Voltage Regulator
- Low Thermal Resistance Surface Mount Packages

DESCRIPTIONS

The UC5602 is a pin compatible version of its predecessor, the UC5601, and is targeted for high volume applications which require active termination, but not the high performance of the UC5601. The major differences are relaxed output current and termination tolerances, and the absence of low side clamps.

The UC5602 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI-2 standard recommends active termination at both ends of the cable segment, and SCSI-3 will make it a requirement.

The UC5602 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance, and then most importantly, to trim the output current to a 7% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown, current limit, and 40mA of active negation sink current capability.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, PLCC and TQFP (thin quad flat pack).

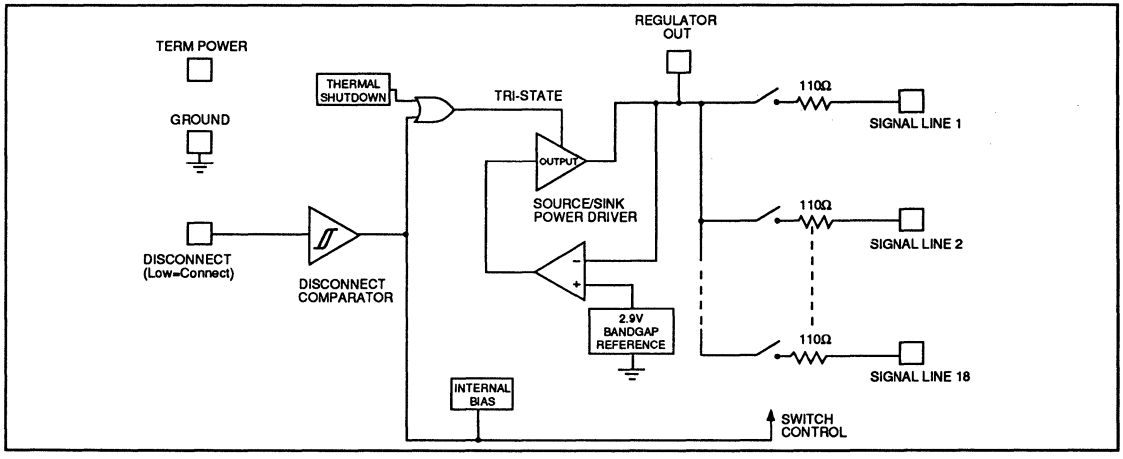
ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current 1A
Power Dissipation 2.5W
Operating Junction Temperature .. -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

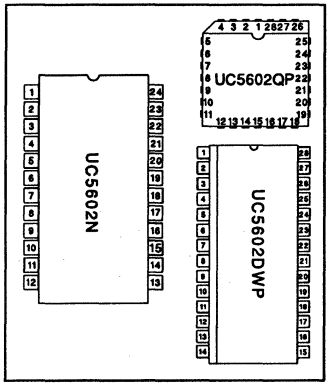
RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 4.0V to 5.25V
Signal Line Voltage ..... 0V to +3V
Disconnect Input Voltage ..... 0V to Termpower

BLOCK DIAGRAM



CONNECTION DIAGRAM



UC5602 SCSI ACTIVE TERMINATOR PINOUT

UC5602

PIN NAME	QP PKG PIN #	DWP PKG PIN #	N PKG PIN #	PIN NAME	QP PKG PIN #	DWP PKG PIN #	N PKG PIN #
TermPower	1	14	12	Termination Line 5	24	6	7
GND*	12	7	24	Termination Line 6	25	10	8
GND*	13	8		Termination Line 7	26	11	9
GND*	14	9		Termination Line 8	27	12	10
GND*	15	20		Termination Line 9	28	13	11
GND*	16	21		Termination Line 10	3	16	14
GND*	17	22		Termination Line 11	4	17	15
GND*	18	28		Termination Line 12	5	18	16
Reg Out	2	15	13	Termination Line 13	6	19	17
Disconnect	19	1	1	Termination Line 14	7	23	18
Termination Line 1	20	2	2	Termination Line 15	8	24	19
Termination Line 2	21	3	3	Termination Line 16	9	25	20
Termination Line 3	22	4	5	Termination Line 17	10	26	22
Termination Line 4	23	5	6	Termination Line 18	11	27	23

*On the QP package pins 12-18 serve as both heatsink, and electrical ground. On the DWP package only pin 28 serves as the electrical ground with pins 7-9, 20-22 as heatsink.

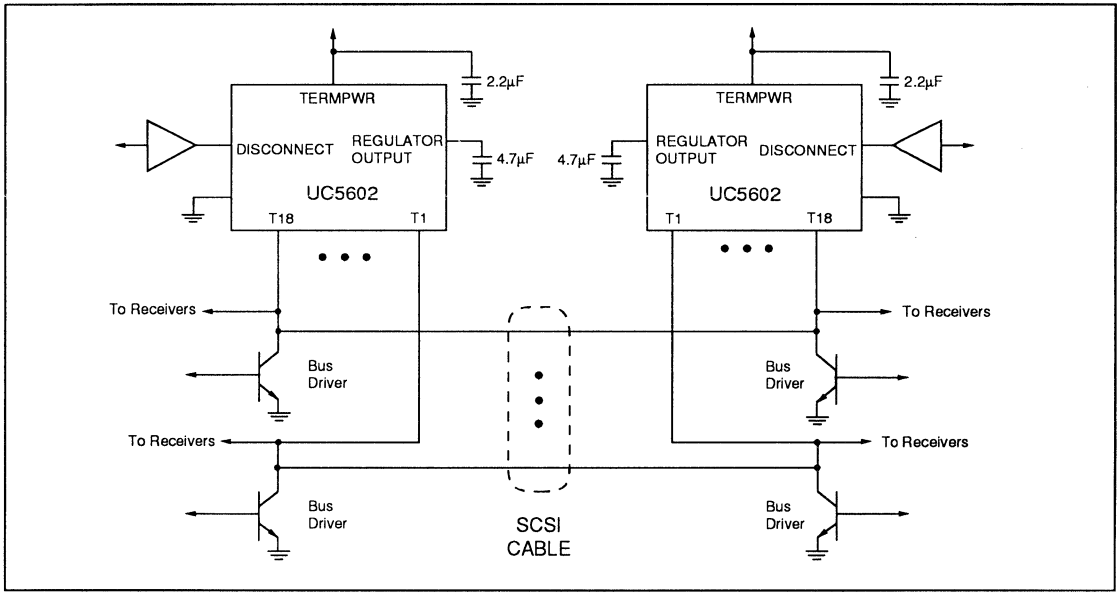
ELECTRICAL CHARACTERISTICS:

Unless otherwise, stated these specifications apply for T_A = 0°C TO 70°C. Termpwr= 4.75V Disconnect = 0V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current Section						
Termpwr Supply Current	All termination lines = Open			20	29	mA
	All termination lines = 0.5V			400	435	mA
Power Down Mode	Disconnect = Open			100	150	uA
Output Section (Termination Lines)						
Termination Impedance	Δ Iterm = – 5mA to – 15mA	T_J=25°C	102	110	118	Ω
		Overtemp	97		129	Ω
Output High Voltage	Termpwr = 4v, (Note 1)	T_J=25°C	2.6	2.9	3.1	V
		Overtemp	2.55		3.2	V
Max Output Current	V_{OUT} = 0.5V	T_J=25°C	-19.5	-21.4	-22.4	mA
		Overtemp	-18.5		-22.4	mA
Max Output Current	V_{OUT} = 0.5V	T_J=25°C	-18.0	-21.5	-22.4	mA
	Termpwr = 4V, (Note 2)	Overtemp	-17.0		-22.4	mA
Output Leakage	Disconnect = Open, V_{IN} = 0V to 5.25V			10	400	mA
Output Capacitance	Disconnect = Open (Note 3)			10		pF
Regulator Section						
Regulator Output Voltage	T_J = 25°C		2.70	2.90	3.10	V
Regulator Output Voltage		T_J=25°C	2.55	2.9	3.1	V
		Overtemp	2.5		3.2	V
Line Regulation	Termpwr = 4V to 6V			10	20	mV
Load Regulation	I Reg = 0 to -400mA			20	50	mV
Drop Out voltage	All Termination Lines = 0.5V Δ V_{OUT} = 100mV			1.0	1.2	V
Short Circuit Current	Regulator Output = 0V		-450	-650	-850	mA
Current Sink Capability	V_{OUT} = 3.5V		20	40		mA
Thermal Shutdown				170		°C
Disconnect Section						
Disconnect Threshold			1.1	1.4	1.7	V
Threshold hysterisis				100		mV
Input Current	Disconnect = 0V			150	200	µA

NOTE 1: Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
NOTE 2: Measuring each termination line while other 17 are low (0.5V).
NOTE 3: Guaranteed by design but not 100% tested in production.

TYPICAL SCSI BUS CONFIGURATION USING THE UC5602



A LOOK AT THE RESPONSE OF A SCSI-2 CABLE

Figure 1 shows a single line of a SCSI cable. The driver is an open collector type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage VSTEP is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL}	=	Driver Output Low Voltage
I_O	=	Current from receiving terminator
Z_0	=	Cable characteristic impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling could occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5602 is trimmed so that the output current (Io) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

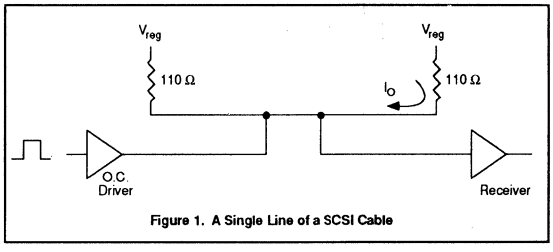


Figure 1. A Single Line of a SCSI Cable

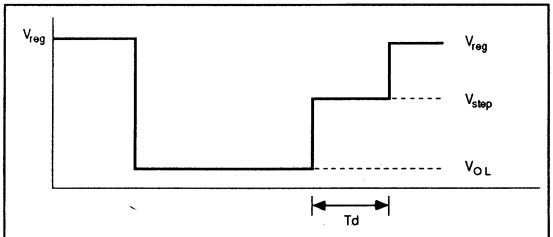


Figure 2. A Typical Response of a SCSI Cable

THERMAL DATA: (see packaging section of UICC data book for more details on thermal performance)

QP package

Thermal Resistance Junction to Leads, θjL ..... 15°C/W

Thermal Resistance Junction to Ambient, θjA ..... 30°–40°C/W

DWP package:

Thermal Resistance Junction to Leads, θjL ..... 18°C/W

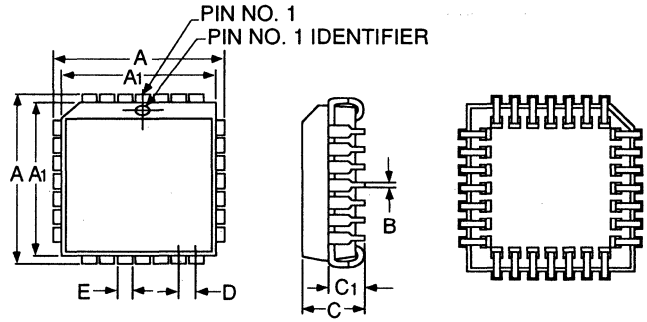
Thermal Resistance Junction to Ambient, θjA ..... 33°–43°C/W

NOTE: *The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θjA numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.*

PACKAGE INFORMATION

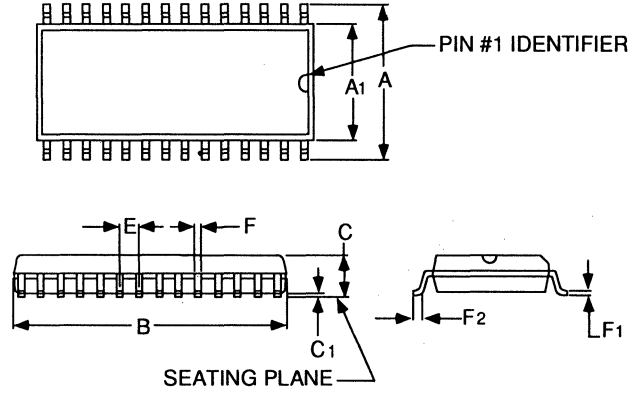
POWER PLCC PACKAGE (QP SUFFIX)

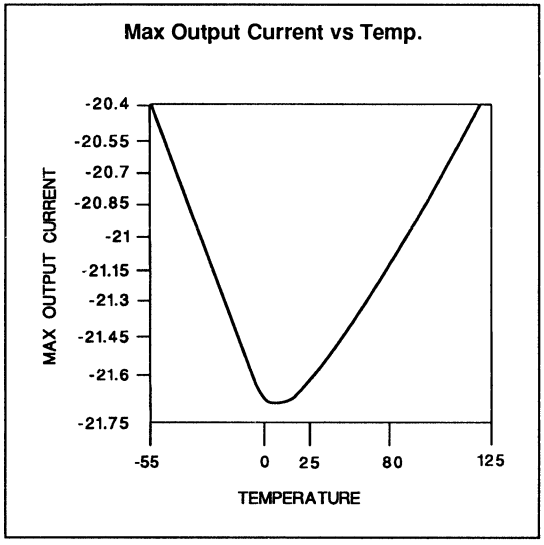
DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.485	.495	12.32	12.57
A_1	.450	.454	11.43	11.53
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C_1	.100	.110	2.54	2.79
D	.050		1.27	
E	.026	.032	0.66	0.51

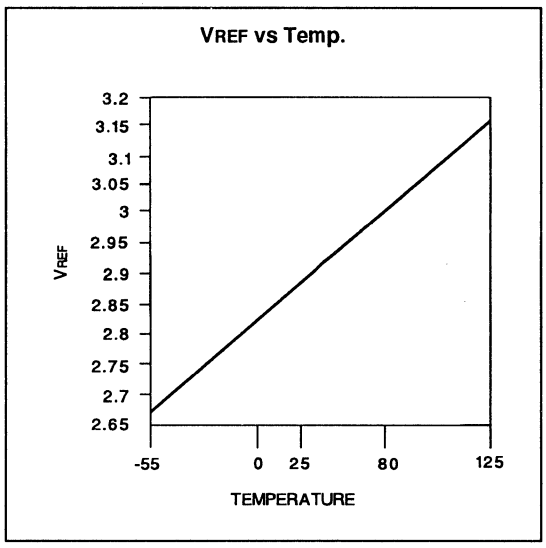


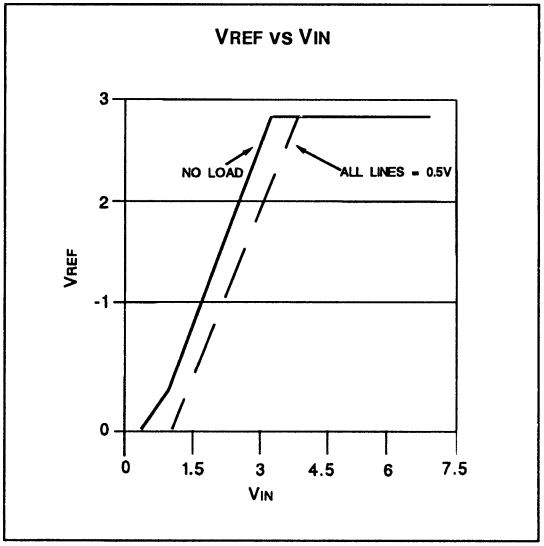
POWER SOIC PACKAGE (DWP SUFFIX)

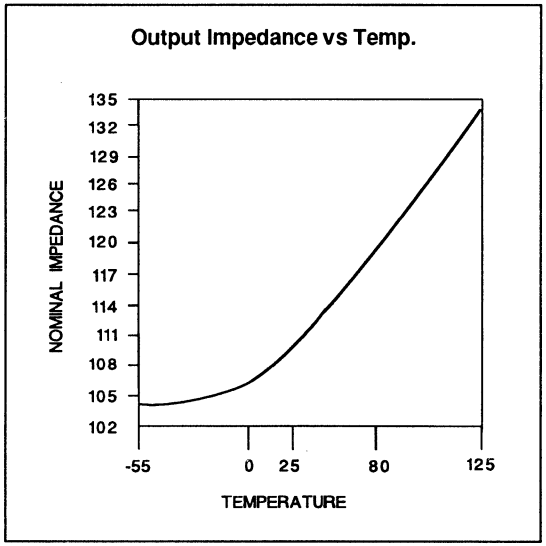
DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.398	.414	10.11	10.51
A_1	.291	.299	7.40	7.60
B	.698	.706	17.73	17.93
C	.096	.104	2.44	2.64
C_1	.004	.012	0.10	0.30
E	.050 BSC		1.27 BSC	
F	.013	.020	0.33	0.51
F_1	.0091	.0125	0.23	0.32
F_2	.020	.040	0.61	1.01











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9-Line SCSI Active Terminator

FEATURES

- Complies with SCSI and SCSI-2 Standards
- Provides Active Termination for 9 Lines
- Power Regulator Output Stage
- -300mA Sourcing Current for Termination
- +300mA Sinking Current for Active Negation
- 6pf Channel Capacitance during Disconnect
- 0.7V Dropout Voltage Regulator
- Logic Command Disconnects all Termination Lines
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 3%
- Trimmed Impedance to 3%
- Negative Clamping on all Signal Lines
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount and Zip Packages

DESCRIPTION

The UC5603 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

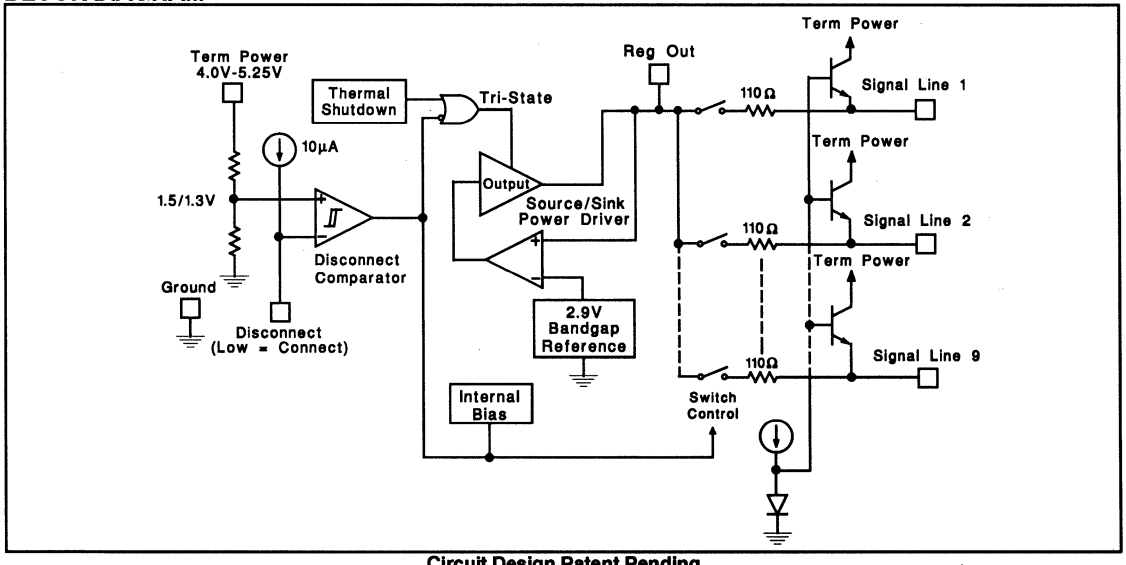
The UC5603 Provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 6pf allows units at interim points of the bus to have little to no effect on the signal integrity.

Functionally the UC5603 is similar to its predecessor, the UC5601 - 18 line Active Terminator. Several electrical enhancements were incorporated in the UC5603, such as a sink/source regulator output stage to accommodate all signal lines at +5V, while the regulator remains at its nominal value, reduced channel capacitance to 6pf typical, and as with the UC5601, custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 3% tolerance, and then most importantly, to trim the output current to a 3% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include negative clamping on all signal lines to protect external circuitry from latch-up, thermal shutdown and current limit.

BLOCK DIAGRAM



Circuit Design Patent Pending

ABSOLUTE MAXIMUM RATINGS

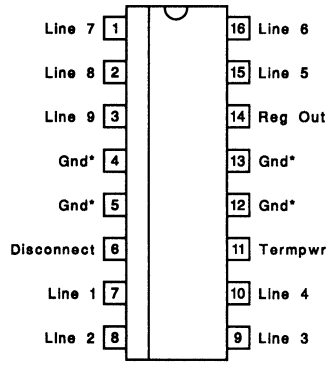
Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Power Dissipation..... 2W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpower

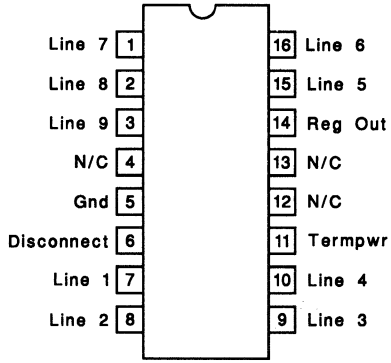
CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Package

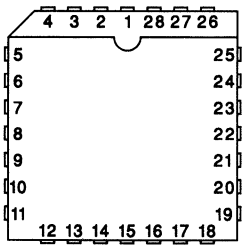


** DP package pin 5 serves as electrical ground; pins 4, 12, 13 serve as heatsink.*

DIL-16 (TOP VIEW)
N or J Package



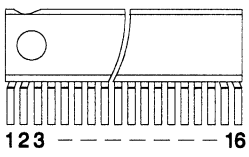
PLCC-28 (TOP VIEW)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1 - 4
Reg Out	5
Line 5	6
Line 6	7
Line 7	8
Line 8	9
Line 9	10
N/C	11
Gnd *	12 - 18
N/C	19
Disconnect	20
Line 1	21
Line 2	22
Line 3	23
Line 4	24
Termpwr	25
N/C	26 - 28

** QP package pins 12 - 18 serve as both heatsink and electrical ground.*

ZIP-16 (TOP VIEW)
Z Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Reg Out	1
Line 5	2
Line 6	3
Line 7	4
Line 8	5
Line 9	6
Gnd	7
Gnd	8
Gnd	9
Gnd	10
Disconnect	11
Line 1	12
Line 2	13
Line 3	14
Line 4	15
Termpwr	16

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS

(Unless otherwise, stated these specifications apply for T_A=0°C to 70°C. Termpwr = 4.75V Disconnect = 0V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		12	18	mA
Termpwr Supply Current	All termination lines = 0.5V		200	220	mA
Power Down Mode	Disconnect = Open		100	150	µA
Output Section (Terminator Lines)					
Terminator Impedance	Item = =5mA to -15mA	107	110	113	Ohms
Output High Voltage	Termpwr = 4V (Note 2)	2.7	2.9		V
Max Output Current	V_{OUT} = 0.5V	-21.1	-21.9	-22.4	mA
Max Output Current	V_{OUT} = 0.5V, Termpwr = 4V (Note 2)	-19.8	-21.9	-22.4	mA
Output Clamp Level	I_{OUT} = -30mA	-0.2	-0.05	0.1	V
Output Leakage	Disconnect = Open, Termpwr = 0V to 5.25 V		10	400	nA
Output Capacitance	Disconnect = Open (Note 3)		6	10	pF
Regulator Section					
Regulator Output Voltage		2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 5V	2.8	2.9	3	V
Line Regulation	Termpwr = 4V to 6V		10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA		20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V		0.7	1	V
Short Circuit Current	V_{REG} = 0V	-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	600	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		1.3	1.5	1.7	V
Threshold Hysteresis		100	160	250	mV
Input Current	Disconnect = 0V		10	15	µA

Note 1: Unless otherwise specified all voltages are with respect to Ground.
Currents are positive into, negative out of the specified terminal.
Note 2: Measuring each termination line while other 8 are low (0.5V).
Note 3: Guaranteed by design but not 100% tested in production.

THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
- Thermal Resistance Junction to Leads, θjL ..... 15°C/W
- Thermal Resistance Junction to Ambient, θja ..... 30°-40°C/W

DP,Z packages:
- Thermal Resistance Junction to Leads, θjL ..... 20°C/W
- Thermal Resistance Junction to Ambient, θja ..... 40°-50°C/W

N packages:
- Thermal Resistance Junction to Leads, θjL ..... 50°C/W
- Thermal Resistance Junction to Ambient, θja ..... 95°-105°C/W

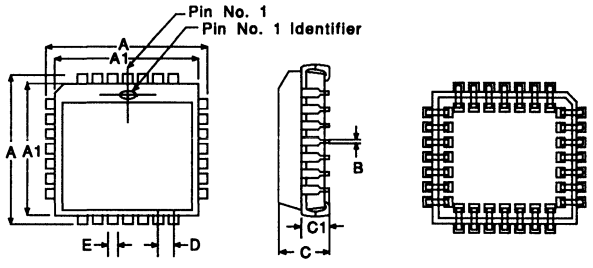
J packages
- Thermal Resistance Junction to Leads, θjL ..... 40°C/W
- Thermal Resistance Junction to Ambient, θja ..... 75°-85°C/W

Note: The above numbers for θjL are maximums for the limiting termal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

PACKAGE INFORMATION

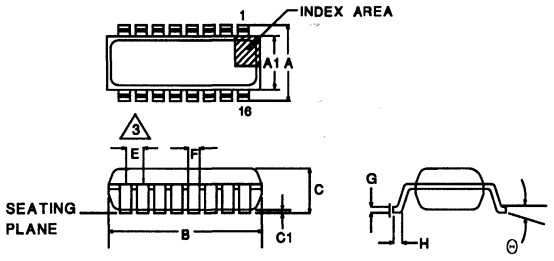
POWER PLCC PACKAGE (QP SUFFIX)

DIMENSIONS				
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.485	.495	12.32	12.57
A1	.450	.454	11.43	11.53
B	.013	.021	0.33	0.53
C	.170	.180	4.32	4.57
C1	.100	.110	2.54	2.79



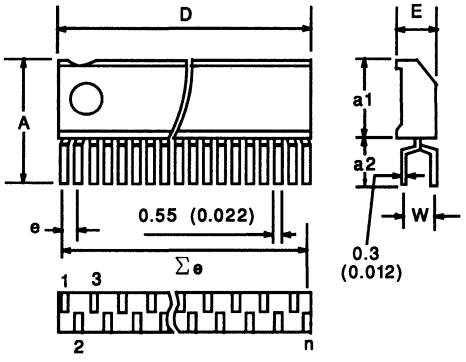
POWER SOIC PACKAGE (DP SUFFIX)

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48



ZIG ZAG INLINE PACKAGE (Z SUFFIX)

PIN COUNT	16
A	9.9 0.386
a1	7.0 0.287
a2	2.9 0.114
D	19.5 0.768
e	1.27 0.05
e	19.05 0.75
E	2.75 0.108
W	2.8 0.110



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APPLICATION INFORMATION

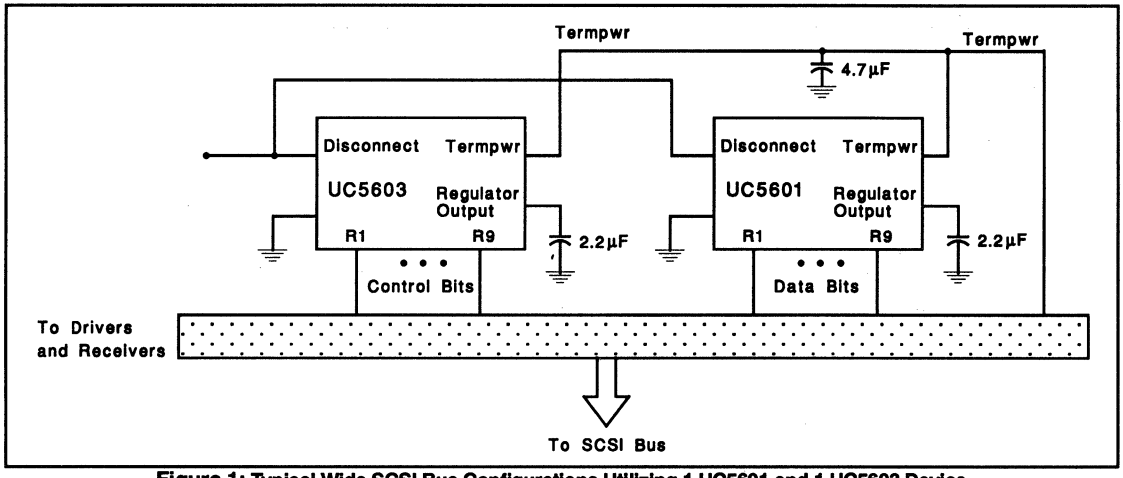

Figure 1: Typical Wide SCSI Bus Configurations Utilizing 1 UC5601 and 1 UC5603 Device

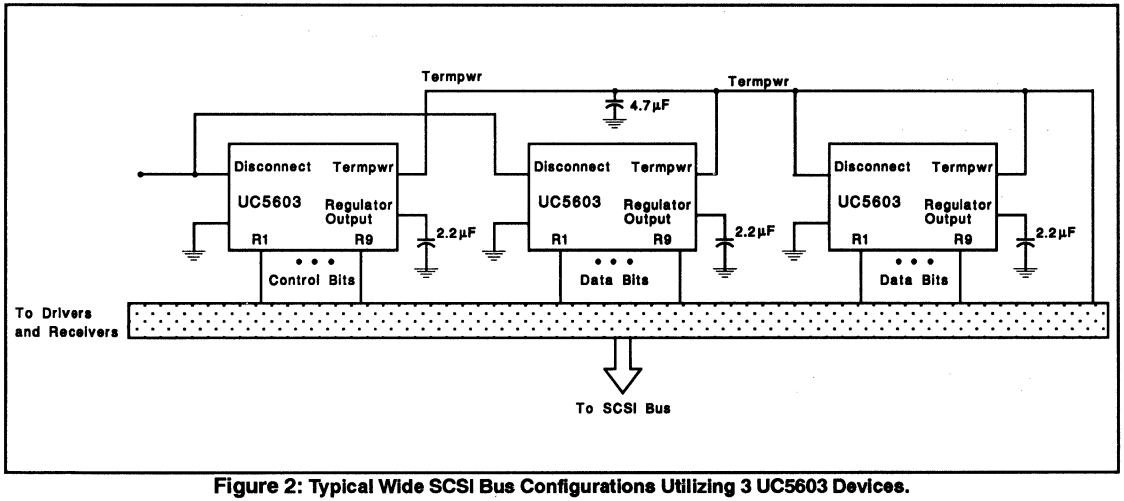

Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5603 Devices.

UNITRODE INTEGRATED CIRCUITS
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Ethernet Coaxial Impedance Monitor

FEATURES

- Compatible with IEEE 802.3 10Base5, 10Base2, and 10BaseT
- Preset and Adjustable Data Thresholds
- Protects DTE from Spurious Data
- Prevents Erroneous Transmission Through Repeaters
- Detects Cable Termination Errors
- Detects Cable Impedance Errors

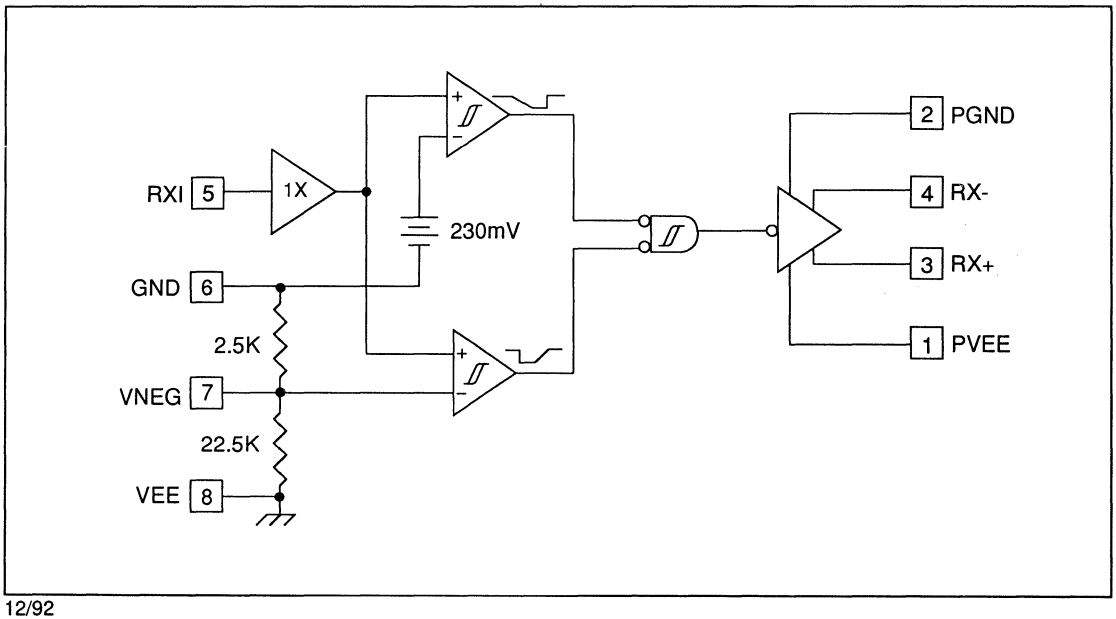
DESCRIPTION

The UC5661 is a monolithic integrated circuit which functions as an Ethernet Coaxial Impedance Monitor (CIM). This IC is intended to augment the receive (RX) function of IEEE 802.3 Coaxial Transceiver Interface (CTI) circuits. The UC5661 implements a hardware algorithm patented by Digital Equipment Corporation to detect reflections on the Ethernet coaxial cable or twisted pair which are caused by improper network termination or physical medium damage. If a physical problem is detected, the UC5661, whose receiver outputs operate in parallel with the CTI, immediately squelches the receive data, preventing the propagation of invalid network packets. During ordinary operation, the CIM RX outputs enable at the beginning of the data packet preamble, making it transparent to normal CTI functions. The valid data threshold, although preset for thick and thin-wire Ethernets, may be adjusted with the addition of one or two external resistors to meet 10BaseT requirements.

A secondary system design feature is provided by the UC5661. A the completion of a normal data transmission, the CIM Squelch activates much faster than typical transceiver ICs. The receiver outputs of the UC5661 have been designed to properly terminate the data packet, even with RX data transformers as small as 16uH, possibly allowing for smaller and less expensive system implementations. In these cases, end-of-packet squelch overshoot will be held to less than 100mV.

7

BLOCK DIAGRAM



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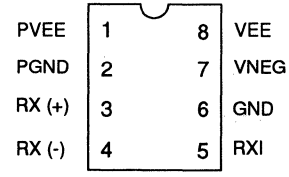
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 1 & 8) ..... - 15V
Input Voltage (Pin 5) ..... +2 to - 10V
Operating Temperature Range
UC5661 ..... 0°C to 70°C
Junction Temperature (Note 1)
UC5661 ..... 125°C
Storage Temperature Range ..... - 55°C to 150°C
Lead Temperature (Soldering, 10SEC) ..... 300°C

Note 1: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

CONNECTION DIAGRAM

DIL-8 (Top View)
J or N Package



DC Electrical Characteristics: Unless otherwise stated, these specifications apply for T_A=0°C to 70°C, Vee = PVee = -9.0V, and R_L = 500 ohms, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Outputs locked or Unlocked, Unloaded		10	20	mA
Input Bias Current	RXI = 0V		2	5	uA
Input Shunt Resistance	RXI = - 2V to 0V	.200	45		Mohm
Input Shunt Capacitance	Note 1		3	4	pF
Vneg (Valid Data Reference)	Pin 7 = open	- 980	- 900	-830	mV
RX Output Voltage High (Squelch)		- 1.2	-.9	0	V
RX Output Voltage Low (Enable)		- 6	- 3.7	- 3.2	V
Output Short Circuit	RX(+) = RX(-) = 9V	- 150			mA
Valid Data Threshold		- 980	- 900	- 830	mV
Data Reflection Threshold		200	230	300	mV

Note 1: This parameter guaranteed but not tested.

AC Electrical Characteristics: Unless otherwise stated, these specifications apply for T_A=0°C to 70°C, Vee = PVee = -9.0V, and R_L = 500 ohms, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{EN} RX Enable Delay	see figure 1, 2		100	400	ns
T_{DIS} RX Disable Delay	see figure 1, 2	250	340	475	ns
T_{FS} RX (+) to RX (-) Falling Edge Skew	see figure 1, 2		5	20	ns
T_{FR} RX (+) to RX (-) Rising Edge Skew	see figure 1, 2		5	20	ns
T_{SQL} RX Squelch Delay	see figure 1, 3		230	2000	ns
T_{REL} RX Release Delay	see figure 1, 3	500	1150	1500	ns

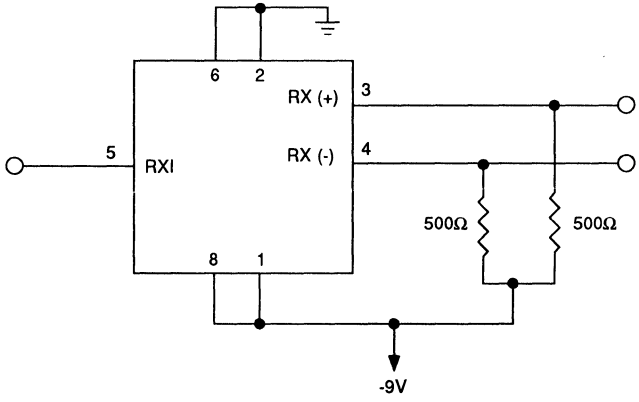


FIGURE 1: SWITCHING TEST CIRCUIT

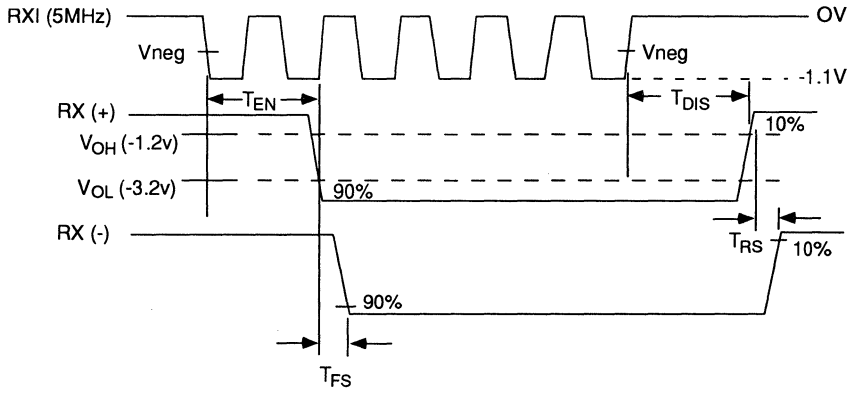


FIGURE 2: INPUT/OUTPUT TIMING DIAGRAM

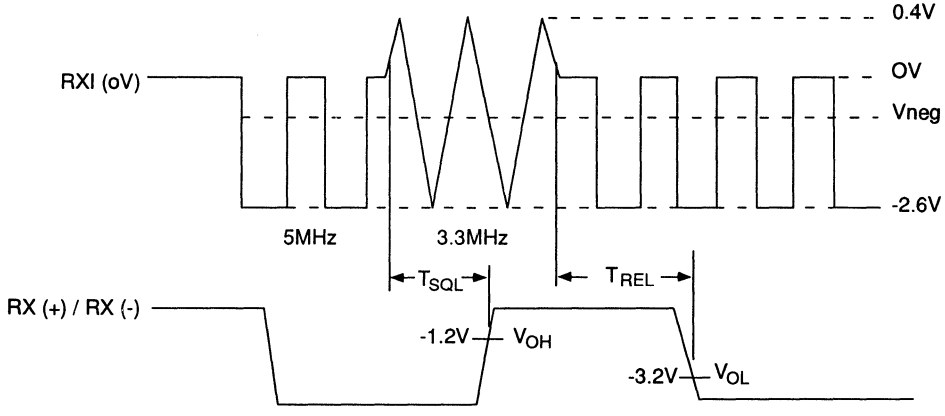


FIGURE 3: SHORT DETECT TIMING DIAGRAM

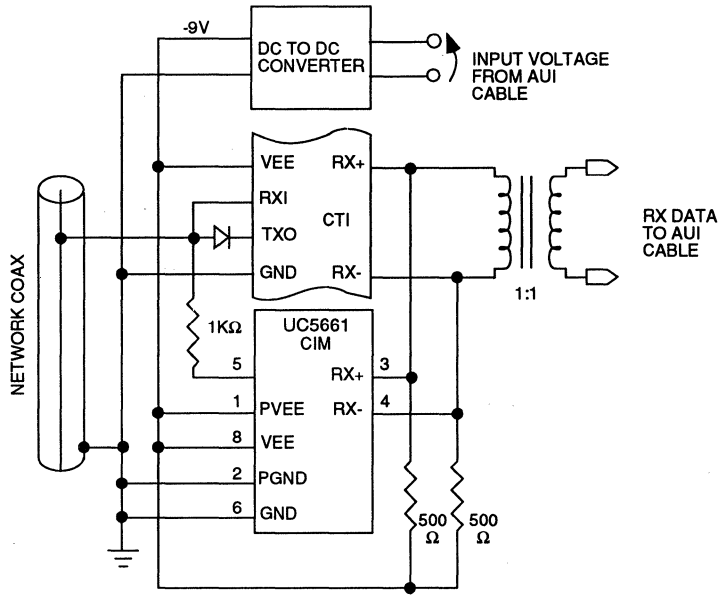


FIGURE 4: TYPICAL APPLICATION

Figure 4 shows the UC5661 (SDI) being used with a Coaxial Transceiver Interface (CTI) device. The primary function of the SDI is to detect LAN cable shorts (or other impedance matching problems) and appropriately squelch the RX outputs of the CTI device to prevent the transmission of corrupted network data. The secondary function of the SDI is to provide improved RX squelching at the completion of a normal data transmission.

To perform the two functions, SDI uses two threshold voltages, Data Reflection Threshold (DRT), and the Valid Data Threshold (VDT). During transmission SDI looks for signal activity above ground and below ground. In the event that the magitude of the input voltage exceeds DRT the outputs will be locked within 2µS and will remain locked for 0.5 to 1.5µS after the last edge below DRT (see figure 3). During signal activity below ground when the signal goes below VDT the outputs will unlock within 400ns. While unlocked, if the input exceeds VDT the outputs will lock within 250 to 475ns relative to the last positive going edge (figure 2).

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DEVICE TEMPERATURE MANAGEMENT

All circuit components will dissipate some power while operating and this causes their temperature to rise. Unitrode integrated circuits are designed to handle a considerable range of temperatures, but there are limits. Each part is characterized for a particular temperature range, and the user must see to it that the specified limits are not exceeded. This brief note will give a few hints on how to do this.

With the power turned off, all components of a given circuit will be at the same temperature as the ambient air (assuming, of course, that sufficient time has elapsed for all differences to settle). With the power on, the various components will be warmed up due to their internal power dissipation, until a new state of equilibrium is reached. In this state, some devices may be better than others, and the air temperature will also be higher than before, but for each device it will be true that the amount of heat transfer occurs between the device's case and the air, as well as by conduction through the P.C. board, of heatsink, and from there to the air.

Since all the heat is generated at the silicon chip, it is safe to assume that the chip must be hotter than the IC case; the case must be hotter than the air, or board, or heatsink; and the board or heatsink must be hotter than the air. In short, heat flows downhill, from points of higher temperature to cooler spots.

The rate of heat flow depends on the temperature difference(ΔT) between the two end points, and also on a quantity called "thermal resistance," which is represented by the symbol θ. Heat is a form of energy, and if we choose the joule as the measuring unit we can specify the rate of heat flow in units of joules per second. Therefore,

$$\text{Rate of heat flow} \frac{\Delta T}{\theta} \text{ [joules per second]}$$

and since joules per second is the same as watts (W), we have

$$\theta = \frac{\Delta T}{W} [^\circ C \text{ per watt}] \qquad (1)$$

The quantity θ defines an important property of materials, with the better thermal conductors having the lowest θ values, Since IC chips must be protected by a variety of packages, it is important for the user to know the thermal resistance θ of each type of package, in order to make certain predictions about the behavior of the device in his circuit.

Table 1 shows thermal resistance values for Unitrode IC packages. Thermal resistance junction to case (θjc) is measured by mounting the device to an essentially infinite heat sink. Power lead frame surface mount packages and the batwing DIP conduct the majority of the dissipated power through their leads rather than through the case. For these noted packages, the specified thermal resistance is junction to lead (θjl).

Junction to ambient (θja) thermal resistance is measured on a 5.0 square inch single sided PC board in still air. Because surface mount devices, including those without power lead frames conduct a significant amount of heat out to the PC board through their leads, the device and PC board must be considered as a system. To indicate this effect, the lower θja given for surface mount packages is for the device mounted on a 5.0 square inch,0.062 inch thick aluminum PC board. The relative behavior of other PC board types and a more detailed discussion on surface mounted devices are covered in more detail in "Thermal Characteristics of Surface Mount Packages" found elsewhere in this section.

You will have noticed that Equation (1) is a sort of "thermal Ohm's law", and that if you know any of the quantities involved, you can calculate the third. With the θ values given in Table 1, you can always calculate the junction temperature by measuring the net input power to the IC.

Now, consider a device such as the UC3620. The data sheet gives us the following Absolute Maximum Ratings:

Total Power Dissipation

(TCASE + 75°C) 25W
Storage & Junction Temp . . . . 40°C to + 150°C

Packaging Information

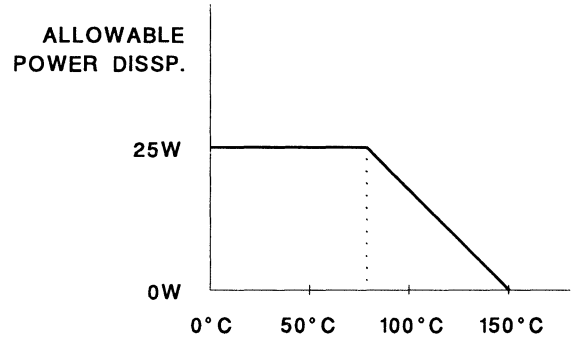
UICC PACKAGE RATINGS

PACKAGE			θjc (°C/W)	θja (°C/W) (2)
PACKAGE SUFFIX	#PINS	DESCRIPTION		
D	8	SO-IC	N/A	84-160
D, DW	14, 16	SO-IC	N/A	50-120
DP	8	SO-IC Power Lead Frame	22 (1)	40-70
DP	16	SO-IC Power Lead Frame	20 (1)	36-58
DWP	28	SO-IC Power Lead Frame	16 (1)	30-50
FQ	48	SQFP	N/A	76-140
FQP	48	SQFP Power Lead Frame	25 (1)	39-100
G	3	TO-257 Non-Isolated Tab	3.5	42
H	3	TO-39, TO-5	20	130
IG	3	TO-257 Isolated Tab	4.0	130
J	8	Ceramic Dip	26	160
J	14, 16	Ceramic Dip	26	110
J	18	Ceramic Dip	22	88
J	20	Ceramic Dip	22	85
J	24, 28	Ceramic Dip	16	65
K	2	TO-3	3	35
L	20	CLCC	18	70
L	28	CLCC	17	65
N	8	Plastic Dip	49	110
N	14, 16	Plastic Dip	46	90
N	16	Plastic Batwing Dip	12 (1)	25-50
N	18	Plastic Dip	40	85
N	20	Plastic Dip	35	79
N	24, 28	Plastic Dip	30	58
Q	20	PLCC	N/A	43-75
Q	28	PLCC	N/A	40-65
QP	28	PLCC Power Lead Frame	14 (1)	28-50
R	2	TO-66	5	40
SP	16	Ceramic/Metal Dip	5	63
SP	24	Ceramic/Metal Dip	3	40
T	3, 5	TO-220	3	60
V,VH	15	Multiwatt (R)	3	35

Table 1. Thermal resistance of Unitrode IC packages

Note 1: Specified thermal resistance is θjl (junction to lead) where noted.
Note 2: Specified θja (junction to ambient) is for devices mounted to 5.0 square inch FR4 PC board with one ounce copper. When resistance range is given, lower values are for 5.0 square inch aluminum PC board - see text.

We can sketch the curve below:



$$\text{slope} = \frac{-25W}{75°C} = \frac{-1}{3} W/°C$$

$$= \frac{-1}{\theta JC}$$

Athough the data sheet does not specifically state the derating factor, we can calculate it from the information given; it is the slope of the line from +75°C + 150°C. In this case, the value is —1/3W/°C at a case temperatures above +75°C. We note that the junction temperature anywhere along the curve is +150°C, and since this is the maximum allowable temperature, we must take steps to stay within the area below the curve.

The thermal resistance can be found simply taking the reciprocal of the derating factor. In the case of our UC3620 for example:

$\theta JC = 3°C/W$

which is also the value given in Table 1 for the 15-pin Multiwatt package.

Suppose one intends to use the UC3620 at 2A continuous output current. The data sheet states that the total voltage drop at the output states is 3.6V maximum. At 2A, this will result in an internal dissipation of 7.2W. If the supply voltage is say, 36V, the quiescent current of 55mA maximum gives us an additional 2W of internal heating, for a total of 9.2W. Furthermore, we decide to provide sufficient cooling to keep the junction temperature at a maximum of 100°C—for increased reliability. Suppose the ambient temperature is to be +50°C maximum. Then, our ΔT is 100°C - 50°C = 50°C, and the required thermal resistance from junction to air will be

$$\theta CA = \frac{50°C}{9.2W} = 5.43°C/W$$

We know already that $\theta JC = 3°C/W$. Mounting the IC to a heatsink will result in an additional thermal resistance in series. If you decide to use a mica insulator coated with thermal grease, you insert an additional 0.3°C/W (see any Semiconductor Accessories Catalog). Therefore, we need a heatsink with a θCA value of

$\theta CA = 5.43 - 3 - 0.3 = 2.13°C/W$

This is the maximum value of thermal resistance between mounting surface and air that will keep the junction temperature at or below the chosen value of 100°C. We need only to go through a heatsink manufacturer's catalog to find a suitable part or extrusion with the required θCA value.

THERMAL CHARACTERISTICS OF SURFACE MOUNT PACKAGES

John A. O'Connor

INTRODUCTION

Surface mount packaging continues to expand market share, displacing dual in-line packages (DIPs) at an ever increasing rate. Smaller surface mount devices allow a significant increase in circuit density with a corresponding decrease in system size. Miniaturization is not without penalty however, as thermal management can quickly dominate system packaging design.

With the familiar DIP, the majority of heat is removed through the case. Typically, this is accomplished by convection air currents, although forced air or conduction cooling is often used in more demanding applications. Unlike the DIP however, the majority of heat is removed from surface mount packages through the leads. This means that the PC board design directly affects the thermal capability of surface mounted circuitry. For optimal thermal design, the integrated circuit, the package, and the PC board must be considered as a system.

Many designers use steady-state thermal behavior (thermal resistance) to predict IC junction temperature. While this approach certainly is valid for devices subjected to continuous power dissipation, it often results in an overly conservative design when dissipation varies over time. Generating a model which accounts for transient thermal behavior allows the designer to fully exploit the system's thermal mass. Instantaneous junction temperature can then be calculated, insuring reliability with minimal system size.

THERMAL MODEL

Figure 1 shows the basic model which is expanded for more complex situations. The power dissipated is represented by the current source. Resistance to heat flow is represented by the resistor, and the thermal mass is represented by the capacitor. The analogous thermal units for the current, thermal resistance, and thermal capacitance are also shown in figure 1. Ground is ambient temperature, so all values are temperature rise above ambient. With more complex systems, it is usually easiest to initially convert to electrical units, analyze the circuit, then convert back to thermal units. This approach allows standard electrical circuit analysis tools and techniques to be used without unnecessary confusion.

A surface mounted device on a PC board can be modeled as in figure 2. Each R-C section roughly

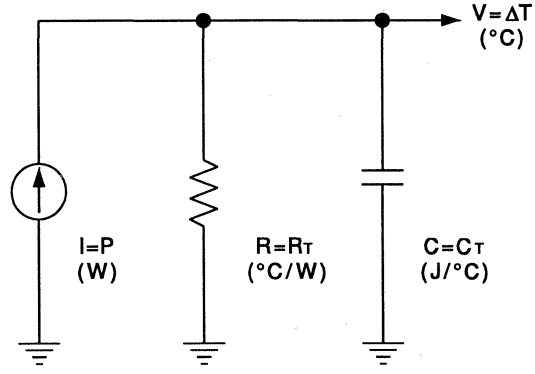


Figure 1. Basic Thermal Model

correlates to the physical system. The first R-C is the device die. The second is the lead frame and package, and the third is the PC board. Other parameters such as the junction to case and case to ambient thermal resistances, are lumped into the three R-C sections. This simplification does cause transient thermal response errors, although normally these errors are small. The additional elements can be broken out separately if greater accuracy is required. Although the physical correlation is far from perfect for the 3 R-C model, the thermal correlation can be very good.

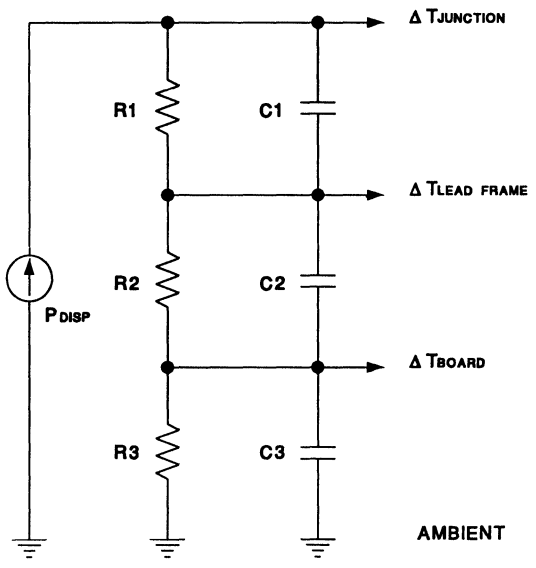


Figure 2: Surface Mounted Device on a PC Board Model

PARAMETER MEASUREMENT

The circuit technique shown in figure 3 can be used to evaluate the thermal performance of almost any IC. Device power dissipation must be known and constant. This is achieved with resistive loading for devices such as voltage regulators or amplifiers. Other devices may require additional circuitry to insure constant dissipation.

The change in forward voltage of a diode is typically utilized for temperature measurement, although any temperature dependant parameter could also be used. Ideally, the diode should be close to the output transistors for maximum accuracy. In practice, this is not critical since the temperature drop across the die will only be a few degrees C in a surface mountable IC. During the test, the measurement diode must not have any current other than the fixed bias current. The bias current should be as small as possible to avoid self-heating the diode.

Many devices have a diode intended for forward biased operation in the actual application circuit such as an output stage clamping diode. If such a diode is not available it may be necessary to forward bias a parasitic diode for measurement. While this approach should be considered a last resort, it can yield acceptable data. If a parasitic diode is forward biased, erratic or unspecified behavior is likely, even with low bias currents. Evaluate the test circuit carefully, insuring that dissipation is constant over the measurement temperature range.

Kelvin all connections to avoid interconnect voltage drops. Every 2mV is approximately 1°C, so even small DC offsets can cause significant error. Without any power applied to the device other than the diode bias current, characterize the diode's forward voltage in an oven at several temperatures over the expected operating junction temperature range. The slope of a best-fit line gives the thermal coefficient (T_C) which is used in subsequent calculations.

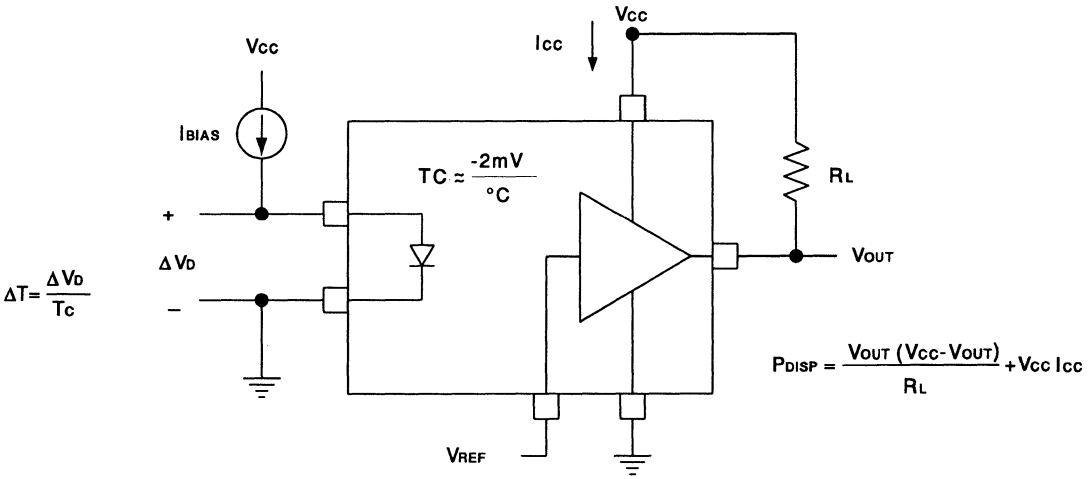


Figure 3: Typical Thermal Test Circuit

Thermocouples are used to sense PC board and ambient temperature. PC board temperature is measured as close to the device as possible.

Some parameters are measured directly while others are derived by curve fitting. Junction to PC board, and PC board to ambient thermal resistance are measured by dissipating a constant power. Allow 15 minutes for the temperature to stabilize. The change in diode forward voltage and PC board temperature give the junction to ambient and board to ambient thermal resistance:

$R_{(j-a)} = \Delta V_D / (T_C P_{DISP})$
$R_{(b-a)} = \Delta T_B / P_{DISP}$

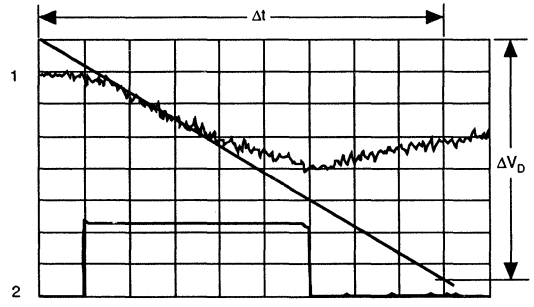
Note that these resistances are based on change in temperature - ambient is assumed constant for the duration of the test. These values correlate to R1, R2, and R3 by:

$$R1 + R2 = R_{(j-a)} - R_{(b-a)} \quad (1)$$

$$R3 = R_{(b-a)} \quad (2)$$

The thermal capacitance of the die is measured by applying a pulsed load and recording the junction temperature waveform. Varying the dissipation pulse width allows observation of each capacitance's effect, although only the die's thermal capacitance can be measured directly. A typical 10ms transient dissipation waveform is shown in figure 4. The thermal time constant of the die is on the order of 30ms. To minimize exponential decay error, the slope of the waveform is measured at (t) = 3ms. The die's thermal capacitance is then:

$$C1 = P_{DISP}\, \Delta t\, T_C / \Delta V_D \quad (3)$$



VERTICAL: (1) V_D, 1mV/DIV
(2) P_{DISP}, 1w

HORIZONTAL: 2ms/DIV

Figure 4: 10ms Transient Dissipation Waveform

Transient waveforms should also be taken for 100ms, 1s, and 10s dissipation intervals to generate an accurate temperature versus time curve. If transient thermal behavior is critical beyond 10 seconds then additional curves must be taken. The thermal time constant of the PC board can go out to several minutes, so a strip chart recorder or computer based data acquisition system will be required. For most systems, this additional data is unnecessary.

The remaining parameters are determined by curve fitting. Visual comparison of measured versus calculated curves is easily done with a spread sheet program. Measured junction temperature versus time data (4 points per decade is sufficient) is entered into the spread sheet. Junction temperature is then calculated at each point with estimated values for R2 and C2 and C3 using:

$$T(t) = P_{DISP}\,[R1(1-e^{-t/\tau 1}) + R2(1-e^{-t/\tau 2}) + R3(1-e^{t/\tau 3})] \quad (4)$$

Data presented in the following section will help in estimating initial values. This procedure is iterated until an acceptable curve fit is achieved. C3's value is iterated only if the measured curve goes out to several minutes. Figure 5 is a typical measured and calculated junction temperature versus time curve. A logarithmic time axis aids in curve fitting by spreading data points evenly.

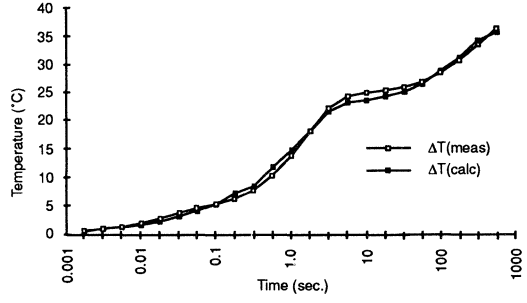


Figure 5: Junction Temperature versus Time for FQP48 Package Dissipating 1W.

Typical Data

The preceding technique was used to characterize two devices in nine different packages. Five different PC board types were also tested to provide relative comparison. This information should be used to help initially determine package, PC board type, and layout. It must be stressed that this typical data should not substitute for a rigorous thermal analysis of the actual application.

PACKAGE	R1 (°C/W)	C1 (J/°C)	τ1 (sec)	R2 (°C/W)	C2 (J/°C)	τ2 (sec)	R3 (°C/W)	C3 (J/°C)	τ3 (sec)	R(J-a) (°C/W)
D8	5	0.0035	0.02	64	0.030	1.9	15	24	360	84
D14	4	0.0045	0.02	45	0.035	1.6	16	24	384	65
DW16	4	0.0045	0.02	44	0.070	3.1	15	24	360	63
DW16	4	0.011	0.04	34	0.11	3.7	13	24	312	51
DWP28	2.5	0.008	0.02	13	0.13	1.7	15	24	360	30
Q20	3	0.010	0.03	26	0.12	3.1	14	24	336	43
Q28	2.5	0.008	0.02	25	0.12	2.9	13	24	312	40
QP28	2.5	0.009	0.02	12	0.25	3.0	14	24	336	28
FQ48	4	0.006	0.02	57	0.07	4.0	15	24	360	76
FQP48	4	0.005	0.02	21	0.08	1.7	14	25	350	39

Figure. 6 Model values Versus Package Type for 1W Dissipation on Aluminum PC Board.

Figure 6 shows model values and time constants versus package type, mounted on an aluminum PC board [1]. Junction to ambient thermal resistance is also shown to indicate overall steady state thermal performance. All data was taken with one watt dissipated. The values that were determined by curve fitting result in a fairly conservative model. Values were chosen which tended predict higher temperature than actually measured where errors could not be eliminated. As indicated, two devices were used for testing. At 7,500 square mils, the UC3730 is representative of the smaller dies typically packaged in D8, D14, and DW16 packages. The UC3173 is 16,500 square mils, and is typical of the dies packaged in the other larger packages.

Both devices were packaged in the DW16 to isolate the effect of die size. The UC1730's smaller die increase R2 by about 30%. Interpolating between these two data points is difficult since the relationship between die size and thermal resistance is nonlinear. Curves are available which account for this dimensional difference [2], although the actual conditions differ and are more complicated than the configuration used to generate the curves. Fortunately, the resulting error will be small in most applications. Conservatively estimating R2 will minimally impact system size, but if a more accurate value is required the actual device can be characterized on a test PC board.

Figure 7 illustrates the power lead frame's dramatic improvement in thermal performance over standard lead frames by comparing the junction to ambient thermal resistances of the QP28 to the Q28, and the FQP48 to the FQ48. Standard lead frames connect the die to the leads thermally through the epoxy molding compound. Power lead frame packages incorporate a single piece for die attachment and ground leads. This uninterrupted, high thermal conductivity path offers a significant improvement over standard lead frames. Occasionally a stiffer but less conductive alloy is use for standard lead frames. The FQ48's poorer thermal performance is partially caused by the lower conductivity alloy.

Printed circuit board design significantly affects the overall thermal performance of the system, particularly with the power lead frame packages. The UC3173 in the DWP28 package was used to

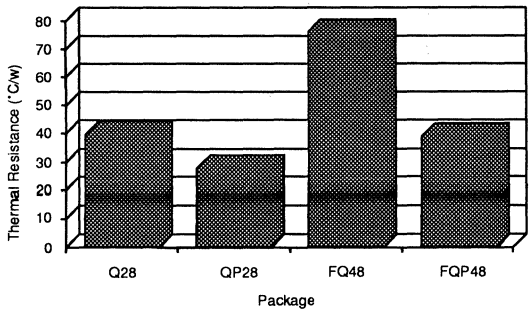


Figure 7: Power lead frames significantly reduce thermal resistance.

compare PC board thermal performance. Five different PC board types were evaluated with one watt dissipated:

1. Single side 1 oz. copper, 0.062 aluminum
2. Single side 1 oz. copper, 0.062 FR4 epoxy fiberglass
3. Single side 2 oz. copper, 0.062 FR4 epoxy fiberglass
4. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.031 FR4 epoxy fiberglass
5. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.062 FR4 epoxy fiberglass

PCB TYPE	R(b-a) (°C/ W)	C(b-a) (J/°C)	τ (sec)
Aluminum	15	24	360
FR4 -1oz.	31	2.5	78
FR4 -2oz.	25	3	74
4 layer - 0.031	21	4	84
4 layer - 0.062	19	5	94

Figure. 8 Board to ambient thermal resistance and capacitance versus PC board type for DWP28 package dissipating 1W.

The thermal resistance, capacitance, and time constants for the five PC boards are shown in figure 8. The PC board layouts used for testing are shown in figure 9. Only the component side is shown for the four layer boards. The back side, which has 10 mil traces on 50 mil centers to provide a typical amount of interconnect copper, and the Vcc plane were unconnected. The inner ground plane is connected to the small component side ground plane through 16 feed-throughs.

As expected, the aluminum PC board's significantly higher specific heat results in nearly an order of magnitude increase in thermal capacitance. Surprisingly the four layer 0.062 board's thermal resistance is nearly as low as the aluminum board's, indicating good heat distribution through the inner planes. Note that although the Vcc plane is unconnected, it does help distribute the heat across the board. Conduction or forced air cooling is necessary to fully exploit the aluminum board's capability.

Summary

A method for accurately modeling the thermal behavior of a surface mounted IC has been presented. The model relies on measured data, insuring excellent correlation to the physical system. Typical thermal behavior of nine different packages and five different PC boards were also presented, indicating relative thermal performance differences. Optimum thermal system design is achievable using the techniques and data presented.

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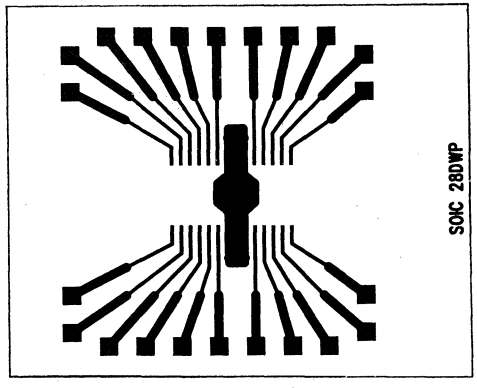
1. Thermal Clad insulated metal substrates, The Bergquist Company, 5300 Edina Industrial Blvd., Minneapolis, MN 55439, 612-835-2322
2. R. Tummala, E. Rymaszewski, "Micro-electronics Packaging Handbook", Van Nostrand Reinhold, 1989, pp173-179

4 Layer-Component Side



Single Sided

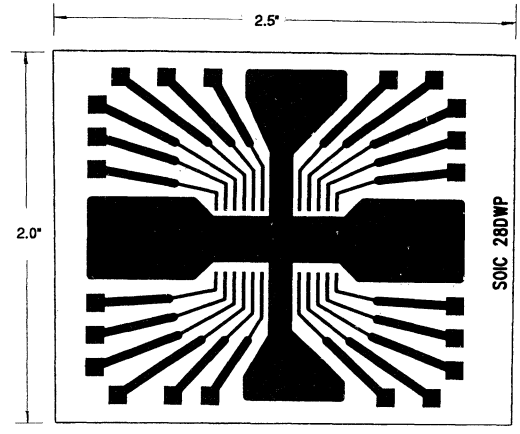
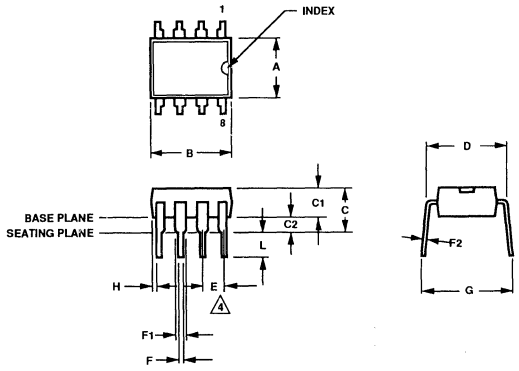


Figure 9. Test PC Board Layouts (SOIC 28DWP)

PACKAGING INFORMATION

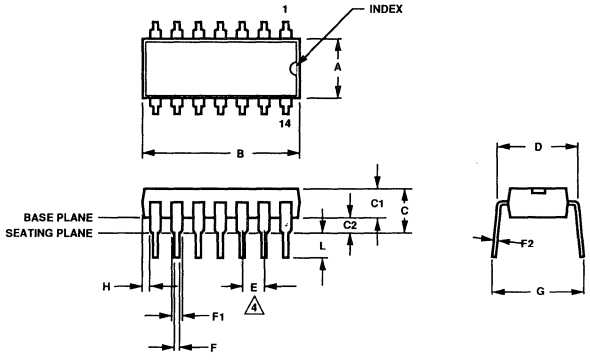
8-PIN PLASTIC
N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



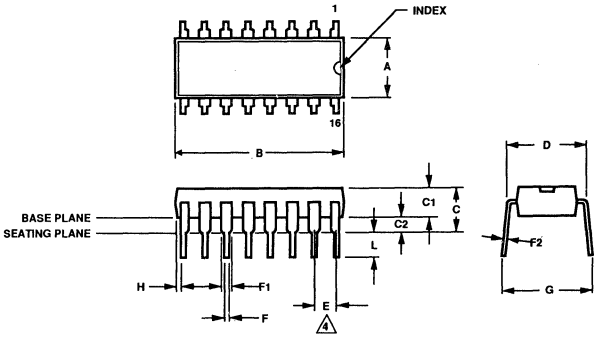
14-PIN PLASTIC
N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



16-PIN PLASTIC
N PACKAGE SUFFIX

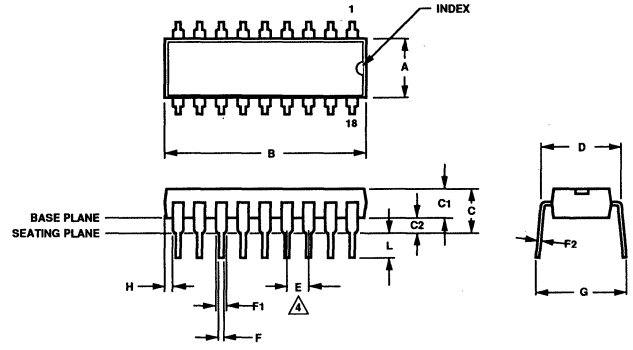
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



PACKAGING INFORMATION

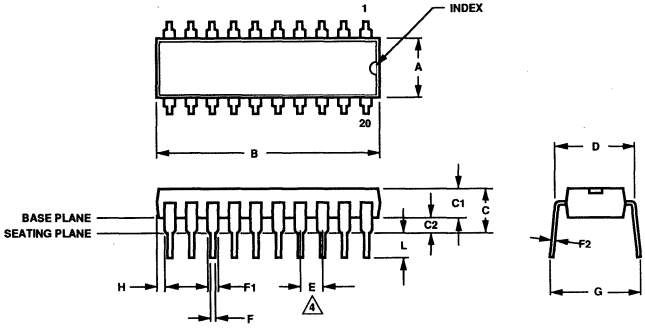
18-PIN PLASTIC
N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



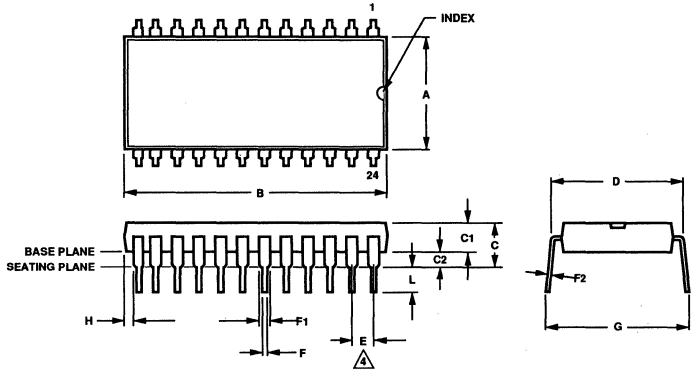
20-PIN PLASTIC
N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	1.010	1.030	25.65	26.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



24-PIN PLASTIC
N PACKAGE SUFFIX

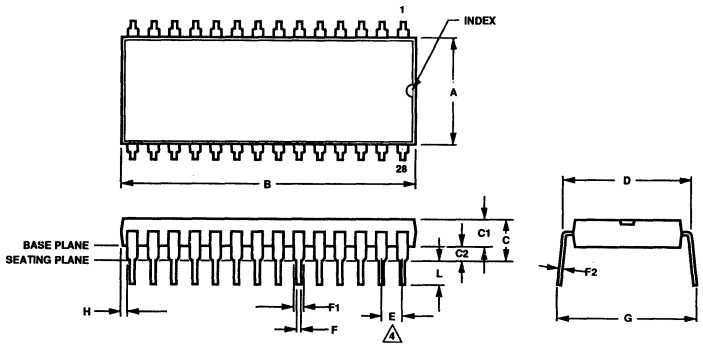
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.230	1.270	31.24	32.26	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



PACKAGING INFORMATION

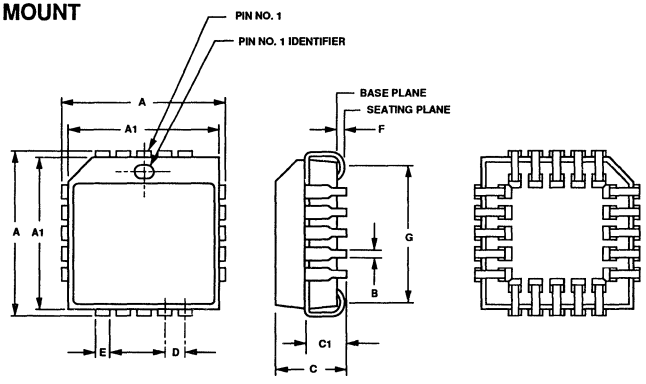
28-PIN PLASTIC
N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.380	1.470	35.10	37.34	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



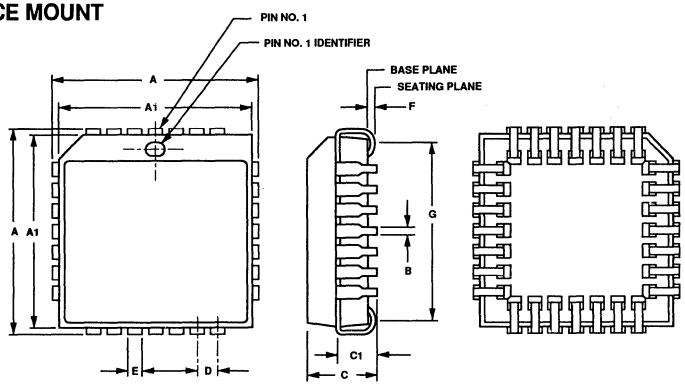
20-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.290	.330	7.37	8.38	



28-PIN PLASTIC PLCC SURFACE MOUNT
Q PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.485	.495	12.32	12.57	
A1	.450	.456	11.43	11.53	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.390	.430	9.91	10.92	

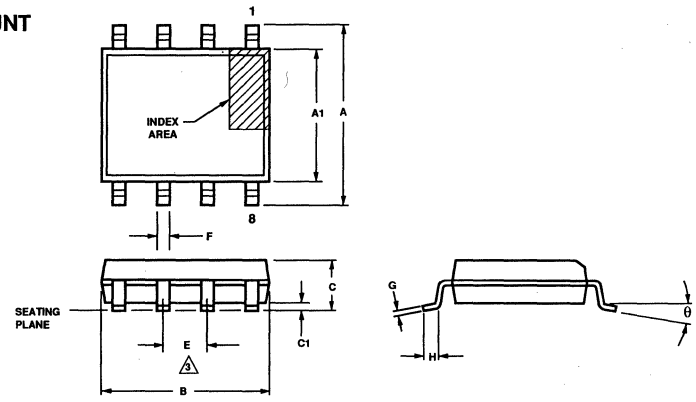


8

PACKAGING INFORMATION

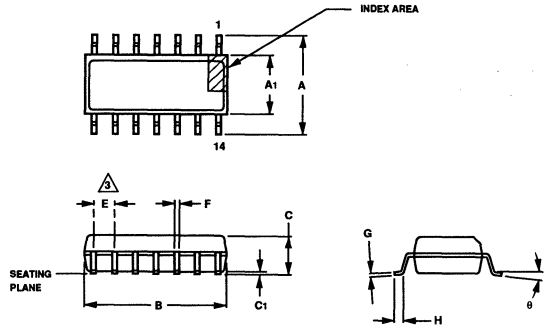
8-PIN SOIC SURFACE MOUNT
D PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



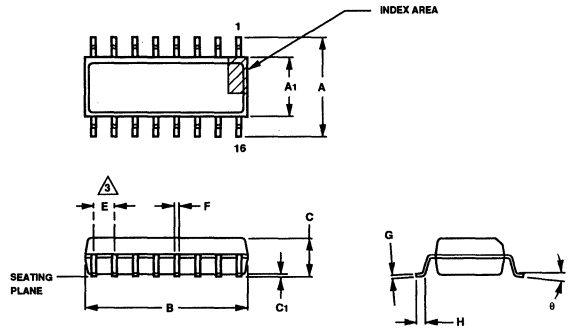
14-PIN SOIC SURFACE MOUNT
D PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



16-PIN SOIC SURFACE MOUNT
D PACKAGE SUFFIX

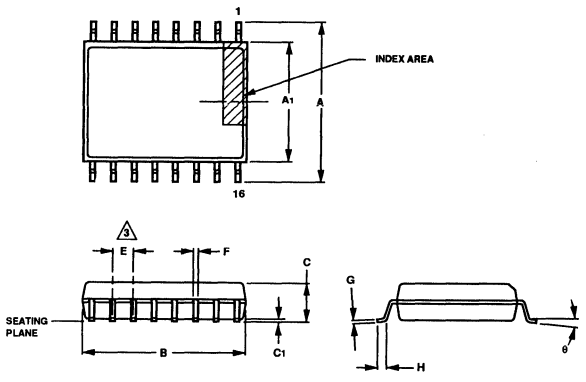
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



PACKAGING INFORMATION

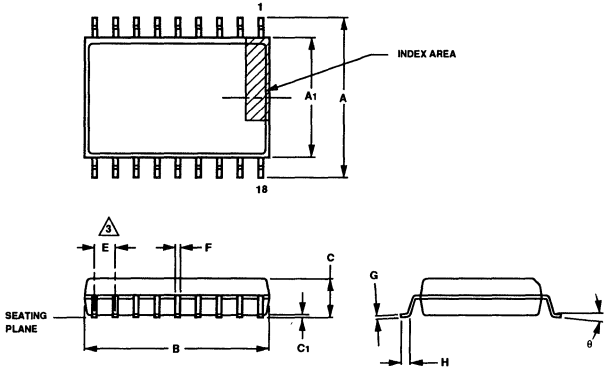
16-PIN SOIC SURFACE MOUNT
DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



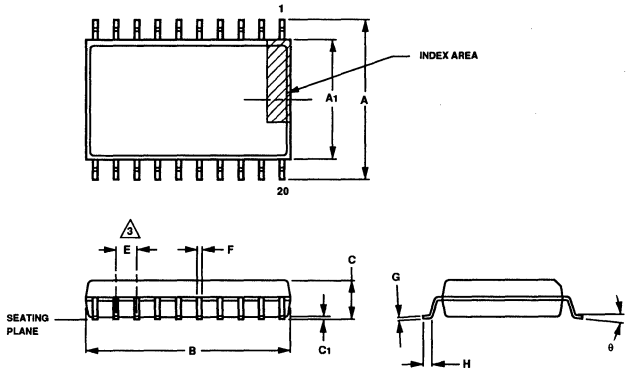
18-PIN SOIC SURFACE MOUNT
DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



20-PIN SOIC SURFACE MOUNT
DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

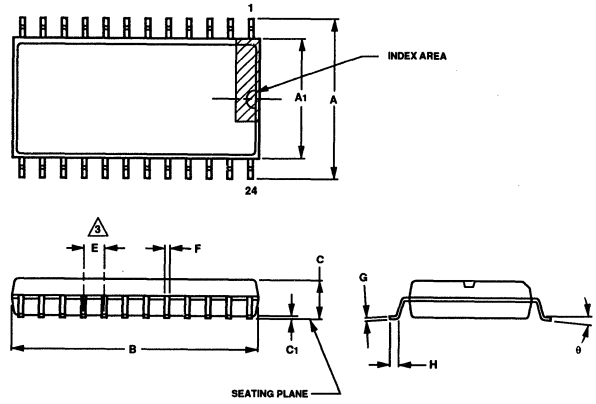


8

PACKAGING INFORMATION

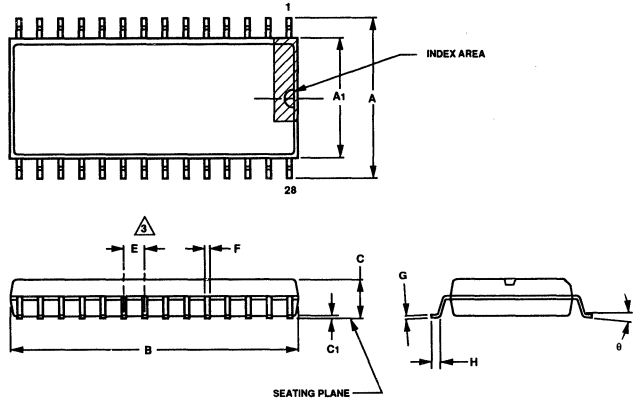
24-PIN SOIC SURFACE MOUNT
DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.598	.606	15.20	15.40
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.019	.035	0.46	0.89
θ	0°	8°	0°	8°



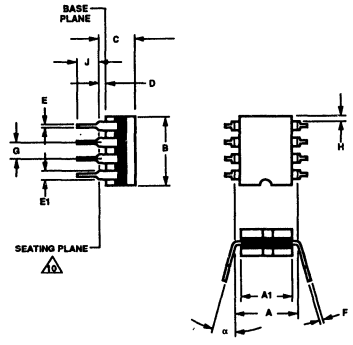
28-PIN SOIC SURFACE MOUNT
DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.698	.706	17.73	17.93
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



8-PIN CERAMIC
J PACKAGE SUFFIX

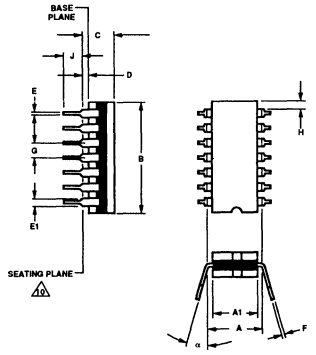
DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.290	0.320	7.37	8.13	7
0.220	0.310	5.59	7.87	4
—	0.405	—	10.29	4
—	0.200	—	5.08	
0.015	0.060	0.38	1.52	3
0.014	0.026	0.36	0.66	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.008	—	0.13	—	6
0.125	0.200	3.18	5.08	
0°	15°	0°	15°	



PACKAGING INFORMATION

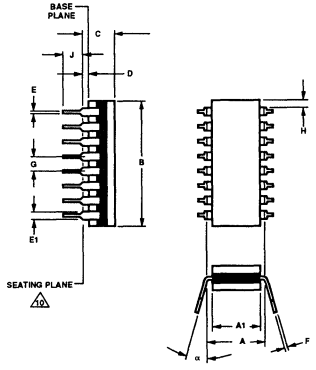
14-PIN CERAMIC J PACKAGE SUFFIX

DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.290	0.320	7.37	8.13	7
0.220	0.310	5.59	7.87	4
—	0.785	—	19.94	4
—	0.200	—	5.08	
0.015	0.060	0.38	1.52	3
0.014	0.026	0.36	0.66	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.005	—	0.13	—	6
0.125	0.200	3.18	5.08	
0°	15°	0°	15°	



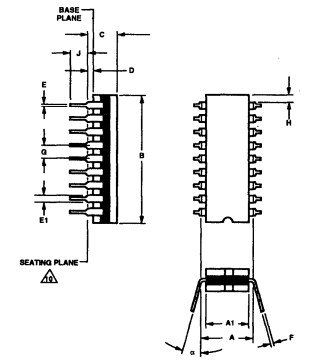
16-PIN CERAMIC J PACKAGE SUFFIX

DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.290	0.320	7.37	8.13	7
0.220	0.310	5.59	7.87	4
—	0.840	—	21.34	4
—	0.200	—	5.08	
0.015	0.060	0.38	1.52	3
0.014	0.026	0.36	0.66	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.005	—	0.13	—	6
0.125	0.200	3.18	5.08	
0°	15°	0°	15°	



18-PIN CERAMIC J PACKAGE SUFFIX

DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.290	0.320	7.37	8.13	7
0.220	0.310	5.59	7.87	4
—	0.960	—	24.38	4
—	0.200	—	5.08	
0.015	0.060	0.38	1.52	3
0.014	0.023	0.36	0.58	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.005	—	0.13	—	6
0.125	0.200	3.18	5.08	
0°	15°	0°	15°	

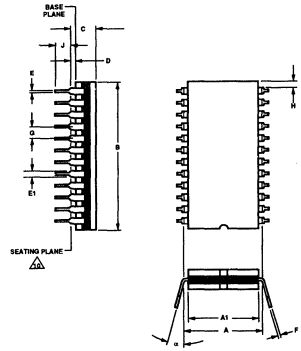


8

PACKAGING INFORMATION

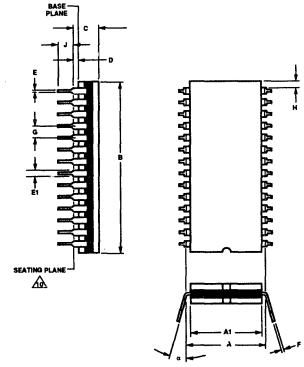
24-PIN CERAMIC
J PACKAGE SUFFIX

DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.590	0.625	14.99	15.88	7
0.515	0.605	13.08	15.37	4
1.180	1.260	29.97	32.00	4
—	0.225	—	5.72	
0.015	0.055	0.38	1.40	3
0.014	0.026	0.36	0.66	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.005	0.065	0.127	1.65	6
0.125	0.200	3.18	5.08	
0°	15°	0°	15°	



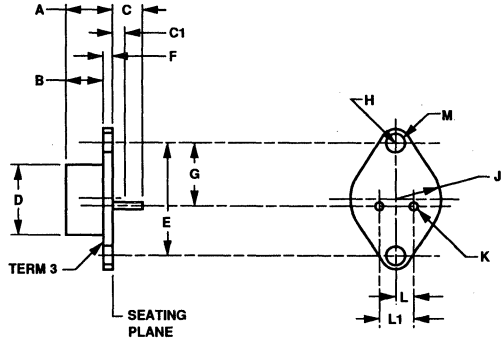
28-PIN CERAMIC
J PACKAGE SUFFIX

DIMENSIONS				
INCHES		MILLIMETERS		NOTES
MIN	MAX	MIN	MAX	
0.590	0.625	14.99	15.88	7
0.570	0.605	14.48	15.37	4
1.380	1.460	35.05	37.08	4
—	0.225	—	5.72	
0.015	0.055	0.38	1.40	3
0.015	0.026	0.38	0.66	8
0.045	0.065	1.14	1.65	2
0.008	0.018	0.20	0.46	8
0.100 BSC		2.54 BSC		5
0.005	0.065	0.127	1.65	6
0.125	0.200	3.167	5.08	
0°	15°	0°	15°	



3-PIN TO-3 METAL*
K PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.250	.285	6.35	7.24	
B	.190	.230	4.83	5.84	
C	.430	.470	10.92	11.94	4
C1	–	.050	–	1.27	3, 4
D	.765	.875	19.43	22.26	
E	1.177	1.197	29.90	30.40	
F	.060	.065	1.52	1.65	
G	.655	.675	16.64	17.14	
H	.169	.176	4.29	4.47	
J	.495	.505	12.57	12.82	
K	.038	.040	0.97	1.02	3, 7
L	.205	.225	5.21	5.72	
L1	.420	.440	10.67	11.18	
M	.152	.160	3.89	4.06	5, 6

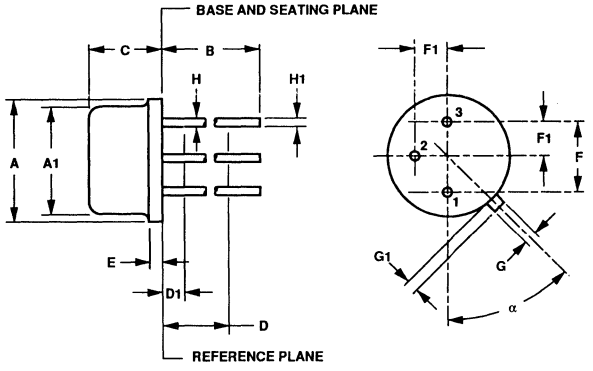


*Consult factory for availability.

PACKAGING INFORMATION

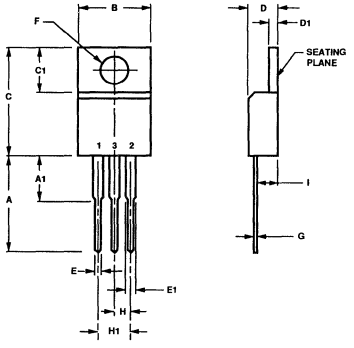
3-PIN TO-5 METAL*
H PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.335	.370	8.51	9.40	
A1	.305	.335	7.75	8.51	
B	.500	–	12.70	–	
C	.165	.185	4.19	4.70	
D	.250	–	6.35	–	3
D1	–	.050	–	1.27	3
E	–	.040	–	1.02	
F	.200 BSC		5.08 BSC		
F1	.100 BSC		2.54 BSC		
G	.028	.034	0.71	0.86	
G1	.029	.045	0.74	1.14	4
H	.016	.019	0.41	0.48	3
H1	.016	.021	0.41	0.53	3
α	45° BSC		45° BSC		



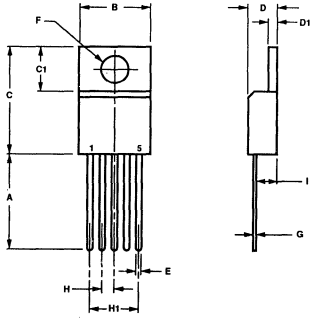
3-PIN TO-220 PLASTIC
T PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A1	–	.250	–	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E1	.045	.070	1.14	1.77
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.090	.110	2.29	2.79
H1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



5-PIN TO-220 PLASTIC
T PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D1	.045	.055	1.14	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.057	.077	1.45	1.96
H1	.258	.278	6.55	7.06
I	.080	.115	2.03	2.92

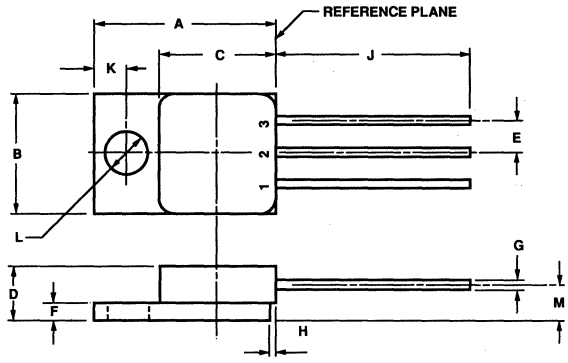


*Consult factory for availability.

PACKAGING INFORMATION

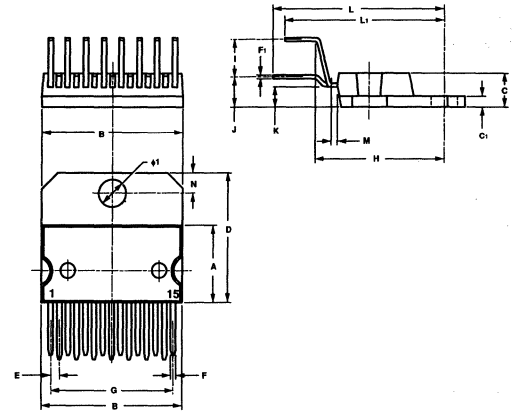
3-PIN TO-257 HERMETIC *
G PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.645	.665	16.38	16.89	
B	.410	.420	10.41	10.62	
C	.410	.430	10.41	10.92	
D	.190	.200	4.83	5.06	
E	.100 BSC		.254 BSC		2
F	.035	.045	0.89	1.14	
G	.027	.035	0.69	0.89	
H	–	.010	–	0.25	
J	.500	–	12.70	–	
K	.115	.121	2.92	3.07	
L	.140	.150	3.56	3.81	DIA.
M	.120 BSC		3.05 BSC		3



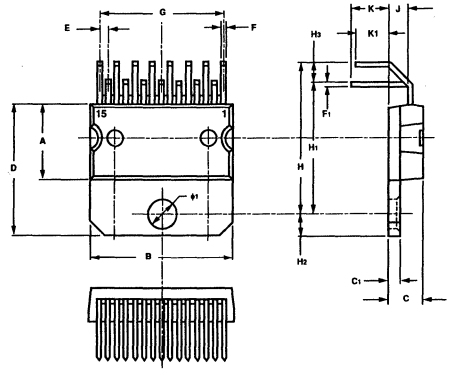
15-PIN VERTICAL MULTIWATT
V PACKAGE SUFFIX

DIMENSIONS						
SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	.413	.417	.421	10.50	10.60	10.70
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.43	4.50	4.58
C_1	.059	.060	.061	1.49	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.038	.050	.062	0.97	1.27	1.57
F	.026	.028	.029	0.66	0.70	.072
F_1	.019	.020	.021	0.50	0.52	0.54
G	.688	.700	.712	17.48	17.78	18.08
H	.699	.704	.709	17.75	17.88	18.00
I	.197	.200	.207	4.75	5.08	5.25
J	.163	.169	.175	4.15	4.30	4.45
K	.089	.096	.104	2.25	2.45	2.65
L	.872	.880	.888	22.15	22.35	22.55
L_1	.870	.878	.886	22.10	22.30	22.50
M	–	.040	–	–	1.00	–
N	.108	.110	.112	2.75	2.80	2.83
ϕ_1	.147	.150	.151	3.73	3.80	3.82



15-PIN HORIZONTAL MULTIWATT
VH PACKAGE SUFFIX

DIMENSIONS						
	INCHES			MILLIMETERS		
	MIN	TYP	MIN	MAX	TYP	MAX
A	.413	.417	.421	10.50	10.60	10.70
B	.783	.787	.791	19.90	20.00	20.10
C	.174	.177	.180	4.43	4.50	4.58
C1	.059	.060	.061	1.49	1.52	1.54
D	.685	.689	.693	17.40	17.50	17.60
E	.038	.050	.062	0.97	1.27	1.57
F	.026	.028	.029	0.66	0.70	0.72
F1	.019	.020	.021	0.50	0.52	0.54
G	.688	.700	.712	17.48	17.78	18.08
H	.804	.810	.816	20.42	20.57	20.72
H1	.707	.713	.719	17.97	18.12	18.27
H2	.109	.110	.112	2.78	2.80	2.85
H3	.087	.096	.106	2.20	2.45	2.70
J	.089	.096	.104	2.25	2.45	2.65
K	.213	.219	.224	5.40	5.55*	5.70
K1	.205	.211	.217	5.20	5.35	5.50
φ	.147	.150	.151	3.73	3.80	3.82

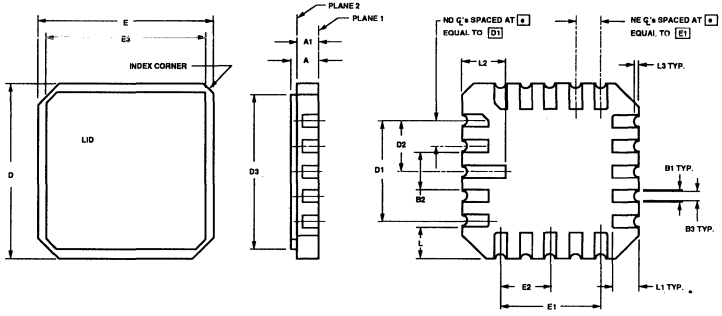


*Consult factory for availability.

PACKAGING INFORMATION

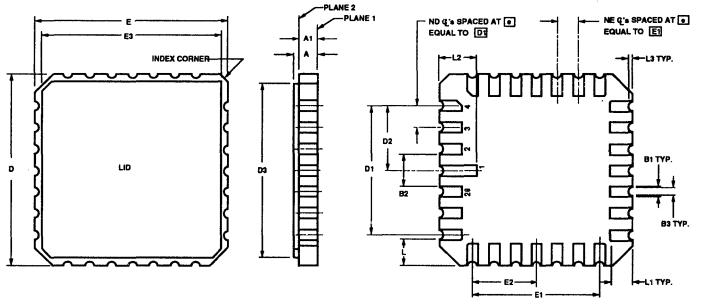
20-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	–	.358	–	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



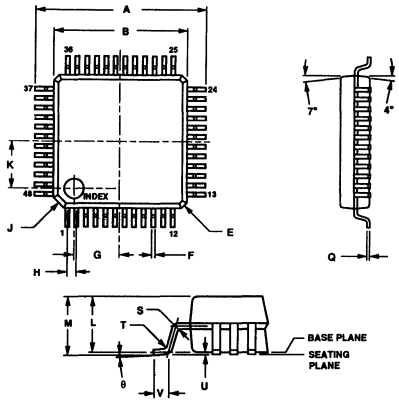
28-PIN CERAMIC LEADLESS SURFACE MOUNT
L PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	–	.460	–	11.68	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	28		28		2
ND/NE	7		7		2
e	.050 BSC		1.27 BSC		10



48-PIN TQFP
FQ PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.338	.370	8.60	9.40	SQ.
B	.272	.280	6.90	7.10	SQ.
E	.012		0.30		C. (3X)
F	.005	.009	0.13	0.23	
G	.094		2.40		REF.
H	.0197 BSC		0.50 BSC		2
J	.022		0.55		C.
K	.094		2.40		REF.
L	.051	.059	1.30	1.50	
M	–	.067	–	1.70	
Q	.0035	.008	0.09	0.20	
S	.0035	–	0.08	–	RAD.
T	.0035	.008	0.08	0.20	RAD.
U	.002	.006	0.05	0.15	3, 4
V	.012	.028	0.30	0.70	
θ	0°	10°	0°	10°	

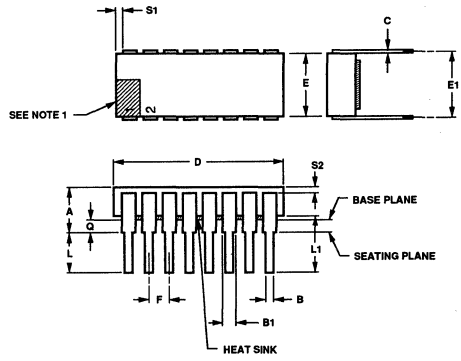


8

PACKAGING INFORMATION

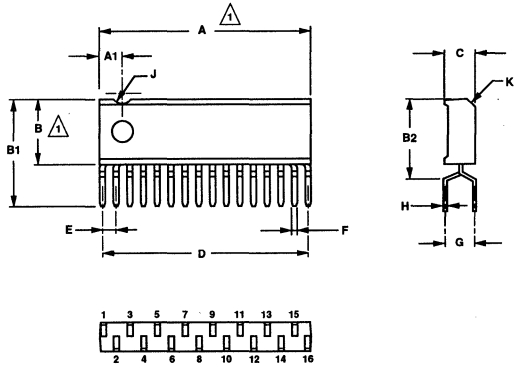
16-PIN SIDEBRAZE DIP
SP PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.200	–	5.08	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	.840	–	21.34	4
E	.220	.310	5.59	7.78	4
E_1	.290	.320	7.37	8.13	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	



16-PIN ZIG-ZAG IN-LINE
Z PACKAGE SUFFIX

DIMENSIONS					
	MILLIMETERS		INCHES		NOTES
	MIN	MAX	MIN	MAX	
A	19.40	19.60	.764	.772	
A1	–	2.00	–	.039	
B	5.70	5.90	.224	.232	
B1	9.40	10.40	.370	.409	
B2	6.50	7.50	.256	.295	
C	2.70	2.90	.106	.114	
D	18.75	19.35	.738	.762	
E	1.07	1.47	.042	.058	
F	0.45	0.65	.018	.026	
G	2.50	3.00	.098	.118	
H	0.23	0.35	.009	.014	
J	1.00 BSC		.039 BSC		RAD.
K	1.00 BSC		.039 BSC		CHAM.



9

Application Notes


INTEGRATED
CIRCUITS
UNITRODE

INTEGRATED CIRCUITS
UNITRODE

APPLICATION/DESIGN NOTES
TABLE OF CONTENTS

9

APPLICATION/DESIGN NOTES
TABLE OF CONTENTS

A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

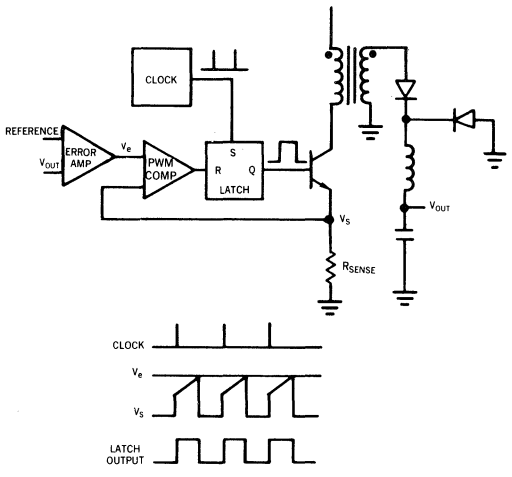


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

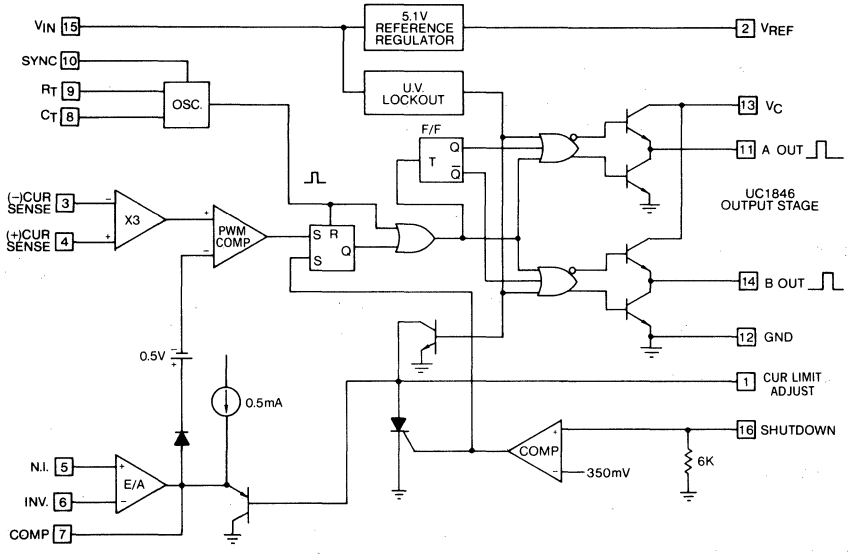


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz .
- An error amplifier with common mode range from ground to V_{cc}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

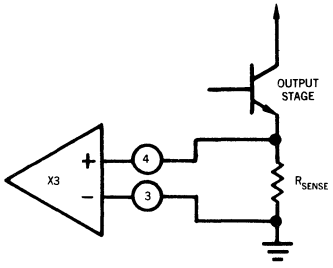
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

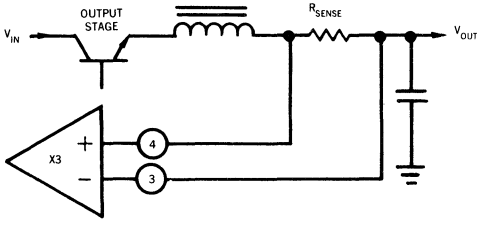
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

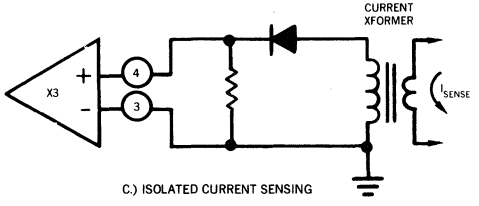
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

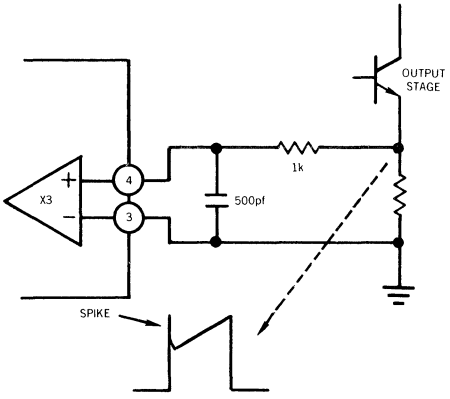


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stabillity and waveform clarity at frequencies in excess of 1MHz.

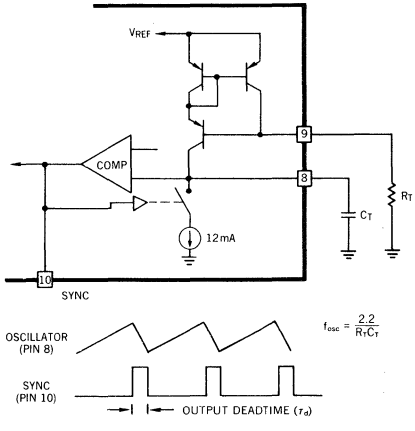


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

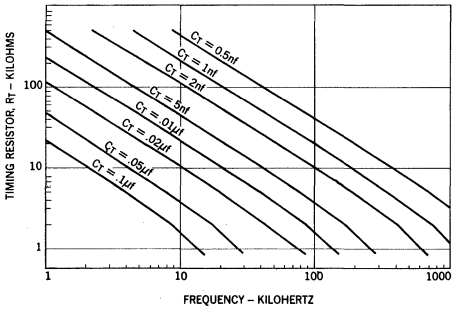


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

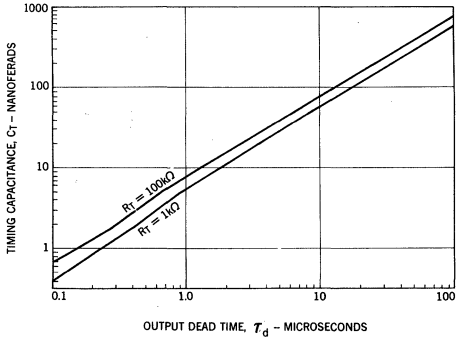


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

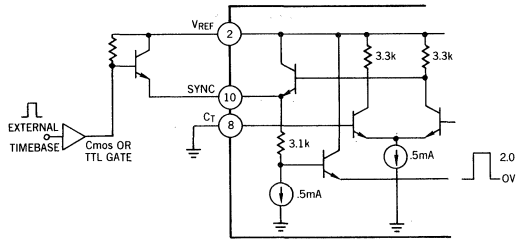


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

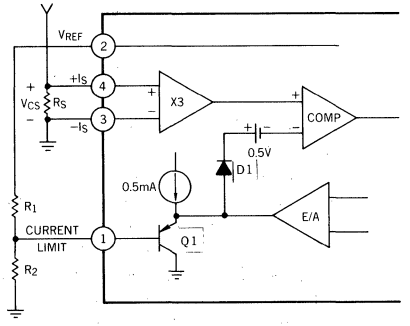


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ −0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2 (V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

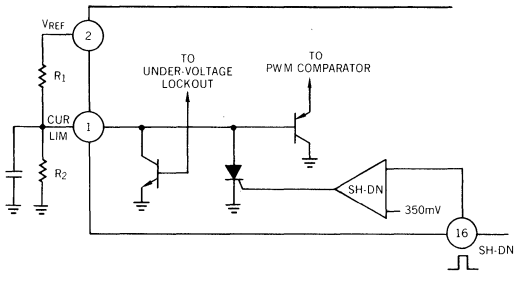


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

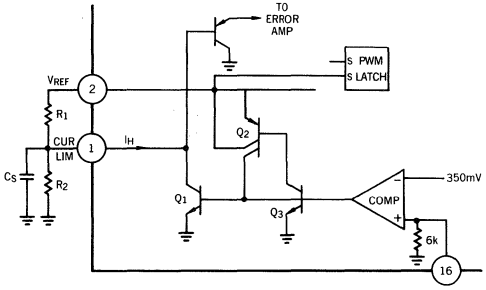


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

9

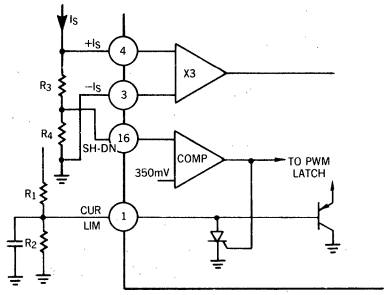


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4-6]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

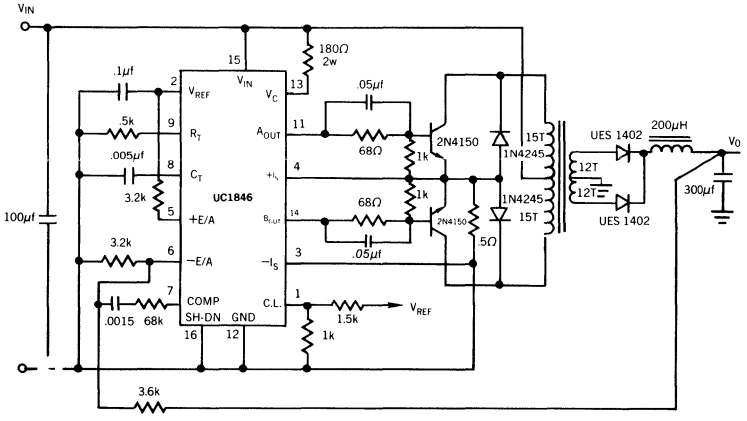
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, −E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

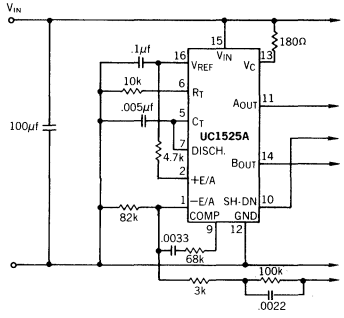
Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

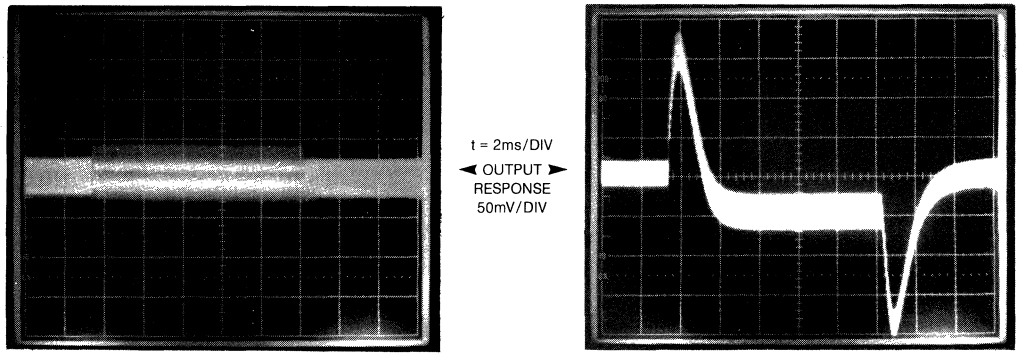


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR



(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS

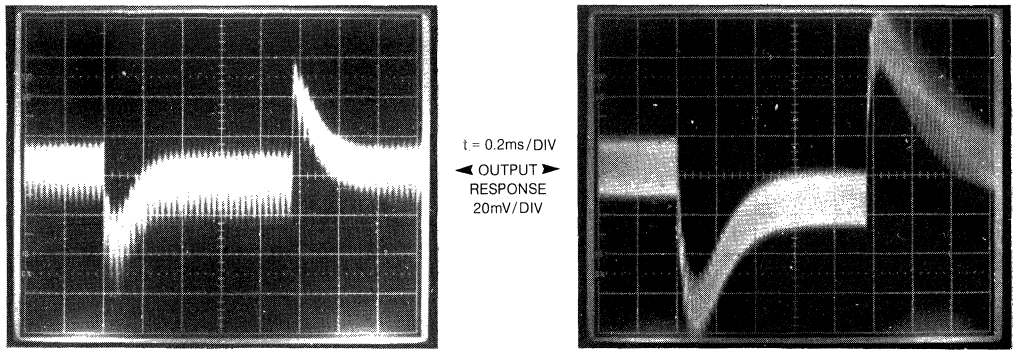


FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

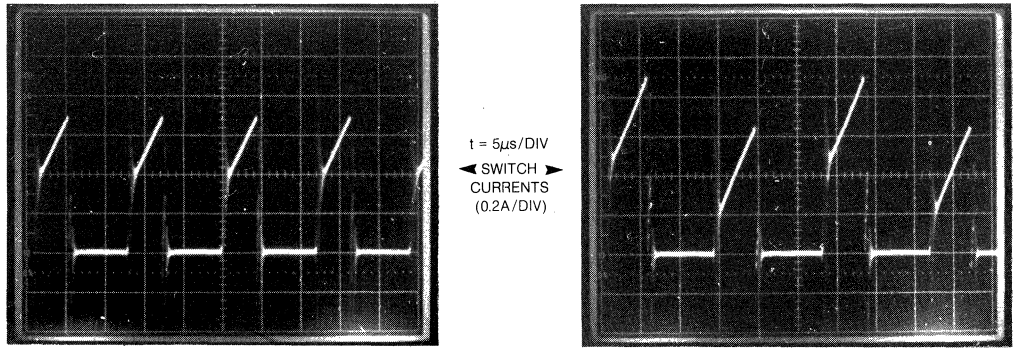


FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

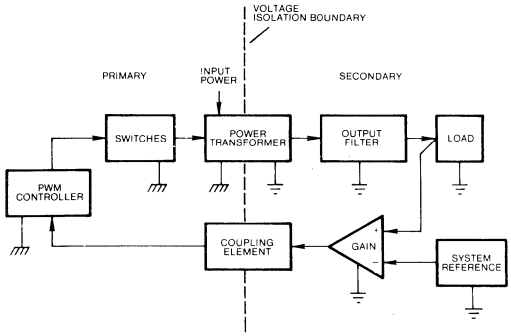


FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best undestood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

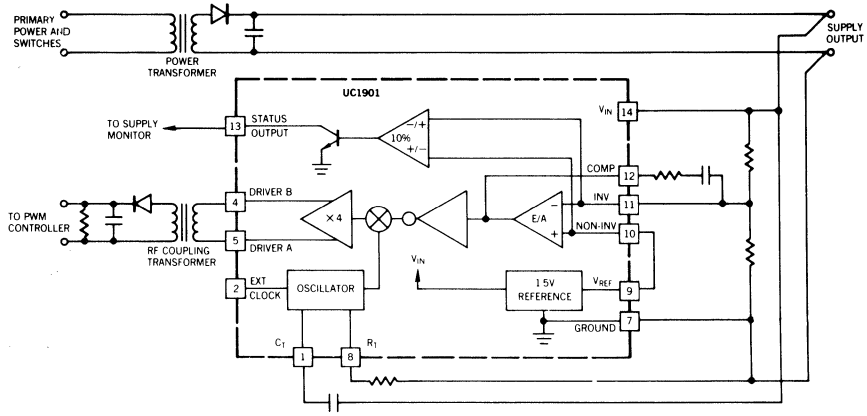


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

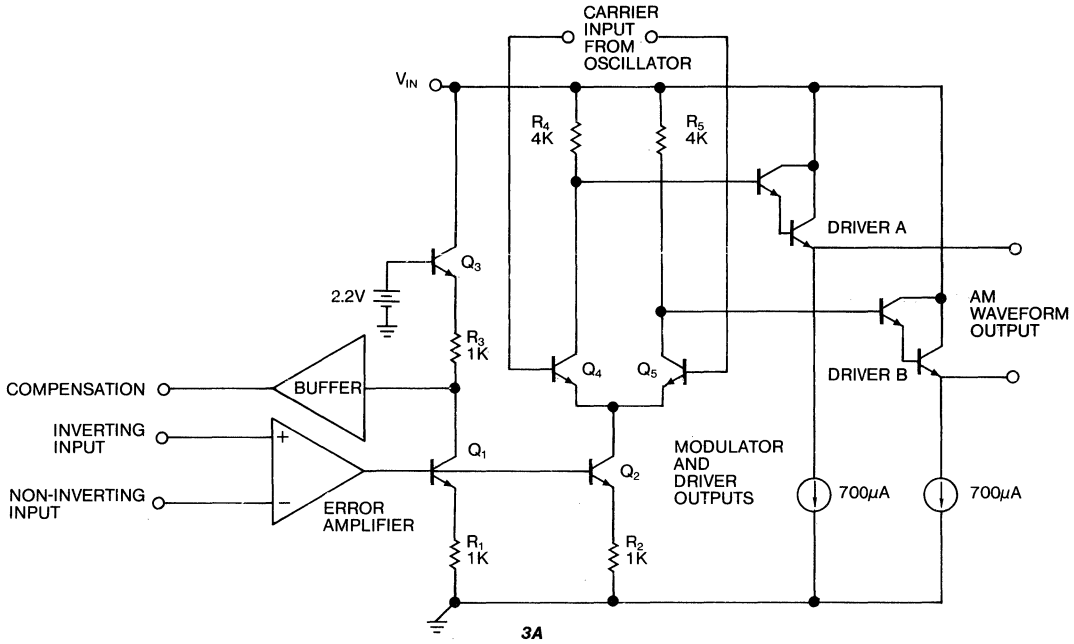


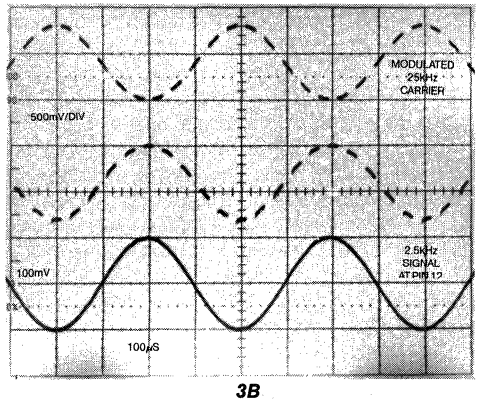
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward converters are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.



3B

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

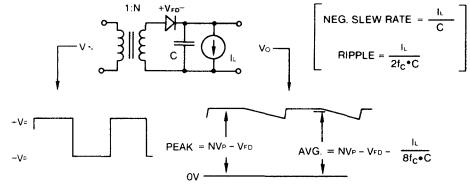


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

$$(1) \qquad L_M \geq \frac{V_P}{4 f_c I_P}$$

Where: L_M = the magnetizing inductance,
V_P = the peak carrier voltage across transformer inputs,
f_C = the UC1901 operating frequency,
I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

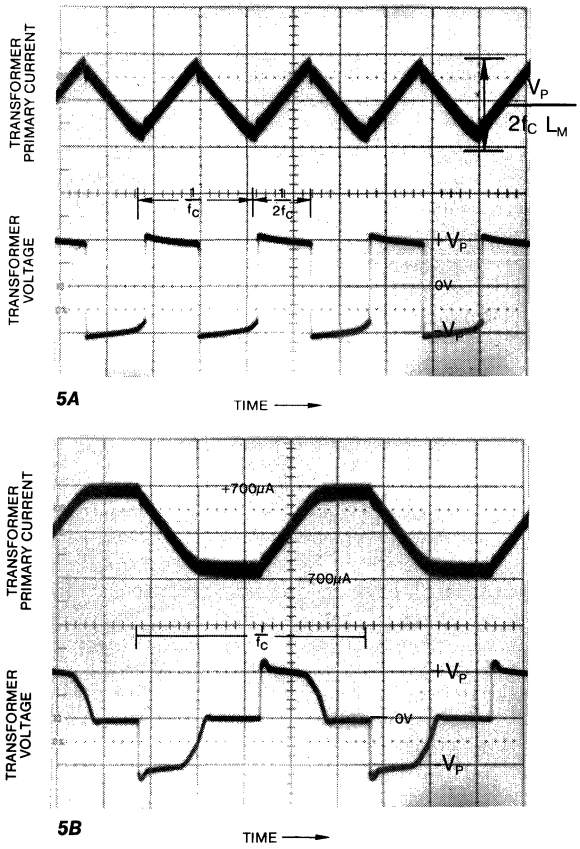


FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the >50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt.

When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 10kΩ. A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

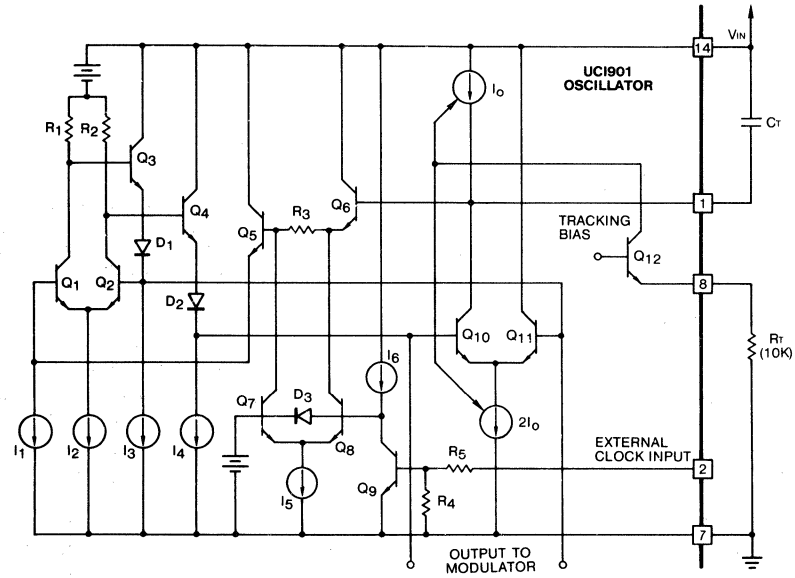


FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

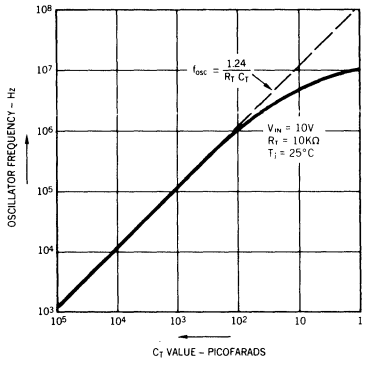


FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

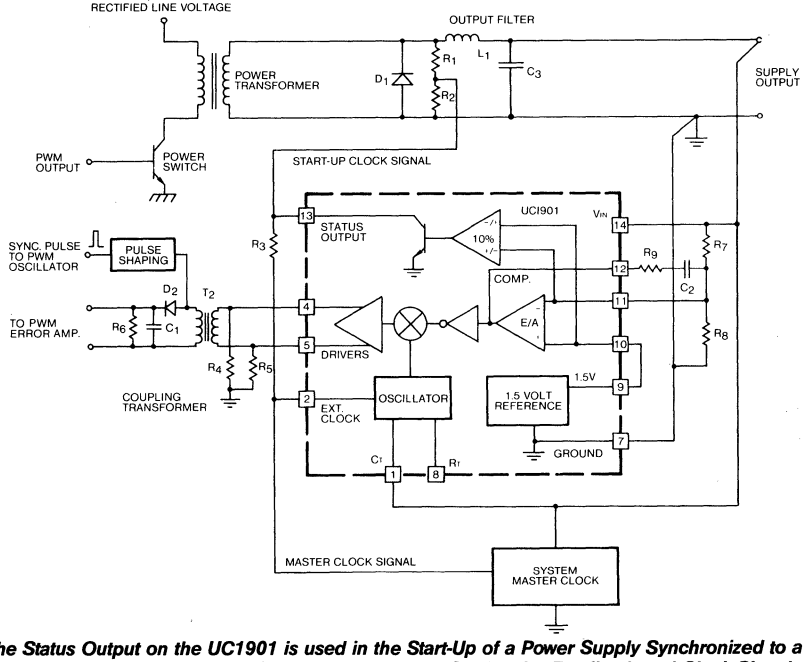


FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (< 150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3) \quad \frac{v_{OUT}}{v_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

V_{IN} = level of the rectified line voltage,

V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,

T_P = One period of the switching frequency,

L_M = Magnetizing inductance of the primary winding,

C_F = A total effective output filter capacitor,

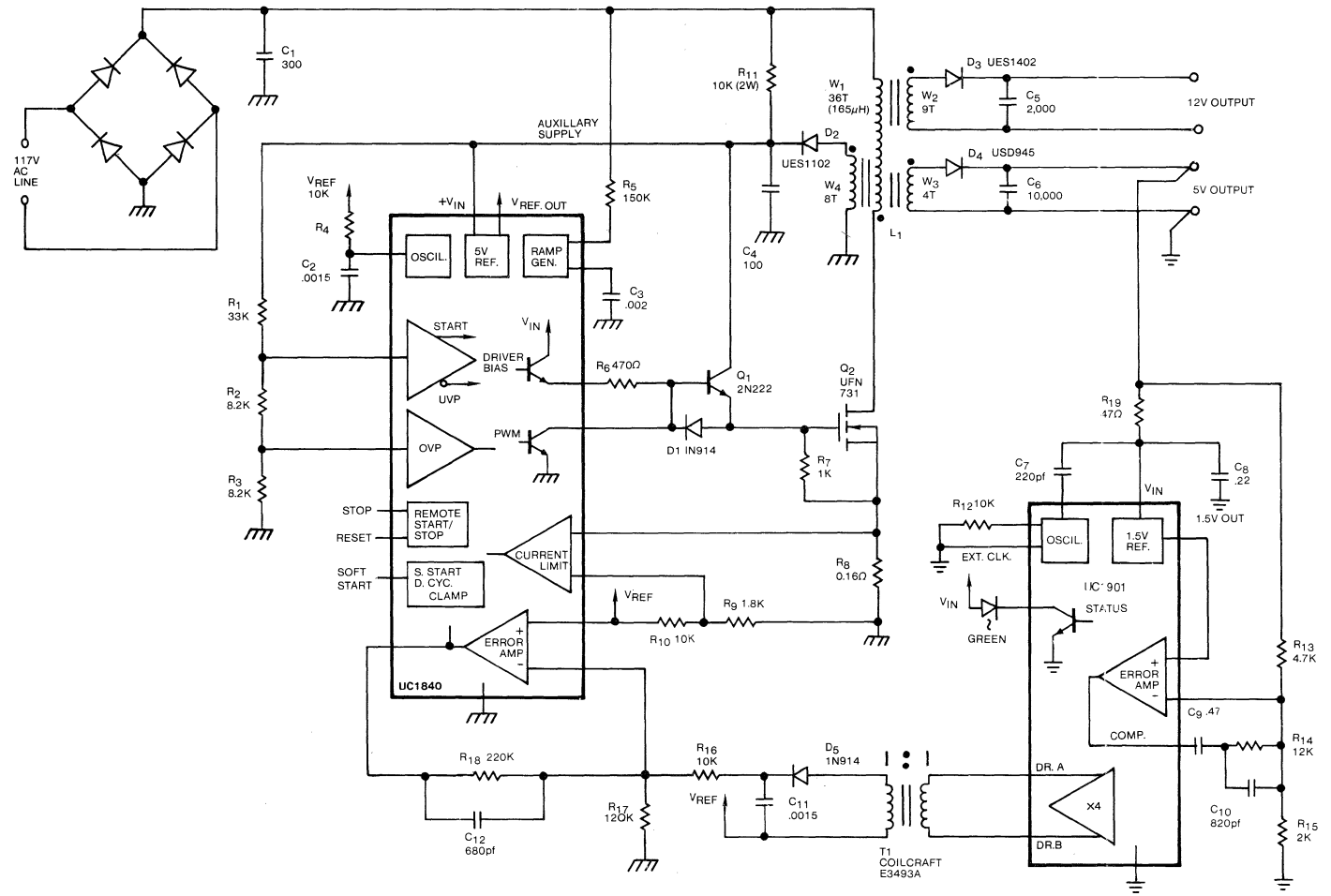


FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\, T_P}{R_5\, C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

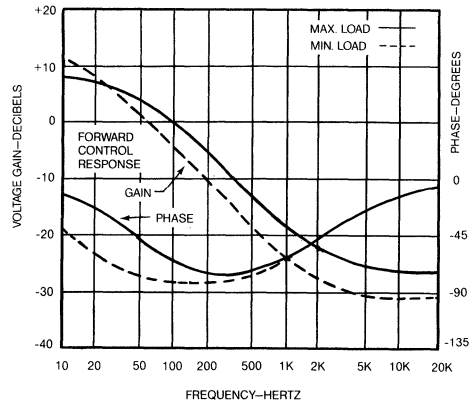


FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

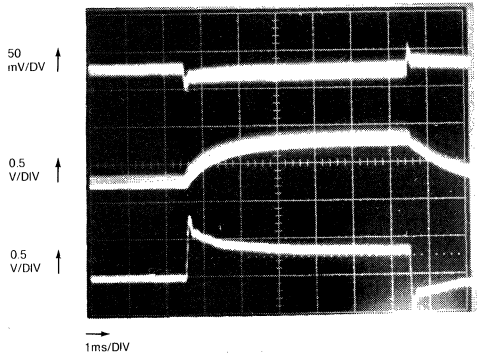


FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF nolding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

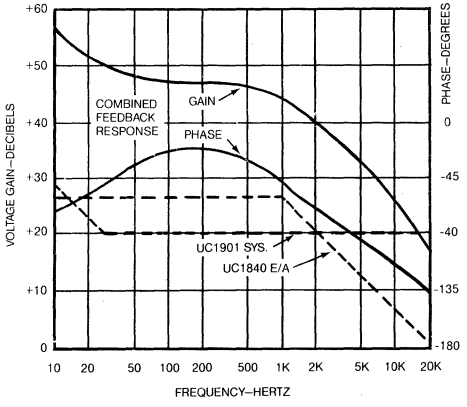


FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

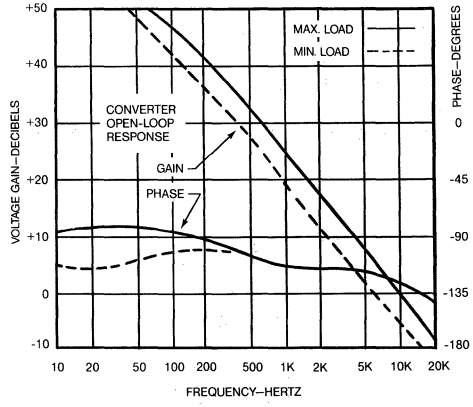


FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of $> 50°$. The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

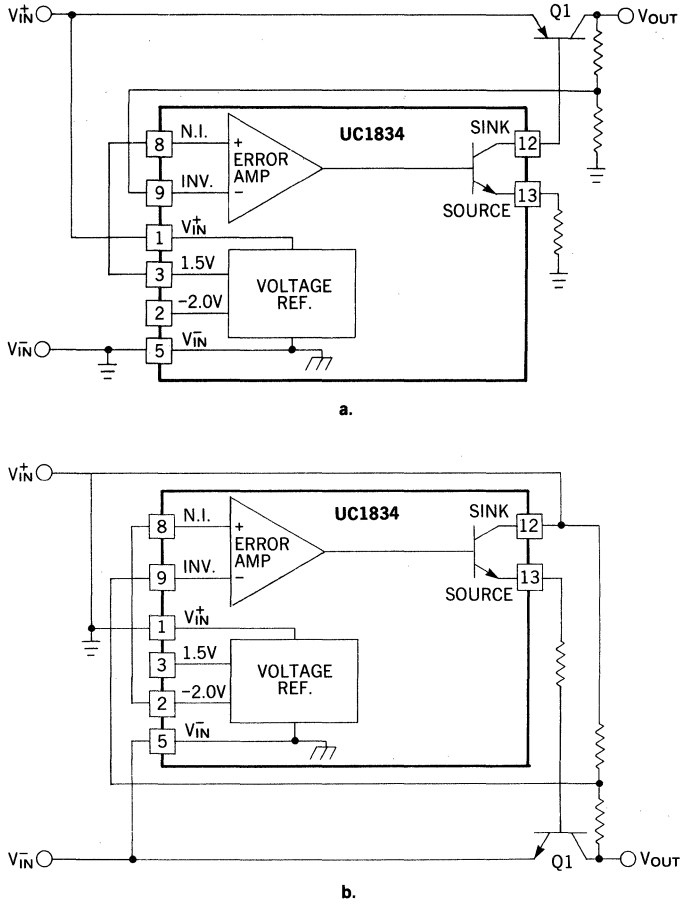


Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

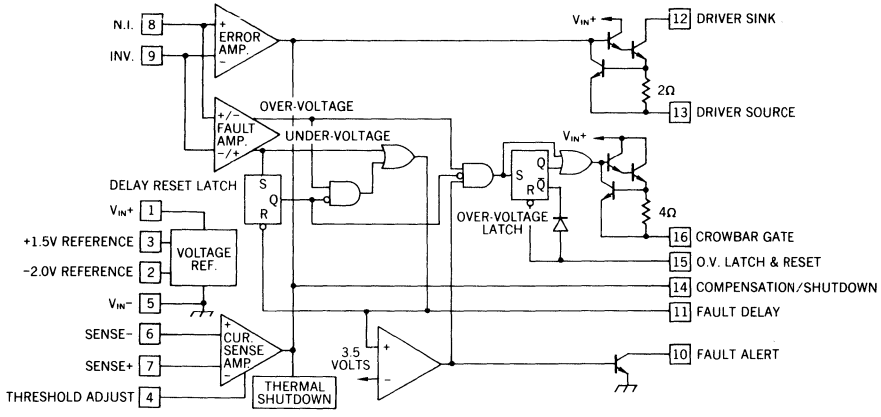


Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~ 30A) is possible with the Darlington pass elements of Figure 3d.

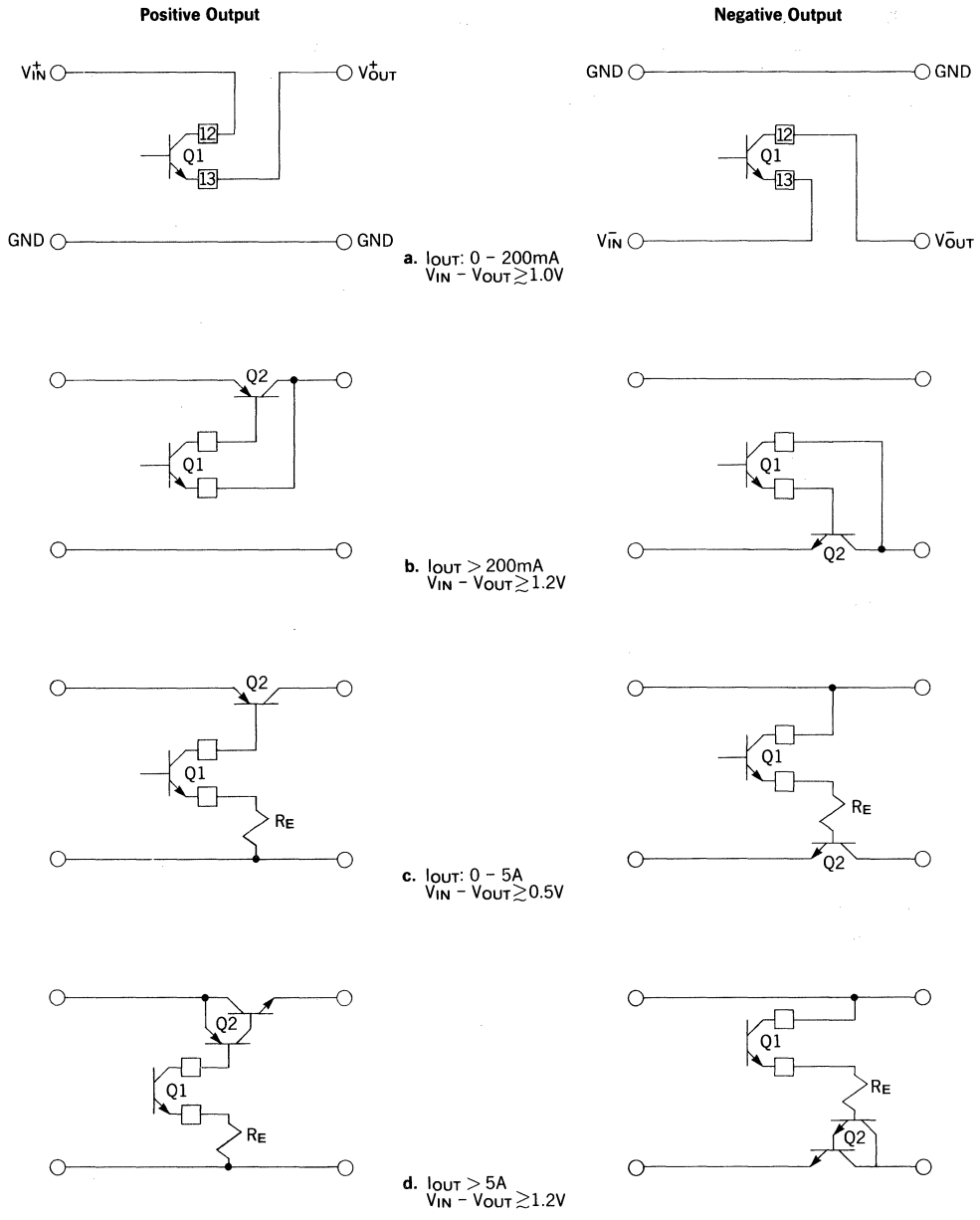


Figure 3. Pass Transistor Configurations

Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

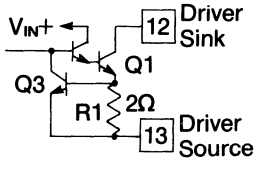
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)}/\beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)}/I_{B(max)(Q2)}$$

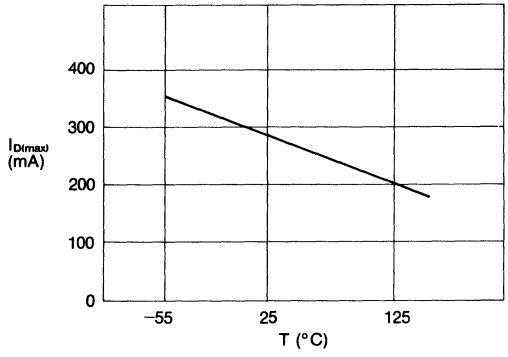
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\ out} - V_{BE(Q1)} - V_{BE(Q2)})/R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

9

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

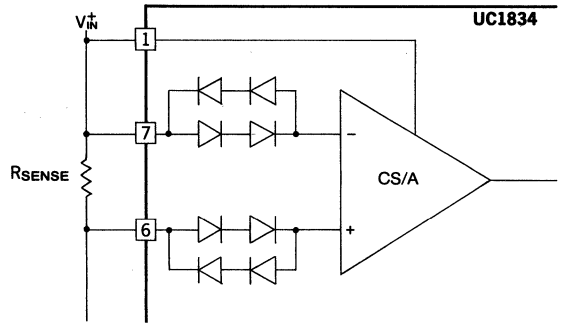


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

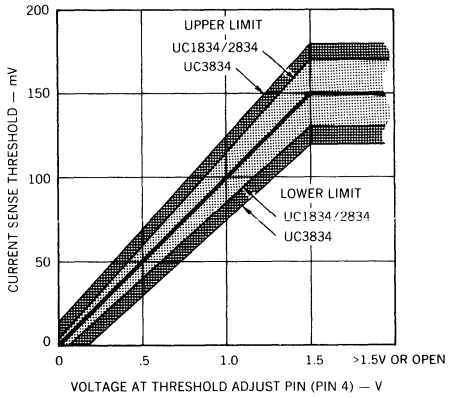


Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

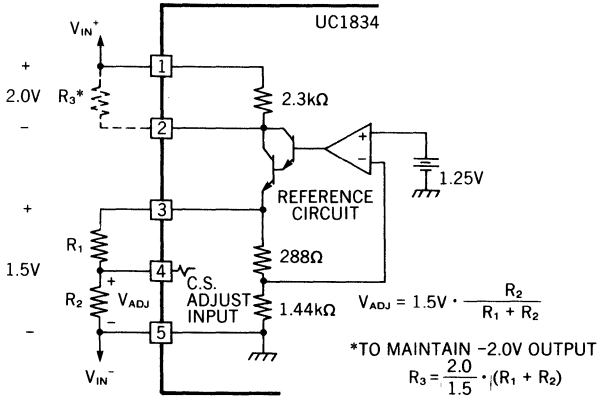


Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage.The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

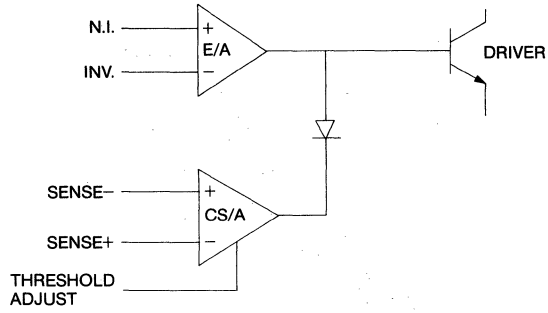


Figure 8. Current Sense Tied to E/A Output

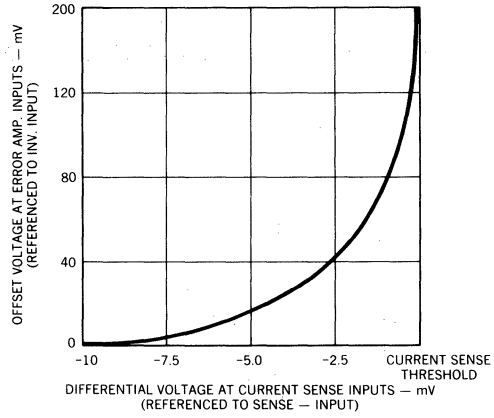


Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$I_{E(max)} \cdot V_{CE} \simeq K$ where K is a constant

or: $I_{E(max)} \simeq K/(V_{IN} - V_{OUT})$ (ignoring the sense resistor voltage drop).

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

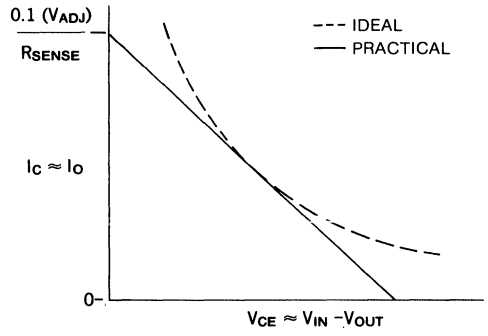


Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

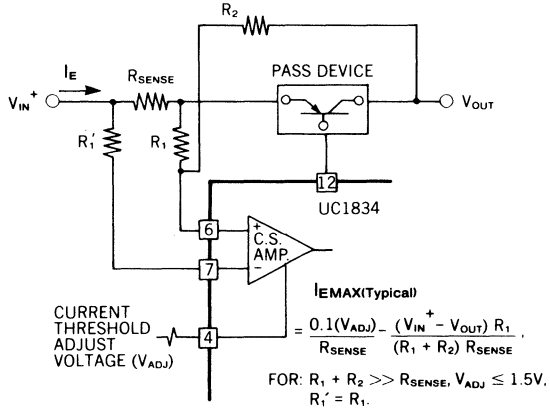


Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

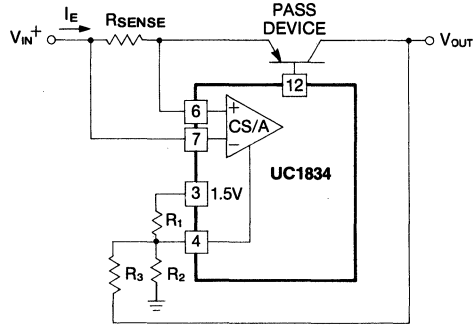


Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

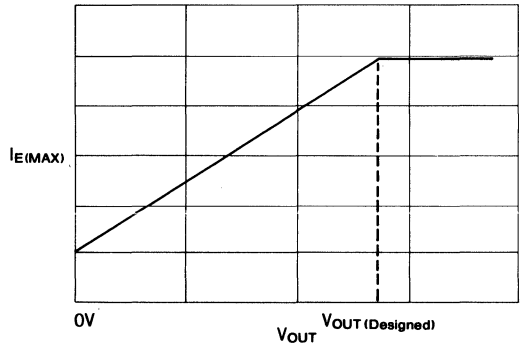


Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

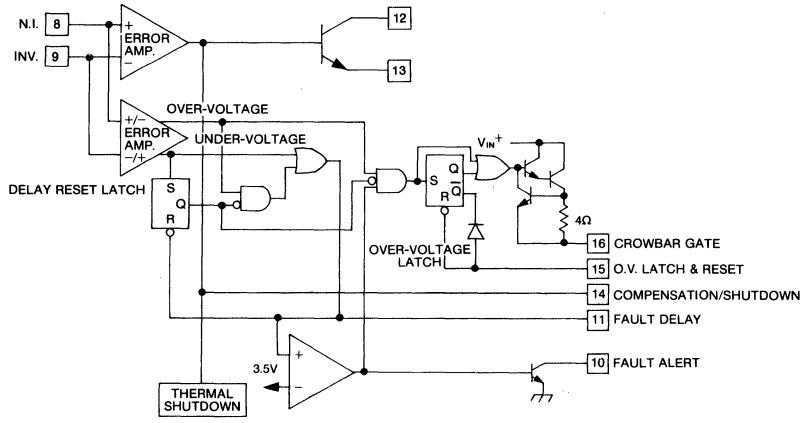


Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_c) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_c.

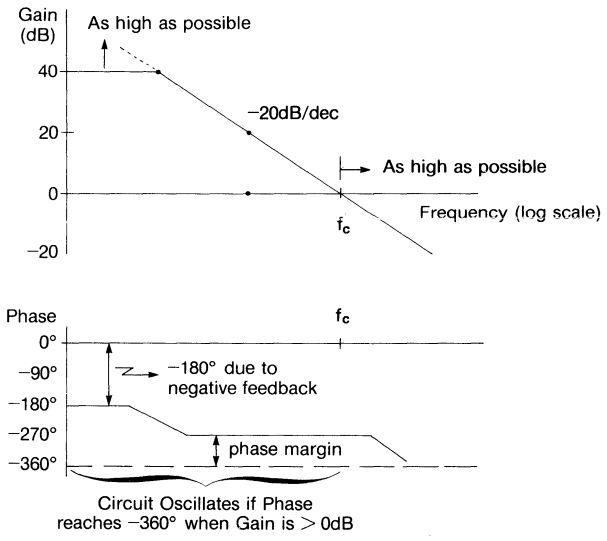


Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

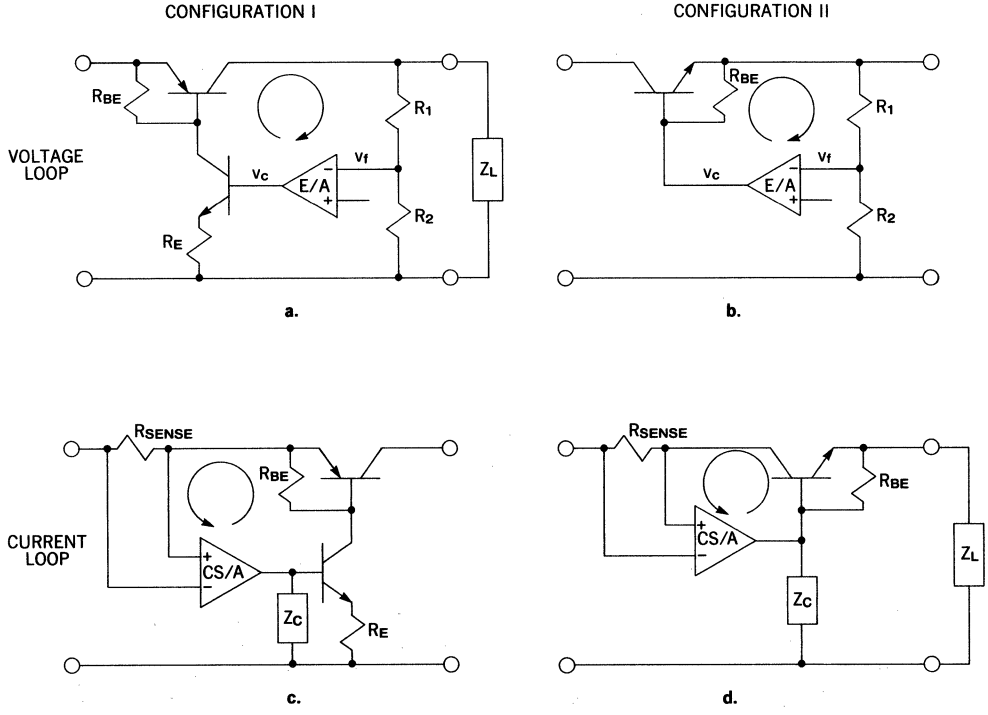


Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50MHz}{200} = 250kHz$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51k\Omega}{(1.7 + 0.51)\ k\Omega} = 20 = 26dB.$$

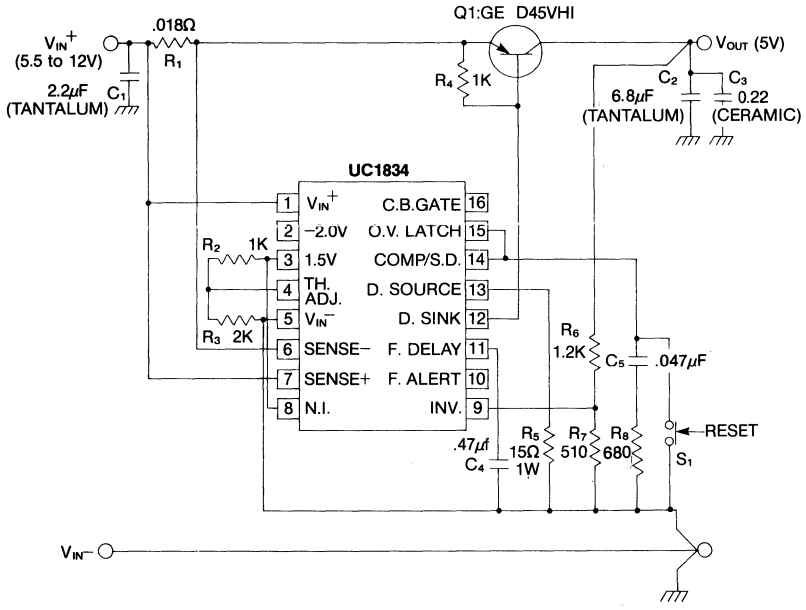


Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

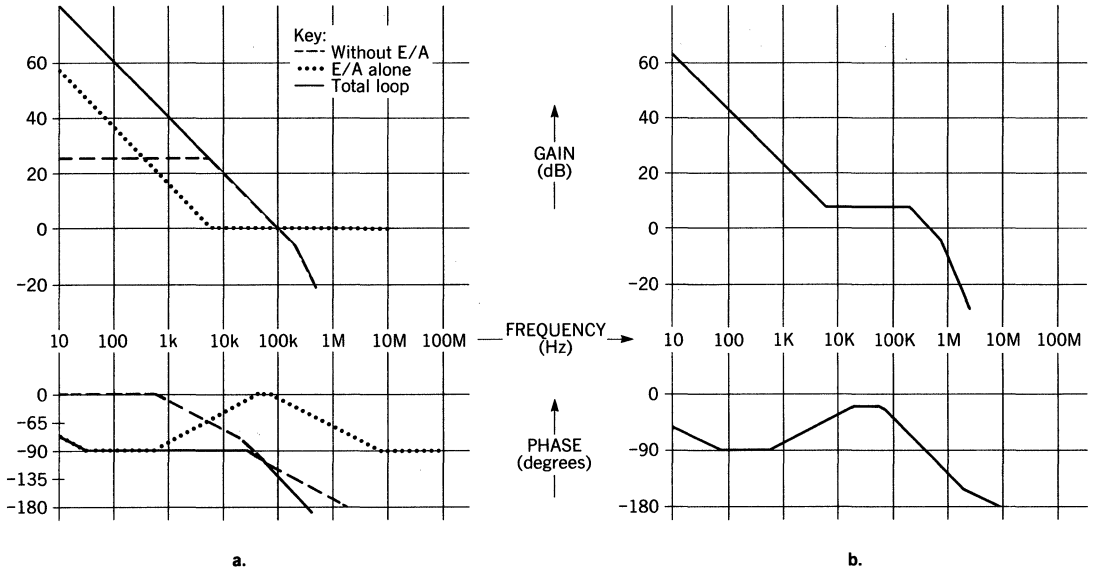


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

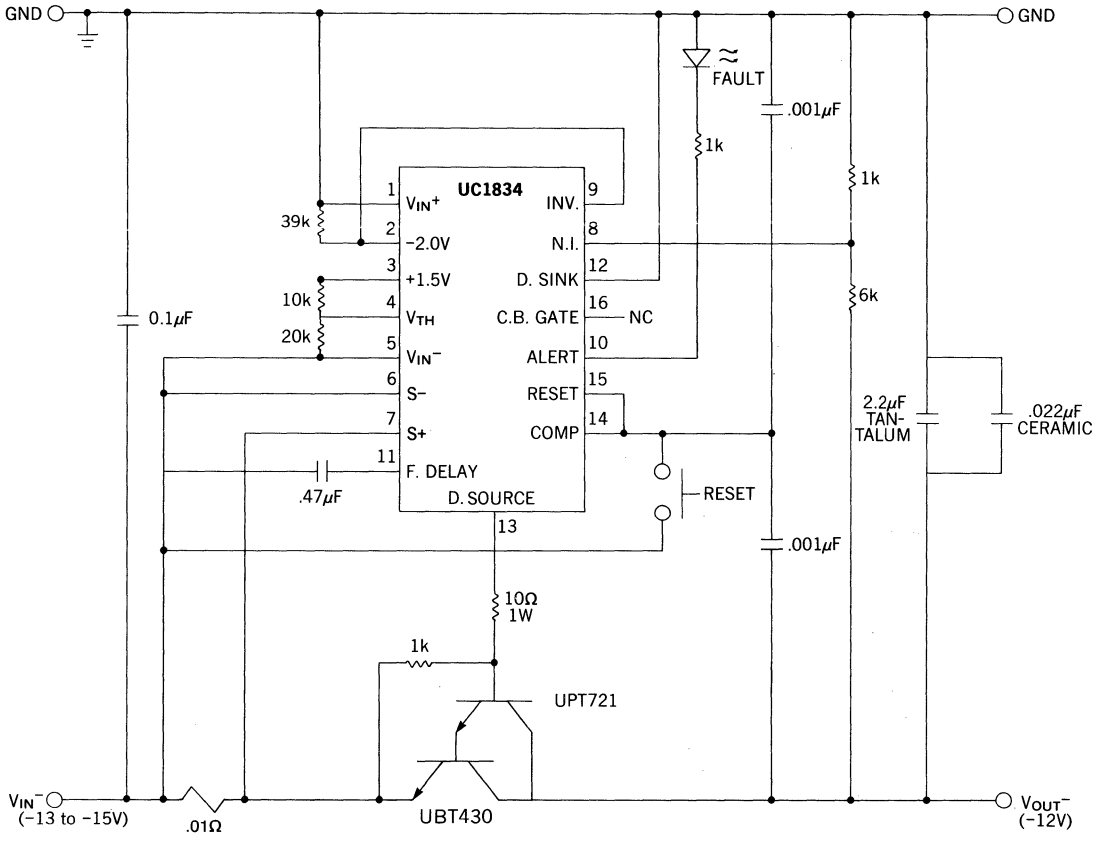


Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{0.026mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

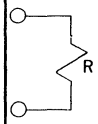
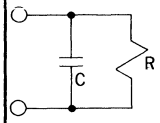
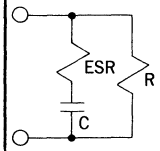
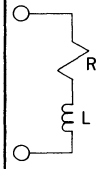
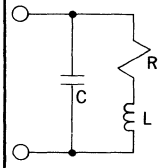
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_c \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

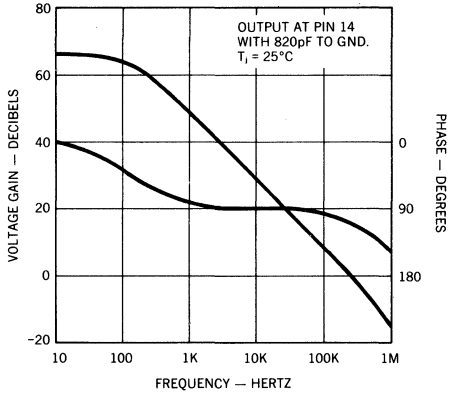


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

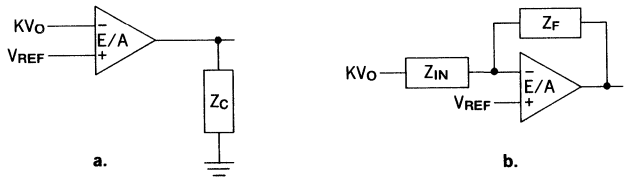


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

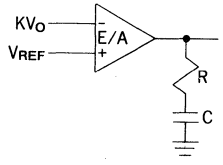
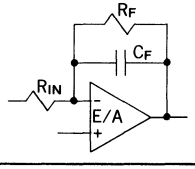
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s R_F C_F)}$	$\frac{1}{2\pi R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

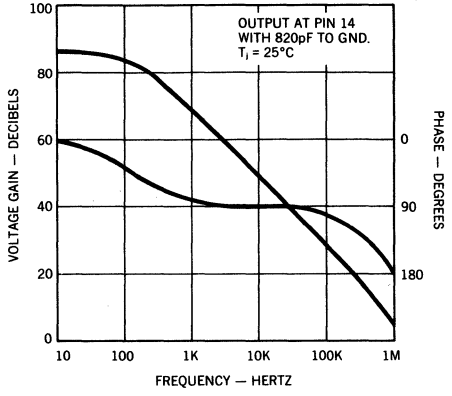


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d).Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

A 25 WATT OFF-LINE FLYBACK SWITCHING REGULATOR

Introduction

This Application Note describes a low cost (less than $10.00) switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc...The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC3844 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOSFET (UFN833) is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. −12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750 Volts
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

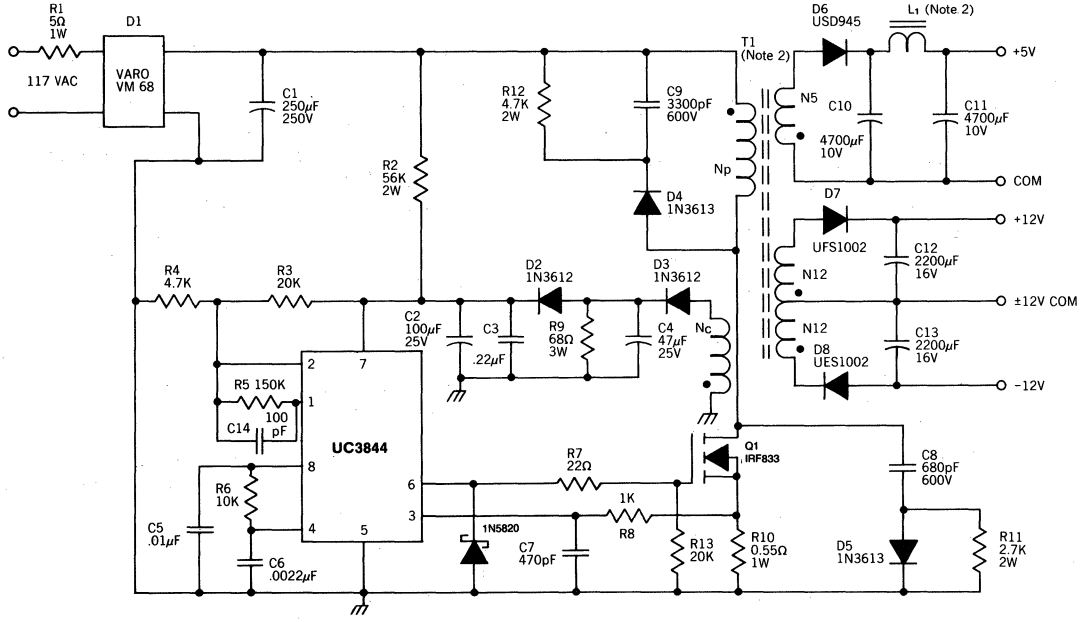
The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOSFET Q1. During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 volt reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

Less than 3.5% line and load regulation is achieved by loading the output of the control winding, Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

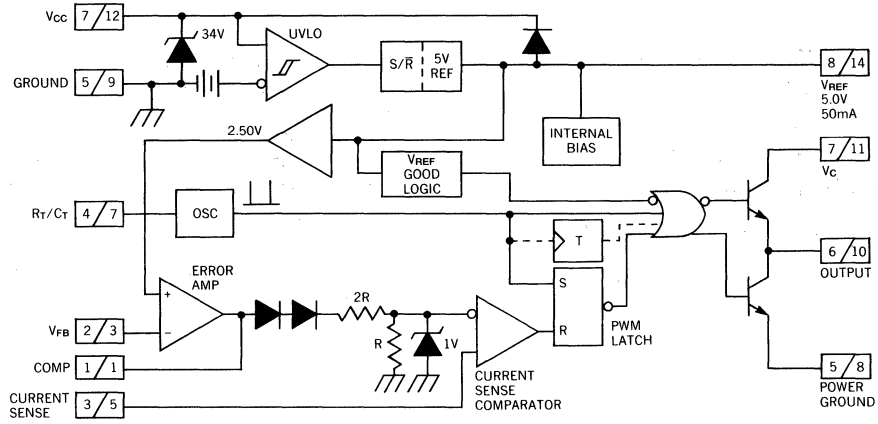
A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

25W OFF-LINE FLYBACK REGULATOR



Notes: 1. All resistors are ¼ watt unless noted
2. See Appendix for construction details

BLOCK DIAGRAM

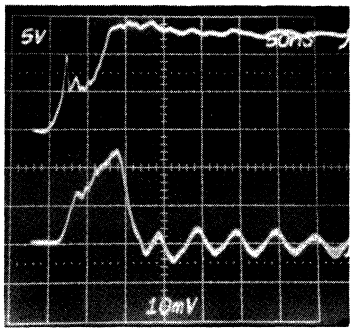


Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.

UC3842/3/4/5 CURRENT MODE PWM CONTROLLER

TYPICAL SWITCHING WAVEFORMS

T_{on} — Drive waveforms

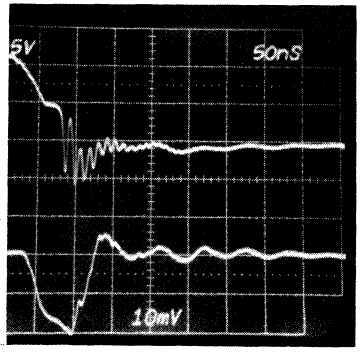


5V/DIV

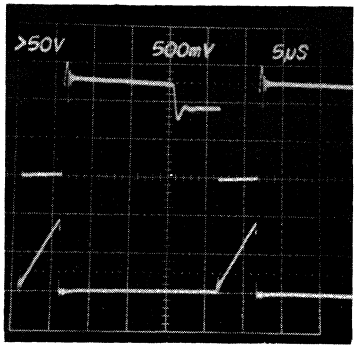
200mA/DIV

Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current

T_{off} — Drive waveforms



Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current



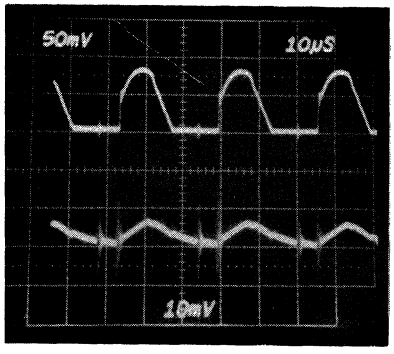
100V/DIV

0.5A/DIV

Upper trace: Q_1 — Drain to source voltage
Lower trace: Primary current — I_D

5A/DIV

50mV/DIV



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

9

PERFORMANCE DATA

CONDITIONS		5V out	12V out	– 12V out
Low Line (95VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.211	12.05	– 12.01
	4.0A	4.854	12.19	– 12.14
± 12 @ 300mA	+5V @ 1.0A	5.199	11.73	– 11.69
	4.0A	4.950	11.68	– 11.63
Nominal Line (120VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.220	12.07	– 12.03
	4.0A	4.875	12.23	– 12.18
± 12 @ 300mA	+5V @ 1.0A	5.208	11.73	– 11.68
	4.0A	4.906	11.67	– 11.62
High Line (130VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.207	12.06	– 12.02
	4.0A	4.855	12.21	– 12.15
± 12V @ 300mA	+5V @ 1.0A	5.200	11.71	– 11.67
	4.0A	4.902	11.66	11.61
Overall Line and Load Regulation		±3.5%	±2.3%	±2.4%

PARTS LIST

IC's		**CAPACITORS**		C10, C11	4700μF, 10V	R7	22Ω
IC1	UC3844	C1	250μF, 250V	C12, C13	2200μF, 16V	R8	1K
POWER MOSFET		C2	100μF, 25V	C14	100pF, 25V	R9	68Ω, 3W
Q1	UFN833	C3	0.22μF, 25V	**RESISTORS**		R10	0.55Ω, 1W
RECTIFIERS		C4	47μF, 25V	R1	5Ω, 1W	R11	2.7K, 2W
D1	VM68 varo	C5	.01μF, 25V	R2	56K, 2W	R12	4.7K, 2W
D2, D3	1N3612	C6	.0047μF, 25V	R3	20K	R13	20K
D4, D5	1N3613	C7	470pF, 25V	R4	4.7K	**MAGNETICS**	
D6	USD945	C8	680pF, 600V	R5	150K	T_1	see appendix
D7, D8	UES1002	C9	3300pF, 600V	R6	10K	L_1	see appendix

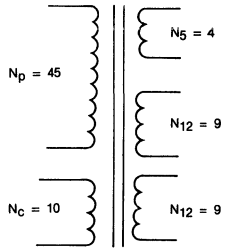
APPENDIX

POWER TRANSFORMER—T1

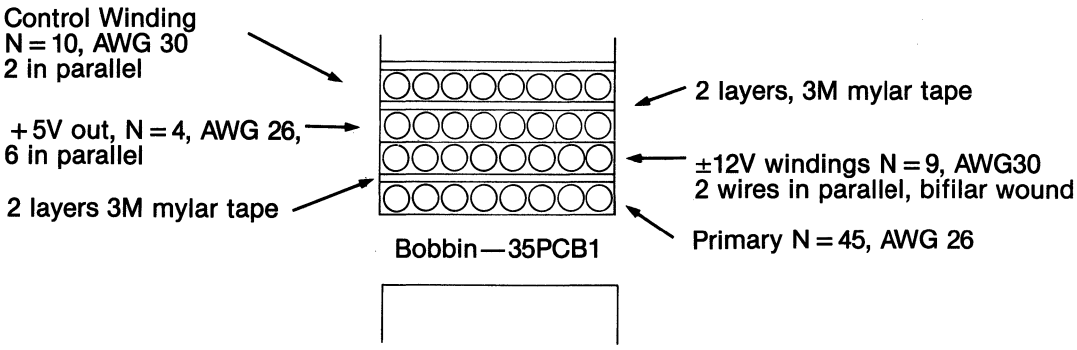
Core: Ferroxcube EC-35/3C8
Gap: 10 mil in each outer leg

NOTE: For reduced EMI put gap in center leg only. Use 20 mil.

Ferroxcube
EC-35/3C8



TRANSFORMER CONSTRUCTION



5V OUTPUT INDUCTOR

Ferroxcube
204 T 250 — 3C8 (toroid)

9

Unitrode Integrated Circuits Corporation
7 Continental Boulevard. • P.O. Box 399 • Merrimack, New Hampshire • 03054-0399
Telephone 603-424-2410 • FAX 603-424-3460

MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated [1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation – usually a single resistor – adds to its attractiveness. However, this introduces a new problem – that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from, yet containing elements of each. Although this has been addressed in part by several authors [1, 2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

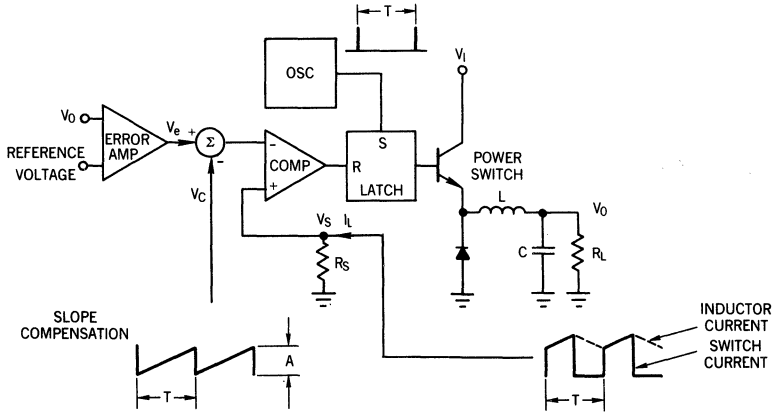


FIGURE 1 – A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in(1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle – regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

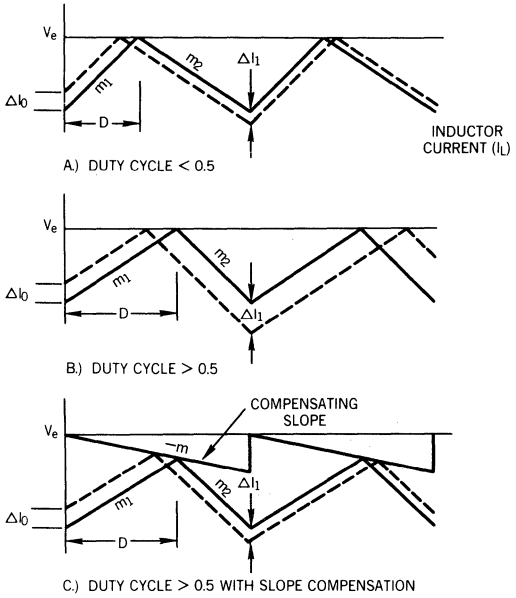


FIGURE 2 – DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for $D < 0.5$ (Figure 2A), and increase with time for $D > 0.5$ (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope $-m$ as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

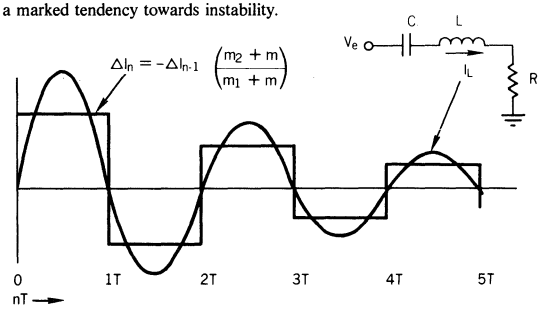


FIGURE 3 – ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

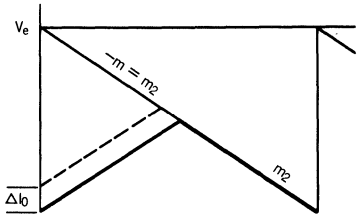


FIGURE 4 – FOR THE CASE OF $m = -m_2$, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

9

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and – because of excess phase shift in the modulator – can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

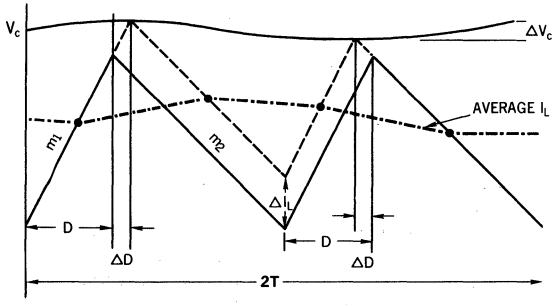


FIGURE 5 – CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation.

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \qquad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \qquad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \qquad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \qquad (7)$$

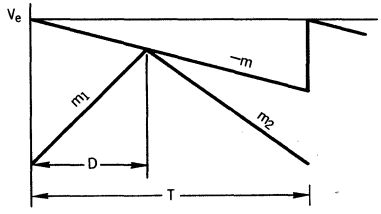


FIGURE 6 – ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \qquad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \qquad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \qquad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = \frac{1}{2}f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \qquad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = \frac{1}{2} f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \qquad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = \frac{1}{2}f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \qquad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation. A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = \frac{1}{2}f_S$, then for the case of $m = 0$ (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -\frac{1}{2}m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

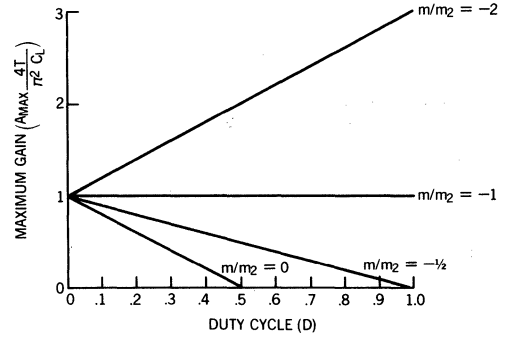


FIGURE 7 – MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage – in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output – or feedforward characteristics. If we choose to add slope compensation equal to $m = -\frac{1}{2} m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -\frac{1}{2} m_2$.

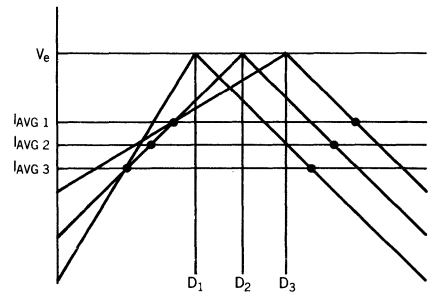


FIGURE 8 – PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

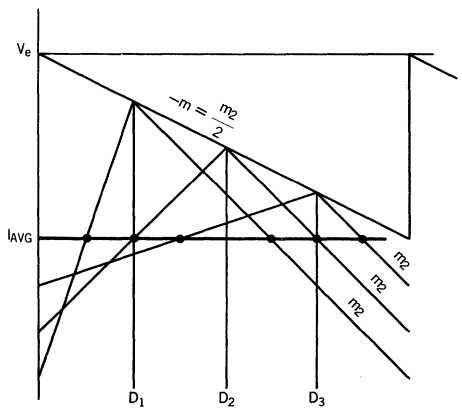


FIGURE 9 – AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUTY CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -\frac{1}{2} m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons – reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current – not just the ripple current. This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -\frac{1}{2} m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

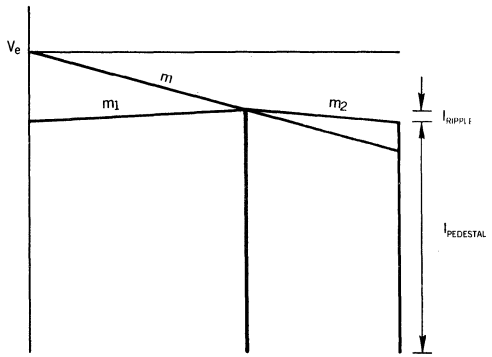


FIGURE 10 – A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

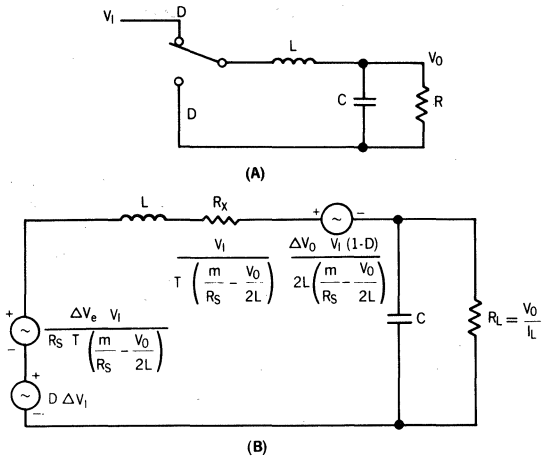


FIGURE 11 – BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations – that in substitute $V_I + \Delta V_I$, $V_0 + \Delta V_0$, $D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables – and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_0}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (17)$$

A third equation – the control equation – relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\, V_0\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1-D)\,\Delta V_0 \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state-space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e\, V_I}{R_S\, LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0\, V_I\,(1-D)}{2L^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation ($m = 0$), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to $L\left(m \gg \frac{R_S V_0}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S V_0}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S V_0}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_0	=	12V
V_I	=	25V
L	=	200μH
C	=	300μf
T	=	20μS
R_S	=	.5Ω
R_L	=	1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced, ripple rejection slowly degrades to that of a voltage-mode converter (−6.4dB for this example).

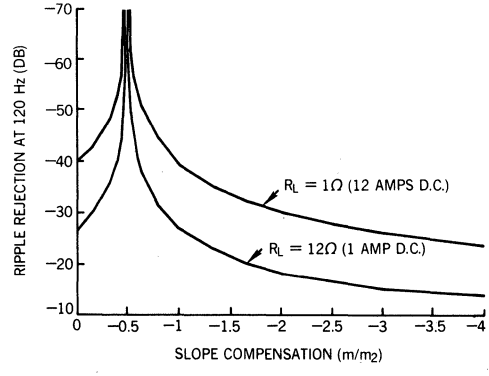


FIGURE 12 – RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used, as is the case for R_L = 1ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}$ m_2, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used, the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift.

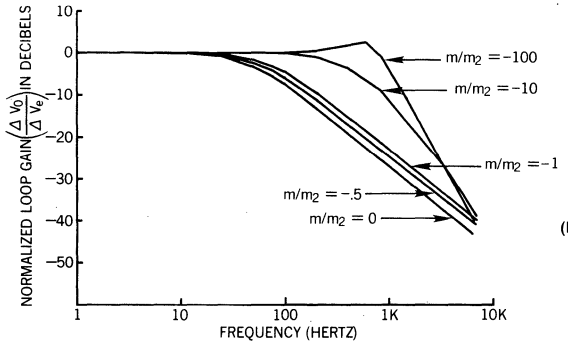
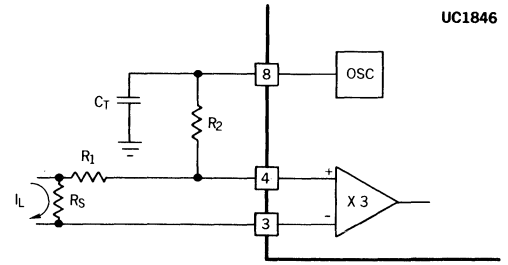
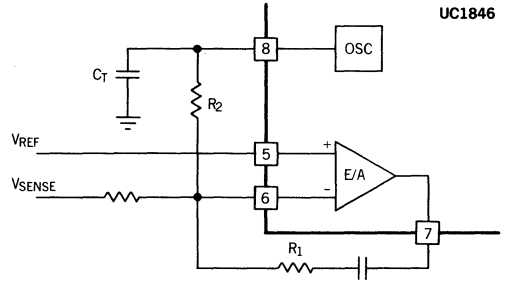


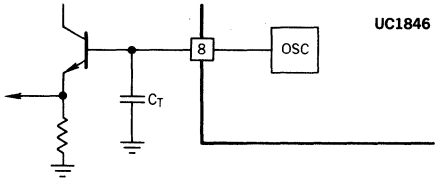
FIGURE 13 – NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 – ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

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UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor

A chopper drive which uses the inductance of the motor as the controlling element causes a temperature rise in the motor due to hysteresis and eddy current losses. For most motors, especially solid rotor constructions, this extra heat can force the designer to go to a larger motor and then derate it, or to a more expensive laminated construction in order to produce enough output torque for the job. Regardless of the motor type, *any* extra heat generated within a system will have to be removed or else other system components will be stressed unnecessarily. This could mean using a fan where convection cooling might otherwise have sufficed. In addition, the EMI generated from both the motor and its leads is of serious concern to the designer in view of ever-increasing EMI regulations.

These problems can be virtually eliminated by borrowing a simple technique from switching power supply designs, i.e., by placing a properly designed low-pass L-C filter across the output and using *this* L to control the UC3717. This removes the high frequency AC chopping losses in the motor by providing it with almost pure DC current. It also confines the EMI-causing, high frequency AC components to within the driver where they are easier to handle. This could allow increased wire lengths and possibly free up some design constraints, but remember that even though DC emits no EMI, the driver will still commutate the windings and can produce some components of frequency as high as 10 kHZ. The design of the L-C filter is straight-forward and its small additional cost can be recovered easily. The Unitrode UC3717, a complete chopper drive for one phase winding on a monolithic IC, makes the design job simple. The end result, a cooler running and EMI quieter step motor, can be achieved with just a few additional passive components.

Preliminary Considerations

For our analysis, we will use a "23" frame, bipolar motor with a solid rotor and the following specifications:

P_{max} =	9.0 Watts	= Maximum power dissipation at 25°C
V_{max} =	3.75 Volts	= Maximum voltage per motor phase at 25°C
I_{max} =	1.25 Amps	= Maximum current per motor phase at 25°C
R_m =	3.0 Ohms	= Resistance of one phase at 25°C
*L_m =	8.4 mH	= Inductance of one phase winding

*It should be noted that L_m, as given in a manufacturer's data sheet, is not always *true average* inductance as seen at high current in a circuit, but rather the inductance reading you would obtain from a low current inductance bridge. This value can differ from in-circuit inductance by a factor of 2 or more! The in-circuit inductance for this motor is 5.0 mH.

We begin by calculating the electrical time constant of one phase winding using the resistance value given above and the *actual* motor inductance:

$$\tau_m = \frac{L_m}{R_m} = \frac{5.0\ \text{mH}}{3.0\ \text{Ohms}} = 1.67\ \text{msec} \quad (1)$$

If one were using a standard voltage drive then it would take approximately τ_m or 1.67 msec to reach the current level required for proper operation. This places a severe restriction on motor speed. Increasing the drive voltage will allow the motor to run faster but will cause it to draw too much current and overheat. Maximum motor speed may be increased by decreasing the time constant. Since L_m is fixed, the only parameter we can change is the effective value of R_m by placing a resistor in series with it. If we place a resistor 4 times R_m in series such that total R is 5 times R_m and increase the drive voltage by a factor of 5 then we will have reduced the time constant by a factor of 5 to 330 μsec and also increased both the maximum motor speed and maximum power output by a factor of 5 each. Unfortunately, we will have increased wasted power by a factor of 5 also.

The Chopper Drive

Using a chopper drive enables one to run at a higher voltage and thus reach proper operating current faster while still protecting the motor from excessive current that would otherwise flow due to the higher voltage. The high voltage is first applied across the motor winding and then, when I_{max} is reached, it is switched off. (If it were not switched off then the maximum current rating of the motor would be quickly exceeded.) The current is then allowed to circulate in a loop within the driver and motor for a fixed time period (t_{off}) after which the voltage is re-applied to the motor. The operating frequency, which is determined by both the motor inductance and t_{off} should be high enough that the resulting current ripple is small compared to the average DC current. Power efficiency is relatively high because there is no external resistor used.

Nothing is free in the world of physics, however, and the price one pays for the extra power output capability is an increase in wasted heat due to hysteresis and eddy current losses *within* the motor instead of in an external resistor. Being within the motor, it can now cause overheating as well as reliability problems. Since the excess heat increases rapidly with the overdrive ratio, this means that at low overdrive ratios (less than 5-to-1) there will be almost negligible heating, but at higher overdrive ratios (more than 10-to-1) the induced motor losses can beome as great as, or actually *exceed*, the I^2R losses! By placing a low-pass L-C filter in the circuit these induced losses can once again become negligible. The L and C components selected should be capable of operating at frequencies of 25 kHz or higher without heating effects in the inductor core or inductive effects in the capacitor.

UC3717 and L-C Filter

Designing with the UC3717

Using a supply voltage (v_s) of 40 volts (approximately a 10/1 overdrive), the turn-on rise-time becomes:

$$t_{rise} = -\tau_m \times Ln(1 - V_m/V_s) = -1.67 \times 10^{-3} \times Ln(1 - 3.75/40)$$
$$= 164\ \mu sec \quad (2)$$

or *an improvement of approximately 10-to-1 in speed capability.*

Using an off-time (t_{off}) of 30 μsec as suggested on the UC3717 data sheet and limiting current (I_w) to 850 mA establishes a voltage across the resistive component of the winding ($V_{w\text{-}on}$) during the "on" time of:

$$V_{w\text{-}on} = I_w \times R_w = .85 \times 3.0 = 2.55\ Volts \quad (3)$$

and during the "off" time (due to a 2.6 volt drop across the upper transistor, as shown in the data sheet, and a 0.4 volt drop across the Schottky "catch" diode) of:

$$V_{w\text{-}off} = V_{transistor} + V_{diode} = 2.6 + 0.4 = 3.0\ Volts \quad (4)$$

Since the voltage and current changes are small, we can substitute a resistance (R_e) equivalent to $V_{w\text{-}off}/I_w$ in series with R_w to adjust the time constant and allow us to calculate the approximate current ripple (ΔI_w) during t_{off}:

$$\Delta I_w = I_w\left(1 - \exp.\left[\frac{-t_{off}(R_w + R_e)}{L_m}\right]\right)$$
$$= .85 \times \left(1 - \exp\left[\frac{-30\times10^{-6} \times (3.0 + 3.5)}{5\times10^{-3}}\right]\right)$$
$$= 33\ mA\ p\text{-}p \quad (5)$$

Knowing ΔI_w, we can now calculate the on-time (t_{on}):

$$t_{on} = \frac{\Delta I_w \times L_m}{V_s - V_{w\text{-}on}} = \frac{33\times10^{-3} \times 5\times10^{-3}}{40 - 2.55} = 4.4\ \mu sec \quad (6)$$

and can also find our operating frequency (f) by:

$$f = 1/(t_{on} + t_{off}) = 1/(4.4 + 30) \times 10^{-6} = 29.1\ kHz \quad (7)$$

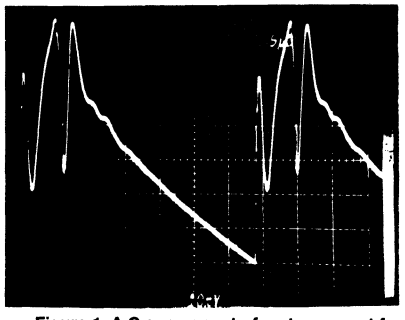

Figure 1. A-C component of motor current for standard chopper configuration.

Since this frequency is well above audible ranges, it will not cause any objectionable sound, but there are still the problems of EMI and excess motor heating to deal with. It is possible to generate EMI due to the current switching that occurs in the motor leads because they carry not only the primary frequency, but also many higher harmonics as well, so they require careful routing, shielding, or both. We can put in a low pass L-C filter to remove these high frequencies and still pass normal commutation currents without any significant loss of motor performance.

Design of the L-C Filter

Figure 2 is a block diagram of a motor connected to 2 UC3717s with the low-pass L-C filters in place.

Again we will use a current of 850 mA in each winding, an off-time of 30 μsec, and an on-time of 4.4 μsec but now we will use an

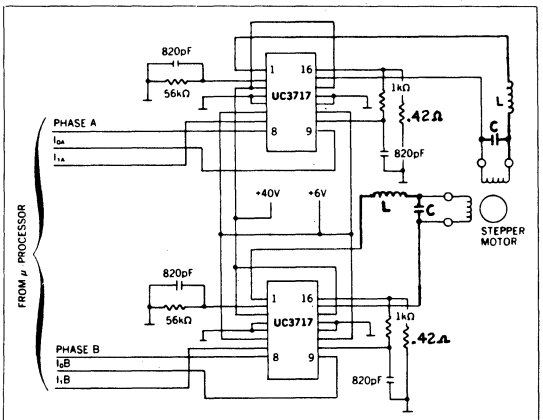

Figure 2. Low-pass L-C filters on outputs.

external inductance (L) to control the chopping. V_{drop} is the sum of the source (V_{so}) and sink (V_{si}) voltage drops at 850 mA:

$$V_{drop} = V_{so} + V_{si} + V_{sense} = (2.6 + 1.9 + 0.36)$$
$$= 4.9\ volts \quad (8)$$

In order to minimize the effects of L on the motor current risetime we will make it 10 times smaller than L_m or 500 μH. In order to keep the peak current in the UC3717 below 1 amp we will use a 0.42 ohm sense resistor and also limit $_{\Delta}I_L$ to 300 mA. Using a variation of equation (6) we can check that:

$$L = \frac{(V_s - V_{drop}) \times t_{on}}{{}_{\Delta}I_L} = \frac{(40 - 4.9) \times 4.4\times10^{-6}}{300\times10^{-3}} = 515\ \mu H \quad (9)$$

is in keeping with the constraints outlined above.

Similarly, we would like to find a value for the capacitor (C) such that it will have less than 1/10 the impedance of L at 29.1 kHz:

$$C = \frac{10}{(2 \times \pi \times f)^2 \times L} = \frac{10}{(2 \times 3.14 \times 29100)^2 \times 500\times10^{-6}} \quad (10)$$
$$= 0.6\ \mu F$$

The test motor and driver, operated unloaded (nothing connected to the output shaft) and in the configuration of *Figure 2*, used values of 500 μH for the inductor and 0.47 μF for the capacitor. *Figure 1* and *Figures 3* through *6* are waveforms obtained from that motor.

The lower trace of *Figure 3* (*Figure 3b*) shows the 330 mA current sawtooth in the inductor, while the upper trace (*Figure 3a*) shows an 8 mA p-p current ripple in the motor winding. While this may seem to indicate only a 12 dB reduction in EMI over *Figure 1*, comparing the *sinusoidal* waveform of *Figure 3a* to the "noisy" *sawtooth* waveform of *Figure 1* will quickly point out sources of

9

UC3717 and L-C Filter

EMI. In *Figure 1*, the oscillations immediately following each switch of the driver are due to the motor's distributed capacitance resonating with its inductance and are a possible source of EMI. In addition, sharp current spikes are allowed to pass along the motor leads and through the motor's distributed capacitance unhindered, thus creating high frequency EMI. EMI spikes were virtually eliminated from *Figure 3a* by using a low ESR capacitor and connecting the motor leads close to the body of the capacitor.

Figure 4 shows motor current superimposed over the inductor current. Just to the left of the center graticle line a ringing occurs in the inductor current that also appears in the motor current, although attenuated. This ringing occurs at a frequency of:

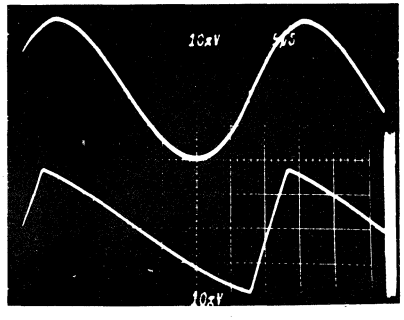

Figure 3. Motor and inductor current waveforms.

$$f_{res.} = 1 / 2\pi\sqrt{L \times C} = 1 / 6.28 \times \sqrt{500\times10^{-6} \times 0.47\times10^{-6}} = 10.4 \text{ kHz} \quad (11)$$

which is the resonant frequency of the L-C filter. This frequency can be lowered by increasing the value of either L or C, although at a cost of reducing the high speed performance of the motor.

The high frequency sawtooth waveforms at the upper, flat portion of the motor current waveform are the 29.1 kHz chopping currents in the inductor. They cause a small corresponding ripple in the motor current but, because the chopping frequency is more than twice the break frequency of the 2-pole L-C filter, we would expect, and can see, an attenuation greater than 12 dB.

In a 2 phase step motor (sometimes referred to as a 4 phase step motor because of the 4 windings used in the unipolar version) the STEP RATE, in full steps per second (FSPS), is 4 times the primary frequency of the motor current waveform. The two phases of the step motor are operated in quadrature and thus will generate 4 distinct states in the 2 phases which correspond to 4 mechanical steps for each electrical cycle.

FSPS = 4 x frequency (for a 2 or "4" phase step motor) (12)

It is important to note at this time that 10.4 kHz is the highest *frequency* that can be passed to this motor without attenuation using the selected components, but that this corresponds to a *step rate* of 41,600 FSPS! The test motor was able to run at 17,000 full steps per second with the L-C filter in place, which is high enough for most situations.

Figures 5 and *6* are current waveforms for the motor running at 1600 FSPS and 16,000 FSPS respectively. The motor was operated with the L-C filter on only the lower trace winding so that the waveforms could be compared easily. Looking at *Figure 5*, one can see that the leading edges of both waveforms have the same risetimes, although the filtered one has more suscepibility toward ringing. From *Figure 6*, one can see that torque is down only 3 dB at 16,000 FSPS and that there are "glitches" in the unfiltered waveform that do not appear in the filtered waveforms.

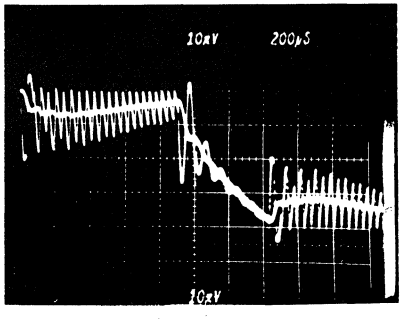

Figure 4. Filter current waveform superimposed over motor current waveform.

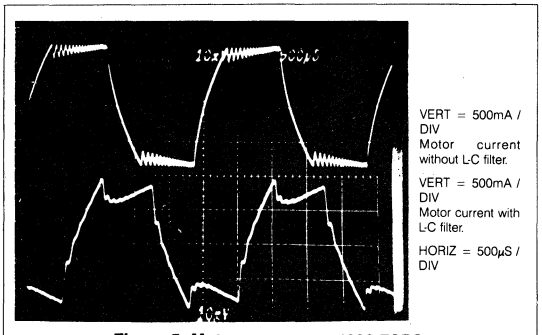

Figure 5. Motor currents at 1600 FSPS.

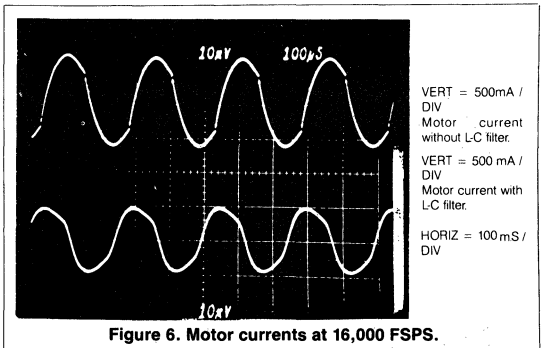

Figure 6. Motor currents at 16,000 FSPS.

Conclusions

The use of a low-pass filter can be an effective heat and EMI reduction mechanism when used with a step motor chopper driver such as the UC3717. The price one pays for a "clean" EMI environment is a *small* loss in very high speed performance. The technique may be applied equally well to non-IC chopper drivers but the peak currents must be accounted for and the minimum value of L adjusted accordingly. 500 μH is the smallest practical L that should be used with the UC3717 since we do not want the

UC3717 and L-C Filter

peak of the ripple to exceed 1.0 amps. This limits the usefulness of the technique to motors with inductances of 2 mH or more. At average currents less than 300 mA, the value of L may have to be larger in order to maintain continuous current in the inductor, but the physical size may be decreased. If an average current in excess of 850 mA is required, then a power amplifier may be added as shown in *Figure 7*. This will extend the peak current capabilities of the chopper drive to higher current and will also allow the value of L to be decreased.

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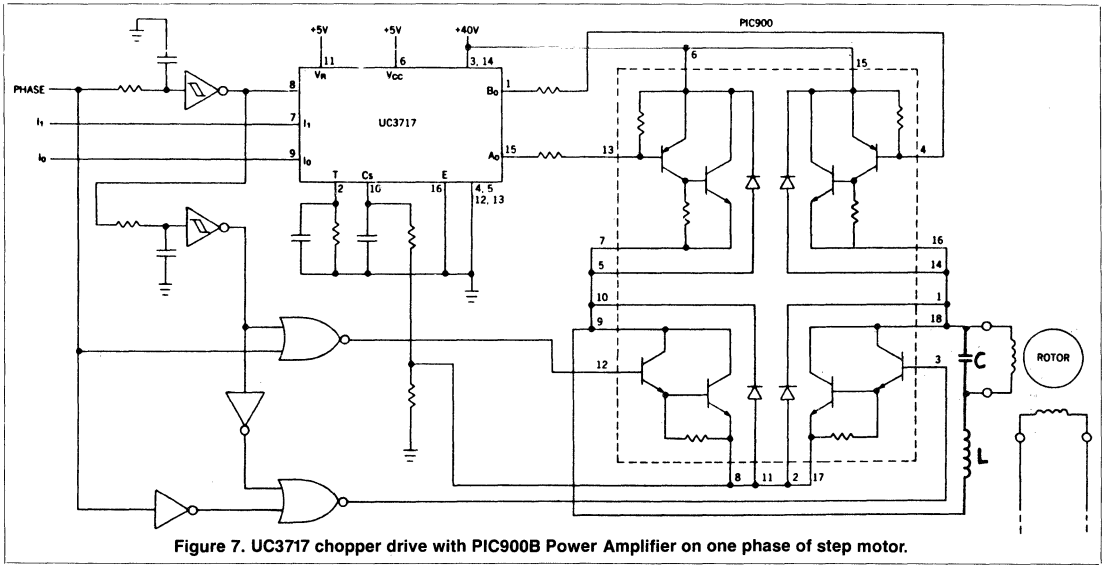

Figure 7. UC3717 chopper drive with PIC900B Power Amplifier on one phase of step motor.

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UC3842/3/4/5 PROVIDES LOW-COST CURRENT-MODE CONTROL

INTRODUCTION

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845. Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

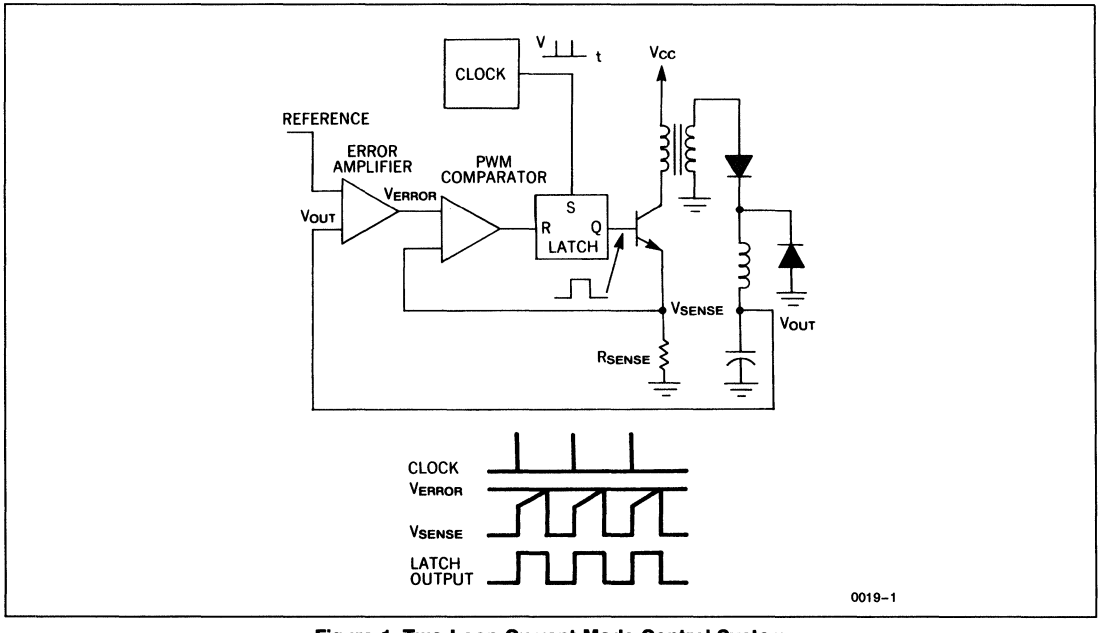


Figure 1. Two-Loop Current-Mode Control System

error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

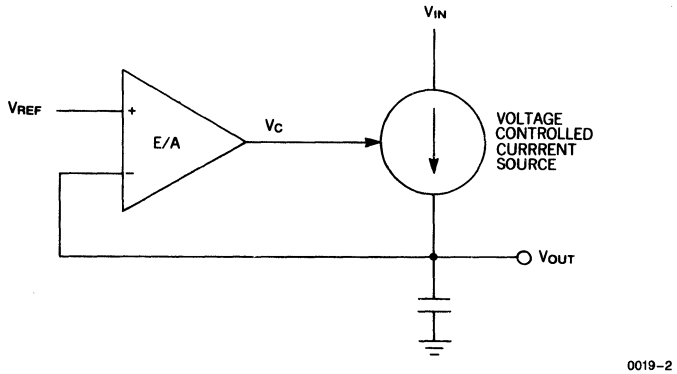
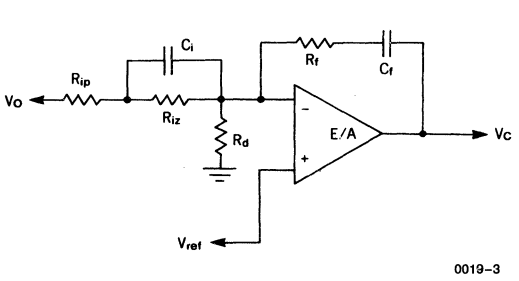
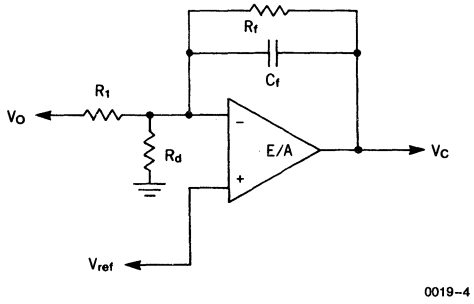


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control



B) Current Mode Control

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

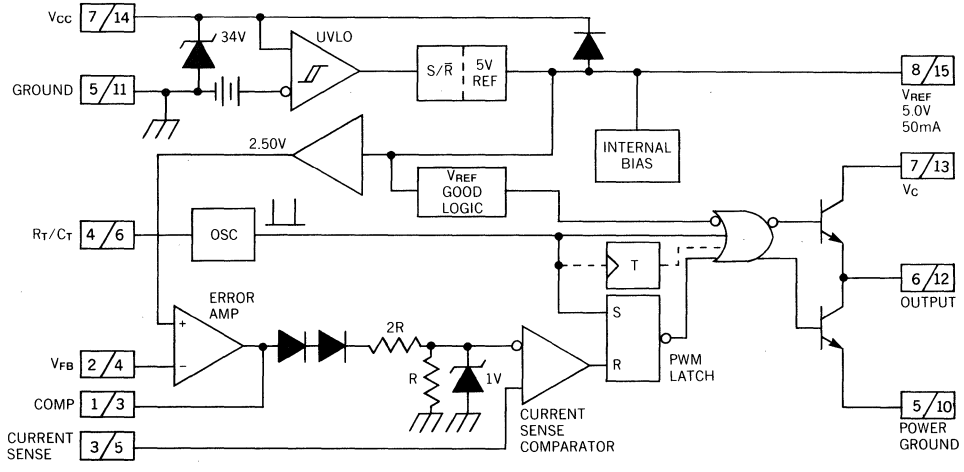
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



Note: 1. A/B A = DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

Figure 4

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.

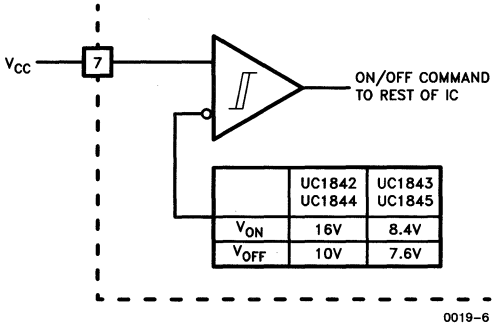


Figure 5

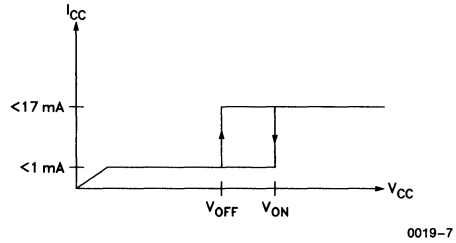


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor C_T is charged from V_{REF} (5V) through the timing resistor R_T, and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of C_T for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72 / (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

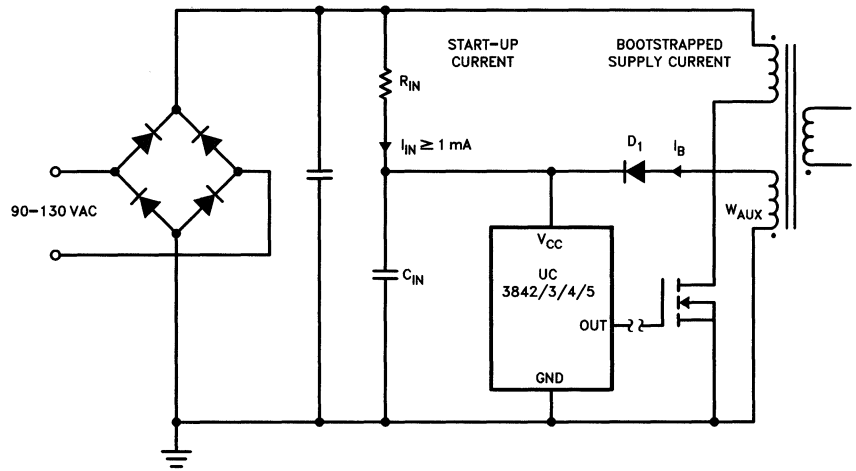


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

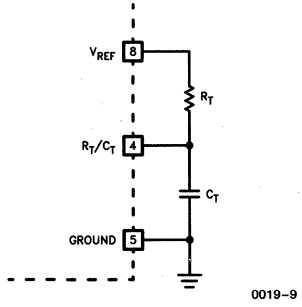


Figure 8

Deadtime vs C_T (R_T > 5k)

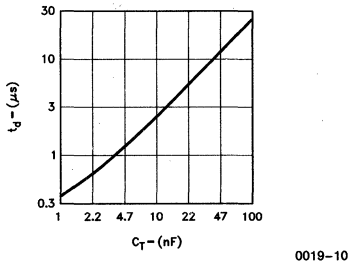


Figure 9

Timing Resistance vs Frequency

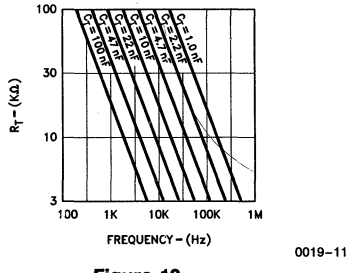


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as **Figure 11** illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_S}$$

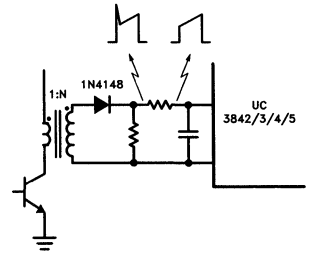


Figure 11. Transformer-Coupled Current Sensing

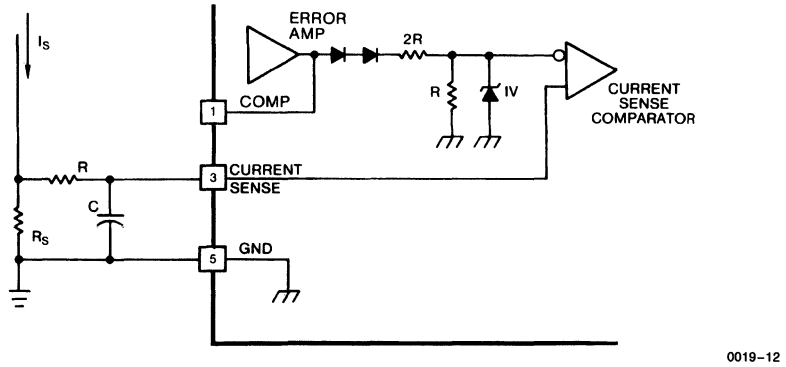


Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = \frac{1}{2\pi} R_F C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

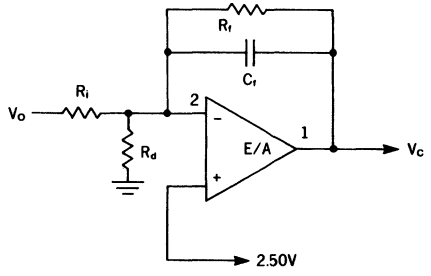


Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

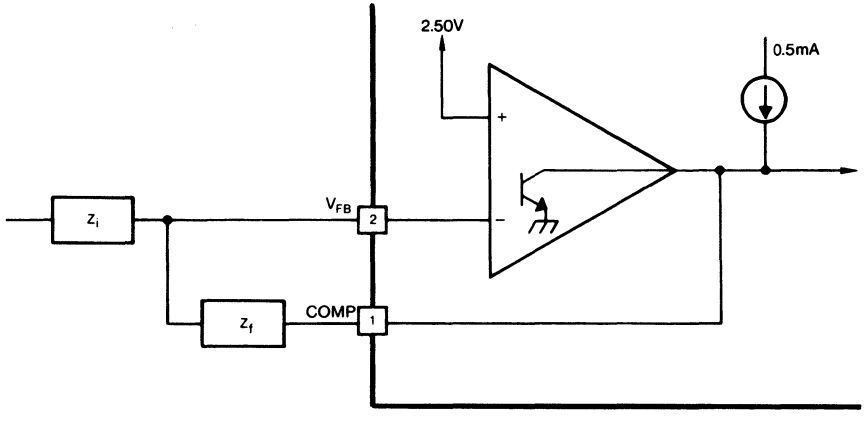


Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I, resulting in a DC error in output voltage (V_O) given by:

$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I$,

It is therefore desirable to keep the value of R_I, as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ±1 amp peak for driving MOSFET gates, and a ±200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most 1- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

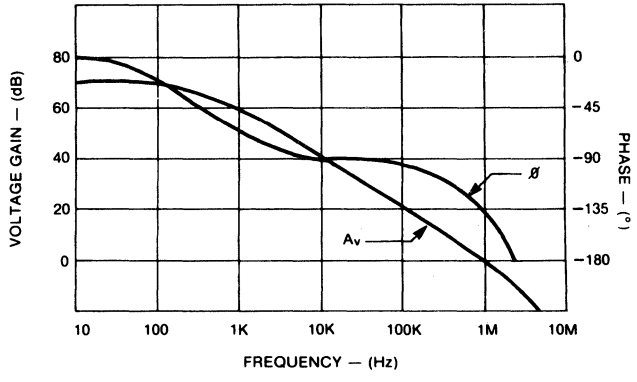


Figure 15. Error Amplifier Open-Loop Frequency Response

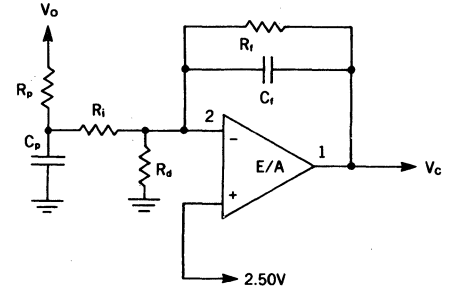


Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ±1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

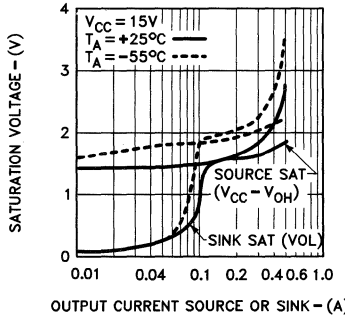


Figure 17. Output Saturation Characteristics

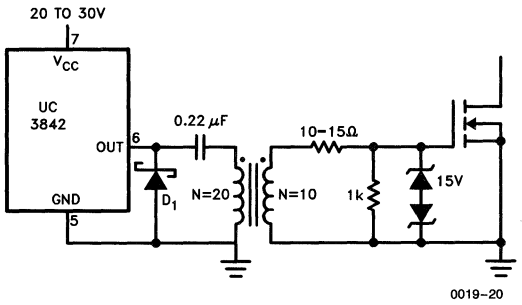


Figure 19. Isloated MOSFET Drive

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

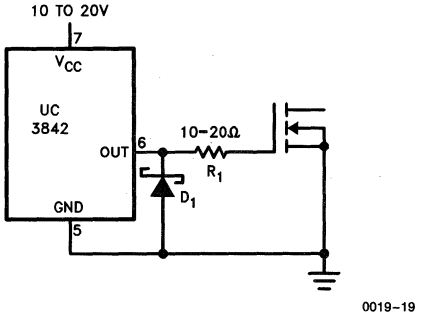


Figure 18. Direct MOSFET Drive

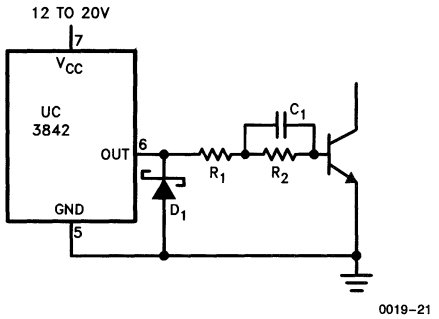


Figure 20. Bipolar Drive with Negative Turn-Off Bias

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 21 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 31 results in an R_T/C_T waveform like that of Figure 21B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

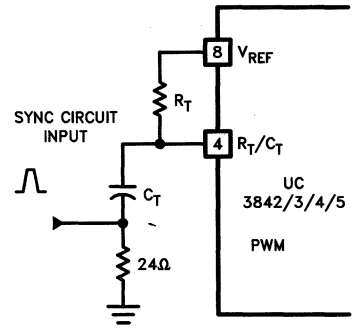


Figure 22. Sync Circuit Implementation

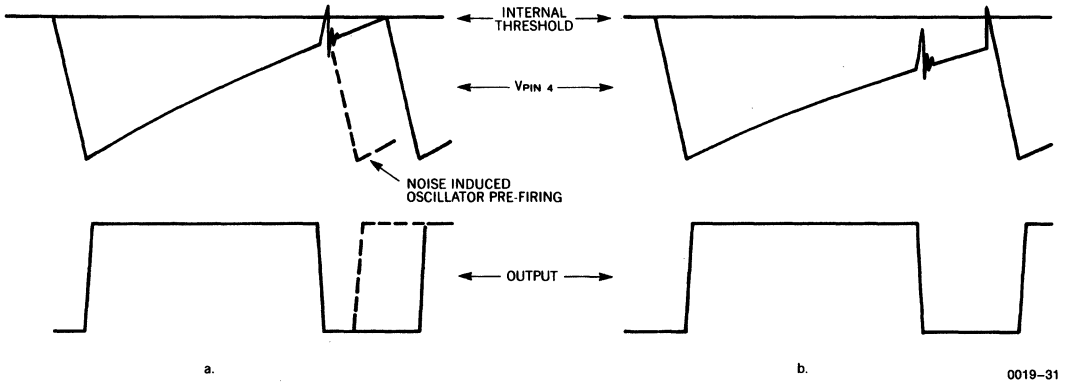


Figure 21. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

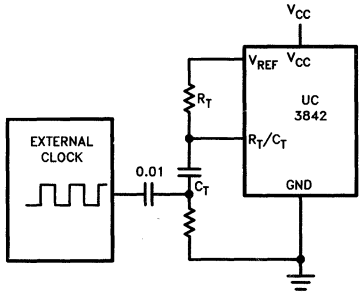
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in "Practical Considerations in Current Mode Power Supplies" listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 23.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a "dead" or off time for the output.

A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



0019-34

$D_{Max} = t_L (t_H + t_L)$
$t_H = 0.693 (R_A + R_B) C$
$t_L = 0.693 R_B C$

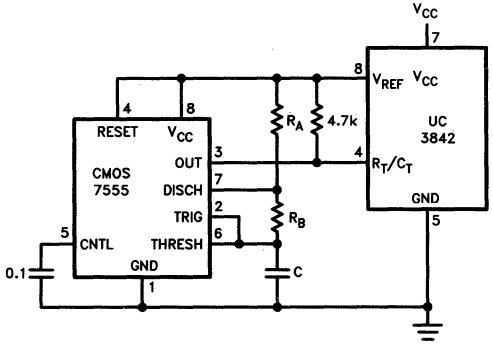


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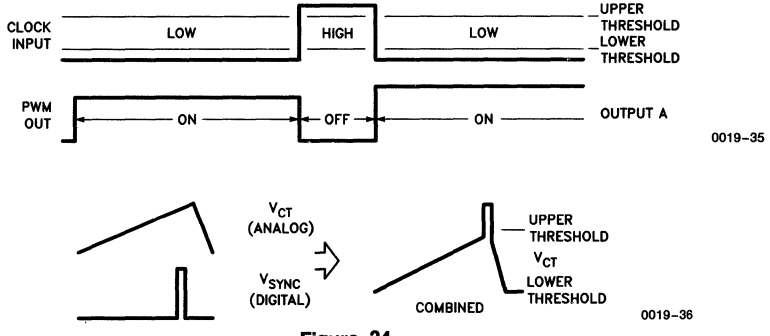
Figure 23

Synchronization to an External Clock



0019-35

0019-36

Figure 24

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 25 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave(s). The photos shown in Figures 26 and 27 depict the circuit waveforms of interest.

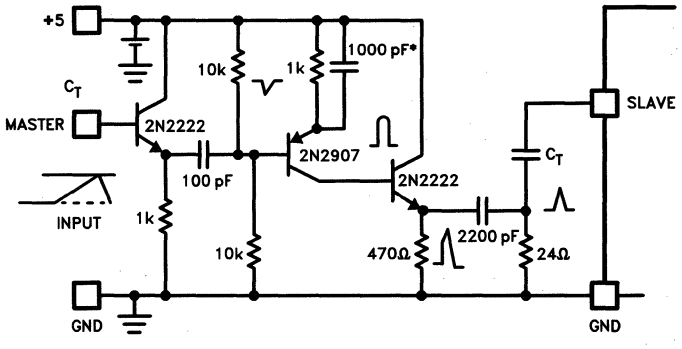
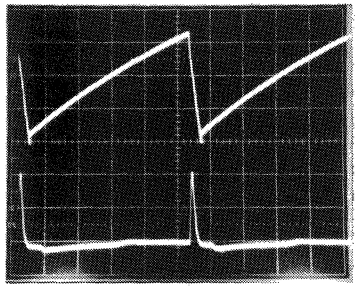


Figure 25. Sync Pulse Generator Circuit

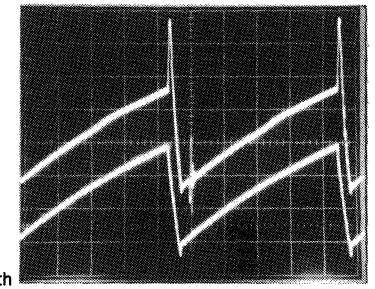


Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

Figure 26. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

Figure 27. Master/Slave Sync Waveforms at C_T

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up
$V_O \approx 2 \times V_{IN}$

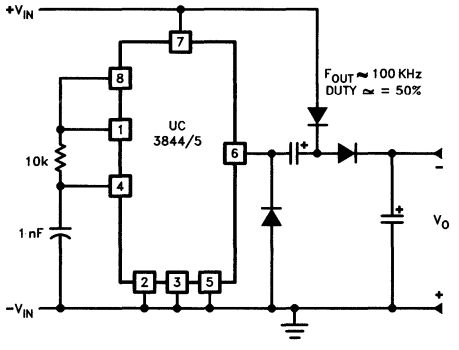


Figure 28

Inverting
$V_O \approx -V_{IN}$

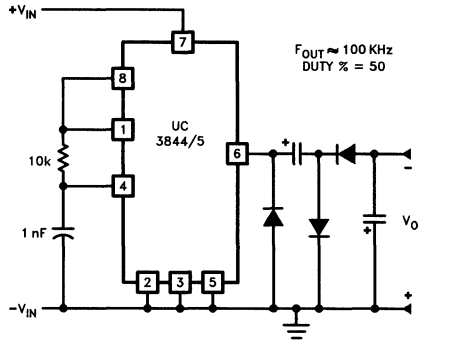


Figure 29

Low Power Buck Regulator—Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see "Closing The Feedback Loop", Buck Topology.

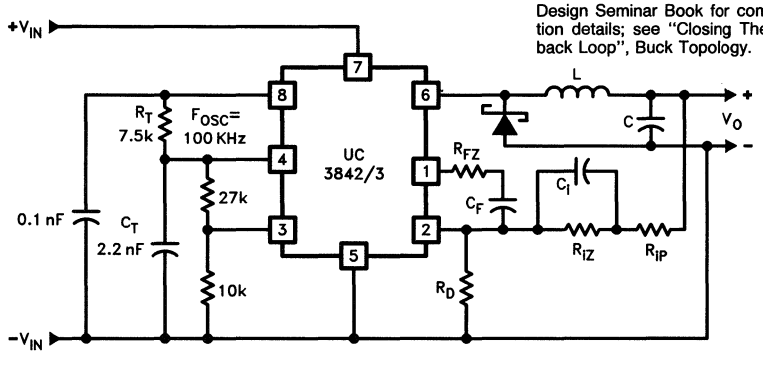


Figure 30

9

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 31 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

Also consult UNITRODE application note U-96 in the applications handbook.

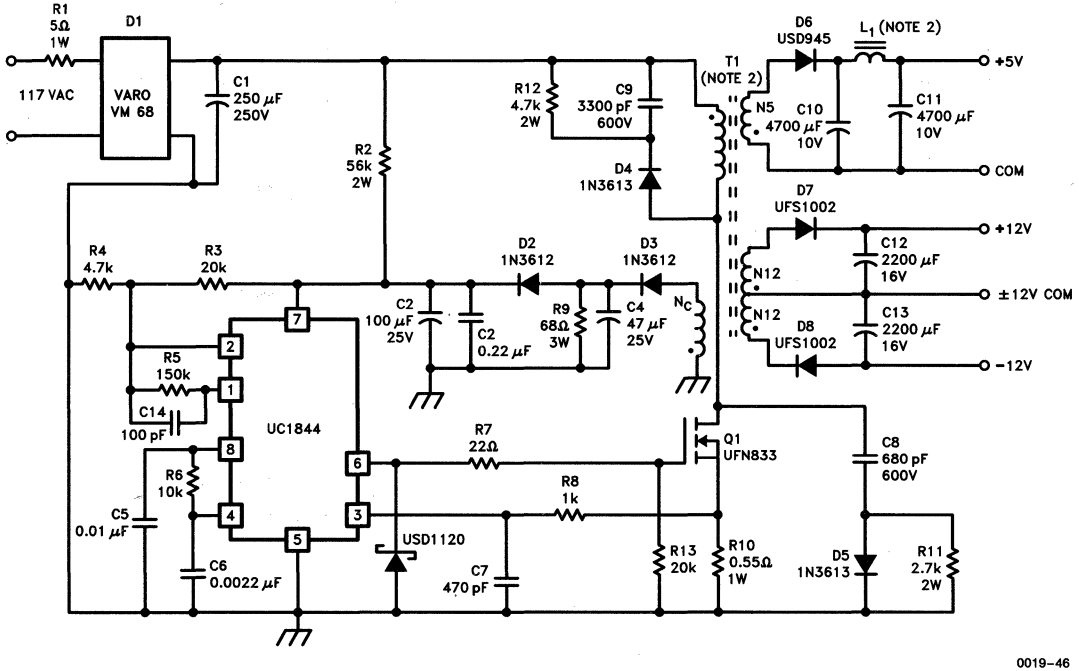


Figure 31

Power Supply Specifications

1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50 mV P-P Max.
   - B. +12V, ±3% 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.
   - C. −12V ±3%, 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.

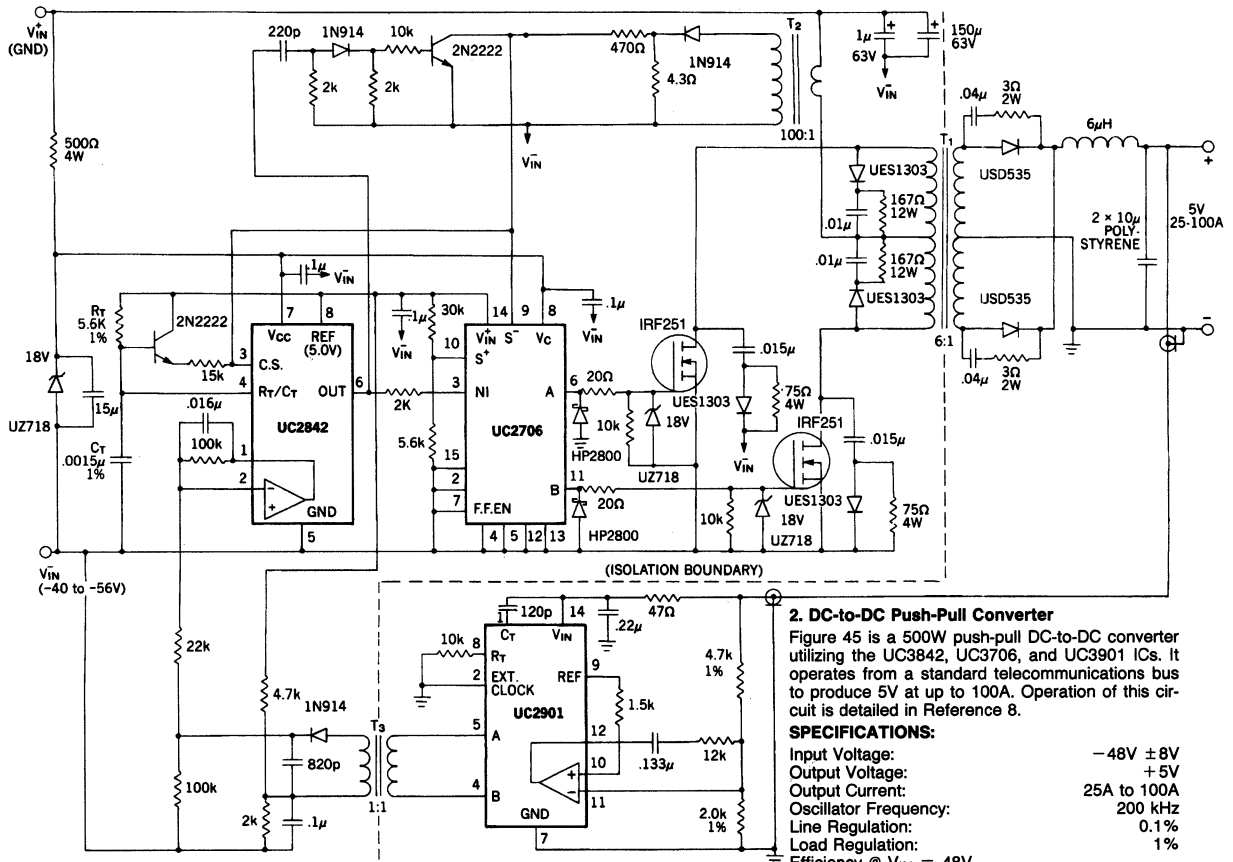


Figure 32. 500W Push-Pull DC-to-DC Converter

2. DC-to-DC Push-Pull Converter

Figure 45 is a 500W push-pull DC-to-DC converter utilizing the UC3842, UC3706, and UC3901 ICs. It operates from a standard telecommunications bus to produce 5V at up to 100A. Operation of this circuit is detailed in Reference 8.

SPECIFICATIONS:

Input Voltage:	−48V ±8V
Output Voltage:	+5V
Output Current:	25A to 100A
Oscillator Frequency:	200 kHz
Line Regulation:	0.1%
Load Regulation:	1%
Efficiency @ V_{IN} = 48V	
I_O = 25A:	75%
I_O = 50A:	80%
Output Ripple Voltage:	200 mV P-P

Also consult application note U-101 in the Unitrode Applications Handbook.

0019-48

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Telephone 603-424-2410 • FAX 603-424-3460

UC1637/2637/3637 SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

INTRODUCTION

There is an increasing demand today for motor control circuits, as a result of the incredible proliferation of automated position control equipment, which is itself made possible by recent developments in the field of digital computation.

The UC1637 Switched Mode Controller for DC motors is one of several integrated circuits offered by Unitrode for motor controls. This Application Note presents the general principles of its operation and the circuit details that optimize its use. As an illustration we will carry out an actual design, which will involve not only the UC1637, but also a power H-bridge using MOSFET transistors, and a modern DC motor tachometer. Using the tach output and UC1637's error amplifier, we will close the velocity control loop after a brief analysis of the factors that affect the feedback loop stability.

To achieve high efficiency power amplification, the UC1637 uses pulse width modulation, or PWM. This technique is employed today in many different circuits where power losses must be minimized, and is most suitable in applications involving inductive loads such as motors, voice coils, etc.

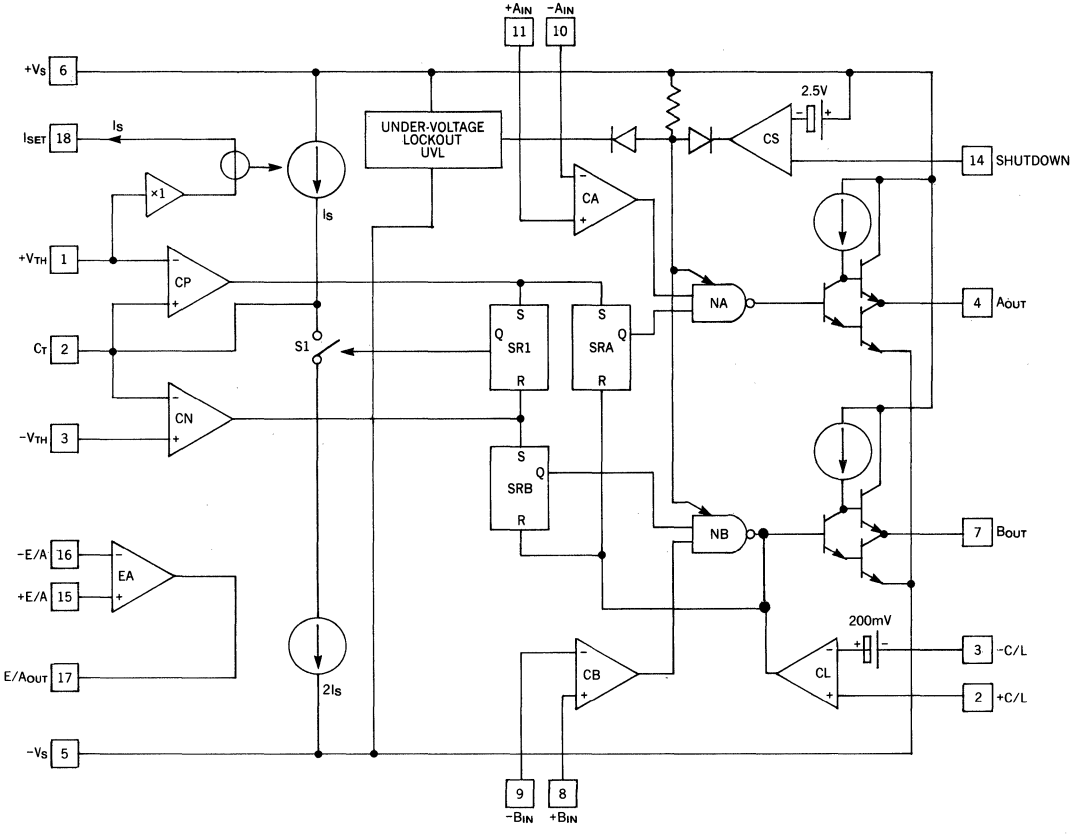


FIGURE 1. BLOCK DIAGRAM OF UC1637.

PULSE WIDTH MODULATION (PWM)

The function of a power amplifier is to regulate the flow of energy from a power supply to a load, under the control of an input signal. A linear amplifier does this by interposing a controlled voltage drop in series with the load, while carrying the full load current. The product of this voltage and current represents the amount of power that must be dissipated by the amplifier itself, and it is easy to see that the method is not very efficient. In fact, its usefulness diminishes rapidly as the amount of power to be controlled increases and, at some point, a more efficient method becomes imperative.

PWM is a switching technique in which the supply voltage is fully applied (switched) to the load and then removed, the "on" and "off" times being precisely controlled. The effect on the load is the same as if some lower voltage were continuously applied whose value depended on the duty-cycle, that is, the ratio of "on" time to the full switching period. Since supply current only flows during the "on" times, it is apparent that the efficiency should be much higher than in the linear amplifier, as in fact it is. Still, switching transistors have small but finite "on" voltages and transition times, all of which introduce losses, which limit practical PWM efficiencies to something between 75% and 90%.

THE UC1637

The diagram of Figure 1 shows in block form the internal organization of the device. The main functions are:

A) Triangular wave generator; CP, CN, S1, SR1
B) PWM comparators; CA, CB
C) Output control gates; NA, NB
D) Current limit; CL, SRA, SRB
E) Error amplifier; EA
F) Shutdown comparator; CS
G) Undervoltage lockout; UVL

The two output lines, A_{OUT} and B_{OUT}, are meant to drive the two legs of an H-bridge power amplifier, with the load driven in bipolar fashion. The A_{OUT} and B_{OUT} outputs themselves are rated at 500mA peak and 100mA continuous, which makes it easy to interface the device with most amplifiers.

In order to generate two PWM output signals, we first produce a triangular waveform, or linear ramp. This is done by charging a capacitor C_T (pin 2) with constant current I_S until the comparator CP, with a fixed threshold voltage of $+V_{TH}$, delivers a pulse to "set" the SR1 latch circuit. This forces Q high, which closes the switch S1 and adds a negative current, $2\times I_S$, to the node of pin 2. As a result, a net current equal to I_S now flows out of C_T, discharging it linearly until the comparator CN resets SR1, and the cycle restarts. Thus, the voltage at pin 2 ramps continuously between $-V_{TH}$ and $+V_{TH}$ at a frequency that depends on these two threshold voltages, on C_T, and on I_S.

The current I_S is programmed by means of a resistor connected to pin 18. The voltage at this pin is equal to $+V_{TH}$ and an internal current mirror forces the charging current I_S to be equal to the current flowing out of pin 18. If a resistor R_S is connected from pin 18 to $-V_S$ (pin 5) instead of to ground, the ramp frequency becomes independent of power supply voltage variations, since I_S will then change together with V_{TH}.

As Figure 2 shows, a triangular waveform can be compared with a reference voltage to generate a PWM signal. The UC1637 uses two separate comparators to generate the two output signals A_{OUT} and B_{OUT}. The way the signals are handled, and the results, are shown in Figure 3 where it can be seen that the difference between V_A and V_B is the cause of the time intervals during which both outputs are low.

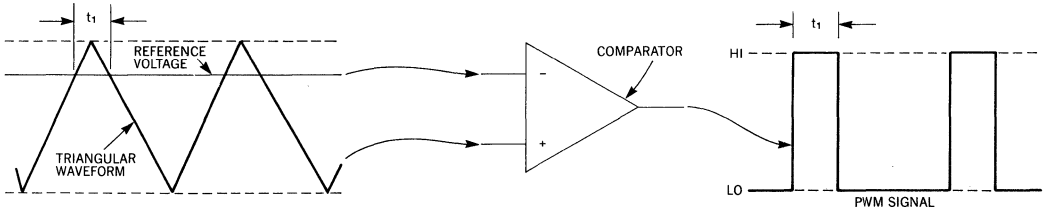


FIGURE 2. HOW A PWM SIGNAL IS GENERATED.

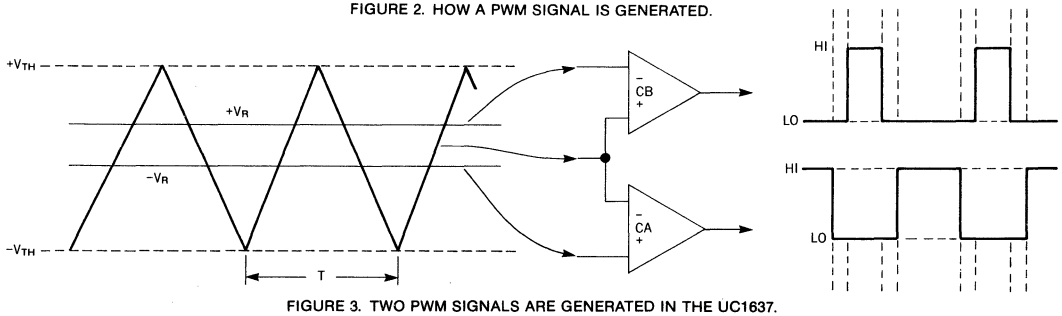


FIGURE 3. TWO PWM SIGNALS ARE GENERATED IN THE UC1637.

The two nand gates, NA and NB, will be enabled if the following two conditions are met:

A) supply voltage $+V_S$ is greater than +4.15 volts (typ)
B) the shut-down input line (pin 14) is at least 2.5 volts (typ) negative with respect to $+V_S$.

If these are satisfied, the A_{OUT} output line will be high if the CA output *and* Q of SRA are both high. Since SRA is set at each positive peak of the oscillator ramp, the output A_{OUT} can be controlled by CA singly — as long as a current-limit pulse from CL does not occur. The operation of the NB gate is similar.

The timing diagrams of Fig. 4 show the sequence of events before and after a current limit pulse occurs. Before time t_1 the PWM action is smoothly controlled by the ramp comparisons with V_A and V_B. The pulse from CL at time t_1 resets both SRA and SRB; the output lines are now disabled until SRA is set (at time t_2) and SRB is set (at time t_3).

The current limit comparator CL provides a means to protect both driver and motor from the consequences of very high currents. If the current delivered by the driver to the motor is made to flow through a low value resistor (for example, see R_S in Figure 7) the voltage drop across this resistor will be a measure of motor current. This voltage is applied between pins 12 and 13 of the UC1637, with pin 12 positive. A 200mV threshold is provided internally (see Figure 1) so that when the R_S voltage is equal to 200mV, the output of CA goes high, resetting both SRA and SRB and, consequently, terminating any active output pulse. This pulse-by-pulse method of current limiting is very fast and provides effective protection, not only for the driver components, but also for the motor, where the possibility of demagnetization due to excessive current is a matter of serious concern.

Finally, the UC1637 contains also an operational amplifier, EA, that can be used to provide gain and phase compensation, as will be seen later.

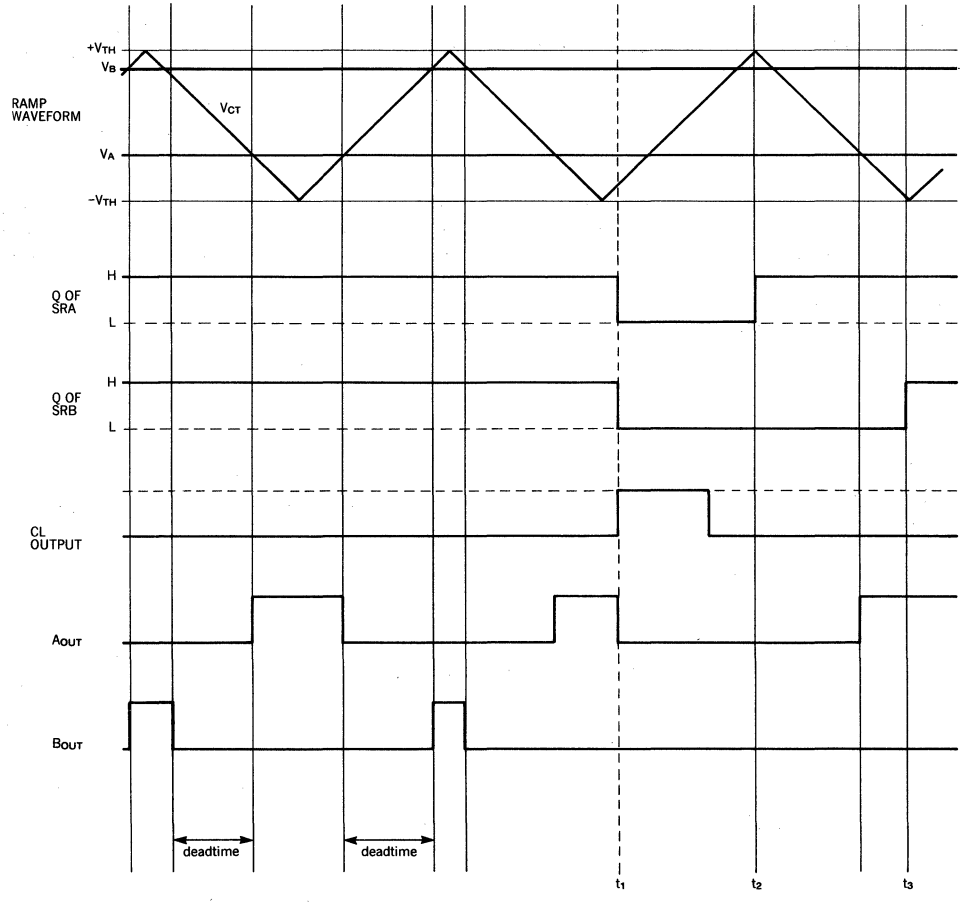


FIGURE 4. TIMING DIAGRAM SHOWING THE GENERATION OF PWM PULSES AT A_{OUT} AND B_{OUT}. BEFORE TIME t_1, THE Q OUTPUTS OF SRA AND SRB ARE BOTH HIGH AND THE OUTPUT PULSES ARE CONTROLLED BY THE RAMP INTERSECTIONS WITH V_A AND V_B. AT TIME t_1, THE CURRENT LIMIT COMPARATOR HAS SENSED EXCESS CURRENT AND THE CL OUTPUT HAS GONE HIGH, RESETTING BOTH SRA AND SRB. THIS TERMINATES THE A_{OUT} PULSE THAT WAS ACTIVE AT THE TIME. A_{OUT} CAN RESUME ONLY AFTER SRA IS SET AT t_2; B_{OUT} CAN RESUME ONLY AFTER SRB IS SET AT t_3.

Figure 5 shows the connections needed to get the ramp generator and the two comparators ready to go. There is no great difficulty in calculating values for the various resistors, which are no more than two simple voltage dividers. Still, certain things should be considered before proceeding.

The input impedance R_{IN}, seen by the control voltage V_C will be

$$R_{IN} = \frac{R_3 + R_4}{2} \quad (1)$$

and this value may be specified or determined in advance. Also, it would be economical to have a minimum number of different values of resistors. If we make

$$R_1 = R_3 \quad (2)$$

we will have four resistors of equal value in the final circuit.

There is also the question of deciding on the separation V_G between the reference voltages $+V_R$ and $-V_R$. The voltage gain of the PWM amplifier will have one of the four characteristics depicted in Figure 6, depending on your choice of reference voltage separation. You can get a linear response by making $V_G = 0$, as in Curve #1, or by making $V_B - V_A = 2V_{TH}$, as in Curve #3. In Curve #2, there is a change in slope due to the contribution, near zero, of both V_A and V_B to the output changes, which in some systems may be undesirable, but which may be of interest due to the fact that it results in zero losses at null.

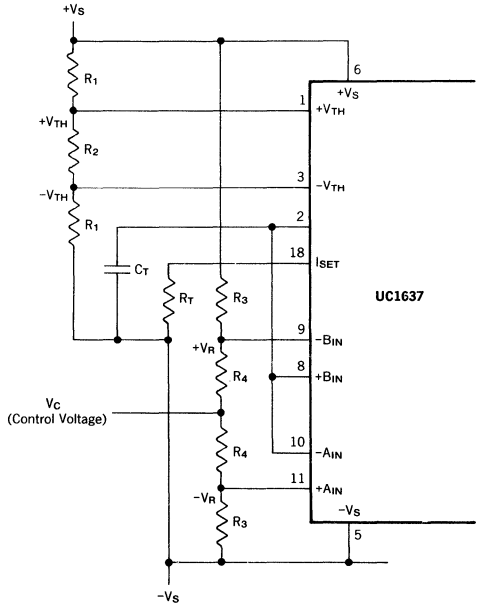


FIGURE 5. SETTING UP THE A AND B COMPARATOR INPUTS.

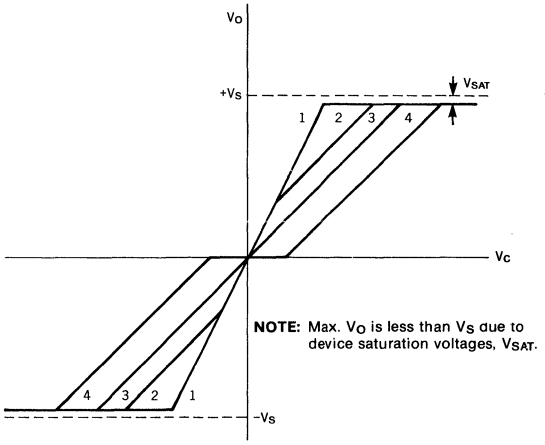


FIGURE 6. PWM VOLTAGE GAIN CHARACTERISTICS OBTAINABLE WITH VARIOUS VALUES OF REFERENCE VOLTAGE SEPARATION, OR GAP VOLTAGE 2 V_R.
1. LINEAR GAIN WITH $V_R = 0$ (a = 0).
2. NON-LINEAR GAIN WITH V_R GREATER THAN ZERO BUT LESS THAN V_{TH} (0 < a < 1).
3. LINEAR GAIN WITH $V_R = V_{TH}$ (a = 1).
4. NON-LINEAR GAIN WITH V_R GREATER THAN V_{TH} (a > 1).
NOTE: THE SLOPE OF LINE 1 IS TWICE THAT OF LINE 3.

At this point, this choice of PWM gain characteristic amounts only to the choice of the ratio between V_R and V_{TH}:

$$a = \frac{V_R}{V_{TH}} \quad (3)$$

The values of V_{TH} and V_R, as well as R_3 and R_4, depend on the following:

$\pm V_S$: power supply voltages
R_{IN}: desired control input resistance
$V_C$max: peak value or input voltage V_C. This is the input voltage at which the output reaches 100% duty cycle
a: ratio of V_R to V_{TH}

These values being known, the designer can proceed to calculate the following circuit values:

$$R_3 = \frac{2\,R_{IN}\,V_S\left(1 + \frac{1}{a}\right)}{V_C\text{max} + V_S\left(1 + \frac{1}{a}\right)} \quad (4)$$

$$R_4 = 2\,R_{IN} - R_3 \quad (5)$$

$$V_A = \frac{V_S R_4}{2 R_{IN}} \quad (6)$$

$$V_{TH} = \frac{V_R}{a} \quad (7)$$

$$R_2 = 2 R_3 \frac{V_{TH}}{V_S - V_{TH}} \quad (8)$$

and, from Eq. (2), $R_1 = R_3$.

Having chosen a frequency f_T for the PWM timing circuit, you can now calculate C_T and R_T. A suitable starting value for the charging current I_S is 0.5mA which gives

$$R_T = \frac{V_S + V_{TH}}{.0005} \quad (9)$$

$$C_T = \frac{.0005}{4 f_T V_{TH}} \quad (10)$$

You will probably need to make an adjustment here, so as to get a standard value for capacitor C_T, and it is best to keep I_S in the range from 0.3mA to 0.5mA when you do this.

It may be desirable, or even necessary in some conditions, to bypass the $+V_{TH}$ and $-V_{TH}$ inputs to ground, and for this, ceramic capacitors of 0.1μf should be adequate. Remember also that terminal 14, the shut-down line, must be held "low" (at least 2.5V below the positive rail) in order to enable the drive. With an external switch to ground, or to $-V_S$, and a pull-up resistor to $+V_S$, this line can be used to enable (low), and disable (high), the output. Both A_{OUT} and B_{OUT} will be low when the shut-down line is high.

The next step is to connect the UC1637 to a suitable power amplifier, and the amplifier to the motor. The UC1637 has provisions for current limiting, as discussed earlier, and you must make arrangements to develop a voltage proportional to motor current at the driver side. This can be done by adding to an H-bridge a low value resistor in series with rail connections. The current limit comparator has a common mode range that reaches all the way down to the negative rail (on the positive side the limit is 3V below the positive rail). A resistor R_S is then added at the bottom of the bridge, and its value is selected so as to give a voltage drop to 200mV when the desired limit current flows.

$$R_S = \frac{.2}{I_{MAX}} \text{ (ohms)} \quad (11)$$

where I_{MAX} is the maximum desired motor current in amperes. In a breadboard, a twisted pair of wires should be used to make the connection from this resistor to pins 12 and 13, and an RC filter should be added, as shown in Figure 7.

On a PC board, it is a good idea to keep R_S close to the UC1637 to minimize the length of the connecting traces. The RC filter should still be used.

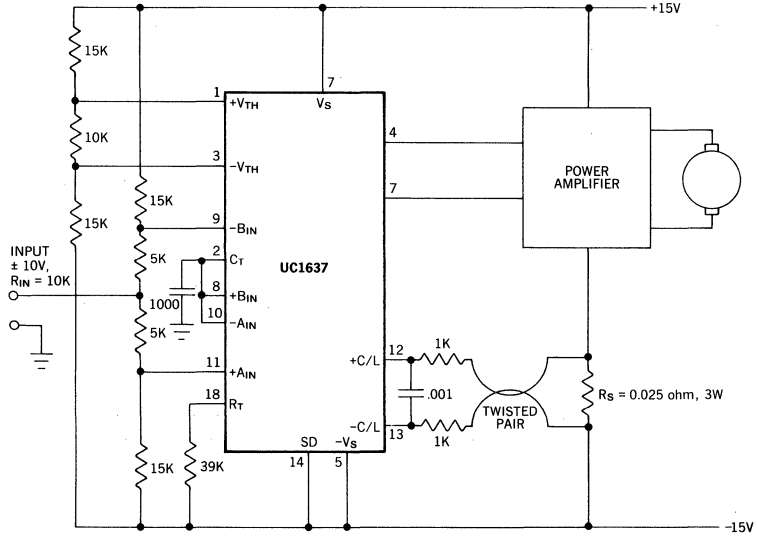


FIGURE 7. CIRCUIT DIAGRAM OF PWM VOLTAGE AMPLIFIER WITH GAIN OF 3.

AN EXAMPLE

We are ready now to design a current limited, PWM voltage amplifier to drive a small DC servomotor. Here are the requirements:

Supply voltages: ±15V
Input: ±10V max.; 10K input res.
PWM frequency: 30KHz
Motor current limited at 8A
Minimum power losses at idle

We have:
$V_S = 15V$
$V_C max = 10V$
$R_{IN} = 10^4$ ohm
$f_T = 3 \times 10^4$ Hz
and $I_{MAX} = 8A$

and also, from the last requirement, a = 1.

FROM EQUATIONS

(4) $$R_3 = \frac{2 \times 10^4 \times 15 \times 2}{10 + 15 \times 2} = 15K$$

(5) $$R_4 = 2 \times 10^4 - 15 \times 10^3 = 5K$$

(6) $$V_R = \frac{15 \times 5 \times 10^3}{2 \times 10^4} = 3.75V$$

(7) $$V_{TH} = 3.75V$$

(8) $$R_2 = (2 \times 15 \times 10^3) \times \frac{3.75}{15 - 3.75} = 10K$$

(9) $$R_T = \frac{15 + 3.75}{.0005} = 37.5K$$

and of course, $R_1 = R_3 = 15K$.

(10) $$C_T = \frac{.0005}{4 \times 30 \times 10^3 \times 3.75} = 1.11 \times 10^{-9} fd$$

If we settle for R_T = 39K, I_S becomes slightly less than 0.5mA and if we then pick C_T = 1000pf, the nominal frequency becomes 32KHz.

To limit the motor current at 8A, we need, from Eq. 11,

$$R_S = \frac{.2}{8} = 0.025 \text{ ohm}$$

The peak power in the resistor will be

$P_S = 8^2 \times .025 = 1.6$ watts.

Incidentally, the voltage gain of the amplifier can be determined from the fact that a 10V change at the input results in a 30V change at the output; therefore, the gain from input to motor terminals is 3. The above circuit is shown in Figure 7.

THE POWER AMPLIFIER

Where space is tight and motor current is less than five amperes, the Unitrode PIC900 offers a perfect solution to your power bridge design. This device comes in a DIL-18 package, requires only 5mA of input drive current, and is rated at 5A absolute maximum output current. It contains all you need for the output H-bridge — including the circulating diodes — and with only a few added parts, you are ready to go. A circuit diagram showing a velocity feedback loop using one UC1637 and one PIC900 appears in the UC1637 data sheet.

For higher currents, you will have to design your own amplifier, and for the purposes of this application note, a sample design is shown in Figure 8. Referring to that circuit, note that with $+V_S$ and $-V_S$ applied, if the inputs are left open, the power MOSFETs are all "off". If Drive A, for example, is driven to within 3.6V of either power rail, then the corresponding output is switched to that rail. Note that since the PNP and NPN junction transistors are by nature faster switching "on" than "off", while the MOSFETs are much faster than the junction transistors driving them, this connection provides a simple guarantee against cross-conduction. Also working toward this goal is the fact that the junction transistor can discharge the MOSFET's input capacitance faster than the 1K, 1W resistor can charge it. The arrangement shown in Figure 8 results in a transition time of about 1.5μS during which both MOSFETs in a given leg are off. This amount of time is a very small portion of the 33μS period toward which we are designing our example.

The power MOSFET transistors, in TO-220 package, are rated at 60V and 12A. The channel "on" resistance is quite low, 0.25 ohms at 8A, for the UFN533, resulting in low thermal losses. You can easily find other devices with even lower R_{DS} values, if needed, but as always, the price you pay is that you must pay the price.

Finally, a word about circulating diodes — conspicuous in Figure 8 by their absence. All power MOSFETs have an intrinsic rectifier, or body diode, a junction rectifier whose current rating is the same as that of the transistor. With the drive format provided by the UC1637, the two bottom MOSFETs (N-channel) are "on" during the time when motor current circulates, and as a result, the reversed diode carries only a small portion of the current; most of it flows from source to drain through the channel. In fact, the diode fully conducts only during the 1.5μS when both devices in one bridge leg are off. You can add fast recovery diodes in shunt with the MOSFETs if you find that they are essential. The intrinsic MOSFET diode is not particularly fast, and as your output current requirements increase, the need for fast external diodes will become more and more apparent.

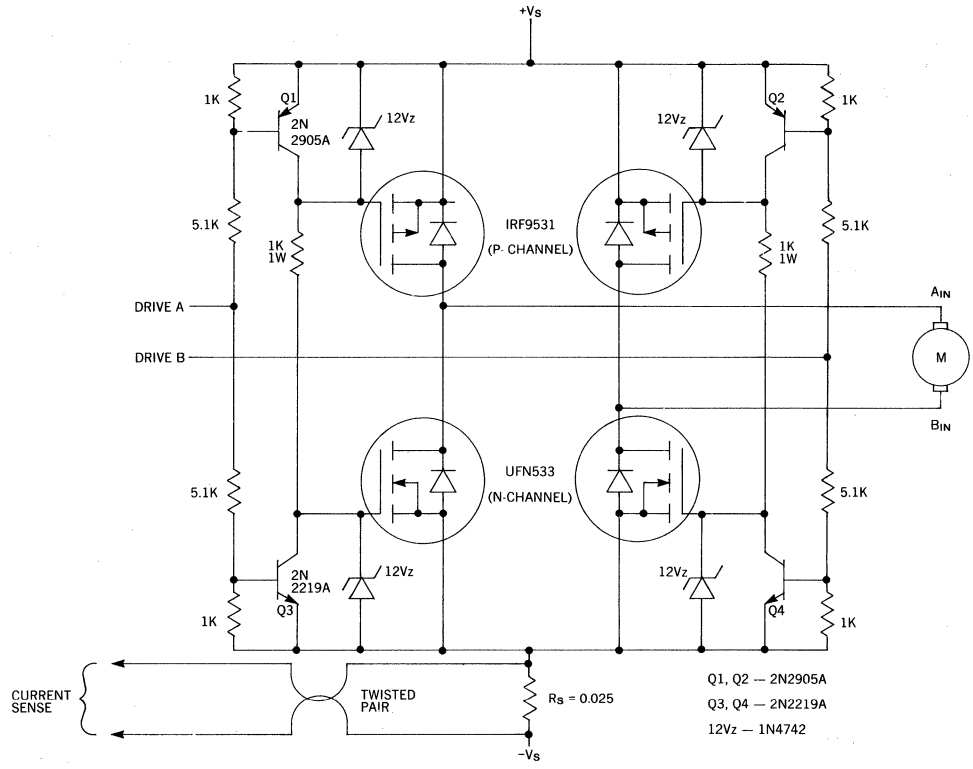


FIGURE 8. THIS 8A POWER AMPLIFIER IS SUITABLE FOR 30KHz OPERATION.

THE SERVOMOTOR

It is convenient to represent the DC servomotor by a simple equivalent circuit, and one such circuit is shown in Figure 9. Note that by expressing the moment of inertia J and the motor constant K in metric units (Nm sec^2 and Nm/A respectively), we avoid the need to include a multiplying constant in the expressions for C_M and e_o. Also, the motor constant K, in metric units, defines both the voltage constant in volt-sec/rad, and the torque constant in Nm/A, as one and the same number.

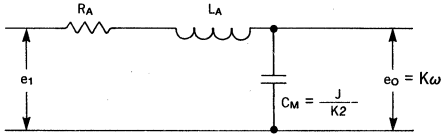


FIGURE 9. EQUIVALENT CIRCUIT OF MOTOR, WHERE J IS THE TOTAL MOMENT OF INERTIA OF ROTOR PLUS LOAD.

R_A = armature resistance; ohms.
L_A = armature inductance; henrys.
C_M = equivalent capacitance; farads.
J = total moment of inertia; Nm sec^2.
K = motor constant; volt sec/rad, or Nm/A.
ω = rotor angular velocity; rad/sec.

TO CONVERT FROM	TO	MULTIPLY BY
oz in sec^2	Nm sec^2	7.06×10^{-3}
volts/KRPM	volt sec/rad	9.55×10^{-3}

The ratio J/K^2 has the dimensions of capacitance, with a value runnng to several thousand microfarads. The voltage across this capacitor is equal to $K\omega$ where ω is the angular velocity of the rotor in rad/sec. Consequently, this voltage is the analog of shaft velocity.

Our equivalent circuit, then, is a simple series connection of R_A, the armature resistance; L_A, the armature inductance; and C_M, the equivalent capacitance, equal to J/K^2. It should come as no surprise that such a circuit will have a natural resonant frequency ω_N, and a resonant Q as well. This is indeed the case, and we have for its transfer function,

$$\frac{e_{o(s)}}{e_{i(s)}} = \frac{1}{(s/\omega_N)^2 + s/Q\omega_N + 1} \quad (12)$$

where $\omega_N = \dfrac{K}{\sqrt{L_A J}}$ (13)

and $Q = \dfrac{K}{R_A}\sqrt{\dfrac{L_A}{J}}$ (14)

We can now use these sample results in our sample design. Here are some of the data given by a motor manufacturer:

EG & G TORQUE SYSTEMS
MODEL NO. MT-2605-102CE
(motor - tach assembly)

MOTOR: K_T = 4.7 oz in/amp
K_V = 3.5V/KRPM
R_A = 0.7 ohms
J_M = 0.0018 oz in sec^2
τ_M = 8.6 ms (mech. time const.)
τ_e = 1.6 ms (el. time const.)
TACH: J_T = 0.001 oz in sec^2
K_V = 3V/KRPM

The several motors in this series and size have the same electrical time constant τ_E, and since we know R_A,

$L_A = \tau_E R_A = 0.016 \times 0.7$
L_A = 1.12 mH

The total moment of inertia is

$J = J_M + J_T = 0.0018 + 0.001$
J = 0.0028 oz in sec^2

In metric units,

$$J = \frac{0.0028}{141.612} \text{ (Nm sec}^2\text{)}$$

Putting K_T in metric units,

$$K = \frac{4.7}{141.612} \text{ (Nm/amp)}$$

The equivalent capacitance is

$$C_M = \frac{J}{K^2} = \frac{141.612 \times 0.0028}{(4.7)^2} = 18{,}000\mu f$$

For the equivalent circuit, then, the values are

R_A = 0.7 ohms
L_A = 1.12 mH
C_M = 18,000μf

The angular velocity will be proportional to the voltage e_o across C_M;

$$\omega = \frac{e_o}{K}$$

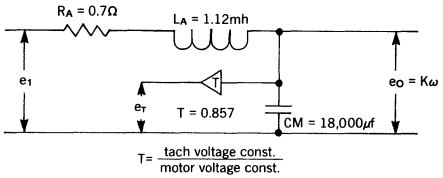


FIGURE 10. THE TACH VOLTAGE e_T IS PROPORTIONAL TO ω.

If the motor has a tachometer attached, we can include it in the equivalent circuit by deriving an equivalent tach voltage proportional to e_o. This is illustrated in Figure 10, where

$$T = \frac{\text{Tach. voltage constant}}{\text{Motor voltage constant}}$$

$$T = \frac{3\text{V/KRPM}}{3.5\text{V/KRPM}} = .857$$

From Eq. 13, ω_N = 222.7 rad/sec

From Eq. 14, Q = 0.356

(Note: Since $\zeta = \frac{1}{2Q}$, the damping factor here is 1.4)

From Eq. 12 and the above data, we can write the ratio of tach voltage to input as

$$\frac{e_T(s)}{e_1(s)} = \frac{.857}{\left(\frac{s}{222.7}\right)^2 + \frac{s}{79.3} + 1} \qquad (15)$$

THE VELOCITY LOOP

Our objective is to put together a feedback loop using our UC1637, H-bridge, and motor: the controlled variable is ω, the motor shaft's angular velocity. For high accuracy, we need a high loop gain, so that small velocity errors are magnified and corrected. The UC1637 internal ERROR amplifier is appropriate for this purpose, and will be used as a summing amplifier. But before proceeding, let us take a look at Figure 11, where a plot of the motor-tach transfer function (Eq. 17) is shown. The plot shows that as the frequency increases, the tach output decreases and the phase lag increases towards a maximum of 180°. This means that although we can introduce plenty of gain at very low frequencies, where the phase lag is low, the added gain must be reduced at the higher frequencies, where the 180° phase lag tends to make our loop a regenerative one. If we want the closed loop response to be "snappy", that is, if we want a bandwidth of several tens of hertz, then the loop gain must be

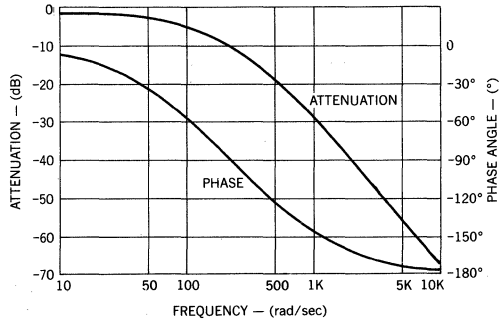
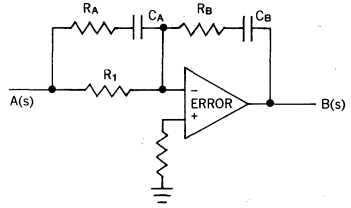


FIGURE 11. PLOT OF MAGNITUDE AND ANGLE OF EQ. 15, WHICH DESCRIBES PERFORMANCE OF OUR TEST MOTOR.

fairly high at all frequencies in the band; yet, for flat response and fast step response with no overshoot we must make certain that the overall phase shift is less than 180° at any frequency at which the gain is greater than unity.



$$\frac{A(s)}{B(s)} = \frac{(1 + sR_BC_B)\,[1 + s(R_1 + R_A)\,C_A]}{sR_1C_B\,(1 + sR_AC_A)}$$

FIGURE 12. ERROR AMPLIFIER WITH ITS FREQUENCY COMPENSATION NETWORK.
THE MAGNITUDE AND ARGUMENT OF THE TRANSFER FUNCTION CAN BE EASILY PLOTTED WITH THE AID OF A PROGRAMMABLE CALCULATOR.

The high gain ERROR amplifier of the UC1637, together with a few external components, is shown in Figure 12. Without R_A and C_A, the phase response of the circuit would go from −90° at low frequencies to 0° at high frequencies. This amount of phase correction is inadequate if we want a tight loop with good transient response. With R_A and C_A shunting R_1, it becomes possible to have a leading phase angle

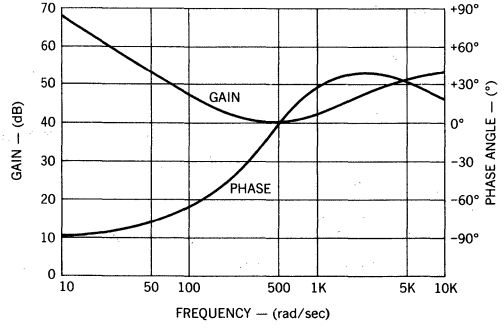


FIGURE 13. MAGNITUDE AND ANGLE OF COMPENSATION AMPLIFIER OF FIGURE 12.

somewhere at midrange, even though the high frequency asymptote is still at zero degrees (R_A and C_A introduce both a zero and a pole). The transfer function of the circuit shown in Figure 12 is plotted in Figure 13 for the following component values:

R_1 = 9.1K
R_A = 1K
C_A = .22μf
R_B = 470K
C_B = .0047μf

The break frequencies are:

$$\frac{1}{R_BC_B} = \frac{1}{(R_1 + R_A)\,C_A} = 450 \text{ rad/sec}$$

$$\frac{1}{R_1C_B} = 23{,}400 \text{ rad/sec}$$

$$\frac{1}{R_AC_A} = 4{,}500 \text{ rad/sec}$$

The plot shown in Figure 14 shows the result of cascading the compensation amplifier, PWM amplifier, and motor-tach. All gain contributions have been simply added together, and all phase contributions have also been added. The result, shown in Figure 14, shows the open loop frequency response of the complete velocity control system.

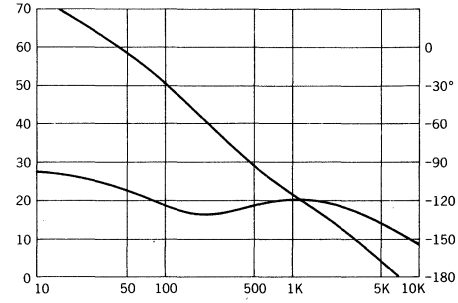


FIGURE 14. OVERALL OPEN-LOOP RESPONSE, INCLUDING +8dB DUE TO PWM AMPLIFIER GAIN AND MOTOR-TACH DC GAIN.

The inclusion of the ERROR amplifier with its compensation components has had the effect of introducing a large amount of gain at the lower frequencies, and also of reducing the phase lag at the higher frequencies. The loop gain is 0dB at about 7KHz, and the phase margin is about 40°.

Moreover, since the phase never exceeds 180°, we have the needed indication of *relative stability*, and can proceed to close the loop as shown in Figure 15 and make measurements. Note that a noise filter has neen added at the output of the tachometer. Such a filter is usually necessary, especially in PWM control loops of relatively wide bandwidth, because of the inevitable AC coupling between the motor signal and the tach output. In our filter, the 3dB cut-off point is at 21KHz, which is high enough not to affect the loop behavior.

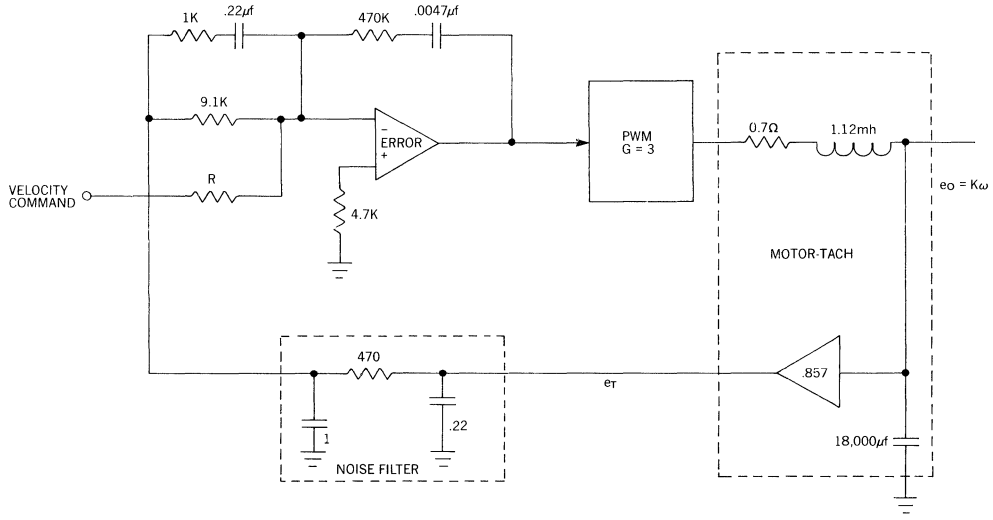
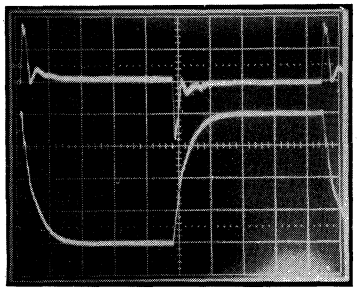


FIGURE 15. THE COMPLETE VELOCITY LOOP.

The oscilloscope trace shown in Figure 16 reveals that the step response of our loop is very well behaved. The motor shaft reaches full speed in less than 10mS, and there is no noticeable overshoot. The net velocity change in Figure 16 amounts to 133 RPM, and the current trace shows that the current does not quite reach the chosen limit of 8A. With larger input steps, the motor accelerates at constant 8A current, and the acceleration rate is approximately 100RPM per millisecond. The 3dB bandwidth of the loop measured about 80Hz.



Top trace: 5A/cm
Bottom trace: 100mV/cm
Horizontal: 5 msec/cm

FIGURE 16. STEP RESPONSE OF THE VELOCITY CONTROL LOOP OF FIGURE 15. THE UPPER TRACE SHOWS THE MOTOR CURRENT; THE LOWER TRACE SHOWS THE TACH OUTPUT VOLTAGE, I.E., MOTOR VELOCITY.

CONCLUSIONS

We have discussed in some detail the characteristics of Unitrode's UC1637 and have presented in detail a design approach which illustrates those points. The sample design was built and tested, with the measured results as presented above. These results show that excellent performance can be obtained with few components, and that the design technique is quite simple. Our velocity loop would perform well as an inner loop in a position control system, for example, although a different response might perhaps be desirable. However that may be, using the UC1637 a sizable portion to the job is completed beforehand.

See Figure 17.

ACKNOWLEDGMENTS

We are grateful to EG & G Torque Systems for providing the motor-tachometer used in the sample design.

The Electro-Craft Corporation generously supplied a copy of their engineering handbook on DC Motors, 5th Edition. This book is highly recommended.

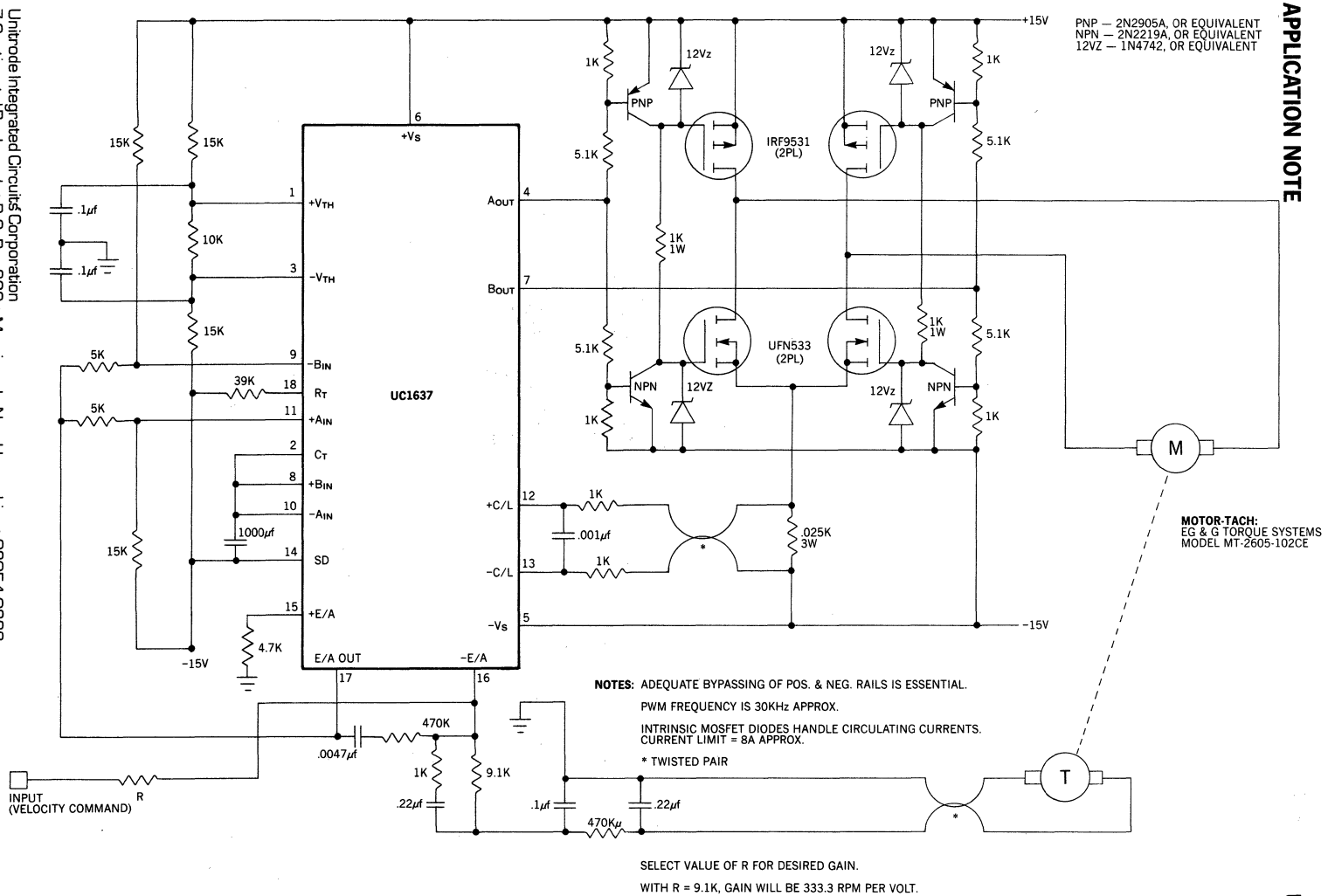


FIGURE 17. COMPLETE VELOCITY CONTROL LOOP OF SAMPLE DESIGN.

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IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

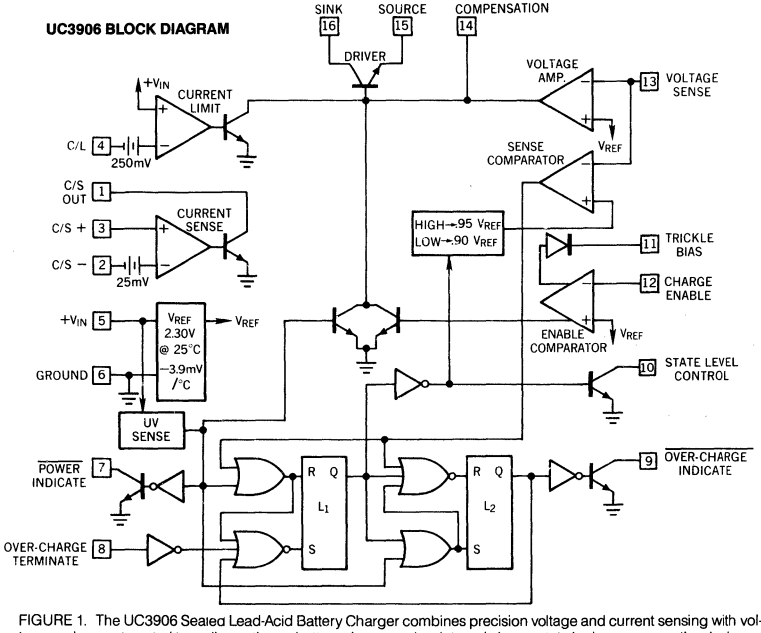

FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger. The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, −40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.

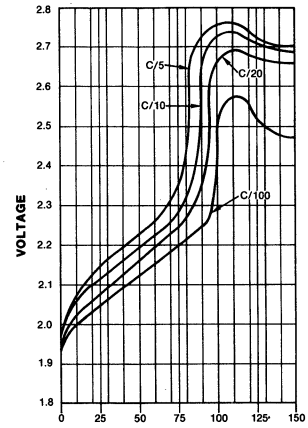

FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products, Inc.)

Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately –4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

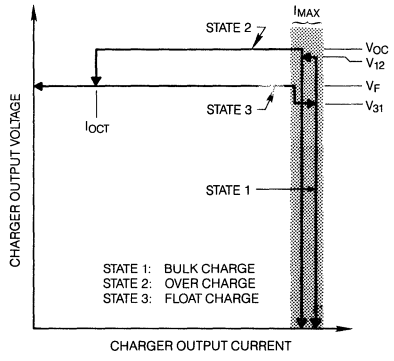

FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger. Internally, the starting of the over-charge state arms the set input of the first latch — assuming no reset signal is present — so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, ($25mV/R_S$), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

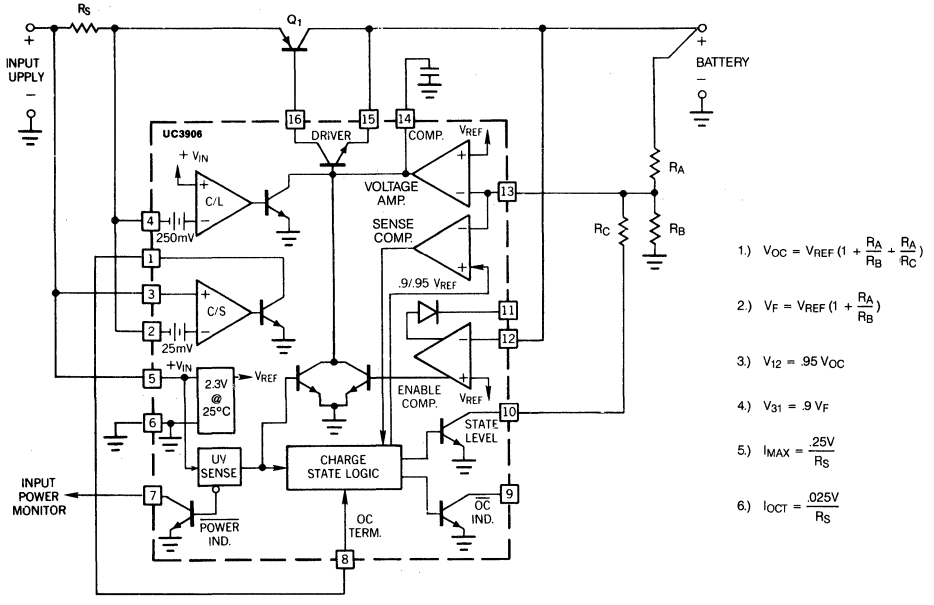

FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

-3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

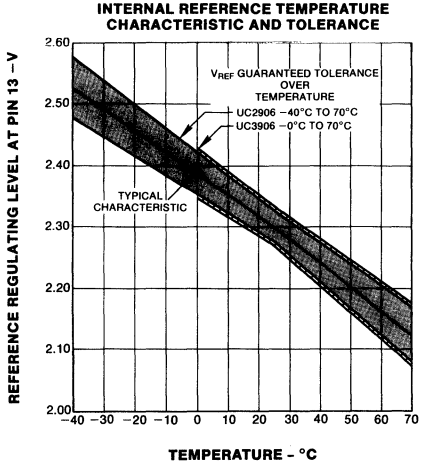

FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C, (-40 to 70°C for the UC2906), to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

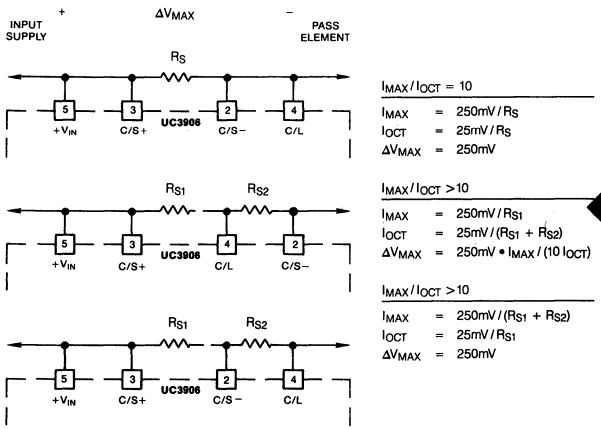

FIGURE 6. Although the ratio of input offset voltages on the current limit and current sense stages is fixed at 10, other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater than 10 is increased voltage drop across the sensing network at I_{MAX}.

of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element. As shown in figure 7, the enable comparator input taps off the battery sensing divider. When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-

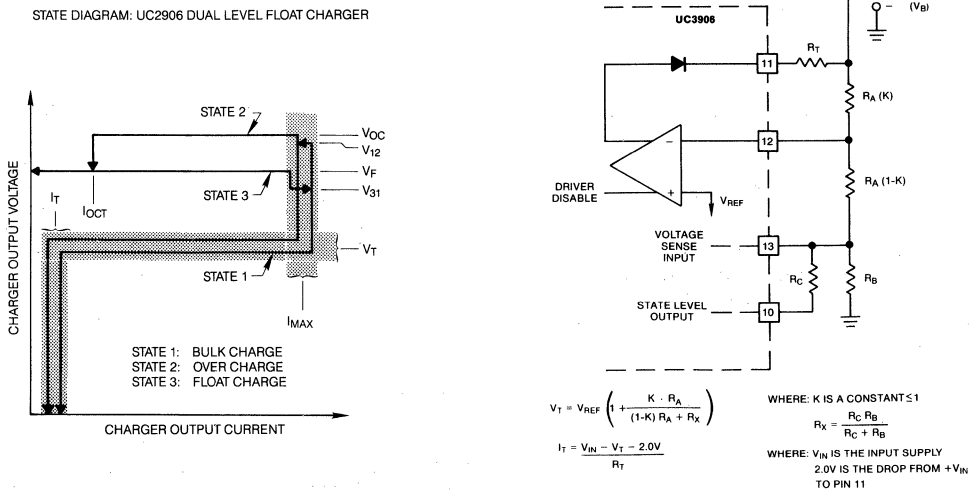

FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor C1 supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

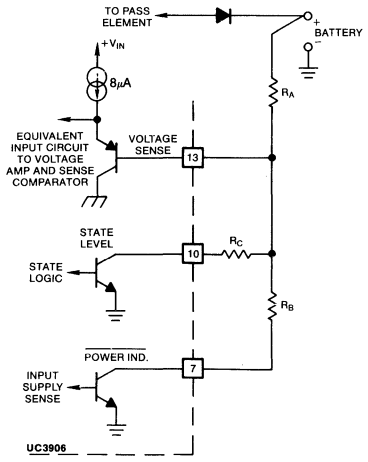

FIGURE 8. By using a diode in series with the pass element, and referencing the divider string to the power indicate pin, pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, I_H, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

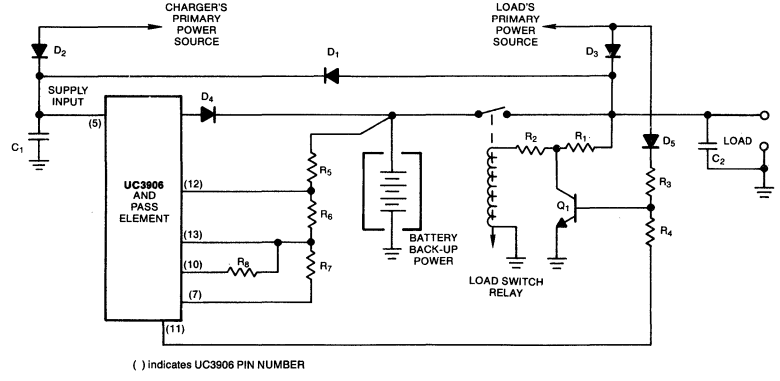

FIGURE 9. Using the enable comparator to monitor the battery voltage a precise discharge cut-off voltage can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (>25mA), then an external buffering element may be required at the output of the current sense comparator.

The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.

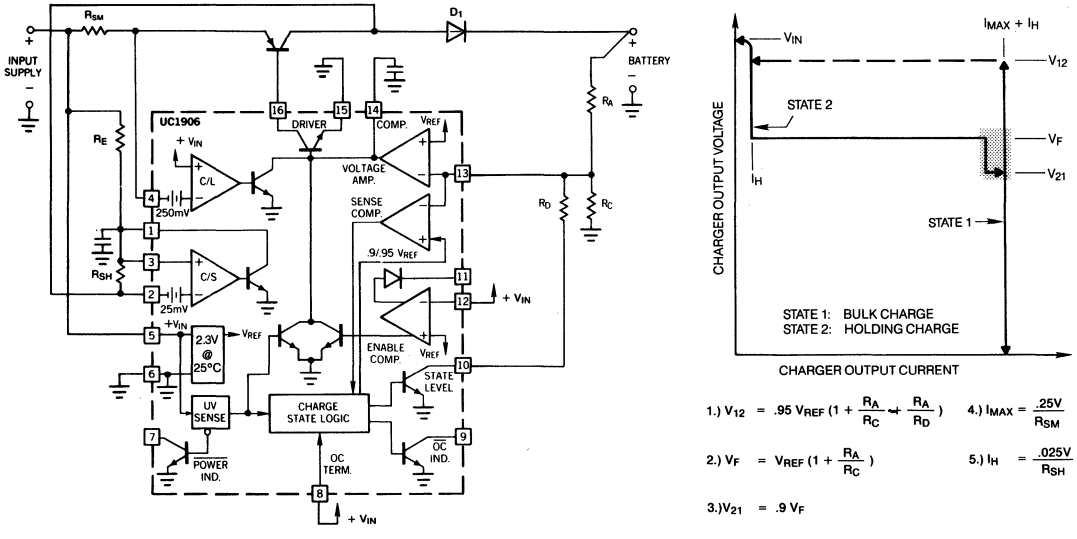

FIGURE 10. A dual step current charger has some advantages when large series strings must be charged. This type of charger maintains constant current during normal charging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to

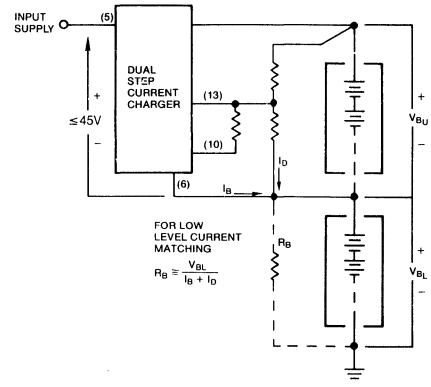

FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bias and divider currents.

the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
TOPOLOGY	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER
CURRENT RANGE	25mA < I < 1000mA	25mA < I < 1000mA	600mA < I < 15A	25mA < I < 1000mA
MINIMUM ΔV	ΔV > 0.5V	ΔV > 2.0V	ΔV > 1.2V	ΔV > 2.7V
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\beta_{Q2}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \cdot I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \cdot \beta_{Q1\,MIN}\,\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \cdot \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot Z_O \cdot \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \cdot \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{R_D + 12} \cdot \beta_{Q1} \cdot \beta_{Q2} \cdot R_S$	$A_{OC} \approx \frac{Z_C}{300} \cdot \frac{1}{12/\beta_{Q1} + Z_O} \cdot R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. = IMPEDANCE AT CHARGER OUTPUT.

FIGURE 12. There are a large number of possible driver/pass element configurations, a few are summarized here. The trade-offs are between current gain, input to output differential, and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by adding a resistor in series with the UC3906 driver.

(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by –3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage . . . . . 9.0V to 13V
Operating temperature range . . . . . 0°C to 70°C
Start-up trickle current (I_T) . . . . . 10mA (V_{IN} = 10V)
Start-up voltage (V_T) 5.1V
Bulk charge rate (I_{MAX}) 500mA (C/5)
Bulk to OC transition voltage (V_{12}) . . 7.125V
OC voltage (V_{OC}) 7.5V
OC terminate current (I_{OCT}) 50mA (C/50)
Float voltage (V_F) 7.0V
Float to Bulk transition voltage (V_{31}) 6.3V
Temperature coefficient on voltage levels . . . . . –12mV/°C
Reverse current at charger output with the input supply at 0.0V . . . . $\leq 5\mu A$

In order to achieve the low input to output differential, (1.5V), the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

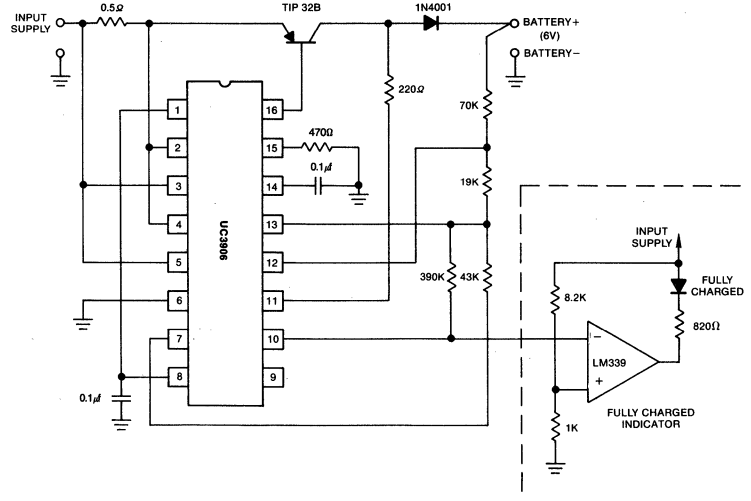

FIGURE 13. This dual level float charger was designed for a 6V (three 2V cells) 2.5AH battery. A separate "fully charged" indicator was added for visual indication of charge completion.

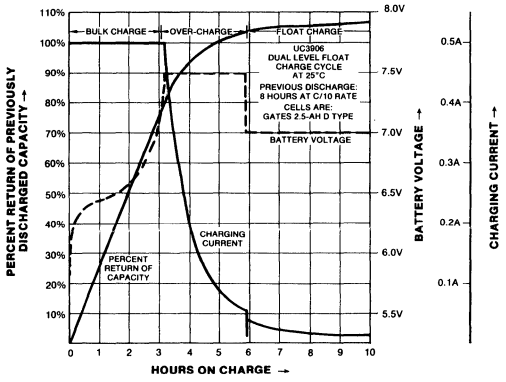

FIGURE 14. The nearly ideal characteristics of the dual level float charger are illustrated in these curves. The over-charge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

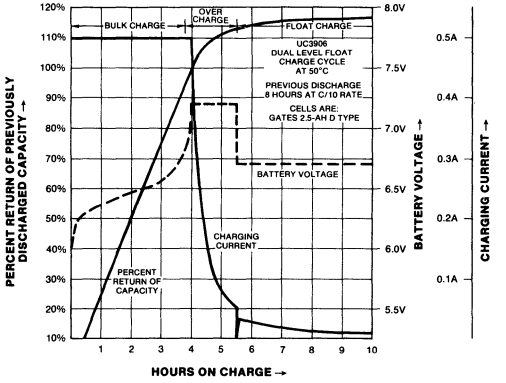

FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge acceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

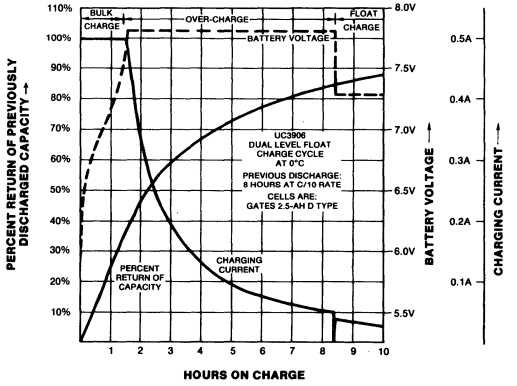

FIGURE 16. At lower temperatures the capacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

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1. Eagle-Picher Industries, Inc., Battery Notes #200, #205A, #206, #207, #208.
2. Gates Energy Products, Inc., Battery Application Manual, 1982.
3. Panasonic, Sealed Lead-Acid Batteries Technical Handbook.
4. Yuasa Battery Co., Ltd., NP series maintenance-free rechargeable battery Application Manual.

9

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UC3620
BRUSHLESS DC MOTORS GET A CONTROLLER IC THAT REPLACES COMPLEX CIRCUITS

A COMMUTATOR AND DRIVER CHIP, COMPLETE WITH THERMAL AND UNDER-VOLTAGE PROTECTION AND TRANSIENT SUPPRESSION, RADICALLY SIMPLIFIES THE CONTROL OF BRUSHLESS DC MOTORS

INTRODUCTION

The popularity of the three-phase, brushless DC motor is on the rise for a number of good reasons: There are no brushes to wear out or to arc over, heat dissipation is better because the windings are on the stator, and good torque control is both possible and relatively easy to achieve with the availability of electronic circuits. The motor's main drawback has been the need to design and assemble a complex circuit consisting of six output power transistors with transient suppression diodes, a switching current control circuit, and a Hall logic decoder, plus loop control and protection circuitry.

The advent of the UC3620 controller chip greatly simplifies the designer's problem, for it integrates all these elements. This chip easily and safely controls motors requiring up to 2A of continuous current, and has a peak rating of 3A. The device has a maximum V_{CC} rating of 40V and is available in a 15-pin package rated at 25W. Only a half dozen external components are needed to get a motor running.

A three-phase brushless DC motor has two, four, or more permanent magnet poles mounted on its rotor. The required rotating field is produced by the stator's stationary windings, whose three phases must be commutated in the proper sequence. This sequence is governed by the rotor's angular position, and consequently, some means must be provided both to sense this position and to use that information to control the commutation sequence.

The sensing is accomplished by three Hall-effect devices mounted on the stator close to the rotor magnets, at the correct rotational angles. An electronic circuit decodes the Hall device signals and controls the direction of the currents applied to the three motor phases. This power switching is done by power transistors.

Another function must be added to the driving electronics, namely, that of controlling the motor current and maintaining it at the correct value. At high speed, the electric motor's back emf limits the phase currents. But at low speeds, the back emf is low (it is zero at stall), and therefore if the current is to be kept constant, the applied voltage must be reduced. This is done by sensing the motor current and using its value to regulate the duty cycle of the applied voltage, thereby controlling the average motor voltage. In this way, a constant-current source of motor power is obtained.

HOW IT WORKS

In the controller chip, each of the three output stages is a totem-pole pair (Figure 1) capable of sourcing and sinking the motor's full rated current. Inductive transients from the load are clamped to V_{CC} by Schottky diodes and to ground by the intrinsic substrate diodes, thus obviating the need for external clamping devices.

The power output stages have two functions. The first is to commutate the three motor phases in the proper sequence, producing unidirectional torque in the rotor. The second is to switch the applied motor voltage in the manner selected and programmed by the user, maintaining the output current at the desired level. This switching control of current is accomplished in a fixed-off-time, two-quadrant mode, providing the automatic peak current limiting and low ripple current essential to high electrical efficiency at the motor windings.

The emitters of the three bottom transistors of the totem-pole output stages are connected to Pin 1, through which all the motor current flows. If a low-value resistor is placed between this pin and ground, a usable voltage proportional to motor current is derived without appreciable I^2R losses.

This current-sensing voltage serves as a feedback signal for the switching current control loop. It is applied to the I_{SENSE} input through an RC filter, which prevents false triggering due to noise spikes in the current waveform.

An internal voltage comparator determines whether the voltage $V_{I\ SENSE}$ is equal to V_{REF}, a positive variable reference voltage dependent on the output of the chip's error amplifier. If Q of the monostable multivibrator (that follows the comparator) is high, the chip's output stages are enabled, the output current increases, and $V_{I\ SENSE}$ also increases until it becomes positive with respect to V_{REF}.

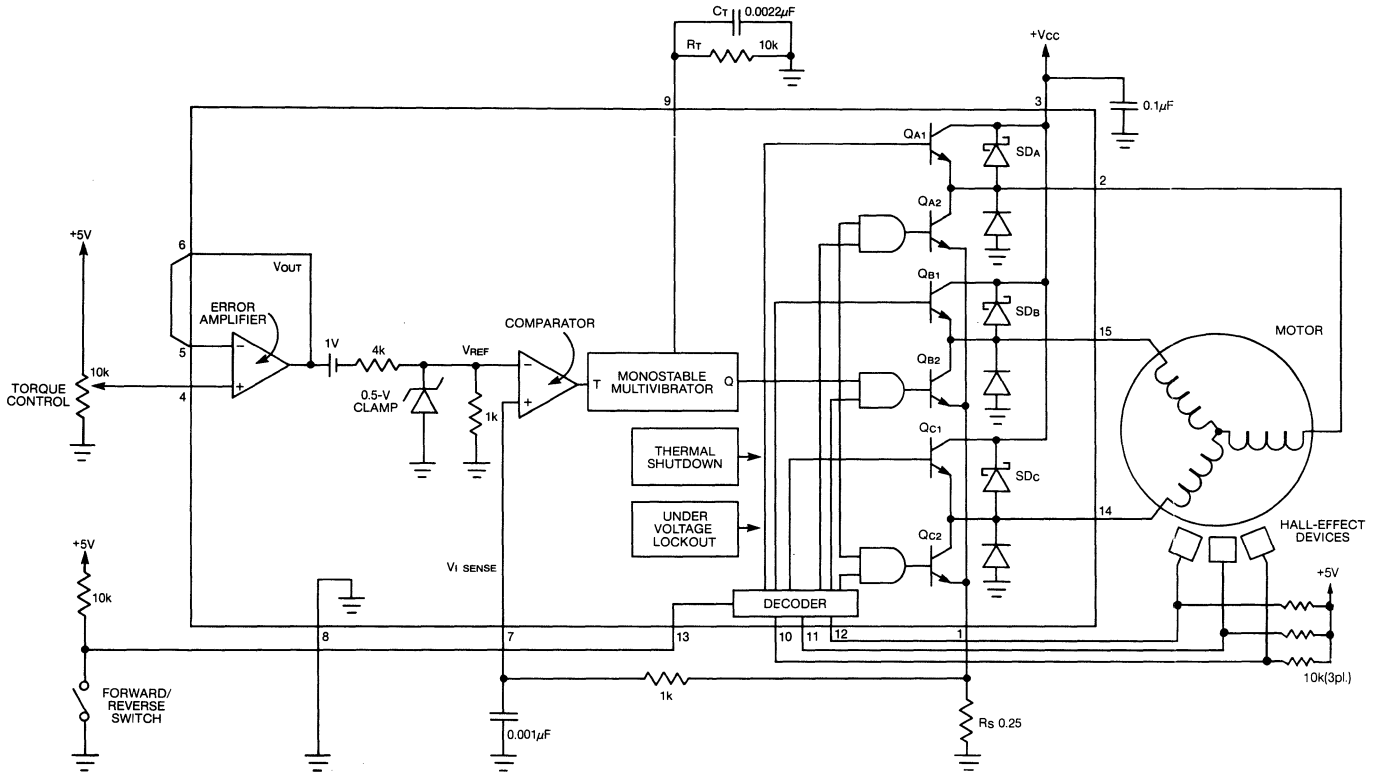


FIGURE 1. THE UC3620 CHIP PROVIDES FULL CONTROL OF MOTOR CURRENTS UP TO 2A, WITH ROTATION IN BOTH DIRECTIONS. HALL-EFFECT DEVICES INTERNAL TO THE MOTOR PROVIDE POSITION INFORMATION THROUGH A DECODER TO THREE TOTEM-POLE DRIVERS. COMPARING THE CHANGING VOLTAGE ACROSS R_S WITH THE ERROR AMPLIFIER OUTPUT HELPS KEEP THE CURRENT CONSTANT.

At this point the comparator resets the monostable, forcing Q low and disabling the output stages. The motor current now circulates through one of the Schottky diodes and the conducting upper transistor because of the stored inductive energy, until the monostable off-time has elapsed (Figure 2). Q then returns to the high state and the cycle is repeated.

The switching off-time is fixed, since it is determined by the user's choice of timing components R_T and C_T. At the start of the off-time, capacitor C_T is charged to +5V, and the monostable outputs are held in the off state until this voltage decays exponentially to a level of 2V. Since resistor R_T supplies the only path for the discharging current, it is possible to calculate the time required, t_{OFF}, in seconds:

$$\exp\left(\frac{-t_{OFF}}{R_TC_T}\right) = \frac{2}{5}$$

or:

$$\frac{-t_{OFF}}{R_TC_T} = \ln(2/5) = -0.916$$

$$t_{OFF} = 0.916R_TC_T$$

When the 2 volt level is reached, the monostable is set again, and the cycle repeats.

The reference voltage, V_{REF}, then, is the controlling voltage of what is in effect a transconductance amplifier of which the controlled output is the motor current through resistor R_S. To repeat, the circuit controls the peak value of the current. If the switching frequency is high (low current ripple), the assumption may be made that the average value of motor current, I_M, is approximately equal to the peak, and so:

$$V_{REF} = I_MR_S$$

$$G_T = \frac{I_M}{V_{REF}} = \frac{1}{R_S} \text{ Siemens}$$

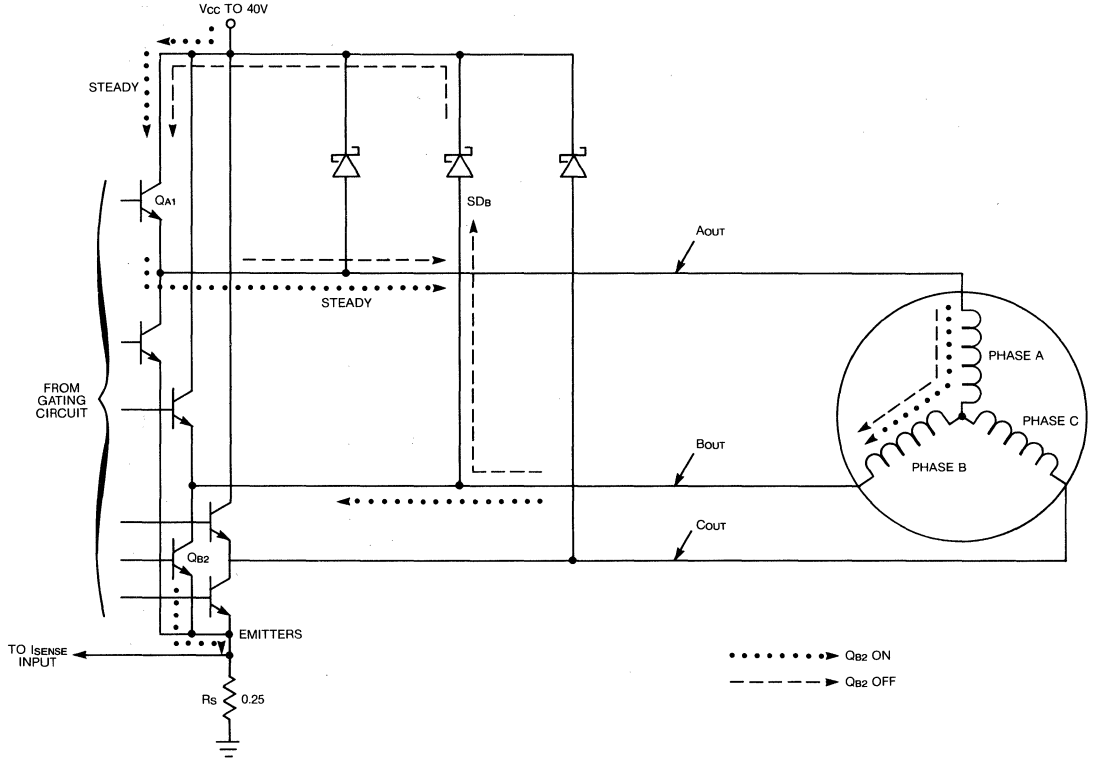


FIGURE 2. WHEN Q_{B2} IS ON, CURRENT FLOWS THROUGH Q_{A1} AND TWO MOTOR WINDINGS TO GROUND (DOTTED ARROWS). DURING THE TIME THAT Q_{B2} IS OFF, THE STORED ENERGY IN THE WINDING INDUCTANCE FLOWS THROUGH SCHOTTKY DIODE SD_B, TRANSISTOR Q_{A1}, AND BACK THROUGH THE WINDINGS (DASHED ARROWS).

The maximum value of V_{REF} is limited to 0.5V by a zener diode (Figure 1 again). This value sets a limit to the maximum motor current as well, since:

$$I_{MAX} = \frac{0.5}{R_S} \text{ amperes}$$

Consequently, the proper selection of R_S protects both the motor and the chip from excess current.

The motor is connected to the chip's three outputs A_{OUT}, B_{OUT}, and C_{OUT}. The motor windings are Y-connected, and the driver energizes two phases at a time, the third one being off. Thus each driver output will be in one of three states: high (V_{CC}), off (high impedance), or low (0V), generating six possible combinations (Table 1).

Table 1. Terminal Conditions for Different Driver Output States

OUTPUT STATE	TERMINAL A	TERMINAL B	TERMINAL C
$A\bar{B}Z$	High	Low	High Z
$AZ\bar{C}$	High	High Z	Low
$ZB\bar{C}$	High Z	High	Low
$\bar{A}BZ$	Low	High	High Z
$\bar{A}ZC$	Low	High Z	High
$Z\bar{B}C$	High Z	Low	High

SIX STATES

In each of the six possible states, one of the upper transistors is on, together with one of the bottom transistors. In any of the states, it is the bottom transistor that controls switching, while the upper device remains conducting. For example, in state $A\bar{B}Z$, current flows continually through upper transistor Q_{A1}, but switches between lower transistor Q_{B2} and Schottky diode SD_B (Figure 2 again). This switching action results in low current ripple through the motor and is known as two-quadrant operation, in which the power supply current flows only in one direction, namely, into the driver (Figure 3). One advantage of this unidirectionality is that a shunt regulator is not necessary to prevent an overvoltage at the V_{CC} bus during motor deceleration.

A more significant advantage is that it results in the least current ripple for a given switching rate. More precisely, the current waveform's form factor (the ratio of its rms to its average value) is closer to unity. Since the amount of I^2R heating depends on the rms value of I, whereas torque depends on the average value, a form factor approaching unity results in greater motor efficiency.

The current reference voltage V_{REF} at the inverting input of the chip's comparator depends on the output voltage, V_{OUT}, of the error amplifier. The relationship between the two is:

$$V_{REF} = \frac{V_{OUT} - 1}{5}$$

The offset of 1V between V_{OUT} and the 5:1 voltage divider ensures that the error amplifier can always achieve zero current at the motor. The amplifier itself has a high gain of 80dB minimum, an f_t of 0.8MHz; and is internally compensated for stable operation.

In a feedback speed control application, even with a reduction in gain of 14dB due to the 5:1 resistive attenuator between the amplifier and the comparator, there is still a minimum DC gain of 66dB, which is more than adequate for most requirements. The same consideration applies to the 1V offset, which is overshadowed by the high-gain loop as well.

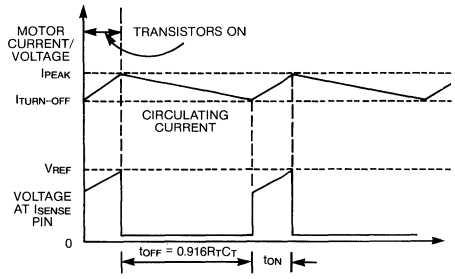


FIGURE 3. THE CHIP'S SWITCHING CIRCUIT CONTROLS MOTOR CURRENT ON A PULSE-BY-PULSE BASIS. WHEN THE BOTTOM TRANSISTOR OF AN OUTPUT STAGE IS ON, THE CURRENT AT FIRST RISES RAPIDLY AND THEN DECAYS SLOWLY AS IT CIRCULATES THROUGH THE TRANSISTOR'S ASSOCIATED DIODE. THE FORM FACTOR OF THE WAVEFORM IS THEREFORE CLOSE TO UNITY, SO THAT HEATING OF THE COILS IS REDUCED.

The chip also includes two protection circuits to help make it more reliable. The under-voltage lockout prevents the output stages from being energized unless the supply voltage can provide sufficient base current to the drive transistors. The maximum V_{CC} start-up threshold is set at 8V and has a built-in hysteresis of 0.5V.

A thermal shutdown circuit affords protection against excessive junction temperatures. This circuit disables the drive transistors when the chip's temperature is between 150°C and 180°C. When the temperature returns to a safe value, normal operation is automatically restored.

When the power source for a motor is DC, a commutator is needed to, in a sense, alternate the power applied to the windings. A brushless DC motor uses an external power commutator. As a rule, however, the motor has an electronic device internal to it that generates information relative to angular position for use in controlling the commutator.

CONTROLLING BRUSHLESS MOTORS TO 2A

The control chip was designed to drive any three-phase brushless DC motor of up to 2A and is particularly suited for motors with integral Hall-effect devices. H_A, H_B, and H_C (Figure 1 again) are TTL-compatible inputs that, together with the Forward-Reverse input (FWD/REV), determine the output states (Table 2).

The commutation logic built into the UC3620 is intended for use with motors with 120 electrical degree Hall codes. Motors that use the alternative 60 electrical degree code can be easily accomodated with the addition of an inverter to reverse polarity of one of the Hall signals.

When used as described, the device operates in a current feedback mode and acts as a current controller, or rather as a transconductance amplifier. This closed-loop circuit can be made part of another feedback loop to control the motor speed. Controlled speed loops are of interest in many applications, some of which require a very high degree of control accuracy. For example, a crystal-referenced phase-locked loop is needed to control the spindle speed of magnetic disk drives.

Table 2. Hall Device Logic Coding

HALL DEVICE INPUTS			FORWARD/ REVERSE LINE	DRIVER OUTPUT
H_A	H_B	H_C		
1	0	1	1	$A\bar{B}Z$
1	0	0	1	$AZ\bar{C}$
1	1	0	1	$ZB\bar{C}$
0	1	0	1	$\bar{A}BZ$
0	1	1	1	$\bar{A}ZC$
0	0	1	1	$Z\bar{B}C$

Note: A change of state in the Forward/Reverse line inverts the output states, thus reversing the direction.

NEW PULSE WIDTH MODULATOR CHIP CONTROLS 1 MHz SWITCHERS

ABSTRACT

Controversy prevails as to the benefits of pushing switched mode pulse width modulated power supplies higher and higher in frequency. Two facts are undisputed though: the industry is pushing switching frequencies up daily and no PWM control IC has been available to optimally control circuits running above several hundred kilohertz. A new IC, the UC3825, has been developed with the top end of the PWM frequency spectrum in mind to simplify high speed control problems. This chip, suitable to either voltage or current mode control, addresses the speed critical parameters that have been glossed over in the past: error amp bandwidth, output drive capability, oscillator frequency range, and propagation delay. A one megahertz, 50 watt supply has been built to demonstrate the chip.

PWM CONTROLLER REVIEW

Briefly reviewing popular control IC's on the market today should serve to illustrate one source of the headaches belonging to designers of high frequency switching power supplies. The snaggle-toothed appearance of the table illustrates the fact that high speed parameters have generally been ignored. The entries in this table represent the tried and true first and second generation standbys (1524, 1525, 494), dedicated off line control (1840), and current mode (1846). All these architectural approaches have certainly proven sufficient for numerous converter designs, but all lack the processing speed required to keep track of a 1 MHz switcher, or even 200 kHz for that matter. Many specifications in the table are missing completely, some are only typical, and the few guaranteed limits leave much room for improvement.

Of prime importance here is the delay time between fault detection and turning off the power switch – the speed critical path. When a fault occurs, either the on chip over-current sense section or an off chip fault detector plus the shutdown section of the chip must work fast enough to turn off the power switch before destructive current levels introduce an automatic (and permanent) power down feature to the supply. This feature, of course, is manifested in blown power devices. The problem is aggravated at the onset of core saturation, since switch currents then rise at much faster rates.

Also important is the drive capability of the output stage of the control chip chosen. Rise and fall times must be consistent with switching speeds or else an output buffer will have to be added. This, of course, adds delay to the speed critical path placing tighter demands on the delays through the chip or forcing the designer to over-specify the power elements to insure fault survival. Over-specifying, however, adds cost, weight and volume as transistors, heat-sinks, and transformers are beefed-up. These consequences are in direct opposition to the very motives for going to higher frequencies in the first place – reduced volume and lower cost.

On-chip error amplifiers have also been a design obstacle in the past. Why build a high frequency switcher and then over compensate the loop due to lack of error amp bandwidth? Designers have been forced to conser-

SPEED COMPARISON OF PWM CONTROLLER IC'S

	SHUT DOWN DELAY (ns)		OVER-CURRENT SENSE DELAY (ns)		ERROR AMP BANDWIDTH (MHz)		ERROR AMP SLEW RATE (V/ s)		OUTPUT RISE/FALL TIME (ns)	
	TYP	MAX	TYP	MAX	TYP	MIN	TYP	MIN	TYP	MAX
SG3524	–	–	–	–	3	–	–	–	200	–
UC3524A	200	–	600	–	3	–	–	–	200	–
UC3525A	200	500	–	–	2	1	–	–	100	600
TL494	–	–	–	–	0.8	–	–	–	200	400
UC3840	–	–	200	400	2	1	0.8	–	–	–
UC3846	300	600	200	500	1	0.7	–	–	50	300
UC3825	50	80	50	80	5.5	3	12	6	30	60

9

vatively use the bandwidth available simply due to a lack of guaranteed specifications in many cases. Also, some characteristics which would prove useful haven't been specified at all. Slew rate is such a specification that has great bearing on the large signal response of the supply.

By comparison, the 3825 specifically addresses the speed critical parameters. Maximum propagation delays of 80 ns nearly belong in the "order of magnitude" improvement catagory. Slicing delays yielded a hefty output stage capable of 1.5 Amp peak currents. The guaranteed rise time is, in fact, more a function of internal slew rates than external loading in the 1000 pF range. The error amp guaranteed to 3 MHz and 6 V/μs promises ease of use when controlling wide-band loops.

UC3825 BLOCK DIAGRAM

The design philosophy for the 3825 was to build a chip faster than any other available and tailor it to fit neatly into high frequency converter designs. It includes a dual totem-pole output stage capable of driving most power mosfet gates stand-alone, and the versatility to be useful for DC to DC, off-line, bridge, flyback, push-pull, and even resonant mode converter topologies. The member of a family covering the conventional temperature ranges, the UC3825 is specified for zero to 70 degrees centigrade while the UC2825 spans −25 to 85, and the UC1825, −55 to 125.

The block diagram of the 3825 (figure 1) is architecturally similar in many respects to a number of previous PWM controllers. It includes an oscillator, under-voltage-lock-out circuit, trimmed bandgap voltage reference, wideband error amplifier, PWM comparator, PWM latch, toggle flip-flop, soft start section, comparators for over-current sensing and reinitializing soft start, and dual totem-pole outputs. The input to the PWM comparator is brought out to a separate pin so that it can be connected either to the timing capacitor for conventional PWM designs or a current sensing network for current mode control schemes.

In normal operation, the oscillator establishes a fixed clock frequency issuing blanking pulses to terminate one period and begin the next. These pulses serve to reset the PWM comparator while blanking the outputs off. After the blanking pulse, one output turns on until the ramp input (level shifted 1.25 Volts) exceeds the error amp output voltage. This sets the PWM latch which turns the output off and triggers the toggle flip-flop, selecting the other output for the next period.

THE SPEED CRITICAL PATH

The blocks that set the 3825 aside as the controller best suited for frequencies over several hundred kilohertz are those in the speed critical path (high-lighted blocks in figure 1.): the PWM comparator and current limit comparator in the front end; the PWM latch and associated internal logic; and the ouput stage. Signal

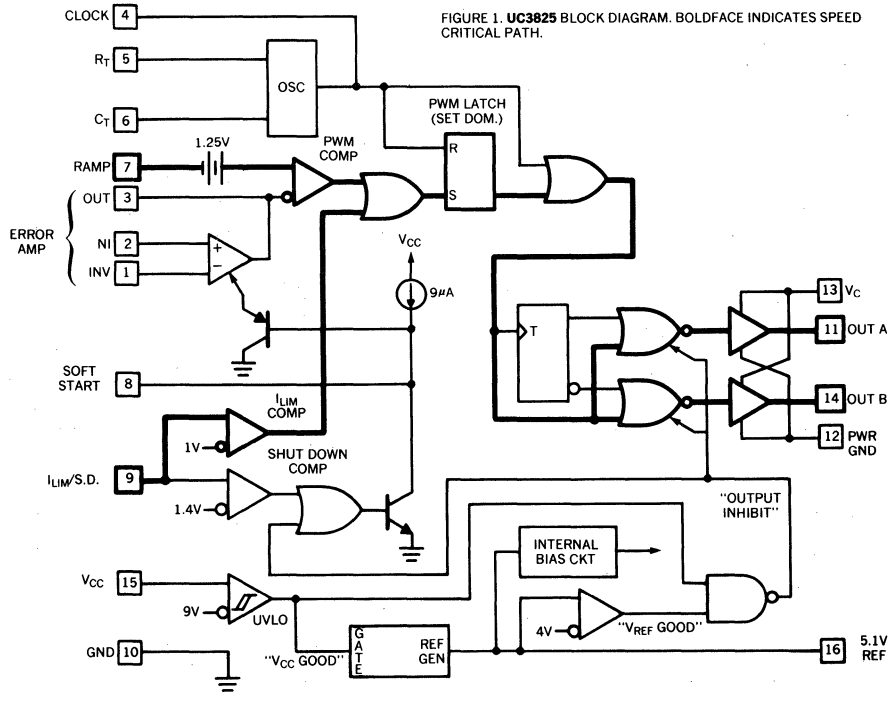


FIGURE 1. **UC3825** BLOCK DIAGRAM. BOLDFACE INDICATES SPEED CRITICAL PATH.

propagation through these subcircuits makes or breaks a design during a fault condition. In the 3825, the propagation delay from either the Ramp input or the Current-limit sense input to the output pins is typically 50ns, very much faster than any chip available today.

Comparators

The PWM comparator is basically an npn differential pair with an emitter follower output (figure 2a). The pair is biased so that the output swing is one Vbe. This guarantees none of the transistors in the comparator will saturate while providing output voltage levels compatible with the internal logic. In order to assure that the input common mode range of the comparator is not exceeded (the range of an npn input pair cannot go below approximately one Volt), a 1.25 Volt level shift is included between the non-inverting input of the comparator and the input pin of the chip. This allows the ramp input to swing from zero to approximately three Volts. The inverting input is tied directly to the output of the error amplifier.

The benefit of this approach is ease of use both in current mode and conventional PWM applications. For the older PWM circuit approach, the ramp input pin can be tied directly to the oscillator Ct pin while current mode users can simply tie a ground referenced current sense network directly to the Ramp pin.

The current limit comparator is very similar in design to the PWM comparator. Its inverting input is referenced internally to a one Volt level derived from the 5.1 Volt reference allowing the non-inverting input to be brought directly to the current limit pin. Functionally, when a fault causes the Current-limit pin to exceed one Volt, it acts just like the PWM comparator, setting the PWM latch and causing the outputs to remain off for the duration of the clock cycle.

The current-limit comparator can also be combined with the 3825 outputs and a few external components to form a constant volt-second product clamp (figure 2b). This clamp is useful in current mode systems to prevent core saturation during load transients. When either output turns on (goes high), capacitor, C, is charged from Vin through resistor, R. Normal circuit operation would turn off the outputs causing C to be discharged before it reaches one Volt. If, however, it does reach one Volt, the current-limit comparator terminates the output pulse. Since the charge rate is proportional to Vin (assuming Vin is much greater than one Volt), then a constant Volt-second product clamp of one Volt times RC is achieved.

Logic

All of the speed critical logic, including the PWM latch, the toggle flip-flop, and various gates are a cross between emitter coupled logic and emitter function logic. In either case, their speed relies on emitter coupled pairs and emitter follower buffers biased to insure that no transistor saturates. Although two OR's, a NOR and the PWM latch are directly in the critical path between the input comparators and the output drivers, they account for only twenty percent of the total delay, the remainder being shared between the comparators and the output stage.

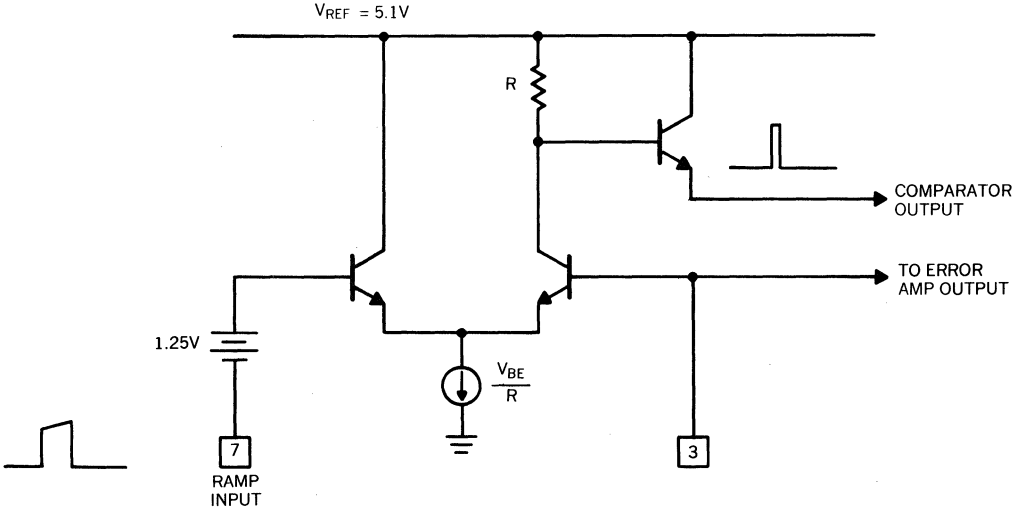
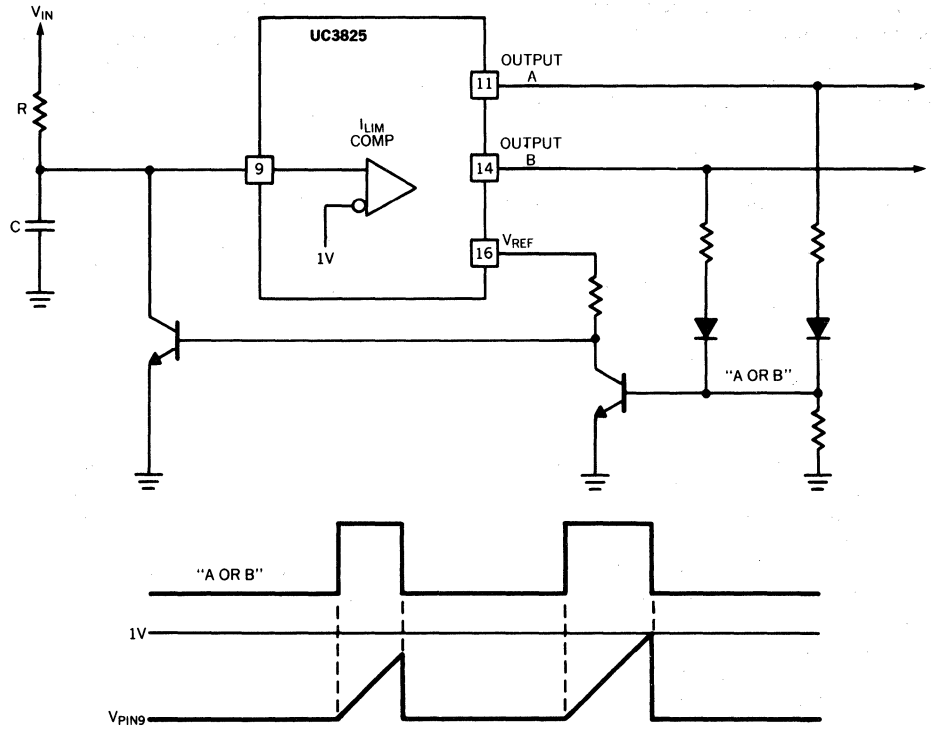


FIGURE 2a. PWM COMPARATOR SCHEMATIC.



MAXIMUM VOLT — SECOND PRODUCT = RC × 1V

FIGURE 2b. CONSTANT VOLT-SECOND PRODUCT CLAMP IMPLEMENTED USING THE CURRENT LIMIT COMPARATOR.

Outputs

Speed from one pin to another does little or no good unless the signal coming out of the chip has the strength to do its job. The dual totem-pole drivers of the 3825 are capable of driving 1000 picofarads from one rail to the other in a mere 30 nanoseconds. In fact the peak current avilable is in excess of 1.5 Amps. This kind of brute strength is sufficient for driving a wide range of power mosfet's in a variety of applications.

Some older PWM controllers with totem-pole output stages are plagued with hefty amounts of cross conducted charge during output transitions. This can result in major self heating problems especially at higher clock rates. The 3825 output stage (figure 3a) has been modeled after the successful designs of the UC3846 and UC3842. The differences are in bias values and the addition of Schottky diodes. This circuit guarantees the output transistors, Q1 and Q2, are driven with complementary signals to keep cross conducted charge under control. This approach necessarily involves a compromise since speed is of the utmost concern. Delays could be inserted to guarantee zero cross conducted charge, but that would be contrary to the required propagation delays for high speed operation. The outputs have been adjusted to yield these rise and fall times at a penalty of only 20 nanocoulombs of cross conducted charge per transition. At a clock frequency of 500 kHz, this only adds an additional 10 mA to the supply current.

Rather than dwell on cross conducted charge, which is measured with no load on the outputs, it is more appropriate to examine the performance with typical loads. The most anticipated load is a power mosfet. The impedence presented by the gate of the fet is application dependent, but is primarily capacitive. Therefore, consider the requirements of driving a capacitor with a square wave voltage. The charge required for one cycle is equal to the capacitance times the voltage. The average current taken from the supply is that charge times the switching frequency. This determines the power required from the supply to drive the cap. Since the cap is an energy storage element, all the power

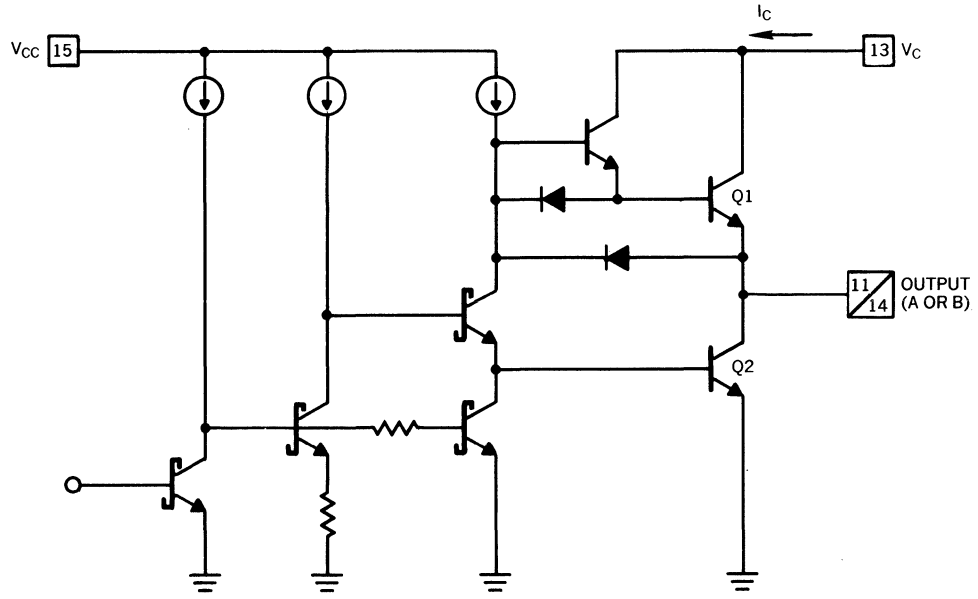
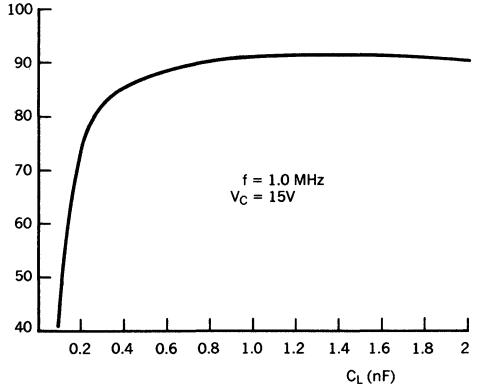


FIGURE 3a. OUTPUT STAGE SIMPLIFIED SCHEMATIC.

taken from the supply is dissipated by the chip. An efficiency figure for the chip can be defined as the ratio of the theoretical power dissipation to the actual power dissipated by the chip. This can be determined for a given frequency and supply voltage by measuring the average supply current into the Vc pin (assuming the peak output voltage is approximately equal to the supply voltage). The figure of efficiency, then, is: (CVf)/Ic. The graph of figure 3b shows the 3825 optimized to drive capacitances above 200pF. Care should always be taken when driving high capacitive loads to make sure the maximum power dissipation level of the chip is not exceeded.

FIGURE 3b

$$\text{EFFICIENCY} = \frac{cvf}{I_C} (\%)$$



Another side effect of the output stage should be considered. Any node in a circuit capable of driving large capacitances at these rates begins quickly to resemble an LC tank. Transmission lines, even one inch in length, can become troublesome. The trouble occurs when, on the falling edge at an output, the load rings and actually pulls the output pin below ground. For years IC manufacturers have been warning users not to allow certain pins to go below ground and the 3825 output pins carry the same warning. The collector of the pull down transistor becomes a parasitic npn emitter when pulled below the chip's substrate, which is grounded (figure 4). The collector, or collectors as the case is, are every other npn collector and pnp base on the chip. The ones that are closer to the parasitic emitter collect proportionally more current than ones further away. Physical size of the parasitic collectors also plays a similar role. The results of this phenomenon can range from nonobservable to severe. Resembling leakage current internally, reference voltages can be altered, oscillator frequency can jitter, or chip temperature can be elevated. Dummy collectors tied to ground are inserted into the 3825 chip which help to attenuate this problem but the designer still needs to be aware of it. The problem's potential is not a horror story, though. Among the easiest of solutions is some form of damping in the load circuit (for example ten ohms series resistance) and a good high speed diode, Schottky if possible, to clamp the output pin's negative going excursion.

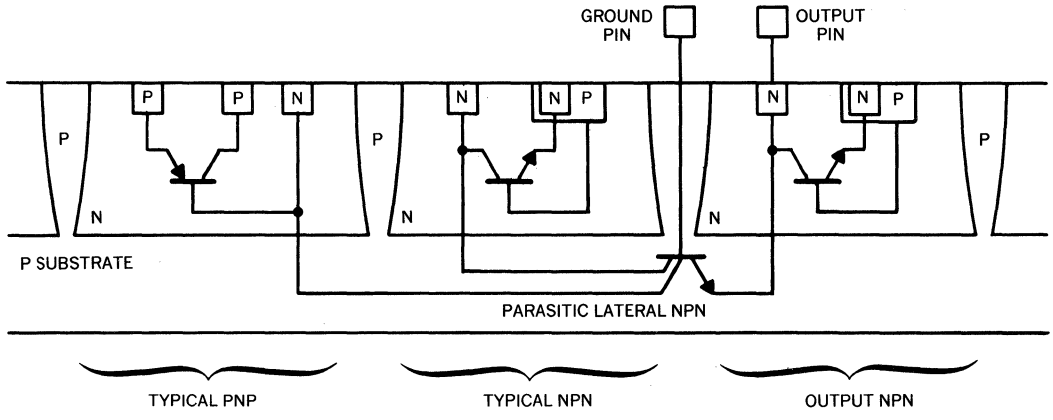


FIGURE 4. PARASITIC NPN TURNS ON WHEN SUBSTRATE – EPI JUNCTION IS FORWARD BIASED.

HIGH SPEED COMPLEMENTARY BLOCKS

An integrated circuit controller with delays of 50ns through its speed critical path is certainly a leading candidate for high frequency switcher applications. There are a few blocks just off the race path that need also to be fast in order to fully qualify the chip for such applications. The oscillator and error amplifier are two such blocks.

Oscillator

From the users point of view, the oscillator looks identical to many that have gone before it (figure 5a). Composed of an all npn comparator, this oscillator has dual thresholds – the upper at 2.8 Volts and the lower at one Volt. Charging current for the timing capacitor, Ct, is mirrored from the timing resistor, Rt. The Rt pin is held at a temperature stable 3 Volts. Temperature stability of the oscillator, then, is achieved by maintaining stable thresholds at the comparator. When Ct has charged to the upper threshold, Q3 turns on to sink a controlled current of approximately 10 mA. The effect of this action is that the discharge of Ct is done in an orderly manner allowing the comparator to reliably catch it when crossing the lower threshold. This also prevents Q3 from saturating, reducing delays in the oscillator and enabling it to operate at higher frequencies. The 3825 oscillator is nominally specified at 400kHz with an initial guaranteed accuracy of 10%. Temperature stability is typically better than 5% while voltage stability (frequency shift over supply voltage) is 0.2%. Oscillator dead time, which effects controller dynamic range, can typically be held to 100ns at 1MHz, allowing 90% duty cycles.

In applications where two 3825's are used in close proximity and synchronization is desired (figure 5b), the oscillator in one chip can be disabled by tying Rt to the reference Voltage. That chip, then, must be clocked by joining the clock pins of both chips. Multiple 3825's also can be synchronized from a master 3825 or other external sync signal. The slave chips are programmed to run at a frequency somewhat lower than the master chip. The master then inserts a sync pulse forcing each slave's Ct over the top threshold and causing discharge action to occur. This way, each chip generates its own clock pulses synchronized to a master clock.

Error Amplifier

The 3825 error amplifier is a voltage gain amp with premium bandwidth and slew rate. Again using only npn's in the signal path, a compensated unity gain bandwidth of 5.5 MHz is achieved. The simplified schematic (figure 6) shows the signal path of the amplifier. Note that while the compensation scheme is not extremely complex or brand new in nature, neither is it the simple dominant pole approach. Included are two zeros located beyond the unity gain frequency to enhance phase margin. One is created by a capacitor across the emitter degeneration resistors in the first stage and the second is formed by a resistor in series with the dominant pole capacitor.

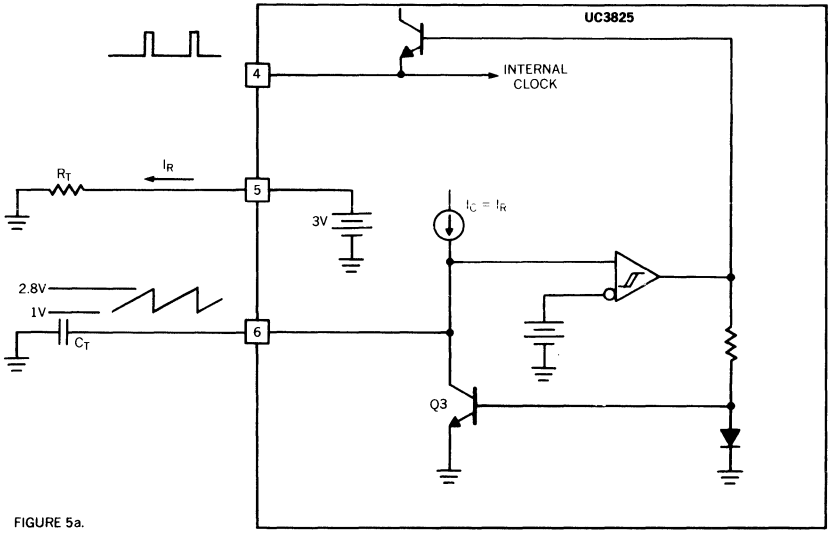


FIGURE 5a.

FIGURE 5b.

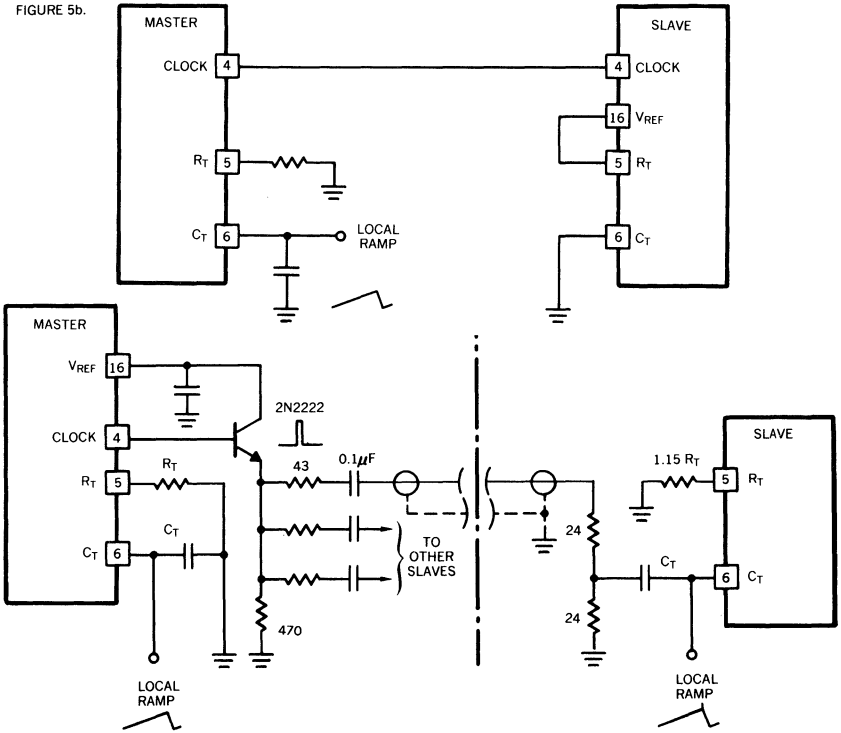


FIGURE 5. OSCILLATOR SIMPLIFIED SCHEMATIC (a) AND TWO SYNCHRONIZATION METHODS (b).

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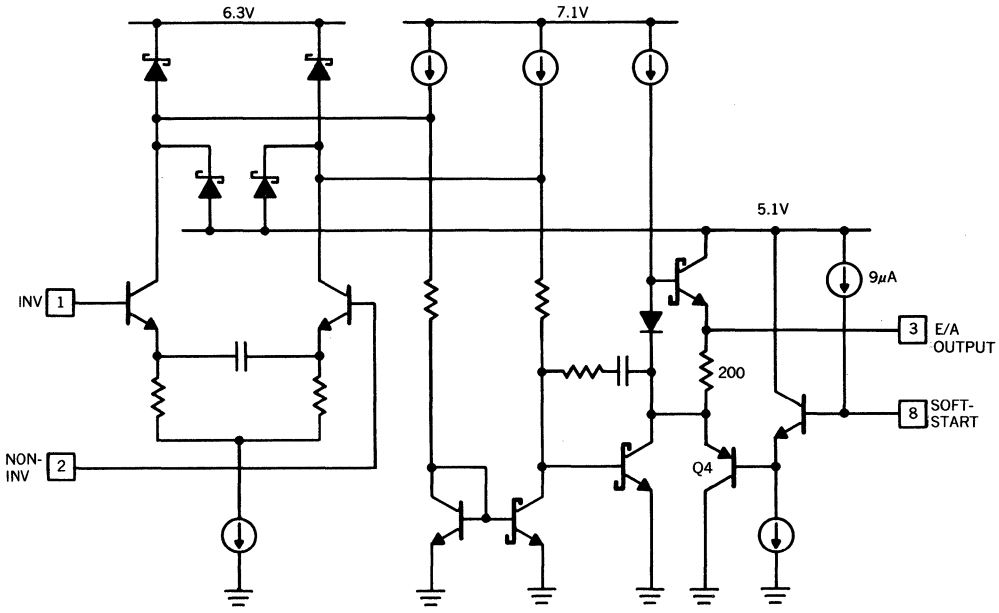

FIGURE 6. SIMPLIFIED SCHEMATIC OF WIDE BAND ERROR AMPLIFIER SHOWING SOFT START CLAMP SCHEME.

By degenerating Gm, the emitter resistors allow an increased first stage bias current level. This contributes to a 12 V/μs typical slew rate. High slew rate, while desirable for good large signal transient response, is not enough to guarantee minimal response time. Often an amplifier may have high slew rates yet exhibit long delay times coming out of saturation when it has been driven to a rail. To defeat this problem, all critical nodes within the amp have been Schottky clamped.

GLUE BLOCKS

The remaining blocks, while not speed critical, mold the 3825 into a more complete PWM controller. The reference, a time proven design, is trimmed to guarantee 5.1 Volts at better than one percent tolerance. This voltage is then held over conditions of line, load, and temperature changes to a two percent total spread.

Soft-start is very simply implemented by a pnp clamp transistor merged into the output stage of the error amp (figure 6). During soft start, while the 9 μA current source is charging the external capacitance on pin 8, Q4 actively forces pin 3 to follow pin 8. In this manner a controlled slow start can be achieved for either voltage or current mode systems. When the error amp comes into regulation, Q4's emitter-base junction is reverse biased and offers no further interference to the normal operation of the amp.

In addition to slow starts, the soft-start pin can be used to other ends. Clamping the maximum voltage this pin is allowed to rise to will then effectively clamp the maximum swing of the error amplifier. In a conventional PWM scheme this results in a duty cycle clamp while in a current mode application, it establishes the maximum peak current level.

Fault conditions are sensed by the 3825 at pin 9 which is shared by the inputs of the current limit comparator and the shut down comparator. When this pin exceeds one Volt, the current limit comparator sets the PWM latch, terminating the output for the remainder of that cycle. As with normal operation, setting the PWM latch causes the toggle flip-flop to switch states. If the pin is further raised to exceed 1.4 Volts, the shut-down comparator forces the soft-start pin to sink a guaranteed minimum of one milliampere rather than sourcing 9 microamperes. Thus the shut down comparator causes the soft start capacitor to be discharged rapidly. After the fault signal is removed the 3825 will then execute a normal soft-start sequence.

One method of combining current-limit and shut-down signals is shown in figure 7. Here, in a current mode control example, a current sense transformer is used to translate switch current to proper voltage analogs for optimal control at both the Ramp and Current-limit sense pins while the shut-down signal is inserted with a resistive summing technique.

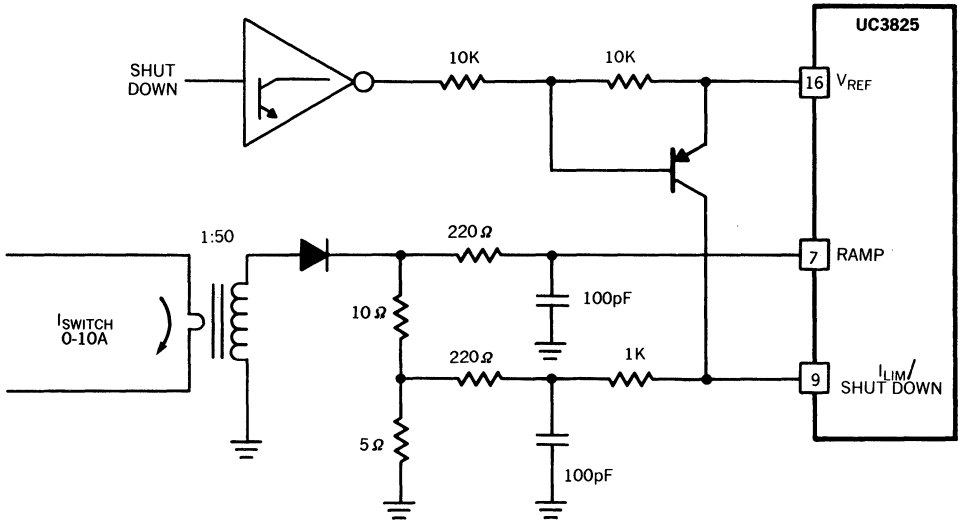

FIGURE 7. CURRENT LIMIT SENSE AND SHUT DOWN SIGNALS ARE COMBINED AT PIN 9 IN THIS CURRENT MODE EXAMPLE.

Starting the 3825 involves the Under-voltage lockout portion of the chip. This block acts like a comparator with it's inverting input biased to 9 Volts and having 0.8 Volts of hysteresis. If Vcc is below the UVLO threshold, the reference generator and the internal bias are turned off, Keeping Icc at a typical 1.1 mA and the outputs in a high impedence state. When Vcc exceeds the UVLO threshold, the reference is turned on and the chip comes alive. Bedlam is avoided, however, as a second comparator monitors the reference voltage and inhibits the outputs until the reference is high enough to ensure intelligent operation. This inhibit signal also holds the soft start pin at a low voltage. After the reference is sufficiently high, the chip begins a soft start sequence.

50 WATT DC-DC PUSH-PULL CONVERTER

A 48 to 5 Volt, 50 Watt converter has been built as a test vehicle for the chip (U-110). Designed around a push pull, current mode controlled topology, the circuit runs from a 1.5 MHz clock. In the interest of simplicity, the ramp input and current limit pins were tied together underutilizing the available dynamic range of the Ramp pin by a factor of 3. A ground plane, judicious bypass capacitors and tight layout technique yielded a circuit that could be easily interrogated without significant noise interference problems.

In this simple application, the 3825 performs all the tasks required to regulate the 50 W power stage. The gate drive for the two power mosfets comes directly from the chip. Current loop slope compensation is resistively summed with the current sense signal at pin 7. Overall loop compensation is implemented with two resistors and a capacitor on the error amplifier. Taking advantage of the 1.5 MHz switching frequency and the wide bandwidth characteristics of the error amp, the control loop was compensated to zero dB at 300kHz.

CONCLUSION

Presenting an easy to use PWM architecture, the UC3825 possesses the necessary high speed characteristics to control switchers in the higher frequency ranges. This fills a void that has hindered high frequency applications in the past. A simple example running at 1.5 MHz points to a future of faster switching supplies.

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USING AN INTEGRATED CONTROLLER IN THE DESIGN OF MAG-AMP OUTPUT REGULATORS

By
Robert A. Mammano, Unitrode IC Corp.
Charles E. Mullett, Mullet Associates, Inc.

Magnetic amplifier technology dates back considerably further than transistors but its wide-spread use has been slow in developing. While many factors may have been responsible for this, at least one — the high cost of tape-wound magnetic cores — has been alleviated with significant recent price reductions and the introduction of less expensive materials. And now, another one — the problems in designing effective control loops utilizing mag amps as voltage regulators — has fallen with the introduction of an IC dedicated to mag amp control — the UC1838.

While there are many types of power supply applications where mag amps may effectively be used, one of the most popular current uses is as a secondary regulator in multiple output power supplies configured as shown in Figure 1. The problem with multiple outputs stems from the fact that the open-loop output impedance of each winding, rectifier, and filter is not zero. Thus, if one assumes that the overall feedback loop holds the output of V_{01} constant, then increasing the loading on V_{01} will cause the other outputs to rise as the primary circuit compensates; similarly; increasing the loading on any of the other outputs will cause that output to droop as the feedback is not sensing those outputs. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated and auxiliary, or secondary regulators are the usual solution. A side benefit of secondary regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratio may not match the ratio of output voltages. Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. Mag amps are a hands down winner in both areas.

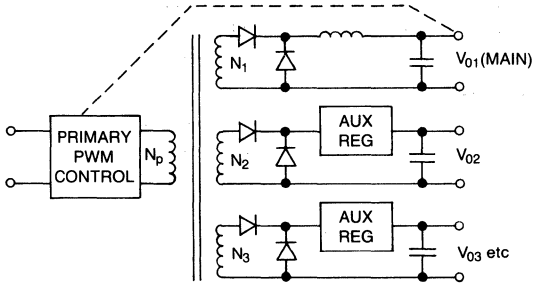


Figure 1. A typical multiple output power supply architecture with overall control from one output.

MAG AMP VOLTAGE REGULATORS

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only subtract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed. As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplied as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

MAG AMP OPERATION

Figure 2 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that N_S is a secondary winding driven from a square wave such that it provides a ±10 volt waveform at v_i. At time t = 0, v_i switches negative. Since the mag amp, L1, had been saturated, it had been delivering +10V to v_3 prior to t = 0 (ignoring diode drops). If we assume v_c = -6V, as defined by the control circuitry, when v_i goes to -10V, the mag amp now has four volts across it and reset current from v_c flows through D1 and the mag amp for the 10 μS that v_i is negative. This net four volts for 10 μS drives the mag amp core out of saturation and resets it by an amount equal to 40V-μS.

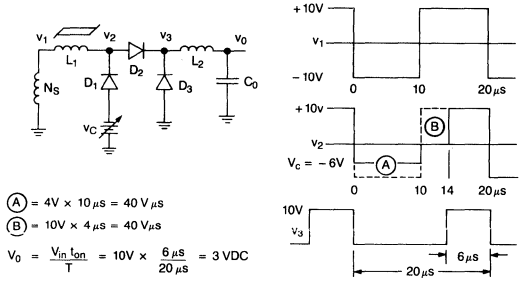


Figure 2. A simplified mag amp regulator and characteristic waveforms.

When t = 10 μS and v_1 switches back to +10V, the mag amp now acts as an inductor and prevents current from flowing, holding v_2 at 0V. This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same 40 volt-μS that was put into the core during reset.

When the core saturates, its impedance drops to zero and v_1 is applied to v_2 delivering an output pulse but with the leading edge delayed by 4 μS.

Figure 3 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

N = mag amp coil turns
Ae = core cross-section area, cm^2
ℓe = core magnetic path length, cm
B = flux density, gauss
H = magnetizing force, oersteads

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I^2R loss — each term very close to zero relative to the output power.

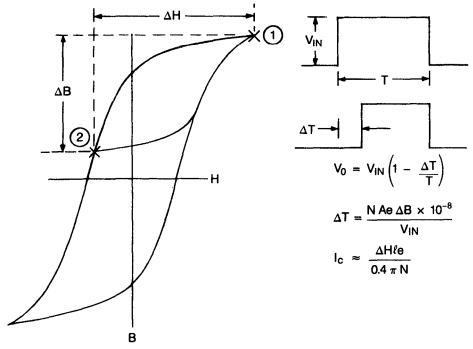


Figure 3. Operating on the B-H curve of the magnetic core.

Figure 4 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

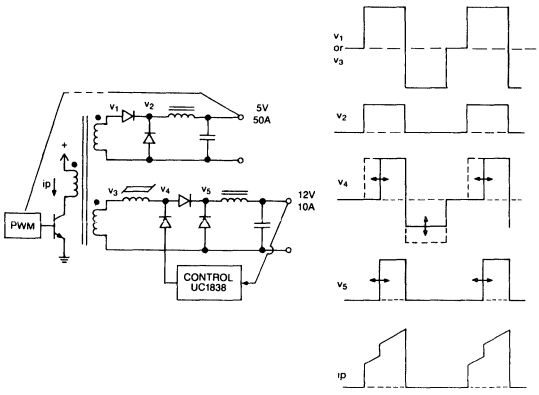


Figure 4. Control waveforms for a typical two-output, secondary regulated, forward converter.

THE UC1838 MAG AMP CONTROLLER

While bringing no major breakthroughs in either integrated circuit or power supply technology, the UC1838 provides a low-cost, easy-to-use, single-chip solution to mag amp control. The block diagrams of this device, as shown in Figure 5, includes three basic functions:

1. An independent, precise, 2.5V reference
2. Two identical, high-gain operational amplifiers
3. A high-voltage PNP reset current driver.

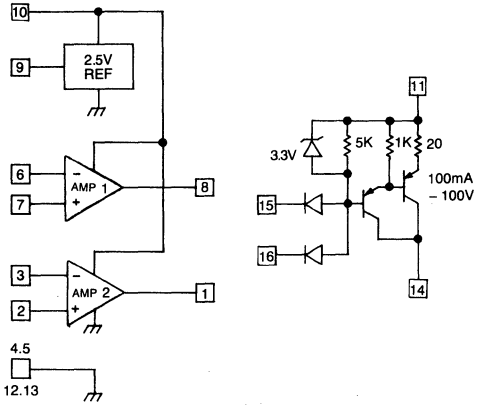


Figure 5. The block diagram of the UC1838 mag-amp control integrated circuit.

The reference is a common band-gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The two op amps are identical with a structure as shown simplified in Figure 6. These amplifiers have PNP inputs for a common mode input range down to slightly below ground and have class A outputs with a 1.5 MA current sink pull down. The open loop voltage gain response, as shown in Figure 7, has a nominal 120 dB of gain at DC with a single pole roll-off to unity at 800 KHz. These amplifiers are unity-gain stable and have a slew rate of 0.3 V/μS.

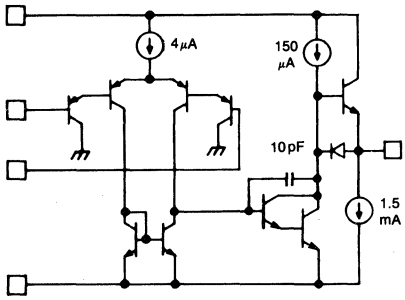


Figure 6. Simplified schematic of each of the operational amplifiers contained within the UC1838.

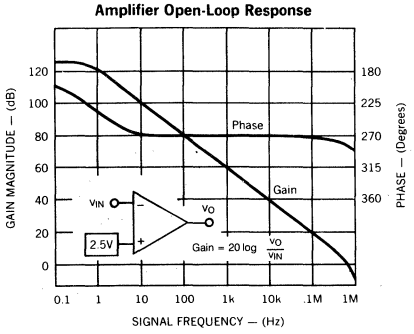


Figure 7. Open-loop gain and phase response for the UC1838 op amps.

Two op amps are included to provide several design options. For example, if one is used to close the voltage feedback loop, the other could be dedicated to some protective function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 MA of reset current with a collector voltage swing of as much as 80 volts negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR" ed to turn on the driver, turning off the supply output.

With internal emitter degeneration, this reset driver operates as a transconductance amplifier providing a reset current as a function of input voltage as shown in Figure 8. The frequency response of this circuit is plotted in Figure 9 showing flat performance out to one megahertz.

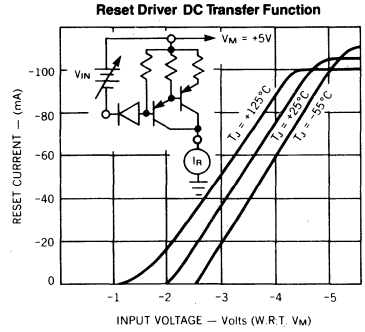


Figure 8. Transconductance characteristics of the UC1838 reset current generator.

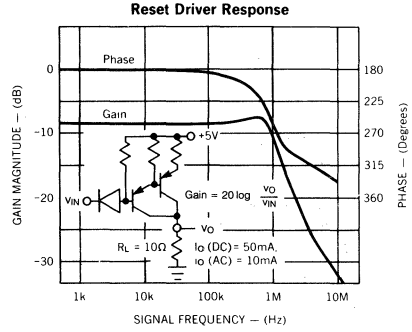


Figure 9. Reset driver frequency response.

Current limiting to protect the output driver is achieved by means of the 3.5 V Zener clamp (which is temperature compensated to match two VBE's) in conjunction with the 20Ω emitter resistor. It should be noted that thermal shutdown is purposely not included since protecting the driver by turning it off would mean losing control of the power supply output. Pin 11 — the emitter of the driver — can be connected to any convenient voltage source from 5VDC to the level used to supply the op amps. Note that the op amp supply must be at least 2 volts higher than the DC level on the inputs, a point to remember when selecting a location for current sensing. One possible configuration for a complete secondary regulator with shutdown control is shown in Figure 10.

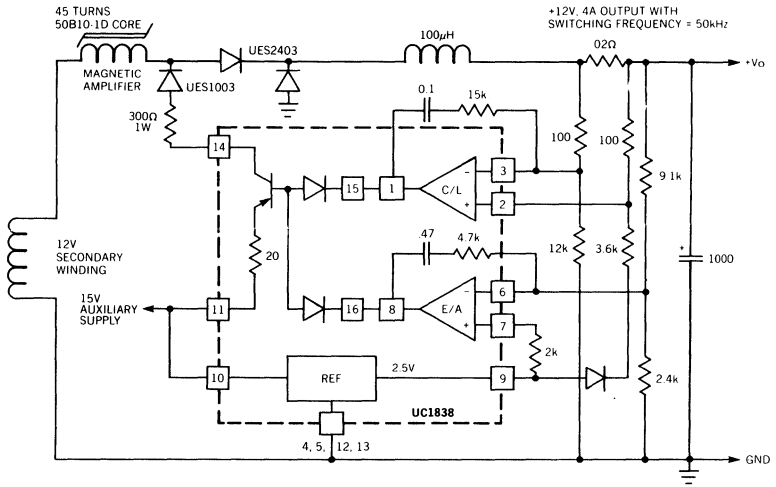


Figure 10. Using the UC1838 to provide both voltage control and over-current shutdown in a typical 12V, 4A regulator.

MAG AMP DESIGN PRINCIPLES

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 11. Some considerations affecting the choices could be:

1. A lower Bmax requires more turns — less important at higher frequencies since fewer turns are required.
2. Higher squareness ratios make better switches
3. Higher I_M requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely

MATERIALS

Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.

Trade Name	Composition	Bmax (kG)	Core Loss @ Bmax	Squareness Ratio	Turns Req'd	I_M (A)
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonol	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.6W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

Figure 11. A comparison of several types of core materials available for mag amp usage.

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the "withstand area," Λ — which the mag amp will be expected to support

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 amp/cm² is a common design rule.
2. Determine core size based upon the area product:

$$AwAe = \frac{Ax \times \Lambda \times 10^8}{\Delta B \times K} \quad \text{where}$$

Aw = Window area, cm²
Ae = Effective core area, cm²
Ax = Wire area, (one conductor) cm²
Λ = Required withstand area, V-sec
ΔB = Flux excursion, gauss
K = Fill factors ≈ 0.1 to 0.3

3. Calculate number of turns from

$$N = \frac{\Lambda \times 10^8}{\Delta B \times Ae}$$

4. Estimate control current from

$$Ic \approx \frac{Hle}{0.4\,\pi\,N} \quad \text{where}$$

l_e = core path length, cm
H is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\Delta T \approx \frac{P \text{ watts}^{0.8}}{A \text{ (surface) cm}^2} \times 444\,^{\circ}C$$

6. Once the mag amp is defined, it can be used in the power supply to verify I_C and to determine the modulator gain so that the control requirements may be determined.

9

COMPENSATING THE MAG AMP CONTROL LOOP

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency.

Figure 12 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

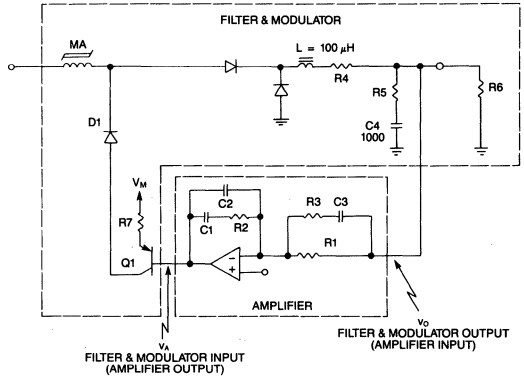


Figure 12. Schematic diagram of a typical regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4) and their parasitic resistances R4 and R5. For this discussion, a 20 KHz, 10 Volt, 10 Amp regulator is used. The output inductor has been chosen to be 100 μH, the capacitor is 1000 μF and each has .01 ohms of parasitic resistance. The load resistor (R6) of 1 ohm is included since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 13 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is $1/(2\pi\sqrt{LC})$, or 316 Hz, and that the magnitude of the response "rolls off" at the slope of -40 dB per decade above the corner frequency. Note also that the phase lag asymptomatically approaches 180 degrees above the corner frequency.

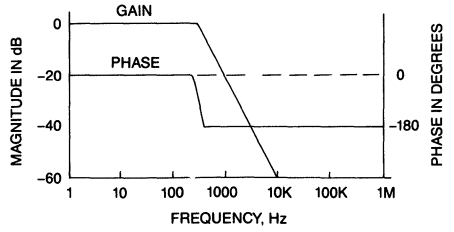


Figure 13. Output filter response.

To include the effects of the mag amp modulator, we must consider the additional phase shift inherent in its transfer function. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the "backswing" of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\varnothing m = -(2D + \alpha)\frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time
α = resetting impedance factor: = 0 for a current source; = 1 when resetting from a low-impedance source; and somewhere in between for an imperfect current source.
ω_S = $2\pi f_S$, where f_S = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 14 illustrates this point. With $\alpha = 0$, we insert no phase delay, and with $\alpha = 1$ we insert maximum phase delay, which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

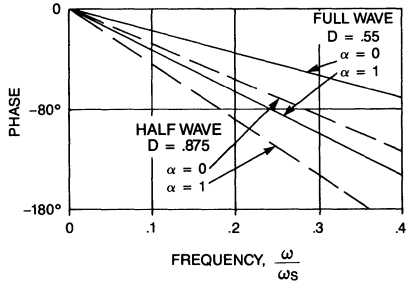


Figure 14. Mag amp phase shift.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the

filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator's phase shift.

Using this technique, the Bode plot for the modulator and output filter of this example has been calculated assuming α = 0.2 and D = 0.6 yielding the graph of Figure 15.

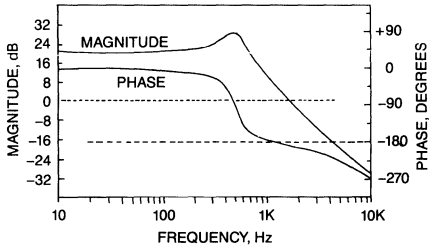


Figure 15. Filter-modulator response including the effects of mag amp phase delay.

If we now close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called "dominant pole" compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 12 allows us to do a much better job, by adding a few inexpensive passive parts. It has the simplified response shown in Figure 16. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.

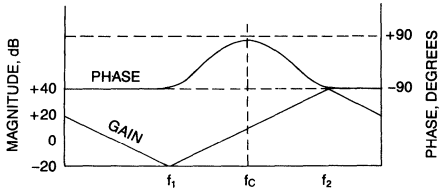


Figure 16. Compensated amplifier frequency and phase response.

The important point is that this circuit provides a phase "bump" — it can have nearly 90° of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies, f1 and f2. This benefit is not free, however. As we ask for more boost (by increasing the separation between f1 and f2) we demand more gain-bandwidth of the amplifier.

DESIGN EXAMPLE

An 8V, 8A Output Derived from a 12V Output — 20 KHz Push-Pull Converter

This example uses the UC1838 to control a full-wave mag amp output regulator, with independent shutdown current limiting. Capsule specifications are as follows:

INPUT: PWM quasi-square wave which, without the magamp, produces 12 Vdc.

OUTPUT: 8.0 Vdc ±1% at load currents from 1 to 8A.

OUTPUT RIPPLE: Less than 50 mV p-p.

TRANSIENT RESPONSE: For load changes of 6 to 8 and 8 to 6A, peak excursion of the output shall be less than ±2% and settle to within 1% of the final value within 500 μS.

OUTPUT PROTECTION: The 8V output shall have independent current limiting, so as not to shut down the 12V output when the 8V output is overloaded or short-circuited. It shall recover from the overload automatically when the overload is removed.

Figure 17 shows the proposed circuit approach. A current transformer has been used to sense the overload, simply to illustrate this approach. A simple series resistor of perhaps .01 or .02 ohms would do as well here, but the current transformer is preferred for high-current outputs.

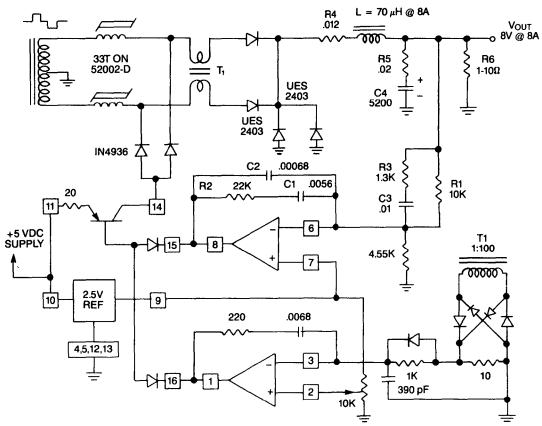


Figure 17. Control and current limiting for a 8V, 8 amp, 20 KHz push-pull converter.

DESIGN APPROACH

With the input waveform already set by the converter design, and the above specifications to define the desired output, the new output circuit will be approached as follows:

1. Draw the preliminary schematic.
2. Design the mag amp.
3. Design the feedback loop.
4. Design the current limiter.
5. Build the breadboard and test it.

PRELIMINARY SCHEMATIC

Figure 17 shows the preliminary circuit diagram. Parasitic resistance of the output filter inductor and capacitor (R4 and R5) are shown, along with the expected feedback com-

pensation elements (R1, R2, R3, C1, C2, and C3). These will be referenced in the mag amp design.

MAG AMP DESIGN

The information necessary to the design is as follows:

1. Input pulse: nominally 32V × 9 μS, = 288 volt-microseconds.
2. Duty ratio of the "off" time: nominally (25 - 9 μS)/ 25 μS = .76, since the frequency at the output is 40 KHz.
3. Output current: 8A.
4. Regulation only, or complete shutdown required? Shutdown.

Comments on the output filter

Design of the output filter is not complicated by the presence of the mag amp. In this case, it was designed with output ripple specs, and capacitor ripple current in mind. Although this design has adequate inductance for continuous conduction of the inductor at minimum load, this is not mandatory. The mag amp, when designed for shutdown, is capable of regulating the output in the discontinuous conduction mode.

Mag amp core selection

1. Wire size: The current waveform in the magamp can be analyzed as follows: During the power pulse, the current is approximately 8A (inaccurate only due to the "tilt" of the top of the current pulse); the duty ratio of this pulse is half the ratio of the output voltage to the pulse height, or .5 × 8/30 = .12. During the dead time between pulses, the inductor current is shared by the rectifier diodes and the "catch" diode. The duty ratio is 1 - 2 × .12 = .76, and the current during this interval is 8/3A. During the remaining interval the current is zero, because the entire 8A is flowing in the other mag amp.

   The rms value of the current can now be computed:

   $Irms = \sqrt{8^2 \times .12 + (8/3)^2 \times .76} = 3.62$ A.

   At 400 Amp/cm², a wire area of approx. .0091 cm² is required. 16 gauge wire has an area of .0131 and is chosen for the mag amp.

2. Core selection: An appropriate material at this frequency is square-loop 80% nickel (Square Permalloy 80 or eq.) with a tape thickness of 1 mil. The saturation flux density if this material is 7000 gauss. A fill factor of 0.2 is chosen for the winding. The required area product is:

   $$AwAe = \frac{Ax \times \Lambda \times 10^8}{\Delta B \times K} = \frac{.0131 \times 288 \times 10^{-6} \times 10^8}{2 \times 7000 \times 0.2} = .135 \text{ cm}^4$$

   which can be divided by 5.07 × 10^{-6} cm²/C.M. in order to refer to core manufacturer's tables.

   An appropriate core is the Magnetics 52002-10, which (with 1 mil tape thickness) has an area product of .026 × 10^6 C.M. cm². The core area of this core is 0.076 cm².

3. Determine the number of turns: The mag amp must be able to withstand the entire area of the input pulse, which is 288 volt-microseconds.

   $$N = \frac{\Lambda \times 10^8}{2 \times Bm \times Ac} = \frac{288 \times 10^{-6} \times 10^8}{2 \times 7000 \times .076} = 27 \text{ turns.}$$

   Allowing an extra 20% for variations in Bm, pulse dimensions, etc., the winding is chosen to be 33 turns.

FEEDBACK LOOP DESIGN

The key steps in the design of the feedback loop are as follows:

1. Determine the modulator's dc transfer function.
2. Plot the transfer function of the modulator and filter, to determine the gain and phase boost required of the feedback amplifier.
3. Design the feedback amplifier.
4. Plot the results in the form of the closed-loop transfer function.

Plotting the modulator's transfer function can be easily done experimentally with the UC1838 by opening the feedback loop at the input to the Reset Driver and driving this point (pin 15 or 16) directly. For interest, the reset current is also measured with the help of a 1 ohm resistor placed in series with the emitter of the reset transistor (pin 11 of the UC1838). The results are shown in Figure 18, with load resistors of 1 ohm and 10 ohms.

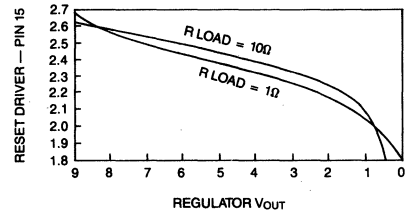


Figure 18. DC gain of the mag amp modulator.

Note that the results are practically the same at both load values. This is to be expected, since the output inductor is still in the continuous conduction mode at the minimum load.

In the region of the desired output (8V and 8A load), the modulator dc gain is approximately 12.5, or 22 dB. In addition to the phase shift of the filter, the modulator contributes additional phase lag! Assuming that we will not attempt to cross unity-gain at a frequency above one-tenth the switching frequency, we can neglect the phase lag due to the impedance of the core and the reset circuit. But we cannot neglect the phase lag resulting from the delay between the time of resetting the core and the time when the core delivers its output:

$$\varnothing_M = 2D \frac{\omega}{\omega_S}, \text{ where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time (.76 in this example)
ω_S = 2 D f_a, where f_a = the switching frequency (40 KHz)

We can use any one of the common circuit analysis programs for analyzing the filter-modulator, neglecting the modulator phase lag when running the program, and then adding it later. Or, the lag may be included in a more sophisticated analysis program. The resultant response prediction is shown in Figure 19.

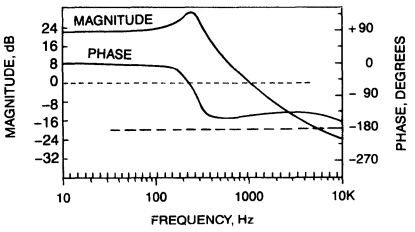


Figure 19. Calculated response plot for the modulator and filter.

Note the shape of the phase response. In the region of 2 KHz the phase lag is decreasing, due to the ESR of the output capacitor. Above 6 KHz the modulator's phase lag becomes important, and the phase lag increases.

Choosing one-tenth the switching frequency for the unity-gain crossover frequency (4 KHz), we can determine the desired gain and phase boost of the feedback amplifier. At 4 KHz, the gain of the modulator is -15 dB (a factor of .179) and the phase shift is -135 degrees. It is generally recommended that there be at least 60 degrees of phase margin at the crossover frequency. This will require reduction of the phase lag to -120 degrees.

In accordance with the design procedure of Venable[2], the required boost is:

Bc = M - P - 90, where

M = desired phase margin, and P = filter & modulator phase shift.

In this case, Bc = 60 - (-135) -90 = 105 degrees. This is comfortably within the theoretical limit of 180 degrees, inherent in the amplifier configuration shown in Figure 17. The gain required at the crossover frequency is the reciprocal of the modulator's gain, or +15dB = a gain of 5.6.

Continuing with the procedure, we can now compute the amplifier components:

$K = (\text{Tan}\ [\ (Bc/4) + 45]\ )^2$	= 8.65
$C2 = 1/(2\ \pi\ f\ G\ R1)$	= .00071 μF
$C1 = C2\ (K - 1)$	= .0055 μF
$R2 = \sqrt{K}/(2\ \pi\ f\ C1)$	= 21,485 ohms
$R3 = R1/(K - 1)$	= 1,302 ohms
$C3 = 1/(2\ \pi\ f\ \sqrt{K}\ R3)$	= .01 μF

where f = crossover frequency in Hz, G = amplifier gain at crossover (expressed as a ratio, not as dB), and K is a factor which describes the required separation of double poles and zeroes to accomplish the desired phase boost. These frequencies are:

$f1 = f/\sqrt{K}$ (double zero), and $f2 = f\sqrt{K}$ (double pole),

In this example, f1 = 1361 Hz and f2 = 11.76 KHz. With this information at hand, it is wise to check the gain-bandwidth required of the feedback amplifier to see that the circuit's needs can be met with one of the amplifers in the UC1838. Knowing that the amplifier rolloff is 20 dB per decade, we can simply calculate the required gain-bandwidth at f2 and see that it is well below the gain-bandwidth of the amplifier.

The gain at f2 is:

$Gf_2 = \sqrt{K}\ G$, and hence the required gain-bandwidth is:

$GBW = \sqrt{K}\ G\ f2 = K\ G\ f$, where G is the desired gain at crossover.

In this example, GBW = 8.65 × 5.6 × 4000 = 194 KHz. This is comfortably below the gain-bandwidth of the amplifier, which is 800 KHz.

For interest, the response of the amplifier is plotted in Figure 20. Note that the gain reaches a minimum at 1.3 KHz, and that the phase boost peaks at 4 KHz, as intended.

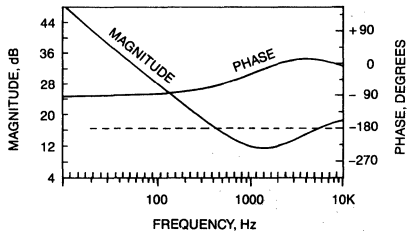


Figure 20. Compensated amplifier response.

Figure 21 shows the overall response, combining the filter-modulator's response with that of the feedback amplifier. Note the 60 degrees of phase margin at the crossover frequency.

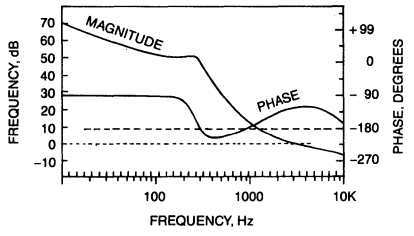


Figure 21. Total loop response with 60 degrees of phase margin at crossover.

CURRENT LIMITER DESIGN

Although a series sensing resistor might have been acceptable at this level of output current, a current transformer, T1 in Figure 17, has been used for the sake of interest. The secondary has 100 turns, and each primary winding is simply one pass through the toroid.

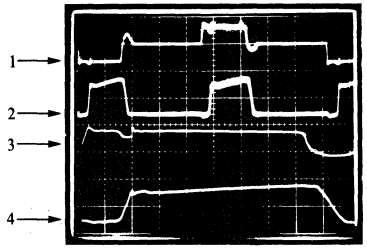
The amplifier performs as an integrator rather than as a comparator, the form found in many primary current limiters of switched-mode controllers. This is not an arbitrary choice. Since the current pulse occurs during the time that the core is obviously not being reset, the circuit must have "memory" — it must apply a shutdown command to the reset transistor during the next reset interval. Although many sophisticated schemes can be devised, the integrator is attractive because of its simplicity.

9

A diode is placed across the input resistor of the integrator, to force its output down quickly when receiving the narrow pulses which occur when the circuit is in current limit. The circuit of this example was developed experimentally. A future goal is to explore this in detail and develop a more rigorous approach. The performance of this circuit is illustrated with waveform photos later in the paper.

BREADBOARD TEST RESULTS

Figure 22 shows the waveform of the input voltage which is applied to the mag amp core, and the current of the two mag amps combined (by placing a current probe on the return leg of the secondary of the converter's transformer). The lower two traces are expanded versions of the top ones, and one can see clearly the effect of the transformer's leakage inductance: the voltage pulse has a "dent" in it during the rise of the current in the mag amp.

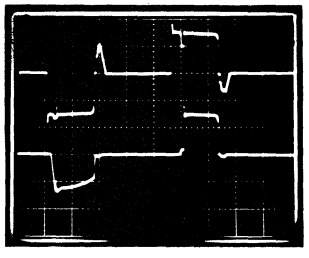


1. Secondary voltage, 50V, 5 μs/div.
2. Current in return (center tap) of secondary. 5A, 5 μs/div.
3. Secondary voltage, 50V, 1 μs/div.
4. Current in return (center tap) of secondary. 5A, 5 μs/div.

Figure 22. Input voltage and current to the mag amp.

Also note the "backswing" at the end of each voltage pulse. This is the discharge of the energy stored in the saturated inductance of the mag amp core. Finally, note the rate of rise of the current pulse, which is determined by the saturated inductance of the mag amp, in series with the leakage inductance of the transformer.

Figure 23 illustrates the operation of the mag amp in more detail. The upper trace is the input voltage of the mag amp, and the lower trace is its output. The reset volt-second product is the difference between the negative pulses of the two traces. The shape of the negative pulse in the lower trace is due to the changing impedance of the mag amp core during reset.

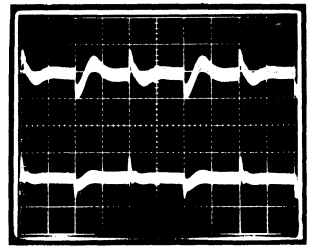


Top: Secondary voltage (into mag amp), 20V × 5 μs/div.
Bot: V_{OUT} of mag amp, 20V × 5 μs/div.

Figure 23. Mag amp operation.

Control loop transient response

To test the response of the regulator to step changes in load, an electronic load was square-wave modulated at 500 Hz, between the values of 6A and 8A. The results are shown in Figure 24. The upper trace is the regulator's output voltage, showing peak excursions of less than 50 mV, and recovery time of .5 ms. The lower trace is the reset current, measured with a current probe at the collector of the reset transistor in the IC.

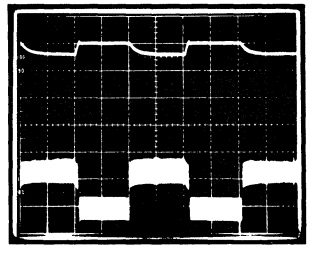


Output transient response 6-8A ΔI_{LOAD}
Top: Output voltage, 50mV × .5 ms/div.
Bot: Reset current, 20mA × .5 ms/div.
(Measured at collector of UC1838 transistor)

Figure 24. Dynamic regulator response to step change in load between 6 and 8 amps.

Response of the current limiter

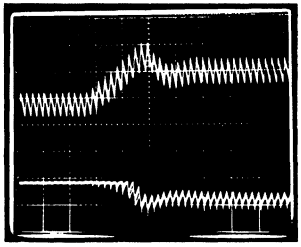
To illustrate the dynamic operation of the limiter, the current limit was set at 7A, and then the electronic load was modulated between 5.7A and 8.7A at a rate of approximately 25 Hz. Figure 25 shows the output voltage in the top trace. The lower trace is the current in the output inductor. Note that the output voltage is well-behaved and that there is no overshoot of the inductor current.



Top: V_{OUT}, 2V × 20 ms/div.
Bot: Inductor current, 2A × 20 ms/div.

Figure 25. Response of current limiter with load switched between 5.7 and 8.5A; with current limit set at 7.5A.

Finally, Figure 26 shows the operation of the current-limiting amplifier. The upper trace is the inductor current, and the lower trace is the output voltage of the current-detecting amplifier. Note the output waveform of the amplifier. Although the amplifier performs as an integrator, it slews fast enough to keep up with the rate of rise of the inductor current, thus adequately protecting the converter and output rectifiers.



Top: Inductor current, 2A × .1 ms/div.
Bot: V_{OUT} of C.L. amp (pin 1), 2V × .1 ms/div.

Figure 26. Response time of current limit amplifier.

APPLICATIONS AT HIGHER SWITCHING FREQUENCIES

As mag amp output regulators are applied at higher and higher switching frequencies, the second-order effects, of course, become more significant.[3] Leakage inductance of the transformer and saturated inductance of the mag amp rob the circuit of its control range, since these produce additional dead time at the leading edge of the output pulse. Even without the mag amp output regulator, this can be a problem in high-frequency switched-mode converters.

Diode storage time has the same result. If the output side of the mag amp "sticks" at ground (during reverse recovery of the rectifier) while its input voltage swings negative, some unwanted reset will be applied to the mag amp. There are techniques to deal with this problem, by providing a shunt recovery path around the mag amp to remove the stored charge in the diode.[4]

The control circuit of the mag amp regulator is not involved in the cycle-by-cycle operation of the circuit; hence, the control IC is not a major barrier to raising the operating frequency. It does affect the situation in an indirect way, however. Its gain-bandwidth may limit the speed of transient response such that the loop crossover frequency cannot be raised in proportion to the switching frequency. In most applications this will not be objectionable. If it is, an outboard op amp can provide the additional gain-bandwidth. If the regulator is not required to have its own current limiter, then the second amplifier can be used in cascade with the first, to provide additional gain-bandwidth.

The integration of the circuit blocks required to implement mag amp output regulators is an important contribution. It is especially beneficial to have the reset transistor included, as this can even eliminate a small heat sink. Finally, it is helpful not only in the design process but also in production to have a single component which encompasses all of the active control functions. As more and more designers are working with the same component, the development of the technology will be more focused, and this will be universally beneficial.

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1. R. D. Middlebrook, "Describing Function Properties of a Magnetic Pulse-Width Modulator," IEEE Power Electronics Specialists Conference, 1972 Record, pp. 21-35.
2. H. Dean Venable, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," Proceedings of the Tenth National Solid-State Power Conversion Conference, Powercon 10 Record, pp. H-1-1 — H-1-12.
3. C. E. Mullett, "Performance of Amorphous Materials in High-Frequency Saturable Reactor Output Regulators," Proceedings of the First International High Frequency Power Conversion Conference, May, 1986, pp. 121-132.
4. C. E. Mullett and R. Hiramatsu, "An Improved Parallel Control Circuit for Saturable Reactor Output Regulators in High-Frequency Switched-Mode Converters," Proceedings of The IEEE Applied Power Electronics Conference and Exposition, April, 1986, pp. 99-106.
5. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, FL in the development of the UC1838.

1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

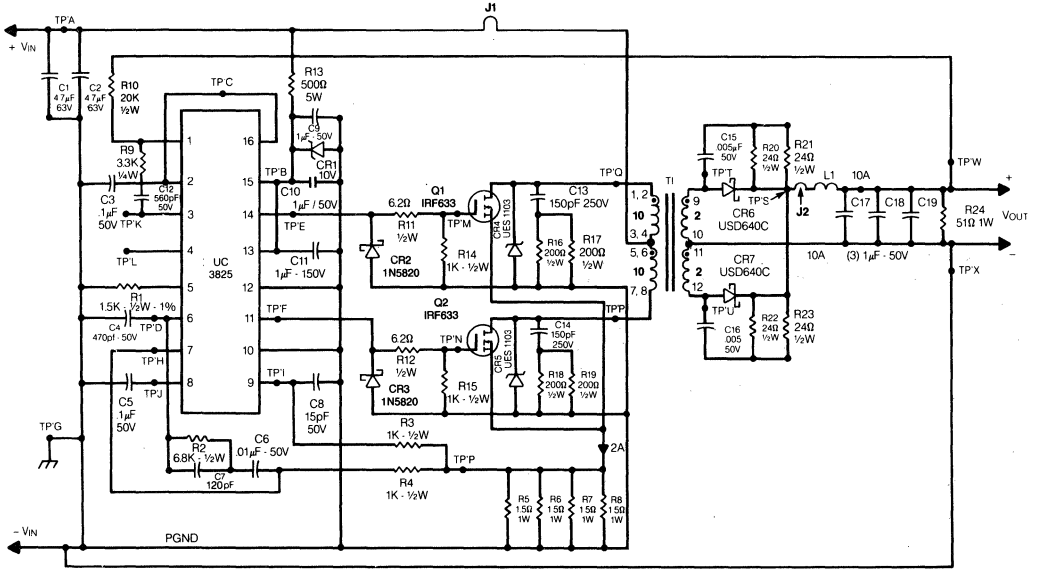
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825. Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.[1]

Figure 1. Schematic Diagram



II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2–10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

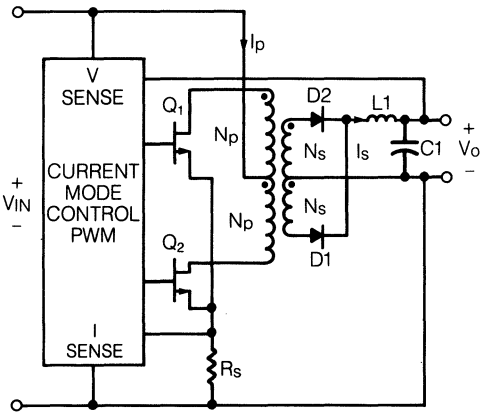


Figure 2. Basic Diagram — Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_s. Simultaneously, diode D1 conducts current I_p x N_p/N_s in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

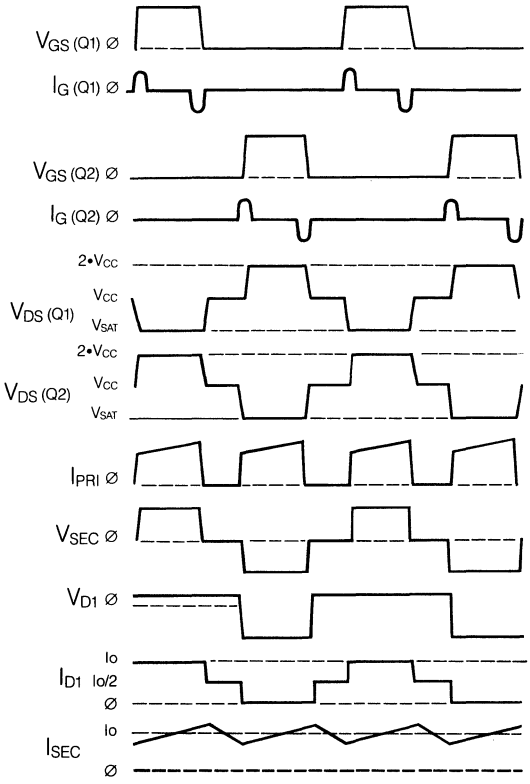


Figure 3. Basic Push-Pull Waveforms

IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{CC} and V_C (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures are used for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} = \frac{68\text{ watts}}{42\text{ volts}} = 1.62\text{ A}$$

The primary current during the transistor on time is:

$$\text{I (p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \leq \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload; V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

P dc = I dc² Rds max • duty
= 2² • 0.8 • 0.85/2 = 1.35 watts

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 –150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) – V xtor (max) – V (Rs) max

V p (min) = 42 v – 2.0 v – 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)

V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \cdot Duty\ (max) \cdot 10^4}{2 \cdot Freq. \cdot N\ (p) \cdot \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared[2] and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \cdot Np = \frac{V\ pri \cdot D\ max \cdot 10^4}{2 \cdot F \cdot \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \cdot 0.85 \cdot 10^4}{2 \cdot 750{,}000 \cdot 10 \cdot 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise[3]

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

$$d\ pen = 7.5 / (frequency^{0.5})\ (cm)$$

At 750 kHz, this corresponds to $8.66 \cdot 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm²

Primary area (Axp) = $1.24A / 450A / cm^2 = 2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$I_{rms(sec)} = \frac{I\,sec^2\,(duty\ on) + \frac{I\,sec^2\,(2 \cdot duty\ off)}{2}}{2}$$

$$I_{rms(sec)} = \frac{10^2\,(.425) + \frac{5^2\,(2 \cdot .075)}{2}}{2}$$

I rms (sec) = 4.81A

Secondary Area (Axs) = $4.81A / 450A / cm^2$
$= 1.07 \cdot 10^{-2}$ cm²

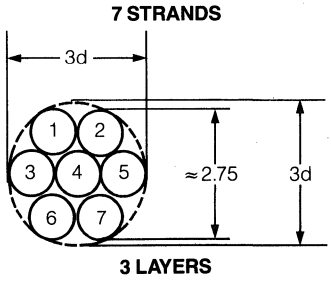


Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\#\text{ conductors}} = \frac{Axp}{7} = \frac{2.75 \cdot 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ cm^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07 \cdot 10^{-2}\ cm}{1.40\ cm} = 7.64 \cdot 10^{-3}\ cm$$

This corresponds to 0.003″ thick foil, a standard value. In practice, slightly thicker foil (0.004″ to 0.005″) may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

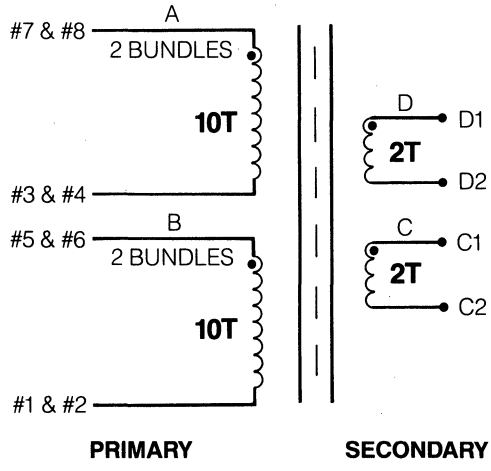


Figure 5. Transformer Schematic

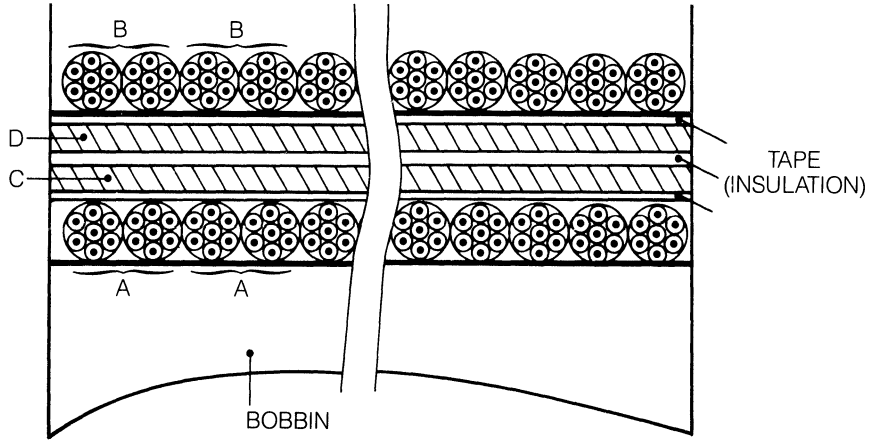


Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of $1.82 \cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$Rpri = \frac{R\ wire \cdot M.L.T. \cdot \#\ turns}{\#\ wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586\ ohm$$

Voltage drop and power loss in each half winding can be also calculated:

$V\ (R\ pri) = Ipri \cdot Rpri = 2.0 \cdot 0.58 = 0.116$ volt (negligible)

$P\ (Rpri) = R\ pri \cdot I\ pri^2 \cdot duty = 0.0586 \cdot 4 \cdot 0.425$
$= 0.0996$ watts

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec $= 1.58 \cdot 10^{-4}$ ohms/cm.

$Rsec = R\ foil \cdot M.L.T. \cdot \#\ turns = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2$
$= 0.00143$ ohm

$V\ (Rsec) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143$ volt (negligible)

$P\ (Rsec) = R\ sec\ (\ (Idc^2 \cdot D\ on) + (\ (Idc/2)^2 \cdot 2 \cdot D\ off)\ )$

$P\ (Rsec) = 0.00143\ (\ (10^2 \cdot 0.425) + (5^2 \cdot 0.15) =$
0.066 watts

Transformer Power Losses

The total copper losses for two windings are then:

$P\ cu = P\ (Rpri) + P\ (Rsec) = 2 \cdot (0.066 + 0.0996)$
$= 0.332$ watts

Estimated eddy current losses are approximately 50% of the copper losses. Pcu ≈ 0.50 watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$P\ core = 3.327 \cdot 0.15 = 0.50$ watt

The total power lost is a summation of the copper and ferrite losses:

$P\ xfmr = P\ cu + P\ core = 0.50 + 0.50 = 1.00$ watts

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\ di}{dt} \therefore L = \frac{V\ dt}{di} = \frac{5.9\ v\ (350)\ 10^{-9}\ s}{3.0\ A} = 690\ nanohenries$$

Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \cdot N^2 \cdot D\ (in),\ N = (L/F \cdot D)^{1/2}\ (turns)$

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690 / 0.0173 \cdot 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns, the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \cdot 10^2 \cdot 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \cdot \frac{T\ period}{2} \cdot \frac{I}{2},\ \text{Delta } Q = I\ p\text{-}p / 8 \cdot F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p / 8 \cdot F \cdot dV = 3 / 8 \cdot 1.5 \cdot 10^6 \cdot 0.10 = 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit / Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section — slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information. Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability[5]

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7), that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

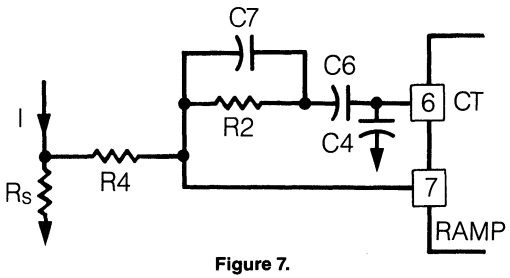


Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

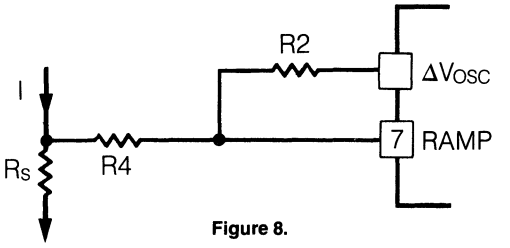


Figure 8.

STEP 1. Calculate Inductor Downslope
S (L) = di/dt = V sec / L = 5.9 V / .740 μH = 8.0 A/μs (1)

STEP 2. Calculate Reflected Downslope to Primary
S(L)' = S(L) / N (turns ratio) = 8.0/5 = 1.6 A/μS (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage
V S(L)' = S(L)' • Rsense = 1.6 • 0.375 = 0.600 V/μs (3)

STEP 4. Calculate Oscillator Slope
V S (osc) = d (V osc) / T on = 1.8 V / 570 ns = 3.15 V/μs (4)

STEP 5. Generate the Ramp Equations
Using superposition, the circuit can be configured as:

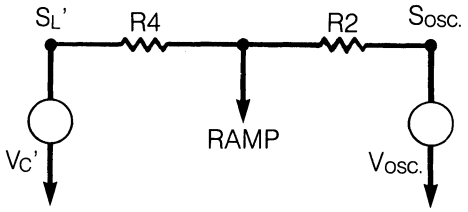


Figure 9.

$$V\,(ramp) = \frac{V\,S\,(L)' \bullet R2}{R2 + R4} = \frac{V\,S\,(osc) \bullet R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,
$$V\,(ramp) = V\,S\,(L)'' + V\,S\,(comp) \quad (6)$$

WHERE
$$V\,S\,(comp) = \frac{V\,S\,(osc) \bullet R4}{R2 + R4}; \quad V\,S\,(L)'' = \frac{V\,S\,(L)' \bullet R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation
$$V\,S\,(comp) = m \bullet S(L)'' \quad (7)$$

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S\,(osc) \bullet R4}{R2 + R4} = \frac{m \bullet V\,S(L)' \bullet R2}{R2 + R4}$$

SOLVING FOR R2:
$$R2 = R4 \bullet \frac{V\,S\,(osc)}{V\,S\,(L)' \bullet m} = R4 \bullet \frac{3.15}{0.600 \bullet 0.75} \quad (9)$$

USING CIRCUIT VALUES,
$$R2 = 7.05 \bullet R4$$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

9

CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency.[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\ \pi\ R\ (load)\ C\ (output)$

$F_z = 1/2\ \pi\ R\ (esr)\ C\ (output)$

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min – 0.300 max

For three capacitors in parallel, ESR = 0.016 – 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

$F_p\ (2A) = 1 / (2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

$F_p\ (10A) = 1 / (2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

$F_z\ (high) = 1 / (2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

$F_z\ (low) = 1 / (2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V\ (output)}{V\ (control)} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V\ (control)} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76 \cdot 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of –16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = 1 / (2 • π • R9 • C12)

therefore, C12 = 1 / (2 • π • R9 • F zero)

C12 = 1 / (2 • 3.14 • 3300 • 100.000) = 480 pF (use 560 pF)

R10 / R9 = approx –16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

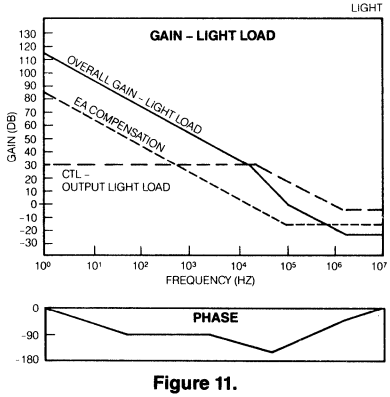


Figure 11.

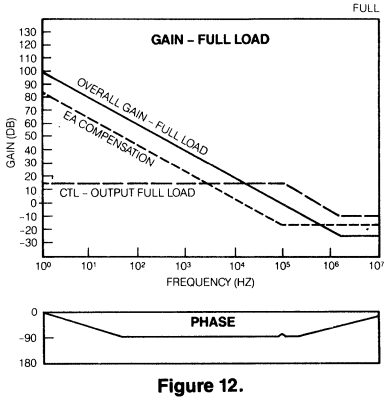


Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13, 14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2, 3	USD1140	40 V, 1 Amp Schottky
CR4, 5	UES1105	150 V, 2.5 Amp Ultrafast
CR6, 7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1, 2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1 K, 1/2 W, 5%	
R5-8	1.5 R, 1 W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5 W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink—Mosfets (AAALL #5786B)	
H2	Heatsink—Diodes (AAALL #5299B)	

Efficiency Measurements

V (In)	I (In)	P (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

V (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg. MV
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses

Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 W
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

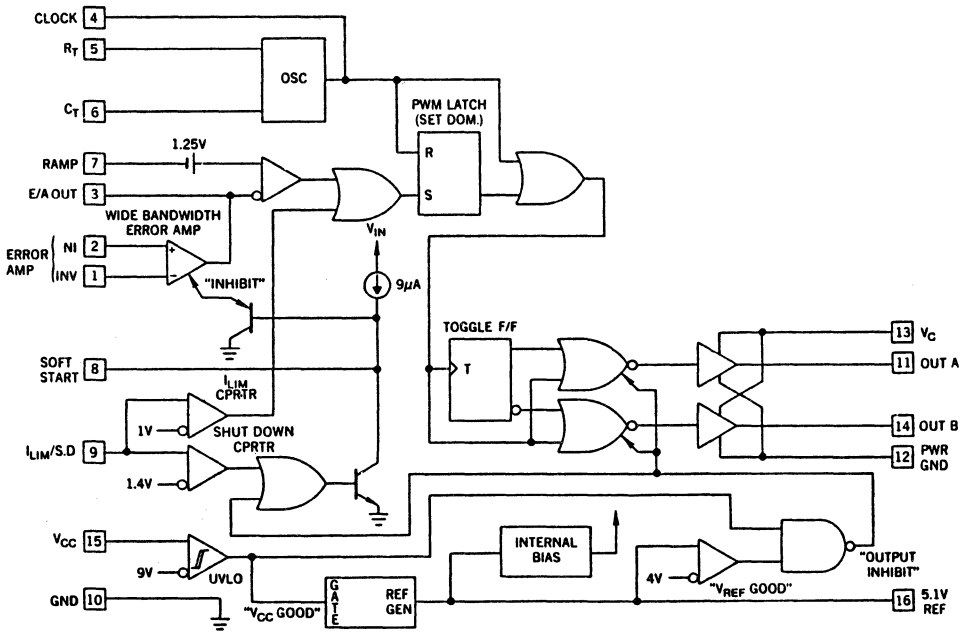
Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

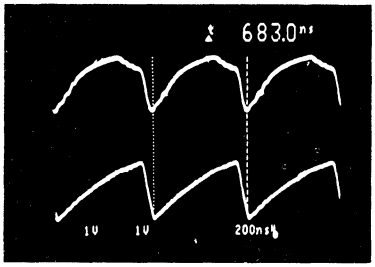
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section C1 — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



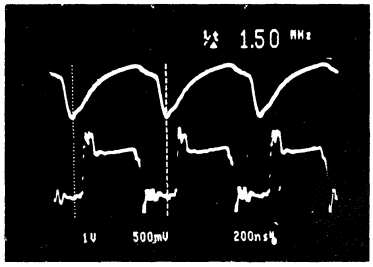
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H', 1 v/cm

Bottom Trace
CT Waveform,
TP 'D', 1 v/cm

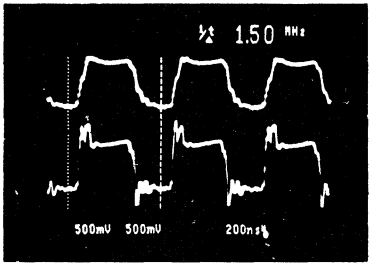
RAMP VOLTAGE



Top Trace
Filtered Ip with
Slope Compensation
TP 'H', 1 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

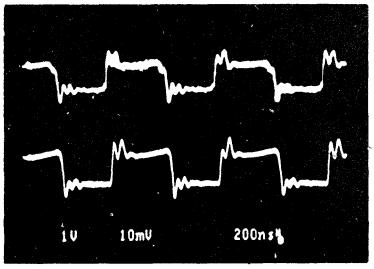
PRIMARY CURRENT



Top Trace
Filtered Ip
TP 'I', .5 v/cm

Bottom Trace
Unfiltered Ip
TP 'P', .5 v/cm

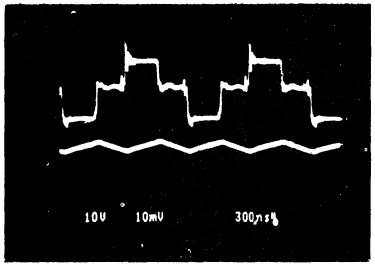
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P', 1 v/cm

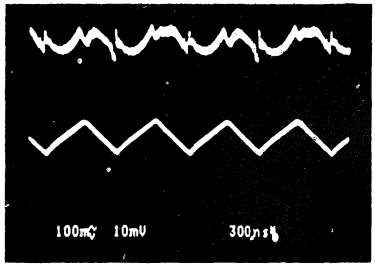
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T', 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W', 100 mv/cm

Bottom Trace
AC Output Current
J2, 2 A/cm

9

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PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant V_{OUT} L_{SEC}.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current I1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

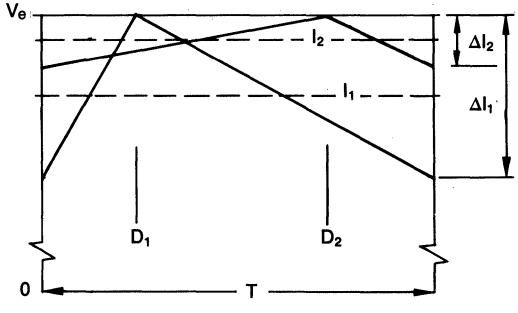

Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

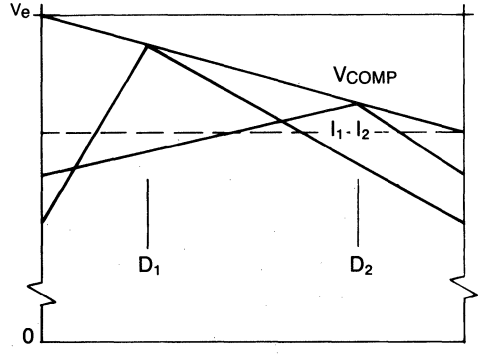

Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator
	ΔV Oscillator (PK-PK Ramp Amplitude)
	I Sense Threshold (Max)
Output	V Secondary (Min)
	L Output
	I AC Secondary (Secondary Ripple Current)
General	R Sense (Current Sensing Resistor)
	M (Amount of Slope Compensation)
	N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

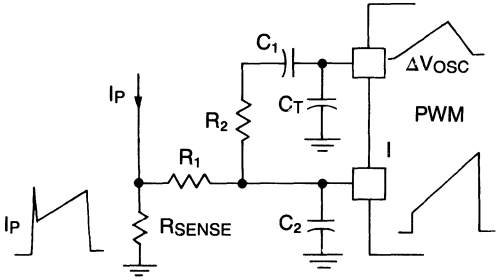

Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

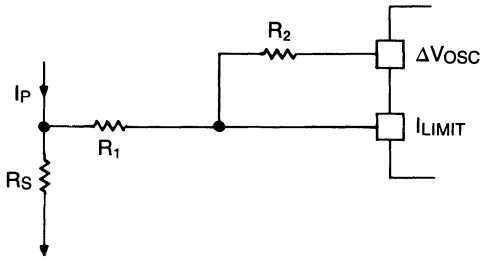

Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d\,(V_{OSC}) / T\ on$ (Volts/Second)

Step 5. Generate the Ramp Equations
Using superposition, the circuit can be illustrated as:

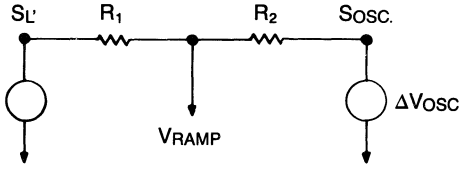

Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$ simplifying,

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)}$$ where

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$, and $$V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation
$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

9

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of down-slope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

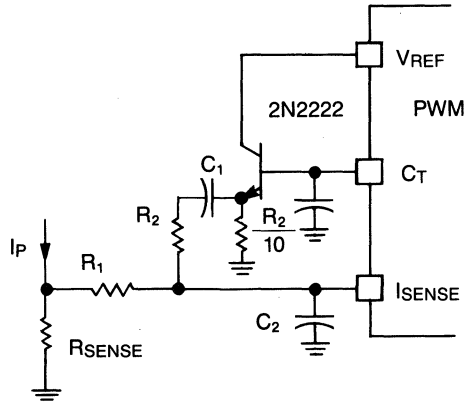

Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 μS
T Deadtime: 500 ns, T on Max = 4.5 μS
Turns Ratio: 15 / 1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<10% I DC)
L Output: 5.16 μh

1. Calculate the Inductor Downslope on the Secondary Side
S (L) = di/dt = V_{SEC}/L_{SEC} = 6 v/5.16 μh = 1.16 A/μs

2. Calculate the Transformed Inductor Slope to the Primary Side
S (L)' = S (L) • Ns/Np = 1.16 • 1/15 = 0.0775 A/μS

3. Calculate the Transformed Slope Voltage at Sense Resistor
V S(L)' = S (L)' • Rsense = 7.72 • 10^{-2} • 0.250 = 1.94•10^{-2} V/μS

4. Calculate the Oscillator Slope at the Timing Capacitor
$S_{(OSC)}$ = d V osc/T on max = 1.8/4.5 = 0.400 V/μS

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M} \quad ; R2 = \frac{1K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

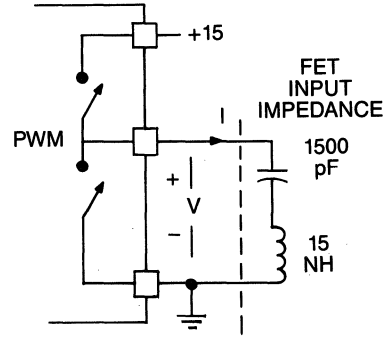

Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

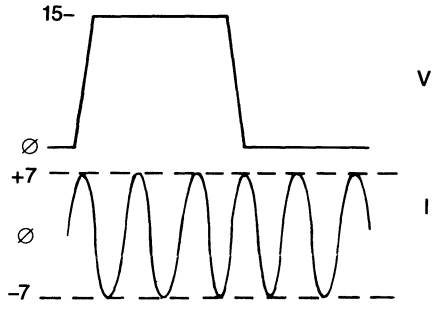

Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (V_C) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

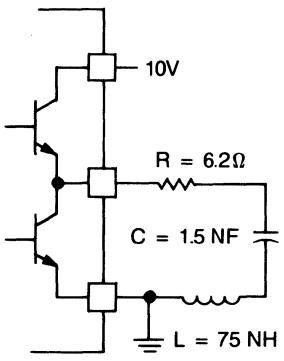

Figure 9. Circuit Parameters

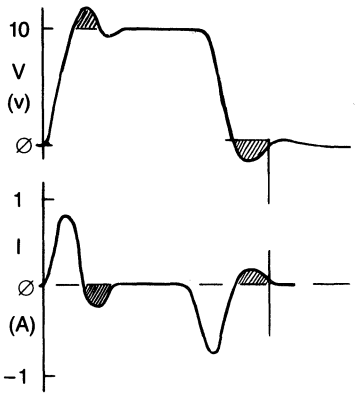

Figure 10. Circuit Response

The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$R\ (gate) \geq 2 \bullet \sqrt{L/C}$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS — highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

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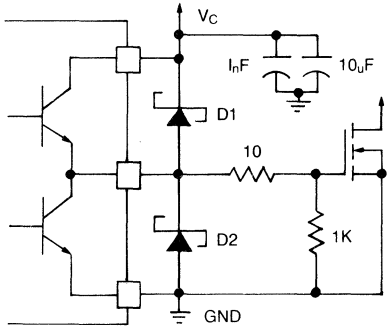
The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure xx when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

Power MOSFET Drive Circuit

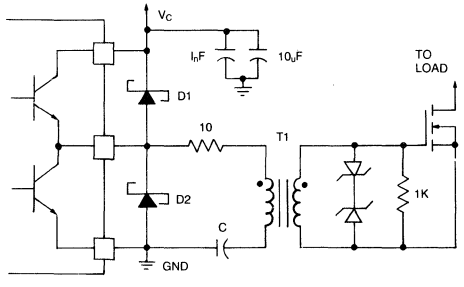


D1.D2: UC3611 Schottky Diodes

Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Figure 12.

inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Transformer Coupled Push-Pull MOSFET Drive Circuit

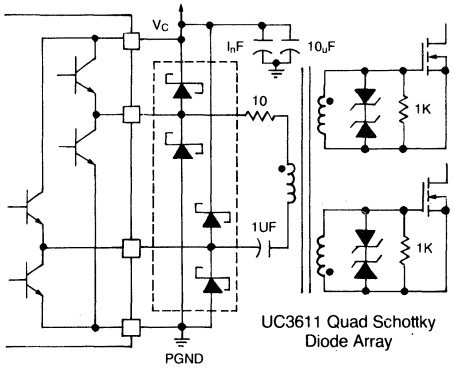


Figure 13.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1.0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET, high speed applications.

SEE APPLICATION NOTE U-118

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resultng in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator. Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

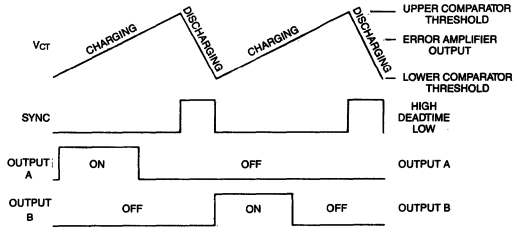


Figure 14. Voltage Mode Control – Normal Operation

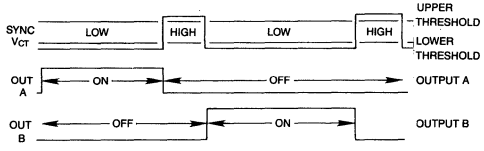


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator. In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

— Sync any PWM to/from any other PWM
— Sync any PWM to/from any number of other PWMs
— Sync from digital levels for simple system integration
— Bidirectional sync signal
— Any PWM can be master or slave with no modifications
— Each control circuit will start and run independently of sync if sync signal is not present
— Localized ramp at Ct for slope compensation
— No critical frequency settings on each module
— High speed — minimum delays
— High noise immunity
— Low power requirements
— Remote off capability
— Minimal effect on frequency, duty cycle, and dead time
— Low cost and component count
— Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

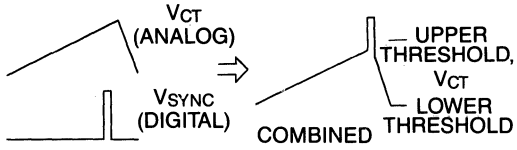


Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor. Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

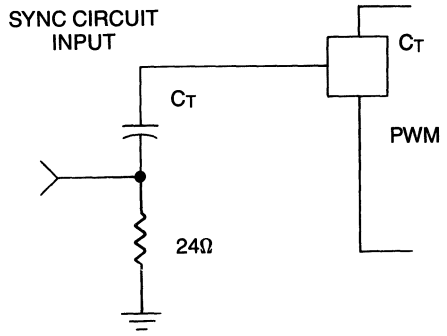


Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail.)

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

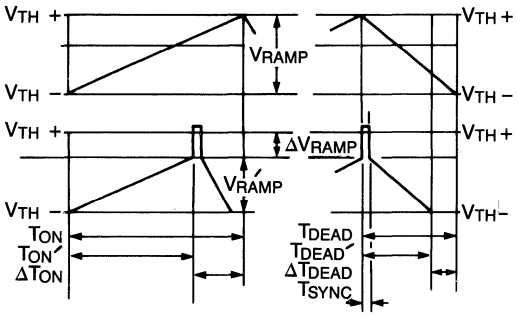


Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\,osc = \frac{1}{Ct}\left[\int I\,chg\,dT = \frac{I\,chg}{Ct}\right]_0^t T$$

$$T\,chg = \{\,\Delta V\,osc \bullet Ct\,\} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\,osc = Vth\ upper - Vth\ lower$$

$$\Delta V\,osc' = \Delta V\,osc\,\frac{(tchg')}{t\,chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\,chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator. Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\,chg'}{T\,chg(o)} = \frac{I\,sync}{T\,orig} = \frac{F\,orig}{F\,sync} = P\ \text{"relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\,chg' = T\,chg(o) \bullet P = 0.85\ T\,chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta[Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\,[Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by $\Delta V\,osc(o) - \Delta Vosc'$, and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\,dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\,dchg' = T\,dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\,dchg(o) \bullet [\Delta V\,dchg' / \Delta Vosc(o)]$$

9

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

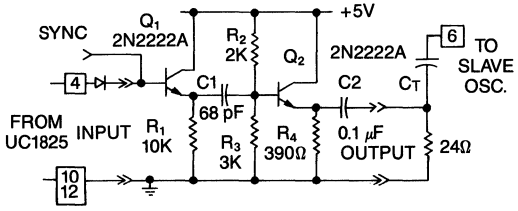
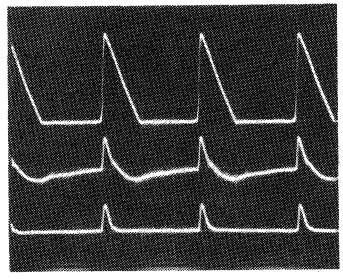


Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor C1, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master. This high speed pulse amplifier circuit adds a minimum of delay (≈50 ns) between the master to slave timing relationship.



Top Trace:
Clock Input

Center Trace:
Base-to-Ground
Voltage at Q2

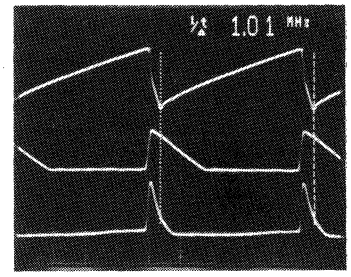
Bottom Trace:
Output Voltage
into 8 ohms

Vertical: 1 Volt/CM

Horizontal:
F OSC = 1 MHz

Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.



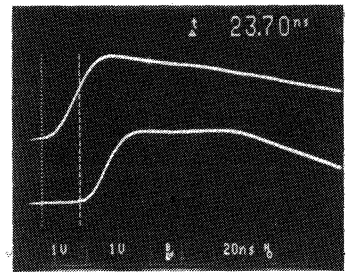
Top Trace:
Master :CT

Center Trace:
Clock Output

Bottom Trace:
V Sync Output

F OSC = 1 MHz

Figure 21. Circuit Timing Waveforms

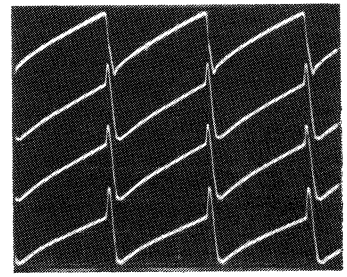


Top Trace:
Master Clock Output

Bottom Trace:
Slave Clock Output

Both: 1 V/CM, 20 ns/CM

Figure 22. Sync Circuit Delay; Input to Output



Trace 1: Master

Trace 2: Slave 1

Trace 3: Slave 2

Trace 4: Slave 3

Vertical: 1 V/CM All

Horizontal:
Fo = 1 MHz

Figure 23. Oscillator Waveforms: Master and Slaves

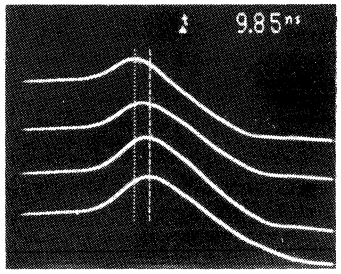


Figure 24. Typical Sync Delay at C_T: Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator. In this instance, the sync pulse forces synchronization at alternate cycles to the master.

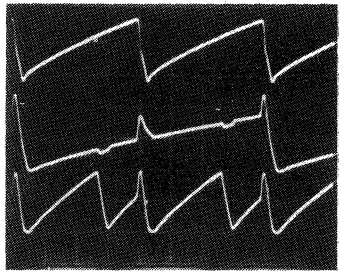


Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

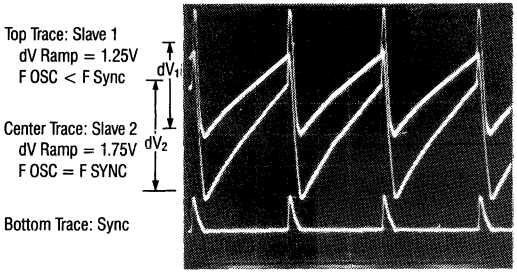


Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

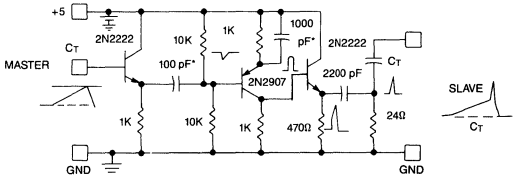


Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

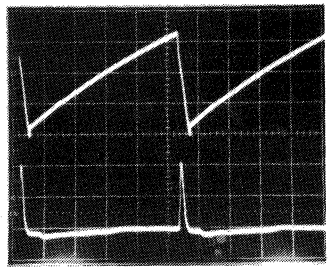


Figure 28. Operating Waveforms at 500 KHz

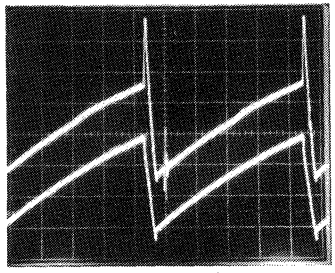


Figure 29. Master/Slave Sync Waveforms at C_T

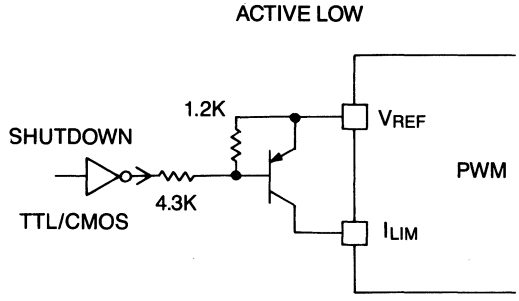
IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

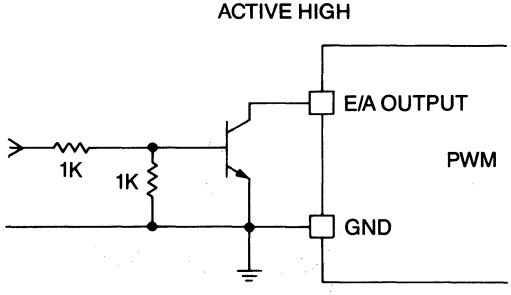
One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.



A. NONLATCHING

Figure 30. PWM Shutdown Circuits

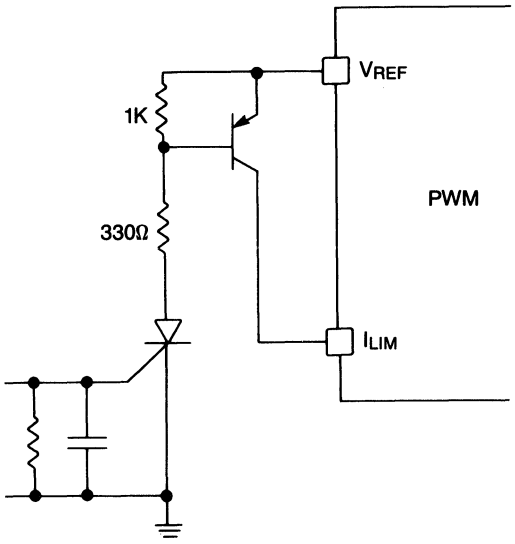


B. NONLATCHING

Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

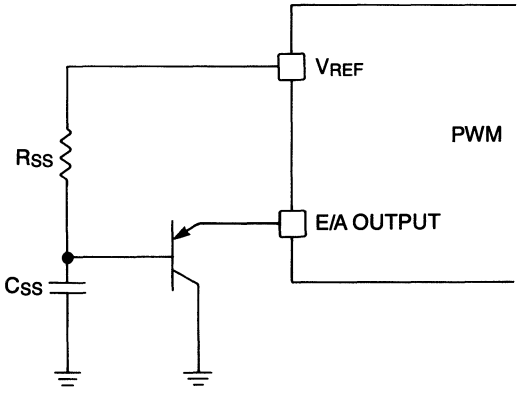


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror. The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

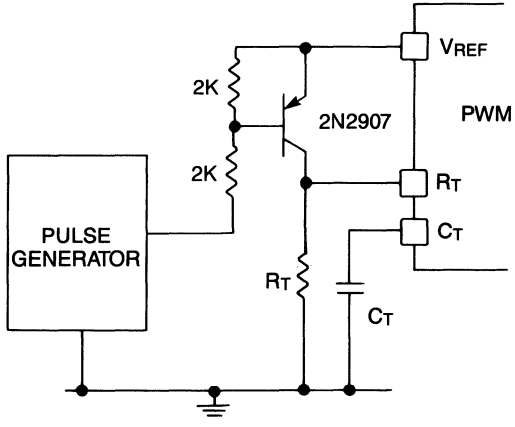
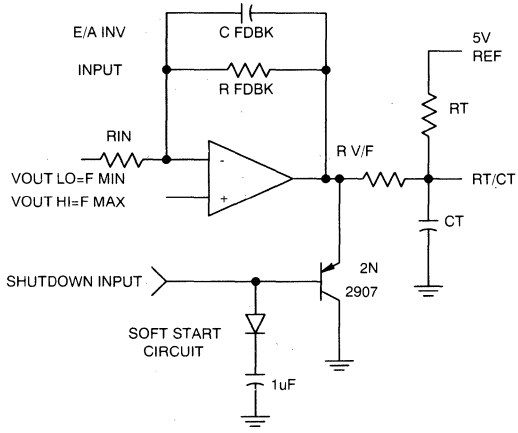


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

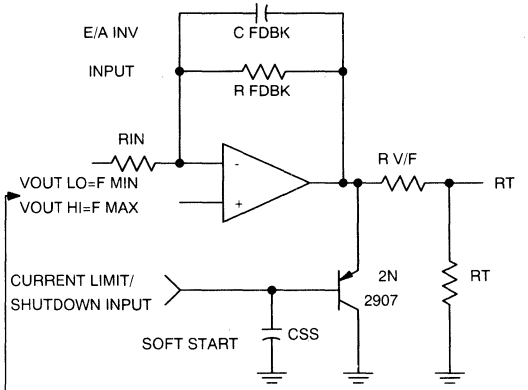
VOLTAGE CONTROLLED OSCILLATOR GENERAL CONFIGURATION

VARIABLE FREQUENCY OPERATION FIXED 50% DUTY CYCLE OSCILLATORS WITH SINGLE PIN PROGRAMMING



UC3851 / UC3844A / UC3845A
*GROUND RAMP OR CURRENT SENSE INPUT

OSCILLATORS WITH SEPARATE RT & CT PINS



UC3823 / UC3825 / UC3846 / UC3847
*GROUND RAMP OR CURRENT SENSE INPUT
USE NONINV E/A INPUT FOR REVERSE V/F OPERATION

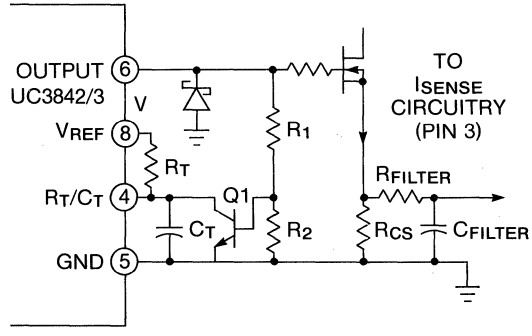
Fixed "Off-Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

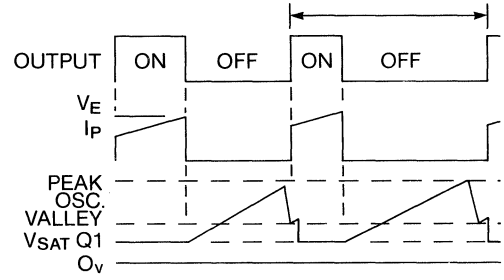
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold. The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

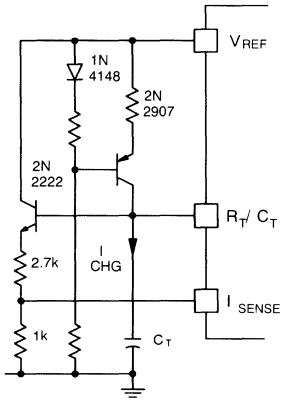


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

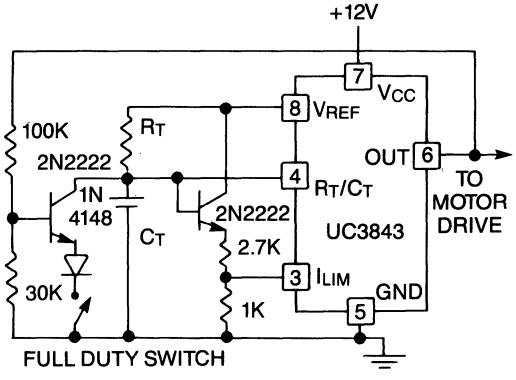


Figure 37. Full Duty Cycle Implementation

VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (<35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

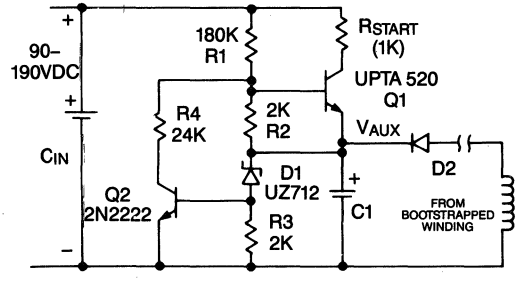


Figure 38. NPN Switches

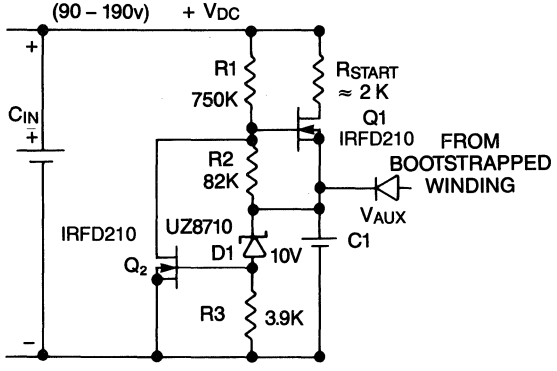


Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor C1 is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to C1 from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and C1 is charged through R start-up from the high voltage DC, as during start-up.

NOTE: SEE DESIGN NOTE DN-26 FOR ADDITIONAL CIRCUITS.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

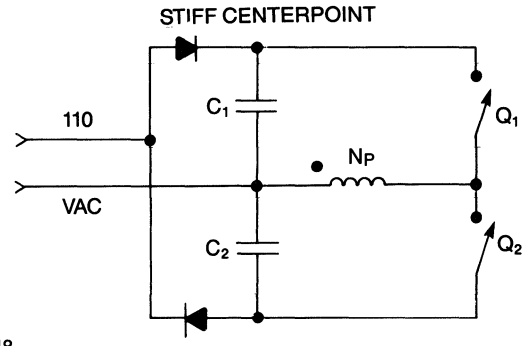


Figure 40.

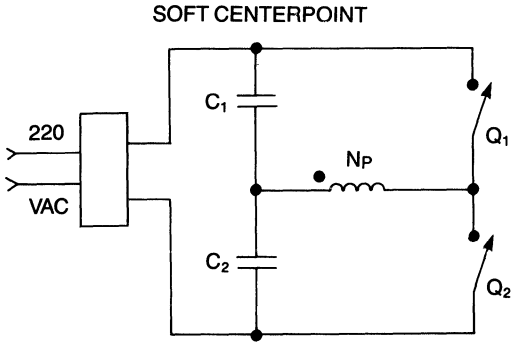


Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

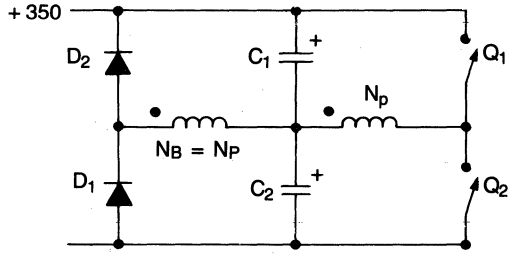


Figure 42. Schematic – Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

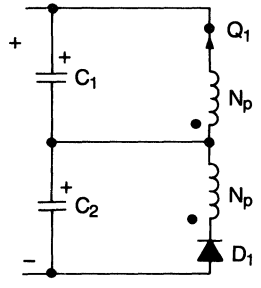


Figure 43. Transistor Q1 On

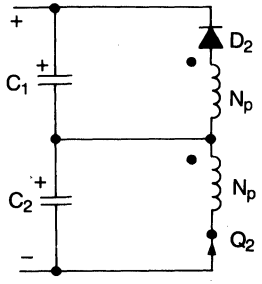


Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

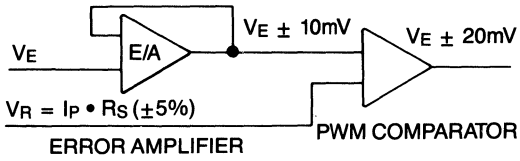


Figure 45. PWM Diagram

In reality, small offets of ±10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ±20 millivolt offset represents a ±2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ±20 millivolts introduces only ±0.5% error to the signal.

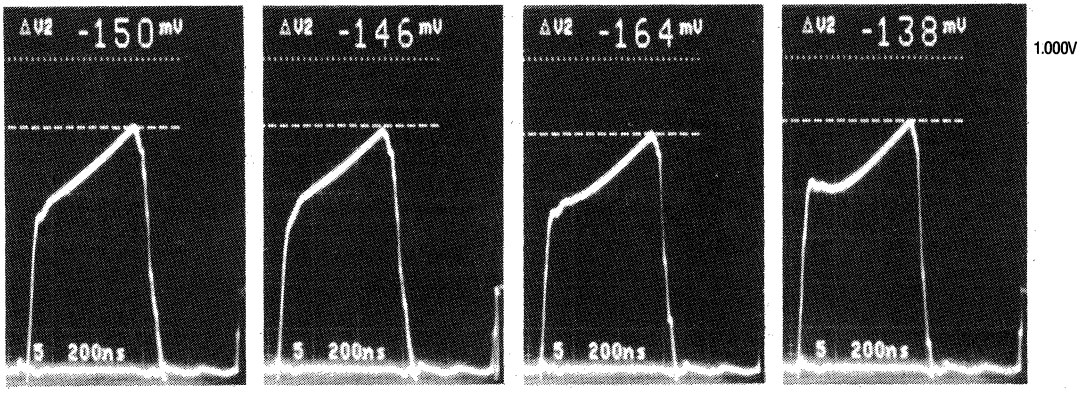
The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ±5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (±2%) / Rs (±5%); therefore Ip' = Ip (±7%) The primary currents (hence output currents) will share within ±seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.



Unit 1 **Unit 2** **Unit 3** **Unit 4**

Figure 46. Primary Currents – Parallel Operation

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor. These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

Top Trace:
V_E: Error Voltage with Noise

Lower Trace:
V_R: Primary Current

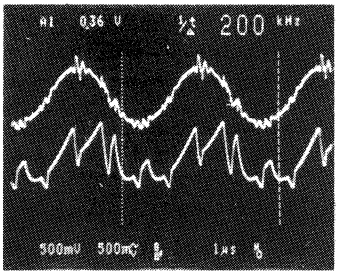


Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter.

Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

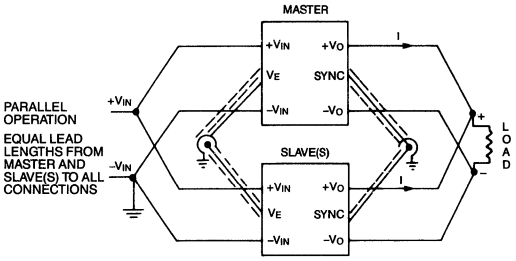


Figure 48.

9

A HIGH PRECISION PWM TRANSCONDUCTANCE AMPLIFIER FOR MICROSTEPPING USING UNITRODE'S UC3637

INTRODUCTION

If you ask a designer why he has chosen a stepping motor for a given application, chances are that his answer will include something about "open loop positioning." Stepping motors can provide accurate positioning without expensive position sensors and feedback loops, and this fact alone results in large savings.

But there is more: steppers are tough and durable, easy to use, and high in power rate. And if you want to close a feedback loop around them, you can do that, too.

Still, there are certain problems. Steppers are *incremental motion* machines, and as such they tend to be noisy and are prone to behave erratically under certain conditions; for example, when the stepping rate is such as to excite a mechnical or electro-mechanical resonant mode. Furthermore, although the angular increments may be small—especially when half-stepping is used—the positioning resolution is restricted to a finite number of discrete points.

Therefore, this question arises: "Is there a method of driving stepping motors such that the resulting movement is smooth and quiet—that is, essentially continuous, as opposed to incremental? And would this result in improved positioning resolution?" We will try to answer these questions here.

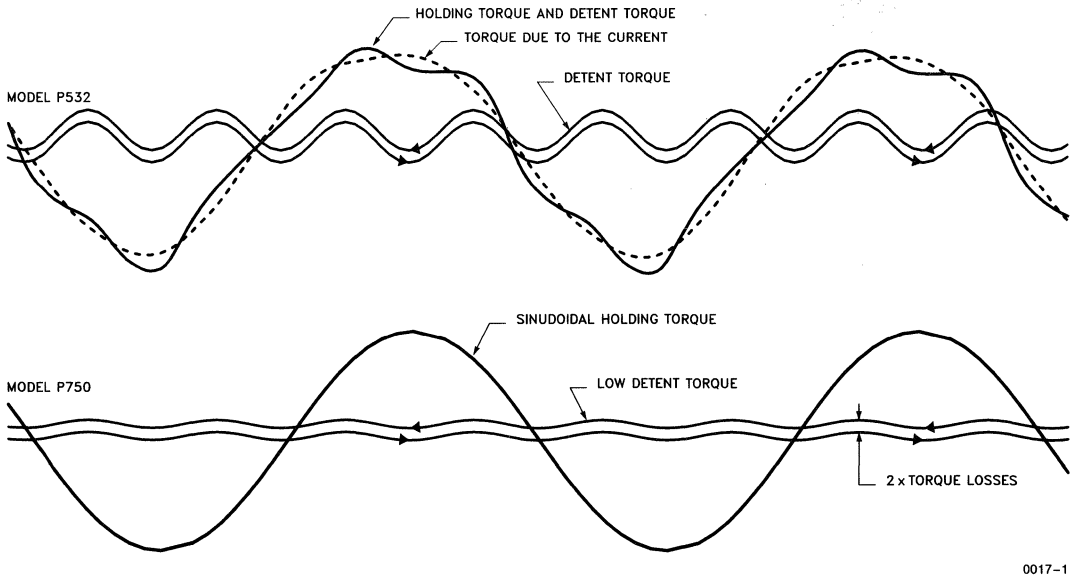


Figure 1. Static Torque Curves of Two Hybird Steppers

STATIC TORQUE CURVES

The curves in Figure 1 illustrate how a stepping motor torque behaves as a function of rotor angle. The detent torque component is a consequence of the magnetic field produced by the rotor magnet (or magnets), and is present with or without phase currents applied. It can be seen that this component contributes a fourth harmonic distortion to the static torque curves. The energized torque curves, in general, have additional harmonic components, mostly the third and fifth. Note that the two motors depicted in Figure 1 have very different characteristics in this respect. The distortion observed in the static torque characteristic is of no great consequence in the more usual applications of stepping motors, using either full step or half step sequences. It is when we start thinking about increasing the positioning resolution of these motors by some method of apportioning currents between the two phases, that we begin to be concerned about the effects of harmonic distortion. Even small amounts of added har-

monics can have a very noticeable effect on the waveshape, as shown in Figure 2.

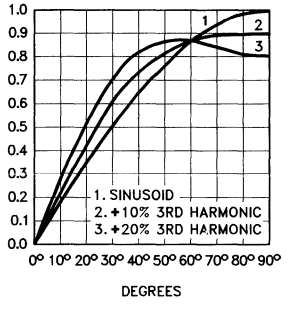


Figure 2. Effect of 10% and 20% Harmonic Content

Figure 3 shows the relationship between sine and cosine waveforms, and what it tells us is that if we can get a motor with a sinusoidal static torque characteristic—i.e., with no harmonic components—and drive phase A with a sine current function and phase B with a cosine current function, we would have smooth shaft rotation and accurate positioning at any angle.

Stepping motors having static torque curves with very low harmonic distortion are commercially available today. But most low-priced, mass produced hybrid steppers exhibit torque curves with enough harmonic components to require careful consideration in any attempt to improve resolution by what is known as *microstepping*. (The name *microstepping* originates from the fact that the required current waveforms are generated by a digital process that aproximates those waveforms incrementally. With thirty-two or sixty-four increments for an electical angle of $\pi/2$ radians, the resulting waveforms are hardly distinguishable from true sine or cosine signals.)

If the nonsinusoidal static characteristic of a given motor is known, it is possible to generate appropriate waveshapes for the phase currents so that the resulting torque curve becomes free of distortion, as required. Note that this involves no additional complexities, since it is just as easy—or difficult—to synthesize one waveform as another. Consequently, one can, in principle, linearize any motor for increased resolution and smoothness through microstepping.

Still, it should be noted that the best efficiency is obtained when the phase current waveshapes are undistorted, because of all suitable waveforms, the sine wave has the lowest form-factor.

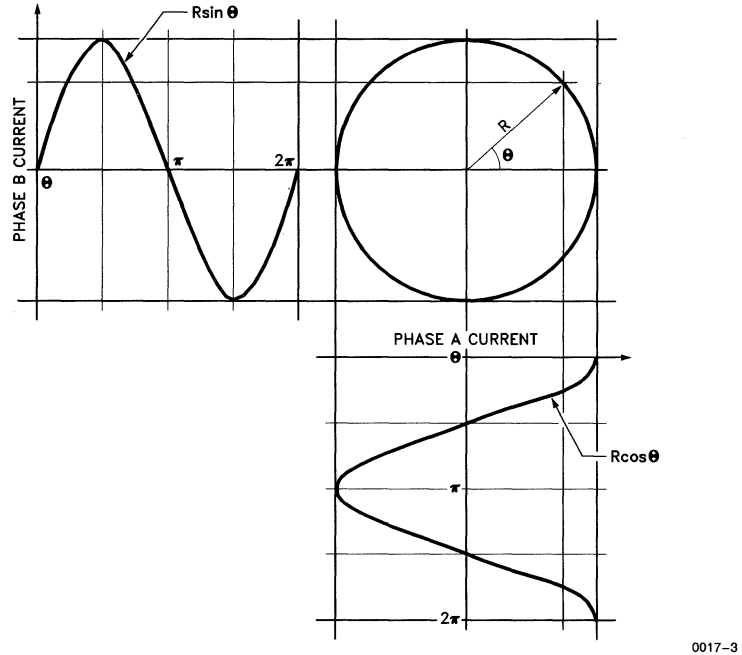


Figure 3. The sum of sine and cosine waveforms is a smoothly rotating vector.

The form-factor of a waveform is the ratio if its rms to average values. For a sine wave, this ratio is:

$$(1)\ ff_S = \frac{0.707}{0.637} = 1.111$$

Some manufacturers have used triangular waveforms—largely because they can be implemented with great simplicity—and it is interesting to note that for such a waveform, the average value is 0.5 V_{PK}, while the rms is 0.577 V_{PK}. Thus the form factor is:

$$(2)\ ff_T = \frac{0.577}{0.5} = 1.155$$

As a consequence, for the same peak power applied to the motor, the rms power of a triangular waveform is 18% less than that of a sine wave, whereas the average current is 21% less. It follows that microstepping with a triangular waveform does not use the full capabilities of the motor.

The same result is obtained with other-waveforms, as long as the peak power is limited, as it must be.

But regardless of all this, the fact remains that whether our motor has a sinusoidal torque curve or a very distorted one, the thing that will be inevitably required will be two amplifiers capable of converting the synthesized waveform into phase currents *at the required power levels*. In the next section, we will describe the design of one such amplifier, having a transconductance linearity of better than 1% and capable of delivering phase currents of up to ±6A.

UNITRODE'S UC3637 PWM CONTROLLER

Pulse width modulation (PWM) is a method of power control whose most attractive feature is the high level of efficiency that can be obtained. With careful design, and using power MOSFETs as output switches, one can easily achieve efficiencies higher than 80%.

The Unitrode UC3637 PWM controller, housed in an eighteen-pin DIL package, was originally intended to serve as a PWM amplifier for brush-type PM servomotors. But, because of its ingenious design, the device has found its way into various other uses as well, such as temperature control, uninterruptible power supplies, and even high fidelity sound reproduction. As we shall see, it can also be used in a high performance PWM transconductance amplifier.

BLOCK DIAGRAM AND LOOP EQUATIONS

A block diagram of the current feedback loop under consideration is shown in Figure 4, where the UC3637 is seen to contain the high-gain error amplifier and the main ingredients of the PWM amplifier. Since we are looking for an output of 6A, an H-bridge power stage must be added. The motor current I_M is sensed by means of a low value resistor R_S, and the derived voltage V_C is used to complete the feedback loop. Not shown in the block diagram is the back-EMF voltage, the product of motor shaft speed and K_V, the motor speed constant. Since this term does not contribute to the dynamics of the current feedback loop, it has purposely been left out.

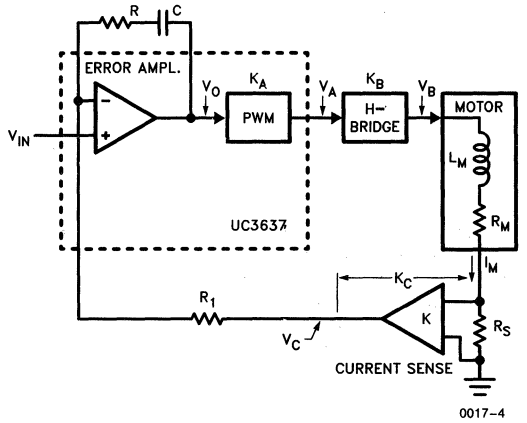


Figure 4. Block Diagram of the Complete Current-Control Loop

The transfer functions of the error amplifier and motor are as follows:

$$(3)\ \frac{V_O}{V_C} = -\frac{1 + sRC}{sR_1C}$$

$$(4)\ \frac{I_M}{V_B} = \frac{1}{R_M(1 + sTm)}$$

where $T_M = L_M/R_M$, the motor's electrical time-constant (R_S is assumed to be low compared with R_M). The forward transfer function is, then:

$$(5)\ G(s) = \frac{-K_A K_B (1 + sRC)}{sR_1R_MC (1 + sTm)}$$

For the feedback transfer functions, we have simply:

$$(6)\ H(s) = \frac{V_C}{I_M} = K_C$$

Thus, for the closed loop,

$$(7)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B (1 + sRC)}{K_AK_BK_C(1 + sRC) + sR_1R_MC (1 + sTm)}$$

If we make the time-constant RC equal to the motor's time-constant T_M, this becomes:

$$(8)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B}{K_A K_B K_C + sR_1 R_M C}$$

$$(9)\ \frac{I_M}{V_{IN}} = \frac{1}{K_C(1 + sT_1)}$$

where,

$$(10)\ T_1 = \frac{R_1 R_M C}{K_A K_B K_C} = \frac{R_1 L_M}{K_A K_B K_C R}$$

By making $RC = T_M$, we have eliminated one of the transfer function poles. The resulting closed-loop response, described by (7) has a gain of $1/K_C$ from $\omega = 0$ to $\omega = 1/T_1$, and drops at -6 bd/octave thereafter.

DESIGNING THE HARDWARE

In designing circuits intended to handle power, it is customary to start with the output stage. This is surely due to the fact that the power stage is more demanding of the designer's attention and care, whereas the low level circuits are far more adaptable to the requirements of the chosen output configuration.

In the present case, power MOSFETs were chosen for the H-bridge because of their low losses, and because of their compatibility with the UC3637 outputs. Each totem-pole leg of the bridge is made up of one N-channel and one P-channel device. Such a pair can be driven in many different ways, of which several were considered for this particular design. The method that was finally chosen, shown in Figure 5, requires a few comments.

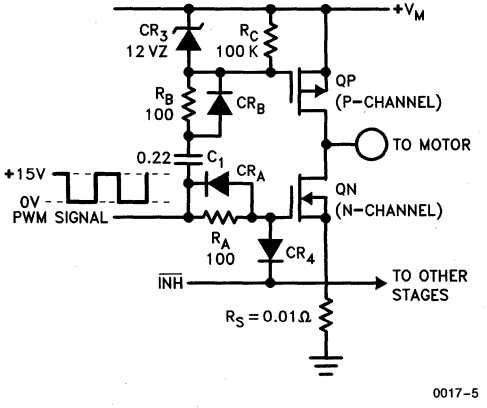


Figure 5. Totem-Pole Leg of Output H-Bridge

The first thing to notice is that the upper MOSFET, transistor QP, has its gate driven through a capacitor, C_1. This is not always practical of course, but in the case of a chopper drive combined with a stepping motor, it turns out that a driving signal is always present. At stand-still and at low speeds, it is the chopping rate that appears; at higher speeds, it is the stepping rate itself, or both. The driver is never required to deliver continuous DC (unchopped) to the motor winding, as it would to the armature of a brush-type DC motor at full speed. Consequently, QP never needs to be held in the ON state for more than a few microseconds, and for this the time constant of C1 R4 is adequate. Also, resistor R_A in parallel with CR_1, together with the gate capacitance of QN, cause this transistor to turn off faster than it turns ON. Since the same thing is done for QP, the problem of cross-conduction is neatly taken care of. The Zener diode CR3 serves as a clamp for the QP gate voltage. Finally, an inhibiting line, INH, is provided as a protection for QP and QN during the power turn-on time, when the $+V_M$ voltage is rising and C1 must be charged. An auxiliary circuit senses a positive dV_M/dt and holds the INH line low, thus keeping QN OFF during this time.

An important point in favor of this arrangement is that the gate-drive circuit losses are independent of V_M and so this voltage can be set anywhere within the Vds rating of the power MOSFETs.

We can now consider the H-bridge with its motor winding load, as shown in Figure 6. The bridge is shown schematically with its driving circuits, but the action is still as shown in Figure 5. For example, when V_{IN} is high, switch S1 is OFF and S3 is ON, and so forth. Furthermore, the opposite side of the bridge is driven by the complementary signal V_{IN}. With V_{IN} low, S1 and S4 will be conducting, and the load current I_M will increase in the positive direction (indicated by the $+I_M$ arrow). Similarly, when V_{IN} is high, both S2 and S3 conduct, causing I_M to increase in the negative direction. Remember that the load is inductive, and that inductance is an energy storing element. Therefore, if we have some positive I_M, due to S1 and S4 being closed, and we switch to S2 and S3 closed, the previous value of I_M will continue to flow "uphill," so to speak, while decreasing. At the time of switching, this current ceases to flow down through sense resistor R_{S4} to ground and starts flowing up through R_{S3} and back to the supply.

Switches S1 through S4 are able to conduct in either direction when in the ON state—a very neat feature of power MOSFETs. Furthermore, their intrinsic diode protects the devices from reverse voltage pulses during the switching no-overlap transition. Since we wish to control this current very closely in both magnitude and direction, it is

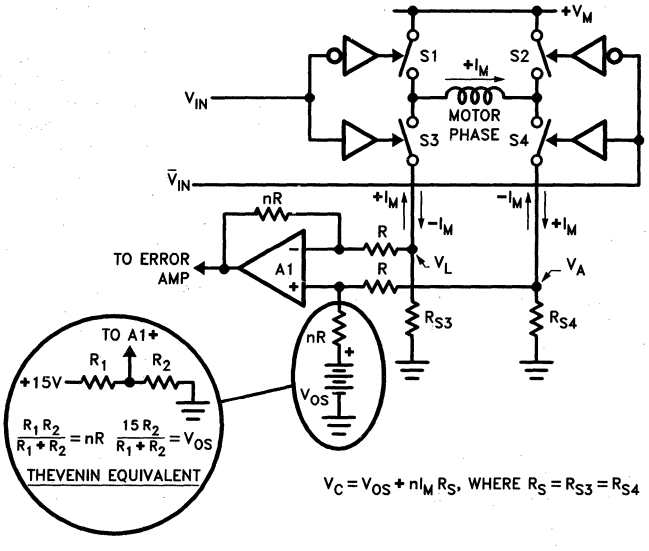


Figure 6. H-Bridge Configuration with Bidirectional Current Sensing

now necessary to generate a voltage V_C that gives an accurate indication of the current I_M over the full range from maximum positive to maximum negative. This is done by the circuit section of Figure 6 which includes the op-amp A1.

In that circuit, the voltage V_{OS} is meant to offset the output V_C of A1 to some chosen value that will correspond to $I_M = 0$. The value of V_C can be written as:

(11) $V_C = V_{CS} + nI_MR_S$

This offset is necessary when the design requires a single polarity supply, as in our case. When two supply polarities are available for the control circuit, one can simply make $V_{OS} = 0$. For the single supply case, the nR and V_{OS} combination is implemented by a simple resistor divider from $\pm V_{CC}$ to ground (a Thevenin equivalent) of the required impedance and open voltage.

To keep the circuit losses to a minimum, we should use low values for the sense resistors R_{S3} and R_{S4}. Yet, they need to be accurate and temperature-stable. In our case, having decided on a V_C scale of 0.5V per motor ampere, we have selected $R_S = 0.1\Omega$ and a current sense amplifier gain $n = 5$. We have also set $V_{OS} = V_{CC}/2 = 7.5V$, so that we will have $V_C = 7.5 + 0.5\ I_M$. This means that as the current I_M varies from +6A to −6A, the analog voltage V_C will vary from +10.5V to +4.5V. At $I_M = 0$, V_C will be equal to 7.5V.

SETTING UP THE PWM CONTROLLER

Having designed the power output stage (H-bridge) and the current-sense circuit, we can proceed to the PWM controller (UC3637) and its external components. The device itself has been described in great detail in its data sheet and in an application note (Publication U-102, available from Unitrode Integrated Circuits Corporation).

In the present design, we use the UC3637 to generate the two H-bridge driving signals V_{IN} and $\overline{V_{IN}}$, at the device's output pins 7 and 4, respectively.

Figure 7 shows in block form the internal workings of the device. Since operation from a single +15V supply is desired, pin 5 will be GROUND and pin 6 will be +15V. We selected, for the ramp oscillator, a waveform as shown in Figure 8, which fits well in the +15V headroom given by our V_{CC} supply. The formulas given in Figure 8 show how the various components are calculated.

Next, we set up the two PWM comparators by tying the inverting inputs (pin 10) of the A comparator, and the noninverting input (pin 8) of the B comparator together and apply the ramp (pin 2) to this line. The remaining comparator inputs (pins 9 and 11) are next connected together to become the PWM input point. It can be seen from the block diagram of Figure 7 that as the control voltage applied to this point varies from +5V to +10V, the duty cycle of the output at pins 4 and 7 also varies. V_4 and V_7 are complementary signals; and the voltage swing of each of these signals is from a low value between 0V and +2V, and a high value between (V_{CC} −2V) and V_{CC}.

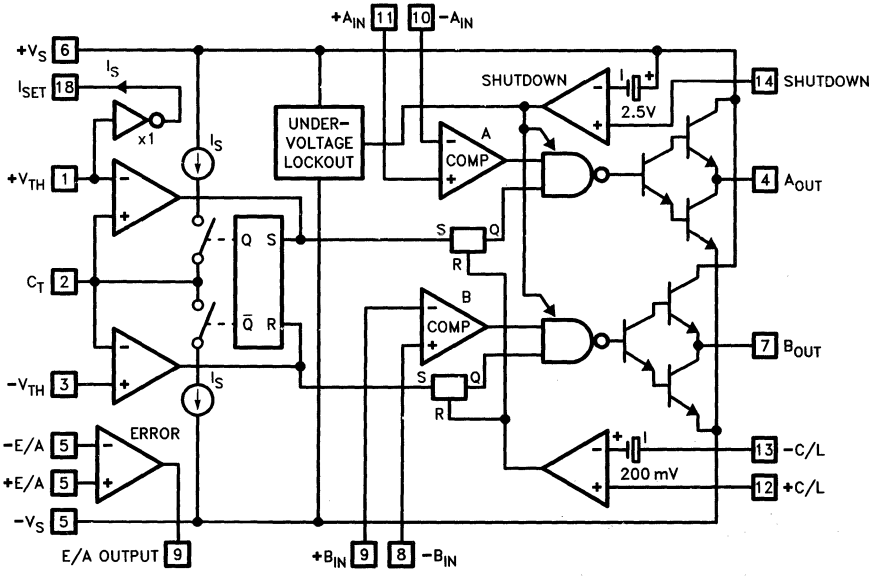
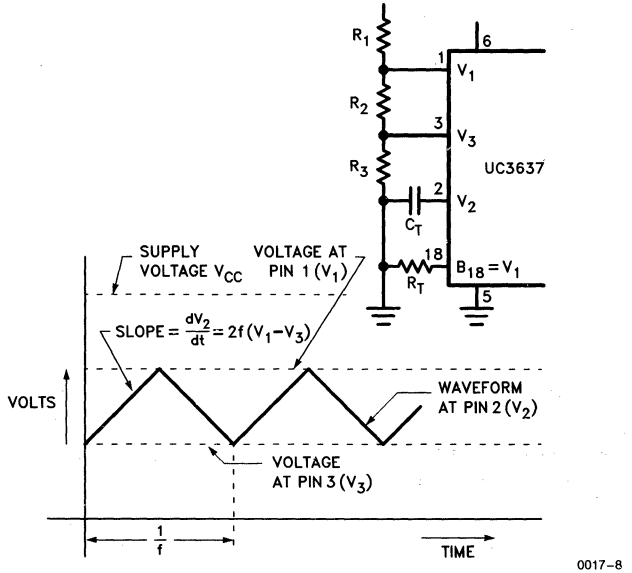


Figure 7. Block Diagram of the UC3637. The two outputs can drive power MOSFETs directly.



f = ramp frequency

$I_T = \frac{V_{18}}{R_T} = \frac{V_1}{R_T}$ (should be about 0.5 mA)

then, $R_T = 2000\ V_1\ (\Omega)$

$C_T = \frac{250 \times 10^{-6}}{f(V_1 - V_3)}(fd)$

Figure 8. Setting up the ramp oscillator requires only five external components.

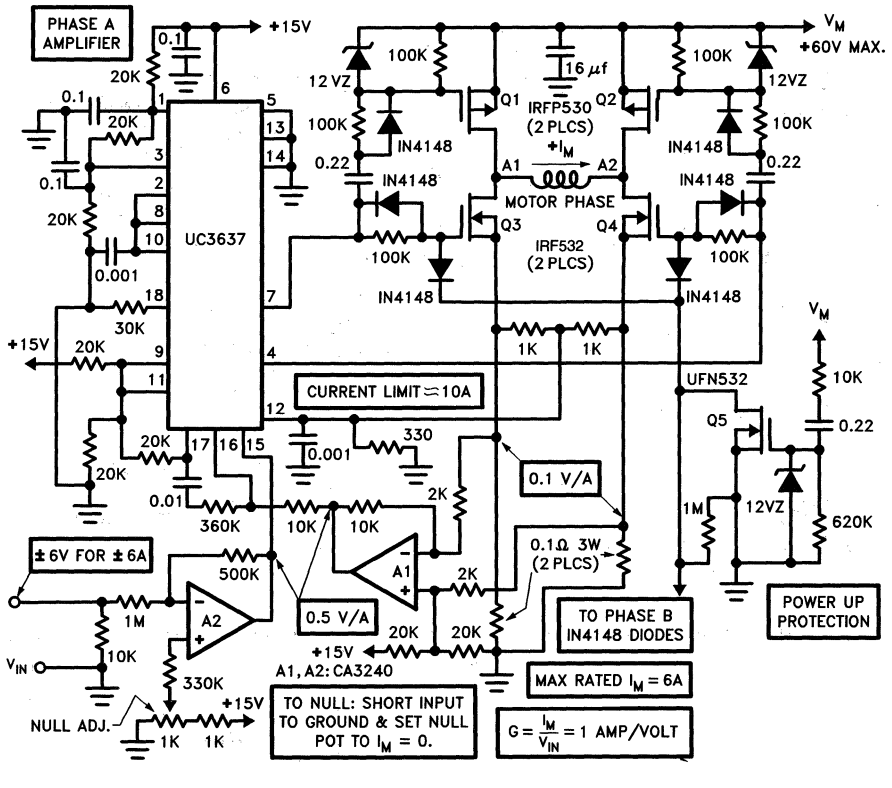


Figure 9. PWM Transconductance Amplifier UC3637

The error amplifier is used as a source for the control signal. But because its output (pin 17) has a voltage range greater than the +5V to +10V range of the V_C ramp signal, and we want to prevent the modulation range from ever reaching 0% or 100% (because of the capacitively coupled P-channel MOSFET devices) we add a simple resistive network consisting of three equal resistors to serve as an attenuator. The final result can be seen in the complete schematic of Figure 9.

CURRENT LIMIT AND CONTROL

The current limit feature of the UC3637 is used to protect the output transistors and motor from excessive current (6A in this case). As the block diagram of Figure 7 shows, the current limit comparator (pins 12 and 13) of the UC3637 is internally biased to a threshold of 200 mV. The network that connects the two sense resistors to pin 12, consisting of two 1K and one 330Ω resistors, causes a voltage of 200 mV to appear at pin 12 when the voltage at either sense resistor is about 1V, corresponding to a current of 10A. Consequently, the maximum output current will be limited to 10A. The current feedback loop is closed by feeding the output of the current sense amplifier to pin 16, the inverting input of the error amplifier of the UC3637. An RC time constant of 3.6 msec is used for the zero in this amplifier's transfer function (equations 8, 9, and 10) which is close to the effective electrical time constant of the motor. Also, a level-shift circuit is provided by means of op amp A2 to permit the use of a control input centered at zero volts, and a control range from −6A to +6A. The circuit allows this even though the op amp is powered by a single positive supply.

TEST RESULTS

The design circuit, shown in Figure 9, was breadboarded for testing at Unitrode and also at Portescap. The assembly includes two amplifiers, one for each motor phase and a "power on" auxiliary circuit for protection of the power MOSFETs. The output devices are equipped with small sheet metal heat sinks.

The circuit draws about 65 mA from the +15V supply. The power output section operates with a supply ranging from +20V to +60V, with no damage occurring if this voltage is lower than +20V.

The circuit performed very well, with excellent linearity and phase matching. The various plots taken, showing output current versus input voltage, are quite straight, and the transconductance is accurate to within 1%. Furthermore, the PWM frequency was subsequently increased to slightly above 100 KHz (by reducing C_T) and the performance re-checked. The result was a marked increase in motor efficiency, due to reduced current ripple, with all other results remaining excellent.

CONCLUSION

Microstepping is a technique of considerable interest in the design of many products, particularly those in which the lower cost of open-loop positioning is an essential parameter. A motor such as Portescap's Model P-750, with its accurately sinusoidal torque curve, becomes even more attractive once its microstepping driver is shown to be fairly simple and inexpensive. The end result is not only precise open loop positioning, but quiet operation, freedom from resonance problems, and excellent electrical efficiency. Incidentally, the motor is available with two quadrature speed sensing coils that can be used for speed and position control, if desired.

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DESIGN NOTES ON PRECISION PHASE LOCKED SPEED CONTROL FOR DC MOTORS

ABSTRACT

There are a number of high volume applications for DC motors that require precision control of the motor's speed. Phase locked loop techniques are well suited to provide this control by phase locking the motor to a stable and accurate reference frequency. In this paper, the small signal characteristics, and several large signal effects, of these loops are considered. Models are given for the loop with design equations for determining loop bandwidth and stability. Both voltage and current motor drive schemes are addressed. The design of a loop for a three phase brushless motor is presented.

PHASE LOCKING GIVES PRECISION SPEED CONTROL

The precise control of motor speed is a critical function in today's disc drives. Other data storage equipment, including 9 track tape drives, precision recording equipment, and optical disc systems also require motor speed control. As the storage density requirements increase for these media, so does the precision required in controlling the speed of the media past the read/write mechanism. One of the best methods for achieving speed control of a motor is to employ a phase locked loop.

With a phase locked loop, a motor's speed is controlled by forcing it to track a reference frequency. The reference input to the phase locked loop can be derived from a precision crystal controlled source, or any frequency source with the required stability and accuracy. A block diagram of the phase locked loop is shown in Figure 1.

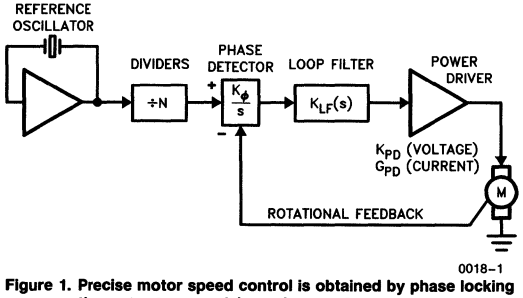


Figure 1. Precise motor speed control is obtained by phase locking the motor to a precision reference frequency.

In Figure 1, a precision crystal oscillator's frequency is digitally divided down to provide a fixed reference frequency. Alternatively, the motor could be forced to track a variable frequency source with zero frequency error. The motor speed is sensed by either a separate speed winding or, particularly in the case of the DC brushless motor, a Hall effect device. The two signals, motor speed and reference frequency, are inputs to a phase detector. The detector output is a voltage signal that is a function of the phase error between the two inputs. The transfer function of the phase detector, K_ϕ, is expressed in volts/radian. A 1/s multiplier accounts for the conversion of frequency to phase, since phase is the time integral of frequency.

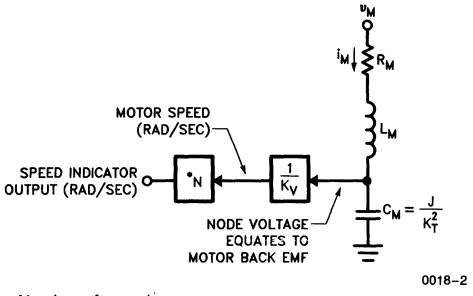
Following the phase detector is the loop filter. This block contains the required gain and filtering to set the loop's overall bandwidth and meet the necessary stability criteria. The output of the loop filter is the control input to the motor drive. Depending on the type of drive used, voltage or current, the driver will have respectively, a V_{OUT}/V_{IN} transfer characteristic, or an I_{OUT}/V_{IN} transconductance.

At first glance, it seems that the motor has simply replaced the V_{CO} (voltage controlled oscillator), in the classic phase locked loop. In fact, it is a little more complicated. The mechanical and electrical time constants of the motor come into play, making the transfer function of the motor more than just a voltage-in, frequency-out block. In order to analyze the loop's small and large signal behavior it is essential to have an equivalent electrical model for the motor.

A SIMPLE ELECTRICAL MODEL FOR A DC MOTOR

Figure 2 is an electrical representation of a DC motor. The terms used are defined here:

- L_M Motor winding inductance in henrys
- R_M Motor winding resistance in Ωs
- J Total moment of inertia of the motor in Nm-sec^2 (**Note:** 1 Nm = 141.6 oz-in)
- K_T Motor torque constant in Nm/Amp
- K_V Voltage constant (back EMF) of motor in volt-sec/rad (**Note:** $K_V = K_T$ in SI units)



*N = Number of speed sense cycles per motor revolution

Figure 2. This simple electrical model is useful for determining the small and large signal characteristics of the motor. Capacitor, C_M is used to model the mechanical energy storage of the motor.

In this model the winding inductance and resistance elements correlate directly with the corresponding physical parameters of the motor, with values taken directly off the manufacturer's data sheet. The capacitor, C_M, models the mechanical energy storage of the motor. Current into the capacitor equates, via motor constant K_T, to motor torque, and the voltage across the capacitor is equal to the motor back EMF. The back EMF voltage equates to motor velocity through the inverse of K_V. In the model, the term N is simply a multiplier equal to the number of feedback cycles obtained per revolution of the motor. For example, in a 4 pole brushless DC motor the commutation Hall effect device outputs will be at twice the rotational frequency of the motor, making N equal to 2.

The equation for the capacitor, given in Figure 2, has the units of Farads if J and K_T are expressed in SI units. In modeling the overall transfer characteristic, it is important that the moment of inertia of the load on the motor be added to the moment of inertia of the motor itself.

It is worthwhile to note that the current into the motor, minus idling current, is proportional to acceleration of the motor. This is easily seen from the model by realizing that the time derivative of the capacitor voltage relates directly to acceleration. The effects of loads on the motor can be modeled by including a current source across the capacitor for constant torque loads, or a resistor for loads that are linearly proportional to motor speed.

TRANSFER FUNCTIONS FOR VOLTAGE AND CURRENT DRIVEN MOTORS

Using the electrical model, the small signal transfer function of the motor is easily derived. Equations 1a and 1b give the small signal frequency response for both the current and voltage driven cases respectively.

$$1a)\quad \frac{N \times \omega_M(s)}{i_M(s)} = \frac{N}{K_V} \times \frac{1}{sC_M}$$

$$1b)\quad \frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{1 + sC_MR_M + s^2 L_MC_M}$$

The transfer function given in equation (1a) describes the small signal response of motor speed, $\omega_M(s)$, to changes in the drive current. Equation (1b) relates the dependence of motor speed to motor drive voltage.

The small signal response of the motor for the current driven case has a DC pole that results from the relationship of motor torque to velocity, that is, motor velocity is proportional to the integral of motor torque over time. In the current driven motor neither the winding resistance nor inductance appear in the transfer function. This is because these elements are in series with the current source output of the driver stage. As long as the output impedance of the driver remains large relative to the impedance of these elements, the resistance and inductance of the motor will have a negligible effect on the small signal response.

The voltage driven response has a second order characteristic that results from the interaction of the series RLC. In many cases the transfer function of the voltage driven case can be simplified. If the quality factor of the series RLC of the motor model is much less than one, as defined in equation 2, then the response of the motor can be accurately approximated by equation 3.

$$2)\quad Q_M = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} = \frac{K_T}{R_M}\sqrt{\frac{L_M}{J}}$$

$$\therefore Q_M \ll 1 \quad \text{If } R_M \gg K_T\sqrt{\frac{L_M}{J}}$$

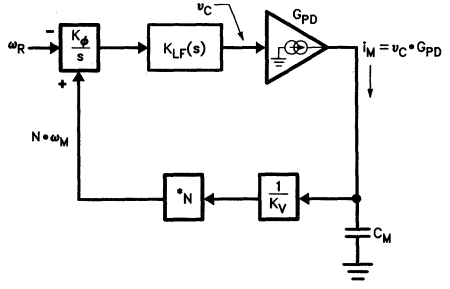
$$3)\quad \text{For } Q_M \ll 1$$

$$\frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{(1 + sC_MR_M)(1 + sL_M/R_M)}$$

CONSIDERING THE WHOLE LOOP

Figure 3 shows the complete speed control loop for the current driven case. The overall open loop response, A_{OLC}, is easily written.

$$4)\quad A_{OLC}(s) = \frac{K_\phi \times K_{LF}(s) \times G_{PD} \times N}{s^2C_M \times K_V}$$



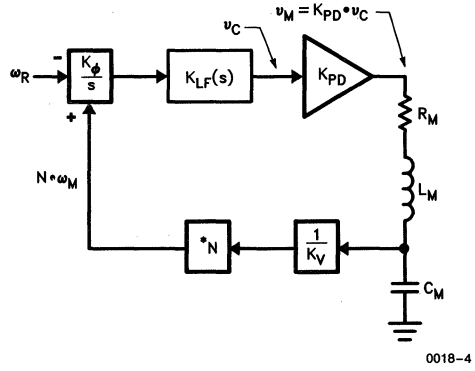
*N = Number of feedback cycles per motor revolution

Figure 3. In this phase locked loop, with current mode drive to the motor, the motor winding resistance and inductance can be ignored as long as the current driver maintains a high output impedance.

For this loop, note that there are two poles in the response at DC, i.e., s = 0. One pole is due to the response of the current driven motor, the second pole is from the frequency to phase transformation of the phase detector. The 180 degrees of phase shift this pair of poles introduce force a phase lead configuration of the loop filter in order to obtain a loop phase margin greater than zero.

The complete voltage loop is shown in Figure 4, and its open loop response, $A_{OLV}(s)$, in equation 5.

$$5)\quad A_{OLV}(s) = \frac{K_\phi \times K_F(s) \times K_{PD} \times N}{sK_V \times (1 + sC_MR_M + s^2 L_MC_M)}$$



*N = Number of feedback cycles per motor revolution

Figure 4. With voltage mode drive to the motor the electrical time constant of the motor plays a part in the small signal response of the speed control loop.

This response has only one pole at DC, although the total number of poles is three versus two for the current driven case. For most motors, particularly those used in constant velocity applications, this transfer function can be simplified by applying the results of equations 2 and 3. This is best illustrated by looking at an example. Consider the following motor, (typical 3-phase brushless for disc drive applications):

K_T ..... 1.5×10^{-2} Nm/Amp
K_V ..... 1.5×10^{-2} V-sec/rad
J (including platters) ..... 1×10^{-3} Nm-sec2
R_M 2.5Ω
L_M ..... 2 mH

For this motor, the model capacitor, C_M, is calculated using the equation in Figure 2 to be equal to 4.4 Farads. If we calculate the quality factor of the series RLC, using equation 2, we find it is equal to 42.4×10^{-3}. This is considerably less than one, and the response closely approximates the non-complex response of equation 3 with poles at 0.014 Hz and 199 Hz.

Typical loop bandwidths will fall well inside this range of frequencies. As long as this is true, the loop response with a voltage driven motor can be approximated by:

$$6)\quad A_{OLV}(s) \approx \frac{K_\phi \times K_{LF}(s) \times K_{PD}/R_M \times N}{s^2 C_M K_V}$$

$$\text{If } Q_M \ll 1 \text{ and } \frac{1}{2\pi C_M R_M} < f < \frac{R_M}{2\pi L_M} \left(f = \left|\frac{s}{2\pi}\right|\right)$$

This expression is the same as the current driven response, equation 4, with the transconductance of the current drive stage, G_{PD}, replaced by the gain of the voltage drive stage divided by the motor winding resistance, K_{PD}/R_M.

CLOSING THE LOOP

When it comes to closing the loop the goal is to have a stable loop with the required loop bandwidth. The variables that must be considered are:

1) The motor
2) The power driver, type and gain
3) The phase detector gain
4) Loop bandwidth
5) The loop filter

The first four of the above variables are usually dictated by conditions other than the stabilizing of the loop. This leaves the loop filter as the tool for achieving the small signal loop requirements.

For many cases involving constant velocity loops for DC motor speed control, the following simple Bode analysis can be applied for determining the design of the loop filter. Assuming we know, or have preliminary guesses for the first four variables listed above, we can plot the Bode asymptotes for phase and gain of the combined response of the motor and power driver. Figure 5 shows, for a typical case, such a plot on a frequency scale that has been normalized to the desired loop bandwidth, or open loop unity gain frequency. This figure illustrates the small signal open loop response for the current driven case, equation 4, minus the response of the loop filter, K_{LF}. If the previously noted assumptions hold, this plot will also apply to the voltage driven case i.e., equation 6.

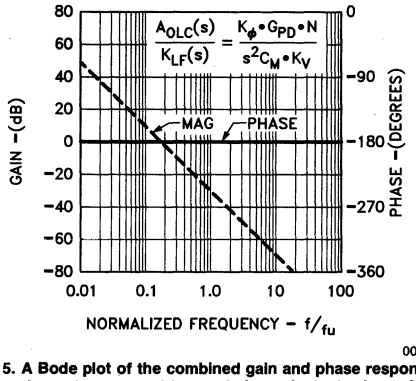


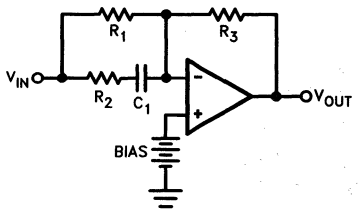
Figure 5. A Bode plot of the combined gain and phase response of the motor, motor drive, and phase dectector is useful in determining the requirements on the loop filter. This plot is normalized to the desired open loop unity gain frequency.

From Figure 5 two restrictions on the loop filter are readily apparent. First, since the remaining portion of the loop has 180° of phase shift over the entire frequency range, the loop filter must have a phase lead at the unity gain frequency and at all frequencies below the unity gain frequency. By meeting this restriction the small signal loop will be unconditionally stable.

Secondly, in order to achieve the desired loop bandwidth, the loop filter must have a voltage gain at the desired unity gain frequency of 30 dB. This level is simply the inverse of the remaining loop's voltage gain at the unity gain frequency.

A loop filter configuration that will meet these restrictions is shown in Figure 6. Also shown in this figure is the small signal response equation for the filter. The response starts out from DC with a flat inverting gain that breaks upward at the zero frequency, ω_Z, and then flattens out again at the pole, ω_P. The pole in this response is necessary to prevent excess feedthrough of residual reference frequency that is present at the outputs of many digital type phase detectors—in fact, as will be discussed in the design example, a separate reference filter is normally required.

A good choice for the relative positioning of the pole and zero of the loop filter response is to space them apart by 1 decade of frequency, and center them around the unity gain frequency. Figure 7 shows the Bode plots of this suggested positioning applied to the case illustrated in Figure 5. As shown, a phase margin of about 45° is obtained with this configuration.



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_3}{R_1} \times \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\,C_1}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

Figure 6. This loop filter configuration provides the required phase lead and gain at the loop crossover frequency.

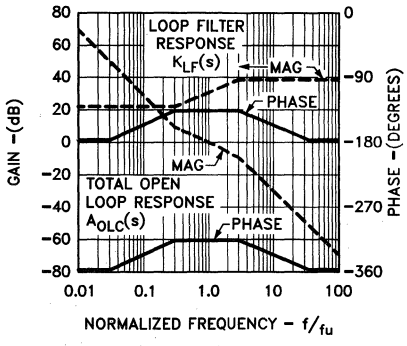


Figure 7. Using the criteria set forth for the design of the loop filter, the resulting Bode plot indicates a phase margin of 45°.

If the above results are acceptable, then the following simple steps can be applied to pick the loop amplifier component values. Referring to Figure 6.

1) Pick R_3 to be as high in value as acceptable for the Op-Amp and board restrictions.

2) $R_1 = (R_3 \times 3.33)/10^{X/20}$, where X is the voltage gain, in dB, required at the unity gain frequency.

3) $R_2 = R_1/9$, sets a 10:1 ratio for ω_P to ω_Z.

4) $C_1 = (2\pi \times R_2 \times 3.33 \times f_{\mu})^{-1}$, where f_{μ} is the loop unity gain frequency.

Using this simple procedure the small signal loop is easily closed for stable static operation.

A DESIGN EXAMPLE

As an example, let us take a look at the complete design of a constant velocity speed control loop for a disc drive application. The performance characteristics for the circuit can be summarized as:

Motor speed ..... 3600 rpm ±60 ppm (0.006%)
Speed stability ..... ±50 ppm
Start-up lock time ..... 10 seconds
Input voltage ..... 12 Volts
Motor idling current ..... 0.5 Amps

The schematic for this design is shown in Figure 8. The motor is a 4 pole 3-phase brushless with the electrical and mechanical specifications given in the figure. The motor is current mode driven with the UC3620 3-phase Switchmode Driver. The speed control function is realized with the UC3633 Phase Locked Controller.

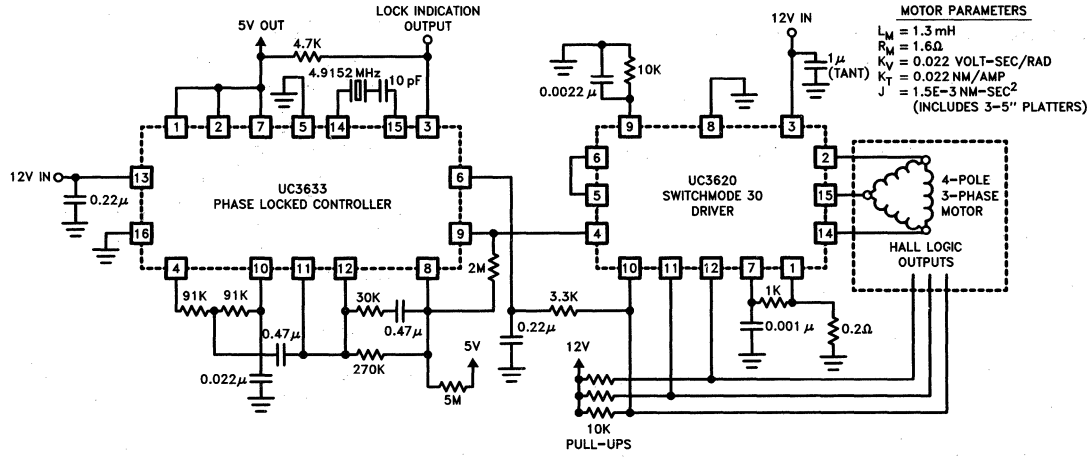


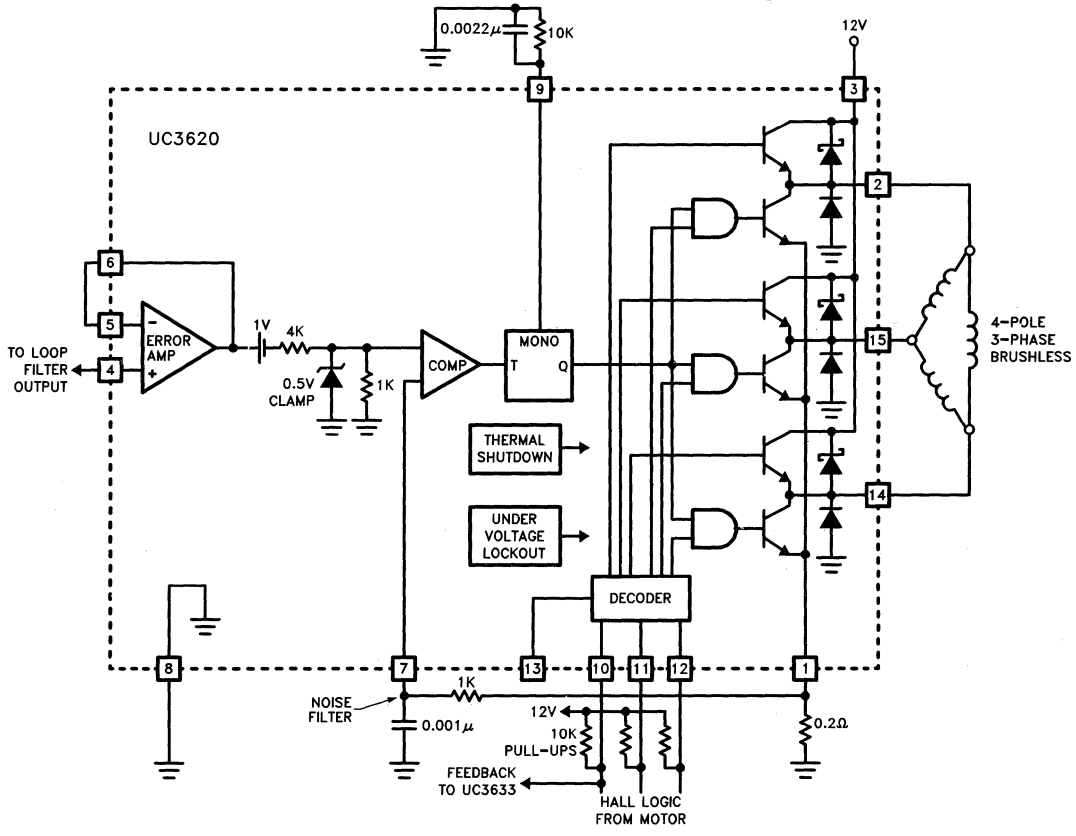
Figure 8. A precision speed control loop uses the UC3620 Switchmode 3-phase Driver and the UC3633 Phase Locked Controller to spin a DC brushless motor at 3600 rpm, ±60 ppm.

POWER DRIVER STAGE

In Figure 9 a detail of the driver IC and the associated circuitry is shown. The UC3620 is a current-mode, fixed off-time, chopper. Three 2-Amp totem pole output stages with catch diodes drive the three motor phases. The outputs are enabled by the internal commutation logic that responds to the three Hall logic signals from the motor. The motor is equipped with open collector Hall devices making the three 10k pull-up resistors on the UC3620 Hall inputs necessary.

Current is controlled by chopping the lowside drive to the phase winding under the command of the UC3620's current sense comparator. The RC combination on the timing pin of the driver sets the off-time at 22 μs. This results in a chopping frequency of well over 20 kHz under normal operating conditions.

The transconductance of the driver is set by the value of current sense resistor used at the emitter pin of the UC3620. With a value of 0.2Ω the transconductance from the error amplifier output to the driver outputs is 1 Amp/Volt. The UC3620 error amplifier is configured here as a unity gain buffer, thus the drive control signal is applied at the non-inverting error amplifier input with the same overall transconductance. An internal 0.5V clamp diode at the current sense comparator input results in a 2.5 Amp maximum drive current. There is a 1V offset internal to the UC3620 that is reflected to the drive control input at zero current. This offset combines with the 0.5 Amp idling current level of the motor to set the steady state DC voltage at the driver control input to be 1.5V.



0018-9

Figure 9. The UC3620 is a current mode fixed off-time driver. This device includes all the drive and commutation circuitry for a three phase brushless motor. The 0.2Ω current sense resistor and the internal divide by five sets the transconductance of this power stage to 1 Amp/Volt.

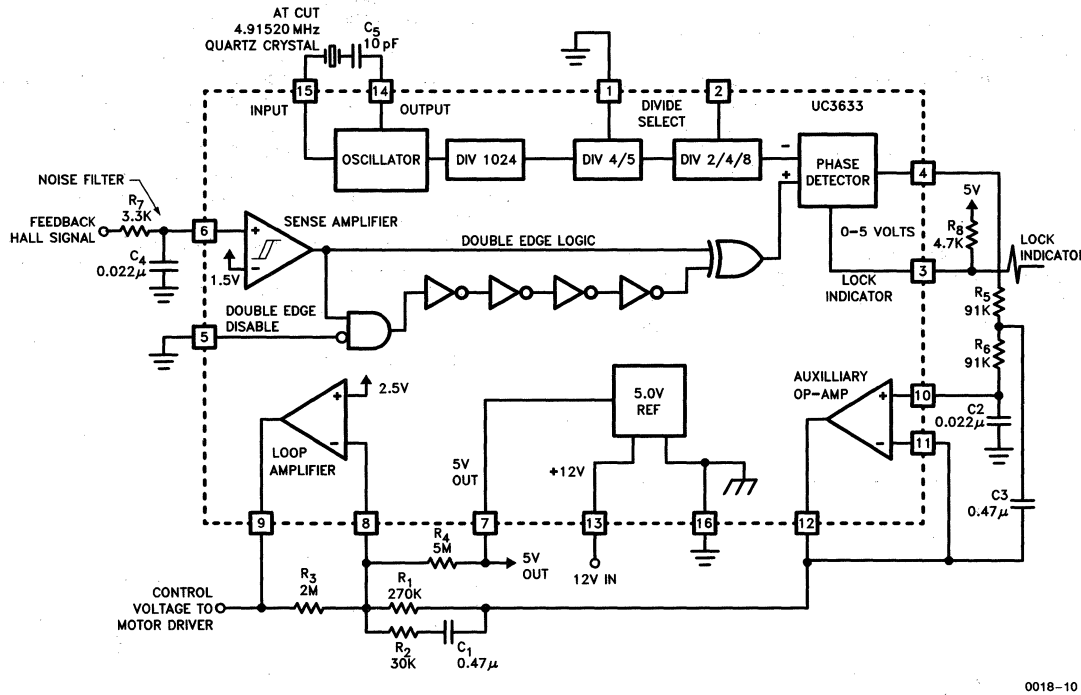


Figure 10. Phase locking the motor to a precision reference frequency is achieved with the UC3633. The double edge sensing option on this device doubles the loop gain and allows twice the reference frequency to be used for a given motor RPM by forcing the phase detector to respond to both edges of the Hall feedback signal.

PHASE LOCKED CONTROL CIRCUIT

A detail of the phase locked control portion of the design is given in Figure 10. The UC3633 contains all of the circuitry required for this function including: a crystal oscillator, programmable reference dividers, a digital phase detector, and op-amps for the required filtering. The UC3633 receives velocity feedback from the Hall signal applied at its sense amplifier input pin. The sense amplifier has a small amount of hysteresis that provides fast rising and falling input edges to the following logic. A double edge option is available on the UC3633 sense amplifier. When this option is enabled, as it is in this design, the phase detector is supplied with a short pulse on both the rising and falling edges of the feedback signal, effectively doubling the loop gain and reference frequency.

The required reference frequency for this loop is 240 Hz, given by the product of the motor rotation of 3600 rpm (60 Hz), the number of cycles/revolution at the Hall outputs (two for a 4 pole motor), and a factor of two as a result of the double edge sensing. The divider options on the UC3633 are set up such that standard microprocessor crystals can be used. In this instance, a 4.91520 MHz (±50 ppm) AT cut crystal is divided by 20,480 to realize a 240 Hz reference frequency input to the phase detector.

The phase detector on the UC3633 responds to phase differences at its two inputs with output pulses at the reference frequency rate. The width of the pulses is linearly proportional to the magnitude of the phase error present.

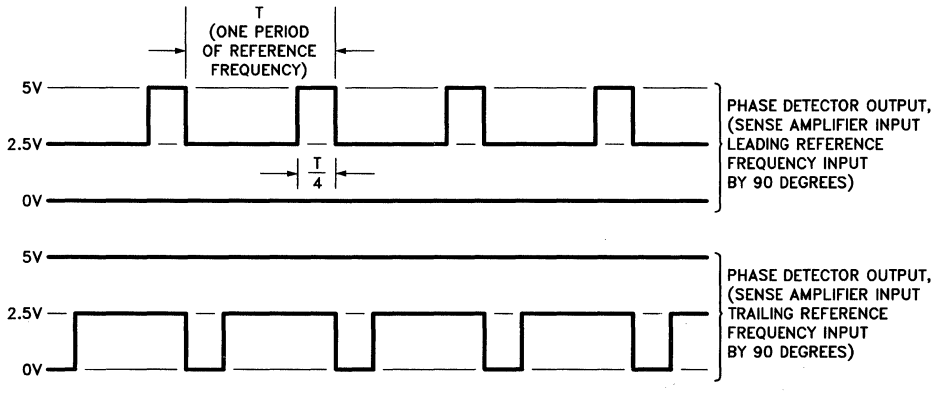


Figure 11. The phase detector on the UC3633 is a digital circuit that responds to phase error with a pulsed output at the reference frequency rate. The width and polarity of the pulses depend respectively on the phase error magnitude and polarity. If any static frequency error is present, the detector will respond with a constant 0 Volt or 5 Volt signal depending on the sign of the error present.

The pulses are always 2.5V in magnitude and are referenced to 2.5V at the detector output. The polarity of the output pulses tracks the polarity of the input phase error. This operation is illustrated in Figure 11. The resulting phase gain of the detector is $2.5V/2\pi$ radians, or about 0.4V/rad, with a dynamic range of $\pm 2\pi$ radians.

The phase detector also has the feature of absolute frequency steering. If any static frequency error exists between the two inputs, the output of the detector will stay in a constant high, or low state; 5V, if the feedback input rate is greater than the reference frequency and 0V, if the opposite frequency relationship exists. The lock indicator output on the UC3633 provides a logic low output when any static error exists between the feedback and reference frequencies.

A unity gain bandwidth of 4 Hz was chosen for this loop. This unity gain frequency is well below the effective sampling frequency, the 240 Hz reference, and is sufficently high to not significantly affect the start-up lock time of the drive system. The design of the loop filter follows the guidelines described earlier. The magnitude of the loop gain, minus the loop filter, at 4 Hz is equal to:

$$\frac{K_\phi \times G_{PD} \times N}{(2\pi f)^2 \times C_M \times K_V} = \frac{(0.4)(1)(4)}{(2\pi 4)^2(3.1)(0.022)}$$

$= 37.2$ E-3 or -28.6 dB.

This dictates that the loop amplifier has a gain of 28.6 dB at 4 Hz. A value for the loop amplifier feedback resistor, R_3, of 2 MΩ was chosen. The values for R_1, R_2 and C_1 were calculated as follows.

$R_1 = (2E6 \times 3.33)/10^{28.6/20} = 248$ kΩ (270 kΩ used).

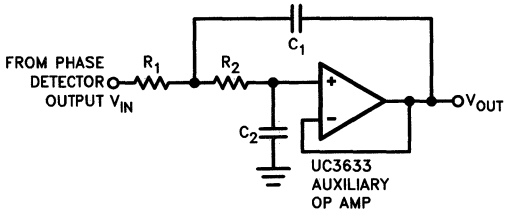
$R_2 = 270/9 = 30$ kΩ

$C_1 = (2\pi \times 30E3 \times 3.33 \times 4)^{-1}$
$= 0.4\ \mu F$ ($0.47\ \mu F$ used).

The additional op-amp on the UC3633 is used to realize a second order active filter to attenuate the reference component out of the phase detector. The filter is a standard quadratic with a natural frequency of 17.2 Hz and a Q of about 2.3. This circuit provides 46 dB of attenuation at 240 Hz while adding only 5° of phase shift at the 4 Hz loop crossover frequency. In Figure 12 design guidelines and response curves for this filter are given.

9

Reference Filter Configuration



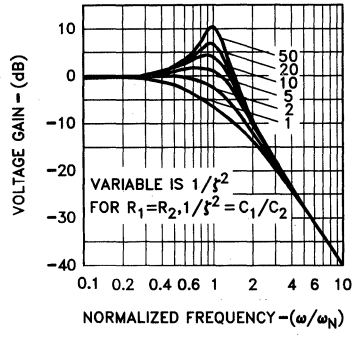
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid—Gain Response



Reference Filter Design Aid—Phase Response

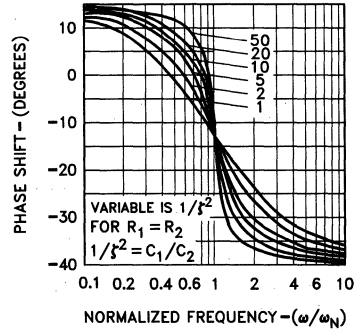


Figure 12. To keep feedthrough of the residual reference frequency at the phase detector output to a minimum, a simple quadratic filter can be used. The design of this filter is easily accomplished with the above equations and response curves.

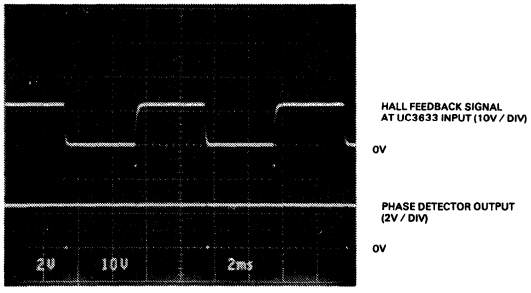
As mentioned earlier, a separate reference filter is required in this type of phase locked loop to attenuate the reference frequency feedthrough at the output of the phase detector. With the active filter following the phase detector, the feedthrough to the loop amplifier is kept to less than $20mV_{pp}$ under the worst case condition of $\pm\pi(180°)$ phase error. This is small compared to the 1.25V DC signal out of the detector at this phase error. If the reference ripple into the loop amplifier becomes large compared to the averaged phase error term, large signal instabilities may result. These are primarily the result of the unidirectional nature of the motor drive.

The static reference ripple at the motor drive input, during phase locked conditions, can be minimized by forcing the loop to lock at zero phase error—at zero phase error there is no reference frequency component at the detector output. The finite DC gain through the loop filter, dictated by the inherent second order nature of the loop, results in a static phase error that is a function of: the DC level required at the motor drive input, the DC gain and reference voltage of the loop amplifier, and the voltage levels out the phase detector. The addition of resistor R_4, see Figure 10, from the loop amplifier's inverting input to

the 5V reference sets the zero phase operating voltage at the loop filter output to 1.5V. This matches the nominal operating voltage required at the UC3620 control input, taking into account the 0.5 Amp idling current of the motor and the 1V offset of the driver. This cancellation is subject to variations due to shifts in DC operating levels, so, while it does significantly reduce static reference feedthrough, it can not be expected to reliably set exactly zero phase operation.

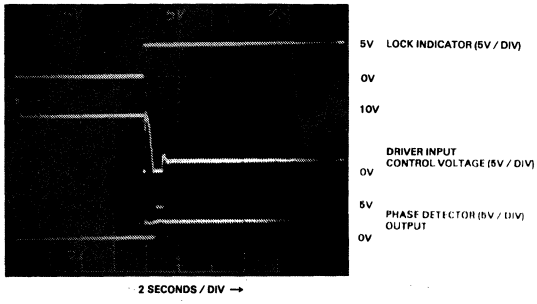
The oscilliscope traces in Figure 13 show the Hall input to the UC3633 along with the output waveform of the digital phase detector under static phase locked conditions. Notice that the phase detector output is alternating between positive and negative output pulses. This is a result of a slight asymmetry on the Hall input signal in conjunction with the use of the double edge sensing being used. In this case, the asymmetry is due to differences in the rising and falling edges of the Hall signal that result from the RC filter at the sense amplifier input. This filter is required to keep high frequency noise from the motor drive out of the phase detector.

The startup response of the motor is pictured in Figure 14. Shown are the voltage waveforms at the lock indicator output, the loop amplifier output, and the phase detector output of the UC3633. At the moment the lock indicator goes high the motor has reached its operating velocity. The absolute frequency steering of the phase detector forces a slight overshoot in frequency that delays the settling of the loop by about 1 second. Without the frequency steering feature the phase detector would command a much lower average drive signal during startup, extending the start time by over 50%.



0018-15

Figure 13. This oscilloscope trace shows the static waveforms at the Hall sensor input, and phase detector output of the UC3633. The static phase error has been adjusted, with R_4 in Figure 10, to be very small. The alternating positive and negative pulses at the output of the phase detector is due to an asymmetry in the Hall signal.



0018-16

Figure 14. The startup lock time of the motor is minimized with the absolute frequency steering feature of the phase detector, keeping lock times under 10 seconds.

9

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UC 3841 PWM CONTROLS 300 WATT OFF-LINE POWER SUPPLY

by Bill Andreycak
UICC Application Dept.

INTRODUCTION

With the introduction of the UC3841, Unitrode has provided a control chip uniquely optimized to implement primary side control for a broad range of power supply applications. This form of control requires significant programming and fault protection intelligence over and above the requirements for merely regulating an output voltage. These are included in the UC3841 in the form of over-voltage, under-voltage, and over-current sensing, in addition to low-current start-up, feed-forward line regulation, duty cycle limiting, slow turn-on, and optional fault latch-off.

Although all of these features are important to most off-line power supplies - and are incorporated in the design described herein - it is beyond the scope of this paper to discuss the inner workings of the control circuit. Rather, the reader is referred to the UC1841/3841 data sheet and to Unitrode Application Note U-91 describing its predecessor, the UC1840 for details of the IC implementation. This note describes the use of the UC3841 as the controller in a typical application - a 300 watt off-line power supply.

TOPOLOGY OVERVIEW

A buck-derived, two transistor forward topology was selected for this example for several important reasons: two 400 volt transistors are typically much less expensive than one 800 volt unit; peak currents and ripple are much less than with a flyback configuration; clamping is done to the bulk DC lines eliminating the need for dissipative high-voltage snubbers; and transformer reset is automatic requiring only a 50% maximum duty cycle limitation. The basic power stage configuration and typical operating waveforms are shown in Figure 1.

While the UC3841 is compatible with either voltage or current mode control, this design is a voltage-mode configuration which takes advantage of the UC3841's controlled PWM ramp waveform to accomplish fast feed-forward line regulation while also guaranteeing an absolute 50% maximum duty cycle clamp.

SWITCHING FREQUENCY

A design decision of equal importance to the power topology is the choice of switching frequency. For this example, 200 kilohertz was selected as an optimum compromise between minimizing the sizes of the magnetic and storage components and achieving a high overall efficiency. This frequency is high enough to keep the number of transformer turns low and yet not so high as to incur significant switching or core losses. Standard commercial devices were used throughout to demonstrate the cost effectiveness of this design.

DESIGN SPECIFICATIONS

The specification goals which were established - and met - for this design example are the following:

Input voltage (110 VAC input) = 85 min, 135 max VAC

Input voltage (220 VAC input) = 170 min, 275 max VAC

AC line frequency = 50 Hz min

DC bulk voltage = 200 min, 385 max VDC

Output voltage = 15 volts

Output current = 20 amps max continuous

Switching frequency = 200 kilohertz

Line regulation = 10 mV

Load regulation = 10 mV

Output voltage ripple = 100 mV pk-pk, DC to 20 MHz

Efficiency = 85% at full load

CIRCUIT OVERVIEW

The complete schematic for this 300 watt power supply is shown in Figure 2 but before discussing the details of the design, it is instructive to understand the overall approach.

The design starts with a 110 volt input voltage doubler for a nominal 290 volt DC main allowing either 110 or 220 volt operation. The control and drive circuitry are configured for low start-up current so that starting energy is accumulated in a low voltage capacitor, C10 in Figure 2, which is charged from the high-voltage bulk DC through a large-valued resistor, R2. After starting, the higher operating currents of the control and drive circuits are supplied from an efficient low-voltage winding on the power transformer. This would normally be a separate primary-referenced axillary winding and isolation would be incorporated in the feedback path for output voltage control. For this example, isolation was

TWO-TRANSISTOR FORWARD CONVERTER

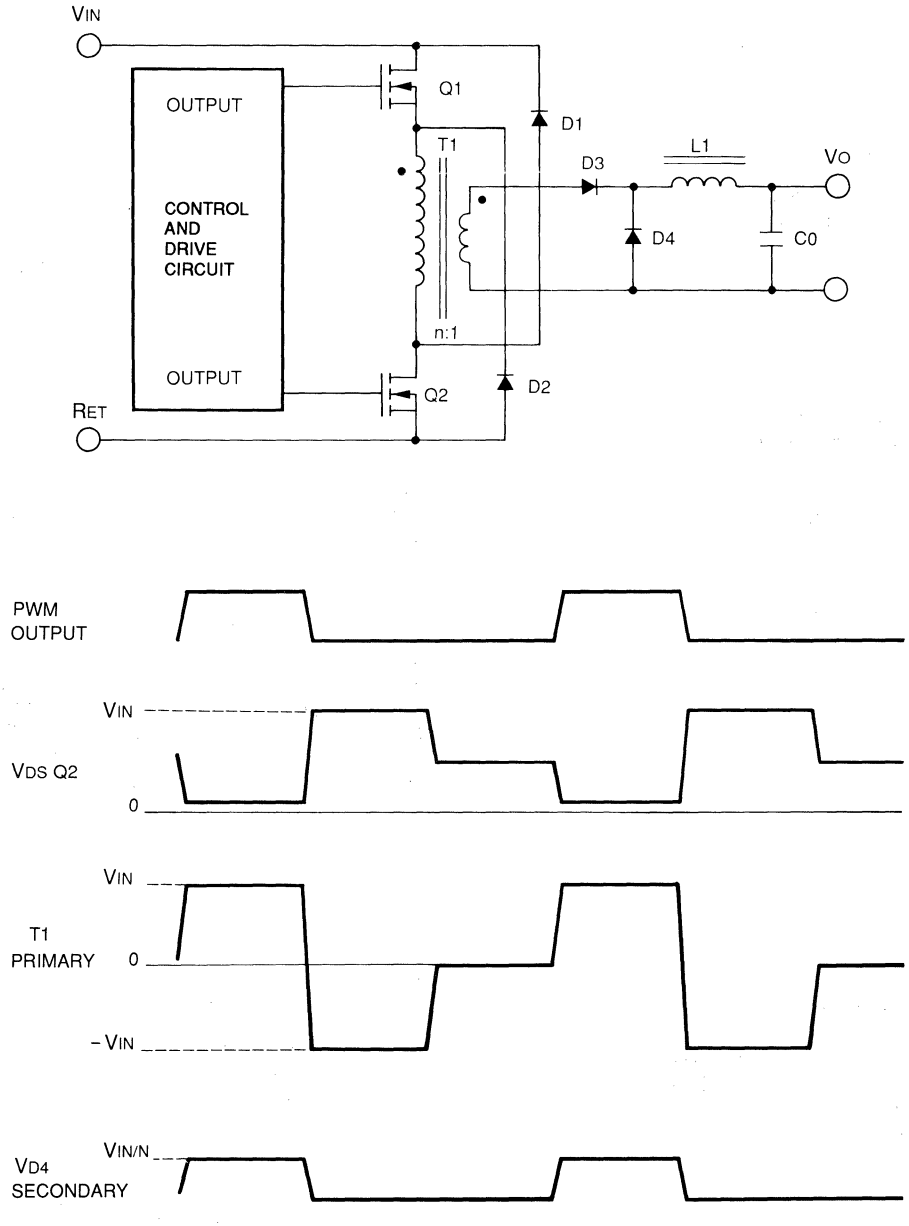

Figure 1. Basic power topology and typical waveforms for the Two-Transistor Forward Converter

ignored and operating power after start-up was taken from the 15 volt output - a simplification which can easily be remedied using common techniques which will not affect the remaining design.

The UC3841 provides the means to sense adequate energy in the start-up capacitor and initiate the turn-on sequence. It then activates the UC3707 Driver which boosts the PWM output from the UC3841 to a high peak current, source/sink drive command.

This signal is level-shifted by transformer T1 and applied simultaneously to the gates of the two power MOSFET switching devices, Q2 and Q3. These two FET's drive the power transformer, T2, in the forward direction with reset provided by D6 and D9.

Additional features which are incorporated in this design include slow turn-on - both initially and after fault shutdown, over-voltage and over-current shutdown, pulse-by-pulse current limiting for light overloads, feed forward for fast line regulation, and a maximum duty cycle clamp.

CIRCUIT DESIGN DETAILS

INPUT STORAGE CAPACITANCE

The amount of input, or bulk storage capacitance for a given power supply design will be determined by the more stringent of three separate requirements:

1. Maintaining a minimum DC bulk voltage as the input capacitor supports the converter between AC cycles.

2. Providing a minimum hold-up time for operation after loss of the AC line voltage.

3. Meeting the requirements for AC RMS charging current.

In this case, the value was calculated to support the primary voltage between AC cycles to a minimum of 200 VDC. In a dual voltage system, the most stringent case is the doubler configuration where there is a 180 degree phase shift between the voltage waveforms on each of the series capacitors. The minimum DC bulk voltage is then the sum of the minimum voltage on one series capacitor plus the average voltage on the other. The value of each capacitor is calculated from the following formula:

$$C1 = C2 = \frac{\text{Output power}}{\text{Efficiency} \times \text{AC frequency} \times (Vc\ peak^2 - Vc\ min^2)}$$

Where, in this example,

AC frequency = 50 Hz,

Vc peak = (80 x 1.414) - Vd = 115 V, and

Vc min = .33 (2 x 200 - Vc peak) = 95 V

which determines a value for C1 and C2 of 1680 microfarads each. This was actually implemented as shown in Figure 2 by four 1000 uF units, C1 through C4.

PRIMARY AND SECONDARY CURRENT

An estimate of the maximum primary and secondary currents is needed to select the power switches, diodes, and transformer wire sizes. A first-order approximation can be calculated from the equation:

$$Ipeak = \frac{\text{Output power}}{\text{Efficiency} \times \text{Input voltage} \times \text{Max duty cycle}}$$

$$= \frac{300}{0.85 \times 200 \times 0.50} = 3.52 \text{ Amps}$$

For rectangular wave forms, RMS currents are calculated by multiplying peak current by the square root of the duty cycle yielding 2.5 Amps of primary current and 14 Amps for the secondary winding.

MOSFET SELECTION

As described in the Topology section, one advantage of the two-transistor forward converter is that the maximum voltage on the power switches does not exceed the peak input voltage. In this example, it allows the use of 500 Volt IRF 840 power MOSFETs which have a fairly low on resistance of 0.8 ohm, more than adequate current capability, and are available in plastic TO-220 packages. Heatsink requirements can be calculated by starting with the DC losses:

$P\ loss = Ip\ peak^2 \times Rds\ on\ max \times D\ max$

Extrapolating the maximum Rds on value for the IRF 840 to a junction temperature of 110°C yields 1.75 ohms which means a DC loss of 10.8 watts. Rounding up to 12 watts to include switching losses means that with a maximum ambient temperature of 70 °C, the junction will stay below 110 °C if the total thermal resistance, including the 1.0°C/W of the TO-220 package, is held to less than 3.3°C/W.

RESET DIODES

Since the current through the reset diodes, D9 and D10, returns to zero when the core completes reset, diode reverse recovery time is not critical. Forward turn-on time is still important, though, in order to catch the transformer energy when the power switches turn off, but this is a much simpler problem and UES 1106 rectifiers are more than equal to the task.

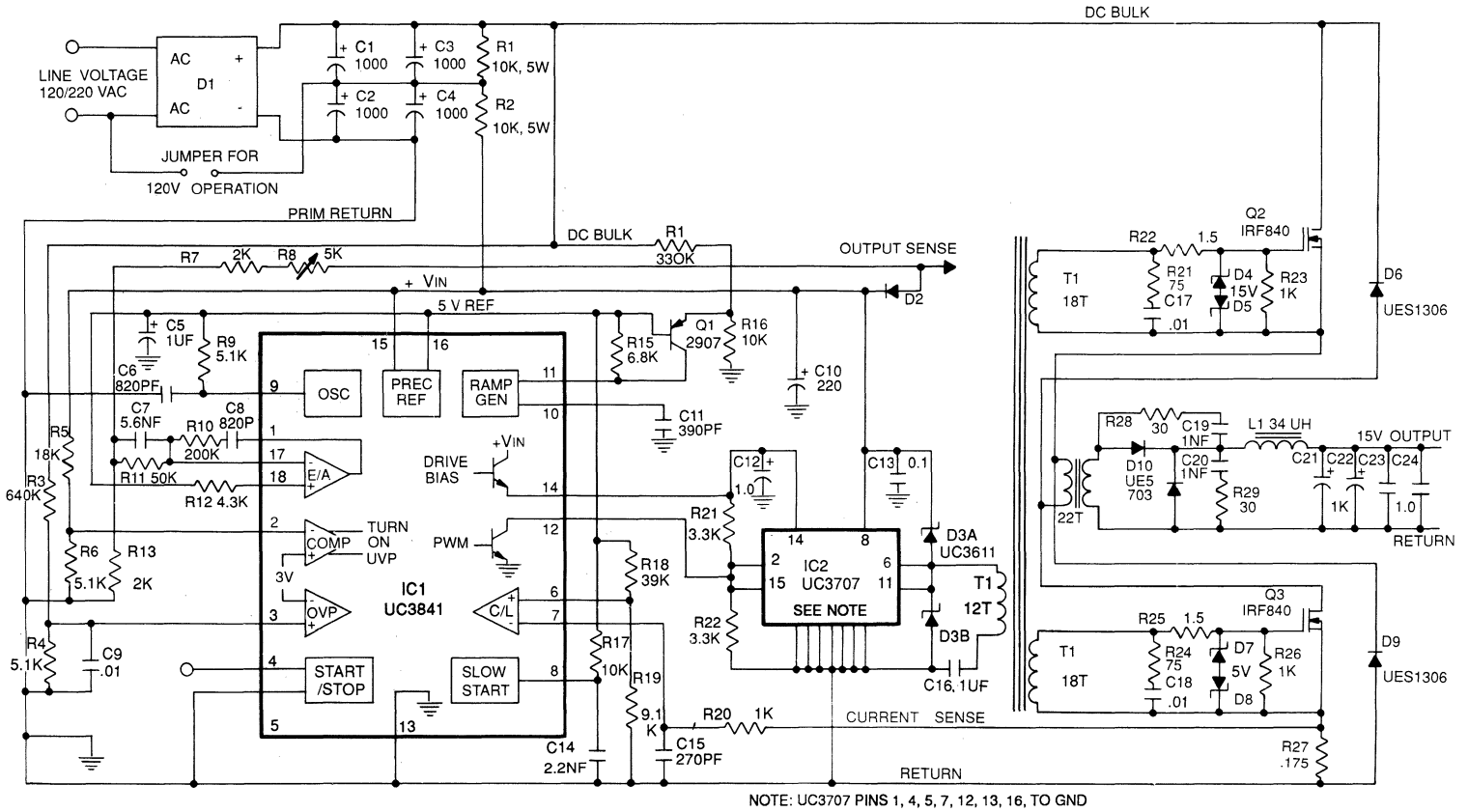

Figure 2. Overall schematic for a 300 watt, off-line power converter using the UC 3841 for control

TRANSFORMER DESIGN

As a general guideline, operation at higher frequencies usually produces a transformer design which is core loss, rather than flux swing, limited. Under these conditions, it is best to start with the core area-product calculation using the formula:

$$AP = AwAe = \left(\frac{Pin \times 10^4}{120\ K\ 2f_t} \right)^{1.58} \times (Kh\ f + Ke\ f^2)^{.66} cm^4$$

where:

Pin = Input Power = 353 Watts

K = Winding Factor = .141 (for a fwd conv)

f_t = Transformer Frequency = 200 kHz

Kh = Hysteresis Coefficient = 4×10^{-5} (3C6A)

Ke = Eddy Current Coefficient = 4×10^{-10} (3C6A)

For this design, the area-product calculates to 2.9 cm^4 allowing a comfortable selection of an ETD-44 ferrite core made of 3C6A material. Core selection is typically an iterative process with the first core choice used to define the windings which, in turn, allows calculation of both winding and core losses. If these answers are not acceptable, another core size is selected and the process repeated.

The manufacturer defines the ETD-44 core as having a volume of 18.0 cm^3 and a thermal resistance of 12°C/W. Selecting 40° C as a reasonable limit for the maximum temperature rise of the transformer and recognizing that core loss will be an important factor, an arbitrary starting point for the transformer design is to allocate 30°C to the core and 10°C to the copper. With this assumption, the core power density can be calculated from:

$$\text{Power Density} = \frac{\text{Temp rise}}{\text{Therm Resist x Volume}} = 140\ mW/cm^3$$

The manufacturer's curves of core losses for the 3C6A material at an operating frequency of 200kHz show a corresponding peak flux density of approximately 600 Gauss which equates to a peak-to-peak value of 1200 Gauss, or 0.12 Tesla. Additional data needed to calculate the primary turns are the primary voltage, Vp = Vin - Vsat, and an estimate of the maximum duty cycle which, to provide some margin, is initially set at 0.47. With these inputs, the primary turns are defined by:

$$Np\ min = \frac{Vp \times Ton \times 10^4}{\text{Flux swing x Core area}}$$

$$= \frac{190 \times 2.35 \times 10^{-6} \times 10^4}{12 \times 1.74} = 21.3 \text{ turns}$$

The transformer turns ratio is defined as:

$$\frac{Np}{Ns} = \frac{Dmax \times Vp}{Vo + Vd} = Dmax \times \frac{190}{15.8} = 12.025\ Dmax$$

At this point, there are two considerations to balance: The desire to make Dmax as close to 0.5 as possible so that the peak current is low, while keeping the number of turns to low, whole numbers. For this example, the best choice is

$$\frac{Np}{Ns} = \frac{22 \text{ Turns}}{4 \text{ Turns}}$$

and Dmax = 0.46.

With this duty cycle, the peak primary current can be more accurately calculated as 3.84 Amps with an RMS value of 2.6 Amps.

The remaining transformer calculations are summarized below:

Primary inductance, Lp = Al x Np^2 = 1.26 mH

Magnetizing current, Im = Vp x Ton / Lp = 347 mA (peak)

Primary conductor area, Axp = Ip rms / 450 = .00578 cm^2 min

Secondary conductor area, Axs = Is rms / 450 = .0301 cm^2 min

While the primary wire area corresponds to a wire size of AWG 19, and the secondary is equivalent to AWG 12, both have to be evaluated in terms of their active area at 200 kHz. From Eddy Current calculations it can be determined that the depth of penetration of current at 200 kHz is .017 cm which does not effectively utilize the .091 cm diameter of AWG 19 wire. While multiple strands of finer wire help, increasing the number of strands also increases the number of layers which forces the wire thickness to be substantially less than the penetration depth in order to minimize the AC loss.

A more effective solution - which is made more practical because of the relatively few number of turns - is the use of flat copper strip. For the primary, a strip .0044 cm thick (approximately 2 mils) and 2.5 cm wide was insulated with 2 mil mylar between each turn and wound in two sections - eleven turns under and eleven turns over the secondary. The secondary was also made of copper strip, in this case .020 cm thick. A cross section sketch of the transformer winding technique is shown in Figure 3.

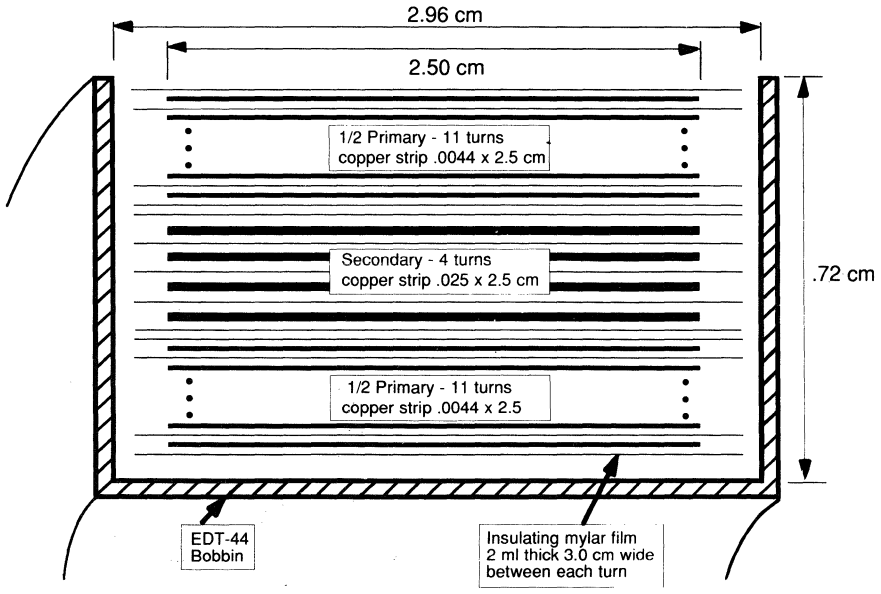

Figure 3. Cross section of one-half of the power transformer illustrating the strip winding techniques which minimize both Eddy Current losses and leakage in ductance.

With the windings defined, the total transformer losses may be calculated as follows:

Core loss = Power density x Volume = 2.52 Watts

$$\text{Primary resistance} = \frac{\text{Copper ohm-cm x ave cm/turn x Np}}{\text{Strip cross-section area}}$$

$$= \frac{2.29 \times 10^{-6} \times 7.6 \times 22}{.0044 \times 2.5} = 35 \text{ milliohm}$$

Wire loss (prim) = $Ip\ rms^2$ x Rp = 0.24 Watts

$$\text{Secondary resistance} = \frac{2.29 \times 10^{-6} \times 7.6 \times 4}{.020 \times 2.5} = 1.39 \text{ milliohm}$$

Wire loss (sec) = 0.26 Watts

Total power loss = 2.52 + 0.24 + 0.26 = 3.02 Watts

Temperature rise = 3.02 W x 12 °C/W = 36 degrees.

GATE DRIVE TRANSFORMER

Since both the number of turns and the currents are small for this gate drive transformer, a toroidal core shape is an efficient solution and the core selected was the Ferroxcube 846T250 made of 3C8 ferrite material with an outside diameter of 0.875 inches. The design equations and guidelines are similar to the power transformer example. In this case, the primary winding is capacitively coupled to the driver IC to prevent core saturation. Because of the DC offset voltage on the capacitor, the primary voltage will now be to some extent dependent upon pulse width. A step-up turns ratio was used to the secondary with 15 volt zener clamps to limit the gate-to-source voltage on each FET. Twelve turns were used for the primary resulting in a 500 Gauss flux swing. Each secondary winding consists of 18 turns and the total core loss is calculated at 0.13 Watt.

OUTPUT INDUCTOR

The output inductor was designed for less than 1.8 Amps of ripple current at full load and minimum duty cycle using the equation:

$$L = \frac{(Vo + Vd) \times Toff}{\Delta Io\ max}$$

and from:

$$Dmin = Dmax \times \frac{Vin\ min}{Vin\ max} = 0.46 \times \frac{200}{385} = 0.239 \text{ and}$$

$$Toff\ max = \frac{1 - Dmin}{f_t} = \frac{0.761}{0.2\ MHz} = 3.81 \text{ us}$$

the inductance value is then defined as:

$$L = \frac{15.8 \times 3.81}{1.8} = 33.4 \text{ uH Min}$$

Selected for this application was an ETD type core made from 3C8 material. This material was chosen because of its high saturation flux density of greater than 3000 gauss. Here again, it is necessary to determine whether the design will be core loss or saturation limited but since this is a forward converter with the inductor in the continuous mode, the AC ripple current is a small percentage of the DC load current and the core should be saturation limited.

The core selection process again starts with a calculation of window - area product using the equation:

$$AP = AwAe = \left(\frac{L \times Ipk \times Ifl \times 10^4}{420 \times K \times Bmax} \right)^{1.31} cm^4$$

$$= \left(\frac{34 \times 10^{-6} \times 25 \times 20 \times 10^4}{420 \times 0.7 \times 0.3} \right)^{1.31} = 2.36\ cm^4$$

With this AP value, an ETD-39 core was selected with a value of Ae = 1.25 cm^2. The minimum number of turns can then be calculated from:

$$Nmin = \frac{L \times Ipk \times 10^4}{Bmax \times Ae} = 23\ Turns$$

The gap length is then calculated using the classic inductance formula:

$$lg = \frac{\mu_o \times \mu_r \times N^2 \times Ae \times 10^{-2}}{L} = 0.219\ cm$$

with $u_o = 4\ \pi \times 10^{-7}$ and $u_r = 1$. To obtain the desired inductance, however, the actual gap must be almost twice as large to account for the fringing field which is not included in the above formula.

This inductor was also wound with copper strip but in this application the task is easier as neither Eddy Current losses nor space for high-voltage insulation need be considered. A strip 2.5 cm wide of 10 mil (.025 cm) copper was used which, with a mean turn length of 6.7 cm, gave a DC resistance of

$$R = \frac{2.29 \times 10^{-6} \times 6.7 \times 23}{0.025 \times 2.5} = 5.65\ mohms$$

and a power loss at full load of 2.26 Watts.

OUTPUT CAPACITOR

There are two sources of ripple voltage which need to be considered in meeting the design goal of 100 millivolts and they are both caused by the inductor ripple current. The first is merely

$$\Delta Vo = \Delta Q / Co$$

and, for a given ripple current, is minimized by increasing the capacitor value. The minimum capacitance, if this was the only contributor, is

$$Cout\ min = \frac{1 \times \Delta Io \times 1 \times 1}{2 \times 2 \times 2f \times \Delta Vo}$$

$$= \frac{1.8}{8 \times 200k \times 0.10} = 11.25\ microfarads$$

The second source of ripple voltage is the voltage drop across the ESR of the capacitor caused by the ripple current. The maximum ESR allowable for 100 mV ripple is

ESR max = 100 mV / 1.8 A = 56 mohms.

The two contributors of ripple voltage do not add directly as there is a 90 degree phase difference between them. Typically, in order to achieve a reasonable ESR, the capacitance value becomes so much greater than the minimum value that the Δ Q / Co term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

For this design, two 470 uF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 mohms - a broad range necessitated by the difficulty in getting specified high-frequency data from capacitor manufacturers.

A final component added to the output filter is a good, high-frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. A 1.0 uF ceramic monolythic capacitor is a good selection for this application.

OUTPUT RECTIFIERS

The output diodes need to be able to handle the output current of 20 Amps, have 150 Volt reverse capability, and be extremely fast. Unitrode UES 703 rectifiers were selected for this application because of their 35 nsec reverse recovery specifications, as well as their low forward drop of 0.8 Volts max. Since one of the output diodes will always be conducting, it is advisable to mount both on the same heatsink designed to dissipate approximately 16 Watts with a 30 °C temperature rise. This will keep the junction temperature below 100 °C in a 70 °C ambient.

PROGRAMING THE CONTROL FUNCTIONS

With the completion of the power path design, the remaining tasks all relate to programing the many functions of the UC3841. In the interests of readability, the description which follows is a somewhat qualitative discussion of the methods for implementing the functions rather than a rigorous derivation of each component's value. Again, reference to the UC3841 data sheet is necessary for detailed specification limits and tolerances.

POWER SUPPLY START UP

When line voltage is first applied, the UC3841 is in its OFF state and draws less than 5mA from the line through R1 and R2. While there is an additional 2.4 mA due to the various programing resistors, the UC3707 draws no current as it is powered from the Driver Bias output of the UC3841 which is off during start up. Therefore, resistors R1 and R2, which are necessary anyway to discharge the bulk storage capacitors, can easily provide the current to charge the start up capacitor, C10, without the power dissipation which would require complex circuitry to disconnect them after start up.

The resistor divider of R5 and R6 performs two functions. The ratio of these resistors determines the actual turn-on voltage at C10 while their effective series impedance provides hysteresis such that turn-off occurs at a lower level than turn-on. In this circuit, the turn-on voltage is 17V and the hysteresis is 3.5V. This means C10 will charge to 17V while most of the circuit is off. When turn-on is initiated, the added load of the driver will cause this voltage to decay and it will fall either to 14.4V where the power supply output will catch it through D2, or, if start up does not take place, to 13.5V where the control will turn off and start a new cycle.

Prior to turn-on, and after a low-voltage turn off, the Soft-Start capacitor, C14 on Pin 8, is clamped low. At turn on, although the Driver Bias immeadiatly activates the UC3707, no power pulses are generated while Pin 8 is low. As C14 charges, PWM commands begin and the pulse width increases with a rate of increase defined by the time constant of C14 and R17. This time constant needs to be selected remembering that while start up is taking place, all the drive energy is coming from C10 so the charge of C14 has to be faster than the discharge of C10. These waveforms are shown in perspective in Figure 4.

START-UP WAVE FORMS

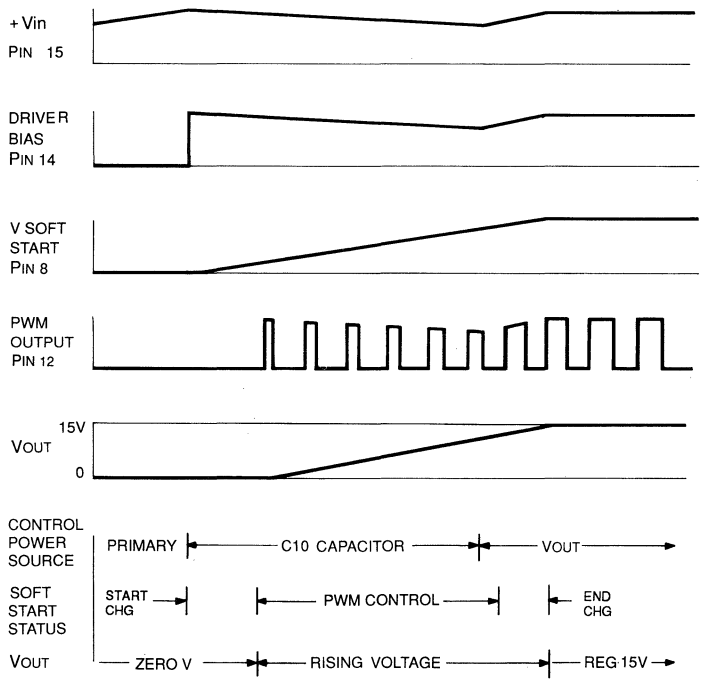

Figure 4. Initial start-up waveforms showing the slow turn on of the power output stage.

OSCILLATOR AND RAMP

The UC3841 operates at a fixed frequency determined by R9 and C6 on Pin 9. The pulse width modulation is performed by comparing the Error Amplifier's output to a separate ramp waveform generated on Pin 10. The slope of this ramp is given a minimum value by R15 charging C11 from the 5.0V reference. These components define a rise time of 2.5 usec and thereby establish a maximum duty cycle clamp of 47 percent. The network of Q1, R14, and R16 sense the DC bulk voltage and provide an increasing charge current to C11 - thereby increasing the slope of the ramp for bulk voltages above 200 volts. This increase in slope linearly tracks the input line voltage and modulates the PWM output signal providing fast, pulse-by-pulse, open-loop line regulation which greatly eases the requirements of the feedback control loop.

FAULT PROTECTION

Load current is sensed through the power transformer by a sense resistor, R27, in series with the power switches. The value of R27, in conjunction with the divider of R18 and R19, establish a threshold at Pins 6 and 7 of 23 Amps as related to the output. When this threshold is exceeded, the UC3841 goes into a pulse-by-pulse reduction in width to limit the energy and allow the power supply output to fall. Because of circuit delays, however, this limiting only works to a minimum pulse width which might allow too much energy to protect against a short circuit. This eventuality is covered by a second, higher threshold in the current sensing circuit which triggers a Fault Latch for immediate shut down. This Fault Latch is also activated by the Over-Voltage comparator which, in this case, is monitoring the input line voltage through R3 and R4.

Once triggered, the Fault Latch immediately terminates the PWM signals and discharges the soft-start capacitor. If the Reset Pin 5 is high, once latched, the circuit will stay off until either the input line is recycled or Pin 5 is momentarily pulled low. If Reset is already low, the Fault Latch will reset when the soft-start capacitor completes its discharge, allowing an automatic restart. The Fault Latch may also be activated externally by forcing positive current into Pin 4.

THE UC3707 DRIVER

This device is used only as an interstage driver to take the pull-down output from the UC3841 and develop the high current turn-on and turn-off commands to the power MOSFETs. This is a dual driver but in this case the two channels are connected in parallel to provide a maximum peak current of 3 Amps, source or sink. Of course, the DIL package would provide a power limitation were it not for the fact that the high currents are needed only to charge and discharge the MOSFET gate capacitance. When driving a load which has both inductance and capacitance, it is important to keep any ringing which might appear on the output of the driver chip confined within the limits of the supply voltage to that chip. This is easily accomplished with the UC3611 Schottky diode array used for diodes D3A and D3B.

CLOSING THE LOOP

In this voltage-mode application, the output filter will exhibit a two pole response to the control loop. Loop compensation at the Error Amplifier is designed to contain two pole-zero pairs by using the configuration shown in Figure 5. This will insure overall loop stability with maximum high frequency response while retaining a large low frequency gain.

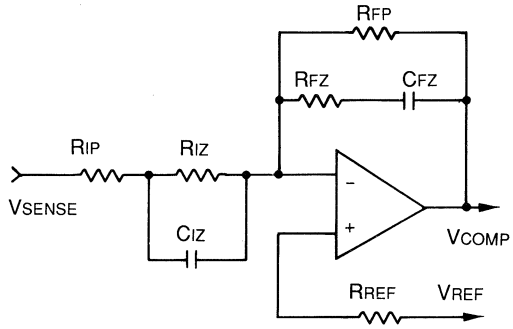

Figure 5. A generalized two pole-zero compensation approach to providing good loop stability.

The generalized approach to this compensation network is to place the first pole at a low frequency, typically around one Hertz. Two zeros are then introduced at approximately one-half the output filter break frequency to compensate for its two-pole rolloff. The amplifier's second pole is placed at a fairly high frequency to provide a predictable gain reduction; however, the amplifier will usually run out of gain-bandwidth prior to reaching this pole.

The output filter response is defined by:

Lout = 34 uH, Cout = 1000 uF,

Rload = 0.75 to 10 ohms, ESR = 3 to 15 mohms

$$\text{Pole freq} = \frac{1}{2\pi\sqrt{L\,C}} = 865\ \text{Hz}$$

$$\text{ESR zero} = \frac{1}{2\pi \times C \times ESR} = 10.6 \text{ to } 53.1\ \text{KHz}$$

The error amplifier compensation poles and zeros are located at the following frequencies referenced to the components of Figure 5:

$$\text{Input zero} = \frac{1}{2\pi \times Riz \times Ci} = 568\ Hz$$

$$\text{Input pole} = \frac{Rip + Riz}{2\pi \times Rip \times Riz \times Ci} = 23\ kHz$$

$$\text{Feedback zero} = \frac{1}{2\pi \times Rfz \times Cf} = 970\ Hz$$

$$\text{Feedback pole} = \frac{1}{2\pi\,(Rfp + Rfz)\,Cf} = 1\ Hz\ (approx)$$

The effect of these poles and zeros is shown graphically in Figure 6 where it can be seen that they provide an overall response with a single pole roll-off to 10 kHz. The gain crosses zero dB at approximately 8 kHz with more than adequate phase margin, regardless of the output capacitor's ESR.

POWER SUPPLY PERFORMANCE

The use of the UC3841 control IC has allowed a very straight forward and simple implementation of a relatively high performance power supply with a remarkedly small number of components. Representative waveforms of performance at several points within the supply are shown in Figures 7 - 10. All the initial performance goals defined for this design were met and it is hoped that with the information presented above, application to more sophisticated or specialized design tasks will be eased.

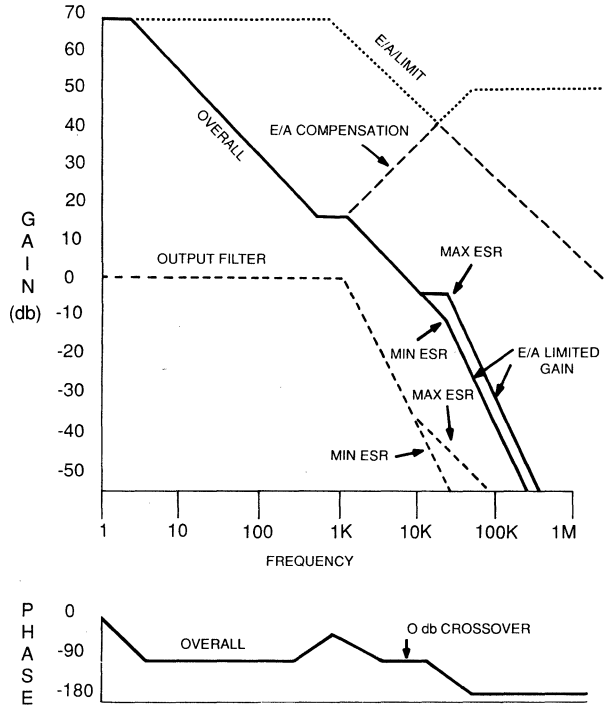

Figure 6. Total power gain and phase relationships showing the effects of loop compensation.

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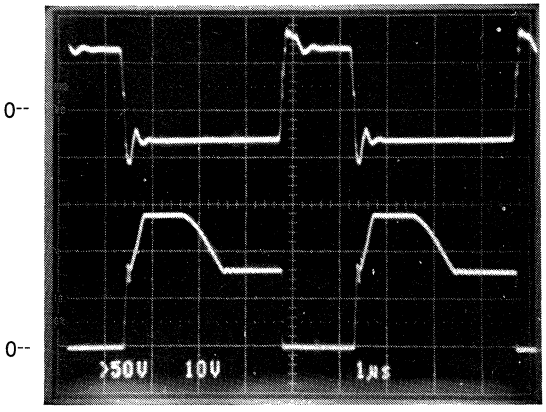
9

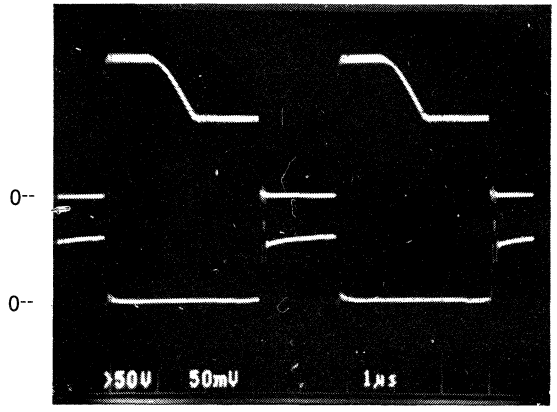
OPERATIONAL WAVEFORMS



PRIMARY

Top: V_{GS} Q1 10 v/cm
Bottom: V_{DS} Q1 100 v/cm
Horizontal: 1 µs/cm

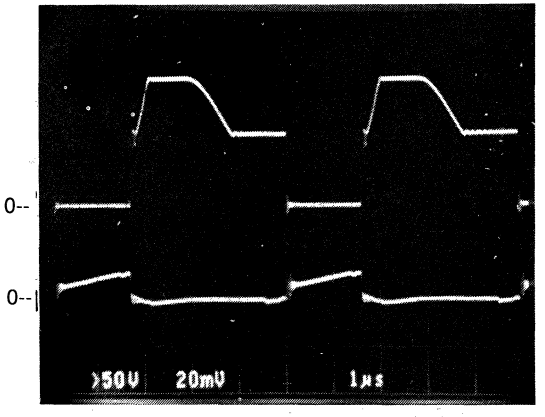
Figure 7. Gate-to-source and Drain-to-source voltage waveforms for the upper FET switch



FULL LOAD

Top: V_{DS} Q1 100 v/cm
Bottom: Ipri 2 A/cm
Horizontal: I µs/cm

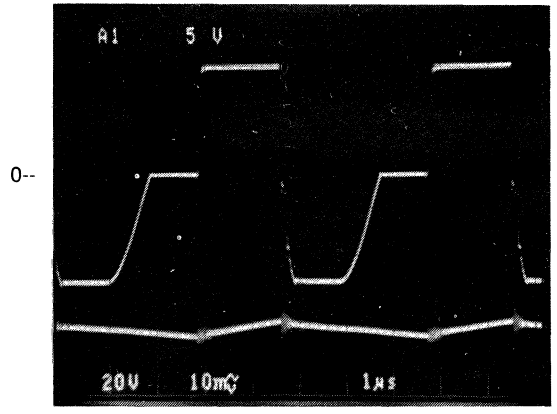
Figure 8. Power switch voltage and current waveforms at full load.



LIGHT LOAD

Top: V_{DS} Q1 100 v/cm
Bottom: Ipri 1 A/cm
Horizontal: 1 µs/cm

Figure 9. Power switch voltage and current waveforms at light load.



SECONDARY

Top: Vsec 20 v/cm
Bottom: Vout (AC) 10 mv/cm
Horizontal: 1 µs/cm

Figure 10. Transformer secondary voltage and power supply output ripple.

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New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors

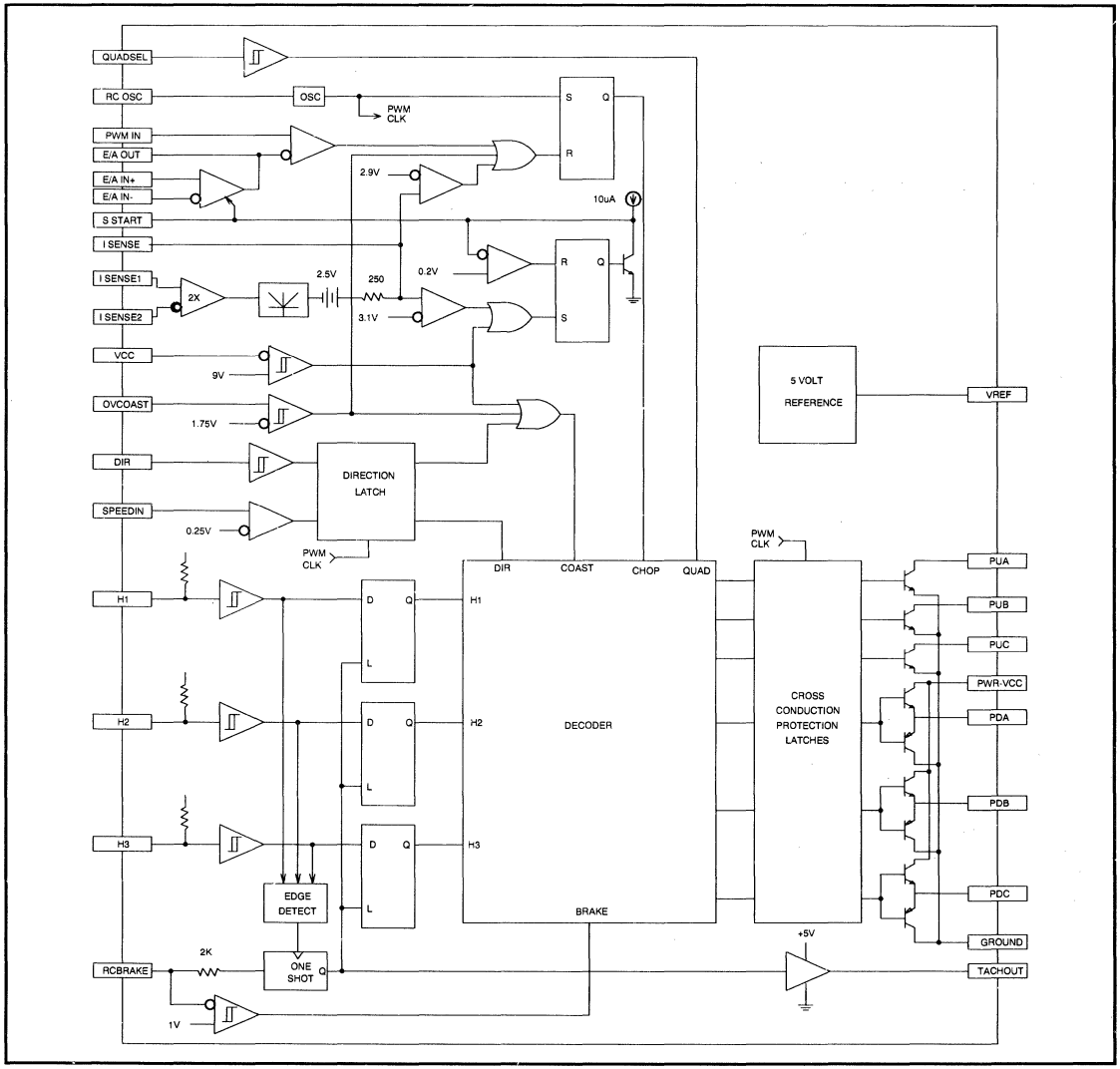
Bob Neidorff, Unitrode Integrated Circuits Corp., Merrimack, NH

Abstract

A new integrated circuit for brushless DC motor control is presented that implements many new techniques to enhance reliability and reduce the detrimental effects of noise. In addition to safety features and noise rejection circuitry, the new circuit contains a complete pulse-width modulator (PWM), a practical tachometer, a precision voltage reference, a high-speed current-sense amplifier, and high-voltage, high power, output stages.

Various applications of the IC are discussed in detail, including using the PWM for fixed frequency and fixed off-time control, driving power MOSFETs, driving bipolar power transistors, and sensing winding current. The IC is shown in applications that allow braking and direction reversal without damage to the motor or the power semiconductors.

BLOCK DIAGRAM OF THE UC3625



The Problem

Conventional brush motors have proven reliable and versatile. They remain popular partly because the pressures to improve haven't been high, and partly because nothing better has been available that is practical. Brushless DC motors (BDCMs) can pack the same horsepower into smaller, lighter boxes. They can also accelerate faster due to inherently lighter rotor construction. Without the friction and arcing of brushes, they are acoustically quieter. As they have permanent magnet rotors, they are faster to manufacture. Permanent magnet rotors also dissipate very little power, so BDCMs have far less heat dissipation problems.

One thing that has held the motor industry back has been the availability of economical control electronics. Recent price trends in power MOSFETs and monolithic motor controllers have reduced these limits. The final hurdle to broad acceptance is assurance of reliability. Brush motors proved their reliability not through design, but instead through over a hundred years of development of rugged brusheS and slip rings.

Two problems with BDCMs today are performance and reliability in the presence of noise. Noise here can refer to externally generated electromagnetic noise, internally generated chopping noise, or inappropriate commands from the operator of the system.

The UC3625 specifically addresses the need for an economical, robust BDCM controller by specifically addressing these failure modes and also by implementing many functions and features desirable in high performance motor systems. The following table outlines some of the important features of the UC3625:

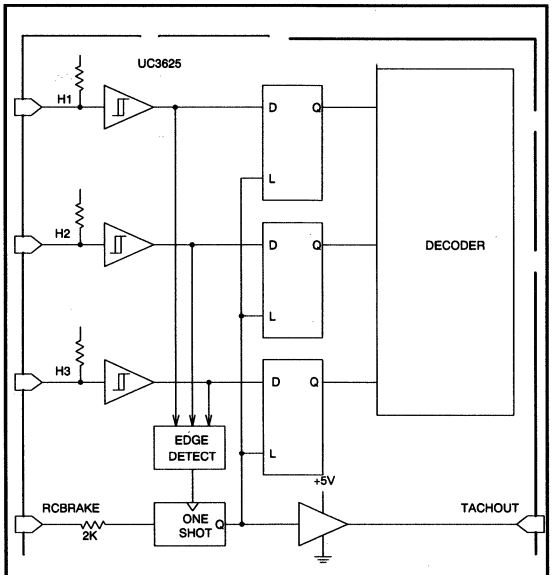
- Push-Pull Low-Side Drivers
- Versatile High-Side Drivers
- Complete PWM
- Two or Four-Quadrant Chopping
- Tachometer
- Soft Start
- Undervoltage Protection
- Overvoltage Protection
- Active Safe Braking
- Differential Current Amp
- Hysteresis on all inputs
- Direction latch
- Cross Conduction prevention

Unique Features For Noise

All logic inputs to the UC3625 have hysteresis and /or latches for maximum noise rejection. The position sensor inputs specifically contain 0.8 volts of hysteresis, yet still meet TTL input thresholds. These inputs also contain pull-up resistors allowing them to directly interface to open-collector sensors.

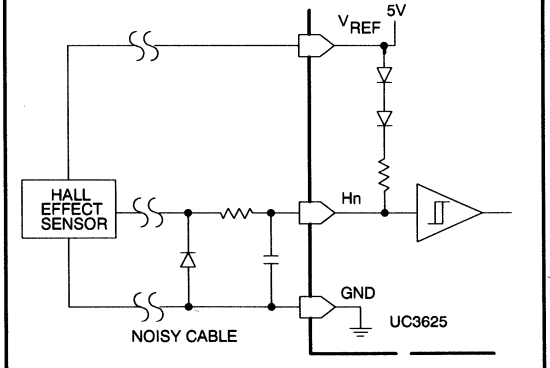
Position sensor inputs are latched immediately following commutation, and remain latched through the on-time of the tachometer monostable (one-shot). This prevents commutation noise from reaching the decoder, latching out the largest noise spike in the motor system. Although this sets a maximum motor speed, correct choice of pulse width guarantees operation up to the maximum speed of the motor while still affording excellent noise rejection.

The one-shot pulse also drives a low saturation-voltage driver connected to TACH OUT. The average value of the voltage on TACH OUT is directly proportional to motor speed, so that the pulse generator doubles as a simple tachometer.



Tachometer Doubles As Input Noise Gate

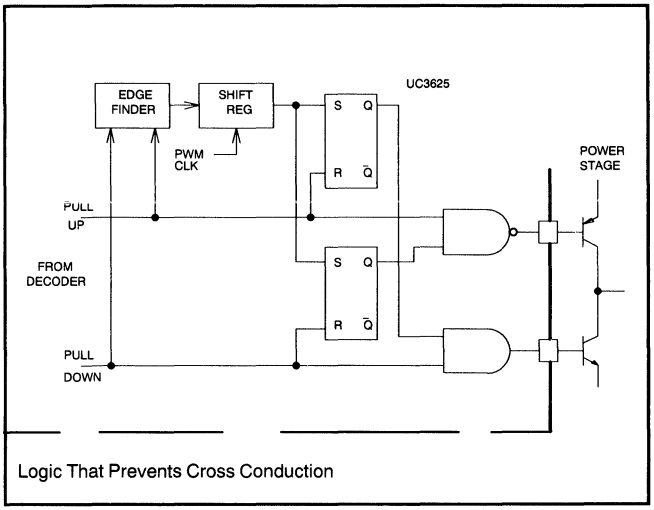
Even with input latches, external noise filtering is often valuable. Chopping noise lends itself to analog low-pass filtering because of its dominant high-frequency components. As high-frequency noise energy can be very strong, zener clamping ahead of the filter can be very effective.



Suggested External Non-Linear Filter For PWM Noise

Cross-Conduction Prevention

To further assure noise immunity, the UC3625 contains latches and a shift register to guarantee that all power stages turn off and remain off for a minimum time before changing states. In addition to preventing noise-induced cross conduction, this prevents cross conduction due to slow power stages.



Logic That Prevents Cross Conduction

The delay time is only inserted when an output is commanded from high to low or vice versa. During normal three phase commutation, outputs are turned off (opened) for a full cycle before changing states, so this delay will not impede normal operation. The only times that this delay will be inserted are during noise spikes, direction reversal, and braking.

Pulse-Width Modulation System

Motors perform better with higher operating voltages because for a given value of inductance, higher voltages can change winding current faster. A necessary adjunct to higher supply voltages is current control, either by linear amplifiers of pulse-width modulation (PWM). The UC3625 uses fixed frequency PWM for chopping.

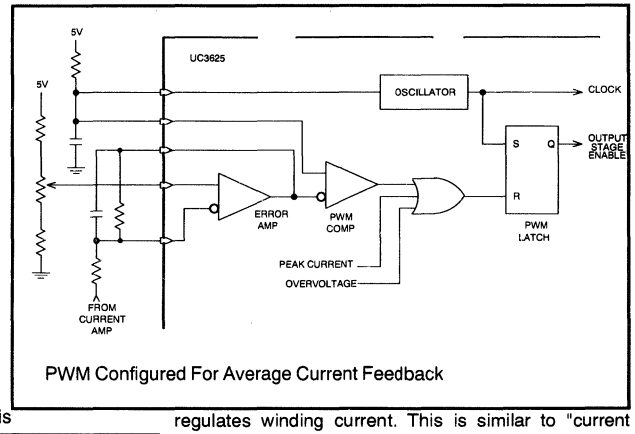
At the heart of the PWM is a sawtooth oscillator. The oscillator is programmed up to 500kHz with one resistor to the reference and one capacitor to the ground. This oscillator is used to enable the PWM latch every cycle, and also to clock the protection shift registers.

Another fundamental part of the PWM is the PWM latch. The output of this latch enables the power stages. The latch is set once per cycle by the oscillator, and cleared by either the PWM comparator, a peak current signal generated in current-sense circuitry, or by a fault signal from the OV/COAST input. This latch is reset dominant, meaning that a steady reset signal from any of three sources completely inhibits the power stages.

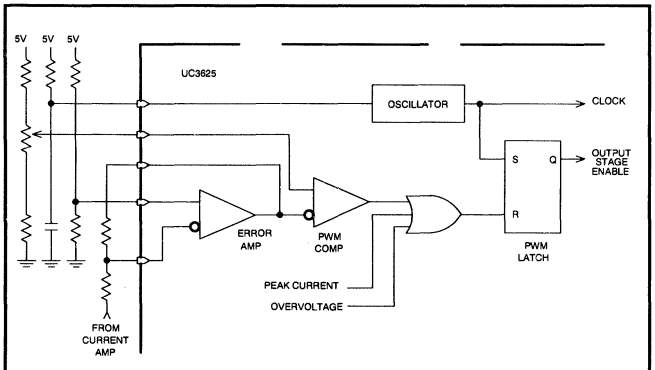
The other elements in the PWM are the PWM comparator and the error amplifier. The PWM comparator is an NPN-input comparator dedicated to comparing the output of the error amplifier to some other signal such as a command voltage, ramp, or sensed signal. The error amplifier is a PNP-input op-amp compensated for unity-gain operation, who's inputs can operate linearly down to ground.

The PWM can be configured into any number of different loops that regulate winding current (torque is nearly proportional to winding current), regulate speed, or regulate some other parameter. The PWM is internally configured for peak current control as well, although this is not intended to be the principle feedback loop.

The approach above compares winding current to a DC voltage with the PWM comparator, and pulse-by-pulse regulates winding current. This is similar to "current mode" in PWM power-supply systems, and offers the advantage of removing the pole caused by load inductance from the feedback loop.



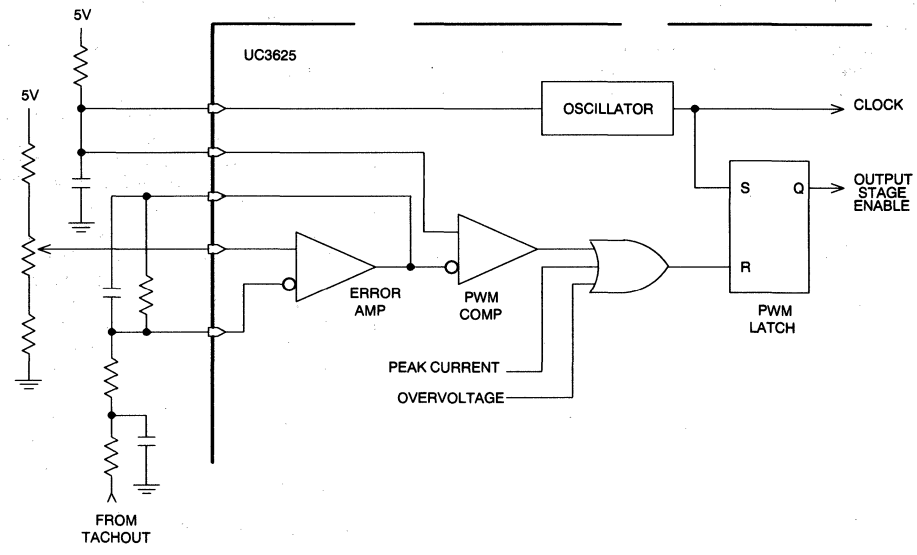
PWM Configured For Average Current Feedback



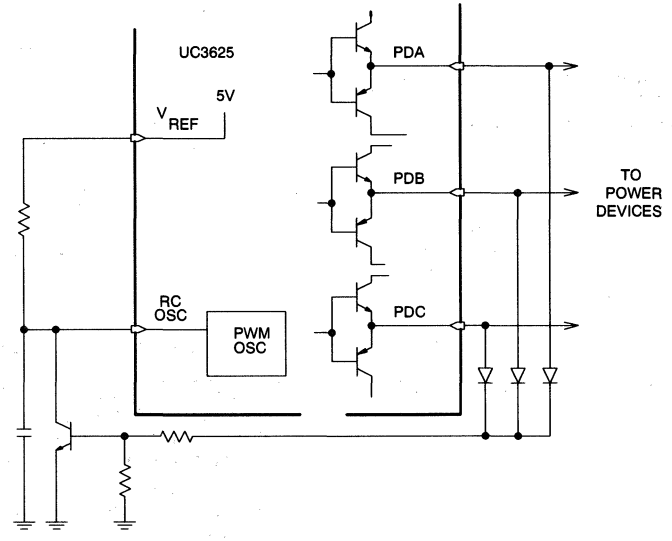
UC3625 PWM Block Diagram Configured For Pulse-By-Pulse Current Control

The PWM can also be configured to use the error amplifier to amplify the difference between the winding current and a desired current, and to use the PWM comparator to compare the error amp output to the oscillator ramp. This current loop operates on average, rather than peak current.

If the PWM comparator is used to compare the oscillator ramp to a DC voltage, then the load duty cycle is directly proportional to the applied DC voltage, as is the average load voltage. This "voltage mode" loop comes close to controlling speed because speed is nearly proportional to average winding voltage. If an overall speed feedback loop is required to regulate speed, this "voltage mode" topology can serve as a local feedback loop to make the system transfer function more linear, and the error amplifier can be used as the overall loop amplifier.



Voltage Mode Speed Control



Circuit For Fixed Off-Time PWM Using the UC3625

The advantages of each topology must be weighed considering complexity, overall stability, and sensitivity to load. In cases where current feedback seems nearly impossible to compensate, some compromise between currrent feedback and voltage feedback is dictated.

The PWM is also configurable to fixed off-time PWM rather than fixed frequency PWM by adding a few external components that couple the output off signal back into the oscillator.

Fixed off-time control is sometimes desirable because it uses one of the easiest feedback loops to compensate. Its main drawback is that the modulation frequency varies with load and speed. This means that for some loads chopping noise can become audible (below 20kHz). This also allows variation in the dead time inserted to prevent output stage cross conduction.

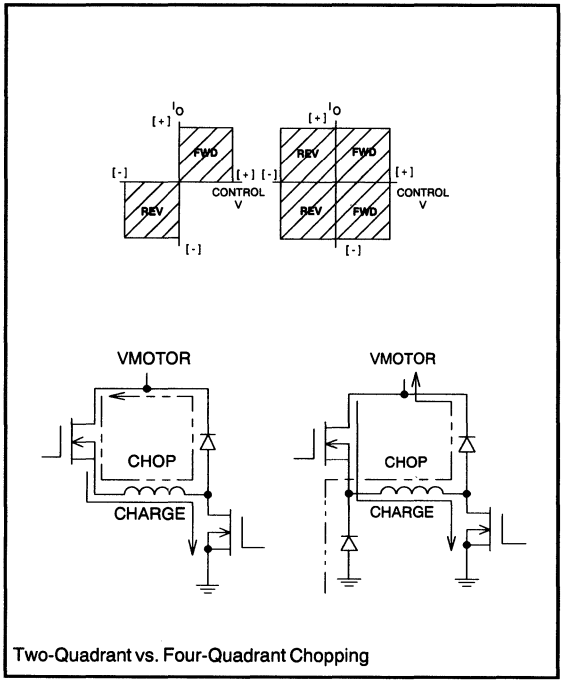
Different Chopping Techniques

Chopping capitalizes on the inductance of the load to maintain load current when the driving voltage is removed. The driving voltage is normally supplied through power switches, and diodes normally conduct across the load when the switches are opened.

Two different methods are common for chopping. The more efficient method chops one low-side power switch while one high-side switch is on. This is referred to as a two-quadrant PWM.

Two-quadrant PWM normally operates with a low duty cycle, as winding current is charged principally by the supply voltage, yet winding inductance is discharged by the voltage drop in the diode circuit (see figure below). Motor back EMF reduces the effective supply voltage and increases the effective diode voltage drop, so the duty cycle tends to increase with speed.

The main advantage of two-quadrant chopping is efficiency. Its main drawback is that it can't quickly decrease winding current. This can be very troublesome in position feedback systems.



Two-Quadrant vs. Four-Quadrant Chopping

In contrast, four-quadrant PWM systems chop both switches, and circulate load current through two diodes backwards into the supply.

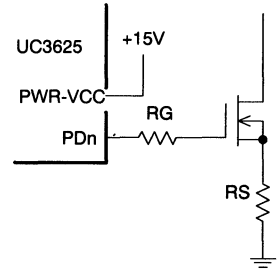
Again ignoring back EMF, four-quadrant chopping produces a nearly symmetrical current waveform, as current rises due to the supply voltage impressed on the load inductance, and decays due to reverse supply and load inductance. With four-quadrant chopping, a motor can decelerate as quickly as it can accelerate.

To program the UC3625 for one approach or the other, apply a logic signal to the QUAD SEL input. QUAD SEL can also be changed during operation to tailor performance to specific requirements.

Power Drivers

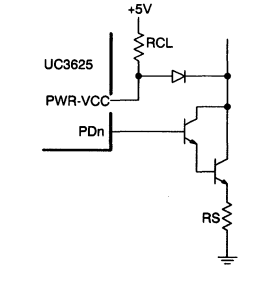
The overwhelmingly dominant power output device in new designs is the N-Channel Enhancement-Mode Power MOSFET. Bipolar power transistors and power darlingtons still have advantages in very high-voltage systems, but these advantages are being continuously eroded by developments in MOSFET structures and merged bipolar MOSFET devices. The UC3625 is able to drive both power MOSFETs and bipolar transistors.

The low-side drivers in the UC3625 are totem-poles capable of greater than 250mA peak gate or base current, but the package and the die are not constructed for continuous power dissipation greater than 1 watt, which imposes an upper limit on the available current for bipolar device drive.



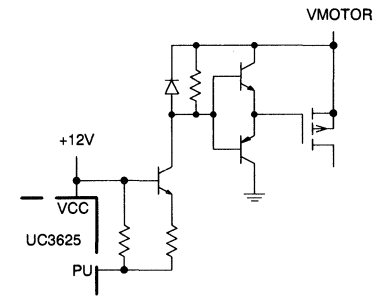
Driving Low-Side MOSFETs with the UC3625

The Power Vcc pin is separated from signal Vcc so that high gate current peaks can be isolated from signal Vcc, and also so that Power Vcc can be tailored to the power device. For fastest switching of power bipolar devices, the Power Vcc pin can be limited and clamped, as shown in this example.

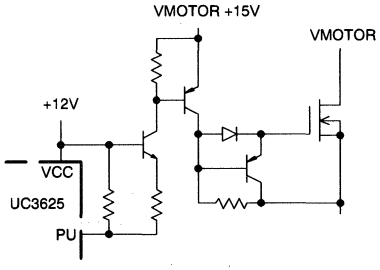


Driving Low-Side Darlingtons with the UC3625

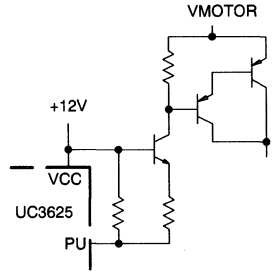
Driving high-side devices with the UC3625 requires level shifting if the motor supply is greater than 50V. The UC3625 high-side outputs are open collector NPN transistors which pull low to turn on high-side MOSFETs or bipolar transistors.



Driving High-Side P-MOSFETs



Driving High-Side N-MOSFETs



Driving High-Side PNP Darlingtons with the UC3625

Although capable of 50mA current sinking, the open collector outputs are normally operated with lower currents to minimize the power supplied by the high-voltage supply.

As a high-side switch, P-channel power MOSFETs are far easier to drive than N-Channel power MOSFETs because the gate of P-channel MOSFETS need not be pulled above the positive supply to obtain low voltage drop. Unfortunately, P-channel power MOSFETs are more expensive and less available than N-channel devices, so the added supply in the N-channel design is often justified.

Current Sense

The UC3625 contains a high-speed gain-of-two differential amplifier dedicated to current sensing. This amplifier can be connected directly across a low-value current-sense resistor or between two different current-sense resistors. Since the amplifier common mode range allows operation one volt below ground, the amplifier has excellent common-mode noise rejection.

The current-sense amplifier also embodies an ideal diode that performs absolute value and level shifting of the input, giving a transfer function of:

$$Vo = 2.5 + 2\ ABS\ (Vi_2 - Vi_1)$$

If the low-side power devices and the lower catch diodes are returned to the same current-sense resistor, and the UC3625 is chopping in four-quadrant mode, then the winding current always flows through the current-sense resistor. The voltage on the current-sense resistor flips polarity every time the PWM chops, but the absolute value current-sense amplifier rectifies this, giving a smoother representation of continuous winding current, and requiring less filtering.

Some filtering of the current-sense signal is always required, however, and the output of the current-sense amplifier is the best place to filter. The amplifier is stable with all capacitive loads, and has approximately 250 ohms output impedance.

Filtering at the input of the current-sense amplifier is also valuable to remove spikes that are faster than the amplifier can track. However, to insure that the absolute value circuit continuously tracks current, use only a minimal amount of input filtering.

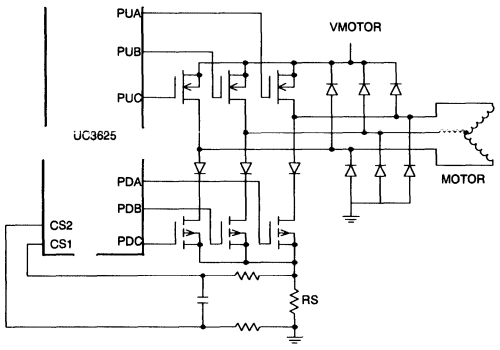
The output of the current amplifier drives two comparators through the filtering resistor: the peak current comparator and the overcurrent comparator. The peak current comparator resets the PWM latch whenever the current-sense voltage exceeds approximately 200mV. The overcurrent comparator initiates soft start if the current-sense voltage exceeds approximately 300mV.

The peak current comparator can be used to limit maximum peak winding current while a larger feedback loop limits winding current to control some other parameter, such as speed or position. The overcurrent comparator then functions as a fail-safe device that commands SOFT START if the peak current loop loses control, as might happen if a power device becomes shorted.

Is it Brake...or Break?

The UC3625 contains provisions for braking by way of a multifunction pin called "RC / BRAKE". This pin also serves as the timing pin for the internal tachometer, pulsing between 1.67V and 3.33V every time the position sensors commutate. To command BRAKE, pull RC/BRAKE low with an open collector gate or switch. The tachometer then stops pulsing and all three low-side drivers turn on.

Normal PWM configurations do not allow braking current to be modulated because the braking current does not normally flow through the sense resistor. The motor control circuit below includes three added diodes that, during BRAKE and all other circumstances causes winding current to flow through the sense resistor. Using this circuit, the UC3625 stops a motor as fast as the peak limit current setting allows and protects the output power devices and the motor.



Circuit For Safe Braking Series diodes guarantee that braking current will flow in the current-sense resistor

Direction Reversal is Worse

As with braking, direction reversal can also force excessive current into power devices if not checked. Direction reversal forces two of the three driver channels to go from high to low or low to high directly. With the UC3625, cross conduction is completely prevented, but high winding current is dependent upon the application. The higher the speed, the higher back EMF, and the higher the potential peak current.

The approach mentioned for braking also limits peak winding current during direction reversal. In addition, the direction latch and shift register in the UC3625 can be configured to prevent direction reversal until motor speed drops to a safe level. This latch also commands COAST whenever a direction reversal is commanded and motor speed is too high.

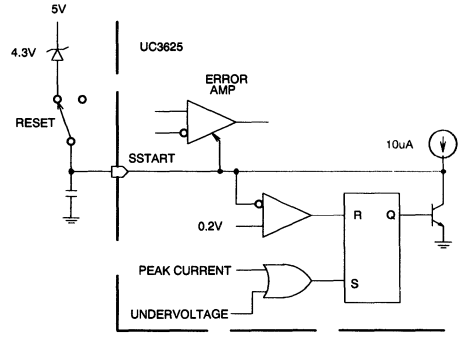
The easiest way to configure this protection is using the internal tachometer to drive "SPEED IN" through a low-pass RC filter. The "SPEED IN" threshold is set to prevent reversal whenever input voltage exceeds approximately 250mV.

Other Protection Features

To prevent confusion or insufficient drive to power MOSFETs, the UC3625 contains a comparator to lock off all six outputs until the Vcc input exceeds 9V, called under-voltage lock-out. The UC3625 also contains an uncommitted comparator that inhibits the outputs and clears the PWM latch whenever its input exceeds 1.75V. This can be used with a voltage divider for an over-voltage inhibit, or can be directly driven from TTL or CMOS for a logic controlled COAST input.

To prevent very high power supply current spikes and to limit average current during faults, the UC3625 contains latched soft start. The latch is set by low power-supply voltage or overcurrent fault, and is only cleared when the setting condition goes away and the soft start input discharges to below approximately 200mV.

Normally, the UC3625 is configured with a capacitor from soft start to ground, which is charged by the soft start 10uA current source. The UC3625 can also be configured to latch soft start until cleared by connecting a 4.3 volt zener and a normallly closed switch from Vref to soft start. The switch then functions as a reset switch.



Manual Fault Reset Circuit Uses Zener Diode to Latch Faults

Voltage Reference

Finally, the UC3625 contains a precision voltage reference trimmed to 5V +/- 2%. This reference powers most of the internal circuitry for supply rejection and is available on the "Vref" pin for driving other circuitry such as Hall-effect position sensors and bias circuits. Operation of the voltage reference is guaranteed with loads up to 30mA, and the reference is also short circuit current limited to approximately 100mA.

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A NEW LINEAR REGULATOR FEATURES SWITCH MODE OVERCURRENT PROTECTION

Robert Mammano and Jonathan Radovsky, Unitrode IC Corp; and
George Harlan, Power General

ABSTRACT

This paper presents a new linear control circuit which, in addition to offering benefits such as low input-out-put differential and a precise reference voltage, features a unique and innovative approach to overload protection. By using duty-ratio, switch-mode protection, this circuit eliminates both the high internal dissipation of constant current limiting and the latch-up tendencies of limiting with current foldback.

THE CURRENT LIMIT PROBLEM

As an opening statement, let us offer as a "given" that all linear power supplies need some form of over-current protection. Traditionally, this protection consists of configuring supply to control current - rather than output voltage - once an established threshold of maximum current has been exceeded. The method of current control can usually be classified as either "constant-current" or "current-foldback" current limiting and, while simple to classify, choosing between these two methods is often less than satisfying.

The protective method most acceptable to the user is constant current limiting with a characteristic as shown in Figure 1. With the knowledge that a power supply will only deliver a maximum current regardless of what he might do to it, the user's job of scaling his cables, switches, connectors, and other components associated with the power inputs to his system is greatly eased. He knows that no matter how non-linear his load may be, he can count on a regulated voltage whenever his current drain is within the supply's rating. Further, he knows that the maximum rated current is always available to meet any demand asked of the supply.

The "benefits" of constant current limiting are another matter to the power supply designer, however. For example, a regulator designed to deliver 12 Volts at a maximum load current of 5 Amps, would probably start with a bulk input voltage of approximately 15 Volts and a constant current limit of 5.5 Amps. Under maximum rated load, the internal dissipation of the regulator is 3V x 5A or 15 watts but with a short to ground, this dissipation jumps to 15V x 5.5A or more than 80 Watts! This means that the thermal management and heat sinking must be sized for the short circuit condition resulting in a massive overkill in terms of volume, complexity, and cost with respect to normal operating conditions.

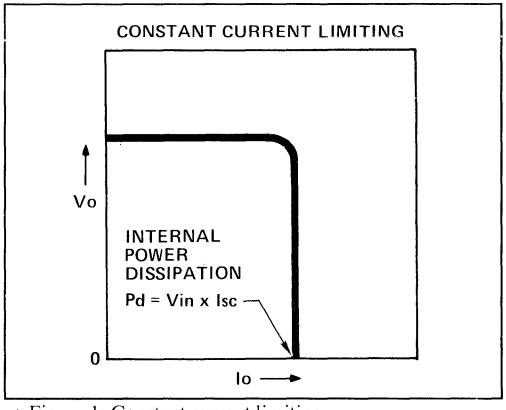

Figure 1: Constant current limiting.

A common solution to this problem is to design a current limiting scheme as illustrated in Figure 2. Here the protection is actuated at 5.5 Amps when the output voltage is at 12 Volts but the allowable current then "folds back" as the output voltage falls due to increasing overload, until it reaches some much lower value - say one Amp in this example - with a shortened output. Now the dissipation with a short circuit is close to the same as it was with rated current and our designer's thermal problems are solved.

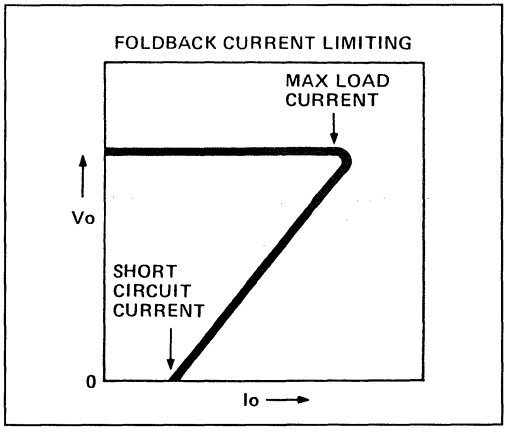

Figure 2: Foldback current limiiting

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But what about his customer? His load may be complex, non-linear, and often not even well understood. Figure 3 shows typical load characteristics for digital and analog circuitry but an actual system may include all of these plus motors which need to be started and capacitors which need to be charged. Any protection scheme which allows the static load line to intersect the foldback current curve as shown in Figure 4 is potentially subject to latch up because the load draws more current than the regulator can supply at the voltage where the curves cross.

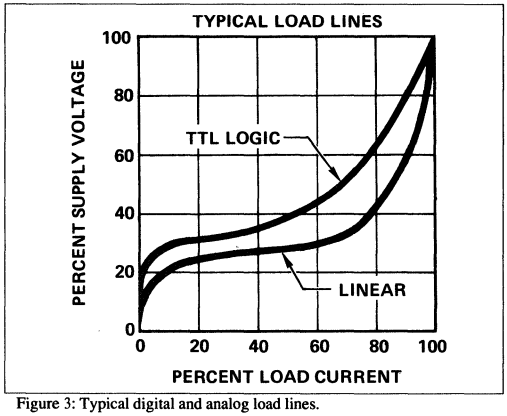


Figure 3: Typical digital and analog load lines.

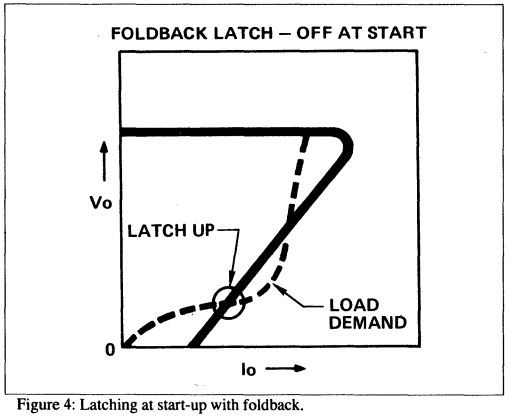


Figure 4: Latching at start-up with foldback.

An application particularly susceptible to latch up due to foldback current limiting occurs when two supplies are used to provide positive and negative voltages to a load where there is a path for "rail-to-rail" loading. As the regulators turn on, their output capacitors are charged at rates determined by the values of the capacitors and the amount of current each regulator can provide as its output rises up the foldback curve. Since these curves are unlikely to be perfectly matched, one output will dominate the other. As the faster one's output voltage increases, it provides more current through the common load. This forces the slower one back down the foldback curve where it provides less current, compounding the problem and ultimately latching when its output is driven past zero to a reversed polarity. Thus a foldback-limited regulator, which might be stable when used by itself, may latch when used as one-half of a dual-polarity system due to this "turn-on slew rate" phenomenon.

So what we have concluded is that while the power supply designer needs to incorporate foldback current limiting to reduce power dissipation, his customer needs constant-current limiting to insure reliable starting. It is the contention of this paper that what they both really need is duty-ratio protection.

DUTY-RATIO OVERCURRENT PROTECTION

Duty-ratio protection can be simply described as a constant current limiting regulator with a timer. The timer's function is to turn the regulator's power stage OFF and ON with an established duty cycle ratio such that the high internal power dissipation of constant current limiting is reduced by the duty ratio to a much more manageable average value.

Referring back to our earlier example of a 12V, 5A regulator, consider setting the constant current limit at 5.5 amps but additionally establish a duty ratio for the timer at 1 to 20 for "ON" to "OFF". If we set the "ON" time sufficiently long to charge whatever capacitance might be on the output, the regulator will power up with the constant current characteristic, insuring start-up regardless of the loading. In the event of an overload or short circuit (defined in this device as remaining in current limiting for a period of approximately 2 x Ton), the regulator will periodically shut down for a time equal to 20 x Ton and then continue to cycle in a 1 to 20 duty cycle until the fault is removed. Although the peak power during Ton might be 80 Watts, the average fault dissipation at this duty ratio is only 4 Watts - less than the normal 15 watt operating power loss, and we have thereby satisfied both the designer and his customer.

INTRODUCING THE UC1833 / UC3833

The block diagram of this new linear regulator control IC is shown in Figure 5. This circuit can be used in many different ways but its primary intent is as a high-efficiency regulator implemented with an external PNP pass transistor as shown in the figure. The circuitry in the right half of the UC1833 block generates the voltage error signal used to activate an NPN Darlington driver which, in turn, drives the base of the PNP pass device. This common-emitter pass transistor configuration allows this type of regulator to operate with a minimum input-output differential of well less than one Volt, even at high loads.

Duty-cycle current limiting is accomplished with the circuitry on the left half of the block diagram, where an Amplifier and a Comparator are seen, both monitoring the voltage drop across a single current sense resistor. The Comparator has an input threshold of 100 mV and, when activated, initiates a timer to alternately clamp and release the base of the driver to ground thereby switching the output of the regulator from Vout to Zero with a low duty ratio.

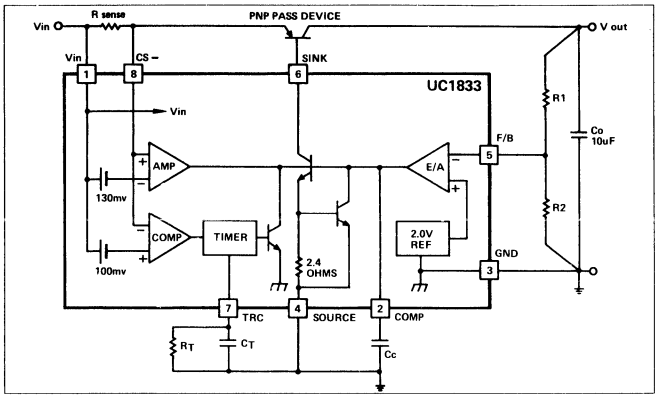


Figure 5: The new UC1833 / UC3833 linear regulator.

The Amplifier part of the current sense circuitry has an input threshold of 130 mV and overrides the output of the Error Amplifier to control the driver - when enabled by the ON-time of the timer - to regulate the supply's output current to a maximum amount determined by 130 mV divided by the value of the sense resistor. The 30 mV differential between the thresholds of the Amplifier and Comparator insures that current limiting can never occur without prior initiation of the timer.

OVERLOAD PROTECTION CIRCUITRY

The operation of the overload protection circuitry can be better understood by referring to the simplified schematic of Figure 6.

The current sensing portion of this circuit is to the left of this figure where the current-sense Comparator and Amplifier are shown sharing the same input sense pins. Note that their offset voltages are derived by a constant current through R1 and R2 in series rather than independently as shown in the more simplified earlier block diagram. By adding 30 mV to the 100 mV offset of the Comparator, the Amplifier's offset will more accurately track that of the Comparator should any variations occur, and the criteria to have the Comparator always activate first is assured.

A characteristic important to current protection is the accuracy of its threshold as any tolerance represents a window of undefined operation which works to the disadvantage of both designer and user of the power supply. Recognizing this, the UC1833's thresholds are derived from its precision reference resulting in a Timer activation threshold guaranteed to 5 percent over all operating conditions.

The output of the Current Amplifier connects into the output stage of the Error Amplifier where it can easily take command when activated. The compensation capacitor must compensate both the voltage and current feedback loops, and since the current loop must override the voltage control, its gain will be higher making the current loop the more difficult to stabilize. To evaluate the current loop, grounding the Timing pin will disable the Timer and allow continuous constant current operation. This can be useful either as a temporary measure while designing the current compensation network, or permanently to implement a constant-current limited power supply.

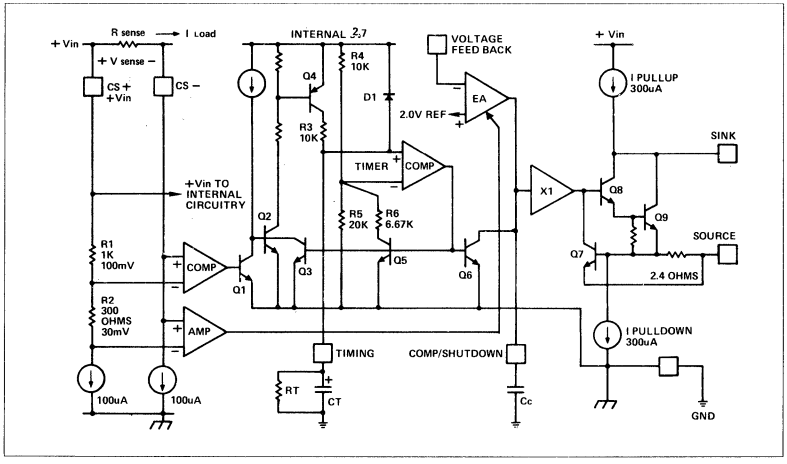


Figure 6: A simplified schematic of the UC1833 control circuitry.

The Current Sense Comparator is phased such that its activation turns off Q1 which turns on Q2 and Q4 to start the timing cycle. The timer is a gated astable relaxation oscillator with ON and OFF times independently programmed using an external resistor and capacitor, RT and CT. The external components work in conjunction with an internally switched 10k timing resistor shown in the schematic as R3. With RT much greater than 10k, the ON time is defined by R3 and CT, while RT and CT determine the OFF time. The thresholds for the Timing Comparator are set at 1/3 and 2/3 of the internally regulated 2.7Vsource by the values of R4, R5, and R6.

Timing waveforms during an overload cycle are shown in Figure 7 where the upper graph shows the output current from the regulator, the center one plots the voltage on the timing components, and the regulator's output voltage is shown in the lower graph. Following the sequence of events as drawn in the figure, when the load current ramps up and crosses the 100 mV Comparator threshold, the initial ON time begins. This initial period is about twice the duration of successive ON-times as the timing capacitor starts its charge from zero initially, while subsequent ramps begin from the lower Comparator threshold. While the timing capacitor is charging, the regulator current is limited by the action of the Current-sense Amplifier to maintain a level of 130 mV across the sense resistor. While in current limiting, the regulator's output voltage falls to whatever value that current will allow across the faulted load impedance.

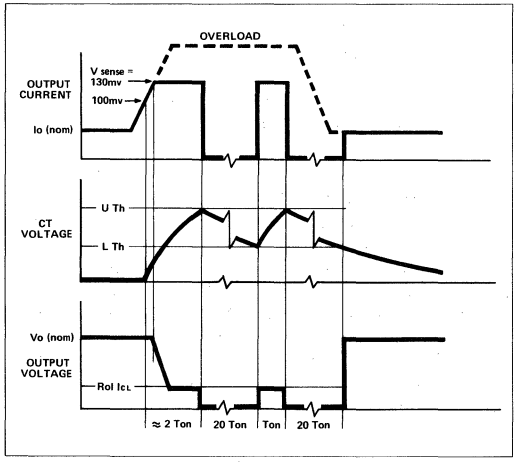


Figure 7: Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.

The ON-time continues until the internal 10k resistor charges the timing capacitor to the upper Timer threshold. At this point, both the ON-time of the regulator and the charging of the timing capacitor are terminated, and the capacitor now discharges through RT, while the regulator is held OFF until the voltage on CT reaches the lower threshold, at which point the cycle repeats. If the load fault is removed during an ON-time, the Timer is immeadiatly disabled allowing the regulator to recover and the timing capacitor to discharge back to zero. If the fault is removed during an OFF-time, the Timer must complete that cycle of capacitor discharge before allowing the regulator to turn back on. In special applications requiring an extended ON-time, the correspondingly long recovery may be accelerated by interrupting the input voltage, as the falling internal 5 V source will discharge CT through D1 and an equivalent 1k impedance.

Duty-ratio protection has greatly eased the problem of heat sinking created with a constant-current solution since the area of the heat sink, or its thermal resistance, need only remove the average power as reduced by the duty ratio. Heat sinks for the internal power devices must now only have adequate thermal mass to absorb the high peak power of the initial ON period.

REMAINING CONTROL CIRCUITRY

Other blocks within the UC1833 include a 2.0 Volt band-gap reference internally trimmed to 1% and a low input-offset Operational Transconductance Amplifier (OTA) to serve as the error sensing and amplifying circuitry. The OTA Error Amplifier has a gm of about 4 millimho and an output current capability of +/- 300 uA. This form of amplifier can usually be compensated with a simple network - often a single capacitor - from its output to ground; but more commonly, an R-C pole-zero pair is also added to compensate for an external PNP pass transistor's gain characteristics.

The Error Amplifier is followed by a unity-gain Buffer Amplifier which controls the Driver Stage consisting of a Darlington transistor pair with local current limiting. This Driver can either source or sink current, allowing its use as a driver for either NPN or PNP pass transistors. The Pullup and Pulldown current-sources shown at the Sink and Source terminals of Figure 6 are to provide turn-off bias to the pass transistor during duty-ratio switching so that it is not turned off into a BV_{CEO} condition.

Not shown on the schematic are two additional forms of protection built into the UC1833: Thermal Shutdown (TSD), and Under Voltage Lockout (UVLO). While it could be argued that thermal protection on the control chip does nothing to protect the pass transistor, the fact that the Driver can conduct up to at least 100 mA with a large portion of the input supply voltage across it, can result in more than acceptable internal heating of the UC1833. A good practice, when voltage levels permit, is the addition of an external resistor in series with either the Source or Sink outputs of the Driver to remove some of the voltage - and therefore some of the dissipation - from the controller.

Under Voltage Lockout keeps the Error Amplifier output low until the supply voltage reaches approximately 4 Volts insuring that all internal circuits - particularly current limiting functions - are intelligent before allowing the pass transistor to turn on. The UVLO function also disables the Pullup current feeding into the Sink terminal, for low input voltages, so that the pass transistor cannot be driven in the reverse direction should the input supply fall with a charged capacitor or other energy source on the output. The Source Pulldown current source is also disabled with UVLO but this terminal also has a two-diode path from the Source to the Compensation terminals. This is to allow any shutdown function which pulls the Comp pin low to discharge capacitance at the regulator's output without reverse-biasing the Driver's emitter-base junction.

THE UC1832 14-PIN CONTROLLER

An important objective in the design of the UC1833 was that in addition to providing significant operating benefits over the omnipresent uA723, the resulting product should be cost-competitive with that device. Committing the UC1833 to an 8-pin

Minidip package allows the potential for meeting the cost objective (plus the benefit of less PC board area), but in several important ways, also restricts the device's versatility. Recognizing this fact led to the introduction of the same chip in a 14-pin package with a UC1832 designation. The block diagram of this device, in a uA723-type application, is shown in Figure 8.

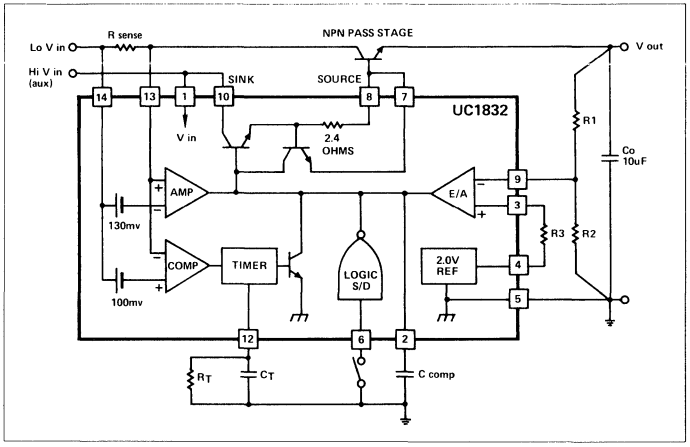


Figure 8: A 14-pin version, designated UC1832 / UC3832, offers enhanced versatility.

The characteristics of the UC1832 include all the performance features of the UC1833 plus the following:

1. Separating the +Vin line from the CS+ terminal so that the controller could be supplied from a higher potential, low-current, auxiliary voltage while sensing current from the main supply.

2. Separating the Reference from the Error Amplifier (+) input and making both accessible to the user. Among other things, this allows phase reversal, an external or divided-down reference, and a convenient access point for soft-start.

3. Providing a separate input to the Driver's local current limiter allows considerable flexibility in setting that limit either higher or lower than the 300 mA (typical) defined by the internal 2.4 ohm resistor.

4. A separate logic-level digital shutdown function has been added to give more programming options such as accepting a shutdown command from an over-voltage sensor or implementing a turn-on delay. This input is fail-safe as it must be pulled low to allow the regulator to turn on.

TYPICAL CIRCUIT APPLICATIONS

Unitrode's Power General Division has already utilized the UC3833 (the commercial version of the UC1833) in several successful power supply designs. A brief description of some of these products will illustrate both the range of applications and the simplicity which this new device brings to power supply design.

The circuit of Figure 9 shows one of the simplest applications of the UC3833 repeated twice to implement a dual-polarity 12 volt, 200 mA supply. The timing components for duty-ratio protection are determined from the following equations:

$$Ton = .69 \times 10k \times CT$$

$$Toff = .69 \times RT \times CT$$

$$\text{Duty-ratio} = Ton/(Ton+Toff)$$
$$= 10k/(10k + RT)$$

The values shown provide approximately 7 mS ON time and 140 mS OFF. These fairly rapid time constants minimize the need for any significant thermal mass in the heat sinks and also allow fast recovery after an overload is removed. With the knowledge that the initial conducting time can be twice the ON time, the maximum output capacitance can be calculated from:

$$C = Imax\ (dt/dV)$$

$$C = 130mV/.5ohm\ (\ 14mS/12V\ ) = 300\ uF.$$

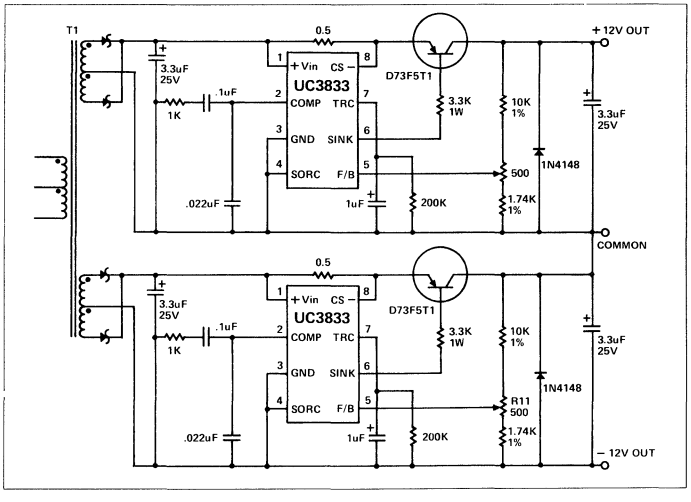


Figure 9: A +/-12V, 200mA regulator is easily implemented with two UC3833 devices.

9

A higher power application is shown in the schematic of Figure 10 which was designed to supply 5 Volts at 5 Amps. The UC3833, configured as shown, will meet this requirement with an input voltage as low as 6 Volts due to the low saturation voltage of the paralleled 2N6489 transistors and the fact that the maximum non-fault voltage on the sense resistor is less than 100 mV. Actually, a little more sense voltage was sacrificed in the interests of selecting a standard resistor value, with the excess divided down by the 56/100 ohm divider. The additional BD438 drive transistor was added to boost the UC3833 drive current and keep the internal power dissipation low.

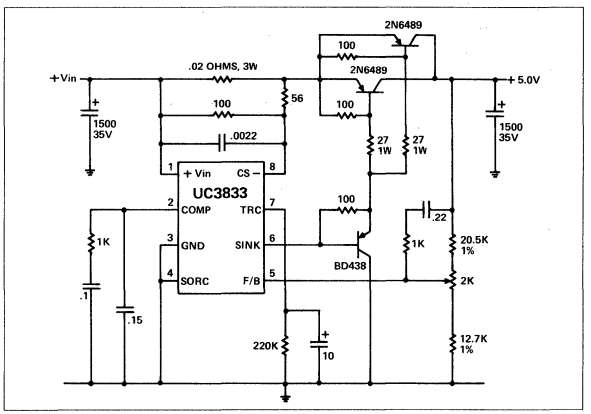


Figure 10: A high-efficiency configuration with added current boost will deliver 5V at 5A from a 6V source.

A third application of the UC3833 is one which took particular benefit from duty-cycle current limiting. This was for a disk drive power supply which required considerable current at turn-on to accelerate the disk. The circuit schematic is the same as that shown in Figure 10 with the voltage sense resistors selected for a 12 Volt output. The power requirements dictated a peak start current of 5 Amps decaying to 3 Amps in 30 seconds as the motor reached operating velocity. The current sense resistor was chosen to give a Timer initiation at 4.75 A and a constant current limit of 6.1 Amps. The timing capacitor value was set at 3300 uF yielding an ON-time of approximately 20 seconds, with 40 seconds for the initial turn on period - during which time the motor current will decrease to less than the lower threshold. With a duty-ratio of 20:1, when a fault does occur, the OFF-time will now be greater than 6 minutes, but, if this is excessive, recycling the input voltage to the regulator will reset the timing capacitor.

CONCLUSION

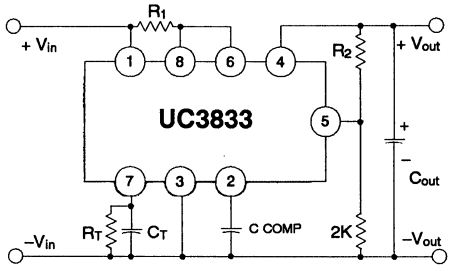
While no one can deny the long-term success of the uA723 as a general-purpose linear regulator controller, there has also long been a call for a device to improve its many limitations. While other products have been marketed offering some parametric improvements, the UC1833 - and its companion UC1832 - are the first to offer an innovative solution to a very basic problem. By combining switch-mode protection with linear regulation, these devices answer the question of which form of protection is best for whom, with a solution that is best for everyone.

UC3833 Typical Applications

See appendix for component selection

LOW CURRENT APPLICATION

using the UC3833 internal drive transistor



TYPICAL OUTPUT CURRENT vs. V_{in} and V_{out}

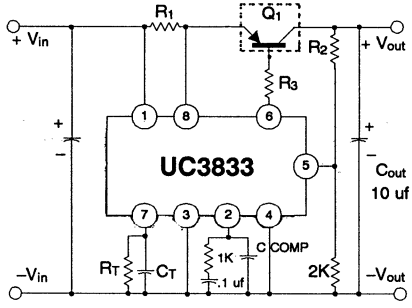
of the UC3833 internal drive transistor
for P_{diss} = 0.5 W (approx.)

		Vin					
	Volts	5	9	12	15	18	24
Vout	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

Fig. 3

LINEAR REGULATOR

using an external power transistor
as a series regulator



P CHANNEL POWER MOSFETs

can also be used as the series pass transistor Q_1

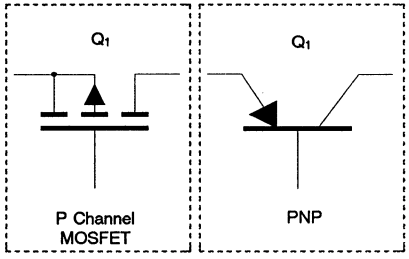
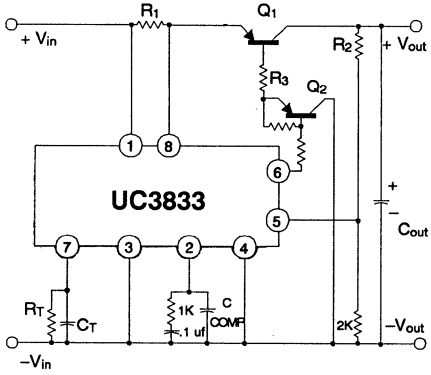


Fig. 4

HIGH CURRENT REGULATOR

using drive transistor Q_2 to increase Q_1 base drive
and reduce UC3833 power dissipation



PARALLEL PASS TRANSISTORS

can be added for high current
or high power dissipation applications

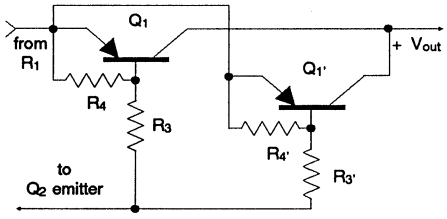


Fig.5

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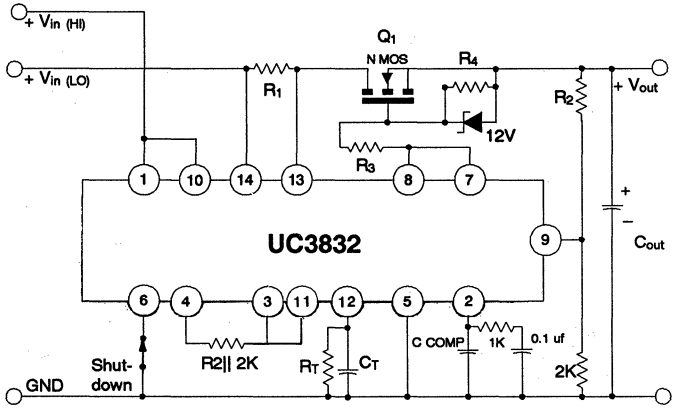
UC3832 Applications

See appendix for component selection

LOW DROPOUT REGULATOR

The UC3832 features a seperate supply input for operation from an auxiliary power source. Useful in low dropout applications.

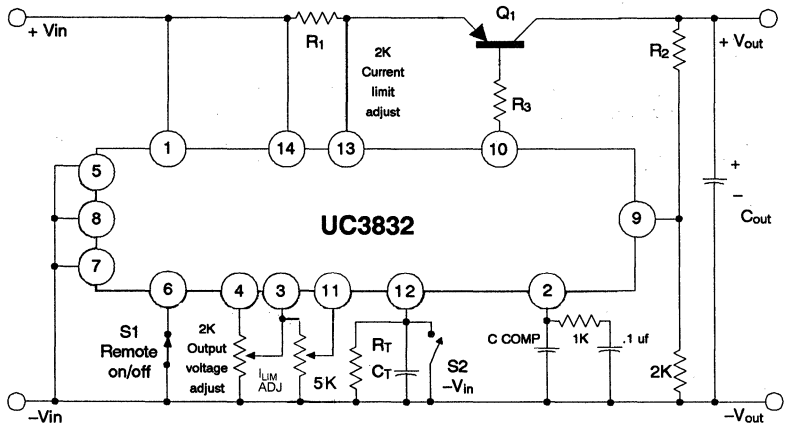


S1 - Closed: Normal operation
Open: Output disable

Fig. 6

PRECISION LABORATORY POWER SUPPLY

featuring adjustable voltage and current limiting



S1 - Closed: Normal operation
Open: Output disable

S2 - Open: Duty ratio current limit
Closed: Constant current output or I_{MAX} adjust.

Fig. 7

APPENDIX

Design Equations and Component Selection

R_1 - Current Sense Resistor

R1 = 0.135 V/I_{OUT} (max) UC1833 AND 1832 WITH V_{ADJ} = 2.5V

LOW CURRENT	
I_{OUT} mA	R_1 ohms
10	13
20	6.5
30	4.3
40	3.3
50	2.7
60	2.2
70	1.8
80	1.6
90	1.5

GENERAL USE	
I_{OUT} A	R_1 ohms
0.10	1.30
0.25	0.52
0.50	0.27
0.75	0.17
1.0	0.13
2.0	0.065
3.0	0.043
4.0	0.032
5.0	0.026

HIGH CURRENT	
I_{OUT} A	R_1 mohm
5	26
6	21
7	18
8	16
9	14
10	13
15	8.6
20	6.5
25	5.2

R_2 - Output Voltage Divider Resistor

$R_2 = (V_{OUT} - 2.0V)/1mA$

FIXED	
V_{OUT}	R_2
5.0	3.0K
9.0	7.0K
12.0	10K
15.0	13K
18.0	16K
24.0	22K

ADJUSTABLE	
$V_{OUT(MAX)}$	R_2
7.0	5K POT
12	10K POT
22	20K POT

R_3 - Drive Current Limit Resistor

$R_3 = ((V_{in} - V_{BE} - V_{sat}) * \text{Beta (min)})/I_{OUT}$ (max)

I_{OUT}	V_{in}		
A	9V	15V	24V
0.10	1.8K	3.2K	5.6K
0.25	680	1.2K	2.2K
0.50	330	650	1.1K
0.75	220	430	750
1.0	180	330	560
2.0	82	160	270
3.0	57	100	180
4.0	43	82	120

I_{OUT}	V_{in}		
A	9V	15V	24V
1.0	200	350	560
2.0	100	175	270
4.0	50	87	140
5.0	40	70	110
7.5	27	47	75
10.0	20	35	57
15.0	13	24	38
20.0	10	17	27

For circuit diagram of Fig. 4,
Beta (min) = 25, V_{BE} = 0.7V, V_{SAT} = 1.5V

For circuit diagram of Fig. 5,
Beta (min) = 25, V_{BE} = 0.7V,
$V_{SAT} \approx V_{BE}(Q_2) + V_{SAT}$ (UC3833) $\approx$ 1.5V

9

R_T and C_T - Timer Duty Duration and Ratio Resistor and Capacitor

$T_{on} = 0.693 * 10K * C_T$

$T_{off} = 0.693 * R_T * C_T$

Duty Ratio = $T_{on}/(T_{on} + T_{off}) = 10K/(10K + R_T)$

NOTE: Typical duty ratios are between 0.5% and 5%

Duty Ratio	R_T ohms
5%	180K
4%	240K
3%	330K
2%	470K
1%	1 MEG
0.5%	2 MEG

T_{on} msec	C_T* uf
1	0.15
2	0.30
5	0.68
10	0.15
20	3.0
50	6.8
75	10
100	15

T_{on} sec	C_T* uf
0.1	15
0.2	30
0.5	68
1.0	150
2.0	300
5.0	680
7.5	1000
10.0	1500

* Timing capacitor C_T should have extremely low leakage current.

Q1 - Pass Transistor

I_{OUT} A	PNP Transistor	P Channel MOSFET	N Channel MOSFET
< 1.0	TIP30 D41D4	IRF9511 RFP5P12	IRF511
2.5	TIP32,34 D45C2	IRF9521 RFP6P08	IRF521
5.0	D45H5,8 MJE6040	IRF9531 RFP12P08	IRF531 IRFZ10
7.5	TIP36 2N6666*	IRF9541	IRF541 IRFZ20
10.0	TIP36,145* 2N6648*	IRF9541 RFK25P08	IRF540 IRFZ20
15.0		IRF9Z30 RFK25P08	IRFZ30
20.0	2N6285*	RFK25P08	IRFZ40

* Darlington transistor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UC1860 – NEW IC CONTROLS RESONANT MODE POWER CIRCUITS

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ABSTRACT

A new integrated circuit, the UC1860, is introduced. Its prime purpose is to provide the control function in resonant mode power supplies operating at frequencies up to 3 MHz. A frequency modulated, fixed on-time control scheme is implemented. Additional features include a programmable under voltage lockout circuit and a programmable soft-start/hic-up circuit.

BACKGROUND

For years, rumblings of the coming (or perhaps more correctly, reapplication) of resonance as a useful tool in the power control world have been growing progressively louder. Being a recognized manufacturer of pulse width modulation control ICs, some of these noises have been focused directly at Unitrode Integrated Circuits Corporation. Receiving, conditioning, filtering, and discriminating these signals, however, has been somewhat of a frustrating chore. Information indeed has been sought to aid in the definition of chip to perform all required resonant mode control functions. Too often the response was an inverse request: "Tell me what the chip looks like and then I can design my power supply." The immaturity of the technology has naturally made the sharing of information somewhat less than authorative. Finally there came a day when a best guess architecture and specification goals list had to be embraced as presumed gospel. It is that choice that has resulted in the chip to be discussed in this paper.

This paper, then, will describe the UC1860 with respect to its architecture and the specific features and performance of some of the sections. The chip is intended to fully implement all features necessary for the control function in a resonant mode power supply.

BLOCK DIAGRAM

The UC1860 control IC is designed to control power conversion circuits requiring frequency modulated fixed pulse widths such as resonant or quasi-resonant mode power supplies (figure 1).

The central section of the system is composed of 6 main blocks. A precision reference is provided for the error amplifier. These serve as the basis to control a variable frequency oscillator (VFO) which in turn triggers a one-shot. The programmable one-shot determines the output pulse width of the output drivers which are specifically designed to drive power mosfet gates. Finally a toggle flip flop steers the one-shot signal to the appropriate output stage.

In a typical application, the error amplifier is used to compare power supply output voltage to the internal reference. The error amplifier is also used as a gain block with which to compensate the overall power supply control loop. The output of the amplifier is resistively coupled to the VFO to control frequency. VFO frequency is directly proportional to error amplifier output voltage. Output pulse width is selected by an external RC pair. Pulses are sequenced to the output pins to activate the switches in the power circuit.

On chip peripheral housekeeping blocks are under voltage lockout (UVLO), fault management, and start-up/restart sequencing. The UVLO block forces the chip to wake up in a consistent and intelligent state when power is applied.

An additional uncommitted open collector comparator is on chip. This comparator can be used to accomplish a host of user defined functions.

ERROR AMPLIFIER

Understanding the chip requires considering the blocks one by one. The first block of interest in the main control section of the chip is the error amplifier. This amplifier is a high bandwidth, low offset, clamped swing design (figure 2). The non-inverting input is internally connected to a resistive divider from the reference voltage. While the divider is set for 3V, the combination of offset voltage and divider accuracy is specified as a ratio of the reference voltage. This allows an external reference of greater accuracy to drive the chip reference for better system accuracy.

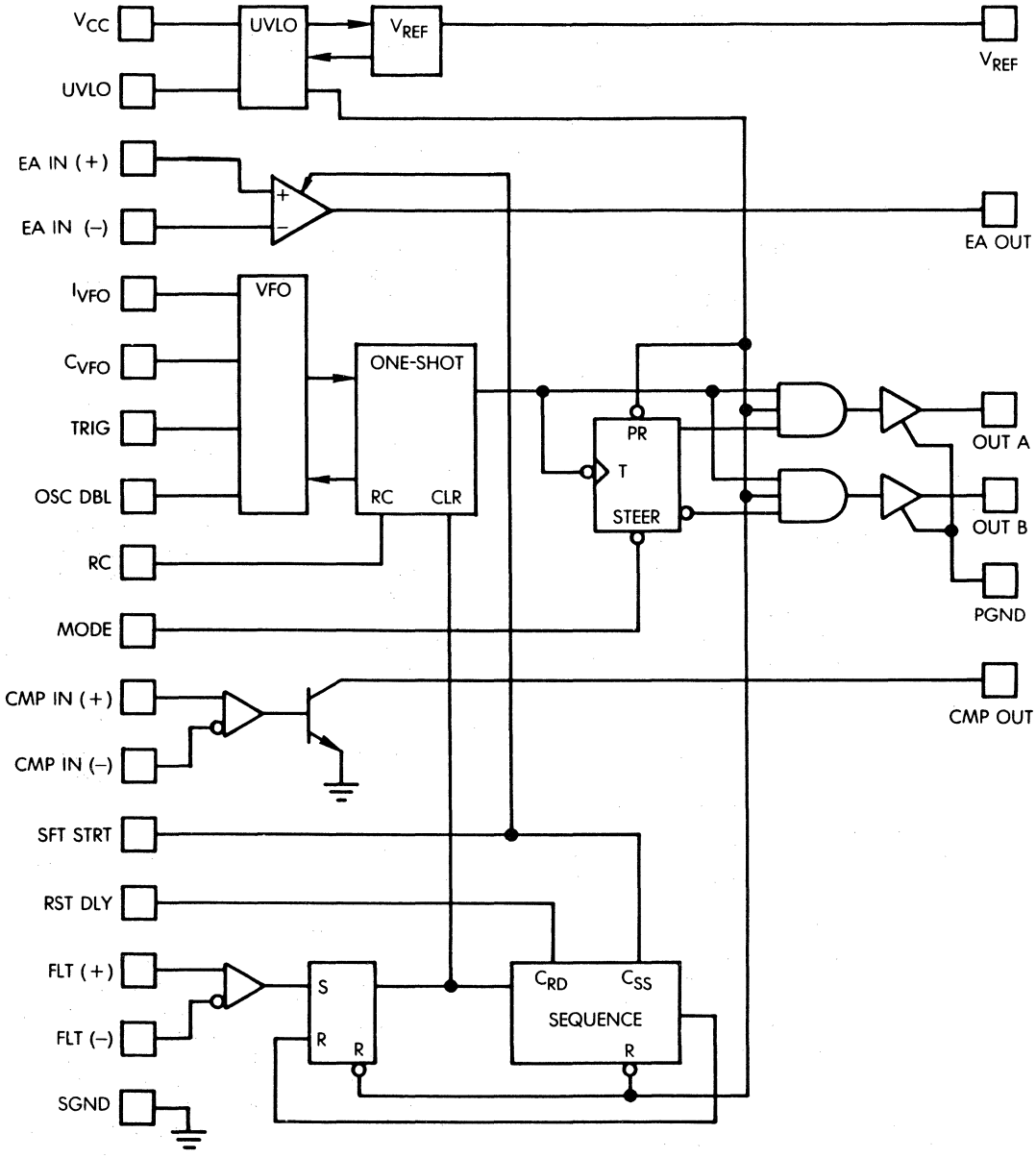


FIGURE 1. UC1860 SIMPLIFIED BLOCK DIAGRAM.

With three gain blocks (transconductance, transresistance, and voltage), the amplifier is compensated by two capacitors. The first feeds forward around the first stage directly to the second stage. This is because the first stage is designed for high gain and low offset but has poor high frequency characteristics. The second capacitor, the main

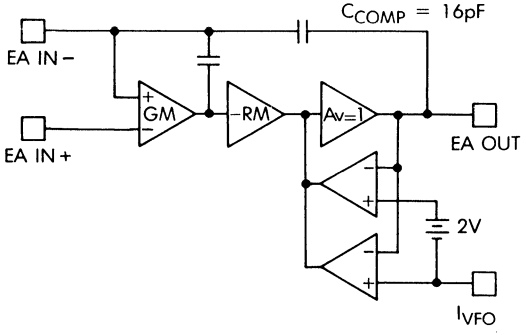


FIGURE 2. ERROR AMPLIFIER WITH OUTPUT SWING CLAMPS.

compensation capacitor, is connected from the output to the inverting input.

Amplifier bandwidth is controlled by the impedance seen by the inverting input terminal. To the first order, bandwidth in a simple feedback configuration is easily calculated by the equation

$$fo = \frac{1}{2\pi(Rin)(Ccomp)} \qquad \text{(eq. 1)}$$

where Ccomp is the internal 16 pF compensation capacitor that appears between the output and inverting input pins. The amplifier is unity gain stable for unity gain bandwidths less than 5 MHz (ie. Rin > 2 kohm).

Higher gain bandwidth products can be obtained by choosing Rin and closed loop gain appropriately. Figure 3

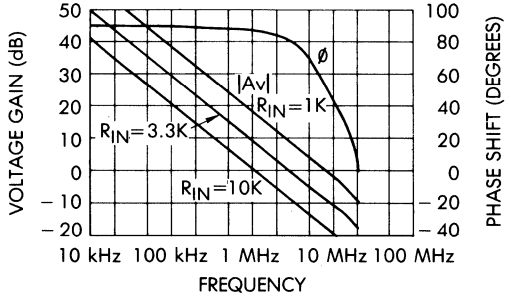


FIGURE 3. ERROR AMPLIFIER FREQUENCY RESPONSE.

shows the gain and phase characteristics of the amplifier for various resistive input impedances. Note that the phase curve is the same at higher frequencies for all three values of Rin shown. This is to be expected, since the higher order poles are internal to the amplifier. The combination of Rin and Ccomp primarily adjust the first pole position leaving higher frequency phase response unchanged.

Since the error amplifier is intended to control the frequency of the VFO, the outputs are clamped to obtain predictable minimum and maximum frequency. Each clamp circuit is actually an independent amplifier that monitors the output of the error amplifier and compares it to a reference. The reference for the lower clamp amplifier is the voltage at the I_{VFO} pin while the upper clamp is 2V higher. If the error amplifier attempts to exceed either of these levels, the appropriate clamp amplifier overrides the third stage of the error amplifier and the output is held at the clamped value. Figure 4 shows a plot of typical input offset voltage as a function of output voltage. In the figure, the horizontal axis is output voltage referenced to the I_{VFO} voltage. Note the sharp edges at the two extremes indicating clamped operation.

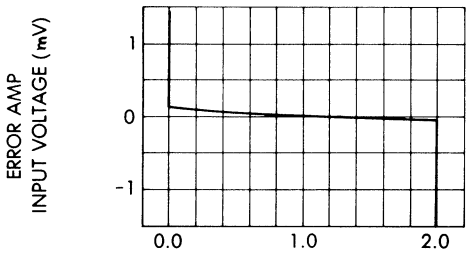


FIGURE 4. ERROR AMPLIFIER DC CHARACTERISTICS.

VARIABLE FREQUENCY OSCILLATOR

The variable frequency oscillator and one-shot functions are closely integrated to achieve the desired operating characteristics. ECL type logic gates and comparators are used to facilitate high frequency (3 MHz) operation. The oscillator will free run at a frequency of approximately

$$f(osc) = \frac{I_{VFO}}{C_{VFO}} \qquad \text{(eq. 2)}$$

In no case, however, can the frequency of the oscillator ever exceed the frequency required to support a complete pulse width from the one-shot.

Figure 5 is a detailed block diagram of both the VFO and the one-shot. The frequency of the VFO is proportional

9

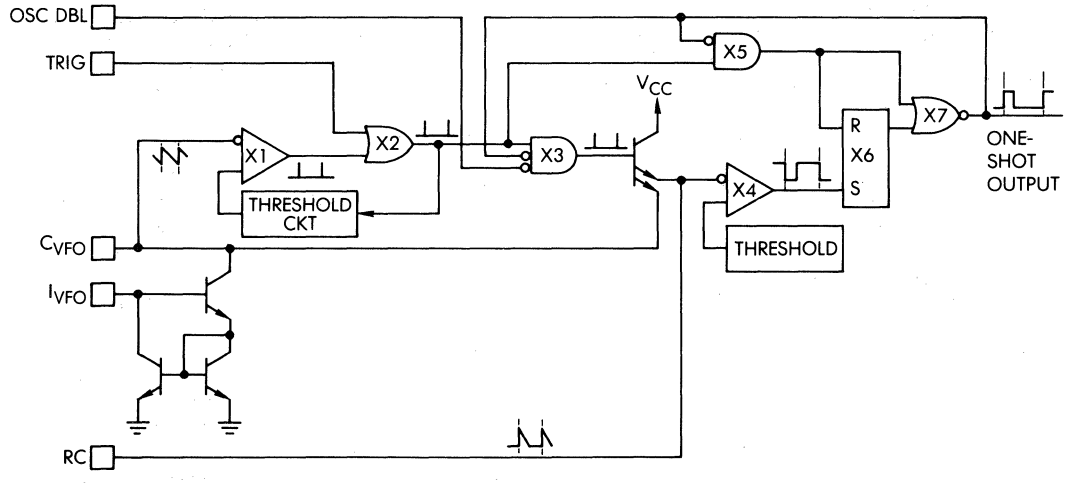


FIGURE 5A. DETAILED BLOCK DIAGRAM OF VFO AND ONE-SHOT.

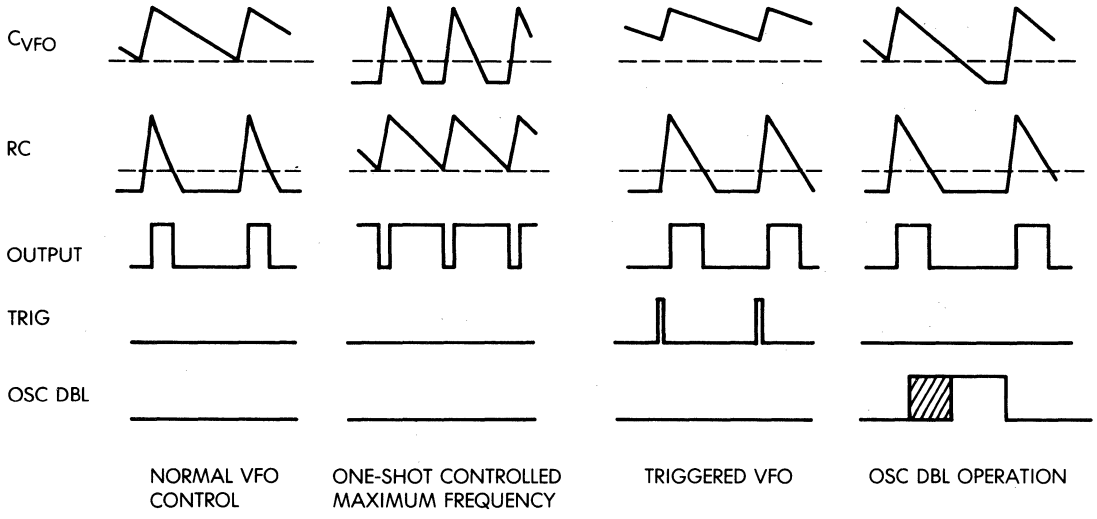


FIGURE 5B. TIMING DIAGRAMS FOR THE VFO AND ONE-SHOT.

to the current into the I_{VFO} pin. This pin is the input to a Wilson style current mirror and exhibits the temperature coefficient of two diodes (approximately 1.4V at 25C with a temperature coefficient of -4mV/C). I_{VFO} current is mirrored about to discharge the timing capacitor, C_{VFO}. Under normal operation, when C_{VFO} discharges to the lower oscillator threshold, hysteretic comparator X1 changes state causing gate X3 to recharge both C_{VFO} and the timing capacitor on the RC pin. Hysteretic comparator X1 then resets and the oscillator recycles.

The trigger (TRIG) and oscillator disable (OSC DBL) inputs can be used to modify the free running characteristics of the oscillator. If TRIG is raised above its threshold during the discharge time of the oscillator, the recharge sequence is immediately executed, resulting in synchronous operation. If, however, OSC DBL is true when either the lower threshold is crossed or the trigger input is received, X1 will change states, but X3 will not recharge the capacitors. They will continue to discharge until a lower retaining level is reached. As soon as OSC DBL returns false, then recharge action occurs immediately.

When the error amplifier output and the oscillator input, I_{VFO} are coupled with a resistor, R_{VFO}, then the oscillator frequency is determined by

$$f(osc) = \frac{V_{EA} - V_{IVFO}}{R_{VFO} * C_{VFO}} \quad \text{(eq. 3)}$$

where V_{EA} is the output voltage of the error amplifier and V_{IVFO} is the input voltage at the IVFO pin. The VFO gain, df/dV_{EA} is

$$\frac{df(osc)}{dV_{EA}} = \frac{1}{R_{VFO} * C_{VFO}} \quad \text{(eq. 4)}$$

With this simple arrangement the maximum frequency is given by

$$f(max) = \frac{2V}{R_{VFO} * C_{VFO}} \quad \text{(eq. 5)}$$

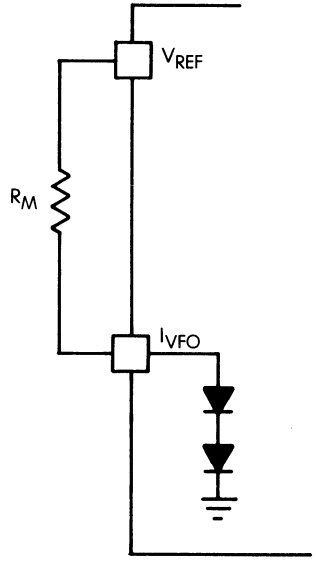
since the error amplifier maximum output is clamped two volts above the IFVO pin. Likewise, the minimum frequency should be zero. There is, however, an obvious limitation of minimum frequency in the input offset voltage of the lower clamp amplifier. Actual minimum frequency is

$$f(min) = \frac{vio}{R_{VFO} * C_{VFO}} \quad \text{(eq. 6)}$$

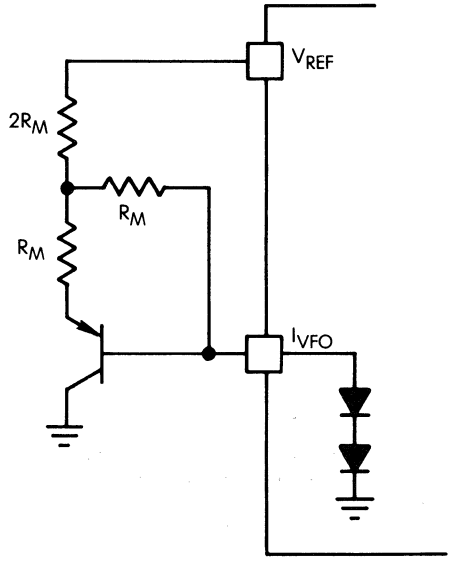
For lower clamp offsets less than 5mV, the maximum range of frequency would be the ratio of 2V and 5mV, or 400 to one.

When a nonzero minimum frequency is desired, an additional current can be injected into the I_{VFO} pin independent from the error amplifier. This can be most easily accomplished by a single resistor from the I_{VFO} pin to V_{REF} (figure 6). In this case, minimum frequency is given by

$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}} \quad \text{(eq. 7)}$$



$$f(min) = \frac{V_{REF} - V_{IVFO}}{R_M * C_{VFO}}$$



$$f(min) = \frac{1V}{R_M * C_{VFO}}$$

FIGURE 6. MINIMUM OSCILLATOR FREQUENCY.

where R_M is the external resistor. It is important to note that this method is not inherently flat over temperature since the voltage at the I_{VFO} pin varies as two diodes. If this variation is unacceptable, three resistors and a pnp transistor can overcome this problem resulting in a minimum frequency of

$$f(min) = \frac{1V}{R_M * C_{VFO}} \quad \text{(eq. 8)}$$

ONE SHOT

The one-shot capacitor at the RC pin is recharged concurrently with C_{VFO}. This sets the output of comparator X4 to a low state allowing S/R latch X6 to be reset. The latch is reset by the signal coming from the output of X2 in the oscillator section via gate X5. The output of X5 also blanks the one-shot off. This is done for accuracy reasons so that the on time is solely a function of the resistive discharge of the RC pin. When both caps have been charged fully, the oscillator circuit drives the output of X2 low allowing both caps to discharge. The timing cap is discharged by an external resistor. The threshold of comparator X4 is set at 80% of the timing capacitor's full charge value. 0.22 time constants are required to reach this threshold making the on time

$$t(on) = 0.22 * RC. \quad \text{(eq. 9)}$$

When the lower threshold is reached, X4 output goes high setting S/R latch, X6, and the one-shot pulse is terminated.

It is important to observe two interactions between the VFO and the one-shot. While the one-shot is high, gate X5 prevents the oscillator from erroneously blanking the output low. The high output also prevents X3 from recharging the timing capacitors in the same way that OSC DBL does. This insures that in no case can the oscillator period (the inverse of eq. 2) be shorter than the time required for the one-shot. In cases where the VFO attempts to overrun the one-shot, the one-shot dominates and establishes maximum frequency.

TOGGLE FLIP FLOP

The output of the one-shot, in addition to limiting the VFO from out running the one-shot, performs two other functions (figure 1). A logic high level from the one-shot causes one or both of the outputs to drive high. The falling edge of the one-shot not only turns the output(s) off, but it triggers the toggle flip flop to change state. The toggle flip flop selects the output to be driven if the output mode control pin is low. If the output pin is high, both toggle outputs are high causing outputs A and B to operate in unison.

OUTPUTS

The output blocks are well suited to driving the active capacitive load presented by power mosfet gates. With this load in mind, they are designed to deliver currents up to 3A in both source and sink directions. Current rise times are in the order of 75A/us. This results in rise and fall times of 50 ns when driving series loads of 10nF and 2.4 ohms (figure 7). Unloaded transitions are 12ns. Of course, cross conducted charge has been minimized within the constraints of high speed design goals.

It is well worth noting that careful attention to low inductance printed circuit board layout along with proper damping and application of schottky clamp diodes are necessary when driving a large capacitive load directly. Disregard for this caution will result in the output/load combination becoming a highly excited tank that will ring and inject current into the chip substrate. Such injection is almost always a sure cause of problems in bipolar ICs.

REFERENCE

The bandgap reference needs little mention since it is a standard, borrowed from many previous designs. Trimmed for precision at wafer probe to 5V, it is specified at 1% tolerance at room temperature with no more than a 2% spread over temperature. While intended as a reference, not a voltage regulator for external use, it has line and load rejection capabilities that will allow it to be used as such for loads under 10mA. A bypass capacitor is required on the reference.

UVLO

The UVLO block (figure 8) consists of three comparators arranged to allow for flexibility of application. They can accommodate off-line, DC to DC, and even operation from a 5V supply.

The first of the three comparators monitors V_{CC}. It has hysteretic thresholds of 17 and 10V. This spread is ideally suited to off-line applications. The output of the V_{CC} comparator is an emitter follower that can go no higher than approximately 6.5V.

The second comparator monitors the UVLO pin which is resistively driven from the output of the V_{CC} comparator. This comparator turns the reference on or off, controlling the bias in the chip. When the reference is off, I_{CC} is less than 0.5mA. After operation commences, I_{CC} increased to approximately 35mA. The thresholds of this second comparator are 4.0 and 3.5V.

The third comparator monitors V_{REF} and has a threshold of 4.5V. If either this comparator or the second has a low output, then the chip is disabled and reset. When this is the case, both output are driven to a low state, the toggle

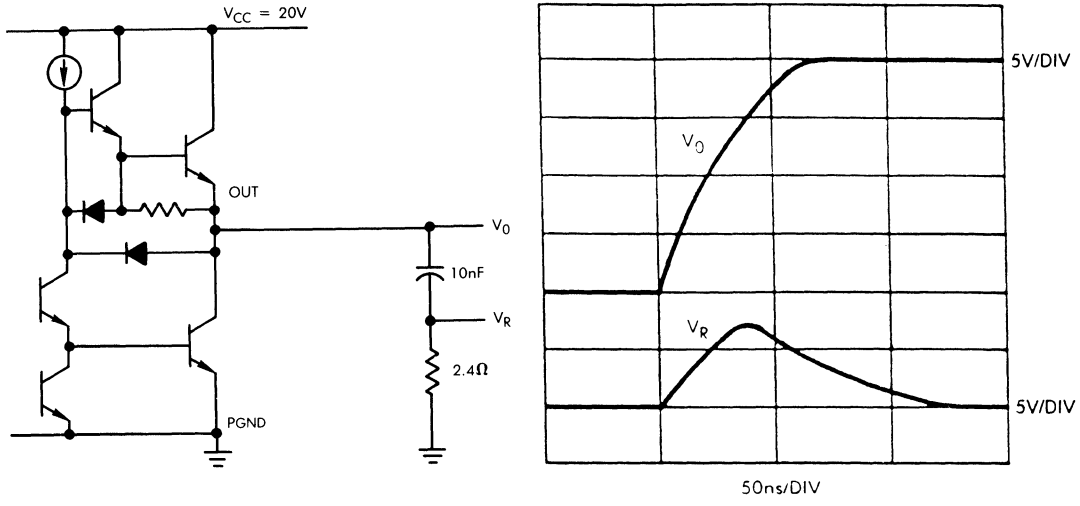


FIGURE 7. OUTPUT STAGE MEASURED PERFORMANCE.

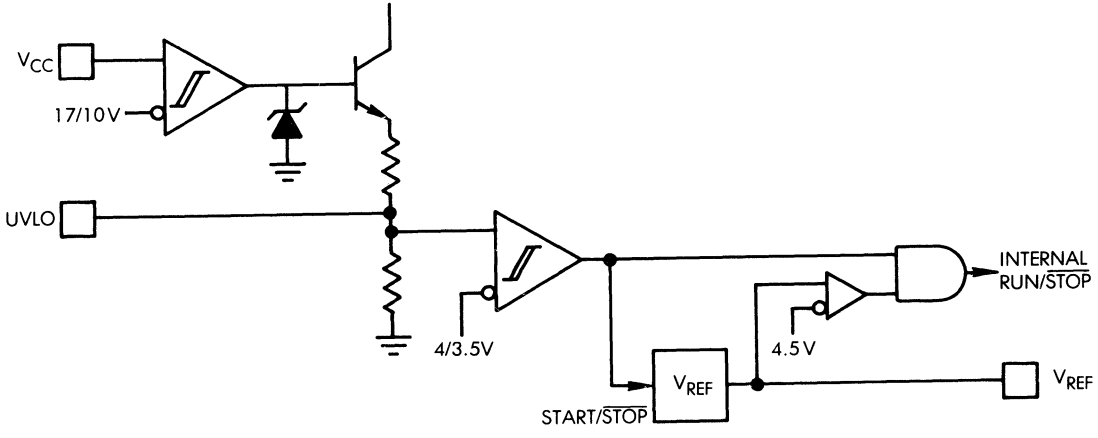


FIGURE 8. UVLO DETAILED BLOCK DIAGRAM.

flip flop is preset to select ouput A, the soft-start capacitor is discharged, and the fault latch is reset.

Application of the UVLO features is simple. With no connection to the UVLO pin, the behavior of the UVLO block is dominated by the V_{cc} comparator and is suited for off-line usage. DC to DC applications can be made by two external resistors, one from V_{cc} to UVLO and the other from UVLO to ground. This exploits the 4V hysteretic threshold of the second comparator. Keep in mind that the UVLO pin has an input impedance of 23 kohm when selecting the two external resistors. Operation from a 5V supply is achieved by tying UVLO, V_{cc}, and V_{REF} all to the external 5V supply. The UVLO pin can also be used to disable the chip at any time by pulling it below 3.5V. The UVLO pin will source no more than 1.5mA when pulled to ground.

FAULT MANAGEMENT AND RESTART SEQUENCING

The fault comparator and latch along with the soft-start and restart delay functions are shown in (figure 9). When the chip is powered up, UVLO resets the fault latch and discharges the soft-start capacitor, C_{SS}. The restart delay capacitor, C_{RD}, is also discharged since the latch is reset. After UVLO, C_{SS} is charged by an internal 5μA current source. The voltage at the soft-start pin is used to modify the upper clamp voltage of the error amplifier. In this way, a slow frequency ramp is obtained from zero to the point where the control loop takes over.

The chip is designed for easy implementation of a hic-up style of fault management. The fault comparator will sense signals with a common mode range of −0.3 to 3.0V. If (hopefully never in your application) the input to the fault comparator causes its output to go high, the fault latch is set. Immediately the one-shot is cleared and the outputs turn off. C_{SS} is also discharged. C_{RD} is then allowed to be charged by an internal 5μA current source. This is the zero power dissipation time in the hic-up cycle. Until the restart delay capacitor charges to 3V, the fault latch cannot be reset. When both the fault comparator output is low and C_{RD} is over 3V, the fault latch is reset. At this point in time, C_{RD} is discharged and C_{SS} is allowed to soft-start the chip. If the cause of the original fault is still present, the chip will continue to hic-up until the fault condition is removed, when normal operation will resume.

Note that the internal 5μA sources are not tightly controlled. However, if either soft-start or restart delay time is critical, a 50k resistor to V_{REF} will provide a precise current that is sufficient to swamp out any inaccuracies of the internal source.

Two variations of the hic-up are possible. Selecting a value of zero for C_{RD} will cause the chip to immediately attempt to restart upon removal of the fault signal. If, on

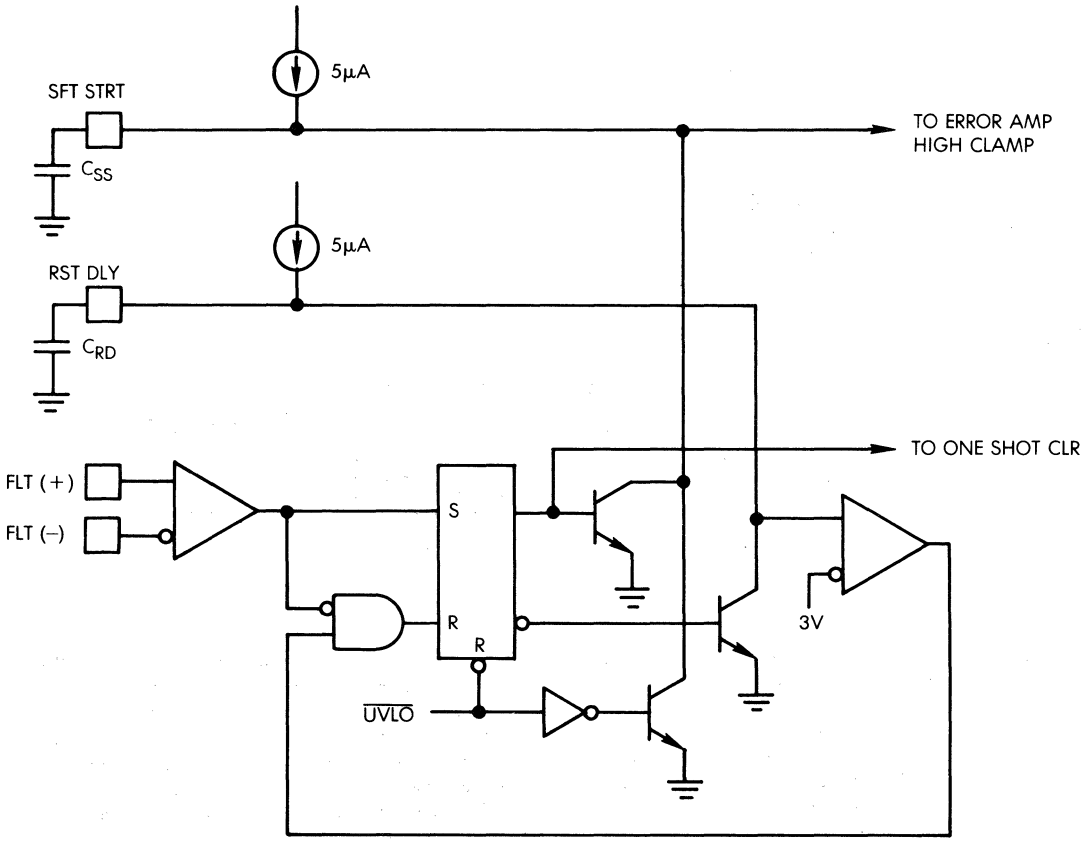


FIGURE 9 FAULT MANAGEMENT AND RESTART SEQUENCING BLOCK DIAGRAM.

the other extreme, fully latched fault behavior is desired, then the restart delay pin (RST DLY) can either be grounded or tied to the open collector output of an external logic gate. This uncommitted comparator could be used for this application. When Restart Delay is held low, then the only ways to reset the fault latch and reinitiate operation of the chip are to remove V_{CC} (UVLO will clear the latch) or release RST DLY, allowing it to exceed 3V.

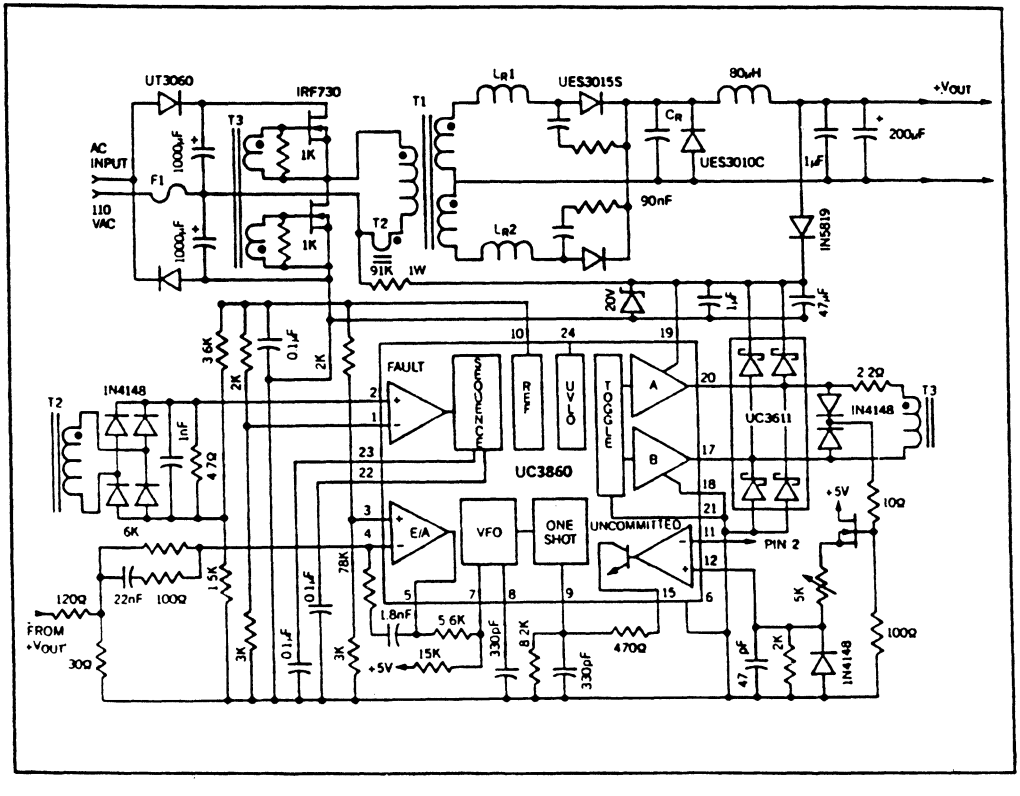
UNCOMMITTED COMPARATOR

The uncommitted comparator is similar in design and speed to the fault comparator except its output drives an open collector npn transistor. This output can be used in a variety of applications. One would be to shunt the RC pin with a second resistor causing a reduction in one-shot pulse width. The input common mode range is identical to the fault comparator, -0.3 to 3.0V.

SUMMARY

The UC1860 control chip has been designed with the necessary features to implement the control function in resonant mode power conversion circuits operating at frequencies up to 3 MHz. While some publicized applications have been considered in the design of this chip, its versatility should accommodate many specific adaptations of resonant mode power systems as well.

150 Watt Quasi-Resonant Power Supply

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UC3860 RESONANT CONTROL IC REGULATES OFF-LINE 150 WATT CONVERTER SWITCHING AT 1 MHZ

ABSTRACT

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms in addition to transferred charge and energy will be analyzed as functions of time, and input/output conditions. Specific and generalized equations are given for this example, also applicable to other topologies by those skilled in modern power supply design.

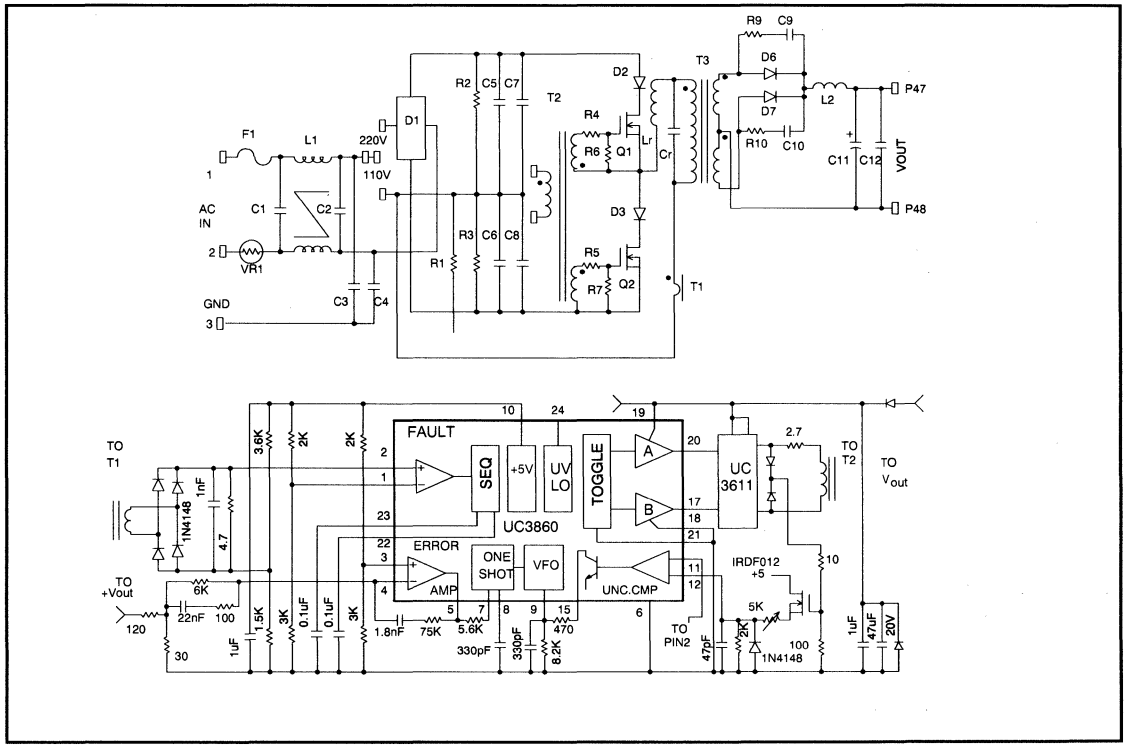
INTRODUCTION

The thrust towards resonant mode power supply designs has been fueled by the industry's demands for increasing power densities and high overall efficiency. Coupled with the additional requirements for low EMI, many designers are exploring the most likely candidate for todays sophisticated, high frequency power supplies; resonant mode power conversion.

amperes of load current, it operates from a 110/220 AC input, or 220 to 380 VDC at high efficiency.

DESIGN CONSIDERATIONS AND OVERVIEW

Although several basic topologies deserve consideration in this off-line application, only the Half Bridge configuration offers numerous key advantages. As opposed to the single-ended Forward converters, the half bridge provides bidirectionial utilization of the transformer, thus eliminating the need to incorporate dissipative or complex flux reset mechanisms. In addition, the primary switched voltage is one-half that of its single ended or full-bridge counter-part, significantly reducing the turn-on losses. As a reminder, zero current switching minimizes ONLY the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge results in lower turn-on losses due to the lower voltage.

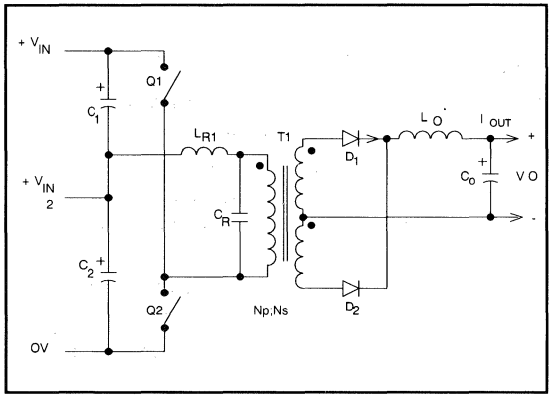


While a bewildering selection of possible resonant mode topologies and configurations exist, this paper will focus on the quasi-resonant half bridge topology. Primary side resonance and zero current switching will be incorporated into the design, with the control circuit essentials performed by the UC3860 resonant mode control IC.

Described in the text is a 150 watt off line converter switching at maximum frequency of 1 megahertz resulting in an effective 500 kilohertz utilization of the main transformer. Delivering 15 volts at 10

Primary side resonance will be utilized in this design, but not as an attempt to minimize the core size. Instead, this technique will reduce the peak secondary currents and rectifier losses. transferrring them to the primary side where the diode voltage drop is less significant, thus enhancing overall efficiency. Additionally, this design can be compared to a previous example [ref. 1] which incorporated secondary side resonance and operated over similar line, load, frequency and power variations.

Half cycle conduction in both design examples accomplishes a undirectional current flow at each of the primary switches. Unlike its full counterpart, all the energy stored i n the resonant capacitor must be transferred to the output, without returning the excess back to the primary storage capacitors.



The UC3860 resonant control IC will adjust the conversion frequency to regulate the fifteen volt output over all line and load combinations. Zero current switching is facilitated by modulating the programmed maximum on-time with the controller's uncommitted comparator. In addition, overload protection is provided by means of a programmable restart delay circuit (hiccup) which reduces the conversion retry rate following a fault detection.

DESIGN SPECIFICATIONS

An off-line 150 watt, single output design has been selected as a typical application. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations.

INPUT VOLTAGE

110 VAC INPUT = 85 MIN, 132 MAX (VAC)

220 VAC INPUT = 170 MIN, 270 MAX (VAC)

DC INPUT = 220 MIN, 380 MAX (VDC)

AC LINE FREQUENCY = 50 HZ MIN

OUTPUT VOLTAGE = 15 VDC

OUTPUT CURRENT = 10 AMPS MAXIMUM CONTINUOUS, 2.5 AMPS MIN

LINE REGULATION = 15 MILLIVOLTS

LOAD REGULATION = 15 MILLIVOLTS

OUTPUT VOLTAGE RIPPLE=

100mV (Pk-Pk), DC-20 MHZ

EFFICIENCY = 75% TYP. AT FULL LOAD

TOPOLOGY FUNDAMENTALS AND OVERVIEW

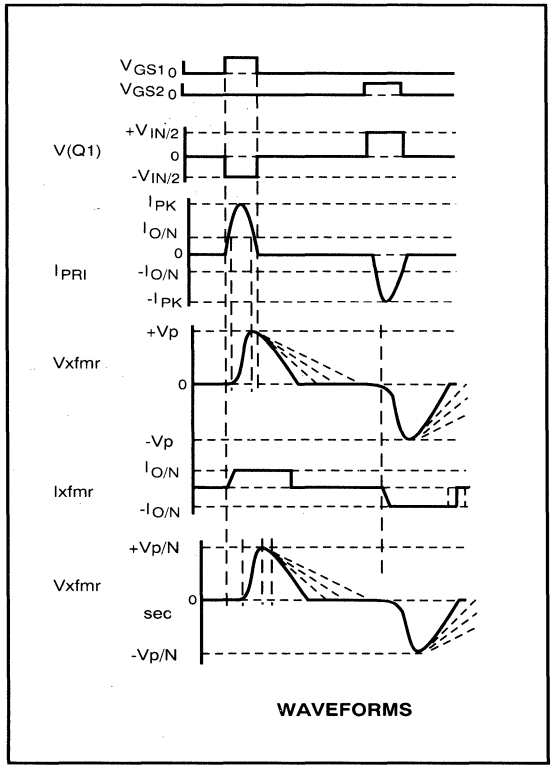
The general circuit diagram for a quasi-resonant half bridge converter using primary side resonance is shown with the corresponding waveforms. Transistors Q1 and Q2 are alternately driven from the control circuitry at a repetition rate determined by the UC3860's error amplifier output voltage and turned off at zero current by the detection circuitry.

Transistor Q1 turns on at time t(0), connecting the series resonant L C tank across the bulk storage capacitor C1, with a voltage potential of +Vin/2. The primary current ramps up linearly at the rate of +Vin/(2*Lr) from zero to Iout/N which is intersected at time t(1). During this interval dt(1-0) all primary current is delivered to the output, and no voltage is across the resonant capacitor Cr.

Beginning at time t(1), primary current can be expressed by adding the two individual components; the "constant" output current Iout/N, and the sinusoidal current (Ir) flowing through the resonant capacitor. The peak resonant current is determined by the iput voltage (+Vin/2) divided by the characteristic tank impedance, Zn. Primary current rises to its peak of Ir plus Iout/N, and decreases sinusoidaly. It intersects the output current (Iout/N) again at time t(2), and crosses zero at time t(3) when the transistor switch is turned off.

In a sinuosidal manner, the resonant capacitor voltage begins its rise at time t(1) and continues to its peak at time t(2). The voltage then decreases until time t(3) where it then begins a linear discharge at the rate of Iout/Cr. Zero voltage is reached at time t(4) when all stored charge in the resonant capacitor has been transferred to the output. This waveform is also the transformer primary voltage, and is reflected to the secondary side by the turns ratio N.

Secondary current has a linear leading edge until reaching its plateau of Iout, assuming a negligible magnetizing current for the output inductor. The resonant capacitor provides a constant current to the output until its charge is totally transferred. At this point, the energy is stored in the output LC section provides a regulated output until the next cycle is initiated. Consecutive switching cycles will repeat the conversion process and corresponding waveforms.

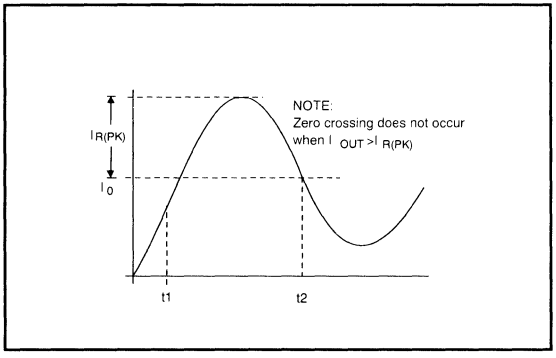


WAVEFORMS

QUASI-RESONANT CIRCUIT LIMITATIONS

In order to facilitate zero current switching, the peak resonant current component I(r) must always be greater than Iout, or the zero inersect will not be reached. Specifically, the output impedance (Zo) must always be greater than the characteristic tank impedance, (Zn). This relationship also specifies the minimum input voltage (Vin min) and maximum output current (Iout) limits for proper circuit operation.

The ideal ratio of the full output current (Iout max) to the minimum resonant peak current Ir(peak) min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents, and losses. A twenty-five percent overload current will be used as a guardband in this design. Typical of many current limit thresholds, it corresponds to an 0.75:1 ration of Iout(max) to Ir(peak)min.



Being a Buck derived topology, the secondary input and output volt-second products must be equal, thus defining Vin (secondary) minimum. The resonant tank inductor and capacitor can be transposed to the secondary also, and calculated knowing Vin min(sec), F(res) and Z(o)min. Once the transformer turns ratio has been determined, these can be appropriately scaled to the primary side.

The resonant L-C components are now uniquely defined by:

$$L(r)sec = \frac{75 * Vsec\,(min)}{2 * Pi * Fres * Iout} = \frac{0.12 Vsec\,(min)}{Fres * Iout\,(max)} = 175nH$$

C(r)sec = 1 [(2*Pi*Fres)^2*L(r)=91nF

Z(r)sec = (L(r)/C(r))$^{0.5}$ = 1.39 ohms,

and Fres = 1.25 MHz

TRANSFORMER TURNS RATIO

The determination of the transformer turns ratio for this design will begin similarly to that of conventional square wave converters. Obviously, the required output volt-second product must first be satisfied with the most difficult condition being low line and full load. A topology coefficient, K(t) is introduced to specify the maximum ratio between the conversion (switching) frequency and the resonant tank frequency. This is somewhat analagous to maximum duty cycle is a square wave converter. As K(t) approaches unity, the utilization is maximized and turns ratio is optimized.

Charge is taken from the bulk storage capacitors during each cycle and stored in the resonant capacitor. The output load discharges this at a rate determined by the output currrent, and the discharge time varies inversely with load current. At full load, the minimum discharge time is reached, reduceing the topology coefficient, K(t), to 0,8 in this application.

To satisfy the required output volt-second product of this Buck derived converter at low line:

$$Vout = \frac{Vpri * K(t)}{2 * N},\ or\ N = \frac{K(t) * [Vp\,(min) - Vloss]}{2 * (Vo + Vd + Vloss)} = 5.1{:}1$$

More specifically, the turns ratio can be calculated by examining the total charge transferred per cycle, Q(t). This varies as a function of Vin, Iout and Vout, assuming C(r) is fixed and zero current switching. [ref 2] Using the specified parameters for this design, the relationships are combined and the quadratic equation is solved, resulting in a turns ratio (Np/Ns) of 5.1:1 also. The design will proceed using a 5:1 ratio for simplicity.

$$N^2\left[\frac{Lrs * Io}{(Vo + Vd)} - Tc\right] + N\,\frac{(Vpri - Vx)}{4 * Fr * (Vo + Vd)} + \frac{Crs * (Vp - Vx)^2}{2 * (Vo + Vd) * Io} = 0$$

where Tc= 1/Fconv(max) = 1us; Vx= Vloss primary MOS switch

Vd=Vrectifier (output); Io=Iout maximum

and Vpri=Vp(minimum)

MAIN TRANSFORMER DESIGN

Off-line transformers lend themselves to low, wide bobbin windows, typical of the ETD geometry. This shape window provides adequate room to accomodate the creepage and clearance distances required for international safety specifications. Transformer losses will be held around one-percent of the total input power, or approximately 2 watts with a temperature rise not to exceed 40 degrees Centigrade. A core size is selected with a thermal impedance R(t) in the neighborhood of 40°C/2W, or 20°C/W. The precise size will be calculated using the area-product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} * 10^4}{120K2f}\right]^{1.58} * (K_h f + K_e f^2)^{0.66} \quad cm^4$$

WHERE:

Pin = Input Power - 180 Watts

K = Winding Factor = 0.163 for a half bridge

f = Transformer Frequency = 500 KHZ

Kh = Hysteresis Coefficient = 4*10^-5 for 3C85

Ke= Eddy Current Coefficient = 4*10^{-10} for 3C85

A calculated area-product of 0.543 cm^4 steers the selection towards the ETD-34 geometry and size, and 3C85 material. Since the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

Calculating the volt-second product for this primary side resonant design is more difficult than for that of its secondary side counterpart. Integrating the complex voltage waveform over the conversion period is the most exact method, as detailed in the charge transfer equations [ref2]. A less precise, yet fairly accurate technique is to assume a triangular voltage waveform, breaking the period into on-time and off-time sections. Addition of these geometric areas (V*t) results in an estimate of the actual primary volt-second product. Core losses will need to be analyzed over the full range of line, load and conversion frequency ranges. The minimum number of primary turns will be calculated using low line conditions, and the cross sectional core area of 0.971 cm^2. A total flux density swing of 1 kiloGauss (per manufacturers data) is recommended not to exceed the allocated temperature rise.

$$Np\,(min) = \frac{PrimaryV * t\ product * 10^4}{FluxSwing * CoreArea}$$

Using low line condition and 10V MOS drop.

$$Np\,(min) = \frac{0.5 * 200 * 10^{-6} * 10^{4}}{0.100\ T * 0.971\ cm^3} = 10.3\,Turns$$

(Use 10 Turns)

The actual core power density is calculated from the following equation, allowing a 20 degree temperature rise due solely to core losses.

$$Power\ Density = \frac{T_r}{R_t \cdot Vol} = \frac{20^{\circ}C}{19 \cdot 7.64} = 138 mw/cm^3$$

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19 degrees C per watt, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between core and copper loss can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accommodate fewer turns, or less copper.

It has already been established in a previous section that the turns ratio for this design be 5:1, Npri: N sec. Minimization of the leakage inductance is obtained by "sandwiching" the secondaries between the primaries, or using a split primary winding technique.

In this example, one-half of the primary number of turns will be wound first, closest to the core center leg. Then, the corresponding secondary is wound directly above its primary, followed by the other secondary. The final winding is the remaining primary half, with good coupling to its corresponding secondary as shown in the following figure.

WINDING ORIENTATION

Copper strap or foil will be utilized for each winding to minimize "build-up" which increases the distance between windings, hence leakage inductance. The necessary primary and secondary copper areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

PRIMARY RMS CURRENT, I pri(rms) = 2.8 AMPS RMS

SECONDARY RMS CURRENT 1sec(rms) - 7.1 AMPS RMS (EACH WINDING)

PRIMARY CONDUCTOR AREA Axp = Ipri(rms)/450 A/cm3 = $6.33 * 10^{-3} cm^2$

SECONDARY CONDUCTOR AREA Axs = 1sec(rms)/450A/Cm3 = $15.8 * 10^{-3} cm^2$

PRIMARY INDUCTANCE, Lpri = Al*Np^2 = 190 uH

SECONDARY INDUCTANCE, Lsec = Al*Ns^2 = 7.6 uH (each)

The primary conductor area is approximately equal to that of an AWG #19 wire, while the secondary area is closest to an AWG #14 wire. From Eddy Current calculations is can be seen that the depth of penetration at 500KHZ is $10.6 * 10^{-13}$ cm, or about the thickness of an umber 37 AWG wire. The most practical technique to minimize the AC loss in a transformer winding is to incoporate copper strip, or foil, as in this design. Its width is determined by the bobbin width and safety spacing requirements of 8 mm per winding as shown.

An 8 millimeter primary to secondary spacing between the winding ends will be subtracted from the bobbin width of 2.1cm, leaving 1.30 cm for the copper strap width. Allowing for tolerances, standard half-inch (0.500") width foil will be utilized in this design.

Standard 2 "mil" (0.002 in) foil will be used for the primary, which is slightly larger than the required thickness of 1.872 thousandths of an inch. The calculated secondary thickness exceeds the depth of penetration, so twin foils each of half the required thickness (0.0085 cm) are mandated. Each of the three "mil" (0.003") foils will be thinly insulated from the other.

The resistance and power loss of each winding is summarized:

R pri = $2.29 * 10^{-6} * 5.99 * 10$ T/$6.18 * 10^{-3}$ = 22.2 milliohms.

R sec = $2.29 * 10^{-6} * 5.99 * 2$T/$21.91 * 10^{-3}$ = 1.25 milliohms

Winding power loss = 1 rms^2 (winding) * Resistance (winding

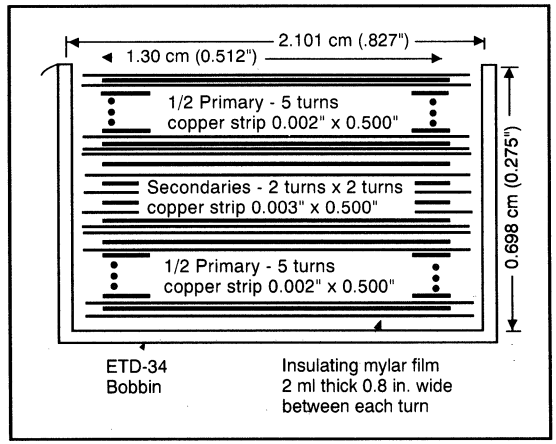
P loss pri = $2.8^2 * 0.0222$ = 174 milliwatts (each wdg)

P loss sec = $7.1^2 * .125 * 1^{-3}$ = 63 milliwatts (each wdg)

P loss copper = 2*(174 + 126 mW) = 0.60 watts

Transformer power loss = copper + core loss = 1.5 watt total

Temperature rise = R(0) * Ploss total = 19°C/W * 1.5 = 28.5°C



DESIGN PROCEDURE AND SUMMARY

The resonant components can now be transformed to primary side values using the caluclated turns ratio N.

L(r)p = L(r)s * N^2 = 4.4 uH

C(r)p = C(r)s / N^2 = 3.6 nF

Z(r)p - [(L(r)p / C(r)p)$^{0.5}$] = 35 ohms

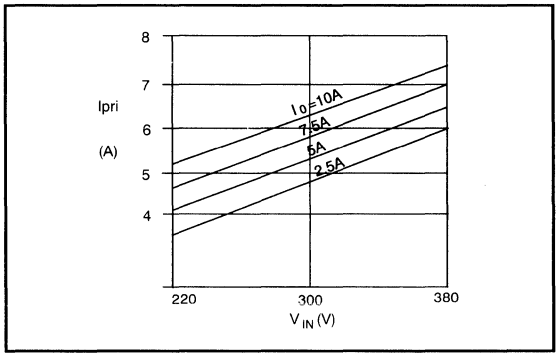
Additionally, the peak primary current and rms currents at the transistor switch, transformer primary and secondary rectifiers are calculated by the following relationships:

I(p)pk = [Io(max)/N] + Vp(max)/(2*X(r)p) = 5.2A @220V, 7.4A @380V

I(p)rms = I(p)pk*[Ton/(2*Tconv[]$^{0.5}$ = 2.85 Arms at XFMR primary (assume pulsed sinusoid) = 2.01 Arms at each switch

I(s)rms = I(o)max*[(Ton/Tconv)0.5] = 7.8Arms at XFMR secondary = 5.5Arms per rectifier

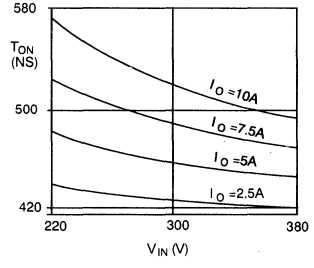
The selection of semiconductors, rectifiers, heatsinking requirements and wire gauges follow standard design practices. For the purpose of this paper, no elaboration is included, however is detailed in references 1 and 2. Using this design equations listed previously and in the Appendix, these parameters can be calculated and plotted over the line and load ranges specified, and are summarized in the following graphs:



TIMING CONSIDERATIONS

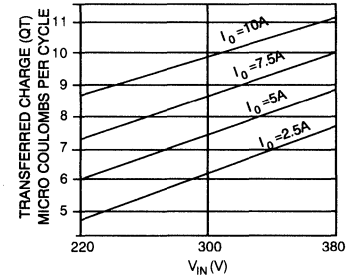
The operation of this quasi-resonant circuit has been described as requiring a variable frequency, FIXED on-time control pulsetrain. In actuality, the on-time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented in chapter five, the on-time is calculated and plotted for the ranges of Vin and Iout.

ON-TIME vs. Vin AND Iout



The charge transferred from the primary to the secondary per cycle is a function of both Vin and Iout. Using the equations presented previously in section 5, the results are graphically represented in the following figure.

Transferred Charge vs. Vin and Iout

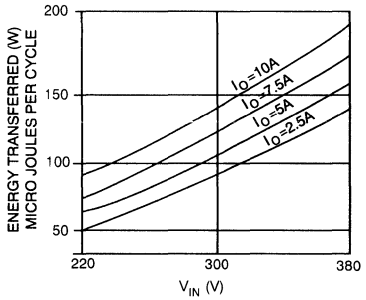


For the selected values of voltage and current shown, the average change required in voltage or output current per micro Coulomb transferred have been calculated.

AVERAGE dV/uC = 5.935 V/uC; and the average dI/uC = 2.086 A/uC

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by Vin / 2 to convert from charge to energy, with the results shown below.

ENERGY TRANSFERRED PER CYCLE



The conversion period is obtained by dividing the energy transferred per cycle by the output power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for various input voltages and output currents below.

CONVERSION FREQUENCY

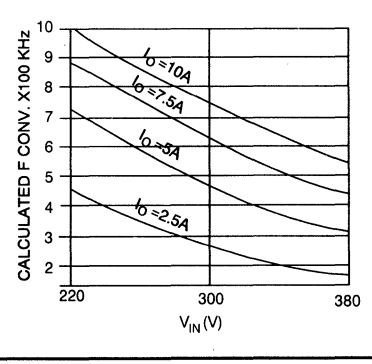
The control circuit adjusts the conversion frequency to maintain a constant output voltage of V out over changing line and load combinations. Maximum conversion frequency will occur at low line and full load, where, by design, the frequency equals the resonant tank frequency divided by K(t). Minimum frequency will occur at high line (Vpri max) and light load (Iout min), and the following equation can be used to estimate the conversion frequency for various line and load possibilities.

$$Tconv = \frac{vpri}{2*N*Io*Vo}\left[\frac{2*N*Lrs*Io^2}{Vpri} + Vpri\frac{*Crs}{N} + \frac{Io}{2*Fr}\right]$$

which can be expanded to account for losses in both the primary switches (Vx) and output rectifiers (Vd) and reduced to:

$$Tconv = \frac{Lrs*Io}{Vo-Vd} + \frac{Crs*(Vp-Vx)^2}{2*N^2*Io*(Vo-Vd)} + \frac{Vp-Vx}{4*N*Fr*(Vo-Vd)}$$

CONVERSION FREQUENCY vs. Vin & Iout



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OUTPUT FILTER DESIGN

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHZ equating to 90 uH. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. A 1.3" o.d. toroidal core of high frequency material was utilized, available as a standard product from Pulse Engineering.

For the output capacitance, two 100 uf electrolytic capacitors were used in parallel to achieve an ESR value of 3 to 15 milliohms — a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers. A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolythic capacitors are used for this application.

THE UC3860 RESONANT MODE CONTROL IC

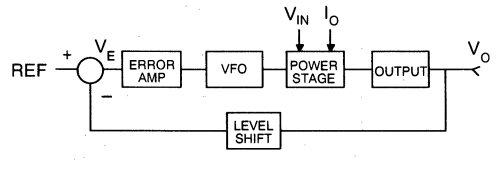
The versitile UC3860 resonant mode controller easily implements fixed on-time, frequency modulated control schemes while providing various user programmable features and unique fault protection. Specifically, this 3 MHz device includes dual 3 amp peak totem pole output drivers and precision clamps on the 5 MHz error amplifier output to accurately control minimum and maximum frequency. In addition, an uncommitted comparator is included for use with zero current switching techniques, and programmable fault thresholds and logic for reduced losses during overload conditions. Preset undervoltage lockout thresholds of 17/10 volts are optimized for off-line designs, but are easily reprogrammed by the user for other applications.

Each of the UC3860 functions are utilized in this design and have been previously highlighted in the references. Zero current detection and switching is performed by connecting the uncommitted comparator's output to the one shot timing network, a technique which allows a programmed maximum on-time that can be modulated as zero current is crossed. Any propagation delays can effectively be "nulled-out" with the addition of anticipator circuit detailed in references 1 and 2. A programmable restart delay following the receipt of a fault condition, often referred to as "hic-cup" has been incorporated in addition to soft start, which gradually increases the conversion frequency in a resonant converter. The UC3860 provides complete regulation and control for this 150 watt design over all line and load combinations.

CLOSING THE LOOP

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

BLOCK DIAGRAM - CONTROL LOOP



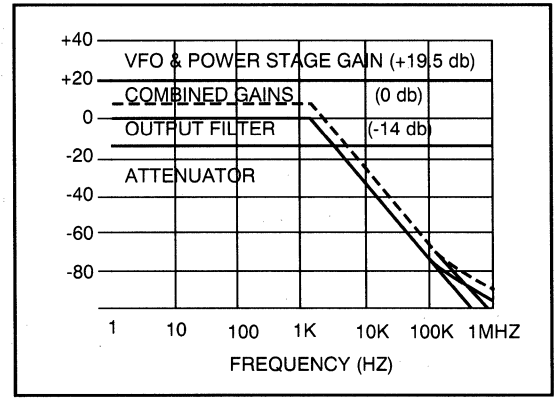
POWER STAGE

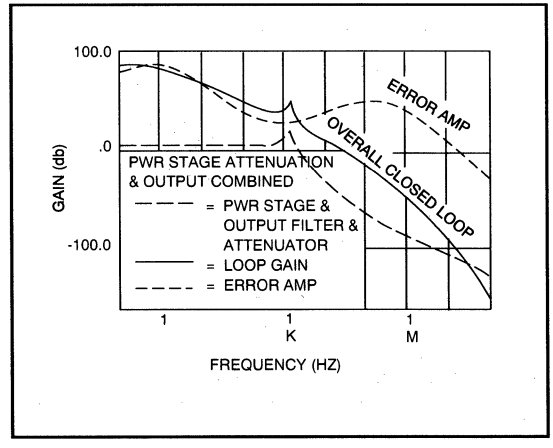
The small signal gain of the power stage will be approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch on-time is constant, and any changes in frequency directly effect the off-time, or resonant capacitor discharge time. Additionally, both Vin and Iout are assumed to be constant during the interval of interest.

Tabulated below at several points of interest are the values for this gain, obtained from the results of previous sections for work done in the references. The gain of the power stage (in volts per hertz) varies significantly over the input and output ranges, and the highest value will be used to approximate the worst case condition.

V IN sec(V)	I OUT (A)	Win uJ/cyc	F conv KHZ	GAIN Vusec	GAIN (db)
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	10.7	20.6
22	7.5	78	900	9.65	19.7
38	7.5	185	450	11.3	21.1
22	10	91	1000	9.55	19.6
38	10	205	560	11.8	21.5

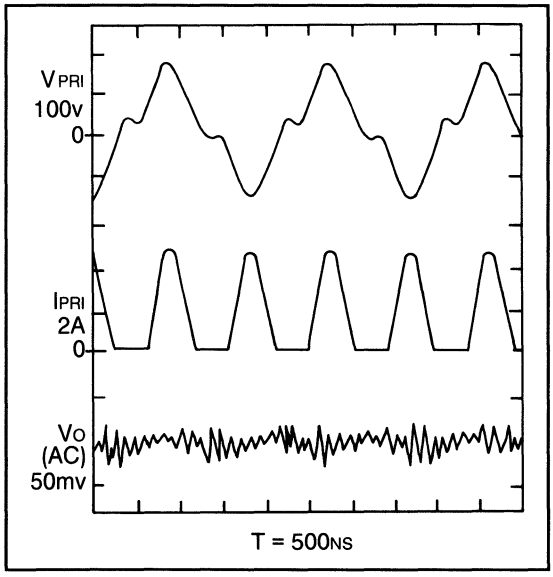
A slightly greater than worst case value of 23 volt-microseconds will be used for the power stage. Multiplying this by the VFO gain of 0.4 Mhz/v results in an combined gain of 9.2 Vout / Vea out.





POWER SUPPLY PERFORMANCE

This 150 watt quasi-resonant supply performed flawlessly over its specified parameters, attaining the overall full load efficiency goal of 80%, however, only at low line. A decrease to 75% was seen as high line was approached, an indication that more attention to high dV/dt losses should be exercised. Nevertheless, low switching noise, quasi-sinusoidal power waveforms and substantially reduced EMI are worthwhile benefits, especially over conventional square wave converters. The relavent primary voltage and current, in addition to secondary voltage waveforms are displayed. These plots were obtained using a 250 MHz bandwidth digitizing scope, UHF measurement techniques and no bandwidth limiting or waveform averaging to distort the high frequency components.



Construction of the power conversion stage was accomplished using the Unitrode UC3860 demonstration kit printed circuit board, with ample facilities to accomodate a variety of quasi-resonant topologies and configurations. The control section was built using the UC3860 evaluation kit p.c. board, and interconnections to the gate drive and current sense transformers made with 75 ohm coaxial cables. An auxiliary winding from the main transformer and opto-coupled feedback were later added to this design for complete primary to secondary isolation.

SUMMARY AND CONCLUSIONS

The ultimate blend of high power density with high efficiency and low noise is realizeable today using quasi-resonant techniques, conventional topologies and existing components. In most applications, the upgrade is quite simple, as many of the devices go unchanged in the process. The control circuit, on the other hand, requires a far more sophisticated controller than for its square wave predecessors. Additionally, as switching frequencies are further pushed towards and beyond a megahertz, the needs for even higher performance and higher speed control logic become increasingly obvious. The UC3860 resonant mode controller exceeds these requirements, simiplifying and condensing the control circuit design process to resistor and capacitor value selections.

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5. MAMMANO, R. "Resonant Mode Converter Topologies", Unitrode Power Supply Design Seminar: SEM-600A

6. WOFFORD, L. "UC1860 - New IC Controls Resonant Mode Power Circuits", APEC 1988

7. Unitrode IC Corp. acknowledges and appreciates the use of this paper from the 1990 "High Frequency Power Conversion" conference.

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NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS

Bill Andreycak
UNITRODE Integrated Circuits Corporation, Merrimack, N.H.

ABSTRACT

Although touted as a high impedance, voltage controlled device, prospective users of Power MOSFETs soon learn that it takes high drive currents to achieve high speed switching. This paper describes the construction techniques which lead to the parasitic effects which normally limit FET performance, and discusses several approaches useful to improve switching speed. A series of drivers ICs, the UC3705, UC3706, UC3707 and UC3709 are featured and their performance is highlighted. This publication supercedes Unitrode Application Note U-98, origionally written by R. Patel and R. Mammano of Unitrode Corporation.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFETs have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process, opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extemely fast switching. Not only is there no storage time inherent with MOSFETs, but the switching times can be user controlled to suit the application. This, or course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFETs are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSEFT can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell - a high power device such as the IRF 150 would have ≈ 20,000 of these cells all connected in parallel.

In operation, when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N-drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N-drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

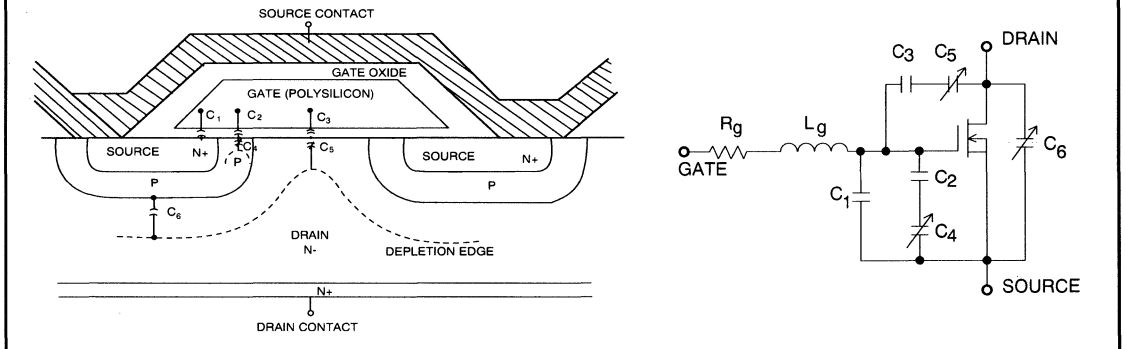


FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

9

In the equivalent model, the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is dielectric capacitance and is fixed while C4 is due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inducitve switching of a large class of applications and is implemented here with a IRF-510 FET, which is a 4 amp, 100V device with the following capacitances:

Ciss ≈ C1 + C4 + C5 = 135 - 150 pF

Crss ≈ C5 = 20 - 25 pF Vgs = 0V

Coss ≈ C5 + C6 = 80-100 pF

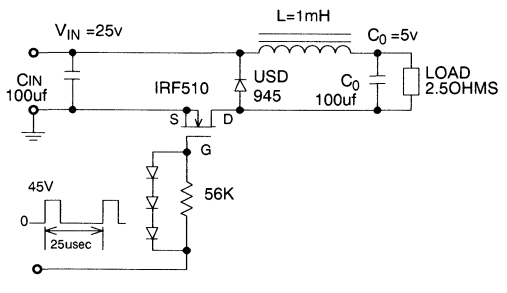


FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration, the load portion of the circuit is established with Vin = 25V. Io = 2A. and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

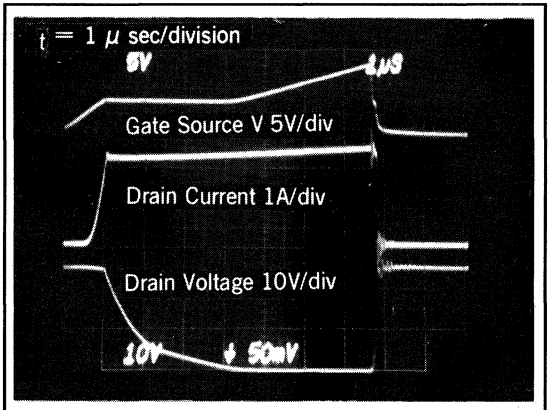


FIGURE 3-FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise tiime is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a significant jump when the drain-gate potential reverses polarity.

6. Unless limited circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold. C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transfered from the free-wheeling diode to the FET.

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

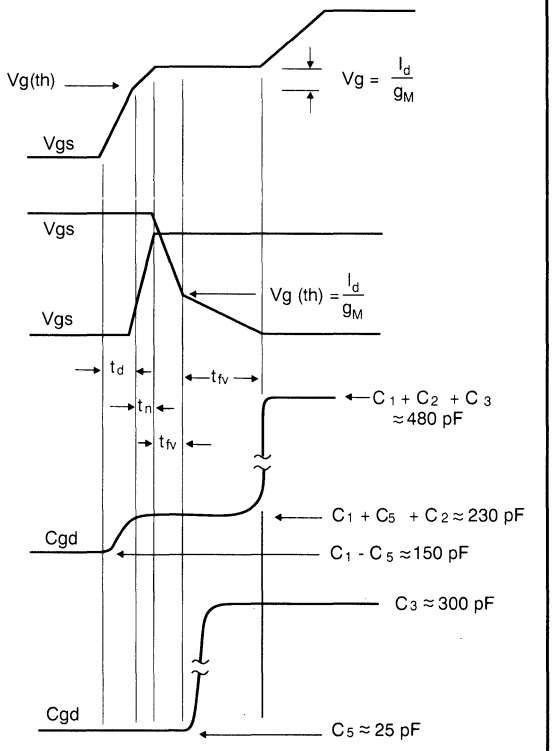


FIGURE 4 - Parasitic CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

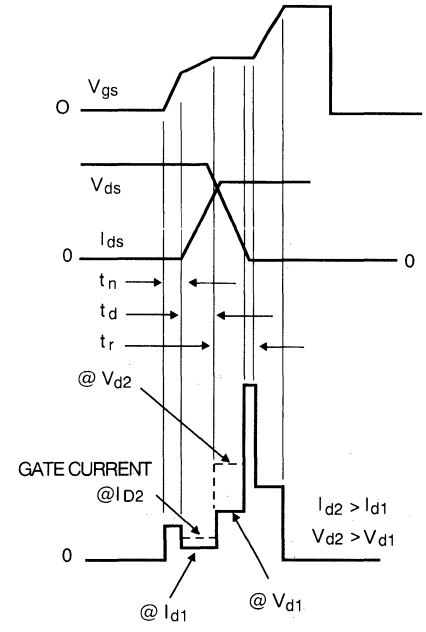


FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

AN OPTIMUM GATE DRIVE

In most switching power supplly applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements

1. An initial fast pulse to get the gate voltage up to threshold.

2. A lesser amount to slow the drain current rise time. This value however, will also be a functiion of the required drain current.

3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.

4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approximated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \qquad \text{where we define } ton = td + tn + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg\,(th) - \frac{Id}{g_M}] - Crss\,[V_{DD} - Vg\,(th)] - CrssV_g\,(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'≈1.5 Ciss. With this assumption.

$$Ip \approx \frac{2}{ton}[Ciss\,(2.5Vg\,(th) + \frac{Id}{g_M}) + Crss\,(V_{DD} - Vg\,(th))]$$

As an example, if one were to implement a 40 V. 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimum drive current for this application would then take 50 nsec to ramp from zero to peak value calculated from

$Ciss = 2000pF$ $\quad ton = 50nsec$
$Crss = 350pF$ $\quad v_{DD} = 40V$
$Vg\,(th) = 3V$ $\quad Id = 10A$

$$g_M = \frac{10A}{2.5V} = 4s$$

$$as\ Ip = \frac{2}{50 \times 10^{-9}}\,[2000 \times 10^{-12}\,(2.5 \times 3 + \frac{10}{4}) + 350 \times 10^{-12}\,(40 - 3)]$$

$\therefore\ Ip = 1.32\ amps\ peak$

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

TOTAL GATE CHARGE (Qg)

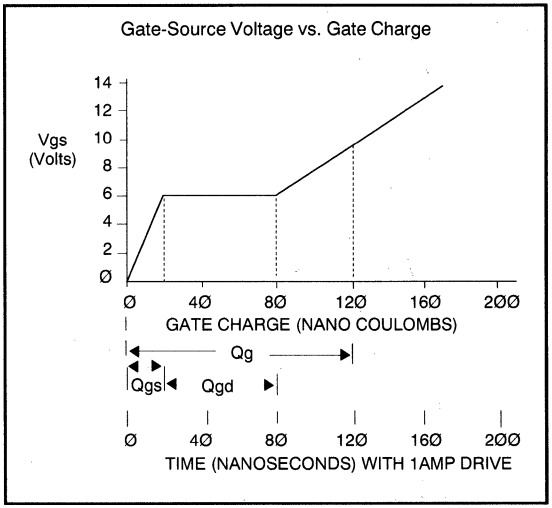
Another approach used to quantify and understand MOSFET gate drive requirements is much simpler than that of examining the instantaneous voltages, currents and capacitances. The term "Total Gate Charge", or Qg specifies the amount of gate charge required to drive the FET gate-to-source voltage (Vgs) from zero to ten volts, or vice-versa. For most high voltage devices, these thresholds correspond to the FET being either completely on or off.

Charge (Q) can be expressed as the product of either current multiplied by time (I*T), or capacitance multiplied by voltage (C*V) in the units of Coulombs. Most contemporary devices have total gate charge requirements in the tens to low hundreds of nano Coulombs, dependent almost entirely on die's geometry. For example, an IRF710 (size 1) FET has a total gate charge requirement of only 7.7 nC whereas the IRFP460 (size 6) demands 120 nC, and both are typical values.

PARAMETER	IRFP 440	IRFP 450	IRFP 460
Qgs (NC)	6.2	11	18
Qgd (NC)	22	43	62
Qg (NC)	42	86	120
Ciss (Nf)	1.3	2.7	4.1

There are two specified parameters contained within the total gate charge expression; Qgs, the gate-to-source charge, and Qgd the gate-to-drain, or "Miller" charge. Qgs is the amount of charge required to bring the gate voltage from zero up to its threshold VGS (th), of approximately 6 volts. Qgd defines the amount of charge that must be input to overcome the "Miller" effect as the drain voltage falls. This occurs during the plateau of the gate-to-source voltage waveform where the voltage is "constant". Excess charge is added to lower the effecive Rds (on) until the gate voltage reaches 10 volts, wher Qg is specified. Further increases above this level do NOT lower Rds (on), so a 10-12 volt driver bias is ideal.

The total charge curve can be examined in sections to define the ideal driver's characteristics. Using a constant current of 1 ampere, the total charge curve (Qg=I*T) in nanoCoulombs also represents the MOSFET turn-on delay, drain current rise and drain voltage fall times in nanoseconds.



First of all, and most importantly, the average capacitive load represented by the FET to the IC driver is NOT the specified MOSFET input capacitance, Ciss. The effecive input capacitance, Ceff, is the total charge divided by the final gate voltage, Vgs(f);

Ceff = Qg(total) / Vgs(f).

Using the total gate charge curve show above, the 460 FET with Vds (off) = 400 volts has an effective input capacitance (Ceff) of approximately 120nC/10v, or 12 nF during the interval of 0 < Vgs < 10v. The specified input capacitance of Ciss = 4.1nF applies only at Vgs=0, and is often mistaken for the driver's actual load.

The Qgs portion of the curve is primarily governed by the driver's ability to quickly turn ON. Therefore, a sharp, fast transition of the totem-pole output from low to high is essential to minimize the delays from 0 < Vgs < VGS (th). In most applications the driver IC is not peak current limited during this interval, since its is more likely to be dV/dT limited. The effective gate (load) capacitance is approximately Qgs / VGS(th), or Ciss.

Evident from the charge specifications, most of the popular size FETs used in switch-mode power supplies (sizes 4. 5 and 6) have much larger Qgd demands than their gate-to-source counterpart, Qgs. During this Qgd interval, the gate voltage remains "constant" while gate charge accumulates and the drain voltage collapses. It is also during this period that most drive circuits are simply peak current limit, whether by the driver IC or an external resistor. High peak currents are necessary for fast transitions through this interval, especially when driving large geometry FETs.

Full drain current is flowing at the beginning of the Qgd portion of the Qg curve, and notice that the drain voltage remains high. FET power loss is at its maximum here, and decreases linearly with Vds. A majority of the Qgd charge goes to combat the "Miller" effects as the drain voltage falls from that of its off condition to Vgs, or approximately Vgs(th). The remainder of the charge is used to bring the drain voltage down below that of the gate, decreasing the

effecive gate capacitance over the Qgd interval since there is relatively no change in gate voltage. The important fact, however, is that high peak currents are needed to minimize the FET power loss and transition time.

The remainder of the gate charge brings the gate voltage from VGS (th) to 10 volts. This "excess" charge reduces the FET "ON" resistance to its minimum, and raising the gate voltage above 10 volts has no further effect on reducing the Rds (on). The effective gate capacitance, which is high, can be obtained by dividing the charge input by the change in gate voltage during this region.

Ceff = [Qg - (Qgd+Qgd)] / (10v - VGS (th)) = 40nC/4v = 10nF for the IRFP460

FET DRIVER ICS

In searching for IC's capable of providing the fast transitions and high peak currents required by power MOSFETs, one of the first devices which became popular was the DS0026. While this IC was origionally designed to be dual clock driver for MOS logic, it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all NPN process which minimizes storage delays, and as a result, offers transition times of approximately 20 nsec. Its disadvantages, however, are high cross conduction currents, as well as requiring excessive supply current when the output is in the low (OFF) state. This leads to higher power dissipation and junction temperature than optimum.

This brings us to newer ICs designed specifically as power MOSFET drivers for switchmode power supply applications. Several factors were taken into consideration while developing the new UC3705/06 /07 /09 series of high current drivers; the most important of which, was to isolate the high power switching noise from the low level analog signals at the PWM. Seperate supply and return paths at the driver to its signal inputs and power outputs further enhances noise immunity. Additionally, several desireable features including an analog shutdown comparator have been incorporated in the UC3706 and UC3707 devices, whereas the UC3705 and UC3709 drivers are optimized for low cost applications which incorporate this function elsewhere in the design. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross-conduction, high speed output circuitry. The corresponding block diagrams and pin assignments are shown in figures 6 thru 9, and followed by the feature selection index.

UC3705 Block Diagram

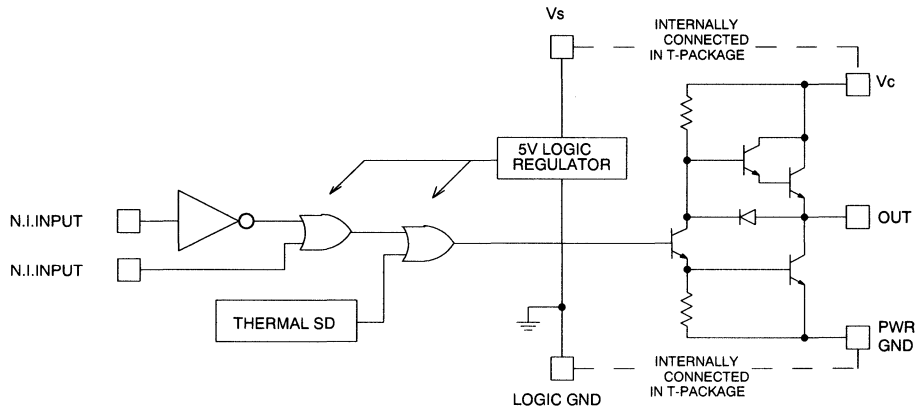


Figure 6

UC3706 Block Diagram

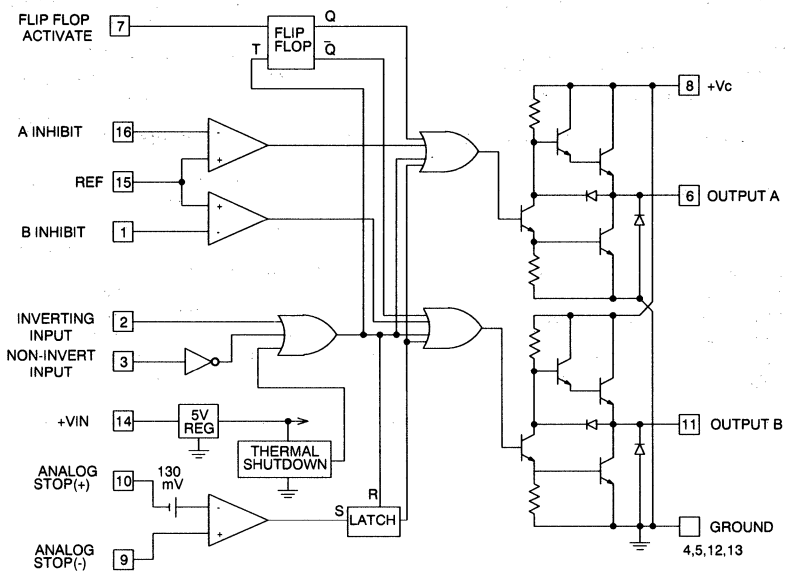


Figure 7

UC3707 Block Diagram

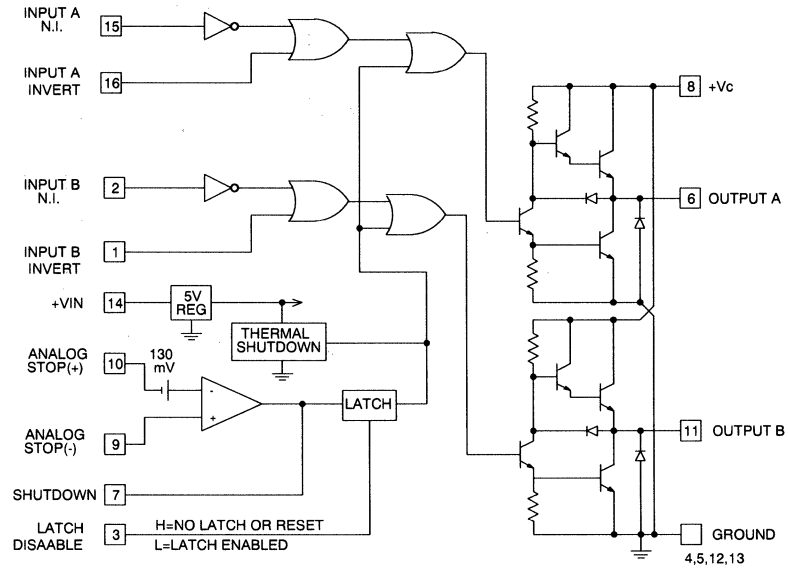
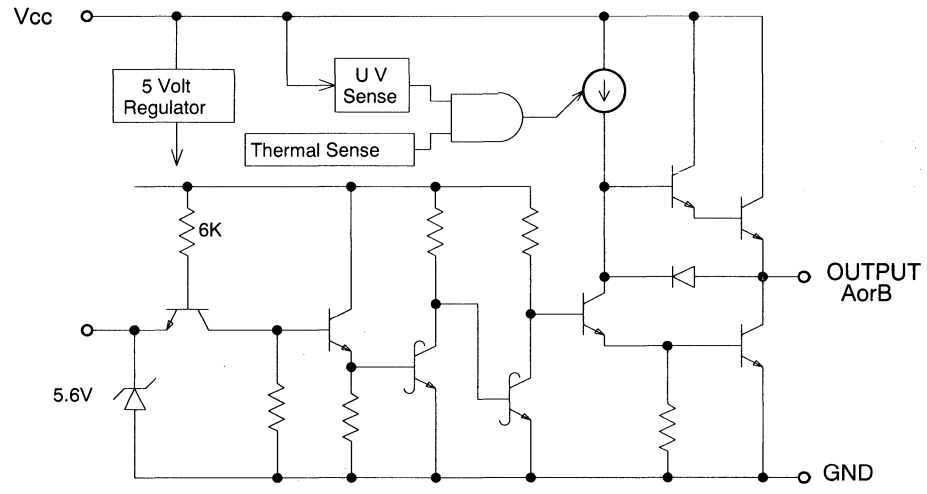


Figure 8

UC3709 Block Diagram



NOTE: One Output Shown

Figure 9

DRIVER FEATURES

- 1.5 Amp Peak Output Current (Per Output)
- 40 Nanosecond Rise & Fall Times into 1NF
- Low Cross Conduction Current Spike
- 5 to 40 Volt Operation
- High Speed Power MOSFET Compatable
- Thermal Shutdown Protection

	DUAL OUTPUTS	INVERTING INPUTS	NON-INVERTING INPUTS	SEPERATE V_C & V_{IN}	SEPERATE PGND & SGND	ANALOG SHUTDOWN	DIGITAL INHIBIT	TOGGLE F/F	LATCH RESET
UC3705		X	X	X	X				
UC3706	X	X	X	X	X	X	X	X	
UC3707	X	X	X	X	X	X	X		X
UC3709	X	X							

1.5 AMP PEAK TOTEM-POLE OUTPUTS

The schematic of the UC3706 output drive circuit is shown in figure 10, which is similar to the other devices in this family. While first appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in figure 11 where it can be seen that while maintaining fast transition times, the cross conduction current spike has been reduced to zero when going low and only 20 nsec with a high transition. This offers negligible increase in internal circuit power dissipation at frequencies in excess of 500KHz.

Typical Output Schematic

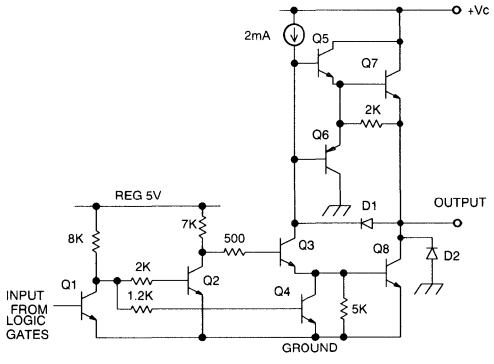


Figure 10

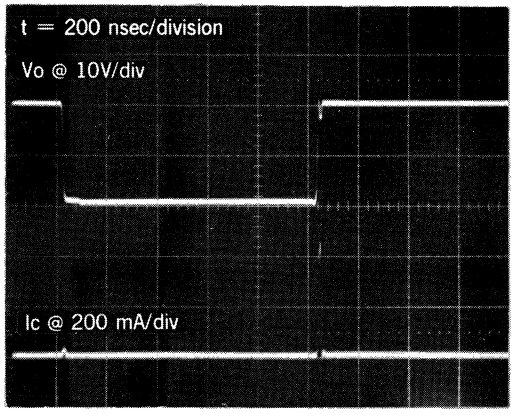


Figure 11

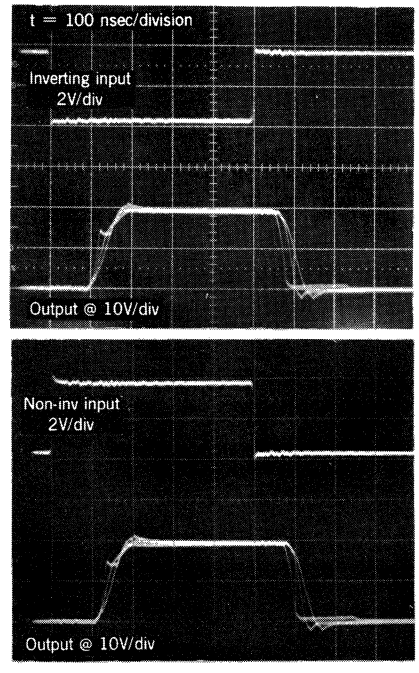


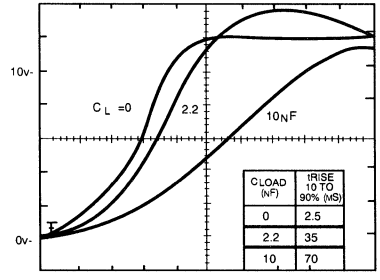
Figure 12

The overall transition time through the UC3706 is shown in figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20 nSec delay in turning off when the non-inverting input is used. Here, and in further discussions note that ON and OFF relate to the driven output switch, i.e., On is with the output HIGH, and vice versa. The shutdown, inhibit and protective functions all force the output LOW when active.

Note that the typical rise and fall times of the output waveform average 20 nsec with no load, 25 nsec with 1 nF, and 35 nsec when the capacitive load is 2.2 nF at room temperature. Multilayer ceramic capacitors are used in this test and located as physically close to the IC output as possible to minimize lead and connection inductance.

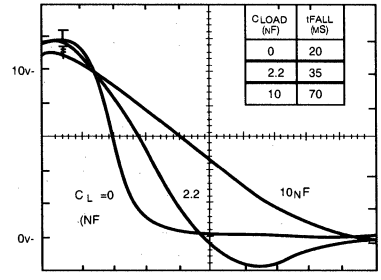
RISE TIMES
INTO 0, 2.2 & 10NF.
(10 TO 90% Vcc)

V=2v/DIV
H= 10NF/DIV
BOTH.



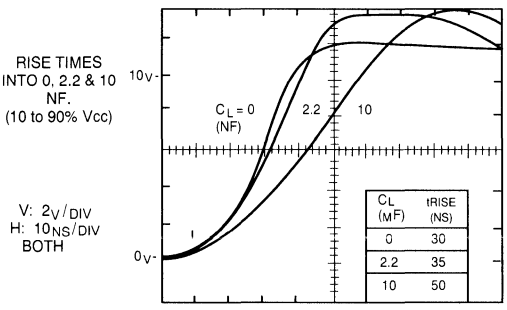
CLOAD (NF)	tRISE 10 TO 90% (MS)
0	2.5
2.2	35
10	70

FALL TIMES
(90 TO 10% Vcc)



CLOAD (NF)	tFALL (MS)
0	20
2.2	35
10	70

Figure 13



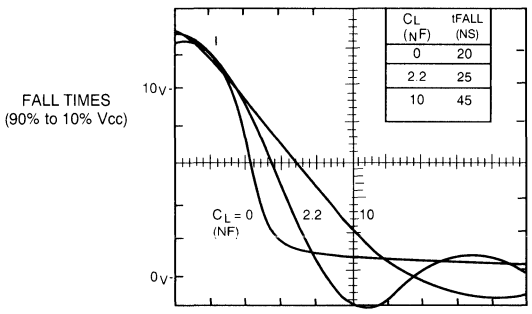
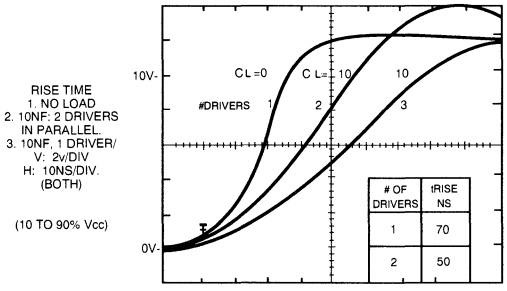


Figure 14



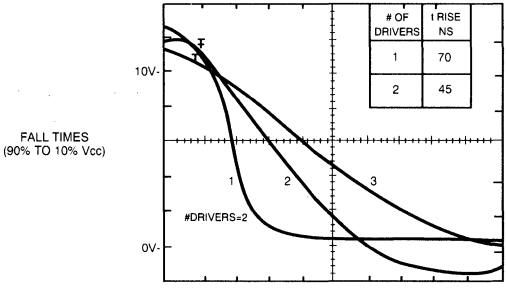


Figure 15

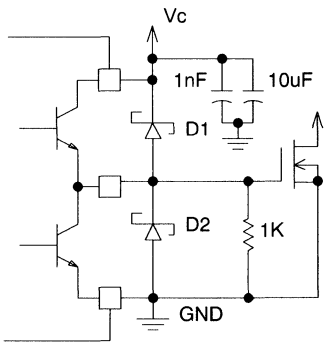
The peak current of each totem-pole output, whether source or sink, is 1.5 amps. However, on dual output versions like the UC3706, UC3707 and UC3709, both of the outputs can be paralled for 3 amp peak currents. In close proximity on the same die, each output virtually shares identical electrical and thermal characteristics. Saturation voltage is high at this current level but falls to under 2V at 500ma per output. Examples of typical switching characteristics are displayed.

It should be noted that while optimized for driving power MOSFET device, the UC3705 /06 /07 /09 ICs perform equally well into bipolar NPN transistors. In a steady-state off condition, the output saturation voltage is less than 0.4 volts as currents to 50 milliamps.

DIRECT COUPLED MOSFET DRIVE

The circuit of figure 17 shows the simplest interface to a power mosfet, direct coupling. In this example, an IRFP460 will be used to demonstrate the typical rise and fall times obtainable with a single 1.5 amp peak totem-pole driver. Further testing will include paralleling both outpus of a dual driver for a 3 amp peak capability. The IRFP460 device was selected, being the largest commercially

POWER MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODES

Figure 16

9

available FET die (a size "6") at the time of this writing whose specifications were listed previously.

The typical values of each charge will later be used in conjunction with the measured driver performance to estimate the actual peak current delivered during each interval of turn-on. The tests shown were conducted at room temperature with the FET located directly at the IC output pins to nullify any effects of series inductance. Additional tests and measurements will demonstrate the effects of circuit inductance on gate driver performance.

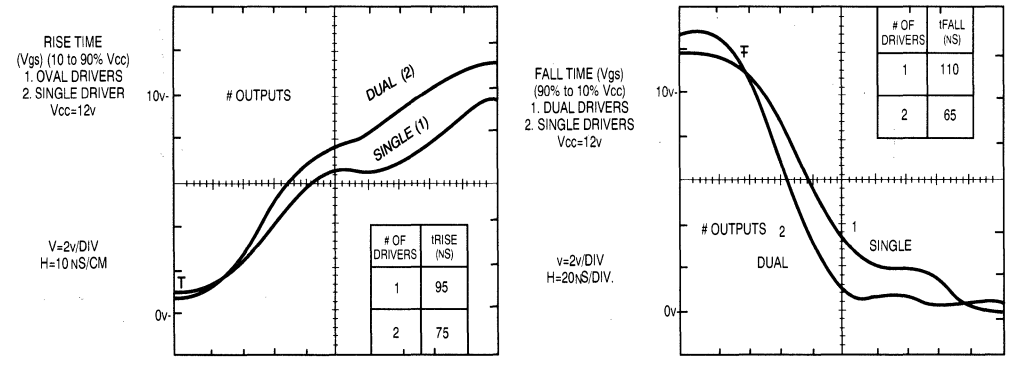


Figure 17

AVERAGE DRIVER CURRENTS DURING TURN-ON & TURN-OFF INTERVAL

EQUATIONS: $Q = CV$; $Q = IT$; $i_{AVG} = \frac{C.V}{T}$

During the transitions between 0 & 10V over Tr & Tf intervals

SINGLE OUTPUT

LOAD	RISE	FALL
C = 2.2NF	0.49A	0.67A
C = 10NF	1.43A	1.43A
IRFP460	1.26A	1.10A

DUAL OUTPUTS

LOAD	RISE	FALL
C = 2.2NF	0.63A	0.88A
C = 10NF	2.0A	2.22A
IRFP460	1.6A	1.85A

While directly connecting the FET gate to the output of the driver is straightforward for testing purposes, it does not represent the "real" application which may include several inches or wire or printed circuit board traces. Here, wiring inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. Extreme examples of this can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings.

Additionally, negative transitions (below ground) at the deriver output can raise havoc with the internal circuitry, leading to undesireable performance. While this is more of a concern with PWMs, (which use low level analog input signals) it will also detract from the drivers peak performance. Both of these conditions can easily be avoided by Schottky clamping the circuit to the auxiliary supply rails.

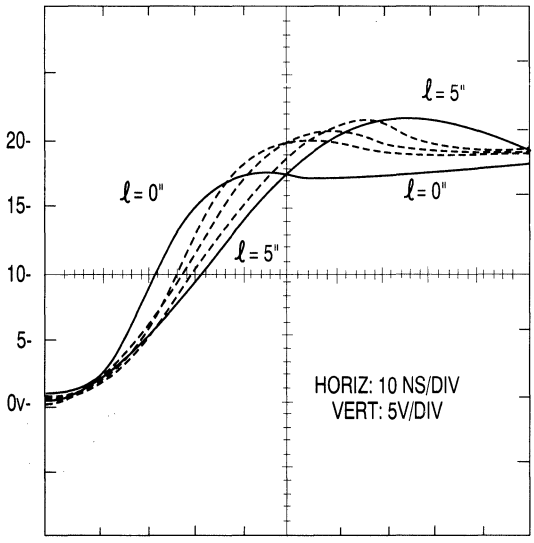


Figure 18

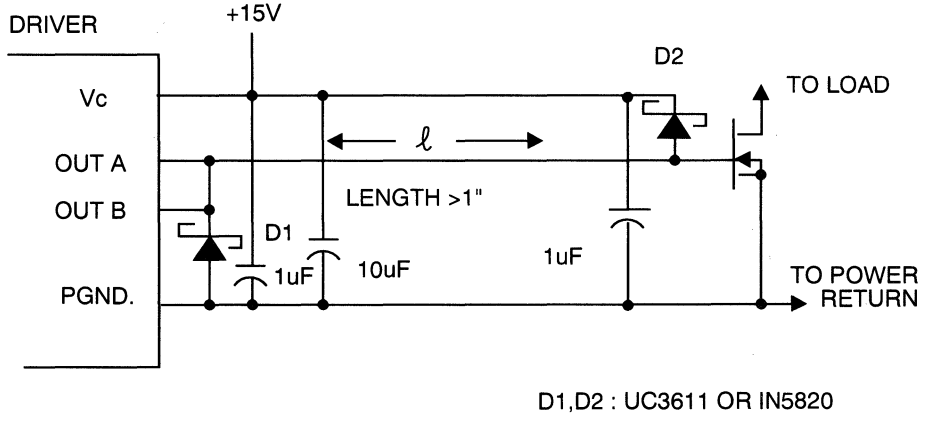
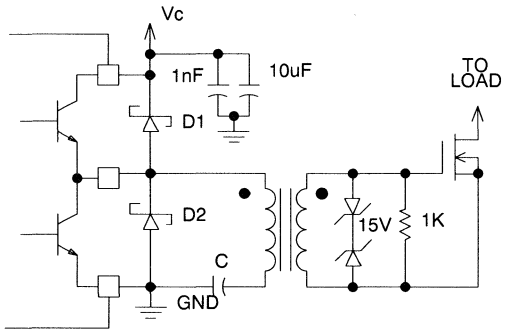


Figure 19

ISOLATED GATE DRIVE

In certain applications, the PWM is referenced to the load or secondary side of the power supply and the gate drive is transformer coupled across the isolation boundary to the power FETs. While this technique may work adequately at low switching frequencies, any series circuit inductance, as shown, will significantly degrade switching speeds and performance as the frequency is increased. An improved version of this circuit locates the drivers on the primary side, as close as possible to the FETs, and transformer couples only the low power input signals. Although somewhat more elaborate, significant improvements in turn-on and turn-off switching times are obtained and the FET switching losses are minimized.

TRANSFORMER COUPLED MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODE ARRAY

Figure 20

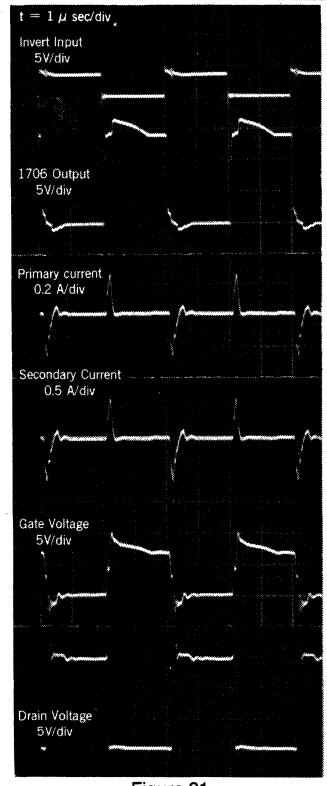


Figure 21

IMPROVED XFMR COUPLED DRIVE CIRCUIT

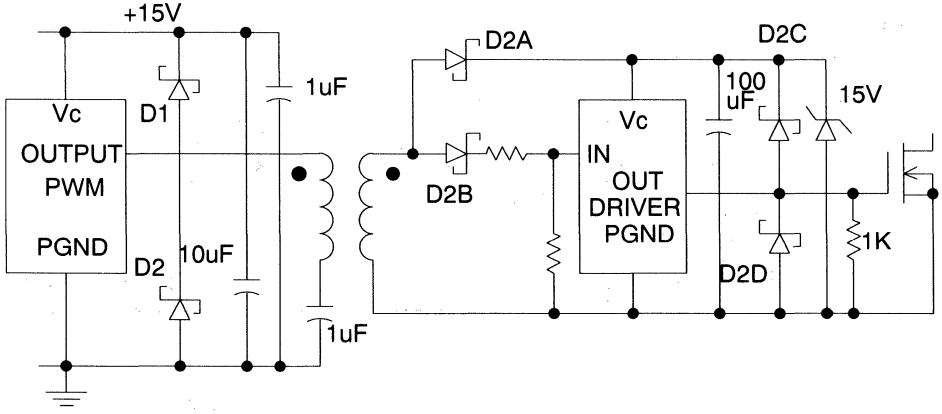


Figure 22

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC3706 can easily be configured for implementing the balanced transformer drive as shown in figure24. Outputs A and B are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC3706 output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back-to-back zeners on the secondaries are necessary to minimize the overshoot causes by the ringing of the gate capacitance with circuit inductances. Waveforms of all significant points within this circuit are shown.

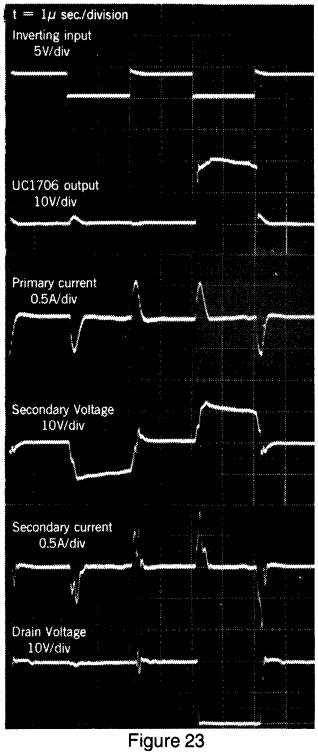


Figure 23

UC 3706 CONVERTS SINGLE OUTPUT PWMS TO HIGH CURRENT PUSH-PULL CONFIGURATION

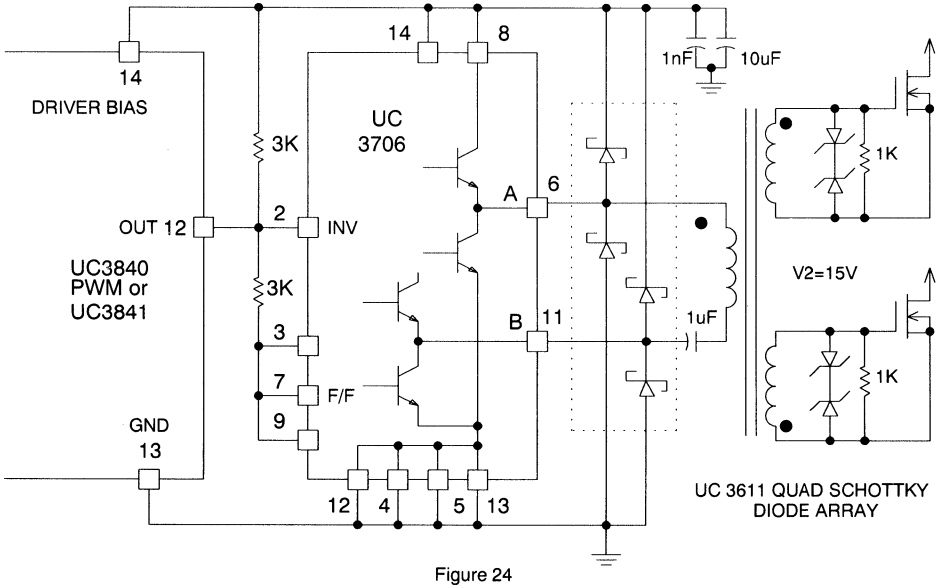


Figure 24

SUPPLYING POWER TO THE DRIVERS

From the block diagrams of figures 6 thru 8, note that the UC3705, UC3706 and UC3707 have two supply terminals, Vin and Vc. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Therefore, Vin can also be used to activate the outputs and no current is drawn from Vc when Vin is low. This is useful in off-line applications where its desireable for the control circuit to have a low start-up current. Several PWM controllers, like the UC1840, UC1841 and the UC1851 feature a Driver Bias output which goes high once the undervoltage lockout threshold is crossed, thus supplying bias to the driver. Adaptations of this technique can be made to work with a variety of other PWMs and control circuits.

USING "SPLIT" SUPPLIES

Many applications utilize a negative voltage rail in the drive circuit to guarantee complete turn-off of power MOSFETs, especially those with low gate threshold voltages, typical of "logic level" input devices. This is easy to implement with any of the UC3705 thru UC3709 drivers by offsetting the input signals with a zener diode equal in voltage to the negative supply, Vee. Although referenced at the driver IC to the Vee rail, these inputs are offset by an equal amount to the PWM controller, simulating a ground referenced input. This technique also offers moderate improvements in FET switching speeds at the penalty of slightly increased effective delay times from the driver inputs. The end results are listed below, which may be beneficial in applications where a tailored gate drive is required to alter the MOSFET switching charcteristics.

POWER MOSFET DRIVE CIRCUIT
USING NEGATIVE BIAS VOLTOGE AND LEVEL SHIFTING
TO GROUND REFERENCED PWMS

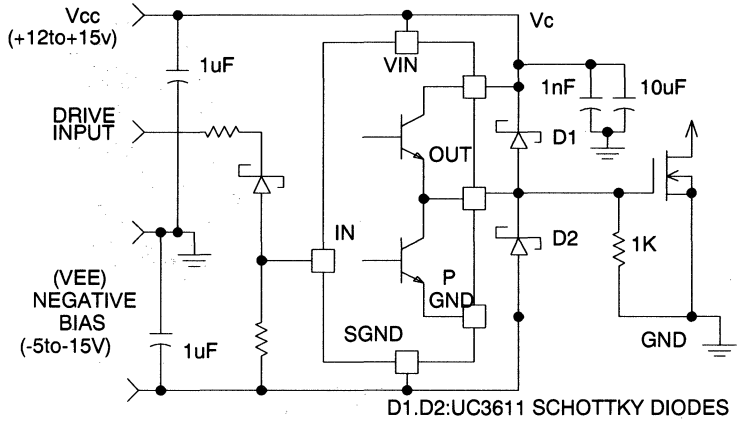


Figure 25

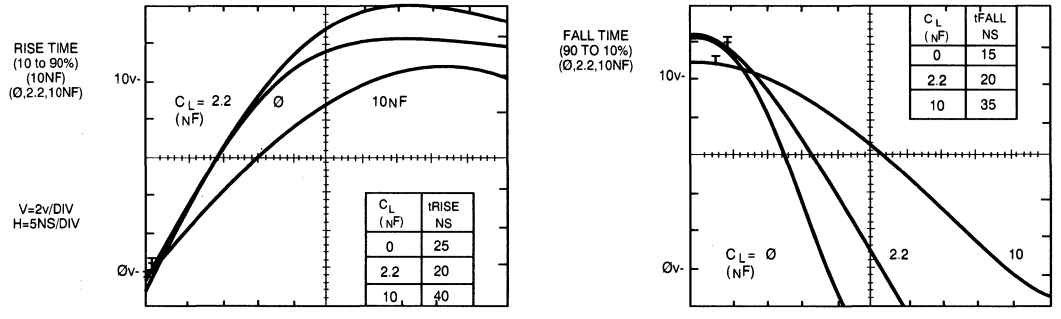


Figure 26

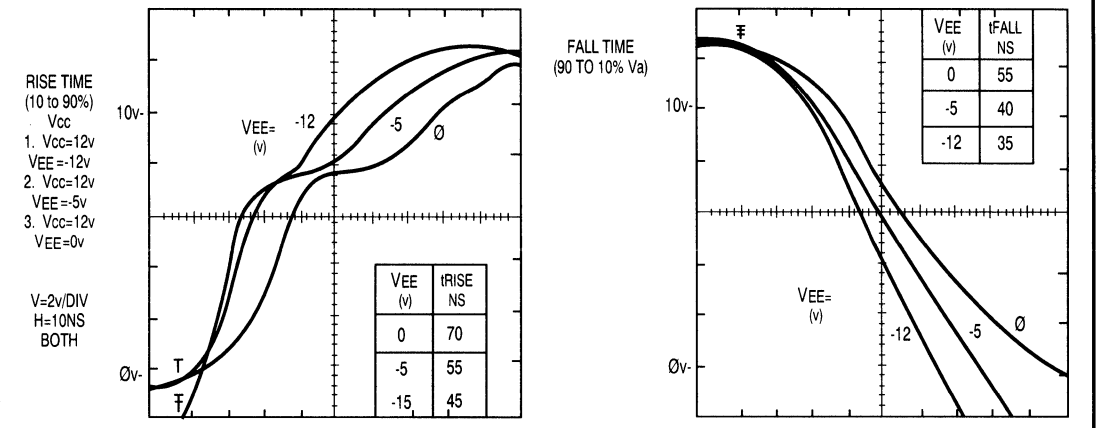


Figure 27

VEE (V)	td Rise to '0" V (NS)	T Rise 0-10V (NS)	Td Fall to begin (NS)	T Fall 10-0V (NS)I	T Delay total (NS)	Tr & Tf total (NS)	T Total tr+tf+trd (NS)
0	56	50	50	45	106	95	201
-5	70	42	50	33	120	75	195
-10	86	34	50	29	136	63	199
-12	93	32	50	28	143	60	203
-15	100	30	50	27	150	57	207

VEE (V)	Delay trd+tfd (NS)	Transition Times tr+tf (NS)
0	Minimum (106NS)	Maximum (95NS)
-15V	Maximum (143NS)	Minimum (60NS)

VEE (V)	Rise	Fall
0	2.4A	2.67A
-5	2.86A	3.64A
-10	3.53A	4.14A
-15	4.0A	4.4A

SUMMARY

This paper has presented an understanding of the dynamics of high speed power MOSFET switching in an attempt to define the optimum gate drive requirements to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed towards achieving these goals. The UC3705, UC3706, UC3707 and UC3709 drivers provide high speed response, 1.5 amps of peak current per output and ease the implementing of either direct or transformer coupled drive to a broad range of power MOSFETs. With these new devices, one more specialized function has been developed to further aid the power supply designer simplify his tasks and enhance power MOSFET switching characteristics.

9

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INTEGRATED
CIRCUITS
UNITRODE

DRIVING THREE-PHASE BRUSHLESS DC MOTORS — A NEW LOW LOSS LINEAR SOLUTION

Robert A. Mammano, V.P. Adv Tech, Unitrode IC Corp and

John J. Galvin, Control Systems Eng, Quantum Corp.

ABSTRACT

A new linear driver for small Brushless DC motors has been developed which has the capability of maximizing the voltage delivered to the motor while additionally providing commutation logic and full control. By using discrete PNP high-side transistor switches in conjunction with integrated saturable NPN low-side drivers, less than one volt total loss can be achieved at currents up to two amps, and complete motor control can be derived from only a five volt power source.

BRUSHLESS DC MOTORS

Although the world has long known of the myriad problems with brush-type DC motors, the development of electronically commutated, or "Brushless" (BDC), motors has not been a simple transition. While Hall Effect sensors have developed to the point where accurate and reliable armature position information can now be readily derived, the problems of amplifying these low-level signals, applying them to the appropriate winding, and then driving that winding with an efficient power transfer still represent a significant challenge. Particularly when this intervening circuitry - none of which was required with brush-type motors - also has to be reliable, very low cost, noise free, and take up minimal space. The problem is further compounded by the need to provide three-phase drive for all but the simplest, specialized motors in order to accommodate bidirectional rotation and wide variations in speed and load.

For complete control of a brushless DC motor, the circuitry must provide at least three functions:

1. Commutation logic to generate the correct phase timing from the Hall sensors. In most cases, this is implemented as a digital decoding function.

2. Power drivers for each of the three output phases. The challenge here is finding a solid state switch as efficient as the old commutator brush.

3. Control circuitry to give the motor some intelligence. This usually means controlling motor current in response to commands based on speed, position, torque, or some other measurable output.

THE SPINDLE DRIVE PROBLEM

Providing the above functions as a spindle driver for rotating memories represents an additional challenge as disk drive users have come to expect the package density and low costs of an integrated driver while at the same time demanding ever higher operating efficiencies to minimize the requirements on power supplies and heat sinks.

While discussing drive efficiency, it is worth noting that disk drives add a further restriction due to the magnetic media and low signal levels involved. This is that the use of switch-mode technology to increase power control efficiency is usually forbidden out of concerns for possible high-frequency EMI noise. Ruling out switch-mode techniques leaves the designer faced with the problem of providing maximum efficiency with linear current control, and thus his quest for power savings can only be directed toward minimizing the drop across the output switches in order to use the highest efficiency motor.

THREE PHASE MOTOR DRIVE

The drive stage for a typical brushless DC motor is shown in Figure 1 where the motor is shown wound in the "Y" configuration. A "delta" form is equally applicable and would make no difference to the switches. The driving problem is immeadiatly apparent in that there are six separate switches required and two are in series with any current path through the motor. With a 12 volt supply and typical bipolar darlington switches - each with a probable 1.5 volt drop - the maximum voltage to the motor is nine volts and one fourth of the input power is lost in the switches.

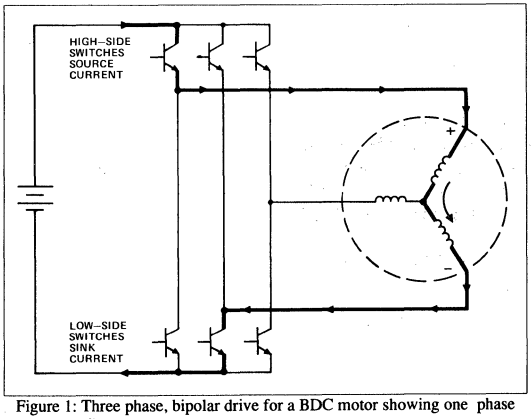

Figure 1: Three phase, bipolar drive for a BDC motor showing one phase of current flow.

These switch voltage drops have added significance in terms of optimizing the motor design since the maximum current through a given motor is defined by the difference between the voltage applied to the motor and the back EMF generated while it is running. Reducing the voltage drop across the switches allows the use of a motor with a higher torque constant and correspondingly higher back EMF which results in a lower motor current for the same load. Since the power loss in the motor is equal to I^2 times the wire resistance, the gain in overall efficiency is more than proportional. For example, with a three volt switch drop from a 12 V supply, an optimum motor choice might have a back EMF of 8 V and require 4 W of power from the supply to do 2.7 W of work. Reducing the switch drop to one volt would now allow a motor with a back EMF of 10.2 V to be used which, with all other factors remaining unchanged, would require only 3.16 W to do the same work. In other words, a 22% increase in the voltage applied to the motor can result in a 27% increase in motor efficiency. This is in addition to saving 2/3 of the power lost in the switches.

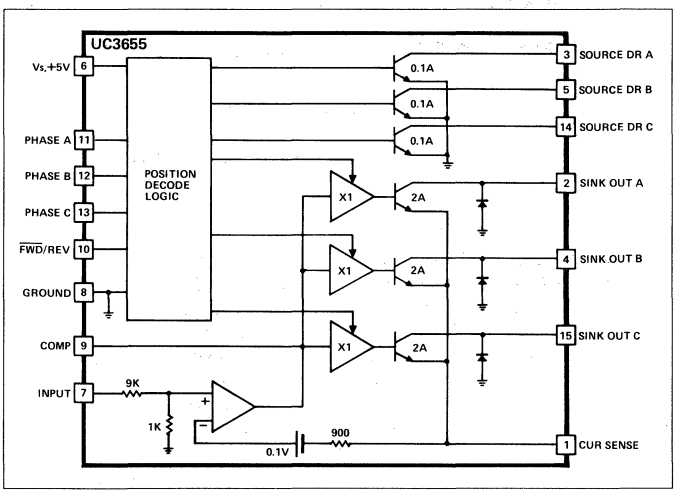

Figure 2: The UC3655 IC provides decode logic, high-current low-side linear drivers under the control of an internal amplifier, and switches to activate high-side, external PNP transistors.

While power MOSFET technology has the potential of offering lower switch losses in discrete form, an integrated monolithic FET structure, while technically feasable, may well be economically impractical. An integrated bipolar transistor scaled for a Vsat of 0.4 V at one amp requires approximately 2000 square mils of silicon, while an integrated DMOS transistor with an Rds(on) value of 0.4 ohms would be closer to 5000 square mils. And it takes six transistors to build a three phase driver. Therefore, a more cost-effective solution would indicate the use of bipolar transistors, but as single saturating switches - not darlingtons.

The low-side switches of Figure 1 are easily integrated in this form as power NPN transistors with their base currents derived efficiently from a five volt power supply. The high-side devices are more of a problem, however, as these need to be PNP transistors to achieve the same low-sat performance, and isolated power PNP transistors are still not compatible with an integrated bipolar process. Thus the decision made for the motor driver described herein was to supply the PNP's as external, discrete saturating switches while the rest of the control circuitry was integrated into a single power IC. The result is the UC3655 illustrated in the block diagram of Figure 2.

THE UC3655 LINEAR BDC MOTOR DRIVER

This device achieves efficient operation by allowing the external PNP's to be selected for the specific application, while internally generating a switched base drive of up to 100 mA - adequate for motor load currents of at least 3 Amps. Because the PNP's are always driven into saturation, their power dissipation will usually be low enough to require no special heat sinking and, in many cases, they may not even need power packages. The only specification of significance for these devices is their saturation voltage for a given base drive. While bipolar PNP transistors are used throughout in this paper, it should be clear that this is a cost consideration and P-channel FET devices could be used as well with the benefit of reduced drive power losses.

The current-limited darlington circuit used for each of the three PNP drivers is shown in the upper portion of Figure 3. This driver is activated by the digital signal from the Channel Select Logic which is defined to allow only one PNP to be on at a time. Note that the total supply current for this stage is a constant 100 uA from the five volt supply for each output.

Each of the low-side motor drivers shown in Figure 3 are, of course, integrated power NPN transistors scaled for a maximum output current of three amps with a very low saturation voltage

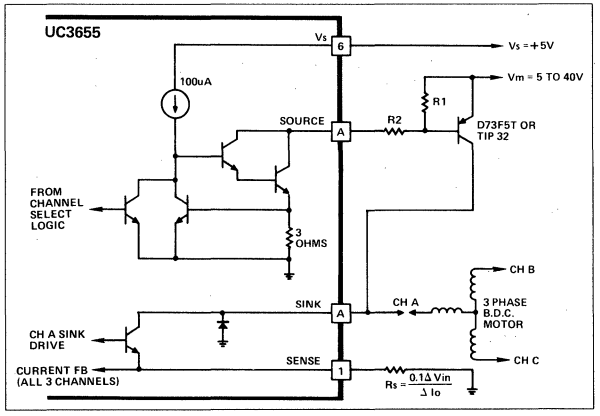

Figure 3: Interfacing the UC3655 to a BDC motor.

drop. At full load, these transistors may need a base drive of up to 50 mA which must come from the five volt supply; however, since they are also used as the means to control the motor current, the action of the control amplifier reduces the base drive as it commands less motor current. The overall schematic of both the amplifier and one of the three low-side drivers is shown in Figure 4.

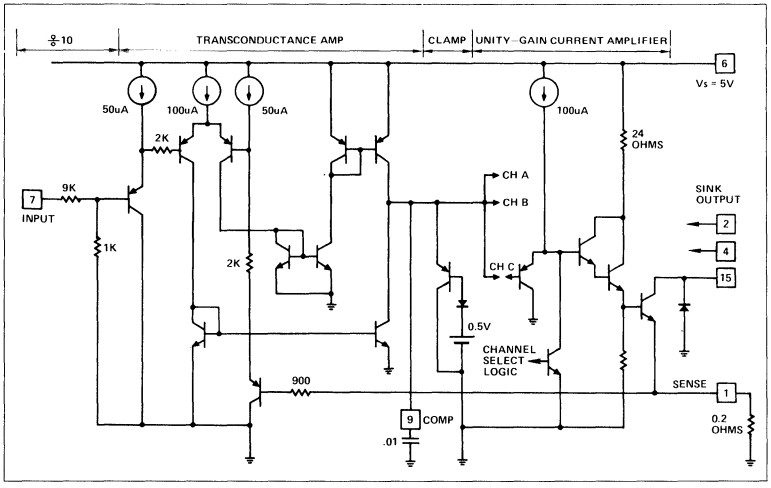

Figure 4: Control of the motor's current requires the four functions shown above, plus the decode logic to define which of the three outputs is active.

This circuitry includes an internal feedback loop to configure the transfer function as a transconductance amplifier controlling motor current from a voltage command. For full control, four functions are included:

1. An input divide-by-ten attenuator to scale a four volt input command range on Pin 7 to a 400 millivolt range across the current sense resistor connected to Pin 1.

2. An amplifier to provide voltage gain. This is also a transconductance type so that the feedback loop may be easily stabilized by a single capacitor from its output on Pin 9 to ground. There is a 100 mV offset built in so that, in conjunction with the input divider, zero output current is commanded with a one volt input.

3. A unity-gain output stage (to the sense resistor) provides the high current output drive with a high input impedance so that the transconductance amplifier is not unduly loaded. Note that the analog command input is gated by the Channel Select Logic so that only one output is on at a time with the other two drivers draining only 100 uA apiece from the supply.

4. A clamp on the output of the transconductance amplifier limits the voltage drop across the sense resistor to approximately 500 mV and thereby provides some measure of over-current protection.

The remaining portion of the UC3655 consists of the decode logic to generate the proper output switch timing from the Hall sensor position indicators. This logic is easily mask programable for other than the standard 60 degree output phasing. The input circuitry to these Channel Select stages has a high impedance, stabilized threshold of 1.5 V and is designed for single-ended, digital-output Hall sensors. For maximum flexibility, pull-up resistors are not included but in niosy environments, should probably be added externally. Where analog, two-terminal Hall sensors are used, the comparator circuit of Figure 5 can be used at each input to give fast, clean transitions.

A fourth input to the decode logic is the direction function addressed through Pin 10. This input circuitry, shown schematicly in Figure 6, has three states:

1. A low input pulls REV low and FWD high, setting up the decoding for a forward rotation.

2. A high input reverses the states of REV and FWD, which the logic decodes as a command for the opposite direction of rotation.

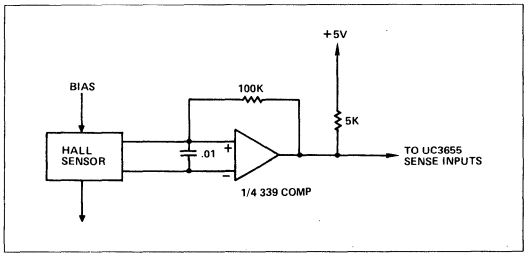

Figure 5: An external comparator added to each sense input will allow the use of low-level, analog Hall sensors.

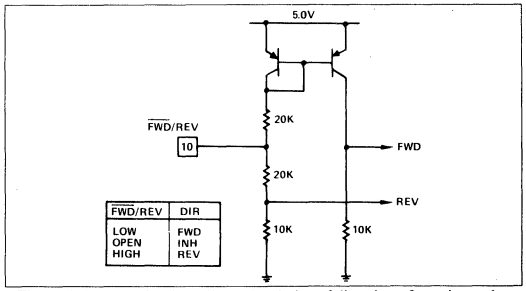

Figure 6: Internal circuitry allows the choice of direction of rotation - plus inhibiting - with a single device pin.

3. If the input is open - or connected to a voltage between 1.8 and 3.2 volts - both FWD and REV are high which the logic defines as a coast condition with all six outputs off.

All outputs are also inhibited if the three Hall inputs are all in the same state, either high or low.

While no braking function is built into the UC3655, it is entirely feasible to provide a rapid deceleration by switching the direction command from FWD to REV with the only precaution being to allow the output transistors to turn off while the command is passing through the INH region. Typically, this might require a 10 usec delay which is easily accommodated with either digital or analog techniques.

It can be seen from the block diagram of Figure 2 that the only supply voltage connection to the UC3655 is a single 5 volt source. From this supply, the quiescent current is less than 10 mA with the outputs inhibited and increases with motor current to approximately 25 mA with a two amp load. The motor voltage is defined by the supply used for the emitters of the PNP transistors and can range from 5 V to 40 V. Note that with this design, a 5 V supply could deliver more than 4 V to the motor - a difficult task for any other integrated circuit topology.

Finally, this device includes the protection of undervoltage lockout, with a threshold of 4.2 V, and thermal shutdown when the junction temperature rises above 150°C. Since the UC3655 is a linear driver, the potential for high dissipation is possible but a Multiwatt power package with adequate heat sinking will accommodate up to 25 watts. For smaller motors, a power 28-pin surface-mount, PLCC configuration with 4 watt capability will be offered.

INTERFACING TO THE MOTOR

The schematic of Figure 3 illustrates the added components necessary to interface the UC3655 to a typical BDC motor with the other two outputs identical to that shown. While resistor R1 serves merely to speed the turn off of the PNP transistors, R2, while optional, serves two functions: It can reduce the PNP base current to less than the internally limited 100 mA, and it absorbs the PNP base drive power losses which would otherwise add to the IC package dissipation.

In driving a BDC motor, there is no concern for cross-conduction current flow where both an NPN and a PNP experience overlapping conduction during switching transitions. This is because the commutation logic never switches any output from low to high or vice versa - there is always an off state in between. The inductance of the motor does force current transients when any transistor turns off, however. When a PNP turns off, residual current transfers to the internal diode at that output, pulling the output slightly below ground potential. When an NPN turns off, the transient current then flows through the PNP in the reverse direction, pulling the output voltage momentarily above the motor supply. Most PNP transistors will readily accept this as long as the voltages are low, but it should be evaluated for each application. Of course, the body diode of a P-channel FET provides this current path inherently.

Typical waveforms for voltage and current at one output are shown in Figure 7. While the voltage always switches to Vm on the high side due to the saturated PNP's, the value on the low side will be determined by the motor resistance and the commanded current. The large negative glitch occurs when the active PNP turns off; the tall spike above Vm occurs with turnoff of the NPN. The two short negative transients which occur while the current sinking NPN is on are caused by state-changes on the other two outputs momentarily interrupting current flow.

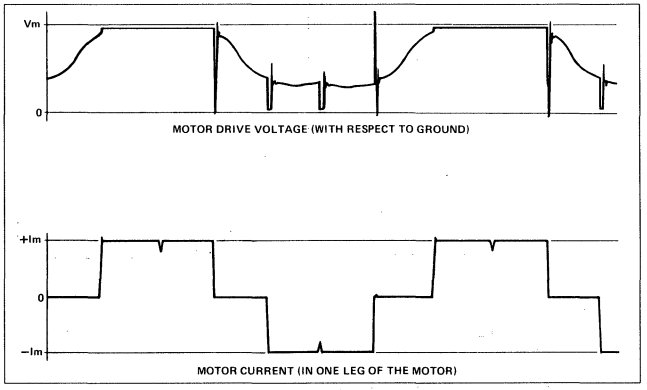

Figure 7: Voltage and current waveforms experienced at each output of the UC3655.

For disk drive or other applications where EMI noise generation at phase changes could be a problem, some slope control should be used on the outputs. While there are several ways to accomplish this, one effective technique is with R-C snubbers as shown in Figure 8. The circulating currents which will flow in these snubbers control the output rise and fall times and significantly reduce the higher frequency harmonics without contributing additional stress to the drive transistors.

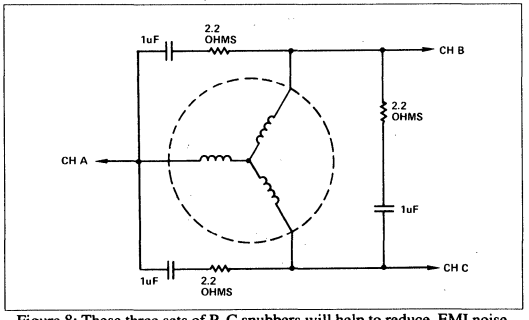

Figure 8: These three sets of R-C snubbers will help to reduce EMI noise.

ALTERNATE CONFIGURATIONS

Although the primary goal in developing the UC3655 was the implementation of a linear, current controlled BDC drive, that is not the only way this device may be used. The benefit of very low saturation voltage drop across the conducting switches has obvious advantages for efficient motor drive without linear control. The internal transconductance amplifier can be disabled by merely connecting the input terminal to the 5 V supply which will pull the compensation terminal up to the internal clamp level and allow the NPN low-side transistors to be switched fully on through the action of the decode logic. Current limiting may still be included by appropriate selection of the sense resistor, or for maximum voltage to the motor, the sense terminal may be connected directly to ground.

In this configuration, the circuit is only utilizing the position decode and output drive circuitry, and the motor will run open loop with its speed (or torque) determined solely by the motor voltage. This suggests another method of control. Since the UC3655 operates with only a 5 volt supply and is unaffected by the motor voltage, Vm, on the PNP emitters, controlling Vm will control motor speed. This can be done with either a linear or switch-mode regulator with the regulator control loop used to control the motor rather than hold the output voltage constant. An example of switching regulator control is shown in Figure 9 where an L296 PWM power supply IC is used as a 100kHz buck regulator. This circuit offers several advantages over other control techniques:

1. Since all power devices are used as switches, overall efficiency can be higher than with a linear approach.

2. The PWM frequency is converted back to DC before it gets to the motor minimizing the potential for harmful EMI.

3. High switching frequencies can be used in the regulator to keep the filter components small but with only ripple current through the motor, internal AC losses there are minimized.

4. A boost configuration could also be used to raise the motor voltage above the supply for faster response, lower currents, and a potentially significant increase in efficiency.

There are also some disadvantages:

1. The added complexity and components of the PWM regulator,

2. The additional switch in series with the motor.

PULSE WIDTH MODULATION OF MOTOR CURRENT

If the application will accept direct switch-mode control of motor current, this approach is also possible with the UC3655. Figure 10 shows the use of a UC3843 Power Supply PWM IC as the control element. Since this device has a very low impedance output drive, it will override the output of the UC3655's control amplifier and apply the PWM signal to whichever output has been activated by the decode logic. To keep switching and motor losses low, the frequency should be limited to the 20-40 kHz range.

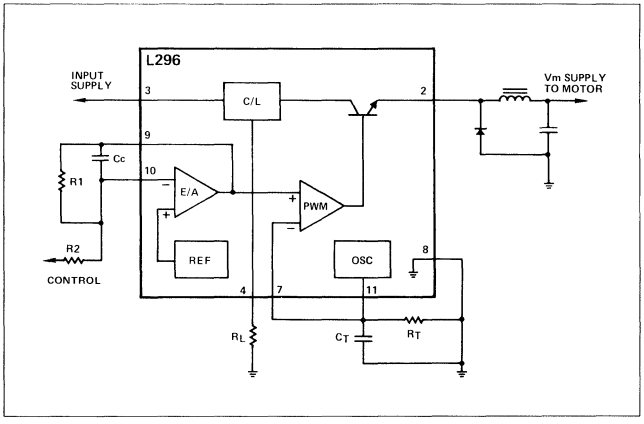

Figure 9: The L296 Buck Switching Regulator will efficiently control motor speed with the internal control loop disabled, by controlling the motor voltage instead.

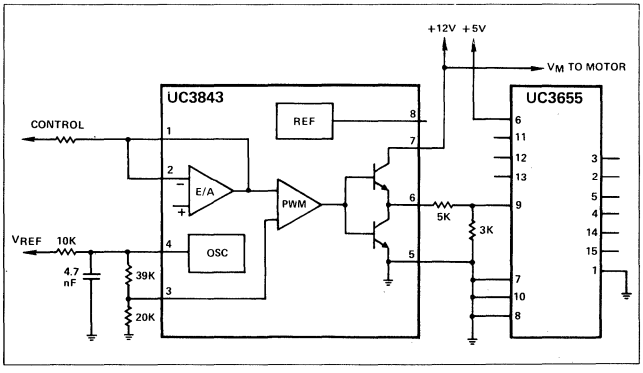

Figure 10: The UC3843 PWM Power Supply Chip can be used as a switch-mode controller for motor current by overriding the UC3655's internal amplifier with a PWM command.

PHASE LOCK LOOP SPEED CONTROL

In many applications where very accurate speed control is required - disk drives, for example - a phase lock loop, locked to a crystal frequency reference, is often utilized. The UC3633 PLL chip has been designed to supply this capability and its use with the UC3655 is shown in Figure 11. In this circuit, a 4.9125 MHz crystal is divided down and compared with a signal from one of the motor's Hall sensors to force rotation at exactly 3600 rpm, +/- 60 ppm. This figure shows the UC3655 used in its conventional linear control mode, but the UC3633 is equally applicable to the other modes of operation discussed above. For further information on the UC3633, refer to Unitrode's Application Note U-113.

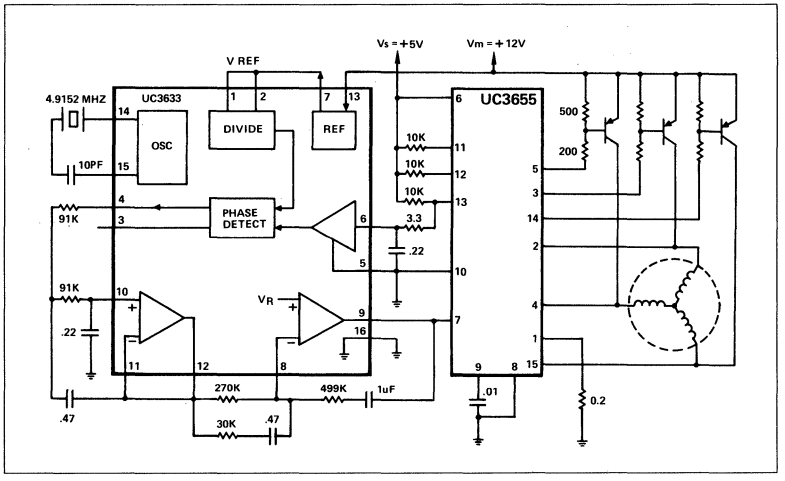

Figure 11: A UC3633 Phase Lock Loop IC can be used with the UC3655 to provide crystal-controlled speed accuracy.

SENSORLESS DRIVE

Finally, with the utilization of a microcontroller it should be possible to implement a drive system without the need for Hall position sensors and thus gain significant cost savings in the motor. Utilizing techniques developed for synchronous and stepper motors, commutation could be done "open loop" without angular position feedback but since the actual commutation point is not likely to occur at the optimum point, motor efficiency will be poor and will vary with load. One approach to solving this problem is the use of a single sensor to generate a reference point, and a digital PLL locked to this reference to generate the correct commutation timing. While this can yield commutation accuracy even higher than that obtainable with a typical sensor-type motor, the obvious disadvantage is increased cost over a completely sensorless design.

By using the back EMF generated by the motor, a signal proportional to the torque angle (commutation error angle) may be derived which can be used to correct the timing. However, simply forcing the commutation generator to deliver the correct timing will not control the speed of the motor. If instead, this signal is used to control the motor current by the approach shown in Figure 12, the commutation points are still generated open loop but, instead of forcing the commutation generator to follow the motor, the motor now follows the commutation generator. If the motor leads or lags, drive current is modified to force the torque angle to be optimum, yielding a PLL motor control system requiring no position sensors.

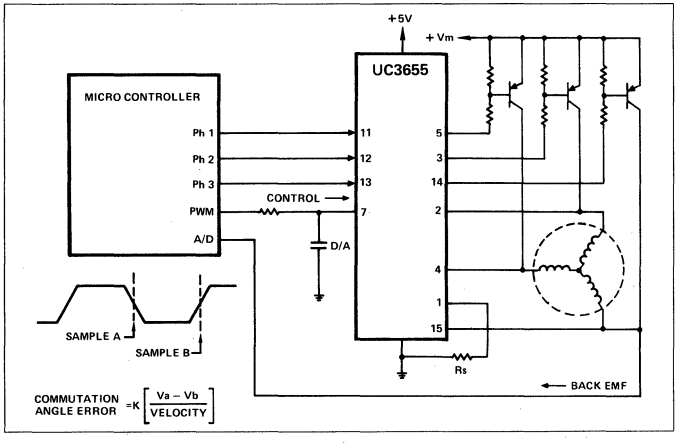

Figure 12: This approach to sensor-less control digitizes the back EMF on one motor phase and computes the commutation angle error from measurements made during the middle of the "off-time".

A SIMPLIFIED APPROACH TO DC MOTOR MODELING FOR DYNAMIC STABILITY ANALYSIS.

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When we say that an electric motor is a device that transforms electric power into mechanical power, we say two things. First, that the motor is — and behaves as — a transformer. Second, that it stands at the dividing line between electrical and mechanical phenomena. In the case of permanent magnet (PM) motors we know that this power transformation works in both directions so that the electrical impedance depends on the mechanical load, while the mechanical behavior of the motor depends on the conditions at the electrical end.

This being the case, it should be possible to represent a motor's mechanical load, on the electrical side, by a set of familiar electrical components such as capacitors or resistors.

CHOOSING A UNIT SYSTEM

Before we get started, let us consider for a moment the system of measurement units that we have chosen.

The metric system of units has undergone a number of changes in its history, of which the latest is the SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is a coherent system, in which the product or quotient of two or more units is the unit of the resulting quantity. It will be seen here that certain simplifications result from using this form of the metric system.

In the SI system, force is measured in Newtons (N) and distance in meters (m). Consequently, the units of torque are Nm (see Conversion Table). If a motor shaft rotates at an angular velocity of ω_M radians per second, with torque T_M, the mechanical power output will be equal to the product T_M and ω_M and the units will be watts if T_M is in Nm.

Motor manufacturers usually specify a torque constant (K_T) and a voltage constant (K_V) for their motors. These constants have different values when the torque and speed are measured in English units, but they have the same numerical value when SI units are used. This becomes obvious when you consider that the electrical input power must be equal to the mechanical output power:

(1) $V_A I_A = T_M \omega_M$ (watts)

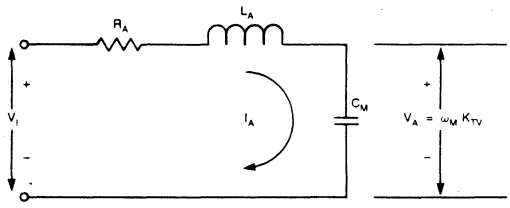
(2) $\frac{V_A}{\omega_M} = \frac{T_M}{I_A} = K_{TV}$

*where V_A is the internally generated armature voltage, or back emf, and I_A is the armature current. (See Fig. 1 for definition of motor terms.)

TABLE 1. UNITS CONVERSION

THESE UNITS	{ × → = = ← ÷ }	SI UNITS	DIM.
oz	2.78×10^{-1}	N	MLT^{-2}
lb	4.448	N	MLT^{-2}
in	2.54×10^{-2}	m	L
ft	3.048×10^{-1}	m	L
gf	9.807×10^{-3}	N	MLT^{-2}
g cm^2	10^{-7}	Nm sec^2	ML^2
ft lb sec^2	1.356	Nm sec^2	ML^2
oz in sec^2	7.063×10^{-3}	Nm sec^2	ML^2
ft lb	1.356	Nm	ML^2T^{-2}
oz in	7.063×10^{-3}	Nm	ML^2T^{-2}

NOTE. The dimensions are M (mass), L (length), and T (time). The gram (g) is a unit of mass, and the gram-force (gf) is a unit of force. The pound (lb) and the ounce (oz) are included as units of force only.



ω_M = motor speed in rad/sec

K_{TV} in Nm/A or Vsec/rad

$C_M = \frac{J}{K_{TV}^2}$ (farads)

FIGURE 1. THIS SERIES RLC CIRCUIT IS AN EXCELLENT MODEL OF A DC MOTOR LOADED WITH AN ESSENTIALLY INERTIAL LOAD. HERE, J IS THE TOTAL MOMENT OF INERTIA, INCLUDING THE ROTOR'S J_M.

If we do the same thing with the familiar electrical transformer, we get the turns ratio:

(3) $V_1 I_1 = V_2 I_2$ (watts)

(4) $\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{N_1}{N_2}$

Thus, the non-dimensional turns ratio N_1/N_2 is analogous to the dimensional torque (or voltage) constant K_{TV}. Furthermore, equations (2) and (4) give us a clear hint that the angular velocity (ω_M) is analogous to voltage, while the torque (T_M) is analogous to current.

9

The units of K_{TV} may be either Nm/A, or V sec/rad. Thus, specifying both K_T and K_V for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer, and can only make sense where redundancy is required.

THE MOTOR AS A TRANSFORMER

We have established an analogy between K_{TV} and a transformer's turns ratio; between angular velocity and voltage; and between torque and current. If the motor behaves as a transformer, then we would expect to find the square of K_{TV} involved in something analogous to impedance transformation.

Suppose we apply a constant current I_A to the armature of a motor whose load is its own moment of inertia J_M (Nm sec^2). We know that according to Newton's law for rotating objects,

(5) $T_M = J_M \alpha_M$

where α_M is the angular acceleration $d\omega_M/dt$.

Since $T_M = I_A K_{TV}$ (Eq. 2)

(6) $$I_A K_{TV} = J_M \frac{d\omega_M}{dt}$$

Furthermore, also from Eq. 2,

(7) $$\omega_M = \frac{V_A}{K_{TV}}$$

so that

(8) $$I_A = \frac{J_M}{K_{TV}^2} \cdot \frac{dV_A}{dt}$$

Equation 6 has a familiar form, and we recognize at once the quantity J_M/K_{TV}^2 as a capacitor. It follows that the motor "reflects" a moment of inertia J_M back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

A neat way to check this result is to equate the energy stored kinetically in J_M with the electrical energy stored in a capacitor C_M:

(9) $\frac{1}{2} C_M V_A^2 = \frac{1}{2} J_M \omega_M^2$

(10) $$C_M = J_M \left(\frac{\omega_M}{V_A}\right)^2$$

Since $\frac{\omega_M}{V_A} = \frac{1}{K_{TV}}$,

(11) $$C_M = \frac{J_M}{K_{TV}^2} \text{ (farads)}$$

Similarly, a torsional spring with spring constant K_S (Nm/rad) is reflected as an inductance of K_{TV}^2/K_S henries. And a viscous damping component B (Nm sec/rad) appears as a resistor of K_{TV}^2/B ohms.

A MOTOR MODEL

Once we can represent the mechanical load by means of electric elements, we can draw an equivalent circuit of the motor and its mechanical load. The armature has a finite resistance R_A and an inductance L_A, through which the torque-generating current I_A must flow. These components are not negligible, and must be included. An inertially loaded motor can be represented as in Fig. 1, where the moment of inertia J is the sum of the load's J_L and the rotor's J_M.

It turns out that in practice, the moment of inertia that the motor must work against — or with, depending on how you look at it — is by far the most important component of the mechanical load. A frictional component also exists, to be sure, but because it is largely independent of speed, it would be represented electrically as a constant current source, which could not affect the dynamic behavior of the motor. And since a torsional spring — which would affect it — is rarely found in practice, we will concentrate on the inertial problem only.

MEASURING THE COMPONENTS

The measurement of R_A and L_A is not difficult. A good ohmmeter will get you R_A, and you can measure the electrical time constant τ_E to calculate L_A:

(12) $L_A = \tau_E R_A$

Just make sure that the rotor remains stationary during these measurements.

In order to determine the value of the capacitor, C_M, we will need to measure the shaft speed. If the motor being measured is a brushless DC motor, we can use the signal from one of the Hall effect devices as a tachometer. If the Hall frequency is f_H, and the number of rotor poles is P, the angular velocity ω_M is

(13) $$\omega_M = \frac{4\pi f_H}{P} \text{ (rad/sec)}$$

With other motors you will need a strobe-light or some other means to measure speed.

A good way to measure C_M is through a measurement of the mechanical time constant T_M. We do this by driving the motor with a constant voltage driver and measuring the time it takes to accelerate from zero speed to 63% of the highest speed achievable at the voltage used. To set a safe limit to the starting current we can reduce the supply voltage or add a series resistor with the motor, or both. The set-up is shown in Fig. 2. Note that the armature resistance R_A is already known, and we add resistors R_B, if needed, to limit the armature current I_A to a value that is safe for both driver and motor.

The first thing to do is let the motor run freely and measure ω_{MAX} and I_{MAX}, and use these values to calculate the armature voltage V_{MAX}:

(14) $V_{MAX} = V_{CC} - V_{SAT} - I_{MAX} (R_A + R_B)$

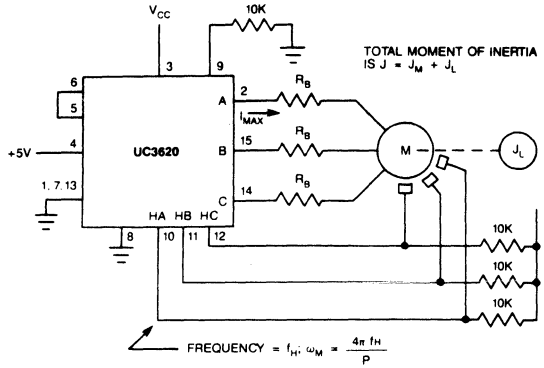


FIGURE 2. SET-UP FOR MEASUREMENT OF $C_M = J/K_{TV}$ OF A 3-PHASE BRUSHLESS DC MOTOR WITH INERTIAL LOAD J1. THE MOTOR VOLTAGE $V_M = V_{CC} - V_{SAT}$, WHERE V_{SAT} IS THE OUTPUT SATURATION VOLTAGE.

Here V_{CC} is the supply voltage, V_{SAT} is the saturation voltage of the driving circuit, and I_{MAX} is the current drawn by the unloaded motor at maximum speed.

Thus we can calculate

$$(15)\quad K_{TV} = \frac{V_{MAX}}{\omega_{MAX}} \quad \text{(Vsec/rad)}$$

Next, set the oscilloscope time scale to that you can easily read a Hall frequency equal to 63% of ω_{MAX}, so that:

$$(16)\quad \omega_M = 0.63\ \omega_{MAX}$$

By holding and releasing the motor shaft, take several readings of the time T_M required to accelerate from zero to ω_M. Remember that these readings are taken "on the fly," since the motor continues to accelerate towards the maximum speed ω_{MAX}. Having obtained a good value of T_M you can now calculate

$$(17)\quad C_M = \frac{T_M}{(R_A + R_B)} \quad \text{(farads)}$$

This completes the RLC equivalent circuit, If the value of J_M is also required, it too can be calculated:

$$(18)\quad J_M = C_M K_{TV}^2$$

THE MOTOR'S TRANSFER-FUNCTION

In the circuit of Fig. 1, V_1 is the voltage applied to the motor leads, and V_A is the actual armature voltage, or back EMF. This latter voltage is equal to $\omega_M K_{TV}$, as we have seen, so that if we want to derive an expression relating the speed to the applied voltage, we can write:

$$(19)\quad \frac{\omega_M}{V_1} = \frac{1}{K_{TV}} \cdot \frac{V_A}{V_1} \quad \text{(rad/Vsec)}$$

If V_1 is a constant voltage, the speed ω_M will also be constant. This is clear from the circuit of Fig. 1 as well as from our experience with motors. If, however, V_1 varies sinusoidaly at some frequency f, the speed ω_M will vary similarly, but the amplitude and phase will in general be different from those of the driving function. This fact is very important if we are to include the motor in a feedback loop, because the motor's contribution to the overall loop gain and phase shift is an important factor in determining stability. The motor's transfer function — i.e. Eq. 19 expressed as a function of frequency — gives us a precise description of how the amplitude and phase behave at different frequencies. To do this, we use the variable $j\omega$, where $j = \sqrt{-1}$, and $\omega = 2\pi f$.

$$(20)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{(j\omega C_m)^{-1}}{j\omega^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(21)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{(j\omega)^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(22)\quad L_A C_M = \frac{1}{\omega_n^2}$$

where ω_n is the natural frequency of the circuit.

$$(23)\quad R_A C_M = \frac{R_A C_M L_A}{L_A} = \frac{R_A}{\omega_n^2 L_A} = \frac{1}{Q\omega_n}$$

since the circuit Q is

$$Q = \frac{\omega_n L_A}{R_A}.$$

Therefore,

$$(24)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Furthermore, using Eq. 19,

$$(25)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} = \left(\frac{1}{K_{TV}}\right) \cdot \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Since we know the values of K_{TV}, ω_n and Q, we can calculate the magnitude and phase angle of Eq. 25 for various values of $j\omega$. For a given $\omega = \omega_1$, Eq. 25 can be evaluated into a complex number $A_1 + jB_1$, whose angle is,

$$(26)\quad \theta_1 = \tan^{-1}\frac{B_1}{A_1}$$

and whose magnitude can be expressed in decibels as follows:

$$(27)\quad M_1 = 20 \log_{10} \sqrt{A_1^2 + B_1^2}$$

A plot of these quantities, using a logarithmic frequency scale, is called a Bode plot, and can be a handy tool in understanding how the device will affect the final loop performance.

9

A DISC - DRIVE EXAMPLE

A small three phase brushless DC motor, measured as above, has the following characteristics:

K_{TV} = 0.015 Nm/A, or Vsec/rad.
R_A = 2.5 ohm
L_A = 0.002 Hy
J = 0.001 Nm sec_2

The J value was measured with three magnetic discs mounted, and represents the actual value required for the application. Using Eq. 11.

$$(28)\quad C_M = \frac{J}{K_{TV}^2} = \frac{.001}{(0.015)^2} = 4.44 \text{ fd}$$

This may seem like an unusually large value for a capacitor, but it simply reflects the large amounts of kinetic energy that can be stored in the included inertia.

From Eq. 22

$$(29)\quad \omega_n = \frac{1}{\sqrt{L_A C_M}} = \frac{1}{\sqrt{0.002 \times 4.44}}$$

$$= 10.61 \text{ rad/sec}$$

From Eq. 23

$$(30)\quad Q = \frac{\omega_n L_A}{R_A} = \frac{10.61 \times 0.002}{2.5} = 0.0085$$

(The quality factor Q has no units). The motor transfer function, given in Eq. 25, is

$$(31)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} =$$

$$= \frac{66.67}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1} \text{ (rad/Vsec)}$$

A calculator that is pre-programed to operate with complex numbers (HP 28C, for example, or 15C) makes the evaluation, of this equation an easy task. With the 28C you can set up a USER routine called BODE, as follows:

<<DEG DUP ABS LOG 20 X SWAP ARG>>

This will convert a complex number x + jy into 20 log $\sqrt{x^2+y^2}$ at level 2, and arc tan (y/x) at level 1. Table 2 shows a list of several such computations of Eq. 31:

At ω = 0, the gain is simply 66.67 rad/Vsec. As ω increases from zero up, the gain decreases as shown in the GAIN column of Table 2. For our Bode plot, we want to show the gain relative to the initial, or DC, gain. Therefore, we subtract 66.67db from each gain value in Table 2 and plot the result. This is the same as plotting only the function

$$(32)\quad G(j\omega) = \frac{1}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1}$$

which should be compared with Eq. 31. The results are shown in Fig. 3.

TABLE 2. CALCULATED VALUES OF EQUATION 31.

ω (rad/sec)	$\frac{\omega_M(j\omega)}{V_1(j\omega)}$	GAIN (db)	PHASE (deg)
0.01	65.9 − j 7.32	36.4	−6.3
0.03	60 − j 20	36.0	−18.4
0.1	29.8 − j 33.2	33.0	−48.0
0.3	5.5 − j 18.4	25.7	−73.3
1.0	0.53 − j 5.95	15.5	−84.9
3.0	0.06 − j 2.00	6.0	−88.4
10.0	0 − j 0.60	−4.4	−89.9
30.0	-4.2×10^{-3} − j 0.20	−14.0	−91.2
100	-4.7×10^{-3} − j 0.06	−24.5	−94.5
300	-4.5×10^{-3} − j 0.02	−34.2	−103.5
1000	-2.9×10^{-3} − j 3.7×10^{-3}	−46.6	−128.6
3000	-7.1×10^{-3} − j 3×10^{-4}	−62.3	−157.4

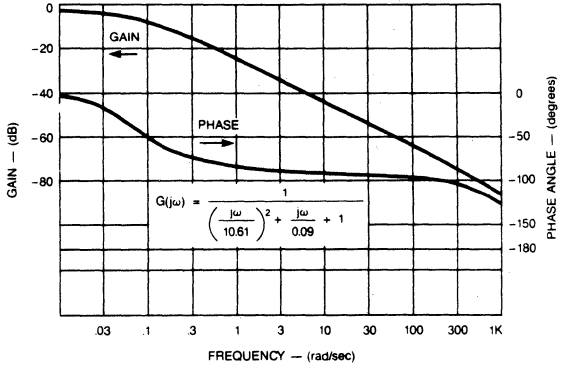


FIGURE 3. BODE PLOT OF MOTOR DATA IN EXAMPLE.

Note that up to about 100 rad/sec (15.9 Hz) the phase lag barely exceeds 90 degrees. The first pole occurs at ω = 0.09 rad/sec, at which point the phase lag is 45 degrees. The second pole, widely separated from the first in this case, occurs at a frequency in excess of 1000 rad/sec, as we can see from the further bend in the phase curve. The gain, which was drooping at a rate of −20db per decade below 100 rad/sec, now begins to bend towards a steeper droop of 40db/dec after the second pole is reached. At very high frequencies, the phase lag will reach 180 degrees.

Used in a speed control feedback loop, this motor will perform well provided that the user takes this gain and phase behavior into account. This is done by incorporating the motor transfer function into the overall loop equation, which will include other components. One's understanding of the motor's behavior improves with this type of analysis, which makes comparisons between different motors more clear and articulate.

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1 MHz 150W RESONANT CONVERTER DESIGN REVIEW

Bill Andreycak

Abstract:

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms and transferred charge and energy will be analyzed as functions of time and input/output conditions. Specific and generalized design equations are given, which are also applicable to other topologies by those skilled in modern power supply design.

Introduction:

The pioneers of resonant mode power conversion have generated a tremendous amount of interest in this new and emerging technology and approach to power conversion. Expectations of lossless switching and multi-megahertz operation are rapidly approaching realization. Given this recent stimulus, a new control IC, the UC3860, has been introduced for controlling many of the various resonant and quasi-resonant design approaches.

Despite the differences among the numerous and quasi-resonant switching topologies, all have one common denominator--the need for a high speed, complete and versatile resonant mode control IC. The ideal candidate would incorporate modulator functions or building blocks that could be easily configured by the user to control various circuit topologies and implementations.

This paper will show one application of this resonant control IC in a typical power supply design example. Described in the text is a 150 watt off-line converter switching at a maximum frequency of 1 megaHertz. This results in an effective 500 kiloHertz utilization of the main transformer. Delivering 15 volts at 10 amperes, of load current, it operates from a 110/220 AC input or from a 220 to 370 V dc bus at high efficiency.

Design Specifications:

An off-line 150 watt, single output design has been selected as a typical application for the purposes of this paper. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations. However, this discussion will concentrate on relevant calculations and new material regarding tthe quasi-resonant converter.

Input Voltage:

(110 V_{AC}) : 85 — 132 V_{AC}

(220 V_{AC}) : 170 — 265 V_{AC}

(DC Input) : 220 — 375 V_{DC}

AC Line Frequency : 50 Hz min

Output Voltage: 15 V_{DC}

Output Current: 2.5 — 10 Amps

Line Regulation: 16 mV

Load Regulation: 15 mV

Output Ripple: 100 mV p-p, dc-20 MHz
Efficiency: 85 % at full load

Quasi-resonant Circuit Operation

The quasi-resonant Buck regulator circuit shown in Fig. 1 is applicable to high frequency power conversion systems and will be dsescribed in detail. Initial conditions are given with the switch Q open, and no current flowing from the input source *V*. The resonant current I_r is zero and no voltage is acrosss either of the resonant components L_r or C_r. There is an output current I_{out} and voltage V_{out} delivered entirely by the output filter components L_o, C_o and D_o. For the purposes of this model, assume that each component is ideal.

Switch Q is closed at time t_o applying voltage V_{IN} across the circuit input. The input current I_{in} begins at zero and rises linearly at the rate of V_{IN}/L_r until it reaches output current I_{out}.

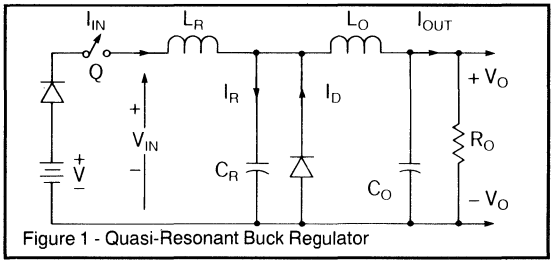


Figure 1 - Quasi-Resonant Buck Regulator

Simultaneously, the output diode current I_d which began at I_{out} linearly decreases to zero. At this point, the input power source is supplying the full output current I_{out}. This occurs at tiime t_1 which will vary linearly with I_{out} and V_{IN}. During the interval between t_o and t_1, no resonant current I_r flows in capacitor C_r.

Beginning at t_1 the resonant circuit current component I_r sinusoidally flows through C_r. This adds to the output current, making the input current the summation of both. Peak input current occurs at $t_1+\pi/(2\omega)$. It later intersects the I_{out} level at t_2, corresponding to $t_1+\pi/\omega$

The sinusoidal input current continues until t_3 where it reaches zero. Here, the switch is opened and turn-off is initiated at *zero current* which facilitates lossless switching. Since t_1 varies with I_{out} and V_{IN}, the zero current switch point t_3 varies also with these changing parameters.

A zero current detection circuit can be used to facilitate turn-off at precisely zero current. Another technique utilizes a fixed *on* time at the primary switches. This time constant is set above the maximum required *on* time of the resonant network over all line and load combinations. While this technique is easier to implement, it may compromise overall design at the maximum conversion frequency. The inability to switch consecutively at maximum rate hurts transformer turns ratio optimization. Higher currents will result due to the lower turns ratio, degrading overall efficiency at all frequencies.

During the interval between t_3 and t_4, C_r discharges, providing a constant current I_{out} to the load. The capacitor voltage decreases linearly, reaching zero at t_4.

The output filter section releases its stored energy between t_4 and t_5. The conversion period ends at t_5, which corresponds to the beginning of the next cycle, t_o. A detailed analysis of the voltages and currents during each interval is provided in the Appendix.

9

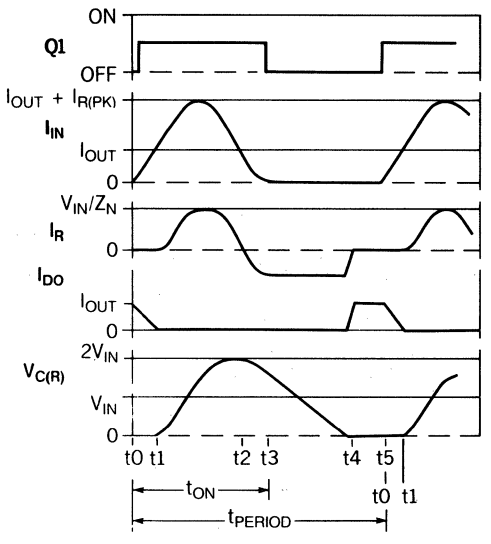


Figure 2 - Quasi-Resonant Waveforms

Quasi-Resonant Half-Bridge— Topology Fundamentals and Overview

The general circuit diagram for a quasi-resonant half bridge converter using secondary side resonance is shown in Fig. 3. The resonant half bridge portion and its associated waveforms are shown in Figs. 4 and 5.

Transistors Q_1 and Q_2 are alternately driven from the control circuitry at a repetition rate, or frequency determined by the error voltage.

Q_1 turns on, connecting the transformer primary across capacitor C_1 with voltage $V_{IN}/2$. This rectangular voltage waveform is divided by the turns ratio N (N_{pri}/N_{sec}) and coupled to the secondary side(s) of the transformer. Diode D_1 is forward biased and secondary current I_{sec} flows through L_{r1} and D_1. This can be expressed as two individual components, the "constant" output current I_{out} and the sinusoidal current I_r through C_r. During this interval, D_2 is reversed biased and is essentially out of the picture.

The secondary current starts at zero at time t_o and ramps up linearly, reaching I_{out} at t_1. I_{sec} then becomes sinusoidal, peaks at $I_{sec(peak)}$, and intersects the output current again at t_2. At t_3, zero current is reached sinusoidally and Q_1 is turned off.

Peak voltage across C_r occurs at t_2 and diminishes during the remainder of the interval ending at t_5. When the voltage across C_r reaches zero, all of its stored charge has been transferred to the output load, thus completing the conversion cycle. This process is repeated for transistor Q_2, resulting in similar operation.

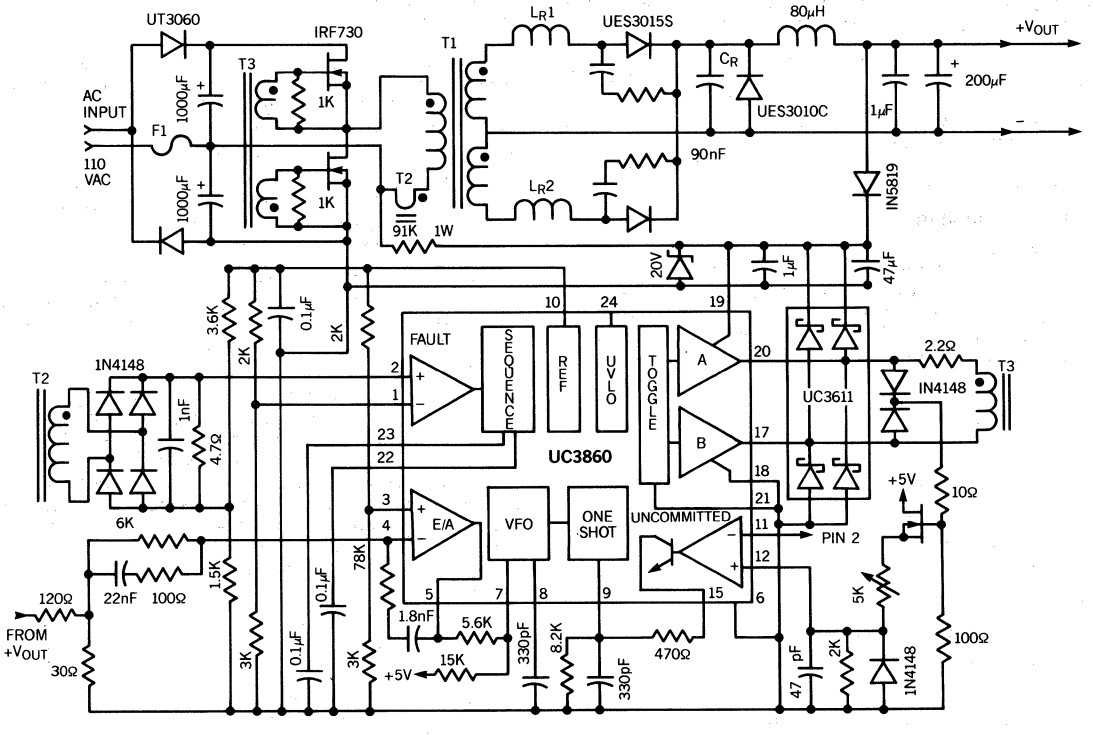


Figure 3 - 150 Watt Off-Line Quasi-Resonant Half Bridge

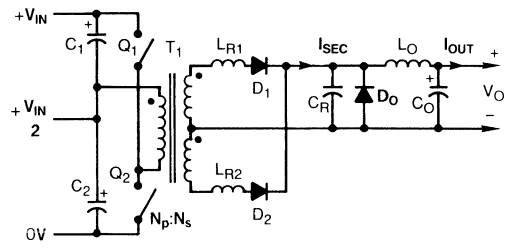


Figure 4 - Quasi-Resonant Half Bridge

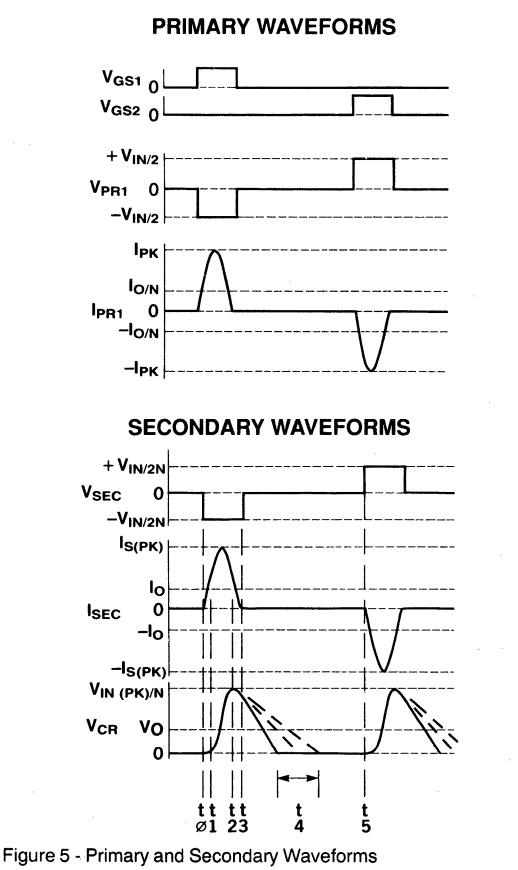


Figure 5 - Primary and Secondary Waveforms

Half Bridge Advantages and Alternatives

The thrust towards resonant mode power supply designs has been fueled by the demands for higher power densities and high overall efficiency. Although several basic topologies deserve consideration in this off-line application, the Half Bridge configuration offers many key advantages.

Unlike the single-ended forward converters, the half bridge provides bidirectional utilization of the tranformer. This eliminates the need to incorporate dissipative or complex flux reset mechanisms for the main transformer. Also, the primary switched voltage is one-half that of its single ended or full-bridge counterpart, halving the transistor voltage rating requirements.

In addition, the reduced voltage significantly reduces turn-on losses. Bear in mind that zero current switches minimizes *only* the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge has the lowest turn-off losses of all configurations.

Transformer size is smaller for the half bridge because the forward converter "wastes" half the period with no power transfer while the core is being reset. Also, all windings have half the number of turns compared to a forward converter approach. This could significantly lower the leakage inductance in certain designs where the low voltage, high current designs stand to benefit the most.

Half Wave Resonance: The half-wave resonant mode of operation facilitates a unidirectional current flow from the primary to the secondary. The major advantages of this can be seen near the primary switches. When a reverse current flows through the Mosfet, its parasitic drain-body diode conducts, exhibiting slow reverse recovery characteristics. To prevent this, the reverse current is generally directed to an external fast recovery diode that shunts the Mosfet. A Schottky diode must be added in series with the Mosfet to guarante that the external diode will conduct. This "elaborate" network is not lossless, and can signifcantly impact the power supply overall efficiency.

Seconday side half wave resonance eliminates the need for these components. Reverse current flow is restricted on the secondary side of the tansformer by the series rectifiers. Serving a dual purpose, these diodes isolate the resonant tank from the primary in addition to rectifying the secondary waveform.

Full wave designs return excess thank energy back to the primary, and require bidirectional switches on the primary. One merit, however, is that the switching frequency range is fairly narrow over various line and load combinations. On the other hand, the half wave resonant approach must span a fairly wide range of switching frequencies to maintain regulation for the the same input and output variations, since all resonant tank energy must be delivered to the output.

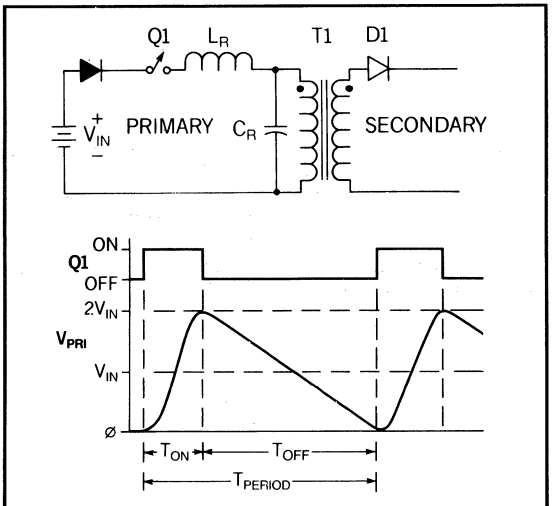


Figure 6 - Primary Side Half Wave Resonance

Secondary Side Resonance: Secondary side resonance helps minimize transformer size. With the resonant capacitor located on the transformer secondary side, the volt-second product depends only on the input voltage and transistor *on* time. During the remainder of the period, or *off* time, the transformer is not supporting the resonant capacitor discharge. Lower core losses are attained with this configuration, and are easier to analyze. The waveform is rectangular and is a function of input voltage, *on* time and switching frequency.

Resonant Control Circuit

Refer to the simplified block diagram and waveforms of Fig.8.

Error amplifier: The error amplifier is used to generate an output voltage proportional to the error between the amplifier inuts. A precision reference voltage is at the noninverting input, while the power supply output voltage is applied to the inverting input. The difference between the two is amplified and will respond to millivolt changes in power supply output voltage, providing tight regulation. The error amplifier output is high when the supply output voltage falls below its setpoint, and a low amplifier output indicates the output voltage is higher than ideal. This variable error amplifier output voltage indicates the need for correction to maintain regulation.

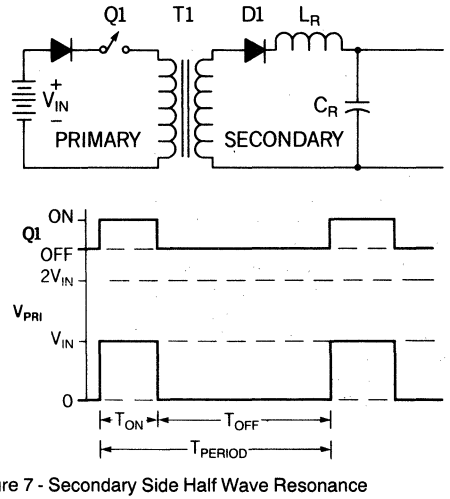


Figure 7 - Secondary Side Half Wave Resonance

Variable frequency oscillator: This device converts a variable input voltage to a variable frequency output pulse train. Increasing input voltage yields an increase in the frequency of the output pulses. Regulation of the output voltage is thus obtained over various line and load combinations by varying the switching (conversion) frequency. The VFO is driven by the error amplifier output voltage and is used to trigger the one-shot pulse generator.

One shot pulse generator: This module generates an accurate pulse width, or duration corresponding to the *on* time required for the resonant tank circuit switches. In fixed *on* time quasi-resonant applications this time constant is set slightly longer than one-half of the full resonant period. Another approach utilizes zero current switching (ZCS) which turns off the switches at zero current. In this application, the one shot is programmed for the maximum circuit on-time and modulated to facilitate ZCS.

Toggle flip flop and gating circuitry: Alternating outputs for "bridge" applications require a toggle flip-flop to divide the VFO frequency by two. This provides out-of-phase drive signals to each of the resonant switches with the proper on-time. In single ended applications like the Buck, Forward and Flyback topologies, toggle function is not used.

High power Mosfet drivers: High peak gate currents are required to deliver sharp Mosfet turn-on and turn-off transitions. The driver accepts low power (TTL) logic inputs and delivers high power (1 to 3 amp peak) Mosfet gate drive compatible outputs.

Zero current switching circuitry: Primary current is monitored and used to turn off the one shot-hence the outputs-when zero current is crossed. This minimizes the switching losses in the primary switches.

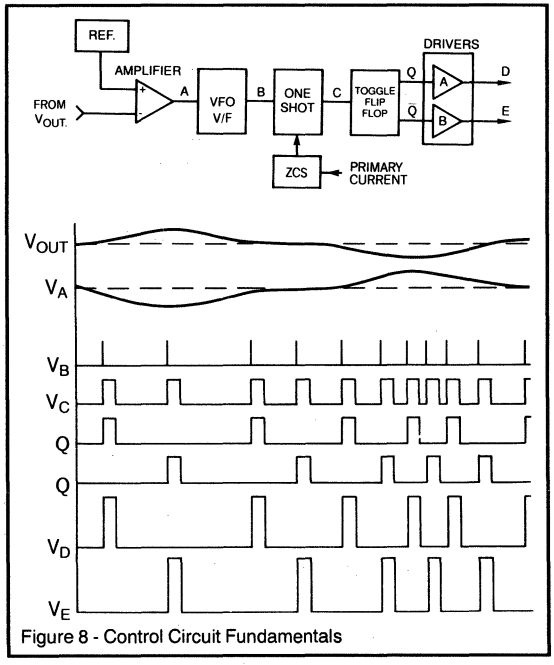


Figure 8 - Control Circuit Fundamentals

Quasi-Resonant Circuit Limitations

One obvious circuit constraint is that the peak resonant current component I_r *must* be greater than I_{out}. Otherwise, zero current will not be reached as shown in the figure below. This relationship specifies the limits of V_{IN} and I_{out} of the resonant tank as a function of the L_r-C_r resonant tank characteristic impedance, Z_r.

Increasing the resonant currrent component far above I_{out} max is one solution, but an inefficient one. The primary switch losses vary with primary current squared, and techniques to minimize this current are required.

The ideal ratio of the output current I_{out} to the minimum resonant peak current $I_{r(pk)}$ min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents and losses. The resonant component initial tolerances and temperature variations need to be analyzed and accommodated by adjusting the ratio of $I_{out\ max}$ to $I_{r(pk)}$. A twenty-five percent safety margin is used in this design corresponding to a ration of 0.75:1.

The resonant L-C elements are now defined *uniquely* by the power supply output voltage and load current for a specirfic resonant tank frequency and current ratio $I_{out\ max}$ to $I_{r(pk)}$.

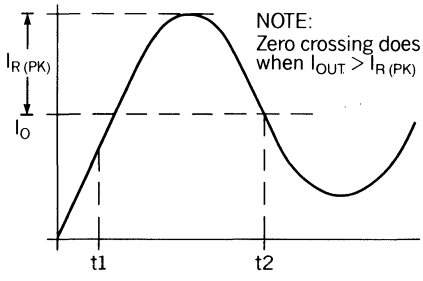


Figure 9 - Inut Current - No Zero Crossing

$$I_{r(min)} = \frac{V_{IN\ min}}{Z_r},\ or\ Z_r \le \frac{V_{IN\ min}}{I_{out\ max}}$$

Substituting $Z_r = \omega_r L_r$ and $V_{IN} = V_{sec}$ for secondary resonance, the resonant inductor L_r and C_r are defined by:

1. $L_r = \frac{0.75 V_{sec\ min}}{\omega I_{out\ max}} \Rightarrow \frac{0.12 V_{sec\ min}}{f_{res} I_{out\ max}}$

2. $C_r = 1 / (\omega^2 L_r) \Rightarrow .025 / (f_{res}{}^2 L_r)$

3. Verify that $Z_r < V_{out} / I_{out\ max}$. If not, the ratio of the resonant to output current may need to be altered.

Transformer Turn Ratio

The transformer turns ratio is derived by equating the circuit input and output volt-second products. A topology coefficient K_t is introduced which sepcifies the ratio of the maximum switching frequency to that of the resonant tank frequency. It is somewhat analagous to maximum duty cycle in a square wave converter. Allowing K_t to approach unity in a resonant converter maximizes the turns ratio, thus lowering the primary current.

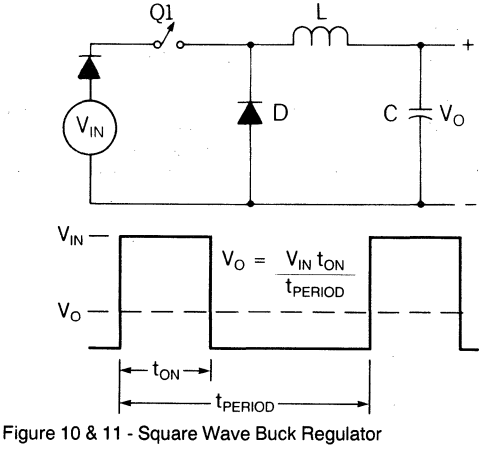


Figure 10 & 11 - Square Wave Buck Regulator

As switching frequencies approach 1 MHz, diode recovery times and Mosfet rise and fall times prevent the topology coefficient from reaching unity. In addition, the resonant capacitor requires time to discharge into the output load. A K_t value of 0.8 is suggested by several of the references listed in the Appendix. The turns ratio can now be calculated from the volt second relationship described previously.

The transformer turns ratio N =

$$V_o = \frac{V_{IN} K_t}{2 N},\quad N = \frac{K_t V_{IN\ min}}{2 V_o}$$

Accounting for the voltage drops, both the primary and secondary:

$$N = \frac{K_t}{2} \cdot \frac{V_{IN\ min} - V_{loss\ pri}}{V_{o\ min} + V_{diode} + V_{loss\ sec}}$$

The actual transformer secondary voltage has now been defined by V_{input} and the turns ratio N. The conversion period or frequency can be extracted from the energy transfer equations in the Appendix by substituting V_{sec} for V_{IN} in the given equations.

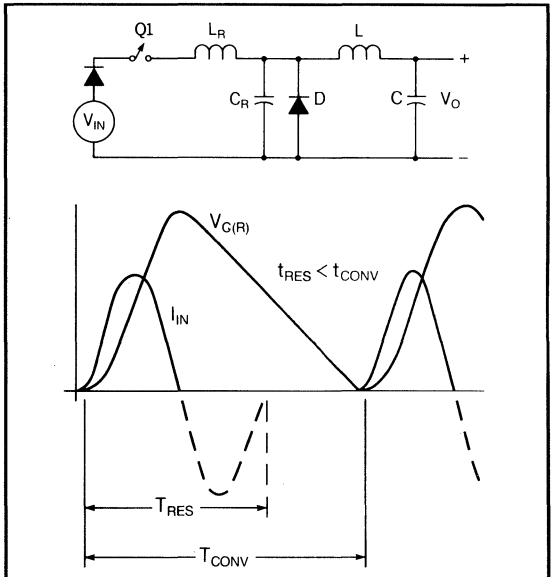


Figure 12 & 13 - Resonant Mode Buck Regulator

Conversion Frequency

As the output load current I_{out} and input voltage V_{IN} vary, the control circuit adjusts the conversion frequency to maintain a constant output voltage, V_{out}. The maximum conversion frequency will occur at low line and full load, where by design, the frequency equals the resonant tank frequency divided by K_t, the topology coefficient.

$$K_t = \frac{f_{conv\ max}}{f_{res}};\quad f_{conv\ max} = K_t f_{res}$$

Minimum frequency will occur at high line $V_{IN\ max}$ and light load $I_{out\ min}$ which can be estimated by the following relationship:

$$1 / f_{conv\ min} = T_{conv\ max} = \frac{V_{IN\ min}\ Q}{2 N V_o I_{o\ min}}$$

where

$$Q = \left[\frac{2 N L_r I_o{}^2{}_{min}}{V_{IN\ min}} + \frac{V_{IN\ min}\ C_r}{N} + \frac{\pi I_{o\ min}}{2 f_{res}}\right]$$

Quasi-Resonant Circuit Relationships

SUMMARY OF APPENDIX1

Timing relationships:

t_o= time when the cycle is initiated
$t_1 = Lr * I_{out} / V_{sec}$
$dt_{21} = \pi/\omega_{res}$
$t_2 = t_1 + dt_{21}$
$dt_{32} = 1/\omega_{res} \times \sin^{-1}(I_{out} Z_r / V_{sec})$

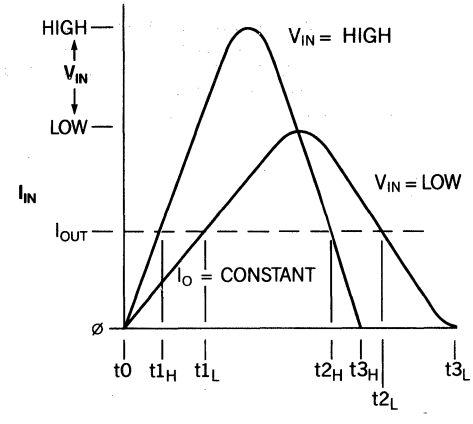


Figure 14 - Effects of Line Change on I_{in}

$t3 = t2 + dt_{32}$
$dt_{43} = V_{C(t3)} C_r / I_{out}$
$t_4 = t_3 + dt_{43}$
$t_5 = [V_{sec} Q_t / (V_{out} I_{out})]$ (approx)

The charge transferred per cycle, Qt, is approximated by:

$Q_t = L_r I_{out}^2 / V_{sec} + 2 V_{sec} Cr + \pi I_{out} / \omega$

Design Procedure and Calculations

The design specifications listed on page 1 will be used for this 150 watt application. A maximum switching frequency of 1 MHz has been selected as a good compromise between the attempts to obtain high power density (small size) and high overall efficiency.

1. Select the maximum switching fequency:

$f_{conv\ max}$ = 1.0 MHz

This also determines the resonant tank circuit frequency using the topology conversion coefficient, K_t.

$K_t = f_{conv\ max} / f_{res}$. Use K_t = 0.8

2. Calculate the resonant tank frequency, fres

$f_{res} = f_{conv\ max} / K_t$ = 1 MHz/0.8 = 1.25 MHz

3. Determine the transformer turns ratio, N

$N = N_{pri} / N_{sec} = K_t V_{IN\ min} / (2V_{out} + V_{diode})$

= 5.19 (use 5:1)

4. Calculate $V_{in\ min}$, the minimum input voltage referred to the secondary:

$V_{in\ min} = V_{s\ min} / 2N$ = 220V/(2 * 5) = 22V

The resonant inductor and capacitor values are calculated using the minimum input voltage to the secondary.

5. Calculate the resonant inductor value, L_r

$L_r = 0.12V_{\ in\ min} / f_{res} I_{out\ max}$ = 176 nH

6. Calculate the resonant capacitor value, C_r

$C_r = .025 / f_{res}^2 I_{out\ max}$ = 90.9 nF

7. Calculate and check resonant impedance Z_n

$Z_n = (L_r / C_r)^{1/2}$ = 1.39Ω (yes, < 1.5 ohms)

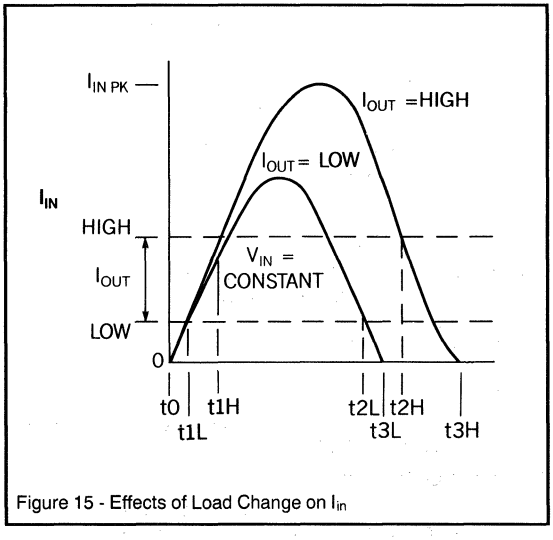


Figure 15 - Effects of Load Change on I_{in}

The basic sections of the circuit are now complete. Detailed analysis of the primary and secondary voltages and currents follow.

Peak Current calculations: The peak secondary current is approximated by :

$I_{sec\ pk} = I_o + V_{in} / Z_n = I_o + V_s / (2 * N * Z_n)$

= .072 V_s

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

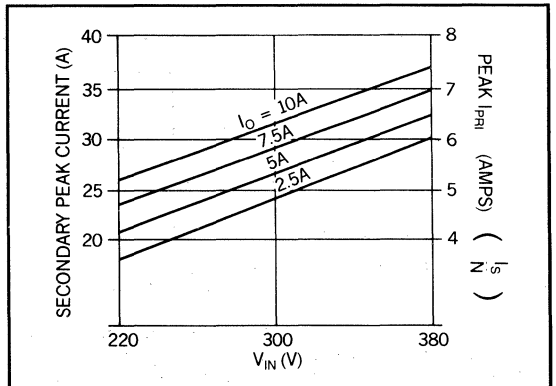


Figure 16 - Peak Secondary Current vs. V_{in} and I_o

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

The peak secondary voltage is:

$V_{s\,pk} = V_{s\,max}/2N = 370/2 * 5 = 37V$

Rectifiers in the secondary circuit need to block at least twice the peak voltage, and are typically selected with a much higher rating. Schottky diodes can be ruled out in this 15V output application due to their 45 to 90 volt breakdown voltages, so an ultra to hyperfast diode is required. A 150 volt, 30 amp (DC) device provides ample safety margin. A low capacitance power package is also desired to minimize parasitics and power losses.

rms current calculations: The primary and secondary RMS currents can be approximated to a high degree of accuracy by a pulsed sinusoidal waveform. The relationships derived in the previous section for peak currents, *on* times and conversion frequencies will be used to calculate the RMS currents incorporating the following equation.

$$I_{rms} = I_{peak}\left[\frac{T_{on}}{2\,T_{per}}\right]^2$$

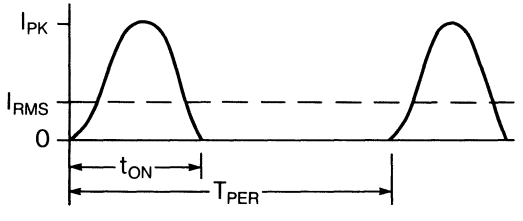


Figure 17 - rms Current Calculation

The primary current calculations will use the conversion period of 1/fconv due to the bidirectional switching of the primary. Secondary currents conduct only once per two conversion periods due to the bridge arrangement of the secondary windings. Both low and high input voltage conditions will be examined at full output load to determine worst case conditions.

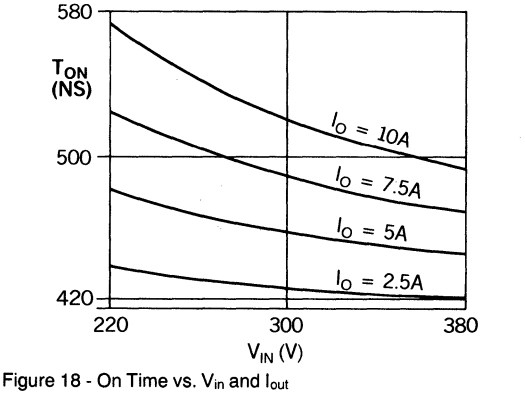


Figure 18 - On Time vs. V_{in} and I_{out}

The transformer primary wire size will be calculated using the rms current components, in addition to thermal considerations of the transistor switches and rectifiers.

Each of the Mosfet switches, secondary rectifiers and transformer secondary windings conduct current only once per two conversion cycles. This results in a lower rms current through each device.

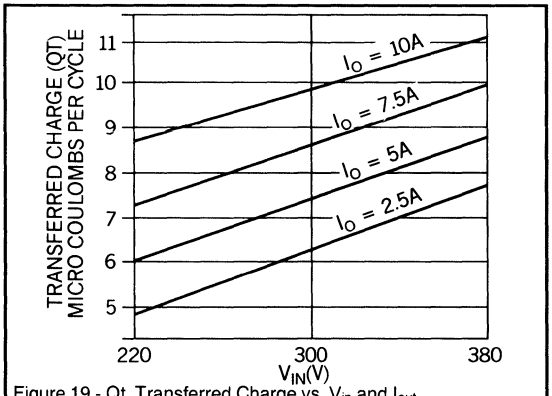


Figure 19 - Qt, Transferred Charge vs. V_{in} and I_{out}

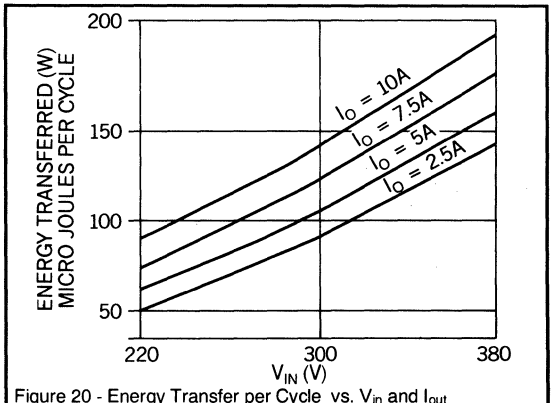


Figure 20 - Energy Transfer per Cycle vs. V_{in} and I_{out}

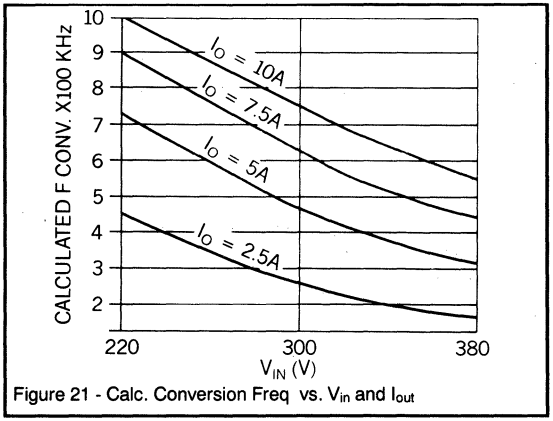


Figure 21 - Calc. Conversion Freq vs. V_{in} and I_{out}

Low Line	High Line
$I_{sec\ pk}$ = 26 A	$I_{sec\ pk}$ = 37A
$I_{pri\ pk}$ = 5.2A	$I_{pri\ pk}$ = 7.4 A
t_{on} = 575 ns	t_{on} = 495 ns
T_{per} =1.0 μs	T_{per} = 1.82 μs

rms Transformer Primary Current:

$I_{pri\ rms}$ = 2.78 A $I_{pri\ rms}$ = 2.72 A

rms Current - Mosfet Switches and Secondary Rectifiers:

$I_{rect\ rms}$ = 9.86 A $I_{rect\ rms}$ = 9.65 A
$I_{MOS\ rms}$ = 1.97 A $I_{MOS\ rms}$ = 1.93 A

Timing Considerations: The operation of this quasi-resonant circuit has been described as requiring a variable frequency, *fixed on time* control pulse train. Actually, the *on* time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented earlier, the *on* time is calculated and plotted for the ranges of V_{in} and I_{out} in Fig. 18.

Transferred charge: The charge transferred from the primary to the secondary per cycle is a function of both V_{in} and I_{out}. Using the equations presented in the Appendix, the results are graphically represented in Fig. 19.

For the selected values of voltage and current shown, the average change required in voltage or output current per microCoulomb transferred havd been calculated.

Avg dV/μC = 5.935, and Avg dI/μC = 2.086

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by $V_{in}/2$ to convert from charge to energy, with the results shown in Fig. 20.

The conversion period is obtained by dividing the energy transferred per cycle by the output power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for varius input voltages and output currents in Fig. 21.

Power Mosfet Switch Considerations

The power Mosfet selection process must take into account the three types of losses incurred by the high voltage switch. First, and probably the most predominant loss contributor is the FET *on* resistance, or $R_{ds(on)}$. Conduction losses are minimized by using a FET with the lowest $R_{ds(on)}$ obtainable.

$P_{loss\ dc} = I_{pri\ rms}{}^2\ R_{ds\ (on)}$ (Watts)

Generally the low resistance is attained by paralleling numerous FET cells of higher on resistance. The result is a single high current, low resistance device with a large die size, or geometry. This technique is great for lower frequency applications where the transition (turn-on and turn-off) times are a small percentage of the entire duty cycle. At high frequencies and especially with high voltages, this paralleling scheme introduces many difficulties in minimizing the switching transition losses.

Each cell has a finite output capacitance which quickly "adds up" when many are placed in parallel. The FET output capacitance is charged and discharged to the FULL input bulk voltage each cycle, contributing losses. At high frequencies, changing to a larger size FET could increase the total FET losses, despite having a lower *on* resistance. The incremental gains of lower conduction losses are lost to the higher switching losses of the larer capacitance FET. For this reason, it is a worthwhile exercise to examine several different size FETs over the line and load ranges of this design.

$P_{loss\ ac} = 0.5 C_{oss}\ V_{in}{}^2 f_{conv}/2$ (watts)

The gate drive power losses are generally negligible with respect to the total losses, but can be calculated from:

$P_{loss\ gate} = 0.5 V_{aux}\ Qt\ f_{conv}/2$ (Watts)

where Q(t) is the FET total gate charge, accounting for the gate to source charge plus the Miller effect charge.

The greatest primary current occurs at full load, which will be used for the worst case evaluation of power losses. Both high and low input voltage were used to calculate the ac losses, then averaged. The following list is a summary of the total power loss for each Mosfet switch in this application. A 100°C junction temperature at the FET die was assumed, where the actual *on* resistance is double that of the published specification. Various size FETs have been analyzed to compare the ac and dc losses to select one which exhibits the lowest total losses.

Circuit specifics (at the FET swithces):

$I_{pri\ rms}$ = 1.97A at V_{in} = 220V, f_{conv} = 1 MHz

$I_{pri\ rms}$ = 1.93A at 375V, 550 KHz

Device	Rds	Coss	Qg	Pdc	Pac	Pg	Ptotal
ea)							
IRF720	3.6	64	20	13.7	1.05	0.08	14.87
IRF730	2.0	100	35	7.62	1.57	0.11	9.30
IRF740	1.1	210	63	4.19	3.30	0.19	7.68
IRF820	6.0	54	19	22.8	0.85	0.07	23.78
IRF830	3.0	91	32	11.4	1.43	0.10	12.96
IRF840	1.7	180	63	6.47	2.83	0.19	9.49
IRFP440	1.7	180	63	6.47	2.83	0.19	9.49
IRFP450	0.8	350	130	3.04	5.51	0.39	8.95
IRFP460	0.54	480	190	2.05	7.56	0.57	10.19

The lowest overall losses are obtained with the 740 type devices which will be utilized in this application. This procedure will yield different results for each application, and is a recommended step towards minimizing power losses.

Rectifier Selection

Evident from Figures 16 and 17 is the need for high performance rectifiers to achieve an overall high efficiency power supply. Peak secondary currents approach 40 amps, with an rms component near 14 amps. Due to the high peak reverse voltages of nearly 100 volts, Schottky diodes cannot be used as the secondary rectifiers. Even the "freewheeling" diode must withstand 80 volt peaks at high line.

Reverse recovery times must be minimal to prevent reverse current from flowing in the primary switches in addition to enhancing efficiency. While the circuit currents are quasi-sinusoidal, the rectifier voltage is not. Parasitic inductances and capacitances of the device and its package must also be accounted for as part of the resonant L-C tank. This implies that the transformer will be designed for a lower leakage inductance than the resonant L and external inductance will be introduced to obtain the precise amount.

The To-247 package will be utilized for two reasons. First, it has lower parasitics and is better suited to high frequency applications than its To-3 metal case counterpart. Second, it is simple to heatsink this flat package, which can be mounted in various configurations.

Unitrode UES3015S ultrafast 30 amp, 150 volt rectifiers were selected for the secondary input diodes. Typical performance characteristics are 35 ns reverse recovery times and less than 1 V forward drop at 30 A and 125°C junction temperature. The "freewheeling" diode used is a Unitrode UES1615S ultrafast type, with 16 amp dc capability and a forward drop of less than 0.85 V. It too exhibits a 25 ns reverse recovery time.

Power dissipation and heatsinking requirements for each device can be calculated using the secondary currents obtained previously in this power supply design. Snubbing of each diode will be left to the prototype stage when any parasitic circuit influences can be evaluated.

Main Transformer Design

The transformer design begins with a basic idea of the core geometry most applicable to the particular design. Off-line supplies lend themselves to low, wide winding windows, typical of the ETD geometry. This window shape provides adequate room to accomodate the creepage and clearance distances required for international safety specifications.

Switching of the transformer primary will occur at a maximum of 500 KHz, and standard ferrite materials will be utilized in this example. With numerous choices to consider, the 3C6A material was selected.

To begin this 150 watt design, a fair estimate is to keep the transformer losses around 1% of the total input power, or approximately 2 watts. In addition, the transformer temperature rise is desired to be less than 40°C for combined copper and core losses. A core size can be approximated knowing that its thermal resistance, R_t, needs to be in the neighborhood of 40°C/2W, or less than 20°C/W. This is useful as a first iteration to determine the approximate operating flux density required. The precise size will be calculated using the area product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} \cdot 10^4}{120 K 2f}\right]^{1.58} \cdot (K_h f + K e f^2)^{0.66} \quad cm^4$$

where:

Pin - Input Power = 180 Watts
K - Winding Factor = 0.163 for half bridge
f - Transformer Frequency = 500 KHz
K_h - Hysteresis Coeff. (3C6A) = 1.10^{-5}
K_e - Eddy Current Coeff. (3C6A) = 4.10^{-10}

For this design, the area-product calculates to 0.543 cm^4, which is slightly less than the smallest standard core size, the ETD-34. Because the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19°C/W, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between the core and copper can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accomodate fewer turns, or less copper. The actual core power density, P_d, is calculated from the following equation, allowing a 20°C temperature rise, T_r, due solely to core losses.

$$Power\ Density = \frac{T_r}{R_t \cdot Vol} = \frac{20°C}{19 \cdot 7.64}$$

Referencing the manufacturers data sheet for the 3C6A material at a power loss density of approximately 140 mW/cm^3 and a 500 KHz operating frequency, it is determined that an operating flux density of 300 gauss (0.030 T) be used. The total flux density swing, ΔB, is twice that, or about 0.060 Tesla. The minimum number of primary turns is calculated assuming 5 V primary drops, low line conditions, and a cross-sectional core area, A_e, of 0.971 cm^2.

$$Power\ Density = \frac{V_{pri}\, t_{on} \cdot 10^4}{\Delta B \cdot A_e}$$

$$= \frac{105 \cdot 575 \cdot 10^{-9} \cdot 10^4}{.060 \cdot 0.971} = 10.3 turns\ (use 10)$$

A turns ratio N of 5:1 was previously established for this design. Minimized leakage inductance is obtained by "sandwiching" the secondaries between the two primary halves. In this example, one-half of the primary turns will be wound first, closest to the core center leg. Then, the entire secondary is wound directly above the primary half. The final winding is remaining primary half, as shown in Fig. 22.

Copper strip or foil will be used for each winding to minimize "build-up" which increases the distance between windings, hence increases leakage inductance. If the transformer leakage inductance is greater than the required resonant inductance, then the transformer must be redesigned for lower leakage.

The required primary and secondary copper cross-section areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

Primary current rms current, $I_{pri\ rms}$ = 2.78 A rms
Secondary rms current, $I_{sec\ rms}$ = 9.86 A rms
Primary copper area, Axp = $I_{pri\ rms}$ /450
= .0062 cm^2

Secondary copper area, $A_{xs} = I_{sec\ rms}/450$
= .022 cm^2

Pri. inductance, $L_{pri} = A_L N_p^2$ = 190μH
Sec (half) inductance, $L_{sec} = A_l N_s^2$ = 7.6μH

The primary conductor area is approximately equal to the area of an AWG # 19 wire, while the secondary area is closest to AWG # 14. Eddy current calculations show that the depth of penetration at 500 KHz is .0106 cm, or about the thickness of anumber 37 AWG wire. The most practical technique to minimize the AC loss in a transformer windingt is to use copper strip or foil, as in this design. Its width is determined by the bobbin width and safety creepage requirements requirements of 8 millimeters as shown.

The required 8 mm primary to secondary spacing between winding ends will be subtracted from the bobbin width of 2.10 cm, leaving 1.30 cm (0.51 inch) for the copper strip width. Allowing for tolerances, standard 0.5 inch width foil will be used in this design. The strip thickness is calculated by dividing the required copper area by the 1.27 cm (0.5 inch) width.

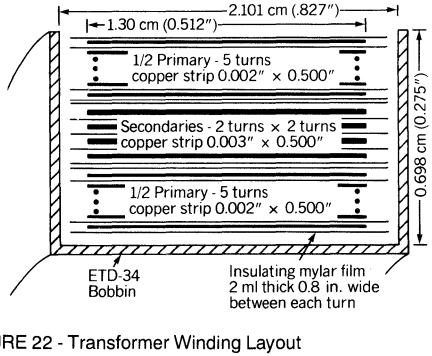


FIGURE 22 - Transformer Winding Layout

Pri thickness = A_{xp}/Width = $6.18 \cdot 10^{-3}/1.27$
= .00475 cm, or .00187 in

Sec Thickness = A_{xs}Width = $2.19 \cdot 10^{-3}/1.27$
= .01685 cm, or .00663 in

9

Standard 2 mil (0.0051 cm) foil will be used for the primary. This is slightly larger than the required thickness of .00475 cm, and is less than 1/2 the .0106 cm penetration depth. Secondary penetration is from both sides because of the interleaved primary, so the calculated secondary thickness should be and is less than twice the penetration depth. Two paralleled 3 mil foils are used as secondary conductors.

The resistance and power loss of each winding is calculated from the following relationships, based on the resistivity of copper at 100°C, $p_{cu} = 2.29 \cdot 10^{-6}$ Ω-cm. Total copper and core losses are also highlighted, in addition to the toal temperature rise at the maximum conversion frequency.

$$\text{Winding resistance} = \frac{p_{cu} \cdot \text{avg length turn} \cdot N}{A_x}$$

$R_{pri} = 2.29 * 10^{-6} * 5.99 * 10/6.18 * 10^{-3} = 22.2\ m\Omega$
$R_{sec} = 2.29 * 10^{-6} * 5.99 * 2/2.19 * 10^{-3} = 1.25 m\Omega$
$P_{loss\ winding} = I_{rms}^2 * R$
$P_{loss\ pri} = 2.78^2 * .0222 = 171\ mW$
$P_{loss\ sec} = 9.86^2 * .00125 = 121.5\ mW$
$P_{loss\ copper} = 2 * 0.171 + 0.1215 = 0{,}4635\ W$
Total power loss = copper losses + core loss
$P_{total} = 0.464 + 1$ (approx) ≤ 1.5 W
Temp. rise = Rt x P_{total} = 19°C/W x 1.5W
= 28.5°C

Output Inductor Design

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHz. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. This mode of operation helps lower the overall losses at full load because with lower ripple the peak current that must be switched is less. In addition, it reduces the size of the output choke since the peak (DC + AC) and full load (DC) current are withinone percent of each other.

$L_o = [(V_{out} + V_{diode}) * t_{off\ max}] / \Delta I_{out}$

= 15.8V x 5 us / 1 A = 80 μH (approx)

At the maximum conversion frequency and $t_{off\ min}$, the output ripple current reduces to:

$\Delta I_{out} = [(V_{out} + V_{diode}) \times t_{off\ min}] / 80\ \mu H = .08A$

Referring to Section M5 of the Unitrode Seminar Manual, core selection starts by calculating the area product:

$$AP = A_w A_e = \left[\frac{L_o I_{pk} I_{fl} \cdot 10^4}{420 \cdot K \cdot B_{max}}\right]^{1.31}$$

A PQ type geometry has been selected for the output choke application. The core set closest in size to the required area product is the PQ 32, which is available in either a 20 or 30 mm height. Of the two, the PQ32/20 size will be used because its height is similar to the ETD34 core set used for the main transformer. Its magnetic area is 1.70 cm^2.

$$N_{min} = \frac{L \cdot I_{pk} I_{fl} \cdot 10^4}{B_{max} A_e}$$

$$= \frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10^4}{0.30 \cdot 1.7}$$

The cores will require gapping to store the required energy without saturation. Gap length is calculated from the inductance formula:

$l_g = (\mu_o \mu_r N^2 A_e \cdot 10^{-2}) \mid L = 0.68 cm$

using $\mu_o = 4\pi \cdot 10^{-7}$ and $\mu_r = 1 (air)$

Correcting the gap length for the fringing field, a gap of .082 cm (.032") should be used.

Again, copper strip is used to minimize losses. Winding resistance and power loss calculations are similar to those of the main transformer design, and total less than 1.5W.

OUTPUT CAPACITOR

There are two components of ripple voltage which need to be considered in meeting the design goal of 100 mV. They are both caused by inductor ripple current. The first is simply:

$\Delta V_{out} = DQ / C_{out}$

For a given ripple current, this component is minimized by increasing the capacitor value. If this were the only contributor, the minimum capacitance required is:

$$C_{outmin} = \frac{1\ \Delta I_{out}\ 1\ 1}{2\ 2\ 2 f \Delta V_{out}}$$

This component varies with frequency. At $f_{conv\ min}$, 6.25μF are needed, but at $f_{conv\ max}$ (1MHz) only 0.1 μF is required to maintain the ripple voltage specification.

The second (and usually predominant) ripple voltage component is the voltage drop across the capacitor Equivalent Series Resistance (ESR) caused by the ripple current of ΔI_{out}. The maximum ESR allowable for 100 mV ripple is:

$ESR_{max} = 100\ mV / 1.0\ A = 100 m\Omega$

The two ripple voltage components do not add directly as they are in quadrature. With electrolytic capacitors, the ESR component dominates the capacitor selection. The resulting capacitance value is so much greater than the minimum value required that the $\Delta Q/C_{out}$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

In this design, two 100 μF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 milliohms - a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers.

A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electryolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolithic capacitors are used for this application. Different capacitor types and values can be paralleled to obtain a low impendance over a broad frequency range, useful in this variable frequency application.

Gate Drive Circuitry

The ideal gate drive circuit must deliver sharp turn-on and turn-off pulses to the high voltage power Mosfets. This is made possible by the UC3860 controller's high speed totem pole drivers. Delivering 3 amp peak currents, the drivers have typical rise and fall times of 25 ns into a 1 nF load.

Half bridge circuits require the use of a gate drive transformer to electrically isolate the "high-side" switching transistor from the control circuit. Driving both transistors from the same transformer 180° out of phase offers nearly identical drive signals to each transistor. This tends to balance the switching losses and maintain a narrower band of the associated transition EMI.

The drive transformer must have low leakage inductance to provide crisp edges during the transitions with little overshoot. This makes zener clamps and snubbing circuits unnecessary at the transformer outputs. A 0.50" O.D. toroid is used, fitted with three identical windings of ten turns each. This helps minimize the transformer magnetizing current and maximizes the peak current delivered to the FET gates.

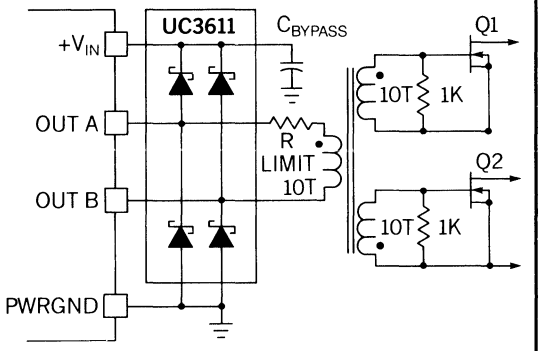


Figure 23 - Gate Drive Circuit

Resistors from gate to source at each FET provide a fairly low impedance to prevent turn-on during start-up while the IC may still be in undervoltage lockout. During regular operation, these resistors have negligible impedance.

On the controller side, the UC3611 quad Schottky diode prevents the ICoutputs from going below ground, avoiding substrate biasing problems. A series resistor limits the peak current to the 3 A rating, and the transformer is reset while both outputs are low, between cycles.

Zero Current Detection and Switching

The primary currrent is used for two important functions in this design, fault protection ans zero current detection. A typical configuration is shown in Fig. 26. The generalized circuit starts with the use of a current transformer in series with the primary of the main transformer to detect primary current. A turns ratio of 1:25 reduces the switch current to a manageable level. It is full wave rectified by 1N4148 diodes (D_6-D_9) and converted to an appropriate unipolar voltage at the current sense resistor, R_{11}. In addition, zero current or zero voltage can be detected by using the UC3860 uncommitted comparator. Its open collector output can interface with the RC *on* timing pin of the one shot, pulling it below the turn off threshold at zero detection. As shown in Fig. 24, this reduces the *on* time of the one shot timer, allowing the Mosfets to switch at zero current for high efficiency.

Implementation reqires shifting the noninverting input between two thresholds so that only the falling edge of primary current is an acceptable input for switching to occur. (See Fig. 25). This is done to prevent a false output from the comparator during the beginning of the cycle, where zero current also occurs. Primary current sensing will be offset by the resistor divider network R_{21} and R_{16} from V_{ref} to ground. This is fed into the invering input of the uncommitted comparator.

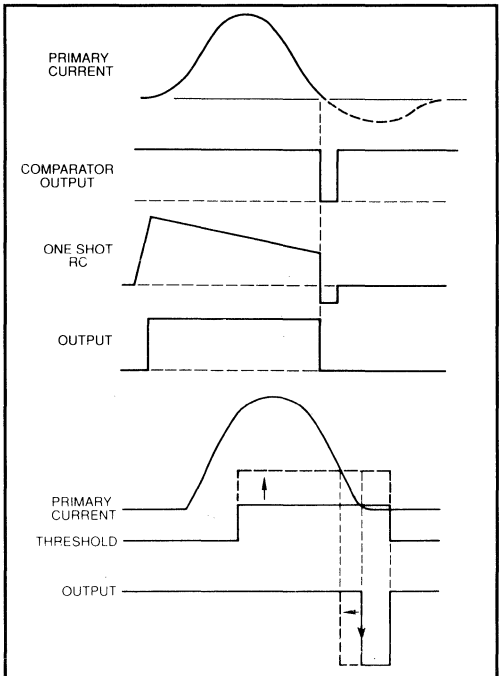


Figure 24 & 25 - Zero Current Switching

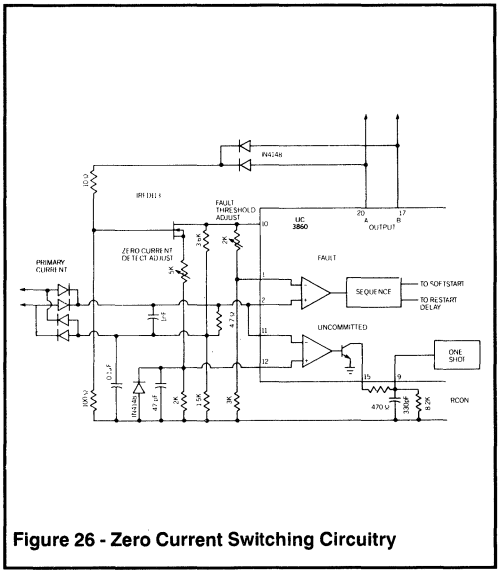


Figure 26 - Zero Current Switching Circuitry

In Fig. 26, adjustments can be made to provide a comparator output *just* prior to zero current by resistor R20. Propagation delays through the IC and drive circuitry, although minimal, can effectively be "nulled-out" along with Mosfet delays by this technique.

The UC3860 Resonant Mode Control IC

The block diagram of the UC3860 in Fig. 27 displays several key building blocks which together provide the functions necessary for precise resonant mode control. To begin, the undervoltage lockout turn-on and turn-off thresholds are pre-programmed for 17 and 10 volts respectively and are used in their standard configuration. This allows ample time for start-up and bootstrapping to occur in an off-line supply while providing adequate Mosfet gate drive voltages. The UVLO can also be reprogrammed for other turn-on and off thresholds. Also, it functions as an alternate shutdown mechanism. While UVLO is invalid, the UC3860 reference voltage output is held low, deactivating the internal circuitry. The 1% accuracy 5.0 V bandgap reference is capable of driving ten milliamps maximum external loads.

The power supply output voltage will be divided down to deliver 3.0 volts at the inverting error amplifier input for the desired V_{out}. With its high gain-bandwidth of 5 MHz, this voltage type op amp also features controlled output voltage excursions. The error amp output swings from 0.0 to 2.0 V above the voltage at the VFO I_{osc} input and tracks this node over temperature. This mechanism facilitates the maximum conversion frequency clamp in addition to the voltage (or current) to frequency conversion gain.

Variable frequency operation commences with the error amplifier providing a variable output voltage. This is transformed to a variable current at the VFO variable current input, I_{vfo}. Internal circuitry mirrors this current to the VFO timing capacitor, C_{vfo}. Maximum frequency occurrs at $2.0V/R_{vfo} * C_{vfo}$, which coincides with the error amplifier upper clamp. Minimum frequency is also programmable via resistor R_m from V_{ref} to the I_{vfo} input. The frequency to voltage gain of the IC in MHz/V (or GHz/V) is also established by these timing components. Additionally, the VFO can be externally triggered and/or disabled at the respective input pin accomodations.

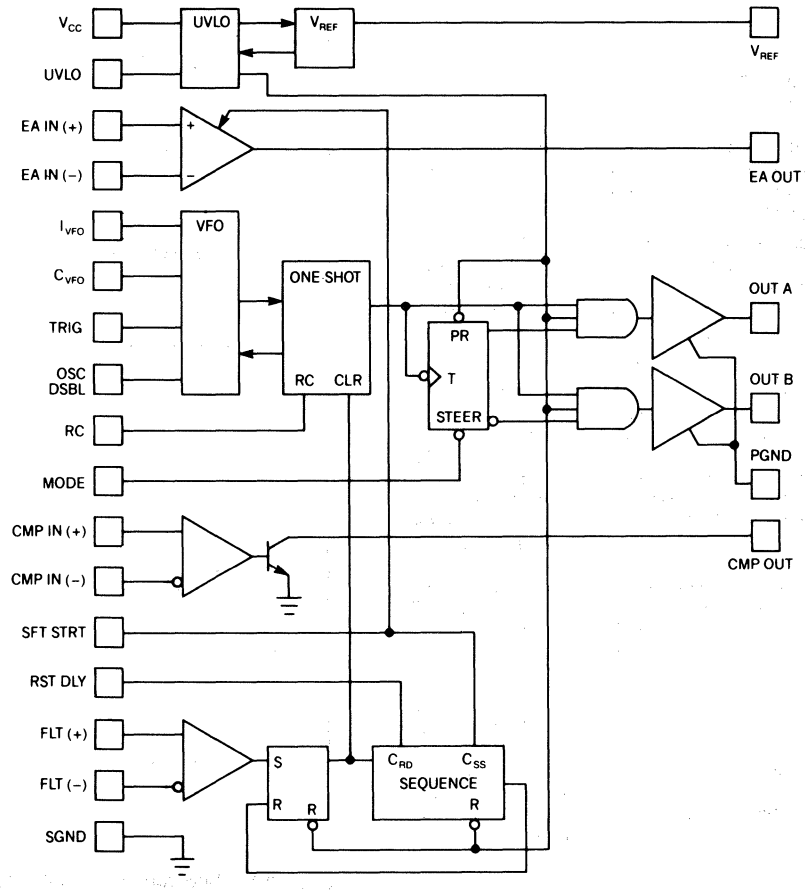


Figure 27 - UC3860 Block Diagram

Fixed on-time pulse widths are generated by the programmable one-shot timing circuit. An RC network is charged by an internal source at the onset of a cycle, then self discharges during the on-time. This occurs between the precise thrsholds of the one-shot's comparators. On-time can easily be shortened by an external in fluence used to discharge the RC components below the comparator's turn-off threshold. This architecture simplifies interfacing with various forms of zero voltage or zero current type switching. The output of the UC3860 uncommitted comparator is an open collector which can interface directly to the one shot (RC) timing pin.

Programming the VFO and One-shot:

Let C_{vfo} = 330 pF, $C_{oneshot}$ = 330 pF
f_{max} = 1.05 MHz, f_{min} = 200 KHz

1. $f_{max} = 2V/R_{vfo}\ C_{vfo}$;
$R_{vfo} = 2/(1.05MHz * 330\ pF) = 5.77\Omega$

2. $f_{min} = 1V/R_m\ C_{vfo}$;
$R_m = 1/(0.2MHz * 330\ pF) = 15.5\ k\Omega$

3. $t_{on} = 0.22 * R_{on} * C_{on}$;
$R_{on} = 600ns/(0.22 * 330\ pF) = 8.26\ k\Omega$

The output from the one-shot feeds another programmable module, the toggle flip-flop. Logic selection at the Output Mode pin either alternates the outputs for the dual-ended configurations, or unifies outputs A with B for single ended applications. As V_{ref} becomes valid, the toggle flip-flop is always steered towards the A output. While this may be of little concern in some designs, a predictable sequence of events upon power-up is always facilitated.

Each totem-pole output is specified for 3 Amp peak drive pulses, sufficient to insure abrupt transitions at the Mosfet switches. When operating in unison, a 6 A peak current is obtained. Rise and fall times into a 1 nF load are typically 20 nanoseconds. As seen in previous high power IC's, the totem pole power ground is terminated through a separate pin which isolates its power ground noise from that of the IC's signal ground.

Soft start is accomplished by limiting the amplifiers output voltage to that of the soft start pin, typical in most IC controllers. An internal 5 microamp current source from V_{ref} pulls up on the external soft start capacitor, which gradually increases the conversion frequency upon start-up, as opposed to widening the pulse width in conventional PWMs.

Fault protection and management circuits included in the UC3860 are fully user programmable. A fault comparator which has both inverting and non inverting inputs is used to drive a programmable sequence latch. The operation of this latch is controlled at the programmable Restart Delay (RST DLY) pin, and has three unique modes. First, it can be oriented to latch the outputs off until UVLO or V_{cc} are toggled, similar to firing a shutdown SCR. Secondly, it can be used to cease operation until the fault input is removed from the comparator, then recommence operation. The third and most popular mode is often referred to as "hic-cup" mode. After receiving a fault, the outputs are turned off for a programmed time interval called the restart delay. Operation is then resumed, provided of course that the fault was removed. Implementation only requires a capacitor from RST DLY to ground.

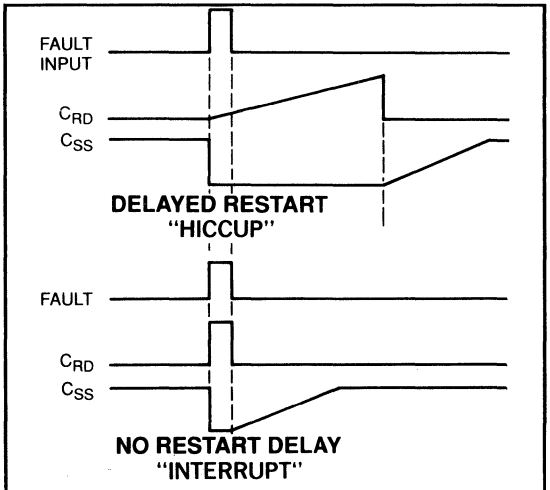


Figure 29 - Fault Management Waverorms

Closing the Loop

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

Error Amplifier: A reference voltage is applied to the noninverting input of the error amplilfier, and the power supply output voltage, through a voltage divider, is applied to inverting input. The error amplifier (E/A) output is commonly referred to as the error voltage V_e, which is an amplifier signal corresponding to the deviation of the power supply output voltage from the desired level. The compensation network is designed last, after analyzing the other loop gain contributors. It will provide adequate phase margin at the desired zero dB crossover point to ensure circuit stability.

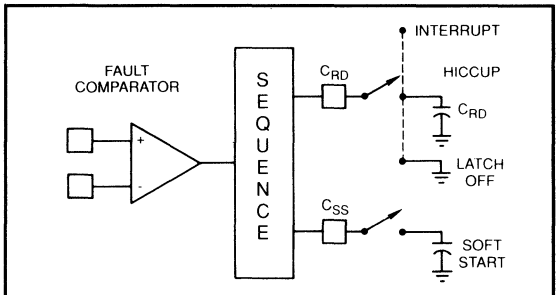


Figure 28 - Fault Management Programming

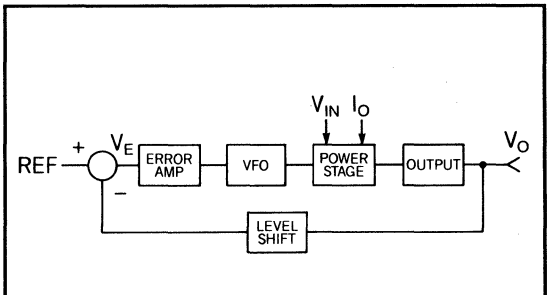


Figure 30 - Control Loop Block Diagram

The varying E/A output voltage V_e is used to gnerate a variable current to the VFO current input pin, I_{vfo}. As this current is varied, so is the power stage conversion frequency. A higher V_e corresponds to a higher conversion frequency. These values are designed to track each other over temperature, and a linear voltage to current transformation can be assumed. The voltage to current gain into the VFO equals the 2 volt maximum output swing of the error amplifier divided by the VFO input resistor.

Variable frequency oscillator: The variable frequency converter stage accepts an input current at the I_{vfo} input and generates a proportional output frequency. The gain of this stage is programmed by the E/A output voltage with the I_{vfo} input resistor and the VFO timing capacitor, C_{vfo}. The VFO output frequency is approximated by:

$f_{osc} = I_{vfo} / C_{vfo}$, and $f_{max} = 2V/(R_{vfo} * C_{vfo})$

The minimum frequency is programmed by a resistor from V_{ref} to the I_{vfo} input, and the transformation of the error amplifier output voltage to frequency is quite linear.

Error amplifier voltage swing = 2 Volts

f_{conv} = 200KHz min = 1 MHz max

VFO gain:

$G_{vfo} = \Delta 800$ kHz / $\Delta 2$ V = 0.4 MHz/V

Power stage: The small signal gain of the power stage is approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch *on* time is constant, and any changes in frequency directly effect the *off* time, or resonant capacitor discharge time. In addition, both V_{IN} and I_{out} are assumed to be constant during the interval of interest.

Based on the relationship that the energy into the resonant circuit, W, equals the output power multiplied by the conversion period:

$W = (Q_{in}\ V_{sec} / 2) = \text{Power} * t_{conv}$
$= V_{out}\ I_{out} / f_{conv}$

therefore:

$V_{out} = f_{conv}\ W / I_{out}$

This term is assumed constant for the interval of interest.

Tabulated below at several points of interest are the values for the values for the power stage gain, from the results of a previous section in this presentation. The gain (in volts per MHz) varies significantly over the input and output ranges and the highest value will be used to approximate the worst case conditon.

V_{IN} sec V	I_{out} A	W_{in} µJ/cyc	f_{conv} kHz	Gain V/MHz	Gain dB
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	21.4	26.6
22	7.5	78	900	19.3	25.7
38	7.5	185	450	22.6	27.0
22	10	91	1000	19.1	25.6
38	10	205	560	23.6	27.5

The worst case value of 23.6 V/MHz will be used for the power stage. Multiplying this by the VFO gain of 0.4 MHz/V results in a combined gain V_{out}/V_e of 9.44 (19.5 dB).

Output Filter Section: The output filter response is defined by:

L_{out} = 80 µH; C_{out} = 200 µF

R_{out} = 1.5 Ω min to 10 Ω max

ESR = 2 to 10 m Ω

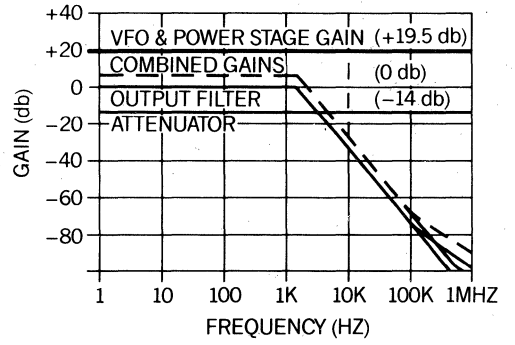


Figure 31 - Gains vs. Frequency

$$\textit{Pole frequency} = \frac{1}{2\pi\ (L_{out}\ c_{out}{}^{0.5})} = 1.25\ kHz$$

$$\textit{ESR Zero} = \frac{1}{2\pi C_{out}\ ESR} = 79.6 - 398\ kHz$$

The output voltage divider shifts the level of the 15 V output to the required 3 V error amplifier input, resulting in a gain of -14 dB.

Compensating the quasi-resonant converter: The generalized approach to this compensation is to place the first pole at a low frequency, typically arond one hertz. Two zeros are then introduced at approximately the output filter break frequency to compensate for its two pole rolloff. A second pole is place at a fairly high frequency to roll off the loop gain in a predictable manner. Unlike their predecessors, the newer control Ics rarely run out of gain bandwidth and require this high frequency pole.

Most of the previously described elements can be lumped together into one gain vs. frequency Bode plot of everything except the error amplifier, as shown in Fig. 31. The VFO, power stage and level shifting voltage divider have gains that are independent of frequency, and are easily combined. The output filter section response is then multiplied by the combined gain of the previous calculation. One curve now depicts the entire loop response from the error amplifier output to its input.

The desired characteristic of overall loop including its zero dB crossover frequency can be shown in a Bode plot, as in Fig. 32. The E/A compensation network will include two zeros near the output filter break frequency to cancel these two poles. Assume for now that the high frequency pole of this circuitry will be around or above the overall zero dB crossover point. The required error amplifier response can now be approximated graphically from the curve and points plotted.

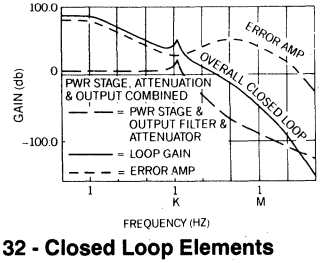


Figure 32 - Closed Loop Elements

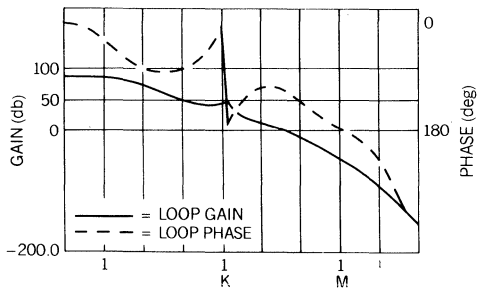


Figure 33 - Loop Gain and Phase

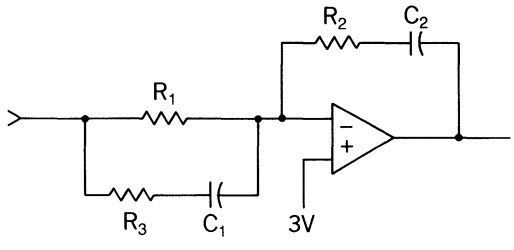


Figure 34 - E/A Compensation Newtork

In this example, two zeros will be introduced in the error amplifier response near the output filter break frequency of 1.25 kHz. A pole is located near the zero dB crossover point at 50 kilohertz. The actual gain and phase obtained in the overall loop is given in Fig. 33

The error amplifier with its compensation network is shown in Fig. 34. It provides high gain at low frequencies and good transient response.

Zero 1:1 ($2\pi R_1C_1$)
Zero 2: $1/(2\pi R_2C_2)$
Pole 1: $1/(2\pi R_3C_1)$
Max Gain: $R_2/(R_1$ & R_3 in parallel)

Input impedance is the parallel combination of R_1, R_2,and R_3

The compensation network is designed to produce:

Zero 1 and Zero 2 at 1.24 kHz

Pole 1 at 70 KHz

> 55 dB loop gain at 50 kHz

Using the previous equations and solving:

R_1 = 6.03K R_2 = 78.1K R3 = 100Ω

C_1 = 22 nF C_2 = 1.7 nF

From the Bode plot of the closed loop response, the supply is compensated to cross 0 dB at approximately 35 kHz, with ample phase margin.

Power Supply Performance

This 150 watt power supply was evaluated while being exercised over various line and load conditions, and exhibited excellent regulation. Response to dynamic loading was well within reasonable limits with little overshoot. Short circuit input current is extremely low, due to the programmed restart delay time constant of 50 milliseconds and soft start of 5 milliseconds.

High efficiency (above 80%) is achieved over the operating ranges. This is quite respectable for a high frequency, off-line power supply. The power stage was constructed on a double sided printed circuit board used for a precious high frequency example (1.5 MHZ current mode) in 1986.

The control circuit is constructed on the Unitrode UC3860 development PC board. The utilization of a ground plane precedes all circuit layout in megaHertz switch mode power designs, and is incorporated here. Coaxial cable interconnects the gate drive, current sense and output voltage signals between the control and power boards. Observation of the circuit waveforms requires the use of a UHF type scope probe socket, or chassis socket. Any length of ground or hook-up wire will distort the true waveforms.

Summary

Above several hundred kiloHertz, the square wave converter may not be optimal for off line designs. Losses associated with switching high voltages at high currents substantially reduce efficiency, power design and generate much EMI. The need for an alternative solution have resulted in various resonant and quasi-resonant approaches, each witih a unique set of merits, applications and control circuit requirements.

The UC3860 controller has integrated the numerous specific functions and "building blocks" required for resonant and quasi-resonant topologies. Configuration for fixed on-time, variable frequency operation is straightforward, and other adaptations are easily made possible. The uncommitted comparator interfaces well with zero current type switching arrangements. Thye UC3860's high speed logic, high power outputs and fault protection circuitry combine for an ideal mix of brains, brawn and speed.

REFERENCES

Unitrode Publications:

Unitrode Power Supply Design Seminar SEM-500:

A2 High Frequency Series Resonant Power Supply Design Review

M5 Power Transformer Design For Switching Power Supplies

M2 Winding Data

C1 Closing The Feedback Loop and Appendices

Other Unitrode Papers:

W. Andreycak, "3 Megahertz Resonant Mode Control IC Regulates 150 Watt Off-Line Supply", *High Frequency Power Conference,* 1988.

R. Mammano, "Resonant Mode Converter Topologies", *Unitrode Power Supply Design Seminar SEM600, Topic 1",* 1988

L. Wofford, "UC1860 - New IC Controls Resonant Mode Power Circuits", *Applied Power Electronics Conference,* 1988.

Additional Referernces:

P. Vinciarelli, "Forward Converter Switching At Zero Current", *U.S. Patent # 4,415,959*

Intertec Communications Press, "Recent Developments In Resonant Power Conversion", 1988 (628 pages - various papers and authors)

9

Resonant Circuits-"Rust Remover" and Appendix

The abrupt transition from conventional square wave conversion to a resonant or quasi-resonant approach can be softened by a review of certain fundamentals. Fig. A1 shows the sine and cosine waveforms along with the timing

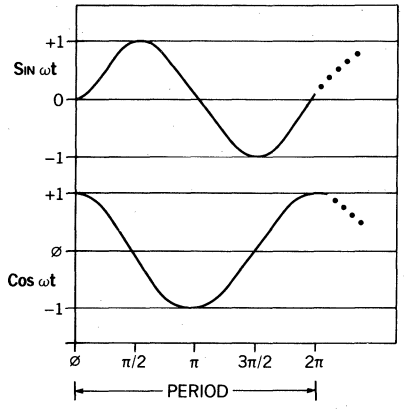
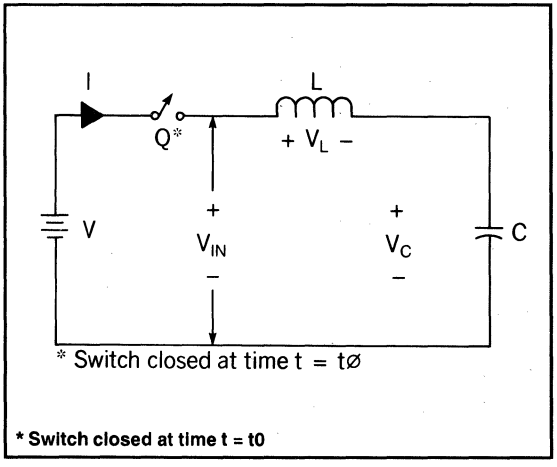


Figure A1 - Sine, Cosine Relationships relationships

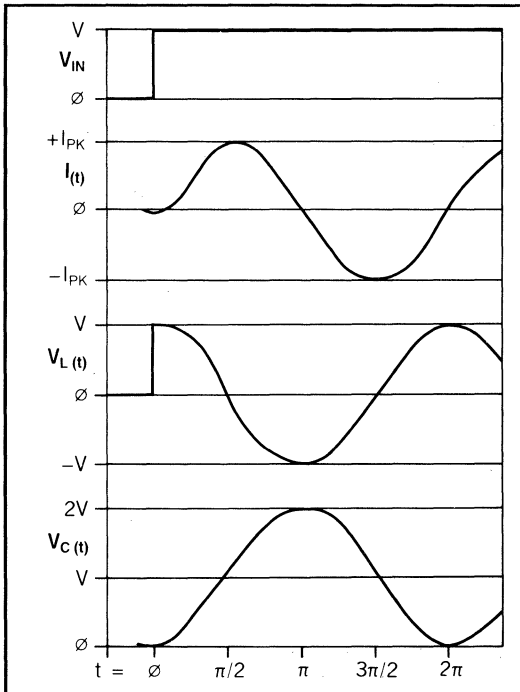


*** Switch closed at time t = t0**

Frequency = $\omega/2\pi$
$T_{period} = 1/f = 2\pi/\omega$

More specific to power conversion, a series resonant LC network driven by a DC voltage source is presented with its corresponding waveforms and equations in Figs. A2 and A3.

$\omega = 1/(LC)^{1/2}$, $Zr = (L/C)^{1/2}$
$i_{pk} = V_{IN} / Z_r$
$i = i_{pk} \sin(\omega t) = V_{IN} \sin(\omega t) / Zr$
$V_L = V_{IN} \cos(\omega t)$
$V_C = V_{IN} [1-\cos(\omega t)]$



Figures A2, A3 - Series Resonant Circuit

Resonant circuit timing relationships and waveforms: The waveforms of a series resonant, parallel loaded circuit will be analyzed in detail and used to generate the relationships between time, current, charge and energy transfer in a a resonant circuit application. Specifically, the buck topology will be used in this example, which can be applied to other topologies and configurations.

The cycle is initiated at time t_o Switch Q1 closes, delivering a rectangular voltage waveform to the resonant circuit. The input current rises linearly to I_{out} at a slope equal to V_{IN}/L_r. It reaches the constant output current level I_{out} at time t_1. The time for this to occur is $\Delta 10 = (t_1-t_0)$. During this interval, all resonant inductor current is directed to the output and none delivered to the resonant capacitor, C_r.

At t_o:

$i_{in} = 0$, $i_{cr} = 0$, $v_{cr} = 0$

From t_o to t_1,

$i_{in} = V_{IN} t / L_r$

At t_1, $i_{in} = I_{out}$

$\Delta t_{10} = L_r I_{out} / V_{IN}$

At time t_1, the input current equals the fixed current I_{out}. The resonant L_r & C_r tank components begin their resonant cycle at zero current, and the input current rises sinusoidally to its peak of $I_{out} + V_{IN}/Z_r$, It will later intersect the output current I_{out} again at time t_2 corresponding to 1/2 the resonant tank period, π radians.

At t_1:

$I_{in} = I_{out}$, $i_{cr} = 0$, $v_{cr} = 0$

From t_1 to t_2:

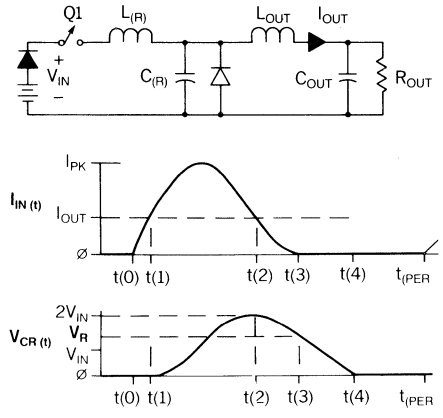
$i_{in} = I_{out} + (V_{IN}/Z_r)\sin\omega(t\text{-}t_1)$

$\Delta t_{21} = \omega/\pi = 1/(2f) = 1/\pi(L_rC_r)^{1/2}$

$$i_{cr} = \frac{V_{IN}}{Z_r} \sin \omega(t\text{–}t_1)$$

$V_{cr} = V_{IN}(1\text{-}\cos\omega(t\text{-}t_1))$

Once the input (inductor) current crosses I_{out} at time t_2 it continues sinusoidally until it reaches zero at time t_3. At th is point, switch Q_1 is turned off to faciiitate zero current switching. The time required to reach zero current from I_{out} is Δ32, and depends upon the amplitude of I_{out} and V_{IN}.



Figures A4, A5 - Quasi Resonant Buck Converter

At t_2:

$i_{in} = I_{out}$, $i_r = 0$, $v_{cr} \sim 2V_{in}$

From t_2 to t_3:

$$\Delta t_{32} = \frac{1}{\omega} \sin^{-1}\left[\frac{I_{out}Z_r}{V_{in}}\right]$$

$$i_{in} = I_{out} + \frac{V_{IN}}{Z_r} \sin \omega(t\text{–}t_1)$$

$V_{cr} = V_{IN}(1\text{-}\cos\omega(t\text{-}t_1))$

The resonant capacitor voltage v_{Cr} discharges linearly during the interval of Δt43, beginning at time t_3. The capacitor voltage and Δt43 are determined from the following equations:

At t_3:

$i_{in} = 0$, $i_{cr} = 0$

From t_3 to t_4:

$v_{cr} = v_{cr(t3)} - I_{out}(t - t_3)/C_r$

$\Delta t_{43} = C_r v_{c(t3)} / I_{out}$

Evident from the previous equations is the need to vary the output *on* time to respond to the various line, load and resonant tank circuit influences.

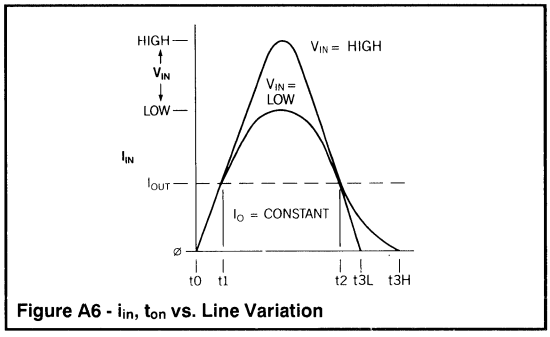


Figure A6 - i_{in}, t_{on} vs. Line Variation

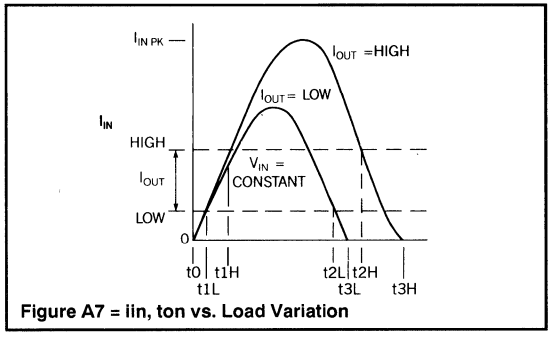


Figure A7 = iin, ton vs. Load Variation

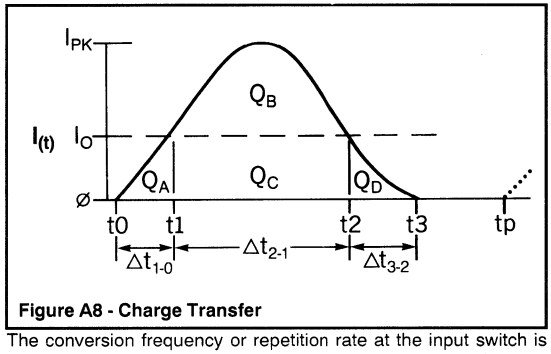


Figure A8 - Charge Transfer

The conversion frequency or repetition rate at the input switch is approximated following some intermediate calculations for total energy transfer from input to output, as follows:

Charge Transfer in the Resonant Circuit

During each resonant cycle a specific amount of charge (Q) is taken from the input supply and transferred to the output load. The corresponding energy (watt-sec) transferred is simply the charge (Q) multiplied by the input voltage V_{IN}. This relationship will be used to approximate the conversion frequencies required to regulate an output voltage for various ranges of input voltages and output currents.

The input current waveform will be divided into four specific intervals to simplify the calculations. The charge transferred in each interval will be calculated by integrating the current waveform throughout the interval.

Qa. The charge transferred during the time interval from to t_o t_1 is

9

calculated from the equation for the area of the triangle formed:

$\Delta t_{1\text{-}0} = LI_o/V_{IN}$

Qa: $= \Delta t_{1\text{-}0} I_o/2 = L_{Iout}{}^2/(2V_{IN})$

Qb: During this resonant half-period, the sinusoidal portion of the input current waveform is integrated over the interval t_1 to t_2.

$i_{in} - I_{out} = (V_{IN} / Z_r)\sin\omega(t\text{-}t_1)$

$$Q_b = \frac{V_{IN}}{Z_r}\int_{t1}^{t2} \sin(\omega(t-t_1))dt$$

$$Q_b = \frac{V_{IN}}{Z_r}\omega\left[-\cos\theta\right]_0^{\pi}$$

$1/ Zr\omega = C_r$

$\therefore Qb = 2VIN\ Cr$

Qc: The rectangular area of charge delivered to the output during interval t_1 to t_2 is:

$Qc = I_{out}\ \Delta\ t2_1$, where $\Delta\tau 2_1 = \pi/\omega$

$Qc = \pi I_{out} / \omega$

Qd: The sinusoidal current decreases from I_{out} to zero during the t_2 and t_3 interval. The charge transferred is calculated by subtracting the sinusoidal component from the rectangular region formed by I_{out} and t_3.

$$Qd = I_{out}\ \Delta\ t_{32} + I_r\int_{t2}^{t3} \sin(\omega(t-t_1))dt$$

$$Qd = I_{out}\ \Delta\ t32 - \frac{V_{IN}}{Z_n\,\omega}\left[\cos\theta\right]_{\pi}^{\pi\ +\ \omega\Delta t\,32}$$

$$Qd = I_{out}\ \Delta\ t_{32} - V_{IN}\ C_r\ [\cos(\pi + \omega\ \Delta\ t_{32}) - \cos\pi]$$

$$\Delta\ t_{32} \approx (1/\omega)sin^{-1}(I_{out}\ Z_n\ /\ V_{IN})$$

For practical purposes, this area can be repesented by a linear approximation without a significant compromise in accuracy. The area formed by $I_{out}\Delta t_{32}/2$ is a reasonable estimate of the area, resulting in approximately 1% error in the total charge transferred.

$Qd \approx I_{out}\ \Delta t_{32}/2 = (1/2\omega) I_{out} \sin^{-1}(I_{out}\ Z_n\ /V_{IN})$

Qt: The total charge transferred from the input to the output per cycle is the summation of charges Qa through Qd.

$Qt = Qa + Qb + Qc + Qd$

$$Qt = \frac{LI_{out}{}^2}{2V_{In}} + 2V_{IN}C_r + \frac{\pi\ I_{out}}{\omega} + \frac{I_{out}}{2\omega}\sin^{-1}\frac{I_oZ_n}{V_{IN}}$$

The approximation made to simplify the calculation of charge Qd also allows the substitution of charge Qa for Qd, thus reducing the total charge transfer to the following.

$Qt = 2Qa + Qb + Qc$

$$Q_t = \frac{LI_{out}{}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}$$

Energy Transfer During the Resonant Cycle

The energy per cycle, W, can be calculated by multiplying the input voltage V_{IN} by the total charge Qt transferred from the input to the output. Dividing the energy per cycle W by the output power P_{out} unveils the conversion period - the inverse of the switching frequency.

$$T_{conv} = \frac{W/cycle}{P_{out}} = \frac{V_{IN}\ Q_t}{V_{out}\ I_{out}}$$

$$= \frac{V_{IN}}{V_{out}\ I_{out}}(Qa + Qb + Qc + Qd)$$

$$= \frac{V_{IN}}{V_{out}I_{out}}(2Qa + Qb + Qc)$$

$$T_{conv} \approx \frac{V_{IN}}{V_{out}\ I_{out}}\left[\frac{L_rI_{out}{}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}\right]$$

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A NEW FAMILY OF INTEGRATED CIRCUITS CONTROLS RESONANT MODE POWER CONVERTERS

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ABSTRACT

A new family of integrated circuits is introduced. Devices from this family implement the necessary architecture to control a broad range of resonant mode converters. Key features in the areas of switch timing, fault management, and soft-start technique are unique to this family. Individual devices are customized to handle off-line or DC to DC, single-ended or dual-switch, zero-voltage-or-current-switched configurations. Specific application to three different resonant mode converters is mentioned.

SURVEY OF EXISTING CONTROL INTEGRATED CIRCUITS

Since 1986, interest in resonant mode power conversion has exploded in the technical conferences. IC makers have been quick to respond with offerings of control ICs. Table 1 is a list of chips available at the present time. To simplify thinking, the first three parts listed are essentially the same design as are the last two. There are significant differences in features and performance levels between the three groups. However, a common operational philosophy is shared by all: fixed-pulse-width variable-frequency. This approach has been applied to zero-current-switched (ZCS), quasi-resonant mode converters with reported success.

Table 1. List of Resonant Mode Control ICs

LD405
GP605
CS3805
- - - - - -
UC3860
- - - - - -
MC34066
CS360

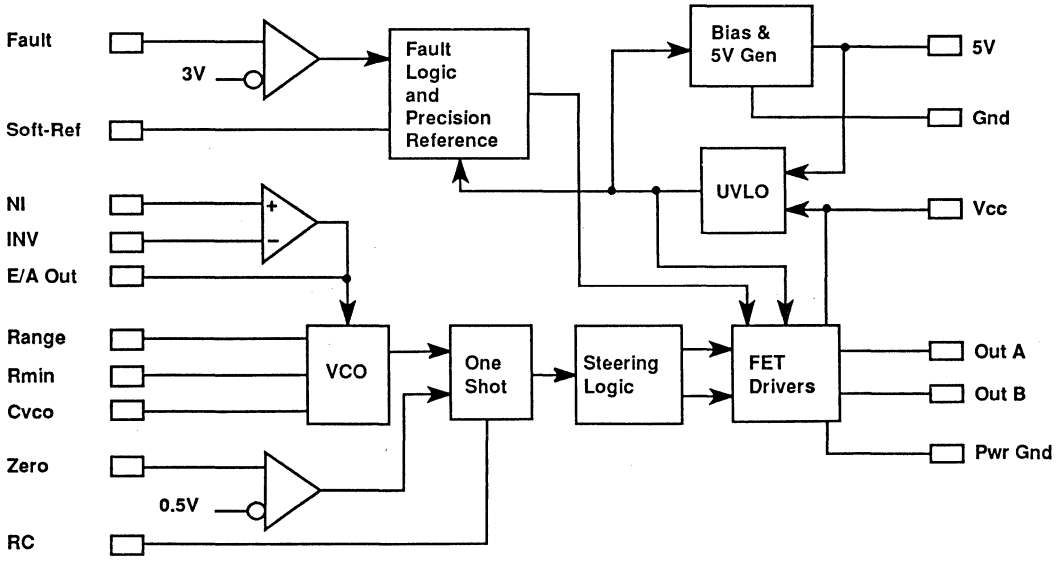

Figure 1. Controller Block Diagram

NEW FAMILY OF RESONANT MODE CONTROL INTEGRATED CIRCUITS

As the discipline is maturing, the advantage of some feature changes has become apparent. Versatility to control both ZCS and zero-voltage-switched (ZVS) converters is needed. The ability to control proper switch times (on or off) with changing line, load, or component values is needed. To address these needs, a family of controllers based on a common silicon die has been developed. Three members of the family, the UC1861, UC1864, and UC1865 will be covered in detail.

The common block diagram of the family is illustrated in figure 1. These parts feature an error amplifier (E/A), voltage controlled oscillator (VCO), one shot timing generator with a zero wave-crossing detection comparator, steering logic to two output drivers, a 5V bias generator, and under voltage lockout (UVLO). A latched fault management scheme provides soft start, restart delay, and a precision reference.

Die options can be produced that give different UVLO levels, as well as different output properties. There are two UVLO options. The first, suited for off-line operation has thresholds of 16 and 10V. While UVLO is active, Icc is less than 0.3mA. The other option is 8 and 7V, to accommodate lower input voltage DC/DC converters.

The flavor of the outputs required by different resonant mode topologies requires the steering logic to be configured specially for each application. The basic options that can be built allow for single or dual switch drive, and controlled on or off times. Zero-current-switching applications require controlled switch on times while zero-voltage-switching applications require controlled switch off times. Figure 2 shows these options.

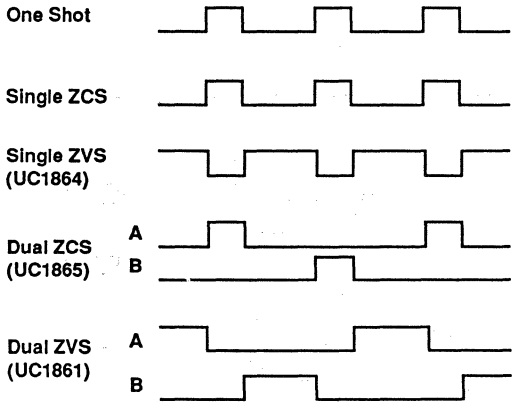

Figure 2. Output Drive For Different Converters

Table 2 details the options implemented in the 1861, '64, and '65. Other options can be built from the same die.

Table 2. Implemented Options in the 1861, '64, '65.

Device	UVLO Vth	Outputs	Zero-(?)-Switching
UC1861	16/10V	Dual	Voltage
UC1864	8/7V	Single	Voltage
UC1865	16/10V	Dual	Current

PRIMARY CONTROL BLOCKS

The fundamental control blocks essential for a majority of resonant mode converters are an error amplifier, VCO, one shot timing generator, and output stage to drive power mosfets.

ERROR AMP & VOLTAGE CONTROLLED OSCILLATOR

Figure 3 details the E/A and VCO. The E/A output directly controls the VCO via the Irange generator. The VCO has inputs for two resistors, R_{ange} and R_{min}, and one capacitor, C_{vco}. R_{min} and C_{vco} determine minimum frequency.

$$F_{min} = \frac{3.6}{(R_{min} * C_{vco})} \quad (1)$$

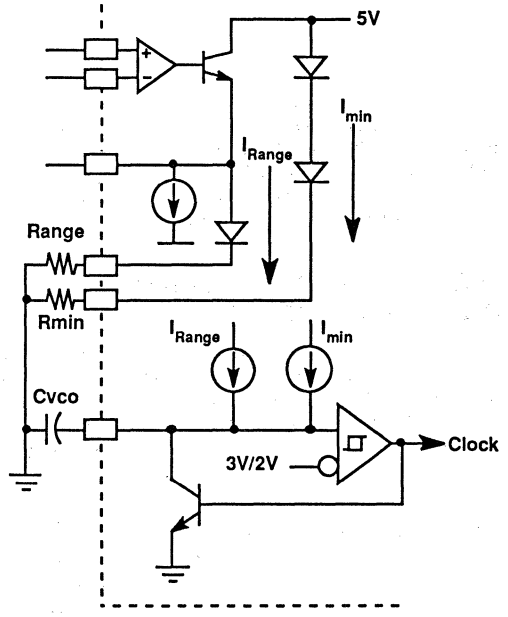

Figure 3. Error Amplifier and Voltage Controlled Oscillator

When the output of the E/A is less than or equal to one diode drop above ground, the VCO operates at minimum frequency. The E/A output can go as high as one diode drop below 5V. When at this potential, the VCO frequency is at its maximum.

$$F_{max} = \frac{3.6}{(R_{ange} \| R_{min}) * C_{vco}} \quad (2)$$

Usable maximum frequency tops out around 1.5MHz. The Frequency range is the difference in equations 2 and 1.

$$\Delta F = \frac{3.6}{R_{ange} * C_{vco}} \quad (3)$$

Since the nominal E/A output swing is approximately 3.6V for full variation in VCO frequency, the gain of the VCO block is

$$dF/dV = \frac{1}{R_{ange} * C_{vco}} \quad (4)$$

In ZCS power supplies, an increase in frequency will correspond to an increase in the converter's output voltage. For these applications the E/A non-inverting input is connected to a reference voltage while the output voltage sense is fed back to the inverting input. For ZVS power supplies, a decrease in frequency corresponds to an increase in output voltage. For these systems, the inputs to the E/A are exchanged.

The common mode range of the E/A is from zero to 6V. This feature allows zero volts to be a valid reference voltage applied to the E/A. Soft start, covered later, takes advantage of this feature.

ONE SHOT TIMING REQUIREMENTS

The basic premise in resonant mode conversion is packets of energy delivered at varying repetition rates. Each energy packet dictates a basic switch on or off time, hence the one shot timer. In ZCS systems the switch is on. In ZVS systems the switch is off. The timer, then, should force the switch to conform to the resonant timing of the tank circuit. It is this conformance that achieves zero stress switching.

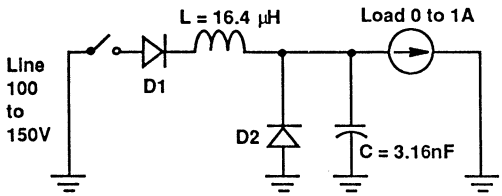

Figure 4. ZCS Resonant Tank Example

For purposes of convenience, a simplified ZCS resonant tank is presented to illustrate the timing requirements of resonant converters in general. This is an example, not a rigorous theoretical presentation. It does, however, demonstrate the problems to overcome in properly controlling a resonant mode converter. The circuit of figure 4 is designed to operate from line inputs of 100 to 150V and 0 to 1A load current. The tank frequency is arbitrarily selected to be 700kHz. A reasonable first guess for tank impedance is determined by

$$Z_o = \frac{V_{lowline}}{I_{max} * 1.386} \quad (5)$$

$$= 72 \text{ ohms.}$$

From the equations governing resonant tank natural frequency and impedance, L and C can be calculated.

$$F_o = \frac{1}{2\pi\sqrt{LC}} = 700\text{kHz} \quad (6)$$

$$Z_o = \sqrt{\frac{L}{C}} = 72 \text{ ohms} \quad (7)$$

$$L = \frac{Z_o}{2\pi F_o} = 16.4\ \mu\text{H} \quad (8)$$

$$C = \frac{1}{2\pi Z_o F_o} = 3.16\text{nF} \quad (9)$$

Figure 5 shows the pertinent current and voltage waveforms for the case of 125V input and 0.8A output. When the switch closes at zero time, the current starts to build linearly. Once the current reaches 0.8A, then load current is completely supplied through the inductor and D2 carries no current. At this point in time the L and C resonate together until inductor current returns to zero. At this time the switch is allowed to turn off, but it doesn't necessarily have to. D1 prevents reverse current in the switch. It isn't necessary to open the switch until the capacitor voltage decays to line voltage. It is acceptable to open the switch any time during this "switch window". If it is opened too soon, the circuit will suffer severe switching losses. If it is not opened, the tank will resume resonating, as shown by the dashed curves. If the switch is opened later than the switch window, not only will the circuit suffer switching losses, but the transfer function becomes overly complex.

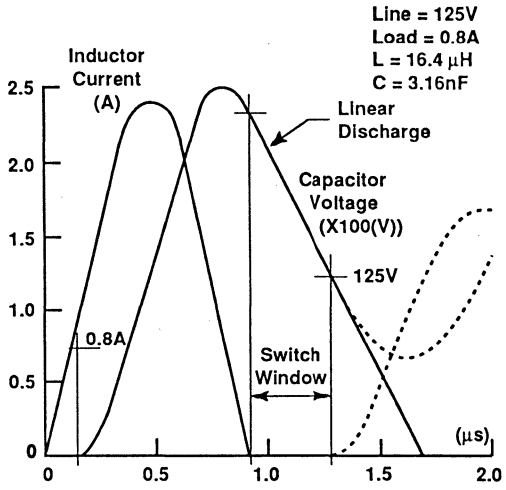

Figure 5. Typical Resonant Tank Waveforms

The graph in figure 6 plots the switch window as a function of load current for both high and low line voltage. For example, at a load current of 0.5A and high line, the switch must be closed for at least 0.80us and need not be opened until 1.61us. Examination reveals the most stringent switch window, 1.03 to 1.21us, occurs at low line and full load. Furthermore, this window is a subset of all other windows. This might lead to choosing a fixed on-time of 1.12us under the assumption that it is relatively easy to build a fixed time one-shot circuit with total variations less than +/-8%. However, further consideration will lead to a different conclusion.

In order to insure that the example in question can be produced, the variations of the resonant components and the possibility of output overload must also be examined. This example continues by assuming total variations for the capacitor are under 10% while under 20% for the inductor. A 20% overload is also allowed.

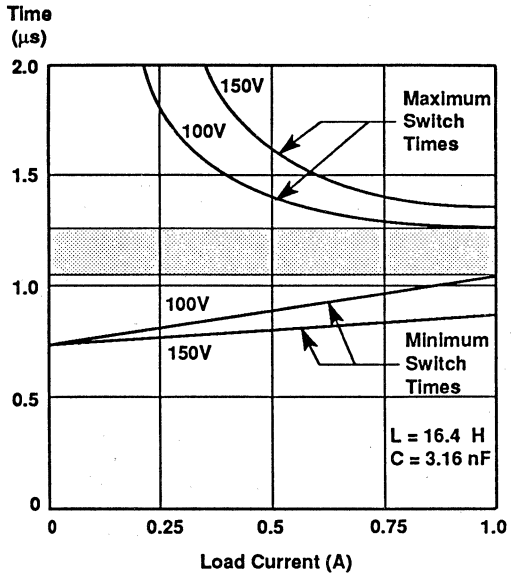

Figure 6. Minimum/Maximum Switch Time vs Load Current

Figure 7 shows the valid switch windows at 1.2A and 100V for nominal component values as well as the four tolerance corners. Several observations can be made. Firstly, the window for the case of +20% inductor and -10% capacitor variations has zero tolerance.

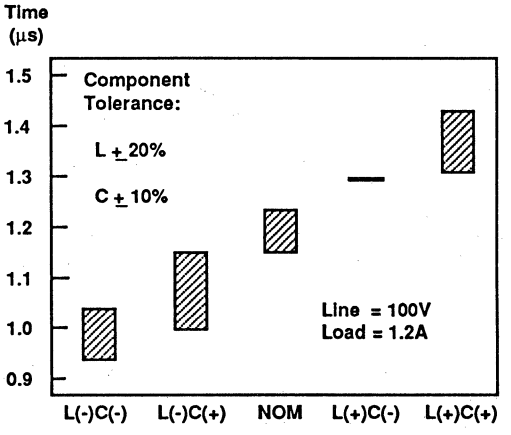

Figure 7. Switch Window vs Component Value

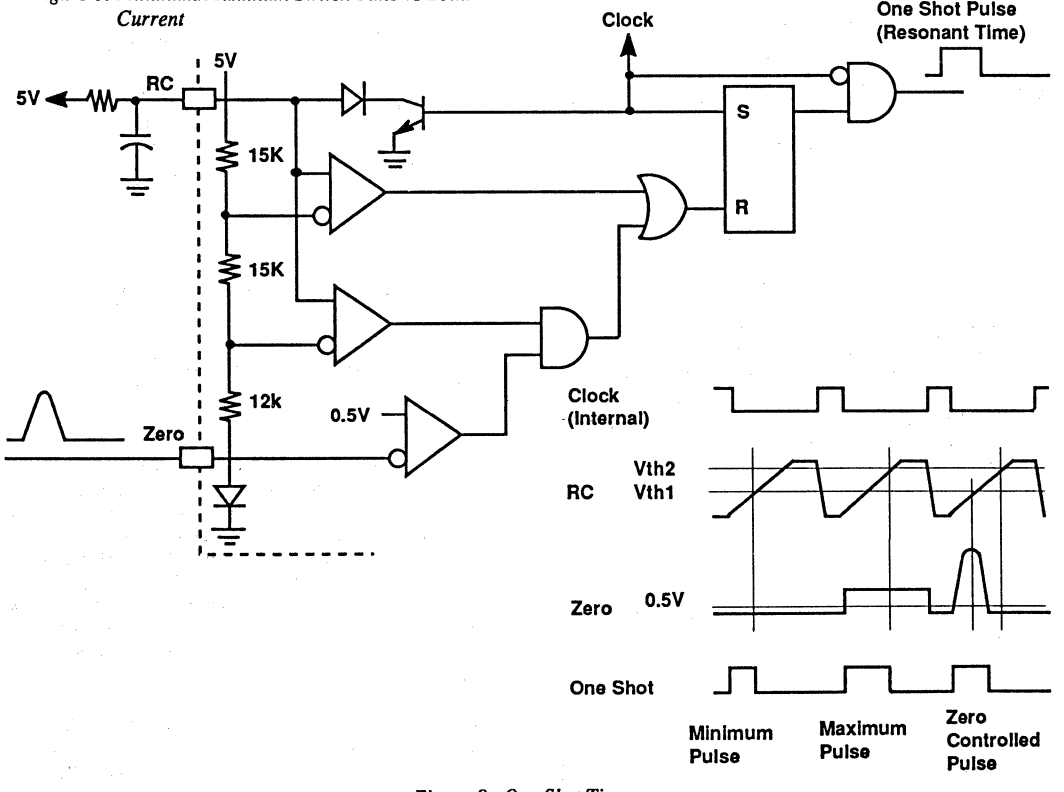

Figure 8. One Shot Timer.

The switch must turn off at 1.30us. This is because the tank impedance is exactly the ratio of low line voltage to overload current for these component values. This is the source of the 1.386 factor in equation 5. Secondly, and the point of the illustration, there is no possible value of fixed switch time that accommodates component variation.

ONE SHOT TIMING GENERATOR

In figure 8, details of the one shot timer are seen. The clock signal from the VCO sets the latch, blanks the output, and causes the RC timing pin to be discharged. The timing pin determines the minimum and maximum times the one shot output will be high.

$$T_{max} = R * C \quad (10)$$

$$T_{min} = 0.3 * T_{max} \quad (11)$$

Between these two limits, the zero detect comparator will terminate the one shot pulse whenever the Zero pin goes below 0.5V. By sensing the zero crossing of the resonant waveform, the one shot adapts to different resonant component values and varying line/load conditions. The switch time will properly track the resonant tank assuring zero stress switching.

STEERING LOGIC & OUTPUT STAGE

Figures 9, 10, and 11, are block diagrams of the steering logic and output stages. Each output stage is a totem pole driver optimized for driving power mosfet gates. Gate currents of 1A can be obtained from each driver. Note the 1864 single driver is actually both drivers on the chip paralleled. Sample waveforms for the three configurations were shown in figure 2.

Fault and UVLO response of the three configurations is identical. These indications always force both drivers to the low state. During UVLO, the outputs can easily sink 20mA irrespective of Vcc.

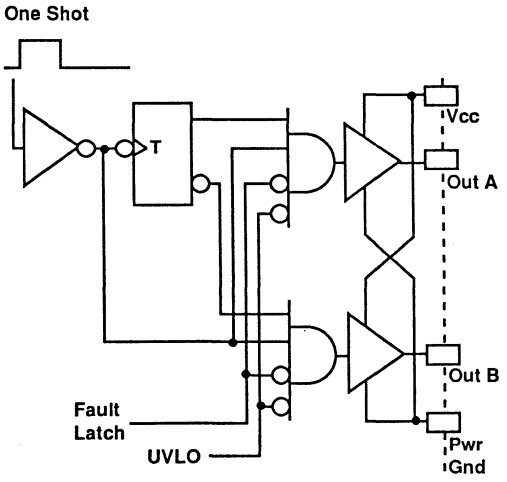

Figure 9. UC1861 Steering Logic

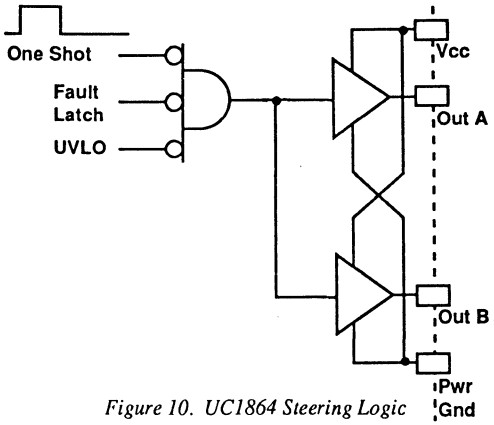

Figure 10. UC1864 Steering Logic

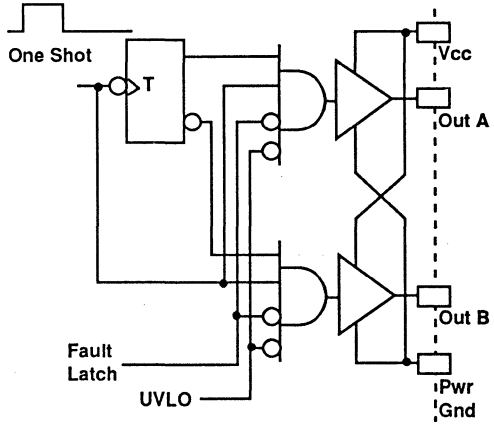

Figure 11. UC1865 Steering Logic

SECONDARY BLOCKS

The secondary blocks on board are UVLO, a 5V bias generator, and fault management with a precision reference. The purpose of the 5V generator is to provide a stable bias environment for internal circuits and up to 10mA of current for external loads. The one shot timing resistor connects to 5V.

UVLO senses both Vcc and 5V. It doesn't allow operation of the chip until both are above preset values. When Vcc is below the UVLO threshold, the 5V generator is off, the outputs are actively pulled low, the fault latch is set, and supply current is less than 300uA.

SOFT START, RESTART DELAY, PRECISION REFERENCE

A novel combination fault management and precision reference is shown in figure 12. One pin is dedicated to a fault sense comparator with a 3V threshold. A second pin does triple duty providing soft start, restart delay, and precision system reference. UVLO initializes the latches, forcing the chip output(s) to be low and the Soft-Ref pin to be discharged. After UVLO, Soft-Ref is charged by an internal 0.5mA current source until is it clamped at

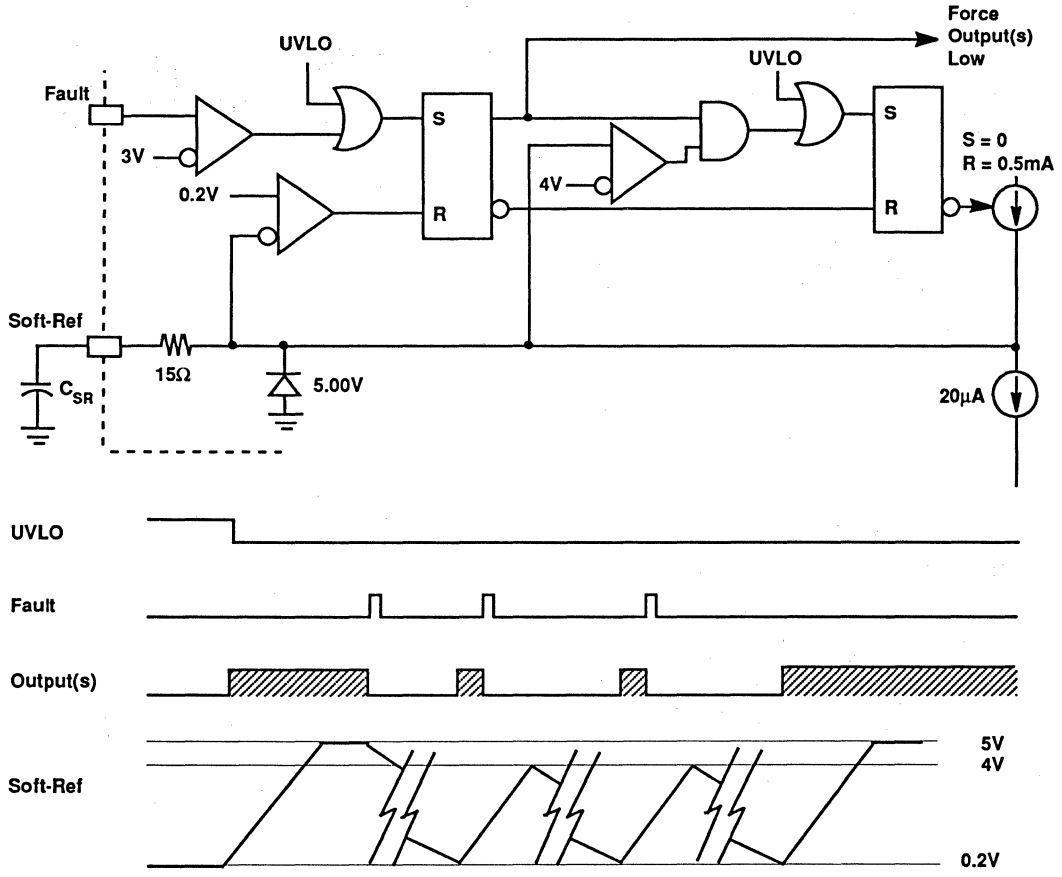

Figure 12. Fault Comparator, Soft Start, Restart Delay And Precision Reference

5V. The soft start time is approximately given by:

$$T_{softstart} = C_{sr} * 10kohms. \quad (12)$$

The recognition of a fault causes the outputs to be driven low and the Soft-Ref pin to be discharged with a 20uA current source. This is the restart delay period. When Soft-Ref reaches 0.2V, the outputs are enabled and the pin is recharged by the 0.5mA current. If a fault should occur before completion of the charge cycle, the outputs are immediately driven low, but the Soft-Ref pin is charged to 4 Volts before the 20uA restart delay current discharges the pin. The restart delay time during continuous fault operation is:

$$T_{restart} = C_{sr} * 190kohms. \quad (13)$$

The ratio of restart delay to soft start is 19:1. If shorter restart delay times are desired, a resistor of 20k or larger can be added from Soft-Ref to ground. The timing equations then become:

$$T_{softstart} = R_{sr} * C_{sr} * \ln\left(\frac{(0.48mA * Rsr) - 0.2}{(0.48mA * Rsr) - 5}\right) \quad (14)$$

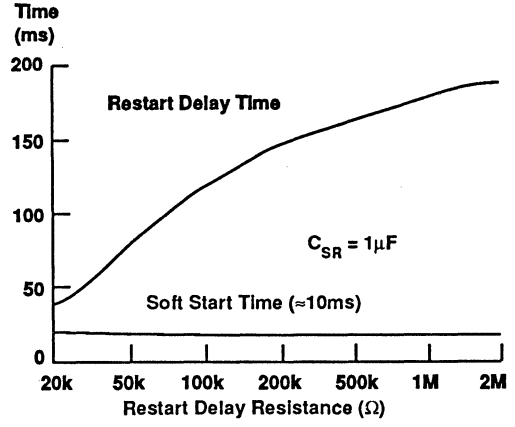

Figure 13. Soft Start And Restart Delay Times

$$T_{restart} = R_{sr} * C_{sr} * \ln\left(\frac{(20uA * Rsr) + 4}{(20uA * Rsr) + 0.2}\right) \quad (15)$$

Soft and restart times are plotted in figure 13 for C_{sr} = 1uF.

The restart feature can be defeated by the addition of a 100k resistor from Soft-Ref to 5V. In this configuration, a fault detection will permanently shut down the converter until either Vcc is recycled and UVLO resets the fault circuit, the 100k resistor is opened, or Soft-Ref is externally pulled to ground. The soft start time becomes:

$$T_{softstart} = C_{sr} * 9.2kohm. \quad (16)$$

The Soft-Ref pin is the system reference pin. By ramping the reference from zero during soft start, the converter output will follow the ramp up under closed loop control. This technique allows controlled starts for both ZCS and ZVS systems with no significant overshoot.

The reference characteristic of the Soft-Ref pin is due to a trimmed 5V zener-type clamp circuit. Fifteen ohms resistance separates the Soft-Ref pin from the clamp to eliminate zener oscillations for any external capacitance value. The clamp zener is designed to tolerate loading of +/- 200uA without degradation of reference accuracy. Loading, however, will alter the soft start and restart delay times, and could even preclude restart delay action unless care is taken in the design.

DC/DC ZVS SINGLE ENDED FORWARD CONVERTER APPLICATION

A ZVS multi-resonant forward converter based on previously reported (ref. 4) work is shown in figure 14. An 1864 is used to control the converter. A 22k resistor from the input line is used to start the circuit, which boot-straps power from the output to the chip after start-up. Before start-up, the chip draws less than 300uA and starts operating when Vcc reaches 8V. After start-up, the 22k resistor dissipates 70mW.

The switch voltage, V_s is sampled with a 100k/5.1k divider network. The chip anticipates zero crossing when V_s = 10V. In this power converter, switch voltages of 200 to 300V are to be expected. A pnp is used to clamp the zero voltage, Vz to prevent damage to the chip. The 100k resistor represents an insignificant load to the resonant circuit.

The paralleled outputs are connected, as good practice dictates, to the mosfet gate with a small-valued resistor. A schottky diode parallels the output pins to protect the chip from negative voltage spikes that might result from parasitic ringing in the gate circuit.

This power stage was demonstrated to have excellent short circuit tolerance when the minimum switching frequency is well controlled. For this reason, the fault input is not used.

Sensed output voltage is scaled & presented to the non-inverting pin of the E/A. The inverting input is DC referenced to the Soft-Ref

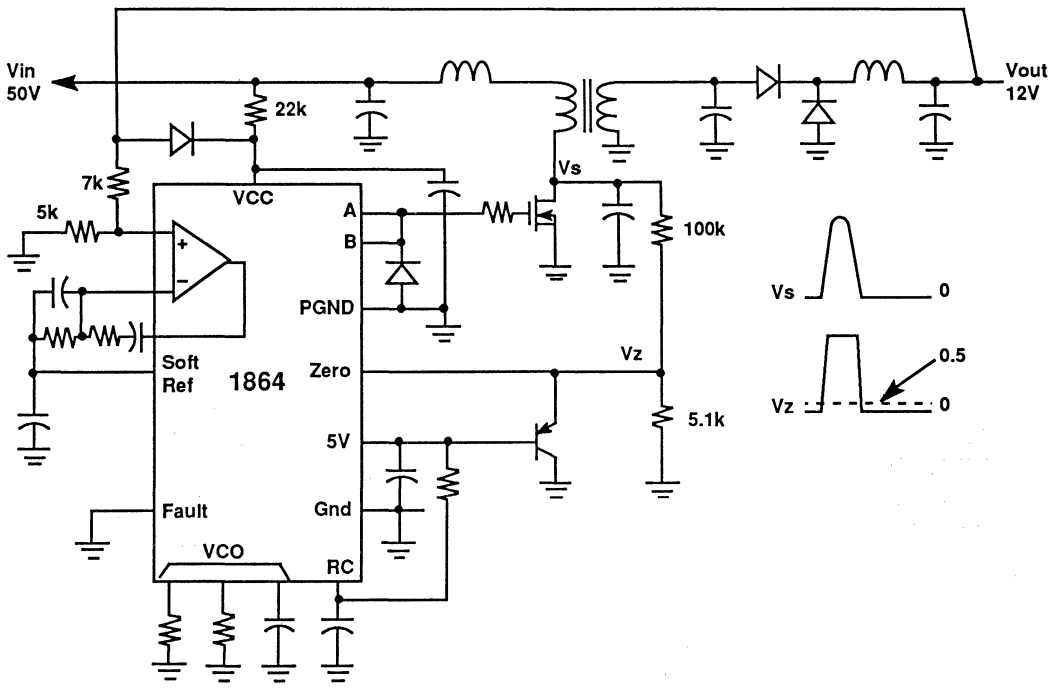

Figure 14. ZVS-MR Forward Converter Controlled By UC1864.

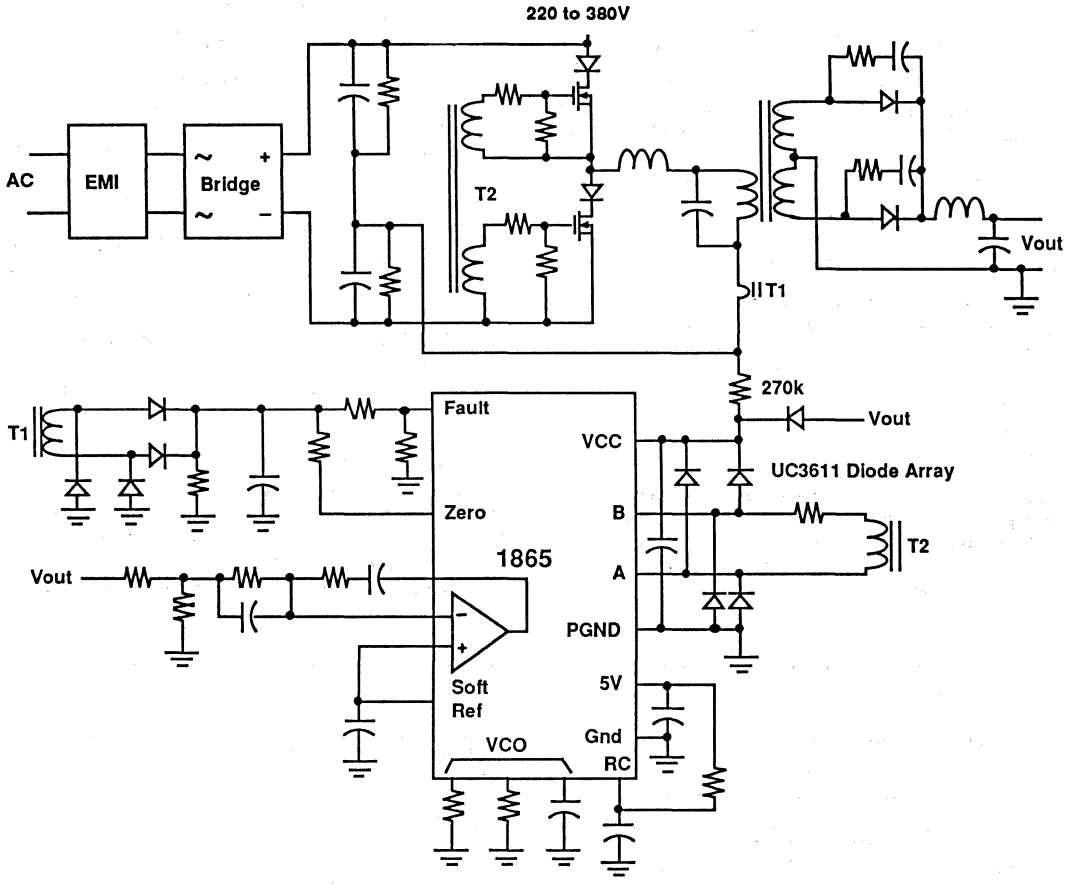

Figure 15. ZCS Off-Line Half-Bridge Converter With UC1865

pin, 5V. The compensation network shown represents zero DC load to the Soft-Ref pin. As long as C_{sr} is much larger than the feedback capacitor, then soft start behavior will be essentially as described in equation 12.

OFF-LINE ZCS HALF-BRIDGE CONVERTER APPLICATION

A ZCS off-line half-bridge converter (ref. 1) with an 1865 control IC is shown in figure 15. Irrelevant details in the converter have been simplified. The wide UVLO hysteresis and low start current of the chip have been used in start-up. A single resistor from the high voltage bus is used to start the circuit which then sustains itself from output voltage.

This circuit samples resonant current with transformer T1. Rectified secondary current, converted to an analog voltage, is applied to the fault and zero inputs of the 1865. Excessive current in the resonant tank will effect a shutdown and restart. The resistor between current sense transformer and the zero pin is to limit

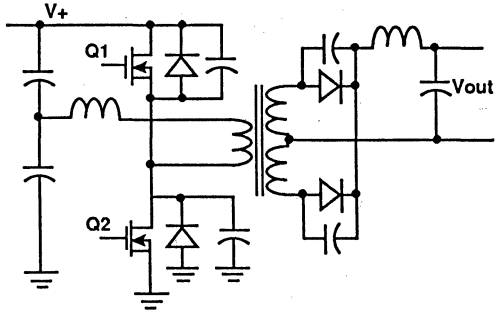

Figure 16. ZVS Half-Bridge Converter

current when the signal is at a high value. The allowable voltage range at the zero pin is zero to 9V, and resistive current limiting to less than 1mA is sufficient.

The half bridge power mosfets are transformer driven from the differentially connected output drivers of the 1865. A UC3611 schottky diode array has been used to prevent the outputs from being forced too far above Vcc or below ground.

The E/A non-inverting input is directly connected to the Soft-Ref pin to take advantage of all three features of the pin. This emphasizes the simplicity of application of the 1865 to this converter.

OFF-LINE ZVS HALF-BRIDGE CONVERTER APPLICATION

An off-line ZVS half-bridge converter (ref. 3) is shown in figure 16. An 1861 controls this converter in much the same manner as the two previous examples and is not shown here. The error amp configuration matches the ZVS example while the output stage is configured like the ZCS example.

This application does, however, present a difficulty in sensing zero voltage to control the one shot. In the first ZVS example, the voltage waveform was ground referenced and unipolar. The ZCS example had bipolar current, but a transformer and diode bridge conditioned the signal for the chip. In this example, zero switch voltage needs to be sensed for both Q1 and Q2. This poses no real problem for Q2. Q1 is another story. Some form of external circuitry must be employed to sense Q1 and translate the information to the ground referenced chip.

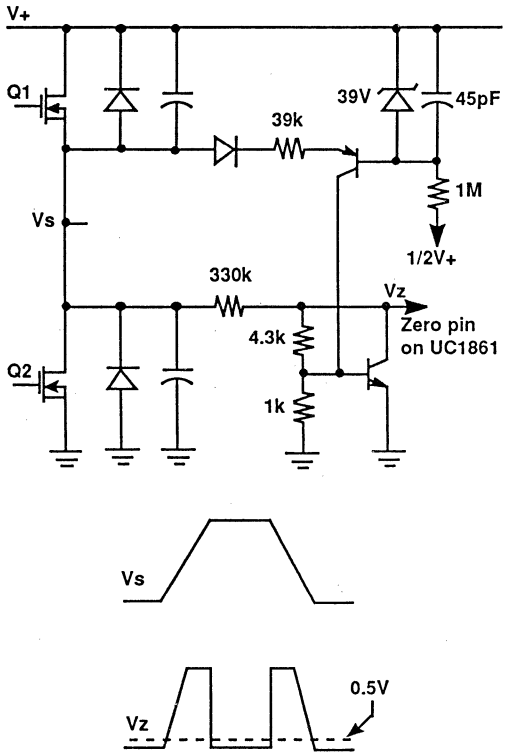

Figure 17. Zero Voltage Sensing Scheme For ZVS Half-Bridge Converter

An easily implemented high voltage comparator circuit is shown in figure 17. The pnp and diode are the only high voltage components used. The circuit dissipates only 300mW. The output of this circuit is applied directly to the zero input of the 1861.

CONCLUSION

A new family of integrated circuits to control resonant mode converters has been introduced that provides several improved features over those previously available. This family has parts that are suited not only to zero-current-switching, but also to zero-voltage-switching converters. The 1861, 1864, and 1865 are suited to off-line ZVS, DC/DC single ended ZVS, and off-line ZCS systems. Controllers for other specific converters can be built from this family. Adaptive control for resonant tank component variations as well as varying line and load conditions is inherent in the chip due to its zero crossing detect circuitry. A unique one pin approach to soft start, restart delay, and system reference provides adjustable restart delay to soft start time ratios as well as closed loop control during soft starts. Relative ease of application to three previously reported converters was discussed.

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3) Jovanovic, Tabisz, Lee, Zero-Voltage-Switching Technique in High-Frequency Off-Line Converters, pp. 23-32, Sixth Annual VPEC Power Electronics Seminar Proceedings, 1988

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9

INTEGRATED CIRCUITS
UNITRODE
APPLICATION NOTE

U-127

UNIQUE CHIP PAIR SIMPLIFIES ISOLATED HIGH SIDE SWITCH DRIVE

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Abstract

High voltage, high current N-channel MOSFETs, now widely accepted in the industry, have found their way into numerous high power designs. As their cost to performance ratio continually improves, gate drive circuitry becomes a more significant factor in overall switch cost. This is most notable in "high-side" switching applications where an isolated gate drive is required. A new integrated circuit pair, the UC3724/UC3725, will be presented which implements a simple, isolated MOSFET gate drive circuit. To achieve a cost effective high side switch drive, UNITRODE has developed a unique modulation technique which transmits both signal and power across a small pulse transformer. This publication supercedes Unitrode Application Note U-124, originally written by C.S.Silva.

INTRODUCTION

Designers of power drives for PWM motor controls and switching power supplies often face the problem of driving the high-side MOSFET transistor in a high voltage power stage. In many applications, for example, bridge and three phase configurations, there are several of these switch drives to implement, and the level of complexity can be discouraging. From a cost standpoint, it is advantageous to utilize N- channel MOSFET devices in comparison to their more expensive - yet easier to drive P- channel counterparts. However, these high-side switch gate drive circuits can quickly become extravagant, and frequently result in complicated or unreliable schemes.

Probably the most common technique used in high-side drive circuits is to generate an isolated, or "floating" auxiliary supply voltage. Referenced to the high-side MOSFET's source, this supply powers a conventional gate drive circuit. The average auxiliary power consumed is generally well below one watt, and varies with switching frequency, FET size and number of paralleled FETs used to configure "one" switch. A typical circuit using this method is shown in figure 1.

With the realization that average MOSFET gate drive power is quite small, charge pump circuits are frequently used to implement the floating supply. In these designs, the storage capacitor can become large in an attempt to minimize the supply's ripple voltage and may impair the useable range of frequencies and duty cycles. Due to this constraint, the switch on-time must be limited by the control circuit, and preferably, undervoltage lockout incorporated in the driver circuit to assure reliable operation.

A simple alternative to this discrete approach can be obtained by using a high voltage IC - provided that the maximum switch voltage and on-time are within it's capability. There is, however, a cost penalty for this single chip solution. While the basic gate drive and protection circuitry have a low voltage requirement, the level shifting transistors necessitate a high voltage IC process - an option which is inherently expensive. Additionally, many motor drive circuits cannot tolerate an on-time limitation, and require an auxiliary power supply for continuous (DC) operation.

Typically, an opto-coupler is used to translate the switch activation command from the ground referenced, or "low-side" control circuitry up to the high-side driver. Unfortunately, this technique comes with its own set of reliability issues which includes low common mode transient immunity, and performance degradation over time and temperature. High voltage MOSFET circuit slew rates can easily exceed 20 kV/us causing opto-coupler self turn-on or turn-off. The opto-coupler's AC common mode rejection must be carefully evaluated, as this specification is usually influenced by common mode voltage as well as dv/dt. Power up and power down sequences also present potential failure without undervoltage lockout circuitry.

TYPICAL HIGH SIDE DRIVER APPLICATION

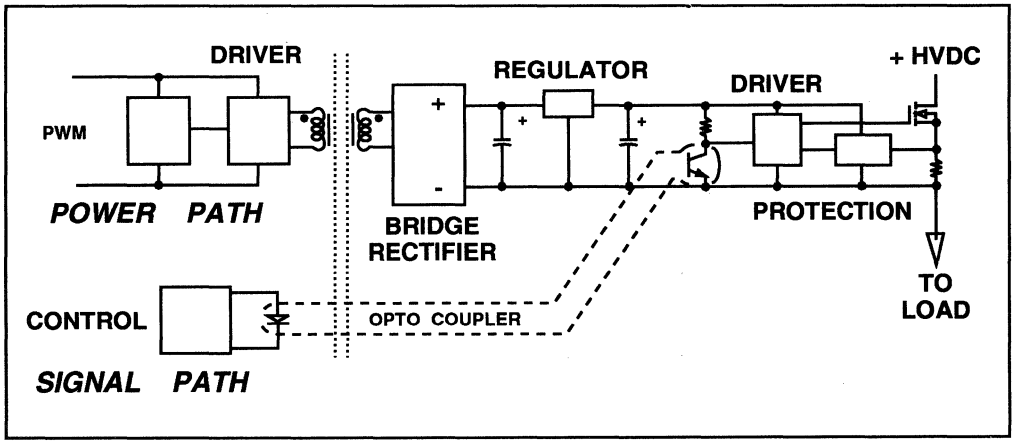

Figure 1.

UC3724 / UC3725 DRIVER PAIR - BASIC CIRCUIT

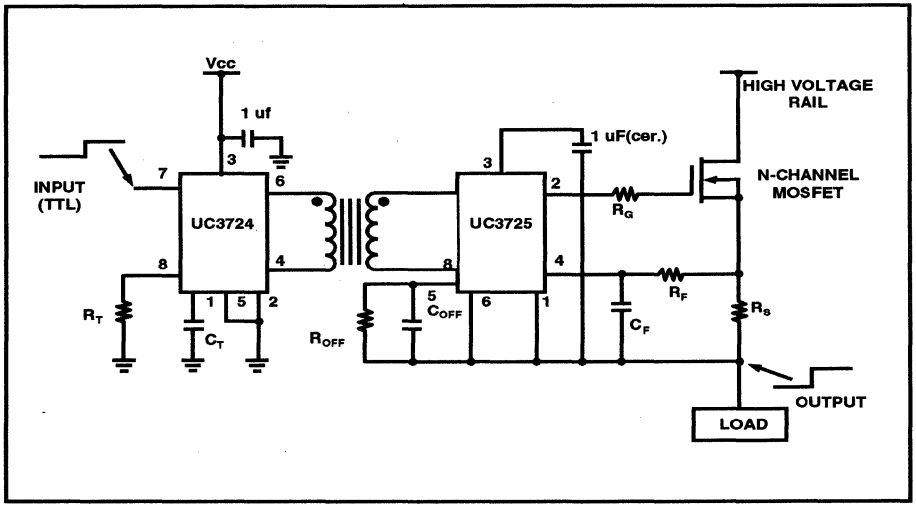

Figure 2.

UC3724/UC3725 DRIVER PAIR

The Unitrode UC3724/UC3725 IC pair offers a compact, and comparatively inexpensive design solution to the problem of supplying both isolated power and command signals. Figure 2 shows the basic circuit implementation. The two ICs, a pulse transformer, and a few passive components form a complete isolated MOSFET driver. A unique modulation technique simultaneously transmits power and command information across the transformer.

Provided the operational voltage is low, integrated circuit technology allows sophisticated circuits to be implemented at low cost. Transformers can easily provide several thousand volts of isolation, while supplying both power and signal. By exploiting each device's strengths, a low cost, high performance solution is achieved.

The UC3724 transmitter IC generates the carrier signal, with one of two possible duty cycles as commanded by the TTL level input. A unique carrier oscillator design not only sets the operating frequency, but also prevents the transformer from saturating, by assuring that the transformer magnetizing current is zero before initiating a subsequent oscillator cycle. Average transformer voltage is always zero, even under the transient conditions caused by input command changes. Saturation of the transformer core is virtually impossible using this technique.

To minimize transformer size and cost, a high frequency carrier is used. Although the carrier frequency limits the maximum transmitted switching frequency, it has no effect on input to output delay, which is solely determined by circuit propagation time.

The UC3725 driver IC rectifies the transformer isolated carrier to power the driver circuitry. Additionally, comparator circuitry determines the input command by sensing which duty cycle is transmitted, driving the MOSFET gate accordingly with the high current output stage. A comparator with programmable off time circuitry implements local over-current protection, while an enable input provides additional control and protection flexibility.

UC3724 ISOLATED DRIVE TRANSMITTER - BLOCK DIAGRAM

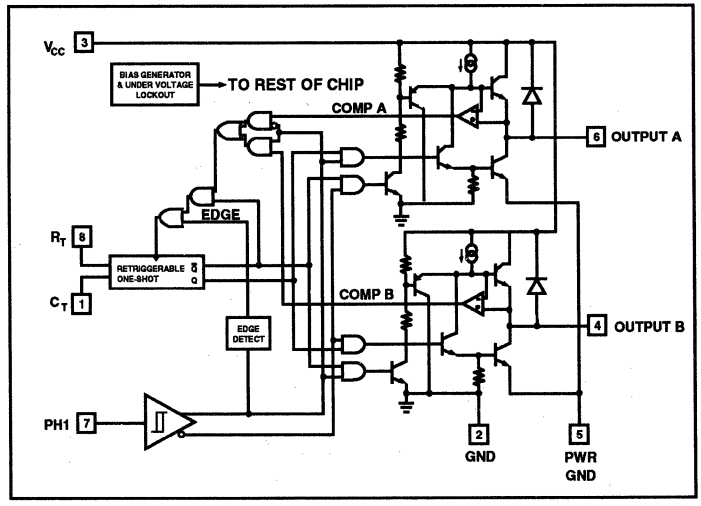

Figure 3.

UC3724 DRIVE TRANSMITTER

The UC3724 block diagram is shown in figure 3. The circuit consists of a bias voltage generator with under voltage lockout, control logic, a retriggerable one-shot, a TTL compatible input with hysteresis, two tri-level output drivers, and two zero current sense comparators.

The under voltage lockout inhibits the output drivers when the input supply voltage is below 9 volts. Once adequate supply voltage is present,

the bias generator supplies the appropriate internal voltages and currents, allowing the outputs to be enabled. This assures correct operation at power-up and power-down.

The carrier oscillator uses both a one-shot pulse width and the transformer core reset time to set the overall period. The one shot pulse width (T_{PW}) equals one-third of the nominal carrier period, and is set by timing resistor (R_T) and capacitor (C_T).

1) $T_{PW} = 0.51 \bullet R_T \bullet C_T + 150ns$ (sec)

"Full" supply voltage is applied to the transformer primary during this time by driving one output high and the other low. Transformer magnetizing current rises linearly at a rate determined by the primary inductance and applied voltage.

2) $di/dt = \dfrac{V_A - V_B}{L_{pri}}$ (*amps* / sec)

When the one-shot pulse ends, the low output switches high, and the high output switches to approximately one-half of the supply voltage. This applies "half" supply voltage to the primary, effectively in a reverse polarity to that of it's previous state. Internal offset circuitry compensates for output conduction voltage drops and maintains the full/half voltage ratio over temperature and supply voltage variations.

Power is transferred to the secondary circuit only while full voltage is applied to the primary. During this period the primary current is a composite of load and magnetizing current. The load current is interrupted when the half voltage is applied, so the residual primary current flowing is the magnetizing current.

With half voltage applied, the magnetizing current falls at one-half of the rate at which it had increased. An interval twice the programmed one-shot period is therefore necessary to reset the cores magnetizing current to zero and prevent any possibility of core saturation. The UC3724 incorporates a zero current detection circuit which guarantees that the magnetizing current has reached zero before initiating another oscillator cycle.

UC3724 OPERATIONAL WAVEFORMS (STEADY STATE)

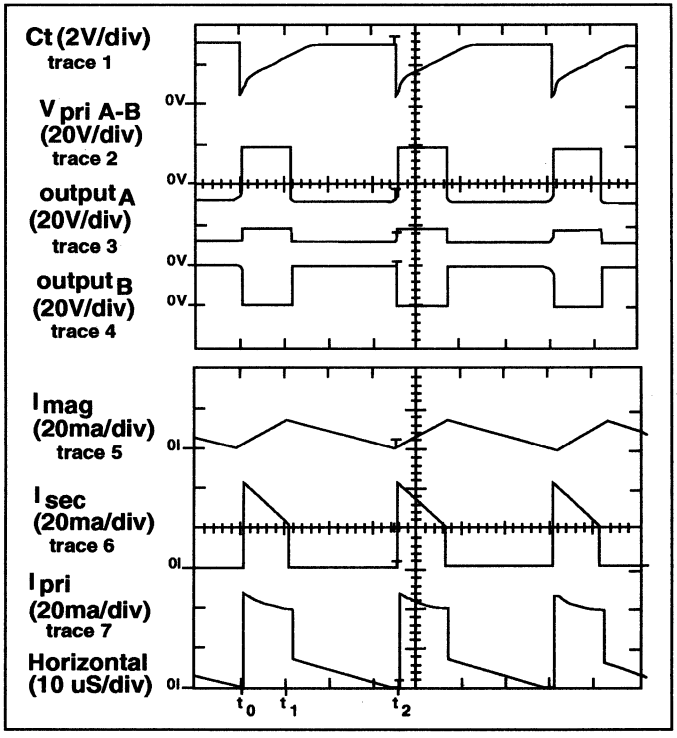

Figure 4.

Steady-state (continuous logic low input command) waveforms are shown in figure 4. The first trace shows timing capacitor (C_T) voltage, which is charged by a current set by the timing resistor (R_T). At time t_0, the one-shot is triggered, discharging the timing capacitor. Output$_A$ (trace 3) switches high, and output$_B$ (trace 4) switches low, with the resulting differential voltage V_{priA-B} (trace 2) applied across the transformer primary. The transformer magnetizing current (trace 5) increases linearly at a rate described by equation 2.

At time t_1, the timing capacitor voltage reaches the 2.5 volt threshold, ending the one-shot period. Output$_A$ is switched to $(V_{CC}/2) + V_{offset}$, and output$_B$ is switched high, allowing it's catch diode to conduct. The primary voltage (V_{priA-B}), is inverted, and reduced in half, causing the magnetizing current to fall at half the rate at which it had increased.

Output$_A$'s current sense comparator senses that the magnetizing current has reached zero at t_2, triggering the one-shot, thus initiating another oscillator cycle. If a continuous high is commanded, the waveforms for output$_A$ and output$_B$ are interchanged, and the magnetizing current is inverted.

At an input command transition, the existing oscillator cycle is terminated, the A and B outputs are reversed, and a new oscillator cycle is initiated. This applies full voltage of the appropriate polarity across the transformer primary for detection by the UC3725. Although the oscillator cycle has been terminated without allowing the core to reset, there is no danger of saturation. By reversing the outputs, the magnetizing current must first cross through zero before rising in the opposite polarity. The peak magnetizing current is actually less than a normal cycle, reducing the fall time, and hence the oscillator period.

UC3725 ISOLATED SIDE MOSFET DRIVER BLOCK DIAGRAM

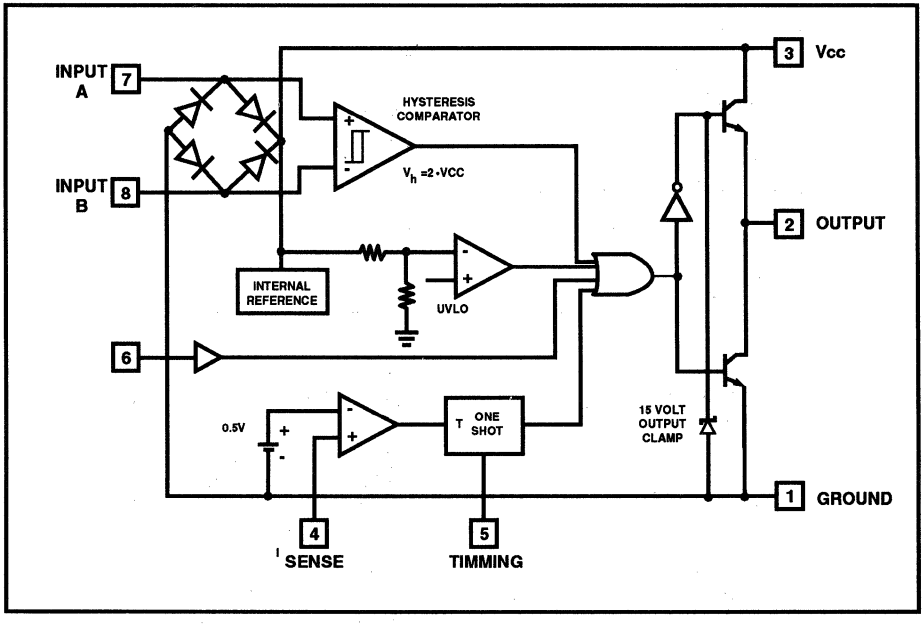

Figure 5.

UC3725 ISOLATED MOSFET DRIVER

The block diagram for the UC3725 is shown in figure 5. The circuit consists of a Schottky bridge rectifier, an internal reference with under voltage lock out, a differential hysteresis comparator, a high current totem-pole driver, a current sense comparator with programmable off time one-shot, and an enable input.

The Schottky bridge rectifies the isolated secondary voltage, providing power for the IC. A small capacitor, typically a 1uf ceramic, provides filtering and bulk storage to supply the high peak currents required to rapidly charge the MOSFET gate.

The undervoltage lockout inhibits the output driver when the supply voltage is below 12 volts. This assures that sufficient voltage is available to drive the MOSFET gate, preventing possible destructive linear operation.

The output driver is capable of delivering nearly two amps peak, which is more than adequate for most applications. The UC3725 features a self biasing drive arrangement which actively sinks gate current during under voltage lockout, preventing MOSFET self turn on. No additional gate to source resistor is required. The output voltage is clamped to 15 volts, which along with under voltage lockout, virtually eliminates the possibility of incorrect gate drive voltages

Over-current protection is provided by monitoring the voltage across a source resistor. The current sense comparator triggers a one-shot, which turns off the MOSFET, when the voltage exceeds 0.5 volts. At power-up, C_{off} is charged to 7 volts. When an over-current is detected, the output is latched off, and the 7 volt source is disabled allowing R_{off} to discharge C_{off}. When C_{off} discharges to 2 volts, the output is enabled and C_{off} is charged back to 7 volts. Off time is typically selected to maintain safe MOSFET junction temperature with a continuous fault load, and is programmed by timing resistor (R_{off}) and capacitor (C_{off}) with the following equation.

3) $T_{off} = 1.28 \bullet R_{off} \bullet C_{off}$ (seconds)

An enable input allows direct output control for specialized applications. It can be used with level shifting transistors, optocouplers, or other source referenced circuitry such as a UC3730 thermal monitor circuit for MOSFET over-temperature protection.

The input command, transmitted by the UC3724, is demodulated using a differential hysteresis comparator. The comparator senses whether the "full voltage" applied to the transformer is positive or negative, corresponding to an "off" or "on" input command. The bridge rectifier causes the peak secondary voltage to always be two diode drops above V_{CC} while the comparator hysteresis is internally set to twice V_{CC}. The MOSFET is turned on when the secondary voltage is more negative than $-(V_{CC})$, and turned off when more positive than V_{CC}. Note that there is a logic inversion between the hysteresis comparator and the gate driver.

Referring to steady-state waveforms (figure 4), the secondary current (trace 6) charges the supply capacitor during the full voltage output segment of the oscillator cycle (time t_0 thru t_1). During the half voltage output segment (time t_1 thru t_2), no secondary current flows, thus only magnetizing current is present in the primary current (trace 7), allowing proper oscillator operation.

For this example, a 30% duty cycle input command was arbitrarily selected, and the associated waveforms are shown in figure 6. At time t_0, the input command (trace 1) transitions from low to high, immediately switching $output_A$ low, $output_B$ high, and retriggering the one-shot. The differential hysteresis comparator switches low, driving the output (trace 4) high, when the transformer secondary voltage ($V_{sec\ A\text{-}B}$, trace 3), is more negative than $-(V_{CC})$. The primary current (trace 2) is inverted from the $output_A$ and $output_B$ reversal, but power delivery to the IC is unaffected due to the bridge rectifier input.

The input command transitions low at time t_1, switching $output_A$ high, $output_B$ low, and retriggering the one-shot. The hysteresis comparator switches high, driving the output low, when the secondary voltage exceeds V_{CC}. Note the reduced magnetizing current fall time, and associated oscillator period reduction, after input command transitions.

9

OPERATIONAL WAVEFORMS AT 30% DUTY CYCLE

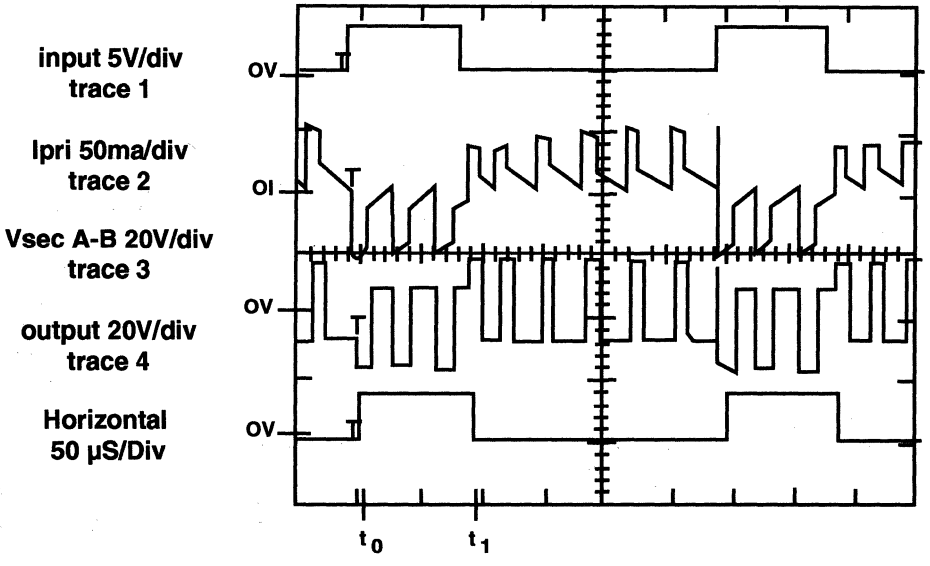

Figure 6.

PRACTICAL CONSIDERATIONS

The selection of carrier frequency (or more appropriately one-shot period since carrier frequency varies at switching transitions), is influenced more by transformer design than performance objectives. The minimum switching command period should be limited to four times the one-shot pulse width, to assure that adequate time is available to reset the core. Note that this limits the maximum switching frequency - but not the duty cycle range which is always 0 to 100%.

Waveforms for a command period approximately four times the one shot pulse width are shown in figure 7. The carrier oscillator has sufficient time to reset the transformer core and prevent saturation.

The one-shot period has no effect on input to output propagation delay, since the leading edge provides the output command information. Turn-on and turn-off propagation delay waveforms are shown in figure 8.

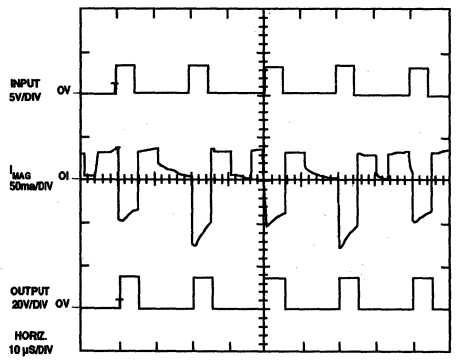

Figure 7.

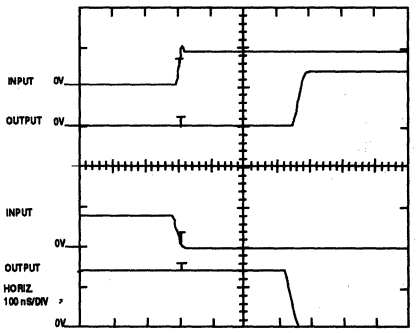

Figure 8.

The maximum carrier frequency is limited to 600 Khz. Most circuits will operate between 200 and 600 Khz., allowing switching frequencies up to 450 Khz., and a simple low cost transformer design. Nominal carrier frequency is calculated using equation 4.

$$4)\ F_c = \frac{1}{3 \bullet T_{PW}} \quad (Hz)$$

where T_{PW} = one-shot pulse width from equation 1.

Power supply voltage directly affects dissipation in the transmitter IC. Typical supply current verses voltage for the UC3724 is shown in figure 9. In most applications, bias power loss is about half of the total power dissipation.

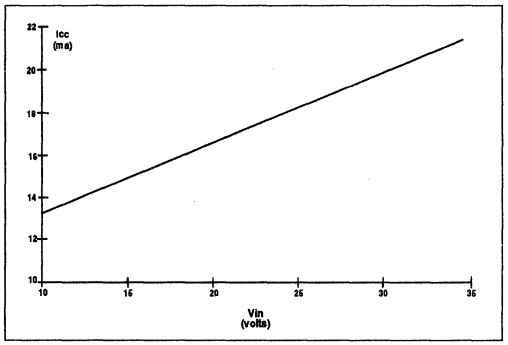

Figure 9.

The UC3725 driver IC provides sufficient gate voltage with a 15 volt supply. Any further increase, although safe since the output is clamped to 15 volts, causes additional bias power dissipation. By adjusting the transformer turns ratio, a 15 to 18 volt secondary supply can be generated with any primary voltage, allowing maximum efficiency .

Magnetizing current also contributes towards increasing dissipation with supply voltage. Although the UC3724 outputs can handle several hundred milliamps of load current with the output transistors in saturation, nearly one-half V_{CC} is across the upper transistors during the magnetizing current fall time. Dissipation during this period usually limits the peak magnetizing current, although catch diode current (which only conducts falling magnetizing current) is limited to 50 mA peak. When the peak magnetizing current falls below 10 ma, the required primary inductance becomes excessive, resulting in a large number of turns or larger core size. Therefore, the optimal range of peak magnetizing current is between 10 and 40 mA.

In many applications, the average gate charge current delivered by the driver is insignificant in relation to the UC3725 bias current. When larger MOSFETs, particularly large parallel assemblies, are driven at higher frequencies, the average gate charge current will have a considerable effect on the total transformer load. Average gate charge current is the product of gate charge (Qg), which is specified by the MOSFET manufacturer, and the switching frequency.

$$5)\ I_g\,(avg.) = Q_g \bullet F_s \quad (amps)$$

where Q_g = gate charge
F_s = switching frequency

All of the charge delivered to the gate at turn-on must be removed at turn-off. The resultant average power dissipated by the driver and gate resistor is described by equation 6.

$$6)\ P_g = Q_g \bullet V_g \bullet F_s \quad (Watts)$$

where V_g = fully charged gate voltage

The over-current input on the UC3725 has a typical delay time of 150 ns. Most applications require a small RC filter to attenuate leading edge current spikes caused by parasitic capacitance and catch rectifier reverse recovery. Careful attention to layout and component selection is necessary to prevent false triggering. The current sense resistor should be non-inductive to minimize spiking and ringing. The filter capacitor should be located as close to the IC as possible, with direct connections to the comparator input and common. The connection between the UC3725 common, and the MOSFET source resistor, must have relatively low impedance to prevent gate drive current from affecting current sense accuracy. In addition this should be a "Kelvin" connection, such that no load current flows through it. If the current sense feature is not required, the comparator input is simply connected to common, and the timing input is allowed to float.

DESIGN PROCEDURE

Typically, the application dictates the MOSFET(s), switching frequency, and switch isolation voltage. For cost considerations, a supply voltage common with other circuitry, is usually chosen to power the UC3724. The designer is then left with the carrier frequency and peak magnetizing current to select. A high carrier frequency is normally used to minimize transformer size and cost. Magnetizing current is initially set to a nominal value, such as 20 ma, and then adjusted if necessary to optimize the transformer design.

The one-shot pulse width is set to 1/3 the carrier frequency using equation 1. By rearranging equation 2, and allowing 2 volts for saturation, the transformer primary inductance can be calculated.

$$7)\ L_{pri} = \frac{(V_{cc}-2)\bullet T_{pw}}{I} \quad \text{(Henries)}$$

where V_{CC} = supply voltage
T_{PW} = one-shot pulse width
I_{mag} = peak transformer magnetizing current

Transformer core selection is an iterative process based on the following two equations.

$$8)\ \Delta B = \frac{V_{applied}\bullet T_{on}\bullet 10^4}{N_{turns}\bullet A_c} \quad \text{(Tesla)}$$

$$9)\ N_{turns} = \sqrt{\frac{L_{pri}\bullet 10^9}{A_L}} \quad \text{(turns)}$$

A toroid is usually the most cost effective core geometry for this application. The core material should be chosen for low losses and high permeability at the design frequency to minimize transformer size and number of turns. Thermal resistance and loss factors provided by the manufacturer are used to select the optimum core size. A flux density of .05 Tesla (500 Gauss) will cause approximately a 20 degree C rise at 500 KHz with common power materials such as Ferroxcube 3C8.

Typically most toroids used for this application have an AL between 1000 and 3000 mH/1000 turns. An estimated number of turns is calculated using an average A_L value of 2000 mH/1000 turns in equation 8. By rearranging equation 7, an approximate core are is calculated using a flux density of .05 Tesla, and the estimated number of turns. This leads to a first core selection, and an actual A_L value, which is used in equation 8 to calculate N_{turns}. The flux density is then checked using equation 7, and a larger or smaller core is selected if necessary.

The turns ratio is calculated using the following equation, which allows 2 volts for UC3724 output saturation, and 3 volts for UC3725 rectifier drop and output saturation.

$$10)\ \text{Turns ratio} = \frac{V_{cc}-2}{V_{gate}+3}$$

The power supplied by the transformer is the sum of the UC3725 bias loss and the average gate charge power. For minimum wire size, the resulting RMS winding currents can be calculated, although typically there sufficient space to use 24 to 28 AWG wire for ease of handling.

High voltage isolation is implemented by sleaving the primary winding with an insulation suitable for the required breakdown voltage. For low leakage inductance, bifilar windings are used, with additional turns added to the primary or secondary for non 1:1 turns ratios.

DESIGN EXAMPLE

The following design example is a general purpose isolated MOSFET gate driver. Up to 200 milliwatts is available for gate drive, which is suitable for most applications. A 15 volt power supply provides sufficient secondary voltage by using a step-up transformer.

Driver specifications :
* 200 milliwatts average gate drive power
* 100 KHz. switching rate
* 15 V supply voltage
* 1KV minimum isolation voltage

A 600KHz. carrier frequency is selected to minimize transformer size and cost. The one-shot pulse width is calculated by rearranging equation 4.

$$T_{pw} = \frac{1}{3 \bullet 600\ KHz}$$

$$= 556ns$$

Since the carrier frequency is near maximum, 2K will be used for R_T . C_T is calculated with equation 1.

$$C_T = \frac{(556\text{-}150)\ ns}{0.51 \bullet 2K}$$

$$= 398pf \text{ (use 390pf)}$$

30mA is selected for the peak magnetizing current. The corresponding primary inductance is calculated with equation 7.

$$L_{pri} = \frac{(15\text{-}2)\ V \bullet 556ns}{30\ mA}$$

$$= 241\mu H$$

The estimated number of turns are calculated using equation 9 with an average value of 2000 mH/1000 turns for A_L.

$$N_{turns} = \sqrt{\frac{241 \bullet 10^9}{2000}}$$

$$= 11 \text{ turns}$$

The approximate core area is calculated with equation 8, using a flux density of 0.05 Tesla.

$$A_c = \frac{13V \bullet 556ns \bullet 10^4}{11\ turns \bullet 0.05\ Tesla}$$

$$= 0.131\ cm^2$$

A one-half inch diameter toroid, Ferroxcube part number 204T250-3C8, is selected which has the following specifications.

$Ac = 0.148\ cm^2$
$A_L = 1620$ mH/1000 turns

N_{turns} is calculated using the actual A_L value in equation 9.

$$N_{turns} = \sqrt{\frac{241 \bullet 10^9}{1620}}$$

$$= 12.2 \text{ turns (use 12 turns)}$$

The flux density is checked using equation 8.

$$\Delta B = \frac{(15\text{-}2)\ V \bullet 556ns \bullet 10^4}{12\ turns \bullet 0.148\ cm^2}$$

$$= 0.041 \text{ Tesla}$$

The turns ratio is calculated using equation 10 for a gate voltage of 12 to 14 volts.

$$\text{Turns ratio} = \frac{(15\text{-}2)\ V}{(12\text{+}3)\ V}$$

$$= 0.867$$

Therefore N_{sec}= 14 turns

The transformer is wound with 26AWG magnet wire for ease of handling. A teflon insulation sleeve is slipped over the primary winding to improve the primary to secondary breakdown voltage. The primary and secondary are wound bifilar, to minimize leakage inductance, then the two remaining secondary turns are wound.

To verify operation, the test circuit shown in figure 10 was built. The over current, gate and bulk storage components are selected per MOSFET and load requirements. Figure 11 and 12 show turn-on and turn-off waveforms respectively.

The lower MOSFET in figure 10 was configured to test self turn-on of the upper driver during high transformer dv/dt. With 300 volts slewing at a rate in excess of 25 kv/us, no evidence of driver self turn-on was observed.

APPLICATIONS

Although the lower MOSFET driver is configured for faster switching than would normally be required, figure 10 is typical of half bridge outputs, where two or three of these circuits could implement a full or three phase bridge respectively. Full isolation for UL or VDE requirements can be met

by using isolated drivers for both upper and lower MOSFETs. This configuration can also greatly reduce noise in high current applications, by completely isolating the control circuitry from output devices.

TYPICAL HIGH SIDE DRIVE APPLICATION CIRCUIT SCHEMATIC

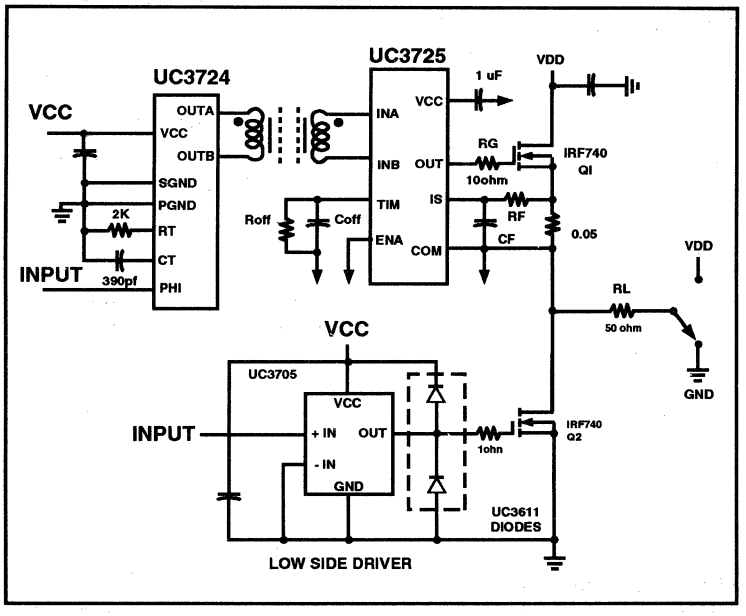

Figure 10

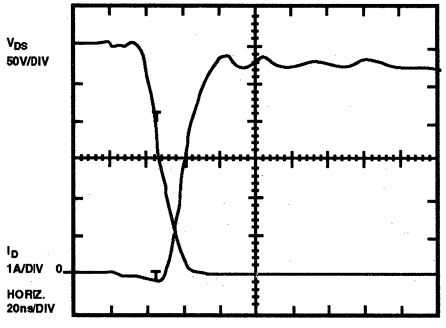

Figure 11

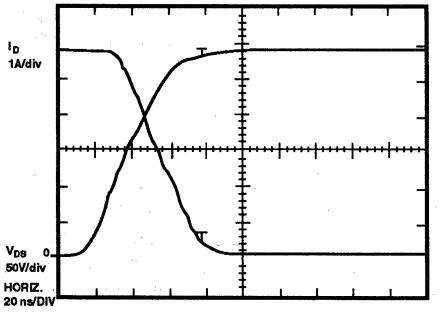

Figure 12

FULL BRIDGE OUTPUT

Some circuits have multiple MOSFETs driven from the same command, which are isolated from each other. A most notable example is the full bridge, which is commonly used in brush and stepper motor drives. Multiple secondaries can drive additional isolated UC3725 circuits, from a single UC3724, further reducing cost and complexity.

Figure 13 shows a fully isolated bridge circuit. By isolating all of the MOSFETs and the current sense signal, complete control to output isolation is achieved. Dual secondaries on each transformer eliminates the requirement for two additional transformers and UC3724s. For feedback and protection, a hall effect current sensor monitors load current directly, while providing high voltage isolation. The local over-current circuit in the upper FET drivers protects during load to ground shorts.

FULL BRIDGE OUTPUT CIRCUIT

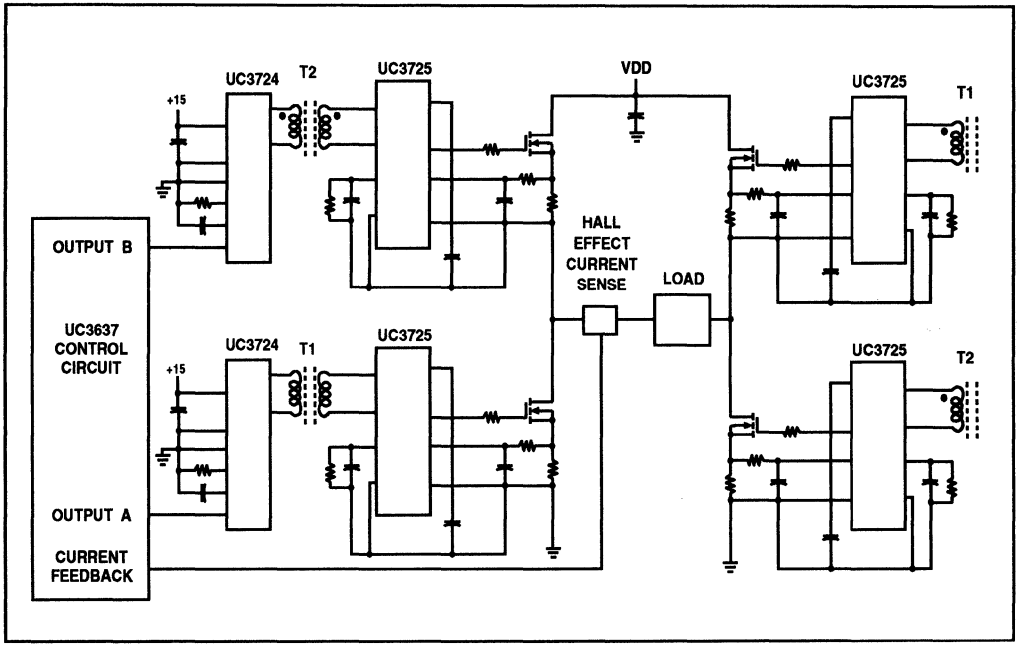

Figure 13

HALF BRIDGE OUTPUT CIRCUIT

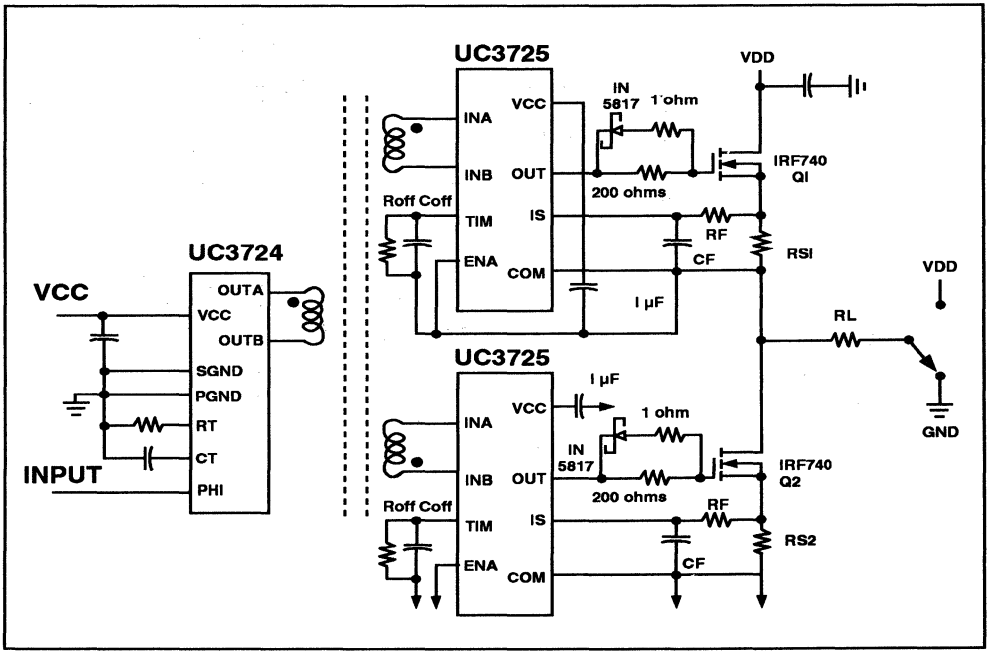

Figure 14

HALF BRIDGE OUTPUT

By reversing the polarity of one of the secondary windings on a dual secondary transformer, two FETs are switched out of phase from each other. A typical application for this arrangement is the half bridge, and is shown in figure 14. Dead-time between turn-off and turn-on is difficult to implement using this technique. To turn off both FETs, the UC3724 supply voltage must be removed, or the UC3725 enable inputs driven high. While shutting down the supply voltage is suitable for power-up/power-down protection, it is to slow to control dead-time. Isolating or level shifting the enable inputs adds complexity and negates the advantage of using a dual secondary transformer. Cross conduction is easily minimized however, by the gate resistor arrangement which provides rapid turn-off and slow turn-on. This technique is also typically used to minimize cross conduction caused by stored charge in the MOSFET body diode.

LEVEL SHIFT DRIVER

The UC3725 makes an excellent level shifted driver for lower voltage, non-isolated applications. All of the necessary protection features which are often omitted in discrete designs are incorporated in the UC3725, assuring reliable operation under all conditions. Figure 15 shows a typical level shift circuit with a "boot-strap" supply. The MPS-U10 level shift transistor has a maximum V_{ceo} of 300 volts, although it's dissipation without a heatsink limits the maximum supply to approximately 200 volts. Figure 16 shows input to output propagation delay while switching 150 volts and 3 amps. A 20 mA current source with a voltage compliance 15 volts above the supply rail can be used in place of the boot-strap circuit, for applications which cannot tolerate an on-time limitation. The cost effectiveness of this approach will depend on supply voltage and number of high-side MOSFETs.

LEVEL SHIFT CIRCUIT

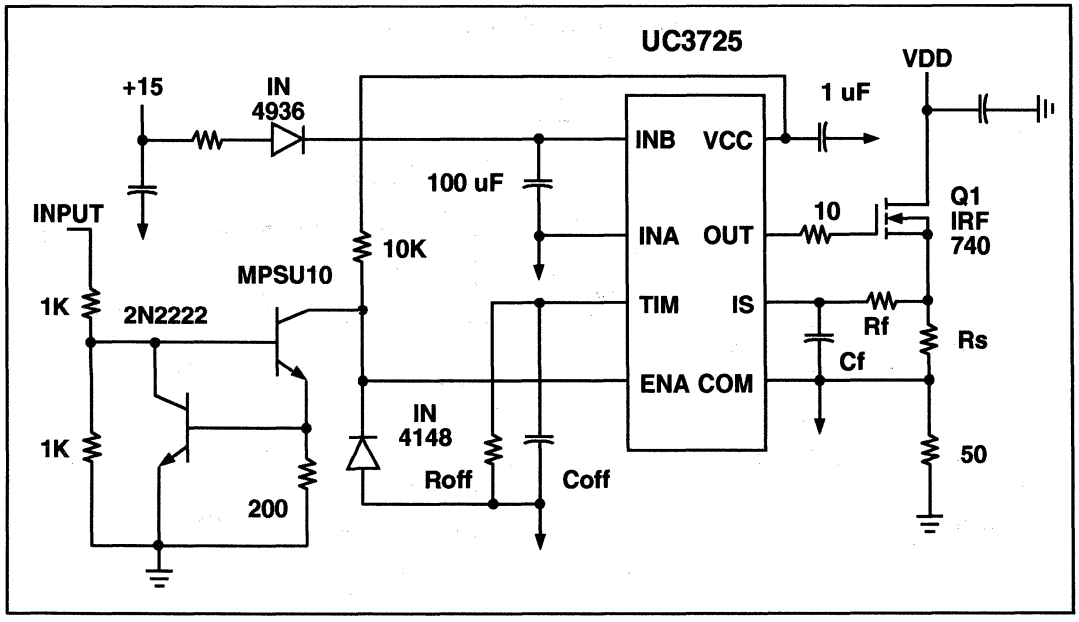

Figure 15

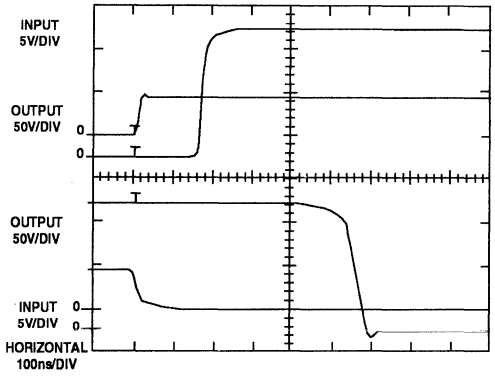

Figure 16.

LATCHED OVER-CURRENT FAULT

Current limiting is provided by the control circuit in many applications. Local protection from the UC3725 is therefore only required for fault conditions which result in high di/dt such as output shorts. It may be desirable to latch the output off under such a fault, rather than enable after a fixed off-time. Figure 17 shows a simple circuit used in place of the timing resistor and capacitor which will latch the output off after the over-current comparator is triggered. The 10uf capacitor resets the circuit at power-up by holding the timing input below the 2 volt one-shot threshold. When an over-current is sensed, the timing input voltage falls, and is clamped at 5.1 volts. The one-shot period normally ends when C_{off} is discharged below 2 volts, but by clamping the voltage, the time constant effectively appears infinite.

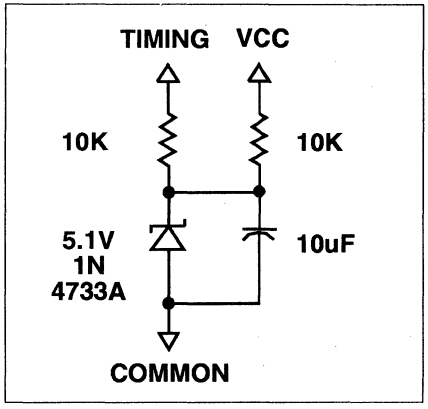

Figure 17

FAST AC SWITCH

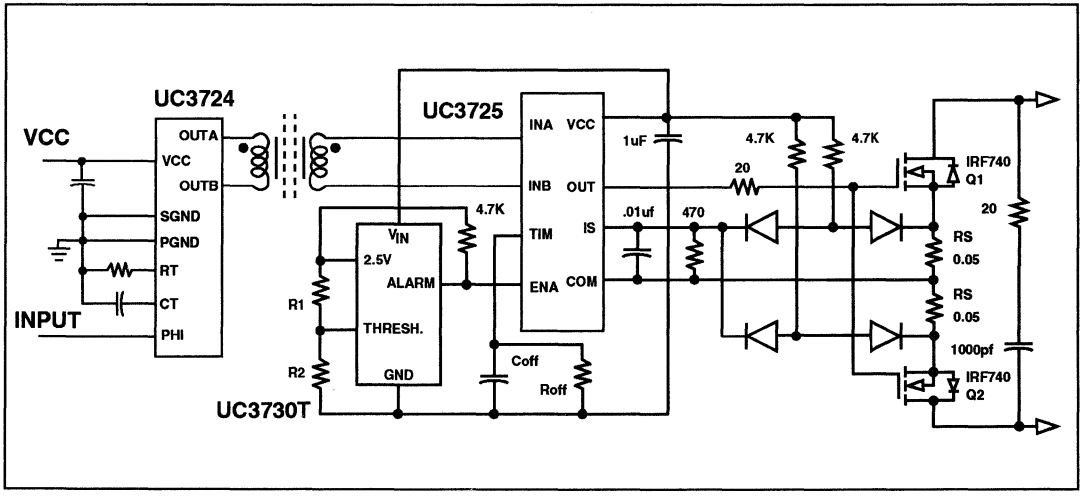

Figure 18

FAST AC SWITCH

Fully isolated gate drive lends itself to unique power switching circuits which are otherwise extremely difficult to implement. Figure 18 is a fast AC switch with over-current and over-temperature protection. The MOSFETs are selected to withstand the peak AC voltage, with each FET blocking in the opposite polarity. Figure 19 shows a 100 ohm load switched across 115 VAC, 60 Hz. The diode network allows current sensing in both directions, with the 4.7K resistors functioning as current sources. Protection against excessive MOSFET junction temperature is accomplished by mounting both FETs and the UC3730T on the same heatsink. MOSFET thermal resistance (junction to heatsink), and maximum FET dissipation must be considered when selecting the shut-down temperature set by R1 and R2. Refer to UC3730 data sheet for additional information. A 1000pf/20 ohm snubber is connected across the switch to reduce turn-off voltage spiking. The actual snubber values required are determined by load conditions.

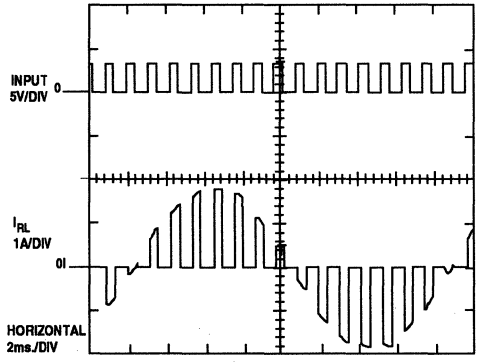

Figure 19.

SUMMARY

A unique integrated circuit pair, the UC3724/UC3725 has been presented that provides a simple, low cost, isolated MOSFET gate drive solution. Protection features prevent abnormal gate drive voltage, and provide over-current limiting. Duty cycle or on time limitations typical of other techniques are avoided, and by utilizing a transformer for isolation, there are no inherent isolation voltage limitations. The circuit is suitable for fully isolated systems which must meet UL or VDE requirements, as well as typical high-side switch applications.

REFERENCES

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2. W. Andreycak, "1.5 mHz CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY", UNITRODE APPLICATION NOTE # U-110

3. W Andreycak, " A NEW GENERATION OF HIGH PERFORMANCE MOSFET DRIVERS FEATURES HIGH CURRENT, HIGH SPEED OUTPUTS", UNITRODE APPLICATION NOTE # U-126

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APPLICATION NOTE

THE UC3823A,B AND UC3825A,B ENHANCED GENERATION OF PWM CONTROLLERS

BILL ANDREYCAK

ABSTRACT

This application note will highlight the enhancements incorporated in four new PWM control ICs, the UC3823A, UC3823B, UC3825A and UC3825B devices. Based upon the industry standard UC3823 and UC3825 controllers, this advanced generation features several key improvements in protection and performance over their predecessors. Newly developed techniques such as leading edge blanking of the current sense input and full cycle soft start protection following a fault have been incorporated into the design. Numerous enhancements to existing standard functions and features have also been made.

INTRODUCTION

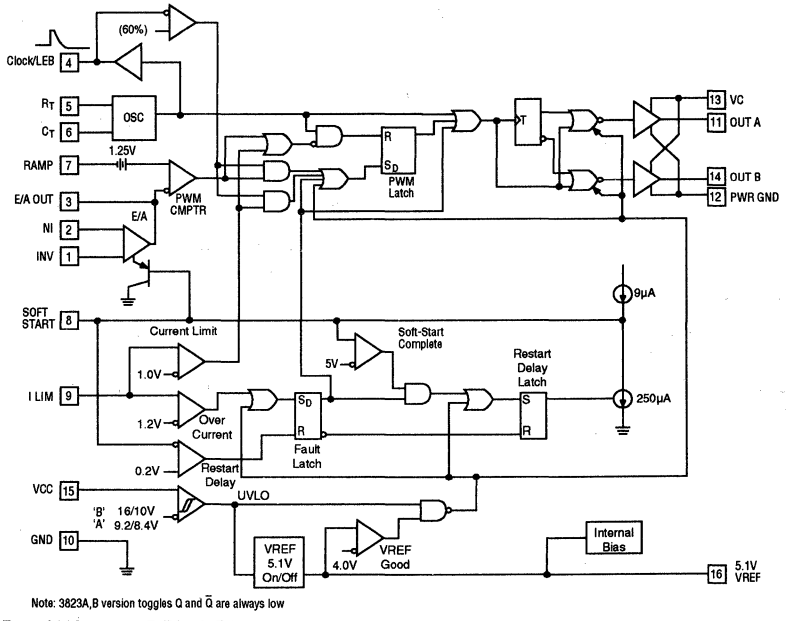
Higher degrees of integrated functions within PWM IC controllers are necessary to remain in pace with todays advancing power supply technology. Many external features, used almost universally by designers, have been built into this new generation of UC3823A,B and UC3825A,B PWM controllers. These control enhancements can be classified as either a performance or protection improvement, and an itemized description of each will be presented. The new features are:

PERFORMANCE IMPROVEMENTS

- Lower startup current
- Accurate oscillator frequency
- Leading Edge Blanking
- Higher current totempole outputs
- Higher G.B.W. Error Amplifier

PROTECTION ENHANCEMENTS

- Active Low outputs during UVLO
- Advanced undervoltage lockout
- Latched fault logic
- Full-cycle soft start
- Restart delay after fault



Note: 3823A,B version toggles Q and $\bar{Q}$ are always low

Figure 1 - UC3823A,B and UC3825A,B Block Diagram

UC3823A,B AND UC3825A,B FEATURES PREVIEW AND APPLICATIONS GUIDE

In most applications, the UC3823A and UC3825A devices are enhanced drop-in replacements for the UC3823 and UC3825 high speed PWMs. The "A" suffix versions (UC3823A and UC3825A) feature similar undervoltage lockout (UVLO) thresholds to the preceding generation which turn on at 9.2 volts and turn off at 8.4 volts. Off-line power supplies can benefit from the wider UVLO hysteresis of the "B" version devices (UC3823B and UC3825B) which turn on at 16 volts and off at 10 volts. This, in conjunction with the lower startup current of 100 microamps can streamline the IC's power supply and minimize startup circuitry power loss.

One significant difference will be found on the UC3823A and UC3823B controllers. Formerly, the UC3823 (non A or B version) provided access to the current limit comparator's threshold at pin 11. This could be accurately set by the user within the range of 1.0 to 1.25 volts with an external reference voltage. The UC3823A and UC3823B devices use pin 11 as a high current totempole output, identical to that found on pin 14. These outputs can be paralleled - effectively doubling the peak output current capability to 4 amps. No access to the previous current limit reference (I LIM REF) comparator is provided as this threshold is internally set to 1.0 volts with a +/- 5% accuracy over all operating conditions. Existing applications can incorporate the UC3823A or UC3823B devices by simply removing any of the former external biasing components to pin 11.

One other major difference to the prior generation of PWMs is the reduced maximum operating supply (Vcc) and collector supply (Vc) voltages of 22 volts versus 30 volts. This characteristic is a principal consideration when determining the IC power supply, as nearly all applications utilize a supply voltage between 10 and 15 volts. Typical supply current is higher; 28 mA versus the former 22 mA, however the maximum Icc is unchanged at 33 mA.

Since many of the enhancements in this new family of PWMs are executed using internal circuitry, most applications require no additional components externally to realize a performance or protection advantage. The list of improvements which includes latched fault protection and full cycle soft start should not require any PC board changes. The leading edge blanking feature, however, will require one capacitor from the CLOCK/LEB (pin4) to ground to facilitate programming.

The improved oscillator section can be optimally programmed for the correct frequency and maximum duty cycle combination. No changes to the timing component values of Rt and Ct are necessary. Additionally, high frequency current mode applications can benefit from the high gain bandwidth error amplifier (12 MHz). Unity gain bandwidth is also up from 5.5 MHz to 9 MHz. This should not require changes to the PC board layout unless the compensation circuit design relied upon the older 5.5 MHz UGBW for high frequency roll-off.

STARTUP FEATURES

Since a majority of PWM applications are off-line converters, a low startup current is desirable. This attribute minimizes the complexity and power loss of the startup power supply once normal operation is attained. Every milliamp of additional startup current drawn by the controller results in a power loss of approximately 385 milliwatts in a power factor corrected application. Heat, PC board real estate and additional cost are unnecessary extras which can be eliminated with a lower startup current controller.

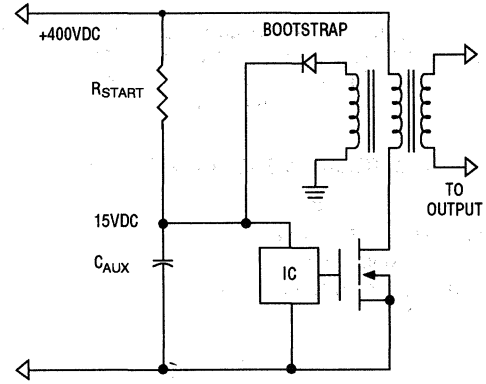


Figure 2 - Startup/Bootstrap Circuit

This new generation of UC3823A,B and UC3825A,B control ICs minimizes the startup current to 100uA typically. Once the IC crosses its undervoltage lockout threshold, the current drawn will increase to the typical running current.

In an off-line converter, two things are necessary to get the main converter up and running when the control IC turns on. First, the IC should contain wide undervoltage lockout hysteresis. Second, the bootstrap supply should come up and into regulation very quickly before the auxiliary capacitor voltage drops below the ICs lower (turn-off) undervoltage lockout threshold.

Undervoltage lockout thresholds are primarily determined by the allowable MOSFET gate voltage range. Operation with gate-to-source voltages above sixteen volts can cause overstress to the device, and voltages lower than about nine volts can cause linear FET operation. The "B" suffix designator (UC3823B and UC3825B) is used to define devices which exhibit typical undervoltage lockout thresholds of

16V (turn-on) and 10V (turn-off) for off-line applications. The "A" suffix parts (UC3823A and UC3825A) incorporate 9.2V (turn-on) and 8.4V (turn-off) thresholds for DC to DC converter applications, and are compatible with existing UC3823 and UC3825 (non A,B) UVLO thresholds.

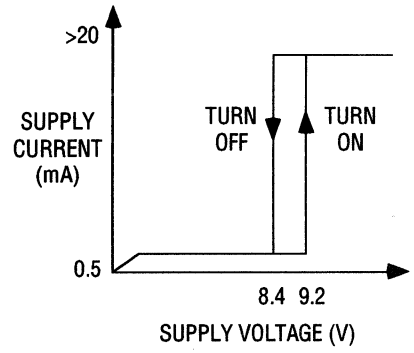


Figure 3 - 9.2/8.4V UVLO Thresholds-DC/DC Converters

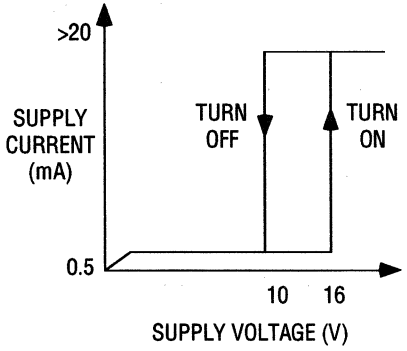


Figure 4 - 16/10V UVLO Thresholds-Off Line Power Supplies

SELF BIASING, ACTIVE LOW OUTPUTS DURING UV LOCKOUT

Another enhancement to the new UC3823A,B and UC3825A,B controllers is found in the output stages. During undervoltage lockout almost all internal functions of the control IC are disabled, primarily to obtain a low startup current. Generally, this would result in little or no available bias to actively keep the outputs low during this power-up condition, when it's needed the most. Outputs are in a high impedance state which is typically about 1 megohm. As the DC (bulk) high voltage rises, a capacitive divider is formed at the MOSFET switch between the drain-to- gate and the gate-to-source capacitances. A quickly rising bulk supply can couple a problematic gate drive command to any FET driven without a gate pull down circuit. Since the control IC is below its turn on threshold, the unbiased output drivers of older PWMs cannot prevent the switch from turning on under these circumstances.

One solution to prevent this parasitic turn-on during undervoltage lockout is to incorporate an active low, self biasing totem-pole design in the driver output. As shown in figure 5, a PNP drive transistor (Q2) is connected between the output pin of the IC and the lower NPN output transistor (Q3). As the output voltage rises, transistor Q1 is biased on through the 50K ohm resistance. This causes the base of Q2 to go low, turning Q2 on. The output pin supplies drive bias to the main totem-pole transistor, Q3, directly through the saturated PNP. Increasing voltage on the output pin provides more drive to transistors Q1, Q2 and Q3. The saturation voltage of this circuit at moderate currents (10mA) is well below the turn on thresholds of the power switching MOSFETs. This circuit is removed from operation once the undervoltage lockout requirements have been satisfied. Transistor Q4 is turned on with a valid UVLO which voids the possibility of transistor Q1 from ever turning on during normal operation. Additionally, a 250 microamp current source from Vcc keeps the PNP predriver (Q2) off after UVLO.

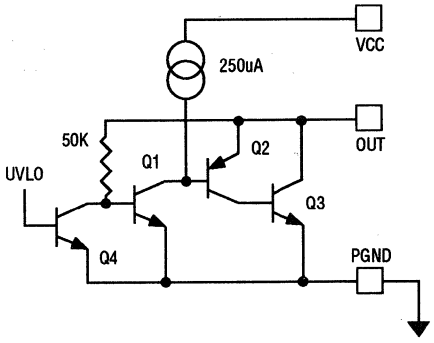


Figure 5 - UVLO Self Biasing Outputs

Another benefit of this technique is obtained during power down. As the IC crosses below its lower UVLO threshold, the self biasing circuitry is enabled. Any residual voltage on the output will similarly turn the totempole stage on which actively pulls the output low. This feature insures correct gate drive operation regardless of the turn off sequence.

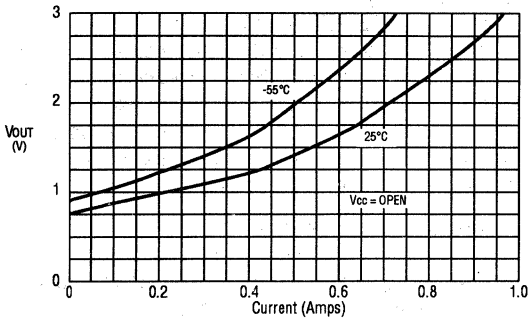


Figure 6 - Output V and I During UVLO

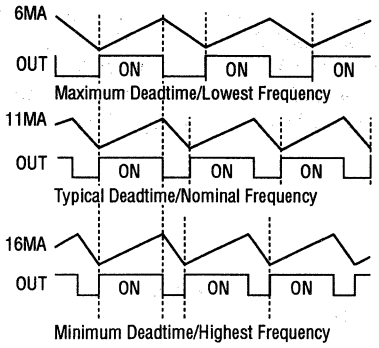


Figure 7 - Frequency and Deadtime Variations vs. Discharge Current Tolerances

OSCILLATOR ACCURACY

Fundamental to the design of any switchmode converter is maintaining an accurate switching frequency. The UC3823A/B and UC3825A/B ICs utilize two pins for the sawtooth oscillator; one each for the timing resistor (Rt) and timing capacitor (Ct). The resistor programs the charging current to the timing capacitor via an internal current mirror with high accuracy. Maximum switch on-time is determined by the rising capacitor voltage whereas deadtime, the programmed switch off time is determined by the timing capacitors discharge.

Considerable improvement has been made to the accuracy of the oscillator discharge current. The previous generation of UC3823/25 devices endured variations of plus or minus forty percent (+/- 40%) over the full military temperature range and production tolerances. This new generation of UC3823A/B and UC3825A/B PWM controllers features a well controlled oscillator discharge current which is "trimmed" at wafer probe testing to +/- 1 milliamp. Oscillator initial accuracy (400 KHz nominal) has been tightened to 375 KHz minimum and 425 KHz maximum. Total variation over all line and temperature ranges is limited to 350 and 450 KHz. A new specification for 1 MHz accuracy has been added, demonstrating a plus or minus fifteen percent total frequency variation at high frequency.

CLOCK OUTPUT

The UC3823A,B and UC3825A,B controllers also feature a TTL/CMOS compatible CLOCK output pin. Specified amplitudes are 3.7 volts in the high (off) state and 0.2 volts during its low state. Additionally, this pin is also used for programming of the leading edge blanking function. Notice that unlike their non A,B predecessors, these enhanced versions cannot be externally synchronized by an input to the clock pin. Synchronization is obtained by forcing a SYNC pulse across a resistor in series with the timing capacitor.

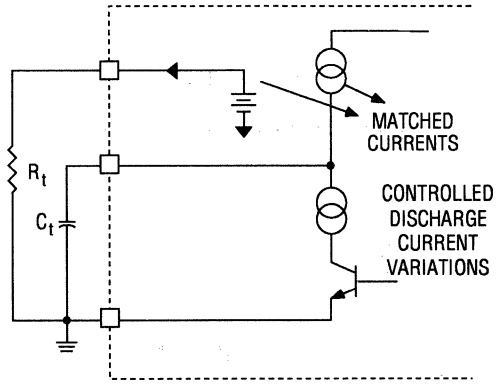


Figure 8 - Controlled Discharge Current

LEADING EDGE NOISE IN THE CURRENT SENSING CIRCUIT

One of the most difficult tasks with peak current mode control is sensing the inductor current. Instead, switch current is generally sensed by means of either a series resistor or current sense transformer. There is some difficulty with using this technique accurately, especially at light current levels. As the switch turns on, circuit parasitics in the power stage, output rectifier reverse recovery characteristics and high current gate drive pulses can create significant noise pulses on the leading edge of the current sense signal. Traditionally, this problem has been overcome by adding a small R-C noise filter between the current sense resistor and the PWM controllers current sense input. At low operating frequencies and high output current levels this R/C filtering technique will generally deliver satisfactory results. However, at higher switching frequencies, and almost always at lighter load currents the leading edge spike amplitude can greatly exceed the peak current sense signal.

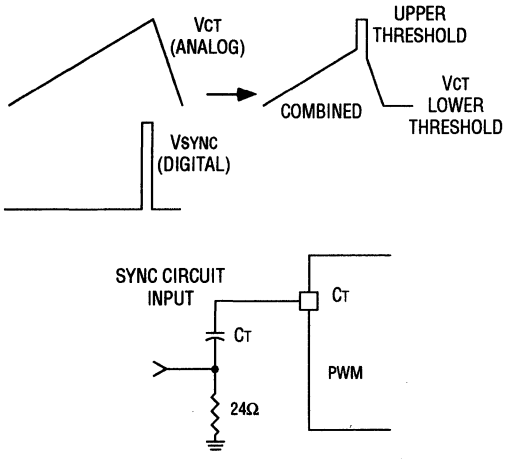


Figure 9 - Synchronization

The leading edge current sense noise shown in figure 10 will cause a premature, false triggering of the pulse width modulator. Additionally, this will lead to instability of the converter by causing the voltage loop to oscillate at light loads. When the PWM is triggered by the noise spike instead of the true current signal - a smaller (minimum) pulse width is delivered to the main switch. The power supply's output voltage subsequently falls which causes the voltage amplifier to command for a higher inductor (switch) current. Eventually this continues until the amplitude is sufficient to rise above the leading edge noise spike.

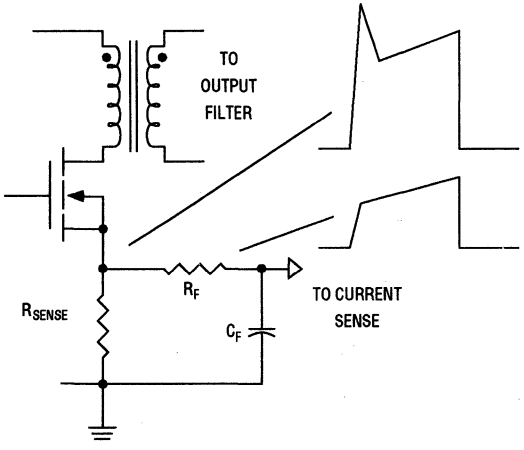


Figure 10 - Current Sensing Technique

Pulse widths too wide for proper operation are now delivered and the output voltage climbs until the voltage amplifier commands less current. This oscillatory process continues at a rate determined by several factors. Noteworthy is that this has nothing at all to do with the instability caused by inadequate slope compensation, or peak-to-average current error. The cause is leading edge noise, and even optimal loop compensation cannot protect against this problem.

LEADING EDGE BLANKING

The RC filter shown in figure 10 can be tailored to work well over a limited range of applications and power levels. Another technique, known as Leading Edge Blanking (LEB) essentially blindfolds (blanks) the PWM comparator for a specific amount of time during the beginning of the cycle. The blanking duration is user programmable and should correspond to the width of the leading edge noise spike. This eliminates the need for filtering of the current sense signal in peak current mode controlled circuits.

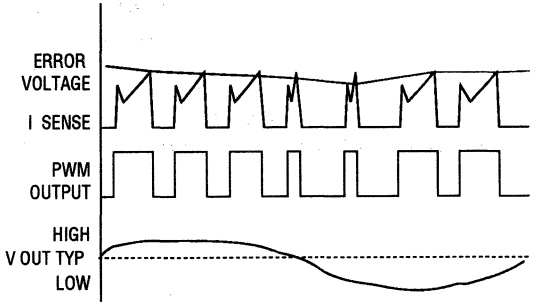


Figure 11 - Instability Caused By Leading Edge Noise Triggering

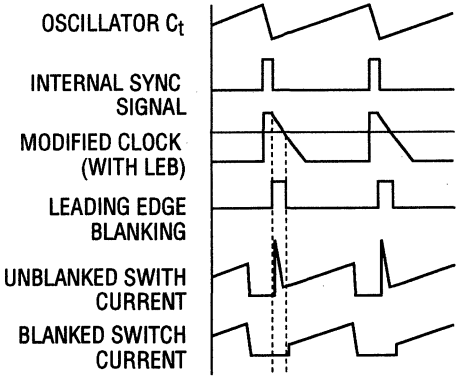


Figure 12 - Leading Edge Blanking Operational Waveforms

9

LEB IMPLEMENTATION

The focal point of any fixed frequency PWM controller is its clock. Used to accurately program the switching frequency and maximum duty cycle, the clock serves as the trigger source for the leading edge blanking circuitry. A digital representation of the timing capacitor charge/discharge status is developed by internal logic. This is made available at the PWMs CLOCK pin for external purposes. The UC3823A,B and UC3825A,B all use a high output to indicate the OFF period of the switching cycle, and a low to indicate the maximum ON time. These levels will be incorporated into the design of the leading edge blanking circuitry.

The clock output of the UC3823A,B and UC3825A,B is pulled high during the oscillator deadtime to approximately 4 volts. A capacitor added to the CLOCK output pin programs the leading edge blanking duration. An internal comparator with an accurate threshold set at 60% of the peak clock amplitude has been added. The LEB programming capacitor is discharged by an internal 10K ohm resistance to ground. The LEB interval is defined by the time required for the capacitance to discharge from 4 volts to the 60% threshold. Once the LEB capacitor discharges below this threshold, the PWM operates normally without any blanking. Programming should accommodate the worst case of leading edge noise. With no programming capacitor added, the ICs function similarly to their predecessors and provide no blanking.

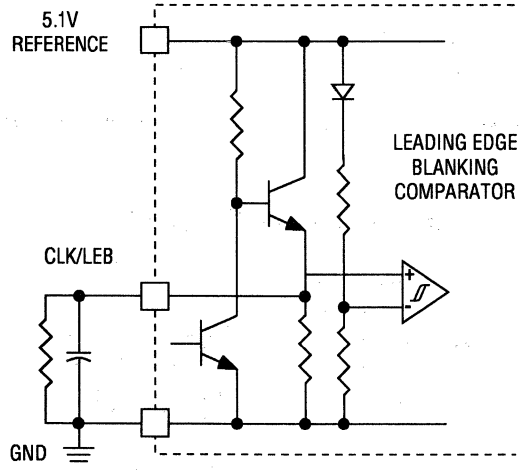


Figure 13 - LEB Circuitry

Because of the leading edge blanking, the PWM outputs will exhibit a minimum ON time in normal operation. The duration corresponds directly to that of the LEB programming, so a minimum duty cycle has also been established. Resolution between zero duty cycle and this minimum duty cycle cannot be obtained - which should also be taken into account when programming the LEB circuitry.

Zero duty cycle is a valid operating condition which can be achieved by one of two methods. The most obvious technique is to bias the error amplifier such that its output is driven below the PWM zero duty cycle threshold of 1.1V. The ICs error amplifier can easily accomplish this while sinking current up to 1 mA, worst case. The second technique utilizes the current limiting feature (ILIM) at pin 9. An ILIM input held above the 1.2V (typ) FAULT threshold will force the PWM's on-time and duty cycle to zero. More details of the interface between the PWM and fault circuitry will be found in the following fault protection section.

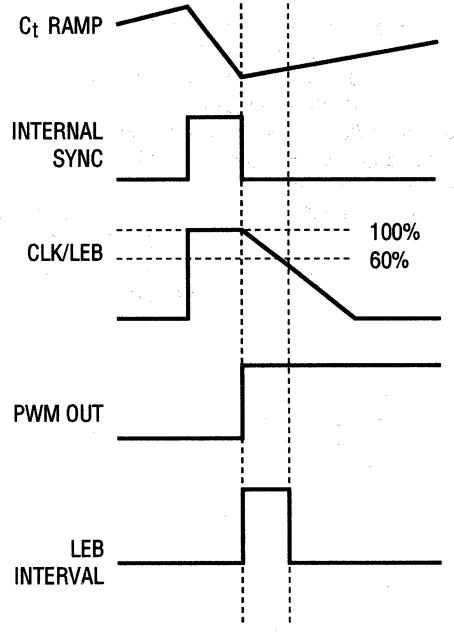


Figure 14 - Blanking Waveforms

LATCHED FAULT PROTECTION

While the previous generation of control ICs offered fault protection circuitry, they did not feature a fully latched shutdown after detecting a fault. The unlatched technique only

discharges the soft start capacitor during the duration of the fault - a duration which can be very brief with a high speed controller. As a result, the duty cycle is not significantly reduced, and the IC continues delivering output pulses at the the switching frequency. Typically, the switching components can easily be dangerously overstressed while also dissipating a significant amount of power.

The new UC3823A,B and UC3825A,B controllers feature a latched fault protection circuit as shown in figure 15. Two comparators are used to offer two stage protection - depending on the amplitude of the fault. The first comparator has a one volt threshold for cycle-by-cycle current limiting. In normal operation this terminates the immediate switch drive pulse but does not trigger the latching fault logic. One volt has been selected as the peak amplitude of the current sense signal for normal operation and slight overloads to accommodate transients.

The second comparator has a slightly higher threshold of 1.20 volts, indicative of a twenty percent overload or fault. When this comparator is tripped, the fault latch is turned on and the soft start capacitor begins discharging. The present output pulse had already been terminated by the one volt comparator circuity while the signal was rising to cross the 1.20 volt level. The over- current latch insures that the PWM latch is held off for an extended period of time, approximately equal to the soft start time constant.

Once this overcurrent latch is set, a second "restart" latch is triggered which insures the proper restart of the control logic. First, a current sink (typically 200 uA) is turned on by the restart latch output which overpowers the 9 uA charging current source and begins discharging the soft start capacitor. The capacitor voltage is monitored by a restart comparator, looking for a decay to the threshold level of 0.2 volts. Once this occurs, the restart comparator resets the overcurrent comparator which sequentially resets the restart latch.

The restart latch can only be set with the right set of conditions as shown in the block diagram. First, undervoltage lockout must be satisfied to insure proper operation during initial power-up. Secondly, the overcurrent (1.2 V) comparator must be triggered, indicative of a valid fault. Last, and most important, is that a full soft start cycle must be completed before the restart latch can be retriggered. A fourth comparator insures that the soft start capacitor voltage has charged to a 5 volt threshold. This indicates that a complete discharge followed by a complete charge has occurred.

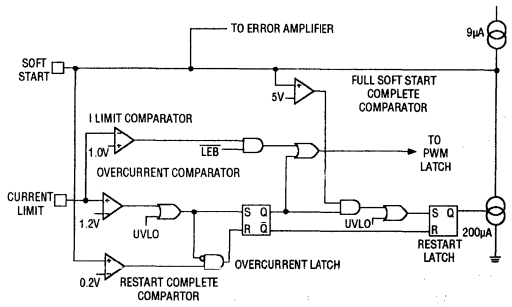


Figure 15 - Latched Fault And Full Cycle Soft Start Protection Circuitry

FULL CYCLE / CONTINUOUS FAULTS

During a fault, many designers prefer to reduce the repetition rate at which the switch is driven rather than to continue at the normal switching frequency. Often called "hiccup", this delayed restart will significantly reduce the overstress and power dissipated during abnormal conditions. Implementation of the latched fault technology results in significantly lower power dissipation during a continuous fault or shorted output stage. Instead of delivering minimum duty cycle pulses at the oscillator frequency, the retry sequence occurs at a repetition rate approximately equal to the soft start period with a continuous fault.

In the worst case, two PWM outputs can occur in a time less than the soft start time constant, but this happens only once with a "true" fault input (>1.2 V). For example, assume that the converter is in normal operation when a fault is detected. The first valid fault immediately turns off the output and triggers the latching overcurrent circuitry. Since the soft start capacitor was fully charged (above 5 volts), the "full soft start complete" comparator allows the overcurrent latch to set the restart latch. Discharge begins and continues until the restart complete comparator is tripped at a soft start capacitor voltage of 0.2 volts. The restart latch is reset, and the soft start capacitor begins charging.

Note that a well defined time is required between this instant and the time when the first output pulse can next occur. The capacitor begins at 0.2 volts and the error amplifier output is internally clamped to the soft start capacitor voltage. Back at the PWM comparator, however, there is a 1.25 volt offset on the ramp pin to facilitate zero duty cycle. Therefore, the soft start capacitor must charge from 0.2 volts to 1.25 volts before the PWM comparator is active.

This provides a slight interval between the worst case of successive output pulses into a shorted load. From this point on, the soft start capacitor must fully charge up to the five volt threshold of the "full soft start complete" comparator. Once in this mode, only one PWM output per soft start period can be obtained into a fault as shown in figure 16.

LEB AND FAULT DETECTION

The leading edge blanking circuitry is interfaced to also blank some of the fault detection circuitry. While numerous arrangements are possible, only one configuration offers a reasonable compromise between quick response and noise immunity. As demonstrated in figure 12, leading edge blanking does inhibit the one volt, cycle-by-cycle current limit comparator during the programmed interval. However, the blanking does not disable the 1.2 volt overcurrent comparator and fault logic. This adaptation will accommodate a moderate amount of leading edge noise without having to significantly filter the current sense, and fault signals. Even if a moderate amount of filtering is required, the latched full cycle shutdown protection minimizes the power dissipation.

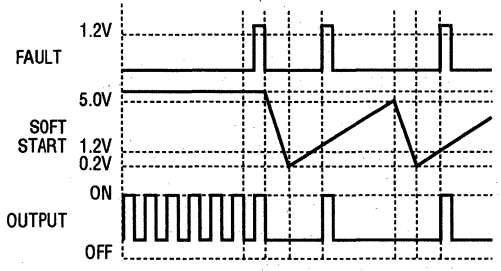


Figure 16 - Full Cycle Soft Start - Operational Waveforms

TIGHTER FAULT THRESHOLDS

This latest generation of IC controllers utilizes a thin film resistor process which provides improved control of the tolerance. These resistors are used to generate accurate voltage thresholds by dividing down the IC's reference voltage internally. Both of the current limiting comparator thresholds have been tightened in the "A" and "B" versions of controllers. The cycle-by-cycle current limit threshold range has been tightened to +/- 5% from its previous +/- 10% specification. The new limits are 0.95V minimum, 1.05V maximum with the center remaining at the previous 1.0 volts.

The overcurrent (fault) threshold, however, has been centered at 1.2 volts instead of the 1.4 volt midpoint of the non A,B versions. The new specifications are 1.14 volts minimum to 1.26 volts maximum. Applications converting to the newer controllers may need to adjust the current sense resistor value accordingly. Typical propagation delay is unchanged at 50 ns typical, and 80 ns maximum.

HIGHER GAIN-BANDWIDTH ERROR AMPLIFIER

Many of the critical UC3823/25 error amplifier specifications have been improved. The characteristics which significantly differ are: input offset voltage - reduced from 10 to 7 mV, unity gain bandwidth - increased from 5.5 MHz to 9 MHz, typical slew rate - reduced from 12 to 9 V/us. Notice that the minimum slew rate is unchanged at 6 V/us.

HIGH POWER OUTPUTS

The industry need for higher switching frequencies and improved efficiency has directly effected the design of the totem-pole output drivers. Many of the capacitive loads (MOSFETS) placed directly on the PWM outputs require high peak currents to obtain adequate switching transitions. The high speed UC3823A,B and UC3825A,B controllers feature peak current ratings of 2 amps, and are capable of slewing 15 volts in 35 nanoseconds into 1000pF. Separate collector supply (Vc) and power ground connections (PGND) help decouple the analog circuitry from the high power gate drive noise.

TYPICAL APPLICATION

The 1.5 MHz, 50 Watt push-pull converter detailed in Application Note U-110 was redesigned to accept the UC3825"B" device. The basic power stage remained similar while an emphasis was placed on control circuit improvements. These enhancements included Leading Edge Blanking of the current sense signal and Restart Delay following a fault. Also, a current sense transformer was installed which not only reduced losses but allowed amplification of the current sense signal to approximately 2.5 volts, thus enhancing noise immunity.

Improvements to the power section of the converter include the use of larger MOSFETS (IRF640's) and the addition of a bootstrap winding for the auxiliary bias supply. The startup resistor from the input supply was increased since the UC3825"B" device features a wide UVLO hysterisis of six volts.

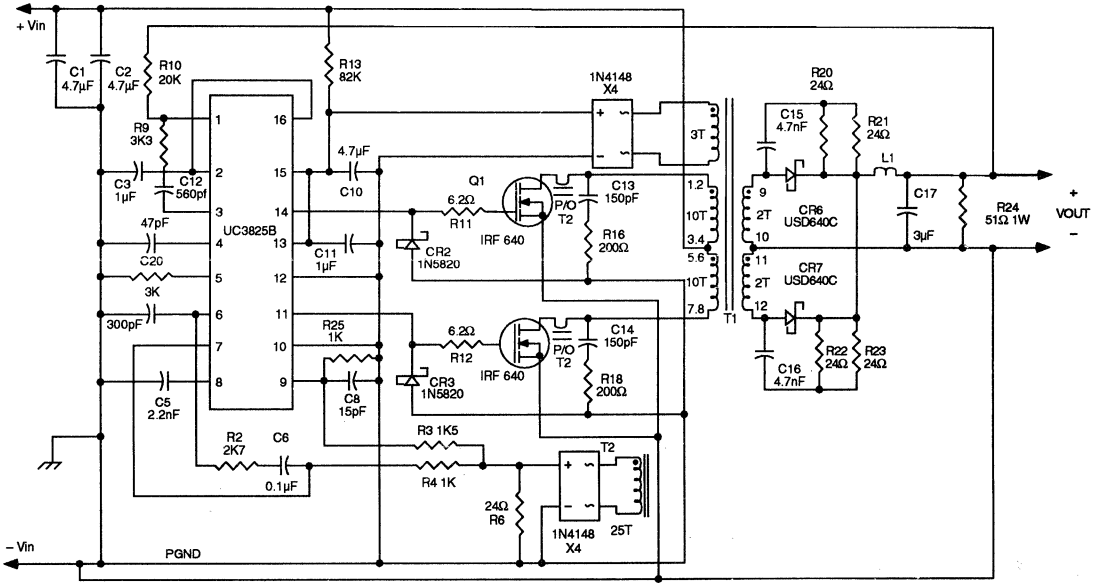


Figure 17 UC3825B Controlled 1.5 MHz Push Pull Converter

CONVERTER PERFORMANCE

The redesigned converter exhibited similar line, load and transient response to the original converter, which was excellent due to the high conversion frequency. A significant improvement was made in the short circuit performance by comparison. While operating into a continuous short circuited output, the UC3825"B" controlled version reduced the converter input power (and dissipation) to approximately one-hundredth of the original design. Featuring the programmable Restart Delay circuitry, the redesigned 50 Watt converter draws only one-quarter of a Watt (1/4 W) of input power with a shorted circuited output.

SUMMARY

This new generation of UC3823A,B and UC3825A,B PWM controllers features a multitude of performance advantages over its predecessors. Higher precision, increased protection and programmable new functions are just a few of the benefits obtainable with these enhanced versions of PWMs. And as the level of sophistication in todays power supplies increases, so too must that of its components - especially control ICs. Containing an expanded list of integrated features, this new era of enhanced UC3823A,B and UC3825A,B controllers overcomes the challenges of the power supply industry for higher levels of power, protection and performance.

ADDITIONAL INFORMATION AND REFERENCES

1. New Pulse Width Modulator Chip Controls 1 MHz Switchers; UNITRODE Application Note # U- 107
2. 1.5 MegaHertz Current Mode IC Controlled 50 Watt Power Supply; UNITRODE IC Databook, Application Note # U-110
3. "Practical Considerations in Current Mode Power Supplies"; UNITRODE IC Databook, Application Note # U-111

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UC3907 LOAD SHARE IC SIMPLIFIES PARALLEL POWER SUPPLY DESIGN

MARK JORDAN
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INTRODUCTION

Many power supply manufacturers have found it economically feasible to make standard modular power supplies which are easily paralleled for higher current applications. If special provisions are not made to equally distribute the load current among the paralleled supplies, then one or more units will hog the load current leaving the other units essentially idle. This results in greater thermal stresses on specific units and a reduction in the system reliability. For example, reliability predictions will indicate that a component operating at 50 degrees above ambient will have one-sixth the lifetime of the same component operating at 25 degrees above ambient [1].

This paper will examine methods for load sharing presently being implemented discretely and then cover Unitrode's single chip solution, the UC3907 Load Share Controller, in several parallel power applications.

SYSTEM REQUIREMENTS

The basic requirements of a power supply system consisting of a number of sources paralleled to increase the total load current are:

- Maintain a regulated output voltage under variations in line or load.
- Control the output current of each supply so they share the total load current equally.

To maximize reliability of the system, there are the following features:

- Achieve redundancy, so that a failure of any one supply can be tolerated as long as there is sufficient current capacity available from the remaining power units.
- Implement a load sharing method without any external control system.

In addition, these are the following desirable features:

- To have a common, low bandwidth share bus interconnecting all power units.
- Achieve good load sharing transient response.
- The ability to margin the system output voltage with one control.

In other words, the combination of power supplies behave like one large supply with equal stress on each of the units. Also, reliability can be optimized by taking advantage of load sharing to incorporate modular redundancy.

LOAD SHARING TECHNIQUES

There are a number of schemes to achieve load sharing. Five approaches are discussed here, with an attempt made to investigate their application, highlighting features and concerns.

THE DROOP METHOD

The simplest method to load sharing is referred to as the droop method. It is an open loop technique which programs the output impedance of the power supplies to obtain load sharing. This method exhibits very poor current sharing at low currents and improves at higher currents, but can still have large current imbalances between supplies. An example of this method is shown in Fig 1 where as the individual supply current increases, the feedback voltage will decrease. This will allow other supplies to distribute more current. The programmed output impedance is given by:

$$Rout = 0.01\ Rs\ N$$

The disadvantages to the droop method are: degradation of load regulation, each module must be individually tweaked to achieve good current sharing, and difficulty in current sharing between parallel modules with different power ratings.

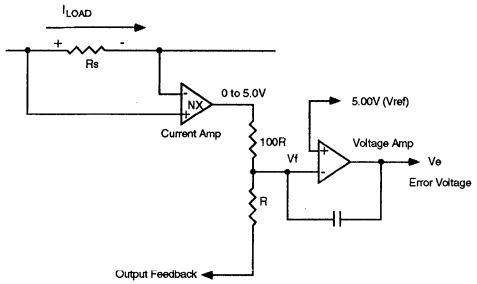

Fig 1 - The Droop method programs the output impedance of the power supplies to achieve load sharing. It is a simple open loop method, but is not accurate.

DEDICATED MASTER

Current mode supplies can accommodate several configurations to achieve a form of load sharing. One approach is to select a master module to perform the voltage control and force the remaining modules (slaves) to act as current sources, as shown in Fig. 2. This technique is facilitated with current mode control, since the error voltage is proportional to load current. If the units were similar in design then a given error voltage on the output of the voltage, or error amplifier will force all units to source the same load current. This technique achieves load sharing but does not achieve redundancy, since if the master fails, the entire system becomes disabled. Another concern with this technique is that the high bandwidth voltage loop is being bussed around the system and is prone to noise pick-up.

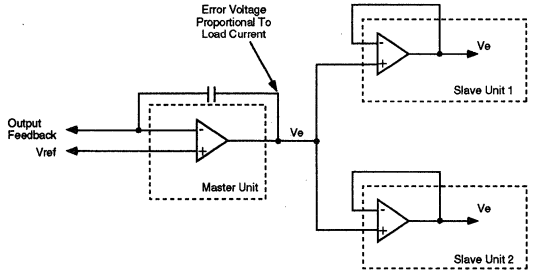

Fig 2 - A dedicated Master approach with current mode supplies will facilitate current sharing but does not achieve redundancy.

EXTERNAL CONTROLLER

Another method is to use an external controller to perform the load sharing. This is achieved by comparing all load sharing signals from the individual power units and adjust the corresponding feedback signal to balance the load currents. This system does perform well but requires an additional controller and multiple connections between the controller and each supply.

AUTOMATIC CURRENT SHARING - AVERAGE CURRENT METHOD

For Automatic current sharing no external controller is required and a single share bus interconnects all the supplies. This requires an adjustment amplifier that compares a current signal from the share bus to the individual units current, and adjusts the reference of the voltage amp until equal load current distribution is achieved.

The average Current method is a patented technique where each power module's current monitor drives a common share bus via a resistor, as shown in Fig 3. The adjust amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjusts the reference accordingly. The node where all resistors connect is a representation of the average load current contribution. While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into current limit, causing the share bus to be loaded down and the output voltage to regulate to the lower adjust limit. A similar failure mode will exist if the share bus is shorted or if any unit on the share bus is inoperative.

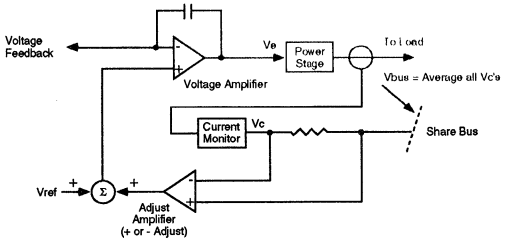

Fig. 3 - The average current method compares the individual load currents to the average load current.

AUTOMATIC CURRENT SHARING - HIGHEST CURRENT METHOD

This technique for automatic current sharing shown in Fig 4 compares the highest current module to each individual current, and adjusts the reference voltage accordingly to correct the imbalance of load current. This technique is similar to the average current method except that the resistor is replaced with a diode, allowing only one unit to communicate on the share bus. This method provides for excellent sharing among the slaves with an error in the master's load current contribution because of the diode.

The UC3907 Load Share Regulator has improved on this method by replacing the diode with a unidirectional buffer to reduce the master's error. An inoperative or insufficient capacity supply will not effect the sharing of the operational units. A shorted share bus will disable the reference adjustment section used for load sharing, making the units operate as stand alone.

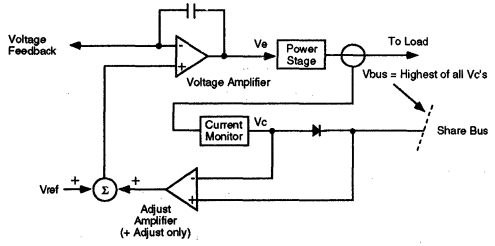

Fig. 4 - The highest current method compares the individual load currents to that of the highest. This method has several advantages over the average current method of load sharing. The UC3907 has implemented and improved version of this technique.

USING THE UC3907 - LOAD SHARE REGULATOR IC

A review of the current sharing technique used on the UC3907 and operating principles will help the reader to understand the application examples that follow and to use the IC in other examples.

A generic load share system with the basic bus connections required to perform accurate output voltage control and load sharing is shown in Fig 5. The output voltage is sensed with a fully differential, high-impedance voltage amplifier. Each individual power supply current is sensed with a differential current amplifier, and is used for the load share portion of the circuit. The share bus signal interconnecting all the paralleled modules is a low-impedance, noise insensitive line. The connection diagram is shown in FIG 6. The following discussion of the voltage and current sharing loops should help the reader understand the operation and features of the IC.

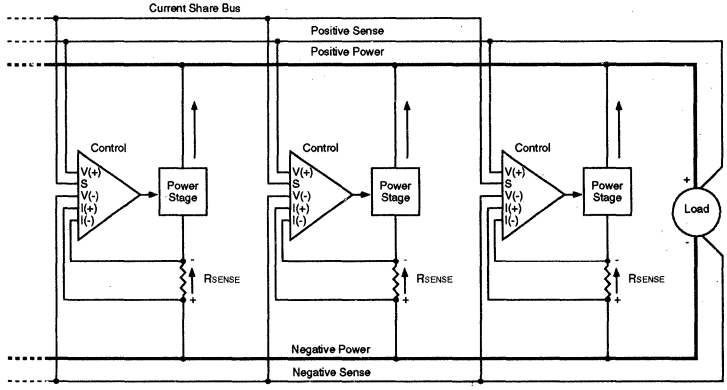

Fig. 5 - System connections for modules with independent load sharing.

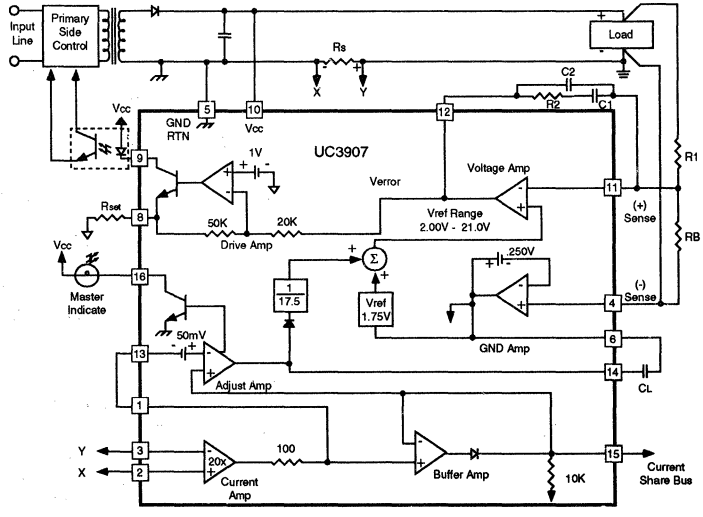

Fig. 6 - The UC3907 will control output voltage and equally distribute load current among the power modules.

THE VOLTAGE LOOP

THE VOLTAGE AMP

This Amplifier is the feedback control gain stage for the power modules output voltage regulation, and the overall voltage loop compensation will normally be applied around this amplifier. The output swing is limited to 2 Volts to improve the large signal response of the system. The voltage amplifier accomplishes the high impedance positive sensing, and the ground amp, the high impedance negative sensing.

THE GROUND AMP

This amplifier is a unity gain buffer with a 0.250V offset. The offset allows the amplifier negative headroom to return all control bias and operating currents while maintaining a high impedance negative sense input (pin 4), where this input is referred to as "true" ground. The output of this amplifier is referred to as Artificial Ground. The 0.250V offset is added to the 1.750V bandgap reference to obtain the 2.00V reference , as seen by the voltage amp, and is trimmed to +/-1.25%.

The ground return (pin 5) should be the most negative voltage available and can range from zero to 5V below the negative sense input. All the IC's current will return through the ground return pin.

THE DRIVE AMP

This amplifier is an inverting amplifier with a gain of -2.5, which couples the feedback signal to the power controller. The Current setting resistor Rset helps to establish the forward transfer function of the control loop and the maximum drive current. The polarity of the drive amp stage is such that an increasing voltage at the plus sense input (pin 11), will increase the opto-couplers current, thereby reducing the primary side PWM's duty cycle. This will insure proper startup since there is no energy on the secondary side during initialization of the power system.

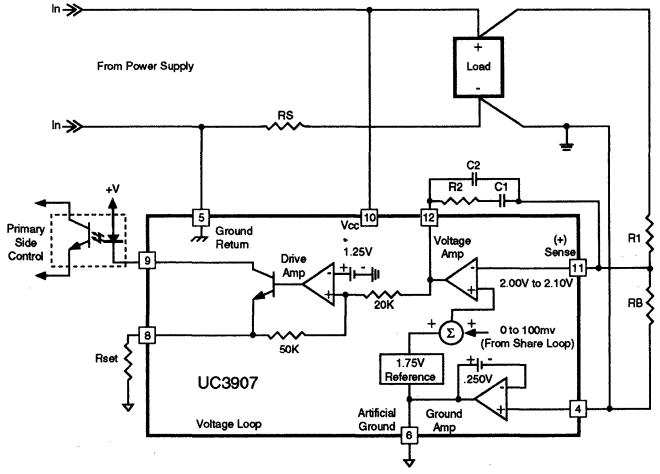

Fig. 7 - The UC3907 Voltage Loop achieves high impedance differential sensing along with optical coupler driving capability.

THE CURRENT LOOP

THE CURRENT AMP AND BUFFER AMP

The current sharing portion of the IC utilizes the current amp, the buffer amp, and the adjust amp as shown in Fig. 8. The Output of the current amp is an analog representation of individual load current, where the output voltage is given by: Vca=20*Rs*Iout. The current amp output feeds an input of a unidirectional buffer which drives the current share bus. Since the buffer amp only sources current, it insures that the module with the highest load current will be the master, or communicator to all other modules, and drives the bus through a low-impedance. All other buffer amplifiers will be inactive with each exhibiting a 10K ohm load impedance to ground.

THE ADJUST AMP

The adjust amplifier will compare its own load current with that of the highest current module, and force a command to adjust the individual modules reference voltage, (as seen by the voltage amp) to maintain equal current sharing. It is a transconductance type amplifier in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to artificial ground. The ground referenced compensation will act similar to that of integral compensation, but without the non-inverting signal feedthrough problems, thereby filtering both inputs from

unwanted noise. The adjust amplifier has a built in 50 millivolt offset on its inverting input, which forces the unit acting as a master to have a low output resulting in a zero adjust command. While the 50mv offset represents an error in current sharing, the gain of the current amplifier reduces it to 2.5 millivolts across the sense resistor. This results in all slave modules sharing equally and the master module running a few percent higher. The offset also provides some immunity from cycling, or fighting for master position due to low frequency noise.

STATUS INDICATE

The status indicate pin is designed to indicate which unit is acting as the master. Its open collector output is activated when the adjust amp output is in the low state. In a case of an overcurrent fault with one of the many paralleled units, this pin will indicate the unit with the highest current which will help diagnose the faulted module. A zero current or low current fault is transparent to the other supplies' and has no effect on voltage regulation and current sharing.

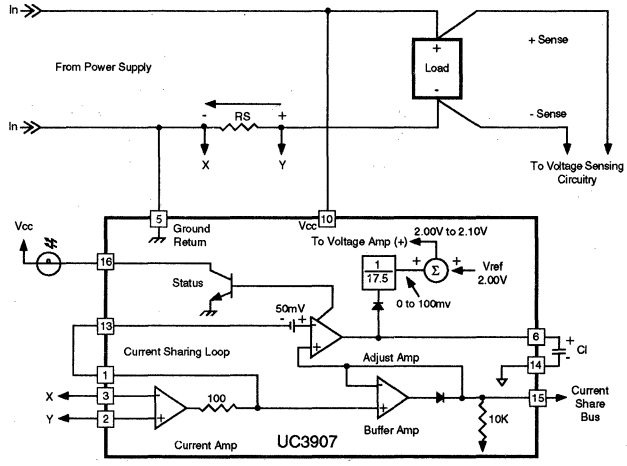

Fig. 8 - Current sharing is achieved with the UC3907 by comparing the individual module's current to that of the highest current module. The necessary adjust command increases the voltage amp reference to accomplish equal load sharing.

START-UP FOR A PARALLEL POWER SYSTEM

Start-up conditions need to be considered in a parallel power supply architecture. A start-up timing example of four 5V power modules in parallel is shown in Fig. 9. Once the primary power is applied, the power stage will be requesting maximum duty cycle until the individual units feed back a signal to regulate the output voltage. At time t1, supply #1 has become the master due to its higher reference voltage. This forces the output voltage to regulate above the other units. The other units will feedback a zero duty cycle signal to the power stage and remain idle. At this point the master unit is supplying all the supply current, and outputting the corresponding current signal on the share bus. The other units' adjust amplifiers sense the difference between their individual load currents and the master's, and start to slew up the adjust amp output to increase their references. At the same time the master's adjust amplifier output remains clamped below the adjust threshold having no effect on its original reference. At time t2 the other three adjust amps have exceeded the adjust threshold and have started to effect the reference as seen by the voltage amp.

At time t3 the unit with the closest reference to the master, supply #2, has reached the point where its references is essentially equal to the master's and the load current becomes equally distributed between the two. The other two modules, #3 and #4, are still adjusting their references and are not yet contributing to the load current. At time t4 the 3rd unit has reached the desired reference and the load current has been equally split between the three, and at time t5 the final unit has completed its reference adjustment, thereby completing the load sharing. If it is necessary to have the units come up sharing, then a soft-start scheme will need to be implemented on the primary side modulator which needs to be much slower than the adjust time. The total adjust time from t1 to t5 for this example is given by:

$$t = \frac{Cl\ Va}{I}$$

where Cl = adjust amp compensation
Va = adjust amp swing
I = Adjust amp max current - 220ua

Cl is chosen from the desired bandwidth

$$Cl = \frac{gm}{2\pi F}$$

where typ gm = 3mS and F = Adjust amp bandwidth.

If the required adjust amp bandwidth were 500 Hz, then Cl will be 1uF. The adjust amp output for the lowest reference will adjust to a voltage calculated as follows:

$$Vadj = (VREF_{max} - VREF_{min})\ 17.5 + 1$$
$$= (30mv\ 17.5) + 1 = 1.53$$

The adjust amp must slew from approximately 0.7V to 1.53V at a slew rate of 220mV/ms which equates to a complete sharing delay time of 3.8 ms.

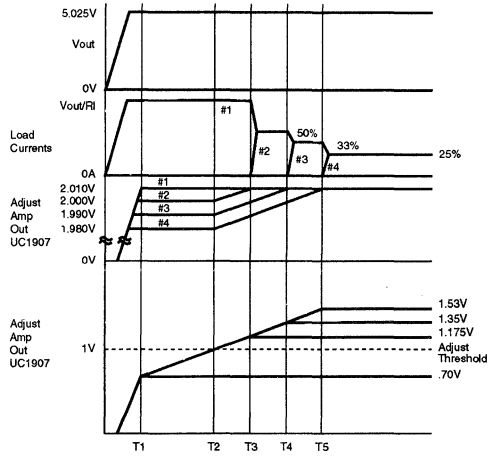

Fig. 9 - Start-up timing of a four module power system using the UC3907 (without soft-start).

THE VOLTAGE AND SHARE LOOP DESIGN

A load sharing system is composed of two loops, the voltage loop and the current share loop. As in conventional designs, the voltage loop regulates the output voltage and is the faster responding loop. The current sharing loop is a lower bandwidth loop to eliminate noise pick-up on the share line, and should be low enough in bandwidth to eliminate interactions with the voltage loop.

A complete loop diagram is shown in Fig. 10. The voltage amp transfer function is designed to optimize the voltage loop response, which is determined by the modulator topology, filters, and other gain functions in the loop. We will work through each gain block for a flyback converter example using the UC3907, and from this the user should be able to expand the design to any topology.

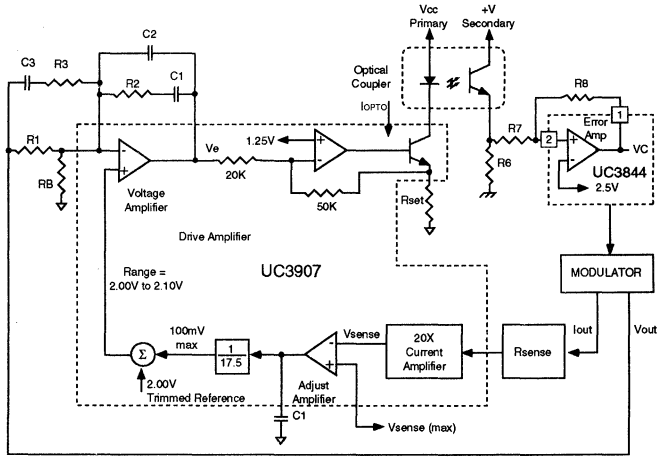

Fig. 10 - The UC3907 can be easily implemented to perform voltage control, and optical coupler drive for isolated applications.

Compensated as shown, the voltage amp response is given by:

$$UGF = \frac{1}{2\pi R_1(C_1 + C_2)} \qquad Pole = Origin$$

UGF = Unity Gain Frequency.

$$Pole\ 2 = \frac{1}{2\pi R_1 C_3} \qquad Pole\ 3 = \frac{1}{2\pi R_2\left(\frac{C_1C_2}{C_1+C_2}\right)}$$

$$Zero\ 1 = \frac{1}{2\pi R_2 C_1} \qquad Zero\ 2 = \frac{1}{2\pi(R_1+R_3)C_3}$$

The drive amp will convert the output of the voltage amp to an error current to be applied to the opto coupler. The current is given by:

$$I_{opto} = \frac{(1.25 - Ve)2.5 + 1.25}{Rset}$$

where Ve = output of the voltage amp - error voltage and the small signal gain is:

$$\frac{I_{opto}}{v_e} = \frac{-2.5}{Rset}$$

The control voltage for the UC3844 pulse width modulator is given by:

$$V_c = (2.5 - I_{opto}\,CTR\,R_6)\left(\frac{R_8}{R_6+R_7}\right) + 2.5$$

where CTR is the current transfer ratio of the opto coupler. and the small signal gain is given by:

$$\frac{v_c}{I_{opto}} = -CTR\,R_6\left(\frac{R_8}{R_6+R_7}\right)$$

therefore the UC3907 error voltage to PWM control voltage gain is given by:

$$\frac{v_c}{v_e} = CTR\,R_6\left(\frac{R_8}{R_6+R_7}\right)\left(\frac{2.5}{R_{set}}\right)$$

The CTR spread can vary from 0.4 to 2 on a given device type, but many manufacturers can sort them out to a +/- 30% tolerance. The CTR is also a function of the driving current and therefore introduces a non-linearity in the feedback gain.

The control to output gain of the modulator for various topologies is referenced in the Unitrode power supply design seminar book. For example, the control to output gain for the discontinuous flyback with current mode control is:

$$\frac{v_o}{v_c} = \sqrt{\frac{Ro\,L\,F}{2}}\,\frac{\left(1+\frac{S}{wz}\right)}{\left(1+\frac{S}{wp}\right)}$$

$$Where\ wz = \frac{1}{Rc\,C} \qquad wp = \frac{1}{Ro\,C}$$

Rc = esr of C's in parallel
Ro= Load resistance
C= Total output Capacitance
L= Primary inductance
F= Switching frequency

The total voltage loop gain is given by:

$$G(S) = A(s)\left(\frac{v_c}{v_e}\right)\left(\frac{v_o}{v_c}\right)$$

where A(s) is the voltage amp transfer function

To bandwidth limit the share loop, the adjust amplifier is compensated where the unity gain frequency of the adjust amp is given by :

$$F = \frac{gm}{2\pi C_l}$$

where typical gm = 3mS.

AN OFF-LINE LOAD SHARE APPLICATION

An off-line power supply application utilizing the UC3907 Load Share Controller is shown in Fig. 11 for a flyback regulator. The UC3844 is the modulator and its switching frequency is determined by Fs = 1.72/(Rt Ct). The resistor R5 will sense the primary inductor current, where the maximum peak current for the UC3844 is given by ISmax= 1.0V/R5. Startup is achieved with R1 and C5 until bootstrap winding W2 can feedback to power the UC3844. The snubber network D3, C4, and R2 prevents turn-off voltage spikes from exceeding the FET breakdown voltage. The primary soft-start circuit is comprised of Q1, R9 and C10.

Note that the resistor Rset and adjust compensation is connected to artificial ground (pin 6). Artificial ground is a replica of the "true" ground voltage on pin 4, negative sense, plus a 0.250V level shift. This allows a low impedance point for ground referenced elements to connect.

A master indicator lamp is included in the design so that the unit supplying the most load current and determining the output regulating voltage can be detected. There are many useful applications for this pin as in supply voltage margining or determination of a faulted supply which is supplying an excess voltage/current.

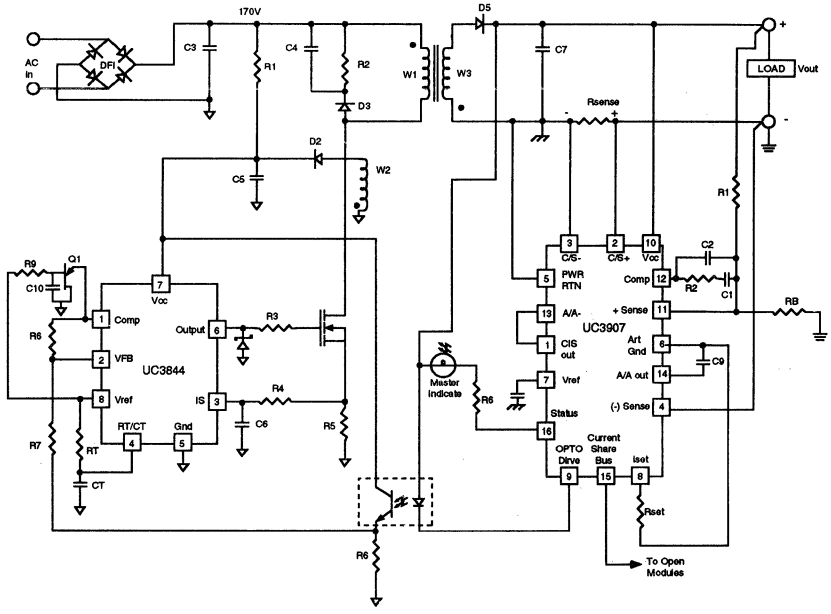

Fig. 11 - The UC3907 in an off-line isolated application.

NON-ISOLATED CONVERTER APPLICATIONS

There are applications were non-isolated DC to DC converters are paralleled to make a power system. Fig. 12 shows a step down, or buck, regulator utilizing the UC3524A voltage mode PWM and the UC3907 Load share IC. For non-isolated parallel power supply applications the current sensing must be done on the high side. The reason for this is that if the sensing was performed on the low side where the power supply inputs and outputs are common, then all the current sense resistors will end up in parallel, defeating the individual sensing and load sharing. The only limitation to high side current sensing in a non-isolated application is that the current amplifier of the UC3907 has a common mode range of 0V to Vin -2V, therefore a form of level shifting or average current sensing would be required.

Since the opto-coupler is not required, an inversion has been eliminated which the driving scheme must accommodate for. The Iset voltage is a gained up inverted error voltage from the UC3907 voltage amp. The UC3524A error amp is set up as an inverter and cancels out the drive amp inversion leaving the error voltage of the UC3907 to be transposed to the UC3524A in proper phase. The iset voltage will swing from 0v to 3.8V min. Current limiting is achieved by taking the current amp output signal from the UC3907 and feeding it in to the UC3524A current limit amplifier, where the current limit is given by:

$$Icl = \frac{5\left(\frac{R_{12}}{R_{11}+R_{12}}\right)+0.2}{20\,R_{sense}}$$

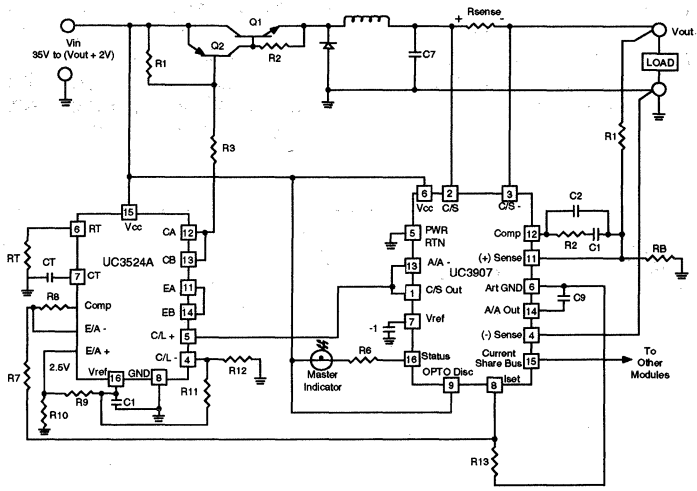

Fig. 12 - The UC3907 in a non-isolated DC to DC converter application.

LINEAR REGULATOR EXAMPLE

A simple linear regulator with load sharing using the UC3907 IC and a few external components is shown in Fig. 13. The phasing of the opto drive pin facilitates darlington drive, and supply current limiting is achieved by Q3, C1, R11, and R12 with the current limit given by:

$$Icl = \frac{VBE_{Q3}\left(1 + \frac{R_{11}}{R_{12}}\right)}{20\,R_{sense}}$$

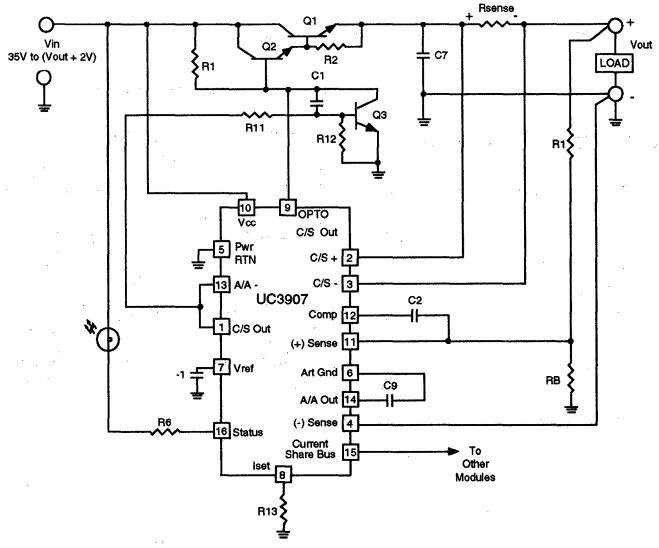

Fig. 13 - With a few external components the UC3907 can make a simple linear regulator with load sharing.

EXTERNAL LOAD SHARING

The UC3907 can be easily incorporated outside the power module to achieve load sharing, as shown in Fig 14. The load sharing loop is similar to previous examples, but instead of adjusting the internal reference of the UC3907, this technique adjusts the (+) sense line of the power module to force equal current sharing. The maximum adjust voltage is given by:

$$Vadj_{max} = 1.75\left(\frac{R_1}{R_2}\right)$$

LOAD SHARING CAN BE EXTERNALLY ADDED TO EXISTING POWER MODULES

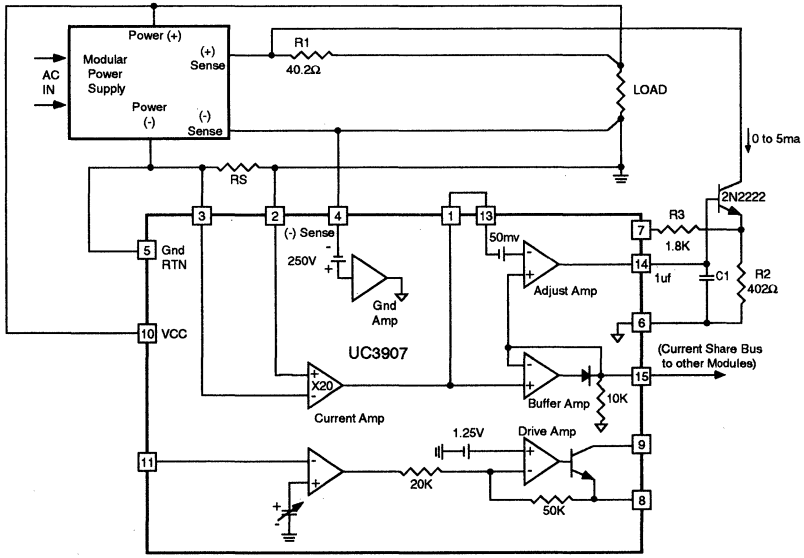

Fig. 14 - The power supplies remote sense inputs are used to facilitate load sharing.

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DEDICATED ICs SIMPLIFY BRUSHLESS DC SERVO AMPLIFIER DESIGN

John A. O'Connor

INTRODUCTION

Brushless DC motors have gained considerable commercial success in high end four quadrant servo systems, as well as in less demanding, one and two quadrant requirements. Cost sensitive four quadrant applications thus far have not fared as well. Designs which meet cost goals often suffer from poor linearity, and cumbersome protection circuits to assure reliable operation in all four quadrants. Better performance entails more complex circuitry and the resulting additional components quickly increase size and cost. Part of the design challenge results from the lack of control ICs tailored to four quadrant applications. The other major obstacle has been implementing a reliable and cost effective high-side switch drive. With recently introduced integrated circuits in both areas, it is now possible to design a rugged, low cost, four quadrant brushless DC servo amplifier with relatively low component count and cost.

SERVO AMPLIFIER REQUIREMENTS

First, let's quickly review general servo amplifier requirements. Figure 1 displays motor speed versus torque, depicting four possible modes of operation. While a system may be considered four quadrant by simply having the ability to operate reliably in all four modes, a servo system generally requires *controlled* operation in

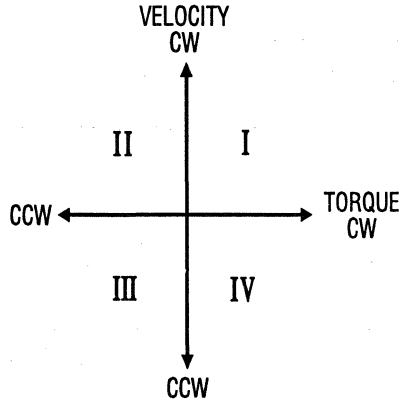

Figure 1 - Four Quadrants of Operation

all four modes. In addition, a smooth, linear transition between quadrants is essential for high accuracy position and velocity control. The major performance differences between brushless DC servo amplifiers are related to accuracy, bandwidth, and quadrant transition linearity.

Most simple brushless DC amplifiers provide two quadrant control, since even the simplest output stages (typically 3 phase bridge) allow rotation reversal. Note that this is operation in quadrants one and three where torque and rotation are in the same direction. This differs from brush motor terminology where two quadrant control normally implies unidirectional rotation with torque control in either direction. Although limited to a single rotation direction, bidirectional torque allows servo velocity control, with rapid, controlled acceleration and deceleration. These characteristics are well suited to numerous applications such as spindle and conveyer drives. With the two quadrant brushless DC amplifier, there are no provisions other than friction to decelerate the load, limiting the system to less demanding applications. Attempting to operate in quadrants two and four will result in extremely nonlinear behavior, and under many circumstances, severe damage to the output stage will follow. This occurs because the two quadrant brushless DC amplifier is unable to completely control current during torque reversal.

TWO QUADRANT VERSUS FOUR QUADRANT CONTROL

Figure 2 shows a three phase bridge output stage for driving a brushless DC motor. Current flow is shown for two quadrant control when operation is in quadrants one or three. The switches commutate based on the motor's

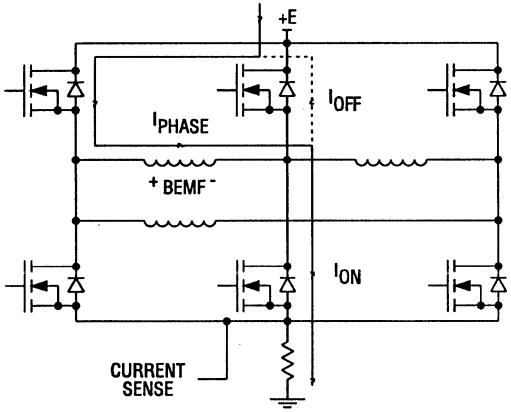

Figure 2 - Two Quadrant Chopping

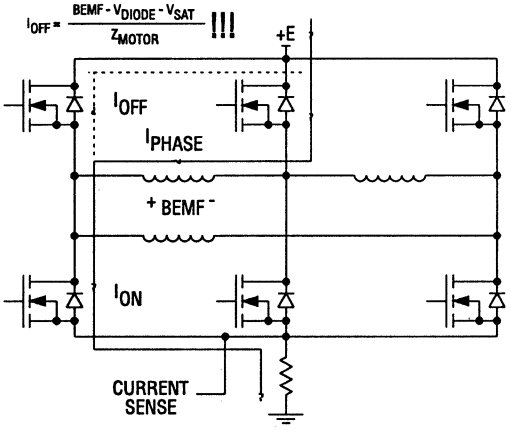

Figure 3 - Two Quadrant Reversal

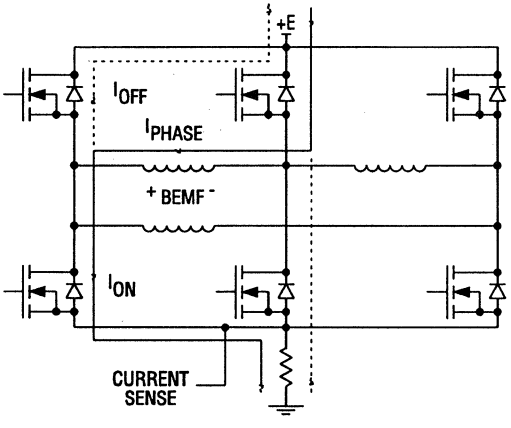

Figure 4 - Four Quadrant Reversal

rotor position, typically using Hall effect sensors for position feedback. Current is controlled by pulse width modulating (PWM) the lower switches. Figure 3 shows current flow if the direction of torque were reversed. The upper switch essentially shorts the motor's back EMF (BEMF), causing current to quickly decay and reverse direction. The current then rises to a value limited only by the motor and drive impedance, yet is undetected by supply or ground sense resistors. As the motor speed rises, its BEMF proportionally increases, quickly escalating the potential circulating current. Even if the output stage is built rugged enough to withstand this abuse, the high uncontrolled current causes high uncontrolled torque, making this technique unsuitable for most servo control applications.

By pulse width modulating the upper switches along with the lower switches, uncontrolled circulating currents are avoided. With both upper and lower switches off during during the PWM off time, motor current will always decay as shown in figure 4. Additionally, motor current always flows through the ground sense resistor, allowing easy detection for feedback. The remainder of this article will feature this mode of control, as it is well suited for a variety of demanding requirements. It should be noted however, that a penalty in the form of reduced efficiency must be paid for the improvement in control characteristics. With two switches operating at the PWM frequency, as opposed to one with two quadrant control, switching losses are nearly doubled. Ripple current is also increased which results in greater motor core loss. Although this is a small price to pay under most circumstances, extremely demanding applications may require switching between two and four quadrant operation for optimum efficiency and control.

FOUR QUADRANT CONTROLLER REQUIREMENTS

In addition to switching both upper and lower transistors, a few supplementary functions are required from the control circuit for reliable four quadrant operation. With two quadrant switching, there is inherent dead time between conduction of opposing upper and lower switches, making cross conduction virtually impossible. Four quadrant control immediately reverses the state of opposing switches at torque reversal, thus requiring a delay between turning the conducting device off and the opposing device on to avoid simultaneous conduction and possible output stage damage.

When torque is reversed, energy stored in the rotating load is transferred back to the power supply, quickly charging the bus storage capacitor. A clamp circuit is

typically used to dissipate the energy and limit the maximum bus voltage. As a second line of defense, an over-voltage comparator is often employed to disable the output if the bus voltage exceeds the clamp voltage by more than a few volts.

CURRENT LOOP CONTROL TECHNIQUE

A transconductance amplifier is normally used for brushless DC servo applications, providing direct control of motor torque. Average current feedback is usually employed rather than the more familiar peak current

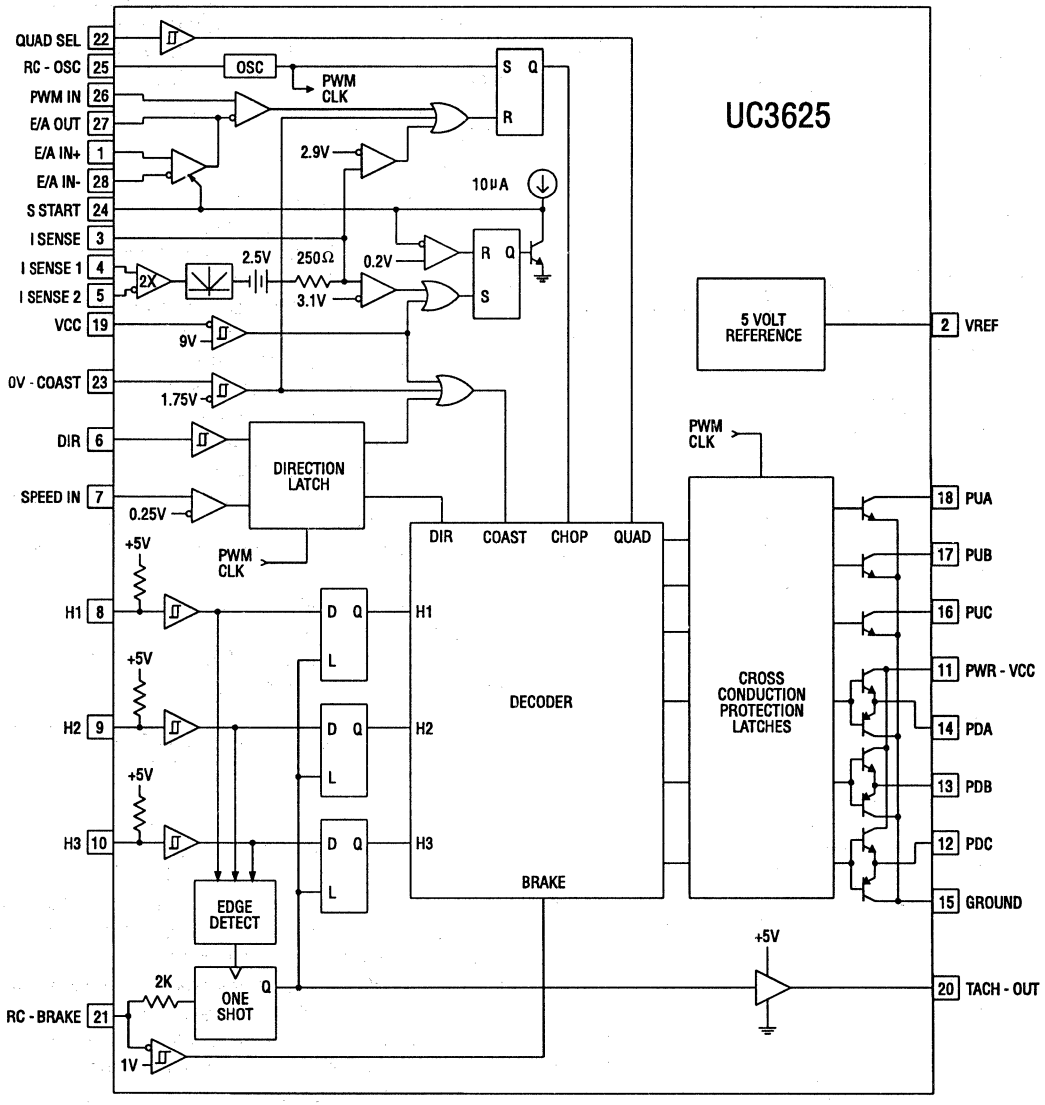

Figure 5 - UC3625 Block Diagram

control for several reasons. Peak current control is subject to subharmonic oscillation at the switching frequency for duty cycles above 50%. This condition is easily circumvented in power supply applications by summing an appropriately scaled ramp signal derived from the PWM oscillator with the current sense signal. This technique is commonly refered to as slope compensation. It can also be shown [3] that for a given inductor current decay rate, which is esentially fixed in a power supply application, there is an optimal compensation level which will produce an output current independant of duty cycle. Unfortunately, the inductor current decay rate in a four quadrant motor control system varies with both speed and supply voltage, making an optimal slope compensation circuit fairly complex. Simpler circuits which provide over compensation assure stability but will degrade accuracy. Furthermore, severe gain degradation occurs when inductor current becomes discontinuous regardless of slope compensation, causing large nonlinearity at light load. This effect can be particularly troublesome for a position control servo. Average current feedback avoids these problems, and is therefore the prefered current control technique for servo applications.

UC3625 BRUSHLESS DC CONTROLLER

Figure 5 shows the UC3625 block diagram. Designed specifically for four quadrant operation, it minimizes the external circuitry required to implement a brushless DC servo amplifier. Flexible architecture and supplementary features make the UC3625 well suited to less demanding applications as well. The UC3625 is described in detail in references [4] and [7], however a few features critical for reliable four quadrant operation should be noted.

Cross conduction protection latches eliminate the possibility of simultaneous conduction of upper and lower switches due to driver and switch turn-off delays. Additional analog delay circuits normally associated with this function are eliminated allowing direct switch interface and reduced component count. An absolute value buffer following the current sense amplifier provides an average winding current signal suitable for feedback as well as protection. An over-voltage comparator disables the outputs if the bus voltage becomes excessive.

Although not absolutely necessary for four quadrant systems, a few additional features enhance two quadrant operation and simplify implementation of switched two / four quadrant control for optimized systems. A direction latch with analog speed input prevents reversal until an acceptably low speed is reached, preventing output stage damage. Two or four quadrant switching can be selected during operation with the Quad Select input. A brake input provides current limited dynamic braking, suitable for applications which require rapid deceleration, but do not need tight servo control.

A SIMPLE BRUSHLESS DC SERVO AMPLIFIER

To demonstrate the relative simplicity with which a brushless DC servo amplifier can be implemented, a 6 amp, off-line 115 VAC amplifier was designed and constructed. Note that current and voltage rather than horsepower are specified. Although theoretically capable of in excess of one horsepower, simultaneous high speed and torque are typically not required in servo applications, reducing the actual output power, and the corresponding power supply requirement. Average current feedback is employed, providing good bandwidth and power supply rejection, thus making the amplifier suitable for many demanding requirements. A complete amplifier schematic is shown in figure 6.

A high performance brushless servo motor from MFM Technology, Inc. was used to evaluate the amplifier. While most of the design is independent of motor parameters, several functions should be optimized for a particular motor and operating conditions. The motor used has the following electrical specifications:

Model M - 178

K_T	79 oz.in./Amp
R_M	1.3 ohms
L_M	5.5 mH
Poles	18

OUTPUT STAGE DESIGN

Having selected a four quadrant control strategy, we proceed to the output stage design, and work back to the controller. High voltage MOSFETs are well suited to this power level, however IGBTs may also be incorporated. MOSFETs were selected to minimize size and complexity, since the body diodes can be used for the flyback rectifiers. Unfortunately, this places greater demands on the MOSFET, and increases the device dissipation. The MOSFETs body diode is typically slower and stores more charge than a discrete high speed rectifier, which necessitates a slower turn-on and a corresponding increase in switching losses. These losses are partially offset by choosing a MOSFET with sufficiently low conduction losses which offers the secondary benefits of greater peak current capability and reduced thermal

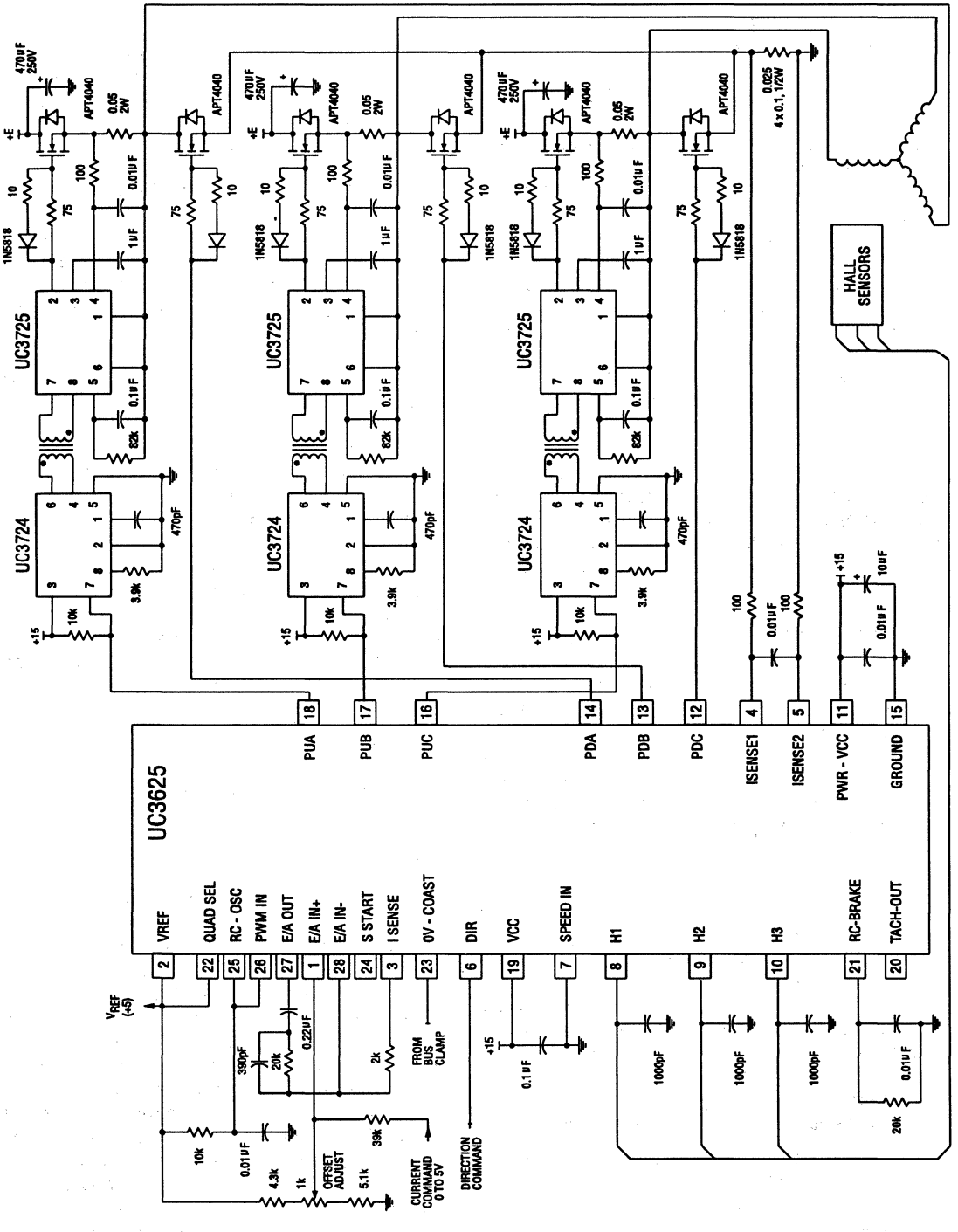

Figure 6 - Brushless DC Servo Amplifier Schematic

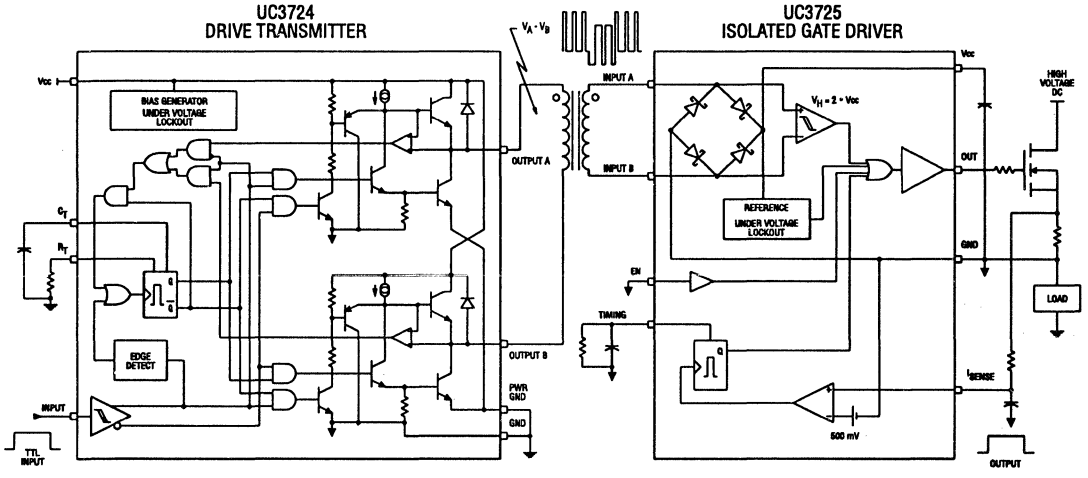

Figure 7 - UC3724/UC3725 Isolated MOSFET Driver

resistance. APT4030BN MOSFETs were selected for the output stage to handle the 6 amp load currents while providing good supply voltage transient immunity. Rated at 400 volts and 0.30 ohms, they allow high efficiency operation and have sufficient breakdown voltage for reliable off-line operation.

While the lower three FETs require simple ground referenced drive, and are easily driven directly from the UC3625, the design of the drive circuit for the upper three FETs has traditionally been challenging. Discrete implementation of the required power supply and signal transmission is often bulky and expensive. In an effort to reduce size and cost, critical functions are often omitted, opening the door to potential reliability problems. Specifically designed for high-side MOSFET drive in motor control systems, the UC3724 / UC3725 IC pair shown in figure 7, offers a compact, low cost solution. A high frequency carrier transmits both power and signal across a single pulse transformer, eliminating separate DC/DC converters, charge pump circuits, and opto-couplers. Signal and power transmission function down to DC, imposing no duty cycle or on-time limitations typical of commonly used charge pump techniques. Under-voltage lockout, gate voltage clamp, and over current protection assure reliable operation.

Design of the upper driver is a straight forward procedure, and is described in detail in reference [5].
For this application, the driver is designed with the following specifications:

500 V minimum isolation
300 kHz carrier frequency
10 Amp over-current fault
10 ms over-current off time

The pulse transformer uses a 1/2 inch O.D. toroid core (Philips 204T250-3E2A) with a 15 turn primary and 17 turn secondary. For high voltage isolation, Teflon insulated wire is used for both primary and secondary.

To provide rapid turn-off for minimal switching losses, with slower turn-on for di/dt control, a resistor/resistor-diode network is used in place of a single gate resistor. Although present generation MOSFETs can reliably commutate current from an opposing FETs body diode at high di/dt, the resulting high peak current and diode snap limit practical circuits to a more moderate rate. This increases dissipation, but significantly eases RFI filtering and shielding, as well as relaxing layout constraints. Additionally, a low impedance is maintained in the off state while turn-on dv/dt is decreased, dramatically reducing the tendency for dv/dt induced turn on. The same gate network is used for both upper and lower MOSFETs.

A sense resistor in series with the bridge ground return provides a current signal for both feedback and current limiting. This resistor, as well as the upper driver current sense resistors should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impossible to eliminate, careful

layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values, and serve double duty as the half-bridge bypass capacitors.

CONTROLLER SETUP

The UC3625 switching frequency is programmed with a timing resistor and capacitor. Unless the motor's inductance is particularly low, 20 kHz will provide acceptable ripple current and switching losses while minimizing audible noise.

(1) $F = 2 / R_{OSC}C_{OSC}$

The relatively small oscillator signal amplitude requires careful timing capacitor interconnect for maximum frequency stability. Circuit board traces should to be as short as possible, directly connecting the capacitor between pins 25 and 15, with no other circuits sharing the board trace to pin 15 (ground).

When tight oscillator stability is required, or multiple systems must be synchronized to a master clock, the circuit shown in figure 8 can be used. As shown, the circuit buffers, and then differentiates the falling edge of the master oscillator. The last stage provides the necessary current gain to drive the 47 ohm resistor in series with the timing capacitor. If the master clock is from a digital source, the first two stages are omitted, and the clock signal is interfaced directly to the final stage through a restive divider as shown. The slaves are programmed to oscillate at a lower frequency than the master. The pulse injected across the 47 ohm resistor causes the oscillator to terminate its cycle prematurely, and thus synchronize to the master clock.

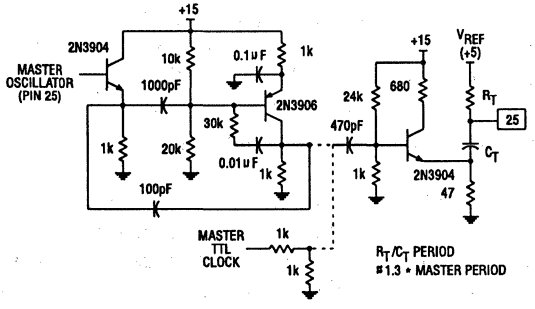

Figure 8 - External Synchronization Circuit

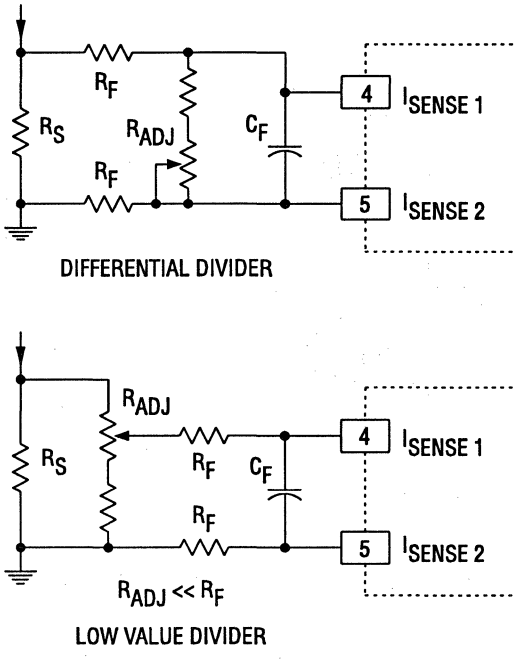

Figure 9 - Balance Impedance Current Sense Input Circuits

The RC-Brake pin serves two functions: Brake command input (not used in this design), and tachometer / digital commutation filter one-shot programming. Whenever the commutation state changes, the one-shot is triggered, outputting a tach pulse and inhibiting another commutation state change until the one-shot terminates. The one-shot pulse width is programmed for approximately 1/2 the shortest commutation period.

(2) $T_{PW} = 0.70\ R_TC_T$

where the shortest commutation period = $20 / (RPM_{MAX}N_{POLES})$

CURRENT SENSING AND FEEDBACK

For optimum current sense amplifier performance, the input impedance must be balanced. Low value resistors (100 to 500 ohm) are used to minimize bias current errors and noise sensitivity. Additionally, if the sense voltage must be trimmed, a low value input divider or a differential divider should be used to maintain impedance matching, as shown in figure 9.

An average current feedback loop is implemented by the circuit shown in figure 10. With four quadrant chopping, motor current always flows through the sense resistor. When PWM is off however, the flyback diodes conduct,

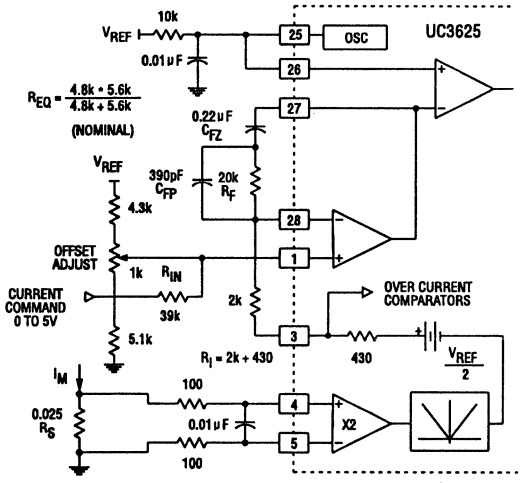

Figure 10 - Average Current Feedback Circuit Configuration

causing the current to reverse polarity through the sense resistor. The absolute value amplifier cancels the current polarity reversal by inverting the negative current sense signal during the flyback period. The output of the absolute value amplifier therefore is a reconstructed analog of the motor current, suitable for protection as well as feedback loop closure.

When the current sense output is used to drive a summing resistor as in this application example, the current sense output impedance adds to the summing resistor value. The internal output resistor and the amplifier output impedance can both significantly effect current sense accuracy if the external resistance is too low. Although not specified, the total output impedance is typically 430 ohms at 25 degrees C. Over the military temperature range of -55 to +125 degrees C, the impedance ranges from approximately 350 to 600 ohms. An external 2 k resistor will result in an actual 2.43 k summing resistance with reasonable tolerance. A higher value external resistor and trim pot will be required if high closed current loop accuracy is required.

The current sense output offset voltage is derived from the +5 V reference voltage. By developing the command offset from the +5 V reference, current sense drift over temperature is minimized. The offset divider must be trimmed initially to accommodate the current sense amplifier offset tolerance.

POWER SUPPLY AND BUS CLAMP

Input power is filtered to reduce conducted EMI, and transient protected using MOVs. Power-up current surge is suppressed using a NTC thermistor, while a bridge rectifier and capacitive filter complete the high voltage supply. A small 60 Hz. transformer supplies 15 Volts through a three pin regulator to power the control and drive circuits.

A bus clamp is easily designed around a UC3725 MOSFET driver, as shown in figure 11. As in the high-side switch drive, the UC3725 assures reliable operation, particularly during power-up and power-down. The divider current is set to 1 mA at the threshold, which is a reasonable compromise between input bias current error and dissipation. An additional tap programs the over-voltage coast a few volts above the bus clamp, saving a resistor and some dissipation while reducing the tolerance between the bus clamp and the over-voltage coast. Setting the bus clamp discharge current equivalent to the maximum motor current will assure effective clamping under all conditions. The load resistor value is therefore:

$$(3) \qquad R_L = \frac{V_{CLAMP}}{I_{MAX}}$$

The load resistor dissipation is dependant on the energy removed from the load inertia, and the frequency with which the energy is removed.

$$(4) \qquad P_{LOAD} = 1/2\, f J\, (\omega_1^2 - \omega_2^2)$$

where J = inertia in Nm sec²
ω_1 = initial velocity in rad/sec
ω_2 = final velocity in rad/sec

Note that if the deceleration time approaches the load resistor's thermal time constant, a higher power resistor will be required to maintain reliability.

CURRENT LOOP OPTIMIZATION

The block diagram of the current control loop is shown in figure 12. The current sense input filter has minimal affect on the loop and can be ignored, since the filter pole must be much higher than the system bandwidth to maintain waveform integrity for over-current protection. The current sense resistor R_S, is chosen to establish the peak current limit threshold, which is typically set 20% higher than the maximum current command level to provide over-current protection during abnormal conditions. Under normal circumstances with a properly compensated current loop, peak current limit will not be exercised. The input divider network provides both offset adjustment and attenuation, with R_{IN} selected to accomodate the current command signal range.

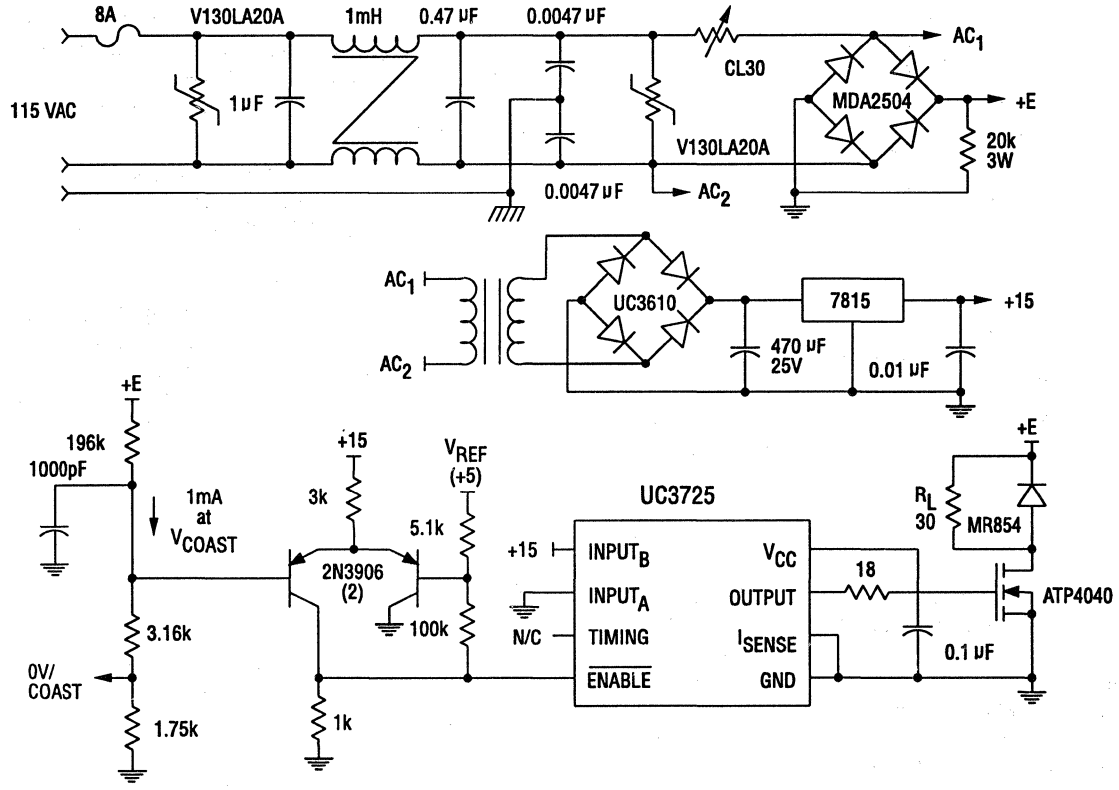

Figure 11 - Power Supply and Bus Clamp

All PWM circuits are prone to subharmonic oscillation if the modulation comparator's two input waveform slopes are inappropriately related. This behavior is most common in peak current feedback schemes, where slope compensation is typically required to achieve stability. Average current feedback systems will exhibit similar behavior if the current amplifier gain is excessively high at the switching frequency. As described by Dixon [2] to avoid subharmonic oscillation for a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion sets the maximum current amplifier gain at the switching frequency, and indirectly establishes the maximum current loop gain crossover frequency.

A voltage proportional to motor current, which is the inductor current, is generated by the current sense resistor and the current sense amplifier circuitry internal to the UC3625. This waveform is amplified and inverted by the current amplifier and applied to the PWM comparator input. Due to the signal inversion, the motor

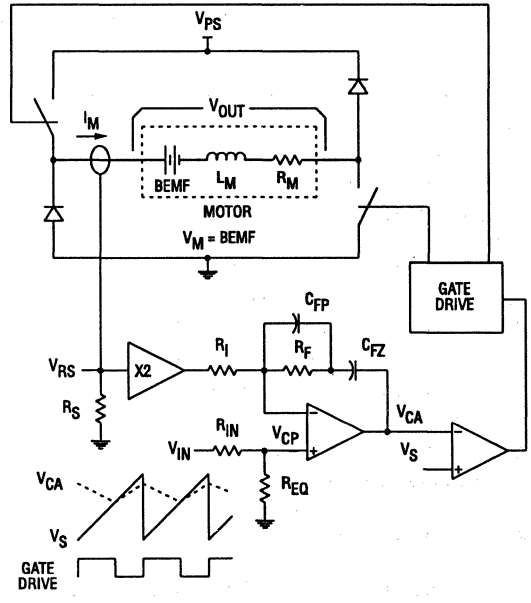

Figure 12 - Current Loop Block Diagram

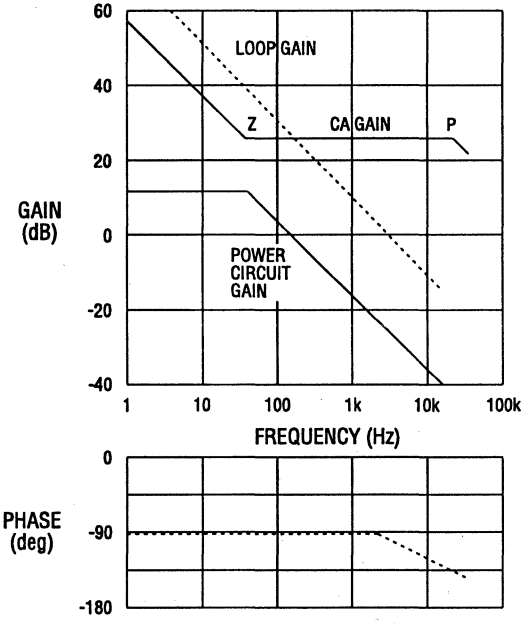

Figure 13 - Open Loop Gain and Phase Versus Frequency

current downslope appears as an upslope as shown in figure 12. To avoid subharmonic oscillation, the current amplifier output slope must not exceed the oscillator ramp slope. A motor control system typically operates over a wide range of output voltages, and is usually powered from an unregulated supply. The operating conditions which cause the greatest motor current downslope must be determined in order to determine the maximum current amplifier gain which will maintain stability. When four quadrant chopping is used, the inductor discharge rate is described by:

$$\text{Motor Current Downslope} = \frac{V_{PS} + V_M}{L_M}$$

The greatest discharge slope therefore occurs when the supply and BEMF voltages are maximum.

The oscillator ramp slope is simply:

$$\text{Oscillator Ramp Slope} = \frac{V_S}{T_S} = V_S f_S$$

Where: V_S is the oscillator ramp peak to peak voltage (1.2 V for the UC3625)
T_S is the switching period
f_S is the switching frequency

The maximum current amplifier gain at the switching frequency is determined by setting the amplified inductor current downslope equal to the oscillator ramp slope.

$$\frac{V_{PS} + V_M}{L_M} R_S G_{CA} = V_S f_S$$

$$(5) \quad \therefore \max G_{CA} = \frac{\Delta V_{CA}}{\Delta V_{RS}} = \frac{V_S f_S L_M}{R_S (V_{PS} + V_M)}$$

The maximum BEMF and supply voltage for the design example are 87 and 175 Volts respectively, which translates to a motor speed of 1500 RPM, and a high-line supply voltage of 125 Volts AC. Using equation (5) with an oscillator voltage of 1.2 volts peak to peak at a frequency of 20 kHz, the maximum value for G_{CA} is 20.2, or 26 dB. The current sense amplifier's gain of two is also part of G_{CA}. With R_I equal to 2.43 k, 20 k is selected for R_F to allow for tolerances, resulting in an actual G_{CA} of 16.5, or 24 dB.

The small-signal control to output gain of the current loop power section is described by:

$$(6) \quad \frac{\Delta V_{RS}}{\Delta V_{CA}} = \frac{R_S 2 V_{PS}}{V_S s L_M}$$

Note that the factor of two in the numerator is a result of four quadrant chopping which only utilizes one-half of the modulator's input range for a given quadrant of operation.

The overall open loop gain of the current loop is the product of the actual current amplifier gain and the control to output gain of the power circuit. The result is set equal to one to solve for the loop gain crossover frequency, f_C:

$$(7) \quad G_{CA} \frac{R_S 2 V_{PS}}{V_S 2\pi f_C L_M} = 1$$

$$(8) \quad f_C = \frac{G_{CA} R_S V_{PS}}{V_S \pi L_M}$$

9

At high line, where the supply is 175 Volts DC, f_c is 3.5 kHz. The crossover frequency drops to 2.8 kHz at low line, where the supply is approximately 140 Volts DC. If greater bandwidth is required, the current amplifier gain must be increased, requiring a corresponding increase in switching frequency to satisfy equation (5).

Up to this point the motor's resistance (R_M) has been ignored. This is valid since L_M predominates at the switching frequency. The motor's electrical time constant L_M/R_M, creates a pole, which is compensated for by placing zero R_FC_{FZ} at the same frequency. Additionally, pole $R_FC_{FP}C_{FZ}/(C_{FP}+C_{FZ})$ is placed at f_S to reduce sensitivity to noise spikes generated during switching transitions. The filter pole at f_S also reduces the amplitude and slope of the amplified inductor current waveform, possibly suggesting that the current amplifier gain could be increased beyond the maximum value from equation (5). Experimentally increasing G_{CA} may incur subharmonic oscillation however, since equation (5) is only valid for a system with a single pole response at f_S. For the design example, standard values are chosen for C_{FZ} and C_{FP} of 0.22 µF and 390 pF respectively, placing the zero at 36 Hz, and the pole at 20 kHz. Figure 13 shows open loop gain and phase verses frequency.

At very light loads, the motor current will become discontinuous - motor current reaches zero before the switching period ends. At this mode boundary, the power stage gain suddenly decreases, and the single pole characteristic of continuous mode operation with its 90 degree phase lag disappears. The current loop becomes more stable, but much less responsive. Fortunately, the high gain of current amplifier is sufficient to maintain acceptable closed current loop gain and phase characteristics at typical outer velocity and/or position loop crossover frequencies.

When the current loop is closed, the output voltage of the current sense amplifier ($2V_{RS}$) is equal to the current programming voltage (V_{CP}) at frequencies below the crossover frequency. The closed current loop transconductance is simply:

$$(9) \quad g_M = \frac{\Delta i_M}{\Delta V_{CP}} = \frac{\Delta V_{RS}/R_S}{\Delta V_{CP}} = \frac{1}{2R_S}$$

At the open loop crossover frequency, the transconductance rolls off and assumes a single pole characteristic. The input divider network attenuates the current command signal to provide compatibility with typical servo controller output voltages, and decreases the closed loop transconductance by the ratio of $R_{EQ}/(R_{EQ}+R_{IN})$. For the design example, the overall amplifier transconductance is 1.25 amps/volt, allowing full scale current (6 amps) with a 5 volt input command.

BIPOLAR TO SIGN/MAGNITUDE CONVERSION

The servo amplifier as shown in figure 6 requires a separate sign and magnitude input command. This is convenient for many microcontroller based systems which solely utilize digital signal processing for servo loop compensation. Analog compensation circuits however, usually output a bipolar signal and require conversion to sign/magnitude format to work with this amplifier. The circuit shown in figure 14 employs a differential amplifier for level shifting and ground noise rejection, and an absolute value circuit with polarity detection for conversion to sign/magnitude format. The current command signal is slightly attenuated and level shifted up 5 volts to allow single supply operation. The input divider circuit has been slightly modified from figure 9 to restore gain and provide a suitable offset adjustment range. Precision resistors (1%) should be used for both the differential amplifier and the absolute value circuit to minimize DC offset errors. Figure 15 shows approximately 2 Amp peak motor current with a 500 Hz sinwave command. Motor current follows the input command with minimal phase lag, however some crossover distortion is present. This is not crossover distortion in the traditional sense, rather it is simply a fixed off-time caused by the cross conduction protection circuitry. Since this distortion is current amplitude independent, and decreases with frequency, its effect on overall servo loop performance is minimal.

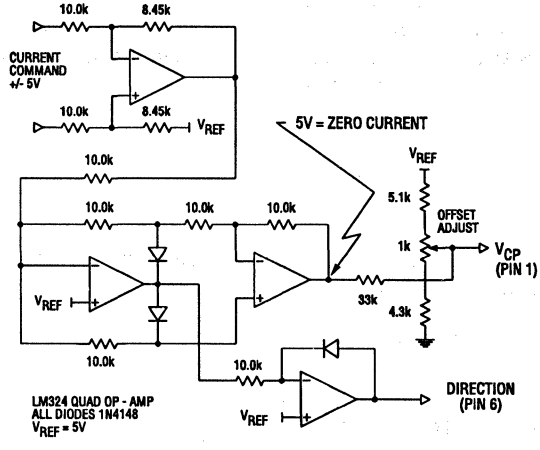

Figure 14 - Bipolar to Sign/Magnitude

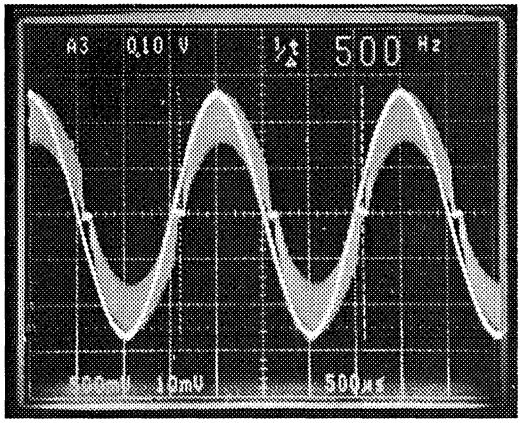

Figure 15 - 500Hz Sine Wave Command and Output Currents

DIRECT DUTY CYCLE CONTROL

There are many less demanding brushless DC servo applications which do not need a transconductance amplifier function yet require controlled operation in all four quadrants. For these systems, direct duty cycle control, also known as voltage mode control is often employed. Note that this is not voltage feedback, which requires additional demodulation circuitry to develop a feedback signal. With direct duty cycle control the amplifier simply provides open loop voltage gain. This technique is particularly advantageous when a microcontroller is used for servo loop compensation. By outputting a PWM signal directly, a digital to analog conversion is eliminated along with the analog pulse width modulator. While the simplicity of this technique is appealing, there are two major problems which must be addressed. The first and less severe problem is the complete lack of power supply rejection. Good supply filtering will often reduce transients to acceptable levels, while the servo loop compensates for slow disturbances. The second and more troublesome predicament is the output nonlinearity which occurs when transitioning between quadrants. This is best illustrated by examining the DC equations for the two possible cases.

When operating in either quadrant one or three, rotation and torque are in the same direction. Assuming operation is above the continuous/discontinuous current mode boundary, the output voltage is described by:

(10) $V_M = 2V_{PS}D - V_{PS}$

where D = PWM duty cycle

When the direction command is reversed while the motor is rotating, operation switches to quadrant two or four, shifting the modulator's maximum output voltage point from full duty cycle to zero duty cycle.

(11) $V_M = 2V_{PS}(1\text{-}D) - V_{PS}$

Note that the gain does not change, only the reference point has shifted. This occurs because the modulator only has a single quadrant control range - four quadrant operation results from the output control logic which is after the modulator. With the transconductance amplifier previously described, the error amplifier quickly slews during quadrant transitions, providing four quadrant control with minimal disturbance. When direct duty cycle control is used however, the servo loop filter must slew to maintain control. Unfortunately, this causes an immediate loop disturbance, with the greatest severity at the duty cycle extremes. This behavior can greatly effect the performance of an analog compensated servo, and therefore limits such systems to lower performance requirements.

With a microcontroller providing the servo loop compensation, nonlinear duty cycle changes can be accommodated, restoring linearity when transitioning between quadrants. Although nonlinear behavior still occurs when motor current becomes discontinuous, the effect on overall system performance is usually minimal. By correcting for quadrant transition nonlinearities, the advantages of an all digital interface can be exploited without severely degrading system performance. The control system is fully digital right up to the output stage, where the motor's inductance finally makes the conversion to analog by integrating the output switching waveform.

The circuit shown in figure 16 uses a PWM input from a microcontroller to set the output duty cycle and synchronize the oscillator, while another input controls direction.

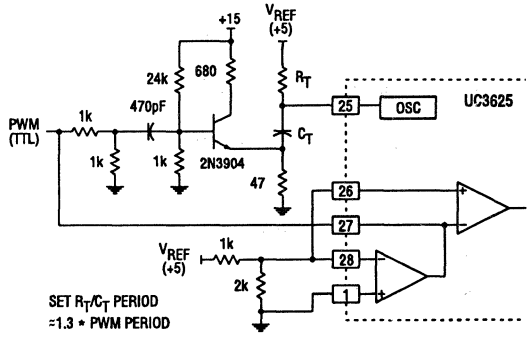

Figure 16 - Digital PWM Interface

Complete line isolation can easily be achieved by using opto-couplers. Although the performance of this technique falls short of the transconductance amplifier, the circuitry's simplicity while maintaining all of the protection features of the UC3625 make it well suited to many cost sensitive applications.

SUMMARY

The application example demonstrates the relative simplicity in implementing a brushless DC transconductance servo amplifier using the latest generation controller and driver ICs. For less demanding applications, direct duty cycle control using a dedicated controller provides size and cost reduction, without sacrificing protection features. While more and more control functions are implemented in microcontrollers today, the task of interfacing to output devices, and providing reliable protection under all conditions will remain a hardware function. Dedicated integrated circuits offer considerable improvement over the discrete solutions used in the past, reducing both size and cost, while enhancing reliability.

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APPLICATION NOTE

Simple Switchmode Lead-Acid Battery Charger

John A. O'Connor

Abstract

Lead-acid batteries are finding considerable use as both primary and backup power sources. For complete battery utilization, the charger circuit must charge the battery to full capacity, while minimizing over-charging for extended battery life. Since battery capacity varies with temperature, the charger must vary the amount of charge with temperature to realize maximum capacity and life. Simple, low cost circuits are currently available for small, low power requirements, while more complex solutions are affordable only on larger more expensive systems. Often the greatest challenge is in designing mid-size, mid-price systems, where obtaining optimum performance at moderate cost and complexity may be nearly impossible without dedicated integrated circuits. This paper describes a compact lead-acid battery charger, which achieves high efficiency at low cost by utilizing switchmode power circuitry, and provides high charging accuracy by employing a dedicated control IC. The circuit described can be easily adapted to lower or higher power applications.

Lead-Acid Basics

Lead-acid battery chargers typically have two tasks to accomplish. The first is to restore capacity, often as quickly as practical. The second is to maintain capacity by compensating for self discharge. In both instances optimum operation requires accurate sensing of battery voltage and temperature.

When a typical lead-acid cell is charged, lead sulfate is converted to lead on the battery's negative plate and lead dioxide on the positive plate. Over-charge reactions begin when the majority of lead sulfate has been converted, typically resulting in the generation of hydrogen and oxygen gas. At moderate charge rates most of the hydrogen and oxygen will recombine in sealed batteries. In unsealed batteries however, dehydration will occur.

The onset of over-charge can be detected by monitoring battery voltage. Figure 1 shows battery voltage verses percent of previous discharge capacity returned at various charge rates. Over charge reactions are indicated by the sharp rise in cell voltage. The point at which over-charge reactions begin is dependent on charge rate, and as charge rate is increased, the percentage of returned capacity at the onset of over-charge diminishes. For over-charge to coincide with 100% return of capacity, the charge rate must typically be less than C/100 (1/100 amps of its amp-hour capacity). At high charge rates, controlled over-charging is typically

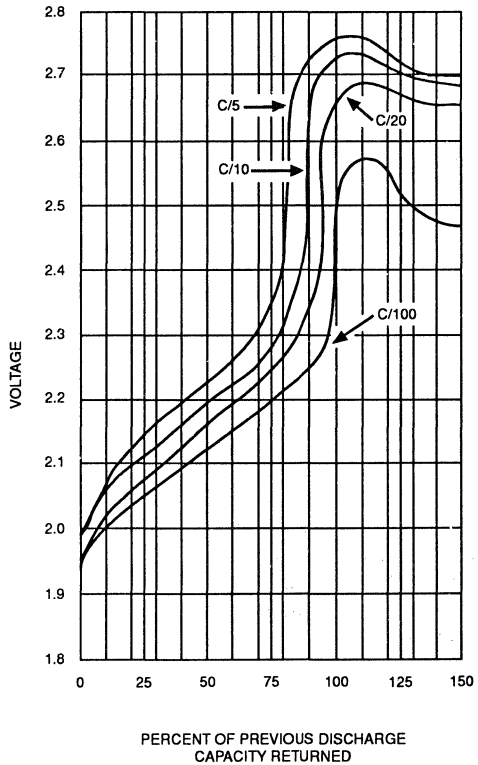

Figure 1. Over-charge reactions begin earlier (indicated by the sharp rise in cell voltage) when charge rate is increased. (Reprinted with the permission of Gates Energy Products, Inc.,)

9

employed with sealed batteries to return full capacity as quickly as possible.

To maintain capacity on a fully charged battery, a constant voltage is applied. The voltage must be high enough to compensate for self discharge, yet not too high as to cause excessive over-charging. While simply maintaining a fixed output voltage is a relatively simple function, the battery's temperature coefficient of -3.9mV/degree C per cell adds complication. If battery temperature is not compensated for, loss of capacity will occur below the nominal design temperature, and over-charging with degradation in life will occur at elevated temperature.

Charging Algorithm

To satisfy the aforementioned requirements and thus provide maximum battery capacity and life, a charging algorithm which breaks the charging cycle down into four states is employed. The charging algorithm is illustrated by the charger state diagram shown in figure 2. Assuming a fully discharged battery, the charger sequences through the states as follows:

1. Trickle-charge If the battery voltage is below a predetermined threshold, indicative of a very deep discharge or one or more shorted cells, a small trickle current is applied to bring the battery voltage up to a level corresponding to near zero capacity (typically 1.7V/cell @ 25 degrees C). Trickle charging at low battery voltages prevents the charger from delivering high currents into a short as well as reducing excessive out-gassing when a shorted cell is present. Note that as battery voltage increases, detection of a shorted cell becomes more difficult.

2. Bulk-charge Once the trickle-charge threshold is exceeded the charger transitions into the bulk-charge state. During this time full current is delivered to the battery and the majority of its capacity is restored.

3. Over-charge Controlled over charging follows bulk-charging to restore full capacity in a minimum amount of time. The over-charge voltage is dependent on the bulk-charge rate as illustrated by figure 1. Note that on unsealed batteries minimal over-charging should be employed to minimize out-gassing and subsequent dehydration. Initially overcharge current is the same as bulk-charge current. As the over-charge voltage is approached, the charge current diminishes. Over-charge is terminated when the current reduces to a low value, typically one-tenth the bulk charge rate.

4. Float-Charge To maintain full capacity a fixed voltage is applied to the battery. The charger will deliver whatever current is necessary to sustain the float voltage and compensate for leakage current. When a load is applied to the battery, the charger will supply the majority of the current up to the bulk-charge current level. It will remain in the float state until the battery voltage drops to 90% of the float voltage, at which point operation will revert to the bulk charge state.

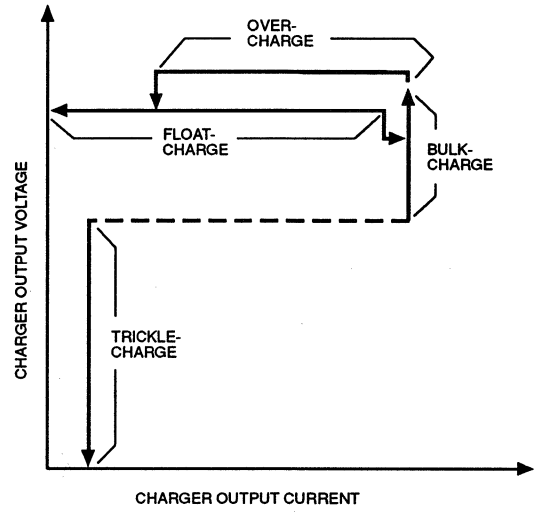

Figure 2. The charging algorithm is broken down into four states

Charger Circuit Design

There are many possible circuit configurations which will provide the necessary control and output charging current. For efficient operation, particularly at higher output currents, switching power circuitry is preferred. To minimize cost as well as complexity each IC used must provide as much functionality as possible. A circuit topology was chosen which utilizes two special purpose ICs and a general purpose op-amp to provide all of the control

functions, while a discrete MOSFET output stage handles the power. The circuit design is modular to simplify modification for different application requirements.

The charger circuit can be divided into three basic blocks. The first is the voltage loop control and state control logic which executes the control algorithm while providing temperature compensation. The second is the switchmode controller which regulates the current to the battery as commanded by the voltage loop control and state control logic. The third is the output power stage which is sized to efficiently deliver the charging current.

Voltage Loop Control and State Control Logic

Initially designed for charging small lead-acid batteries using a linear pass transistor for current control, the UC3906 directly implements the voltage loop control and state control logic while providing the appropriate temperature compensation. The block diagram of the UC3906 is shown in figure 3.

Battery voltage is monitored with a resistor divider string. This network establishes the float voltage, the over-charge voltage, and the trickle-charge threshold voltage by comparing to the precision temperature compensated reference. Since temperature is monitored on chip it is critical that the battery and the UC3906 are in close proximity, and

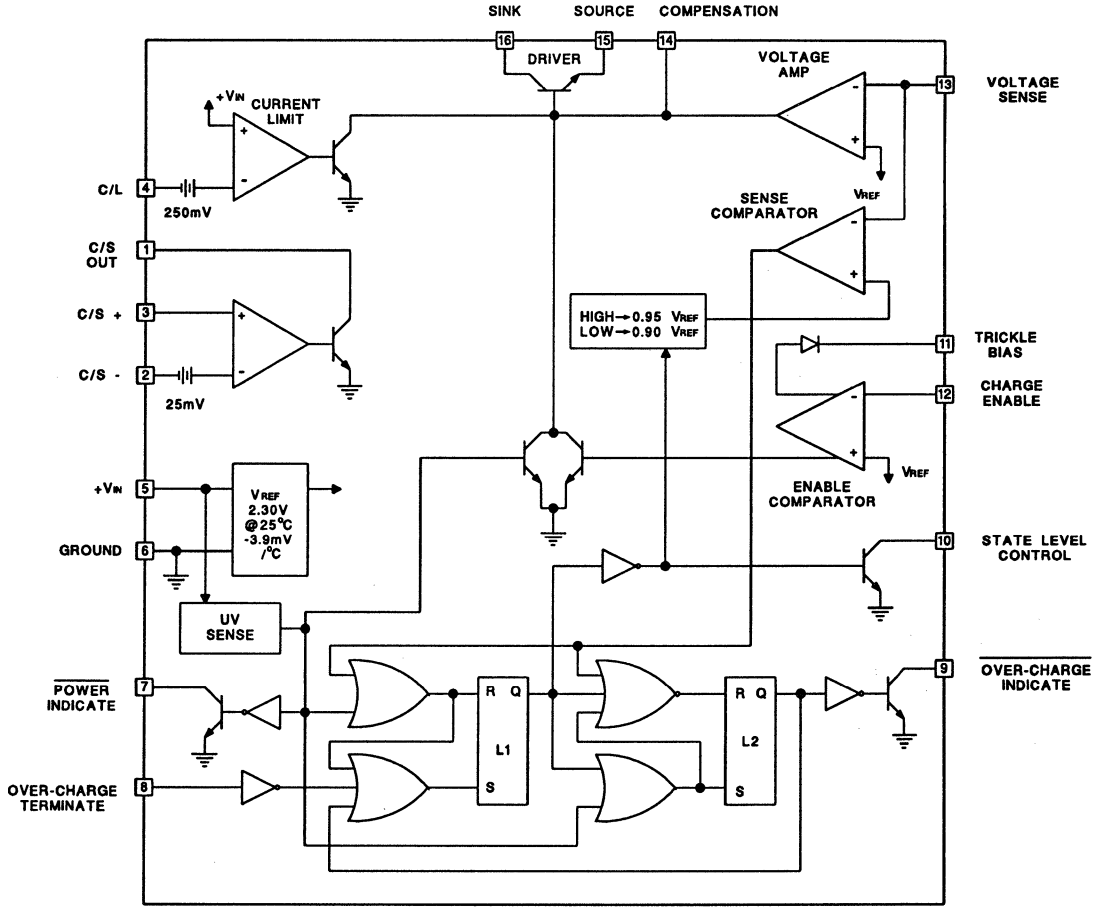

Figure 3. UC3906 Lead-Acid Battery Charger block diagram

that self-heating or heating from other components is minimized.

The differential current sense comparator is used to terminate over-charging and transition to the float state. The voltage amplifier provides gain and compensation for the voltage loop. The UC3906 is covered in detail in reference [3].

Switchmode Current Source

The charging algorithm places great demands on the current loop. during bulk charge full current must be supplied, yet during the float state the current draw may be only a few milliamps. This equates to a dynamic range in excess of 60 dB which can be very difficult to achieve with common peak current mode techniques. The wide dynamic range also requires operation with both continuous and discontinuous inductor current, potentially adding complication to voltage loop stabilization. Although load resistors can be employed to reduce the required dynamic range, their use can significantly degrade efficiency, particularly while in the float state. Note that a high value load resistor (10 k) is employed to assure operation down to zero output current and to provide a discharge path for the output capacitor. Additionally, to provide precise bulk and trickle-charge current levels the closed current loop transconductance must be accurate. Average current feedback will circumvent these potential problems, and is the key to a successful implementation of the switching current source for this application.

Figure 4 shows the basic implementation of average current feedback. While slightly more complicated than typical peak current mode control schemes, average current feedback offers several critical performance enhancements. The high gain of the error amplifier at lower frequencies provides high closed current loop accuracy and accommodates the large output stage nonlinearity which occurs when the inductor current becomes discontinuous. Good switching spike noise immunity is inherent with this technique permitting stable operation at narrow duty cycles.

A UC3823 PWM controller shown in figure 5 was chosen for the current loop control circuit for several reasons. First and most importantly it is capable of operating linearly from very small duty cycles to near

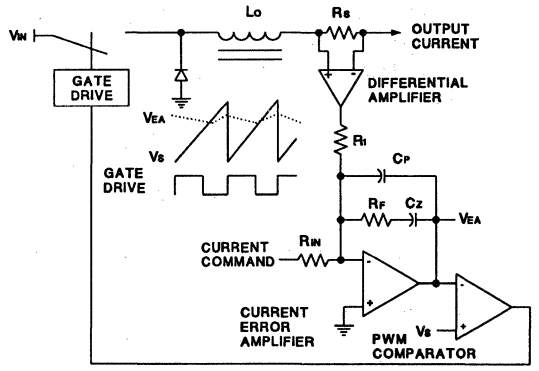

Figure 4. Average Current Feedback Loop

100% duty cycle. Secondly the error amplifier bandwidth and configuration are well suited to the average current loop's requirements. Additionally, the output driver affords a simple interface to most discrete output power stages.

A separate op-amp configured as a differential amplifier senses the output current and level shifts the signal to the appropriate voltage. The offset and common mode rejection of this amplifier are the major source of current loop error.

Output Power Stage

To simplify development a simple buck regulator output stage was used. For further simplicity the high-side switch is implemented using a direct coupled P-channel MOSFET. A switched current sink provides gate charge, turning the MOSFET on while a zener diode limits the gate to source voltage to 12 volts. A second emitter switched current sink drives a PNP which removes gate charge, turning the MOSFET off. Undoubtedly this output stage is suitable for many applications, although higher power capability and efficiency can be achieved using N-channel devices. A relatively low value output inductor was chosen to minimize size and cost since operation in the discontinuous current mode is of no concern with average current feedback. Output ripple voltage is also not critical so the output capacitor was selected for ripple current capability. High frequency ringing caused by circuit parasitics is damped with a small RC snubber across the catch rectifier. A rectifier in series with the output

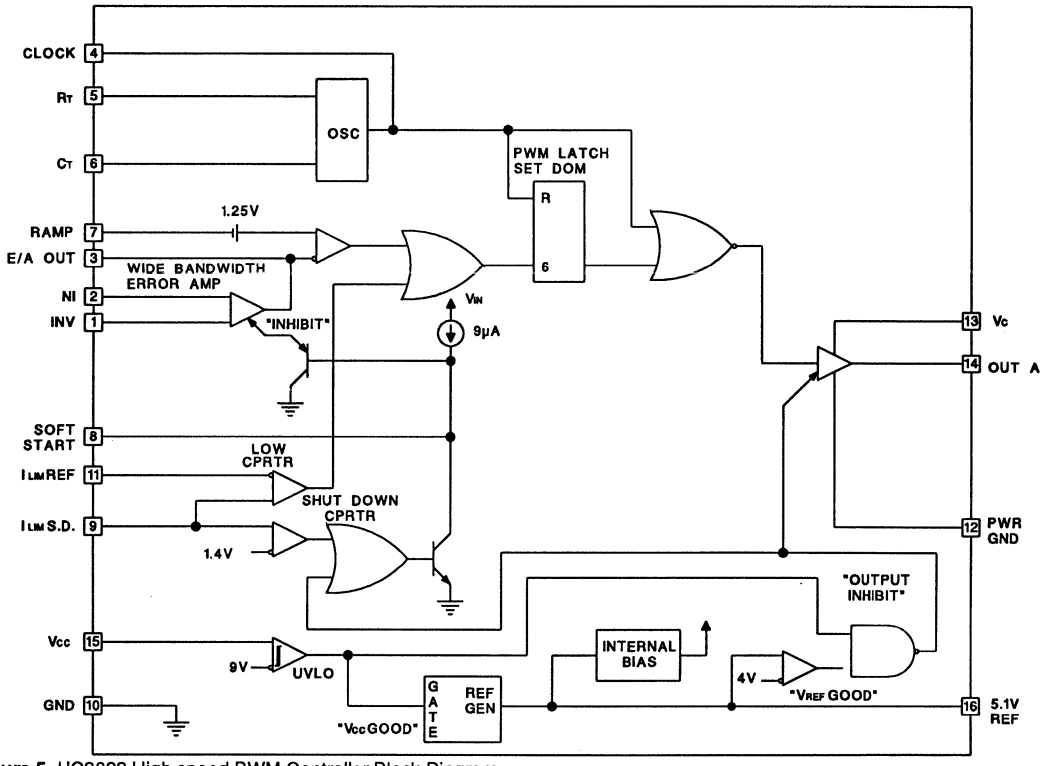

Figure 5. UC3823 High speed PWM Controller Block Diagram

prevents the battery from back driving the charger when input power is disconnected.

Complete Charger Circuit

A complete schematic for the switch-mode charger is shown in figure 6. Control circuit power is supplied from an emitter follower off a zener shunt regulator. The PWM frequency is set to 100 kHz as a reasonable compromise between output filter component size and switching loss. Output current is sensed in the battery return lead to minimize common mode voltage errors. This arrangement also allows direct current sensing for pulse by pulse current limiting adding further protection during abnormal conditions. The differential amplifier is set to a gain of 5 with the output signal referenced to the UC3823s 5.1V reference.

The current feedback signal is summed with the current command signal at the error amplifier's inverting input. To accommodate worst case offset in both the error amplifier and the differential amplifier and allow zero output current, the non-inverting input of the error amplifier is biased 130 mV below the 5.1 V reference. Trickle bias is accomplished by injecting a small current into the differential amplifier's negative op-amp input, thus causing a proportional output current to balance the loop. Additionally, a 100 pF capacitor across the PWM comparator inputs enhances noise immunity, particularly at low duty cycles.

For maximum control and float voltage accuracy, the UC3906s ground is connected to the battery's negative terminal, thereby rejecting the current sense resistors voltage drop. The internal emitter follower output transistor interfaces to the current source as illustrated in figure 7. The voltage amplifier drives the output current command signal. The current command signal is limited by clamping the voltage amplifier output through a diode to 4.2 V. The clamp also prevents the emitter follower from

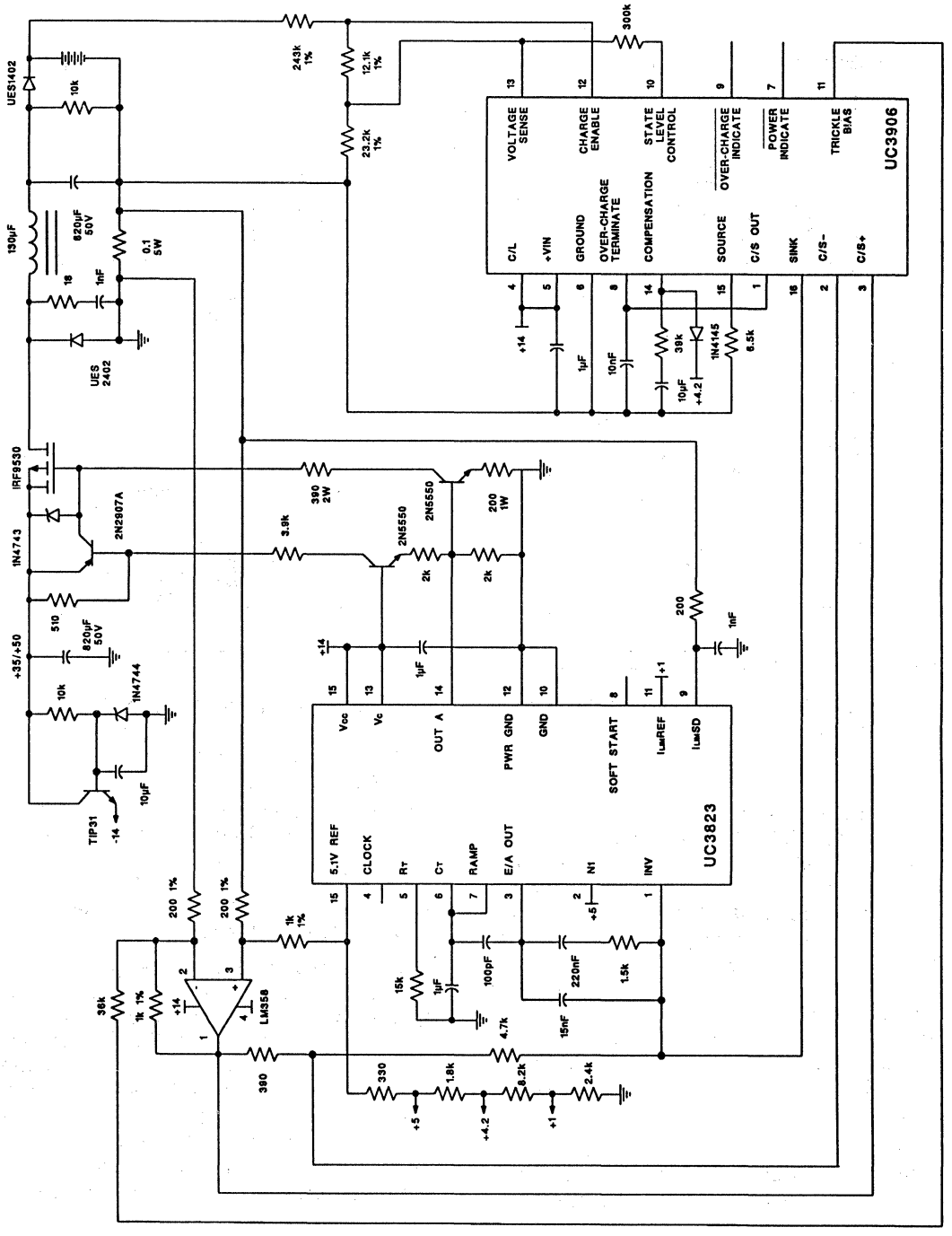

Figure 6. Switchmode Lead-Acid Battery charger schematic

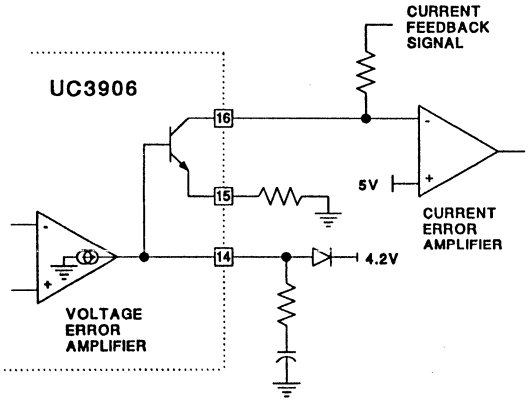

Figure 7. The UC3906's output transistor provides the interface to the switchmode current source.

saturating which would cause a large difference between collector and emitter currents due to excessive base drive.

Battery voltage is sensed by the resistor divider string, with the values shown for a typical 24 V (12 cell) application. Other battery voltages are easily accommodated by simply changing the divider values using the procedure presented in the UC3906 data sheet, although changes in input voltage may require modification of the output circuit and the control circuit power supply. The resistor divider establishes all of the state transitions with the exception of over-charge terminate, which is determined by detecting when the output current has tapered off to approximately one-tenth the bulk charge level. This is accomplished by the UC3906s current sense comparator which senses the appropriately scaled signal from the differential amplifier output.

Current and Voltage Loop Compensation

The charger circuit implements a two loop control system with the current loop operating inside the voltage loop. During trickle-charge, bulk-charge and the beginning of over-charge the voltage loop is saturated and the current loop is essentially driven from a fixed reference.

With continuous inductor current the control to output gain of the current loop shown in figure 4 exhibits a single pole response from the output inductor. The error amplifier gain at the switching frequency is set such that the amplified inductor current down-slope is less than the oscillator-ramp up-slope as seen by the PWM comparator. By setting the two slopes equal under worst case conditions (at maximum output voltage) maximum closed loop bandwidth is achieved without subharmonic oscillation.

Placing a zero below the minimum loop crossover frequency significantly boosts low frequency gain while a pole placed above the maximum crossover frequency enhances noise immunity. Note that since loop response is not particularly critical for battery charging, conservative compensation with plenty of phase margin is normally employed.

When inductor current becomes discontinuous, the power circuit gain suddenly drops, requiring large duty cycle changes to significantly effect output current. The single pole characteristic of continuous inductor current with its 90 degree phase lag disappears. The current loop becomes more stable, but less responsive. Fortunately the high gain of the error amplifier easily provides the large duty cycle changes necessary to accommodate changes in output current, thereby maintaining good average current regulation.

The block diagram of the voltage loop is shown in figure 8. With an inner transconductance loop the control to output gain of the voltage loop exhibits a single pole response from the output capacitor and equivalent load resistance. While it may initially appear that a simple fixed gain on the voltage amplifier would provide suitable loop compensation, further examination shows a severe drop in voltage gain at high loads, which would drastically reduce DC accuracy. A zero is placed in the voltage amplifier's transfer function to boost low frequency gain and therefore restore DC accuracy.

The current loop's single pole response above its crossover frequency cancels the output stage zero resulting from the output capacitor's capacitance and ESR. Note again that since wide bandwidth is not required for battery charging, the voltage loop crossover frequency is well below both the current loop's pole and the output capacitor's zero. Low leakage capacitors must be used for the compensation network to maintain high DC gain

since the voltage amplifier is a transconductance type. Loop stabilization is covered extensively in references [1] and [2].

Charger Performance Summary

The charger circuit properly executes the charging algorithm, exhibiting stable operation regardless of battery conditions including an open circuit load. The circuit was tested with 6,12 and 24 V batteries by modifying only the battery voltage sense divider. As would be expected, circuit efficiency was best at high battery voltage, approaching 85% while bulk-charging a 24 V battery with a 40 V input supply voltage.

An analysis of circuit losses indicates several areas where efficiency could be improved. Any accuracy and offset improvement in the differential amplifier will allow a corresponding decrease in current sense resistor value and hence dissipation, while maintaining the same overall current loop accuracy. Replacing the output blocking rectifier with a Schottky would save a few watts if the Schottky's leakage could be tolerated. Further improvement could be made in that area by using a relay to disconnect the charger when input power is removed. A more conservative inductor design with less resistance would save a little over one watt. As expected, the greatest losses occur in the output switch. A lower on resistance FET and a higher peak current gate drive to reduce switching losses could save more than 5 watts. Incorporating a few of these improvements will easily increase circuit efficiency to greater than 90%.

Alternate Circuit Configurations

While the charger circuit as designed may be suitable for many applications, a few modifications should satisfy the majority of additional requirements. Higher voltage batteries can be charged by designing a higher voltage output stage. N-channel MOSFETs are preferable for cost and efficiency reasons, but are more difficult to drive than P-channels. Fortunately, the remainder of the circuit will require minimal modification.

Some applications may require both the battery and charger to share a common ground and thus prohibit current sensing in the batteries negative return. The differential amplifier can sense current at the inductor output if tighter tolerance resistors to improve CMRR are used. While this simple modification renders a suitable signal for closing the current loop, another current sense signal referenced to ground must be developed for pulse by pulse current limiting. This signal is most easily derived by using a PNP level shift transistor, connecting the base to the 5.1 V reference and the emitter through a resistor to the differential amplifier output.

At higher battery voltages it may be desirable to float with a current rather than a voltage. Varying self-discharge rates of individual cells in high voltage batteries causes inevitable differences in cell charge levels. By employing a float current and applying a small continuous overcharge, variation of charge between cells is minimized. Precise output at float current levels places great demands on current loop accuracy, and will add unnecessary expense to the current sensing circuitry. A more cost effective alternative is to use a fixed linear current source which should be small and inexpensive considering the very low output current.

Thus far the input supply has not been addressed and is assumed to be from a voltage required elsewhere in the system or from a typical line frequency transformer, rectify bridge and filter capacitor. This may represent more than half the cost of the charger, and is certainly the majority of its size and weight. An obvious alternative is to replace the buck output section with a transformer coupled output, taking advantage of the switching control circuit already present. Buck derived circuits such as forward, half-bridge and full-bridge easily interface with the existing design, however resonant and flyback circuits are also applicable. A small (0.75 W) auxiliary supply will be required to power the control circuitry since the modulator will output zero at times, prohibiting the use of a bootstrap winding commonly used on switching power supplies. This

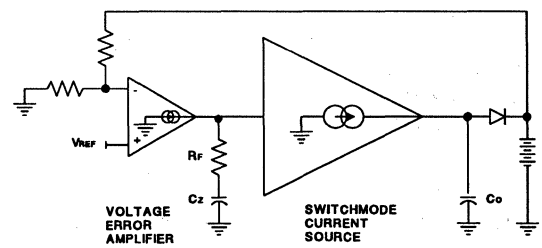

Figure 8. Voltage Control Loop block diagram

approach is particularly cost effective for stand-alone applications, allowing the design of a compact, light weight, high performance charger.

Summary

A practical switchmode lead acid battery charger circuit has been presented which incorporates all of the features necessary to assure long battery life with rapid charging capability. By utilizing special function ICs, component count is minimized, reducing system cost and complexity. With the circuit as presented, or with its many possible variations, designers need no longer compromise charging performance and battery life to achieve a cost effective system.

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POWER FACTOR CORRECTION USING THE UC3852 CONTROLLED ON-TIME ZERO CURRENT SWITCHING TECHNIQUE

BILL ANDREYCAK

INTRODUCTION

The controlled on-time, zero current switching technique provides a simple and efficient solution to obtaining high power factor correction. This discontinuous inductor current approach essentially programs a constant switch on-time during one line half-cycle. It does not require any "complex" analog square, multiply and divide functions to control the instantaneous switch current as with other PFC techniques. Additionally, zero current switching limits the peak current to exactly twice that of the average inductor current over all line and load combinations. High efficiency operation is also achieved with no boost rectifier recovery concerns and power loss. In a typical 80 Watt application the UC3852 PFC technique delivers a power factor of 0.998 with 5.8% Total Harmonic Distortion at nearly 94% efficiency.

CIRCUIT SCHEMATIC

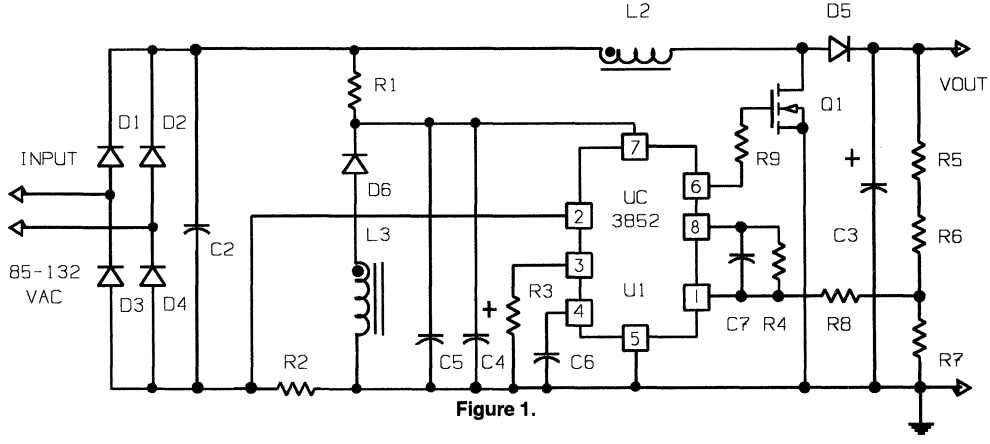


Figure 1.

UC3852 FEATURES

The UC3852 PFC controller contains several features which minimize external parts count while providing excellent performance and protection. Optimized for this off-line PFC application, the UC3852 delivers high power factor (0.997 typical) and a low cost overall solution.

OFF-LINE PROTECTION

- undervoltage lockout with hysteresis 16V turn-on, 11 V turn-off [1]
- clamped 12V gate drive output [2]
- active low, self biasing output [3]
- overcurrent protection [4]

CONTROL CIRCUIT ATTRIBUTES

- programmable maximum frequency [5]
- programmable maximum on-time [6]
- overcurrent indication output [7]

OPERATIONAL CHARACTERISTICS

- low operating current [8]
- low start-up current (0.4 mA) [1]
- few external required components
- 30 V maximum supply input

CONTROL TECHNIQUE

- Zero Current Switching [9]
- controlled on-time [6]
- high noise immunity [6]

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

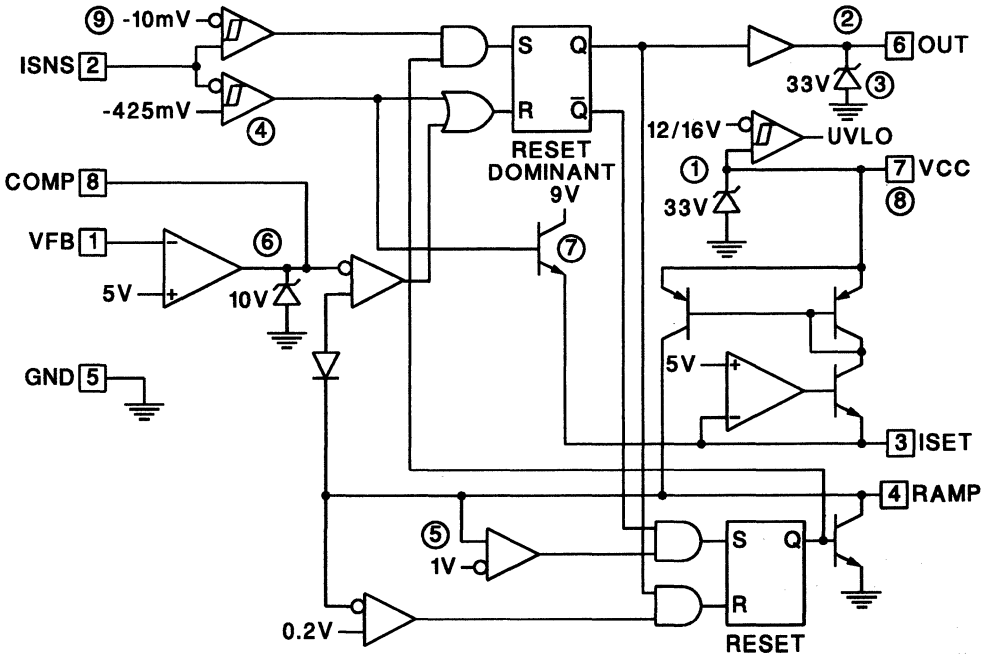


Figure 2.

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

PFC TECHNIQUE OVERVIEW

Most power factor correction techniques incorporate the boost topology which can be operated in either the continuous or discontinuous inductor current modes and switched at a fixed or variable frequency. Generally, the fixed frequency, continuous inductor current variety is preferred for higher power applications to minimize the peak current. Below about 500 Watts, the discontinuous inductor current version operated in a variable frequency mode offers several advantages. Benefits include reduced inductor size, minimal parts count and low cost of implementation. This paper will highlight the controlled on-time, zero current switched variety of discontinuous inductor current PFC operation.

FUNDAMENTALS

CONTROLLED ON-TIME

On-time of the PFC switch is controlled by the voltage error amplifier of the UC3852 which is compared to a sawtooth waveform generated at the ICs RAMP function at pin 4. The PFC switch on-time varies with line and load conditions but should be considered constant for one line half-cycle. A low frequency bandwidth is necessary in the voltage error amplifier loop compensation which is typically rolled off to cross zero dB below the line frequency.

ZERO CURRENT SWITCHING

Zero current switching facilitates three important advantages in this application. First, the inductor current must be zero before the next switching cycle is initiated inferring high efficiency and elimination of the boost rectifier recovery loss. Secondly, the change in inductor current (delta IL) is equal to the peak inductor current (IL(pk)) since current starts and returns to zero each cycle. The discontinuous boost converter current waveform has a triangular shape with an area (charge) equal to one-half of the product of its height (peak current) multiplied by its base (time). Since the timebase can be considered as a series of consecutive triangles, the peak current is therefore limited to exactly twice that of the average current. This is valid for both the steady state and instantaneous switching cycle relationships. The converter operates right on the border between continuous and discontinuous current modes which results in variable frequency operation.

The "fixed" on-time in conjunction with zero current switching provide automatic power factor correction of the input current. This can be demonstrated by analyzing the basic inductor waveform using specific attributes of this PFC technique for either charging and discharging of the inductor current. Since the inductor charging condition is being controlled by the UC3852 circuitry it will be used for the analysis.

INDUCTOR WAVEFORM

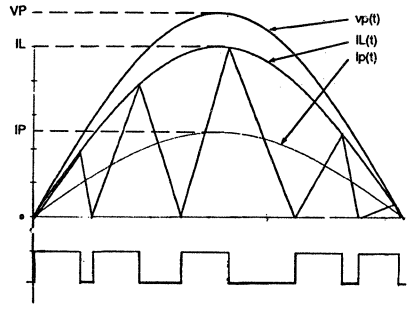


Figure 3.

$$1.\ \frac{V}{L} = \frac{dI}{dt}$$

For the PFC boost converter operation, V can be replaced by Vin(t), the instantaneous voltage across the inductor. Also, it is assumed that the inductance and the switch on-time is constant for the duration of one line-half cycle. The change in inductor current, delta I is actually the peak value of current (Ipk(t)) since the inductor always begins charging at zero current, as forced by zero current switching. Substituting these relationships into the inductor wave from equation will demonstrate the simplicity of this specific technique when used for power factor correction.

V = Vin(t)

L = constant

dI = Ipk(t)

dt = constant

2. $Ipk(t) \propto Vin(t)$

This relationship demonstrates that the instantaneous line current will exactly track that of the instantaneous line voltage. Since the input voltage waveform is sinusoidal (Vin sin(wt)), then so is the input current (Ipk sin (wt)). This controlled on-time, zero current switched technique provides automatic power factor correction with very simple control circuitry.

PFC POWER STAGE DESIGN

It is advantageous to begin the power relationships from the AC line input of the preregulator and work towards the DC output section. The instantaneous primary voltage (Vp(t)) is related to the steady state peak input (VP) by the following relationship:

3. $VP(t) = VP \sin(wt)$

where $VP = \sqrt{2} \times Vp(rms)$

The amplitude of Vp(t) varies between zero and VP as sin(wt) goes from zero to one for one line half-cycle. Note that Vp(t) and VP are always positive with respect to the PFC circuit common due to the bridge rectification of the AC input waveform. The input current can similarly be expressed as :

4. $IP(t) = IP \sin(wt)$

where $IP = \sqrt{2} \times Ip(rms)$}

Input power to the PFC converter is the Root Means Squared (RMS) component of the line voltage (Vp(RMS)) multiplied by the line current (Ip(RMS)). This can also be expressed using the peak terms of each waveform which is simpler for this application.

5. $Pin = \frac{VP}{\sqrt{2}} \times \frac{IP}{\sqrt{2}}$

$$Pin = \frac{(VP \times IP)}{2}$$

The average DC output current (Io) is determined by dividing the output power (Po) by the output voltage (Vo).

6. $Po = \frac{Vo}{Io}$

Converter efficiency (n) can also be factored into the design equations although it may typically be in the neighborhood of 94% at full load.

7. $Pin = \frac{Po}{n}$

or $Po = Pin \times n$

where $Pin = \frac{(VP \times IP)}{2}$

7A. $Po = \frac{(VP \times IP \times n)}{2}$

Equation 7A. can expressed with regard to primary current.

7B. $IP = \frac{(2 \times Po)}{(VP \times n)}$

It has been already established that the peak inductor current is exactly twice that of the average inductor current due to zero current switching.

8. $IL(pk) = 2 \times IL(avg)$

The average input current must be equal to the average inductor current since they are in series.

9. $Ipri(avg) = IL(avg)$

Combining equations yields the peak inductor current to the input current.

10. $Ipri(pk) = \frac{(4 \times Po)}{(VP \times n)}$

The inductor current can now be analyzed in its time variant form and over all line and load conditions.

11. $IL(t) = \frac{(4 \times Po \times \sin(wt))}{(VP \times n)}$

TIMING RELATIONSHIPS

Steady state conditions will be used to analyze the timing relationships of this controlled on-time PFC technique. The peak primary voltage (VP) will be used as the starting point for the calculations, so the input line must be specified.

The inductor relationship of equation 1. will be solved for the specific on-time required to charge the inductor to the correct peak current. This equation can be restated for a given set of operating conditions as:

12. $t(on) = IL(pk) \times \frac{L}{VP}$

Substituting equation 10. for IL(pk) into equation 12 results in:

12A. $t(on) = \frac{(4 \times Po \times L)}{(VP^2 \times n)}$

The instantaneous switch off-time varies not only with the line and load conditions, but also with the instantaneous line voltage. Off-time is analyzed by solving equation 1. for the inductor discharging where the voltage across the inductor is Vout minus Vin. This should be solved for the time required to discharge the current from its instantaneous peak to zero, which can be expressed as:

13. $t(off) = \frac{(IL(pk) \times L)}{(Vo - VP(\sin(wt)))}$

Substituting equation 10. for IL(pk) above will expand the off-time equation to:

13A. $t(off) = \frac{(4 \times Po \times L \times \sin(wt))}{VP \times (Vo - (VP \times \sin(wt)))}$

Due to the high efficiency during the boost inductor discharge and lack of rectifier recovery losses, the efficiency term (n) is essentially one. Loss can be ignored during the off-time since the boost diode forward voltage drop is very small in comparison to

9

the high voltage DC output, and resistive losses at these lower powers and currents are minimal.

CONVERSION PERIOD

The total time for one switching cycle is obtained by adding the on-time with the instantaneous off-time. Switching frequency is the reciprocal of the cyclical switching period which varies with line, load and instantaneous line voltage.

14. $t(per) = t(on) + t(off)$

$$t(per) = 4 \times Po \times L \times \frac{1}{VP^2} + \frac{\sin(wt)}{VP \times [Vo - VP\sin(wt)]}$$

SWITCHING FREQUENCY

15. $f(conv) = 1 / t(per)$

Switching frequency varies with the steady state line and load operating conditions along with the instantaneous input line voltage. Generally, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. Many applications can use thirty kiloHertz (30 kHz) as a good first approximation. Higher frequency operation should also be evaluated as this can significantly reduce the inductor size without negatively impacting efficiency or cost. In most applications, the minimum switching frequency will coincide with full load operation during the peak of the input voltage waveform at low line. In contrast, the highest frequency conversion occurs at light load and high line conditions, just as the input voltage waveform nears the zero crossing point. A plot of t(on), t(off), t(per) and switching frequency versus instantaneous line voltage is shown in figure 4 and for the specific application circuit of figure 1. Figure 5 demonstrates the typical changes incurred in conversion frequency from low to high line inputs.

SELECTING THE OUTPUT VOLTAGE

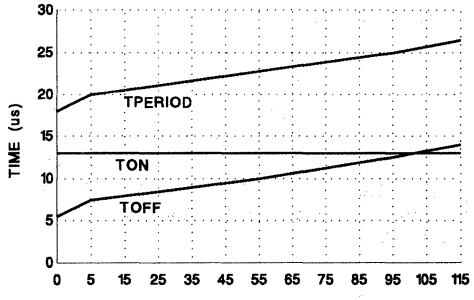
The boost converter output voltage should be designed to be at least thirty volts higher than the peak of the input voltage at high line. This will prevent long conversion cycles due to the small voltage across the discharging boost inductor. When this thirty volt margin is ignored, the minimum switching frequency will occur at the peak of high line operation and not at low line, but also at full load. This will require recalculation of the timing intervals.

INDUCTOR CONSIDERATIONS

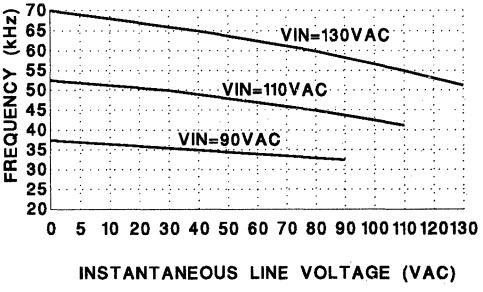
The exact inductor value can determined by solving equation 14 for the required inductance at the selected minimum operating frequency. Maximum on-time needs to be programmed into the UC3852 timing circuit. Both t(on)max and t(off)max will be individually calculated and added together to obtain the maximum conversion period, t(per)max. This is required to obtain the inductor value. Equations 12A and 13A will be solved for their respective maximums.

$$12B.\ t(on)\ max = \frac{4 \times L \times Po\ (max)}{VP\ (min)^2}$$

$$13B.\ t(off)\ max = \frac{4 \times L \times Po\ (max)}{[VP\ (min) \times (Vo - VP\ (min)]}$$



Conversion Times vs Instantaneous Line Nominal Line Voltage
Fig. 4



Conversion Frequency vs Instantaneous Line
Fig. 5.

14A. $t(per)max = t(on)max + t(off)max$

The minimum conversion frequency (F(conv)min) corresponds to the reciprocal of the maximum conversion period, t(per)max.

15A. $F(conv)min = 1 / t(per)max$

INDUCTOR VALUE

The inductance value necessary for an application can be obtained by substituting equations 12B and 13B into 15A. using the relationship of 14A.

$$16A.\ L = \frac{VP\ (min)^2 \times [Vo - VP\ (min)]}{4 \times Po\ (max) \times Vo \times F\ (conv)\ min}$$

This equation provides insight as to the possible ways to reduce the inductor value (size and cost) for a given set of design specifications. The most obvious approach is to increase the minimum conversion frequency above thirty kiloHertz if none of the other parameters (Vo, Po) can be varied.

INDUCTOR DESIGN SUMMARY

Generally, the size and cost of an inductor vary with its energy storage capacity, W(L). Although most of the energy is stored in the air gap (with a gapped ferrite design), the core set must support the necessary flux density (B)without saturating or exhibiting high core loss. The required energy storage of the boost inductor is:

17. W(L) = 0.5*L*IL(pk)^2

The number of turns required for a selected core size and material is:

18. N = L*IL(pk)*10^4 / (Bmax*Ae)

where Bmax is in Teslas and Ae is in square centimeters (cm^2)

The center leg gap to achieve the correct

inductance and storage is expressed by:

19. l(gap)={Uo*Ur*N^2*Ae*10^-2}/L (cm)

where Uo=4*Pi*10^-7 (permitivity of free space), and Ur=1 (relative permeability of air)

OUTPUT CAPACITOR

The value of output capacitance is a generally determined by the required hold-up time or the acceptable output ripple voltage for a given application. It may also be governed by the specified ripple current rating or capacitor temperature rise. Typically, an approximation of one microFarad per Watt (1uF/W) is a good starting point. The exact value can later be changed depending on conversion frequency and other factors previously mentioned.

Electrolytic capacitors are typically used near 80% of their working voltage. This will necessitate a 500 VDC rating for use in a 264 VAC PFC application which may not be practical from a cost perspective. One option is to connect two lower voltage capacitors in series, each having the same value and a 250VDC rating.

SEMICONDUCTOR SELECTION

Peak currents and voltages must first be known over all operating conditions to select the proper MOSFET switch and boost rectifier. Standard design practice is to derate all semiconductors to about 75% of their maximum ratings, indicating the use of 500+ volt devices.

Low cost bipolar transistors are an acceptable alternative to MOSFETs if the conversion frequency is maintained fairly low. Inexpensive high voltage diodes with recovery times of 200 nanoseconds, or less should be used for the boost rectifier. Two popular devices are the 1N4937 and MUR160. Speed is not an issue with the input bridge rectifiers where 1N4004 to 1N4006 types are acceptable. High frequency switching noise in the PFC converter should be well filtered before reaching the input bridge diodes due to their low speed characteristics. This is best accomplished by adding an L/C filter between the bridge rectifier DC output and the boost converter.

CONTROL CIRCUIT DESIGN :

PROGRAMMING THE UC3852

STARTUP CIRCUITRY

The UC3852 design incorporates a low startup current feature and draws less than one milliamp (mA) from the Vcc bias supply. This minimizes the power loss due to with the startup resistor after the converter begins operation when a bootstrap winding supplies the full DC supply current. The UC3852 IC turns on when Vcc reaches approximately 16 volts, and IC supply current will increase to its operational level. Undervoltage lockout protection will turn the UC3852 device off when the supply voltage falls below the lower UVLO threshold of approximately 10 volts.

The startup circuitry for this off-line consists of a startup resistor from Vcc to the input supply voltage and a storage capacitor from Vcc to ground. Typically, select Rstart to supply around 1.5 milliamps (rms) of charging current (I(charge) at low line. The exact value can be obtained from the following approximations.

$$R(start) = \frac{VP(min) - V(turn\text{-}on)}{1.41 \times I(charge)}$$

The Vcc bias supply filter capacitor value is determined by several factors, but primarily by the UC3852 undervoltage lockout hysteresis. Implementation and phasing of this boost inductor winding in addition to soft start circuitry will also effect the capacitance.

$$C(Vcc) = \frac{(ICC - I(charge) \times t(boot)}{UVLO\ hysteresis}$$

For many applications, the following approximations can be used:

ICC = 10 mA

I(charge) = 1.5 mA

t(boot) = 10 ms (one-half cycle at 50 Hz)

UVLO hysteresis = 5 volts

V(turn-on) = 15V

A standard 15 uF electrolytic with an adequate voltage rating (35V once derated) is used.

PROGRAMMING THE ON-TIME

The maximum switch on-time must be calculated to program the UC3852 oscillator. This maximum occurs when the line voltage, VP is at its minimum and the output power is at its maximum. This is more commonly known as the low line, full load condition.

t(on)max = 4*Pout(max)*L / Vp(min)^2

The UC3852 on-time is programmed by R/C components and uses two of the IC pins. A resistor from the ISET pin to ground programs the charging current into the RAMP pin. The Iset pin has an output voltage of approximately 5 volts, so the ISET is 5 volts divided by Rset. Typical charging current should range between 100 and 600 microamps.

The RAMP pin is used as one input to the Pulse Width Modulator of the UC3852. Internally, the RAMP voltage is compared to the error amplifier output (COMP) voltage to determine the exact on-time. The RAMP pin has a maximum amplitude of approximately 9 volts, and begins charging from approximately 0.2 volts, or an 8.8 volt swing.

The RAMP capacitor value is selected to program the maximum switch on-time as it charges from 0.2 to 9 volts by Iset. It can be calculated from the capacitor charge equation, shown below.

C = (I * dt) / dV

C(RAMP) = [Iset * t(on)max] / 8.8 V

The RAMP capacitor should be selected first from a list of standard values within the 100pF to 1nF range. The resulting ISET programming resistor selection is much easier as standard values with an initial tolerance of one percent (1%) are readily available.

$$RSET = \frac{5 \times t(on)max}{8.8 \times C(RAMP)}$$

or

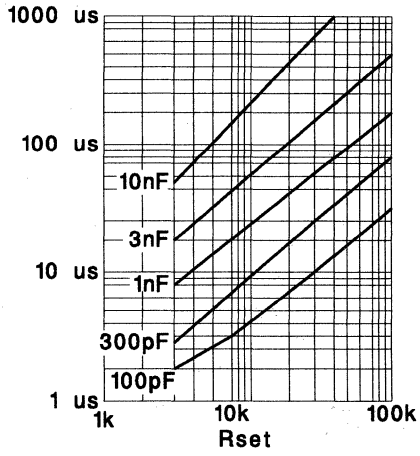
RSET = 0.568 * t(on)max / C(RAMP)

t(on)max = [RSET*C(RAMP)] / 0.568

UC3852 ON-TIME vs. RSET & C(RAMP)

ERROR AMPLIFIER COMPENSATION

Power Factor Correction using the ZCS controlled on-time technique requires a very low bandwidth voltage loop to deliver high power factor (). This is necessary to keep the switch on-time constant during any one line cycle. Other advantages to this approach are high noise immunity, and simplicity,



Max On-Time vs Rset and Ct
Fig. 6

since no squarer, multiply or divide circuitry is needed.

Configuration of the compensation circuitry is shown in the UC3852 PFC application schematic. First, the PFC preregulator output voltage (Vout) is accurately divided down to 5.0 volts to interface with the error amplifier. Three standard one-half watt resistors are used to avoid needing more expensive, high voltage rated resistors for this application. This signal goes through a 20K ohm input resistor to the error amplifier inverting input. Feedback components are a 1 meg ohm resistor and a 0.1 uF capacitor in parallel from the E/A output to the inverting input.

This recommended amplifier compensation delivers one low frequency pole in the loop response at 1.6 Hz, as programmed by 1 meg ohm and 0.1 uF components. Low frequency gain is determined by the 20 K ohm input resistor, the output voltage divider resistance and the 5.0 reference voltage seen at the amplifiers (internal) noninverting input.

Many other compensation arrangements are possible.

Using this compensation network, a low frequency gain of approximately 34 dB is achieved. This rolls off with a single pole (-20 dB/decade) response centering at 1.6 Hz. The gain curve will intersect zero dB at about 120 Hz and result in excellent power factor correction. Better dynamic response and less overshoot of the output voltage can be obtained by adjusting the 20 K ohm input resistor to increase low frequency gain and move the zero dB crossing out to a higher frequency. Some slight degradation of the power factor is to be expected by increasing the loop response.

SOFT START

Soft starting of the output is optional, but recommended to minimize the output voltage overshoot upon power-up. This does not occur in applications which will always have some load on the output. However, most electronic ballast have either no load, or a very light load on the output at power-up and will see the overshoot. Soft start implementation requires only a diode and capacitor from the compensation pin to ground. Another diode from the capacitor to VCC discharges the soft start capacitor to the falling Vcc voltage when the AC line power is removed. This will guarantee that the circuit will always start up in soft start if the line is AC plug is removed for a few seconds. Again, this is an optional feature which depends on the application.

One "trick" to significantly reduce the size of the soft start capacitor is to replace the diode with a cheap PNP transistor. A capacitance multiplier can be obtained by connecting the PNP emitter to the error amplifier output and soft start capacitor from the base to ground. The collector of the transistor is connected to ground. This adaptation will scale the capacitance value up by beta of the transistor at the amplifier output. A 2N2907 or equivalent is a popular choice and will reduce the capacitance value by a factor of approximately 50.

A 1N914 or 1N4148 signal diode should be used from the base to emitter to prevent negative base-emitter voltages from damaging the transistor. Additionally, this transistor can easily be interfaced with any optional fault protection schemes to soft start the controller following a fault.

SOFT START IMPLEMENTATION

CURRENT SENSE

Current in the PFC design is sensed in the return line of the preregulator circuitry at the AC input bridge rectifiers. One side of the current sense resistor is referenced to the UC3852 "ground" connection. The other end of the resistor develops the current sense voltage which is equivalent to minus IL(t) * Rsense. The UC3852 zero current detection circuitry incorporates two comparators, one for zero current detection and another for over current protection.

ZERO CURRENT DETECTION

The zero current detection circuitry uses a negative 10 millivolt (-10mV) threshold as its reference. This negative threshold guarantees that there are no

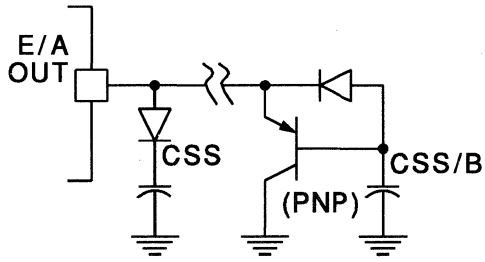


Figure 7.

startup problems since this input must be pulled below ground for normal operation. Whenever the zero detect input is raised above the minus ten millivolt threshold, the comparator is triggered and the next switching cycle begins.

Inductor current can be sensed by a current sense resistor which develops minus 400mV maximum during an overcurrent condition. This should only occur at a twenty percent overload, or 1.2 * IL(pk).

R(shunt) = 0.4 V / (1.2 * IL(pk))

Power dissipated in the shunt can be calculated by using the RMS component of the line current. The peak input current (IP) is one half of the peak inductor current (IL(max). The RMS component of the line current (IP(rms)) is obtained by dividing the peak line current (IP) by the square root of two (1.41).

IP(rms) = [IL(pk) / (2 * 1.414)]

P (R(sense)) = IP(rms)^2 * R(sense)

Standard value, low resistance (1 ohm or less) one-eighth to one-quarter watt resistors can used alone or paralleled to obtain the exact value. Carbon composition or film resistors exhibit low series inductance and will work best.

A small R/C filter can be added in the current sense circuitry to filter out switching noise caused by circuit parasitics. This delay will minimally effect the precise two-to-one ratio of the peak to average

duce the amount of EMI/RFI filtering required by minimizing the rectifier recovery noise. For best results, the filter delay time should match the rectifiers recovery time. A ten ohm resistor and a one nanoFarad (1 nF) capacitor are good starting values.

OVERCURRENT FAULT PROTECTION

The UC3852 contains and overcurrent comparator (-400mV) which quickly terminates the PWM output. This comparator also drives circuitry connected to the ISET pin which raises its normal 5 volt amplitude to 9 volts during the overcurrent condition. In addition to programming the ramp capacitor charging current, the ISET pin can be used to drive external fault protection circuits. A resistor in series with a 5.6 volt zener diode to the ISET pin will develop approximately 3.4 volts across the resistor when an overcurrent fault is detected. This signal can be used to trigger external shutdown or hiccup circuitry.

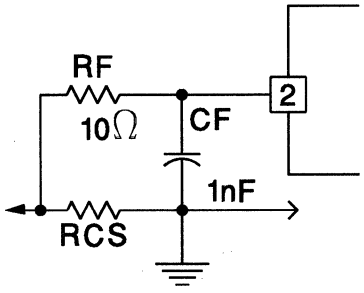


Figure 8.

GATE DRIVE

The UC3852 PWM output section is MOSFET compatible and rated for a one amp peak current. This totem pole design also features a twelve volt (12V) clamped output voltage to prevent excessive gate voltage when used with unregulated (Vcc) supply voltages. A twelve ohm resistor between the UC3852 and the MOSFET switch gate will limit the peak output current to its one amp maximum during normal operation.

Additionally, the UC3852 self biasing active low totem-pole design holds the MOSFET gate low during undervoltage lockout, preventing catastrophic problems at power-up and removal of the AC input.

inductor current and have an insignificant impact on power factor. However, this modification can re

ADVANCED PROTECTION CIRCUITRY

Certain applications of the UC3852 control IC may require sophisticated protection features. Some examples of these options are overvoltage protection and restart delay, soft start or latch-off following a fault. Each of these features can be added to the control circuit with a minimal amount of external parts, and often combined using shared components.

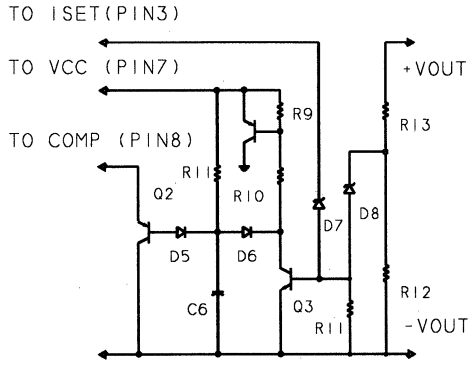


Figure 9.

LIST OF COMPONENTS

C6 = 1 uF, 35V
D5,6 = IN4148
D7 = 6.2 V ZENER
D8 = 40 V ZENER
Q2,4 = 2N2907
Q3 = 2N2222
R9,10 = 10 K
R11 = 1 MEG
R12 = 24 K
R13 = Calculate for OVP
R14 = 1 K

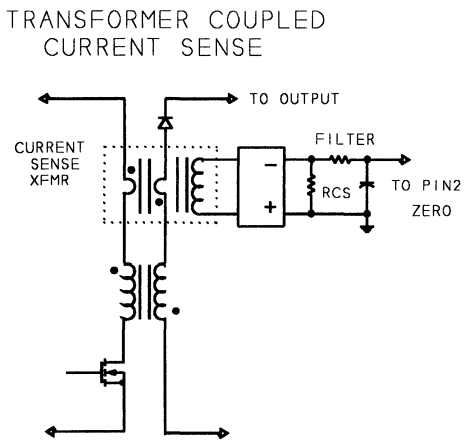


Figure 10.

Soft start is programmed by R11, C6 and the beta of Q2. Overcurrent protection starts at the UC3852 ISET pin which outputs a 9 V signal during a fault. This drives Q3 on through D7 and discharges C6 causing a soft start. Q4 also turns on with this arrangement which discharges Vcc causing a "hiccup". This is optional, and replacing Q3 with an SCR would latch the circuit off until power is reset. Overvoltage protection is attained via R11, R12, R13 and zener diode D8. When enough current flows through the zener (D8), R11 biases transistor Q3. Protection is similar to the overcurrent condition.

Regulated Auxiliary Bias Circuit

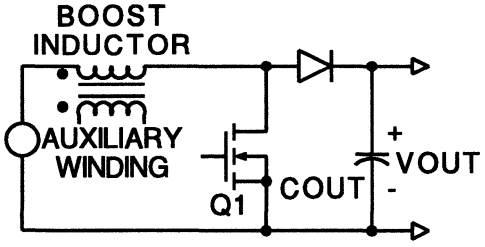


Figure 11.

CURRENT SENSE TRANSFORMERS

A transformer can be used to sense current in most of the UC3852 applications for higher efficiency. Two primary windings are needed to sense each component of the switched current. These may also be unequal in number of turns, depending on the input and output currents (or voltages). A single secondary winding and bridge rectification recreates the total inductor current. A small R/C filter network may be required to smoothen out spikes caused by the leakage inductance.

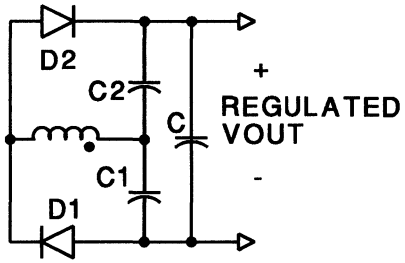


Fig. 12

Universal AC Input Feedforward Circuit

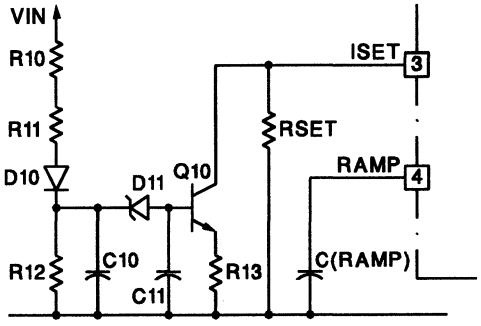


Figure 13.

REGULATED BOOTSTRAP SUPPLY

A regulated auxiliary supply is obtainable with a slight modification to the bootstrap interface and two inexpensive components. This circuit is advantageous in applications which incorporate other control ICs for the main converter or ballast drive sections. A regulated auxiliary voltage is NOT needed for the UC3852 which features a clamped twelve volt (typical) gate drive output voltage. This insures proper drive amplitude for power MOSFETs with an unregulated IC supply voltage to 30 volts.

9

Dual AC Input Range (110/220 VAC)
Feedforward Circuit

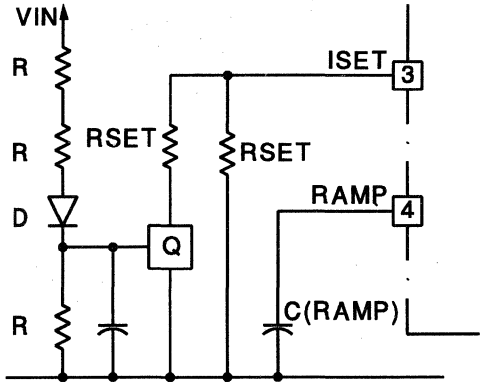


Figure 14.

OTHER PFC APPLICATIONS

The basic PFC schematic of Figure 1 can be used as a template for other PFC applications with different input voltage ranges and output power levels. A majority of the changes will be to accommodate higher (or lower) voltages and currents. Once familiar with the complete design procedure as outlined in this application note, designers are encouraged to recalculate the values for their applications using the same guidelines.

UNIVERSAL AC INPUT RANGE

The UC3852 controlled-on time, zero current switched PFC technique can be used to accommodate wide AC input voltages with the addition of a simple feedforward circuit. This external circuitry is required to cancel out the line dependent changes in the switch on-time over the three-to-one input range from 85 to 264 volts. Otherwise, the approximate nine-to-one control range of the UC3852 on-time would be fully used for line regulation allowing no accommodation for load changes.

CIRCUIT OPERATION

The rectified input voltage is applied across the network consisting of R10 through R12, D12 and C10. Capacitor C10 charges to the peak of the divided input voltage and is large enough to maintain this level over one line cycle. Diode D11 serves as an offset to bypass the range extender circuitry until a sufficient minimum line voltage has been established, typically 80 VAC. Capacitor C11, a small filter capacitor and the base of transistor Q10 reach a voltage of V(C10) minus the Zener forward voltage drop of diode D11. As this voltage rises, the emitter of Q10 and voltage across resistor R13 follows, offset by the base-emitter diode drop of Q10. This increasing bias pulls more current from the UC3852 ISET pin which sits at a fixed voltage. The current in both resistor R13 and resistor RSET is pulled from the UC3852 ISET output. Within the UC3852, the ISET current is mirrored to the RAMP capacitor (Cramp) which is compared to the error amplifier output to determine the ON-time. As the input voltage increases bias to Q10, more current is pulled from ISET thus increasing the RAMP charging current. For a fixed output load, this circuit performs the function of voltage feedforward and can keep the error amplifier output voltage fixed regardless of AC input voltage. This allows the full use of the ICs ON-time control range to accommodate load variations.

FEEDFORWARD CIRCUIT DESIGN

LOW LINE:

ISET= 5V/RSET

t(on)max=8.8*Cramp / ISET

HIGH LINE:

ISET= 5V/(RSET || RSET')

GENERAL:

V(C10)=1.41*VIN*R12/(R10+R11+R12)

NOTE:V(C10)MAX=5V+Vzener

ISET(MIN)=5V/RSET

ISET(MAX)=ISET(MIN)+5V/R13

FEEDFORWARD BEGINS WHEN :

V(C10)-Vzener-Vbe(Q10) 0V

COMPONENTS:

C10=22uF/16V Q10=2N2222

C11=1nF/16V R10,11=100K

D10=1N4148 R12,13=5.1K

D11=1N5221(2.4V) RSET=51K

CONTINUOUS CURRENT PFC BOOST CONVERTER

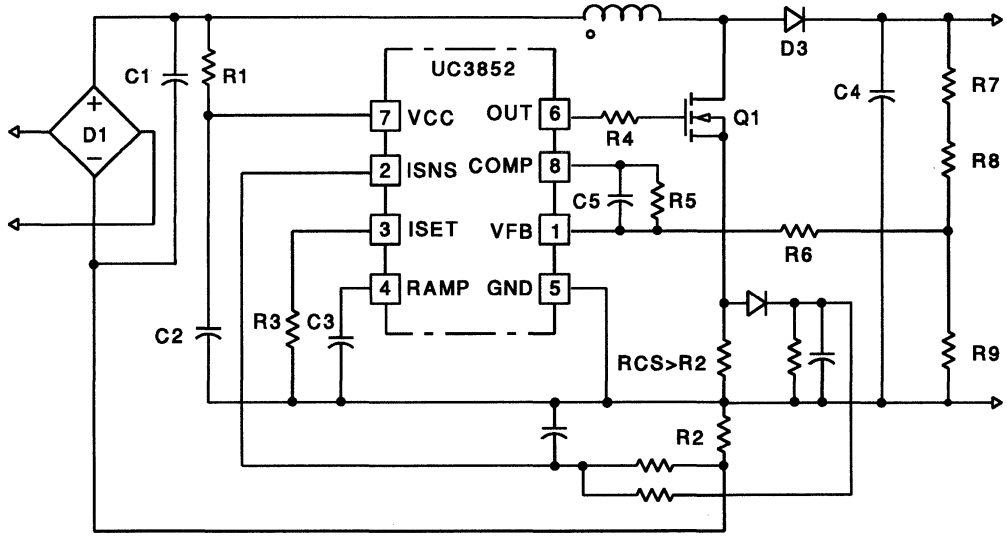


Figure 15.

CONTINUOUS PFC CURRENT IMPLEMENTATION

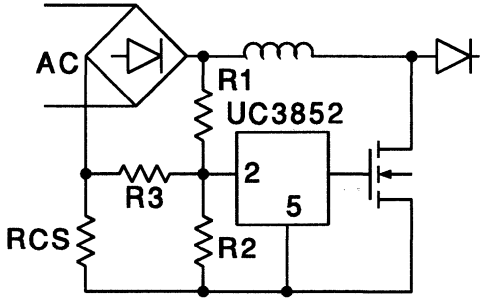


Figure 16.

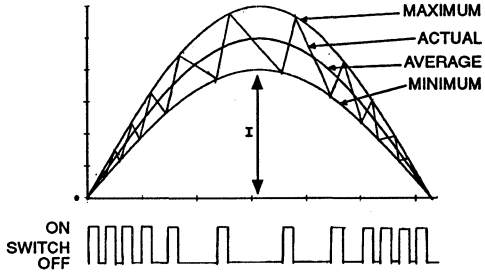


Figure 17.

UC3852 CONTROLLED PFC FLYBACK CONVERTER

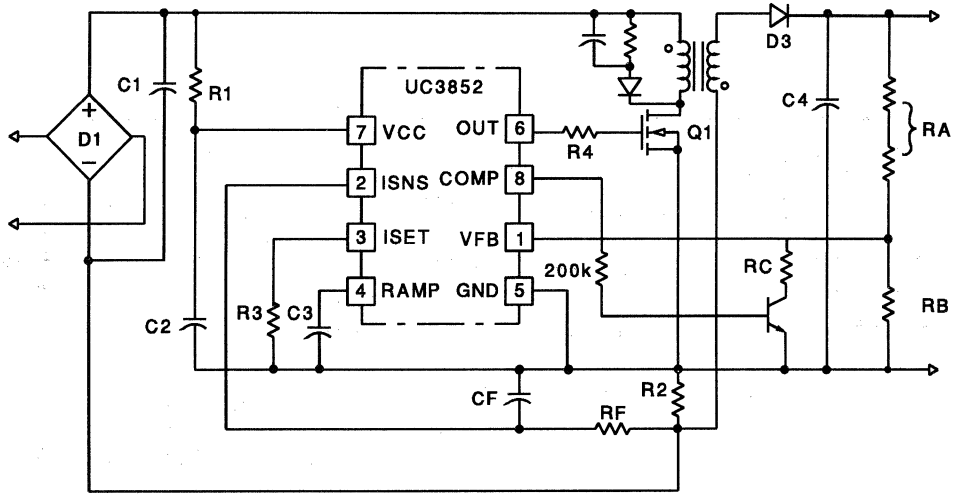


Figure 18.

UC3852 AS A CAPACITIVE DISCHARGE DRIVER

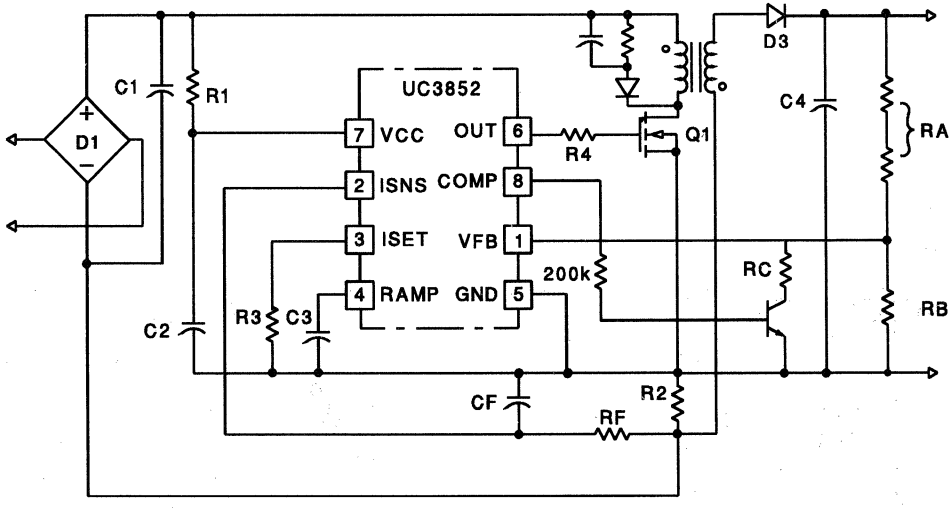


Figure 19.

AUTORANGE (110/220) VOLTAGE FEEDFORWARD CIRCUIT

Input line voltage feedforward can also be obtained with a simple circuit for dual AC input ranges with less demanding load variations. Shown below is a single step autorange circuit for use with the UC3852 timing circuitry. Basically, the TL431 is used as a comparator to switch in a second timing resistor (RSET') when the input voltage exceeds a preset threshold.

The AC input voltage is rectified by diode D20 and divided down by resistors R20 and R21. Capacitor C20 peak charges and filters this waveform to develop a DC voltage proportional to the input line. RSET is programming the initial charging current to the timing capacitor CRAMP. When the voltage across C20 exceeds the 2.5 V threshold of the TL431 comparator, its output goes low. This places

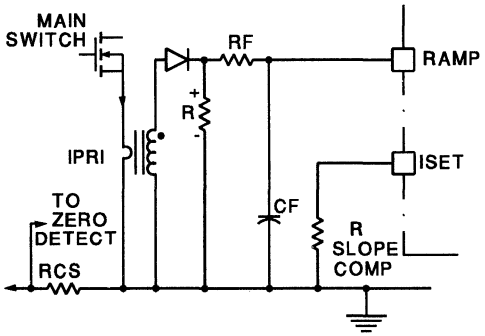


Figure 20.

a second timing resistor, RSET', in parallel with the original one thus increasing the current to CRAMP and performing line feedforward. Resistor values should be selected to switch in the feedforward compensation at approximately 155 VAC which is mid-range between high line of a 110 VAC input (130 VAC) and low line for a 220 VAC input (180 VAC). The value of RSET' must be selected to account for the TL431 output saturation voltage.

CONTINUOUS CURRENT PFC BOOST CONVERTER

The zero current switched PFC technique can also be modified to operate in the continuous inductor current mode. A positive amplitude, small offset signal is derived from the input voltage waveform. It gets added to the normal current sense signal which is negative with respect to ground. Summing these two signals to the ZEROinput biases the actual inductor current sense more positive. Therefore, the zero current detection threshold is crossed before the inductor current is actually zero, and the PFC preregulator operates with continuous current. The exact amplitude of both parts of the inductor current can be determined by adjusting the inductance, on-time, and current sense resistor.

OTHER PFC TOPOLOGIES

The UC3852 can also perform power factor correction using the Flyback topology with a slight degradation to Power Factor. A Flyback topology is commonly used to generate a lower (or much higher) voltage output than the Boost converter. A nonisolated version of this is shown in Figure 18. for simplicity.

A resistor in series with the power return lead senses the inductor charging current while the switch is on, similar to that of the boost converter. However, the discharging current information is lost when the switch is off while the stored inductive energy is delivered to the output. A second current sense resistor is added in series with the secondary winding as shown to recover this information. A small amount of filtering may be necessary to smoothen out switching noise spikes while summing the current sense signals.

Good regulation of the output voltage will be obtained with this technique although some 120 Hz (2 x line frequency) ripple is to be expected. The flyback circuitry cannot fully transfer power when the input line voltage goes down near zero each cycle. This approach has numerous applications where a small amount of power supply ripple is acceptable. Post regulator circuits can be added to improve regulation if necessary.

CAPACITIVE DISCHARGE CIRCUITS

The UC3852 can also be used in capacitive discharge circuits, typical of photoflash and strobe applications. In fact, the circuit shown below will provide the minimum recharge time for a given peak input current. Zero current switching insures that the next switching cycle is initiated as soon as the inductor current discharges to zero. There is no deadtime between conversion cycles and the output is charged as quickly as possible for the programmed maximum inductor current.

Regulation is achieved by using a burst mode of operation where the UC3852 stops delivering output pulses when the output voltage setpoint is reached. Operation will begin again when the output voltage drops below the lower programmed threshold. Both of these thresholds are pro-

grammed by Ra, Rb and Rc according to the following formulas.

Vout(max) = (5*(Ra+Rx))/Rx

Vout(min) = (5*(Ra+Rb))/Rb

where Rx=(Rb*Rc)/(Rb+Rc)

NON PFC APPLICATIONS USING VARIABLE FREQUENCY OPERATION

Conventional PWM (non PFC) applications using a variable frequency control techniques can also be implemented with the UC3852. This applies to both current mode and variable ON-Time control methods. Typical examples of these are discontinuous current boost and flyback converters. Variable frequency operation is popular in numerous applications as it can minimize the peak current in comparison to fixed frequency designs. The zero current detection and switching technique of the UC3852 should be used in its standard configuration with current sensed below ground, although a current transformer can be introduced.

IMPLEMENTING CURRENT MODE

The ICs RAMP input will be used as the current sense input to be compared to the error amplifier output for current mode control. A current transformer is recommended to fully utilize the 9 volt compliance of this pin. This implementation allows for a wide load swing with maximum noise immunity. The RAMP pin gets discharged by internal IC logic to 0.2 V at the end of each ON-time. Therefore, some series impedance to the current sense resistor is recommended to keep load current outside of the IC. Any filter capacitor to suppress the switch leading edge noise spike will also get discharged. The ramp pin does not need a programming resistor, but one could be used to introduce optional slope compensation via the filter capacitor.

VARIABLE ON-TIME CONTROL

The switch ON-Time can also be controlled by comparing a sawtooth ramp to the error amplifier output. Configuration of this is basically identical to the standard PFC application using a RAMP capacitor and resistor to program the maximum ON-Time. Error amplifier compensation is likely to be much different and utilize a much higher loop crossover frequency than its PFC counterpart. The ICs error amplifier is similar to a '741 type general purpose OP-AMP and is programmed accordingly.

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2. AHMED, SAEED, : "Controlled On-time Power FActor Correction Circuit with Input Filter"; Thesis, Virginia Polytechnic Institute.

3. MAMMANO,BOB and DIXON,LLOYD: "Designing High Power Factor Systems - Choosing the Optimum Circuit Topology", PCIM Magazine, March 1991.

PERFORMANCE EVALUATION

The UC3852 controlled PFC circuit shown in Figure 1 was constructed using the list of materials provided for this application. Power Factor and Total Harmonic Distortion to the 50th harmonic were measured using a VOLTEC PM- 3000 AC power analyzer. Test results indicated a power factor of 0.998 and T.H.D. below 6% at nominal line and full load. Very similar readings were obtained over the complete input voltage range and a moderate load change. Zero Current Switching (ZCS) facilitates high overall efficiency with this PFC technique.

UC3852 PFC TEST CIRCUIT

SPECIFICATIONS:

VIN = 85 TO 135 VAC

VOUT = 350 VDC

POUT = 86 W

MEASURED PERFORMANCE :

P.F. = 0.998

T.H.D. = 5.81 %

TEST CONDITIONS:

(nominal line)

VIN = 115.7 VAC

IIN = 0.799 AAC

PIN = 92.13 W

VA IN = 91.84

INRUSH Ipk = 17.7 A

VOUT = 355.6 VDC

IOUT = 0.242 ADC

POUT = 86.1 W

EFFICIENCY = 93.45 %

CURRENT WAVEFORM :

HARMONIC CONTENT

1st : 0.775 Amp

3rd : 3.91 %

5th : 0.82 %

7th : 0.38 %

9th : 0.35 %

11th : 1.30 %

13th : 0.21 %

LIST OF MATERIALS

CAPACITORS

C2 = 0.47 uF / 200 V

C3 = 82 uF / 400 V

C4 = 22 uF / 35 V

C5 = 0.1 uF / 35 V

C6 = 1 nF / 16 V

C7 = 0.1 uF / 16 V

DIODES

D1-4 = 1N4004, 1 A / 400V

D5 = 1N4937, 1 A / 600V

trr = 200ns

D6 = 1N4148, 0.2 A / 50 V

INDUCTORS

L2 = 1 mH Boost inductor

L3 = Several turns on L2 to provide 20 VDC supply voltage

RESISTORS

R1 = 100 k ohms 1 Watt

R2 = 0.1 ohm 1 W non-inductive

R3 = 18.2 k ohms 1% 1/2 W

R4 = 1 meg ohm 1/4 W

R5 = 330 k ohms 1% 1/2 W

R6 = 390 k ohms 1% 1/2 W

R7 = 10 k ohms 1% 1/4 W

R8 = 20 k ohms 1/4 W

R9 = 10 ohms 1/2 W non-inductive

TRANSISTOR

Q1 = IRF830 500 V / 4 A

INTEGRATED CIRCUIT

U1 = UC 3852

UCC 3800/1/2/3/4/5 BiCMOS CURRENT MODE CONTROL ICs

BILL ANDREYCAK

INTRODUCTION

Power supply design has become increasingly more challenging as engineers confront the difficulties of obtaining higher power density, improved performance and lower cost. The control for many of these switchmode supplies was revolutionized with two significant introductions; an advance technique known as current mode control, and a novel PWM solution, the UC3842 controller. This IC contained several innovative features for general purpose current mode controlled applications. Included were high speed circuitry, undervoltage lockout, an op-amp type error amplifier, fast overcurrrent protection, a precision reference and a high current totem-pole output.

The popular UC3842 control circuit architecture has been recently improved upon to deliver even higher levels of protection and performance. Advanced circuitry such as leading edge blanking of the current sense signal, soft-start and full cycle restart have been built-in to minimize external parts count. Additionally, these integrated circuits have been developed on a BiCMOS wafer fabrication process geared to virtually eliminate supply power and propagation delays in comparison to the bipolar UC3842 devices. These sophisticated new BiCMOS controllers, the UCC3800 through UCC3805 pulse width modulators address the challenges presented by the upcoming generations of power supply designs. This application note will highlight the features incoporated into this new generation of PWM controllers in addition to realizeable enhancements in typical applications. The specific differences between members of the UCC3800/1/2/3/4/5 family are reflective of their maximum duty cycle, undervoltage lockout thresholds and reference voltage which are summarized in the following table.

Unitrode Part #	Max Duty Cycle	VRef (V)	UVLO Turn-On	UVLO Turn-Off
UCC3800	100%	5.0	7.2	6.9
UCC3801	50%	5.0	9.4	7.4
UCC3802	100%	5.0	12.5	8.4
UCC3803	100%	4.0	4.1	3.6
UCC3804	50%	5.0	12.5	8.4
UCC3805	50%	4.0	4.1	3.6

UCC3800/1/2/3/4/5 PWM FEATURES

A. Low start-up current
B. Undervoltage lockout
C. Low operating current
D. Internal soft start
E. Self biasing output during UVLO
F. Leading Edge Blanking
G. Self regulating Vcc supply
H. Full cycle restart after fault
I. Clamped gate drive amplitude
J. Reduced propagation delays
K. 5 Volt operation (UCC3803 & 05)

IN-CIRCUIT ADVANTAGES vs. UC3842

- Greatly reduced power requirements
- Eliminates bootstrap supply
- Fewer external components
- Lower junction temperature
- Reduced stress during faults
- No current sense R/C filter network
- Faster response to fault
- Higher frequency operation
- Higher maximum duty cycles

UCC3800/1/2/3/4/5 DEVICE OVERVIEW

The BiCMOS UCC3800/1/2/3/4/5 devices have similar standard features and pinouts to the bipolar UC3842/3/4/5 PWMs and are enhanced replacements in many applications. There are a few important differences however which may require minor modifications to existing applications.

APPLICATION DIFFERENCES

1. Maximum supply voltage from a low impedance source: 12V versus 30V
2. Undervoltage lockout thresholds
3. Start-up current
4. Operating current
5. Oscillator timing component values
6. Reference voltage (UCC3803 and 05)
7. Vcc supply self clamping zener voltage
8. Internal soft start
9. Internal full cycle restart
10. Clamped gate drive voltage
11. Current loop gain
12. E/A reference voltage ('03 & '05)

UCC3800/1/2/3/4/5 BLOCK DIAGRAM

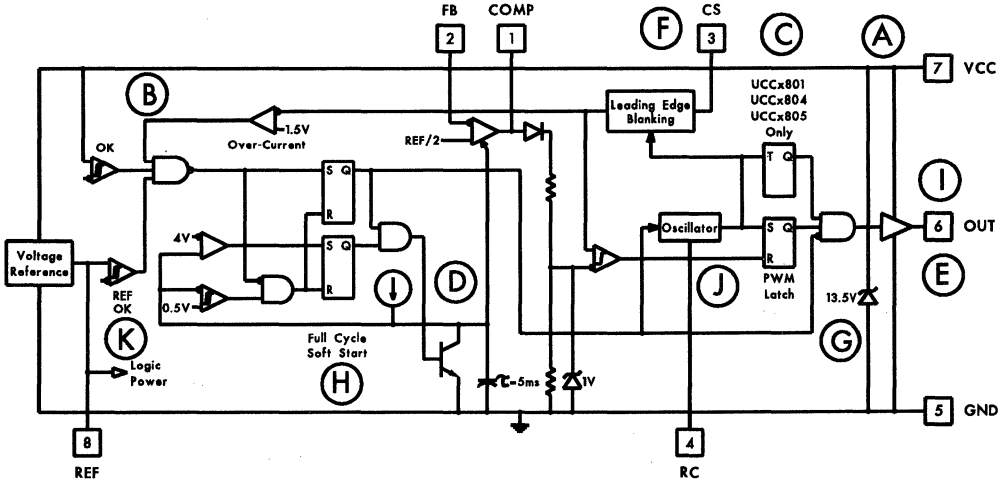


Figure 1

SUPPLYING POWER

An internal Vcc shunt regulator is incorporated in each member of the UCC3800/1/2/3/4/5 PWMs to regulate the supply voltage at approximately 13.5 volts. A series resistor from Vcc to the input supply source is required with inputs above 12 volts to limit the shunt regulator current as shown in figure 2. A maximum of 10 milliamps can be shunted to ground by the internal regulator.

The internal regulator in conjunction with the device's low startup and operating current can greatly simplify powering the device and may eliminate the need for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and needs no external zener diode or regulator protection with a current limited input supply. The UVLO start-up threshold is 1.0 volts below the shunt regulator level on the '02 and '04 devices to guarantee start-up.

It is important to bypass the ICs supply (Vcc) and reference voltage (Vref) pins with a 0.1uF to 1uF ceramic capacitor to ground. The capacitors should be located as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in off-line applications to hold the supply voltage (Vcc) above the UVLO turn-off threshold during start-up.

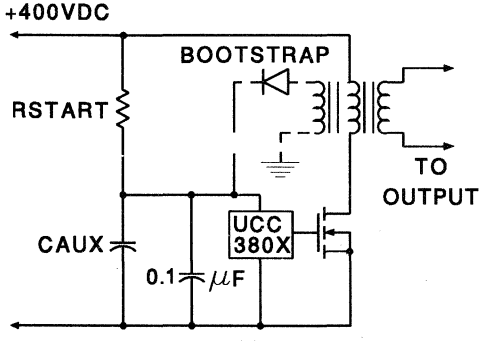


Figure 2

UNDERVOLTAGE LOCKOUT

The UCC3800/1/2/3/4/5 devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (Vcc) and the reference voltage (Vref) are monitored by the UVLO circuitry. An active low, self biasing totem pole output during UVLO design is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCC 3802/3/4/5 devices are different from the previous generation of UC3842/3/4/5 PWMs. Basically, the thresholds are optimized for two groups of applications; off-line power supplies and DC-DC converters. The UCC3802 and UCC3804 feature typical UVLO thresholds of 12.5V for turn-on and 8.3V for turn-off, providing 4.3V of hysteresis. For low voltage inputs which include battery and 5V applications, the UCC3803 and UCC3805 turn on at 4.1V and turn off at 3.6V with 0.5V of hysteresis. The UCC3800 and UCC3801 have UVLO thresholds optimized for automotive and battery applications.

During UVLO the IC draws approximately 100 microamps of supply current. Once crossing the turn-on threshold the IC supply current increases typically to about 500 microamps, over an order of magnitude lower than bipolar counterparts.

SELF BIASING, ACTIVE LOW OUTPUT

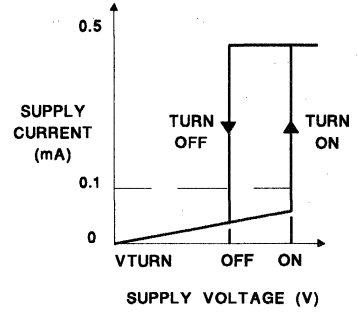


Figure 3

Device	Vton	Vtoff
UCC3800	7.2	6.9
UCC3801	9.4	7.4
UCC3802, 4	12.5	8.3
UCC3803, 5	4.1	3.6

DURING UNDERVOLTAGE LOCKOUT

The self biasing, active low clamp circuit shown eliminates the potential for problematic MOSFET turn on. As the PWM output voltage rises while in UVLO, the P device drives the larger N type switch ON which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the ICs supply voltage during undervoltage lockout.

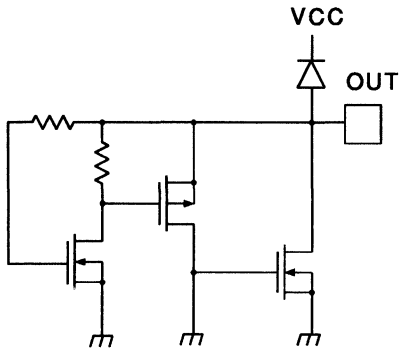


Figure 4

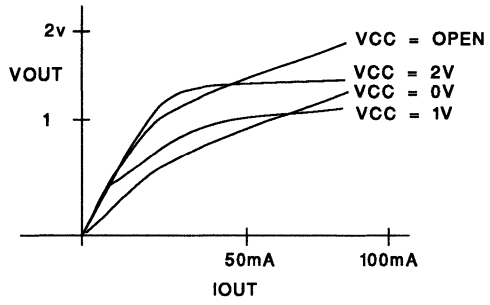


Figure 5

REFERENCE VOLTAGE

The traditional 5.0V amplitude bandgap reference voltage of the UC3842 family can be also found on the UCC3800,1,2 and UCC3804 devices. However, the reference voltage of the UCC3803 and UCC3805 device is 4.0 volts. This change was necessary to facilitate operation with input supply voltages below five volts. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO which can be used as a UVLO status indication.

REFERENCE DIFFERENCES

Note that the 4V reference voltage on the UCC3803 and UCC3805 is derived from the supply voltage (Vcc) and requires about 0.5V of headroom to maintain regulation. Whenever Vcc is below approximately 4.5V, the reference voltage also will drop outside of its specified range for normal operation. The relationship between Vcc and Vref during this excursion is shown in Figure 7.

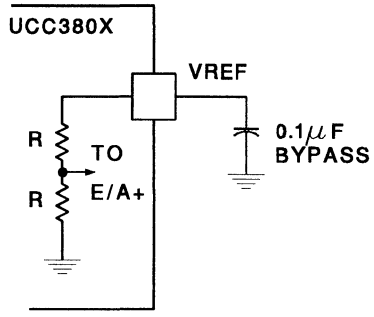


Figure 6

The noninverting input to the error amplifier is tied to one-half of the PWMs reference voltage, Vref. Note that this input is 2.0V on the UCC3803 and UCC3805 and 2.5V on the higher reference voltage parts, the UCC3800, UCC3801, UCC3802 and UCC3804.

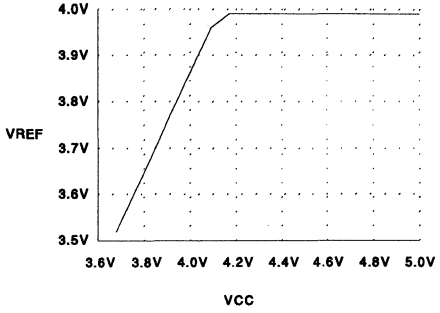


Figure 7

OSCILLATOR SECTION

The oscillator section of the UCC3800 through UCC3805 BiCMOS devices has few similarities to the UC3842 type — other than single pin programming. It does still utilize a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values will need to be changed since a much lower charging current is desirable for low power operation.

Several characteristics of the oscillator have been optimized for high speed, noise immune operation. The oscillator peak to peak amplitude has been increased to 2.45V typical versus 1.7V on the UC 3842 family. The lower oscillator threshold has been dropped to approximately 0.2 volts while the upper threshold remains fairly close to the original 2.8 volts at approximately 2.65V.

Discharge current of the timing capacitor has been increased to nearly 20 milliamps peak as opposed

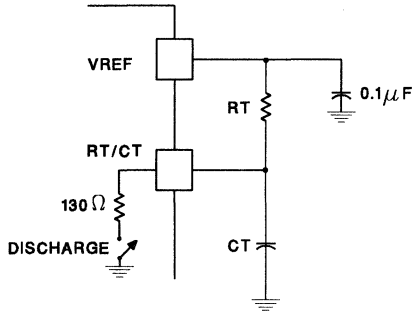


Figure 8

to roughly 8mA. As shown, this can be represented by approximately 130 ohms in series with the discharge switch to ground. A higher current was necessary to achieve brief deadtimes and high duty cycles with high frequency operation. Practical applications can utilize these new ICs to a 1 MHz switching frequency.

SYNCHRONIZATION

Synchronization of these PWM controllers is best obtained by the universal technique shown in figure 12. The ICs oscillator is programmed to free run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the resistor in series to ground with the timing capacitor to force synchronization. Typically, a one volt amplitude pulse of 100 nanoseconds width is sufficient for most applications.

The ICs can also be synchronized to a pulse train input directly to the oscillator Rt/Ct pin. Note that the IC will internally pull low at this node once the upper oscillator threshold is crossed. This 130 ohm impedance to ground remains active until the pin is lowered to approximately 0.2 V. External synchronization circuits should accommodate these conditions.

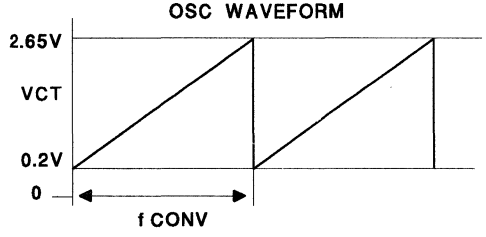


Figure 9

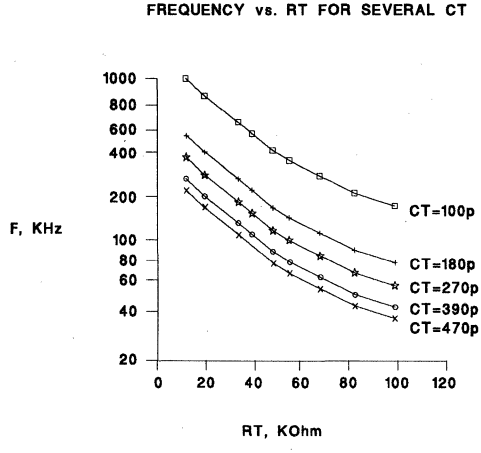


Figure 10

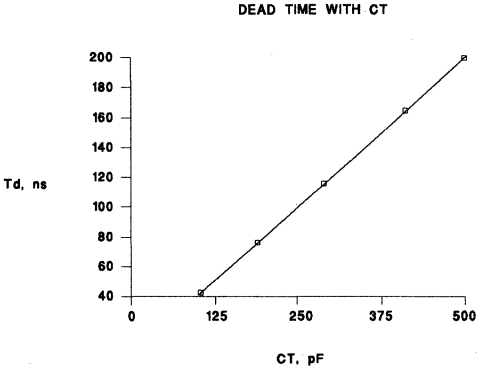


Figure 11

PWM SECTION : MAXIMUM DUTY CYCLE

Maximum duty cycle is higher for these devices than for their UC3842/3/4/5 predecessors. This is primarily due to the higher ratio of timing capacitor discharge to charge current which can exceed one-hundred to one in a typical BiCMOS application. **Attempts to program the oscillator maximum duty cycle much below the specified range by adjusting the timing component values of Rt and Ct) should be avoided.** There are two reasons to refrain from this design practice. First, the ICs high discharge current would necessitate higher charging currents than necessary for pro-

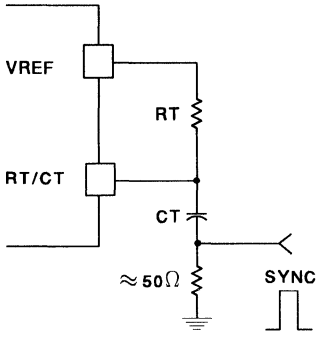


Figure 12

gramming, defeating the purpose of low power operation. Secondly, a low value timing resistor will prevent the capacitor from discharging to the lower threshold and initiating the next switching cycle.

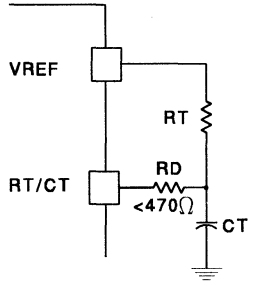


Figure 13

DEADTIME CONTROL

Deadtime is the term used to describe the guaranteed OFF time of the PWM output during each oscillator cycle. It is used to insure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation.

The deadtime of the UCC380x PWM family is determined by the internal 130 Ohm discharge impedance and the timing capacitor value. Larger capacitance values extend the deadtime whereas smaller values will result in higher maximum duty cycles for the same operating frequency. A curve for deadtime versus timing capacitor values is provided below.

Increasing the deadtime is possible by adding a resistor between the Rt/Ct pin of the IC and the timing components. The deadtime increases with the discharge resistor value to about 470 Ohms as indicated from the curve. Higher resistances should be avoided as they can decrease the deadtime and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing Rt will "freeze" the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V.

Reducing the maximum duty cycle can be accomplished by adding a discharge resistor (below 47 Ohms) between the ICs Rt/Ct pin and the actual Rt/Ct components. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge – but not the charging portion of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude.

Because of the reduced peak-to-peak amplitude, the exact value of Ct may need to be adjusted from UC3842 type designs to obtain the correct initial oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values since these are readily available in finer numerical increments.

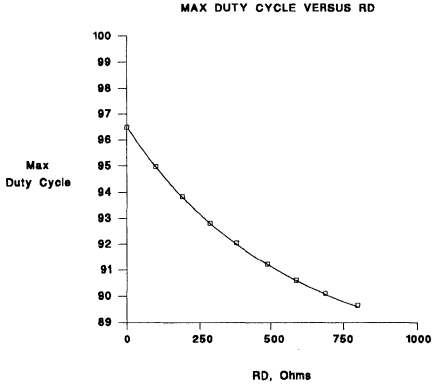


Figure 14

LEADING EDGE BLANKING

A 100 nanosecond leading edge blanking interval is applied to the current sense input circuitry of the UCC3800/1/2/3/4/5 devices. This internal feature has been incorporated to eliminate the need for an external resistor-capacitor filter network to sup-

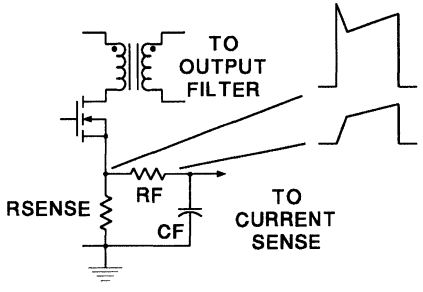


Figure 15

press the switching spike associated with turn-on of the power MOSFET. This 100 nanosecond period should be adequate for most switchmode designs but can be lengthened by adding an external R/C filter.

Note that the 100 ns leading edge blanking is also applied to the cycle-by-cycle current limiting function in addition to the overcurrent fault comparator.

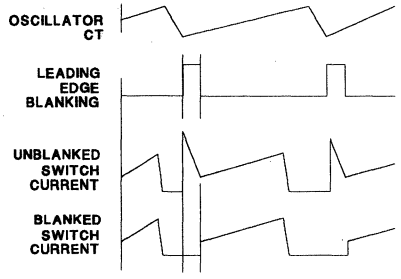


Figure 16

MINIMUM PULSE WIDTH

The leading edge blanking circuitry can lead to a minimum pulse width equal to the blanking interval under certain conditions. This will occur when the error amplifier output voltage (minus a diode drop and divided by 1.65) is lower than the current sense input. However, the amplifier output voltage must also be higher than a diode forward voltage drop of about 0.5V. It is only during these conditions that a minimum output pulse width equal to the blanking duration can be obtained.

Note that the PWM comparator has two inputs; one is from the current sense input. The other PWM input is the error amplifier output which has a diode and two resistors in series to ground. The diode in this network is used to guarantee that zero duty cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, along with pulse width.

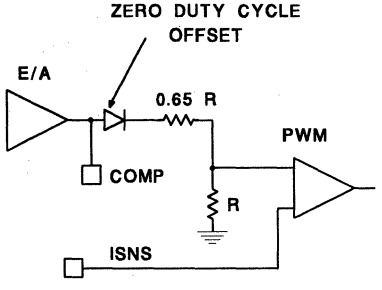


Figure 17

Zero duty cycle is achievable by forcing the error amplifier output below the zero duty cycle threshold of one diode voltage drop.

PROTECTION CIRCUITRY: CURRENT LIMITING

A 1.0 volt (typical) cycle-by-cycle current limit threshold is incorporated into the UCC3800 family. Note that the 100 nanosecond leading edge blanking pulse is applied to this current limiting circuitry. The blanking overrides the current limit comparator output to prevent the leading edge switch noise from triggering a current limit function.

Propagation delay from the current limit comparator to the output is typically 70 nanoseconds. This high speed path minimizes power semiconductor dissipation during an overload by abbreviating the on time.

CURRENT SENSE OFFSET CIRCUITRY

For increased efficiency in the current sense circuitry, the circuit shown in figure 23 can be used. Resistors R1 and R2 bias the actual current sense resistor voltage up, allowing a small current sense amplitude to be used. This circuitry provides current limiting protection with lower power loss current sensing.

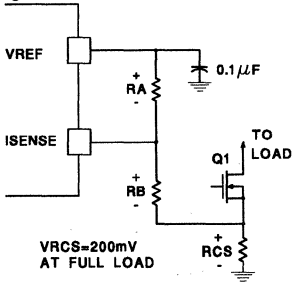


Figure 18

The example shown uses a 200 millivolt full scale signal at the current sense resistor. Resistor Rb biases this up by approximately 700 mV to mate with the 0.9V minimum specification of the current limit comparator of the IC. The value of resistor Ra changes with the specific IC used, due to the different reference voltages. The resistor values should be selected for minimal power loss. For example, a 50 uA bias sets Rb = 13k ohms, Ra=75 k ohms (UCC3800,1,2,4) or Ra=56k ohms with the UCC3803 and UCC3805 devices.

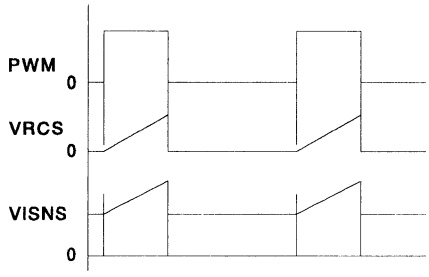


Figure 19

OVERCURRENT PROTECTION AND FULL CYCLE RESTART

A separate overcurrent comparator within the UCC 3800/1/2/3/4/5 devices handles operation into a short circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5 volt threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft start capacitor to generate a delay before retry is attempted. Often referred to as "hiccup", this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components.

Internally, the ICs overcurrent comparator triggers latched circuitry to instantly turn the PWM output off and discharge the soft start capacitor to 0.5 volts. This capacitor is then allowed to slowly charge via a current source to 4 volts while the PWM output is held low. Once the 4V threshold is reached, the soft start capacitor is again discharged and the latch is reset. This brings the PWM back into soft start which results in normal operation with the fault removed. This entire procedure is repeated every time the overcurrent comparator detects a fault.

Low leakage transformer designs are recommended in high frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the over-current comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short circuit power dissipation of the converter.

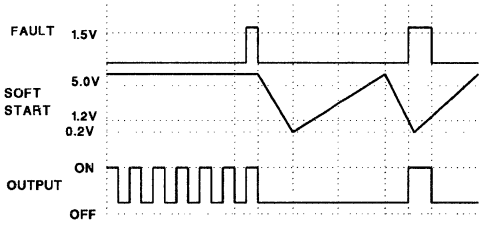


Figure 21

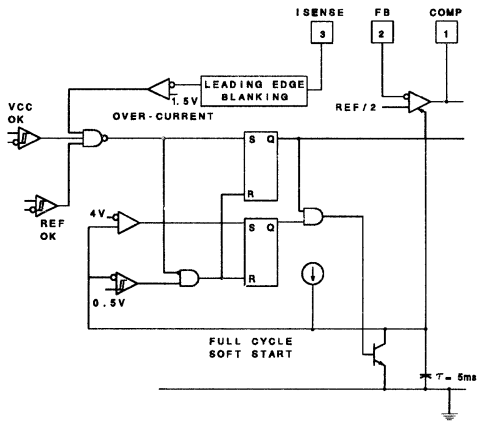


Figure 20

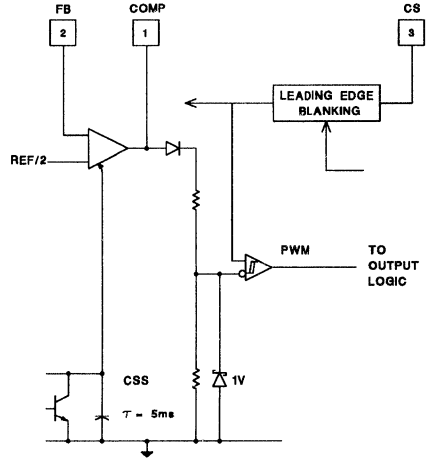


Figure 22

SOFT START

Internal soft starting of the PWM output is accomplished by gradually increasing error amplifier (E/A) output voltage. When used in current mode control, this implementation slowly raises the peak

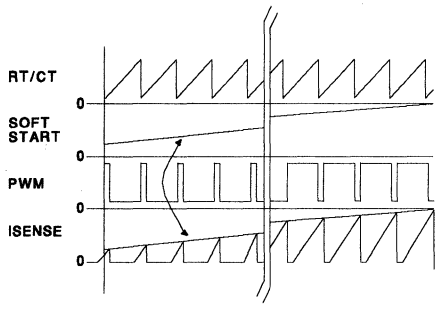


Figure 23

switch current each PWM cycle in comparison, forcing a controlled start-up. In voltage mode (duty cycle) control, this feature continually widens the pulse width.

The soft start capacitor (Css) is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of Css occurs whenever the overcurrent protection comparator is triggered by a fault.

Soft start is performed within the UCC3800/-1/2/3/4/5 devices by clamping the E/A amplifier output to an internal soft start capacitor (Css) which is charged by a current source. The soft start clamp circuitry is overridden once Css charges above the voltage commanded by the error amplifier for normal PWM operation.

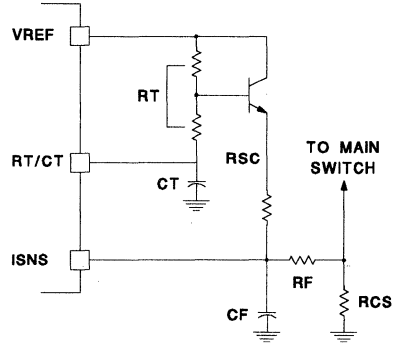


Figure 24

APPLICATIONS SECTION: CURRENT MODE CONTROL

Peak current mode control is obtained by feeding the converters switch current waveform into the current sense (Isens) input of a UCC3800/1/2/3/4/5 device. The sense resistor should be selected to develop a 0.9 V peak amplitude at full load, including slope compensation. Because of the internal 100 ns typical leading edge blanking, the traditional resistor-capacitor (Rf/Cf) filter to suppress the turn-on noise spike may not be needed.

SLOPE COMPENSATION

Slope compensation can be added in all current mode control applications to cancel the peak to average current error. Slope compensation is neces-

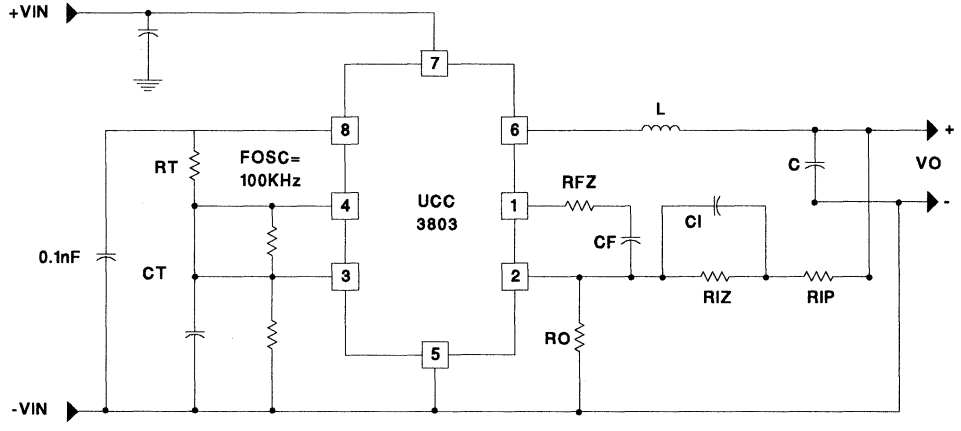


Figure 27

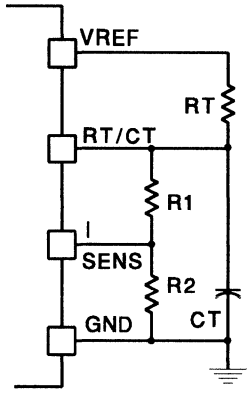
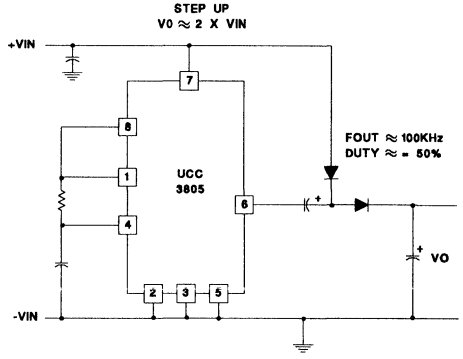


Figure 25



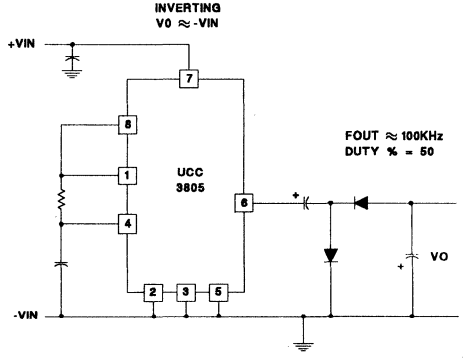


Figure 26

sary with applications with duty cycles exceeding 50%, but also improves performance in those below 50%.

Primary current is sensed using resistor Rcs in series with the converter switch. A R/C filter is also required as the capacitor will be charged from both the current sense and slope compensating circuits. The timing resistor can be broken up into two series resistors to bias up the NPN follower. This is needed to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous current converters. A NPN voltage follower drives the slope compensating programming resistor (Rsc) to provide a slope compensating current into Cf.

VOLTAGE MODE OPERATION

Any current mode control IC can be used as a direct duty cycle control (voltage mode) by applying a sawtooth ramp to the current sense input. The exponential charging of the timing capacitor (Ct) is used as an approximation of a sawtooth. This shape is obtained by using a high value timing resistance (Rt) to the reference voltage (Vref).

The oscillator waveform is resistively divided down by R1 and R2 to a 0.9V maximum amplitude and fed into the current sense input for duty cycle control. A small capacitor across R1 might be necessary to completely bring the current sense input to

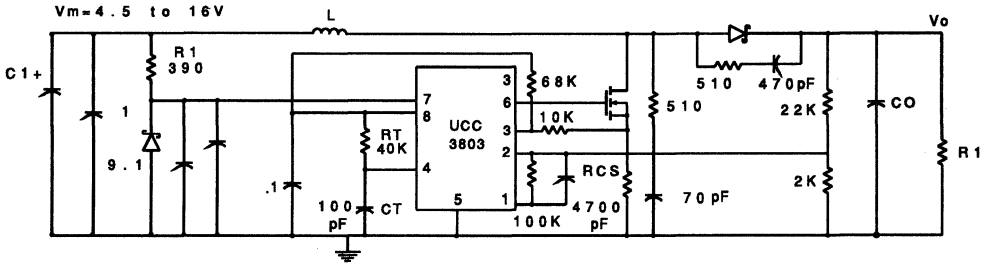


Figure 28

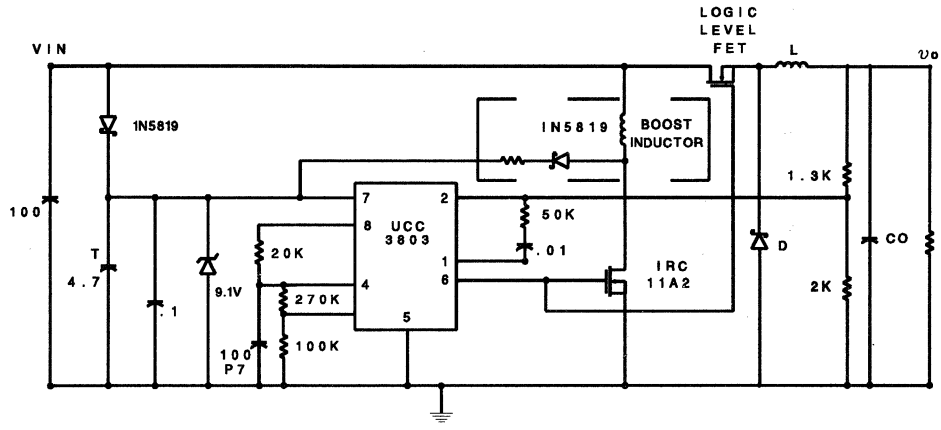


Figure 29

zero volts at the beginning of each PWM cycle. Current in the divider network should be kept around 50 microamps, a compromise between low power consumption and good noise immunity. A 15K ohm and 30 K ohm are used in the example.

This circuit can also be used to program the PWM maximum duty cycle. Values should be calculated to attain the 0.9V current sense voltage at the desired maximum duty cycle.

LOW POWER DC/DC CONVERTERS CHARGE PUMP CONVERTERS

Charge pump converters are popular for simple, low power applications. The two basic applications are free running step-up and inverting switchers which use few external components as shown.

LOW POWER BUCK REGULATOR

For voltage step down applications, the UCC 380x totem pole output can be used as both the switch and commutating diode of the buck regulator. Power dissipation and the one amp peak current rating of the ICs output stage limit the range of applications to less than 1 amp of output current. High frequency operation permits the use of small and inexpensive surface mount components.

BUCK-BOOST CONVERTER for VOLTAGE STEP-UP and/or STEP-DOWN APPLICATIONS

A two-switch buck-boost converter can be controlled by the UCC380x family of PWMs. This specific converter is useful in applications where the input voltage can be both higher and lower than the de-

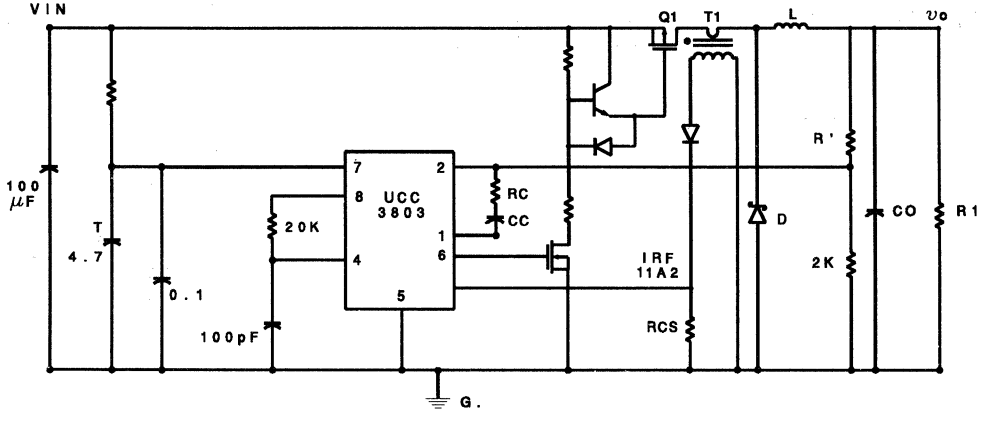
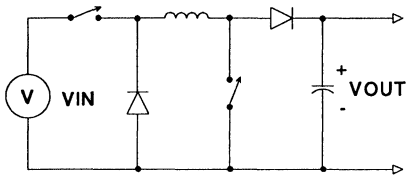


Figure 30

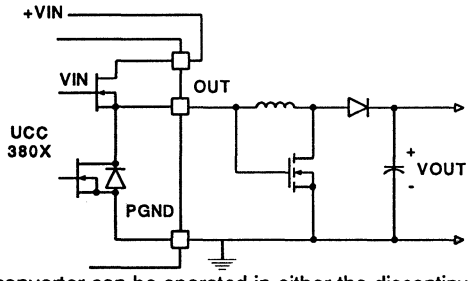
SIMPLIFIED TWO SWITCH
BUCK/BOOST CONVERTER



DRIVE SWITCHES TOGETHER

sired output voltage. Implementation combines the voltage step-down characteristic of the buck regulator with the voltage step-up of the boost converter. Both switches are driven simultaneously with this adaptation to simplify the control algorithm. Note that the PWM output of the IC will be used directly for the high side switch in a low power pplication thus requiring only one external switch. Also, the body diode of the lower side totem-pole output is used as one of the commutating rectifiers, further reducing complexity. As shown, this approach is ideal for low voltage, low power DC to DC applications. Higher voltage and higher power applications will require the use of discrete semiconductors for the high side switch and lower diode.

Duty cycle is varied with input line voltage to provide a regulated output. A curve is provided to demonstrate the ideal converter voltage gain as a function of duty cycle. This non isolated buck-boost



converter can be operated in either the discontinuous and continuous inductor current modes. High frequency switching permits the use of very small and inexpensive surface mount inductors for most low power applications. The converter can be controlled by duty cycle modulation (voltage mode) or current mode control, and with or without overcurrent protection.

BOOST CONVERTERS

The UCC 3803 and UCC 3805 devices are fully operational from a 4.5 volt input supply and are ideally suited for 5VDC and battery input PWM boost converter applications. MOSFETs featuring "logic level" gate thresholds are the most likely candidates for the PWM switch as opposed to using standard devices which typically require a gate voltage near 12 volts to be fully on. Currently, many popular N channel MOSFETs are available with logic level gate inputs as an option. Note that many logic level FETs have maximum gate voltage ratings of +/- 10V as opposed to +/- 20V for most conventional FETs which limits their application. Also note that the UCC 380x devices will require a current limited supply when used above 12 volts from a low impedance source.

A basic current mode controlled boost converter application circuit is shown. Typical component values for 250 kHz operation are listed in the following tables for a 12V and 24V output applications. The boost converter design equations are summarized below.

BOOST DESIGN SUMMARY:

(Discontinuous inductor current)

$$Vout = Vin \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Iin = Iout \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Ip = 2 \times Iin \times \frac{t(period)}{t(on)}$$

$$Ip = \frac{2 \times t(period) \times Iout \times (t(on) + t(off))}{[t(on) \times t(off)]}$$

$$\text{where } t(period) = \frac{1}{F(switching)}$$

$$L = \frac{Vout\ minus\ Vin\ (min) \times t(off)]}{Ip}$$

$$C\ out = \frac{(Ip \times t(off)\ max)}{2 \times dVout}$$

$$ESR\ (max) = \frac{dVout}{Ip}$$

9

BOOST CONVERTER DESIGN TABLE 1

VIN = 4.5 to 10 VDC

VOUT = 12 VDC

IOUT = 0.2, 0.4, 1 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	3A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	1.8uH
PCH-(1)	27-123	27-682	27-182
Cout (2)	100uF	300uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1* (3)	2A/50V RFL2NO5L	IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 2

VIN = 4.5 to 10 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	3A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	3.9uH
PCH-(1)	27-123	27-682	27-392
Cout (2)	100uF	200uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1* (3)	2A/50V RFL2NO5L	8A/50V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 3

VIN = 10 to 18 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	22uH	12uH	3.9uH
PCH-(1)	27-223	27-123	27-392
Cout (2)	100uF	200uF	500uF
Rcs(ohm)	0.2	0.1	0.066
Q1* (3)	3A/60V IRFF113	3A/60V IRFF113	IRFF133

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

BUCK REGULATOR

The buck regulator is a more difficult design challenge than the boost converter due to the high side switch. A transformer coupled gate drive is typically required to deliver drive pulses to the switch, which requires about ten volts above the input voltage for proper drive. Current mode control further complicates the design by requiring a current transformer to level shift the high side current sense signal down to the ground based input of the IC. In many applications, direct duty cycle control (voltage mode) can be used to simplify the design although overcurrent protection is lost with common ground applications.

Several examples of common buck regulator application circuits are shown below. Direct duty cycle control is used for simplicity, however current mode control can be easily adapted as shown in the example. Tables listing component values and typical part numbers have been included.

DESIGN EQUATIONS:

$Vout = Vin * D$ (duty cycle)

$$\text{where } D = \frac{T(on)}{T(period)}$$

$$L = Vout \times \frac{t(off)}{d\,Io}$$

where: Delta Io is the inductor ripple current and equal to one-half of the minimum output current. Minimum output current has been selected as 10% of the full load current

$$Ipk = Io + \frac{d\,Io}{2}$$

$$Iin(DC) = Iout * D$$

$$Cout = \frac{d\,Io}{(8 \times F \times d\,Vout)}$$

where F is the switching frequency and Δ Vout is the output ripple voltage

BUCK REGULATOR DESIGN TABLES

TABLE 4

VIN = 4.5 to 10 VDC

VOUT = 3.3 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/20V 1N5820	12A/45V 12TQ045	12A/45V 12TQ045
L	39uH	22uH	6.8uH
PCH-(1)	27-393	45-223	45-682
Cout (2)	2uF	4.7uF	10uF
Q1* (3)	8A/60V IRLZ14	8A/60V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number. LOGIC LEVEL gate threshold.

TABLE 5

VIN = 10 to 18 VDC

VOUT = 5 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/40V 1N5822	3A/40V 1N5822	12A/40V 12TQ045
L	120uH	39uH	22uH
PCH-(1)	27-1243	45-393	45-223
Cout (2)	2uF	5uF	10uF
Q1* (3)	4A/50V IRF9Z12	8A/50V IRF9Z22	12A/50V IRF9Z30

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number. LOGIC LEVEL gate threshold.

TABLE 6

VIN = 10 to 18 VDC

VOUT = 9 VDC

IOUT = 1, 3, 5 ADC

IOUT	1A	3A	5A
D1	3A/40V 1N5822	3A/40V 1N5822	12A/40V 12TQ045
L	39uH	12uH	6.9uH
PCH-(1)	27-293	27-123	27-682
Cout (2)	1uF	3uF	5uF
Q1* (3)	4A/50V IRF9Z12	8A/50V IRF9Z22	12A/50V IRF9Z30

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESL.
NOTE 3: MOSFET ratings and part number. LOGIC LEVEL gate threshold.

OFF-LINE APPLICATIONS: FORWARD AND FLYBACK CONVERTERS

Several benefits can be realized in off-line applications by using the low current, UC380x BiCMOS PWM controllers. First, the IC can be powered from a resistor to the rectified input voltage source, eliminating the bootstrap winding. This applies to most low frequency applications (50kHz) where the DC supply current required for the gate drive is low. Soft start of the power supply and delayed restart following a fault requires no external parts.

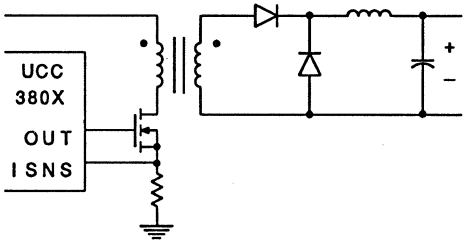


Figure 31

The internal leading edge blanking eliminates filtering of the current sense signal. Also, the ICs undervoltage lockout thresholds, internal Vcc shunt regulator and active low totem pole output eliminate any problematic gate drive operation.

The basic schematic of a forward converter is shown in figure 31, and a flyback is shown in figure 32. In each, the UCC3804 limits the maximum duty cycle to 50% by internal logic, allowing time for the main transformer to reset. Applications which utilize higher maximum duty cycles, for example 65%, should use the UCC 3802 device without the internal toggle flip flop.

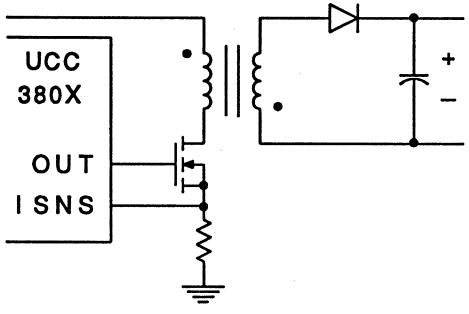


Figure 32

UCC380X OTHER APPLICATIONS: UNIVERSAL SYNC GENERATOR

The UCC3803 can be used as a synchronization (SYNC) pulse generator and driver for a variety of applications. Basically, one circuit shown uses the leading edge blanking duration as the SYNC output pulse width. The current limit input is biased at 1.25 volts to terminate the output pulse immediately after the ICs internal blanking pulse width. The oscillator is resistively programmed to a DC level of 1.25 volts also, midway between its upper and lower thresholds. When a TTL compatible SYNC pulse is injected, the amplitude at the oscillator input is raised above its upper threshold. This turns on the internal discharge circuitry which pulls the pin to about 0.2 volts, crossing the lower oscillator threshold. Once this occurs, the discharge transistor is turned off and the ICs output is turned on, generating the SYNC pulse. Note that the current sense input is biased to turn the ICs output off following the leading edge blanking duration, which is used to program the SYNC output pulse width. This 100 nanosecond duration is ideal for synchronizing most PWMs used today with the technique shown.

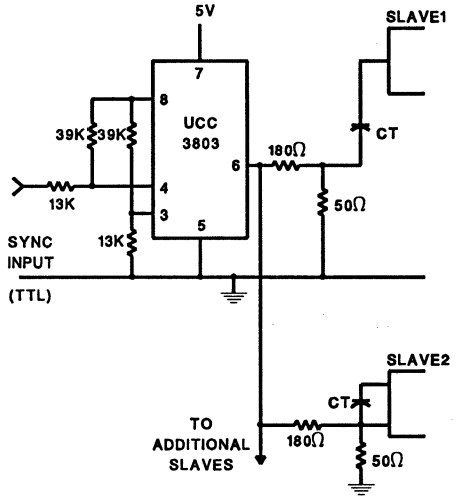


Figure 33

This circuit can be adapted to generate other width pulses with minor modifications. A capacitor can be added across the lower resistor in the divider network to the current sense input for extending the pulse width. Note that the voltage must be limited below 1.4 volts or a full cycle soft start will be incurred. Also, this capacitor must be discharged before the beginning of each pulse for proper timing

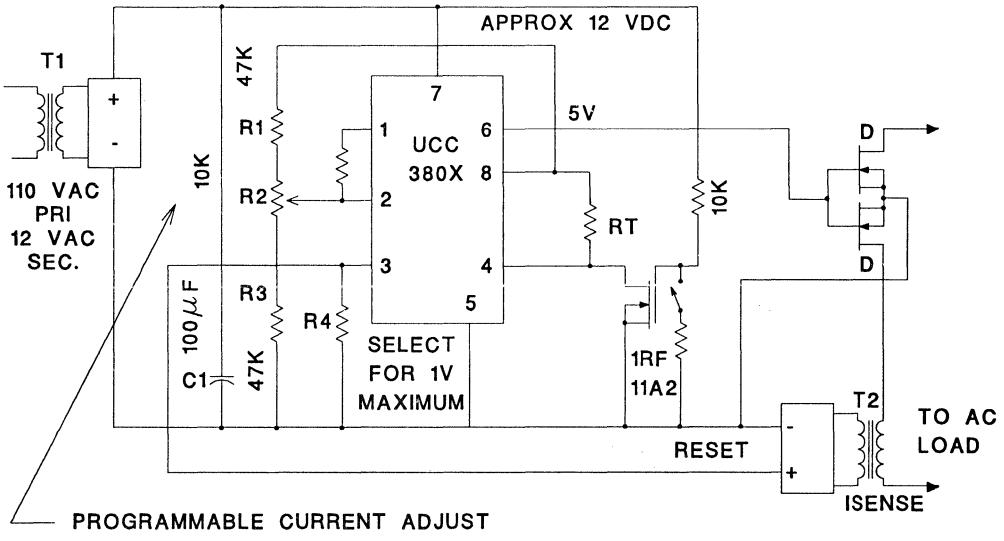


Figure 34

to occur. One recommendation is to diode couple the current sense input to the oscillator Rt/Ct pin. External circuits can also be used for more precise programming.

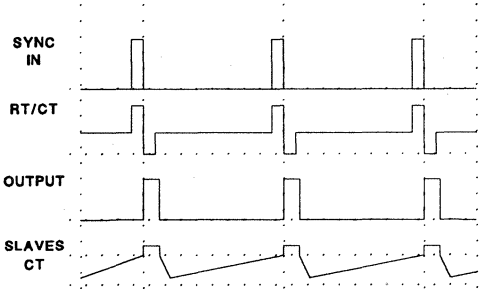


Figure 35

VFO APPLICATIONS

Members of the UCC380x family of devices are adaptable for use in variable frequency applications. The most direct means of accomplishing this is to vary the charging current to the oscillator timing capacitor. Note that the minimum compliance voltage of the current source must exceed the upper oscillator threshold of approximately 2.7 volts. The VFO current source can be generated by an external op-amp for general purpose applications as shown.

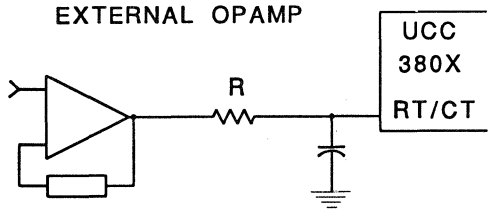


Figure 36

Some VFO applications can utilize the ICs internal error amplifier to vary the frequency over a programmed minimum and maximum frequency range. This is done by programming the minimum frequency by a resistor to Vref. Another current sink/source is formed by a resistor to the E/A output. This arrangement performs frequency modulation as the E/A output voltage is varied. Applications which require a fixed 50% duty cycle at varying frequencies, electronic ballasts, for ex-

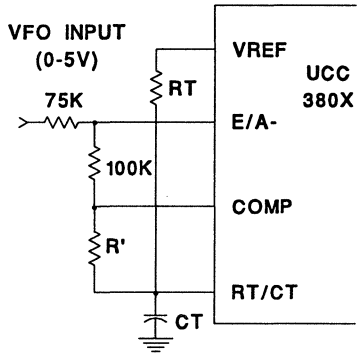


Figure 37

ample, should use the UCC3804 or UCC3805 devices. Output frequency from these will be one-half of the ICs oscillator due to the internal divide-by-two gating circuitry.

FIXED OFF-TIME APPLICATIONS

Obtaining a fixed off-time, variable on-time control technique is easily implemented with the UCC380x family. The oscillator Rt/Ct timing components are used to generate the off-time rather than the operating frequency. Implementation is shown in the corresponding figure.

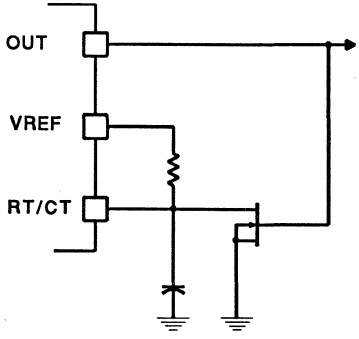


Figure 38

FULL DUTY CYCLE APPLICATIONS

Any of the UCC380x PWM controllers can be used at full (100%) duty cycle. This mode of operation may be required in certain applications, including DC switch drivers. Implementation requires "freezing" the oscillator so that the output stays high until it is time to turn off. Switch Q1 insures that the PWM output is high when switch Q2 is activated to stop the oscillator. Current limiting can still be accomplished by using the current sense feature of the IC, in addition to modulating the peak current via the error amplifier.

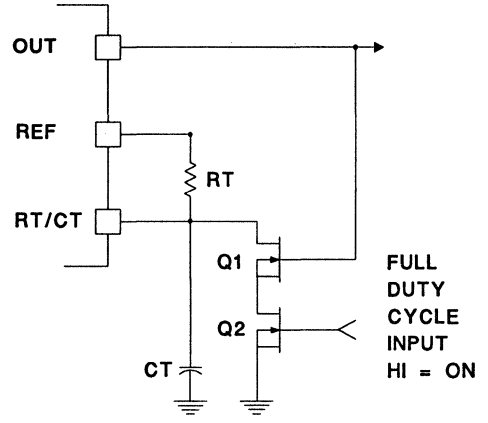


Figure 39

HIGH SPEED, PROGRAMABLE ELECTRONIC CIRCUIT BREAKER

A high speed, programmable electronic circuit breaker can be built using the UCC380x family to perform the control and MOSFET drive functions. Basically, back-to-back power MOSFETS are used as the switching element although an SCR, TRIAC or bipolar switch can also be used. The MOSFETS are connected with the sources tied together to simplify the gate drive while providing a blocking path to current in either direction. Current limiting for an AC supply requires a current transformer, also shown, which can be simplified to a resistor for use in DC input applications. The current sense input to the IC can either be biased up for lower power loss in the current sense network, or programmed by adjusting the error amplifier output voltage to yield a similar result.

SWITCHING COMPONENT NOTES: P CHANNEL MOSFET SWITCHES

Logic level P channel MOSFETs are unavailable today which limits their applications to those with input voltages greater than about ten volts for proper gate drive. The P channel switch will also require a small N channel device to invert its gate drive command, due to the active high output of the PWM. High speed PNP transistors are also a suitable choice for some applications.

N CHANNEL MOSFET SWITCHES

Proper gate drive for N channel switches will require a supply voltage which is several volts above the input voltage. This is not a problem in five volt input applications using logic level FETs if a nine volt (or higher) supply is also available. If not, one option is to construct a very low power boost converter to generate the nine volt supply to power the IC and gate drive. The boost converter switch can be driven from the UCC380x output which is switching the main output. Small, inexpensive surface mount inductors, switches and diodes are readily available. Another possibility is to build a charge pump circuit driven from the PWM output as shown, provided that only a few volts of headroom are required.

GATE DRIVE TRANSFORMER

Higher input voltage applications will require a gate drive transformer due to 12 volt maximum supply rating of the UCC 380x IC family. A small ferrite toroid with two windings and minimal insulation is typically used. A capacitor is placed in series with the primary and is needed for proper reset of the core. The DC offset introduced by the capacitor will effect the primary to secondary turns ratio of the transformer which is dependant on the application. A PULSE Engineering (phone 619-268-2400) model PE-64973 can be employed in a most Buck regulator designs.

CURRENT SENSE TRANSFORMER

A current sense transformer is required in the buck regulator application for current mode control. This transformer is used to level shift the current signal from the high side input supply to the ground referenced PWM circuitry. A high turns ratio should be incorporated to reduce power dissipation. Parasitic noise can be minimized by inserting the transformer in series with the drain of the power switch as opposed to its source. A PULSE Engineering (phone 619-268-2400) model PE-64978 current transformer with a one turn primary and 50 turn secondary can be used in most applications.

ADDITIONAL INFORMATION

1. UNITRODE Application Note U-100A;
" The UC3842/3/4/5 Series of Current Mode PWM ICs" :
   - UC3842/3/4/5 PWMs
   - Applications Information

2. UNITRODE Application Note U-111;
" Practical Considerations in Current Mode Power Supplies" ;
   - Fixed OFF-Time Implementation
   - Full Duty Cycle
   - Paralleling Power Supplies
   - Shutdown Techniques
   - Slope Compensation (implementation)
   - Soft Start
   - Synchronization
   - Variable Frequency Operation
   - Voltage Mode Operation

3. UNITRODE Application Note U-96A
"A 25 Watt Off-Line Flyback Switching Regulator":
   - Flyback Converter Design

4. UNITRODE Application Note U-97
"Modelling, Analysis and Compensation of the Current Mode Converter "
   - Current Mode Control
   - Slope Compensation

9

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UC3854 Controlled Power Factor Correction Circuit Design

PHILIP C. TODD

ABSTRACT

This Application Note describes the concepts and design of a boost preregulator for power factor correction. This note covers the important specifications for power factor correction, the boost power circuit design and the UC3854 integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. This design procedure is directly applicable to the UC3854A/B as well as the UC3854. The recommendations in Unitrode Design Note DN-39 cover other areas of the circuit and, while not discussed here, must be considered in any design. This application note supersedes Application Note U-125 "Power Factor Correction With the UC3854."

INTRODUCTION

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor.

The most general definition of power factor is the ratio of real power to apparent power.

$$PF = \frac{P}{(Vrms \times Irms)} \quad \text{or} \quad PF = \frac{Watts}{V.A.}$$

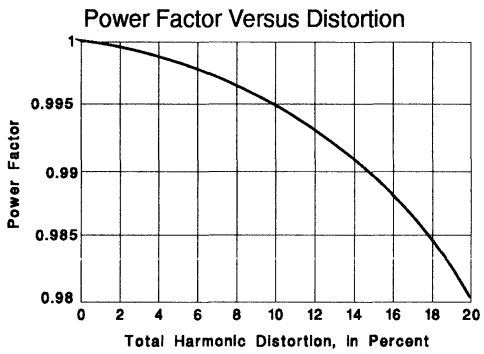
Where P is the real input power and Vrms and Irms are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case. If the load is a pure resistance the real power and the product of the RMS voltage and current will be the same and the power factor will be 1.0. If the load is not a pure resistance the power factor will be below 1.0.

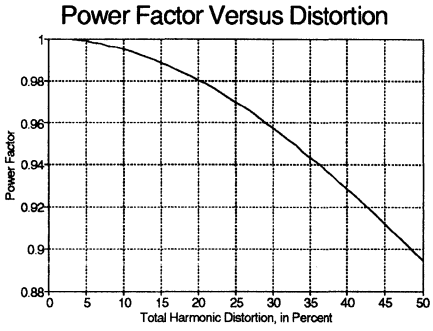
Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

$PF = \text{Cos}\ \theta$

The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feedforward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current without increasing the total power being drawn. A non-linear load will therefore have a poor power factor because the RMS value of the current is high but the total power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from





Harmonic Order	Permissible current	Maximum permissible current
n	mA/W	A
Odd harmonics		
3	3.4	2.30
5	1.9	1.14
7	1.0	0.78
9	0.5	0.40
11	0.35	0.33
13	0.3	0.21
15 up	3.85/n	$0.15 \times \frac{15}{n}$
Even harmonics		
2	1.8	1.08
4	0.7	0.42
6	0.5	0.30
>8	$\frac{3}{n}$	$\frac{1.80}{n}$

Table 1

several sources: the feedforward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. But power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

The trend among the world standards organizations responsible for power quality is to specify maximum limits for the amount of current allowed at each of the harmonics of the line frequency. IEC 555-2 specifies each harmonic up through and beyond the 15th and the amount of current permissible at each. Table 1 lists the requirements for IEC 555-2 as of the time of this writing. There are two parts to the specification, a relative distortion and an absolute distortion maximum. Both limits apply to all equipment. This table is included here as an example of a line distortion specification. It is not intended to be used for design purposes. The IEC has not finalized the requirements of IEC 555 at this time and major changes are possible.

Active Power Factor Correction

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either

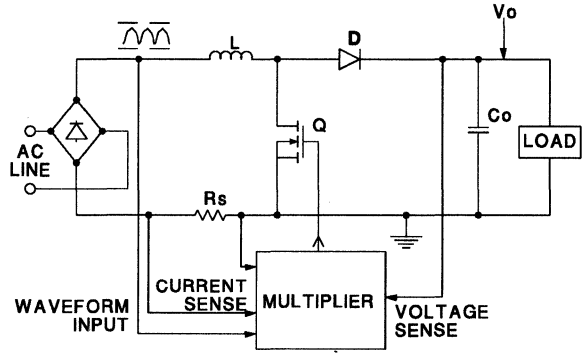


Figure 1

Basic Configuration of High Power Factor Control Circuit

peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854. Peak current mode control has a low gain, wide bandwidth current loop which generally makes it unsuitable for a high performance power factor corrector since there is a significant error between the programming signal and the current. This will produce distortion and a poor power factor.

Average current mode control is based on a simple concept. An amplifier is used in the feedback loop around the boost power stage so that input current tracks the programming signal with very little error. This is the advantage of average current mode control and it is what makes active power factor correction possible. Average current mode control is relatively easy to implement and is the method described here.

A block diagram of a boost power factor corrector circuit is shown in Figure 1. The power circuit of a

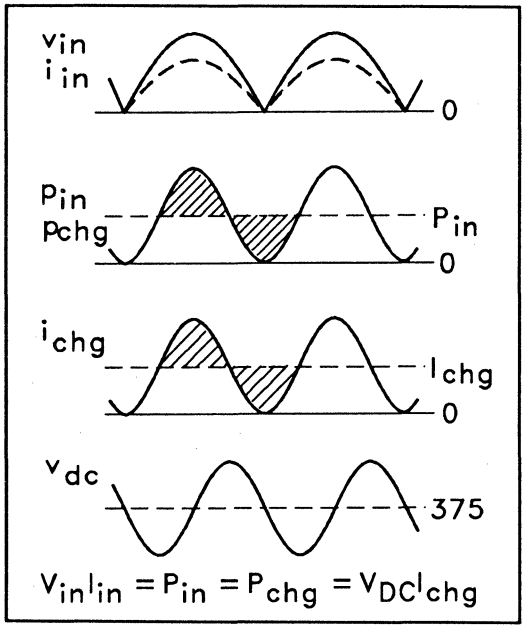


Figure 2. Preregulator Waveforms

boost power factor corrector is the same as that of a dc to dc boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.

The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. This is shown in Figure 2. The top waveform shows the voltage and the current into the power factor corrector and the second waveform shows the flow of energy into and out of the output capacitor. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow. The third waveform in Figure 2 shows the charging and discharging current. This current has a different shape from the input current and is almost entirely at the second harmonic of the AC line voltage. This flow of energy into and out of the capacitor results in ripple voltage at the second harmonic also and this is shown in the fourth waveform in Figure 2. Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

Control Circuits

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Figure 3 is a block diagram which shows the basic control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called Imo for multiplier output current. The multiplier input from the rectified line voltage is shown as a current in Figure 3 rather than as a voltage signal because this is the way it is done in the UC3854.

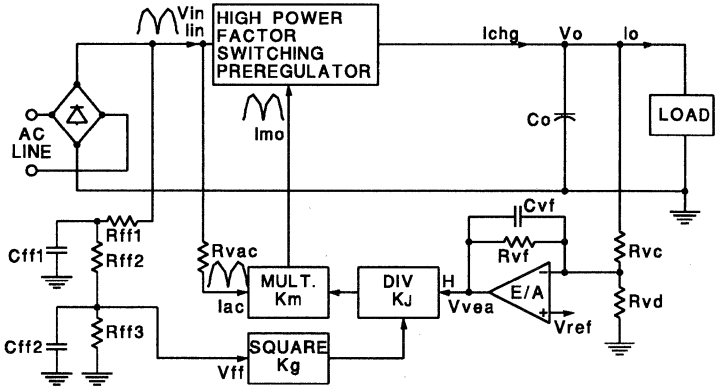


Figure 3. High Power Factor

Figure 3 shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feedforward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage (Vvea).

The current programming signal must match the rectified line voltage as closely as possible to maximize the power factor. If the voltage loop bandwidth were large it would modulate the input current to keep the output voltage constant and this would distort the input current horribly. Therefore the voltage loop bandwidth must be less than the input line frequency. But the output voltage transient response must be fast so the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keep the loop gain constant so the bandwidth can be as close as possible to the line frequency to minimize the transient response of the output voltage. This is especially important for wide input voltage ranges.

The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control. The output of the voltage error amplifier actually controls the power delivered to the load. This can be seen easily from an example. If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feedforward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector. This can be used to limit the maximum power which the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

Input Distortion Sources

The control circuits introduce both distortion and displacement into the input current waveform. These errors come from the input diode bridge, the multiplier circuits and ripple voltage, both on the output and on the feedforward voltage.

There are two modulation processes in an active power factor corrector. The first is the input diode bridge and the second is the multiplier, divider, squarer circuit. Each modulation process generates cross products, harmonics or sidebands between the two inputs. The description of these mathematically can be quite complex. Interestingly enough, however, the two modulators interact and one becomes a demodulator for the other so that the result is quite simple. As shown later, virtually all of the ripple voltages in an active power factor corrector are at the second harmonic of the line frequency. When these voltages go through the multiplier and get programmed into the input current and then go through the input diode bridge the second harmonic voltage amplitude results in two frequency components. One is at the third harmonic of the line frequency and the other is at the fundamental. Both of these components have an amplitude which is half of the amplitude of the original second harmonic voltage. They also have the same phase as the original second harmonic. If the ripple voltage is 10% of the line voltage amplitude and is phase shifted 90 degrees the input current will have a third harmonic which is 5% of the fundamental and is shifted 90 degrees and a fundamental component which is 5% of the line current and is displaced by 90 degrees.

The feedforward voltage comes from the rectified AC line which has a second harmonic component that is 66% of the amplitude of the average value. The filter capacitors of the feedforward voltage divider greatly attenuate the second harmonic and effectively remove all of the higher harmonics but some of the second harmonic is still present at the feedforward input. This ripple voltage is squared by the control circuits as shown in Figure 3. This doubles the amplitude of the ripple since it is riding on top of a large DC value. The divider process is transparent to the ripple voltage so it passes on to the multiplier and eventually becomes third harmonic distortion of the input current and a phase displacement. The doubling action of the squarer means that the amplitude of the input current distortion in percent is the same as the amplitude of the ripple voltage, in percent, at the feedforward input.

Needless to say, the feedforward ripple voltage must be kept small to achieve a low distortion input current. The ripple voltage could be made small with a single pole filter with a very low cutoff frequency. However, fast response to changes of the input voltage is also desirable so the response time of the filter must be fast. These two requirements are, of course, in conflict and a compromise must be found. A two pole filter on the feedforward input has a faster transient response than a single pole filter for the same amount of ripple attenuation. Another advantage of the two pole filter has is that the phase shift is twice that of the single pole filter. This results in 180 degrees of phase shift of the second harmonic and brings both the resulting third harmonic and the displacement component of the input current back in phase with the voltage. A second harmonic ripple voltage of 3% at the feedforward input results in a 0.97 power factor just from the displacement component if a single pole filter is used for the feedforward voltage. With a two pole filter there is no displacement component to the power factor because it is in

phase with the input current. The third harmonic component of the input current resulting from the second harmonic at the feedforward input will have the same amplitude as the second harmonic ripple voltage. If 3% second harmonic is present on the feedforward voltage the line current waveform will contain 3% third harmonic distortion.

The output voltage has ripple at the second harmonic due to the ripple current flowing through the output capacitor. This ripple voltage is fed back through the voltage error amplifier to the multiplier and, like the feedforward voltage, programs the input current and results in second harmonic distortion of the input current. Since this ripple voltage does not go through the squarer the amplitude of the distortion and displacement are each half of the amplitude of the ripple voltage. The ripple voltage at the output of the voltage error amplifier must be in phase with the line voltage for the displacement component to be in phase. The voltage error amplifier must shift the second harmonic by 90 degrees so that it will be in phase with the line voltage.

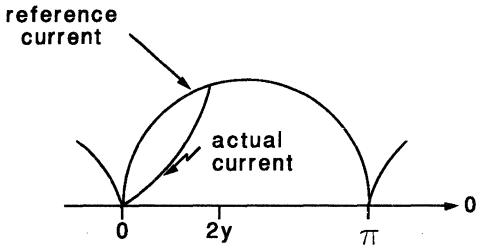


Figure 4. Cusp Distortion

The voltage loop of a boost converter with average current mode control has a control to output transfer function which has a single pole roll off characteristic so it could be compensated with a flat gain error amplifier. This produces a very stable loop with 90 degrees of phase margin. However, it provides less than optimum performance. The ripple voltage on the output capacitor is out of phase with the input current by 90 degrees. If the error amplifier has flat gain at the second harmonic frequency the distortion and displacement generated in the input current will be 90 degrees out of phase with the rectified AC line. The power factor can be improved by introducing phase shift into the voltage error amplifier response. This shifts the displacement component of the power factor back into alignment with the input voltage and increases the power factor. The amount of phase shift which can be added is determined by the need to keep the voltage loop stable. If the phase margin is reduced to 45 degrees the phase at the second harmonic will be very close to 90 degrees and this brings the displacement component back in phase with the input voltage.

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin.

Cusp Distortion

Cusp distortion occurs just after the AC line input has crossed zero volts. At this point the amount of current which is required by the programming signal exceeds the available current slew rate. When the input voltage is near zero there is very little voltage across the inductor when the switch is closed so the current cannot ramp up very quickly so the available slew rate is too low and the input current will lag behind the desired value for a short period of time. Once the input current matches the programmed value the control loop is back in operation and the input current will follow the programming signal. The length of time that the current does not track the programmed value is a function of the inductor value. The smaller the inductor value the better the tracking and the lower the distortion but the smaller inductor value will have higher ripple current. The amount of distortion generated by this condition is generally small and is mostly higher order harmonics. This problem is minimized by a sufficiently high switching frequency.

UC3854 Block Diagram

A block diagram of the UC3854 is shown in Figure 5 and is the same as the one in the device data sheet. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of Figure 5 contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsens. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

The output of the voltage error amplifier, Vvea, is available on pin 7 of the UC3854 and it is also an input to the multiplier. The other input to the multiplier is pin 6, Iac, and this is the input for the programming wave shape from the input rectifiers. This pin is held at 6.0 volts and is a current input. The feedforward input, Vff, is pin 8 and its value is squared before being fed into the divider input of the multiplier. The Iset current from pin 12 is also used in the multiplier to limit the maximum output current. The output current of the multiplier is Imo and it flows out of pin 5 which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin 4, the Isens pin. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin 14. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin 16. The output voltage is clamped internally to the UC3854 at 15 volts so that power MOSFETs will not have their gates over driven. An emergency peak current limit is provided on pin 2 and it will shut the output pulse off when it is pulled slightly below ground. The reference voltage output is connected to pin 9 and the input voltage is connected to pin 15.

DESIGN PROCESS

Power Stage Design

This analysis of the power stage design makes use of a 250W boost converter as an example. The control circuit for a boost power factor corrector does not change much with the power level of the converter. A 5000 watt power factor corrector will have almost the same control circuits as a 50 watt

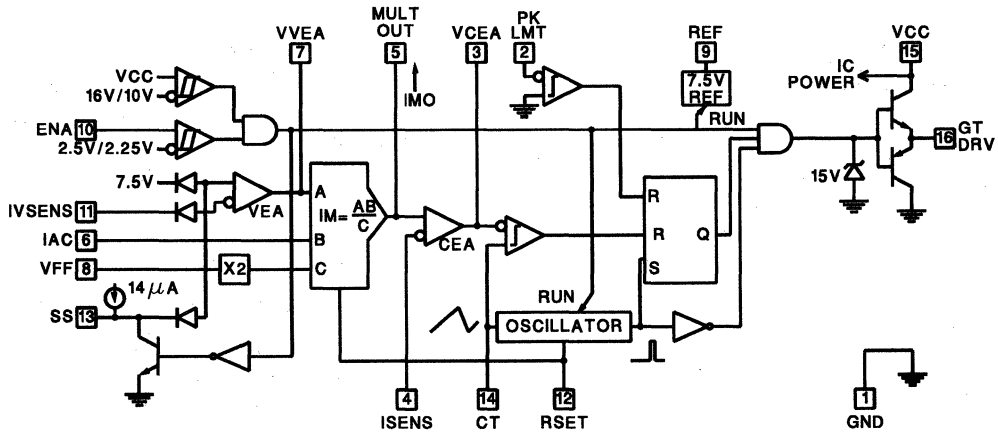


Figure 5. UC3854 Block Diagram

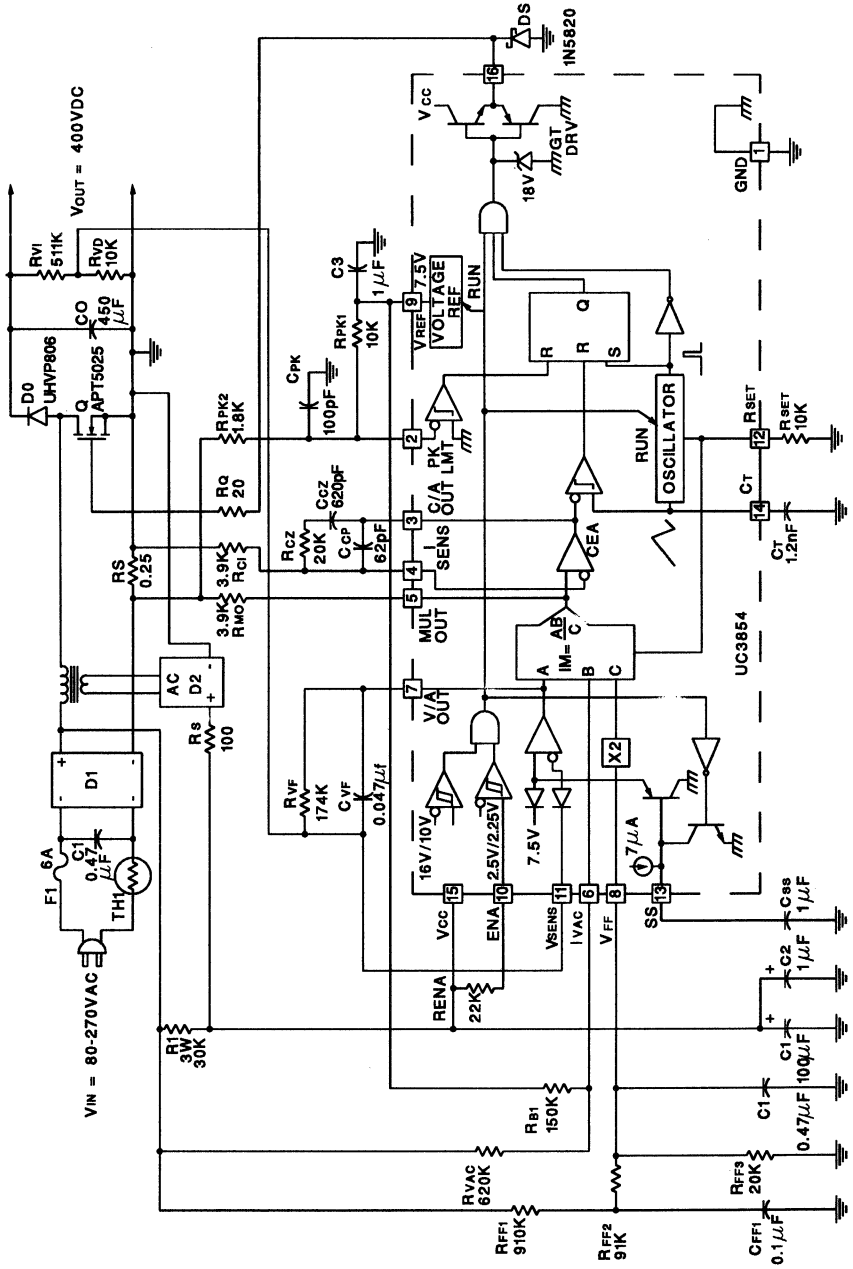


Figure 6.
Complete Schematic of 250W Power Factor Preregulator

corrector. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design process is the same and the power stage is scalable a 250 watt corrector serves well as an example and it can be readily scaled to higher or lower output levels. Figure 6 is the schematic diagram of the circuit. Please refer to this schematic in the discussion of the design process which follows.

Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

Maximum power output: 250W

Input voltage range: 80-270Vac

Line frequency range: 47-65Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20KHz to 300KHz proves to be an acceptable compromise. The example converter uses a switching frequency of 100KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak

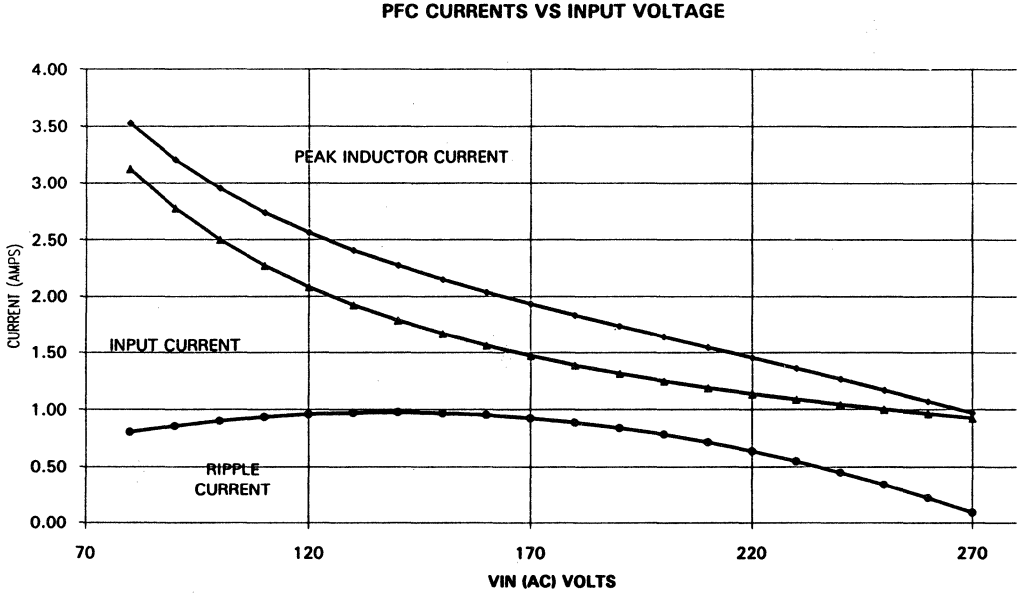


Figure 7

current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I\,line\,(pk) = \frac{\sqrt{2} \times P}{Vin\,(min)}$$

For the example converter the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 7 is a graph of the peak to peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{Vo - Vin}{Vo}$$

$$L = \frac{Vin \times D}{fs \times \Delta I}$$

Where ΔI is the peak-to-peak ripple current. In the example 250W converter D=0.71, ΔI=900ma, and L=0.89mH. For convenience the value of L is rounded up to 1.0mH.

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2μF per watt of output. In our 250W example the output capacitor is 450μF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2μF per watt, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capcitance value in terms of the hold-up time.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - Vo\,(min)^2}$$

Where Co is the output capacitor, Pout is the load power, Δt is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. For the example converter Pout is 250W, Δt is 64msec, Vo is 400V and Vo(min) is 300V so Co is 450μF.

Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation. The choice of these components is beyond the scope of this Application Note. The switch must have a current rating at least equal to the maximum peak current in

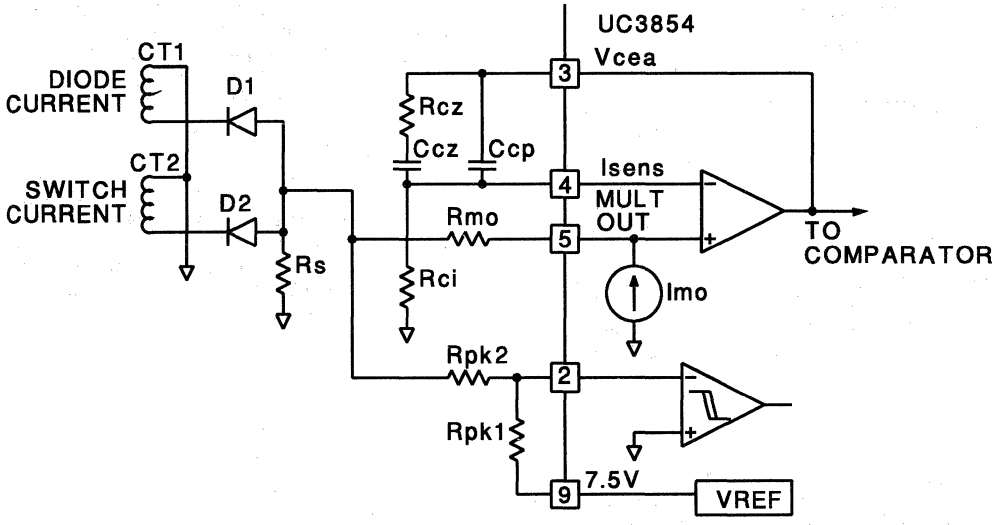


Figure 8.
Current Transformers Used with Negative Output

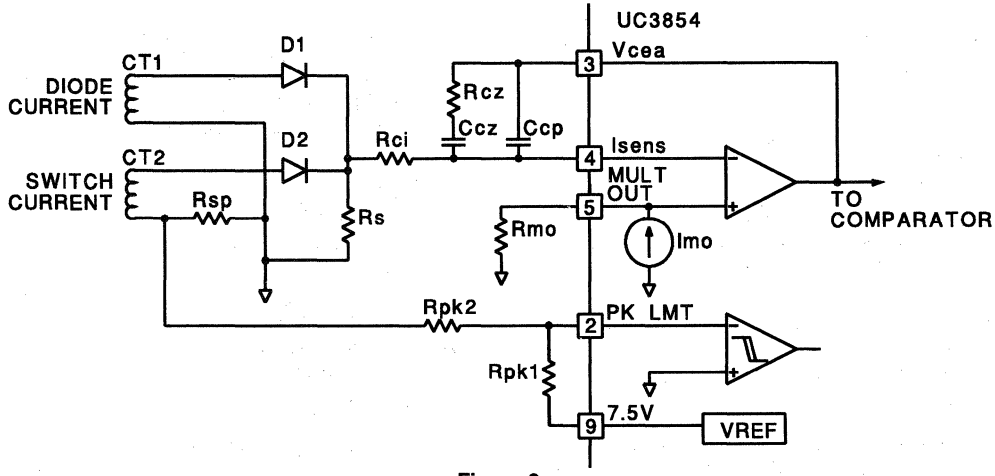


Figure 9.
Current Transformers Used with Positive Output

the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the example circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 500Vdc breakdown and 23Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 8, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 9, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figures 8 and 9 respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 9) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 6) so the inverting input to the current error amplifier (pin 4) is connected to ground through Rci. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be zero. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor Rmo). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be zero because it is connected through Rci to ground.

The voltage across Rs, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 volt or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25 ohm resistor was chosen for Rs in the example converter and at the worst case peak current of 5.6 amps gives a maximum voltage of 1.40V peak.

Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor.

The equation for the voltage divider is given below:

$$Rpk2 = \frac{Vrs \times Rpk1}{Vref}$$

Where Rpk1 and Rpk2 are the resistors of the voltage divider, Vref is 7.5 volts on the UC3854, and Vrs is the voltage across the sense resistor Rs at the current limit point. The current through Rpk2 should be around 1mA. The peak current limit in the example circuit is set at 5.4 amps with an Rpk1 of 10K and Rpk2 of 1.8K. A small capacitor, Cpk, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current Iac (pin 6), the feedforward voltage Vff from the input (pin 8), and the voltage error amplifier output voltage Vvea (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

Where Km is a constant in the multiplier and is equal to 1.0, Iac is the programming current from the rectified input voltage, Vvea is the output of the voltage error amplifier and Vff is the feedforward voltage.

Feedforward Voltage

Vff is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a Vff range of 1.4 to 4.5 volts. The UC3854 has an internal clamp which limits the effective value of Vff to 4.5 volts even if the input goes above that value. The voltage divider for the Vff input has three resistors (Rff1, Rff2 and Rff3 - see Figure 6) and two capacitors (Cff1 and Cff2) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270Vac the average value of a half sine will be 243Vdc and the peak will be 382V.

The Vff voltage divider has two DC conditions to meet. At high input line voltage Vff should not be greater than 4.5 volts. At this voltage the Vff input clamps so the feedforward function is lost. The voltage divider should be set up so that Vff is equal to 1.414 volts when Vin is at its low line value and the upper node of the voltage divider, Vffc, should be about 7.5 volts. This allows Vff to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the Vff input goes below 1.414 volts. The Vff input should always be set up so that Vff is equal to 1.414 volts at the minimum input voltage. This may cause Vff to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have Vff clip at the high end rather than to have the multiplier output clip on the low end of the range. If Vff clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of Vff is 4.5 volts. If Rff1, the top resistor of the divider, is 910K and Rff2, the middle resistor, is 91K and Rff3, the bottom resistor, is 20K the maximum value of Vff will be 4.76 volts when the input voltage is 270Vac RMS and the DC average value will be 243 volts. When the input voltage is 80Vac RMS the average value is 72 volts and Vff is 1.41Vdc. Also at Vin=80Vac the voltage at the upper node on the voltage divider, Vffc, will be 7.83 volts. Note that the high end of the range goes above 4.5 volts so that the low end of the range will not go below 1.41 volts.

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, Vvea, is clamped inside the UC3854 at 5.6 volts. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given Vvea voltage regardless of line voltage changes. If 5.0V is established as the maximum normal operating level then 5.6V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of Vff at 1.414 volts. This can be seen by plugging these values into the equation for the multiplier output current given above. When Vff is large the inherent errors of the multiplier are magnified because Vvea/Vff becomes small. If the application has a wide input voltage range and if a very low harmonic distortion

is required then Vff may be changed to the range of 0.7 to 3.5 volts. To do this an external clamp MUST be added to the voltage error amplifier to hold its output below 2.00 volts. In general, however, this is not a recommended practice.

Multiplier Input Current

The operating current for the multiplier comes from the input voltage through Rvac. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6mA. At high line the peak voltage for the example circuit is 382Vdc and the voltage on pin 6 of the UC3854 is 6.0Vdc. A 620K value for Rvac will give an Iac of 0.6mA maximum. For proper operation near the cusp of the input waveform when Vin=0 a bias current is needed because pin 6 is at 6.0Vdc. A resistor, Rb1, is connected from Vref to pin 6 to provide the small amount of bias current needed. Rb1 is equal to Rvac/4. In the example circuit a value of 150K for Rb1 will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for Imo, given above, for this condition. The peak value of Iac will be 182 microamps when Vin is at low line. Vvea will be 5.0 volts and Vff will be 2.0. Imo will then be 365 microamps maximum. Imo may not be greater than twice Iac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The Iset current places another limitation on the multiplier output current. Imo may not be larger than 3.75 / Rset. For the example circuit this gives Rset = 10.27K maximum so a value of 10K is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. Rmo, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be zero under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 amps in the example circuit and the current sense resistor is 0.25 ohms so the peak voltage across the sense resistor is 1.4 volts. The maximum multiplier output current is 365 microamps so the summing resistor, Rmo, must be 3.84K and a 3.9K resistor is chosen.

Oscillator Frequency

The oscillator charging current is Iset and is determined by the value of Rset and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$Ct = \frac{1.25}{Rset \times fs}$$

Where Ct is the value of the timing capacitor and fs is the switching frequency in Hertz. For the example converter fs is 100KHz and Rset is 10K so Ct is 0.00125µF.

Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (Rs) forming a low pass filter. The equation for the control to input current transfer function is:

$$\frac{Vrs}{Vcea} = \frac{Vout \times Rs}{Vs \times sL}$$

Where Vrs is the voltage across the input current sense resistor and Vcea is the output of the current error amplifier. Vout is the DC output voltage, Vs is the peak-to-peak amplitude of the oscillator ramp, sL is the impedance of the boost inductor (also jwL), and Rs is the sense resistor (with a current transformer it will be Rs/N). This equation is only valid for the region of interest between the resonant frequency of the filter (LCo) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (Vin=0) the inductor current is given by the ratio of the converter output voltage and the inductance (Vo/L). This current flows through the current sense resistor Rs and produces a voltage

with the slope VoRs/L (with current sense transformers it will be VoRs/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Where fci is the current loop crossover frequency and Rcz/Rci is the gain of the current error amplifier. This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400Vdc and the inductor is 1.0mH so the down slope of inductor current is 400mA per microsecond. The current sense resistor is 0.25 ohms so the input to the current error amplifier is 100mV per microsecond. The oscillator ramp of the UC3854 has a peak to peak value of 5.2V and the switching frequency is 100KHz so the ramp has a slope of 0.52 volts per microsecond. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (Rci) value of 3.9K the feedback resistance (Rcz) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9KHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45 degrees. If the zero is lower in frequency the phase margin will be greater. A 45 degree phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of Rcz. The equation is: Ccz = 1 / (2π x fci x Rcz). The example converter has Rcz=20K and fci=15.9KHz so Ccz=500pF. A value of 620pF was chosen to give a little more phase margin.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62pF capacitor for Ccp which gives a pole at 128KHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62pF is adequate in this case.

Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90 degrees. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$Vopk = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), fr is the ripple frequency which is the second harmonic of the input line frequency, Co is the value of the output capacitance and Vo is the DC output voltage. The example converter has a peak ripple voltage of 1.84Vpk.

The amount of distortion which the ripple contributes to the input must be decided next. This deci-

sion is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range (ΔVvea) of 1.0 to 5.0 volts so the peak ripple voltage at the output of the voltage error amplifier is give by Vvea(pk) = %Ripple x ΔVvea. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, Gva, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter Gva is 0.0326.

The criteria for the choice of Rvi, the next step in the design process, are reasonably vague. The value must be low enough so that the opamp bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511K resistor was chosen for Rvi and it will have power dissipation of about 300mW.

Cvf, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$Cvf = \frac{1}{2\pi fr \times Rvi \times Gva}$$

The example converter has a Cvf value of 0.08μF. If this value is rounded down to Cvf=0.047μF the phase margin will be a little better with only a little more distortion so this value was chosen.

The output voltage is set by the voltage divider Rvi and Rvd. The value of Rvi is already determined so Rvd is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example Rvd=10K will give an output voltage of 390Vdc. This could be trimmed up to 400VDC with a 414K resistor in parallel with Rvd but for this application 390Vdc is acceptable. Rvd has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$Gbst = \frac{Pin \times Xco}{\Delta Vvea \times Vo}$$

Where Gbst is the gain of the boost stage including the multiplier, divider and squarer, Pin is the average input power, Xco is the impedance of the output capacitor, ΔVvea is the range of the voltage error amplifier output voltage (4 volts on the UC3854) and Vo is the DC output voltage.

The gain of the error amplifier above the pole in its frequency response is given by:

$$Gva = \frac{Xcf}{Rvi}$$

Where Gva is the gain of the voltage error amplifier, Xcf is the impedance of the feedback capacitance and Rvi is the input resistance.

The gain of the total voltage loop is the product of Gbst and Gva and is given by the this equation:

$$Gv = \frac{Pin \times Xco \times Xcf}{\Delta Vvea \times Vo \times Rvi}$$

Note that there are two terms which are dependent on f, Xco and Xcf. This function has a second order slope (-40dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set Gv equal to one and rearrange the equation to solve for fvi. Xco is replaced with 1/(2πfCo) and Xcf is replaced with 1/(2πfCvf).

The equation becomes:

$$fvi^2 = \frac{Pin}{\Delta Vvea \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Solving for fvi in the example converter gives fvi=19.14Hz. The value of Rvf can now be found by setting it equal to the impedance of Cvf at fvi. The equation is: Rvf=1/(2πfviCvf).

In the example converter a value of 177K is calculated and 174K is used.

Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (Cff1 and Cff2) attenuate the ripple voltage from the rectified input voltage. The

9

second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the "gain" of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is Gff = 1.5 / 66.2 = 0.0227.

The recommended divider string impliments a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$$fc = \sqrt{Gff} \times fr$$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120Hz so the cutoff frequency is fc=0.15x120=18Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this applivation, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

In the example converter Rff2 is 91K and Rff3 is 20K; so,

Cff1=1/2πx18x91K=0.1μF;

Cff2=1/2πx18x20K=0.44μF;

so choose Cff2=0.47μF.

This completes the design of the major circuits of an active power factor corrector.

DESIGN PROCEDURE SUMMARY

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:

   Pout (max): 250W
   Vin range: 80-270Vac
   Line frequency range: 47-65Hz
   Output voltage: 400Vdc

2. Select switching frequency:

   Example:

   100KHz

3. Inductor selection:

   A. Maximum peak line current. Pin ≈ Pout(max)

   $$Ipk = \frac{\sqrt{2} \times Pin}{Vin\ (min)}$$

   Example:

   Ipk=1.41x250/80=4.42 amps

   B. Ripple current.

   $$\Delta I = 0.2 \times Ipk$$

   Example:

   ΔI=0.2x4.42= 0.9 amps peak to peak

   C. Determine the duty factor at Ipk where Vin(peak) is the peak of the rectified line voltage at low line.

   $$D = \frac{Vo - Vin\ (peak)}{Vo}$$

   Example:

   D=(400-113)/400=0.71

   D. Calculate the inductance. fs is the switching frequency.

   $$L = \frac{Vin \times D}{fs \times \Delta I}$$

   Example:

   L=(113x.71)/(100,000x0.9)=0.89mH

   Round up to 1.0mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for Co are 1μF to 2μF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. Δt is the hold-up time in seconds and V1 is the minimum output

capacitor voltage.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - V1^2}$$

Example:
Co=(2x250x34msec)/(400-350)=450µF

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0V is a typical value for Vrs.

A. Find $Ipk(max) = Ipk + \frac{\Delta I}{2}$

Example:

Ipk(max)=4.42+0.45 ≈ 5.0amps peak

B. Calculate sense resistor value.

$$Rs = \frac{Vrs}{Ipk(max)}$$

Example:

Rs=1.0/5.0=0.20 ohms. Choose 0.25ohms

C. Calculate the actual peak sense voltage.

$$Vrs(pk) = Ipk(max) \times Rs$$

Example:

Vrs(pk)=5.0x0.25=1.25V

6. Set independent peak current limit. Rpk1 and Rpk2 are the resistors in the voltage divider. Choose a peak current overload value, Ipk(ovld). A typical value for Rpk1 is 10K.

$$Vrs(ovld) = Ipk(olvd) \times Rs$$

Example:

Vrs(ovld)=5.6x0.25=1.4V

$$Rpk2 = \frac{Vrs(ovld) \times Rpk1}{Vref}$$

Example:

Rpk2=(1.4x10K)/7.5=1.87K. Choose 1.8K

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, Km=1, Iac is the multiplier input current, Vff is the feedforward voltage and Vvea is the output of the voltage error amplifier.

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

A. Feedforward voltage divider. Change Vin from RMS voltage to average voltage of the rectified input voltage. At Vin(min) the voltage at Vff should be 1.414 volts and the voltage at Vffc, the other divider node, should be about 7.5 volts. The average value of Vin is given by the following equation where Vin(min) is the RMS value of the AC input voltage:

$$Vin(av) = Vin(min) \times 0.9$$

The following two equations are used to find the values for the Vff divider string. A value of 1 Megohm is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

$$Vff = 1.414V = \frac{Vin(av) \times Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vnode \approx 7.5V = \frac{Vin(av) \times (Rff2 + Rff3)}{Rff1 + Rff2 + Rff3}$$

Example:

Rff1=910K, Rff2=91K, and Rff3=20K

B. Rvac selection. Find the maximum peak line voltage.

$$Vpk(max) = \sqrt{2} \times Vin(max)\}$$

Example:

Vpk(max)=1.414x270=382Vpk

Divide by 600 microamps, the maximum multiplier input current.

$$Rvac = \frac{Vpk(max)}{600E-6}$$

Example:

Rvac=(382)/6E-4=637K. Choose 620K

C. Rb1 selection. This is the bias resistor. Treat this as a voltage divider with Vref and Rvac and then solve for Rb1. The equation becomes:

$$Rb1 = 0.25\ Rvac$$

Example:

Rb1=0.25Rvac=155K. Choose 150K

D. Rset selection. Imo cannot be greater than twice the current through Rset. Find the multiplier input current, Iac, with Vin(min). Then calculate the value for Rset based on the value of Iac just calculated.

$$Iac(min) = \frac{Vin(pk)}{Rvac}$$

Example:

Iac(min)=113/620K=182µA

$$Rset = \frac{3.75}{2 \times Iac(min)}$$

Example:

9

Rset=3.75V/(2x182μA)=10.3Kohms.

Choose 10Kohms

E. Rmo selection. The voltage across Rmo must be equal to the voltage across Rs at the peak current limit at low line input voltage.

$$Rmo = \frac{Vrs(pk) \times 1.12}{2 \times Iac(min)}$$

Example:

Rmo=(1.25x1.12)/(2x182E-6)=3.84K.

Choose 3.9Kohms

8. Oscillator frequency. Calculate Ct to give the desired switching frequency.

$$Ct = \frac{1.25}{Rset \times fs}$$

Example:

Ct=1.25/(10K x 100K)=1.25nF.

9. Current error amplifier compensation.

A. Amplifier gain at the switching frequency. Calculate thevoltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (Rs/N) for Rs. The equation is:

$$\Delta Vrs = \frac{Vo \times Rs}{L \times fs}$$

Example:

ΔVrs=(400x0.25)/(0.001x100,000)=1.0Vpk

This voltage must equal the peak to peak amplitude of Vs, the voltage on the timing capacitor (5.2 volts). The gain of the error amplifier is therefore given by:

$$Gca = \frac{Vs}{\Delta Vrs}$$

Example:

Gca=5.2/1.0=5.2

B. Feedback resistors. Set Rci equal to Rmo.

Rci = Rmo

Rcz = Gca x Rci

Example:

Rcz=5.2x3.9K=20Kohms

C. Current loop crossover frequency.

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Example:

fci=(400x0.25x20K)/(5.2x2πx0.001x3.9K)

=15.7KHz

D. Ccz selection. Choose a 45 degree phase margin. Set the zero at the loop crossover frequency.

$$Ccz = \frac{1}{2\pi \times fci \times Rcz}$$

Example:

Ccz=1/(2πx15.7Kx20K)=507pF.

Choose 620pF

E. Ccp selection. The pole must be above fs/2.

$$Ccp = \frac{1}{2\pi \times fs \times Rcz}$$

Example:

Ccp=1/(2πx100Kx20K)=80pf.

Choose 62pF

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes ½% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, Vff, contributes 1% third harmonic to the input current for each 1% second harmonic at the Vff input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the Vff input and 0.75% is allocated to the output ripple voltage or 1.5% to Vvao. The remaining 0.75% is allocated to miscellaneous nonlinearities.

11. Voltage error amplifier compensation.

A. Output ripple voltage. The output ripple is given by the following equation where fr is the second harmonic ripple frequency:

$$Vo(pk) = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Example:

Vo(pk)=250/(2π120x450E-6x400)=1.84Vac

B. Amplifier output ripple voltage and gain. Vo(pk) must be reduced to the ripple voltage allowed at the output of the voltage error amplifier. This sets the gain of the voltage error amplifier at the second harmonic frequency. The equation is:

$$Gva = \frac{\Delta Vvao \times \%Ripple}{Vo(pk)}$$

For the UC3854 Vvao is 5-1=4V

Example:

Gva=(4x0.015)/1.84=0.0326

C. Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of Rvi is reasonably arbitrary.

Example:

Choose Rvi=511K

$$Cvf = \frac{1}{2\pi \times fr \times Rvi \times Gva}$$

Example:
Cvf=1/(2πx120x511Kx0.0326)=0.08μF.

Choose 0.047μF

D. Set DC output voltage.

$$Rvd = \frac{Rvi \times Vref}{Vo - Vref}$$

Example:

Rvd=(511Kx7.5)/(400-7.5)=9.76K.

Choose 10.0K

E. Find pole frequency. fvi = unity gain frequency of voltage loop.

$$fvi^2 = \frac{Pin}{\Delta Vvao \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Example:

$$fvi = \sqrt{(250/(4x400x511Kx450E{-}6x47E{-}9x39.5))} =$$

19.1 Hz

F. Find Rvf.

$$Rvf = \frac{1}{2\pi \times fvi \times Cvf}$$

Example:

Rvf=1/(2πx19.1x47E-9)=177K. Choose 174K

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10 above.

$$Gff = \frac{\%THD}{66.2\%}$$

Example:

Gff=1.5/66.2=0.0227

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$fp = \sqrt{Gff} \times fr$$

Example:

fp=0.15x120=18Hz

Select Cff1 and Cff2.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

Example:

Cff1=1/(2πx18x91K)=0.097μF. Choose 0.10μF

Cff2=1/(2πx18x20K)=0.44μF. Choose 0.47μF

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The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters

by JOHN A. O'CONNOR

ABSTRACT

This application note describes the UC3848 average current mode PWM controller. The unique features of this controller are discussed, which make primary side average current mode control practical for isolated converters. The UC3848 employs a current waveform synthesizer which monitors switch current and simulates the inductor current down slope, generating a complete current waveform without actual secondary side measurement. Primarily intended for single ended converters, several additional features such as accurate duty-cycle and volt-second limiting allow maximum transformer and switch utilization. A three output, 200 watt off-line design example is presented which also features planar magnetics and a coupled output inductor.

INTRODUCTION

The UC3848 represents a significant advance in the control of single switch forward converters. Generally considered simple and reliable, but non-optimum in transformer and switch utilization, the single switch forward has previously been reserved for less demanding applications. Upon careful examination however, it is apparent that many of the perceived limitations actually result from the control circuitry rather than the converter topology itself.

The advantages that an inner current loop brings to power supply design and performance are well known [1]. Current mode control is usually preferred over direct duty cycle control because of the superior input supply rejection and simplified voltage loop closure. Average current feedback provides additional advantages over the more common peak current feedback. Major benefits include inherent slope compensation, better noise rejection, and the ability to operate with both continuous and discontinuous inductor current. Additionally, average current feedback provides significantly better closed current loop accuracy. This further improves input supply rejection and current limit accuracy. Average current feedback is detailed in the references [2,3,4].

Maximum power component utilization requires carefully defined and controlled operating mode boundaries. While this can be said of many converter topologies, it is particularly critical with the single switch forward because of the transformer reset mechanism. Energy in the transformer leakage and magnetizing inductance must be removed after each energy transfer cycle. Above all, the control circuit must insure that this condition is achieved. Total losses are generally minimized by bringing the peak power transfer as close to the average as possible. This indicates that improvements in efficiency and component utilization are obtainable by maximizing duty-cycle. Unfortunately, maximizing duty-cycle conflicts with assuring transformer reset, traditionally requiring an overly conservative design to assure reliability.

Previously, these characteristics have limited the single switch converter to low-power, low-end applications. The UC3848 Average Current Mode PWM Controller allows operation beyond conventional limitations by employing highly accurate circuitry to provide programmable operating boundaries, and by implementing an inner average current feedback loop for improved control characteristics and accuracy. This control circuit advance capitalizes on unique, patented circuitry, and the precision achievable with Unitrode's thin-film resistor process.

The UC3848 Average Current Mode PWM Controller

The block diagram of the UC3848 shown in figure 1, illustrates a number of unique functions. Although the IC can certainly be used for flyback,

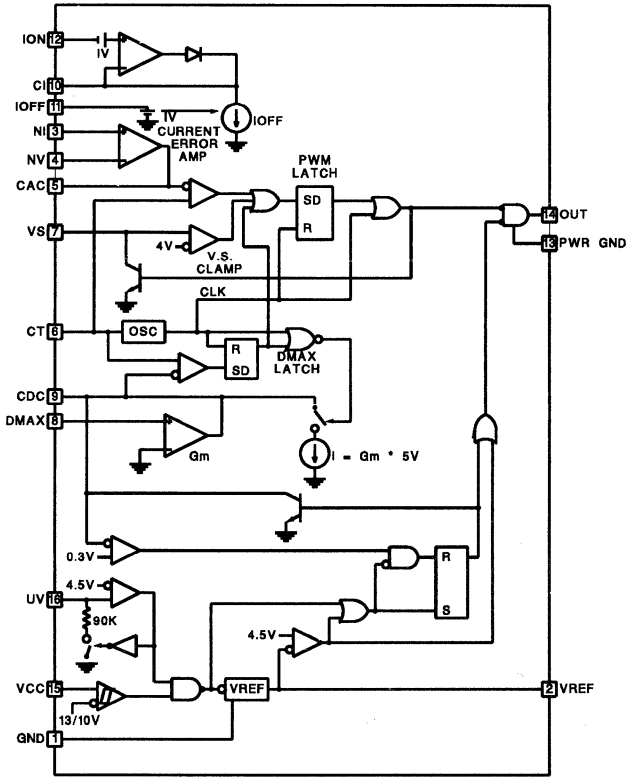

Figure 1

UC3848 Average Current Mode PWM Controller

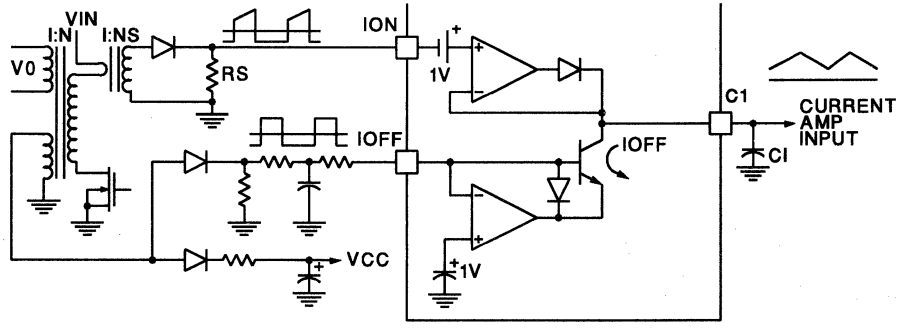

Figure 2

Inductor Current Waveform Synthesizer

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boost, as well as other buck derived converters [4], the UC3848 has been optimized for forward converter use. The UC3848s precision functions bring switching power supply control to a new level:

- Average Current Mode Control
- Average Current Sense Signal Synthesizer
- Programmable Maximum Duty-Cycle and Volt-Second Control
- Under Voltage Lockout (UVLO) monitors Vcc, Vin, and Vref
- 2 Amp peak MOSFET Driver with Active Low During UVLO
- 8MHz gain-bandwidth Current Error Amplifier
- Latched PWM comparator
- Practical Operation up to 1MHz
- Low Start-Up Current (500uA)
- Precision Reference (1% @ 5V)

The sophistication and performance of the UC3848 may at first appear contradictory to simple forward converter design. A truly simple implementation however, is best achieved by maintaining simple power circuitry, and placing the complexity and precision in the control circuitry where it can be integrated into a single IC.

Average Current Mode Control

Average current loop implementation first requires an average current signal for the control variable. This immediately presents a problem with isolated converters since this signal is entirely on the secondary side. A current sense transformer cannot be used to directly sense output inductor current with buck derived converters since the inductor normally has a continuous DC component. A potentially complex and expensive solution is avoided with the realization that output inductor current is directly reflected to the primary during the switch on time. Simply scaling the switch current by the transformer turns ratio provides the rising portion of the inductor current waveform. When the switch is off, the inductor current decays at V_{OUT}/L. This information can be used to synthesize an analog of the actual output inductor current without any secondary connections.

Inductor current is synthesized by the UC3848 with a circuit that behaves similar to a track and hold amplifier, as shown in figure 2. While the switch is on, a unity gain buffer charges an external capacitor (C_I), essentially following the rising input current waveform. A one volt offset is also added to provide sufficient headroom for the buffer's output stage. When the switch turns off, a programmable current sink discharges the capacitor, simulating the actual inductor current decay. Several techniques are available for setting the discharge current, depending on the required accuracy of the current sense signal. If good short-circuit accuracy is required, an analog of the output voltage is required to control the synthesizer capacitor discharge rate. There are two simple ways to derive this signal on the primary side.

The first method uses a transformer bootstrap winding voltage as shown in figure 2. The average value of the rectified output and bootstrap winding voltages are directly proportional. By adding a separate rectifier and filter to this winding, the capacitor discharge current can be programmed to track V_{OUT}. Typically, a bootstrap winding is employed with off-line converters to power the control circuitry after initial start-up, so the raw signal is usually present at no additional cost. Note that an error is present during transients since the filter creates a lag between the output and the filtered bootstrap voltages.

If the transient error is unacceptable, the technique shown in figure 3 can be used. A secondary winding on the output inductor provides a voltage directly proportional to the output without filtering. While the switch is off, V_{OUT} is across the output inductor. Any other winding on the inductor will have a voltage proportional to V_{OUT} by the turns

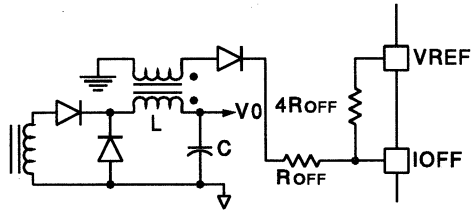

Figure 3
IOFF Generation using Second Inductor Winding

ratio of the two windings. The sense winding rectifier drop cancels the output rectifier drop when the turns ratio is 1:1, yielding excellent signal accuracy. While this approach is simple and accurate, it does come at additional expense since this winding is not normally required. Additionally, high voltage agency approved isolation is required for off-line converters, adding further cost and manufacturing complexity to the inductor.

With either of these techniques, an offset current may be added to compensate for the synthesizer's

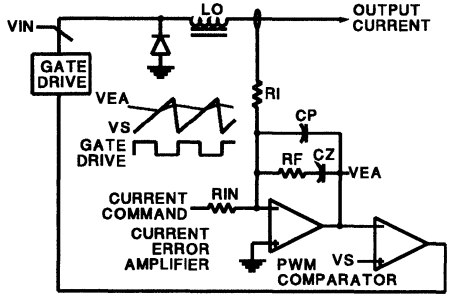

FIGURE 4. AVERAGE CURRENT FEEDBACK LOOP

Figure 4

Average Current Feedback Loop

one volt offset. Connecting a resistor with a value four times the I_{OFF} input resistor between the V_{REF} and I_{OFF} pins cancels the offset.

Often, a fixed discharge current is acceptable. This is programmed by connecting a resistor between the V_{REF} and I_{OFF} pins. The synthesized current waveform is quite accurate when the output voltage is near the regulating value, however an error exists during start-up and output short-circuit. During a short, the current decays much slower since V_{OUT} is only the output rectifier and circuit resistance voltage drops. The current ripple also becomes a small fraction of its value at the regulating voltage. The synthesizer however, discharges the capacitor as if the output were not shorted, and therefore underestimates the output inductor current. The short-circuit current will then exceed the programmed limit by almost one-half of the normal peak-to-peak ripple current. Typically, the inductor ripple current is 20% to 30% of the maximum DC value, corresponding to a short circuit current 10% to 15% higher than the maximum output current available at normal output voltage.

The current error amplifier has sufficient gain to use a current sense resistor directly in most applications. A current sense transformer however, results in better performance by allowing a larger amplitude, lower noise signal. Ideally, the current sense signal is scaled to 4 volts at the maximum current level. The current transformer load resistance is then:

$$R_S = 4V \times N \times \frac{N_S}{I_L} \qquad (1)$$

where N = transformer turns ratio
N_S = current transformer ratio
I_L = maximum load current

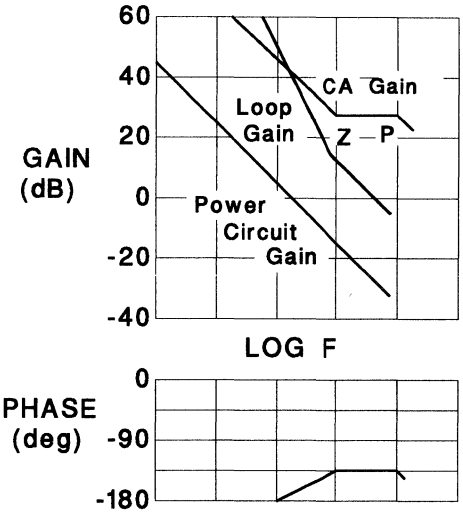

Figure 5

Open Current Loop Response

With multiple secondaries, normalize all other loads to the main output through the turns ratio directly. Note that for these calculations, output inductors and their effect on ripple current is not considered, since the UC3848 controls average, not peak current. Output inductances must be normalized to the main output through the turns ratio squared however, when calculating peak current and current ripple.

The recommended nominal I_{OFF} current is 100µ A, leaving C_I the remaining current synthesizer component.

$$C_I = \frac{(100\mu A \times N \times N_S \times L_{NORM})}{(Rs \times V_{OUT}(nom))} \qquad (2)$$

where L_{NORM} = normalized output inductance

Figure 5 shows the average current feedback loop. This inner loop is analogous to direct duty-cycle or voltage-mode control except that the control variable is output inductor current rather than output voltage. Properly compensated, the open loop gain is comparable to peak current-mode's at high frequency, and becomes orders of magnitude higher as frequency decreases. The open current loop response shown in figure 6 illustrates this behavior. This high open loop gain translates into high

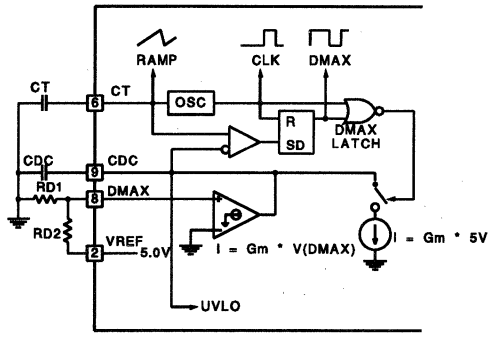

Figure 6

Duty-Cycle Limit Programming

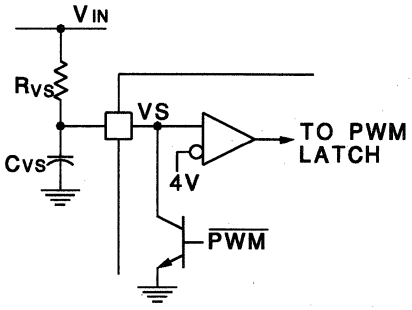

Figure 7

Volt-Second Clamp

closed loop accuracy. In comparison, peak current mode relies entirely on it's transfer function accuracy, and has no means by which to reduce errors. This characteristic difference from peak current-mode is attributed to the current error amplifier's compensation, and is key to the resulting performance enhancements.

The increased gain at low frequency provides excellent closed current loop accuracy, even when the inductor current becomes discontinuous. High open loop gain also allows greater filtering of the current sense signal with no degradation in closed loop accuracy. It is this characteristic, along with the larger amplitude signals that provides significantly reduced noise susceptibility in comparison to peak current-mode control.

PWM Oscillator

Oscillator programming is simplified by providing internally set charge and discharge currents. Excellent initial accuracy and temperature stability are assured by precision thin-film resistors. Since only a timing capacitor (C_T) is required to set the frequency, external component error contribution is minimal. The precision high speed oscillator combined with short propagation delay through the PWM circuitry allows practical operation up to 1MHz.

A 200µA charge current and a 1800µA discharge current generates a sawtooth waveform with a well defined rise/fall relationship and accurate frequency. During discharge, the output driver is disabled, limiting the maximum duty-cycle to 90%. Note that this maximum can be reduced by the accurate, duty-cycle limit and the volt-second product limit circuits, which are explained in following sections. Oscillator frequency is programmed by:

$$F = \frac{1}{(10k + C_T)} \qquad (3)$$

If greater frequency accuracy is required, a trim resistor in parallel with C_T can be added to lower the frequency. The trim resistor should not be less than 40kΩ, limiting the maximum trim range to 25% below nominal. Frequency decrease as a function of trim resistance is shown on the UC3848 data sheet.

Duty-Cycle Limiting and Soft Start

The conventional single switch forward converter design usually limits the maximum duty-cycle to 50%. This limit however, is only required if a one-to-one clamp winding is employed to facilitate transformer core reset. While some designers still use this technique, a resistor/capacitor/diode (RCD) clamp has become more prevalent. The RCD clamp eliminates a transformer winding and potentially offers a wider duty-cycle range. Currently, a 50% duty-cycle limit is primarily used because it can be accurately derived from a toggle flip-flop. To exploit a wider duty-cycle, an accurate, programmable duty-cycle clamp is required.

The UC3848 employs a unique, patented technique to limit the maximum duty-cycle to a value programmed by a resistive divider. The circuit utilizes a capacitor (C_{DC}) for integration only, and does not rely on its absolute value for maximum duty-cycle accuracy. The absolute value of C_{DC} does set the soft-start time constant, although high precision is not normally required for this function.

Internally, the UC3848 capitalizes on the excellent matching characteristics achievable on an IC to implement a charge balanced loop. A matched transconductance source and sink form a precision integrator circuit, as shown in figure 6. The current

source is externally programmed to Gm x V_{DMAX} and is on continually. The current sink is internally set at Gm x 5V, and is switched on and off. The resulting discharge current is Gm(5V - $_{DMAX}$). The current source and sink charge and discharge C_{DC}, while its voltage is compared with the oscillator voltage.

The current sink discharges C_{DC} from the time that the switch is turned on until the oscillator voltage becomes greater than C_{DC}'s voltage. For the remainder of the period, C_{DC} is charged by the current source. Note that C_{DC}'s voltage is essentially a DC level with a very small ripple component unless it is a particularly small value. C_{DC} maintains a constant voltage only if the average applied charge is zero. The charge balanced loop therefore forces $I_{DISCHARGE}$ x $T_{ON(max)}$ to equal I_{CHARGE} x $T_{OFF(min)}$. A large offset voltage between C_T and C_{DC} may be observed when measuring an actual circuit. This offset contributes negligible error since high DC loop gain reduces its effect by several orders of magnitude.

While the circuit's operation may seem complicated, it couldn't be easier to apply. A voltage divider from V_{REF} to D_{MAX} as shown if figure 6 sets the maximum duty-cycle. The circuit inherently provides soft-start at initial power-up as C_{DC} charges to it's steady state value. Increasing C_{DC} extends the loop settling time, and hence the soft-start time constant, with no effect on the programmed maximum duty-cycle. Note that the single pole loop response avoids overshoot, regardless of the integrating capacitor value. Soft-start after fault is explained in the under-voltage lockout section. Maximum duty-cycle and soft-start are programmed by the following relationships:

$$D_{MAX} = \frac{R_{D2}}{(R_{D1} + R_{D2})} \quad (4)$$

$$\tau_{ss} = 20k \times C_{DC} \quad (5)$$

Volt-Second Product Limit

During transients it may be desirable to limit the duty-cycle below the programmed maximum value. For example, active transformer reset circuits vary the clamp voltage inversely proportional to the input supply voltage [5]. During steady state operation the peak MOSFET voltage varies much less than with passive clamp circuits. Unless the input voltage range is large, the peak MOSFET voltage will be fairly constant. This occurs because the applied volt-second product remains constant over the entire operating duty-cycle range during steady state. Thus as the input voltage goes up and the duty-cycle decreases, the clamp voltage goes down as the reset time increases.

If during a transient the duty-cycle is allowed to increase excessively, the MOSFET will be subjected to significantly higher voltages. This assumes that the reset circuit's clamp voltage can slew rapidly. If it cannot, the magnetizing current will ratchet up, possibly saturating the transformer. Both scenarios are easily prevented by simply limiting the maximum applied volt-second product.

The UC3848 generates a voltage proportional to the volt-second product with the circuit shown in figure 7. A current directly proportional to the supply voltage (V_{IN}/R_{VS}) charges a capacitor (C_{VS}) while the MOSFET is on. When the MOSFET is turned off, the capacitor is discharged. Volt-second limiting is accomplished by comparing the capacitor's voltage to a 4 volt reference, and terminating the pulse width for the remainder of the switching period. Normally, the worst case MOSFET voltage occurs during maximum input voltage at the volt-second limited duty-cycle. However, high turns ratio designs which allow a very wide duty-cycle may actually generate the highest MOSFET voltage during low-line at the volt-second limited duty-cycle.

Since the volt-second product is constant it can be calculated at any input voltage. The effectiveness

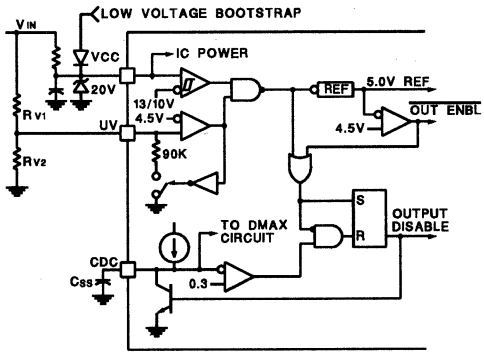

Figure 8

Under Voltage Lockout

of the volt-second limit however, should be analyzed at minimum and maximum input voltage, in addition to a few more typical voltages. The volt-second product clamp is programmed by:

$$V_{IN} \times T_{ON} = 4.0V \times R_{VS} \times C_{VS} \quad (6)$$

Under Voltage Lockout

Programmable under voltage lockout (UVLO) further defines operating mode boundaries. V_{CC}, V_{IN},

and V_{REF} are monitored to insure that the chip supply, main input supply, and reference are within specification before enabling the output stage. Figure 8 shows the block diagram of the UVLO circuitry.

The V_{CC} comparator monitors the chip supply voltage. Hysteretic thresholds at 13V and 10V insure that sufficient voltage is available to power the chip and fully turn on the MOSFET. The V_{IN} comparator monitors the input supply through a resistive divider. A small capacitor from UV to ground is usually required to filter noise from this high impedance node. Both the thresholds and the hysteresis are programmed by the divider values with the relationships:

$$V_{IN(ON)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2'}}\right) \quad (7)$$

$$V_{IN(OFF)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2}}\right) \quad (8)$$

where $R_{V2'} = R_{V2} \parallel 90k$

$$V_{IN(HYS)} = 4.5V \times \frac{R_{V1}}{90k} \quad (9)$$

When either the V_{CC} or the V_{IN} comparator are low, the bias circuitry to the rest of the chip is off. The quiescent current (I_{CC}) is nominally 500μ A to facilitate off-line applications. Once both V_{CC} and V_{IN} are within specification, the bias circuitry for the rest of the chip is activated. The output driver and C_{DC} pin are still held low until V_{REF} exceeds the 4.5V threshold of the V_{REF} comparator. When the V_{REF} comparator goes high, control of the output driver transfers to the PWM circuitry and C_{DC} is allowed to charge, soft-starting the supply.

If any of the three monitored voltages falls below their threshold during start-up or normal operation, the UVLO latch is set, the output driver is held low, and C_{DC} is discharged. This state is maintained until C_{DC} is fully discharged, at which point operation is as described above.

Output Driver

High current transistors enable the output driver to deliver 2 amps peak allowing direct interface to any MOSFET typically used in single ended converters. The driver also incorporates self-biasing circuitry that maintains a low impedance to ground during UVLO. This assures that high dv/dt at V_{IN} during power-up cannot inadvertently turn on the MOSFET through its miller capacitance.

The combination of high peak current, stray circuit inductance, and capacitive gate load result in reflections back to the driver, which if left unclamped, will cause erratic chip behavior. External schottky diodes from the output to V_{CC} and ground will divert the reflected current and assure reliable operation. A well designed layout with typical circuit values will normally require 1A, 20V schottky clamp diodes. Looser layouts, longer gate drive traces, and lower gate resistor values all place greater demand on the output clamping circuit, and may necessitate higher current diodes.

Voltage Reference and Error Amplifier

Since the UC3848 is intended for primary side control, the voltage reference (V_{REF}) does not affect output voltage stability. It does however, affect current limiting and the other precision circuits previously mentioned, and has therefore been designed for good initial accuracy and temperature drift. The reference should be capacitively bypassed to reduce high frequency output impedance and noise susceptibility.

To facilitate wide bandwidth current loops, the error amplifier has an 8Mhz gain bandwidth product. Even with small current feedback signals such as from a current sense resistor, loop bandwidth will almost always be limited by external circuit characteristics rather than error amplifier limitations. The amplifier's 8 V/s slew rate assures that even during large signal transients, external components will determine circuit behavior.

Design Example

A 200 watt off-line supply utilizing the UC3848 is shown in figure 9. It delivers a regulated +5V at 20A, and a semi-regulated +/-15V at 3.3A. The conversion frequency is 260kHz, which was determined to be a reasonable compromise between size and efficiency. A coupled output inductor improves dynamic cross regulation and steers some of the +5V ripple current to the +/-15V filter capacitors [9]. This results in minimal total output capacitor volume. A bridge/doubler input rectifier allows operation over an input range of 85 to 265VAC. For simplicity and cost, an RCD clamp is employed to facilitate transformer reset. This common configuration is typical of many commercial applications.

The transformer turns ratio is selected to minimize MOSFET stress. Ideally, the maximum duty-cycle should be as large as possible, allowing the highest turns ratio and lowest reflected load current. This must be balanced against the peak MOSFET voltage developed during transformer reset.

Since the UC3848 can accurately define operating mode boundaries, any practical duty-cycle range can be used. This allows maximum utilization of both current and voltage capability of a particular

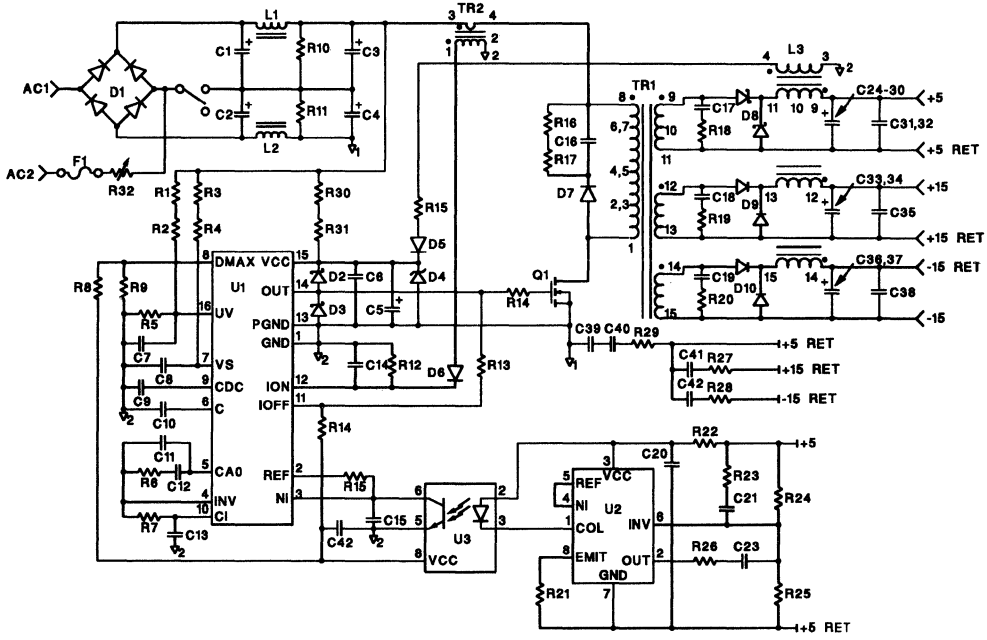

Figure 9

200W 3 OUTPUT FORWARD CONVERTER

MOSFET. The RCD clamp allows some trade-off in dissipation versus peak MOSFET voltage. Turns ratio and clamp optimization requires a good estimation of leakage inductance, switch capacitance, and transformer interwinding capacitance, since energy stored in these parasitics will be transferred or dissipated each switching cycle. RCD clamp optimization is covered in detail in reference [6].

The design example transformer uses a 16:1 turns ratio (primary to 5 volt), allowing a wide input supply range and reliable use of an 800V MOSFET. The MOSFET, an APT801R2BN from Advanced Power Technology [7], is rated at 800V and has 1.2Ω maximum on resistance at 25°C. A planar transformer and coupled output inductor from Signal Transformer Co. [8] are used, which offer several advantages over custom wound components. Planar construction provides tighter parameter tolerance. Compact, low profile magnetics help achieve high power density. Their standard design provides agency approved insulation and known performance characteristics, greatly reducing the number of iterations to produce a good power supply design.

The duty-cycle is limited to 0.6, maintaining regulation down to approximately 160 VDC in. With the switching frequency programmed for 260 kHz, the nominal volt-second product is 345 Vs. The volt-second clamp is programmed to 425 Vs to allow for tolerances and large signal transients.

A current transformer senses switch current resulting in minimal loss and good signal quality. A 1000pF capacitor shunts the high frequency turn-on spike before feeding the current sense signal to the UC3848s current waveform synthesizer. A fixed I_{OFF} value renders an acceptable short circuit current for this application. Average short circuit losses are kept low by the hiccup action which occurs as the boot-strap supply colapses and the supply restarts. Highly accurate short circuit current is most advantageous when a continuous supply is available for the control circuit such as in low voltage DC to DC converter applications.

When the MOSFET is on, the current synthesizer's I_{OFF} current is increased through a resistor connected to the gate driver output (R13). This allows C_I's voltage to better follow rectifier reverse recovery spikes present in the current waveform. This technique allows minimal filtering of the current

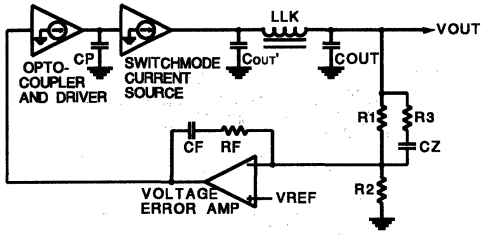

Figure 10

Voltage Feedback Loop

sense signal, and thus preserves accuracy.

The coupled output inductor provides good dynamic cross regulation, and steers some of the 5 volt ripple current to the +/-15 volt outputs where it is more efficiently filtered. Although this technique minimizes size and complexity, it does negate two major advantages of average current mode control. The average current loop maintains excellent regulation down to zero load for the fully regulated output. Unfortunately, the semi-regulated outputs will degrade quickly as the inductor current becomes discontinuous, forcing minimum loads for reasonable output voltage tolerance. Also, stray and leakage inductance between the secondary circuits introduces parasitic tank circuits, which if underdamped, will cause output ringing and instability. Generally, electrolytic output capacitors, low coupled inductor leakage inductance, and tight layout will allow successful implementation, although loop bandwidth must usually be compromised to maintain stability. Coupled output inductor design and application is detailed in reference [9].

Without the additional output circuitry parasitics, a single output supply with average current feedback has excellent regulation and transient response from zero to full load. There is also much less restriction on output capacitor type, allowing small ceramic or film capacitors in many applications. Although the design example's closed loop bandwidth is not as high as would be achievable with a single output, the electrolytic output capacitors store enough energy to provide good transient response and low output impedance.

Control Loops

A block diagram of the voltage feedback loop is shown in figure 10. For clarity, the inner average current feedback loop is shown as a transconductance amplifier, and is identical to figure 4. Current loop compensation is best described in the references [2,3], as a number of subtleties must be considered for optimal performance. The basic approach is easily summarized:

To avoid subharmonic oscillation of a single pole system, the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This puts an upper limit on the current amplifier gain, and indirectly sets the loop gain crossover frequency. As derived in [2], the resulting unity gain crossover frequency will be:

$$f_C = \frac{(f_S V_{IN})}{(2\pi V_{OUT})} = \frac{f_S}{(2\pi D)} \qquad (10)$$

The crossover frequency must be reduced in a practical system to account for tolerances and additional waveform slope injected by output voltage ripple through the voltage error amplifier. For the design example, f_C is approximately 50kHz at the maximum duty-cycle.

At the switching frequency, the average current loop's behavior is similar to peak current mode control. Placing a zero at one-half the crossover frequency increases the loop gain with decreasing frequency, providing high closed current loop accuracy. To further reduce noise susceptibility, a pole is placed at the switching frequency. While such a low frequency filter is completely unacceptable with peak sensing, the high gain at low frequency assures accurate current limiting. It is these fundamental differences from peak current mode which provide the performance enhancements.

The voltage loop reference and error amplifier reside on the secondary side as typically configured in off-line power supplies. A UC19432 incorporates a high precision reference, voltage error amplifier, and programmable transconductance amplifier for accurate opto-coupled feedback. Voltage loop compensation is normally the same as with peak current mode control and is described in detail in the references [2,9,10]. As previously noted, an additional LC pole resulting from leakage and stray inductance requires additional compensation. Ultimately, this parasitic restricts the bandwidth of this coupled inductor design example, although transient response is still quite good. The same control configuration with a single output supply provides optimal performance and allows simpler compensation.

Summary

The UC3848 clearly demonstrates the next level of switching power supply control achievable with improved techniques and precision circuitry. High

performance and high power density objectives coupled with the need for simplicity and low cost have called for further refinement of single switch conversion. The UC3848 answers that call combining precision circuitry, average current mode control and function flexibility, allowing optimal power component utilization and performance.

References:

[1]V. Holland, "Modelling, Analysis and Compensation of the Current-Mode Converter" Unitrode application note U-97

[2]L. Dixon, "Control Loop Design", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800, 1991

[3]L. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode application note U-140

[4]B. Mammano, "Average Current-Mode Control Provides Enhanced Performance for a Broad Range of Power Topologies", PCIM conference proceedings, 1992

[5]B. Carsten, "Design Techniques for Transformer Active Reset Circuits at High Frequencies and Power Levels", High Frequency Power Conversion conference proceedings, 1990

[6]C.S.Leu, G.C.Hua, F.C. Lee, C. Zhou, "Analysis and Design of RCD Clamp Forward Converter", Virgina Power Electronics Center seminar proceedings, 1992

[7]Planar Magnetics data sheet, Signal Transformer Co., Inwood, NY, 516-239-5777

[8]APT801R2BN data sheet, Advanced Power Technology, Bend, OR, 503-382-8028

[9]L. Dixon, "Coupled Filter Inductors in Multi-Output Buck Regulators", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800, 1991

[10]L. Dixon, "Closing the Feedback Loop", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM700, 1990

Unitrode Data Sheets:

UC3848
UC19432

PARTS LIST FOR 200W CONVERTER

R1, 2	825k	1%
R3, 4	243k	1%
R5	42.2k	1%
R6, 7	10k	
R8	10.0k	1%
R9	15.0k	1%
R10, 11	62k	1w
R12	68	
R13	36k	
R14	39k	
R15,23	2k	
R16, 17	15k	3w
R18	10	2w
R19, 20	33	1/2w
R21	33	
R22	200	
R24	18.7k	1%
R25	6.49k	1%
R26	1k	
R27, 28	20	
R29	100	
R30, 31	120k	1/2w
R32	5ΩNTC	thermistor

C1-C4	390µF	20%	200V
C5	100µF	20%	25V
C6, 20, 31, 32, 35, 38	1µF		
C7, 14	1nF		
C8	220pF	5%	
C9	47nF		
C10	390pF	5%	
C11	22pF		
C12	330pF		
C13	220pF		
C15	10nF		
C16	2.2nF		
C17	4.7nF		100V
C18, 19	470pF		500V
C21, 23	3.3nF		
C24-C30	1000µF	20%	10V
C32, 33, 36, 37	330µF	20%	25V
C39, 40	2.2nF	20%	500V
	class x/y		
C41, 42	100nF	20%	100V

D1	MB106-ND	(Diodes, Inc.)
D2, 3	1N5820	
D3	1N4745A	
D4, 5	1N4148	
D6	10DF8	(International Recifier)
D7	40CPQ060	(International Recifier)
D9, 10	10CTF20	(International Recifier)
Q1	APT801R2BN	(Advanced Power Technology)
L1, 2	RL-1160-1.0	(Renco)
L3	SHFI-2515	(Signal Transformer Co.)
TR1	SHF-2525-16	(Signal Transformer Co.)
TR2	PE64978	(Pulse Engineering)
U1	UC3848	
U2	UC19432	

NOTE: All resistors 5%, 1/4 watt unless noted
All capacitors 10%, 50V unless noted

UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

APPLICATION NOTE

PHASE SHIFTED, ZERO VOLTAGE TRANSITION DESIGN CONSIDERATIONS and the UC3875 PWM CONTROLLER

BILL ANDREYCAK

ABSTRACT

This Application Note will highlight the design considerations incurred in a high frequency power supply using the Phase Shifted Resonant PWM control technique. An overview of this switching technique including comparisons to existing fixed frequency non-resonant and variable frequency Zero Voltage Switching is included. Numerous design equations and associated voltage, current and timing waveforms supporting this technique will be highlighted. A general purpose Phase Shifted converter design guide and procedure will be introduced to assist in weighing the various design tradeoffs. An experimental 500 Watt, 48 volt at 10.5 amp power supply design operating from a preregulated 400 volt DC input will be presented as an example. Considerations will be given to the details of the magnetic, power switching and control circuitry areas. A summary of comparative advantages, differences and tradeoffs to other conversion alternatives is included.

UC3875 CONTROL CIRCUIT SCHEMATIC

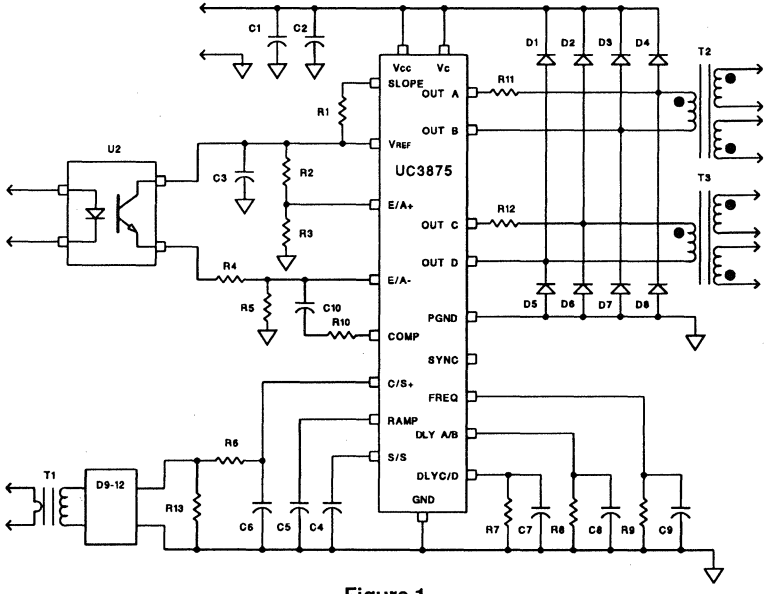

Figure 1

INTRODUCTION

The merits of lossless transitions using Zero Voltage Switching techniques have already been established in power management applications. [1-5] Effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique. The full bridge topology as shown in figure 2. will be the specific focus of this presentation, with an emphasis placed on the fixed frequency, phase shifted mode of operation.

Full Bridge Topology - General Circuit

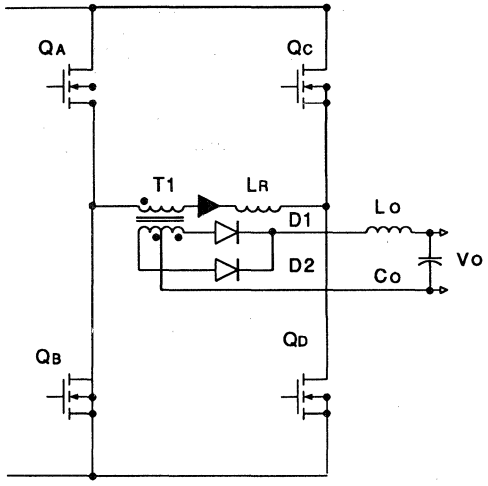

Figure 2

SWITCH DRIVE COMMANDS

The diagonal bridge switches are driven together in a conventional full bridge converter which alternately places the transformer primary across the input supply, Vin, for some period of time, t(on) as shown in figure 3.

Power is only transferred to the output section during the ON times of the switches which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Conventional Full Bridge PWM Waveforms

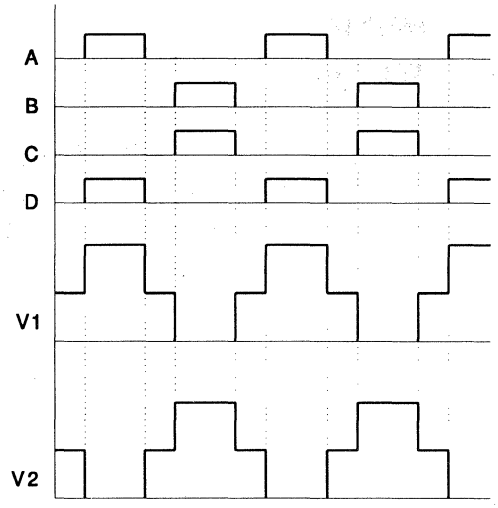

Figure 3

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in figure 4.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (Coss) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge "leg" with zero voltage across it enabling Zero Voltage Switching upon its turn ON.

Phase Shifted PWM Control Waveforms

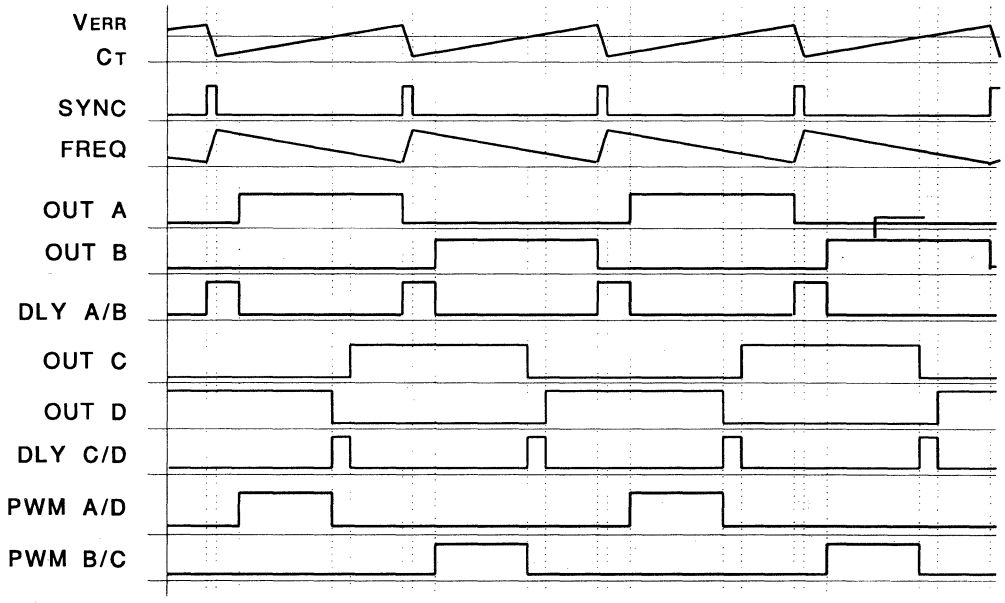

Figure 4

ZVS FUNDAMENTALS

An intentional dead-time can be introduced in the power conversion cycle whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather then turn the switch on instantly when zero voltage is attained, the switch is held off while the primary current circulates into the shorted primary through the body diode and the opposite leg switch, which is still on. This off time is used to fill in the voids between the point where zero voltage has been reached where the switch needs to turned on to achieve fixed frequency operation.

Fixed frequency operation is obtainable over an identified range of input voltages and output currents. For reference purposes, the variable frequency ZVS technique has similar limitations for proper operation which occur at minimum output load and maximum input line as shown in figure 5.

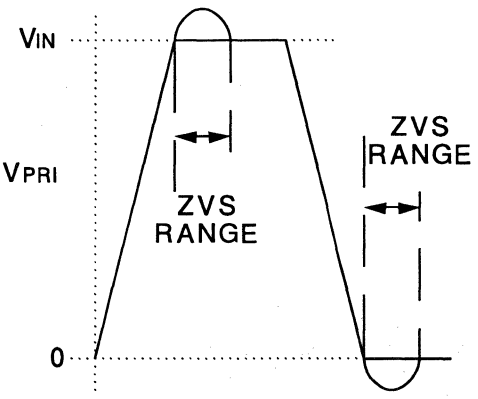

Figure 5

ZVS Limitations

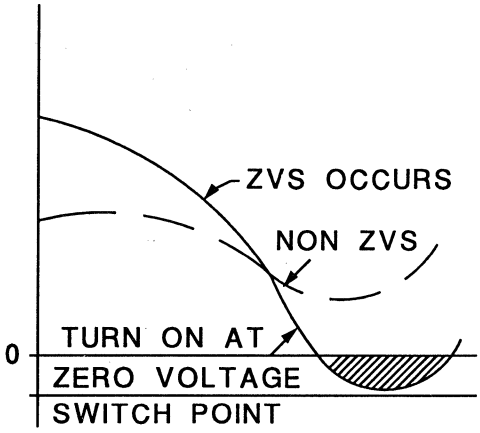

Figure 6

Phase Shifted PWM Switch Orientation

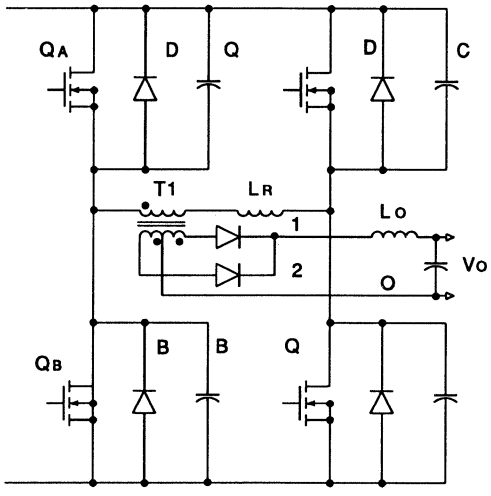

Figure 7

PHASE SHIFTED FUNDAMENTALS

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its nonresonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's constructuin. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

CIRCUIT SCHEMATIC AND DESCRIPTION

Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in figure 7. including voltage and current designations.

The basic circuit is comprised of four switches labeled QA through QD and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (IP) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also accounted for by multiplying the output inductance by the turns ratio squared (N^2), or dividing the secondary AC ripple current Isec(ac) by the turns ratio (N) as shown in figure 8.

Primary Magnetic Components

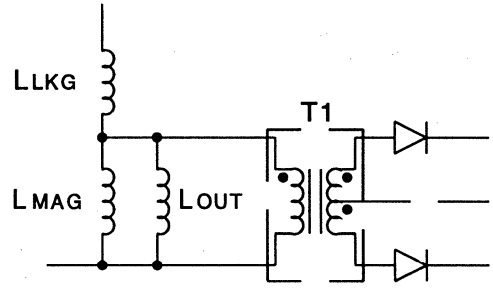

Figure 8

INITIAL CONDITIONS : t = t(0)

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as Ip(t(0)).

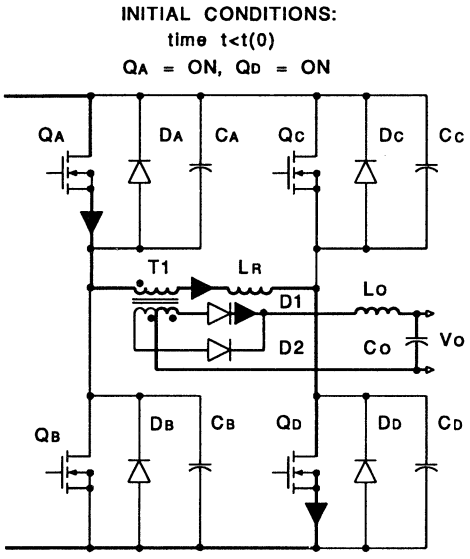

Figure 9

RIGHT LEG RESONANT TRANSITION : INTERVAL: t(0) <t <t(1)

The primary current flowing at time t(0) is equal to Ip(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right. Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at Ip(t(0)) by the resonant inductance (Lp(res)) of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, Lr. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external "shim" inductor to control the accuracy. It's also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.

With switch QD turned off, the primary current continues to flow using the switch output capacitance,

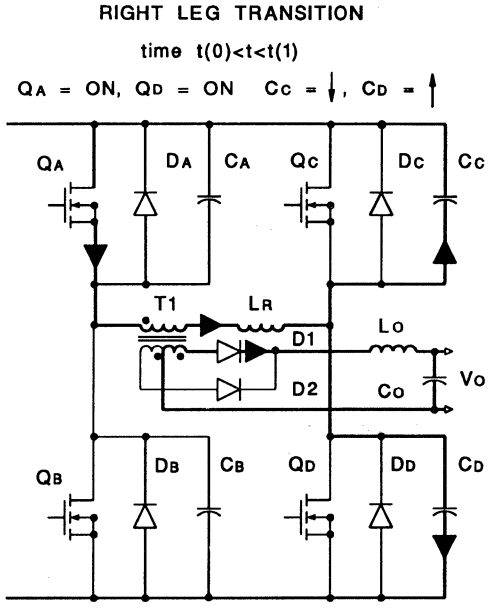

Figure 10

Coss to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, Vin+. Simultaneously, the transformer capacitance (Cxfmr) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased fom Vin to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, Vout*N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt.

CLAMPED FREEWHEELING INTERVAL
Time t(1) <t <t(2)

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode.

LEFT LEG TRANSITION :
Time t(2) <t <t(3)

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been previously turned ON and switch QA will now be turned OFF. The primary current will continue to

CLAMPED FREEWHEELING INTERVAL
time t(1)<t<t(2)
Q_A = ON, Q_C = ON, D_C = ON

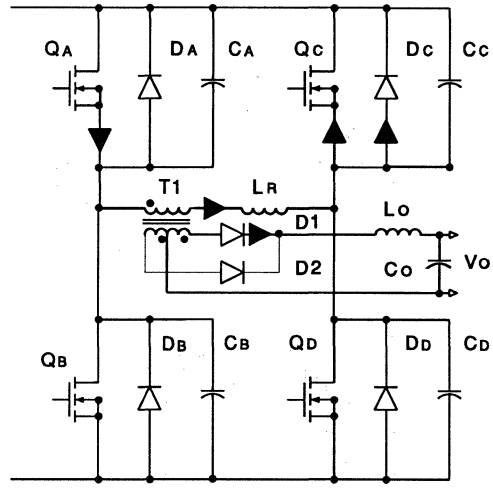

Figure 11

flow but the path has changed to the output capacitance (Coss) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation.

LEFT LEG TRANSITION
time t(2)<t<t(3)
Q_A = OFF, Q_C = ON, D_C = ON C_B = ↓, C_A = ↑

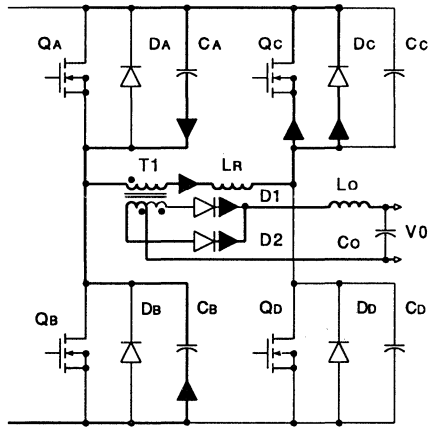

Figure 12

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial (IP(t(0)) value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

POWER TRANSFER INTERVAL
Time t(3) <t <t(4)

This interval of the phase shifted cycle is basically identical to that of conventional square wave power convesion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by Vin and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, Iout/N. The two time variant contributors to primary current are the magnetizing current (Imag) and the output inductor magnetizing contribution reflected to the primary, Lout/N^2. The exact switch ON time is a function of Vin, Vout and N the transformer turns ratio, just as with conventional converters.

POWER TRANSFER INTERVAL
time t(3)<t<t(4)
Q_B = ON, Q_C = ON

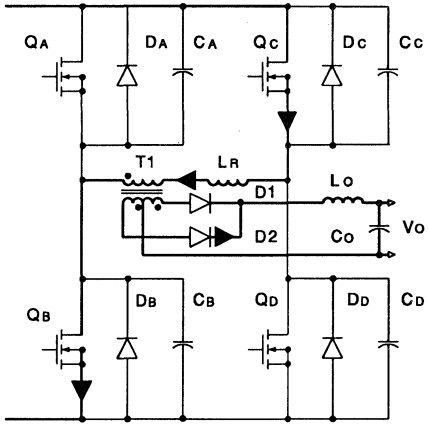

Figure 13

9

SWITCH TURN OFF; TIME t(4)

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, Coss. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, Vin. The output capacitance of the lower switch in the left hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage.

The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set QA and QD.

OPERATIONAL WAVE FORMS

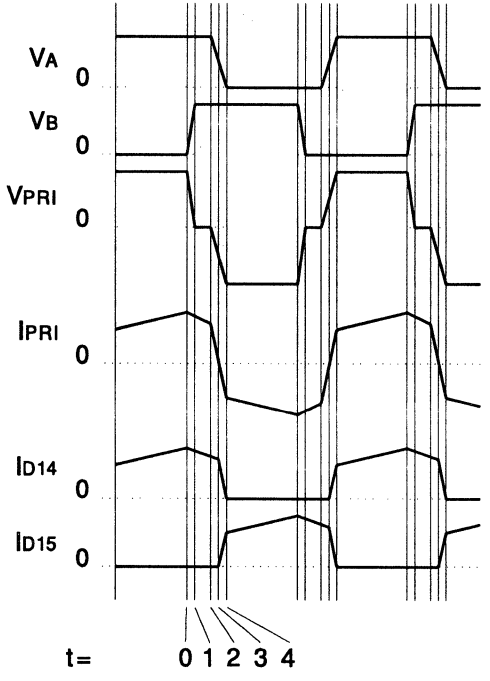

Figure 14

RESONANT TANK CONSIDERATIONS

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.

RESONANT CIRCUIT LIMITATIONS

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (Wr) of the tank circuit. Elements of this tank are the the resonant inductor (Lr) and capacitor (Cr), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance Cxfmr. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, Wr :

$$Wr = \frac{1}{(Lr \times Cr)\ \hat{}\ 0.5}$$

$$t(\max)\ transition = 4 \times Wr$$

Coss, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 * Coss. Transformer capacitance (Cxfmr) must also be added as it is **NOT** negligible in many high frequency applications.

The resonant capacitance, Cr :

$$Cr = [\,(\frac{8}{3}\,C_{oss}) + Cxfmr\,]$$

The capacitive energy required to complete the transition , W(Cr) is:

$$W(Cr) = \frac{1}{2} \times Cr \times VPri\text{^}2$$

This energy can also be expressed as:

$$W(Cr) = [\,(\frac{4}{3} \times Coss) + Cxfmr\,] \times Vin\text{^}2$$

STORED INDUCTIVE ENERGY

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, Lr:

$$W(Lr) = \frac{1}{2}\, x\, Lr\, x\, Ipri\text{^}2$$

RESONANT CIRCUIT SUMMARY

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships.

The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t(max) at light load.

$$Fres = 4 \times t(\max)$$

$$Fres = \frac{1}{t(res)} \quad or$$

$$t(res) = \frac{1}{Fres} = \frac{1}{(4 \times t(\max))}$$

where $Wr = 2 \times \pi \times Fres$

$$Wr = \frac{2 \times \pi}{t(res)}$$

Reorganizing and combining these relationships;

$$Wr = \left[\frac{(2 \times \pi)}{(4 \times t(\max))}\right]$$

$$Wr = \frac{\pi}{(2 \times t(\max))}$$

The resonant radian frequency (Wr) is related to the resonant components by the equation:

$$Wr = \frac{1}{(Lr \times Cr)\text{^}2}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$Lr = \frac{1}{(Wr\text{^}2 \times Cr)}$$

Previously outlined relationships for Wr and Cr can be introduced to result in the following specific equation.

$$Lr = \frac{1}{\left[\frac{\pi}{(2 \times t(\max))}\right]\text{^}2 \times \left[(\frac{8}{3} \times Coss) + Cxfmr\right]}$$

Note that this figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.

$$\frac{d\,IPri}{dt} = \frac{Vin}{Lr}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

STORED ENERGY REQUIREMENTS

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times Lr \times IPri(\min)\text{^}2 > \frac{1}{2} \times Cr \times Vin(\max)\text{^}2, \; or$$

$$Lr \times IPri(min)\text{^}2 > Cr \times Vin(\max)\text{^}2$$

Since Cr and Vin are known or can be estimated for a given application, this term becomes a constant and Lr has been quantified.

MINIMUM PRIMARY CURRENT

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$IPri(\min) = \left[\frac{(Cr \times Vin\text{^}2)}{Lr}\right]\text{^}0.5$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower that IP(min) it can be used as a confirmation of the mathematics.

$$IR(average) = Cr \times \frac{Vin}{t(\max)}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually cores loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

PHASE SHIFTED PWM CONTROL CIRCUITRY

Probably the most critical control aspect in the phase shifted PWM technique is the ability to span the full 0 to 180 degree phase shift range. Falling short of performance on either end of the spectrum can place unnecessary burdens on the fault protection circuitry or primary switches. Loss of control at either extreme will result in catastrophic consequences by simultaneously turning on both transistors in a given "leg" of the converter. The UC3875 Phase Shifted controller features the required circuitry to deliver both zero and effectively full duty cycle - effortlessly. Additionally, the UC3875 controller is utilized to perform the necessary control, decoding, protection and drive functions for this application. Peak current mode control is implemented for this example although the IC is equally suited for conventional voltage mode control, with or without input voltage feed forward. When used in current mode, the IC accepts a zero to 2.7 volt amplitude maximum current senses input and makes adding slope compensation a simple function.

UC3875 Block Diagram

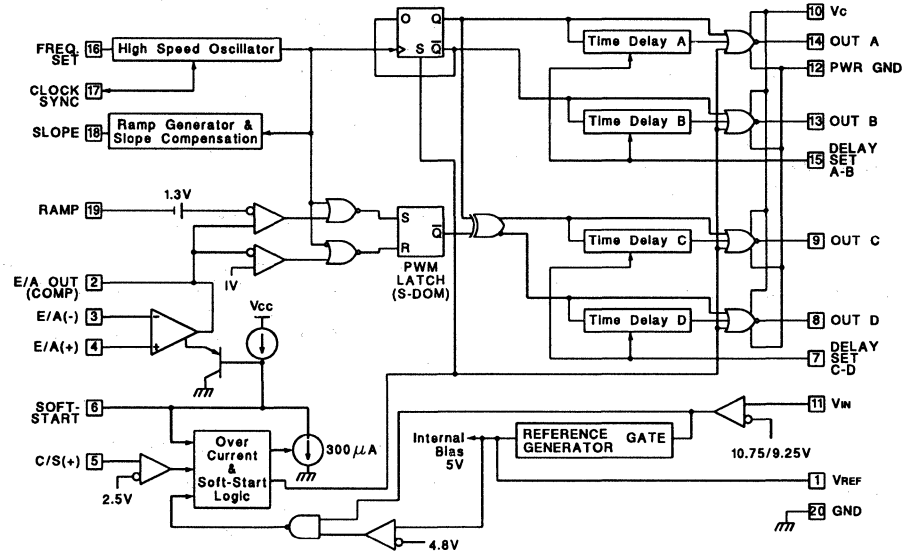

Figure 16

UNITRODE UC3875 PHASE SHIFTED PWM CONTROL IC - BLOCK DIAGRAM

A synchronizable oscillator is programmed by a resistor capacitor network from the frequency set pin to ground. Synchronization is performed by driving the SYNC pin from another UC3875 or external circuitry. The precision 5.0 volt bandgap reference is available to program the noninverting input of the error amplifier as well as optional external functions. Output regulation is achieved using the 7 MHz gain-band width on-board error amplifier which feeds the high speed PWM circuitry. Soft starting is accomplished with a capacitor to ground which gradually increases the error amplifier output, corresponding to pulse width, phase shift or peak current, depending on the exact implementation. This signal is compared to the Ramp input of the IC having a usable input range from zero to 2.7 volts.

Delays between the output drive commands to facilitate Zero Voltage Switching are programmed at the Delay Set inputs. One unique feature of the UC3875 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different primary currents during one switching cycle which cause and result in different resonant transition times between the leading and falling edges. Inability to program each of these durations will generally result in lossy, non-zero voltage switching of the full bridge converters switches under some operating conditions.

The four UC3875 output totem poles can each deliver a two amp peak gate drive current, more than adequate in a high frequency transformer coupled gate drive application. To minimize noise transmitted back to the analog circuitry, the output section features its own collector power supply (Vc) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply further enhances performance.

Fault protection is established by the programmable current limit circuitry. Full cycle restart corresponding to the time programmed by the soft start interval minimizes power dissipation in a short circuited output.

TYPICAL APPLICATION CIRCUIT SCHEMATIC SUMMARY

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. switching losses due to the simultaneous overlapof voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage acvantageously. For most applications, there is little reason to consider the traditional square wave counterpart of theis phase shifted PWM technique for future designs.

Very high frequency operation of this technique, beyond 500 KHz, is probable above the optimal operating point. Transition times quickly erode the usable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and repower loss in the switches. Any incremental gains in cost or power density by reducting the size of the output filter are probably nullified by the needs for larger MOSFETs and heatsinks. This phase shifted PWM technique does excel in the overall majority of mid to high power, off-line applications. Peak efficiency will be obtained in applications with moderate load ranges, however excellent results can also be obtained in most designs with load ranges of ten-to one. A subgroup of applications may exist where non ZVS operation extremely light loads is acceptable, especially when the advantages under all other operating conditions are considered. Additionally, the Unitrode UC3875 Phase Shifted Controlller IC has been introduced to simplify the control circuit design challenge. Features of the UC3875 include 2 MHz operation and four 2 amp peak totem-pole output drivers for high frequency applications. Separate programming of the different AD and BC leg transition intervals has made available to optimize converter performance.

Finally, the flexible control logic permits current mode or voltage mode control, with or without input voltage feed forward. The complexity of control, drive and protection of the fixed frequency phase shifted converter has been fully addressed in a single integrated solution.

UC3875 Phase Shifted PWM Converter
Control and Output Circuit Schematic

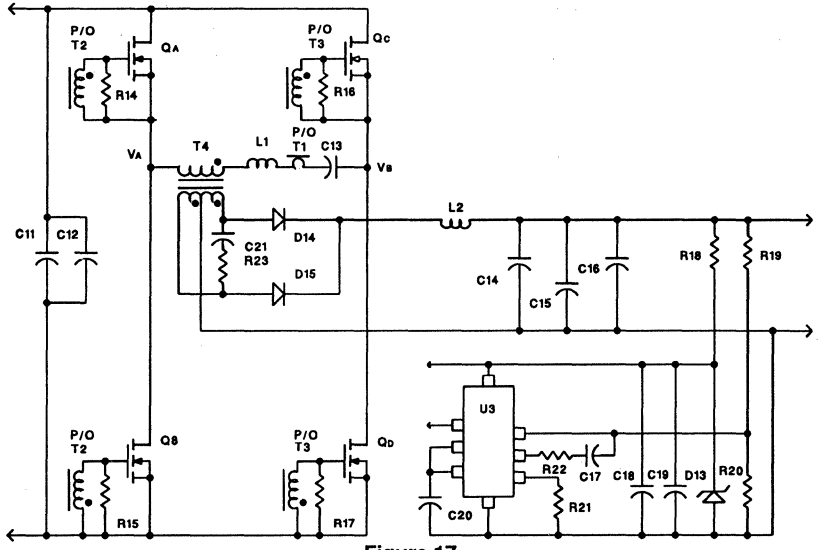

Figure 17

UC 3875 Phase Shifted PWM Converter
Control and Drive Circuit Schematic

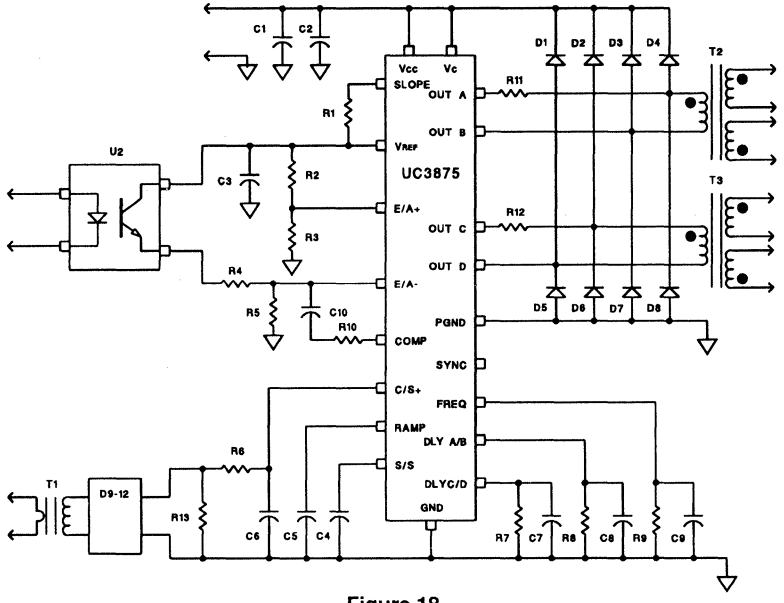

Figure 18

UC3875 F.B.P.S. CONVERTER

LIST OF MATERIALS

CAPACITORS

All are 20 VDC Ceramic Monolithic or Multilayer UNLESS "*" indicated.

C1= 1 µF
C2= 47 µF/25V ELECTROLYTIC
C3= 1 µF
C4= 1 µF
C5= 75 pF/16V POLYSTYRENE
C6= 0.001 µF
C7, 8= 0.01 µF
C9= 470 pF
C10= 0.1 µF
C11= 1 µF/450VDC POLY
C12= 47µ/450VDC ELECTROLYTIC
C13= 1.2µF/450 VDC POLY
C14= 1µF/100VDC
C15, 16= 220µF/63VDC ELECTROLITIC
C17= TBD
C18= 1µF
C19= 22 µF/25VDC ELECTROLITIC
C20= 1 µF
C21= 2.7 nF/200V POLY/low ESL&ESR

DIODES
D1-8= 1N5820 3A/20V SCHOTTKY
D9-12= 1N4148
D13= 12V 3W ZENER
D14, 15= 15A/200V FAST RECOVERY

INDUCTORS
L1= 47µH/3A
L2= 100µH/15A

MOSFET TRANSISTORS
QA-D=IRF840 NMOS

Bill Andreycak / UICC
2/24/93

RESISTORS

All are 1/2 Watt, 1%, Metal Film UNLESS "*" indicated

R1= 75K
R2= 2K
R3= 3K
R4= 470 Ohm
R5= 3K
R6= 100 Ohm
R7, 8= 6.8K
R9= 43K
R10= 150K
R11, 12= 10 Ohm
R13= 20 Ohm
R14-17= 10K
R18= 3.6K, 1WATT
R19= 36K
R20= 1K
R21= TBD
R22= TBD
R23= 110 Ohms/5W Carbon

TRANSFORMER
T1= 1 SENSE
T2, 3= GATE DRIVERS
T4= MAIN XFMR

INTEGRATED CIRCUITS
U1= UC3875 PMW
U2= OPTO
U3= UC19432

One Switching Cycle

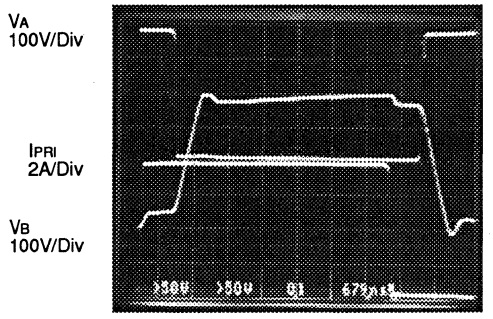

Figure 19

Primary Waveforms

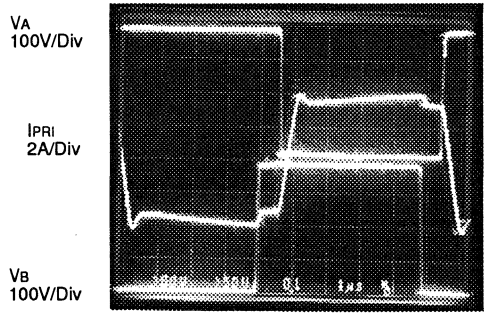

Figure 20

Secondary Waveforms

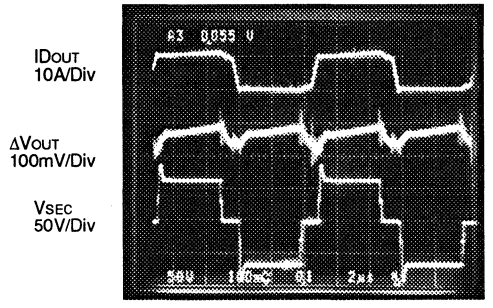

Figure 21

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APPLICATION NOTE

PRACTICAL CONSIDERATIONS IN HIGH PERFORMANCE MOSFET, IGBT and MCT GATE DRIVE CIRCUITS

BILL ANDREYCAK

INTRODUCTION

The switchmode power supply industry's trend towards higher conversion frequencies is justified by the dramatic improvement in obtaining higher power densities. And as these frequencies are pushed towards and beyond one megahertz, the Mosfet transition periods can become a significant portion of the total switching period. Losses associated with the overlap of switch voltage and current not only degrade the overall power supply efficiency, but warrant consideration from both a thermal and packaging standpoint. Although brief, each of the Mosfet switching transitions can be further reduced if driven from from a high speed, high current totem-pole driver - one designed exclusively for this application. This paper will highlight three such devices; the UC1708 and UC1710 high current Mosfet driver ICs, and the UC1711 high speed driver. Other Mosfet driver ICs and typical application circuits are featured in UNITRODE Application Note U-118.

EFFECTIVE GATE CAPACITANCE

The Mosfet input capacitance (Ciss) is frequently misused as the load represented by a power mosfet to the gate driver IC. In reality, the effective input capacitance of a Mosfet (Ceff) is much higher, and must be derived from the manufacturers' published total gate charge (Qg) information. Even the specified maximum values of the gate charge parameter do not accurately reflect the driver's instantaneous loads during a given switching transition. Fortunately, FET manufacturers provide a curve for the gate-to-source voltage (Vgs) versus total gate charge in their datasheets. This will be segmented into four time intervals of interest per switching transition. Each ofthese will be analyzed to determine the effective gate capacitance and driver requirements for optimal performance.

Inadequate gate drive is generally the result of underestimating the effective load of a power mosfet to its driver.

TOTAL GATE CHARGE (Qg)

First, a typical high power Mosfet "Gate Charge versus Gate-to-Source Voltage" curve will be examined. An IRFP460 device has been selected and this curve is applicable to most other Fet devices by adjusting the gate charge numbers accordingly. Both turn-on and turn-off trasnsitions are shown with the respective drain currents and drain-to-source voltages.

TURN-ON WAVEFORMS
Gate voltage vs time

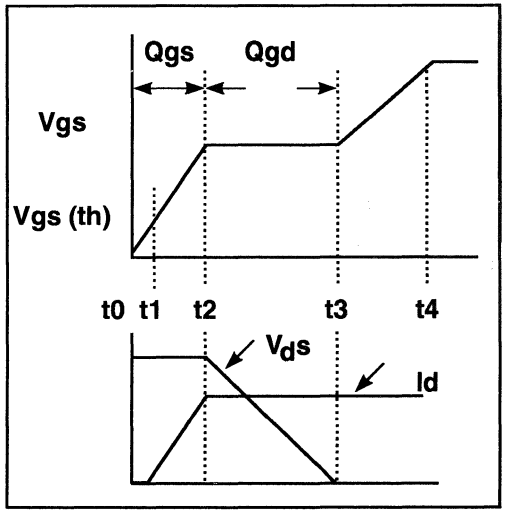


Figure 1.

INTERVAL t0-t1

The time required to bring the gate voltage from zero to its threshold Vgs(th) can be expressed as a delay time. Both the voltage across the switching device and current through it are uneffected during this interval.

INTERVAL t1-t2

This period starts at time t1 when the gate voltage has reached Vgs(th) and drain current begins to flow. Current continues to rise until essentially reaching its final value at time t2. While this occured, the gate to source voltage had also been increasing. The drain-to-source voltage remains unchanged at Vds(off). Power in the Mosfet is wasted by the simultaneous overlap of voltage and current.

INTERVAL t2-t3

Beginning at time t2 the drain-to-source voltage starts to fall which introduces the "Miller" capacitance effects (Cgd) from the drain to the Mosfet gate. The result is the noticeable plateau in the gate voltage waveform from time t2 until t3 while a charge equal to Qgd is admitted. It is here that most drive circuits are taxed to their limits. The interval concludes at time t3 when the drain voltage approaches its minimum.

INTERVAL t3-t4

During this final interval of interest the gate voltage rises from the plateau of the prior region up to its final drive voltage. This increasing gate voltage decreases Rds(on), the Mosfet drain-to-source resistance. Bringing the gate voltage above 10 to 12 volts, however, has little effect on further reducing Rds(on).

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t0-t1	0-threshold	0	Vds(off)	Slew rate (dv/dt)
t1-t2	thrs-plateau	rising	Vds(off)	Slew rate (dv/dt)
t2-t3	V(plateau)	Ion(dc)	falling	Peak current I(max)
t3-t4	rising	Ion(dc)	Ion*Rds(t)	Peak I & dv/dt

TURN-OFF WAVEFORMS
Gate voltage vs time

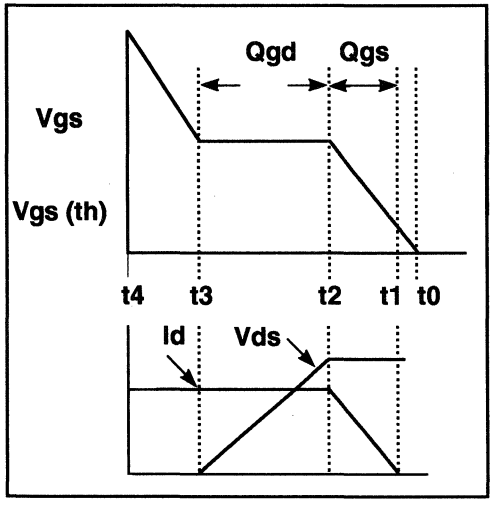


Figure 2

The intervals during turn-off are basically the same as those described for turn-on, however the sequence and corresponding waveforms are reversed.

INTERVAL t4-t3

The beginning of the turn-off cycle can be described as a delay from the final drive voltage (Vgs(on)) the the plateau region. Both the drain voltage and current waveforms remain unchanged while the devices effective resistance (Rds(on)) increases as the gate voltage decreases.

INTERVAL t3-t2

Once the plateau is reached at time t3, the gate voltage remains constant until time t2. Gate charge due to the Miller effect is being removed, an amount equal to Qgd. The drain voltage rises to its off state amplitude, Vds(off), while the drain current continues to flow and equals I(on). This lossy transition ends at time t2.

INTERVAL t2-t1

Once the Miller charge is completely removed, the gate voltage is reduced from the plateau to the threshold voltage causing the drain current to fall from I(on) to zero. Transition power loss ends at time t1 when the gate threshold is crossed.

INTERVAL t1-t0

This brief period is of little interest in the turn-off sequence since the device is off at time t1.

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t4-t3	falling	Ion(dc)	Ion* Rds(t)	Peak I and dv/dt
t3-t2	V(plateau)	Ion(dc)	falling	Peak Current I (max)
t2-t1	Vplat-thrsh	falling	Vds(off)	Slew rate (dv/dt)
t1-t0	thrsh-0	0	Vds(off)	Slew rate (dv/dt)

FET Transition Power Loss

During each of the FET turn-on and turn-off sequences power is lost due to the switching device's simultaneous overlap of drain - source voltage and drain current. Since both the FET voltage and current are externally controlled by the application, the driver IC can only reduce the power losses by making the transition times as brief as possible. Minimization of these losses simply requires a competant driver IC, one able to provide high peak currents with high voltage slew rates.

A review of the prior transition waveforms indicates that power is lost between the times of t1 and t3. While t2 serves as the pivot point for which waveform is rising or falling, as the equations show its irrelavent in the power loss equation. For the purpose of brevity, the waveform of interest can be approximated as a triangle while the other waveform is constant. The duration between times t1 and t3 can now be defined as the net transition time, t(tran), with a conversion period of t(period)

During the two intervals from t1 to t3:

$$Ploss = \frac{0.5 * I(on) * Vds(off) * t(2\text{-}1)}{t(period)}$$

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(3\text{-}2)}{t(period)}$$

Combininig the two equations with t(tran) = t3-1 results in a net loss of :

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(trans)}{t(period)}$$

Since these loses are incurred twice percycle, first at turn-on and then again at turn-off, the net result is a doubling of the power loss.

Ploss = Vds(off)*I(on)*t(trans)/t(period)

This relationship displays the need for fast transitions at any switching frequency, and is of significant concern at one megaHertz. Minimization of the FET transition power loss can be achieved with high current drivers.

GATE CHARGE

Each division of the transition interval has an associated gate charge which can be derived from the FET manufacturers datasheets. Since there are three basic shapes to the Vgs curve, the interval from t0 to t1 can be lumped together with that of the t1 to t2 period. For most large FET geometries, the amount of charge in the t0 to - t1 span is negligible anyway. This simplification allows an easy calculation of the effective gate capacitance for each interval along with quantifying the peak current required to traverse in a given amount of time.

Charge can be represented as the product of capacitance multiplied by voltage, or current multiplied by time. The effective gate capacitance is determined by dividing the required gate charge (Qg) by the gate voltage during a given interval. Likewise, the current necessary to force a transition within a specified time is obtained by dividing the gate charge by the desired time.

Cgs (effective) = delta Qg / delta Vgs

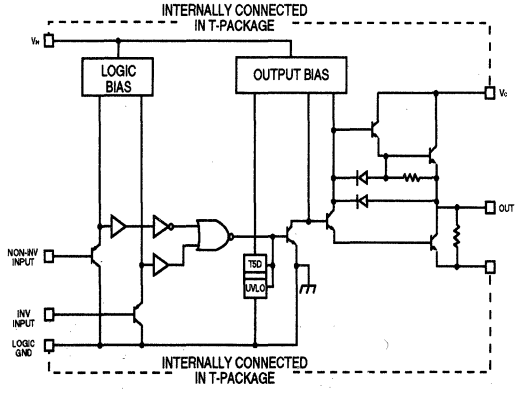
Ig(required) = delta Qg / t(transition)

UC1710
The "MILLER KILLER"

High peak gate drive currents are desirable in paralleled FET applications, typical of a high power switching section or power factor correction stage. Dubbed as "the Miller Killer", the UC1710 boasts a guaranteed 6 amp peak output current. This hefty driver current minimizes the FET parasitic "Miller" effects which would otherwise result in poor transi-

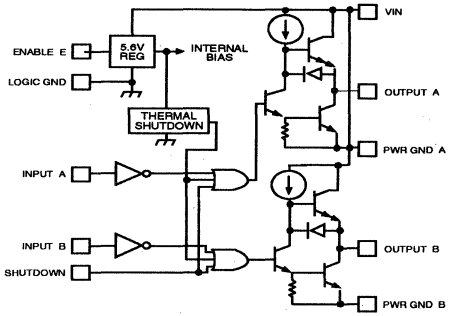
tion performance. Higher currents are possible with this driver, however the limiting factor soon becomes the parasitic series inductance of the FET package (15 nH) and the layout interconnection of 20 nH/inch. An RF type arrangement of the PC board layout is an absloute **MUST** to realize this device's full potential.

UC 1710 BLOCK DIAGRAM



The UC1710 has "no-load" rise and fall times of 20 nanoseconds (or less) which do not change significantly with any loads under 3 nanoFarads. It's also specified into a load capacitance of 30 nanoFarads, roughly equivalent to what is represented by three paralleled "size 6" FET devices. Propagation delays are brief with typical values specified at 35 nanoseconds from either input to a ten percent change in output voltage.

UC 1708 BLOCK DIAGRAM



The UC1708 is a unique blend of the high speed attributes of the UC1711 along with the higher peak current capability of the UC1710. This dual noninverting driver accepts positive TTL/CMOS logic from control circuits and provides 3 amp peak outputs from each totem pole.

Propagation delays are under 25 nanoseconds while rise and fall times typically run 35 nonoseconds into 2.2 nanofarads. The output stage design is a "no float" version which incorporates a self biasing technique to hold the outputs low during undervoltage lockout, even with Vin removed.

In the 16 pin DIL package, the device features a remote ENABLE and SHUTDOWN function in addition to seperate signal and power grounds. The ENABLE function places the device in a low current standby mode and the SHUTDOWN circuitry is high speed logic directly to the outputs.

UC1708 / 1710 / 1711 PERFORMANCE COMPARISON
TABLE 1.

PARAMETER	LOAD	UC1708	UC1710	UC1711
Propagation Delay t(plh) input to 10% output	0 1.0 nF 2.2 nF 30 nF	25 25 25 -	30 - 30 30	10 15 20 -
Raise time t(tlh) 10% to 90% rise	0 1.0 nF 2.2 nF 30 nF	25 30 40 -	20 - 25 85	12 25 40 -
Propagation Delay t(phl) input to 90% output	0 1.0 nF 2.2 nF 30 nF	25 25 25 -	30 - 30 30	3 5 -
Fall Time t(thl) 90% to 10% fall	0 1.0 nF 2.2 nF 30 nF	25 30 40 -	15 - 20 85	7 25 40 -

TRANSITION PERFORMANCE

Using the table above, the driver output slew rates and average current delivered can be calculated. The figures can be compared to lower power op-amps or comparators to gain a perspective on the relative speed of these high performance drivers.

The UC 1708 delivers output slew rates (dv/dt) in the order of 300 to 480 volts per microsecond, at average load currents of under one amp, depending on the load. The high speed UC1711 exhibits similar characteristics under loaded conditions, but can achieve a no load slew rate of over 1700 volts per microsecond - nearly 2 volts per nanosecond.

For higher power applications, the UC1710 "Miller Killer" will produce an average current of 4.5 amps AT slew rates of 150 volts per microsecond. With lighter loads it will deliver an average current of 1.5 amps at a slew rate of approximately 500 volts per microsecond. In most applications, the UC1710 will easily outperform "homebrew" discrete mosfet transistor totempole drive techniques.

Each device in this new generation of MOSFET drivers is significantly more responsive than the earlier counterparts for a given application - whether it's higher speed (UC1711), higher peak current (UC1710) or a combination of both (UC1708).

DRIVER CONSIDERATIONS

As previously demonstrated, the ideal MOSFET gate drive IC is a unique blend of both high speed switching and high peak current capability. Initially, the high speed is required to bring the gate voltage from zero to the plateau, but the current is low. Once the plateau is intersected, the driver voltage is fairly constant, and the IC must switch modes. Instantly, the driver current snaps to its maximum as charge is injected to overcome the FET's Miller effects. Finally, a combination of both high slew rate and high current is needed to complete the gate drive cycle.

At turn-off this sequence is reversed, first demanding both high slew rate and high current simultaneously. This is followed by the plateau region which is limited only by the maximum driver current. Finally, there is high speed discharge of the gate to zero volts.

Optimization of a driver for this type of application can be difficult. In general, the MOSFET driver IC output stage is designed to switch as fast as the manufacturer's process will allow.

CROSS CONDUCTION

There are numerous tradeoffs involved in the design of these drivers beyond the obvious choices of number of outputs and peak current capability. Cross-conduction is defined as the conduction of current through both of the totem pole transistors simultaneously from Vin to ground. It is an unproductive loss in the output stage which results in unnecessary heating of the driver and wasted power. Cross conduction is the result of turning one transistor ON before the opposing one is fully off, a compromise often necessary to minimize the input to output propagation delays.

An interesting observation is that cross-conduction is less of a concern with large capacitive loads (FETs) than with unloaded or lightly loaded driver outputs. Any capacitive load will reduce the slew of the output stage, slowing down its dv/dt. This causes a portion of the cross conduction current to flow from the load, rather than from the input supply through the driver's opposite output transistor. The power loss associated with a drivers inherent cross-conduction is unchanged with large capacitive loads, however it is not caused by a "shoot-through" of supply current.

DRIVER PERFORMANCE

There are a variety of applications for MOSFET drivers - each with its own unique set of speed and peak current requirements. Most general purpose drivers feature 1.5 amp peak totem-pole outputs which deliver rise and fall times of approximately 40 nanoseconds into 1 nanoFarad. Propagation delays are in the neighborhood of 40 to 50 nanoseconds, making these devices quite adaptable to numerous power supply and motor control applications. These specifications can be used for a comparison to those of a new series of higher speed and higher current devices, specifically, the UC1708, UC1710 and the UC1711 power MOSFET drivers. Each member in this group of "third" generation driver ICs features significant performance improvements over their predecessors with one parameter optimized for a specific set of applications.

MOSFET DRIVER IC FEATURE AND PERFORMANCE OVERVIEW
TABLE 2.

Feature	UC1708	UC1710	UC1711
Number of outputs Peak output current (per output)	2 3 A	1 6 A	2 1.5 A
Noninverting input-output logic Inverting input-output logic	YES	YES YES	 YES
Maximum supply voltage Vcc Typical supply current Icc (1.)	35V 16ma	20V 30ma	40V 17ma
Remote Enable Shutdown Input	YES YES	 YES (2)	
Seperate grounds, signal and power Seperate Vin and Vc pins	YES (3)	YES (3) YES (3)	
8 pin DIL package 16 pin DIL package 5 pin TO-220 package	YES YES	YES YES YES	YES YES

Note 1. Typical Vc plus Vcc current measured at 200KHZ, 50 % duty cycle and no load
Note 2. Using the device's other input
Note 3. Package dependant

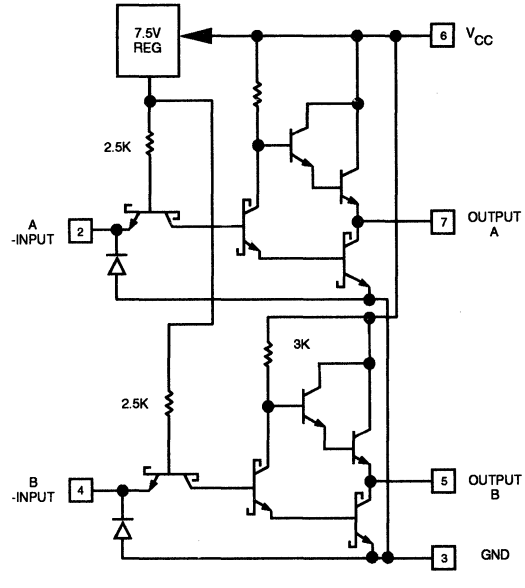
PROPAGATION DELAYS

The power supply industry's trend towards higher power densities has thrust switching frequencies well beyond one megaHertz in many low to medium power systems. With a one microsecond total conversion period, or less, the FET switching transitions should be in the order of low tens of nanoseconds to yield high efficiency. Additionally, the propagation delays from the driver input to output should be around ten nanoseconds for quick response.

UC1711

The UC1711 device features typical propagation delays of three and ten nanoseconds at no load, depending on the transition. Coupled with dual 1.5 amp peak totem-pole outputs, this device is optimized for high frequency FET drive applications. Its all NPN Schottky transistor construction is not only fast, but radiation tolerant as well.

UC1711 BLOCK DIAGRAM



GATE DRIVE POWER CONSIDERATIONS

Perhaps the most popular misconception in the power supply industry is that a FET gates require NO power from the auxiliary supply - that both turn-on and turn-off are miraculously power free. Another fallacy is that the driver consumes all the measured supply current, Icc, and none of it is used to transition the gates. Obviously, both of these statements are false.

In reality, the power required by the gate itself can be quite substantial in high frequency applications. Calculation of this begins by listing the specified total gate charge for the FET device, Qg.

The gate power utilized in charging and discharging a capacitor at frequency "F" is:

P(cap) = C * V^2 * F

Substituting the gate charge for capacitance multiplied by voltage (Q=C*V) in this equation results in:

P(gate) = Qg * V * F

The gate power required verses FET size and switching frequencies is tabulated for some common applications in Table 3. Table 4. transforms this power into driver input current at a nominal 12 volt bias.

GATE POWER (mW) VS. SWITCHING FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	10	18	28	36	46	90	136	180
SIZE 2	16	30	46	60	76	153	226	300
SIZE 3	28	54	82	108	136	275	406	504
SIZE 4	48	96	144	192	240	480	720	960
SIZE 5	100	200	300	400	550	1W	1.5W	2W
SIZE 6	144	288	432	576	720	1.4W	2W	>2W

Table 3.

DC SUPPLY CURRENT (mA) VS. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	1	1	2	4	5	6	10	12
SIZE 2	1	2	4	5	6	10	16	20
SIZE 3	2	4	6	8	10	16	26	36
SIZE 4	4	8	10	12	16	32	48	64
SIZE 5	8	14	20	26	32	66	100	130
SIZE 6	10	20	28	38	48	96	144	190

Table 4.

The driver output stage can be modelled as a resistance to the respective auxiliary supply rail driving an ideal FET capacitor. All of the power used to charge and discharge the MOSFET gate capacitor is completely transferred into heat by the driver. This gate power loss adds to the driver's own power loss - resulting in a net driver power dissipation equal to it's input voltage, Vcc, multiplied by the sum of the gate and driver currents, Ig + Icc. This can be calculated or determined empirically by measuring the driver DC input voltage and current.

THERMAL CONSIDERATIONS

Proper IC package selection and/or device heatsinking is the only method available to insure a safe operating junction temperature, tj. All IC's are specified and graded for various junction temperature ranges, and priced accordingly. As a precaution, it should be noted that using a device outside its tested temperature range can result in poor performance, parameters which run outside their specifications, and quite possibly - no operation at all.

JUNCTION TEMPERATURE

The junction temperature of the driver IC is obtained by first calculating the device's thermal rise above the ambient temperature. This is obtained by multiplying the average input power (Vin*Iin) by the device's thermal impedance to air, theta JA (Oja). This term is then added to the ambient temperature to yield the resulting junction temperature, Tj.

If the driver is thermally attached to a heatsink or "cold plate", then the thermal impedance from the device junction to it's package case, theta JC (Ojc), is used to determine the thermal rise. Likewise, this thermal rise is added to the heatsink temperature to determine the junction temperature. In either case, the maximum junction temperature (tj(max)) should be determined and checked against the device's absolute maximum specification.

Average supply currents for each of the three drivers of interest varies primarily with the switching frequency. Rather than listing each driver independantly, an rough approximation of 25 milliamps will be used as the driver current, regardless of the specific device utilized and switching frequency. In addition, a typical supply voltage of 12 volts results in a power dissipation by the driver itself of 300 milliwatts.

The calculated gate power of Table 5. has been added to the estimated 300mW of device power to formulate Table 6. - the driver total power dissipation. This is of particular interest in selecting a driver package (8 pin, TO-220, etc) and heatsink determination for a specific maximum junction temperature, or rise. Typical junction temperature rises vs. frequency and FET size for a IC package, and recommendations are shown in table 7.

AVERAGE POWER DISSIPATION (mW) VS. FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	310	318	3 28	336	346	390	436	480
SIZE 2	316	330	346	360	376	452	526	600
SIZE 3	328	354	382	408	436	570	706	840
SIZE 4	348	396	444	492	540	780	1.0W	1.3W
SIZE 5	400	500	600	700	800	900	1.7W	2.4W
SIZE 6	444	588	732	876	1.0W	1.7W	2.5W	3.1W

Table 5.

PACKAGE RECOMMENDATIONS

For P(diss) = or < 500mW
A: 8 pin DIL, <40 C rise
B: 8 pin DIL, <45 C rise
C: 8 pin DIL, <50 C rise

For P(diss) = or > 500mW (using heatsink)
D: 8 pin DIL, <40 C rise
E: 8 pin DIL, <50 C rise

For P (diss) > 500mW
F: TO-220 recommended

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	A	A	B	B	B	C	D	D
SIZE 2	A	B	B	B	C	D	D	D
SIZE 3	B	B	C	D	D	D	E	F
SIZE 4	B	C	D	D	D	F	F	F
SIZE 5	C	D	D	E	F	F	F	F
SIZE 6	D	D	E	F	F	F	F	F

Table 6.

HIGH POWER APPLICATIONS

Most high power applications require the use of "monster" MOSFETs or several large FETs in parallel for each switch. Generally, these are low to medium frequency applications (less than 200kHz) where obtaining a low Rds(on) is of primary concern to minimize the DC switch loss. It is not uncommon to find two, three and even four large devices used in parallel, although some of these combinations are unlikely from a cost versus performance standpoint.

Table seven displays the individual FET device characteristics and several popular parallel arrangements. Listed in descending order is Rds (on) at room temperature and the total gate charge required. This will ultimately be used to determine the gate drive current in Table 8., total power dissipation in Table 9., and driver IC recommendation in Table 10 for various applications.

PARALLELED MOSFET CHARACTERISTICS - TABLE 7.

MOSFET ARRANGEMENT	Rds (on) effective	Qg (nC) total	MOSFET ARRANGEMENT	Rds (on) effective	Qg (nC) total
1 X SIZE 4	0.85	63	2 X SIZE 5	0.200	260
1 X SIZE 5	0.40	130	2 X SIZE 6	0.135	380
1 X SIZE 6	0.27	190	3 X SIZE 5 (1)	0.133	390
2 X SIZE 4 (1)	0.425	126	4 X SIZE 5 (1)	0.100	520
3 X SIZE 4 (1)	0.283	189	3 X SIZE 6 (2)	0.090	570
4 X SIZE 4 (1)	0.213	252	4 X SIZE 6 (2)	0.068	760

1. Consider another selection 2. Consider a "Monster" FET

AVERAGE SUPPLY CURRENT (mA) VS. FREQUENCY AND FET SELECTION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	31	39	45	51	65	77
2 X SIZE 6	135	35	45	53	63	83	101
3 X SIZE 6	90	39	53	69	73	91	139
4 X SIZE 6	68	45	63	82	101	139	177

*Includes 25mA of driver supply current

Table 8

POWER DISSIPATION (mW) VS. FREQUENCY AND APPLICATION

		SWITCHING FREQUENCY (kHz)					
FET ARRANGEMENT	Rds mohm	25	50	75	100	150	200
2 X SIZE 5	200	372	468	540	612	780	924
2 X SIZE 6	135	420	540	636	756	1.0W	1.2W
3 X SIZE 6	90	468	636	828	876	1.1W	1.7W
4 X SIZE 6	68	540	756	984	1.2W	1.7W	2.1W

* Includes 300mW of driver dissipation

Table 9.

DRIVER IC AND PACKAGE SELECTION GUIDE

Selection Guide for < 50 C rise

A: 8 pin DIL or 20 pin PLCC
B: 8 pin DIL with heatsink. or TO-220.
C: TO-220 with heatsink

		SWITCHING FREQUENCY (kHz)					
FET ARRANGEMENT	Rds mohm	25	50	75	100	150	200
2 X SIZE 5	200	A	B	C	C	C	C
2 X SIZE 6	135	B	C	C	C	C	C
3 X SIZE 6	90	B	C	C	C	C	C
4 X SIZE 6	68	C	C	C	C	C	C

Table 10.

UC1710 DRIVER PERFORMANCE

Although capacitive in nature, the FET "Miller" effects and demands on the driver differ significantly than a true capacitor load as previously described. Table 11. shows the typical response of the UC1710 "Miller Killer" driving a single APT5025BN (size 6) device and paralleled MOSFET combinations for reference.

UC1710 RISE, FALL AND DELAY TIMES VS. LOADS

TEST CONDITIONS		Tp LH	Tt LH	Tp HL	Tt HL	Tp +Tt LH	Tt +Tp HL
NO LOAD	VDS	28	12	36	12	40	50
ONE	0	28	26	38	30	54	68
APT5025	350	28	35	40	30	63	70
TWO	0	28	38	40	36	66	76
APT5025	350	28	48	42	38	76	80
THREE	0	28	48	42	48	76	90
APT5025	350	28	60	44	58	88	92

Table 11.

PERFORMANCE COMPARISONS

"HOMEBREW" TOTEM-POLES VS INTEGRATED CIRCUIT DRIVERS

The prior lack of "off-the-shelf" high current or high speed drivers had prompted many to design their own gate drive circuits. Traditionally, an NPN-PNP emitter follower arrangement had been used in lower frequency applications as shown in Figure 7.

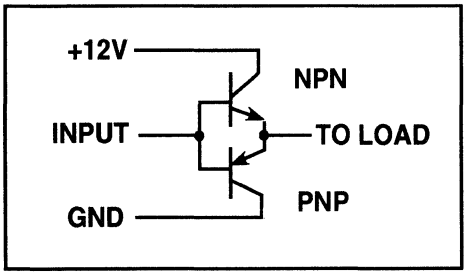


Figure 7

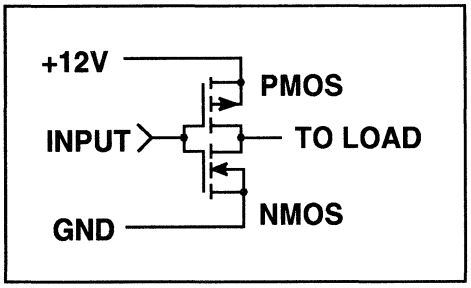


Figure 8

For higher speed applications, a P and N channel FET pair can be used as shown in figure 8. The circuit is configured with the P channel MOS as the upper side switch to simplify the auxiliary bias. Otherwise, a gate drive potential of ten volts above the auxiliary bias would required.

Unfortunately, this configuration has a few drawbacks. First, it leads to an inverting logic flow from the driver input to its output, complicating matters especially during power-up and power-down sequences. Without a clever undervoltage lockout circuit the main power switch will tend to be ON as the auxiliary supply voltage is raised or lowered while the PWM is OFF.

Cross conduction of both FETs is unavoidable with this configuration due to the difference between the gate threshold voltages of each device. Both P and N channel devices are cross conducting while their input drive waveform is above Vgs(th) of the N device and below that of the P device. One technique to minimize the cross conduction peak current is to add some resistance between the FETs. While this does minimize the "shoot-through" current, it also limits the peak current available to the load. This somewhat defeats the purpose of using the MOSFETs in the first place to deliver high currents. The resistor serves an additional purpose of damping the gate drive oscillations during the transitions. In a practical application, two resistors can be used in the place of one with the center-tap connecting to the FET gate,or load as shown in figure 9.

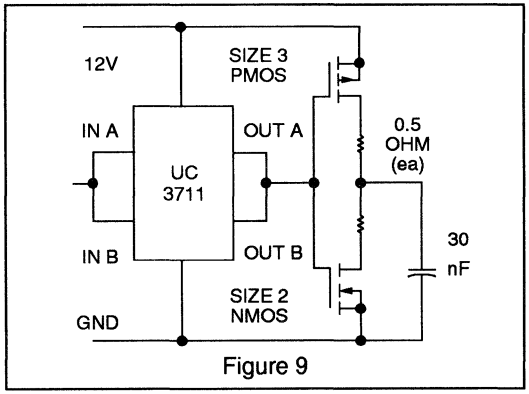
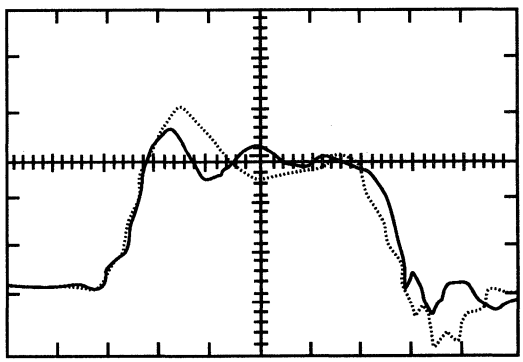


Figure 9

The performance of the circuit in figure 9 was evaluated and compared to that of the UC1710 driver into a 30 nanoFarad load. A size three P type FET and a size two N channel device were connected in series with two one-half ohm resistors to limit the shoot-through current. These FETs were driven from the UC1711 dual driver which can deliver 3 Amp peak gate drive currents for rapid transitions. The results of this test are shown in figure 10.

Driver Performance into 30nF load

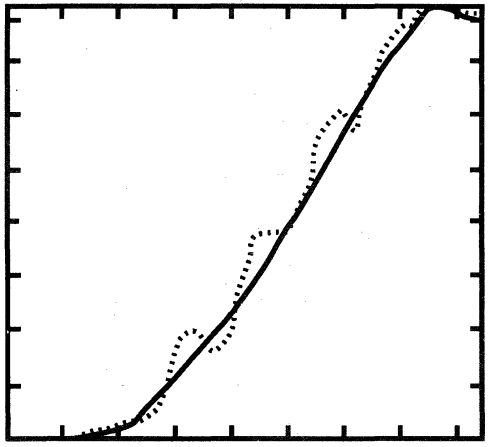


Lines: solid=UC3710, dashed=discrete
Figure 10. - VERT: 5V/DIV: HORIZ: 50 nS/DIV

The test results indicate very similar performance into this load from either technique. Obviously, the "homebrew" approach utilizes a total of three devices in comparison to a single UC1710 driver to obtain essentially the same high speed performance. Additionally, the cost of the P channel FET alone may exceed the price of the UC1710 device, not to mention the difference in PC board real estate. As a final note, the discrete FET approach required over 10 milliamps more supply current than the single UC1710 driver or a increase in supply current of twenty percent. Results of this test shown in figures 11 and 12.

RISE AND FALL TRANSITION PERFORMANCE INTO 30 nF

RISE TIMES (Fig 11.)



FALL TIMES (Fig 12.)

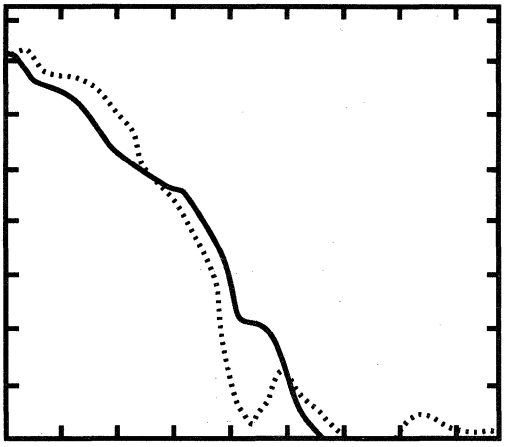


PHOTO SCALES (BOTH): VERT=2V/DIV, HORIZ=10 nS/DIV
LINES: SOLID = UC3710; DASHED = DISCRETE CIRCUIT OF FIGURE 9.

POWER DEVICES

IGBTs and MCTs: While existing generations of power MOSFETs continue to be enchanced for lower RDS(on) and faster recovery internal diodes, alternative new devices have also been introduced. Among the most popular, and viable for high voltage high power applications are IGBTs (Insulated Gate Bipolar transistors) and MCTs (MOS Controlled Thyristors). Although frequently drawn as an NPN structure, the IGBT actually resembles a PNP bipolar transistor with an internal MOS device to control the base drive. Indicative by its description, the MCT is essentially an SCR structure also utilitzing a MOS drive stage. Both devices offer significant cost advantages over MOSFETs for a given power capability.

MOSFET, IGBT and MCT Gate Drives: There are numerous reasons for driving the MOSFET gate to a negative potential during the device's off state. Degradation of the gate turn-on threshold over time and especially following high levels of irradiation are amongst the most common. However, with IGBTs, the important concern is the ability to keep the device off following turn-off with a high drain current flowing. On larger IGBT's with ratings up to 300 Amps, inductive effects caused by the device's package alone can "kick" the effective gate-to-emitter voltage positive by several Volts at the die - even with the gate shorted to the emitter at the package terminals. Actually, this is the result of the high current flowing in the emitter lead (package) inductance which can less than 1nH. The corresponding voltage drop changes polarity at turn off, thus pulling the emitter below the gate, or ground. If high enough, a fast turn off will be followed by a parasitic turn-on of the

switch, and potential destruction of the semiconductor. Applying the correct amplitude of negative gate voltage can insure proper operation under these high current turn-off conditions. Also, the negative bias protects against turn-on from high dv/dt related changes that could couple into the gate through the "Miller" capacitance.

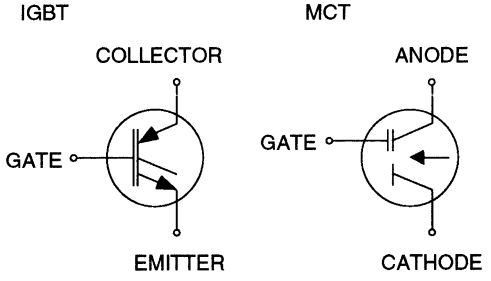


Figure 13 - IGBT and MCT Diagrams

Unlike power MOSFET switches, IGBT transconductance continues to increase with gate voltage. While most MOSFET devices peak with about 10 to 12 Volts at the gate, IGBT performance steadily improves up to the suggested 16 Volt maximum gate voltage. Typically, most IGBT manufacturers recommend a negative drive voltage between -5 and -15V. Generally, it is most convenient to derive a negative voltage equal in amplitude to the positive supply rail, and ±15V is common.

The gate charge required by an IGBT (for a given voltage and current rating) is noticeably less than that of a MOSFET. Part of this is due to the better utilization of silicon which allows the IGBT die to be considerably smaller than its FET counterpart. Additionally, the IGBT (being a bipolar transistor) does not suffer from the severe "Miller" effects of the MOS devices, easing the drive requirements in a given application. However, because of their advantages, most available IGBTs have fairly high gate charge demands - simply because of their greater power handling capability.

In contrast, MCTs (MOS Controlled Thyristors) exhibit the highest silicon utilization level among power switching devices. While relatively new to the market, these devices are quickly gaining acceptance in very high power (above several kilowatts) applications because of their high voltage (1000V) and high current (to 1000A) capability. Recently introduced parts boast maximum ratings to one megawatt, ideal for large industrial motor drives and high power distribution—even at the substation level. These devices are essentially MOS controlled SCRs and are intended for low frequency switchmode conversion. They will most likely replace high power discrete transistors, Darlingtons and SCRs because of their higher efficiency and lower cost.

Gate Charge and Effective Capacitance with Negative Bias: While several MOSFET and IGBT manufacturers recommend negative gate voltages in the device's off state, few publish any curves or information about gate charge characteristics when the gate is below zero Volts. This complicates the gate drive circuit design as each IGBT, MOSFET or MCT switch must be evaluated by the user over the ranges of operation conditions. A test fixture as shown in Figure 14 can be used to provide empirical generalizations for devices of interest. A switched constant current source/sink has been configured using a simple dual op-amp to drive a "constant" 1mA at the device under test (DUT). Gate voltage versus time can be monitored which provides the exact gate charge requirements for a given device. Any application specific requirements can also be accommodated by modifying the test circuit with external circuitry.

Negative Gate Charge - Empirical Data: Several MOSFET, IGBT and MCT gate charge measurements were taken to establish the general characteristics with negative gate charge and effective capacitance during this third quadrant operation was calculated and compared to of the first quadrant specifications from the manufacturers data sheets. Figure 15 demonstrates the general relationships of gate charges for comparison.

Both the IGBT and MCT have similar negative bias gate charge requirements as with an applied positive bias. The MOSFET, however, exhibits a slightly reduced gate charge in its negative bias region, somewhere between 70 and 75 percent of its positive bias charge. The MOSFET's more significant "Miller" effect in the first quadrant is responsible for this since the higher effective capacitance during the plateau region does not occur with negative bias.

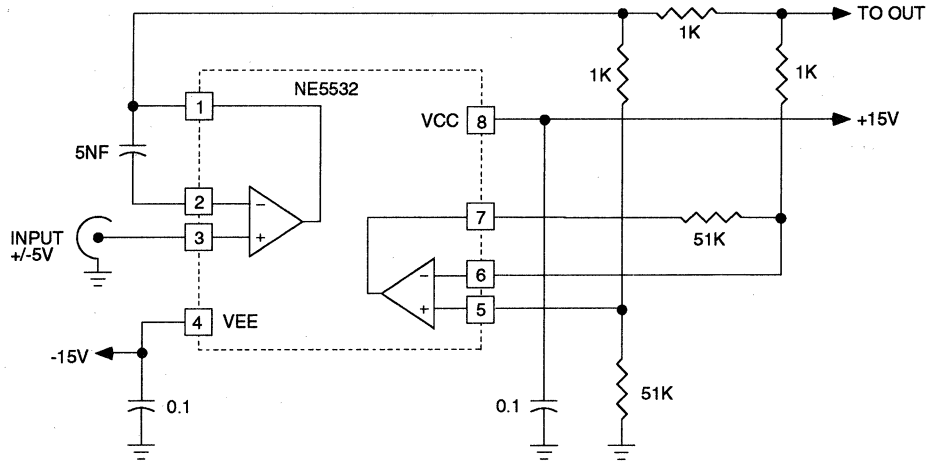


Figure 14 - Gate Charge Test Circuit

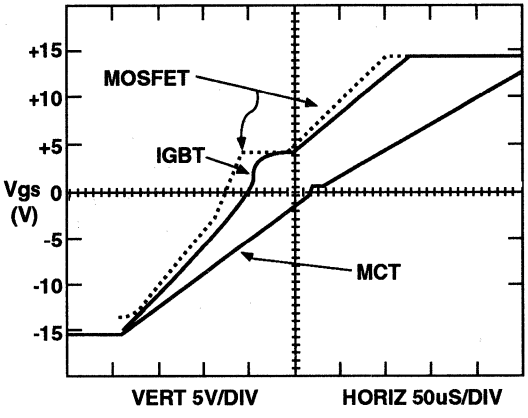


Figure 15 - Gate Charge Comparison Low to High Transition

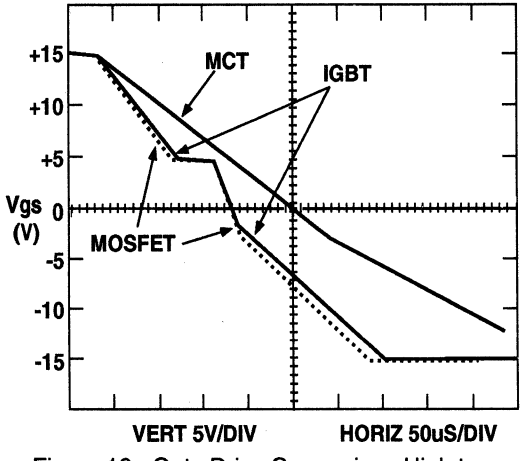


Figure 16 - Gate Drive Comparison High to Low Transition

Total Gate Power - Negative Drive Voltage Applications: All of the previously presented gate power equations still apply, however they must be modified to include the additional charge requirements of the negative supply voltage. For the sake of simplicity, a multiplication factor can be used for recalculation of the exact figures. When identical amplitudes of positive and negative supply voltages are used, for example ±15V, then the gate power utilized can be simply multiplied by a factor of two. This completes the process for the IGBTs and MCTs. The total MOSFET gate charge, on the other hand, should only be multiplied by a factor of 1.7 to 1.75 to accommodate the reduced negative bias demands. Additionally, if a negative supply voltage different than the positive rail voltage is used, for example +15 and -5, then the scaling factor must be adjusted accordingly. In this case, the new total gate power would be 1+ (-5/-15) or 1.33 times the initial 0-15V gate power for IGBTs and MCTs. The negative drive voltage scaling factor (-5/-15) would be multiplied by the 70 to 75% index if a MOSFET were used instead of an IGBT or MCT. This would result in a 1.23 to 1.25 times net increase over the initial (0-15V) gate power demand.

SUMMARY

The need for higher speed and higher current FET driver ICs has become increasingly apparent as power conversion switching frequencies are pushed towards and beyond one megaHertz. Likewise, the quest for higher overall efficiencies has resulted in creation of large, even "monster" size MOSFET geometries. These industry trends have stimulated the development of innovative MOSFET driver ICs - ones which would significantly outperform any of their predecessors, including discrete versions.

A new generation of high speed and high current MOSFET drivers has been presented. Each optimized for a unique blend of these attributes, the UC1708, UC1710 and the UC1711 devices successfully conquer the challenges of obtaining rapid transitions in MOSFET gate drive circuits.

REFERENCES

UNITRODE Application Note U-118, " New Driver IC's Optimize High Speed Power MOSFET Switching Characteristics" , UNITRODE LINEAR IC DATA-BOOK, IC 600

INTERNATIONAL RECTIFIER Application Notes AN-937, AN-947 and Datasheets, I.R. HEXFET Power MOSFET Designers Manual HDB-4

ADVANCED POWER TECHNOLOGY Databook 1989

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220
UC1706/3706 UC1707/3707	Dual High Current MOSFET Compatible Output Driver Dual Uncommitted High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Conversion (1706 Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	16 Pin DIL "Batwing"
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25n Sec Rise and Fall Times • 25n Sec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8-Pin DIL 16-Pin DIL
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8Pin DIL
UC1710/3710	High Current/Speed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8 Pin DIL 5 Pin TO-220
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 15nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8-Pin DIL
UC3724 UC3725 (PAIR)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600kHz Carrier Capability • Local Current Limiting Feature	8 Pin DIL (Pair)

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Zero Voltage Switching Resonant Power Conversion

Bill Andreycak

Abstract

The technique of zero voltage switching in modern power conversion is explored. Several ZVS topologies and applications, limitations of the ZVS technique, and a generalized design procedure are featured. Two design examples are presented: a 50 Watt DC/DC converter, and an off-line 300 Watt multiple output power supply. This topic concludes with a performance comparison of ZVS converters to their square wave counterparts, and a summary of typical applications.

Introduction

Advances in resonant and quasi-resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Currently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals and relevant voltage and current waveforms.

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicized by another at various power conferences [2,3]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters [4,5,6,7,8]. In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the MOSFET output capacitance (C_{OSS}) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique [9,10].

Zero Voltage Switching Overview

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.

Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly

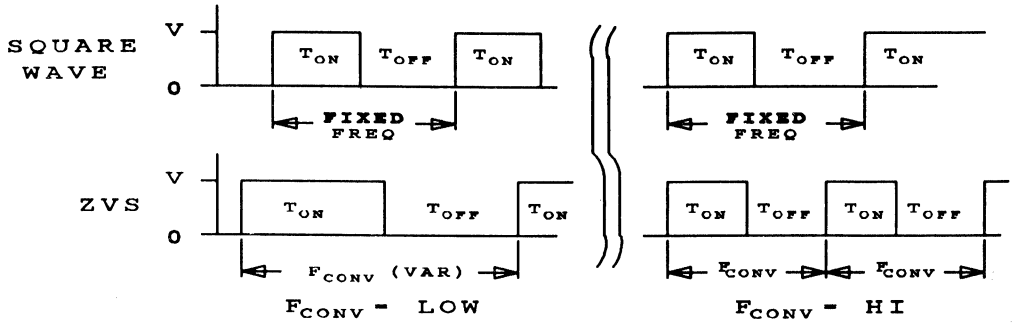

Fig. 1 - Zero Voltage Switching vs. Conventional Square Wave

unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (C_{OSS}) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V_{DS} equals zero.

The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, however a list of references describing the others has been included in the appendix.

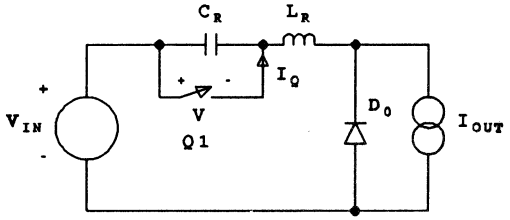

Fig. 2 - Resonant Switch Implementation

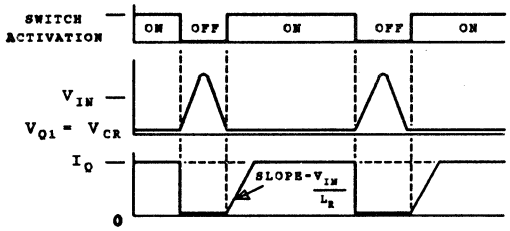

Fig. 3 - General Waveforms

ZVS Benefits

- Zero power "Lossless" switching transitions
- Reduced EMI / RFI at transitions
- No power loss due to discharging C_{OSS}
- No higher peak currents, (ie. ZCS) same as square wave systems
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and component *L* & *C*

9

- Reduced gate drive requirements (no "Miller" effects)
- Short circuit tolerant

ZVS Differences:

- Variable frequency operation (in general)
- Higher off-state voltages in single switch, unclamped topologies
- Relatively new technology - users must climb the learning curve
- Conversion frequency is inversely proportional to load current
- A more sophisticated control circuit may be required

ZVS Design Equations

A zero voltage switched Buck regulator will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevant polarities are shown in Fig. 4.

Typical design procedure guidelines and "shortcuts" will be employed during the analysis' for the purpose of brevity. At the onset, all components will be treated as though they were ideal which simplifies the generation of the basic equations and relationships. As this section progresses, losses and non-ideal characteristics of the components will be added to the formulas. The timing summary will expound upon the equations for a precise analysis.

Another valid assumption is that the output

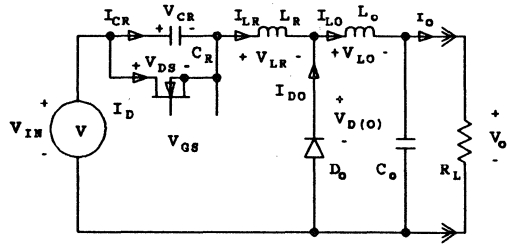

Fig. 4 - Zero Voltage Switched Buck Regulator

filter section consisting of output inductor L_O and capacitor C_O has a time constant several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value L_R and the magnetizing current ΔI_{Lo} as well as the inductor's DC resistance is negligible. In addition, both the input voltage V_{IN} and output voltage V_O are purely DC, and do not vary during a given conversion cycle. Last, the converter is operating in a closed loop configuration which regulates the output voltage V_O.

Initial Conditions: Time interval < t_0

Before analyzing the individual time intervals, the initial conditions of the circuit must be defined. The analysis will begin with switch Q_1 on, conducting a drain current I_D equal to the output current I_O, and $V_{DS} = V_{CR} = 0$ (ideal). In series with the switch Q_1 is the resonant inductor L_R and the output inductor L_O which also conduct the output current I_O. It has been established that the output inductance L_O is large in comparison to the resonant inductor L_R and all components are ideal. Therefore, the voltage across the output inductor V_{Lo} equals the input to output voltage differential; $V_{Lo} = V_{IN} - V_O$. The output filter section catch diode D_O is not conducting and sees a reverse voltage equal to the input voltage; $V_{Do} = V_I$, observing the polarity shown in Figure 4.

Table I - INITIAL CONDITIONS

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=V_{CR}=0$; $I_D=I_{LR}=I_{LO}=I_O$
D_O	OFF	$V_{DO}=V_{IN}$; $I_{DO}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
L_O		$V_{LO}=V_{IN}-V_O$; $I_{LO}=0$

Capacitor Charging State: t_0 - t_1

The conversion period is initiated at time t_0 when switch Q_1 is turned OFF. Since the current through resonant inductor L_R and output inductor L_O cannot change instantaneously, and no drain current flows in Q_1 while

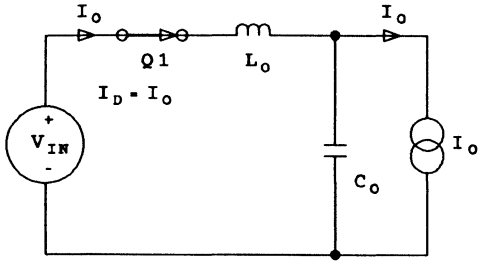

Fig. 5 - Simplified Model

$$V_{CR}(t) = \frac{I_O t}{C_R} \quad ; \quad t_{01} = \frac{C_R V_{IN}}{I_O}$$

$$I_{CR} = I_O \qquad for\ t_0 < t < t_1$$

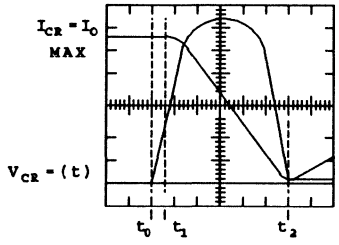

Fig. 6 - Resonant Capacitor Waveforms

it is off, the current is diverted around the switch through the resonant capacitor C_R. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage ($V_{CR} = V_{IN}$). Since the current is not changing, neither is the voltage across resonant inductor L_R.

At time t_0 the switch current I_D "instantly" drops from I_O to zero. Simultaneously, the resonant capacitor current I_{CR} snaps from zero to I_O, while the resonant inductor current I_{LR} and output inductor current I_{LO} are constant and also equal to I_O during interval t_{01}. Voltage across output inductor L_O and output catch diode D_O linearly decreases during this interval due to the linearly increasing voltage across resonant capacitor C_R. At time t_1, V_{CR} equals V_{IN}, and D_O starts to conduct.

Table II - CAPACITOR CHARGING: t_0 - t_1

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$I_D = 0$; $V_{DS(t)} = V_{CR(t)}$
C_R	Charging	$I_{CR} = 0$; $V_{CR(t)}$ RISES LINEARLY $V_{CR(t0)} = 0$; $V_{CR(t1)} = V_{IN}$
L_R		$I_{LR(t)} = I_O$; $V_{LR} = 0$
D_O	OFF	$V_{DO(t0)} = V_{IN}$; $V_{DO(t1)} = 0$; DECREASES LINEARLY
L_O		$V_{LO(t0)} = V_{IN} - V_O$; $V_{LO(t1)} = -V_O$ DECREASES LINEARLY ; $I_{LO} = I_O$

Resonant State: t_1 - t_2

The resonant portion of the conversion cycle begins at t_1 when the voltage across resonant capacitor V_{CR} equals the input voltage V_{IN}, and the output catch diode begins conducting. At t_1, current through the resonant components I_{CR} and I_{LR} equals the output current I_O.

The stimulus for this series resonant L-C circuit is output current I_O flowing through the resonant inductor prior to time t_1. The ensuing resonant tank current follows a cosine function beginning at time t_1, and ending at time t_2. At the natural resonant frequency ω_R, each of the *L-C* tank components exhibit an impedance equal to the tank impedance, Z_R. Therefore, the peak voltage across C_R and switch Q_1 are a function of Z_R and I_O.

The instantaneous voltage across C_R and Q_1 can be evaluated over the resonant time interval using the following relationships:

$$V_{CR(t)} = V_{CR(t1)} + \frac{I_O}{\omega_R C_R} \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

$$Z_R = 1/\omega_R C_R \quad ; \quad V_{CR(t1)} = V_{IN}$$

$$\therefore \quad V_{CR(t)} = V_{IN} + I_O Z_R \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

Of greater importance is the ability to solve the equations for the precise off-time of the switch. This off-time will vary with line and load changes and the control circuit must respond in order to facilitate true zero voltage switching. While some allowance does exist for a fixed off time technique, the degree of lati-

tude is insufficient to accommodate typical input and output variations. The exact time is obtained by solving the resonant capacitor voltage equations for the condition when zero voltage is attained.

$$Let\ V_{CR(t)} = 0\ ;\ I_O Z_R\ SIN(\omega_R(t-t_1)) = -V_{IN}$$

The equation can be further simplified by extracting the half cycle (180 degrees) of conduction which is a constant for a given resonant frequency, and equal to π/ω_R.

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin \left[\frac{V_{IN}}{I_O Z_R} \right]_{t_1}^{t_2}$$

The resonant component current ($I_{CR} = I_{LR}$) is a cosine function between time t_1 and t_2, described as:

$$I_{CR(t)} = I_O \cos\left[\omega_R(t-t_1)\right]_{t_1}^{t_2}$$

The absolute maximum duration for this interval occurs when 270 degrees ($3\pi/2\omega_R$) of resonant operation is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line voltage are approached.

Contributions of line and load influences on the resonant time interval t_{12} can be analyzed individually as shown in Figs. 7 and 8.

Prior to time t_1, the catch diode D_O was not conducting. Its voltage, V_{DO}, was linearly decreasing from V_{IN} at time t_0 to zero at t_1 while input source V_{IN} was supplying full output current, I_O. At time t_1, however, this situation changes as the resonant capacitor initiates resonance, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage, V_{DO}, changes polarity as it begins to conduct, supplementing the decreasing resonant inductor current with diode current I_{DO}, extracted from stored energy in output inductor L_O. The diode current waveshape follows a cosine function during this interval, equalling I_O minus $I_{CR}(t)$.

Also occurring at time t_1, the output filter inductor L_O releases the stored energy required

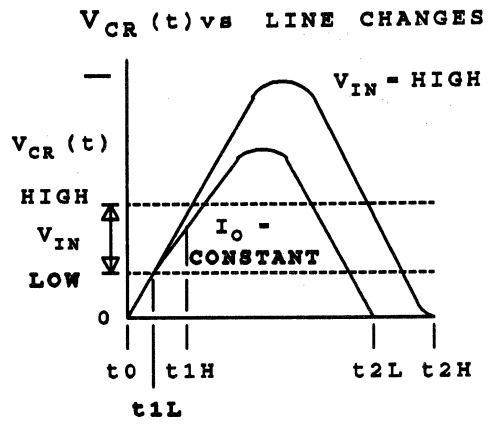

Fig. 7 -- Resonant Capacitor Voltage vs. Line

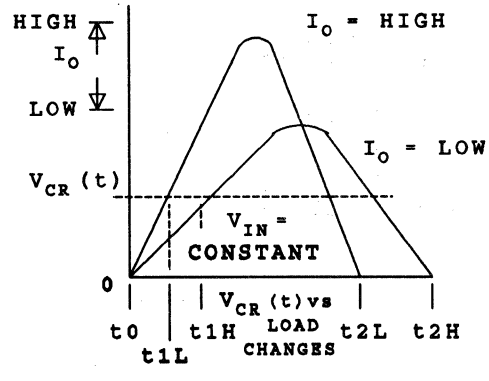

Fig. 8 -- Resonant Capacitor Voltage vs. Load

to maintain a constant output current I_O. Its reverse voltage is clamped to the output voltage V_O minus the diode voltage drop V_{DO} by the convention followed by Figure 4.

Table III - RESONANT INTERVAL: t_1 - t_2

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$V_{DS(t)} = V_{CR(t)}$
C_R	Resonant	$V_{CR(t)} = V_{IN} + (I_O Z_R \sin(\omega_R(t-t_1)))$ $I_{CR(t)} = I_O \cos(\omega_R(t-t_1))$
L_R	Resonant	$V_{LR(t)} = [I_O Z_R \sin(\omega_R(t-t_1))$ $I_{LR(t)} = I_{CR(t)}$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O	Discharge	$V_{LO} = -(V_O + V_{DO(fwd)})$

Inductor Charging State: t_2 - t_3

To facilitate zero voltage switching, switch Q_1 is activated once the voltage V_{DS} across Q_1 and resonant capacitor V_{CR} has reached zero, occurring at time t_2. During this inductor charging interval t_{23}, resonant inductor current I_{LR} is linearly returned from its negative peak of minus I_O to its positive level of plus I_O.

The output catch diode D_O conducts during the t_{23} interval. It continues to freewheel the full output current I_O, clamping one end of the resonant inductor to ground through D_O. There is a constant voltage, V_{IN} - V_{DO}, across the resonant inductor. As a result, I_{LR} rises linearly, I_{DO} decreases linearly. Energy stored in output inductor L_O continues to be delivered to the load during this time period.

A noteworthy peculiarity during this time-span can be seen in the switch drain current waveform. At time t_2, when the switch is turned on, current is actually returning from the resonant tank to the input source, V_{IN}. This indicates the requirement for a reverse polarity diode across the switch to accommodate the bi-directional current. An interesting result is that the switch can be turned on at any time during the first half of the t_{23} interval without affecting normal operation. A separate time interval could be used to identify this region if desired.

$$\frac{dI_R}{dt} = \frac{V_{IN}}{L_R} \; ; \; dt = dI_R L_R / V_{IN}$$

$$\therefore \; t_{23} = \frac{L_R \Delta I_R}{V_{IN}}$$

$$\text{where } \Delta I_R = -I_O \text{ to } +I_O = 2I_O$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}} \quad \text{and varies with } V_{IN} \text{ and } V_O$$

Power Transfer State: t_3 - t_4

Once the resonant inductor current I_{LR} has reached I_O at time t_3, the zero voltage switched converter resembles a conventional square wave power processor. During the remainder of the conversion period, most of the pertinent waveforms approach DC conditions.

Table IV - INDUCTOR CHARGING: t_2 - t_3

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$I_{D(t)} = -I_O + ((V_{IN} + V_{DO})/L_R)t$
C_R		$V_{CR} = 0$
L_R	Charging	$V_{LR} = V_{IN} + V_{DO}$ $I_{LR(t)} = -I_O + (V_{LR}/L_R)(t\text{-}t2)$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O		$I_{LO} = I_O$; $V_{LO} = -(V_O + V_{DO})$

Assuming ideal components, with Q_1 closed, the input source supplies output current , and the output filter inductor voltage V_{LO} equals V_{IN} - V_O. The switch current and resonant inductor current are both equal to I_O, and their respective voltage drops are zero ($V_{DS} = V_{LR} = 0$). Catch diode voltage V_{DO} equals V_{IN}, and $I_{DO} = 0$.

In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the t_{34} interval. Variable frequency operation is actually the result of modulating the on-time as dictated by line and load conditions. Increasing the time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter. For example, if the output voltage were to drop in response to an increased load, the conversion frequency would decrease in order to raise the effective ON period. Conversely, at light loads where little energy is drawn from the output capacitor, the control circuit would adjust to minimize the t_{34} duration by increasing the conversion frequency. In summary, the conversion frequency is inversely proportional to the power delivered to the load.

$$V_O = \frac{V_{IN} t_{34}}{t_{01} + t_{12} + t_{23} + t_{34}} = \frac{V_{IN} t_{34}}{t_{03} + t_{34}}$$

$$t_{34} = \frac{V_O t_{03}}{V_{IN} - V_O}$$

9

Table V - POWER TRANSFER: t_3 - t_4

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=I_O R_{DS(ON)}$; $I_D=I_O$
C_R		$V_{CR}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
D_O	OFF	$V_{DO}=V_{IN}$
L_O	Charging	$V_{LO}=V_{IN}-V_O$; $I_{LO}=I_O$

V_{IN} = 18 V
V_O = 5 V
I_O = 5 A

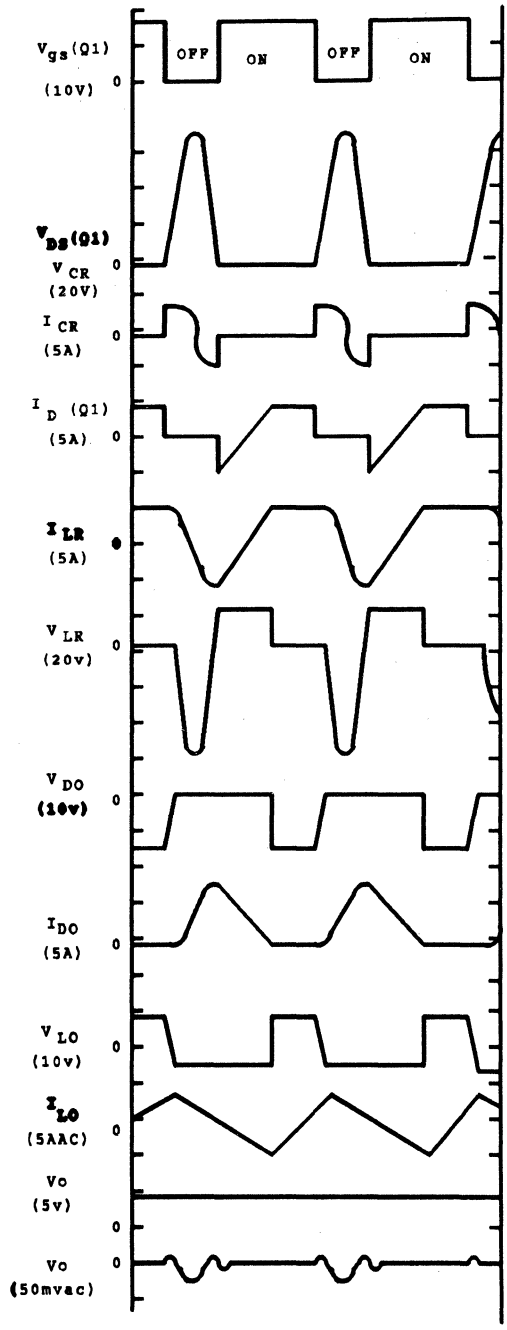

Fig. 9 -- ZVS Buck Regulator Waveforms

ZVS Converter Limitations:

In a ZVS converter operating under ideal conditions, the on-time of the switch ($t_{23}+t_{34}$) approaches zero, and the converter will operate at maximum frequency and deliver zero output voltage. In a practical design , however, the switch on-time cannot go to zero for several reasons.

First of all, the resonant tank components are selected based on the maximum input voltage V_{INmax} and minimum output current I_{Omin} for the circuit to remain resonant over all operating conditions of line and load. If the circuit is to remain zero voltage switched, then the resonant tank current cannot be allowed to go to zero. It can, however, reach I_{Omin}.

There is a finite switch on-time associated with the inductor charging interval t_{23} where the resonant inductor current linearly increases from - I_O to + I_O. As the on-time in the power transfer interval t_{34} approaches zero, so will the converter output voltage. Therefore, the minimum on-time and the maximum conversion frequency can be calculated based upon the limitation of I_{Omin} and zero output voltage.

The limits of the four zero voltage switched time intervals will be analyzed when I_O goes to I_O minimum. Each solution will be retained in terms of the resonant tank frequency ω_R for generalization.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{O\min}}{V_{INmax}\omega_R}$$

$$\therefore t_{01\max} = \frac{C_R V_{INmax}}{I_{O\min}} = 1/\omega_R$$

$$t_{12\max} = \frac{3\pi}{2\omega_R} = \frac{1.5\pi}{\omega_R}$$

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax}}{I_{O\min}\omega_R}$$

$$\therefore t_{23} = \frac{2L_R I_{O\min}}{V_{INmax}} = \frac{2}{\omega_R}$$

$$t_{34\min} = 0$$

Both the minimum on-time and maximum off-time have been described in terms of the resonant tank frequency , ω_R. Taking this one step further will result in the maximum conversion frequency $f_{CONVmax}$, also as a function of the resonant tank frequency.

Minimum On-Time:

$$t_{23\min} = \frac{2}{\omega_R} = \frac{1}{\pi f_R} = \frac{0.318}{f_R}$$

Maximum Off-Time:

$$t_{01}+t_{12\min} = \frac{1+1.5\pi}{\omega_R} = \frac{0.909}{f_R}$$

The maximum conversion frequency corresponds to the minimum conversion period, $T_{CONVmin}$, which is the sum of the minimum on-time and maximum off-time:

$T_{CONVmin}$:

$$t_{01}+t_{12\min}+t_{23} = \frac{0.909+0.308}{f_R} = \frac{1.227}{f_R}$$

The maximum conversion frequency, $f_{CONVmax} = 1/T_{CONVmin}$, equals

$$F_{CONV\max} = \frac{1}{T_{CONV(\min)}} = \frac{f_R}{1.227}$$

The ratio of the maximum conversion frequency to that of the resonant tank frequency can be expressed as a topology coefficient, K_T. For this zero voltage switched Buck regulator and its derivatives, K_{Tmax} equals:

$$K_{T\max} = \frac{F_{CONVmax}}{f_R} = \frac{f_R/1.227}{f_R} = 0.815$$

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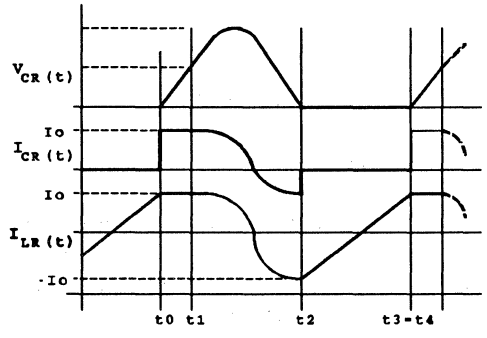

Fig. 10 -- Waveforms at $F_{CONV} = K_T \cdot f_R$

In a realistic application, the output voltage of the power supply is held in regulation at V_O which stipulates that the on-time in the power processing state, t_{34}, cannot go to zero as in the example above. The volt-second product requirements of the output must be satisfied during this period, just as in any square wave converter design. Analogous to minimum duty cycle, the minimum on-time for a given design will be a function of V_{IN}, V_O and the resonant tank frequency, ω_R.

Although small, a specific amount of energy is transferred from the input to the output during the capacitor charging interval t_{01}. The voltage into the output filter section linearly decreases from V_{IN} at time t_0 to zero at t_1, equal to an average value of $V_{IN}/2$. In addition, a constant current equal to the output current I_O was being supplied from the input source. The average energy transferred during this interval is defined as:

$$W_{IN} = \frac{1}{2} V_{IN} I_O t_{01} = \frac{V_{IN} I_O}{2} \frac{C_R V_{IN}}{I_O} = \frac{V_{IN}^2 C_R}{2}$$

The equation can be reorganized in terms of C_R and ω_R as:

$$W_{IN} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

This minimum energy can be equated to minimum output watts by dividing it by its conversion period where t_{34} equals zero. Topology coefficient K_T will be incorporated to define the ratio of the maximum conversion frequency (minimum conversion period) to that of the resonant tank frequency, ω_R.

$$W_{IN} = P_O T_{CONV} \quad , \quad Where \; T_{CONV} = \frac{7.71}{\omega_R}$$

$$W_{IN} = P_{O\min} \frac{7.71}{\omega_R} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

$$P_{O\min} = V_O I_{O\min} = \frac{V_{IN}^2 I_{O\min}}{2(7.71) V_{IN\max}}$$

This demonstrates that a zero power output is **unobtainable** in reality. The same is true for the ability to obtain zero output voltage. The equation can be rewritten as:

$$V_{O\min} = \frac{V_{IN}^2}{2(7.71) V_{IN\max}} = \frac{0.065\, V_{IN}^2}{V_{IN\max}}$$

Solving for the highest minimum output voltage, the worst case for occurs when I_O equals I_{Omin} and V_{IN} is at its maximum, V_{INmax}.

$$V_{O\min} = 0.065\, V_{IN\max} \; ; \quad \approx 6.5\%\; V_{IN\max}$$

$$P_{O\min} = 0.065\, V_{IN\max} I_{O\min} \; ; \quad \approx 6.5\%\; P_{IN\min}$$

Under normal circumstances the circuit will be operating far above this minimum requirement. In most applications, the amount of power transferred during the capacitor charging interval t_{01} can be neglected as it represents less than seven percent (7%) of the **minimum** input power. This corresponds to less than one percent of the total input power assuming a 10:1 load range.

ZVS Effective Duty Cycles:

A valid assumption is that a negligible amount of power is delivered to the load during the capacitor charging interval t_{01}. Also, no power is transferred during the resonant period from t_{12}. Although the switch is on during period t_{23}, it is only recharging the

resonant and output inductors to maintain the minimum output current, I_{Omin}. In summary, NO output power is derived from V_{IN} during interval t_{03}.

The power required to support V_O at its current of I_O is obtained from the input source during the power transfer period t_{34}. Therefore, an effective "duty cycle" can be used to describe the power transfer interval t_{34} to that of the entire switching period, t_{04}, or T_{CONV}.

ZVS - Effective Duty Cycle Calculations:

$$\text{"Duty Cycle"} = \frac{V_O}{V_{IN}} = \frac{t_{34}}{t_{04}}$$

$$\text{"Duty Cycle"} = \frac{t_{34}}{t_{01}+t_{12}+t_{23}+t_{34}}$$

And can be analyzed over line and load ranges using previous equations for each interval.

Accommodating Losses in the Design Equations:

Equations for zero voltage switching using ideal components and circuit parameters have been generated, primarily to understand each of the intervals in addition to computer modeling purposes. The next logical progression is to modify the equations to accommodate voltage drops across the components due to series impedance, like $R_{DS(on)}$, and the catch diode forward voltage drop. These two represent the most significant loss contributions in the buck regulator model. Later, the same equations will be adapted for the buck derived topologies which incorporate a transformer in the power stage.

The procedure to modify the equations is straightforward. Wherever V_{IN} appears in the equations while the switch is on it will be replaced by $V_{IN}-V_{DS(on)}$, the latter being a function of the load current I_O. The equations can be further adjusted to accept changes of $R_{DS(on)}$ and V_F, etc. with the device junction temperatures. Resonant component initial tolerances, and temperature variations likewise could optionally be evaluated.

A computer program to calculate the numerous time intervals and conversion frequencies as a function of line and load can simplify the design process, if not prove to be indispensable. Listed in the Appendix of this section is a BASIC language program which can be used to initiate the design procedure.

To summarize: When the switch is on, replace V_{IN} with $(V_{IN}-V_{DS(on)}) = (V_{IN}-I_O \cdot R_{DS(on)})$. When the free-wheeling diode is on, replace V_O with (V_O+V_F).

$$t_{01} = \frac{C_R(V_{IN}-I_O R_{DS(on)})}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R}\arcsin\left[\frac{V_{IN}-I_O R_{DS(on)}}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}-I_O R_{DS(on)}}$$

$$t_{34} = \frac{(V_O+V_F)(t_{01}+t_{12}+t_{23})}{(V_{IN}-I_O R_{DS(on)})-(V_O+V_F)}$$

$$Z_R = \frac{V_{INmax}-R_{DS(on)} I_{O\min}}{I_{O\min}}$$

Transformer Coupled Circuit Equations:

The general design equations for the Buck topology also apply for its derivates; namely the forward, half-bridge, full-bridge and push-pull converters. Listed below are the modifications and circuit specifics to apply the previous equations to transformer coupled circuits.

General Transformer Coupled Circuits. Maintaining the resonant tank components on the primary side of the transformer isolation boundary is probably the most common and simplest of configurations. The design procedure begins by transforming the output voltage and current to the primary side through the turns ratio, N. The prime (') designator will be used to signify the translated variables as seen by the primary side circuitry.

9

$$N = \frac{Primary\ Turns}{Secondary\ Turns}$$

$I_O' = I_O/N$; $V_O' = V_O \cdot N$; and $Z_O' = Z_O \cdot N^2$

To satisfy the condition for resonance, $I_R < I_O'$

$$I_R \le I_O' = I_O/N \ ; \ Z_R \le \frac{V_{INmax}}{I_{O\ min}} = \frac{V_{INmax} N}{I_O}$$

The resonant tank component equations now become:

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax} N}{I_{Omin} \omega_R}$$

Note: the calculated resonant inductance value does not include any series inductance, typical of the transformer leakage and wiring inductances.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{Omin}}{N V_{INmax} \omega_R}$$

Note: the calculated resonant capacitor value does not include any parallel capacitance, typical of a MOSFET output capacitance, C_{OSS}, in shunt. Multi-transistor variations of the buck topology should accommodate all switch capacitances in the analysis.

Timing Equations (including N):

$$t_{01} = \frac{C_R V_{IN} N}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin\left[\frac{V_{IN} N}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2 L_R I_O}{V_{IN} N}$$

$$t_{34} = \frac{N V_O (t_{01}+t_{12}+t_{23})}{V_{IN} - N V_O}$$

$$T_{CONV} = t_{01}+t_{12}+t_{23}+t_{34}$$

Determining Transformer Turns Ratio (N): The transformer turns ratio is derived from the equations used to define the power transfer interval t_{34} in addition to the maximum off-time, t_{03}. While this may first seem like an iterative process, it simplifies to the volt-second product relationship described. The general equations are listed below.

The turns ratio N is derived by substituting $N \cdot V_O$ for the output voltage V_O in the power transfer interval t_{34} equation. Solving for N results in the relationship:

$$N V_O / V_{IN} = t_{34} / (t_{01}+t_{12}+t_{23}+t_{34})$$

$$N = \frac{V_{IN\min} t_{34}}{V_O t_{04}}$$

The transformer magnetizing and leakage inductance is part of the resonant inductance. This requires adjustment of the resonant inductor value, or both the resonant tank impedance Z_R and frequency ω_R will be off-target. One

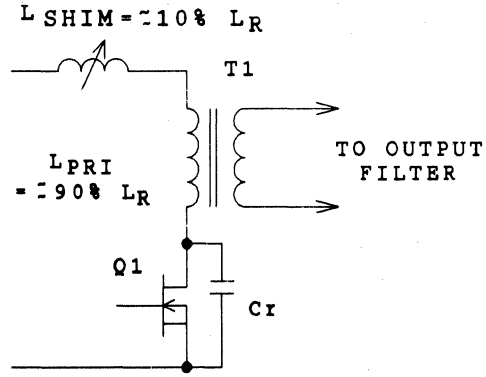

Fig. 11 -- Transformer Inductance "Shim"

option is to design the transformer inductance to be exactly the required resonant inductance, thus eliminating one component. For precision applications, the transformer inductance should be made slightly smaller than required, and "shimmed" up with a small inductor.

Expanding ZVS to Other Topologies

ZVS Forward Converter - Single Ended: The single ended forward converter can easily be configured for zero voltage switching with the addition of a resonant capacitor across the switch. Like the buck regulator, there is a high voltage excursion in the off state due to resonance, the amplitude of which varies with line and load. The transformer can be designed so that its magnetizing and leakage inductance equals the required resonant inductance. This simplifies transformer reset and eliminates one component. A general circuit diagram is shown in Fig. 12 below. The associated waveforms for when L_{PRI} equals L_R are shown in Fig. 13.

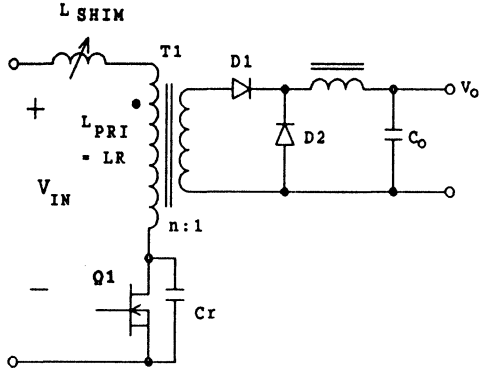

Fig. 12 -- ZVS Forward Converter

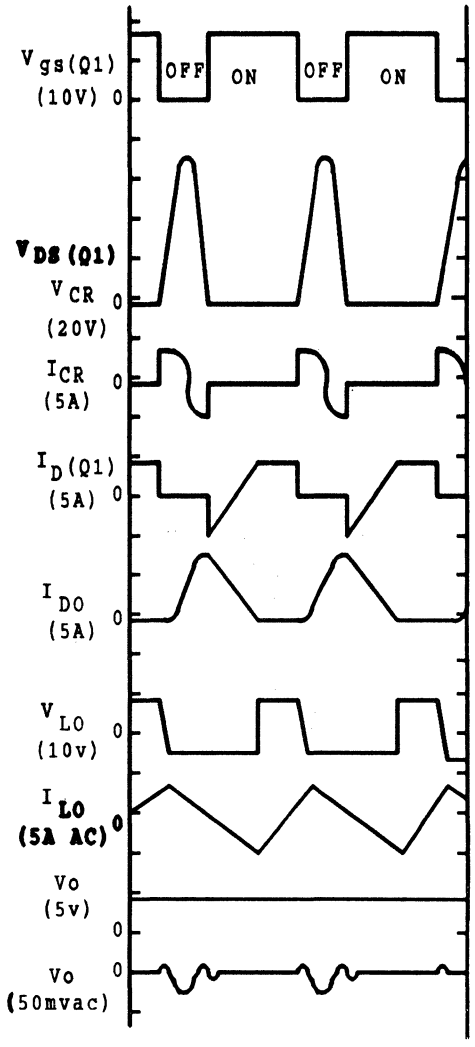

Fig. 13 -- Forward Converter Waveforms

ZVS Clamped Configurations -- Half and Full Bridge Topologies: Zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains similar, there is a difference in the resonant t_{12} interval.

While single switch converters have high off-state voltage, the bridge circuits clamp the switch peak voltages to the DC input rails, reducing the switch voltage stress. This alters the duration of the off segment of the resonant interval, since the opposite switch(es) must be activated long before the resonant cycle is completed. In fact, the opposite switch(es) should be turned on immediately after their voltage is clamped to the rails, where their drain to source voltage equals zero. If not, the resonant tank will continue to ring and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes.

Examples of this are demonstrated in Figs. 14 and 15. To guarantee true zero voltage switching, it is recommended that the necessary sense circuitry be incorporated.

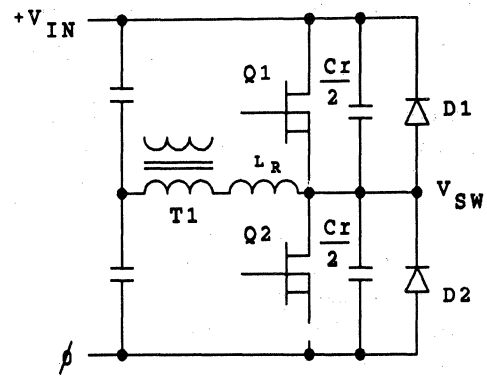

Fig. 14 -- Clamped ZVS Configuration

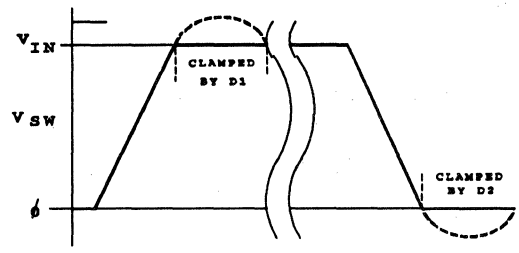

Fig. 15 -- Clamped ZVS Waveforms

ZVS Half Bridge: The same turns ratio, N, relationship applies to the half bridge topology when V_{IN} in the previous equations is considered to be one-half of the bulk rail-to-rail voltage. V_{IN} is the voltage across the transformer primary when either switch is on.

Refer to the circuit and waveforms of Figs. 14 and 15. C_R, the resonant capacitor becomes the parallel combination of the two resonant capacitors, the ones across each switch. Although the resonant inductor value is unaffected, all series leakage and wiring inductance must be taken into account.

The off state voltages of the switches will try to exceed the input bulk voltage during the resonant stages. Automatic clamping to the input bulk rails occurs by the MOSFET body diode, which can be externally shunted with a higher performance variety. Unlike the forward converter which requires a core reset equal to the applied volt second product, the bidirectional switching of the half (and full) bridge topology facilitate automatic core reset during consecutive switching cycles [11,12].

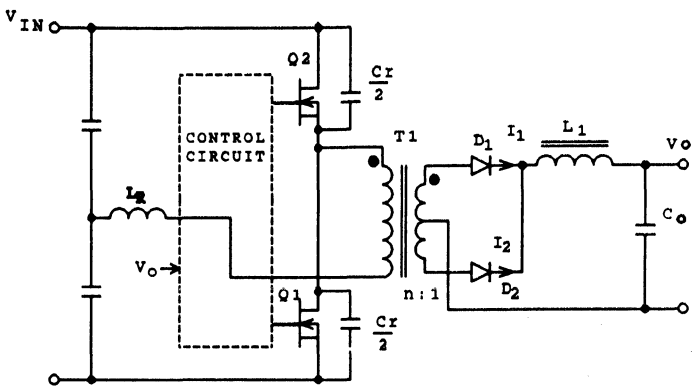

Fig. 16 -- ZVS Half Bridge Circuit

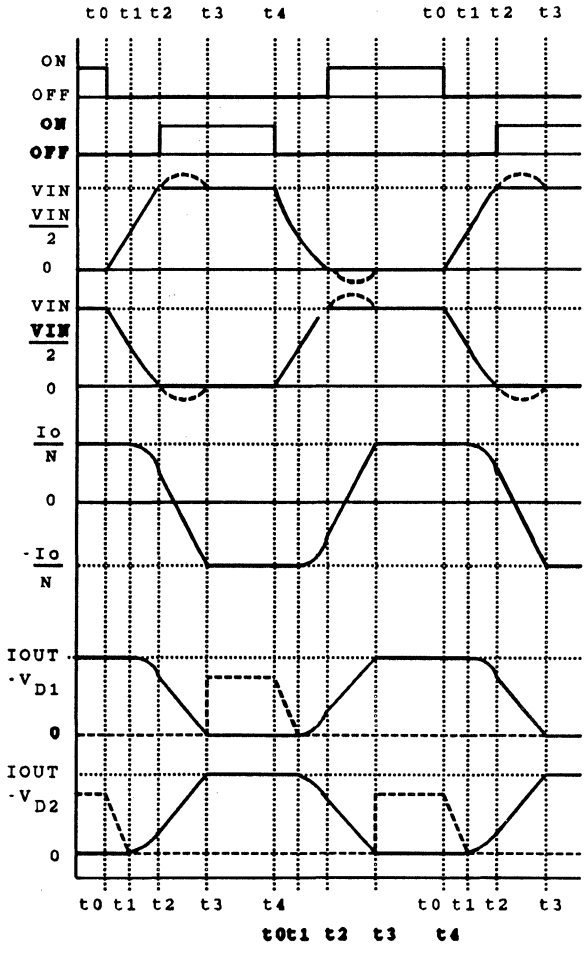

Fig. 17 -- ZVS Half Bridge Waveforms

ZVS Full Bridge: The equations represented for the forward topology apply equally well for one conversion cycle of the full bridge topology, including the transformer turns ratio. Since the resonant capacitors located at each switch are "in-circuit" at all times, the values should be adjusted accordingly. As with the half bridge converter, the resonant capacitors' voltage will exceed the bulk rails, and clamping via the FET body diodes or external diodes to the rails is common [13].

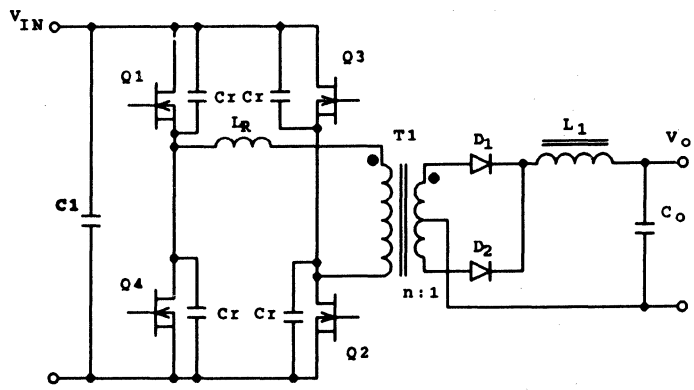

Fig. 18 -- ZVS Full Bridge Circuit

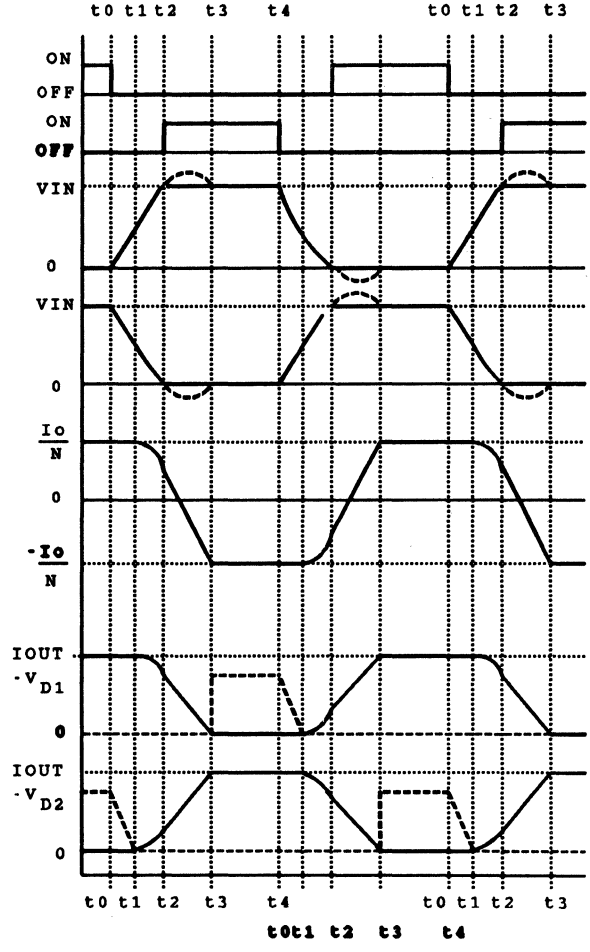

Fig. 19 -- ZVS Full Bridge Waveforms

ZVS Design Procedure

Buck Derived Topologies -- Continuous Output Current:

1. List all input/output specs and ranges.

   V_{IN} min & max ; V_O ; I_O min & max

2. Estimate the maximum switch voltages. For unclamped applications (buck and forward):

   $V_{DSmax} = V_{INmax}(1+(I_{Omax}/I_{Omin})$

   Note: Increase I_{Omin} if V_{DSmax} is too high if possible).

   For clamped applications (bridges): $V_{DSmax}=V_{INmax}$

3. Select a resonant tank frequency, ω_R (HINT: $\omega_R=2\pi f_R$).

4. Calculate the resonant tank impedance and component values.

5. Calculate each of the interval durations (t_{01} thru t_{34}) and their ranges as a function of all line and load combinations.
   (See Appendix ___ for a sample computer program written in BASIC)

   Additionally, summarize the results to establish the range of conversion frequencies, peak voltages and currents, etc.

6. **Analyze the results.** Determine if the frequency range is suitable for the application. If not, a recommendation is to limit the load range by raising I_{Omin} and start the design procedure again. Verify also that the design is feasible with existing technology and components.

7. Finalize the circuit specifics and details.

- ☐ Derive the transformer turns ratio. (non-buck applications)
- ☐ Design the output filter section based upon the lowest conversion frequency and output ripple current,I_O(ac).
- ☐ Select applicable components; diode, MOSFET etc.

8. Breadboard the circuit **carefully** using RF techniques wherever possible. Remember -- parasitic inductances and capacitances prefer to resonate upon stimulation, and quite often, **unfavorably.**

9. Debug and modify the circuit as required to accommodate component parasitics, layout concerns or packaging considerations.

Avoiding Parasitics

Ringing of the catch diode junction capacitance with circuit inductance (and package leads) will significantly degrade the circuit performance. Probably the most common solution to this everyday occurrance in square wave converters is to shunt the diode with an R-C snubber. Although somewhat dissipative, a compromise can be established between snubber losses and parasitic overshoot caused by the ringing. Unsnubbed examples of various applicable diodes are shown in Fig. 20 below.

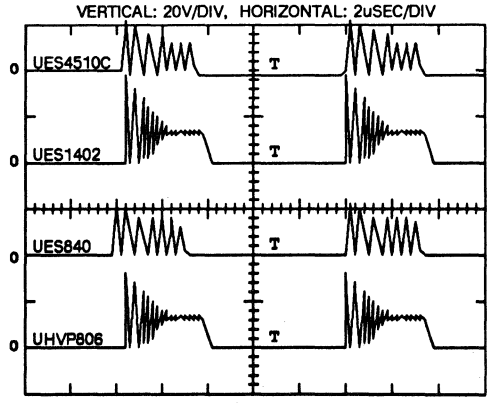

Fig. 20 -- Catch Diode Ringing

Multiresonant ZVS Conversion

Another technique to avoid the parasitic resonance involving the catch diode capacitance is to shunt it with a capacitor much larger than the junction capacitance. Labelled C_D, this element introduces favorable switching characteristics for both the switch and catch diode. The general circuit diagram and associated waveforms are showm below, but will not be explored further in this presentation [14,15].

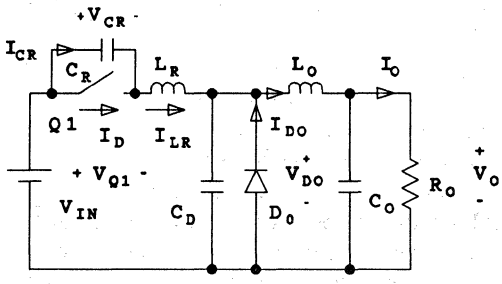

Fig. 21 -- Multiresonant ZVS Circuit

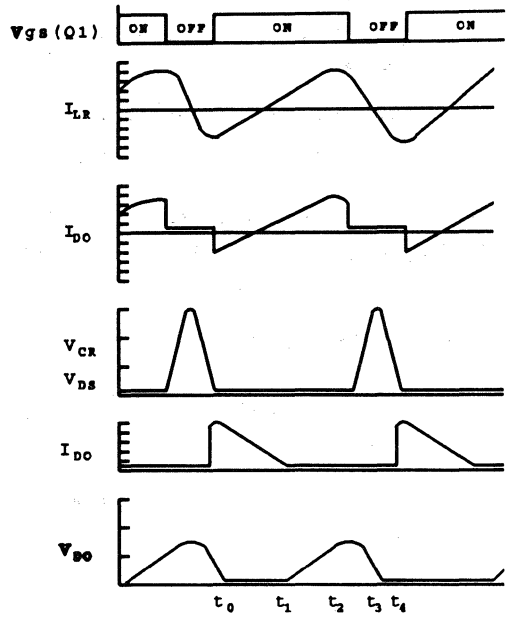

Fig. 22 -- Multiresonant Waveforms

Current Mode Controlled ZVS Conversion

Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise ON time of the power switch -- an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

Principles of operation. Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry. When the resonant capacitor voltage crosses zero, the UC3864 output goes high. This turns ON the power switch and recycles the UC3843A to initiate the next current mode controlled period. The UC3864 fault circuitry functions, but its error amplifier and VCO are not used.

ZVS Forward Converter -- Design Example

1. List circuit specifications:

V_{IN} = 18 to 26 V
V_O = 5.0 V ; I_O = 2.5 to 10 A

2. Estimate the maximum voltage across the switch:

$V_{DSmax} = V_{INmax}(1+(I_{Omax}/I_{Omin}))$
$= 26 \cdot (1+(10/2.5)) = 26 \cdot 5 = 130$ V

3. Select a resonant tank frequency, ω_R.

A resonant tank period frequency of 500KHz will be used. It was selected as a compromise between high frequency operation and low parasitic effects of the components and layout.

f_R = 500KHz ; $\omega_R = 3.14 \cdot 10^6$ radians/sec

4. Calculate the resonant tank impedance and component values.

Resonant tank impedance, $Z_R > V_{INmax}/I_{Omin}$

To accommodate the voltage drop across the MOSFET, calculate $V_{DS(on)min}$, which equals $R_{DS(on)}I_{Omin} = 0.8 \cdot 2.5 = 2$V

$Z_R = (V_{INmax}-V_{DSmin})/I_{Omin}$

$Z_R = (26-2)/2.5 = 10\ \Omega$

$C_R = 1/(Z_R\omega_R) = 1/(10 \cdot 3.14 \cdot 10^6) = 32$nF

$L_R = Z_R/\omega_R = 10/3.34 \cdot 10^6 = 3.18\mu$H

5. Calculate each of the interval durations (t_{01} thru t_{34}) and ranges as they vary with line and load changes.

The zero voltage switched buck converter "gain" in kiloHertz per volt of V_{IN} and kHz per amp of I_O can be evaluatated over the specified ranges. A summary of these follows:

Table VI - Interval Durations vs. Line & Load

	V_{IN}=18 I_O=2.5	V_{IN}=18 I_O=10	V_{IN}=26 I_O=2.5	V_{IN}=26 I_O=10
t_{10}	0.217	0.055	0.314	0.078
t_{12}	1.29	1.06	1.49	1.08
t_{23}	0.93	3.72	0.64	2.58
t_{34}	1.39	6.68	0.78	1.78
T_{CONV}	3.83	11.51	3.23	5.52
f_{CONV}	261kHz	87kHz	310kHz	181kHz
Transistor Switch Durations:				
t_{ON}	2.32	10.4	1.42	4.36
t_{OFF}	1.51	1.11	1.80	1.16

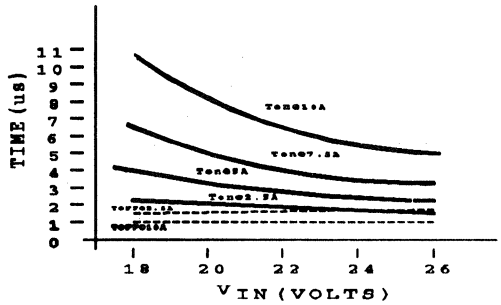

Fig. 23 - Switch Times vs. Line & Load

df_{CONV}/dV_{IN} vs I_O

I_O =	2.5A	5A	7.5A	10A	avg
df/dV =	6.1	11.2	11.9	11.7	10.2

Highest "gain" (11.9 kHz/V) occurs near full load.

df_{CONV}/dI_O vs V_{IN}

V_{IN} =	18	20	22	24	26	avg
df/dV =	23.3	22.1	20.5	18.8	17.3	20.4

Highest "gain" (23.3 kHz/A) occurs at V_{INmin}.

It may be necessary to use the highest gain values to design the control loop compensation for stability over all operating conditions. While this may not optimize the loop transient response for all operating loads, it will guarantee stability over the extremes of line and load.

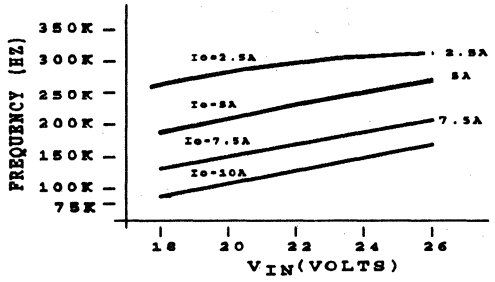

Fig. 24 - Conversion Freq. vs. Line & Load

6. Analyze the results.

The resonant component values, range of conversion frequencies, peak voltage and current ratings seem well within the practical limits of existing components and technology.

7. Finalize the circuit specifics and details based on the information obtained above.

A. Output Filter Section: Select L_O and C_O for operation at the lowest conversion frequency and designed ripple current.

B. Heatsink Requirements: An estimate of the worst case power dissipation of the power switch and output catch diode can be made over line and load ranges.

C. Control Circuit: The UC3861-64 series of controllers will be examined and programmed per the design requirements.

Programming the Control Circuit

One-shot: Accommodating Off-time Variations. The switch off-time varies with line and load by ≈ ± 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects results in an much wider excursion. For all practical purposes, a true fixed off-time technique will *not* work.

Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-

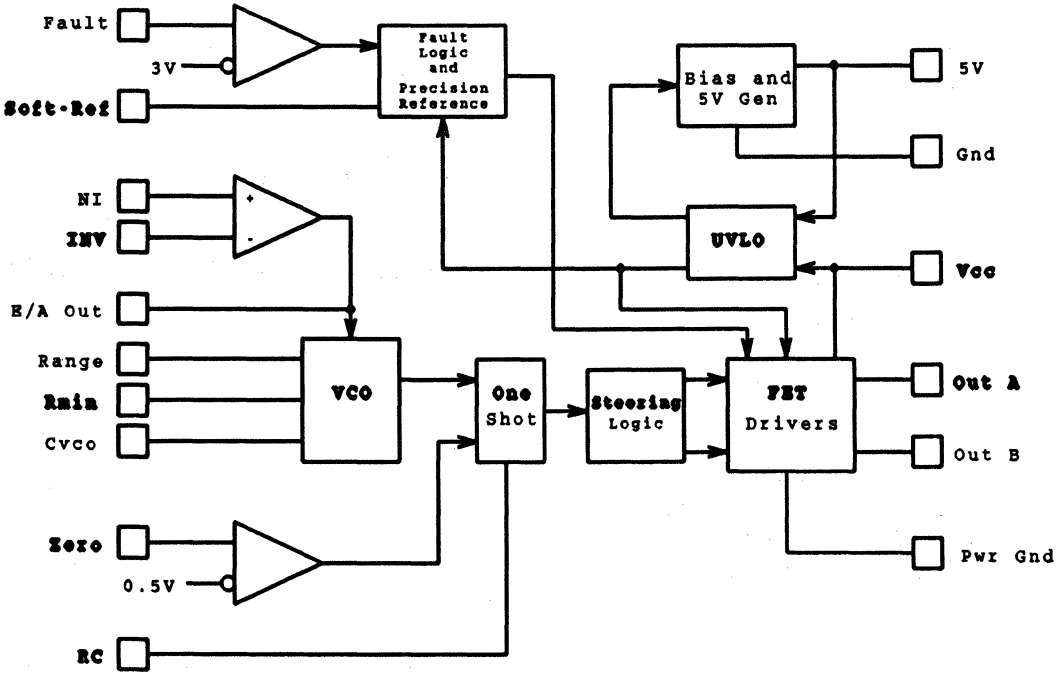

Fig. 25 -- The UC3861-64 ZVS Contollers -- Block Diagram

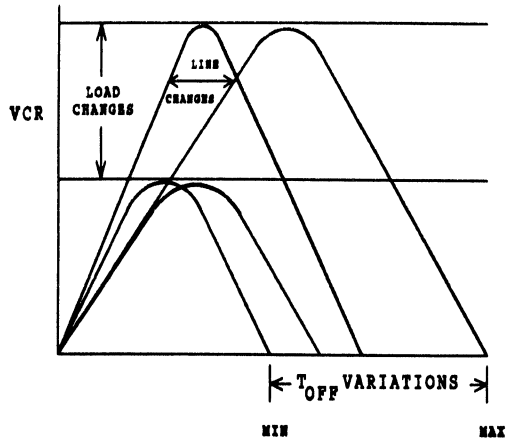

Fig. 26 -- C_R Volts & Off-time vs. Line & Load

time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

Referring to Fig. 26, in this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a 3:1 range capability and will be programmed for 2.2 uS (max), controllable down to 0.75 uS. Programming of the one-shot requires a single R-C time constant, and is straightforward using the design information and equations from the data sheet. Implementation of this feature is shown in the control circuit schematic.

Programming the VCO. The calculated range of conversion frequencies spans 87 to 310 kHz. These values will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences.

First, a minimum f_C of 75 kHz has been selected and programmed according to the following equation:

$$F_{VCOmin} = 3.6/(R_{min}C_{VCO})$$

The maximum f_C of 350 kHZ is programmed by:

$$F_{VCOmax} = 3.6/(R_{min} \parallel R_{range}) \cdot C_{VCO}$$

Numerous values of R_{min} and C_{VCO} will satisfy the equations. The procedure can be simplified by letting R_{min} equal 100K.

$$C_{VCO}\ (\mu F) = 0.036/f_{min}\ (kHz)$$

$$R_{RANGE}\ (k\Omega) = 100/(f_{CONVmax}/f_{CONVmin} - 1)$$

where R_{min}=100K, C_{VCO}=470pF, R_{RANGE} = 27K

The VCO gain in frequency per volt from the error amplifier output is approximated by:

$$dF/dV = 1/(R_{RANGE}C_{VCO}) = 78.2\ kHz/V$$

with an approximate 3.6 volt delta from the error amplifier.

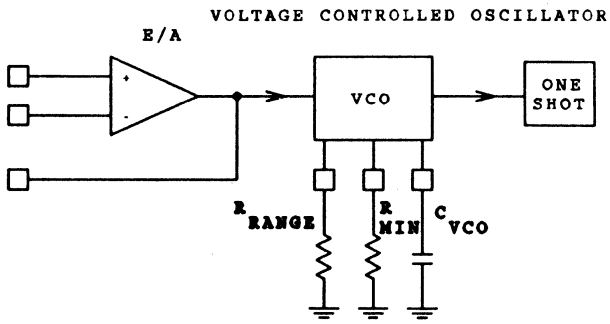

Fig. 27 -- E/A - VCO Block Diagram

Fault Protection - Soft Start & Restart Delay: One of the unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latch off following fault, etc) with a single resistor.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 ms and a restart delay of approximately 200 ms. The preprogrammed ratio of 19:1 (restart delay to soft start) will be utilized, however the relevant equations and relationships have also been provided for other applications. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short circuit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold.

Optional Programming of T_{SS} and T_{RD} :

Soft Start: $T_{SS} = C_{SR} \cdot 10K$

Restart Delay: $T_{RD} = C_{SR} \cdot 190K$

Timing Ratio: $T_{RD}:T_{SS} \approx 19:1$

Gate Drive: Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem pole outputs shows 30 ns rise and fall times into 1nF.

Loop Compensation -- General Information. The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unike the dual loop system of current mode control, the ZVS output filter section exhibits

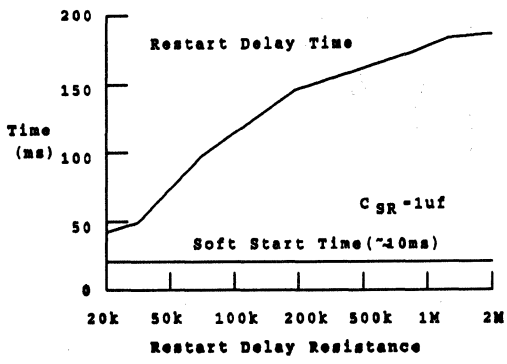

Fig. 28 -- Programming T_{SS} and T_{RD}

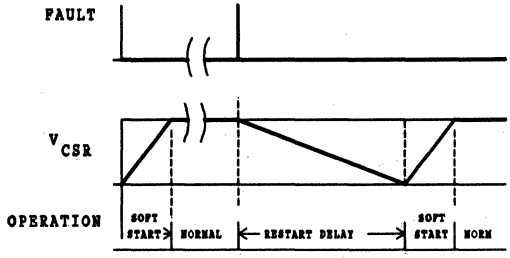

Fig. 29 -- Fault Operational Waveforms

a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for the highest low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filter's two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

A noteworthy alternative is the use of a two loop approach which is similar to current mode control, eliminating one of the output poles. One technique known as Multi-Loop Control for Quasi-Resonant Converters [18] has been

developed. Another, called Average Current Mode Control is also a suitable candidate.

$$\omega_{P1} = \frac{1}{R_{FP}C_F} \quad ; \quad \omega_{Z1} = \frac{1}{(R_{FP}\|R_{FZ})C_F}$$

$$\omega_{Z2} = \frac{1}{(R_{IP}+R_{IZ})C_I} \quad ; \quad \omega_{P2} = \frac{1}{R_{IP}C_I}$$

$$Gain\ at\ f_{Z1}, f_{Z2} = \frac{R_{FP}\|R_{FZ}}{R_{IP}+R_{IZ}}$$

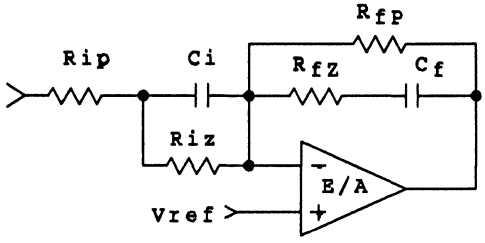

Fig. 30 -- Error Amplifier Compensation

Summary

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the MOSFET output capacitance can be significant at high switching frequencies, impairing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [14,15] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of

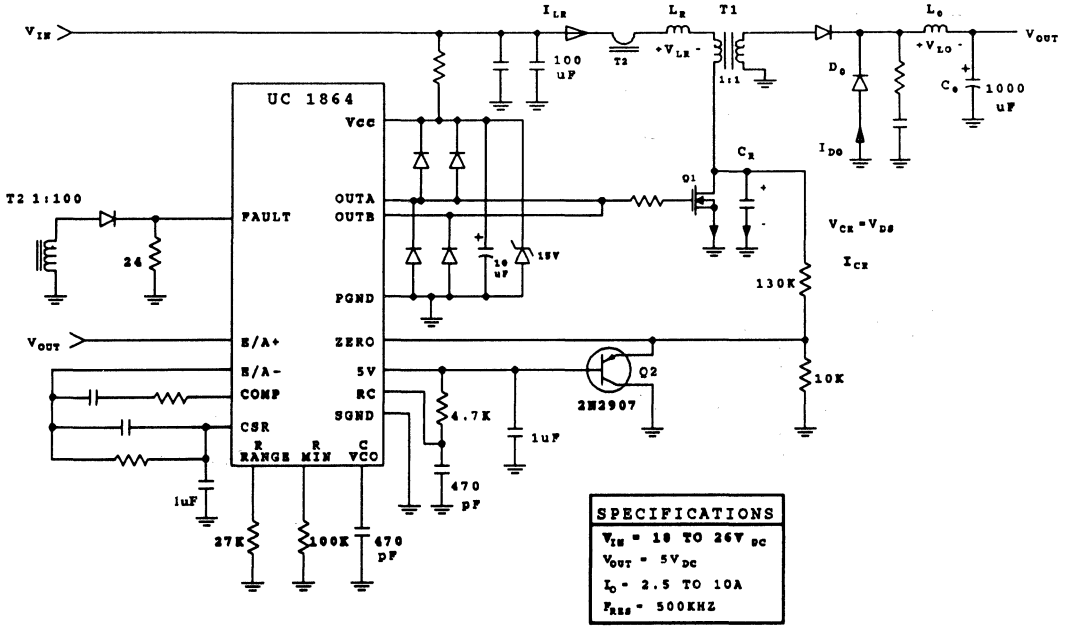

Fig. 31 -- Zero Voltage Switched Forward Converter

the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detrimental parasitic generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

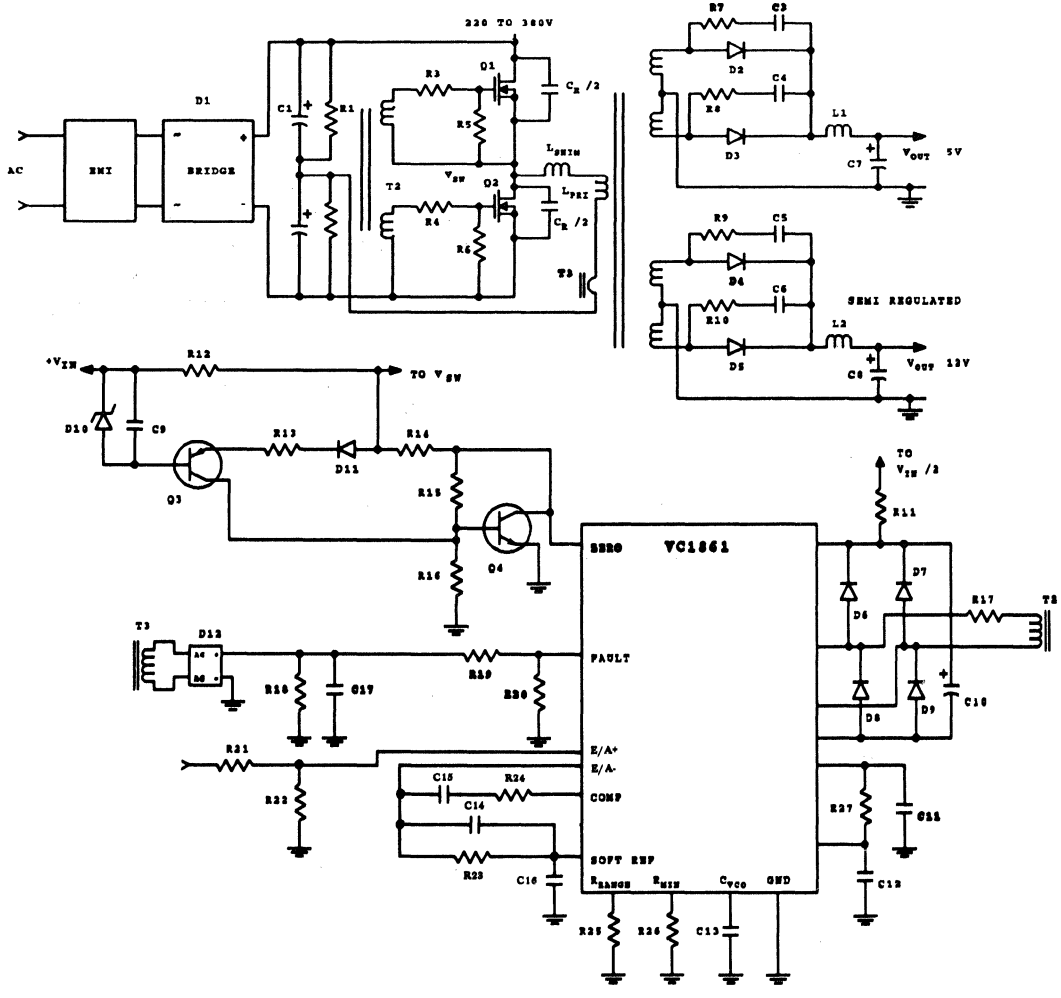

Fig. 32 -- Zero Voltage Switched Half-Bridge Converter

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Additional References:

- "High Frequency Resonant, Quasi-Resonant and Multi-Resonant Converters," *Virginia Power Electronics Center, (Phone # 703-961-4536), Edited by Dr. Fred C. Lee*
- "Recent Developments in Resonant Power Conversion," *Intertec Communication Press (Phone # 805-658-0933), Edited by K. Kit Sum*

```
10 ' Zero Voltage Switching Calculations and Equations
20 ' Using the Continuous Current Buck Topology
30 ' in a Typical DC/DC Converter Power Supply Application
40 '
50 PRINTER$ = "lpt1:": ' Printer at parallel port #1 **********
60 '
70 ' Summary of Variables and Abbreviations
80 '
90 ' Cr = Resonant Capacitor
100 ' Lr = Resonant Inductor
110 ' Zr = Resonant Tank Impedance
120 ' Fres = Resonant Tank Frequency (Hz)
130 '
140 ' VImin = Minimum DC Input Voltage
150 ' VImax = Maximum DC Input Voltage
160 ' Vdson = Mosfet On Voltage = Io*Rds
170 ' Rds = Mosfet On Resistance
180 ' Vdsmax = Peak MOSFET Off State Voltage
190 ' Vo = DC Output Voltage
200 ' Vdo = Output Diode Voltage Drop
210 ' Iomax = Maximum Output Current
220 ' Iomin = Minimum Output Current
230 '
240 ' Start with parameters for low voltage dc/dc buck regulator
250 '
260 ' ****Define 5 Vi and 5 Io data points ranging from min to max*****
270 ' (Suggestion: With broad ranges, use logarithmic spread)
280 DATA 18,20,22,24,27 : 'Vi data
290 DATA 2.5,4,6,8,10 : 'Io data
300 FRES = 500000!
310 VO = 5!
320 VDO = .8
330 RDS = .8
340 SAFT = .95
350 '
360 FOR J = 1 TO 5: READ VI(J): NEXT
370 FOR K = 1 TO 5: READ IO(K): NEXT
380 CLS
390 PRINT "For output to screen, enter 'S' or 's',"
400 INPUT "Otherwise output will be sent to printer : ", K$
410 IF K$ = "S" OR K$ = "s" THEN K$ = "scrn:" ELSE K$ = PRINTER$
420 OPEN K$ FOR OUTPUT AS #1: CLS
430 PRINT #1, "================================================"
440 PRINT #1, " Zero Voltage Switching Times (uSec) vs. Vi, Io"
450 PRINT #1, "================================================"
460 '
```

```
470 ' =========HERE GOES===========
480 '
490 VIMAX = VI(5): IOMIN = IO(1): IOMAX = IO(5)
500 ZR = (VIMAX - (RDS * IOMIN)) / (IOMIN * SAFT)
510 WR = 6.28 * FRES
520 CR = 1 / (ZR * WR)
530 LR = ZR / WR
540 '
550 FOR J = 1 TO 5: VI = VI(J)
560   PRINT #1, USING "                Input Voltage = ###.## V"; VI
570   FOR K = 1 TO 5: IO = IO(K)
580     RSIN = (VI / (IO * ZR)):   VDSON = RDS * IO
590 '
600     D(0, K) = IO * .000001:  ' Compensate for later mult. by 10^6
610     D(1, K) = (CR * VI) / IO: 'dt01
620     D(2, K) = (3.14 / WR) + (1 / WR) * ATN(RSIN / (1 - RSIN ^ 2)): 'dt12
630     D(3, K) = (2 * LR * IO) / VI: 'dt23
640     D(6, K) = D(1, K) + D(2, K) + D(3, K): ' dt03
650     D(4, K) = ((VO + VDO) * D(6, K)) / ((VI - VDSON) - (VO + VDO)): 'dt34
660     D(5, K) = D(1, K) + D(2, K) + D(3, K) + D(4, K): 'Tconv
670   NEXT K
680 '
690   PAR$(0) = "Io (A) ="
700   PAR$(1) = "dt01   ="
710   PAR$(2) = "dt12   ="
720   PAR$(3) = "dt23   ="
730   PAR$(4) = "dt34   ="
740   PAR$(5) = "Tconv  ="
750   PAR$(6) = "dt03   ="
760 '
770   FOR P = 0 TO 6
780     PRINT #1, PAR$(P);
790     FOR K = 1 TO 5
800       PRINT #1, USING " ####.###"; D(P, K) * 1000000!;
810     NEXT K: PRINT #1,
820   NEXT P
830 PRINT #1,
840 NEXT J
850 '
860 PRINT #1, "Additional Information:"
870 PRINT #1, "Zr(Ohms) ="; INT(1000! * ZR) / 1000
880 PRINT #1, "wR(KRads)="; INT(WR / 1000)
890 PRINT #1, "Cr(nF)   ="; INT((1000 * CR) / 10 ^ -9) / 1000
900 PRINT #1, "Lr(uH)   ="; INT((1000 * LR) / 10 ^ -6) / 1000
910 PRINT #1, "Vdsmax   ="; VIMAX * (1 + IOMAX / IOMIN)
920 END
```

Zero Voltage Switching Times (uSec) vs. Vi, Io

Input Voltage = 18.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.218	0.136	0.091	0.068	0.054
dt12 =	1.290	1.153	1.096	1.070	1.056
dt23 =	0.931	1.490	2.235	2.980	3.725
dt34 =	1.387	1.791	2.682	4.118	6.677
Tconv =	3.825	4.571	6.103	8.236	11.511
dt03 =	2.439	2.780	3.421	4.118	4.835

Input Voltage = 20.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.242	0.151	0.101	0.076	0.061
dt12 =	1.339	1.175	1.108	1.079	1.062
dt23 =	0.838	1.341	2.011	2.682	3.352
dt34 =	1.150	1.406	1.987	2.852	4.186
Tconv =	3.569	4.074	5.207	6.688	8.661
dt03 =	2.419	2.667	3.220	3.836	4.475

Input Voltage = 22.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.266	0.166	0.111	0.083	0.067
dt12 =	1.390	1.198	1.120	1.087	1.069
dt23 =	0.762	1.219	1.829	2.438	3.048
dt34 =	0.988	1.153	1.557	2.136	2.958
Tconv =	3.406	3.737	4.616	5.744	7.141
dt03 =	2.418	2.584	3.060	3.608	4.183

Input Voltage = 24.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.290	0.182	0.121	0.091	0.073
dt12 =	1.442	1.223	1.133	1.096	1.075
dt23 =	0.698	1.117	1.676	2.235	2.794
dt34 =	0.870	0.975	1.268	1.682	2.241
Tconv =	3.301	3.498	4.199	5.103	6.183
dt03 =	2.431	2.522	2.930	3.421	3.941

Input Voltage = 27.00 V

Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.327	0.204	0.136	0.102	0.082
dt12 =	0.516	1.264	1.153	1.109	1.085
dt23 =	0.621	0.993	1.490	1.987	2.483
dt34 =	0.442	0.793	0.983	1.253	1.604
Tconv =	1.906	3.254	3.763	4.451	5.254
dt03 =	1.464	2.461	2.780	3.198	3.650

Additional Information:
Zr(Ohms) = 10.526
wR(KRads)= 3140
Cr(nF) = 30.254
Lr(uH) = 3.352
Vdsmax = 135

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THE UCC3883 AND UCC3885 MEET ISDN REQUIREMENTS IN A SWITCH MODE POWER CONVERTER

Larry Wofford
Design Manager

ABSTRACT

The recommendations of Section 9 from CCITT I.430 include several requirements that make the design of ISDN compatible power supplies complicated. This paper covers a set innovative solutions to simplify the design task using a new pair of integrated circuits.
Specific areas addressed will include:

1) *Providing a highly regulated output voltage while maintaining galvanic isolation,*
2) *Soft Starting a power converter with an isolation barrier in the voltage feedback loop,*
3) *Synchronization of an isolated power converter,*
4) *Providing continuous inrush current limit capability,*
5) *Communicating restricted mode and other status information to a secondary-side CPU or controller,*
6) *Handling output overload conditions in a flyback topology, and*
7) *Power consumption budgeting for ISDN restricted mode operation.*

ISDN POWER SUPPLIES

The design of ISDN terminal equipment (TE) power supplies, in many ways, is identical to the common garden variety 100W computer power supply... at least the physics of the power transfer comes from the same text book. However, ISDN supplies are typically very demanding in the areas of size, cost, and efficiency. A supply required to be fully compatible with the recommendations of CCITT I.430 has significant additional complexity. Solutions to the specific technical hurdles will certainly be accepted as commonplace soon. For the time being, however, they represent some new challenges.

Galvanic isolation is often required. Transformer coupled switching stages nicely address the isolation issue for power transfer, but other entities must cross the isolation boundary besides power. If tight output regulation is not at issue, then a tertiary winding can be used to achieve some level of regulation. However, many times output regulation must be controlled from

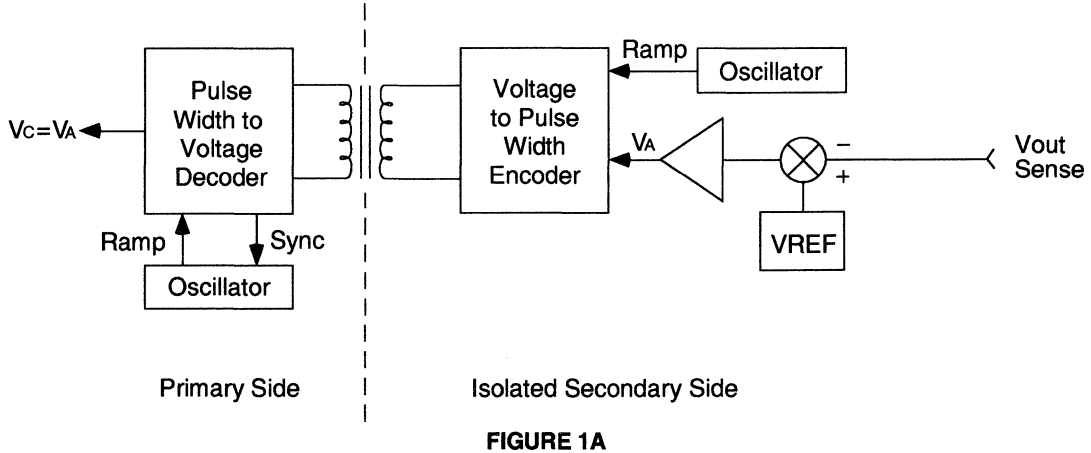

FIGURE 1A
ISOLATION FEEDBACK BRIDGE

the secondary side of the circuit. This means a feedback signal must also cross the isolation boundary.

Common to any isolated supply with feedback across the isolation boundary is the problem of starting the supply. Some sensible fashion of primary side "blind" soft start followed by a secondary side take over must be carefully planned.

ISDN supplies have other bits of information that need to cross the boundary. If voice band aliasing is a key concern, then a synchronizing signal must cross the boundary from a secondary side frequency reference to slave the repetition rate of the power switch. In addition, restricted mode information from the Network Termination (NT) is conveyed to the TE via line polarity. This information then, is on the primary side of the power supply, but needs to be known on the secondary side. Another useful item of information is the status of the line voltage which presents the same problem as the restricted mode status information.

Another feature required of ISDN supplies is inrush current limiting. Again, though this is not a new concept to power supplies, it is important for new reasons. High-power converters are fed from low impedance sources and inrush currents can be large enough to damage components if not properly managed. ISDN supplies, being fed from relatively high impedance lines, need to control inrush so as not to interfere with other TEs already connected to the network. Inrush events of concern occur when a TE is connected to a network or when the NT reverses polarity from normal mode to restricted mode or vice versa.

Of all the differences, perhaps one of the most dramatic is the requirement to process power over an extremely wide range. In restricted mode, when the TE can draw only 25mW, it is essential that both good output regulation be maintained while holding efficiency as high as possible. The discontinuous flyback is most often chosen as the topology to accomplish this feat.

SECONDARY SIDE REGULATION

The discontinuous flyback topology, chosen for it's efficiency at light load, naturally lends itself to power transfer across an isolation boundary. In order to achieve tight output regulation over all conditions, the voltage reference and error amplifier must reside on the secondary side of the circuit. The output of the error amplifier must then be transmitted to the primary side of the circuit in order to close the feedback loop.

The UCC2885 and UCC2883 are new control chips designed specifically for ISDN supplies. A pulse width encoded scheme (Figure 1) is used by the chip set to bridge the isolation barrier.

TRANS-ISOLATION COMMUNICATIONS

Key to achieving good regulation with galvanic isolation is the trans-isolation communications scheme implemented by the 2885 and 2883. The isolation boundary is bridged by a pulse transformer which carries four distinct information entities across the boundary.

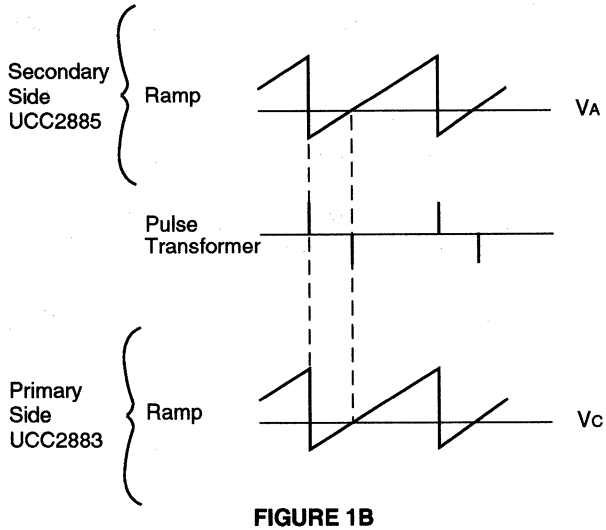

FIGURE 1B
ISOLATION FEEDBACK WAVEFORMS

The first bit of information is clock synchronization. At the beginning of a normal oscillator period on the secondary side, the 2885 will drive a very short duration positive polarity pulse through the transformer. This pulse is used to synchronize the oscillator on the 2883. The same timing components are used on both chips to achieve optimal tracking of the oscillator ramps. Since the 2883 frequency is slaved to the 2885, an external frequency reference introduced to the 2885 SYNC input will automatically lock the converter to a master frequency reference. The SYNC input is CMOS logic compatible.

It is important that both chips have similar oscillators, since they play a key role in transferring the error amplifier information across the boundary. The secondary side oscillator ramp is compared to the error amplifier output in classical pulse width modulation fashion. When the ramp crosses the amplifier output, a second pulse is applied to the transformer, this one of identical duration but opposite polarity. On the primary side,this pulse is used to sample and hold the 2883 oscillator ramp. This voltage is the decoded analog of the secondary side error amplifier output. Even if the oscillator ramps have a 20% mismatch, that represents only 2dB of gain error which has no impact on either loop compensation or output regulation accuracy.

A key benefit to this communications technique is the fact that the feedback signal is digitally encoded before it crosses the isolation boundary, resulting in excellent noise immunity in a naturally noisy environment. Another noteworthy item is that the short pulses driven into the transformer allow minimum power loss in the technique while requiring as little as 50uH of magnetizing inductance.

What if the 2885 error amplifier is temporarily driven fully low by a negative load step? Contrary to the description above, the 2885 will ship a single negative polarity pulse at the beginning of each oscillator cycle. The 2883 understands this as a request for zero duty cycle while maintaining oscillator synchronization. This confirms to the 2883 that the 2885 is still in control.

The other two bits of information flow from the primary to the secondary. The 2883 has two comparators to monitor restricted mode status and line voltage. When the 2883 receives the first pulse to mark the beginning of the oscillator period, if the NT is in normal mode, the 2883 will shunt a low value of resistance across the pulse transformer. This sudden impedance change is detected by the 2885 and it latches this data which will then appear at the RMODE pin of the 2885 indicating the system is not in restricted mode. If the NT changes polarity for restricted mode, then the shunting action will not take place and the 2885 will appropriately decode this fact and change the RMODE status output.

Likewise, if the 2883 detects low input line voltage then the same shunting action occurs during the second communications pulse. The 2885 interprets this action and drives the LOLINE status output accordingly.

Implemented this way, the Low Line information actually has priority over restricted mode information, since it is carried on the second pulse instead of the first. (Recall the first will not occur when the 2885 is requesting zero duty cycle.) The power loss caused by the shunting resistor is small, but even so, the convention chosen requires no shunting action when the system is in restricted mode and the line is sufficiently high. This is the set of circumstances where efficiency is most critical.

Note the magnetizing current in the pulse transformer is not going to become unwieldy. For normal operation, the widths of the first and second pulses track and so there is first order volt second balance. Between pulses the 2885 drives both terminals of the transformer low. Any mismatch in communication pulses will result in a circulating current between pulses. Two things limit this current. First is the selection of the magnetizing inductance. While the chips will function with 50uH, larger values will obviously reduce circulating current and lower the power loss. Secondly, the 2885 driver has finite impedance, and will tend towards a compensating offset voltage to keep the core balanced. For reasonable values of magnetizing inductance, this offset voltage will not materially affect the noise immunity of the communications scheme.

PRIMARY SIDE "BLIND" SOFT START

Orderly start up using the 2885 and 2883 is a relatively simple task. When line voltage is first applied (Figure 2), a depletion mode NMOS controlled by a linear preregulator amplifier in the 2883 supplies initial start up current. The control amplifier will regulate Vcc to 9.5V. After the power supply is operational, a boot strap winding will more efficiently supply power to the IC by raising Vcc above 9.5V. The control amplifier, driven out of regulation, will hold the gate of the NMOS at ground.
When the rising supply voltage (Figure 3) to the 2883 exceeds 4.4V, the chip will initiate a blind soft start. The capacitor on the CSTART pin is slowly charged by a

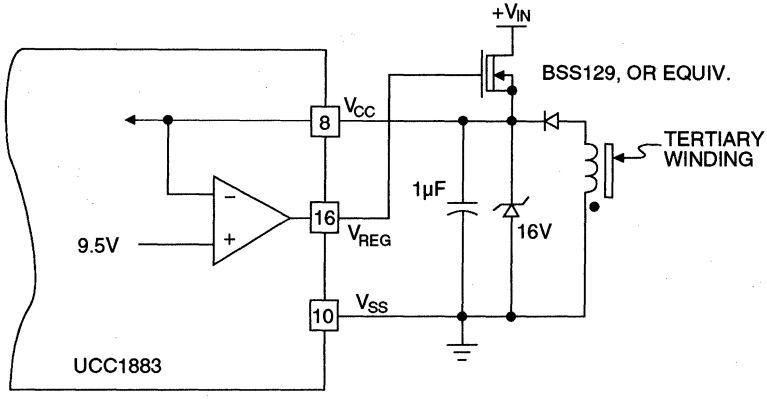

FIGURE 2
9.5V PRE-REGULATOR

25uA current. The rising voltage on CSTART is compared to the free running local oscillator to pulse width modulate the output switch.

As the duty cycle increases, progressively more and more energy is delivered to the secondary side and the output voltage begins to rise. The 2885 will remain dormant until it's Vcc exceeds 2.8V. This is the point at which it starts charging the capacitor on SOFT REF. The 2885 issues no feedback pulses, however, until the SOFT REF catches the sense voltage fed back to the inverting input of the error amplifier forcing the amplifier output high.

Upon receipt of the first feedback signals from the 2885, the 2883 immediately ceases it's blind soft start and begins obeying the feedback signal from the 2885. Orderly soft start is then completed under closed loop control as SOFT REF finishes charging to 2.0V.

TRANSIENT LINE CURRENT

I.430 strictly addresses the surge current a TE may

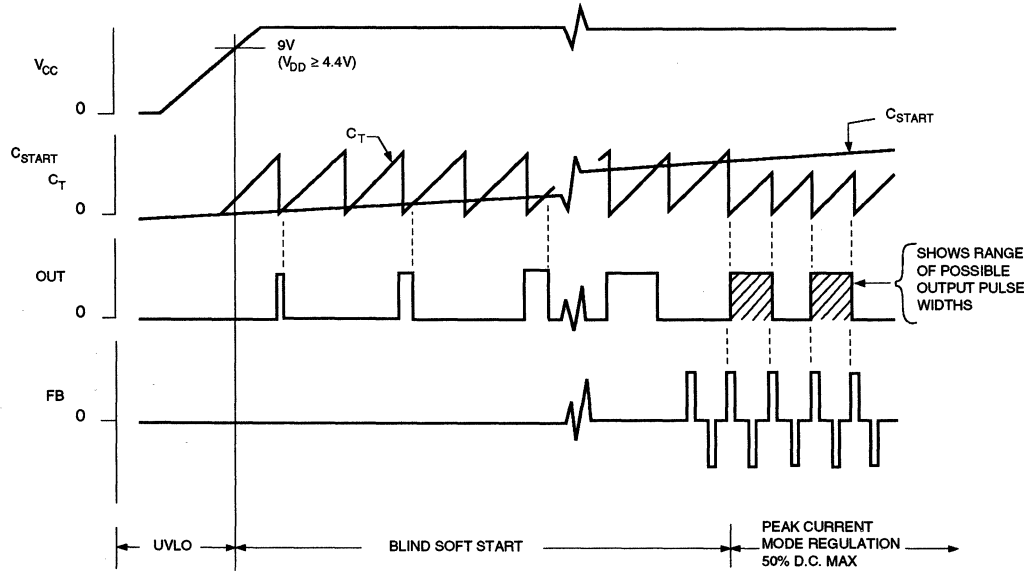

FIGURE 3
START UP WAVEFORMS

require of the NT. For practical purposes, it is sufficient to discuss a current mask composed of an undefined current for an initial period of 5us followed by a limited current of 55mA. There is more that must be considered to achieve full compliance, but solving this part of the exercise will make the remainder rather trivial.

The 2883 is used to control (Figure 4) a PMOS device in series with the return of the power feed. Current programmed by an external resistor RBIAS is scaled and forced into the input current limit resistor RP. TE return current is sensed by resistor RS. As long as the drop across RS is less than the drop on RP, the control amplifier will saturate in the negative direction causing the PMOS to behave as a low resistance switch. If return current attempts to increase without bound, the amplifier takes over and the current is held to a value programmed as:

ILIMIT = (RP/RS + 1) * 0.4V / RBIAS.

RP and RS should be chosen for a voltage drop large enough to render control amplifier offset inconsequential. Remember, however, that large values of RS represent power loss. This is most likely only a full load concern, and has little effect on restricted mode. For example, if the current limit value is 55mA and RS is chosen for a 150mV drop, then when running at 24V in restricted mode, the loss in RS is only 3uW. Efficiency at full load (assuming 1W) is impacted by a loss of 4.7mW (less than 0.5%).

The 10pF capacitor across RP is added to maintain good phase margin in the control loop. The diode shunting RS will limit any error voltage stored on the 10pF cap during the initial inrush transient.

Note that resistor RI shunting the PMOS is essential to start up. When power is first applied, the control amplifier output cannot go to a negative potential. RI will bleed charge onto the input bypass capacitor until there is enough voltage for the 2883 to operate properly.

RESTRICTED MODE POWER BUDGET

Blanc [Reference 2] has carefully analyzed the power consumption budget of a supply intended to be partially compatible with I.430. Essentially there is no change in that evaluation for the 2885 and 2883 and it need not be repeated here. When operating with 25mW of input power, a fully I.430 compatible supply built with the 2885 and 2883 can supply approximately 13mW of regulated power.

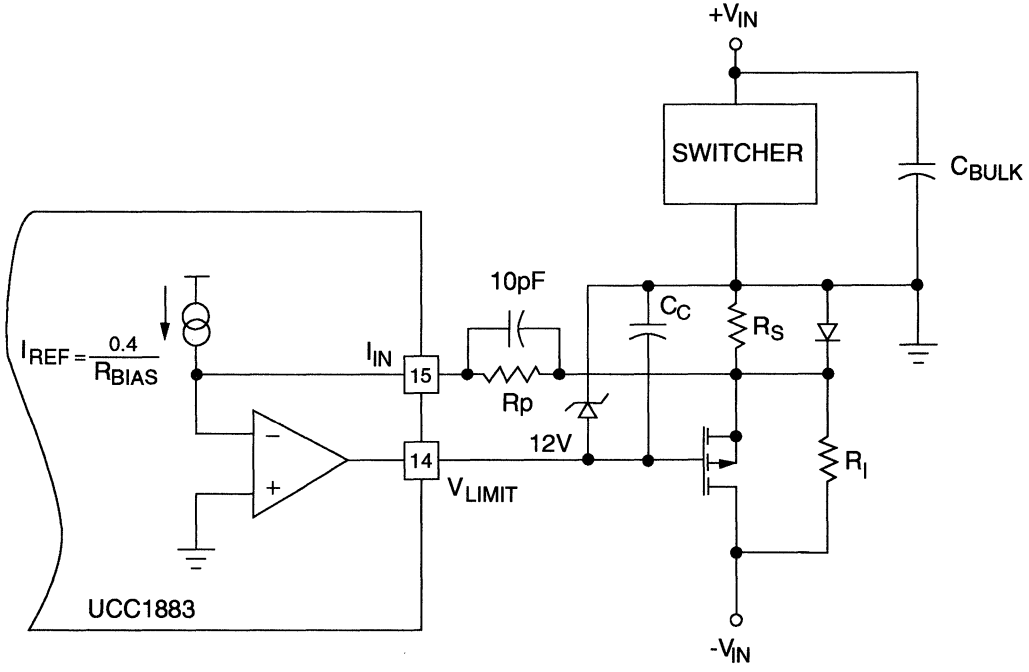

FIGURE 4
INPUT CURRENT LIMIT

I.430 recommendations also allow for supplies operating at higher input line voltage, and at power levels up to 8W. The bias current in the chip set is programmable and the power switch is external to allow for evolving I.430 specification.

OVERLOAD MANAGEMENT

Perhaps a drawback of the discontinuous flyback converter is the current stress the output diode must endure during short circuit. If the diode is chosen to survive this condition, then it is vastly over designed for nominal full load conditions. A means to alleviate this problem is to never allow the converter to operate for extended periods of time in a current limit condition.

The 2883 has a pin to time overload conditions (Figure 5). A current will charge or discharge a capacitor on the overload pin, COL. As long as each pulse is terminated by normal PWM action, the current discharges the pin. When ever the output is terminated due to Isense exceeding the peak current limit threshold, the COL pin is charged. If a number of consecutive cycles are terminated for this cause, then the COL voltage will exceed an internal 1.5V threshold causing the chip to shut down. A restart delay period will be observed before switching may again commence. This method will effectively limit the duty cycle of the stress on the output diode, allowing the diode to be specified for full load operation instead of over specified for short circuit operation.

On any cycle that the Isense pin exceeds the peak current limit threshold by 25%, the chip will immediately shut down and initiate restart delay.

SUMMARY — A SAMPLE ISDN 1W SUPPLY

Power supplies for ISDN applications can be designed without inordinate pain where the special requirements of I.430 are concerned (Figures 6, 7 and 8). The primary and secondary are galvanically isolated in a supply using the UCC2883/2885 chip set. Better than 3% output regulation can be achieved for input power ranging from 25mW to 1W. Efficiency at 25mW will exceed 50%. Inrush current can accurately be limited to 55mA both for line transients and for hot connection to the line. Initial inrush transient currents in excess of 55mA will be suppressed within 5us. Input line polarity and amplitude can be known on the secondary side via two CMOS logic compatible status bits.

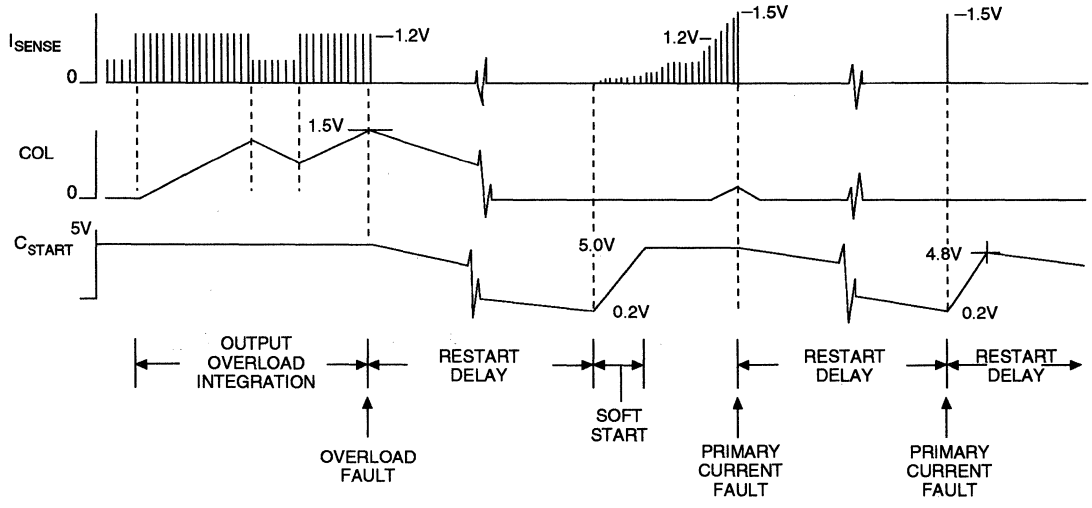

FIGURE 5
OVERLOAD WAVEFORMS

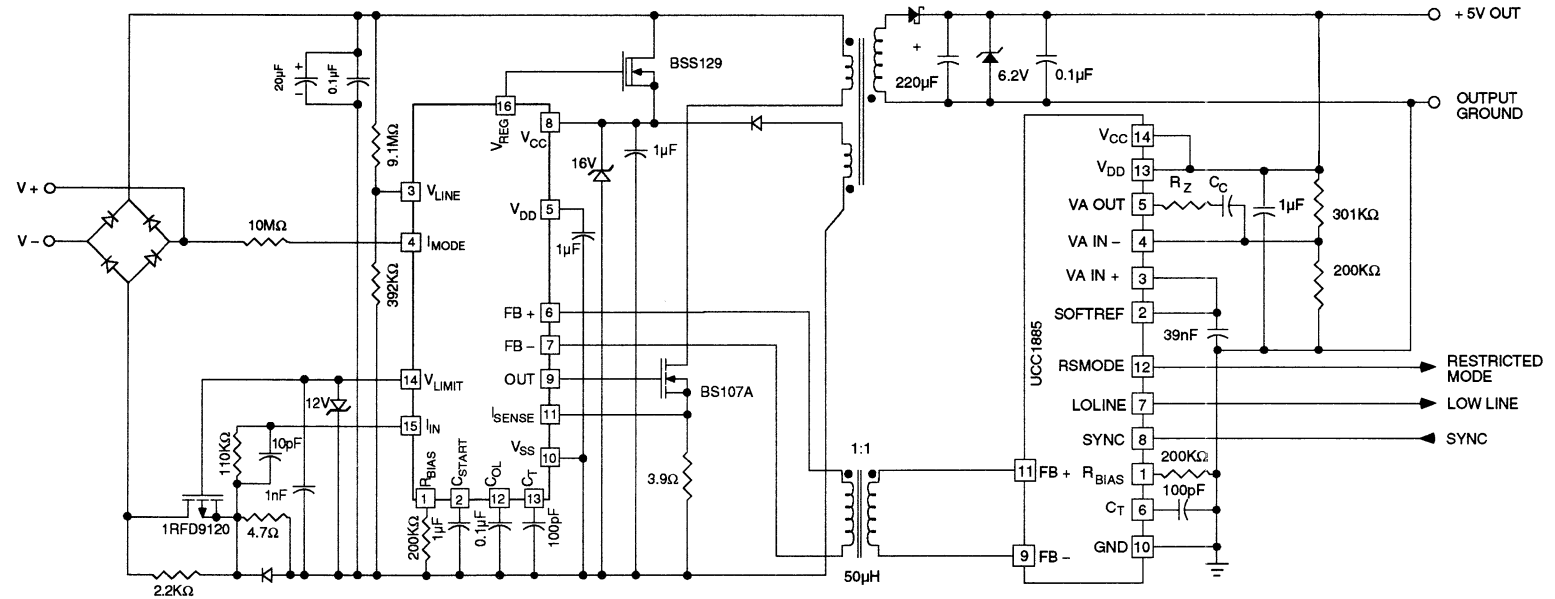

FIGURE 6
ISDN 1W SUPPLY

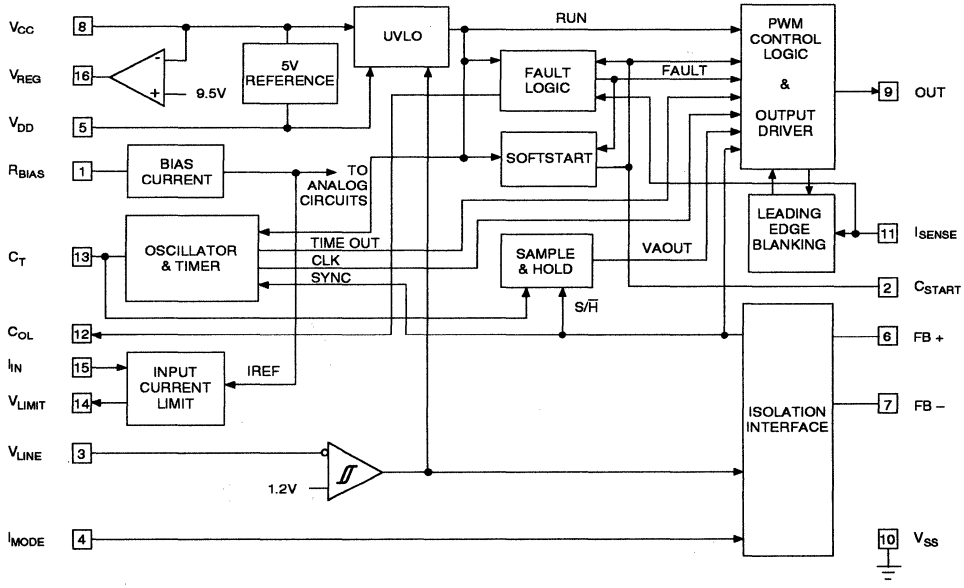

FIGURE 7
UCC2883 BLOCK DIAGRAM

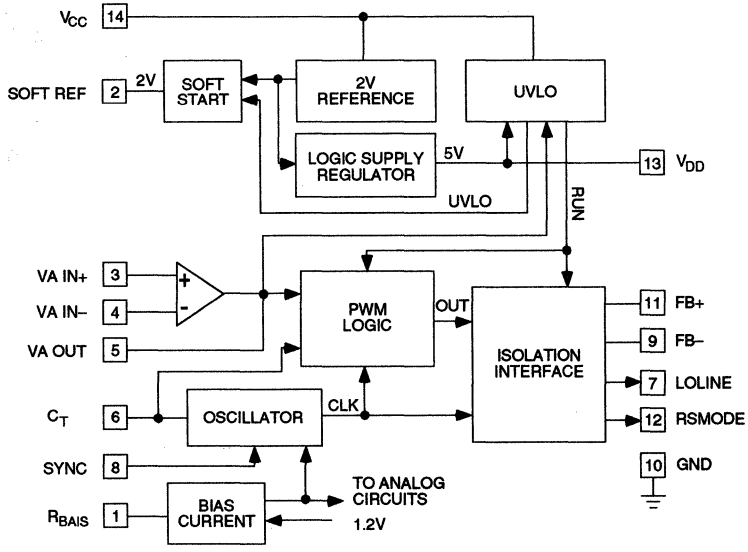

FIGURE 8
UCC2885 BLOCK DIAGRAM

ACKNOWLEDGEMENT

Grateful acknowledgement is extended to Ray Orr and Dave Cooper of Bell Northern Research for help understanding I.430 and it's ramifications.

REFERENCES

1) CCITT Recommendation I.430, Section 9

2) J. Blanc, "ISDN DC/DC conversion to the CCITT standards", Communications International, June 1989

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Average Current Mode Control of Switching Power Supplies

Lloyd Dixon

Abstract

Current mode control as usually implemented in switching power supplies actually senses and controls peak inductor current. This gives rise to many serious problems, including poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain cannot correct. Average current mode control eliminates these problems and may be used effectively to control currents other than inductor current, allowing a much broader range of topological application.

General Perspective

Current mode control is a two-loop system as shown in the simple example of Fig. 1. The switching power supply inductor is "hidden" within the inner current control loop. This simplifies the design of the outer voltage control loop and improves power supply performance in many ways, including better dynamics. The objective of this inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control. (Switch current --equal to inductor current during the "on" time--is often sensed.) If the inductor ripple current is small, peak inductor current control is nearly equivalent to average inductor current control.

In a conventional switching power supply employing a buck derived topology, the inductor is in the output. Current mode control then is actually output current control, resulting in many performance advantages. On the other hand, in a high power factor preregulator using the boost topology, the inductor is in the input. Current mode control then controls input current, allowing it to be easily conformed to the desired sinusoidal waveshape.

Peak Current Mode Control Problems

Poor noise immunity. The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop–see Fig. 1. The comparator turns the power switch off when the instantaneous current reaches the desired level. The current ramp is usually quite small compared to the programming level, especially when V_{IN} is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a subharmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

Slope compensation required. The peak current mode control method is inherently unstable at duty ratios exceeding 0.5,

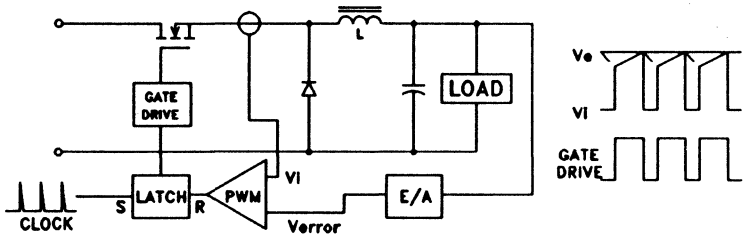

Fig. 1 - Peak Current Mode Control Circuit and Waveforms

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resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability. In a buck regulator the inductor current downslope equals V_O/L. With V_O constant, as it usually is, the compensating ramp is fixed and easy to calculate–but it does complicate the design. With a boost regulator in a high power factor application, the downslope of inductor current equals $(V_{IN}-V_O)/L$ and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

Peak to average current error. The peak to average current error inherent in the peak method of inductor current control is usually not a serious problem in conventional buck-derived power supplies. This is because inductor ripple current is usually much smaller than the average full load inductor current, and because the outer voltage control loop soon eliminates this error.

In high power factor boost preregulators the peak/avg error is very serious because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor current ramp makes the already poor noise immunity much worse.

Topology problems. Conventional peak current mode control actually controls inductor current. As normally used for output current control, it is most effective when applied to a buck regulator where the inductor is in the output. But for flyback or boost topologies the inductor is not in the output, the *wrong* current is controlled, and much of the advantage of current mode control is lost.

Likewise, the boost topology with its inductor at the input is well suited for input current control in a high power factor preregulator, but buck and flyback topologies are not well suited because the inductor is not in the input and the wrong current is controlled.

Average Current Mode Control

Peak current mode control operates by directly comparing the actual inductor current waveform to the current program level (set by the outer loop) at the two inputs of the PWM comparator. This current loop has low gain and so cannot correct for the deficiencies noted above.

Referring to Fig. 2, the technique of average current mode control overcomes these problems by introducing a high gain integrating current error amplifier (*CA*) into the current loop. A voltage across R_P (set by the outer loop) represents the desired current program level. The voltage across current sense resistor R_S represents actual inductor current. The difference, or current error, is amplified and compared to a large amplitude sawtooth (oscillator ramp) at the PWM comparator inputs.

The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the *CA*. Compared with peak current mode control, the current loop gain crossover frequency, f_C, can be made approximately the same, but the gain will be much greater at lower frequencies.

The result is:

1) Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor preregulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

2) Slope compensation is not required, but

there is a limit to loop gain at the switching frequency in order to achieve stability.

3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, *volts* away from the corresponding current error level at the input of the PWM comparator.

4) The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.

Designing the Optimum Control Loop

Gain Limitation at f_S: Switching power supply control circuits all exhibit subharmonic oscillation problems if the slopes of the waveforms applied to the two inputs of the PWM comparator are inappropriately related.

With peak current mode control, slope compensation prevents this instability.

Average current mode control has a very similar problem, but a better solution. The oscillator ramp effectively provides a great amount of slope compensation. One criterion applies in a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion puts an upper limit on the current amplifier gain at the switching frequency, indirectly establishing the maximum current loop gain crossover frequency, f_C. It is the first thing that needs to be considered in optimizing the average current mode control loop.

In the following examples, we assume that the power circuit design has been completed, and only the *CA* compensation remains to be worked out.

Example 1: Buck Regulator Output Current. The simple buck regulator shown in Fig. 2 has the following operating parameters:

Switching Frequency, f_S = 100 kHz
Input Voltage, V_{IN} = 15 - 30V
Output Voltage, V_O = 12V
Output Current, I_O = 5A (6A O.L.)
Inductance, L = 60 μH
max. ΔI_O @ 30V (100 kHz) = 1.2A
Sense Resistance, R_S = 0.1Ω

C_{FP} is temporarily omitted. Zero $R_F C_{FZ}$ is well below the switching frequency. Near f_S, the amplifier gain is flat. The overall current loop has only one active pole (from the inductor).

The inductor current is sensed through R_S. (How this is accomplished will be discussed later.) The inductor current waveform with its sawtooth ripple component is amplified and inverted through the CA and applied to the comparator. The inductor current downslope (while the switch is off) becomes an upslope, as shown in Fig. 2. To avoid subharmonic oscillation, this off-time CA output slope must not exceed the oscillator ramp slope. In Fig. 2, the off-time CA output slope is much less than the oscillator ramp slope, indicating that the CA gain is less than optimum.

Calculating the slopes:

Inductor Current Downslope = Vo/L
Oscillator Ramp Slope = $Vs/Ts = Vs f_S$

Where V_S is the oscillator ramp p-p voltage, T_S and f_S are the switching period and frequency.

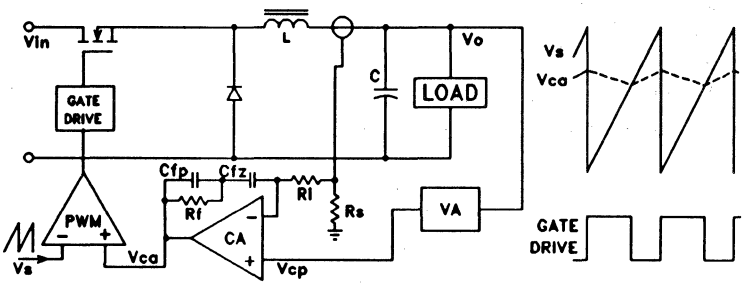

Fig. 2 - Average Current Mode Control Circuit and Waveforms

The inductor current downslope is translated into a voltage across current sense resistor R_S and multiplied by the *CA* gain, G_{CA}. This is set equal to the oscillator ramp slope to determine the *CA* gain allowed at f_S:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max \; G_{CA} = \frac{v_{CA}}{v_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (1)$$

Applying the values given in the example, and with V_S of 5Vpp, the maximum G_{CA} at the switching frequency is 25 (28dB). The current error amplifier gain at f_S is set to this optimum value by making the ratio $R_F/R_I = 25$.

The small-signal control-to-output gain of the buck regulator current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\frac{V_{IN}}{sL} = \frac{1590}{f} \quad (@30V) \qquad (2)$$

The overall open loop gain of the current loop is found by multiplying (1) and (2). The result is set equal to 1 to solve for the loop gain crossover frequency, f_C:

$$\frac{R_S}{V_S}\frac{V_{IN}}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S V_{IN}}{2\pi V_O} = \frac{f_S}{2\pi D} \qquad (3)$$

Setting the *CA* gain at the limit found in (1), the crossover frequency will never be less than one sixth of the switching frequency. (This is exactly the same result reported by Middlebrook [1] for peak current mode control with recommended slope compensation.) In this example, f_C is 20 kHz with V_{IN} at 15V (D=.8), and 40 kHz when V_{IN} at 30V (D=.4).

If the error amplifier had a flat gain characteristic, the phase margin at crossover would be 90°–much more than required–and the gain at lower frequencies wouldn't be much better than with peak current mode control. But zero $R_F C_{FZ}$ placed at 10 kHz, below the minimum crossover frequency, reduces the phase margin to 63°, and boosts the low frequency gain dramatically, with an integrator gain of 250K/f. It is this characteristic which causes the current loop to rapidly and accurately home in on the average current called for by the outer loop. Even though the comparator actually turns off the power switch when a *peak* inductor current is reached, this peak current level is adjusted by the current amplifier so that the average current is correct.

Fig. 3 shows the start-up waveforms of the voltages at the PWM comparator inputs and the inductor current with V_{IN} at 30V and full load. Note how the amplified and inverted inductor current downslope virtually coincides with the oscillator ramp, because the CA gain was set at the optimum level according to Equation (1). Note also that if the CA gain is increased further, not only will the off-time slope exceed the oscillator ramp slope, but the positive excursion may reach the CA compliance limit, clipping or clamping the waveform.

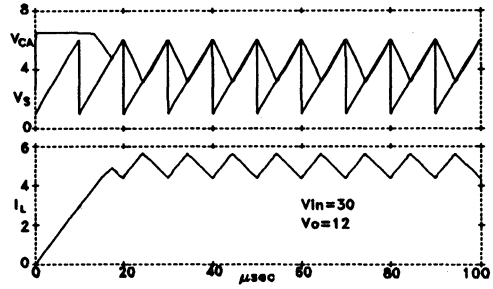

Fig. 3 - Buck Waveforms, Optimized Gain

Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at switching frequency f_S (100 kHz). This pole has one purpose–to eliminate noise spikes riding on the current waveform, the nemesis of peak current mode control. The sawtooth CA output waveform is also diminished, especially the higher order harmonics, and shifted in phase as shown in Fig. 4. The pole-zero pair (at 100 kHz and 10 kHz) reduces the phase margin at crossover to a very acceptable 45°–see Fig. 5.

The reduced amplitude and slopes of the CA waveform resulting from the 100 kHz pole might suggest that the *CA* gain could be in-

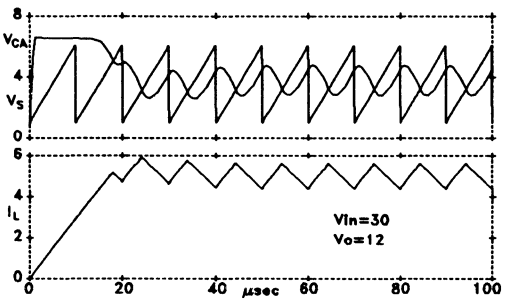

Fig. 4 - Buck with Additional Pole at f_S

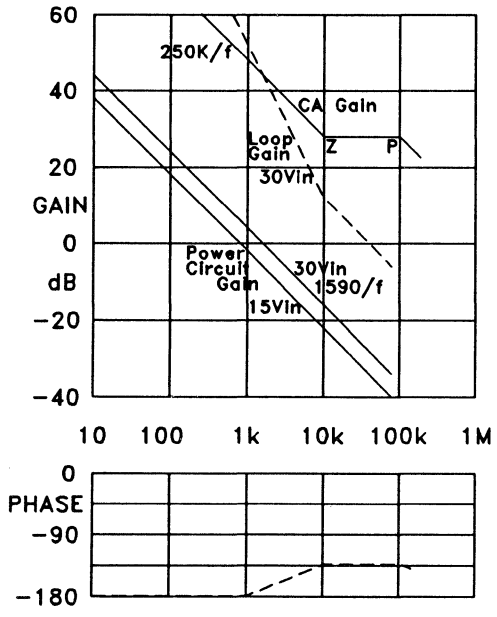

Fig. 5 - Buck Regulator Bode Plot

creased beyond the maximum value from Equation (1), but beware–Eq. (1) is valid only for a system with a single pole response at f_S, but with C_{FP} added there are now two active poles at f_S. Experimentally, increasing G_{CA} may incur subharmonic oscillation.

Discontinuous Operation. When the load current I_O becomes small, the inductor current becomes discontinuous. The current level at the continuous/discontinuous mode boundary is:

$$I_O = I_L = \frac{V_O(V_{IN}-V_O)}{V_{IN}2f_SL} \quad (4)$$

Worst case is at max V_{IN}, when ripple current is greatest. In this example, the mode boundary occurs at I_O ($=I_L$) of 0.2A when V_{IN} is 15V, and at 0.6A when V_{IN} is 30V.

In the discontinuous mode, below the mode boundary, changes in I_O require large duty cycle changes. In other words, the power circuit gain suddenly becomes very low. Also, the single pole characteristic of continuous mode operation with its 90° phase lag disappears, so the power circuit gain is flat–independent of frequency. The current loop becomes more stable, but much less responsive.

With peak current mode control in the discontinuous mode, peak/avg current error becomes unacceptably huge. But with average current mode control, the high gain of the current error amplifier easily provides the large duty cycle changes necessary to accommodate changes in load current, thereby maintaining good average current regulation.

Referring to Fig. 2, when the current loop is closed, the voltage across current sense resistor V_{RS} equals the current programming voltage V_{CP} (from the voltage error amplifier) at frequencies below f_S. The transconductance of the closed current loop is a part of the outer voltage control loop:

$$g = \frac{\hat{i}_L}{\hat{v}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{CP}} = \frac{1}{R_S} \quad (5)$$

The closed loop transconductance rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

Example 2: Boost Regulator Input Current. A 1 kW off-line preregulator (Fig 6) operates with the following parameters:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
Output Volts, V_O = 380Vdc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
ΔI_L, ΔI_{IN} @90V = 3.4A
R_S = 0.05Ω

The max. overload line current at min. V_{IN} corresponds to 1080W input. The max. peak overload 60Hz line current (17A) should–by design–correspond to a limit on the current programming signal, I_{CP}. The max peak 100kHz current through the switch and rectifier is 17A plus one-half ΔI_L: 17 + 3.4/2 = 18.7A

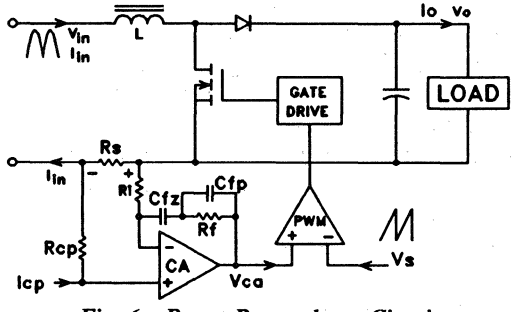

Fig. 6 - Boost Preregulator Circuit

The current downslope occurs when the power switch is off:

$$\textit{Inductor Current Downslope} = (V_O - V_{IN})/L$$
$$\textit{Worst case when } V_{IN} = 0: \quad = V_O/L$$
$$\textit{Oscillator Ramp Slope} = Vs/Ts = Vs f_s$$

Multiply the downslope by R_S and CA gain and set equal to the oscillator ramp slope, then solve for maximum CA gain:

$$(V_O/L) R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max \; G_{CA} = \frac{\hat{v}_{CA}}{\hat{v}_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (6)$$

Note the form of Equation (6) is identical to the buck regulator in (1). Using the values for this application, the maximum G_{CA} is 6.58, accomplished by making R_F/R_I = 6.58.

The small-signal control-to-input gain of the current loop power section (from v_{CA} at the CA output, to v_{RS}, the voltage across R_S) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_S}{V_S} \frac{V_O}{sL} = \frac{2420}{f} \qquad (7)$$

Note that (7) is nearly identical to (2) for the buck regulator, except the gain depends on V_O (which is constant), rather than V_{IN}.

The overall current loop gain is found by multiplying (6) and (7). The result is set equal to 1 to solve for the crossover frequency, f_C:

$$\frac{R_S}{V_S} \frac{V_O}{2\pi f_C L} \frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S}{2\pi} \qquad (8)$$

With the CA gain at the limit found in (6), the current loop f_C is *fixed* at $f_S/6$ (16.7 kHz).

As with the earlier example, with a flat gain error amplifier the phase margin at crossover is 90°–larger than necessary. So zero $R_F C_{FZ}$ is set at 1/2 of the minimum crossover frequency ($f_C/2 = f_S/12$ = 8.33 kHz), providing a low frequency boost with an integrator gain of 55K/f. Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at 6 times the zero frequency (50 kHz) to eliminate noise spikes. Together, the zero at 8.33 kHz and the pole at 50 kHz leave a phase margin at crossover of 40°. Startup waveforms are shown in Fig. 7, and the Bode plot in Fig. 8.

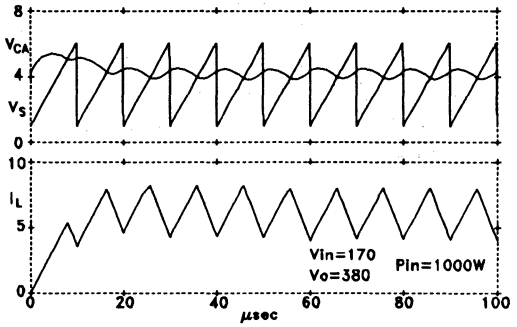

Fig. 7 - Boost Regulator Waveforms

Referring back to Fig. 6 – when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. In this case, programmed with a current source I_{CP}, the current gain of the closed current loop is:

$$G = \frac{i_L}{i_{CP}} = \frac{v_{RS}/R_S}{v_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (9)$$

The closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

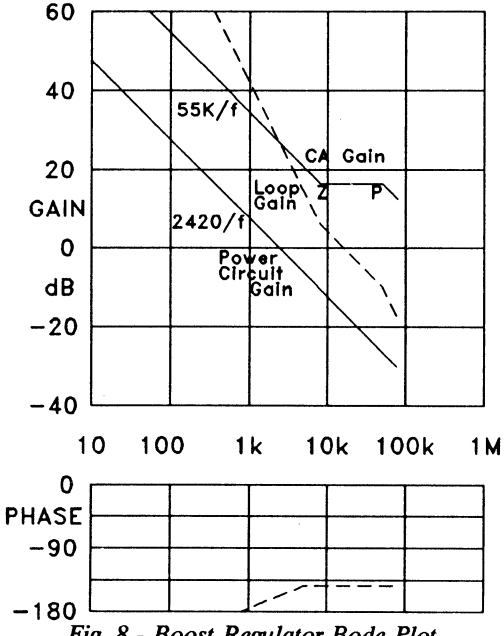

Fig. 8 - Boost Regulator Bode Plot

In a high power factor preregulator application, the current is programmed to follow the rectified line voltage. As the rectified sine wave voltage and current approache the cusp at zero, the inductor current becomes discontinuous. Discontinuous operation can occur over a substantial portion of the line cycle, especially when line current is low at high line voltage and/or low power input. With peak current mode control, discontinuous operation results in a large peak/average current error. A large inductance is required to make ripple current small and put the mode boundary at a low current level. However, average current mode control eliminates the peak/average error. A small inductance can and should be used to reduce cost, size and weight and improve current loop bandwidth.

Figure 9 shows a boost preregulator programmed to follow a 60 Hz (rectified) sine wave input. The lower waveforms show the programmed and actual line current waveforms. (The programmed waveform has been increased by 5% to make the two waveforms visible. The actual waveform leads the programmed waveform by a small amount and has less than 0.5% 3rd harmonic distortion! The upper waveforms show the duty cycles of the switch and diode throughout the line cycle. The inductor current is continuous when the current is high, and the switch and diode duty cycles add up to 1. But as the current approaches zero crossing, operation becomes discontinuous as shown by the appearance of "dead" time (when neither the switch, the diode, or the inductor are conducting).

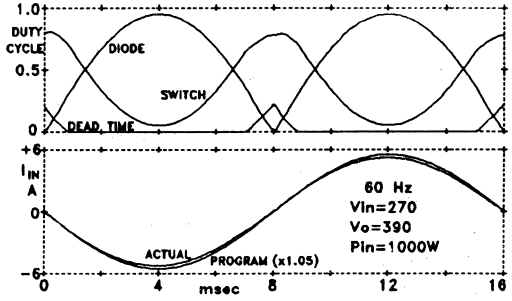

Fig. 9 - Boost 60Hz Sine Wave Input Current

Note that the switch duty cycle does not change as much when operation becomes discontinuous. With the boost (and flyback) topology in the discontinuous mode, average input current tends to follow input voltage at a constant duty cycle. Even though plenty of CA gain is available to change the duty cycle, little change is required for perfect tracking.

Figure 10 shows how the actual input current sine wave tracks the programming signal at 400 Hz. The distortion is worse -- 4.5% 3rd harmonic. This is for two reasons:

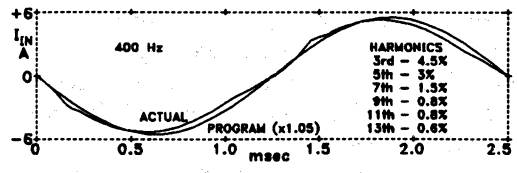

Fig. 10 - Boost 400Hz Sine Wave Input Current

1. The harmonic components of the rectified 400 Hz waveform are at higher frequencies and closer to the current loop crossover frequency where the loop gain is less, compared with the 50 or 60 Hz harmonics.
2. The inductor current has difficulty rising off zero because the input voltage is so very low at that point. So the inductor current lags coming off zero, then catches up and overshoots the programmed level. (This effect is much worse with peak current mode control because of the large inductor required.)

Controlling Average Switch Current

In the previous examples, average current mode control was applied to controlling inductor current (buck output current and boost input current). This is relatively easy because the inductor current is mostly DC with only a small amount of ripple to deal with. But if it is desired to use a buck or flyback topology to control input current in a high power factor application, then the chopped current waveform through the power switch must be averaged, a more difficult task.

Example 3: Flyback Regulator Input Current: A 1000 W off-line preregulator uses a flyback circuit in order to achieve a standard 300V output bus even though the input voltage ranges above and below 300V (Figs. 11,12).

The flyback converter could be designed to operate in the discontinuous inductor current mode in this application. The discontinuous flyback converter is not difficult to control (crudely) by fixing the duty cycle during each line half-cycle, but the peak currents through the power switch and rectifier are nearly twice as high as with continuous mode operation.

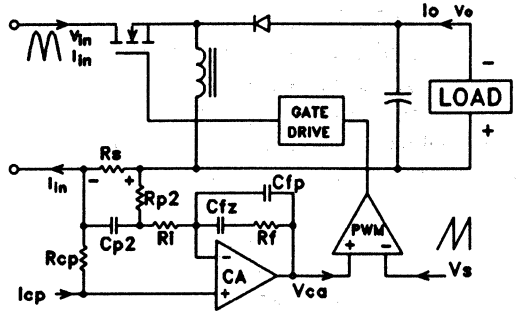

Fig. 11 - Flyback Preregulator Circuit

The high peak current lowers efficiency and requires devices with higher current ratings.

Continuous mode operation suffers the problem that the boundary is crossed into the discontinuous mode at light loads and high input voltage, unless a large filter inductor is used, which hurts the frequency response and the power factor as well as the pocketbook.

This dilemma disappears with average current mode control because it functions well in the discontinuous as well as the continuous mode, enabling the use of a small inductance value. In this example, the flyback converter operates in the continuous mode when it is important do so--at high current levels, to keep the maximum peak current to half that of a strictly discontinuous flyback converter. The operating parameters are:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
Output Volts, V_O = 300V dc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
ΔI_L @90V = 3.6A
R_S = 0.025Ω

The max. overload rms line current at min. V_{IN} equates to 1080W input (2160Wpk 60Hz). The max. overload peak 60 Hz line current (17A) should be made to correspond to a limit on the current programming input, I_{CP}. Unlike the boost converter, the flyback input current is chopped, so the peak 100kHz current through

the switch, the inductor, and the rectifier are much greater than the 60 Hz peak current–see Fig. 12. The worst case, at low line and max. overload input current is:

$$I_{PK(100kHz)} = \frac{I_{PK(60Hz)}}{D} = \frac{17}{.702} = 24.2A$$

Add to this one-half ΔI_L to obtain the absolute max. peak current through the switch, inductor, and rectifier: 24.2 + 3.6/2 = 26A.

Compared to the boost converter, the flyback topology requires higher current and higher voltage devices and generates a lot more input noise because of the chopped waveform. In its favor, the flyback converter can operate with any input/output voltage ratio, can provide current limiting, and input/output isolation.

As discussed in the previous example, the boost converter amplifier gain at f_S was limited only by the criteria that the inductor current downslope must not exceed the oscillator ramp slope. The power circuit control-to-input current gain had a simple −1 slope from zero to f_S, making it very easy to compensate.

But with the flyback converter, the chopped switch current waveform will be averaged. This results in a lower crossover frequency, f_C, and lower gain-bandwidth for two reasons:

1. The large amplitude chopped current waveform must be integrated by the CA. The upslope of the resulting triangular waveform at the CA output must not exceed the oscillator ramp slope. (The inductor current downslope is not relevant.)
2. There is a zero (conventional left half-plane) in the control-to-input current gain characteristic. This zero moves with output current level. Loop gain crossover cannot be much higher than the lowest zero frequency.

The small-signal control-to-input gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_S}{V_S}\left[I_L + \frac{V_O}{sL}\right] \qquad (10)$$

This is the characteristic of a "normal" zero–a -1 slope with 90° phase lag below f_Z and flat gain with no phase shift above f_Z. The zero frequency may be calculated:

$$f_Z = \frac{V_O}{2\pi L I_L} \qquad (11)$$

Note that the zero moves inversely with inductor current and inductance value. This zero has a big effect on loop compensation. To obtain the best loop response, it is important that f_{Zmin} be as high as possible, by making the inductance small. Fortunately, with average current mode control, there is no need to worry about crossing into discontinuous operation. The limit on making the inductance too small is when the inductor ripple current becomes too large, increasing peak switch and rectifier currents an undesirable amount.

Using the specific values of this example, the power circuit gain is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{I_L}{200} - j\frac{960}{f}$$

The minimum zero frequency is 8 kHz, which occurs at 24.2A, the max. overload *inductor* current at 90V low line. The gain above f_Z is 0.12 (-18.4dB). The power circuit gain is shown in the Bode plot of Fig. 13.

Turning now to the current error amplifier (Fig. 11), the chopped input (switch) current waveform shown in Fig. 12 flows through R_S. The average value of this waveform, chopped at 100 kHz, is compared to the current program level across R_{CP} and amplified. Assume for the moment that C_{P2} is zero and C_{FZ} is shorted. The CA gain in the vicinity of 100 kHz is determined by integrator $(R_I+R_{P2})C_{FP}$. Averaging is accomplished because the DC gain is high, but the 100 kHz rectangular waveform with its harmonics is amplified relatively little. The rectangular waveform is converted into a triangular wave as shown in Fig. 12.

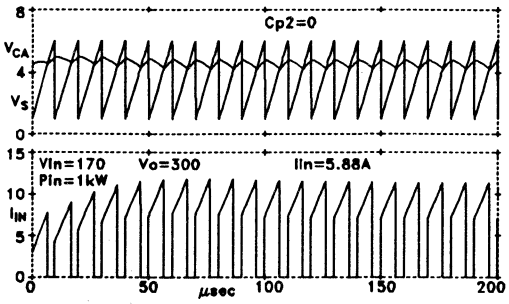

Fig. 12 - Flyback Regulator Waveforms

The optimum CA integrator gain at 100 kHz is the gain at which the maximum CA output upslope equals the oscillator ramp slope. This is the same principle used in the previous two examples, but in those cases the inductor (whose current was being controlled) did most of the averaging. The inductor did the integration to provide the triangular ripple current waveform and the CA gain was flat in the vicinity of f_S. But in this flyback preregulator example, the chopped *switch* current is being controlled so the averaging and the triangular waveshape are achieved by an integrating amplifier.

The upslope of the CA output occurs when the switch is off and the 100 kHz current waveform is at zero. The CA inputs are both at program voltage V_{CP}. V_{CPmax} equates to the max. overload peak 60Hz input current (17A) through R_S. Therefore, during the switch "off" time, the maximum current through $R = (R_I + R_{P2})$ is:

$$I_{RImax} = \frac{V_{CPmax}}{R} = \frac{I_{INpk} R_S}{R}$$

The upslope of the CA output is determined by the current through R_I charging C_{FP}:

$$\text{max } CA \text{ } Upslope = \frac{I_{RImax}}{C_{FP}} = \frac{I_{INpk} R_S}{C_{FP} R_I}$$

$$Oscillator \text{ } Ramp \text{ } Slope = V_S / T_S = V_S f_S$$

Equating the slopes and solving for C_{FP}:

$$\frac{I_{INpk} R_S}{C_{FP} R} = V_S f_S$$

$$C_{FP} = \frac{I_{INpk} R_S}{V_S f_S R} \qquad (12)$$

Using the values from this example, and assuming R = 10K (R_I=9K, R_{P2}=1K) :

$$C_{FP} = \frac{17 \times .025}{5 \times 0.1 \times 10^6 \times 10K} = 85\,pF$$

The CA integrator gain may now be calculated and entered in the Bode plot:

$$G_{CA} = \frac{1}{2\pi f R C_{FP}} = \frac{187{,}000}{f} \qquad (13)$$

The compensation circuit as designed so far (with C_{P2} zero and C_{FZ} open) has high loop gain and is very stable only when the inductor current is high, maintaining the power circuit zero near the position shown in Fig. 13, so that its gain is flat at f_C. At lower current levels, the power circuit zero slides down to the right and

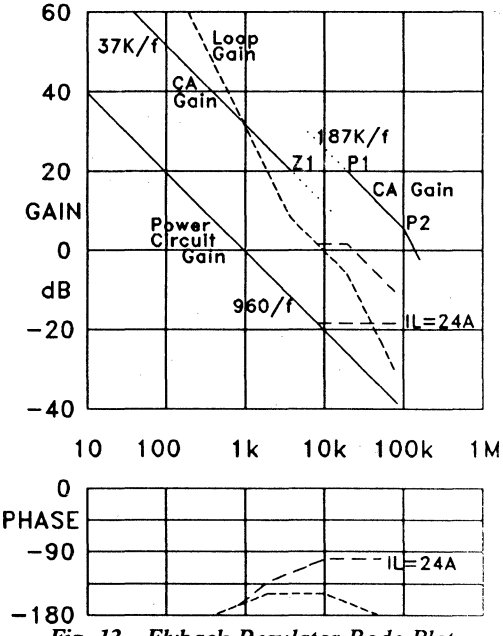

Fig. 13 - Flyback Regulator Bode Plot

the power circuit gain at f_C has a -1 slope. With the -1 slope of the CA gain, the overall current loop gain has a slope of -2 at crossover, and will ring excessively. It is necessary to add a pole-zero pair to the CA gain to reduce the slope to -1 in the vicinity of f_C. Offsetting the integrator gain by a factor of 5, as shown in the Bode plot, provides a phase bump which increases the actual phase margin to 42°, a slightly underdamped condition (the Bode *approximation* is 31°, as shown).

The offset factor of 5 is provided by $C_{FZ} = 4 \cdot C_{FP} = 340\text{pF}$. C_{FZ} and C_{FP} in parallel set the integrator gain at low frequencies to 37,000/f.

The location of the flat portion of the CA gain characteristic is determined by R_F. It is easiest to solve this graphically using the Bode plot. Ideally, Z1 and P1 should bracket the crossover frequency. *Simply slide the flat portion up and down between the integrator slopes until its gain is equal (but opposite in sign) to the power circuit gain at the same frequency as the center of the flat portion.* That frequency is the crossover frequency, f_C. In Fig 13, the CA gain in the flat portion is 10 (20dB). This is accomplished by:

$$R_F = 10R = 10\,(R_1 + R_{P2}) = 100K \quad (14)$$

The precise value of R_F (and f_C) is not at all critical. The phase bump is broad, and the loop response is really determined by the integrator gain below f_C (37,000/f).

Finally, an additional pole $R_{P2}C_{P2}$ is placed at 100kHz to filter out noise spikes. This pole frequency is too high to significantly affect phase margin at crossover.

Referring back to Fig. 11 – when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. Programmed with a current source I_{CP}, the current gain of the closed current loop is identical to Eq. 9:

$$G = \frac{\hat{i}_L}{\hat{i}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (15)$$

Just as in the previous examples, the closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S. The moving zero of the flyback power circuit is hidden within the inner current loop, and is invisible to the outer voltage control loop. In fact–regardless of the power circuit topology–with average current mode control, the external characteristics of the current loops are identical: flat gain, rolling off with a single pole characteristic above the open loop crossover frequency.

Example 4: Buck Regulator Input Current: The buck regulator is sometimes used in high power factor preregulator applications. It can only function when V_O is less than V_{IN}, so the output bus voltage must be low. Normally, a low output voltage should be avoided, because the bus filter capacitor becomes large and expensive, but in applications such as telephone or battery charging this is not a problem and/or there is no choice. With 120V line input and 48 volt output bus, the input current will drop to zero for a substantial portion of each line cycle, each time the instantaneous line voltage goes below 48V. Third harmonic distortion will be 7 - 8% at low line, but the power factor of 0.99 is good enough for most applications.

Although the flyback topology might be used in the same low voltage output application, the buck topology operates with lower inductor current and lower peak current through the switch and rectifier. Peak voltages on the switch and rectifier are also much lower. But the flyback topology can provide line isolation in the preregulator by using a flyback transformer instead of simple inductor.

The buck circuit can be almost the same as the flyback circuit of Fig. 11, interchanging the inductor and the rectifier (cathode up).

The control loop design procedure is the same as for the flyback in Example 3. The buck regulator has the same left half-plane zero. In fact, the power circuit control-to-input gain equation is identical to Eq. 10 for the flyback circuit.

Controlling Average Rectifier Current

Peak current mode control has been used with great success in conventional power supplies using buck-derived topologies. It works well because peak current mode control actually controls inductor current, and the inductor is located in the output of all buck topologies. When boost or flyback topologies are used, peak current mode control functions poorly, because the wrong current is controlled–the inductor current is not in the output. Although peak current mode control eliminates the inductor from the small-signal characteristic of the outer loop, the right half-plane zero present in boost and flyback outputs remains to plague outer loop compensation.

In boost or flyback circuits, the diode is in the output side, and ideally the diode current should be controlled, not inductor current. This is no problem for average current mode control. Its integrating current error amplifier can average the rectangular diode current waveform in the same way that it averages the switch current in the input of the buck or flyback preregulators discussed earlier. The right half-plane zero forces a lower current loop crossover frequency, but the RHP zero is "buried" within the current loop. The outer voltage control loop sees only a flat gain characteristic with a single pole roll-off at the crossover frequency–just the same as all the other topologies previously discussed. A flyback circuit using average current mode control is shown in Figure 14.

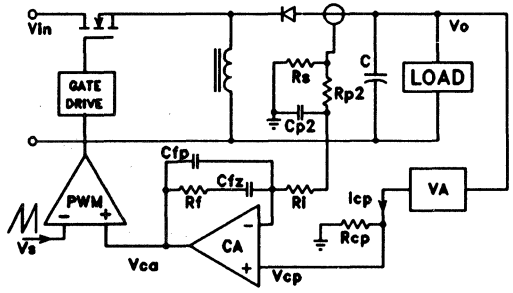

Fig. 14 - Flyback Output Current Control

The circuit is almost identical to the flyback preregulator of Fig. 11, except output current is sensed and controlled.

The small-signal control-to-output gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left(\frac{V_O}{sL} - I_L\right) \qquad (16)$$

The same equation applies to controlling the output current of a boost circuit. Note the similarity with Eq. 10 for flyback or buck input current control. In Eq. 16, low frequency gain depends on V_{IN} rather than V_O, but more importantly, the inductor current I_L has a minus sign, which represents 180° phase lag above the zero frequency. This is the characteristic of a right half-plane zero, and it makes the loop compensation much more difficult. It is usually necessary to cross over at a frequency one half to one fourth of the RHP zero frequency in order to cross over with adequate phase margin. This results in lower closed loop bandwidth for the current loop than the previous examples. However, once this is accomplished, the RHP zero does not appear in the outer loop.

It is very important to make the inductance small to achieve the highest possible RHP zero frequency. Fortunately, average current mode control allows the mode boundary to be crossed. This permits a much smaller inductance than with peak current mode control, resulting in a much higher RHP zero frequency and higher crossover frequency.

Current Sensing

One important advantage of having a high gain current error amplifier is that it permits a very small current sense resistor value resulting in low power dissipation. The CA can make up for the gain lost with the small resistor.

In many applications, however, using a current sense resistor in the direct path of the current to be measured is not practical. The tiny R_S value may be difficult to implement, and the power dissipation in a practical sense

resistor is too great. Often, the R_S circuit location is at a large potential difference from the control circuit. This is especially a concern when current must be sensed on the other side of the isolation boundary.

A current sense transformer (C.T.) can provide the necessary dielectric isolation and eliminate the need for an extreme low-value resistor. As shown in Fig. 15, this technique

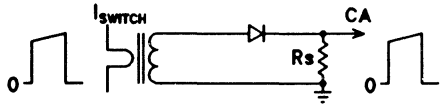

Fig. 15

works well for average current mode control when the current to be sensed and averaged is a pulse which returns to zero within each switching period–such as switch current (buck or flyback input current) or diode current (boost or flyback output current). Although "transformers can't couple DC", a C.T. does couple the entire instantaneous current waveform including its DC component if the core is reset to zero baseline each time the pulse goes to zero.

Total reset requires the same volt-seconds (of opposite sign) that were applied to "set" the core. At duty cycles approaching 1.0–which can occur temporarily with most topologies–the time available for reset may be only a tiny fraction of the switching period. Achieving total reset in a short time requires a large backswing of voltage across the C.T., so don't use low voltage diodes to couple the C.T. to R_S.

With a boost converter controlling input current in a high power factor preregulator application, a current sense resistor easily ties in directly with the control circuit, as shown in Fig. 6. Nevertheless, many designers would prefer to use a current transformer to minimize power loss and allow the use of a much higher R_S value. However, since the input current of a boost converter *is* the inductor current, the input current never goes to zero when operating in the continuous mode. Therefore, a C.T. can't be used to sense input current of a boost converter because the DC value is lost, and the C.T. cannot reset–it will saturate. The same problem occurs in a buck regulator circuit, where the C.T. can't directly sense average output (inductor) current.

The answer to this problem is to use *two* C.T.s–one sensing switch current, the other sensing diode current. By summing their outputs as shown in Fig. 16, the true inductor current is reconstituted. Each C.T. has plenty of time to reset.

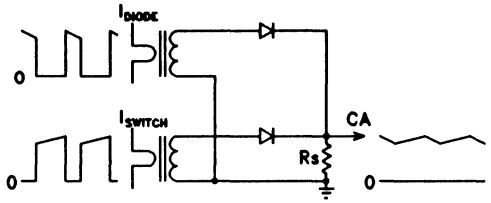

Fig. 16

Using Current Sense Transformers:
It is not difficult to achieve excellent results using low cost commercially available pulse transformers. A current sense "inductor" such as Pulse Engineering 51688 is a toroidal core wound with 200 secondary turns for a secondary inductance of 80 mH. A 0.18" hole is provided to slip the primary wire through.

The pulse voltage across the windings of a current transformer generates a magnetizing current which starts at zero and increases fairly linearly with time. The magnetizing current subtracts from the pulse current delivered to the secondary. Initially, the current through R_S is precisely I_{PRI}/N, but as time passes, the secondary current drops off more rapidly than it should. This effect is called "droop". It is usually not a problem if certain precautions are observed. The amount of current droop through the current sense resistor can be calculated:

$$\Delta I_{PRI(droop)} = \frac{N_S}{N_P}\frac{V_S}{L_S}\Delta t \qquad (17)$$

where N is the turns ratio, V_S the voltage across the secondary, L_S the secondary inductance and Δt is the max. pulse width. As the

equation shows, droop is minimized by maximizing secondary inductance–use the largest you can get. Don't use a large R_S value to obtain a large secondary voltage–its not necessary and makes reset more difficult. Make the turns ratio as low as possible by using two or three primary turns if space allows. Don't reduce the turns ratio by reducing the secondary turns–this is counter-productive because the inductance goes down with the turns *squared*.

For example, consider the flyback input current preregulator of Fig. 11, using a current transformer in series with switch instead of the 0.025Ω sense resistor shown. Using the Pulse Engineering #51688 current sense inductor with one turn primary, the turns ratio is 1:200. Secondary inductance is 80 mH. The 24A max. overload pulse current becomes a 0.12A current pulse on the secondary side. A 10Ω sense resistor will have a max. voltage of 1.3V sent to the CA, and the max. secondary voltage including diode forward drop is 2.0V. The maximum pulse width is 7.02μsec.

Applying these values to Eq. 17:

$$\Delta I_{PRI(droop)} = \frac{200}{1}\,\frac{2.0}{80\times10^{-3}}\,7\times10^{-6} = .035A$$

Only 35mA droop out of 24A isn't bad!

When two C.T.s are used–one on either side of isolation boundary-their turns ratios must be proportioned the same as the power transformer pri/sec turns ratio so that currents through R_S will be equalized.

All of the equations containing R_S given earlier in this paper assume the sense resistor is measuring current directly. When using a current sense transformer, reflect the actual R_S on the C.T. secondary side into the primary by substituting $R_S N_P/N_S$.

References:

[1] S.Hsu, A.Brown, L.Rensink, R.D.Middlebrook, "Modelling and Analysis of Switching DC-to-DC Converters in Constant Frequency Current Programmed Mode, "*IEEE PESC Proceedings,* 1979

[2] R.D.Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming," *IEEE PESC Proceedings,* June 1985

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Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution

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Abstract - **This paper describes a zero voltage switched (ZVS) resonant converter for driving cold cathode fluorescent lamps. Primarily intended for liquid crystal display (LCD) back-lighting, the circuit features minimal component count and size. A specially designed integrated circuit provides all control functions for a current fed push-pull ZVS converter, and also contains an auxiliary pulse width modulated (PWM) controller to develop a programmable supply voltage for the LCD. Analysis and simulation of the converter, and a complete circuit schematic are presented. The analysis and simulation results are validated by experimental circuit waveforms and critical performance parameters.**

Introduction

The proliferation of laptop and notebook computers places an ever increasing demand on display technology. High resolution and contrast are required to run today's graphics based programs, increasing the conflict between display performance, size and efficiency. The LCD with cold cathode fluorescent back lighting best satisfies this design requirement, however the lamp and its high voltage AC supply still remain the major contributor to battery drain.

The cold cathode fluorescent lamp (CCFL) requires 1-2 kV to fire. Sine wave drive is preferred to minimize RF interference and maximize lamp efficiency over time. Converter efficiency and size are extremely critical. These formidable requirements demand a highly efficient conversion topology and maximum circuit integration.

A zero voltage switched resonant topology will maximize efficiency by eliminating losses associated with charging parasitic capacitances to high voltages. This topology can be controlled using discrete circuitry. The most common implementation is a Royer oscillator modified to provide ZVS operation. While this at first appears to be a good solution, and is commonly used today, it suffers from several limitations.

High voltage DC to AC conversion is only part of the display supply. The average output current must be programmable for lamp intensity control, and the LCD requires a programmable low voltage supply for contrast adjustment. This additional circuitry, implemented discretely or with multiple ICs results in a large number of components, significantly impacting size and reliability. Synchronization is also preferred to eliminate beat frequency effects such as lamp intensity modulation, further complicating the design. Minimizing circuit complexity and bulk are best achieved through integration.

Cold Cathode Lamp Characteristics

The CCFL presents a highly nonlinear load to the converter as illustrated in fig. 1. Initially when the lamp is cold (inoperative for some finite time), the voltage to fire the lamp is typically more than three times higher than the sustaining voltage. The lamp characterized in fig. 1 fires at 1600V and exhibits an average sustaining voltage (V_{FL}) of 300V. Notice that the lamp initially exhibits a positive resistance and then transitions to a negative resistance above 1mA. These characteristics dictate a high output impedance (current source) drive to suppress the negative load resistance's effect and limit current during initial lamp firing. Since the ZVS converter has a low output impedance, an additional "lossless" series impedance such as a coupling capacitor must be added.

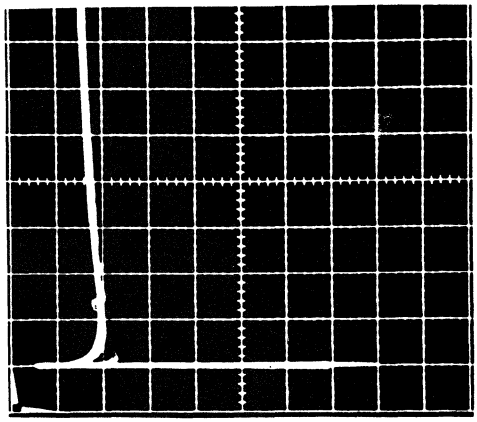

Fig. 1 Cold Cathode Lamp Current as a function of Voltage
Vertical: 2mA/div. Horizontal: 200V/div.

To facilitate analysis, the equivalent CCFL circuit shown in figure 2 is used. V_{FL} is the average lamp sustaining voltage over the operating range. The lamp impedance (R_{FL}) is a complex function but can be considered a fixed negative resistance at the sustaining voltage. Stray lamp and interconnect capacitance are lumped together as C_{FL}.

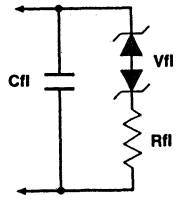

Fig. 2 CCFL equivalent circuit

ZVS Resonant Converter Topology

The current fed push-pull converter shown in fig. 3 is driven at it's resonant frequency to provide ZVS operation. The push-pull output MOSFETS (Q1 & Q2) are alternately driven at 50% duty cycle. Commutation occurs as V1 and V2 resonate through zero thereby insuring zero voltage switching. This virtually eliminates switching losses associated with charging MOSFET output and stray capacitance, and reduces gate drive losses by minimizing gate charge.

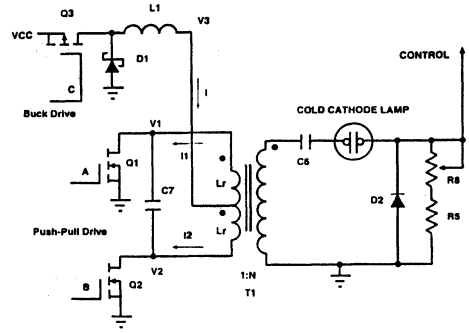

Fig. 3 Current Fed Push-Pull ZVS Resonant Converter

Current is supplied to the push-pull stage by a buck regulator (Q3). The control circuitry forces the average voltage across the current sense resistor (R8+R5) and rectifier (D2) to equal a reference voltage. Adjusted R8 varies the current and the lamp's brightness. The non-linearity introduced by D2 is insignificant since R8 is adjusted for a particular brightness with no concern of the actual current level.

Winding inductance, L_R, and C_R, the combined effective capacitance of C7 and the reflected secondary capacitances make up the resonant tank. The secondary side of the transformer exhibits a symmetrical sine wave voltage varying from about 300V to 1500V peak. Capacitor C6 provides ballasting and insures that the converter is only subjected to positive impedance loads.

Waveform Analysis

Simulated converter voltage and current waveforms are shown in fig. 4. At time t_0, the primary current (I1 & I2) has reached it's peak value. The push-pull drain voltages (V1 & V2) have resonated to zero. The primary voltage (V3) has also resonated to zero, and through the control circuitry commutated Q1 off and Q2 on. The energy stored in L_R is also at it's peak. This energy is transferred from L_R to the effective resonant capacitance (C_R) during time t_0 to t_1, causing C_R's voltage to sinusoidally increase.

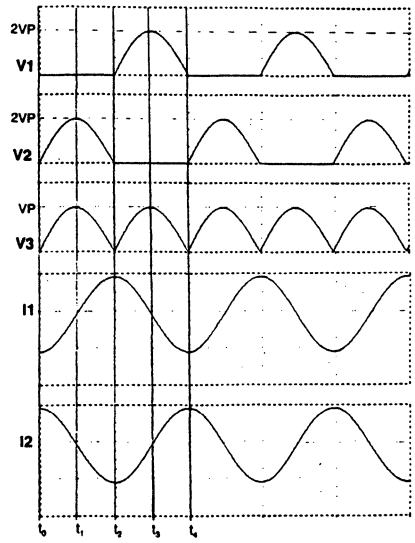

Fig. 4 Converter Voltage and Current Waveforms

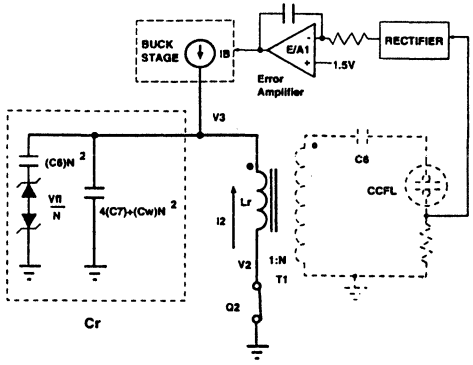

Fig. 5 Simplified converter model

At time t_1, all of the inductive energy in L_R has transferred to C_R, resulting in zero current through L_R and maximum voltage across C_R. From time t_1 to t_2, the energy transfers from C_R back to L_R, decreasing C_R's voltage while L_R's current increases.

The resonant current through L_R at time t_2 is equal and opposite to it's value at t_0. The reflected load current flows during the MOSFET on time, and is observed as a slight current amplitude asymmetry. The voltages at V1, V2, and V3 have resonated back to zero, causing the control circuitry to commutate Q2 off and Q1 on. The cycle continues symmetrically during the t_2 through t_4 interval, producing fully sinusoidal voltage and current waveforms.

Simplified Converter Model

The converter model shown in fig. 5, which is valid for one half cycle simplifies analysis by reflecting all impedances to the primary and eliminating the transformer. The differential voltage developed across the push-pull stage primary (V1-V2) exhibits twice the voltage excursion as the center-tap (V3). This reflects C7 to V3 through the turns ratio squared, resulting in 4(C7) at V3. The secondary winding capacitance is also reflected by the square of the turns ratio (n). Reflected winding capacitance is usually significant due to the high turns ratios typically employed. The buck stage operates in continuous current mode and is synchronized to the push-pull stage.

Lamp current is proportional to lamp intensity, and is used as the feedback variable. Buck current (I_B) is the response variable, which in turn regulates the average push-pull primary voltage. The coupling capacitor's high impedance transforms the secondary voltage to lamp current.

Control Equations

Variable Summary:

C_R = Effective resonant tank capacitance
C_W = Secondary interwinding capacitance
F_L = Average lamp voltage
I_B = Average Buck output current
L_R = Primary Winding Inductance
n = Transformer turns ratio
Z_{sec} = Secondary impedance

Fig. 6 shows the buck output stage and forced output voltage waveform. The output voltage is a rectified sine wave, corresponding to the synchronous, resonant push-pull stage input

9

voltage. The inductor output configuration exhibits high impedance at the resonant frequency and averages the output voltage throughout the cycle. The buck output voltage as a function of time is:

$$V_{out}(t) = V_p \sin(\omega t)$$

Where the angular frequency is:

$$\omega = 2\pi f = \frac{2\pi}{2t_1} = \frac{\pi}{t_1}$$

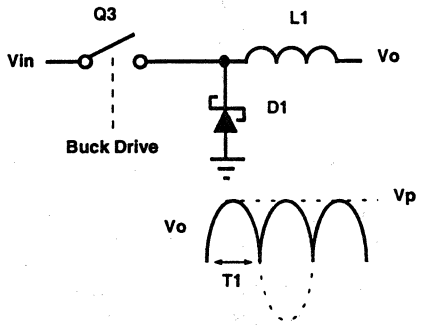

Fig. 6 Buck converter stage

The volts-second product across the inductor must be zero during steady state. Setting the on and off volt-second products equal and integrating gives the buck's transfer function:

$$V_{LR}(t_{on}) = -V_{LR}(t_{off})$$

$$\int_0^{t_{on}} V_{LR}dt = -\int_{t_{on}}^{t_1} V_{LR}dt$$

$$V_P = \frac{\pi}{2} Vi\ D \qquad (1)$$

This transfer function is identical to the familiar DC output buck transfer function, with the $\pi/2$ term accounting for peak versus average output voltage. As with the DC buck, primary voltage varies linearly with duty-cycle.

The peak primary voltage is also related to peak lamp current by:

$$V_P = \frac{(I_{FL(peak)})(Z_{sec}) + V_{FL}}{n} \qquad (2)$$

Setting (1) and (2) equal and solving for $I_{FL\ (avg)}$ expresses lamp current as a function of duty-cycle:

$$I_{FL(avg)} = \frac{DV_i\, n - \frac{2\ V_{FL}}{\pi}}{Z_{sec}} \qquad (3)$$

As expected from fig. 5, the lamp sustaining voltage, V_{FL} introduces a nonlinearity.

Buck output current is related to lamp current be equating input and output powers. The input power is:

$$P_{input} = \frac{1}{t}\int P dt$$

$$= \frac{1}{\pi/2}\int_0^{\pi/2} I\ V_P \sin(t)\, dt$$

$$P_{input} = \frac{2\ I_B\ V_P}{\pi}$$

The power to the load is:

$$P_{out} = V_{FL}\ I_{FL}\ (avg)$$

For analytical purpose, 100% power transfer is assumed:

$$P_{out} = P_{input}$$

$$V_{FL}\ I_{FL(avg)} = \frac{2I_B V_P}{\pi}$$

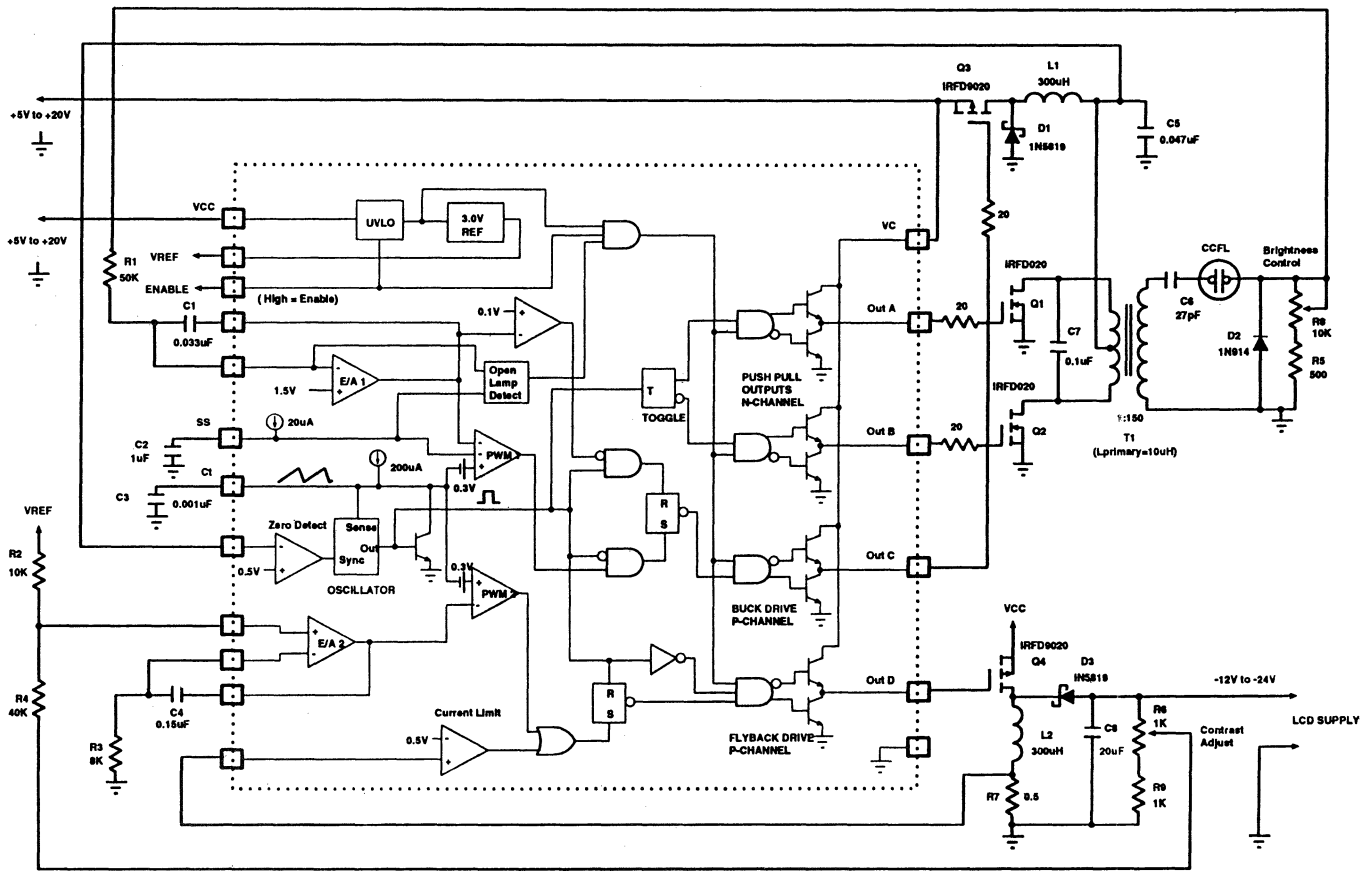

Fig. 7 UC3871 Application circuit

$$I_B = \frac{\pi I_{FL(avg)} V_{FL}}{2 V_P} \quad (4)$$

Substituting (2) for V_P in (4) gives the buck output current as a function of lamp current:

$$I_B = \frac{n V_{FL}}{Z_{sec} + \frac{V_{FL}}{\pi I_{FL(avg)}}} \quad (5)$$

The resonant frequency is approximately:

$$f_R \approx \frac{1}{2\pi\sqrt{L_R C_R}} \quad (6)$$

The nonlinearity introduced by V_{FL} causes the resonant frequency to vary with load. At very low lamp intensity the secondary voltage barely crests above V_{FL}. The effective resonant capacitance, C_R, is primarily the sum of C7 and C_W reflected to the primary. As the secondary voltage increase above V_{FL}, the reflected C6 value adds to the resonant capacitance, decreasing the frequency. The frequency range is approximated by assuming C6 has negligible effect at minimum lamp intensity, and fully adds to C_R at maximum intensity.

The peak resonant inductor current is the sum of the reflected load current from (5) and the resonant current:

$$I_{LR(peak)} = \frac{V_P}{Z_{tank}} + I_b \quad (7)$$

The tank impedance is determined by setting the resonant energy storage terms equal:

$$\frac{1}{2} L_R I^2 = \frac{1}{2} C_R V^2$$

Solving for V_R/I_R gives the tank impedance:

$$Z_{tank} = \sqrt{\frac{L_R}{C_R}} \quad (8)$$

Although relatively large currents are circulated through the resonant tank, the switches operate at low current levels. This is a direct result of the continuous resonant topology; the switches only must handle the energy that is removed by the load and lost in parasitics. The peak switch current is:

$$I_{SW(peak)} = I_b \quad (9)$$

The UC3871
A Completely Integrated Solution

Fig. 7 shows a complete application circuit using the UC3871 Synchronous Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

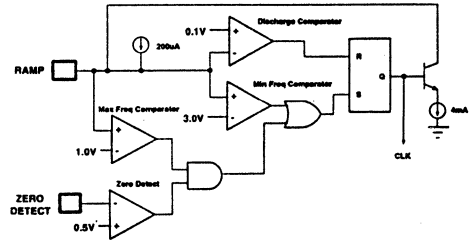

Fig. 8 UC3871 Oscillator Block Diagram

The Oscillator and synchronization circuitry are shown in fig. 8. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating

a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in fig. 9 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

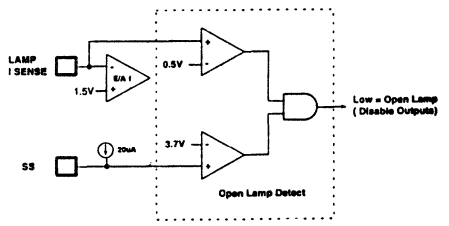

Fig. 9 Open Lamp Detect Circuit

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shut-down, the IC typically draws less than 100nA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

Application Circuit Example

The application circuit shown in fig.7 resonates at approximately 50khz. This frequency allow a reasonable compromise between size and efficiency. This relatively low frequency by today's standards results from high voltage insulation and spacing requirements, and practical limitations in reducing stray and interwinding capacitance. The half wave current sense signal is sensed by Error Amp 1 and averaged by integral compensation. The range of current control is 500µA to 10mA.

A flyback converter generates the LCD supply, outputting -12V to -24V to bias monochrome LCDs. Color displays normally require a positive bias voltage. Since this voltage typically must also be stepped up, a coupled inductor flyback is normally used.

Actual circuit waveforms agree with the spice simulated waveforms in fig. 4. Distortion caused by lamp nonlinearity is clearly visible at the operating extremes. At more nominal levels, the waveforms are more ideal, with only a small amount of observable distortion.

All of the following waveforms were taken at minimum and maximum lamp intensity to indicate worst case conditions. Nominal measured efficiency was 80%. Further improvement is possible with lower resistance magnetics and lower on resistance MOSFETs. Fig. 10 shows secondary output voltage, fig 11 shows lamp voltage, and fig. 12 shows lamp current. Notice that the lamp voltage is fairly constant with widely varying current. A frequency shift from about 48kHz to 57kHz is also observed over the lamp intensity range. The lamp current exhibits additional harmonics induced by it's nonlinearity. Push-pull MOSFET drain to source voltage is shown in fig. 13, and drain current is shown in fig. 14. The transformer center-tap voltage (buck output) is shown in fig. 15. All waveforms are sinusoidal, exhibiting minimal harmonic content.

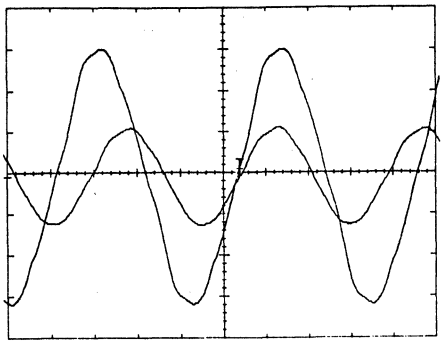

Fig. 10 Secondary output voltage
Vertical: 500V/div. Horizontal: 5μs/div.

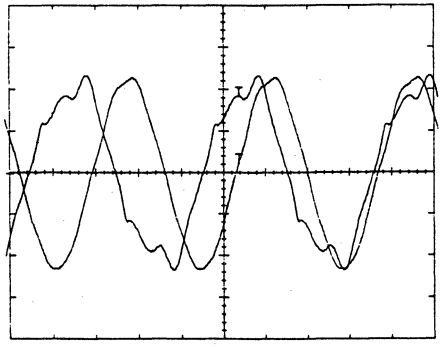

Fig. 11 lamp voltage
Vertical: 200V/div. Horizontal: 5μs/div.

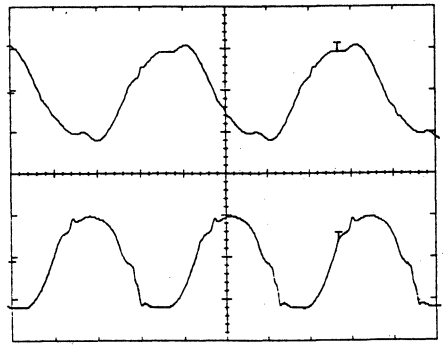

Fig. 12 Lamp current
Vertical: 10mA/div. Horizontal: 5μs/div.
500μA/div.

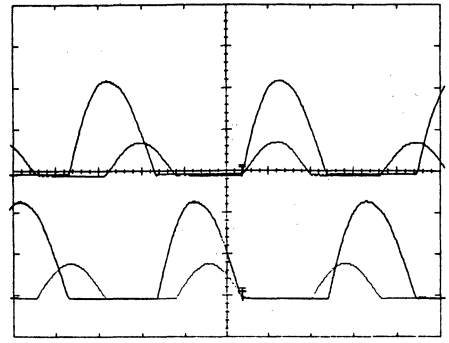

Fig. 13 Push-Pull MOSFET drain to source voltage
Vertical: 10V/div. Horizontal: 5μs/div.

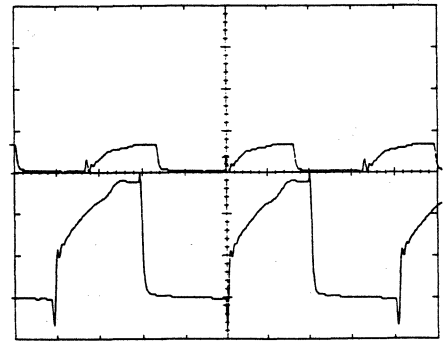

Fig. 14 Push-pull MOSFET drain current
Vertical: 200mA/div. Horizontal: 5μs/div.

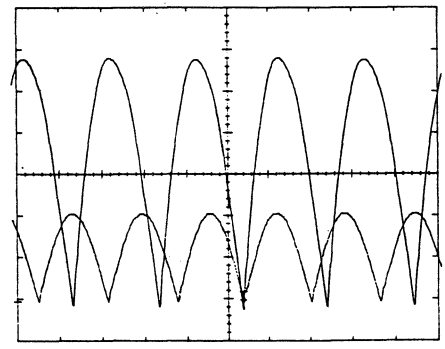

Fig. 15 Buck output voltage
Vertical: 200mA/div. Horizontal: 5μs/div.

Summary

The current fed push-pull ZVS converter efficiently develops high voltage, sinusoidal power for driving cold cathode fluorescent lamps. Design equations have been derived, and verified experimentally, simplifying application circuit design and analysis. The UC3871 provides a complete solution for high performance back-light and LCD power supplies.

APPLICATION NOTE

VOLTAGE-MODE CONTROL REVISITED - A NEW HIGH-FREQUENCY CONTROLLER FEATURES EFFICIENT OFF-LINE PERFORMANCE

by

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ABSTRACT

With modern day emphasis on advanced power supply topologies, the advantages of voltage-mode control have been neglected. A new control IC optimizing this topology for high-frequency, off-line applications brings voltage-mode control into the modern era and combines the efficiencies and high frequency performance of a BiCMOS design with a noise resistant, low-cost circuit solution.

INTRODUCTION

With all the interest in advanced power control topologies such as peak and average current-mode, resonant and quasi-resonant approaches, soft switching and phase shift control, it is easy to lose sight of the fact that "old-fashioned" voltage-mode still has a lot to offer. Specifically, in applications where control is needed over wide variations in line and load, the use of voltage-mode control will maintain stable, noise-free performance over a wider range of operating conditions than any other circuit topology. When more recent circuit enhancements such as voltage feed-forward, programmable duty-cycle clamping, fast current limiting, and low-power BiCMOS processing are included, a very effective and yet easy-to-use power control component is the result.

LIMITATIONS OF CURRENT-MODE CONTROL

With the introduction of current-mode control back in 1983, several important performance enhancements were featured, including:

* Instant response to line variations
* Inherent pulse-by-pulse current limiting
* Faster loop response

While these characteristics were quite significant compared to the technology of the day in 1983, more recent developments have shown that current-mode control is not the only way of achieving them. Specifically, voltage feed-forward can be added to voltage-mode circuits to accomplish the same instant response to line voltage, and the fast current feedback loop necessary for effective current limiting of current-mode circuits is equally applicable to voltage mode. While current-mode does minimize the effect of the output filter inductance - a characteristic which can be used to improve overall gain bandwidth - increasing the switching frequency can push the output filter resonant frequency to the point where excellent response can still be achieved, even with a two-pole output filter.

Before discussing the positive aspects of voltage-mode control, it is worth spending a little more time on current-mode. Although the past 10 years have seen many highly successful designs which have utilized peak current-mode topologies, few would argue with the contention that the design process is more complex. For example, some of the design considerations which are unique to peak current- mode control are:

* Dealing with the leading-edge current spike usually present on the current ramp waveform.

* Dealing with additional noise or ringing on the current waveform when the power switch turns off.

* Adding the appropriate amount of slope compensation for stable operation.

* Analyzing circuit performance with two feedback loops.

* Providing good regulation with multiple outputs.

* Obtaining an adequate amplitude ramp waveform for stable pulse-width modulation at light load and minimum input voltage.

Although solutions can and have been found for all the above issues, they do not come without a good deal of difficulty, and since none of them apply to voltage-mode control, there is a growing incentive to readdress this topology.

VOLTAGE-MODE REVISITED

The typical voltage-mode circuit will use a fixed-frequency, constant-amplitude ramp waveform to compare against the output from an error amplifier. As the error amp's output moves up and down the ramp, a corresponding change is made to the power switch's on- time. With a large-amplitude ramp waveform which is disassociated from the supply's power stages, noise-free pulse-width modulation is much more readily achievable. The traditional problem with this form of control is that a change in the input voltage must go through the output filter, be sensed as an error at the output, and be fed back to change the modulation and provide a correction.

Current-mode control bypasses this process as a change of input voltage is directly impressed across the output inductor, which immediately changes the slope of inductor current, and since this is the ramp which controls the PWM, response within one switching period is achieved.

The same result can be achieved with voltage-mode control, however, by making the slope of the oscillator-derived ramp proportional to input voltage. This is voltage feed-forward which means input variations are fed directly to the modulator, bypassing the output filter and the error amplifier. In addition to providing instant response, the input voltage term is canceled from the forward transfer function, resulting in constant gain and a simpler feedback compensation problem. Since the voltage ramp waveform is typically derived from the timing oscillator, the trick is to provide this variable slope while maintaining a constant switching frequency. Another feature which is highly desirable, and often implemented in this same section of the control circuitry is the ability to limit the maximum switch duty-cycle to insure non- saturation of the magnetic components of the power supply. The combination of all these features was a major goal in the development of a new voltage-mode control integrated circuit - the UCC3570.

INTRODUCING THE UCC3570

The objective in the design of the UCC3570 was to develop an easy- to-use controller, optimized for low-power off-line applications, free of the noise and stability issues of current-mode control, but allowing equal or better power supply performance to be achieved. An important technique in achieving this objective was the utilization of a BiCMOS manufacturing process which offered high speed circuitry with low internal current consumption and small overall die size. This last characteristic has allowed the full- featured UCC3570 to be offered in the 14-pin small outline, surface mount package.

The overall block diagram of the UCC3570 is shown in Figure 1. Remembering again that this device is optimized for low-power, off- line applications, it can be seen from Figure 1 that the basic architecture includes the following features in addition to voltage feed-forward:

* A fixed-frequency pulse-width modulator
* Provisions for low-current off-line startup
* A single high-current totem pole output driver
* Unique voltage and current fault protection

Other performance features which have been included in this design include programmable deadband control, soft-start turn on, highspeed current limiting, latched shutdown capability, a synchronizable oscillator, and the availability of a five-volt bias source. A voltage error amplifier is not included as off-line power supplies almost always require isolation and the optimum location for the error amplifier is on the secondary side of the isolation boundary. Here the feedback gain can be incorporated with voltage sensing and the system reference in an IC such as the UC39431 which combines these functions with an optimum drive circuit for an

optocoupler. Figure 2 illustrates the use of this device with the opto as an ideal means of providing an isolated feedback signal to the primary side UCC3570.

The following discussion will provide a better understanding of the unique features of the UCC3570.

RAMP GENERATION CIRCUITRY

The ramp generation portion of the UCC3570, which is shown in Figure 3, actually performs several circuit functions. The ramp waveform is formed on an external capacitor which is charged with a current source proportional to the input line voltage and discharged with a user-setable constant current sink. The circuit is clocked from a constant-frequency, separate oscillator which, in turn, can be either free running or externally synchronized. Switching between the charging and discharging currents is accomplished by a flip-flop which is set with the constant- frequency clock signal, and reset when the ramp reaches four volts. To accomplish a constant ramp amplitude, the bottom of the ramp is held at one volt while awaiting the clock command to start the next charge cycle. The logic is defined such that an output drive pulse can only occur during the rising portion of the ramp waveform and is held off for both the fall time and any wait time prior to the start of the next switching period.

This operation can be visualized with the aid of Figure 4 which shows the three regions in the ramp waveform: the variable rise time, the programmed constant fall time, and the wait time which is the remainder of the constant overall switching period. Figure 5 shows the effect of changing operating conditions on the ramp waveform. With the assumption of a constant feedback voltage, a high line voltage yields a fast rise time and a narrow output pulse, while a low line voltage reduces the rise time to produce a wider output pulse. The relationship is linear so that the result is a constant volt-second product to the power transformer, regardless of input voltage. If the fall time is set to provide a minimum output deadtime at the minimum input voltage - as in Figure 5B - a higher voltage will increase the minimum deadtime - as in Figure 5A. If the input voltage should fall below the expected minimum such that the ramp has not reached 1V by the end of the period, then the ramp will miss the clock signal and remain reset with the output off for the entire next period - as shown in Figure 5C.

Note that the ramp discharge current is determined by external current-setting resistor R4. In addition to the output deadtime, this resistor also programs the currents for the timing oscillator, the soft-start, and fault shutdown circuits.

One last function contained within the ramp circuitry is that the Vfwd terminal which monitors the input line voltage to control the ramp up-slope has boundary limits established by a pair of shutdown comparators which define a 4:1 operating range. Should the voltage at this pin rise above 4V, or fall below 1V, the PWM output will be forced off. More about this feature in the Fault Protection section.

START-UP FEATURES

The features in the UCC3570 associated with startup and shutdown are shown in Figure 6. Note that there are two terminals which are connected (through an impedance) to the high voltage DC bus, Vin, and both contain voltage monitoring functions. Vfwd measures the bus voltage directly through divider R1/R2 and, with no capacitance, this pin will respond instantly to line voltage changes. The Vcc pin, on the other hand, responds to line voltage changes with a delay caused by the C1/R5 time constant. Since the voltage at both pins must be above minimum for operation, the usual process is that turn on is initiated by the voltage at Vcc while turn off is triggered by a falling voltage at Vfwd. The turn on sequence should proceed as follows:

1. Vfwd rises above 1.0V. Icc will be less than 100uA.
2. Vcc rises above 13V and activates the internal reference. At this point, Icc will increase to approximately 1mA plus any loads on the reference.
3. When Vref rises above 4.5V, the Soft-start clamp is released and as the voltage on Cs rises, the output will start switching with increasing pulse-widths. With the onset of switching, Icc will rise to a value determined by the power switch gate charge requirements and the switching frequency.

As Icc increases, Vcc will probably fall but with 5V of hysteresis, significant energy may be drawn from C1 before turn off is initiated by the UVLO comparator. If this should occur, the circuit is reset, reducing Icc back to 80uA, and thus allow another attempt to start.

FAULT PROTECTION

The circuitry within the UCC3570 associated with fault protection is shown in Figure 7. The potential faults which have been considered and provided for include the following:

* Over and under voltage on the input line.

* Excessive load current of a temporary nature.

* A continuous overload or shorted output.

In addition, there are several ports where a shutdown command may be inserted, either directly or through an optical coupler from load-related faults.

Note from Figure 7 that there are four inputs to the PWM-stop OR gate, any one of which will immediately terminate output pulses and hold them off for as long as that signal is high. Three of these come from the line over- and under-voltage comparators and the current limit comparator and provide for pulse-by-pulse shutdown. The fourth comes from a shutdown latch which provides for a permanent shutdown until reset by a low signal from either Vfwd or Vcc. These two pins allow several operating options. By appropriately selecting the source impedance to Vcc, the circuit can be made to permanently latch off or automatically restart depending on whether the load with no bootstrap energy will pull the voltage on Vcc below its

low threshold. If Vcc falls below 9V, the shutdown latch will reset and the circuit will restart. If it does not, reset must come from Vin, either by temporally removing input power or by momentarily pulling Vfwd low.

Setting the shutdown latch also can come from two sources. If the current limit pin sees a level of 0.6V (as distinguished from the pulse-by-pulse threshold of 0.2V) the latch will be set. In addition, every time the 0.2V level is exceeded, an increment of current will be delivered to the Count pin. This current will be integrated by means of the external capacitor, Cf, and when the voltage exceeds 4V, the shutdown latch will also be set providing for a delayed shutdown with user selectable time constants. Note that any time the shutdown latch is set, the soft-start capacitor is discharged providing for a controlled restart.

A 50-WATT FLYBACK EXAMPLE

Figure 8 is the schematic for a 12V, 4A supply capable of operating from an 85 Vrms to 265 Vrms power line. This circuit incorporates all the protective features described and is most noteworthy by the minimum number of active devices needed. With a switching frequency of 100 kHz, the efficiency is close to 90% over the full line voltage range, allowing the circuit to be packaged in a very small module with minimal heat sinking requirements. A contributor to the high efficiency is allowing the duty-cycle to extend to 60% with the assurance of an absolute clamp at that level. Automatic restart after a shutdown is provided with a time constant of approximately 25 msec defined by the value of the soft-start capacitor, and the delayed shutdown is set to accept 5000 over- current pulses before activation. (approximately 60 msec)

The transformer consists of a total of 79 turns on a EI375 core with a 36 mil gap. The 1.2 cu in size of this design was greatly aided by the fact that a minimum of 4 usec of reset time is assured, allowing maximum utilization of the core. With a 12V output, the rectifiers allow as little as 5% reset voltage under short circuit conditions which would normally let the transformer ratchet up to saturation, a problem which the shutdown latch effectively alleviates.

SUMMARY

While the modern power supply designer today has innumerable choices available from which to select the configuration and the components to satisfy his requirements, the combination of efficient operation, simple control algorthym, high level of protection, ease of programmability, and low cost all point to the UCC3570 as the controller of choice for for a broad range of off-line power requirements.

Acknowledgement: This Application Note was originally presented in a paper at the 1993 High Frequency Power Conference sponsored by INTERTEC Communications and was published in the Conference Proceedings.

A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

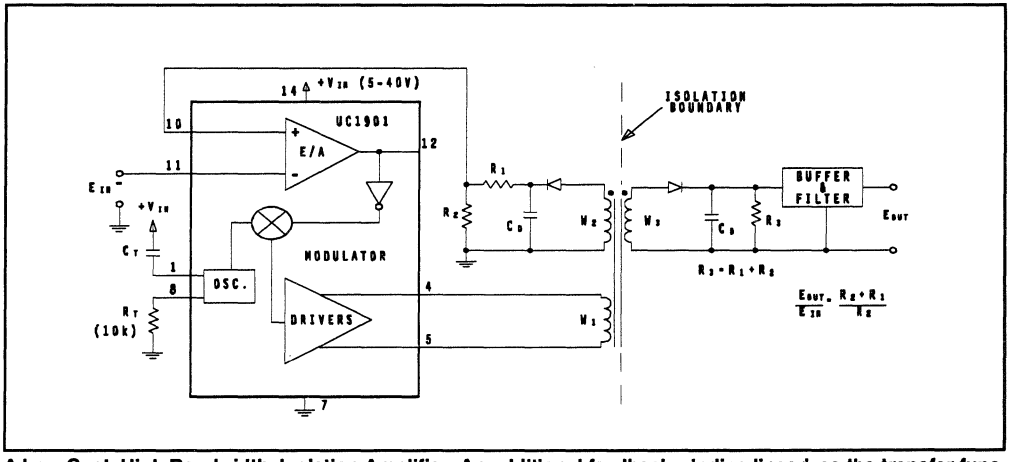
The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal, AC, transfer functions can be established across the isolation boundary.

The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W2 and W3) on a small signal transformer. The demodulated signal from winding W2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

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UC3842A
LOW COST START-UP AND FAULT PROTECTION CIRCUIT

This circuit optimizes control circuit performance to include:

- **Low Start-up Current, Less Than 0.5 ma**
- **MOSFET Compatible Undervoltage Lockout Thresholds 16V Turn-on, 10V Turn-off**
- **Programmable Restart Delay HICCUP Fault Protection**
- **Auxiliary 5V Precision Reference**
- **Overvoltage/Overtemperature Protection**

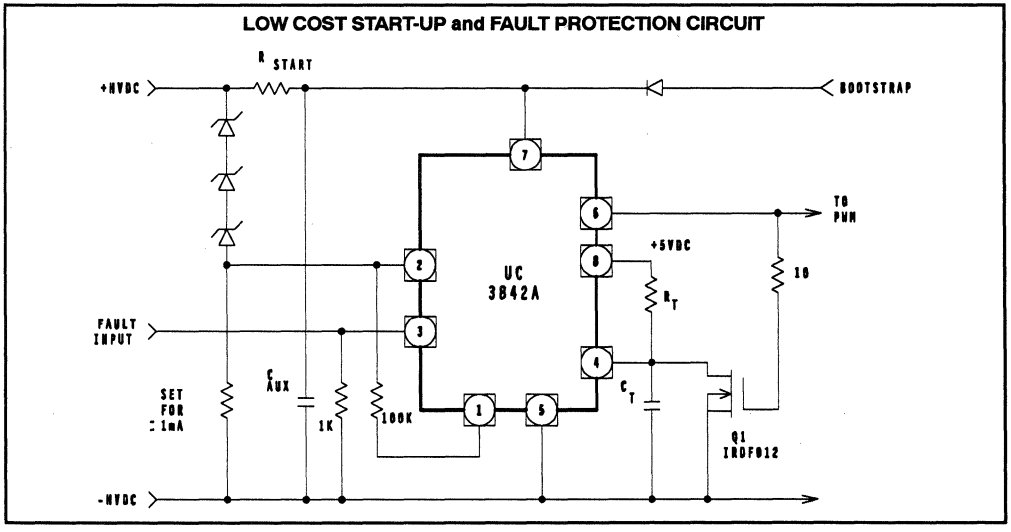
CIRCUIT DESCRIPTION AND OPERATION:

The UC3842A Controller is featured in this design ***NOT*** as the power supply control IC, but in a supervisory function to assist the principal PWM. It will be utilized to facilitate a low current start-up of less than 0.5 milliamp from the high voltage bulk supply. Additionally, the UC3842A features 16 volt turn-on and 10 volt turn-off thresholds, ideally suited for power mosfet gate drive circuits. The 1 amp output of the UC3842A is used to switch the auxiliary supply voltage to the principal PWM controller, a UC3825 or UC3846 for example.

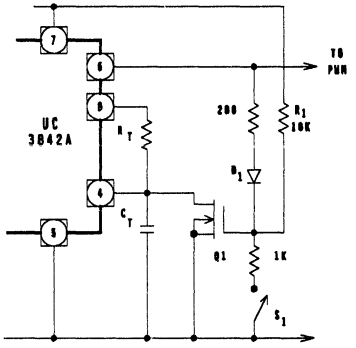
The oscillator of the UC3842A is configured to generate a constant off time, corresponding to the desired restart delay interval. At the beginning of its operation, the UV initiates a clock cycle and the PWM output at pin 6 goes high. This is fed to transistor Q_1 which pulls the R_t/C_t input at pin 4 low, thus "freezing" the oscillator, while keeping the PWM output high. Once a valid fault (greater than 1 volt) is received at the current sense input (pin 3), the output at pin 6 will go low. Transistor Q_1 is then turned off, and the oscillator generates an off period, or delay as programmed by the R_t/C_t components. This procedure will repeat as often as dictated by the fault conditions, but significantly reduces the average short circuit currents and power dissipation.

The UC3842A's current sense node is used as the fault input, and can be configured to provide numerous safeguards. Primary overvoltage protection is accomplished by using a simple resistor divider network or series string of zener diodes to the high voltage rail. Overtemperature protection is possible by including the UC3730 Precision Thermal Monitor IC, or a variable impedance thermistor. In a simple configuration, the fault circuit is designed to deliver a 1 volt input to pin 3 of the UC3842A when a fault response is necessary. The error amplifier can also be biased to accept lower amplitudes of valid fault inputs at the current sense input. A precision five volt auxiliary supply is made available at the IC's reference output, pin 8 and can supply 20 milliamps maximum.

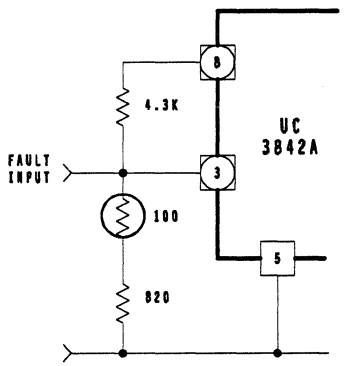
UC3842A Supervisory Function Circuits



COMBINED LATCH/RESET/HICCUP FUNCTIONS
General Circuit



OVER-TEMPERATURE PROTECTION
using 50 to 100Ω thermocouples



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UC1842/UC1842A FAMILY
SUMMARY OF FUNCTIONAL DIFFERENCES

The industry standard series of UC1842/43/44/45 devices has been improved for higher frequency, off-line power supplies. This new "A" series of controllers, UC1842A/43A/44A/45A, feature three major advantages over their predecessors as shown in the summary below.

Start Up Current

	UC1842/45	UC1842A/45A
Typical (T_J = 25°C)	0.5ma	0.3ma
Maximum (T_J = 25°C)	1.0ma	0.5ma

Oscillator Discharge Current

	UC1842/45			UC1842A/45A		
	MIN	TYP	MAX	MIN	TYP	MAX
At T_J = 25°C (mA)	7	10	13	7.8	8.3	8.8
Overtemp. Range	6	—	14	7.5	—	8.8

Output Saturation

	UC1842/45	UC1842/45A
During UVLO	1V @ 0.2ma	1V @ 10ma

The reduced start-up current is of particular concern in offline supplies where the IC is "powered-up" from the high voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Lowering this by 50% in the "A" version family will reduce the resistors power loss by the same percentage.

Precision operation at high frequencies with an accurate maximum duty cycle can now be obtained with the "A" family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or deadtime.

Another significant improvement has been made in the output section, specifically to the lower totem-pole transistor's operation during undervoltage lockout. The "A" series of devices prevent the power MOSFETs from parasitically turning-on at powerup due to the "Miller" effect. This new technique allows the IC to sink higher currents at lower saturation voltages than it's predecessors.

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UC3840/UC3841/UC3851 PWM CONTROLLERS SUMMARY OF FUNCTIONS AND DIFFERENCES

The UC3840/UC3841 and UC3851 PWM controllers incorporate numerous protection features for switch mode power supplies. The list includes programmable undervoltage lockout thresholds, programmable current limit thresholds, overvoltage protection, soft-start and external stop/reset capability. While these controllers are similar in concept, there are subtle differences amongst them in the operation of the error latch circuitry, specifically, the external stop and reset inputs. The UC3841 and UC3851 ICs feature an improved circuit design which simplifies the interface to the internal protection circuitry. A summary of the functions and modes of operation is listed below.

EXTERNAL STOP

	UC3840	UC3841/51
Low (<0.8V)	Stop	Defeat E/L Operation
High	Normal	Stop
Open	Normal	Normal
Cap. to GND During Power-up	Not Recommended	Delay E/L Operation at ~ 13msec/μF

E/L= Error Latch

RESET

	UC3840	UC3841/51
High (>3.2V)	Latch	Latch
Low (<2.8V)	Requires UV Cycle to Reset	Reset

SOFT START

	UC3840	UC3841/51
After UV or Reset	Unlatched	Latched (Vss ≤ 0.40V)

The UC3851 controller incorporates two additional features, a toggle flip-flop for an accurate 50% maximum duty cycle clamp, and a 1 amp peak totem-pole output for driving power MOSFETs. Maximum duty cycles and output configurations for each device is shown below.

MAXIMUM DUTY CYCLE (T_J = 25°C)

	UC3840/41	UC3851
R_T = 20k, C_T = 1nF	0-95%	0-46%

PWM OUTPUT

	UC3840/41	UC3851
1A (PK)	Open Collector Active Low	Totem Pole Active High

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UC3842A FAMILY
FREQUENCY FOLDBACK TECHNIQUE PROVIDES PROTECTION

Excessive power dissipation in switching devices can occur during start-up and overload conditions in many switchmode power supplies. Many sophisticated PWM controllers provide the means for protection against these conditions; however, simple low-cost controllers will require additional circuitry. The circuit described below utilizes only one additional resistor and transistor to enhance the performance of the UC3842A family of controllers.

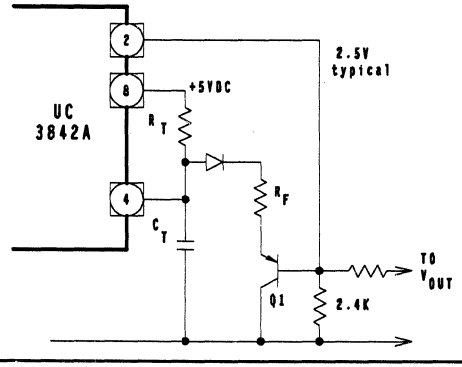
The power supply output voltage is fed to the error amplifier inverting input (pin 2) at a 2.5 volt amplitude under normal operating conditions. During start-up or overload, however, this voltage can drop to zero. The circuit shown uses this feedback voltage to divert normal charging current from the IC's timing capacitor to ground whenever the feedback voltage is below the 2.5 volt nominal. A linear three-to-one reduction of oscillator frequency is obtainable for most applications. This technique lengthens the potential maximum on-time and reduces the programmed deadtime. In many circuits, however, the peak current limit threshold is reached early in the cycle under these overload conditions, and this is not a problem. For most applications, the foldback resistor value (R_F) should equal that of the timing resistor (R_T).

EXAMPLE:

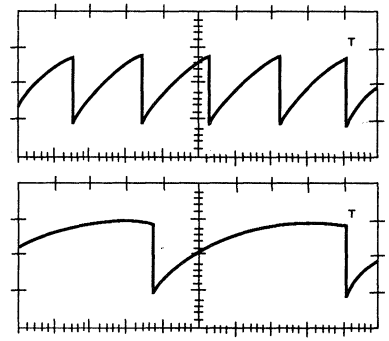
100 kHz operation, R_T = 15k, C_T = 1 nF, R_F = 15k, Q_1 = 2N2907A

OPERATING MODE	NORMAL	OVERLOAD
$V_{E/A}$ - (pin 2)	2.50V	0.00V
Oscillator Freq.	105 kHz	36 kHz

FREQUENCY FOLDBACK TECHNIQUE CIRCUIT



OSCILLATOR FREQUENCY



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PROGRAMMABLE ELECTRONIC CIRCUIT BREAKER

The design of a programmable electronic circuit breaker is shown below which utilizes the UC3843A control IC to facilitate a high speed turn-off following an overcurrent condition. This low cost, industry standard IC contains the required protection features and drive capability in a single 8 pin device.

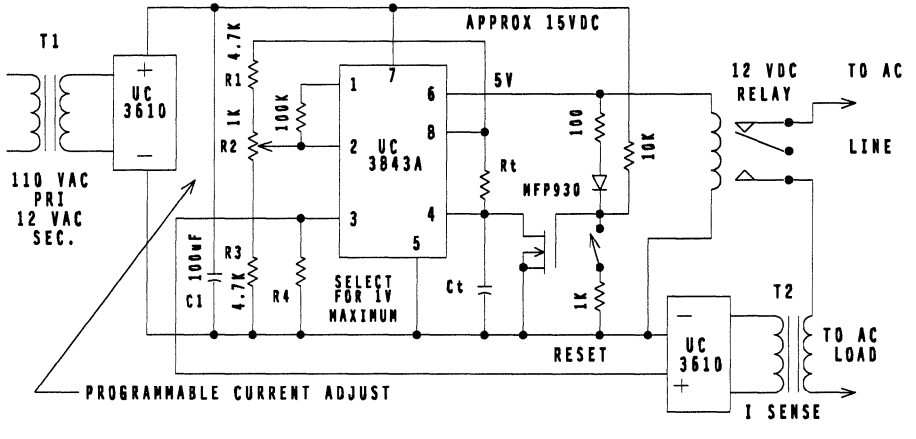
CIRCUIT OPERATION

Power to the controller is provided by a simple, low cost 60Hz transformer from the AC line which delivers 12 VAC at the secondary. The output current is determined primarily by the relay used with an additional 10 milliamps, or so, drawn by the IC. Undervoltage lockout prevents any operation until 10 VDC is obtained across capacitor C1, when the UC3843A will turn on. The PWM output at pin 6 goes high which drives the relay ON and switches the load across its respective power source. The load current is sensed by the current transformer T2, multiplied by its turns ration(N) and develops a voltage across the sense resistor R4. This resistor is scaled to delivery 1 volt maximum at the full load current and is one input to the PWM comparator.

While the output at pin six is high transistor Q1 is also turned ON which disables the ICs oscillator, locking the output high until toggles by the PWM. A 10k resistor (R5) to the supply voltage (pin 7) supplies bias to Q1 after the output has gone low, providing a latched OFF condition. This can easily be reset by pulling Q1's gate low through 1k ohms to ground as shown.

SCHEMATIC DIAGRAM

ELECTRONIC CIRCUIT BREAKER FEATURES HIGH SPEED CURRENT LIMITING



The other input to the PWM comparator is represented by the voltage at pin 1, the error amplifier output which can be adjusted by resistor R2. Internally, this voltage is reduced by two diode drops then attenuated to one-third its amplitude. The PWM circuitry compares this voltage with that of the current sense input at pin 3. When the current sense input exceeds the threshold set by resistor R2, the comparator is tripped and the ouptput at pin 6 is latched OFF.

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CURRENT MODE CONTROLLED QUASI-RESONANT ZERO VOLTAGE SWITCHING POWER CONVERSION

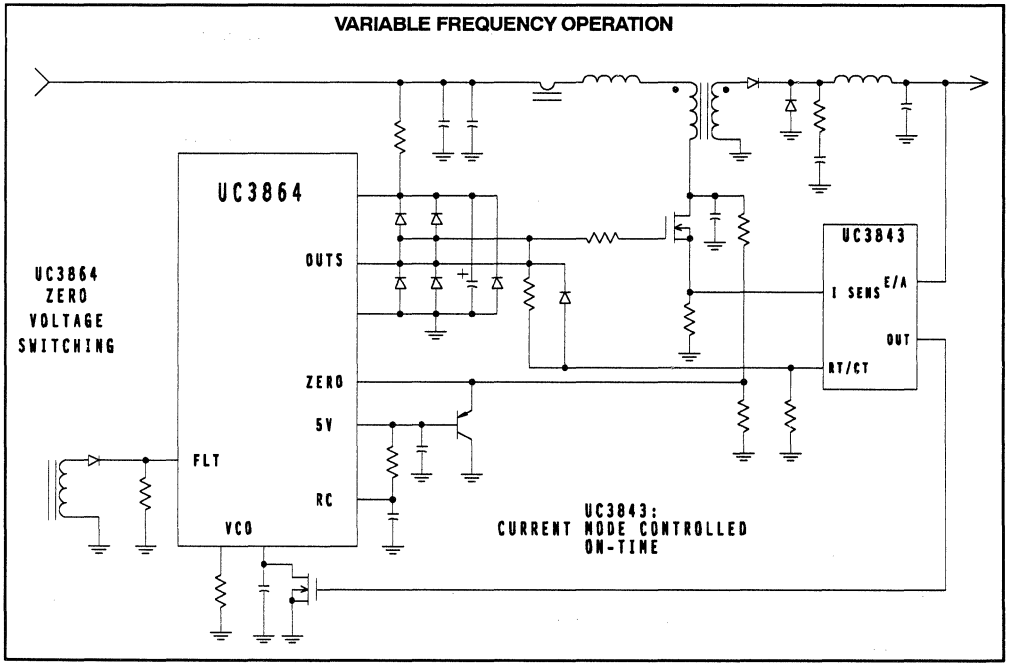
Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise switch ON time, an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

PRINCIPLES OF OPERATION

Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator (VCO) to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry in their standard configuration. When the resonant capacitor voltage crosses zero, the UC3864 output goes high. This turns ON transistor Q1 and recycles the UC3843A which initiates the next current mode controlled period. The UC3864 error amplifier and VCO are not used, however the fault protection circuitry will still respond to an overcurrent fault.

CURRENT MODE CONTROLLED ZVS FORWARD CONVERTER



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OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES

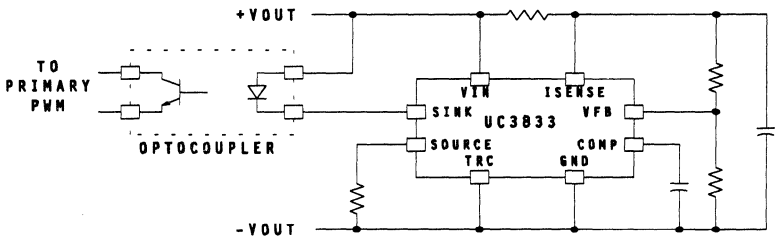
The use of optocouplers in the feedback path of switch-mode power supplies is probably one of the most common practices in the industry. Benefits of this method include low component cost, high voltage isolation and simplicity of design and implementation. Although adequate for many existing designs, the need for additional loop gain bandwidth occurs as switching frequencies are pushed towards the megahertz region.

One of the most popular ways to drive an optocoupler utilizes a TL431 Adjustable Shunt Regulator. It is configured on the output side of the power supply to modulate the optocoupler's photo diode current as a function of the power supply output voltage. Across its isolation boundary, the optocoupler transistor is connected to the PWM controller's error amplifier on the primary side of the power supply. Variations in the output voltage are optically transferred back to the error amplifier and control loop for correction. Providing additional features like over current protection or external shutdown require extra optocouplers and drive mechanisms, thus increasing the circuit complexity.

A linear regulator control IC, such as the UC3832, UC3833 or UC3836 can be substituted for the '431 while providing numerous additional features besides regulating the output. Overcurrent limiting and fault protection can be combined with the error voltage to drive the optocoupler and override it when necessary. Handshaking with external control logic, such as shutdown and sequencing is greatly simplified since the control IC is referred to the same ground. The most obvious benefit, however, is the introduction of the supplementary error amplifier in the feedback loop with programmable compensation.

Depending on the specific application, current limiting can be tailored to accommodate a programmable foldback characteristic, constant current or complete overcurrent shutdown. The UC3832 and UC3833 provide an addition level of versatility by offering a programmable duration event timer in the current limit circuitry. An adjustable trip threshold to accommodate varying load demands can be facilitated with the UC3832. For additional information, please consult application note U-116 and the respective device data sheets.

UC3833 LINEAR CONTROL IC DRIVES OPTOCOUPLED FEEDBACK



9

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Design Note

OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES USING THE UC 3901 AND UC3903

Numerous techniques and devices are available to the designers of optocoupler feedback circuits. The more traditional approaches utilize either an adjustable shunt regulator like the TL431 device or an op-amp and voltage reference as the optocoupler driver. While these approaches do satisfy the basic requirements in many applications, quite often they lack the performance that is achievable from a more sophisticated circuit. Too often, these low cost solutions necessitate additional protection circuitry elsewhere in the control circuit to overcome the deficiencies in the feedback path.

A variety of low cost supervisory ICs contain the required building blocks for the more demanding optocoupler feedback drive applications. Initially developed to address other specific power supply tasks, several control ICs excel in the role as precision optocoupler control and drivers.

The basic building blocks necessary for optocoupler feedback control are a precision reference, an error amplifier and a drive stage capable of approximately 20 milliamps. In a typical application, the power supply output voltage is monitored and compared to a reference voltage to the error amplifier inputs. Loop compensation and gain are programmed around the amplifier, and the resultant error voltage (Ve) modulates the optocoupler drive current, hence feedback.

In addition to the simple regulation of output voltage, several other housekeeping functions can be performed on the secondary side of the power supply - all with a single integrated controller. Fault protection, for example, from an over voltage or an over current condition can be detected and used to override the normal optocoupler drive. An undervoltage lockout feature could prevent false feedback information during power-up and power down sequences of the power supply. Also, a POWER-OK indicator could separately communicate with the primary side controller, or used to gate the optocoupler drive at the secondary side.

Basic Optocoupler Driver Circuit

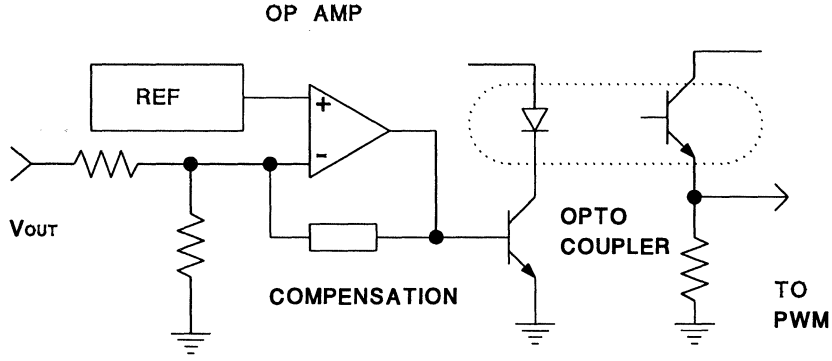

Figure 1.

THE UC 3901 ISOLATED FEEDBACK GENERATOR

Many isolated feedback applications required higher performance than can be obtained from an optocoupler feedback technique. Generally, these fall into one of two categories; high frequency switchers (above 250kHz) and those with very high voltage isolation requirements (greater than 5kV). The UC 3901 was developed to amplitude modulate a high frequency carrier applied to a transformer in place of the optocoupler. A peak detection circuit is used to reconstruct the error voltage waveform across the isolation boundary.

By disabling the internal oscillator, no chopping occurs and the outputs operate as linear drivers. When placed across an optocoupler this configuration yields similar results to other drive techniques - with two advantages. First, a closed loop startup of the power supply can be obtained since both inputs to the error amplifier are made available. Rather than using the traditional approach of soft-starting the error amplifier output, the noninverting, or reference input is gradually ramped up. This technique prevents a large overshoot from occurring as the output approaches regulation. In contrast to the prior method, the amplifers loop compensation network is not abnormally biased during startup - causing the output excursions. Additionally, an over and under voltage detection is available at the UC3901 "Status output" pin. This open collector output can drive a separate fault indication optocoupler for communication to the PWM controller.

Optocoupler Drive Circuit Features Additional Protection

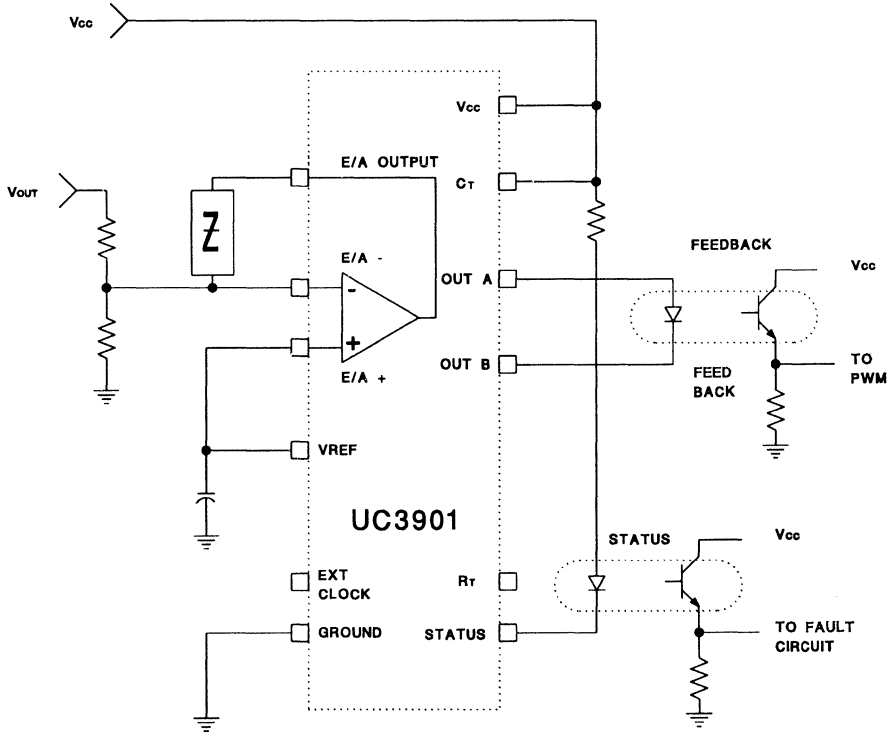

Figure 2.

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IGBT DRIVE USING MOSFET GATE DRIVERS

John A. O'Connor

IGBT Drive Requirements

Insulated gate bipolar transistors (IGBTs) are gaining considerable use in circuits requiring high voltage and current at moderate switching frequencies. Typically these circuits are in motor control, uninterruptible power supply and other similar inverter applications. Much of the IGBTs popularity stems from its simple MOSFET-like gate drive requirement. In comparison to bipolar transistors which were formally used in such designs, the IGBT offers a considerable reduction in both size and complexity of the drive circuitry. Recent improvements in IGBT switching speed has yielded devices suitable for power supply applications, thus IGBTs will compete with MOSFETs for certain high voltage applications as well. Many designers have therefore turned to MOSFET drivers for their IGBT drive requirements.

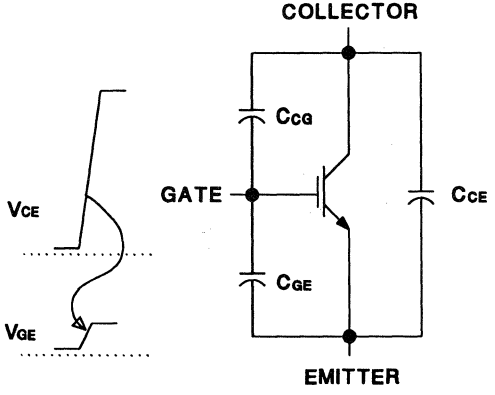

Figure 1. High dv/dt at the collector couples to the gate through parasitic capacitance.

IGBT drive requirements can be divided into two basic application categories: Those that do not apply high dv/dt to the collector/emitter of the IGBT when it is off, and those that do. Examples of the former are buck regulators and forward converters, where only one switch is employed or multiple switches are activated synchronously. High dv/dt is applied during the off-state in most bridge circuits such as inverters and motor controllers, when opposing devices are turned on. Simultaneous conduction of opposing devices can occur in such circuits, often with catastrophic results if proper gate drive and layout precautions are not followed. This behavior is caused by parasitic collector to gate (miller) capacitance, effectively forming a capacitive divider with the gate to emitter capacitance and thus inducing a gate to emitter voltage as illustrated in figure 1.

When high off-state dv/dt is not present, the IGBT can be driven like a MOSFET using any of the gate drive circuits in the UC37XX family as well as from the drivers internal to many switching power supply controllers. Normally 15 volts is applied gate to emitter during the on-state to minimize saturation voltage. The gate resistor or gate drive current directly controls IGBT turn-on, however turn-off is partially governed by minority carrier behavior and is less effected by gate drive.

There are several techniques which can be employed to eliminate simultaneous conduction when high off-state dv/dt is present. The most important technique, which should always be employed, is a Kelvin connection between the IGBT emitter and the driver's ground. High di/dt present in the emitter circuit can cause substantial transient voltages to develop in the gate drive circuit if it is not properly referenced. The Kelvin drive connection also minimizes the effective driver impedance for maximum attenuation of the dv/dt induced gate voltage. This requirement adds complication to driving multiple ground referenced IGBTs due to finite ground circuit impedance. Substantial voltages may develop across the ground impedance during switching, requiring level shift or isolation circuitry at the command signal to allow Kelvin drive circuit connections.

Bipolar Gate Driver

A Kelvin connected unipolar driver may often be adequate at lower switching speeds, however negative gate bias must be applied during the off-state to utilize the IGBT at higher rates. This becomes apparent when one considers that the gate to emitter threshold voltage drops to approximately 1.4 volts at high temperature. With high dv/dt at the collector, a very low and impractical drive

impedance is required to assure that the device remains off. By utilizing a negative turn-off bias, an adequate voltage margin is easily achieved, allowing the use of a more practical gate drive impedance. Fortunately most gate drivers have sufficient voltage capability to be used with bipolar

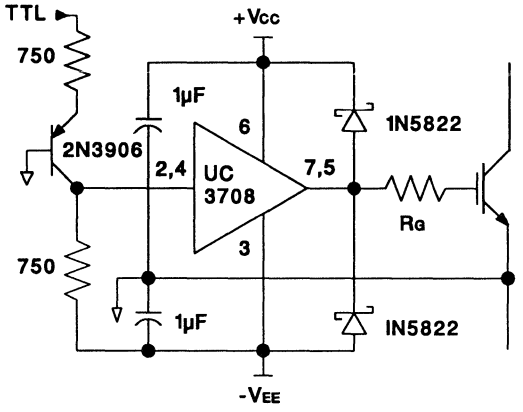

Figure 2. Bipolar IGBT gate drive using the U3708

power supplies. The UC3708 shown in figure 2 can deliver up to 6 amps peak with both output's paralleled, and is particularly suited to driving IGBTs. For added reliability during power sequencing, its output's "self bias", actively sinking current when insufficient supply voltage is present. The positive supply,+Vcc, is normally 15 to 16 volts and the negative supply, -VEE, typically ranges between -5 and -15 volts depending on circuit conditions. A PNP level shift circuit references the drive signal to ground. Opto-couplers are also commonly employed, and may be interfaced directly to the gate driver by referencing the signal to the negative supply. Note that this is a very demanding application for optocouplers, and only devices rated for high CMRR should be used.

Isolated Gate Driver

A bipolar IGBT gate driver with over-current protection can be implemented using the UC3724/UC3725 isolated gate driver pair as shown in figure 3. The UC3724/UC3725 transmits both power and signal across a small pulse transformer, thereby achieving low cost, high voltage isolation. An additional transformer winding develops a negative voltage, providing a bipolar supply for the UC3708. The UC3724/UC3725 can also be used for circuits which do not require negative turn-off bias by simply eliminating the negative supply and external driver, and using the UC3725 to drive the IGBT gate directly. Application note U-127 covers the UC3724/UC3725 in depth.

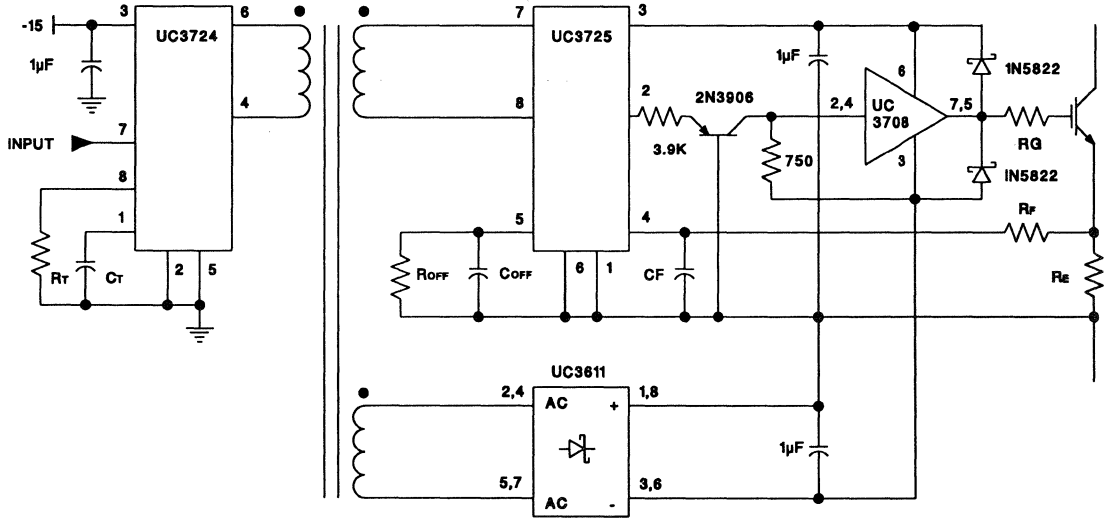

Figure 3. Power and signal are coupled to the UC3708 through the UC3724 / UC3725 Isolated Gate Driver Pair.

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Design Note

UC1525B/UC1527B DEVICES
Comparison Summary to UC1525A/27A Devices

The UC1525B and UC1527B devices are enhanced versions of the previous generation of UC1525A and UC1527A devices. They are pin-for-pin compatible and direct replacements for the "A" versions in almost all applications. Significnt improvements have been made in the 5.1V reference voltage and the output drivers as itemized in the tables below.

PARAMETER	NEW: UC1515B/27B	OLD: UC1525A/27A
REFERENCE VOLTAGE		
V_{REF} (min)	5.062 V	5.05 V
V_{REF} (max)	5.138 V	5.15 V
Line Regulation (max)	+/-10 mV	+/-20 mV
Load Regulation (max)	+/-15 mV	+/-50 mV
Temperature Stability (max)	+/-30 mV	+/-50 mV
Total Output Variation (max)	5.036 V to 5.164 V	5.00 V to 5.20V
Long Term Stability (max)	+/-10 mV	+/-50 mV
Temperature Coefficient (typ)	8 ppm/deg. C	
PWM OUTPUT SECTION		
Minimum On-Time (typ)	350 nS	600 nS
Cross Conduction	30 nC	150 nC
SUPPLY CURRENT		
ICC Increase (40 kHz to 400 kHz)	15 mA (max)	40 mA (typ)
ESD PROTECTION		
Discharge Withstand Voltage (typ)	2 kV (typ all pins)	no protection

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PWM OPERATION WITH LOW INPUT VOLTAGES

Bill Andreycak

Many of the PWM control ICs available today feature undervoltage lockout circuitry (UVLO) which requires minimum of 8 to 16 volts for turn-on to occur. This protection feature also makes them unsuitable for many low input voltage, or battery powered applications. A few of the mature ICs, however, can be "tricked" into operation by simply overriding their undervoltage lockout protection. The list includes the UC494A, UC1524 (non A), UC1526A, UC1841 and UC1851 PWM controllers.

5 VOLT INPUT PWM OPERATION

These devices relied primarily on the reference voltage (VREF) to be within its normal operating range to determine UVLO. Whenever the input voltage (VIN) is too low, the reference voltage, derived from the input, would also be too low. These devices can be brought into operation by pulling VREF, VIN and VC (or collector supplies) above approximately 4.7 volts. Operation from a fixed 5 volt input supply can be achieved with a slight degradation of performance.

A simple modification to this technique will allow operation with a variable low voltage DC input. A limiter circuit shown in figure 2 pulls VREF up to VCC when the input voltage is below about 5.5 volts. This circuitry then breaks the connection allowing Vcc to rise without pulling VREF any higher. This is necessary to prevent VREF from exceeding its maximum rating of about 6 volts. Most of the PWMs listed will supply adequate bias to VREF with VCC above 6 volts. The limiter circuit can be modified to accommodate each individual controller and application, typically by adjusting the 20 K ohm base-to-emitter resistor. Another choice to the list of PWMs is the UC1860 controller which is fully functional at an input of 5 volts. This high speed device features operation to 3 MHz with dual 2 amp peak outputs. Although intended for variable frequency resonant mode conversion, it can be operated at a fixed frequency and pulse width modulated. (END)

VREF LIMITER CIRCUIT

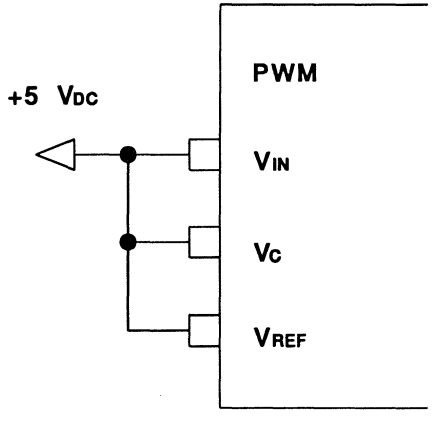

Figure 1.

VREF LIMITER CIRCUIT

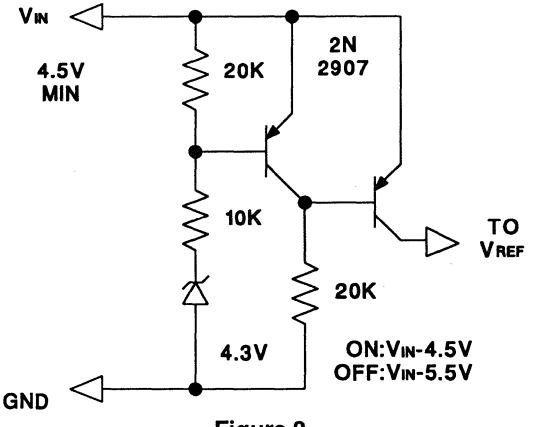

Figure 2.

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UNIQUE "CHEAP AND DIRTY" CONVERTER FOR LOW POWER BIAS SUPPLIES

Bill Andreycak

Regulated output voltage is obtained - regardless of input voltage

Most power supply designs use PWM controller ICs and MOSFET switches which require 10 to 15 volt bias supplies for proper operation. A common application problem is to first generate an auxiliary supply within this range. Although simple in many applications, developing this supply with a variable low voltage input can be challenging especially when the input amplitude goes both below and above the desired output voltage. The circuit shown below is a unique, inexpensive solution to this problem.

Basically, the topology is a two transistor flyback (buck-boost) converter which provides a noninverting output polarity. By varying the duty cycle, the output voltage can be either higher or lower than the input amplitude. This attribute makes this approach ideally suited for many widerange input or automotive applications. Likewise, this technique is equally applicable to power factor correction applications. Additionally, the inductor can be operated in either the continuous or discontinuous current modes.

BUCK-BOOST CONVERTER (2 XTOR)

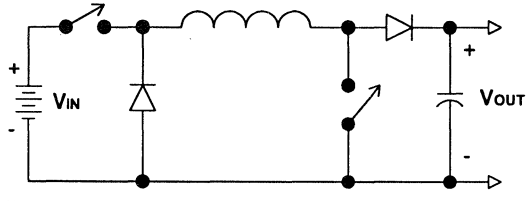

Figure 1.

Implementation of this technique will require a "high side" switch connected to the input voltage (VIN) and a low side switch to ground. Both of these are activated together, placing the inductor across the input supply while the switches are on. At turn off, the inductor is placed across the output capacitor and the two diodes conduct until the current reaches zero (discontinuous mode) or the next switching cycle is initiated (continuous mode). Inductor voltage and current waveforms are shown at maximum duty cycle for clarity.

INDUCTOR VOLTAGE AND CURRENT

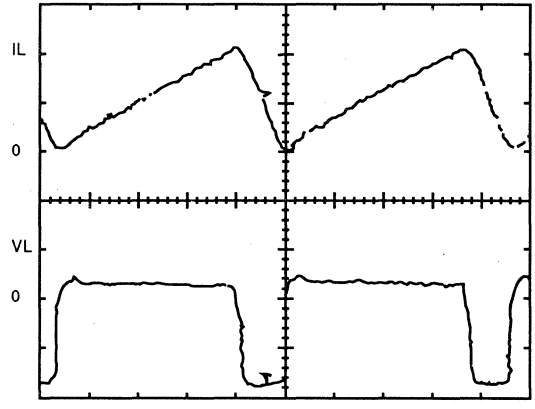

Figure 2.

At first, most PWM controllers may seem to be likely candidates for implementation of this technique. However, only one PWM features the ability to simultaneously switch both outputs together. The UC494A provides this operational mode by grounding its output control (O/C) input. Also limiting the IC selection is the fact that one IC output must go high and the other low each cycle. This is accomplished by connecting each of the UC494A's output collectors and emitters as required.

Switching at 200kHz in this application, the UC494A is programmed by a 9.1 K timing resistor (RT) and 470 pF capacitor (CT). High frequency conversion facilitates the use of a small (surface mount) inductor and output storage capacitor. Output voltage is regulated by using the ICs "A" amplifier as the voltage error amplifier. The 15 volt output is divided

down to 5 volts across the 15 K ohm resistor at pin 1 and compared to the reference voltage at pin 14. The 30K ohm resistor to Vout can be changed to provide different output voltages if required. Amplifier "B" is not used, but can be configured to provide overcurrent or overvoltage protection if desired. Schottky (1N5820) diodes are used in the power stage to maximize efficiency. Standard silicon diodes can be substituted in cost sensitive applications with some performance degradation. Efficiency for the 400 mW converter shown in figure 3 is approximately 50% for inputs between 7 and 16 volts and decreases slightly at higher and lower inputs. Consult Unitrode Design Note DN-37 for further information about 5 volt PWM operation.

BUCK BOOST CONVERTER USING THE UC 494A PWM CONTROLLER

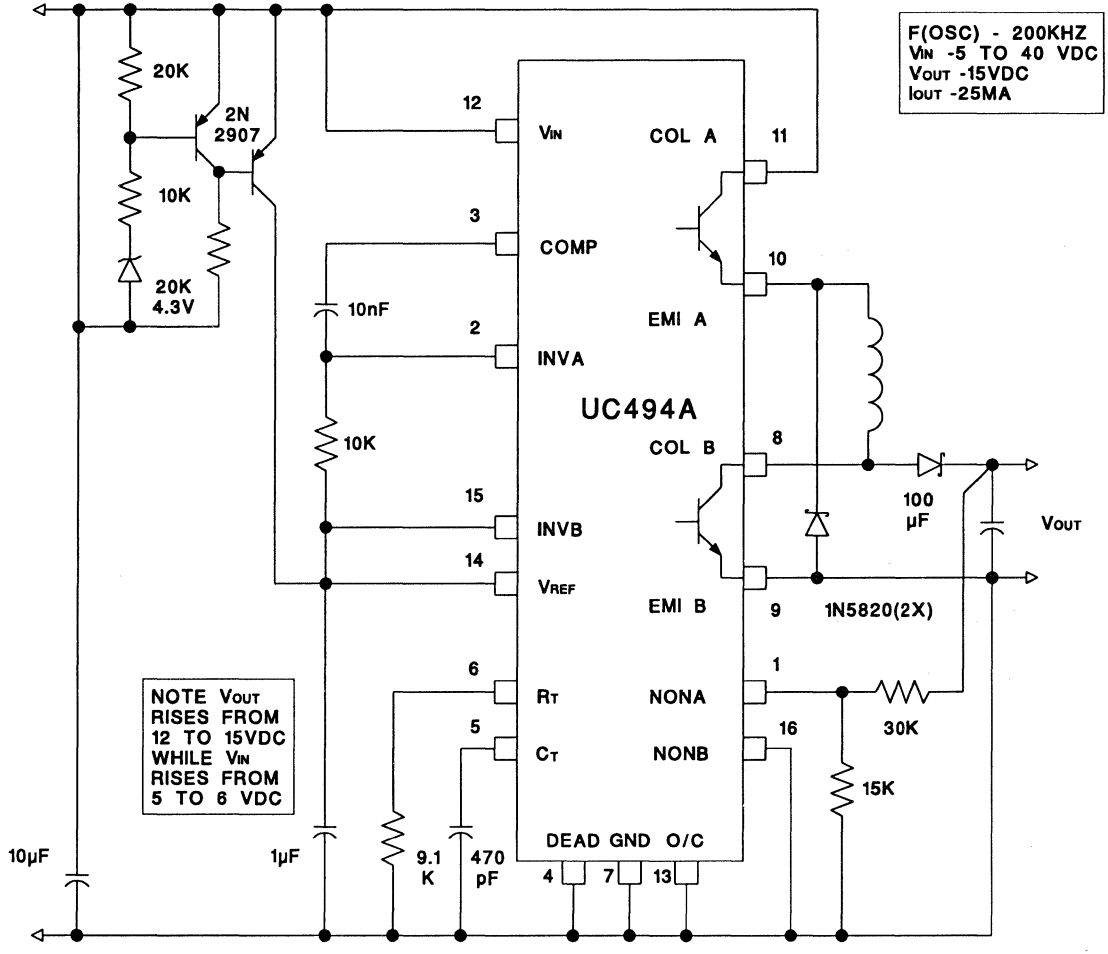

Figure 3.

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OPTIMIZING PERFORMANCE IN UC3854 POWER FACTOR CORRECTION APPLICATIONS

by Bill Andreycak

The performance of the UC3854 Power Factor Correction IC in the 250 watt application example has been evaluated using a precision PFC/THD instrument. The result was a power factor of 0.999 and Total Harmonic Distortion (THD) of 3.81%, measured to the 50th line frequency harmonic at nominal line and full load. Users should get similar results at these conditions. as well as over most line and load ranges. Summarized next are the circuit modifications which will improve the performance of most UC3854 PFC applications.

AMPLIFIER CLAMPS

There are a few ways to improve the obtainable power factor and performance in an application circuit. First, both the voltage and current amplifier outputs should have a "clamp" circuit to limit the output voltage swing and prevent saturation of the amplifier. Without the clamps, overshoot of the respective voltage or current loop could result thus degrading optimal performance. The current amplifier should be clamped with a 7.5 volt zener diode from the output (pin3) back to the inverting input ISENSE(pin4). Similarly, the voltage amplifier is clamped by installing a 1N4148 signal diode from its output (pin7) to the inverting input (pin11). Both examples are shown in figure 1. Each amplifier is self protected with internal current limiting, however the IC power consumption may increase during this interval.

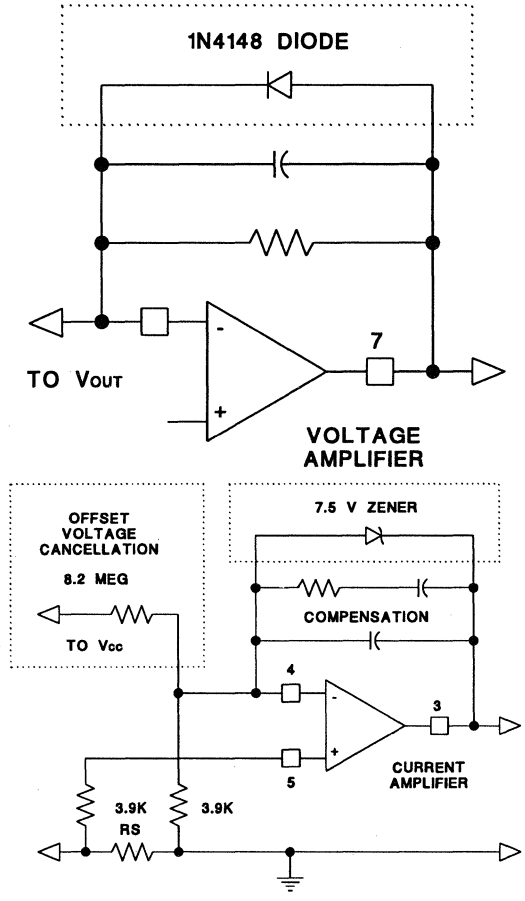


Figure 1.

CURRENT AMPLIFIER

OFFSET VOLTAGE CANCELLATION

The current amplifier maximum input offset voltage is specified as +/- 4 millivolts. Failing to accommodate the offset voltage can causes a spike in the leading edge of the line current following the zero voltage crossing. The spike will occur until the current amplifier comes out of saturation and then resumes normal operation. The worst case offset voltage can be canceled by adding a small current to the biasing resistor (R3) located from I SENSE (pin 4) to ground. This cancellation current (1.1μA), when multiplied by the bias resistor value (3.9K) should be designed to provide the four millivolt offset.

This offset cancellation current should be obtained from the UC3854 supply voltage. Although a constant current source is optimal, a resistor from Vcc to the I SENSE input will provide acceptable results as shown also in figure 1. An 8.2 megohm resistor will develop a 1.1 microamp current into the 3.9 K ohm resistor used in the design example. This will generate a 4.28 millivolt offset at the worst case of operation where Vcc is 9 volts. It is adviseable to generate this bias from Vcc and not the UC3854 reference which is inactive until the undervoltage lockout threshold is reached. Bias cancellation circuits from the reference could cause the current amplifier to saturate before the devices crosses its UVLO turn-on threshold. This condition will increase the start-up current of the UC3854 above its 2 milliamp specification and may prevent start-up in certain off-line applications.

CURRENT SENSE AMPLITUDE

The current sense signal should be made as high as possible, and a one volt full scale signal is recommended. Since resistive sensing can cause high power loss many users elect to generate only 100 to 200 millivolts at full load. In comparison, ground noise and slight amplifier offset voltages represent a higher percentage of the total current sense signal. Best results are obtained with the one volt (max) input and lower performance could be incurred with lower current sense signals. especially at light loads and high line voltages. Alternatives to resistive current sense are given below .

CURRENT SENSE TECHNIQUES

An optional technique to resistive current sensing should be considered to reduce power loss in the current sense circuitry. Two current sense transformers can be installed to sum both the switch and diode currents which will recreate the actual inductor current as shown in figure 2. These transformers must be designed to operate over the full range of duty cycles for the PFC converter design which approaches 100% as the line voltages nears zero.

Another current sensing option is to use a DC current sense module or transformer which is typically Hall Effect based. Two application concerns are the cost and accuracy of this technique which may limit its usage to only specialized applications.

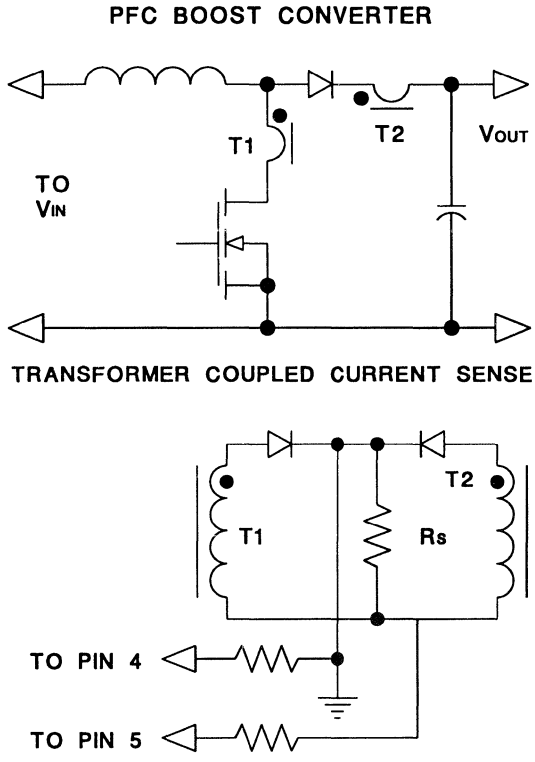
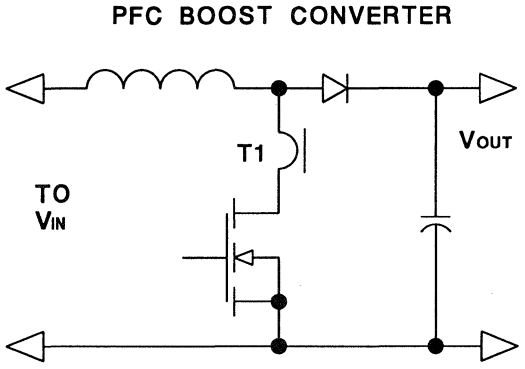


Figure 2.

A single current sense transformer in series with the PFC switch can also be used. This technique will require some additional circuitry to accurately reconstruct the primary current signal as shown in figure 3. Generating the inductor current signal while the switch is on is a simple task. The difficulty is in reconstructing the inductor current while the switch is off while no current is flowing in the current sense transformer.

Inductor current sensing can be simplified to use only one current sense transformer and a current sink circuit. The current sense signal is developed across resistor RI through diode DI while the switch is on. A second diode to the current sense transformer develops an identical voltage across capacitor CI as determined by the current sense resistor primary current and turns ratlo. When the PFC switch turns off capacitor CI maintains the peak amplitude of the previous current sense signal.

Charge is removed by an ideal current sink circuit which lowers the capacitor voltage linearly during one switching cycle. The current is scaled to discharge at the rate proportional to Vout minus



SINGLE TRANSFORMER CURRENT SENSE

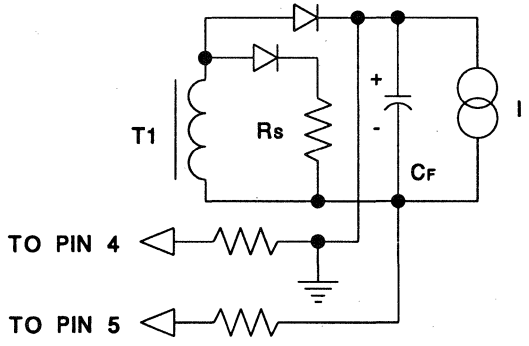


Figure 3.

Vin(t) divided by the inductor value, L. The input voltage (Vin) is constantly varying throughout the AC line cycle and so must the capacitor discharge current.

The circuitry shown in figure 4 will modulate the current sink inversely with the instantaneous line voltage. This will result in the correct discharge of capacitor C1 to reconstruct the actual inductor current. Polarity has been optimized for use with the UC3854 which requires a current sense signal below the ground reference. Another option is to develop a few volts of current sense signal to improve noise immunity and resistively divide this down to the one volt maximum input to the UC3854 controller.

Transistors QI through Q4 should be identical for best results. Transistors QI and Q3 are for temperature compensation of the base emitter

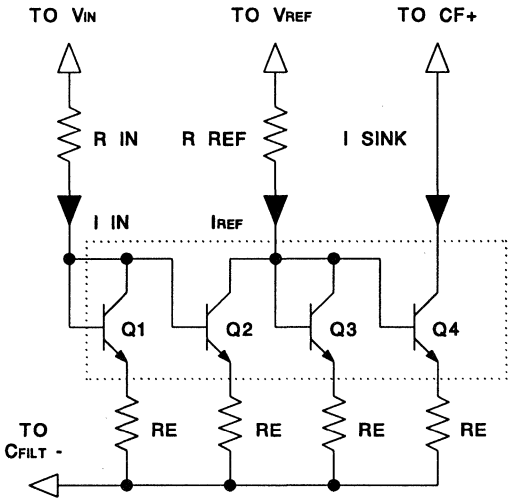
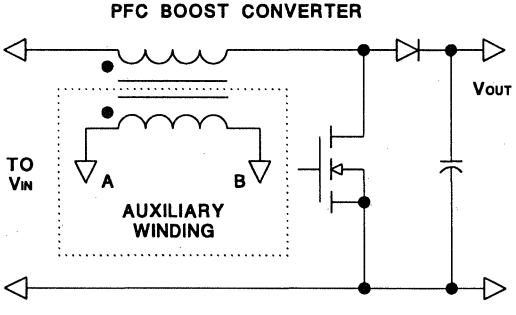


Figure 4.

junctions of Q2 and Q3. Emitter ballasting (50 to 100 mV) will also improve performance. The emitter currents of QI and Q2 should be similar and equal to Vin/Rin. This current is diverted away from the bases of Q3 and Q4 which limits the total range of sink current to the current sense filter capacitor, CFILT.

SCHOTTKY PROTECTION DIODES

Each pin of the UC3854 must be protected from negative voltages exceeding minus three hundred millivolts (-0.3V) maximum. In most applications, only three pins of the IC need external protection Schottky diodes. The gate drive output (pin 16) requires a 1N5820 3 amp Schottky diode to protect against parasitic inductive effects with high speed switching. The multiplier output (pin 5) and peak current limit (pin 2) need Schottky diode protection during abnormal overcurrent conditions and during the initial inrush currents upon power-up. A 1N5817 Schottky diode will provide adequate clamping since



REGULATED AUXILIARY BIAS

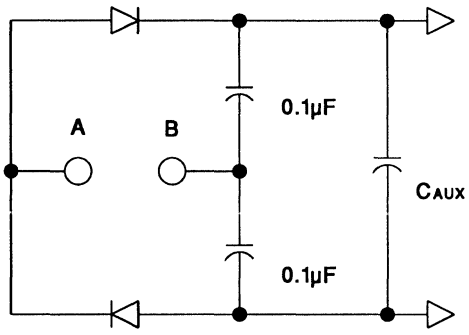


Figure 5.

the currents are low due to series resistors to the current sense circuitry.

REGULATED AUXILIARY SUPPLY

A secondary winding on the PFC boost inductor can be used to deliver a regulated auxiliary bias supply with few external components as shown in figure 5. Unlike more conventional and unregulated single diode or bridge rectifier techniques, this approach uses two diodes in a full wave configuration.

This arrangement develops two separate voltages across capacitors C1 and C2 each with 120 Hz components. However, when these two are summed at capacitor C3, the line variations are canceled, and a regulated auxiliary bias is obtained. The number of turns on the secondary winding will adjust the bias supply voltage. Additional windings on the boost inductor with similar rectification and filter circuitry can be used to deliver other semi-regulated isolated outputs.

UC 3854 POWER FACTOR CORRECTION EVALUATION KIT

LIST OF COMPONENTS

CAPACITORS (25 VDC)
C1 = 0.47 µF/250 VAC
C2 = 450 µF/450 VDC
C3 = 270 pF
C4 = 1 µF
C5 = NOT USED
C6 = 47 nF
C7 = 0.47 µF
C8 = NOT USED
C9 = 100 mF
C10 = 10 nF
C11 = 1 nF
C12 = 0.1 µF
C13 = 62 pF
C14 = NOT USED
C15 = 620 pF
C16 = 1 µF

DIODES
D1 =4 AMP/800VDC BRIDGE
D2 = UHVP806 FAST RECOVERY
D3 = 18 V ZENER
D4 = 1N5821 SCHOTTKY 3A
D5 = 1N4148
D6 = 1 AMP/100V BRIDGE
D7 = 1N5817 Schottky
D8 = 1N5817 Schottky

FUSE
F1 - 6A/250VAC FUSE

INDUCTOR
L1 = 1 milliHenry Inductor

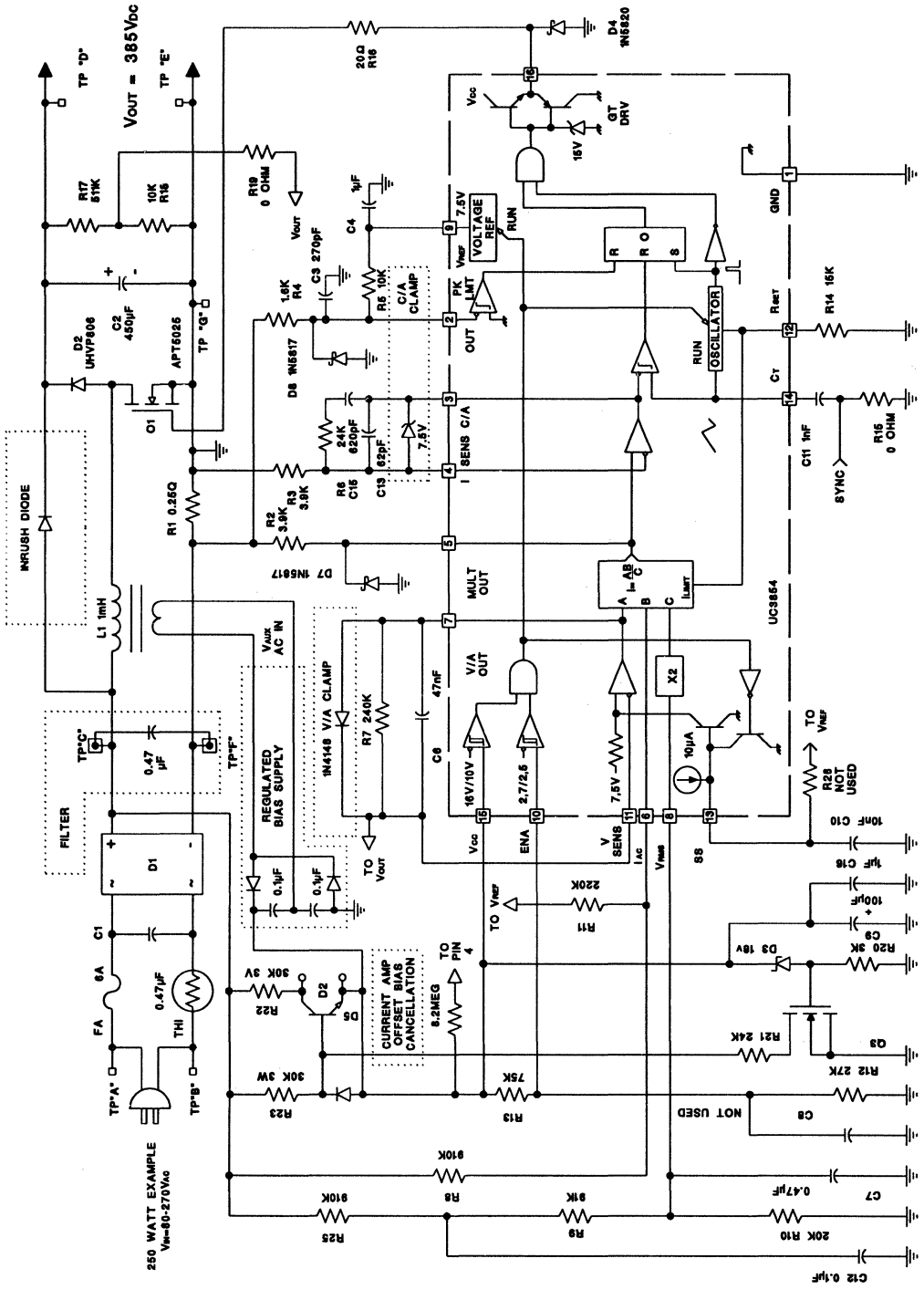
TRANSISTORS
Q1 = 500V/0.25 ohm NMOS FET
Q2 = 450V/0.5A NPN
Q3 = 50V/.5A NMOS FET

RESISTORS (1/2 WATT)
R1 - 0.25 ohm/5 WATT
R2 = 3.9 K
R3 = 3.9 K
R4 = 1.6 K
R5 = 10 K
R6 = 24 K
R7 =240 K
R8 = 910 K (400V)
R9 = 91 K
R10 = 20 K
R11 = 220 K
R12 = 27 K
R13 = 75 K
R15 = ZERO ohm
R20 = 3 K
R21 = 24 K
R22 = 30 K/3W
R23 = 470 K
R24 = USER SPECIFIED
R25 = 910 K (400V)
R26 = NOT USED (OPEN)

THERMISTOR
TH1 = ohm NTC

INTEGRATED CIRCUIT
U1 = UC3851 PFC CONTROLLER

UC3854 Evaluation PC Board Schematic
250 Watt Power Factor Correction Application



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THE EFFECTS OF OSCILLATOR DISCHARGE CURRENT VARIATIONS ON MAXIMUM DUTY CYCLE AND FREQUENCY IN UC3842 AND UC3842–"A" PWM ICs

by YEAM CHONG HOCK

Many designers try to program a precise maximum duty cycle and operating frequency by careful selection of the oscillator timing components, Rt and Ct. Because of the variations in oscillator discharge current, very accurate programming is not easily obtainable. However, it is possible with ICs which contain a "trimmed" discharge current which has specified limits. This Design Note will detail programming frequency and maximum duty cycle with both types of oscillators. Simplified equations will be used to develop obtainable ranges for these parameters over IC tolerances.

ON-TIME

Maximum on-time directly corresponds to the maximum charging time of the timing capacitor. Charging time (Tc) is determined by the timing capacitor value (Ct), the charging current (IRt) and the voltage amplitude between the upper and lower oscillator thresholds.

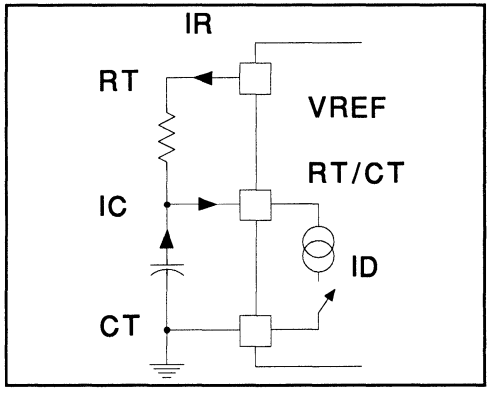

Figure 1: Basic UC3842 Oscillator Circuit

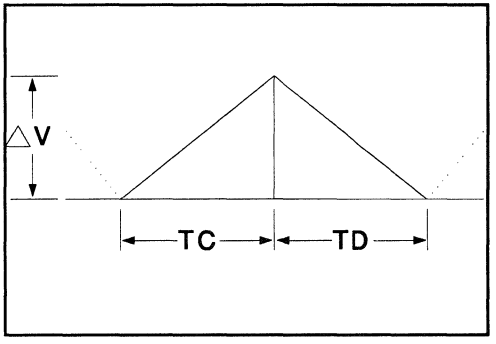

Figure 2: Timing Waveforms and Design Equations

OFF-TIME (DEADTIME)

The off-time occurs while the timing capacitor is discharged from the oscillator upper threshold to it lower threshold. The discharge current actuall sinks two currents to ground. One current is flowing from the discharging timing capacitor. Another current flows from the timing resistor (Rt) pulling to Vref. Therefore, the effective timing capacitor discharge current (ICt) is the ICs discharge current (Id) minus the timing resistor charging current (IRt). Maximum duty cycle and switching frequency can be controlled by accurately setting the ratio of

these currents and capacitor value. The related equations are listed below.

CHARGING :

$ICt = C \times \frac{dV}{Tc}$ ICt = C * dV / Tc

$ICt = \frac{5V}{Rt}$ (*approximation*)

$TC = c \times \frac{dV}{IRt}$

DISCHARGING :

$ICt = Id - IRt$

$Td = c \times \frac{dv}{(IRt - Id)}$

$Td = \frac{(Id - IRt)}{Id}$

DUTY CYCLE :

$D = \frac{Tc}{(Tc + Td)}$

$D = \frac{(Id - Rt)}{Id}$

SWITCHING FREQUENCY :

$F = \frac{1}{Tper} = \frac{1}{(Tc + Td)}$

$F = \frac{(Id - IRt)}{(Id \times Tc)}$

EXAMPLE 1:

This example will calculate the potential variations in maximum duty cycle and frequency using a standard UC3842 device. A ten milliamp internal discharge current (Id = 10mA) will be used for initial programming. The worst case limits of 6 and 14 milliamp discharge currents will be used to analyze the possible variations. A target of 100kHz at 60% duty cycle will be used.

$Id = 10mA$ (*typical*)

Id (min) = $6ma$, Id (max) = $14ma$

F (*typ*) = $100kHz$

$D = 0.60$ (60%)

Based on the 10 mA discharging current and the equations previously mentioned;

$IRt = 4mA$, and $Tc = 6us$

Using the same Rt and Ct values with a discharge current of 6 mA results in :

$Dmax = 0.33$ (30%)

$F = 55kHz$

When the highest discharge current of 14 mA is used, the results are :

$Dmax = 0.71$ (71%)

$F = 118kHz$

Therefore, the total possible range due to discharge current variations in maximum duty cycle and frequency is :

$Dmax = 33\ 71$ *percent*

$Frequency = 55\ 188kHz$

In most applications this range is far too wide to use in a high volume production environment. One technique to minimize the effects of the discharge current is to have the ICs sorted into different groups. Each group can have a tight distribution or tolerance and will use a specific timing resistor and capacitor to achieve the desired frequency and duty cycle. Each other group will also need a specific Rt and Ct fro that group. Keeping these groups seperated can create problems in some production situations. One alternative is to have the ICs measured and "binned" at the factory. Another way is to use only ICs within one distribution group, for example, 10 mA +/- 1 mA. Listed below is a general procedure to follow with grouped parts.

1. Sort ICs by discharge current range
ex: 7mA +/- 1 mA (6 - 8 mA total)

2. Select Rt and Ct using previous equations and worst case conditions.

Table 1 shows the results of selecting ICs by discharge current. The oscillator was programmed not to exceed 100 kHz and 60% maximum duty cycle.

I Discharge (+/- 1mA)	Rt (k)	Ct (nF)	Minimum Duty%	Maximum Duty%	Minimum Freq (kHz)	Maximum Freq (kHz)
7mA	1.56	11.3	47	60	77.8	100
9mA	1.25	14.1	50	60	83.3	100
11mA	1.04	16.9	52	60	86.7	100

TRIMMED DISCHARGE CURRENT

Very repeatable and predictable high volume prouduction can be rescued from these variations by using the right IC, one with a trimmed discharge current. The UC3842A, UC3843A, UC3844A and UC3845A devices have an internal factory trimmed discharge current with a tight distribution. This is set at 8.3 mA typically, and can only vary between a low of 7.5 mA and a high of 8.8 mA. Programming these ICs for a 50% maximum duty cycle and 100 kHz switching frequency will result in worst case variations of :

$D(\min) = 56\%$

$D(\max) = 62\%$

$F(\min) = 92.9kHz$

$F(\max) = 103.8kHz$

This is a significant improvement over the non "A" version devices. The accuracy of these ICs will improve when these ICs are used at wider maximum duty cycles, for example 65 to 85 percent. The UC3844A and UC3845A are intended for 50% maximum duty cycle applications and contain a flip flop to insure that 50% D(max) is never exceeded. The UC3842A and UC3843A have maximum duty cycles near 100% and can be adjusted lower using the appropriate Rt and Ct components.

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EXTEND CURRENT TRANSFORMER RANGE

by PHILIP C. TODD

Transformers are used extensively for current sensing because they can monitor currents with very low power loss and they have wide bandwidth for good waveform fidelity. Current transformers perform well in applications with symmetrical AC currents such as push-pull or full bridge converter topologies. In single-ended applications, especially boost converters, problems can arise because of the need to accurately reproduce high duty factor, unipolar, waveforms. Unipolar pulses may saturate the current transformer and, if this happens, over current protection will be lost and, for current mode control, regulation will be lost and an over voltage condition will result.

The transformer core must be reset after each pulse so that the full range of the transformer will be available for the next pulse. Self reset of the current transformer is the most common techniques used but it has drawbacks. Self reset uses the energy stored in the current transformer core for reset and depends on the open circuit impedance of the current transformer to generate enough volt-seconds in a short period of time for reset. Current transformers operated above a 50% duty factor may not have enough stored energy to allow complete reset in the time available and this situation becomes worse as the duty factor approaches 100%.

The magnetizing inductance of the current transformer must be kept high because this determines the amount of droop the current waveform will exhibit over the pulse period. The higher the inductance the lower the droop will be. The waveform droop opposes slope compensation and should be kept to a minimum. High magnetizing inductance also means that the core stores very little energy which can be used to reset the core.

The current transformer turns ratio generally needs to be high to lower the power loss. The more turns put on the core, however, the greater the leakage inductance and the greater the parallel capacitance. The leakage inductance by itself is generally not a problem but it will limit the current rise and fall times. The parallel capacitance also limits the bandwidth of the current transformer but it is a greater problem during transformer reset. For the transformer to reset properly, all of the energy stored in the core must be removed. In self reset this energy must transfer from the magnetizing inductance to the parallel capacitance in a resonant manner. If the capacitance is too large, the resonant frequency will be too low and the magnetizing inductance will not be reset before the next pulse begins.

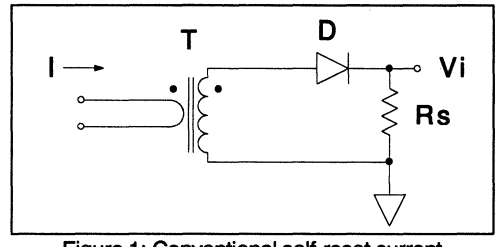

Figure 1: Conventional self-reset current transformer

Figure 1 shows a conventional current transformer circuit which uses self reset. The current I flowing in the primary, causes a current to flow through D and Rs to generate an output voltage proportional to Vc=IRs/N where N is the current transformer turns ratio. The problems discussed above occur during the reset interval when I=O. The core of T may not have enough energy to fully reset itself in the time available given the secondary capacitance of T plus the capacitance of D.

The problems with self reset of current transformers for unipolar pulse applications can be overcome with simple forced reset techniques derived from magnetic amplifiers. Duty factors above 90% are achievable with these techniques.

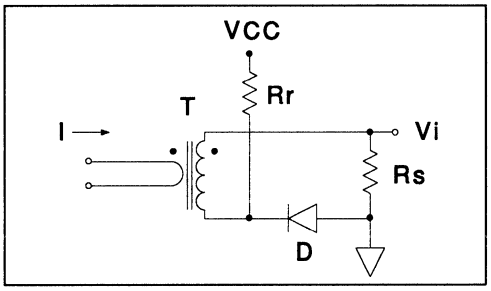

Figure 2: Current transformer with forced reset

Figure 2. shows the same circuit as Figure 1 configured for forced reset. The diode D has been moved from the high side of the transformer secondary winding to the ground side. This, of course, has no effect on the operation of the circuit and during the pulse this circuit behaves exactly as expected. During reset, however, Rr makes the circuit operation quite a bit different.

A current from Vcc through Rr can be much greater than the self reset current available from the magnetizing current of the transformer. This forcing current rapidly charges the parasitic capacitances and reverses the voltage on the secondary of the transformer. The applied volt-seconds can quickly reset the core so that high duty-factor operation is possible.

The forced reset may be high enough to drive the current transformer into saturation and this is an acceptable practice because the core will be saturated in the opposite direction (i.e. full reset) from the current pulse to be measured. This can be beneficial in some applications as it doubles the number of volt-seconds available from the transformer.

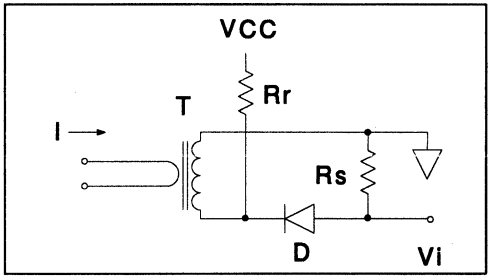

Figure 3: Negative output current sense

In some applications it may be desirable to generate a negative voltage from the current transformer. This can be accomplished without a negative voltage source to reset the transformer. Figure 3 shows the configuration. In this circuit there will be an error because the reset current subtracts from the sense current in Rs during the pulse. Care must be taken to minimize this effect.

There are other circuit configurations which are possible to force reset of the current transformer. Switches may be used to switch the reset current on and off. Additional windings or center tapped windings may be used also. Many circuits are possible and may provide a specific improvement at the expense of complexity. The circuits shown here are the simplest available and illustrate the basic concept.

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DESIGN CONSIDERATIONS FOR TRANSITIONING FROM UC3842 TO THE NEW UCC3802 FAMILY

John Gaumont

In an attempt to stay abreast of trends in the power supply marketplace, the Power Supply Design Engineer is perpetually seeking methods of improving upon existing designs. Requirements such as lower power for battery operated equipment, higher switching frequencies for reduced magnetics size, higher levels of circuit integration for improved reliability and lower cost have become necessities for survival.

The UCC3802 offers numerous advantages which allow the Power Supply Design Engineer to meet these challenging requirements. Features include:

- BI-CMOS Process
- Low Starting Supply Current: typically 100µA
- Low Operating Supply Current: typically 500µA
- Pin out Compatible with UC3842 and UC3842A families
- 5 Volt Operation (UCC3803, UCC3805)
- Leading Edge Blanking of Current Sense Signal
- On-Chip Soft Start
- Internal Full Cycle Restart Delay
- 1% Voltage Reference
- Up to 1 MHz Oscillator
- Self-Biasing Output Low During UVLO
- Very Few External Components Required
- 70ns Response from Current Sense to Output
- Available in Surface Mount or DIP Package

The UCC3802 family of devices are pin out compatible with the UC3842 and UC3842A families however, they are **NOT PLUG-IN COMPATIBLE.** In general, the UCC3802 requires fewer external components and consumes less operating current. The following UCC3802 family attributes should be considered **BEFORE** inserting the device into a UC3842/42A family socket:

1. Maximum supply voltage
2. Turn-on and Turn-off thresholds
3. Oscillator Rt, Ct values
4. Schottky diodes may not be required on output due to MOS body diode
5. No current sense filter required
6. No soft start circuitry required
7. Auxiliary power (bootstrap winding) may not be required

Detailed Pin By Pin Description

PIN 1 COMP--The UCC3802 has a true low output impedance error amplifier which both sources and sinks current. The error amplifier associated with the UC3842 family is an open collector in parallel with a current source. The UCC3802 has power-up soft start and fault soft start built on-chip with a fixed COMP rise time to 5V in 5ms. Therefore, **NO EXTERNAL SOFT START CIRCUITRY IS REQUIRED** saving 1 resistor, 1 capacitor, and 1 PNP transistor.

PIN 2 FB--The UCC3802 features a 2 MHz bandwidth error amplifier versus 1 MHz on the UC3842. Feedback techniques are identical to the UC3842 family. Stray capacitance on FB should be kept as small as possible, and the lead length as short as possible to achieve best stability.

PIN 3 CS--The UCC3802 current sense is significantly different from its predecessor. The UC3842 current sense input connects to only the PWM comparator. The UCC3802 Current Sense input connects to two comparators; the PWM comparator and the over-current comparator. Internal leading edge blanking masks the first 100ns of the current sense signal. This **MAY ELIMINATE THE NEED FOR AN RC CURRENT SENSE FILTER AND PREVENT FALSE TRIGGERING** due to leading edge noise. Connect CS directly to MOSFET source current sense resistor. The gain of the current sense amplifier on the UCC3802 family is typically 1.65 V/V versus typically 3 V/V with the UC3842 family.

PIN 4 RC--The UCC3802's oscillator allows for operation to 1 MHz versus 500KHz with the UC3842.

Both devices make use of an external resistor to set the charging current for the capacitor which determines the oscillator frequency. For the UCC3802 and UCC3804 F(Hz) = 1 .5/R(OHMS)C(F). For the UCC3803 and UCC3805 F(Hz)=1.0/R(OHMS)C(F). The two equations are different due to different reference voltages. The recommended range of timing resistor values is between 20K and 200K; the recommended range of timing capacitor values is between 100pF and 1000pF. The peak to peak amplitude of the oscillator waveform is 2.45 Volts versus 1.7 Volts. For best performance, keep the timing capacitor lead to GND as short as possible. Separate ground traces for the timing capacitor and all other pins are recommended. The maximum duty cycle for the UCC3802/03 is approximately 99%; the maximum duty cycle for the UCC3803/04 is approximately 49%. The duty cycle **CANNOT** be easily modified by adjusting the RT and CT pins, unlike the UC3842A family. The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor RT and the internal oscillator discharge transistor on-resistance, like the UC3842. However, maximum duty cycle limits less than 90% for the UCC3802/03 and less than 45% for the UCC3804/05 can not reliably be set in this manner.

PIN 5 GND--Both devices same.

PIN 6 OUT--The output of the UCC3802 is a CMOS output versus a Bipolar output on the UC3842. Peak output current remains the same +/- 1 Amp. The CMOS output provides very smooth rising and falling waveforms, with virtually no overshoot or undershoot. Additionally, the CMOS output provides a low resistance to the supply in response to overshoot, and a low resistance to ground in response to undershoot. Because of this, **SCHOTTKY DIODES MAY NOT BE NECESSARY** on the output. Furthermore, the UCC3802 has a self-biasing, active low output during UVLO. This feature **ELIMINATES THE GATE TO SOURCE 'BLEEDER' RESISTOR** associated with the MOSFET gate drive. Finally, **NO MOSFET GATE VOLTAGE CLAMP** is necessary with the UCC3802 as the on-chip zener diode automatically clamps the output to VCC.

PIN 7 VCC--The UCC3802 has a lower VCC (supply voltage) of 13.5 Volts typical versus 30 Volts on the

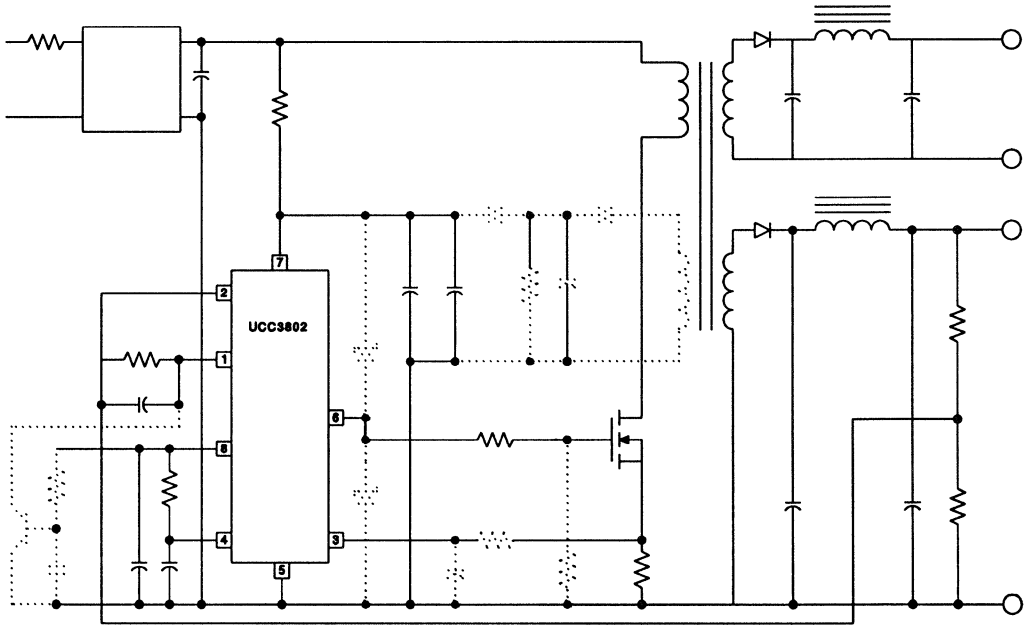

Figure 1

Figure 1 illustrates a nonisolated off-line flyback. Dotted components may be eliminated using the UCC3802 family.

UC3842. For applications which require a higher VCC voltage, a resistor must be placed in series with VCC to increase the source impedance. The maximum value of this resistor Rmax = (VIN(min)-VCC(max))/(ICC + (Qgate)(F)). Additionally, the UCC3802 has an on-chip zener diode to regulate VCC to 13.5 Volts. The turn-on and turn-off thresholds for the UCC3802 family are significantly different: 12.5V and 8V for the UCC3802 and UCC3804; 4.1 V and 3.6V for the UCC3803 and UCC3805. 5 Volt PWM operation is now possible. To ensure against noise related problems, filter VCC with an electrolytic and bypass with a ceramic capacitor to ground. Keep the capacitors close to the IC pins.

PIN 8 REF--The UCC3802 and UCC3804 have a 5 Volt reference. The UCC3803 and UCC3805 have a 4 Volt reference; both +/- 1% versus +/- 2% on the UC3842 family. The output short circuit current is lower...5mA versus 30mA. REF should be bypassed to ground with a ceramic capacitor to prevent noise problems. REF can be used as a logic output; as when VCC is lower than the UVLO threshold, REF is held low.

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