



**UM82C384
Memory Controller**

T-52-33-21

I General Description

The UM82C384 is one of UMC's High End AT (HEAT) Chip Set. It provides memory control functions which facilitate wide ranges of DRAM and CPU speed selections for 80386 AT system design.

II Features

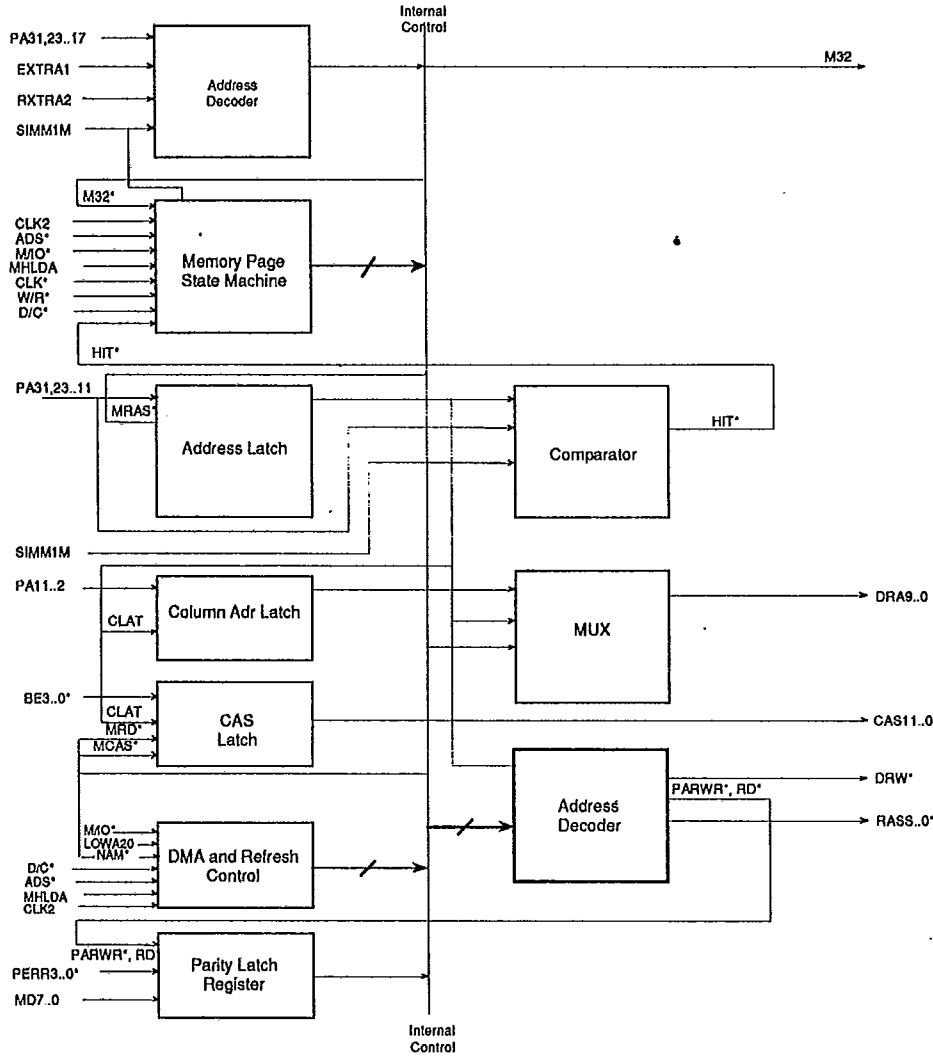
- Supports 16MHz, 20MHz and 25MHz Intel 80386
- Supports DRAM speed range from 60ns up to 120ns
- Supports 256K and 1M DRAM
- Supports up to 12M Bytes on board memory
- Using page mode DRAM to reduce wait states for same page memory access (hit)
- Relocates BIOS to high speed DRAM for very fast BIOS function calls
- 1.2 μ CMOS technology



UM82C384
Memory Controller

T-52-33-21

III Block Diagram



PC Mainboard

Figure 1. UM82C384 Block Diagram



UM82C384
Memory Controller

T-52-33-21

IV Pin Configuration

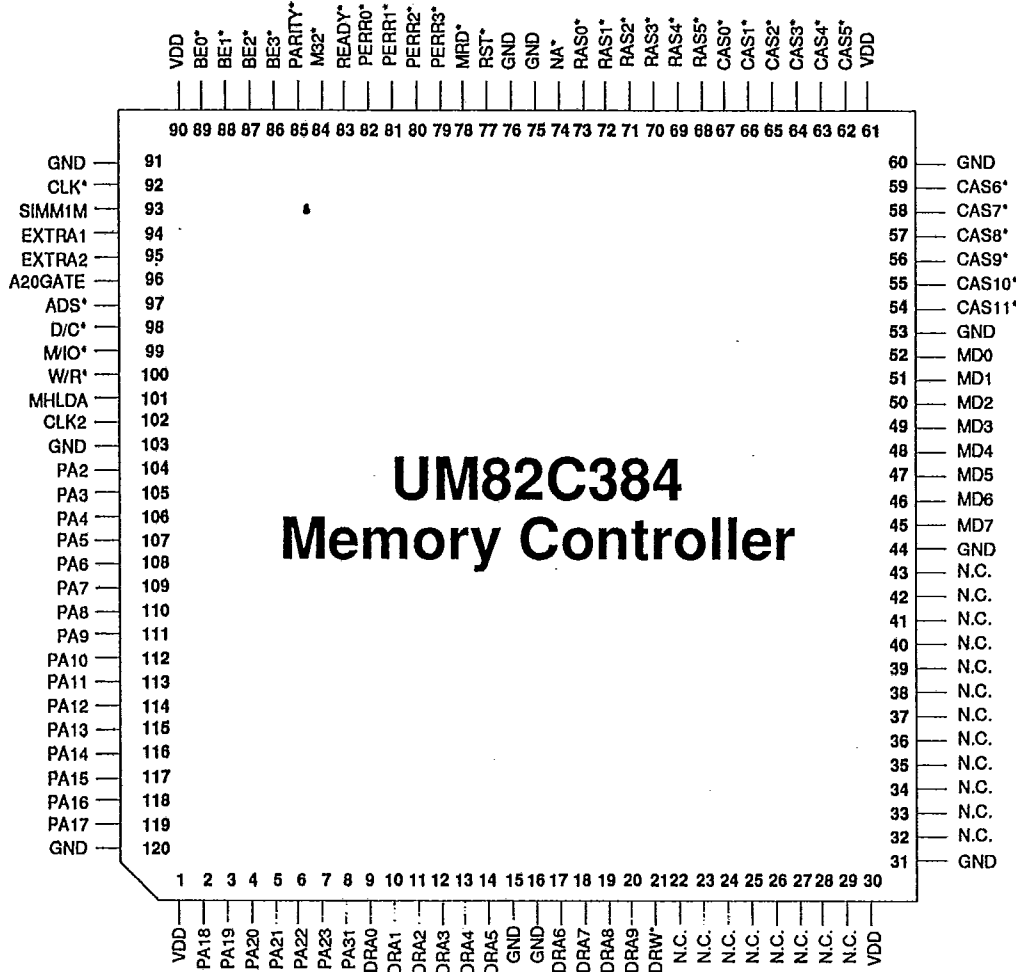


Figure 2. Pin Configuration



T-52-33-21

VI Functional Description

(a) Memory Mapping:

The memory mapping of UMC 386PC/AT chip set is shown in Figures 3 and 4. The 640 KB of base memory can execute existing MS-DOS applications developed for 80286-based product. On top of the base memory is 128KB video RAM, 64KB LIM pages and 128KB system BIOS. The extended memory can be 1M, 2M, 3M, 7M, and 11M bytes. The size of the memory is determined by SIMM1M, EXTRA1, and EXTRA2 as listed in table 2.

PC Mainboard

SIMM1M	EXTRA1	EXTRA2	System Memory	DRAM Type
0	0	0	1M	256K
0	1	0	2M	
0	1	1	3M	
1	0	0	4M	1M
1	1	0	8M	
1	1	1	12M	
0	0	1	*Illegal	
1	0	1		

Table 2



**UM82C384
Memory Controller**

T-52-33-21

	8XCOXXXX	RAM Diagnostic & Relocation Register	
		Not Used	
Bank 1	FFFFFF FA0000	Relocated BIOS	384K
		Not Used	
Bank 3	2FFFFFF 200000	2M - 3M	1M
Bank 2	1FFFFFF 100000	1M - 2M	1M
Bank 1	0FFFFFF 0E0000	System BIOS	128K
		128KB Video RAM & 64KB LIM Pages	
	09FFFF 000000	DOS Base Memory	640K

Figure 3. Memory Mapping when using 256K DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.



**UM82C384
Memory Controller**

T-52-33-21

	8XCOXXX	RAM Diagnostic & Relocation Register	
		Not Used	
Bank 1	FFFFFF FA0000	Relocated BIOS	384K
		Not Used	
Bank 3	8FFFFFF 800000	8M - 12M	4M
Bank 2	7FFFFFF 400000	4M - 8M	4M
Bank 1	3FFFFFF 100000	1M - 4M	3M
	0FFFFFF 0E0000	System BIOS	128K
		128KB Video RAM & 64KB LIM Pages	
	09FFFF 000000	DOS Base Memory	640K



Figure 4. Memory Mapping when using 1M DRAM. M32* is active in all regions except in regions marked "not used" and video RAM and LIM pages.



**UM82C384
Memory Controller**

T-52-33-21

(b) ROM Mapping:

Of the 384KB of memory addressed on top of the 16MB address space, the last 128KB has a special addressing feature. This 128-KB block, starting at address FE0000, can be relocated (mapped) via special hardware map registers to the system BIOS (0E0000 - 0FFFFFF). When mapped, the 128-KB RAM block normally located at FE0000 can be addressed at either FE0000 or 0E0000. The ROM devices are not accessible while the RAM is mapped to the address space normally occupied by the ROMs.

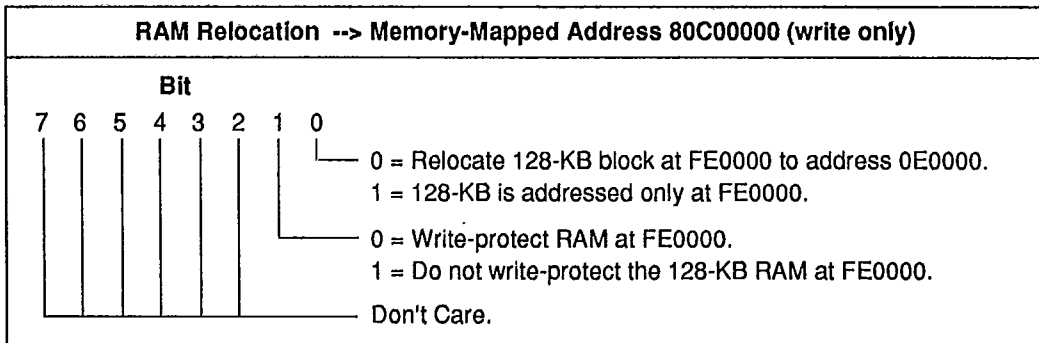
In addition to this relocation capability, the 128KB block of RAM beginning at address FE0000 can be write-protected by special hardware registers on the system memory board. The relocation and write-protection capabilities allow the system ROM to be replaced by high-speed RAM having the same contents (Shadow RAM).

(c) Memory Mapped Registers:

UM82C384 has two memory-mapped registers: one is used in RAM relocation, the other is for RAM diagnostics

RAM relocation:

The address and contents of the special memory-mapped hardware register used in the RAM relocation is shown in the following bit map. This register is a write-only register:





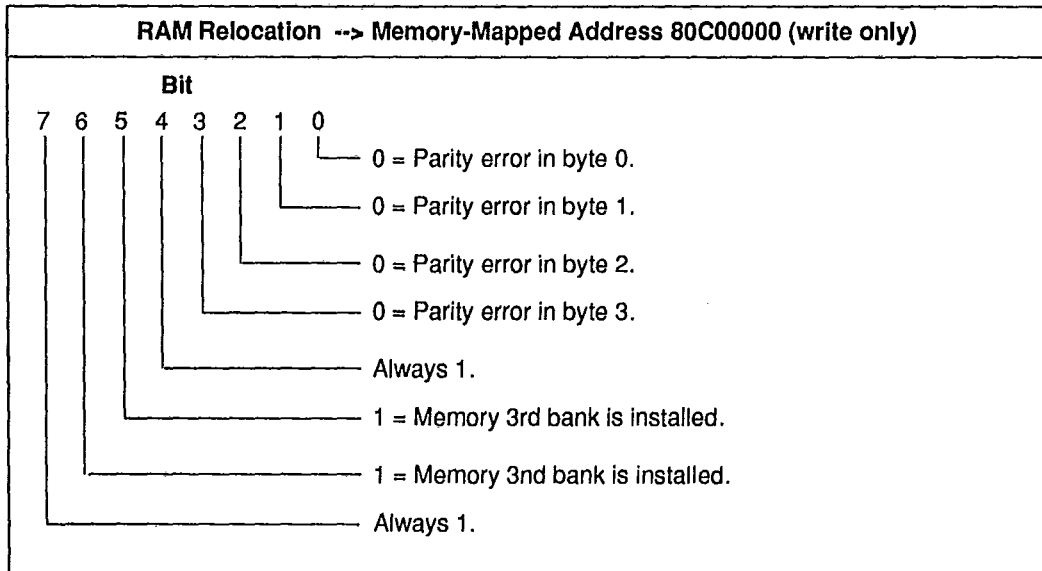
**UM82C384
Memory Controller**

T-52-33-21

PC Mainboard

RAM Diagnostics:

The RAM diagnostics register helps test the memory subsystems. This register allows a diagnostics program to read the state of memory configuration jumpers on the system memory board. The register also contains the status of the parity bits for each of the four bytes of a 32-bit memory access. RAMs can be tested very quickly, because they are performed by reading and writing 32-bit data patterns. When a parity error is detected, a diagnostics program uses the RAM diagnostics register to determine which byte in the 32-bit double-word caused the error. The address and contents of the memory-mapped diagnostics register are shown in the following bit map. This register is a read-only register. Writing to this register affects the contents of the RAM relocation register since they share the same memory location.





**UM82C384
Memory Controller**

T-52-33-21

(d) Bus Cycle Status Definitions

Table 3 gives the bus cycle status definition for the MHLDA, M/IO* D/C*, and W/R* signals:

MHLDA	M/IO*	D/C*	W/R*	Cycle Type
0	0	0	0	CPU Interrupt Acknowledge
0	0	0	1	Invalid Cycle Type
0	0	1	0	CPU I/O Read
0	0	1	1	CPU I/O Write
0	1	0	0	CPU Memory Instruction Prefetch Read
0	1	0	1	CPU Halt or Shutdown
0	1	1	0	CPU Memory Data Read
0	1	1	1	CPU Memory Data Write
1	0	0	0	Invalid Cycle type
1	0	0	1	DRAM Refresh - 3 (see note)
1	0	1	0	DMA Memory Write
1	0	1	1	DMA Memory Read
1	1	0	0	Invalid Cycle Type
1	1	0	1	DRAM Refresh - 2 (see note)
1	1	1	0	Non-CPU Cycle - Transition State
1	1	1	1	DRAM Refresh - 1 (see note)

Note: DRAM Refresh Cycles follow the following sequence:
1 → 2 → 3 → 2 → 1

Table 3



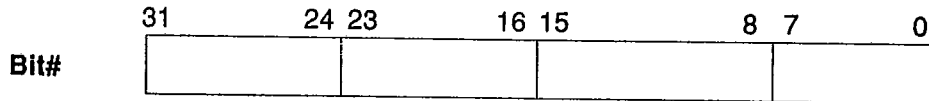
**UM82C384
Memory Controller**

T-52-33-21

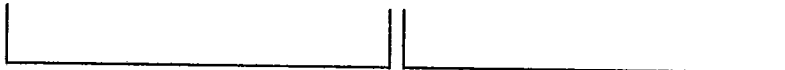
(e) RAS, CAS signals and DRAM Module

In order to reduce loading for RAS and CAS signals, six RAS signals and twelve CAS signals are generated to drive three banks of DRAMs. The following tables illustrate the connection of RAS and CAS signals to different banks of DRAMs.

Bank 1	RAS0*, RAS1*, CAS0* - CAS3*
Bank 2	RAS2*, RAS3*, CAS4* - CAS7*
Bank 3	RAS4*, RAS5*, CAS8* - CAS11*



Bank 1	CAS3*	CAS2*	CAS1*	CAS0*
Bank 2	CAS7*	CAS6*	CAS5*	CAS4*
Bank 3	CAS11*	CAS10*	CAS9*	CAS8*



Bank 1	RAS1*	RAS0*
Bank 2	RAS3*	RAS2*
Bank 3	RAS5*	RAS4*



**UM82C384
Memory Controller**

T-52-33-21

(f) DRAM Address corresponding to CPU Address

The following table illustrates the DRAM address corresponding to the CPU address when using 256K or 1M DRAM.

DRAM Address	256K DRAM		1M DRAM	
	Column	Row	Column	Row
- DRA0	PA2	PA12	PA2	PA12
- DRA1	PA3	PA13	PA3	PA13
- DRA2	PA4	PA14	PA4	PA14
- DRA3	PA5	PA15	PA5	PA15
- DRA4	PA6	PA16	PA6	PA16
- DRA5	PA7	PA17	PA7	PA17
- DRA6	PA8	PA18	PA8	PA18
- DRA7	PA9	PA19	PA9	PA19
DRA8	PA10	PA11	PA10	PA20
DRA9	0	0	PA11	PA21

Note: DRA0 - DRA7 are in opposite phase with the real CPU address.