TOSHIBA AMERICA, INC.

LOGIC
TC74HC SERIES

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October 1988

INTRODUCTION

During the last several years, the scale of integration of LSI's has increased rapidly. Because of this progress, heat radiation has become a big problem, similar to the way that bipolar LSI's have been struggling for many years, it is well known that only CMOS technology can reduce this problem. The use of CMOS technology has been increasing in the field of LSI's such as high performance microprocessors and large capacity memories. Additionally, high speed CMOS devices utilizing microlithography technology have been developed as general purpose logic IC's interfacing with these high performance LSI's.

Since the introduction of the TC74HCxxx series as a high speed CMOS logic family as a new generation in 1982, TOSHIBA has produced 176 type numbers to the present time for use a variety of applications. Because the 74HC series is a CMOS design, it is susceptible to latch-up; and because of a thin gate oxide structure, electrostatic discharge (ESD) is also a problem. TOSHIBA has been working on development of CMOS devices which overcome these problems.

In response to the latch-up and ESD issues, and, as a consequence of improvements in design rules and processes, TOSHIBA has revised the TC74HCxxx series and now produces the TC74HCxxxA series. This revision has ample capacity for handling ESD as well as the elimination of latch-up in normal applications. The TC74HCxxxA series also provides an increased speed of operation of 20% to 30% over the original series. The original TC74HCxxx series will be replaced with the "A" revision series which is upward compatible. Presently, TOSHIBA produces 100 TC74HCxxxA part types and will have more than 200 part types by the middle of 1989.

This book provides technical information on TOSHIBA's TC74HCxxxA series of high speed C^2MOS devices. In addition, this book contains technical information on TC74HCxxx products for which the "A" versions are still under development.

The information contained in this data book is subject to change without notice.

NOTE: TOSHIBA does not assume any responsibility for use of any circuity described; no circuit patent licenses are implied, and TOSHIBA reserves the right, at any time without notice, to change said circuitry.

CHANGE-OVER TO THE NEW ENHANCED VERSION
(Announce of the discontinuation of current products)

TOSHIBA has been producing 176 types of TC74HCxxx series since 1982 which are well accepted in the world-wide market place.

The last year, TOSHIBA started supplying a new enhanced version which is employed with refined design and process technologies resulting the higher performance of AC characteristics, ESDS, and reliability etc.

Now TOSHIBA recommends customers to replace the current version with the new enhanced version. Already 100 part-numbers of current 74HCxxx series are announced in July '88 to be discontinued at the end of March '89.

In this time period customers are kindly requested to change-over from the current version to the new enhanced version.

The new enhanced version is named TC74HCxxxA series available both in DIP and SOP which will surely, TOSHIBA believes, satisfy custom's requirement.

〔Maintenance-Discontinued TYPE LIST.〕

TYPE NO.	TYPE NO.	TYPE NO.	TYPE NO.	TYPE NO.
TC74HC 00P/F	TC74HC 77P/F	TC74HC 163P/F	TC74HC 283P/F	TC74HC 574P/F
02P/F	85P/F	164P/F	298P/F	595P
03P/F	109P/F	165P/F	299P	597P/F
04P/F	125P/F	166P/F	323P	640P/F
U04P/F	126P/F	174P/F	367P/F	T640P/F
T04P/F	131P/F	175P/F	368P/F	643P/F
08P/F	132P/F	238P/F	373P/F	T643P/F
10P/F	133P/F	240P/F	374P/F	646P
11P/F	137P/F	T240P/F	T374P/F	T646P
14P/F	138P/F	241P/F	375P/F	648P
TC74HC 20P/F	TC74HC T138P/F	TC74HC T241P	TC74HC 386P/F	TC74HC T648P
21P/F	139P/F	244P/F	390P/F	651P
27P/F	151P/F	T244P/F	393P/F	T651P
32P/F	154P	245P/F	533P/F	652P
42P/F	155P/F	T245P/F	534P/F	T652P
51P/F	157P/F	251P/F	540P/F	688P/F
73P/F	158P/F	257P/F	541P/F	4002P/F
74P/F	160P/F	258P/F	563P/F	4075P/F
75P/F	161P/F	273P/F	564P/F	T7007P/F
76P/F	162P	280P/F	573P/F	7266P/F

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	03AP/AF*	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	14	112
	04AP/AF*	HEX INVERTER	14	115
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	11AP/AF*	TRIPLE 3-INPUT AND GATE	14	130
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	20AP/AF*	DUAL 4-INPUT NAND GATE	14	136
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	574AP/AF	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	539
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	690P	DECADE COUNTER REGISTER (3-STATE)	20	615
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	692P	DECADE COUNTER REGISTER (3-STATE)	20	627
TC74HC	693P	4-BIT BINARY COUNTER REGISTER (3-STATE)	20	627
	696P	U/D DECADE COUNTER/REGISTER (3-STATE)	20	639
	697P	U/D 4-BIT BINARY CTR./REGISTER (3-STATE)	20	639
	698P	U/D DECADE COUNTER/REGISTER (3-STATE)	20	650
	699P	4-BIT BINARY CTR./REGISTER (3-STATE)	20	650
	4002AP/AF	DUAL 4-INPUT NOR GATE	14	662
	4016AP/AF	QUAD BILATERAL SWITCH	14	—
	4017P/F	DECADE COUNTER/DIVIDER	16	665
	4020P/F	14-STAGE BINARY COUNTER	16	671
	4022P/F	OCTAL COUNTER/DIVIDER	16	676
TC74HC	4024P/F	7-STAGE BINARY COUNTER	14	682
	4028P/F	BCD-TO-DECIMAL DECODER	16	687
	4040P/F	12-STAGE BINARY COUNTER	16	692
	4049P/F	HEX BUFFER (INV.)	16	697
	4050P/F	HEX BUFFER	16	697
	4051AP/AF	8-CHANNEL ANALOG MULTIPLEXER	16	701
	4052AP/AF	DUAL 4-CHANNEL ANALOG MULTIPLEXER	16	701
	4053AP/AF*	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	16	701
	4060P/F	14-STAGE BINARY COUNTER/OSCILATOR	16	708
	4066P/F	QUAD BILATERAL SWITCH	14	714
TC74HC	4072P/F	DUAL 4-INPUT OR GATE	14	719
	4075AP/AF	TRIPLE 3-INPUT OR GATE	14	723
	4078P/F	8-INPUT OR/NOR GATE	14	726
	4094P/F	8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)	16	730
	40102P	DUAL BCD PROGRAMMABLE DOWN COUNTER	16	737
	40103P	8-BIT BINARY PROGRAMMABLE DOWN COUNTER	16	737
	40105AP/AF	4 BITS×16 WORDS FIFO REGISTER	16	748
	4316AP	QUAD BILATERAL SWITCH	16	—
	4351AP	8-CHANNEL ANALOG MULTIPLEXER	20	—
	4352AP	DUAL 4-CHANNEL ANALOG MULTIPLEXER	20	—

Type Number		Function	Pin	Page
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	4514P	4-TO-16 LINE DECODER/LATCH	24	762
	4515P	4-TO-16 LINE DECODER/LATCH (INV.)	24	762
	4518P/F	DUAL DECADE COUNTER	16	767
	4520P/F	DUAL 4-BIT BINARY COUNTER	16	767
	4538P/F	DUAL MONOSTABLE MULTIVIBRATOR	16	774
	4543P/F	BCD TO 7 SEGMENT LATCH/DECODER/DRIVER	16	782
	T7007AP/AF	HEX BUFFER	14	788
	7240AP/AF	OCTAL BUS BUFFER (3-STATE/INV.)	20	—
TC74HC	7241AP/AF	OCTAL BUS BUFFER (3-STATE)	20	—
	7244AP/AF	OCTAL BUS BUFFER (3-STATE)	20	—
	7266AP/AF	QUAD EXCLUSIVE NOR GATE	14	423
	7292P	PROGRAMMABLE DIVIDER/TIMER	16	791
	7294P	PROGRAMMABLE DIVIDER/TIMER	16	791
	7640AP/AF	OCTAL BUS TRANSCEIVER (3-STATE/INV.)	20	—
	7643AP/AF	OCTAL BUS TRANSCEIVER (3-STATE)	20	—
	7645AP/AF	OCTAL BUS TRANSCEIVER (3-STATE)	20	—

- All DIP 24pin products service as enclosure of the narrow type (300mil)
- — denotes the products under development
- TOSHIBA is expanding the number of "A" series
- The type numbers marked * have "FN" product

2.HIGH SPEED CMOS SELECTION GUIDE

GATE	NAND		74HC00A 74HCT00A 74HC03A 74HC10A 74HC20A 74HC30 74HC132A 74HC133A
	NOR		74HC02A 74HCT02A 74HC27A 74HC4002A 74HC4078
	AND		74HC08A 74HCT08A 74HC09A 74HC11A 74HC21A
	OR		74HC32A 74HCT32A 74HC4072 74HC4075A 74HC4078
	INVERTER,BUFFER		74HC04A 74HCT04A 74HCU04A 74HC05A 74HC14A 74HC4049 74HC4050 74HCT7007A 74HC07A
	EXCLUSIVE OR/NOR		74HC86 74HCT86A 74HC266A 74HC386A 74HC7266A
	SCHMITT TRIGGER		74HC14A 74HC132A
	MULTI FUNCTION		74HC51A
	LEVEL SHIFTER		74HC4049 74HC4050
	BUS BUFFER		74HC125A 74HC126A 74HC240A 74HCT240A 74HC241A 74HCT241A 74HC244A 74HCT244A 74HC365 74HC366 74HC367A 74HC368A 74HC540A 74HCT540 74HC541A 74HCT541 74HC7240A 74HC7241A 74HC7244A
	BUS TRANSCEIVER		74HC242 74HC243 74HC245A 74HCT245A 74HC620 74HC623 74HC640A 74HCT640A 74HC643A 74HCT643A 74HC646A 74HCT646A 74HC648A 74HCT648A 74HC651A 74HCT651A 74HC652A 74HCT652A 74HC7640A 74HC7643A 74HC7645A
FLIP-FLOP	J-K FLIP-FLOP		74HC73A 74HC76A 74HC107 74HC109A 74HC112 74HC113
	D FLIP-FLOP		74HC74A 74HCT74A 74HC174A 74HC175A 74HC273A 74HC377 74HCT174
		3-STATE	74HC374A 74HCT374A 74HC534A 74HCT534A 74HC564A 74HCT564 74HC574A 74HCT574 74HC646A 74HCT646A 74HC648A 74HCT648A 74HC651A 74HCT651A 74HC652A 74HCT652A
LATCH			74HC75A 74HC77A 74HC259 74HC375A
		3-STATE	74HC373A 74HCT373 74HC533A 74HCT533 74HC563A 74HCT563 74HC573A 74HCT573
MULTI VIBRATOR			74HC123 74HC221 74HC423 74HC4538 74HC123A* 74HC221A* 74HC423A*
DECODER			74HC42A 74HC131A 74HC137A 74HCT137 74HC138A 74HCT138 74HC139A 74HC154A 74HC155A 74HC237 74HC238A 74HC4028 74HC4514 74HC4515
		7-SEGMENT	74HC4511 74HC4543
ENCODER			74HC147 74HC148
REGISTER			74HC164A 74HCT164A 74HC165A 74HC166A 74HC173 74HC194 74HC195 74HC299A 74HC323A 74HC595A 74HC597A 74HC4094
		MULTI PORT	74HC670
		FIFO	74HC40105A
COUNTER		BINARY	74HC161A 74HC163A 74HC191 74HC193 74HC393A 74HC590 74HC592 74HC593A 74HC691 74HC693 74HC697 74HC699 74HC4520
		DECADE	74HC160A 74HC162A 74HC190 74HC192 74HC390A 74HC690 74HC692 74HC696 74HC698 74HC4518
		DIVIDER	74HC4017 74HC4020 74HC4022 74HC4024 74HC4040 74HC4060 74HC40102 74HC40103 74HC7292 74HC7294
MULTIPLEXER		ANALOG	74HC4051A 74HC4052A 74HC4053A 74HC4351A 74HC4352A 74HC4353A
		DIGITAL	74HC151A 74HC153 74HC157A 74HCT157A 74HC158A 74HCT158A 74HC251A 74HC253 74HC257A 74HCT257 74HC258A 74HCT258A 74HC298A 74HC352A 74HC353A 74HC354 74HC356
ANALOG SWITCH			74HC4016 74HC4066 74HC4316A
COMPARATOR			74HC85A 74HC688A 74HCT688A
ADDER			74HC283A
ALU			74HC181 74HC182
PARITY TREE			74HC280A

Including under development type number

*)tw out=1.0•Cx•Rx

GATE

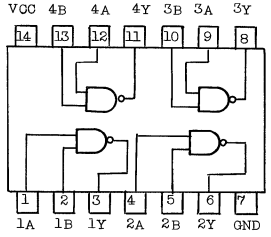
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 00	QUAD 2-INPUT NAND GATE	LS00	4011, 7400	14
74HC T00	QUAD 2-INPUT NAND GATE	LS00	4011, 7400	14
74HC 03	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	LS03	*40107,*5029	14
74HC 10	TRIPLE 3-INPUT NAND GATE	LS10	4023	14
74HC 20	DUAL 4-INPUT NAND GATE	LS20	4012	14
74HC 30	8-INPUT NAND GATE	LS30	4068	14
74HC 133	13-INPUT NAND GATE	LS133		16
74HC 02	QUAD 2-INPUT NOR GATE	LS02	4001	14
74HC T02	QUAD 2-INPUT NOR GATE	LS02	4001	14
74HC 27	TRIPLE 3-INPUT NOR GATE	LS27	4025,*4000	14
74HC4002	DUAL 4-INPUT NOR GATE	*LS25	4002	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 08	QUAD 2-INPUT AND GATE	LS08	4081	14
74HC T08	QUAD 2-INPUT AND GATE	LS08	4081	14
74HC 09	QUAD 2-INPUT AND GATE (OPEN DRAIN)	LS09	4081	14
74HC 11	TRIPLE 3-INPUT AND GATE	LS11	4073	14
74HC 21	DUAL 4-INPUT AND GATE	LS21	4082	14
74HC 32	QUAD 2-INPUT OR GATE	LS32	4071	14
74HC 32	QUAD 2-INPUT OR GATE	LS32	4071	14
74HC4075	TRIPLE 3-INPUT OR GATE		4075	14
74HC4072	DUAL 4-INPUT OR GATE		4072	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 04	HEX INVERTER	LS04	*4069U	14
74HC T04	HEX INVERTER	LS04	*4069U	14
74HC U04	HEX INVERTER (SINGLE STAGE)	*LS04	4069U,7404U	14
74HC 05	HEX INVERTER (OPEN DRAIN)	*LS04	*4069U	14
74HC 51	DUAL 2W-2I AND/OR INVERT GATE	LS51	*4085	14
74HC 86	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC T86	QUAD EXCLUSIVE OR GATE	LS88,LS386	4030	14
74HC 266	QUAD EXCLUSIVE NOR GATE (OPEN DRAIN)	LS266	4077	14
74HC7266	QUAD EXCLUSIVE NOR GATE	*LS266	4077	14
74HC 386	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC 14	HEX SCHMITT INVERTER	LS14	4584	14
74HC 132	QUAD 2-INPUT SCHMITT NAND	LS132	4093	14

* Suggested alternative

GATE

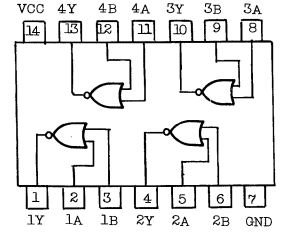
QUAD 2-INPUT NAND GATE

00
T00 Positive logic : $Y = \overline{AB}$



QUAD 2-INPUT NOR GATE

02
T02 Positive logic : $Y = \overline{A+B}$

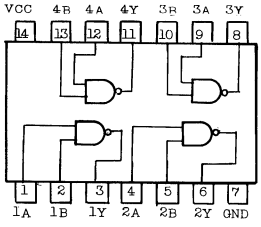


GATE (Continued)

QUAD 2-INPUT NAND GATE WITH OPEN DRAIN OUTPUT

03

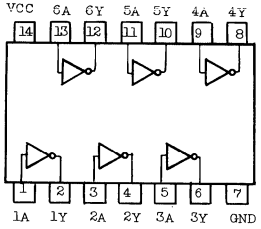
Positive logic: $Y = \overline{AB}$



HEX INVERTER

04 05
T04
U04

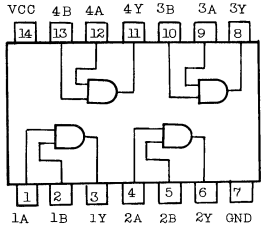
Positive logic: $Y = \overline{A}$



QUAD 2-INPUT AND GATE

08 09
T08

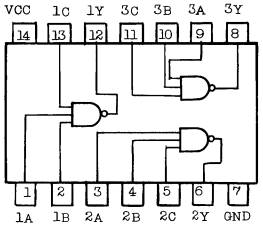
Positive logic: $Y = AB$



TRIPLE 3-INPUT NAND GATE

10

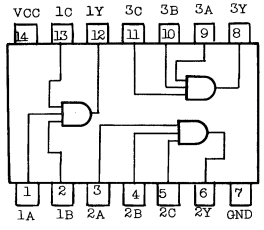
Positive logic: $Y = \overline{ABC}$



TRIPLE 3-INPUT AND GATE

11

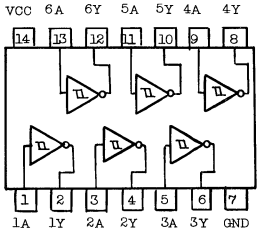
Positive logic: $Y = ABC$



HEX SCHMITT INVERTER

14

Positive logic: $Y = \overline{A}$

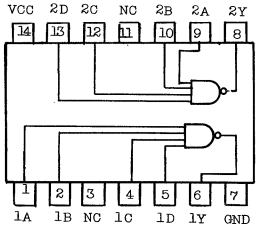


GATE (Continued)

DUAL 4-INPUT NAND GATE

20

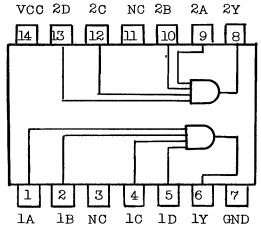
Positive logic: $Y = \overline{ABCD}$



DUAL 4-INPUT AND GATE

21

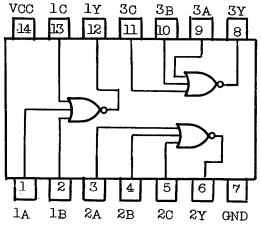
Positive logic: $Y = ABCD$



TRIPLE 3-INPUT NOR GATE

27

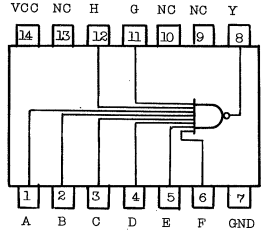
Positive logic: $Y = \overline{A+B+C}$



8-INPUT NAND GATE

30

Positive logic: $Y = \overline{ABCDEFGH}$

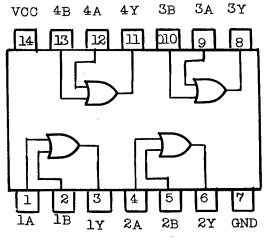


QUAD 2-INPUT OR GATE

32

T32

Positive logic: $Y = A+B$

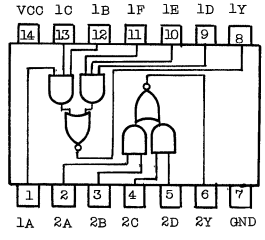


DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

51

Positive logic: $1Y=\overline{1A \cdot 1B \cdot 1C+1D \cdot 1E \cdot 1F}$

$2Y=\overline{2A \cdot 2B+2C \cdot 2D}$



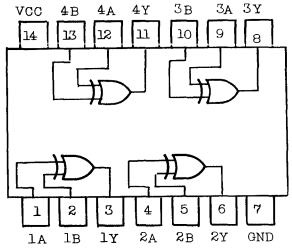
GATE (Continued)

QUAD 2-INPUT EXCLUSIVE-OR GATE

86

T86

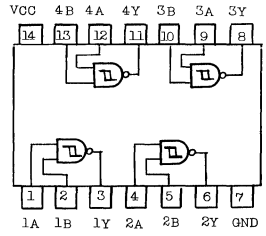
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



QUAD 2-INPUT SCHMITT NAND GATE

132

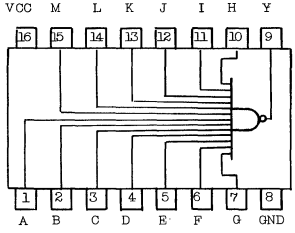
Positive logic: $Y=\overline{AB}$



13-INPUT NAND GATE

133

Positive logic: $Y=\overline{ABCDEFGHIJKLM}$

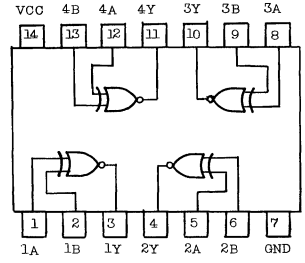


QUAD 2-INPUT EXCLUSIVE-NOR GATE

266

7266

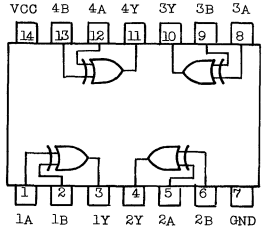
Positive logic: $Y=\overline{A\oplus B}=AB+\overline{A}\overline{B}$



QUAD 2-INPUT EXCLUSIVE-OR GATE

386

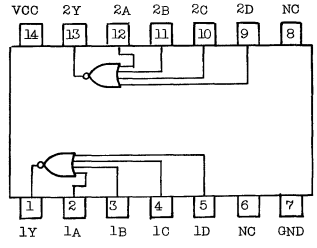
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



DUAL 4-INPUT NOR GATE

4002

Positive logic: $Y=\overline{A+B+C+D}$

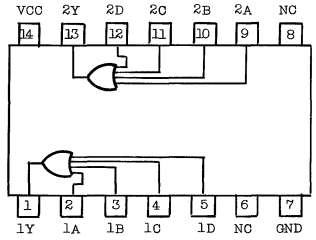


GATE (Continued)

DUAL 4-INPUT OR GATE

4072

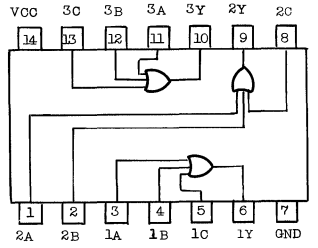
Positive logic: Y=A+B+C+D



TRIPLE 3-INPUT OR GATE

4075

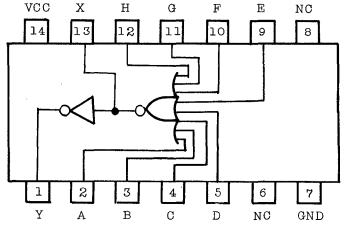
Positive logic: Y=A+B+C



8-INPUT NOR GATE

4078

Positive logic: Y=A+B+C+D+E+F+G+H



BUFFER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 07	HEX BUFFER	LS07		14
74HCT7007	HEX BUFFER	*LS07		14
74HC4049	HEX BUFFER (INVERTING)		4049	16
74HC4050	HEX BUFFER		4050	16
74HC 125	QUAD BUS BUFFER	LS125	5024	14
74HC 126	QUAD BUS BUFFER	LS126	5025	14
74HC 240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HCT240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HC 241	OCTAL BUS BUFFER	LS241		20
74HCT241	OCTAL BUS BUFFER	LS241		20
74HC 244	OCTAL BUS BUFFER	LS244		20
74HCT244	OCTAL BUS BUFFER	LS244		20
74HC 365	HEX BUS BUFFER	LS365A		16
74HC 366	HEX BUS BUFFER (INVERTING)	LS366A		16
74HC 367	HEX BUS BUFFER	LS367A	5012	16
74HC 368	HEX BUS BUFFER (INVERTING)	LS368A		16
74HC 540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HCT540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HC 541	OCTAL BUS BUFFER	LS541		20
74HCT541	OCTAL BUS BUFFER	LS541		20
74HC7240	OCTAL BUS BUFFER (SCHMITT IN)	LS240		20
74HC7241	OCTAL BUS BUFFER (SCHMITT IN)	LS241		20
74HC7244	OCTAL BUS BUFFER (SCHMITT IN)	LS244		20
74HC 242	QUAD BUS TRANSCEIVER (INVERTING)	LS242		14
74HC 243	QUAD BUS TRANSCEIVER	LS243		14
74HC 245	OCTAL BUS TRANSCEIVER	LS245		20
74HCT245	OCTAL BUS TRANSCEIVER	LS245		20
74HC 620	OCTAL BUS TRANSCEIVER (INVERTING)	LS620		20
74HC 623	OCTAL BUS TRANSCEIVER	LS623		20
74HC 640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HCT640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HC 643	OCTAL BUS TRANSCEIVER	LS643		20
74HCT643	OCTAL BUS TRANSCEIVER	LS643		20
74HC7640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HC7643	OCTAL BUS TRANSCEIVER	LS643		20
74HC7645	OCTAL BUS TRANSCEIVER	LS245		20

* Suggested alternative

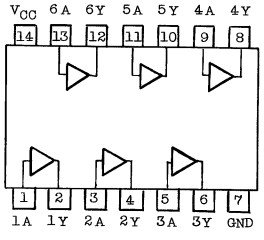
BUFFER

HEX BUFFER

07

T7007

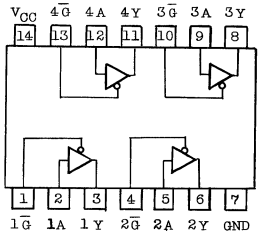
Positive logic : Y = A



QUAD BUS BUFFER

125

Positive logic : Y = A

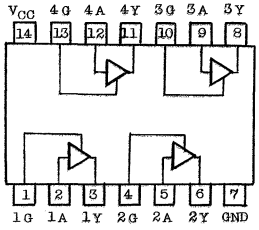


BUFFER (Continued)

QUAD BUS BUFFER

126

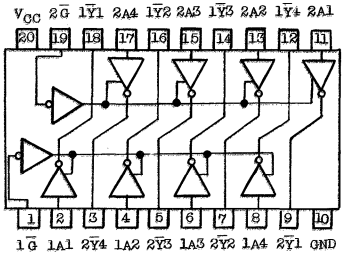
Positive logic: Y = A



OCTAL BUS BUFFER (INVERTING)

240

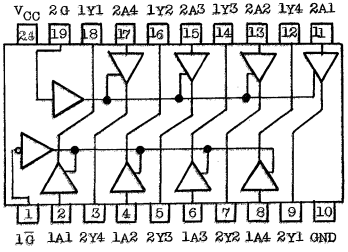
T240



OCTAL BUS BUFFER

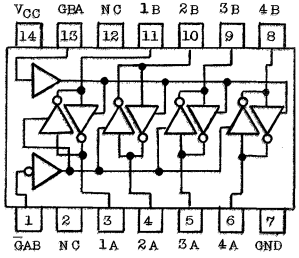
241

T241



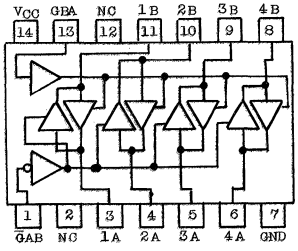
QUAD BUS TRANSCEIVER (INVERTING)

242



QUAD BUS TRANSCEIVER

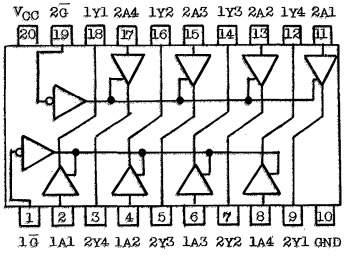
243



OCTAL BUS BUFFER

244

T244

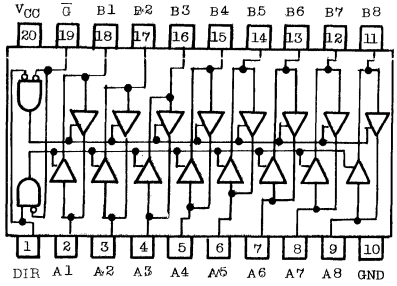


BUFFER (Continued)

OCTAL BUS TRANSCEIVER

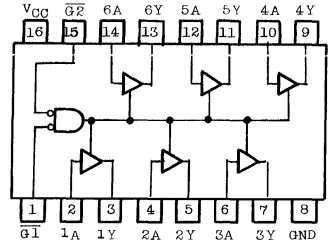
245

T245



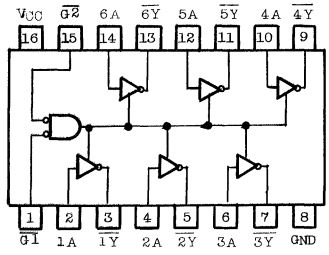
HEX BUS BUFFER

365



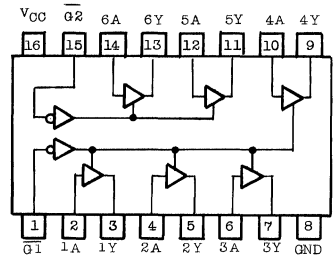
HEX BUS BUFFER (INVERTING)

366



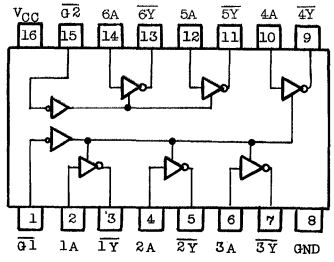
HEX BUS BUFFER

367



HEX BUS BUFFER (INVERTING)

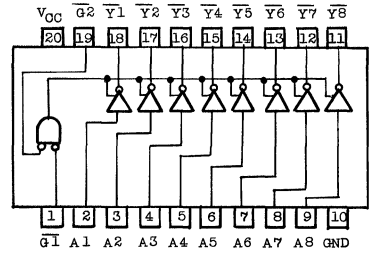
368



OCTAL BUS BUFFER (INVERTING)

540

T540

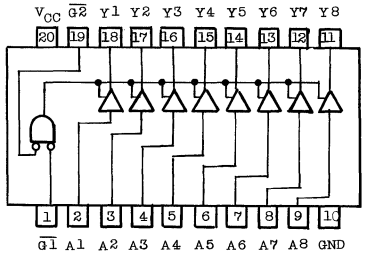


BUFFER (Continued)

OCTAL BUS BUFFER

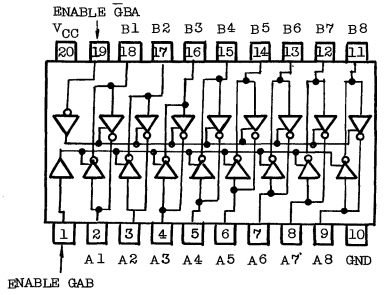
541

T541



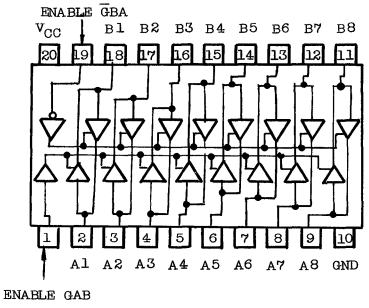
OCTAL BUS TRANSCEIVER (INVERTING)

620



OCTAL BUS TRANSCEIVER

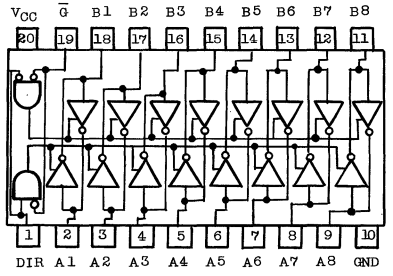
623



OCTAL BUS TRANSCEIVER (INVERTING)

640

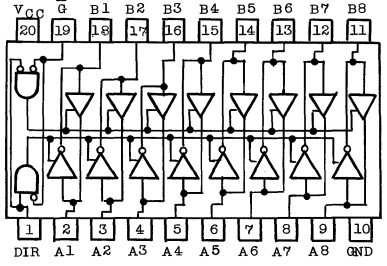
T640



OCTAL BUS TRANSCEIVER

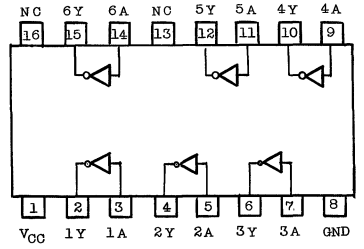
643

T643



HEX BUFFER/CONVERTER (INVERTING)

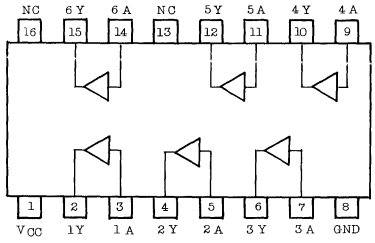
4049



BUFFER (Continued)

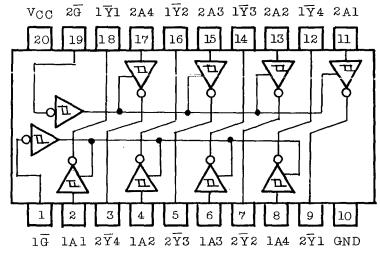
HEX BUFFER/CONVERTER

4050



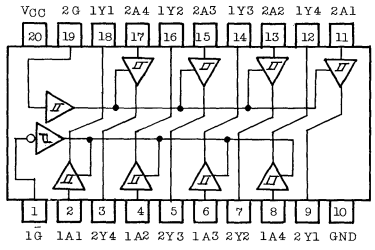
OCTAL BUS BUFFER (INVERTING)

7240



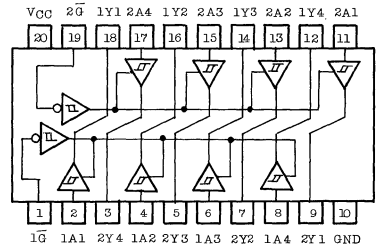
OCTAL BUS BUFFER

7241



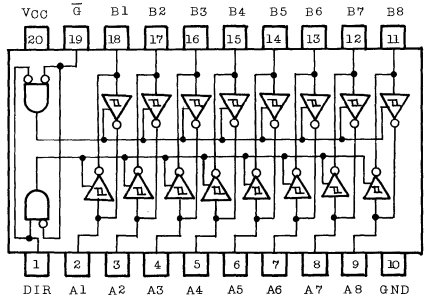
OCTAL BUS BUFFER

7244



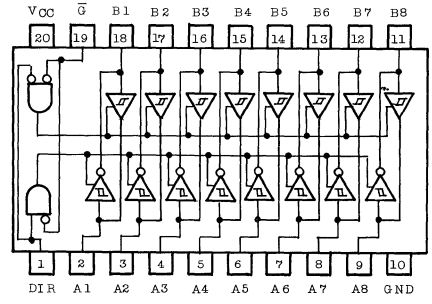
OCTAL BUS TRANSCEIVER (INVERTING)

7640



OCTAL BUS TRANSCEIVER

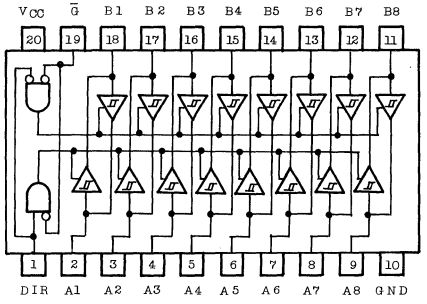
7643



BUFFER (Continued)

OCTAL BUS TRANSCEIVER

7645



FLIP-FLOP

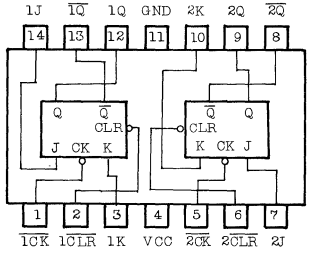
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 73	DUAL J-K FLIP-FLOP WITH CLEAR	LS73A,LS107A		14
74HC 76	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 107	DUAL J-K FLIP-FLOP WITH CLEAR	LS107A,LS73A		14
74HC 109	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS109A		16
74HC 112	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 113	DUAL J-K FLIP-FLOP WITH PRESET	LS113A		14
74HC 74	DUAL D F/F WITH PRESET AND CLEAR	LS74A	4013	14
74HC T74	DUAL D F/F WITH PRESET AND CLEAR	LS74A	4013	14
74HC 174	HEX D FLIP-FLOP WITH CLEAR	LS174	40174	16
74HCT174	HEX D FLIP-FLOP WITH CLEAR	LS174	40174	16
74HC 175	QUAD D FLIP-FLOP WITH CLEAR	LS175	40175	16
74HC 273	OCTAL D FLIP-FLOP WITH CLEAR	LS273		20
74HCT273	OCTAL D FLIP-FLOP WITH CLEAR	LS273		20
74HC 377	OCTAL D-TYPE FLIP-FLOP			20
74HC 374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 534	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS534		20
74HCT534	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS534		20
74HC 564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HCT564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HC 574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HCT646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HC 648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HCT648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HC 651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HCT651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HC 652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24
74HCT652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24

* Suggested alternative

FLIP-FLOP

DUAL J-K FLIP-FLOP WITH CLEAR

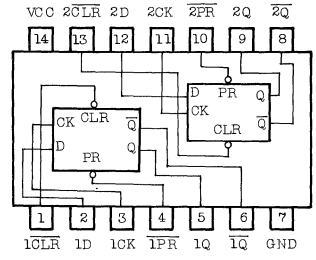
73



DUAL D FLIP-FLOP WITH PRESET AND CLEAR

74

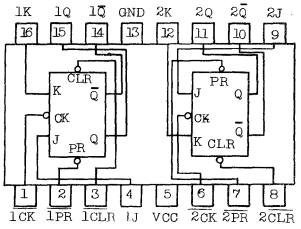
T74



FLIP-FLOP (Continued)

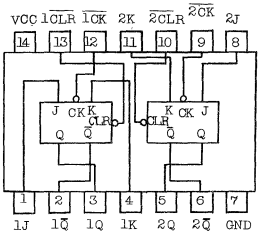
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

76



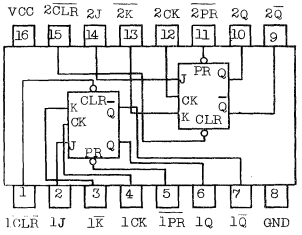
DUAL J-K FLIP-FLOP WITH CLEAR

107



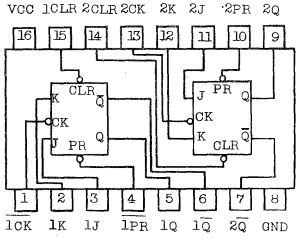
DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR

109



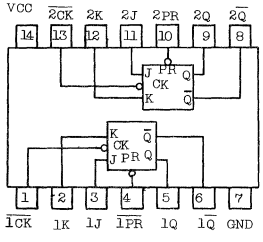
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

112



DUAL J-K FLIP-FLOP WITH PRESET

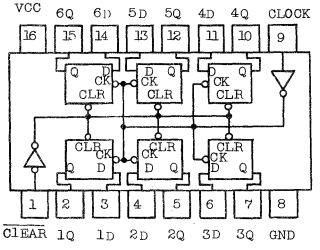
113



HEX D FLIP-FLOP WITH CLEAR

174

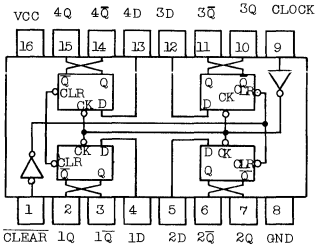
T174



FLIP-FLOP (Continued)

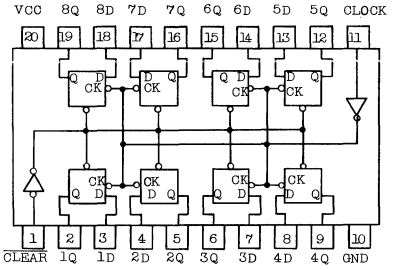
QUAD D FLIP-FLOP WITH CLEAR

175



OCTAL D FLIP-FLOP WITH CLEAR

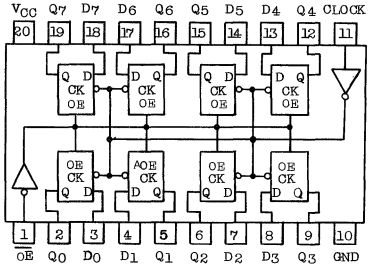
273
T273



OCTAL D FLIP-FLOP (3-STATE)

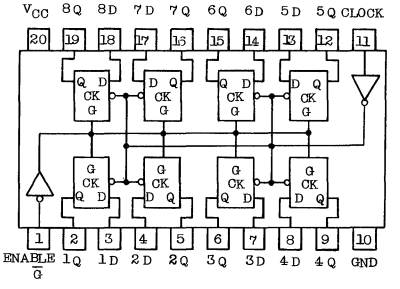
374

T374



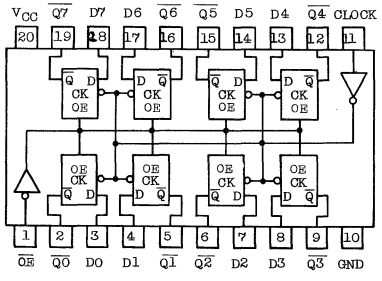
OCTAL D FLIP-FLOP

377



OCTAL D FLIP-FLOP (3-STATE/INV.)

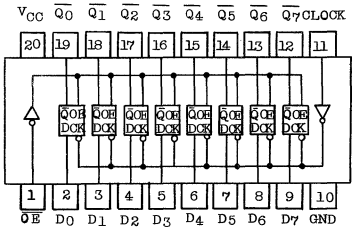
534
T534



OCTAL D FLIP-FLOP (3-STATE/INV.)

564

T564

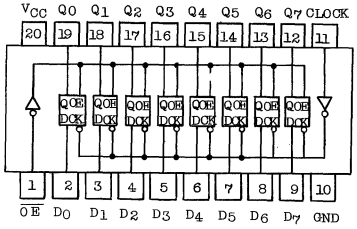


FLIP-FLOP (Continued)

OCTAL D FLIP-FLOP (3-STATE)

574

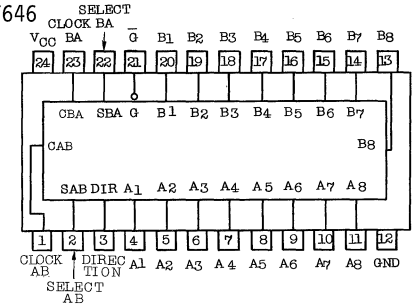
T574



OCTAL BUS TRANSCEIVER REGISTER (3-STATE)

646

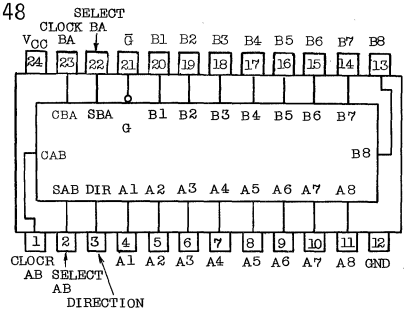
T646



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

648

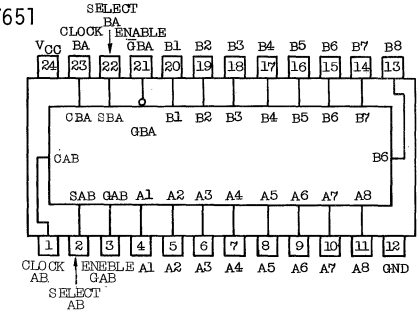
T648



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

651

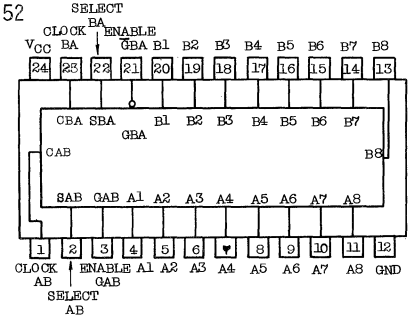
T651



OCTAL BUS TRANSCEIVERS REGISTER (3-STATE)

652

T652



LATCH

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 75	4-BIT D-TYPE LATCH	LS75	*4042	16
74HC 77	4-BIT D-TYPE LATCH	LS77	*4042	14
74HC 259	8-BIT ADDRESSABLE LATCH	LS259	*4099	16
74HC 279	QUAD $\overline{S}$-$\overline{R}$ LATCH	LS279	*4043,*4044	16
74HC 375	QUAD D-TYPE LATCH	LS375		16
74HC 373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HC 533	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS533		20
74HCT533	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS533		20
74HC 563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HCT563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HC 573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20

* Suggested alternative

LATCH

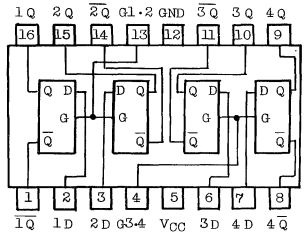
4-BIT LATCH

75

FUNCTION TABLE

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Q}$n

X:DON'T CARE



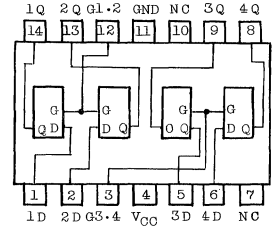
4-BIT LATCH

77

FUNCTION TABLE

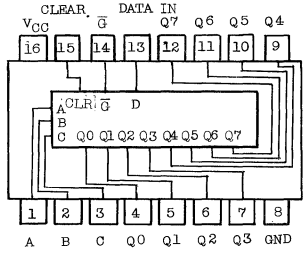
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Q}$n

X:DON'T CARE



8-BIT ADDRESSABLE LATCH

259



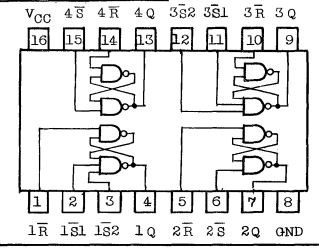
QUAD $\overline{S}$-$\overline{R}$ LATCH

279

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{S}$*	$\overline{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

* FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:
H=BOTH $\overline{S}$ INPUTS HIGH
L=ONE OF BOTH INPUTS LOW

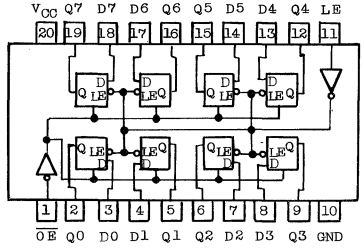


LATCH (Continued)

OCTAL LATCH (3-STATE)

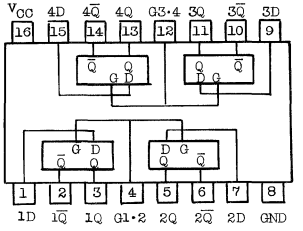
373 NONINVERTED DATA OUTPUTS

T373



QUAD LATCH

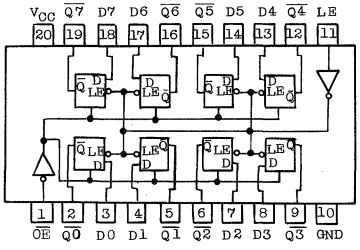
375



OCTAL LATCH (3-STATE)

533 INVERTED DATA OUTPUTS

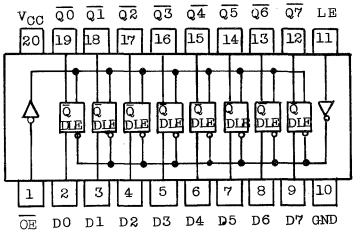
T533



OCTAL LATCH (3-STATE)

563 INVERTED DATA OUTPUTS

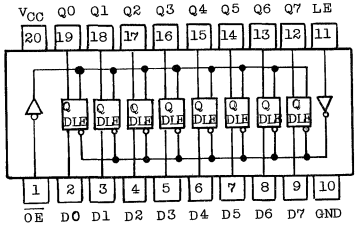
T563



OCTAL LATCH (3-STATE)

573 NONINVERTED DATA OUTPUTS

T573



MULTIVIBRATOR

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 123	DUAL MONOSTABLE MULTIVIBRATOR	LS123	*4538,*4528	16
74HC 221	DUAL MONOSTABLE MULTIVIBRATOR	LS221	*4538,*4528	16
74HC 423	DUAL MONOSTABLE MULTIVIBRATOR	LS423	*4538,*4528	16
74HC4538	DUAL MONOSTABLE MULTIVIBRATOR	*LS423	4538, 4528	16

* Suggested alternative

MULTIVIBRATOR

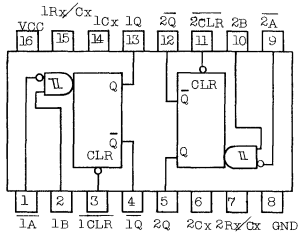
DUAL RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR

123

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎
↓	L	H	⎍	⎎

X : DON'T CARE



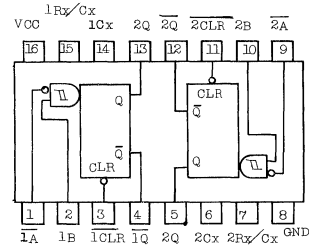
DUAL MONOSTABLE MULTIVIBRATOR

221

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎
↓	L	H	⎍	⎎

X : DON'T CARE



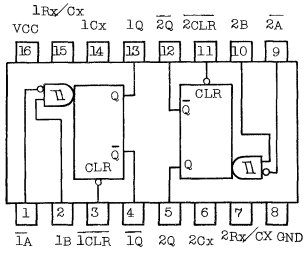
DUAL RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR

423

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎

X : DON'T CARE



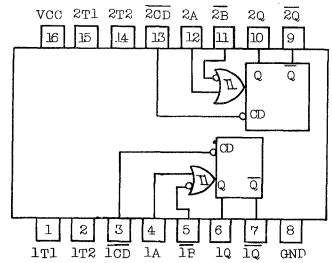
DUAL RETRIGGERABLE MONOSTABLE MULTI-VIBRATOR

4538

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CD}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⎍	⎎
H	↓	H	⎍	⎎

X : DON'T CARE



DECODER

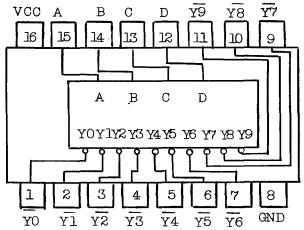
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 42	BCD TO DECIMAL DECODER	LS42	*4028	16
74HC 131	3-TO-8 LINE DECODER/LATCH	LS131		16
74HC 137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HCT137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HC 138	3-TO-8 LINE DECODER	LS138		16
74HCT138	3-TO-8 LINE DECODER	LS138		16
74HC 139	DUAL 2-TO-4 LINE DECODER	LS139	4556,*4555	16
74HC 154	4-TO-16 LINE DECODER	LS154	*4515	24
74HC 155	DUAL 2-TO-4 LINE DECODER	LS155	*4556,*4555	16
74HC 237	3-TO-8 LINE DECODER/LATCH			16
74HC 238	3-TO-8 LINE DECODER			16
74HC4028	BCD-TO DECIMAL DECODER		4028	16
74HC4514	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4514	24
74HC4515	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4515	24
74HC4511	BCD TO 7 SEGMENT L/D/D (LED)	*LS47,*LS48,*LS49	4511	16
74HC4543	BCD TO 7 SEGMENT L/D/D (LCD)	*LS47,*LS48,*LS49	4543	16

* Suggested alternative

DECODER (Continued)

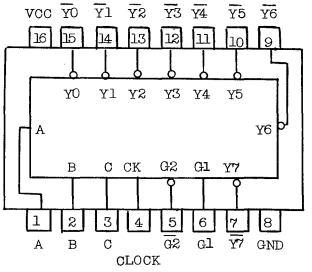
BCD TO DECIMAL DECODER

42



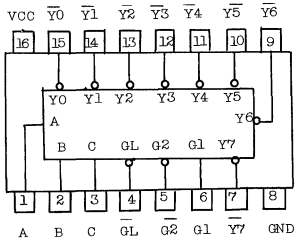
3-TO-8 LINE DECODER/LATCH

131



3-TO-8 LINE DECODER/LATCH

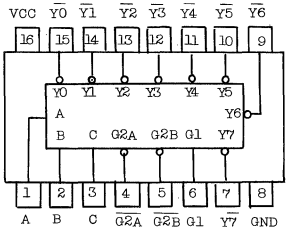
137



3-TO-8 LINE DECODER

138

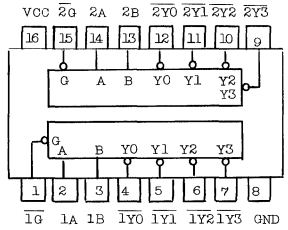
T138



DECODER (Continued)

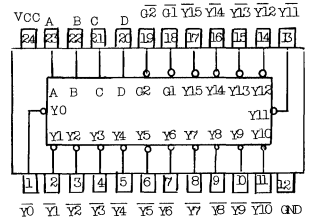
DUAL 2-TO-4 LINE DECODER

139
T139



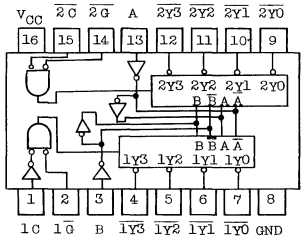
4-TO-16 LINE DECODER

154



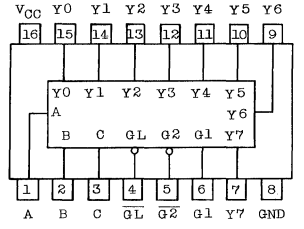
DUAL 2-TO-4 LINE DECODER
3-TO-8 LINE DECODER

155



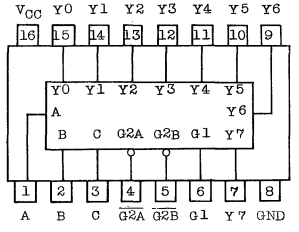
3-TO-8 LINE DECODER/LATCH

237



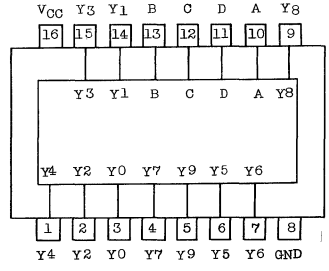
3-TO-8 LINE DECODER

238



BCD-TO-DECIMAL DECODER

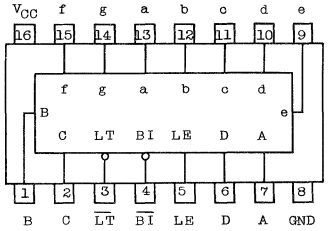
4028



DECODER (Continued)

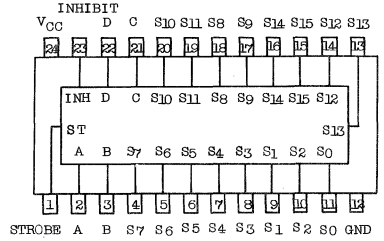
BCD TO 7 SEGMENT LATCH/DECODER/DRIVER

4511



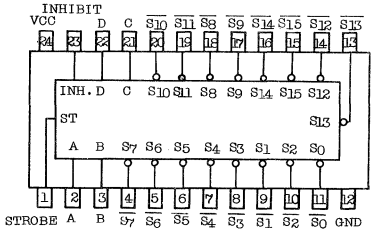
4-TO-16 LINE DECODER/LATCH

4514



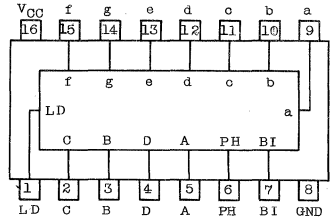
4-TO-16 LINE DECODER/LATCH

4515



BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

4543



ENCODER

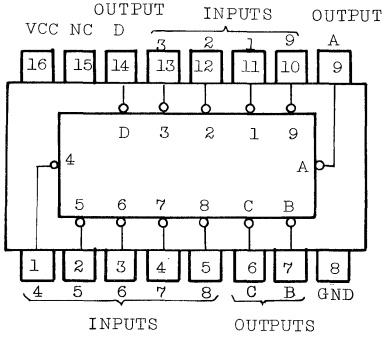
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 147	10-TO-4 LINE PRIORITY ENCODER	LS147		16
74HC 148	8-TO-3 LINE PRIORITY ENCODER	LS148	*4532	16

* Suggested alternative

ENCODER

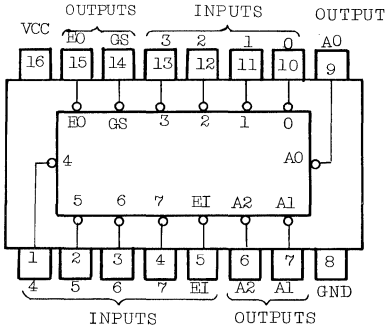
10-TO-4 LINE PRIORITY ENCODER

147



8-TO-3 LINE PRIORITY ENCODER

148



REGISTER

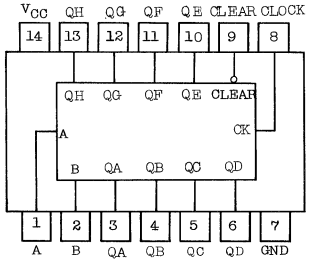
品　名	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 164	8-BIT SIPO SHIFT REGISTER	LS164	*4034	14
74HCT164	8-BIT SIPO SHIFT REGISTER	LS164	*4034	14
74HC 165	8-BIT PISO SHIFT REGISTER	LS165	*4014,*4021	16
74HC 166	8-BIT PISO SHIFT REGISTER	LS166	*4014,*4021	16
74HC 173	QUAD D-TYPE REGISTER (3-STATE)	LS173	4076	16
74HC 194	4-BIT PIPO SHIFT REGISTER	LS194A	40194,*40104	16
74HC 195	4-BIT PIPO SHIFT REGISTER	LS195A	*4035	16
74HC 299	8-BIT PIPO SHIFT REGISTER	LS299	*4034	20
74HC 323	8-BIT PIPO SHIFT REGISTER	LS323	*4034	20
74HC 595	8-BIT SHIFT REGISTER/LATCH (3-STATE)	LS595		16
74HC 597	8-BIT LATCH/SHIFT REGISTER	LS597		16
74HC 670	4 WORD × 4-BIT REGISTER FILE (3-STATE)	LS670		16
74HC4094	8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)		4094	16

* Suggested alternative

REGISTER

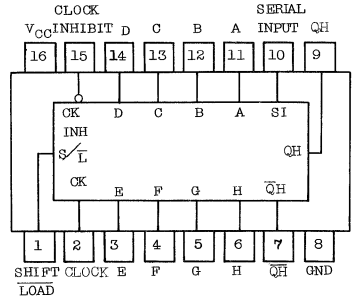
8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

164
T164



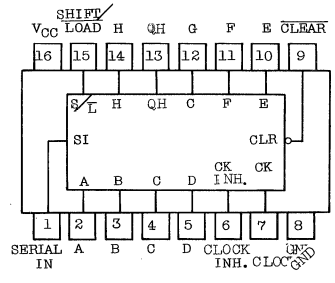
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

165



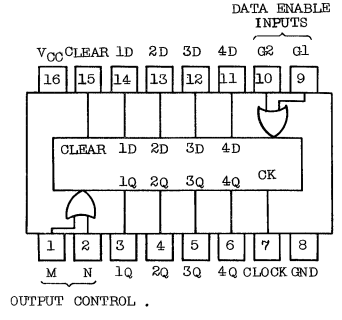
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT

166



QUAD D FLIP-FLOP (3-STATE)

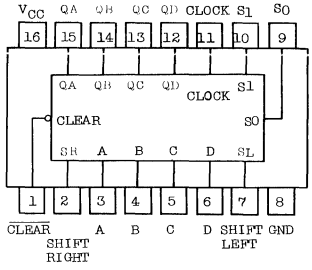
173



REGISTER (Continued)

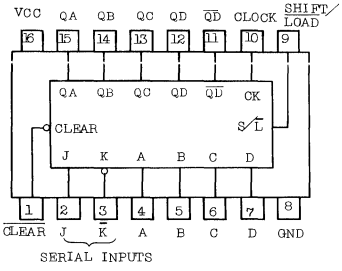
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

194



4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

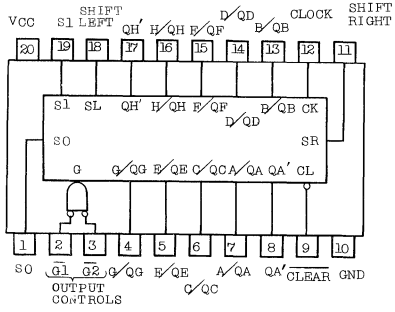
195



8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER (3-STATE)

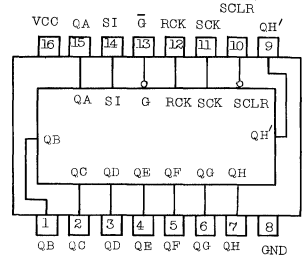
299 DIRECT CLEAR

323 SYNCHRONOUS CLEAR



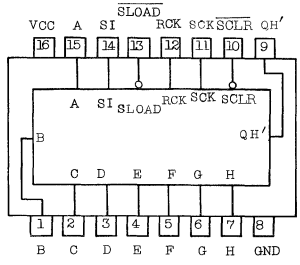
8-BIT SHIFT REGISTER/LATCH (3-STATE)

595



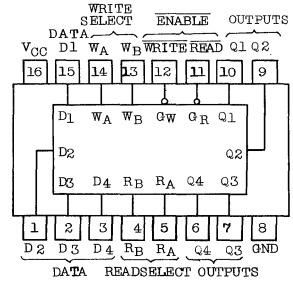
8-BIT LATCH/SHIFT REGISTER

597



4 WORD x 4 BIT REGISTER FILE(3-STATE)

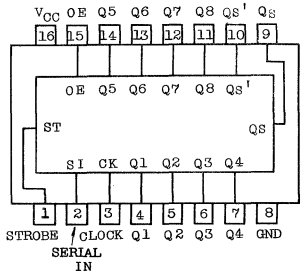
670



REGISTER (Continued)

8-BIT SERIAL-IN / PARALLEL-OUT SHIFT REGISTER/LATCH (3-STATE)

4094



COUNTER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 161	SYNC. BINARY COUNTER WITH ASYNC. CLEAR	LS161A	40161	16
74HC 163	SYNC. BINARY COUNTER WITH SYNC. CLEAR	LS163A	40163	16
74HC 191	4-BIT BINARY UP/DOWN COUNTER	LS191	*4516	16
74HC 193	SYNC. UP/DOWN BINARY COUNTER	LS193	40193	16
74HC 393	DUAL BINARY COUNTER	LS393	*4520	14
74HC 590	8-BIT BINARY COUNTER/REGISTER (3-STATE)	LS590		16
74HC 592	8-BIT REGISTER/BINARY COUNTER	LS592		16
74HC 593	8-BIT REGISTER/BINARY COUNTER (3-STATE)	LS593		20
74HC 691	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS691		20
74HC 693	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS693		20
74HC 697	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS697		20
74HC 699	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS699		20
74HC4520	DUAL 4-BIT BINARY COUNTER		4520	16
74HC 160	SYNC. DECADE COUNTER WITH ASYNC. CLEAR	LS160A	40160	16
74HC 162	SYNC. DECADE COUNTER WITH SYNC. CLEAR	LS162A	40162	16
74HC 190	BCD UP/DOWN COUNTER	LS190	*4510	16
74HC 192	SYNC. UP/DOWN DECADE COUNTER	LS192	40192	16
74HC 390	DUAL DECADE COUNTER	LS390		16
74HC 690	DECADE COUNTER REGISTER (3-STATE)	LS690		20
74HC 692	DECADE COUNTER REGISTER (3-STATE)	LS692		20
74HC 696	U/D DECADE COUNTER/REGISTER (3-STATE)	LS696		20
74HC 698	U/D DECADE COUNTER/REGISTER (3-STATE)	LS698		20
74HC4518	DUAL DECADE COUNTER		4518	16
74HC4017	DECADE COUNTER/DIVIDER		4017	16
74HC4020	14-STAGE BINARY COUNTER		4020	16
74HC4022	OCTAL COUNTER/DIVIDER		4022	16
74HC4024	7-STAGE BINARY COUNTER		4024	14
74HC4040	12-STAGE BINARY COUNTER		4040	16
74HC4060	14-STAGE BINARY COUNTER/OSCILLATOR			16
74HC40102	DUAL BCD PROGRAMMABLE DOWN COUNTER		40102	16
74HC40103	8-BIT BINARY PROGRAMMABLE DOWN COUNTER		40103	16
74HC7292	PROGRAMMABLE DIVIDER/TIMER	*LS292		16
74HC7294	PROGRAMMABLE DIVIDER/TIMER	*LS294		16

* Suggested alternative

COUNTER

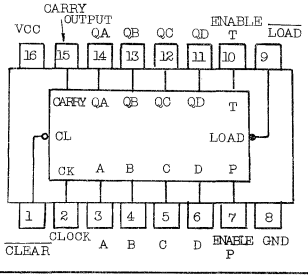
PRESETTABLE 4-BIT COUNTER

160 DECADE, ASYNCHRONOUS CLEAR

161 BINARY, ASYNCHRONOUS CLEAR

162 DECADE, SYNCHRONOUS CLEAR

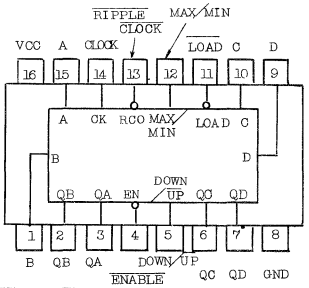
163 BINARY, SYNCHRONOUS CLEAR



SYN. 4-BIT UP/DOWN COUNTER

190 BCD

191 BINARY

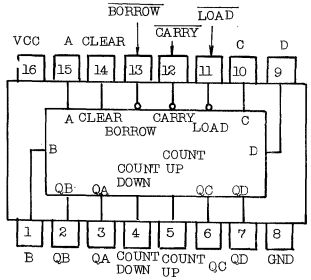


COUNTER (Continued)

SYNC. 4-BIT UP/DOWN COUNTER

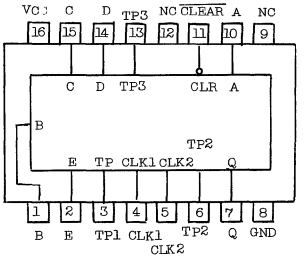
192 BCD

193 BINARY



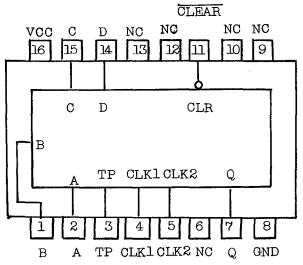
PROGRAMMABLE DIVIDER/TIMER

7292 FROM 2^2 to 2^{31}



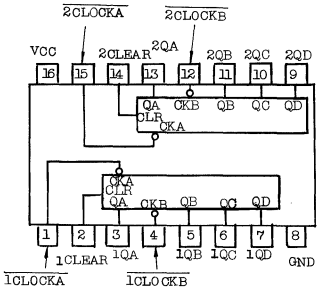
PROGRAMMALBE DIVIDER/TIMER

7294 FROM 2^2 to 2^{15}



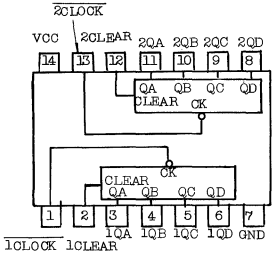
DUAL DECADE COUNTER

390 (BI-QUINARY OR BCD)



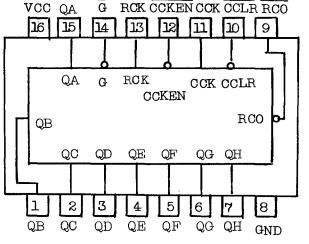
DUAL 4-BIT BINARY COUNTER

393



8-BIT BINARY COUNTER WITH OUTPUT REGISTER (3-STATE)

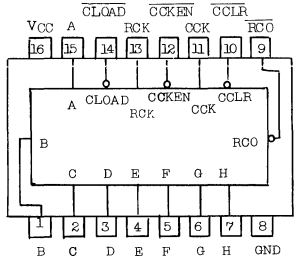
590



COUNTER (Continued)

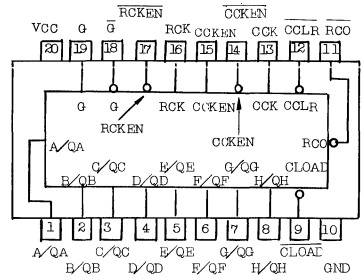
8-BIT BINARY COUNTER WITH INPUT REGISTER

592



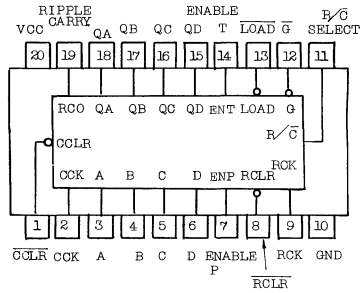
8-BIT BINARY COUNTER WITH INPUT REGISTER (MULTIPLEXED 3-STATE OUTPUTS)

593



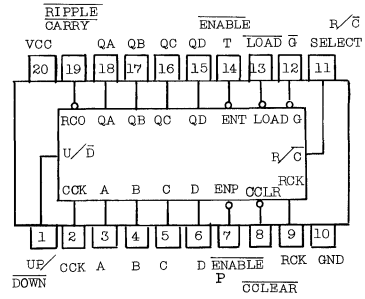
SYNCHRONOUS COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUT

690 DECADE, DIRECT CLEAR
691 BINARY, DIRECT CLEAR
692 DECADE, SYNCHRONOUS CLEAR
693 BINARY, SYNCHRONOUS CLEAR



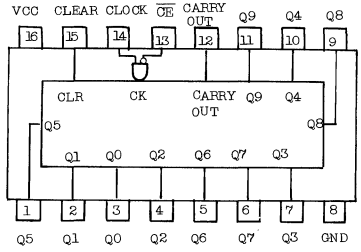
SYNCHRONOUS UP/DOWN COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUTS

696 DECADE, DIRECT CLEAR
697 BINARY, DIRECT CLEAR
698 DECADE, SYNCHRONOUS CLEAR
699 BINARY, SYNCHRONOUS CLEAR



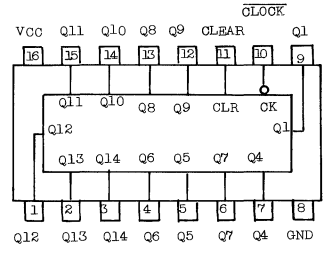
DECADE COUNTER/DIVIDER

4017



14-STAGE BINARY COUNTER

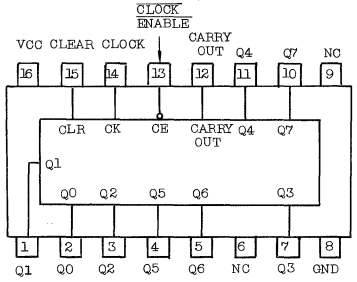
4020



COUNTER (Continued)

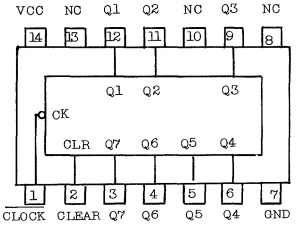
OCTAL COUNTER/DIVIDER

4022



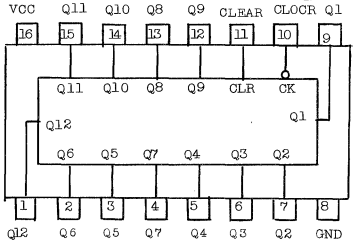
7-STAGE BINARY COUNTER

4024



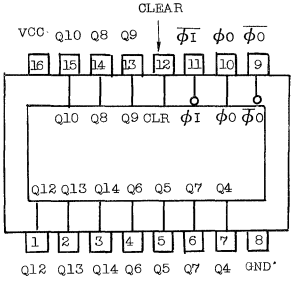
12-STAGE BINARY COUNTER

4040



14-STAGE BINARY COUNTER/OSCILLATOR

4060

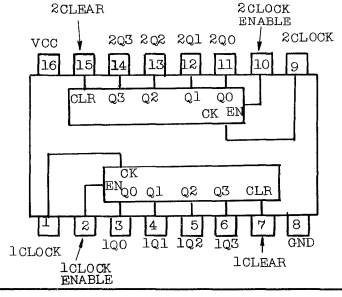


DUAL DECADE COUNTER

4518

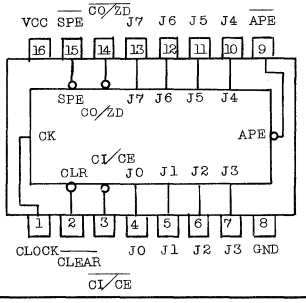
DUAL BINARY COUNTER

4520



PROGRAMMABLE DOWN COUNTER

40102 DUAL BCD
40103 8-BIT BINARY



MULTIPLEXER

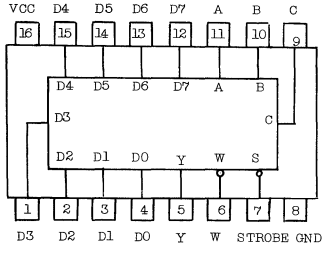
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC4016	QUAD BILATERAL SWITCH		4016	14
74HC4051	8-CHANNEL ANALOG MULTIPLEXER		4051	16
74HC4052	DUAL 4-CHANNEL ANALOG MULTIPLEXER		4052	16
74HC4053	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER		4053	16
74HC4066	QUAD BILATERAL SWITCH		4016,4066	14
74HC4316	QUAD BILATERAL SWITCH		*4016	16
74HC4351	8-CH. ANALOG MUX. WITH ADD. LATCH		*4051	20
74HC4352	DUAL 4-CH. ANALOG MUX. WITH ADD. LATCH		*4052	20
74HC4353	TRIPLE 2-CH. ANALOG MUX. WITH ADD. LATCH		*4053	20
74HC 151	8-CHANNEL MULTIPLEXER	LS151	*4512	16
74HC 153	DUAL 4-CHANNEL MULTIPLEXER	LS153	*4539	16
74HC 157	QUAD 2-CHANNEL MULTIPLEXER	LS157		16
74HC 158	QUAD 2-CHANNEL MULTIPLEXER (INVERTING)	LS158		16
74HC 251	8-CHANNEL MULTIPLEXER (3-STATE)	LS251	*4512	16
74HC 253	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	LS253	*4539	16
74HC 257	QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	LS257		16
74HC 258	QUAD 2-CHANNEL MULTIPLEXER (3-STATE/INVERTING)	LS258		16
74HC 298	QUAD 2-CHANNEL MULTIPLEXER/REGISTER	LS298		16
74HC 352	DUAL 4-CHANNEL MULTIPLEXER	L5352	*4539	16
74HC 353	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	LS354	*4539	16
74HC 354	8-CHANNEL MULTIPLEXER/REGISTER	LS354	*4512	20
74HC 356	8-CHANNEL MULTIPLEXER/REGISTER	LS356	*4512	20

* Suggested alternative

MULTIPLEXER

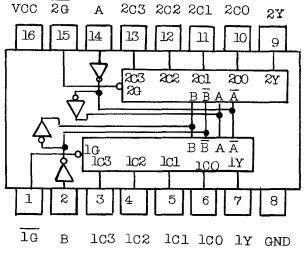
8-CHANNEL MULTIPLEXER

151



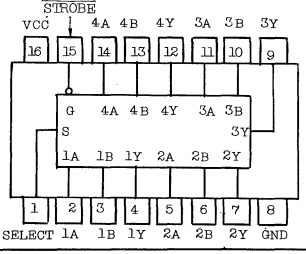
DUAL 4-CHANNEL MULTIPLEXER

153



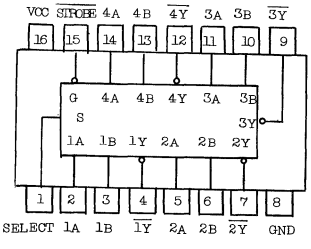
QUAD 2-CHANNEL MULTIPLEXER

157 NONINVERTED DATA OUTPUTS



QUAD 2-CHANNEL MULTIPLEXER

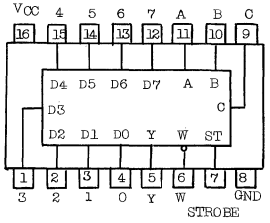
158 INVERTED DATA OUTPUTS



MULTIPLEXER (Continued)

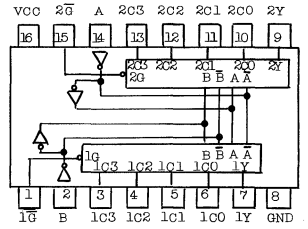
8-CHANNEL MULTIPLEXER (3-STATE)

251



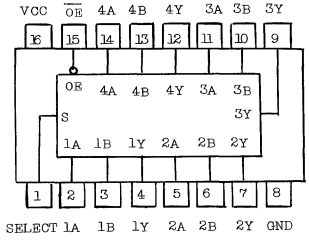
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)

253



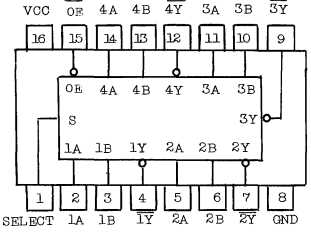
QUAD 2-CHANNEL MULTIPLEXER (3-STATE)

257 NONINVERTED DATA OUTPUTS



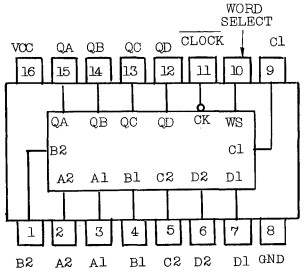
QUAD 2-CNANNEL MULTIPLEXER (3-STATE)

258 INVERTED DATA OUTPUTS



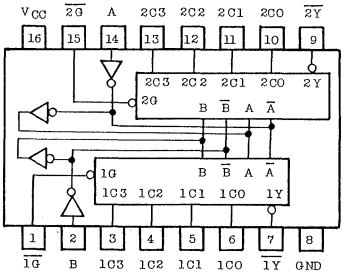
QUAD 2-CHANNEL MULTIPLEXERS WITH OUTPUT REGISTER

298



DUAL 4-CHANNEL MULTIPLEXER

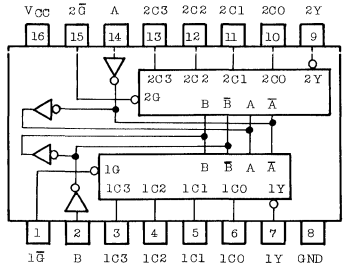
352



MULTIPLEXER (Continued)

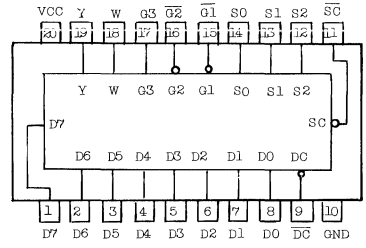
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)

353



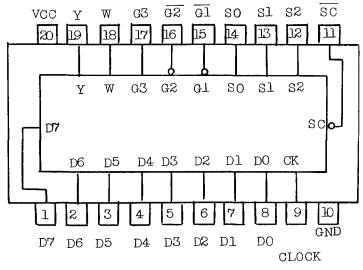
8-CHANNEL MULTIPLEXER WITH LATCH (3-STATE)

354



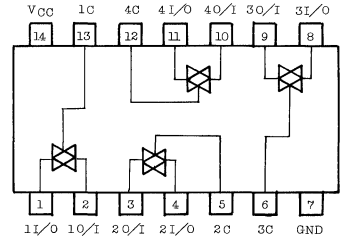
8-CHANNEL MULTIPLEXER WITH FLIP-FLOP (3-STATE)

356



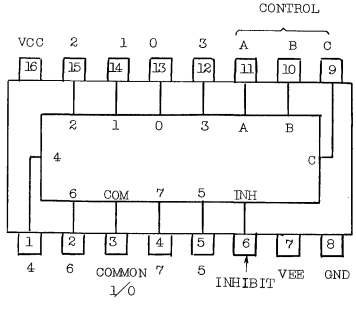
QUAD BILATERAL SWITCH

4016



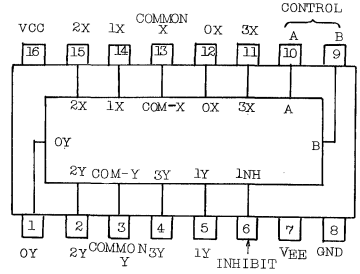
8-CHANNEL ANALOG MULTIPLEXER

4051



DUAL 4-CHANNEL ANALOG MULTIPLEXER

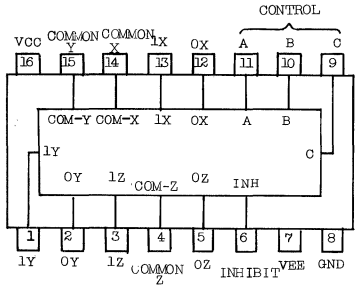
4052



MULTIPLEXER (Continued)

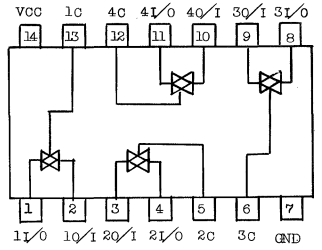
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER

4053



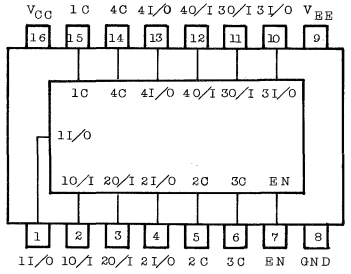
QUAD BILATERAL SWITCH

4066



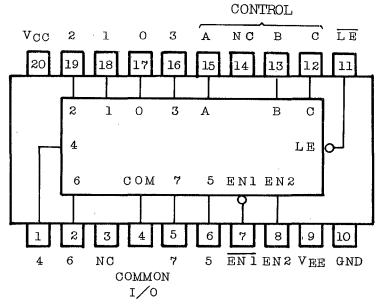
QUAD BILATERAL SWITCH

4316



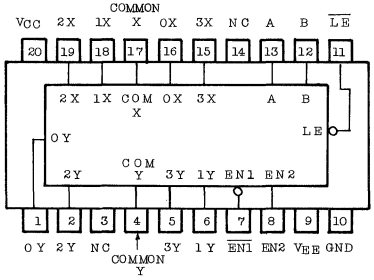
8-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH

4351



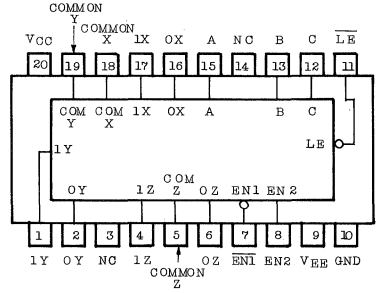
DUAL 4-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH

4352



TRIPLE 2-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH

4353



COMPARATOR

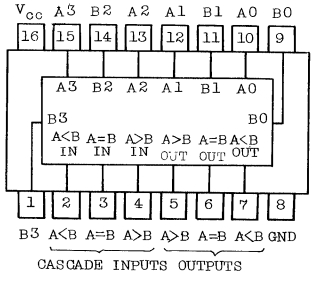
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 85	4-BIT MAGNITUDE COMPARATOR	LS 85	*4063, *4585	16
74HC 688	8-BIT EQUALITY COMPARATOR	LS688		20
74HCT688	8-BIT EQUALITY COMPARATOR	LS688		20

* Suggested alternative

COMPARATOR

4-BIT MAGNITUDE COMPARATOR

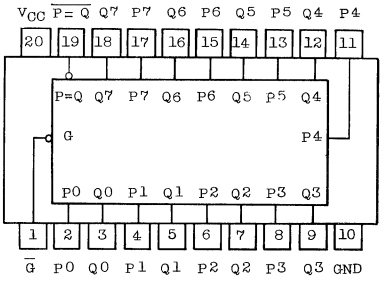
85



8-BIT EQUALITY COMPARATOR

688

T688



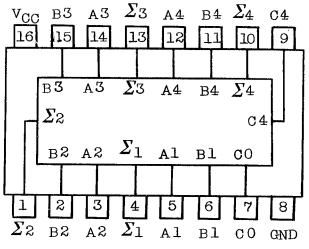
ADDER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 283	4-BIT BINARY FULL ADDER	LS283,LS83	4008	16

ADDER

4-BIT BINARY FULL ADDER

283



ALU

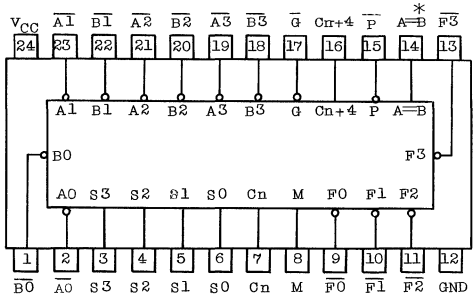
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 181	ARITHMETIC LOGIC UNIT	LS181		24
74HC 182	LOOK AHEAD CARRY LOGIC	LS182		16

ALU

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

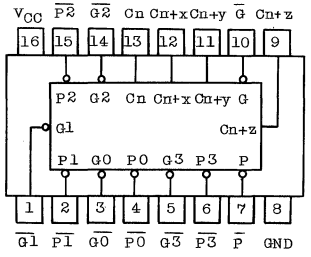
181

*: OPEN DRAIN OUTPUT



LOCK AHEAD CARRY GENERATOR

182



PARITY TREE

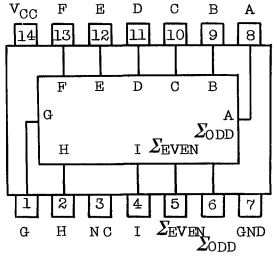
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC280	9-BIT PARITY GENERATOR/CHECKER	LS280	*4531	14

* 類似品

PARITY TREE

9-BIT ODD/EVEN PARITY GENERATOR/ CHECKER

280



3. PRODUCT OUTLINE OF THE TC74HCxxxA SERIES

The TC74HCxxxA series is an improved High Speed Logic development of TOSHIBA. Some of these improvements are outlined below:

(1) Increased Speed of Operation:

Over 20 companies now manufacture the 74HC series worldwide. The JEDEC JC40.2 committee has standardized the electrical characteristics of this series in JEDEC Standard 7A. This permits interchangeability of devices between manufacturers for greater end-user convenience. Increasing the speed of the TC74HCxxxA series by an average of 20% to 30% ensures compatibility with Standard 7A as well as with most other worldwide 74HC products. TOSHIBA achieved the higher speed by using a thinner gate oxide layer and by decreasing the effective channel length and the internal parasitic capacitance to increase transconductance gm per unit channel width by 30% over that of the original series.

(2) Latch-up Strength:

TOSHIBA had previously improved the TC74HC series to make it latch-up resistant. By using the same process, the TC74HCxxxA revision also has a high resistance to latch-up; TOSHIBA high speed C^2MOS products can be used in applications in which noise and surges often occur.

Table 3-1 shows the results of latch-up tests.

Table 3-1 Results of Latch-up Tests **

		TC74xxx series		TC74xxxA series	
method	pin	TC74HC00P	TC74HC74P	TC74HC00AP	TC74HC74AP
Current Injection (static trigger)	Input	>±70mA *	>±70mA *	>±300mA	>±300mA
	Output	>±300mA	>±300mA	>±300mA	>±300mA
Charge Injection (dynamic trigger)	Input	>±250V	>±250V	>±250V	>±250V
	Output	>±250V	>±250V	>±250V	>±250V
	Power supply	>±250V	>±250V	>±250V	>±250V

* Input protection resistor limits current

** See Fig. 9-14 Latch-up strength measurement system in Sect. 9-7.

(3) Electrostatic Discharge:

In the original TC74HCxxx series, TOSHIBA designed in an input protective circuit which combines silicon diodes with a polysilicon series resistor (Fig. 3–1(a)). This circuit suppresses excess current flow in the input terminal when the input voltage is higher than V_{CC} or lower than GND. This circuit is effective for increased latch–up protection, but the electrostatic discharge protection, measured using the MIL–STD method (100pF/1.5kohms), was about ±2.0kV maximum. Anything above this caused burn damage to the polysilicon resistor or increased breakdown of the oxide film directly under the polysilicon.

As there is no latch–up problem with the revised types, the TC74HCxxxA series, TOSHIBA uses a protective circuit composed of high thermal capacity silicon diodes and a resistor constructed by diffusion (Fig. 3–1(b)). According to MIL–STD, any product not reaching a ±2.0kV level must carry an ESD Sensitive (ESDS) label. TOSHIBA's TC74HCxxxA series far surpasses this level with a 2.0kV or greater rating using the MIL method.

Table 3–2 shows the Electrostatic Discharge Test Results.

Fig. 3–1 The Input Protective Circuits

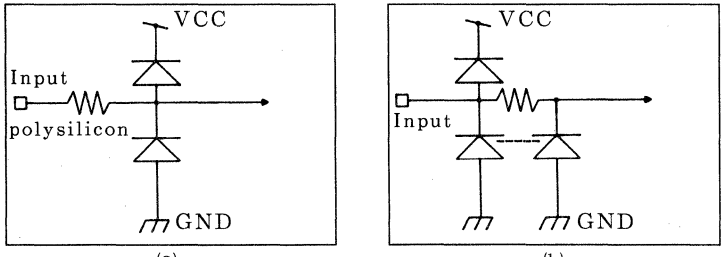
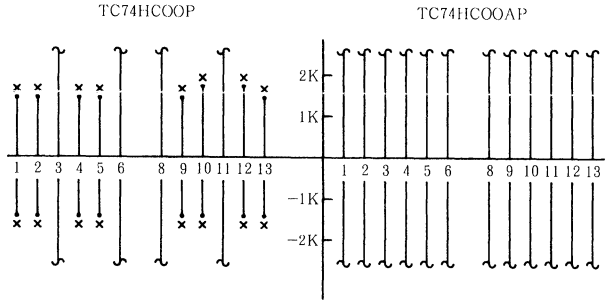
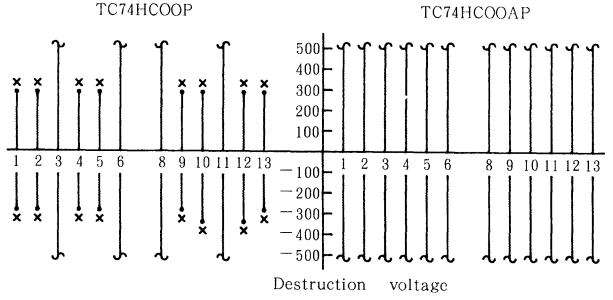


Table 3-2 ESD Test Result

(a) MIL Method (C=100pF, R= 1.5KΩ)

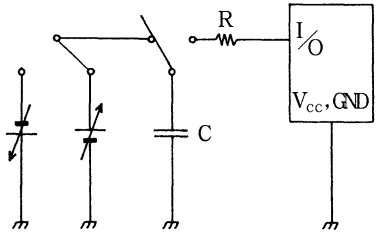


(b) EIAJ Method (C=200pF, R=0Ω)



·Normal ×Destruction ⊥ Discharge stopped

(c) Test Circuit



3–1 Features

The TC74HCxxxA series has the following features as compared to other standard Logic IC:

(1) High Speed Operation: Same as LSTTL

(2) Low Power Dissipation: Same as standard CMOS series (μW)

(3) Output Drive Capability: Capable of directly driving 10 LSTTL loads (Standard output type).
Capable of directly driving 15 LSTTL loads (Buffer output type).

(4) High Noise Immunity: HC/HCU Type ··· 45% V_{CC} (Typ.)
HCT Type ····· 25% V_{CC} (Typ.)

(5) Wide Operating Voltage Range:
HC/HCU Type ··· 2 to 6V
HCT Type ····· 4.5 to 5.5V

(6) Wide Operating Temperature Range: −40 to + 85℃

(7) Self−contained static electricity protective circuit:
±500V (typ.) by EIAJ method
±3000V (typ.) by MIL STD method
(All inputs and outputs)

(8) Ample Latch up Capacity: Total input and output ±300 mA and above.

(9) Based on the same pin connection and function with LSTTL,
and line up with CMOS original version.

(10) Wide product Line up: Over 200 types

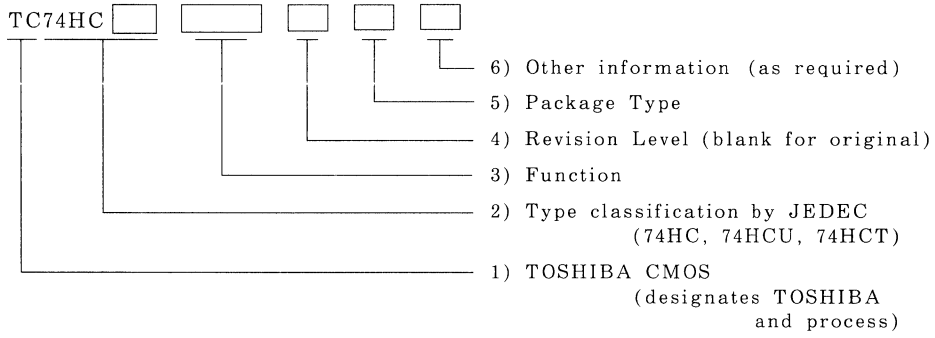
Table 3−2 shows comparison of characteristics of various logic families.

Parameter		HS−C²MOS (TC74HCxxxA)	LSTTL	HS−C²MOS (TC40Hxxx)	C²MOS (TC4xxx)	Condition
Propagation Delay Time GATE (C_L=15pF)		6ns typ	9ns typ	15ns typ	65ns typ	V_{CC} =5.0V Ta=25℃
Maximum Clock Frequency J/KF • F (C_L=15pF)		80MHz typ	45MHz typ	20MHz typ	2MHz typ	
Quiescent Power Dissipation (GATE)		0.01 μW typ	8mW typ	0.01 μW typ	0.01 μW typ	Over temperature and voltage range
Input Voltage	V_{IH}	3.5V min	2.0V min	4.0V min	3.5V min	V_{CC} =5.0V Over temperature range
	V_{IL}	1.5V max	0.8V max	1.0V max	1.5V max	
Output Current	$\|I_{OH}\|$	4mA min*1	0.4mA min*2	0.36mA min*3	0.42mA min*3	*1 V_{CC}=4.5V *2 V_{CC}=4.75V *3 V_{CC}=5V Over temp. range
	I_{OL}	4mA min	4mA min	0.8mA min	0.42mA min	
Operating Voltage Range		2~6V	4.75~5.25V	2~8V	3~18V	
Operating Temperature Range		−40~85℃	0~70℃	−40~85℃	−40~85℃	

Table 3−2 Comparison of Logic Family Characteristics

3–2 Method of Designating the TC74HC Series

The TC74HC series is designated by the standard established by JEDEC and is as shown below;



(Example) TC74HCT240AP

High Speed C^2MOS IC which is pin and functionally compatible with the bipolar 74LS240
Input is designed for TTL voltage levels, and direct driving from LSTTL is possible.
Package type is plastic Dual Inline Package (DIP).

(1) "TC"

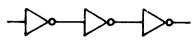
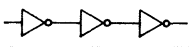
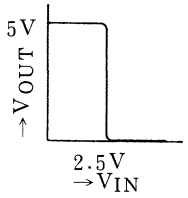
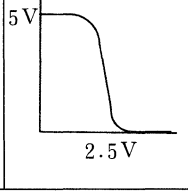
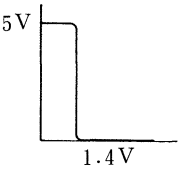
Proprietary name identifying TOSHIBA CMOS devices.

(2) Type classification (HC, HCU, HCT)

In the high speed CMOS, HC family, there are HCU types and HCT types in addition to the HC types. There differentiations were made by JEDEC in order to separate CMOS devices of the same function but with different input levels or the existence of a buffer.

TYPE	Internal stages	Input threshold voltage
HC	Two stages and above	CMOS level
HCU	One stage	CMOS level
HCT	Two stages and above	TTL level

Taking an inverter as an example, we can show the difference between these types as follows:

	TC74HC04A	TC74HCU04A	TC74HCT04A
Logic Diagram			
Input–Output Voltage transfer characteristics			

(3) Function

Functions are expressed by English number of two to five figures.
In the case of TC74HC series, these numbers are the same as LSTTL and 4000B/4500B devices having the same pin connections and function.

00～999 ····· Product with same pin connections and function as 74LS series.
(Example) 74LS240↔74HC240

4000～40199 ····· Product with same pin connection and function standard
4500～4599 CMOS 4000B/4500B series.
(Example) 40102B↔74HC40102

4300～4399 ····· Function unique to 74HC series.
7000～7999 However, some function approaches LSTTL or 4000B series.
(Example) Same function with 74HC7266A↔74LS266.
However, output is of normal buffer structure (Not open drain).

(4) Revision Level

This symbol is used to clarify the revision of product when improvements which will rechange the characteristics of product is made. Normally, it is blank, but if there is a revision, English characters are given successively from A. Safix A of TC74HCxxxA series indicate the types which have refined AC characteristics due to redesign of IC chip but still meet JEDEC standards for the family.

(5) Package Type

English characters showing type of package.

P ····· dual in line package (DIP) Plastic
F ····· 200 mil small outline IC (SOIC) Plastic
FN ····· 150 mil small outline IC (SOIC) Plastic

In the TC74HC series, narrow 300 mil type 24 pin DIP package was recently developed. With this developement, in the case of the P type, 14/16/20/24 pins devices all have a 300 mil width (7.62 mm width).

(6) Other information

For example, in the case of SOIC Tape and Reel specifications, the following indicators are added to the part name:

−TP 1 or −TP 2	Adhesive Tape and Reel (Difference in pin 1 position)
−EL	Embossed Tape and Reel

4. EXPLANATION OF RATINGS AND STANDARDS

4-1 Maximum Ratings

In general, the maximum rating value should not be exceeded in order to guarantee the life and reliability of integrated circuit products.

Absolute Maximum Rating should not be exceed even for a moment.

When the device is used in excess of any maximum rating, the device may not recover, and, in many cases, permanent damage will occur.

In designing the circuit, therefore, it is necessary to pay attention to the fluctuation of supply voltage, characteristics of interconnecting parts, ambient temperature, and surges in input and output signal lines, so that the maximum ratings will not be exceeded.

Table 4-1 indicates common absolute maximum ratings of TC74HC series. When the maximum ratings and common ratings differ, the former shall control. For definition of parameters, refer to Table 4-2.

Table 4-1 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25 (standard type) ± 35 (buffer type)	mA
DC V_{CC}/Ground Current	I_{CC}	± 50 (standard type) ± 75 (buffer type)	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

* 500mW in the range of Ta=−40℃～ 65℃. From Ta=65℃to 85℃ a derating factor of−10mW/℃ shall be applied until 300mW.

Table 4–2

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	Indicates the voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
DC Input Voltage DC Output Voltage	V_{IN} V_{OUT}	Indicates the voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
Input Diode Current Output Diode Current	I_{IK} I_{OK}	Indicates the current value at which the IC does not present breakdown due to latch–up when input current or output current flows. * Practically, the design in which DC current flows is not recommended. When a flow of curent cannot be prevented, adopt a current value lower than this.
DC Output Current DC V_{CC}/Ground Current	I_{OUT} I_{CC}	Output current indicates the current value which can flow from one output. As V_{CC}/GND current includes output current, in the case of an IC having many output terminals, substantial V_{CC}/GND current can flow.
Power Dissipation	P_D	Indicates consumption power not causing breakdown of the over the entire operating temperature range.
Storage Temperature	T_{stg}	Indicates the ambient temperature range not causing deterioration of characteristics and a relisbility when left for a long time in a state without supply voltage.
Lead Temp. and Time	T_L	Indicates the conditions when soldering is carried out after IC mounted on printed board.

4–2 Recommended Operating Condition

These are the conditions in which the operation of the TC74HC series is guaranteed, and when exceed, operation is not guaranteed even if it is within the maximum rating of Table 4–1.

Common recommended operating conditions of 74HC series are shown in Table 4–3. When recommended operating conditions of each device and common recommended operating conditions differ, the former shall control. As for the meaning of each item, refer to Table 4–4.

Table 4–3 Common Recommended Operating Conditions

(a) 74HC Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

(b) 74HCT Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

Table 4−4

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	Indicates supply voltage range guaranteeing normal operation of the IC.
Input Voltage Output Voltage	V_{IN} V_{OUT}	Indicates supply voltage range guaranteeing normal operation of the IC.
Operating Temperature	T_{opr}	Indicates operating temperature range guaranteeing normal operation and electrical characteristics of the IC.
Input Rise and Fall Time	t_r, t_f	Indicates rise and fall time range of input signal which will not cause malfunction due to oscillation of the output.

4−3 DC characteristics

Table 4−5 shows DC characteristics of HC types. For the meaning of each parameter, refer to Table 4−7. Table 4−5 is a standard DC characteristics table, and when it differ from individual characteristics, the later shall control. DC characteristics are regulated by JEDEC (Standard 7A). In the TC74HC series, all devices meet or exceed this standard.

Table 4−6 indicates characteristics table standardized by JEDEC.

Table 4–5 TC74HC series DC Characteristics Table

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level * * Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level * * Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA*	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA*	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA*	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA*	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current**	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	−	−	1.0	−	10.0	
			FF	6.0	−	−	2.0	−	20.0	
			MSI	6.0	−	−	4.0	−	40.0	

Note) * Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}|$=I_{OL}=6mA, 7.8mA)
** Items guaranteed to exceed JEDEC standard 7A.

Table 4-6 JEDEC Standard No.7A (DC Electrical characteristics)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.3	−	0.3	V
				4.5	−	−	0.9	−	0.9	
				6.0	−	−	1.2	−	1.2	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	−	−	1.9	−	V
				4.5	4.4	−	−	4.4	−	
				6.0	5.9	−	−	5.9	−	
			I_{OH} =−4 mA*	4.5	3.98	−	−	3.84	−	
			I_{OH} =−5.2mA*	6.0	5.48	−	−	5.34	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	−	0.1	−	0.1	V
				4.5	−	−	0.1	−	0.1	
				6.0	−	−	0.1	−	0.1	
			I_{OL} =4 mA*	4.5	−	−	0.26	−	0.33	
			I_{OL} =5.2mA*	6.0	−	−	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	−	−	2.0	−	20.0	
			FF	6.0	−	−	4.0	−	40.0	
			MSI	6.0	−	−	8.0	−	80.0	

Note) * Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}|$=I_{OL}=6mA, 7.8mA)

Table 4–7

Parameter	Symbol	Explanation
High–Level Input Voltage	V_{IH}	This is an input voltage capable of setting the input of the IC to a high level, and the minimum value is guaranteed. Judgement in this case is made by confirming that it is above the prescribed V_{OH} when output voltage should be at a high level, and below the prescribed V_{OL} when output voltage should be at a level.
Low–Level Input Voltage	V_{IL}	This is an input voltage capable of setting the input of the IC to a low level, and the maximum value is guaranteed. The method of judgement is the same as V_{IH}.
High–Level Output Voltage	V_{OH}	This is an output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the output level goes high. In this case, there is guaranteed a minimum value of output voltage obtainable when the specified output current (I_{OH}) flows out.
Low–Level Output Voltage	V_{OL}	This is an output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the output level goes low. In this case, there is guaranteed a maximum value of output voltage obtainable when the specified output current (I_{OL}) flows out.
Input Leakage Current	I_{IN}	This is the current flowing at the input terminal when a voltage is impressed on the input terminal of IC. Normally, this current is so small that measurement is made with the maximum value of supply voltage.
3–State Output Off–State Current	I_{OZ}	This is the leakage current flowing at the output terminal when the output is in a high impedance state, the device having a three state output or open drain output.
Quiescent Supply Current	I_{CC}	This is the current flowing from V_{CC} terminal into the IC when V_{CC} or GND level is held constant without changing the input voltage. The maximum value under all theoretical conditions allowable for the measured IC is guaranteed.

4–4 AC Characteristics

AC characteristics guarantee transient characteristic of products.

In general, impressed input waveform is set so as to have an amplitude of V_{CC} to GND and rise and fall time of 6ns.

Table 4–8 explains the meaning of each parameter of the AC characteristics, Fig. 4–1 shows the output connection diagrams for measurement and Fig. 4–2 illustrates the measured waveforms.

Table 4–8

Parameter	Symbol	Explanation	Drawing NO.	
			HC	HCT
Output Transition Time	t_{TLH} t_{THL}	Indicates the time during which the output voltage (V_{OH}, V_{OL}) rises from 10% to 90%, and the time during which the output voltage falls down from 90% to 10%.	(i)	(iv)
Propagation Time	t_{pLH} t_{pHL}	Indicates the time between input signal appliation and output response detection. t_{pLH} is the case in which the output changes from low level to high level, and t_{pHL} is the case in which the output changes from high level to low.		
Output Disable Time	t_{pLZ} t_{pHZ}	Indicates the time, between when signal is applied to the output control terminal and 3 state output is set to a high impedance state.	(iii)	(vi)
Output Enable Time	t_{pZL} t_{pZH}	Indicates the time, between when signal is applied to the output control terminal and 3 state output becomes a low or high level from the high impedance state.		
Maximum Clock Frequency	f_{MAX}	Indicates the maximum frequency at which the IC operates normally.	(ii)	(v)

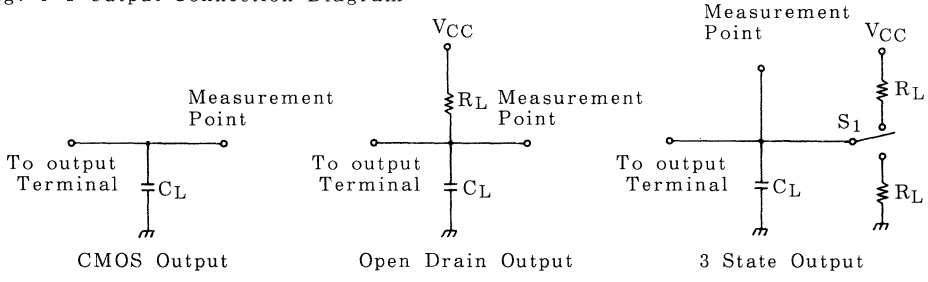
Timing requirements are a prerequisite to the normal function of devices. (See Table 4–9)

Table 4-9

Parameter	Symbol	Explanation	Drawing NO.	
			HC	HCT
Minimum Set-up Time	t_s	Regarding certain data, indicates the time in which the data must be applied and held before the input regarding that data (clock, etc.) changes. For example, when the data is read in at a rise of next clock pulse, it is necessary to apply data before the rising edge of the clock pulse, to a value at least equal to the minimum value of ts.	(ii)	(v)
Minimum Hold Time	t_h	Regarding certain data, indicates the time in which the data must be held after the input regarding that data (clock, etc.) has changed.		
Minimum Removal Time	t_{rem}	Indicates the minimum time after releasing of an asynchronous input (clear, preset, etc.) and until application of next input (clock, etc.).		
Minimum Pulse Width	t_w	Indicates the minimum pulse width that a clock input, etc. is acceptable as a normal signal.		
Clock Frequency	f	Indicates the clock frequency that is operated the IC normally.		

Perameter	Symbol	Explanation
Input Capacitance	C_{IN}	Indicates the capacitance between input and GND.
Output Capacitance	C_{OUT}	Indicates the capacitance associated with a 3 state output or a open drain output in the high impedance state.

Fig. 4-1 Output Connection Diagram

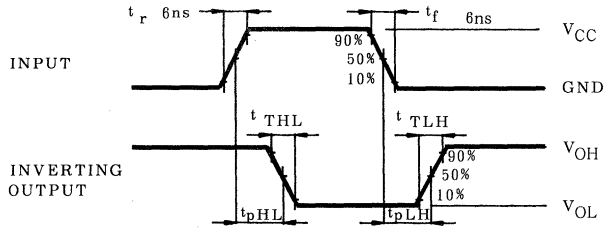


Note) C_L includes the capacitance of probe, etc.

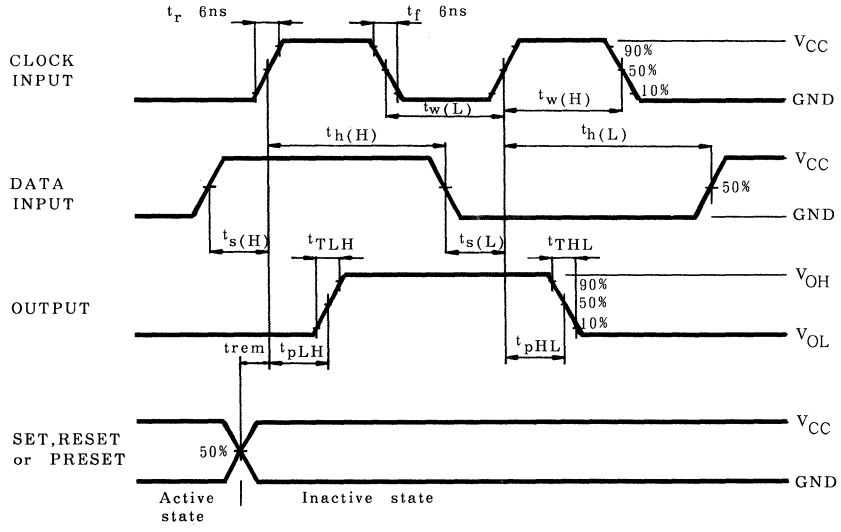
Fig. 4-2 Switching Characteristics Test Waveform

(1) HC Type

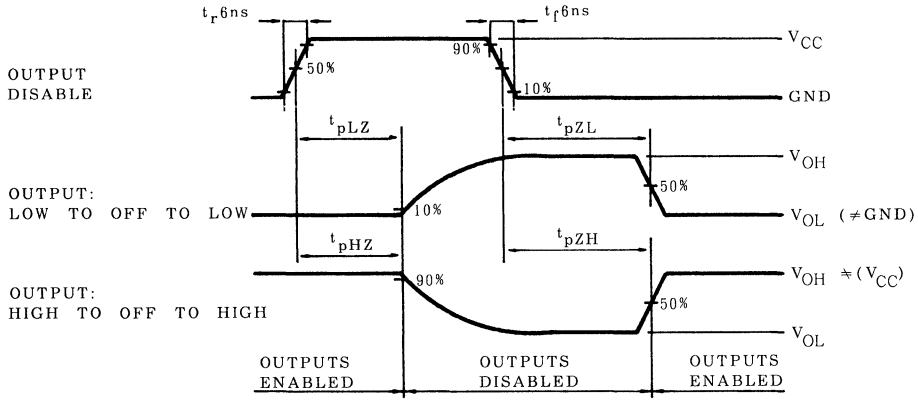
i) t_{TLH} , t_{THL} , t_{pLH} , t_{pHL}



ii) t_w , t_s , t_h , t_{rem}

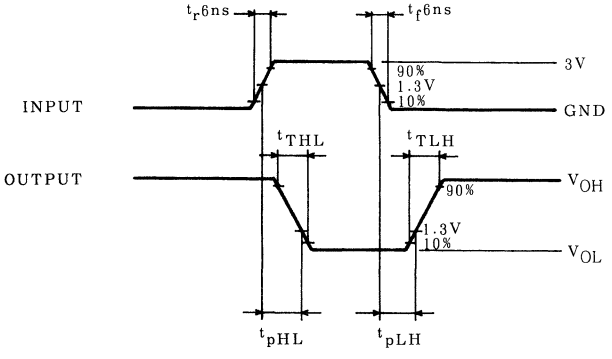


iii) t_{pLZ} ,t_{pHZ} ,t_{pZL} ,t_{pZH}

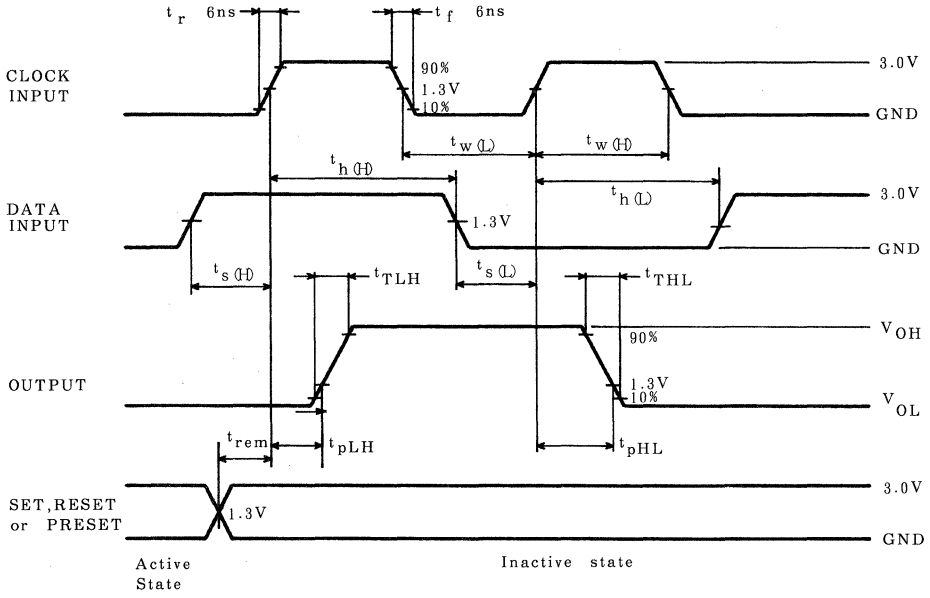


(2) HCT Type

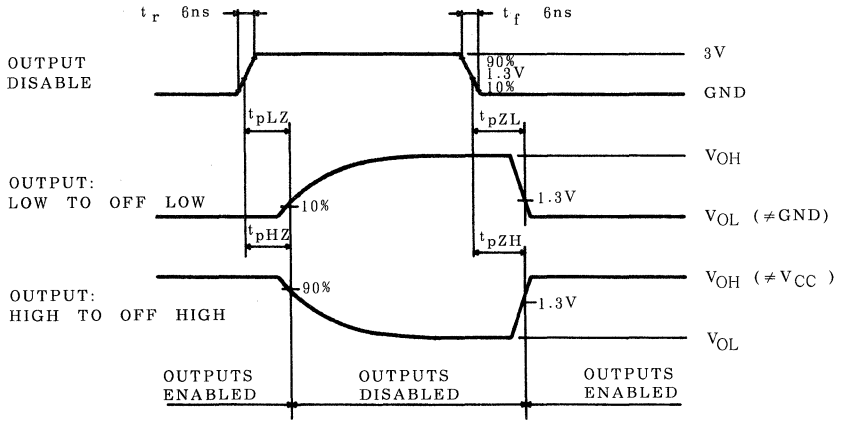
iv) t_{TLH} ,t_{THL} ,t_{pLH} ,t_{pHL}



V) t_w, t_{su}, t_h, t_{rem}



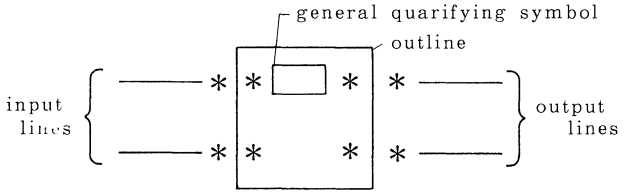
vi) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



5. EXPLANATION OF IEC LOGIC SYMBOLS

5-1 Symbol composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols. The purpose of a general qualifying symbol is to accurately portray the logic function of the device.

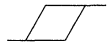
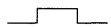
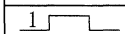
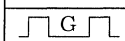
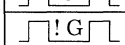
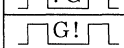


*: qualifying symbol locations for inputs and outputs

5-2 Qualifying Symbols

(1) General Qualifying Symbols

symbol	definition
&	**AND element**
≥1	**OR element**
=1	**EXCLUCIVE OR element**
=	**Logic identify element. If all inputs have the same logic state then the output is at internal logc "1".**
2K	**Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1".**
2K+1	**Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1".**
1	**Buffer element without amplified output.**
▷ or ◁	**Buffer element with amlified output. The triangle points in the direction of signal flow.**

symbol	definition
	Schmitt–trigger. It has hysterisis characteristic.
	Retriggerable monostable element.
	Non–Retriggerable monostable element.
	Astable element
	Synchronous–starting astable element.
	Synchronous–stopping astable element.
SRGm	Shift register. "m" :number of bits.
CTRm	Binary counter. "m" :number of bits. cycle length:2
CTRDIVm	Counter with cycle length m.
RCTRm	Ripple carry counter. "m" :number of bits. cycle length:2
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer / data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P–Q	Subtractor.
CPG	Look–ahead carry generator.
π	Multiplier.
COMP	Comparator.
ALU	Arithmetic logic unit.
ROM	Read only memory.
RAM	Random access memory.
FIFO	First–in First–out memory.
I=0	When power is switched ON, the element goes to internal logic "0".
I=1	When power is switched ON, the element goes to internal logic "1".
	Delay element with specified delay times.

(2) Inputs and Outputs Qualifying Symbols

symbol	definition
	Logic negation at an input. An external logic "0"("1") produces an internal logic "1"("0").
	Logic negation at an output. An internal logic "0"("1") produces an external logic "1"("0").
	Porlarity indicator at an input. A "L"(Low) level active.
	Porlarity indicator at an output. A "L" level active.
	Porlaroty indicator at an input where the signal flow is from right to left.
	Porlaroty indicator at an output where the signal flow is from right to left.
	Indicator for direction of signal flow.
	Bidirection information flow (alternate).
	Dynamic input Positive logic. Negative logic. Porlarity indicate. The above transitions produce the internal logic active.
	Dynamic input Positive logic. Negative logic. The above transitions produce the internal logic active.
	Dynamic input Porlarity indicate. The above transitions produce the internal logic active.
	Non-logic connection.
	Input for analog signals.

(3) Symbols of the internal connection

symbol	definition
	A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left -hand side produces a transistory logic "1" at the right-hand side.
	Internal input (virtual). This input is always at internal logic "1" state unless this is overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated by dependency notation.

(4) Symbols inside the outline

symbol	definition
	Delayed output. The output change is delayed until the input that indicated the change returns to its initial external state or level.
	Schmitt trigger input.
	Open-drain output without internal pulled-up resistor.
	Open-drain output with internal pulled-up resistor.
	Open-source output without internal pulled-down resistor.
	Open-source output with internal pulled-down resistor.
	Three-state output.
	Bufferd output. (The triangle points in the direction of signal flow)
	Enable input.
J, K, D	Information inputs of disable elements.
R, S, T, C	Control inputs of disable elements.
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left. "m"=1,2,3,···, however, the number may be omitted when "m"=1.
	Counting input. Count-up or count-down are indicted by + and − respectively. The number "m" is the count per command and may be omitted when "m"=1.
	Bit-grouping symbol. "m" is the highest power of 2 in the group.
	Content input. The internal logic "1" sets the element to the value "m".
	Content output. For example, when the input state is "1", the internal registor sets "9".
	Line-grouping symbol. The inputs enclosed by this symbol from a single logic input.
	Fixed-mode input, Fixed-state output. This input (output) is parmanently at internal logic "1".

5–3 Dependency Notation

Dependency notation is the powerful tool that makes IEC Logic Symbols compact and yet meaningful with IEC symbols, the relationships between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved.
In dependency notation, the terms "affecting" and "affected" are used.

(1) The general rules applied to dependency notation.

1) The input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved followed by an appropriately–chosen identifying number.

2) Each input or output affected by that affecting input (or output) is labelled with that same number.

3) If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs.

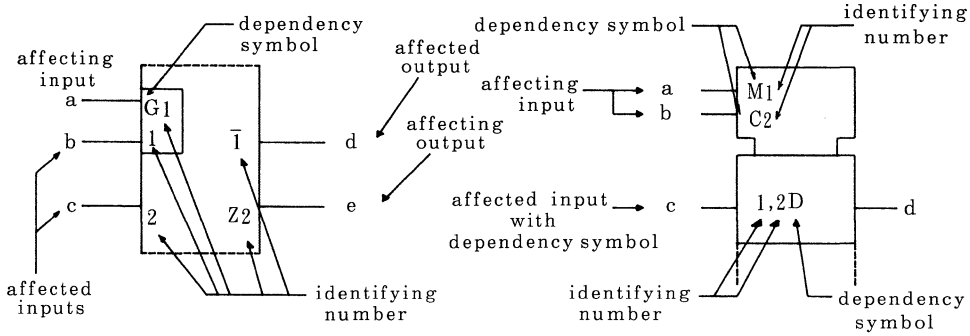
4) If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.

5) If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.

6) If the labels denoting the function of effected inputs or outputs are numbers (ex. outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greak letters.

7) If an input or output is affected more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships.

Fig. 5-1 Example for dependency notation



(2) Symbols for dependency notation

function	symbol	Input State "1"	Input State "0"
AND	G	Permits action	Imposes "0" state
OR	V	Imposes "1" state	Permits action
Negate (EX-OR)	N	Complements state	No effect
Interconnection	Z	Imposes action	Permits action
Control	C	Permits action	Prevents action
Set	S	S=1, R=0	No effect
Reset	R	S=0, R=1	No effect
Enable	EN	Permits action	Prevents action of input
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Adress	A	Permits action (Adress selected)	Prevents action (Adress not selected)

6. HOW TO READ MIL TYPE LOGIC SYMBOLS AND TRUTH TABLES

6-1 How to read MIL type Logic Symbols

Table 6-1 shows the MIL type logic symbols used in high-speed CMOS IC. This logical chart is based on MIL-STD-806B, and clocked inverter and transmission gate employ specific symbols.

Table 6-1 MIL Logic Symbols

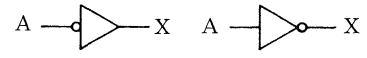
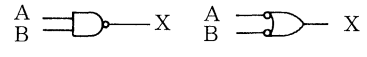
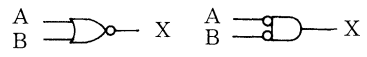
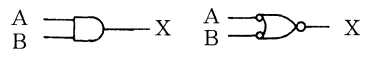
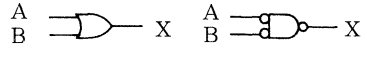
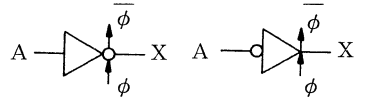
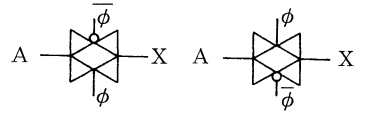
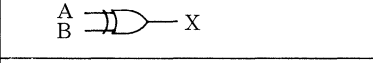
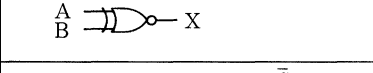
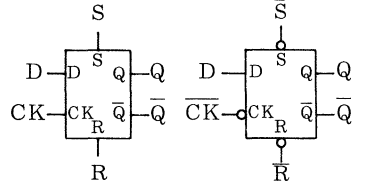
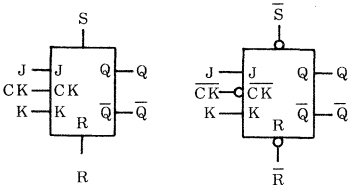
Circuit Function	Logic Symbol	Logical Equation or Truth Table
Inverter		$X=\overline{A}$
NAND Gate		$X=\overline{A \cdot B}=\overline{A}+\overline{B}$
NOR Gate		$X=\overline{A+B}=\overline{A} \cdot \overline{B}$
AND Gate		$X=A \cdot B=\overline{\overline{A}+\overline{B}}$
OR Gate		$X=A+B=\overline{\overline{A} \cdot \overline{B}}$
Clocked Inverter (Note 1)		ϕ | A | X H | H | L H | L | H L | X | Z X:Don't Care Z:High Impedance
Transmission Gate (Note 2)		ϕ | A | X H | H | H H | L | L L | X | Z X:Don't Care Z:High Impedance
EXCLUSIVE-OR Gate		$X=(A+B) \cdot (\overline{A}+\overline{B})$
EXCLUSIVE-NOR Gate		$X=(A \cdot B)+(\overline{A} \cdot \overline{B})$
D-Type Flip-Flop		S | R | D | CK | Q H | L | X | X | H L | H | X | X | L L | L | H | ↑ | H L | L | L | ↑ | L L | L | X | ↓ | Qn△ X:Don't Care △:No Change

Table 6-1 (Cont'd)

Circuit Function	Logic Symbol	Logical Equation or Truth Table
J/K Type Flip-Flop		See below

S	R	J	K	CK	Q
H	L	X	X	X	H
L	H	X	X	X	L
L	L	L	L	↓	Qn△
L	L	L	H	↓	L
L	L	H	L	↓	H
L	L	H	H	↓	$\overline{Qn}$▽
L	L	X	X	↑	Qn△

X:Don't Care
△:No Change
▽:Toggle

Note 1) Clocked Inverter

A clocked inverter has the circuit shown in Fig. 6-1. In this figure, Q1 and Q2 are P-channel MOS FET, and Q3 and Q4 are N-channel MOS FET, and four FET are all connected in series from V_{CC} to GND.

If ϕ signal is at a high level, Q1 and Q4 turn on, and can be regarded as simply a inverter composed of Q2 and Q3. When ϕ signal is at a low level, both Q1 and Q4 turn off, and regurdless of the condition of the A input, the output, B is set to a high impedance condition cut off from both V_{CC} and GND.

That is to say, a clocked inverter can be used as a switch to turn off input and output.

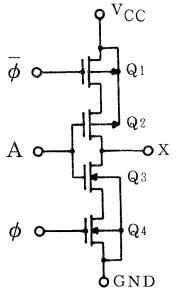


Fig. 6-1 Clocked Inverter

Note 2) Transmission Gate

Transmission gate has the circuit shown in Fig. 6-2. As shown in this figure, Q1 is a P-channel MOS FET and Q2 is an N-channel MOS FET which are connected in parallel.

If ϕ signal is at a high level, both Q1 and Q2 turn on, and a signal can be applied in either direction.

If ϕ signal is at a low level, both Q1 and Q2 turn off, and no signal can be passed.

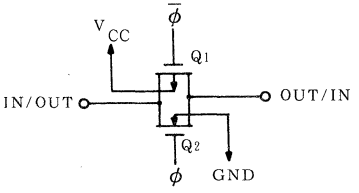


Fig. 6-2 Transmission Gate

6–2 How to Read Truth Table

Table 6–2 indicates the definition of symbols described in Truth Table.

Table 6–2

Symbol	definition
H	High level (Indicates stationary input or output)
L	Low level (Indicates stationary input or output)
	Indicates leading edge changing from "L" to "H".
	Indicates trailing edge changing from "H" to "L".
X	Don't cate (Either "H" or "L")
Z	High impedance state
a ····· h	Input level of stationary state of each input of A to H.
Q_0	Level of Q just before the realization of input condition indicated in Truth Table.
Qn	Level of Q just before inputting of active edge ( or )
	One "H" level pulse.
	One "L" level pulse.

7. COMMON ELECTRICAL CHARACTERISTICS

7-1 Power Dissipation

The power dissipation of CMOS device is composed of two components: one static, the other dynamic.

The total power dissipation is the sum of static and dynamic power dissipation.

Static power dissipation is obtained by multiplying quiescent supply current by the supply voltage range.

Dynamic power dissipation is obtained by taking the following operating supply current value.

(1) Static power dissipation

In the case of CMOS ICs, under the condition in which inputs are fixed at V_{CC} or GND level, either N-channel FET or P-channel FET turns off. For this reason, the current from V_{CC} to GND becomes only the reverse-direction saturated current of the PN junction and the surface leakage current due to the stain in the chip surface, and is a current of less than several nA at room temperature.

Therefore, in the case where the inputs are driven by another CMOS, or the inputs are pulled-down to GND or pulled-up to V_{CC} , the static power dissipation can be obtained as follows:

$$P_{d\ (DC)} = V_{CC} \cdot I_{CC}$$

For HCT devices where specific input pins are driven at LSTTL levels the following applies:

When being driven with a TTL V_{OH} , HCT devices exhibit additional currents (I_C) as specified on HCT device data sheets.

Therefore, the HCT static power dissipation is dependent on the number of inputs applied with the TTL V_{OH} logic voltage level, and can be obtained as follows:

$$P_{d\,(DC)} = V_{CC} \cdot I_{CC} + nV_{CC} \cdot I_{Cn} \cdot dn$$

n : the number of input at 0~2.4V (TTL V_{IH} level)

d : duty cycle

I_C: quiescent current when V_{IH} =2.4V

(Ref. Technical data sheets)

(2) Dynamic power dissipation

The dynamic power dissipation of a MOS IC is calculated by summing "a" and "b" below:

a) The switching current obtained by charge and discharge of each capacitance added to gate output current when the gate in the circuit including the output buffer makes an inversion.

b) The through current flowing when the P-channel FET and the N-channel FET which constitute the gate during inversion time turn on briefly at the same time.

When rise and fall times of the input signal are small (about 6ns), through current of the gate is usually negligibly small in comparison with the switching current.

For this reason, the dynamic supply current is governed by internal capacitance of the IC and the charging and discharging current of the load capacity (C_L).

An example is given here for C_L = 0pF.

For the inversion of internal gate outputs from low to high level, it is necessary that the electric charge corresponding to $Ci \cdot V_{CC}$ be supplied from the V_{CC} line to the internal capacitance Ci.

Therefore the value obtained by multiplying $Ci \cdot V_{CC}$ to the output inversion frequency (Frequency:f) within a certain period corresponds to the mean current to be supplied from the V_{CC} line to the IC during that period.

In an actual IC, several gates operate simultaneously, and their respective internal capacity and inversion frequency are different.

Therefore, dynamic supply current in an IC is as follows:

$$I_{CC}\ (opr.) = V_{CC} \cdot \sum_{1}^{n} f_n \cdot Ci_n$$

fn: frequency of internal operated gate

As fn is divisible by an integer of input frequency (f_{IN}), the gate operating with fn/m frequency can be considered equivalently as the capacitance of Ci/m.

Hence, the above equation can be rewritten as:

$$I_{CC}\ (opr.) = V_{CC} \cdot f_{IN} \cdot \sum_{1}^{n} Ci/m_n$$

f_{IN} : input frequency

m: integer

The final term is defined as C_{PD}.

Dynamic power dissipation with load capacity is given by the following equation:

$$P_D \text{ (opr.)} = C_{PD} \cdot V_{CC}{}^2 \cdot f_{IN} \cdot C_{PD}$$

Total dynamic power dissipation with load capacity is given by the following equation:

$$P_D \text{ (opr.)} = C_{PD} \cdot V_{CC}{}^2 \cdot f_{IN} + \sum_{1}^{n} (C_L n \cdot V_{CC}{}^2 \cdot f_O n)$$

C_L : load capacity
f_O : output frequency
n : integer of output

However, in specific applications such as crystal oscillators, supply current characteristics are controlled by through current, and the calculation result by C_{PD} can not be used.

7–2 Standardized Capacitance Power Dissipation (C_{PD}) Test Procedure

The purpose of the C_{PD} value is to allow the user to estimate actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basic, the remaining are measured on a "per device" basis. Each devices unique set up is listed in the Table 7–1, "Pin condition Table".

Measurements for all devices are to be made at V_{CC}=5.0V at Ta=25℃ and, if the devices are tested at a enough high frequency, the DC supply current will contribute a negligible amont to the overall power consumption and can thereby ignored. For this reason, the power consumption is measured at 1MHz. Any device with 3–state outputs is measured in an enabled state of outputs.

In order to determine the C_{PD} of a single section of a device (i.e., one of four gates or one of two flip–flops in a package), the following procedures should be used.

As for the C_{PD} value for a device with a common clock, it can be easily obtained by measuring both the C_{PD} of a device with only one portion of the device active, and the C_{PD} found with all portions of the device active. The C_{PD} value obtained by above two conditions should be shown.

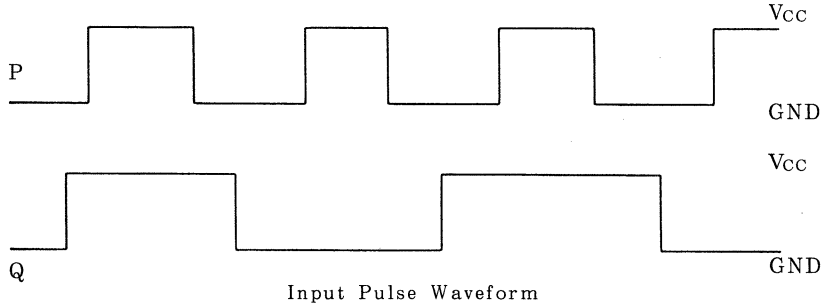
Gates:	Switch one input while biasing the remaining input(s) so that the output(s) will switch.
Flip–flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Latches:	Switch the enable and data inputs such that the latch toggles.
Decoders/ Demultiplexers:	Switch one address pin which changes two outputs
Date selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.

Analog switches:	Switch one address/select pin which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance as shown above.
Counters:	Switch the clock with the other inputs biased so that the device counts.
Shift registers:	Switch the clock while alternating the inputs so that the device shifts alternation 1's and 0's through the register.
Transceivers:	Switch only one data input. Place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Display Drivers:	Switch one input so that approximately one-half of the outputs change state.
ALUs/Address:	Switch the least significant bit. Bias the remaining inputs so that the device is alternately adding 0000(binary) or 0001(binary) to 1111(binary).

Details of each IC's pin condition are listed in Table 7-1.

-Explanation of symbol-

V = V_{CC} (+5.0V)
G = GND (0 V)
H = logic 1 (V_{CC})
L = logic 0 (GND)
X = don't care. V_{CC} or GND. but not switching
R = 1.0 kΩ pull-up resistor to an additional 5.0V supply other than V_{CC} supply
O = open
P = 50% duty cycle input pulse (shown below)
Q = 50% duty cycle half frequency out-of-phase input pulse (shown below)



Input Pulse Waveform

Table 7-1 C_{PD} Test Condition

Type No.		Pin																					
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
00		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
02		O	P	L	O	X	X	G	X	X	O	X	X	O	V	•	•	•	•	•	•	•	•	•	•
03		P	H	R	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
04		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
08		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
10		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
11		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
14		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
20		P	H	O	H	H	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
21		P	H	O	H	H	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
27		P	L	X	X	X	O	G	O	X	X	X	O	L	V	•	•	•	•	•	•	•	•	•	•
30		P	H	H	H	H	H	G	O	O	O	H	H	O	V	•	•	•	•	•	•	•	•	•	•
32		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
42		O	O	O	O	O	O	O	G	O	O	O	L	L	L	P	V	•	•	•	•	•	•	•	•
51		P	X	X	X	X	O	G	O	L	L	L	H	H	V	•	•	•	•	•	•	•	•	•	•
73		P	H	H	V	X	X	X	O	O	X	G	O	O	H	•	•	•	•	•	•	•	•	•	•
74		H	Q	P	H	O	O	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•
75		O	Q	X	X	V	X	X	O	O	O	O	G	P	O	O	O	•	•	•	•	•	•	•	•
76		P	H	H	H	V	X	X	X	X	O	O	X	G	O	O	H	•	•	•	•	•	•	•	•
77		Q	X	X	V	X	X	O	O	O	O	G	P	O	O	•	•	•	•	•	•	•	•	•	•
85		L	H	P	H	O	O	O	G	L	L	L	L	L	L	L	V	•	•	•	•	•	•	•	•
86		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
107		H	O	O	H	O	O	G	X	X	X	X	P	H	V	•	•	•	•	•	•	•	•	•	•
109		H	H	L	P	H	O	O	G	O	O	X	X	X	X	X	V	•	•	•	•	•	•	•	•
112		P	H	H	H	O	O	O	G	O	X	X	X	X	X	H	V	•	•	•	•	•	•	•	•
113		P	H	H	H	O	O	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•
123		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
125		H	P	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
126		H	P	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
131		Q	L	L	P	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
132		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
133		P	H	H	H	H	H	H	G	O	H	H	H	H	H	H	V	•	•	•	•	•	•	•	•
137		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
138		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
139		L	P	L	O	O	O	O	G	O	O	O	O	X	X	X	V	•	•	•	•	•	•	•	•
147		H	H	H	H	H	O	O	G	O	H	P	H	H	O	O	V	•	•	•	•	•	•	•	•
148		H	H	H	H	L	O	O	G	O	P	H	H	H	O	O	V	•	•	•	•	•	•	•	•
151		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
153		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•

Type No.		Pin																						
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
154		O	O	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V
155		L	L	L	O	O	O	O	G	O	O	O	O	P	L	L	V	•	•	•	•	•	•	•	•
157	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
157	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
158	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
158	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
160		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
161		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
162		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
163		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
164		Q	H	O	O	O	O	G	P	H	O	O	O	O	V	•	•	•	•	•	•	•	•	•	•
165		H	P	X	X	X	X	O	G	O	Q	X	X	X	X	L	V	•	•	•	•	•	•	•	•
166		Q	X	X	X	X	L	P	G	H	X	X	X	O	X	H	V	•	•	•	•	•	•	•	•
173	1*	L	L	O	O	O	O	P	G	L	L	X	X	X	O	L	V	•	•	•	•	•	•	•	•
173	4*	L	L	O	O	O	O	P	G	L	L	Q	Q	Q	Q	L	V	•	•	•	•	•	•	•	•
174	1*	H	O	Q	X	O	X	O	G	P	O	X	O	X	X	O	V	•	•	•	•	•	•	•	•
174	6*	H	O	Q	Q	O	Q	O	G	P	O	Q	O	Q	Q	O	V	•	•	•	•	•	•	•	•
175	1*	H	O	O	Q	X	O	O	G	P	O	O	X	X	O	O	V	•	•	•	•	•	•	•	•
175	4*	H	O	O	Q	Q	O	O	G	P	O	O	Q	Q	O	O	V	•	•	•	•	•	•	•	•
181		P	H	H	L	L	H	H	L	O	O	O	G	O	B	O	O	O	L	H	L	H	L	H	V
182		H	L	H	L	H	L	O	G	O	O	O	O	P	H	L	V	•	•	•	•	•	•	•	•
190		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
191		X	O	O	L	L	O	O	G	X	X	H	O	O	P	X	V	•	•	•	•	•	•	•	•
192		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
193		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
194		H	Q	X	X	X	X	X	G	H	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
195		H	H	L	X	X	X	X	G	H	P	O	O	O	O	O	V	•	•	•	•	•	•	•	•
221		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
237		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
238		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
242		L	O	P	X	X	X	G	O	O	O	O	O	L	V	•	•	•	•	•	•	•	•	•	•
243		L	O	P	X	X	X	G	O	O	O	O	O	L	V	•	•	•	•	•	•	•	•	•	•
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
251		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
253		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•
257	1*	P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•

* number of sections active

Type No.		Pin																						
		0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0	2 1	2 2	2 3	2 4
257	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
258	1 *	P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•
258	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
259		L	L	L	O	O	O	O	G	O	O	O	O	Q	P	H	V	•	•	•	•	•	•	•	•
266		P	L	B	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
273	1 *	H	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
273	8 *	H	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
279		L	P	P	O	X	X	O	G	O	X	X	X	O	X	X	V	•	•	•	•	•	•	•	•
280		L	L	O	L	O	O	G	P	L	L	L	L	L	L	V	•	•	•	•	•	•	•	•	•
283		O	H	L	O	P	H	L	G	O	O	H	L	O	L	H	V	•	•	•	•	•	•	•	•
298	1 *	L	L	H	L	L	L	L	G	L	Q	P	O	O	O	O	V	•	•	•	•	•	•	•	•
298	4 *	L	L	H	H	L	L	H	G	H	Q	P	O	O	O	O	V	•	•	•	•	•	•	•	•
299		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
323		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
352		L	L	X	X	L	H	O	G	O	L	L	X	X	P	X	V	•	•	•	•	•	•	•	•
353		L	L	X	X	L	H	O	G	O	L	L	X	X	P	X	V	•	•	•	•	•	•	•	•
354		X	X	X	X	X	X	L	H	L	G	L	L	L	P	L	L	H	O	O	V	•	•	•	•
356		X	X	X	X	X	X	X	Q	P	G	L	L	L	L	L	L	H	O	O	V	•	•	•	•
365		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
366		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
367		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
368		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
373	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
373	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
374	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
374	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
375		Q	O	O	P	O	O	Q	G	X	O	O	X	O	O	X	V	•	•	•	•	•	•	•	•
377	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
377	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
386		P	L	O	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
390		P	L	O	Q	O	O	O	G	O	O	O	X	O	X	X	V	•	•	•	•	•	•	•	•
393		P	L	O	O	O	O	G	O	O	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
423		L	P	H	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
533	1 *	L	O	Q	X	O	O	X	X	O	G	G	P	X	X	O	O	X	X	O	V	•	•	•	•
533	8 *	L	O	Q	Q	O	O	Q	Q	O	G	G	P	Q	Q	O	O	Q	Q	O	V	•	•	•	•
534	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
534	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
540	1 *	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
540	8 *	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•

* number of sections active

Type No.		Pin																						
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
541	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
541	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
563	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
563	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
590		O	O	O	O	O	O	O	G	O	H	P	H	P	L	O	V	•	•	•	•	•	•	•	•
592		X	X	X	X	X	X	X	G	O	H	P	H	X	H	X	V	•	•	•	•	•	•	•	•
593		O	O	O	O	O	O	O	O	H	G	O	H	P	L	H	X	H	L	H	V	•	•	•	•
595		O	O	O	O	O	O	O	G	O	H	P	P	L	Q	O	V	•	•	•	•	•	•	•	•
597		X	X	X	X	X	X	X	G	O	H	P	X	H	Q	X	V	•	•	•	•	•	•	•	•
620		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
623		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
643		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
646		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
648		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
651		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	X	X	V
652		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	X	X	V
670		Q	Q	Q	L	P	O	O	G	O	O	L	L	L	P	Q	V	•	•	•	•	•	•	•	•
688		L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	O	V	•	•	•	•
690		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
691		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
692		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
693		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
696		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
697		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
698		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
699		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
4002		O	P	L	L	L	O	G	O	X	X	X	X	O	V	•	•	•	•	•	•	•	•	•	•
4016		O	O	O	O	X	X	G	O	O	O	O	X	P	V	•	•	•	•	•	•	•	•	•	•
4017		O	O	O	O	O	O	O	G	O	O	O	O	L	P	L	V	•	•	•	•	•	•	•	•
4020		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V	•	•	•	•	•	•	•	•
4022		O	O	O	O	O	O	O	G	O	O	O	O	L	P	L	V	•	•	•	•	•	•	•	•
4024		P	L	O	O	O	O	G	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•	•	•
4028		O	O	O	O	O	O	O	G	O	P	X	X	X	O	O	V	•	•	•	•	•	•	•	•

* number of sections active

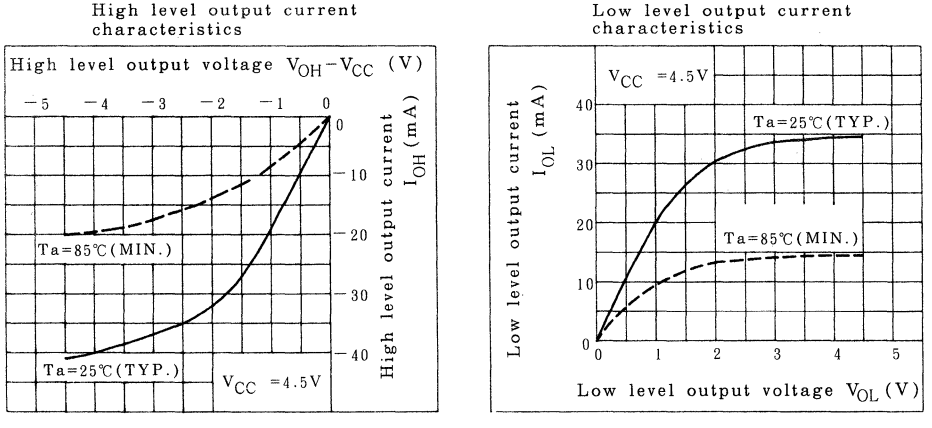
Type No.		Pin																						
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4040		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V	•	•	•	•	•	•	•	•
4049		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O	•	•	•	•	•	•	•	•
4050		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O	•	•	•	•	•	•	•	•
4051		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
4052		O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	•	•	•	•	•	•	•	•
4053		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
4060		O	O	O	O	O	O	O	G	O	O	P	L	O	O	O	V	•	•	•	•	•	•	•	•
4066		O	O	O	O	X	X	G	O	O	O	O	X	P	V	•	•	•	•	•	•	•	•	•	•
4072		O	P	L	L	L	O	G	O	X	X	X	X	O	V	•	•	•	•	•	•	•	•	•	•
4075		P	L	X	X	X	O	G	L	O	O	X	X	X	V	•	•	•	•	•	•	•	•	•	•
4078		O	P	L	L	L	O	G	O	L	L	L	L	O	V	•	•	•	•	•	•	•	•	•	•
4094		H	Q	P	O	O	O	O	G	O	O	O	O	O	O	H	V	•	•	•	•	•	•	•	•
4316		O	O	O	O	P	X	L	G	G	O	O	O	O	X	X	V	•	•	•	•	•	•	•	•
4351		O	O	O	O	O	O	L	H	O	G	H	P	L	O	L	O	O	O	O	V	•	•	•	•
4352		O	O	O	O	O	O	L	H	O	G	H	P	L	O	O	O	O	O	O	V	•	•	•	•
4353		O	O	O	O	O	O	L	H	O	G	H	P	L	O	L	O	O	O	O	V	•	•	•	•
4511		L	L	H	H	L	L	P	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
4514		H	P	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	L	L	L	V
4515		H	P	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	L	L	L	V
4518		P	H	O	O	O	O	L	G	X	X	O	O	O	O	X	V	•	•	•	•	•	•	•	•
4520		P	H	O	O	O	O	L	G	X	X	O	O	O	O	X	V	•	•	•	•	•	•	•	•
4538		G	R	H	P	H	O	O	G	O	O	X	X	L	O	G	V	•	•	•	•	•	•	•	•
4543		H	L	L	H	L	P	L	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
7007		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
7240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7266		P	L	O	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
7292		H	L	O	P	L	O	O	G	O	L	H	O	O	L	L	V	•	•	•	•	•	•	•	•
7294		H	L	O	P	L	O	O	G	O	O	H	O	O	L	L	V	•	•	•	•	•	•	•	•
7640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
7643		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
7645		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
40102		P	H	L	L	L	L	L	G	H	L	L	L	L	O	H	V	•	•	•	•	•	•	•	•
40103		P	H	L	L	L	L	L	G	H	L	L	L	L	O	H	V	•	•	•	•	•	•	•	•
40105		L	O	P	Q	Q	Q	Q	G	L	O	O	O	O	O	P	V	•	•	•	•	•	•	•	•

7–3 Output Current Characteristics

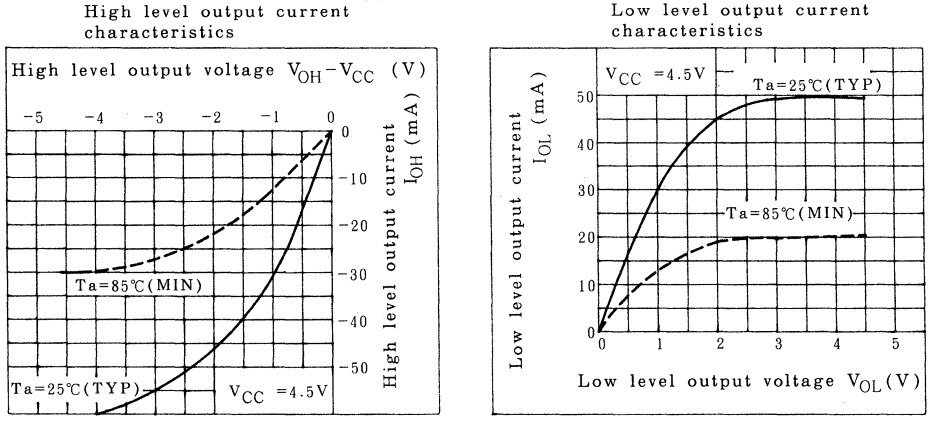
The output current characteristics of TC74HC series can be divided into standard and buffer types. An IC of the standard type is capable of directly driving 10 LSTTL, and guarantees $V_{CC} - V_{OH} \leqq 0.37V$, $V_{OL} \leqq 0.33V$ over the entire temperature range. The buffer type, is capable of directly driving 15 LSTTL under the same conditions.

Fig. 7–2 shows the standard output current characteristics of each type when used at the 4.5V.

Note) The solid line shows standard characteristics chart. Because there are variations depending upon the samples, use the broken line and separate standard values when making design.



(i) Standard Type



(ii) Buffer Type

Fig. 7–2 Standard Output Current Characteristics

When the structure of device has been decided upon, the current flowing in MOS FET is determined by gate voltage V_{GS} and voltage V_{DS} between source and drain. In the actual IC, the gate voltage of output step MOS FET becomes nearly V_{CC} and GND level. Therefore, if $|V_{GS}| = V_{CC}$ is considered, the following equation is realized in non-saturation zone:

$$I_{DS} = K \left[2 V_{DS} (V_{GS} - V_T) - V_{DS}^2 \right]$$

If V_{DS} is made constant, I_{DS} is proportional to $V_{CC} - V_T$. In the saturation zone:

$$I_{DS} = K (V_{GS} - V_T)^2$$

Thus, I_{DS} is proportional to $(V_{CC} - V_T)^2$ not to V_{DS} . Here, V_T is the threshold voltage proper to MOS FET's, and is set to a value of about 0.7V in TC74HC series.

Fig. 7-3 shows supply voltage-output current characteristics of standard type outputs. This figure shows standard values. Note that the variation of output current at low supply voltage becomes large in comparison with that at 4.5V.

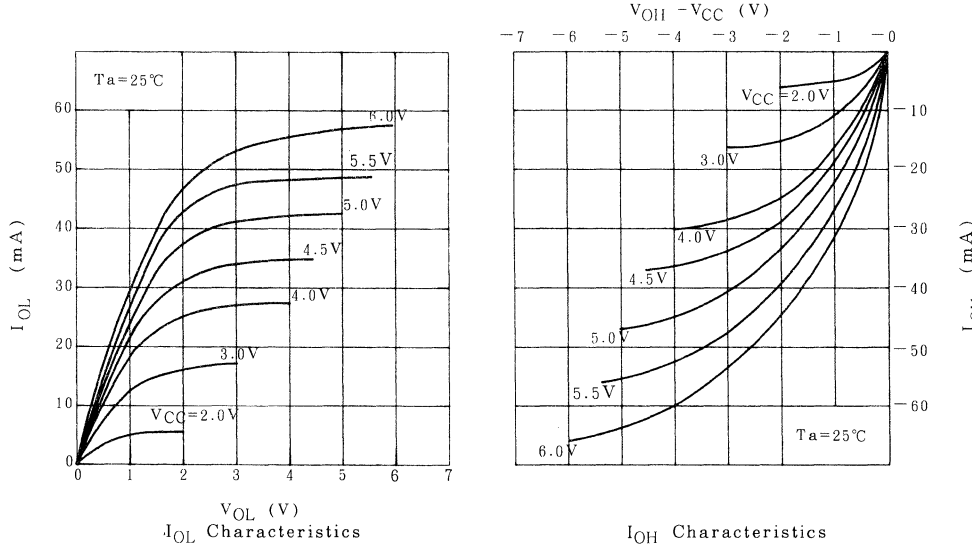


Fig. 7-3 Standard Output Current Characteristics

7–4 AC Electrical Characteristics

(1) Supply voltage dependence

Transient characteristics of IC's such as propagation delay time and maximum operating frequency are determined by delay time of the inner gate or rise time and fall time of the output buffer.

Internal delay is considered to be chiefly due to integral effect of the on resistance of the MOS FET and load capacitance does not remarkably depend upon supply voltage, the drain current characteristics of MOS FET determines the dependence of AC electric characteristics on supply voltage.

Fig. 7–4 shows the dependence on supply voltage of propagation delay time in a representative gate IC.

In JEDEC standard 7A, the coefficient of dependance on supply voltage is determine as follows: In the worst case, adopt the broken line indicated in Fig. 7–4 which was made on the basis of JEDEC standard.

Table 7–1 Calculation of AC Standard Value (expecting f_{MAX})

V_{CC}	Ta=25℃	Ta=−40∼85℃
2.0	5.00X	5.00Y
4.5	X	Y=1.25X
6.0	0.85X	0.85Y

Table 7–2 Calculation of f_{MAX} Standard Value

V_{CC}	Ta=25℃	Ta=−40∼85℃
2.0	0.20X	0.20Y
4.5	X	Y=0.80X
6.0	1.18X	1.18Y

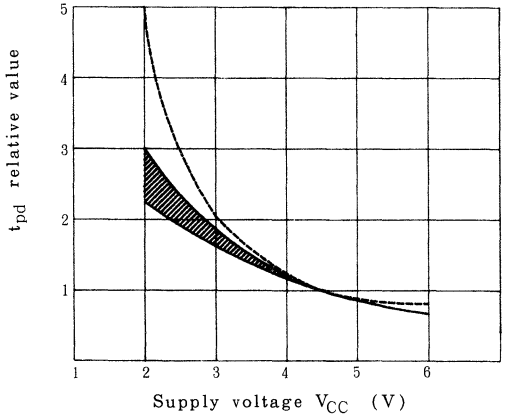


Fig. 7–4 Dependance on Supply Voltage of Propagation Delay Time (Gate IC)

(2) Load capacitance dependence

In TC74HC series, output current has been widely improved in comparison with the conventional 4000B/4500B series, and a capacitive load can be driven at high speed.

However, since output impedance is determined when supply voltage is selected, rise and fall time of output waveform or propagation delay time will increase in proportion to an increase of load capacitance.

Fig. 7–5 indicates the load capacitance dependence on output rise and fall time at a supply voltage of 4.5V. Fig. 7–6 shows the load capacitance dependence on propagation delay time.

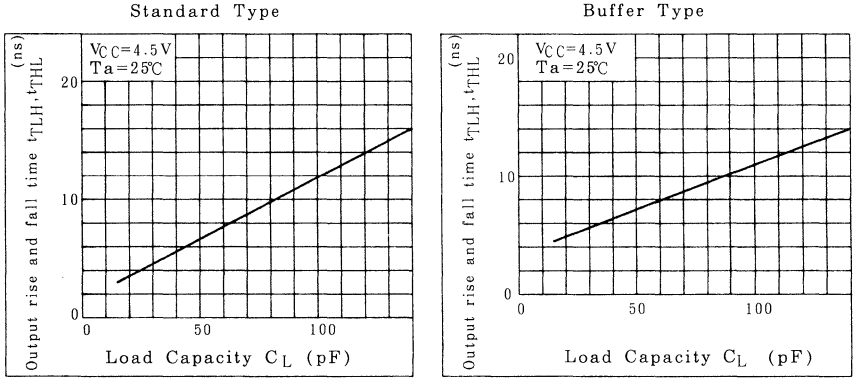


Fig. 7–5 Load Capacitance Dependence of t_{TLH}, t_{THL} (standard characteristics)

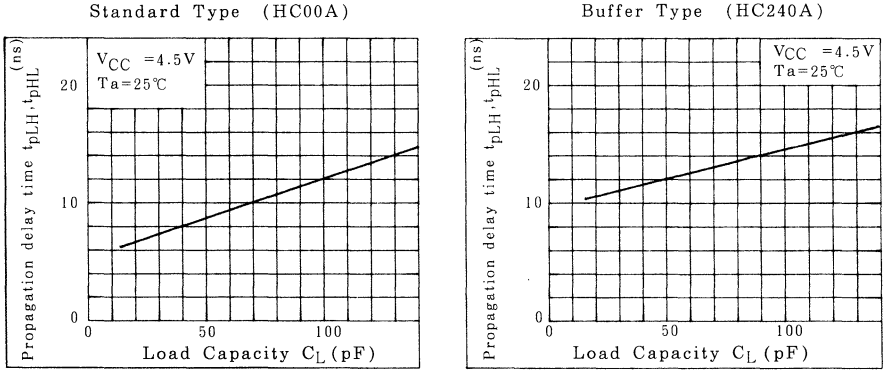


Fig. 7–6 Load Capacitance Dependence of t_{pLH}, t_{pHL} (standard characteristics)

In the TC74HC series, AC characteristics are guaranteed using a load capacitance of 50pF. Propagation delay time using load capacitance, other than the above is obtained by the following equation:

(Example) High level propagation delay time in the case of load capacitance of XpF.

$$t_{pLH}\ (X) = A\ (X - 50) + t_{pLH}\ (50)$$

A: High level propagation delay time increase rate per unit load capacitance(ns/pF)

Table 7-3 Load Capacitance Dependence of AC Electrical Characteristics (ns/pF)

		Standard Output		Buffer Output	
	V_{CC}	Typical value (Ta=25℃)	Limit value (Ta=25℃)	Typical value (Ta=25℃)	Limit value (Ta=25℃)
t_{TLH}, t_{THL}	2.0	0.33	0.83	0.22	0.55
	4.5	0.12	0.24	0.08	0.16
	6.0	0.09	0.16	0.06	0.11
t_{pLH}, t_{pHL}	2.0	0.17	0.43	0.13	0.33
	4.5	0.06	0.12	0.05	0.10
	6.0	0.043	0.077	0.038	0.068

Table 7-3 shows increase rate per unit capacity of AC electrical characteristics having load capacitance dependence.

In the case of a heavy capacitive load, it is necessary to make the calculation using the limit values in this table.

In TC74HCxxxA series, AC characteristice of 15pF load capacitance (standard output, V_{CC} =5.0V) or 150pF load capacitance (buffer output, V_{CC} =2, 4.5, 6V) is guaranteed. (See the technical data seets)

7–5 Temperature Parameters of Various Characteristics

In TC74HC series, operation over the wide temperature range of −40℃ to 85℃ is guaranteed. This section shows how the switching time and output current are influenced by temperature.

(1) Temperature Characteristics of Output.Current

Fig. 7–7 indicates temperature versus output current. In this figure, the solid line shows the temperature dependence in a standard sample. Therefore, when designing, use the broken line as it is the worst case.

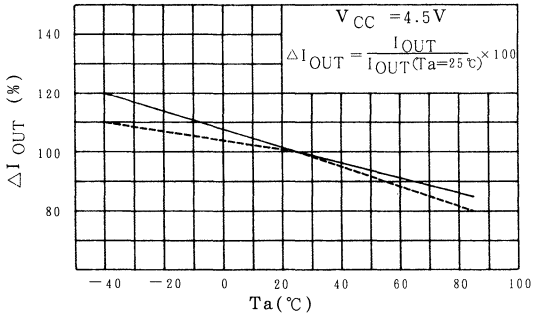


Fig. 7–7

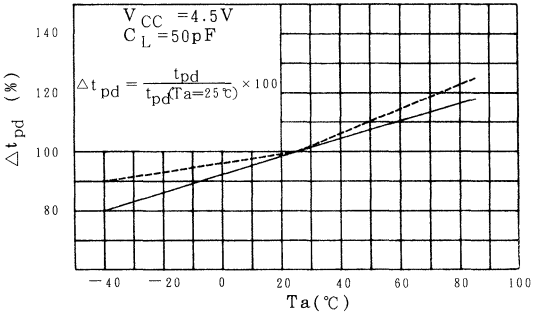


Fig. 7–8

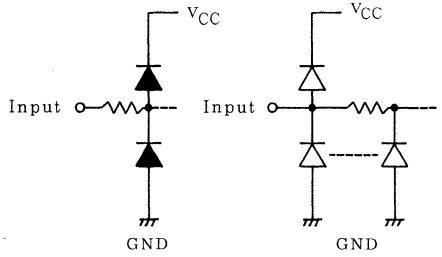
(2) Temperature Characteristics versus Propagation Delay Time

Fig. 7–8 shows temperature versus propagation delay time. The solid line in this figure indicates standard temperature dependence at the Gate of the IC. When designing, therefore, use the broken line indicated as the worst case.

8 PRECAUTIONS IN HANDLING

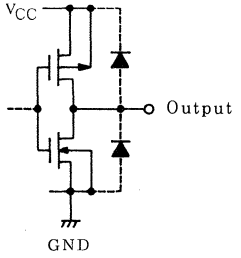
8-1 Electric Static Discharge

CMOS IC has a very thin gate insulation oxide film. When high voltage is applied to this gate electrode (input of CMOS IC), the oxide film directly under the gate can sometimes breaks down. In TC74HCxxxA series, as shown in Fig. 8-1, protect diodes are added to all input terminals in order to protect CMOS gate from such voltage. However, protective circuits may not necessarily be effective against accidental high voltage; care must be fully taken in handling CMOS IC's.



i) TC74HCxxx ii) TC74HCxxxA

Fig. 8-1 (a) Input Protective Circuits



(b) Output Equivalent Circuit

Further, as a parastic diode is formed between each terminal as indicated in Fig. 8-1, thermal breakdown, etc, due to excessive current may sometimes occur when the voltage exceeding the ratings is applied between each terminal.

Therefore, care must be taken at the time of assembling and adjustment.

(1) Electrostatic Discharge Test Method

Fig. 8-2 shows the electrostatic discharge test method. In Fig. 8-2, the test is conducted with C=200 pF, R=0 Ω. Table 8-1 shows the results of electrostatic discharge tests applied to a representative type of the TC74HC series.

In the test method, standardized by EIAJ, it is acknowledged that ±200V is sufficient to withstand damage in ordinary service. As shown be Table 8-1 Toshiba's TC74HC series has ample protection.

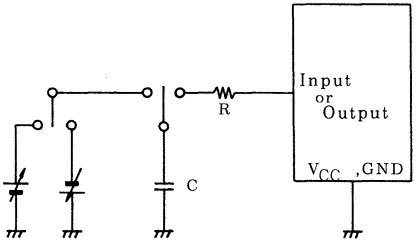


Fig. 8-2 Test Circuit

Table 8-1 Test Result

C=200pF, R=0Ω, Impression frequency 3 times

Name	Output		Input	
	Impression of + voltage	Impression of − voltage	Impression of + voltage	Impression of − voltage
TC74HC 00AP	> 500V	> −500V	> 500V	> −500V
TC74HC 02AP	> 500V	> −500V	> 500V	> −500V
TC74HC 74AP	> 500V	> −500V	> 500V	> −500V
TC74HC139AP	> 500V	> −500V	> 500V	> −500V
TC74HC240AP	> 500V	> −500V	> 500V	> −500V
TC74HC373AP	> 500V	> −500V	> 500V	> −500V

8-2 Precautions in Handling

(1) Transportation and Storage

As the input and output terminals of unmounted CMOS IC's are in a state of high impedance, they are apt to receive induction from the surrounding charged body, space electric fields, and the human body.

For this reason, it is necessary, in transporting and storing them, to use dielectric mats, metal cases or aluminum foil boxes, so that each terminal of the IC will be at same potential.

As the TC74HC series are inserted in magazines and are given antistatic treatment at the time of shipment, do not remove devices from the magazines unnecessaryly. Especially, avoid the use of plastic or vinyl containers which are apt to create static charges.

(2) Assembling

When installing CMOS IC on the printed wiring board, it is necessary to protect the electric equipment, working stand and operators from static electricity by grounding. It is advisable to ground the working stand by spreading a metal plate or aluminum foil on the surface. Grounding of operators should be made through a resistance of about 1MΩ so as to prevent electric shock. It is convenient to make grounding through a metallic ring or metallic wrist bands. Also, it is advisable to not wear working clothes make of chemical fibers. Further, it is necessary to periodically check electric equipment to insure absence of electric leakage.

When shaping the lead during the packaging of IC, it is advisable to use pincet or similar jig, so that stress may not be given to the device leads at the package entrance.

When storing or transporting the completely assembled printed wiring board, short circuit the terminals of printed wiring board or cover the entire board with aluminum foil, so that the input terminals of the IC are open.

(3) Soldering, washing

When soldering by use of a soldering iron, carry out the work at the temperature of 260℃ or below within 10 seconds. It is confirmed that the reliability of TC74HC series is not affected when subjected to a temperature stress at the lead of 260℃ for 10 seconds.

Use a soldering iron having no electrical leakage its end. It is recommended to use A class iron having insulation resistance exceeding 10MΩ. When using soldering tank, it is necessary to ground the tank so as to prevent the electric potential of the soldering tank from affecting the work.

After soldering, the IC's on the printed wiring board, cleaning is done to remove flux, etc. For this cleaning use a flux removing abluent or a cleaning method utilizing ultrasonic wave. Care must be taken in the selection of this solvent so as to prevent adverce effects to the package and marking of the CMOS IC.

In general, it is advisable to use Freon™ series cleaners.

When using ultrasonic cleaning, it is necessary to prevent stress due to resonance from being imparted to the IC or printed wiring board. Because of this, it is necessary to consider the method such that the main body becomes a shade against vibration, and also to use a cleaning time of less than 30 seconds.

(4) Adjustment, Test

When making adjustment and test after the completion of printed wiring board, it is necessary to check for solder bridge or cracks on the printed wiring board before application of supply power. As CMOS systems require only a small supply current, it is well to apply current limiting during test by using a constant voltage power source.

Before mounting or dismounting printed wiring boards into or out of the test fixture, always cut off the power supply.

When inspecting each part of the printed wiring board with a probe, care must be taken to prevent contact of the tip of the probe with other signal or power lines. It is advisable to install a special test pin for use with probes.

When the test is conducted under high proper and low temperature, it is necessary to ensure grounding of the constant temperature oven.

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9 PRECAUTIONS IN DESIGNING CIRCUITS

9–1 Input Processing

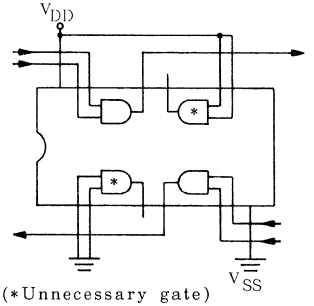
(1) Processing of unnecessary gate

Inputs of CMOS IC have such a high impedance that the logical level becomes undefined under open conditions. In this case, if input is at an intermediate level, the transistors of both P–channel and N–channel turn on, and unnecessary supply current flows.

Therefore, as shown in Fig. 9–1, be sure to connect unnecessary input lines to V_{CC} , GND or other inputs and the output to the logical level as determined by the inputs.

In the case of CMOS, if a soldered part has bad contact, a function of the system or an increase in supply current will occur. Therefore, care must be taken at the time of soldering.

Fig. 9–1 Treatment of Input



(*Unnecessary gate)

(2) Input processing of printed wiring board

When the input terminal of a printed wiring board is connected directly to a CMOS input, that input electrically floats. This condition is the same as a single IC being transported or stored. It is advisable, therefore, to connect this input to V_{CC} or GND through a resistance on the printed wiring board, as indicated in Fig. 9–2.

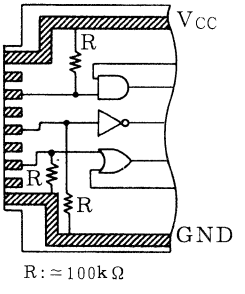


Fig. 9–2 Input processing of Printed Wiring Board

9–2 Design of Power Source

In general, CMOS has a small current consumption in comparison with bipolar digital IC's and, therefore, it need only a small capacity power supply. However, from the operational standpoint, CMOS consumes power in transition state, and therefore it is necessary to keep high frequency impedance of the power source at a low level.

It is advisable to make the wiring of the power source (V_{CC}) and GND lines thick and short, and insert, as a high frequency filter, a 0.001 μF to 0.1 μF capacitor between V_{CC} and GND for each IC.

Also, it is recommended to insert a capacitor of about 10 μF to 100 μF between power supply entrance and GND as low frequency filter. As mean supply current differs considerably depending u pon the operating frequency of the system, existence of capacitive load, rise and fall of the input signal and supply voltage attention must be especially given in the case of a simple power source by using a Zener diode, or by battery drive. When there is overshoot or undershoot during transition time of the supply power, use a filter, etc. so that the maximum rating is not exceeded.

9–3 On Output Short–circuit

In the TC74HC series, a buffer is added to the output, and both flow–out (I_{OH}) and flow–in (I_{OL}) current drive is possible. For this reason, excessive current flows in CMOS output when the high level output line is shorted to the GND line or the low level output line is shorted to the V_{CC} line. Particularly, when the supply voltage is high, I_{OH} and I_{OL} are excessive and may damage the device; therefore care must be taken not to cause output short circuit.

It is, of course, impossible to directly connect ordinary outputs together, but in the case of an IC which has a 3 state output, wired OR is permitted provided that more than two outputs are not enabled simultaneously.

Further, in order to improve drive capacity, it is possible to connect the gates in the same package as shown in Fig. 9–3.

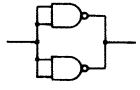


Fig. 9–3 Example of increase of driving capacity

9–4 Effect on Input of Slow Rise Time and Fall Time

When the waveform of slow rise fall time is impressed to CMOS input, it sometimes happens that output tends to oscillate around V_{TH} (threshold voltage of circuit) of input waveform. This is because the CMOS gate becomes a linear amplifier equivalent in the vicinity of V_{TH}, and minute power source ripple and noise components are amplified and appear in the output.

To prevent this, it is necessary to insert a high frequency filter capacitor between V_{CC} and GND of the oscillating IC, or use a Schmitt trigger IC.

In the case of TC74HC series, excepting HCU types or Schmitt trigger IC's, input rise and fall time is regulated as shown in Table 9–1.

Proper design requires that these rise and fall time limits be observed.

Fig. 9–4 shows an example of a malfunction when a shift counter is designed by using a type D flip–flop of another package. In this case, the malfunction is considered to be caused by the difference in circuit threshold level of separate D type flip flops.

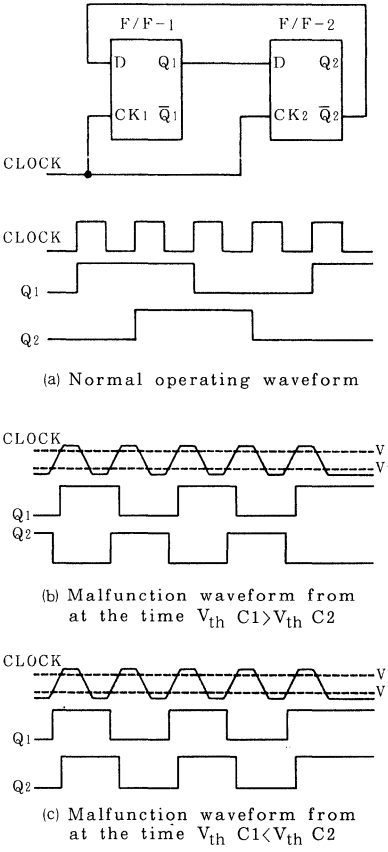


Fig. 9–4 Example of Malfunction

Let circuit threshold level of F/F–1 be V_{th} C1, and that of F/F–2 be V_{th} C2. Then, as shown in Fig. 9–4, time difference Δt is formed while the rising waveform of clock pulse cuts the respective circuit threshold voltage, and thus malfunction takes place.

The following condition is required for insuring normal operation:

$$\Delta t < t_{pd}\ (CK-Q) + t_{set-up}$$

In this case, there is a possibility of malfunction even though the input signal is within the standard value of Table 9–1. Therefore, care must be taken in design of sequence circuit clock inputs.

Table 9–1 Standard Value of Input Rise and Fall Time

Item	Symbol	Limit	Unit
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

9–5 Precautions for Wiring

(1) Output waveform distortion

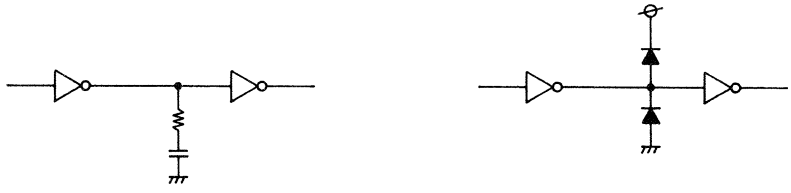
As, the output impedance of the TC74HC series is very low in comparison with conventional standard CMOS IC, distortion is somtimes caused in the output waveform depending upon the L component of the wiring, when the wiring connected to output end is long or when capacitance is connected between signal line and V_{CC} or GND. Therefore, when designing the printed wiring board, take care not to make signal wiring length too long. In the case of double sides printed wiring boards, it is ideal to limit signal wire length to 30cm or less. Especially, in the clock signal line, distortion of the waveform causes malfunction.

(2) Precautions for arrangement

The output of TC74HC series has a fast rise and fall time, and makes a full swing between V_{CC} – GND; therefore it become a noise source to other signals. It is desirous to locate the output separately from a part which is sensitive to the noise of an analog circuit. Also, care must be taken for the reduction the number of loads and curtailment of wiring length.

(3) Termination

From its physical and electrical characteristics, the TC74HC series is apt to cause overshoot and undershoot, and this leads to malfunction of the circuit or breakdown of passive IC's. These troubles can be prevented to some extent by terminating the end of signal line. Fig. 9–5 indicates examples o f general termination.



(a) Termination by CR (b) Termination by Diode

Fig. 9–5 Examples of Termination

9-6 Interface

(1) Input and output interface

When interconnecting a CMOS system, an exchange of signals with external circuits or mechanisms is usually done. These input and output signal lines are naturally made long in many cases, and have distributed inductance or reactance. Therefore, if directly connected to CMOS, they will give rise to various troubles.

Conceivable troubles may be the malfunction due to induced noise, and the destruction of the input/output element due to surge. To cope with these problems, reduction of signal line impedance (driving impedance) or insertion of noise eliminating circuit on the receiving side is done for the former, while surge protective measures are taken for the latter.

Fig. 9-6 illustrates an example of making noise and surge protection on the input side.
(a) and (b) of this figure show an example of absorbing noise by integrating the input waveform.
(c) and (d) indicate an example of protecting CMOS from input surge.

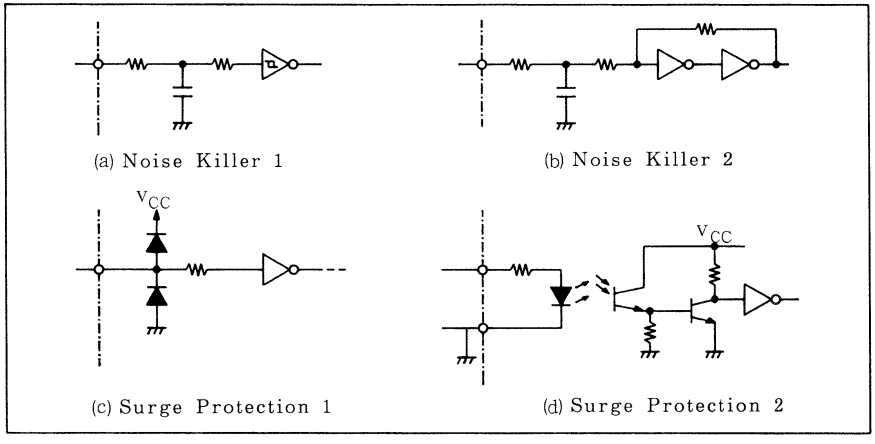


Fig. 9-6 CMOS Input Protective Circuits

Fig. 9-7 gives examples of output interface. There are other methods, but in any case, some protection should be given to an interface involving long signal line.

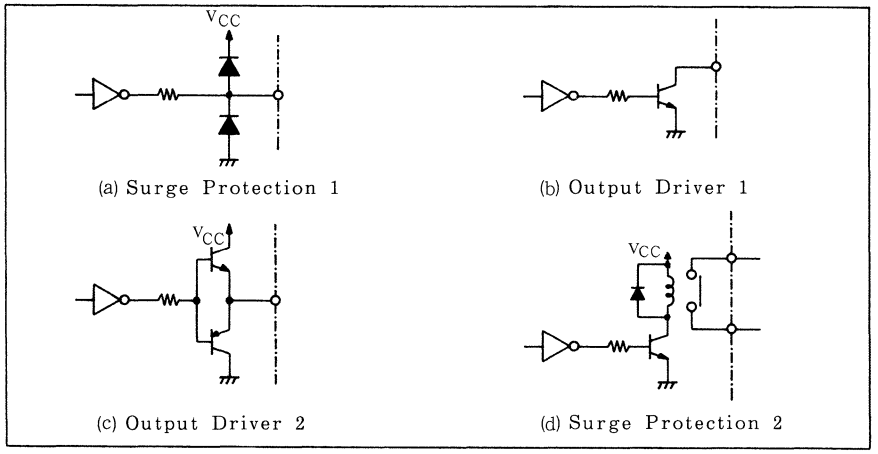


Fig. 9-7 Output Protection/Driving Circuits

(2) Interface of CMOS IC

In the case of the mutual interface between CMOS IC, input impedance of CMOS has so large value that the limitation of fan out may not be so large. However, there is actually a need to consider the fall of propagation time due to the adding effect of load capacitance and an increase of power consumption.

As input capacitance of CMOS is about 5pF per input, if 10 fan outs are taken for example, load capacitance 50pF, and further, the line capacitance on the printed wiring board must also be taken into account. This shows that the processing speed of system is controlled not only by the circuit constituants but also by fan out.

When constructing a system with CMOS IC, it is recommended to examine the fan out by taking these points into consideration.

(3) Interface between different CMOS families

The problem to be considered between different CMOS families is the difference of supply voltage requirements between families. When different CMOS families are used with the same power source, it is all right to pay attention to the problems due to the propagation delay time difference, but in the case of different power source, a voltage level converting circuit is needs.

Fig. 9–8 shows an interface method from the standard CMOS operating at 6V~15V to 74HC. The most popular method is to use CMOS (4049B/4050B) which has a level shift function as shown in this figure.

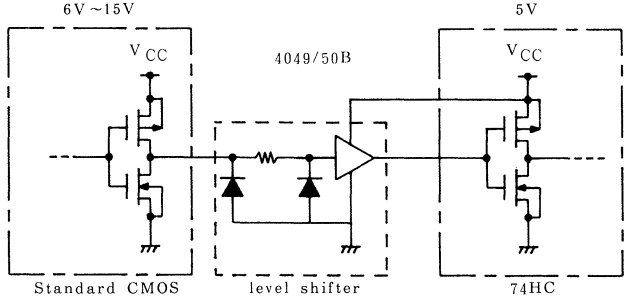
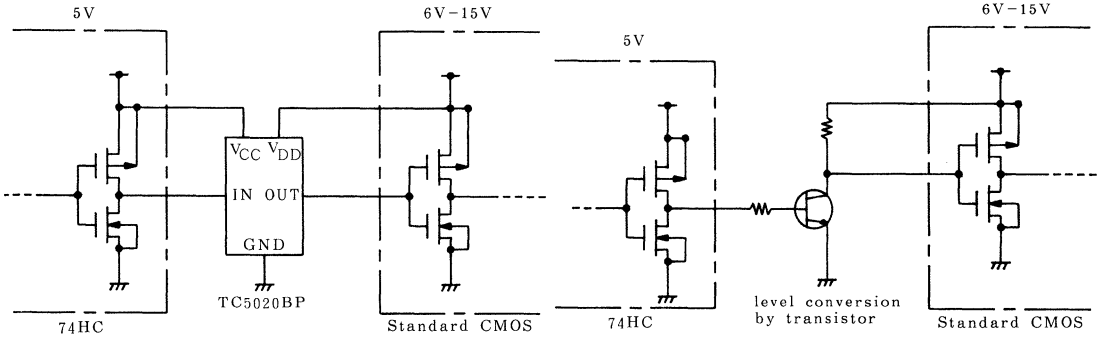


Fig. 9–8 Standard CMOS→74HC Interface

The 4049B/4050B has GND side diode only, and is so constructed that current does not flow in the power source (V_{CC}) of a 5V system even though a voltage of 15V is impressed.

On the other hand, an interface from 74HC to standard CMOS can be realized by using TC5020BP, a level shift IC, as indicated in Fig. 9–9(a). Further, it is also possible to use discrete transistors as shown in Fig. 9–9(b). The circuit employing discrete transistors can, of course, be used for power inversion.

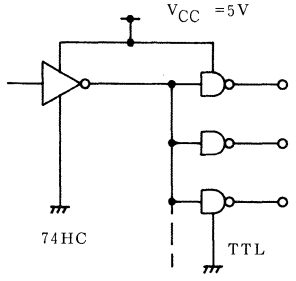


(a) Example of using level shifter IC (b) Example of using transistor

Fig. 9–9 74HC →Standard CMOS Interface

(4) Interface with TTL

When driving TTL with the TC74HC series, input and output voltage levels can be connected without trouble. Fan out is decided by output current of CMOS IC and input current of TTL. An example is shown in Fig. 9–10.



Fan Out Number

	Standard Type	Buffer Type
TTL	2	3
S TTL	2	3
LS TTL	10	15
ALS TTL	20	30

Fig. 9–10 TC74HC → TTL Interface

In this way, the TC74HC series is capable of directly driving various TTL devices.
On the other hand, when driving TC74HC series from TTL, it is necessary to convert the output voltage level of TTL to the input level of 74HC. Normally, TC74HCT series devices which have same input level as LSTTL are used. The input current of TC74HCT series is very small like that of TC74 HC series, and therefore no burden is imposed on the driving side 74LS, and the speed also does not fall too much. Therefore it can be said to be an effective method. Another method is to use pull up resistor as shown in Fig. 9–11.

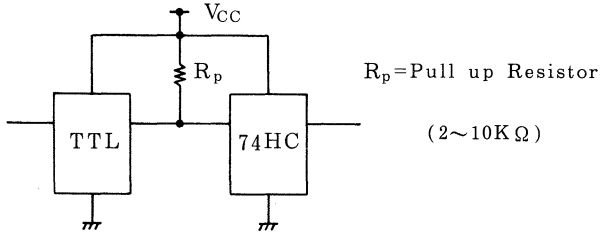


Fig. 9–11 TTL → TC74HC Interface

(5) Interface with CPU

At present, 74LS series TTL is used universally as the peripheral supporting logic for MOS microprocessors. Since TC74HC series has the same speed as 74LS, it can be used as microprocessor peripheral logic. As for an interface between CMOS CPU and 74HC series, there is no problem because both are CMOS. At present, however, the priority of NMOS CPU is higher, and interface of NMOS to CMOS must be taken into consideration.

Output of most NMOS CPU's rises to near V_{CC}, but as shown in Fig. 9–12, as outputs of both driving MOS and load MOS are constituted with enhancement type, no deflection takes place until V_{CC}. For this reason, in order to certainly carry out the signal transfer from NMOS CPU to 74HC, it is easy to use the 74HCT series which has a TTL level input. When connecting 74HC series, a pull up resistor is used as indicated in Fig. 9–12.

Next, driving an NMOS CPU from 74HC series can be connected without difficulty. This is because, normally, the input of NMOS if of high impedance like CMOS, and DC fan out need not be taken into consideration.

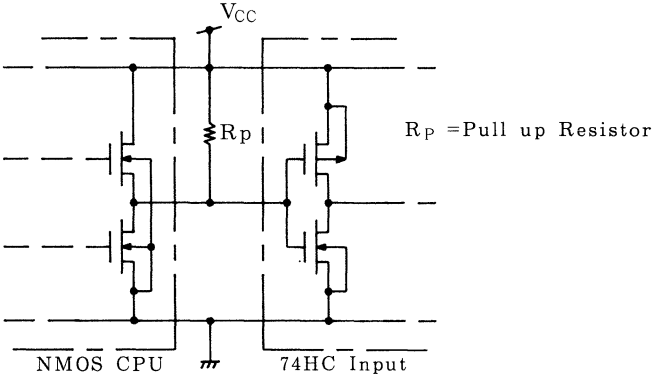


Fig. 9–12 NMOS CPU Interface

9-7 Latch-up

Latch-up is a phenomenon peculiar to CMOS, and is also called SCR (Silicon Controlled Rectifier) Phenomenon. During the normal operation time, if excessive voltage and current caused by big noise or accidental surge is applied on the input or output terminal, or a supply source amplitude suddenly fluctuates, abnormal current flows between V_{CC} and GND, and this abnormal current continues to flow even though the disturbance signal is cut off, and finally damage is caused. Latch -up is the name given to this phenomenon.

Once the latch-up takes place, the original condition is not restored unless the power supply is cut off or voltage is lowered, and an overcurrent continues to flow between V_{CC} and GND. If this status is left alone, destruction of element such as melting of wiring will take place.

(1) Cause of latch-up

Fig. 9-13 shows as equivalent circuit due to the parasitic element. NPN transistor Q_2 is formed in the P-well of NMOS side while PNP transistor Q_1 is formed in the N-substrate of PMOS side, and a parasitic resistor exists between terminals. As is shown from the current path through the medium of the parasitic element, these parasitic elements constitute a Thyristor.

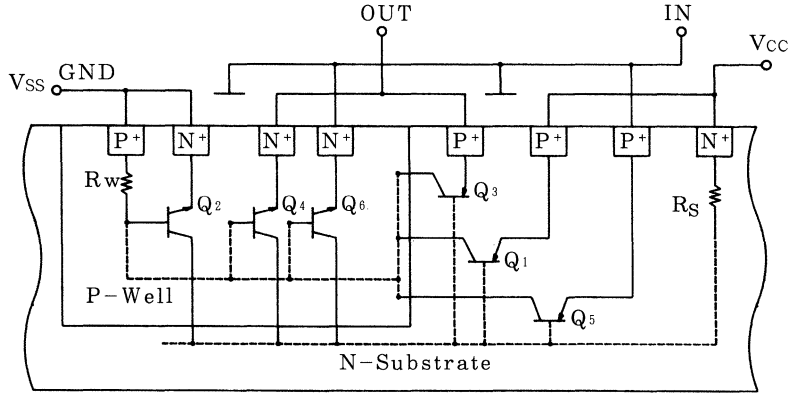


Fig. 9-13 Internal Equivalent Circuit of CMOS IC

For example, if current flows into the N−substrate from external sources, a voltage drop takes place in the resistor Rs of the N−substrate, and this causes to turn on parasistic transistor Q_1 , and current flows towards GND from V_{CC} through the medium of resistor Rw of P−Well. When current flows in Rw, voltage drop takes place at both ends of Rw, Q_2 turns on, and further supply current flows through Rs. As a result, the voltage drop at both ends of Rs furthers increases, Q_1 and Q_2 are left in the turn−on state, and the supply current continues to increase.

In this way, if the voltage drop takes place in resistance Rw of the P−Well and in resistance Rs of the N−substrate, latch−up occurs, and the following causes are considered:

1) To make input voltage higher than V_{CC} + V_F
(Q_5 of Fig. 8−13 turns on)

2) To make input voltage lower than GND − V_F
(Q_6 of Fig. 8−13 turns on)

3) To make output voltage higher than V_{CC} + V_F
(Q_3 of Fig. 8−13 turns on)

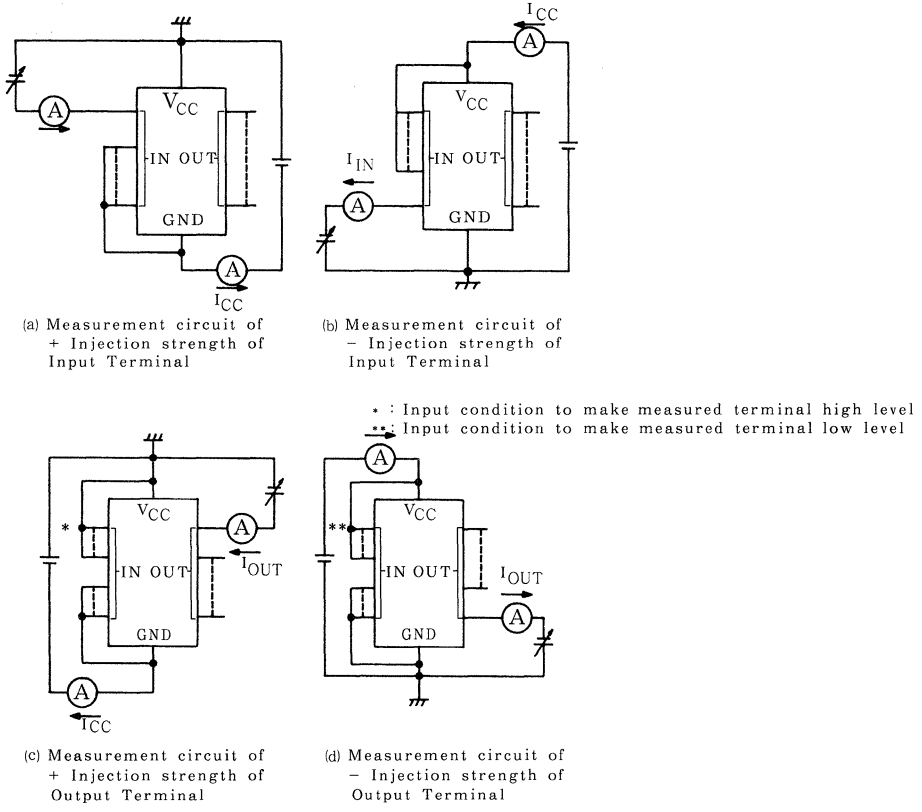
4) To make output voltage lower than GND − V_F
(Q_4 of Fig. 8−13 turns on)

5) To raise supply voltage V_{CC} above the rated value and to cause breakdown.
(To directly force current in Rw or Rs)

Here, V_F is the forward voltage between base and emitter of parasitic bipolar transistor Q_3 −Q_4 .

(2) Latch−up strength measurement

Fig. 9−14 illustrates measurement example of latch−up strength. As indicated in Fig. 8−14, latch−up is induced by forcing current into input terminal (+ injection) or forcing current out of output terminal (− injection), and the current value at that time is measured.



(a) Measurement circuit of + Injection strength of Input Terminal

(b) Measurement circuit of − Injection strength of Input Terminal

(c) Measurement circuit of + Injection strength of Output Terminal

(d) Measurement circuit of − Injection strength of Output Terminal

Fig. 9−14 Latch-up Strength Measurement Circuits by Current Feeding System

(3) Countermeasures

As ample margin is provided for latch−up as explained in (2), there is no problem in using the unit within the standards. However, since the interface part has the possibility of receiving excessive surge, it is recommended that the protective circuit be added as indicated in Fig. 9−15.

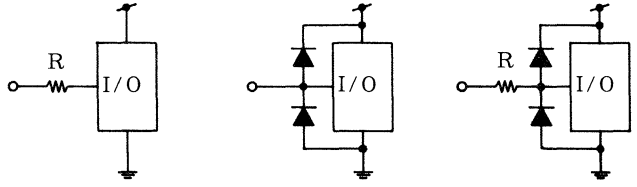


Fig. 9−15 Example of Latch-up Prevention Methods

10. DATA SHEETS

TC74HC00AP/AF/AFN

QUAD 2-INPUT NAND GATE

The TC74HC00A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

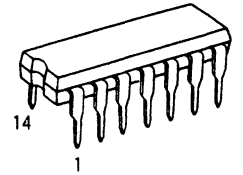
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

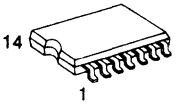
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

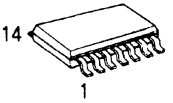
- High Speed ..... t_{pd}=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS00



DIP14 (3 D14A-P)

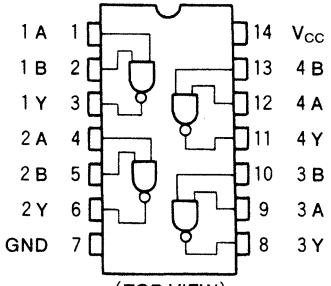


MFP 14
(F14GB-P)



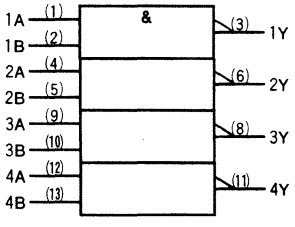
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ～85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC02AP/AF/AFN

QUAD 2-INPUT NOR GATE

The TC74HC02A is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

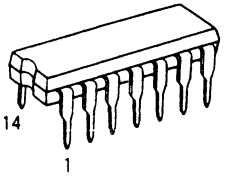
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

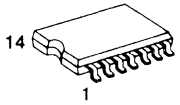
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

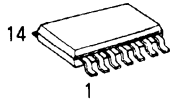
- High Speed ..... t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS02



DIP14 (3 D14A-P)

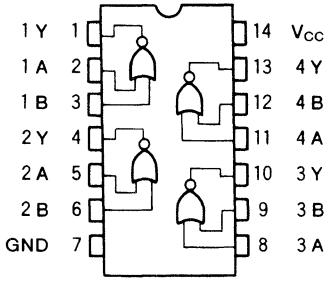


MFP 14
(F14GB-P)



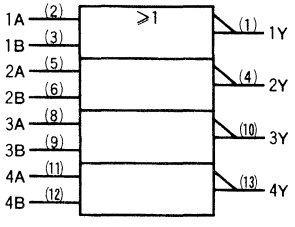
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	21	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC03AP/AF/AFN

QUAD 2-INPUT NAND GATE (OPEN DRAIN)

The TC74HC03A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

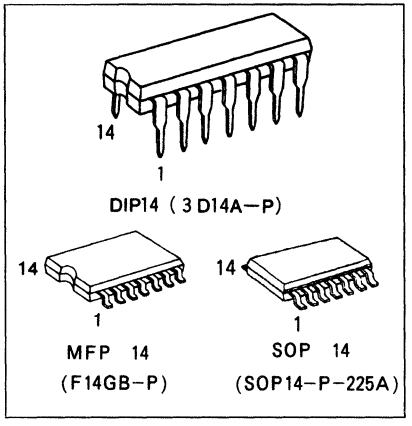
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74 HC00A. But the TC74HC03A has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therfore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

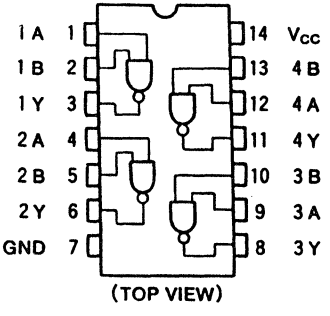
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

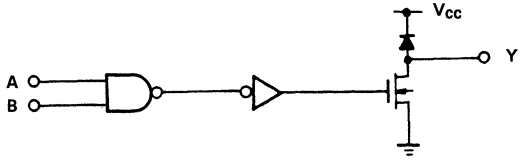
- High Speed ····· t_{pZ} =5ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS03



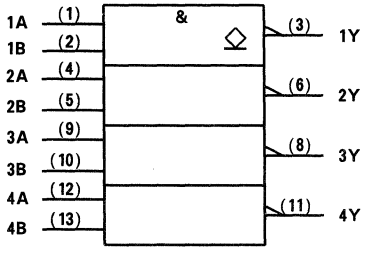
PIN ASSIGNMENT



SYSTEM DIAGRAM(per gate)



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	$+25$	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	–	5	12	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	–	5	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	–	20	75	–	95	
			4.5	–	10	15	–	19	
			6.0	–	9	13	–	16	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	–	24	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	5	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC04AP/AF/AFN

HEX INVERTER

The TC74HC04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

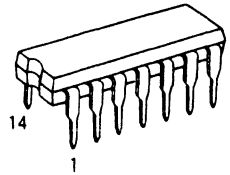
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including buffered output, which provide high noise immunity and stable output.

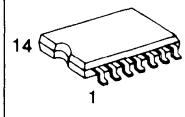
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

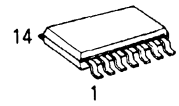
- High Speed ····· tpd=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS04



DIP14 (3 D14A-P)

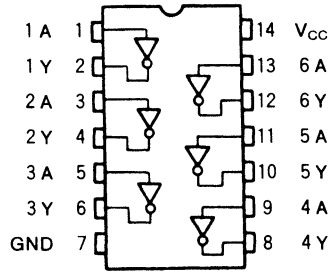


MFP 14
(F14GB-P)



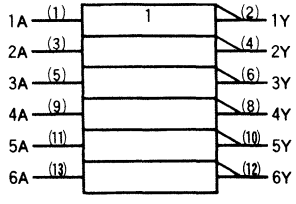
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

TC74HCT04AP/AF/AFN

HEX INVERTER

The TC74HCT04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

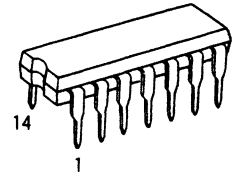
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

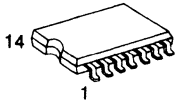
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

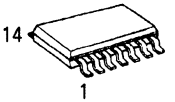
- High Speed ····· t_{pd}=8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS04



DIP14 (3 D14A−P)

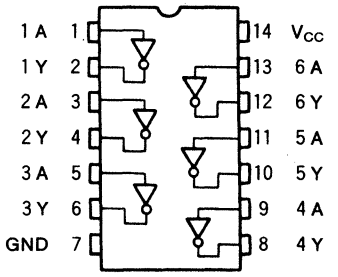


MFP 14
(F14GB−P)



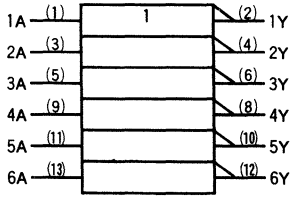
SOP 14
(SOP14−P−225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ≀ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ≀ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	1.0	−	10.0	μA
	I_C	PER INPUT: V_{IN} =0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	–	8	15	–	19	ns
			5.5	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	–	11	18	–	23	
			5.5	–	9	16	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

TC74HCU04AP/AF/AFN

HEX INVERTER

The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

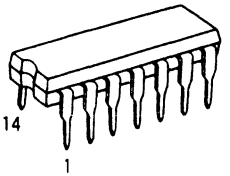
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Since the internal circuit is composed of a single stage inverter, it can be used in analog applications such as crystal oscillators.

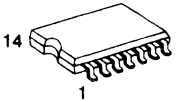
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

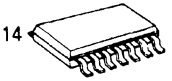
- High Speed ····· t_{pd}=4ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=10% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS04



DIP14 (3 D14A-P)

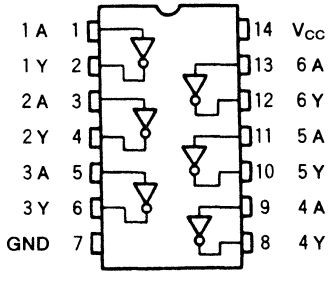


MFP 14
(F14GB-P)



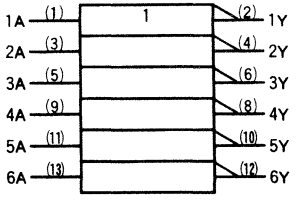
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.7	−	−	1.7	−	V
				4.5	3.6	−	−	3.6	−	
				6.0	4.8	−	−	4.8	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.3	−	0.3	V
				4.5	−	−	0.9	−	0.9	
				6.0	−	−	1.2	−	1.2	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IL}	I_{OH} =−20 μA	2.0	1.8	2.0	−	1.9	−	V
				4.5	4.0	4.5	−	4.4	−	
				6.0	5.5	5.9	−	5.9	−	
		V_{IN} = GND	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} =20 μA	2.0	−	0.0	0.2	−	0.2	V
				4.5	−	0.0	0.5	−	0.5	
				6.0	−	0.1	0.5	−	0.5	
		V_{IN} = V_{CC}	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	4	8	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	18	60	–	75	
			4.5	–	6	12	–	15	
			6.0	–	5	10	–	13	
Input Capacitance	C_{IN}			–	9	15	–	15	pF
Power Dissipation Capacitance	C_{PD}(1)			–	13	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

TC74HC08AP/AF/AFN

QUAD 2-INPUT AND GATE

The TC74HC08A is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

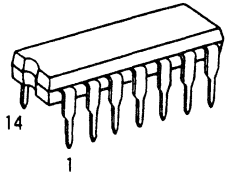
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

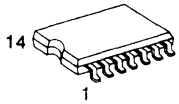
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

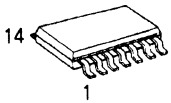
- High Speed ..... t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS08



DIP14 (3 D14A-P)

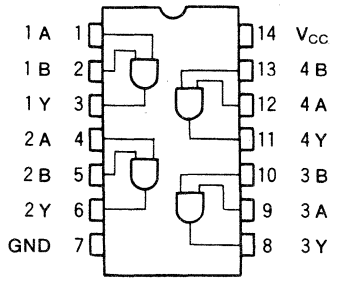


MFP 14
(F14GB-P)



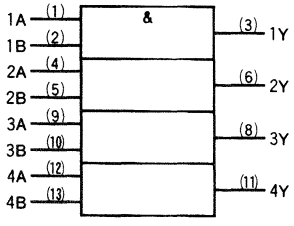
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	24	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	19	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TRIPLE 3-INPUT NAND GATE

The TC74HC10A is a high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

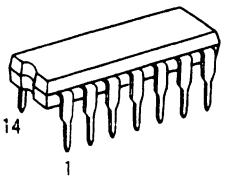
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

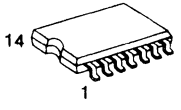
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

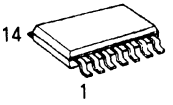
- High Speed ..... t_{pd}=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS10



DIP14 (3 D14A-P)

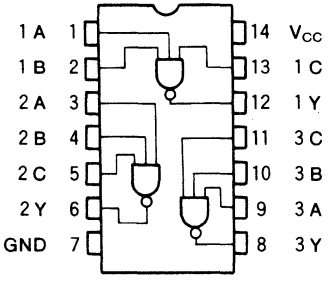


MFP 14
(F14GB-P)



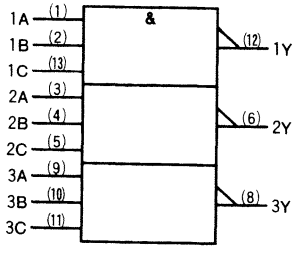
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	ns
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	23	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC11AP/AF/AFN

TRIPLE 3-INPUT AND GATE

The TC74HC11A is a high speed CMOS 3-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

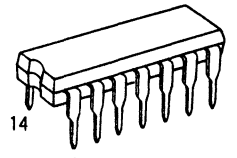
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including a buffer output, which provide high noise immunity and stable output.

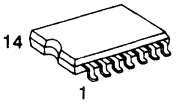
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

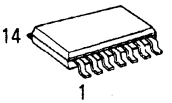
- High Speed ····· t_{pd}=7ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS11



DIP14 (3 D14A-P)

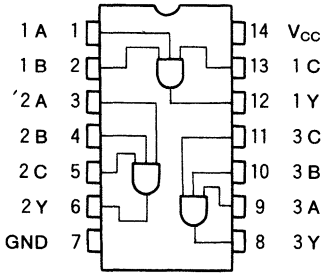


MFP 14
(F14GB-P)



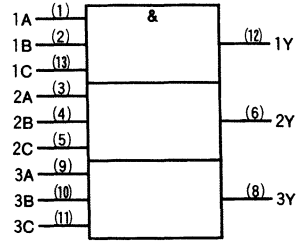
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	7	14	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	30	85	–	105	ns
			4.5	–	10	17	–	21	
			6.0	–	9	14	–	18	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	32	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{ (per Gate)}$$

TC74HC14AP/AF/AFN

HEX SCHMITT INVERTER

The TC74HC14A is a high speed CMOS SCHMITT INVERTER fabricated with silicon gate C^2MOS technology.

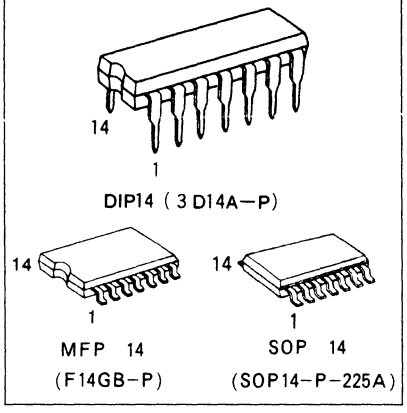
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HC04A but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger function, the TC74HC14A can be used as a line receivers which will receive slow input signals.

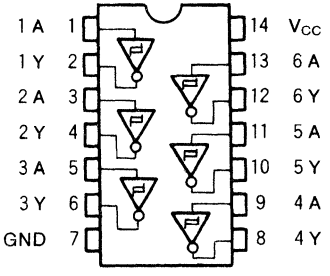
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

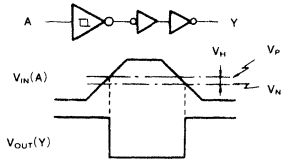
- High Speed ····· t_{pd}=11ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{IH}=1.1V at V_{CC}=5V
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS14



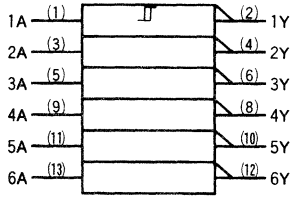
PIN ASSIGNMENT



SYSTEM DIAGRAM,WAVEFORM



ICE LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			2.0	1.0	1.25	1.5	1.0	1.5	V
				4.5	2.3	2.7	3.15	2.3	3.15	
				6.0	3.0	3.5	4.2	3.0	4.2	
Negative Threshold Voltage	V_N			2.0	0.3	0.65	0.9	0.3	0.9	V
				4.5	1.13	1.6	2.0	1.13	2.0	
				6.0	1.5	2.3	2.6	1.5	2.6	
Hysteresis Voltage	V_H			2.0	0.3	0.6	1.0	0.3	1.0	V
				4.5	0.6	1.1	1.4	0.6	1.4	
				6.0	0.8	1.2	1.7	0.8	1.7	
High−Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	$I_{OH}=-20\,\mu A$	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			$I_{OH}=-4$ mA	4.5	4.18	4.31	−	4.13	−	
			$I_{OH}=-5.2$mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	$I_{OL}=20\,\mu A$	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			$I_{OL}=4$ mA	4.5	−	0.17	0.26	−	0.33	
			$I_{OL}=5.2$mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	21	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	125	–	155	
			4.5	–	14	25	–	31	
			6.0	–	12	21	–	26	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	28	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{(per Gate)}$$

TC74HC20AP/AF/AFN

DUAL 4-INPUT NAND GATE

The TC74HC20A is a high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

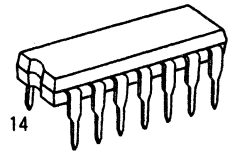
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

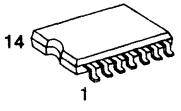
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

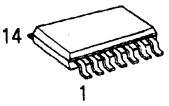
- High Speed ····· t_{pd}=8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH}=V_{NIL} 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS20



DIP14 (3 D14A-P)

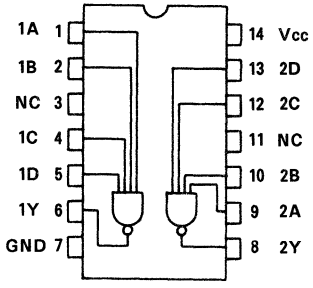


MFP 14
(F14GB-P)



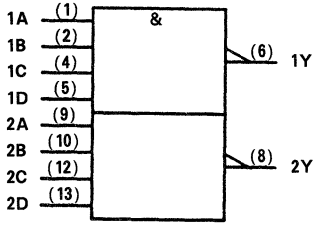
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	5	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	44	90	–	115	
			4.5	–	11	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	29	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Gate)}$$

TC74HC21AP/AF/AFN

DUAL 4-INPUT AND GATE

The TC74HC21A is a high speed CMOS 4-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

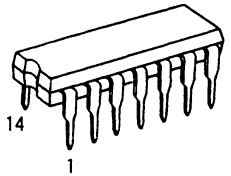
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

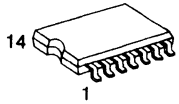
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

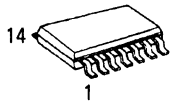
- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS21



DIP14 (3 D14A-P)

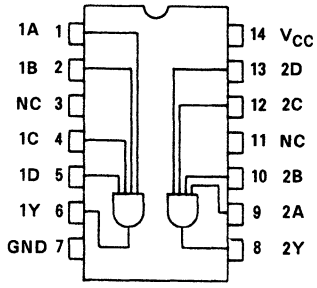


MFP 14
(F14GB-P)



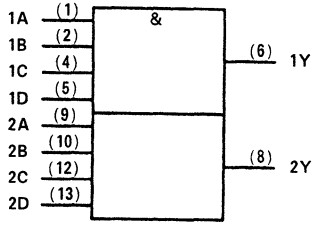
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs				Outputs
A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

TC74HC27AP/AF/AFN

TRIPLE 3-INPUT NOR GATE

The TC74HC27A is a high speed CMOS 3-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

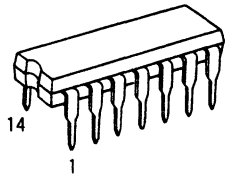
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

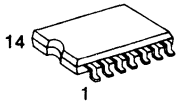
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

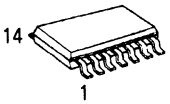
- High Speed ..... t_{pd}=7ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS27



DIP14 (3 D14A-P)

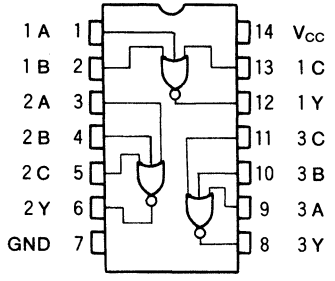


MFP 14
(F14GB-P)



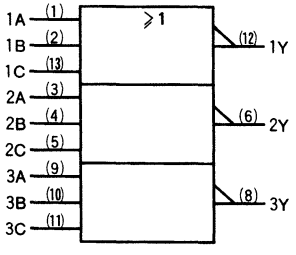
SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	7	15	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	30	90	–	115	
			4.5	–	10	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{(per Gate)}$$

TC74HC30P/F 8-INPUT NAND GATE

The TC74HC30 is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

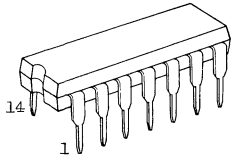
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 5 stages including buffer output, which enables high noise immunity and stable output.

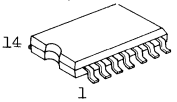
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=12ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS30.



DIP14(3D14A-P)



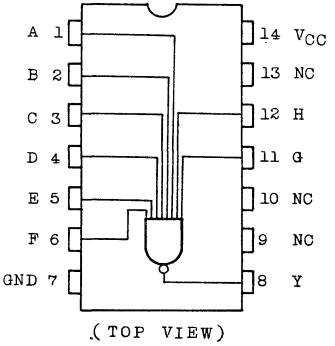
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

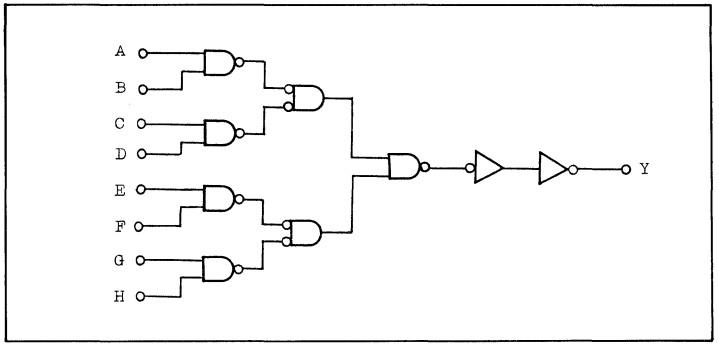
PIN ASSIGNMENT



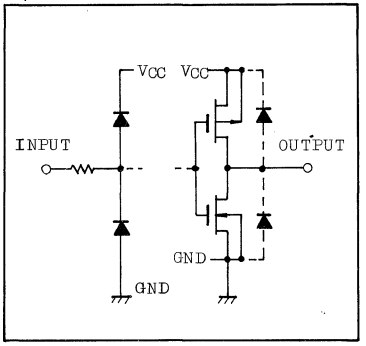
(TOP VIEW)

NC : No Connection

LOGIC DIAGRAM



INPUT and OUTPUT
EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

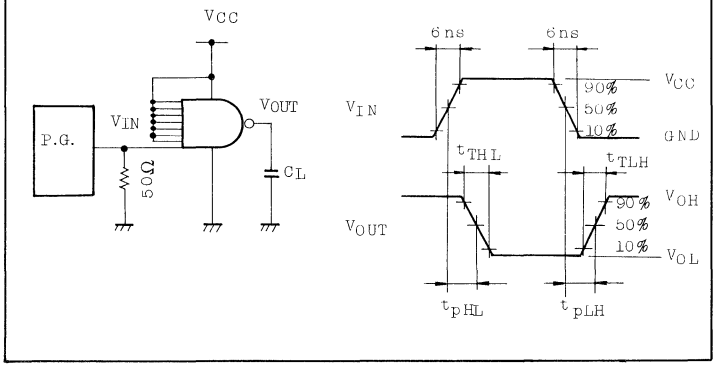
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

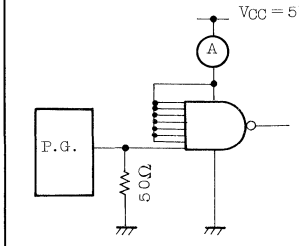
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC32AP/AF/AFN

QUAD 2-INPUT OR GATE

The TC74HC32A is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

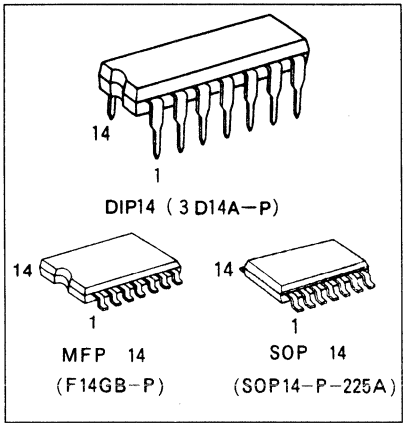
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

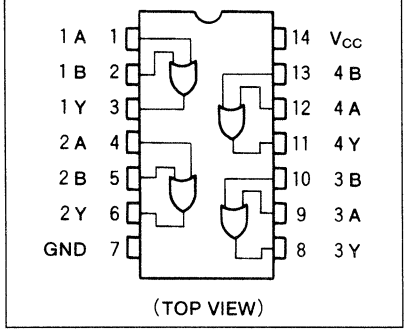
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

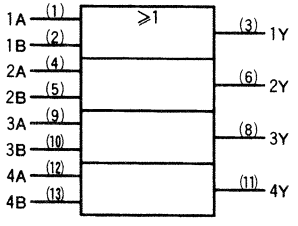
- High Speed ..... t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS32



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	24	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	21	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC42AP/AF/AFN

BCD-TO-DECIMAL DECODER

The TC74HC42A is a high speed CMOS BCD-to-DECIMAL DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

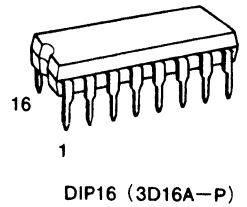
A BCD code applied to the four inputs (A-D) sets a low level at one of ten decoded outputs. A illegal BCD code such as eleven thru fifteen sets all outputs high. This device can be used as 3-to-8 LINE DECODER when input D is held low.

This device is useful for code conversion , address decoding , memory selection , multiplexing , or readout decoding.

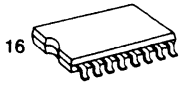
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

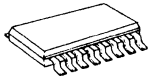
- High Speed ····· t_{pd}=13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS42



DIP16 (3D16A-P)

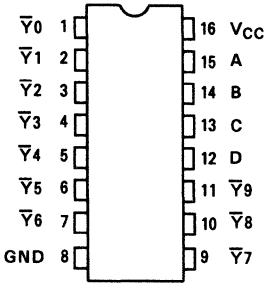


MFP 16
(F16GC-P)



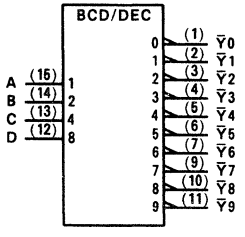
SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

ICE LOGIC SYMBOL

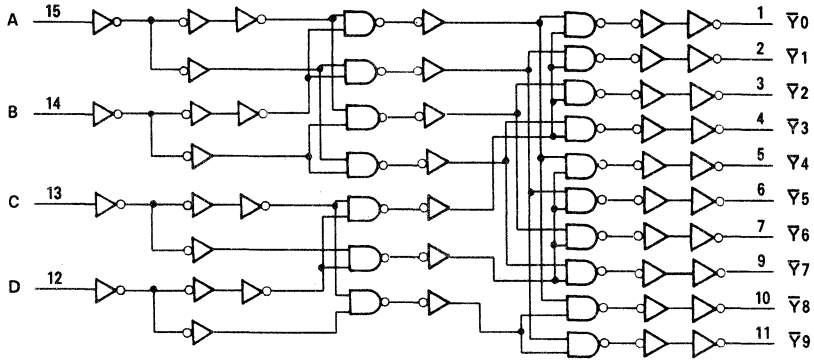


TRUTH TABLE

CODE	BCD INPUTS				DECIMAL OUTPUTS									
No.	D	C	B	A	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	$\overline{Y}8$	$\overline{Y}9$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
–	H	X	H	X	H	H	H	H	H	H	H	H	H	H
–	H	H	X	X	H	H	H	H	H	H	H	H	H	H

X; Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	13	25	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	48	145	–	180	
			4.5	–	16	29	–	36	
			6.0	–	14	25	–	31	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	68	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC51AP/AF/AFN

DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

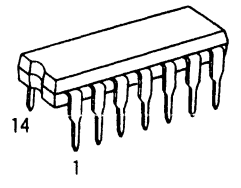
The TC74HC51A is a high speed CMOS 2-WIDE 2-INPUT/3-INPUT AND/OR/INVERT GATE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

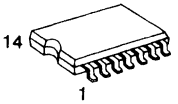
It contains a 2-WIDE 2-INPUT AND/OR/INVERT GATE and a 2-WIDE 3-INPUT AND/OR/INVERT GATE .

The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffer outputs, which provide high noise immunity and stable output.

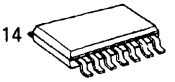
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14 (3 D14A-P)



MFP 14
(F14GB-P)

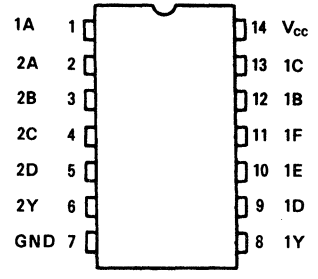


SOP 14
(SOP14-P-225A)

FEATURES:

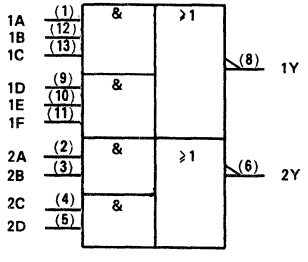
- High Speed ····· t_{pd}= 10 ns(Typ.)atV_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)atTa=25℃
- High Noise Immunity ····· V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS51

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

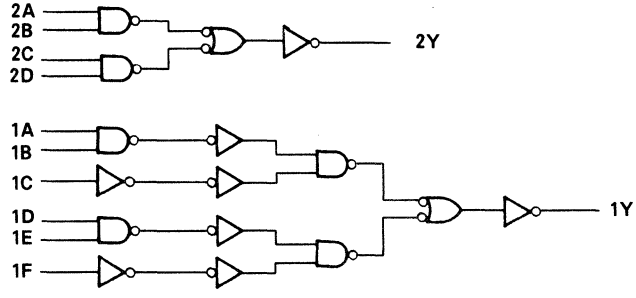
INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

X:Don't care

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	39	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	35	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

TC74HC73AP/AF

DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC73A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

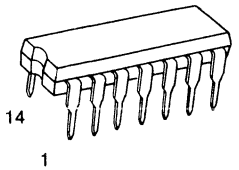
Depending on the logic levels applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.

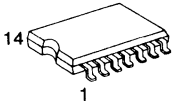
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=55MHz(Typ.) V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.) Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS73

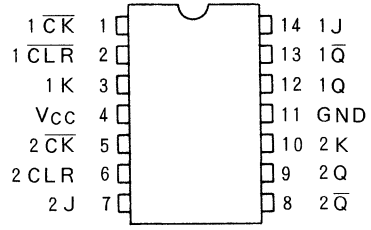


DIP14 (3D14A-P)



MFP14 (F14GB-P)

PIN ASSIGNMENT



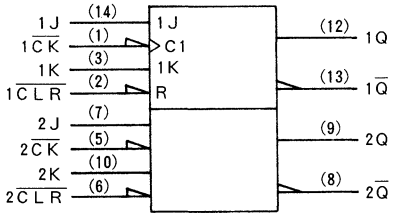
(Top View)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	–
H	H	L	↓	H	L	–
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X : Don't Care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	11	21	
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	15	25	
Maximum Clock Frequency	f_{MAX}		35	75	−	MHz

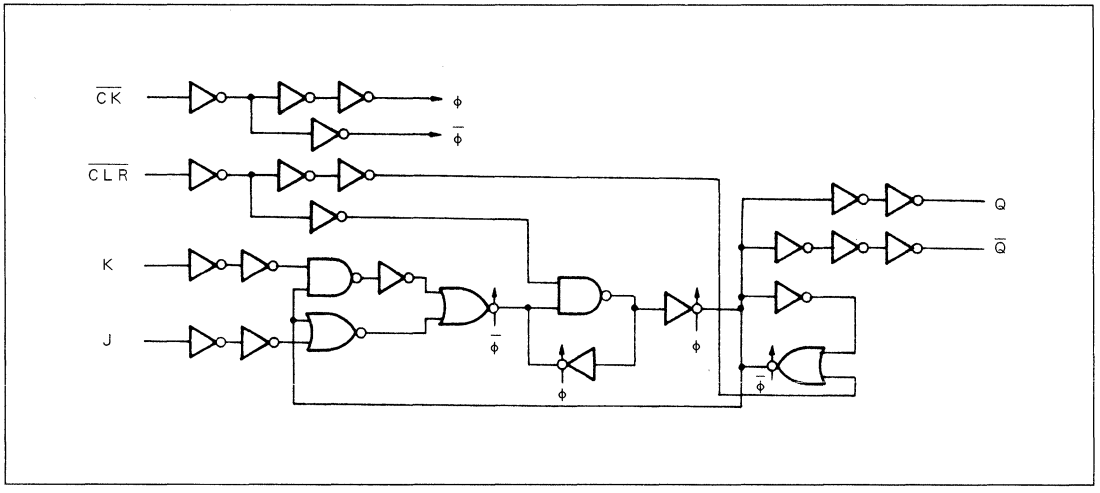
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	42	125	−	155	
			4.5	−	14	25	−	31	
			6.0	−	12	21	−	26	
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	54	145	−	180	
			4.5	−	18	29	−	36	
			6.0	−	15	25	−	31	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	−	5	−	MHz
			4.5	30	60	−	24	−	
			6.0	35	80	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	35	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM



TC74HC74AP/AF/AFN

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74HC74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

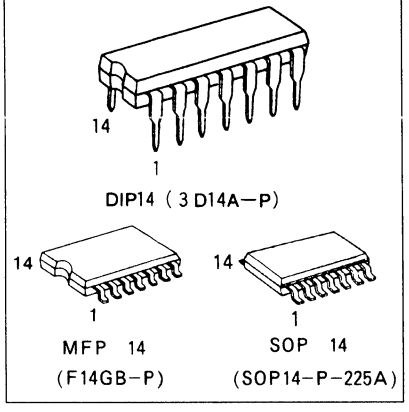
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

$\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the CLOCK and are accomplished by setting the applopriate input to an "L" level.

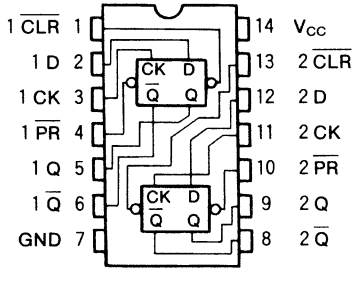
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=77MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS74



PIN ASSIGNMENT

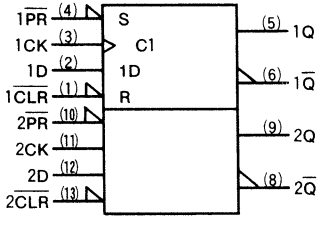


TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	14	26	
Maximum Clock Frequency	f_{MAX}		36	77	−	MHz

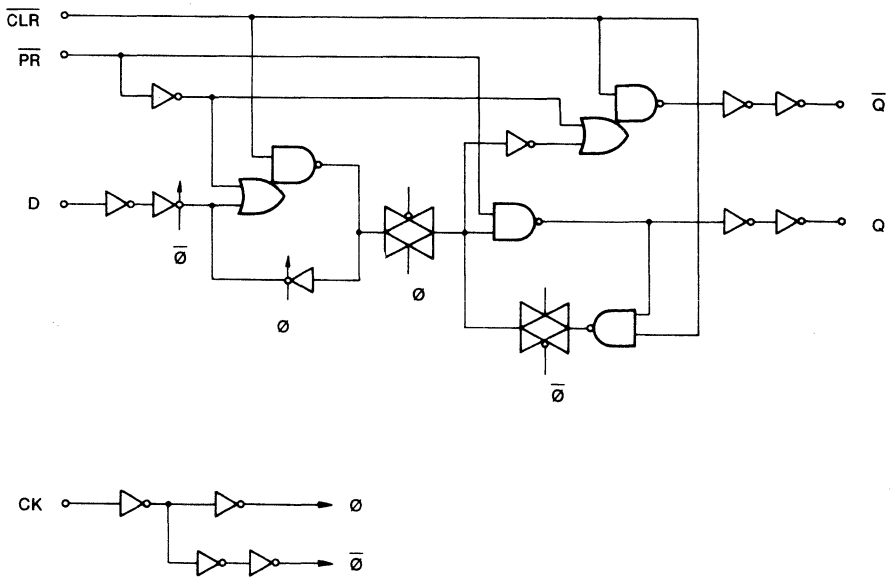
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	48	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	51	150	−	190	
			4.5	−	17	30	−	38	
			6.0	−	15	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	21	−	5	−	MHz
			4.5	31	63	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	34	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM (1/2package)



TC74HC75AP/AF

4-BIT D TYPE LATCH

The TC74HC75A is a high speed CMOS D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

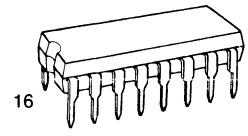
It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4) and each group can be used in different circuits.

Data applied to the data inputs are transferred to the Q and $\overline{Q}$ outputs when the enable input is high.When the enable input is low,the outputs are not affected.

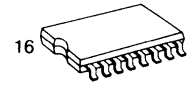
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS75

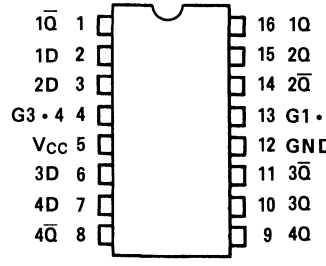


DIP16 (3D16A-P)



MFP16 (F16GC-P)

PIN ASSIGNMENT



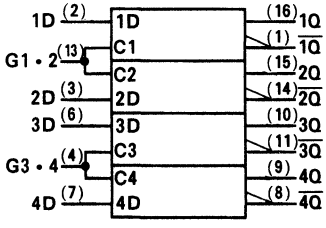
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\overline{Q}$n	LATCH

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (G)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	10	18	
Propagation Delay Time (G−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	10	21	

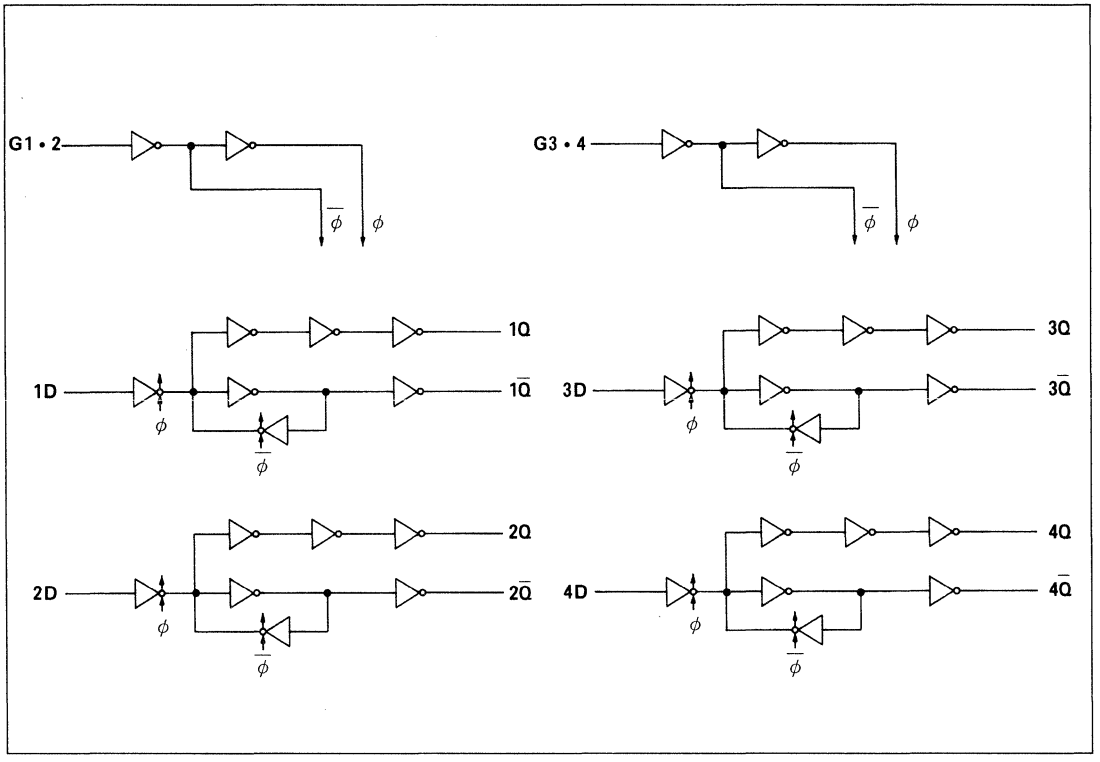
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	36	110	−	140	
			4.5	−	12	22	−	28	
			6.0	−	10	19	−	24	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	40	125	−	155	
			4.5	−	13	25	−	31	
			6.0	−	11	21	−	26	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	30	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Latch)}$$

SYSTEM DIAGRAM



TC74HC76AP/AF

DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

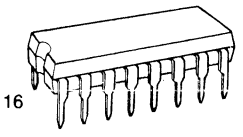
The TC74HC76A is a high speed CMOS J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

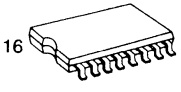
In accordance with the logic level applied to the J and K inputs,the outputs change state on the negative going transition of the clock pulse.

$\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the clock and are accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16 (3D16A-P)

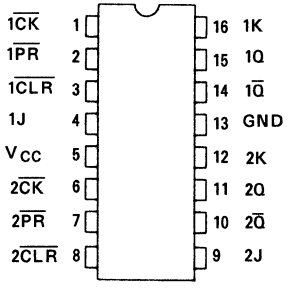


MFP16 (F16GC-P)

FEATURES:

- High Speed ····· f_{MAX}=65MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS76 .

PIN ASSIGNMENT



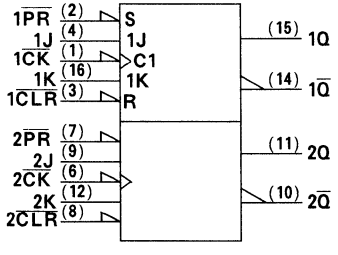
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$,$\overline{PR}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	12	21	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	14	24	
Maximum Clock Frequency	f_{MAX}		33	65	−	MHz

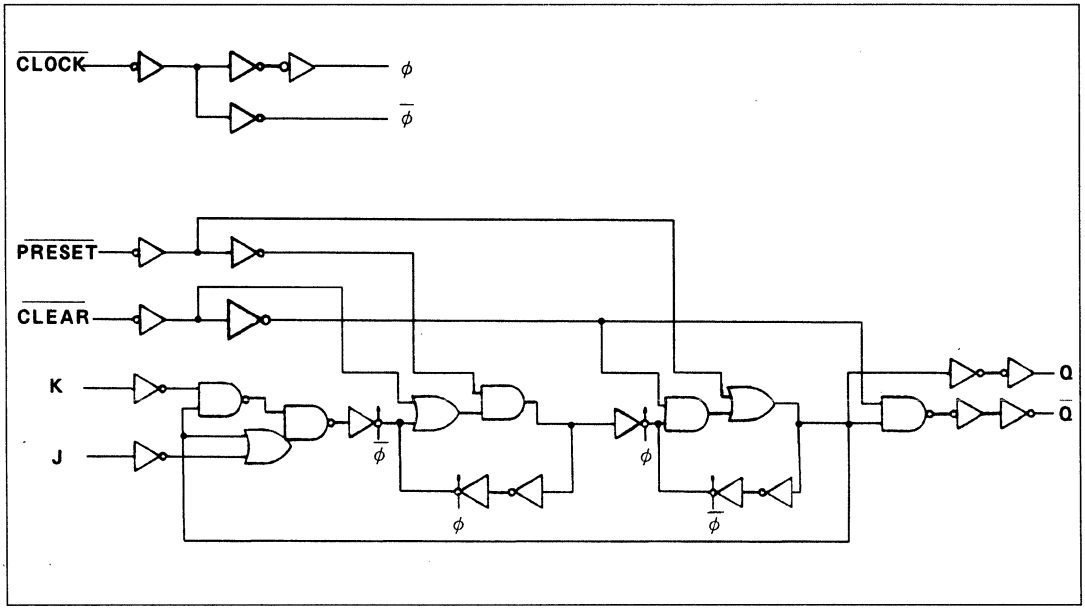
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	60	125	−	155	
			4.5	−	15	25	−	31	
			6.0	−	13	21	−	26	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	76	140	−	195	
			4.5	−	18	28	−	39	
			6.0	−	16	24	−	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	21	−	5	−	MHz
			4.5	31	63	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{(per F/F)}$$

SISTEM DIAGRAM (1/2 package)



4-BIT D TYPE LATCH

The TC74HC77A is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissiparion.

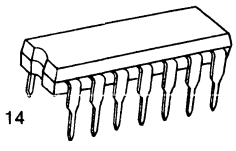
It contains two groups of 2-bit latches controlled by an enable input (G1, 2 or G3, 4) and these two groups may be used in different circuits.

The data applied to the data inputs are transferred to the respective Q outputs when the enable input is held high. When the enable input is low, the outputs remain at the level at the time the enable goes low.

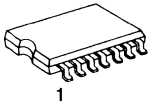
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS77

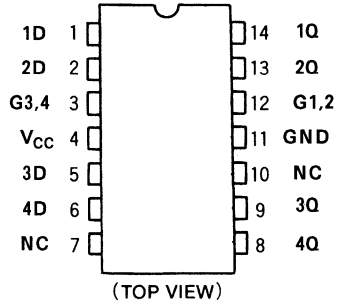


DIP14 (3D14A-P)



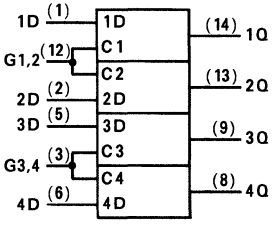
MFP14 (F14GB-P)

PIN ASSIGNMENT



(TOP VIEW)
NC:NO CONNECTION

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION
D	G	Q	
L	H	L	—
H	H	H	—
X	L	Q_n	LATCH

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (G)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		−	10	17	
Propagation Delay Time (G−Q)	t_{pLH} t_{pHL}		−	10	17	

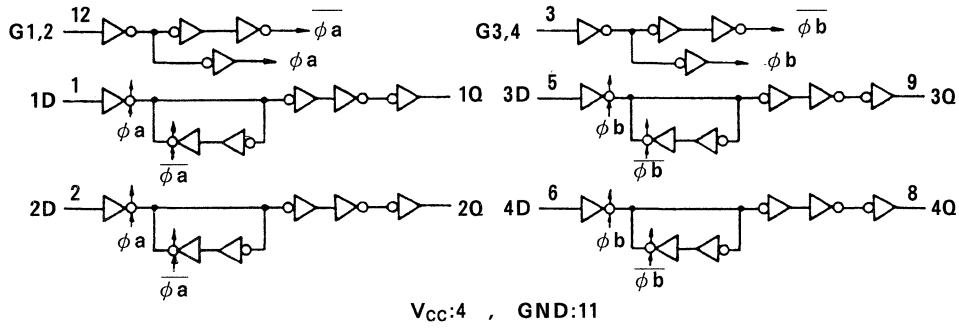
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Propagation Delay Time (G−Q)	t_{pLH} t_{pHL}		2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	20	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4(\text{per Gate})$$

SYSTEM DIAGRAM



4-BIT MAGNITUDE COMPARATOR

The TC74HC85A is a high speed CMOS 4 BIT MAGNITUDE COMPARATOR fabricated with silicon gate C^2MOS technology.

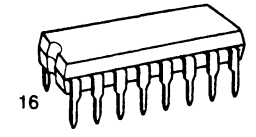
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC85A compares two 4-bit words applied to inputs A0~A3 and B0~B3, and provides a high voltage level on one of three outputs: A>B, A<B, or A=B.

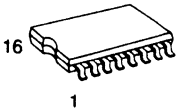
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

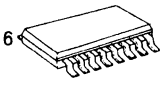
- High Speed ····· t_{pd} =22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS85



DIP16 (3D16A-P)

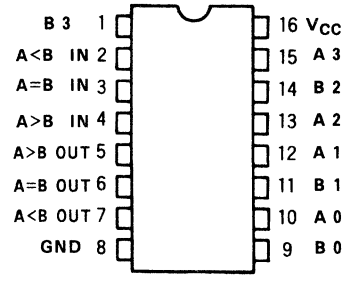


MFP 16
(F16GC-P)



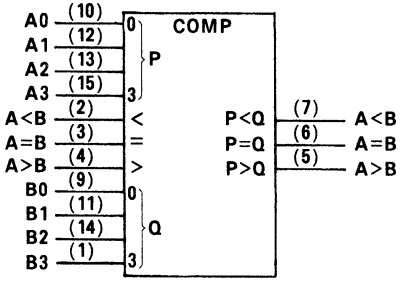
SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

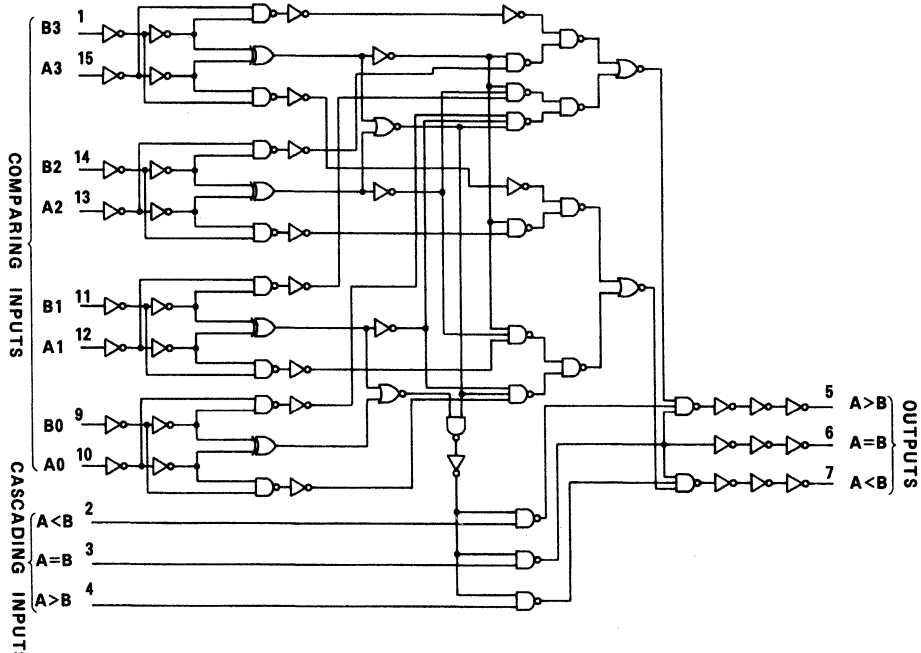


TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3> B3	X	X	X	X	X	X	H	L	L
A3= B3	A2> B2	X	X	X	X	X	H	L	L
A3= B3	A2= B2	A1> B1	X	X	X	X	H	L	L
A3= B3	A2= B2	A1= B1	A0> B0	X	X	X	H	L	L
A3= B3 ,	A2= B2 ,	A1= B1 ,	A0= B0	L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3= B3	A2= B2	A1= B1	A0< B0	X	X	X	L	H	L
A3= B3	A2= B2	A1< B1	X	X	X	X	L	H	L
A3= B3	A2< B2	X	X	X	X	X	L	H	L
A3< B3	X	X	X	X	X	X	L	H	L

X:Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B–OUT)	t_{pLH} t_{pHL}		–	22	34	
Propagation Delay Time (CASCADE–OUT)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

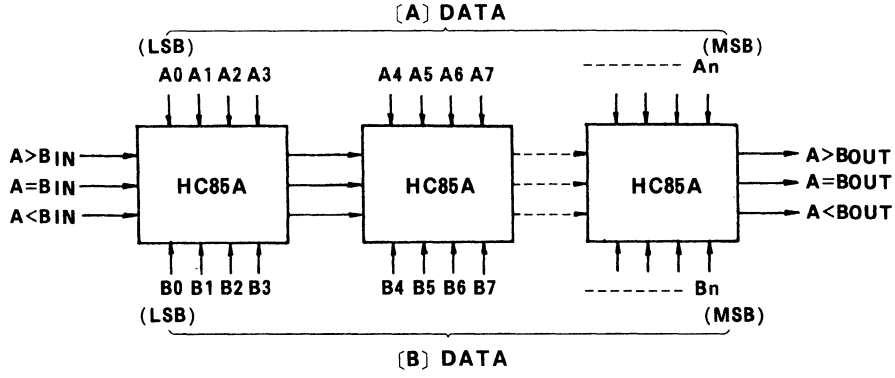
PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B–OUT)	t_{pLH} t_{pHL}		2.0	–	90	195	–	245	
			4.5	–	26	39	–	49	
			6.0	–	22	33	–	42	
Propagation Delay Time (CASCADE–OUT)	t_{pLH} t_{pLH}		2.0	–	40	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	11	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION

N-BIT CASCADING CONNECTION



COMPARING INPUT	CASCADING INPUT			OUTPUT		
	A>B	A=B	A<B	A>B	A=B	A<B
〔A〕 > 〔B〕	X	X	X	H	L	L
〔A〕 = 〔B〕	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
〔A〕 < 〔B〕	X	X	X	L	L	H

X:Don't Care

TC74HC86P/F

TC74HC86P/F QUAD EXCLUSIVE OR GATE

The TC74HC86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate C^2MOS technology.

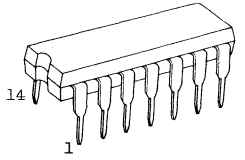
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Input and output buffer are installed, which enables high noise immunity and stable output.

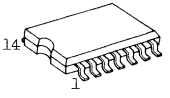
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS86

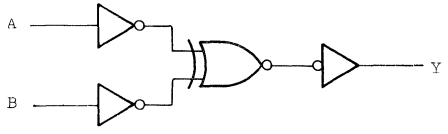


DIP14(3D14A-P)

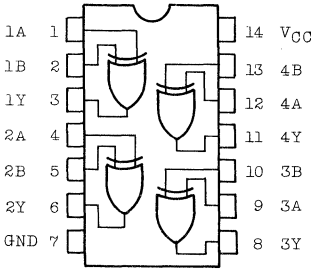


MFP14(F14GB-P)

LOGIC DIAGRAM (per Gate)



PIN ASSIGNMENT



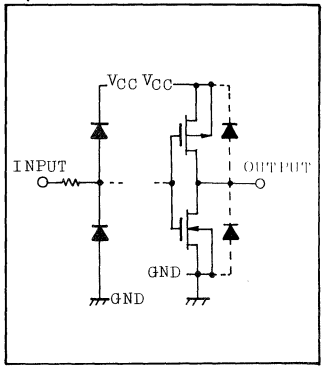
(Top View)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

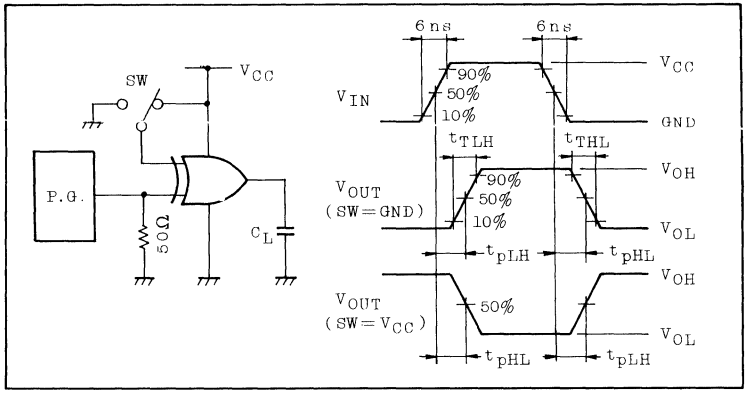
PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

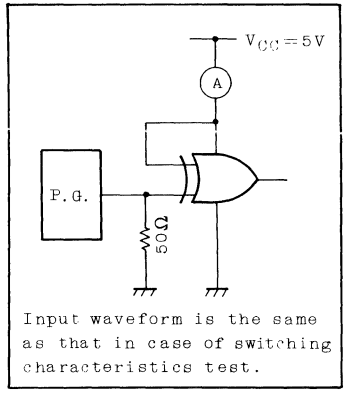
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	120	-	150	ns
			4.5	-	16	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

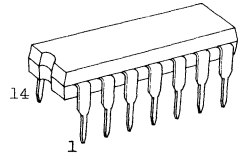
TC74HC107P/F

TC74HC107P/F DUAL J-K FLIP FLOP WITH CLEAR

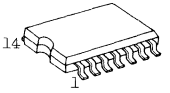
The TC74HC107 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=52MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=2μA(Max.) (Ta=25°C)
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS107



DIP14(3D14A-P)



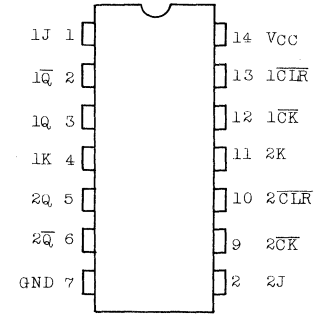
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿VCC+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Doide Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{STG}	-65∿150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

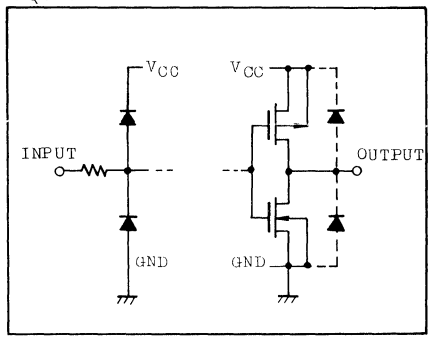


(TOP VIEW)

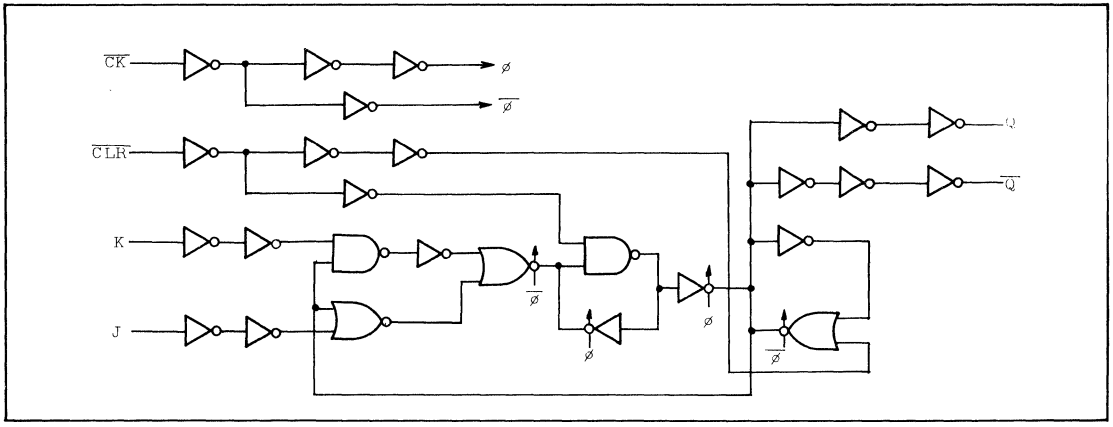
TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	--
H	H	L	↓	H	L	--
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

INPUT and OUTPUT
EQUIVALENT CIRCUIT



LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	48	-	24	-	
			6.0	35	56	-	28	-	

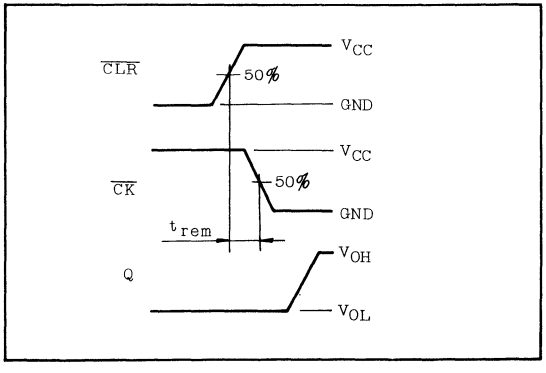
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

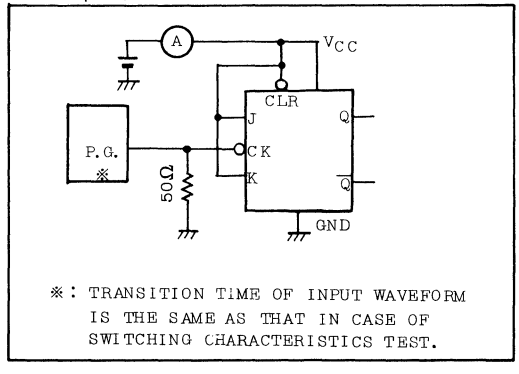
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

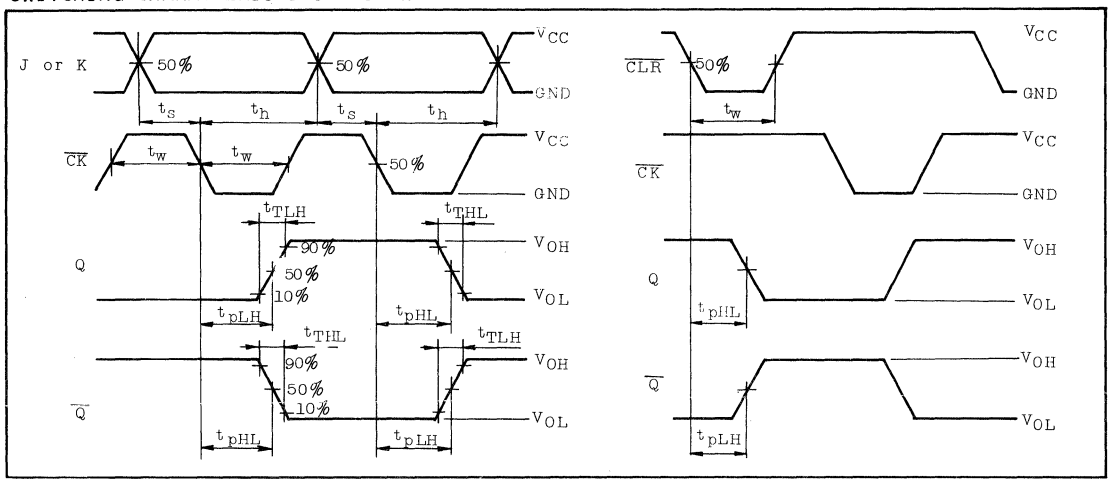


$I_{CC(opr.)}$ TEST CIRCUIT



※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC109AP/AF/AFN

DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR

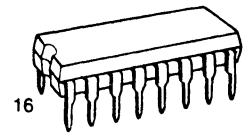
The TC74HC109A is a high speed CMOS J-$\overline{K}$ FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level applied to the J and $\overline{K}$ inputs,the outputs change state on the positive going transition of the clock pulse.

$\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and are accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16 (3D16A-P)

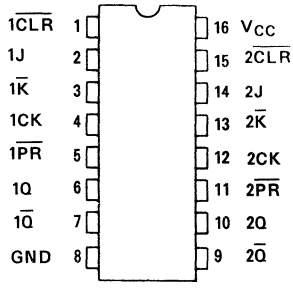
MFP 16 (F16GC-P)

SOP 16 (SOP16-P-225A)

FEATURES:

- High Speed ····· f_{MAX}=63MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS109.

PIN ASSIGNMENT



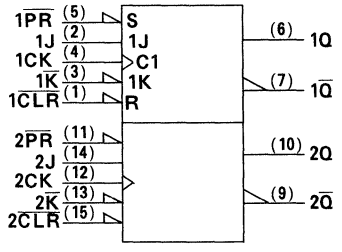
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	L	↓	L	L	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{PR}$,$\overline{CLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{PR}$,$\overline{CLR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Propagation Delay Time ($\overline{PR}$,$\overline{CLR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Maximum Clock Frequency	f_{MAX}		33	63	−	MHz

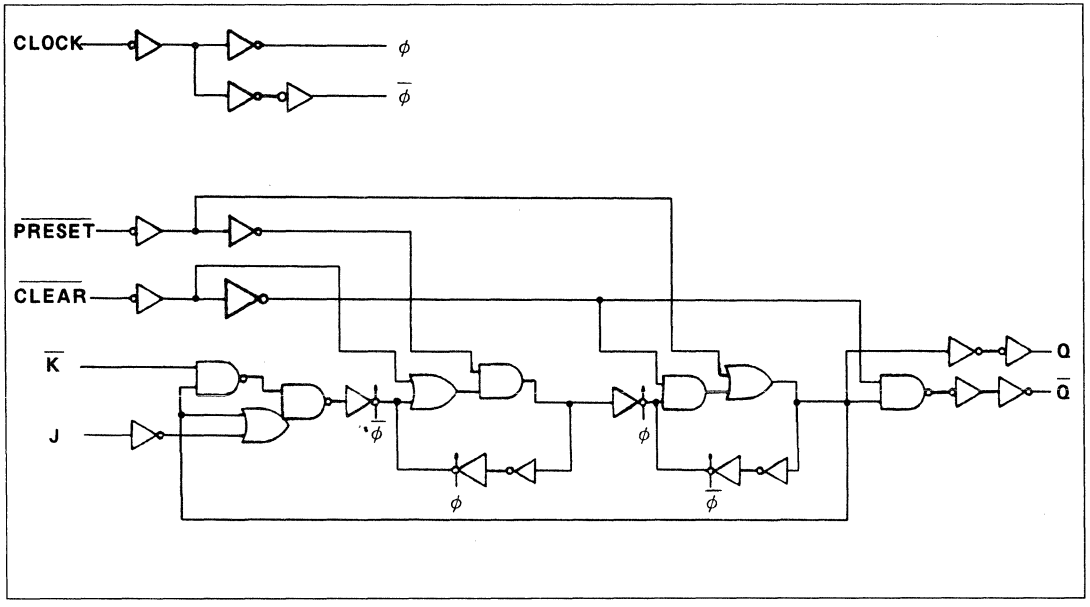
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Propagation Delay Time ($\overline{PR}$,$\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	17	−	5	−	MHz
			4.5	31	59	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	41	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{(per F/F)}$$

SISTEM DIAGRAM (1/2package)



TC74HC112P/F DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC112 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

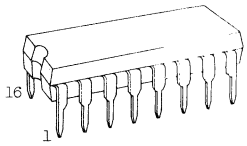
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

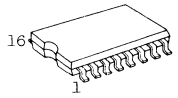
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=58MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS112



DIP16(3D16A-P)



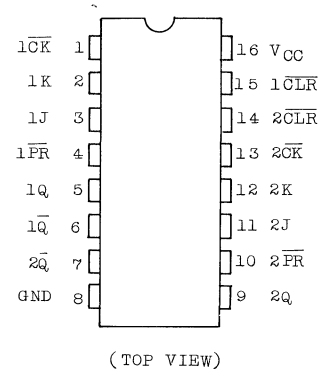
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



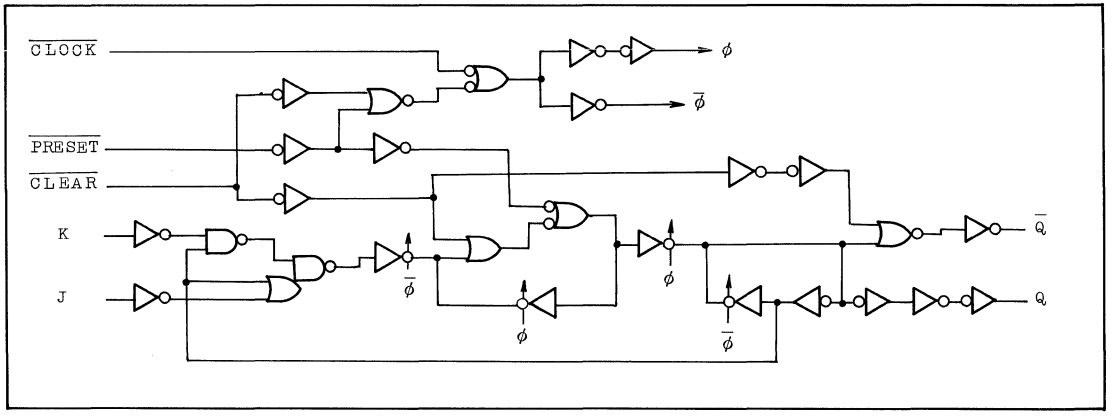
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

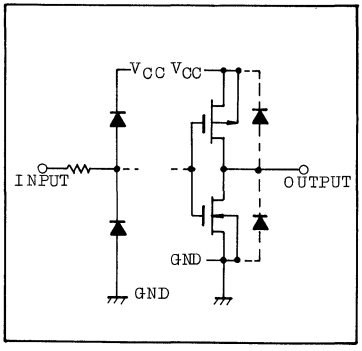
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	92	180	-	225	
	t_{pHL}		4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	53	-	24	-	
			6.0	35	62	-	28	-	

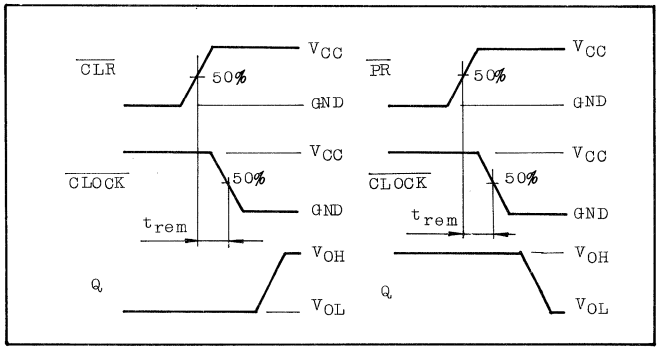
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∼85°C MIN.	Ta=-40∼85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	40	100	-	120	
			4.5	-	10	20	-	24	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	54	-	-	-	

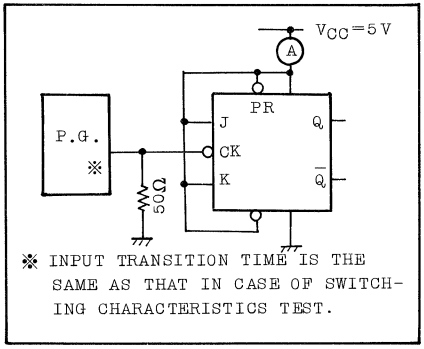
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

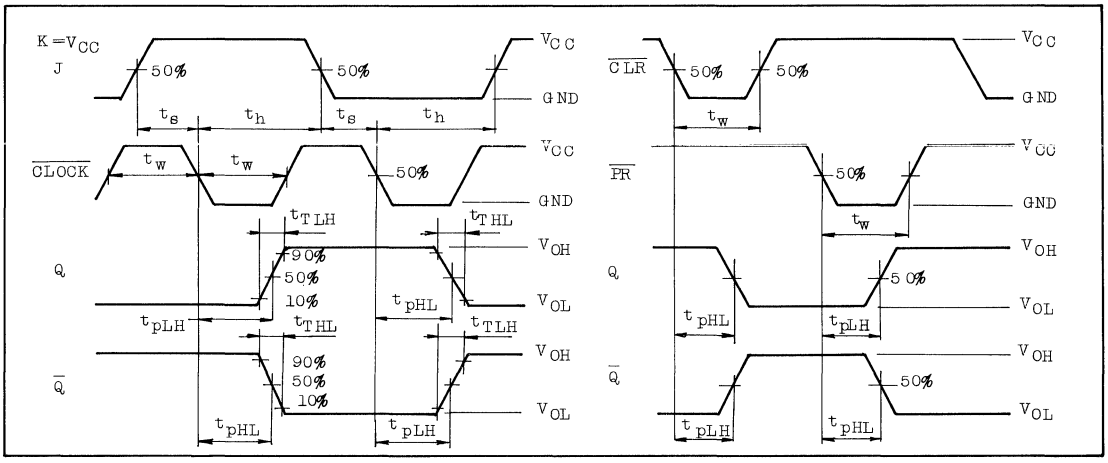


I_{CC}(opr.) TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC113P/F

TC74HC113P/F DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC113 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

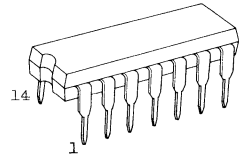
In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The preset function is accomplished independently of the clock condition when the preset input ($\overline{PR}$) is taken low.

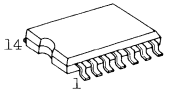
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=63MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS113



DIP14(3D14A-P)



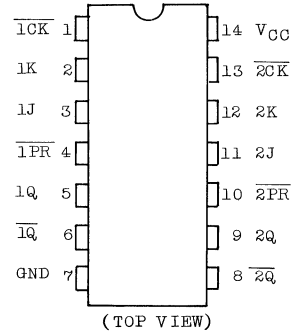
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



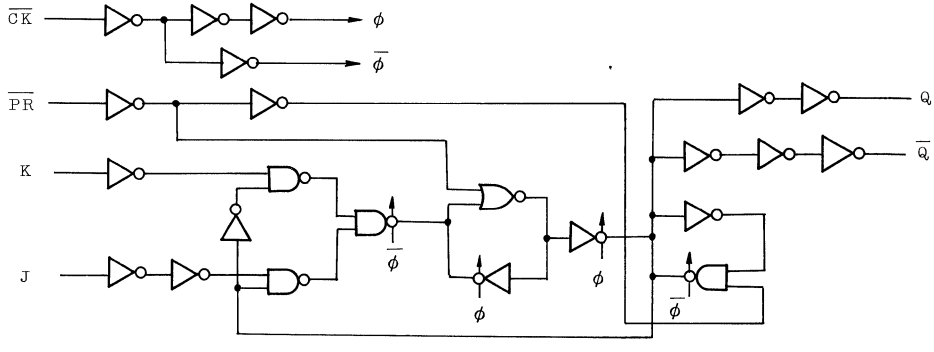
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	Preset
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	-
H	H	L	↓	H	L	-
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X:DON'T CARE

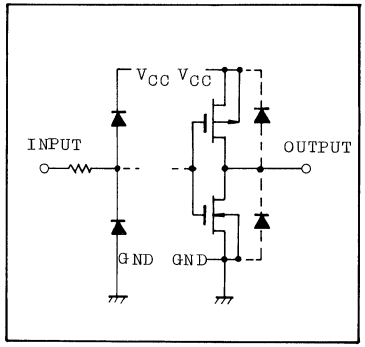
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	-	5	-	MHz
			4.5	32	58	-	27	-	
			6.0	38	68	-	32	-	

AC ELECTRICAL CHARACTERISTICS (Continued)

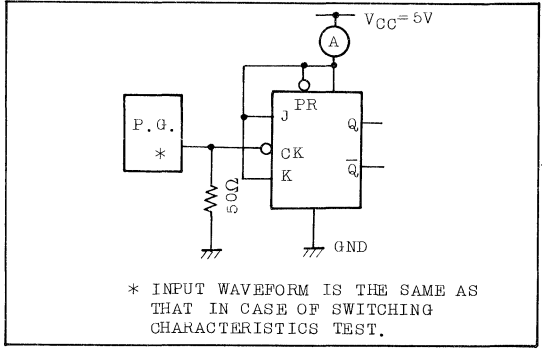
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	25	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{PR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	38	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

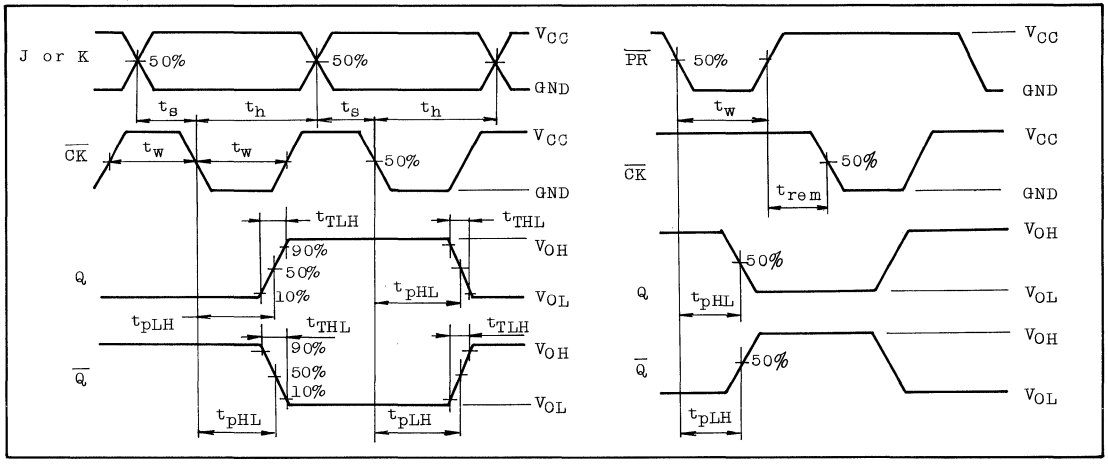
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \quad \text{(per Circuit)}$$

$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWTICHING CHARACTERISTICS TEST WAVEFORM



TC74HC123P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

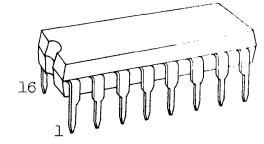
The TC74HC123, is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CL}$ INPUT (Positive-edge input). After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5KΩ to 1MΩ
..... $V_{CC}\geqq$3.0V from 1KΩ to 1MΩ

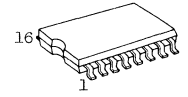
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=28ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range .... $t_{W(OUT)}$=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



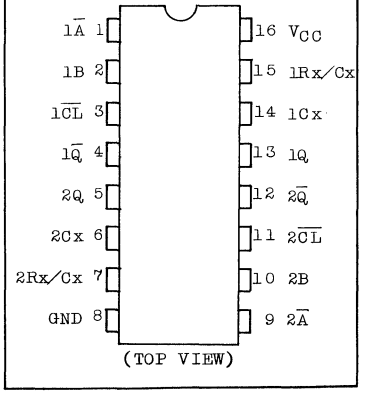
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

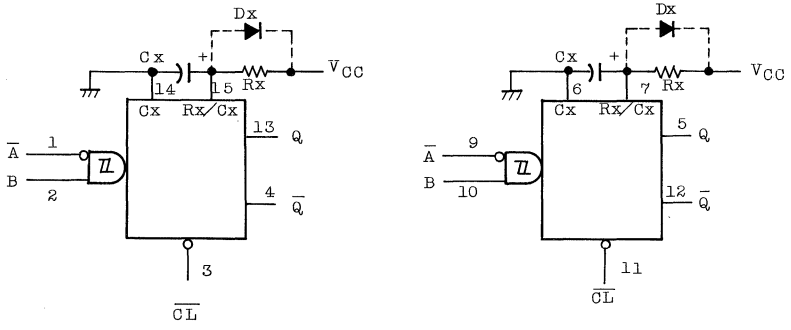


TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎎	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⎍	⎎	OUTPUT ENABLE
L	H	↑	⎍	⎎	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

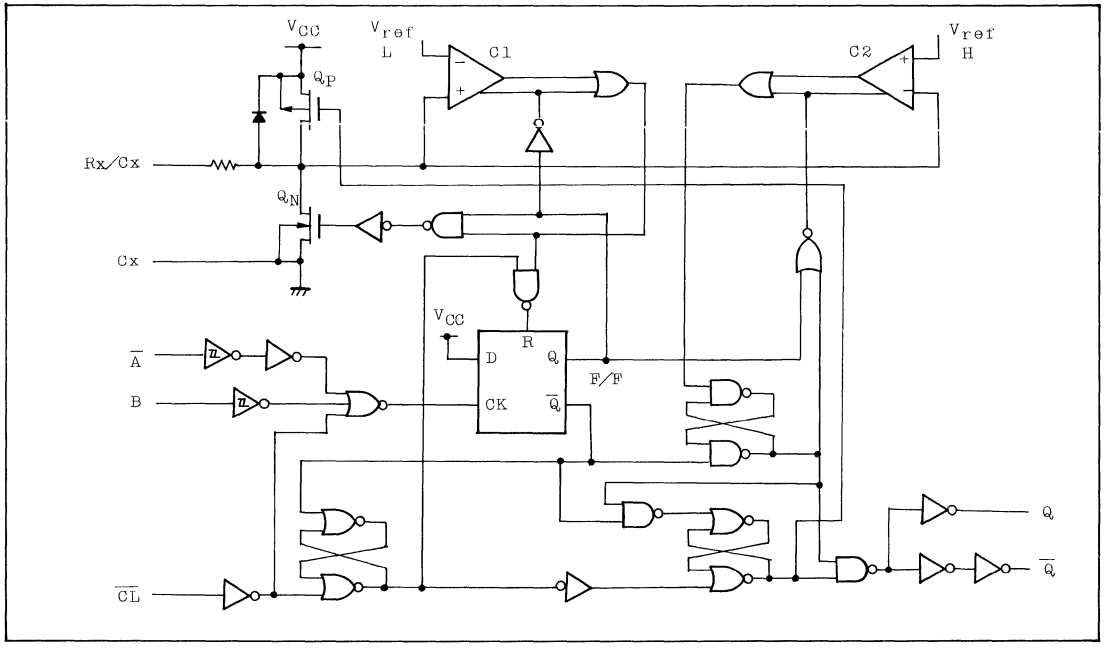
External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

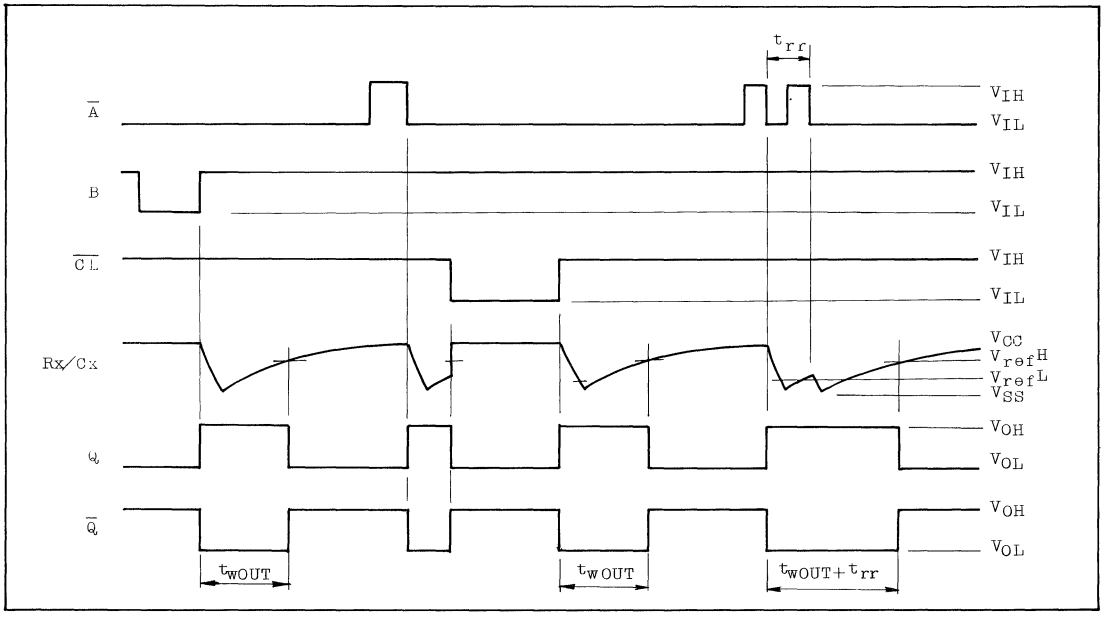
(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CL}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.46 \quad Cx\ Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

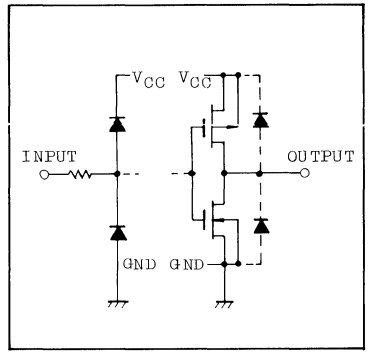
(4) Reset operation

$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=VCC or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per Circuit

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	t_{PLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{PHL}		6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)	t_{pLH}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
	t_{pHL}		6.0	-	29	45	-	55	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Minimum Pulse Width (TRIGGER)	$t_{w(H)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
	$t_{w(L)}$		6.0	-	9	17	-	21	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error Between Circuits In Same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	ns
			6.0	-	63	-	-	-	
		Cx=0.01μF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	t_{wOUT} (MIN.)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	t_{wOUT}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1μF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	113	-	-	-	

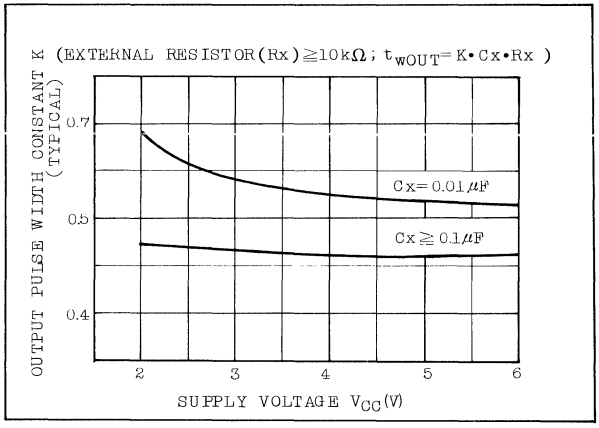
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2 \quad \text{(per monostable)}$$

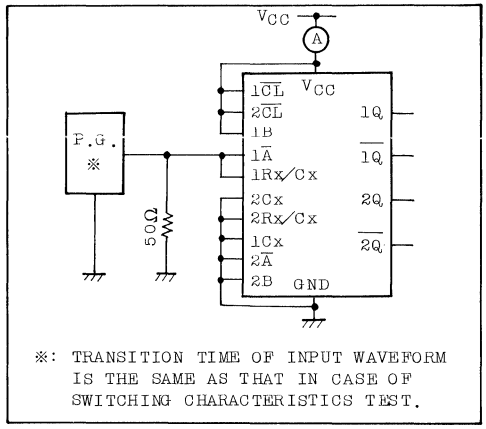
(I_{CC}': Active Supply Current)

(Duty: %)

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

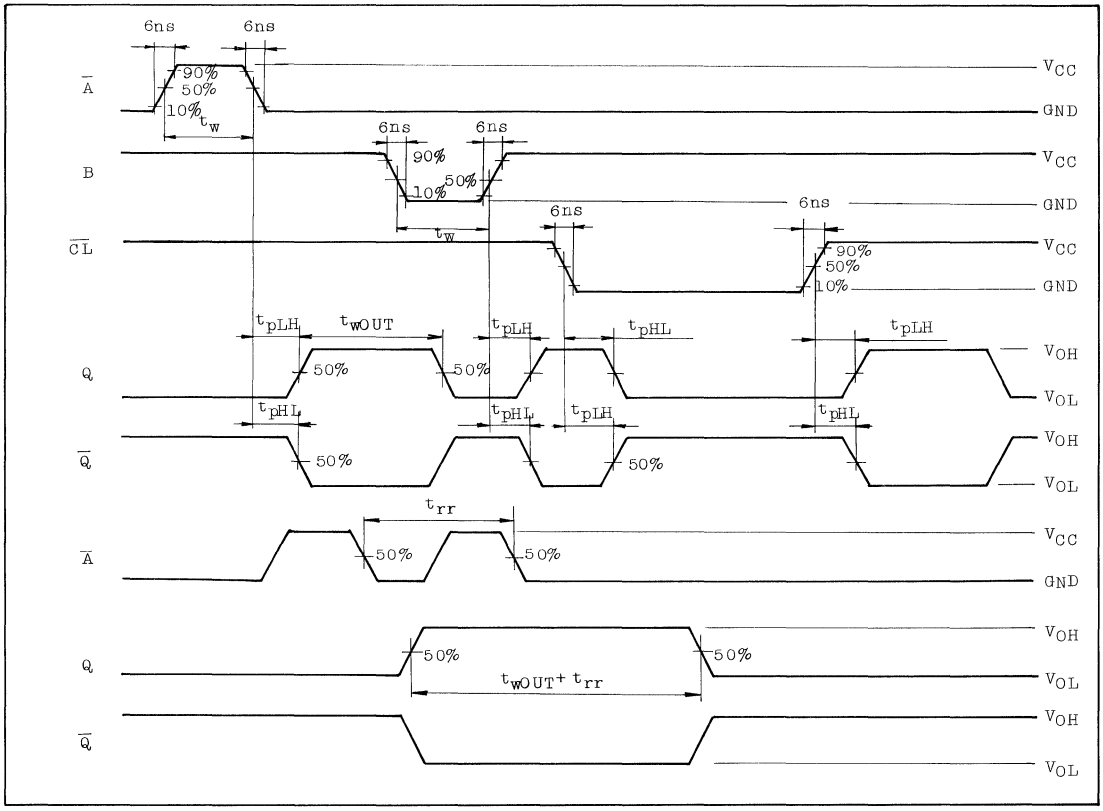


$I_{CC(opr.)}$ TEST WAVEFORM

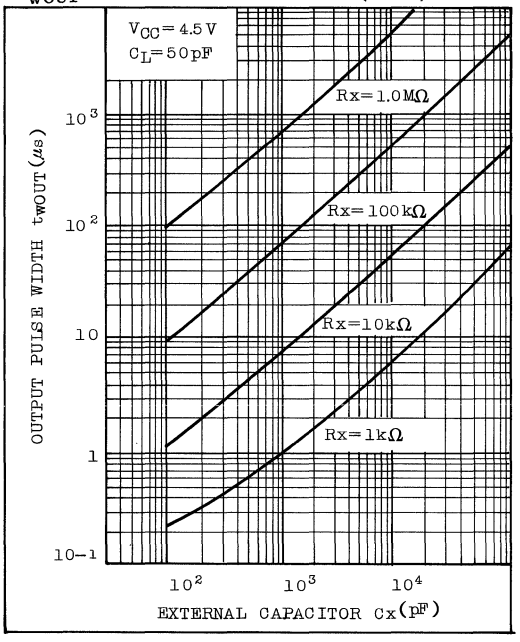


※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

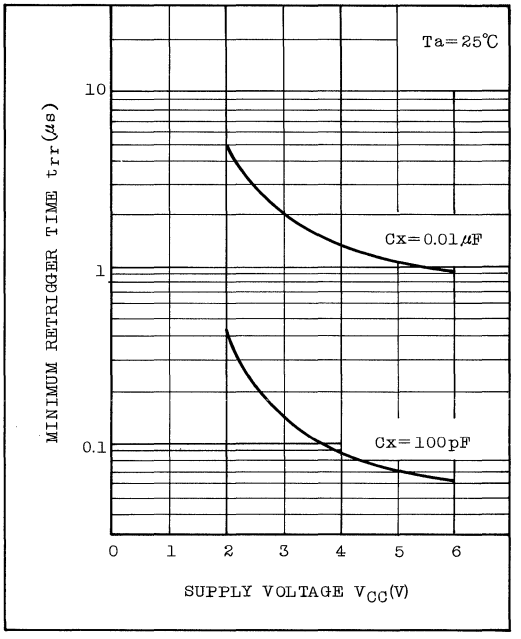
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



TC74HC125AP/AF/AFN QUAD BUS BUFFER
TC74HC126AP/AF QUAD BUS BUFFER

The TC74HC125A/126A are high speed CMOS QUAD BUS BUFFERs fabricated with silicon gate C^2MOS technology.

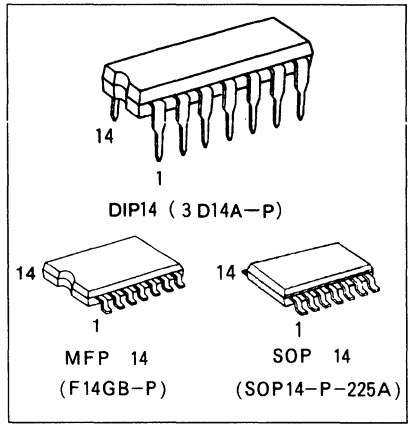
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC125A requires the 3-state control input $\overline{G}$ to be set high to place the output into the high impedance state, whereas the TC74HC126A requires the control input to be set low to place the output into high impedance.

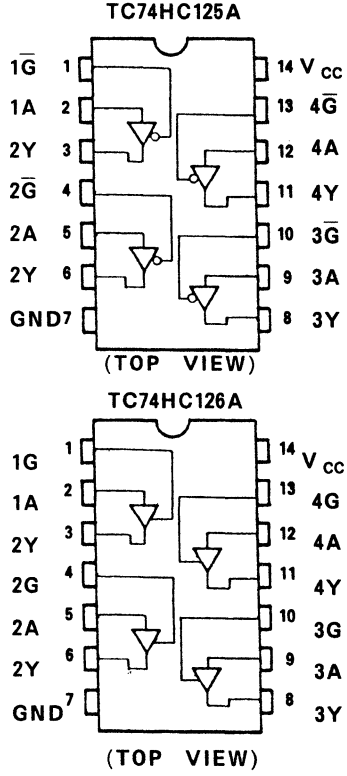
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

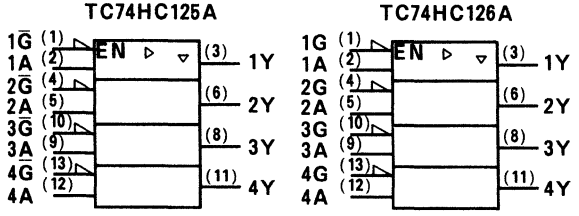
- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS125/126



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

TC74HC125A

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't Care
Z: High Impedance

TC74HC126A

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't Care
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	−	30	90	−	115	
				4.5	−	11	18	−	23	
				6.0	−	10	15	−	20	
			150	2.0	−	42	130	−	165	
				4.5	−	14	26	−	33	
				6.0	−	12	22	−	28	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1\,k\Omega$	50	2.0	−	30	90	−	115	
				4.5	−	11	18	−	23	
				6.0	−	10	15	−	20	
			150	2.0	−	42	130	−	165	
				4.5	−	14	26	−	33	
				6.0	−	12	22	−	28	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	24	100	−	125	
				4.5	−	12	20	−	25	
				6.0	−	10	17	−	21	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	41	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC131AP/AF

3-TO-8 LINE DECODER/LATCH

The TC74HC131A is a high speed CMOS 3-to-8 LINE DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

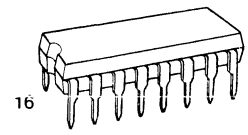
It is composed of 3-bit input register with a common CLOCK input and 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into input register on the positive going transition of the clock pulse. The value of the binary data determines which one of outputs will go to low.

When enable input G1 held low or $\overline{G2}$ is held high, the decoding function is inhibited and all outputs go high. These enable inputs are provided for cascade connection and for use as an address decoder for memory systems.

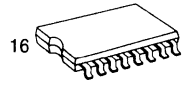
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V

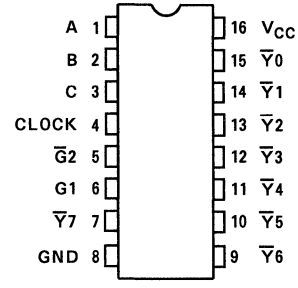


DIP16 (3D16A-P)



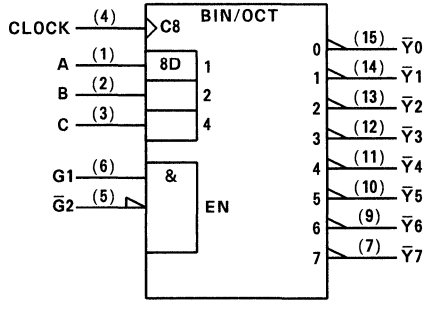
MFP16 (F16GC-P)

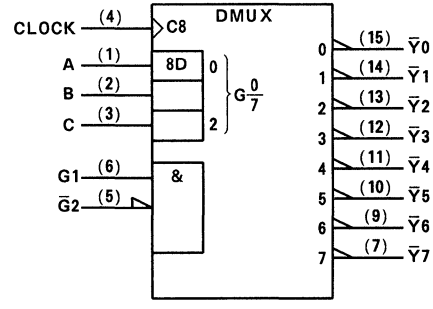
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



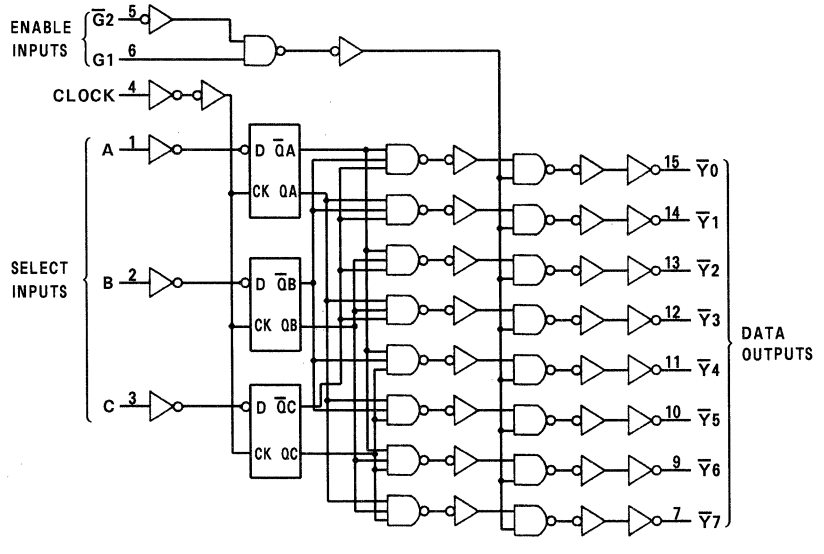


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE		CLOCK	SELECT											
G1	$\overline{G2}$		C	B	A	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	↑	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}0$
H	L	↑	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}1$
H	L	↑	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}2$
H	L	↑	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}3$
H	L	↑	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}4$
H	L	↑	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}5$
H	L	↑	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}6$
H	L	↑	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}7$
H	L	↓	X	X	X	NO CHANGE								

X : DON'T CARE

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.13	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B, C)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−$\overline{Y}$)	t_{pLH} t_{pHL}		−	22	35	
Propagation Delay Time (G1, G2−$\overline{Y}$)	t_{pLH} t_{pHL}		−	12	24	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	78	200	−	240	
			4.5	−	26	40	−	48	
			6.0	−	22	34	−	41	
Propagation Delay Time (G1, $\overline{G2}$−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	60	140	−	175	
			4.5	−	15	28	−	35	
			6.0	−	13	24	−	30	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	37	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC132AP/AF/AFN

QUAD 2-INPUT SCHMITT NAND GATE

The TC74HC132A is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fabricated with silicon gate C^2MOS technology.

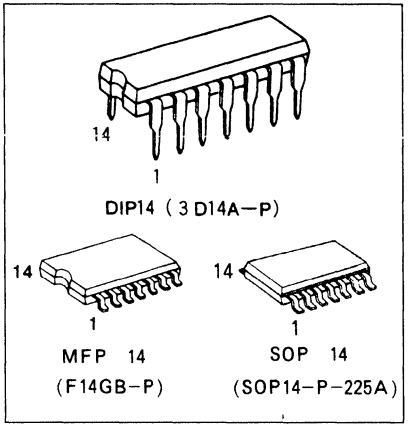
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HC00A but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger inputs, the TC74HC132A can be used as a line receiver for slow input signals.

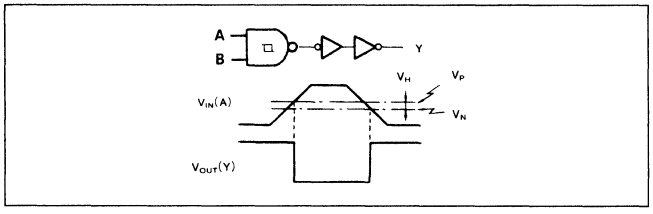
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

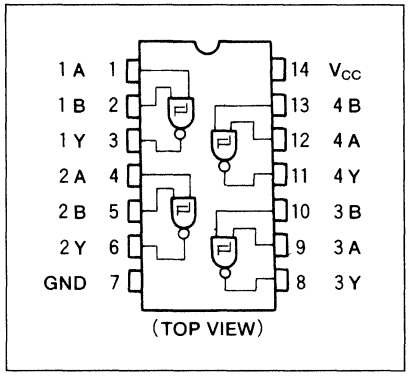
- High Speed ····· t_{pd}=11ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{IH}=1.1V at V_{CC}=5V
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS132



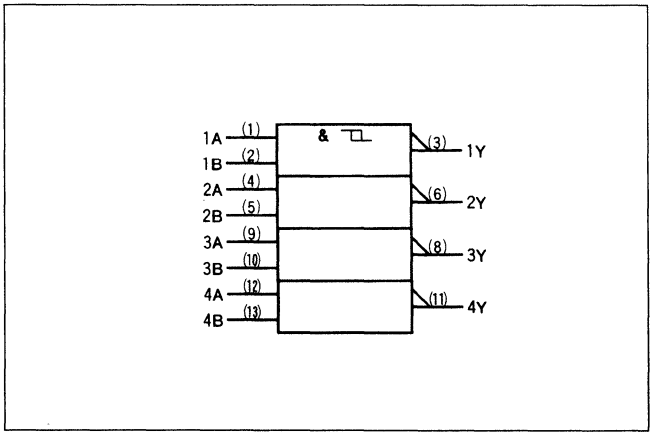
SYSTEM DIAGRAM,WAVEFORM



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			2.0	1.0	1.25	1.5	1.0	1.5	V
				4.5	2.3	2.7	3.15	2.3	3.15	
				6.0	3.0	3.5	4.2	3.0	4.2	
Negative Threshold Voltage	V_N			2.0	0.3	0.65	0.9	0.3	0.9	V
				4.5	1.13	1.6	2.0	1.13	2.0	
				6.0	1.5	2.3	2.6	1.5	2.6	
Hysteresis Voltage	V_H			2.0	0.3	0.6	1.0	0.3	1.0	V
				4.5	0.6	1.1	1.4	0.6	1.4	
				6.0	0.8	1.2	1.7	0.8	1.7	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =Vcc or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =Vcc or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	18	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	110	–	140	ns
			4.5	–	14	22	–	28	
			6.0	–	12	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	29	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC133AP/AF

13-INPUT NAND GATE

The TC74HC133A is a high speed CMOS 13-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

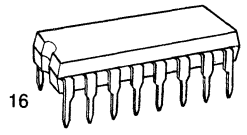
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 7 stages, including a buffer output, which provide high noise immunity and stable output.

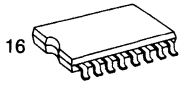
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS133

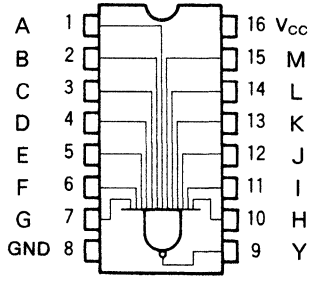


DIP16 (3D16A-P)



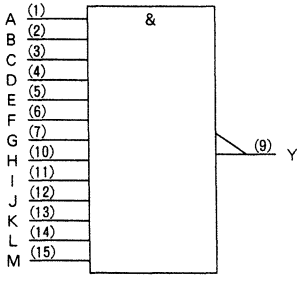
MFP16 (F16GC-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs	Outputs
All Inputs High	L
All Other Combinations	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25℃, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	13	22	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25℃			Ta = −40 ~ 85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	130	–	165	ns
			4.5	–	16	26	–	33	
			6.0	–	14	22	–	28	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	29	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

3-TO-8 LINE DECODER/LATCH

The TC74HC137A is a high speed CMOS 3-to-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

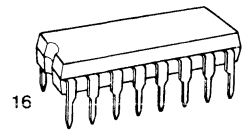
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is composed of a 3-bit input latches with a common $\overline{GL}$ enable input and a 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of the outputs will go low. When the enable input G1 is held low or $\overline{G2}$ is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application of address decoder for memory system.

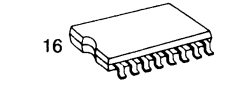
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS137

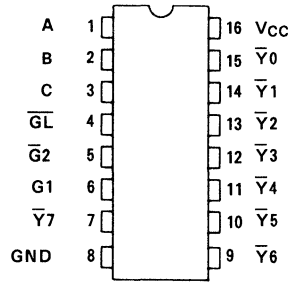


DIP16 (3D16A-P)



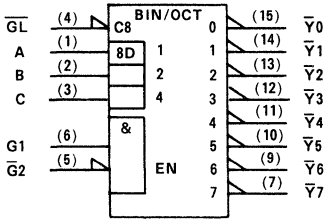
MFP16 (F16GC-P)

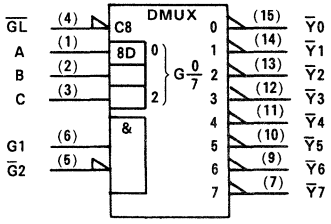
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



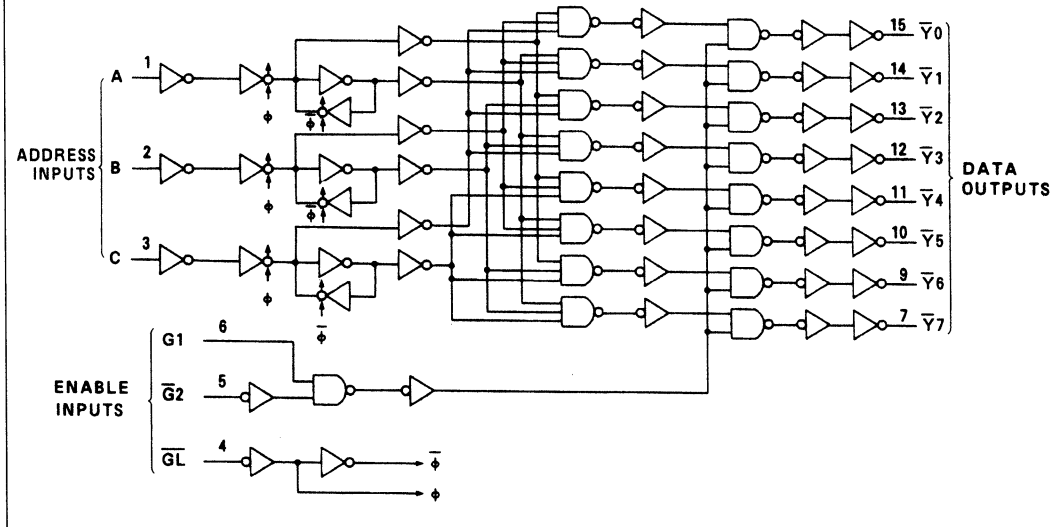


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			ADDRESS											
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
L	L	H	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
L	L	H	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
L	L	H	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
L	L	H	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
L	L	H	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
L	L	H	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
L	L	H	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
L	L	H	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$
H	L	H	X	X	X	OUTPUTS are latched at the time when $\overline{GL}$ is taken High level.								

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C−$\overline{GL}$)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B, C−$\overline{GL}$)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		−	11	19	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		−	12	19	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	18	29	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH} t_{pHL}		−	17	28	

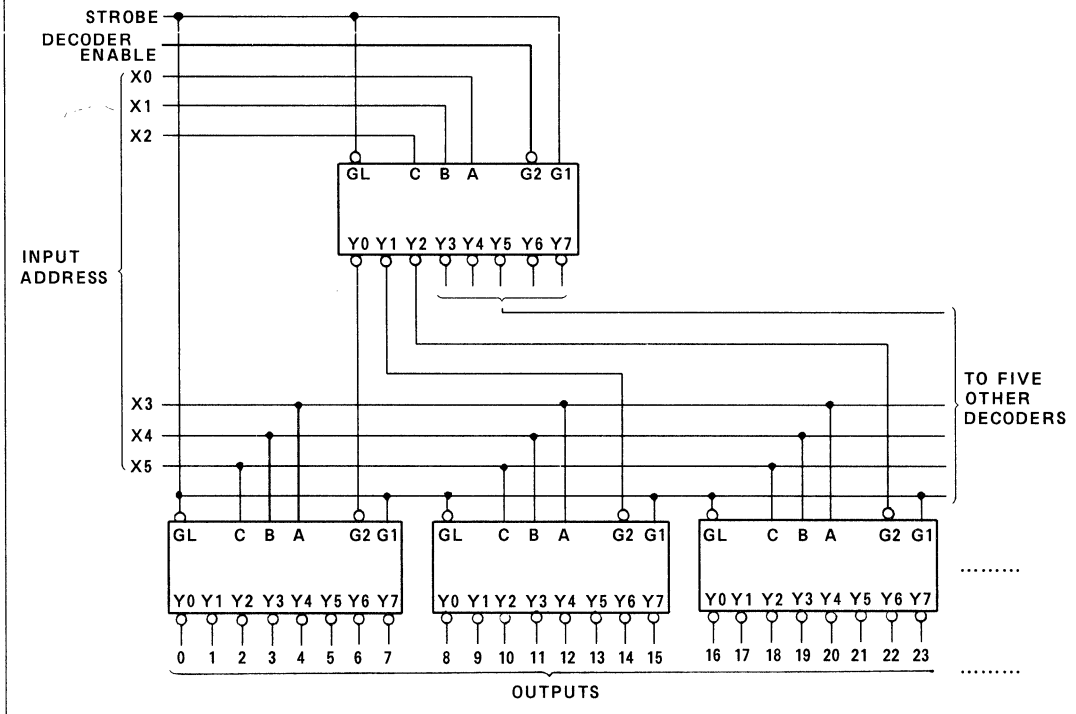
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	45	115	−	145	
			4.5	−	14	23	−	29	
			6.0	−	12	20	−	25	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	50	115	−	145	
			4.5	−	15	23	−	29	
			6.0	−	13	20	−	25	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	70	170	−	215	
			4.5	−	22	34	−	43	
			6.0	−	19	29	−	37	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	70	165	−	205	
			4.5	−	21	33	−	41	
			6.0	−	18	28	−	35	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	56	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

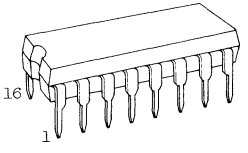
TC74HCT137P/F

TC74HCT137P/F 3-TO-8 LINE DECODER/LATCH

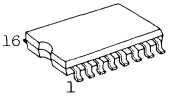
The TC74HCT137 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go low. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS137



DIP16(3D16A-P)



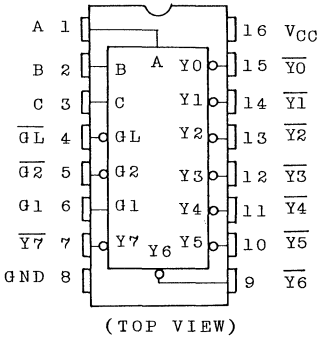
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



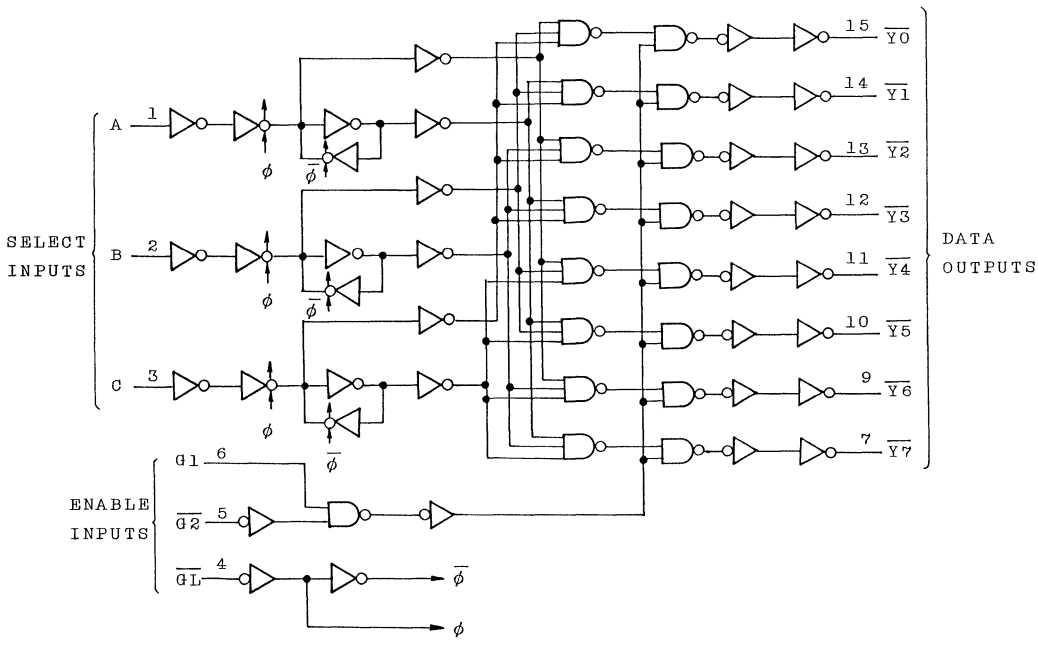
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	Output corresponding to stored address, L; all others, H							

X : DON'T CARE

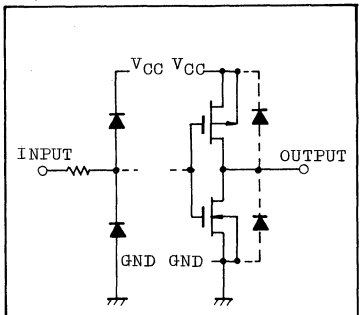
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

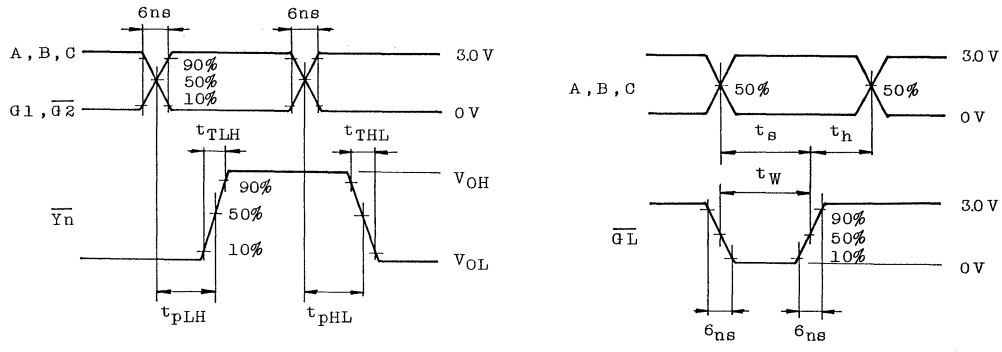
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	25	39	-	49	
Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	24	37	-	46	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	34	52	-	65	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	29	45	-	56	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		4.5	-	8	15	-	19	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		4.5	-	2	10	-	13	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		4.5	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	68	-	-	-	

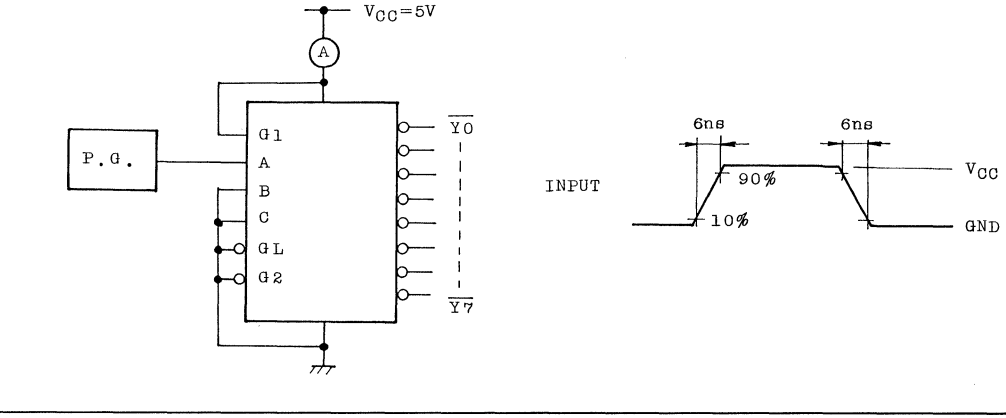
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

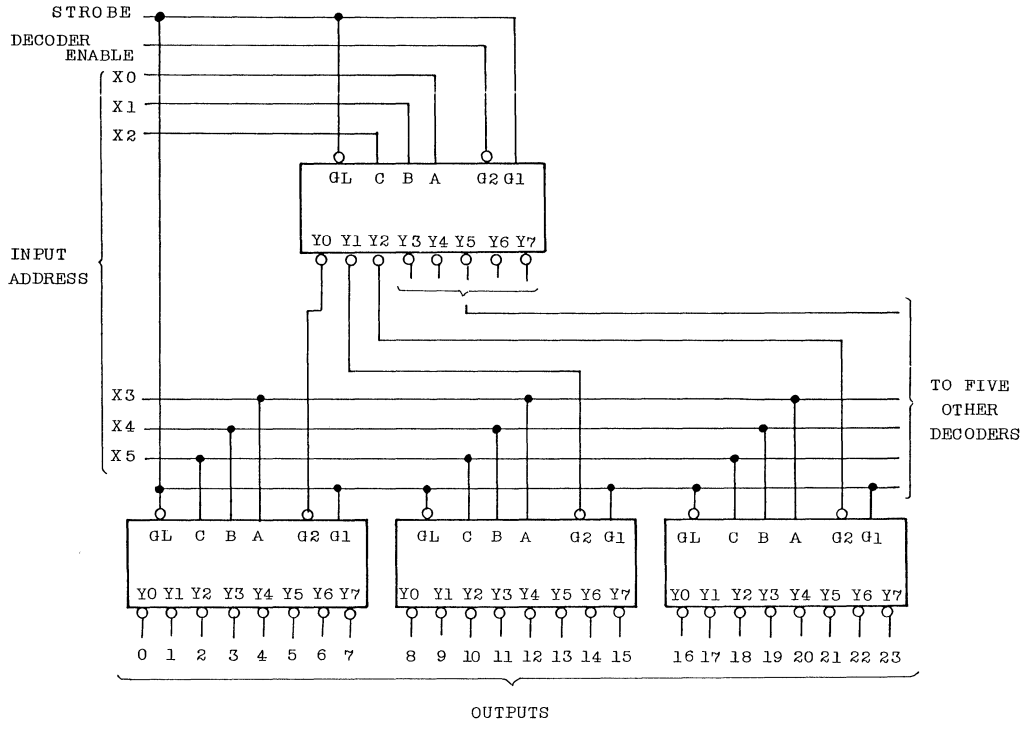
SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HC138AP/AF/AFN

3-TO-8 LINE DECODER

The TC74HC138A is a high speed CMOS 3-to-8 DECODER fabricated with sillicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs ($\overline{Y}0$-$\overline{Y}1$) will go low.

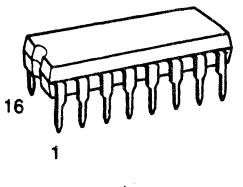
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

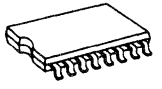
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

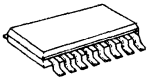
- High Speed ····· t_{pd}=16ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS138.



DIP16 (3D16A-P)

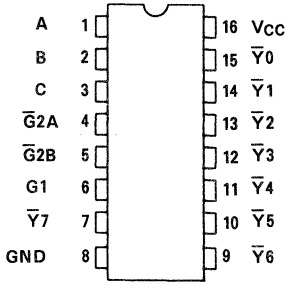


MFP 16
(F16GC-P)



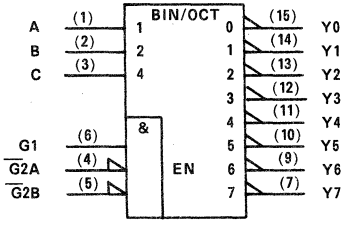
SOP 16
(SOP16-P-225A)

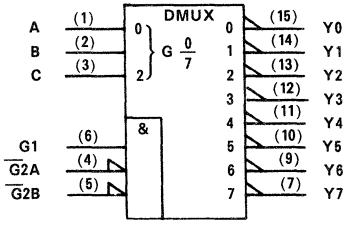
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



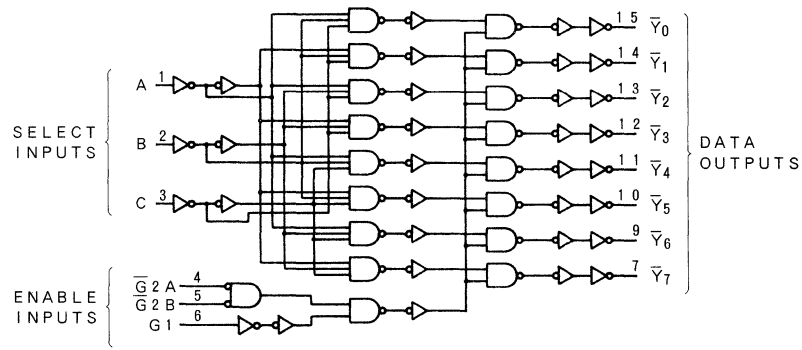


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		–	16	26	
Propagation Delay Time (G,$\overline{G}$−$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	25	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	70	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	16	26	–	32	
Propagation Delay Time (G,$\overline{G}$−$\overline{Y}$)	t_{pLH} t_{PLH}		2.0	–	65	145	–	180	
			4.5	–	18	29	–	36	
			6.0	–	15	25	–	31	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	47	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HCT138AP/AF/AFN

3-TO-8 LINE DECODER

The TC74HCT138A is a high speed CMOS 3-to-8 LINE DECODER fabricated with sillicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs (Y0-Y1) will go low.

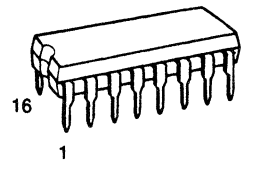
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

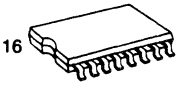
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

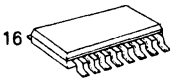
- High Speed ..... t_{pd}=17ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs..... V_{IH} =2V (Min.)
  V_{IL} =0.8V(Max.)
- Wide interfacing ability.....LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Pin and Function Compatible with 74LS138.



DIP16 (3D16A-P)

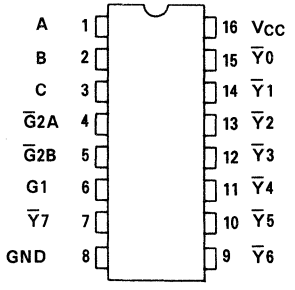


MFP 16
(F16GC-P)



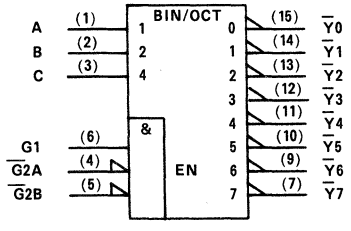
SOP 16
(SOP16-P-225A)

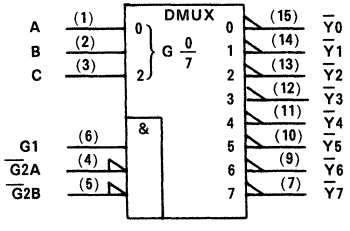
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



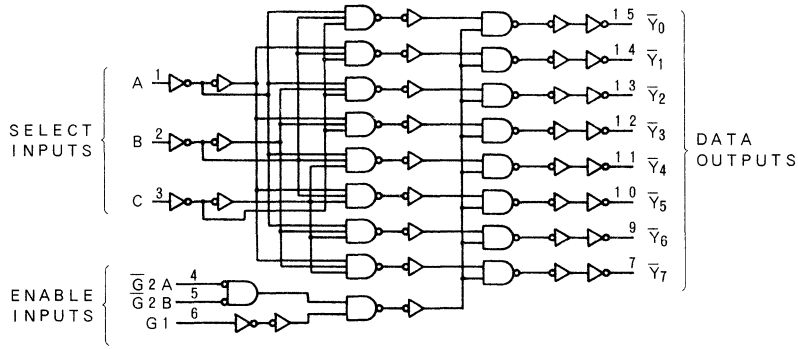


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 500$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ～ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ～ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$I_{OH}=-20\ \mu A$	4.5	4.4	4.5	−	4.4	−	V
			$I_{OH}=-4$ mA	4.5	4.18	4.31	−	4.13	−	
High−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	$I_{OL}=20\ \mu A$	4.5	−	0.0	0.1	−	0.1	V
			$I_{OL}=4$ mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	± 0.1	−	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	I_C	PER INPUT: V_{IN}=0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		–	17	28	
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	25	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		–	17	28	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	21 18	33 30	– –	44 40	
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	19 17	30 27	– –	38 34	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	22 20	33 30	– –	41 37	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	55	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC139AP/AF/AFN

DUAL 2-TO-4 LINE DECODER

The TC74HC139A is a high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

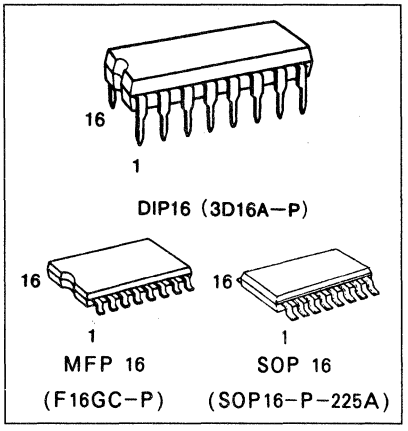
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held "H", all four outputs are fixed at a high logic level independent of the other inputs.

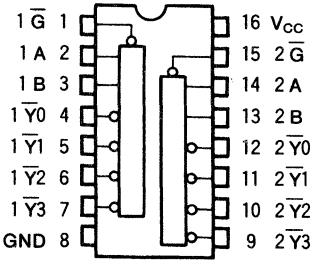
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.

FEATURES:

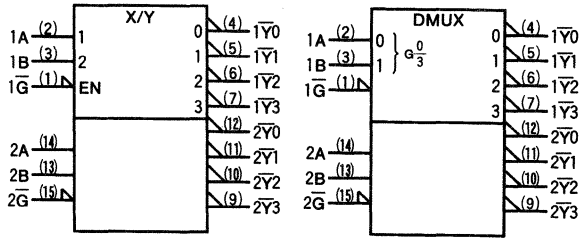
- High Speed ..... t_{pd}=16ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS139



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
G̅	B	A	Y̅0	Y̅1	Y̅2	Y̅3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y̅0
L	L	H	H	L	H	H	Y̅1
L	H	L	H	H	L	R	Y̅2
L	H	H	H	H	H	L	Y̅3

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B−$\overline{Y}$)	t_{pLH} t_{pHL}		–	12	22	
Propagation Delay Time ($\overline{G}$−Y)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	45	130	–	165	
			4.5	–	15	26	–	33	
			6.0	–	13	22	–	28	
Propagation Delay Time ($\overline{G}$−Y)	t_{pLH} t_{pHL}		2.0	–	39	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	11	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	46	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

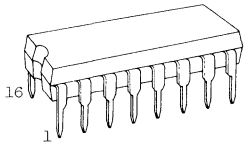
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

TC74HC147P/F 10-TO-4 LINE PRIORITY ENCODER

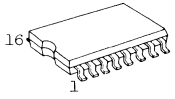
The TC74HC147 is a high speed CMOS 10-TO-4 LINE PRIORITY ENCODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS147



DIP16(3D16A-P)



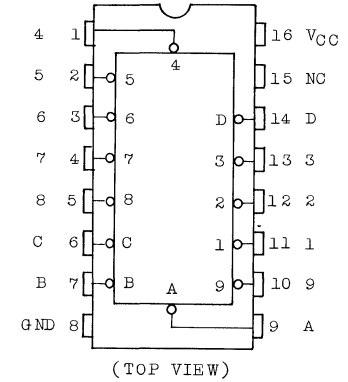
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



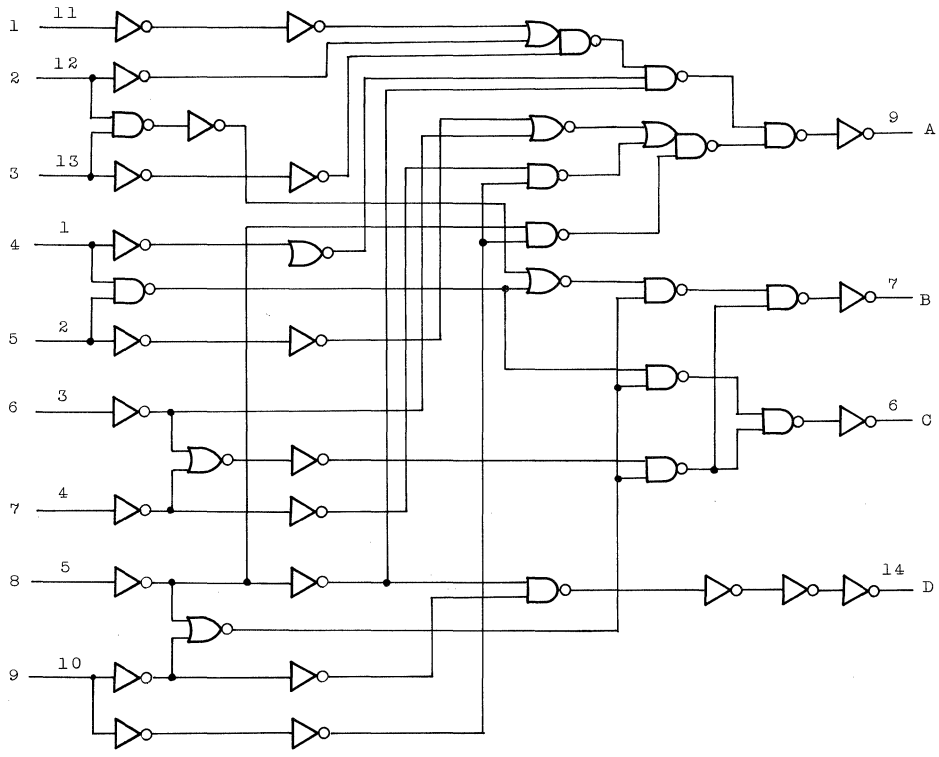
(TOP VIEW)
NC : NO CONNECTION

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

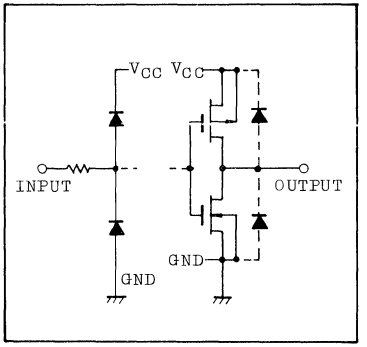
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

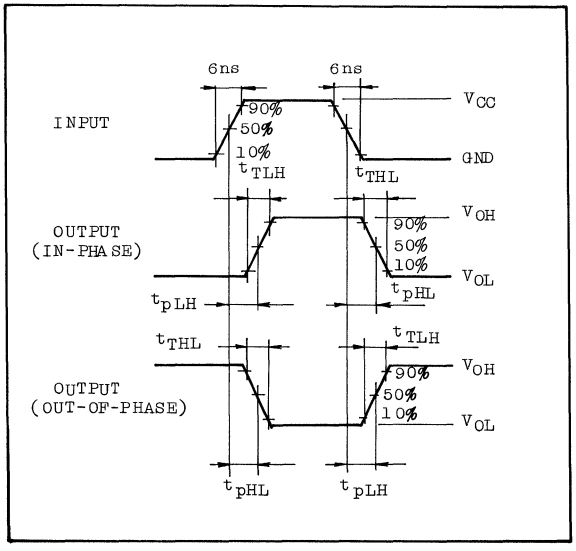
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	37	-	-	-	

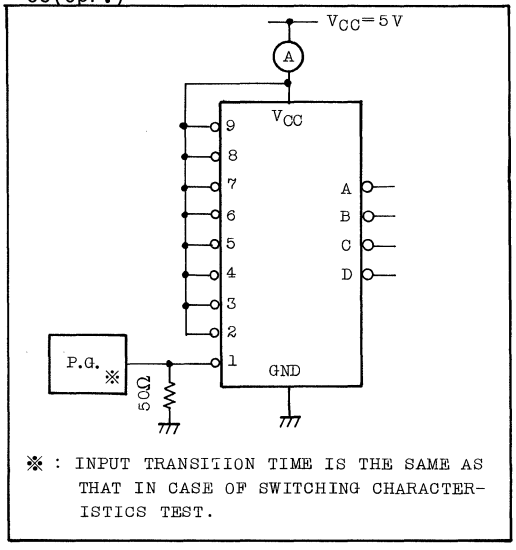
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST WAVEFORM



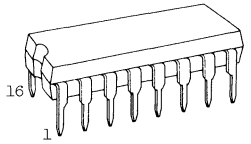
※ : INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC148P/F 8-TO-3 LINE PRIORITY ENCODER

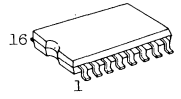
The TC74HC148 is a high speed CMOS 8-TO-3 LINE PRIORITY ENCODER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The encoder detects "L" level of the highest order among eight input signals and outputs the corresponding signal position in binary code. The inputs are eight input signals of 0 through 7 and input EI and when EI is set to "H" level, the encode operation is inhibited making all the outputs at "H" level. The encoded output appears on three signal lines A0 through A2 in binary. Outputs EO and GS are the outputs to indicate the operational mode of encoder and used when the number of bits is to be increased by cascade connection. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS148



DIP16(3D16A-P)



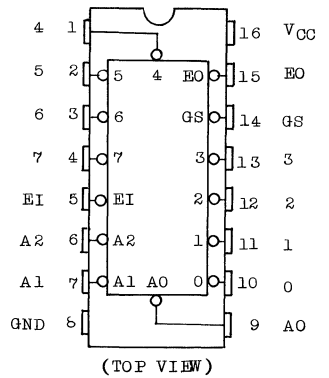
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



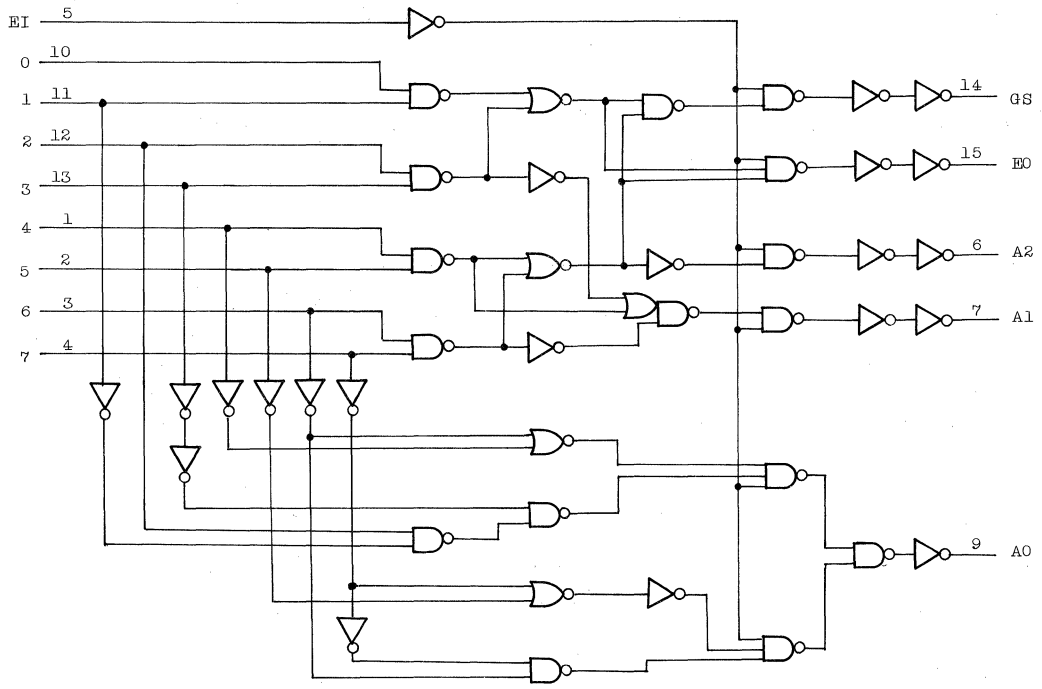
(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X : Don't Care

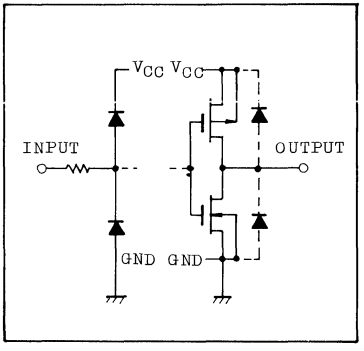
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

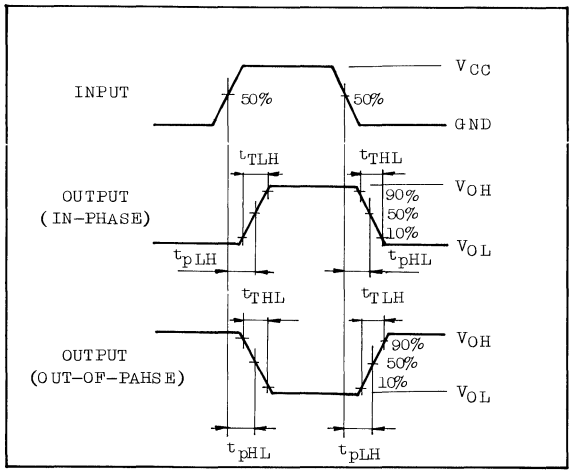
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (IN - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (IN - EO, GS)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (EI - EO)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (EI - GS)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Propagation Delay Time (EI - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10		10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	57	-	-	-	

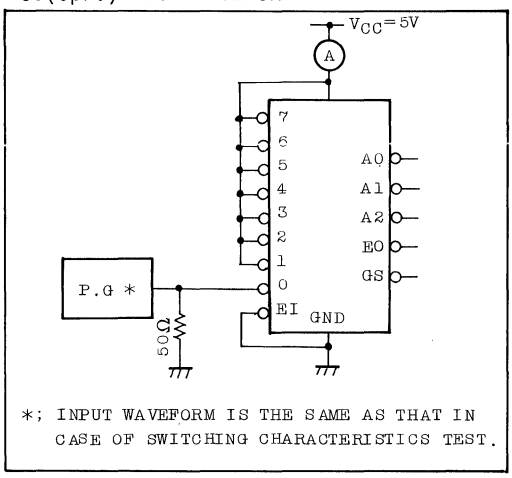
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



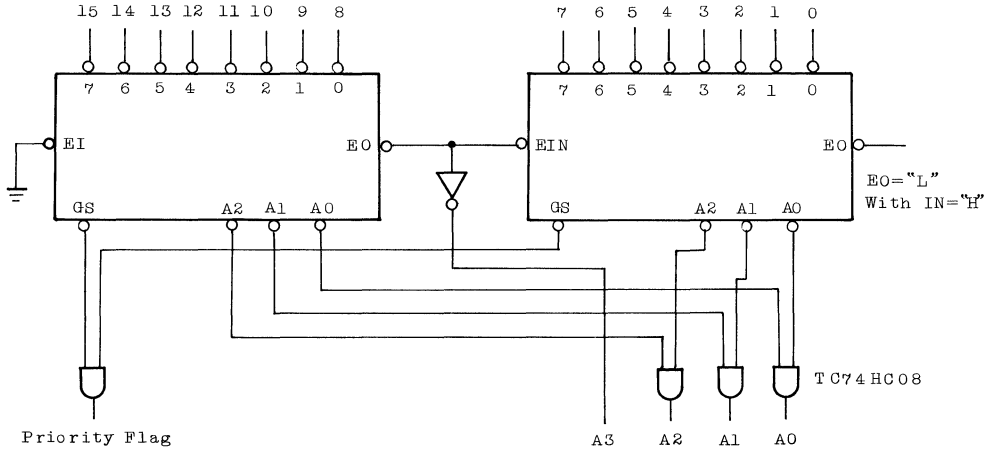
I_{CC}(Opr.) TEST WAVEFORM



*; INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

4-bit CASCADE CONNECTION



TC74HC151AP/AF/AFN

8-CHANNEL MULTIPLEXER

The TC74HC151A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

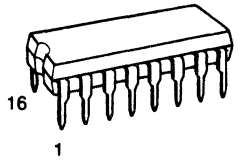
One of eight date input signals (D0–D7) is selected by decoding of the three-bit address input (A, B, C). The selected data appears on two outputs : non-inverting (Y) and inverting (W).

The strobe input provides two output conditions ; a low level on the strobe input transferrs the selected data to the outputs. A high level on the strobe input sets the Y output low and the W output high without regard to the data or select input conditions.

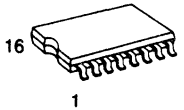
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

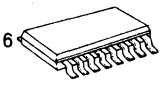
- High Speed ····· t_{pd} =15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS151



DIP16 (3D16A-P)

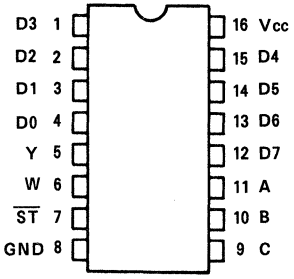


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



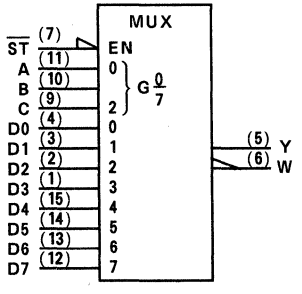
(TOP VIEW)

TRUTH TABLE

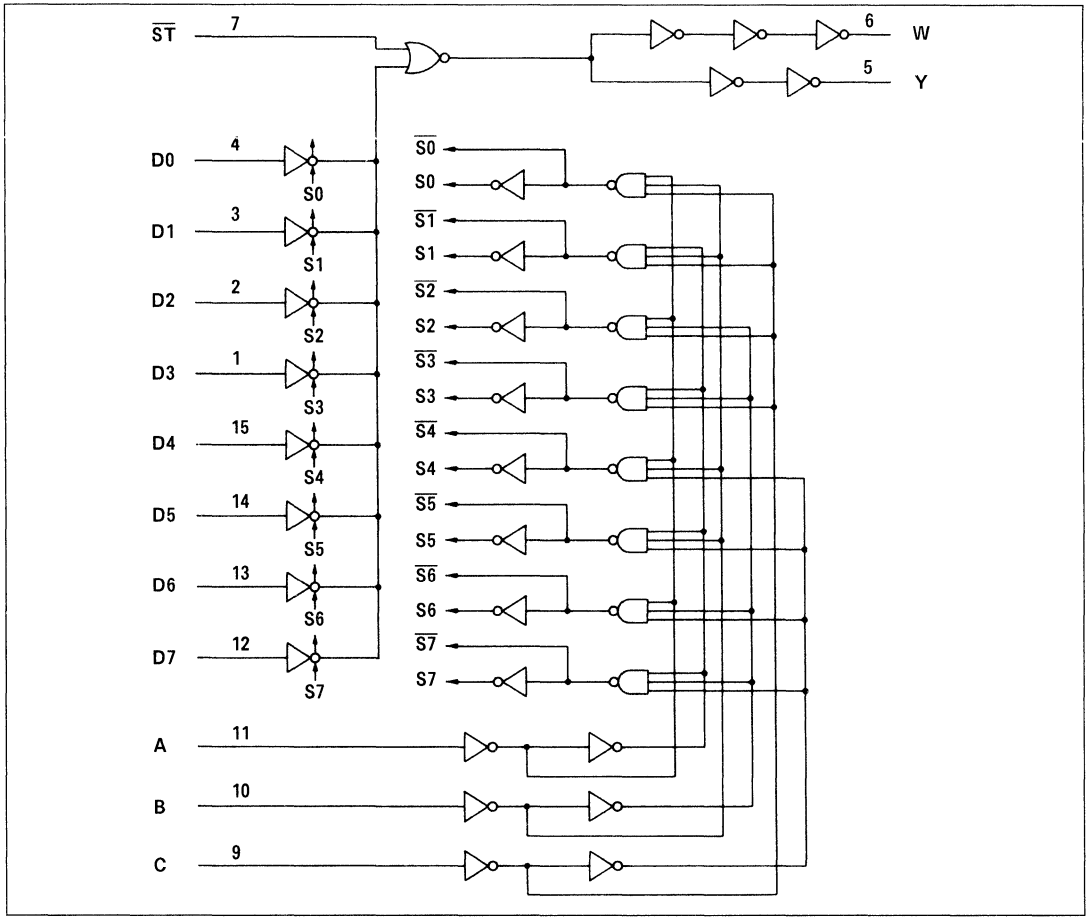
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{ST}$		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time ($\overline{ST}$–Y)	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time ($\overline{ST}$–W)	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		–	19	31	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time ($\overline{ST}$–Y)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time ($\overline{ST}$–W)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	69	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC153P/F
TC74HC253P/F

TC74HC153P/F DUAL 4-CHANNEL MULTIPLEXER

TC74HC253P/F DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74HC153 and TC74HC253 are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

Both achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipations.

The designer has a choice of complementary output (HC153) and 3-state output (HC253).

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

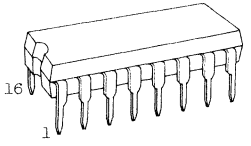
Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections.

The strobe input ($\overline{G}$) can be used to inhibit the data output; the output of HC153 is fixed in low level and the output of HC253 is disabled to be high impedance unconditionally, while the strobe input is held low.

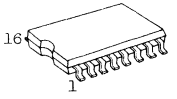
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS153/253.

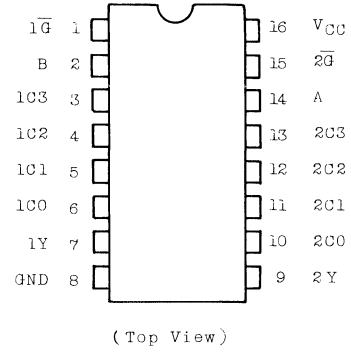


DIP16(3D16A-P)

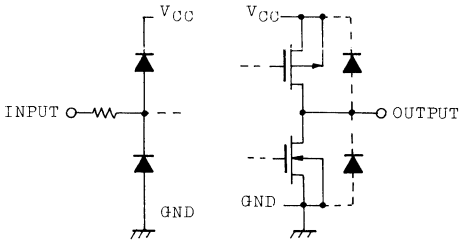


MFP16(F16GC-P)

PIN ASSIGNMENT



INPUT and OUTPUT EQUIVALENT CIRCUIT



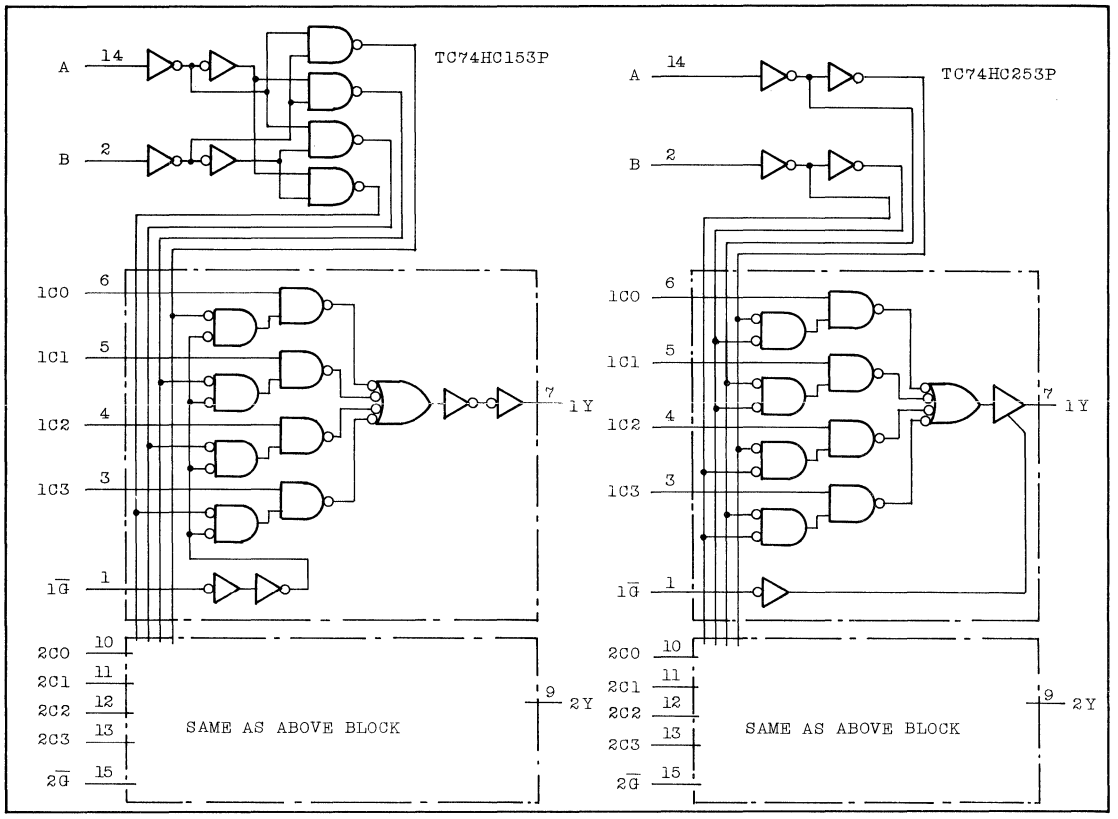
TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC153	HC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X : Don't care

Z : High Impedance

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}(1)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

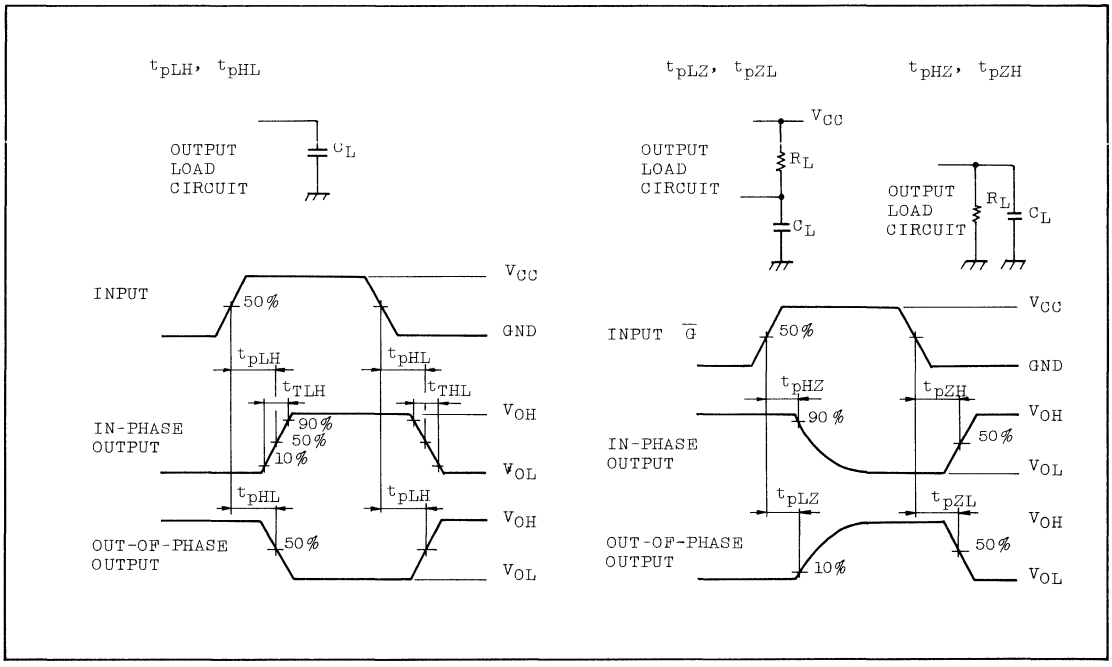
Note (1) Applied only for TC74HC253P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

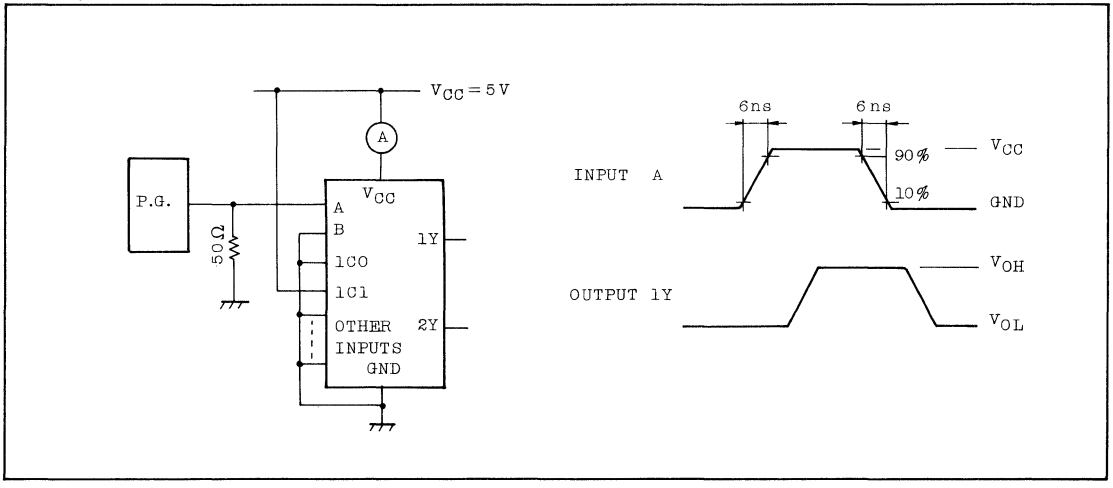
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	75	-	95	ns
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
TC74HC153/253 Propagation Delay Time C_n - Y	t_{pLH} t_{pHL}		2.0	-	68	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
TC74HC153/253 A,B - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC153 Propagation Delay Time $\overline{G}$ - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC253 Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	46	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
TC74HC253 Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	TC74HC253		-	7	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC153		-	56	-	-	-	
		TC74HC253		-	56	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Channel)

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC154AP

4-TO-16 LINE DECODER

The TC74HC154A is high speed CMOS 4 to 16 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C MOS technology.

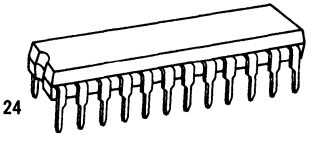
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A binary code applied to the four inputs Athru D is decoded within the device. Depending on the binary code, causes one of sixteen outputs to go low, when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are held low. When either strobe input is held high, the decoding function is inhibited to keep all outputs high. The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decoding circuits in a memory control system.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

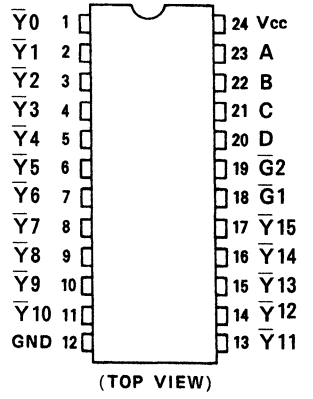
FEATURES:

- High Speed ····· t_{pd}=15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS154



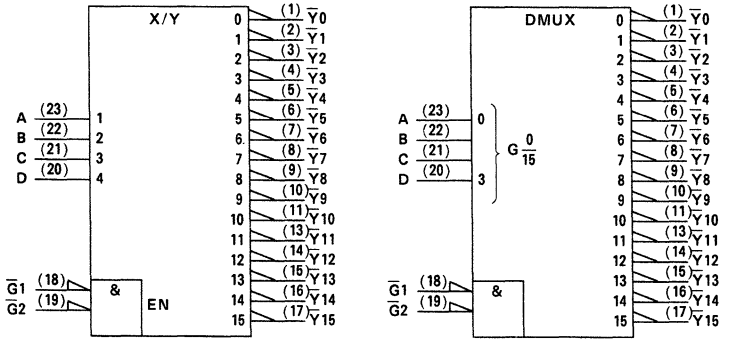
DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

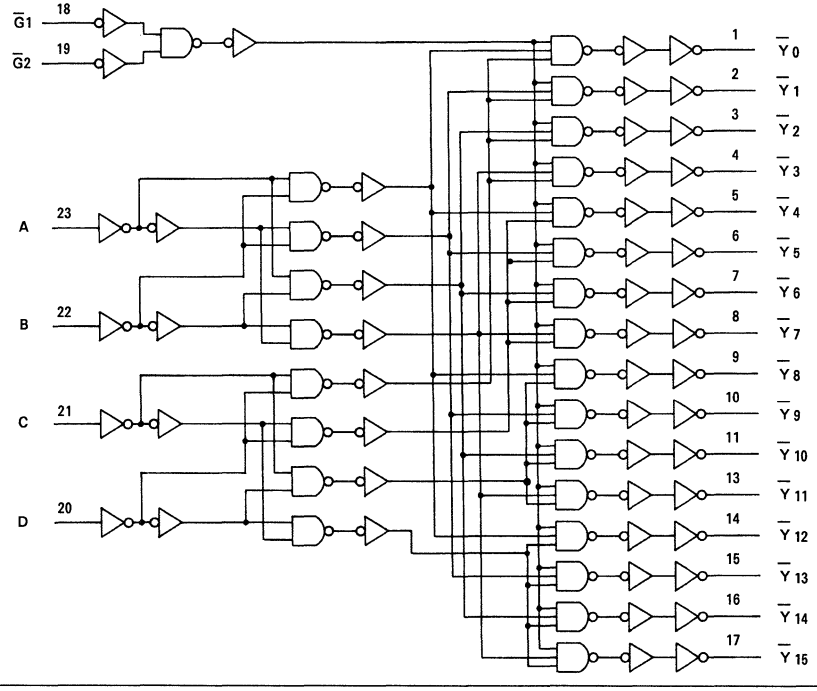


TRUTH TABLE

INPUT						SELECTED OUTPUT(L)
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y}0$
L	L	L	L	L	H	$\overline{Y}1$
L	L	L	L	H	L	$\overline{Y}2$
L	L	L	L	H	H	$\overline{Y}3$
L	L	L	H	L	L	$\overline{Y}4$
L	L	L	H	L	H	$\overline{Y}5$
L	L	L	H	H	L	$\overline{Y}6$
L	L	L	H	H	H	$\overline{Y}7$
L	L	H	L	L	L	$\overline{Y}8$
L	L	H	L	L	H	$\overline{Y}9$
L	L	H	L	H	L	$\overline{Y}10$
L	L	H	L	H	H	$\overline{Y}11$
L	L	H	H	L	L	$\overline{Y}12$
L	L	H	H	L	H	$\overline{Y}13$
L	L	H	H	H	L	$\overline{Y}14$
L	L	H	H	H	H	$\overline{Y}15$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r , t_f	0~1000(V_{CC} =2.0V) 0~ 500(V_{CC} =4.5V) 0~ 400(V_{CC} =6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.5 3.15 4.2	− − −	− − −	1.5 3.15 4.2	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.5 1.35 1.8	− − −	0.5 1.35 1.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH}=−4 mA I_{OH}=−5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=4 mA I_{OL}=5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B, C, D–$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	30	
Propagation Delay Time ($\overline{G}1$, $\overline{G}2$–$\overline{Y}$)	t_{pLH} t_{pHL}		–	14	28	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B, C, D–$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	65	175	–	220	
			4.5	–	19	35	–	44	
			6.0	–	16	30	–	37	
Propagation Delay Time ($\overline{G}1$, $\overline{G}2$–Y)	t_{pLH} t_{pHL}		2.0	–	55	160	–	200	
			4.5	–	17	32	–	40	
			6.0	–	15	27	–	34	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	57	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC155AP/AF/AFN

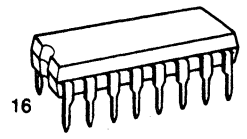
DUAL 2-TO-4 LINE DECODER/DUAL 3-TO-8 LINE DECODER

The TC74HC155A is a high speed CMOS DUAL 2-to-4 LINE DECODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It features dual 1-to-4 line demultiplexers with individual strobe input(1G and 2G),individual data inputs(1C and 2C)and common binary address inputs(A and B).
When both decoders are enabled by the strobes,the inverted output of 1C data and non-inverted output of 2C data will be brought to the selected output pins of each section.
A 1-to-8 line demultiplexer can be easily built up by providing a data signal to both the 1C and 2C inputs;the output order will be 1Y3(MSB),1Y2,1Y1,1Y0,2Y3,2Y2,2Y1,2Y0(LSB).
This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and 2C is held low.

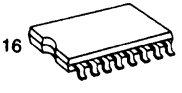
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

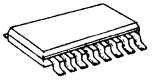
- High Speed ····· t_{pd} =12ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS155



DIP16 (3D16A-P)

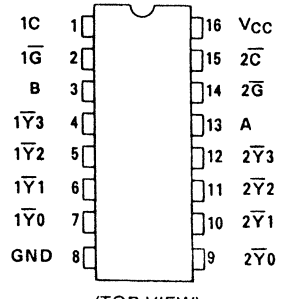


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

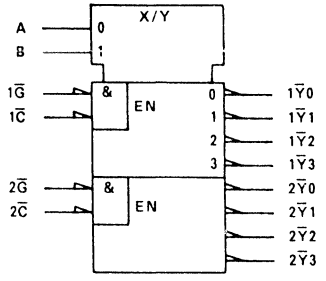
INPUTS				OUTPUTS			
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X : DON'T CARE

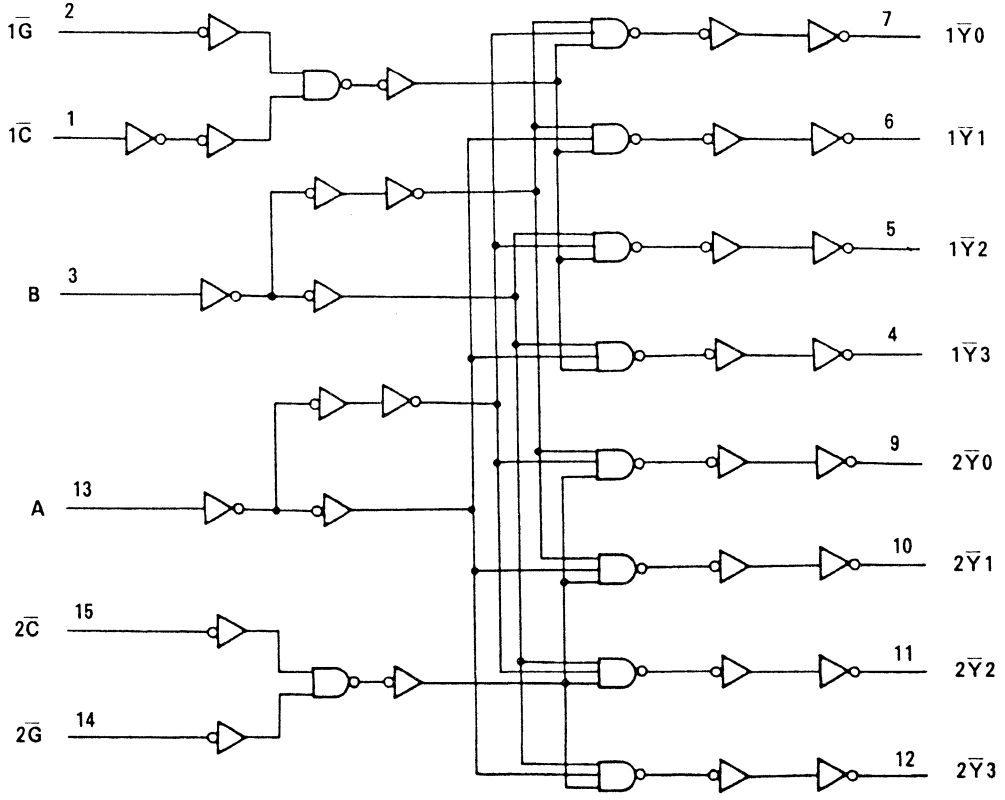
INPUTS				OUTPUTS			
B	A	2G	2C	2Y0	2Y1	2Y3	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

X : DON'T CARE

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	12	22	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	45	130	–	165	ns
			4.5	–	15	26	–	33	
			6.0	–	13	22	–	28	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	(Note 1)		–	53	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC157AP/AF/AFN
TC74HC158AP/AF/AFN

TC74HC157AP/AF/AFN QUAD 2-CHANNEL MULTIPLEXER
TC74HC158AP/AF/AFN QUAD 2-CHANNEL MULTIPLEXER(INVERTING)

The TC74HC157A and TC74HC158A are high speed CMOS 2-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC158A is an inverting multiplexer while the TC74HC157A is a non-inverting.

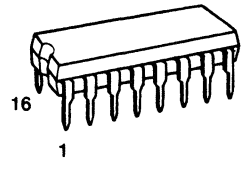
When $\overline{\text{STROBE}}$ is held high, selection of data is inhibited and all the outputs become low in the case of HC157A or high in the case of HC158A.

The SELECT decoding determines whether the A or B inputs get transferred to their corresponding Y ($\overline{Y}$) outputs.

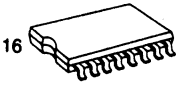
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

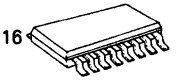
- High Speed ..... t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =4μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL} =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS157/158



DIP16 (3D16A-P)



MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

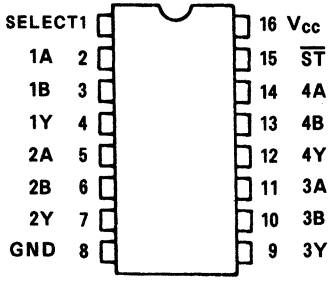
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{\text{ST}}$	SELECT	A	B	Y(157A)	$\overline{Y}$(158A)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care

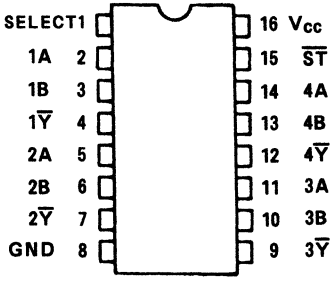
PIN ASSIGNMENT

TC74HC157A



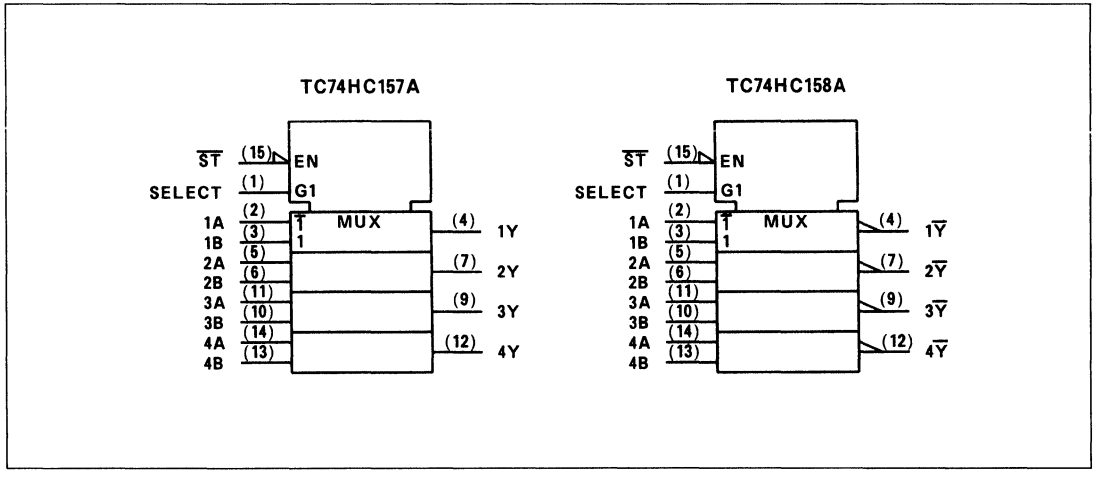
(TOP VIEW)

TC74HC158A



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		–	10	16	
Propagation Delay Time (SELECT–Y)	t_{pLH} t_{pHL}		–	13	21	
Propagation Delay Time ($\overline{STOROBE}$–Y)	t_{pLH} t_{pHL}		–	10	19	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time (SELECT–Y)	t_{pLH} t_{pHL}		2.0	–	50	125	–	155	
			4.5	–	16	25	–	31	
			6.0	–	14	21	–	26	
Propagation Delay Time ($\overline{STOROBE}$–Y)	t_{pLH} t_{pHL}		2.0	–	36	115	–	145	
			4.5	–	12	23	–	29	
			6.0	–	10	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC157A			57	–	–	–	
		TC74HC158A			53	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

TC74HC160AP/AF•TC74HC161AP/AF/AFN
TC74HC162AP/AF•TC74HC163AP/AF/AFN

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

TC74HC160AP/AF	DECADE, ASYNCHRONOUS CLEAR
TC74HC161AP/AF/AFN	BINARY, ASYNCHRONOUS CLEAR
TC74HC162AP/AF	DECADE, SYNCHRONOUS CLEAR
TC74HC163AP/AF/AFN	BINARY, SYNCHRONOUS CLEAR

The TC74HC160A, 161A, 162A and 163A are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent STTL while maintaining the CMOS low power dissipation.

The 74HC160A/162A are BCD decade counters and the TC74HC161A/163A are 4 bit binary counters.

The CLOCK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ inputs are active on low logic level.

Presetting of all four IC's is synchronous to the rising edge of CLOCK.

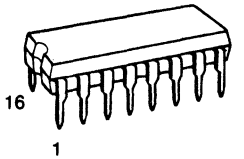
The clear function of the TC74HC162A/163A is synchronous to CLOCK, while the TC74HC160A/161A are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

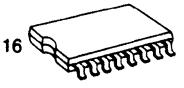
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

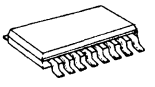
- High Speed ····· f_{MAX}=63MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS160~163



DIP16 (3D16A-P)

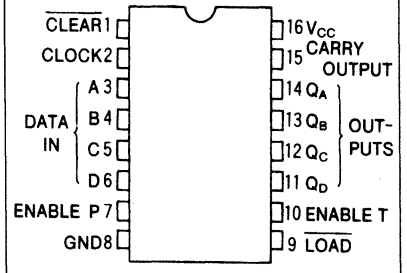


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

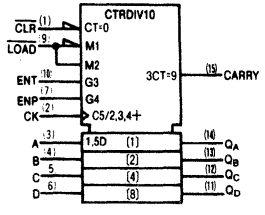
PIN ASSIGNMENT



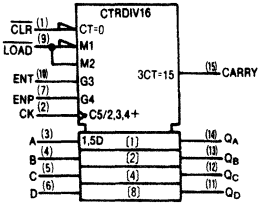
(TOP VIEW)

IEC LOGIC SYMBOL

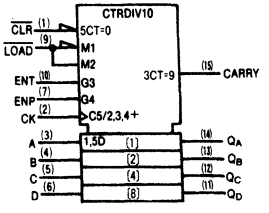
TC74HC160A



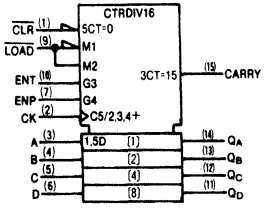
TC74HC161A



TC74HC162A



TC74HC163A



TRUTH TABLE

TC74HC160A/161A INPUTS					TC74HC162A/163A INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↓	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↓	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↓	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↓	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↓	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↑	NO CHANGE				NO COUNT

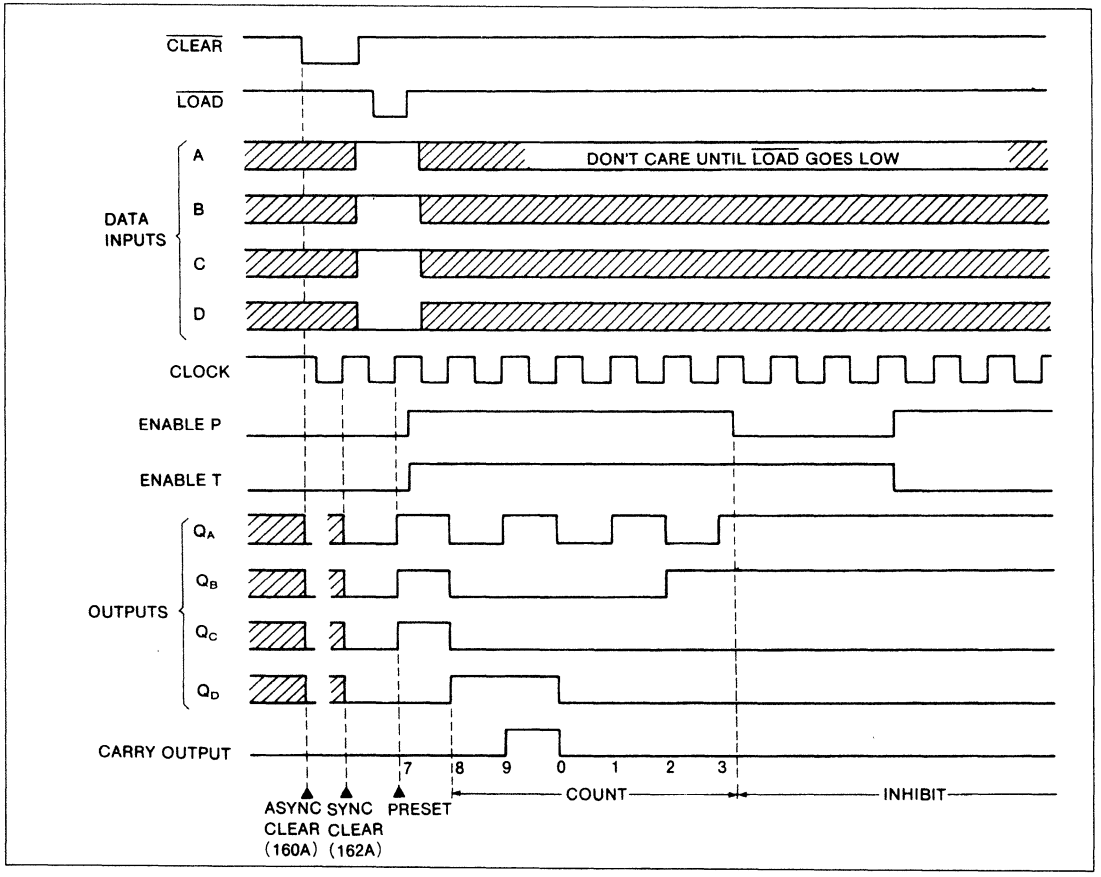
Note X : Don't care

A, B, C, D : Logic Level of Data Inputs

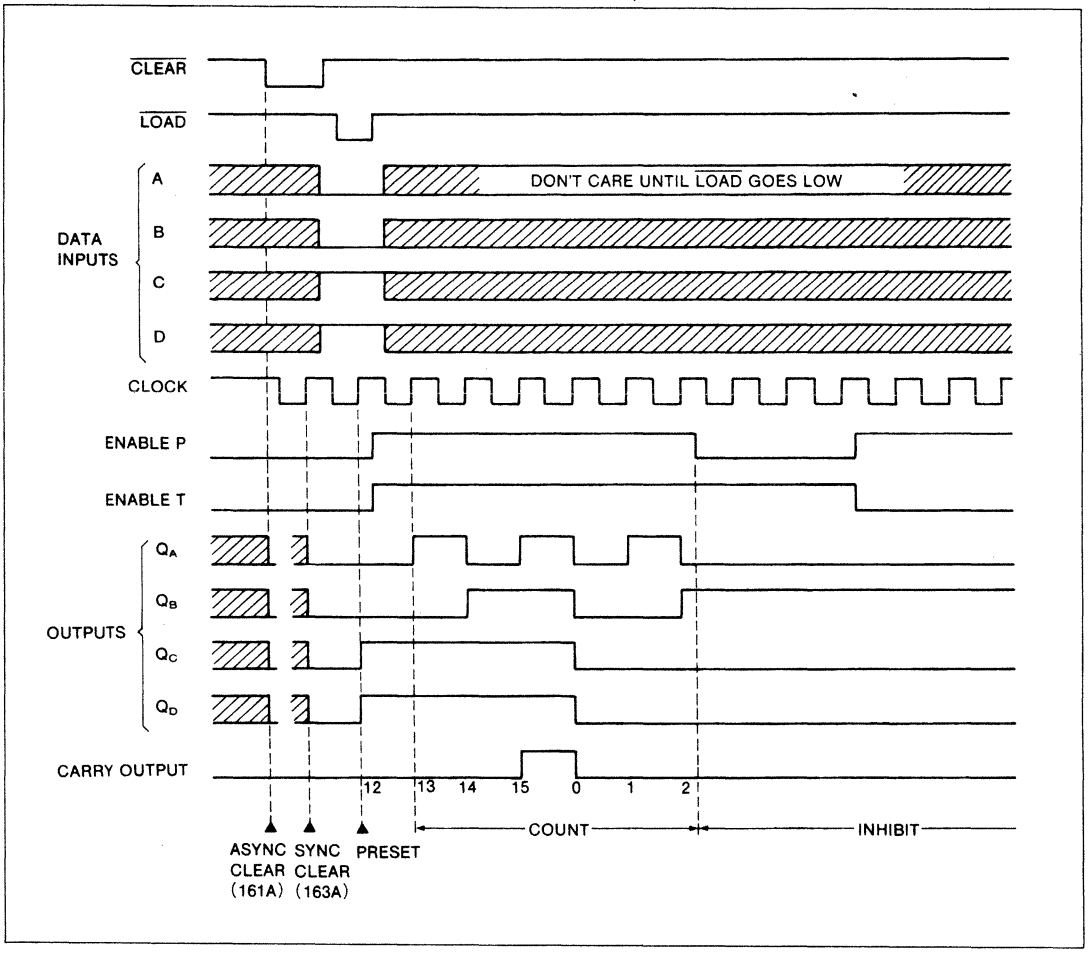
Carry : CARRY=ENT·Q_A·$\overline{Q_B}$·$\overline{Q_C}$·Q_D·····(TC74HC160A/162A)

CARRY=ENT·Q_A·Q_B·Q_C·Q_D·····(TC74HC161A/163A)

TIMING CHART (TC74HC160A/162A:DECADE COUNTER)

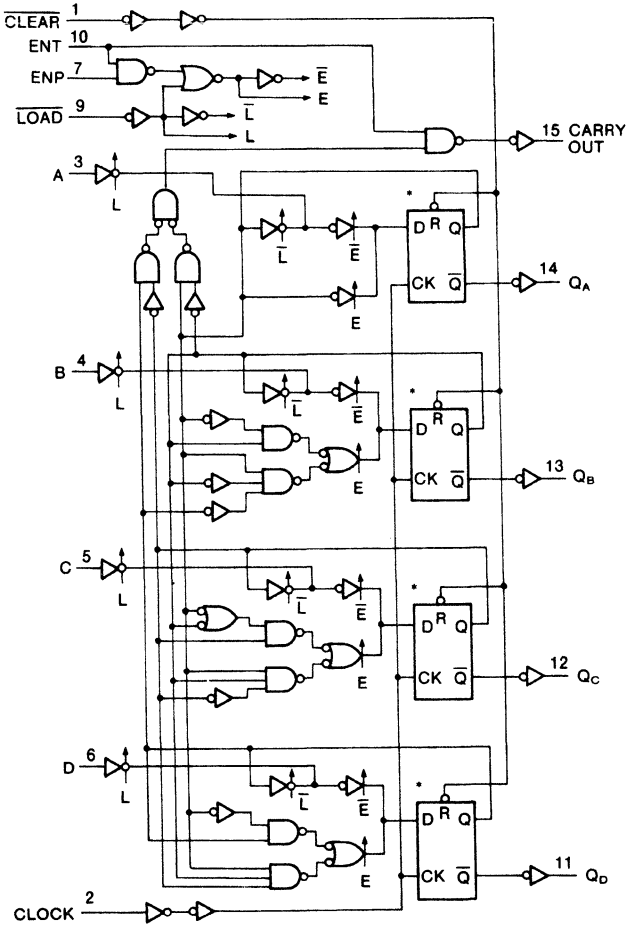


TIMING CHART (TC74HC161A/163A: BINARY COUNTER)



SYSTEM DIAGRAM

TC74HC160A/TC74HC162A



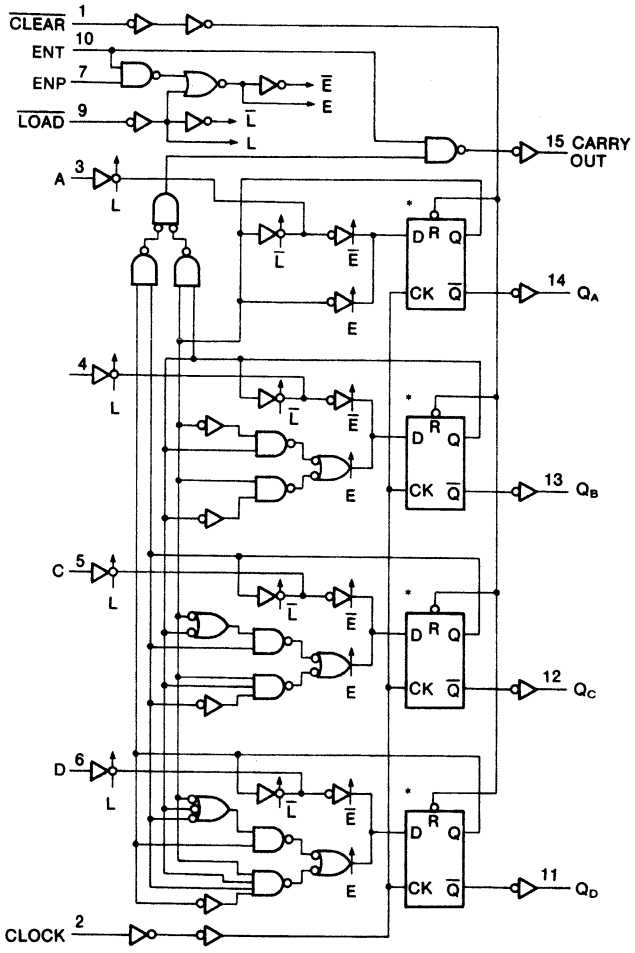
*TRUTH TABLE OF INTERNAL F/F

TC74HC160A					TC74HC162A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↓	L	L	H
L	↓	H	L	H	L	↓	H	L	H
H	↓	H	H	L	H	↓	H	H	L
X	↑	H	NO CHANGE		L	↑	H	NO CHANGE	

X : Don't Care

SYSTEM DIAGRAM

TC74HC161A/TC74HC163A



*TRUTH TABLE OF INTERNAL F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↓	L	L	H
L	↓	H	L	H	L	↓	H	L	H
H	↓	H	H	L	H	↓	H	H	L
X	↑	H	NO CHANGE		L	↑	H	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.7	−	−	1.7	−	V
				4.5	3.6	−	−	3.6	−	
				6.0	4.8	−	−	4.8	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.3	−	0.3	V
				4.5	−	−	0.9	−	0.9	
				6.0	−	−	1.2	−	1.2	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.8	2.0	−	1.8	−	V
				4.5	4.0	4.5	−	4.0	−	
				6.0	5.5	5.9	−	5.5	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.2	−	0.2	V
				4.5	−	0.0	0.5	−	0.5	
				6.0	−	0.1	0.5	−	0.5	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$	Fig. 1	2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)*	$t_{W(L)}$	Fig. 4	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{LOAD}$, ENP, ENT)	t_s	Fig. 2, 3	2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (A, B, C, D)	t_s	Fig. 2	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{CLEAR}$)**	t_s	Fig. 5	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h	Fig. 2, 3, 5	2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)*	t_{rem}	Fig. 4	2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	Fig. 1	−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}	Fig. 1	−	13	21	
Propagation Delay Time (CLOCK−CARRY) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	−	16	26	
Propagation Delay Time (CLOCK−CARRY) [Preset Mode]	t_{pLH}	Fig. 2	−	18	30	
	t_{pHL}		−	20	35	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}	Fig. 6	−	10	17	
Propagation Delay Time ($\overline{CLEAR}$−Q)*	t_{pHL}	Fig. 4	−	17	26	
Propagation Delay Time ($\overline{CLEAR}$−CARRY)*	t_{pHL}	Fig. 4	−	20	35	
Maximum Clock Frequency	f_{MAX}		36	63	−	MHz

* : for TC74HC160A/161A only
** : for TC74HC162A/163A only

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}	Fig. 1	2.0	−	48	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	14	21	−	26	
Propagation Delay Time (CLOCK−CARRY) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	2.0	−	57	150	−	190	
			4.5	−	19	30	−	38	
			6.0	−	16	26	−	33	
Propagation Delay Time (CLOCK−CARRY) [Preset Mode]	t_{pLH}	Fig. 2	2.0	−	66	175	−	220	
			4.5	−	22	35	−	44	
			6.0	−	19	30	−	37	
	t_{pHL}		2.0	−	72	200	−	250	
			4.5	−	24	40	−	50	
			6.0	−	20	34	−	43	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}	Fig. 6	2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}	Fig. 4	2.0	−	60	150	−	190	
			4.5	−	20	30	−	38	
			6.0	−	17	26	−	33	
Propagation Delay Time ($\overline{CLEAR}$−CARRY)	t_{pHL}	Fig. 4	2.0	−	72	200	−	250	
			4.5	−	24	40	−	50	
			6.0	−	20	34	−	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	62	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)	(注 1)		−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:
In case of TC74HC160A/162A:

$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{CO}}{10} \right)$$

In case of TC74HC161A/163A:

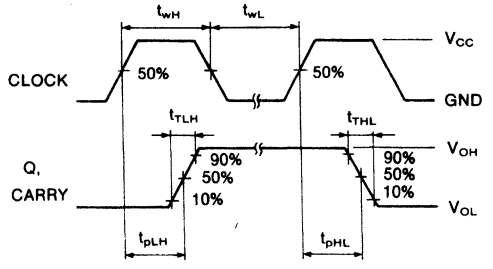
$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C_{QA}～C_{QD} and C_{CO} are the capacitances at QA～QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CLOCK.

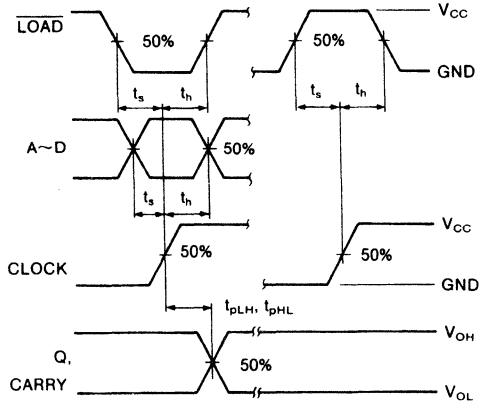
(2) * for TC74HC160A/161A only
* * for TC74HC162A/163A only

SWITCHING CHARACTERISTICS TEST WAVEFORM

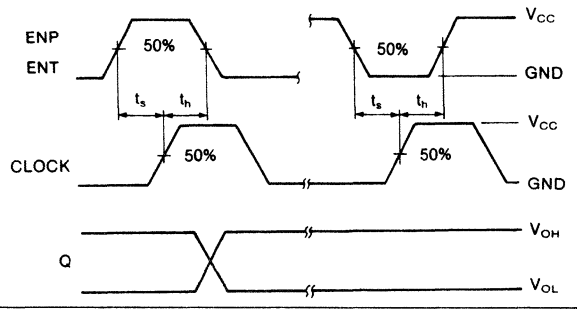
COUNT MODE (Fig. 1)



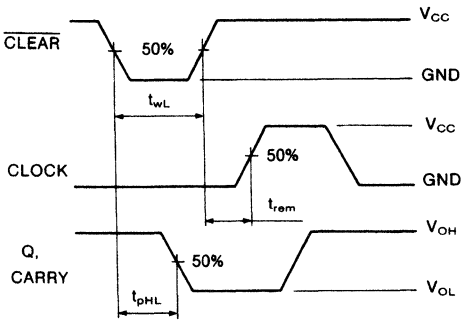
PRESET MODE (Fig. 2)



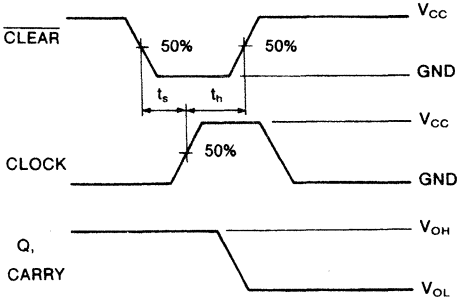
COUNT ENABLE MODE (Fig. 3)



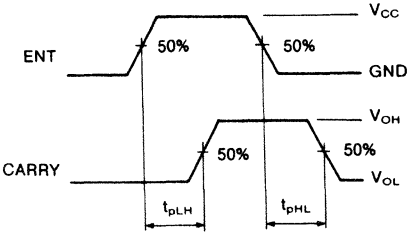
CLEAR MODE (TC74HC160A/161A) (Fig. 4)



CLEAR MODE (TC74HC162A/163A) (Fig. 5)

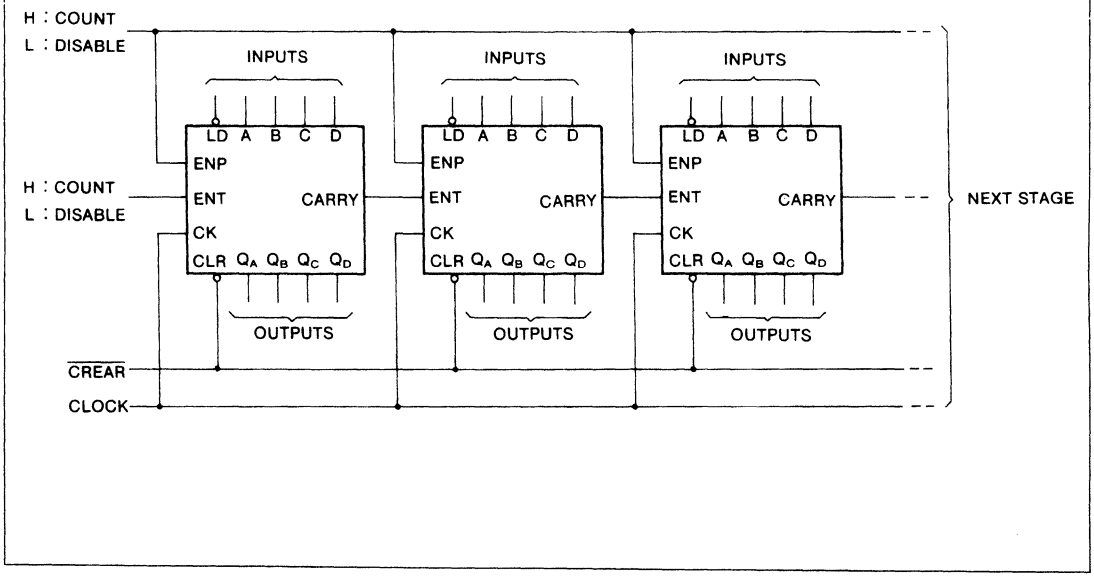


CASCADE MODE (Fix Maximum Count) (Fig. 6)



TYPICAL APPLICATION

PARALLEL CARRY N-BIT COUNTER



TC74HC164AP/AF/AFN

8-BIT SHIFT REGISTER(S-IN, P-OUT)

The TC74HC164A is a high speed CMOS 8-BIT SERIAL -IN PARALLEL-OUT SHIFT REGISTER fablicated with silicon gate C^2MOS technology.

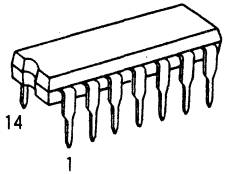
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{CLEAR}$ input. Two serial data inputs (A, B) are provided so that one may be used as a data enable.

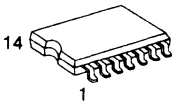
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

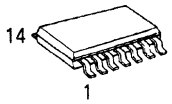
- High Speed ····· f_{MAX}=58MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS164



DIP14 (3 D14A-P)

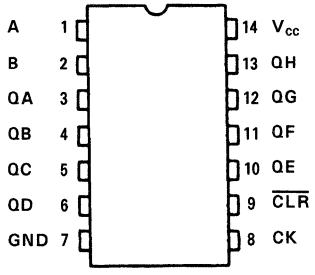


MFP 14
(F14GB-P)



SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

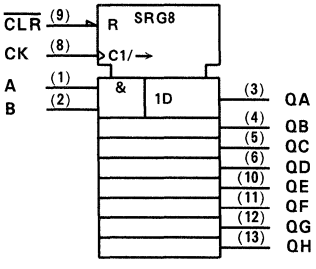
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CK	SERIAL IN		QA	QB	···	QH
		A	B				
L	X	X	X	L	L	···	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	···	QGn
H	↑	X	L	L	QAn	···	QGn
H	↑	H	H	H	QAn	···	QGn

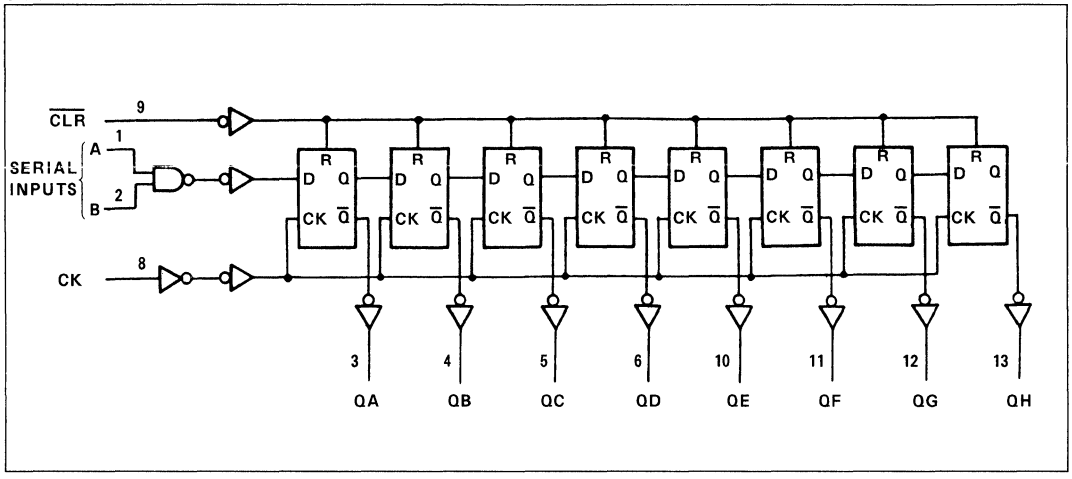
X: Don't Care

QAn~QGn: The level of QA~QG, respectively, before the most recent positive edge of the clock.

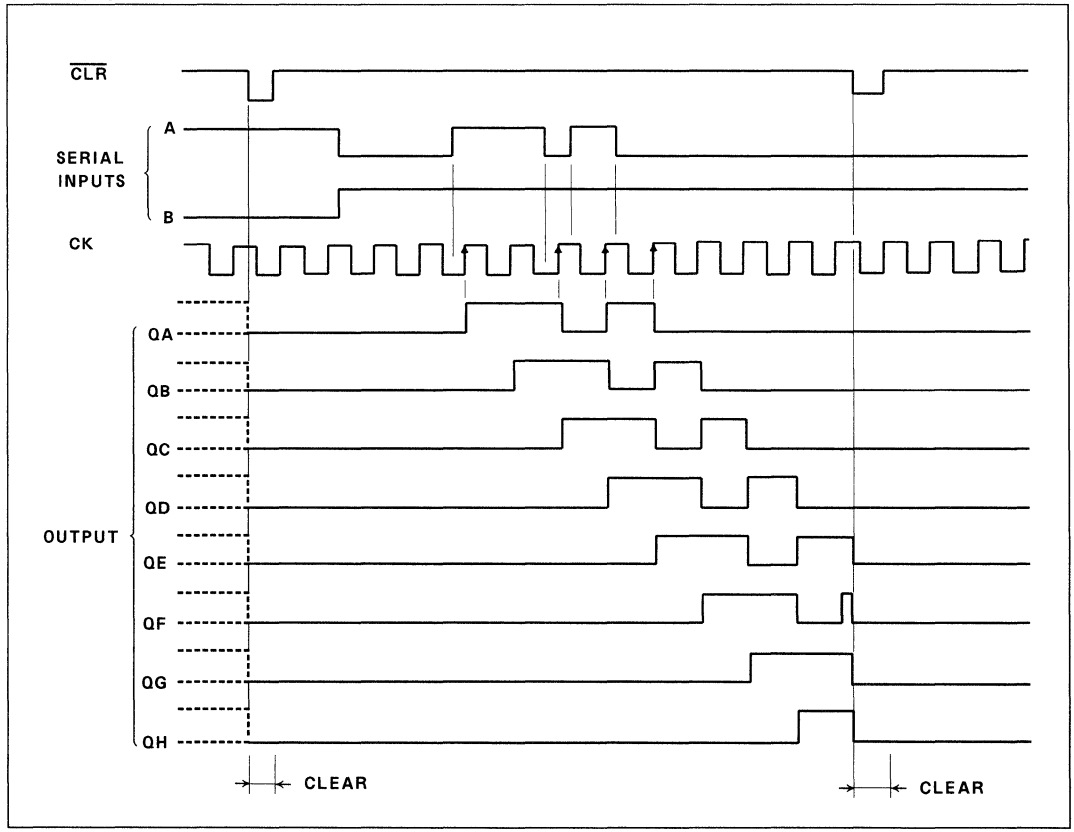
IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	80	100	
			4.5	−	16	20	
			6.0	−	14	17	
Minimum Set−up Time (A, B)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Qn)	t_{pLH} t_{pHL}		−	15	27	
Propagation Delay Time ($\overline{CLEAR}$−Qn)	t_{pHL}		−	16	30	
Maximum Clock Frequency	f_{MAX}		33	58	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Qn)	t_{pLH} t_{pHL}		2.0	−	57	160	−	200	
			4.5	−	19	32	−	40	
			6.0	−	16	27	−	34	
Propagation Delay Time ($\overline{CLEAR}$−Qn)	t_{pHL}		2.0	−	60	175	−	220	
			4.5	−	20	35	−	44	
			6.0	−	17	30	−	37	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	62	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	107	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TC74HC165AP/AF/AFN

8-BIT SHIFT REGISTER (P-IN,S-OUT)

The TC74HC165A is a high speed CMOS 8-BIT PARALLEL/ SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock inputs. When the SHIFT/$\overline{\text{LOAD}}$ input is held high,the serial data input is enabled and the eight frip-frops perform serial shifting with each clock pulse.

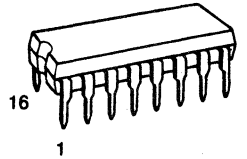
When the SHIFT/$\overline{\text{LOAD}}$ input is held low, the parallel data is loaded asynchronously into the register at positive going transition of the clock pulse.

The CLOCK-INHIBIT input should be shifted high only when the CLOCK input is held high.

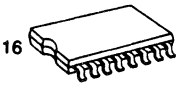
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

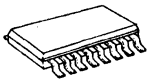
- High Speed ..... f_{MAX}=56MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS165



DIP16 (3D16A-P)

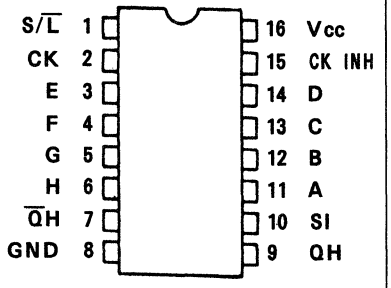


MFP 16
(F16GC-P)



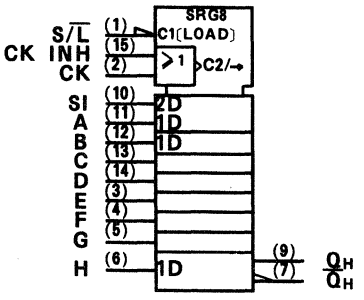
SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

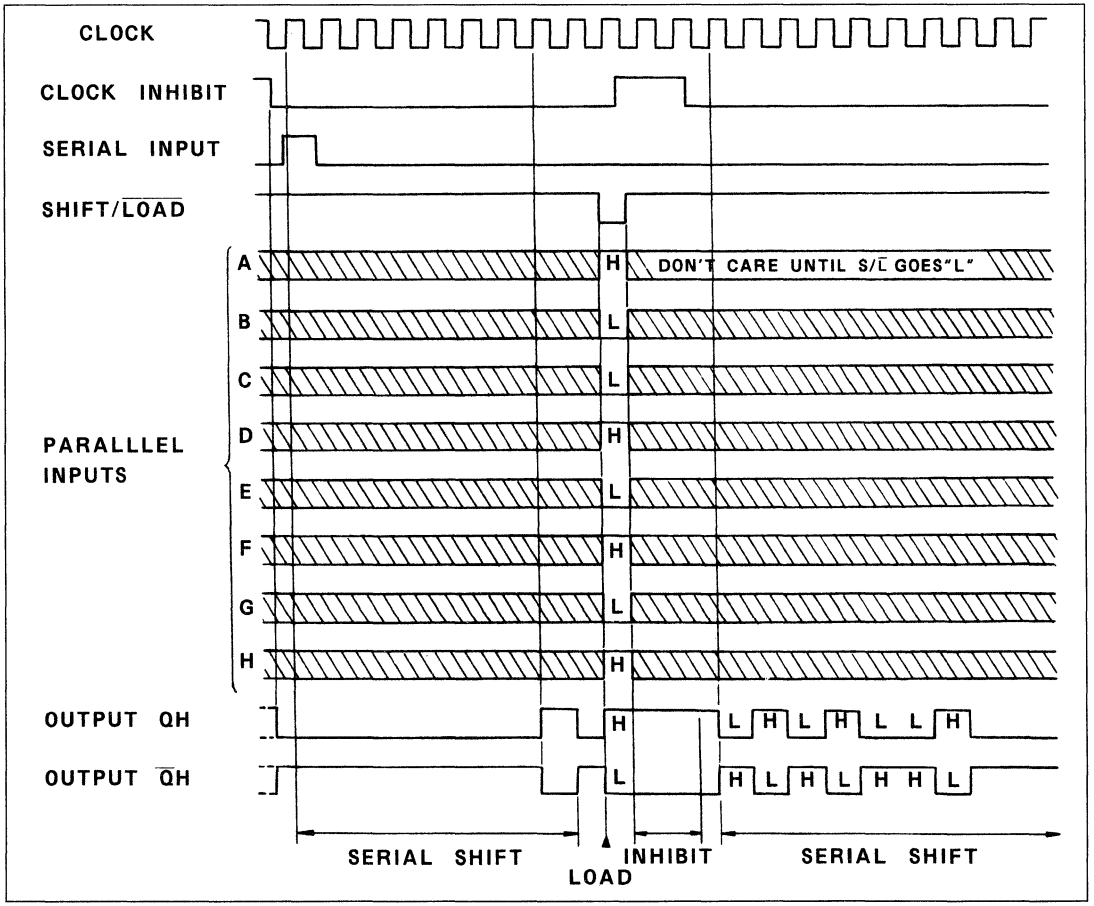


TRUTH TABLE

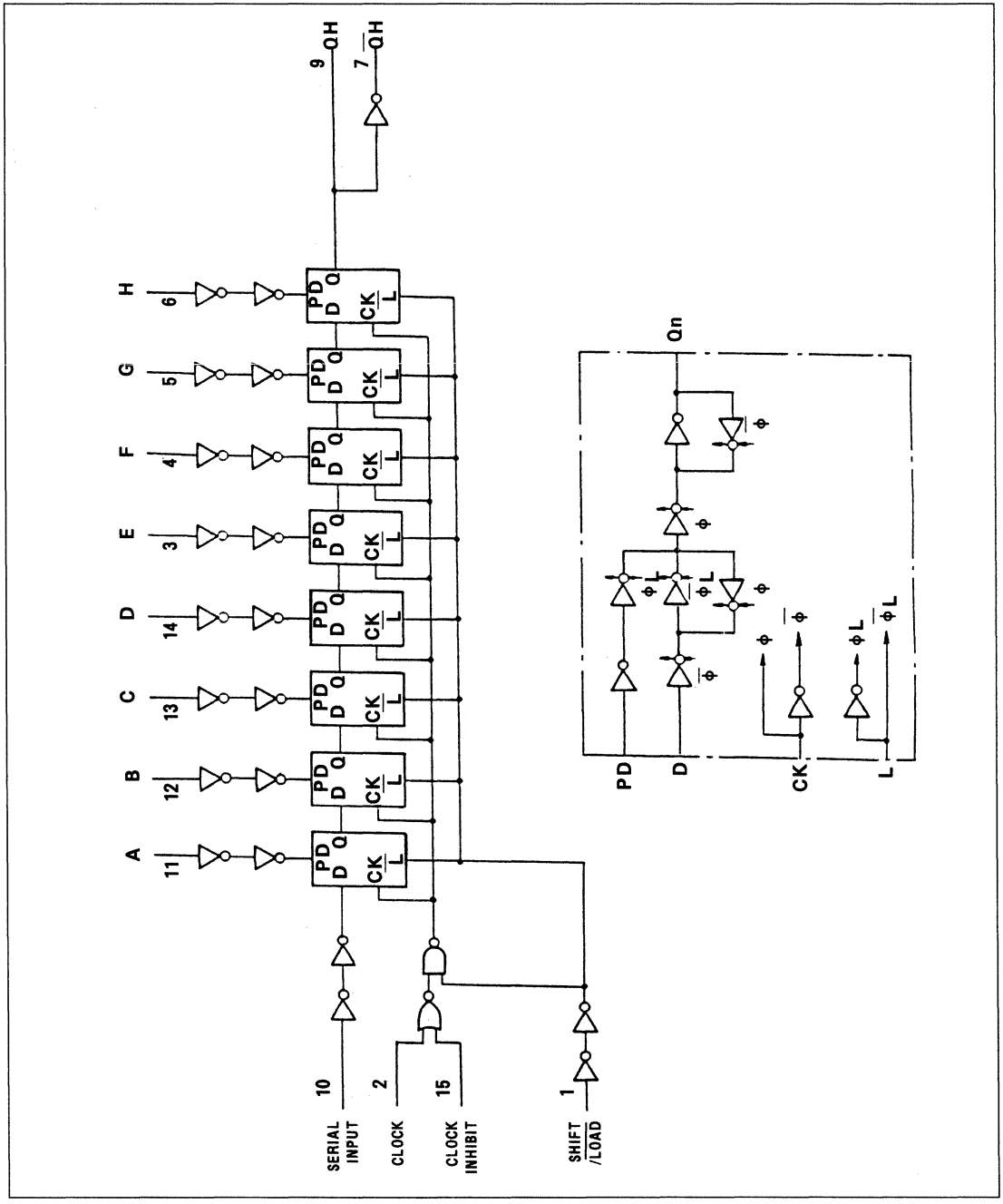
INPUTS					INTERNAL OUTPUTS		OUTPUTS	
SHIFT/$\overline{\text{LOAD}}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A……H	QA	QB	QH	$\overline{\text{QH}}$
L	X	X	X	a …… h	a	b	h	$\overline{\text{h}}$
H	L	↑	H	X	H	QAn	QGn	$\overline{\text{QGn}}$
H	L	↑	L	X	L	QAn	QGn	$\overline{\text{QGn}}$
H	↑	L	H	X	H	QAn	QGn	$\overline{\text{QGn}}$
H	↑	L	L	X	L	QAn	QGn	$\overline{\text{QGn}}$
H	X	H	X	X	No change			
H	H	X	X	X	No change			

X:Don't Care
a……h :The level of steady input voltage at inputs A through H respectively.
QAn~QGn:The level of QA~QG,respectively,before the most recent positive transition of the CLOCK.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied untii 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING RECOMMENDED OPERATING CONDITIONS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK, CK INH)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (S/$\overline{L}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (PI−S/$\overline{L}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI−CK,CK INH)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (S/$\overline{L}$−CK,CK $\overline{INH}$)	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (PI−S/$\overline{L}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (SI−CK,CK INH)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (S/$\overline{L}$−CK,CK INH)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time (CK INH−CK) (CK−CK INH)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	30	24	
			6.0	−	41	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CK,CK INH−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time (S/$\overline{L}$−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time (H−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	14	26	
Maximum Clock Frequency	f_{MAX}		35	56	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CK,CK INH−QH,$\overline{Q}$H)	t_{pLH} t_{pHL}		2.0	−	55	150	−	190	
			4.5	−	18	30	−	38	
			6.0	−	15	26	−	33	
Propagation Delay Time (S/$\overline{L}$−QH,$\overline{Q}$H)	t_{pLH} t_{pHL}		2.0	−	60	165	−	205	
			4.5	−	19	33	−	41	
			6.0	−	16	28	−	35	
Propagation Delay Time (H−QH,$\overline{Q}$H)	t_{pHL}		2.0	−	52	135	−	170	
			4.5	−	17	27	−	34	
			6.0	−	14	23	−	29	
Maximum Clock Frequency	f_{MAX}		2.0	7	14	−	6	−	MHz
			4.5	30	46	−	24	−	
			6.0	41	65	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	55	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC166AP/AF/AFN

8-BIT SHIFT REGISTER (P-IN,S-OUT)

The TC74HC166A is a high speed CMOS 8 BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with sillicon gate C^2MOS technology.

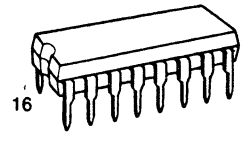
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, includng the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing chrts.

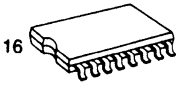
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

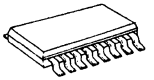
- High Speed ····· f_{MAX}=57MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS166



DIP16 (3D16A-P)

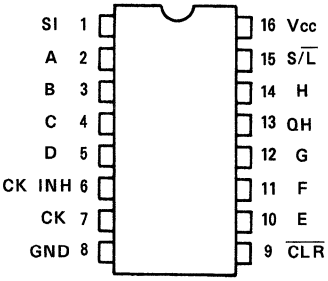


MFP 16
(F16GC-P)



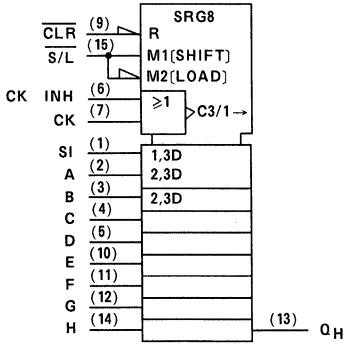
SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



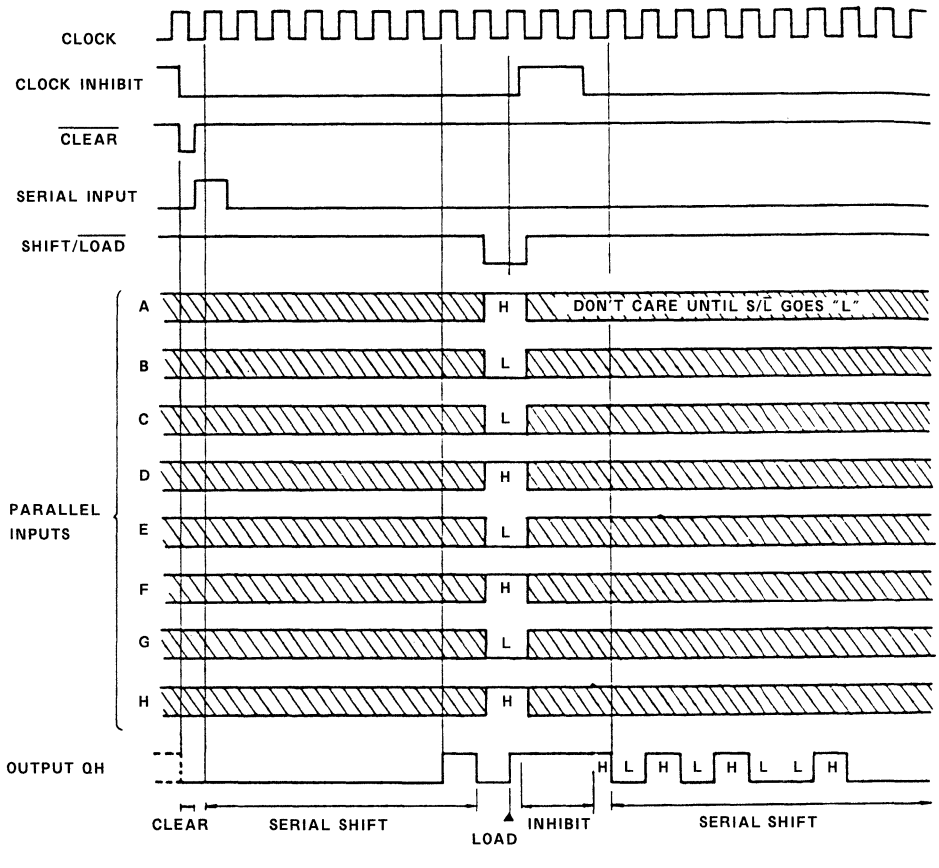
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
$\overline{\text{CLEAR}}$	SHIFT/$\overline{\text{LOAD}}$	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A ····· H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↑	X	X	No change	
H	L	L	↓	X	a ····· h	a b	h
H	H	L	↓	H	X	H QAn	QGn
H	H	L	↓	L	X	L QAn	QGn
H	X	H	X	X	X	No change	

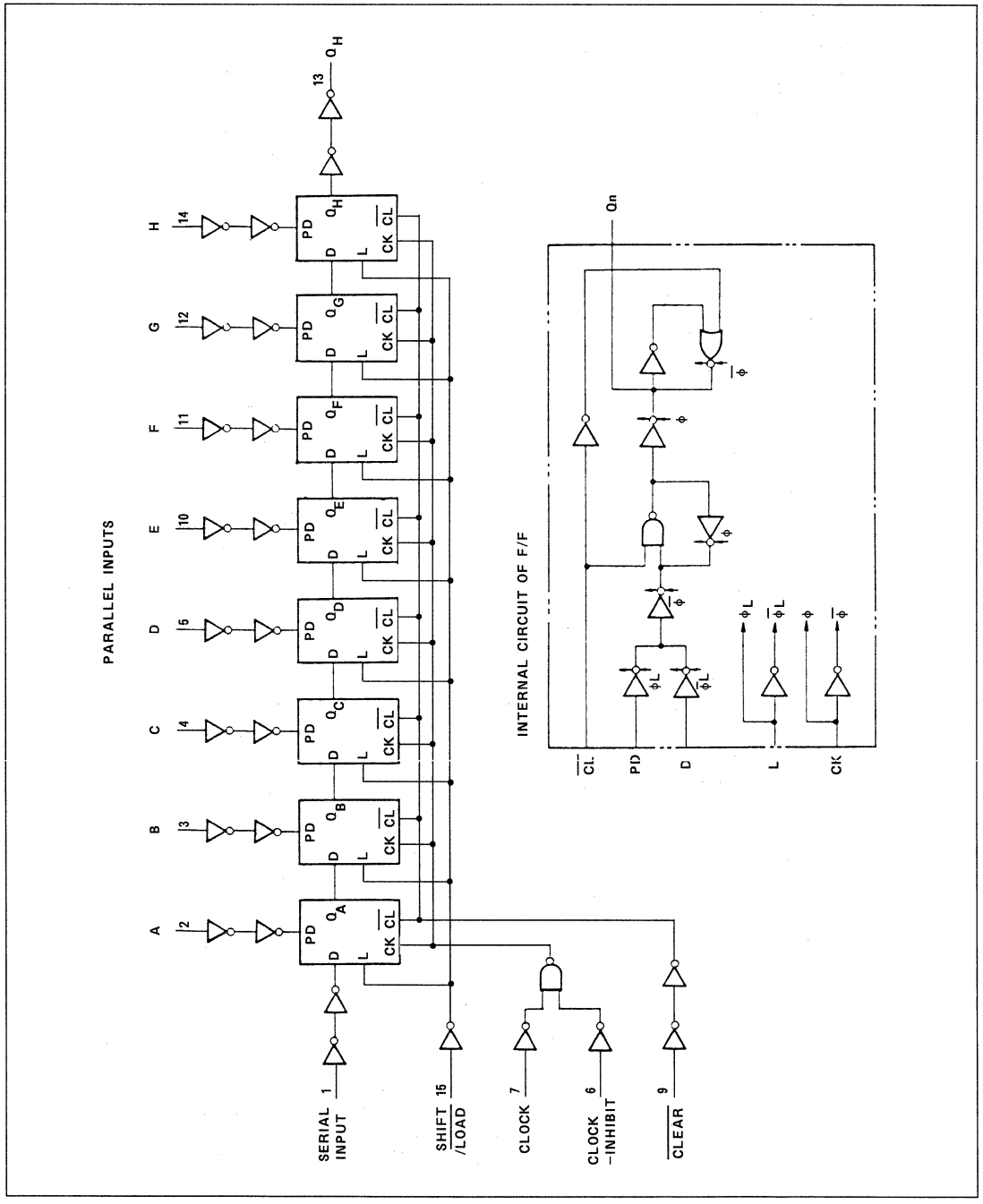
X : Don't care

a ····· h : The level of steady state input voltage at inputs A through H respectively

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI,PI)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (S/$\overline{L}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (SI,PI)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (S/L)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−QH)	t_{pLH} t_{pHL}		−	16	26	
Propagation Delay Time ($\overline{CLEAR}$−QH)	t_{pHL}		−	15	24	
Maximum Clock Frequency	f_{MAX}		33	57	−	MHz

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−QH)	t_{pLH} t_{pHL}		2.0	−	70	150	−	190	
			4.5	−	20	30	−	38	
			6.0	−	16	26	−	32	
Propagation Delay Time ($\overline{CLEAR}$−QH)	t_{pHL}		2.0	−	60	135	−	170	
			4.5	−	18	27	−	34	
			6.0	−	14	23	−	29	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	−	5	−	MHz
			4.5	31	50	−	25	−	
			6.0	36	63	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	60	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

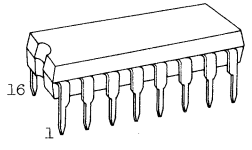
TC74HC173P/F

TC74HC173P/F QUAD D-TYPE REGISTER (3-STATE)

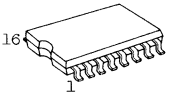
The TC74HC173 is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device is composed of four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs ($D_1 - D_4$) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low. The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, and otherwise the outputs are in a high-impedance state. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS173



DIP16(3D16A-P)



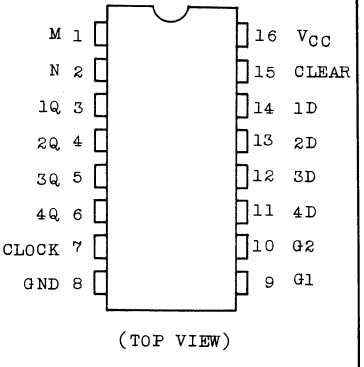
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

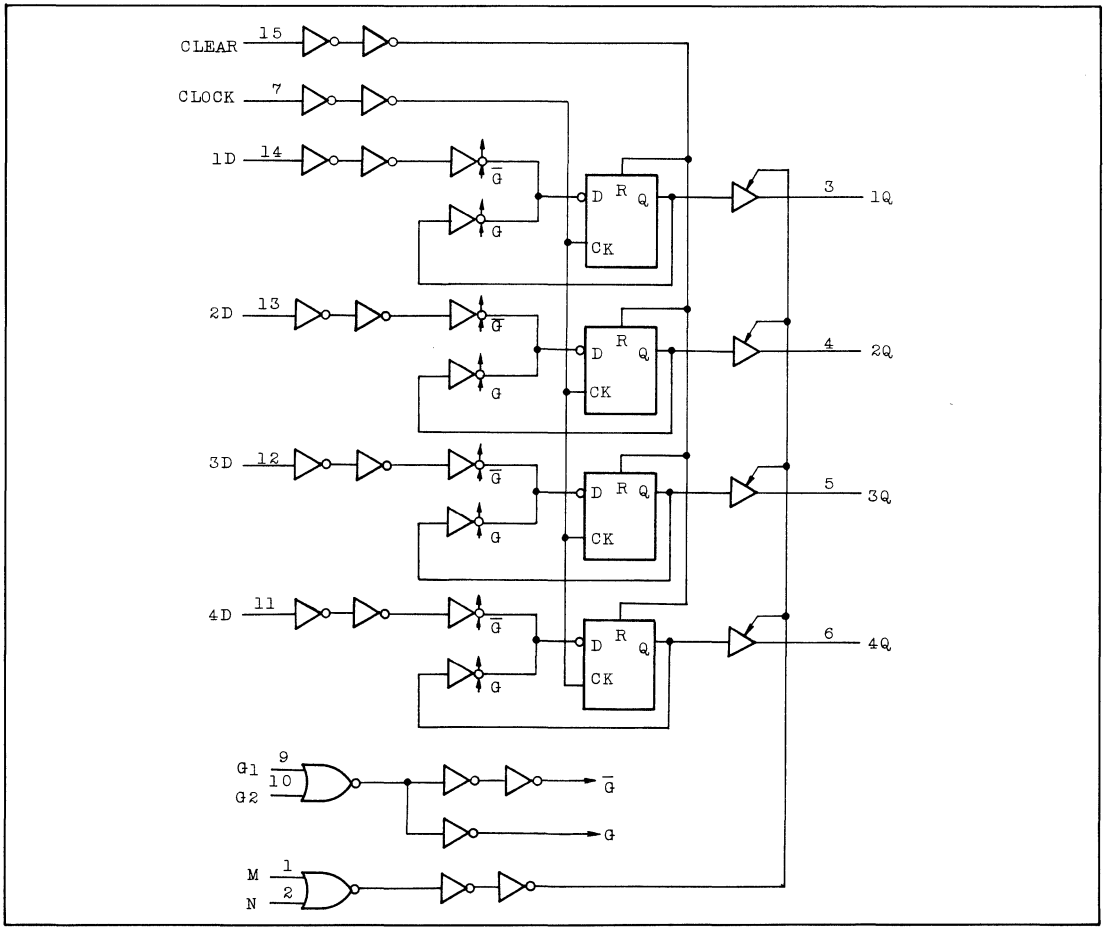
TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	Dn	OUTPUT CONTROL M	OUTPUT CONTROL N	Qn
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↓	X	X	X	L	L	Q0
L	↑	H	X	X	L	L	Q0
L	↑	X	H	X	L	L	Q0
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L

X : DON'T CARE

Z : HIGH IMPEDANCE

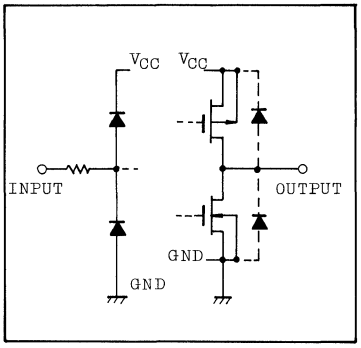
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CLOCK - Q)	t_{PLH} t_{PHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (CLEAR - Q)	t_{PLH} t_{PHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time (G_1, G_2)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time (D)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6 0	-	7	13	-	16	
Minimum Hold Time (G_1, G_2, D)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

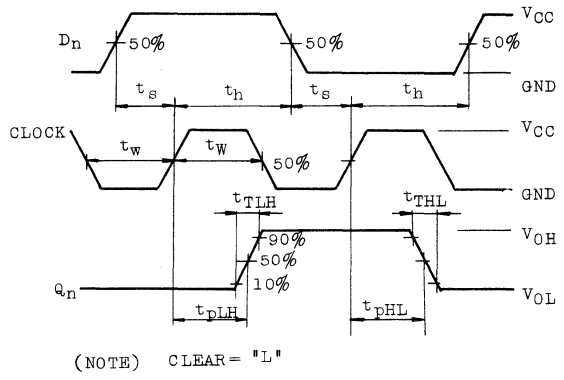
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per 1 Circuit)}$$

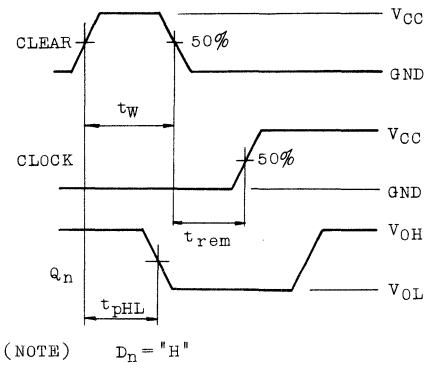
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD(total)}=14+16 \cdot n$$

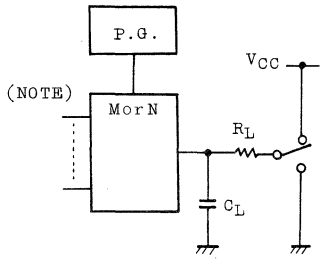
SWITCHING CHARACTERISTICS TEST WAVEFORM



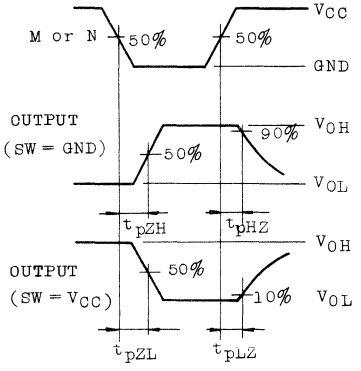
(NOTE) CLEAR = "L"



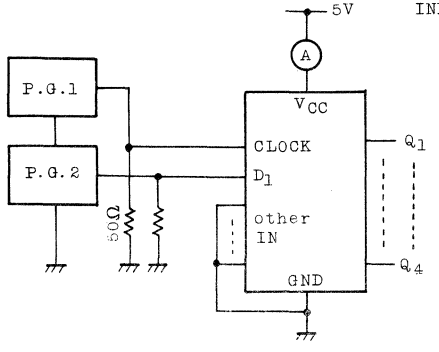
(NOTE) D_n = "H"



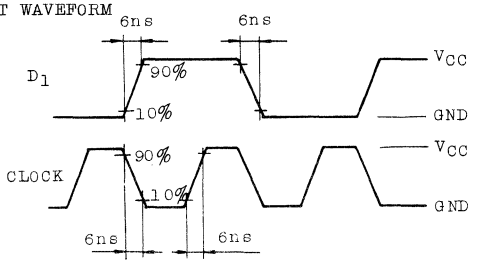
(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM



HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74HC174A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

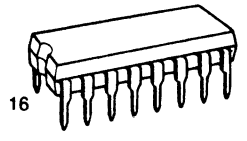
Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.

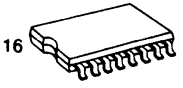
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

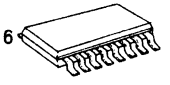
- High Speed ..... f_{MAX}=71MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS174



DIP16 (3D16A-P)

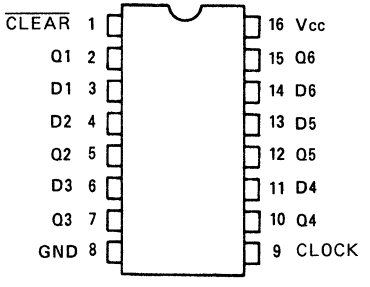


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



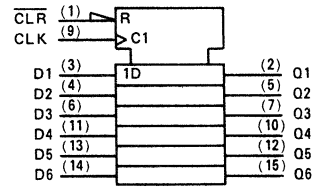
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L	⌐	L	–
H	H	⌐	H	–
H	X	⌙	Qn	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	
Clock Frequency	f		2.0	−	6	4	MHz
			4.5	−	33	26	
			6.0	−	38	30	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	14	26	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		−	15	26	
Maximum Clock Frequency	f_{MAX}		39	71	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	27	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	68	150	−	190	
			4.5	−	17	30	−	38	
			6.0	−	14	26	−	32	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		2.0	−	72	150	−	190	
			4.5	−	18	30	−	38	
			6.0	−	15	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	−	4	−	MHz
			4.5	33	59	−	26	−	
			6.0	38	71	−	30	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	40	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

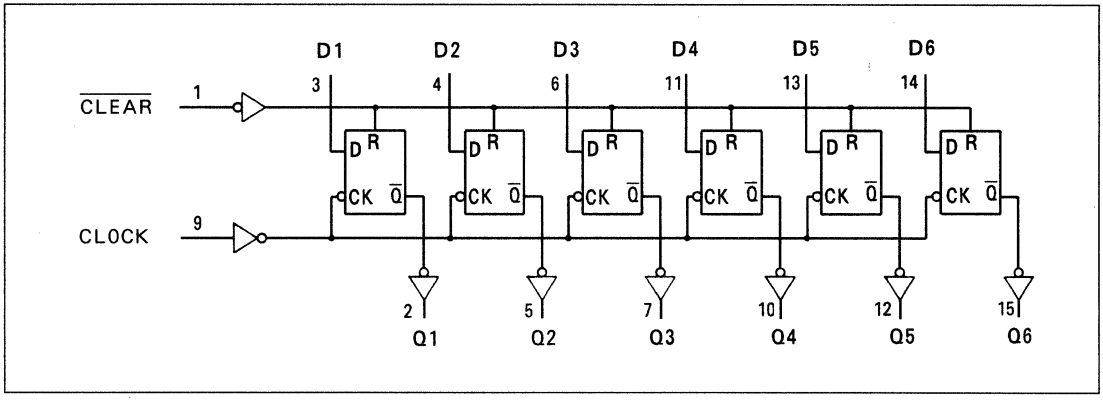
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=28+12 \cdot n$$

SYSTEM DIAGRAM



TC74HC175AP/AF/AFN

QUAD D-TYPE FLIP FLOP WITH CLEAR

The TC74HC175A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

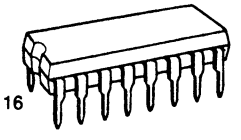
Information signals applied to D inputs are transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q outputs are at the low logic level and the $\overline{Q}$ outputs are at the high logic level independent of the other inputs.

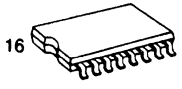
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

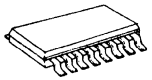
- High Speed ..... f_{MAX}=63MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS175



DIP16 (3D16A-P)

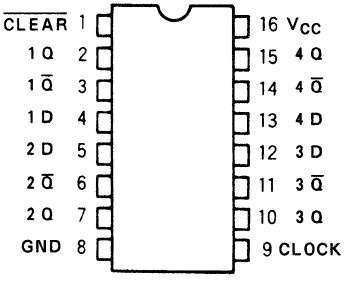


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



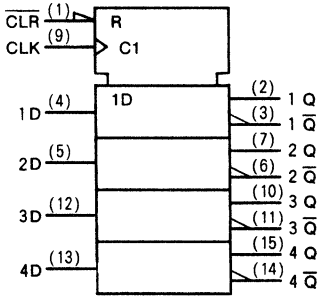
(TOP VIEW)

TRUTH TABLE

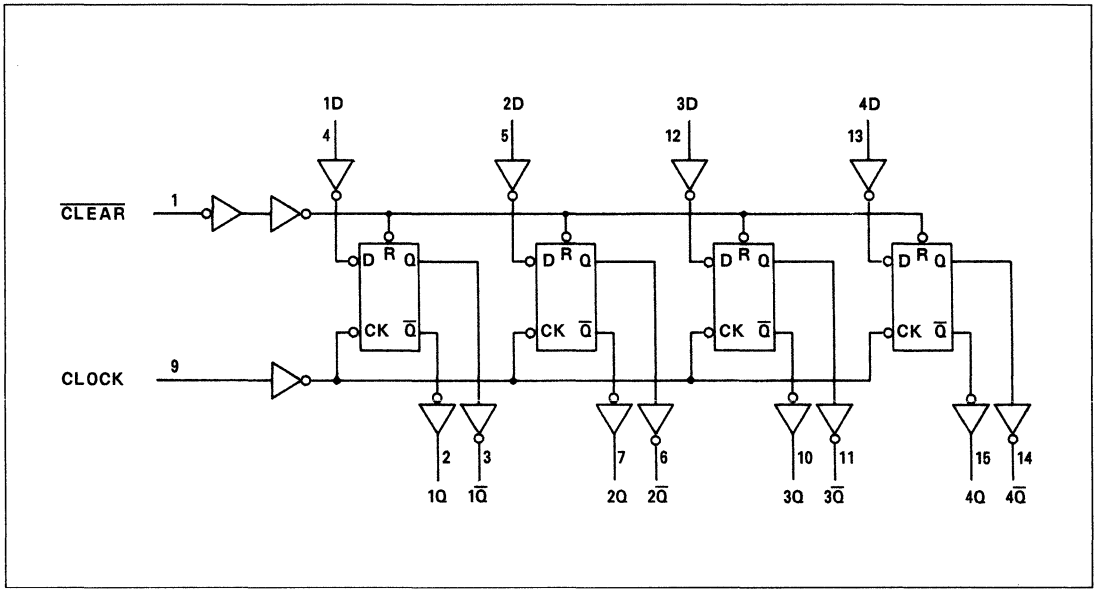
INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	Clear
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Q_n	$\overline{Q}_n$	No change

X : Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	16	24	
Propagation Delay Time ($\overline{CLEAR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	13	21	
Maximum Clock Frequency	f_{MAX}		36	63	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	70	140	−	175	
			4.5	−	19	28	−	35	
			6.0	−	16	24	−	30	
Propagation Delay Time ($\overline{CLEAR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	125	−	160	
			4.5	−	16	25	−	32	
			6.0	−	12	22	−	27	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	63	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	53	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=32+21 \cdot n$$

TC74HC181P ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The TC74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT(ALU)/FUNCTION GENERATORS fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This circuit perform 16 binary arithmetic operations on two 4-bit word as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

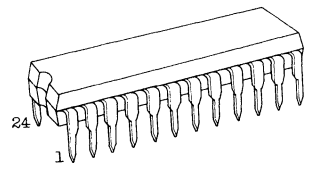
When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look ahead scheme is made available in these devices for fast, simultaneous carry generation be means of two cascade-outputs (pins 15 and 17) for the four bits in the package.

When used in conjunction with the TC74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

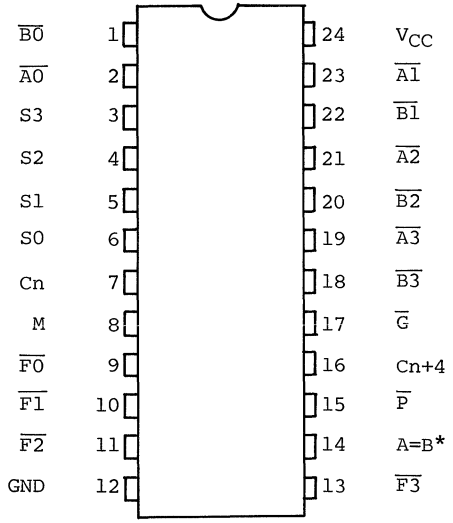
FEATURES:

- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS181



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

*: Open drain Output Structure

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A=B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

FUNCTIONAL DESCRIPTION

The HC181 will accomodate active-high or active-low data, if the pin designations are interpreted as show below.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn+4	$\overline{P}$	$\overline{G}$
Active-high data(Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{Cn}$	$\overline{Cn+4}$	X	Y

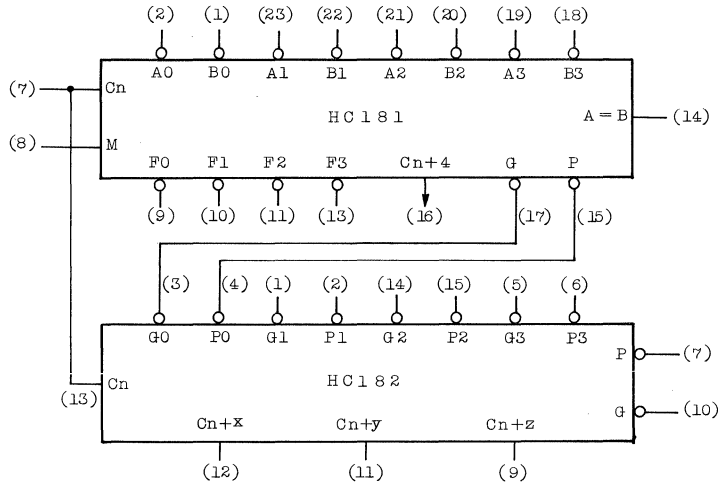
Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to produce A-B.

The HC181 also be utilized as a comparator. The A=B output is internally decoder from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with Cn=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output Cn+4	Active-low data (Figure 1)	Active-high data (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

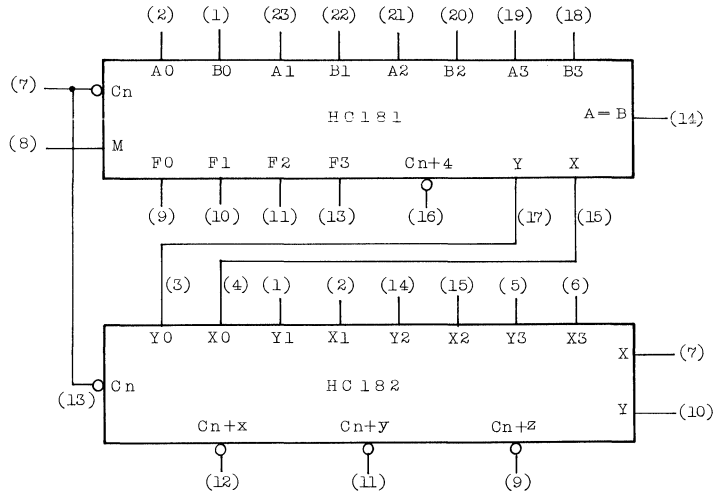


(Figure 1)

Table 1

Selection				Active Low Data		
				M=H	M=L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ Minus 1	F = ($A\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus(A + $\overline{B}$) Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Puls (A + B)	F = AB Plus(A + $\overline{B}$) Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus(A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\overline{B}$ Plus (A + B)	F = $A\overline{B}$ Plus(A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\overline{B}$ Plus A	F = $A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.



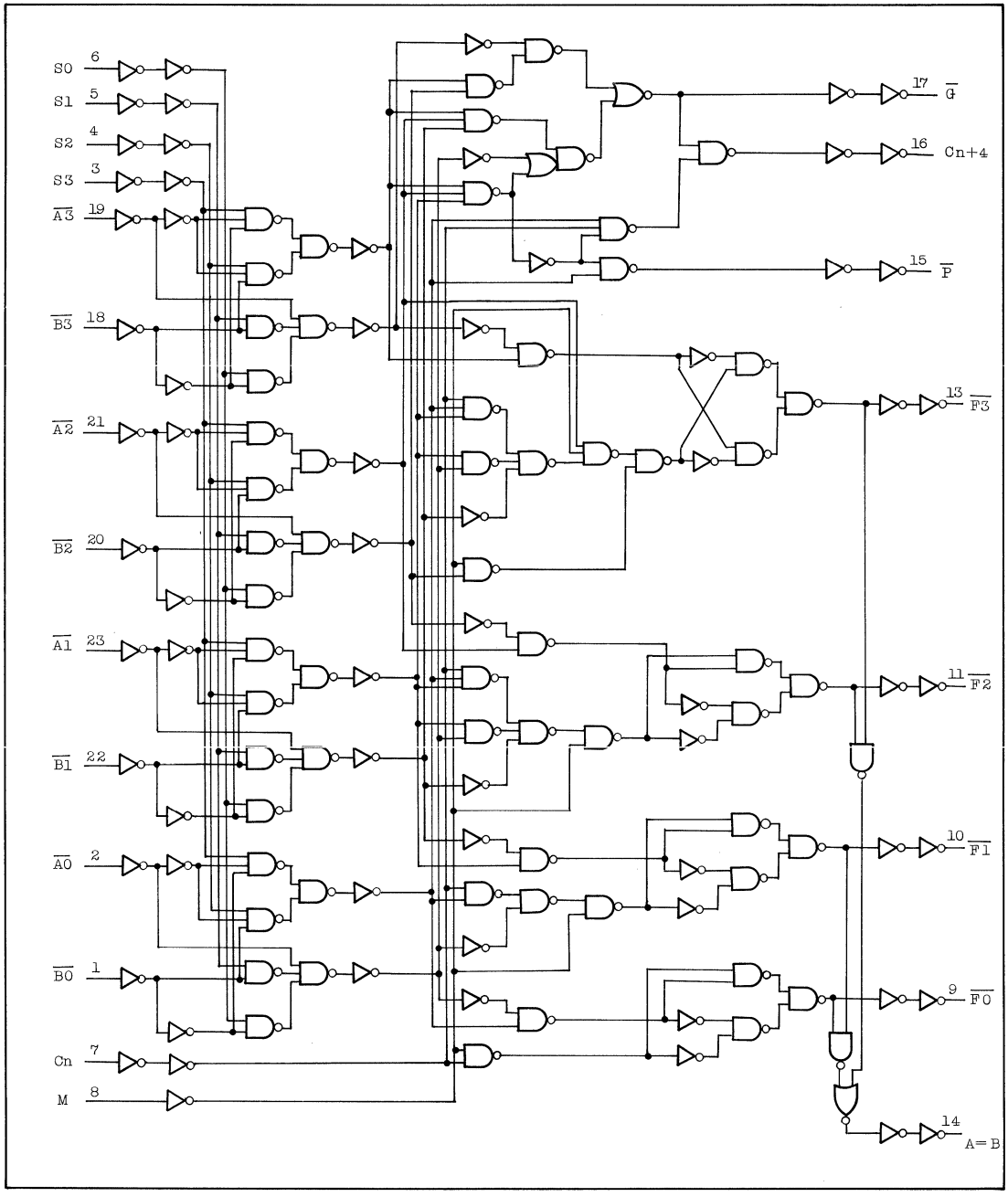
(Figure 2)

Table 2

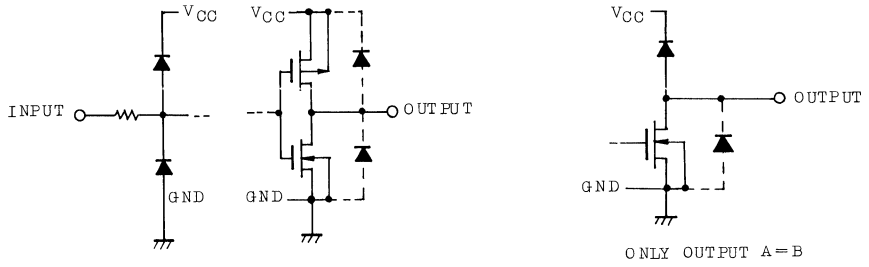
Selection S3	S2	S1	S0	Active High Data: M=H Logic Functions	M=L: Arithmetic Operations: C_n=H (no carry)	M=L: Arithmetic Operations: C_n=L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A+B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1(2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Any output except A=B	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.00	0.1	-	0.1	V
				4.5	-	0.00	0.1	-	0.1	
				6.0	-	0.00	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	$V_{IN}=V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (1)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time (2)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (3)	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (4)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
Propagation Delay Time (5)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (6)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Propagation Delay Time (7)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (8)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (9)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (10)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (11)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
3-State Output Enable Time (12)	t_{pZL}	R_L=1kΩ	2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
3-State Output Disable Time (12)	t_{pLZ}	R_L=1kΩ	2.0	-	140	260	-	325	
			4.5	-	35	52	-	65	
			6.0	-	30	44	-	55	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	216	-	-	-	

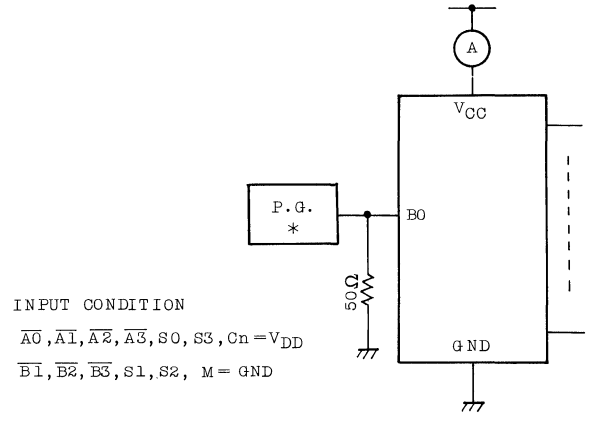
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

PROPAGATION DELAY TIME TEST CONDITIONS

TEST NO.	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M=GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A=B	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)

$I_{CC(opr.)}$ TEST CIRCUIT



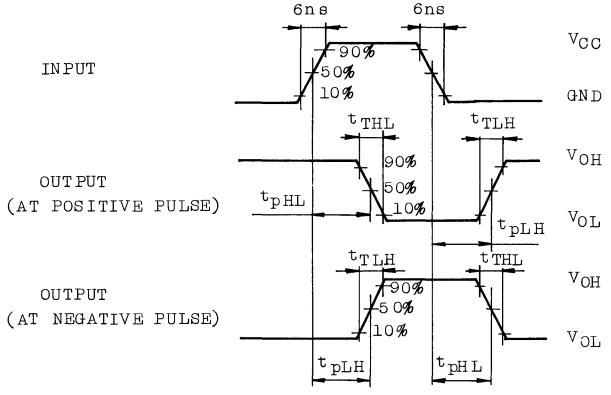
INPUT CONDITION

$\overline{A0}, \overline{A1}, \overline{A2}, \overline{A3}, S0, S3, Cn = V_{DD}$

$\overline{B1}, \overline{B2}, \overline{B3}, S1, S2, M = GND$

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC182P/F

TC74HC182P/F LOOK AHEAD CARRY LOGIC

The TC74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated with silicon gate C^2MOS technology.

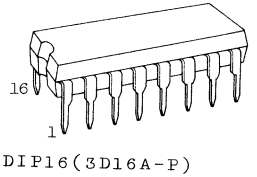
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

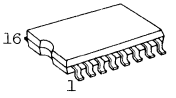
When used in conjunction with the HC181 arithmetic logic unit, these generators provide hihg-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate(P) and carry generate(G) are in negated form; therefore, the carry functions (inputs, output, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

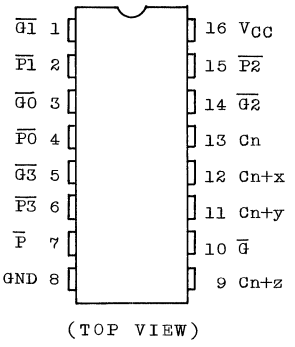


MFP16(F16GC-P)

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS182

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
All other combinations			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

X: Don't care

$Cn+x=G0 + P0Cn$

$Cn+y=G1 + P1G0 + P1P0Cn$

$Cn+z=G2 + P2G1 + P2P1G0 + P2P1P0Cn$

$\overline{G}=\overline{G3+P3G2+P3P2G1+P3P2P1G0}$

$\overline{P}=\overline{P3P2P1P0}$

or

$\overline{Cn+x}=\overline{Y0(X0+Cn)}$

$\overline{Cn+y}=\overline{Y1[X1+Y0(X0+Cn)]}$

$\overline{Cn+z}=\overline{Y2\{X2+Y1[X1+Y0(X0+Cn)]\}}$

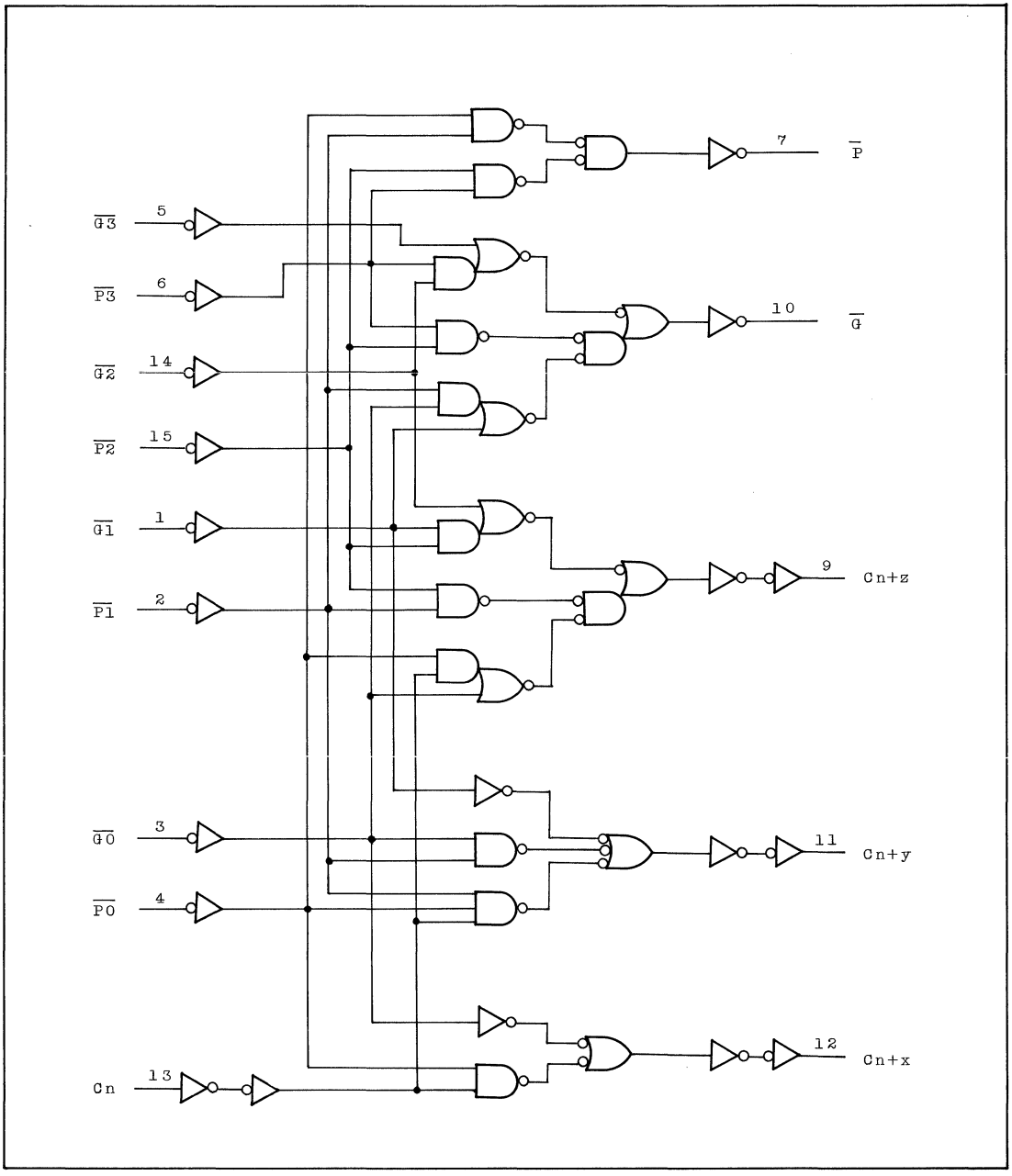
$Y=Y3(X3+Y2)(X3+X2+Y1)(X3+X2+X1+Y0)$

$X=X3+X2+X1+X0$

Pin Designation

Active "L"	Active "H"	Pin No.	Function
$\overline{G0},\overline{G1},\overline{G2},\overline{G3}$	G0,G1,G2,G3	3,1,14,5	Carry Generate Inputs
$\overline{P0},\overline{P1},\overline{P2},\overline{P3}$	P0,P1,P2,P3	4,2,15,6	Carry Propagate Inputs
Cn	$\overline{Cn}$	13	Carry Input
Cn+z, Cn+y Cn+z	$\overline{Cn+x}$, $\overline{Cn+y}$ $\overline{Cn+z}$	12,11,9	Carry Outputs
$\overline{G}$	Y	10	Carry Generate Output
$\overline{P}$	X	7	Carry Propagate Output
VCC		16	Supply Voltage
GND		8	Ground

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

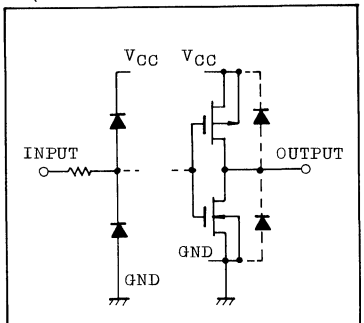
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

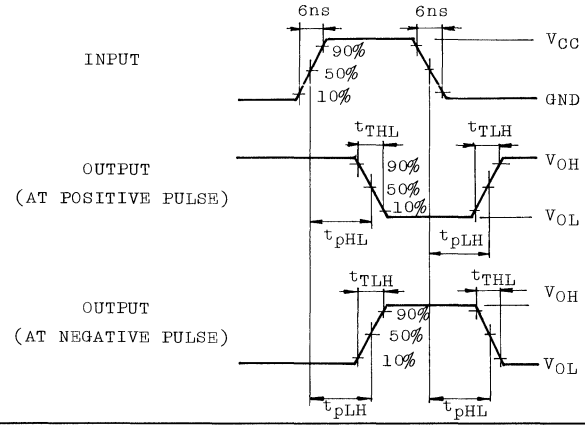
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$ - Cn+x, Cn+y / $\overline{P0},\overline{P1},\overline{P2}$ - Cn+z)	t_{pLH}		2.0	-	72	145	-	180	
	t_{pHL}		4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$ - $\overline{G}$ / $\overline{P1},\overline{P2},\overline{P3}$)	t_{pLH}		2.0	-	84	165	-	205	
	t_{pHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)	t_{pLH}		2.0	-	80	155	-	195	
	t_{pHL}		4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time (Cn - Cn+x, Cn+y, Cn+z)	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	88	-	-	-	

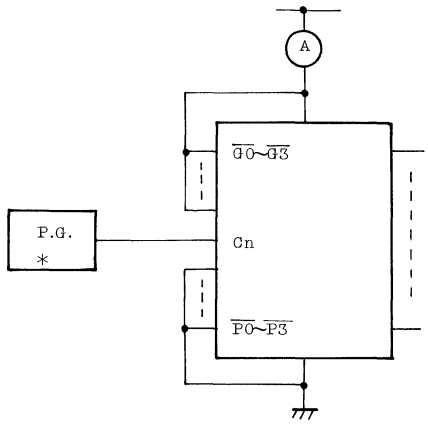
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

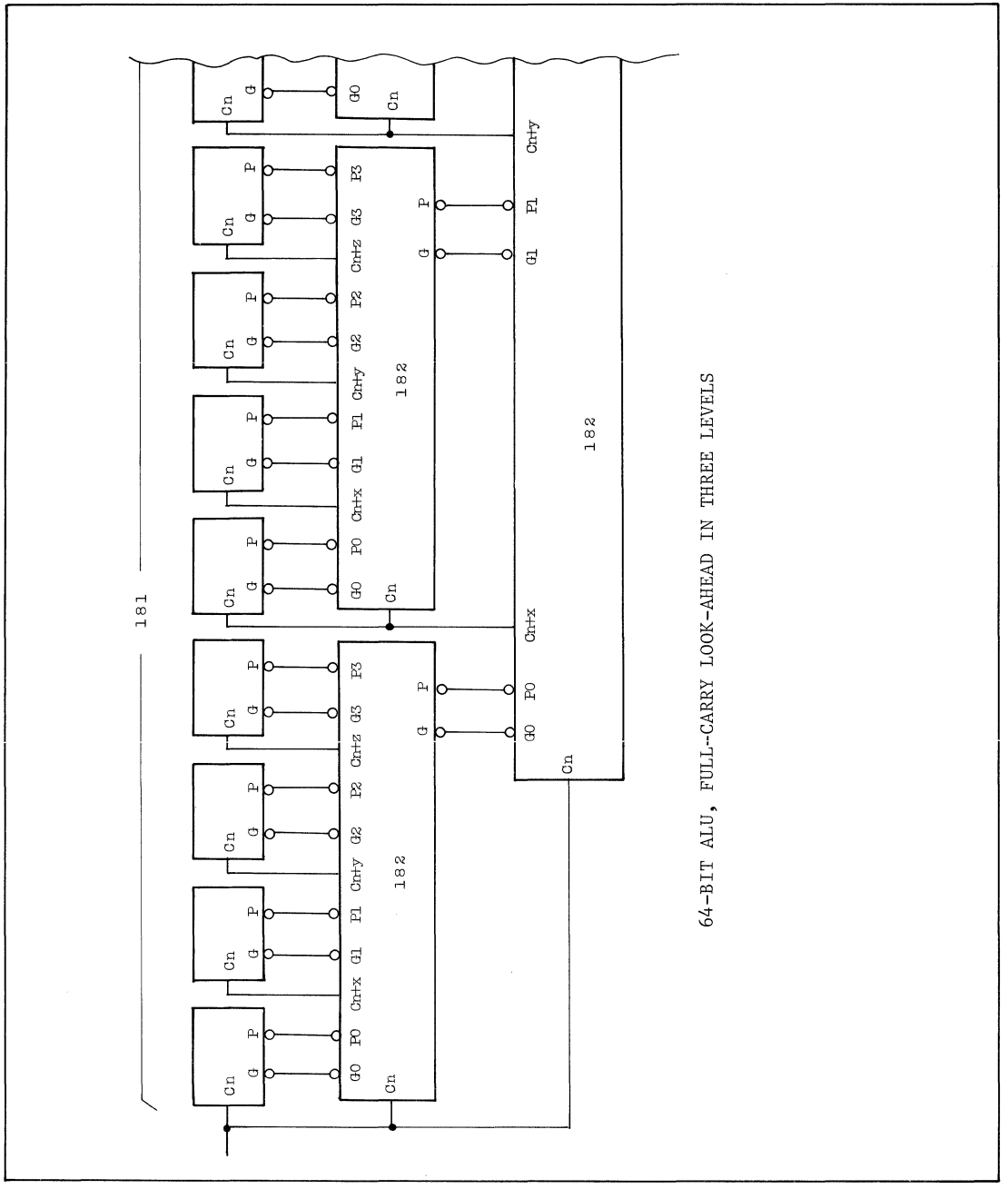


$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION



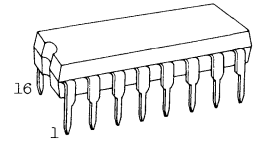
64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

TC74HC190P/F BCD UP/DOWN COUNTER
TC74HC191P/F 4-BIT BINARY UP/DOWN COUNTER

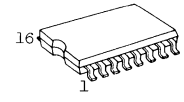
The TC74HC190 and TC74HC191 are high speed CMOS 4-BIT UP/DOWN COUNTERS fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC190 is BCD up/down counter and the TC74HC191 is 4-bit binary up/down counter.
These devices have asynchronous inputs LOAD ($\overline{LOAD}$). $\overline{LOAD}$ is active low and Load the load data.
The direction of the count is determined by the level of the DOWN/$\overline{UP}$ input. When low, the counter counts up and when high, it counts down. These counter change on the positive transition of the clock input.
Enable input ($\overline{ENABLE}$) and two CARRY output ($\overline{RIPPLE\ CLOCK\ OUT}$, MAX/MIN) are provided to enable easy cascading of counters, which facilitates easy implementation of N-bit counters without using external gate.
All inputs are equipped with protection circuits against static discahrge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- High Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS190/191



DIP16(3D16A-P)



MFP16(F16GC-P)

TRUTH TABLE

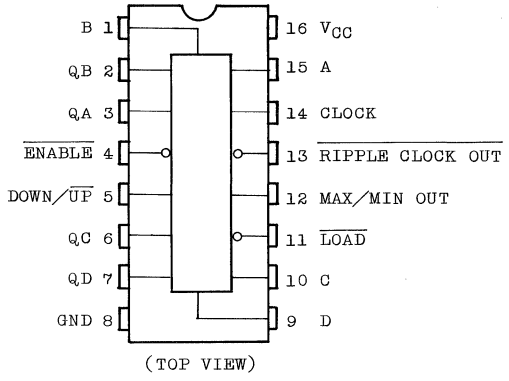
INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	Preset Data
H	L	L	↓	Up Count				Up count
H	L	H	↓	Down Count				Down Count
H	H	X	↓	No Change				No Count
H	X	X	↑	No Change				No Count

Note X: Don't care

a ∿ d: The level of steady state inputs at inputs A through D respectively.

PIN ASSIGMENT

TC74HC190/191



ABSOLUTE MAXIMUM RATINGS

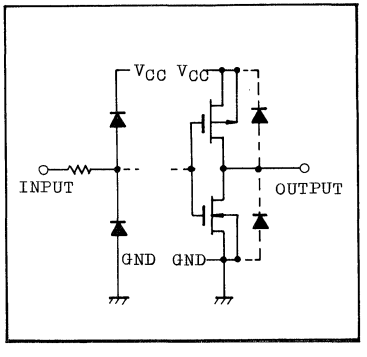
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

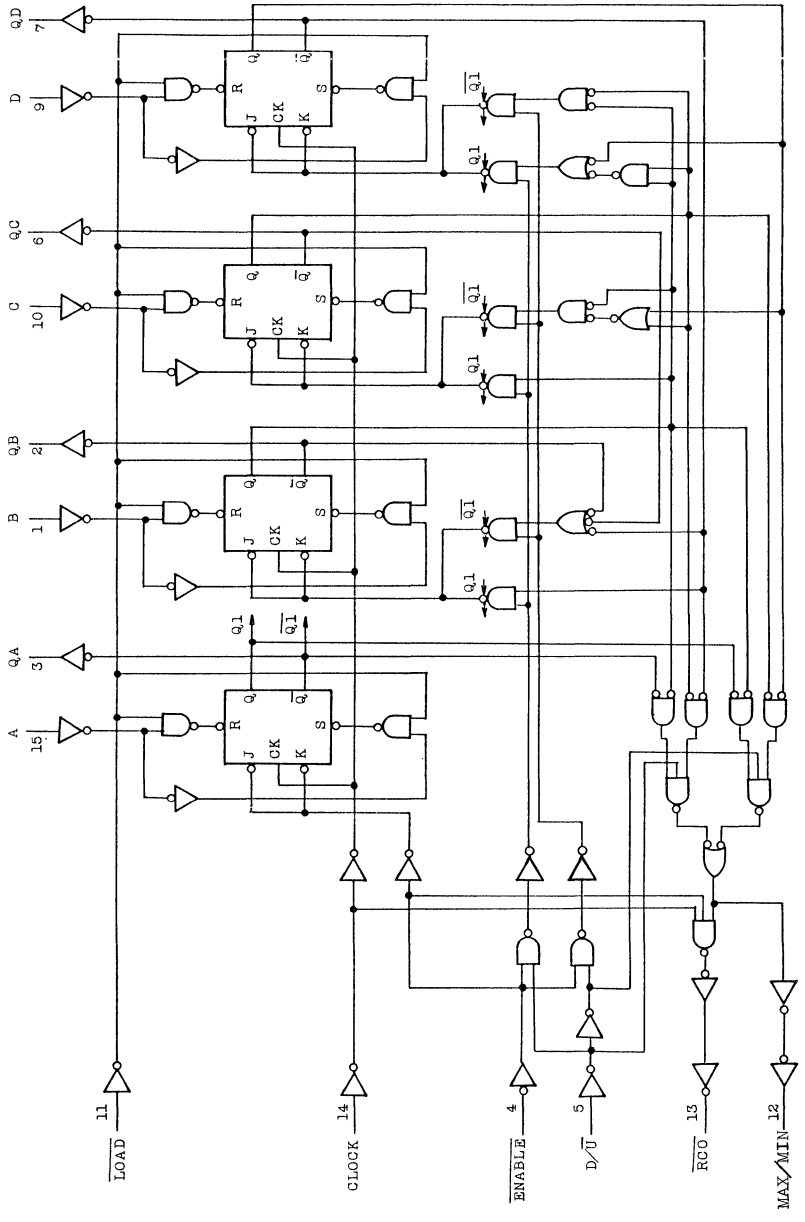
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



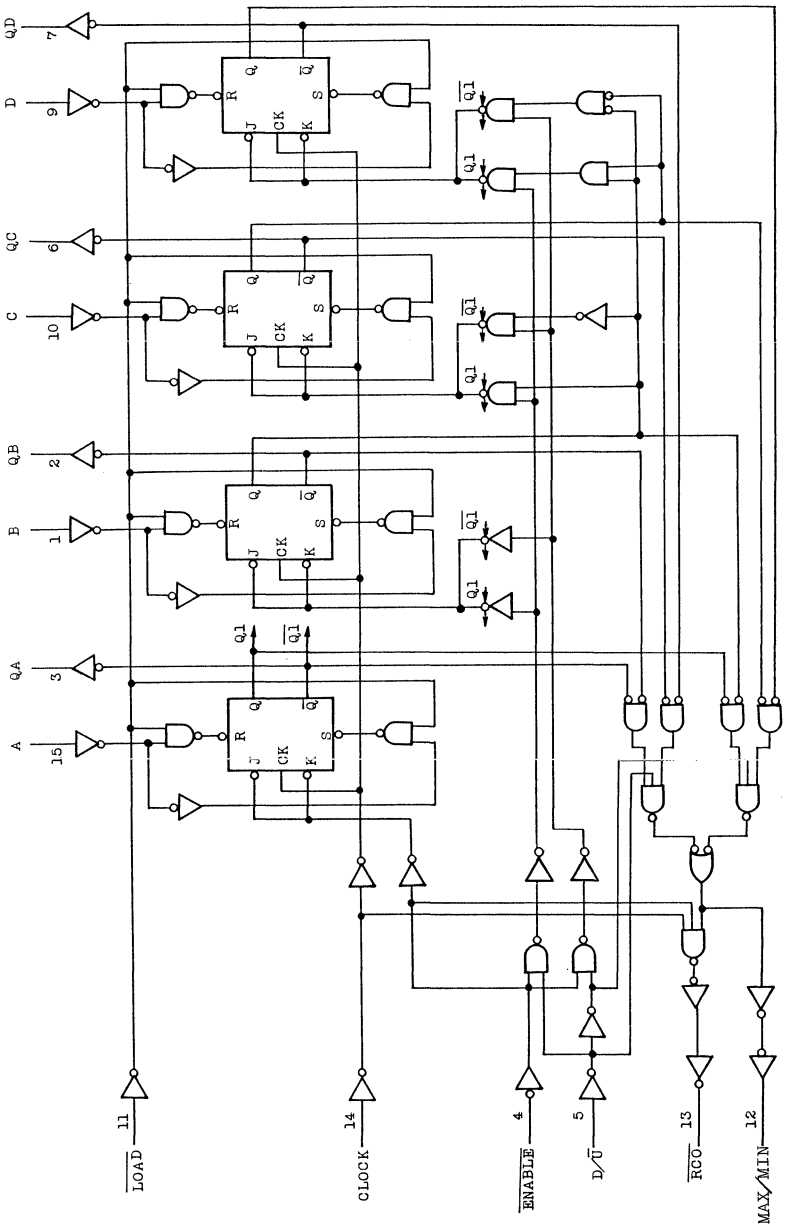
LOGIC DIAGRAM - 1

TC74HC190



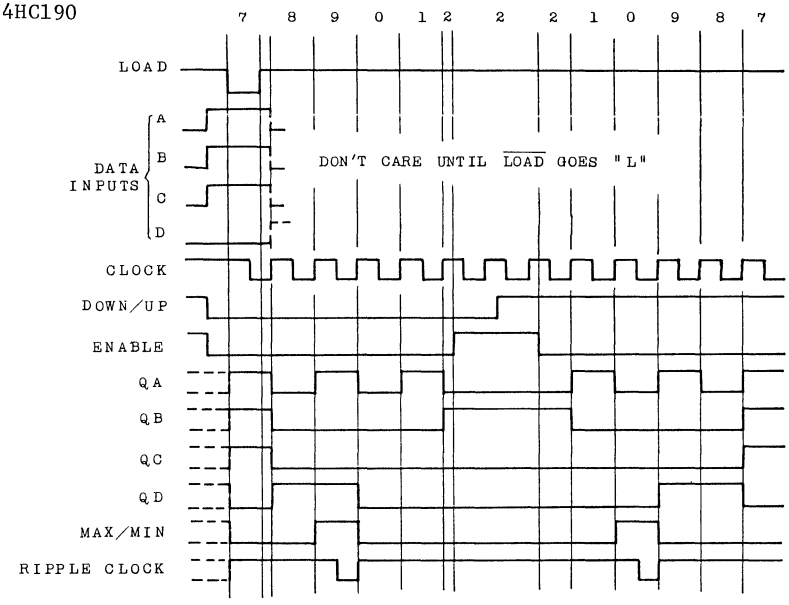
LOGIC DIAGRAM - 2

TC74HC191

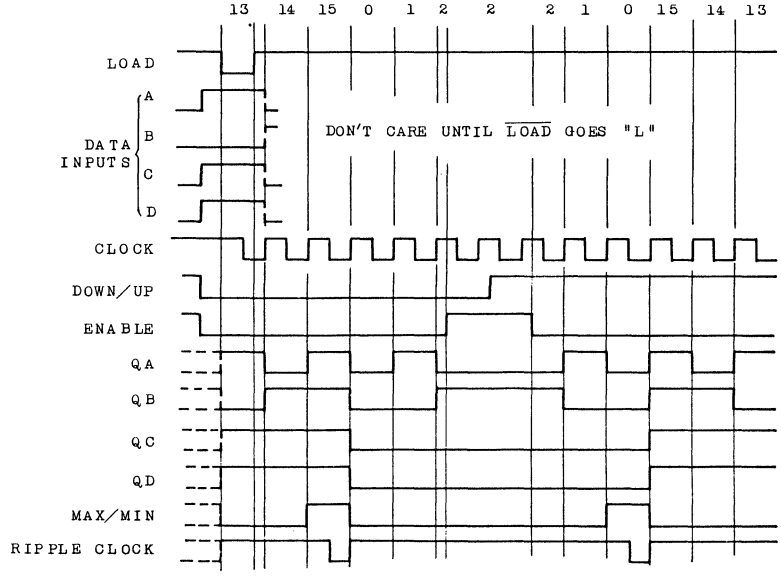


TIMING CHART

TC74HC190



TC74HC191



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagrtion Dealy Time (CLOCK - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{pLH} t_{pHL}		2.0	-	104	205	-	255	ns
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Propagation Dalay Time (DATA -Q)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time ($\overline{ENABLE}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (D/$\overline{U}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (D/$\overline{U}$ - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	25	42	-	20	-	
			6.0	29	49	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	45	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Set-up Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_s		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	

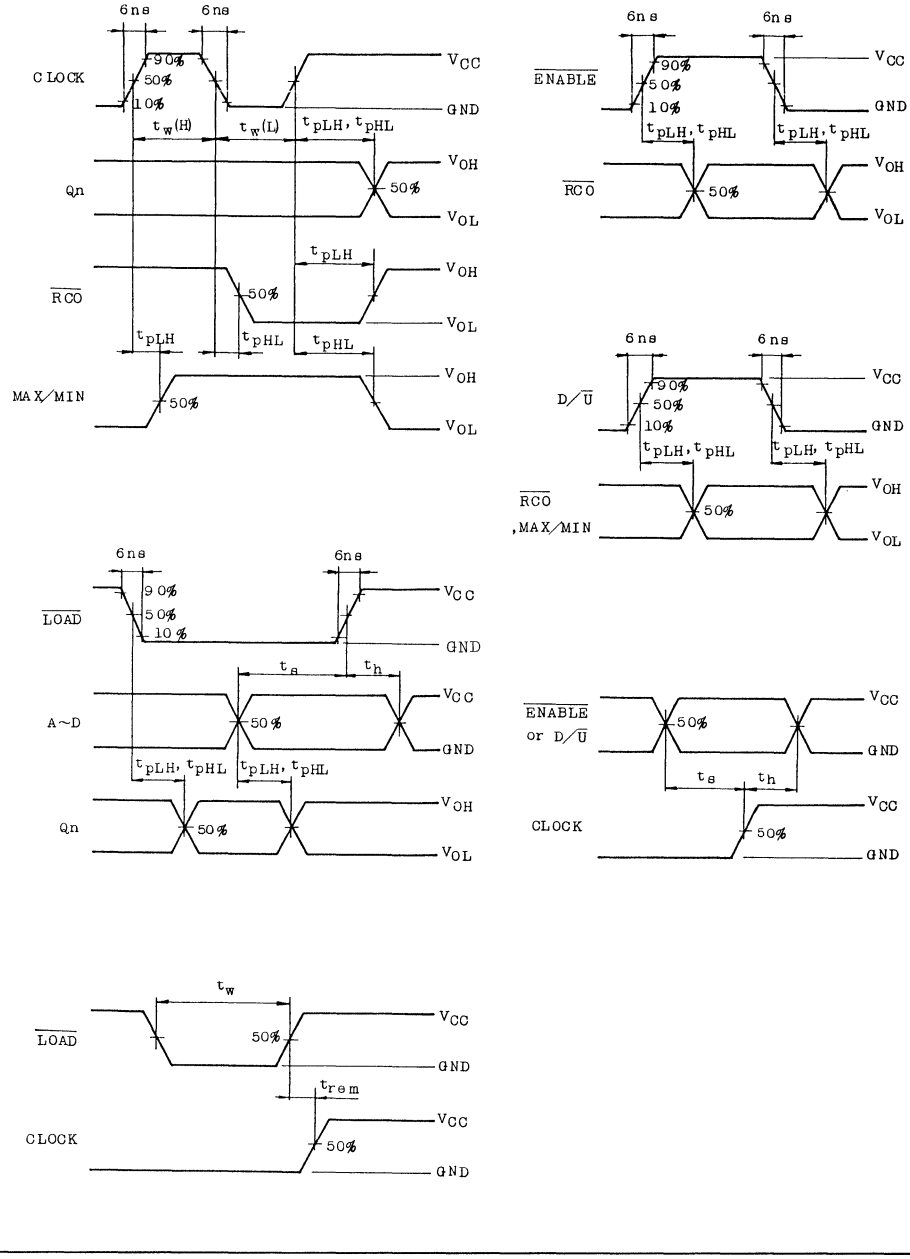
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	5	-	5	ns
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}				5	10		10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	124	-	-	-	

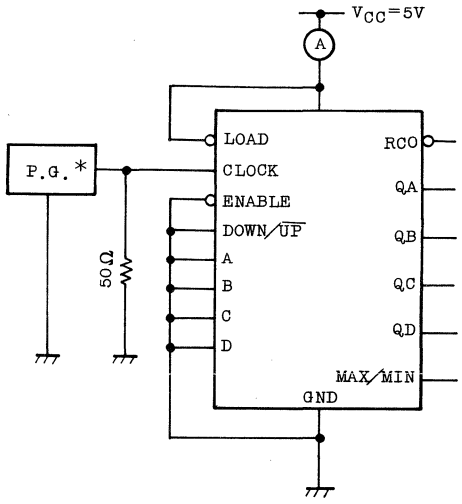
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST WAVEFORM



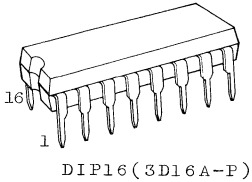
* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC192P/F SYNCHRONOUS UP/DOWN DECADE COUNTER
TC74HC193P/F SYNCHRONOUS UP/DOWN BINARY COUNTER

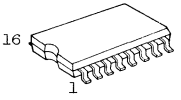
The TC74HC192 and TC74HC193 are high speed CMOS SYNCRONOUS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C^2MOS technology. They achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipaiton. These counters have a clear input(CLEAR), a load input($\overline{LOAD}$), load data inputs(A - D), two clock inputs(COUNT UP/COUNT DOWN), four count data outputs(Q_A - Q_D) and carry and borrow outputs. CLEAR is active high and forces Q_A thru Q_D outputs low independently of the other inputs. $\overline{LOAD}$ is active low and load the load data when CLEAR input is held low. COUNT UP input pulse and COUNT DOWN input pulse independently bring a up-counting or down at the positive going transition of each clock pulse. CARRY and BORROW outputs are provided in order to make a cascade connection without external circuitry. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=32MHZ(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS192/193



DIP16(3D16A-P)



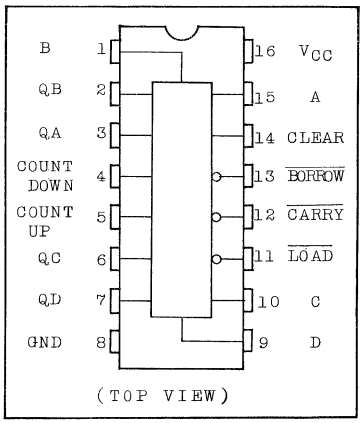
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

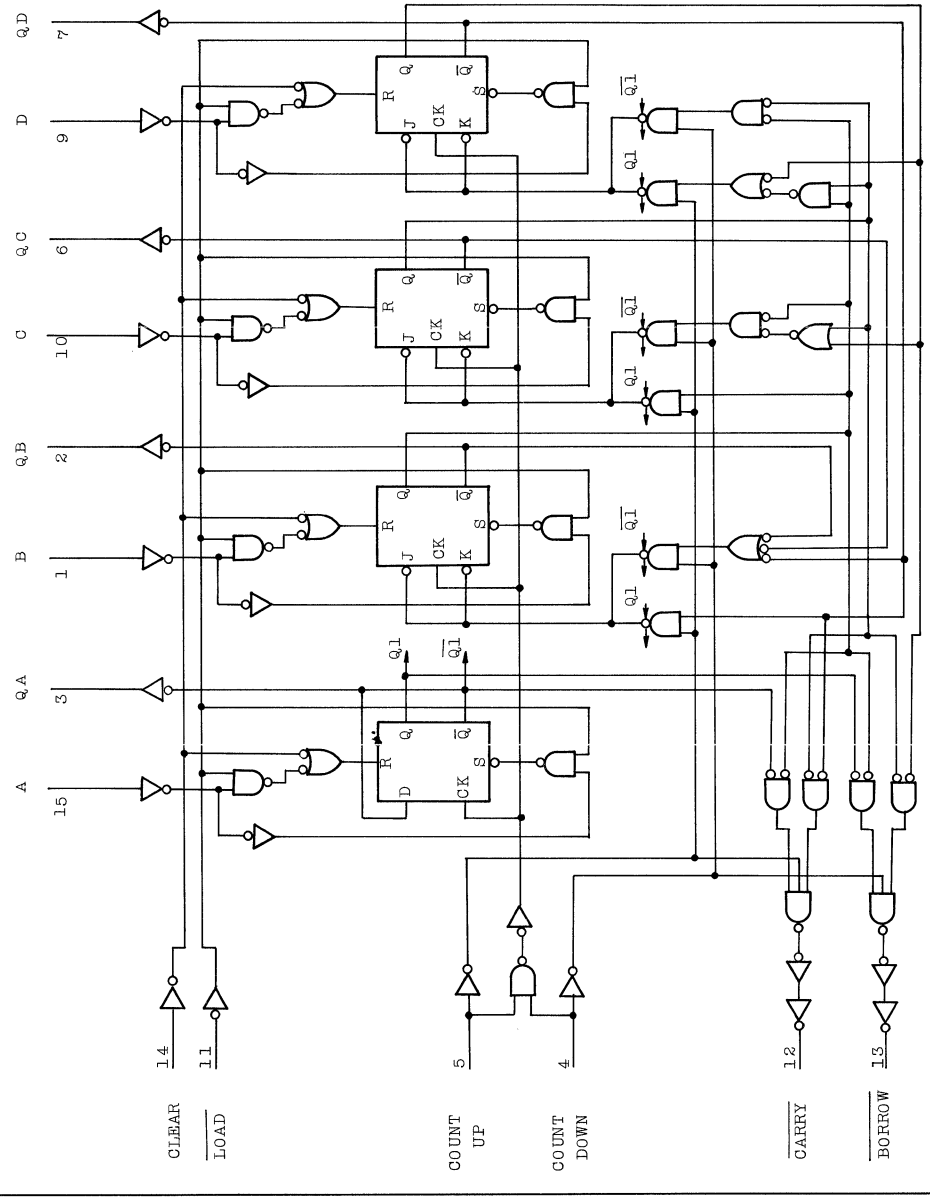
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



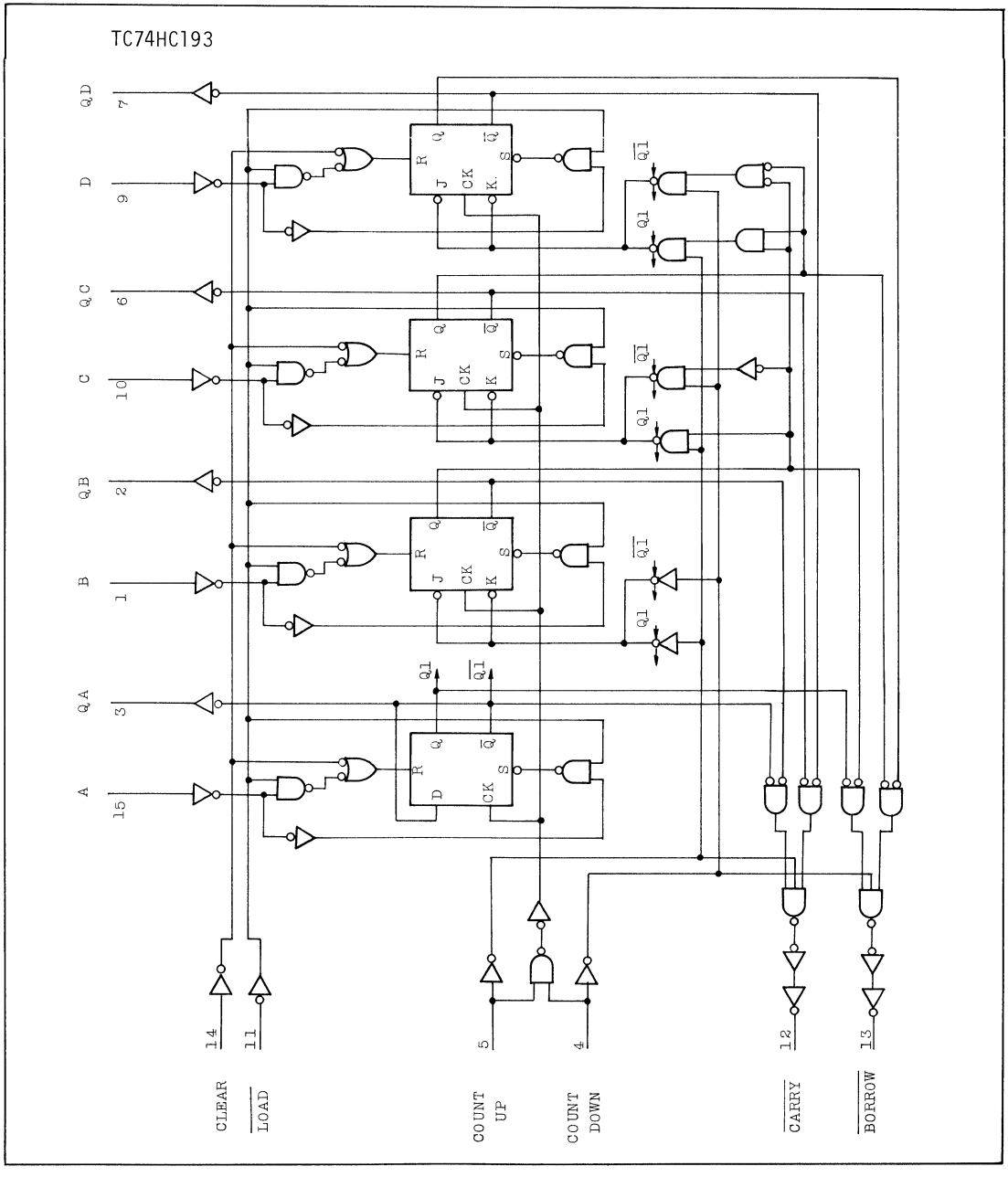
CIRCUIT DIAGRAM

TC74HC192

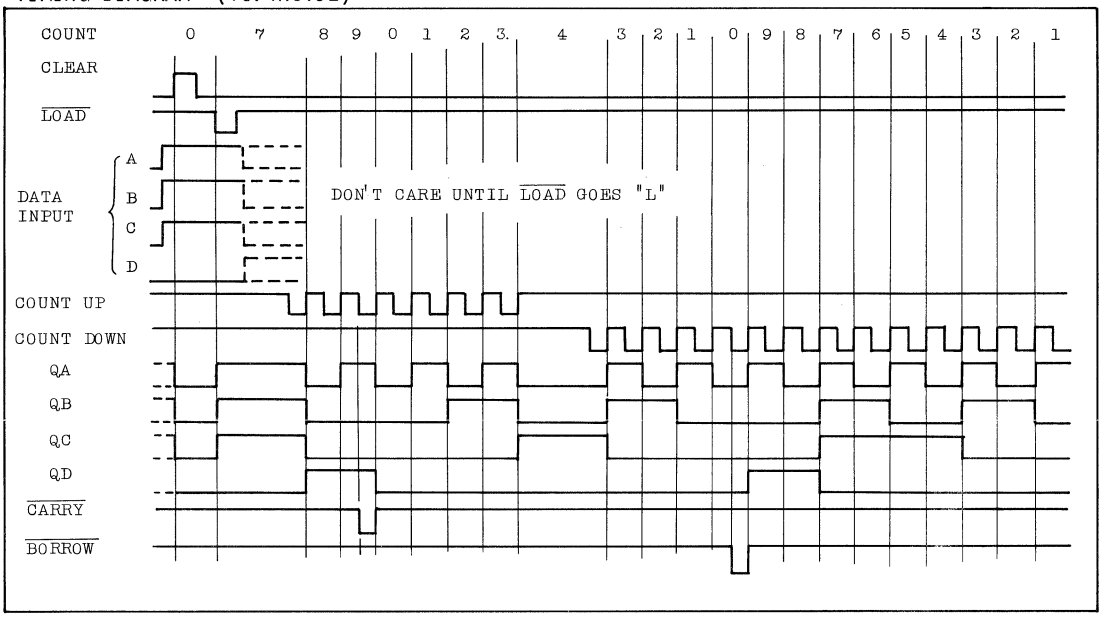


CIRCUIT DIAGRAM

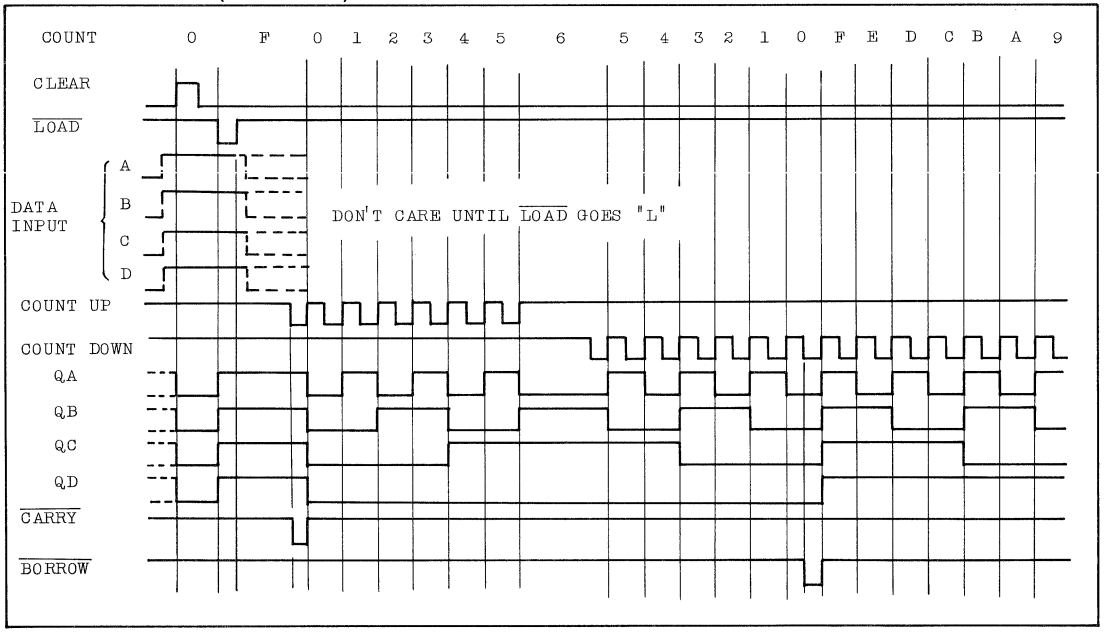
TC74HC193



TIMING DIAGRAM (TC74HC192)



TIMING DIAGRAM (TC74HC193)



TRUTH TABLE

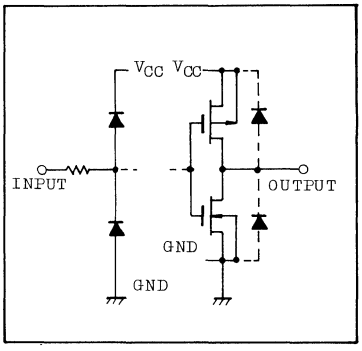
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	FUNCTION
↑	H	H	L	COUNT UP
↓	H	H	L	NO COUNT
H	↑	H	L	COUNT DOWN
H	↓	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (UP, DOWN - Q)	t_{PLH} t_{PHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Propagation Delay Time (UP - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	76	140	-	175	
			4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time (DOWN - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	76	140	-	175	
			4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{PLH} t_{PHL}		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	160	310	-	390	
			4.5	-	40	62	-	78	
			6.0	-	34	53	-	66	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	144	280	-	350	
			4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (JAM IN - Q)	t_{PLH} t_{PHL}		2.0	-	116	230	-	290	ns
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Propagation Delay Time (JAM IN - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	172	330	-	415	
			4.5	-	43	66	-	83	
			6.0	-	37	56	-	71	
Propagation Delay Time (JAM IN - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	144	265	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (CLEAR - Q)	t_{PHL}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (CLEAR - $\overline{CARRY}$)	t_{PLH}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CLEAR - $\overline{BORROW}$)	t_{PHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Frequency (CLOCK)	f_{MAX}		2.0	3	7	-	2.5	-	MHz
			4.5	16	29	-	13	-	
			6.0	19	34	-	15	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	70	150	-	190	ns
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	32	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(H)}$		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	45	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	

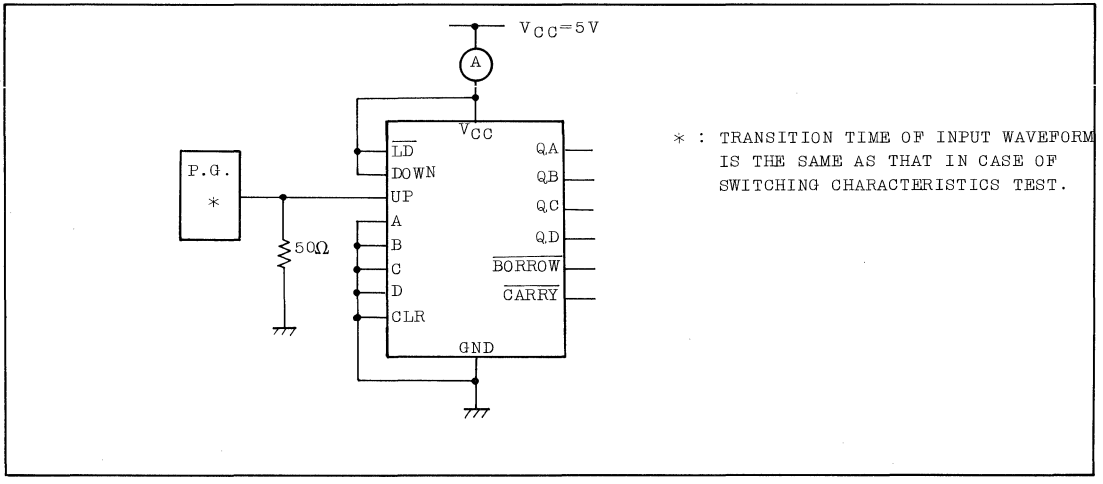
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_s		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	66	-	-	-	

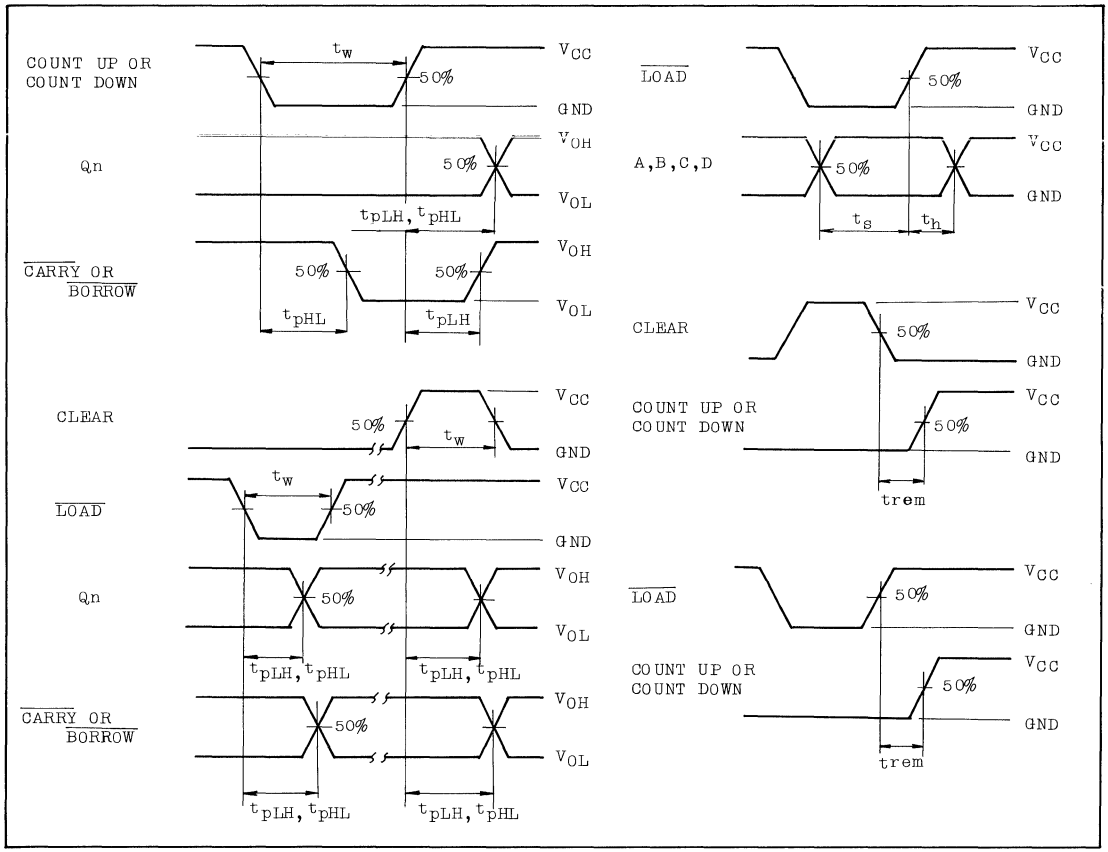
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{DD(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

$I_{CC(opr.)}$ TEST WAVERORM



SWITCHING CHARACTERISTICS TEST WAVEFORM



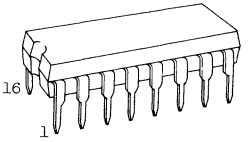
TC74HC194P/F

TC74HC194P/F 4-BIT PIPO SHIFT REGISTER

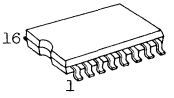
The TC74HC194 a high speed CMOS 4-BIT BIDIRECTIONAL SHIFT REGISTER fabricated with silicon C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of parallel in, parallel out, 4 ibt register with shift right and shift left input. In parallel mode, data of D0 ∿ D3 are stored into the internal flip-flops at the low-to-high level transition of the clock pulse. Shift right and shift left inputs are inhibited during parallel operating mode. In shift right and shift left modes, data from shift right and shift left inputs are shifted to the right and to the left by 1 bit, respectively, synchronously with the low-to-high level edge of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS194



DIP16(3D16A-P)



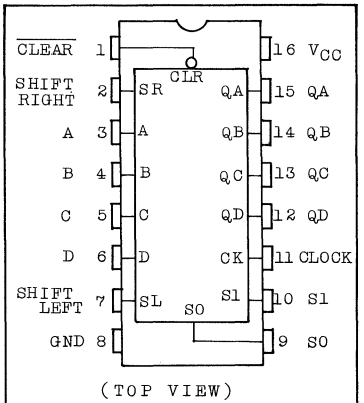
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



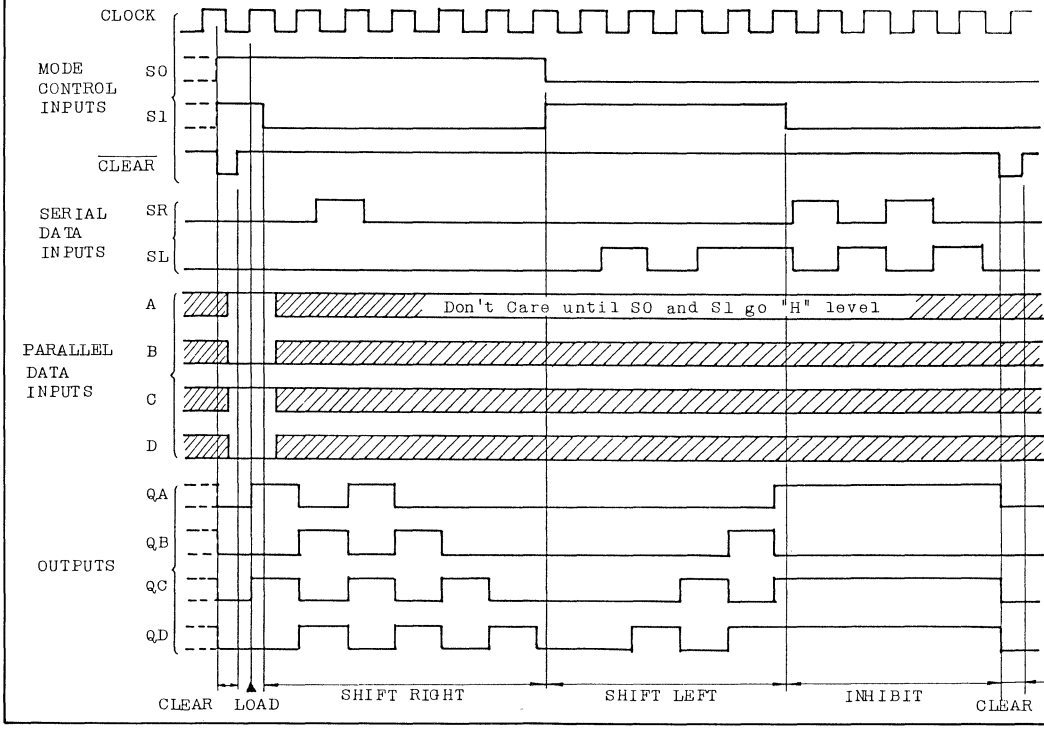
(TOP VIEW)

TRUTH TABLE

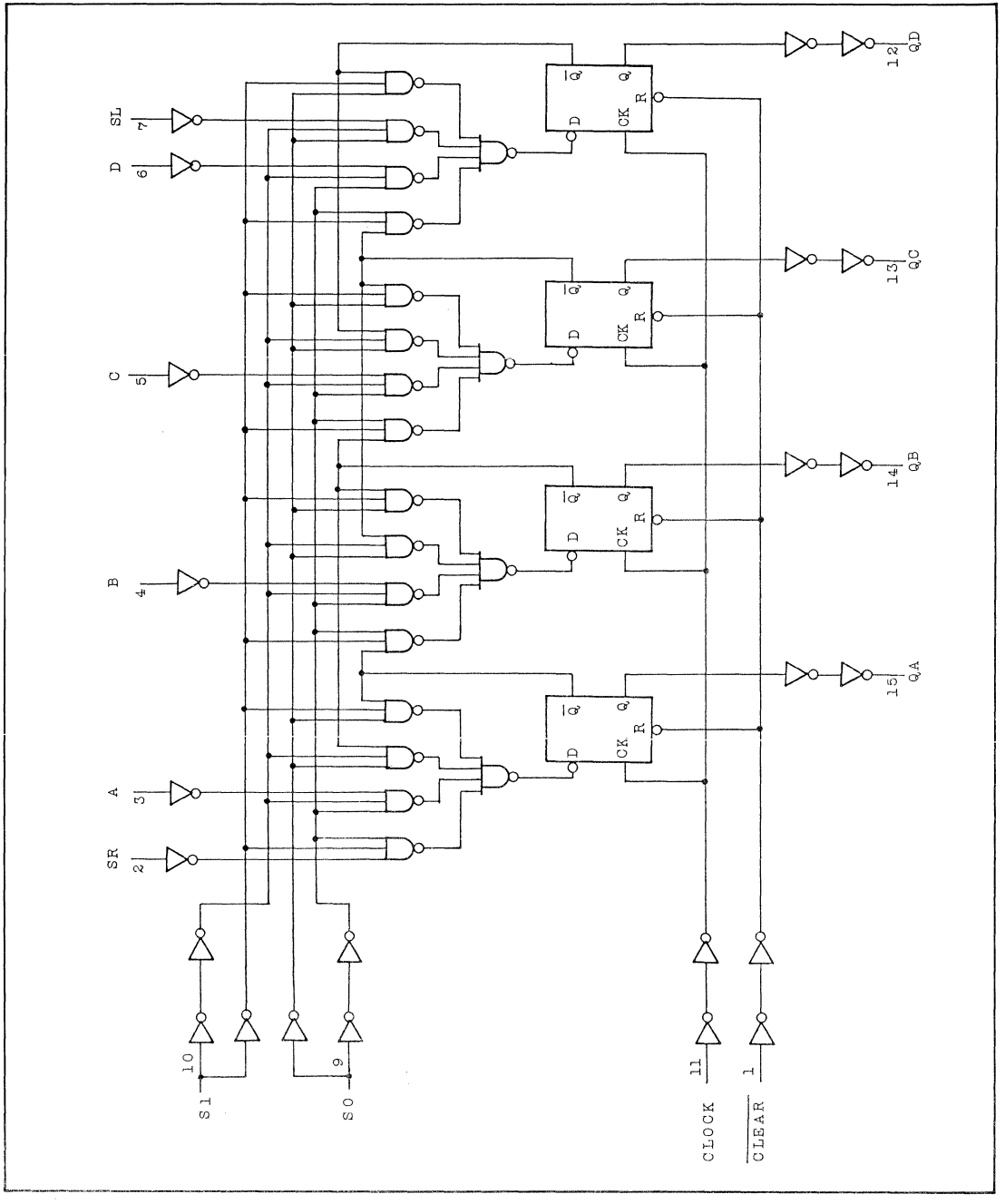
INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SL	SR	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

X: Don't care
a ∿ d: The level of steady state input voltage at input A ∿ D respectively
QA0 ∿ QD0: No change
QAn ∿ QDn: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

TIMING CHART



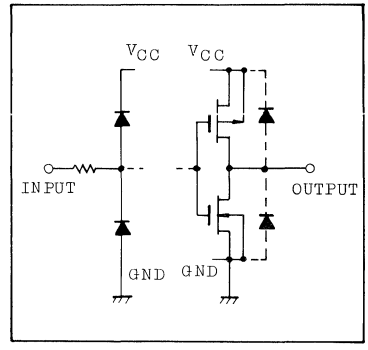
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15		
				6.0	4.2	-	-	4.2		
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

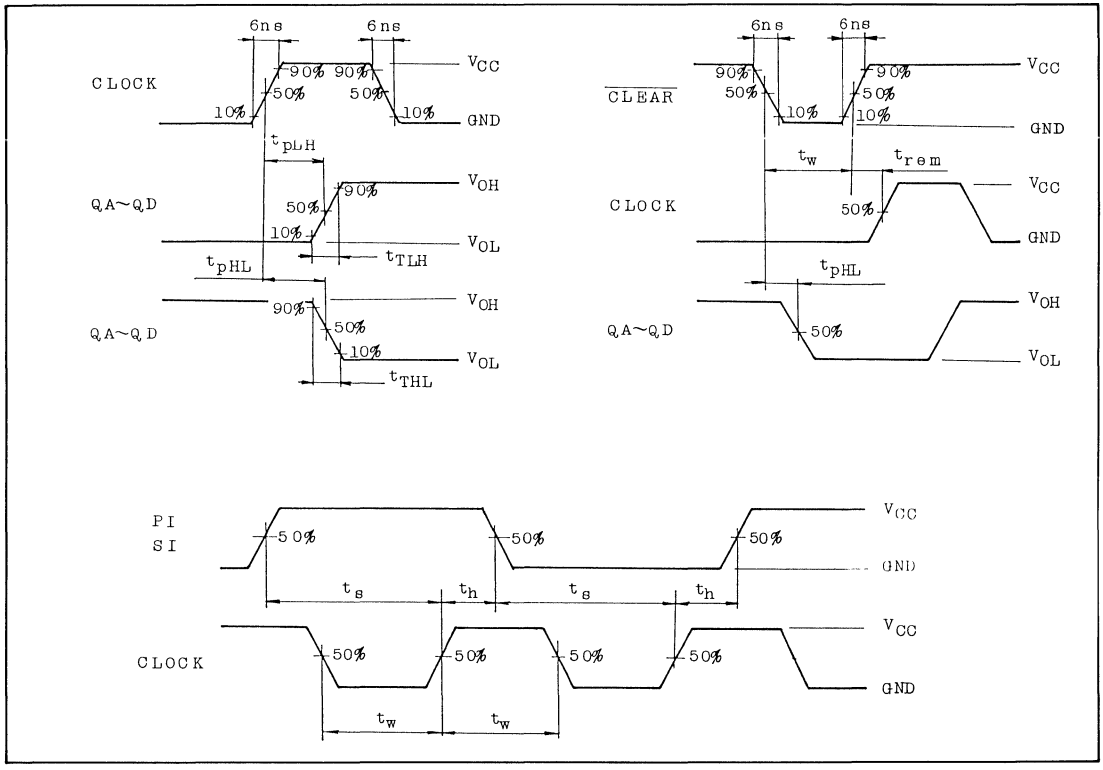
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S_{IN}, P_{IN})	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S0, S1)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	103	-	-	-	

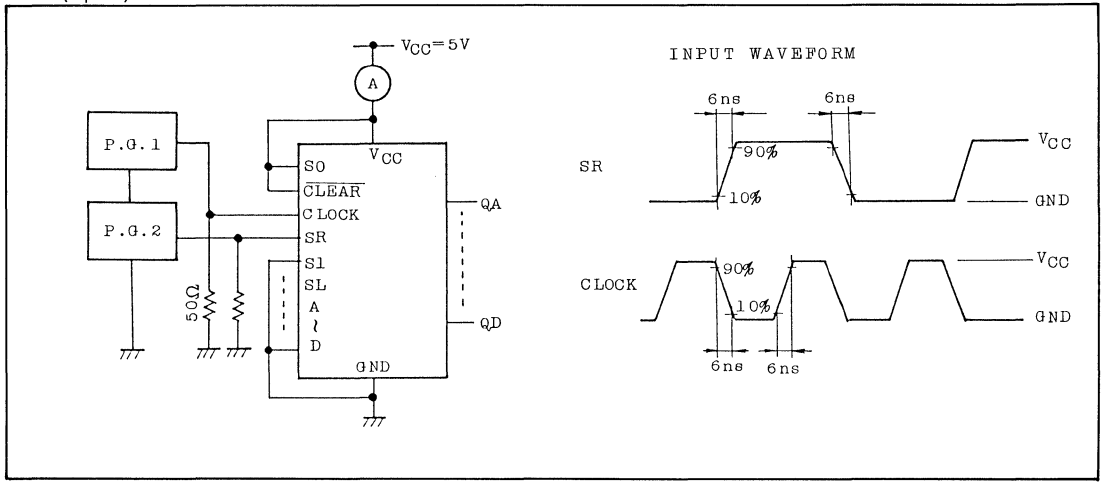
Note (1): C_{PD} is defined as the vlaue of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit.) Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



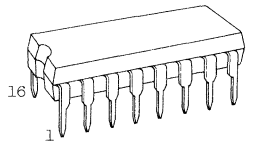
TC74HC195P/F

TC74HC195P/F 4-BIT PARALLEL SHIFT REGISTER

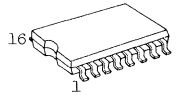
The TC74HC195 is a high speed CMOS 4-BIT SHIFT REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This register features parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{LOAD}$ input. When the SHIFT/$\overline{LOAD}$ input is held low, the parallel mode operation is designated. The data of A∿D inputs is loaded into the internal register and appears at the outputs after the positive transition of the clock. When the SHIFT/$\overline{LOAD}$ input is held high, the serial mode operation having J, $\overline{K}$ logical inputs is designated and four flip-flops perform shifting at the positive transition of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS195



DIP16(3D16A-P)



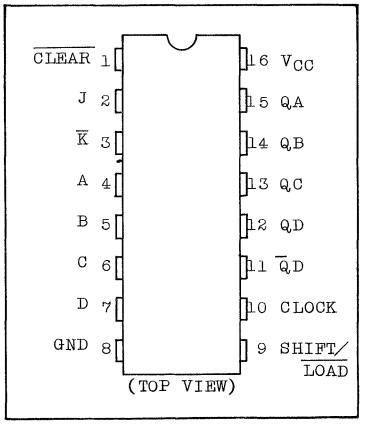
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	X	↓	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

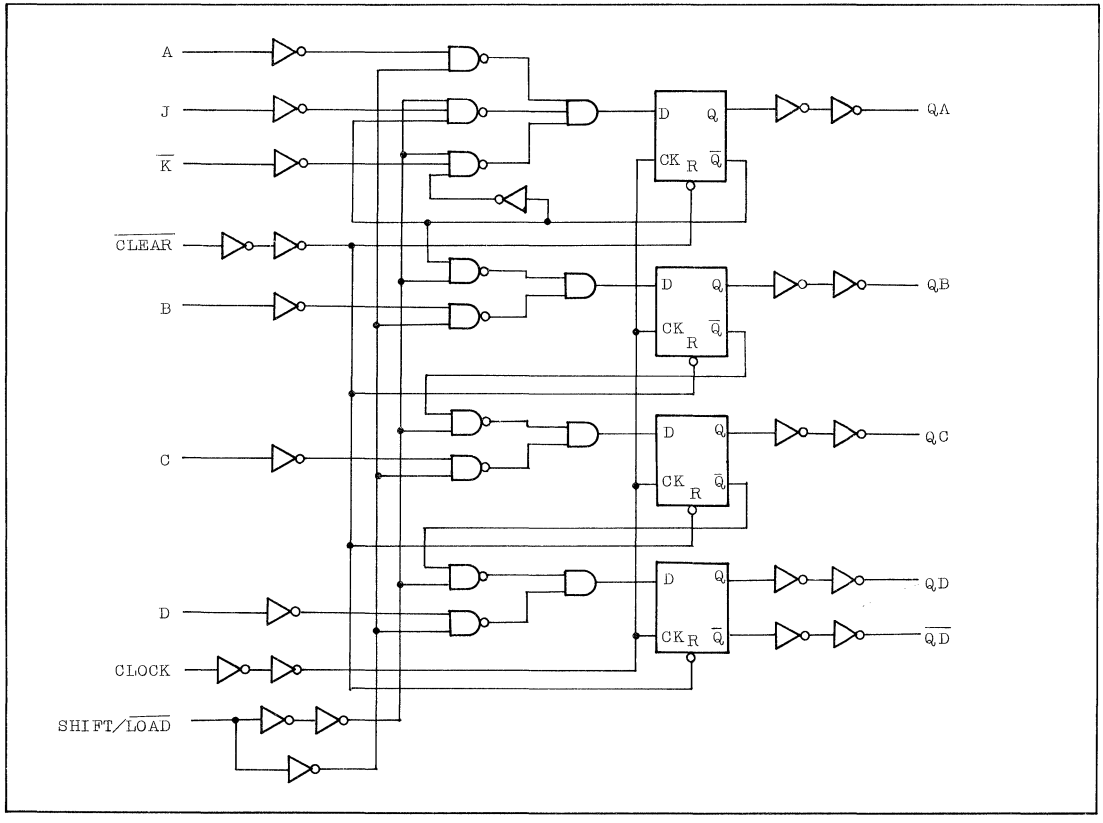
X: Don't care

$Q_{A0} \sim A_{D0}$: No change

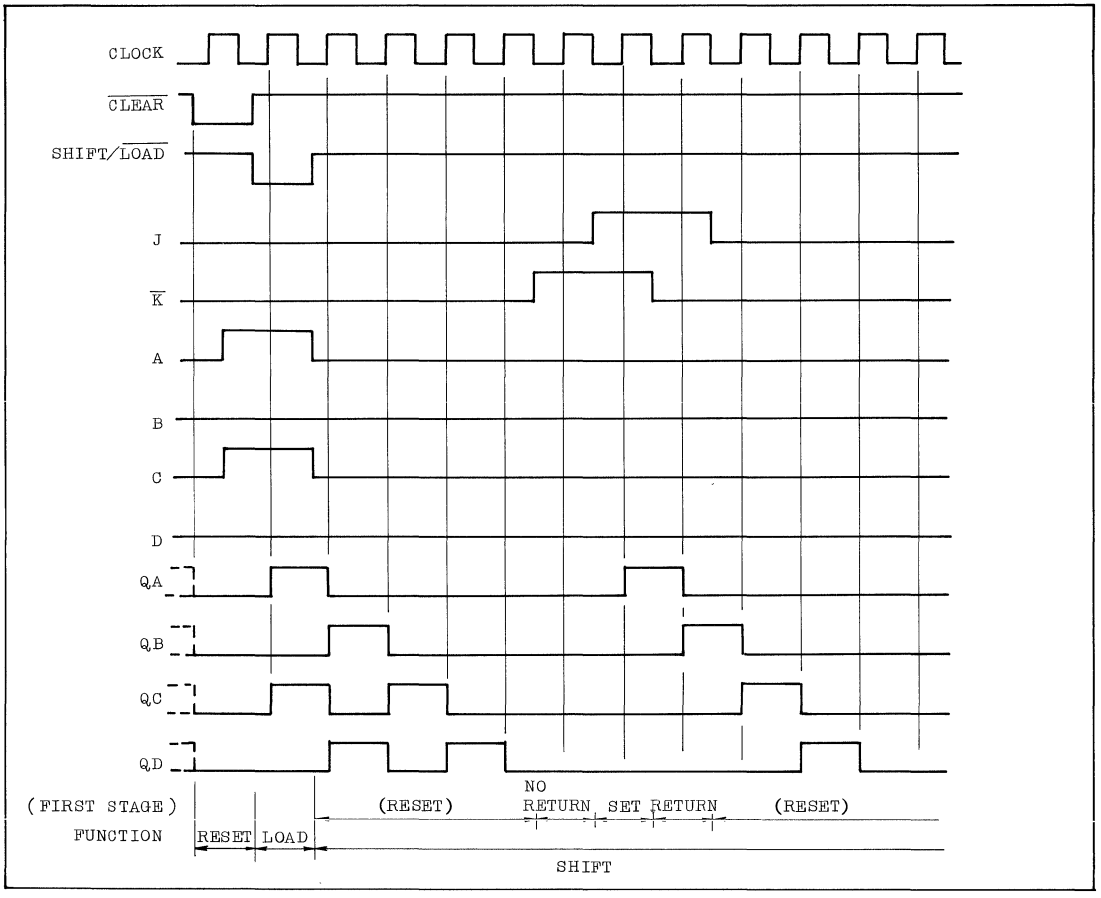
$Q_{An} \sim Q_{Dn}$: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

a ...d, $\overline{d}$: The level of steady state input voltage at inputs A ~ D respectively.

LOGIC DIAGRAM



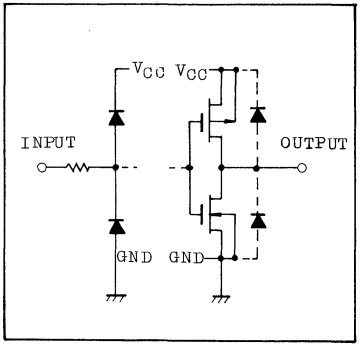
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Propagation Delay Time ($\overline{CLR}$ - Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	32	51	-	27	-	
			6.0	38	60	-	32	-	

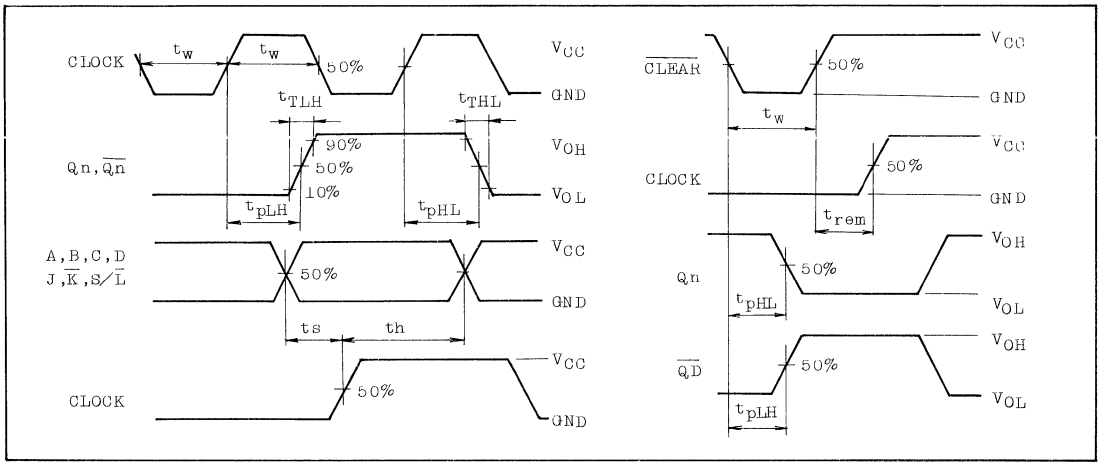
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (PI)	t_s		2.0	-	15	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set Up Time (J, $\overline{K}$, S/$\overline{L}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	1	5	-	6	
			6.0	-	1	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	115	-	-	-	

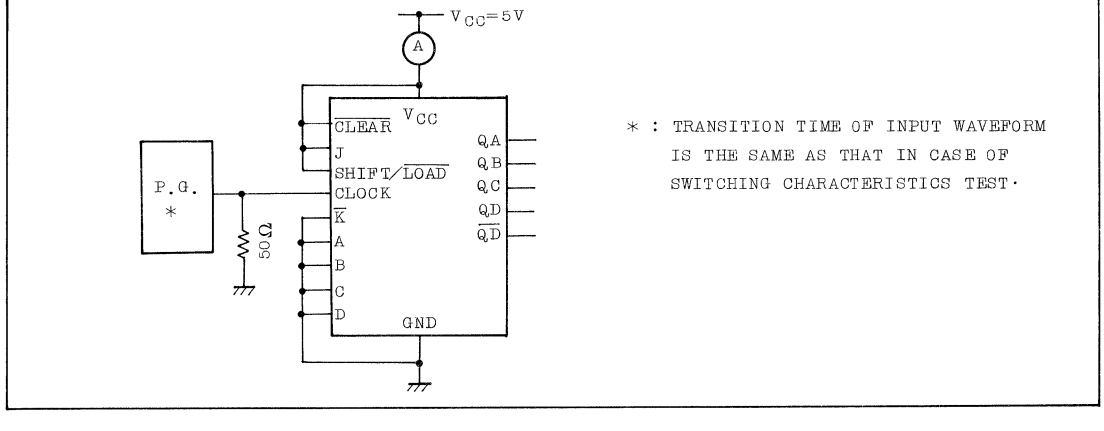
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC221P/F

TC74HC221P/F DUAL MONOSTABLE MULTIVIBRATOR

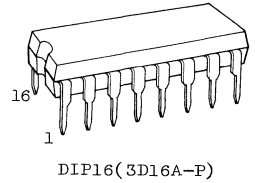
The TC74HC221 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaing the CMOS low power dissipation.
There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CLR}$ INPUT (Positive-edge input). After triggering, Output keeps MONOSTABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CLR}$ input breaks this STABLE STATE. Next coming new trigger in MONOSTABLE period is not effected. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5kΩ to 1MΩ
$V_{CC}\geqq$3.0V from 1kΩ to 1MΩ

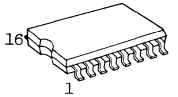
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=32ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at VCC=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range .... t_w(OUT)=150ns ∿ 60s over at V_{CC}=4.5V
- Pin and Function Compatible with LS221



DIP16(3D16A-P)



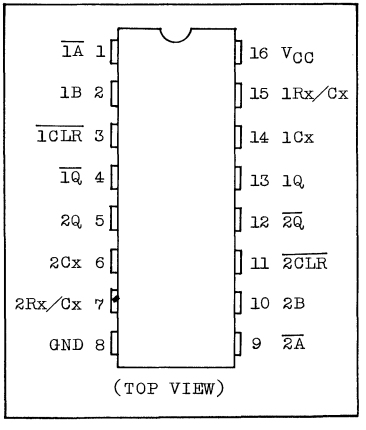
MFP16(F16GG-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP) * 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



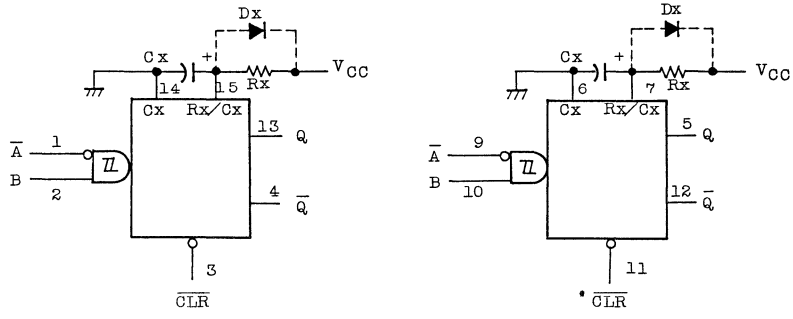
TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎴	OUTPUT ENABLE
X	L	H	L△	H△	INHIBIT
H	X	H	L△	H△	INHIBIT
L	↑	H	⎍	⎴	OUTPUT ENABLE
L	H	↑	⎍	⎴	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE

△: EXCEPT FOR MONOSTABLE PERIOD

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

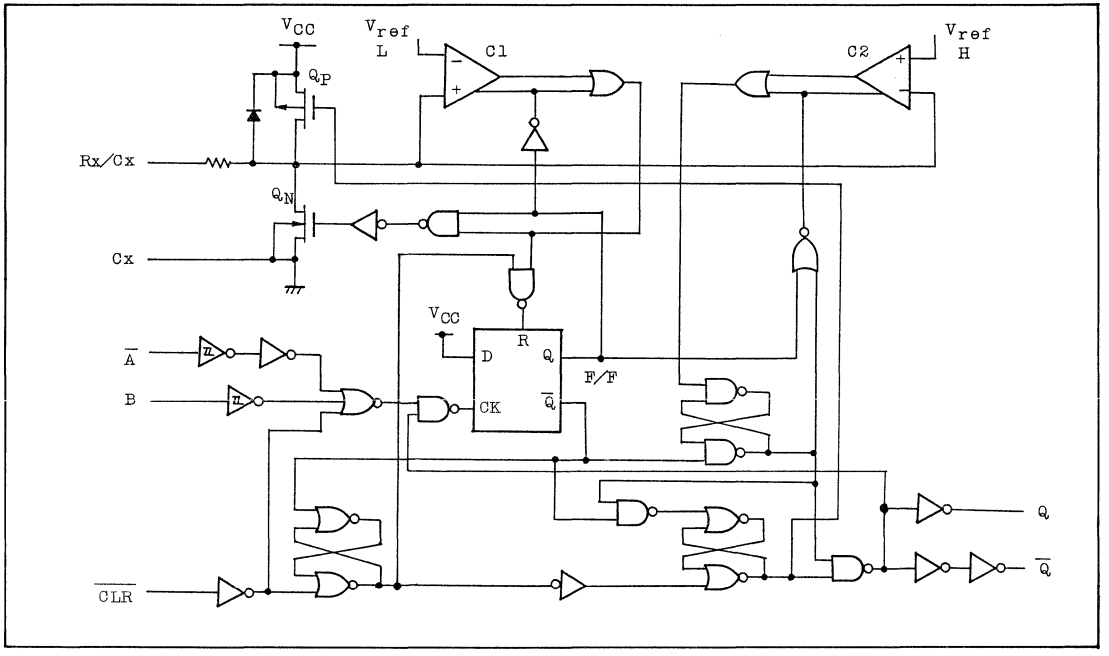
External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls dowen rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

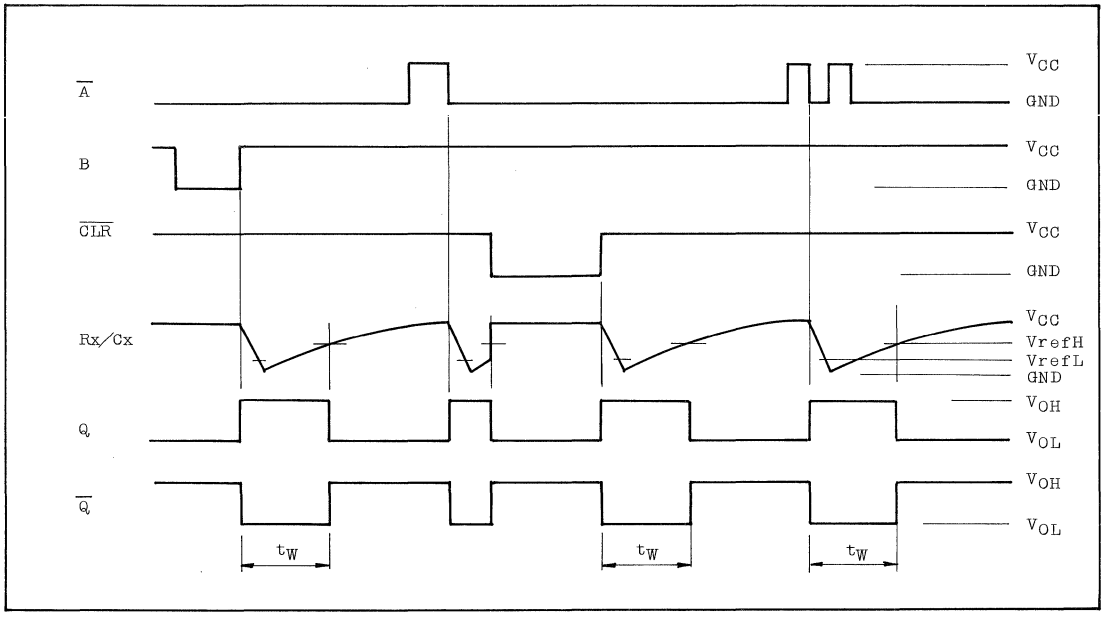
(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CLR}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx.Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_W(OUT)$ is as follows.

$$t_W(OUT) = 0.70 \quad Cx \; Rx$$

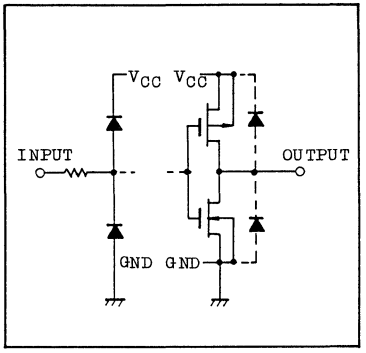
(3) Reset operation

$\overline{CLR}$ is normally "H". If $\overline{CLR}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CLR}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=−40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=VCC or GND R/C_{ext}=0.5V_{CC}		2.0	−	40	120	−	160	μA
				4.5	−	0.1	0.3	−	0.4	mA
				6.0	−	0.2	0.6	−	0.8	mA

*: per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

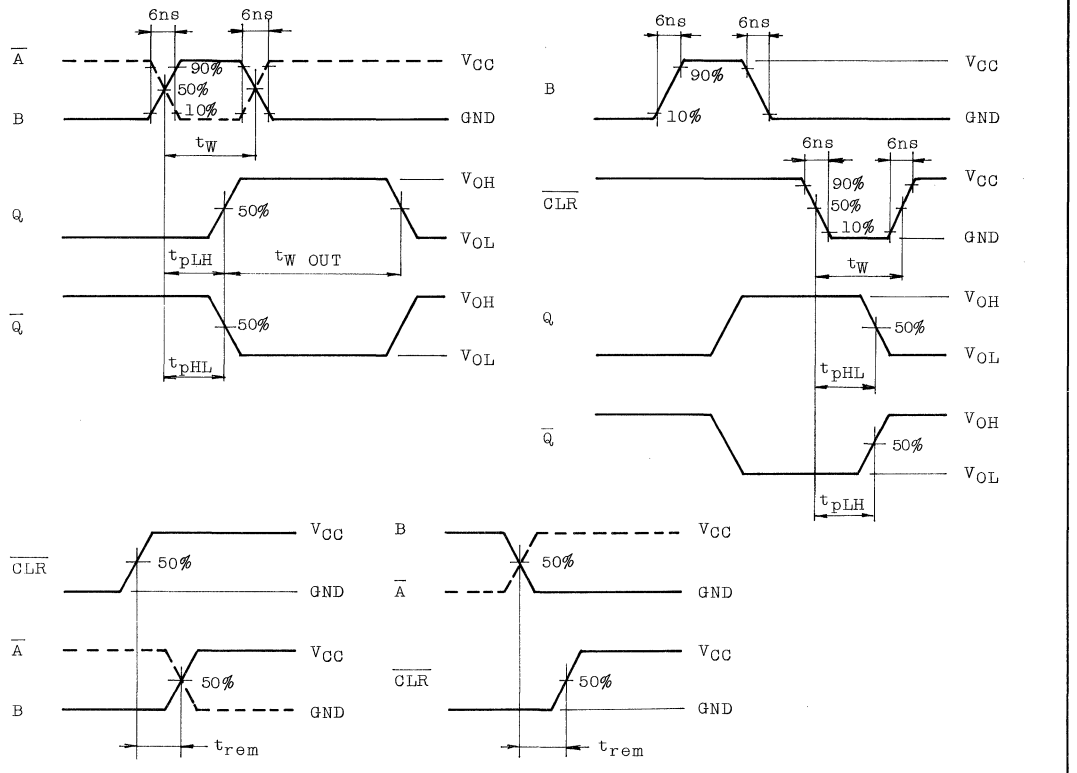
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$,B TRIGGER-Q,$\overline{Q}$)	t_{pLH}		2.0	-	144	280	-	350	
	t_{pHL}		4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CLR}$ TRIGGER-Q,$\overline{Q}$)	t_{pLH}		2.0	-	164	310	-	390	
	t_{pHL}		4.5	-	41	62	-	78	
			6.0	-	35	53	-	66	
Propagation Delay Time ($\overline{CLR}$-Q,$\overline{Q}$)	t_{pLH}		2.0	-	108	210	-	265	
	t_{pHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Trigger Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error. Between Circuits In same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Removal Time ($\overline{A}$,B TRIGGER)	t_{rem}		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$ TRIGGER)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Output Pulse Width	t_{wOUT} (MIN)	Cx=0, Rx=5kΩ (V_{CC}=2V)	2.0	-	490	1450	-	1825	
		Rx=1kΩ (V_{CC}=4.5, 6V)	4.5	-	190	290	-	365	
			6.0	-	170	260	-	325	
Output Pulse Width	t_{wOUT}	Cx=0.01μF, Rx=10kΩ	2.0	72	85	98	72	98	μs
			4.5	72	80	88	72	88	
			6.0	72	80	88	72	88	
		Cx=0.1μF, Rx=10kΩ	2.0	0.67	0.75	0.83	0.67	0.83	ms
			4.5	0.67	0.73	0.79	0.67	0.79	
			6.0	0.67	0.73	0.79	0.67	0.79	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	109	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test circuit). Average operating current can be obtained by equation hereunder.

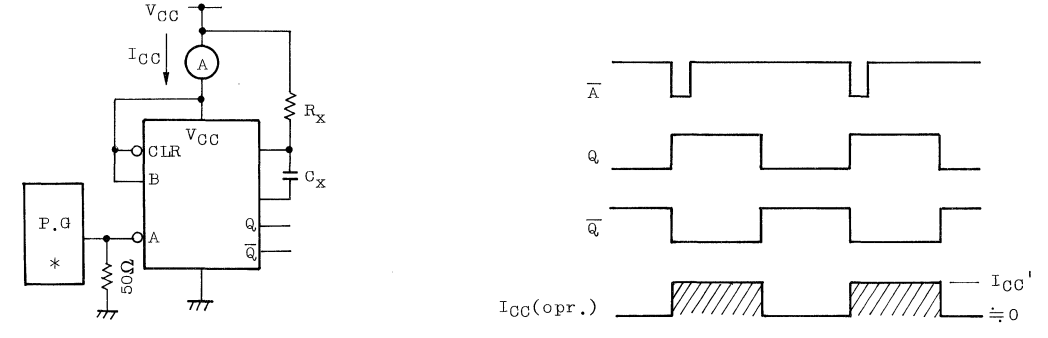
$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current, Duty: %)

SWITCHING CHARACTERISTICS TEST WAVEFORM

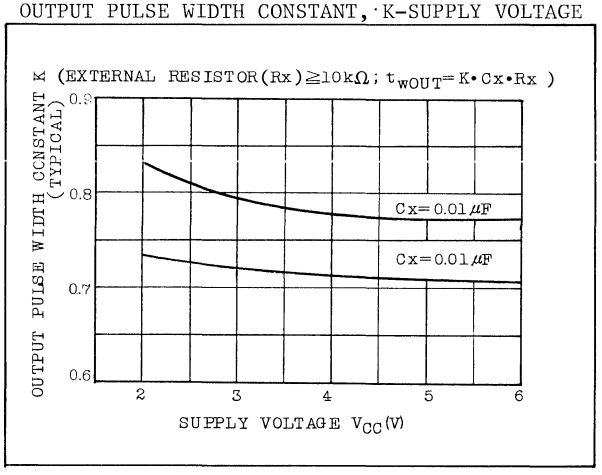


I_{CC}(opr.) TEST WAVEFROM

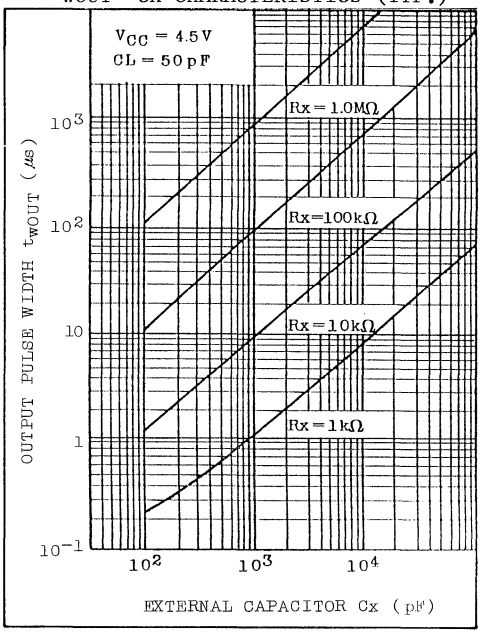


* INPUT TRANSITION TIME : 6ns ,
$V_{IH} = V_{CC}, V_{IL} = GND$

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



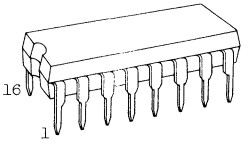
TC74HC237P/F

TC74HC237P/F 3-TO-8 LINE DECODER/LATCH

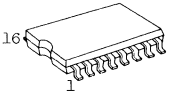
The TC74HC237 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go high. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Inverting type of the 74HC137



DIP16(3D16A-P)



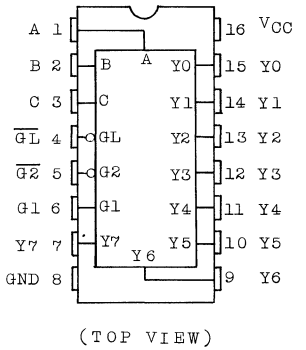
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



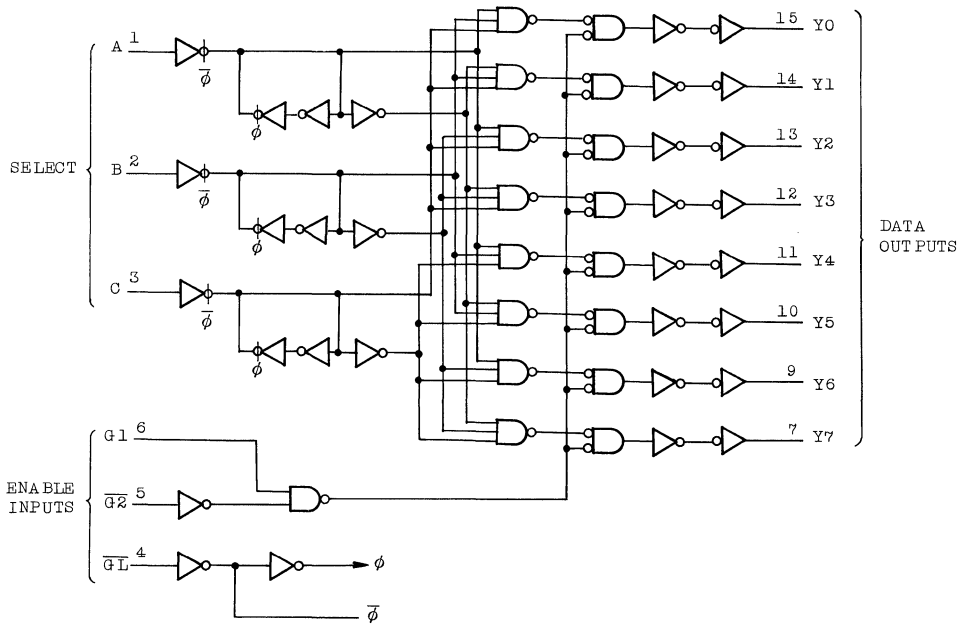
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H ; ALL OTHERS, L							

X : DON'T CARE

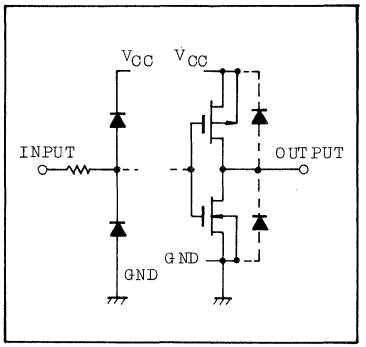
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

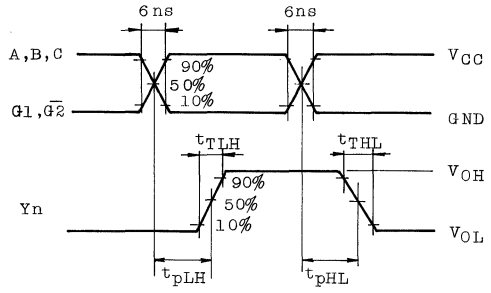
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

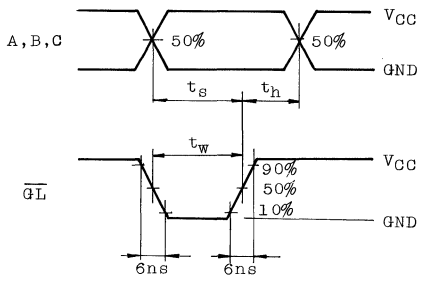
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - Y)	t_{pLH}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
	t_{pHL}		6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
	t_{pHL}		6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{GL}$ - Y)	t_{pLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
	t_{pHL}		6.0	-	22	34	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
	t_{pHL}		6.0	-	20	31	-	38	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		2.0	-	12	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

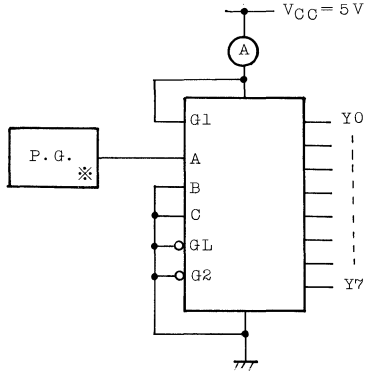
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



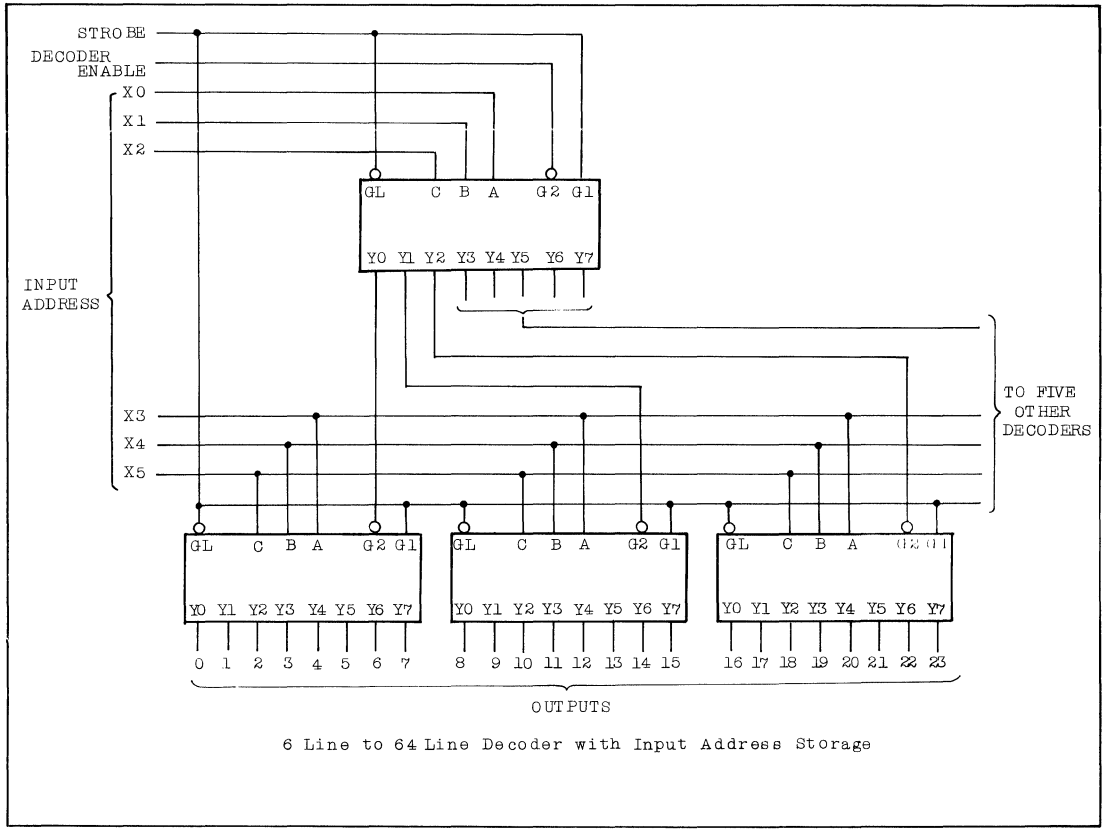


$I_{CC(Opr.)}$ TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HC238AP/AF

3-TO-8 LINE DECODER

The TC74HC238A is a high speed CMOS 3-to-8 DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled,3 Binary Select inputs(A,B and C)determine which one of the outputs(Y0-Y1)will go high.

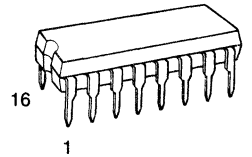
When enable input G1 is held low or either $\overline{G}$2A or $\overline{G}$2B is held high,decoding function is inhibited and all the outputs golow.

G1,$\overline{G}$2A,and $\overline{G}$2B inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

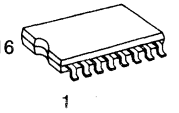
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· tpd=14ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH} =V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ···| I_{OH} |=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS238

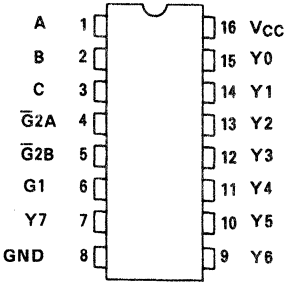


DIP16 (3D16A-P)



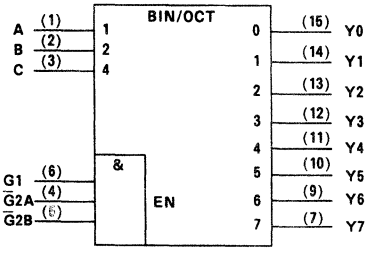
MFP16 (F16GC-P)

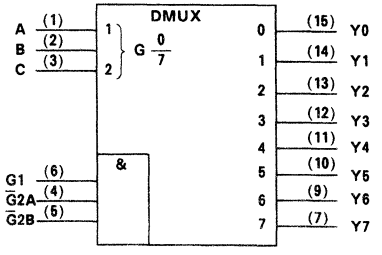
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



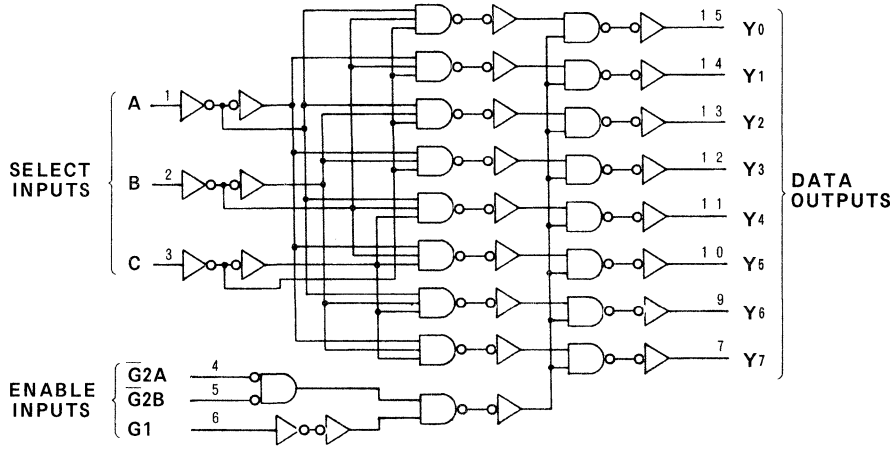


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
L	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	X	H	X	X	X	L	L	L	L	L	L	L	L	NONE
H	L	L	L	L	L	H	L	L	L	L	L	L	L	Y0
H	L	L	L	L	H	L	H	L	L	L	L	L	L	Y1
H	L	L	L	H	L	L	L	H	L	L	L	L	L	Y2
H	L	L	L	H	H	L	L	L	H	L	L	L	L	Y3
H	L	L	H	L	L	L	L	L	L	H	L	L	L	Y4
H	L	L	H	L	H	L	L	L	L	L	H	L	L	Y5
H	L	L	H	H	L	L	L	L	L	L	L	H	L	Y6
H	L	L	H	H	H	L	L	L	L	L	L	L	H	Y7

X:Don't care

SYSTEM DIAERAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C–Y)	t_{pLH} t_{pHL}		–	14	26	
Propagation Delay Time (G,$\overline{G}$–$\overline{Y}$)	t_{pLH} t_{pHL}		–	14	26	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C–Y)	t_{pLH} t_{pHL}		2.0	–	50	150	–	190	
			4.5	–	17	30	–	38	
			6.0	–	15	26	–	32	
Propagation Delay Time (G,$\overline{G}$–Y)	t_{pLH} t_{pHL}		2.0	–	50	150		190	
			4.5	–	17	30		38	
			6.0	–	15	26		32	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	53	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC240AP/AF
TC74HC241AP/AF
TC74HC244AP/AF

OCTAL BUS BUFFER

TC74HC240AP/AF	INVERTED, 3-STATE OUTPUTS
TC74HC241AP/AF	NON-INVERTED, 3-STATE OUTPUTS
TC74HC244AP/AF	NON-INVERTED, 3-STATE OUTPUTS

The TC74HC240A, 241A and 244A are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

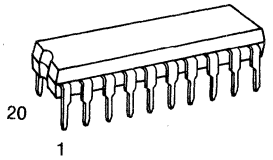
The 74HC240A is an inverting 3-state buffer having two active-low output enables. The TC74HC241A and TC74HC244A are non-inverting 3-state buffers that differ only in that the 241A has one active-high and one active-low output enable, and the 244A has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

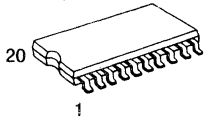
All inputs are equipped with protection circuits against static discharge or tansient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=10ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS240/241/244



DIP20 (3D20A-P)



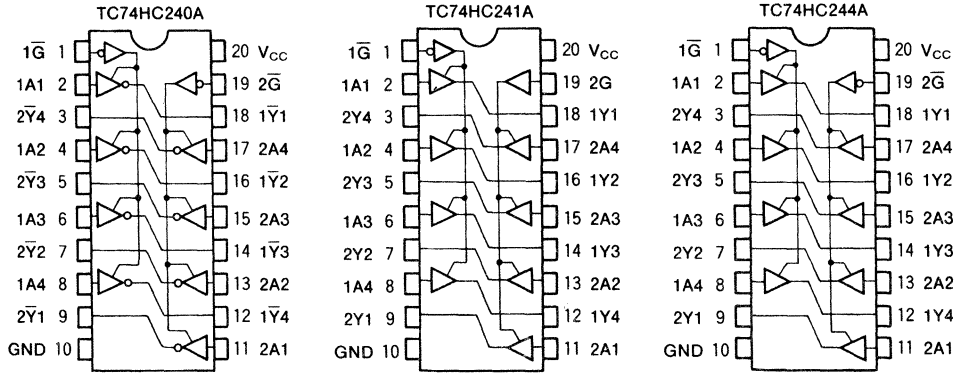
MFP20 (F20GA-P)

TRUTH TABLE

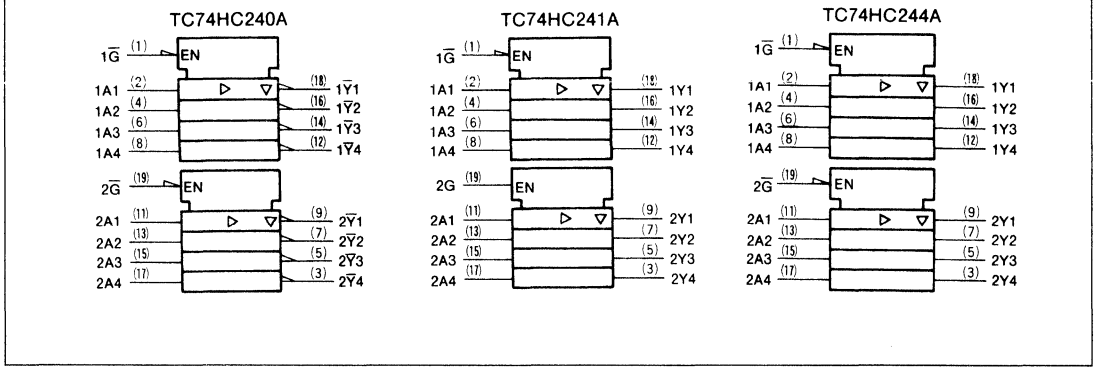
INPUTS			OUTPUTS	
$\overline{G}$	$G^{\triangle}$	A_n	Y_n	$\overline{Y}_n^{\triangle\triangle}$
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : for TC74HC241A only
△△ : for TC74HC240A only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2		
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	36	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	51	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	14	22	−	28	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	
	t_{pZH}		150	2.0	−	63	165	−	205	
				4.5	−	21	33	−	41	
				6.0	−	18	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	32	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	14	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD}(1)$	TC74HC240A			−	31	−	−	−	
		TC74HC241A/244A			−	33	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HCT240AP/AF
TC74HCT241AP/AF
TC74HCT244AP/AF

OCTAL BUS BUFFER WITH TTL INPUT LEVEL
TC74HCT240AP/AF INVERTED,3-STATE OUTPUTS
TC74HCT241AP/AF NON-INVERTED,3-STATE OUTPUTS
TC74HCT244AP/AF NON-INVERTED,3-STATE OUTPUTS

The TC74HCT240A, HCT241A and HCT244A are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C^2MOS technoligy.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

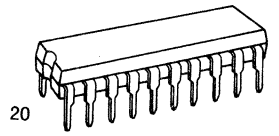
The TC74HCT240A is an inverting 3-state buffer having two active-low output enables. The TC74HCT241A and TC74HCT244A are non-inverting 3-state buffers that differ only in that the HCT241A has one active-high and one active-low output enable, and the HCT244A has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers,etc.

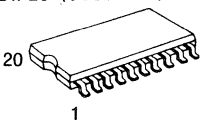
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=13ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.),V_{IH}=2.0V(Min.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS240/241/244



DIP20 (3D20A-P)



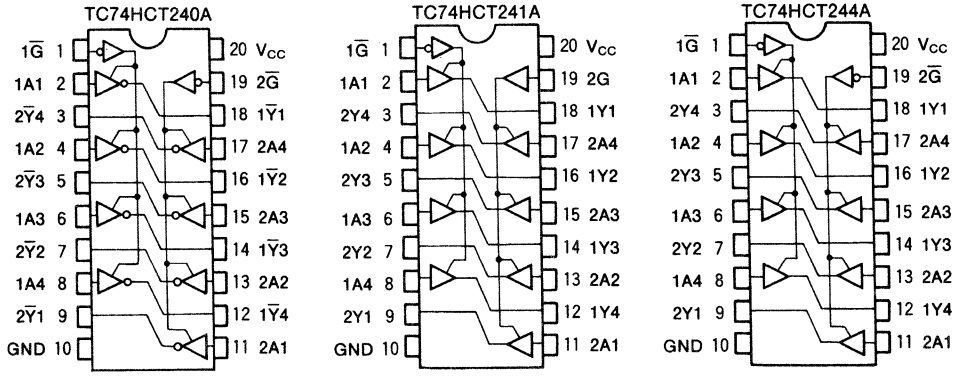
MFP20 (F20GA-P)

TRUTH TABLE

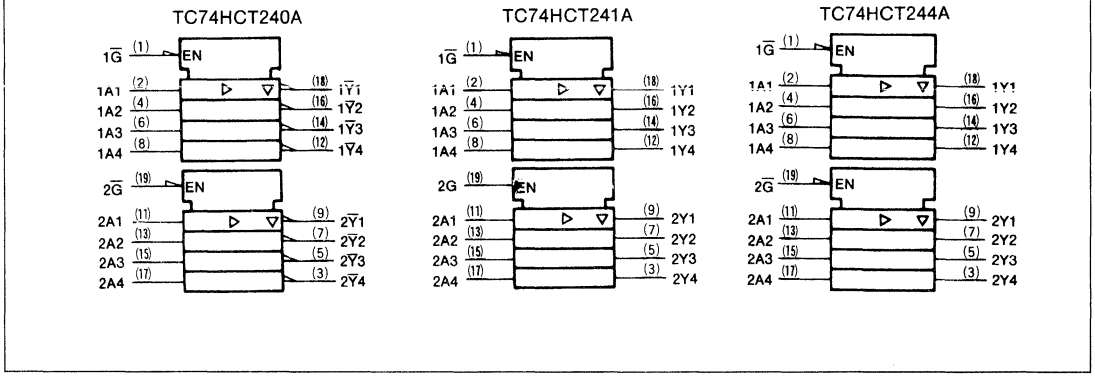
INPUTS			OUTPUTS	
$\overline{G}$	$G^{\triangle}$	A_n	Y_n	$\overline{Y}_n^{\triangle\triangle}$
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : TC74HCT241A Only
△△ : TC74HCT240A Only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ～ 5.5	V
Input Voltage	V_{IN}	0 ～ V_{CC}	V
Output Voltage	V_{OUT}	0 ～ V_{CC}	V
Operating Temperrature	T_{opr}	−40 ～ 85	℃
Input Rise and Fall Time	t_r , t_f	0 ～ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ～85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ～ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ～ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{IN}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	I_C	Per input: V_{IN} =0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time *	t_{pLH}		50	4.5	−	15	22	−	28	
				5.5	−	13	20	−	25	
	t_{pHL}		150	4.5	−	21	30	−	38	
				5.5	−	16	27	−	34	
Propagation Delay Time * *	t_{pLH}		50	4.5	−	15	25	−	31	
				5.5	−	13	22	−	28	
	t_{pHL}		150	4.5	−	21	33	−	41	
				5.5	−	18	29	−	37	
3−State Output Enable Time	t_{pZL}	$R_L=1\,k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	14	27	−	34	
	t_{pZH}		150	4.5	−	23	38	−	48	
				5.5	−	20	34	−	43	
3−State Output Disable Time	t_{pLZ}	$R_L=1\,k\Omega$	50	4.5	−	16	30	−	38	
	t_{pHZ}			5.5	−	13	27	−	34	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	A n			−	13	−	−	−	
Power Dissipation Capacitance (Note 1)	C_{PD}	*			−	33	−	−	−	
		* *			−	31	−	−	−	

Note 1 : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/8(\text{per bit})$$

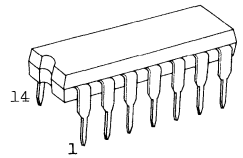
Note 2 : * =TC74HCT240A
* * =TC74HCT241A/HCT244A

TC74HC242P/F
TC74HC243P/F

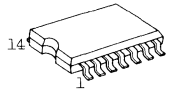
QUAD BUS TRANSCEIVER

TC74HC242P/F 3-STATE, INVERTING
TC74HC243P/F 3-STATE, NON-INVERTING

The TC74HC242 and TC74HC243 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by $\overline{GAB}$, GBA. $\overline{GAB}$ and GBA inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14(3D14A-P)



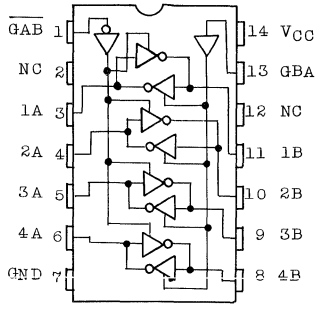
MFP14(F14GB-P)

FEATURES:

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS242/243

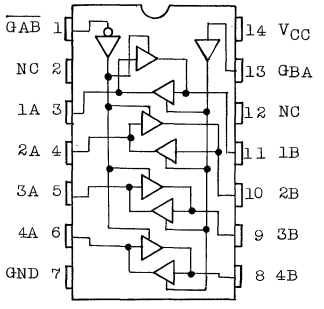
PIN ASSIGNMENT

TC74HC242



(TOP VIEW)

TC74HC243



(TOP VIEW)

NC : NO CONNECTION

TRUTH TABLE

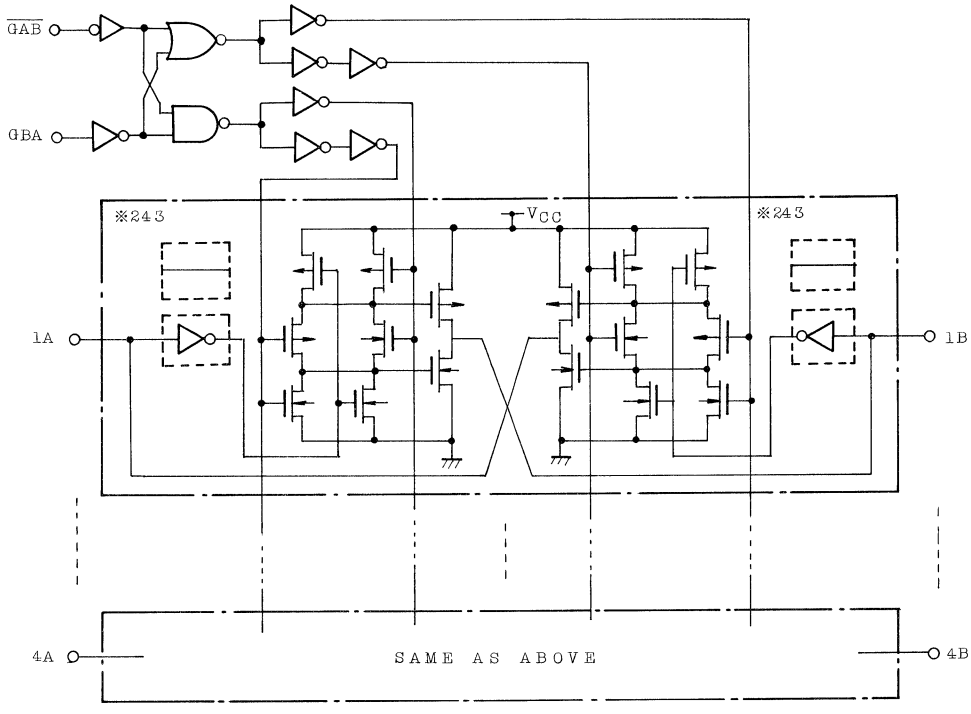
INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GBA	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	A=$\overline{B}$	A=B
L	L	INPUT	OUTPUT	B=$\overline{A}$	B=A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

Z : HIGH IMPEDANCE

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

LOGIC DIAGRAM



In case of TC74HC243, input inverters marked ※ are eliminated.

ABSOLUTE MAXIMUM RATINGS

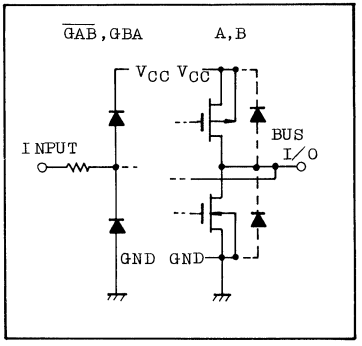
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be a applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MIN.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to $\overline{GAB}$, GBA

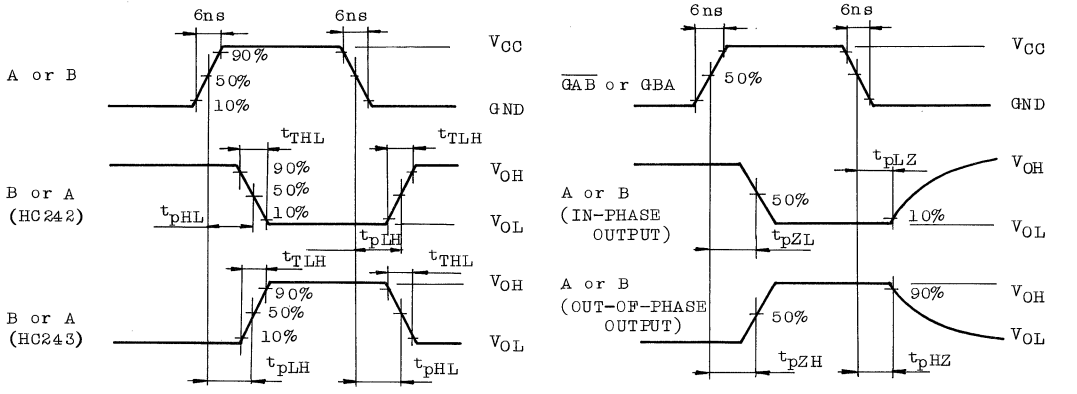
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time	t_{pLH}	TC74HC242	2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
	t_{pHL}	TC74HC243	2.0	-	44	90	-	115	
			4.5	-	12	18	-	23	
			6.0	-	10	15	-	20	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}	$\overline{GAB}$, GBA		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC242		-	42	-	-	-	
		TC74HC243		-	36	-	-	-	

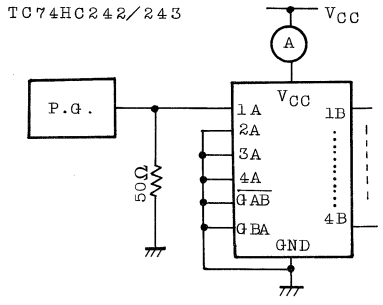
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC245AP/AF
TC74HC640AP/AF
TC74HC643AP/AF

OCTAL BUS TRANSCEIVER
TC74HC245AP/AF 3-STATE, NON-INVERTING
TC74HC640AP/AF 3-STATE, INVERTING
TC74HC643AP/AF 3-STATE, INVERTING AND NON-INVERTING

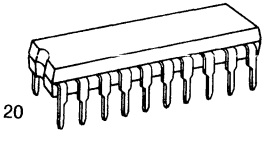
The TC74HC245A, 640A and 643A are high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

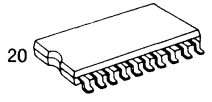
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20 (3D20A-P)



MFP20 (F20GA-P)

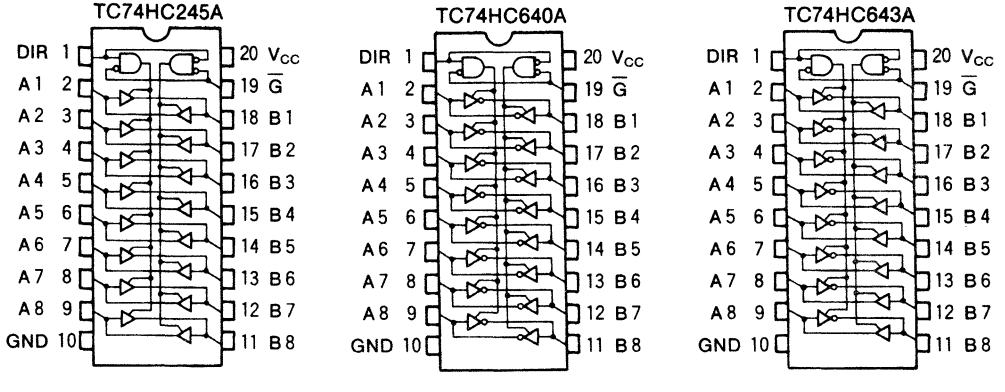
FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ····· $|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS245,640,643

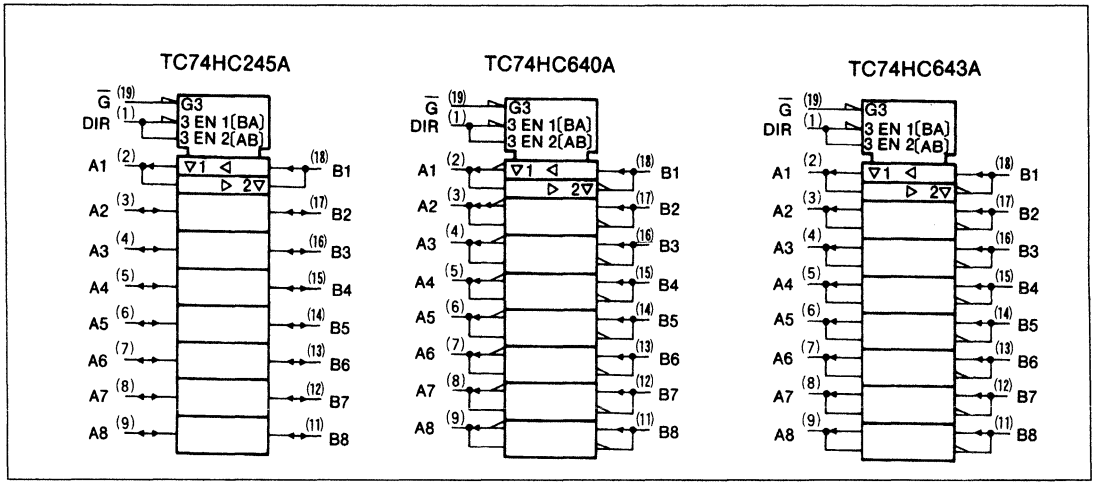
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	HC245A	HC640A	HC643A
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	33	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	48	120	−	150	
				4.5	−	16	24	−	30	
				6.0	−	14	20	−	26	
3−State Output Enable Time	t_{pZL}	R_L = 1 kΩ	50	2.0	−	48	150	−	190	
				4.5	−	16	30	−	38	
				6.0	−	14	26	−	32	
	t_{pZH}		150	2.0	−	63	180	−	225	
				4.5	−	21	36	−	45	
				6.0	−	18	31	−	38	
3−State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	−	37	150	−	190	
				4.5	−	17	30	−	38	
				6.0	−	15	26	−	32	
Input Capacitance	C_{IN}	DIR, G			−	5	10	−	10	pF
Bus Input Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC245A			−	39	−	−	−	
		TC74HC640A/643A			−	37	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TC74HCT245AP/AF
TC74HCT640AP/AF
TC74HCT643AP/AF

OCTAL BUS TRANSCEIVER
TC74HCT245AP/AF 3-STATE,NON-INVERTING
TC74HCT640AP/AF 3-STATE,INVERTING
TC74HCT643AP/AF 3-STATE,INVERTING AND NON-INVERTING

The TC74HCT245A, HCT640A and HCT643A are high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

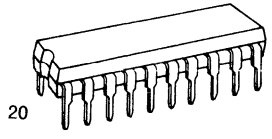
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

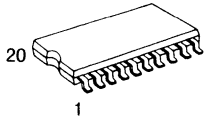
They are intended for two-way asynchronous communication between data busses. The direction of date transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20 (3D20A-P)



MFP20 (F20GA-P)

FEATURES:

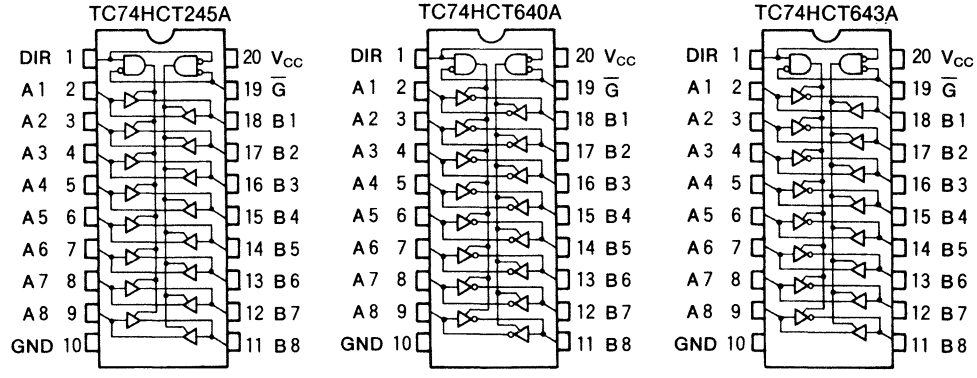
- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at TA=25°C
- Combatible with TTL outputs ····· V_{IL}=0.8V(Max.), V_{IH}=2.0(Min.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS245,640,643

APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is the output mode. Damage may result.

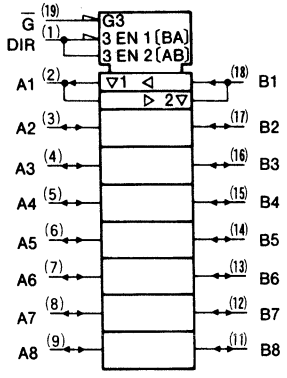
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)

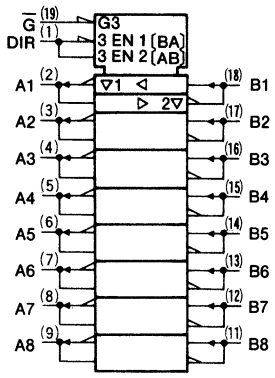


IEC LOGIC SYMBOL

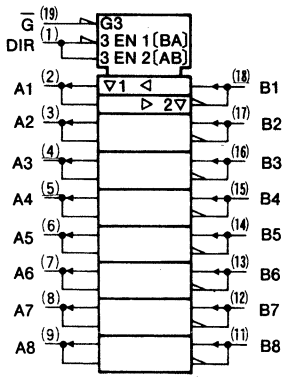
TC74HCT245A



TC74HCT640A



TC74HCT643A



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	HCT245A	HCT640A	HCT643A
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High Impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	I_C	Per input: V_{IN} =0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time	t_{pLH}		50	4.5	−	13	22	−	28	
				5.5	−	11	20	−	25	
	t_{pHL}		150	4.5	−	18	30	−	38	
				5.5	−	16	27	−	34	
3−State Output Enable Time	t_{pZL}	$R_L=1\,k\Omega$	50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
	t_{pZH}		150	4.5	−	24	38	−	48	
				5.5	−	22	34	−	43	
3−State Output Disable Time	t_{pLZ}	$R_L=1\,k\Omega$	50	4.5	−	17	30	−	38	
	t_{pHZ}			5.5	−	16	27	−	34	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT245A			−	41	−	−	−	
		TC74HCT640A/T643A			−	39	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

8-CHANNEL MULTIPLEXER (3-STATE)

The TC74HC251A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

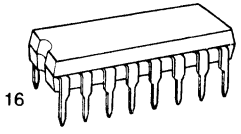
One of eight data input signals (D0–D7) is selected by decoding of the address inputs (A, B, C). The selected data appears on two output; non-inverting (Y) and inverting (W).

When the strobe input is held high, both outputs are in the high-impedance state.

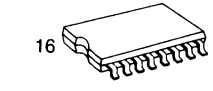
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS251

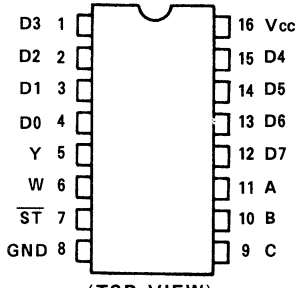


DIP16 (3D16A-P)



MFP16 (F16GC-P)

PIN ASSIGNMENT



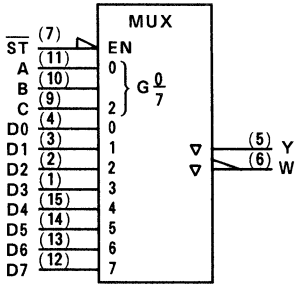
(TOP VIEW)

TRUTH TABLE

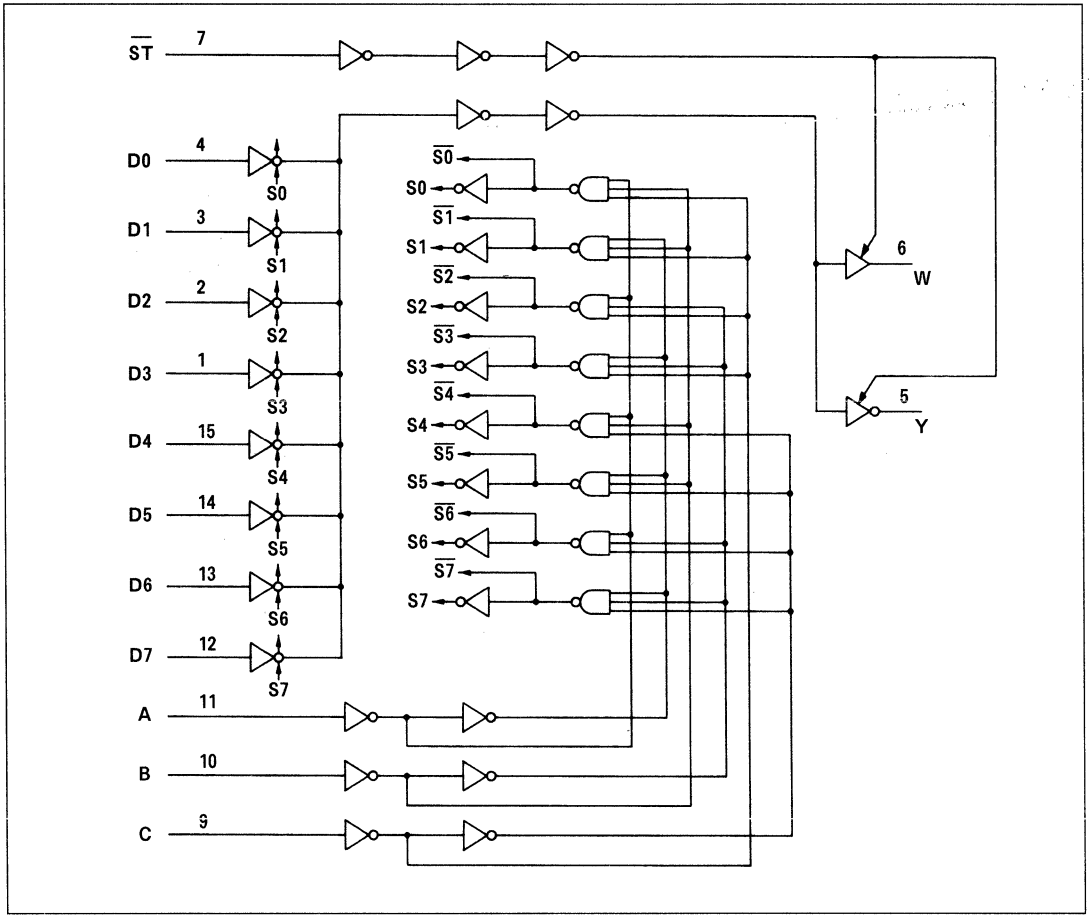
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{ST}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't care Z : High Impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Off Leak Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		–	19	31	
3–State Output Enable Time	t_{pZL} t_{pZH}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=–40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	17	28	–	35	
			6.0	–	14	24	–	30	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		2.0	–	70	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	21	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	21	
3–State Output Enable Time	t_{pZL} t_{pZH}		2.0	–	40	105	–	130	
			4.5	–	13	21	–	26	
			6.0	–	10	19	–	22	
3–State Output Disable Time	t_{pLZ} t_{pHZ}		2.0	–	25	105	–	130	
			4.5	–	13	21	–	26	
			6.0	–	11	19	–	22	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	69	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC257AP/AF/AFN
TC74HC258AP/AF

TC74HC257AP/AF/AFN 2-CHANNEL MULTIPLEXER(3-STATE)
TC74HC258AP/AF 2-CHANNEL MULTIPLEXER(3-STATE,INVERTING)

The TC74HC257A and TC74HC258A are high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technolgy.

They achive the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each is composed of four independent 2-channel multiplexers with common SELECT and OUTPUT ENABLE($\overline{OE}$).

The TC74HC257A is an inverting multiplexer, while the TC74HC258A is non-inverting.

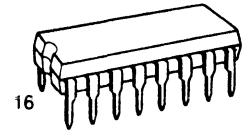
If $\overline{OE}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.

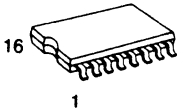
All inputs are equipped with protection citcuits against static discharge or transient excess voltage.

FEATURES:

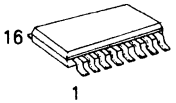
- High Speed ····· t_{pd} =10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ =28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS257/258



DIP16 (3D16A-P)



MFP 16
(F16GC-P)



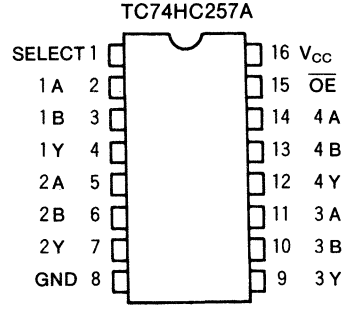
SOP 16
(SOP16-P-225A)

TRUTH TABLE

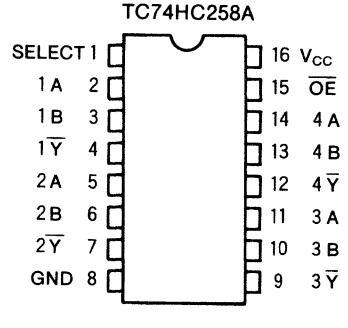
INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y(257A)	$\overline{Y}$(258A)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care
Z : High Impedance

PIN ASSIGNMENT

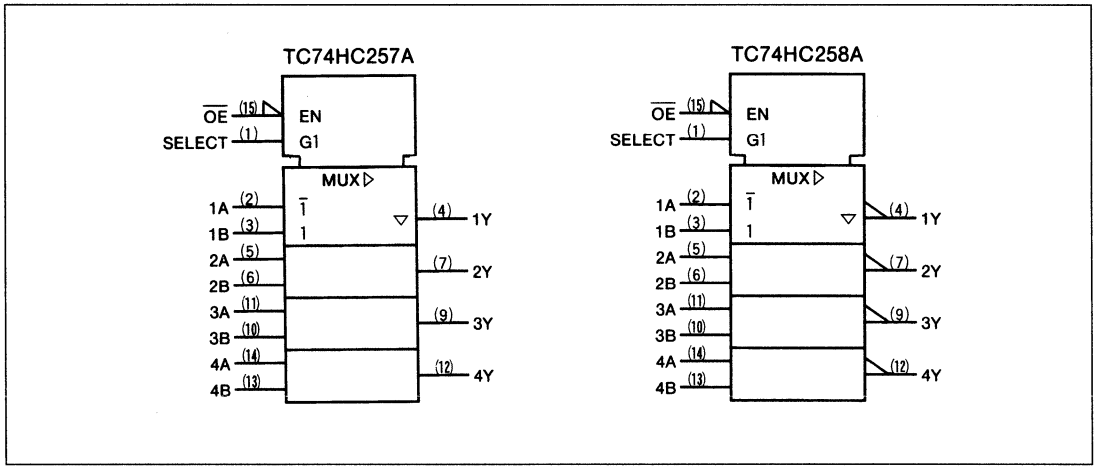


(TOP VIEW)



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6$ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (A, B−Y, $\overline{Y}$)	t_{pLH}		50	2.0	−	45	100	−	125	
				4.5	−	13	20	−	25	
				6.0	−	11	17	−	21	
	t_{pHL}		150	2.0	−	62	140	−	175	
				4.5	−	18	28	−	35	
				6.0	−	15	24	−	30	
Propagation Delay Time (SELECT−Y, $\overline{Y}$)	t_{pLH}		50	2.0	−	45	100	−	125	
				4.5	−	13	20	−	25	
				6.0	−	11	17	−	21	
	t_{pHL}		150	2.0	−	62	140	−	175	
				4.5	−	18	28	−	35	
				6.0	−	15	24	−	30	
3−State Output Enable Time	t_{pZL}	$R_L = 1\,k\Omega$	50	2.0	−	40	110	−	140	
				4.5	−	12	22	−	28	
				6.0	−	10	19	−	24	
	t_{pZH}		150	2.0	−	57	150	−	190	
				4.5	−	17	30	−	38	
				6.0	−	14	26	−	33	
3−State Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	2.0	−	28	140	−	175	
				4.5	−	14	28	−	35	
				6.0	−	13	24	−	30	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74HC257A			−	47	−	−	−	
		TC74HC258A			−	47	−	−	−	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

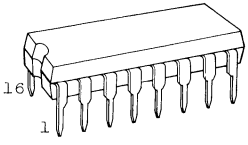
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{(per bit)}$$

TC74HC259P/F 8-BIT ADDRESSABLE LATCH

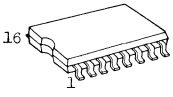
The TC74HC259 is a high speed CMOS 8-BIT ADDRESSABLE LATCH fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by A, B and C inputs. When $\overline{CLEAR}$ input is held "H" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "L" level, the data is written into the bit selected by A, B and C inputs, the other bits hold their previous conditions. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$($\overline{G}$) input held "H" level, write of all bits is inhibited regardless of A, B and C input, and their previous conditions are held. When $\overline{CLEAR}$ input is held "L" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "H" level, all bits are reset to "L" level regardless of the other inputs. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$ ($\overline{G}$) input held "L" level, all bits which isn't selected by A, B and C inputs are reset to "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS259



DIP16(3D16A-P)



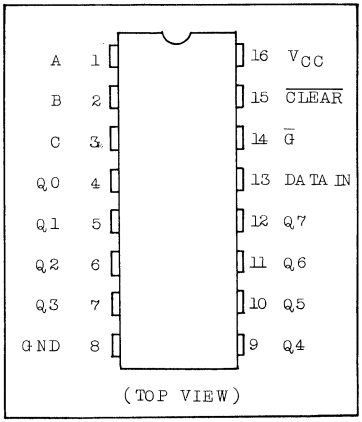
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

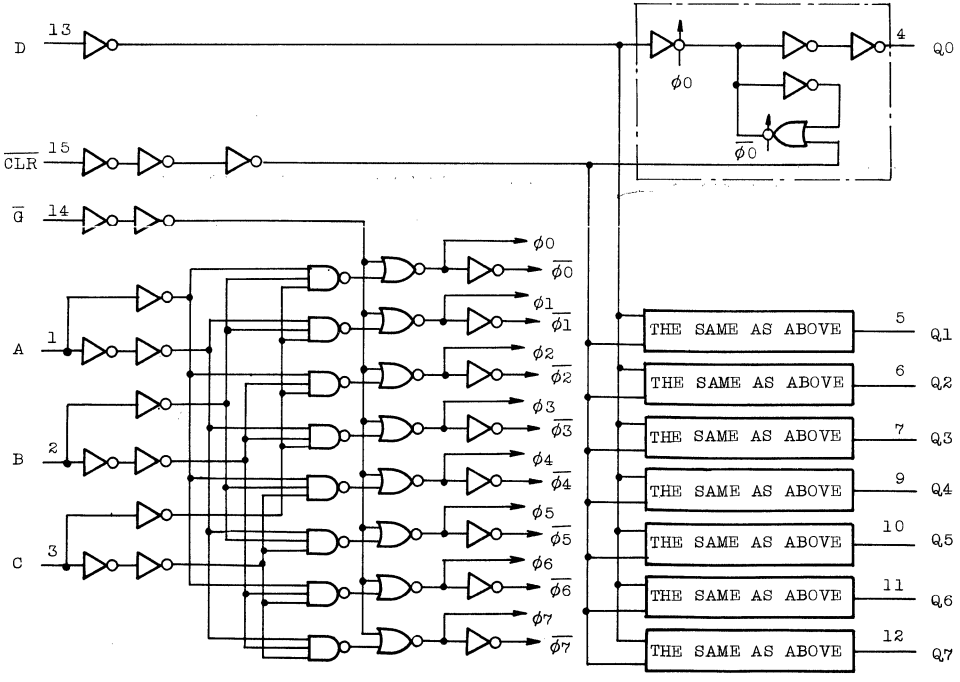
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	**Qi0**	ADDRESSABLE LATCH
H	H	Qi0	Qi0	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO "L"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : THE LEVEL AT THE DATA INPUT

Q_{i0} : THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i=0,1,·····,7).

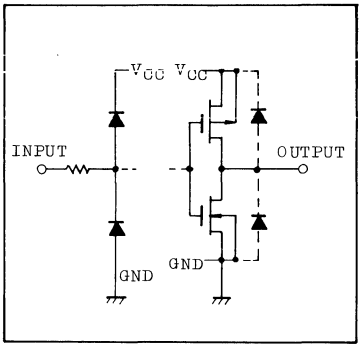
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

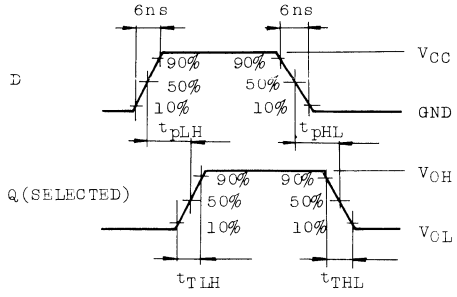
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH}		2.0	-	64	130	-	165	
	t_{pHL}		4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (A, B, C - Q)	t_{pLH}		2.0	-	96	190	-	240	
	t_{pHL}		4.5	-	24	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time ($\overline{G}$ - Q)	t_{pLH}		2.0	-	84	165	-	205	
	t_{pHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	15	23	-	29	
Minimum Pulse Width ($\overline{G}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (DATA)	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Hold Time (DATA)	t_h		2.0	-	10	25	-	30	
			4.5	-	2	5	-	6	
			6.0	-	2	5	-	5	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	32	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

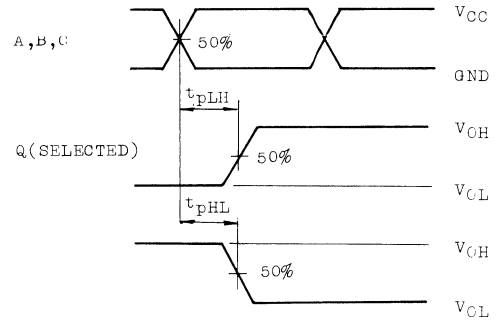
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

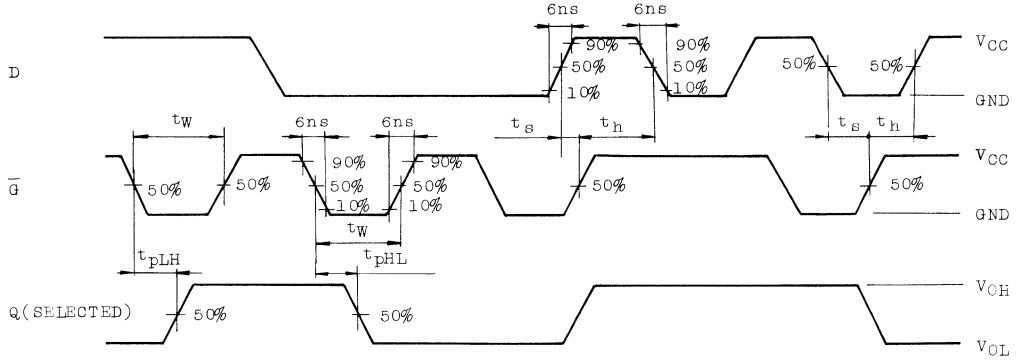
WAVEFORM 1. ($\overline{G}$=L, $\overline{CLR}$=H, A~C=STABLE)



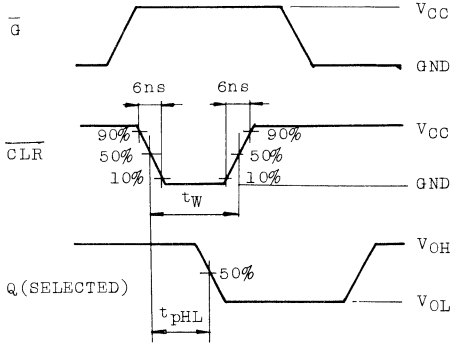
WAVEFORM 2. ($\overline{G}$=L)



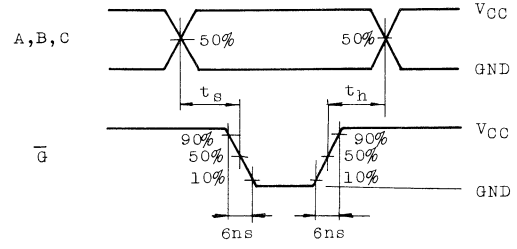
WAVEFORM 3. ($\overline{CLR}$=H, A~C=STABLE)



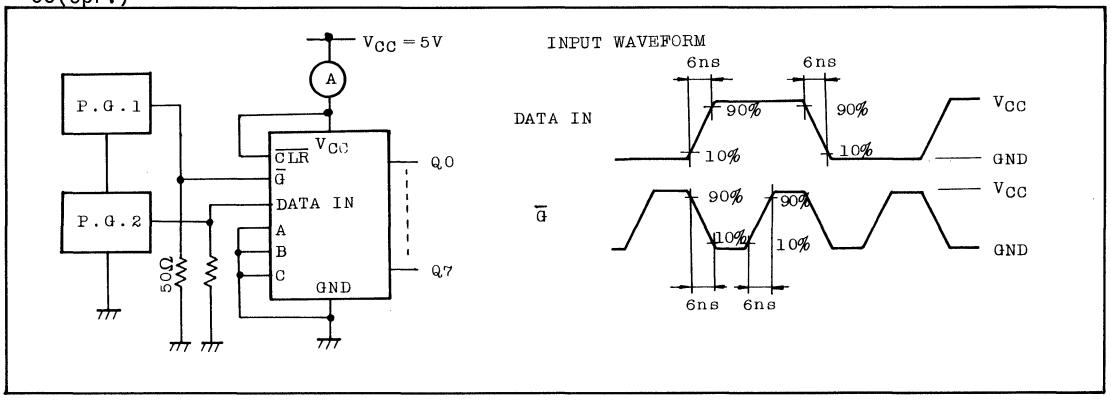
WAVEFORM 4. (D=H, A~C=STABLE)



WAVEFORM 5. ($\overline{CLR}$=H)



I_{CC}(Opr.) TEST CIRCUIT



TC74HC266AP/AF QUAD EXCLUSIVE NOR GATE (OPEN DRAIN)
TC74HC7266AP/AF QUAD EXCLUSIVE NOR GATE

The TC74HC266A/7266A are high speed CMOS QUAD EXCLUSIVE NOR GATE fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC266A has a high-performance MOS N-channel transistor (OPEN-DRAIN output).

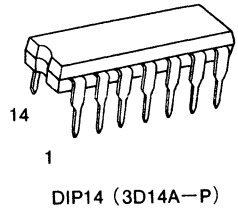
Therefore, with suitable output pullup resistors, this device can be used in wired-AND application.

The TC74HC7266A has a output buffer which is CMOS structure.

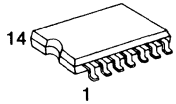
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS266

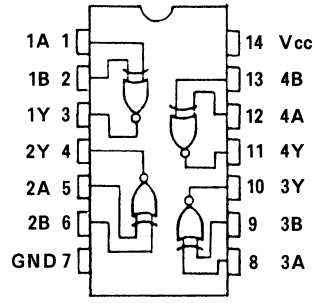


DIP14 (3D14A-P)



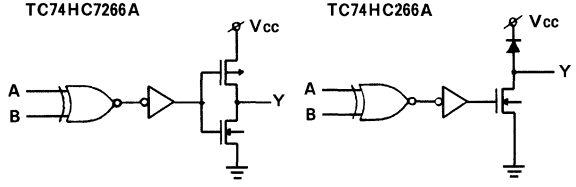
MFP14 (F14GB-P)

PIN ASSIGNMENT

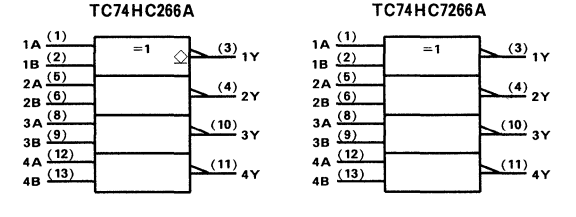


(TOP VIEW)

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y	
		7266A	266A
L	L	H	Z
L	H	L	L
H	L	L	L
H	H	H	Z

Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL} (TC74HC7266A)	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} (TC74HC266A)		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time *	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time **	t_{pLZ}	R_L=1kΩ	–	11	17	
Propagation Delay Time **	t_{pZL}	R_L=1kΩ	–	10	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time **	t_{pLZ}	R_L=1kΩ	2.0	–	26	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	11	17	–	21	
Propagation Delay Time **	t_{pZL}	R_L=1kΩ	2.0	–	40	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	3	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC266A		–	16	–	–	–	
		TC74HC7266A		–	30	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

* for TC74HC7266A only
** for TC74HC266A only

TC74HC273AP/AF

OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74HC273A is a high speed CMOS OCTAL D TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

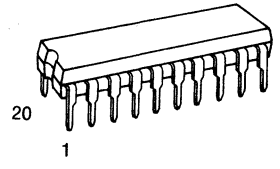
Information signals applied to D inputs are transfered to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held "L", the Q outputs are at a low logic level independent of the other inputs.

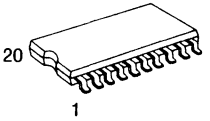
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=48MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS273

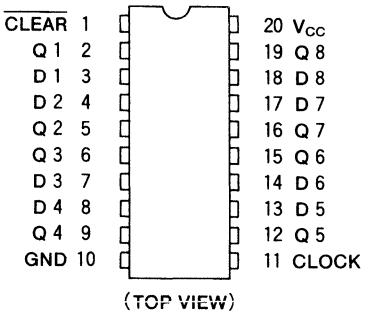


DIP20 (3D20A-P)



MFP20 (F20GA-P)

PIN ASSIGNMENT

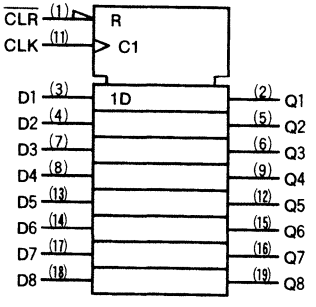


TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↓	L	—
H	H	↓	H	—
H	X	↑	Q_n	No change

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

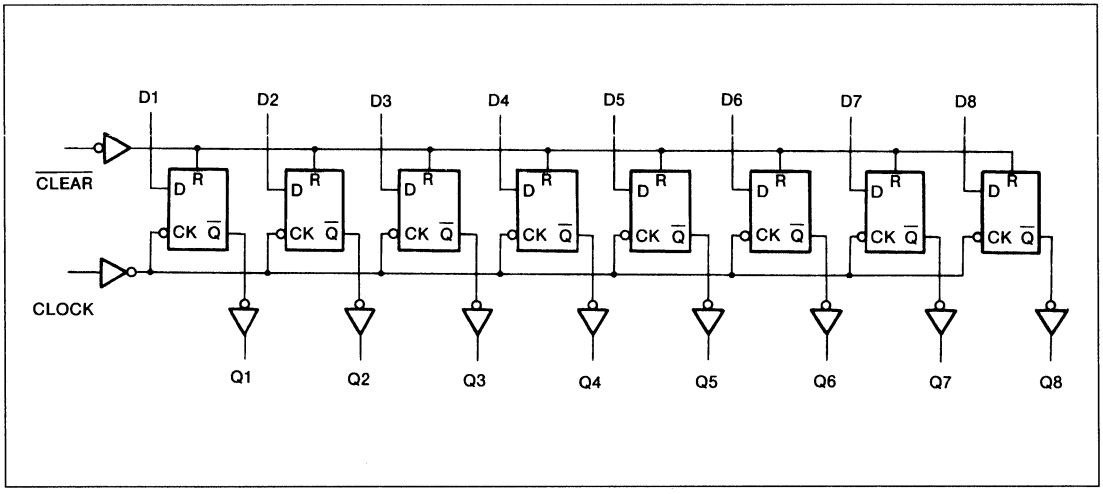
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		−	16	27	
Maximum Clock Frequency	f_{MAX}		40	67	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	54	145	−	180	
			4.5	−	18	29	−	36	
			6.0	−	15	25	−	31	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		2.0	−	60	160	−	200	
			4.5	−	20	32	−	40	
			6.0	−	17	27	−	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	30	56	−	24	−	
			6.0	35	66	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	43	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$(per Flip Flop)
And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:
$C_{PD}(total)=32+11 \cdot n$

SYSTEM DIAGRAM



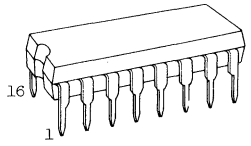
TC74HC279P/F

TC74HC279P/F QUAD S-R LATCH

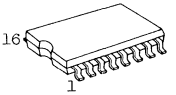
The TC74HC279 is a high speed CMOS QUAD S-R LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Each latch has an independent Q output and set and reset inputs. $\overline{S}$ and $\overline{R}$ are accomplished by "L" level. When $\overline{S}$ input is placed at "L", Q output becomes "H" and when $\overline{R}$ input is placed at "L", Q output becomes "L". When both of $\overline{S}$ and $\overline{R}$ are placed at "L", $\overline{S}$ takes precedence resulting Q="H" and when both of $\overline{S}$ and $\overline{R}$ are placed at "H", Q output doesn't change.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS279



DIP16(3D16A-P)



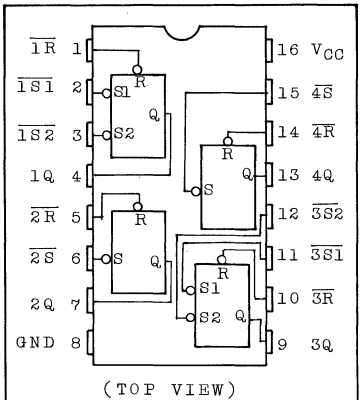
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{S}$ #	$\overline{R}$	Q
H	H	Q0
L	H	H
H	L	L
L	L	H

NOTE :

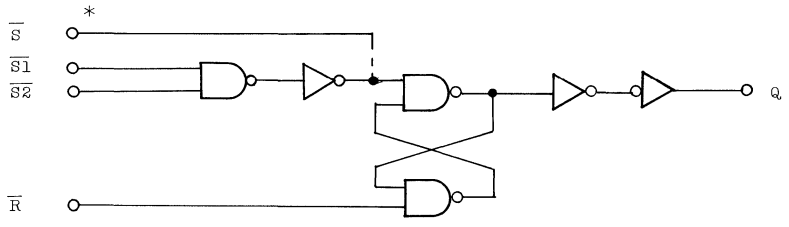
Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

\# FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:

H = BOTH $\overline{S}$ INPUTS HIGH

L = ONE OF BOTH INPUTS LOW

LOGIC DIAGRAM (Per Circuit)

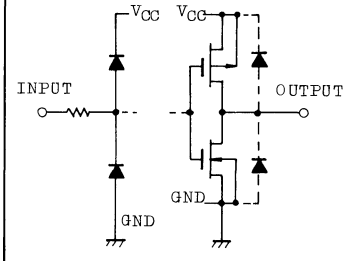


* : FOR LATCH WITH ONE $\overline{S}$ INPUT

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L-50pF, Input t_r-t_f-6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{S1}$, $\overline{S2}$ - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{S}$ - Q)	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Delay Time ($\overline{R}$ - Q)	t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	

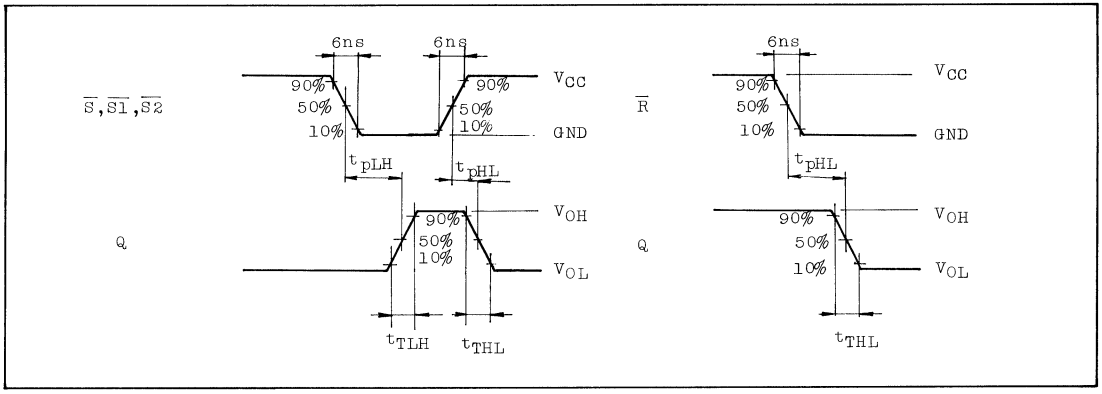
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	26	-	-	-	

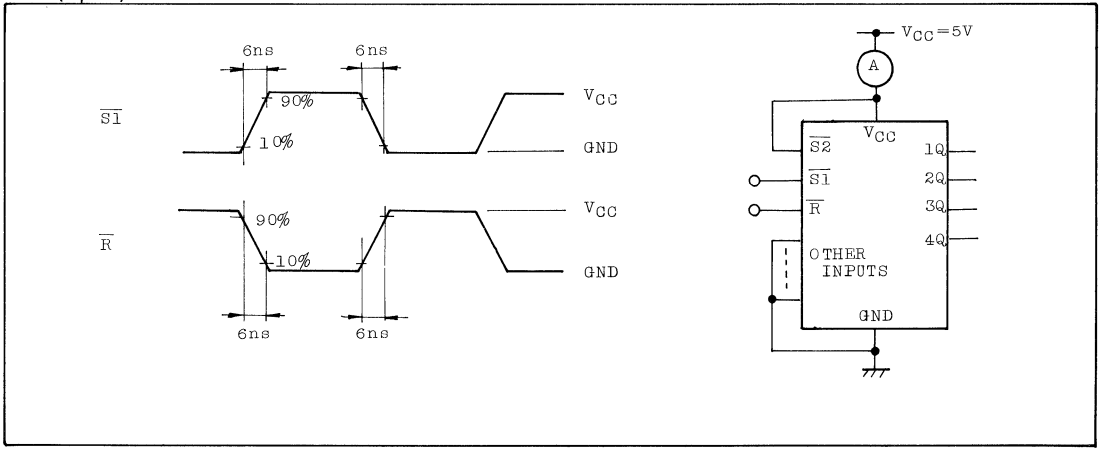
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC280AP/AF

8-CHANNEL MULTIPLEXER

The TC74HC280A is a high speed CMOS 9-BIT PARITY GENERATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC280A is composed of nine data inputs A thru I and odd/even parity outputs ΣODD and ΣEVEN.

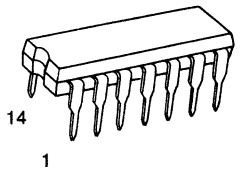
The odd parity output is high when an odd number of data inputs are high. The even parity output is high when an even number of data inputs are high.

The word-length capability is easily expanded by cascading.

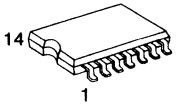
All inputs are equipped with protection circuits aainst static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS280

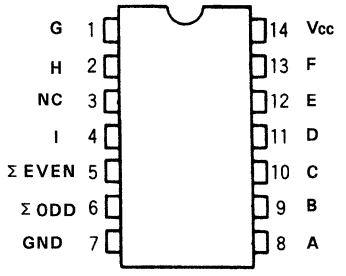


DIP14 (3D14A-P)



MFP14 (F14GB-P)

PIN ASSIGNMENT

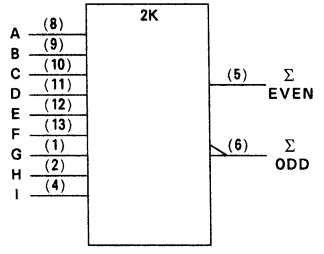


(TOP VIEW)
NC : No Connection

TRUTH TABLE

Number of inputs A through I that are High	Outputs	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	22	35	

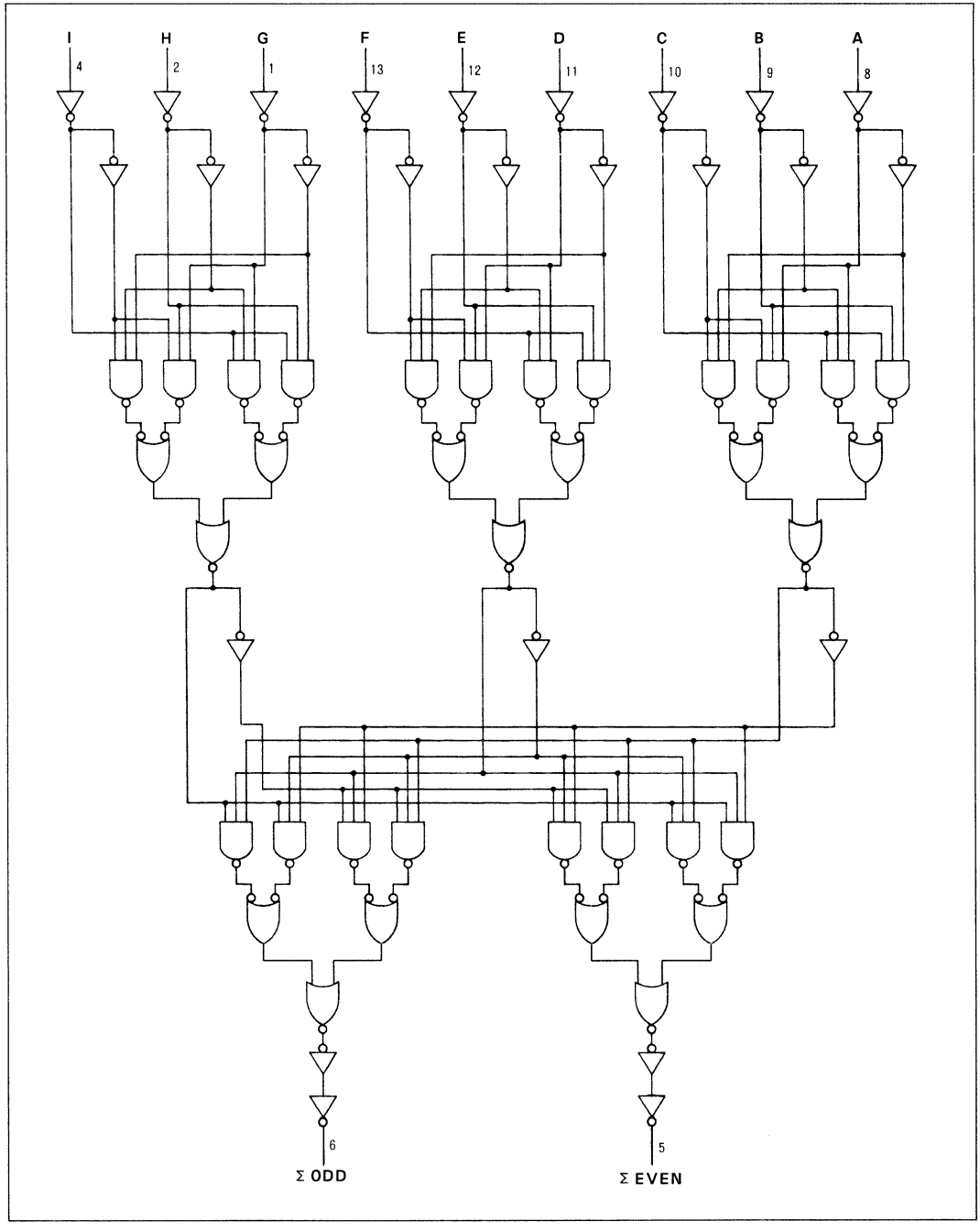
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	80	200	–	250	
			4.5	–	26	40	–	50	
			6.0	–	22	34	–	43	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	61	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SYSTEM DIAGRAM



TC74HC283AP/AF/AFN

4-BIT BINARY FULL ADDER

The TC74HC283A is a high speed CMOS 4-BIT BINARY FULL ADDER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit.

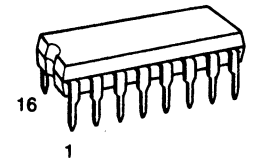
This adder features full internal look-ahead across all four bits.

A 4 × n bit binary adder is easily built up by cascading the HC283A without any additional logic.

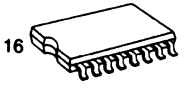
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

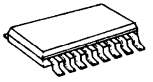
- High Speed ····· t_{pd}=17ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS283



DIP16 (3D16A-P)

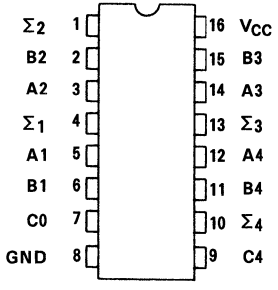


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT

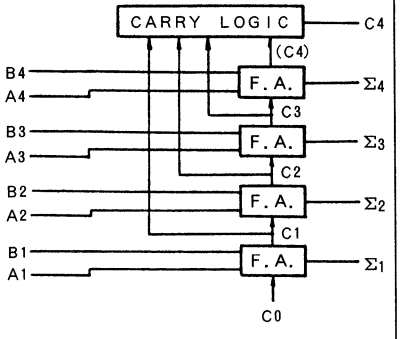


(TOP VIEW)

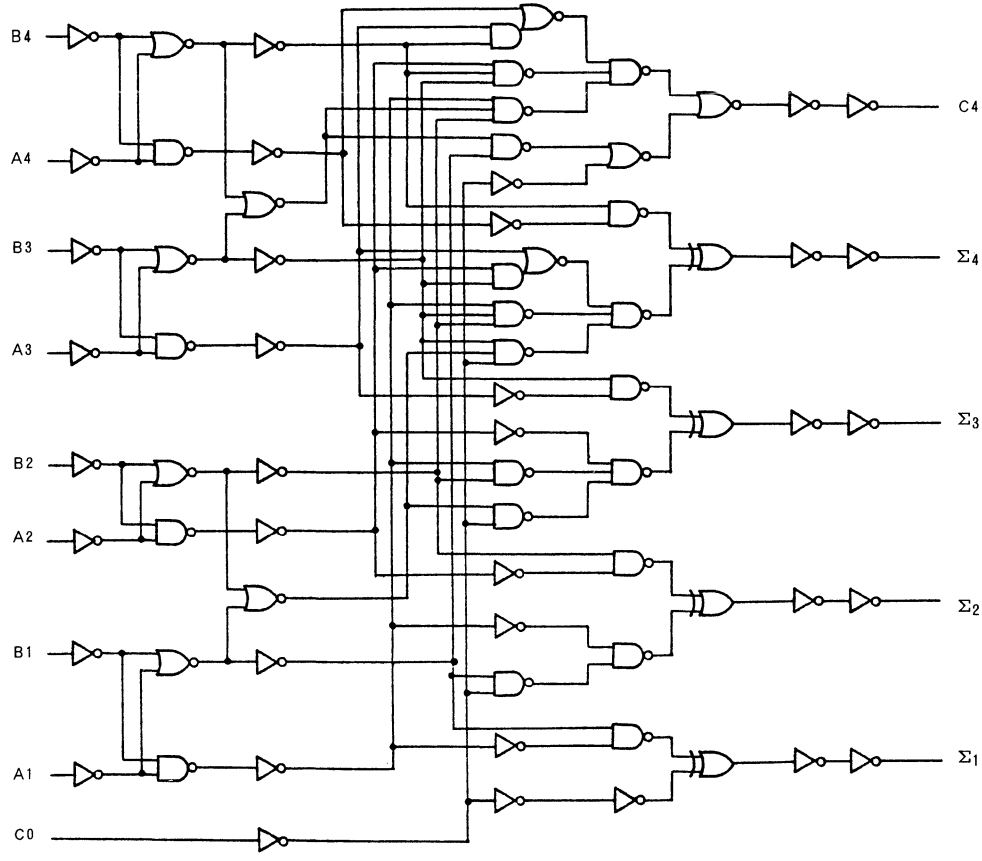
TRUTH TABLE(1 bit)

INPUTS			OUTPUTS	
Bn	An	cn-1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

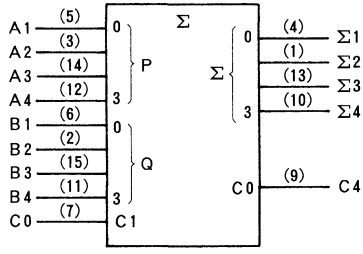
BLOCK DIAGRAM



SYSTEM DIAGRAM



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($C_0 - \sum n$)	t_{pLH} t_{pHL}		–	17	26	
Propagation Delay Time ($C_0 - C_4$)	t_{pLH} t_{pHL}		–	17	26	
Propagation Delay Time (An,Bn$-\sum n$)	t_{pLH} t_{pHL}		–	23	37	
Propagation Delay Time (An,Bn$-C_4$)	t_{pLH} t_{pHL}		–	21	34	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($C_0 - \sum n$)	t_{pLH} t_{pHL}		2.0	–	60	150	–	190	
			4.5	–	20	30	–	38	
			6.0	–	17	26	–	32	
Propagation Delay Time ($C_0 - C_4$)	t_{pLH} t_{pHL}		2.0	–	60	150	–	190	
			4.5	–	20	30	–	38	
			6.0	–	17	26	–	32	
Propagation Delay Time (An,Bn$-\sum n$)	t_{pLH} t_{pHL}		2.0	–	95	210	–	265	
			4.5	–	27	42	–	53	
			6.0	–	22	36	–	45	
Propagation Delay Time (An,Bn$-C_4$)	t_{pLH} t_{pHL}		2.0	–	80	195	–	245	
			4.5	–	25	39	–	49	
			6.0	–	20	33	–	42	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	126	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC298AP/AF

QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

The TC74HC298A is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

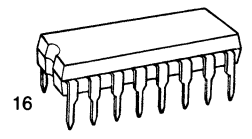
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains a 4-bit 2-channel multiplexer and a 4-bit output register. When the word select input (W.S.) is held low, the data of word 1(A1, B1, C1, D1) is selected and is applied to the registers. When W.S. is held high, the data of word 2 (A2, B2, C2, D2) will be applied to the registers. This selected data is transfered to the output (QA, QB, QC, QD) on the negative going transition of $\overline{CLOCK}$.

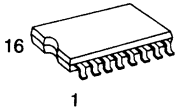
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=73MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS298

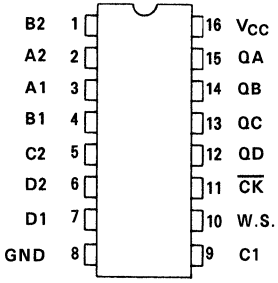


DIP16 (3D16A-P)



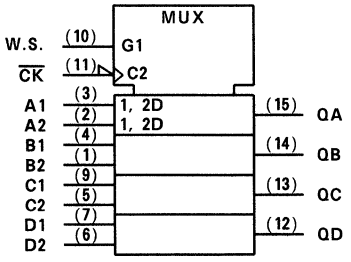
MFP16 (F16GC-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

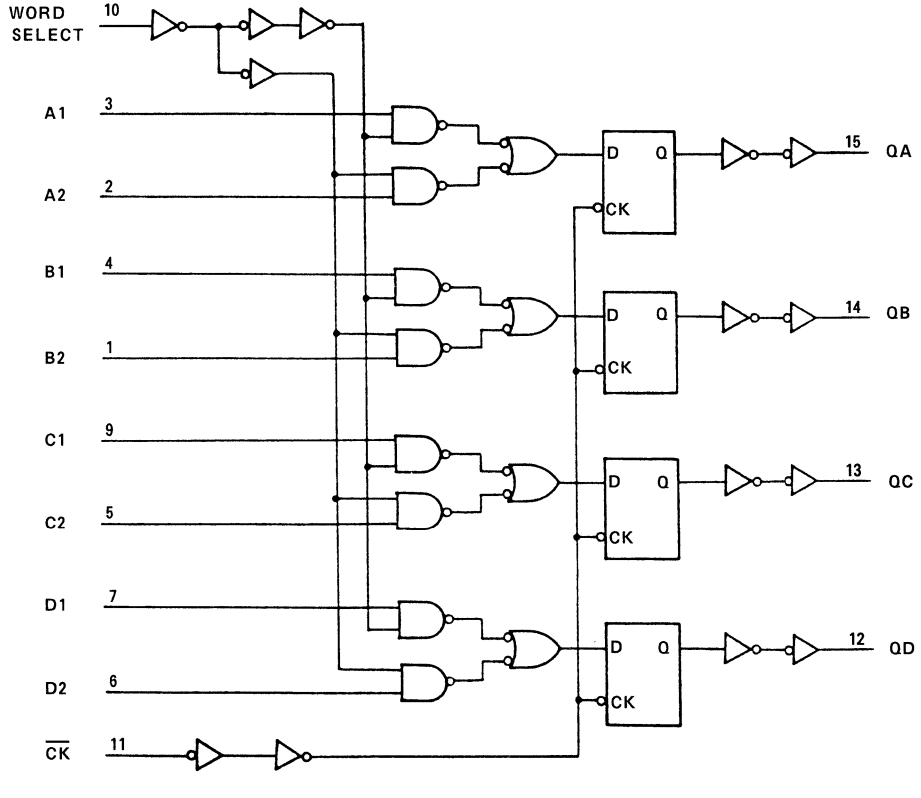


TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CK}$	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QD0	QD0

X : Don't care (Including transition)
a1, a2····· : The Level of steady-state Input at A1, A2, etc.
QA0, QB0··· : The level of QA, QB, etc. entered on the most recent negative transition of the clock input.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C, D)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (W. S.)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (A, B, C, D)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time (W. S.)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	35	27	
			6.0	−	41	33	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		−	12	21	
Maximum Clock Frequency	f_{MAX}		38	73	−	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		2.0	−	45	125	−	155	
			4.5	−	15	25	−	31	
			6.0	−	13	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	7	22	−	6	−	
			4.5	35	67	−	28	−	
			6.0	41	79	−	33	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

And the total C_{PD} when n−bits operate can be gained by the following equation:

$$C_{PD}\text{ (total)}=27+12 \cdot n$$

TC74HC299AP/AF
TC74HC323AP/AF

TC74HC299AP/AF 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
TC74HC323AP/AF 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

The TC74HC299A and TC74HC323A are high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

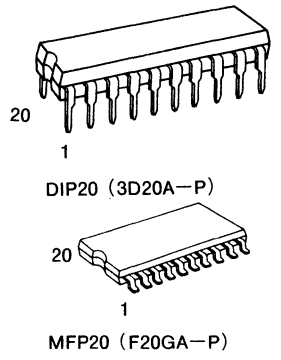
They have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. Clear function on the TC74HC299A is asynchronous to CLOCK, while the TC74HC323A is cleared synchronous to CLOCK.

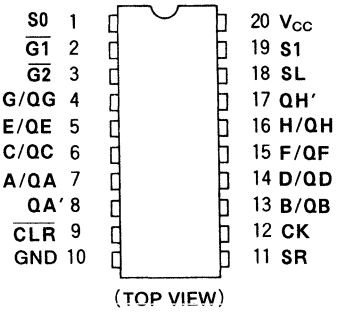
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

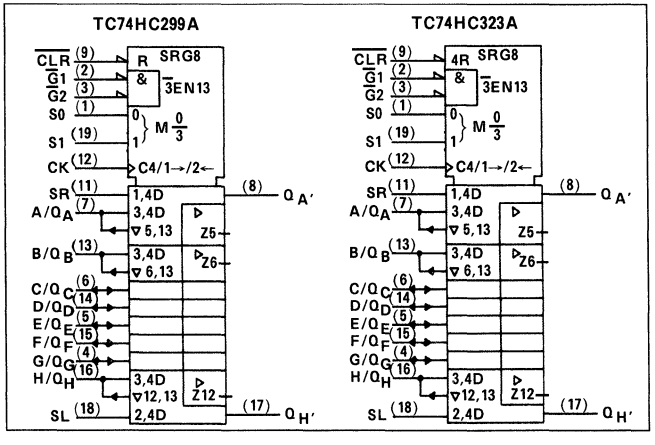
- High Speed ····· f_{MAX}=42MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For QA',QH'
- Symmetrical Output Impedance ···
  $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QA', QH'
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS299/323



PIN ASSIGNMENT



IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

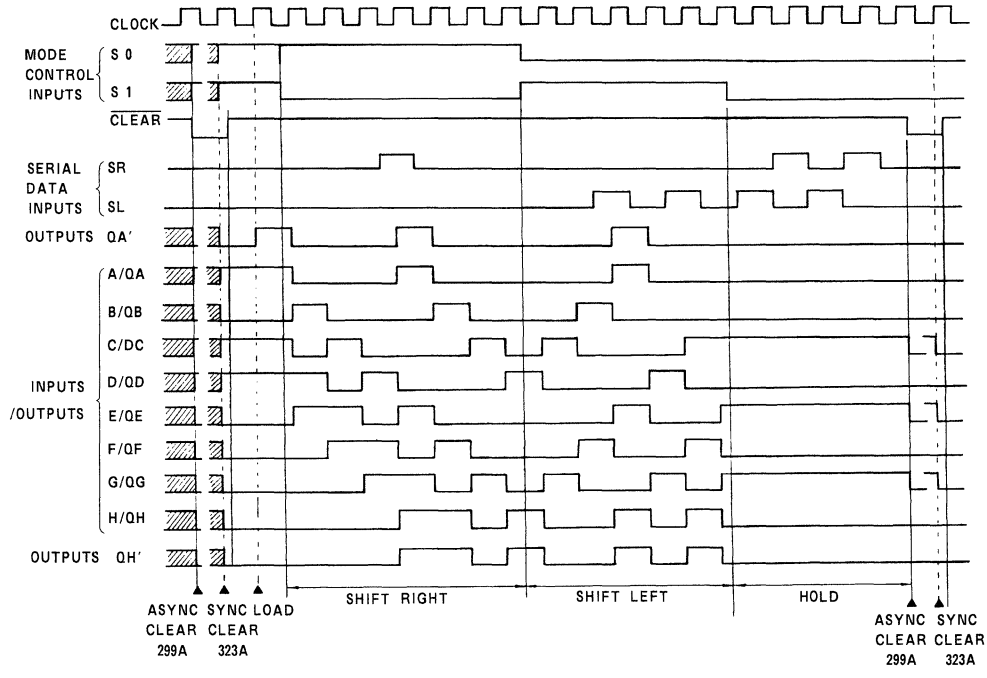
TRUTH TABLE

MODE	INPUTS										INPUTS/OUTPUTS		OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CK		SERIAL			A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *	(299A)	(323A)	SL	SR					
Z	L	H	H	X	X	X	X	X	X		Z	Z	L	L
CLEAR	L	L	X	L	L	X	↓	X	X		L	L	L	L
	L	X	L	L	L	X	↓	X	X		L	L	L	L
HOLD	H	L	L	L	L	X	X	X	X		QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓		X	H		H	QGn	H	QGn
	H	L	H	L	L	↓		X	L		L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓		H	X		QBn	H	QBn	H
	H	H	L	L	L	↓		L	X		QBn	I	QBn	L
LOAD	H	H	H	X	X	↓		X	X		a	h	a	h

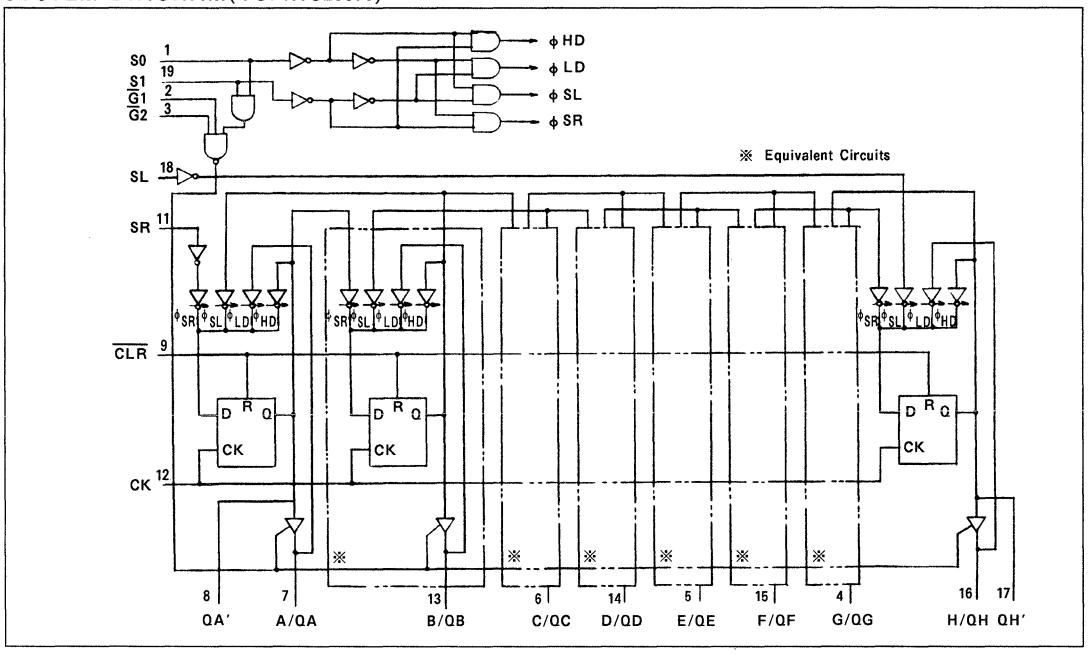
* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z :High Impedance
Qn0:The level of An before the indicated steady-state input conditions were established.
Qnn:The level of Qn before the most recent active transition indicated by ↓ or ↑.
a,h :The level of the steady-state inputs A, H, respectively.
X :Don't care

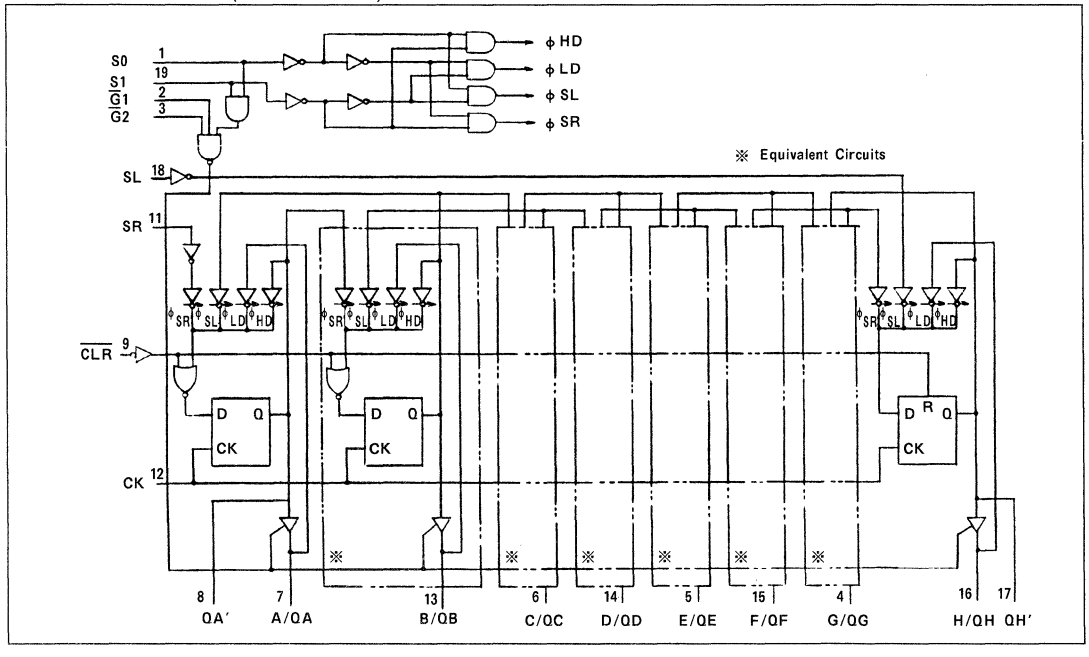
TIMING CHART



SYSTEM DIAGRAM(TC74HC299A)



SYSTEM DIAGRAM(TC74HC323A)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (Q_H') / ($Q_A \sim Q_H$)	I_{OUT}	± 25 / ± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		Q_A', Q_H'	I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
		$Q_A \sim Q_H$	I_{OH} = −6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		Q_A', Q_H'	I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
		$Q_A \sim Q_H$	I_{OL} = 6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING RECOMMENDED OPERATING CONDITIONS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ～85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SL,SR,A～H)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (S0,S1)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time ($\overline{CLR}$)**	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (SL,SR,A～H)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (S0,S1)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time ($\overline{CLR}$)**	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	8	10	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

Note :* TC74HC299A only
** TC74HC323A only

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (QA',QH')	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CK−QA',QH')	t_{pLH} t_{pHL}		−	19	30	
Propagation Delay Time ($\overline{CLR}$−QA',QH')	t_{pLH} t_{pHL}		−	17	30	
Maximum Clock Frequency	f_{MAX}		35	73	−	MHz

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Output Transition Time (QA～QH)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (QA',QH')	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CK−QA'QH')	t_{pLH} t_{pHL}		50	2.0	−	85	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	18	29	−	37	
Propagation Delay Time ($\overline{CLR}$−QA',QH')**	t_{pHL}		50	2.0	−	85	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	18	30	−	37	
Propagation Delay Time (CK−QA～QH)	t_{pLH} t_{pHL}		50	2.0	−	80	160	−	20	
				4.5	−	21	32	−	40	
				6.0	−	17	27	−	34	
			150	2.0	−	100	200	−	250	
				4.5	−	26	40	−	50	
				6.0	−	21	34	−	43	
Propagation Delay Time ($\overline{CLR}$−QA～QH)**	t_{pHL}		50	2.0	−	85	190	−	240	
				4.5	−	24	38	−	48	
				6.0	−	18	30	−	38	
			150	2.0	−	105	230	−	90	
				4.5	−	29	46	−	58	
				6.0	−	22	36	−	46	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	60	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	13	22	−	28	
			150	2.0	−	78	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	17	29	−	36	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	54	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	33	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	12	−	5	−	MHz
				4.5	30	58	−	24	−	
				6.0	35	80	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	$C_{PD}(1)$				−	170	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

* TC74HC299A only

** TC74HC323A only

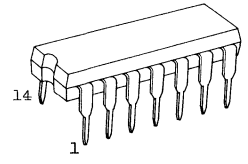
TC74HC354P/F

TC74HC354P/F 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

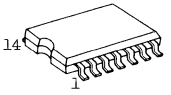
The TC74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC354 is similar in function to TC74HC356, which has a 8-bit flip-flop as the data registers instead of 8-bit latch. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=33ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS354



DIP14(3D14A-P)



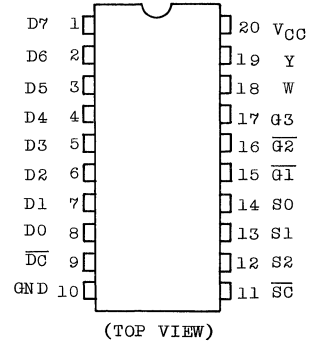
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	$\overline{DC}$	G1	G2	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z : HIGH IMPEDANCE

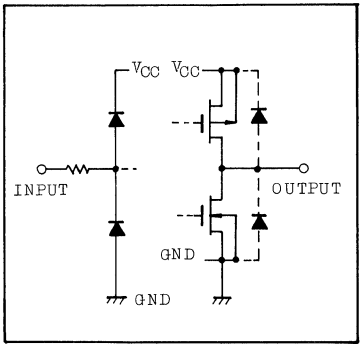
D0n·····D7n : THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7 ,RESPECTIVELY, BEFORE THE MOST RECENT LOW-TO-HIGH TRANSITION OF DATA CONTROL.

: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW.

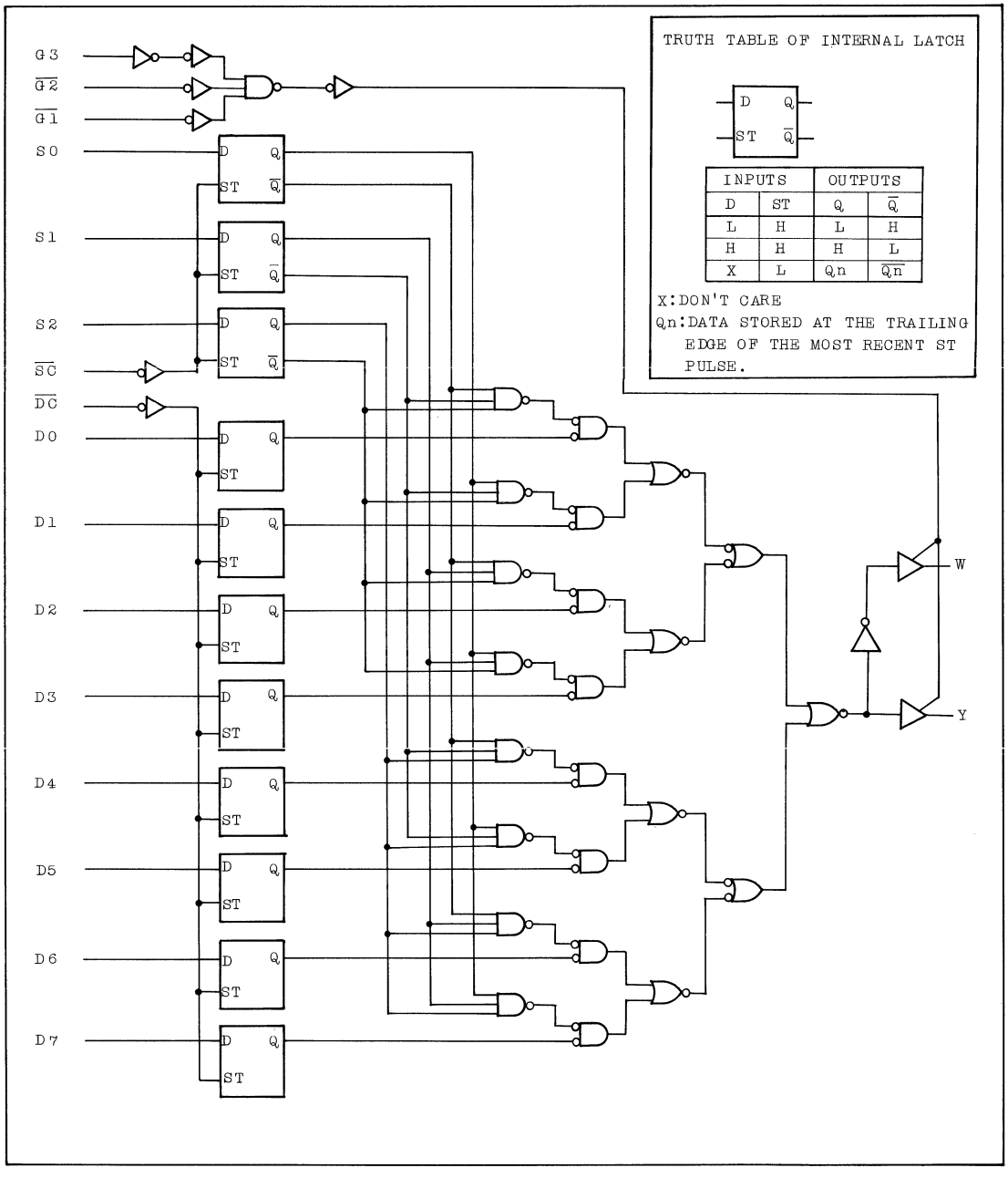
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-7.8mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=7.8mA$	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (Dn - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time ($\overline{DC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	

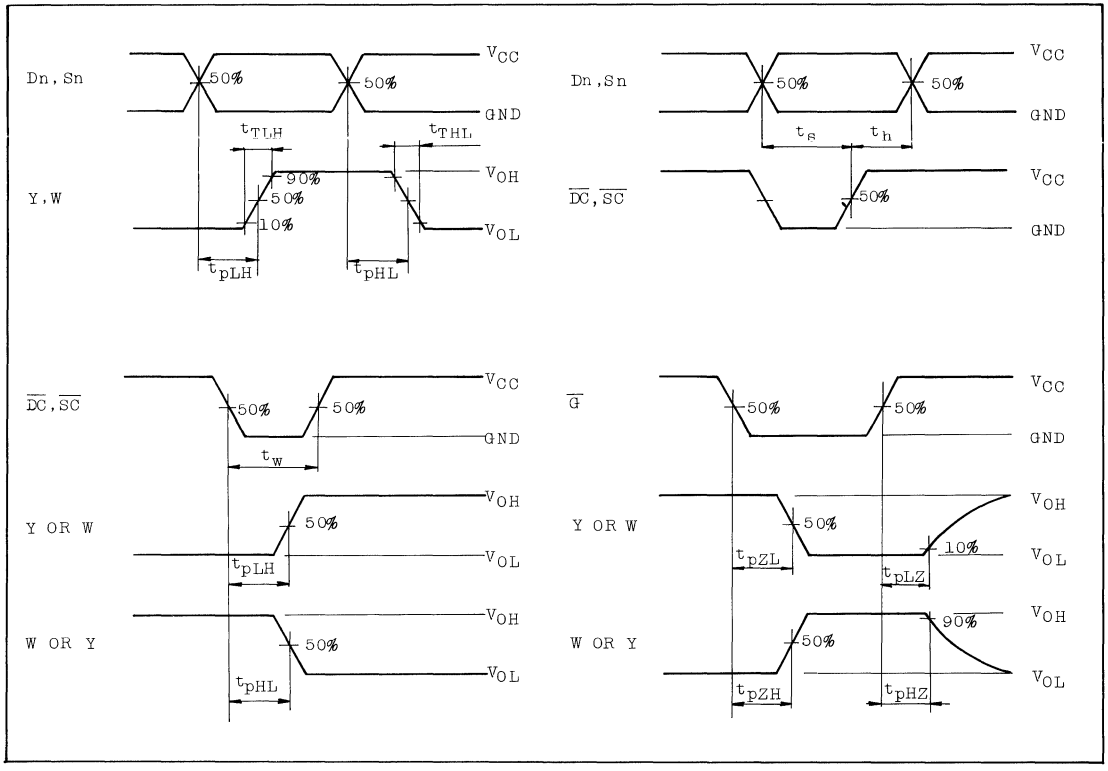
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time (Sn - Y, W)	t_{pLH} t_{pHL}		2.0	-	152	285	-	355	nS
			4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	156	295	-	370	
			4.5	-	39	59	-	74	
			6.0	-	33	50	-	63	
Minimum Pulse Width ($\overline{DC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	84	-	-	-	

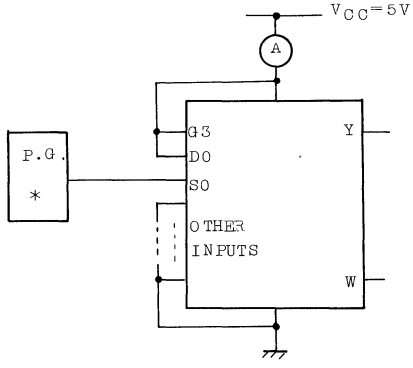
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



ICC(opr.) TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC356P/F

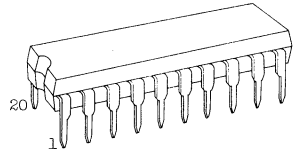
TC74HC356P/F 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

GENERAL DESCRIPTION

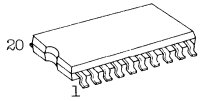
The TC74HC356 is high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC356 is similar in function to TC74HC354, which has a 8-bit latch as the data register instead of 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=29ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Ouptut Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS356



DIP20(3D20A-P)



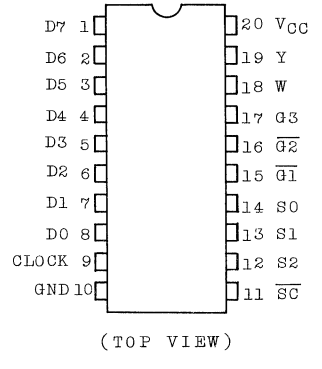
MFP20(F20GA-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	CLOCK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z: HIGH IMPEDANCE

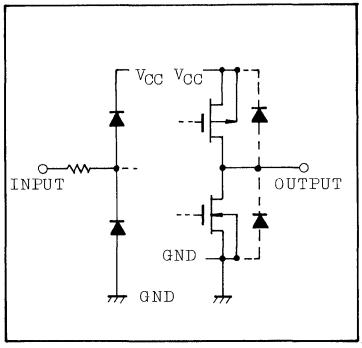
D0 ····· D7: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, AT THE TIME OF THE LOW-TO-HIGH TRANSITION OF CLOCK.

#: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH SC LOW.

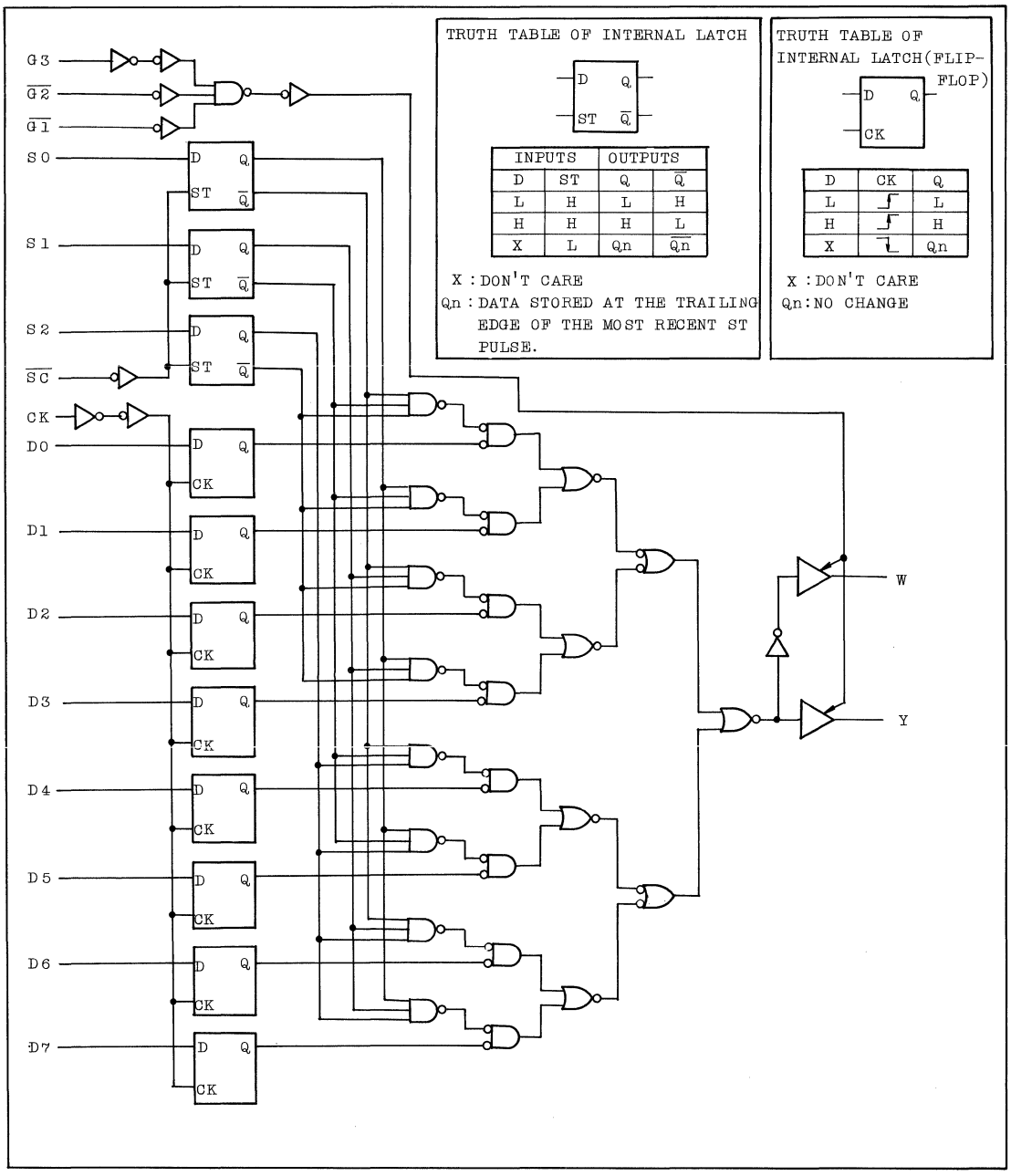
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE
Qn : DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE OF INTERNAL LATCH(FLIP-FLOP)

D	CK	Q
L	↑	L
H	↑	H
X	↓	Qn

X : DON'T CARE
Qn : NO CHANGE

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Ouptut Transition Time	t_{TLH}		2.0	-	25	60	-	75	
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (CLOCK - Y, W)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (Sn - Y, W)	t_{pLH}		2.0	-	152	285	-	355	
	t_{pHL}		4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	

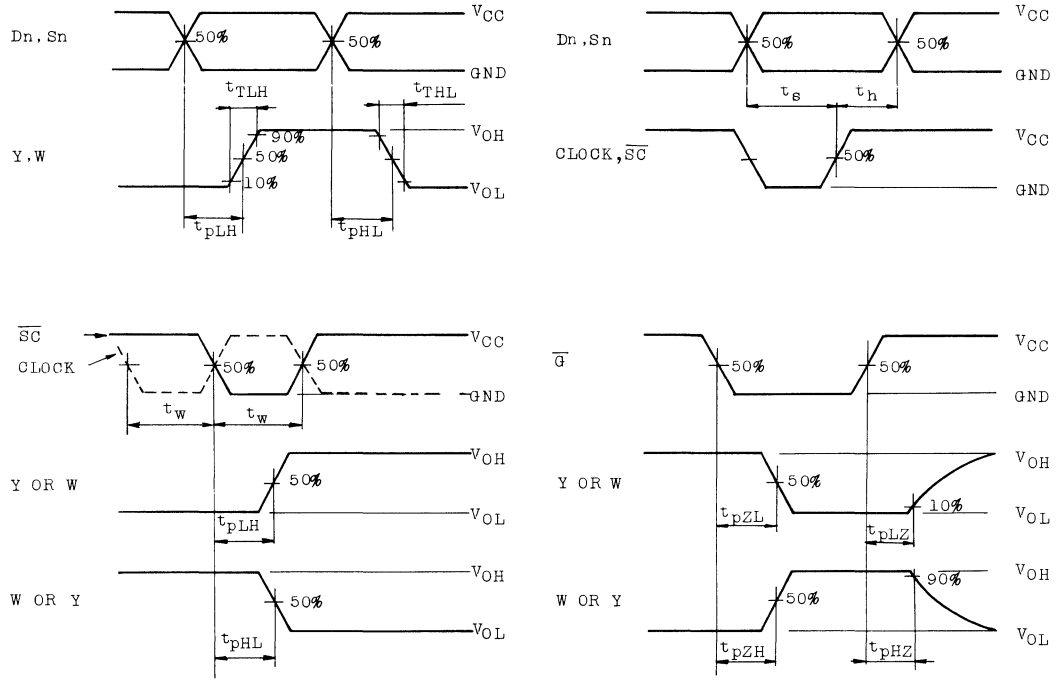
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	156	295	-	370	ns
			4.5	-	39	59	-	74	
			6.0	-	33	50	-	63	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	53	-	-	-	

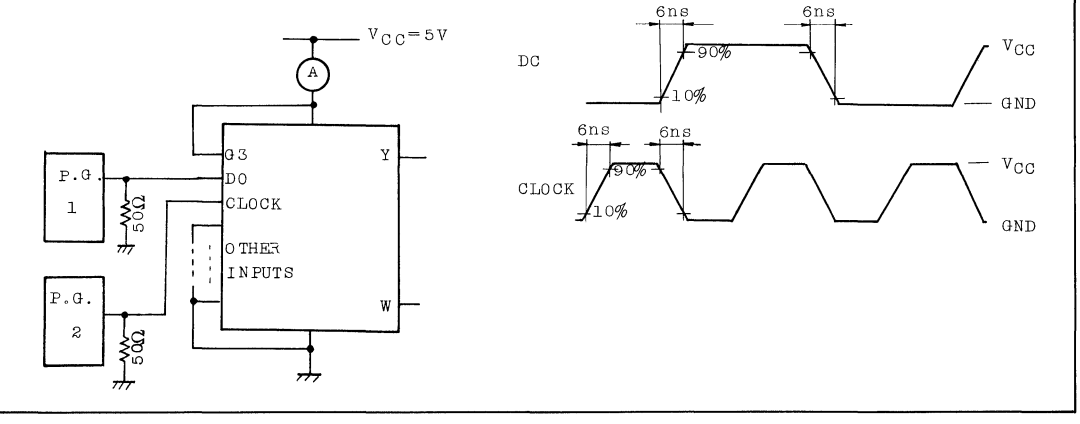
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT, WAVEFORM



TC74HC365P/F
TC74HC366P/F

HEX BUS BUFFER
TC74HC365P/F NON-INVERTING
TC74HC366P/F INVERTING

The TC74HC365 and TC74HC366 are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.

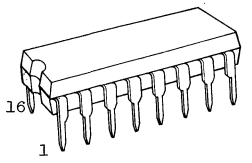
These devices achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$); all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, and at the other conditions these output are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366).

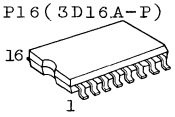
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS365/366

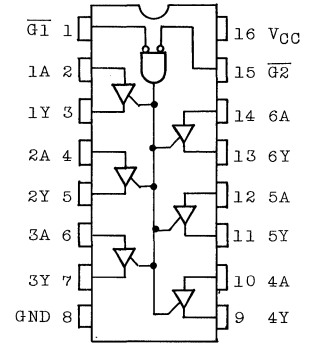


DIP16(3D16A-P)

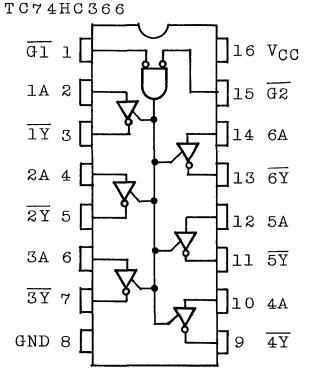


MFP16(F16GC-P)

PIN ASSIGNMENT



(TOP VIEW)



(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn(365)	$\overline{Yn}$(366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X : DON'T CARE
Z : HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

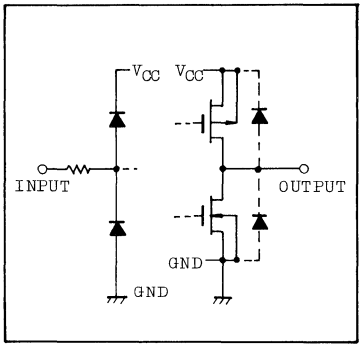
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time **	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	96	175	-	220	
			4.5	-	24	35	-	44	
			6.0	-	20	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

AC ELECTRICAL CHARACTERISTICS (Continued)

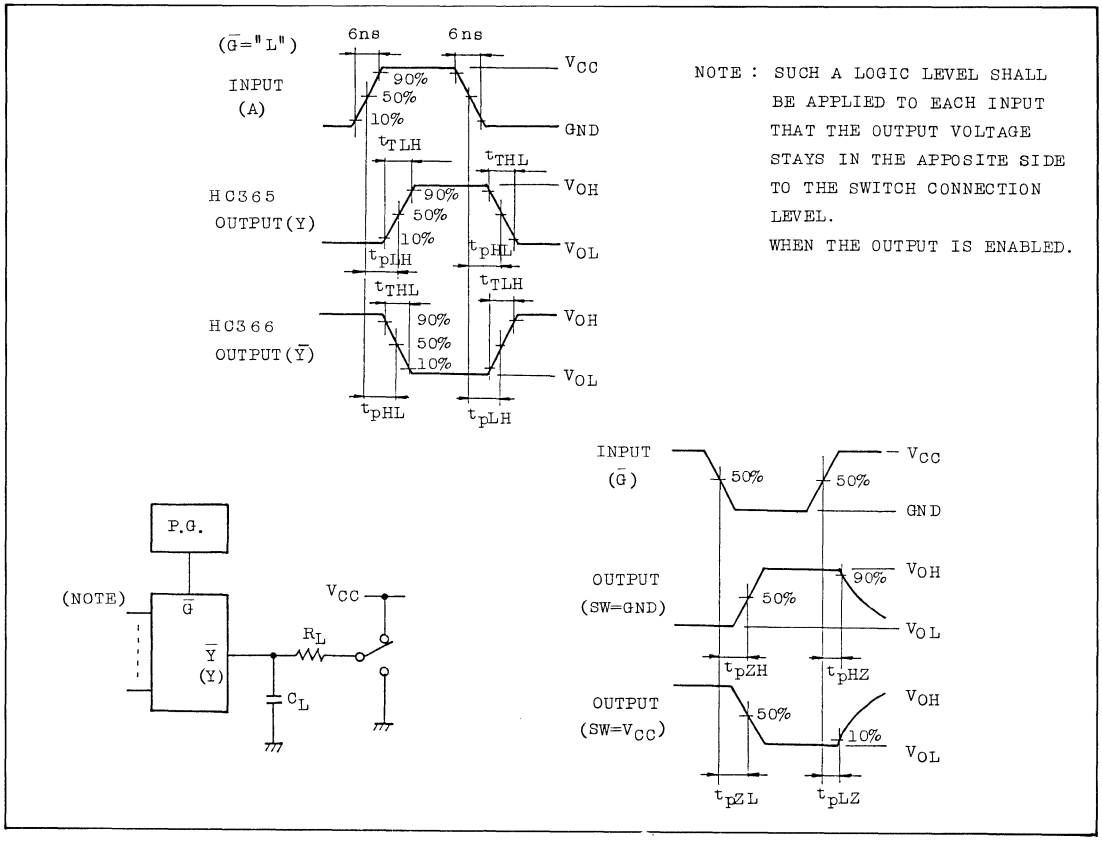
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HC365		-	33	-	-	-	pF
		TC74HC366		-	31	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

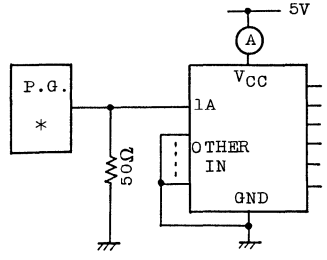
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per Circuit)}$$

(2) * : for TC74HC365 only.
**: for TC74HC366 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC367AP/AF/AFN
TC74HC368AP/AF/AFN

HEX BUS BUFFER
TC74HC367AP/AF/AFN NON-INVERTED
TC74HC368AP/AF/AFN INVERTED

The TC74HC367A and TC74HC368A are high speed CMOS 3-STATE BUS BUFFERs fablicated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

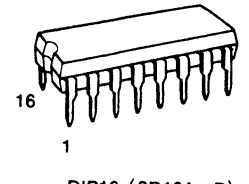
They contain six buffers; four buffers are controlled by an enable input ($\overline{G}1$), and the other two buffers are controlled by another enable input ($\overline{G}2$). The outputs of each buffer group are enabled when $\overline{G}1$ and/or $\overline{G}2$ inputs are held low; if held high, these outputs are in a high impedance state.

The TC74HC367A is a non-inverting output type, while the TC74HC368A is an inverting output type.

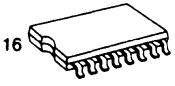
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

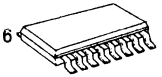
- High Speed ····· t_{pd} =11ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS367/368



DIP16 (3D16A-P)

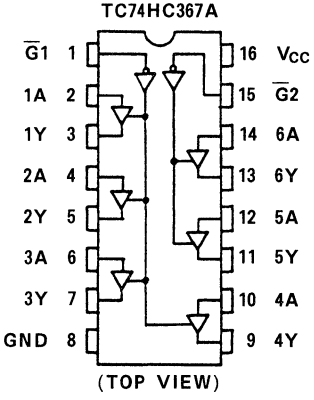


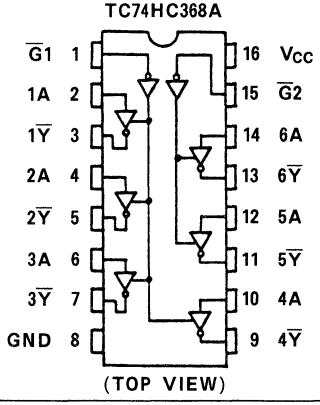
MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



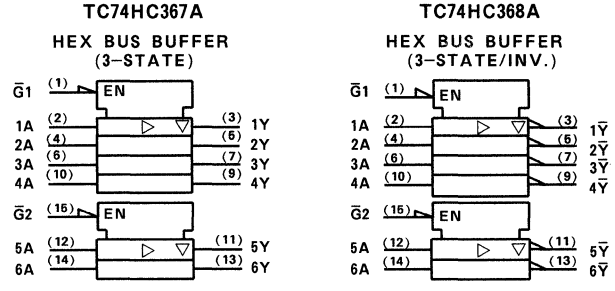


TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Y(367A)	$\overline{Y}$(368A)
L	L	L	H
L	H	H	L
H	X	Z	Z

X:DON'T CARE Z:HIGH IMPEDANCE

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃				Ta=−40 ～85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

ACELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	Vcc	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	−	36	95	−	120	
				4.5	−	12	19	−	24	
				6.0	−	10	16	−	20	
			150	2.0	−	40	130	−	165	
				4.5	−	16	26	−	33	
				6.0	−	14	22	−	28	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	36	120	−	150	
				4.5	−	12	24	−	30	
				6.0	−	10	20	−	26	
			150	2.0	−	40	160	−	200	
				4.5	−	16	32	−	40	
				6.0	−	14	27	−	34	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	35	120	−	150	
				4.5	−	15	24	−	30	
				6.0	−	13	20	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HC367A			−	36	−	−	−	
		TC74HC368A			−	30	−	−		

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$(per bit)

TC74HC373AP/AF
TC74HC533AP/AF

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC373AP/AF NON-INVERTING
TC74HC533AP/AF INVERTING

The TC74HC373A and TC74HC533A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

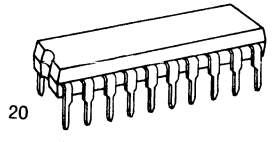
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC373A has non-inverting outputs, and TC74HC533A has inverting outputs.

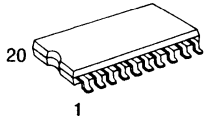
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=11ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS373/533

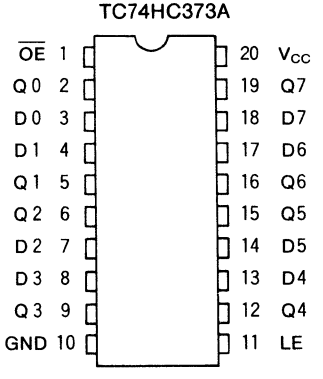


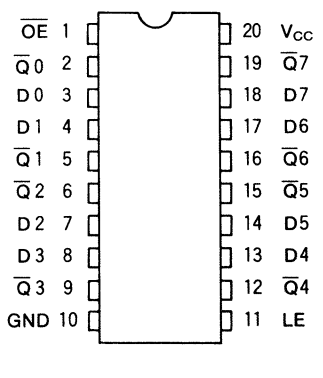
DIP20 (3D20A-P)



MFP20 (F20GA-P)

PIN ASSIGNMENT



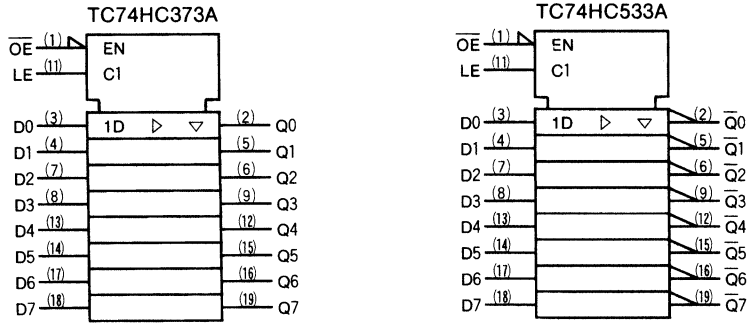


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC373A)	$\overline{Q}$(HC533A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

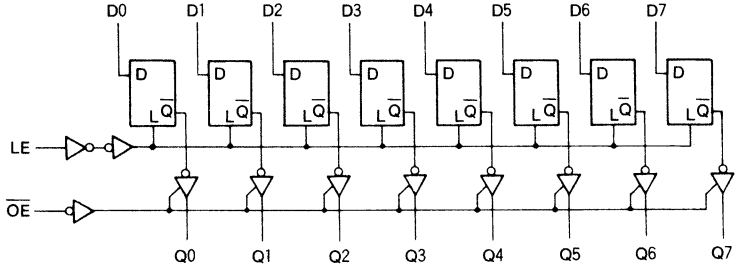
X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL

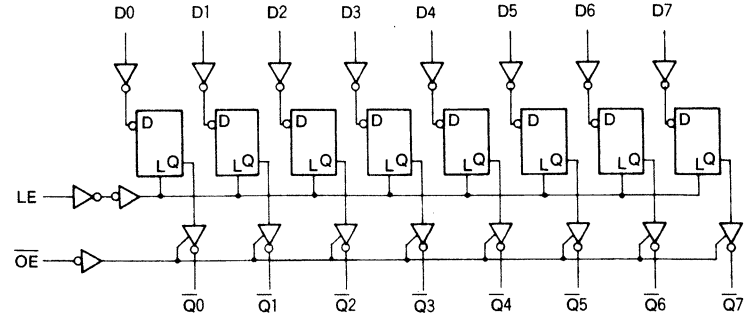


SYSTEM DIAGRAM

TC74HC373A



TC74HC533A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Data)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	39	125	−	155	
				4.5	−	13	25	−	31	
				6.0	−	11	21	−	26	
	t_{pZH}		150	2.0	−	54	175	−	220	
				4.5	−	18	35	−	44	
				6.0	−	15	30	−	37	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	30	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	13	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	38	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(total)=22+16 \cdot n$$

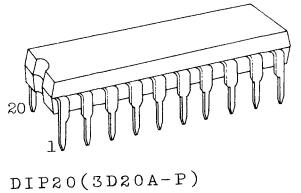
TC74HCT373P/F

TC74HCT373P/F OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

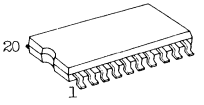
The TC74HCT373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
It may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT373 is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The TC74HCT373 and the TC74HCT573 have the same function and the same characteristics respectively, but have the different pin layouts. The three-state output configuration and the wide choise of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High speed ..... t_{pd}=19ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V (Min.), V_{IL}=0.8V(Max.)
- Wide interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS373

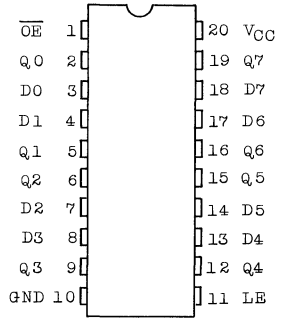


DIP20(3D20A-P)



MFP20(F20GA-P)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

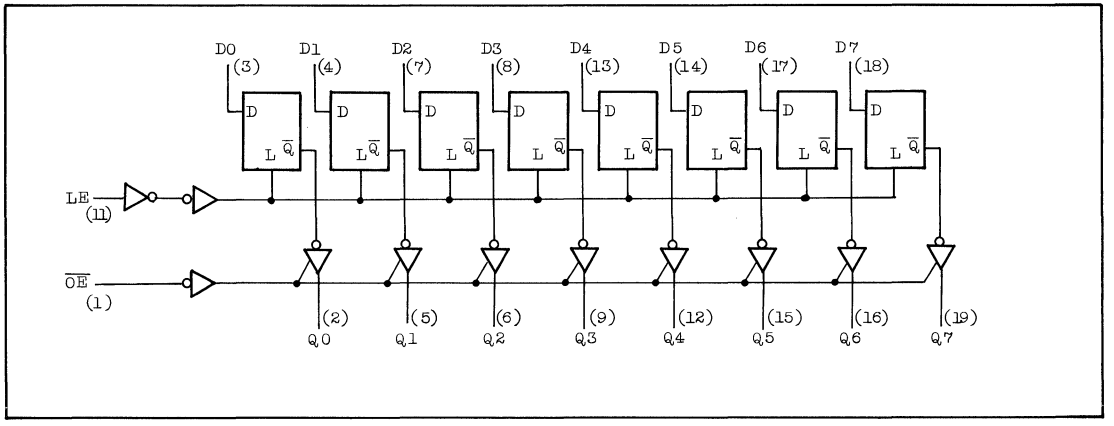
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q(HCT373)
H	X	X	Z
L	L	X	No change•
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

•: Q output was latched at the time when the LE input is taken low logic level.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

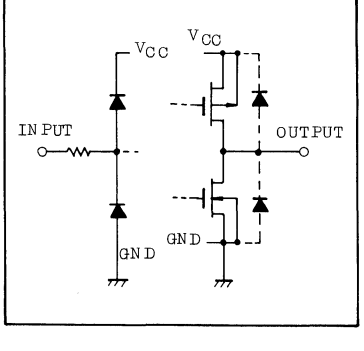
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (LE - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Propagation Delay Time (D - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	ns

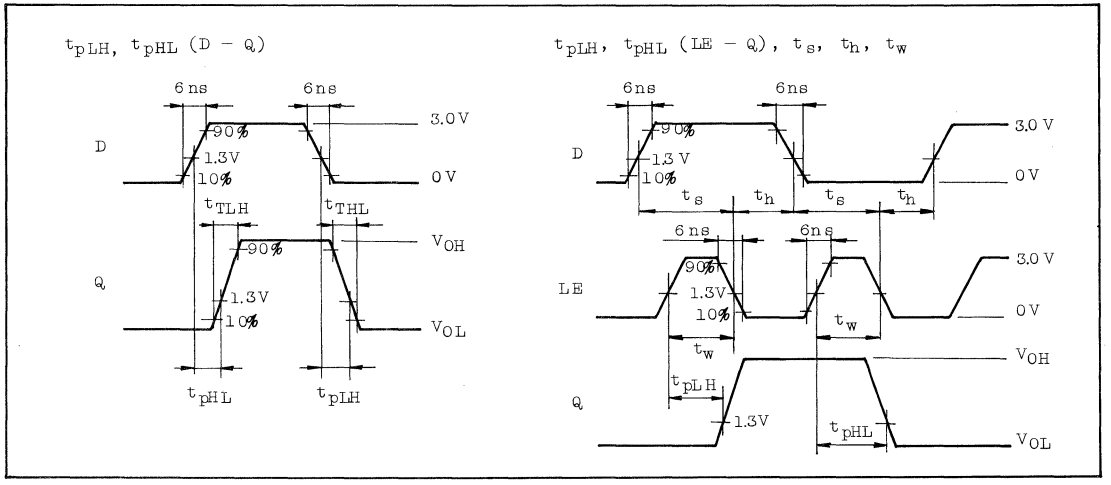
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Set-up Time	t_s		4.5	-	0	5	-	6	ns
Minimum Hold Time	t_h		4.5	-	3	10	-	13	ns
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	23	35	-	44	ns
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	21	30	-	38	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	55	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumpiton without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

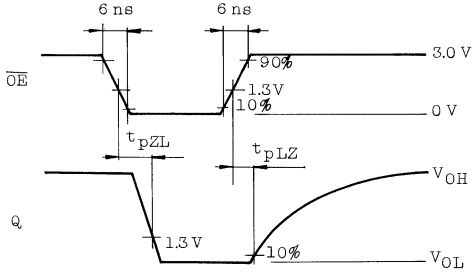
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

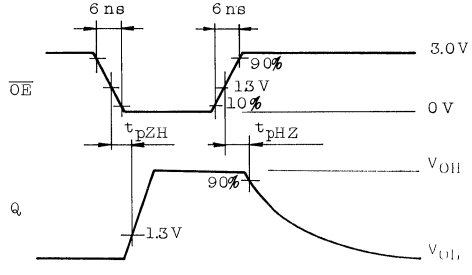
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line to GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

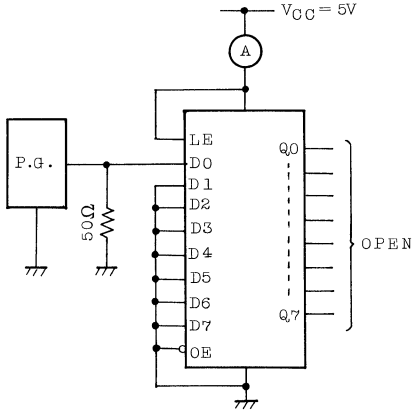


t_{pHZ}, t_{pZH}

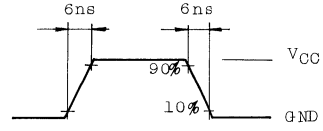
The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.



I_{CC}(Opr.) TEST CIRCUIT



INPUT WAVEFORM



TC74HC374AP/AF
TC74HC534AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HC374AP/AF NON-INVERTING
TC74HC534AP/AF INVERTING

The TC74HC374A and TC74HC534A are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

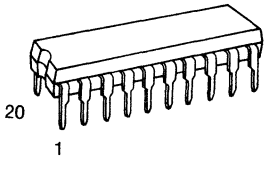
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC374A has non-inverting outputs, and TC74 HC534A has inverting outputs.

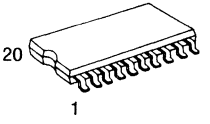
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=77MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS374/534



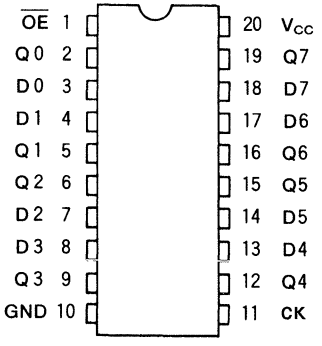
DIP20 (3D20A-P)



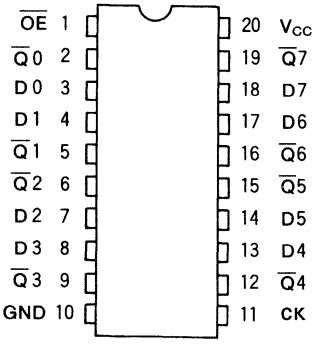
MFP20 (F20GA-P)

PIN ASSIGNMENT

TC74HC374A



TC74HC534A

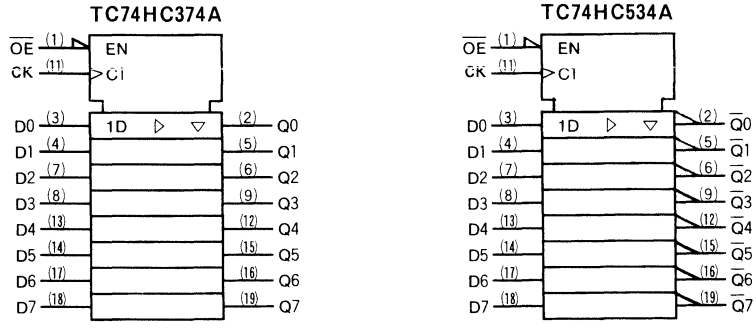


TRUTH TABLE

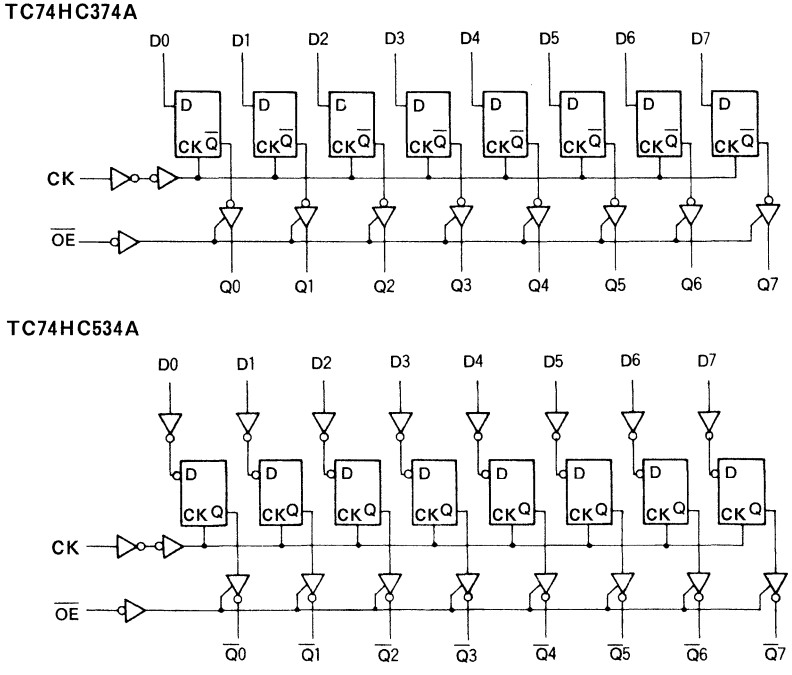
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(HC374A)	$\overline{Q}$(HC534A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Cange

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Dn)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (Dn)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	45	140	−	175	
				4.5	−	15	28	−	35	
				6.0	−	13	24	−	30	
	t_{pHL}		150	2.0	−	60	190	−	240	
				4.5	−	20	38	−	48	
				6.0	−	17	32	−	41	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	39	135	−	170	
				4.5	−	13	27	−	34	
				6.0	−	11	23	−	29	
	t_{pZH}		150	2.0	−	54	185	−	230	
				4.5	−	18	37	−	46	
				6.0	−	15	31	−	39	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	30	135	−	170	
				4.5	−	13	27	−	34	
				6.0	−	12	23	−	29	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	18	−	5	−	
				4.5	31	75	−	25	−	
				6.0	36	90	−	29	−	
			150	2.0	4	16	−	3	−	
				4.5	22	54	−	17	−	
				6.0	26	62	−	20	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)				−	47	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Flip Flop)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(total)=30+17 \cdot n$$

TC74HCT374AP/AF
TC74HCT534AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

TC74HCT374AP/AF NON-INVERTING
TC74HCT534AP/AF INVERTING

The TC74HCT374A and HCT534A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

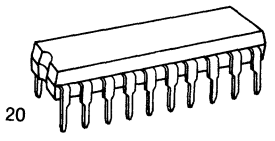
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HCT374A has non-inverting outputs, and the TC74HCT534A has inverting outputs.

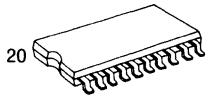
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=41MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V (Min.)
  V_{IL}=0.8V (Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS374/534



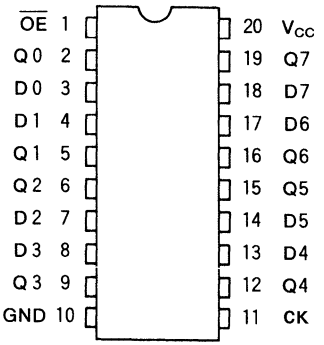
DIP20 (3D20A-P)



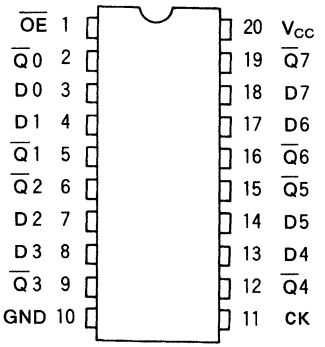
MFP20 (F20GA-P)

PIN ASSIGNMENT

TC74HCT374A



TC74HCT534A

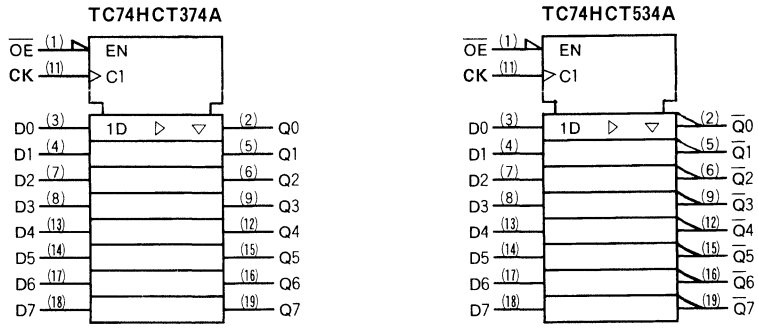


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(T374A)	$\overline{Q}$(T534A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

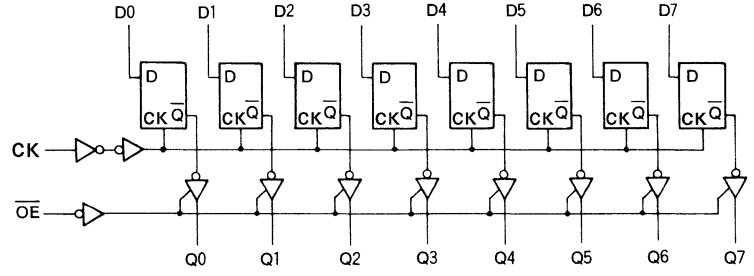
X : Don't Care
Z : High Impedance
$Q_n(\overline{Q_n})$: No Change

IEC LOGIC SYMBOL

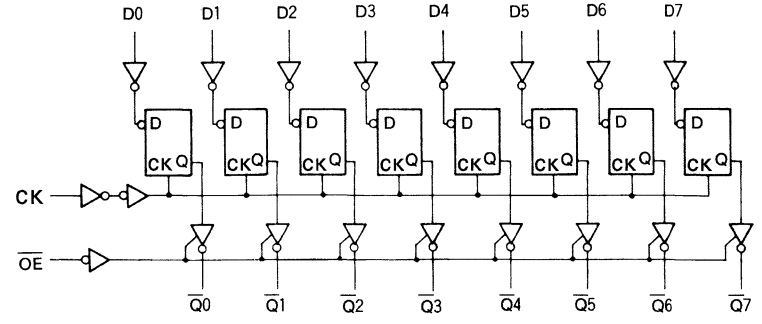


SYSTEM DIAGRAM

TC74HCT374A



TC74HCT534A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	I_C	PER INPUT: V_{IN} =0.5V or2.4V OTHER INPUT: V_{IN} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Set−up Time (Dn)	t_s		4.5	−	15	19	
			5.5	−	14	17	
Minimum Hold Time (Dn)	t_h		4.5	−	0	0	
			5.5	−	0	0	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5	−	7	12	−	15	ns
				5.5	−	6	11	−	14	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5	−	20	30	−	38	
				5.5	−	17	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	22	33	−	41	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	14	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	19	33	−	41	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	16	28	−	35	
				5.5	−	14	24	−	30	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	50	−	25	−	
				5.5	37	59	−	30	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	48	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total})=30+18 \cdot n$$

TC74HC375AP/AF

4-BIT D TYPE LATCH

The TC74HC375A is a high speed CMOS D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

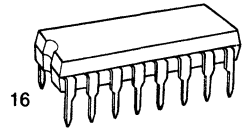
It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4) and each group can be used in different circuits.

Data applied to the data inputs are transferred to the Q and $\overline{Q}$ outputs when the enable inputs is high. When the en able input is low, the outputs are not affected.

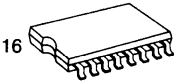
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =4 μ A(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH}=V_{NIL} =28%V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL} =4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)= 2 V~6V
- Pin and Function Compatible with 74LS375

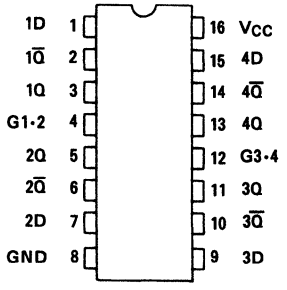


DIP16 (3D16A-P)



MFP16 (F16GC-P)

PIN ASSIGNMENT



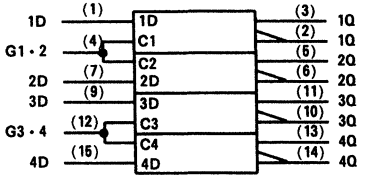
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\overline{Q}$n	LATCH

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIRMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (G)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	14	20	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	20	

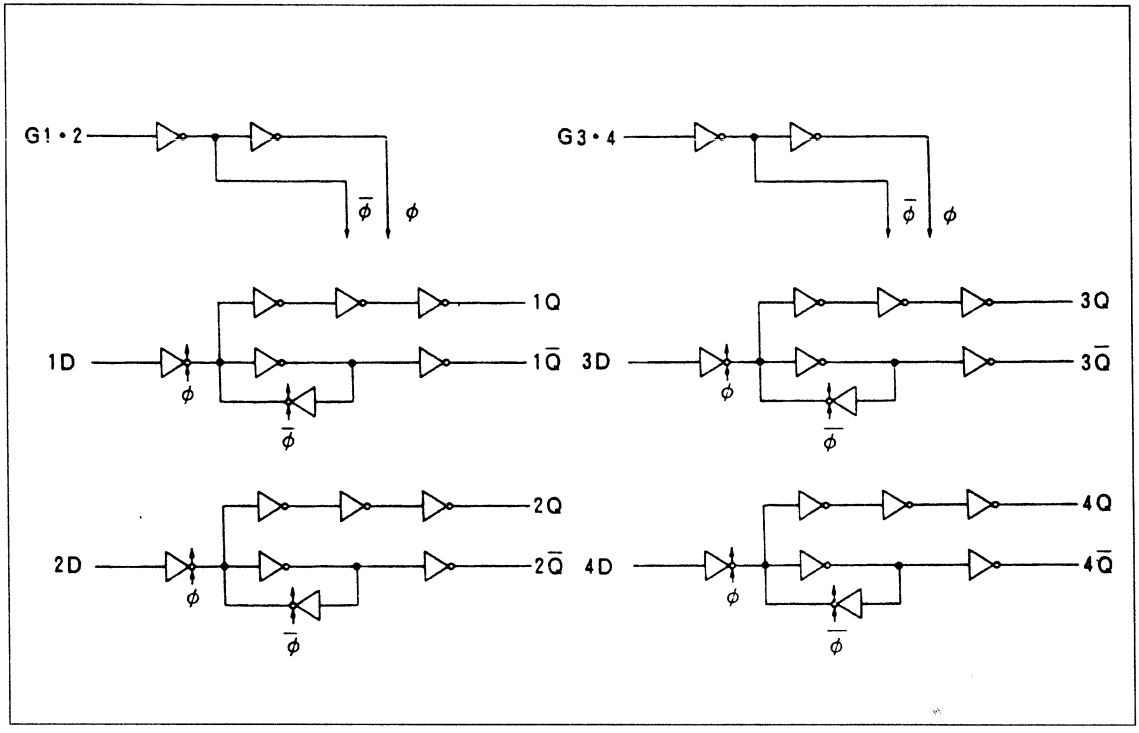
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITI...	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	60	120	−	150	
			4.5	−	17	24	−	30	
			6.0	−	15	20	−	26	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	56	120	−	150	
			4.5	−	16	24	−	30	
			6.0	−	14	20	−	26	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	55	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Latch)}$$

SYSTEM DIAGRAM



TC74HC377P/F

TC74HC377P/F OCTAL D-TYPE FLIP-FLOP

The TC74HC377 is high speed CMOS D-TYPE FLIP-FLOP fabricated with silicon C^2MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS Low power dissipation.

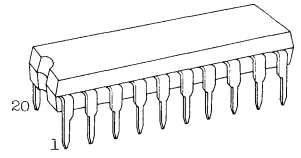
These eight flip-flops are controled by a clock input (CLOCK) and a enable input ($\overline{G}$). Information signals applied to D inputs are transferred to the Q outputs on the positive-going edge of the clock pulse.

When the enable input ($\overline{G}$) is held high, each Q outputs isn't changed.

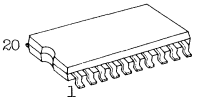
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL(74LS377)



DIP20(3D20A-P)



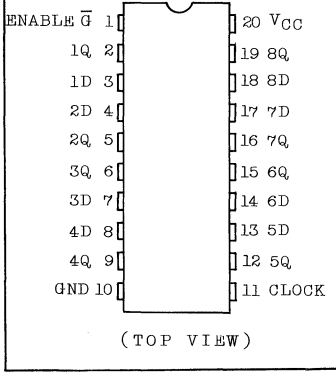
MFP20(F20GA-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



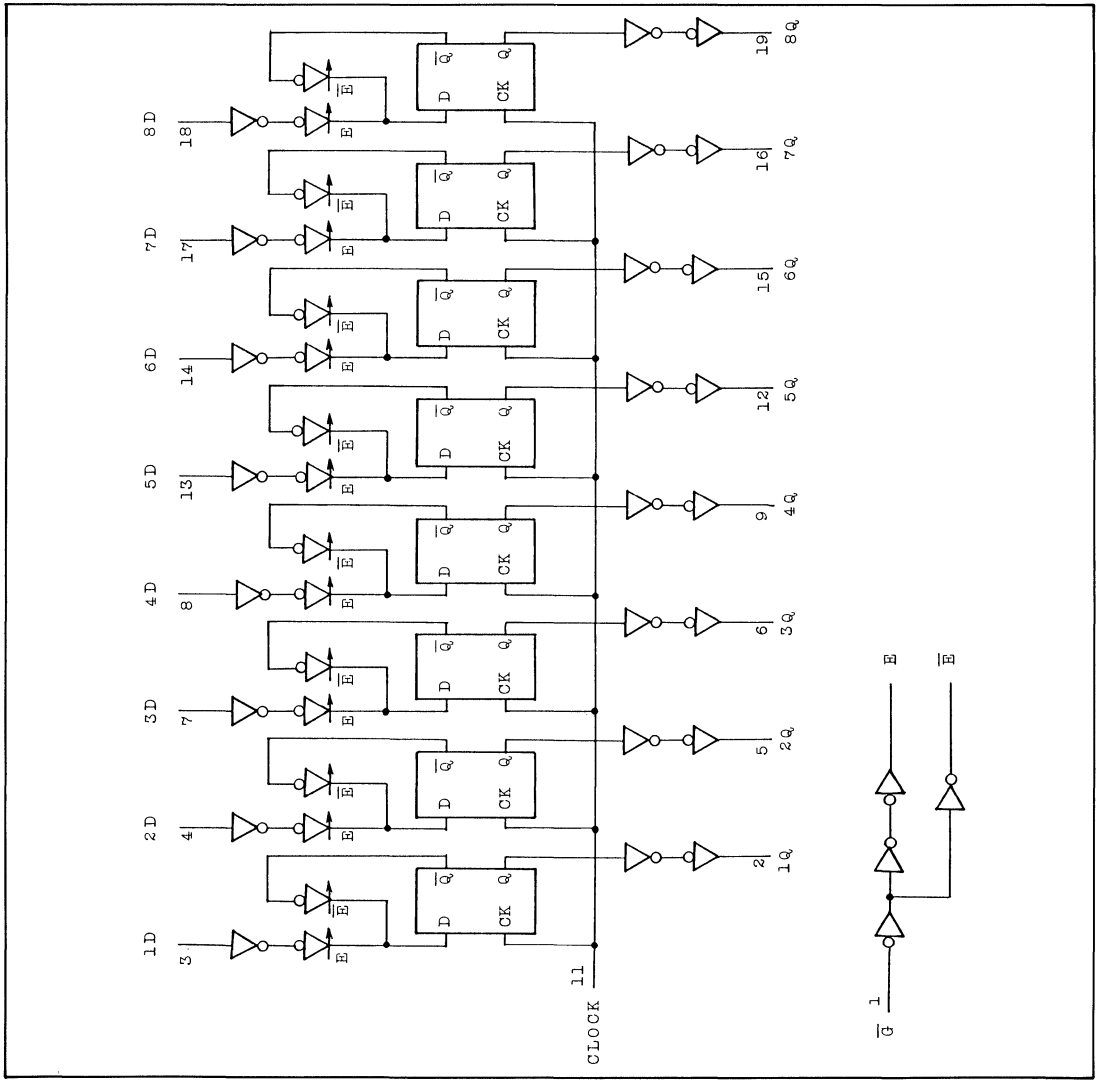
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{G}$	CLOCK	DATA	Q
H	X	X	No Change
L	↑	L	L
L	↑	H	H
X	↓	X	No Change

X ; Don't care

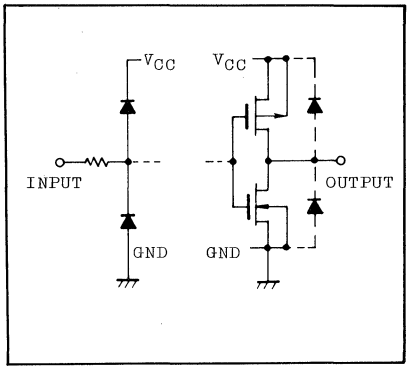
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

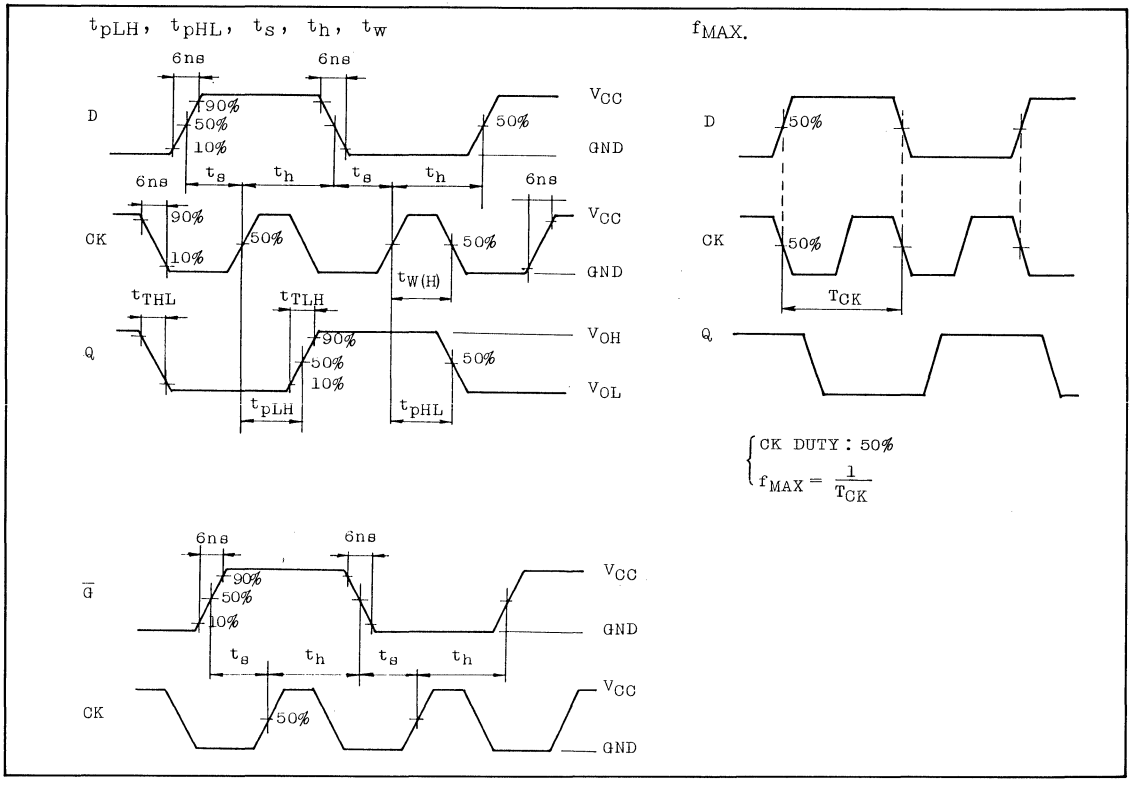
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	50	-	27	-	
			6.0	35	59	-	32	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (D - CK)	t_s		2.0	-	24	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set-up Time Enable ($\overline{G}$ - CK)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}				5	10		10	pF
Power Dissipation Capacitance	C_{PD}(1)				34				

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

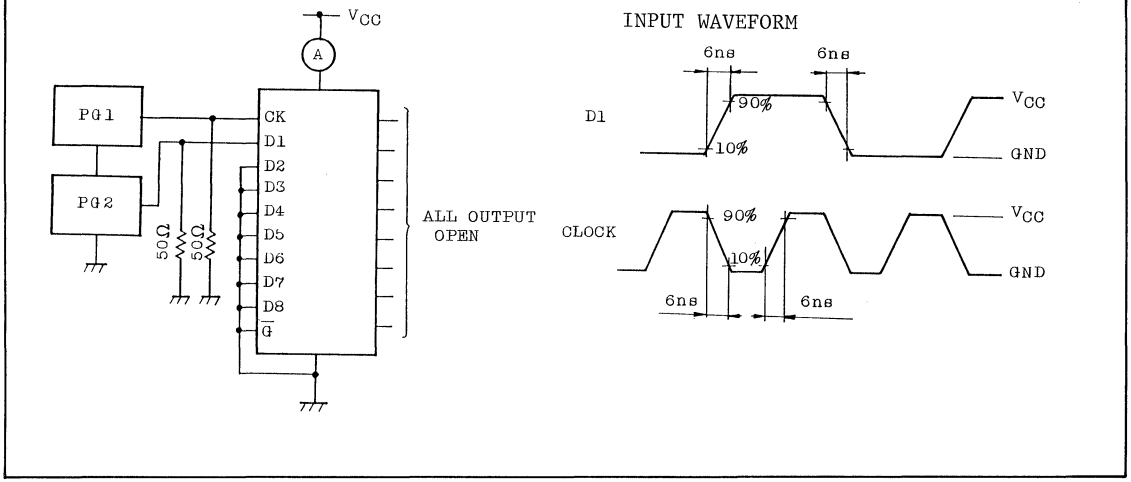
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$$

And the C_{PD} when n pcs of FLIP-FLOP operate, can be gained by following equation. $C_{PD}(TOTAL)=22+12\times n$ [pF]

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



TC74HC386AP/AF

QUAD EXCLUSIVE OR GATE

The TC74HC386A is a high speed CMOS EXCLUSIVE-OR GATE fabricated with silicon gate C^2MOS technology.

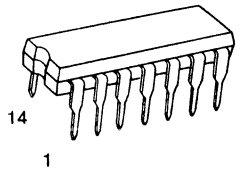
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is includes on output buffer, which provide high noise immunity and stable output.

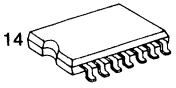
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS386

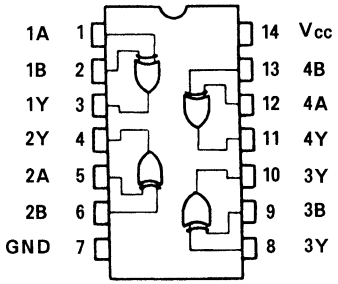


DIP14 (3D14A-P)



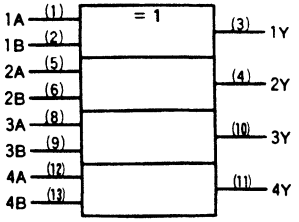
MFP14 (F14GB-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	48	100	–	125	ns
			4.5	–	12	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	31	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC390AP/AF/AFN

DUAL DECADE COUNTER

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER LATCH fabricated with silicon gate C^2MOS technology.

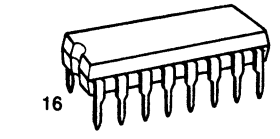
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A ($\overline{CKA}$). The divided-by-five counter is incremented on the negative going transition of clock B ($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

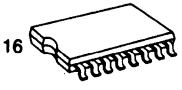
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

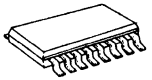
- High Speed ····· f_{MAX}=84MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS390



DIP16 (3D16A-P)

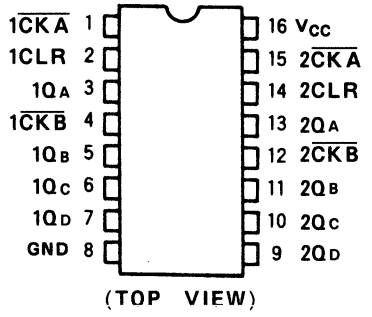


MFP 16
(F16GC-P)

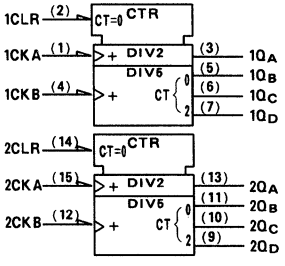


SOP 16
(SOP16-P-225A)

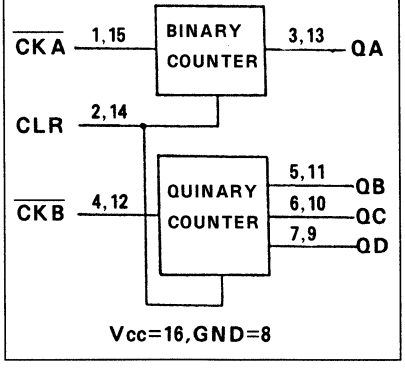
PIN ASSIGNMENT



IEC LOGIC SYMBOL



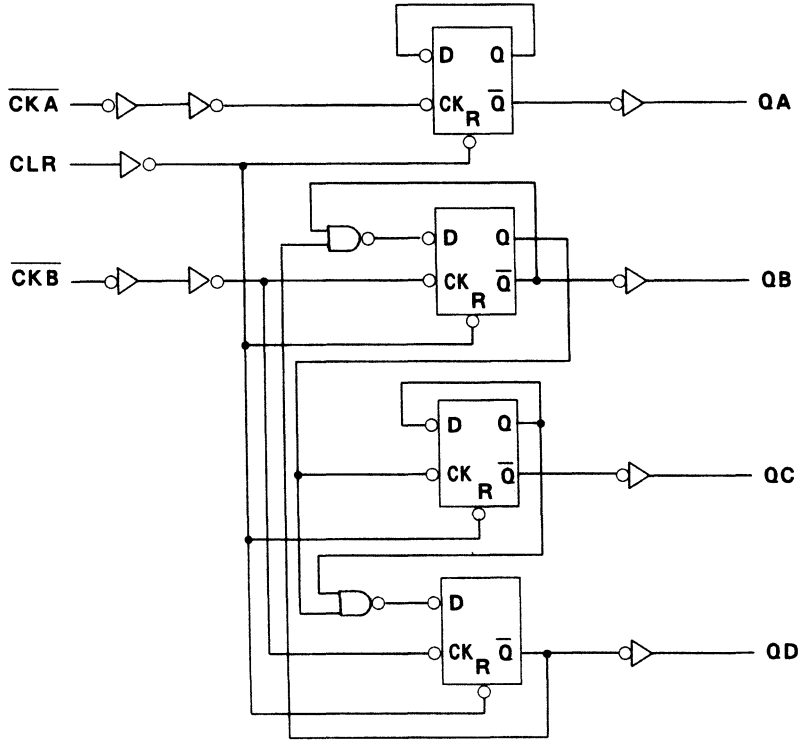
BLOCK DIAGRAM



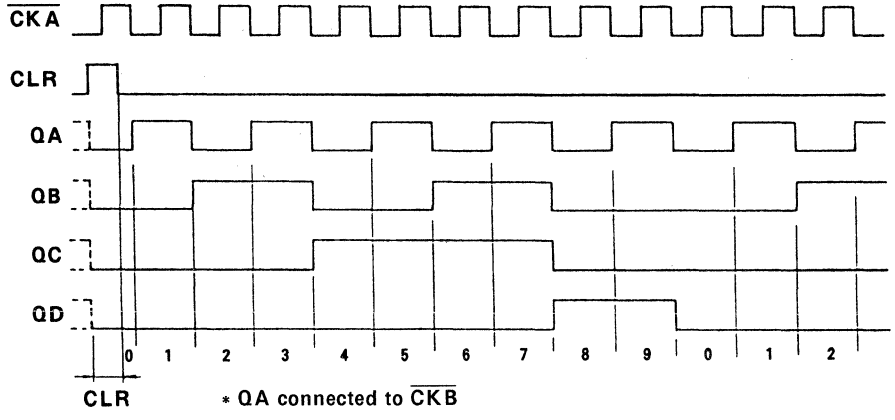
TRUTH TABLE

INTPUTS			OUTPUTS			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

SYSTEM DIAGRAM(1/2 package)

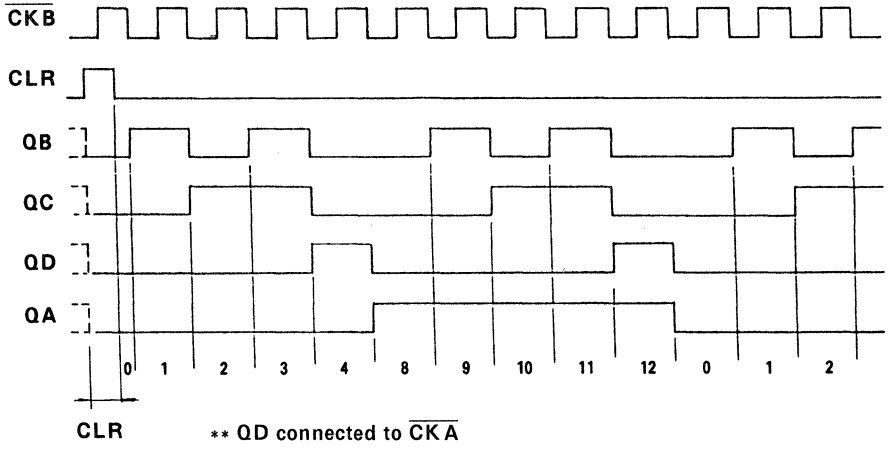


(1)BCD COUNT SEQUENCE*



* QA connected to $\overline{CKB}$

(2)BI-QUINARY COUNT SEQUENCE**



** QD connected to $\overline{CKA}$

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Clock Frequency ($\overline{CKA}$)	f		2.0	−	6	5	
			4.5	−	32	26	
			6.0	−	38	31	
Clock Frequency ($\overline{CKB}$)	f		2.0	−	6	5	
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CKA}$−QA)	t_{pLH} t_{pHL}		−	10	20	
Propagation Delay Time ($\overline{CKA}$−QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	−	29	51	
Propagation Delay Time ($\overline{CKB}$−QB, QD)	t_{pLH} t_{pHL}		−	12	22	
Propagation Delay Time ($\overline{CKB}$−QC)	t_{pLH} t_{pHL}		−	17	32	
Propagation Delay Time (CLR−Qn)	t_{pHL}		−	12	26	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}		35	84	−	MHz
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}		33	65	−	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CKA}$−QA)	t_{pLH} t_{pHL}		2.0	−	39	120	−	150	
			4.5	−	13	24	−	30	
			6.0	−	11	20	−	26	
Propagation Delay Time ($\overline{CKA}$−QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	2.0	−	102	290	−	365	
			4.5	−	34	58	−	73	
			6.0	−	29	49	−	62	
Propagation Delay Time ($\overline{CKB}$−QB, QD)	t_{pLH} t_{pHL}		2.0	−	45	130	−	165	
			4.5	−	15	26	−	33	
			6.0	−	13	22	−	28	
Propagation Delay Time ($\overline{CKB}$−QC)	t_{pLH} t_{pHL}		2.0	−	63	185	−	165	
			4.5	−	21	37	−	33	
			6.0	−	18	31	−	28	
Propagation Delay Time (CLR−Qn)	t_{pHL}		2.0	−	45	150	−	190	
			4.5	−	15	30	−	38	
			6.0	−	13	26	−	32	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}		2.0	6	20	−	5	−	MHz
			4.5	32	77	−	26	−	
			6.0	38	90	−	31	−	
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}		2.0	6	15	−	5	−	
			4.5	31	60	−	25	−	
			6.0	36	70	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	44	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Counter)}$$

TC74HC393AP/AF/AFN

DUAL BINARY COUNTER

The TC74HC393A is a high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

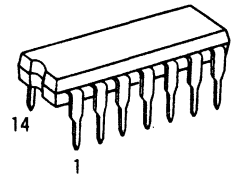
It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the $\overline{CLOCK}$ pulse. The counter can be reset to "0" (Q0~Q3="L") by a high at the CLEAR input regardless of other inputs.

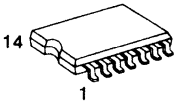
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

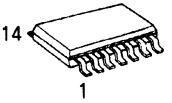
- High Speed ····· f_{MAX}=72MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS393



DIP14 (3 D14A-P)

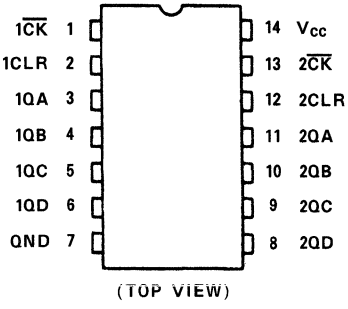


MFP 14
(F14GB-P)

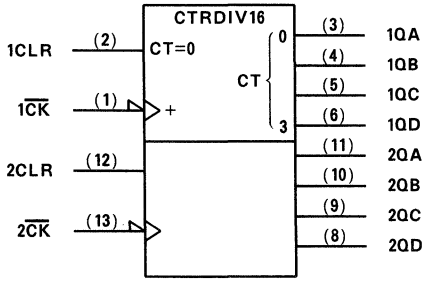


SOP 14
(SOP14-P-225A)

PIN ASSIGNMENT



IEC LOGIC SYMBOL

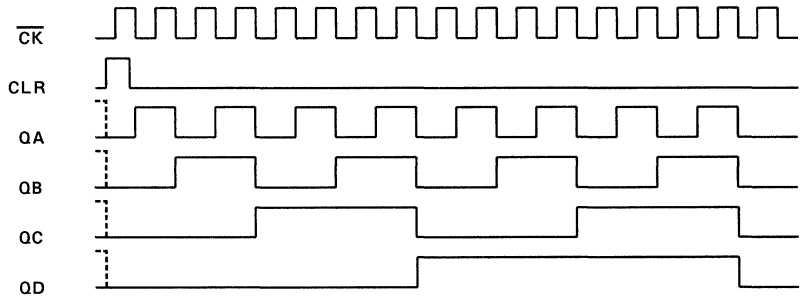


TRUTH TABLE

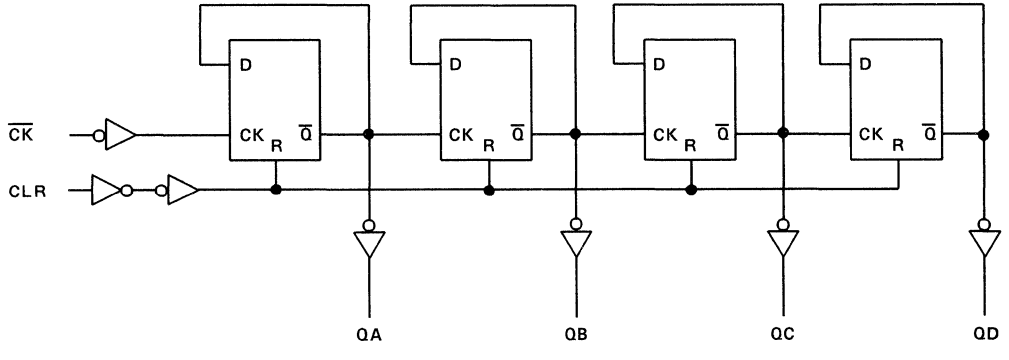
INPUTS		OUTPUTS			
$\overline{CK}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

X : Don't care

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$–QA)	t_{pLH} t_{pHL}		–	12	20	
Propagation Delay Time ($\overline{CLOCK}$–QB)	t_{pLH} t_{pHL}		–	16	31	
Propagation Delay Time ($\overline{CLOCK}$–QC)	t_{pLH} t_{pHL}		–	21	38	
Propagation Delay Time ($\overline{CLOCK}$–QD)	t_{pLH} t_{pHL}		–	25	46	
Propagation Delay Time (CLEAR–Qn)	t_{pHL}		–	15	26	
Maximum Clock Frequency	f_{MAX}		35	72	–	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time ($\overline{CLOCK}$–QA)	t_{pLH} t_{pHL}		2.0	–	45	120	–	150	
			4.5	–	15	24	–	30	
			6.0	–	13	20	–	26	
Propagation Delay Time ($\overline{CLOCK}$–QB)	t_{pLH} t_{pHL}		2.0	–	60	180	–	225	
			4.5	–	20	36	–	45	
			6.0	–	17	31	–	38	
Propagation Delay Time ($\overline{CLOCK}$–QC)	t_{pLH} t_{pHL}		2.0	–	80	220	–	275	
			4.5	–	25	44	–	55	
			6.0	–	21	37	–	47	
Propagation Delay Time ($\overline{CLOCK}$–QD)	t_{pLH} t_{pHL}		2.0	–	100	260	–	325	
			4.5	–	30	52	–	65	
			6.0	–	26	44	–	55	
Propagation Delay Time (CLEAR–Qn)	t_{pHL}		2.0	–	55	150	–	190	
			4.5	–	18	30	–	38	
			6.0	–	15	26	–	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	22	–	5	–	
			4.5	32	67	–	27	–	
			6.0	38	77	–	32	–	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	40	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC423P/F

TC74HC423P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

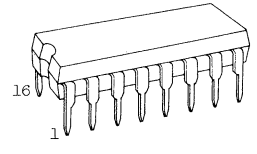
The TC74HC423 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is $\overline{A}$ INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... No limitation
External resistor Rx ..... V_{CC} = 2.0V from 5KΩ to 1MΩ
$V_{CC} \geqq$ 3.0V from 1KΩ to 1MΩ

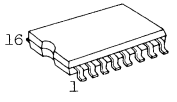
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=28ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range ... t_w(OUT)=120nS ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



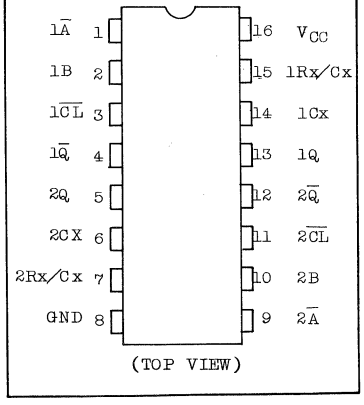
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

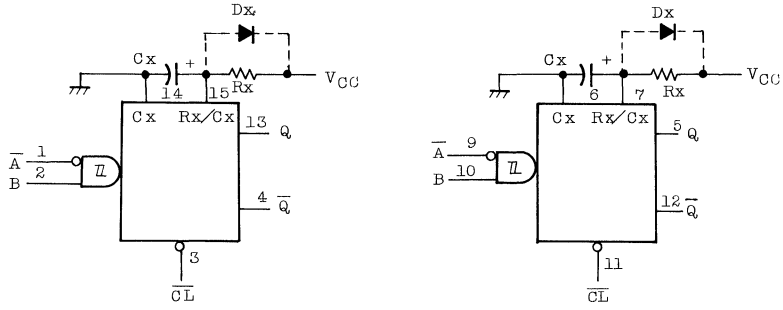


TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎎	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⎍	⎎	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

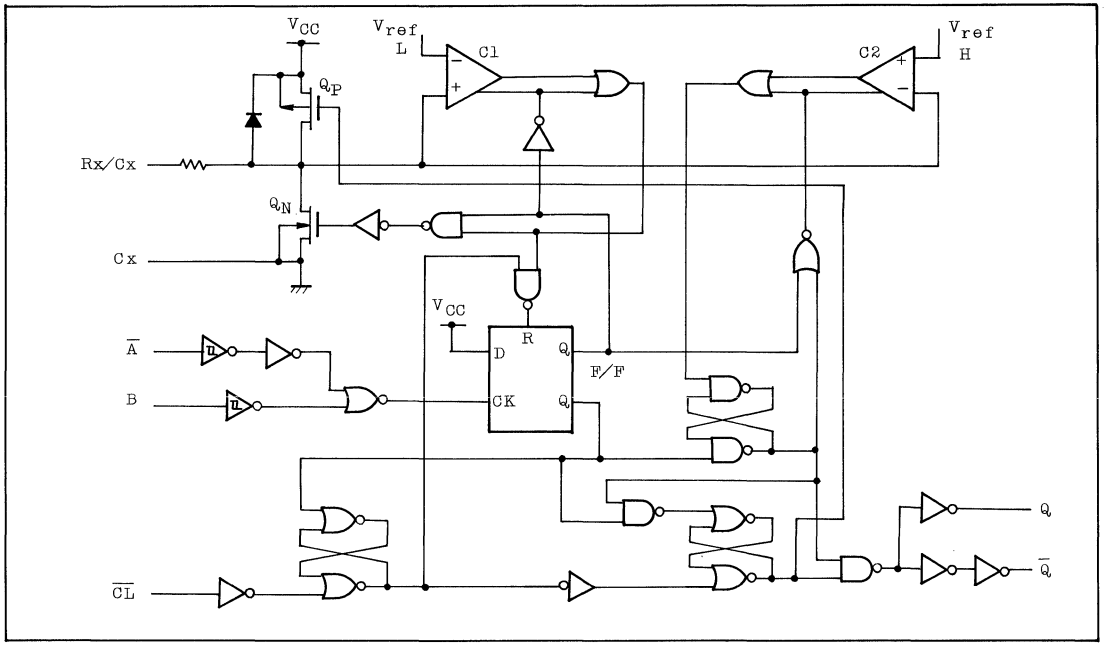
External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

$$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$$

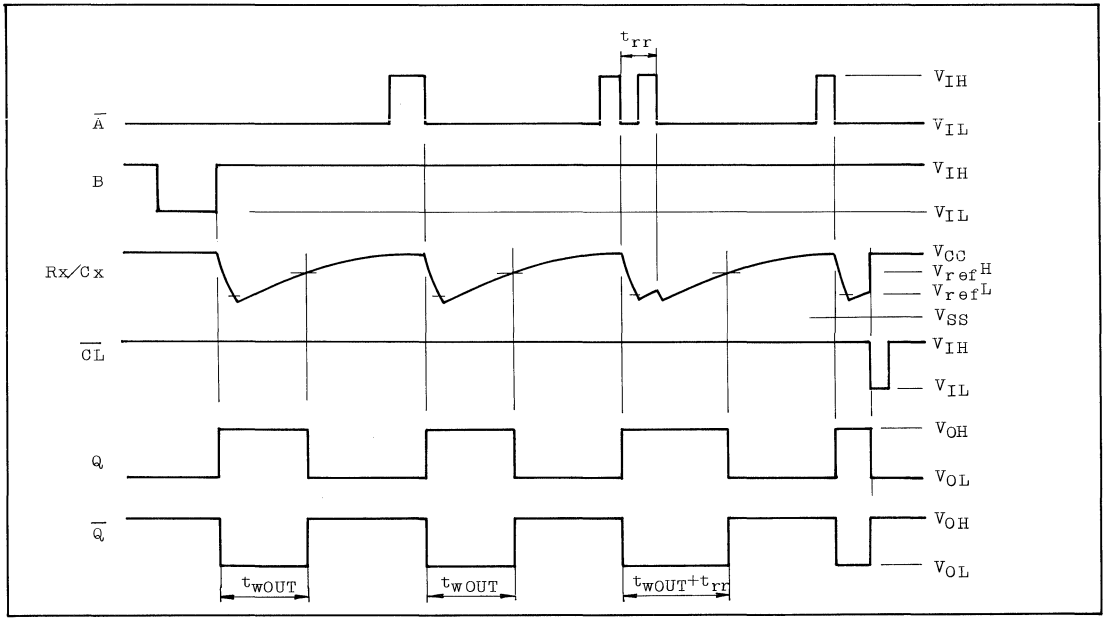
(t_f is the time from voltage supply turning of to level of voltage supply becoming 0.4 V_{CC})

In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition $\bar{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\bar{A}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.
After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.
By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.46 \quad Cx \; Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

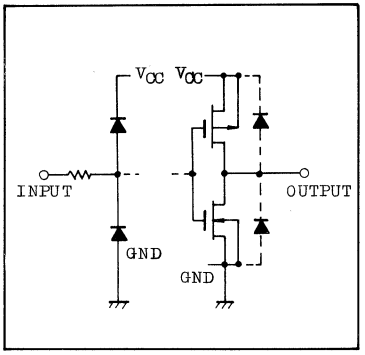
(4) Reset operation

$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) ($V_{CC}\geqq$3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

* : Per Circuit

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

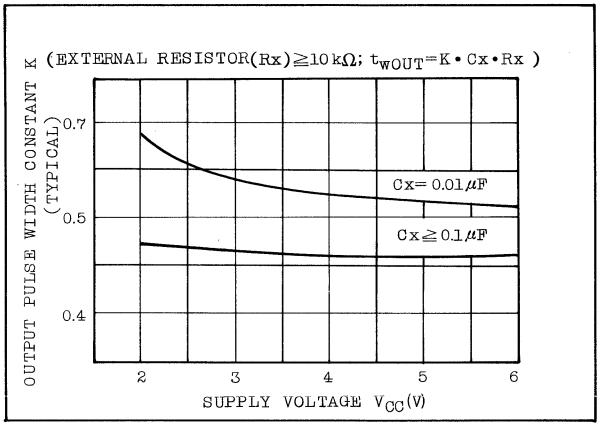
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Minimum Pulse Wdith ($\overline{A}$, B)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Pulse Width Error Between Circuits In Same Package	ΔT_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	ns
			6.0	-	63	-	-	-	
		Cx=0.01uF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	T_{out} (MIN)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	T_{out}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1uF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	113	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

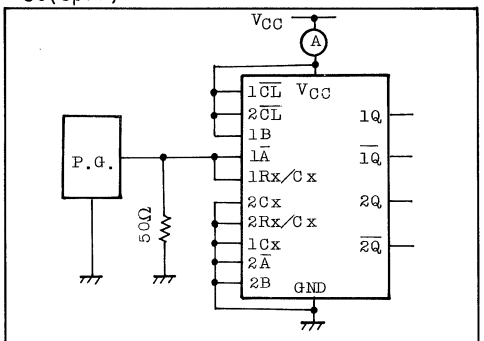
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2 \quad \text{(per monostable)}$$

(I_{CC}': Active Supply Current) (Dury: %)

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

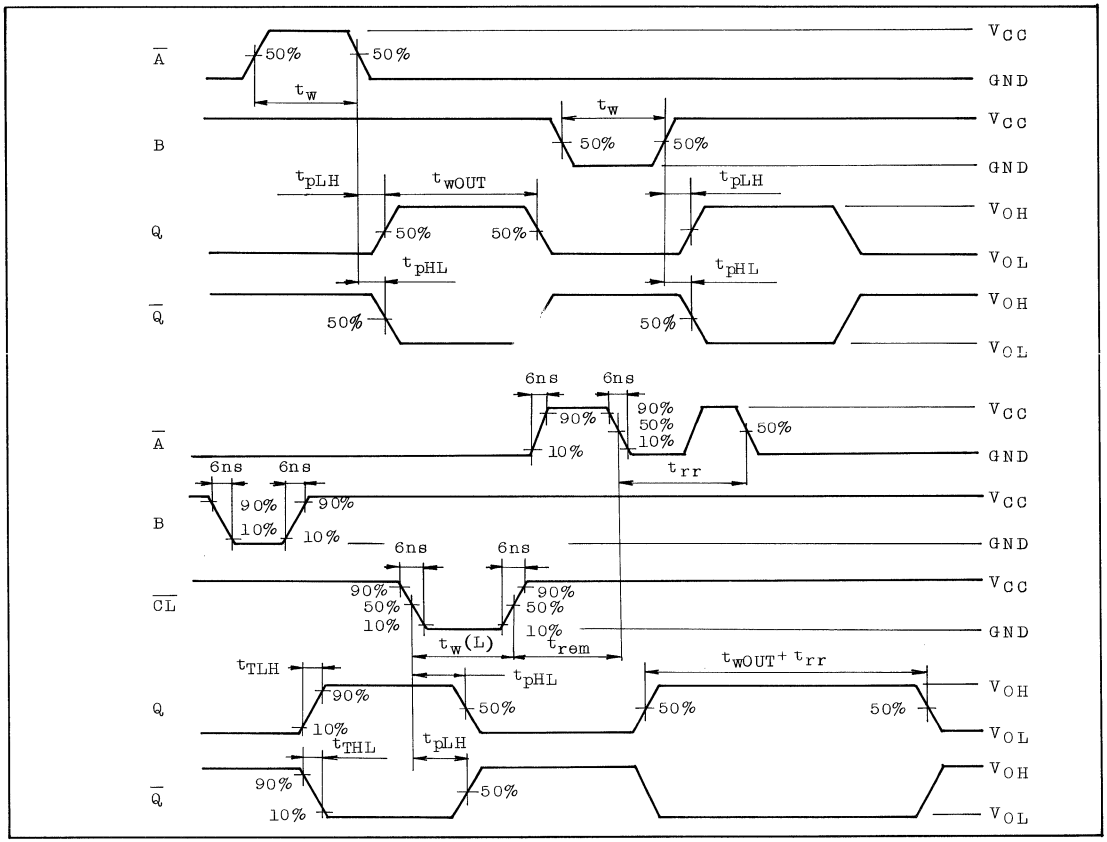


I_{CC}(opr.) TEST WAVEFORM

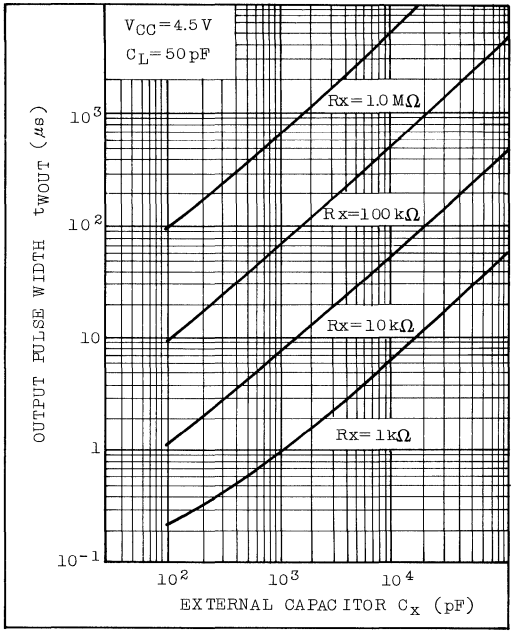


※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

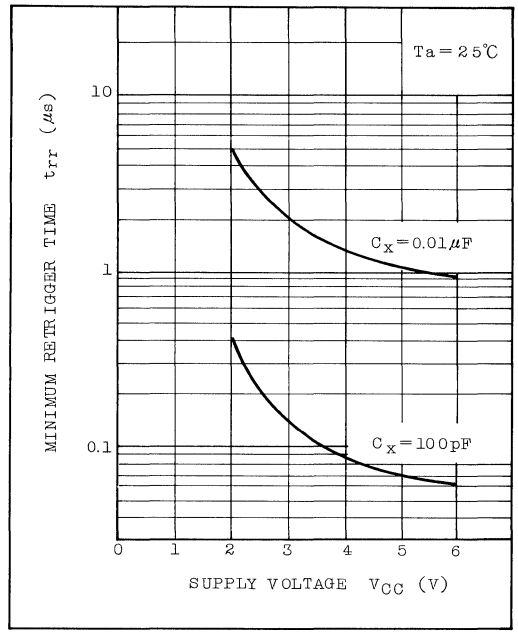
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



TC74HC540AP/AF
TC74HC541AP/AF

OCTAL BUS BUFFER
TC74HC540AP/AF INVERTING,3-STATE OUTPUTS
TC74HC541AP/AF NON-INVERTING,3-STATE OUTPUTS

The TC74HC540A/TC74HC541A are high speed CMOS OCTRAL BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

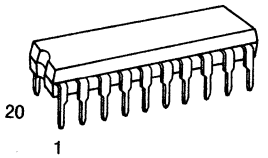
The TC74HC540A is a non-inverting type, and the TC74 HC541A is an inverting type.

When either $\overline{G}1$ or $\overline{G}2$ are high, the terminal outputs are in the high-impedance state.

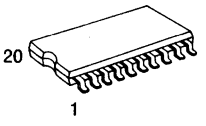
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS540/541



DIP20 (3D20A-P)



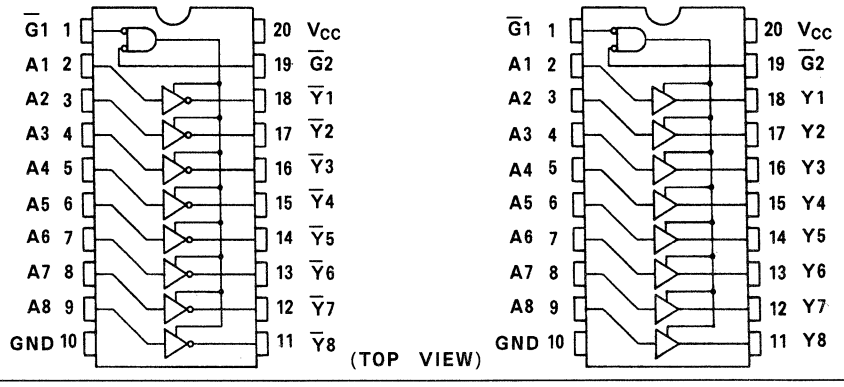
MFP20 (F20GA-P)

TRUTH TABLE

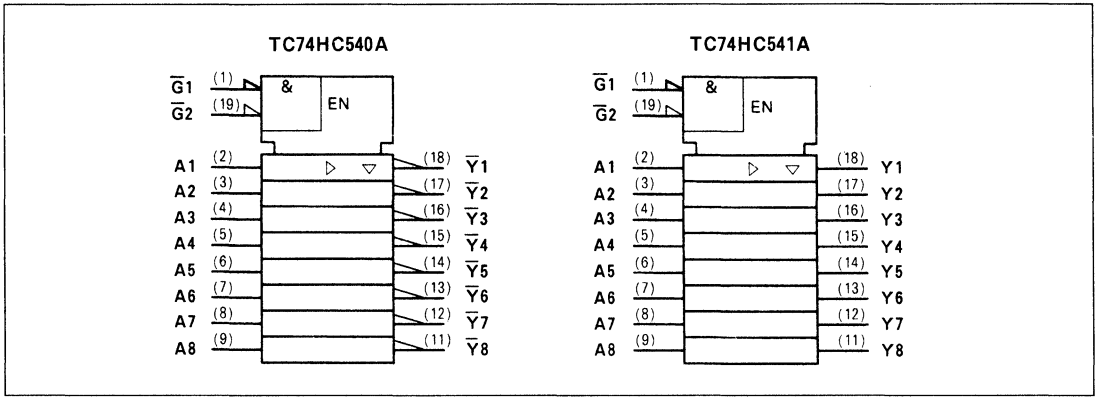
INPUTS			OUTPUTS	
$\overline{G}1$	$\overline{G}2$	An	Yn*	$\overline{Y}n$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X : Don't Care
Z : High Impedance
* : Yn ····· HC541A
$\overline{Y}n$ ····· HC540A

PIN ASSIGNMENT



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	36	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	51	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	14	22	−	28	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	2.0	−	45	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pZH}		150	2.0	−	60	165	−	205	
				4.5	−	19	33	−	41	
				6.0	−	16	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	40	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC540A			−	32	−	−	−	
		TC74HC541A			−	35	−	−	−	

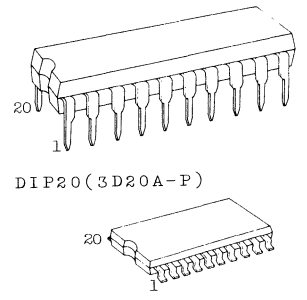
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HCT540P/F
TC74HCT541P/F

TC74HCT540P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HCT541P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

The TC74HCT540 and TC74HCT541 are high speed CMOS OCTAL BUS BUFFER fabricated with silicon gate C^2MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT540 is non-inverting type. The TC74HCT541 is inverting type. If either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



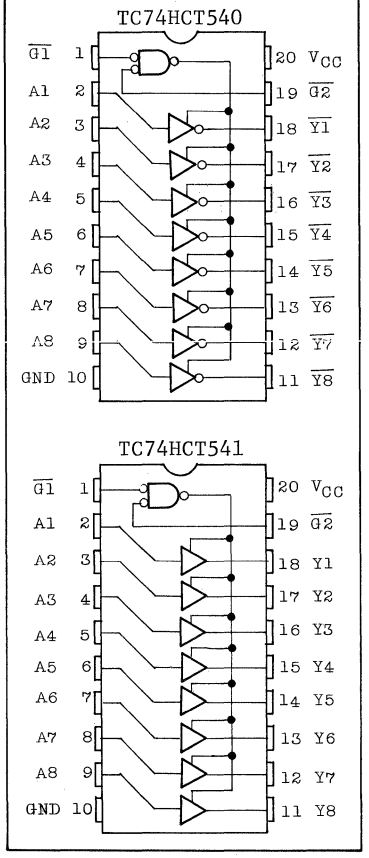
FEATURES:

- High Speed ..... t_{pd}=13ns(T540) at V_{CC}=5V
  16ns(T541)
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74LS540/541

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

PIN ASSIGNMENT (TOP VIEW)

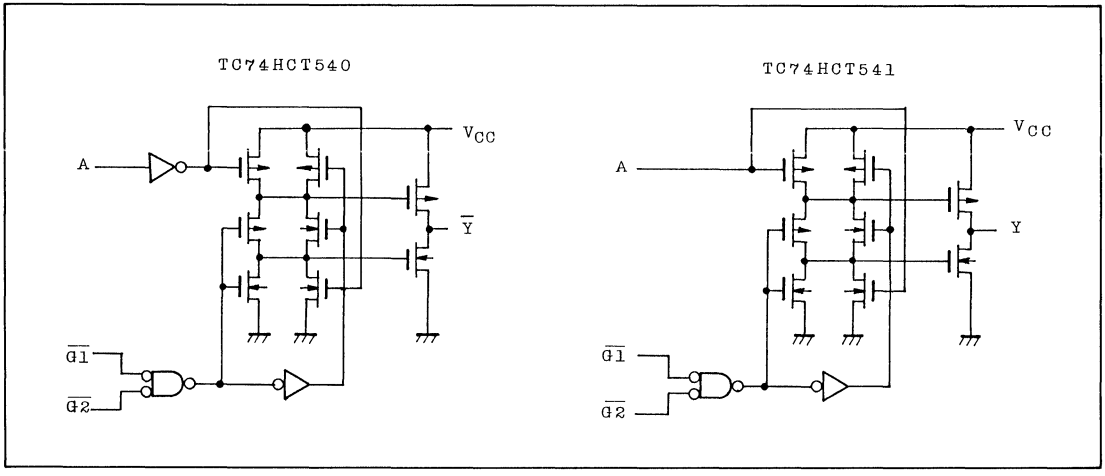


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: Don't Care
Z: High Impedance
*: Yn HCT541
$\overline{Yn}$ HCT540

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

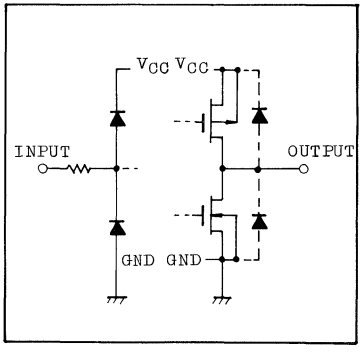
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP)* 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	
	I_C	Per Input: V_{IN}=2.4V or 0.5V Other Input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT540	4.5	-	16	26	-	32	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT541	4.5	-	19	30	-	36	
Output Enable Time	t_{pLZ} t_{pZH}	R_L=1kΩ	4.5	-	23	36	-	44	

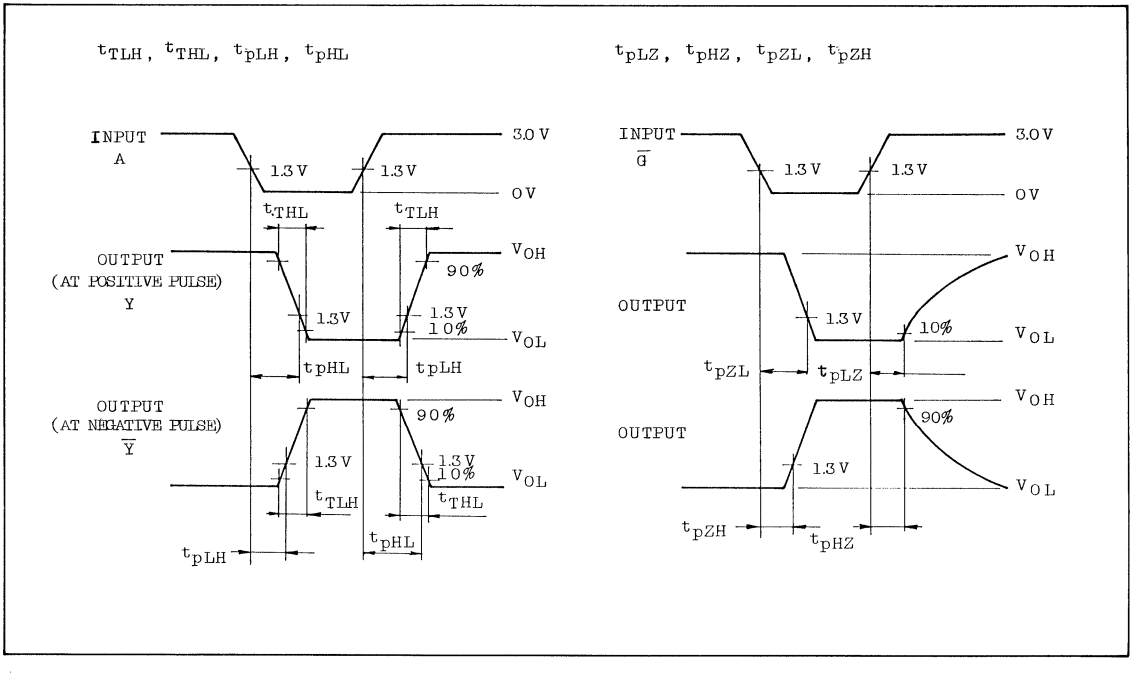
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	23	33	-	39	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT540		-	37	-	-	-	
		TC74HCT541		-	39	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

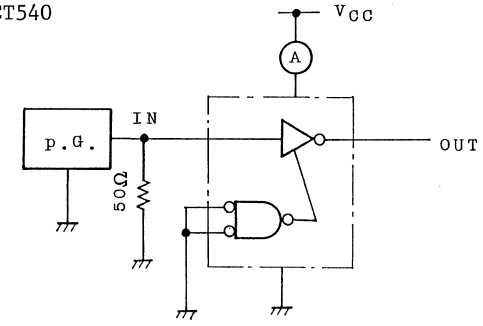
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Gate)}$$

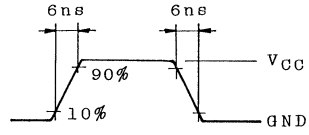
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT

TC74HCT540





The other inputs are connected V_{CC} line or GND line.

Test circuit of the TC74HCT541 is the same as this.

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC563AP/AF INVERTING
TC74HC573AP/AF NON-INVERTING

The TC74HC563A and TC74HC573A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achive the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input($\overline{OE}$).

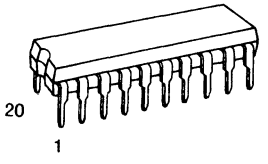
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC563A has inverting outputs, and TC74HC573A has non-inverting outputs.

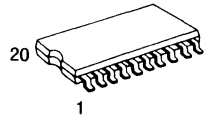
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS563/573

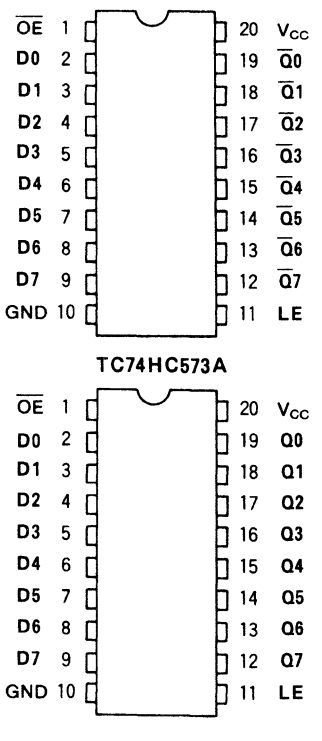


DIP20 (3D20A-P)



MFP20 (F20GA-P)

PIN ASSIGNMENT

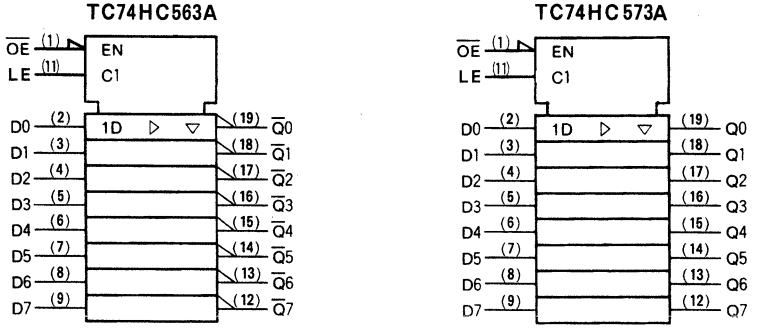


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC573A)	$\overline{Q}$(HC563A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

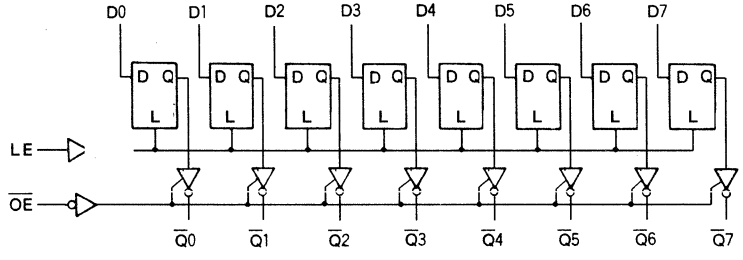
X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : Q($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL

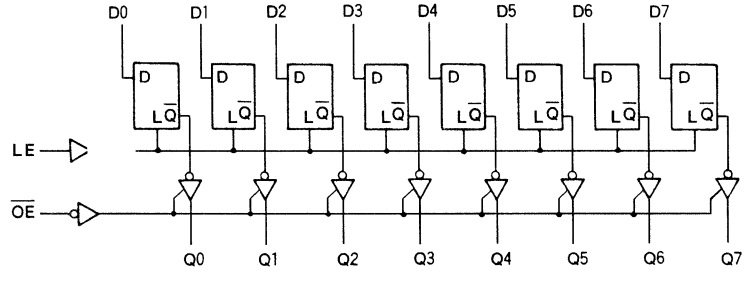


SYSTEM DIAGRAM

TC74HC563A



TC74HC573A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Data)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	13	20	−	25	
	t_{pHL}		150	2.0	−	60	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	17	26	−	33	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	110	−	140	
				4.5	−	14	22	−	28	
				6.0	−	12	19	−	24	
	t_{pHL}		150	2.0	−	57	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	32	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	55	140	−	175	
				4.5	−	17	28	−	35	
				6.0	−	14	24	−	30	
	t_{pZH}		150	2.0	−	66	180	−	225	
				4.5	−	22	36	−	45	
				6.0	−	19	31	−	38	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	40	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	15	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC563A			−	49	−	−	−	
		TC74HC573A			−	51	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

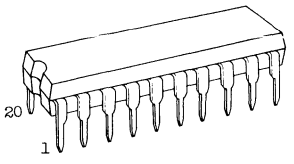
$C_{PD}(total)=33+16 \cdot n$ (TC74HC563A)
$C_{PD}(total)=33+18 \cdot n$ (TC74HC573A)

TC74HCT563P
TC74HCT573P

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT563P INVERTING
TC74HCT573P NON-INVERTING

The TC74HCT563 and TC74HCT573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input(LE) and a output enable input($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs.
The three-state output configuration and the wide choice of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

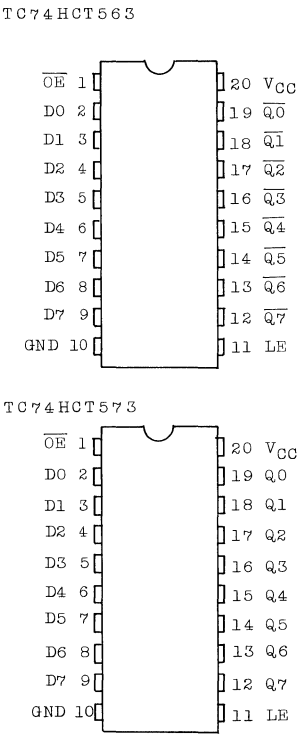


DIP20(3D20A-P)

FEATURES:

- High Speed ..... t_{pd}=20ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS563/573

PIN ASSIGNMENT (TOP VIEW)



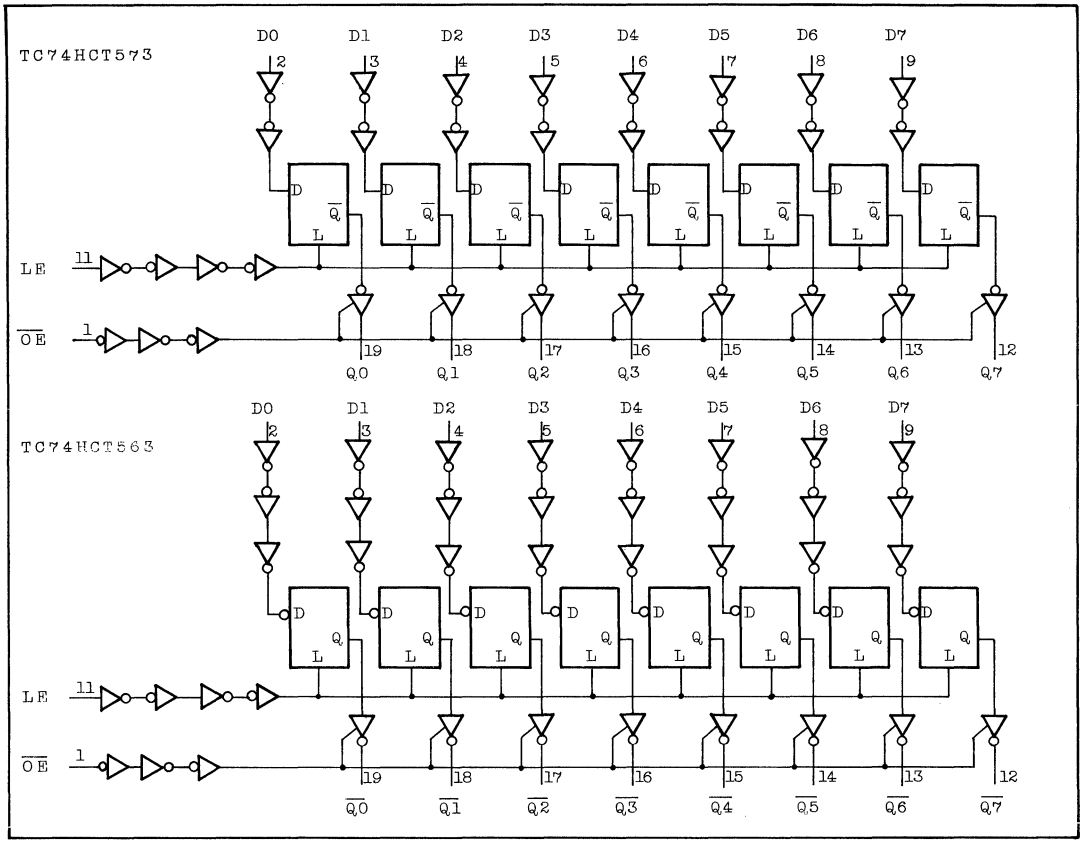
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HCT573)	$\overline{Q}$(HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	$\overline{Qn}$
L	H	L	L	H
L	H	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE

Qn : Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

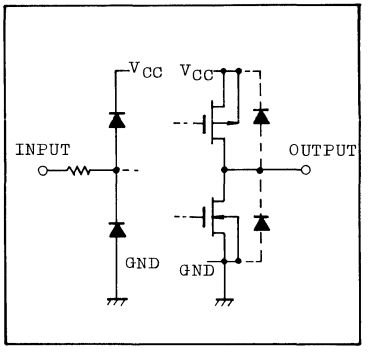
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65~150	°C
Lead Temperature (10 sec)	T_L	300	°C

* 500mW in the range of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500 (V_{CC}=4.5V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	19	ns
Propagation Delay Time (LE - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	24	35	-	44	
Propagation Delay Time (D - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	22	35	-	44	
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	
Minimum Set-up Time	t_s		4.5	-	2	10	-	13	
Minimum Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT563		-	41	-	-	-	
		TC74HCT573		-	41	-	-	-	

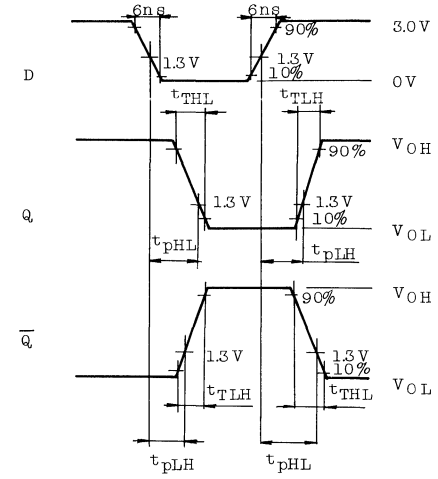
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

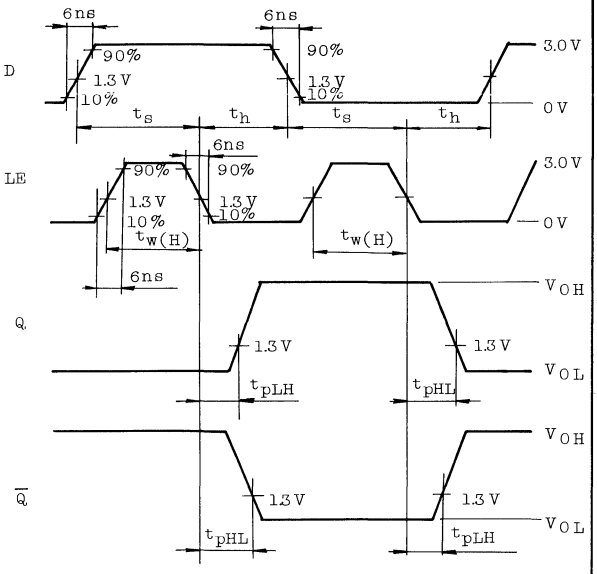
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

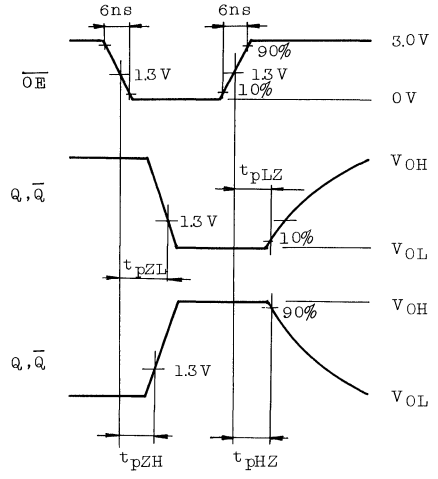
t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}

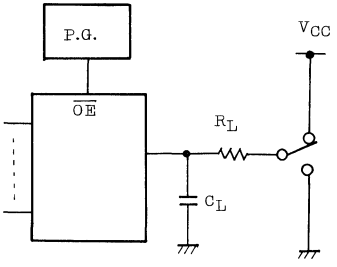


t_{pLH}, t_{pHL}(LE-Q,$\overline{Q}$), t_s, t_h, t_w



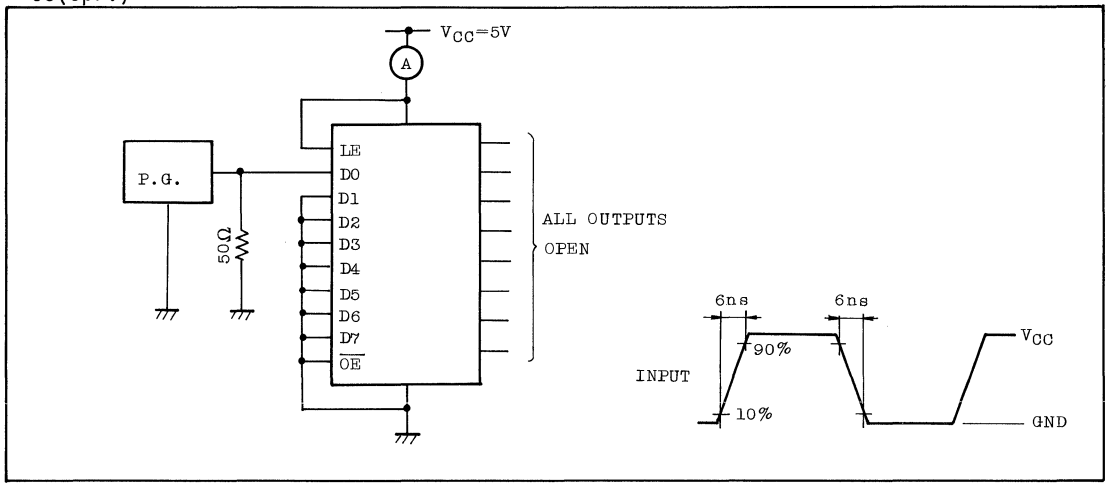
t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}





(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC564AP/AF
TC74HC574AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HC564AP/AF INVERTING
TC74HC574AP/AF NON-INVERTING

The TC74HC564A and HC574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

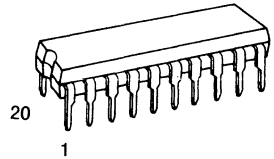
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HC564A has inverting outputs, and the TC74 HC574A has non-inverting outputs.

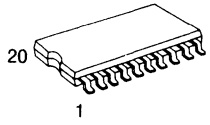
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=62MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS564/574



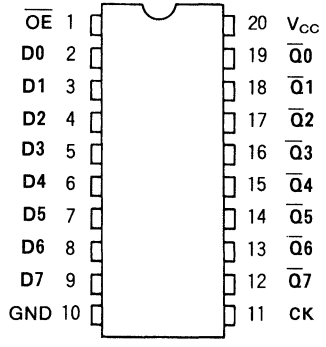
DIP20 (3D20A-P)



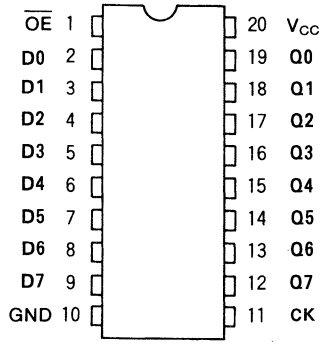
MFP20 (F20GA-P)

PIN ASSIGNMENT

TC74HC564A



TC74HC574A

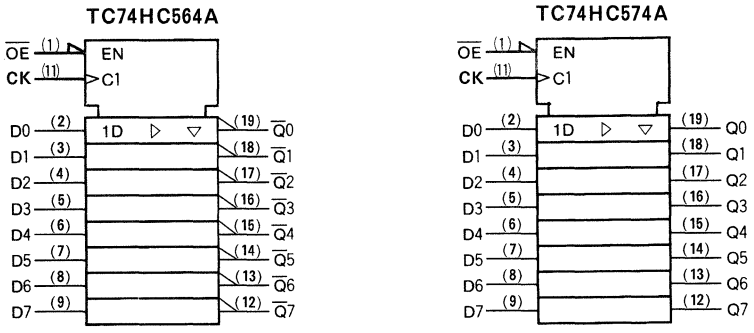


TRUTH TABLE

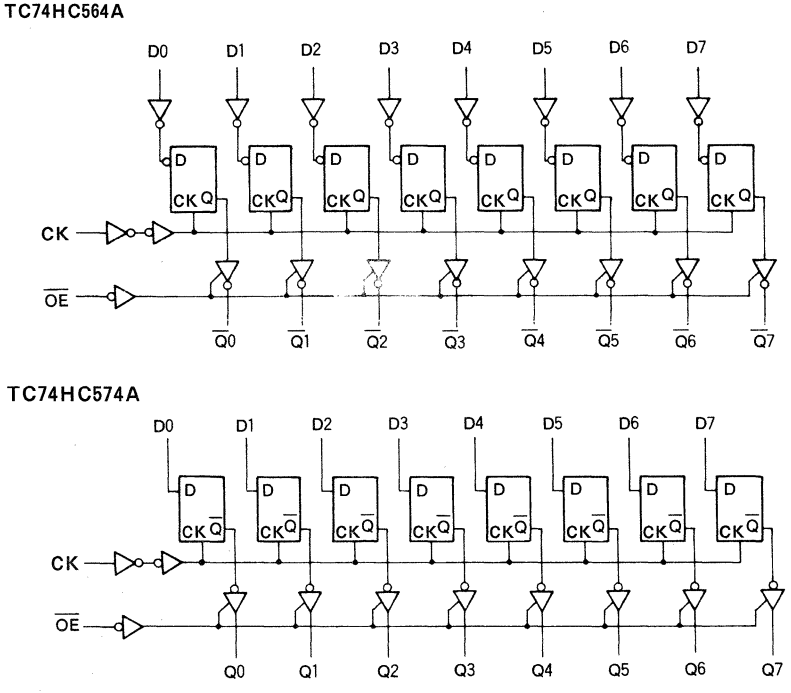
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574A)	$\overline{Q}$(564A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Dn)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (Dn)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	24	
			6.0	−	36	28	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	2.0	−	70	150	−	190	
				4.5	−	20	30	−	38	
				6.0	−	15	26	−	33	
			150	2.0	−	88	190	−	240	
				4.5	−	25	38	−	48	
				6.0	−	19	33	−	41	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	12	21	−	26	
			150	2.0	−	60	165	−	205	
				4.5	−	20	33	−	41	
				6.0	−	16	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	34	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	15	21	−	26	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	17	−	5	−	
				4.5	31	50	−	24	−	
				6.0	36	59	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	54	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per bit})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total})=39+15 \cdot n$$

TC74HCT564P
TC74HCT574P

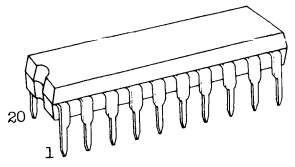
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT564P INVERTING
TC74HCT574P NON-INVERTING

The TC74HCT564 and TC74HCT574 are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology. These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These 8-bit D-type flip-flops are controlled by a clock input(CK) and a output enable input($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely (HCT574) or inversely (HCT564) to the logic state that were setup at the D inputs. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

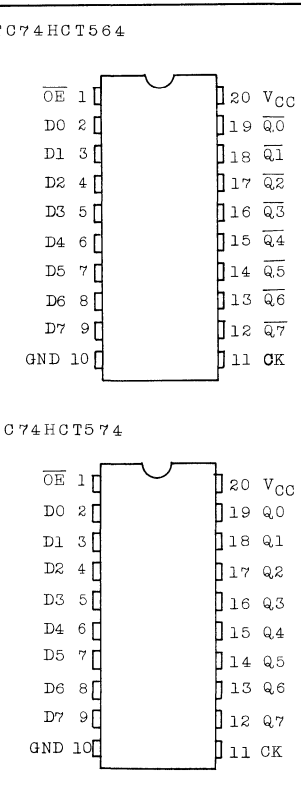
FEATURES:

- High Speed ..... f_{MAX}=41MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Pin and Function Compatible with 74LS564/574



DIP20(3D20A-P)

PIN ASSIGNMENT (TOP VIEW)

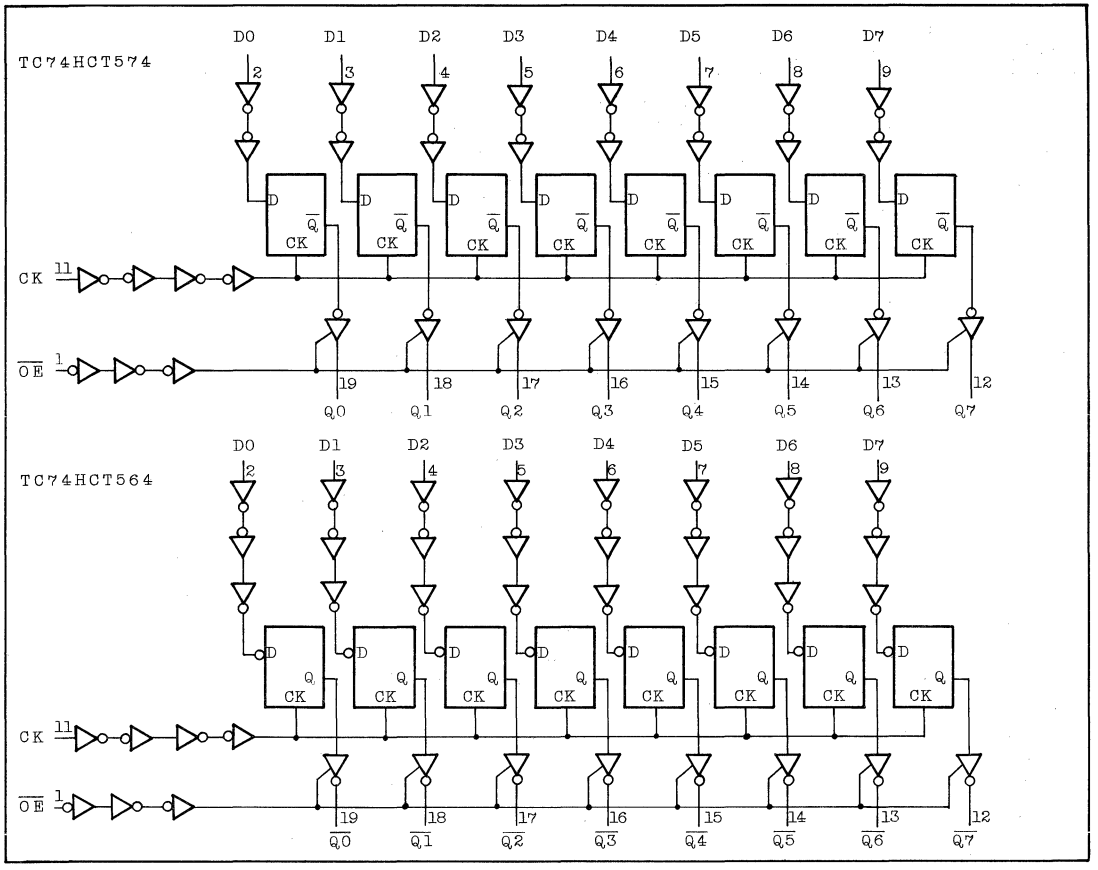


TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(HCT574)	$\overline{Q}$(HCT564)
H	X	X	HZ	HZ
L	↓	X	Qn	Qn
L	↑	L	L	H
L	↑	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE
Qn : NO CHANGE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

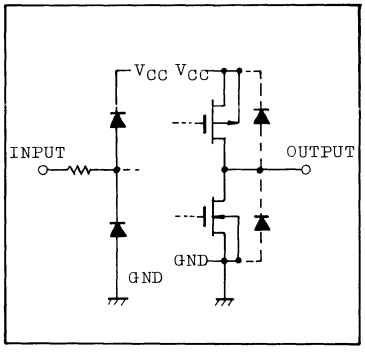
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10 sec)	T_L	300	°C

* 500mW in the ragne of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ≤ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ≤ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		4.5	-	26	41	-	51	ns
Maximum Clock Frequency	f_{MAX}		4.5	25	38	-	20	-	MHz
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		4.5	-	8	15	-	19	ns
Minimum Set-up Time	t_s		4.5	-	1	10	-	13	ns
Minimum Hold Time	t_h		4.5	-	-	5	-	5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Quiescent Supply Current	C_{PD}(1)	TC74HCT564		-	60	-	-	-	pF
		TC74HCT574		-	57	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

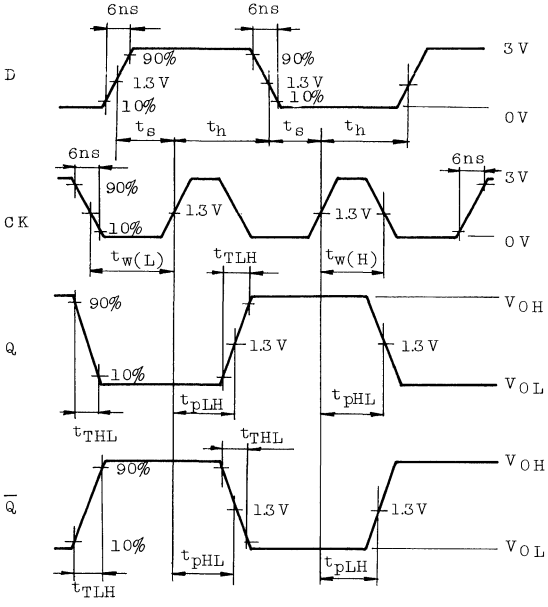
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Flip-Flop)}$$

And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation.

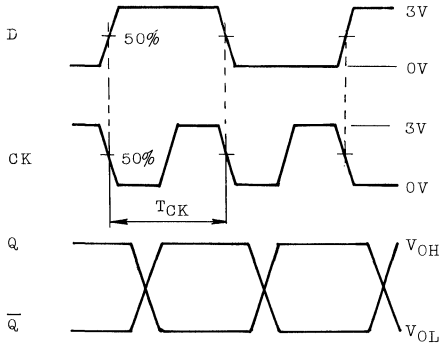
$$C_{PD}(TOTAL)=40+20\times N \ [pF] \quad (TC74HCT564)$$
$$C_{PD}(TOTAL)=37+20\times N \ [pF] \quad (TC74HCT574)$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



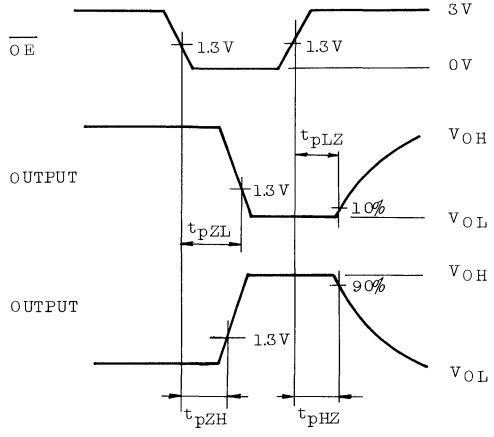
f_{MAX}.

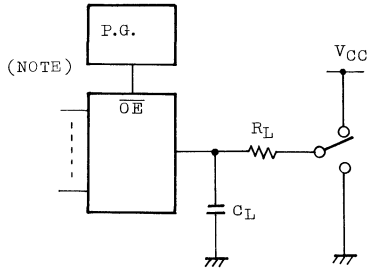


{CLOCK DUTY : 50%

$f_{MAX} = \frac{1}{T_{CK}}$

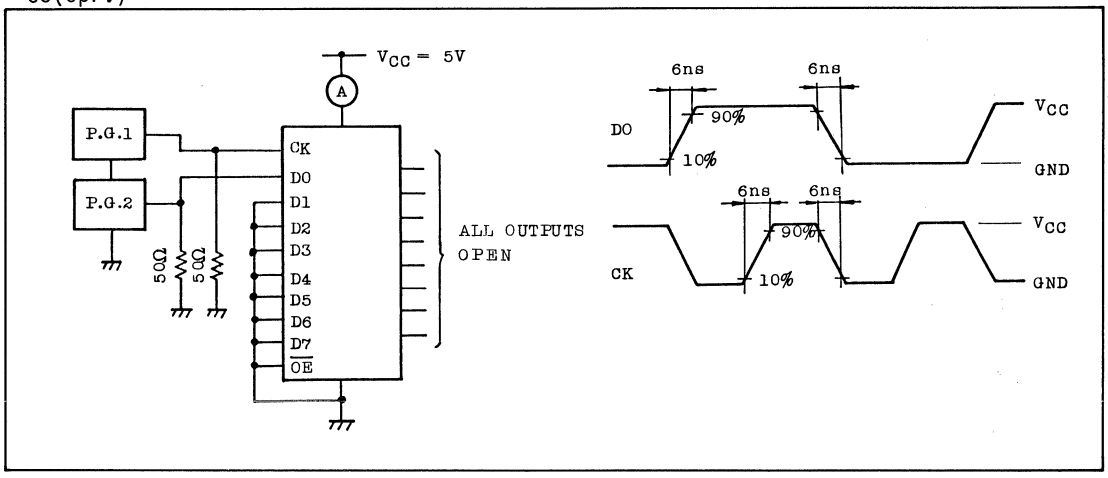
t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}





(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

I_{CC}(Opr.) TEST CIRCUIT

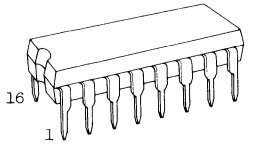


TC74HC590P 8-BIT BINARY COUNTER/REGISTER WITH 3-STATE OUTPUTS

The TC74HC590 is a high speed CMOS 8-bit counter/register fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level. If Counter Clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronous to clock. Data of the internal counter are loaded to register at positive edge of Register Clock (RCK) and Outputs are controlled by Enable Control ($\overline{G}$). All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .... 10 LSTTL Loads (For RCO)
  15 LSTTL Loads (For QA∿QH)
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA∿QH Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For RCO Output
- Balanced Propagation Delays ..... $t_{pLH}\doteqdot t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with LSTTL(74LS590)



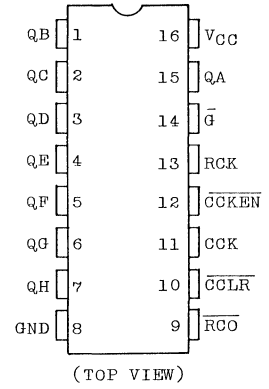
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 for QA∿QH ±20 for $\overline{RCO}$	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{STG}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

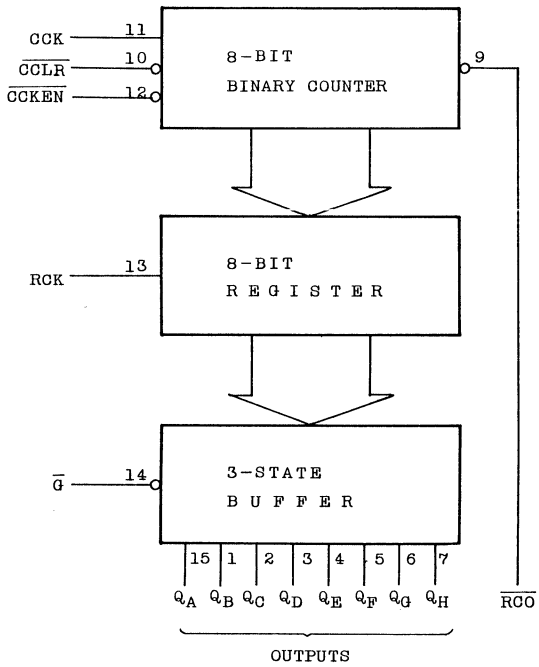
INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↓	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	↑	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↓	ADVANCE ONE COUNT.
X	X	H	L	↑	NO COUNT
X	X	H	H	X	NO COUNT

X: Don't care

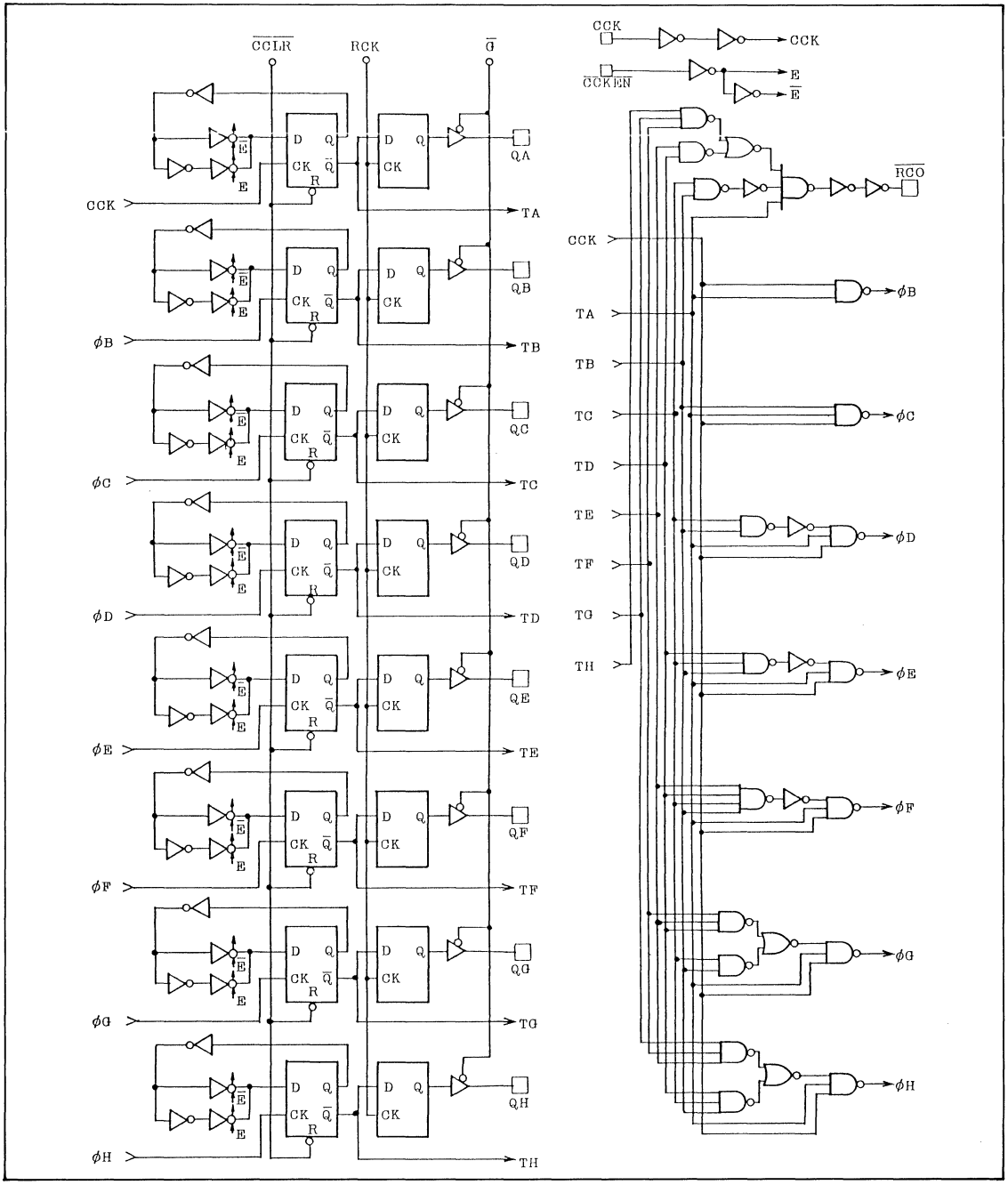
$\overline{RCO} = QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'$

(QA' ∿ QH': Internal outputs of the counter)

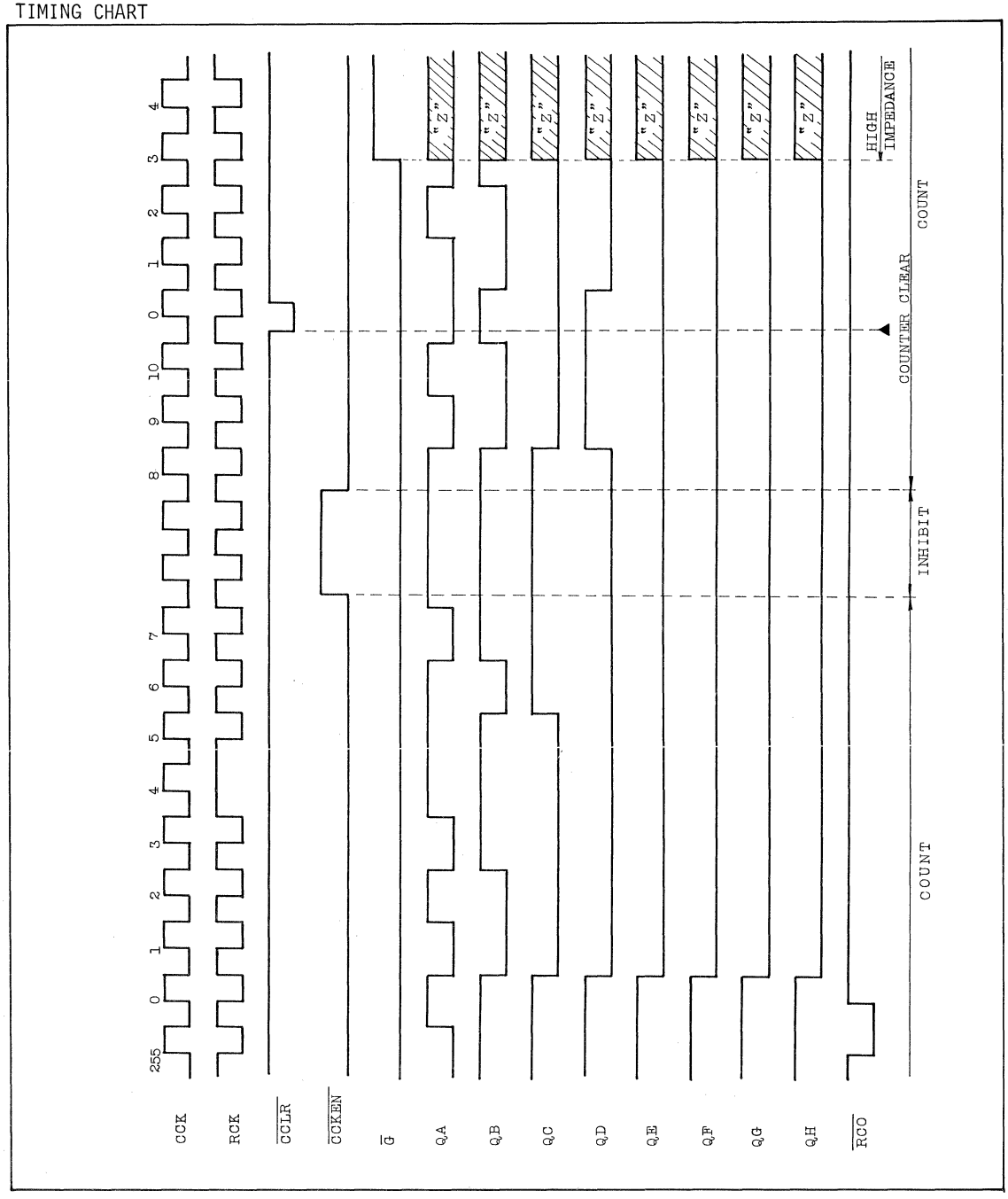
BLOCK DIAGRAM



LOGIC DIAGRAM



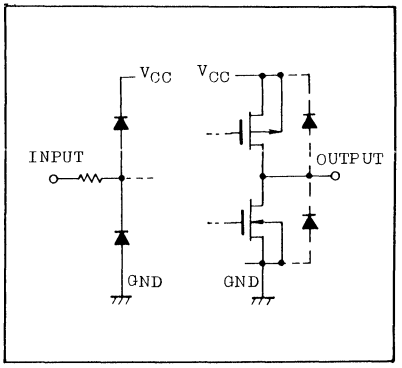
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	-.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (CCLR - $\overline{RCO}$)	t_{pLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	32	-	16	-	
			6.0	24	38	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	48	125	-	160	ns
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	92	200	-	250	
			4.5	-	23	40	-	50	
			6.0	-	20	34	-	43	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Minimum Hold Time	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	RL=1kΩ	2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	RL=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	

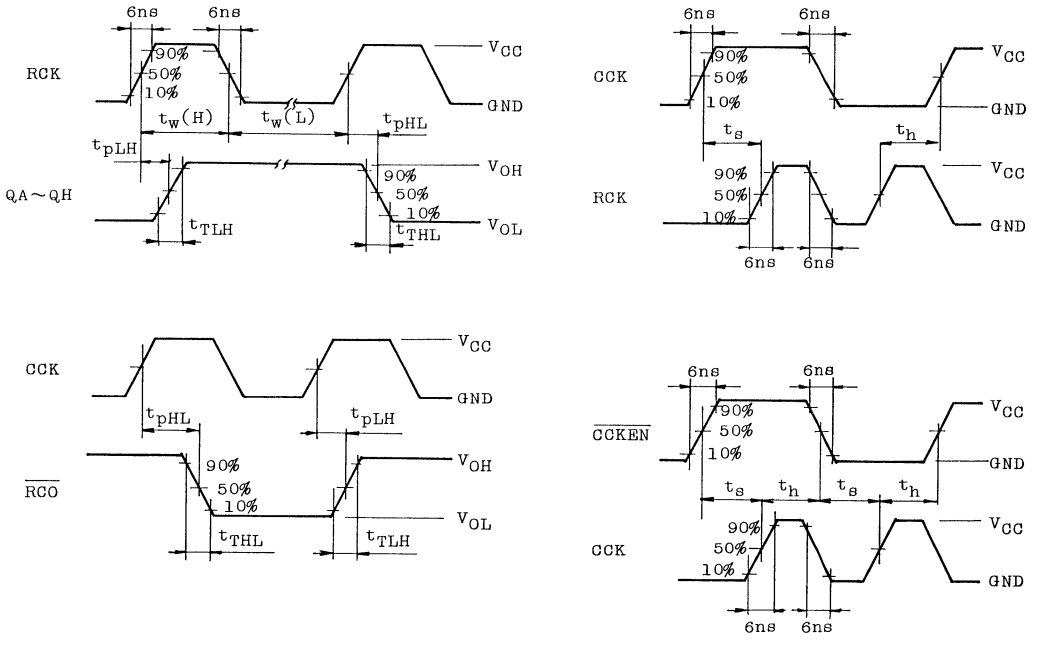
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40∿85°C		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}		-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$		-	95	-	-	-	

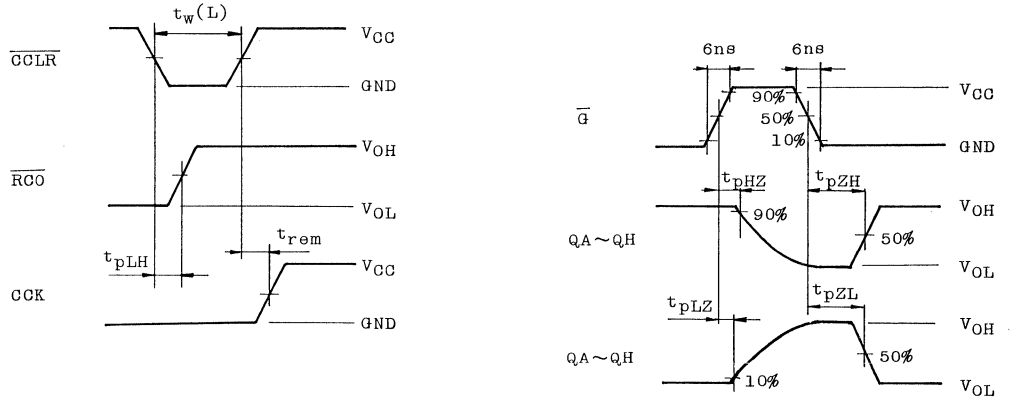
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

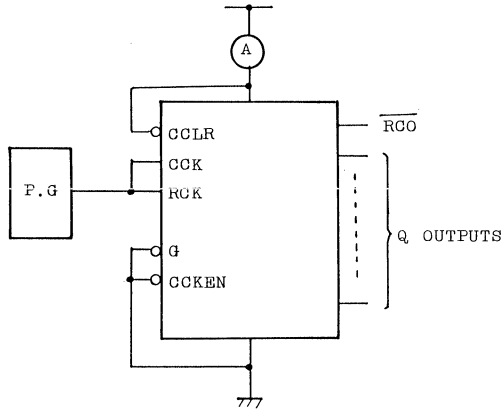
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST WAVEFORM



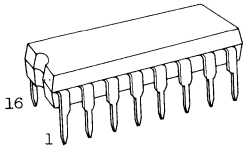
TC74HC592P

TC74HC592P 8-BIT BINARY COUNTER WITH INPUT REGISTER

The TC74HC592 is a high speed CMOS 8-bit register/counter fabricated with silicon gate C^2MOS technology.
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level.
If Counter clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronous to clock.
Input A∿H are loaded to register at positive edge of Register Clock (RCK), and register outputs are loaded to Counter when Counter Load ($\overline{CLOAD}$) is held "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=38MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with LSTTL(74LS592)



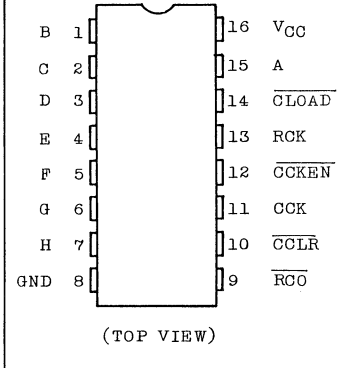
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

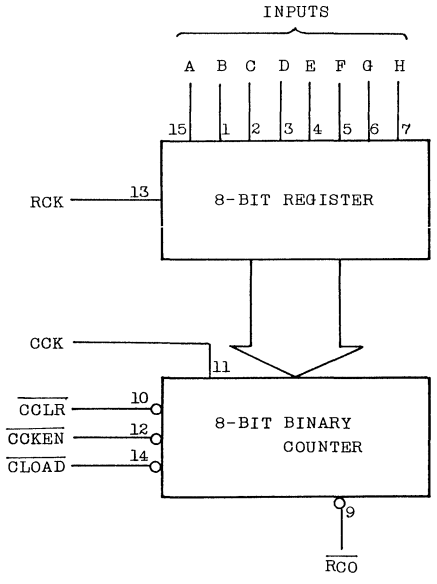
INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	REGISTER DATA IS LOADED INTO COUNTER.
X	H	L	X	X	COUNTER CLEAR
↓	H	H	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
↑	H	H	X	X	REGISTER STATE IS NOT CHANGED.
X	H	H	L	↓	COUNTER ADVANCES THE COUNT.
X	H	H	L	↑	NO COUNT
X	H	H	H	X	NO COUNT

X: Don't care

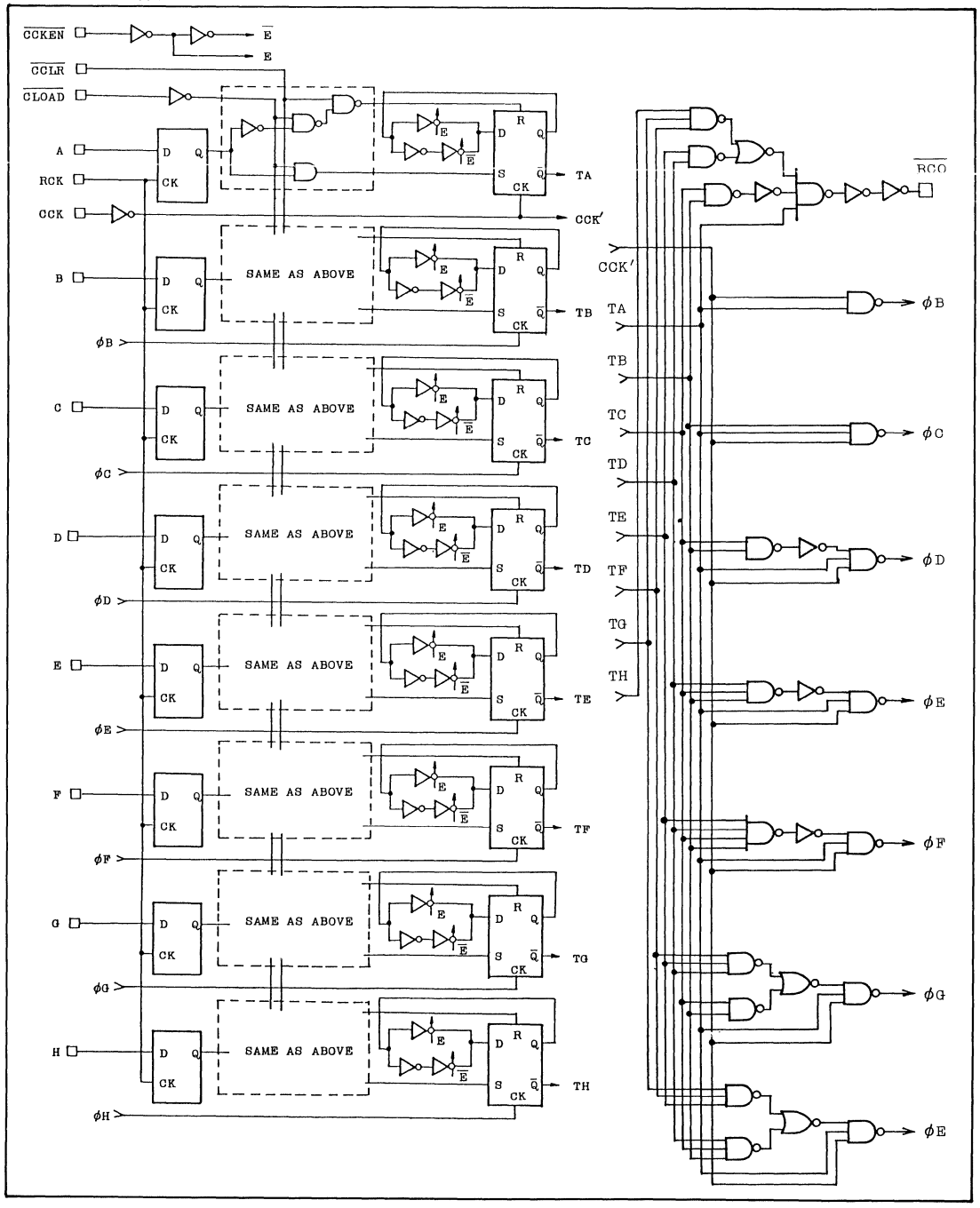
$\overline{RCO}=\overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA' ∿ QH'; Internal outputs of the counter)

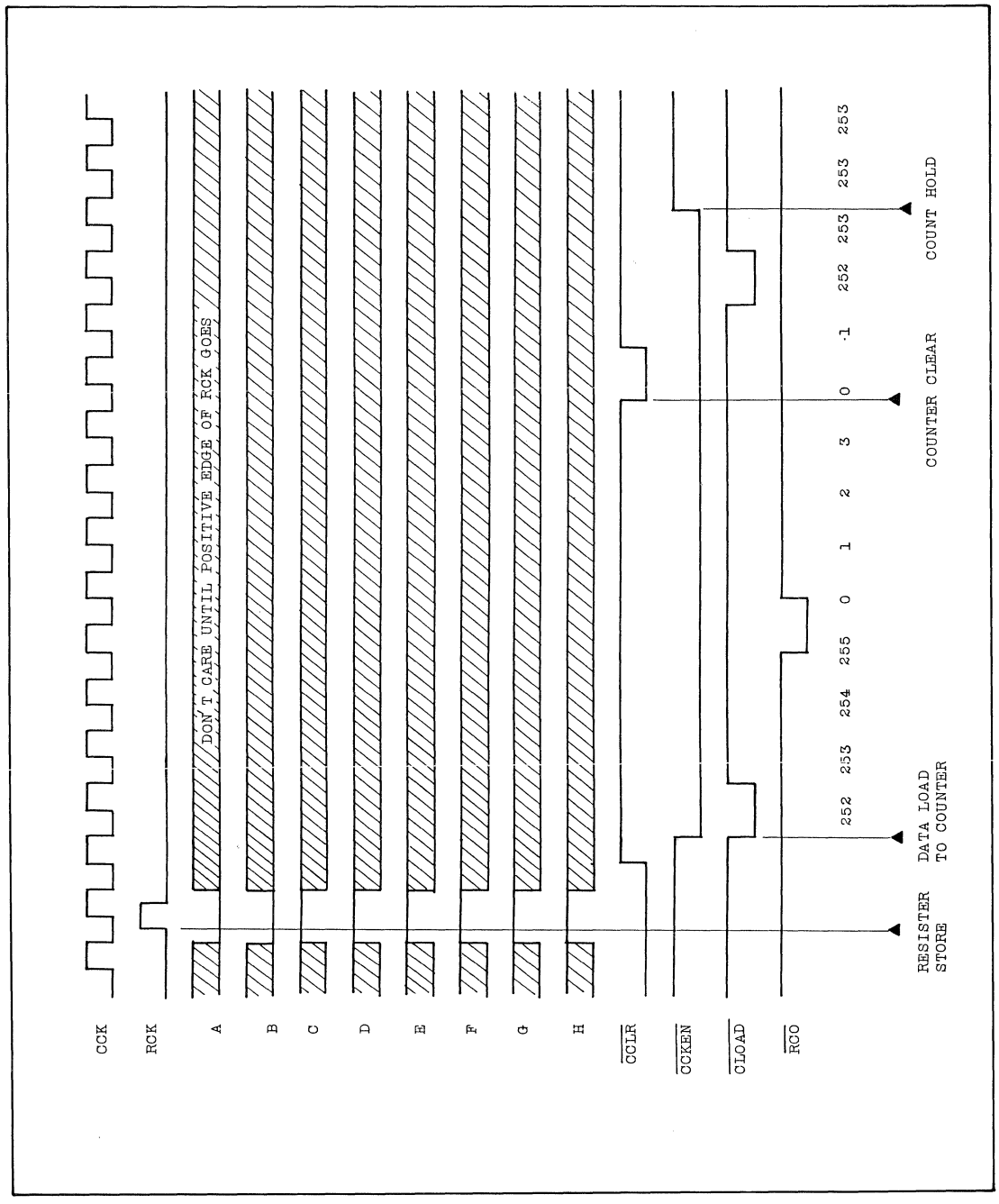
BLOCK DIAGRAM



LOGIC DIAGRAM



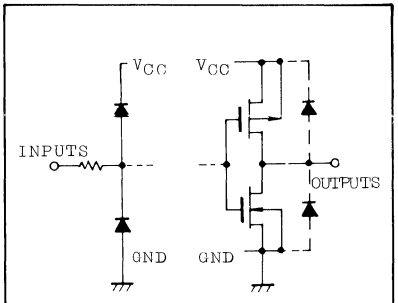
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CCK}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CLOAD}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	164	315	-	395	
			4.5	-	41	63	-	79	
			6.0	-	35	54	-	67	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (RCK - $\overline{RCO}$)	t_{pLH} t_{pHL}	$\overline{CLOAD}$="L"	2.0	-	188	360	-	450	
			4.5	-	47	72	-	90	
			6.0	-	40	61	-	77	
Maximum Clock Frequency	f_{MAX}		2.0	4	9	-	3.5	-	MHz
			4.5	22	34	-	18	-	
			6.0	26	42	-	21	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Pulse Width ($\overline{CLOAD}$)	$t_{w(L)}$		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Removal Time ($\overline{CLOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	t_s		2.0	-	32	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	17	-	16	
Minimum Set-up Time (RCK - $\overline{CLOAD}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Set-up Time (A∿H - RCK)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

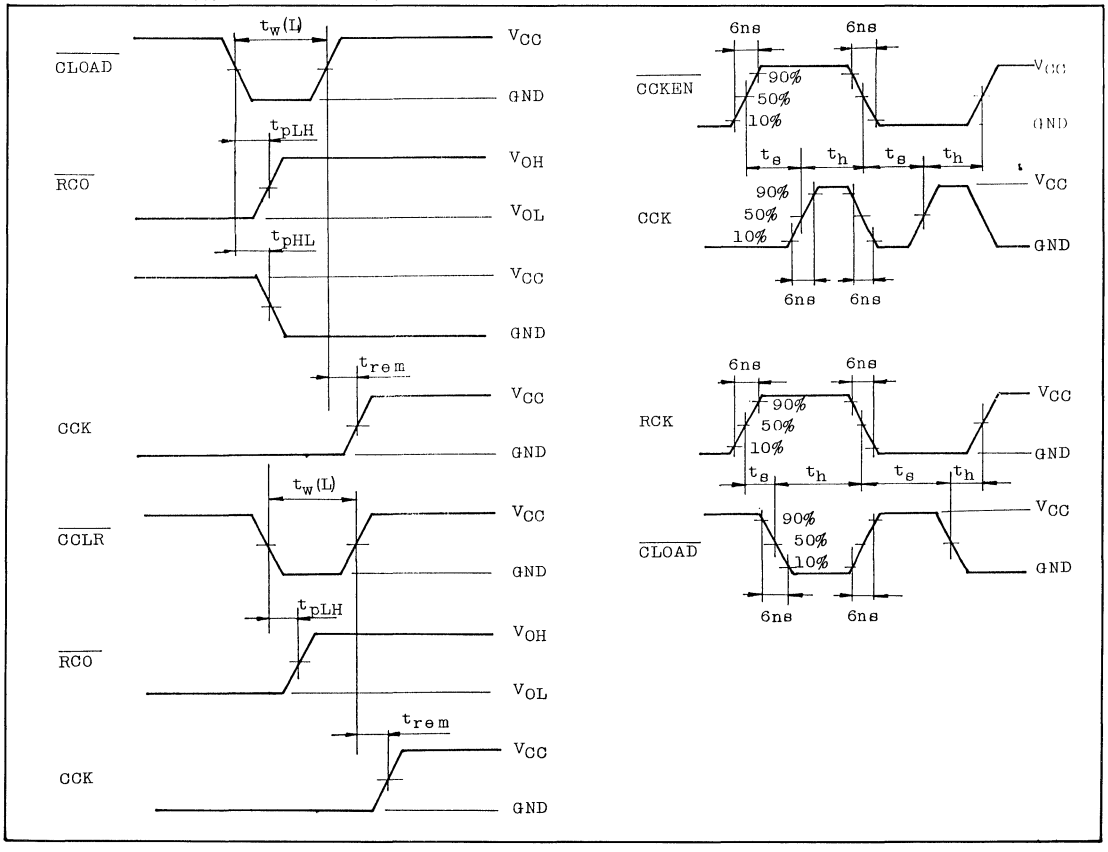
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Hold Time	t_h		2.0	-	-	25	-	30	ns
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	44	-	-	-	

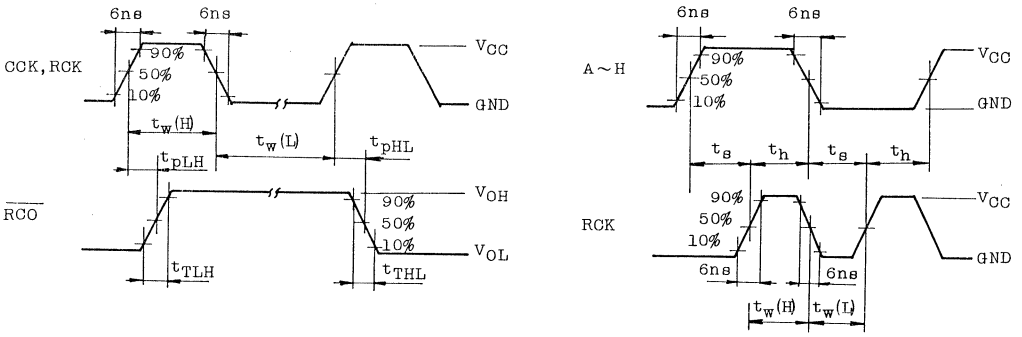
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

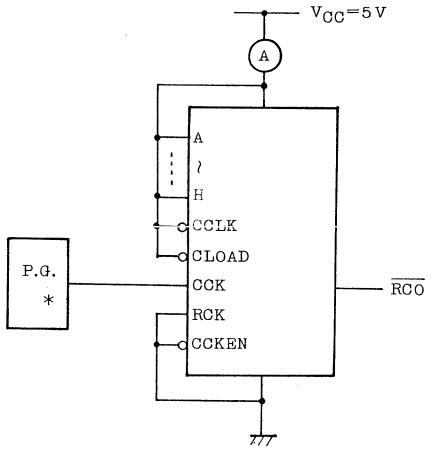
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT



TC74HC595AP/AF/AFN

8-BIT SHIFT REGISTER/LATCH(3-STATE)

The TC74HC595A is a high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

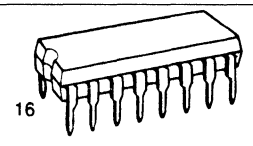
The TC74HC595A contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

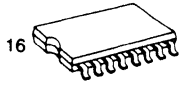
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

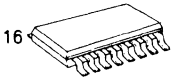
- High Speed ····· f_{MAX}=55MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For QH'
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QH'
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS595



DIP16 (3D16A-P)

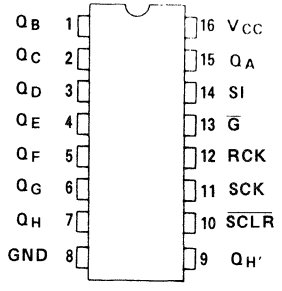


MFP 16
(F16GC-P)



SOP 16
(SOP16-P-225A)

PIN ASSIGNMENT



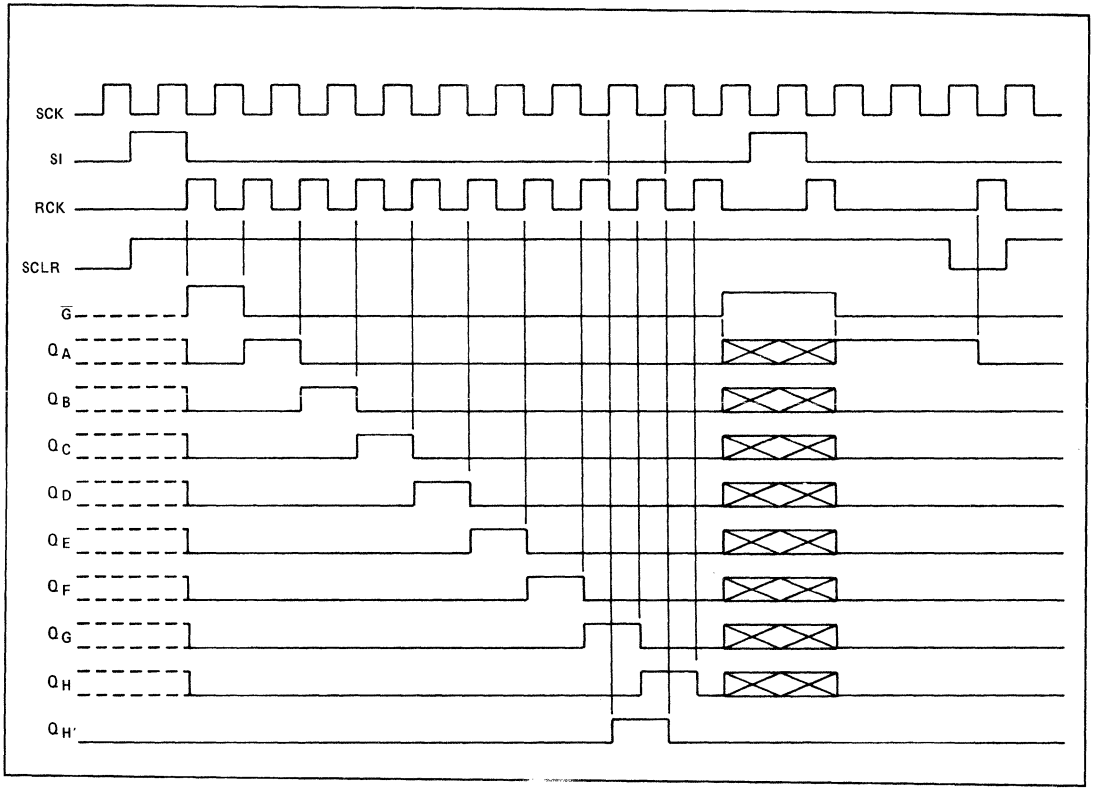
(TOP VIEW)

TRUTH TABLE

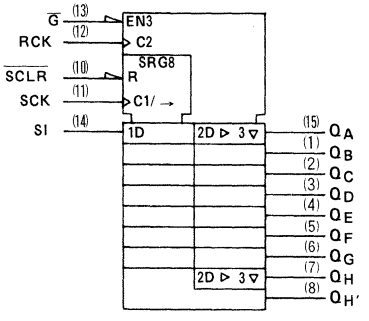
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

X : DON'T CARE

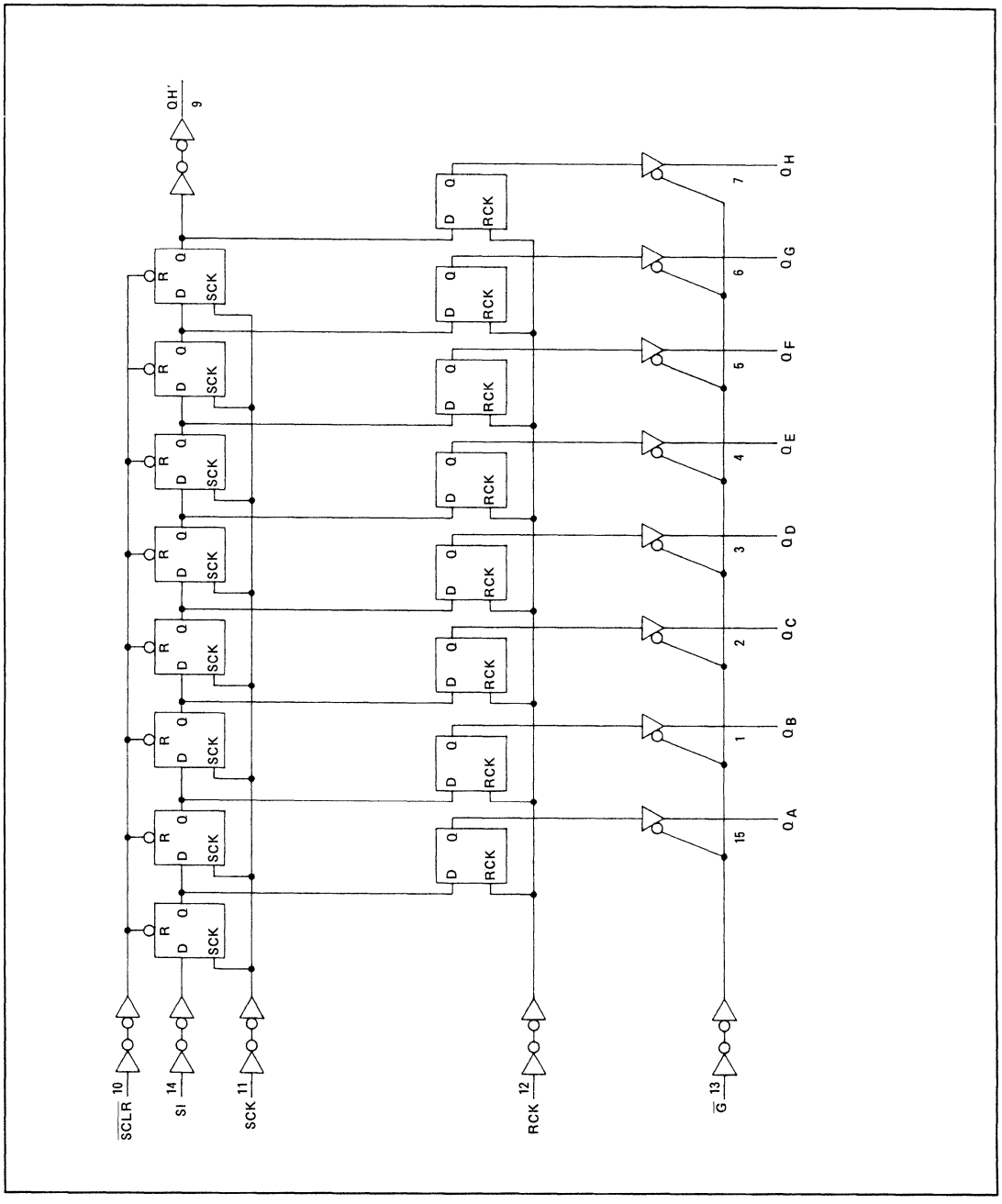
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (Q_H') / (Q_A~Q_H)	I_{OUT}	±25 / ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		Q_H'	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_A~Q_H	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		Q_H'	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_A~Q_H	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} =V_{IH} or V_{IL} V_{OUT} =V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK,RCK)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI−SCK)	t_s		2.0	−	50	165	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (SCK−RCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{SCLR}$−RCK)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{SCLR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	25	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Q_H')	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (SCK–Q_H')	t_{pLH} t_{pHL}		–	12	21	ns
Propagation Delay Time ($\overline{SCLR}$–Q_H')	t_{pLH} t_{pHL}		–	15	30	ns
Maximum Clock Frequency	f_{MAX}		35	77	–	MHz

AC ELECTRICAL CHARACTERISTICS(C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40 ~85°C MIN.	Ta=−40 ~85°C MAX.	UNIT
Output Transition Time (Qn)	t_{TLH} t_{THL}		50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Output Transition Time (Q_H')	t_{TLH} t_{THL}		50	2.0	–	30	75	–	95	
				4.5	–	8	15	–	19	
				6.0	–	7	13	–	16	
Propagation Delay Time (SCK–Q_H')	t_{pLH} t_{pHL}		50	2.0	–	45	125	–	155	
				4.5	–	15	25	–	31	
				6.0	–	13	21	–	26	
Propagation Delay Time ($\overline{SCLR}$–Q_H')	t_{pLH} t_{pHL}		50	2.0	–	60	175	–	220	
				4.5	–	18	35	–	44	
				6.0	–	15	30	–	37	
Propagation Delay Time (RCK–Qn)	t_{pLH} t_{pHL}		50	2.0	–	60	150	–	190	
				4.5	–	20	30	–	38	
				6.0	–	17	26	–	32	
			150	2.0	–	75	190	–	240	
				4.5	–	25	38	–	48	
				6.0	–	22	32	–	41	
Output Enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	–	45	135	–	170	
				4.5		15	27	–	34	
				6.0	–	13	23	–	29	
			150	2.0	–	60	175	–	220	
				4.5	–	20	35	–	44	
				6.0	–	17	30	–	37	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	–	30	150	–	190	
				4.5	–	15	30	–	38	
				6.0	–	14	26	–	33	
Maximum Ciock Frequency	f_{MAX}		50	2.0	6	17	–	5	–	MHz
				4.5	30	50	–	25	–	
				6.0	35	59	–	28	–	
Input Capacitance	C_{IN}				–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)				–	184	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

8-BIT LATCH/SHIFT REGISTER(3-STATE)

The TC74HC597A is a high speed CMOS 8-BIT PARALLEL-IN/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

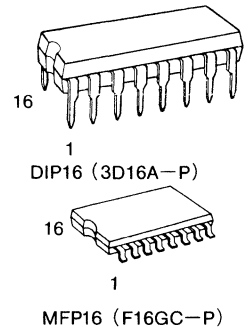
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of an 8-bit data register feeding an 8-bit shift register. The parallel data on the A~H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{SLOAD}$ input is held low, the input register data is passed into the shift registers. When $\overline{SLOAD}$ input is held high, the serial data input (SI) is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear input ($\overline{SCLR}$) sets the 8-bit shift register to zero.

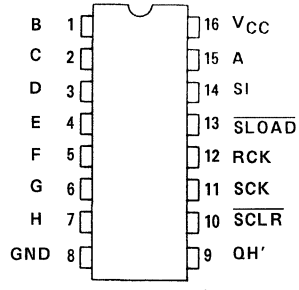
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS597



PIN ASSIGNMENT

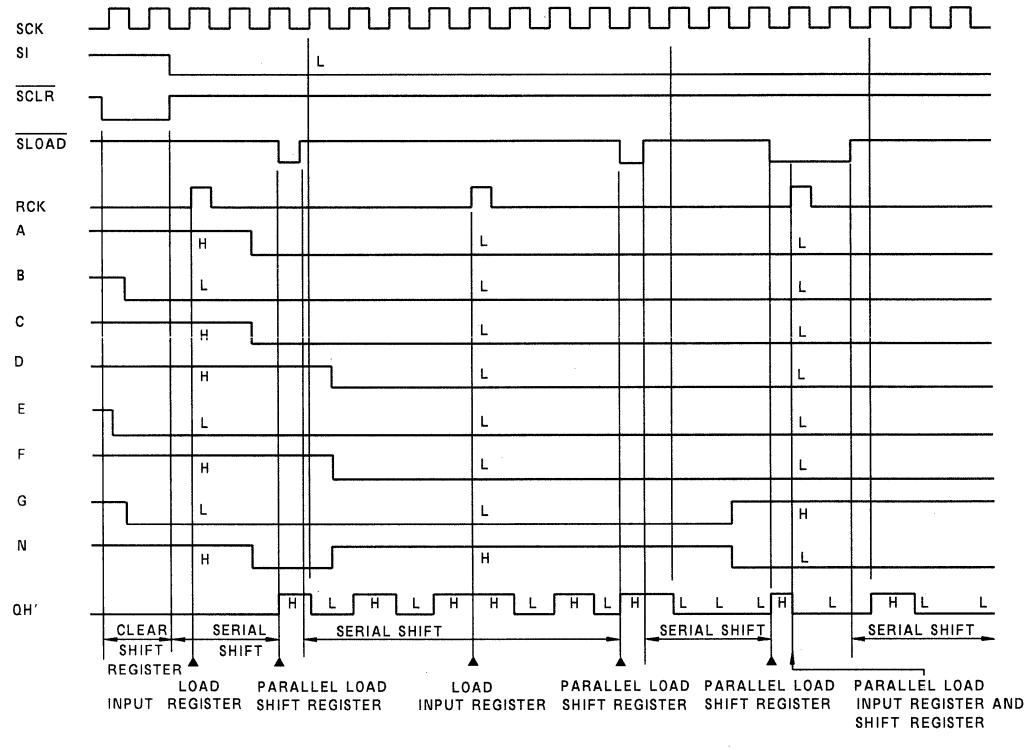


TRUTH TABLE

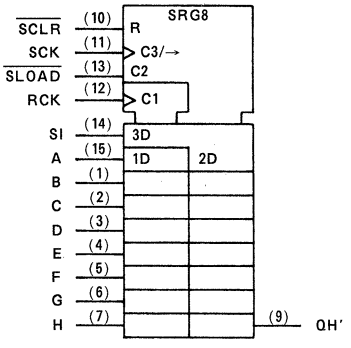
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S. R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S. R.
L	↓	H	H	X	First stage of S. R. become "L". Other stages store the data of previous stage, respectively.
H	↓	H	H	X	First stage of S. R. become "H". Other stages store the data of previous stage, respectively.
X	↓	H	H	X	State of S. R. is not changed.
X	X	X	X	↓	Input data on A~H line is stored into input register
X	X	X	X	↓	Storage register state is not changed.

X : DON'T CARE

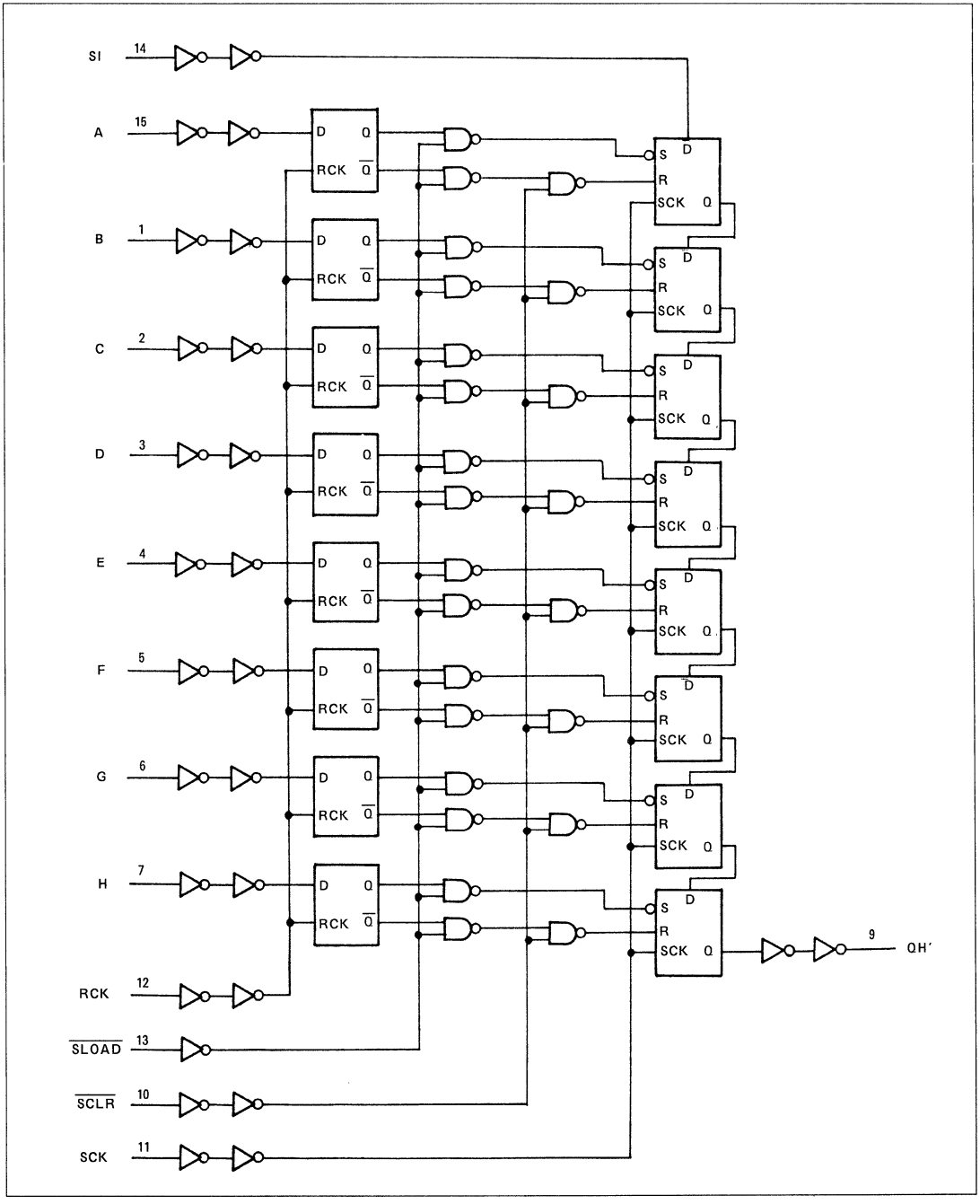
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(FMP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ～85℃ LIMIT	UNIT
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SLOAD}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (RCK−$\overline{SLOAD}$)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (SI−SCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (PI−RCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{SCLR}$, $\overline{SLOAD}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	5	8	ns
Propagation Delay Time (SCK−QH')	t_{pLH} t_{pHL}		−	16	25	
Propagation Delay Time ($\overline{SCLR}$−QH')	t_{pLH} t_{pHL}		−	20	32	
Propagation Delay Time ($\overline{SLOAD}$−QH')	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (RCK−QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ ="L"	−	25	37	
Maximum Clock Frequency	f_{MAX}		30	59	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	32	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (SCK−QH')	t_{pLH} t_{pHL}		2.0	−	78	145	−	180	
			4.5	−	20	29	−	36	
			6.0	−	16	25	−	31	
Propagation Delay Time ($\overline{SCLR}$−QH')	t_{pLH} t_{pHL}		2.0	−	90	175	−	220	
			4.5	−	24	35	−	44	
			6.0	−	20	30	−	37	
Propagation Delay Time ($\overline{SLOAD}$−QH')	t_{pLH} t_{pHL}		2.0	−	80	175	−	220	
			4.5	−	22	35	−	44	
			6.0	−	18	30	−	37	
Propagation Delay Time (RCK−QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ ="L"	2.0	−	112	210	−	265	
			4.5	−	30	42	−	53	
			6.0	−	24	36	−	45	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	−	5	−	MHz
			4.5	30	48	−	24	−	
			6.0	35	50	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	60	−	−	−	

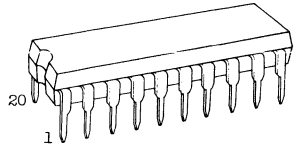
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC620P
TC74HC623P

OCTAL BUS TRANSCEIVER
TC74HC620P 3-STATE, INVERTING
TC74HC623P 3-STATE, NON-INVERTING

The TC74HC620 and TC74HC623 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by GAB, $\overline{GBA}$, GAB and $\overline{GBA}$ inputs are equipped with protection circuits against static discharge or transient excess voltage.



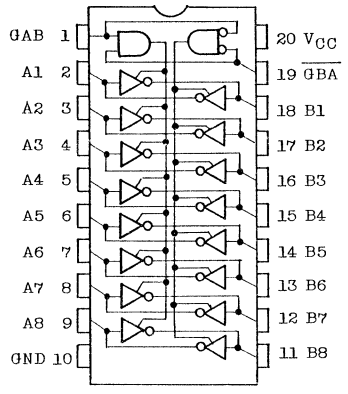
DIP20(3D20A-P)

FEATURES:

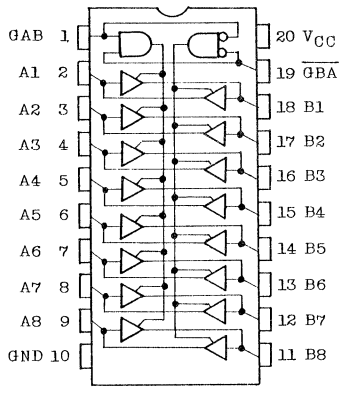
- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Disspation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .. $|I_{OH}|=I_{OL}$=6mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS620/623

PIN ASSIGNMENT (TOP VIEW)

TC74HC620



TC74HC623



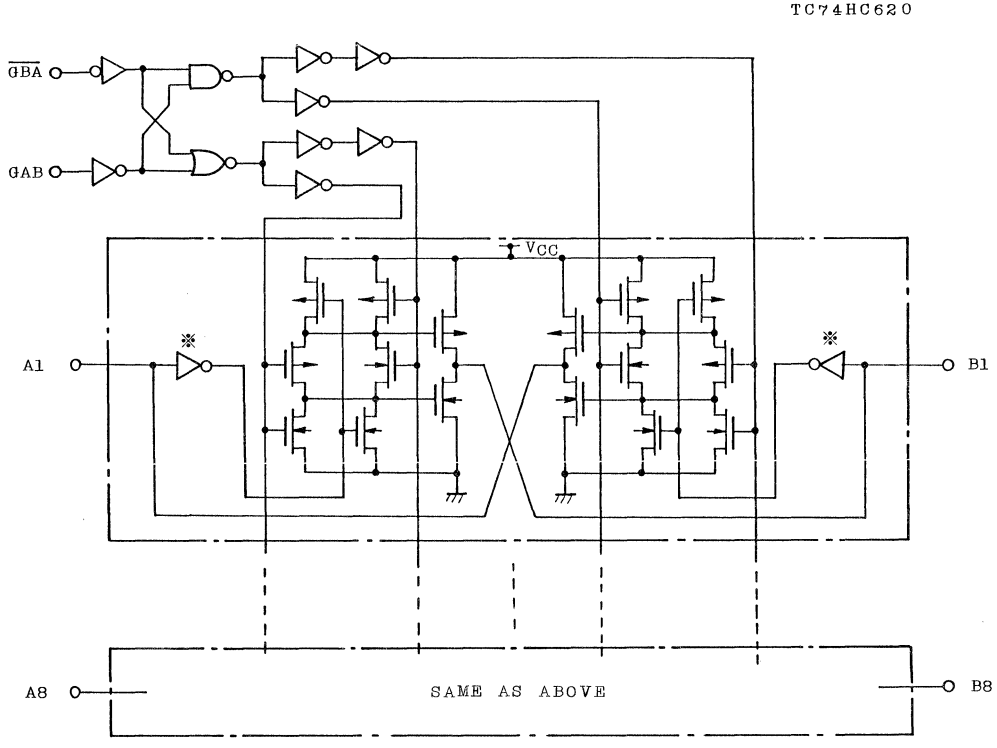
NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A Bus	B Bus	HC620	HC623
L	L	Output	Input	$A = \overline{B}$	A = B
H	H	Input	Output	$B = \overline{A}$	B = A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

LOGIC DIAGRAM



Note: In case of TC74HC623, input inverters marked ※ at A bus and B bus are eliminated respectively.

ABSOLUTE MAXIMUM RATINGS

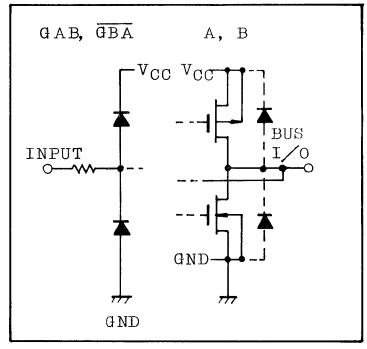
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Bus Terminal 3-State Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Lekage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to GAB, $\overline{GBA}$ input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

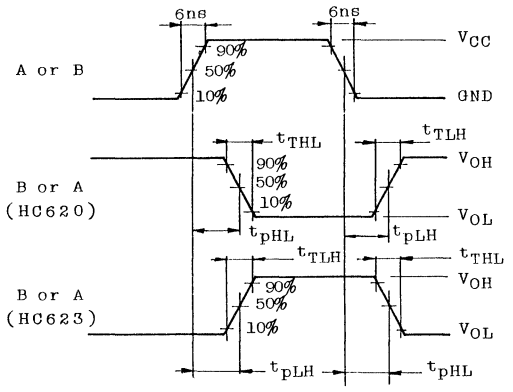
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Dealy Time **	t_{pLH} t_{pHL}		2.0	-	40	85	-	105	
			4.5	-	11	17	-	21	
			6.0	-	10	14	-	18	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	74	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	10	26	-	33	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	100	180	-	225	
			4.5	-	25	36	-	45	
			6.0	-	21	31	-	38	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC620		-	40	-	-	-	
		TC74HC623		-	35	-	-	-	

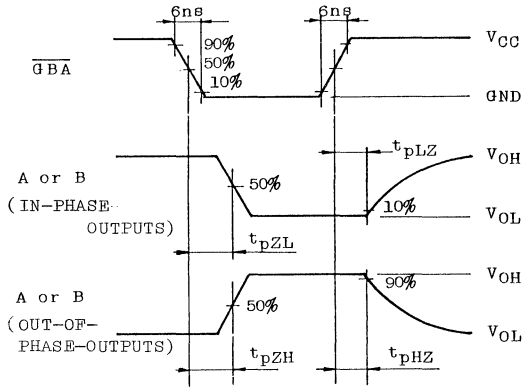
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN}$$

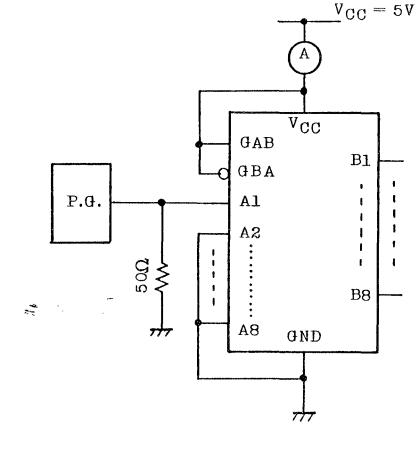
(2) * TC74HC620 ** TC74HC623

SWITCHING CHARACTERISTICS TEST WAVEFORM





$I_{CC(Opr.)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC646AP
TC74HC648AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HC646AP NON-INVERTING
TC74HC648AP INVERTING

The TC74HC646A/648A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

When the direction input (DIR) is held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the DIR input is held low, the A1 thru A8 become outputs and the B1 thru B8 become inputs.

The enable input $\overline{G}$ is held high, both the A Bus and B Bus become high impedance.

The select inputs (SAB, SBA) can multiplex stored and real-time (transparent mode) data.

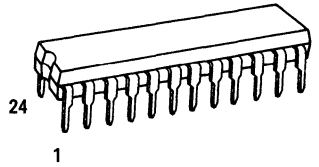
Data on the A Bus or B Bus can be clocked into the registers on the positive going transition of either CAB or CBA clock inputs, respectively.

The TC74HC646A is a non-inverting output type while the TC74HC648A is of the inverting output type.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

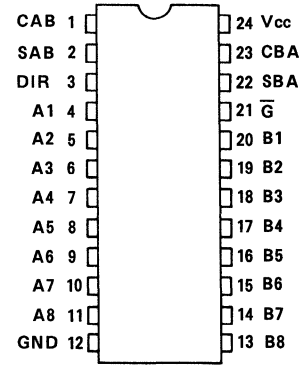
FEATURES:

- High Speed ····· f_{MAX}=73MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS646/648.



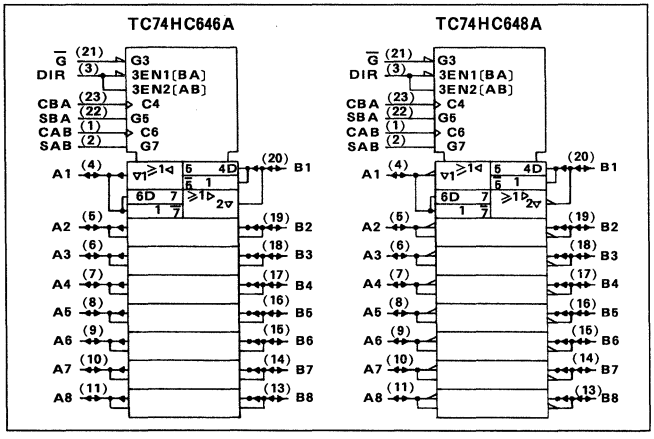
DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

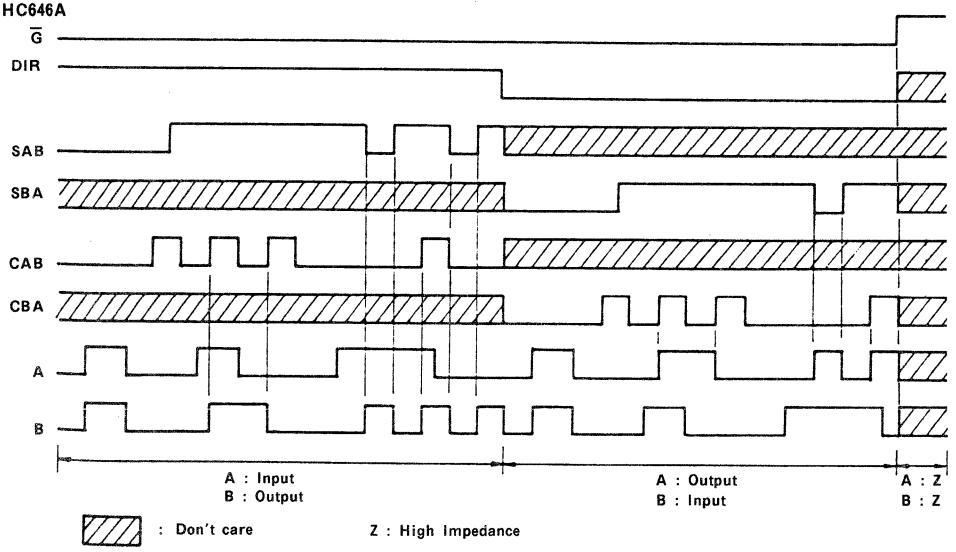
TC74HC646A (The truth table for TC74HC648A is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X	X	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip–flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip–flops on the rising edge of CAB.
		X	X*	H	X	X	Qn	The data in the A storage flip–flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip–flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip–flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip–flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip–flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes: X: Don't Care
Qn: The data stored into the internal flip–flops by most recent low to high transition of the clock inputs.
Z: High Impedance
* The clocks are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and/or B Busses may be clocked into the storage flip–flops at any time.

TIMING CHART

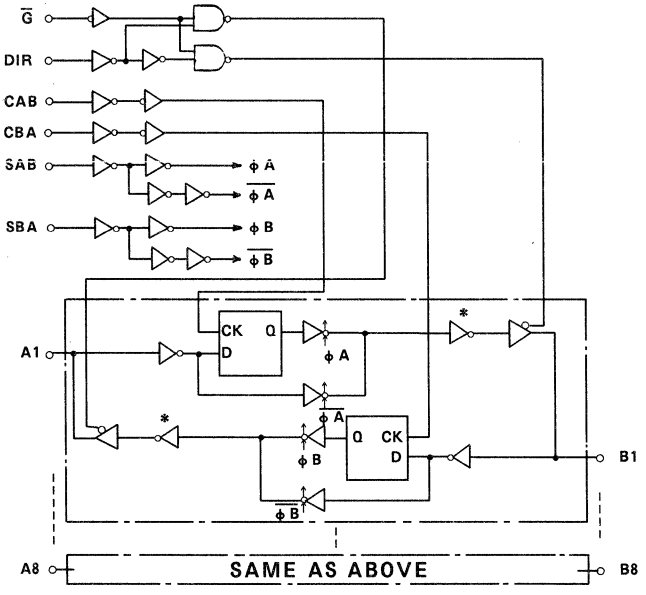
TC74HC646A



Note: The timing chart for TC74HC648A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HC648A



Note: In case of TC74HC646A output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIRMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (BUS−BUS)	t_{pLH} t_{pHL}		50	2.0	−	74	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
			150	2.0	−	91	190	−	240	
				4.5	−	26	38	−	48	
				6.0	−	22	32	−	41	
Propagation Delay Time (CAB,CBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
			150	2.0	−	116	250	−	315	
				4.5	−	33	50	−	63	
				6.0	−	28	43	−	54	
Propagation Delay Time (SAB,SBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	81	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	20	29	−	37	
			150	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
Output Enable time ($\overline{G}$,DIR−BUS)	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	84	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	20	30	−	37	
			150	2.0	−	102	215	−	270	
				4.5	−	29	43	−	54	
				6.0	−	25	37	−	46	
Output Disable time ($\overline{G}$,DIR−BUS)	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	60	175	−	220	
				4.5	−	23	35	−	44	
				6.0	−	20	30	−	37	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	−	19	6	−	5	MHz
				4.5	−	67	31	−	25	
				6.0	−	79	36	−	29	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8 \text{(per bit)}$$

TC74HCT646AP
TC74HCT648AP

OCTAL BUS TRANSCEIVER/REGISTER

TC74HCT646AP NON-INVERTING
TC74HCT648AP INVERTING

The TC74HCT646A/HCT648A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

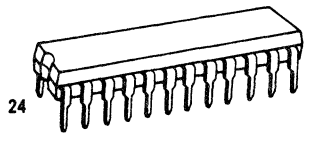
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74HCT646A is a non-inverting output type while the TC74HCT648A is of the inverting output type.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

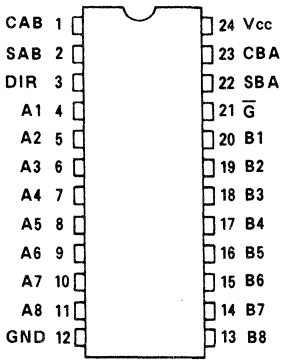
FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- Compatible with TTL Output ····· V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648



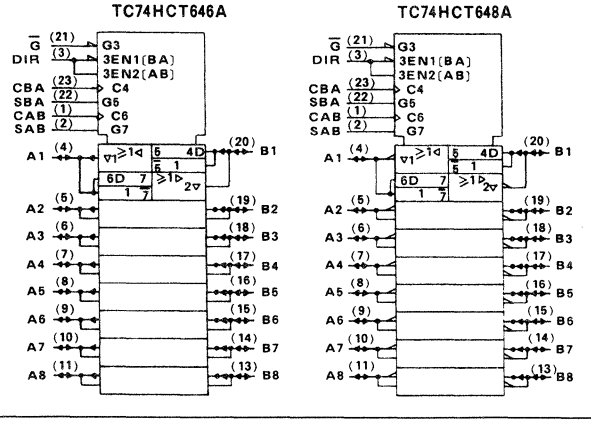
DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

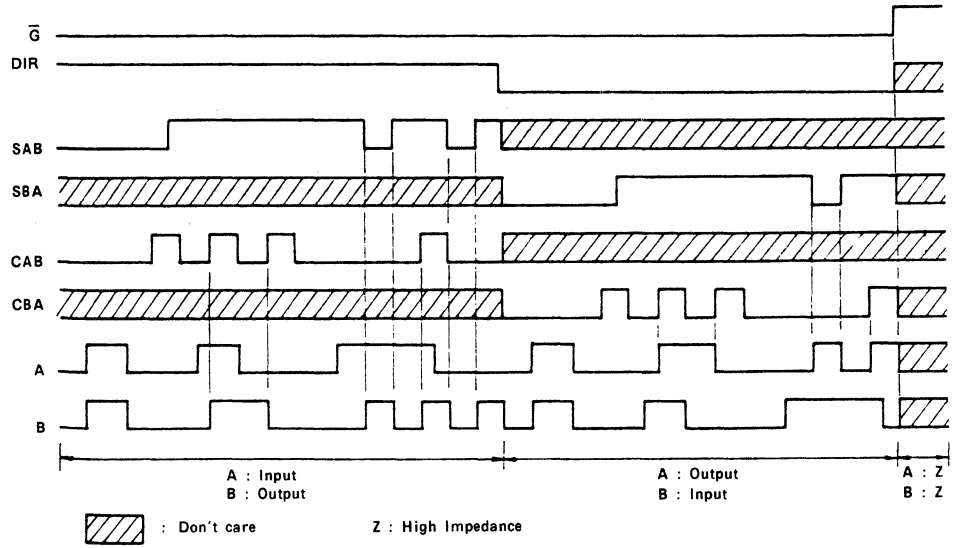
TC74HCT646A(The truth table for TC74HCT648A is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
* The clock are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and /or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

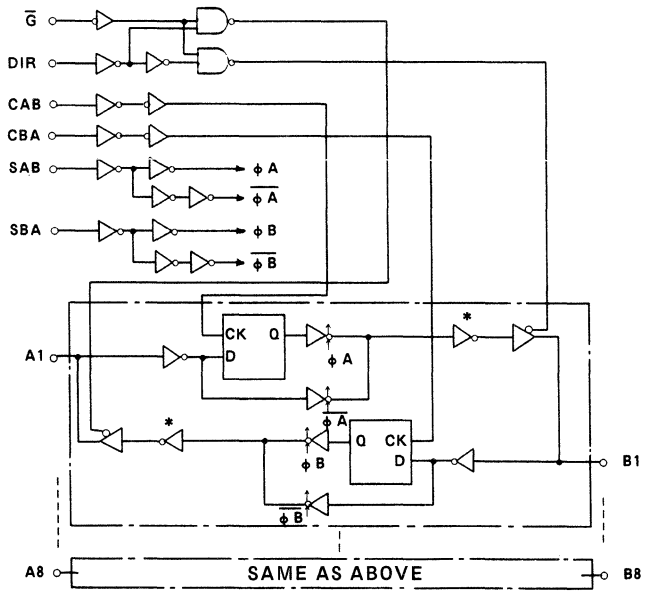
TC74HCT646A



Note: The timing chart for TC74HCT648A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HCT648A



Note: In case of TC74HCT646A output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ～ 7	V
DC Input Voltage	V_{IN}	−0.5 ～V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ～V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ～150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5～5.5	V
Input Voltage	V_{IN}	0～V_{CC}	V
Output Voltage	V_{OUT}	0～V_{CC}	V
Operating Temperature	Topr	−40～85	℃
Input Rise and Fall Time	t_r, t_f	0～500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ～ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ～ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH}= −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}= −6 μA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=6 μA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	I_C	Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		4.5	−	15	19	ns
	$t_{W(H)}$		5.5	−	14	17	
Minimum Set−up Time	t_s		4.5	−	10	13	ns
			5.5	−	9	12	
Minimum Hold Time	t_h		4.5	−	5	5	ns
			5.5	−	5	5	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time (BUS−BUS)	t_{pLH}		50	4.5	−	20	30	−	38	
				5.5	−	17	27	−	34	
	t_{pHL}		150	4.5	−	25	38	−	48	
				5.5	−	22	34	−	43	
Propagation Delay Time (CAB, CBA−BUS)	t_{pLH}		50	4.5	−	29	44	−	55	
				5.5	−	26	40	−	50	
	t_{pHL}		150	4.5	−	34	52	−	65	
				5.5	−	31	47	−	59	
Propagation Delay Time (SAB, SBA−BUS)	t_{pLH}		50	4.5	−	24	34	−	43	
				5.5	−	21	31	−	39	
	t_{pHL}		150	4.5	−	29	42	−	53	
				5.5	−	26	38	−	46	
Output Enable time (DIR, $\overline{G}$−BUS)	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	26	38	−	48	
				5.5	−	23	34	−	43	
	t_{pZH}		150	4.5	−	31	46	−	58	
				5.5	−	28	41	−	52	
Output Enable time (DIR, $\overline{G}$−BUS)	t_{pLZ}	$R_L=1k\Omega$	50	4.5	−	26	35	−	44	
	t_{pHZ}			5.5	−	23	32	−	40	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	55	−	25	−	MHz
				5.5	37	61	−	30	−	
Input Capacitance	C_{IN}	DIR, $\overline{G}$, SAB, SBA, CAB, CBA			−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT646A			−	40	−	−	−	
		TC74HCT648A			−	39	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HC651AP
TC74HC652AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HC651AP INVERTING
TC74HC651AP NON-INVERTING

The TC74HC651A/652A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuiry arranged for multiplexed transmission of data directly from the internal registers.

When the enable inputs GAB and $\overline{GBA}$ are held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the GAB and $\overline{GBA}$ are held low, the A1 thru A8 become outputs and the B1 thru B8 become inputs. When GAB is low and $\overline{GBA}$ is high, the outputs functions of the A and B Busses are disabled.

The select inputs (SAB,SBA) can multiplex stort and real-time(transparent mode)data.

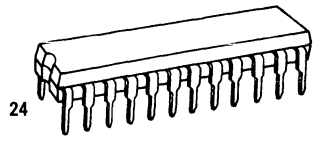
Data on the A Bus or B Bus can be clocked into the registers on the positive ging transition of either CAB or CAB clock inputs, respectively.

The TC74HC651A is of the inverting output type while the TC74HC652A is a non-inverting output type.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

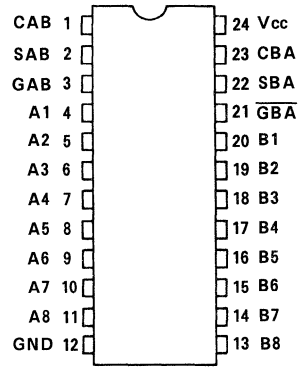
FEATURES:

- High Speed ····· f_{MAX}=73MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS651/652.



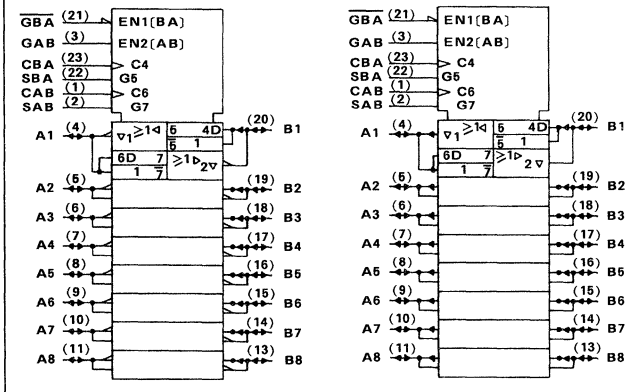
DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

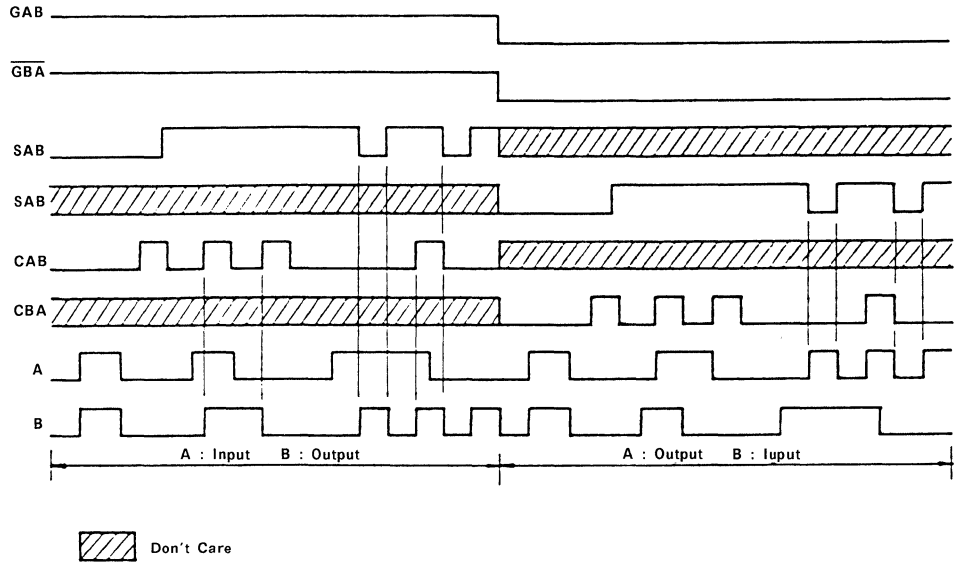
TC74HC652A (The truth table for TC74HC651A is the same, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of the A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip–flops. Data on the Bus will be stored on the rising edge of the Clock.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip–flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip–flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip–flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip–flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip–flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip–flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data in the A storage flip–flops are displayed on the B Bus, and the data in the B storage flip–flops are displayed onthe A

Notes: X: Don't Care Qn: The data stored into the internal flip–flops by most recent low to high transition of the clock inputs. Z: High Impedance * The clocks are not internally gated with either Output Enables or Select Inputs. Therfore, data on the A and/or B Busses may be clocked into the storage flip–flops at any time.

TIMING CHART

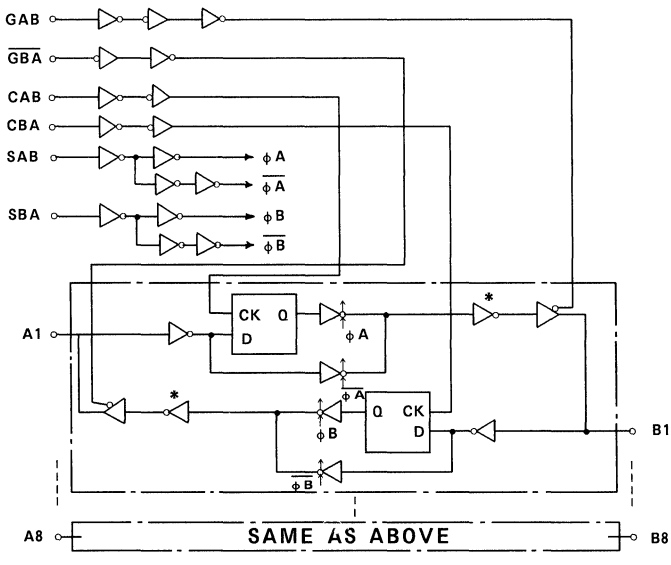
TC74HC652A



Note: The timing chart for TC74HC651A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HC651A



Note: In case of TC74HC652A output inverter marked * at A bus and B bus areeliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIRMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (BUS−BUS)	t_{pLH} t_{pHL}		50	2.0	−	74	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
			150	2.0	−	91	190	−	240	
				4.5	−	26	38	−	48	
				6.0	−	22	32	−	41	
Propagation Delay Time (CAB,CBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
			150	2.0	−	116	250	−	315	
				4.5	−	33	50	−	63	
				6.0	−	28	43	−	54	
Propagation Delay Time (SAB,SBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	81	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	20	29	−	37	
			150	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
Output Enable time (GAB,$\overline{GBA}$−BUS)	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	74	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	
			150	2.0	−	91	215	−	270	
				4.5	−	26	43	−	54	
				6.0	−	22	37	−	46	
Output Disable time (GAB,$\overline{GBA}$−BUS)	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	50	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	−	19	6	−	5	MHz
				4.5	−	67	31	−	25	
				6.0	−	79	36	−	29	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

OCTAL BUS TRANSCEIVER/REGISTER

TC74HCT651AP NON-INVERTING
TC74HCT652AP INVERTING

The TC74HCT651A/HCT652A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

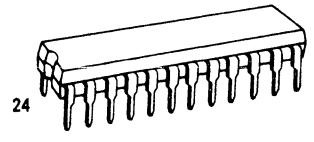
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of date directly from the internal registers.

The TC74HCT651A is of the inverting output type while the TC74HCT652A is a non-inverting output type.

ALL inputs are equipped with protection circuits against static dischage or transient excess voltage.

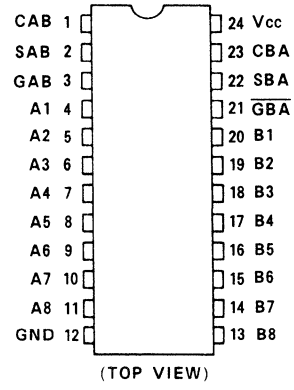
FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL Output ····· V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS651/652



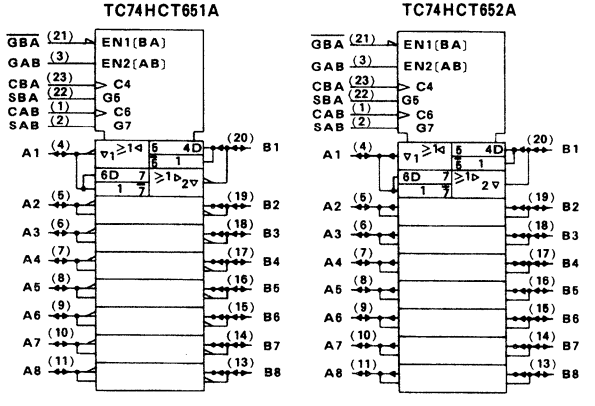
DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminal must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

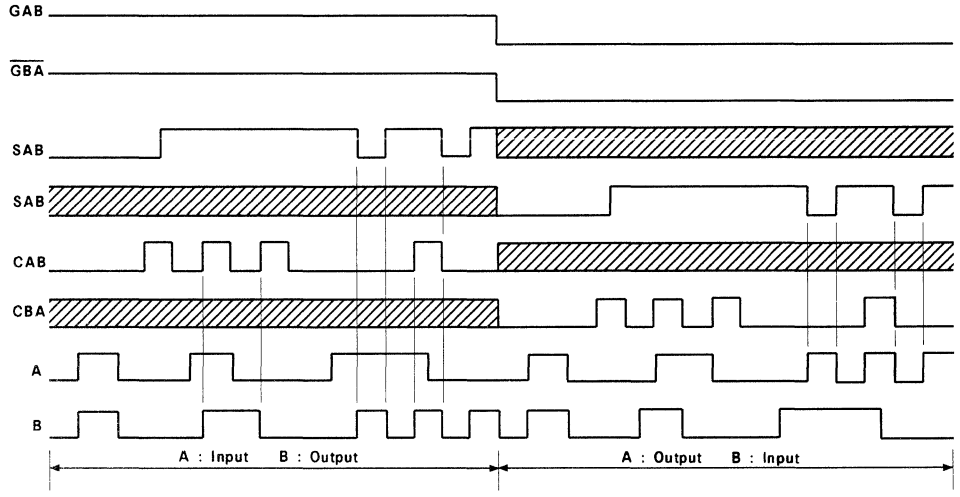
TC74HCT652A(The truth for TC74HCT651A is the same, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
* The clock are not internally gated with either GAB or $\overline{GBA}$. Therfore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

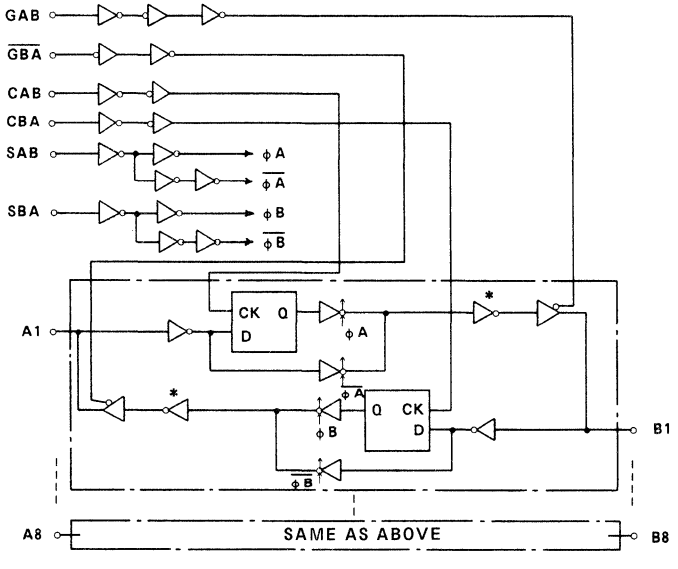
TC74HCT652A



Note : The timing chart for TC74HCT651A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HCT651A



Note : In case of TC74HCT652A output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5～5.5	V
Input Voltage	V_{IN}	0～V_{CC}	V
Output Voltage	V_{OUT}	0～V_{CC}	V
Operating Temperature	Topr	−40～85	℃
Input Rise and Fall Time	t_r, t_f	0～500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ～ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ～ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$I_{OH}=-20\ \mu A$	4.5	4.4	4.5	−	4.4	−	V
			$I_{OH}=-6\ mA$	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	$I_{OL}=20\ \mu A$	4.5	−	0.0	0.1	−	0.1	V
			$I_{OL}=6\ mA$	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{IN}=V_{CC}$ or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	−	−	4.0	−	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V, Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		4.5	−	15	19	ns
	$t_{W(H)}$		5.5	−	14	17	
Minimum Set−up Time	t_s		4.5	−	10	13	ns
			5.5	−	9	12	
Minimum Hold Time	t_h		4.5	−	5	5	ns
			5.5	−	5	5	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	20	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time (BUS−BUS)	t_{pLH}		50	4.5	−	20	30	−	38	
				5.5	−	17	27	−	34	
	t_{pHL}		150	4.5	−	25	38	−	48	
				5.5	−	22	34	−	43	
Propagation Delay Time (CAB, CBA−BUS)	t_{pLH}		50	4.5	−	29	44	−	55	
				5.5	−	26	40	−	50	
	t_{pHL}		150	4.5	−	34	52	−	65	
				5.5	−	31	47	−	59	
Propagation Delay Time (SAB, SBA−BUS)	t_{pLH}		50	4.5	−	24	34	−	43	
				5.5	−	21	31	−	39	
	t_{pHL}		150	4.5	−	29	42	−	53	
				5.5	−	26	38	−	48	
Output Enable time (GAB, $\overline{GBA}$−BUS)	t_{pZL}	$R_L = 1\,k\Omega$	50	4.5	−	22	33	−	41	
				5.5	−	20	30	−	37	
	t_{pZH}		150	4.5	−	27	41	−	51	
				5.5	−	24	37	−	46	
Output Enable time (GAB, $\overline{GBA}$−BUS)	t_{pLZ}	$R_L = 1\,k\Omega$	50	4.5	−	24	35	−	44	
	t_{pHZ}			5.5	−	22	32	−	40	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	55	−	25	−	MHz
				5.5	37	61	−	30	−	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$, SAB, SBA, CAB, CBA			−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT651A			−	38	−	−	−	
		TC74HCT652A			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

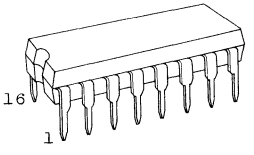
TC74HC670P

TC74HC670P 4-WORD x 4-BIT REGISTER FILE (3-STATE)

The TC74HC670 is a high speed CMOS 4-WORD × 4-BIT REGISTER FILE fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.
Four data inputs are avairable which are used to supply the 4-bit word to be stored. Location of the word is determined by the A and B inputs. When the WRITE-ENABLE input is "H", the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the READ-ENABLE input "H", the data outputs are inhibited and go into the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS670



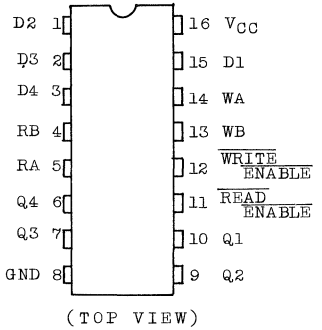
DIP16 (3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

WRITE FUNCTION TABLE

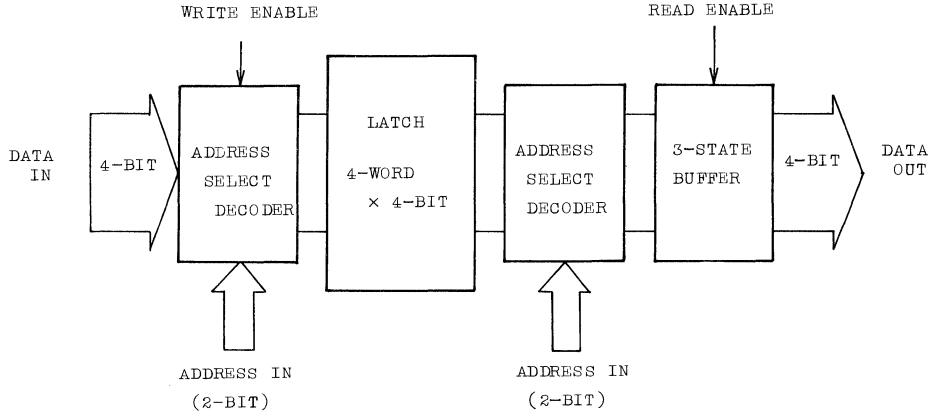
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

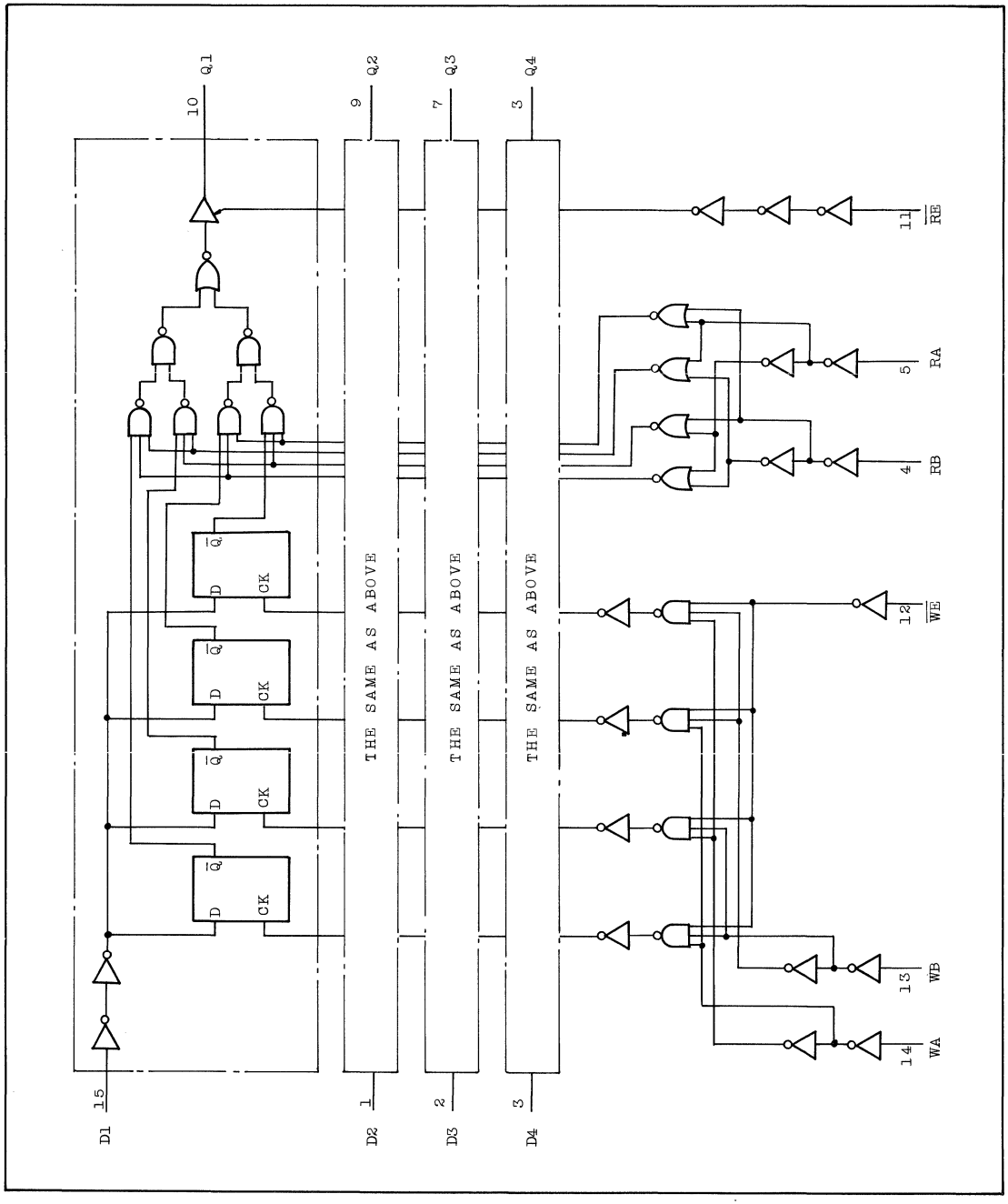
READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES
1. X : DON'T CARE Z : HIGH IMPEDANCE
2. (Q=D) = THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3. Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4. W0B1 = THE FIRST BIT OF WORD 0, etc.

BLOCK DIAGRAM



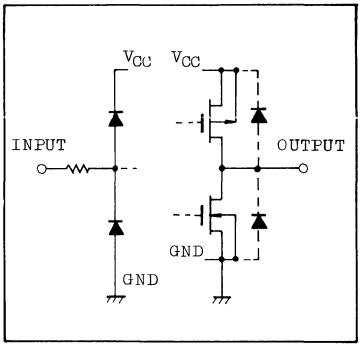
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

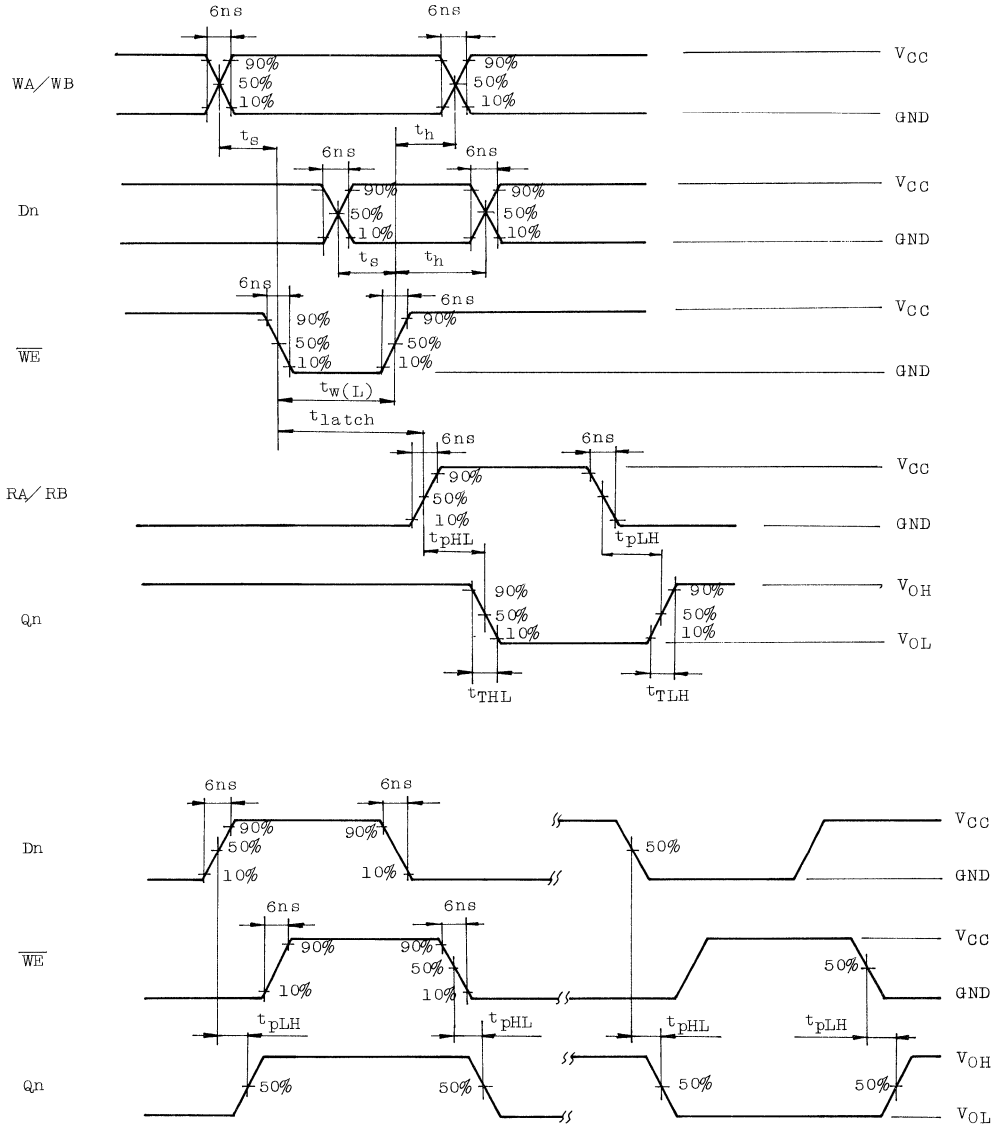
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (RA, RB - Qn)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{WE}$ - Qn)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Propagation Delay Time (Dn - Qn)	t_{pLH} t_{pHL}		2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Minimum Pulse Width ($\overline{WE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Dn - $\overline{WE}$)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set-up Time (WA, WB - $\overline{WE}$)	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time (Dn - $\overline{WE}$)	t_h		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (WA, WB - $\overline{WE}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Latch Time ($\overline{WE}$ - RA, RB)	(1) t_{latch}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	68	120	-	150	
			4.5	-	17	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(2)			-	44	-	-	-	

Note(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

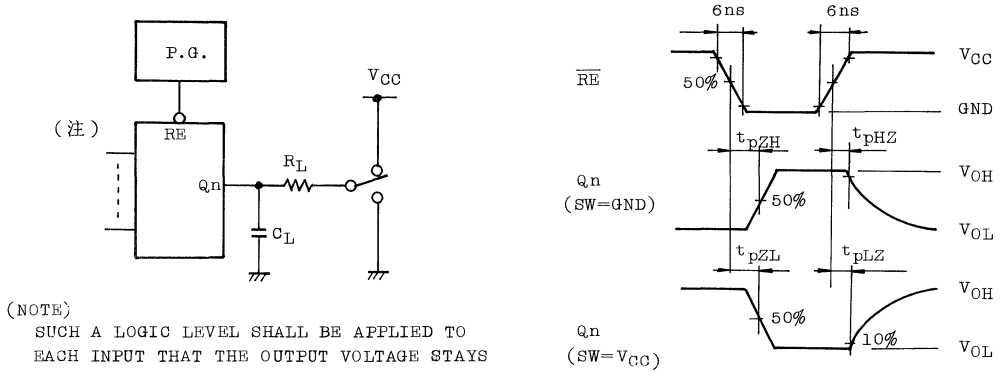
(2): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

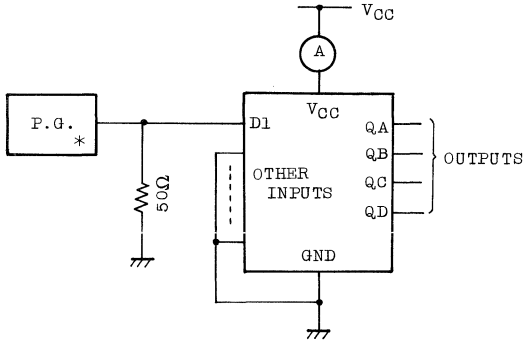


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



(NOTE)
SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC688AP/AF

8-BIT EQUALITY COMPARATOR

The TC74HC688A is a high speed cmos 8-BIT EQUALITY COMPARATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

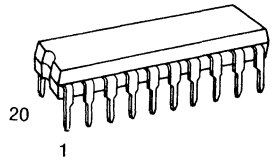
The TC74HC688A compares two 8-bit binary or BCD words applied inputs $P_0 \sim P_7$, and inputs $Q_0 \sim Q_7$, and indicates whether or not they are equal.

A signal active low enable is provided to facilitate cascading of several packages to compare of words greater than 8 bits

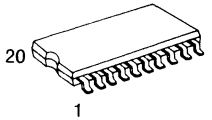
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS688

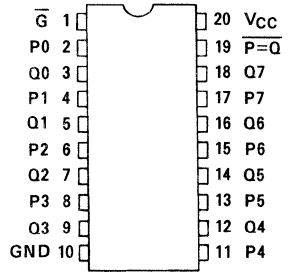


DIP20 (3D20A-P)



MFP20 (F20GA-P)

PIN ASSIGNMENT



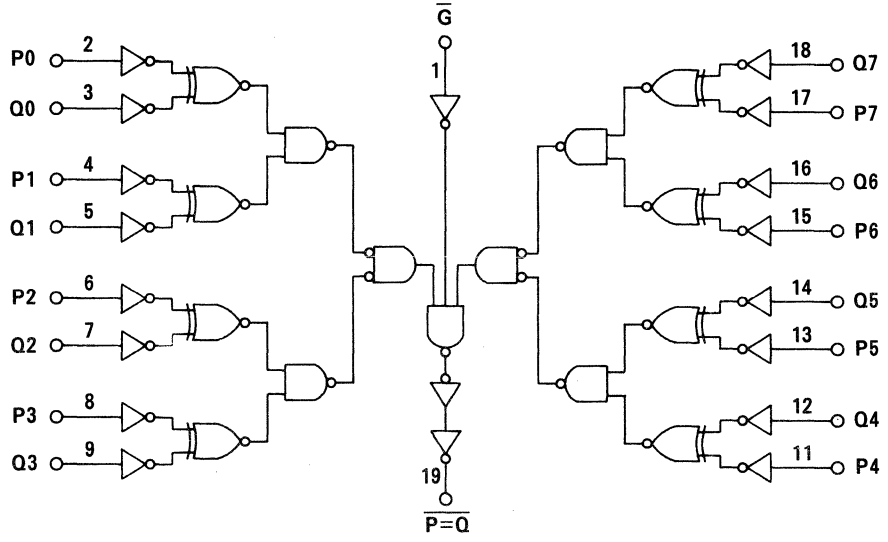
(TOP VIEW)

TRUTH TABLE

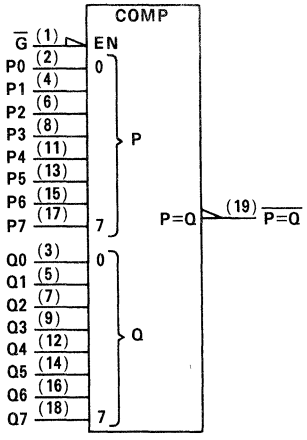
INPUTS		OUTPUT
P , Q	$\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X : Don't care

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (Pn, Qn–$\overline{P}$=$\overline{Q}$)	t_{pLH} t_{pHL}		–	17	29	
Propagation Delay Time ($\overline{G}$–$\overline{P}$=$\overline{Q}$)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=–40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (Pn, Qn–$\overline{P}$=$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	60	170	–	215	
			4.5	–	21	34	–	43	
			6.0	–	17	29	–	37	
Propagation Delay Time (G–$\overline{P}$=$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	40	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	10	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	32	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC690P DECADE COUNTER REGISTER
TC74HC691P 4-BIT BINARY COUNTER REGISTER

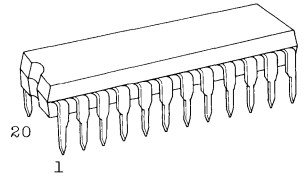
The TC74HC690/691 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

TC74HC690 is BCD DECADE COUNTER, TC74HC691 is 4-BIT BINARY COUNTER, these devices have Registers respectively.
If LOAD input ($\overline{LOAD}$) is held "L", DATA input (A ∿ D) are loaded in internal counter at positive edge of counter clock input ($\overline{CCK}$). And at counter mode, internal counter counts up at positive edge of counter clock. If counter clear input ($\overline{CCLR}$) is held "L", internal counter cleared asynchronously to counter clock.

Internal counter's outputs are stored in output register at positive edge of register clock (RCK). If register clear input ($\overline{RCLR}$) is held "L", the register cleared asynchronously to register clock. At this point, internal counter outputs no change. The outputs (Q_A ∿ Q_D) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$). Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

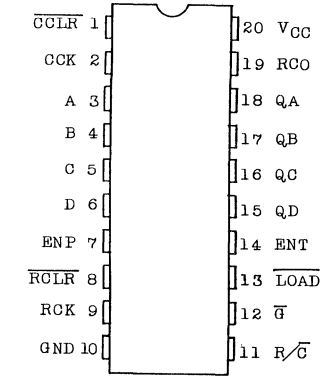


DIP20(3D20A-P)

FEATURES:

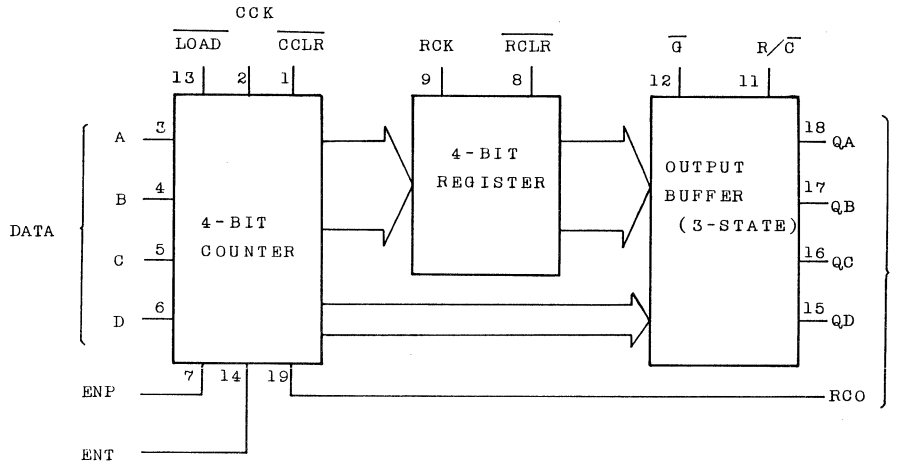
- High Speed ..... f_{MAX}=33MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads (For Q_A ∿ Q_D)
  10 LSTTL Loads (For RCO)
- Symmetrical Output Impedance
  $|I_{OH}|=I_{OL}$=6mA(Min.) for Q_A ∿ Q_D Output
  $|I_{OH}|=I_{OL}$=4mA(Min.) for RCO Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL(74LS690/691)

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



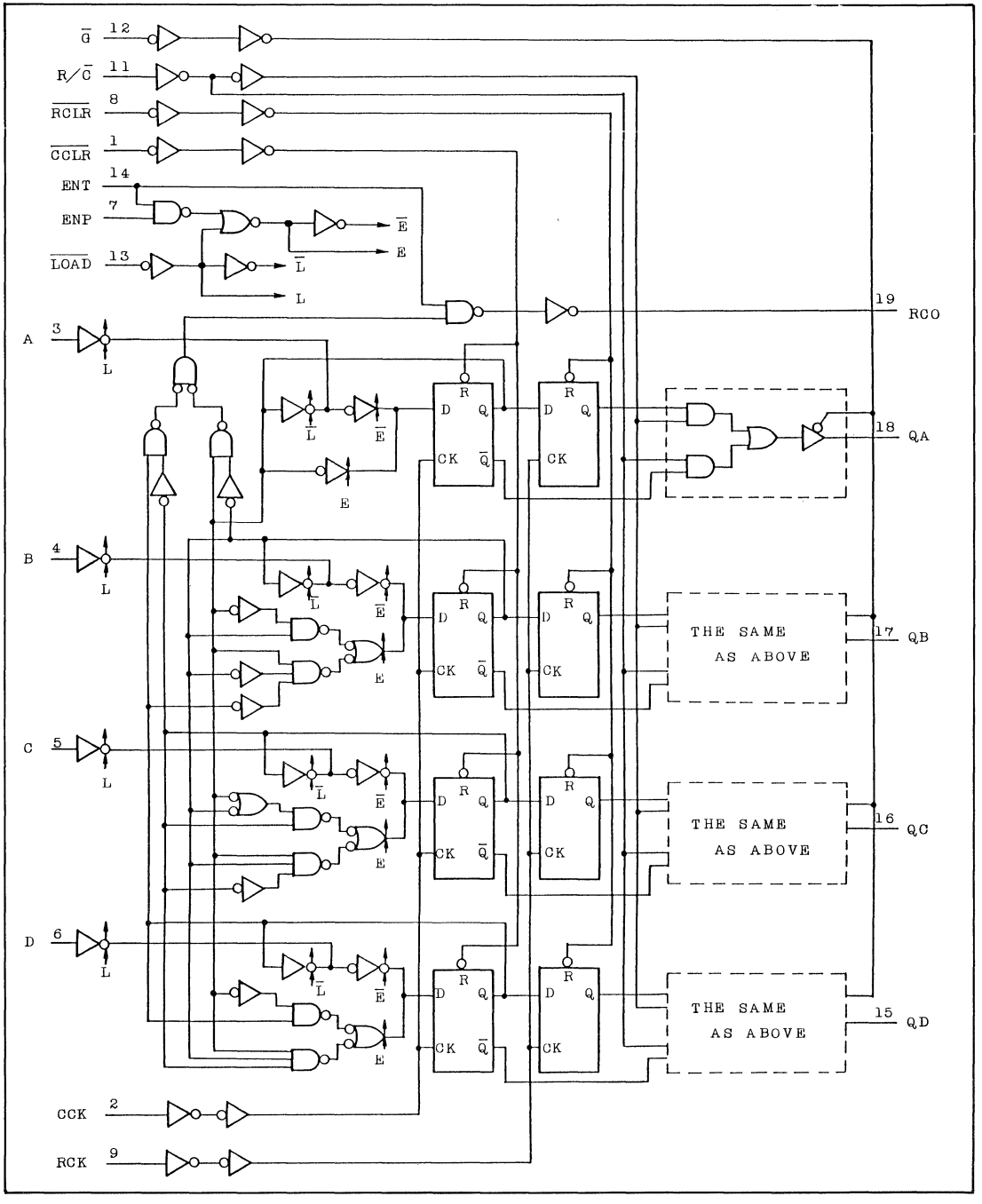
TRUTH TABLE

INPUTS									OUTPUTS				FUUCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	↓	X	X	L	L	NO CHANGE				COUNT DISABLE
H	H	X	L	↓	X	X	L	L					NO CHANGE
H	H	H	H	↓	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	X	H	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO CHANGE

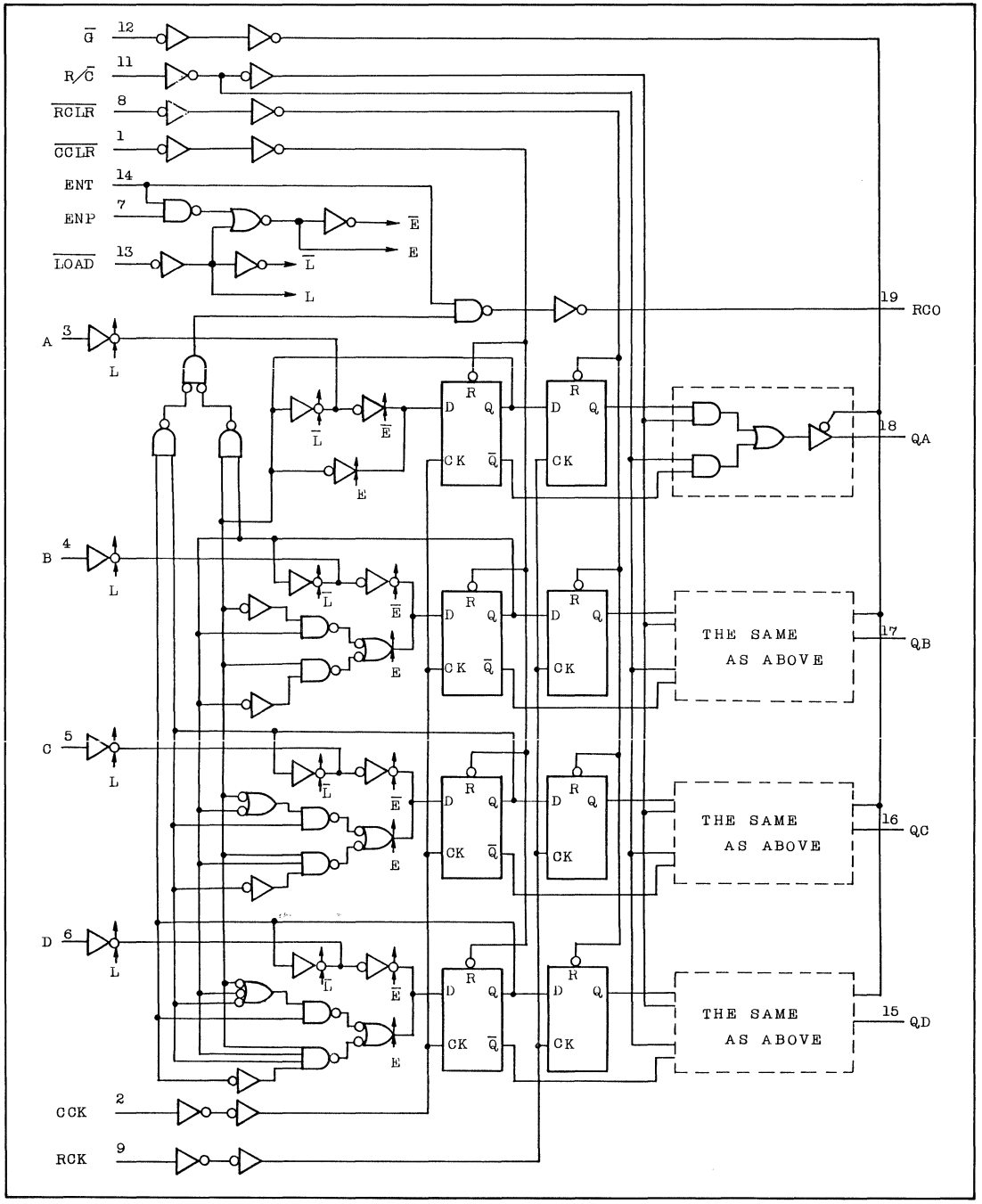
X: Don't Care
Z: High Impedance
a∿d: The level of steady state input voltage at inputs A∿D respectively.
a'∿d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.

TC74HC690 RCO=QA • QD • ENT
TC74HC691 RCO=QA • QB • QC • QD • ENT

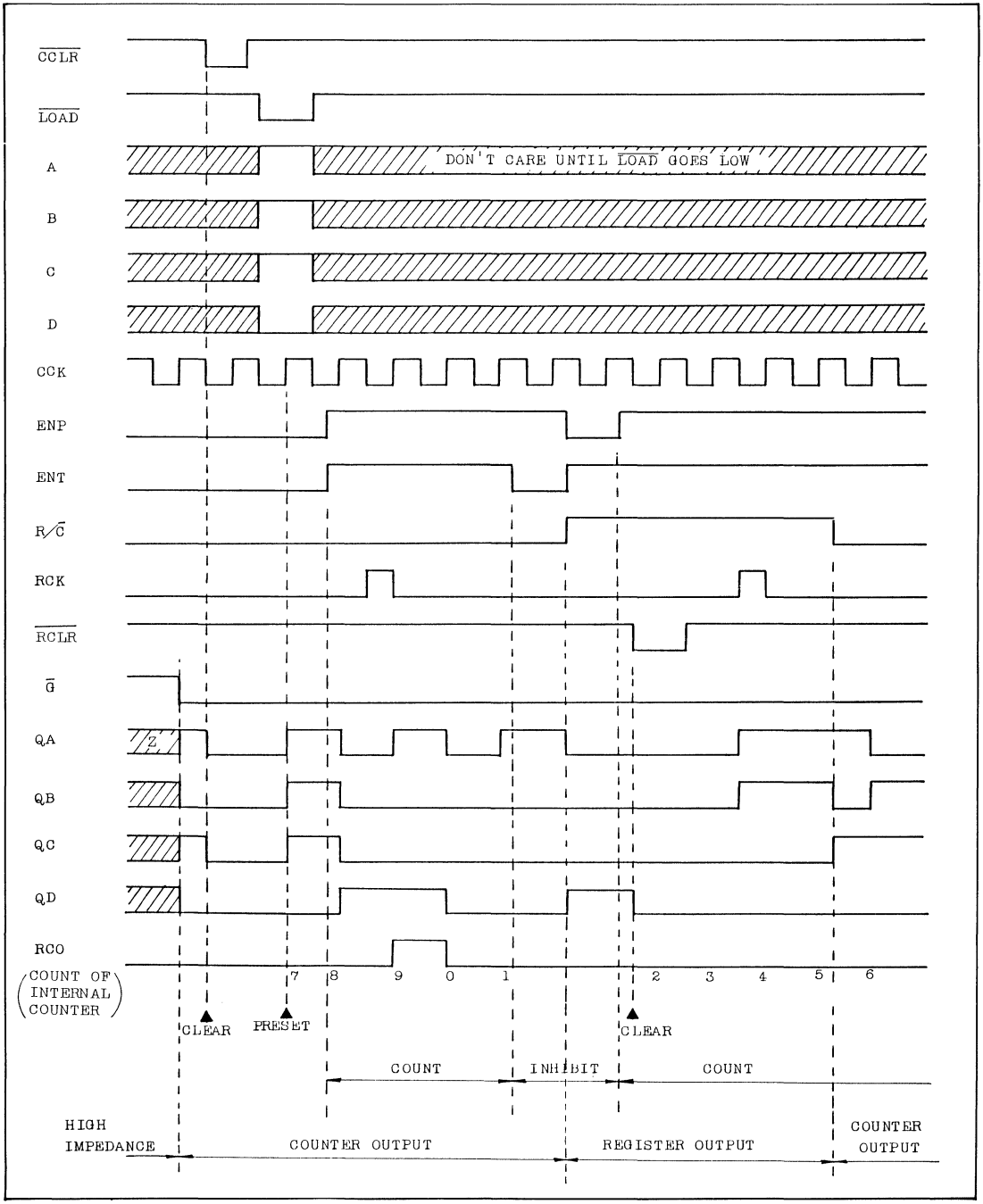
LOGIC DIAGRAM TC74HC690



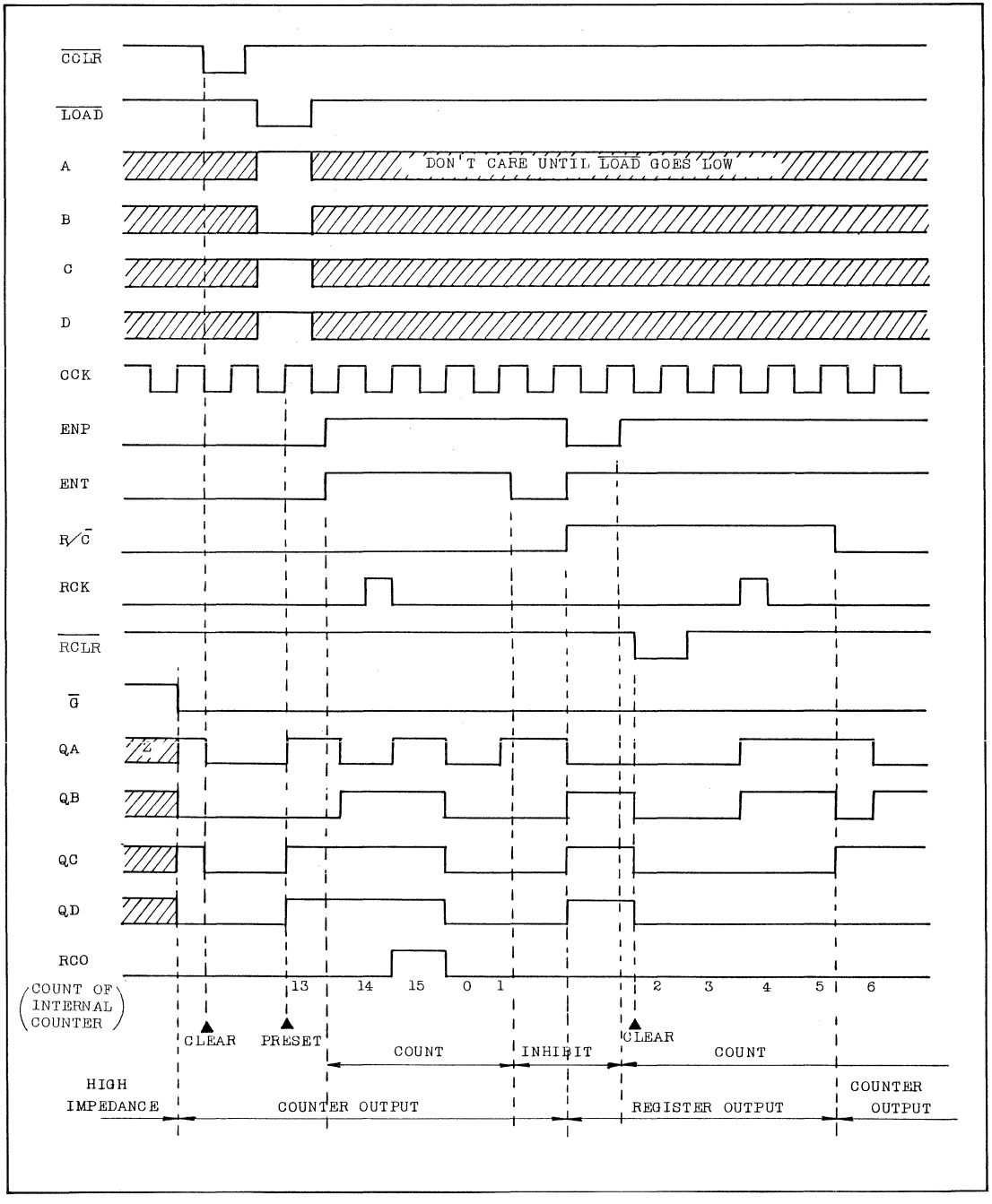
LOGIC DIAGRAM TC74HC691



TIMING CHART TC74HC690

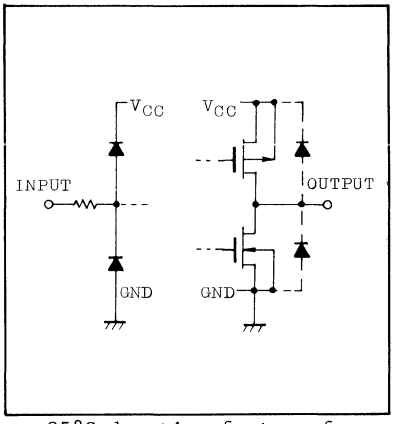


TIMING CHART TC74HC691



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage Range		V_{CC}	-0.5 ∿ 7	V
DC Input Voltage		V_{IN}	-0.5 ∿ V_{CC}+0.5	
DC Output Voltage		V_{OUT}	-0.5 ∿ V_{CC}+0.5	
Input Diode Current		I_{IK}	±20	mA
Output Diode Current		I_{OK}	±20	
DC Output Current	(RCO)	I_{OUT}	±25	
	(QA ∿ QD)		±35	
DC V_{CC}/Ground Current		I_{CC}	±70	
Power Dissipation		P_D	500*	mW
Storage Temperature		T_{STG}	-65 ∿ 150	°C
Lead Temperature(10sec)		T_L	300	



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r,t_f	0∿1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		RCO	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA∿QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		RCO	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Off Leak Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0		40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (RCO)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CCK - RCO)	t_{pLH} t_{pHL}		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($R/\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (ENT - RCO)	t_{pLH} t_{pHL}		2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	

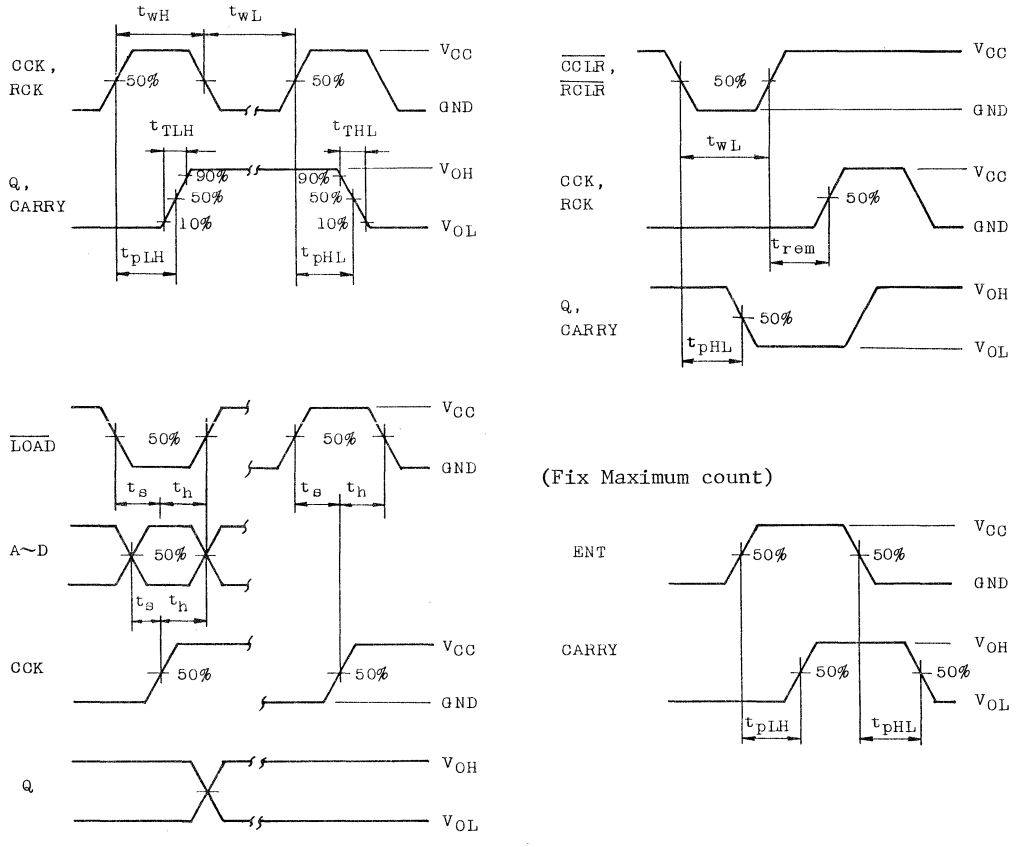
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	160	305	-	380	ns
			4.5	-	40	61	-	76	
			6.0	-	12	52	-	65	
Propagation Delay Time ($\overline{CCLR}$ - RCO)	t_{pLH}		2.0	-	132	255	-	320	
			4.5	-	33	51	-	64	
			6.0	-	28	44	-	54	
Propagation Delay Time ($\overline{RCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$, $\overline{RCLR}$)	$t_{w(L)}$		2.0	-	44	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set up Time ($\overline{LOAD}$, ENT, ENP)	t_s		2.0	-	80	175	-	220	
			4.5	-	20	35	-	44	
			6.0	-	17	30	-	37	
Minimum Set up Time (A, B, C, D)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set up Time (CCK - RCK)	t_s		2.0	-	76	175	-	220	
			4.5	-	19	35	-	44	
			6.0	-	16	30	-	37	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	170	-	215	
			4.5	-	23	34	-	43	
			6.0	-	20	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	80	-	-	-	

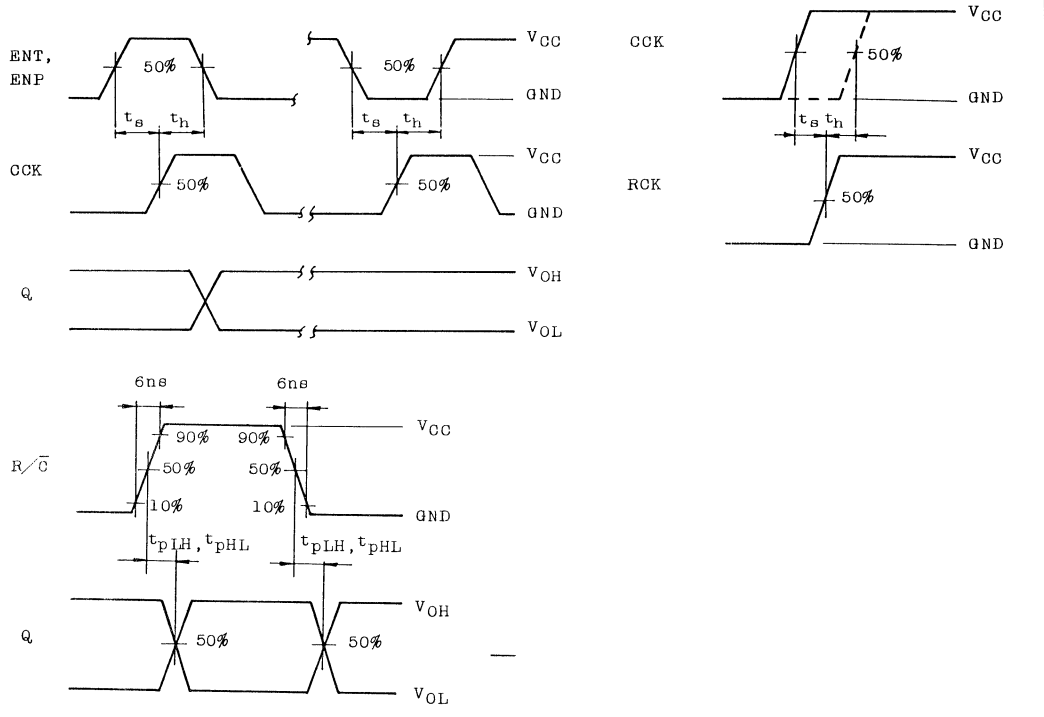
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 1)

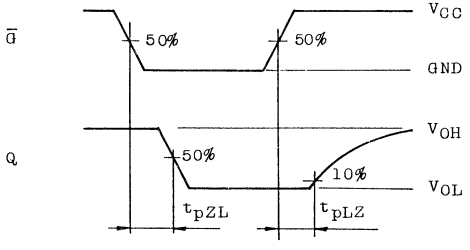


SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 2)



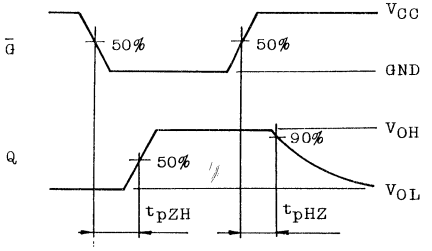
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.

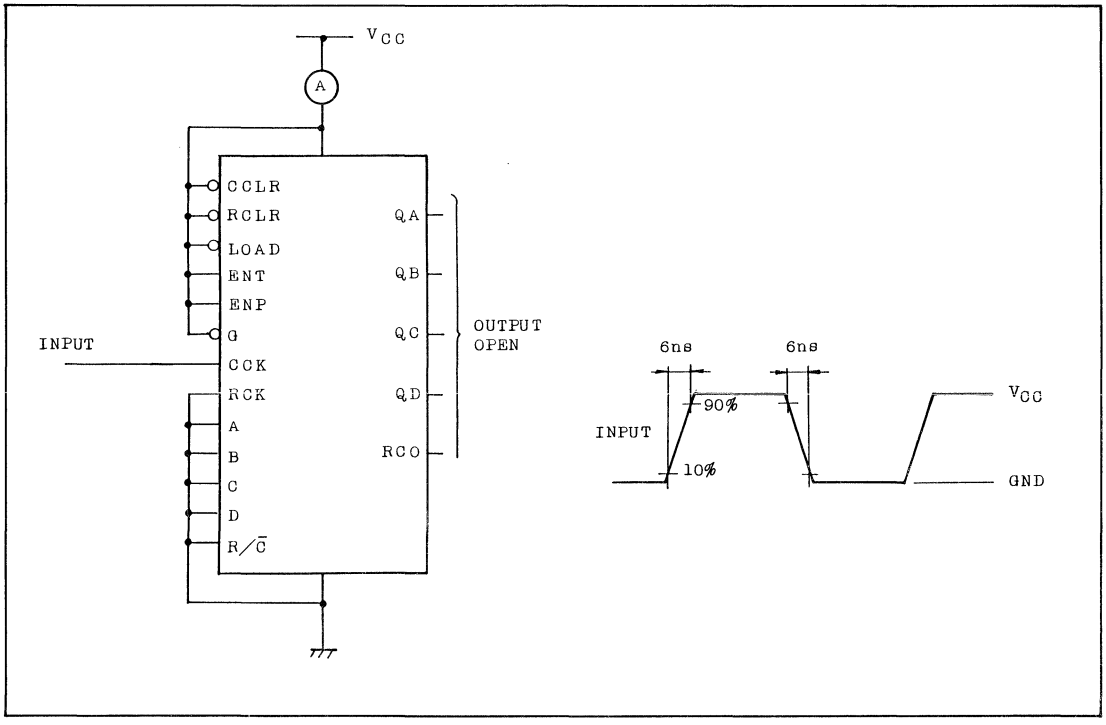


t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.



I_{CC}(Opr.) TEST WAVEFORM



TC74HC692P
TC74HC693P

TC74HC692P DECADE COUNTER REGISTER
TC74HC693P 4-BIT BINARY COUNTER REGISTER

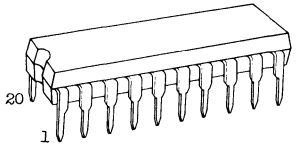
The TC74HC692/693 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalnet LSTTL while maintaining the CMOS low power dissipation.

TC74HC692 is BCD DECADE COUNTER, TC74HC693 is 4-BIT BINARY COUNTER, these devices have Registers respectively.
If LOAD input ($\overline{LOAD}$) is held "L", DATA input (A ∿ D) are loaded in internal counter at positive edge of counter clock input ($\overline{CCK}$). And at counter mode, internal counter counts up at positive edge of counter clock. If counter clear input ($\overline{CCLR}$) is held "L", internal counter cleared synchronously to counter clock.

Internal counter's outputs are stored in output register at positive edge of register clock (RCK). If register clear input ($\overline{RCLR}$) is held "L", the register cleared synchronously to register clock. At this point, internal counter outputs no change. The outputs (Q_A ∿ Q_D) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$).
Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

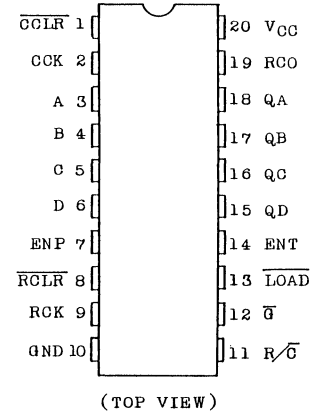


DIP20(3D20A-P)

FEATURES:

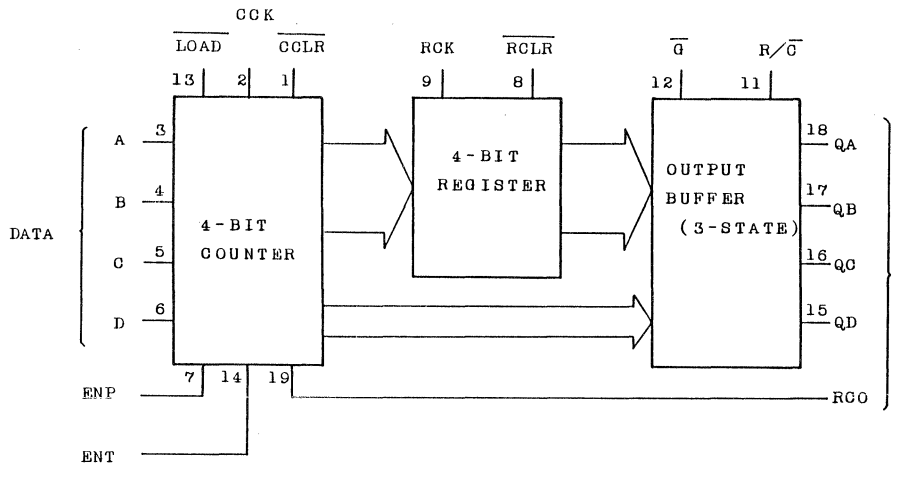
- High Speed ..... f_{MAX}=33MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads (For Q_A ∿ Q_D)
  10 LSTTL Loads (For RCO)
- Symmetrical Output Impedance
  $|I_{OH}|=I_{OL}$=6mA(Min.) for Q_A ∿ Q_D Output
  $|I_{OH}|=I_{OL}$=4mA(Min.) for RCO Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS692/693)

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



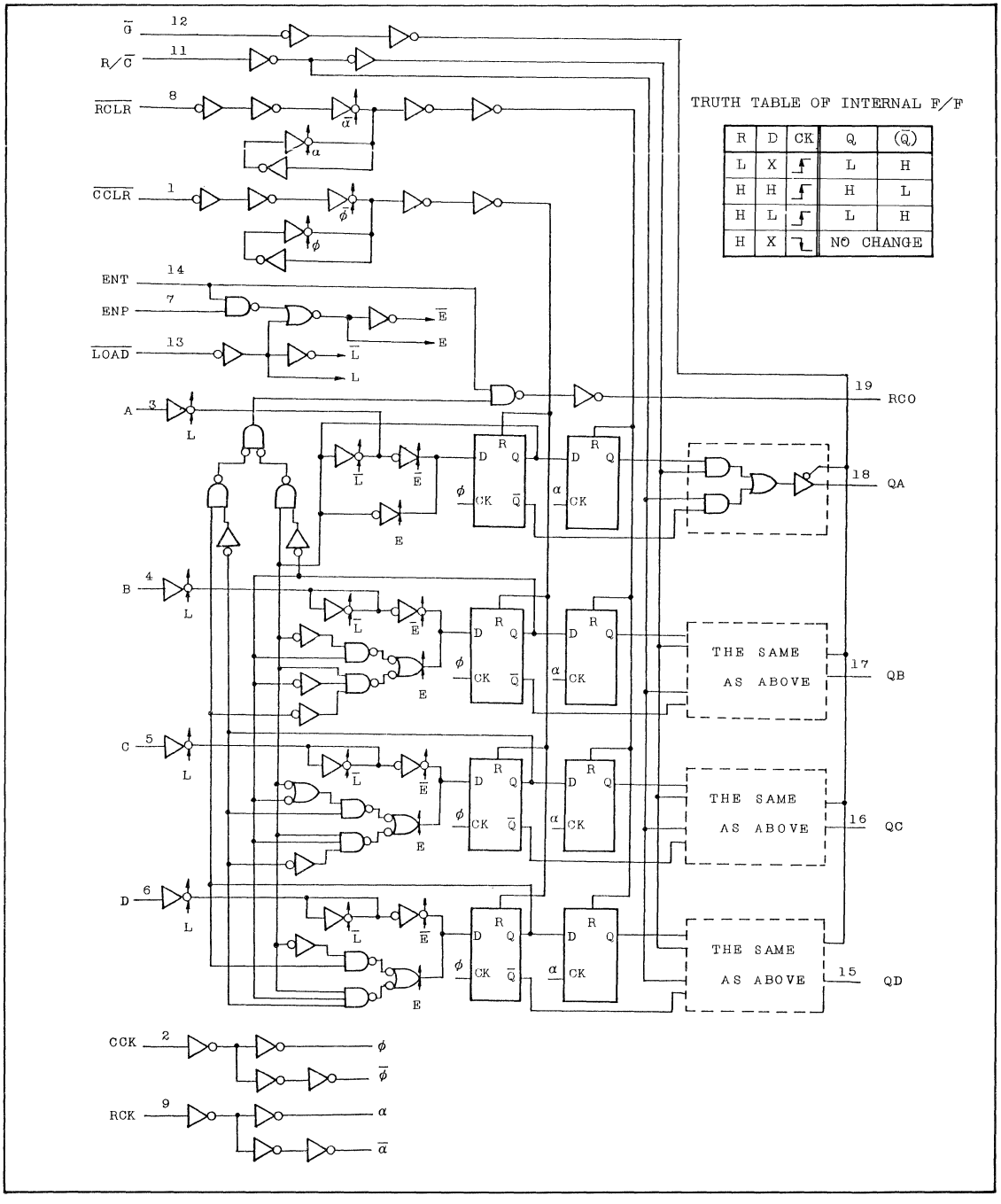
TRUTH TABLE

INPUTS									OUTPUTS				FUUCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↓	X	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	↓	X	X	L	L	NO CHANGE				COUNT DISABLE
H	H	X	L	↓	X	X	L	L					NO CHANGE
H	H	H	H	↓	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	↓	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	X	H	↓	H	L	a′	b′	c′	d′	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO CHANGE

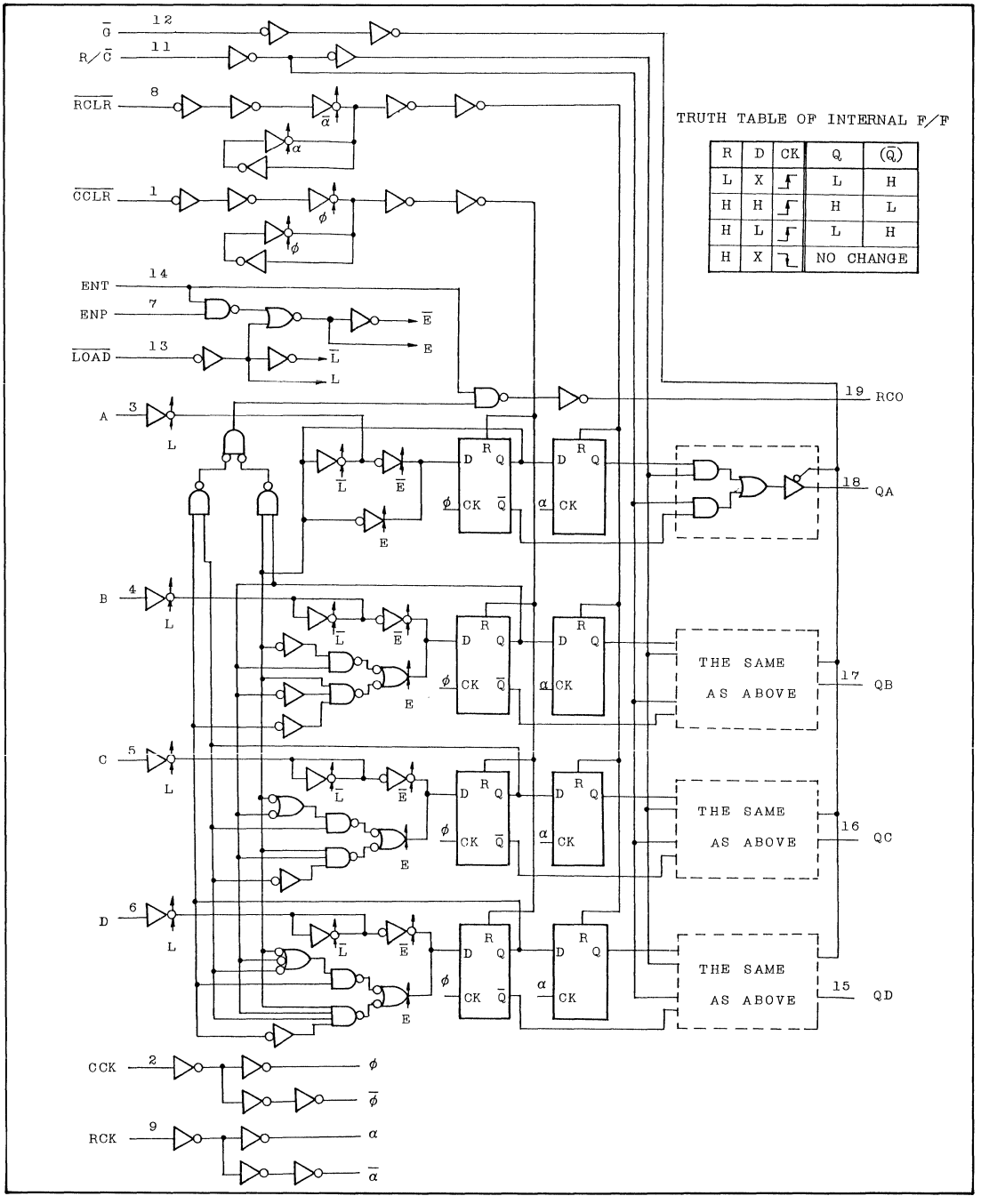
X: Don't Care
Z: High Impedance
a∿d: The level of steady state input voltage at inputs A∿D respectively.
a'∿d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.

TC74HC692 RCO = QA • QD • ENT
TC74HC693 RCO = QA • QB • QC • QD • ENT

LOGIC DIAGRAM TC74HC692



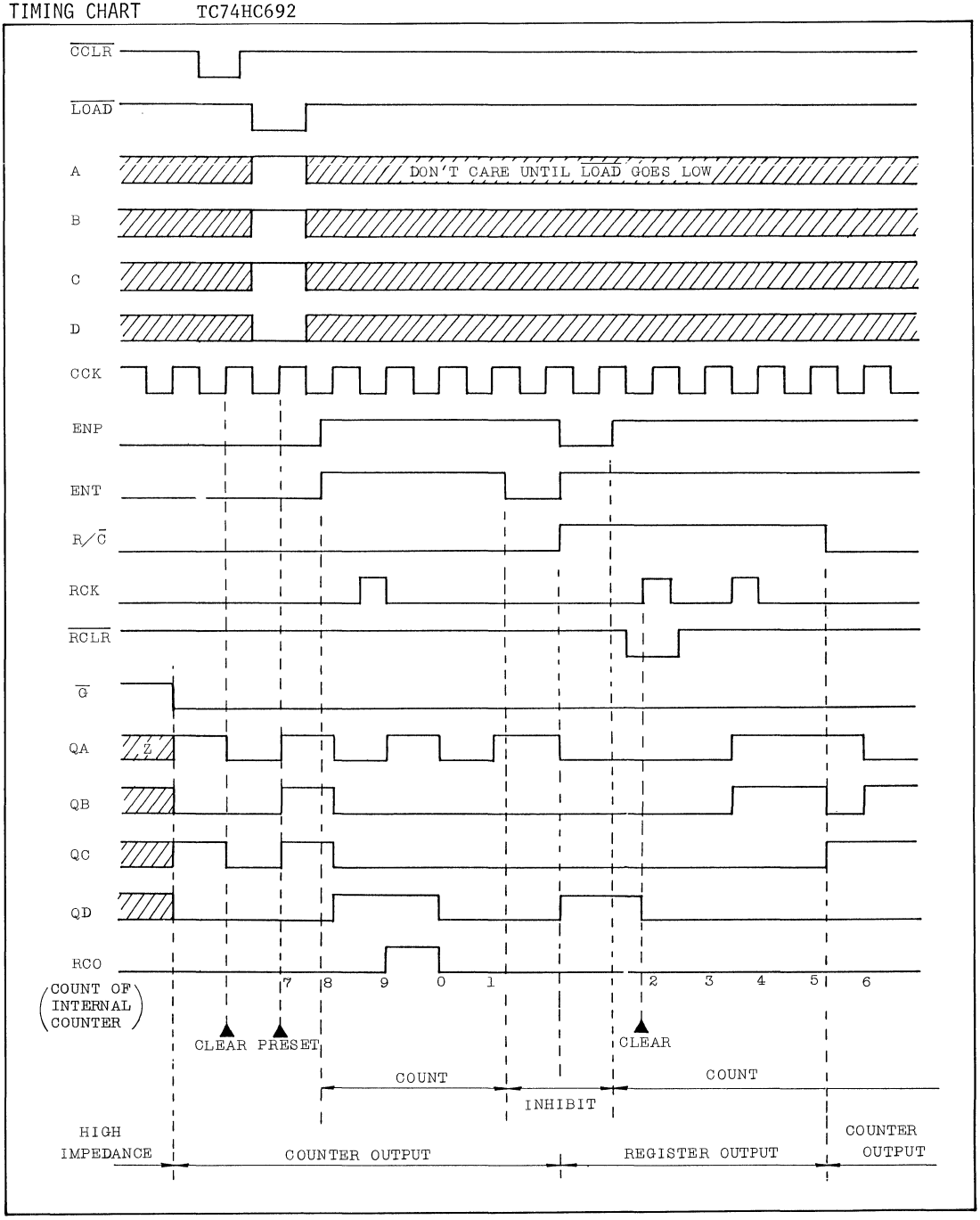
LOGIC DIAGRAM TC74HC693



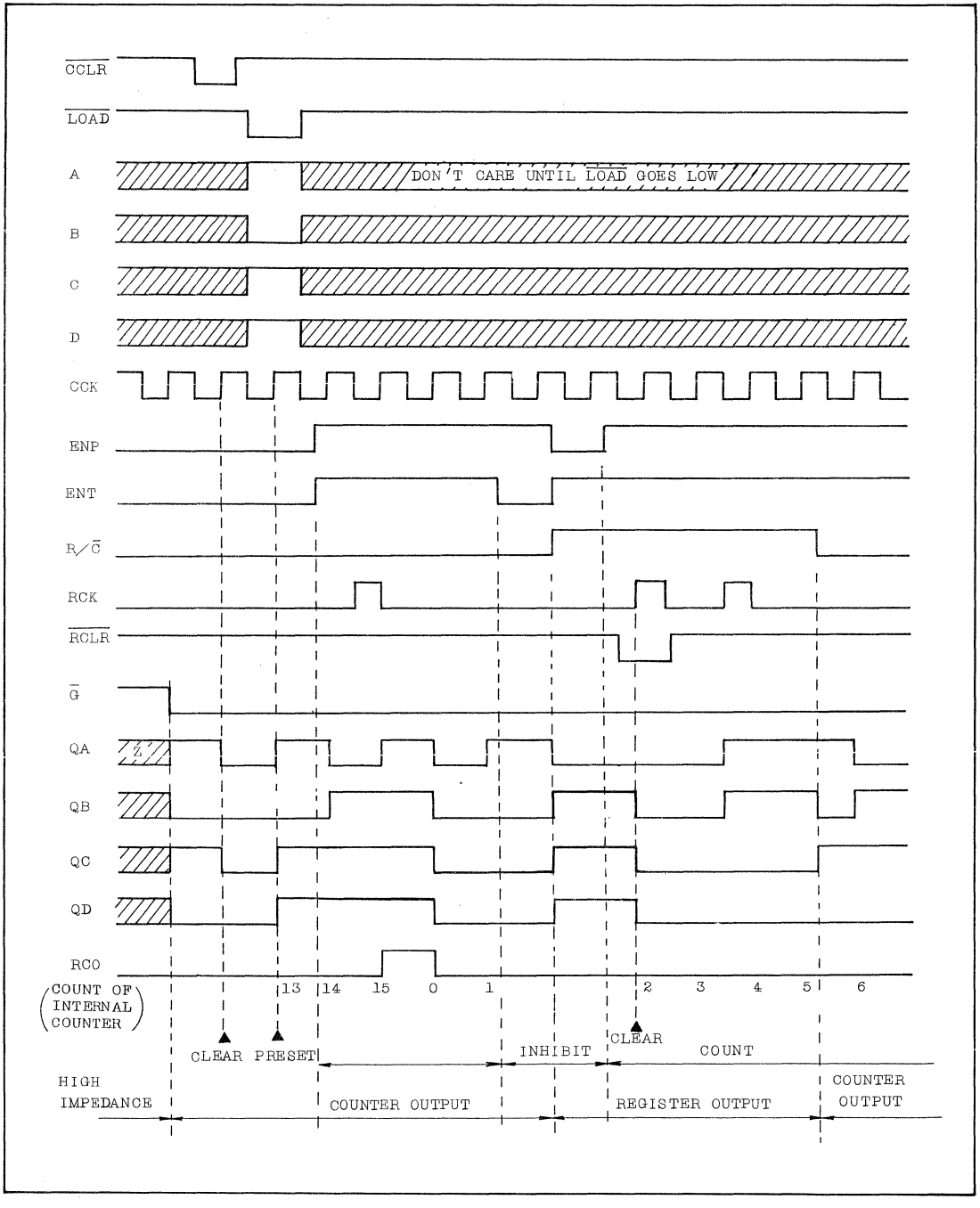
TRUTH TABLE OF INTERNAL F/F

R	D	CK	Q	($\overline{Q}$)
L	X	↓	L	H
H	H	↓	H	L
H	L	↓	L	H
H	X	↑	NO CHANGE	

TIMING CHART TC74HC692

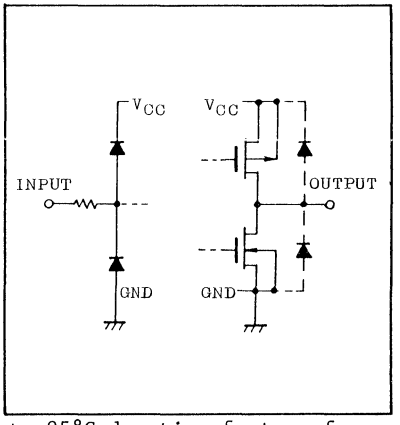


TIMING CHART TC74HC693



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage Range		V_{CC}	-0.5 ∿ 7	V
DC Input Voltage		V_{IN}	-0.5 ∿ V_{CC}+0.5	
DC Output Voltage		V_{OUT}	-0.5 ∿ V_{CC}+0.5	
Input Diode Current		I_{IK}	±20	mA
Output Diode Current		I_{OK}	±20	
DC Output Current	(RCO)	I_{OUT}	±25	
	(QA ∿ QD)		±35	
DC V_{CC}/Ground Current		I_{CC}	±70	
Power Dissipation		P_D	500*	mW
Storage Temperature		T_{STG}	-65 ∿ 150	°C
Lead Temperature(10sec)		T_L	300	



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r,t_f	0∿1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		RCO	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		RCO	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Off Leak Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}; $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (RCO)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	132	260	-	325	
			4.5	-	33	52	-	65	
			6.0	-	28	44	-	55	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time (CCK - RCO)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (R/C - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (ENT - RCO)	t_{pLH} t_{pHL}		2.0	-	48	95	-	120	
			4.5	-	12	19	-	24	
			6.0	-	10	16	-	20	

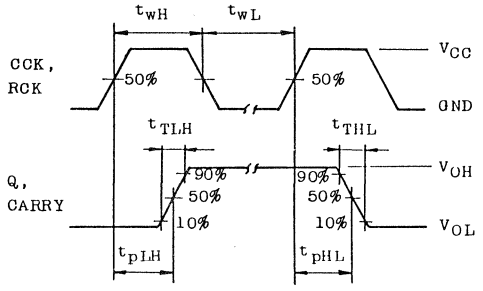
AC ELECTRICAL CHARACTERISTICS (Continued)

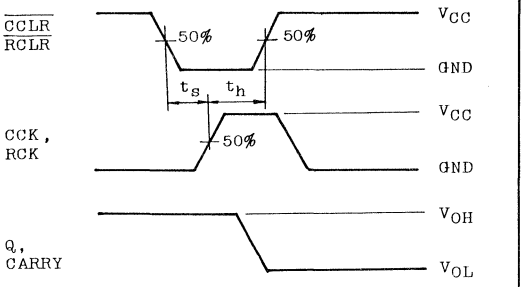
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	48	125	-	160	ns
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time ($\overline{LOAD}$, ENT, ENP)	t_s		2.0	-	68	150	-	190	
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	33	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time ($\overline{CCLR}$, $\overline{RCLR}$)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	68	150	-	190	
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	33	
Minimum Data Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	145	-	180	
			4.5	-	20	29	-	36	
			6.0	-	17	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	95	-	-	-	

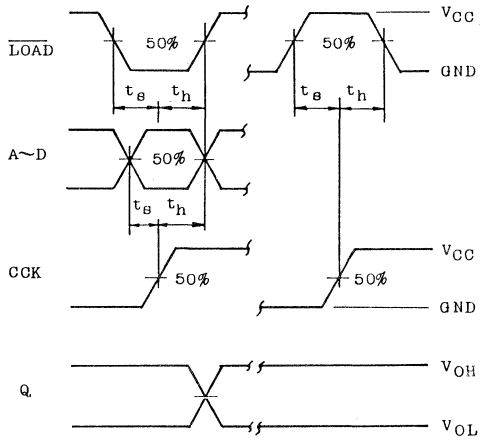
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

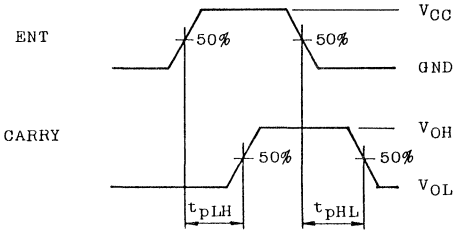
SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 1)

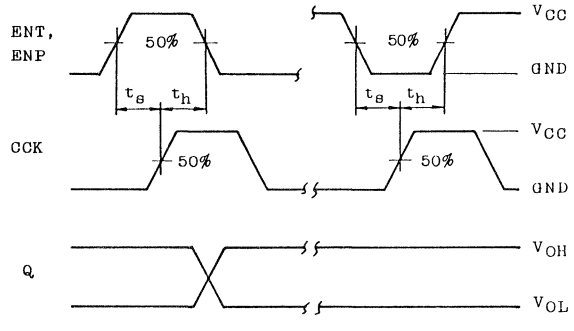


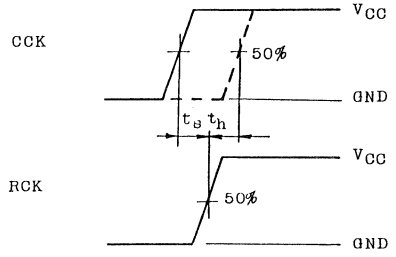




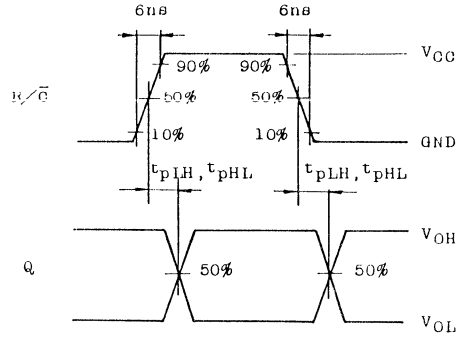
(Fix Maximum count)





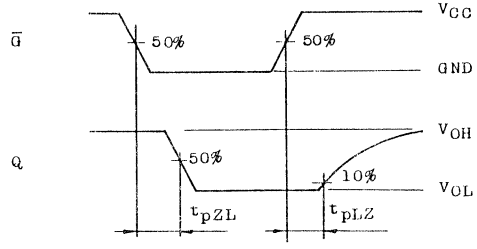


SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 2)



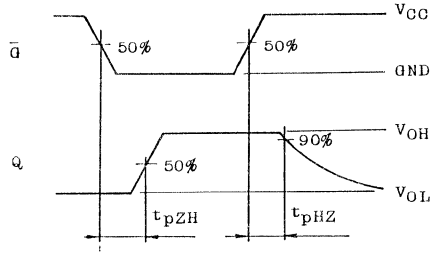
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\bar{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\bar{G}$ input is held low.

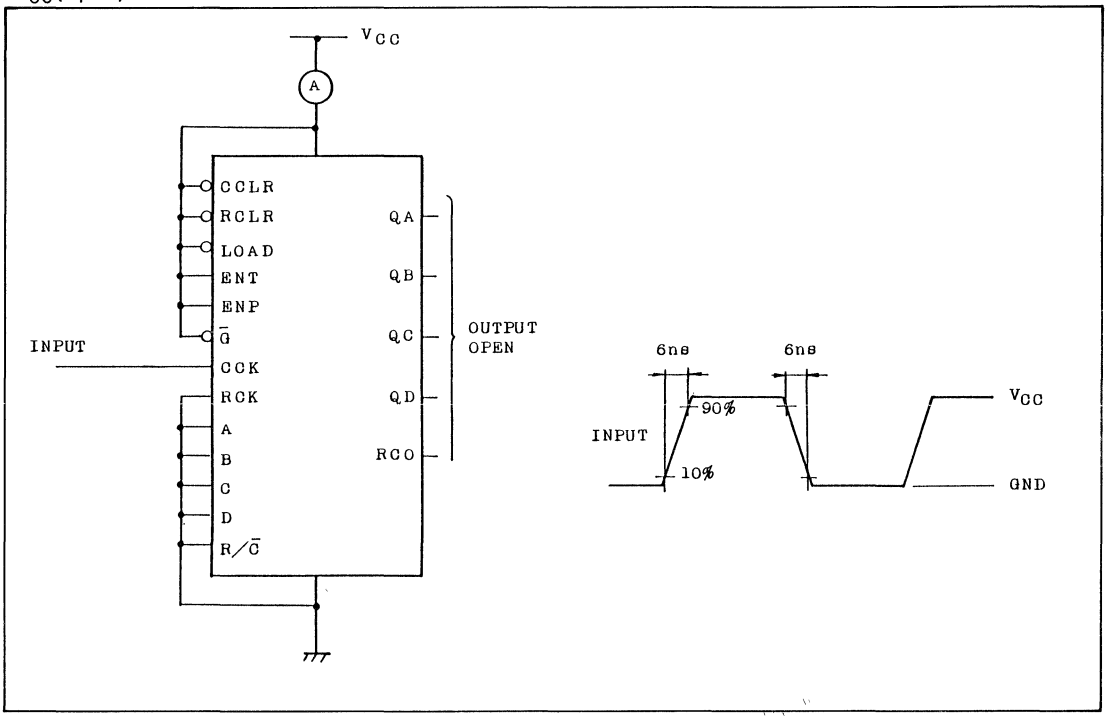


t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\bar{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\bar{G}$ input is held low.



I_{CC}(Opr.) TEST WAVEFORM



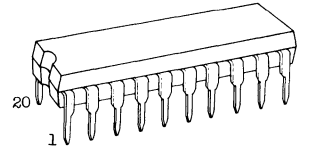
TC74HC696P
TC74HC697P

TC74HC696P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC697P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC696 is BCD DECADE COUNTER, and TC74HC697 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input $U/\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ∿ QD) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$). Their clear function are cleared asynchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=33MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ∿ QD)
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA∿ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS696/697)



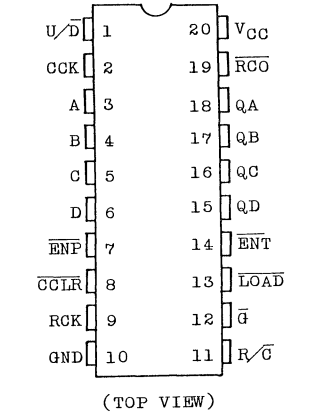
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ∿ QD) ±20 (RCO)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L					
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

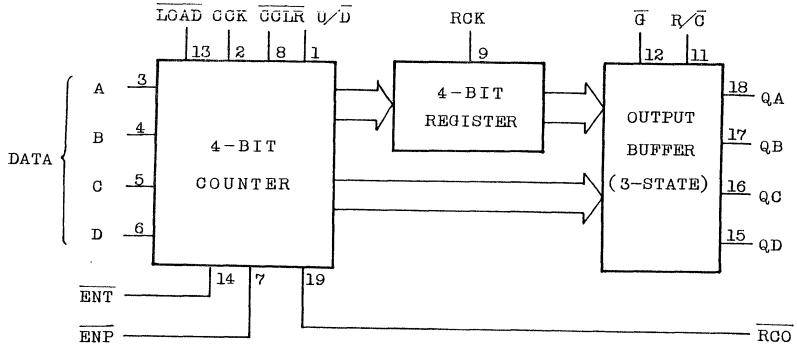
X: Don't care
Z: High Impedance
a ∿ d : The level of steady state inputs at inputs A through D respectively.
a' ∿ d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

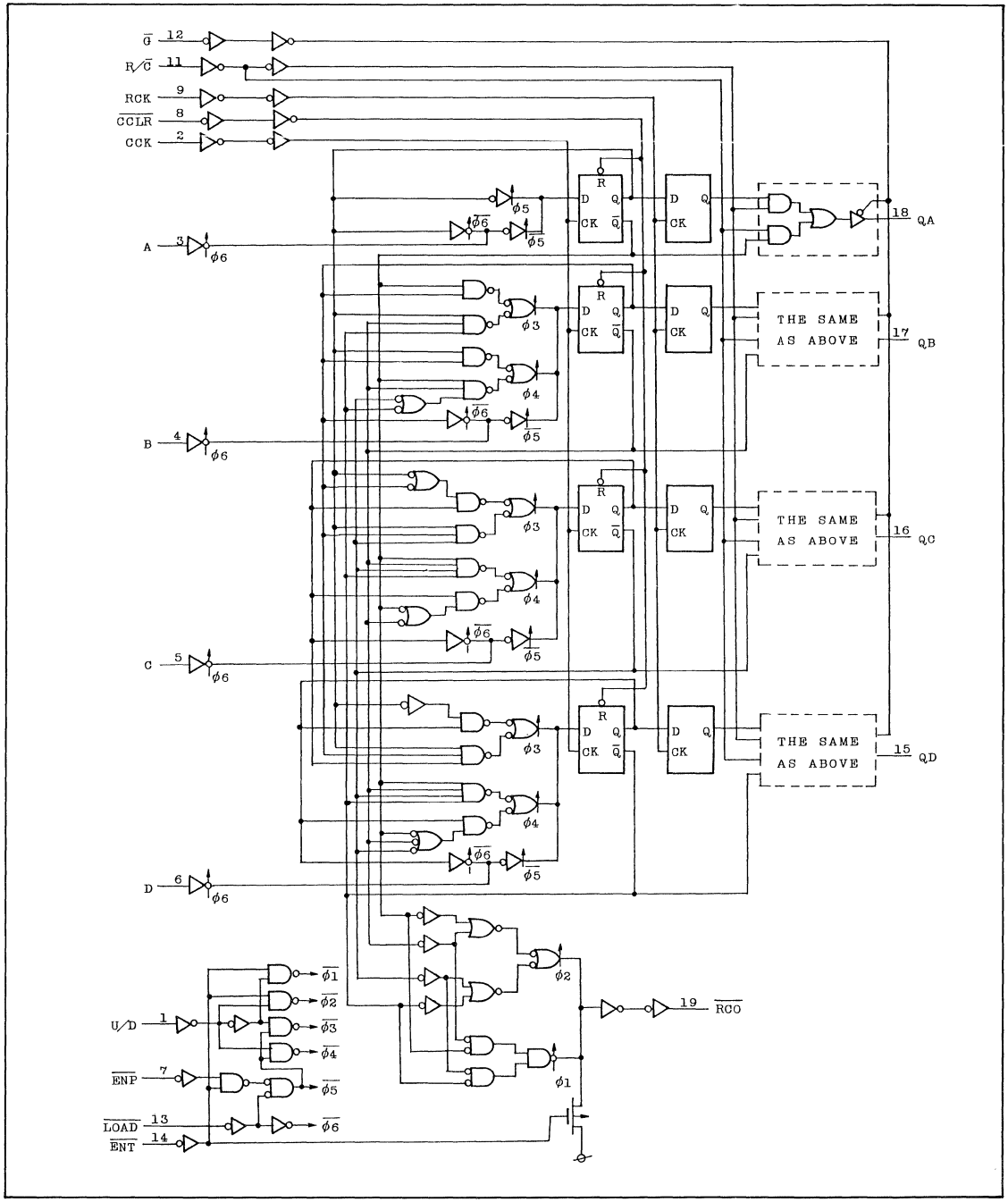
TC74HC696 $\overline{RCO}=\overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)}$

TC74HC697 $\overline{RCO}=\overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

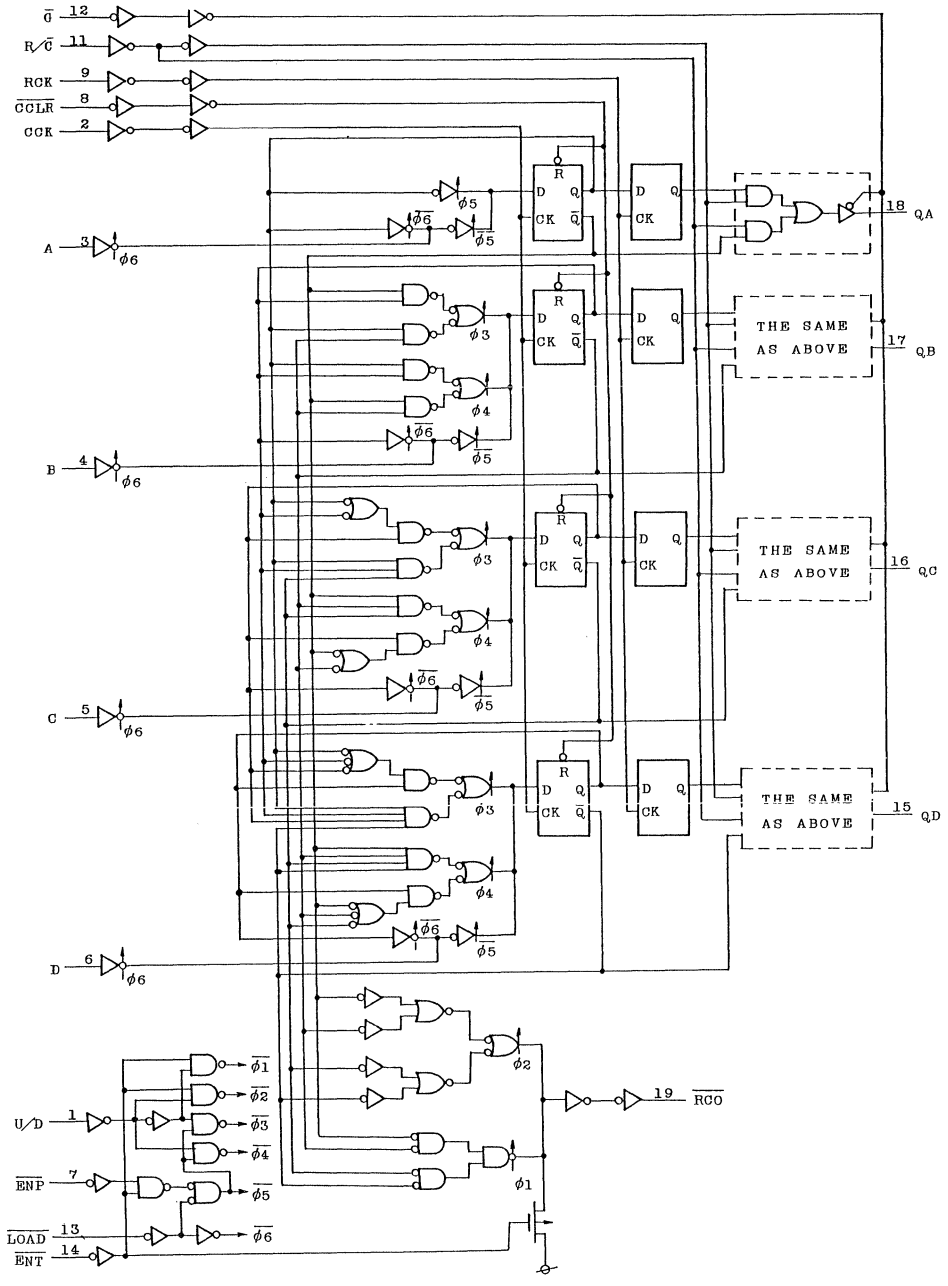
BLOCK DIAGRAM



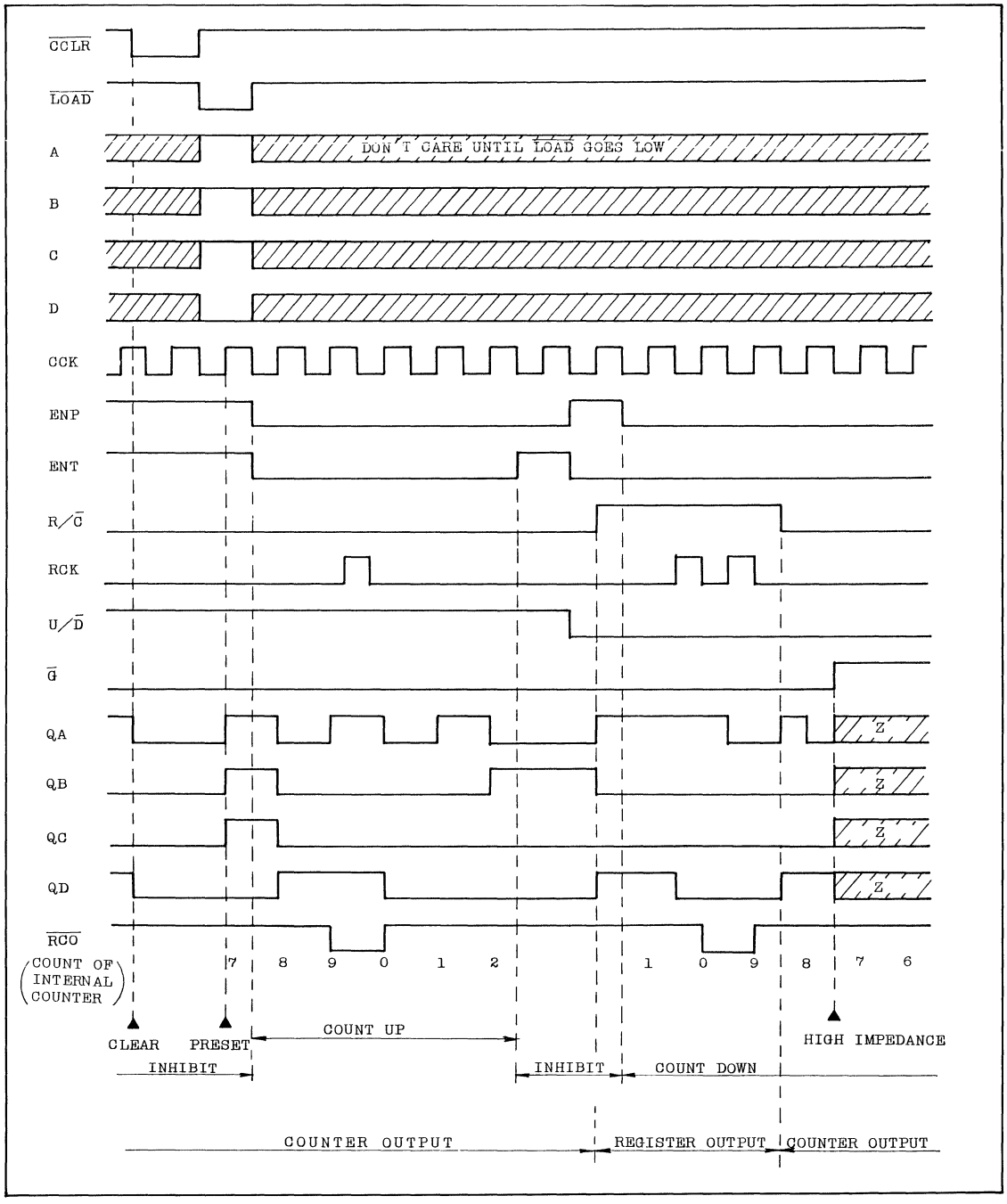
LOGIC DIAGRAM TC74HC696



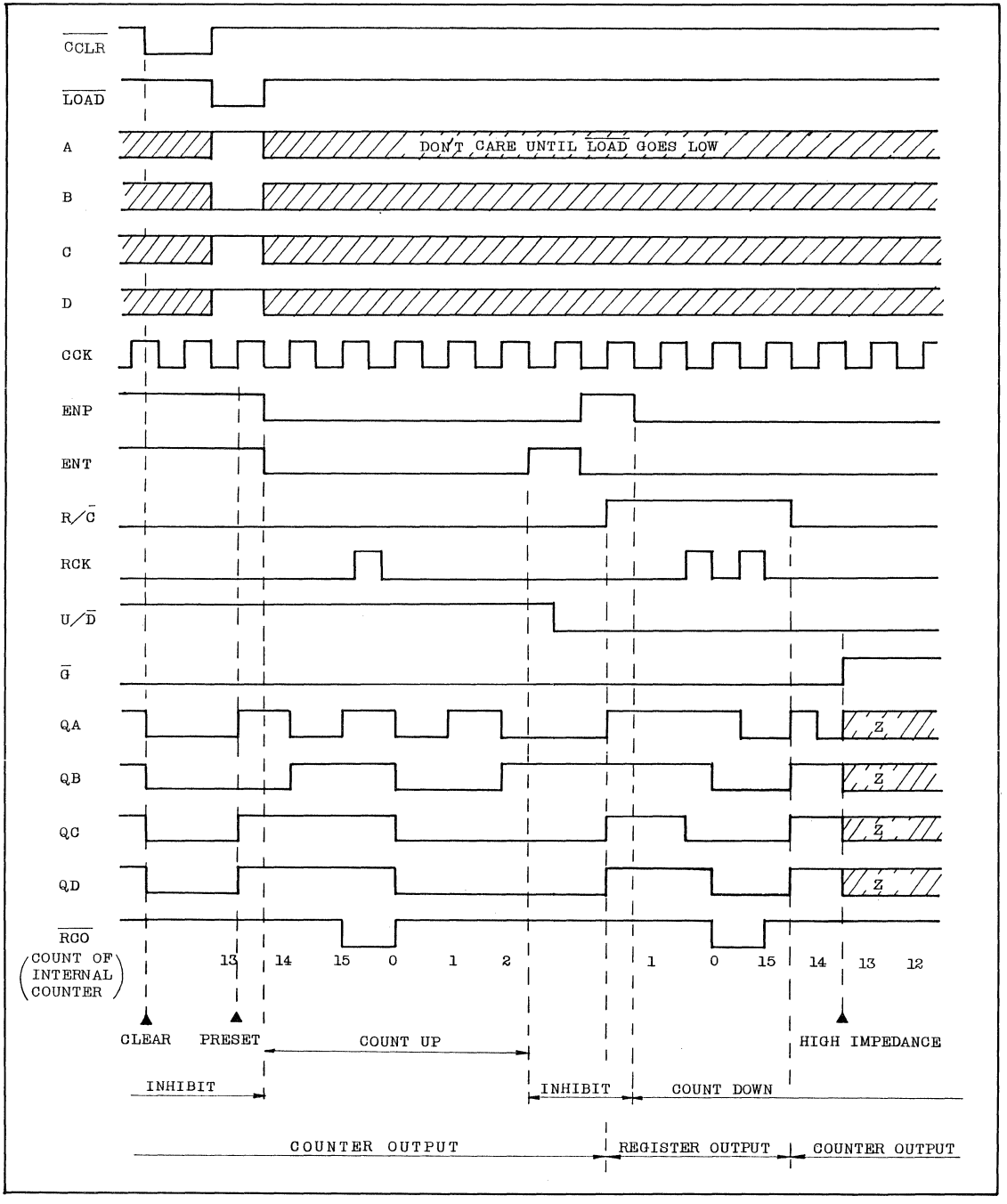
LOGIC DIAGRAM TC74HC697



TIMING CHART TC74HC696



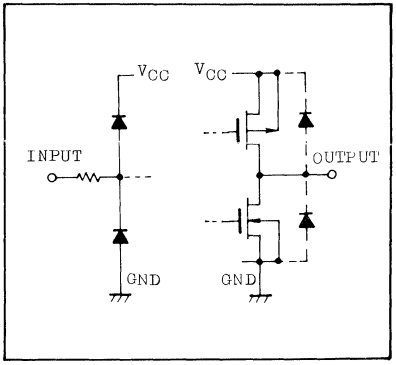
TIMING CHART TC74HC697



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	160	305	-	380	
			4.5	-	40	61	-	76	
			6.0	-	34	52	-	65	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	225	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pHL}		2.0	-	172	325	-	405	
			4.5	-	43	65	-	81	
			6.0	-	37	55	-	69	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Widht (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	96	225	-	280	
			4.5	-	24	45	-	56	
			6.0	-	20	38	-	48	

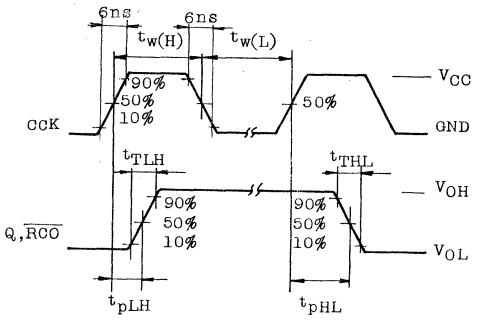
AC ELECTRICAL CHARACTERISTICS (Continued)

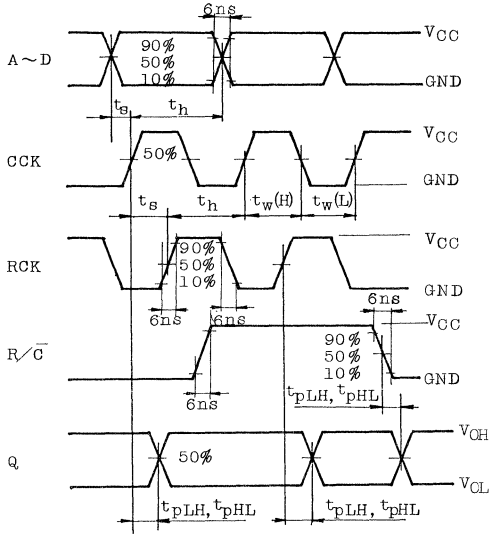
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	20	75	-	95	ns
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	52	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
Minimum Set-up Time ($U/\bar{D}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC696		-	90	-	-	-	
		TC74HC697		-	92	-	-	-	

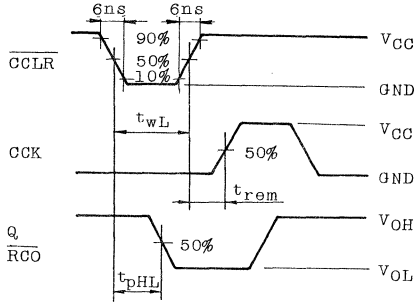
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

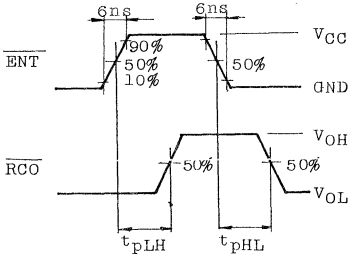
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

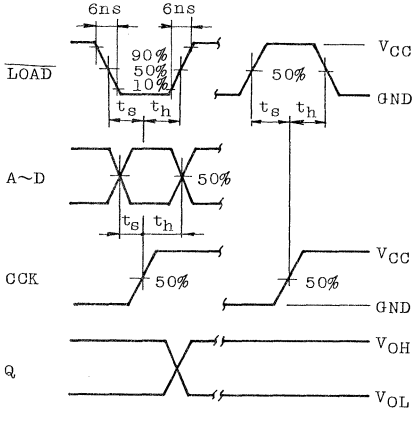
SWITCHING CHARACTERISTICS TEST WAVEFORM

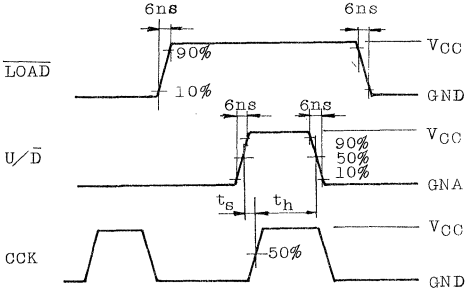






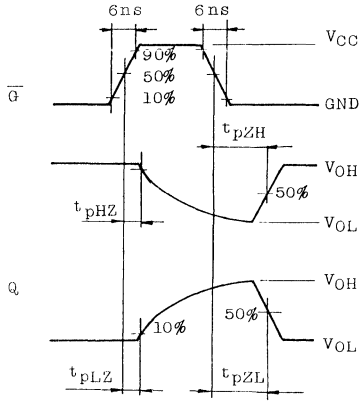


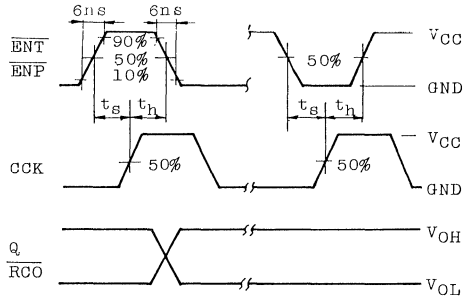




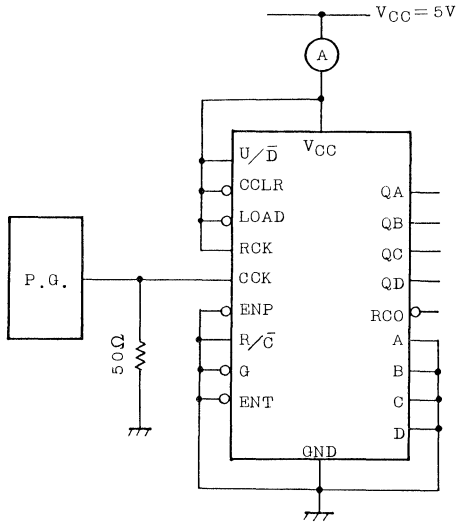
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE





I_{CC}(Opr.) TEST CIRCUIT



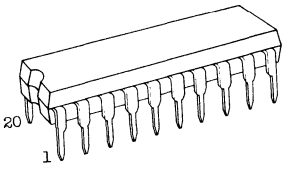
TC74HC698P
TC74HC699P

TC74HC698P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC699P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC698/699 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC698 is BCD DECADE COUNTER, and TC74HC699 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input $U/\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ∿ QD) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$). Their clear function are cleared synchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=31MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ∿ QD)
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ∿ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS698/699)



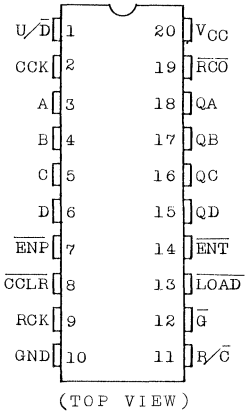
DIP20(3D20AP)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ∿ QD) ±25 ($\overline{RCO}$)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIBNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↓	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↓	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↓	X	X	L	L					
H	H	L	L	↓	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↓	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO LOAD

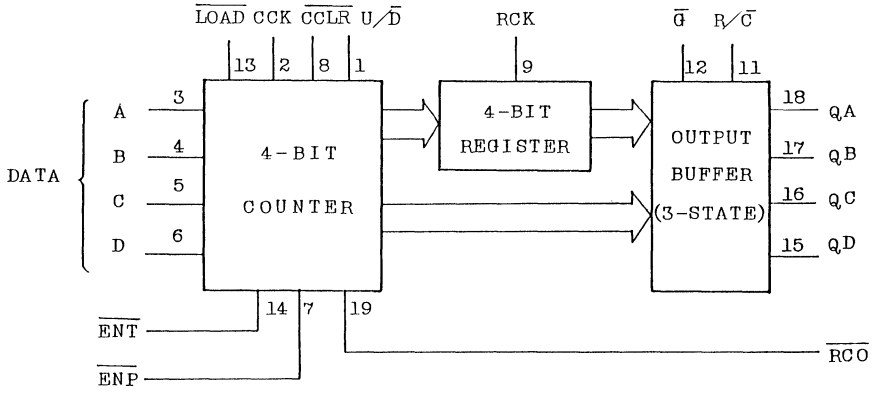
X: Don't care
Z: High Impedance
a ∿ d : The level of steady state inputs at inputs A through D respectively.
a' ∿ d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

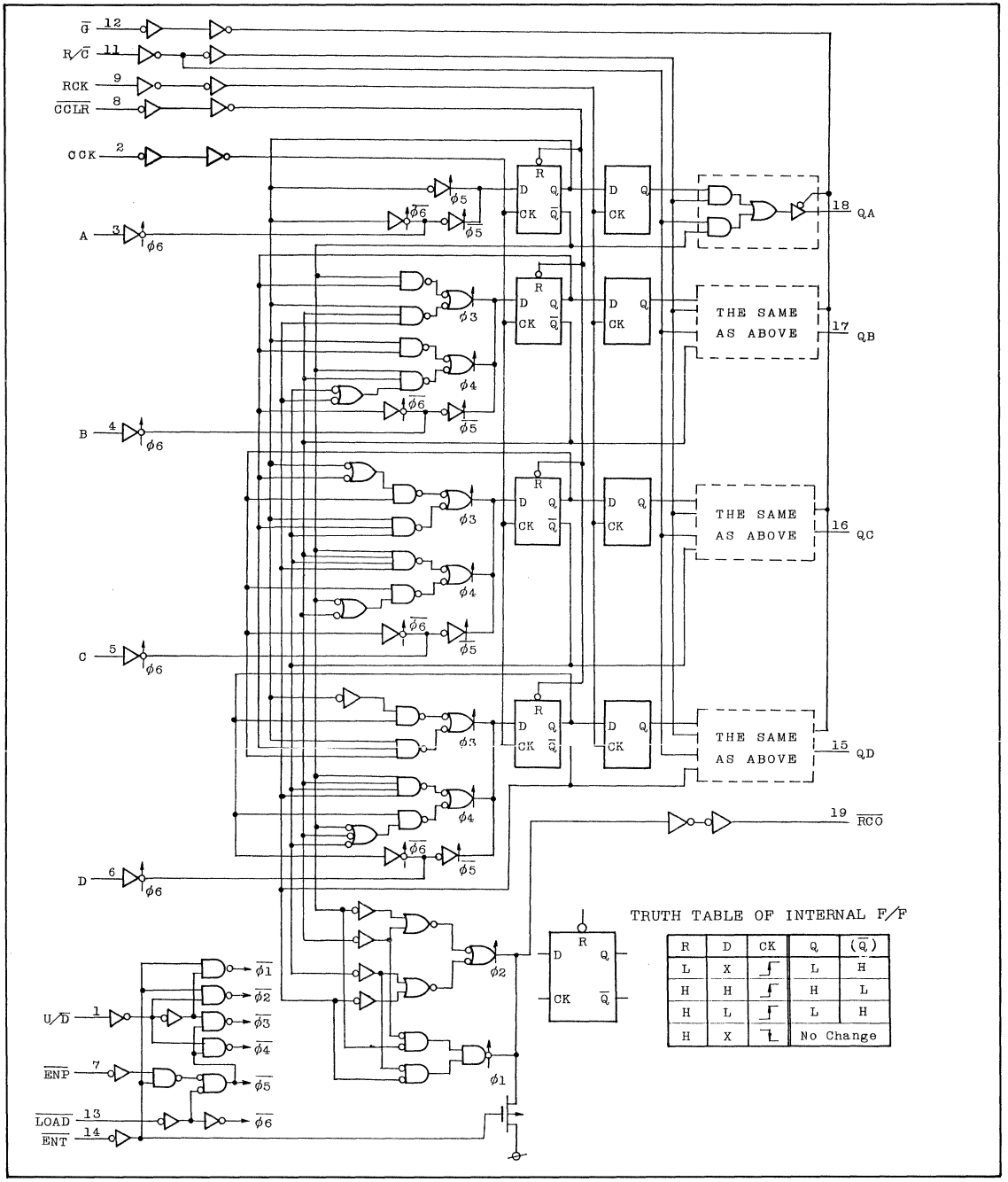
TC74HC698 $\overline{RCO}=\overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)}$

TC74HC699 $\overline{RCO}=\overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

BLOCK DIAGRAM



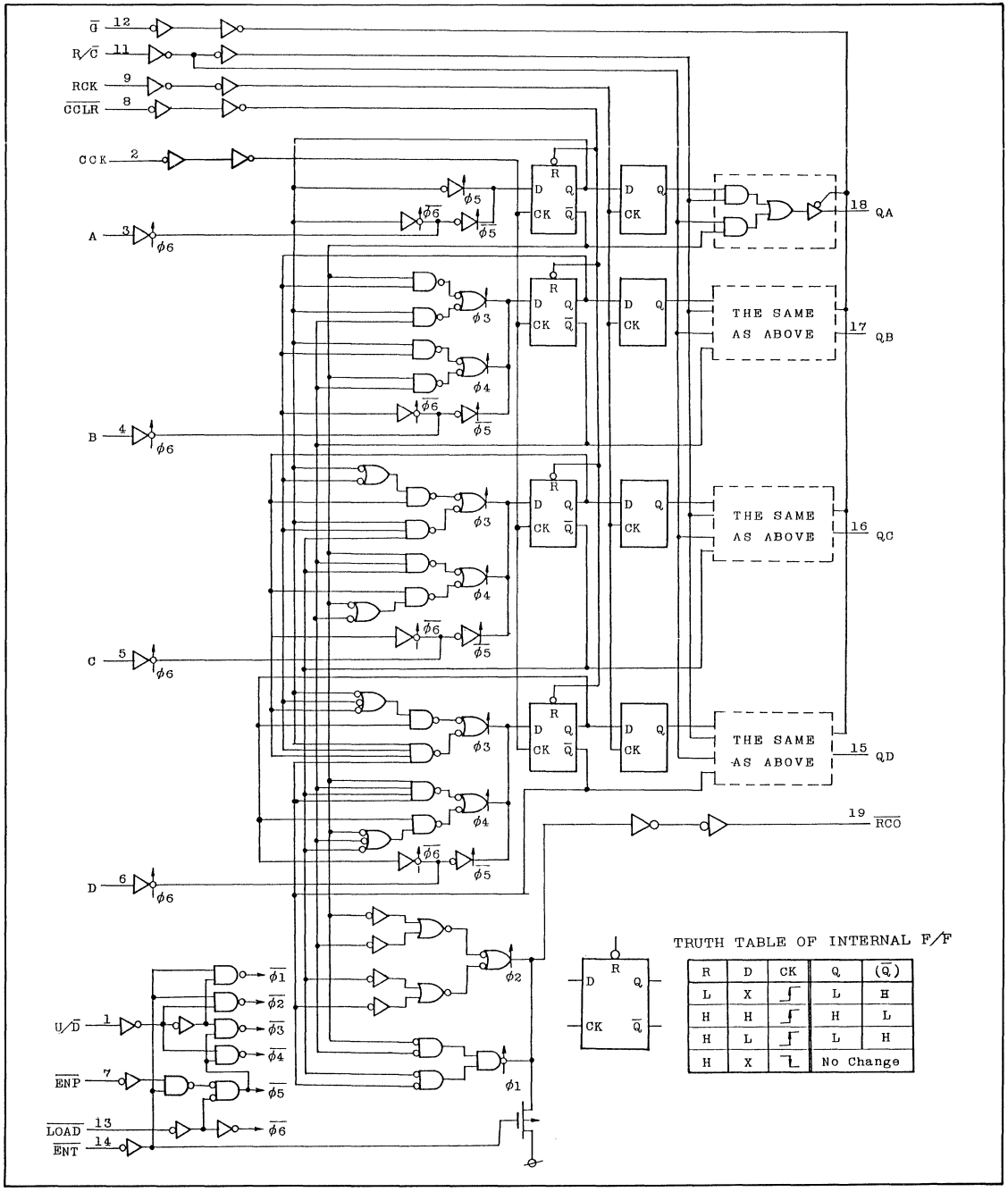
LOGIC DIAGRAM TC74HC698



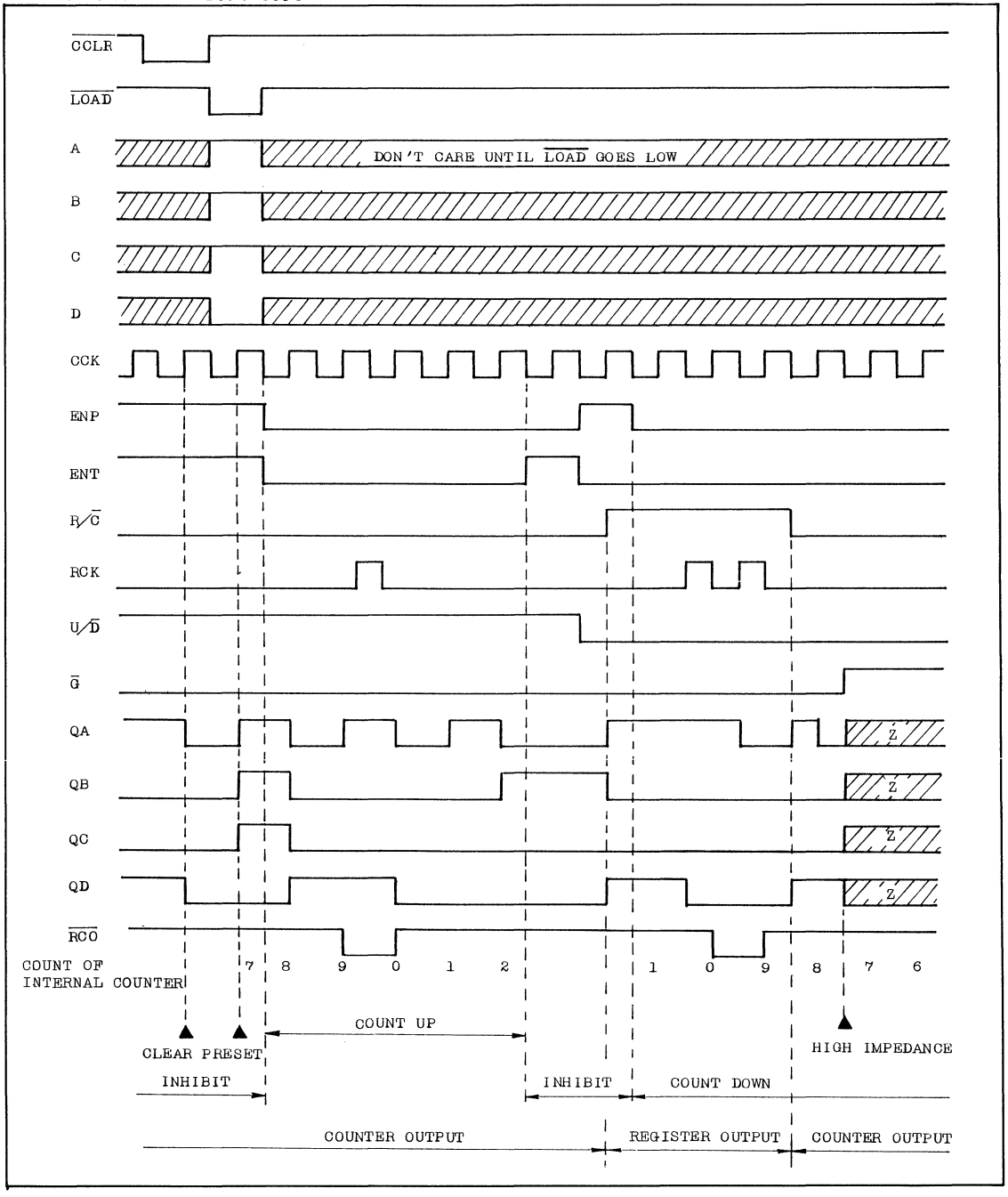
TRUTH TABLE OF INTERNAL F/F

R	D	CK	Q	($\overline{Q}$)
L	X	↓	L	H
H	H	↓	H	L
H	L	↓	L	H
H	X	↑	No Change	

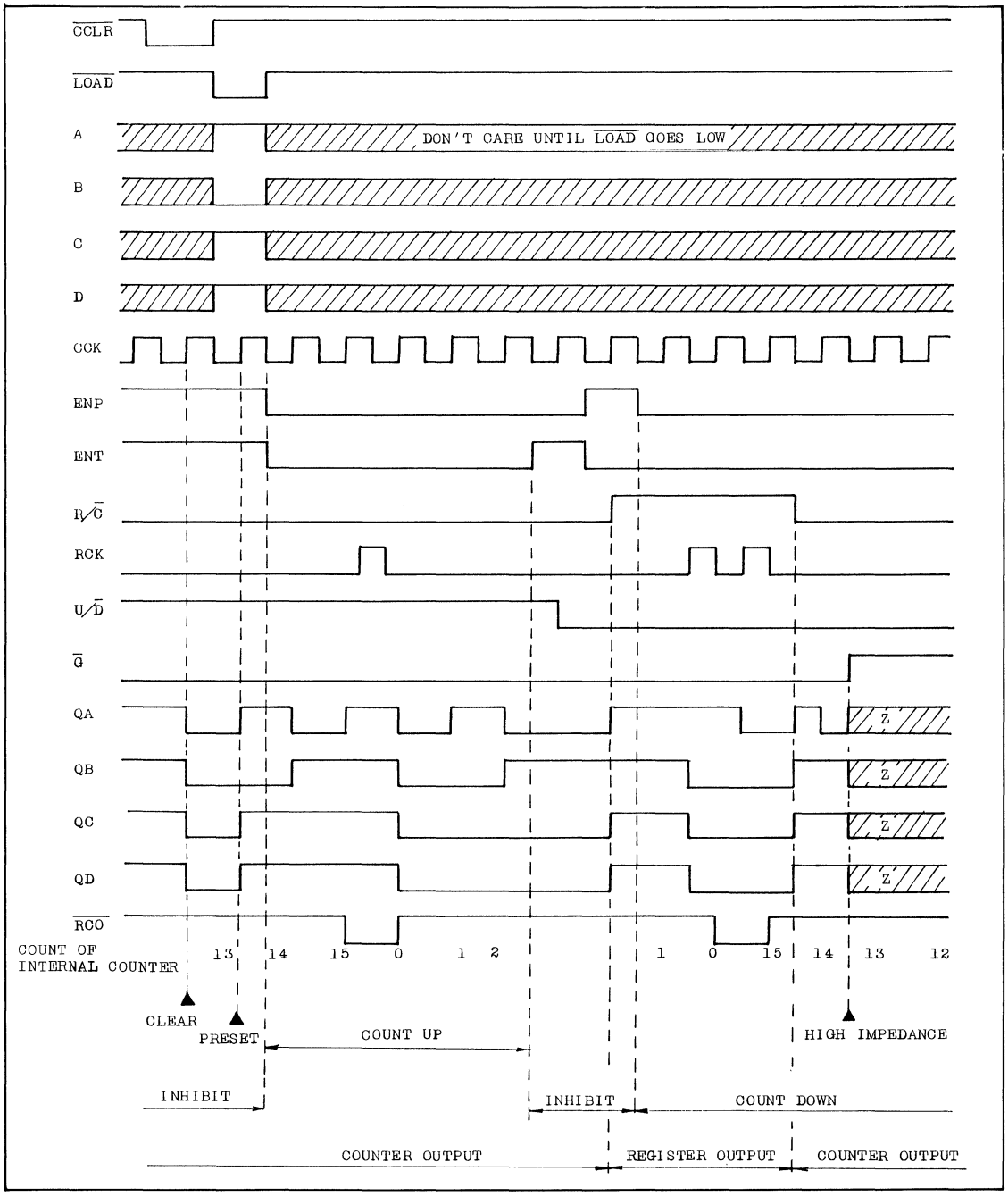
LOGIC DIAGRAM TC74HC699



TIMING CHART TC74HC698



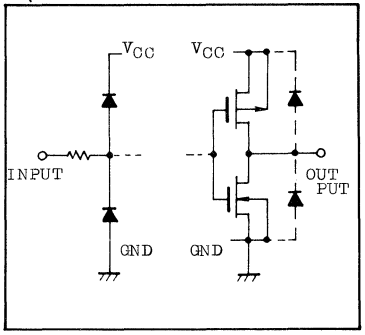
TIMING CHART TC74HC699



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	144	275	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Maximum Clock Frequency (CCK, RCK)	f_{MAX}		2.0	3.5	7	-	2.5	-	MHz
			4.5	18	28	-	14	-	
			6.0	21	33	-	16	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	44	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	84	200	-	250	
			4.5	-	21	40	-	50	
			6.0	-	18	34	-	43	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

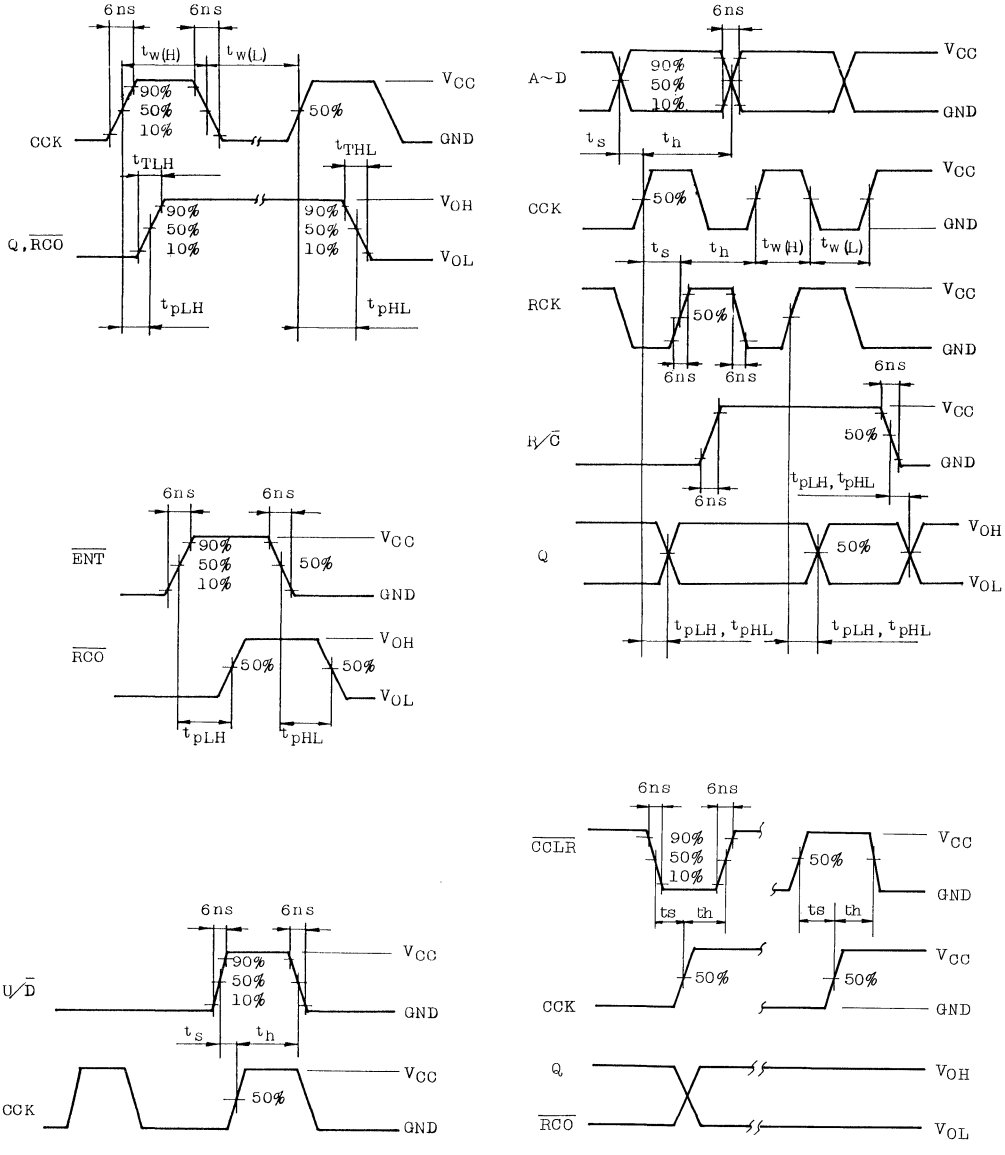
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Minimum Set-up Time ($\overline{CCLR}$)	t_s		2.0	-	12	50	-	65	ns
			4.5	-	3	10	-	13	
			6.0	-	2.5	9	-	11	
Minimum Set-up Time (U/$\overline{D}$)	t_s		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Hold Time	t_h		2.0	-	-	25	-	36	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	145	-	180	
			4.5	-	20	29	-	36	
			6.0	-	17	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD} (1)			-	113	-	-	-	

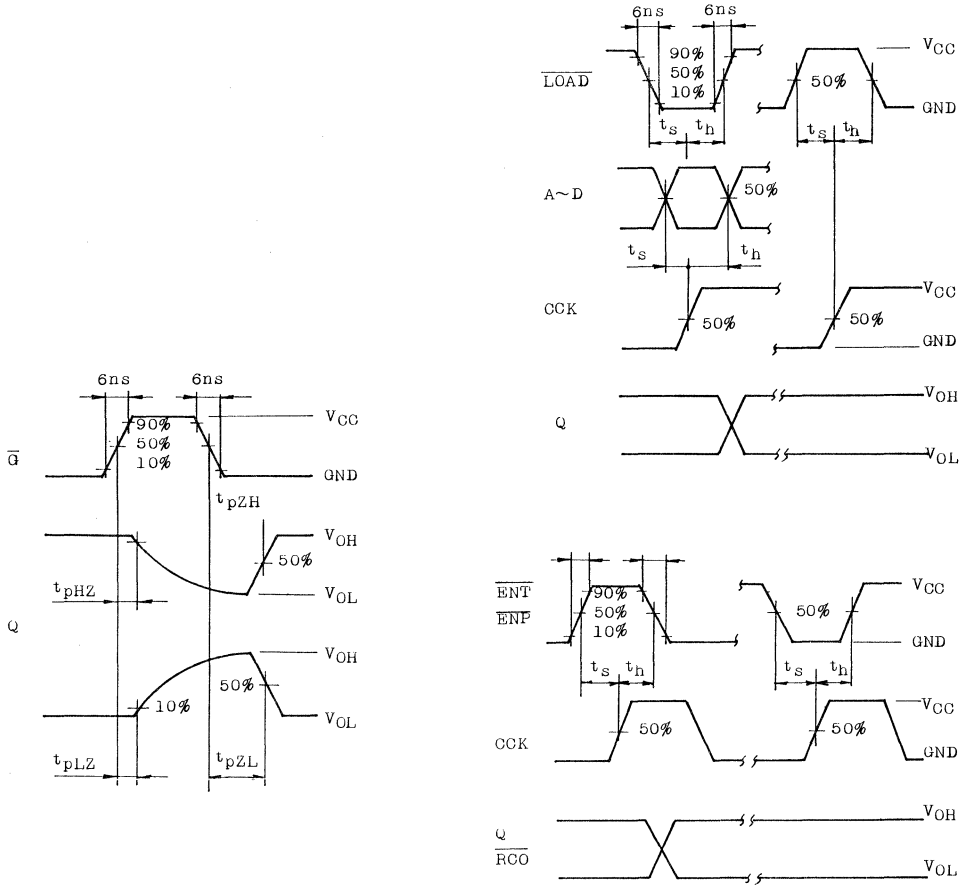
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.)=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

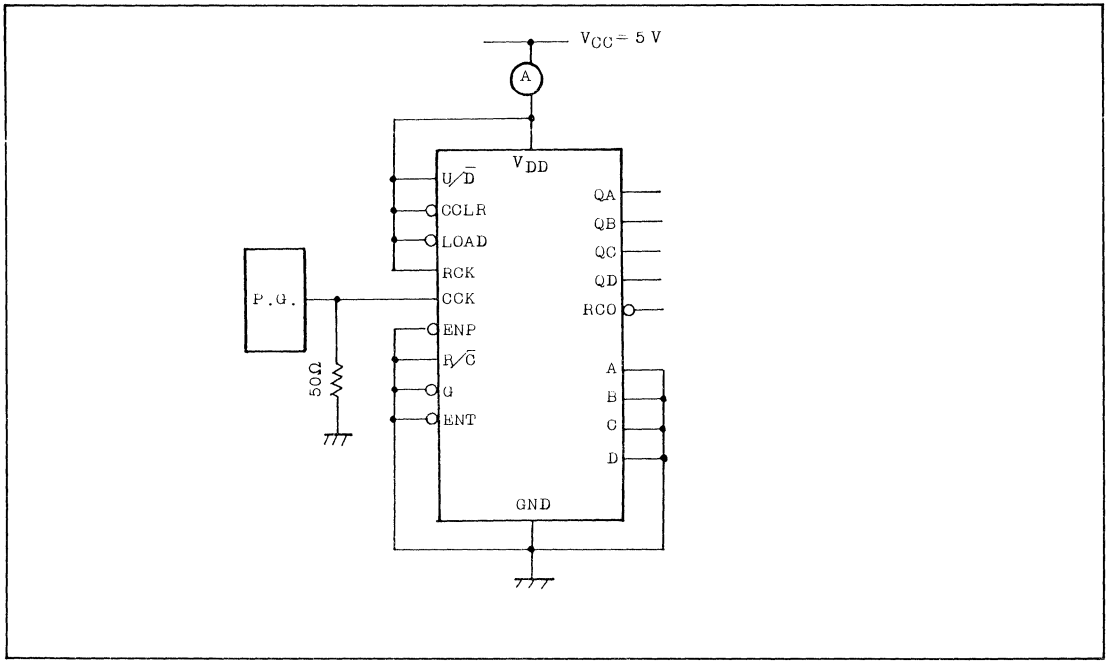
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT



TC74HC4002AP/AF

DUAL 4-INPUT NOR GATE

The TC74HC4002A is a high speed CMOS 4-INPUT NOR GATE fabricated with sillicon gate C^2MOS technology.

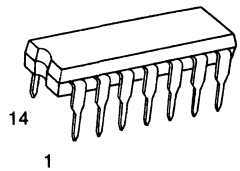
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

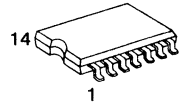
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4002B.

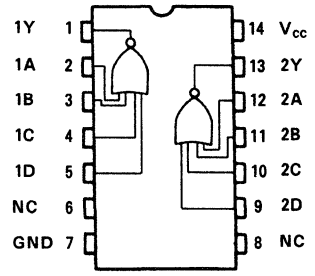


DIP14 (3D14A-P)



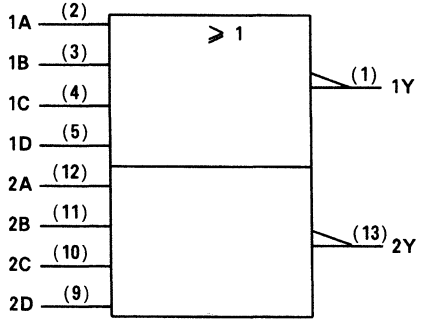
MFP14 (F14GB-P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	22	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

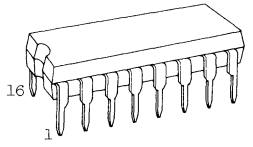
TC74HC4017P/F

TC74HC4017P/F DECADE COUNTER/DIVIDER

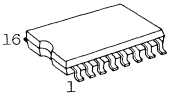
The TC74HC 4017 is a high speed CMOS DECADE JOHNSON COUNTER fabricated with silicon C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 5-stage divided-by-10 Johnson counter with 10 decoded output (Q0 - Q10) and carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{CE}$ input is held low, or it is advanced on the negative edge of the clock enable signal ($\overline{CE}$) when CLOCK input is held high, and selected one of ten outputs goes high. Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4017B



DIP16(3D16A-P)



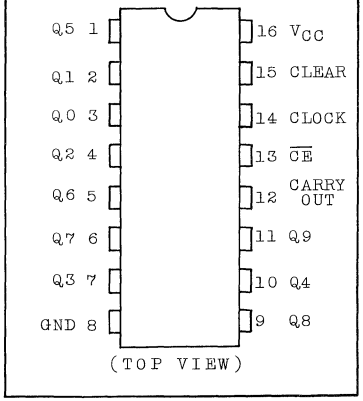
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



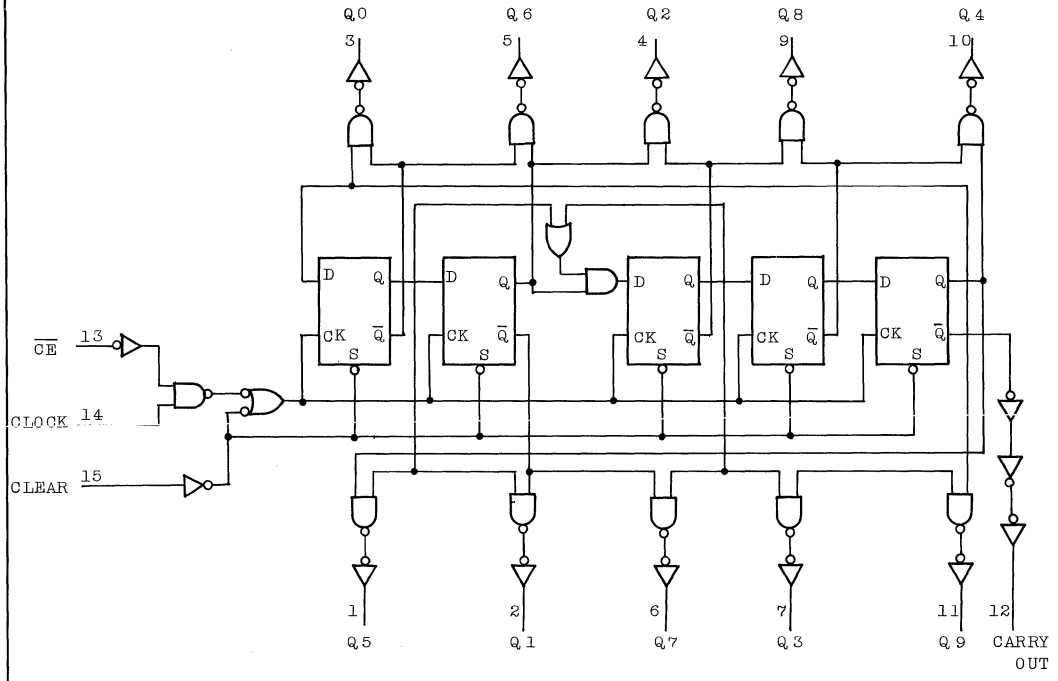
(TOP VIEW)

TRUTH TABLE

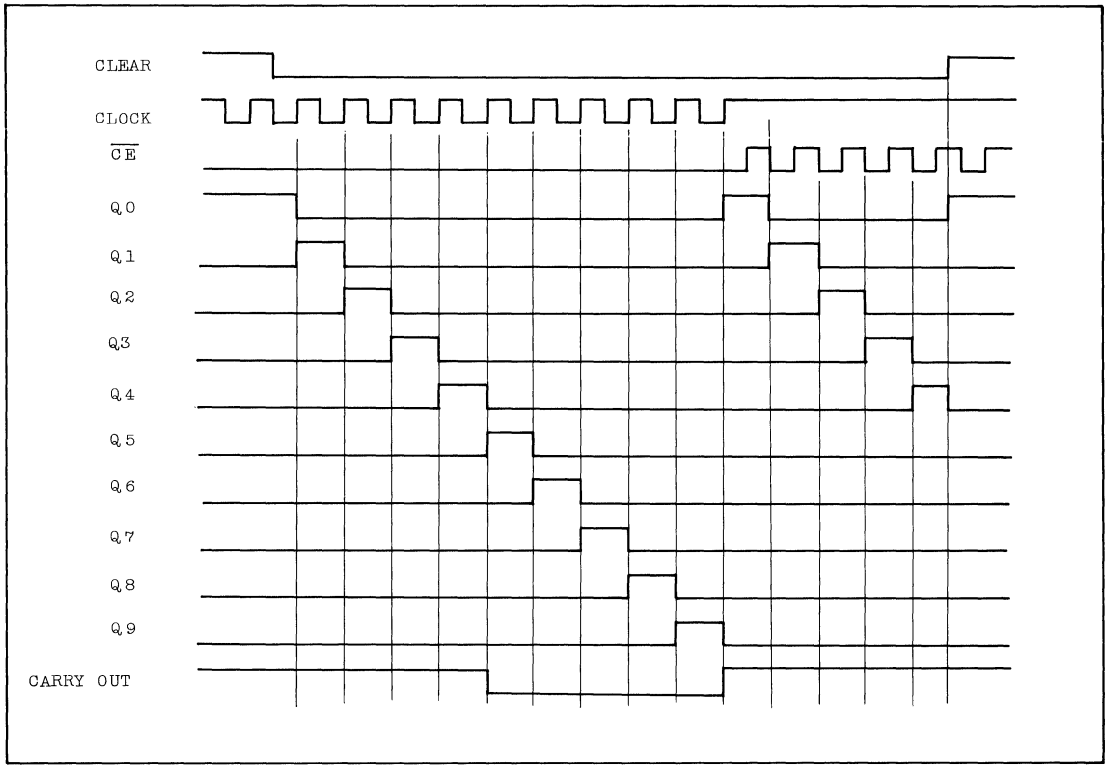
CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↓	L	L	Qn+1
↓	L	L	Qn
H	↓	L	Qn
H	↓	L	Qn+1

X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



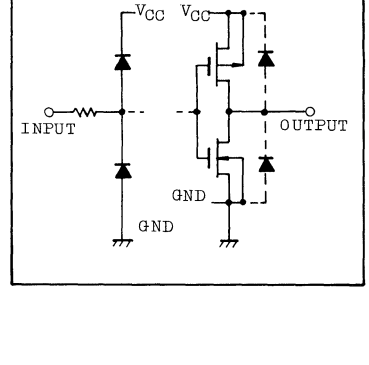
TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK, $\overline{CE}$ - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

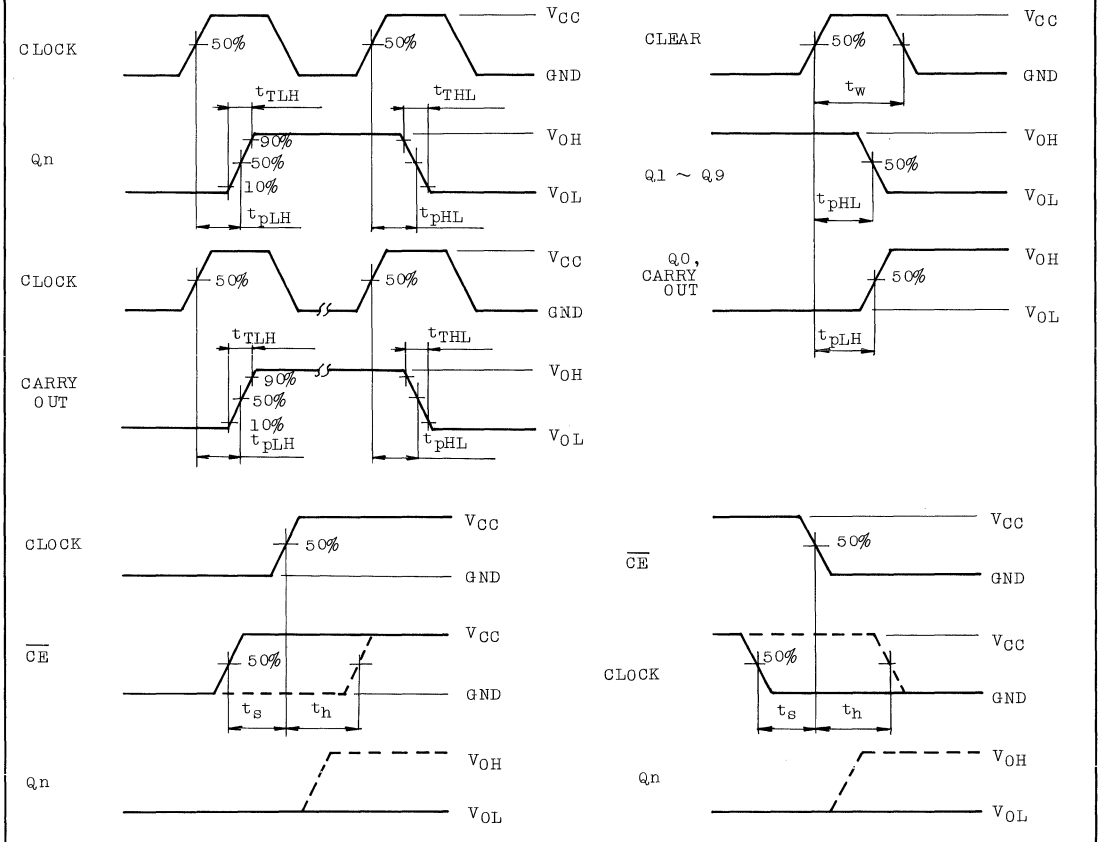
AC ELECTRICAL CAHRACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	41	-	20	-	
			6.0	29	48	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	74	-	-	-	

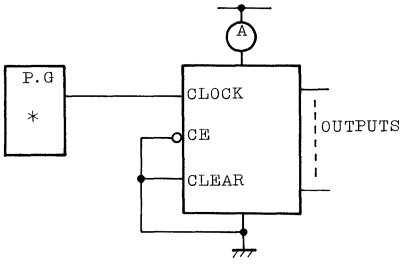
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

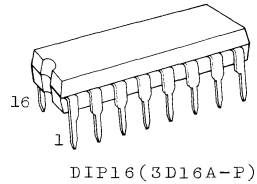
TC74HC4020P/F

TC74HC4020P/F 14-STAGE BINARY COUNTER

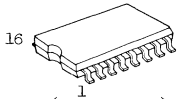
The TC74HC4020 is a high speed CMOS 14-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4020B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accoumplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. Twelve kinds of divided output are provided; 1'st and 4 stage thru 14 stage. And at the last stage, 1/16384 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V∿6V
- Pin and Function Compatible with 4020B.



DIP16(3D16A-P)



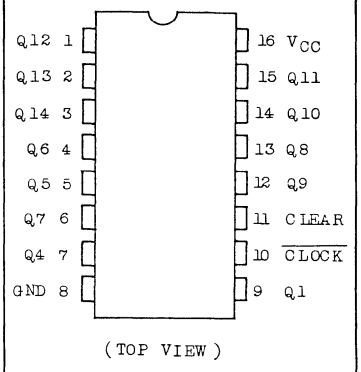
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



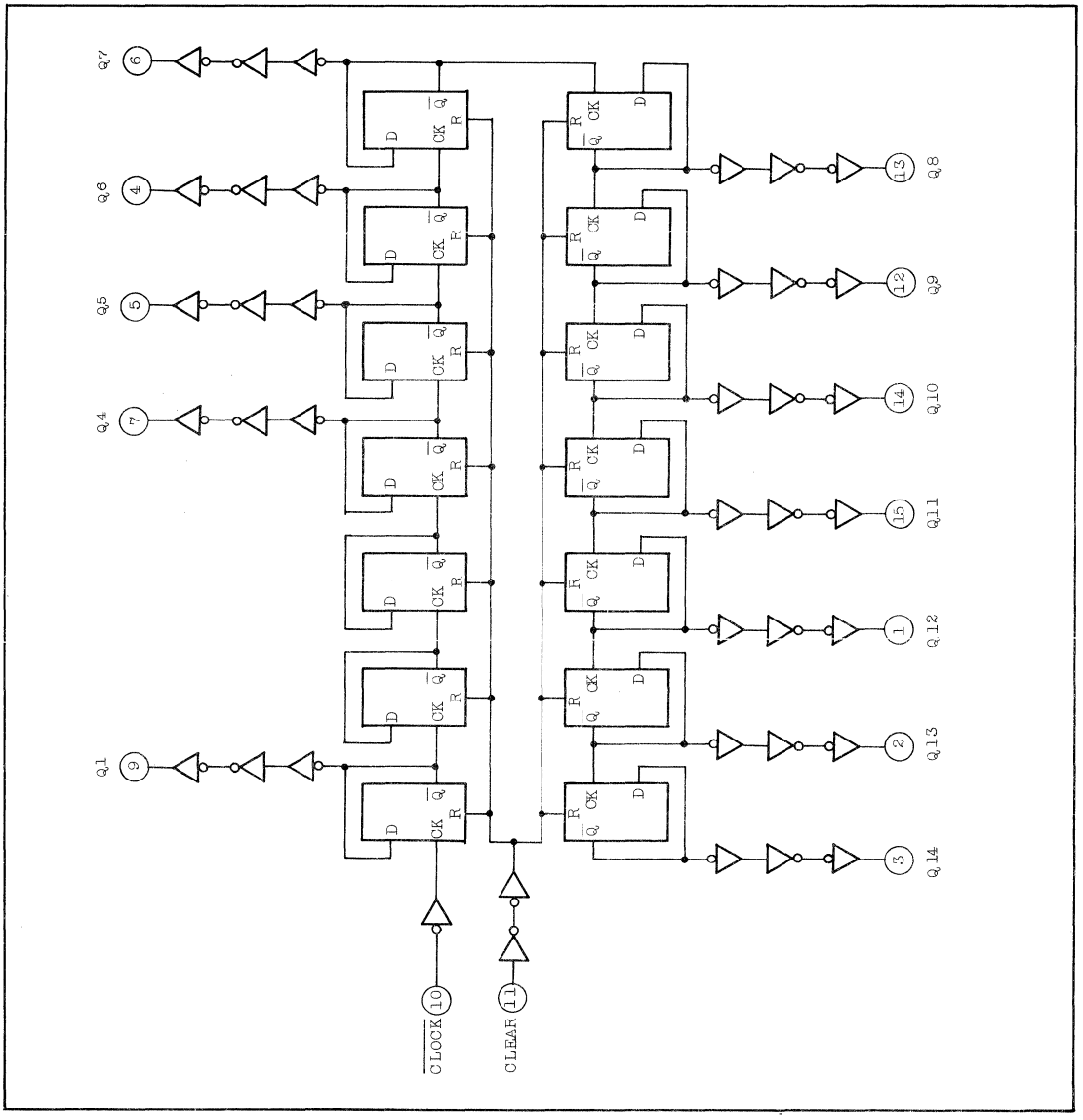
(TOP VIEW)

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⌐	L	NO CHANGE
¬	L	ADVANCE TO NEXT STATE

X : DON'T CARE

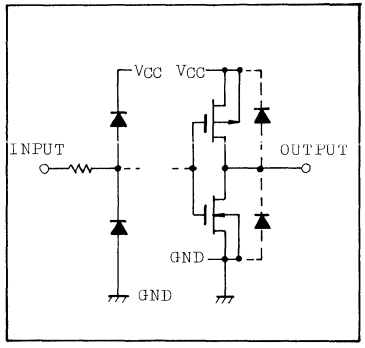
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

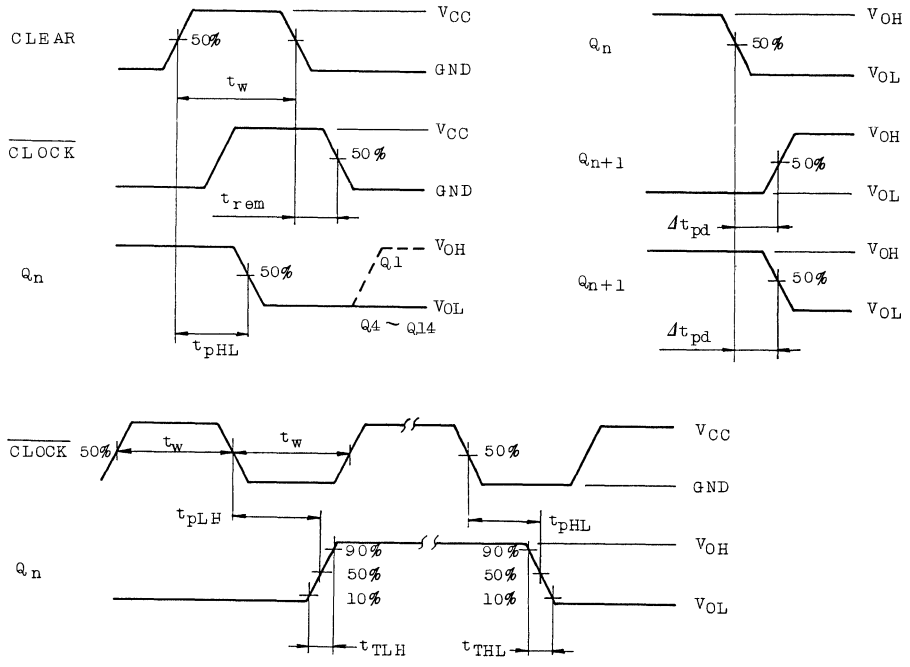
AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q_1)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time Difference (Q_n - Q_{n+1})	Δt_{pd}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time (CLEAR)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	23	-	-	-	

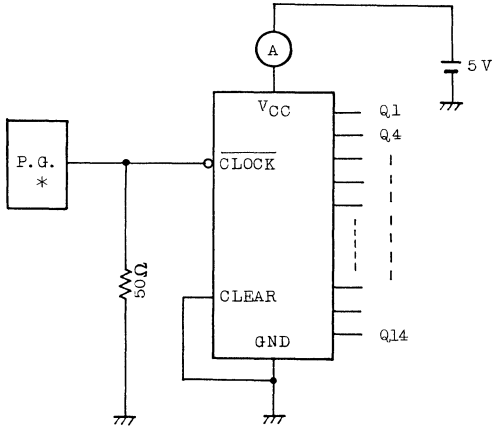
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

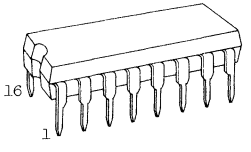
TC74HC4022P/F

TC74HC4022P/F OCTAL COUNTER/DIVIDER

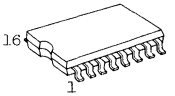
The TC74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 4-stage divide-by-8 Johnson counter with 8 decoded output ($Q_0 - Q_7$) and Carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{\text{CLOCK ENABLE}}$ input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high.
Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=43MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}= 4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4022B



DIP16(3D16A-P)



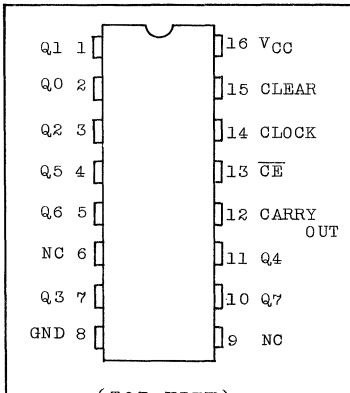
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



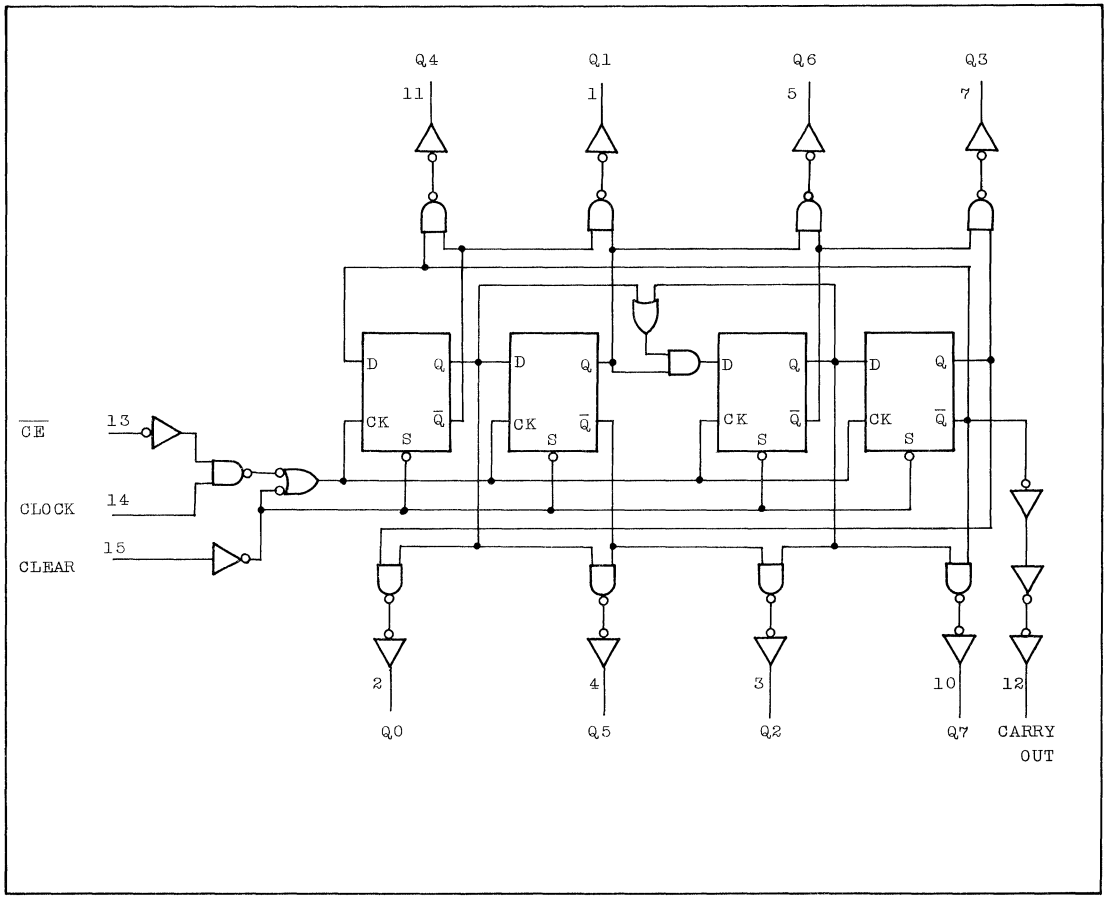
(TOP VIEW)

TRUTH TABLE

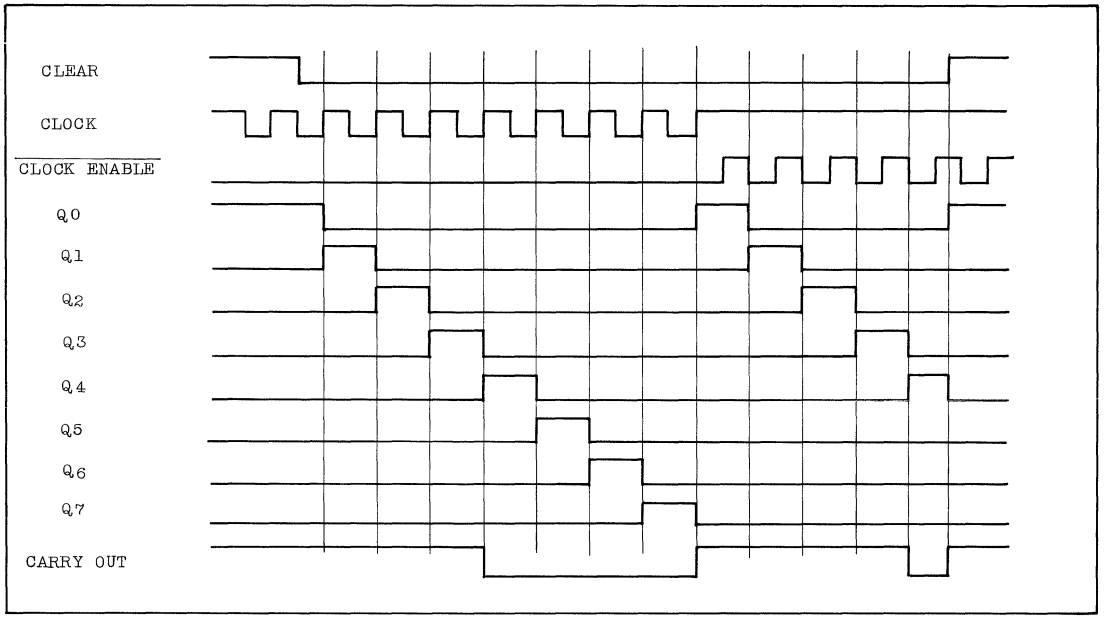
CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↓	L	L	Qn+1
↑	L	L	Qn
H	↓	L	Qn
H	↑	L	Qn+1

X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



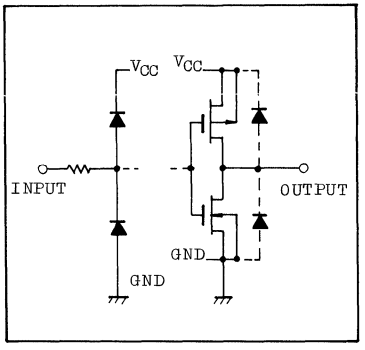
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Suppl Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

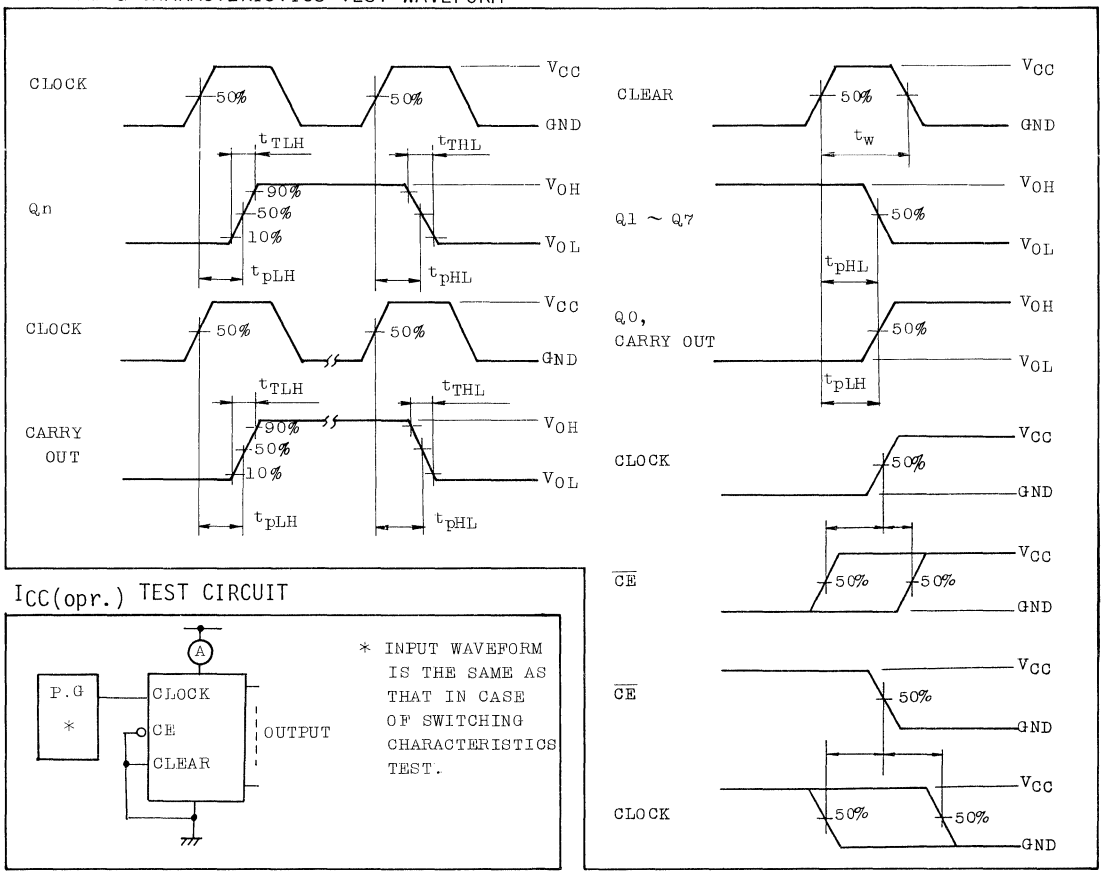
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Maximum Clock frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	40	-	20	-	
			6.0	29	47	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	52	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

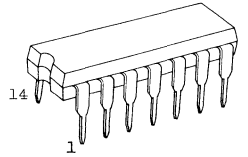
TC74HC4024P/F

TC74HC4024P/F 7-STAGE BINARY COUNTER

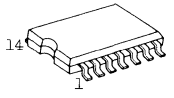
The TC74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4024B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the $\overline{CLOCK}$ input brings one increment to the counter. Seven kinds of divided output are provided; 1'st and 4 stage thru 7 stage. And at the last stage, 1/128 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 4024B.



DIP14(3D14A-P)



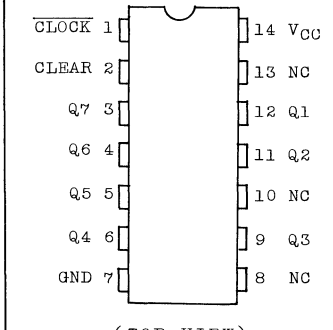
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



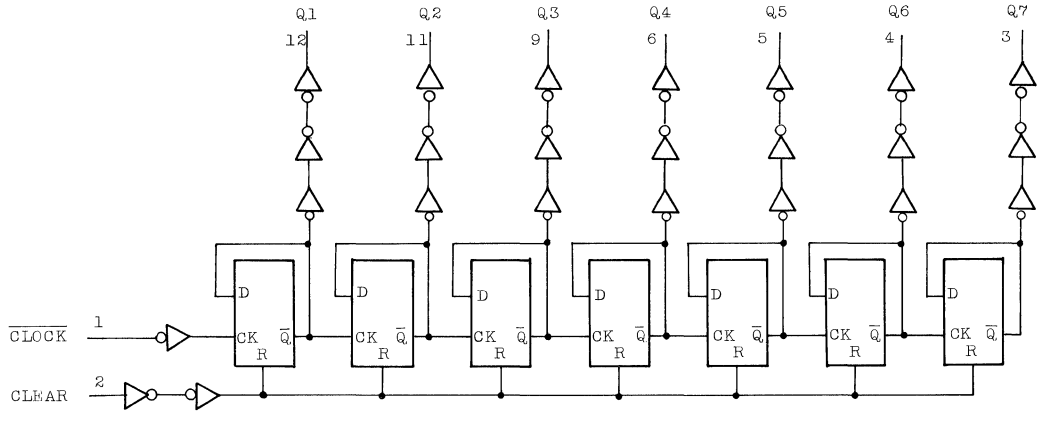
(TOP VIEW)

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

X : DON'T CARE

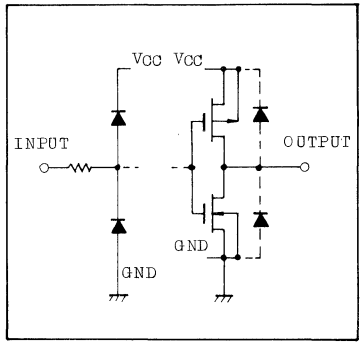
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

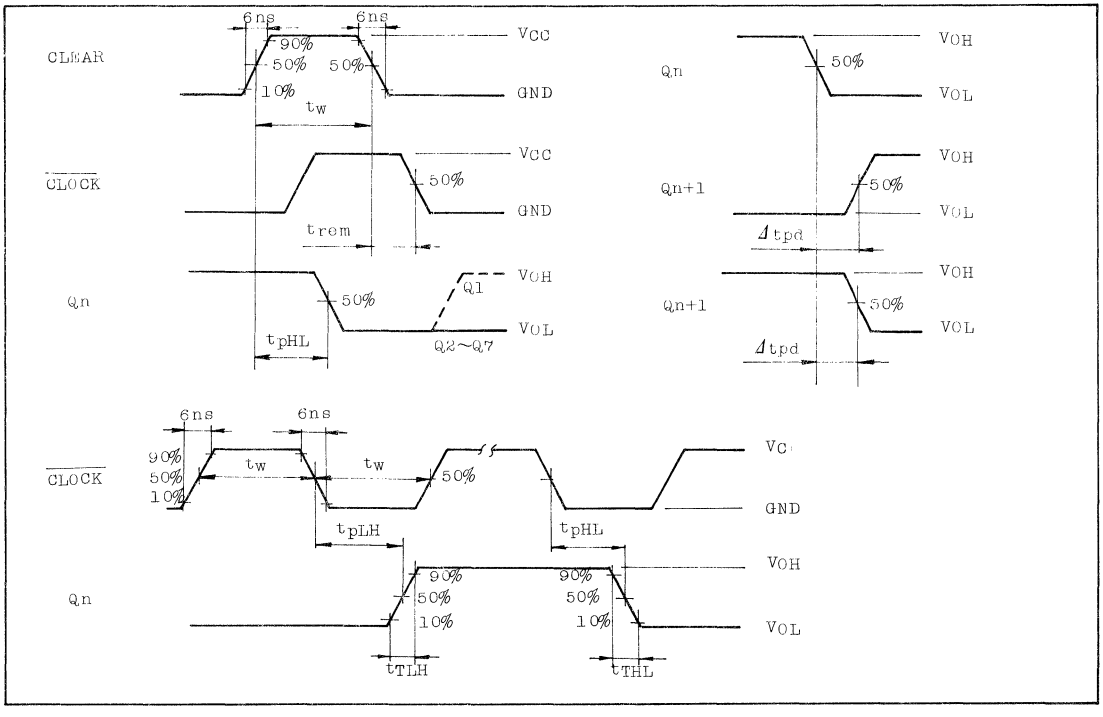
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time Difference (Qn - Qn+1)	Δtpd		2.0	-	28	60	-	75	
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

AC ELECTRICAL CHARACTERISTICS (Continued)

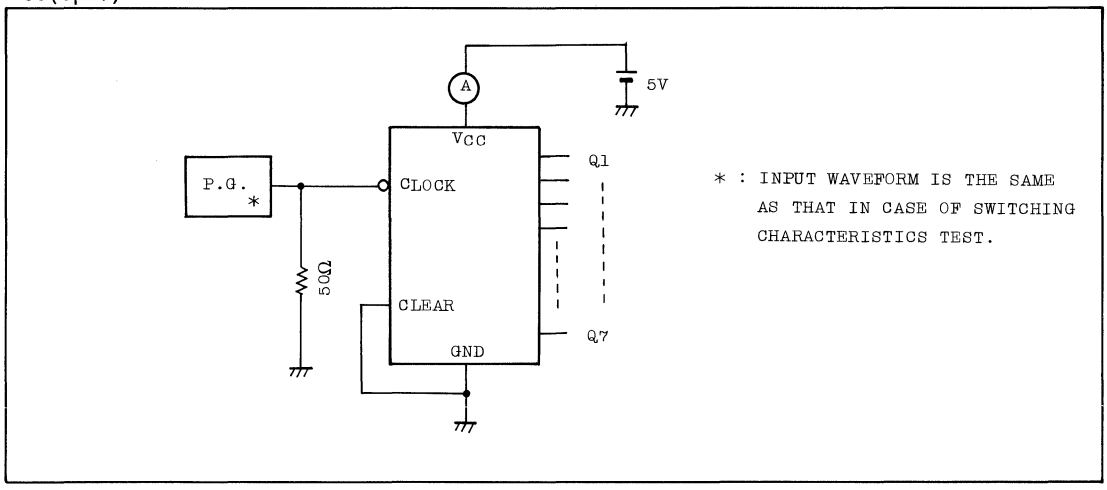
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	42	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

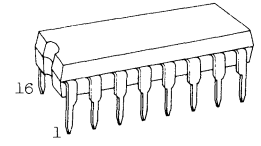
TC74HC4028P/F

TC74HC4028P/F BCD-TO-DECIMAL DECODER

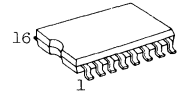
The TC74HC4028 is a high speed CMOS DECIMAL DECODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
A BCD code applied to the four input (A thru D) provides a high level at the selected one of the decimal decoded outputs. A illegal BCD code such as eleven to fifteen gives a low level at all outputs.
The device also can be used as 3-to-8 LINE DECODER, when D input is assigned as a disable input.
The device is useful for code conversion, address decoding, memory selection, demultiplexing, or read out decoding.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=25ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays.....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range....$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4028B

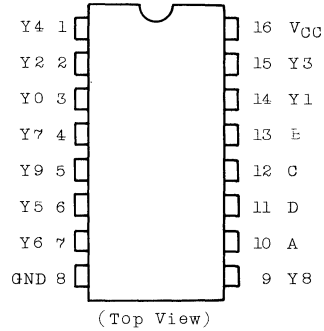


DIP16(3D16A-P)



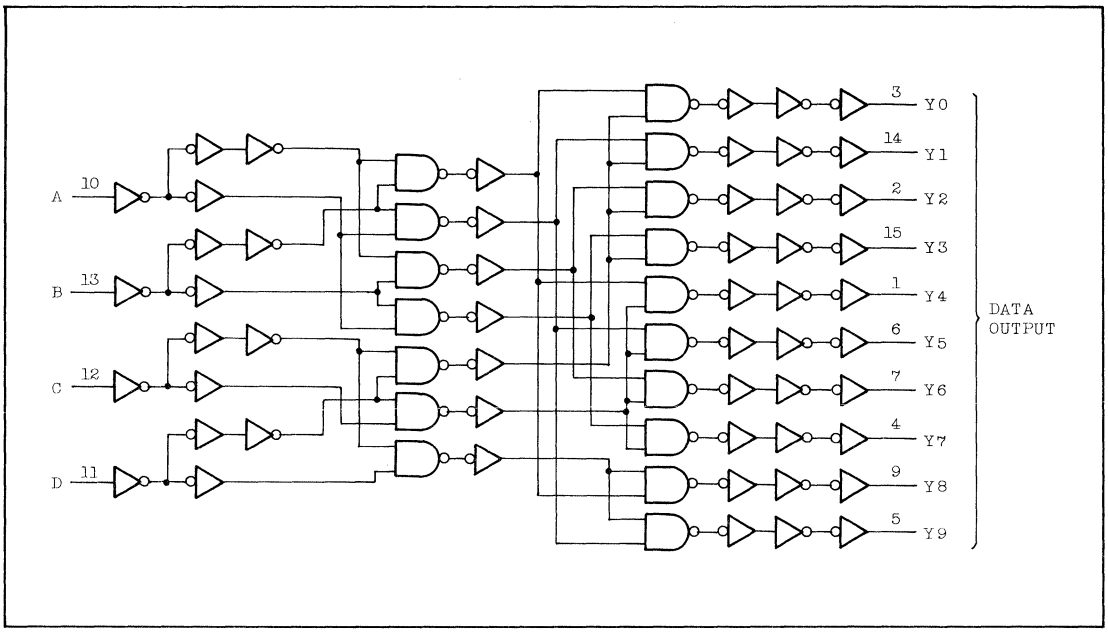
MFP16(F16GC-P)

PIN ASSIGNMENT



(Top View)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS										SELECTED OUTPUT
D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y_0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y_1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y_2
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y_3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y_4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y_5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y_6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y_7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y_8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y_9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

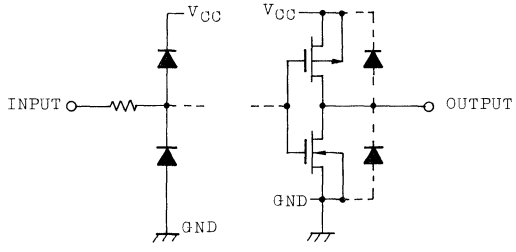
X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

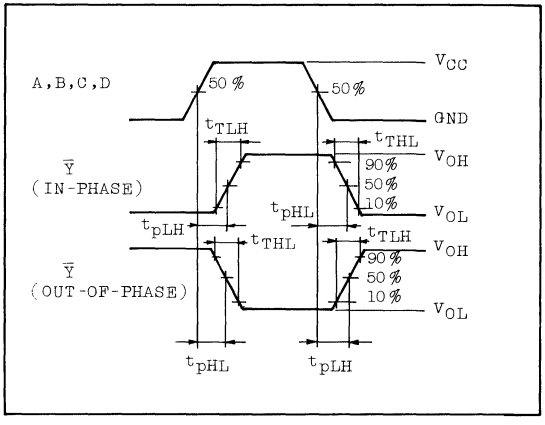
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A,B,C,D)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	58	-	-	-	

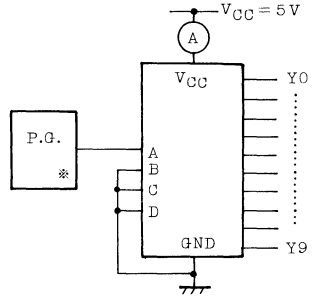
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



※ Input transition time is the same as that in case of switching characteristics test.

TC74HC4040P/F

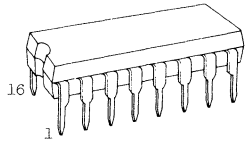
TC74HC4040P/F 12-STAGE BINARY COUNTER

GENERAL DESCRIPTION

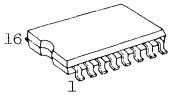
The TC74HC4040 is a high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4040B) with the same power dissipation.
A clear input is used to reset the counter to all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. All divided output stages are provided, and 1/4096 divided frequency will obtained at the last stage.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V∿6V
- Pin and Functional Compatible with 4040B.



DIP16(3D16A-P)



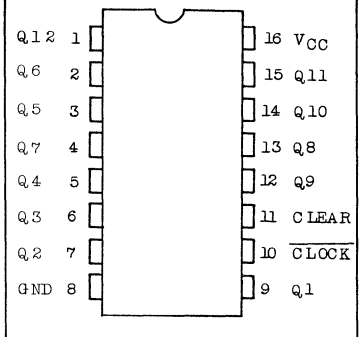
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



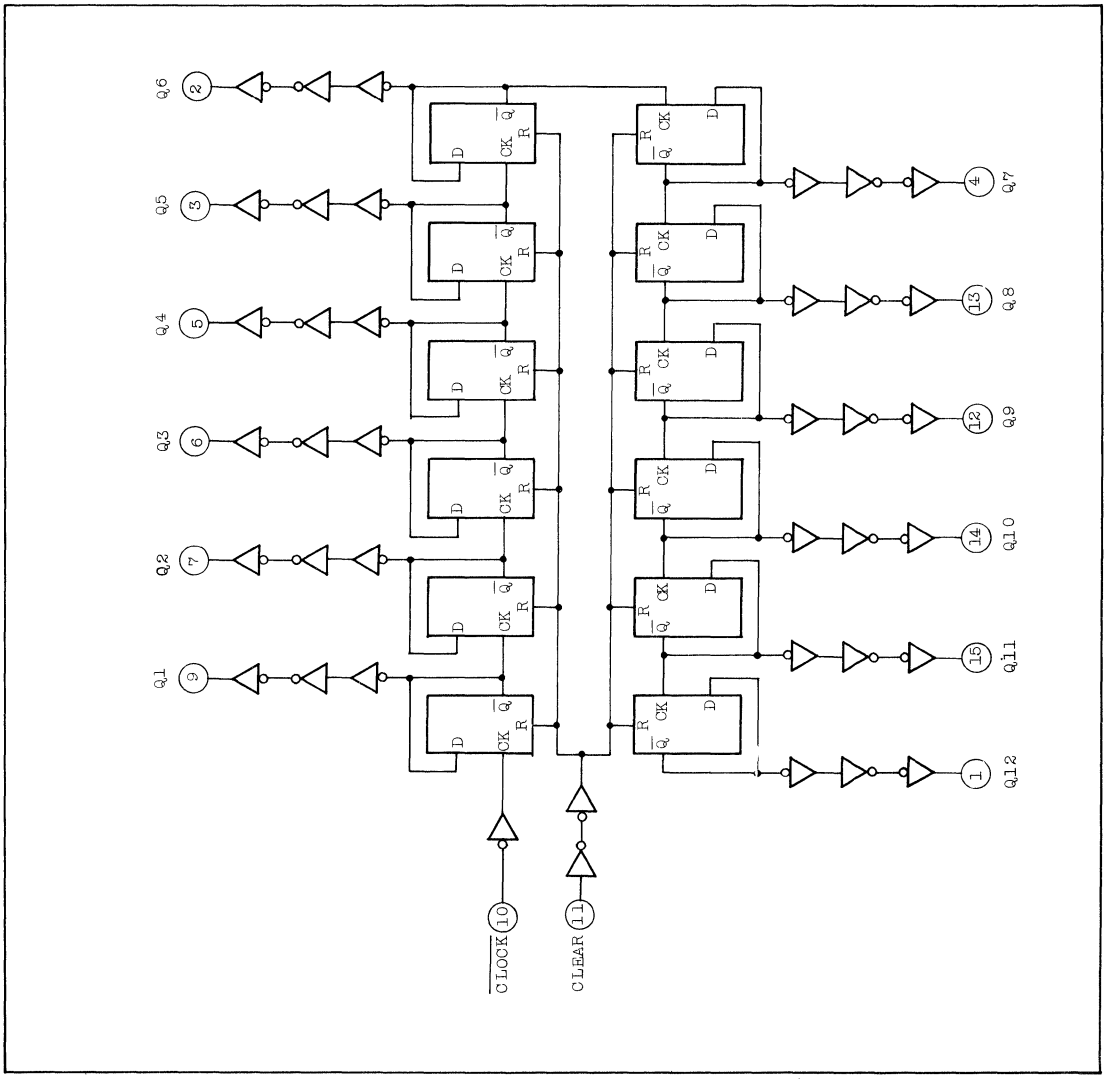
(TOP VIEW)

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⌐‾	L	NO CHANGE
‾⌐	L	ADVANCE TO NEXT STATE

X : DON'T CARE

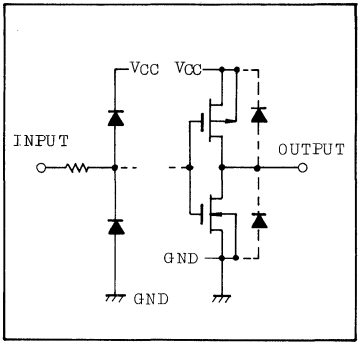
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

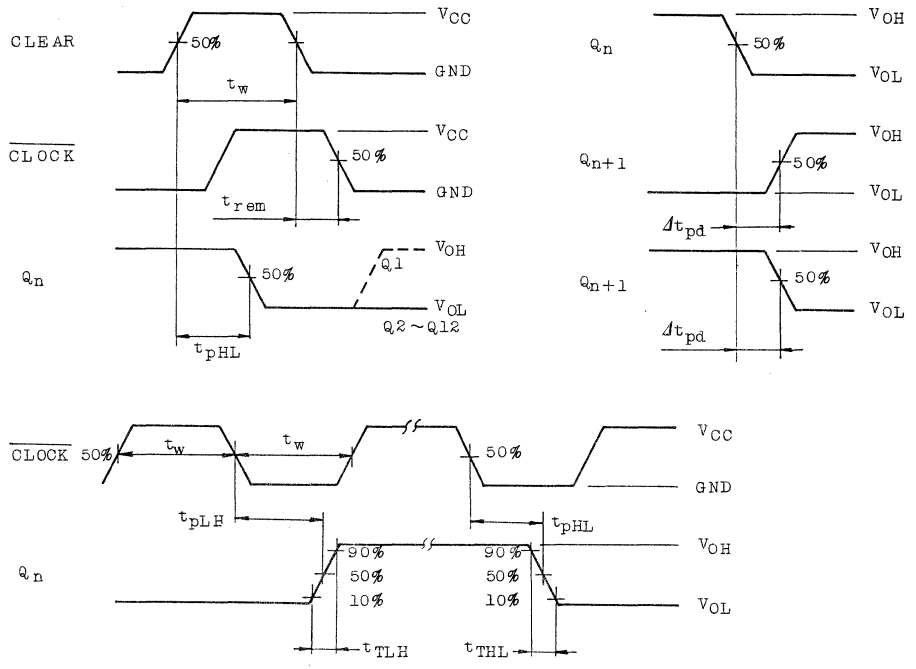
AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
($\overline{CLOCK}$ - Q_1)	t_{pHL}		6.0	-	15	25	-	31	
Propagation Delay Time Difference (Q_n - Q_{n+1})	Δt_{pd}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time (CLEAR)	t_{pHL}		2.0	-	104	205	-	225	
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	32	-	-	-	

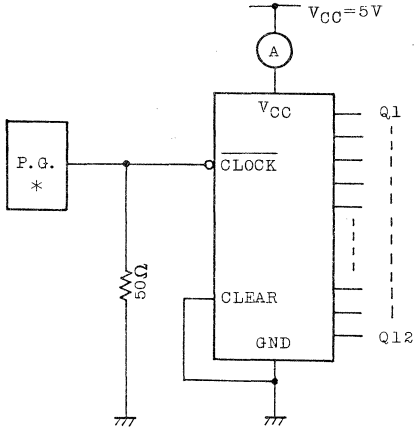
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

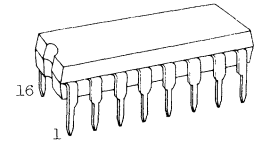
TC74HC4049 P/ F HEX BUFFER/CONVERTER (INVERTING)

TC74HC4050 P/ F HEX BUFFER CONVERTER

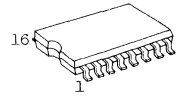
The TC74HC4049 and the TC74HC4050 are high speed CMOS HEX BUFFER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC4049 is an inverting buffer, while the TC74HC4050 is a non-inverting buffer.
The internal circuit is composed of 3-stage or 2-stage inverters, which enables high noise immunity and stable output.
Input protection circuits are different from those of the high speed CMOS IC's.
They eliminate diodes of V_{CC} side and enable logic-level conversion from high-level voltage (up to 15V) to low-level voltage.
These IC's are useful for battery back up circuits, because input voltage can be appled on IC's which is not biased by V_{CC}.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4049B, 4050B.



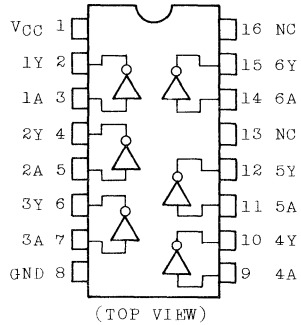
DIP16(3D16A-P)



MFP16(F16GC-P)

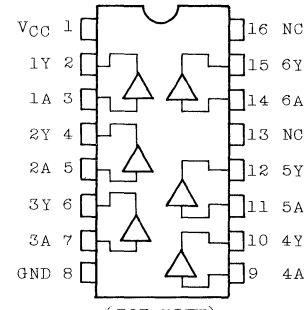
PIN ASSIGNMENT

TC74HC4049



(TOP VIEW)

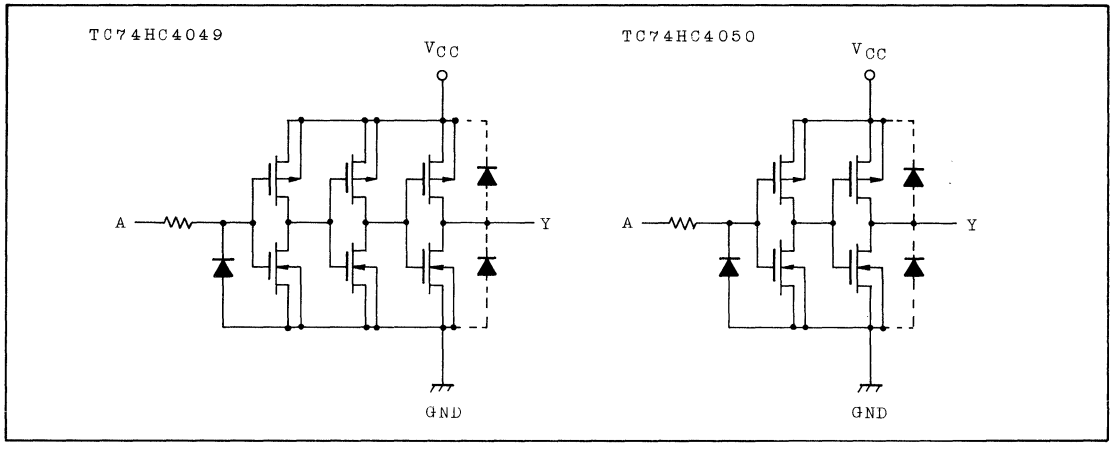
TC74HC4050



(TOP VIEW)

NC : No Connection

CIRCUIT SCHEMATIC (per Gate)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ 18*	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)**/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

Note.
*DC input voltage is able to impress -0.5V to 18V based on GND without any relation to voltage of V_{CC}. Recommended operating condition is from 0V to 15V and it is possible to vonvert logic-level from 15V to 5V or 5V to 2V.

**500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ 15	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

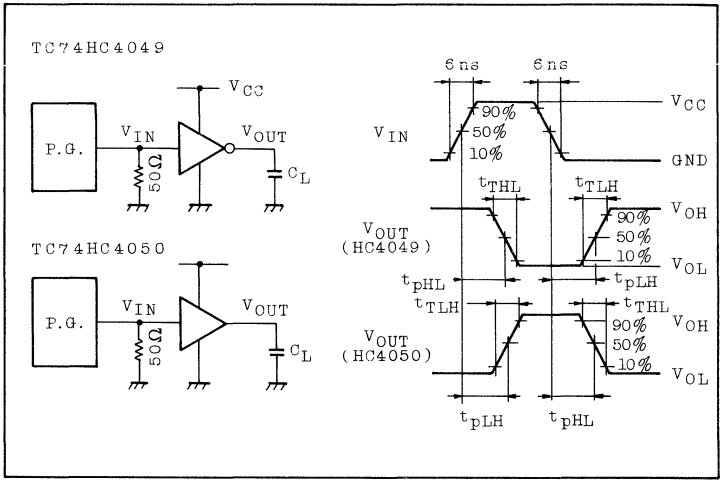
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

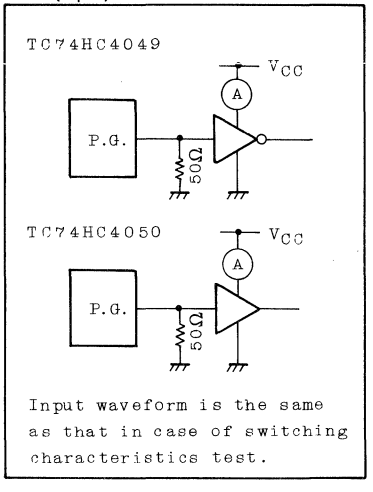
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC4051AP/AF
TC74HC4052AP/AF
TC74HC4053AP/AF/AFN

TC74HC4051AP/AF 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4052AP/AF DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4053AP/AF/AFN TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel × 2 configuration and the TC74HC4053A has a 2 channel × 3 configuration.

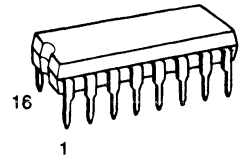
The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ($V_{CC}-V_{EE}$) can then be switched by the small logical amplitude (V_{CC}-GND) control signal.

For example, in the case of V_{CC}=5V, GND=0V, V_{EE}=−5V, signals between −5V and + 5V can be switched from the logical circuit with a single power supply of 5V. As the ON−resistance of each switch is low, they can be connected to circuits with low input impedance.

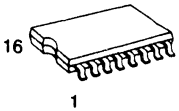
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

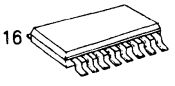
- High Speed ····· t_{pd}=15ns(typ.)atV_{CC}=5V,V_{EE}=0V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Low ON Resistance ····· R_{ON}=50Ω(typ.)at $V_{CC}-V_{EE}$=9V
- High Degree of Linearity ··· THD=0.02%(typ.)at $V_{CC}-V_{EE}$=9V
- Pin and Function Compatible with 4051/4052/4053B



DIP16 (3D16A−P)

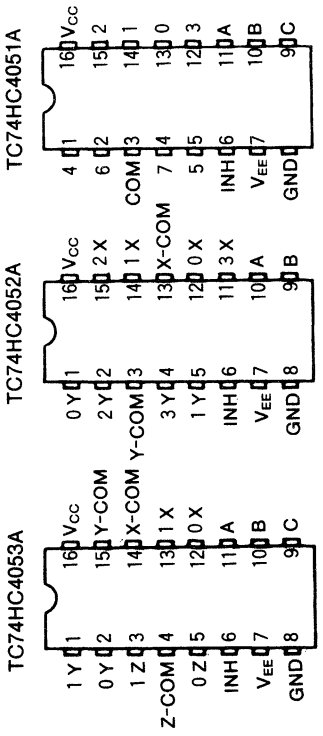


MFP 16
(F16GC−P)



SOP 16
(SOP16−P−225A)

PIN ASSIGNMENT

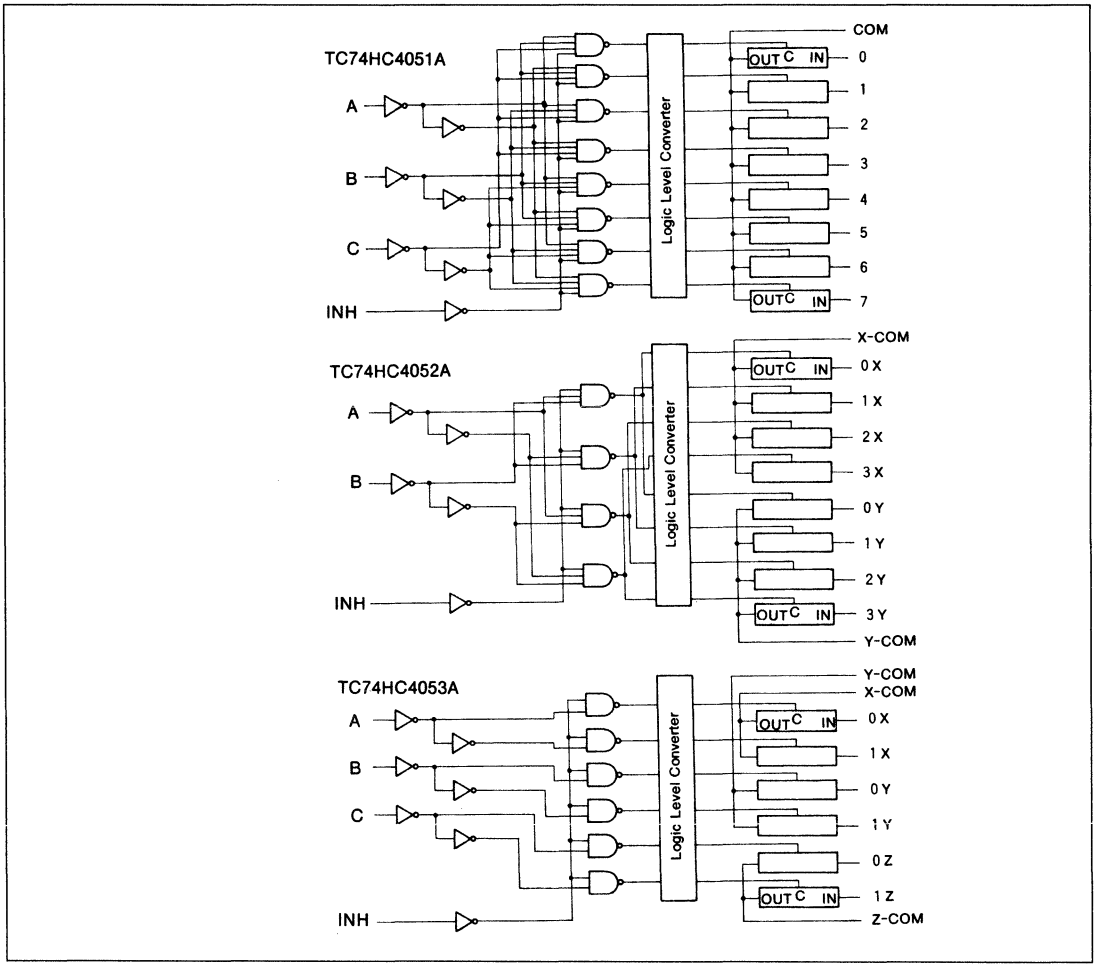


TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	— —	0X, 0Y, 1Z
L	H	L	H	5	— —	1X, 0Y, 1Z
L	H	H	L	6	— —	0X, 1Y, 1Z
L	H	H	H	7	— —	1X, 1Y, 1Z
H	X	X	X	NONE	NONE	NONE

X : DON'T CARE, * : Except HC4052A

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

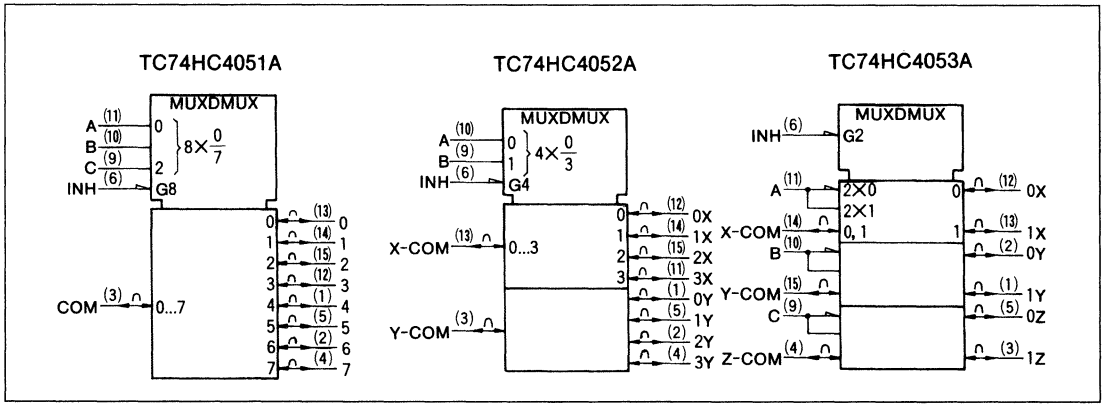
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
Supply Voltage Range	$V_{CC}-V_{EE}$	−0.5 ~13	V
Control Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
Switch I/O Voltage	$V_{I/O}$	V_{EE} −0.5 ~V_{CC}+0.5	V
Control Input Diode Current	I_{CK}	±20	mA
I/O Diode Current	I_{IOK}	±20	mA
Switch through Current	I_T	±25	mA
DC V_{CC} or GND Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	2 ~ 6	V
Supply Voltage Range	V_{EE}	−6 ~ 0	V
Supply Voltage Range	$V_{CC}-V_{EE}$	2 ~ 12	V
Control Input Voltage	V_{IN}	0 ~ V_{CC}	V
Switch I/O Voltage	$V_{I/O}$	V_{EE} ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Control Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

IEC LOGIC SYMBOL



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{EE}	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Control Input Voltage	V_{IHC}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Control Input Voltage	V_{ILC}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
ON Resistance	R_{ON}	$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND	4.5	−	85	180	−	225	Ω
			−4.5	4.5	−	55	120	−	150	
			−6.0	6.0	−	50	100	−	125	
		$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ or V_{EE} $I_{I/O} \leq 2mA$	GND	2.0	−	150	−	−	−	
			GND	4.5	−	70	150	−	190	
			−4.5	4.5	−	50	100	−	125	
			−6.0	6.0	−	45	80	−	100	
Difference of ON Resistance Between Switches	$\triangle R_{ON}$	$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND	4.5	−	10	30	−	35	
			−4.5	4.5	−	5	12	−	15	
			−6.0	6.0	−	5	10	−	12	
Input/Output Leakage Current (SWITCH OFF)	I_{OFF}	$V_{OS}=V_{CC}$ or GND $V_{IS}=$GND or V_{CC} $V_{IN}=V_{ILC}$ or V_{IHC}	GND	6.0	−	−	± 60	−	± 600	nA
			−6.0	6.0	−	−	±100	−	±1000	
Switch Input Leakage Current (SWITCH ON)	I_{IZ}	$V_{OS}=V_{CC}$ or GND $V_{IN}=V_{ILC}$ or V_{IHC}	GND	6.0	−	−	± 60	−	± 600	
			−6.0	6.0	−	−	±100	−	±1000	
Control Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	GND	6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	GND	6.0	−	−	4.0	−	40.0	
			−6.0	6.0	−	−	8.0	−	80.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns, GND=0V)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Phase difference between Input and Output	$\varphi_{I/O}$	ALL TYPES		GND	2.0	−	25	60	−	75	ns
				GND	4.5	−	6	12	−	15	
				GND	6.0	−	5	10	−	13	
				4.5	4.5	−	4	−	−	−	
Output Enable Time	t_{pZL} t_{pZH}	*1	4051	GND	2.0	−	64	225	−	280	
				GND	4.5	−	18	45	−	56	
				GND	6.0	−	15	38	−	48	
				−4.5	4.5	−	18	−	−	−	
		*1	4052	GND	2.0	−	64	225	−	280	
				GND	4.5	−	18	45	−	56	
				GND	6.0	−	15	38	−	48	
				−4.5	4.5	−	18	−	−	−	
		*1	4053	GND	2.0	−	50	225	−	280	
				GND	4.5	−	14	45	−	56	
				GND	6.0	−	12	38	−	48	
				−4.5	4.5	−	14	−	−	−	
Output Disable Time	t_{pLZ} t_{pHZ}	*1	4051	GND	2.0	−	100	250	−	315	
				GND	4.5	−	33	50	−	63	
				GND	6.0	−	28	43	−	54	
				−4.5	4.5	−	29	−	−	−	
		*1	4052	GND	2.0	−	100	250	−	315	
				GND	4.5	−	33	50	−	63	
				GND	6.0	−	28	43	−	54	
				−4.5	4.5	−	29	−	−	−	
		*1	4053	GND	2.0	−	95	225	−	280	
				GND	4.5	−	30	45	−	56	
				GND	6.0	−	26	38	−	48	
				−4.5	4.5	−	26	−	−	−	
Control Input Capacitance	C_{in}	ALL TYPES		−	−	−	5	10	−	10	pF
COMMON Terminal Capacitance	C_{IS}		4051	−5.0	5.0	−	36	70	−	70	
			4052			−	19	40	−	40	
			4053			−	11	20	−	20	
SWITCH Terminal Capacitance	C_{OS}		4051	−5.0	5.0	−	7	15	−	15	
			4052			−	7	15	−	15	
			4053			−	7	15	−	15	
Feedthrough Capacitance	C_{IOS}		4051	−5.0	5.0	−	0.95	2	−	2	
			4052			−	0.85	2	−	2	
			4053			−	0.75	2	−	2	
Power Dissipation Capacitance	C_{PD}	*2	4051	GND	5.0	−	70	−	−	−	
			4052			−	71	−	−	−	
			4053			−	67	−	−	−	

* 1: R_L=1kΩ

* 2: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

ANALOG SWITCH CHARACTERISTICS(GND=0V,Ta=25°C)

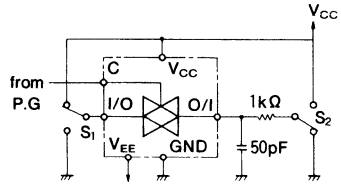
PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	V_{CC}	TYP.	UNIT
Sine Wave Distortion (T.H.D)		R_L=10kΩ, C_L=50pF, f_{IN}=1kHz	V_{IN}=4.0V_{P-P}		−2.25	2.25	0.025	%
			V_{IN}=8.0V_{P-P}		−4.5	4.5	0.020	
			V_{IN}=11.0V_{P-P}		−6.0	6.0	0.018	
Frequency Response (Switch ON)	f_{MAX}	Adjust f_{IN} Voltage to obtain 0dBm at Vos; Increase f_{IN} Frequency until dB Meter reads−3dB; R_L=50Ω, C_L=10pF, f_{IN}=1MHz, Sine Wave	* 1	ALL	−2.25	2.25	120	MHz
			* 2	4051			45	
				4052			70	
				4053			95	
			* 1	ALL	−4.5	4.5	190	
			* 2	4051			70	
				4052			110	
				4053			150	
			* 1	ALL	−6.0	6.0	200	
			* 2	4051			85	
				4052			140	
				4053			190	
Feedthrough Attenuation (Switch OFF)		Vin is centered at(V_{CC}−V_{EE})/2, Adjust input for 0dBm; R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	
Crosstalk (Control Input to Signal Output)		R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Square Wave (t_r=t_f 6 ns)			−2.25	2.25	60	mV
					−4.5	4.5	140	
					−6.0	6.0	200	
Crosstalk (Between any switches)		Adjust V_{IN} to obtain 0dBm at Input; R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	

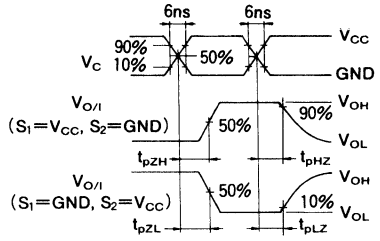
* 1: Input COMMON Terminal, and measured at SWITCH Terminal.
* 2: Input SWITCH Terminal, and measured at COMMON Terminal.

NOTE:These characteristics are determined by design of devices.

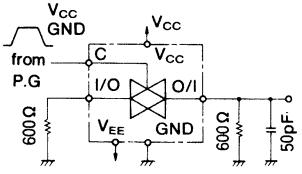
SWITCHING CHARACTERISTICS TEST CIRCUITS

1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

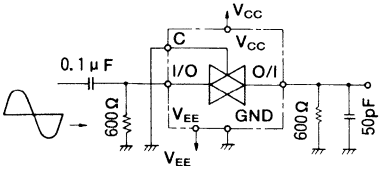




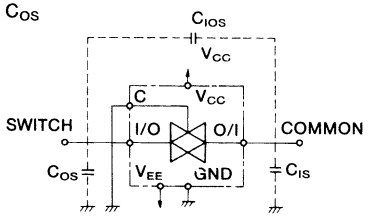
2. CROSS TALK (CONTROL INPUT-SWITCH OUTPUT)
fin=1MHz duty=50% tr=tf=6ns



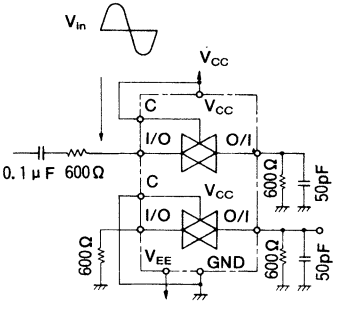
3. FEEDTHROUGH ATTENUATION



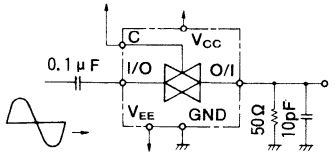
4. C_{IOS}, C_{IS}, C_{OS}



5. CROSSTALK (BETWEEN ANY TWO SWITCHES)



6. FREQUENCY RESPONSE (SWITCH ON)



TC74HC4060P/F

TC74HC4060P/F 14-STAGE BINARY COUNTER/DIVIDER WITH OSCILLATOR

The TC74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It operates ten times as fast as that of metal-gate C^2MOS IC (4060BP) with the same power dissipation.

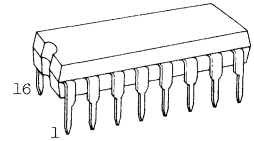
The oscillator configuration allows designs of either RC or crystal oscillator circuits. A clear input is used to reset the counter to the all low level state and disable the oscillator. A high level at CLEAR accomplishes the reset function.

A negative transition on the clock input incliments the counter. Ten kinds of devided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. And at the last stage, 1/16384 devided frequency is obtained.

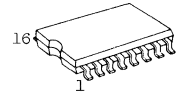
The $\overline{\phi}_I$ input and the CLEAR input are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed.....f_{max}=60MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.) (Ta=25°C)
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Oscillator Configulation .....RC or Crystal Oscillator
- Schmitt Trigger Clock Input
- Pin and Function Compatible with 4060B

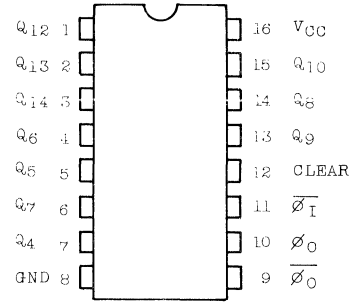


DIP16(3D16A-P)



MFP16(F16GC-P)

PIN ASSIGNMENT

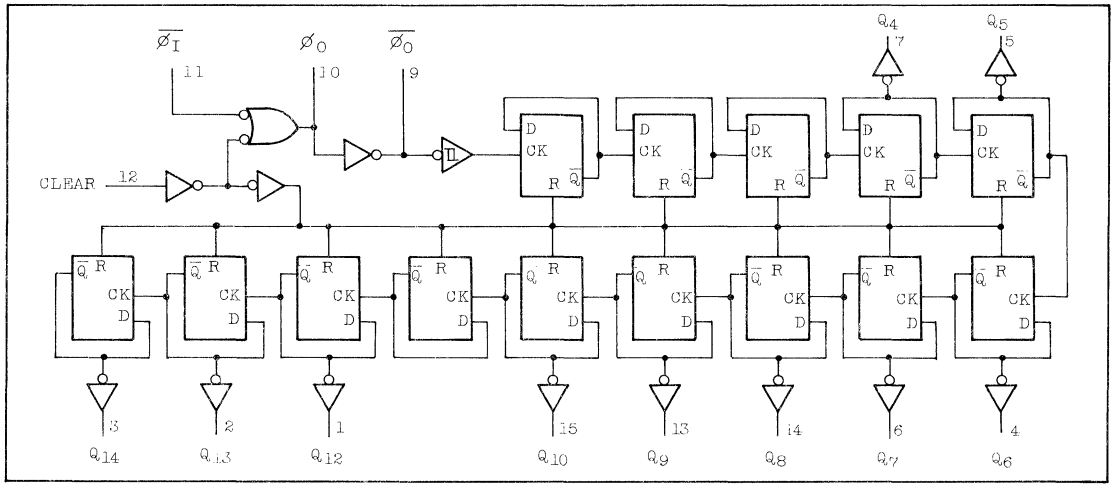


TRUTH TABLE

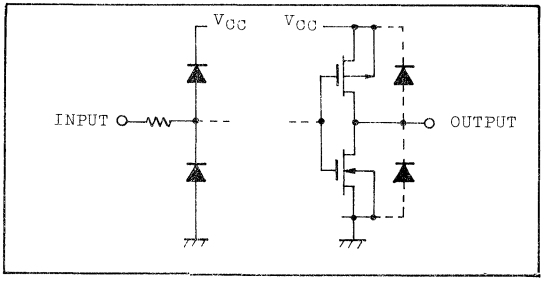
INPUTS		FUNCTION
$\overline{\phi_I}$	CLEAR	
x	H	Counter is reset to zero state. ϕ_O output goes to high level $\overline{\phi_O}$ output goes to low level
↓	L	Count up one step.
↑	L	No change.

x Don't care

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q Outputs)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.8	2.0	-	1.8	-	V
				4.5	4.0	4.5	-	4.0	-	
				6.0	5.5	5.9	-	5.5	-	
Low-Level Output Voltage (Q Outputs)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Low-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.2	-	0.2	V
				4.5	-	0.0	0.5	-	0.5	
				6.0	-	0.1	0.5	-	0.5	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

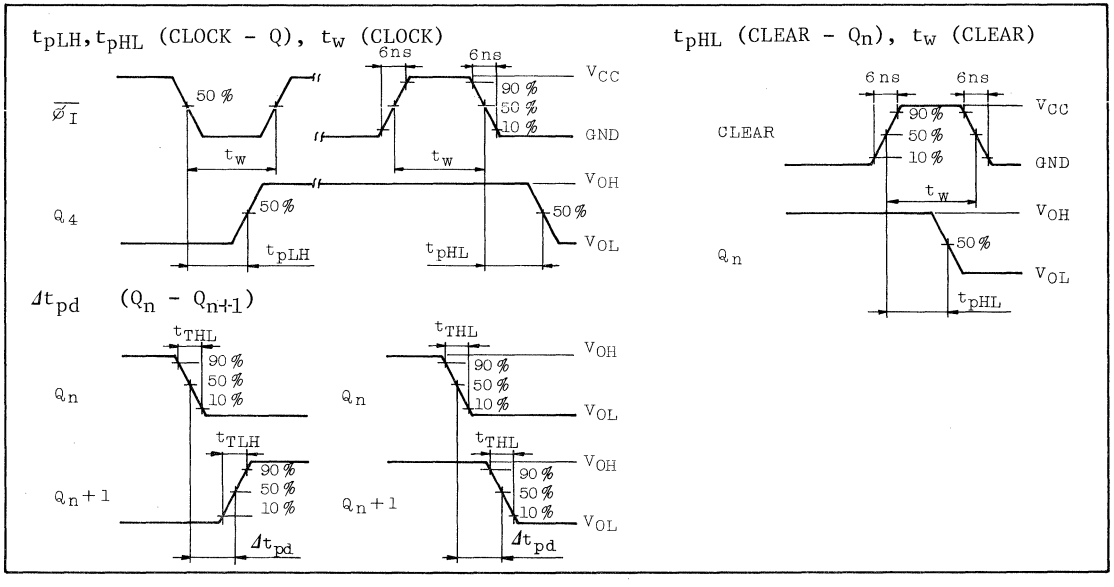
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q Outputs)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time $\overline{\phi}_I$ - Q_4	t_{pLH} t_{pHL}		2.0	-	196	370	-	465	
			4.5	-	49	74	-	93	
			6.0	-	42	63	-	79	
Propagation Delay Time Difference Q_n - Q_{n+1}	Δt_{pd}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time CLEAR - Q_n	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns) (CONTINUED)

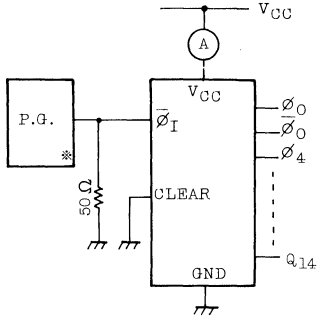
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width CLOCK ($\overline{\phi}_I$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
CLEAR	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time CLEAR	t_{rem}		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	33	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



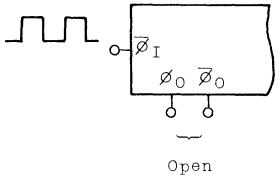
※ $\overline{\phi}_I$ input $t_r=t_f=6ns$ Duty=50%

Note

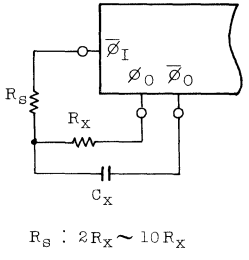
When CR or crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the measured value from the test circuit shown left, because these oscillion circuits spend much supply current.

TYPICAL CLOCK DRIVE CIRCUITS

EXTERNAL CLOCK DRIVE

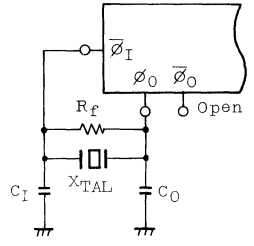


TYPICAL RC CIRCUIT



R_S : $2R_X \sim 10R_X$

TYPICAL CRYSTAL CIRCUIT



TC74HC4066P/F

TC74HC4066P/F QUAD BILATERAL SWITCH

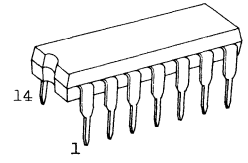
The TC74HC4066 is a high speed CMOS QUAD BILATERAL SWITCH fabricated with silicon gate C^2MOS technology.

It consists of four independent high speed switches capable of controlling either digital or analog signals with as low power dissipation as that of metal-gate C^2MOS IC.

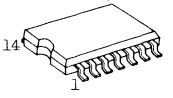
C input is provided to control the switch; the switch is ON while the C input is maintained at high level, and the switch is OFF while at low level.

FEATURES:

- High Speed.....t_{pd}=12ns(Typ.) (V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.) (Ta=25°C)
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Low ON Resistance.....R_{ON}=80Ω(Typ.) (V_{CC}=5V)
- High Degree of Liniarity.....DISTORTION=0.05%(Typ.) (V_{CC}=5V)
- Pin and Function Compatible with 4066B

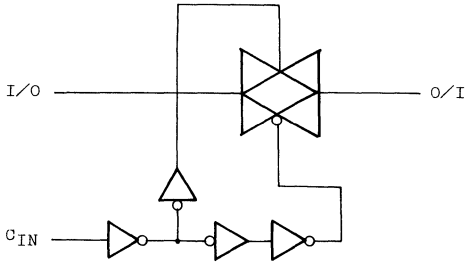


DIP14(3D14A-P)

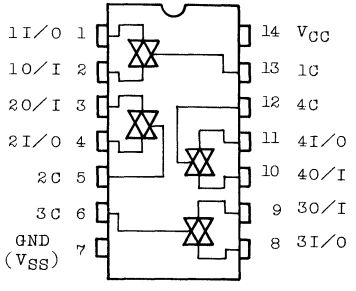


MFP14(F14GB-P)

LOGIC DIAGRAM (PER CHANNEL)



PIN ASSIGNMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

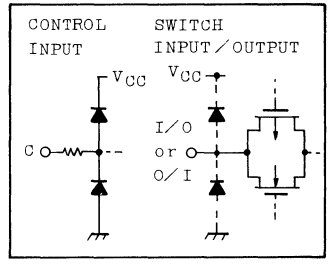
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Control Input Voltage	V_{IH}	Refer to R_{ON} specification	2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Control Input Voltage	V_{IL}	$\|I_{OFF}\| \leqq 1.0\mu A$	2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	
ON Resistance	R_{ON}	$V_C=V_{IHC}$ $V_{I/O}=0 \sim V_{CC}$ $I_{I/O}=100\mu A$	2.0	-	2000	-	-	-	Ω
			4.5	-	100	200	-	250	
			6.0	-	60	170	-	210	
Difference of ON Resistance Between Any Two of Four Switches	ΔR_{ON}	$V_C=V_{IHC}$ $I_{I/O}=100\mu A$	2.0	-	50	-	-	-	
			4.5	-	3	-	-	-	
			6.0	-	2	-	-	-	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Input/Output Leakage Current (Switch OFF)	I_{OFF}	$V_C=V_{ILC}$ $V_{I/O}=6V$, $V_{O/I}=0V$ or $V_{I/O}=0V$, $V_{O/I}=6V$	6.0	-	-	±0.1	-	±0.1	μA
Input Leakage Current	I_{IN}		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input tr=tf=6ns)

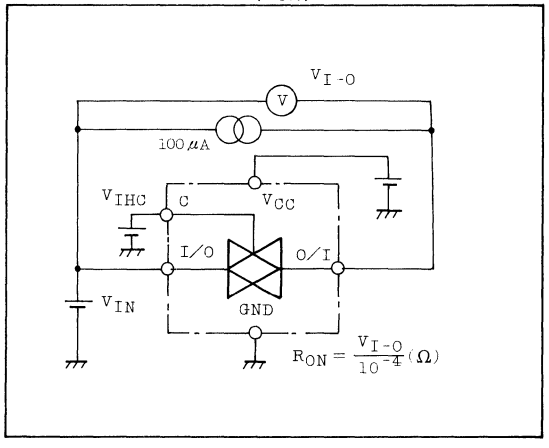
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Phase Difference between Input to Output	φ_{I-O}	R_L=10kΩ	2.0	-	13	50	-	65	ns
			4.5	-	5	10	-	13	
			6.0	-	4	9	-	11	
Output Enable Time	t_{pZH} t_{pZL}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	64	115	-	145	
			4.5	-	16	23	-	29	
			6.0	-	14	20	-	25	
Sine Wave Distortion		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=10kΩ f=1kHz	2.5	-	0.05	-	-	-	%
Frequency Response (Switch ON) $20\log_{10}\frac{V_{out}}{V_{in}}$=-3dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	30	-	-	-	MHz
Feedthrough Attenuation (Switch OFF) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	1.0	-	-	-	
Crosstalk (Control Input to Signal Output)		R_{IN}=1kΩ R_L=10kΩ	2.0	-	25	-	-	-	mV
			4.5	-	60	-	-	-	
			6.0	-	75	-	-	-	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns) (CONTINUED)

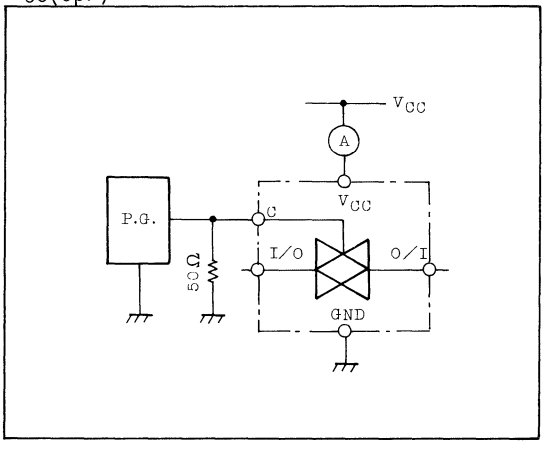
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Cross talk (Between any two switches) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V, V_{in}=0.88VRMS, R_L=1kΩ	2.5	-	1.5	-	-	-	MHz
Maximum Control Input Frequency		R_L=1kΩ, C_L=15pF, V_{OUT}=1/2 V_{CC}	2.0	-	20	-	-	-	MHz
			4.5	-	30	-	-	-	
			6.0	-	30	-	-	-	
Control Input Capacitance	C_{IN}			-	5	10	-	10	pF
Switch Input/Output Capacitance	$C_{I/O}$			-	6	-	-	-	pF
Feedthrough Capacitance	C_{I-O}			-	0.5	-	-	-	pF
Power Dissipation Capacitance	C_{PD}(1)			-	13	-	-	-	pF

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per CHANNEL)

CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT

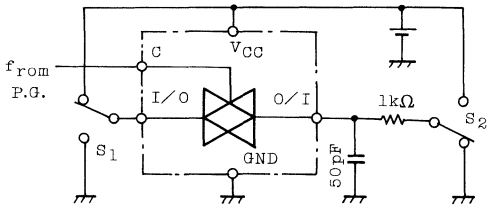


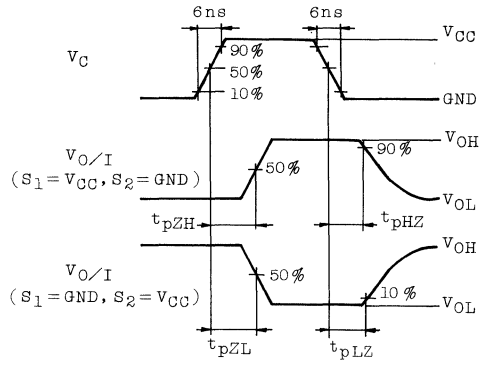
$I_{CC(opr)}$ TEST CIRCUIT



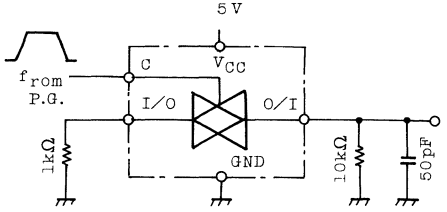
SWITCHING CHARACTERISTICS TEST CIRCUIT

1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

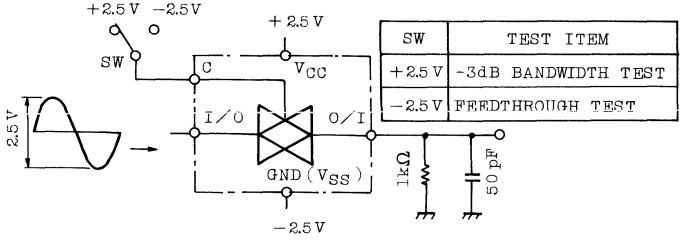




2. CROSSTALK (CONTROL TO OUTPUT)

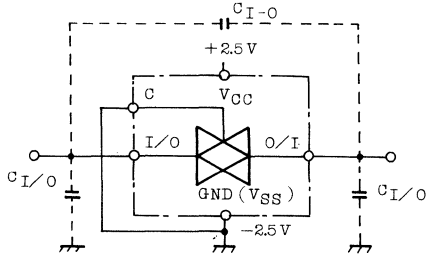


3. BANDWIDTH AND FEEDTHROUGH ATTENUATION

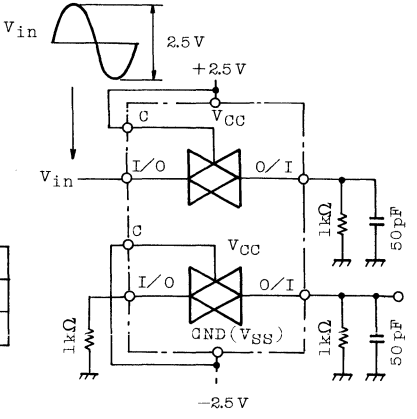


SW	TEST ITEM
+2.5 V	-3dB BANDWIDTH TEST
−2.5 V	FEEDTHROUGH TEST

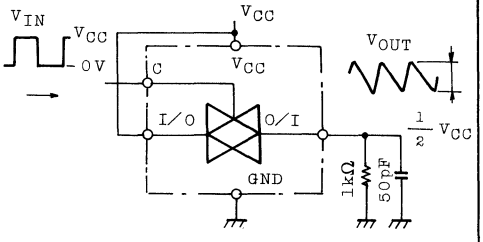
4. C_{I-O}, $C_{I/O}$



5. CROSSTALK BETWEEN ANY TWO SWITCHES



6. MAXIMUM CONTROL FREQUENCY



TC74HC4072P/F

TC74HC4072P/F DUAL 4-INPUT OR GATE

The TC74HC4072 is a high speed CMOS 4-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

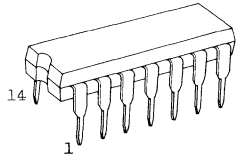
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output.

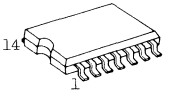
All inputs are equipped with protection circuits against static discharge or excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance...$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range...V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 4072B

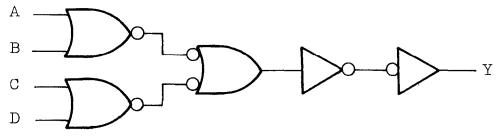


DIP14(3D14A-P)

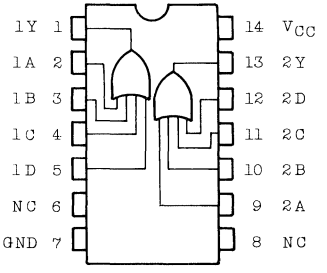


MFP14(F14GB-P)

LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)



PIN ASSIGNMENT



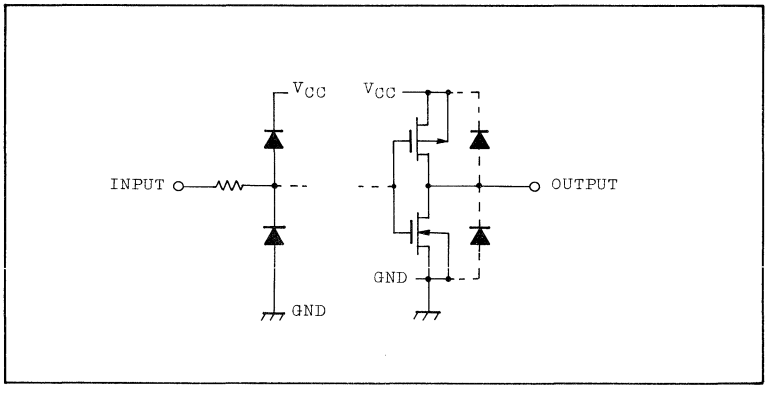
(Top View)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40 ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

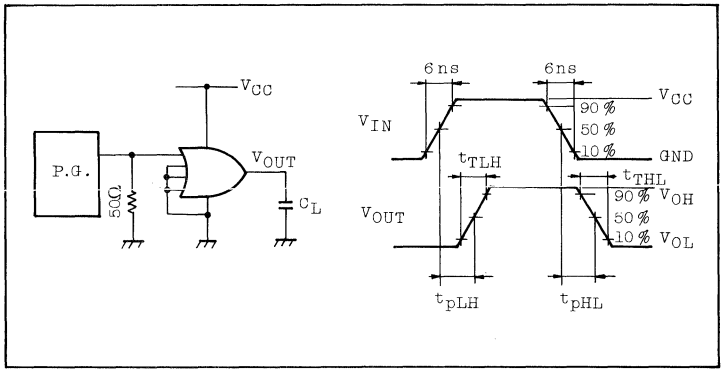
PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

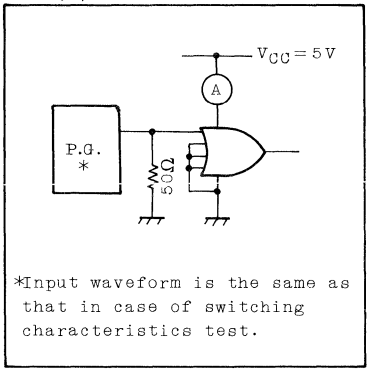
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT and WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



*Input waveform is the same as that in case of switching characteristics test.

TC74HC4075AP/AF

TRIPLE 3-INPUT OR GATE

The TC74HC4075A is a high speed CMOS 3-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

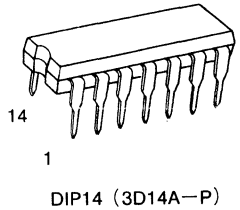
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including a buffer output, which provide high noise immunity and stable output.

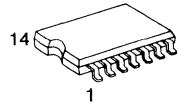
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =8ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4075B

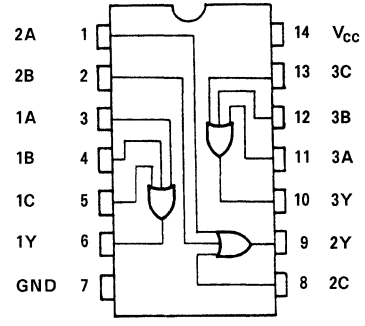


DIP14 (3D14A-P)

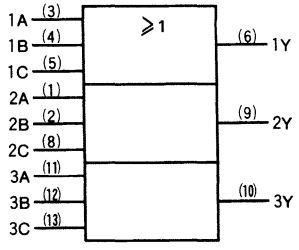


MFP14 (F14GB-P)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	2.0	−	20.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	35	90	–	115	
			4.5	–	11	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	27	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{(per Gate)}$$

TC74HC4078P/F

TC74HC4078P/F 8-INPUT NOR GATE

The TC74HC4078 is a high speed CMOS 8-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

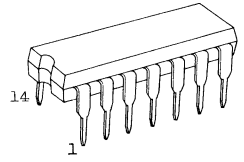
It operates ten times as fast as that of metal-gate C^2MOS IC (4078B) with the same power dissipation.

Output X is 8-INPUT NOR, output Y is 8-INPUT OR. Both outputs are buffered, which enables high noise immunity and stable output.

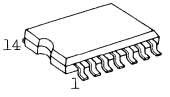
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4078B



DIP14(3D14A-P)



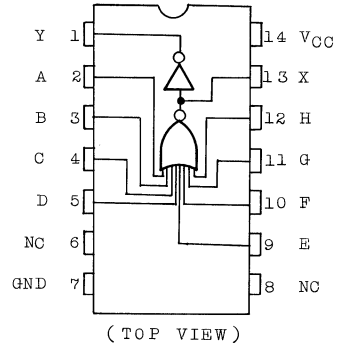
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

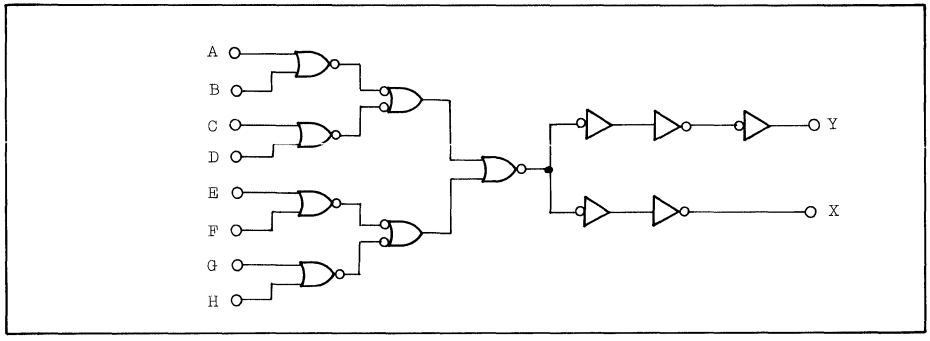
PIN ASSIGNMENT



(TOP VIEW)

NC:No Connection

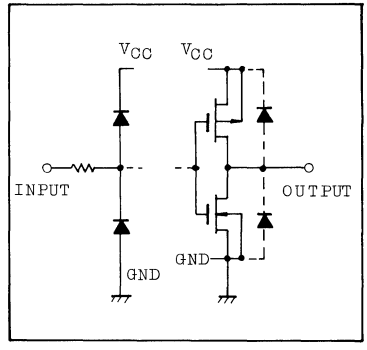
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=−40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

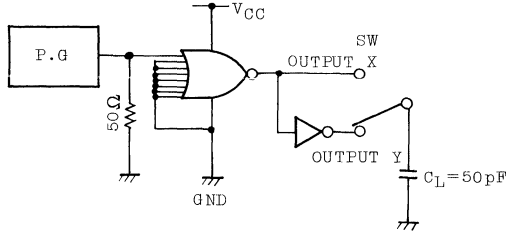
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	68	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	73	-	-	-	

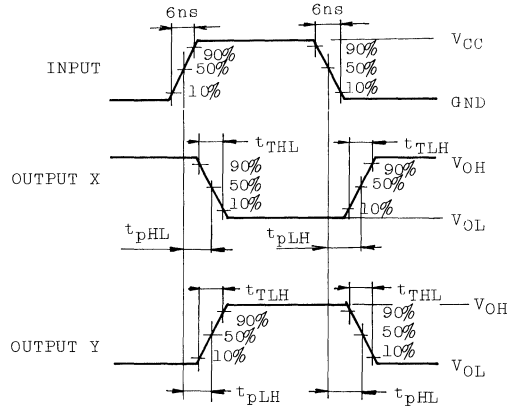
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

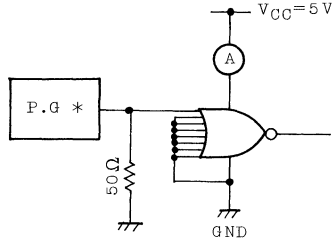
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT





I_{CC}(Opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

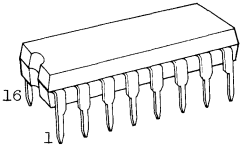
TC74HC4094P/F

TC74HC4094P/F 8-BIT SHIFT AND STORE REGISTER (3-STATE)

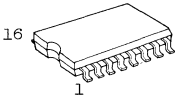
The TC74HC4094 is a high speed CMOS 8-STAGE SHIFT-AND-STORE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device consists of an 8-bit shift register and a 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices. Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided to a latch, which latches data on the negative going transition of the STROBE input signal. When STROBE input is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=42MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Oerating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 4094B



DIP16(3D16A-P)



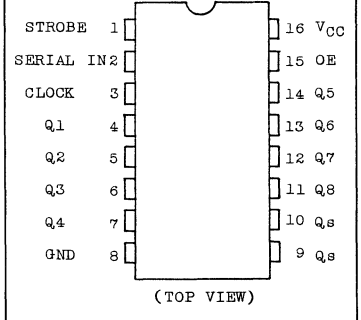
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

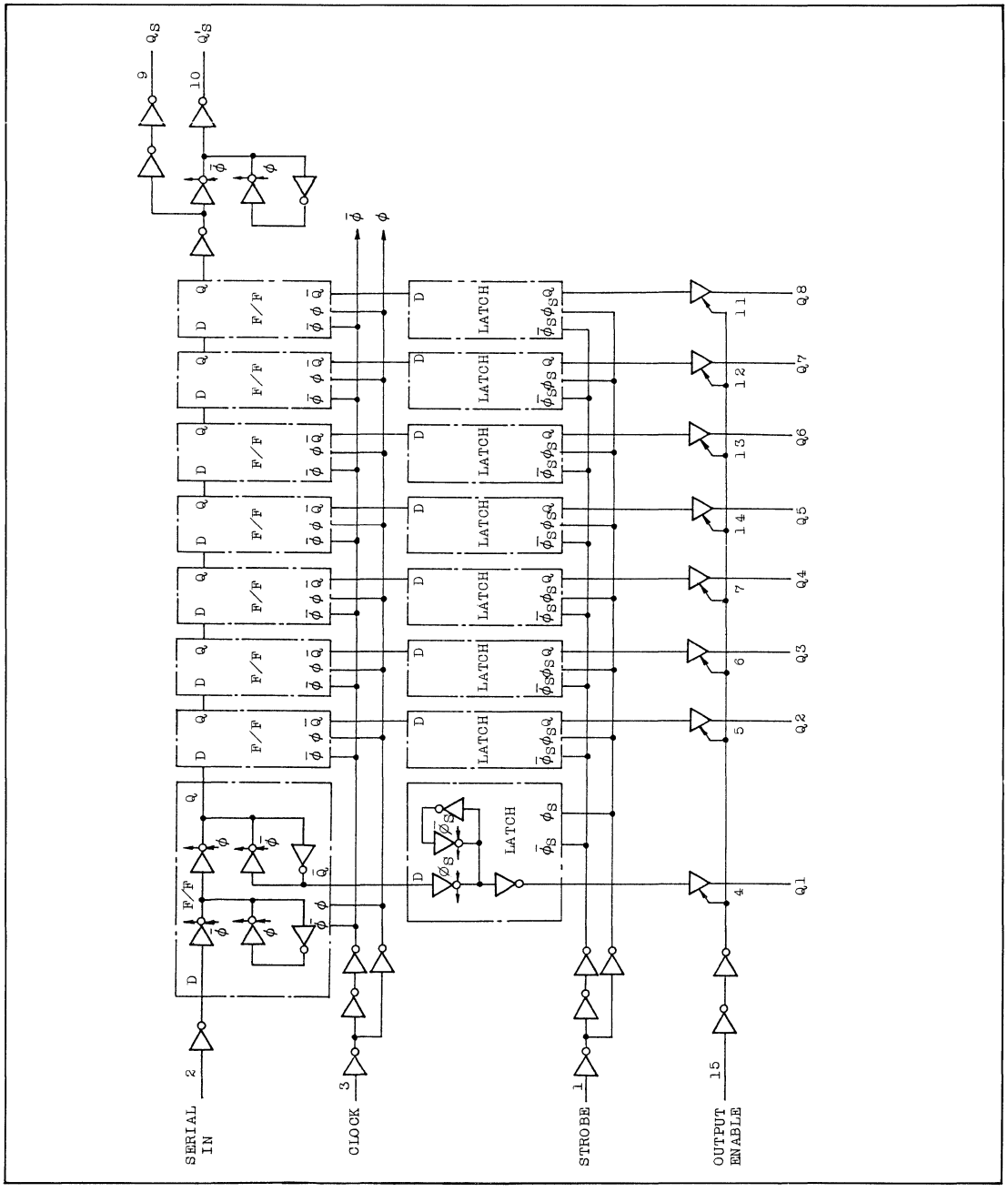
* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

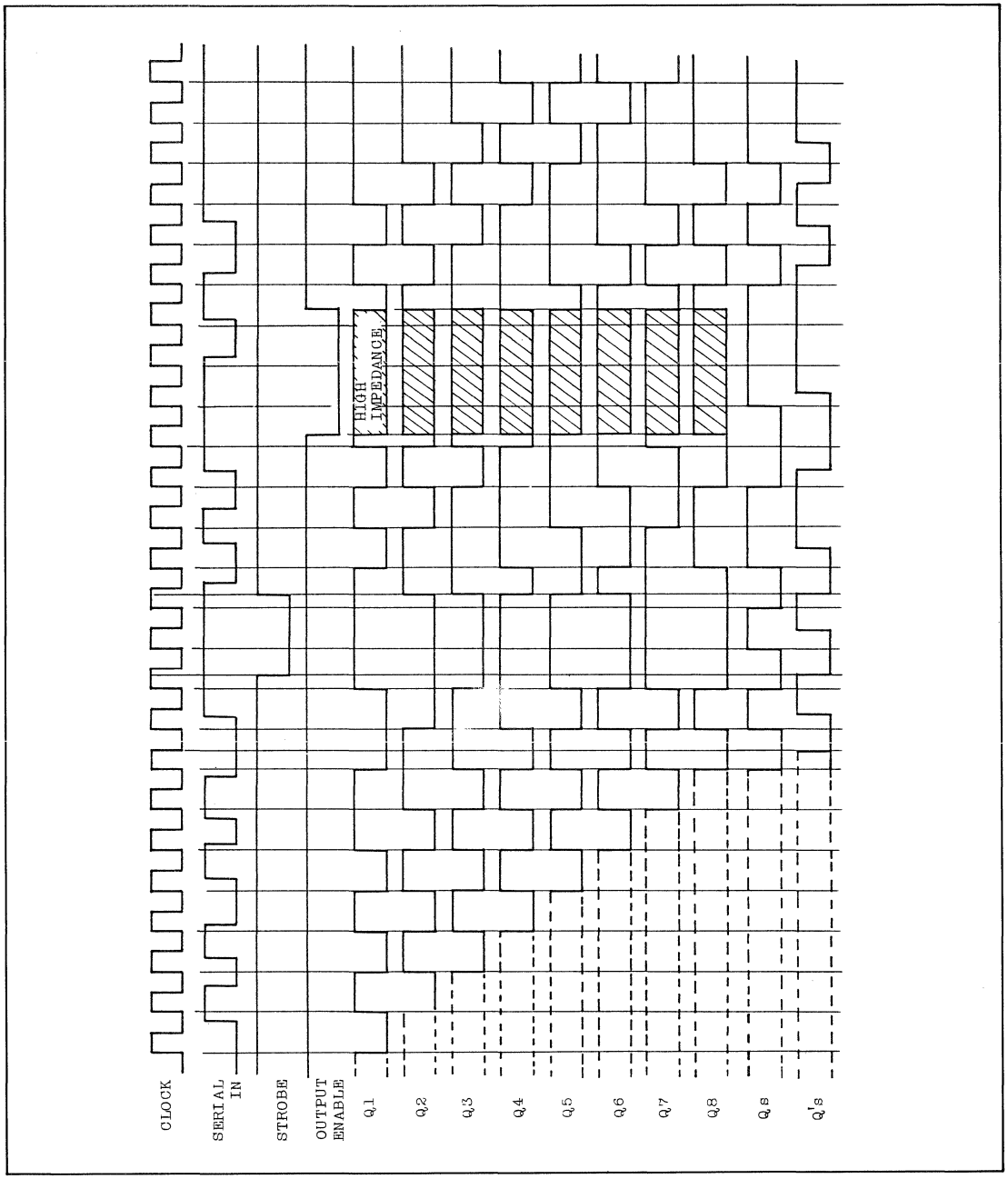


(TOP VIEW)

LOGIC DIAGRAM



TIMING CHART



TRUTH TABLE

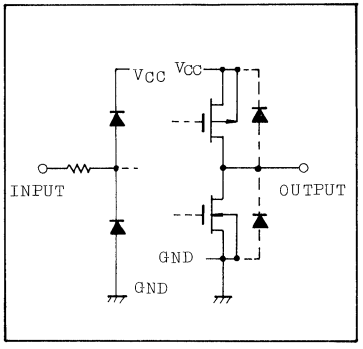
CK	OE	ST	SI	PARA.OUT		SERI.OUT	
				Q_1	Q_n	Q_s	Q'_s
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	L	X	X	Z	Z	NC	Qs

X : DON'T CARE
NC: NO CHANGE
Z : HIGH IMPEDANCE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Cutput Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	TYP.	MAX.	-40 ~ 85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn)	t_{PLH}		2.0	-	140	270	-	340	
			4.5	-	35	54	-	68	
	t_{PHL}		6.0	-	30	46	-	58	
Propagation Delay Time (CLOCK - Qs, Qs')	t_{PLH}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
	t_{PHL}		6.0	-	22	34	-	43	
Propagation Delay Time (STROBE - Qn)	t_{PLH}		2.0	-	135	210	-	265	
			4.5	-	27	42	-	53	
	t_{PHL}		6.0	-	23	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	4	10	-	3	-	MHz
			4.5	20	38	-	16	-	
			6.0	24	45	-	19	-	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	ns
			4.5	-	9	20	-	25	
	$t_{w(L)}$		6.0	-	8	17	-	21	
Minimum Strobe Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	

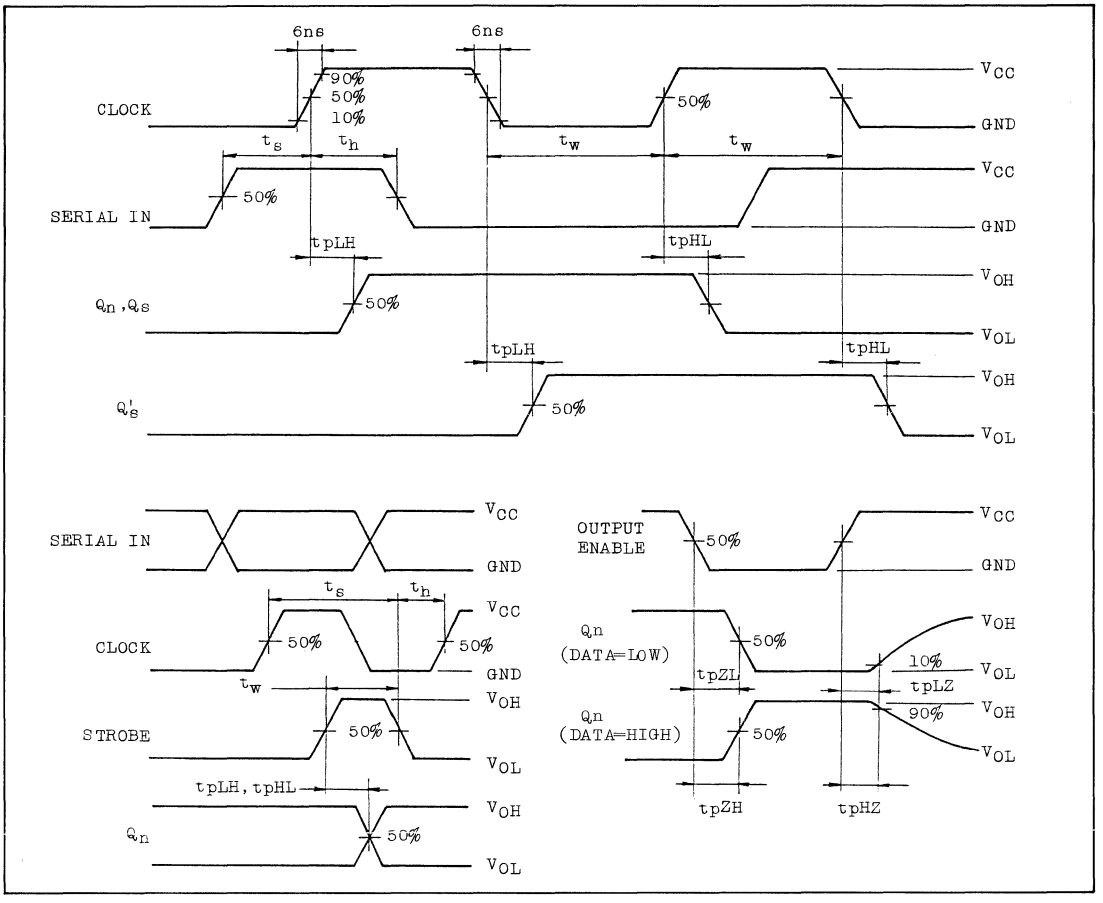
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Serial In Set-up Time	t_s		2.0	-	25	75	-	95	ns
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Strobe Set-up Time	t_s		2.0	-	50	150	-	190	
			4.5	-	13	30	-	38	
			6.0	-	11	26	-	33	
Minimum Serial In Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Strobe Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD} (1)			-	167	-	-	-	

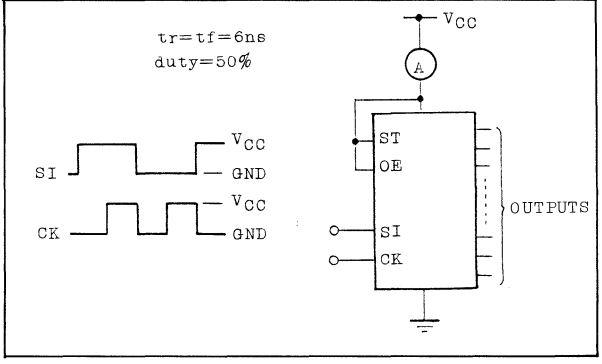
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

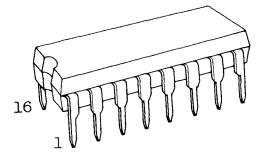
At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC40102P DUAL BCD PROGRAMMABLE DOWN COUNTER
TC74HC40103P 8-BIT BINARY PROGRAMMABLE DOWN COUNTER

The TC74HC40102 and TC74HC40103 are high speed CMOS PROGRAMMABLE DOWN COUNTER fabricated with silicon gate C^2MOS technology.
They operate ten times as fast as that of metal-gate C^2MOS IC (40102/40103B) with the same power dissipation. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero. As the TC74HC40102 adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The 74HC40103 with 8-bits binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{CLR}$ control input setting counter to maximum counting mode.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range .....V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 40102B, 40103B



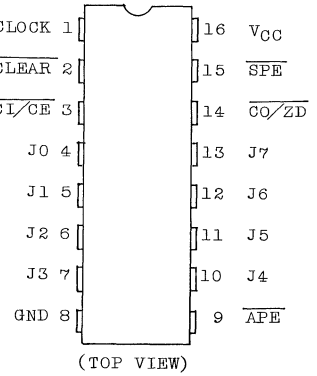
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

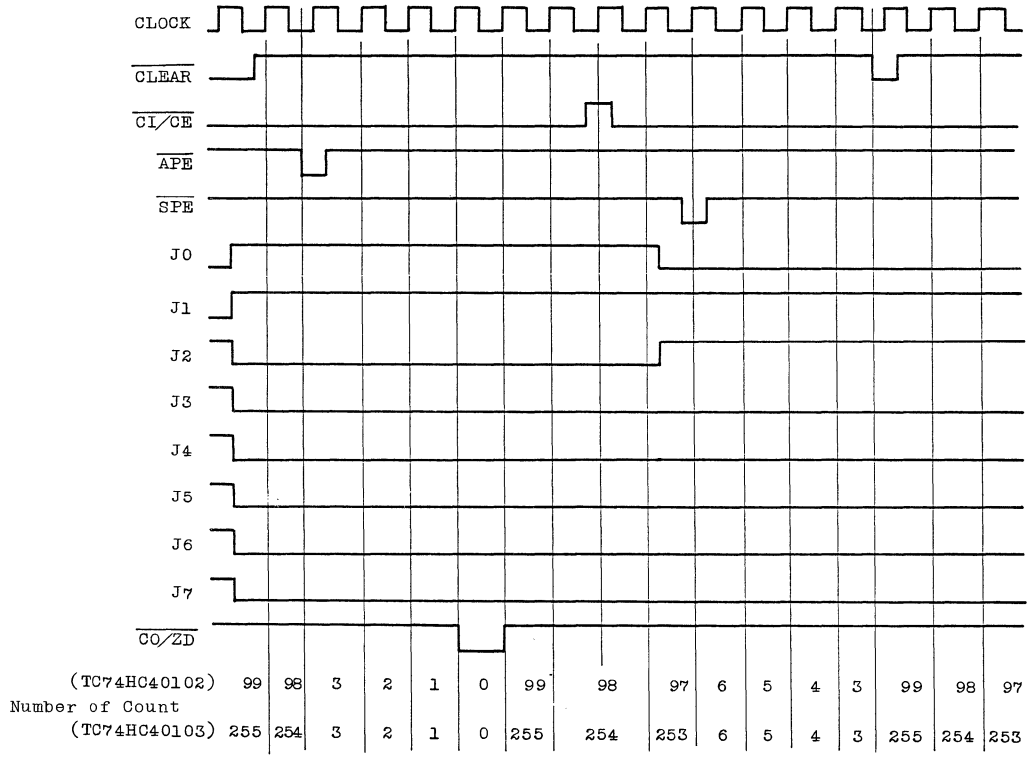
TRUTH TABLE

CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	X	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	X	X	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	X	X	X	Clear	Counter is set to maximum count.

Note 1. X: Don't care

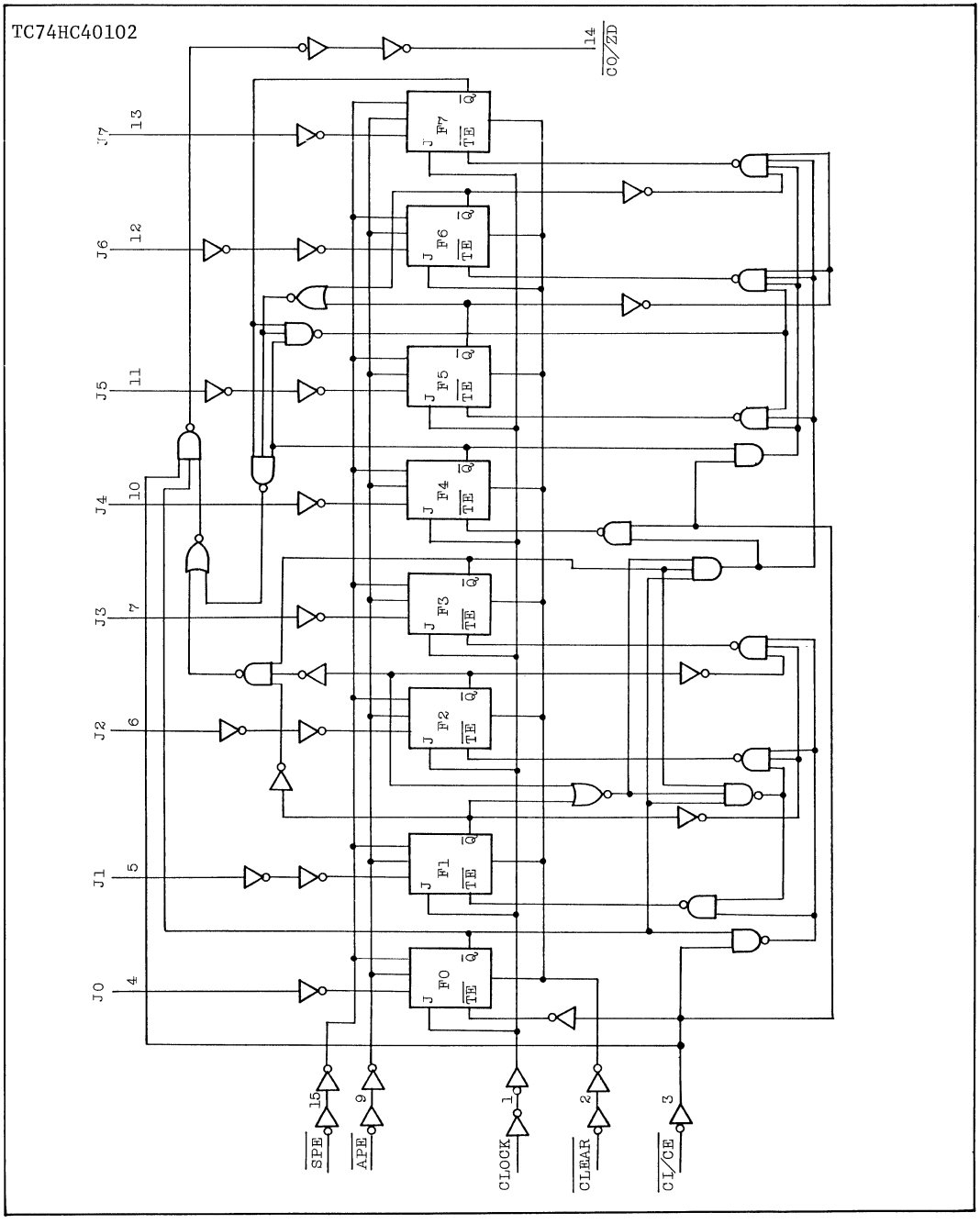
2. Maximum count: "99" for TC74HC40102 and "255" for TC74HC40103.

TIMING CHART



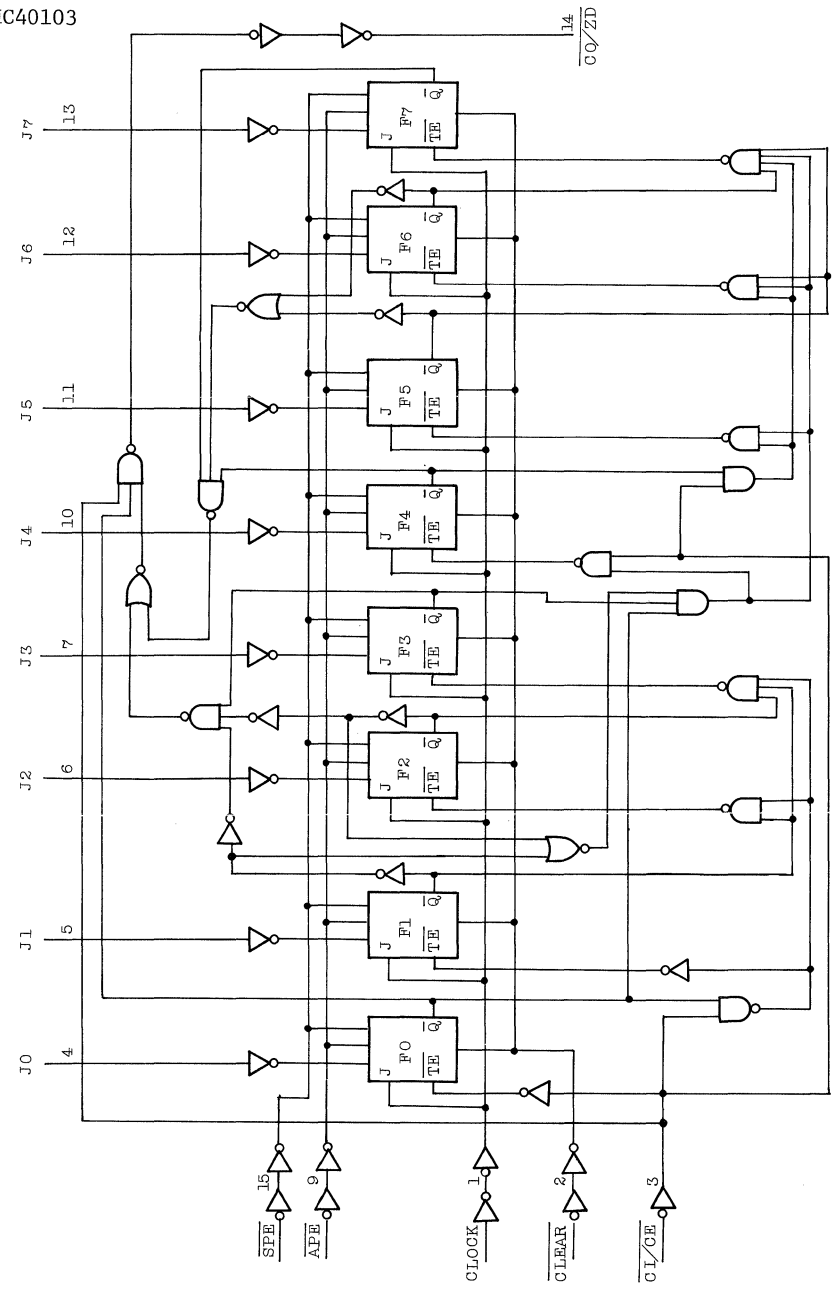
LOGIC DIAGRAM

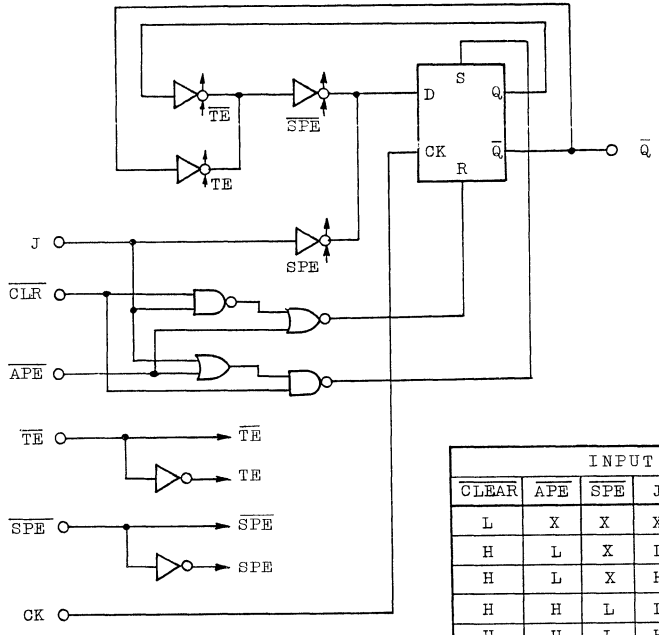
TC74HC40102



LOGIC DIAGRAM

TC74HC40103





INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q_n}+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↓	L
H	H	L	H	X	↓	H
H	H	L	X	X	↑	$\overline{Q_n}$
H	H	H	X	L	↓	Q_n
H	H	H	X	H	X	$\overline{Q_n}$

FUNCTIONAL DESCRIPTION

The TC74HC40102 and TC74HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103 adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level.

(Continued)

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102 and 255 for the TC74HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102 and TC74HC40103, respectively, when clock input alone is given without various kinds of preset operations.

PRESET OPERATION AND RESET OPERATION

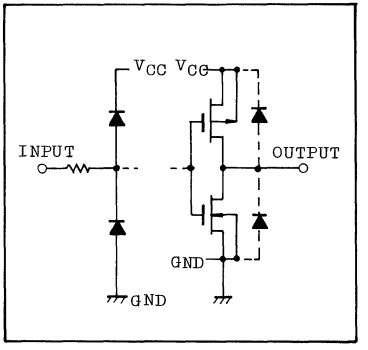
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	128	245	-	305	
	t_{pHL}		4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	156	300	-	375	
	t_{pHL}		4.5	-	39	60	-	75	
			6.0	-	33	51	-	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

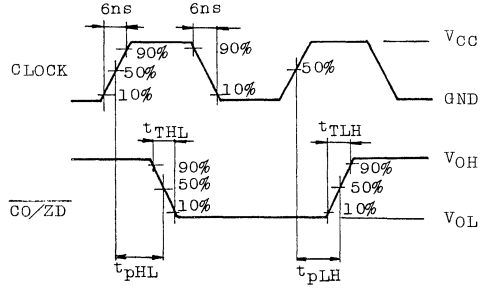
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CLEAR}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	124	240	-	300	ns
			4.5	-	31	48	-	60	
			6.0	-	27	41	-	51	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	31	-	16	-	
			6.0	24	36	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$, $\overline{APE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$, $\overline{APE}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set up Time ($\overline{SPE}$ - CK)	t_s		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Set up Time ($\overline{CI/CE}$ - CK)	t_s		2.0	-	56	125	-	160	
			4.5	-	14	25	-	32	
			6.0	-	12	21	-	27	
Minimum Set up Time (Jn - CK)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set up Time (Jn - $\overline{APE}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (All Inputs)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	74HC40102		-	110	-	-	-	
		74HC40103		-	128	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

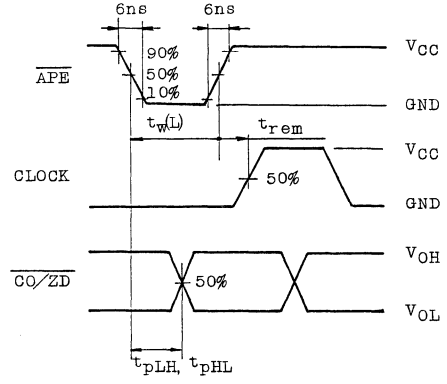
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

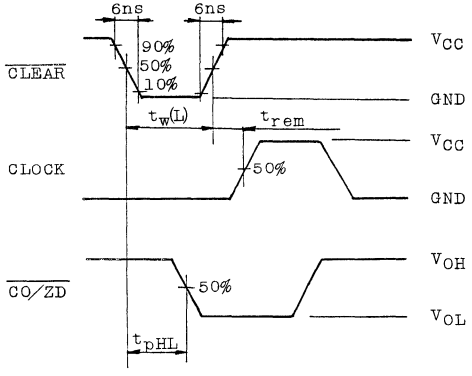
WAVEFORM 1



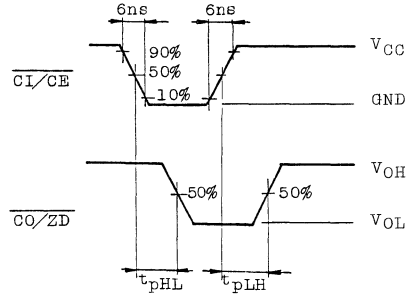
WAVEFORM 2



WAVEFORM 3

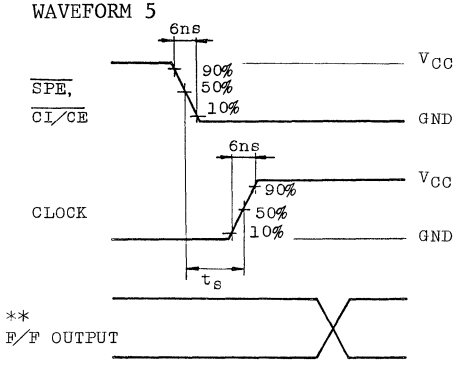


WAVEFORM 4

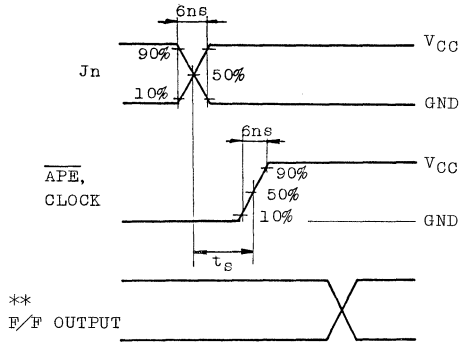


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

WAVEFORM 5

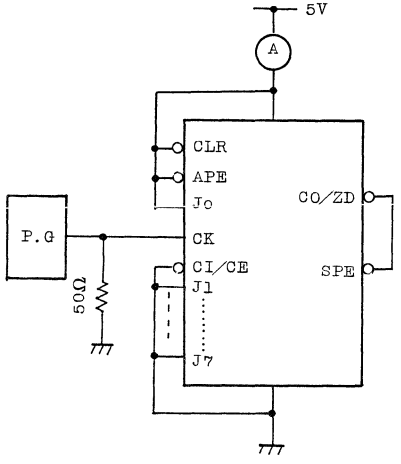


WAVEFORM 6



(** F/F output is internal signal of IC)

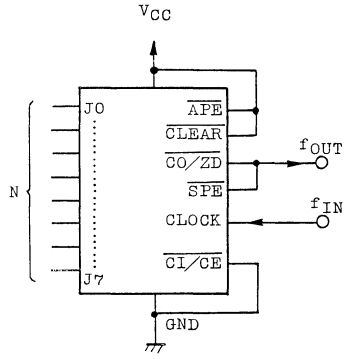
I_{CC}(Opr.) TEST CIRCUIT



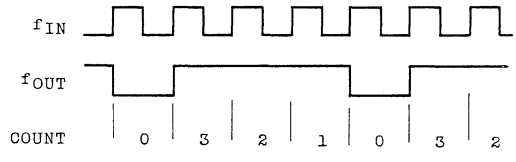
Input transition time is the same as that in case of switching characteristics test.

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

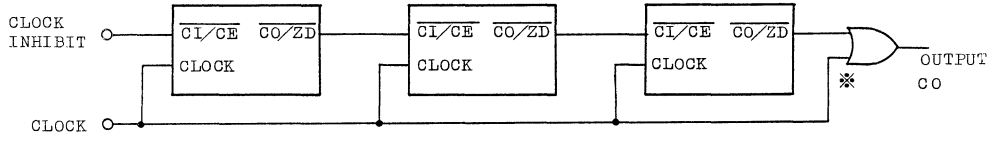


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (J0, J1=V_{CC}, J2 ∿ J7=GND)



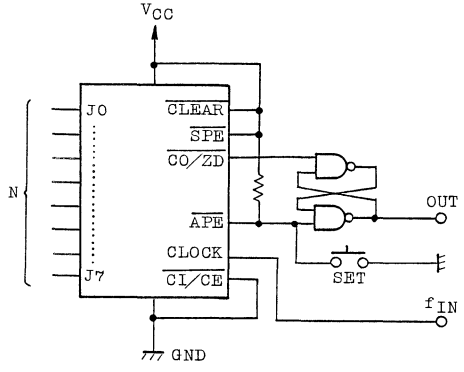
- TC74HC40102P .... 1/2 to 1/100 are dividable.
- TC74HC40103P .... 1/2 to 1/256 are dividable.

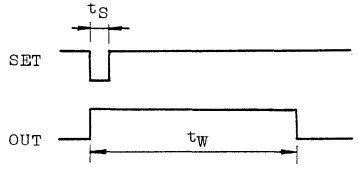
PARALLEL CARRY CASCADING



※ At synchronous cascade connection, huzzerd occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC74HC32 or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ∿ the above formula.

TC74HC40105AP/AF

FIFO 4 Bit × 16 Word REGISTER

The TC74HC40105A is a high speed CMOS 4bit x 16word first-in, first-out (FIFO) Strage Register fabricated with silicon gate C^2MOS technolgy.

It achieves the high speed operation while maintaining the CMOS low power dissipation.

The device is capable of handling 16 four-bit words and it is possible to handle the input and output data at different shifting rates.

When the DATA-IN-READY (DIR) is high, data is written into the registers by a low to high transition of the SHIFT IN (SI) input. And when DATA-OUT-READY (DOR) is high, data is read out of the registers by a high to low transition of the $\overline{\text{SHIFT OUT}}$ ($\overline{\text{SO}}$) input.

If the MASTER RESET (MR) is high, the DIR goes high and DOR goes low. The data in the internal registers are not changed but are declared invalid.

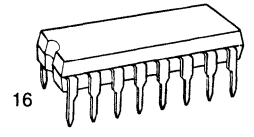
The TC74HC40105A can be cascaded to form longer registers or wider words.

The DATA OUTPUTs (Qn) are 3-State Outputs. When $\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$) is held high, the Qn's are in high impedance state.

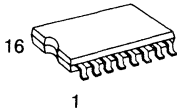
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=25MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· 4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Load
  - 10(For DIR, DOR)
  - 15(For $Q_0 \sim Q_3$)
- Symmetrical Output Impedance ···
  - $|I_{OH}|=I_{OL}$=4mA(Min.)(For DIR, DOR)
  - $|I_{OH}|=I_{OL}$=6mA(Min.)(For $Q_0 \sim Q_3$)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V

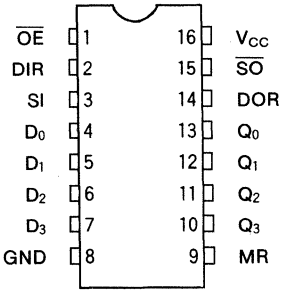


DIP16 (3D16A-P)

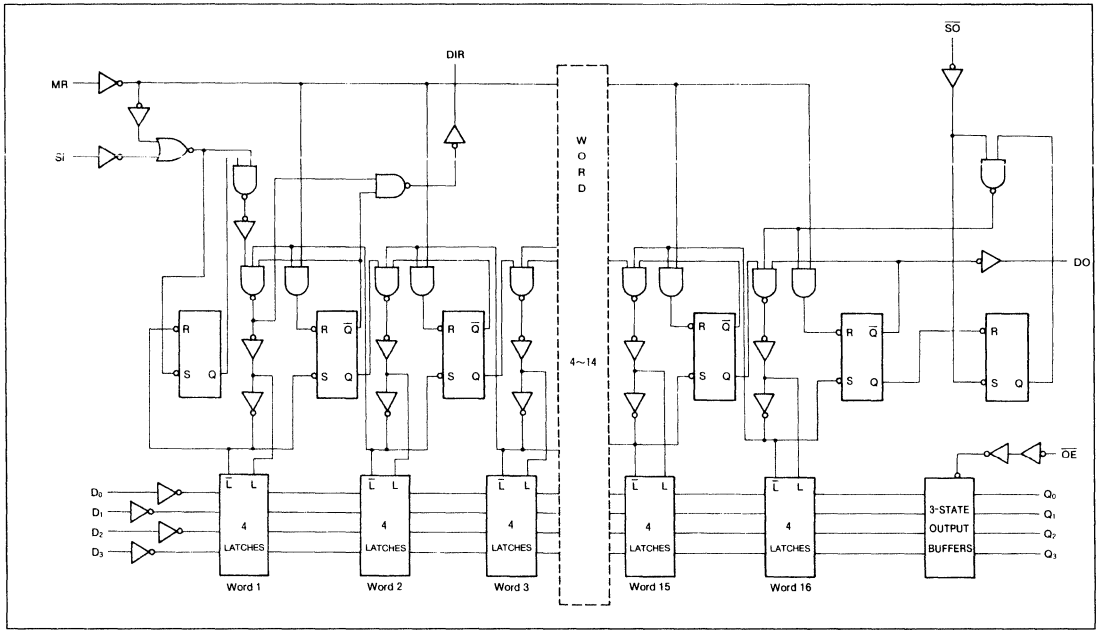


MFP16 (F16GC-P)

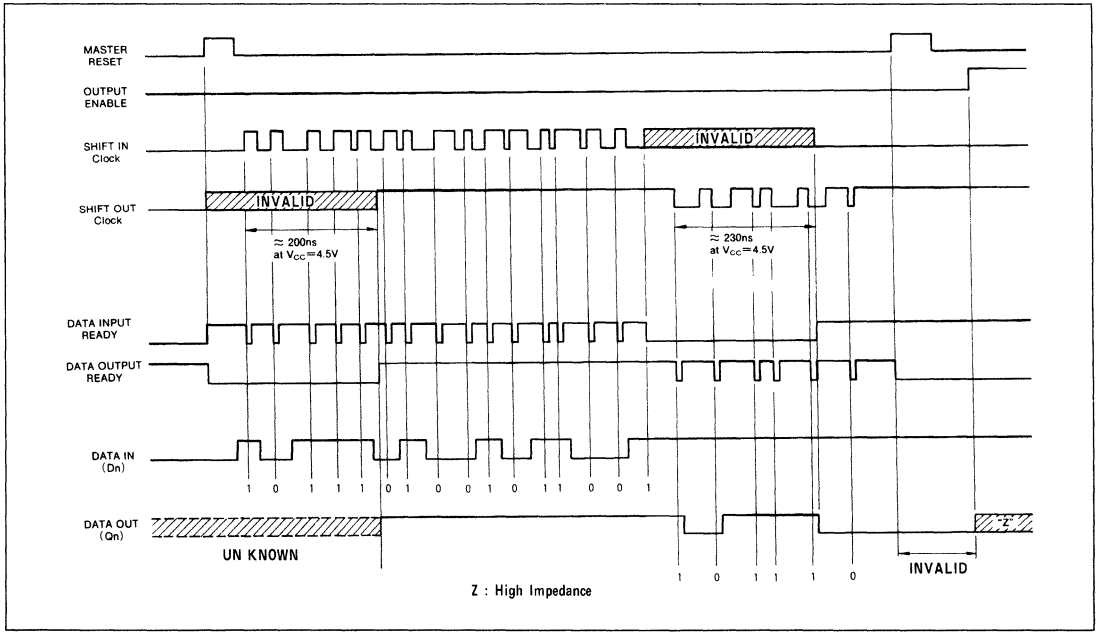
PIN ASSIGNMENT



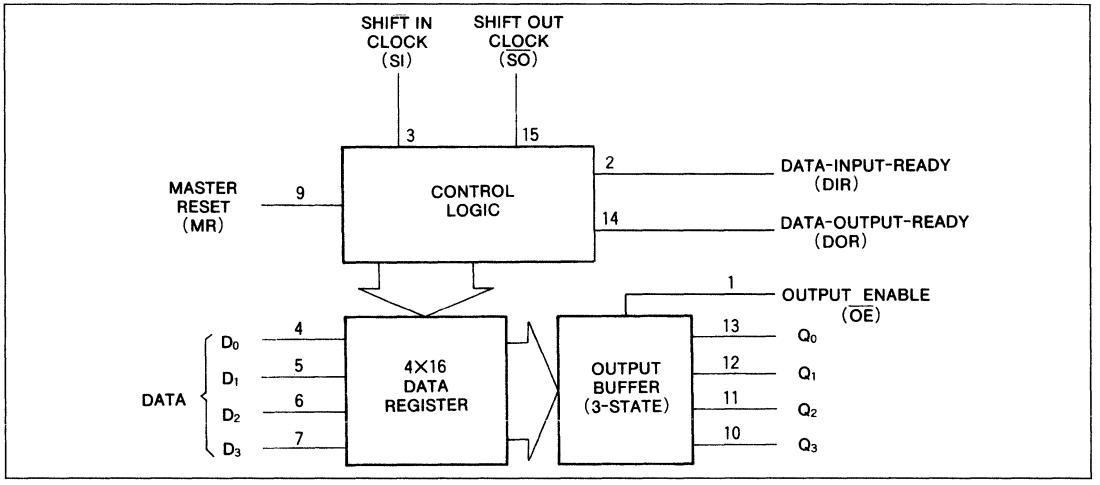
SYSTEM DIAGRAM



TIMING DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1) **WRITING DATA**

Data can be written into the FIFO whenever DIR is high and a low to high transition occurs on the SI pin. DIR will toggle momentarily until the data has been transferred to the second word register.

SI must be toggled before the next 4-bit word can be written. The first and subsequent words will automatically ripple to the output end of the device even if there is not a full 16 words of input data. When all 16 words are filled with data, DIR will go low and additional data cannot be written into the device.

2) **READING DATA**

When a data word appears in the sixteenth data register (just before the output buffer), DOR goes high and, if $\overline{OE}$ is low, data can be output on the high to low transition of $\overline{SO}$.

The data remaining in the registers now ripples to the next higher word position opening the first word position for new data. DIR goes high and additional data can be written in. During the output of data, DOR toggles momentarily after each read. When the data registers become empty, DOR goes low and $\overline{SO}$ is ignored.

3) **MASTER REST**

When a high is input to MR, the internal control logic is initiallized. This causes DIR to go high and DOR to go low. The contents of the data registers are not changed, but are invalid and will be written over when the first word is loaded.

4) **CASCADING**

The TC74HC40105A can be cascaded to form longer registers simply by connecting DOR of the first device to SI of the second and DIR of the second device to $\overline{SO}$ of the first. Additional devices may be cascaded by repeating the above. Of course, the Qn outputs of the first device must be connected to the Dn inputs of the second.

In this mode, an MR pulse must be applied after the supply voltage is turned on. For words wider than 4-bits, the DIR and DOR outputs from each FIFO must be ANDed respectively and the SI and $\overline{SO}$ inputs must each be paralleled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (DIR, DOR) (Q_0 ~ Q_3)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		DIR, DOR	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_0 ~ Q_3	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		DIR, DOR	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_0 ~ Q_3	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (SI)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SO}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (MR)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (DATA−SI)	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (DATA−SI)	t_h		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Removal Time (MR−SI)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	3	24	MHz
			4.5	−	15	12	
			6.0	−	18	13	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (DIR,DOR)	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (SO,MR−DOR)	t_{pHL}		−	16	30	
Propagation Delay Time (SO DIR)	t_{pLH}		−	242	365	
Propagation Delay Time (SI,DOR)	t_{pLH}		−	181	273	
Propagation Delay Time (SI−DIR)	t_{pHL}		−	22	35	
Propagation Delay Time (MR−DIR)	t_{pLH} t_{pHL}		−	25	39	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Output Transition Time (Q_0～Q_3)	t_{TLH} t_{THL}		50	2.0	−	21	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (DIR,DOR)	t_{TLH} t_{THL}		50	2.0	−	24	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (SO,MR−DOR)	t_{pHL}		50	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Propagation Delay Time (SO−DIR)	t_{pLH}		50	2.0	−	798	2000	−	2500	
				4.5	−	266	400	−	500	
				6.0	−	226	340	−	425	
Propagation Delay Time (SI−DOR)	t_{pLH}		50	2.0	−	597	1500	−	1875	
				4.5	−	199	300	−	375	
				6.0	−	169	255	−	319	
Propagation Delay Time (SI−DIR)	t_{pHL}		50	2.0	−	78	200	−	250	
				4.5	−	26	40	−	50	
				6.0	−	22	34	−	43	
Propagation Delay Time (SO−Qn)	t_{pLH} t_{pHL}		50	2.0	−	156	400		500	
				4.5	−	52	80		100	
				6.0	−	44	68		85	
			150	2.0	−	171	440		550	
				4.5	−	57	88		110	
				6.0	−	48	75	−	94	
Propagation Delay Time (SI−Qn)	t_{pLH} t_{pHL}		50	2.0	−	612	1500	−	1875	
				4.5	−	204	300	−	375	
				6.0	−	173	255	−	319	
			150	2.0	−	627	1540	−	1925	
				4.5	−	209	308	−	385	
				6.0	−	178	262	−	327	
Propagation Delay Time (MR−DIR)	t_{pLH} t_{pHL}		50	2.0	−	87	225	−	280	
				4.5	−	29	45	−	56	
				6.0	−	25	38	−	48	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1\,k\Omega$	50	2.0	−	45	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	13	21	−	26	
			150	2.0	−	60	165	−	205	
				4.5	−	20	33	−	41	
				6.0	−	17	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	32	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	3	7	−	2.4	−	MHz
				4.5	15	22	−	12	−	
				6.0	18	26	−	14	−	
			150	2.0	2.6	6	−	2	−	
				4.5	13	20	−	10	−	
				6.0	15	24	−	12	−	
Output Pulse Width (DIR)	$t_{W(H)}$ $t_{W(L)}$		50	2.0	−	95	−	−	−	ns
				4.5	−	25	−	−	−	
				6.0	−	21	−	−	−	
Output Pulse Width (DOR)	$t_{W(H)}$ $t_{W(L)}$		50	2.0	−	95	−	−	−	
				4.5	−	25	−	−	−	
				6.0	−	21	−	−	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	300	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TC74HC4511P/F BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

The TC74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fablicated with silicon gate C^{2}MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

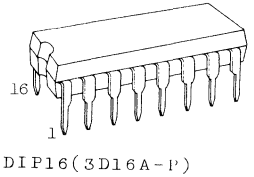
The segment output driver, which is CMOS construction, has large I_{OH} capability which enables to drive cathode common LED directly.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L". These functions are regardless of other inputs and used to test display.

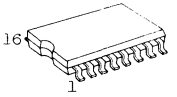
BI input is used to pulse-modulate the brightness of the display.

When error input code (over 10) is applied to BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

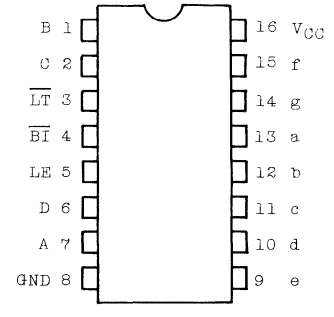


MFP16(F16GC-P)

FEATURES:

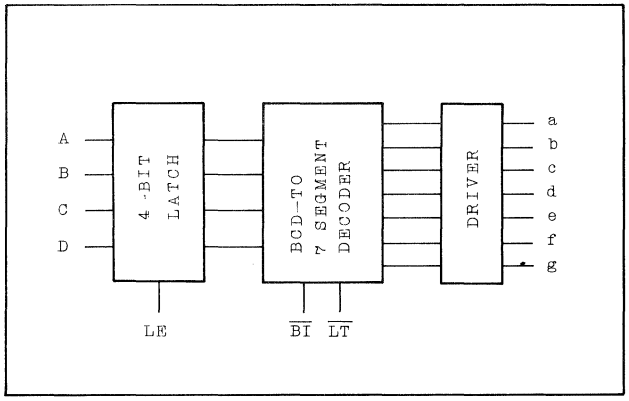
- High Speed.....t_w=15ns(Max.) at V_{CC}=4.5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTTL Loads
- High Output Current.....|I_{OH}|=20mA
- Wide Operating Voltage Range.$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with standard CMOS 4511B.

PIN ASSIGNMENT

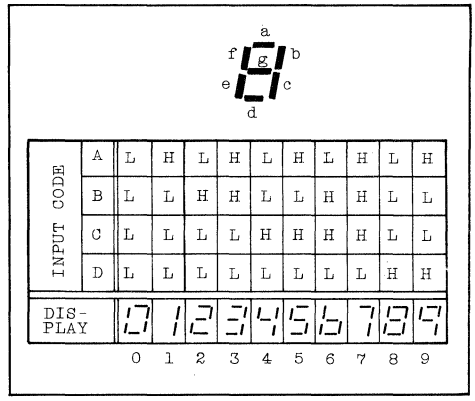


(Top View)

BLOCK DIAGRAM

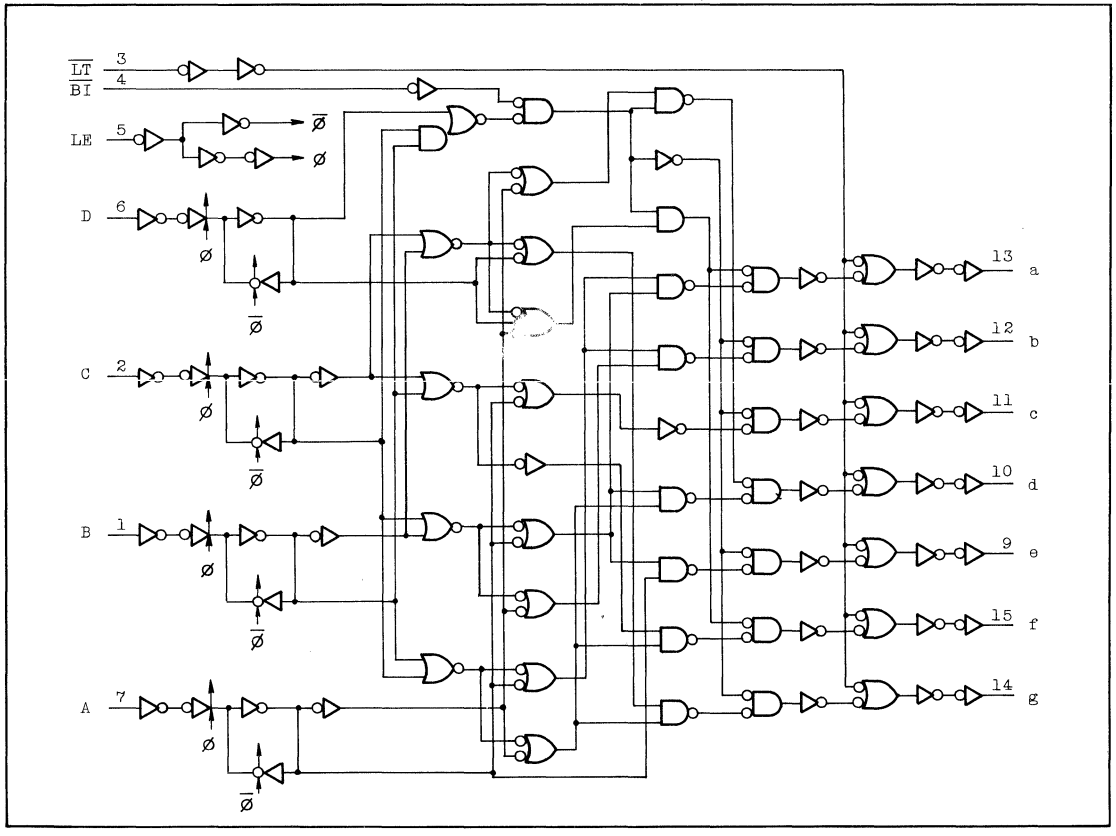


DISPLAY MODE



INPUT CODE										
A	L	H	L	H	L	H	L	H	L	H
B	L	L	H	H	L	L	H	H	L	L
C	L	L	L	L	H	H	H	H	L	L
D	L	L	L	L	L	L	L	L	H	H
DISPLAY	0	1	2	3	4	5	6	7	8	9

LOGIC DIAGRAM



TRUTH TABLE

INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

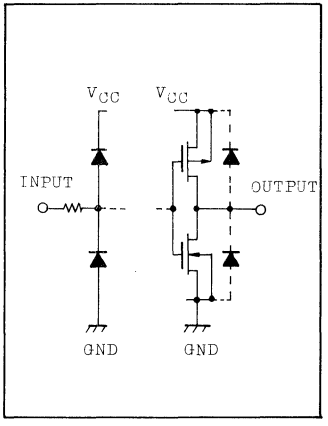
X: Don't care.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25/-35	mA
DC V_{CC}/Ground Current	I_{CC}	+150/-50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C
shall be applied until 300mW.

INPUT and OUTPUT
EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

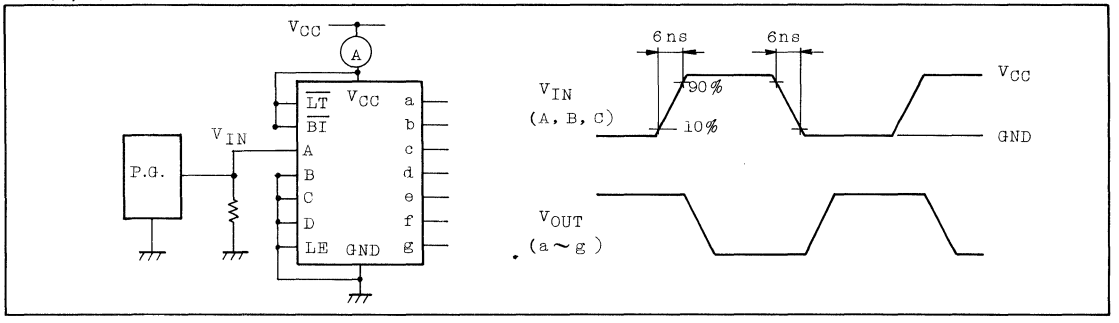
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-20[illegible]	4.5	3.20	3.80	-	2.90	-	
			I_{OH}=-[illegible].2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

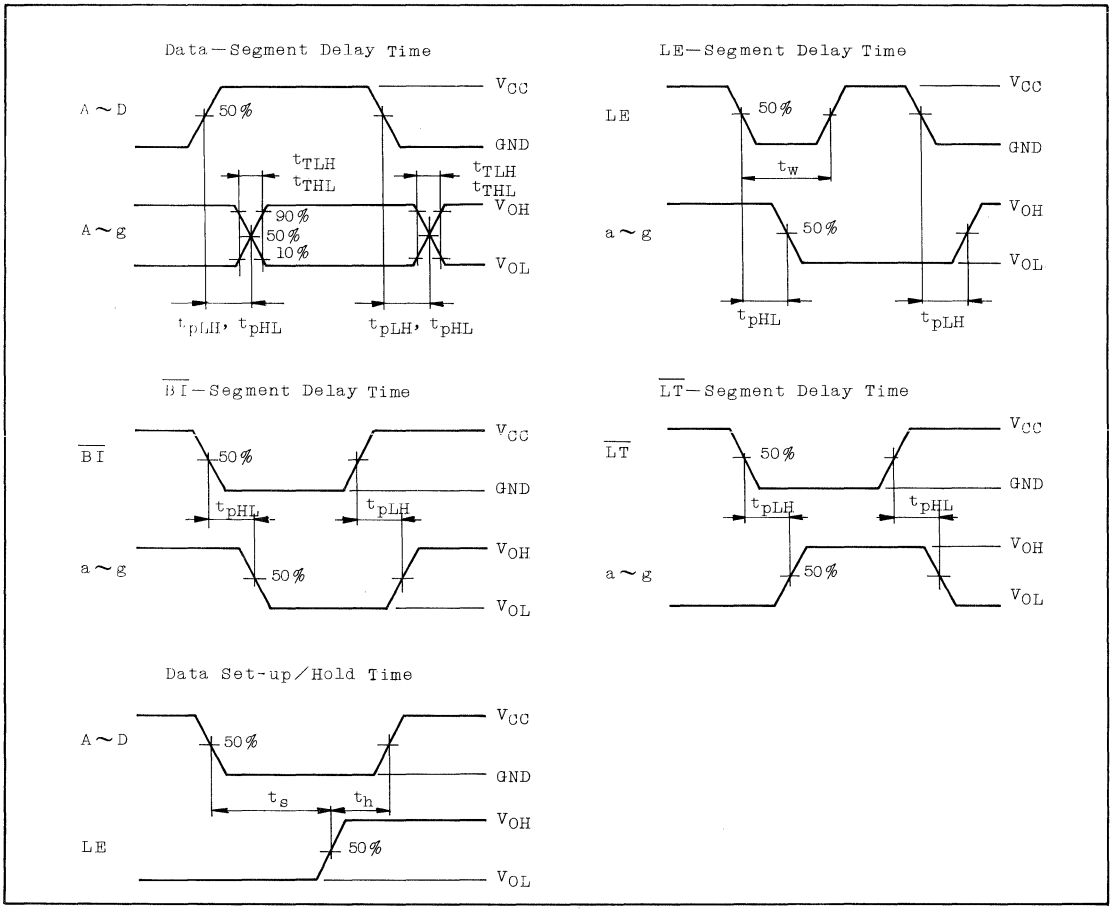
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time Low to High	t_{TLH}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Output Transition Time High to Low	t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (BCD-Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Propagation Delay Time ($\overline{BI}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	116	250	-	315	
			4.5	-	29	50	-	63	
			6.0	-	25	43	-	54	
Propagation Delay Time ($\overline{LT}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Propagation Delay Time (LE - Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Minimum Pulse Width (LE)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Data Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	136	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

$I_{CC(opr)}$ TEST CIRCUIT

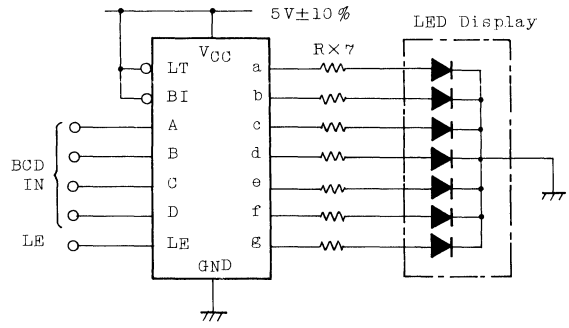


SWITCHING CHARACTERISTICS TEST WAVEFORM



APPLICATION CIRCUIT

Static Display Circuit



Recommended Resistance R

DISPLAY	COLOR	LETTER HIGHT	R
TLR358	Red	13.4mm	390Ω
TLR362	"	14.2	"
TLR332	"	7.6	"
TLR342	"	10.9	"
TLG358	Green	13.4mm	160Ω
TLG362	"	14.2	"
TLG332	"	7.6	"
TLG342	"	10.9	"

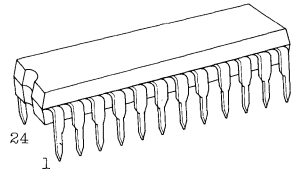
TC74HC4514P
TC74HC4515P

TC74HC4514P 4-TO-16 LINE DECODER/LATCH
TC74HC4515P 4-TO-16 LINE DECODER/LATCH (INV.)

The TC74HC4514 and TC74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTS fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. A binary code stored in the four input latches (A thru D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of latches. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at 25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V ∿ 6V
- Pin and Function Compatible with 4514B/4515B



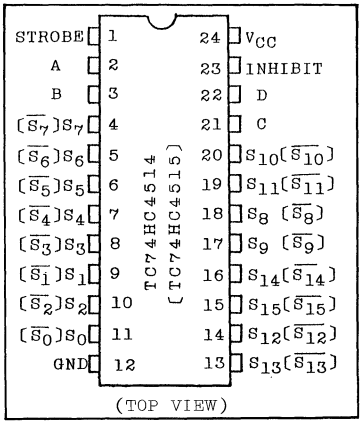
DIP24(3D24A-P)
0.300 INCH(7.62mm) ROW SPACING

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

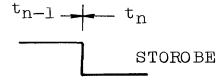


TRUTH TABLE

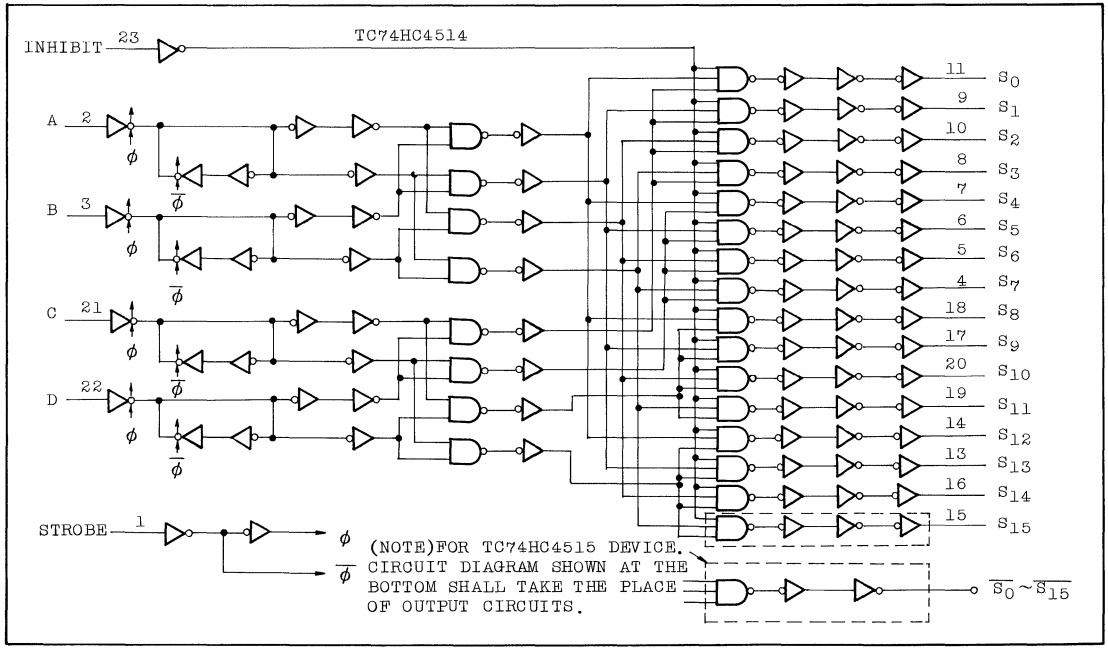
INPUTS					SELECTED OUTPUT TC74HC4514P — "H" (TC74HC4515P — "L")
INHIBIT	A	B	C	D	
L	L	L	L	L	S_0 ($\overline{S_0}$)
L	H	L	L	L	S_1 ($\overline{S_1}$)
L	L	H	L	L	S_2 ($\overline{S_2}$)
L	H	H	L	L	S_3 ($\overline{S_3}$)
L	L	L	H	L	S_4 ($\overline{S_4}$)
L	H	L	H	L	S_5 ($\overline{S_5}$)
L	L	H	H	L	S_6 ($\overline{S_6}$)
L	H	H	H	L	S_7 ($\overline{S_7}$)
L	L	L	L	H	S_8 ($\overline{S_8}$)
L	H	L	L	H	S_9 ($\overline{S_9}$)
L	L	H	L	H	S_{10} ($\overline{S_{10}}$)
L	H	H	L	H	S_{11} ($\overline{S_{11}}$)
L	L	L	H	H	S_{12} ($\overline{S_{12}}$)
L	H	L	H	H	S_{13} ($\overline{S_{13}}$)
L	L	H	H	H	S_{14} ($\overline{S_{14}}$)
L	H	H	H	H	S_{15} ($\overline{S_{15}}$)
H	X	X	X	X	TC74HC4514 — ALL OUTPUTS "L" (TC74HC4515 — ALL OUTPUTS "H")

- X : DON'T CARE
- STROBE="H" ; REFER TO TRUTH TABLE
- STROBE="L"

  DATA AT THE NEGATIVE GOING TRANSITION OF STROBE SHALL BE PROVIDED ON THE EACH OUTPUT WHILE STROBE IS HELD LOW.



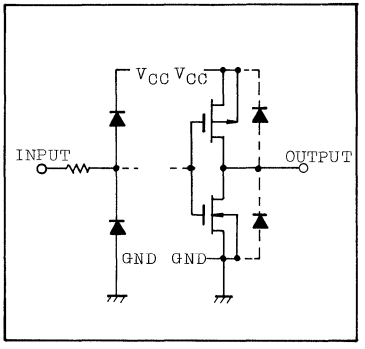
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

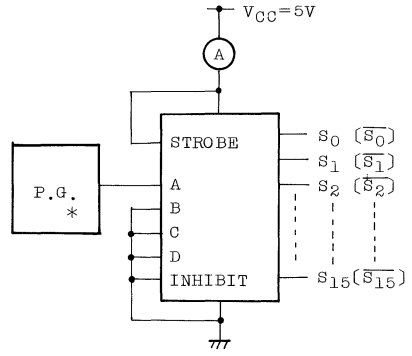
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Rise, Fall Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	nS
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time DATA - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	108	215	-	270	
			4.5	-	27	43	-	54	
			6.0	-	23	37	-	46	
STROBE - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	124	245	-	305	
			4.5	-	31	49	-	61	
			6.0	-	26	42	-	52	
INHIBIT - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Mininum Pulse Width STROBE	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time DATA	t_s		2.0	-	10	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time DATA	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4514P		-	69	-	-	-	
		[TC74HC4515P]		-	[72]	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

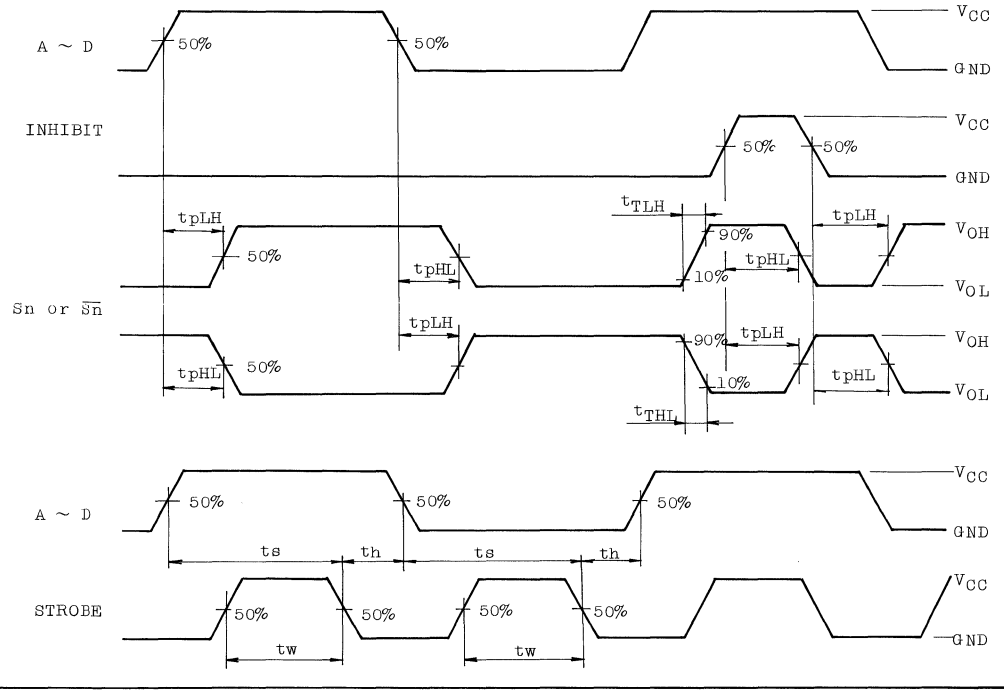
$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISITCS TEST WAVEFORM

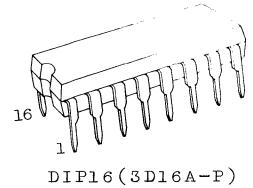


TC74HC4518P/F DUAL BCD COUNTER
TC74HC4520P/F DUAL 4-BIT BINARY COUNTER

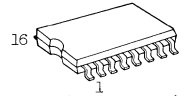
The TC74HC4518 and TC74HC4520 are high speed CMOS DUAL BCD/4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.
It operates ten times as fast as that of metal-gate C^2MOS IC (4518B/4520B) with the same power dissipation.
Since both of TC74HC4518 and TC74HC4520 contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" ($Q_0 \sim Q_3$="L") by giving "H" level signal to CLEAR input regardless of other inputs. The counting condition is changed by the positive going transition of CLOCK input if CE="H" or by the negative going transition of CE if CLOCK="L".
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4518B/4520B



DIP16(3D16A-P)



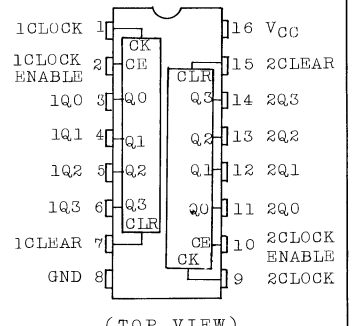
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



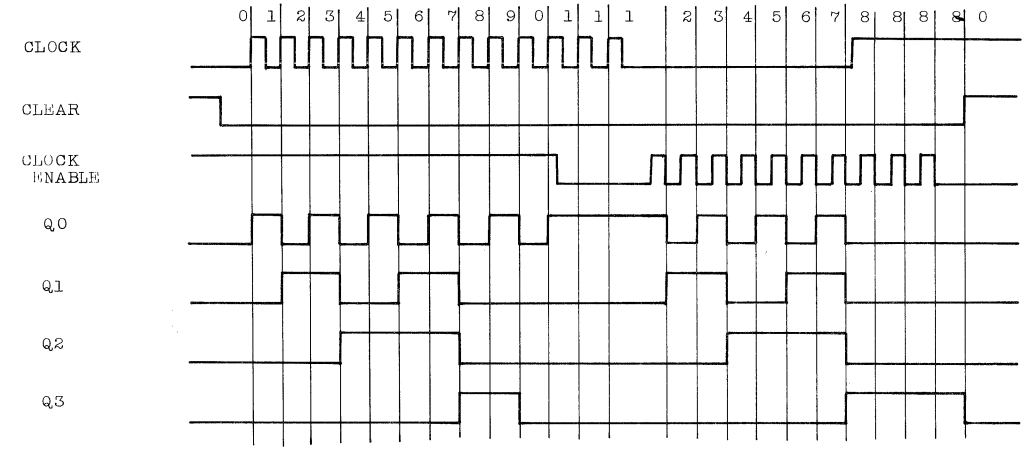
TRUTH TABLE

INPUTS			FUNCTION
CLOCK	CLOCK ENABLE	CLEAR	
↑	H	L	INCLEMENT COUNTER
L	↓	L	INCLEMENT COUNTER
↓	X	L	NO CHANGE
X	↑	L	NO CHANGE
↑	L	L	NO CHANGE
H	↓	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

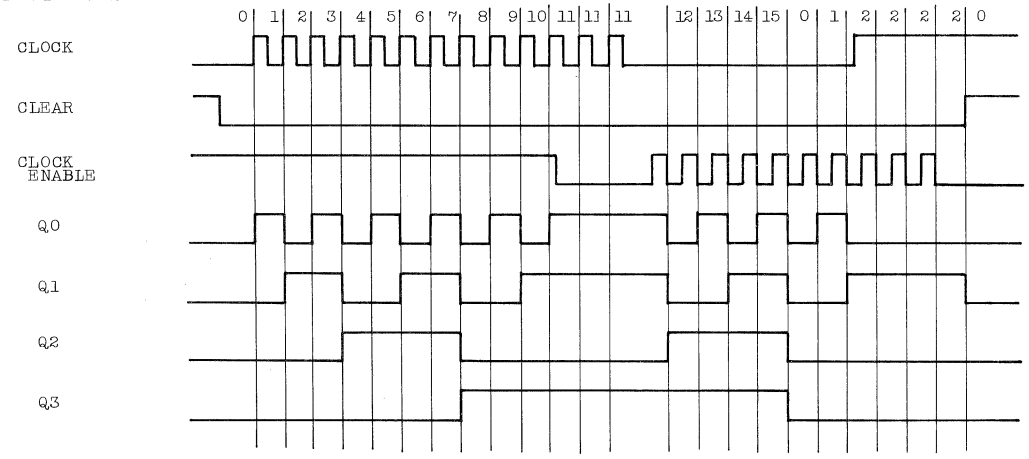
X : DON'T CARE

TIMING CHART

TC74HC4518

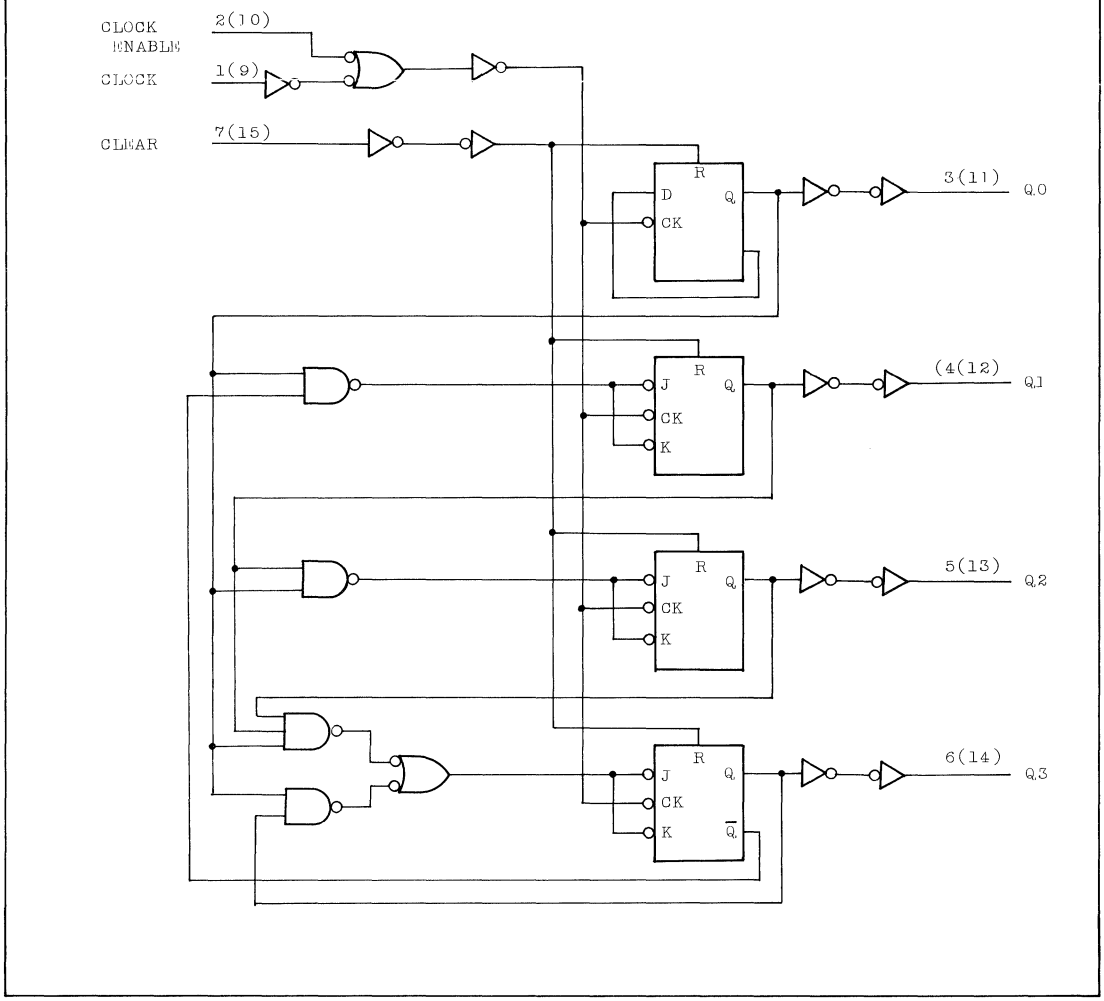


TC74HC4520

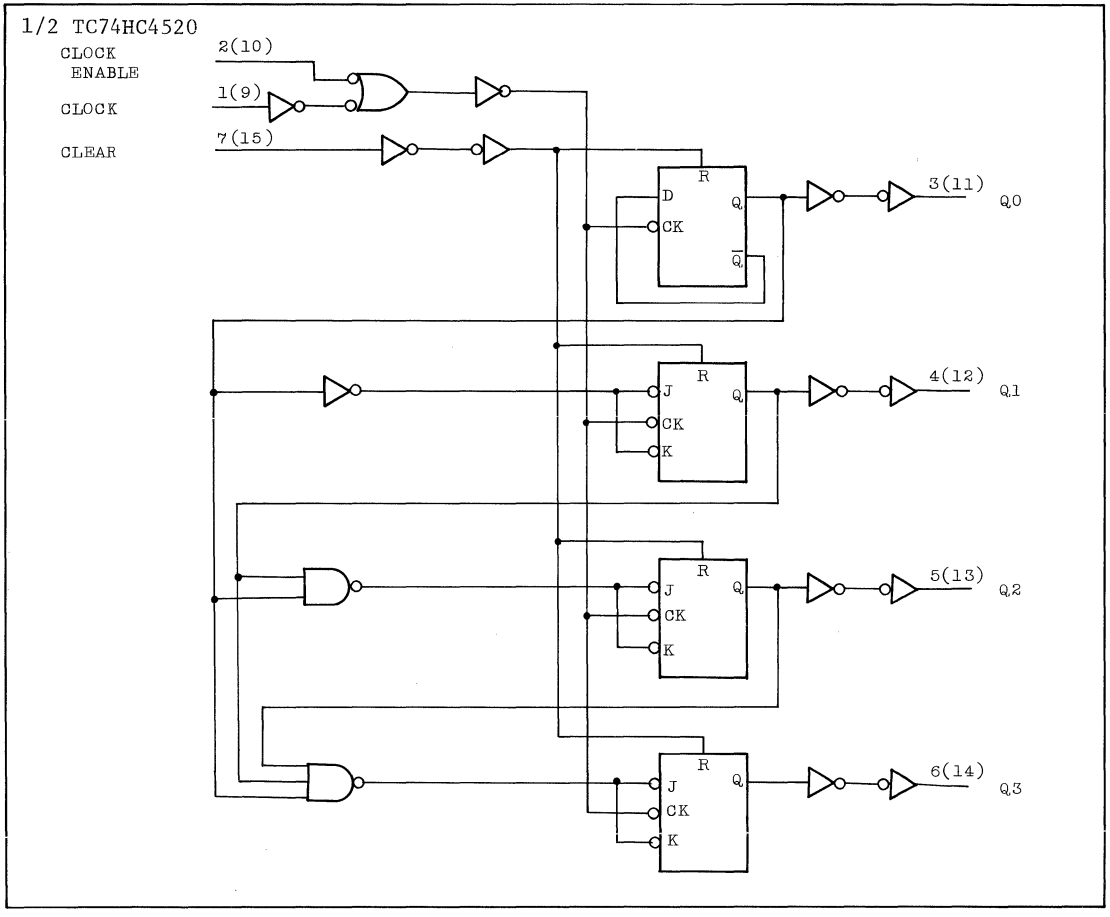


LOGIC DIAGRAM

1/2 TC74HC4518



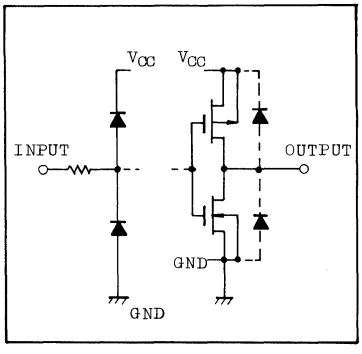
LOGIC DIAGRAM (Continued)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CK, CE - Qn)	t_{pLH} t_{pHL}		2.0	-	100	190	-	240	
			4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time (CLR - Qn)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	25	48	-	20	-	
			6.0	29	56	-	24	-	

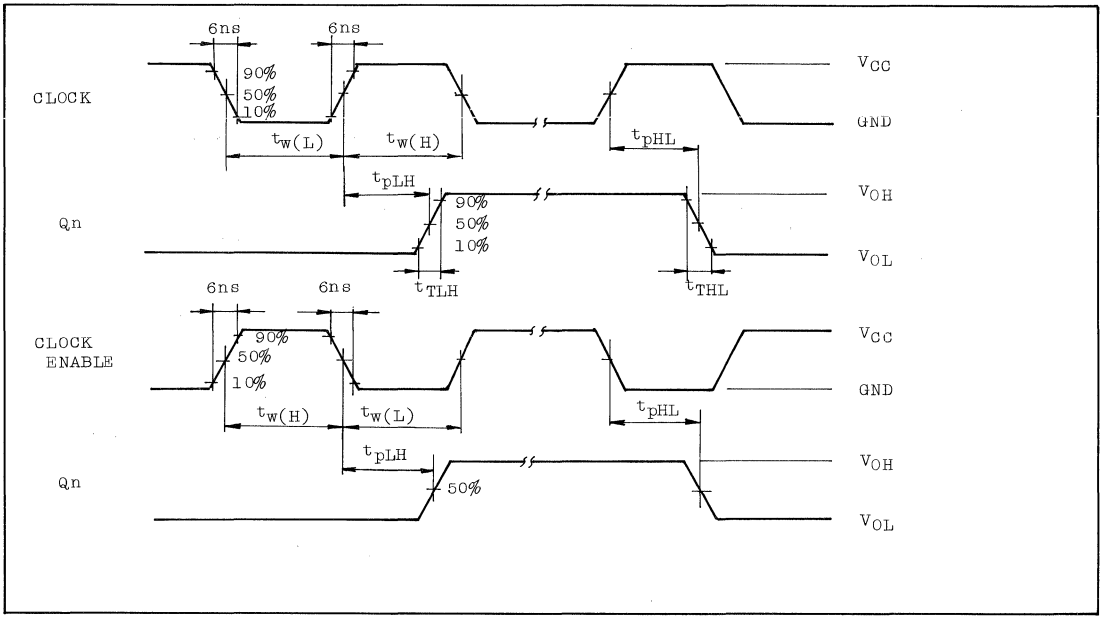
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CK, CE)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum PUlse Width (CLR)	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Removal Time (CLR)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4518		-	145	-	-	-	
		TC74HC4520		-	145	-	-	-	

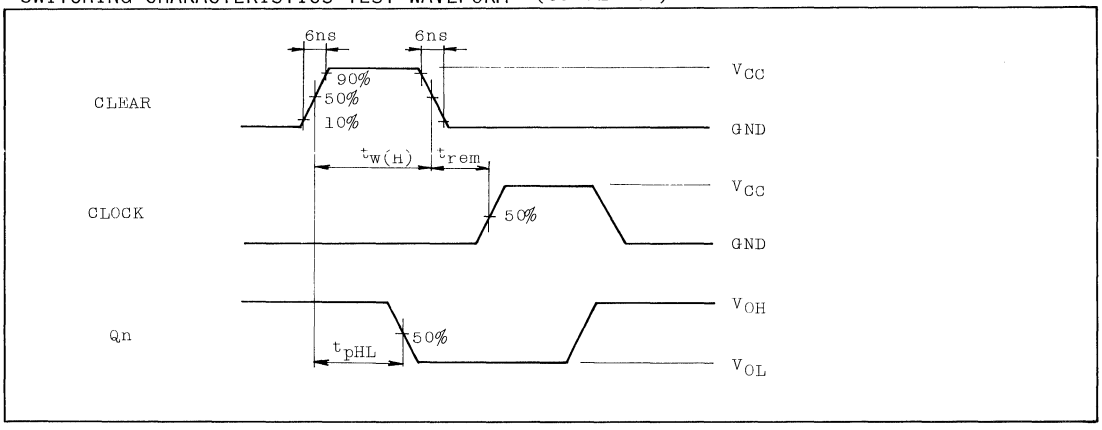
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

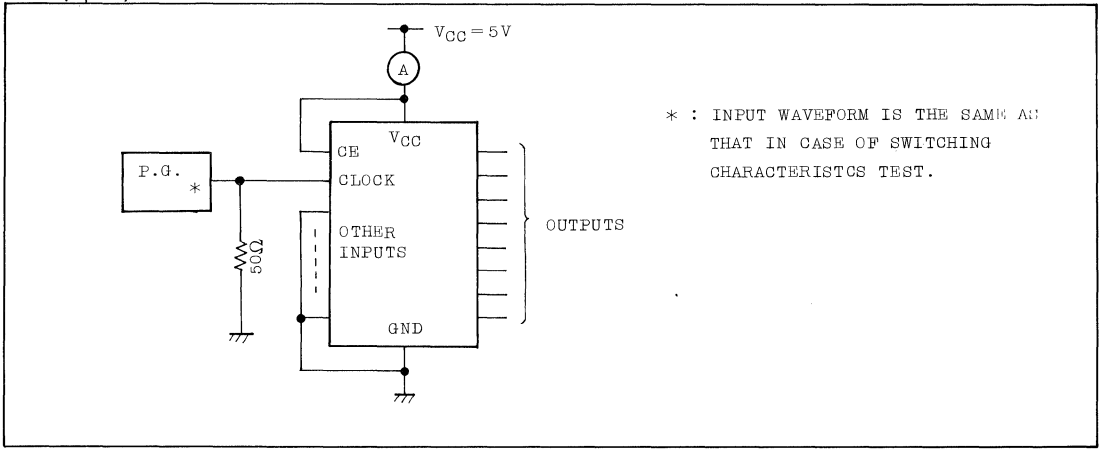
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTCS TEST.

TC74HC4538P/F

TC74HC4538P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

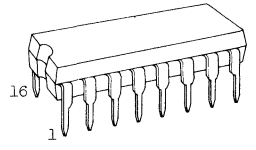
The TC74HC4538 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Positive-edge input), another is $\overline{B}$ INPUT (Negative-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CD}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC} = 2.0V from 5kΩ to 1MΩ
$V_{CC} \geqq$ 3.0V from 1kΩ to 1MΩ

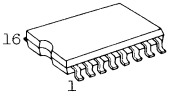
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=27nS(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Wide Output Pulse Width Range ..... t_W(OUT)=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



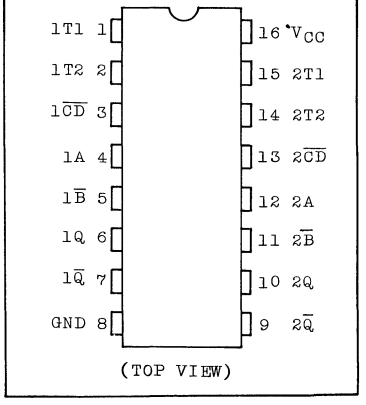
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

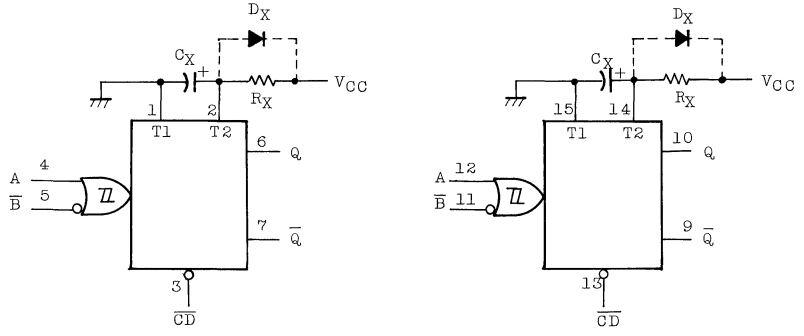


TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎎	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⎍	⎎	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

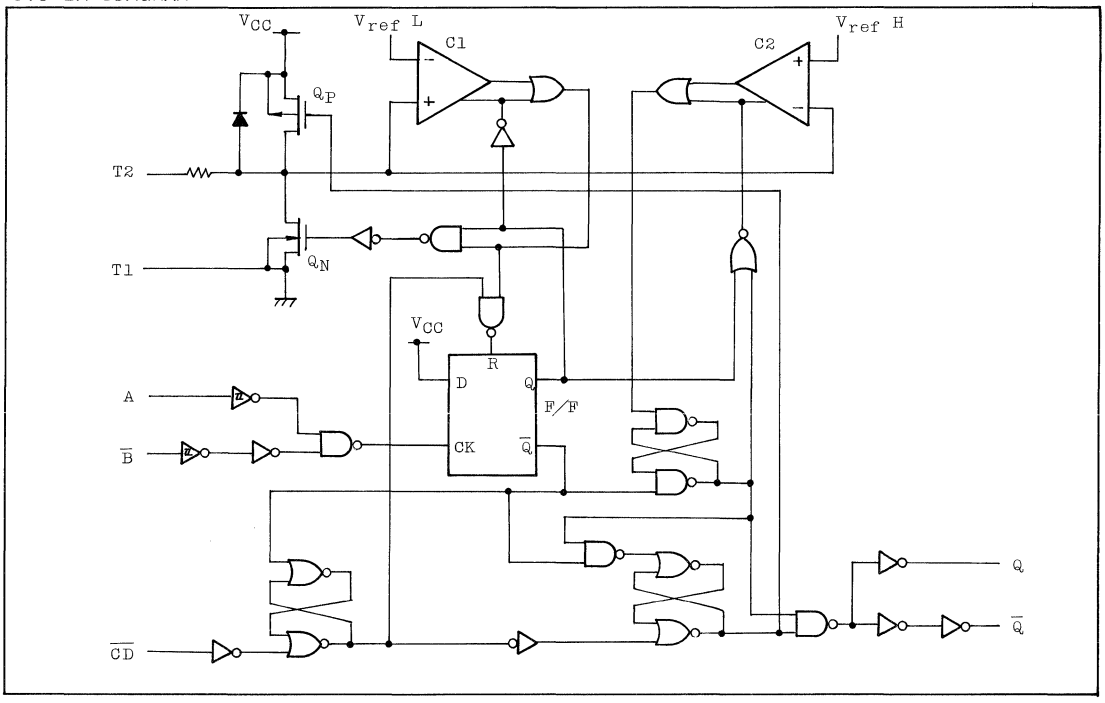
External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA.
In the case of large Cx, limitation of falling down time of voltage supply is as follows

$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

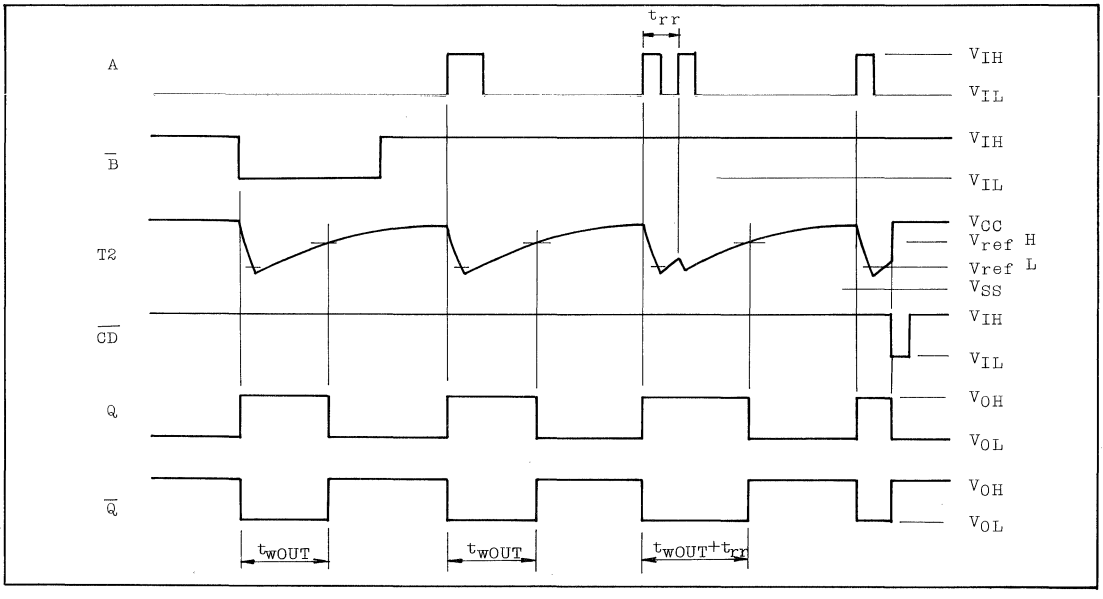
(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC}.)

In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

SYSTEM DIAGRAM



TIMING CHART



FUCNTIONAL DESCRIPTION

(1) Stand-by State

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to T2 node) are in off state.
Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition A INPUT is "L" level and $\overline{B}$ INPUT have falling down signal. Under the condition $\overline{B}$ INPUT is "H" level and A INPUT has rising up signal.
After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of T2 node becomes lower. If voltage level of T2 falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of T2 starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of T2 changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations.
That means, after triggering the voltage level of T2 becomes VrefH, IC keeps its MONO STABLE STATE.
In the case $Cx \cdot Rx$ are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{w(OUT)}$ is as follows.

$$t_{w(OUT)} = 0.72\ Cx\ Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of T2 falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(Min.) depends on V_{CC} and Cx.

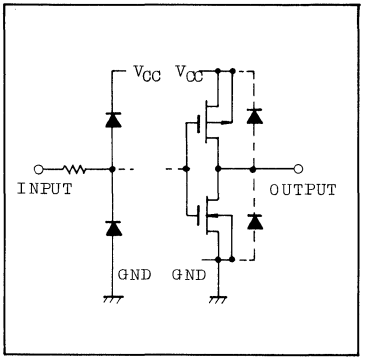
(4) Reset operation

$\overline{CD}$ is normally "H". If $\overline{CD}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level.
This means if $\overline{CD}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CD}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/Cext=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per circuit

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, $\overline{B}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{CD}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Output Pulse Width	t_{wOUT}	Cx=12pF Rx=1kΩ	3.0	-	210	-	-	-	
			5.0	-	140	-	-	-	
		Cx=100pF Rx=10kΩ	3.0	-	1.45	-	-	-	μs
			5.0	-	1.40	-	-	-	
		Cx=1000pF Rx=10kΩ	3.0	-	10.5	-	-	-	
			5.0	-	10.0	-	-	-	
Output Pulse Width Error Between Circuits (In same Package)	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Trigger Pulse Width	$t_{w(H)}$ $t_{w(L)}$	A_{IN} B_{IN}	2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	4.5	-	74	-	-	-	
			6.0	-	63	-	-	-	
		Cx=0.01μF Rx=1kΩ	4.5	-	1.1	-	-	-	μs
			6.0	-	1.0	-	-	-	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{OUT}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	90	-	-	-	

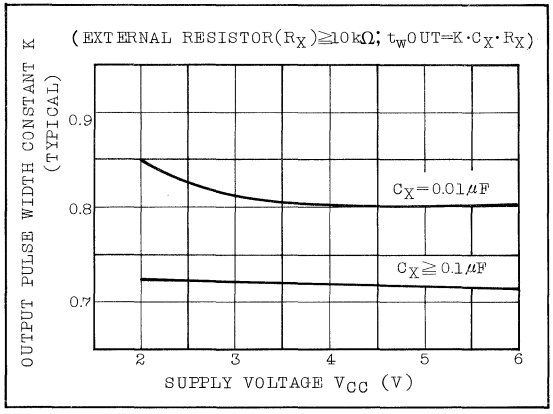
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2$ (per monostable)

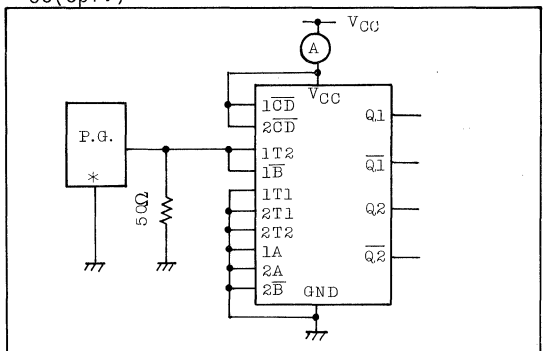
(I_{CC}': Active Supply Current)

(Duty: %)

OUTPUT PULSE WIDTH CONSTANT,K-SUPPLY VOLTAGE

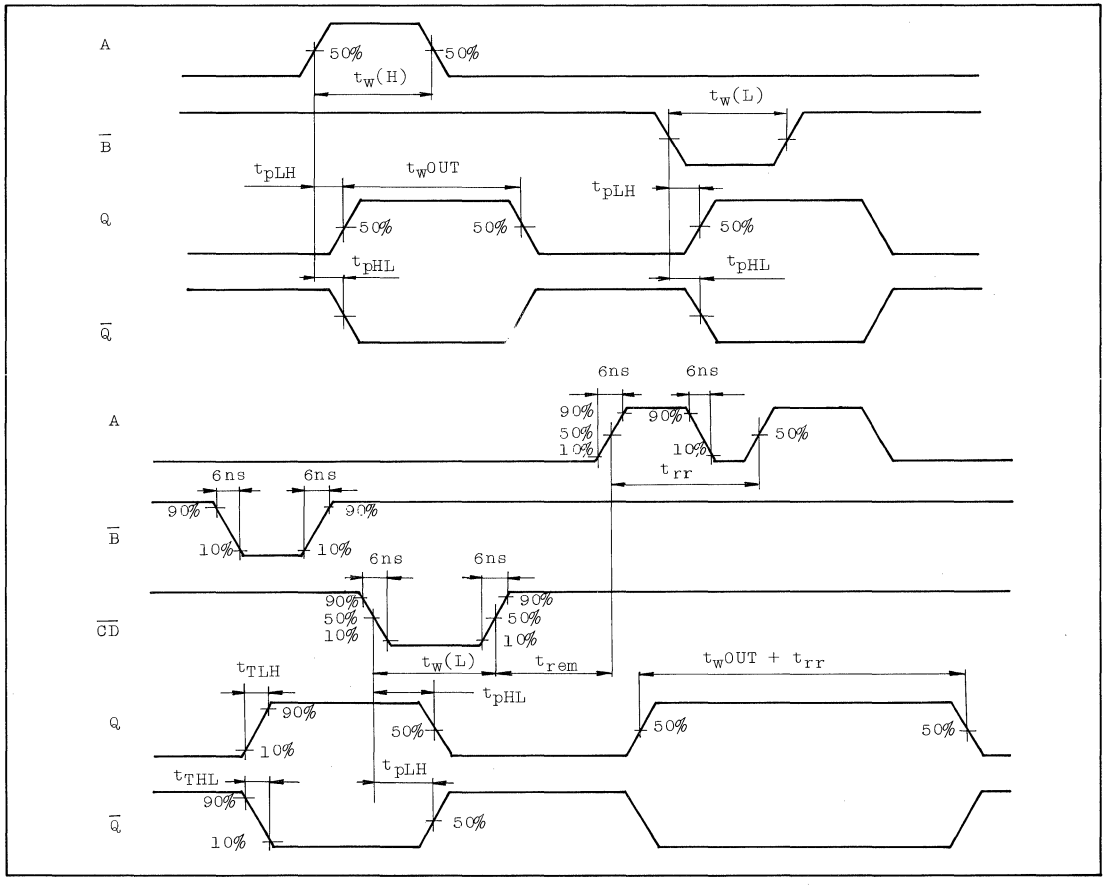


$I_{CC(opr.)}$ TEST WAVEFORM

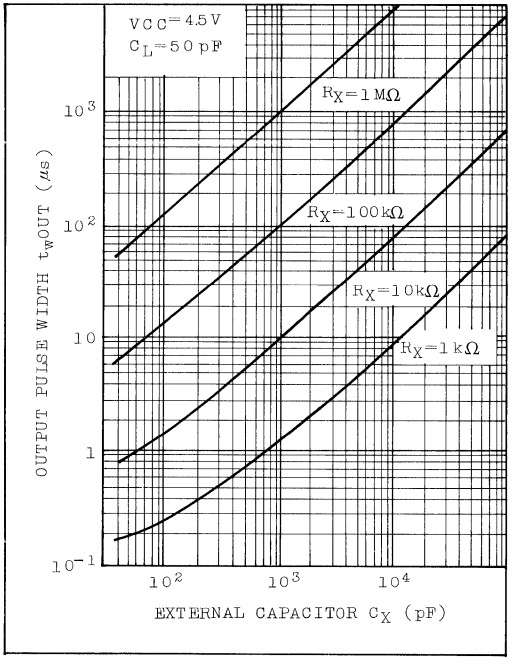


*: INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

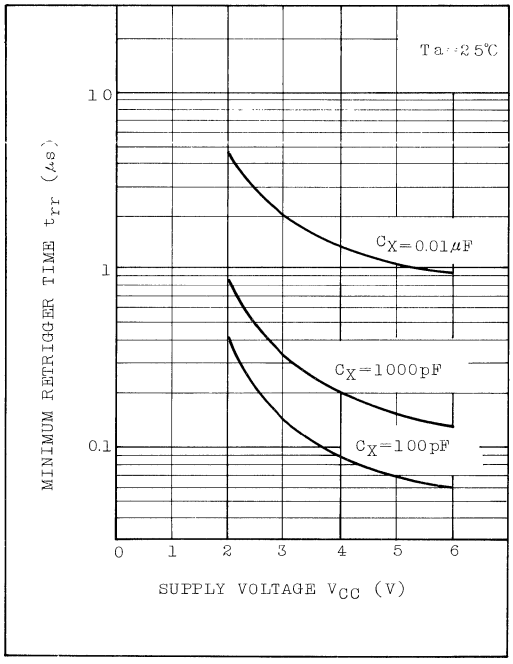
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



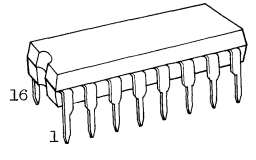
TC74HC4543P/F

TC74HC4543P/F BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

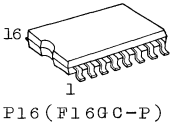
The TC74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated with silicon gate C^2MOS technology. It achieves the high speed latch and decode operation twenty times as fast as the standard CMOS 4511B while maintaining the CMOS low power dissipation. This device consists of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for the liquid crystal display (LCD). When any illegal BCD input signal is applied or BI input is held high, the display is blanked. In case of driving LCD, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as transistor array is required. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_w=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V∿6V
- Pin and Function Compatible with 4543B



DIP16(3D16A-P)



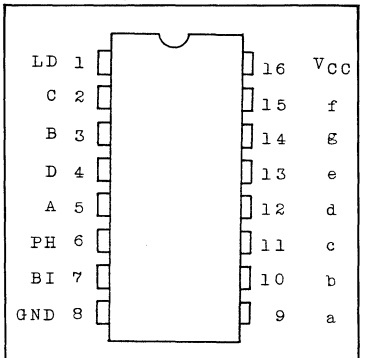
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

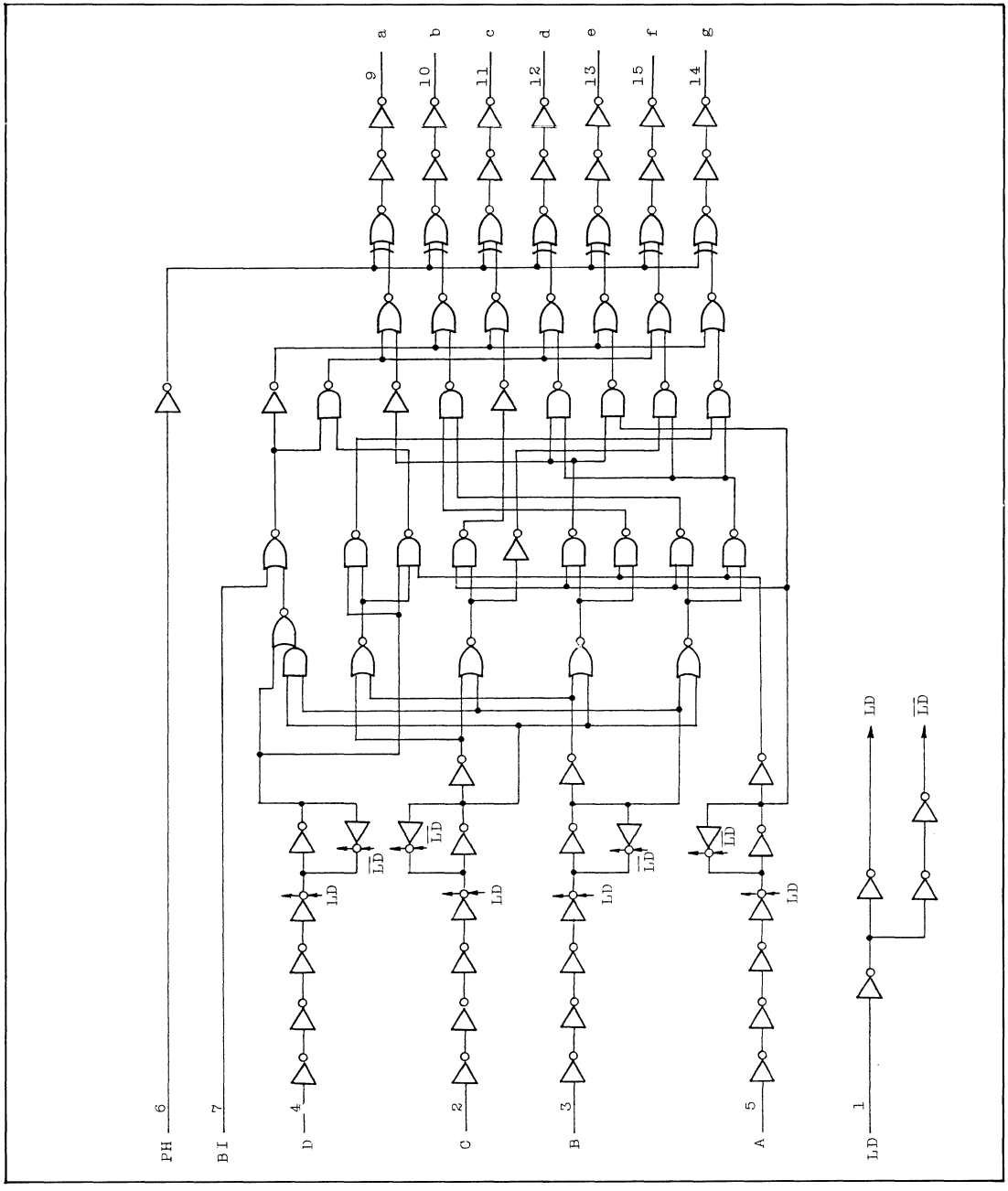
* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

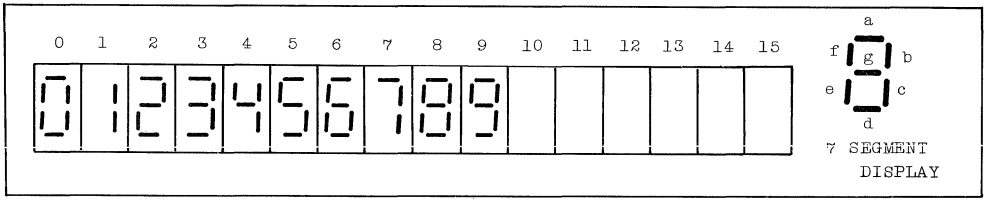
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	###							###
↑	↑	H		↑			INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X : DON'T CARE

↑ : SAME AS ABOVE COMBINATIONS

: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD="H"

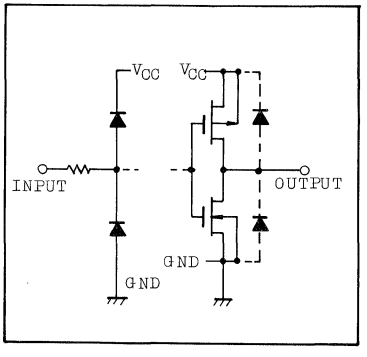
DISPLAY MODE



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time BCD - OUT	t_{pLH}		2.0	-	200	385	-	480	
			4.5	-	50	77	-	96	
	t_{pHL}		6.0	-	43	65	-	82	
BI - OUT	t_{pLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{pHL}		6.0	-	26	41	-	51	
PH - OUT	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	

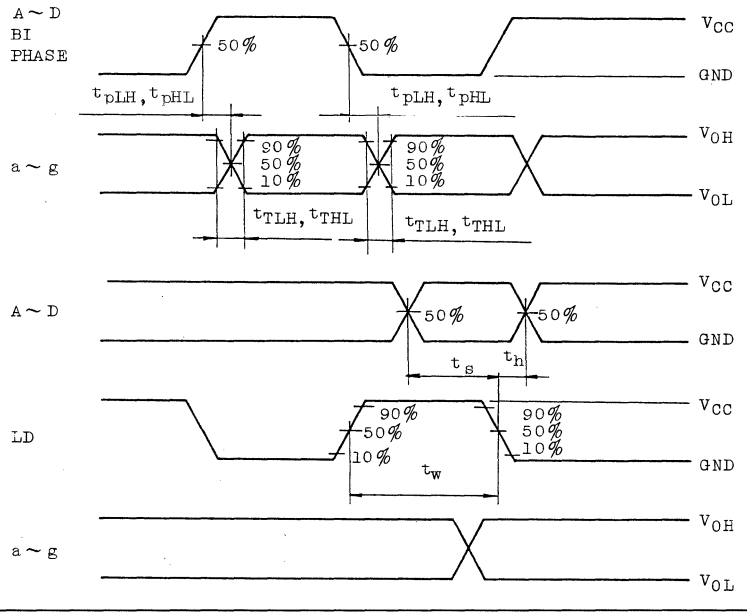
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Minimum Pulse Width (LD)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	30	-	-	-	

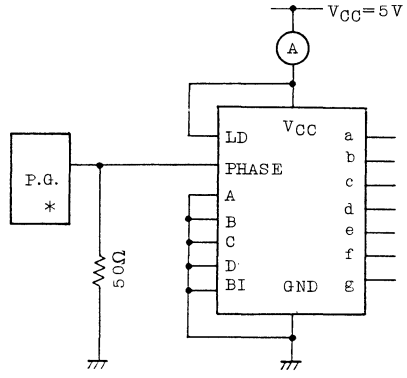
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HCT7007AP/AF

HEX BUFFER

The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

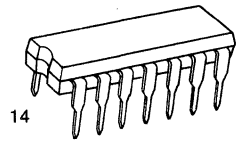
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.

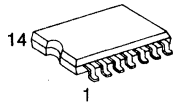
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =11ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs····· V_{IH}=2V(Min.)
  V_{IL} =0.8V(Max.)
- Wide Interfacing ability····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS07

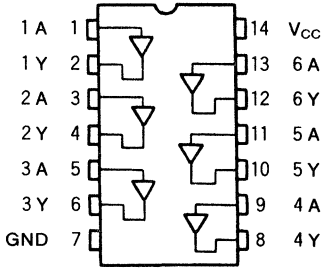


DIP14 (3D14A−P)



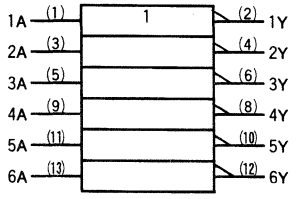
MFP14 (F14GB−P)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	L
H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5～5.5	V
Input Voltage	V_{IN}	0～V_{CC}	V
Output Voltage	V_{OUT}	0～V_{CC}	V
Operating Temperature	Topr	−40～85	℃
Input Rise and Fall Time	tr, tf	0～500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40～85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ～ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ～ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$I_{OH}=-20\ \mu A$	4.5	4.4	4.5	−	4.4	−	V
			$I_{OH}=-4\ mA$	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	$I_{OL}=20\ \mu A$	4.5	−	0.0	0.1	−	0.1	V
			$I_{OL}=4\ mA$	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	$V_{IH}=V_{IL}$ or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IH}=V_{IL}$ or GND		5.5	−	−	1.0	−	10.0	μA
	I_C	PER INPUT: V_{IN} =0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5 5.5	– –	14 12	23 21	– –	28 26	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	22	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

TC74HC7292P
TC74HC7294P

TC74HC7292P PROGRAMMABLE DIVIDER/TIMER
TC74HC7294P PROGRAMMABLE DIVIDER/TIMER

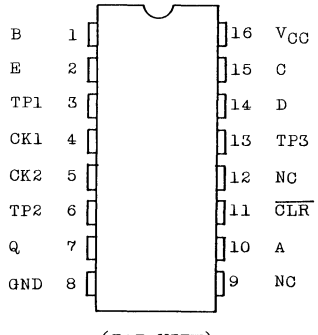
The TC74HC7292 and TC74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table (1)).
The TC74HC7292 can divide from 2^2 to 2^{31}, and the TC74HC7294 can divide from 2^2 to 2^{15}.
Both types feature an active-low clear input to initialize the state of all flip-flops.
To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the 74HC7292 and TP on the 74HC7294).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... $f_{MAX}=\begin{matrix}50MHz\ [7292]\\60MHz\ [7294]\end{matrix}$ (Typ.) at $V_{CC}=5V$
- Low Power Dissipation ..... $I_{CC}=4\mu A$(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}=28\%\ V_{CC}$(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Summetrical Output Impedance ..... $|I_{OH}|=I_{OL}=4mA$(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC(Opr.)}=2V\sim 6V$
- Pin and Function Compatible with 74LS292/294

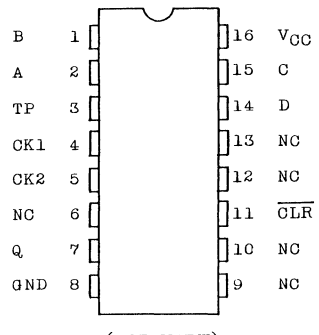
PIN ASSIGNMENT

TC74HC7292



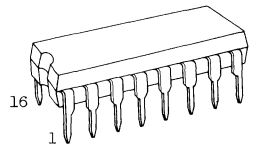
(TOP VIEW)

TC74HC7294



(TOP VIEW)

NC: NO CONNECTION



DIP16(3D16A-P)

TRUTH TABLE

$\overline{\text{CLEAR}}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↓	L	UP Count
H	L	↓	
H	H	X	NO Change
H	X	H	

TC74HC7292

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP2	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

TRUTH TABLE

TC74HC7294

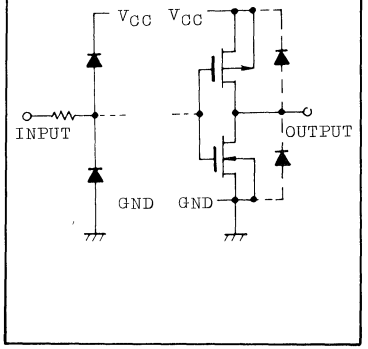
PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

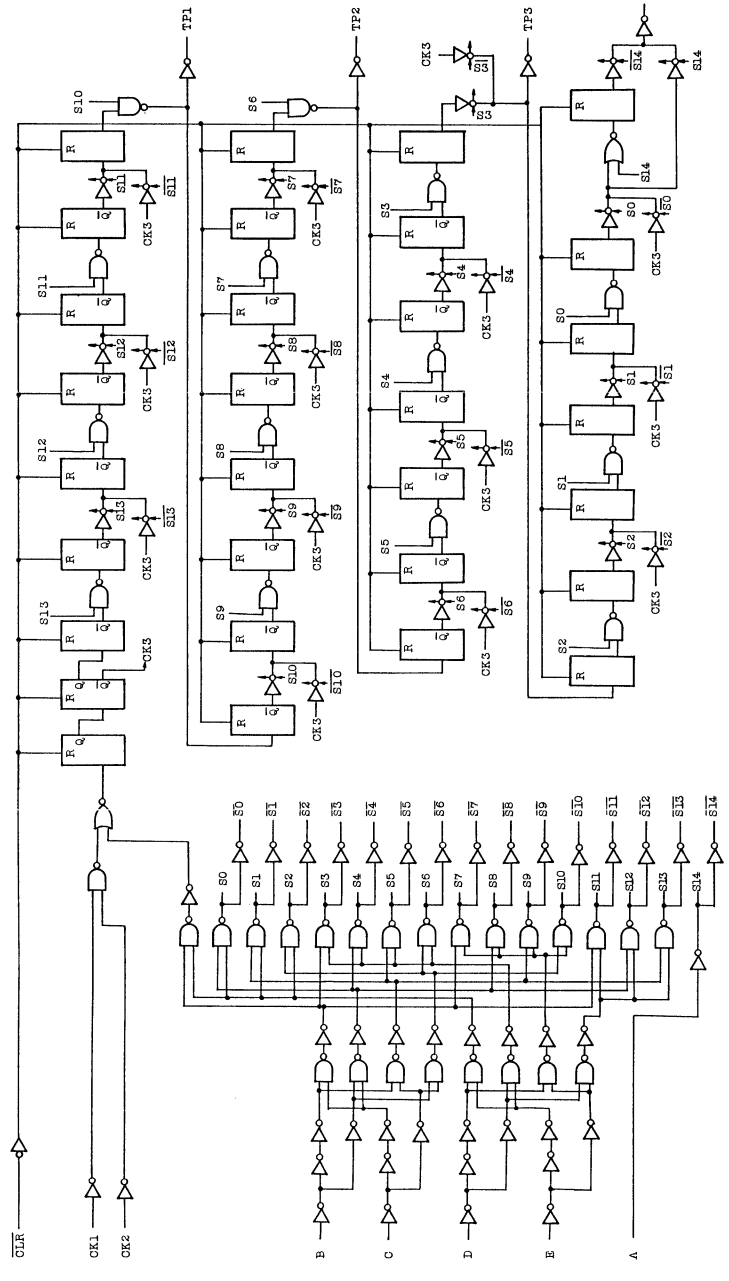
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



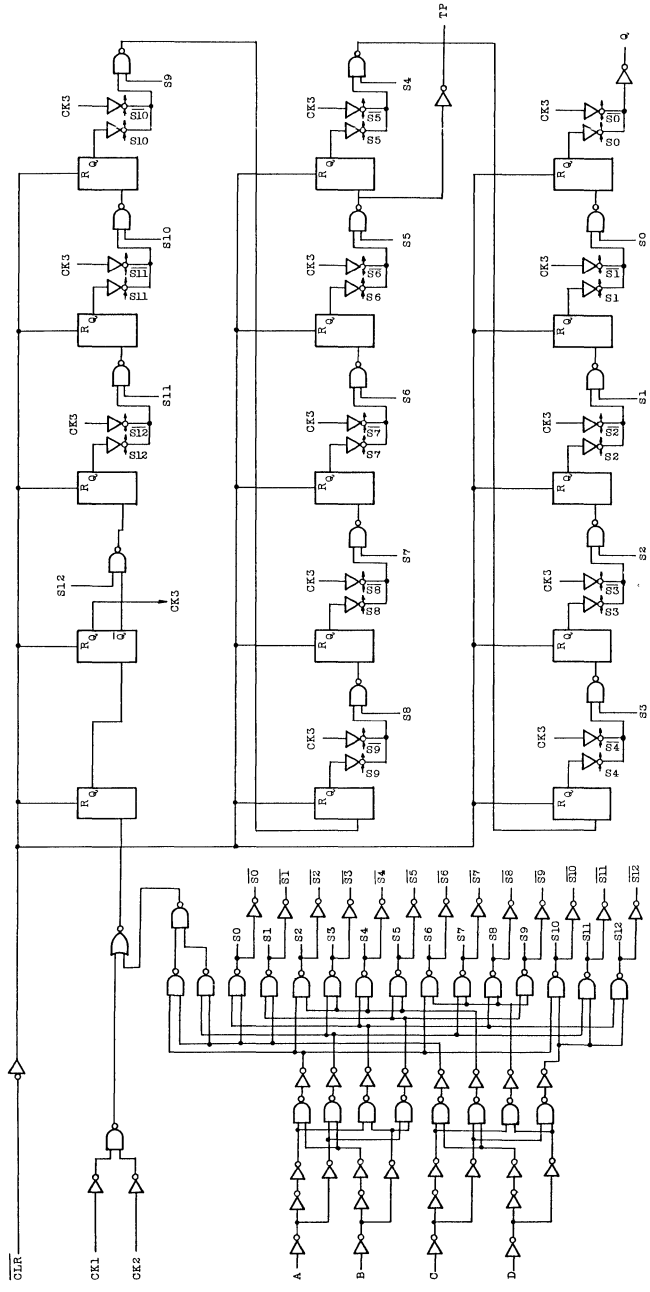
LOGIC DIAGRAM

TC74HC7292



LOGIC DIAGRAM

TC74HC7294



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

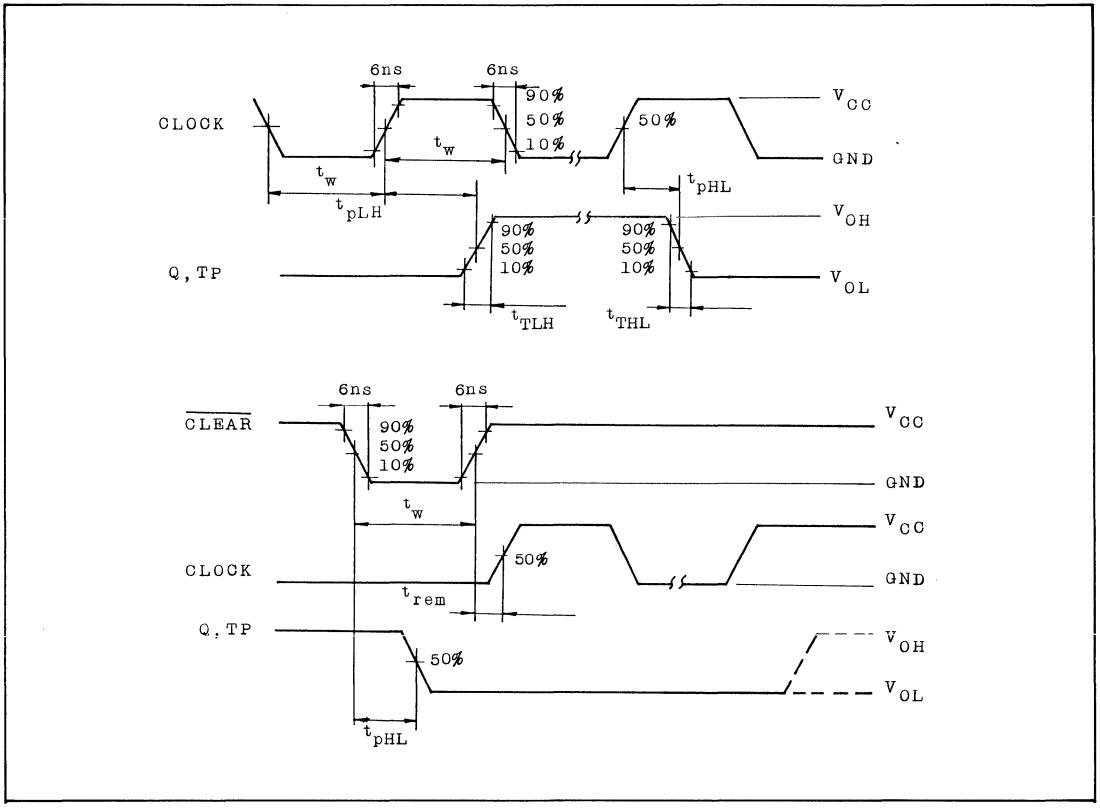
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Transition Time (TP)	t_{TLH}		2.0	-	132	255	-	320	
	t_{THL}		4.5	-	33	51	-	64	
			6.0	-	28	43	-	54	
Propagation Delay Time (CLOCK - Q) *	t_{pLH}	B="H" A=C=D=E="L"	2.0	-	264	500	-	625	
	t_{pHL}		4.5	-	66	100	-	125	
			6.0	-	56	85	-	106	
Propagation Delay Time (CLOCK - Q) **	t_{pLH}	B="H" A=C=D="L"	2.0	-	236	455	-	570	
	t_{pHL}		4.5	-	59	91	-	114	
			6.0	-	50	77	-	97	
Propagation Delay Time ($\overline{CLEAR}$ - Q) *	t_{pHL}		2.0	-	224	425	-	530	
			4.5	-	56	85	-	106	
			6.0	-	48	72	-	90	
Propagation Delay Time ($\overline{CLEAR}$ - Q) **	t_{pHL}		2.0	-	204	390	-	490	
			4.5	-	51	78	-	98	
			6.0	-	43	66	-	83	
Maximum Clock Frequency *	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	32	48	-	26	-	
			6.0	38	56	-	31	-	
Maximum Clock Frequency **	f_{MAX}		2.0	7	14	-	6	-	ns
			4.5	32	55	-	30	-	
			6.0	44	65	-	35	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	36	100	-	125	
	$t_{w(L)}$		4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Pulse Width ($\overline{CLEAR}$) *	$t_{w(L)}$		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Pulse Width ($\overline{CLEAR}$) **	$t_{w(L)}$		2.0	-	72	175	-	220	
			4.5	-	18	35	-	44	
			6.0	-	15	30	-	37	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	74HC7292		-	22	-	-	-	
		74HC7294		-	23	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

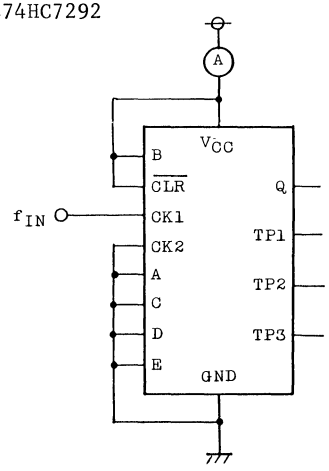
(2): * ; for TC74HC7292
**; for TC74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM

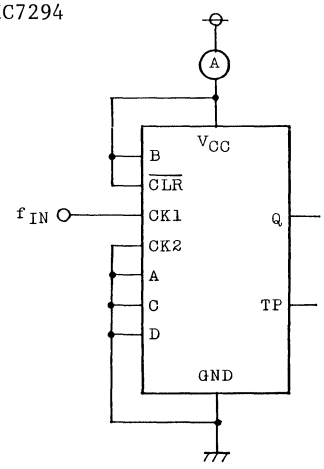


I_{CC}(Opr.) TEST CIRCUIT

TC74HC7292



TC74HC7294

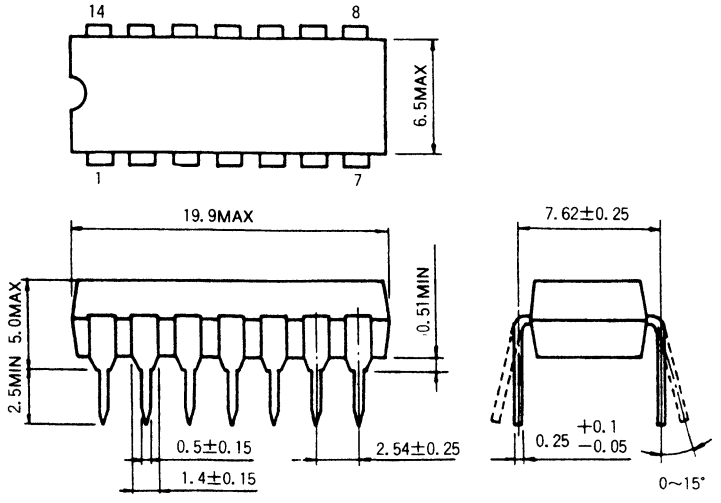


* Input transition time is the same as that in case of switching characteristics test.

11. OUTLINE DRAWINGS

DIP 14 PIN OUTLINE DRAWING (3D14A-P)

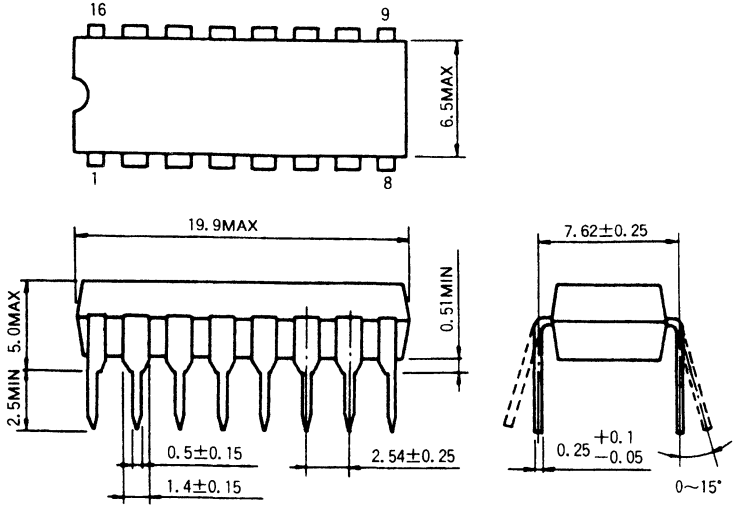
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No.14 leads.

DIP 16 PIN OUTLINE DRAWING (3D16A-P)

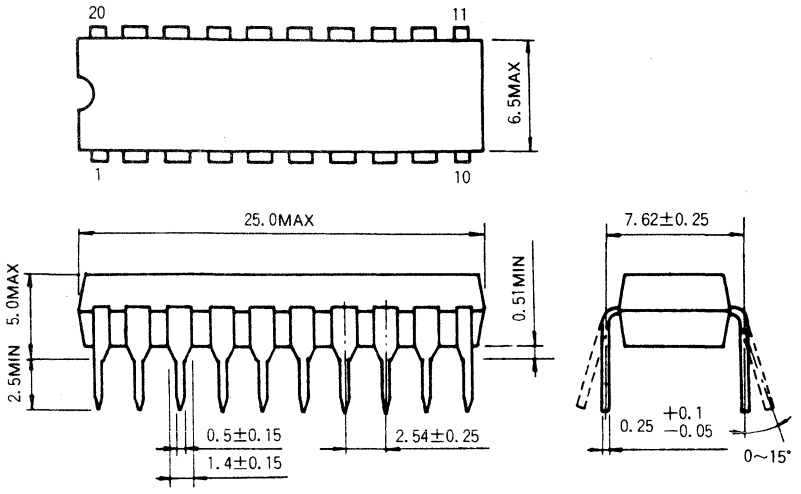
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No.16 leads.

DIP 20 PIN OUTLINE DRAWING (3D20A-P)

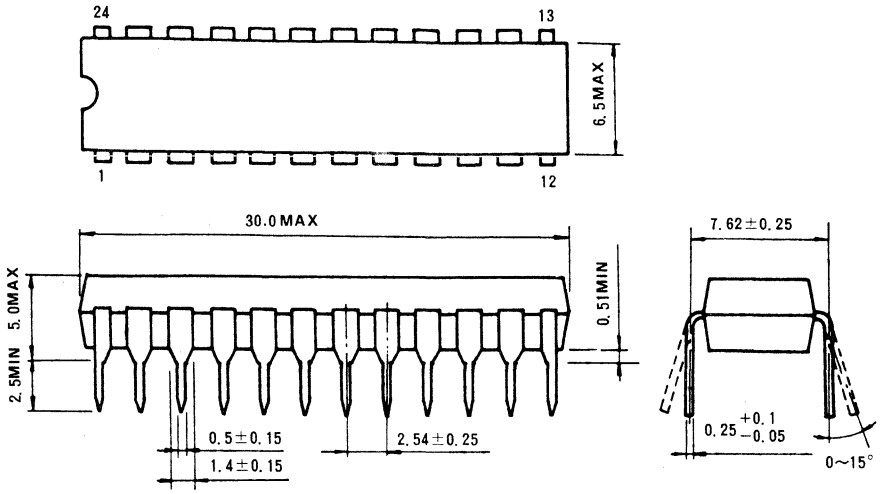
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 20 leads.

DIP 24 PIN OUTLINE DRAWING(3D24A-P)

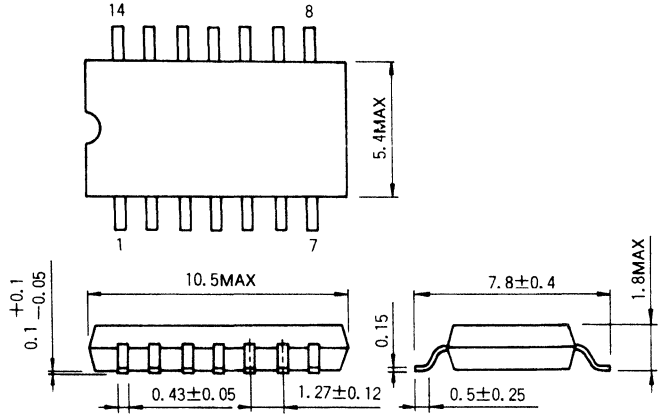
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 24 leads.

MFP 14 PIN OUTLINE DRAWING (F14GB-P)

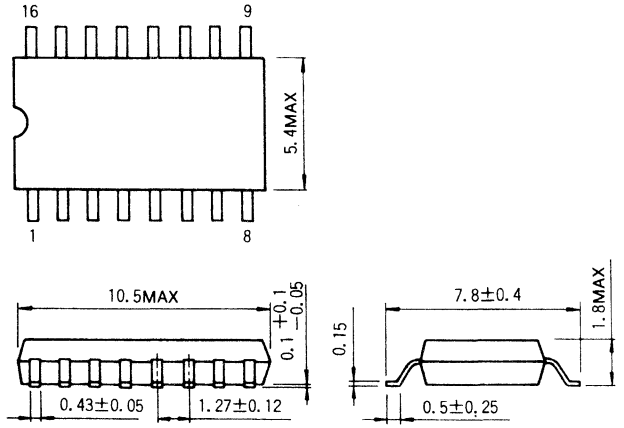
Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 14 leads.

MFP 16 PIN OUTLINE DRAWING (F16GC-P)

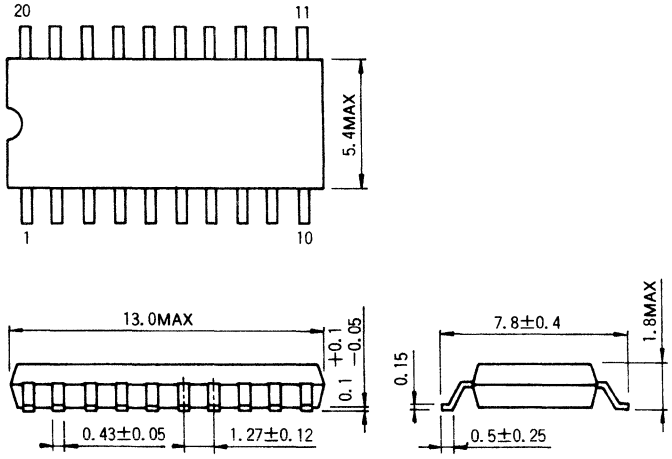
Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 16 leads.

MFP 20 PIN OUTLINE DRAWING (F20GA-P)

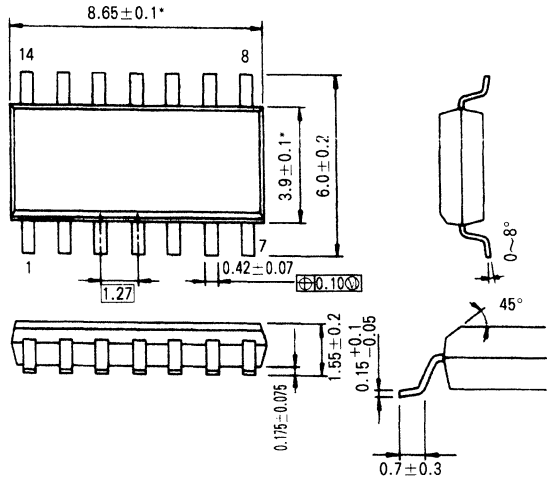
Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 20 leads.

150mil BODY SOP 14PIN OUTLINE DRAWING (SOP14-P-225A)

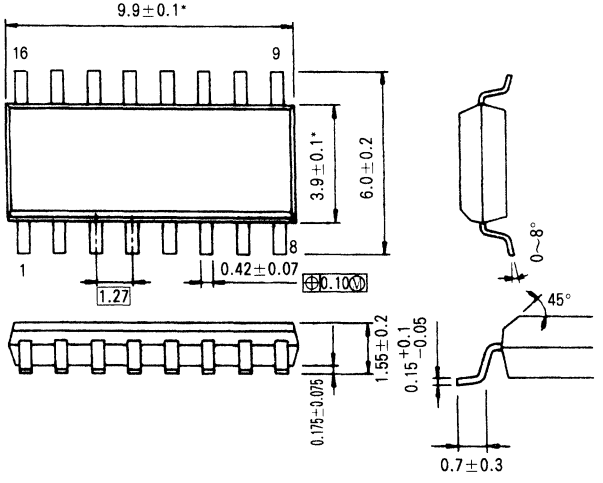
Unit in mm



Note) Dimensions denotes * are reference datums on the molded body and don't include mold flash or protrusions.
Mold flash or protrusion shall not exceed 0.15mm on any side.

150mil BODY SOP 16PIN OUTLINE DRAWING (SOP16-P-225A)

Unit in mm



Note) Dimensions denotes * are reference datums on the molded body and don't include mold flash or protrusions.
Mold flash or protrusion shall not exceed 0.15mm on any side.

12. CROSS REFERENCE TABLE

CROSS REFERENCE TABLE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC00A	MC74HC00	SN74HC00	CD74HC00	PC74HC00	MM74HC00
TC74HCT00A			CD74HCT00	PC74HCT00	MM74HCT00
TC74HC02A	MC74HC02	SN74HC02	CD74HC02	PC74HC02	MM74HC02
TC74HCT02A			CD74HCT02	PC74HCT02	
TC74HC03A	MC74HC03	SN74HC03	CD74HC03	PC74HC03	MM74HC03
TC74HC04A	MC74HC04	SN74HC04	CD74HC04	PC74HC04	MM74HC04
TC74HCU04A	MC74HCU04	SN74HCU04	CD74HCU04	PC74HCU04	MM74HCU04
TC74HCT04A	MC74HCT04		CD74HCT04	PC74HCT04	MM74HCT04
TC74HC05A	MC74HC05	SN74HC05			
TC74HC07A					
TC74HC08A	MC74HC08	SN74HC08	CD74HC08	PC74HC08	MM74HC08
TC74HCT08A			CD74HCT08	PC74HCT08	
TC74HC09A		SN74HC09			
TC74HC10A	MC74HC10	SN74HC10	CD74HC10	PC74HC10	MM74HC10
TC74HC11A	MC74HC11	SN74HC11	CD74HC11	PC74HC11	MM74HC11
TC74HC14A	MC74HC14	SN74HC14	CD74HC14	PC74HC14	MM74HC14
TC74HC20A	MC74HC20	SN74HC20	CD74HC20	PC74HC20	MM74HC20
TC74HC21A		SN74HC21	CD74HC21	PC74HC21	
TC74HC27A	MC74HC27	SN74HC27	CD74HC27	PC74HC27	MM74HC27
TC74HC30A	MC74HC30	SN74HC30	CD74HC30	PC74HC30	MM74HC30
TC74HC32A	MC74HC32	SN74HC32	CD74HC32	PC74HC32	MM74HC32
TC74HCT32A			CD74HCT32	PC74HCT32	
TC74HC42A	MC74HC42	SN74HC42	CD74HC42	PC74HC42	MM74HC42
TC74HC51A	MC74HC51	SN74HC51			MM74HC51
TC74HC73A	MC74HC73	SN74HC73	CD74HC73	PC74HC73	MM74HC73
TC74HC74A	MC74HC74	SN74HC74	CD74HC74	PC74HC74	MM74HC74
TC74HCT74A			CD74HCT74	PC74HCT74	MM74HCT74
TC74HC75A	MC74HC75	SN74HC75	CD74HC75	PC74HC75	MM74HC75
TC74HC76A	MC74HC76	SN74HC76			MM74HC76
TC74HC77A		SN74HC77			
TC74HC85A	MC74HC85	SN74HC85	CD74HC85	PC74HC85	MM74HC85
TC74HC86A	MC74HC86	SN74HC86	CD74HC86	PC74HC86	MM74HC86
TC74HCT86A			CD74HCT86	PC74HCT86	
TC74HC107A	MC74HC107	SN74HC107	CD74HC107	PC74HC107	MM74HC107
TC74HC109A	MC74HC109	SN74HC109	CD74HC109	PC74HC109	MM74HC109
TC74HC112A	MC74HC112	SN74HC112	CD74HC112	PC74HC112	MM74HC112
TC74HC113A	MC74HC113	SN74HC113			MM74HC113
TC74HC123			CD74HC123	PC74HC123	
TC74HC123A	MC74HC123A				MM74HC123A
TC74HC125A	MC74HC125	SN74HC125	CD74HC125	PC74HC125	MM74HC125
TC74HC126A	MC74HC126	SN74HC126	CD74HC126	PC74HC126	MM74HC126
TC74HC131A					
TC74HC132A	MC74HC132		CD74HC132	PC74HC132	MM74HC132
TC74HC133A	MC74HC133	SN74HC133			MM74HC133
TC74HC137A	MC74HC137	SN74HC137	CD74HC137	PC74HC137	MM74HC137

CROSS REFERENCE TABLE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HCT137A		SN74HCT137	CD74HCT137	PC74HCT137	
TC74HC138A	MC74HC138	SN74HC138	CD74HC138	PC74HC138	MM74HC138
TC74HCT138A		SN74HCT138	CD74HCT138	PC74HCT138	MM74HCT138
TC74HC139A	MC74HC139	SN74HC139	CD74HC139	PC74HC139	MM74HC139
TC74HCT139A			CD74HCT139	PC74HCT139	
TC74HC147A	MC74HC147	SN74HC147	CD74HC147	PC74HC147	MM74HC147
TC74HC148A		SN74HC148			
TC74HC151A	MC74HC151	SN74HC151	CD74HC151	PC74HC151	MM74HC151
TC74HC153A	MC74HC153	SN74HC153	CD74HC153	PC74HC153	MM74HC153
TC74HC154A	MC74HC154	SN74HC154	CD74HC154	PC74HC154	MM74HC154
TC74HC155A					MM74HC155
TC74HC157A	MC74HC157	SN74HC157	CD74HC157	PC74HC157	MM74HC157
TC74HCT157A			CD74HCT157	PC74HCT157	MM74HCT157
TC74HC158A	MC74HC158	SN74HC158	CD74HC158	PC74HC158	MM74HC158
TC74HCT158A			CD74HCT158	PC74HCT158	MM74HCT158
TC74HC160A	MC74HC160	SN74HC160	CD74HC160	PC74HC160	MM74HC160
TC74HC161A	MC74HC161	SN74HC161	CD74HC161	PC74HC161	MM74HC161
TC74HC162A	MC74HC162	SN74HC162	CD74HC162	PC74HC162	MM74HC162
TC74HC163A	MC74HC163	SN74HC163	CD74HC163	PC74HC163	MM74HC163
TC74HC164A	MC74HC164	SN74HC164	CD74HC164	PC74HC164	MM74HC164
TC74HCT164A			CD74HCT164	PC74HCT164	MM74HCT164
TC74HC165A	MC74HC165	SN74HC165	CD74HC165	PC74HC165	MM74HC165
TC74HC166A	MC74HC166	SN74HC166	CD74HC166	PC74HC166	
TC74HC173A	MC74HC173	SN74HC173	CD74HC173	PC74HC173	MM74HC173
TC74HC174A	MC74HC174	SN74HC174	CD74HC174	PC74HC174	MM74HC174
TC74HCT174A			CD74HCT174	PC74HCT174	
TC74HC175A	MC74HC175	SN74HC175	CD74HC175	PC74HC175	MM74HC175
TC74HC181A	MC74HC181		CD74HC181	PC74HC181	MM74HC181
TC74HC182A	MC74HC182		CD74HC182	PC74HC182	MM74HC182
TC74HC190A	MC74HC190	SN74HC190	CD74HC190	PC74HC190	MM74HC190
TC74HC191A	MC74HC191	SN74HC191	CD74HC191	PC74HC191	MM74HC191
TC74HC192A	MC74HC192	SN74HC192	CD74HC192	PC74HC192	MM74HC192
TC74HC193A	MC74HC193	SN74HC193	CD74HC193	PC74HC193	MM74HC193
TC74HC194A	MC74HC194	SN74HC194	CD74HC194	PC74HC194	MM74HC194
TC74HC195A	MC74HC195	SN74HC195	CD74HC195	PC74HC195	MM74HC195
TC74HC221			CD74HC221	PC74HC221	
TC74HC221A	MC74HC221A				MM74HC221A
TC74HC237A	MC74HC237	SN74HC237	CD74HC237	PC74HC237	MM74HC237
TC74HC238A		SN74HC238	CD74HC238	PC74HC238	MM74HC238
TC74HC240A	MC74HC240	SN74HC240	CD74HC240	PC74HC240	MM74HC240
TC74HCT240A	MC74HCT240	SN74HCT240	CD74HCT240	PC74HCT240	MM74HCT240
TC74HC241A	MC74HC241	SN74HC241	CD74HC241	PC74HC241	MM74HC241
TC74HCT241A	MC74HCT241	SN74HCT241	CD74HCT241	PC74HCT241	MM74HCT241
TC74HC242A	MC74HC242	SN74HC242	CD74HC242	PC74HC242	MM74HC242
TC74HC243A	MC74HC243	SN74HC243	CD74HC243	PC74HC243	MM74HC243

CROSS REFERENCE TABLE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC244A	MC74HC244	SN74HC244	CD74HC244	PC74HC244	MM74HC244
TC74HCT244A	MC74HCT244	SN74HCT244	CD74HCT244	PC74HCT244	MM74HCT244
TC74HC245A	MC74HC245	SN74HC245	CD74HC245	PC74HC245	MM74HC245
TC74HCT245A	MC74HCT245	SN74HCT245	CD74HCT245	PC74HCT245	MM74HCT245
TC74HC251A	MC74HC251	SN74HC251	CD74HC251	PC74HC251	MM74HC251
TC74HC253A	MC74HC253	SN74HC253	CD74HC253	PC74HC253	MM74HC253
TC74HC257A	MC74HC257	SN74HC257	CD74HC257	PC74HC257	MM74HC257
TC74HCT257A			CD74HCT257	PC74HCT257	MM74HCT257
TC74HC258A		SN74HC258	CD74HC258	PC74HC258	
TC74HCT258A			CD74HCT258	PC74HCT258	
TC74HC259A	MC74HC259	SN74HC259	CD74HC259	PC74HC259	MM74HC259
TC74HC266A	MC74HC266	SN74HC266			MM74HC266
TC74HC273A	MC74HC273	SN74HC273	CD74HC273	PC74HC273	MM74HC273
TC74HCT273A			CD74HCT273	PC74HCT273	MM74HCT273
TC74HC279A					
TC74HC280A	MC74HC280	SN74HC280	CD74HC280	PC74HC280	MM74HC280
TC74HC283A	MC74HC283		CD74HC283	PC74HC283	MM74HC283
TC74HC298A	MC74HC298	SN74HC298			MM74HC298
TC74HC299A	MC74HC299		CD74HC299	PC74HC299	MM74HC299
TC74HC323A					MM74HC323
TC74HC352A		SN74HC352			
TC74HC353A		SN74HC353			
TC74HC354A	MC74HC354	SN74HC354	CD74HC354	PC74HC354	MM74HC354
TC74HC356A	MC74HC356	SN74HC356	CD74HC356	PC74HC356	MM74HC356
TC74HC365A	MC74HC365	SN74HC365	CD74HC365	PC74HC365	MM74HC365
TC74HC366A	MC74HC366	SN74HC366	CD74HC366	PC74HC366	MM74HC366
TC74HC367A	MC74HC367	SN74HC367	CD74HC367	PC74HC367	MM74HC367
TC74HC368A	MC74HC368	SN74HC368	CD74HC368	PC74HC368	MM74HC368
TC74HC373A	MC74HC373	SN74HC373	CD74HC373	PC74HC373	MM74HC373
TC74HCT373A	MC74HCT373	SN74HCT373	CD74HCT373	PC74HCT373	MM74HCT373
TC74HC374A	MC74HC374	SN74HC374	CD74HC374	PC74HC374	MM74HC374
TC74HCT374A	MC74HCT374	SN74HCT374	CD74HCT374	PC74HCT374	MM74HCT374
TC74HC375A		SN74HC375			
TC74HC377A		SN74HC377	CD74HC377	PC74HC377	
TC74HC386A		SN74HC386			
TC74HC390A	MC74HC390	SN74HC390	CD74HC390	PC74HC390	MM74HC390
TC74HC393A	MC74HC393	SN74HC393	CD74HC393	PC74HC393	MM74HC393
TC74HC423			CD74HC423	PC74HC423	
TC74HC423A					MM74HC423A
TC74HC533A	MC74HC533	SN74HC533	CD74HC533	PC74HC533	MM74HC533
TC74HCT533A	MC74HCT533	SN74HCT533	CD74HCT533	PC74HCT533	MM74HCT533
TC74HC534A	MC74HC534	SN74HC534	CD74HC534	PC74HC534	MM74HC534
TC74HCT534A	MC74HCT534	SN74HCT534	CD74HCT534	PC74HCT534	MM74HCT534
TC74HC540A	MC74HC540	SN74HC540	CD74HC540	PC74HC540	MM74HC540
TC74HCT540A	MC74HCT540	SN74HCT540	CD74HCT540	PC74HCT540	MM74HCT540

CROSS REFERENCE TABLE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC541A	MC74HC541	SN74HC541	CD74HC541	PC74HC541	MM74HC541
TC74HCT541A	MC74HCT541	SN74HCT541	CD74HCT541	PC74HCT541	MM74HCT541
TC74HC563A	MC74HC563	SN74HC563	CD74HC563	PC74HC563	MM74HC563
TC74HCT563A		SN74HCT563	CD74HCT563	PC74HCT563	MM74HCT563
TC74HC564A	MC74HC564	SN74HC564	CD74HC564	PC74HC564	MM74HC564
TC74HCT564A		SN74HCT564	CD74HCT564	PC74HCT564	MM74HCT564
TC74HC573A	MC74HC573	SN74HC573	CD74HC573	PC74HC573	MM74HC573
TC74HCT573A		SN74HCT573	CD74HCT573	PC74HCT573	MM74HCT573
TC74HC574	MC74HC574	SN74HC574	CD74HC574	PC74HC574	MM74HC574
TC74HCT574		SN74HCT574	CD74HCT574	PC74HCT574	MM74HCT574
TC74HC590A					MM74HC590
TC74HC592A					MM74HC592
TC74HC593A					MM74HC593
TC74HC595A	MC74HC595				MM74HC595
TC74HC597A	MC74HC597		CD74HC597	PC74HC597	MM74HC597
TC74HC620A	MC74HC620	SN74HC620			
TC74HC623A	MC74HC623	SN74HC623			
TC74HC640A	MC74HC640	SN74HC640	CD74HC640	PC74HC640	MM74HC640
TC74HCT640A	MC74HCT640	SN74HCT640	CD74HCT640	PC74HCT640	MM74HCT640
TC74HC643A	MC74HC643	SN74HC643	CD74HC643	PC74HC643	MM74HC643
TC74HCT643A	MC74HCT643	SN74HCT643	CD74HCT643	PC74HCT643	MM74HCT643
TC74HC646A	MC74HC646	SN74HC646	CD74HC646	PC74HC646	MM74HC646
TC74HCT646A	MC74HCT646	SN74HCT646	CD74HCT646	PC74HCT646	
TC74HC648A	MC74HC648	SN74HC648	CD74HC648	PC74HC648	MM74HC648
TC74HCT648A		SN74HCT648	CD74HCT648	PC74HCT648	
TC74HC651A	MC74HC651	SN74HC651			
TC74HCT651A		SN74HCT651			
TC74HC652A	MC74HC652	SN74HC652			
TC74HCT652A		SN74HCT652			
TC74HC670A	MC74HC670		CD74HC670	PC74HC670	
TC74HC688A	MC74HC688	SN74HC688	CD74HC688	PC74HC688	MM74HC668
TC74HCT688A			CD74HCT688	PC74HCT688	MM74HCT688
TC74HC690A					
TC74HC691A					
TC74HC692A					
TC74HC693A					
TC74HC696A					
TC74HC697A					
TC74HC698A					
TC74HC699A					
TC74HC4002A	MC74HC4002	SN74HC4002	CD74HC4002	PC74HC4002	MM74HC4002
TC74HC4016A	MC74HC4016		CD74HC4016	PC74HC4016	MM74HC4016
TC74HC4017A	MC74HC4017	SN74HC4017	CD74HC4017	PC74HC4017	MM74HC4017
TC74HC4020A	MC74HC4020	SN74HC4020	CD74HC4020	PC74HC4020	MM74HC4020
TC74HC4022A		SN74HC4022			

CROSS REFERENCE TABLE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC4024A	MC74HC4024	SN74HC4024	CD74HC4024	PC74HC4024	MM74HC4024
TC74HC4028A					
TC74HC4040A	MC74HC4040	SN74HC4040	CD74HC4040	PC74HC4040	MM74HC4040
TC74HC4049A	MC74HC4049		CD74HC4049	PC74HC4049	MM74HC4049
TC74HC4050A	MC74HC4050		CD74HC4050	PC74HC4050	MM74HC4050
TC74HC4051A	MC74HC4051		CD74HC4051	PC74HC4051	MM74HC4051
TC74HC4052A	MC74HC4052		CD74HC4052	PC74HC4052	MM74HC4052
TC74HC4053A	MC74HC4053		CD74HC4053	PC74HC4053	MM74HC4053
TC74HC4060A	MC74HC4060	SN74HC4060	CD74HC4060	PC74HC4060	MM74HC4060
TC74HC4066A	MC74HC4066	SN74HC4066	CD74HC4066	PC74HC4066	MM74HC4066
TC74HC4072A					
TC74HC4075A	MC74HC4075	SN74HC4075	CD74HC4075	PC74HC4075	MM74HC4075
TC74HC4078A	MC74HC4078	SN74HC4078A			MM74HC4078
TC74HC4094A			CD74HC4094	PC74HC4094	
TC74HC40102A			CD74HC40102	PC74HC40102	
TC74HC40103A			CD74HC40103	PC74HC40103	
TC74HC40105A			CD74HC40105	PC74HC40105	
TC74HC4316A	MC74HC4316		CD74HC4316	PC74HC4316	MM74HC4316
TC74HC4351A	MC74HC4351		CD74HC4351	PC74HC4351	
TC74HC4352A	MC74HC4352		CD74HC4352	PC74HC4352	
TC74HC4353A	MC74HC4353		CD74HC4353	PC74HC4353	
TC74HC4511A	MC74HC4511		CD74HC4511	PC74HC4511	MM74HC4511
TC74HC4514A	MC74HC4514	SN74HC4514	CD74HC4514	PC74HC4514	MM74HC4514
TC74HC4515A		SN74HC4515	CD74HC4515	PC74HC4515	
TC74HC4518A			CD74HC4518	PC74HC4518	MM74HC4518
TC74HC4520A			CD74HC4520	PC74HC4520	MM74HC4520
TC74HC4538A	MC74HC4538		CD74HC4538	PC74HC4538	MM74HC4538
TC74HC4543A	MC74HC4543		CD74HC4543	PC74HC4543	MM74HC4543
TC74HCT7007A					
TC74HC7240A					
TC74HC7241A					
TC74HC7244A					
TC74HC7266A	MC74HC7266	SN74HC7266	CD74HC7266		
TC74HC7292A					
TC74HC7294A					
TC74HC7640A					
TC74HC7643A					
TC74HC7645A					

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