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Volume 3: Peripheral Drivers, Data Acquisition Systems, Hall-Effect Devices

TEXAS INSTRUMENTS

Linear and Interface Circuits Applications

Volume 3

Peripheral Drivers, Data Acquisition Systems, and Hall Effect Devices

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Preface

This is the third volume in a three-volume series of Linear and Interface Circuit Applications books. To maintain overall continuity in the series, the section numbers in this book follow those in Volume 2. Volume 1 presented information on operational amplifiers, voltage regulators, and timers. Volume 2 provides information on display drivers and data line drivers, receivers, and transceivers. Volume 3 provides information on peripheral drivers, data acquisition circuits, and Hall effect circuits.

The purpose of this series of books is to present linear and interface circuit applications in a manner that will give the reader a basic understanding of the products and provide simple but practical examples for typical applications. Care has been taken to choose illustrations which are of interest, at least by analogy, to a wide class of readers. This material is written for not only the design engineer but also for engineering managers, engineering technicians, system designers, and marketing or sales people with some technical background. The authors have attempted to avoid lengthy mathematical analyses for technical elegance, so that the important points may be clearly emphasized and not obscured by distracting derivations. In cases where a rigorous derivation has been omitted, an attempt has been made to state the results precisely and to emphasize limitations that are practically significant.

To facilitate their use, the sections have been made basically independent. The primary goal of the books is to assist the user in selecting the proper device for a particular application. To accomplish this, key features of devices are presented along with discussions of device or system theory and requirements.

Potential uses of the devices are demonstrated in circuit applications. These applications are not intended to be a how-to for specific circuits but to be examples of how the device might be used to solve your specific design requirements. In each case, a data book or data sheet should be referred to for complete device characteristics and operating limits. The circuit examples selected for this book have accrued from numerous customer inquiries and related laboratory simulations.

This series of books has been written primarily by two members of the Linear Applications Staff. They would like to express their appreciation for the helpful inputs and assistance from members of the Linear Applications Lab, Product Engineering Staff, and Field Application Engineering.

Section 10

Peripheral Drivers

Peripheral drivers are general-purpose integrated circuits that can be used to interface between TTL, MOS, and CMOS logic levels and higher voltage, higher current components. Higher voltage and higher current components include lamps, relays, solenoids, data transmission lines, and motors (Figure 10-1).

requiring additional drive power. These peripheral drivers usually include output transistors to provide the required drive capability, preceded by logic level shifting circuitry. Level shifting is accomplished by integrated resistors and diodes or logic gates. Figure 10-2 illustrates the two basic configurations of peripheral drivers. One uses resistor and/or

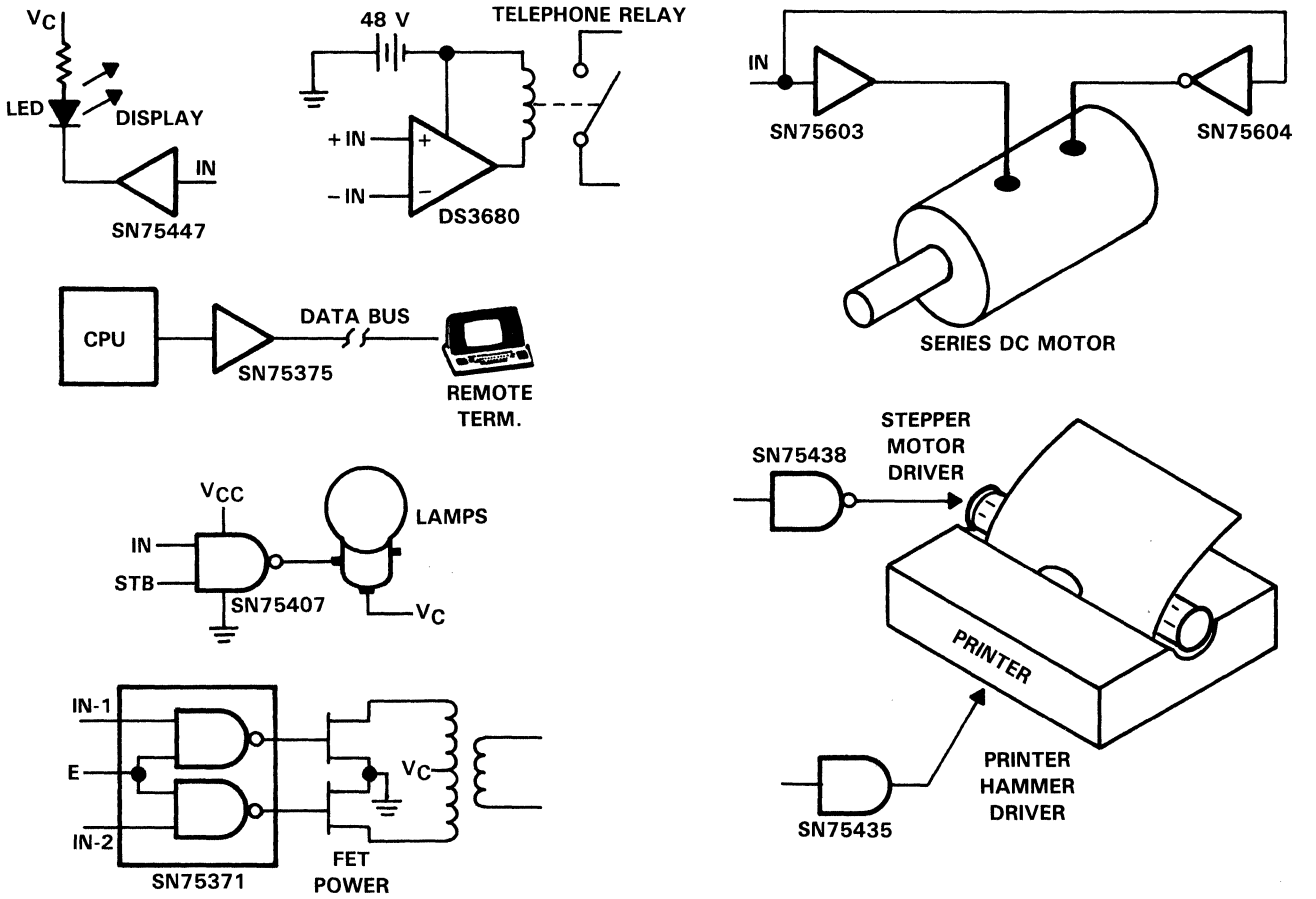


Figure 10-1. Typical Uses for Peripheral Drivers

DEVICE CONSIDERATIONS AND PRODUCT DESCRIPTIONS

BASIC CONFIGURATIONS

In the mid 1960s, integrated circuit logic gates were combined with a variety of discrete small signal transistors and power transistors to provide the desired interfacing. Integrated circuit devices were developed to allow direct, single IC interfacing from logic levels to components

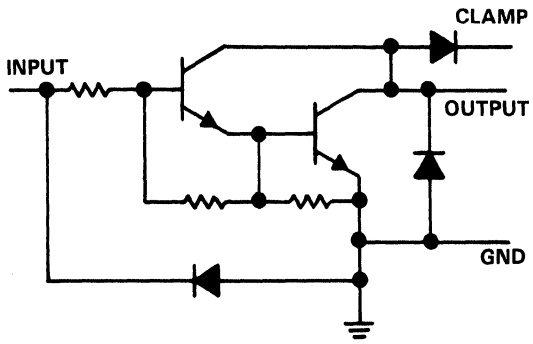
diode level shifting [Figure 10-2(a)], and the other uses logic gate level shifting [Figure 10-2(b)].

TYPICAL REQUIREMENTS

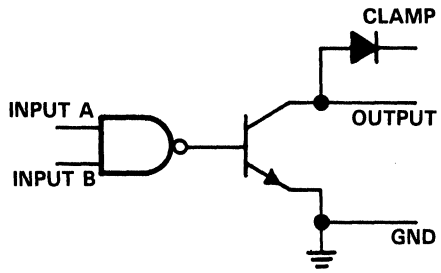
Power

Peripheral drivers are used in situations which require them to dissipate a significant amount of power. As a result, most IC peripheral drivers are designed to handle at least 1 W. Packages with copper lead frames are often used to

improve power handling capability. The small dual-in-line 8-pin package with a copper lead frame will typically handle over 1.4 W at 25 °C. The 14- and 16-pin packages with copper lead frames are rated at 2 W or greater.



(a) RESISTOR/DIODE INPUT



(b) GATE INPUT

Figure 10-2. Basic Peripheral Driver Input Configurations

Voltage

Voltage capability ranges from a minimum of 15 V to 100 V. Care must be exercised in the selection of drivers for switching applications. The switching voltage output limits are generally less than the maximum dc standoff voltage [$V_{(BR)CER}$]. For example, a typical peripheral driver with a standoff voltage rating of 30 V may not be suitable for use as a 24-V relay driver, even if an output clamp diode is used. The high level output voltage after switching (V_{OH}) is typically 20 V for this device. The output voltage swing of 24 V or 25 V would result in secondary breakdown and device latch-up. This is a destructive condition which could result in device failure. The correct device for this application would have a V_{OH} rating of 30 V. Gate controlled input devices require a 5-V supply in addition to any higher level supply required for the output circuit.

Current

Peripheral drivers are designed to operate at output current levels of 100 mA to 2 A. As with output voltage, device output current selection should be done with care. Most devices will have a continuous output current rating and a peak current rating. Peak current ratings are specified for a maximum on time of 10 ms and a duty cycle of 50% or less. NOTE: The peak current level of integrated circuit drivers should not be exceeded, no matter how short the time or how low the duty cycle. Although average power dissipation may be within limits if the on times and duty cycles are very short, chip surface metal migration may occur with any current above the rated peak level. Metal migration results in destruction of the chip surface metal. This is associated with the output emitter contacts, and eventually causes device failure. For example, short current spikes associated with charging a capacitive load could seem to have no immediate effect on the device. However, if the peak current level is exceeded for even a short time, a small amount of deterioration occurs and the device will exhibit long-term failure.

Speed

Peripheral drivers can be used as switches and are therefore operating in a dc or very low frequency mode. Other applications, such as memory clock drivers require speeds as high as 10 MHz. At low or high data rates or dc operation, the device must never exceed its voltage, current or power limits.

High-speed operation can, in some applications, result in excessive power dissipation. High-speed power dissipation can (and should) be limited to improve operating reliability. Turn-on transients are one form of excessive power that can be controlled to some extent. Figure 10-3 illustrates the effects of transients on power dissipation as frequencies are increased.

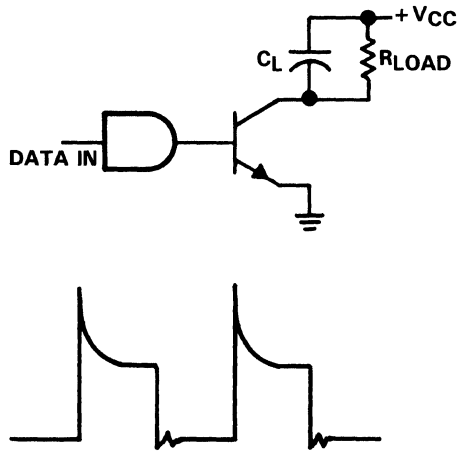
Logic

Generally these devices are used to interface between logic level signals and circuits requiring more drive power. Most peripheral driver inputs are compatible with TTL voltage levels. The input resistance of some devices is high allowing compatibility with low level CMOS, MOS, and low power Schottky TTL, as well as standard TTL.

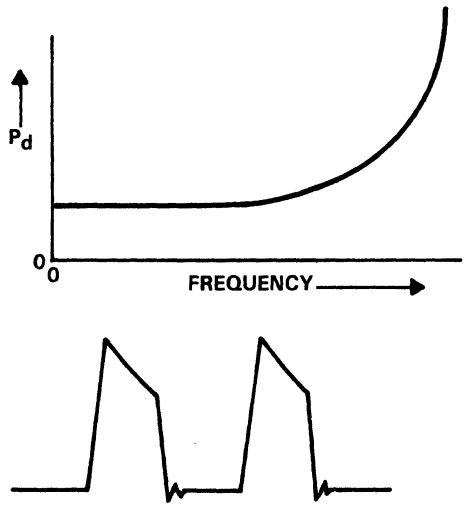
PERIPHERAL DRIVER DEVICES

A wide variety of peripheral drivers is available for today's design engineer. The first monolithic IC peripheral driver, the SN75450B which was introduced by Texas Instruments in 1968 (Figure 10-4), was very basic and versatile, allowing many application options. This versatility has accounted for its continued popularity. The SN75450B's schematic and logic symbol diagrams are illustrated in Figures 10-5 and 10-6. Note that the output transistor's emitter, collector, and base leads are pinned out separately to allow for various methods of interconnections.

Key design features of the SN75450B include the ability to switch load currents of 300 mA. It has a dc off-state transistor collector output voltage capability of 30 V and can switch off 300 mA with inductive loads while operating from collector supply voltages of up to 20 V. The SN75450B also features fast (less than 30 ns) switching speeds for use in high speed logic interfacing applications. As shown in Figure 10-5, its TTL compatible inputs are diode clamped for protection from negative voltage transients.



(a) PEAK SURGE ADDS 80% TO AVERAGE DC POWER



(b) PEAK SURGE ADDS 12% TO AVERAGE DC POWER

Figure 10-3. Transient Effects on Power Dissipation

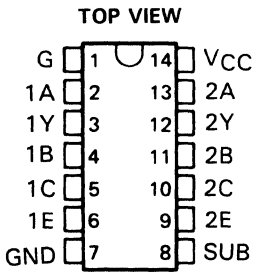
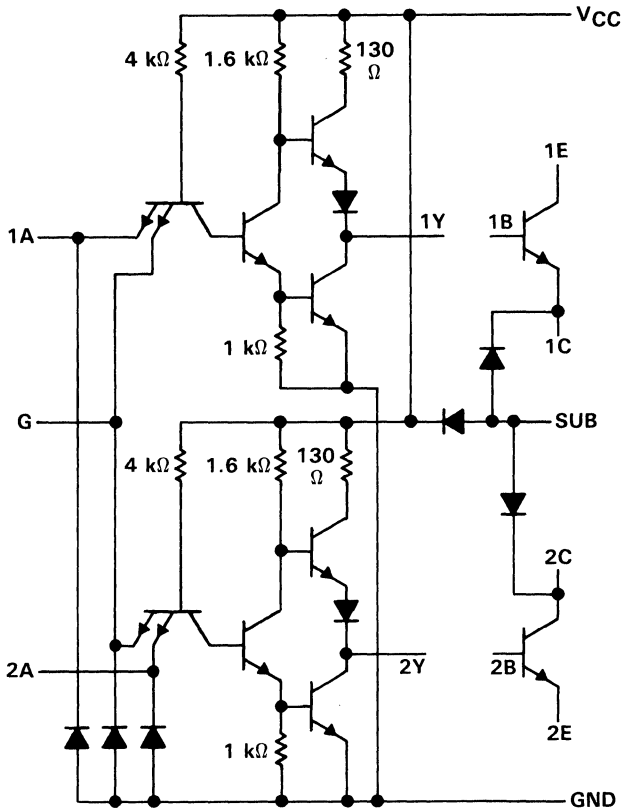


Figure 10-4. SN75450B Peripheral Driver

It was noted that in most of the applications using the SN75450B device, the emitters were tied together and grounded. Also the gate outputs were tied to the transistor base inputs. Implementing this configuration yielded the next device in this series — the SN75451B. Other devices with different logic functions, but basically the same operating characteristics, led to the series of drivers summarized in Table 10-1.



Resistor values shown are nominal.

Figure 10-5. SN75450B Schematic

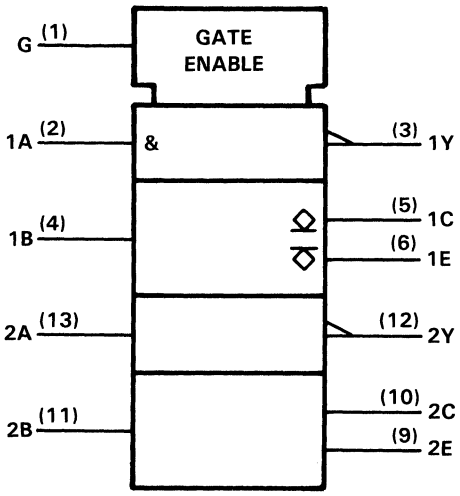


Figure 10-6. SN75450B Logic Symbol

Table 10-1. Summary of Series 55450B/75450B

DEVICE	CIRCUIT LOGIC	PACKAGES
SN75450B	AND	J,N
SN75451B	AND	JG,P,D
SN75452B	NAND	JG,P,D
SN75453B	OR	JG,P,D
SN75454B	NOR	JG,P,D

SN75431, '461 and '471 Series

The need for different voltages, currents and speeds has resulted in the development of several families of peripheral drivers. Families with the same block diagram and basic function as the '451 series include the SN75431, SN75461, and SN75471 series. Figures 10-7 and 10-8 list the basic schematics, logic symbols, and package pinouts for these four families.

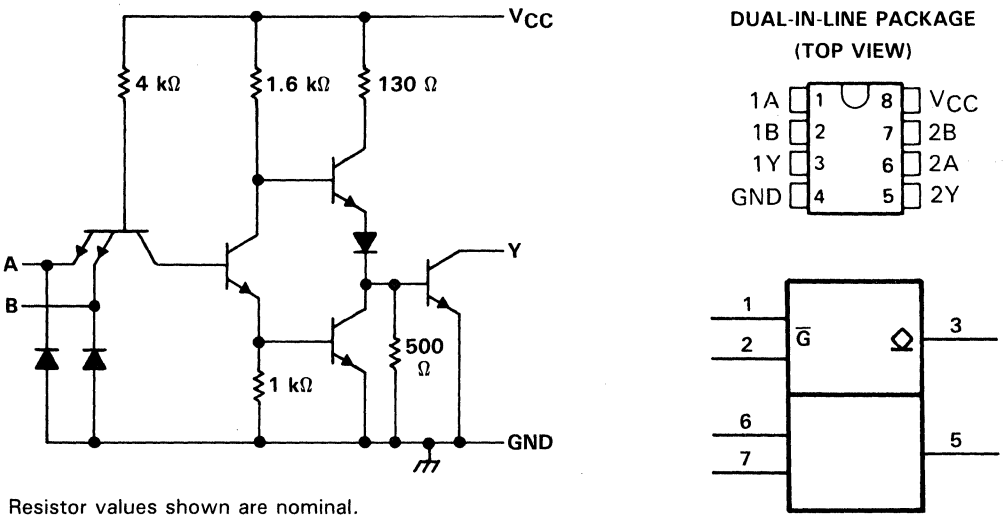
Features and comparisons of the SN75431, 451, 461, and 471 families are listed in Table 10-2.

Table 10-2. SN75431 Series Device Features

FAMILY	OFFSTATE VOLTAGE (V)	SWITCH LOAD VOLTAGE (V)	OUTPUT CURRENT (mA)	TYPICAL t_{pd} (ns)
SN75431-434	15	15	300	15
SN75451-454	30	20	300	20
SN75461-464	40	30	300	35
SN75471-474	70	55	300	35

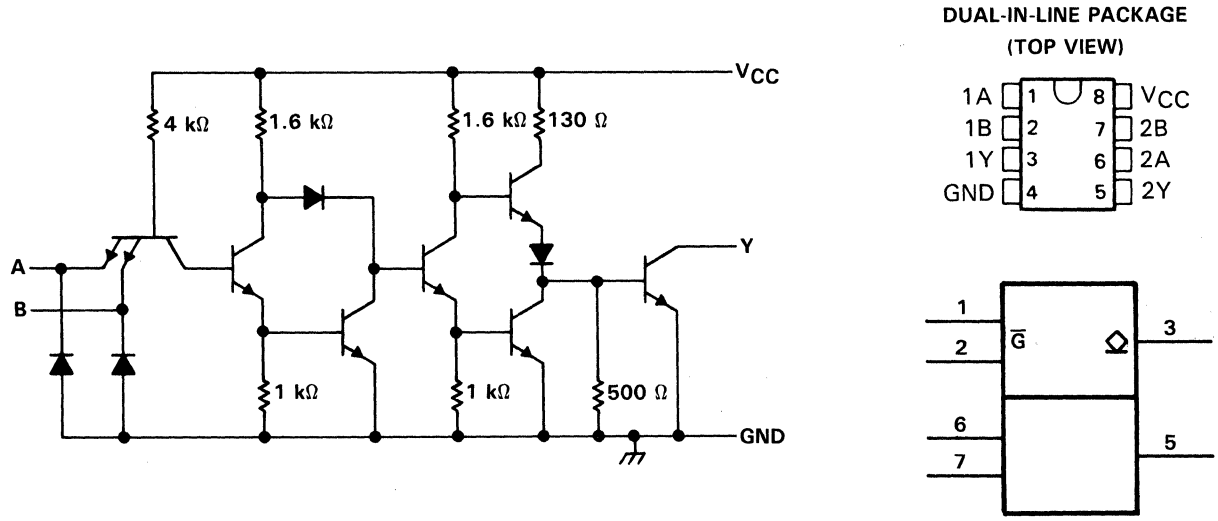
SN75446 and SN75476 Series

The SN75446 and SN75476 series are also dual drivers but have additional features illustrated in Figure 10-9. Both the SN75446 series and the SN75476 series have PNP input transistors, resulting in compatibility with TTL, MOS, and low level CMOS logic. Built-in output clamp diodes allow clamping of inductive loads without external diodes. The 446 series provides 350 mA continuous output and 70-V standoff with 50-V inductive switching capability. The 476 series provides 300 mA continuous output current with 70-V standoff and 55-V inductive switching capability. These devices are especially suited for driving inductive loads such as relays, solenoids, printer hammers, and motors. Figure 10-10 shows the package and function similarities between these devices and their interchangeability.



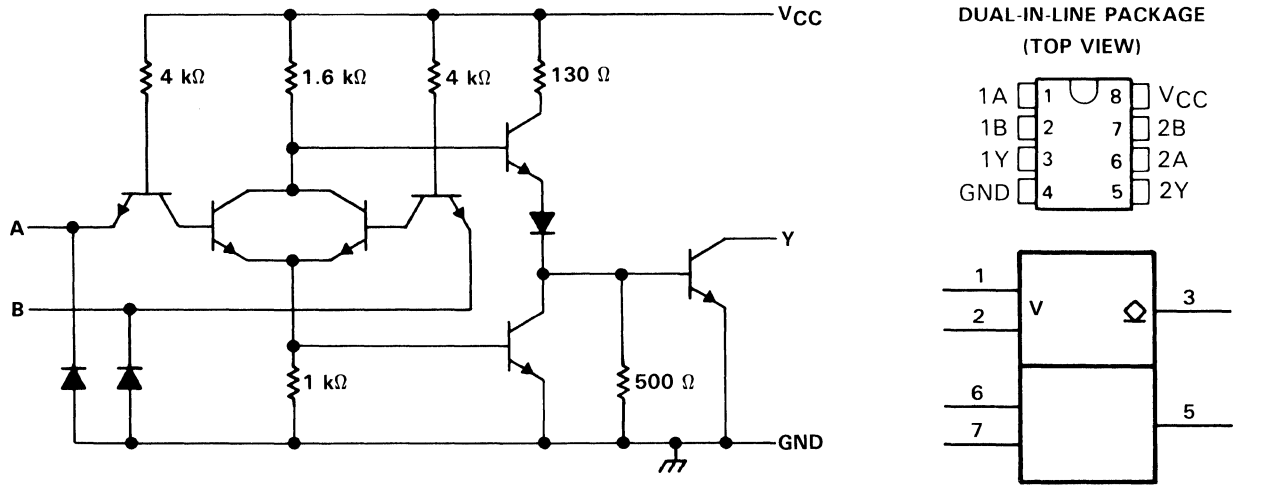
Resistor values shown are nominal.

(a) SN55/75431, SN55/75451, SN55/75461, SN55/75471



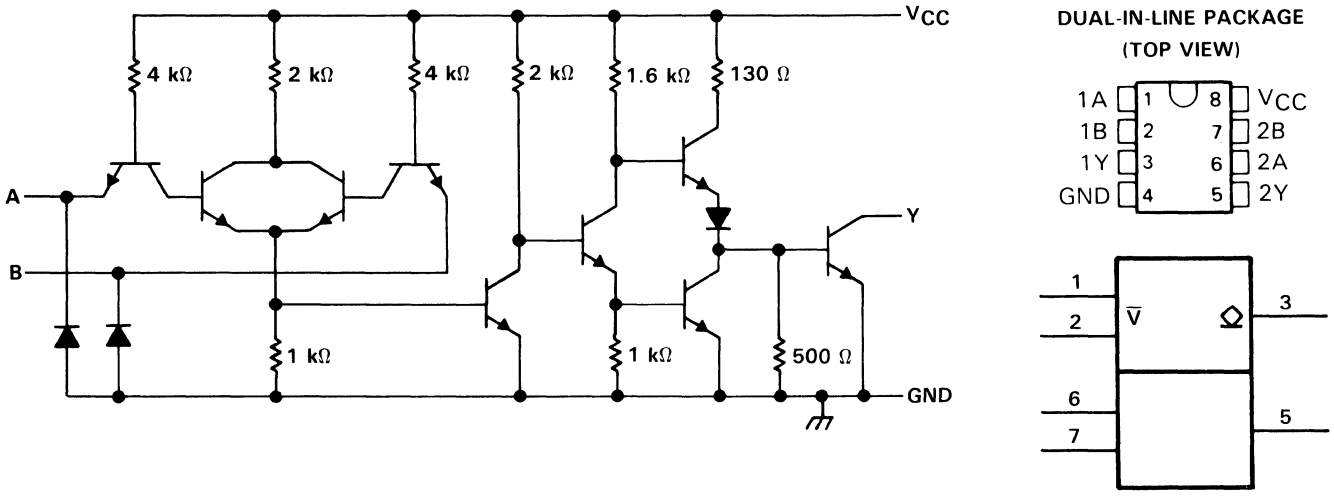
(b) SN55/75432, SN55/75452, SN55/75462, SN55/75472

Figure 10-7. SN75431/451/461 and 471 Series (AND, NAND) Schematics and Diagrams



Resistor values shown are nominal.

(a) SN55/75433, SN55/75453, SN55/75463, SN55/75473



(b) SN55/75434, SN55/75454, SN55/75464, SN55/75474

Figure 10-8. SN75431/451/461 and 471 Series (OR, NOR) Schematics and Diagrams

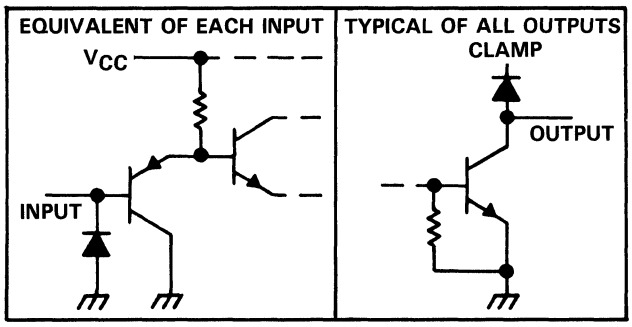


Figure 10-9. Schematics of Device Inputs and Outputs

SN75436, SN75437A, and SN75438

The SN75436, SN75437A and SN75438 are quad, gate controlled, peripheral drivers. They are designed for driving loads requiring relatively high power (15 to 35 W). Each device features four open-collector output drivers with common enables. These devices are designed for use as relay drivers, printer hammer or other types of solenoid drivers, lamp drivers, motor drivers, data line drivers, and memory drivers. The basic device schematic diagrams, Figure 10-11, show some of the special features of this series. PNP transistors provide high-impedance inputs for TTL and CMOS compatibility. Low power logic control circuitry results in less than 26 mW standby power. Open-collector output transistors provide low resistance saturated outputs

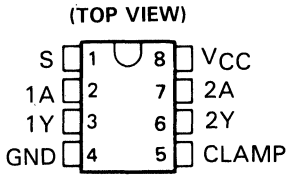
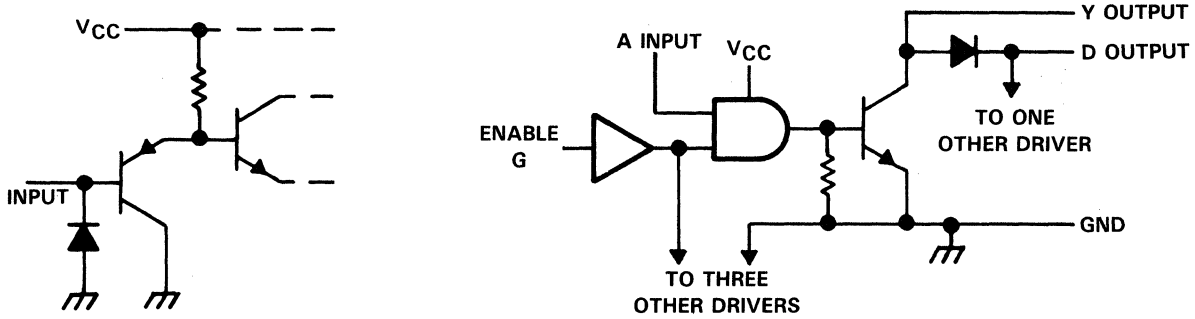


Figure 10-10. SN75446 and SN75476 Series Package Pinouts



(a) EQUIVALENT OF EACH INPUT

(b) FUNCTIONAL BLOCK DIAGRAM

Figure 10-11. Basic Device Schematics

resulting in low V_{SAT} levels. The outputs of these devices do not have spurious transients during power-up or power-down sequencing. The device package, Figure 10-12, provides four heat sink pins to help conduct heat from the device. As a result of this, and their copper leads, the SN75436, SN75437A and SN75438 packages are rated for 2 W continuous power dissipation at 25 °C or less (free-air operating temperature). Inputs and outputs are conveniently located on opposite sides of the package for easy PC-board layout and assembly. Table 10-3 compares the maximum output current, output saturation voltage, and switching voltage for these three devices.

(TOP VIEW)

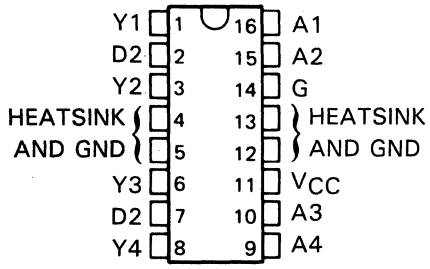


Figure 10-12. Package Pinout

Table 10-3. Device Selection Guide

Feature	436	437A	438
Output current	500 mA	500 mA	1000 mA
Maximum V_{SAT}	0.5 V	0.5 V	1.0 V
Max switching voltage	50 V	35 V	35 V

SN75435 Quad Driver

The SN75435 consists of four peripheral drivers, each with up to 20 W output drive capability. It features (Figures 10-13 and 10-14) four open-collector drivers with a common enable input that, when taken low, disables all four outputs (Table 10-4). Output on resistance is less than 1 Ω at an output current of 500 mA. The standard 2-W DIP (Figure 10-13) is used for this device. Output clamp diodes for transient protection are built in. The SN75435 is also free of spurious transients during power-up and power-down sequencing. Device standby power is less than 53 mW allowing cool operation and good long-term reliability.

One unique feature is that each driver output is protected against load shorts with its own latching over-current shutdown circuitry. The output will be turned off whenever a load short is detected. A short on one output does not affect the other three drivers. The latch for shutdown will hold the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the over-current shutdown to allow for a load capacitance of 500 μF at 35 V. Figure 10-15 illustrates the recommended maximum supply voltage versus load capacitance.

Table 10-4. SN75435 Function Table

INPUTS					OUTPUTS			
1A	2A	3A	4A	G	1Y	2Y	3Y	4Y
L	L	L	L	X	H	H	H	H
X	X	X	X	L	H	H	H	H
H	L	L	L	H	L	H	H	H
L	H	L	L	H	H	L	H	H
L	L	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L
H	H	H	H	H	L	L	L	L

(TOP VIEW)

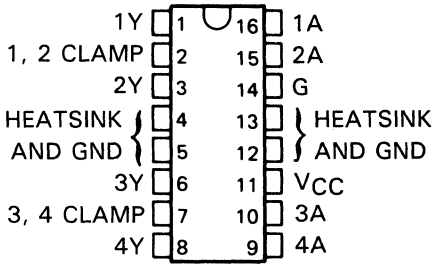


Figure 10-13. SN75435 Package Pinout

The SN75435, Figure 10-16, has high-impedance PNP inputs to provide both TTL and low level CMOS compatibility. Inputs are also diode clamped for negative voltage input transient protection. Although very well suited for driving solenoids, relays, memory systems, and LED

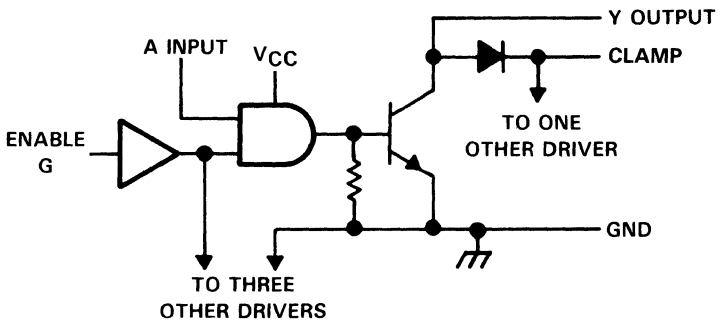


Figure 10-14. SN75435 Basic Logic Diagram

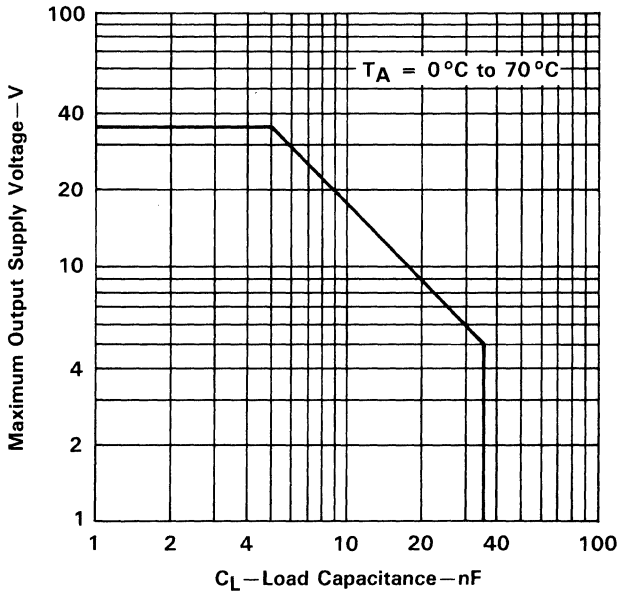


Figure 10-15. Recommended Maximum Supply Voltage vs Load Capacitance

circuits, this device is particularly well suited for driving lamps and motors.

SN75440 Quad Peripheral Driver

The SN75440 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The package Figure 10-17 allows easy heat sinking and will provide 2-W power handling capability at 25 °C. The device standby power is only 21 mW. Each device has four noninverting open-collector outputs with 600 mA sink capability and will switch inductive loads with a supply voltage of 35 V. The SN75440 also features an enable input control on pin 14, Figure 10-17, for enabling or disabling all four outputs. The open-collector outputs, Figure 10-18, are diode protected for transient protection and have a low on-state resistance of less than 1.5 Ω. The outputs are free from spurious transitions (glitching) during power-up or power-down sequencing.

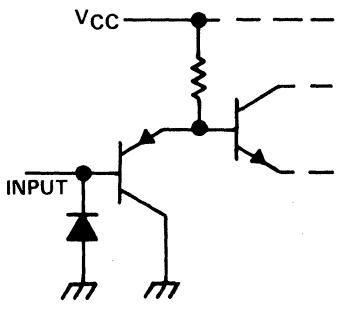


Figure 10-16. SN75435 Equivalent Schematic of Each Input

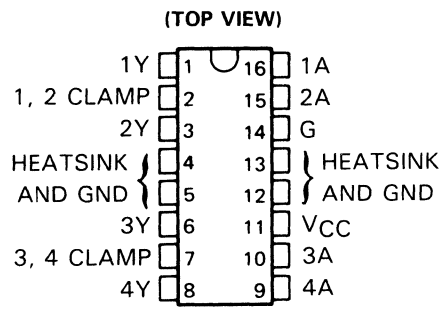


Figure 10-17. SN75440 Package Pinout

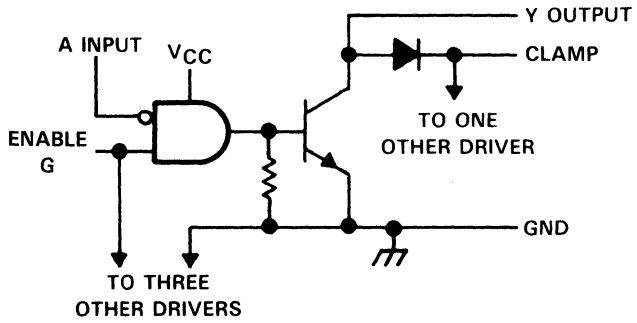


Figure 10-18. SN75440 Logic Diagram (Each Driver)

PNP inputs, Figure 10-19, have low level input currents of less than 10 μA. Functional relationships between the input and output logic functions are given in Table 10-5. Applications include driving relays, lamps, solenoids, motors, LEDs, data transmission lines, printer hammers, and other systems with high drive power requirements.

SN75603, SN75604, and SN75605

The SN75603, SN75604, and SN75605 are power peripherals with three-state outputs having the capability to

Table 10-5. SN75440 Logic Functions

INPUTS		OUTPUT
A	G	Y
L	H	L
H	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

sink or source currents up to 2 A while switching bidirectional loads at voltages of 8 V to 40 V. They come in a straight KH, or formed KV, 5-lead power package illustrated in Figure 10-20. They are rated at 6.25 W at or below 125 °C. The devices have built-in input and output transient diodes (Figure 10-21) and thermal shutdown protection. Table 10-6 provides the input-output functions for all three devices. Note that the SN75603 and SN75604 are both in their high impedance output state if their enable input is low. The SN75605 uses an exclusive-OR input control and if either the enable or the direction control inputs are low the output is in the high impedance state.

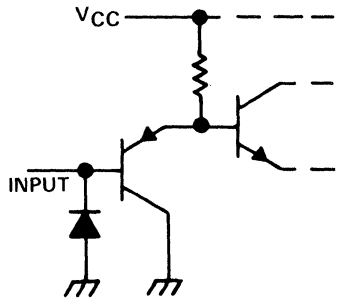


Figure 10-19. SN75440 Equivalent Schematic of Each Input

Table 10-6. SN75603/604 and 605 Function Table

INPUTS		OUTPUT		
EN	DIR	SN75603	SN75604	SN75605
L	L	Z	Z	L
L	H	Z	Z	Z
H	L	L	H	Z
H	H	H	L	H

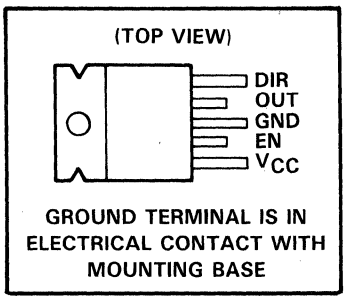


Figure 10-20. SN75603/604 and 605 Package Pinout

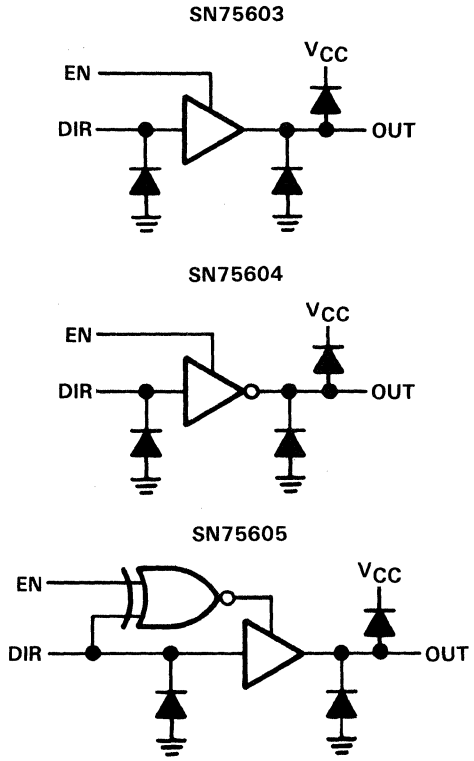


Figure 10-21. SN75603/604 and 605 Logic Diagrams

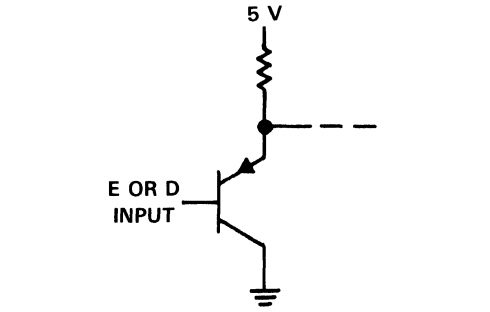
The equivalent input and output schematics are shown in Figure 10-22. PNP input transistors provide high input impedance with both TTL and CMOS compatibility. Internal propagation delays are such that simultaneous conduction of sink and source outputs cannot occur. These devices are especially suited for driving bidirectional dc and stepper motors as well as reversible solenoids and relays.

The SN75603 and SN75604 are designed to be used together as complementary half-H drivers. Their direction controls are complementary allowing the pair to function as full-H drivers with the direction control function implemented by a single logic control line.

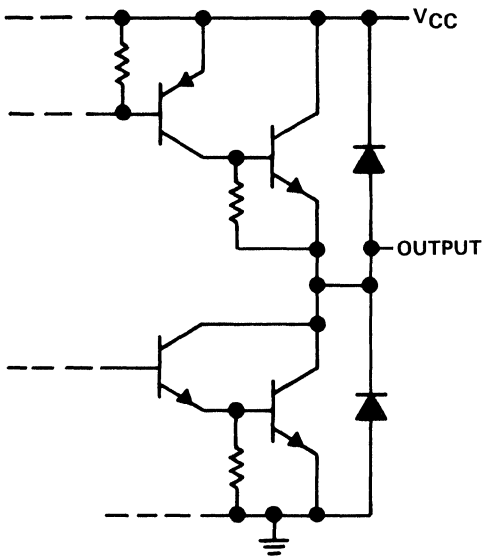
The SN75605 (a functional equivalent to the Sprague UDN2949) provides a high impedance output when either the enable or the direction control is low. Note: If both of the inputs are low at the same time, the output will be in the low state. If both inputs are high, then the output will be high.

SN75372 Dual and SN75374 Quad Power FET Drivers

The SN75372 and SN75374 are designed to drive capacitive type loads at relatively high data rates. Primary uses include driving power FET devices in switching applications and interfacing between TTL and MOS or CMOS. Their totem-pole outputs provide high speed sink and source capability ideally suited to driving the capacitive input characteristics of power FET devices. The SN75372 is a dual driver with TTL compatible inputs and totem-pole outputs that can source, from a V_{CC2} supply level of up to 24 V and sink currents of 100 mA minimum. Even when



INPUT SCHEMATIC



OUTPUT SCHEMATIC

Figure 10-22. Equivalent SN75603/604 and 605 Input and Output Schematics

operating into a 390-pF load device propagation delays are typically less than 35 ns with transition times accounting for 25 ns of that. The result is a very adequate speed for driving power FETs. Figures 10-23 and 10-24 show the basic circuit configurations for the SN75372 and SN75374. Both devices have input and output transient protection diodes. These devices have transient overdrive protection to minimize power dissipation. The typical standby power is 22 mW for the dual SN75372 and 38 mW for the quad SN75374.

The dual SN75372 comes in the 8-pin DIP package, Figure 10-25, and has a common enable. The quad SN75374 comes in a 16 pin, Figure 10-26, and has 2 enables for each pair of drivers. An additional feature of the SN75374, shown in both Figures 10-24 and 10-26, is the availability of the pre-driver supply rail (V_{CC3} on pin 9). With V_{CC3} at 3 to 4 V above the value of V_{CC2}, it is possible to drive the output level very close to the V_{CC2} rail.

When driving capacitive loads at relatively high data rates, the package power dissipation will become significant and it is desirable to know what to expect. Figures 10-27 and 10-28 illustrate the total package power dissipation that may be expected versus operating frequency with several different capacitive loads for the SN75372 and SN75374.

DS3680 Quad Telephone Relay Driver

The DS3680 quad relay driver is a monolithic integrated circuit designed to interface from TTL to telephone relay systems or other −48 V systems. It is capable of sourcing 50 mA from standard −52 V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common- mode input range of ±20 volts referred to battery ground. Each driver in the package has common-mode input

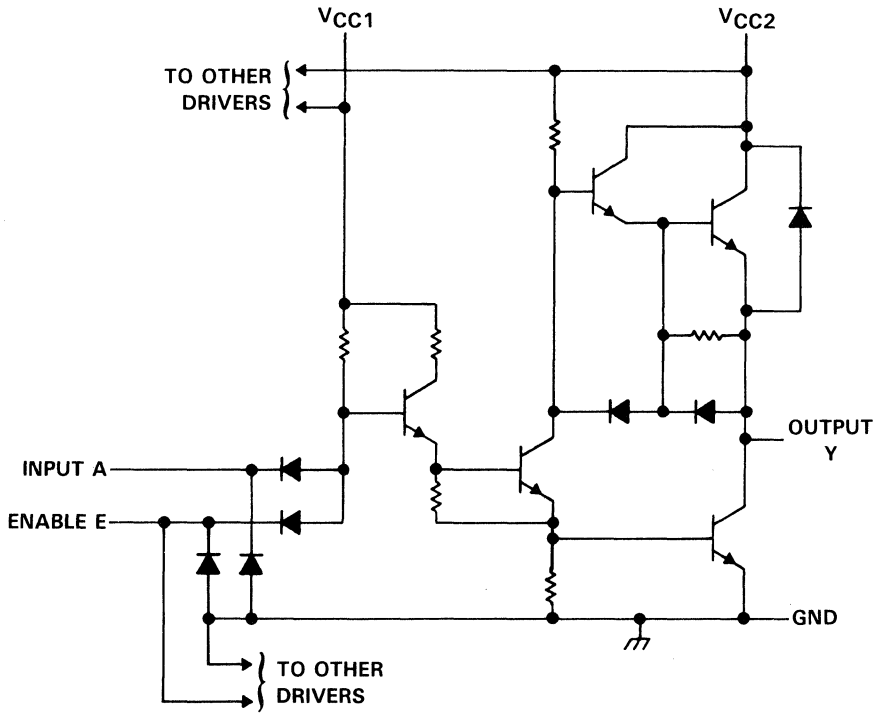


Figure 10-23. SN75372 Schematic (Each Driver)

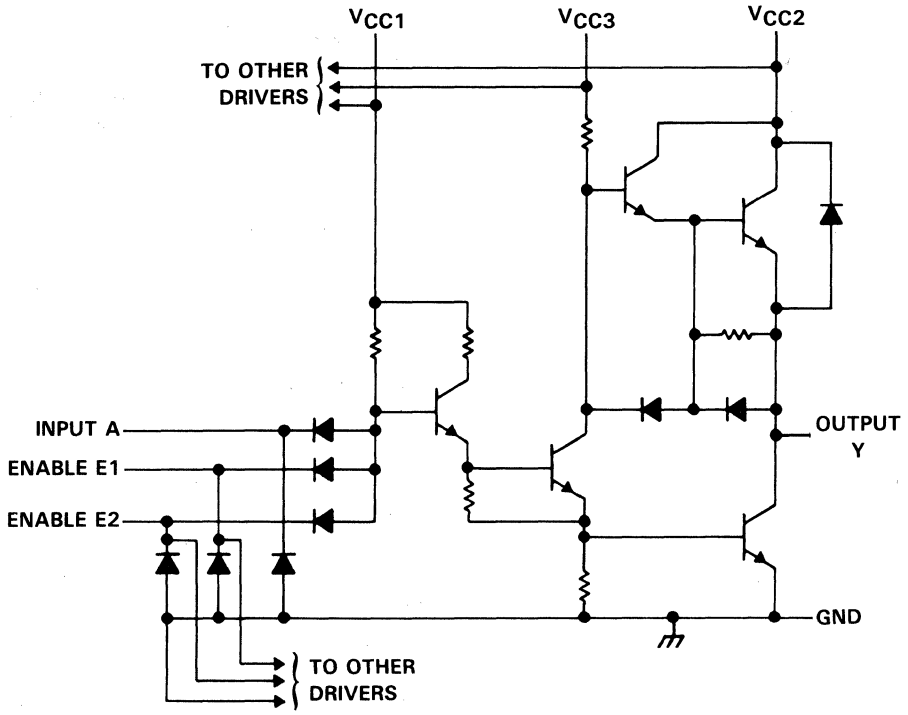


Figure 10-24. SN75374 Schematic (Each Driver)

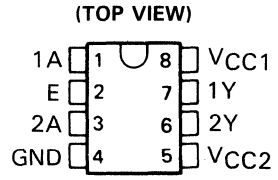


Figure 10-25. SN75372 Package Pinout

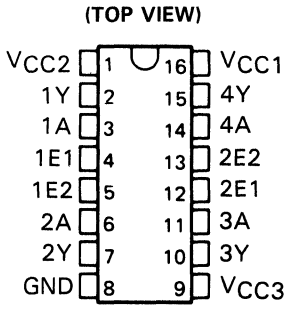


Figure 10-26. SN75374 Package Pinout

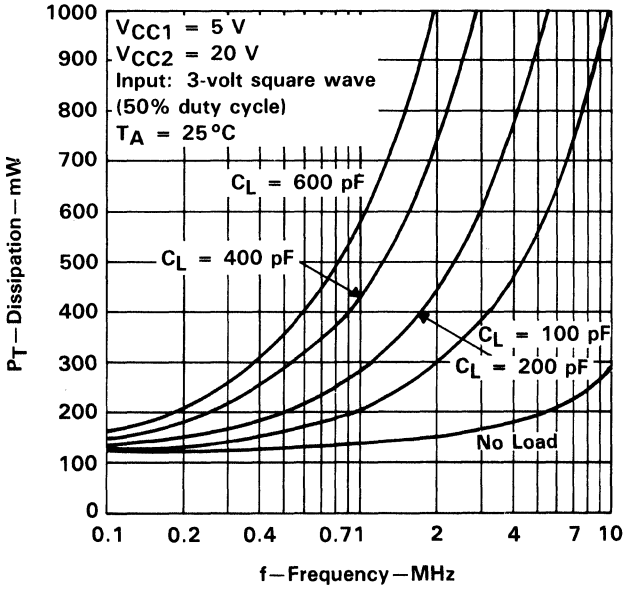


Figure 10-27. Total Dissipation Both 372 Drivers vs Frequency

voltage independent of the other drivers. High input impedance with low input current (typically less than 100 μA) results in minimum loading of the driving circuit. Built-in driver output clamp diodes eliminate the need for external networks to limit high voltage kickback levels present when switching inductive loads. A fail-safe feature incorporated in the DS3680 ensures that if either input is open, the driver output will be off. Figures 10-29 and 10-30 illustrate each driver's logic symbol and schematic diagram respectively. Figure 10-31 shows the convenience of the package pinout with inputs on one side and outputs on the other. Ground is located on a corner pin to implement easy board layouts.

Some peripheral drivers are basically Darlington transistor arrays designed to have logic compatible inputs. They are often used in high current applications where the control logic is provided externally. The following devices are of this type.

SN75064/ULN2064 Series Quad Peripheral Drivers

The SN75064, SN75065, SN75066, SN75067, ULN2064, ULN2065, ULN2066, and ULN2067 are quad high current, high voltage Darlington switches. Each device

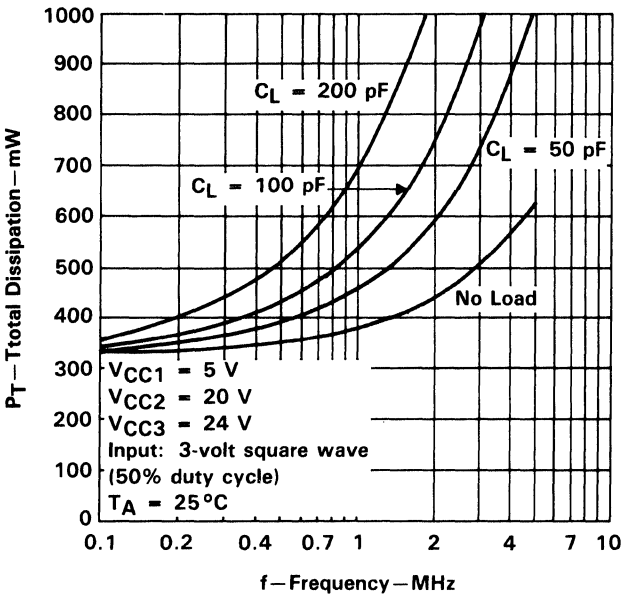


Figure 10-28. Total Dissipation All 374 Drivers vs Frequency

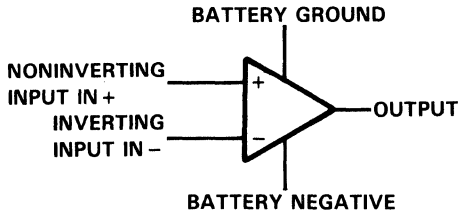


Figure 10-29. DS3680 Logic Diagram (Each Driver)

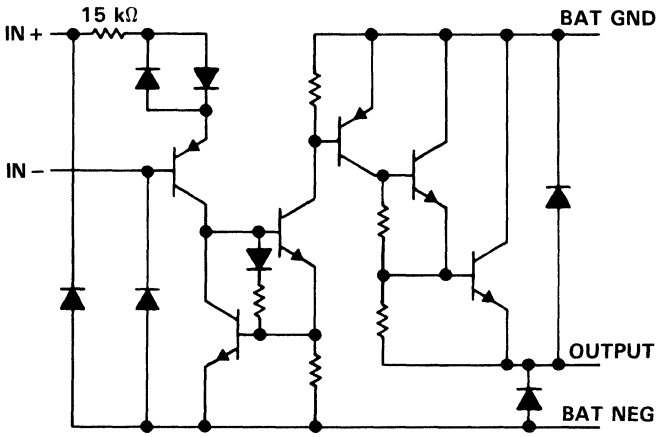


Figure 10-30. Schematic Diagram (Each Driver)

has four Darlington transistor drivers with common-cathode clamp diodes for switching inductive loads (Figure 10-32). Each of the drivers has 0.5 A output current capability, and their inputs and outputs may be paralleled for even higher current handling. Connected as common emitter circuits, these devices provide sink current drive for switching a variety of applications including relays, printer hammers, lamps, display circuits, memory circuits, and data transmission lines. The NE packages (Figure 10-32) are rated at 2 W. Output loads may be operated from voltages up to 50 or 80 V, depending on the device type.

The SN75064, ULN2064, SN75065, and ULN2065 are intended for use with TTL and 5-V MOS logic. The SN74066, ULN2066, SN75067 and ULN2067 are intended for use with PMOS and higher voltage CMOS logic. The SN75 series devices have a slightly higher maximum $V_{CE(sat)}$ specification and feature economical pricing. The ULN series devices have slightly lower maximum $V_{CE(sat)}$ and are recommended where output low level voltages are critical.

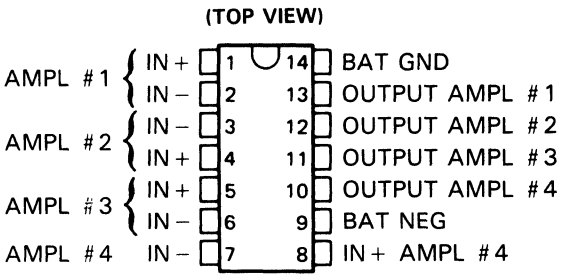
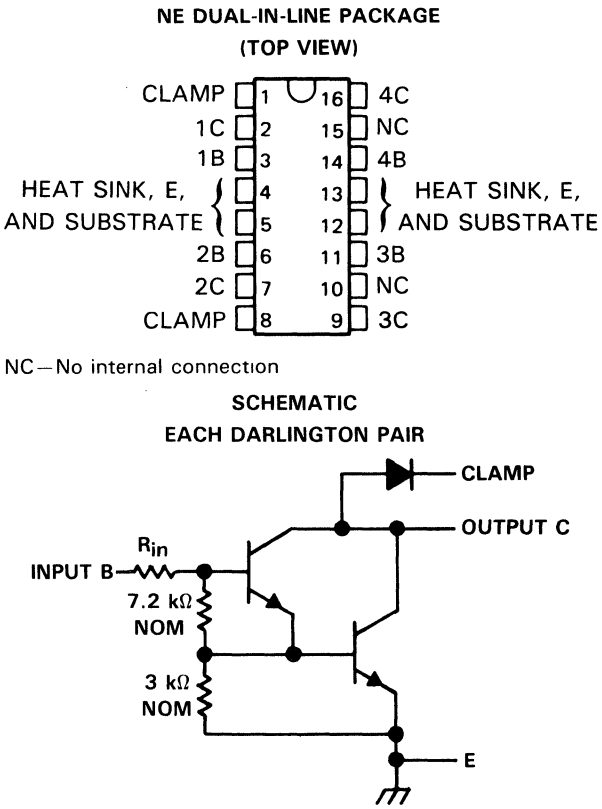


Figure 10-31. DS3680 Package Pinout



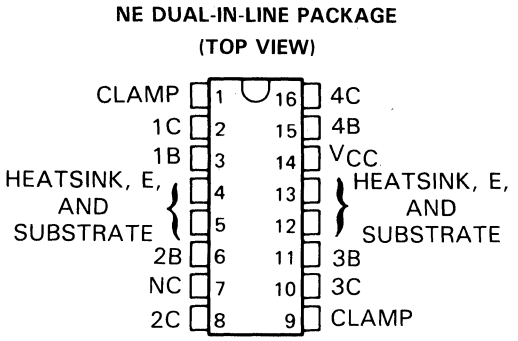
SN75064, SN75065 R_{in} = 350 Ω NOM
ULN2064B, ULN2065B

SN75066, SN75067 R_{in} = 3 kΩ NOM
ULN2066B, ULN2067B

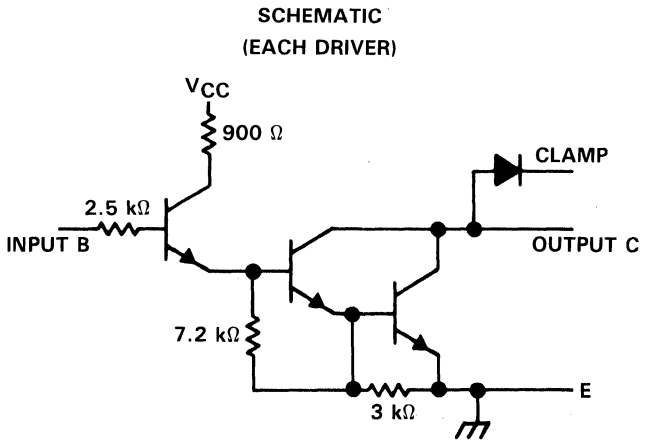
Figure 10-32. SN75064 Series and ULN2064 Series Package Pinout and Schematic

SN75068/ULN2068 and SN75069/ULN2069 Quad Darlington Switches

The SN75068/ULN2068 and SN75069/ULN2069 are quad high voltage, high current Darlington drivers (Figure 10-33). Their outputs have common cathode clamp diodes for switching inductive loads. A third transistor at the input acts as a preamplifier providing high current gain and input compatibility with low power TTL and 5-V CMOS signals. With a maximum input current of only 250 μA at a V_{in} of 2.4 V, these devices may be operated directly from low power sources such as CMOS microprocessors or computers. Their outputs can sink up to 1.5 A and switch voltages of up to 50 V for the 068 devices and 80 V with the 069 devices. The recommended V_{CC} for the preamp is 5 V.



NC—No internal connection



Resistor values shown are nominal.

Figure 10-33. SN75068, SN75069, ULN2068, and ULN2069 Package Pinout and Schematic

SN75074/ULN2074 and SN75075/ULN2075 Quad Darlington Sink or Source Drivers

The SN75074/ULN2074 and SN75075/ ULN2075 are quad, high current, high voltage Darlington transistor switches (Figure 10-34). They feature output voltage operation up to 80 V and output current capabilities of up to 1.5 A. These devices are unique in that they feature uncommitted collectors and emitters allowing sink or source applications. Inputs with respect to the emitters are compatible with TTL logic levels. These devices are particularly useful in H-drive applications because of the ability to perform both sink and source functions.

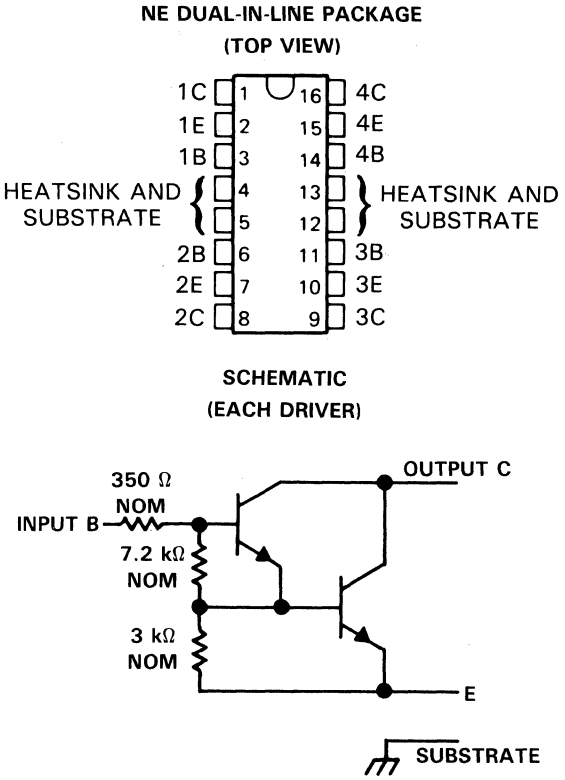


Figure 10-34. SN75074, SN75075, ULN2074, and ULN2075 Package Pinout and Schematic

SN75465 and ULN2001A Series Seven Channel Darlington Transistor Arrays

The SN75465 series and the ULN2001A series are high voltage, high current Darlington npn transistor arrays with common cathode clamp diodes for switching inductive loads (Figure 10-36). Each Darlington pair has a collector current rating of 500 mA. Darlington drivers may also be paralleled for higher current capability when using the (N) plastic dual-in-line package (Figure 10-35.) Total package substrate current for the N package is 2.5 A. The (J) ceramic dual-in-

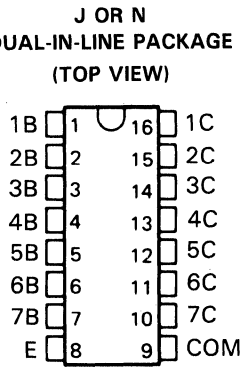


Figure 10-35. SN75465 and ULN2001A Series Package Pinout

line package is limited to 500 mA total current. The SN75465 series devices have a 100 V maximum collector-emitter voltage rating while the ULN2001A series have a 50 V maximum.

The SN75465 and ULN2005A have 1.05-kΩ series base input resistors and are especially designed for standard TTL or other sources with TTL equivalent or greater drive current capability.

The SN75466 and ULN2001A are general-purpose arrays with no input resistors or diodes for level shifting. They have a guaranteed minimum h_{FE} of 1000. These devices will work well as switches or linear amplifiers.

The SN75467 and ULN2002A are especially designed for use with 14 V to 25 V input signals, typical of PMOS logic devices. Each driver has a zener diode and resistor in series with its input to limit the input current for high voltage applications.

The SN75468 and ULN2003A have 2.7-kΩ resistors in series with their inputs allowing them to be compatible with TTL and 5-V CMOS logic.

The SN7469 and ULN2004A have 10.5-kΩ resistors in series with their inputs. They operate from medium logic voltage levels of 6 V to 15 V, typical of some CMOS and PMOS logic.

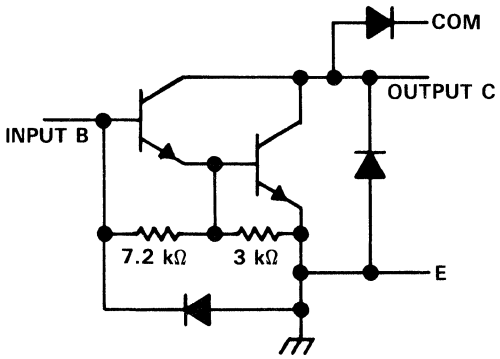
UDN2841 and UDN2845 Quad High Current Darlington Drivers

The UDN2841 and UD2845 are quad peripheral drivers designed for high voltage (up to 50 V), high current (to 1.5 A) switching applications. These devices are designed to provide a solution to the unique application requirements resulting from loads that must operate from a negative supply rail. Such systems include electronic-discharge printers, bipolar and unipolar dc motors, telephone relays, matrix displays, PIN diodes and other high current loads operating from negative power supplies.

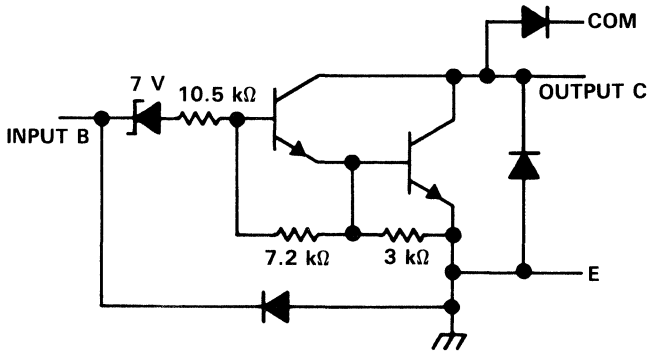
The UDN2841 is intended for current sink applications where, for example, the load is connected between ground and the driver's collector. The emitter is connected to the negative supply and the driver acts as a sink to that supply (Figure 10-37).

The UDN2845 is intended for use as a sink and source combination allowing bidirectional switching where both ends of the load are floating. An application example would be driving a reversible dc solenoid.

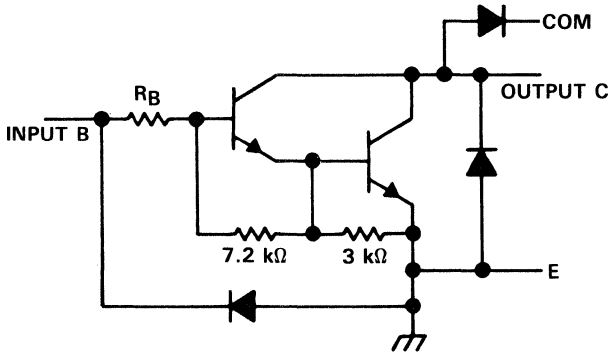
Both the UDN2841 and UDN2845 drivers feature a pnp input transistor that acts as a signal level translator and provides a high input impedance for compatibility with



(a) SN75466/ULN2001A



(b) SN75467/ULN2002A



(c) SN75465, ULN2005A, SN75468, ULN2003A, SN75469, AND ULN2004A

Figure 10-36. Schematics of Darlington Pairs

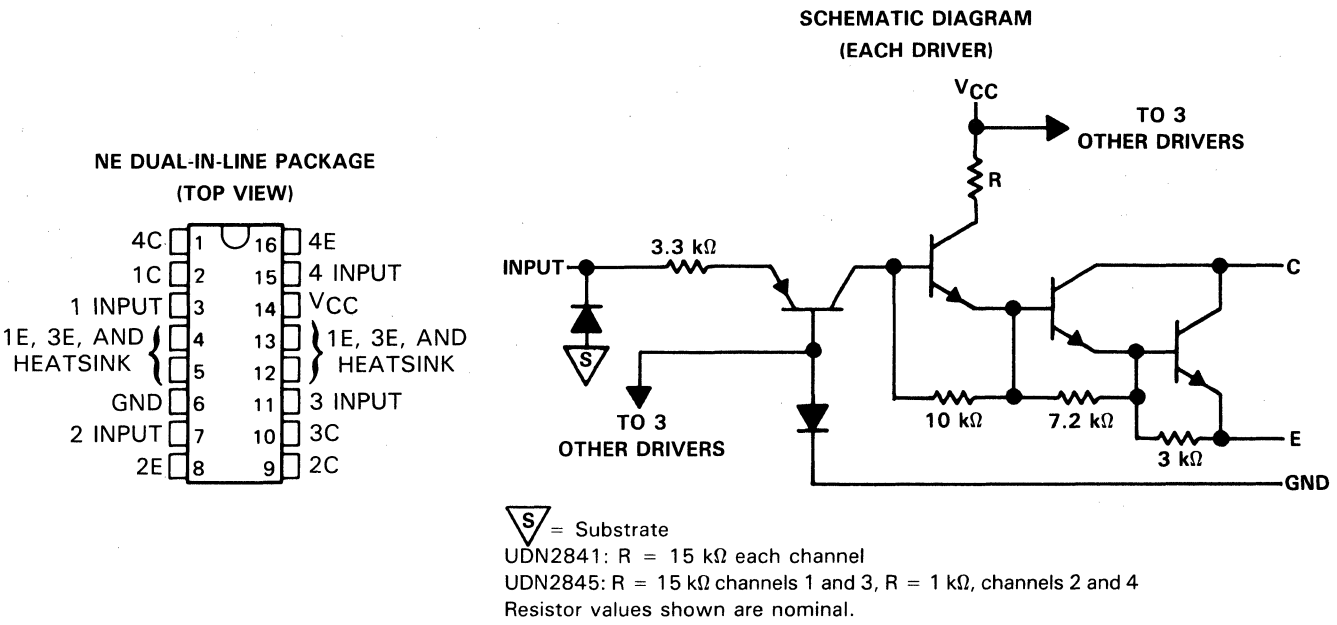


Figure 10-37. UDN2841 and UDN2845 Package Pinout and Schematic

standard TTL as well as low power 5-V CMOS. Following the pnp input is an npn transistor acting as a preamplifier and providing the gain required to adequately drive the 1.5 A Darlington output pair. Drivers 2 and 4 have uncommitted emitters and collectors while drivers 1 and 3 have emitters internally connected to the substrate. For proper operation, these emitters and the substrate must be connected to the most negative supply voltage.

PERIPHERAL DRIVER APPLICATIONS

PERIPHERAL DRIVER-OPTO APPLICATIONS

Driving Tungsten Filament, or Equivalent, Incandescent Lamps

Incandescant lamps have a characteristic that can pose a serious problem to monolithic integrated circuit drivers. The resistance of the typical incandescent bulb varies significantly with changes in filament temperature. For example, a typical general-purpose bulb, type 1815, is rated at 14 V and 200 mA operating current. One might assume that a monolithic driver rated at 300-mA continuous and 500-mA peak surge would be adequate for driving a lamp requiring only 200-mA drive current. The problem becomes evident if the turn-on surge current is monitored. Type 1815 bulbs have a (cold) turn-on peak surge current of up to 10 times their steady-state value, possibly as high as 2.7 A. Figure 10-38 illustrates a test of surge current for a type 1815 bulb. To overcome the problem of high turn-on surge current the designer has two alternatives: Select a driver with a 3 A surge capability, or do something to limit the surge current.

Several methods can be employed to limit surge currents when using peripheral drivers. One method uses keep-alive resistors as shown in Figure 10-39. These resistors maintain the off-state current at about 50% of the normal steady-state level and result in a standby light intensity of about 10% of normal. Steady-state current for the particular bulbs being used was 250 mA and the warm-up current was 120 mA. With the keep-alive resistor, the surge current is limited to only 500 mA or twice the normal steady-state value.

Figure 10-40 illustrates the limiting of base drive to limit surge current.

The h_{FE} for the particular device output transistors used was about 84. If a peak surge current of 500 mA is selected, the value of the base resistor can be determined by the following equation. The resulting limitation in the output surge current is shown in Figure 10-41.

$$R = \frac{V_{OH} - V_{BE}}{I_{B(limit)}}$$

Where:

$$V_{OH} = 3.5 \text{ V (typical)}$$
$$V_{BE} = 0.7 \text{ V (typical)}$$

$$I_{B(limit)} = \frac{I_{C(limit)}}{h_{FE}}$$

$$= \frac{500 \text{ mA}}{84} = 5.95 \text{ mA}$$

Therefore:

$$R = \frac{3.5 \text{ V} - 0.7 \text{ V}}{0.00595 \text{ A}} = 470 \ \Omega$$

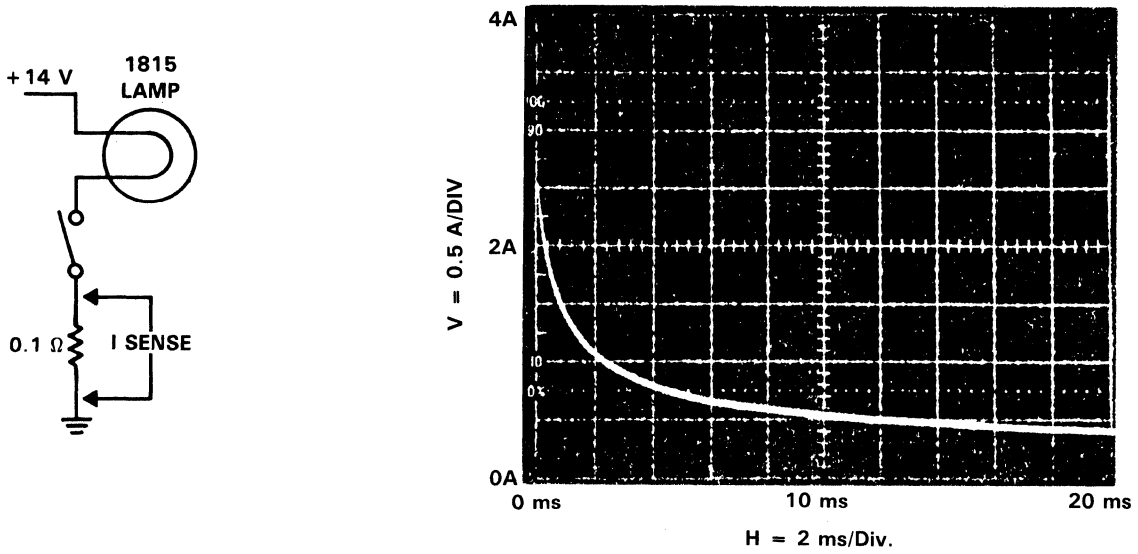


Figure 10-38. Results of Lamp Surge Current Test

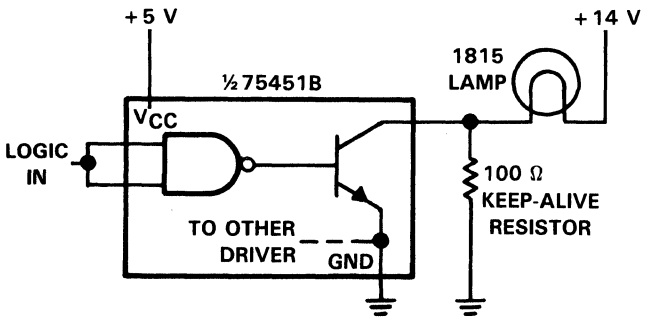


Figure 10-39. Limiting Surge Current with Keep-Alive Resistors

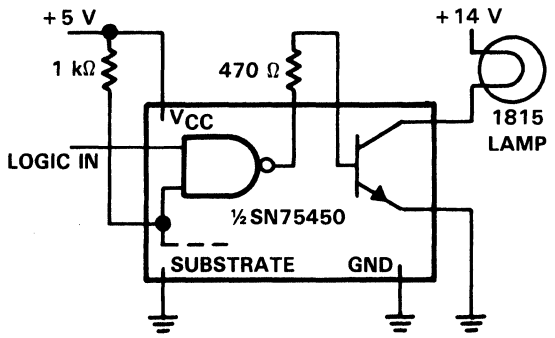


Figure 10-40. Base Drive Current Limiting

This method is not the best solution because of the dependency on h_{FE} and V_{BE}. A resistor value would need to be calculated for each device. A similar method that is much less susceptible to variations in output device parameters is illustrated in Figure 10-42. The current limiting resistor in series with the output transistor's emitter is small enough to be of little significance at the steady-state on level, but will limit the peak levels. The resistor value required may be calculated from the following equation.

$$R = \frac{V_{OH} - V_{BE}}{I_{OP}}$$

Where:

V_{OH} = 3.5 V , V_{BE} = 0.7 V and
I_{OP} = 500 mA (the desired peak limit)

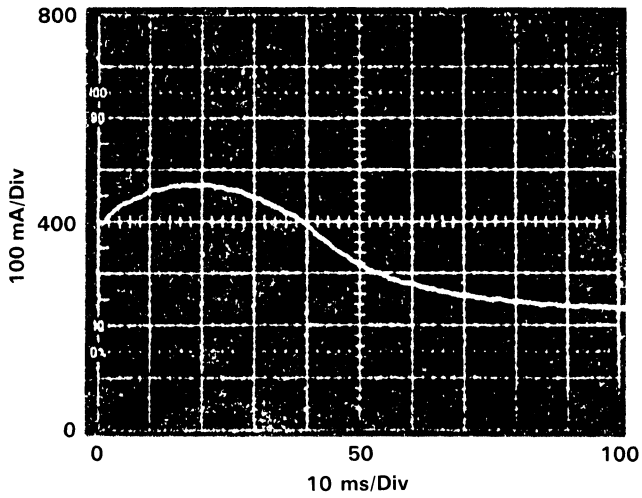


Figure 10-41. Base Drive Limited Surge Current

In this application the value of R is 5.6 Ω. The resulting surge current limitation is shown in Figure 10-43.

Consistency of performance can be improved by using both drivers in a dual peripheral driver package. The circuit in Figure 10-44 uses one transistor (Q2) to sense the output level and clamp it at the desired peak value by controlling

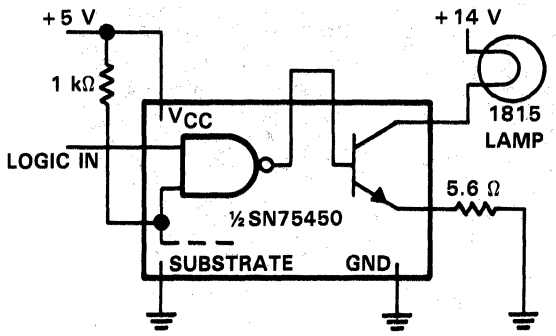


Figure 10-42. Emitter Resistor Surge Limiting Circuit

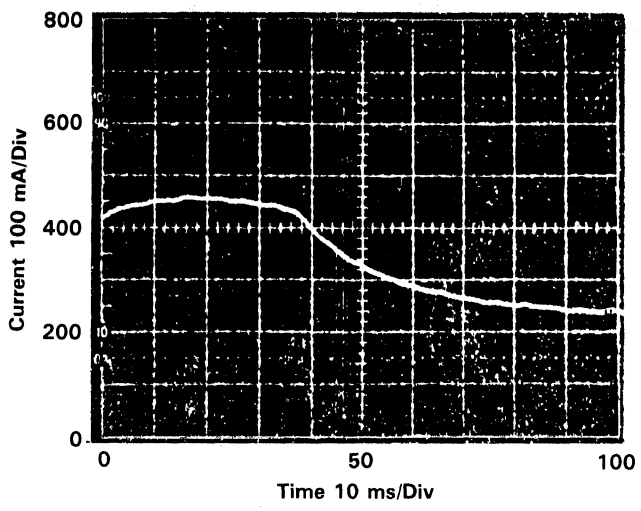


Figure 10-43. Output Current vs Time for Emitter Limiting Circuit

the amount of base drive to the output transistor (Q1). A V_{BE} of only about 0.75 V is required to turn on the sensing transistor. The value of the sensing resistor is therefore:

$$R = \frac{V_{BE}\ (on)}{I_{OP}}$$

For I_{OP} = 0.5 A, R = 1.5 Ω.

The 68-Ω resistor in the gate output limits the gate output current level during clamping only. This resistor must be small enough to not limit the transistor output current during normal operation.

When current through the sense resistor is high enough to cause a 0.75 V base-emitter voltage on Q2, Q2 will start to turn on. The collector of Q2 is connected to the base of Q1 and will clamp its base drive, limiting I_{OUT} peak at the selected value, as shown in Figure 10-45.

Another dual stage circuit that will provide consistent performance is the delayed turn-on configuration shown in Figure 10-46.

In this application, limited lamp current is allowed for a period of 150 to 200 ms while the lamp warms up and increases its resistance. After this delay full power is applied, but the bulb resistance is higher and only a small surge current is experienced. A 27-Ω resistor is used in series with the initial switch, limiting the peak current to under 500 mA. The second driver channel has an RC delay network at its input consisting of a 5.6-kΩ resistor and a 62-μF capacitor. The resulting RC time constant is 354 ms. For a logic input voltage of 3.5 V, with the gate input threshold level of 1.4 V,

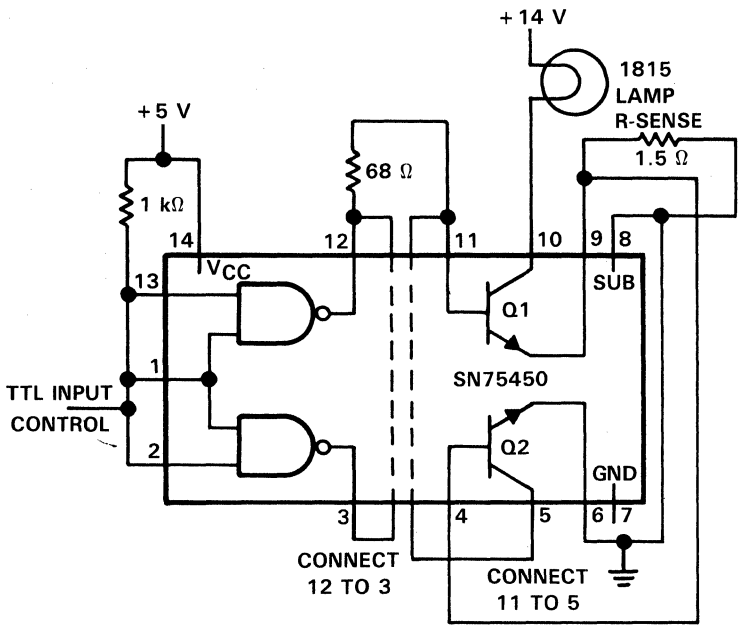


Figure 10-44. Transistor Current Sensing and Peak Limiting

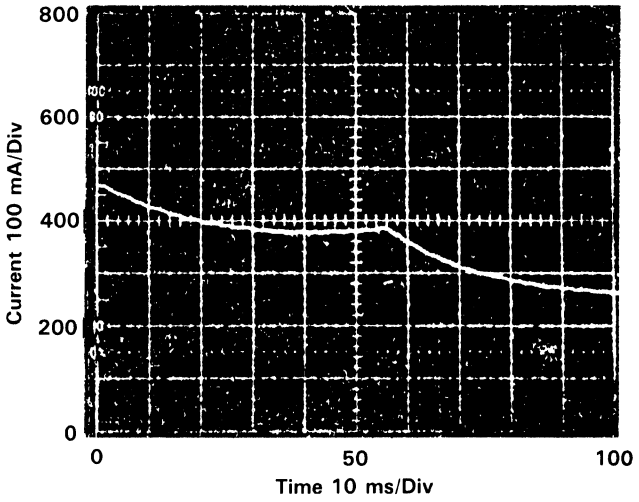


Figure 10-45. Output Current vs Time for Current Sensing Circuit

the second channel will be turned on when its input voltage reaches 1.4 V or 40% of the logic "1" level. A 40% amplitude level will occur at 0.5 RC time constants. Thus the delayed full power turn-on will occur at 0.5 × 354 ms or at about 177 ms as illustrated in Figure 10-47. In this application, the initial surge current is limited to 425 mA and the delayed turn-on surge is only 300 mA.

Driving Remotely Located LED Devices

There are times when it is necessary to drive an LED indicator from a remote location. This requires sending the control signal from one location to another, over a data transmission line, and then providing sufficient drive power to drive the LED. Figure 10-48 illustrates a method often used for this type of remote application.

The SN75372 dual FET driver has the speed and power capability to drive a data transmission line and the LED directly without additional circuitry. As shown in Figure 10-49, the LED may be connected between a supply and the signal line (driven in the sink mode) or between ground and the signal line (driven in the source mode).

In calculating the values for current limiting resistors (R), consideration of the SN75372's output voltages V_{OH} and V_{OL} must be made. For example:

$$R_H = \frac{V_S - V_{OL} - V_{LR} - V_F}{I_O}$$

$$R_H = 158.5\ \Omega$$

Where:

V_S = Supply voltage
= 5 V
V_{OL} = Driver low level output voltage
= 0.2 V
V_{LR} = Voltage drop due to line resistance.
= 0.03 V (100 ft line at 20 mA)
V_F = Forward voltage drop of LED
= 1.6 V (at 20 mA)
I_O = Driver output current
= 20 mA

$$R_L = \frac{V_{OH} - V_{LR} - V_F}{I_O}$$

$$R_L = 78.5\ \Omega$$

Where:

V_{OH} = Driver high level output voltage
$V_{OH} = V_{CC2} - 1.8$ V (at 20 mA)
V_{OH} = 3.2 V

Standard resistor values of 150 Ω and 75 Ω may be used.

RELAY AND SOLENOID DRIVER APPLICATIONS

When peripheral drivers are used to drive inductive loads such as relays and solenoids, special attention should be given to the device's switching voltage, as well as current and power capabilities. Most peripheral drivers have their

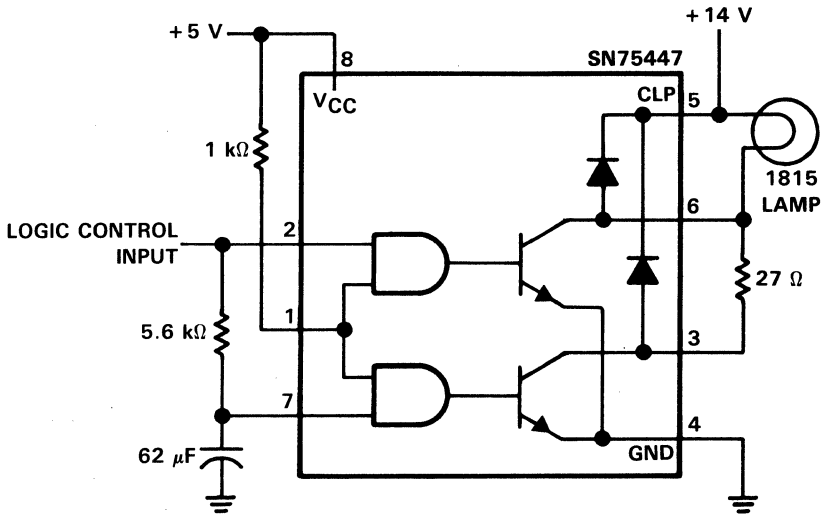


Figure 10-46. Two Stage, Full Power Delayed, Surge Limiting Circuit

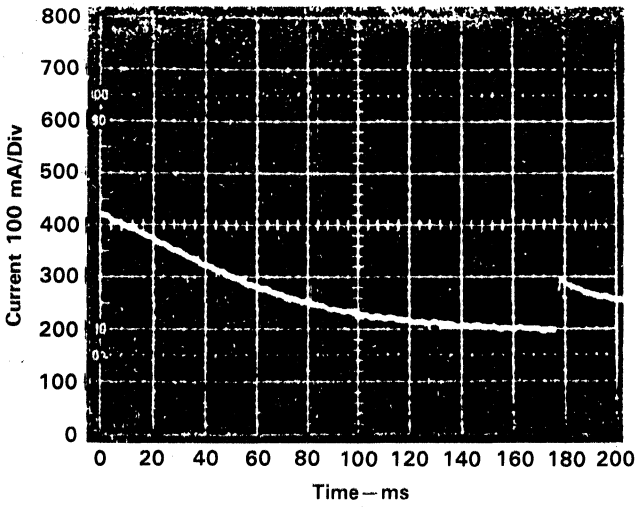


Figure 10-47. Delayed Turn-on Surge Current vs Time

maximum switching voltage specified and care must be taken to avoid exceeding this parameter. Often clamp diodes are used to prevent excessively high voltages at the driver output when driving inductive loads. Figure 10-50 illustrates the basic application and the typical waveform of a diode clamped output. Many peripheral drivers now have built-in inductive clamp diodes.

Printer Hammer Driver Application

In this application, the hammer solenoids require operation from a 30-V supply with peak driver currents of 300 mA. More than one hammer may be actuated at a time. The SN75447 peripheral driver was selected for this application (Figure 10-51). This dual driver will switch up to 50 V (after conducting 300 mA) without latching or breaking down. In addition, the output transient suppression diodes are included in the driver. Since both outputs of the dual driver may be on at the same time, its power handling capabilities must be compared with actual worst case operating conditions. Maximum 5 V supply power dissipation for the SN75447 is equal to 5.25 V times 18 mA (the maximum specified chip supply voltage and current) or 94.5 mW. Output power will be the product of the worst case V_{OL} and the peak (I_{OL}) expected. For this device the output power dissipation, with both outputs on, will be 2(300 mA)(0.65 V) or 390 mW. Power handling capability for this device is 1380 mW at 25 °C. The package has a derating factor of 11.1 mW/ °C which yields an 880-mW power capability at the maximum operating temperature of 70 °C. Since the total (chip supply power of 94.5 mW and the output power of 390 mW) is 484.5 mW, it is well within the 880 mW capability at 70 °C, making the SN75447 a good choice.

Driving a Reversible Solenoid

There are times when the solenoid or relay to be driven is bidirectional and therefore must be driven in both directions. Some peripheral drivers are specifically suited for those applications. Bidirectional drive is most easily accomplished with drivers having a combination of both sink and source outputs or totem-pole outputs. The devices in Table 10-7 are examples of drivers suited for bidirectional drive.

Table 10-7. Devices for Bidirectional Drive

DEVICE	V_{CEmax} (V)	I_{Cmax} (A)	$V_{CE(sat)}$ @ I_{Cmax} (V)	t_{PHL} (μs)	t_{PLH} (μs)
SN75603	40	2.0	2.0	1.8	1.4
SN75604	40	2.0	2.0	1.8	1.4
SN75605	40	2.0	2.0	1.8	1.4
UDN2845	50	1.5	1.6	1.5	1.0
ULN2075	80	1.5	1.5	1.5	1.0
ULN2074	50	1.5	1.5	1.5	1.0

Several of these devices are suitable for applications where the supply voltage is over 40 V. In applications where the supply voltage is negative, the UDN2845 will meet the circuit requirements. In Figure 10-52, the basic circuit configuration for driving a bidirectional or reversible solenoid, requiring a negative 48 V supply and 0.7 A, is shown. The logic input control signals could be derived directly from a microprocessor or other types of logic control devices. Input control voltage levels for the UDN2845 are standard TTL or low-level CMOS. Input current requirements are less than 500 μA. Diodes are used to clamp the voltage overshoot and undershoot levels thus protecting the driver outputs from the excessive voltage peaks that can occur when switching inductive loads.

Opto Isolated and Time Controlled Reversible Solenoid Drive

In this application, it is necessary to provide reversible solenoid drive with one position actuated for about 56 minutes out of an hour time period and the other position actuated

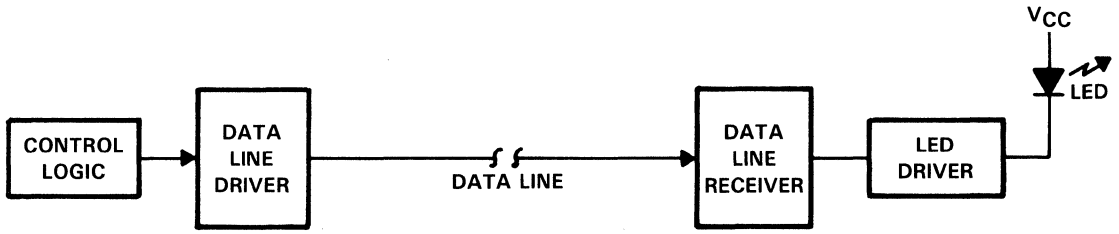


Figure 10-48. Block Diagram of a Typical Remote LED Drive Scheme

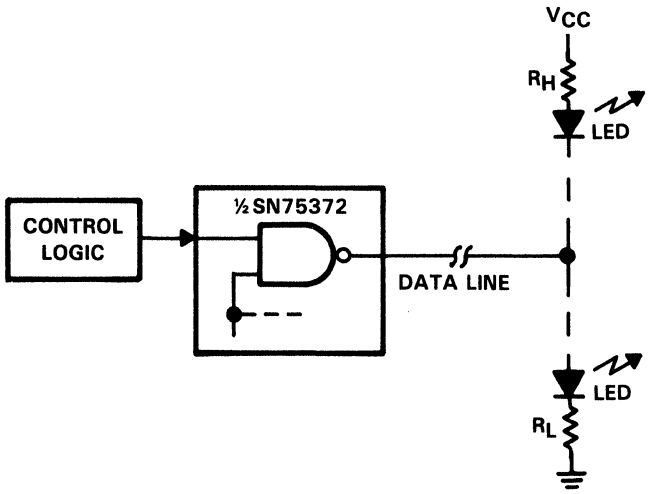
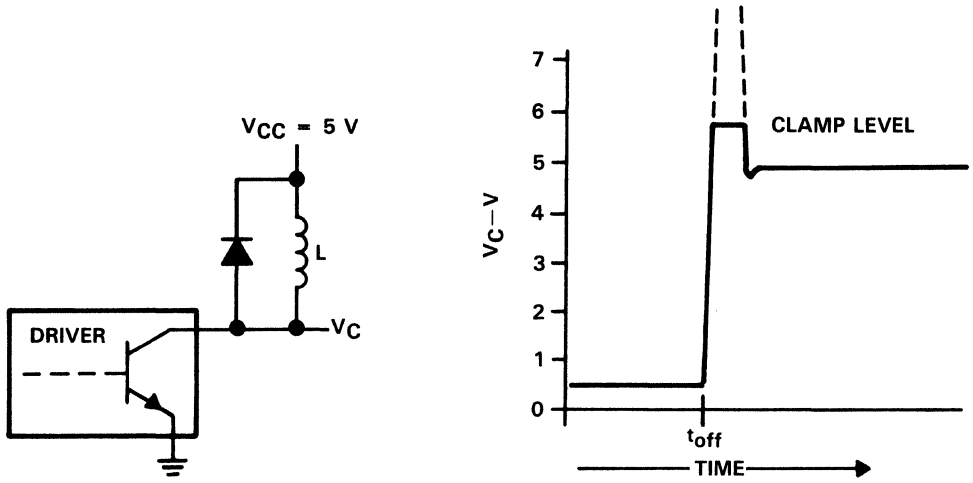


Figure 10-49. SN75372 as a Remote LED Driver



(a) BASIC DIODE CLAMPING (b) CLAMPED OUTPUT TRANSITION

Figure 10-50. Diode Clamping of Driver V_C

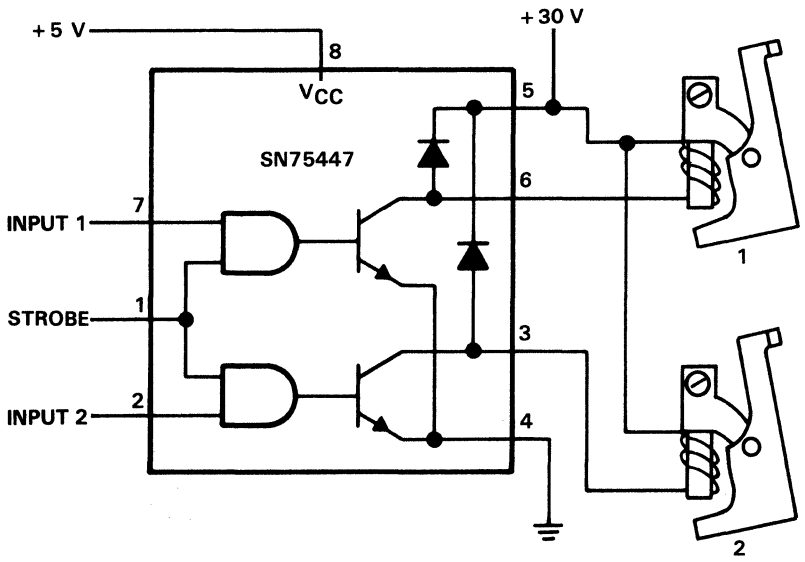


Figure 10-51. SN75447 Dual Hammer Driver

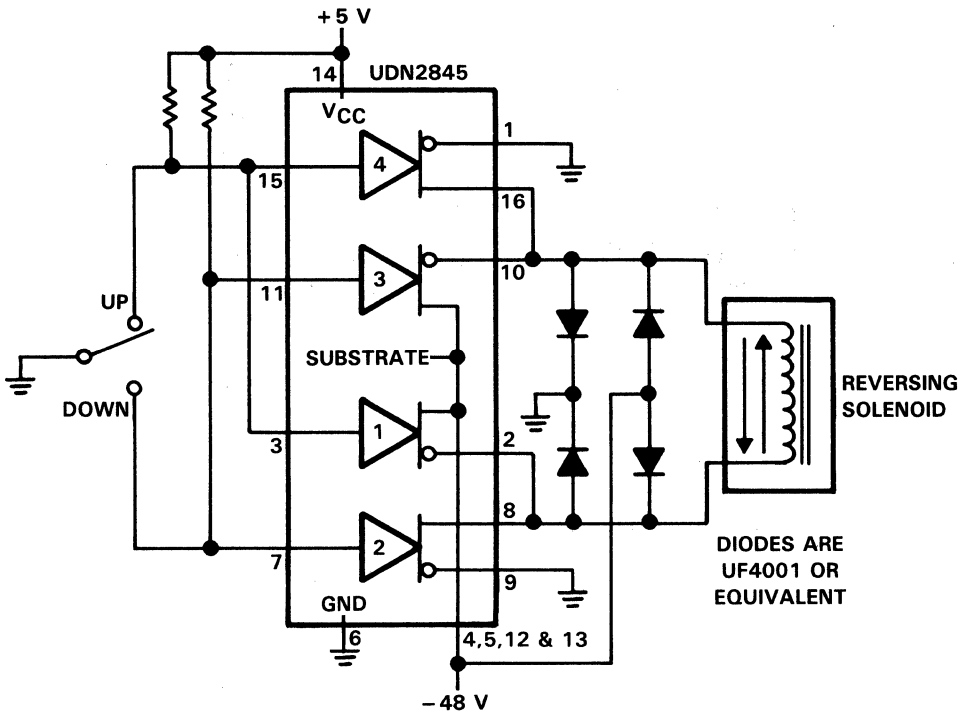
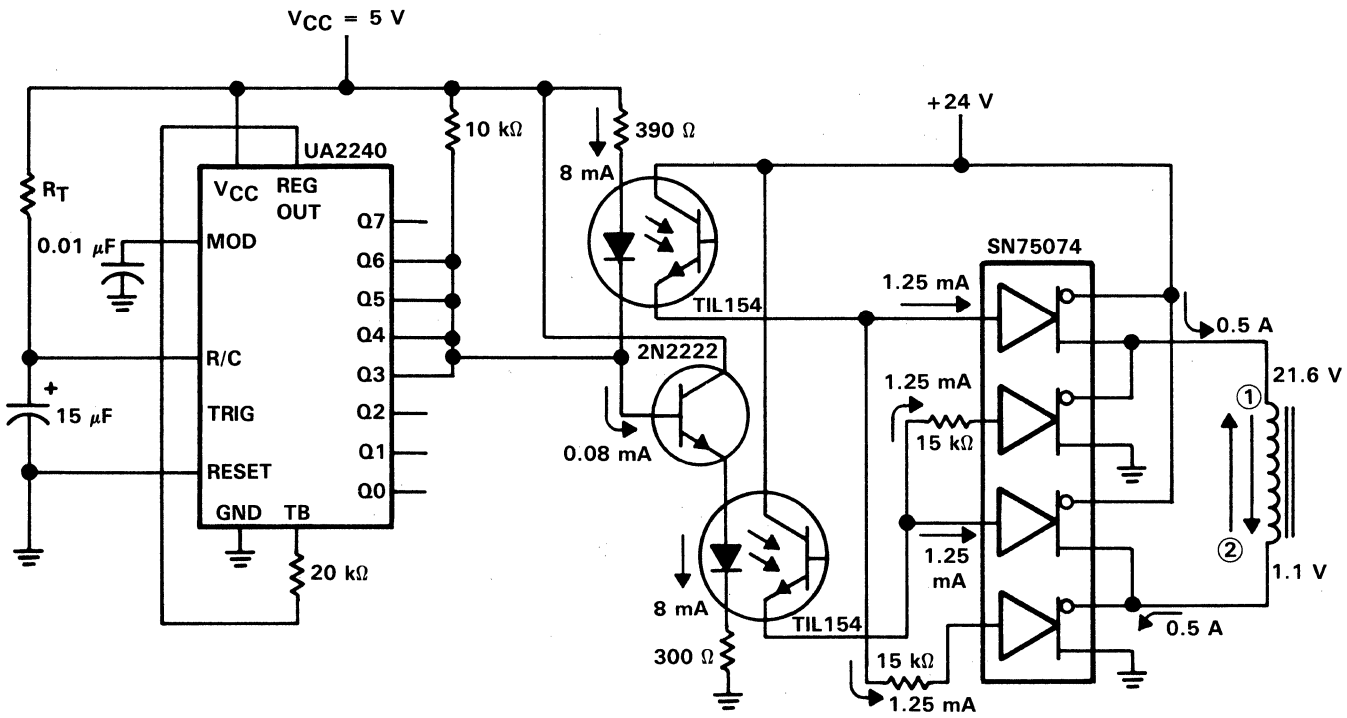


Figure 10-52. Driving a Reversible Solenoid from a Negative Supply



R_T = 937.5 kΩ for exactly 15 μF to generate 1 hour in 256 steps or t_{Bo} = 14.0625 seconds.
Solenoid position ① ~ 56 min
Solenoid position ② ~ 4 min

Figure 10-53. Opto Isolated and Timer Controlled Reversible Solenoid Driver

for about 4 minutes. This is a continuously repeating function that requires the timer circuitry to be isolated from the solenoid supply (Figure 10-53).

Timing is accomplished using a μA2240 programmable timer connected in the astable mode with a time base of about 14.06 s. A time base (t_b) of exactly 14.0625 s will result in a system cycle time of 256 X t_b or 3600 s (1 hr). The timing network consists of a 15-μF capacitor C_T and an R_T of about 940 kΩ. R_T will need to be adjusted to yield a value for t_b as close to 14.0625 s as is practical. Timer outputs Q3, Q4, Q5 and Q6 are wire-ORed to yield the proper output sequence. The result for an accurate time base will be an

output that is low for 56.25 minutes and high for 3.75 minutes. The total time may be adjusted by R_T but the ratio of time high to time low will remain the same. Opto isolation with TIL154 optocouplers provides 2500 V isolation between the controller and the solenoid circuits. The SN75074 driver requires two control inputs, one inverted from the other. One TIL154 is used to couple, in-phase, with the drivers for the forward direction. The inverted drive is done using a 2N2222 NPN transistor operating as an emitter follower driver between the timer and the second TIL154 optocoupler. Output drivers for the reverse direction receive their drive signals inverted from those for the forward direction, allowing the SN75074 to function as a bidirectional solenoid driver. The many applications for a bidirectional solenoid or relay driver include: Fluid Flow Valve Control, Car Electric Door Locks, Relay Switching, and Position Controls.

Power Solenoid Drive

When relatively high power solenoids must be driven, the SN75603, SN75604, and SN75605 are particularly well suited. Individually as drivers, with up to 70 W or more output drive capability, or two in combination for bidirectional drive, this series is a good selection for applications requiring relatively high drive currents.

Figure 10-54 shows the SN75603 and inverting SN75604 in a basic drive configuration for a reversing power solenoid. These devices will sink or source up to 2.0 A from supply rails of 8 V to 40 V. A typical application would be a power solenoid required for operation of a fluid flow control valve.

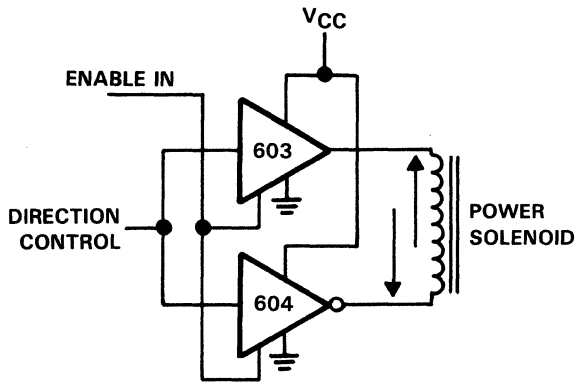


Figure 10-54. Driving a Reversible Power Solenoid

INTELLIGENT SWITCHES

Automotive Lights On Warning

The SN75604, with input control logic but requiring only one supply rail, may be used in special applications requiring input logic where only one supply voltage is available. An example is illustrated in Figure 10-55, a "Lights On" sensor and alarm driver.

In this application, the device V_{CC} and enable inputs are connected to a voltage lead from the light switch. The

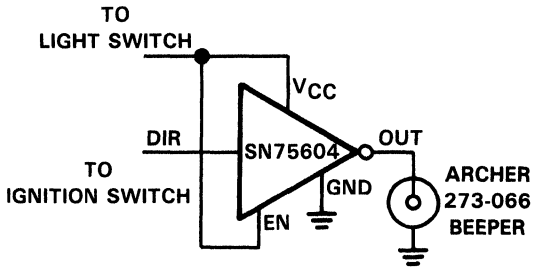


Figure 10-55. Automotive "Lights On" Sensor and Alarm Driver

direction control input is connected to a lead from the ignition switch. Table 10-8 is the truth table for this circuit configuration.

Table 10-8. Lights On Alarm Circuit Truth Table

Light Switch	Ignition Switch	Alarm
ON	ON	OFF
OFF	ON	OFF
ON	OFF	ON
OFF	OFF	OFF

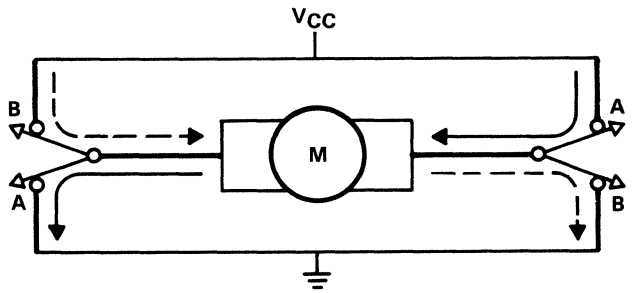
Only operation of the lights without the ignition will result in the alarm sounding. The beeper used in this application is an Archer 273-066 that will operate from 3 V to 28 V. At a typical 12-V level, it will produce a pulsating tone of about 95 dB at 30 cm. The alarm "on" current is about 12 mA when operating from a 12-V supply.

DRIVING MOTORS

"H" OR BRIDGE DRIVE

When it is necessary to switch both ends of a motor winding for forward and reverse operation, a basic "H" or bridge drive is normally used. Figure 10-56 illustrates the basic "H" configuration.

The drivers, or switches, at each end of the motor must be capable of providing both source and sink current to the motor. A single integrated circuit driver capable of providing



Current B ⟶ Flows through the motor left to right
Current A ⟵ Flows through the motor right to left

Figure 10-56. Basic H Motor Drive Configuration

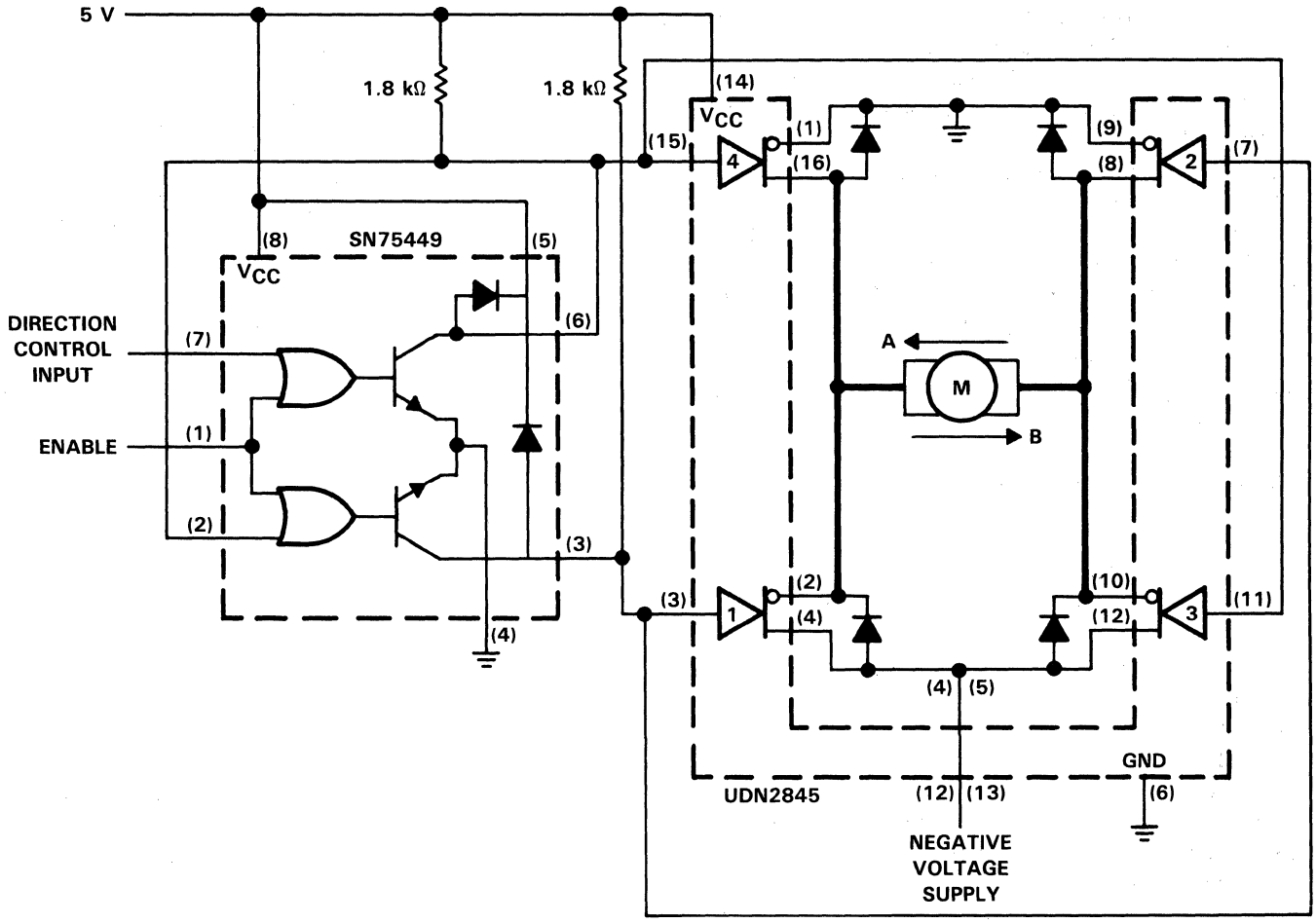


Figure 10-57. UDN2845 Provides Full-H DC Motor Drive

both the source and sink drive is often referred to as a half "H" driver. A circuit with two sink and two source drivers in a single package is referred to as a full "H" driver.

"H" MOTOR DRIVE FOR NEGATIVE SUPPLIES

The UDN2845 provides, in one package, the sink and source drivers needed in a full "H" drive of a dc motor using a negative supply, as illustrated in Figure 10-57. The dc motor in this example is a Pittman model 13104B827. It requires a 300 mA steady state current at 12 V. Turn-on surge currents as high as 1.5 A can be expected. Table 10-9 shows the motor drive conditions for various combinations of input logic.

Table 10-9. Motor Control Truth Table

INPUT DIRECTION CONTROL	ENABLE INPUT	OUTPUT DRIVE TO MOTOR
X	H	OFF
0	L	→ B
1	L	A ←

SPEED CONTROLLED, REVERSIBLE DC MOTOR DRIVE WITH THE SN75603 AND SN75604

For continuous current applications of up to 2 A, the complementary, half "H" SN75603 and SN75604 drivers are recommended. Figure 10-58 illustrates a reversible dc motor drive application with adjustable speed control. The "D" inputs for these drivers are complementary and may be tied together and driven from the same logic control for bidirectional motor drive. The enables are tied together and driven by a pulse-width-modulated generator providing "on" duty cycles of 10% to 90% for speed control. A separate enable control is provided through an SN7409 logic gate. Table 10-10 is the truth table for this motor controller application.

Definitions for the terms used in the truth table (Table 10-10) are as follows:

EN	Enable
DC	Direction Control
SP.C	Speed Control
A	Direction of Current — Right to Left
B	Direction of Current — Left to Right
H	Logic 1 Voltage Level
L	Logic 0 Voltage Level
N	Speed Control Set for Narrow Pulse Width
W	Speed Control Set for Wide Pulse Width
X	Irrelevant

Table 10-10. Truth Table for Motor Control Circuit (Figure 10-58)

EN	DC	SP.C	MOTOR DIRECTION	MOTOR SPEED
L	X	X	OFF	OFF
H	L	N	A	SLOW
H	L	W	A	FAST
H	H	N	B	SLOW
H	H	W	B	FAST

DRIVING POWER FETs FOR DC MOTOR CONTROL

When motors require discrete drivers for high power levels, it may be desirable to use power FET drivers. This is particularly true where pulse-width-modulated speed control and high-speed switching are required. For the application shown in Figure 10-59, an IRF151 power FET was selected for its speed, low on-state resistance and resulting high efficiency. A natural characteristic of this type of power FET is its large channel area and relatively high gate input capacitance. The IRF151 has a typical on-state resistance of 0.055 Ω and a maximum gate input capacitance of 4000 pF. If the power FET is driven from a typical open-collector peripheral driver, as shown in Figure 10-59, a long turn-on time will result. The long turn-on time is due to the product of FET input capacitance and static pull-up resistance. This approach is inadequate for efficient high frequency applications. The preferred method for high speed FET driver applications uses an active pull-up as well as an active pull-down, or totem-pole driver such as the SN75372. Figure 10-60 illustrates the use of an SN75372 to drive the FET gate input and the resulting fast gate switching speed.

STEPPER MOTOR DRIVE

Drive circuitry for stepper motors must have characteristics peculiar to the type of motor being driven. Before looking at drivers for stepper motors, a look at the basic stepper motor and its requirements is in order.

Basic stepper motor action may be illustrated (see Figure 10-61) as a permanent magnet rotor that rotates to align itself with magnetic fields. The magnetic fields are generated sequentially by stator coils located around the rotor. If voltage is applied to coil A (A to A′) the rotor is attracted to and aligns itself with coil A. If the voltage is switched sequentially to coil B (B to B′), then coil C (C to C′), coil D (D to D′), coil A (A′ to A), coil B (B′ to B),

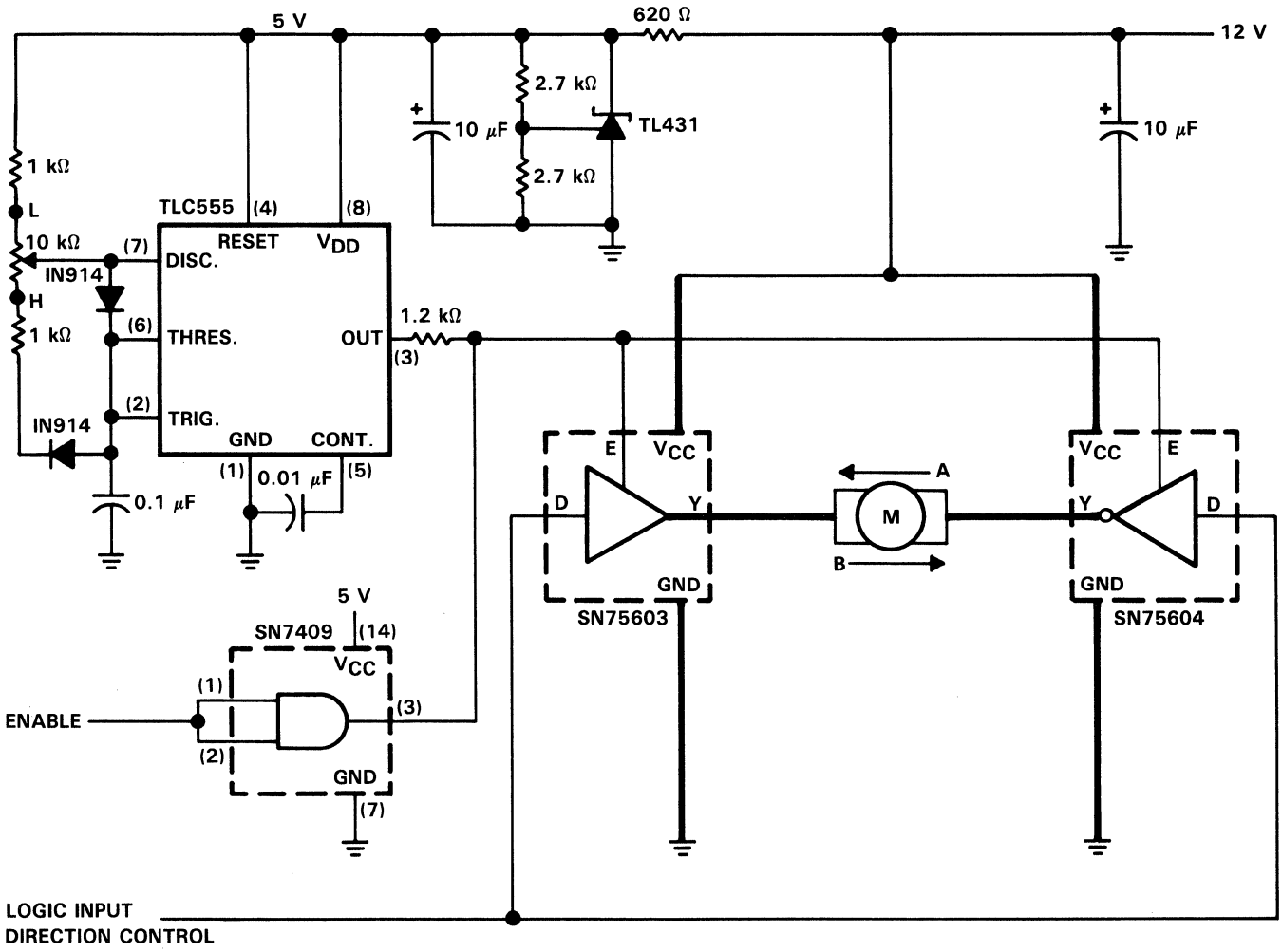


Figure 10-58. SN75602 and SN75604 Devices in a Bidirectional Motor Control Application with Speed Control

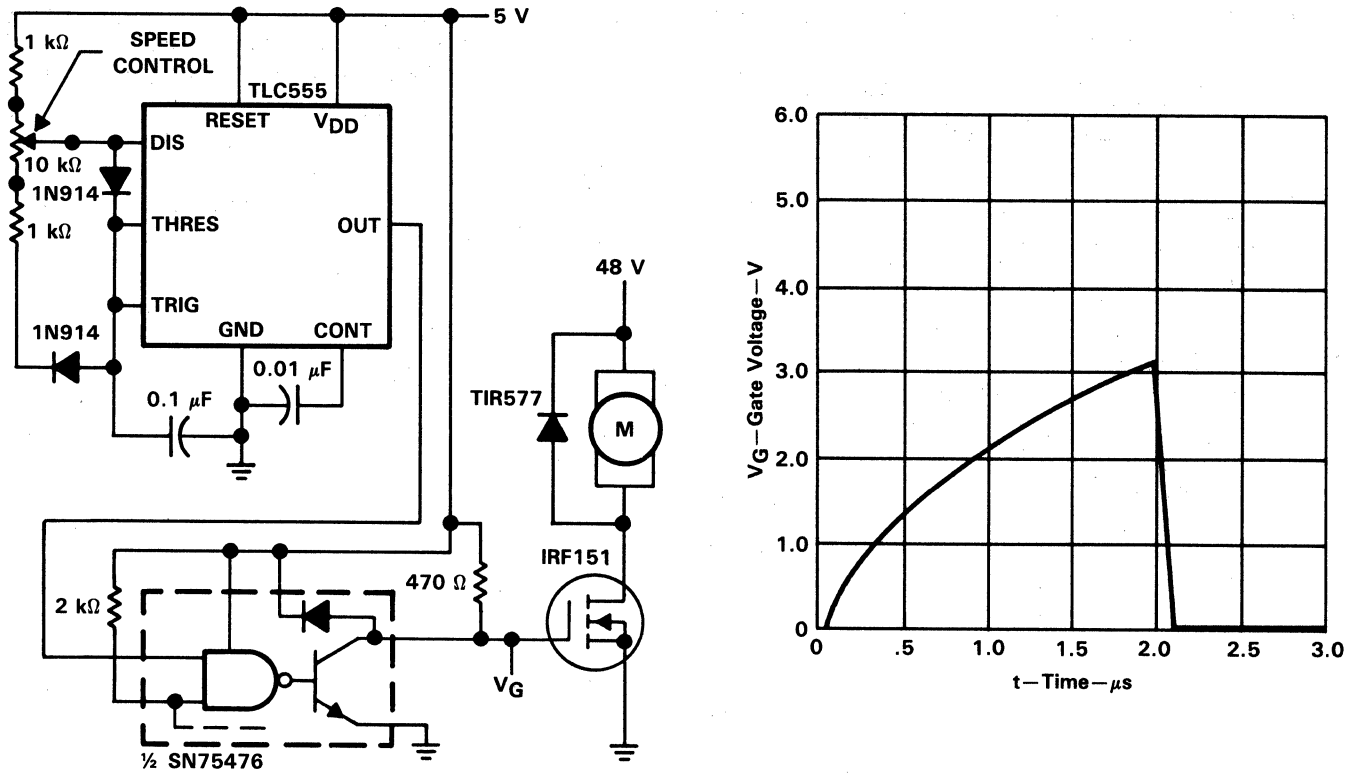


Figure 10-59. Open-Collector Drive and Resulting FET Gate Response

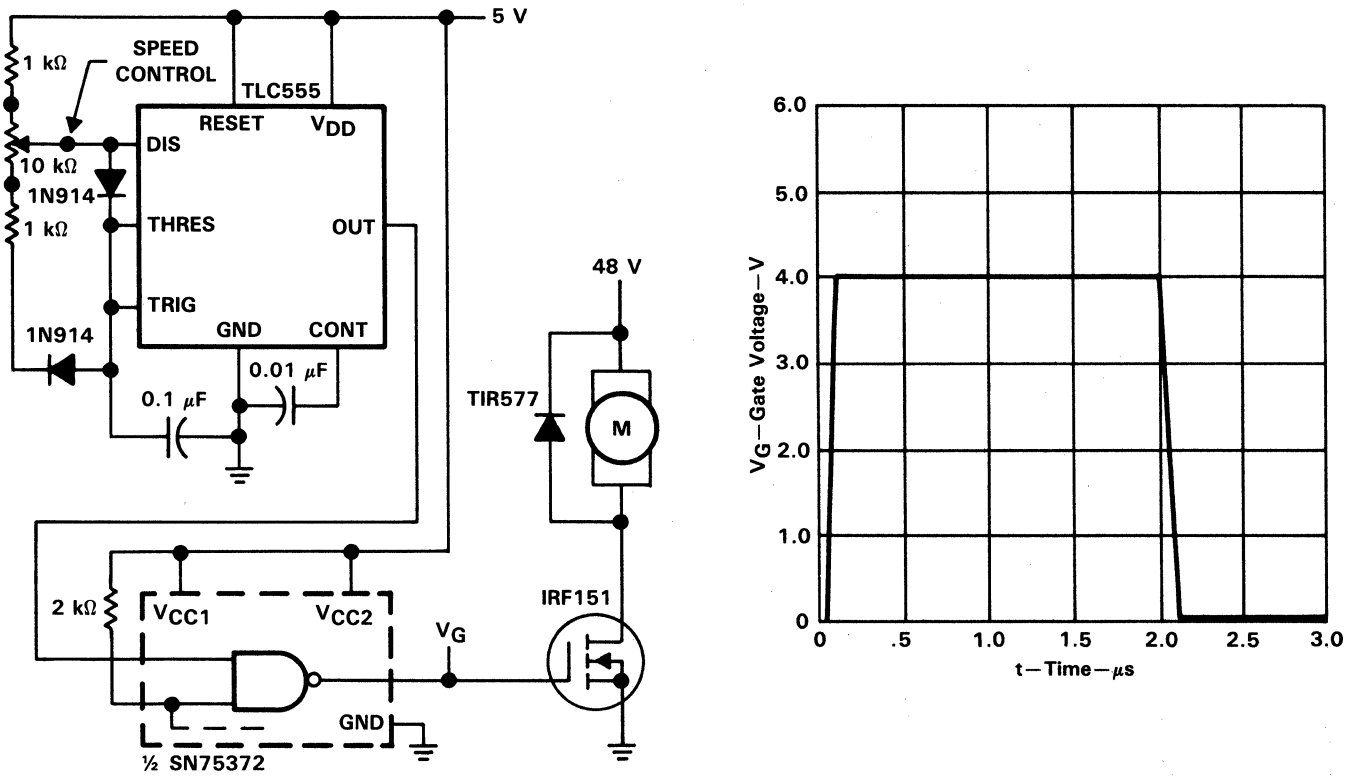


Figure 10-60. SN75372 Totem-Pole Drive and Resulting FET Gate Response

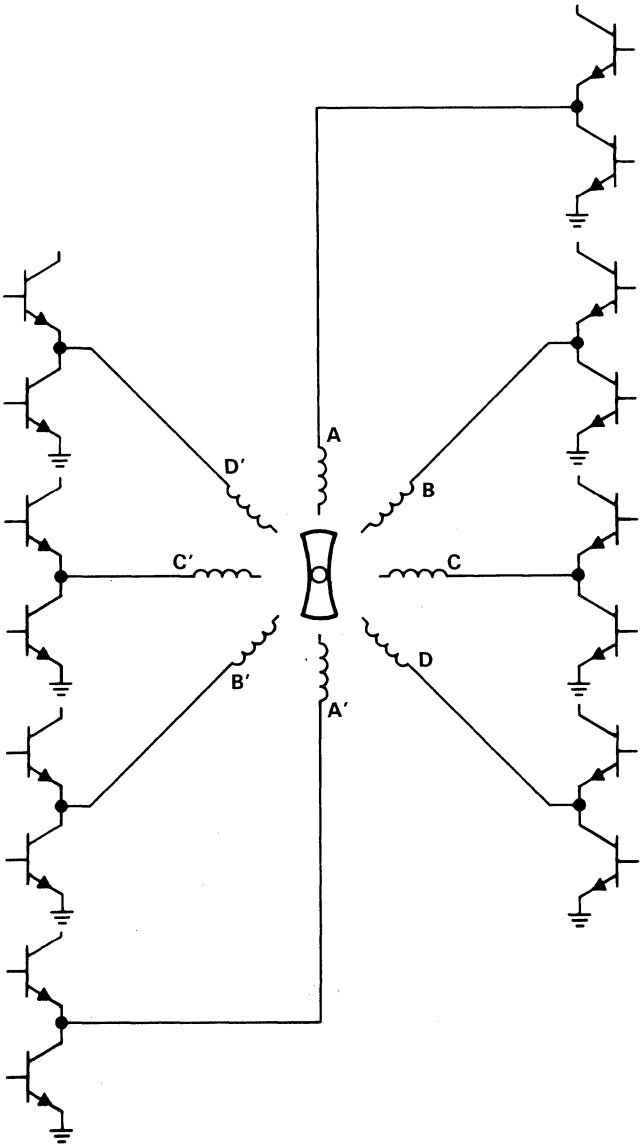


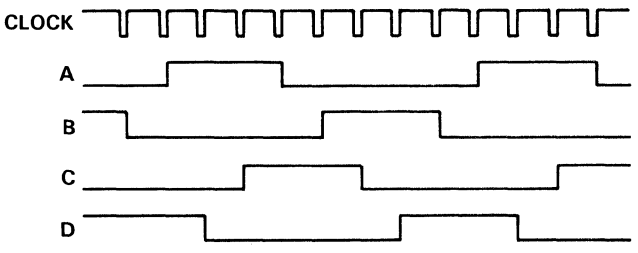
Figure 10-61. Basic Stepper Motor Action

coil C (C′ to C), coil D (D′ to D) and then repeat coil A (A to A′), the rotor will have followed the magnetic field step-by-step for a full 360 degrees of rotation.

The magnetic field in a stator coil will hold the rotor in a fixed position as long as voltage is applied to that coil. Switching the voltage from coil to coil causes the rotor to move, following the field. The rate at which the coils are sequentially switched will determine the rotor speed. In a basic two-pole rotor stepper configuration, with eight stator positions, (8 x 1500) or 12,000 steps per minute will be required to rotate at 1500 rpm. In this typical application a clock rate of 200 Hz is required to provide 12,000 steps per minute. Since the rotor follows the field, simply reversing the timing sequence will result in reversing the direction of rotation.

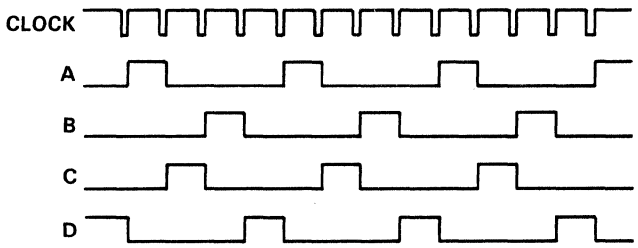
The basic drive mode just described is sometimes called the wave-mode and requires only one phase (or coil) to be on at a time. However most wave-mode stepper motor drives are not this simple. Other more common drives include the normal-mode, with two phases on at a time, and the "half-step" mode having one phase on then two phases on then one phase, and so on. The waveforms for these drive methods are illustrated in Figure 10-62.

A multiple-pole wave-mode motor is often used to provide short rotations per step where rotor position is more critical. Figure 10-63 shows a stepper motor configuration having eight stator poles and seven permanent magnet rotor poles. Opposing stator coils (180 degrees apart) are connected in series and are phased to provide rotor attraction at one coil and repulsion at the other. Shifting the drive from stators 1 and 5 to stators 2 and 6 (clockwise) results in a rotor pole being attracted to stator 2 and repelled from stator 6, resulting in a slight counterclockwise rotation. Sixty-four steps are required to complete one full revolution of the rotor, each step being 5.625°.



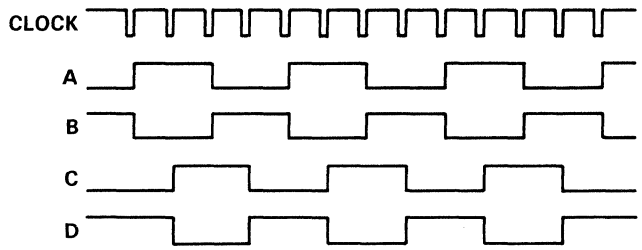
HALF STEP MODE

Provides 2 phases on, 1 phase on, 2 phases on, 1 phase on type of drive sequence.



WAVE DRIVE MODE

Provides 1 phase on at a time.



NORMAL DRIVE MODE

Provides, sequentially overlapping, 2 phases on at a time.

Figure 10-62. Half-Step, Wave and Normal-Drive Mode Waveforms

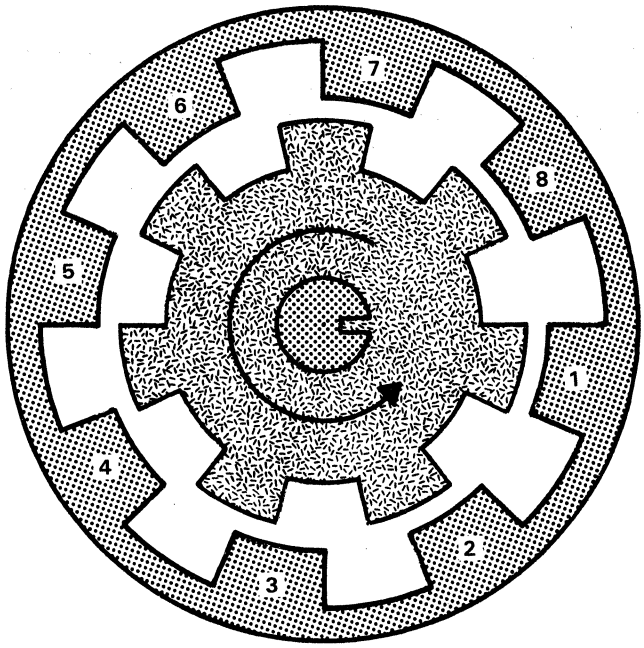


Figure 10-63. 8-Pole, 64-Steps per Revolution, Stepper Motor

The motor stator windings in this example are bridge driven with half "H" drivers at each end of the coils as illustrated in Figure 10-64. The drivers used are the SN75603 and SN75604. They provide complementary outputs allowing each set of coils to be controlled by the same data input pulse. The enables for each set are also paralleled and only four data inputs and four enable inputs are required. Driver data inputs (AD through DD) and enable inputs (AE through DE) provide a type of wave-mode drive that results in sequential stepping. Motor control waveforms are generated using the controller circuitry illustrated in Figure 10-65.

The clock generator shown in Figure 10-65 is a TLC555 timer connected as an astable oscillator operating at 400 Hz. Its output feeds an SN74198 8-bit shift register which generates eight waveforms, four data and four enable. These waveforms are combined with the aid of an SN7432 quadruple OR gate to form the correct drive patterns. Notice that simply changing the operating mode of the SN74198 register from shift left to shift right results in reversing the direction of motor rotation.

The shift register is automatically cleared during power-up by the resistor-capacitor (RC) network on the $\overline{CLR}$ input. The RC time constant needed to obtain the desired $\overline{CLR}$ pulse width may be calculated as follows:

$$RC = \frac{t_{wC}}{2.303\left(-\log\frac{1 - V_T}{V_S}\right)}$$

where

t_{wC} is the clear pulse width; 1.0 ms for this application
V_T is the typical clear input threshold; 1.4 V
V_S is the supply voltage

In this example, the calculated value for RC is about 3.0 ms. Selecting a 0.1 μF capacitor for C, the resistor value will be 30 kΩ.

At power-up, the $\overline{CLR}$ pulse sets all shift register outputs low. The SN74198 outputs are connected to inputs of an SN74260 device that contains two 5-input NOR gates. With all of the SN74260 inputs low at turn-on, its outputs will be high. The outputs are fed through OR gates to the serial inputs (SR and SL) of the shift register. Thus, it provides the initial logic high-level input that will be shifted, QA through QH. When QH goes high, it is fed through OR gates back to the register's serial inputs to continue the cycle. During reverse rotation, the QA pulse is fed back to the serial inputs to continue the cycle.

Resulting data and enable control pulses are illustrated in Figure 10-66. Shift register outputs QA, QB, QC, and QD are the data pulses AD, BD, CD, and DD, respectively. An SN7432 device containing four 2-input OR gates is used to combine the QA with QE, QB with QF, QC with QG and QD with QH to form the enable pulses AE, BE, CE, and DE.

A 400 Hz clock input will result in 2.5 ms wide steps. This type of application requires 64 steps (0.16 seconds) per revolution of the motor. The motor speed will therefore be 375 rpm during continuous operation.

DRIVING DATA TRANSMISSION LINES

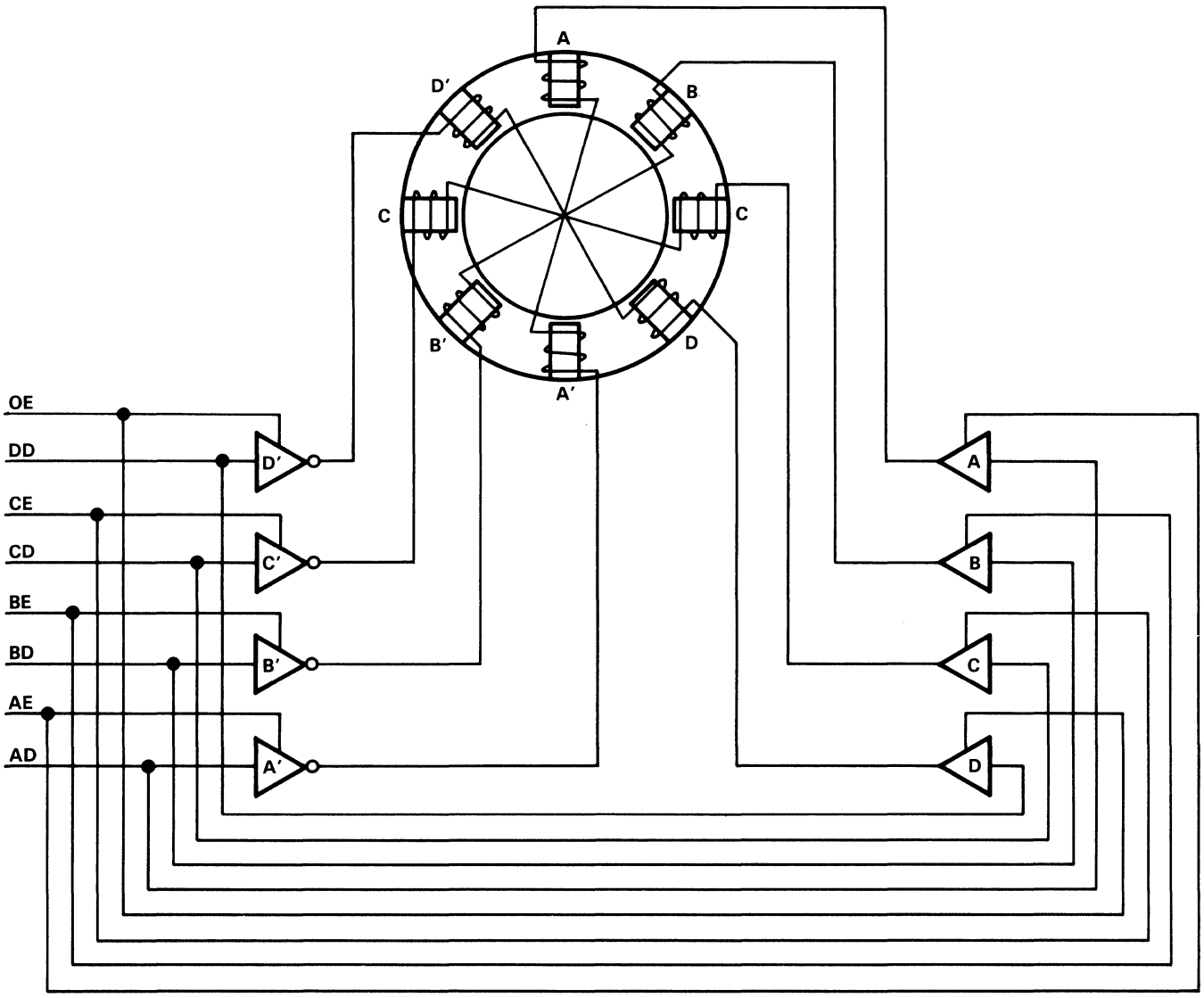
Because of their drive power capabilities, peripheral drivers are suitable for driving data transmission lines. The SN75450B type devices, for example, allow sink or source mode or differential line drive operation as illustrated in Figure 10-67. In Figure 10-67(a), the SN75450 is connected as a dual source-mode line driver and the outputs are terminated to ground with resistors equal to the line's characteristic impedance. For this illustration, the output transistor base bias resistor (R_b) was calculated using typical 25 °C values for the SN75450B output transistor characteristics and a V_O of 3.5 V. The line termination resistor is 120 Ω, and transistor h_{FE} is 50.

$$R_b = (V_{CC} - V_b)/I_b$$

where:

$V_{CC} = 5$ V
$V_b = V_O + V_{be} = 3.5\text{ V} + 0.8\text{ V} = 4.3$ V
$I_b = I_O/h_{FE} = 29.17\text{ mA}/50 = 0.583$ mA
$R_b = (5\text{ V} - 4.3\text{ V})/0.583\text{ mA} = 1.2$ kΩ.

Figure 10-67(b) illustrates dual sink mode line drivers with the lines terminated in their characteristic impedance to the supply rail. Other peripheral drivers from the SN75451B, SN75461, and SN75471 families may be used as sink drivers. A combination of the two drive modes is shown in Figure 10-67(c) where the SN75450B is connected as a single balanced (differential) mode driver. In this example, the line termination resistors are equal to about one-half of the characteristic line impedance (or 62 Ω) and will



A, B, C and D are SN75603 drivers (non-inverted outputs).
A′, B′, C′ and D′ are SN75604 drivers (inverted outputs).

Figure 10-64. Bridge Driven 8-Pole Stepper Motor

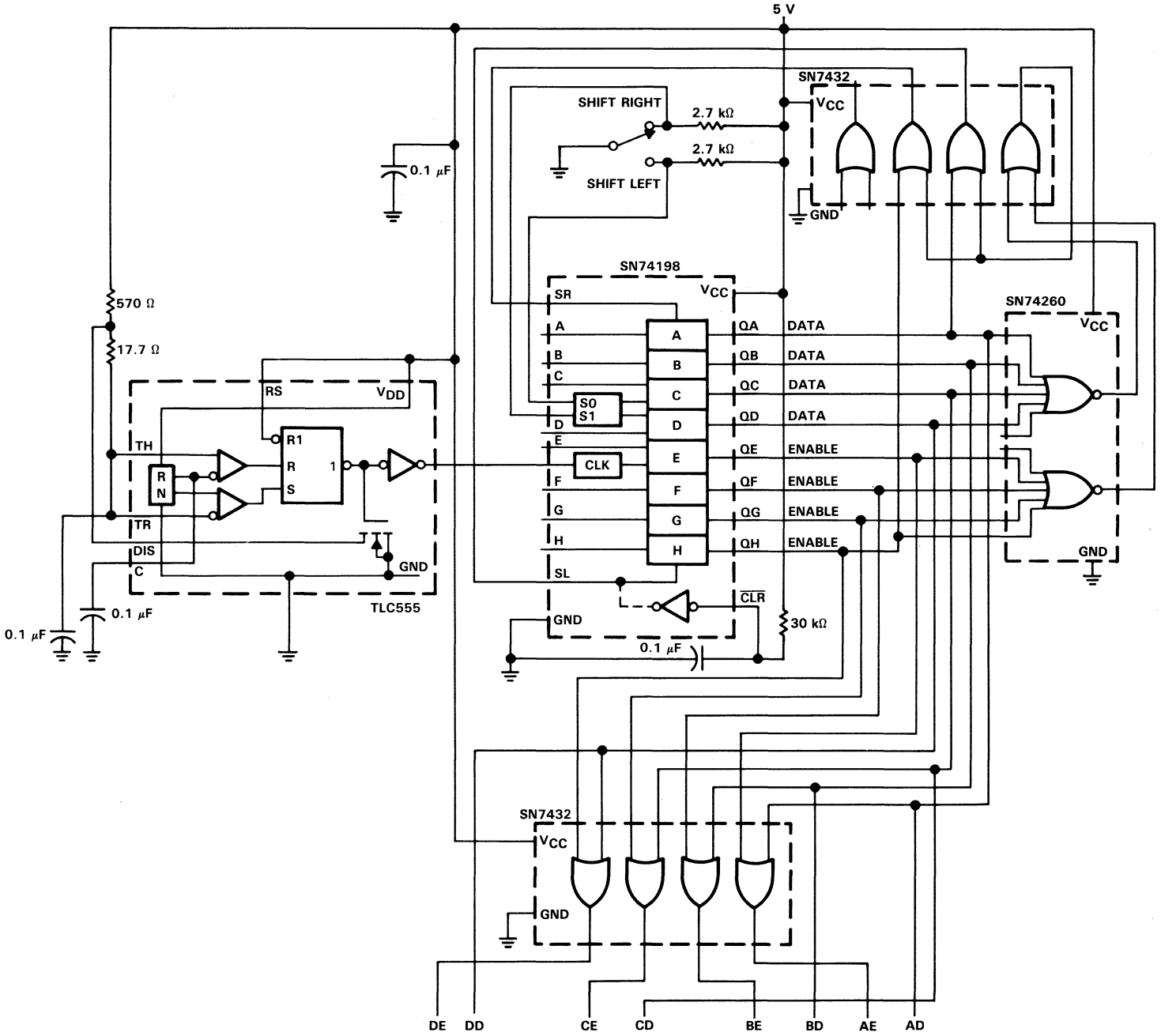


Figure 10-65. Motor Control Waveform Generator

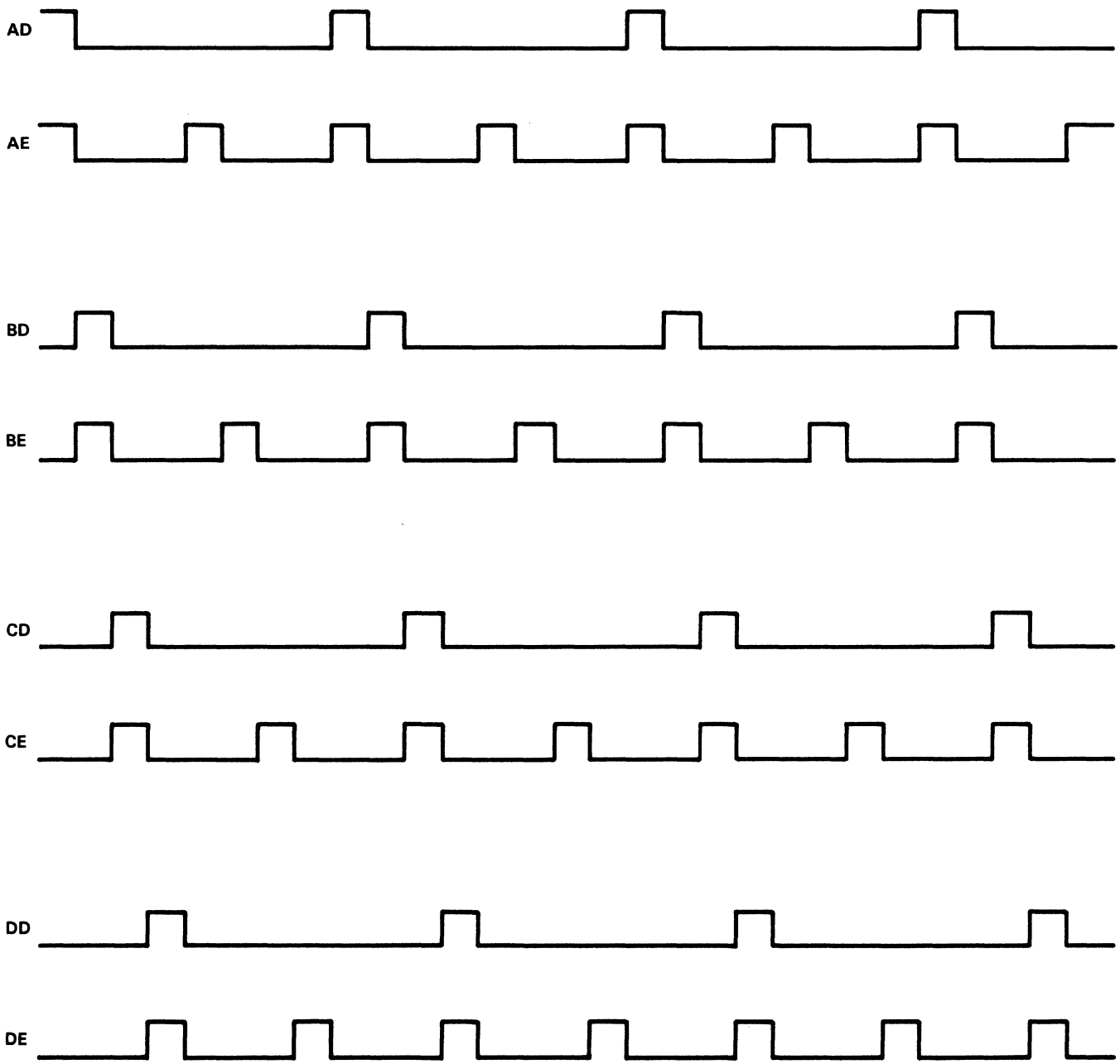
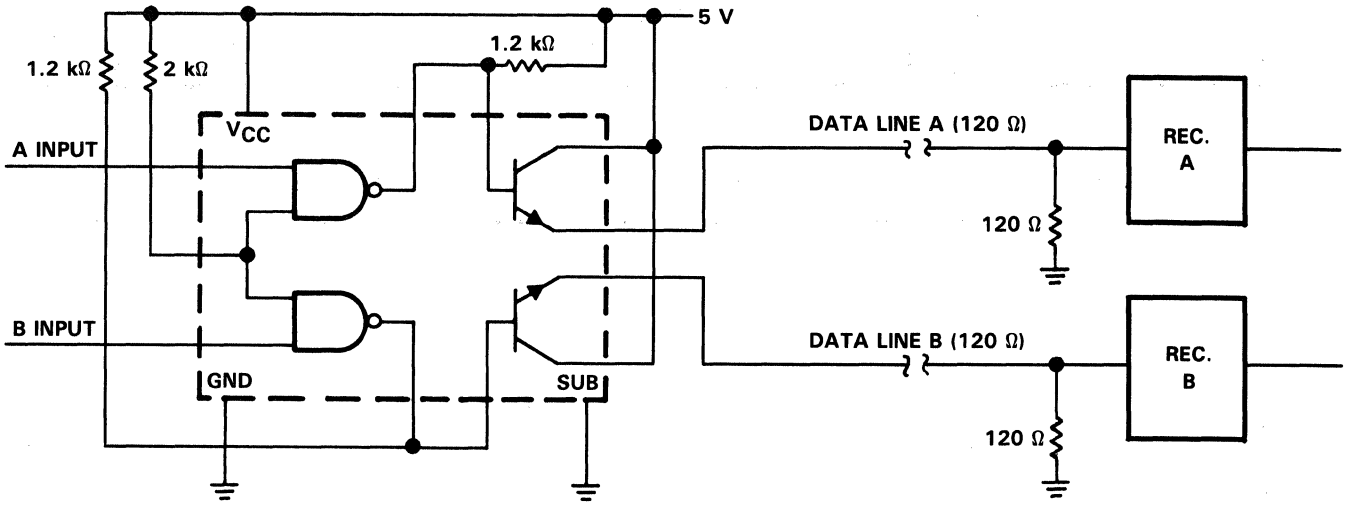
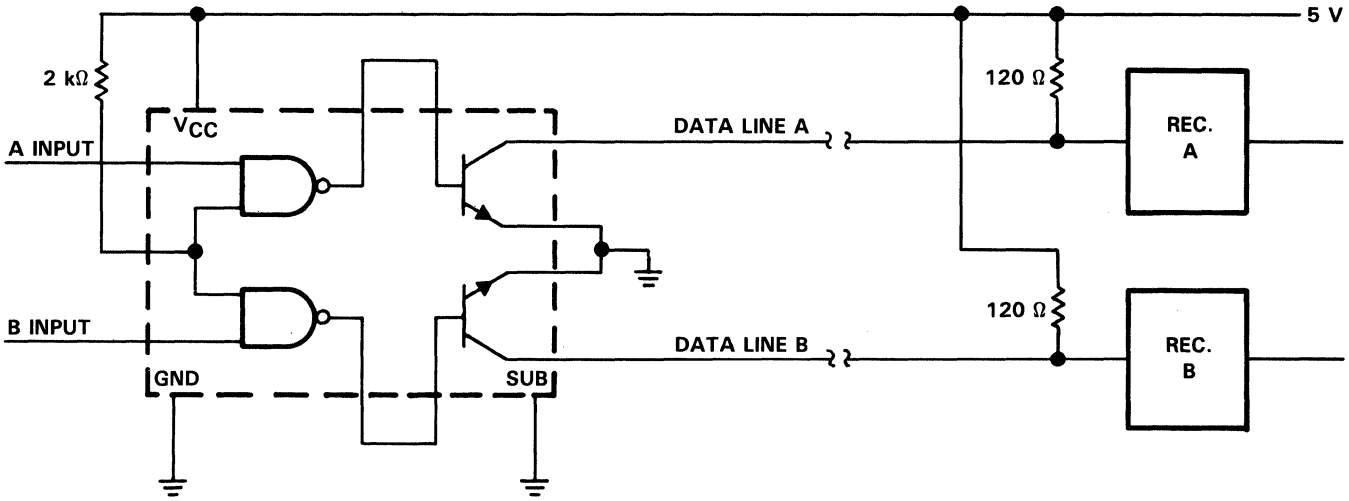


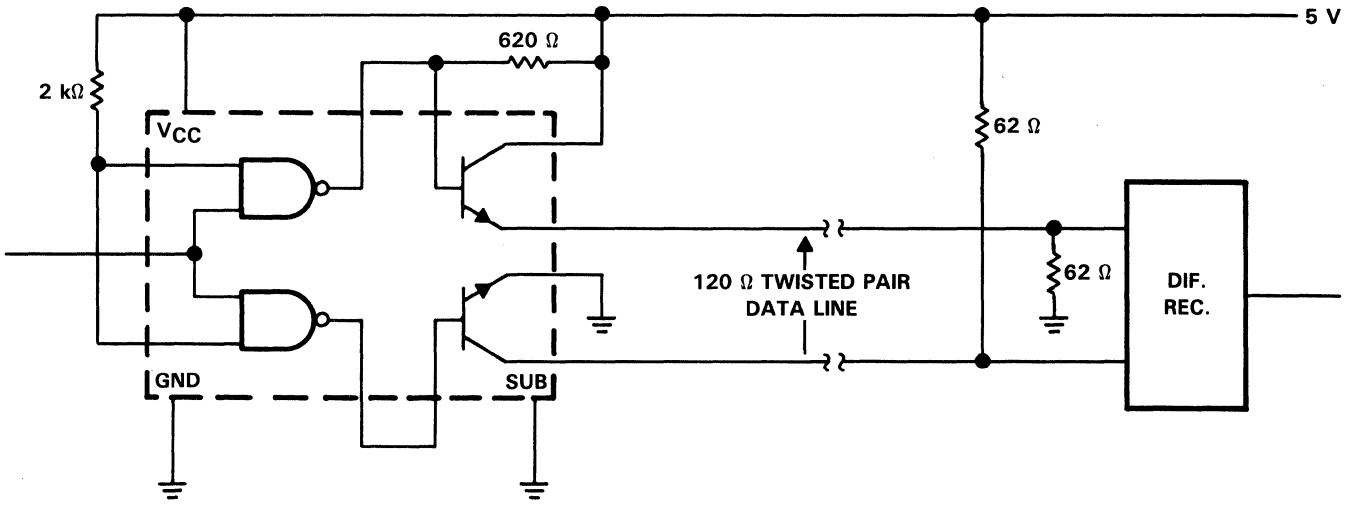
Figure 10-66. Data and Enable Control Pulses



(a) SN75450B AS DUAL SOURCE-MODE LINE DRIVER



(b) SN75450B AS DUAL SINK-MODE LINE DRIVERS

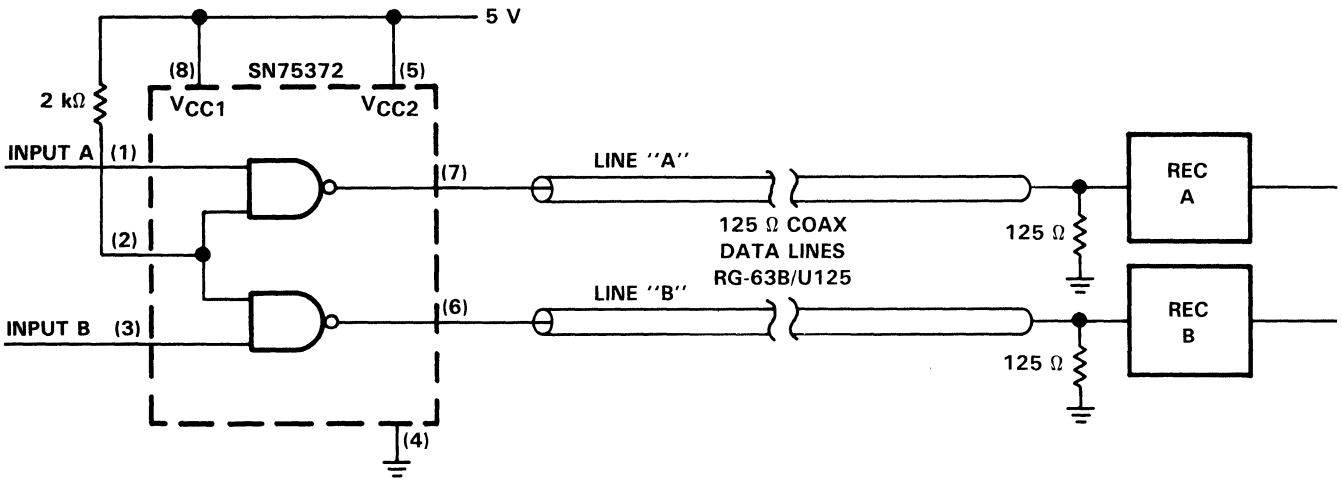


(c) SN75450B AS DIFFERENTIAL LINE DRIVER

Figure 10-67. SN75450B as Data Line Driver

result in a driver output current of 3.5 V/62 Ω or about 56.5 mA. Base current I_b is equal to 56.5 mA/50 or 1.13 mA. Base resistance R_b, for the source transistor, is (5 V-4.3 V)/ 1.13 mA or about 620 Ω.

With any of these three drive modes, there are some limitations on speed due to the long RC time constants of line capacitance and termination resistance. Rather than using open-collector or emitter-follower output drive devices when high speed operation is desired, a totem-pole output driver is recommended. The SN75372 is a dual driver with totem-pole outputs. This device will drive single ended coaxial or twisted-pair lines at high data rates as illustrated in Figure 10-68. With transition times less than 12 ns, the SN75372 drivers can transmit data at frequencies up to 20 MHz.



For Data Transmission Rates Up to 20 MHz

Figure 10-68. High-Speed Coaxial Data Line Transmission

Section 11

Data Acquisition Systems

A data acquisition system in the broad sense could mean any method used for obtaining or acquiring any type of data, however, a data acquisition system (DAS) usually denotes a group of electronic devices that are connected to perform the measurement and quantization of analog electrical signals for digital processing. Stated another way, the DAS is the interface between analog and digital electrical signals. Although most physical attributes are analog in nature, many are not electrical and must be converted to the electrical world using sensors or transducers. For the purposes of this text this conversion will be assumed and all inputs will be considered electrical.

TYPICAL SYSTEMS

A digital voltmeter is a DAS that simply displays its output as a numerical value.An automatic process control system containing a large computer and a DAS provides a greater range of data acquisition functions. The trend seems to be for a DAS to be coupled with a microprocessor or minicomputer in most applications today. A typical system with a minicomputer is illustrated in Figure 11-1.

Key parts of the system include:

Analog Multiplexer — This function allows the selection of any one of several analog signals.

Signal Conditioner — This function usually follows the multiplexer, but could be used on any or all input signal lines, to prepare the signals for conversion. The conditioning required might include one or more of the following: linear or logarithmic amplification, filtering, peak detection, sample-and-hold, or track-and-hold.

Analog-to-Digital (A/D Converter) — The A/D converter translates the analog signal to a digital format.

I/O Controller — The I/O controller generates the system timing and controls the memory READ/WRITE functions.

Minicomputer — An operational computer system based on a microprocessor chip. It contains memory (storage) and is controlled by software.

Output Buffer — The output buffer combines the data with the proper signal format for output to the specific peripheral devices. The output buffer is also called a peripheral controller.

Peripheral — Different microcomputer-type output devices such as a line printer, floppy-disk, or magnetic tape storage unit.

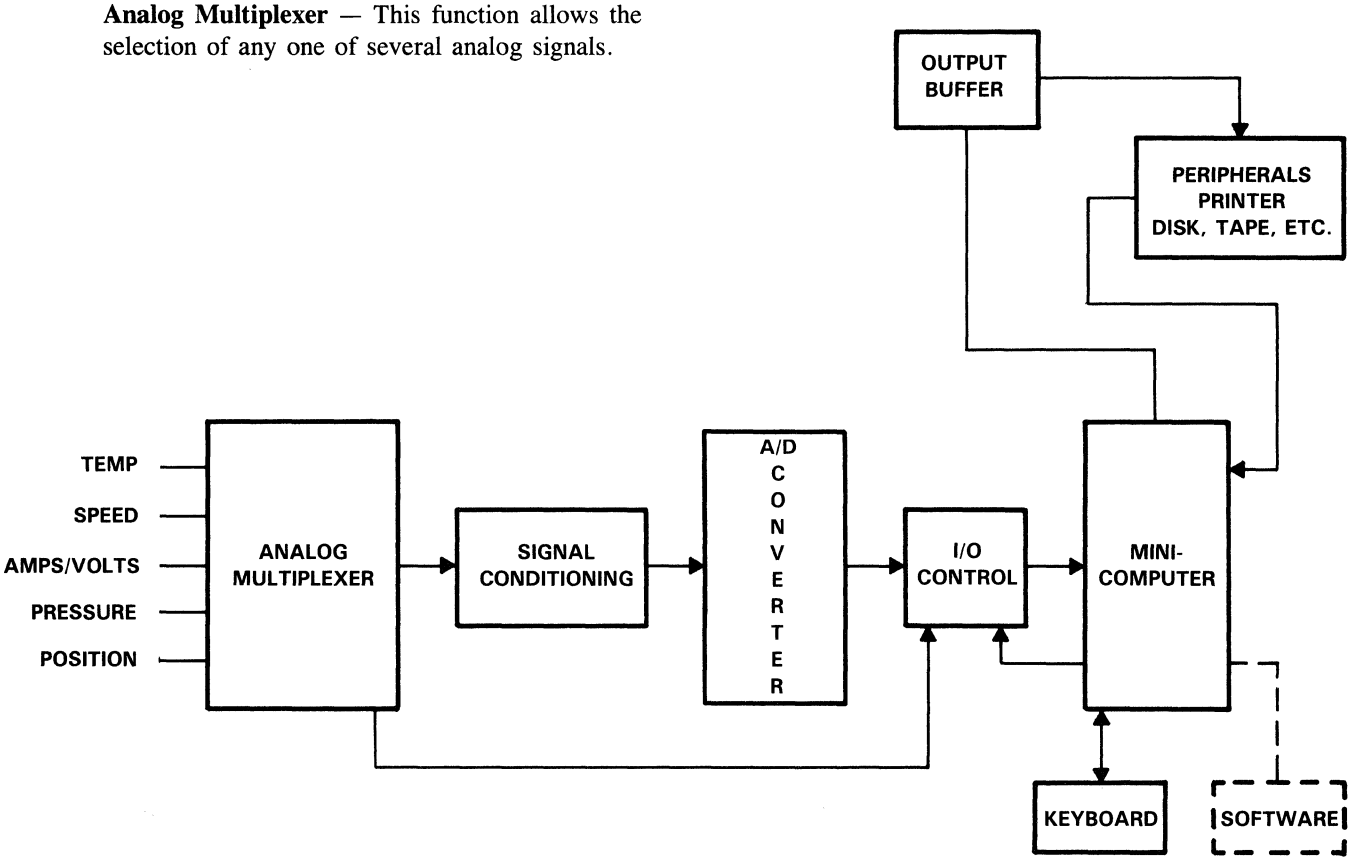


Figure 11-1. Typical Automated DAS

MICROPROCESSOR-CONTROLLED DAS

The latest trend in test instrumentation is to include a microprocessor in the equipment as shown in Figure 11-2. This system gives the user more flexibility and programming power.

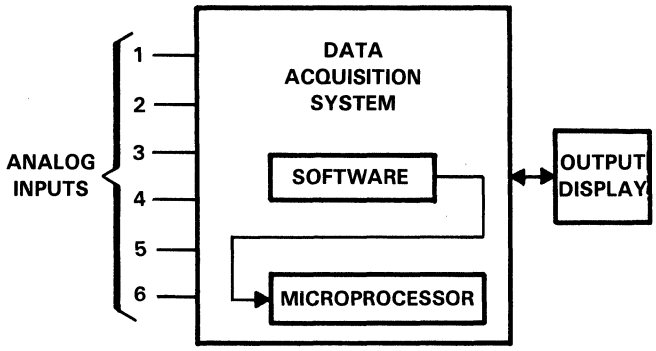


Figure 11-2. Microprocessor-Controlled DAS

A different configuration is shown in Figure 11-3. In this system each channel has its own signal conditioning and A/D converter. This allows processing of analog signals from very diverse sources or when high calibration accuracy is required.

BASIC USES OF A DAS

Any hardware system that is analog and digital in nature will have a DAS included in the system. The potential use of such a system will include four broad areas:

1. Data Logging
2. Signal Analysis
3. Automated Testing
4. Process Control

DATA LOGGING

Data logging involves not only measuring the analog inputs but also translating the results to digital signals and storing the data for further processing or analysis. Figure 11-1 shows such a system. These functions may be performed at precise intervals and at accuracies beyond a person's capability of doing it manually. Present data logging equipment is highly portable and very automated. When in remote locations very little operator attention is required.

SIGNAL ANALYSIS

Many processes used today generate time-varying signals from which data must be extracted. Examples are radar tracking, air traffic control, seismic exploration, and patient monitoring in hospitals. The most common method of analyzing this information is to translate it into an appropriate Fourier series transform for analysis in the frequency domain. Low cost computer hardware coupled with fast Fourier transforms (FFT), makes this approach feasible. Growth in this area is limited only by the cost of computer storage, speed of the computer, and the data acquisition hardware.

PROCESS CONTROL

For many years process control systems were human-controlled. Today, the DAS is a way of life. The process monitoring systems presently in use may monitor hundreds of inputs, display the readings, make calculations, and provide instant data feedback to the operator. The operator takes appropriate action based on the computer output. As computer equipment becomes more complex, more decisions are made by the system. See Figure 11-4 for a typical computer-automated process control system.

BASIC SAMPLING CONCEPTS

For a data acquisition system to function, the input signal must be sampled. Sampling may be defined as measuring a continuous function at discrete time intervals. These sampled signals represent some analog parameter converted to a series of discrete values.

A typical data acquisition sampling system is shown in Figure 11-5 and is made up of these major processes:

1. SAMPLING — the act of measuring a continuous function at discrete time intervals

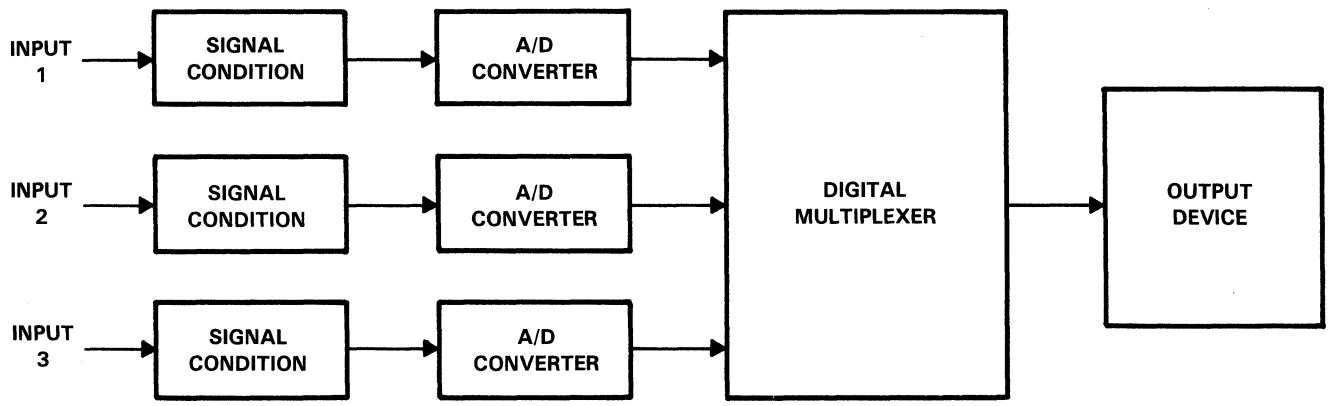


Figure 11-3. DAS with Conditioning and A/D Converter for Each Input

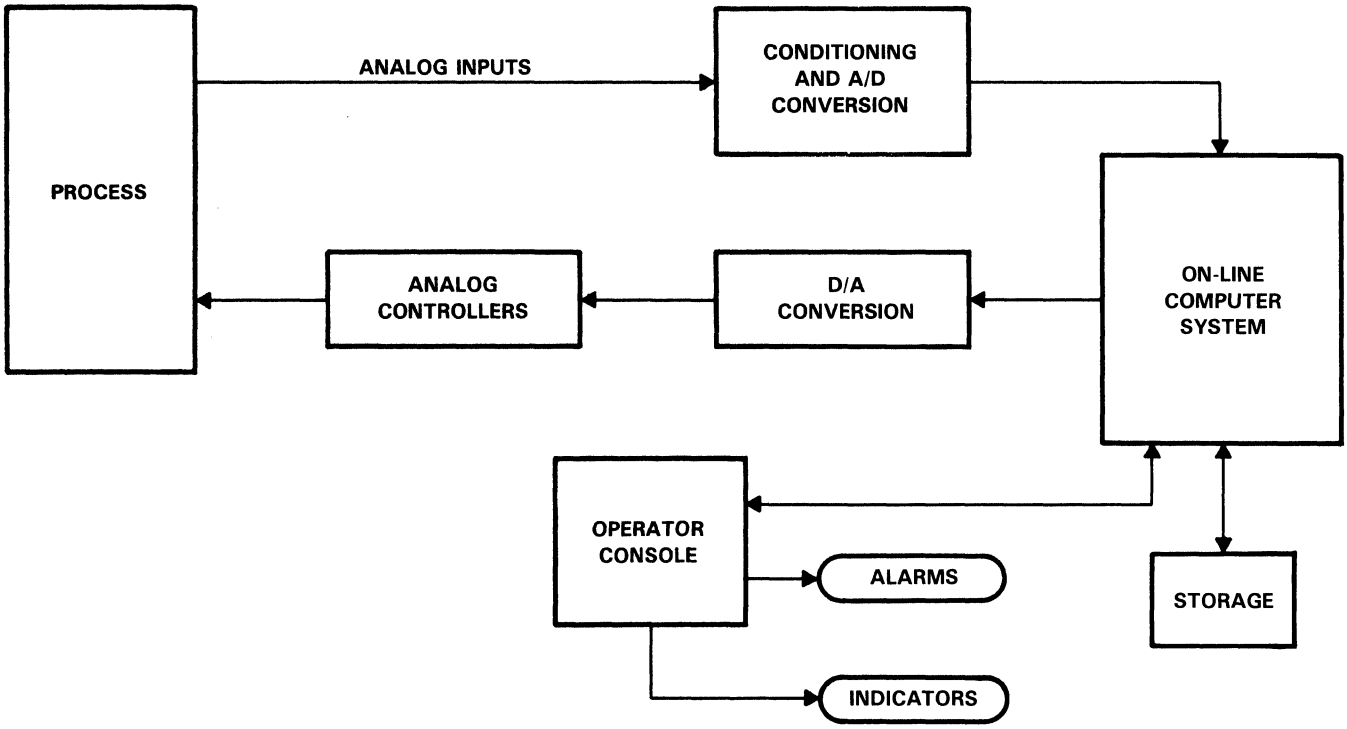


Figure 11-4. Computer-Automated Process Control

2. QUANTIZATION — approximating the linear curve by a series of stair-step values called levels
3. DIGITAL PROCESSING — evaluating the linear function as a series of discrete values represented by ones and zeros
4. RECOVERY — by the use of a D/A converter, returning the processed information to an analog form.

Besides the required number of bits (or quantization levels), the only other major problems are proper A/D conversion and the conversion of the digital signal back to analog.

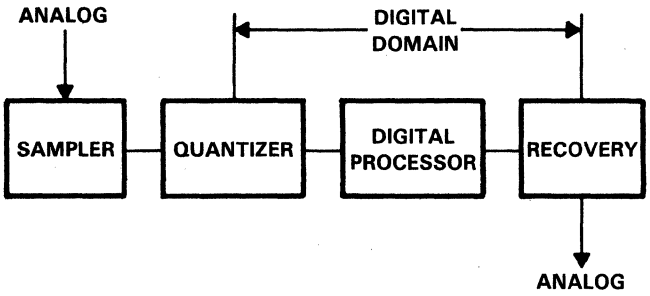


Figure 11-5. Data Acquisition Sampling System

TYPES OF SIGNALS

Before designing a data acquisition system and applying these sampling concepts, we must determine the nature of the signal to be processed. Is it dc or dynamic? Is it steady or random? What are the dynamic range, frequency range, and noise characteristics?

DC SIGNALS

While it may seem strange at first, dc signals too are sampled. In many systems the dc power supplies are monitored to keep them within tolerance. The system must be designed to compensate for undesirable noise signals sometimes present on the input being sampled.

Signal averaging is often a solution to this problem. In using this approach, a large number of measurements of the combined dc/noise signals is made and their sum is divided by the number of measurements. The sample rate should be relatively slow to minimize the effects of random noise signals. Another method used when sampling a dc signal containing noise would be to remove the noise with a low-pass filter. Often a combination of both averaging and filtering are used.

DYNAMIC SIGNALS

The majority of signals we are interested in are dynamic in nature. These signals are constantly changing, often in an unpredictable manner. Dynamic signals may be represented and analyzed in either the time domain or in the frequency domain.

The two major classes of dynamic signals are:

1. Deterministic signals — those that have known characteristics and can be described by mathematics.
2. Random Signals — those whose behavior is highly unpredictable.

DETERMINISTIC SIGNALS

Both periodic signals and transients are classified as deterministic signals. Periodic signals repeat at regular

intervals, while transients are irregular in occurrence and decay to a zero value after a length of time.

The simplest periodic waveform is a sine wave. While both the time and frequency domain plots are simple, they prove that even the sine wave has representations in both domains (Figure 11-6).

A somewhat more complex plot is shown in the typical periodic function in Figure 11-7. This illustrates several harmonically, time-locked sinusoidal signals. The time domain plot is shown at (a) while (b) depicts the frequency-domain magnitude plot containing a dc component and three other discrete frequency components at f1, f2, and f3. These plots are in the form of discrete line spectra, which characterize periodic waveforms.

From a data acquisition point of view, one of the most important periodic waveforms is shown in Figure 11-8. This illustrates a rectangular pulse train with its corresponding frequency spectrum.

The rectangular pulse train illustrates an actual, finite-width sampling function. If the pulse train rep rate increases (T decreases), the number of spectral lines decreases. As the pulse width decreases, the zero crossings move out, extending the frequency content over a wider range.

RANDOM SIGNALS

As defined, the exact value of a random signal cannot be predicted in advance. Most signals we deal with fall into this class. The random signal is not repeatable, therefore its time function is aperiodic and its frequency plot is a "closed" spectrum. See Figure 11-9 which illustrates a band-limited nonperiodic signal.

These are the types of signals that will be encountered in everyday use of a data acquisition system.

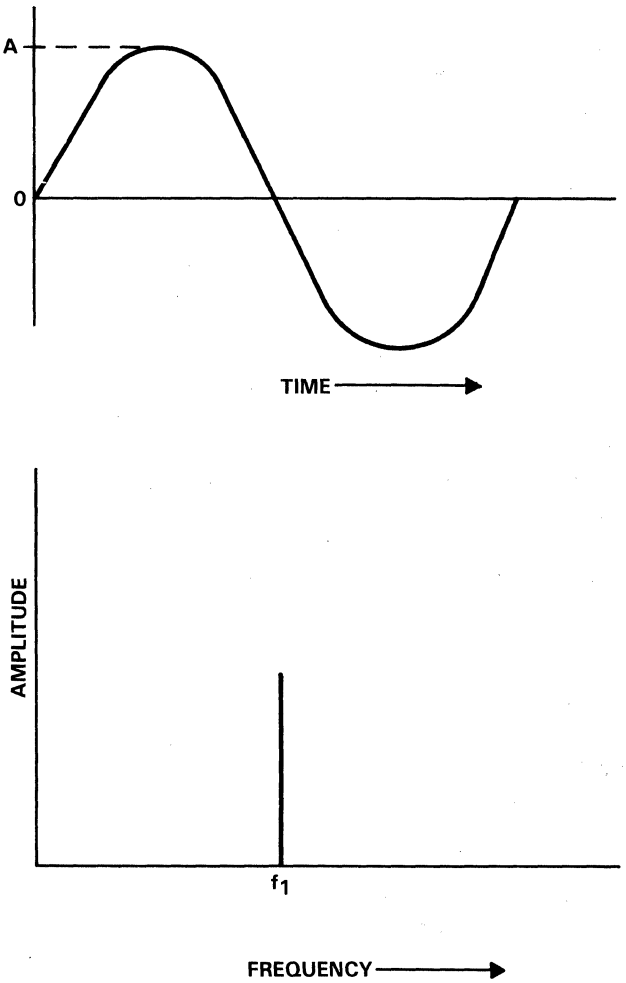


Figure 11-6. Time and Frequency Domain of a Single Sine Wave

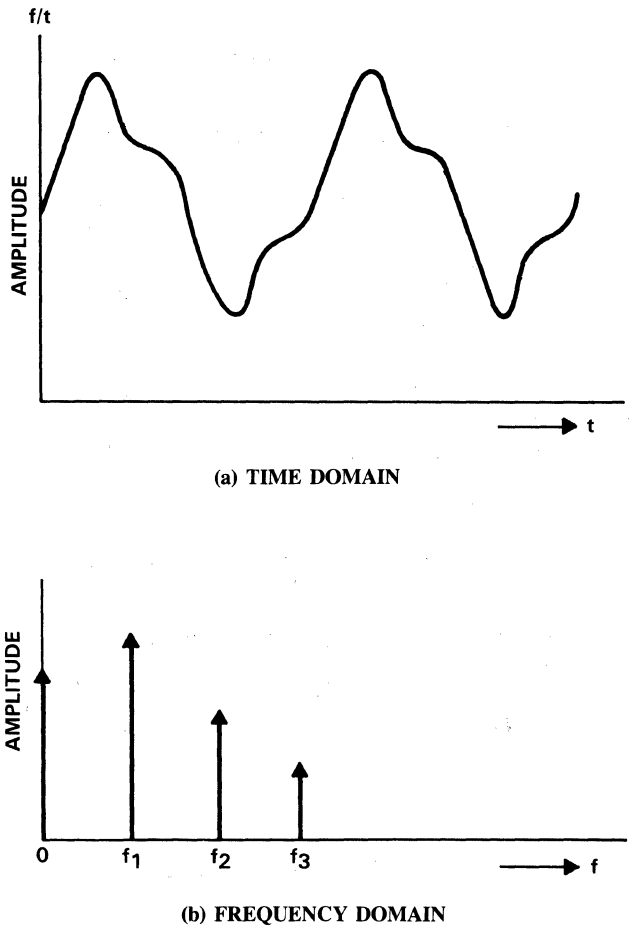


Figure 11-7. Typical Periodic Function

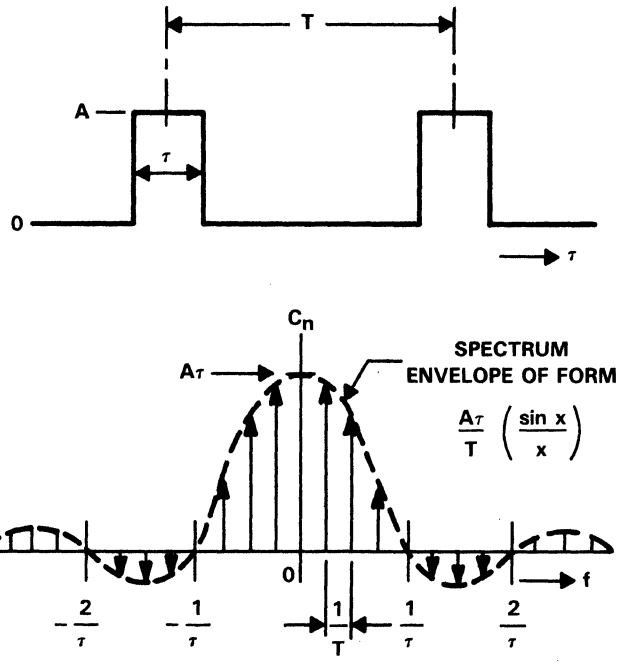


Figure 11-8. Rectangular Pulse Train with Frequency Spectrum

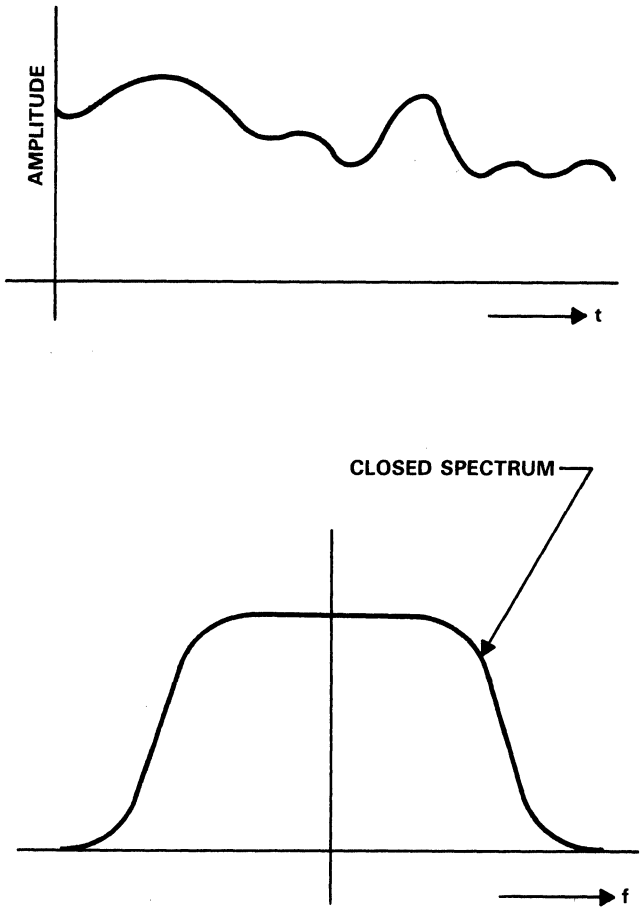
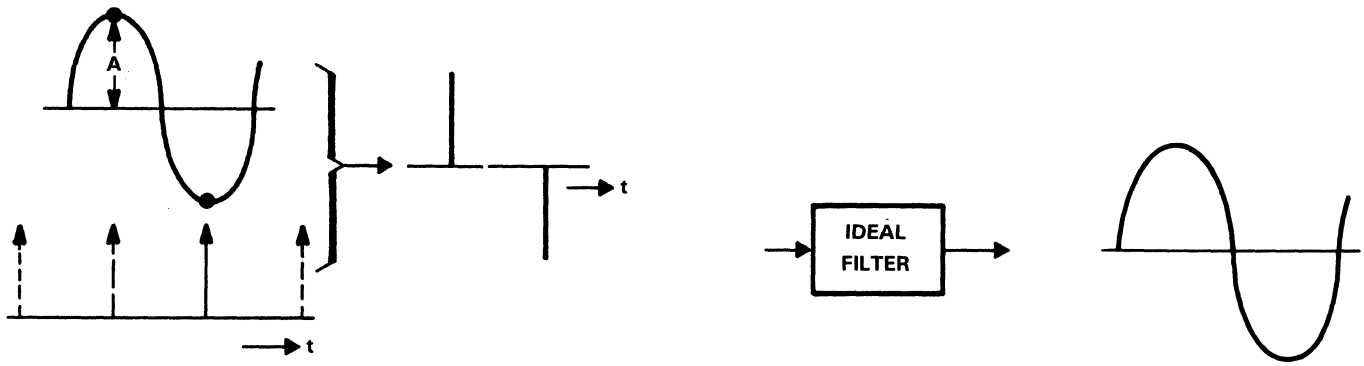


Figure 11-9. Band-Limited Nonperiodic Signal



(a) SAMPLE FUNCTION (b) SAMPLED FUNCTION (c) RECOVERY (d) RECOVERED SIGNAL

Figure 11-10. Basics of the Sampling Theorem

FREQUENTLY USED TERMS AND CONCEPTS

THE SAMPLING THEOREM

The sampling theorem states that signals with a finite bandwidth of f-hertz can be described by sampling the signals at instants separated by T = 1/2f seconds. Basically, this means the signal must be sampled at a rate at least twice the frequency of the highest frequency in the spectrum being analyzed. This concept is shown in Figure 11-10.

Here, the sine wave is sampled at its positive and negative peaks. Part (b) shows the sampled function with respect to time. Part (d) shows the original sine wave reproduced after passing it through an ideal "box" filter (c).

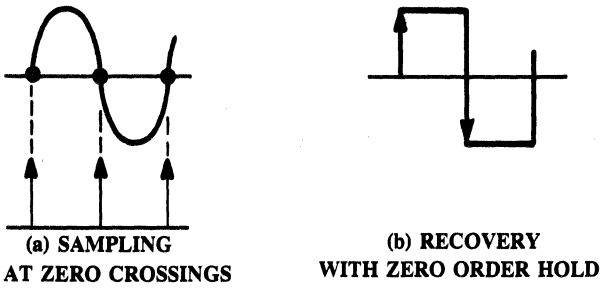


Figure 11-11. Sampling Theorem Problems

A number of difficulties can occur in practice when sampling at precisely the Nyquist rate. Two problems may occur. First, if the sampling points chosen fall precisely on the zero crossings, zero output would occur. See Figure 11-11(a).

The second difficulty arises in attempting to build an ideal filter that cuts perfectly above the highest frequency, f. Consider what happens if the reconstruction filter is a simple D to A converter (zero-order hold). As seen in Figure 11-11(b), the square wave has many more frequencies than the original single sine wave.

ALIASING

The dictionary defines the word alias as "an assumed name" or "to be called by another name." Likewise, the concept of aliasing means the same thing when applied to frequencies in a sampled data system. When a given frequency is sampled at a rate much lower in frequency than the original, the resultant frequency is the "alias" of the original. An example of aliasing in the time domain is shown in Figure 11-12.

The actual signal is being sampled at a rate that is somewhat less than one sample per cycle. The resultant frequency is about one-third the original signal. If we could accurately read the waveforms in Figure 11-12, we would find:

$$f(alias) = f(actual) - f(sample)$$

In the time domain, the pulses spread apart. In the frequency domain, the spectra move closer together and eventually overlap as in Figure 11-13.

It is important to note that the aliasing is centered about a point that is equal to one-half the sample frequency or $f_S/2$.

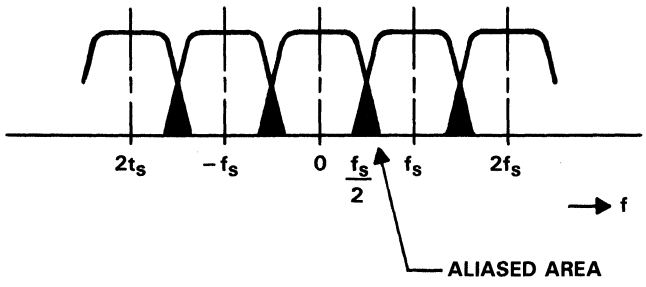


Figure 11-13. Aliasing in the Frequency Domain

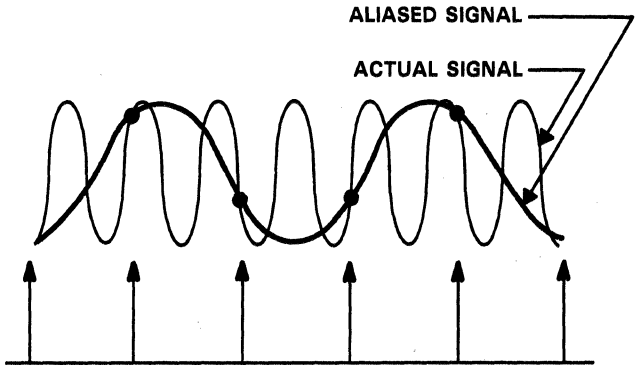


Figure 11-12. Aliasing in the Time Domain

THE NYQUIST CRITERION

When sampling an analog signal, the Nyquist criterion must always be followed. The Nyquist criterion, named after the individual who discovered it, states that the sampling frequency must be greater than twice that of the highest frequency to be sampled ($f_S > 2f_h$). F_S is the sample frequency and f_h is the highest frequency to be sampled.

ALIASING FILTER

The signals of interest usually contain noise which is much wider in bandwidth than the frequencies of interest. Unless some type of filtering is used, the noise folds over and back into the useful spectrum. The obvious solution is then to add a presampling or "anti-aliasing" filter prior to sampling. Figure 11-14 (a) and (b) shows the removal of aliasing with a presampling filter.

To illustrate the point, a "box" filter is shown. Although this type of filter is impossible to construct, it shows that the spectra no longer overlap. In practice, complex filters introduce time delay and are expensive to build. In a multichannel system, each channel might have a filter prior to the multiplexer and the system cost would increase significantly. The final solution results from a combination of sample rate selection and presample filtering.

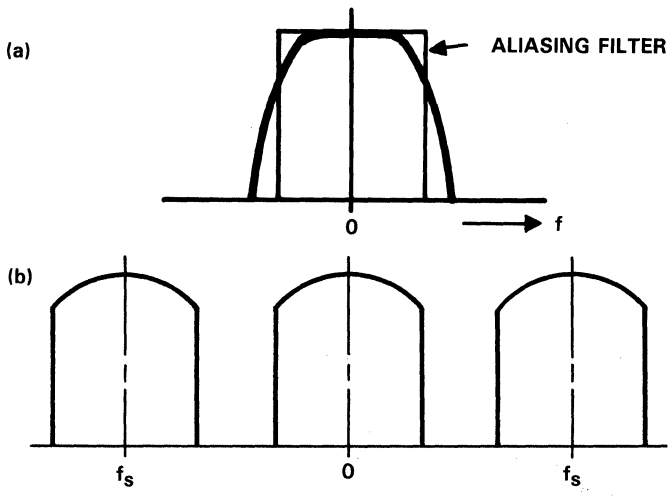


Figure 11-14. Removal of Aliasing with a Presampling or Aliasing Filter (a) and Result (b)

QUANTIZATION

In order for a computer or other digital equipment to process signals, they must first be converted from the analog domain to the digital domain. This process is called quantization. Quantization may be defined as the conversion of an input function which may have values in a continuous range to an output that has only discrete values.

Quantization is sometimes combined with sampling as the operations occur simultaneously. The transfer function for a typical quantizer or A/D converter is found in Figure 11-15.

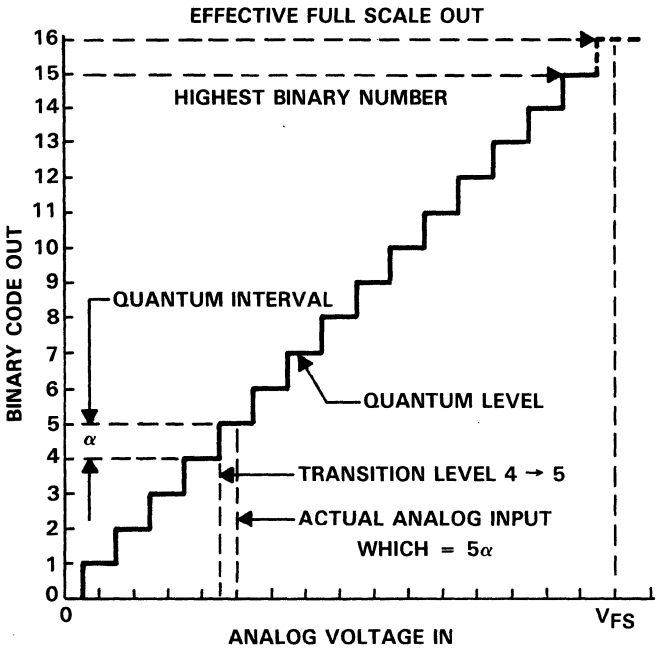


Figure 11-15. Transfer Function for 4-Bit Binary (16-Level) Quantizer

The horizontal scale represents the analog input voltage which may be any value between zero volts and the full-scale value, V_{FS}. The output can exist only as one of 16 discrete values from zero to 15. This "staircase" output has "flats" which represent the digital output code. These "flats" represent the quantum levels. For a binary-based (power-of-2) quantizer, the quantum interval is defined as:

$$\alpha = \frac{V_{FS}}{2^n}$$

where:

V_{FS} = full-scale voltage input
2 = binary number base
n = number of bits (binary)
2^n = number of quantizing intervals.

For the 4-bit quantizer shown in Figure 11-15, the quantum interval is:

$$\alpha = \frac{V_{FS}}{2^n} = \frac{V_{FS}}{2^4} = \frac{V_{FS}}{16}$$

The steps continue to double in number and halve in size as the number of quantizer bits increase, as shown in Table 11-1.

Table 11-1. Binary Steps Per Bit

n	Steps
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1,024
11	2,048
12	4,096
13	8,182
14	15,384
15	32,768
16	65,536

BINARY CODES

Straight and Offset Binary Codes

Several binary codes are commonly used. The two most common are straight binary and offset binary as found in Table 11-2.

Table 11-2. Straight and Offset Binary Codes

	Bit Position				Level	
	2^3	2^2	2^1	2^0	Straight Binary	Offset Binary
Straight Binary Zero →	0	0	0	0	0	−7
	0	0	0	1	1	−6
	0	0	1	0	2	−5
	0	0	1	1	3	−4
	0	1	0	0	4	−3
	0	1	0	1	5	−2
	0	1	1	0	6	−1
Offset Binary Zero →	0	1	1	1	7	−0
	1	0	0	0	8	+0
	1	0	0	0	9	+1
	1	0	1	0	10	+2
	1	0	1	1	11	+3
	1	1	0	0	12	+4
	1	1	0	1	13	+5
	1	1	1	0	14	+6
	1	1	1	1	15	+7

Straight binary is a unipolar code where 0000 is equal to 0 (also analog zero) while 1111 is equal to level 15. Offset binary is a bipolar code which has 0000 equal to −7 and 1111 equal to +7. For this situation, the most significant bit is the sign bit, with 0 = minus(−) and 1 = plus(+). Actually, there are no "zero" levels in the offset binary code. Rather, there are two near-zero levels, each half a quantum interval from true analog zero.

One's and Two's Complement Codes

Two more codes that are widely used and are more compatible with digital computers are the one's complement and two's complement binary codes. Although both codes are bipolar, they differ chiefly in the positioning of the true analog zeros.

The one's complement code is identical to the offset binary code with the exception that the sign bit is inverted. In this case, 1 is negative and 0 is positive. Like offset binary, this system has two zero levels.

The two's complement code differs in that it has only one zero level and it is coincident with the 0000 code. There is also one more negative level (−8) than positive (+7). The sign is also the complement of that for offset binary. See Table 11-3.

Table 11-3. One's and Two's Complement Binary Codes

	Bit Position				Level	
	2^3	2^2	2^4	2^0	Two's	One's
	1	0	0	0	−8	−7
	1	0	0	1	−7	−6
	1	0	1	0	−6	−5
	1	0	1	1	−5	−4
	1	1	0	0	−4	−3
	1	1	0	1	−3	−2
	1	1	1	0	−2	−1
	1	1	1	1	−1	−0
One's Zero →						
Two's Zero →	0	0	0	0	0	+0
	0	0	0	1	+1	+1
	0	0	1	0	+2	+2
	0	0	1	1	+3	+3
	0	1	0	0	+4	+4
	0	1	0	1	+5	+5
	0	1	1	0	+6	+6
	0	1	1	1	+7	+7

All three bipolar codes discussed thus far are variations of straight binary and require offsetting of analog zero with respect to code levels or inversion of the sign bit.

Absolute-Value-Plus-Sign Code

Another binary code, popular in the 1970s, is the absolute-value-plus-sign code shown in Table 11-4.

In this code, the lower three bits are exactly the binary representation of the associated level, e.g., 111 = 7. Therefore, the lower three bit codes reflect about zero level (+3 has the same code as −3). As in other bipolar codes, the most significant (2^3) bit is the sign designator.

Table 11-4. Absolute-Value-Plus-Sign Code

	Bit Position				Level
	2^3	2^2	2^1	2^0	
	0	1	1	1	−7
	0	1	1	0	−6
	0	1	0	1	−5
	0	1	0	0	−4
	0	0	1	1	−3
	0	0	1	0	−2
	0	0	0	1	−1
	0	0	0	0	−0
Zero →					
	1	0	0	0	+0
	1	0	0	1	+1
	1	0	1	0	+2
	1	0	1	1	+3
	1	1	0	0	+4
	1	1	0	1	+5
	1	1	1	0	+6
	1	1	1	1	+7

Gray Code

Another code used by some quantizers is the Gray code. See Table 11-5.

Table 11-5. The Gray Code

	Bit Position				Level
	2^3	2^2	2^1	2^0	
	0	0	0	0	0
	0	0	0	1	1
	0	1	0	1	2
	0	0	1	0	3
	0	1	1	0	4
	0	1	1	1	5
	0	1	0	1	6
	0	1	0	0	7
Midpoint →					
	1	1	0	0	8
	1	1	0	1	9
	1	1	1	1	10
	1	1	1	0	11
	1	0	1	0	12
	1	0	1	1	13
	1	0	0	1	14
	1	0	0	0	15

This code has two unique features. First, like the absolute-value-plus-sign code, the lower three bits reflect about the scale midpoint. Secondly, only one bit changes as the code progresses from one level to the next. The Gray code is used for most types of electromechanical quantizers and for cyclic-type A/D converters.

BCD Code

The final code to be discussed is the 8421 binary-coded decimal, which is commonly referred to as BCD. This code is used when direct decimal readouts are necessary. Although binary in form, the codes exist only in decades (0 to 9). When the decade limit is exceeded, the code carries to the next higher decade. See Table 11-6.

Table 11-6. The 8421 Code

8	4	2	1	Level
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Each increasing decade is identical to the figures shown in Table 6, but has a 10X magnifier associated with it. The quantum interval for 8421 BCD code is calculated as:

$$\alpha = \frac{V_{FS}}{10^m}$$

where:

V_{FS} = full scale voltage input
m = number of decades
10^m = number of quantum levels.

SIGNAL RECOVERY

The sample data process cannot be considered complete until a function called recovery is effected. The recovery function must accurately reconstruct the original time signal or a derivative of it. The two main sources of errors in recovery are errors of omission and errors of commission.

An error of omission is shown in Figure 11-16. The dashed line shows the sampled analog signal while the arrowheads depict the specific sampling points. A certain amount of signal trend information is missing in between these points. Once quantization has occurred and the samples have only discrete values, difficulties are compounded.

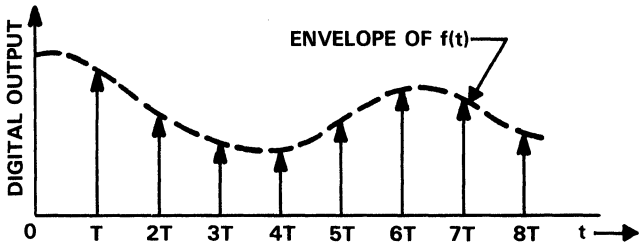
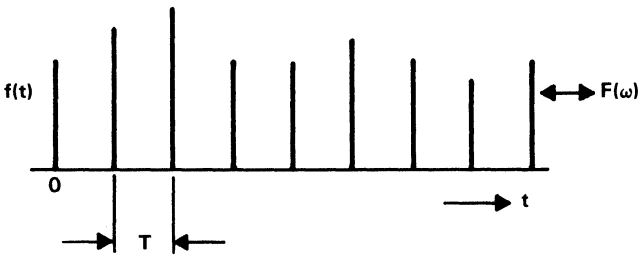


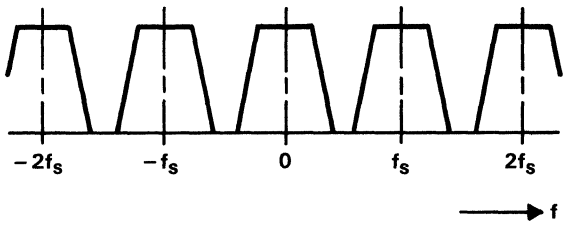
Figure 11-16. Typical Digital Processor Output, f(t) [Error of Omission]

The second error problem is the error of commission. See Figure 11-17. The signal sampling is shown in Figure 11-17(a). When examining the frequency spectrum in Figure 11-17(b), not only is the original signal spectrum present, but many additional spectra are also present and centered about multiples of the sample frequency. If these extra outputs are not eliminated, erroneous results will occur.

The ideal recovery function would be a rectangular or "box" filter. Unfortunately, it is not physically possible to implement a filter with these ideal characteristics.



(a) SAMPLED INPUT

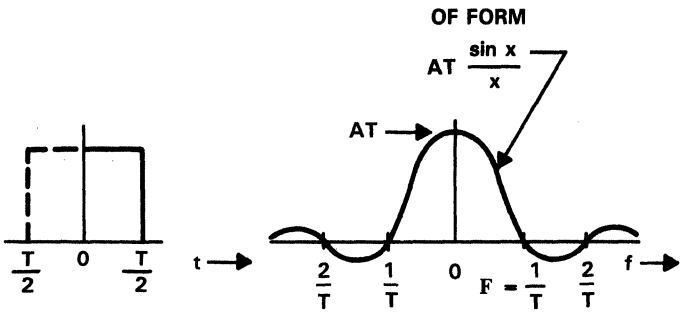


(b) FREQUENCY DOMAIN RESULT

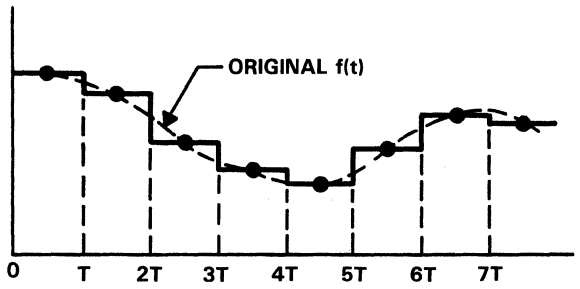
Figure 11-17. Error of Commission

One of the most common methods of reconstruction is the zero-order hold function as shown in Figure 11-18.

Figure 11-18(a) shows that the time and frequency representation for the zero-order hold function is rectangular in the time domain and (sin x)/x in the frequency domain. Figure 11-18(b) shows the final result in the time domain. This output is instantly recognized as that of a typical digital-to-analog (D/A) converter. While this reconstruction process results in some error, the worst case error would occur at zero crossing of the sine wave at the highest frequency in the original signal.



(a) RECOVERY FUNCTION, IN BOTH DOMAINS



(b) RECONSTRUCTED FUNCTION, f(t)

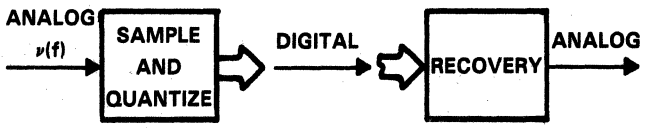
Figure 11-18. Staircase or Zero-Order Hold Recovery

A DATA ACQUISITION EXAMPLE

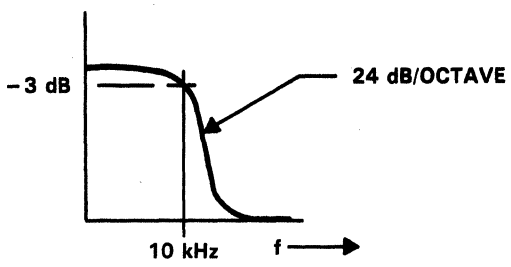
The following example will help to tie together the concepts discussed thus far. A simple digital data system is shown in Figure 11-19(a).

Assume the analog input has the characteristics of a fourth-order Butterworth spectrum and the highest frequency of interest is at 20 kHz. The four initial requirements for our example are:

1. Dynamic range >70 dB
2. Aliasing error <0.1%
3. Recovery error <0.1%
4. Aperture error <0.1%



(a) EXAMPLE SAMPLE DATA SYSTEM



f	%A	RESPONSE
10 kHz	70.7	-3 dB
20 kHz	4.4	-27 dB
40 kHz	0.28	-51 dB
80 kHz	0.018	-75 dB
120 kHz	0.0044	-87 dB
160 kHz	0.0011	-99 dB

(b) CHARACTERISTICS OF FOURTH ORDER INPUT

Figure 11-19. Data Acquisition Example

The parameters to be determined are:

1. Number of quantization levels (bits)
2. Sample rate
3. Sampling aperture operator
4. Recovery operator

The first unknown to determine is the number of bits. The system dynamic range has been specified as 70 dB, which is equivalent to the ratio of 3162 to 1. The closest larger binary number is 4096, or 12 bits, which is equal to 72 dB. Thus, a 12-bit A/D converter would be chosen.

The next unknown to consider is the sampling rate. This becomes somewhat more complex as two requirements must be satisfied to determine this parameter; one for aliasing and one for recovery error. Consider the aliasing problem first. It requires the error due to folding to be less than 0.1% of the expected value at the highest frequency of interest, 20 kHz. Figure 11-19(b) shows that at 20 kHz, the signal levels are 4.4% of the dc value. The overlap of the first harmonic spectrum must not be greater than 0.1% of the 4.4% value. This then is the 0.0044% point on the chart in Figure 11-19(b) or −87 dB. This overlap occurs when the first spectrum contribution of f_S − 120 kHz coincides with the 20 kHz point on the original spectrum. This is shown in Figure 11-20.

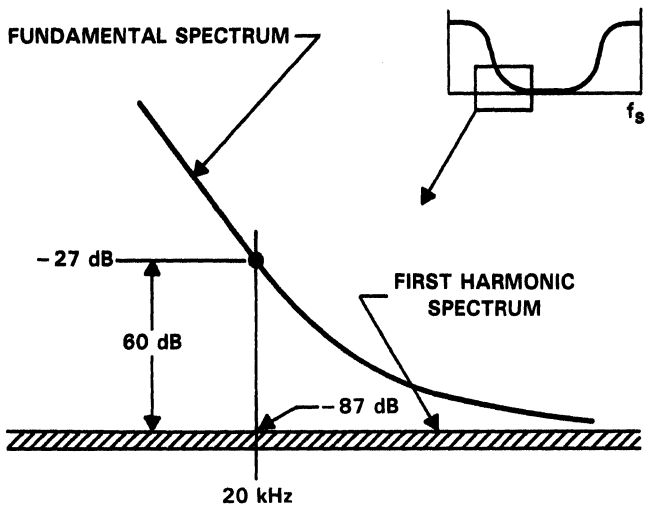


Figure 11-20. Effect of Aliasing, f_S = 120 kHz

This shows a 1000 to 1, or 60 dB, difference between the two spectra. The sample rate to satisfy this requirement must be equal to or greater than:

$$120 \text{ kHz} + 20 \text{ kHz} = 140 \text{ kHz}$$

Using this analogy, a 140 kHz sampling frequency will satisfy the aliasing error requirement of this example. Before selecting 140 kHz as the sampling rate, consider the impact of the recovery error requirement. Assume we choose the recovery filter to have the same characteristics as the input spectrum, namely a 4-pole Butterworth. To meet an rms recovery error of 0.1%, a 4-pole Butterworth filter spectrum must have 36 samples per cycle of a 3-dB bandwidth. Calculate as follows:

$$\frac{f_S}{f_{3dB}} = 36 \text{ samples per cycle}$$

where:

f_S = sampling frequency
f_{3dB} = 3 dB down point or 10 kHz
$f_S = 36 \times 10 \text{ kHz} = 360 \text{ kHz}$

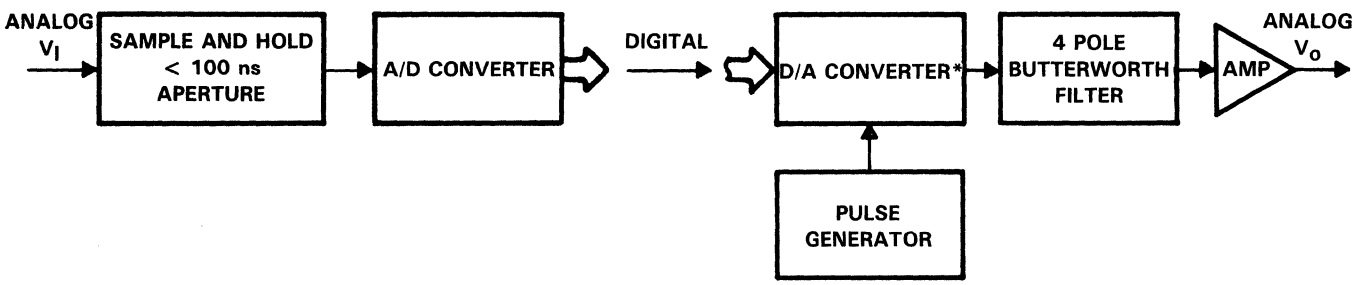
To meet the original requirements of our example, at a sampling rate of 360 kHz, aliasing is negligible. A suitable selection for this example would be a 12-bit, 500 kHz, successive approximation A/D converter.

The third consideration is aperture error and a decision must be made concerning whether to use a sample-and-hold function ahead of the converter. The basic aperture of an A/D converter is:

$$\text{Aperture} = \frac{1}{f_S} = \frac{1}{500 \text{ kHz}} = 2 \ \mu s$$

An aperture like this would be equivalent to placing a (sin x)/x filter in the system, with the first zero crossing at 500 kHz. This would cause between one and 2% attenuation at 20 kHz. To achieve our design requirement of less than 0.1%, a sample-and-hold with an aperture of less than 100 ns would be required.

The final requirement to contend with is the recovery operator. The final recovery filter was previously chosen to be a 4-pole Butterworth. Before continuing, the data must first be converted from digital binary numbers to analog values. If we utilized a simple D/A converter (zero-order hold) with 500 kHz update rate ahead of the filter, we still have the (sin x)/x filtering problem. In fact, it will be more severe than the final recovery filter. One solution would be to utilize a D/A converter with return-to-zero outputs of less than 100 ns in width. The final system configuration is shown in Figure 11-21.



*100 ns return-to-zero

Figure 11-21. Complete Data Acquisition System

SUMMARY OF DESIGN CONSIDERATIONS

There is usually more than one solution for any specific A/D design situation. Filters other than the 4-pole Butterworth filter could be used in recovery. Tighter aliasing error requirements could have greatly affected the sample rate. Each problem must be considered individually, and then a decision made after considering the hardware available and the parametric requirements of the specific application.

To implement a successful design, you must know what the input signal spectrum looks like, what you ultimately wish to obtain from it, and how to apply the rules of sampling, quantization, and recovery on an individual basis.

SYSTEM PARAMETERS

To properly design a data acquisition system, the system parameters must be thoroughly defined. A large number of converter products are available today. Manufacturers may specify the parametric capabilities of devices in different ways. Two basic factors should be a key in choosing the right device for a particular application. The first is to completely define the design objectives and the second is to understand what the data sheet specifications mean. If there is any difficulty in understanding the specs, consult with the manufacturer before proceeding with the design.

UNDERSTANDING MAJOR SYSTEM PARAMETERS

Absolute Accuracy — This is an indication of the discrepancy between the data acquisition system measured value of a given input and the National Bureau of Standards measured volt. It implies that the system's voltage reference is traceable to the NBS standard and is periodically calibrated.

Relative Accuracy — This is a measure of the data acquisition system's ability to yield correct output codes, for all possible input voltages, relative to its full-scale range. It is a direct function of the system's linearity.

The most typical way of stating accuracy is:

$\pm 0.01\%$ of FSR (analog inaccuracies)

where:

FSR = full-scale reading

This term includes all the analog sources of error such as linearity, drift, and component error.

$\pm$ 1/2 LSB (quantization error)

where

LSB = least significant bit

This term is determined by the number of available quantization levels.

Precision — Precision is a measure of the system's repeatability. In other words, it is the system's ability to produce the same output code when making successive measurements of the same input value. Internal system-generated noise is one cause of poor precision.

Resolution/Dynamic Range — This is the ability of a data acquisition system to distinguish between adjacent analog input levels. A 10-bit system would be capable of distinguishing between input levels that differ by 1/1024 of the full-scale range (10 bits = 2^{10} = 1024). Resolution also defines the system dynamic range which may be stated:

1024 to 1 or (dB = 20 $\log_{10}$ 1024) = 60 dB

Overrange — When the normal full-scale voltage is exceeded on many data systems, the output continues to register the code assigned to the full-scale value.

Linearity — Two types of nonlinearity are involved. The first is integral nonlinearity, which is the maximum deviation from a best straight line drawn through the transfer curve. See Figure 11-22.

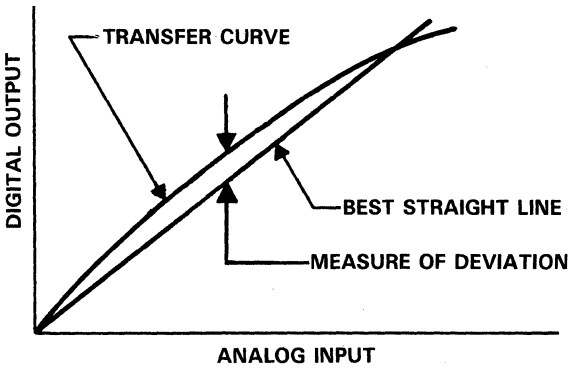


Figure 11-22. Integral Nonlinearity

Integral nonlinearity is usually specified as a percentage of full scale or in terms of quantum level (such as $\pm$ 1/2 LSB).

The second type of nonlinearity is differential nonlinearity. This is the measure of the maximum deviation of any quantum interval in the system's transfer function from the theoretical value. Differential nonlinearity may be specified as a percentage of quantum interval or LSB. See Figure 11-23.

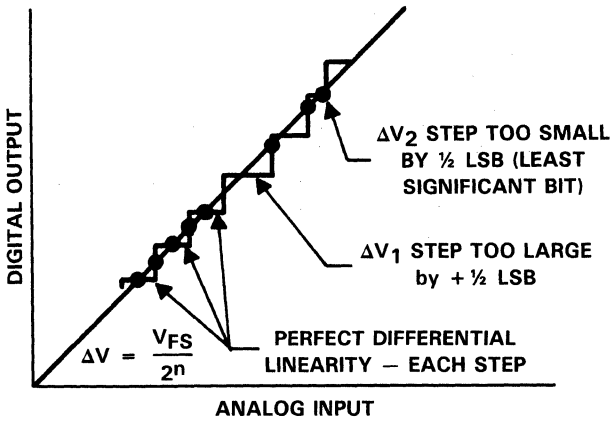


Figure 11-23. Examples of Differential Nonlinearity

Monotonicity — Monotonicity, in a data acquisition system, is a guarantee that the system's output code will continue to increase (or decrease) with a continuously increasing (or decreasing) input. This problem most likely occurs at the halfway or quarter-way points of full-scale readings.

Temperature Coefficients — Changes in ambient temperature affect a system's ability to produce accurate measurements. The two major problems are gain change and zero shift. See Figure 11-24.

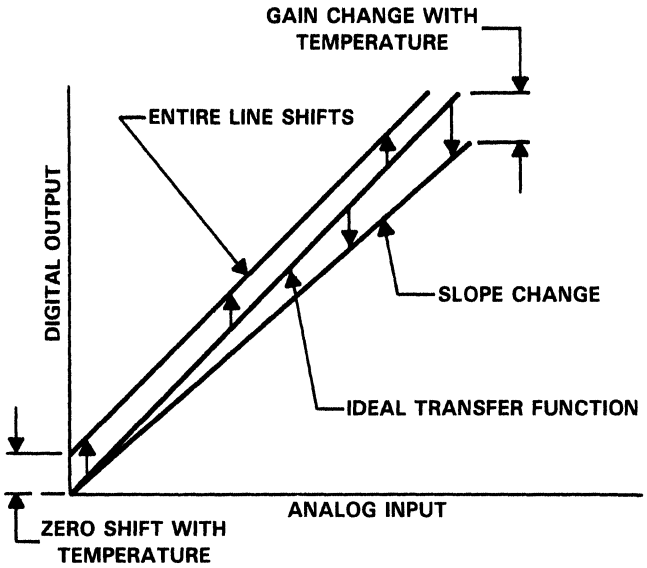


Figure 11-24. Temperature Effects on Accuracy

Temperature can also adversely affect integral and differential linearity. Temperature coefficients are factors which should not be overlooked.

Noise — Noise is a constant problem in any acquisition system. Normal noise is that noise appearing at the two measurement terminals, along with the desired signal. Common-mode noise is interference that appears simultaneously on both measurement inputs. Most common-mode noise may be attributable to the 60 Hz power line frequency.

Conversion Speed — Conversion speed provides an indication of system sampling rate, and is usually expressed in conversions per second. A communications type data acquisition system, for example, might have a conversion rate of 10 conversions per microsecond which equates to a conversion speed of 10M conversions per second.

Settling Time — This is the time between the application of a full-scale input step and the stabilization of the output to within a specified error band. Once the ringing has settled to within the error band, an accurate conversion can occur. See Figure 11-25.

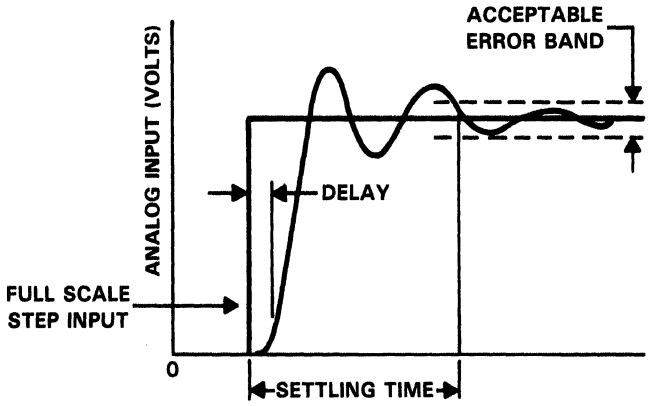


Figure 11-25. Example of Settling Time

Aperture Time — Aperture time is the width of the sampling window or the actual time the system requires to obtain a sample.

Acquisition Time — Acquisition time applies to systems containing a sample-and-hold function. It defines the time required to sample an analog signal within the specified system accuracy. A typical acquisition time would be specified to 0.1% of full-scale = 4 μs.

Hold Time/Droop Rate — This parameter also concerns systems with a sample-and-hold function. Hold time defines how long the system can hold the stored value to a given accuracy. Droop rate indicates the loss of charge per unit of time. Although both specifications are still used, droop rate is more popular.

Cross Talk — This is very important in a multichannel system. It is an indication of signal leakage from one channel to any other.

DC Input Characteristics — These characteristics are offset voltages, offset currents, and bias currents. An offset of 10 mV will shift inputs of some systems by several significant bits. Although sometimes neglected, the dc input characteristics are important in some applications and should not be overlooked.

METHODS OF A/D CONVERSION

Several types of A/D converters are available. Some feature speed of conversion, while others are known for their higher resolution. The four most widely used methods are as follows:

1. Single slope
2. Dual slope
3. Successive approximation
4. Flash and semi-flash

Each of these methods has advantages and disadvantages. Some of the primary features of these conversion techniques are shown in the following chart:

TYPE	SPEED	ERROR	RESOLUTION
Single-slope	Slow	High	Med-High
	(ms)	±1 LSB	(8—14 Bits)
Dual-slope	Slow	High	High
	(ms)	±1 LSB	(10—18 Bits)
Successive-	Med	Low-Med	Med-High
Approximation	(μs)	±0.5 LSB	(8—16 Bits)
Flash	Fast	Low-Med	Low-Med
	(μs)	±0.25 LSB	(4—8 Bits)

KEY SELECTION CRITERIA FOR A/D CONVERTERS

NUMBER OF BITS

In a digital (binary) system, each bit of information is represented by a "1" or a "0". Four bits are required to represent the decimal numbers 0 through 15 (16 different states). An 8-bit number can represent the decimal numbers 0 through 255 (256 states). It follows that with more bits, or sampling points of the input signal, the output data will be more precise. For example, a 4-bit converter could specify values between 0 and 1.0 V in 1/16-V increments, but an 8-bit converter could specify values in this same range in 1/256-V increments. Thus, more bits of output data provide higher resolution.

CONVERSION SPEED

The process of sampling and converting an analog signal value to a digital number is not instantaneous. A finite amount of time is required for the conversion process to be completed. Faster individual conversions means more conversions per unit of time. For example, a conversion speed of 1.0 ms implies 1000 conversions per second and a conversion speed of 100 μs implies 10,000 conversions per second.

CONVERSION ACCURACY

There is a limit to how closely an A/D converter can approximate a given voltage level. The A/D converter approximates the linear curve by a series of stair-step values called quantization levels. See Figure 11-26.

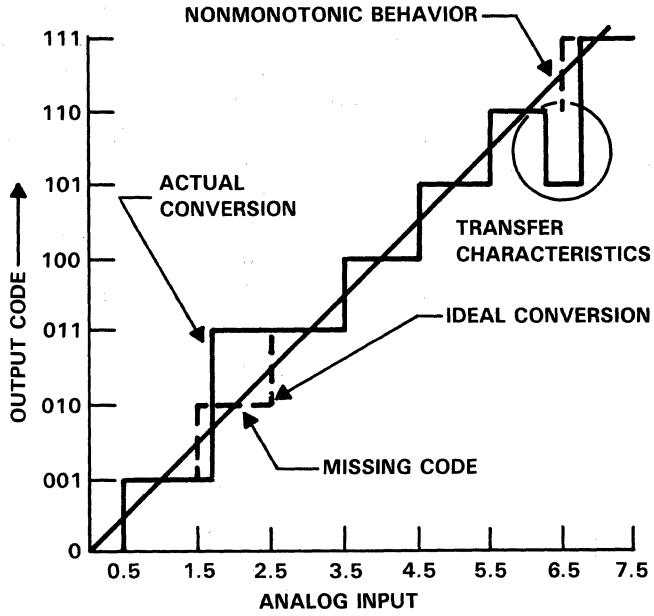


Figure 11-26. A/D Conversion Quantization Levels

Depending on when the sample is taken, the sample can be in error. The method for determining the error that can be expected from a given A/D converter is expressed relative to the number of quantization levels, specifically to the variation in LSB.

$$\text{Value of LSB} = \frac{\text{Full scale voltage}}{2^n}$$

where:

LSB = least significant bit
n = number of bits of resolution

From this we see that a 10-bit A/D converter is not as good as an 8-bit converter if the 10-bit A/D converter has an error of ±4 LSB and the 8-bit A/D has an error of only ±1/2 LSB when sampling a full-scale voltage range of 4 V. As an example, assume a 4 V full-scale range and compare an 8-bit converter with a 10-bit converter.

8-Bit Converter $\quad \text{LSB} = \frac{4\text{ V}}{2^8} = 15.6\text{ mV per step}$

10-Bit Converter $\quad \text{LSB} = \frac{4\text{ V}}{2^{10}} = 3.9\text{ mV per step}$

If the 8-bit error is ±1/2 LSB, it is accurate to ±7.8 mV. The 10-bit converter with an error of ±4 LSB is accurate to only ±15.6 mV.

The accuracy of an analog-to-digital conversion may be defined as linearity. Errors are defined and measured in terms of the analog values at which the transitions occur, in relation to the ideal transition values. Figure 11-27 shows the transition errors including offset and range errors.

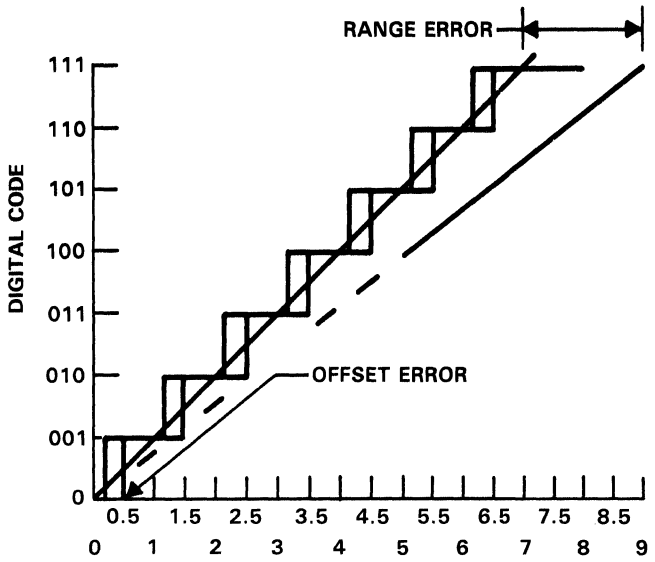


Figure 11-27. A/D Transition Errors

CONVERSION TECHNIQUES

SINGLE-SLOPE A/D CONVERTER

A single-slope integrator arrives at its digital output by comparing the unknown analog input signal to a ramp voltage generated from a reference. The ramp must be precisely controlled so that it is very linear, and takes exactly 2 raised to the n^{th} number of clock pulses to go from 0 V to full scale. By counting the number of clock pulses required to build the ramp from 0 V to the value of the unknown analog signal, a digital value of the analog signal is obtained. For example, assume a 6-bit A/D converter and a full scale reading of 5 V. See Figure 11-28.

6 Bit A/D Converter = $2^{(6)}$ or 64 increments
Full scale resolution = 64 divisions
Full scale voltage = 5 V
Analog input voltage = 34/64 of full scale
Analog input voltage = 5 V × 34/64 = 2.6 V

The requirements for a good single-slope A/D converter are:

1. A stable reference voltage to build the ramp
2. A stable clock (oscillator) to count the ramp
3. A stable and linear integrator to control the accuracy of the ramp.

Figure 11-29 shows the functional block diagram of a single-slope A/D converter.

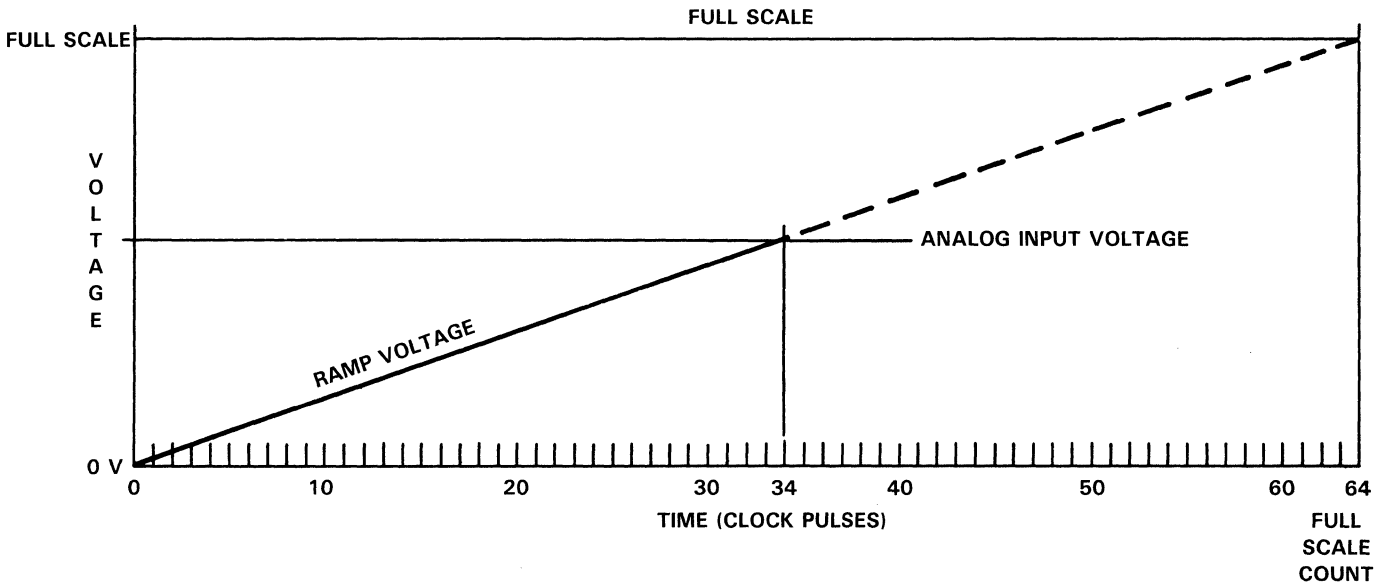


Figure 11-28. Ramp/Analog Voltage Comparison on a 6-Bit A/D Converter

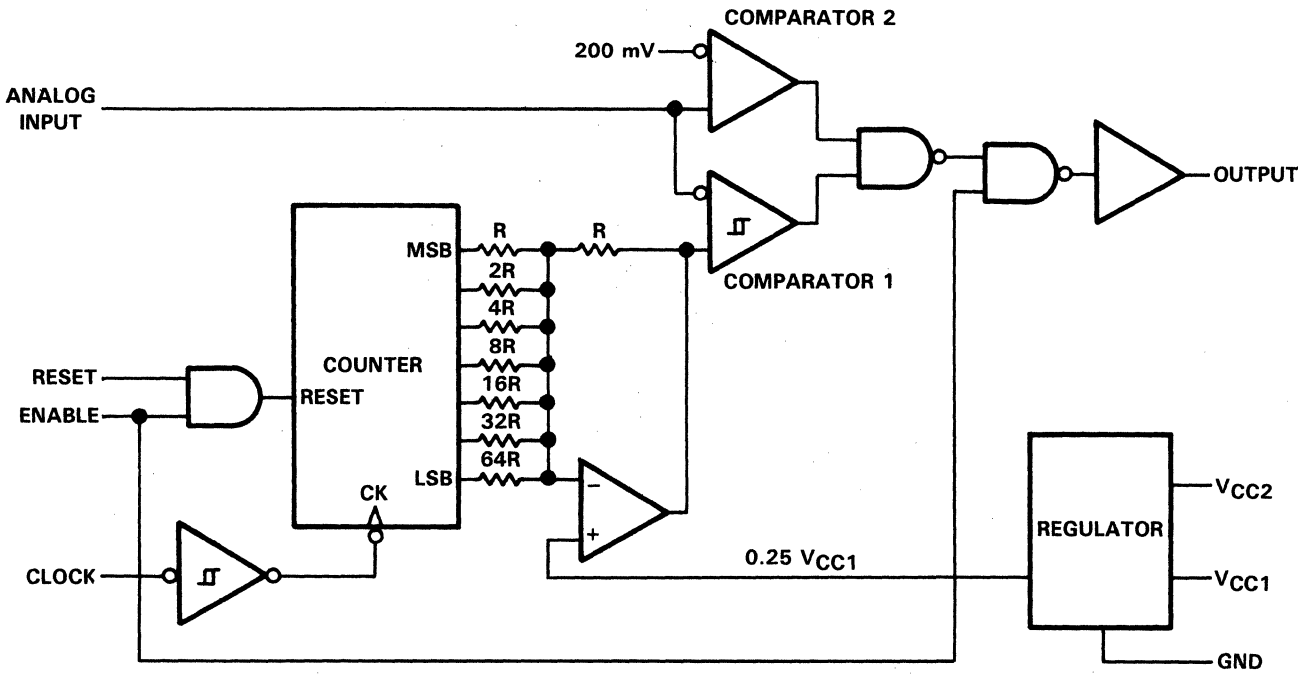


Figure 11-29. Single-Slope A/D Converter

DUAL-SLOPE A/D CONVERTER

Dual-slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter. The speed of this conversion technique is slow but the accuracy is high.

Like the single-slope A/D, the dual-slope integrator arrives at its digital output by building ramps. Its greater accuracy and lower conversion speed result from building two ramps instead of one. The first integration (ramp building) is accomplished using the unknown analog input and integrating for a fixed time (T). The peak value of this integration is proportional to the value of the unknown analog input. See Figure 11-30.

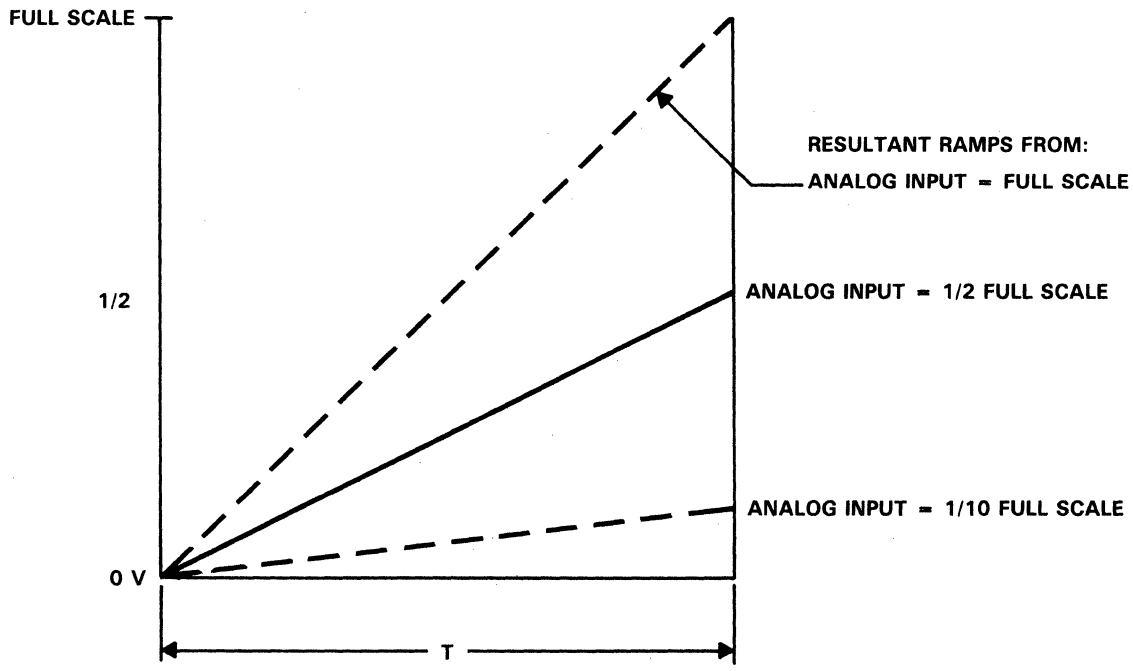


Figure 11-30. Ramp 1 — Dual-Slope A/D Converter

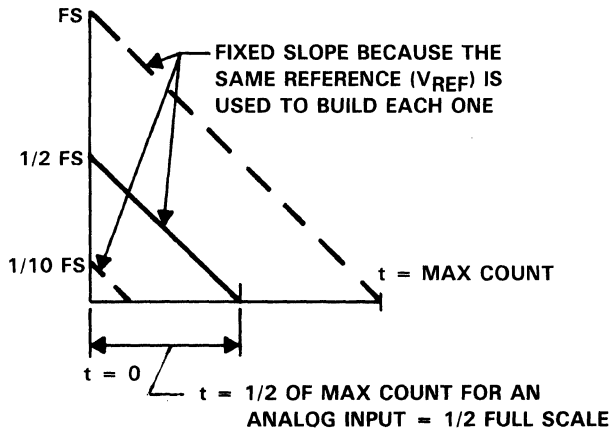


Figure 11-31. Ramp 2 — Dual-Slope A/D Converter

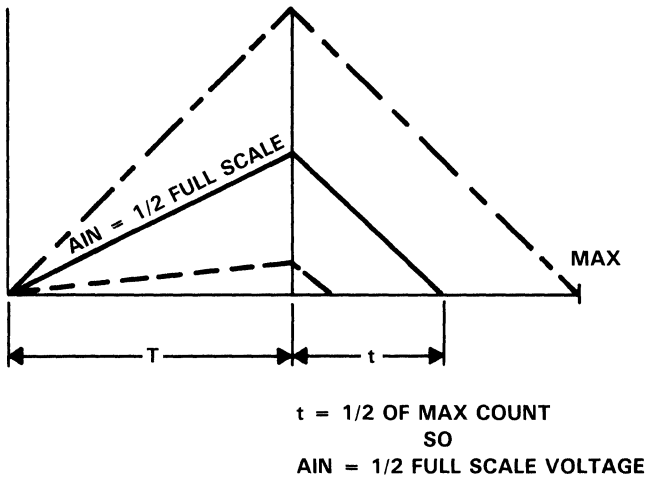


Figure 11-32. Ramps 1 and 2 — Dual-Slope A/D Converter

The resultant value is then integrated back down to 0 V at a fixed rate by using a reference voltage for a variable time (t). Since the reference causes this second ramp to have a fixed slope, the time (t) required to reach 0 V is proportional to the peak value of the first ramp. See Figure 11-31.

Putting these two ramps together, using the same clock to count (T) and (t), and using the same integration network to build both ramps allows errors in the clock frequency and linearity errors due to a nonlinear integrator to cancel. This leaves the stability of the reference voltage as the determining factor in overall accuracy. See Figure 11-32 for both ramps.

While the conversion speed of a dual-slope A/D converter is slow, resolution ranges of from 8 to 14 bits are available. Figure 11-33 shows a functional block diagram of a dual-slope A/D converter.

SUCCESSIVE-APPROXIMATION CONVERTERS

The successive-approximation converter has been used for a long time and is still the most common A/D converter for applications with sampling rates of about 1 MHz maximum. The name "successive approximation" comes from the fact that the converter arrives at a numerical value by making successively more precise observations until it

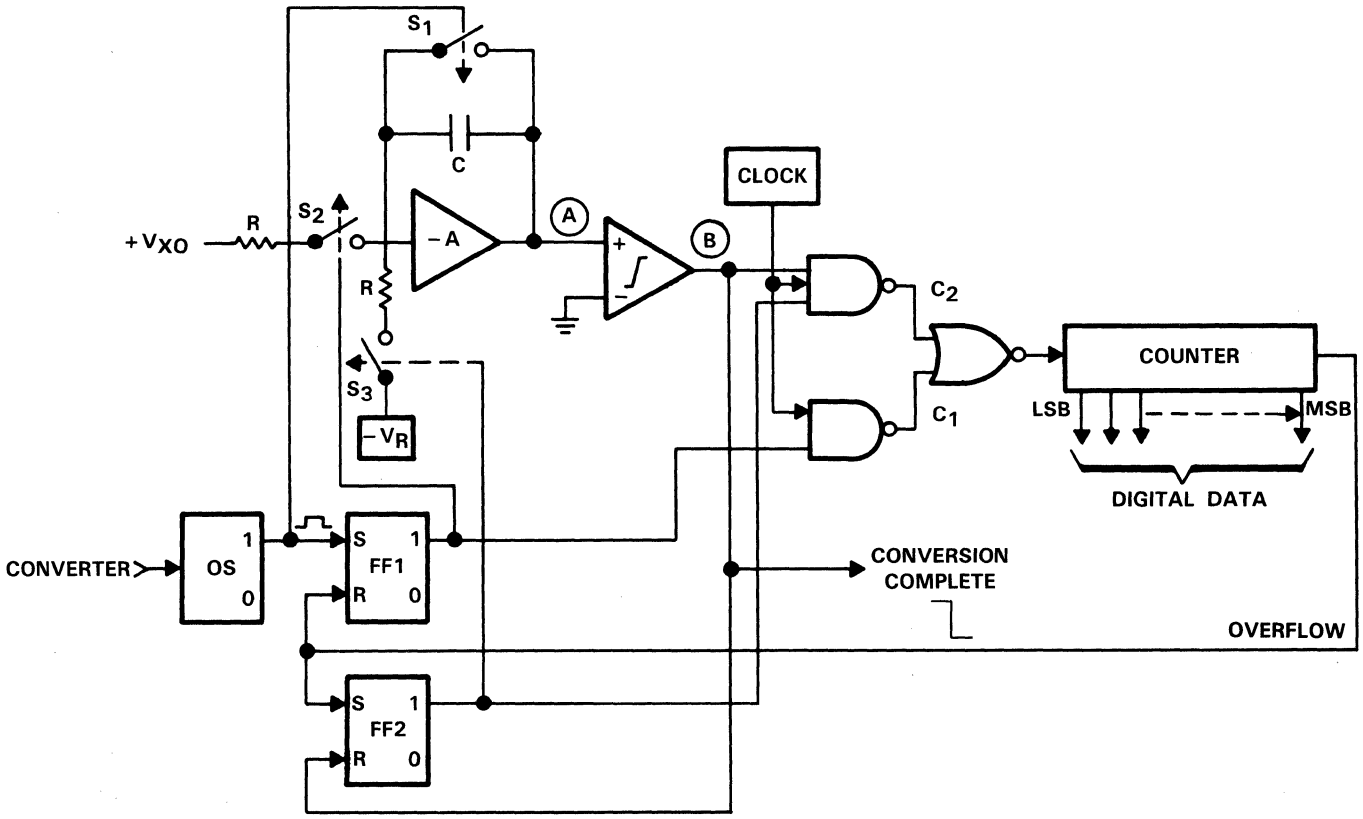


Figure 11-33. Dual-Slope A/D Converter Functional Diagram

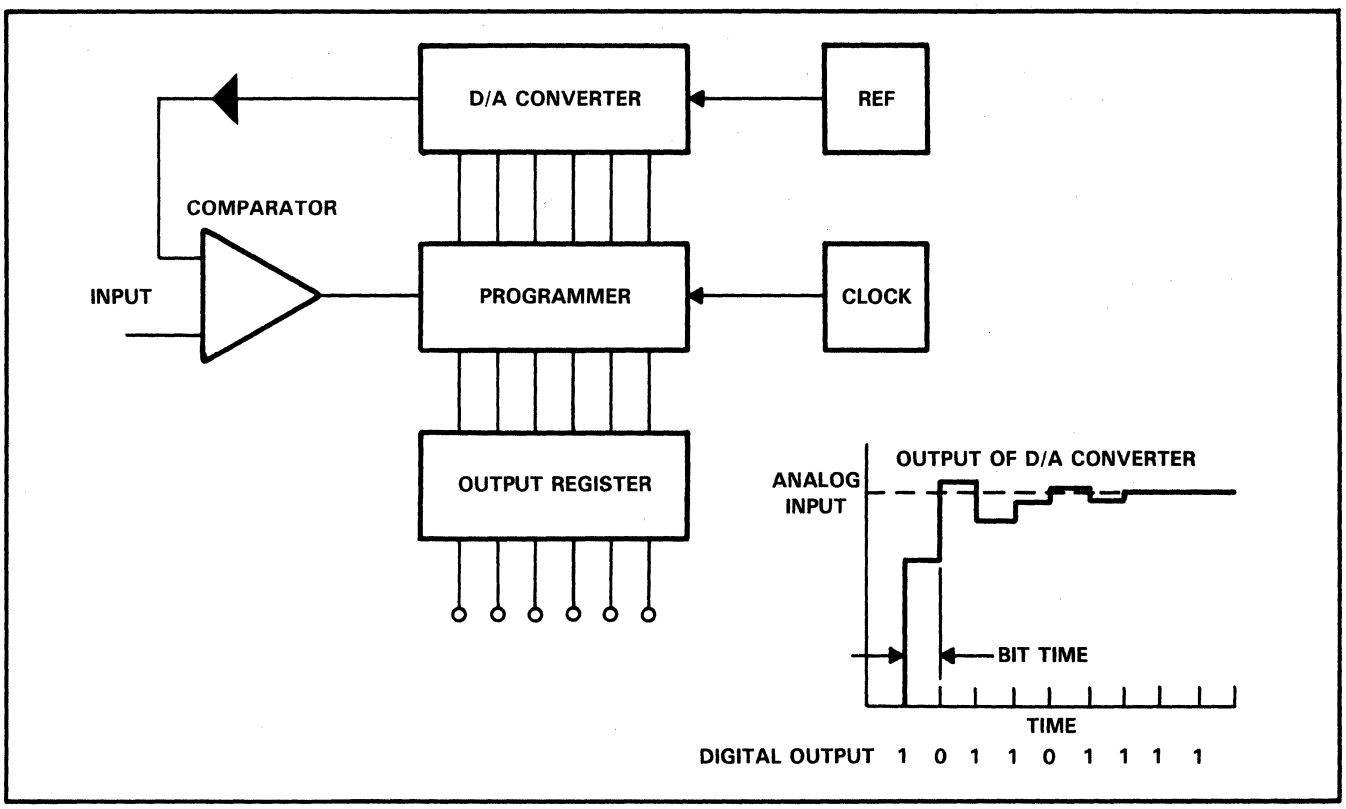


Figure 11-34. Successive-Approximation A/D Converter Block Diagram

has arrived at the closest answer.

Successive approximation does not use ramps to generate its digital output as the integration techniques did. Instead of ramps, it uses a digital-to-analog converter that allows the respective bit values to be successively compared with the input, from the MSB to LSB, in a series of steps. This method compares, in sequence, a series of binary-weighted values with the analog input to produce an output digital code in "n" steps, where "n" is the resolution of the converter. In the past, "resistor-ladder" designs were used to implement the conversion. Recent design techniques employ switched-capacitor networks utilizing charge redistribution on weighted capacitors to accomplish the A/D conversion. Figure 11-34 shows a block diagram of a typical successive-approximation A/D converter.

On the input, a single voltage comparator is driven by the signal on one input and by a reference D/A converter on the other. The D/A converter is programmed (with MSB = 1, other bits = 0) to produce a voltage equal to one-half of the full-scale reading of the A/D measuring range. The comparator determines if the D/A output is above or below the input signal level. In Figure 11-34 the input is above the D/A value so that a "1" appears as the first digital output code. The D/A now increases the D/A output by 1/2 the previous amount and being above the input signal causes a "0" to be the second coded value. This process continues until it can no longer divide the previous step in half. The result now goes to the output register.

While all this happens very fast, the signal must be held constant while the successive-approximation converter does its processing. This is accomplished with a sample-and-hold circuit which would be ahead of the comparator in Figure 11-34. Between conversions, the sample-hold circuit acquires the input signal, and, just before the conversion starts, places it in hold, where it remains until the conversion is complete. A simplified sample-hold circuit is shown in Figure 11-35.

Basically, a sample-hold circuit is a "voltage memory" device that stores a given voltage on a high-quality capacitor. This capacitor must have low leakage and low dielectric absorption. An electronic switch is connected to the hold capacitor so that when the switch closes, the capacitor charges with the input voltage. When the switch opens, the capacitor retains this charge for the desired period of time. The TLC271 op amps are connected as unity-gain buffer stages,

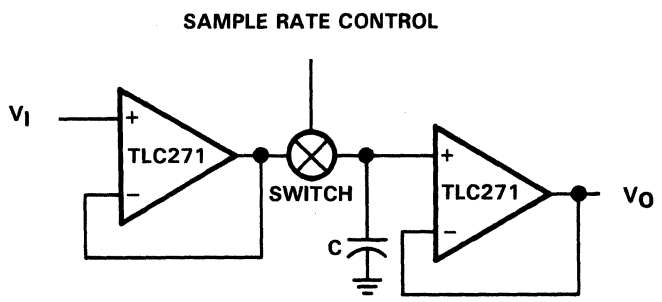


Figure 11-35. Basic Sample-Hold Switch

offering the high impedance needed in this application. This is very important when operating at the output of an analog multiplexer because the source should not be loaded. The output impedance of the buffer is low so that the sample-hold circuit can more easily drive the A/D converter input. Usually an FET type of device is used as the electronic sample rate control as it must be fast and have very low off-state leakage.

Binary Bit Weighting

In a binary number, the MSB (most significant bit) is always equal to 1/2 the full scale or maximum value. The next MSB is equal to 1/4 the maximum value, the next 1/8, the next 1/4, etc., until we arrive at the LSB (least significant bit) which has the value of the Maximum Value/$2^{(n)}$ (where "n" = number of bits).

As an example, assume we have a full scale (or maximum value) of 4 V. With a 4-bit converter, a 4-bit binary number would be arrived at as follows:

MSB (most significant bit)	= 4 × 1/2 = 2 V
Next MSB	= 4 × 1/4 = 1 V
Next MSB	= 4 × 1/8 = 1/2 V
LSB (least significant bit)	= 4 × 1/16 = 1/4 V
Full-Scale Reading	= 3 3/4 V

Thus, on a 4-bit converter the resolution is defined as:

$$\text{Resolution} = \frac{\text{Full Scale}}{2^4 \text{ bits}} = 1/4 \text{ V}$$

Therefore we can only determine the actual value in 1/4 V steps.

Creating a Digital Number

As stated previously, a successive-approximation converter has a built-in D/A converter which it uses to compare the output of the D/A with the analog input. It must then decide which binary number most closely represents the analog input. To do this the A/D starts with the MSB. See Figure 11-36.

As seen in the above example, the A/D compares its 1/2 full-scale value with the analog input and decides if it is at or above, or below, the 1/2 full scale value. If the input is below it sets the MSB to "0", if the input is at or above the 1/2 full scale value, it sets the MSB to "1". It then considers the next MSB in the same manner and continues until it has checked the LSB. After checking the LSB, the number remaining in the counter is the most accurate binary representation of the analog input voltage that is within the capability of the 4-bit A/D.

For the 4-bit converter, only 4 steps were required to arrive at the digital number. For an 8-bit converter, 8 steps would be required. The number of bits equals the number of steps. Each step is completed very fast, so even an 8-bit A/D requires much less time than would be required by a single ramp as in the case of a single-slope A/D converter.

The requirements for building a good successive-approximation converter are a stable reference voltage, an

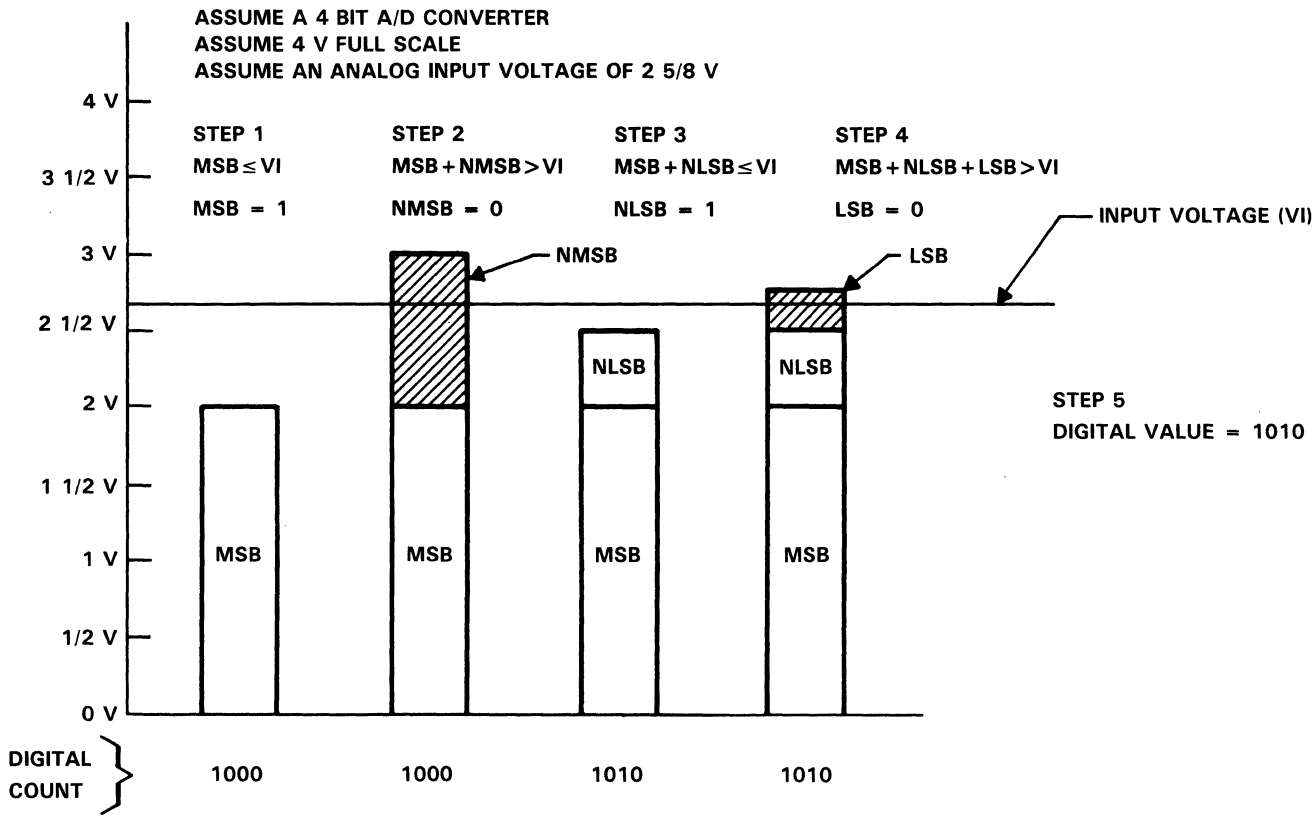


Figure 11-36. 4 V 4-Bit Successive Approximation A/D Converter Output

accurate D/A converter, and sufficient control logic to handle the counters, output registers, etc.

In summary, the successive-approximation A/D is faster but generally less accurate than a single- or dual-slope A/D.

FLASH A/D CONVERTERS

The flash A/D converter gets its name from its ability to do the conversion very rapidly. The flash converter gives an answer every time it receives a clock pulse.

As discussed previously, the successive-approximation A/D converter needs a clock pulse for each bit of resolution it provides. The flash A/D converter also does not need a sample-hold circuit or a D/A converter. The fast conversion speed is accomplished by providing a comparator for every quantization level except one ($2^n - 1$ comparators). The quantization level that does not require a comparator can be zero or full scale depending on how the reference is applied.

The power and speed of this technique lies in the fact that all comparators examine the input voltage simultaneously in parallel and make an immediate, total conversion. The limiting factor of this conversion system is the number of comparators required, which necessitates a larger bar of silicon material and increased cost. See Figure 11-37 for the block diagram of a flash converter.

As shown, one input of each comparator is connected to the input signal. The other input is connected to a voltage divider (resistor ladder network) chain that is fed by the reference. The reference is equal to the full-scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple. When the rising edge of the clock arrives, the comparators quickly latch in a "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referenced above the input signal remain turned off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparison is converted to a binary code by the decoder network. The number of bits in the code is equal to the number of bits of resolution.

In summary, a flash converter can give an answer every time it receives a clock pulse, although $2^n - 1$ comparators are required to perform the conversion function. It is significant to note that each time the number of bits of resolution increases by one, the number of comparators essentially doubles. As an example:

A 6-bit resolution converter requires 63 comparators.
A 7-bit resolution converter requires 127 comparators.
An 8-bit resolution converter requires 255 comparators.

Presently the units on the market range from 4 bits at 50 MHz to 100 MHz to 6 bits at 100 MHz. These devices are built using the bipolar process.

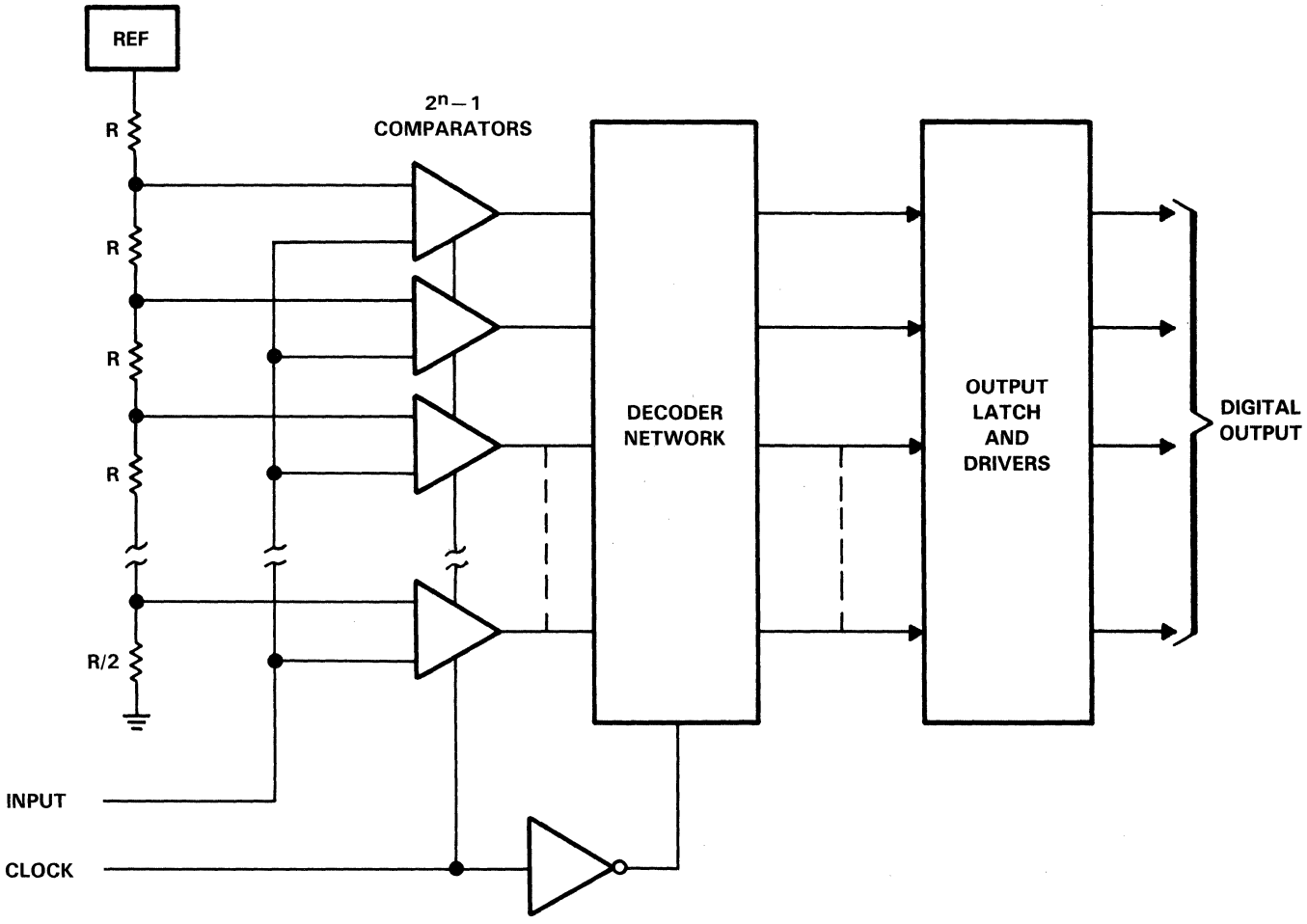


Figure 11-37. Flash A/D Converter Block Diagram

DEVICE TYPES

The use of digital techniques in measurement, communication, and control systems has increased rapidly in the past few years. Control systems use a combination of digital and analog (linear) circuit techniques. One of the key devices in these systems is the analog-to-digital (A/D) converter. Because of their inherent complexity, A/D converters have always been a challenge to IC designers. Through the continuous progress in design and process technology, economical monolithic devices are available to meet a wide range of application requirements. Today, the LinCMOS™ technology provides increased speeds, better input stability, lower power requirements, and increased thermal stability for demanding applications.

ADC0803 AND ADC0805 8-BIT SUCCESSIVE APPROXIMATION A/D CONVERTERS WITH DIFFERENTIAL INPUTS

The ADC0803 family of A/D converters are 8-bit devices which feature a conversion time of 100 μs and an access time of 135 ns. This converter requires no zero adjust, has an on-chip clock generator, and will operate from a single 5-V supply. As shown in Figure 11-38, the pinout allows for easy PC board layout. The data output pins are grouped together and the ground and V_{CC} pins are located at the package corners.

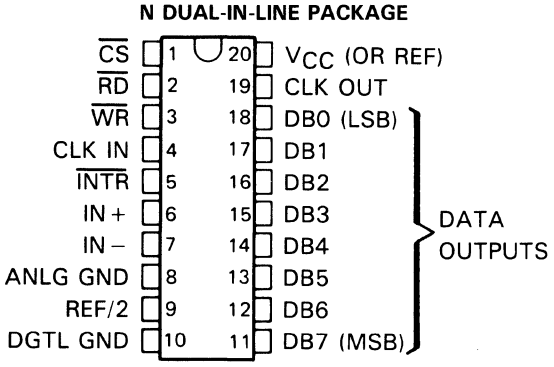


Figure 11-38. ADC0803 and ADC0805 Pinout (Top View)

Description

The ADC0803 and ADC0805 are CMOS 8-bit successive-approximation analog-to-digital converters that use a modified potentiometric 256-resistor ladder network. These devices are designed to operate from common microprocessor control buses, with the 3-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port. Figure 11-39 shows a functional block diagram and the timing diagrams are illustrated in Figure 11-40.

A differential analog voltage input allows increased common-mode rejection and eliminates offset due to the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to analog ground (ANLG GND). The devices can operate with an external clock signal or, the on-chip clock generator can be used independently by adding an external resistor and capacitor to set the time period.

Principles of Operation

The ADC0803 and ADC0805 each contain a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive-approximation logic to match an analog differential input voltage ($V_{I+} - V_{I-}$) to a corresponding tap on the resistor network. The most significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start($\overline{CS}$) input at a low level. To ensure start-up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low any time after that will interrupt a conversion in process.

When the $\overline{WR}$ input goes low, the internal successive-approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter will remain in its reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts. When the $\overline{CS}$ and $\overline{WR}$ inputs are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the 8-bit shift register and the conversion process is started. If the $\overline{CS}$ and $\overline{WR}$ inputs are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the 3-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is completed.

When a low is at both the $\overline{CS}$ and $\overline{RD}$ inputs, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the $\overline{CS}$ or $\overline{RD}$ input returns to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

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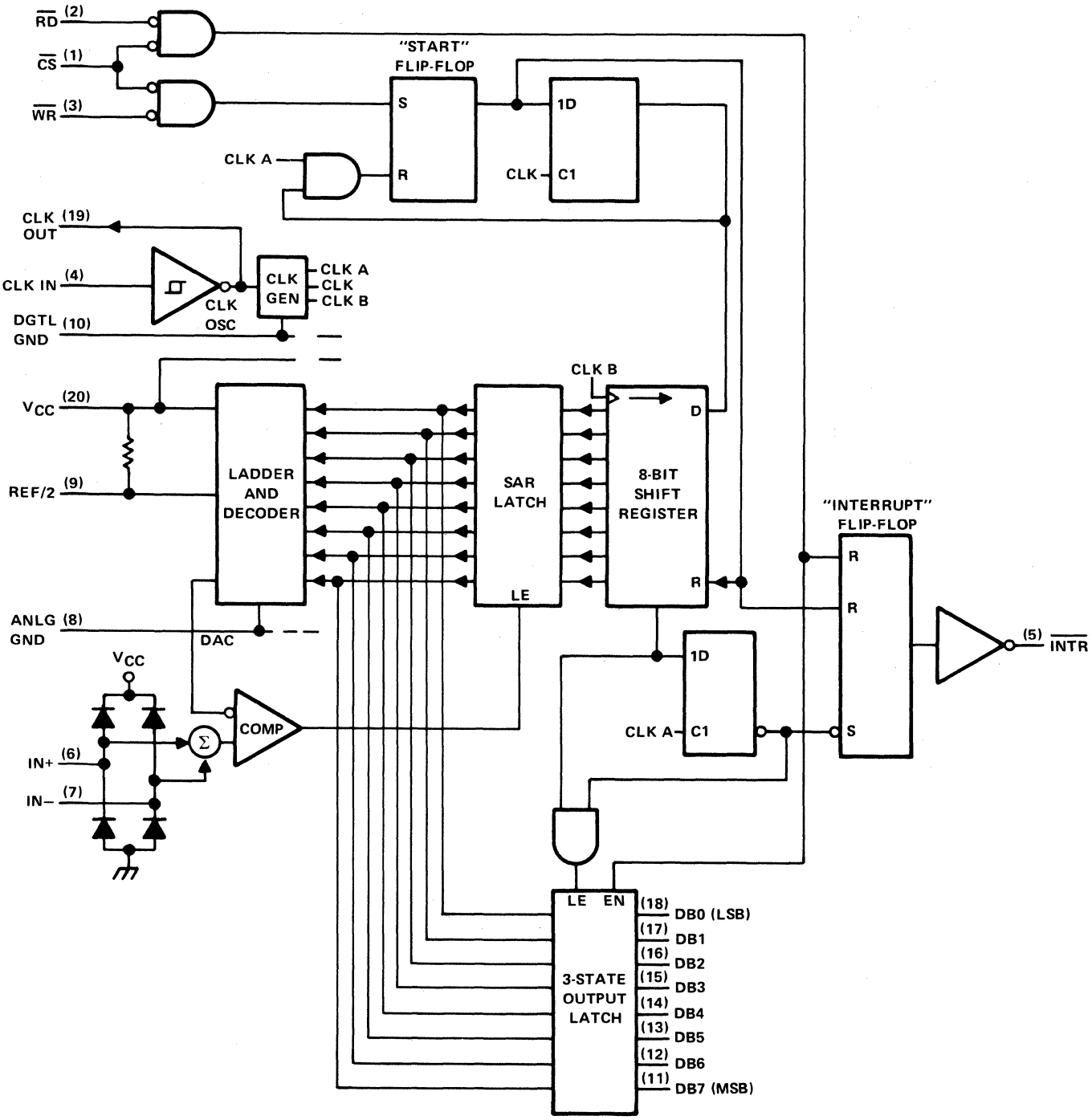
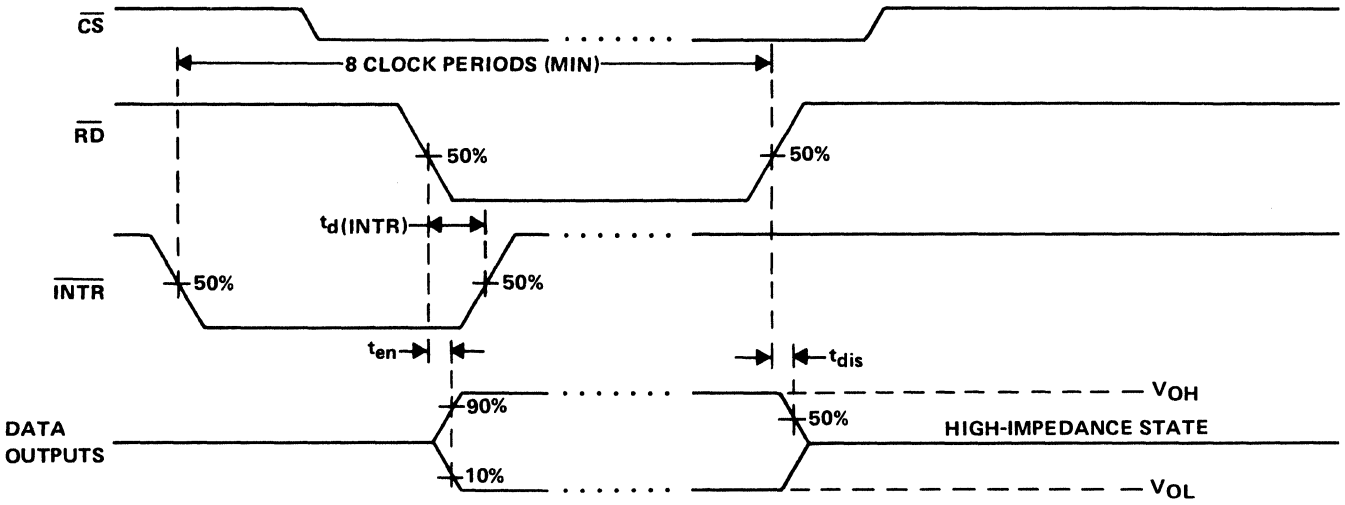
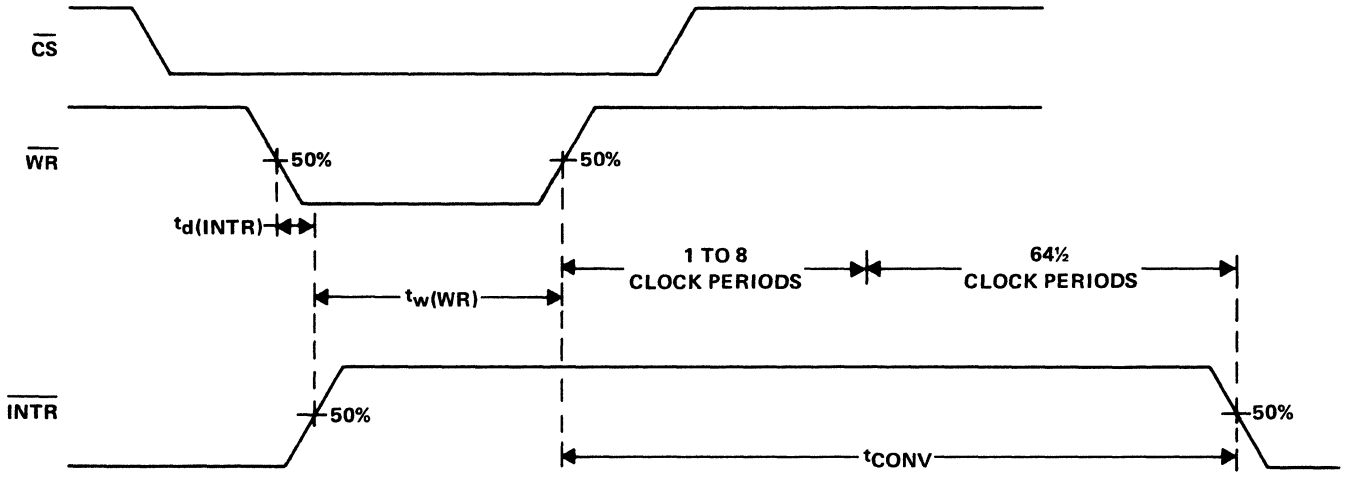


Figure 11-39. Functional Block Diagram (Positive Logic)



READ OPERATION TIMING DIAGRAM

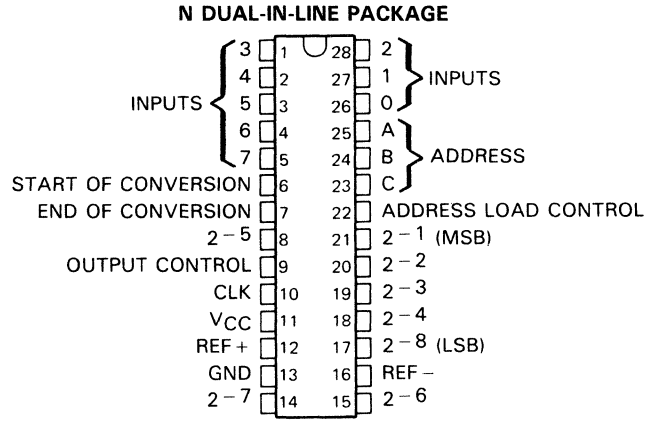


WRITE OPERATION TIMING DIAGRAM

Figure 11-40. Timing Diagrams

ADC0808, ADC0809 CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

The ADC0808 and ADC0809 are 8-bit A/D converters that offer latched address inputs as well as latched 3-state outputs. The total unadjusted error in the ADC0808 is ± 1/2 LSB max and for the ADC0809 is ± 1.0 LSB max. These devices feature ratiometric conversion with a conversion time of 100 μs. They may be powered from a single 5-V supply and are easily connected to a microprocessor. Figure 11-41 shows how the inputs and address lines have been grouped to facilitate PC board layout.



Filgure 11-41. ADC0808, ADC0809 Pinout (Top View)

Description

The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital A/D converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled

by a microprocessor through the 3-bit address decoder with address load control to select any one of eight single-ended analog switches connected directly to the converter. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). The functional block diagram is shown in Figure 11-42 and the operating sequence in Figure 11-43.

The comparison and conversion methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the converter and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

Multiplexer

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. Address load control loads the address code into the decoder on a low-to-high transition.

MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

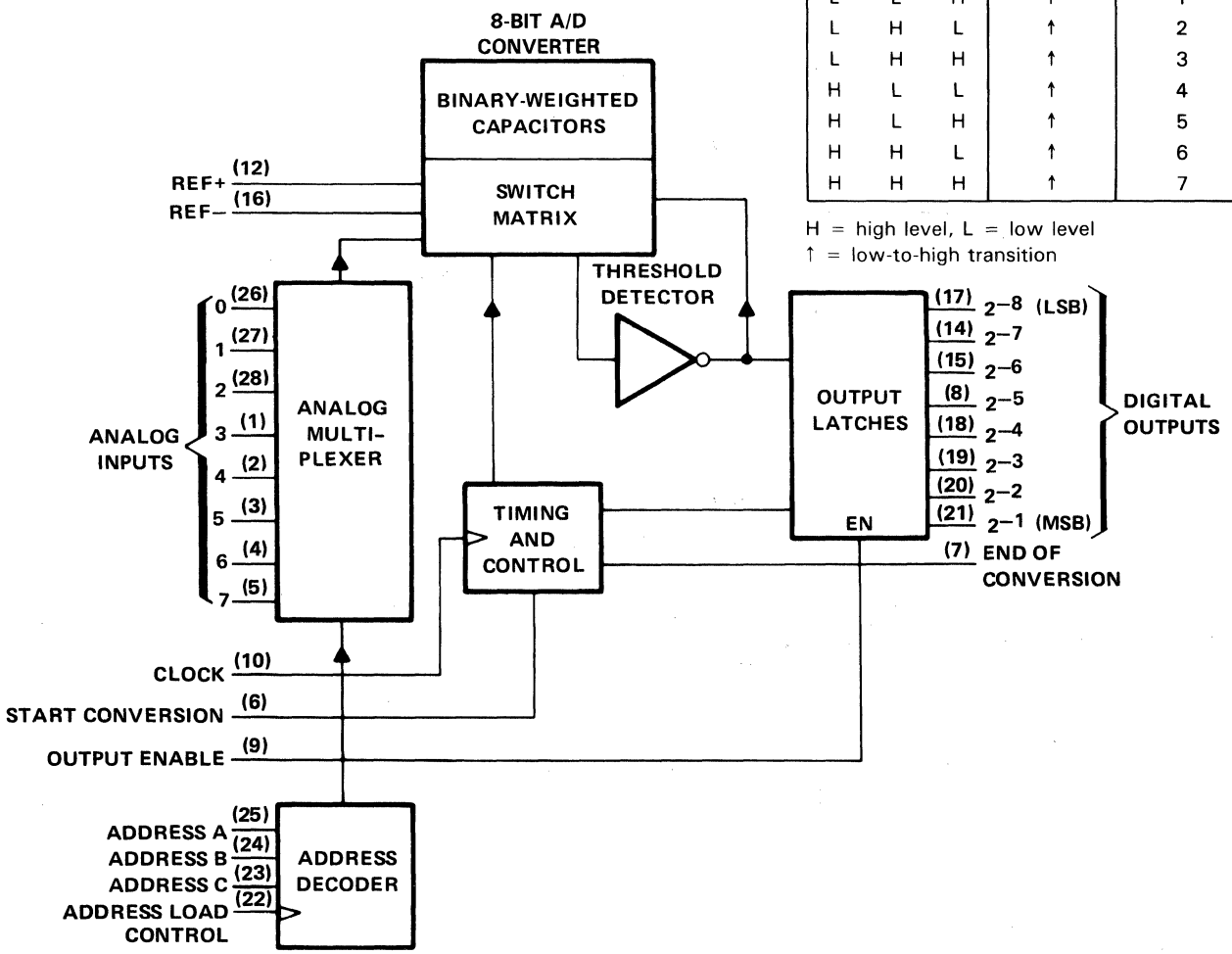


Figure 11-42. Functional Block Diagram (Positive) and Function Table

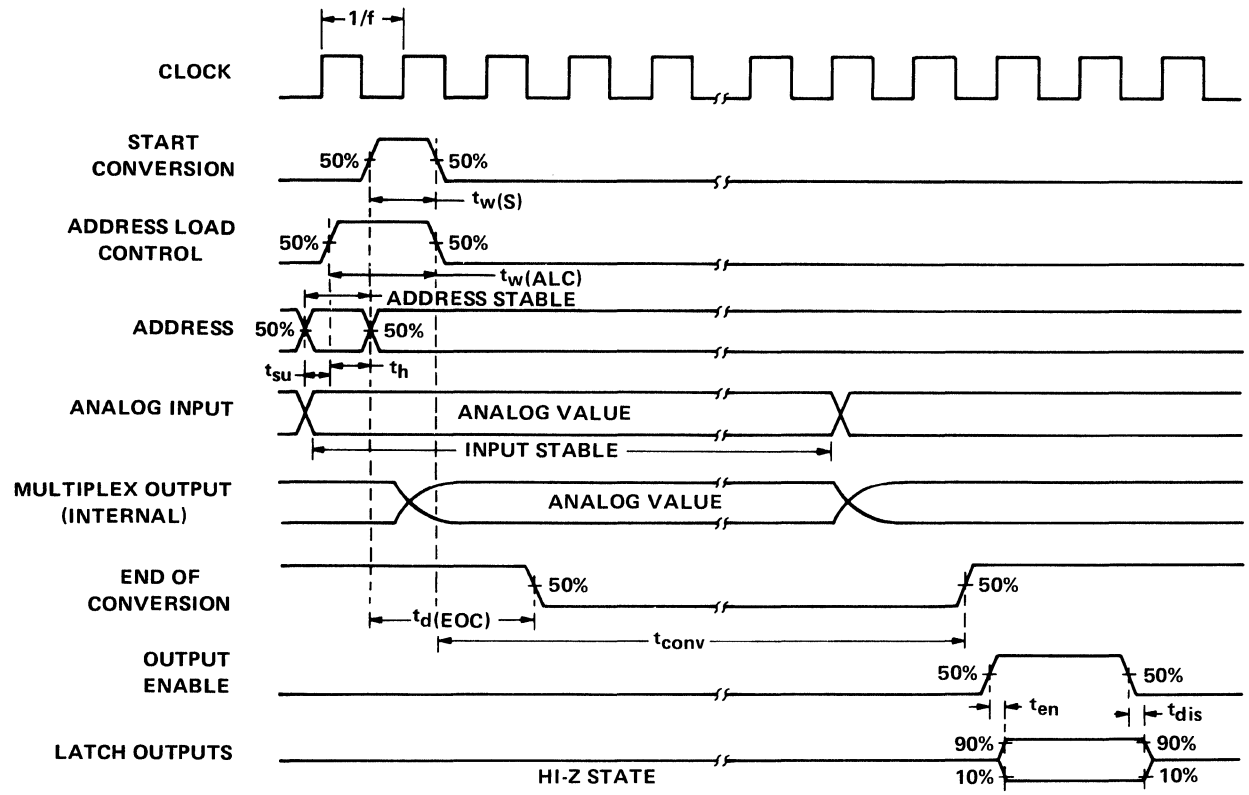


Figure 11-43. Operating Sequence

Converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 11-44).

In the first phase of the conversion process, the analog input is sampled by closing switch S_C and all S_T switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all S_T switches and the S_C switch are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 of this capacitor is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF −. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF −. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF + through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, then the 32-weight capacitor, and so on until all bits are counted.

With each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. This conversion process is successive approximation, but relies on charge redistribution rather than a successive-approximation register (and reference D/A) to count and weigh the bits from MSB to LSB.

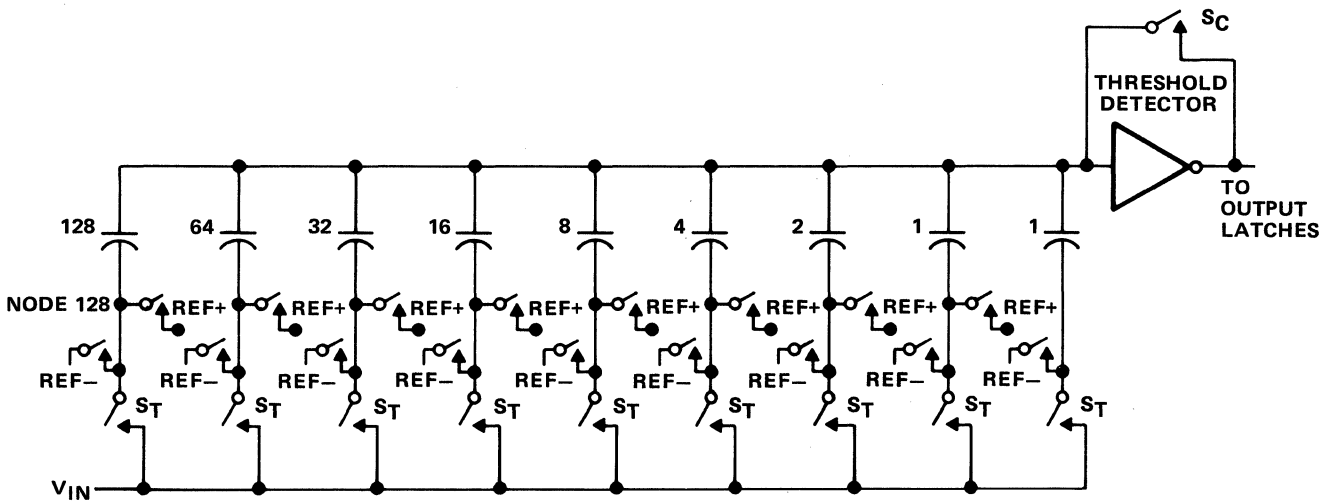


Figure 11-44. Simplified Model of the Successive-Approximation System

ADC0831, ADC0832, ADC0834, ADC0838 2-, 4-, 8-CHANNEL A/D PERIPHERALS WITH SERIAL CONTROL AND MULTIPLEXER OPTIONS

The ADC0831, ADC0832, ADC0834, and ADC0838 A/D converters are another family of A/D converters that may be easily used with a microprocessor or operated stand-alone. There is no zero or full-scale adjust. An on-chip shunt regulator on the ADC0834 and ADC0838 allows operation with high-voltage supplies. A conversion time of 32 μs is possible at a clock frequency of 250 kHz. The input voltage range is 0 to 5 V with a single 5 V supply. The systematic placing of data lines, V_{CC}, and ground terminals shown in Figure 11-45 allows efficient PC board layout.

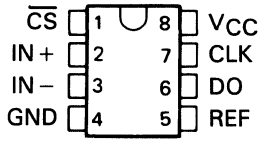
Description

The ADC0831, ADC0832, ADC0834, and ADC0838 are 8-bit successive-approximation analog-to-digital converters each with a serial input/output and configurable input multiplexer with up to 8 channels on the ADC0838. The serial input/output can be used with standard shift registers or microprocessors. See Figure 11-46 for a functional block diagram of the ADC0831 and ADC0832 and Figure 11-47 for the functional block diagram of the ADC0834 and ADC0838.

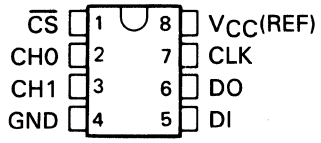
The 2-, 4-, or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment. Figures 11-48 and 11-49 show the ADC0832 and ADC0834—838 input and data output timing diagrams and Figure 11-50 shows the ADC0831 sequence of operation. The operating sequence for the ADC0832 is illustrated in Figure 11-51 while the ADC0834 sequence of operation is shown in Figure 11-52. The ADC0838 sequence of operation is shown in Figure 11-53.

The differential analog voltage input increases the common-mode rejection and eliminates the offset due to the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

P DUAL-IN-LINE PACKAGE

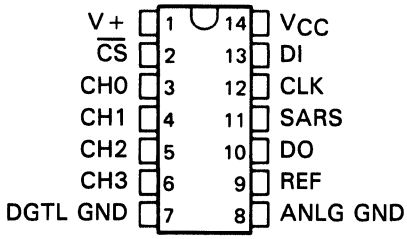


(a) ADC0831

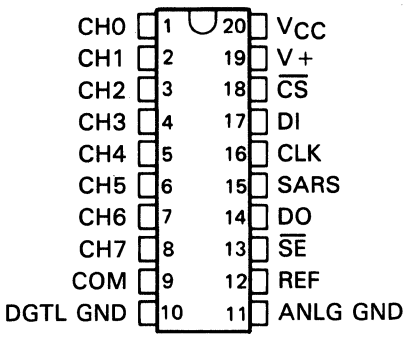


(b) ADC0832

N DUAL-IN-LINE PACKAGE



(c) ADC0834



(d) ADC0838

Figure 11-45. ADC0831, ADC0832, ADC0834, ADC0838 Pinouts (Top View)

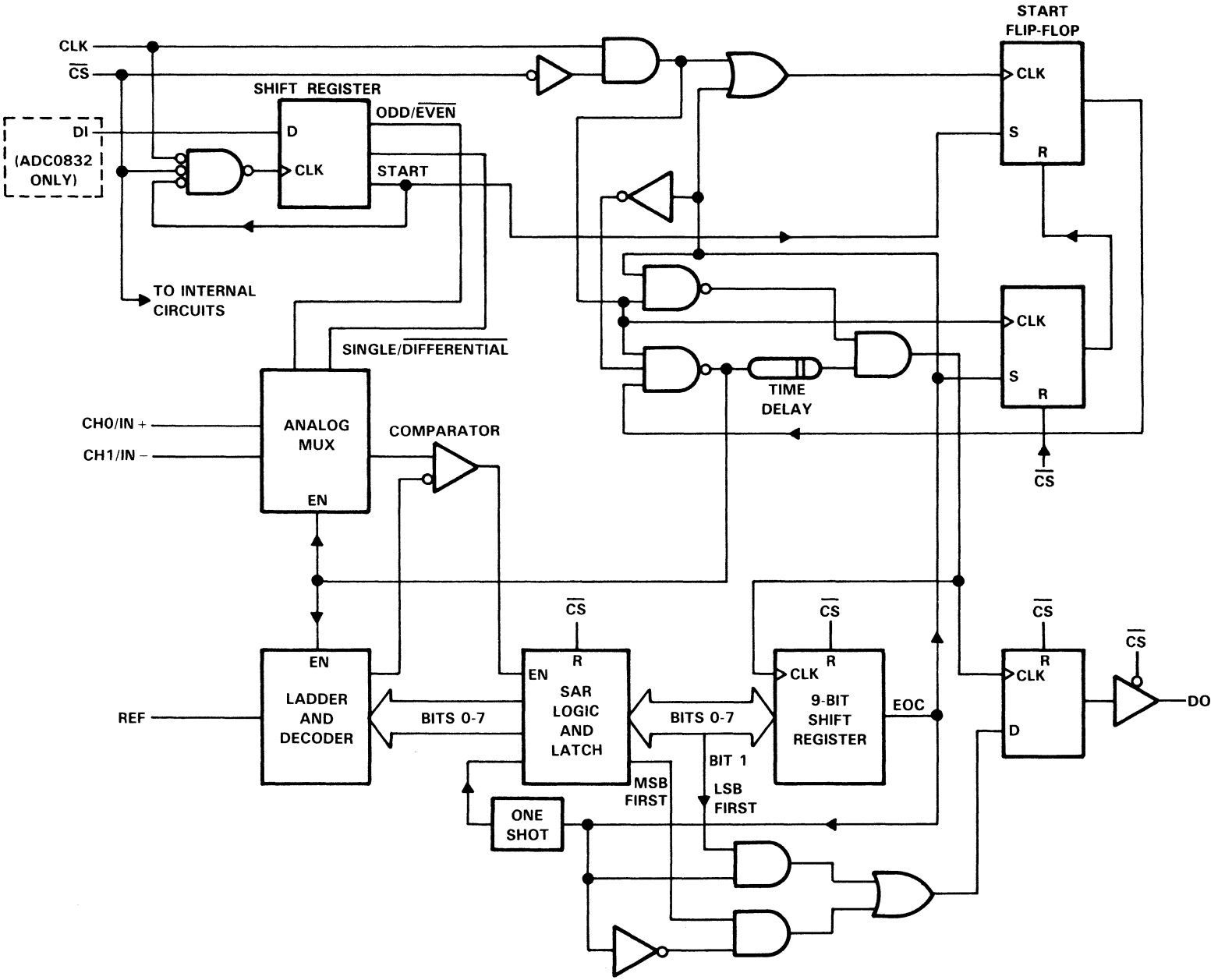
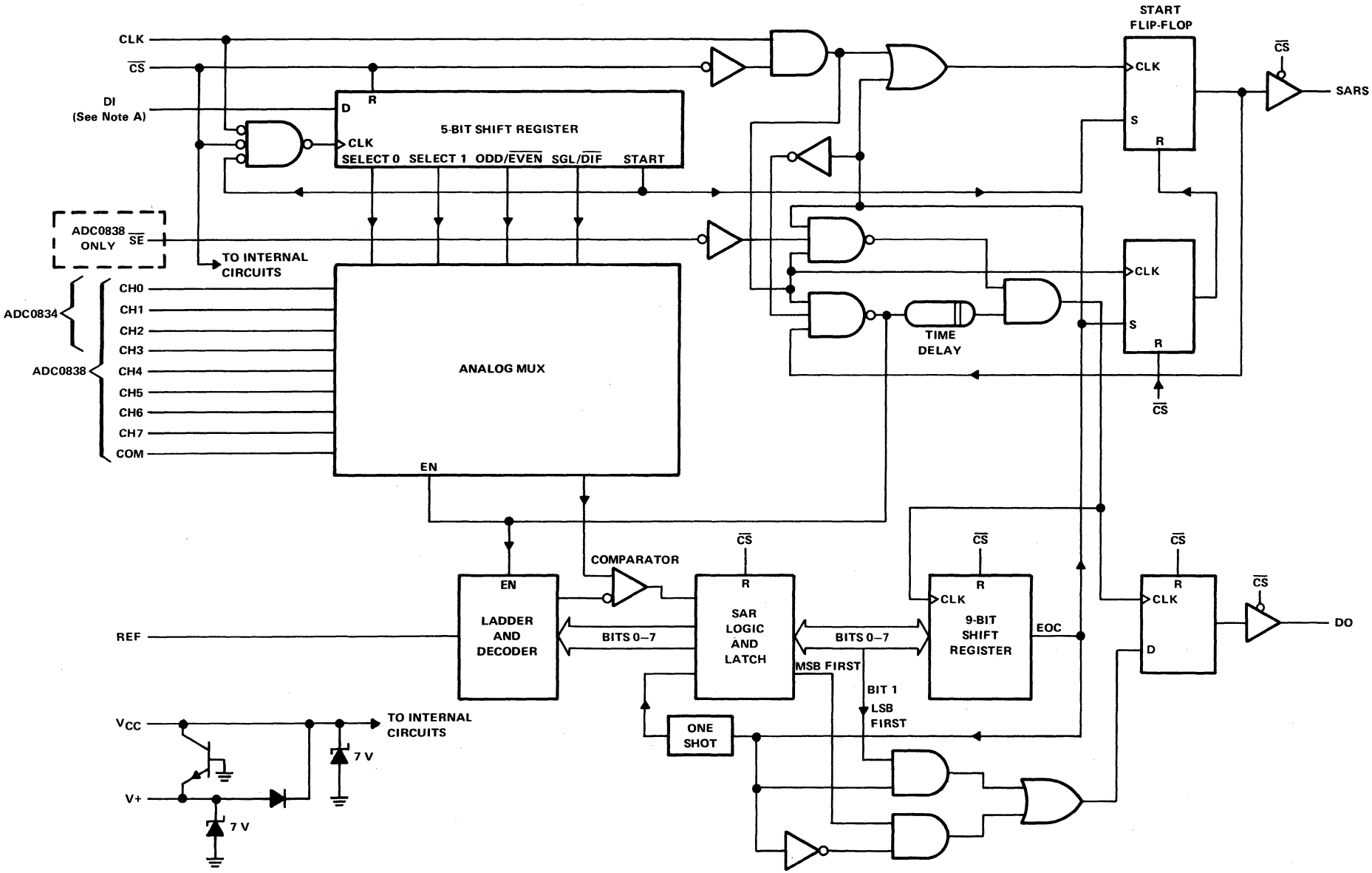
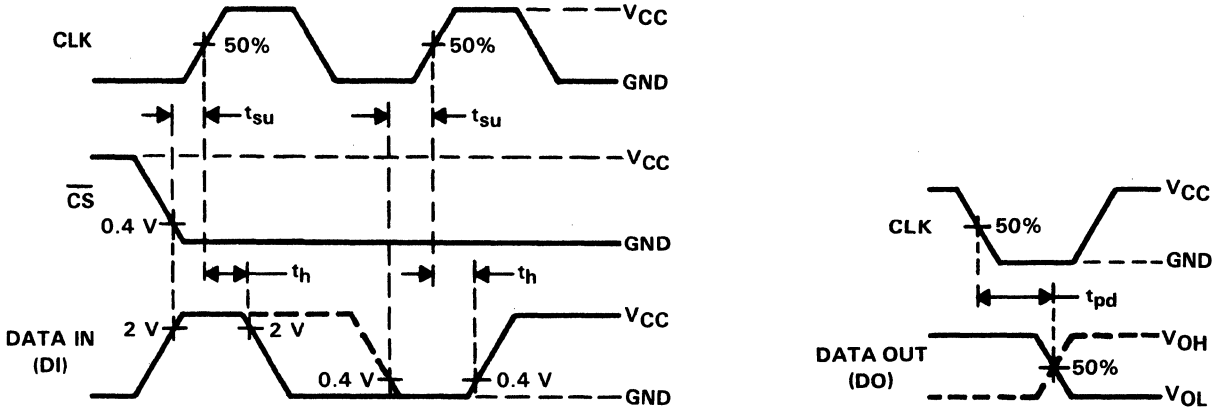


Figure 11-46. ADC0831A-B, ADC0832A-B Functional Block Diagram



NOTE A: For the ADC0834, DI is input directly to the D input of SELECT 1, SELECT 0 is forced to a high.

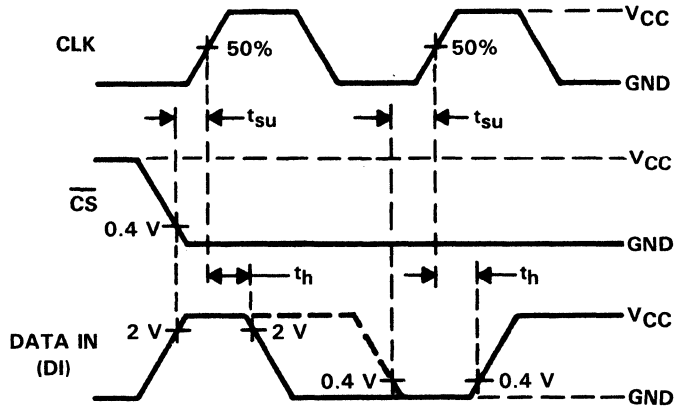
Figure 11-47. ADC0834A-B, ADC0838A-B Functional Block Diagram



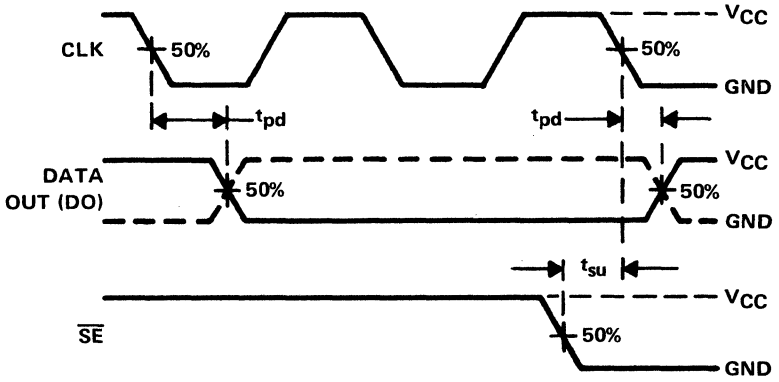
(a) DATA INPUT TIMING

(b) DATA OUTPUT TIMING

Figure 11-48. ADC0832 Data Input and Output Timing Diagram



(a) DATA INPUT TIMING



(b) DATA OUTPUT TIMING

Figure 11-49. ADC0834, ADC0838 Data Input and Output Timing Diagram

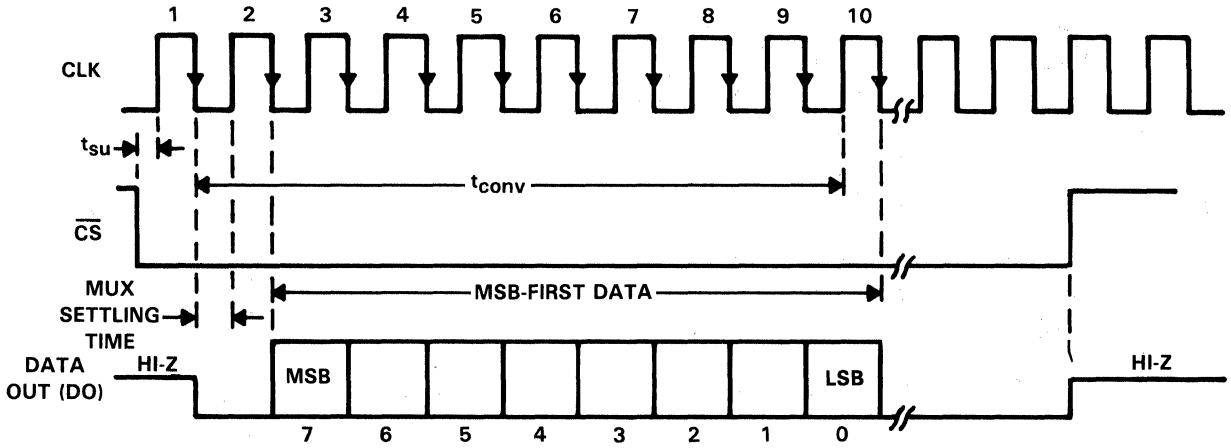


Figure 11-50. ADC0831 Sequence of Operation

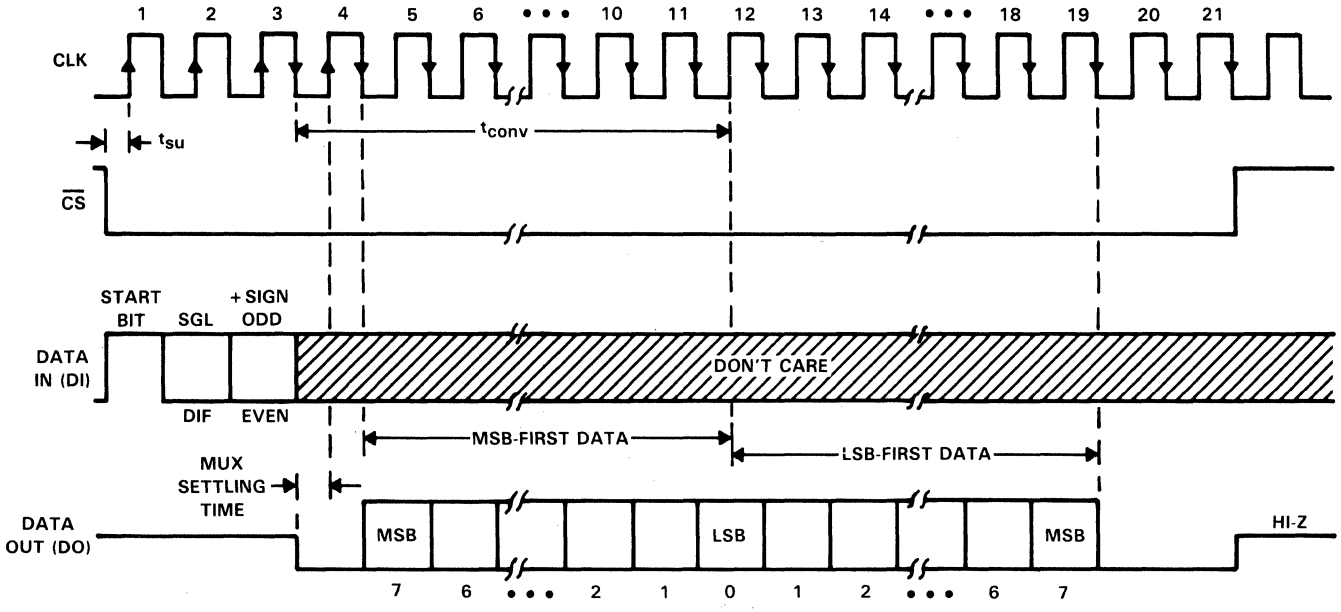


Figure 11-51. ADC0832 Sequence of Operation

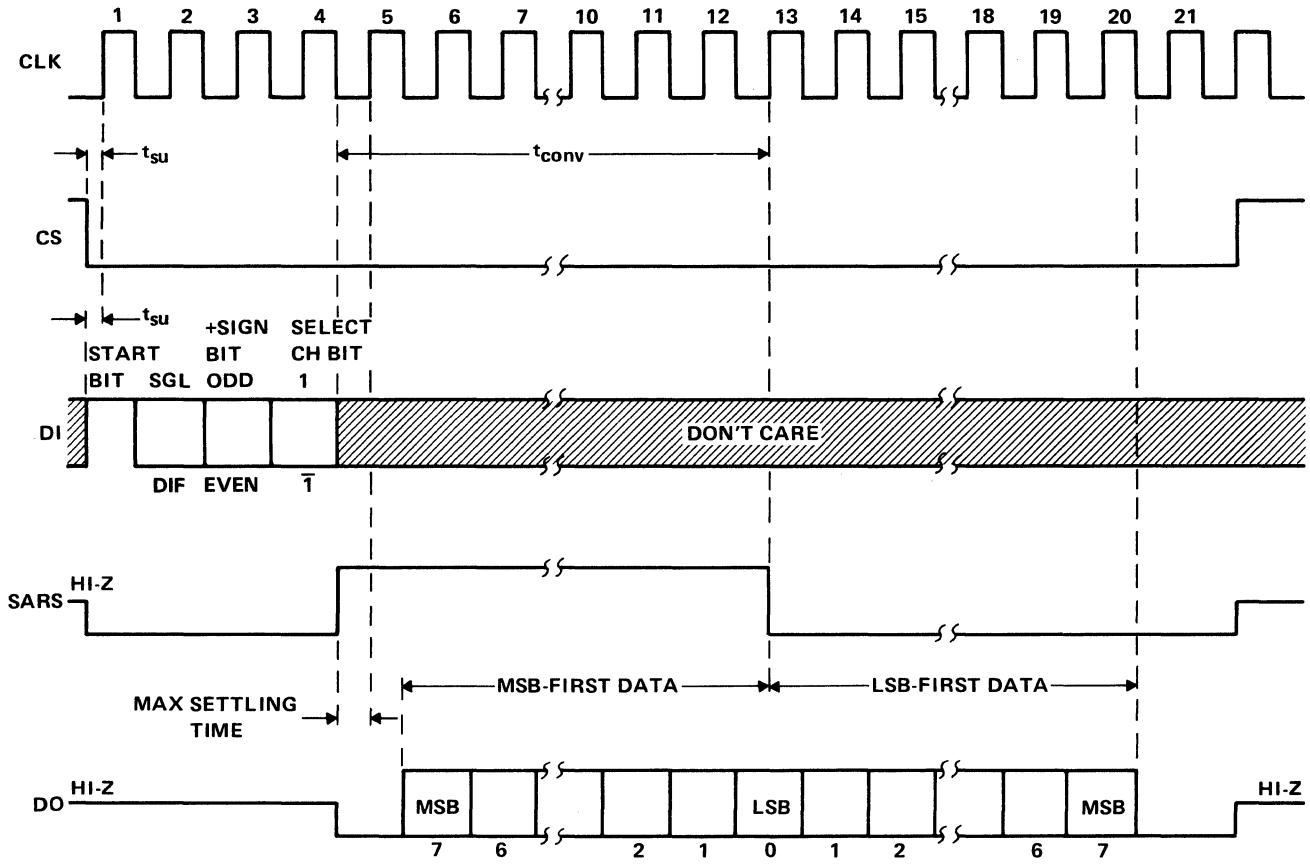


Figure 11-52. ADC0834 Sequence of Operation

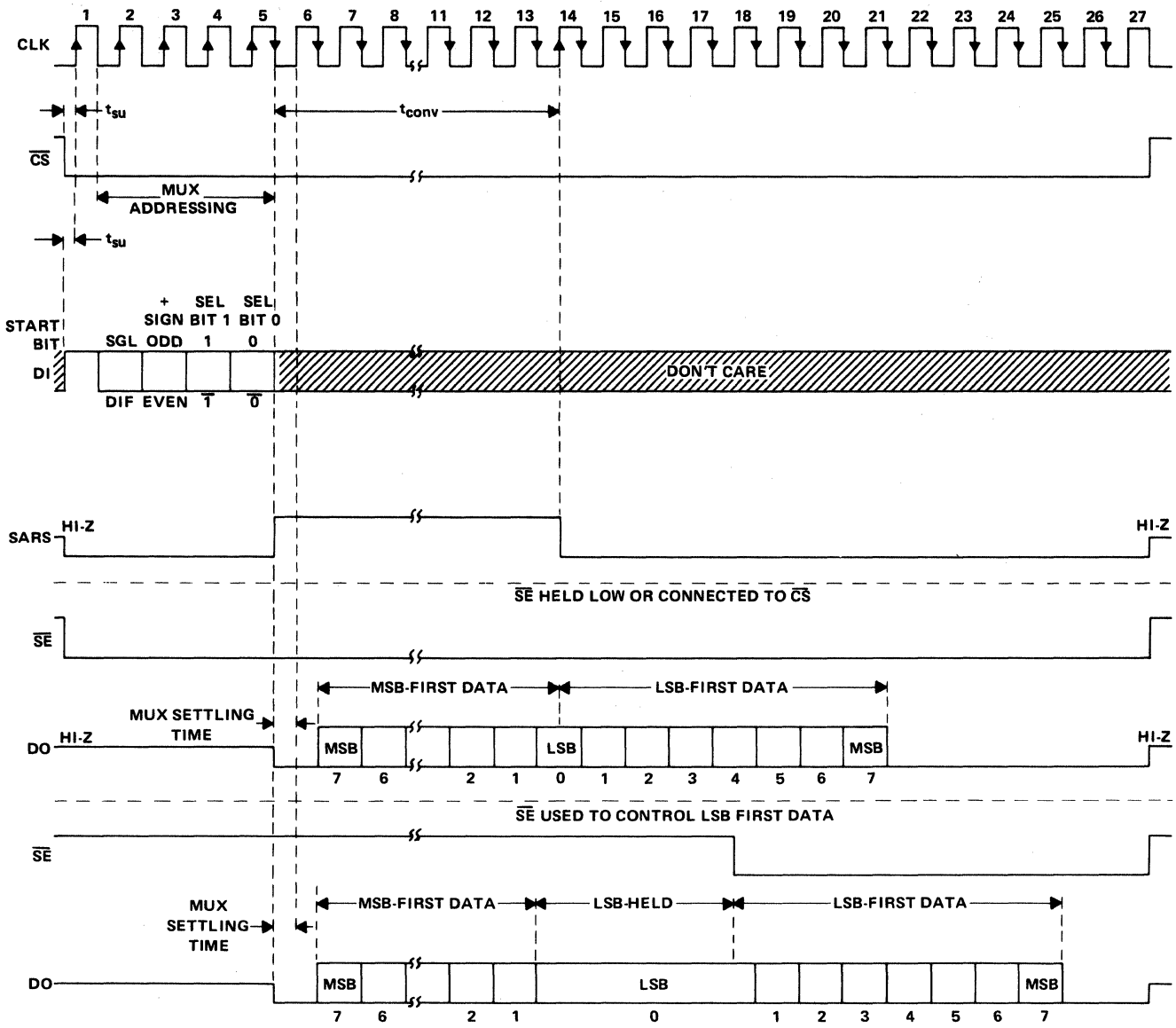


Figure 11-53. ADC0838 Sequence of Operation

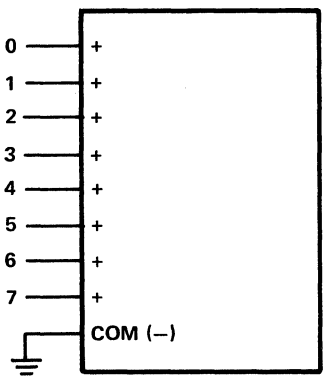
Principles of Operation

The ADC0831, ADC0832, ADC0834, and ADC0838 use a sample data comparator structure that converts differential analog inputs by a successive-approximation routine. The input voltage to be converted is applied to a channel terminal and is compared to ground (single-ended), to an adjacent channel (differential), or to a common terminal (pseudo differential) that can be an arbitary voltage. The input terminals are assigned a positive (+) or negative (−) polarity. If the signal input applied to the assigned positive terminal is less than the signal on the negative terminal, the converter output is all zeros.

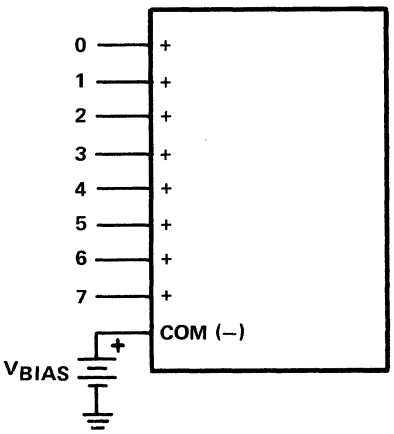
Channel selection and input configuration are under software control using a serial data link from the controlling processor. A serial communication format allows more functions to be included in a converter package with no increase in pin count. In addition, it eliminates the transmission of low-level analog signals by facilitating the remote location of the converter at the analog sensor. This process returns noise-free digital data to the processor.

A particular input configuration is assigned during the multiplexer addressing sequence. The multiplexer address is shifted into the converter through the data input (DI) line. (The ADC0831, unlike the ADC0832, ADC0834, and ADC0838, contains only one differential input channel having a fixed polarity assignment and does not have multiplexer addressing.) The multiplexer address selects the analog inputs to be enabled and determines whether the input is single-ended or differential. When the input is differential, the polarity of the channel input is assigned. Differential inputs are assigned to adjacent channel pairs. For example, channel 0 and channel 1 may be selected as a differential pair. However, these channels cannot act differentially with any other channel. In addition to selecting the differential mode, the polarity may also be selected. Either channel of the channel pair may be designated as negative or positive.

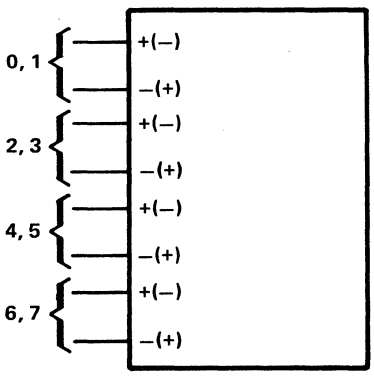
As shown in Figure 11-54, the ADC0838 has several input multiplexer options. In Figure 11-54(a), it is used for 8 single-ended inputs. In Figure 11-54(b), it is being used for a pseudo differential input. In this mode, the voltage on the COM(−) input is negative compared to any other channel. This voltage can be any reference potential common to all channel inputs. This feature is useful in single-supply applications where all analog circuits are biased to a potential other than ground. Figure 11-54(c) shows an ADC0838 set up with four differential inputs. Figure 11-54(d) illustrates



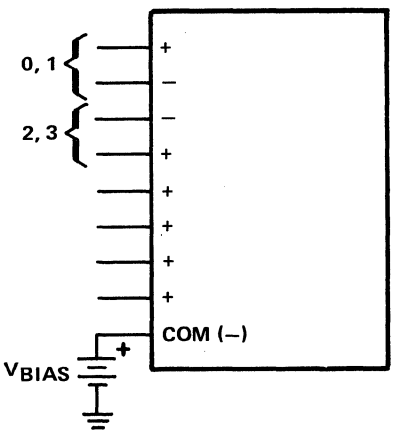
(a) 8 SINGLE-ENDED



(b) 8 PSEUDO-DIFFERENTIAL



(c) 4 DIFFERENTIAL



(d) MIXED MODE

Figure 11-54. Analog Input Multiplexer Options for ADC0838

the mixed mode option. Selection of this mode allows combinations of differential pairs and single-ended inputs.

A conversion is initiated by setting the chip select ($\overline{CS}$) input low, which enables all of the logic circuits. The $\overline{CS}$ input must be held low for the complete conversion process. On each low-to-high transition of the clock input received from the processor, the data on the DI input is clocked into the multiplexer address shift register. The first logic high on the input is the start bit. A 2-to-4 bit assignment word follows the start bit. On each successive low-to-high transition of the clock input, the start bit and assignment word are shifted through the shift register. When the start bit has been shifted into the start location of the multiplexer register, the input channel has been selected and conversion starts. The SAR status output (SARS) goes high to indicate that a conversion is in progress and the DI input to the multiplexer shift register is disabled for the duration of the conversion.

An interval of one clock period is automatically inserted to allow for the selected multiplexer channel to settle. The data output (DO) comes out of the high-impedance state and provides a leading low for this one clock period of multiplexer settling time. The SAR comparator compares successive outputs from the resistive-ladder with the incoming analog signal. The comparator output indicates whether the analog input is greater or less than the resistive-ladder output. This data is parallel loaded in to a 9-bit shift register that immediately outputs an 8-bit serial data word to the DO output with the most significant bit (MSB) first. After eight clock periods, the conversion is complete and the SAR status (SARS) output goes low. When $\overline{CS}$ goes high, all internal registers are cleared. At this time, the output circuits go to three state. If another conversion is desired, the $\overline{CS}$ line must make a high-to-low transition followed by address information.

In the ADC0831, only MSB-first data is output. The ADC0832 and ADC0834 output the LSB-first data after the MSB-first data stream. In the ADC0838, the programmer has the option of selecting MSB-first data or LSB-first data. To output LSB-first data, the shift enable ($\overline{SE}$) control input must go low. Data stored in the 9-bit shift register is now output with LSB first. The DI and DO pins can be tied together and controlled by a bidirectional processor I/O bit received on a single wire. This is possible because the DI input is examined only during the multiplexer addressing interval and the DO output is still in a high-impedance state.

TL500C THRU TL503C ANALOG-TO-DIGITAL CONVERTER BUILDING BLOCKS

TL500C/TL501C

The TL500C and TL501C analog processors have true differential inputs and automatic zero. They feature automatic polarity status and have a high input impedance in the range of $10^9\ \Omega$ typically. Figure 11-55 shows the pinout of the TL500C and TL501C. The TL500C has a resolution of 14 bits when used with the TL502C digital processor. It features a linearity error of 0.001% and has a 4-1/2 digit readout

N DUAL-IN-LINE PACKAGE

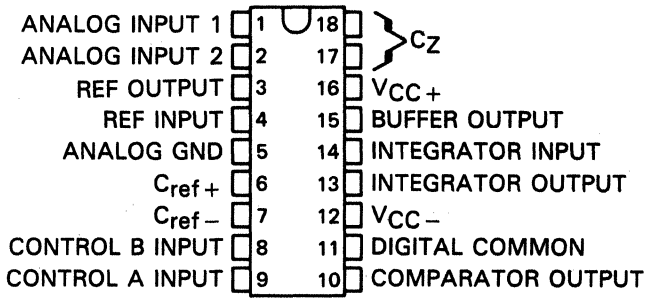


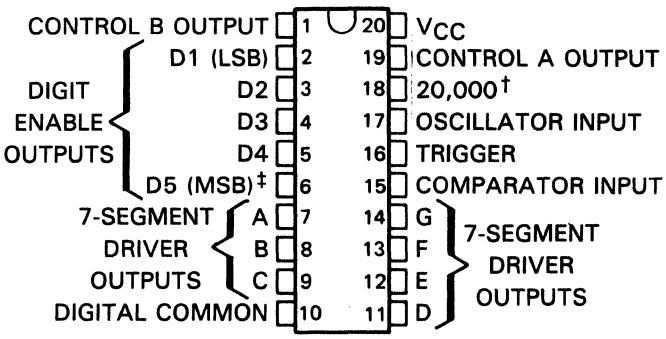
Figure 11-55. TL500C and TL501C Pinout (Top View)

accuracy when used with an external reference. The TL501C is capable of 10 to 13 bits of resolution when used with the TL502C processor. It has a linearity error of 0.01% and a 3-1/2 digit readout accuracy.

TL502C/TL503C

The TL502C and TL503C are digital processors which feature interdigit blanking as well as over-range blanking. They have fast display scan rates and the internal oscillator may be driven or free-running. These devices have 4-1/2 digit display circuitry. Figures 11-56 and 11-57 show the pinout of the TL502C and TL503C, respectively. The TL502C is compatible with popular 7-segment common-anode displays and features a high-sink-current segment driver for large displays. The TL503C features multiplexed BCD outputs with high sink current capability.

N DUAL-IN-LINE PACKAGE

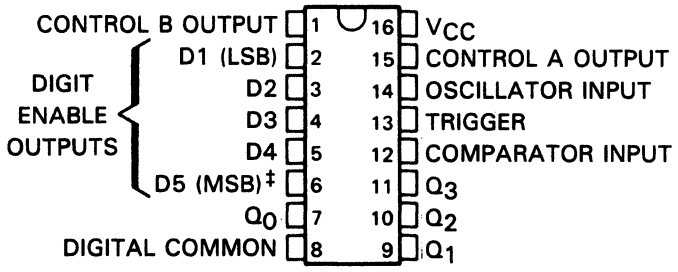


†Provides an output of $f_{osc} \div 20{,}000$.

‡Means D5, the most significant bit, is also the sign bit.

Figure 11-56. TL502 Pinout (Top View)

N DUAL-IN-LINE PACKAGE



‡Means D5, the most significant bit, is also the sign bit.

Figure 11-57. TL503 Pinout (Top View)

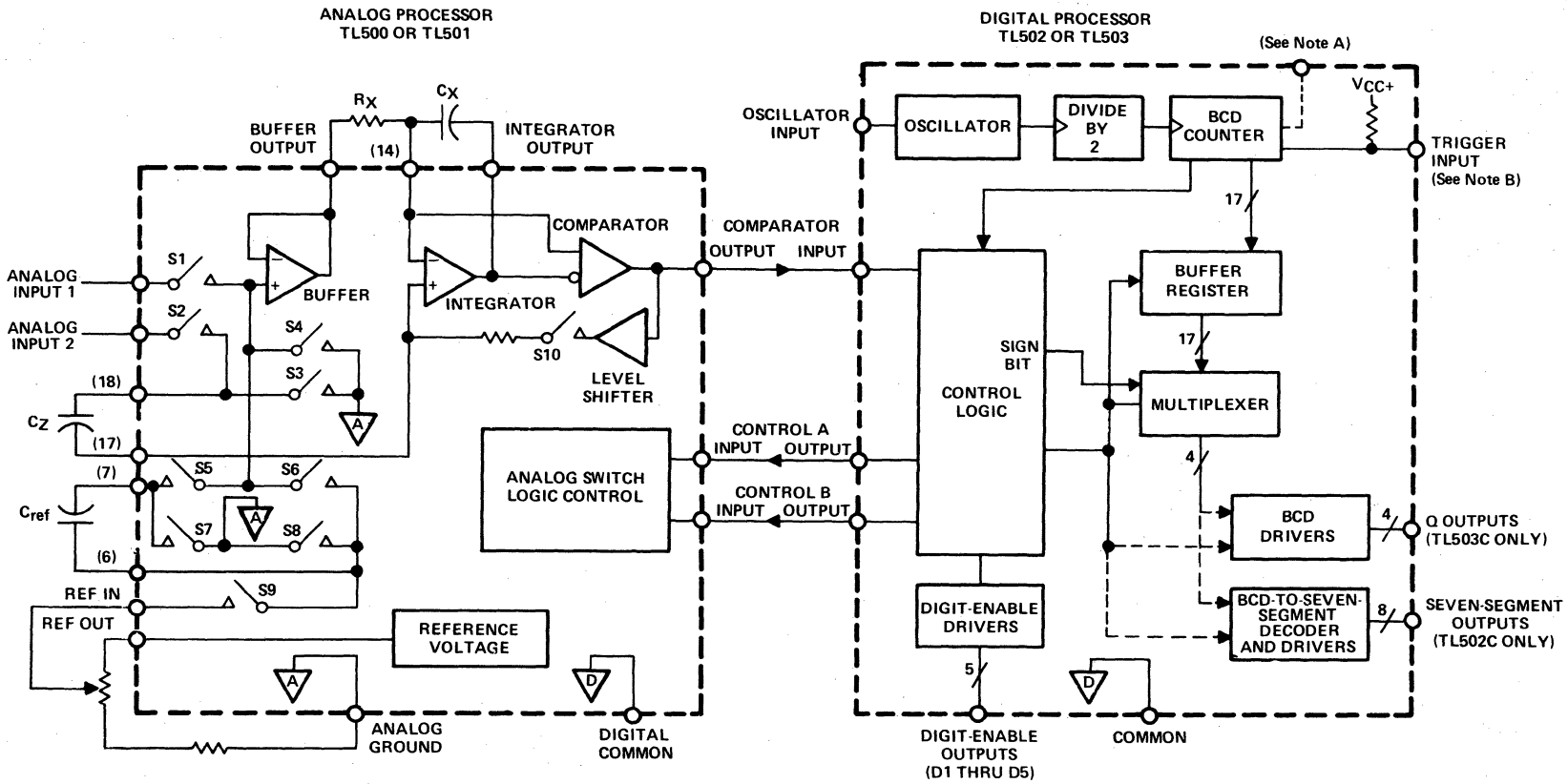
General Overall Description

The TL500C and TL501C analog processors and TL502C and TL503C digital processors provide the basic functions for a dual-slope-integrating analog-to-digital converter.

The TL500C and TL501C contain the necessary analog switches and decoding circuits, reference voltage generator, buffer, integrator, and comparator. These devices may be controlled by the TL502C, TL503C, by discrete logic, or by a software routine in a microprocessor.

The TL502C and TL503C both include oscillator, counter, control logic, and digit enable circuits. The TL502C provides multiplexed outputs for 7-segment displays, while the TL503C has multiplexed BCD outputs.

When used in complementary fashion, these devices form a system that features automatic zero-offset compensation, true differential inputs, high input impedance, and capability for 4-1/2 digit accuracy. Applications include the conversion of analog data from high-impedance sensors of pressure, temperature, light, moisture, and position. Analog-to-digital-logic conversion provides display and control signals for weight scales, industrial controllers, thermometers, light-level indicators, and many other applications. See Figure 11-58.



NOTES: A. Pin 18 of the TL502 provides an output of f_{osc} (oscillator frequency) ÷ 20,000.
B. The trigger input assumes a high level if not externally connected.

Figure 11-58. Block Diagram of Basic Analog-to-Digital Converter Using TL500C or TL501C and TL502C or TL503C

MODE	ANALOG INPUT	COMPARATOR	CONTROLS A AND B	ANALOG SWITCHES CLOSED
Auto Zero	X	Oscillation	L L	S3, S4, S7, S9, S10
Hold†				
Integrate Input	Positive	H	H H	S1, S2
	Negative	L		
Integrate Reference	X	L‡	L H	S3, S6, S7
		H‡	H L	S3, S5, S8

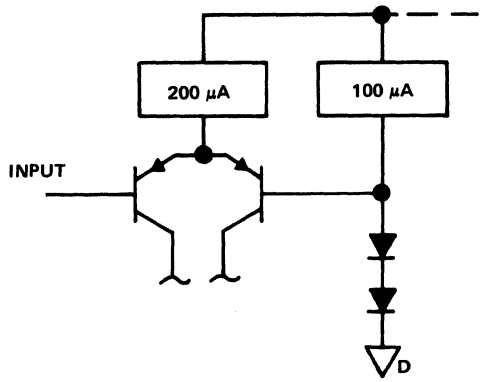
H ≡ High, L ≡ low, X ≡ Irrelevant

† If the trigger input is low at the beginning of the auto-zero cycle, the system will enter the hold mode. A high level (or open circuit) will signal the digital processor to continue or resume normal operation.

‡ This is the state of the comparator output as determined by the polarity of the analog input during the integrate input phase.

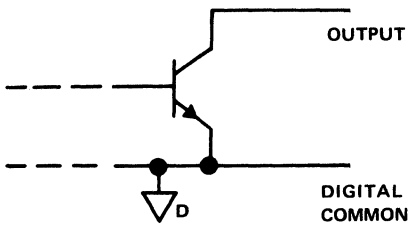
Description of TL500C and TL501C Analog Processors

The TL500C and TL501C analog processors are designed to compensate automatically for internal zero offsets, integrate a differential voltage at the analog inputs, integrate a voltage at the reference input in the opposite direction, and provide an indication of zero-voltage crossing. The external control mechanism may be a microcomputer and software routine, discrete logic, or a TL502C or TL503C digital processor. The TL500C and TL501C are designed primarily for simple, cost-effective, dual-slope analog-to-digital converters. Both devices feature true differential analog inputs, high input impedance, and an internal reference-voltage source. See Figure 11-59 for the input schematic and Figure 11-60 for the output schematic. The TL500C provides 4-1/2 digit readout accuracy when used with a precision external reference voltage. The TL501C provides 100-ppm linearity error and 3-1/2 digit accuracy capability. These devices are manufactured using TI's advanced technology to produce JFET, MOSFET, and bipolar devices on the same chip. The TL500C and TL501C are intended for operation over the temperature range of 0 °C to 70 °C.



CONTROL A AND CONTROL B INPUTS

Figure 11-59. TL500C and TL501C Input Schematic



COMPARATOR OUTPUT

Figure 11-60. TL500C and TL501C Output Schematic

Description of TL502C/503C Digital Processors

The TL502C and TL503C are control logic devices designed to complement the TL500C and TL501C analog processors. They feature an internal oscillator, interdigit blanking, and fast display scan rate. The internal-oscillator input is a Schmitt trigger circuit that can be driven by an external clock pulse or provide its own time base with the addition of a capacitor. The typical oscillator frequency is 120 kHz with a 470-pF capacitor connected between the oscillator input and ground.

The TL502C provides 7-segment-display output drivers capable of sinking 100 mA and compatible with popular common-anode displays. The TL503C has four BCD output drivers capable of 100-mA sink current. The code for each digit is multiplexed to output drivers in phase with a pulse on the appropriate digit-enable line at a digit rate equal to f_{osc} divided by 200 (Table 11-7 and Figure 11-61). Each digit-enable output is capable of sinking 20 mA. Figure 11-62 shows input/output schematics of the TL502C and TL503C. Table 11-8 is the Table of Special Functions.

Table 11-7

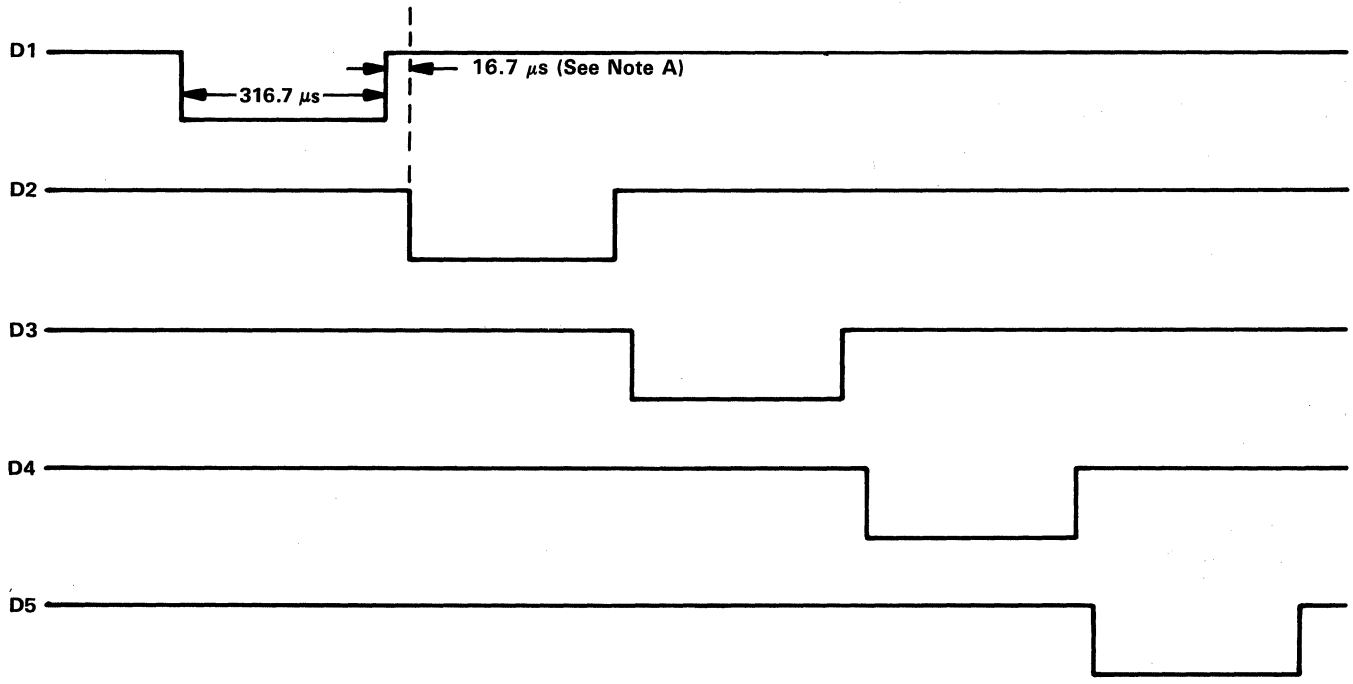
(a) DIGITS 1 THRU 4 NUMERIC CODE

NUMBER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3 8	Q2 4	Q1 2	Q0 1
0	L	L	L	L	L	L	H	L	L	L	L
1	H	L	L	H	H	H	H	L	L	L	H
2	L	L	H	L	L	H	L	L	L	H	L
3	L	L	L	L	H	H	L	L	L	H	H
4	H	L	L	H	H	L	L	L	H	L	L
5	L	H	L	L	H	L	L	L	H	L	H
6	L	H	L	L	L	L	L	L	H	H	L
7	L	L	L	H	H	H	H	L	H	H	H
8	L	L	L	L	L	L	L	H	L	L	L
9	L	L	L	L	H	L	L	H	L	L	H

H = high level, L = low level

(b) DIGIT 5 (MOST SIGNIFICANT DIGIT) CHARACTER CODES

CHARACTER	TL502C SEVEN-SEGMENT LINES							TL503C BCD OUTPUT LINES			
	A	B	C	D	E	F	G	Q3 8	Q2 4	Q1 2	Q0 1
+	H	H	H	H	L	L	L	H	L	H	L
+1	H	L	L	H	L	L	L	H	H	H	L
−	L	H	H	L	H	H	L	H	L	H	H
−1	L	L	L	L	H	H	L	H	H	H	H



NOTE A: The BCD or seven-segment driver outputs are present for a particular digit slightly before the falling edge of that digit enable.

Figure 11-61. TL502 and TL503 Digit Timing with 120 kHz Clock Signal at Oscillator Input

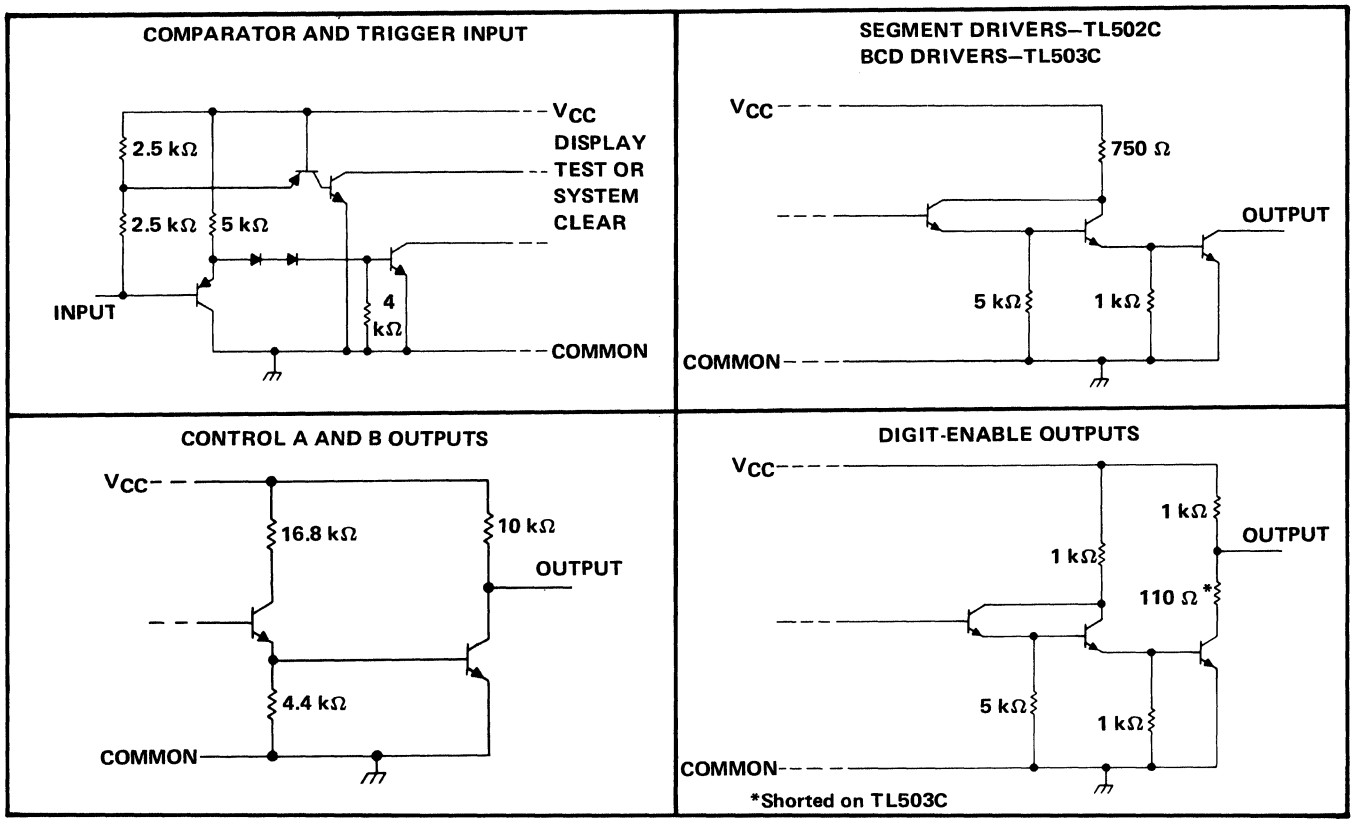


Figure 11-62. TL502C and TL503C Inputs and Outputs Schematics

Table 11-8. Table of Special Functions*

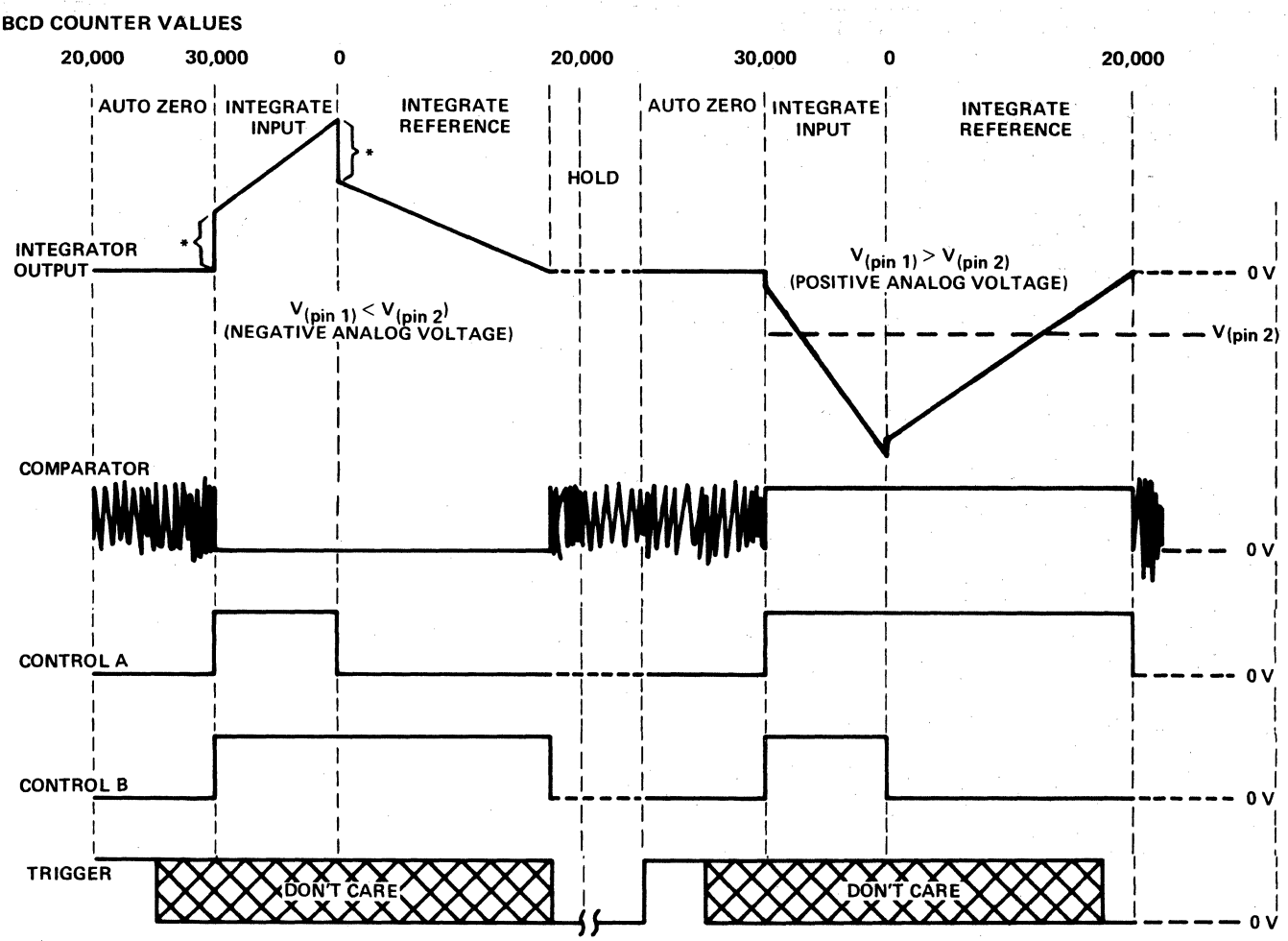
TRIGGER INPUT	COMPARATOR INPUT	FUNCTION
$V_I \leq 0.8$ V	$V_I \leq 6.5$ V	Hold at auto-zero cycle after completion of conversion
2 V $\leq V_I \leq$ 6.5 V	$V_I \leq 6.5$ V	Normal operation (continuous conversion)
$V_I \leq 6.5$ V	$V_I \geq 7.9$ V	Display Test: All BCD outputs high
$V_I \geq 7.9$ V	$V_I \leq 6.5$ V	Internal Test
Both inputs go to $V_I \geq 7.9$ V simultaneously		System Clear: Sets CBC counter to 20,000. When normal operation is resumed, cycle begins with Auto Zero.

*V_{CC} = 5 V ± 10%

The comparator input of each device, in addition to monitoring the output of the zero-crossing detector in the analog processor, may be used in the display test mode to check for wiring and display faults. A high logic level (2 to 6.5 V) at the trigger input with the comparator input at or below 6.5 V starts the integrate-input phase. Voltage levels equal to or greater than 7.9 V on both the trigger and comparator inputs clear the system and set the BCD counter to 20,000. When normal operation resumes, the conversion cycle is restarted at the zero phase. These devices are manufactured using I^2L and bipolar technologies.

Principles of Operation

The basic principle of dual-slope-integrating converters is relatively simple (refer to Figure 11-58). The relationship of the charge and discharge values is shown in Figure 11-63.



*This step is the voltage at pin 2 with respect to analog ground.

Figure 11-63. Voltage Waveforms and Timing Diagram

Capacitor, C_X, is charged through the integrator from V_{CT} for a fixed period of time at a rate determined by the value of the unknown voltage input. The capacitor is then discharged at a fixed rate determined by the reference voltage back to V_{CT} where the discharge time is measured precisely.

$$V_{CX} = V_{CT} - \frac{V_I\, t_1}{R_X C_X} \quad \text{charge} \qquad (1)$$

$$V_{CT} = V_{CX}\, \frac{V_I}{V_{ref}} = -\frac{t_2}{t_1} \quad \text{discharge} \qquad (2)$$

Combining equations 1 and 2 results in:

$$\frac{V_I}{V_{ref}} = -\frac{t_2}{t_1} \qquad (3)$$

where:

V_{CT} = Comparator (offset) threshold voltage
V_{CX} = Voltage change across C_X during t_1 and t_2 (equal in magnitude)
V_I = Average value of input voltage during t_1
t_1 = Time period over which unknown voltage is integrated
t_2 = Unknown time period over which a known reference voltage is integrated

Equation (3) illustrates the major advantages of a dual-slope converter:

1. Accuracy is not dependent on absolute values of t_1 and t_2, but is dependent on their ratios. Long-term clock frequency variations will not affect the accuracy.
2. Offset values, V_{CT}, are not important.

The BCD counter in the digital processor (Figure 11-58) changes at a rate equal to one-half the oscillator frequency. The BCD counter and the control logic divide each measurement cycle into three phases.

Auto-Zero Phase

The cycle begins at the end of the integrate-reference phase when the digital processor applies low levels to inputs A and B of the analog processor. If the trigger input is at a high level, a free-running condition exists and continuous conversions are made. However, if the trigger input is low, the digital processor stops the counter at 20,000, entering a hold mode. In this mode, the processor samples the trigger input every 4000 oscillator pulses until a high level is detected. When this occurs, the counter is started again and is carried to completion at 30,000. The reference voltage is stored in the reference capacitor C_{ref}, comparator offset voltage is stored in the integration capacitor C_X, and the sum of the buffer and integrator offset voltages is stored on auto-zero capacitor C_Z. During the auto-zero phase, the comparator output is characterized by an oscillation (limit cycle) of indeterminate waveform and frequency that is filtered and dc shifted by the level shifter.

Integrate-Input Phase

The auto-zero phase is completed at a BCD count of 30,000, and high levels are applied to both control inputs to initiate the integrate-input phase. The integrator charges C_X for a fixed time of 10,000 BCD counts at a rate determined by the input voltage. Note that during this phase, the analog inputs see only the high impedance of the noninverting operational amplifier input. Therefore, the integrator responds only to the difference between the analog input terminals, providing true differential inputs.

Integrate-Reference Phase

At a BCD count of 39,999 + 1 = 40,000 or 0, the integrate-input phase is terminated and the integrate-reference phase is begun by sampling the comparator output. If the comparator output is low, corresponding to a negative average analog input voltage, the digital processor applies a low and a high to control inputs A and B, respectively, the positive side of the reference voltage stored on C_{ref} is applied to the buffer. If the comparator output is high, corresponding to a positive input, control inputs A and B are made high and low, respectively, and the negative side of the stored reference voltage is applied to the buffer. In either case, the processor automatically selects the proper logic state to cause the integrator to ramp back toward zero at a rate proportional to the reference voltage. The time required to return to zero is measured by the counter in the digital processor. The phase is terminated when either the integrator output crosses zero and the counter contents are transferred to the register, or the BCD counter reaches 20,000 and the overrange indication is activated. When activated, the overrange indication blanks all but the most significant digit and sign.

Seventeen parallel bits (4-1/2 digits) of information are strobed into the buffer register at the end of the integration phase. Information for each digit is multiplexed out to the BCD outputs (TL503C) or the 7-segment drivers (TL502C) at a rate equal to the oscillator frequency divided by 400.

Capacitor Selection Guidelines

The auto-zero capacitor C_Z and reference capacitor C_{ref} should be within the recommended range of operating conditions and should have low leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. A polypropylene-dielectric capacitor similar to TRW's X363UW is recommended for 4-1/2 digit accuracy. For 3-1/2 digit applications, polyester, polycarbonate, and other film dielectrics are usually suitable. Ceramic and electrolytic capacitors are not recommended.

The time constant R_XC_X should be kept as near the minimum value as possible and is given by the formula:

$$\text{Minimum } R_XC_X = \frac{V_{ID}\ (\text{full scale})\ t_I}{V_{OM-} - V_{I(\text{pin 2})}}$$

where:

V_{ID} (full scale) = Voltage on pin 1 with respect to pin 2
t_I = Input integration time in seconds
$V_{I(\text{pin 2})}$ = Voltage on pin 2 with respect to analog ground

Bypassing and Stray Coupling

Stray coupling from the comparator output to any analog pin (in order of importance 17, 18, 14, 7, 6, 13, 1, 2, 15) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01 μF ceramic capacitor.

Analog and digital common are internally isolated and may be at different potentials. Digital common can be within 4 V of the positive or negative supply with the logic decode still functioning properly.

TL505C ANALOG-TO-DIGITAL CONVERTER

The TL505 is a dual-slope A/D converter with 1-bit resolution and a 3-digit accuracy of 0.1%. It has an internal reference, automatic zero, and operates from a single supply. It features a high-impedance MOS input and consumes typically only 40 mW of power. It is designed chiefly for use with the TMS1000 microprocessor family for low-cost, high-volume applications. Figure 11-64 shows the package pin assignment.

Description

The TL505C is an analog-to-digital converter building block designed for use with TMS1000 type microprocessors. See Figure 11-65 for the functional block diagram. The TL505C contains the analog elements (operational amplifier, comparator, voltage reference, analog switches, and switch

drivers) necessary for a unipolar automatic-zeroing dual-slope converter. The logic for the dual-slope conversion can be performed by the associated MPU as a software routine or it can be implemented with other components such as the TL502C logic-control device.

The high-impedance MOS inputs permit the use of less expensive, lower value capacitors, and conversion speeds from 20 per second to 0.05 per second.

N DUAL-IN-LINE PACKAGE

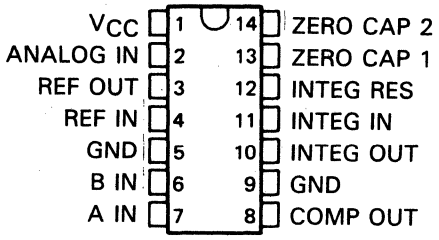


Figure 11-64. TL505C Pinout (Top View)

Definition of Terms

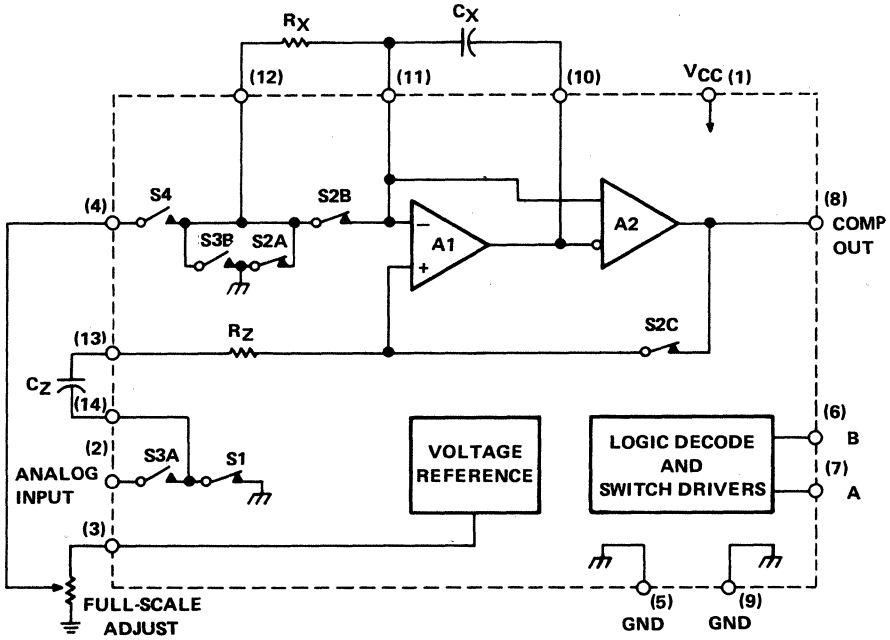
Zero Error — The intercept (b) of the analog-to-digital converter system transfer function $y = mx + b$, where y is the digital output, x is the analog input, and m is the slope of the transfer function, which is approximated by the ratiometric reading.

Linearity Error — The maximum magnitude of the deviation from a straight line between the end points of the transfer function.

Ratiometric Reading — The ratio of negative integration time (t_2) to positive integration time (t_1).

Principles of Operation

A block diagram of an MPU system utilizing the TL505C is shown in Figure 11-66. The TL505C operates in a modified positive-integration three-step dual-slope conversion mode. The A/D converter waveforms during the conversion process are illustrated in Figure 11-67.



NOTE: Analog and digital GND are internally connected together.

Figure 11-65. Functional Block Diagram

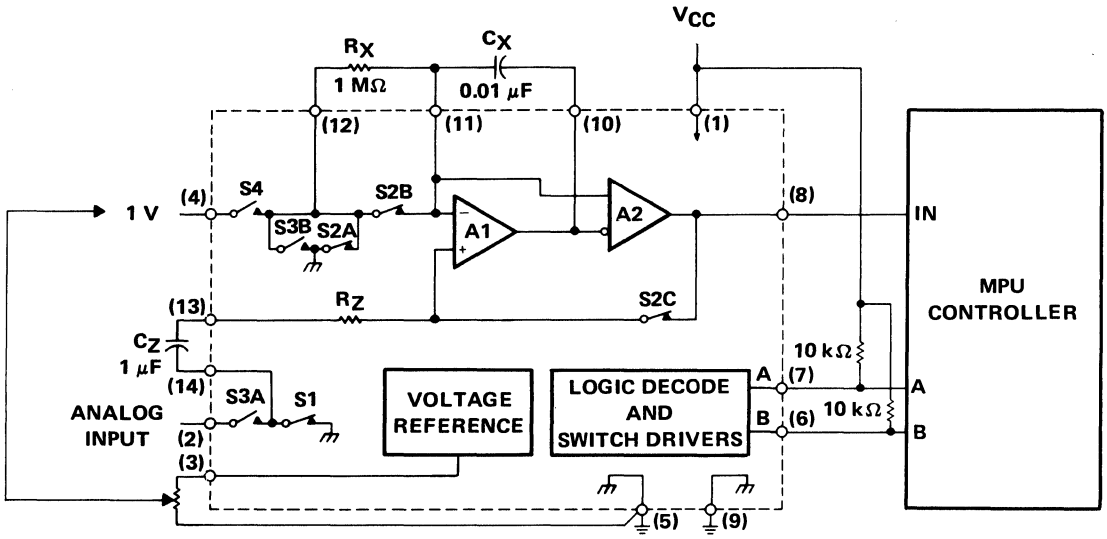
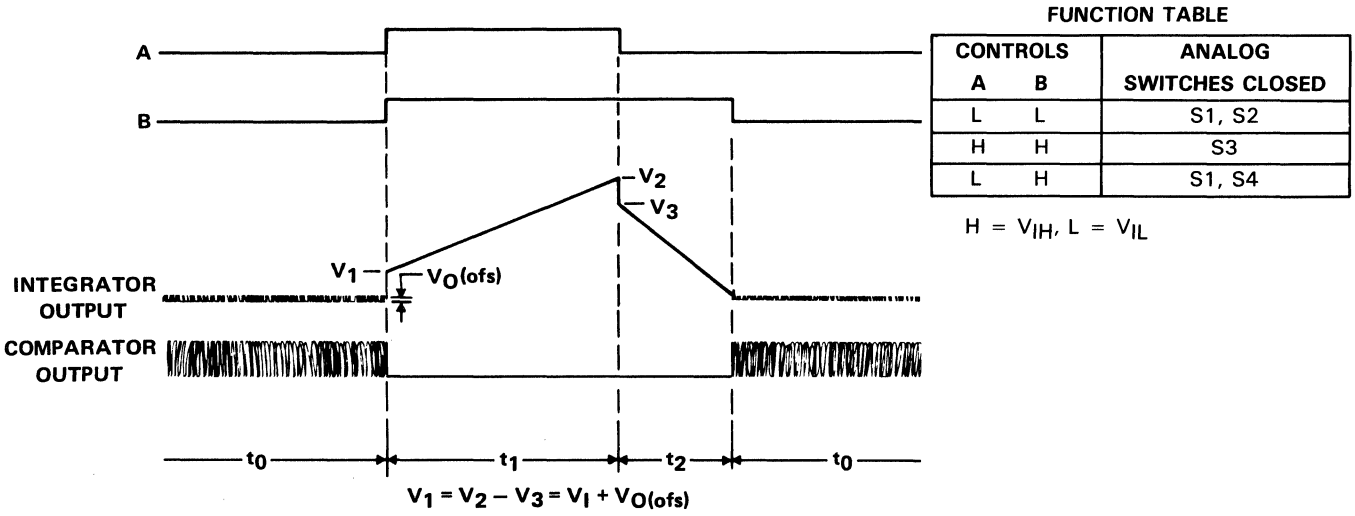


Figure 11-66. Functional Block Diagram of TL505C Interface with a Microprocessor System



FUNCTION TABLE

CONTROLS A	CONTROLS B	ANALOG SWITCHES CLOSED
L	L	S1, S2
H	H	S3
L	H	S1, S4

H = V_{IH}, L = V_{IL}

Figure 11-67. Conversion Process Timing Diagrams

The first step of the conversion cycle is the auto-zero period t_0 during which the integrator offset is stored in the auto-zero capacitor and the offset of the comparator is stored in the integrator capacitor. To accomplish this, the MPU takes both the A and B inputs low. This is decoded by the switch drivers, which close S1 and S2. The output of the comparator is connected to the input of the integrator through the low-pass filter consisting of R_Z and C_Z. The closed loop of A1 and A2 will seek a null condition where the offsets of the integrator and comparator are stored in C_Z and C_X, respectively. This null condition is characterized by a high-frequency oscillation at the output of the comparator. The purpose of S2B is to shorten the amount of time required to reach the null condition.

At the conclusion of t_0, the MPU takes both A and B inputs high. This closes S3 and opens all the other switches. The input signal V_I is applied to the noninverting input of A1 through C_Z. V_I is then positively integrated by A1. Since the offset of A1 is stored in C_Z, the change in voltage across C_X will be due to only the input voltage. It should be noted that since the input is integrated in a positive integration during t_1, the output of A1 will be the sum of the input voltage, the integral of the input voltage and the comparator offset, as shown in Figure 11-67. The change in voltage across capacitor C_X during t_1 is given by:

$$V_{CX(1)} = \frac{V_I\, t_1}{R_1\, C_X} \qquad (1)$$

where

$R_1 = R_X + R_{S3B}$ and R_{S3B} is the resistance of switch S3B.

At the end of t_1, the MPU takes the A input low and the B input high. This turns on S1 and S4; all other switches are turned off. In this state, the reference is integrated by A1 in a negative sense until the integrator output reaches the comparator threshold. At this point, the comparator output goes high. This change in state is sensed by the MPU, which terminates t_2 by again taking the A and B inputs both low. During t_2, the change in voltage across C_X is given by:

$$V_{CX(2)} = \frac{V_{ref}\, t_2}{R_2} \qquad (2)$$

where

$R_2 = R_X + R_{S4} + R_{ref}$ and R_{ref} is the equivalent resistance divider.

Since $V_{CX1} = V_{CX2}$, equations (1) and (2) can be combined to give

$$V_I = V_{ref}\frac{R_1\, t_2}{R_2\, t_1} \qquad (3)$$

This equation is a variation on the ideal dual-slope equation, which is

$$V_I = V_{ref}\frac{t_2}{t_1} \qquad (4)$$

Ideally then, the ratio of R1/R2 would be exactly equal to one. In a typical TL505C system where $R_X = 1\ M\Omega$, the scaling error introduced by the difference in R_1 and R_2 is so small that it can be neglected, and equation (3) reduces to (4).

TL507I, TL507C
ANALOG-TO-DIGITAL CONVERTER

The TL507 is an economical single-slope, 7-bit resolution A/D converter. It features guaranteed monotonicity and ratiometric conversion. Operating from a single supply, it consumes only 25 mW of power at a supply voltage of 5 V and has a conversion speed of approximately 1 ms. See Figure 11-68 for the pin assignment of this converter.

P DUAL-IN-LINE PACKAGE

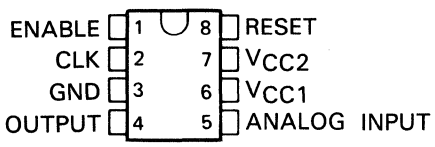


Figure 11-68. TL507 Pinout (Top View)

Description

The TL507 is a single-slope A/D converter designed to convert analog input voltages between 0.25 V_{CC} and 0.75 V_{CC} into a pulse width modulated output code. It contains a 7-bit synchronous counter, a binary weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

In continuous operation, it is possible to obtain conversion speeds up to 1000 per second. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation coupled with low cost, make this converter especially useful for a wide variety of applications. See Figure 11-69 for the functional block diagram and Figure 11-70 for input/output schematics.

Definition of Terms

Zero Error — The intercept (b) of the A/D converter system function $y = mx + b$, where y is the output of the ladder network, x is the analog input, and m is the slope of the transfer function.

Overall Error — The magnitude of the deviation from a straight line between the endpoints of the transfer function.

Differential Nonlinearity — Maximum deviation of an analog value change that is associated with a 1 bit code change (1 clock pulse) from its theoretical value of 1 LSB.

Principles of Operation

The TL507 like all single-slope converters is basically a voltage-to-time or current-to-time converter. An external clock signal is applied through a buffer to a negative edge triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from 0.75 V_{CC1} down to 0.25 V_{CC1}. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault detector. With the analog input voltage within the 0.25 V_{CC1} to 0.75 V_{CC1} range, the duty cycle of the output signal is determined by the unknown analog input as shown in the waveform and function table in Figure 11-71.

For illustration, assume $V_{CC1} = 5.12$ V,

$0.25\ V_{CC1} = 1.28$ V

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\ V_{CC1})}{128} = 20 \text{ mV}$$

$0.75\ V_{CC1} - 1 \text{ count} = 3.82$ V

The output is an open-collector npn transistor capable of withstanding up to 18 V in the off state. The output is current limited within the 8 mA to 12 mA range; however, care must be taken to ensure that the output does not exceed 5.5 V in the on state. The voltage regulator section allows operation from either an unregulated 8 V to 18 V V_{CC2} supply source or a regulated 3.5 V to 6 V V_{CC1} supply. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open.

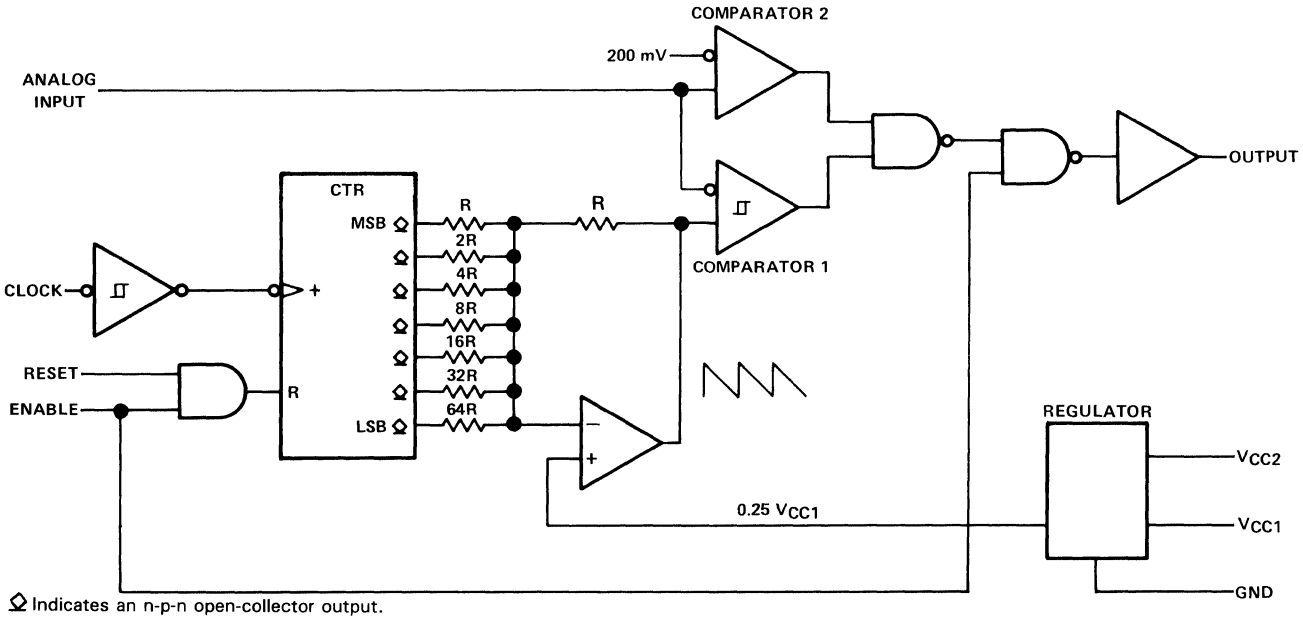
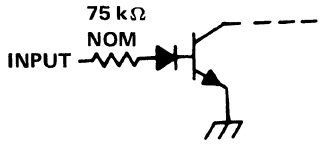
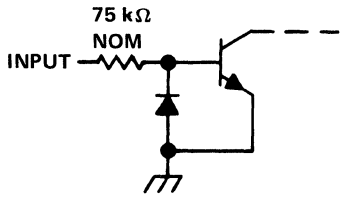


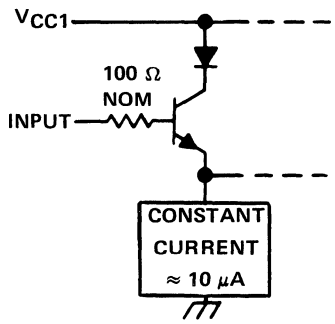
Figure 11-69. TL507 Functional Block Diagram



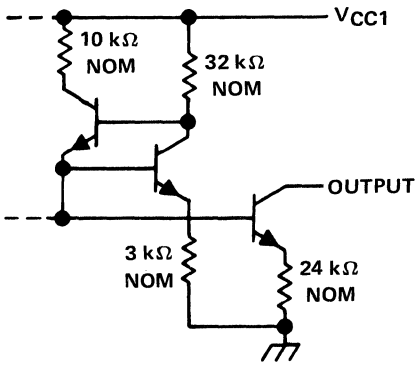
(a) EQUIVALENT OF ENABLE AND RESET INPUTS



(b) EQUIVALENT OF CLOCK INPUT

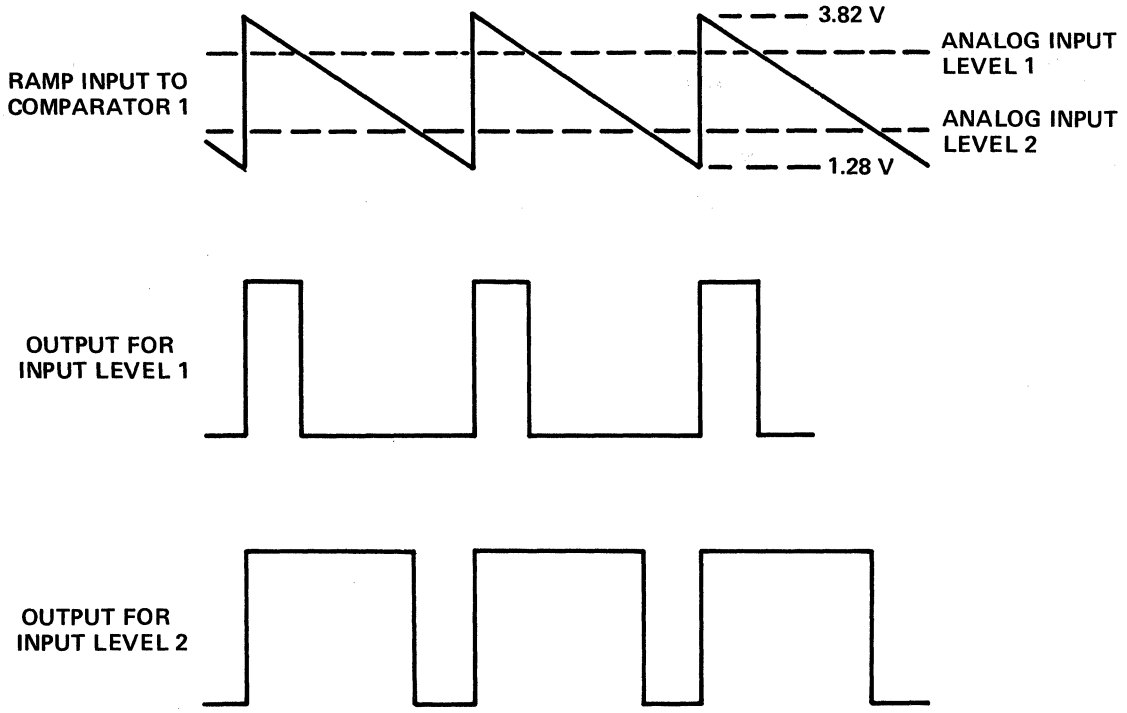


(c) EQUIVALENT OF ANALOG INPUT



(d) OUTPUT

Figure 11-70. Schematics of Inputs and Outputs



FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
V_I < 200 mV	H	L
V_{ramp} > V_I > 200 mV	H	H
V_I > V_{ramp}	H	L

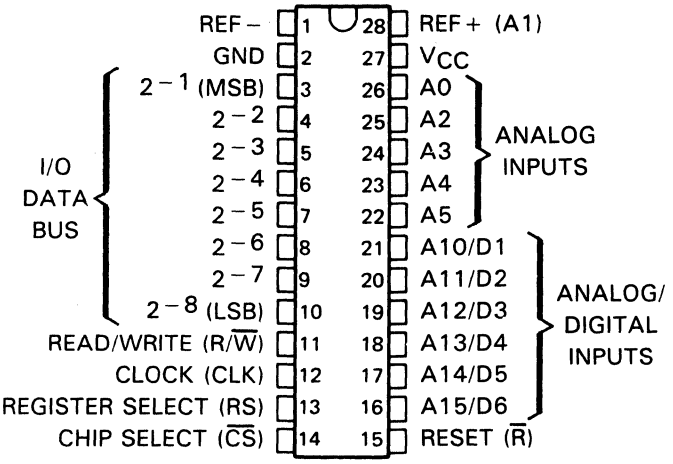
†Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

A high level on the reset pin clears the counter to zero, which sets the internal ramp to 0.75 V_{CC}. Internal pull-down resistors keep the reset and enable pins low when not connected.

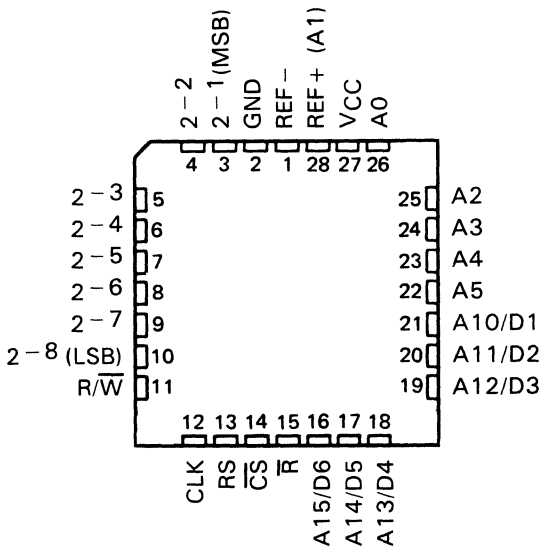
Figure 11-71. TL507 Function Table and Timing Diagram

TLC532, TLC533 LinCMOS 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH 5 ANALOG AND 6 MULTIPURPOSE INPUTS

The TLC532 and TLC533 are 8-bit A/D converters built with the LinCMOS technology. The unadjusted error is ±0.5 LSB and the devices feature ratiometric conversion. The I/O bus is three-state bidirectional. The access plus conversion time is 15 μs maximum for the TLC532 and 30 μs for the TLC533. There are 5 analog and 6 multipurpose inputs plus an analog on-chip 12-channel mixer. Other features are three on-chip sample-and-hold functions and 5 V single supply operation. Power consumption is low, typically 6.5 mW. Figure 11-72(a) and (b) show the device pinouts. The I/O data bus lines as well as the analog input lines are grouped together for efficient PC board layout.



(a) J OR N DUAL-IN-LINE PACKAGE



(b) FN CHIP-CARRIER PACKAGE

Figure 11-72. TLC532A and TLC533A Pinouts (Top View)

Description

The TLC532A and TLC533A are monolithic LinCMOS peripheral intergrated circuits each designed to interface with a microprocessor for analog data acquisition. Figure 11-73 shows the function table and Figure 11-74 is the functional block diagram. These devices are complete peripheral data acquisition systems on a single chip that can convert analog signals to digital data from up to 11 external analog terminals. Each device features operation from a single 5-V supply. Each contains a 12-channel analog multiplexer, an 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold, three 16-bit registers, and microprocessor-compatible control logic circuitry. Additional features include a built-in self-test, six multipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accessed via the microprocessor data bus in two 8-bit bytes (most significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or six digital signals and the positive reference voltage that may be used for self-test.

The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored in 10 μs (TLC532A) or 20 μs (TLC533A) after instructions from the microprocessor have been recognized. The on-chip sample-and-hold functions automatically miniminze errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

ADDRESS/CONTROL					DESCRIPTION
R/W	RS	CS	R	CLK	
X	X	X	L†		Reset
L	H	L	H	↓	Write bus data to control register
H	L	L	H	↑	Read data from analog conversion register
H	H	L	H	↑	Read data from digital data register
X	X	H	H	X	No response

H = High-level, L = Low-level, X = Irrelevant
↓ = High-to-low transition, ↑ = Low-to-high transition
†For proper operation, Reset must be low for at least three clock cycles.

Figure 11-73. Function Table

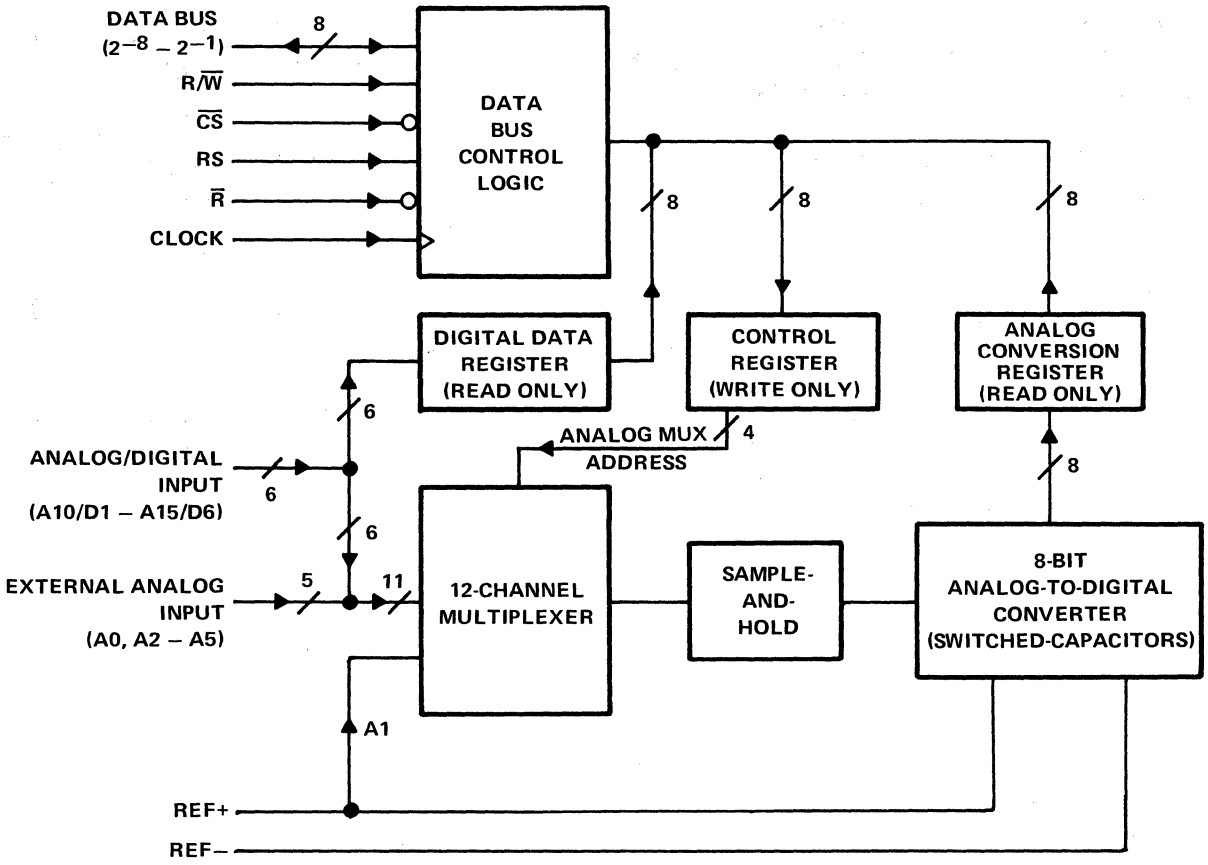


Figure 11-74. Functional Block Diagram

Principles of Operation

The TLC532A and TLC533A can be directly connected to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible three-state data bus, the three control inputs (Read/Write, Register Select, and Chip Select), and the Clock input. Each device contains three 16-bit internal registers. These registers are the control register, the analog conversion data register, and the digital data register.

A high level at the Read/Write input and a low level at the Chip Select input set the device to output data on the 8-line data bus for the microprocessor. A low level at the Read/Write input and a low level at the Chip Select input set the device to receive instructions into the internal control register on the 8-line data bus from the microprocessor. When the device is in the read mode and the Register Select input is at a low level, the microprocessor reads the data contained in the digital data register.

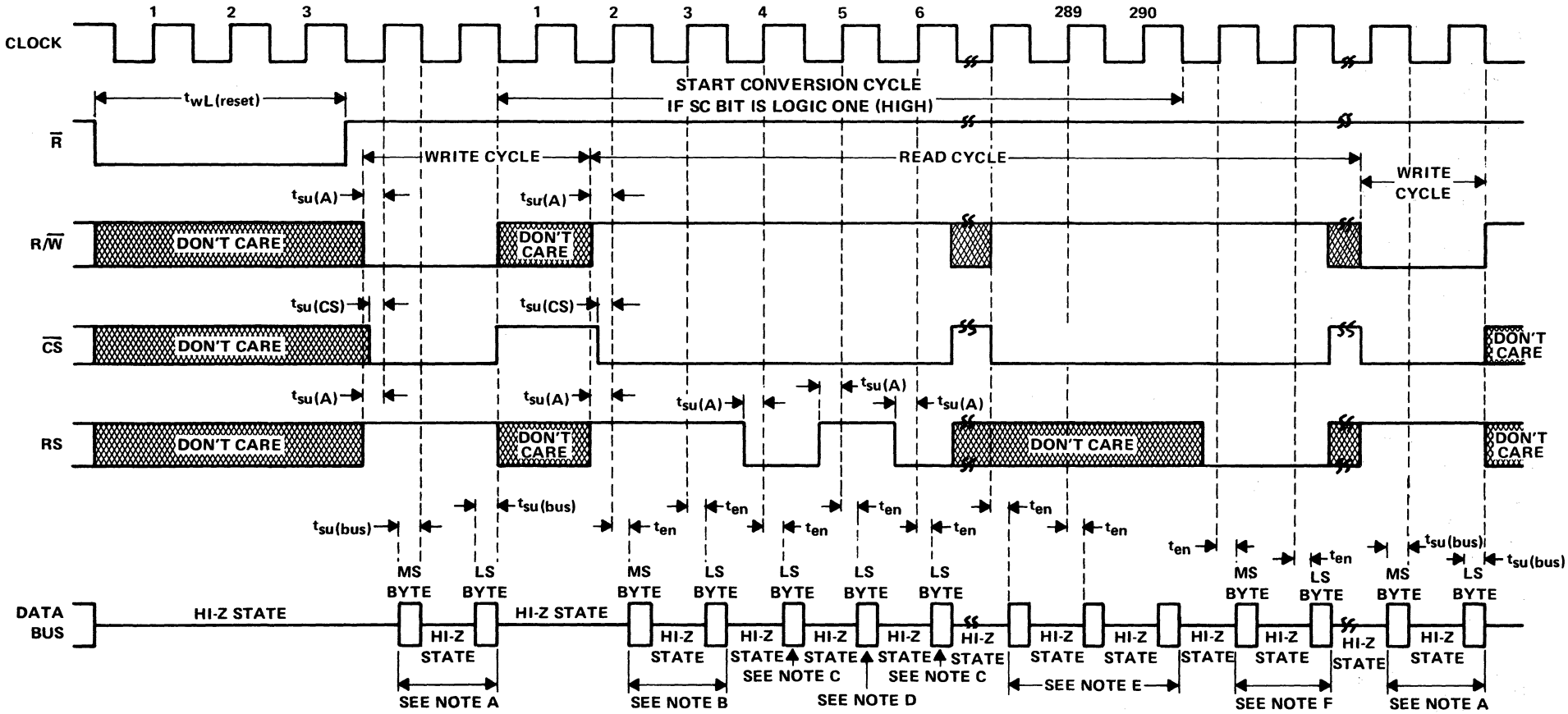
The control register is a write-only register into which the microprocessor writes the command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and the most recent conversion results. The digital data register is also a read-only register that holds the digital input

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the clock input in a normal 16-bit microprocessor instruction. The internal pointer will automatically point to the most significant byte any time that the Chip Select is at a high level for at least one clock cycle. This causes the device to treat the next signal on the 8-line data bus as the most significant (MS) byte. A low level at the Chip Select input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the Clock goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the least significant (LS) byte and remains there for as long as Chip Select is low. The MS byte of any register may be accessed by either an 8-bit or 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

Noramlly, a two-byte word is written into or read from the controlling microprocessor, but a single byte can be read by the microprocessor by proper manipulation of the Chip Select input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register.

A conversion cycle is started after a two-byte instruction is written into the control register and the start conversion (SC) bit is a logic high. This two-byte instruction also selects the input analog channel to be converted. The end-of-conversion (EOC) status bit in the analog conversion data register is reset and it remains at that level until the conversion is completed, when the status bit is set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cycle is completed. If a new conversion command is entered into the coantrol register while the conversion cycle is in progress, the on-going conversion will immediately begin.

The Reset input allows the device to be externally forced to a known state. When a low level is applied to the Reset input for a minimum of three clock periods, the start conversion bit of the control register is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the Reset input going to a low level. A typical operating sequence timing diagram is shown in Figure 11-75.



NOTES: A. This is a 16-bit input instruction from the microprocessor being sent to the control data register.
B. This is the 2-byte (16-bit) content of the digital data register being sent to the mircoprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor.
E. These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor.

Figure 11-75. Typical Operating Sequence

TLC540, TLC541 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

The TLC540 and TLC541 are LinCMOS A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. Included is an on-chip 12-channel analog multiplexer and built-in self-test mode. The sample-and-hold is software controllable. Total unadjusted error is ± 0.5 LSB max. The pin layout is shown in Figures 11-76(a) and (b).

Typical Performance	TLC540	TLC541
Acquisition Time	2 μs	3.6 μs
Conversion Time	9 μs	17 μs
Sampling Rate	75×10^3	40×10^3
Power Dissipation	6 mW	6 mW

Description

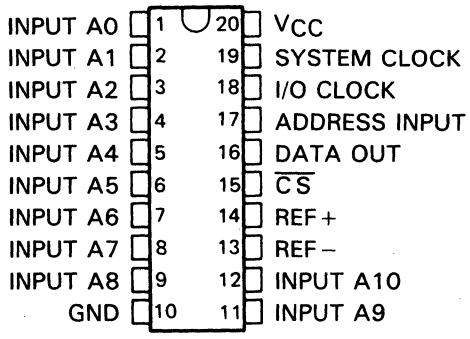
The TLC540 and TLC541 are LinCMOS A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs (including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input). The system clock is a 4-MHz clock for the TLC540 and a 2.1-MHz clock for the TLC541. Figure 11-77 shows a functional block diagram. Each device design features simultaneous read/write operation that allows high-speed data transfers and sample rates of up to 75,180 samples per second for the TLC540 and 40,000 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under processor control.

The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 9 μs for the TLC540 and 17 μs for the TLC541 over the full operating temperature range.

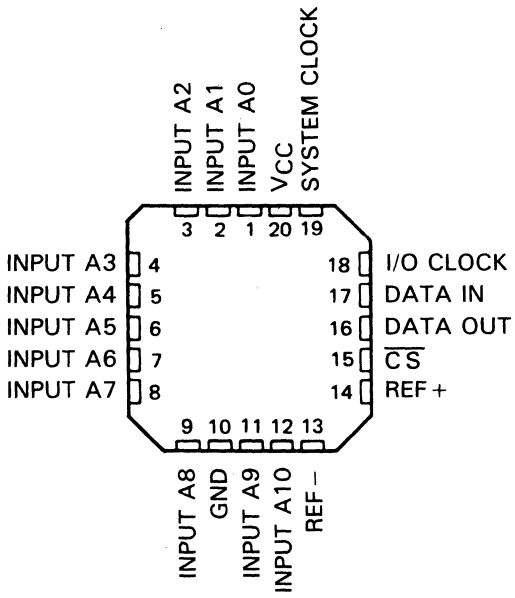
Principles of Operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. With judicious interface timing, a TLC540 conversion can be completed in 9 μs, while complete input-conversion-output cycles are being repeated every 14 μs. With a TLC541, a conversion can be completed in 19 μs, while complete input-conversion-output cycles are repeated every 35 μs. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test", and in any order desired by the controlling processor.

The System and I/O clocks are normally used independently and do not require any special speed or phase



(a) N DUAL-IN-LINE PACKAGE



(b) FN CHIP-CARRIER PACKAGE

Figure 11-76. TLC540 and TLC541 Pinouts (Top View)

relationships between them. This independence simplifies the hardware and software control tasks for the device. Once a clock signal within the specification range is applied to the system clock input, the control hardware and software need only be concerned with addressing the desired analog channel, reading the previous conversion result, and starting the conversion by using the I/O clock. The System clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task. See Figure 11-78 for Operating Sequence Timing.

When chip select ($\overline{CS}$) is high, the Data Out pin is in a three-state condition, and the Address Input and I/O Clock pins are disabled. This feature allows each of these pins, with the exception of $\overline{CS}$, to share a control logic point with their counterpart pins on additional A/D devices when additional TLC540 and TLC541 devices are used. This feature serves to minimize the required control logic pins when using multiple A/D devices.

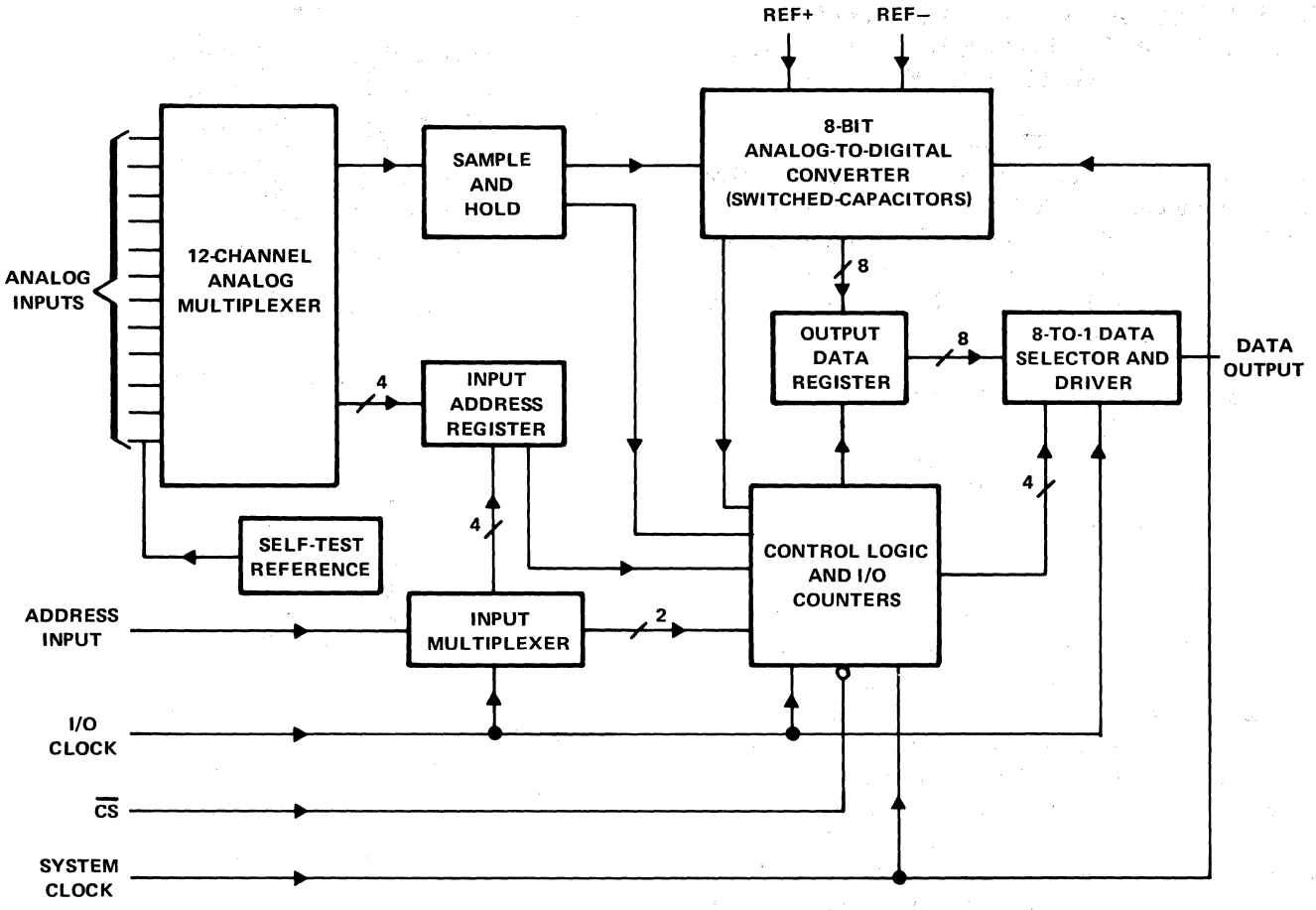
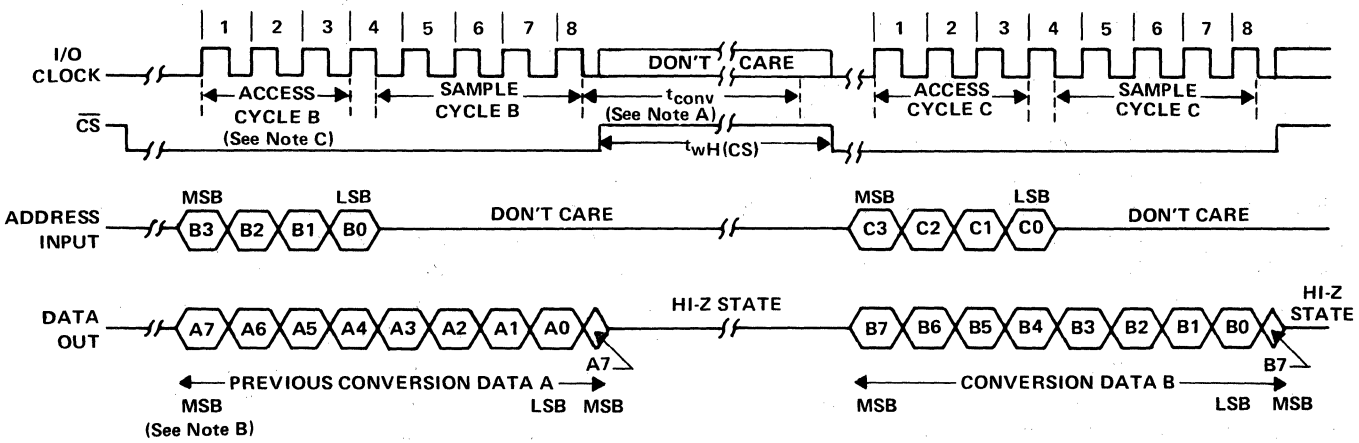


Figure 11-77. Functional Block Diagram



NOTES: A. The conversion cycle, which requires 36 internal system clock periods, is initiated with the 8th I/O clock pulse trailing edge after $\overline{CS}$ goes low for the channel whose address exists in memory at the time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6-A0) will be clocked out on the first seven I/O clock falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three internal system clock cycles (1.4 μs at 2 MHz) after a chip select transition before responding to control input signals. Therefore, no attempt should be fmade to clock-in address data until the minimum chip-select setup time has elapsed.

Figure 11-78. Operating Sequence

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the System clock after a $\overline{CS}$ (high-to-low) transition before the transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the DATA OUT pin.
2. A new positive-logic multiplexer address is shifted in on the first 4 rising edges of the I/O clock. The negative edges of these four I/O clocks shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the newly addressed analog input after the 4th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final (8th) clock cycle is applied to the I/O clock pin. The falling edge of this clock cycle completes the analog sampling process and initiates the hold function. Conversion is then performed during the next 36 System clock cycles.

$\overline{CS}$ can be kept low during periods of multiple conversion. Also, if $\overline{CS}$ is taken high, it must remain high until the end of conversion. Otherwise, a valid falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 System clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

It is possible to connect the System and I/O clocks together in special situations where controlling circuitry must be minimized. In this case, the following special requirements must be taken into consideration in addition to the requirements of the normal control sequence, which was previously described.

1. When $\overline{CS}$ is recognized by the device to be at a low level, the common clock signal is used as an I/O clock. When the $\overline{CS}$ is recognized by the device to be at a high level, the common clock signal is used to drive the "conversion crunching" circuitry.
2. The device will recognize a $\overline{CS}$ transition only when the $\overline{CS}$ input changes and subsequently the System Clock pin receives two positive edges and then a negative edge. For this reason, after a $\overline{CS}$ negative falling edge, the first two clock cycles will not shift in the address because a low $\overline{CS}$ must be recognized before the I/O clock can shift in an analog channel address. Also, upon shifting in the address, $\overline{CS}$ must be raised after the 6th I/O clock, so that a $\overline{CS}$ low level will be recognized upon the lowering of the 8th I/O clock signal. Otherwise, additional common clock cycles will be recognized as I/O clocks and will shift in an erroneous address.

For certain applications, such as strobing, conversion must be started at a specific point in time. These devices will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 4th I/O clock cycle, the hold function is not initiated until the negative edge of the 8th I/O clock cycle. Thus, the control circuitry can leave the I/O clock signal in its high state during the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC540 and TLC541 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software will then immediately lower the I/O clock signal and initiate the hold function to hold the analog signal at the desired point in time and start conversion.

TLC548 TLC549 LinCMOS 8-BIT ANALOG-TO-DIGITAL PERIPHERAL WITH SERIAL CONTROL

The TLC548 and TLC549 are LinCMOS A/D converters using the 8-bit switched-capacitor successive-approximation technology. The typical unadjusted error is ±0.5 LSB maximum. Conversion time is 17 μs and total access plus conversion time is 45,500 conversions per second minimum for the TLC548 and 40,000 conversions per second minimum for the TLC549. The sample-and-hold is on-chip and is software controllable. Power consumption is a low 6 mW typical. Power supply range is from 3 V to 6 V. Figure 11-79 shows the pinout arrangement of the device.

P DUAL-IN-LINE PACKAGE

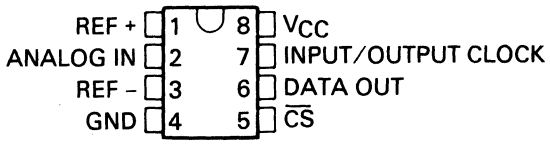


Figure 11-79. TLC548 and TLC549 Pinout (Top View)

Description

The TLC548 and TLC549 are LinCMOS A/D peripheral integrated circuits built around an 8-bit switched-capacitor successive-approximation ADC. See Figure 11-80 for the functional block diagram. They are designed for serial interface with a microprocessor peripheral through a three-state data output and an analog input. The TLC548 and TLC549 use only the Input/Output clock (I/O Clock) input along with the Chip Select ($\overline{CS}$) input for data control. The I/O clock input frequency of the TLC548 is guaranteed up to 2.048 MHz, and the I/O Clock input frequency of the TLC549 is guaranteed to 1.1 MHz.

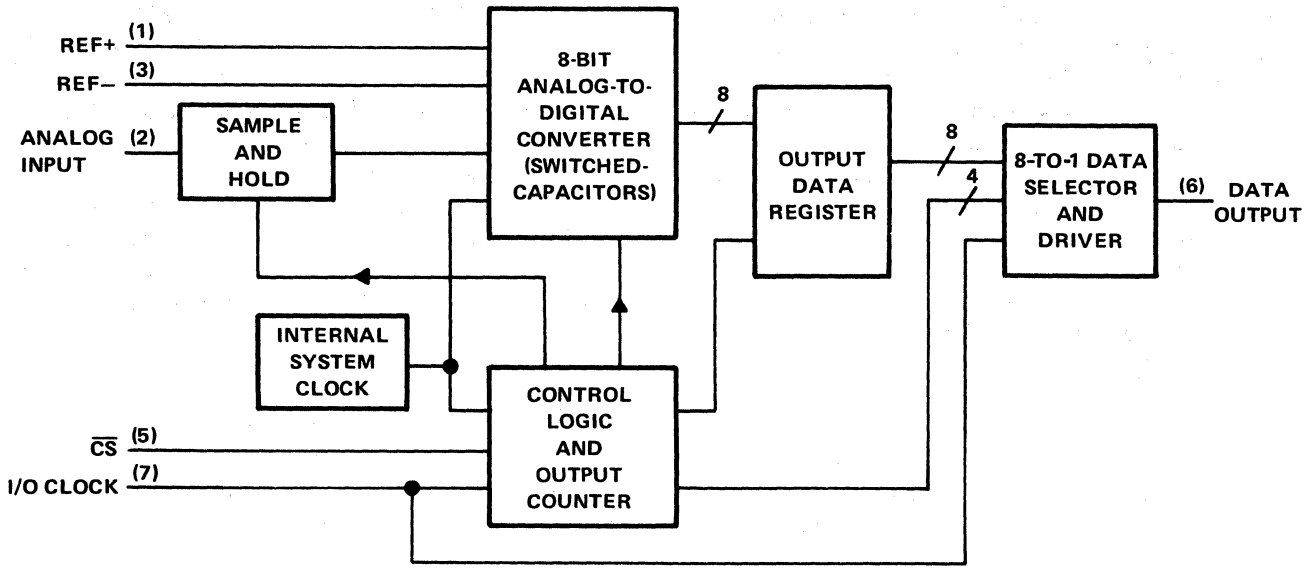


Figure 11-80. Functional Block Diagram

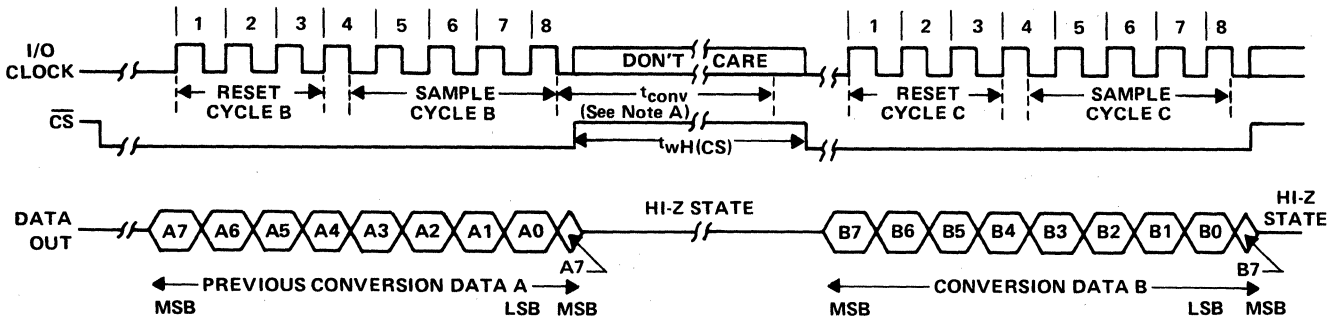
Operation of the TLC548 and TLC549 is very similar to that of the more complex TLC540 and TLC541 devices. However, the on-chip system clock of these devices allows internal device operation to proceed independently of serial input/output data timing and permits manipulation of the TLC548 and TLC549 as desired for a wide range of software and hardware requirements. The I/O Clock, together with the internal system clock, allows high-speed data transfer and minimum sample rates of 45,500 per second for the TLC548, and 40,000 per second for the TLC549.

Additional TLC548/549 features include versatile control logic, an on-chip sample-and-hold circuit that can operate automatically or under microprocessor control, and a high-speed converter with differential high-impedance reference voltage inputs that ease ratiometric conversion, scaling, and circuit isolation from logic and supply noises. Design of the totally switched-capacitor successive-approximation converter circuit allows guaranteed low-error conversion of ± 0.5 least significant bit (LSB) in less than 17 μs.

Principles of Operation

The TLC548 and TLC549 are each a complete data acquisition system on a single chip. Each includes such functions as internal system clock, sample-and-hold, 8-bit A/D converter, data register, and control logic. See Figure 11-81 for operating sequence timing. For flexibility and access speed, there are two control inputs: I/O Clock and Chip Select ($\overline{CS}$). These control inputs and a TTL-compatible three-state output facilitate serial communications with a microprocessor or minicomputer. A conversion can be completed in a maximum of 17 μs, while complete input-conversion-output cycles are repeated at a maximum of every 22 μs for the TLC548 and 25 μs for the TLC549, respectively.

The internal system clock and I/O clocks are used independently and do not require any special speed or phase relationships between them. This independence simplifies the hardware and software control tasks for the device. Due to this independence and the internal generation of the system clock, the control hardware and software need only be



NOTE A: The conversion cycle, which requires 36 system clock periods, is initiated with the 8th I/O clock↓.

Figure 11-81. Operating Sequence

concerned with reading the previous conversion result and starting the conversion by using the I/O clock. The internal system clock will drive the "conversion crunching" circuitry so that the control hardware and software need not be concerned with this task.

When $\overline{CS}$ is high, the Data Out pin is in a high-impedance condition and the I/O clock pin is disabled. This feature allows each of these pins, with the exception of $\overline{CS}$, to share a control logic point with its counterpart pin when additional TLC548 or TLC549 devices are used. This serves to minimize the required control logic pins when using multiple TLC548 and TLC549 devices.

The control sequence has been designed to minimize the time and effort required to initiate conversion and obtain the conversion result. A normal control sequence is:

1. $\overline{CS}$ is brought low. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for two rising edges and then a falling edge of the internal system clock after a $\overline{CS}$ (high-to-low) transition before the transition is recognized. This technique is used to protect the device against noise when the device is used in a noisy environment. The MSB of the previous conversion result will automatically appear on the data out pin.
2. The negative edges of the first four I/O clocks shift out the 2nd, 3rd, 4th, and 5th most significant bits of the previous conversion result. The on-chip sample-and-hold begins sampling the analog input after the 4th falling edge. The sampling operation basically involves the charging of internal capacitors to the level of the analog input voltage.
3. Three more clock cycles are then applied to the I/O pin and the 6th, 7th, and 8th conversion bits are shifted out on the negative edges of these clock cycles.
4. The final (8th) clock cycle is applied to the I/O Clock pin. The on-chip sample-and-hold begins the hold function upon the falling edge of this clock cycle. The hold function will continue for the next four internal system clock cycles. After these four system clock cycles, the hold function ends and conversion is performed during the next 32 system clock cycles, giving a total of 36 cycles. After the 8th I/O clock cycle, $\overline{CS}$ must go high or the I/O clock must remain low for at least 36 system clock cycles to allow for the hold and conversion functions.

$\overline{CS}$ can be kept low during periods of multiple conversion. Also, if $\overline{CS}$ is taken high it must remain high until the end of conversion. Otherwise, a falling edge of $\overline{CS}$ will cause a reset condition, which will abort the conversion in progress.

A new conversion may be started and the ongoing conversion simultaneously aborted by performing steps 1 through 4 before the 36 system clock cycles occur. Such action will yield the conversion result of the previous conversion and not the ongoing conversion.

For certain applications, such as strobing, it is necessary to start conversion at a specific point in time. These devices will accommodate these applications. Although the on-chip sample-and-hold begins sampling upon the negative edge of the 4th I/O clock cycle, the hold function does not begin until the negative edge of the 8th I/O clock cycle, until the moment at which the analog signal must be converted. The TLC548 and TLC549 will continue sampling the analog input until the 8th falling edge of the I/O clock. The control circuitry or software will then immediately lower the I/O clock signal and start the holding function to hold the analog signal at the desired point in time and start conversion.

TL0808, TL0809 LOW-POWER CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

The TL0808 and TL0809 are monolithic CMOS 8-bit A/D converters. They will operate with a 3-V supply making them ideal for battery type applications. Conversion time is 100 μs and they consume typically only 0.3 mW of power. They feature latched three-state outputs and latched address inputs. These A/D devices eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. The pin layout is shown in Figure 11-82. This grouping of input and address lines permits efficient pc board layout.

N DUAL-IN-LINE PACKAGE

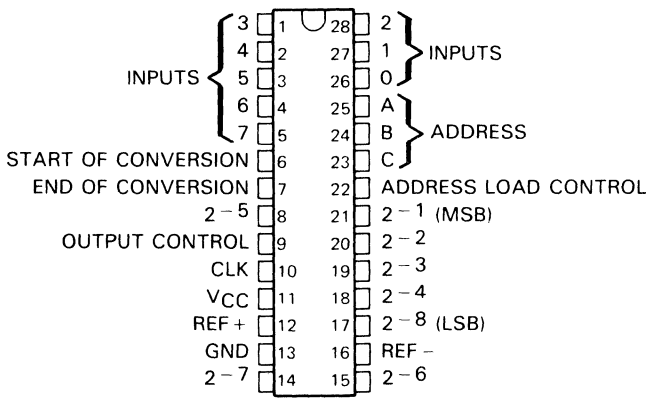


Figure 11-82. TL0808 and TL0809 Pinouts (Top View)

Description

The TL0808 and TL0809 are monolithic CMOS devices with a 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. See Figure 11-83 for the functional block diagram and function table. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a

switched-capacitor array, a sample-and-hold, and a successive approximation register (SAR).

The comparison and conversion methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are three-state output latches from the SAR and latched inputs to the multiplexer address decoder. The single 3-V supply and extremely low power requirements make the TL0808 and TL0809 especially useful for a wide variety of applications including portable battery and LCD applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

Principles of Operation

The TL0808/0809 each consists of an analog signal multiplexer, an 8-bit successive-approximation converter, and related control and output circuitry.

MULTIPLEXER FUNCTION TABLE

INPUTS				SELECTED
ADDRESS			ADDRESS	ANALOG
C	B	A	STROBE	CHANNEL
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

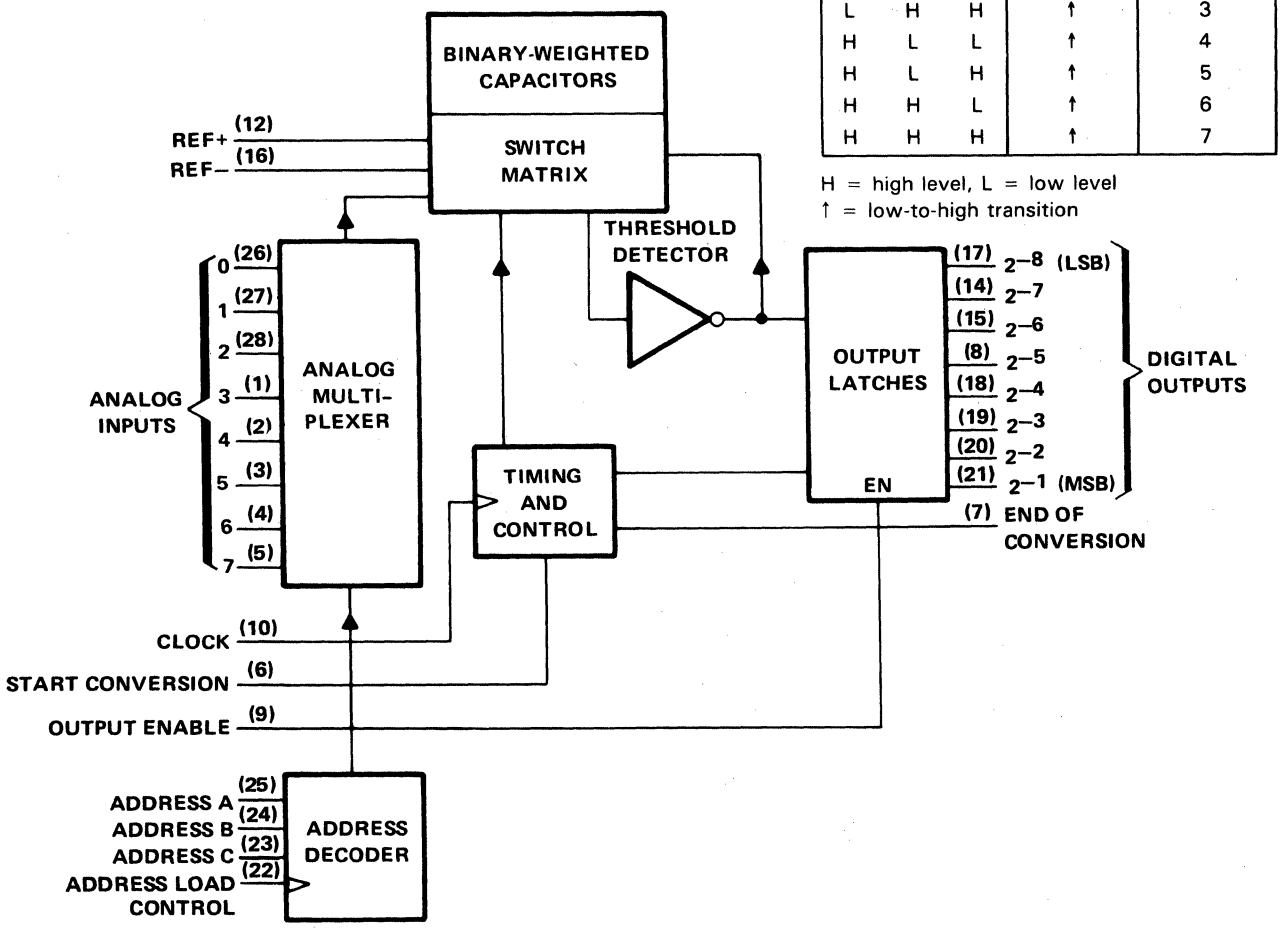


Figure 11-83. Functional Block Diagram (Positive Logic)

Multiplexer

See Figure 11-84 for the operating sequence timing. The analog multiplexer selects 1 of 8 single-ended input channels as determined by the address decoder. The Address Load Control clocks the address code into the decoder on a low-to-high transition. The output latch is reset by the positive-going edge of the start pulse. Sampling also starts with the positive-going edge of the start pulse and lasts for 32 clock periods. The conversion process may be interrupted by a new start pulse before the end of 64 clock periods. The previous data will be lost if a new start-of-conversion occurs before the 64th clock pulse. Continuous conversion may be accomplished by connecting the End-of-Conversion output to the start input. If used in this mode, an external pulse should be applied after power-up to assure start up.

Converter

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors as shown in Figure 11-85. The conversion process uses successive approximation, but it relies on charge redistribution rather than a successive-approximation register (and reference DAC) to count and weight the bits from MSB to LSB.

In the first phase of the conversion process, the analog input is sampled by closing switch SC and all ST switches, and by simultaneously charging all the capacitors to the input voltage. In the next phase of the conversion process, all SC and ST switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all eight bits are identified, and then the charge-convert sequence is repeated.

In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 128). Node 128 is switched to the reference voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF−. If the voltage at the summing node is greater than the trip-point of the threshold detector (approximately one-half the V_{CC} voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to REF−. If the voltage at the summing node is less than the trip point of the threshold detector, this 128-weight capacitor remains connected to REF+ through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so on, until all bits are counted.

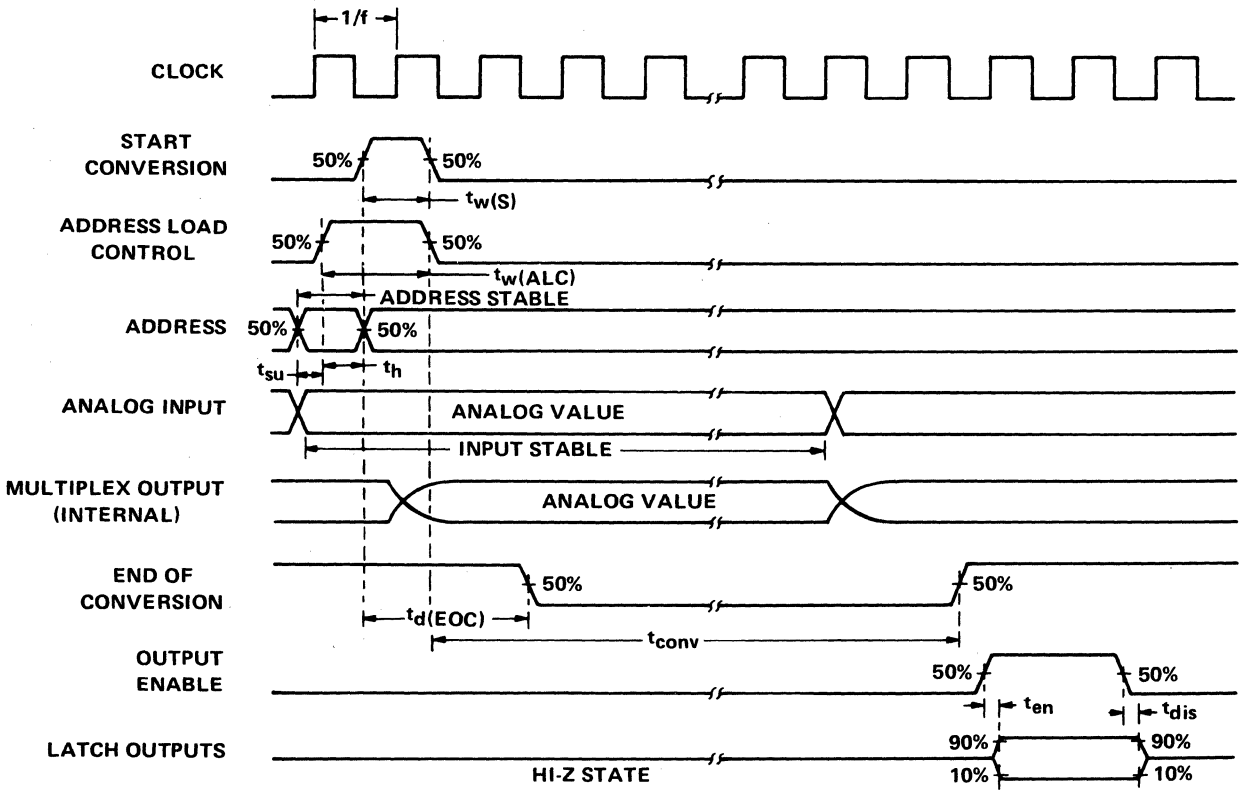


Figure 11-84. Operating Sequence

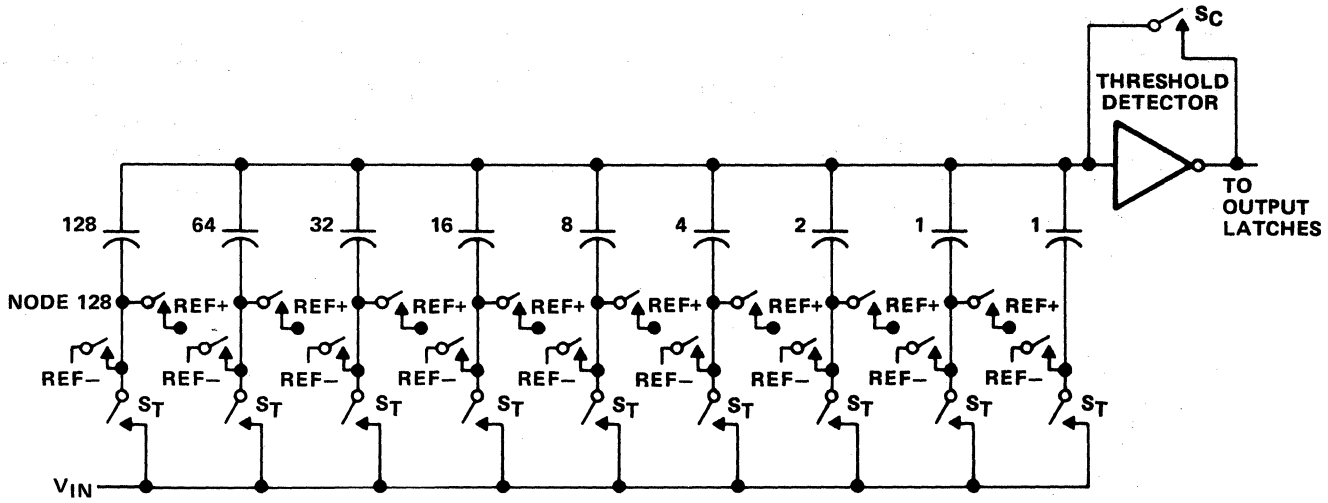


Figure 11-85. Simplified Model of the Successive-Approximation System

A/D CONVERTER APPLICATIONS

A/D converters are used in industrial control systems, automatic testing systems, communications and signal analysis systems, consumer appliance controls, displays, and automotive applications. Digital methods, especially with microprocessors, can provide powerful tools for dealing with analog functions in all of these applications.

An expanding use of A/D conversions is in digital signal processing. Television stations use this highly specialized technique to perform isolation and special effects seen on sports telecasts. However, digital signal processing is not limited to television. The medical community uses it to create and store visual images from computerized CAT scanners and ultrasound analysis equipment. Digital signal processing is also used by the military in radar, sonar, missile tracking, and secure communications. Geologists also use these techniques in analyzing earth science data, and astronomers apply the techniques in using radio telescopes.

Because the majority of applications for A/D converters involve the use of microprocessors, primary emphasis in this section has been directed toward interfaces for A/D converters and a variety of popular microprocessors. Most of the applications present hardware configurations and associated software that can be used with the following microprocessor integrated circuits:

1. Zilog Z80A and Z80
2. Intel 8051 and 8052
3. Intel 8048 and 8049
4. Motorola 6805
5. Motorola 6800, 6802, 6809, and 6809E
6. Rockwell 6502 and 6522 VIA

These microprocessors are representative of devices being used today and their inclusion in this book should not be implied as recommendation, or that other devices should not be considered for specific applications. Likewise, the circuits and software are presented only as working examples of each type of interface.

INTERFACE FOR ADC0803, ADC0804, AND ADC0805 CONVERTERS TO ZILOG Z80A AND Z80 MICROPROCESSORS

This application illustrates the circuit configuration and the associated software that can be used to operate the ADC080X family of A/D converters with the ZILOG Z80A and Z80. The A/D circuits are 8-bit successive-approximation A/D converters that feature microprocessor-compatible control logic and parallel communication with the microprocessor via the data bus. The configuration features are as follows:

1. Minimum circuitry
2. Low cost
3. Very fast communication between the microprocessor and A/D converter
4. Optional microprocessor-interrupt acknowledgement of the end of conversion
5. Differential analog voltage inputs, which reject both common-mode voltages and the offset of the zero-input analog voltage value
6. Optional on-board generation of the A/D clock signal with an external resistor and capacitor.

The basic differences between the A/D converters in this family are given in Table 11-9.

Table 11-9. Differences Between Devices in the ADC080X A/D Converter Family (Note 1)

	0803	0804	0805	UNIT
Total maximum adjusted error (with full-scale adjust)	±1/2	—	—	LSB
Total maximum unadjusted error ($V_{ref}/2$ = 2.5 V)	—	—	—	LSB
Total maximum unadjusted error ($V_{ref}/2$ = open)	—	±1	±1	LSB
Operating free-air temperature range	−40 to 85	0 to 70	−40 to 85	°C

NOTE 1: Conversion accuracies listed are with V_{CC} at 5 V and the clock frequency at 640 kHz. If a faster clock is used, conversion time will decrease proportionately and the accuracy will tend to decrease slightly.

Circuitry

Figure 11-86 shows the interconnection between the microprocessor and the A/D converter. The A/D converter write $\overline{WR}$ and read $\overline{RD}$ signals, which are generated by the microprocessor, are not masked by an addressing scheme. However, if additional I/O devices were placed on the data bus, masking could be easily designed.

The SN74393 dual binary counter generates a 500 kHz clock signal for the A/D converter. Any binary counter may be used instead of the SN74393. In addition, any clock signal within the clock frequency specification may be used. Another way to generate the clock signal is to use an external resistor and capacitor in conjunction with the CLK IN and CLK OUT pins of the A/D converter. The configuration and frequency equation for this method are shown in Figure 11-87.

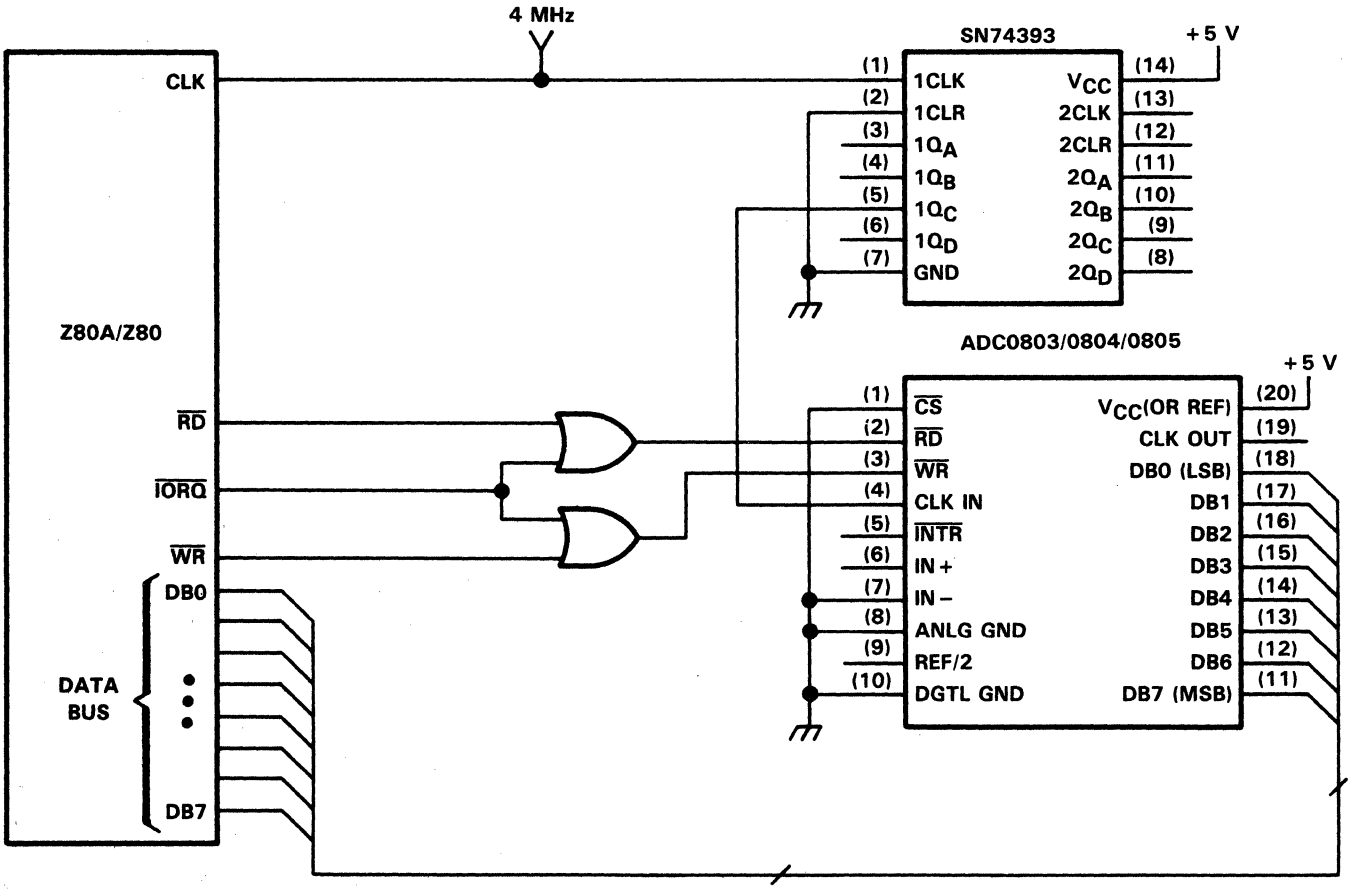


Figure 11-86. Circuit Diagram for Z80A/Z80 to ADC0804/0805 Interface

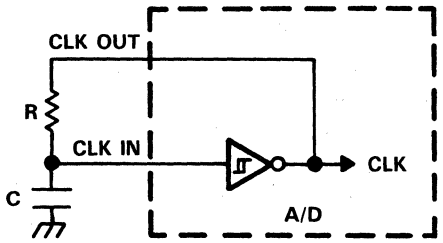


Figure 11-87. Configuration and Equations for On-Board Clock Generator

Timing Diagram

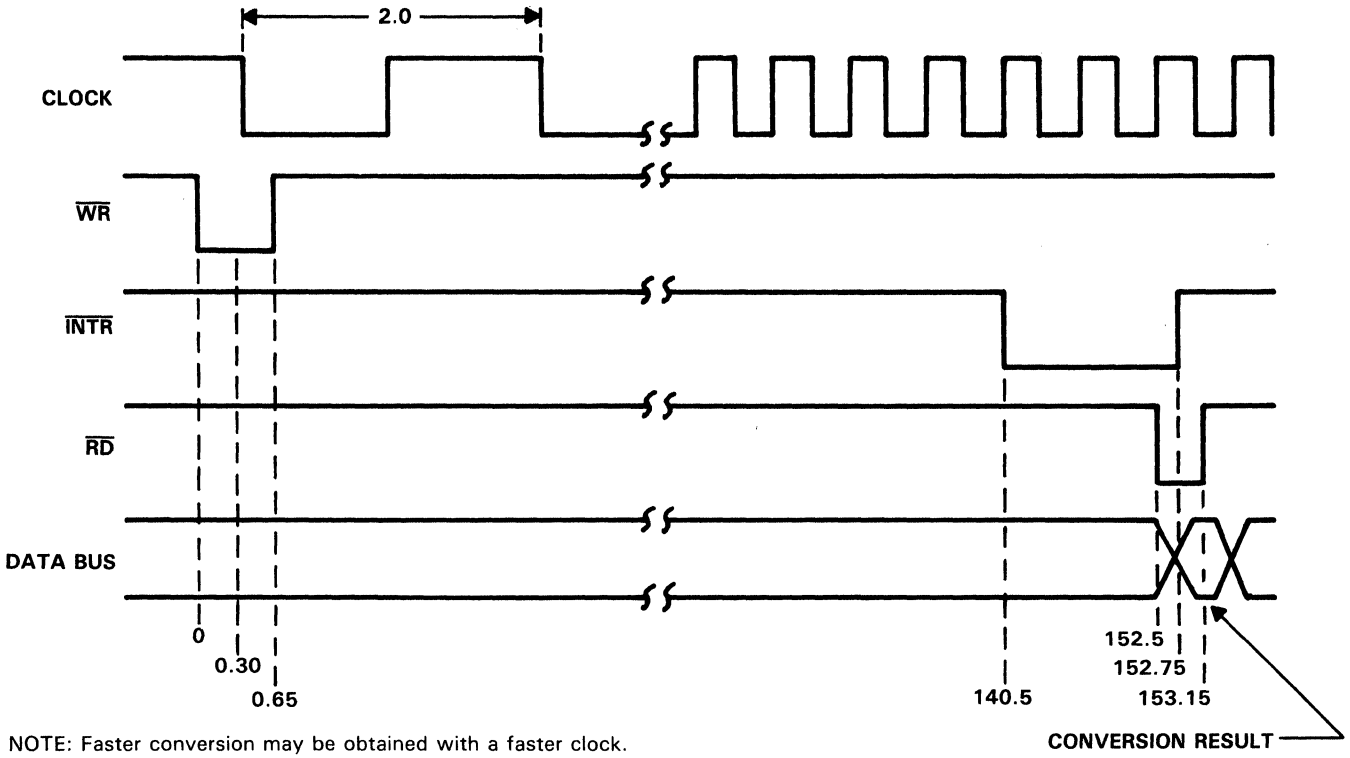
Figure 11-88 shows the timing diagram for the interface. With a 500 kHz clock, the conversion time is 140.5 μs and the A/D $\overline{\text{INTR}}$ pin is reset when the $\overline{\text{RD}}$ signal goes low.

Software

The following software listing presents the software for this interface. The software is minimal due to the microprocessor-compatibility of the A/D converter. In allowing time for conversion, the designer can use any delay that is convenient, including a timer function. Another method is to use the $\overline{\text{INTR}}$ signal on the A/D converter to start a microprocessor interrupt routine that reads the conversion result. If an on-board clock generator like the one shown in Figure 11-87 is used, the conversion time will vary with the tolerances of the resistor and capacitor. In this situation, the designer can allow a conservative delay to assure that the conversion is complete before reading the result. Another method might be to wait for an acknowledgement of the $\overline{\text{INTR}}$ signal and use this to inform the microprocessor of a completed conversion.

```
                        ;               Software for Z80/Z80A, ADC0803,
                        ;               ADC0804, ADC0805, Interface
                        ;
                        ;
FF 00                   WRITE:  EQU FFH         ;Interface write address
FF 00                   READ:   EQU FFH         ;Interface read address
                                                ;The above addresses could be
                                                ;anything unless they are used
                                                ;to drive an address decode
                                                ;circuit, which addresses
                                                ;the A/D IC
                        ;
0000    D3 FF           START:  OUT (WRITE),A   ;Start conversion of analog
                                                ;channel; the contents of the
                                                ;accumulator are not important;
                                                ;the write pulse however, is.

                        ;
                        ;Before reading the conversion result, a slightly
                        ;greater than 140 microsecond delay (with a 500 kHz
                        ;A/D clock), to allow for conversion time, can be
                        ;selected in any way which is convenient for the designer.
                        ;                       OR
                        ;The microprocessor can continue to perform main
                        ;program software and the conversion result can be
                        ;retrieved by an interrupt routine, which is initiated
                        ;by the INTR(bar) signal, which signifies the end of
                        ;conversion, on pin 5.
                        ;
0002    DB FF                   IN A, (READ)    ;Read conversion result
                                                ;into the A register
0004                            END
```



NOTE: Faster conversion may be obtained with a faster clock.

Figure 11-88. Timing Diagram for Z80A/Z80 to ADC0803/0804/0805 Interface

INTERFACE FOR ADC0803, ADC0804, AND ADC0805 CONVERTERS TO THE ROCKWELL 6502 MICROPROCESSOR

This application shows the circuit configuration and the associated software that can be used to operate this family of A/D converters with the Rockwell 6502 microprocessor. The interface circuit diagram is shown in Figure 11-89.

A data conversion cycle begins by performing a write to the ADC080X with a Start (STA) accumulator instruction. The conversion requires between 66 and 73 clock cycles. The ADC080X provides an interrupt request signal when the conversion is complete. The circuit timing is shown in Figure 11-90.

An alternate method for retrieving the conversion result would be to use a wait state in a software delay loop until the conversion results are read into the 6502 with an LDA instruction. A software listing for a typical interrupt service routine is shown. Note that the circuit employs a minimum of address decoding hardware; some applications may require additional decoding hardware.

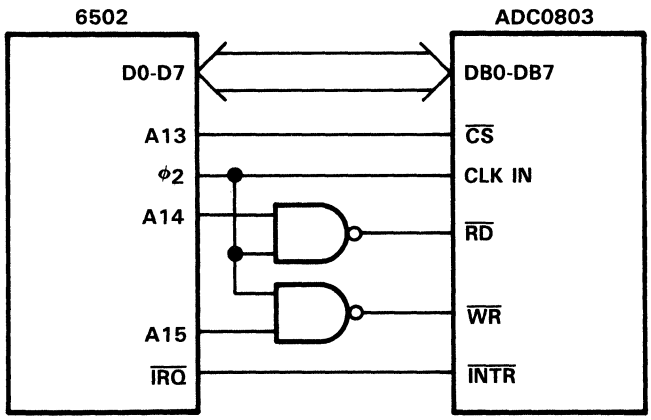


Figure 11-89. 6502 to ADC0803/0804/0805 Interface Circuit Diagram

```
;               Register Assignments for ADC0803, ADC0804,
;               and ADC0805 to 6502 Interface
;
WRITE:      .EQU 8800H
READ:       .EQU 4800H
;
;
MAIN:           .
                .
                .

                STA WRITE       ;Start conversion

                .
                .
                .

ISR:        PHA             ;Save contents of accumulator
            LDA READ        ;Read conversion results
            STA DATA        ;Store results in memory
            PLA             ;Restore accumulator
            RTI             ;Return to main program
```

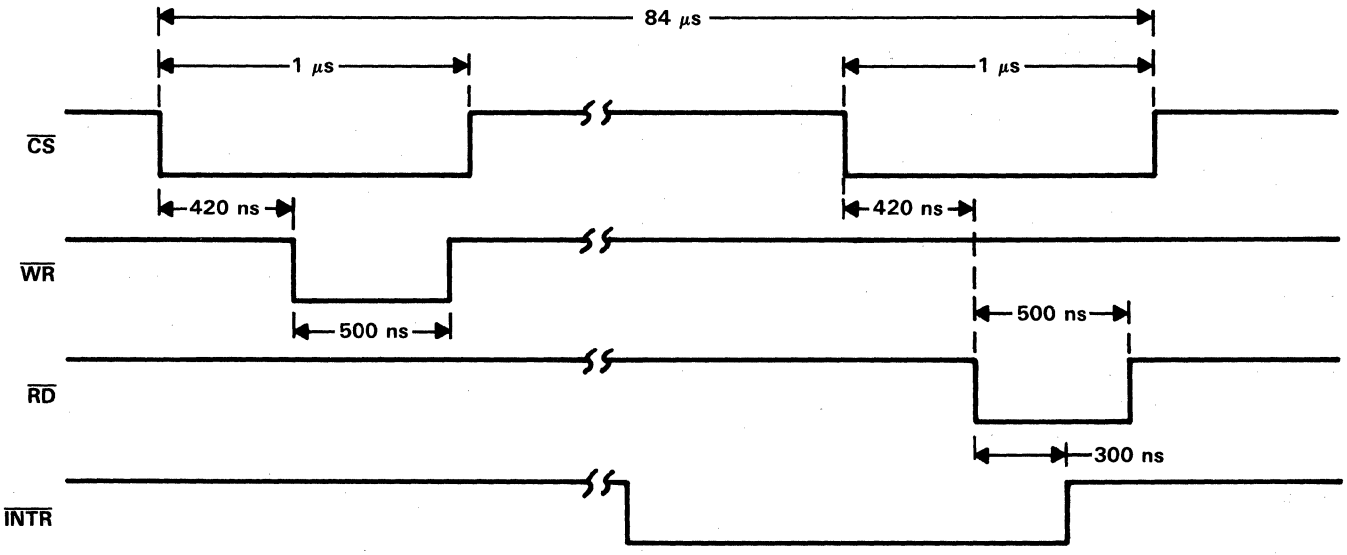


Figure 11-90. 6502 to ADC0803/0804/0805 Interface Timing Diagram

INTERFACE FOR ADC0808, ADC0809, TL0808, TL0809, TL520,TL521 AND TL522 CONVERTERS TO ZILOG Z80A AND Z80 MICROPROCESSORS

This application presents the circuit configuration and the associated software that can be used to operate this family of A/D converters with the ZILOG Z80A and Z80. These A/D circuits are 8-bit successive-approximation A/D converters that feature microprocessor-compatible control logic and parallel communication with the microprocessor via the data bus. This configuration features:

1. Minimum circuitry
2. Low cost
3. Very fast communication between the microprocessor and A/D converter
4. Optional microprocessor-interrupt acknowledgement of the end of conversion
5. Convenient control of the analog multiplexer.

Some of the basic differences between the A/D converters in these families are listed in Table 11-10. However, these are not the only differences. The TL0808 and TL0809 and ADC0808 and ADC0809 have the same pinout, but the TL520, TL521, and TL522 pinout is different from the 0808 and 0809.

Table 11-10. Differences Between ADC/TL0808-ADC/TL0809 and TL520-TL522 A/D Converter Families (Note 1)

	V_{CC} SUPPLY (volts)	CONVERSION (μs)
TL0808/TL0809	2.75 V to 5.5 V	100 μs
ADC0808/ADC0809	4.5 V to 6 V	100 μs
TL520	3 V to 5.5 V	70 μs
TL521	3 V to 5.5 V	100 μs
TL522	2.75 V to 5.5 V	200 μs

NOTE 1: The conversion times require a 640 kHz clock. If faster conversion is desired, a faster clock is required. Both conversion time and conversion accuracy are specified in the data sheets when using a 640 kHz clock. If a faster clock is used, conversion time will decrease proportionately and the accuracy may stay within the 640 kHz specification or decrease slightly.

Figure 11-91 shows the interconnection points between the microprocessor and the A/D converter for a typical interface application.

Figure 11-92 shows the interconnection between the microprocessor and the TL0808 and TL0809 and ADC0808 and ADC0809 A/D converters. The interface will also work with the TL520, TL521, and TL522 if the different pinout is considered. The SN74393 dual binary counter is used to generate a 500 kHz clock for the A/D converter. Any binary counter may be used instead of the SN74393 or any clock signal within the A/D converter clock frequency specification may be used. The microprocessor-generated A/D control and address signals are not masked by an addressing scheme; however, if additional I/O devices are placed on the data bus, masking would be necessary.

Timing Diagram

Figure 11-93 is the timing diagram for the interface. With a 500 kHz A/D clock, the conversion time for the TL0808, TL0809, ADC0808, or ADC0809 devices is 130 μs with the EOC signal going low about 6 μs after activation of the output enable signal.

Software

The associated program listing presents the software routines for this interface. The coding is minimal due to the microprocessor-compatibility of the A/D converters. This code is written so that it may be easily incorporated into a subroutine if desired. In allowing time for conversion, the designer may use any delay which is convenient, including a timer function, or the End of Conversion (EOC) signal on the A/D converter to initiate a microprocessor interrupt routine that reads the conversion result.

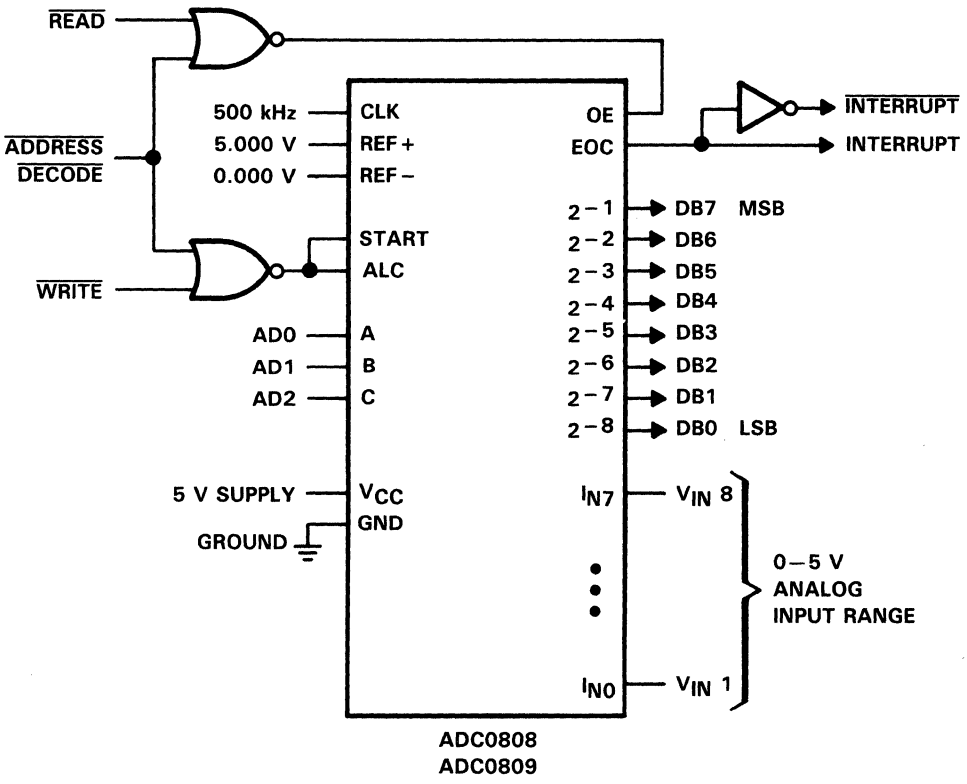


Figure 11-91. Typical Interface Application

```
                        ;Interface Software for Z80A/Z80-TL0808 / TL0809 ICs
                        ;                                -ADC0808 / ADC0809 ICs
                        ;                                -TL520 / TL521 / TL522 ICs
                        ;
                        ;
        FF 00           READ:       EQU FFH             ;Interface read address; this
                                                        ;address could be anything
                                                        ;unless it is used to drive
                                                        ;an address decode circuit,
                                                        ;which addresses the A/D IC
                        ;
0000    0E 00           START:      LD C,00H            ;Prepare to address analog
                                                        ;channel 0; 01 would address
                                                        ;channel 1, etc.
                        ;
0002    ED 49           LOD0808:    OUT (C),C           ;Start conversion of analog
                                                        ;channel per C register
                        ;
                        ;Before reading the conversion result, a slightly
                        ;greater than / microsecond delay (with a 500 kHz
                        ;A/D clock), to allow for conversion time, can be
                        ;selected in any way which is convenient for the
                        ;designer.
                        ;                       OR
                        ;The microprocessor can continue to perform main
                        ;program software and the conversion result can be
                        ;retrieved by an interrupt routine, which is initiated
                        ;by the End of Conversion (EOC) signal on pin 7 of the
                        ;ADC0808/0809 and TL0808/0809 ICs and on pin 22 of the
                        ;TL520/521/522 ICs.
                        ;
0004    DB FF                       IN A, (READ)        ;Read conversion result
                                                        ;into the A register
0006                                END
```

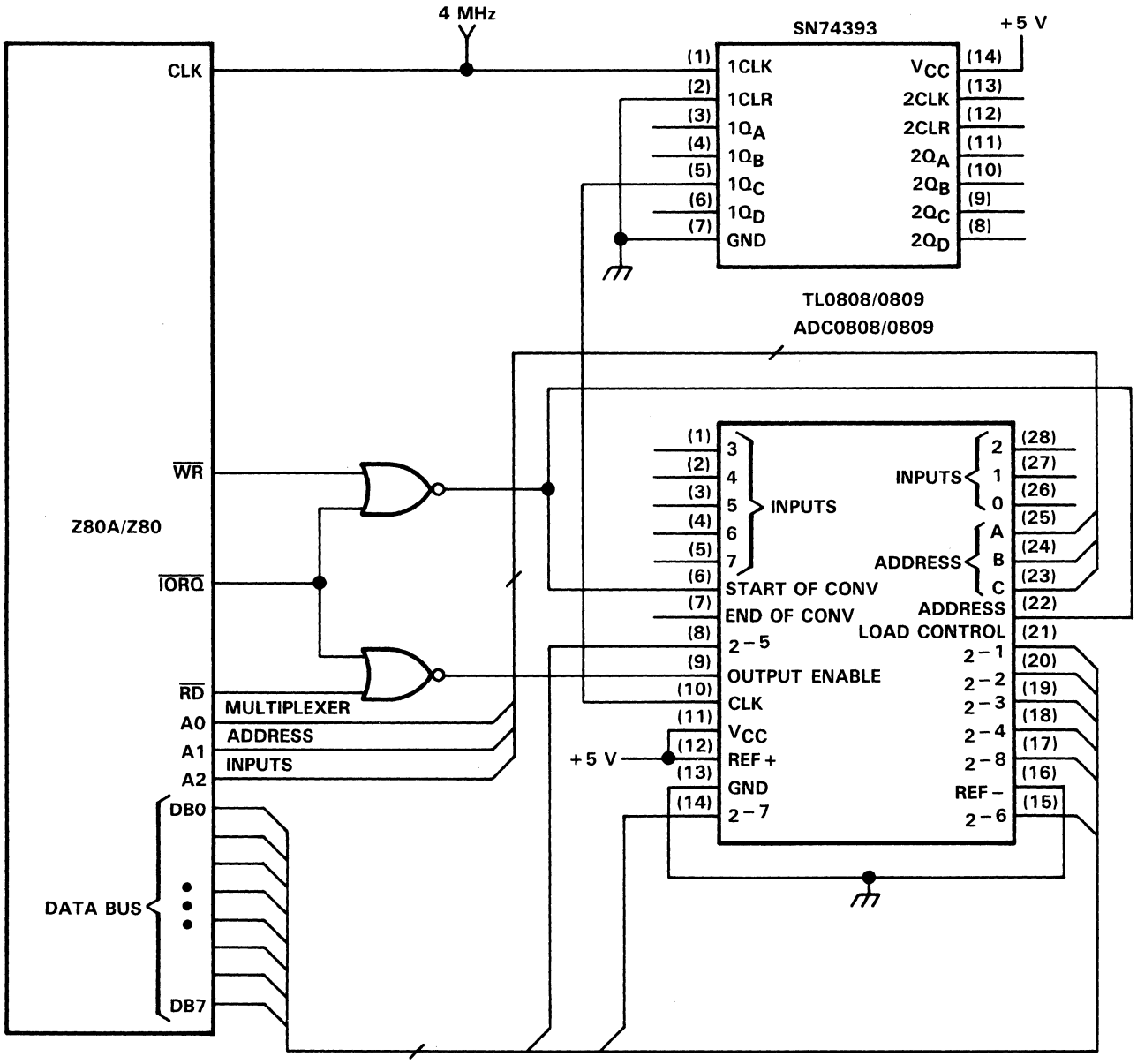
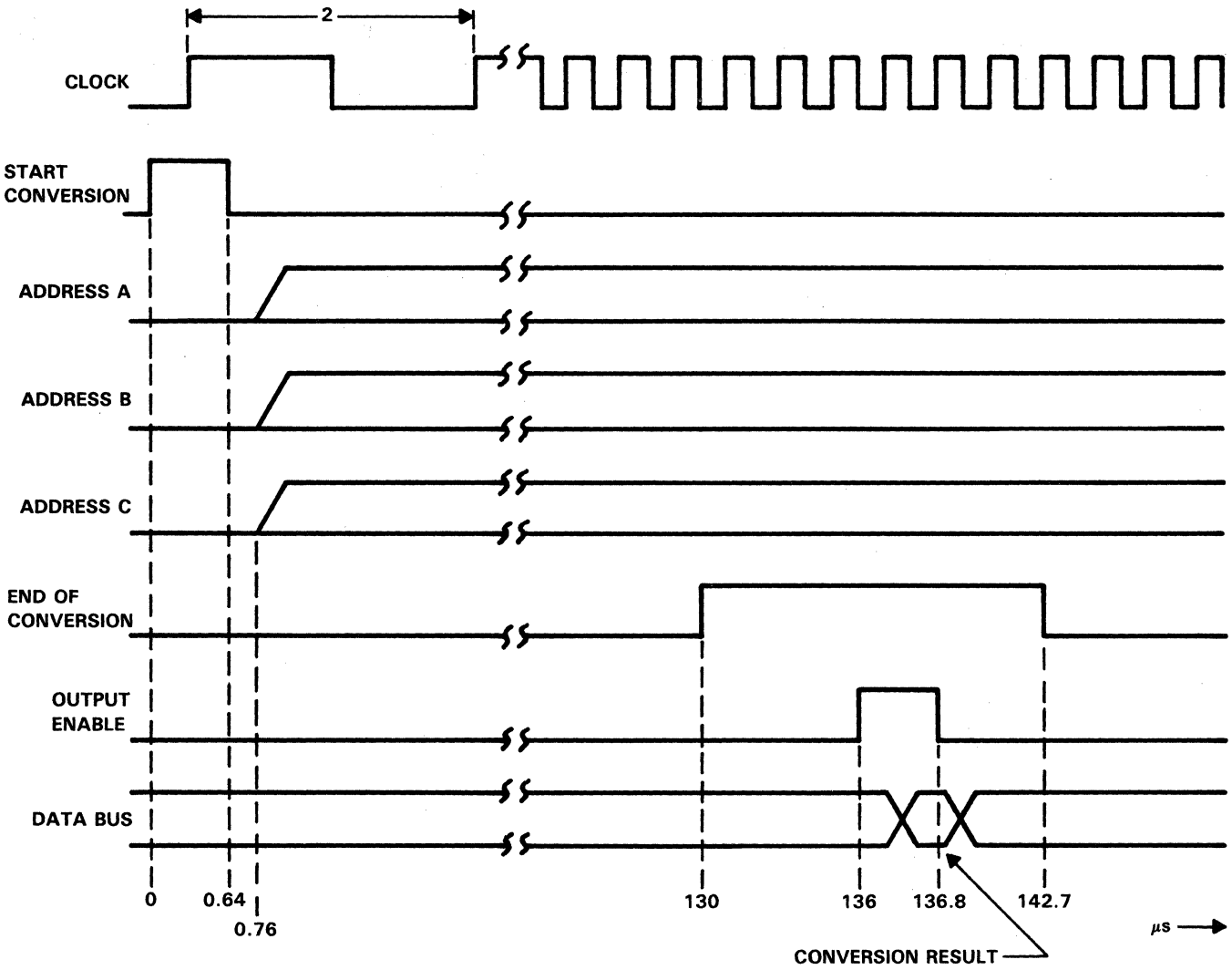


Figure 11-92. Circuit Diagram for Z80A/Z80 to TL0808/0809 ADC0808/0809 Interface



NOTE: Faster conversion may be obtained with a faster clock.

Figure 11-93. Timing Diagram for Z80/Z80A to TL0808/0809 ADC0808/0809 Interface

INTERFACE FOR ADC0808 AND ADC0809 CONVERTERS TO THE ROCKWELL 6502 MICROPROCESSOR

This application shows the circuit configuration and the associated software that can be used to operate the ADC0808 and ADC0809 A/D converters with the Rockwell 6502 microprocessor. The interface circuit diagram is shown in Figure 11-94. A data conversion cycle is initiated by performing an STA instruction. This generates a start conversion pulse that clears the EOC line. The address in memory where the accumulator stores its contents determines which channel is selected for conversion. The conversion requires approximately 65 clock cycles. The clock frequency may vary from 10 kHz to 1.28 MHz, however, when it is above 640 kHz the accuracy may decrease slightly. The circuit timing diagram is shown in Figure 11-95.

Upon completion of the conversion, the EOC signal is set and may be used to generate an interrupt signal for the Rockwell 6502. Also, a software delay loop may be used to achieve the proper delay until conversion is complete.

If the interrupt scheme is chosen, the interrupt service routine must either start another conversion cycle that will clear the EOC signal or disable the interrupts. If this is not done, the Rockwell 6502 will remain in the interrupt service routine loop. It may be desirable to add a flip-flop and an AND gate to control the enabling and disabling of the EOC signal. Structuring of the interrupt and the address decoding scheme are both flexible and should be optimized for the particular application. A software listing for an interrupt service routine follows.

```
;               Register Assignments for ADC0808 and ADC0809
;               Interface to the Rockwell 6502
ADC0808         .EQU 4000H
WRITE0          .EQU 8000H
WRITE1          .EQU 8001H
  .               .    .
  .               .    .
  .               .    .
WRITE7          .EQU 8007H
;
;
MAIN:             .
                  .
                  .
                STA WRITE0          ;Start conversion, clear interrupt
                  .
                  .
                  .


ISR:            PHA                 ;Save accumulator
                LDA ADC0808         ;Read conversion results into acc.
                STA DATA            ;Store conversion results
                PLA                 ;Restore accumulator
                PLP                 ;Pull status from stack
                SEI                 ;Disable interrupts
                PHP                 ;Push status back on stack
                RTI                 ;Return to main program
```

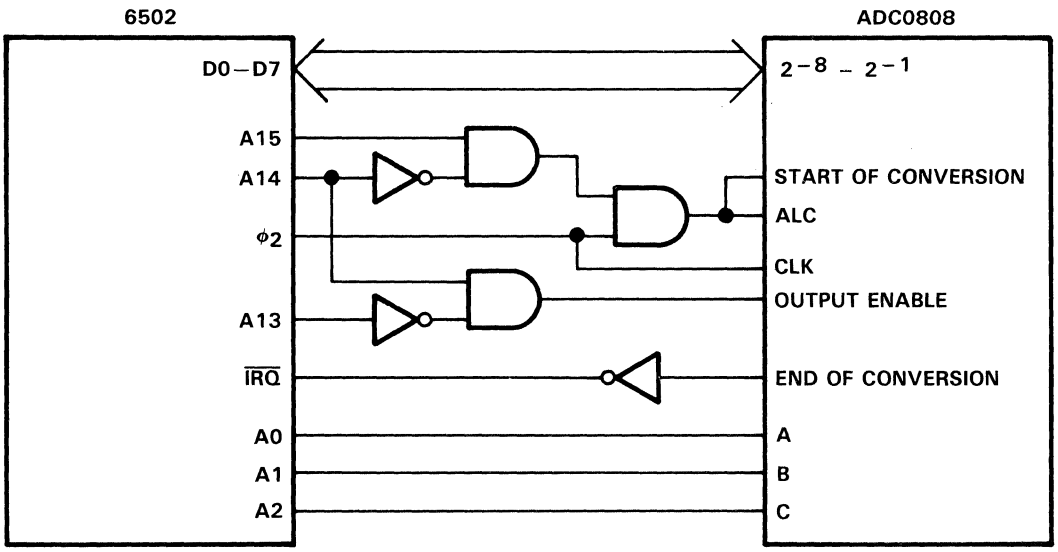


Figure 11-94. 6502 to ADC0808 Interface Circuit Diagram

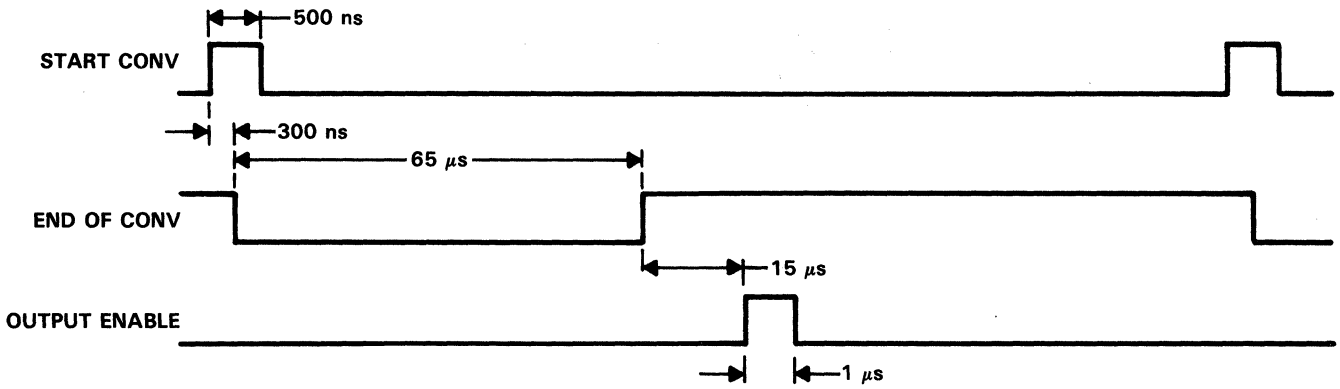


Figure 11-95. 6502 to ADC0808 Interface Timing Diagram

INTERFACE FOR ADC0808, ADC0809, TL0808, TL0809, TL520, TL521, AND TL522 CONVERTERS TO THE MOTOROLA 6800 MICROPROCESSORS

This application illustrates a circuit configuration and the software that can be used to operate this family of A/D converters with the Motorola 6800 family of microprocessors. Figure 11-91 shows a typical interface application. Figure 11-96 shows the interconnection between the Motorola 6802 microprocessor and the TL0808 or TL0809 A/D converters. Although Figure 11-96 shows circuitry for the TL0808/ADC0808 and TL0809/ADC0809 A/D converters, the interface will also work with the TL520, TL521, and TL522 devices if the different pinout is considered.

The SN74393 dual binary counter is used to generate a 500 kHz clock for the A/D converter. Any binary counter may be used in place of the SN74393 or any clock signal within the A/D converter clock frequency specification can be used. The 6800 E clock or E clock equivalent, if within the clock frequency specification, may also be connected directly to the clock input of the A/D converter. When using the Motorola microprocessors with clock frequencies greater than 1 MHz, the designer must check to see that the A/D converter write and read timing specifications are met. The microprocessor-generated A/D control and address signals are masked by the 4000H-7FFFH addressing range. A more efficient addressing scheme can easily be implemented if desired. Table 11-11 provides information for adapting the circuit of Figure 11-96 for use with other members of the 6800 family of microprocessors.

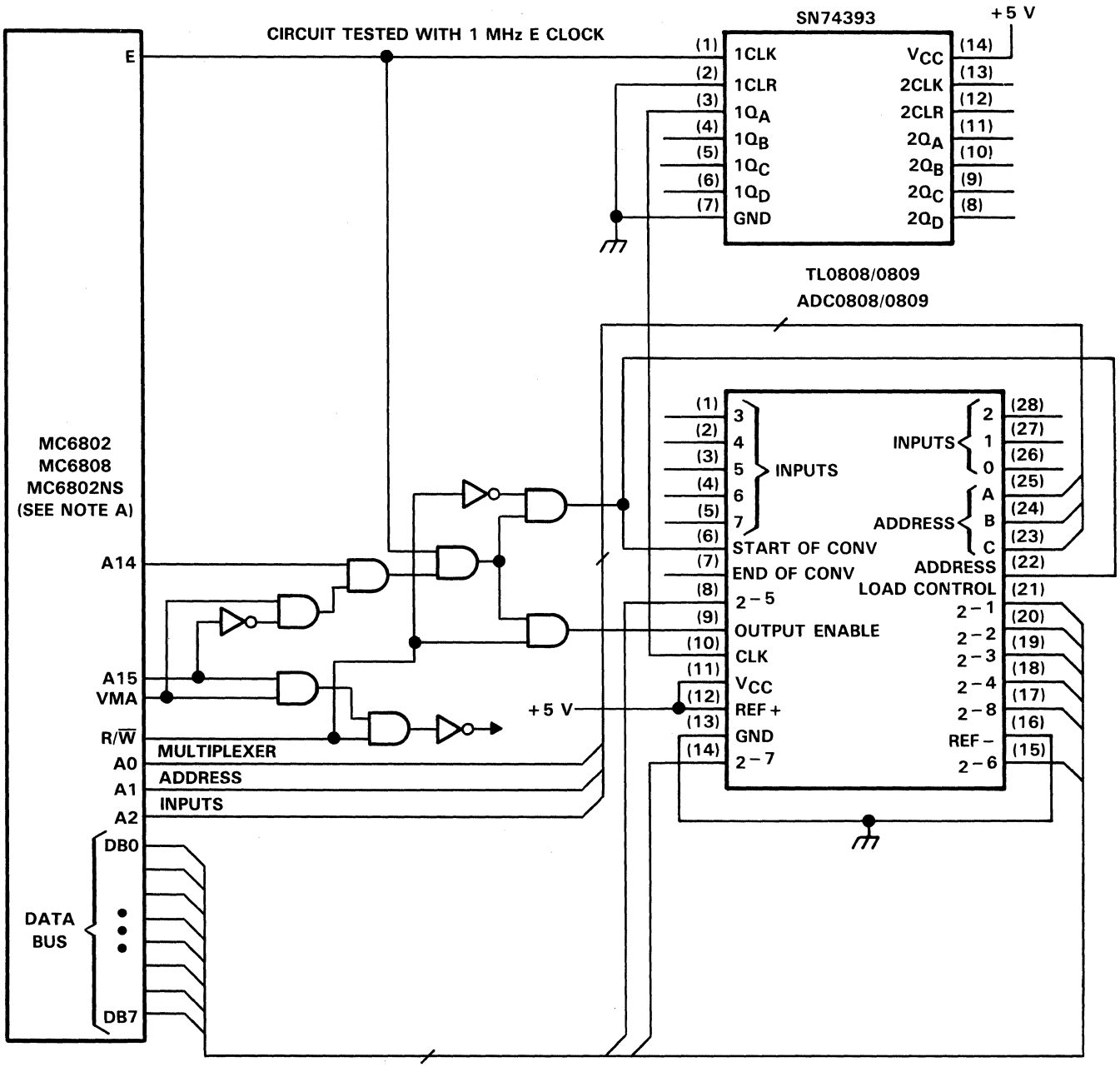
Timing Diagram

Figure 11-97 is the timing diagram for this interface. With a 500 kHz A/D clock, the conversion time for the TL0808/TL0809 and ADC0808/ADC0809 A/D converters is 130 μs. The EOC signal falls approximately 6 μs after activation of the OUTPUT ENABLE signal.

Software

The software listing for this interface follows. The software is minimal due to the microprocessor-compatibility of the A/D converter devices. In allowing time for conversion, the designer can use any delay which is convenient, including either a timer function or the EOC signal to initiate the microprocessor interrupt routine that reads the conversion result.

```
                        ;          Software for Motorola 680X-TL0808 / TL0809 ICs
                        ;                                -ADC0808 / ADC0809 ICs
                        ;                                -TL520 / TL521 / TL522 ICs
                        ;
                        ;
        40 00           READ:      EQU 4000H          ;Interface read address; this
                                                      ;address is selected to ensure
                                                      ;that the read operation reads
                                                      ;the conversion result byte
                                                      ;and does not read the program
                                                      ;memory or on-board RAM (if
                                                      ;the microprocessor is the
                                                      ;6802) by mistake
                        ;
0000    B7 40 00        START:     STAA 4000H         ;Address analog channel 0 and
                                                      ;start conversion; 4001 would
                                                      ;address channel 1, etc.
                        ;
                        ;Before reading the conversion result, a slightly
                        ;greater than 130 microsecond delay (with a 500 kHz
                        ;A/D clock), to allow for conversion time, can be
                        ;selected in any way which is convenient for the
                        ;designer.
                        ;                    OR
                        ;The microprocessor can continue to perform main
                        ;program software and the conversion result can be
                        ;retrieved by an interrupt routine, which is initiated
                        ;by the End of Conversion (EOC) signal on pin 7 of the
                        ;ADC0808/0809 and TL0808/0809 ICs and on pin 22 of the
                        ;TL520/521/522 ICs.
                        ;
0003    B6 40 00                   LDAA READ          ;Read conversion result
                                                      ;into the A accumulator
0006                               END
```



NOTE A: Refer to Table 11-11 for information about other Motorola microprocessors.

Figure 11-96. Circuit Diagram for TL0808/0809 Interface

Table 11-11. Considerations for Using Other Microprocessors

MICROPROCESSOR	E CLOCK OR E CLOCK EQUIVALENT
6800	ϕ_2 is equivalent to the 6802/6809 E pin
6802/6808/6802ns	See Figure 11-96
6809	See Figure 11-96
6809E/68HC09E	See Figure 11-96 and "Motorola 8-bit Microprocessor and Peripheral Data Book" for clock generator — pg. 3-277

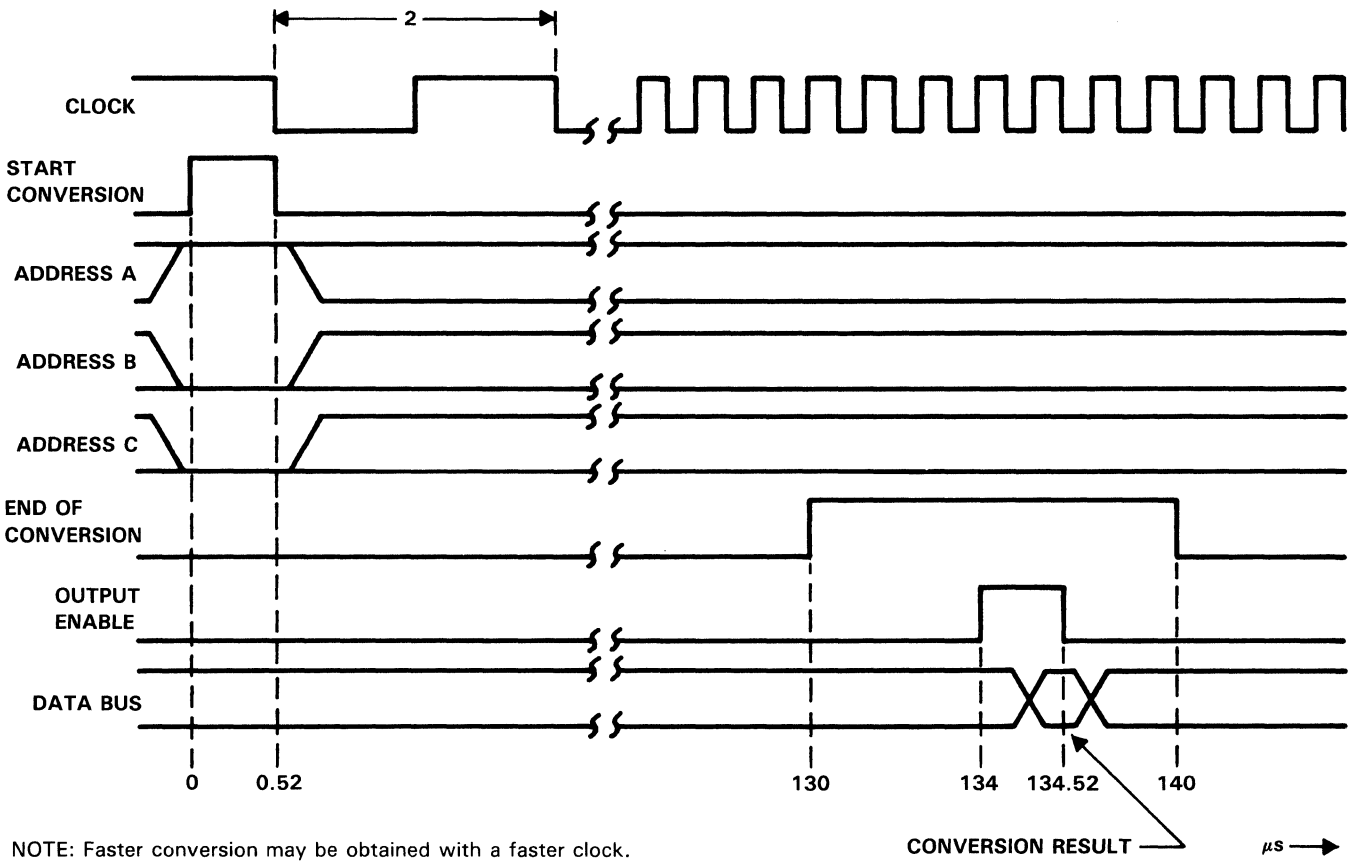


Figure 11-97. Timing Diagram for 680X to TL0808/00809 ADC0808/0809 Interface

INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO ZILOG Z80A AND Z80 MICROPROCESSORS

The ADC0831, ADC0832, ADC0834, and ADC0838 devices are 8-bit successive-approximation analog-to-digital converters with serial input/output and configurable input multiplexers with up to 8 channels. These A/D converters are designed to easily communicate with microprocessors in a serial fashion. The hardware configurations and the associated software presented can be used to operate the ZILOG Z80A and Z80 microprocessors with the ADC0830 converters. The timing diagrams show the interaction between the microprocessor and the A/D converter.

The ADC0832, ADC0834, and ADC0838 A/D converters can be software configured in either the single-ended or differential input mode. Additionally, the differential ± inputs can be interchanged through software manipulation.

The serial interface features:

1. Low cost
2. Minimum circuitry
3. Fast conversion and communication between the A/D converter and the microprocessor
4. Remote control advantages of serial A/D converters.

Circuitry — ADC0832, ADC0834, and ADC0838

Figure 11-98 shows the interconnection between the microprocessor and the ADC0832, ADC0834, and ADC0838 A/D converters. The interconnection is identical for all three A/D converters. The microprocessor DO pin can be used to transmit to and receive digital data between the ADC083X DI and DO pins, respectively. The SN74126 3-state buffer output is in the high-impedance state except during a microprocessor read operation. The SN74174 quad D-type flip-flop is used to synchronize and slow down the write/read communication between the microprocessor and ADC083X so the ADC083X timing specifications are satisfied. Rather than NOR gates, OR gates may be used to activate the flip-flops and 3-state buffer on the positive transitions of the write WR and read RD strobes, instead of on the negative transitions. However, if OR gates are used, a SN74125 buffer must be used in place of the SN74126.

Timing Diagram — ADC0838 Device

Figure 11-99 is the timing diagram for the Z80A and Z80 to ADC0838 interface. Addressing the analog channel, performing conversion, and retrieving the conversion result requires 260 μs. The timing diagrams for the ADC0832 and ADC0834 converters are similar except fewer input bits are transmitted to the A/D converter. The 3-state buffer enable

strobes occur 2.5 μs after the negative transition of the clock CLK signal so the conversion result bits have sufficient time to set up on the DO line before being read by the microprocessor.

Software — ADC0832, ADC0834, and ADC0838 Devices

The following software listing presents the interface software for these A/D converters. The software is written so it can be readily applied to any of the three A/D converters. Also, the software can be easily incorporated into a subroutine so the designer can access the software quickly.

The software differences for these A/D converters are as follows:

	ADC0832	ADC0834	ADC0838
Send Select Bit 1	No	Yes	Yes
Send Select Bit 0	No	No	Yes

The above differences are accommodated by initializing the C and B registers correctly before accessing the software. The software listing shows the interface software routines and Tables 11-12 through 11-17 list the mux addressing to accommodate the differences.

```
                        ; Software for Z80/Z80A to ADC0838, ADC0834, ADC0832 Interface
                        ;
                        ;
        FF 00           WRITE:    EQU FFH          ;Interface write address
        FF 00           READ:     EQU FFH          ;Interface read address
                        ;
0000    06 05           START:    LD B,05H         ;ADC0838; Input bit counter = 5
                                                   ;ADC0834; Input bit counter = 4
                                                   ;ADC0832; Input bit counter = 3
0002    0E 15                     LD C,15H         ;Load input address in C.
                                                   ;C0 is sent first
                        ;
0004    3E 04           ADC83X    LD A,04H         ;CS(bar)(A2) = 1,CLK(A1) = 0,
                                                   ;D1/D0(A0) = 0
0006    D3 FF                     OUT (WRITE),A    ;Write these values to A/D
0008    3E 00                     LD A,00H         ;Lower CS(bar)
000A    D3 F                      OUT (WRITE),A
000C    CB 1F           ADC83X1:  RR A             ;Prepare to load next input bit in A
000E    CB 19                     RR C             ;Put next input bit in carry
0010    CB 17                     RL A             ;Load next input bit in A0 and realign
                                                   ;A1 & A2 so they are correct
0012    D3 FF                     OUT (WRITE),A    ;Set up next bit on D1 line
0014    F6 02                     OR 02H           ;Raise CLK line and clock in,
0016    D3 FF                     OUT (WRITE),A    ;next bit
0018    E6 FD                     AND FDH          ;Lower CLK line
001A    D3 FF                     OUT (WRITE),A
001C    10 EE                     DJNZ ADC83X1     ;If B>0; branch
001E    06 08                     LD B,08H         ;Conversion bit counter = 8
0020    3E 02           ADC83X0:  LD A,02H         ;Raise CLK & keep CS(bar) = 0
0022    D3 FF                     OUT (WRITE),A
0024    3E 00                     LD A,00H         ;Lower CLK line and clock out,
0026    D3 FF                     OUT (WRITE),A    ;next conversion bit
0028    DB FF                     IN A,(READ)      ;Put next conversion bit in A0
002A    CB 1F                     RR A             ;Put conversion bit in carry
002C    CB 11                     RL C             ;Put conversion bit in C0 and
                                                   ;shift other conversion bits in C
002E    10 F0                     DJNZ ADC83X0     ;If B>0; branch
0030    F6 04                     OR 04H           ;Raise CS(bar)
0032    D3 FF                     OUT (WRITE),A
0034                              END              ;Conversion result in register C
```

ADC0832 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 1)

Table 11-12. Single-Ended MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO REGISTER C
	SGL/$\overline{DIF}$	ODD/SIGN	0	1	
1	1	0	+		#03H
1	1	1		+	#0BH

Table 11-13. Differential MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO REGISTER C
	SGL/$\overline{DIF}$	ODD/SIGN	0	1	
1	0	0	+	−	#01H
1	0	1	−	+	#09H

NOTE 1: Internally, Select 0 is low. Select 1 is high, COMMON is internally connected to ANLG GND.

ADC0834 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 2)

Table 11-14. Single-Ended MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO REGISTER C
	SGL/$\overline{BIT}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	1	0	0	+				#03H
1	1	0	1			+		#0BH
1	1	1	0		+			#07H
1	1	1	1				+	#0FH

Table 11-15. Differential MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO REGISTER C
	SGL/$\overline{BIT}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	0	0	0	+	−			#01H
1	0	0	1			+	−	#09H
1	0	1	0	−	+			#05H
1	0	1	1			−	+	#0DH

NOTE 2: Internally, Select 0 is high, COMMON is internally connected to ANLG GND.

ADC0838 MUX ADDRESSING (5-BIT SHIFT REGISTER)

Table 11-16. Single-Ended MUX Mode

START BIT	MUX ADDRESS				ANALOG SINGLE-ENDED CHANNEL NO.									PUT DATA INTO REGISTER C
	SGL/$\overline{DIF}$	ODD/SIGN	SELECT		0	1	2	3	4	5	6	7	COM	
			1	0										
1	1	0	0	0	+								−	#03H
1	1	0	0	1			+						−	#13H
1	1	0	1	0					+				−	#0BH
1	1	0	1	1							+		−	#1BH
1	1	1	0	0		+							−	#07H
1	1	1	0	1				+					−	#17H
1	1	1	1	0						+			−	#0FH
1	1	1	1	1								+	−	#1FH

Table 11-17. Differential MUX Mode

START BIT	MUX ADDRESS			ANALOG DIFFERENTIAL CHANNEL-PAIR NO.								PUT DATA INTO REGISTER C
	SGL/$\overline{DIF}$	ODD/SIGN	SELECT	0		1		2		3		
			1 0	0	1	2	3	4	5	6	7	
1	0	0	0 0	+	−							#011H
1	0	0	0 1			+	−					#11H
1	0	0	1 0					+	−			#09H
1	0	0	1 1							+	−	#19H
1	0	1	0 0	−	+							#05H
1	0	1	0 1			−	+					#15H
1	0	1	1 0					−	+			#0DH
1	0	1	1 1							−	+	#13H

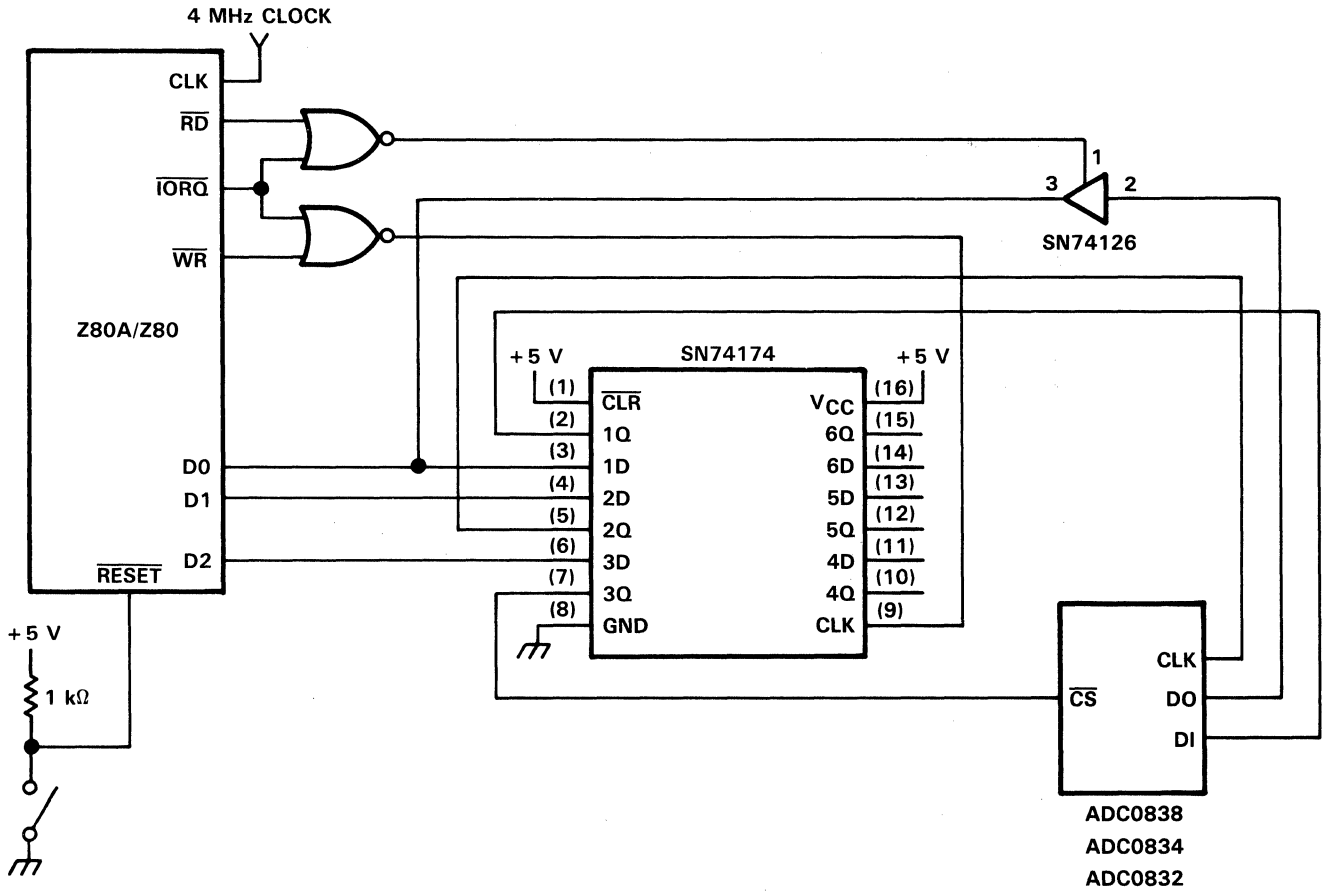


Figure 11-98. Z80A/Z80 to ADC0838, ADC0834, ADC0832 Interface Circuit Diagram

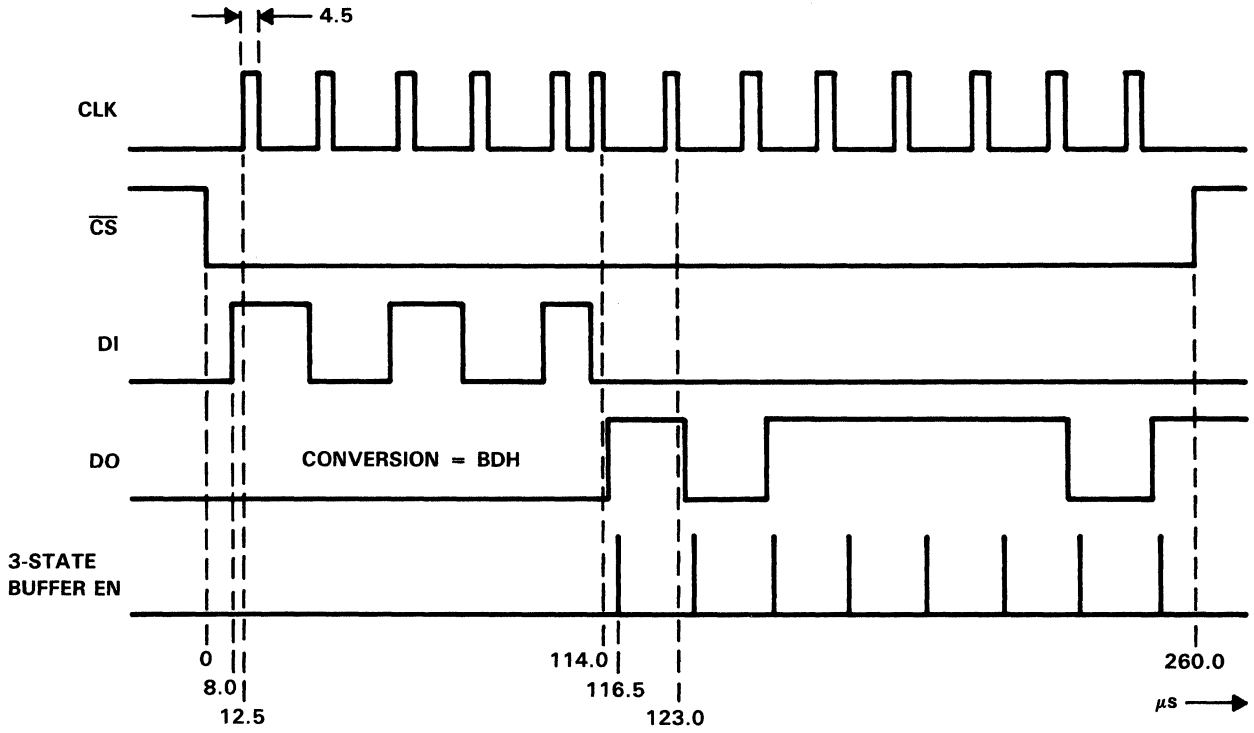


Figure 11-99. Timing Diagram for Z80A/Z80 to ADC0838 Interface (Microprocessor Clock = 4 MHz)

Circuitry — ADC0831 Device

Figure 11-100 shows the interconnection between the microprocessor and the ADC0831 converter. The circuitry is basically the same as for the ADC0832, ADC0834, and ADC0838 devices except that the ADC0831 device does not have a DI line.

Timing Diagram — ADC0831 Device

Figure 11-101 is the timing diagram for the Z80A and Z80-ADC0831 interface. Performing conversion and retrieving the conversion result requires 181 μs. The 3-state buffer enable strobes occur 2.5 μs after the negative transition of the clock CLK signal so the conversion result bits have sufficient time to set up on the DO line before these bits are read by the microprocessor.

Software — ADC0831 Device

The software listing for the ADC0831 follows. The software can be easily incorporated into a subroutine so the designer can access the software quickly. An initial A/D clock cycle must occur before the eight subsequent clock cycles extract the conversion result bits from the A/D converter.

```
                        ; Software for Z80/Z80A to ADC0831 Interface
                        ;
                        ;
          FF 00         WRITE:    EQU FFH          ;Interface write address
          FF 00         READ:     EQU FFH          ;Interface read address
                        ;
0000      3E 04         START:    LD A,04H         ;CS(bar)(A2) = 1,CLK(A1) = 40,
0002      D3 FF                   OUT (WRITE),A    ;Write these values to A/D
0004      3E 00                   LD A,00H         ;Lower CS(bar)
0006      D3 FF                   OUT (WRITE),A
0008      3E 02                   LD A,02H         ;Raise CLK initially
000A      D3 FF                   OUT (WRITE),A
000C      3E 00                   LD A,00H         ;Lower CLK initially
000E      D3 FF                   OUT (WRITE),A
0010      06 08                   LD B,08H         ;Conversion bit counter = 8
0012      3E 02         ADC8310:  LD A,00H         ;Raise CLK & keep CS(bar) = 0
0014      D3 FF                   OUT (WRITE),A
0016      3E 00                   LD A,00H         ;Lower CLK line and clock out,
0018      D3 FF                   OUT (WRITE),A    ;next conversion bit
001A      DB FF                   IN A,(READ)      ;Put next conversion bit in A0
001C      CB 1F                   RR A             ;Put conversion bit in carry
001E      CB 11                   RL C             ;Put conversion bit in C0 and
                                                   ;shift other conversion bits in C
0020      10 F0                   DJNZ ADC8310     ;If B>0; branch
0022      3E 04                   LD A,04H         ;Raise CS(bar)
0024      D3 FF                   OUT (WRITE),A
0026                              END              ;Conversion result in register C
```

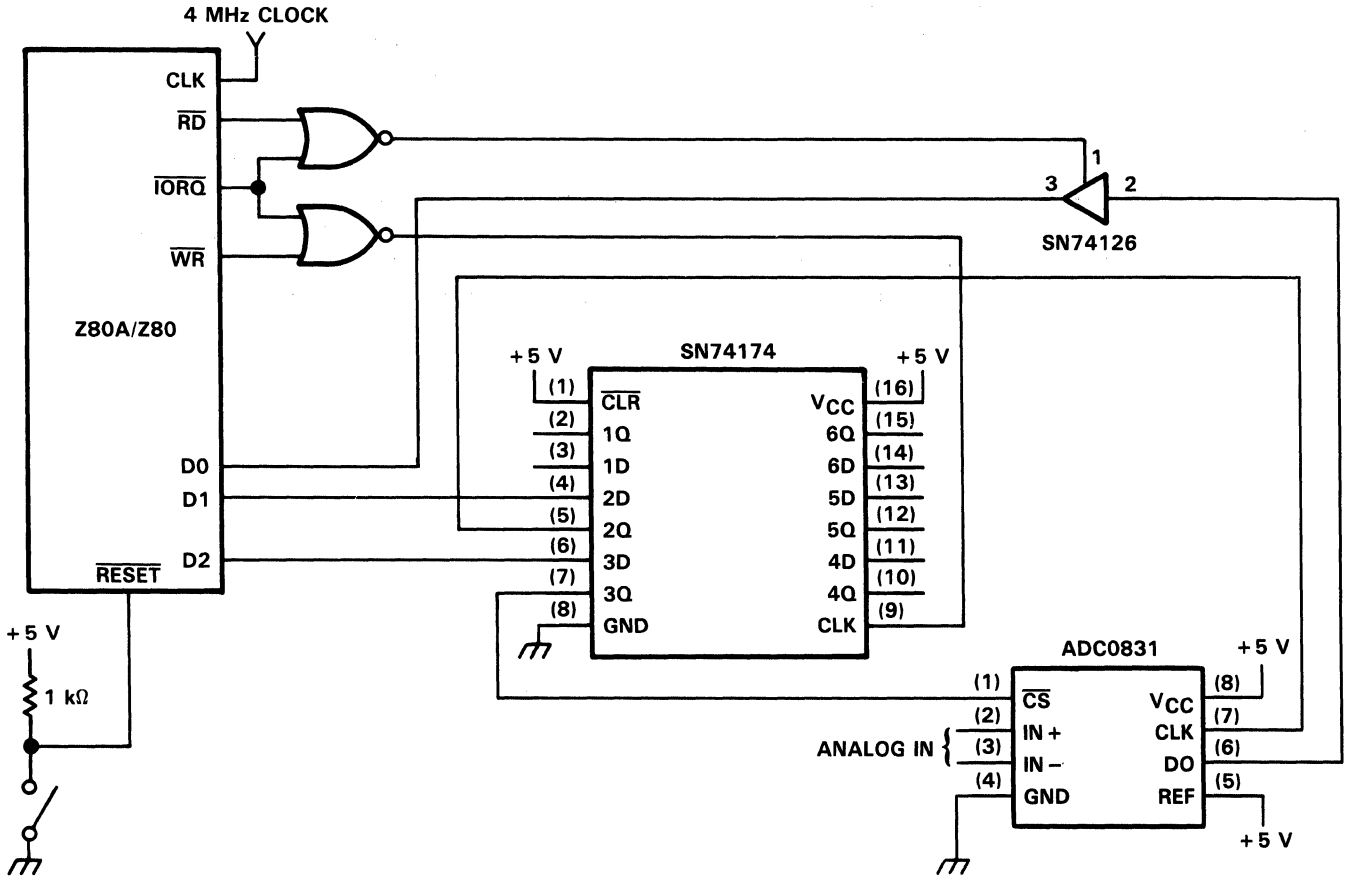


Figure 11-100. Z80A/Z80 to ADC0831 Interface Circuit Diagram

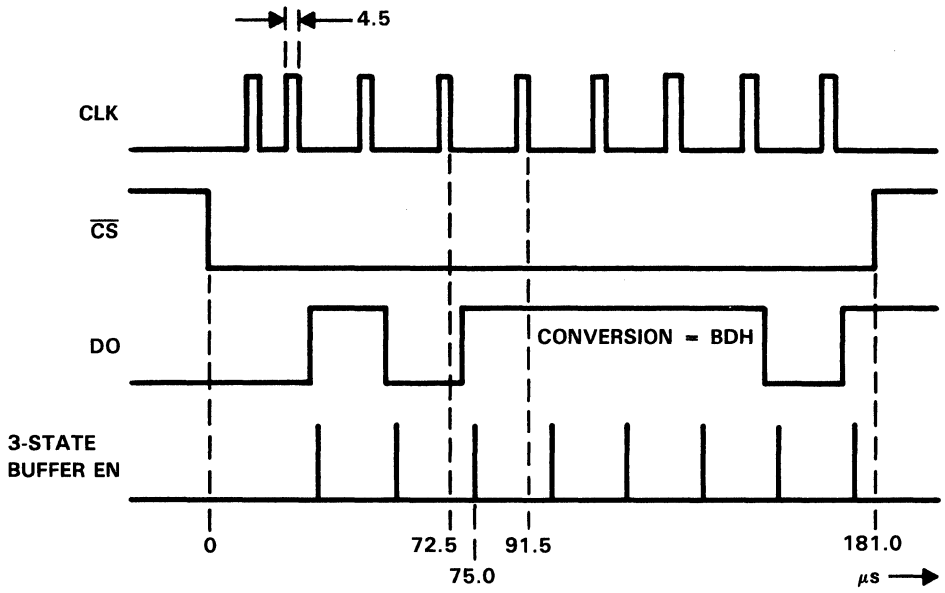


Figure 11-101. Timing Diagram for Z80A/Z80 to ADC0831 Interface (Microprocessor Clock = 4 MHz)

INTERFACE FOR ADC0831, ADC0832, AND ADC0838 CONVERTERS TO THE ROCKWELL 6502 MICROPROCESSOR

The ADC083X family of successive-approximation A/D converters features 8-bit resolution, microprocessor-compatible control logic, serial data communication, and 1, 2, 4, or 8 analog inputs, which may be operated in the single-ended, differential, or pseudo-differential mode.

A circuit for an ADC0831 device interface to a 6502 microprocessor is shown in Figure 11-102. The timing diagram for this circuit is shown in Figure 11-103 and the interface software is shown as a listing. The interface circuit operates under complete control of the software. The system clock Phi 2 is used as the clocking signal to latch data from the address bus into the D-type flip-flops. By writing to the correct address locations, the CS and CLK signals are generated. The address decoding scheme is quite simple; therefore, a few additional gates may be required to provide proper address decoding in more complex applications. Since the ADC0831 device has only a single analog input, no multiplexer address is required which simplifies the timing.

A similar circuit for a 6502 to ADC0838 interface is presented in Figure 11-104. The timing diagram is shown in Figure 11-105 and the interface software listing follows. The operation of this circuit is basically the same as the above circuits with the addition of the DI input for the analog multiplexer address. Operation of the ADC0838 is the same as the ADC0831 converter with the exception of the multiplexer address which can be changed in software. With the software listings presented, one data acquisition cycle can be accomplished in 221 μs using the ADC0831 circuit and in 345 μs using the ADC0838 circuit.

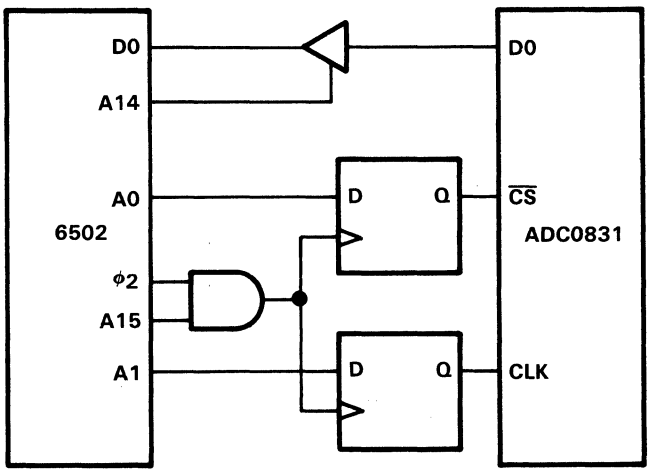


Figure 11-102. 6502 to ADC0831 Interface Circuit Diagram

```
; Software Listing for ADC0831, ADC0832, and ADC0838 to 6502 Interface
;                Register Assignments
;
ADC0831        .EQU 4000H
;
;
START:         STA $8000          ; Bring /CS low
               LDY #$08           ; Initialize bit counter
               STA $8002          ; Bring CLK high
               STA $8000          ; Bring CLK low
               STA $8002          ; Bring CLK high
               STA $8000          ; Bring CLK low
LOOP:          STA $8002          ; Bring CLK high
               LDA ADC0831        ; Read bit into accumulator
               ROR A              ; Rotate new bit into carry
               TXA                ; Transfer result into accumulator
               ROL A              ; Rotate new bit into result
               TAX                ; Put result back into X register
               STA $8000          ; Bring CLK low
               DEY                ; Decrement bit counter
               BNE LOOP           ; Go back and get another bit
               STA $8001          ; Bring /CS high

;              Register Assignments
;
MUXADDRESS     .EQU 0000H
ADC0838        .EQU 4000H
;
;
START:         LDA #$C0           ;
               STA MUXADDRESS     ; Initialize muxaddress
               STA $8000          ; Bring /CS low
               LDY #$05           ; Initialize counter
LOOP1:         ROL MUXADDRESS     ; Rotate address bit into carry
               BCS SET            ; Is address bit set?
               STA $8000          ; Set up a low to be clocked in
               STA $8004          ; Bring CLK high write high to D1
               STA $8000          ; Bring CLK low
               JMP CONTINUE       ; Skip to continue
SET:           STA $8001          ; Set up a high to be clocked in
               STA $8005          ; Bring CLK high, write high to D1
               STA $8001          ; Bring CLK low
CONTINUE:      DEY                ; Decrement Counter
               BNE LOOP1          ; Go back to clock out next bit
               STA $8004          ; Bring CLK high
               STA $8000          ; Bring CLK low
               LDY #$08           ; Initialize counter
LOOP2:         STA $8004          ; Bring CLK high
               LDA ADC0838        ; Read bit in from ADC0838
               ROR A              ; Rotate new bit into carry
               TXA                ; Transfer result into accumulator
               ROL A              ; Rotate new bit into result
               TAX                ; Replace result back in X register
               STA $8000          ; Bring CLK low
               DEY                ; Decrement counter
               BNE LOOP2          ; Go back to clock next result bit
               STA $8002          ; Bring /CS high
```

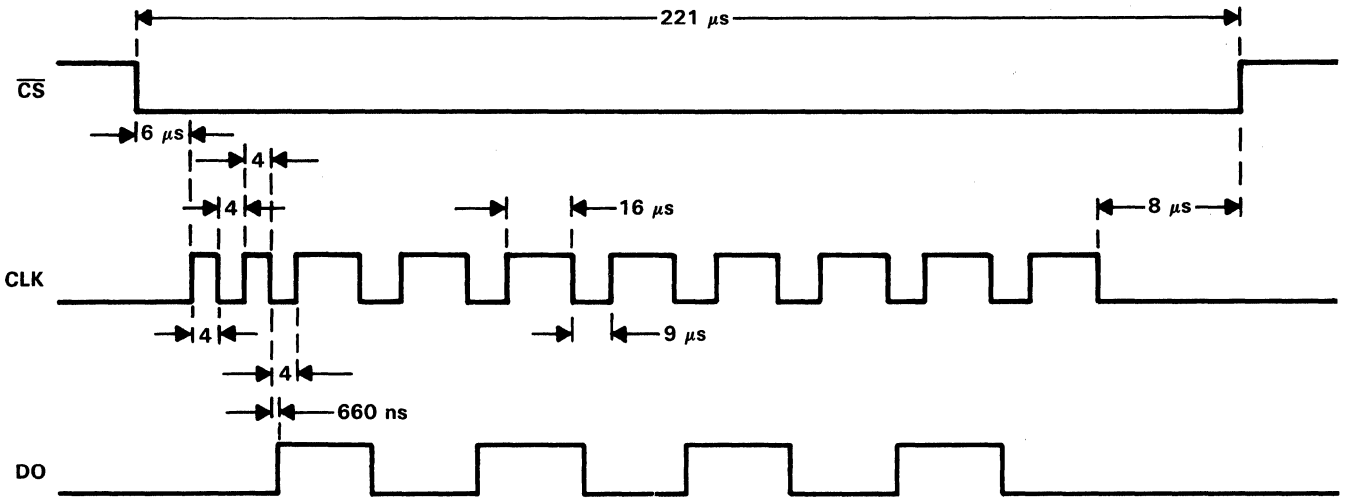


Figure 11-103. 6502 to ADC0831 Interface Timing Diagram

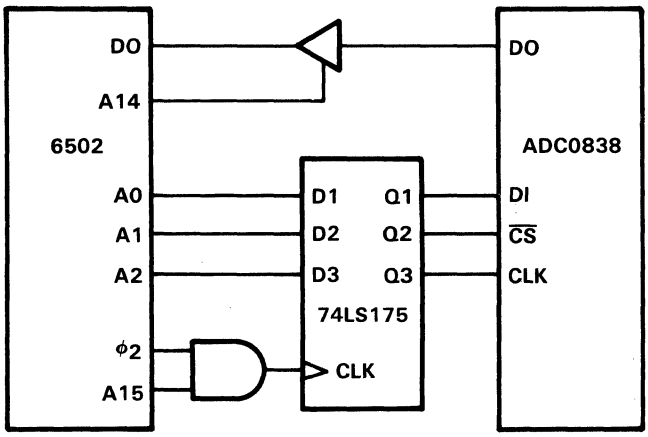


Figure 11-104. 6502 to ADC0838 Interface Circuit Diagram

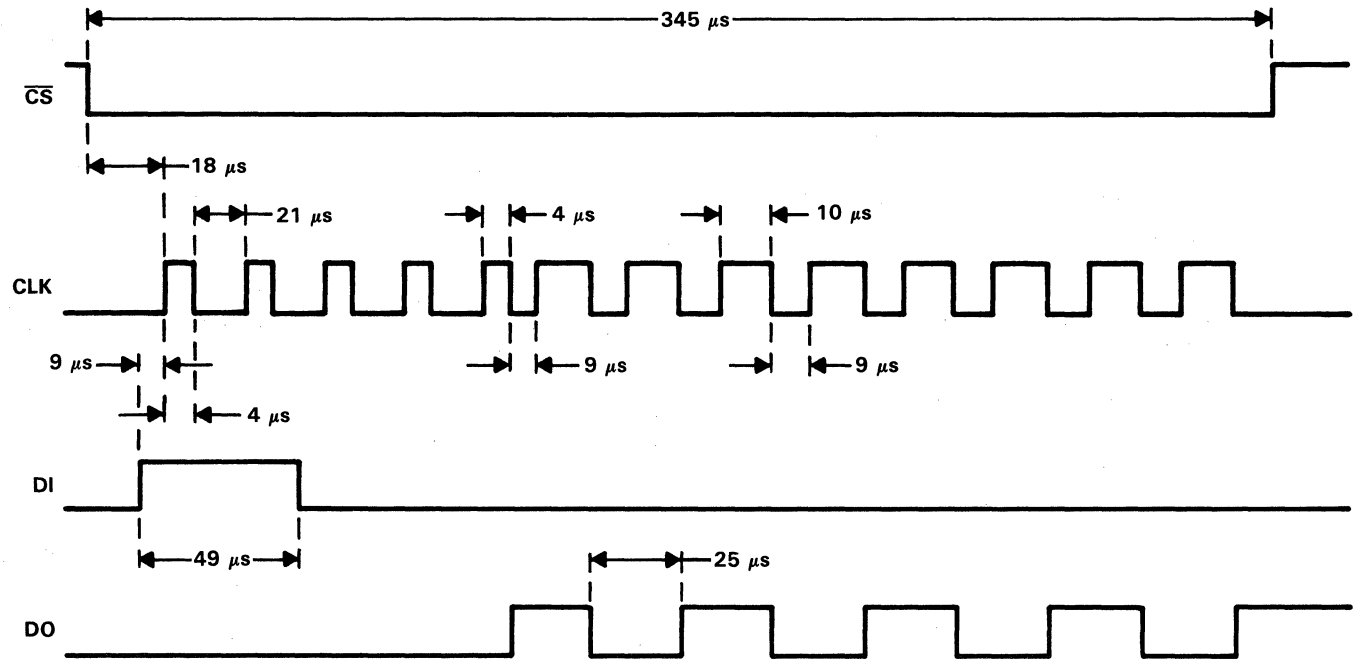


Figure 11-105. 6502 to ADC0838 Interface Timing Diagram

INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO THE MOTOROLA 6805 MICROPROCESSOR

This application describes the circuit configuration and the associated software that can be used to operate the 6805 single-chip microprocessor with the ADC083X converters. The converters are 8-bit successive-approximation devices with serial input/output and a configurable input multiplexer with up to eight channels. These A/D converters are designed to communicate easily with microprocessors in a serial mode. Timing diagrams are presented that describe the interaction between the microprocessor and the A/D converter.

The ADC0832, ADC0834, and ADC0838 devices may be software configured in either the single-ended or differential input mode. Also, the differential [2] inputs can be interchanged through software manipulation. This interface features:

1. Low-cost A/D devices
2. Direct connection between the A/D converter and the microprocessor
3. Fast conversion and communication between the A/D converter and the microprocessor
4. Remote control advantage of serial A/D converters.

Circuitry — ADC0832, ADC0834, and ADC0838 Devices

Figure 11-106 shows the interconnection between the microprocessor and the ADC0832, ADC0834, and ADC0838 A/D converters. This interconnection is identical for all three A/D converters. A microprocessor port pin can be saved by connecting the A/D converters's DI and DO pins to only one microprocessor pin. However, the designer must be careful to define this port pin as an input pin immediately after the initial input bits have been transmitted to the A/D converter. In so doing, the designer will ensure that the pin will be configured as an input when the data conversion mode bits are received by the microprocessor.

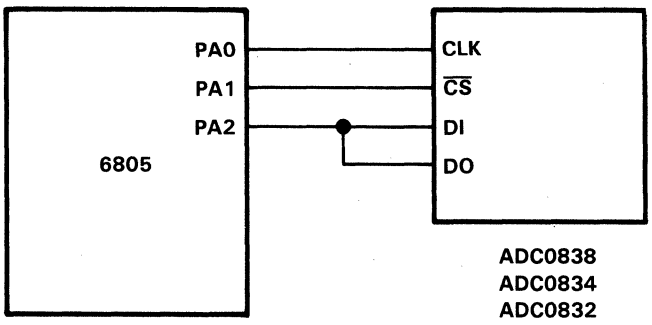


Figure 11-106. 6805 to ADC0832, ADC0834 and ADC0838 Interface Circuit Diagram

Timing Diagram — ADC0838 Device

Figure 11-107 is the timing diagram for the 6805 to ADC0838 interface. Addressing the analog channel, performing conversion, and retrieving the conversion result requires 420 μs. The timing diagrams for the ADC0832 and ADC0834 devices are similar except fewer input bits are transmitted to the A/D converter. The CLC instruction in the software listing provides sufficient delay to allow the A/D converters to set up the conversion result bits on the DO line before they are read by the microprocessor.

Software — ADC0832, ADC0834, and ADC0838 Devices

The software listing describes the software routines for these A/D converters. The software is written so it can be readily applied to any of the three A/D converters as a subroutine so the designer can access the software quickly.

The software differences for these devices are listed below:

	ADC0832	ADC0834	ADC0838
Send Select Bit 1	No	Yes	Yes
Send Select Bit 0	No	No	Yes

The above differences are accommodated by initializing the accumulator and index register correctly before accessing the subroutine. The software listing and Tables 11-18 through 11-23 describe how to accommodate these differences.

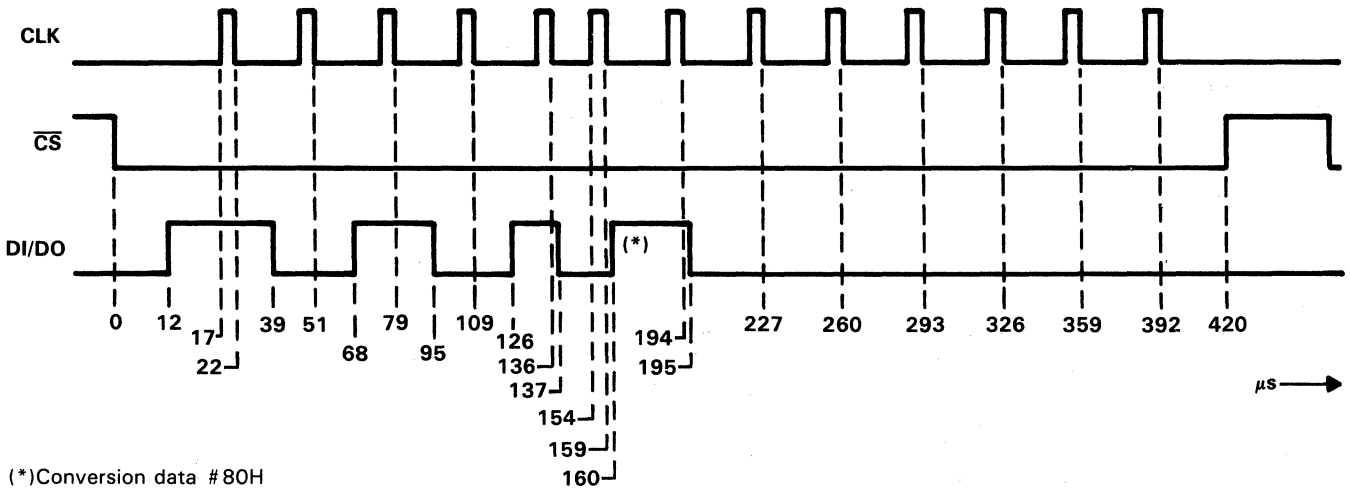


Figure 11-107. Timing Diagram for 6805 to ADC0838 Interface

```
                        ; Software for ADC0832, ADC0834, and ADC0838 to 6805 Interface
                        ;
        ORG  $100H      ; Initialize the starting address for the software
        LDA  #07H       ; Initialize Port A, I/O Pins
        STA  DDR A      ; Configures Port A.0 to A.2 as output pins
        LDA  #A8H       ; For MUX addressing, select appropriate START BIT,
                        ; SGL/DIF(bar), ODD/SIGN, SELECT BIT 1, SELECT BIT 0
                        ; & Load into Acc. Designer can select any MUX
                        ; addressing mode by changing the immediate data.
                        ; See Table 1 to 6 to select the desired MUX
                        ; addressing mode)
        LDX  #05H       ; Set bit counter to 5 or 4 or 3. Designer can
                        ; select any A/D chip out of ADC0838, ADC0834,
                        ; ADC0832.
                        ; Set the immediate date as follows:
                        ;  ADC0838 → Set bit counter to 5
                        ;  ADC0834 → Set bit counter to 4
                        ;  ADC0832 → Set bit counter to 3
        BSR  S83X       ; Load conversion mode bits into Data Input on
                        ; the A/D & Acquire Conversion result into Acc
                        ; from Data out.
                        ; Subroutine S83X
S83X    BCLR 0, Port A  ; Lower CLK
        BCLR 1, Port A  ; Lower Chip Select
S83XRO  ROL  A          ; Shift Conversion Mode bit into C
        BCS  S83XBC     ; If Carry is set ; BRANCH
        BCLR 2, Port A  ; Set 083X DI line to 0
        JMP  S83XJM     ; Go & Raise CLK
S83XBC  BSET 2, Port A  ; Set 083 DI line to 1
S83XJM  BSET 0, Port A  ; Raise CLK
        BCLR 0, Port A  ; Lower CLK
        DECX            ; Decrement Counter
        BNE  S83XRO     ; Do 5 or 4 or 3 times
        BCLR 2, DDR A   ; Configures Port A.2 as an input pin
        LDX  RO, #08H   ; Set bit counter to 8
S83XI   BSET 0, Port A  ; Raise CLK
        BCLR 0, Port A  ; Lower CLK
        CLC             ; Initialize C = 0
        BRCLR 2, Port A, S83X
                        ; If 083X Data out = 0; BRANCH
        SEC             ; 083X Data out = 1; Set C = 1
S83XB   LDA  $20H       ; Get Serial Buffer
        ROL  A          ; Shift Data out Bit into Serial Buffer
        STA  $20H       ; Store Serial Buffer
        DECX            ; Decrement Counter
        BNE  S83XI      ; Do 8 times
        BSET 1, Port A  ; Raise Chip Select
        LDA  $20H       ; Conversion Data is in Accumulator
        RTS             ; Return from Subroutine
        END             ;
```

ADC0832 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 1)

Table 11-18. Single-Ended MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO A_{CC}
	SGL/$\overline{DIF}$	ODD/SIGN	0	1	
1	1	0	+		#C0H
1	1	1		+	#D0H

Table 11-19. Differential MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO A_{CC}
	SGL/$\overline{DIF}$	ODD/SIGN	0	1	
1	0	0	+	−	#80H
1	0	1	−	+	#90H

NOTE 1: Internally, Select 0 is low. Select 1 is high, COMMON is internally connected to ANLG GND.

ADC0834 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 2)

Table 11-20. Single-Ended MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO A_{CC}
	SGL/$\overline{BIT}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	1	0	0	+				#C0H
1	1	0	1			+		#D0H
1	1	1	0		+			#E0H
1	1	1	1				+	#F0H

Table 11-21. Differential MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO A_{CC}
	SGL/$\overline{BIT}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	0	0	0	+	−			#80H
1	0	0	1			+	−	#90H
1	0	1	0	−	+			#A0H
1	0	1	1			−	+	#B0H

NOTE 2: Internally, Select 0 is high, COMMON is internally connected to ANLG GND.

ADC0838 MUX ADDRESSING (5-BIT SHIFT REGISTER)

Table 11-22. Single-Ended MUX Mode

START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG SINGLE-ENDED CHANNEL NO. 0	1	2	3	4	5	6	7	COM	PUT DATA INTO A_{CC}
1	1	0	0	0	+								−	#C0H
1	1	0	0	1			+						−	#C8H
1	1	0	1	0					+				−	#D0H
1	1	0	1	1							+		−	#D8H
1	1	1	0	0		+							−	#E0H
1	1	1	0	1				+					−	#E8H
1	1	1	1	0						+			−	#F0H
1	1	1	1	1								+	−	#F8H

Table 11-23. Differential MUX Mode

START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG DIFFERENTIAL CHANNEL-PAIR NO. 0	1	2	3	4	5	6	7	PUT DATA A_{CC}
1	0	0	0	0	+	−							#80H
1	0	0	0	1			+	−					#88H
1	0	0	1	0					+	−			#90H
1	0	0	1	1							+	−	#98H
1	0	1	0	0	−	+							#A0H
1	0	1	0	1			−	+					#A8H
1	0	1	1	0					−	+			#B0H
1	0	1	1	1							−	+	#C8H

Circuitry — ADC0831 Device

Figure 11-108 shows the interconnection between the microprocessor and the ADC0831 converter. To assure that the conversion result bits can be read by the microprocessor, the port pin which is assigned to the DO line of the A/D converter must be configured as an input.

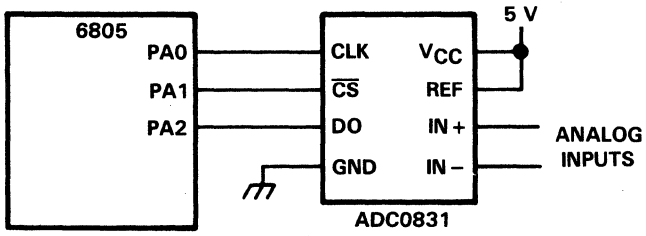


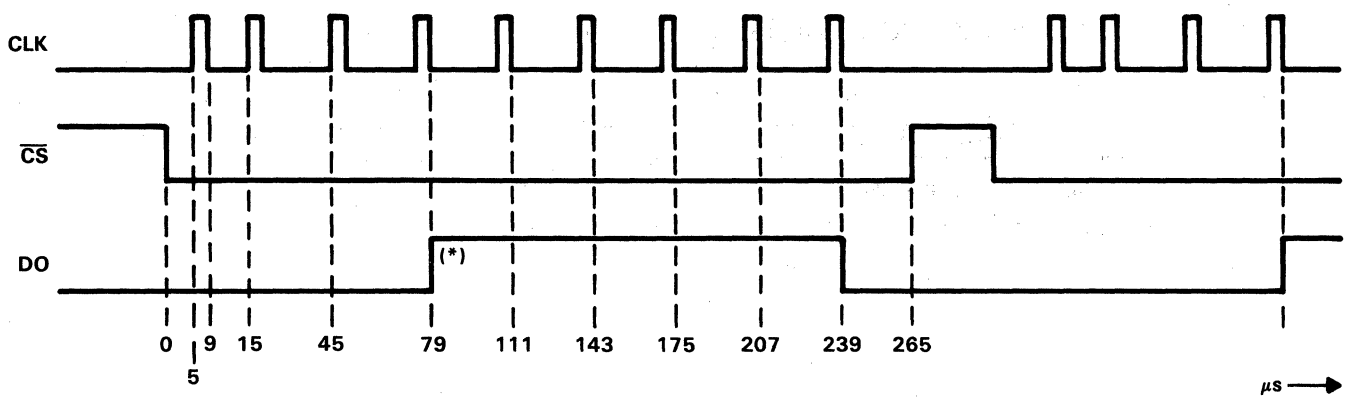
Figure 11-108. 6805 to ADC0831 Interface Circuit Diagram

Timing Diagram — ADC0831 Device

The timing diagram for the 6805 to ADC0831 interface is shown in Figure 11-109. Performing conversion and retrieving the conversion result requires 265 μs. The CLC instruction in the software listing provides sufficient delay to allow the A/D converters to set up the conversion result bits on the DO line before they are read by the microprocessor.

Software — ADC0831 Device

The following software listing presents the routines for this converter. The software is written as a subroutine so the designer can access the software quickly. An initial A/D clock cycle must occur before the eight subsequent clock cycles can be used to extract the conversion result bits from the A/D converter.



(*)Conversion data #3EH

Figure 11-109. Timing Diagram for 6805 to ADC0831 Interface

```
                                ; Software for 6805 to ADC0831 Interface
                                ;
            ORG  $100H          ; Initialize the starting address for the software
            BSR  S831           ; Branch to the Subroutine
                                ; Load 9 clocks to CLK input on the A/D [
                                ; Acquire the Conversion Result into Accumulator.
                                ;
                                ; Subroutine S831
S831        LDA  #03H           ; Initialize Port A, I/O pins
            STA  DDR A          ; Configures Port A.0 and A.1 as output pins
                                ; and Port A.2 as an input pin
            BCLR 0, Port A      ; Lower CLK
            BCLR 1, Port A      ; Lower Chip Select
            BSET 0, Port A      ; Raise CLK
            BCLR 0, Port A      ; Lower CLK
            LDX  #08H           ; Set bit counter to 8
S831I       BSET 0, Port A      ; Raise CLK
            BCLR 0, Port A      ; Lower CLK
            CLC                 ; Initialize C=0
            BRCLR 2, Port A, S831B ; If 0831 Data out=0; BRANCH
            SEC                 ; 0831 Data out=1; Set C=1
S831B       LDA  $20H           ; Get Serial Buffer
            ROL  A              ; Shift Data out Bit into Serial Buffer
            STA  $20H           ; Store Serial Buffer
            DECX                ; Decrement Counter
            BNE  S831I          ; Do 8 times
            BSET 1, Port A      ; Raise Chip Select
            LDA  $20H           ; Conversion Data is in Accumulator
            RTS                 ; Return from Subroutine
            END                 ;
```

INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO MOTOROLA 6800, 6802, 6809, AND 6809E MICROPROCESSORS

The ADC083X family of 8-bit successive-approximation A/D converters is designed to communicate easily with microprocessors in a serial mode. This application shows the circuit configurations and the software that can be used to operate this family of microprocessors with the ADC083X converters. Timing diagrams show the interaction between the microprocessor and the A/D converter.

The ADC0832, ADC0834, and ADC0838 A/D converters can be software configured in either the single-ended or differential input mode. Further, the differential inputs can be interchanged through software manipulation. This interface features:

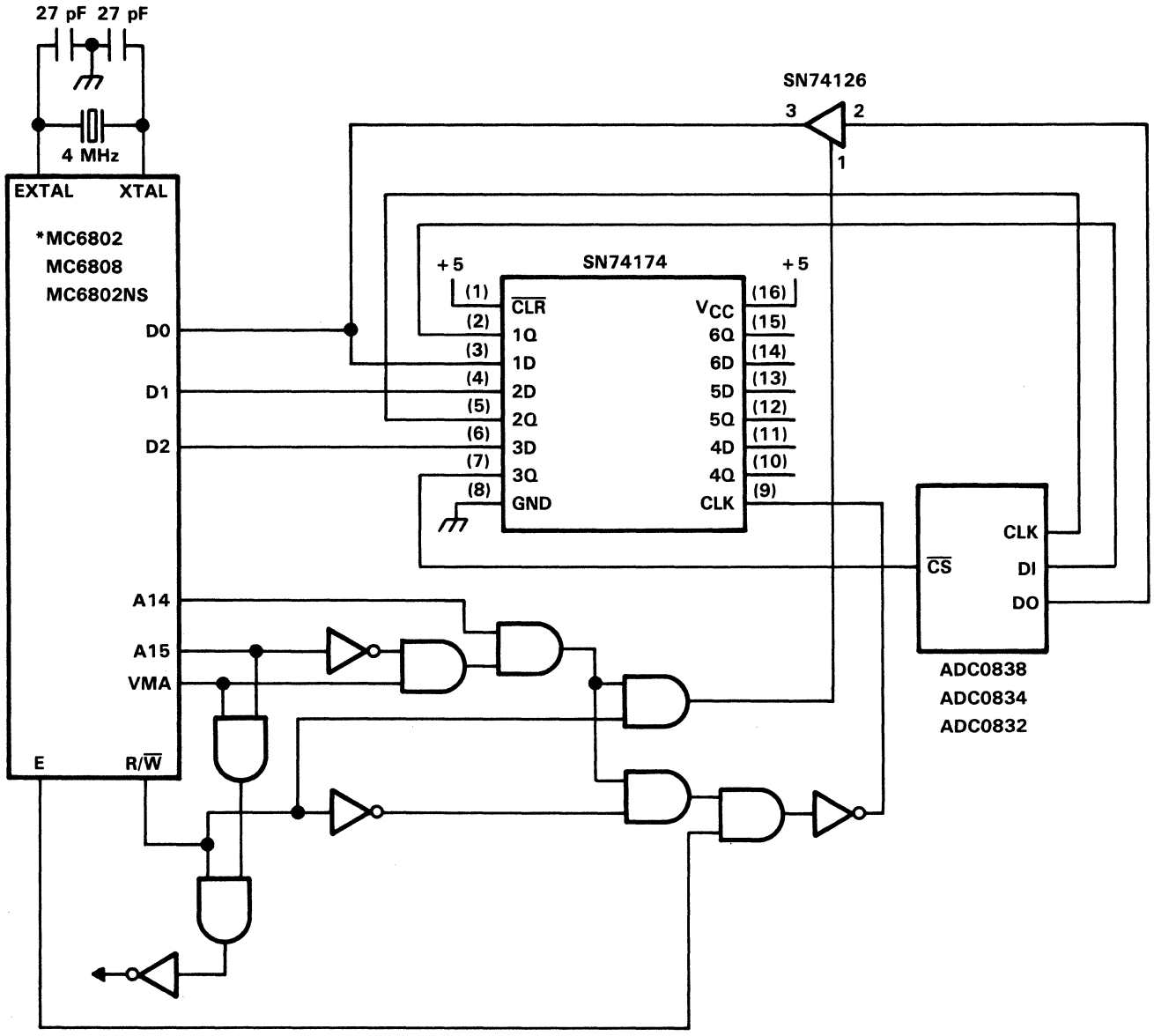
1. Low-cost A/D converter
2. Minimum circuitry
3. Fast conversion and communication between the A/D converter and the microprocessor
4. Remote control advantages of serial A/D converters.

Circuitry — ADC0832, ADC0834, and ADC0838 Devices

Figure 11-110 shows the interconnection between the microprocessor and the ADC0832, ADC0834, and ADC0838 A/D converters. The interconnection is identical for all three converters. The microprocessor DO pin can be used to transmit to and receive digital data from the ADC083X DI and DO pins, respectively. The SN74126 3-state buffer output is in the high-impedance state except during a microprocessor read operation. The SN74174 quad D-type flip-flop is used to synchronize and slow down the write/read communication between the microprocessor and ADC083X converter family so the timing requirements are satisfied. The configuration of AND gates and inverters assures that the flip-flops receive the A/D input data on the negative edge of the E clock. Thus, the flip-flops will receive the correct data. Also, this configuration enables the 3-state buffer and allows the microprocessor to read the A/D DO line when the read/write and address lines are correctly activated. Table 11-24 provides information for adapting the circuit of Figure 11-110 for use with other members of the 6800 family of microprocessors.

Timing Diagram — ADC0838 Device

Figure 11-111 presents the timing diagram for the 6802 to ADC0838 interface. Addressing the analog channel, performing conversion, and retrieving the conversion result requires 449 μs. The timing diagrams for the ADC0832 and ADC0834 converters are similar except fewer input bits are transmitted to the A/D converter. The 3-state buffer enable strobes occur 3 μs after the negative transition of the CLK signal so the conversion result bits have sufficient time to set up on the DO line before these bits are read by the microprocessor.



*See Table 11-24 for information about other Motorola microprocessors.

Figure 11-110. Circuit Diagram for the ADC0832, ADC0834, and ADC0838 Interface

Table 11-24. Adapting Figure 11-121 and Figure 11-124 to Other 6800 Family Microprocessors

MICROPROCESSOR	CRYSTAL OSCILLATOR AND E PIN
6800	ϕ_2 is equivalent to the 6802/6809 E pin. See Figure 11-121 and Figure 11-124.
6802/6808/6802ns	See Figure 11-121 and Figure 11-124
6809	See Figure 11-121 and Figure 11-124
6809E/68HC09E	See Figure 11-121. MC6809 Data sheet for Clock Generator information.

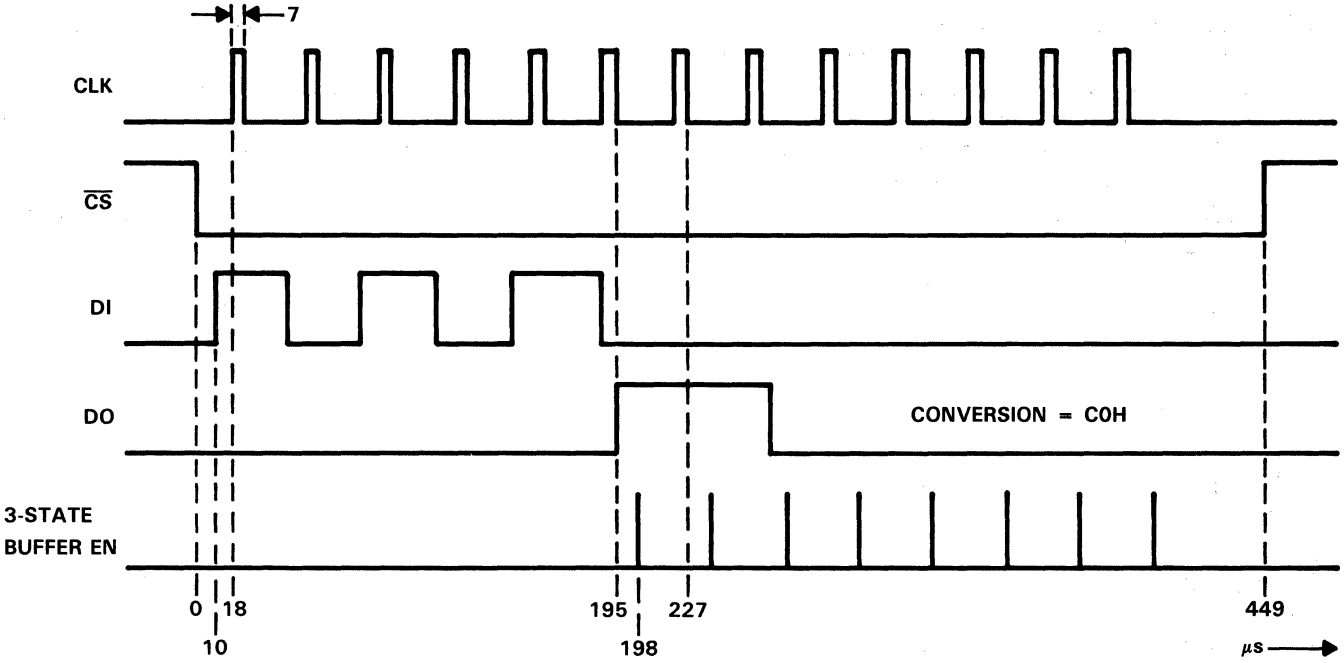


Figure 11-111. Timing Diagram for 6802 — ADC0838 Interface (1 MHz Microprocessor Clock Cycle)

Software — ADC0832, ADC0834, and ADC0838 Devices

The software listing for these converters follows this discussion. The software is written for any of the three A/D converters. Also, the software can be easily incorporated into a subroutine so the designer can access the software quickly. The software differences for these A/D converters are as follows:

	ADC0832	ADC0834	ADC0838
Send Select Bit 1	No	Yes	Yes
Send Select Bit 0	No	No	Yes

The above differences are accommodated by correctly clearing the B accumulator and a byte of RAM that is used as a bit counter before accessing the software. The software listing and Tables 11-25 through 11-30 describe how to accommodate these differences.

```
                        ; Software for 680X Family to ADC0838, ADC0834, ADC0832 Interface
                        ;
                        ;
        40 00           WRITE:      EQU 4000H           ;Interface write address
        40 00           READ:       EQU 4000H           ;Interface read address
                        ;
0000    C6 15           START:      LDAB #15H           ;Load input address in B, See
                                                        ;Tables 11-25 to 11-30, B0 is sent first
0002    86 0                        LDAA #10H           ;ADC0838; Input bit counter = 10H
                                                        ;ADC0834; Input bit counter = 08H
                                                        ;ADC0832; Input bit counter = 04H
0004    97 00           STAA        0000H               ;Store bit counter in RAM
                        ;
0006    86 04           ADC83X      LDAA #04H           ;CS(bar)(A2) = 1, CLK(A1) = 0,
                                                        ;DI/D0(A0) = 0
0008    B7 40 00        STAA        WRITE               ;Write these values to A/D
000B    86 00           LDAA        #00H                ;Lower CS(bar)
000D    B7 40 00                    STAA WRITE
0010    46              ADC83XI:    RORA                ;Prepare to load next bit in A
0011    56                          RORB                ;Put next input bit in carry
0012    49                          ROLA                ;Load next input bit in A0 and re-
                                                        ;align A1 & A2 so they are correct
0013    B7 40 00                    STAA WRITE          ;Set up next bit on DI line
0016    8A 02                       ORAA #02H           ;Raise CLK line and clock in,
0018    B7 40 00                    STAA WRITE          ;next bit
001B    84 FD                       ANDA #FDH           ;Lower CLK line
001D    B7 40 00                    STAA WRITE
0020    76 00 00                    ROR 0000H           ;Rotate bit counter
0023    24 EB                       BCC ADC83XI         ;If carry = 0; branch
0025    86 80                       LDAA #80H           ;Conversion bit counter = 8
0027    97 00                       STAA 000H           ;Store bit counter in RAM
0029    86 2            ADC83XO:    LDAA #02H           ;Raise CLK & keep CS(bar) = 0
002B    B7 40 00                    STAA WRITE
002E    86 00                       LDAA #00H           ;Lower CLK line and clock out,
0030    B7 40 00                    STAA WRITE          ;next conversion bit
0033    B6 40 00                    LDAA READ           ;Put next conversion bit in A0
0036    46                          RORA                ;Put conversion bit in carry
0037    59                          ROLB                ;Put conversion bit in B0 and
                                                        ;shift other conversion bits in B
0038    76 00 00                    ROR 0000H           ;Rotate bit counter
003B    24 EC                       BCC ADC83XO         ;If carry = 0; branch
003D    86 04                       LDAA #04H           ;Raise CS(bar)
003F    B7 40 00                    STAA WRITE
0042                                END                 ;Conversion result is in B accumulator
```

ADC0832 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 1)

Table 11-25. Single-Ended MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO ACCUMULATOR B
	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1	
1	1	0	+		#03H
1	1	1		+	#0BH

Table 11-26. Differential MUX Mode

START BIT	MUX ADDRESS		CHANNEL NO.		PUT DATA INTO ACCUMULATOR B
	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1	
1	0	0	+	−	#01H
1	0	1	−	+	#05H

NOTE 1: Internally, Select 0 is low. Select 1 is high, COMMON is internally connected to ANLG GND.

ADC0834 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 2)

Table 11-27. Single-Ended MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO ACCUMULATOR B
	SGL/$\overline{\text{BIT}}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	1	0	0	+				#03H
1	1	0	1			+		#0BH
1	1	1	0		+			#07H
1	1	1	1				+	#0FH

Table 11-28. Differential MUX Mode

START BIT	MUX ADDRESS			CHANNEL NO.				PUT DATA INTO ACCUMULATOR B
	SGL/$\overline{\text{BIT}}$	ODD/SIGN	SELECT 1	0	1	2	3	
1	0	0	0	+	−			#01H
1	0	0	1			+	−	#09H
1	0	1	0	−	+			#05H
1	0	1	1			−	+	#0DH

NOTE 2: Internally, Select 0 is high, COMMON is internally connected to ANLG GND.

ADC0838 MUX ADDRESSING (5-BIT SHIFT REGISTER)

Table 11-29. Single-Ended MUX Mode

START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG SINGLE-ENDED CHANNEL NO. 0	1	2	3	4	5	6	7	COM	PUT DATA INTO ACCUMULATOR B
1	1	0	0	0	+								−	#03H
1	1	0	0	1			+						−	#13H
1	1	0	1	0					+				−	#0BH
1	1	0	1	1							+		−	#1BH
1	1	1	0	0		+							−	#07H
1	1	1	0	1				+					−	#17H
1	1	1	1	0						+			−	#0FH
1	1	1	1	1								+	−	#1FH

Table 11-30. Differential MUX Mode

START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG DIFFERENTIAL CHANNEL-PAIR NO. 0: 0	0: 1	1: 2	1: 3	2: 4	2: 5	3: 6	3: 7	PUT DATA INTO ACCUMULATOR B
1	0	0	0	0	+	−							#01H
1	0	0	0	1			+	−					#11H
1	0	0	1	0					+	−			#09H
1	0	0	1	1							+	−	#19H
1	0	1	0	0	−	+							#05H
1	0	1	0	1			−	+					#15H
1	0	1	1	0					−	+			#0DH
1	0	1	1	1							−	+	#13H

Circuitry — ADC0831 Device

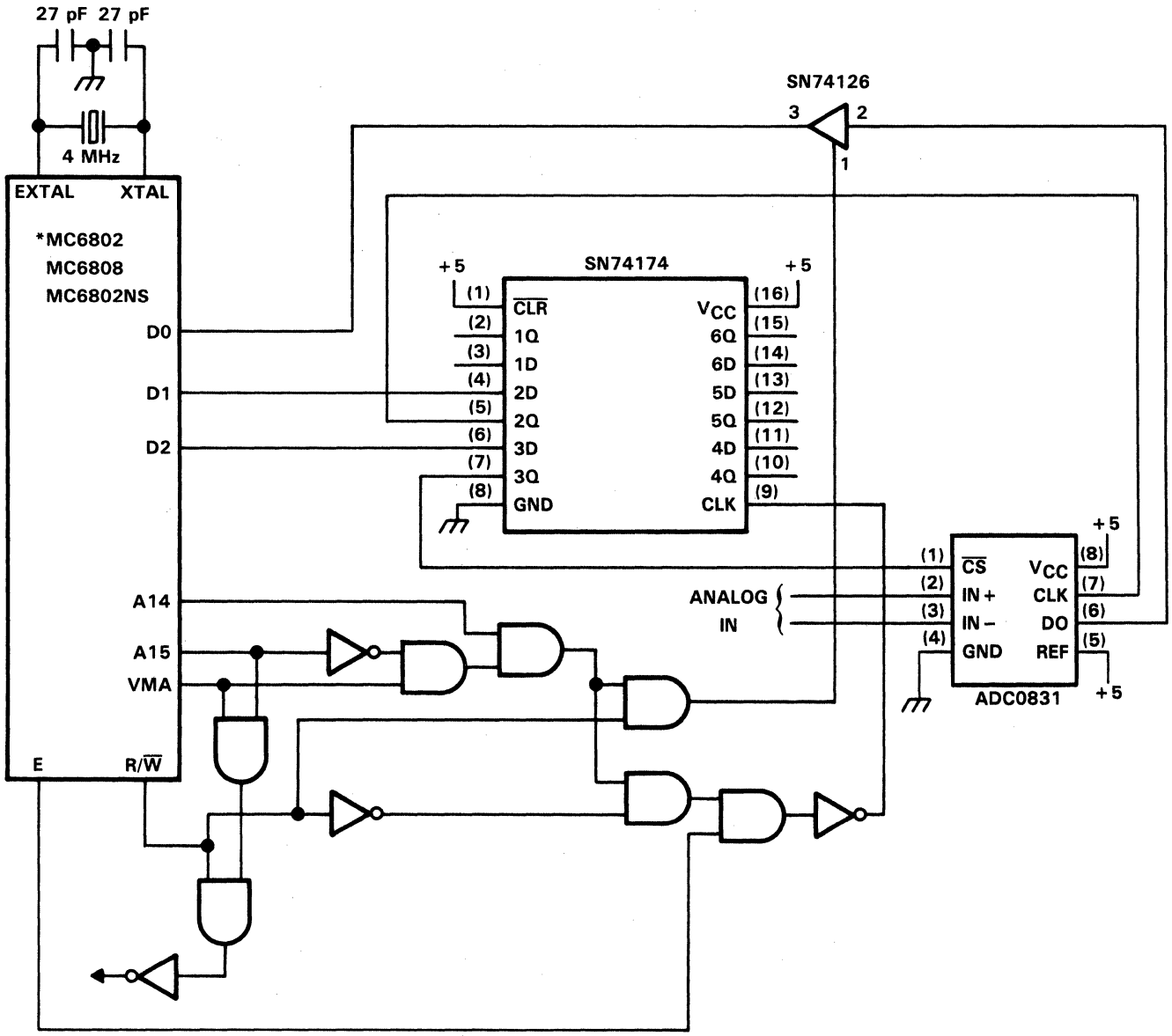
Figure 11-112 shows the interconnection between the microprocessor and the ADC0831 converter. The circuitry is basically the same as for the ADC0832, ADC0834 and ADC0838 interface except the ADC0831 does not have a DI line. Table 11-24 provides information that will help the designer adapt the circuit of Figure 11-112 to other members of the 6800 family of microprocessors.

Timing Diagram — ADC0831 Device

Figure 11-113 shows the timing diagram for the 6802 to ADC0831 interface. Performing conversion and retrieving the conversion result requires 283 μs. The 3-state buffer enable strobes occur 3 μs after the negative transition of the CLK signal so the conversion result bits have sufficient time to set up on the DO line before these bits are read by the microprocessor.

Software — ADC0831 Device

The following software listing provides the software routines for this converter. The software can be easily incorporated into a subroutine so the designer can access the software quickly. An initial A/D clock cycle must occur before the eight subsequent clock cycles can be used to extract the conversion result bits from the A/D converter.



*See Table 11-24 for information about other Motorola microprocessors.

Figure 11-112. Circuit Diagram for the ADC0831 Interface

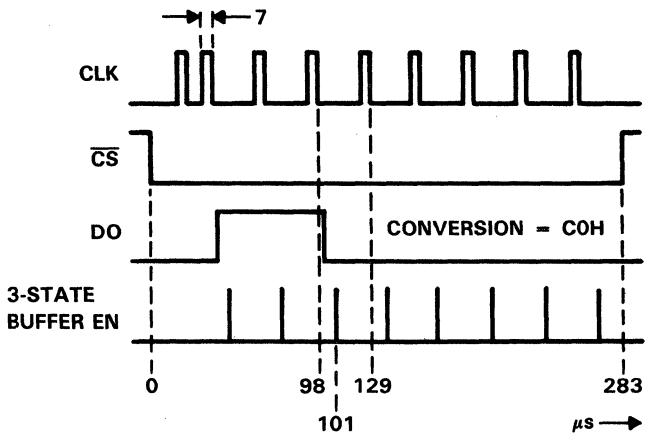


Figure 11-113. Timing Diagram for 6802 to ADC0831 Interface (1 MHz Microprocessor Clock Cycle)

```
                        ; Software for 680X Family to ADC0831 Interface
                        ;
                        ;
        40 00           WRITE:    EQU 4000H       ;Interface write address
        40 00           READ:     EQU 4000H       ;Interface read address
                        ;
0000    86 04           START:    LDAA #04H       ;CS(bar)(A2) = 1, CLK(A1) = 0
0002    B7 40 00                  STAA WRITE      ;Write these values to A/D
0005    86 00                     LDAA #00H       ;Lower CS(bar)
0007    B7 40 00                  STAA WRITE
000A    86 02                     LDAA #02H       ;Raise CLK initially
000C    B7 40 00                  STAA WRITE
000F    86 00                     LDAA #00H       ;Lower CLK initially
0011    B7 40 00                  STAA WRITE
0014    86 80                     LDAA #80H       ;Conversion bit counter = 8
0016    97 00                     STAA 0000H      ;Store bit counter in RAM
0018    86 02           ADC8310:  LDAA #02H       ;Raise CLK and keep CS(bar) = 0
001A    B7 40 00                  STAA WRITE
001D    86 00                     LDAA #00H       ;Lower CLK line and clock out,
001F    B7 40 00                  STAA WRITE      ;next conversion bit
0022    B6 40 00                  LDAA READ       ;Put next conversion bit in A0
0025    46                        RORA            ;Put conversion bit in carry
0026    59                        ROLB            ;Put conversion bit in B0 and
                                                  ;shift other conversion bits in B
0027    76 00 00                  ROR 0000H       ;Rotate bit counter
002A    24 EC                     BCC ADC8310     ;If carry = 0; branch
002C    86 04                     LDAA #04H       ;Raise CS(bar)
002E    B7 40 00                  STAA WRITE
0031                              END             ;Conversion result is in B accumulator
```

INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO INTEL 8051 AND 8052 MICROPROCESSORS

This appplication presents the circuit configurations and the associated software that can be used to operate the 8051 and 8052 family of microprocessors with the ADC083X converters. Timing diagrams show the interaction between microprocessor and the A/D converter.

The ADC0832, ADC0834, and ADC0838 converters can be software configured in either the single-ended or differential input mode. Also, the differential ± inputs may be interchanged through software manipulation. This serial interface features:

1. Low-cost A/D converter
2. Direct connection between the A/D converter and the microprocessor
3. Fast conversion and communication between the A/D converter and the microprocessor
4. Remote control advantages of serial A/D converters.

The 8051 and 8052 microprocessor family consists of the following:

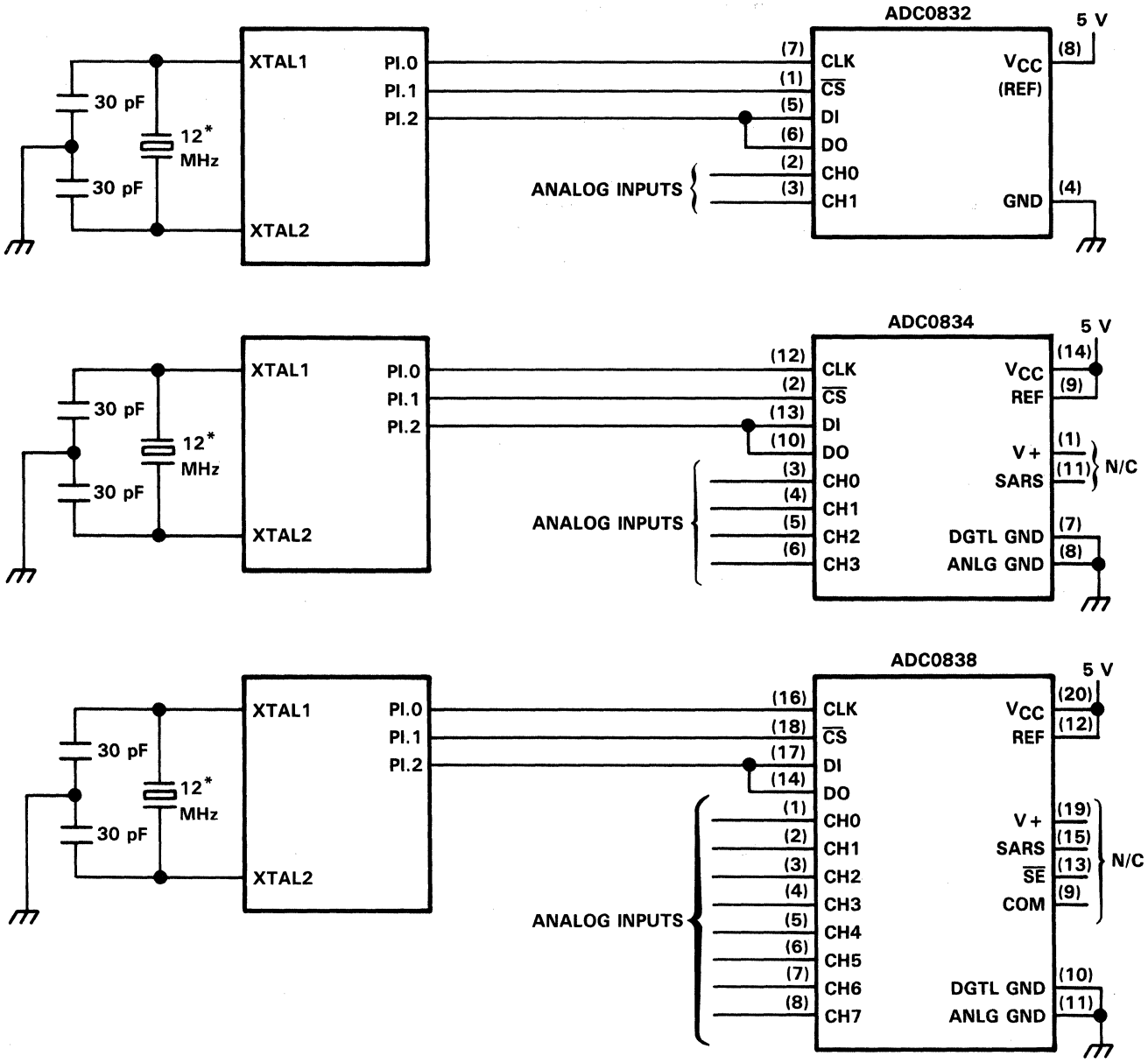
8031AH	8052AH
8032AH	80C51
8051AH	8751H

Circuitry — ADC0832, ADC0834, and ADC0838 Devices

Figure 11-114 shows the interface between the microprocessor and the ADC0832, ADC0834, and ADC0838 A/D converters. The interconnection is identical for these converters. A microprocessor port pin can be saved by connecting the A/D converter's DI and DO pins to one microprocessor port pin. However, the designer must be careful to define this port pin as an input pin immediately after the initial input bits have been transmitted to the A/D converter. By doing this, the designer will ensure that the pin will be configured as an input when the data conversion bits are received by the microprocessor.

Timing Diagram — ADC0838 Device

Figure 11-115 presents the timing diagram for the 8051 and 8052 to ADC0838 interface. Addressing the analog channel, performing conversion, and retrieving the conversion result requires only 150 μs. The timing diagrams for the ADC0834 and ADC0832 converters are similar except fewer input bits are transmitted to the A/D converter. The CLR instruction in the software listing provides sufficient delay to allow the A/D converter to set up the conversion result bits on the DO line before they are read by the microprocessor.



*11 MHz for 8048/49 Family

Intel 8051/52 Family: 8031AH, 8051AH
8032AH, 8052AH
8751AH, 80C51

Intel 8048/49 Family: 8048AH, 8748H
8035AHL, 8049AH
8749H, 8039AHL
8050AH, 8040AHL
80C49

Figure 11-114. The Intel 8051/52 or 8048/49 to ADC0832, ADC0834, and ADC0838 Interface Circuit Diagram

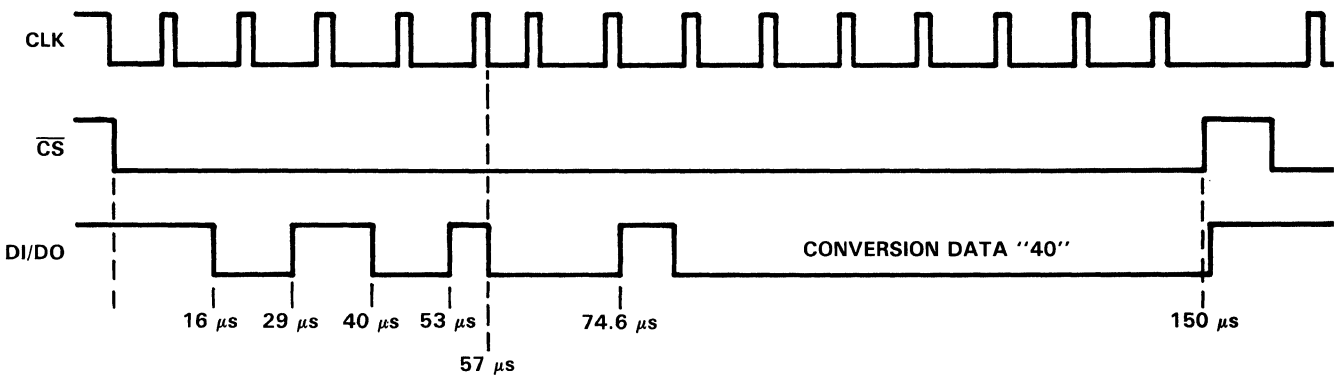


Figure 11-115. Timing Diagram for the Intel 8051/52 to ADC0838 Interface

Software

The following software listing provides the software routines for these A/D converters. The software is written so it can be readily applied to any of the three A/D converters and as a subroutine so the designer can access the software quickly.

The software differences for these A/D converters are as follows:

	ADC0832	ADC0834	ADC0838
Send Select Bit 1	No	Yes	Yes
Send Select Bit 0	No	No	Yes

The above differences are accommodated by initializing the accumulator and the R6 register correctly before accessing the subroutine. The software listing and Tables 11-31 through 11-36 describe how to accommodate these differences.

```
                    ; Software for Intel 8051/52 or 8048/49 to ADC0832, 0834, 0838 Interface
                    ;
        MOV A, #A8H ; For MUX addressing, select appropriate
                    ; START BIT, SGL/DIF(bar), ODD/SIGN, SELECT
                    ; BIT 1, SELECT BIT 0 and Load into Acc.
                    ; Designer can select any MUX addressing
                    ; mode by changing the immediate data
                    ; (See Table 1 to 6 to select the desired
                    ; MUX addressing mode)
        MOV R6, #05H; Set bit counter to 5
                    ; Designer can select any A/D chip out of
                    ; ADC0838, ADC0834, ADC0832
                    ; Set the immediate data as follows:
                    ;  ADC0838 → Set bit counter to 5
                    ;  ADC0834 → Set bit counter to 4
                    ;  ADC0832 → Set bit counter to 3
        ACALL S83X  ; Load conversion mode bits into Data Input
                    ; on the A/D chip & Acquire Conversion
                    ; Result into Accumulator from Data Output
                    ;
                    ; Subroutine S83X
        CLR P1.0    ; Lower CLK
S83X    CLR P1.1    ; Lower Chip Select
S83XRL  RLC A       ; Shift Conversion Mode bit into C
        JC S83XJC   ; If Carry is set ; BRANCH
        ANL P1, #FBH; Set 083X DI line to 0
        SJMP S83XSJ ; Go & Raise CLK
S83XJC  ORL P1, #04H; Set 083X DI line to 1
S83XSJ  NOP         ; Delay to Set up Mode bit
        CPL P1.0    ; Raise CLK
        NOP         ; Delay to slow CLK
        CLR P1.0    ; Lower CLK
        DJNZ R6, 83XRL ; Do 5, 4, or 3 times
        ORL P1, #04H; Configure P1.2 as an input pin
        MOV R0, #08H; Set bit counter to 8
```

```
S83XI   CPL P1.0            ; Raise CLK
        NOP                 ; Delay to slow CLK
        CLR P1.0            ; Lower CLK
        CLR C               ; Initialize C = 0
        JNB P1.2, S83XJ     ; If 083X Data out = 0; BRANCH
                            ; This pin must be in input mode

        CPL C               ; 083X Data out = 1; Set C = 1
S83XJ   MOV A,R1            ; Get Serial Buffer
        RLC A               ; Shift Data out Bit into Serial Buffer
        MOV R1,A            ; Store Serial Buffer
        DJNZ R0, S83XI      ; Do 8 times
        CPL P1.1            ; Raise Chip Select
        MOV A,R1            ; Conversion Data is in Accumulator
        RET                 ;
        END;
```

ADC0832 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 1)

Table 11-31. Single-Ended MUX Mode

START	MUX ADDRESS		CHANNEL NO.		PUT DATA
BIT	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1	INTO A_{CC}
1	1	0	+		#C0H
1	1	1		+	#D0H

Table 11-32. Differential MUX Mode

START	MUX ADDRESS		CHANNEL NO.		PUT DATA
BIT	SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1	INTO A_{CC}
1	0	0	+	−	#80H
1	0	1	−	+	#A0H

NOTE 1: Internally, Select 0 is low. Select 1 is high, COMMON is internally connected to ANLG GND.

ADC0834 MUX ADDRESSING (5-BIT SHIFT REGISTER) (See Note 2)

Table 11-33. Single-Ended MUX Mode

START	MUX ADDRESS			CHANNEL NO.				PUT DATA
BIT	SGL/$\overline{\text{BIT}}$	ODD/SIGN	SELECT 1	0	1	2	3	INTO A_{CC}
1	1	0	0	+				#C0H
1	1	0	1			+		#D0H
1	1	1	0		+			#E0H
1	1	1	1				+	#F0H

Table 11-34. Differential MUX Mode

START	MUX ADDRESS			CHANNEL NO.				PUT DATA
BIT	SGL/$\overline{\text{BIT}}$	ODD/SIGN	SELECT 1	0	1	2	3	INTO A_{CC}
1	0	0	0	+	−			#80H
1	0	0	1			+	−	#90H
1	0	1	0	−	+			#A0H
1	0	1	1			−	+	#B0H

NOTE 2: Internally, Select 0 is high, COMMON is internally connected to ANLG GND.

ADC0838 MUX ADDRESSING (5-BIT SHIFT REGISTER)

Table 11-35. Single-Ended MUX Mode

START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG SINGLE-ENDED CHANNEL NO. 0	1	2	3	4	5	6	7	COM	PUT DATA INTO A_{CC}
1	1	0	0	0	+								−	#C0H
1	1	0	0	1			+						−	#C8H
1	1	0	1	0					+				−	#D0H
1	1	0	1	1							+		−	#D8H
1	1	1	0	0		+							−	#E0H
1	1	1	0	1				+					−	#E8H
1	1	1	1	0						+			−	#F0H
1	1	1	1	1								+	−	#F8H

Table 11-36. Differential MUX Mode

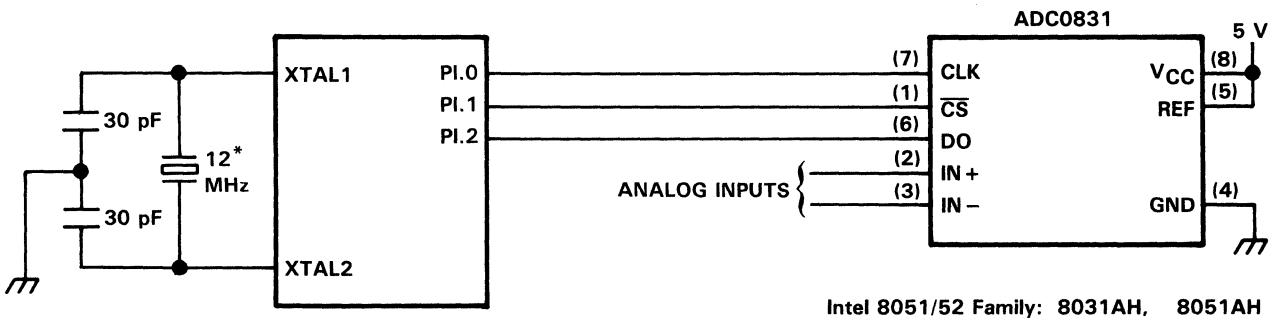
START BIT	MUX ADDRESS: SGL/$\overline{DIF}$	MUX ADDRESS: ODD/SIGN	MUX ADDRESS: SELECT 1	MUX ADDRESS: SELECT 0	ANALOG DIFFERENTIAL CHANNEL-PAIR NO. 0: 0	0: 1	1: 2	1: 3	2: 4	2: 5	3: 6	3: 7	PUT DATA A_{CC}
1	0	0	0	0	+	−							#80H
1	0	0	0	1			+	−					#88H
1	0	0	1	0					+	−			#90H
1	0	0	1	1							+	−	#98H
1	0	1	0	0	−	+							#A0H
1	0	1	0	1			−	+					#A8H
1	0	1	1	0					−	+			#B0H
1	0	1	1	1							−	+	#B8H

Circuitry — ADC0831 Device

Figure 11-116 shows the interconnection between the microprocessor and the ADC0831 converter. To assure that the conversion result bits can be read by the microprocessor, the designer must configure the microprocessor port pin which is assigned to the DO line of the A/D converter as an input.

Timing Diagram — ADC0831 Device

Figure 11-117 shows the timing diagram for the 8051 and 8052 to ADC0831 interface. Performing conversion and retrieving the conversion result requires only 91 μs. The CLR C instruction in the software listing provides sufficient delay to allow the A/D converter to set up the conversion result bits on the D line before they are read by the microprocessor.



*11 MHz for 8048/49 Family

Intel 8051/52 Family: 8031AH, 8051AH, 8032AH, 8052AH, 8751AH, 80C51

Intel 8048/49 Family: 8048AH, 8748H, 8035AHL, 8049AHL, 8749H, 8039AHL, 8050AH, 8040AHL, 80C49

Figure 11-116. The Intel 8051/52 or 8048/49 to ADC0831 Interface Circuit Diagram

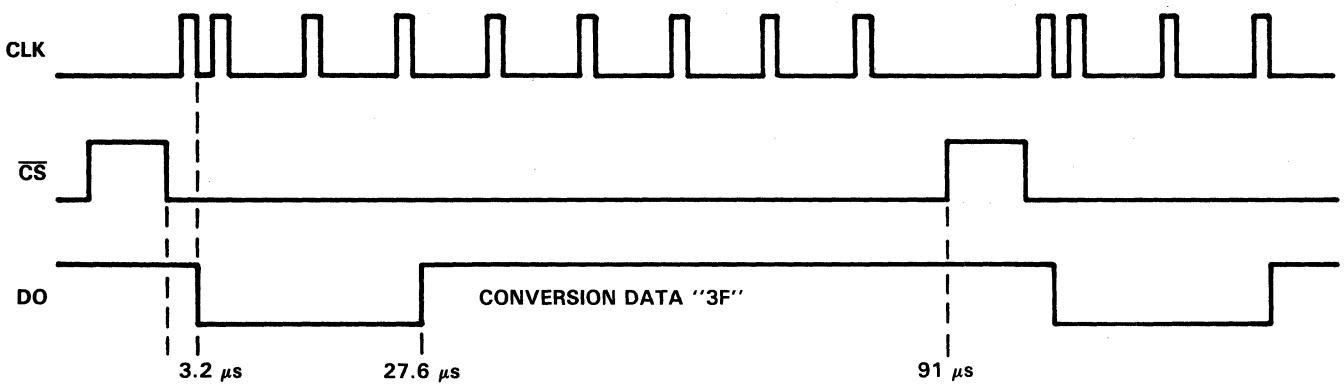


Figure 11-117. Timing Diagram for the Intel 8051/52 to ADC0831 Interface

Software — ADC0831 Device

The following software listing provides the software routines for this A/D converter. The software is written as a subroutine so the designer can access the software quickly. An initial A/D clock cycle must occur before the eight subsequent clock cycles can be used to extract the conversion result bits from the A/D converter.

```
                        ; Software for Intel 8051/52 Interface to ADC0831
                        ;
                        ;
                        ;
                        ;
        ACALL S831      ; Load 9 clocks to CLK input on the A/D
                        ; chip & Acquire Conversion result
                        ; into Accumulator
                        ;
                        ; Subroutine S831
S831    ORL P1,04H      ; Configure P1.2 as an input pin
        CLR P1.0        ; Lower CLK
        CLR P1.1        ; Lower Chip Select
        CPL P1.0        ; Raise CLK
        NOP             ; Delay to slow CLK
        CLR P1.0        ; Lower CLK
        MOV R0, #8H     ; Set bit counter to 8
S831I   CPL P1.0        ; Raise CLK
        NOP             ; Delay to slow CLK
        CLR P1.0        ; Lower CLK
        CLR C           ; Initialize C=0
        JNB P1.2,S831J  ; If 0831 Data out=0 ; BRANCH
                        ; This pin must be in input mode
        CPL C           ; 0831 Data out=1 ; Set C=1
S831J   MOV A,R1        ; Get Serial Buffer
        RLC A           ; Shift Data out Bit into Serial Buffer
        MOV R1,A        ; Store Serial Buffer
        DJNZ R0,S831I   ; Do 8 times
        CPL P1.1        ; Raise Chip Select
        MOV A,R1        ; Conversion Data is in Accumulator
        RET             ;
        END             ;
```

INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO INTEL 8048 AND 8049 MICROPROCESSORS

Refer to the INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO INTEL 8051 AND 8052 MICROPROCESSORS application for additional information regarding these devices. The 8048 and 8049 microprocessor family consists of the following:

8035AHL	8045AH	8748AH
8039AHL	8049AH	8749H
8040AHL	8050AH	80C49

Circuitry — ADC0838, ADC0834, and ADC0832

See Figure 11-114 in the previous application for circuitry also used with this family of converters.

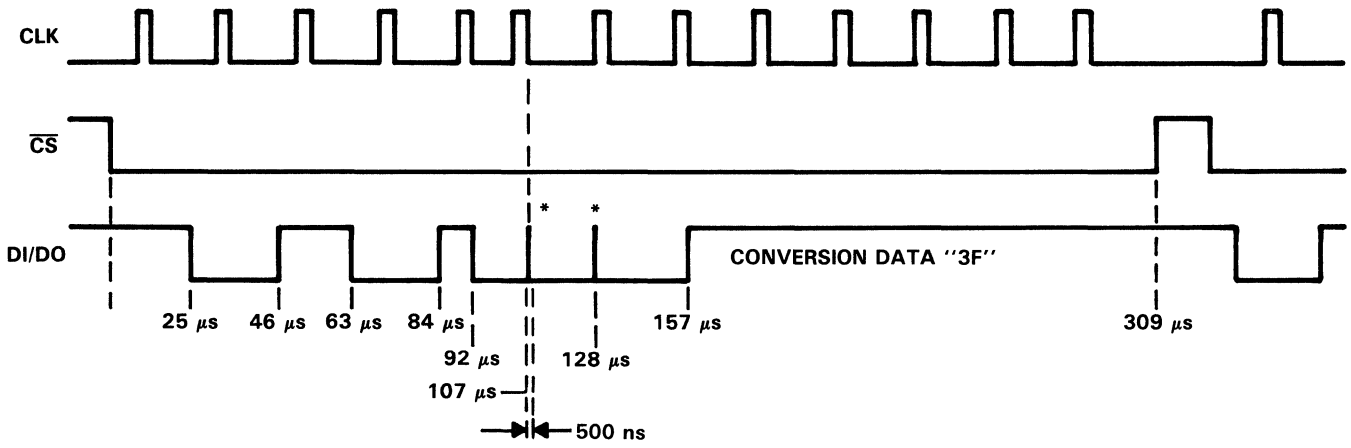
Timing Diagram — ADC0838 Device

Figure 11-118 presents the timing diagram for the 8048 and 8049 to ADC0838 interface. Addressing the analog channel, performing conversion, and retrieving the conversion result requires 309 μs. The timing diagrams for the ADC0834 and ADC0832 converters are similar except fewer input bits are transmitted to the A/D converter.

The NOP and CLR C instructions in the software listing provide sufficient delay to allow the A/D converter to set up the conversion result bits on the DO line before they are read by the microprocessor. Also, these instructions guarantee that occasional spikes on the DI/DO line during clock edges will not cause erroneous readings. These spikes appeared during our testing and may have been due to our test circuit layout. However, these spikes are harmless because they appear during clock edges and the delay time of the NOP and CLR C instructions is longer than the decay time of the spikes. Therefore, the DO line can be read accurately. If the designers feel uncomfortable with these spikes, they may connect the DI/DO line to a microprocessor port other than the port to which the A/D clock line is connected. For example, the A/D converter chip select and clock lines might be connected to port 1 of the microprocessor, while the DI/DO line might be connected to port 2. This use of two different ports eliminates the occasional spike action.

Software — ADC0838, ADC0834, and ADC0832 Devices

See the INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO INTEL 8051 AND 8052 MICROPROCESSORS application for more information on these A/D converters. When reading that application, substitute the software listing for this application.



*Designer may see some spikes on the Data Output that do not effect the reading of the conversion results, since the microprocessor reads the DO pin after the spikes occur (see description of timing diagram).

Figure 11-118. Timing Diagram for the Intel 8048/49 to ADC0838 Interface

```
                    ; Software for Intel 8051 and 8052 to ADC8032,
                      ADC8034 and ADC8038 Interface
MOV A, #A8H         ; For MUX addressing, select appropriate
                    ; START BIT, SGL/DIF(bar), ODD/SIGN, SELECT
                    ; BIT 1, SELECT BIT 0 and Load into Acc.
                    ; Designer can select any MUX addressing

                    ; mode by changing the immediate data
                    ; (See Table 1 to 6 to select the desired
                    ; MUX addressing mode)
```

```
        MOV R6, #05H        ; Set bit counter to 5
                            ; Designer can select any A/D chip out of
                            ; ADC0838, ADC0834, ADC0832
                            ; Set the immediate data as follows:
                            ; ADC0838 → Set bit counter to 5
                            ; ADC0834 → Set bit counter to 4
                            ; ADC0832 → Set bit counter to 3
        CALL S83X           ; Load conversion mode bits into Data Input
                            ; on the A/D chip & Acquire Conversion
                            ; Result into Accumulator from Data Output
                            ;
                            ;
                            ; Subroutine S83X
        ANL P1,#FEH         ; Lower CLK
S83X    ANL P1,#FDH         ; Lower Chip Select
S83XRL  RLC A               ; Shift Conversion Mode bit into C
        JC S83XJC           ; If Carry is set: BRANCH
        ANL P1,#FBH         ; Set 83X DI line to 0
        JMP S83XSJ          ; Go & Raise CLK
S83XJC  ORL P1,#04H         ; Set 83X DI line to 1
S83XSJ  NOP                 ; Delay to Set up Mode bit
        ORL P1,#01H         ; Raise CLK
        NOP                 ; Delay to slow CLK
        ANL P1,#FEH         ; Lower CLK
        DJNZ R6,S83XRL      ; Do 5, 4, or 3 times
        MOV R0,#08H         ; Set bit counter to 8
S83XI   ORL P1,#01H         ; Raise CLK
        NOP                 ; Delay to slow CLK
        ANL P1,#FEH         ; Lower CLK
        NOP                 ; To guarantee that occasional spike on DI/DO
                            ; at clock edges do not cause erroneous readings
        CLR C               ; Initialize C=0
        IN A,P1             ; Get Port 1
        CPL A               ; Complement Accumulator
        JB2 S83XJ           ; If 083X Data out=1: BRANCH
        CPL C               ; 083X Data out=1: Set C=1
S83XJ   MOVA,R1             ; Get Serial Buffer
        RLC A               ; Shift Data out Bit into Serial Buffer
        MOV R1,A            ; Store Serial Buffer
        DJNZ R0,S83XI       ; Do 8 times
        ORL P1,#02H         ; Raise Chip Select
        MOV A,R1            ; Conversion Data is in Accumulator
        RET                 ;
        END                 ;
```

Circuitry — ADC0831 Device

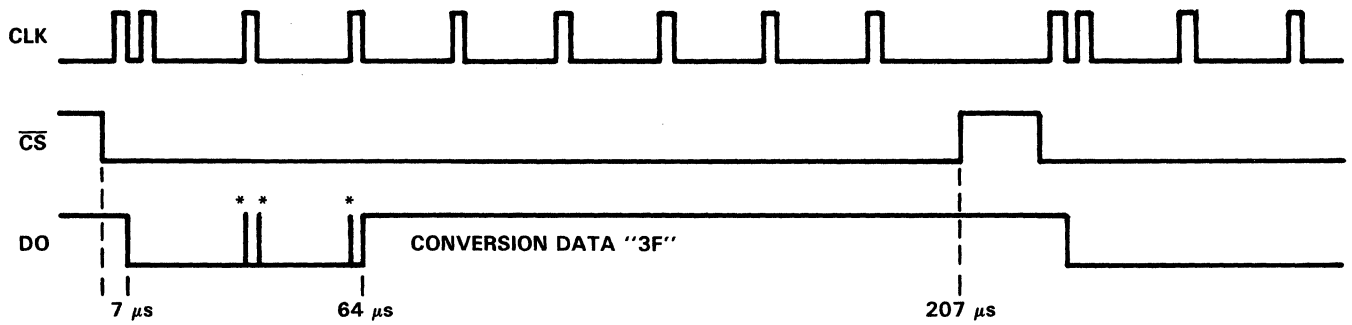
See the INTERFACE FOR ADC0831, ADC0832, ADC0834, AND ADC0838 CONVERTERS TO INTEL 8051 AND 8052 MICROPROCESSORS application.

Timing Diagram — ADC0831 Device

Figure 11-119 shows the timing diagram for the 8048 and 8049 to ADC0831 interface. Performing conversion and retrieving the conversion result requires only 207 μs. The CLR instruction in the software listing provides sufficient delay to allow the A/D converter to set up the conversion result bits on the DO line before they are read by the microprocessor.

Software — ADC0831 Device

The following software listing provides the software routines for this A/D converter. The software is written as a subroutine so the designer can access the software quickly. An initial A/D clock cycle must occur before the eight subsequent clock cycles can be used to extract the conversion result bits from the A/D converter.



*Designer may see some spikes on the Data Output that do not effect the reading of the conversion results, since the microporcessor reads the DO pin after the spikes occur (see description of timing diagram).

Figure 11-119. Timing Diagram for the Intel 8048/49 to ADC0831 Interface

```
                                ; Software for Intel 8048/49 Interface to ADC0831
                                ;
                                ;
                                ;
        CALL S831               ; Load 9 clocks to CLK input on the A/D
                                ; chip & Acquire Conversion result
                                ; into Accumulator
                                ;
                                ; Subroutine S831
S831    ORL P1,#04H             ; Configure P1.2 as an input pin
        ANL P1,#FEH             ; Lower CLK
        ANL P1,#FDH             ; Lower Chip Select
        ORL P1,#01H             ; Raise CLK
        NOP                     ; Delay to slow CLK
        ANL P1,#FEH             ; Lower CLK
        MOV R0,#08H             ; Set bit counter to 8
S831I   ORL P1,#01H             ; Raise CLK
        NOP                     ; Delay to slow CLK
        ANL P1,#FEH             ; Lower CLK
        NOP                     ; To guarantee that occasional spikes on
                                ; DI/DO line at clock edges do not cause
                                ; erroneous readings
        CLR C                   ; Initialize C=0
        IN A,P1                 ; Get Port 1
        CPL A                   ; Complement Accumulator
        JB2 S831J               ; If 0831 Data out=1 ; BRANCH
        CPL C                   ; 0831 Data out=1 ; Set C=1
S831J   MOV A,R1                ; Get Serial Buffer
        RLC A                   ; Shift Data out Bit into Serial Buffer
        MOV R1,A                ; Store Serial Buffer
        DJNZ R0,S831I           ; Do 8 times
        ORL P1,#02H             ; Raise Chip Select
        MOV A,R1                ; Conversion Data is in Accumulator
        RET                     ;
        END                     ;
```

TL500, TL501, TL502, AND TL503 DEVICES APPLICATION EXAMPLES

The TL500 and TL501 devices are dual-slope A/D converters implemented with bipolar and MOSFET elements. These converters feature:

1. True differential inputs
2. Automatic zero
3. Automatic polarity
4. High input impedance: (10^9 Ω typically).

The major differences between the two devices are given in Table 11-37.

Table 11-37. Major Differences Between the TL500 and the TL501

	TL500	TL501
Resolution	14 bits (with TL502)	10-13 bits (with TL502)
Linearity Error	0.001%	0.01%
Readout Accuracy	4-1/2 Digits (with external ref.)	3-1/2 Digits

The TL502 and TL503 devices are digital processors, or control circuits, that contain an oscillator circuit and output devices. These are monolithic circuits using I^2L and bipolar techniques. These digital processing devices feature:

1. Fast display scan rates
2. Internal oscillator (free-running or driven)
3. Interdigit blanking
4. Overrange blanking
5. 4-1/2 digit display circuitry
6. High sink-current digit drivers.

The major differences between the two digital processors are given in Table 11-38.

Table 11-38. Major Differences Between the TL502 and the TL503

TL502	TL503
Compatible with Seven-Segment Common-Anode Displays	Multiplexed BCD Outputs
High Sink-Current Segment Driver for Large Displays	High Sink-Current BCD Outputs

The dual-slope technique used on the TL500 and TL501 devices results in a high degree of noise rejection due to input voltage integration. This means an expensive sample-and-hold circuit can be avoided, even when the input has a high noise content.

When compared to successive-approximation A/D converters, the speed of the dual-slope technique (less than 150 conversions per second) seems slow. However, this speed is generally adequate for most industrial applications such as temperature measurement or digital panel meters that depend upon the human eye for reading speed.

External Components Selection Guide

The proper selection of external components is required for the accurate and reliable operation of an A/D converter. These components are shown in Figure 11-120. Capacitors C_Z and C_R should be types with very low leakage; plastic foil capacitors are excellent. The capacitors should be at least 200 nF. A higher value should be used in 4-1/2 digit applications and circuits with low conversion speeds (one conversion per second). Capacitance of 1 μF is usually a suitable choice.

Ceramic or aluminum electrolytic capacitors should not be used because of their high leakage. This also applies when choosing C_X, particularly in 4-1/2 digit applications when a capacitor with very low dielectric loss should be used. Polypropylene capacitors are well suited to this application.

The value of resistor R_X should be in the range of 15 kΩ to 100 kΩ; a carbon film resistor would be suitable. The minimum RC time constant for the integrator can be calculated using the following equation:

$$TC = R_X \times C_X \times \frac{V_{EMAX} \times t_1}{(V_{OMAX}) - V_{CM}}$$

In the above equation, V_{EMAX} represents the maximum input voltage between pins 1 and 2. When using the TL502 or TL503 device, this value will be 200 mV. V_{OMAX} is the maximum output voltage of the integrator at pin 13. With a supply voltage of ± 12 V, this should be +8 V or −5 V. V_{CM} is the common-mode voltage between pin 2 and the analog ground as indicated in Figure 11-121.

If a differential input is not required, connecting pin 2 to analog ground will set V_{CM} to zero. The duration of the V_E integration phase is equal to t_1. When using the TL502 or TL503 device, t_1 can be calculated from the oscillation frequency:

$$t_1 = \frac{20{,}000}{f_{osc}}$$

Example: A value of 470 pF for C_{osc} results in a frequency of approximately 160 kHz. Thus, the period of t_1 is 125 ms. (The oscillator circuit is part of the logic control circuit in TL502 or TL503, and is discussed later.)

Resistor R_E and capacitor C_E are not strictly necessary to the operation of the converter as resistor R_E constitutes a protection circuit for the analog inputs. If the input voltages cannot be guaranteed to remain below the value of the supply voltage V_{CC}, then R_E should be included to limit the current which will flow through the TL500 and TL501 internal clamp diodes. The value of R_E should not exceed 100 kΩ.

Each analog input is connected through an analog switch to the high-impedance buffer or integrator inputs. These switches are MOSFET devices having fixed drain-gate capacitance. If the inputs to the switches are also high

impedance, then significant feed-through or interaction may occur between the switch control signals and the input voltages. Eventual converter errors can be avoided if the input impedance is decreased using capacitor C_E with a capacitance of 10 to 100 nF.

The reference voltage at pin 4, which is 100 mV for an input voltage range of 200 mV, may be derived from the internal reference voltage (REF OUT) through a voltage divider. The total resistance of the divider should be within the range of 1 kΩ to 10 kΩ. For applications that require high precision, a temperature-compensated reference voltage source is recommended. If the value of R_X is within the recommended range of 15 kΩ to 100 kΩ, the output impedance of the reference voltage source should not exceed 2 kΩ.

Supply voltages for the TL500 and TL501 devices may be selected within the range of 5 V to 18 V and −8 V to −18 V. Operation at voltages approaching the lower limits is not recommended and should only be considered for applications which do not require high resolution.

Both the common-mode range and the maximum output voltage of the integrator are approximately 3 V. In the case of 4-1/2 digit applications, a power supply of ±12 V minimum is recommended because of the eventual increase in the dynamic range of the integrator.

The analog and digital ground connections of the TL500 and TL501 devices are internally isolated from each other. The digital ground connection serves as a reference point for the A and B control inputs and the comparator output. The operation of the TL500 and TL501 devices is guaranteed if the potential of the digital ground is within the range of $-V_{CC}$ to $+V_{CC}$ minus 4 V.

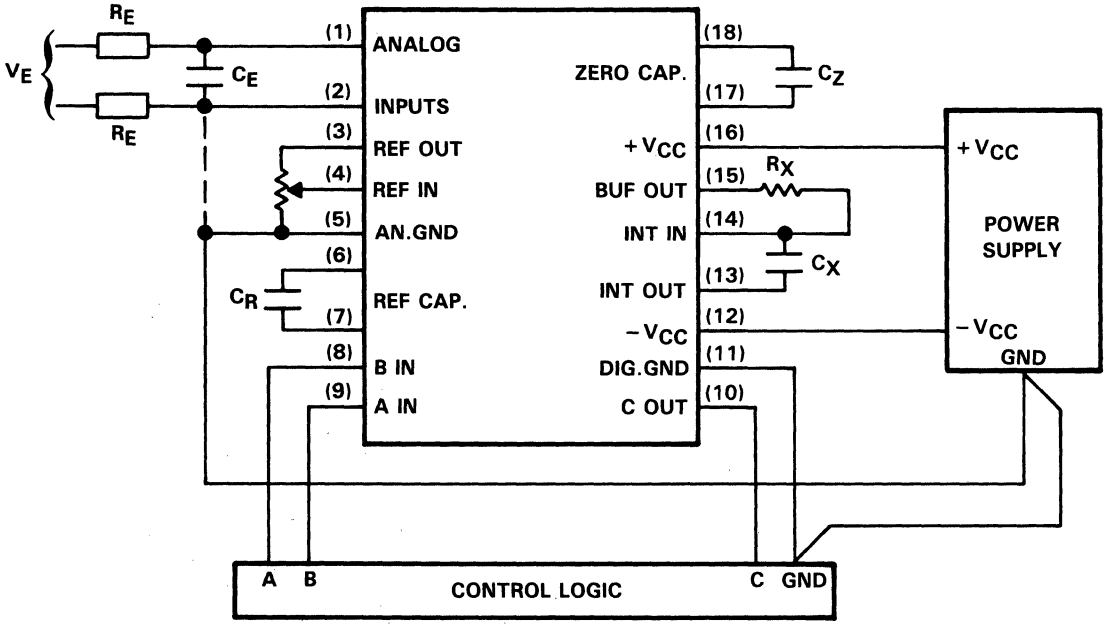
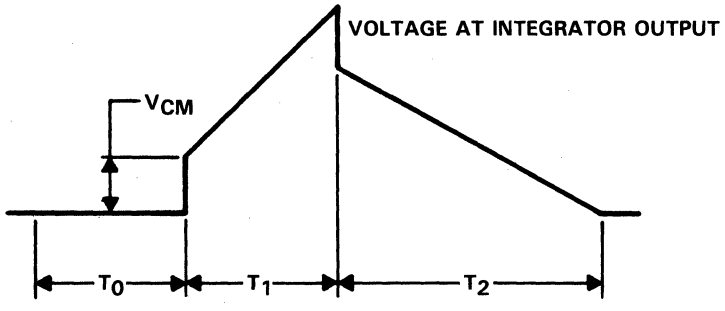


Figure 11-120. TL500/501 Wiring Diagram



V_{CM} = VOLTAGE BETWEEN ANALOG GROUND (PIN 5) AND ANALOG INPUT (PIN 2).

Figure 11-121. Example With Constant Common-Mode Voltage

Printed Circuit Board Layout Notes

When constructing an A/D circuit on a printed circuit board, the layout has a significant effect on accuracy. Coupling of the digital control signals to the analog components can often be the cause of unexplainable errors. The following points should be observed.

It is essential that the TL500 and TL501 supply voltages be adequately decoupled. Tantalum capacitors are recommended and should be located as close as possible to the device. The analog and digital grounds should be connected together at the power supply as illustrated in Figure 11-120. This ensures that no current from the digital circuitry can flow along the analog ground connections. The ground connection of the internal reference voltage-divider network or an external reference voltage should be connected directly to the analog ground pin of the TL500 and TL501 devices. The connections to C_R, C_Z, C_X, and R_X should be kept as short as possible and isolated from any digital control wiring.

TL502 and TL503 Control Circuits

The TL502 and TL503 contain not only the necessary logic to control the TL500 and TL501 A/D converters, but also have outputs for driving a 4-1/2 digit display in either the 7-segment or BCD code respectively. The TL502 and TL503 devices are also suitable for controlling the TL505 device.

Figure 11-122 shows the block diagram of the TL502 or TL503 device connected to a TL500 or TL501 A/D converter. The oscillator in the TL502 and TL503 can operate either as a free-running oscillator with an external capacitor connected between the oscillator input and digital ground or may be driven by an external TTL signal. The oscillation frequency when operating in the free-running mode is approximately 160 kHz with a 470 pF external capacitor. The TL502 and TL503 devices require 80,000 cycles from the oscillator for a complete conversion. If a 470 pF capacitor is used, the result is a conversion speed of about 2 measurements per second.

For 4-1/2 digit applications, an external oscillator is recommended. This oscillator should not have any short-term frequency variations, although long-term variations do not have a direct effect on the conversion result. To obtain a stable display, it is necessary to reject the power line frequency. It is desirable that the oscillation frequency be an even multiple of the power line frequency. The external oscillator should be synchronized.

The oscillation frequency range is approximately 10 kHz to 1 MHz. Below 10 kHz the display begins to flicker, and because of the long conversion time, this low frequency is not recommended. Above 1 MHz, reliable operation of the TL502 and TL503 devices is no longer guaranteed for all operating conditions. Higher conversion speeds can be achieved with the A/D converters if a fast TTL or microprocessor control is used.

Logic Inputs and Outputs

The TL502 and TL503 devices have two inputs, trigger and comparator, that can control a total of five different functions.

The conversion may be interrupted using the trigger input; a logic low (0) at the trigger input will cause the converter to stop at the beginning of the next Auto Zero phase. Under these conditions, logic outputs A and B are reset low and the previous conversion result is displayed. However, the internal operation of the device continues, and if the trigger input receives another high level, a new conversion begins with the next Auto Zero phase.

If the trigger input rises more than approximately 2.5 V above V_{CC}, the device enters a test mode in which the operation of the multiplexer is inhibited and all the segments or BCD outputs are activated. Certain decades of the main counter are bypassed relative to the digit output under control to accelerate the operation of the controller.

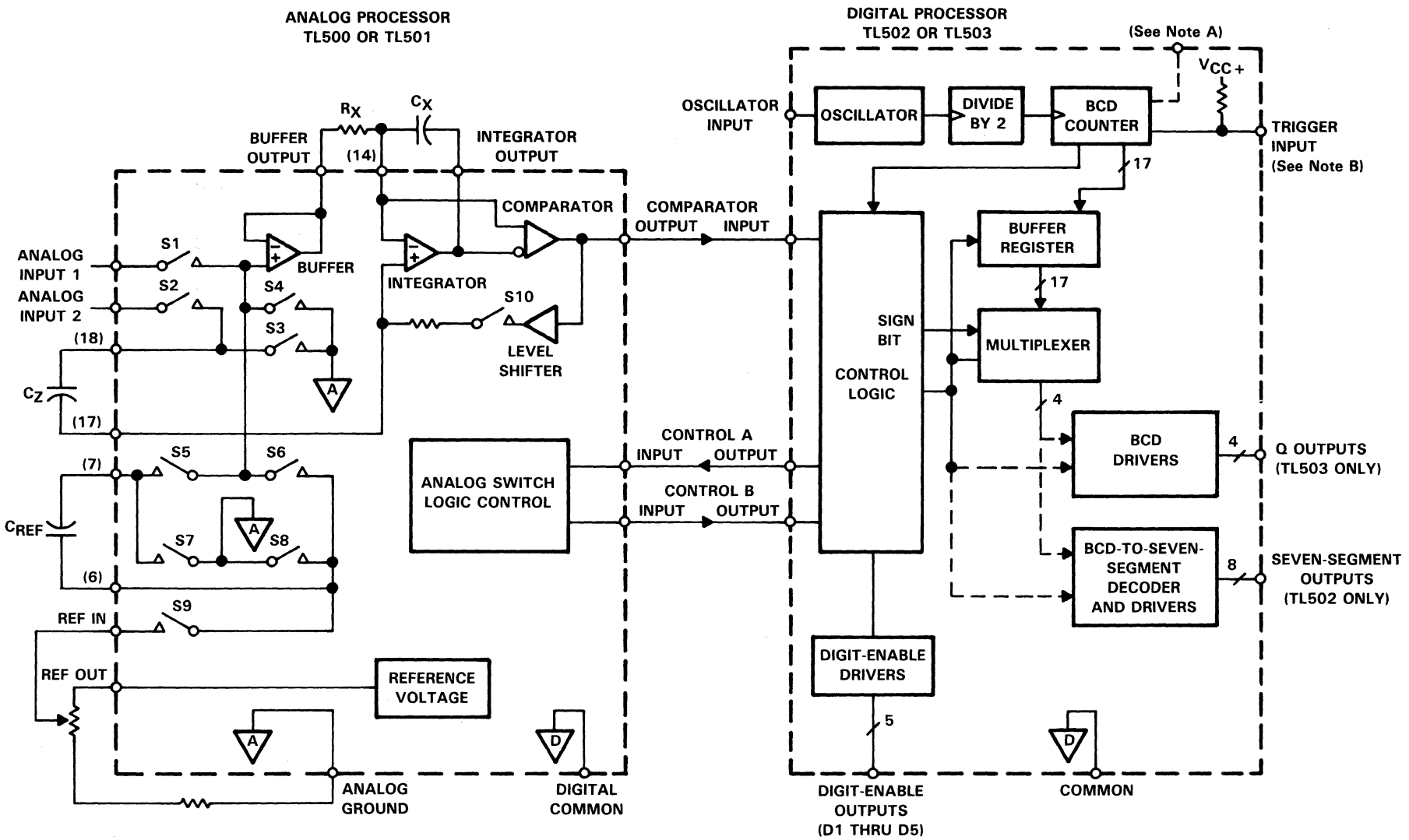
The comparator input receives information from the A/D converter regarding the polarity of the unknown voltage. This information determines whether the A or B output is set low in the following phase and when a positive or negative reference voltage is integrated. The control logic recognizes the end of the integration phase when the switching threshold of the comparator is crossed. The value from the main counter is then transferred to a register, and the A and B logic outputs are set low. Figure 11-123 shows a typical circuit with both comparator and trigger inputs.

If the comparator input rises more than approximately 2.5 V above V_{CC}, a display test begins but the control logic continues to operate. However, normal conversion is not guaranteed in this case because comparator information cannot be communicated.

If signals are applied simultaneously to both the trigger and comparator inputs, the logic is reset. When this mode ends, control begins again with the start of the next Auto Zero phase; until then, the outputs display 19999.

The TL502 device has an oscillator output that is labelled 20,000. The frequency of this output is the oscillator frequency divided by a factor of 20,000 and has a mark-space ratio of 1:4. This output is suitable for controlling a phase locked loop (PLL) circuit so the oscillator frequency is locked to an even multiple of the line frequency. Figure 11-124 shows the block diagram of a typical PLL circuit. This type of circuit is recommended when a stable display is required at relatively high conversion rates that will remain stable, even when the input voltage has superimposed line frequency hum.

The A and B outputs, as well as the 20,000 oscillator output, have internal pull-up resistors; therefore, they are TTL compatible and the A and B outputs can be connected directly to the relevant inputs of the TL500 and TL501 devices.



NOTES: A. Pin 18 of the TL502 provides an output of f_{osc} (oscillator frequency) ÷ 20,000.
B. The trigger input assumes a high level if not externally connected.

Figure 11-122. Block Diagram of Basic Analog-to-Digital Converter Using TL500C or TL501C and TL502C or TL503C

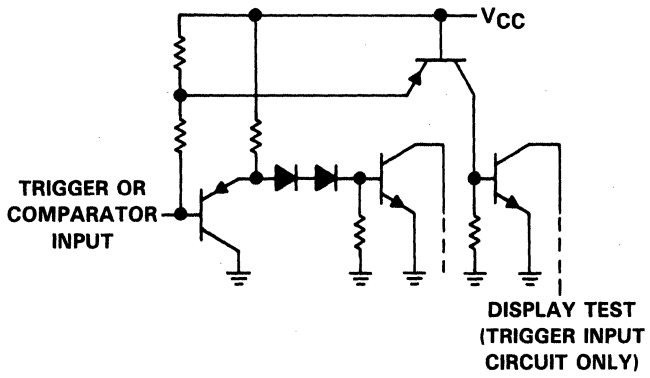


Figure 11-123. Typical of Both Comparator and Trigger Input Circuits

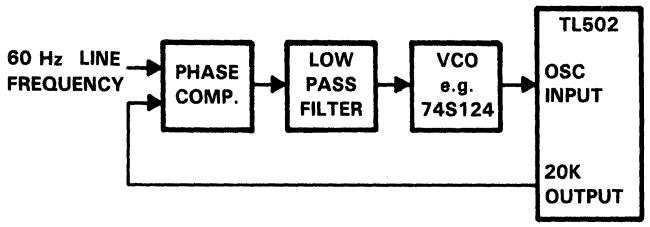


Figure 11-124. Synchronization of the Oscillator Frequency

Driving a Display Using the TL502 Device

The TL502 device can drive up to a 4-1/2 digit display in a multiplexed mode. This has the advantage of minimizing the device outputs required and also simplifies the PC board layout.

In most simple applications, the display will consist of 7-segment, common-anode LEDs. Because the I^2L technology does not permit the manufacture of suitable PNP drive transistors, it is necessary to use external drive transistors to drive each digit anode. The display cathodes are connected by a current-limiting resistance R_V to the relevant segment output shown in Figure 11-125.

Calculation of the Current-Limiting Resistor

The segment current and the brightness of the display are set by resistor R_V. From Figure 11-125, the voltage drop across R_V is:

$$V_{RV} = V_{CC} - V_F - V_{CEsat} - V_{OL}$$

$$= 5\ V - 1.7\ V - 2 \times 0.2\ V$$

$$= 2.9\ V$$

As indicated in the segment current waveform in Figure 11-126, each digit is active for 19% of the time. If the display requires an average segment current of 15 mA to achieve a specific brightness, the peak current (I_P) can be calculated by the equation:

$$I_P = \frac{15\ mA}{19\%}$$

$$= \text{approx. } 80\ mA$$

and R_V can be calculated by:

$$R_V = \frac{V_{RV}}{I_P}$$

$$= \frac{2.9\ V}{80\ mA}$$

$$= \text{approx. } 36\ \Omega$$

In practice, a value of 39 Ω would be chosen because it is the next higher standard value. A power rating of 1/4 W is adequate.

Application of the TL503 BCD Outputs

The outputs of the TL503 device correspond to the multiplexer timing diagram in Figure 11-126. The clock time of the multiplexer is 200 x ($1/f_{osc}$). The digital outputs are active low. The BCD outputs are the open-collector type and are active high.

If the conversion results are recorded by a microprocessor, the following procedure may be used. The trigger input must be low prior to conversion. When the controlling program requires a new conversion, a logic high signal is directed to the trigger input for a period of not less than 2000 x ($1/f_{osc}$) and the A/D converter immediately starts a conversion. When period t satisfies the condition shown below

$$2000 \times (1/f_{osc}) < t < 40{,}000 \times (1/f_{osc}),$$

the microcomputer awaits an end of conversion signal. This signal is processed from the A and B control signals by a NOR gate. After this signal has been received, the new result may be used.

The actual data transmission is synchronized using the digital outputs with each digit triggering a different interrupt.

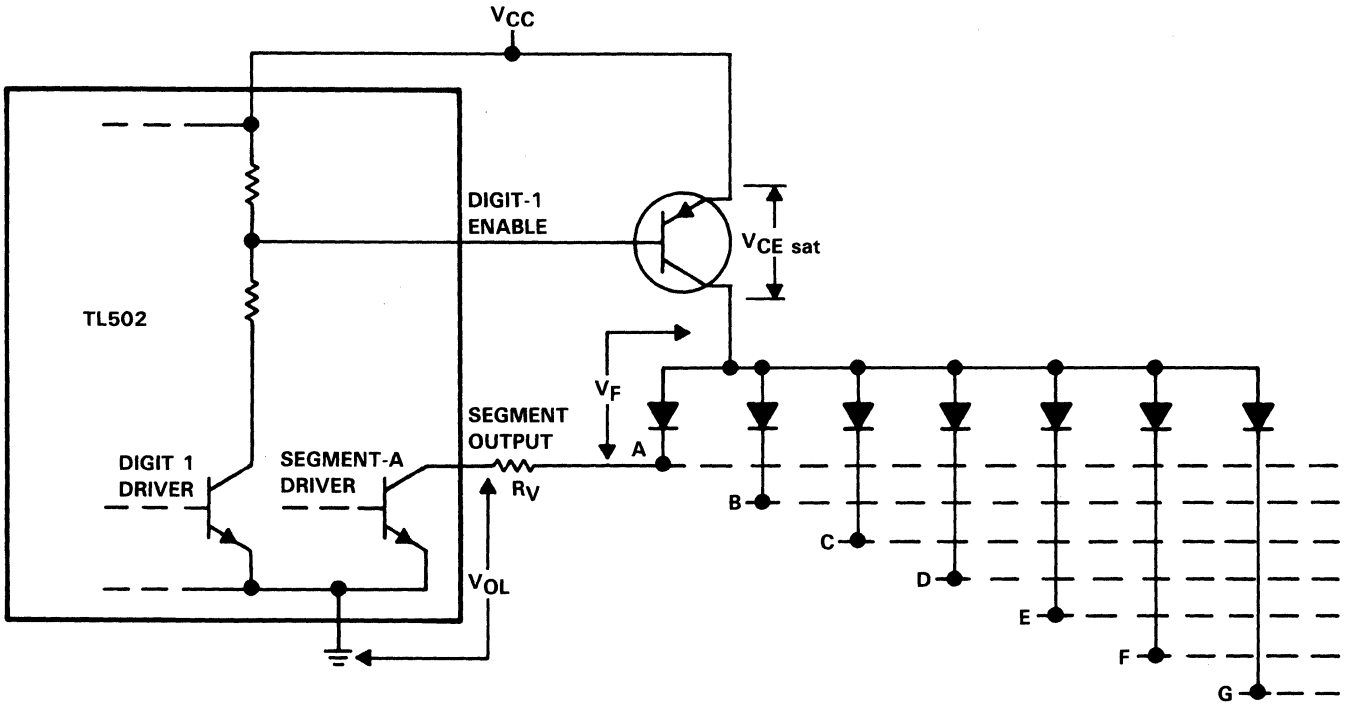


Figure 11-125. Display Driving

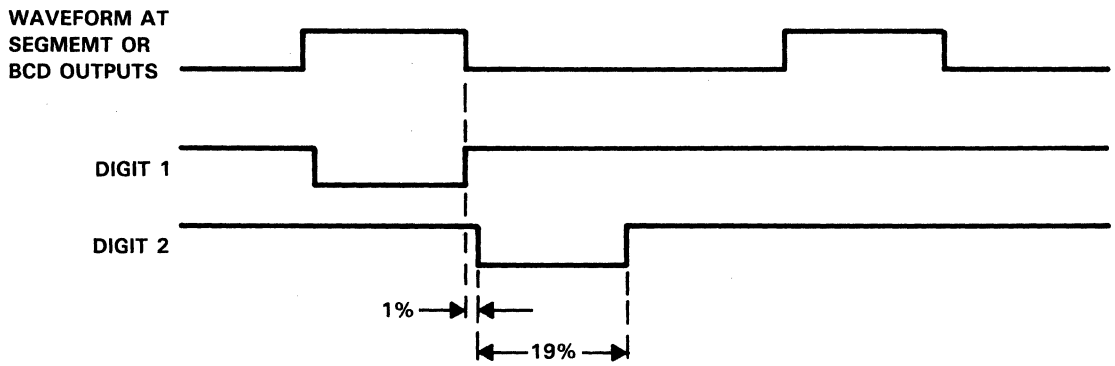


Figure 11-126. Multiplexer Timing Diagram

This guarantees the integrity of the BCD information. The minimum time required for a complete transfer, therefore, corresponds to the duration of the multiplexer period. This time can be decreased if two or more bits of digital information are combined. It is possible to combine all 18 bits using the demultiplexer shown in Figure 11-127. The BCD information from each digit is transmitted to the quadruple D-type flip-flop using the negative edge of the digital outputs. Figure 11-126 indicates that this negative edge is available after a time delay of two clock cycles. If required, the inputs to the flip-flops may be inhibited during the read process by using the enable inputs.

Digital Panel Meter Using the TL501 and TL502 Devices

The input voltage range of the digital panel meter shown in Figure 11-128 is ±2.0 V and when using the component values shown, a conversion rate of approximately 2 conversions per second is produced. Other conversion rates can be achieved by using different size capacitors for C_O and C_X. Pins 2 and 5 on the TL501 device may be jumpered together when no common-mode input voltage exists. The equation for selecting values for R_X and C_X is given in the External Components Selection Guide section. When necessary, an RC time constant protection network may be connected to the input.

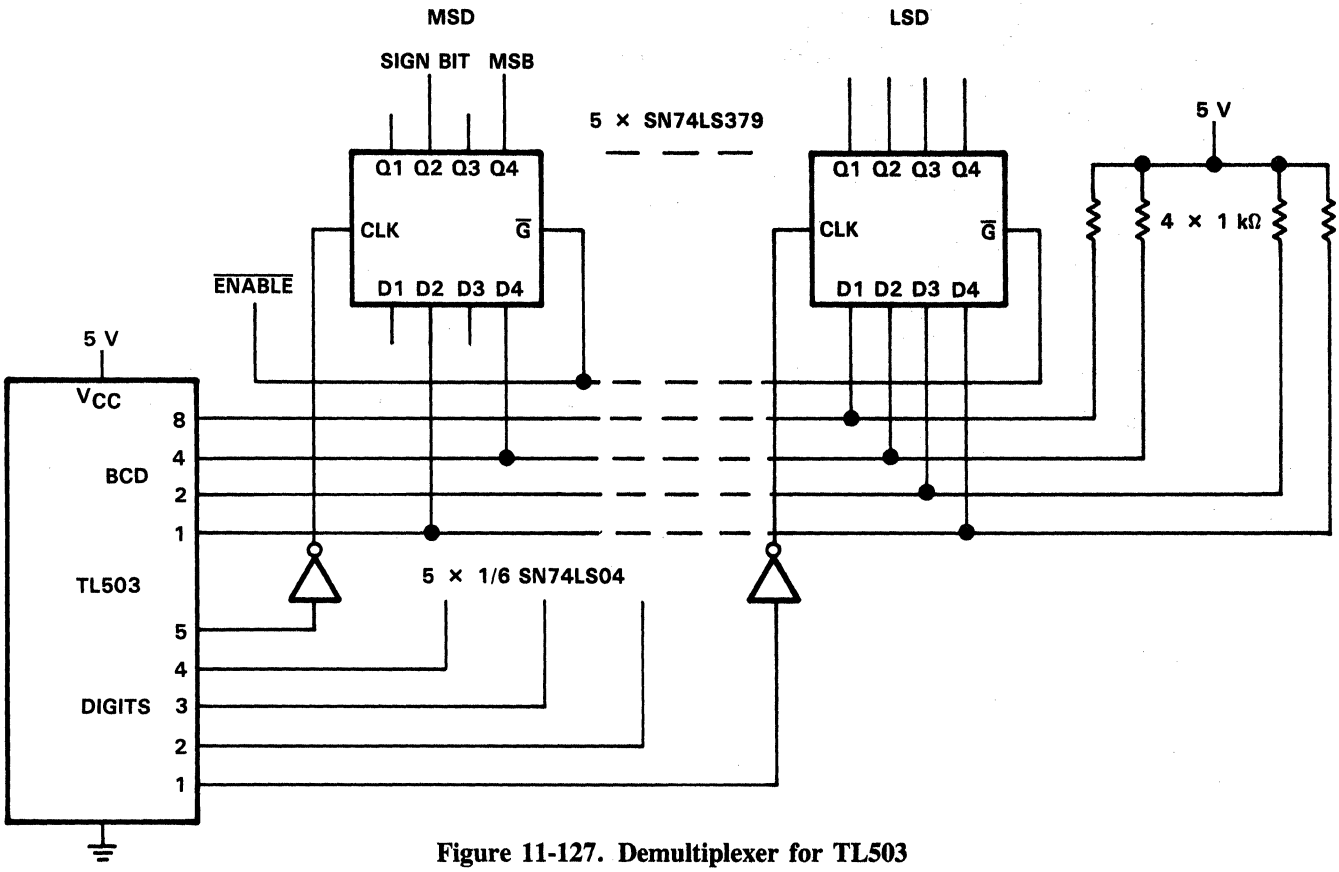


Figure 11-127. Demultiplexer for TL503

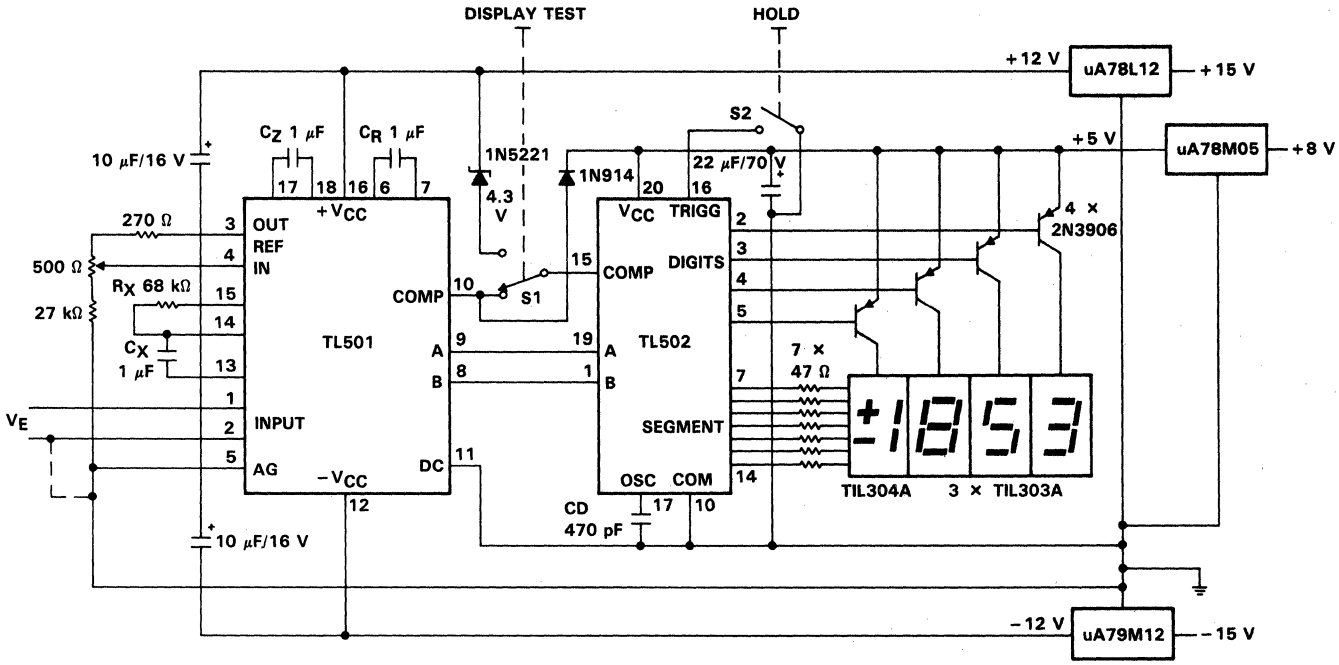


Figure 11-128. Digital Panel Meter Using TL501

Note that the recommended use of separate grounds is shown in Figure 11-128. It is essential that the analog and digital grounds be connected only at the power supply.

Switch S1 provides a means of activating the display test mode. The required 7.5-V supply is provided from the 12 V line using a 1N5221 zener diode to provide a 4.3-V drop. A changeover switch is required because the comparator output of the TL501 device is not short circuit protected. Remember that after a display test, the display contains an invalid result.

By operating the HOLD switch, S2, conversion results can be stored or readings can be manually observed. The different pin-out of the TIL304A device (sign and MSB digits) means that pins 1 and 14 must be connected to the digit driver. Pin 7 connects to the limiting resistor of segment E or F and pin 8 connects to the limiting resistor of segment G.

Digital Thermometer

The digital thermometer diagram shown in Figure 11-129 is an application that uses the differential inputs of the TL500 or TL501 device to measure a voltage from a bridge circuit. When the circuit is calibrated, the voltage that represents an actual temperature is indicated on the LED readout.

The temperature sensor is a silicon thermistor with a positive temperature coefficient and a low time constant (less than 1.5 seconds). Excluding linearity of the sensor, the linearity error of the circuit is less than 0.5% over the temperature range of $-55\,°C$ to $+125\,°C$.

The calibration of the circuit is straightforward. First, potentiometer P0 is adjusted for the zero point. This is accomplished by adjusting P0 to a preset voltage of 0.258 x V_{REF} V (approximately 0.31 V) at the wiper of P0. Second, the thermometer is calibrated by applying a known temperature to the thermistor and adjusting potentiometer P1 for about 0.153 x V_{REF} V (approximatley 0.19 V) at the wiper of P1.

The decimal point is fixed between digits 2 and 3 by connecting the relevant cathode of the display to digital ground through a 56-Ω resistor.

Precision Panel Meter Application

Figure 11-130 shows a 4-1/2 digit precision panel meter using the TL500 and TL502 devices. The input voltage range is ±200 mV. This means that current measurements are possible with only an additional shunt resistor.

The use of a precision reference voltage source is recommended so the circuit may be used over a wide temperature range. The 100 mV reference voltage is obtained from a TL431 shunt regulator and a voltage divider comprised of a 250-Ω cermet trimmer potentiometer and a 2500-Ω metal film resistor. No allowance has been made for a common-mode input voltage. If this is required, the connection from pin 2 to pin 5 should be opened and a larger capacitor inserted.

The TL502 device is controlled by a NE555 external oscillator. Its frequency is adjusted to an even multiple of the power line frequency to guarantee a high degree of power line frequency suppression.

The latch, implemented with an SN74LS02 device, increases the performance of the circuit at input voltages of almost zero. If the input voltage is very low, the integrator of the TL500 device can only produce a small ramp signal. In this case, low-level interfering signals are sufficient to cause an incorrect comparator switching sequence. This result is especially noticeable during the switch-over from the up-integration phase to the down-integration phase. The comparator signal, delayed by one-half of a clock cycle, is directed to the control logic through the latch. Thus, interference impulses caused by crosstalk from the A and B control signals no longer have any influence on the comparator input.

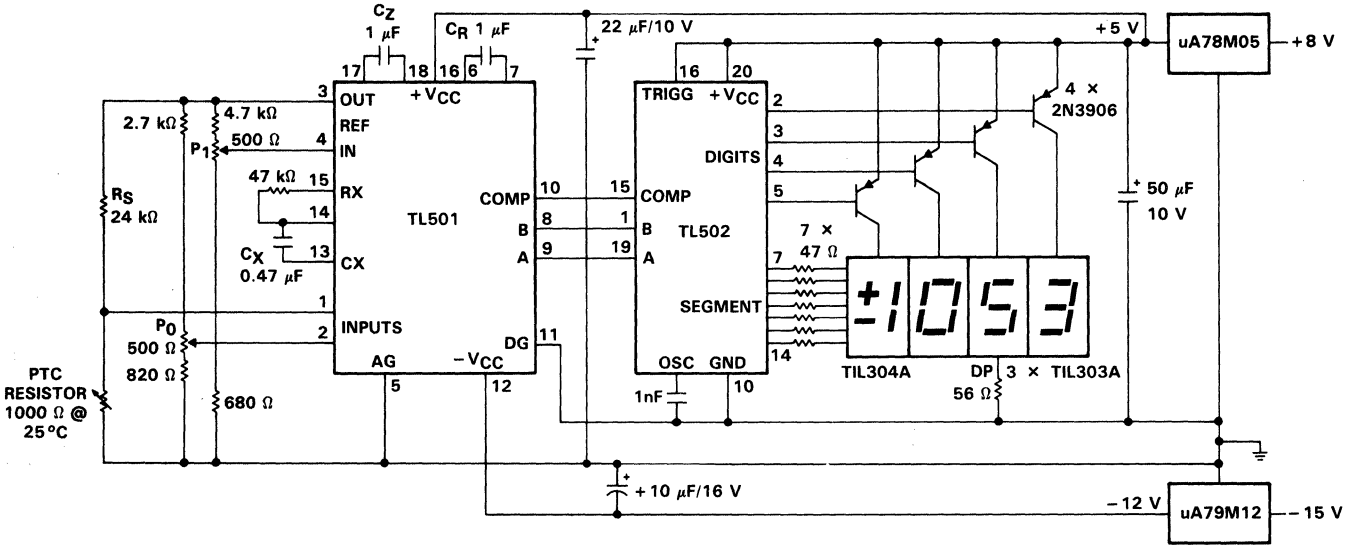


Figure 11-129. Digital Thermometer

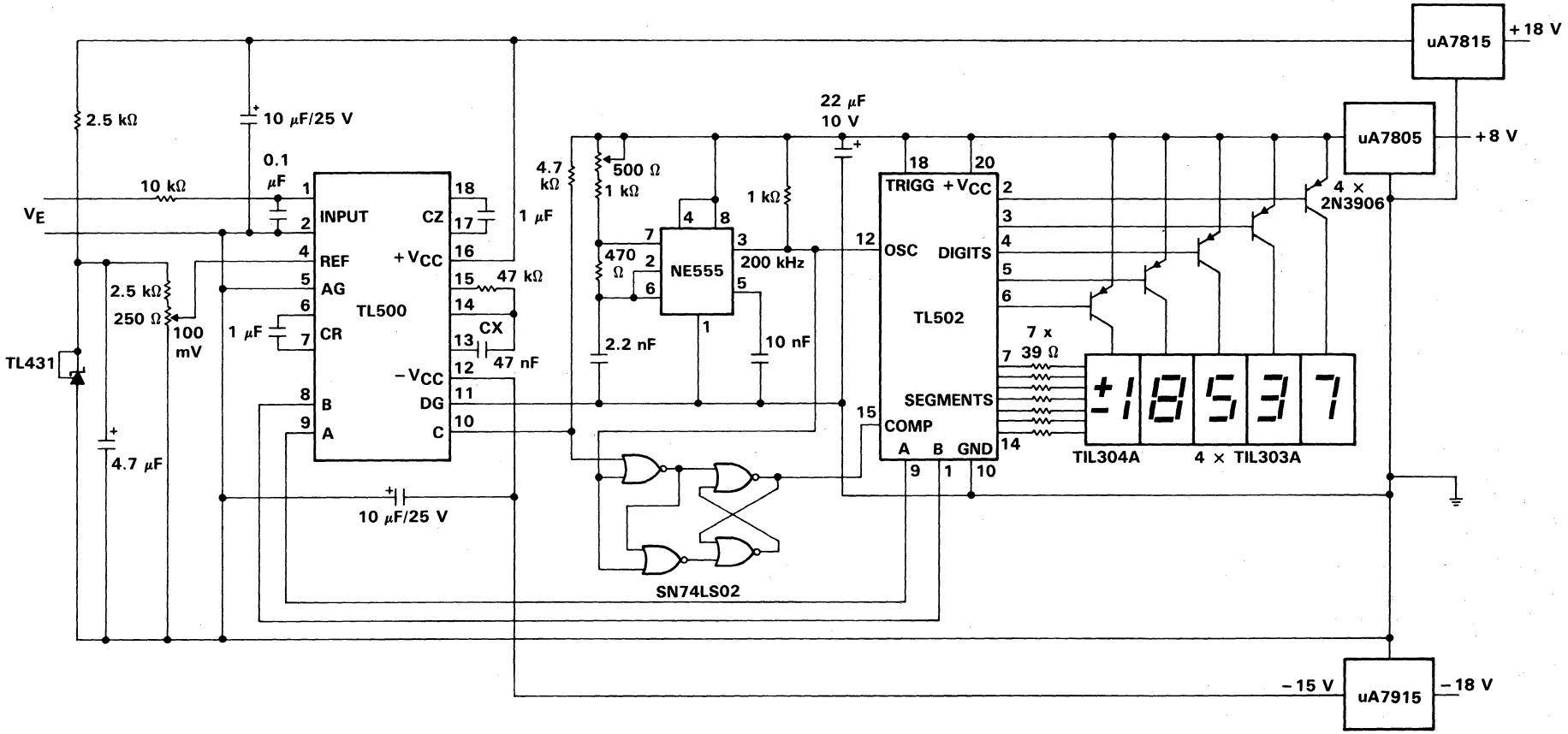


Figure 11-130. Precision Panel Meter

The suggested display is composed of four TIL303A devices and a single TIL304A device. When connecting the TIL304A device, the minus sign should be connected to segment outputs A and D. All other connections are identical to the TIL303A device.

TL505 A/D CONVERTER APPLICATIONS

The TL505 device is a dual-slope A/D converter with 10-bit resolution and 3-digit accuracy. It has a high-impedance MOSFET input. It was developed for use with a microcomputer, but can be used in combination with discrete control logic such as the TL502 or TL503 devices. The TL505 device requires only a single supply voltage in the 7- to 15-V range.

Functional Description

Figure 11-131 shows a simplified functional circuit diagram of the TL505 device. The dual-slope principle has already been described using the TL500 device; therefore, only the functional differences of the TL505 device will be described. Figure 11-132 describes the function of the A and B control inputs of the TL505 device with reference to the switches in Figure 11-131.

The TL505 device, like the TL500 device, starts a conversion during the Auto Zero phase when all offset error voltages are stored on capacitors C_X and C_Z. However, the operation of the TL505 device differs from the TL500 device in the integration phase that follows the Auto Zero phase. During the integration phase, operational amplifier A1 functions as a noninverting integrator. The input voltage is

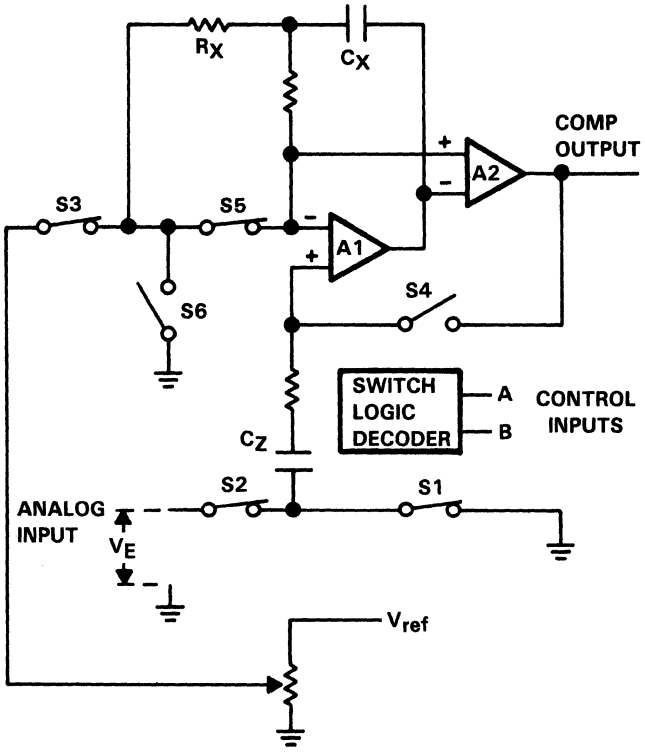


Figure 11-131. Functional Circuit Diagram for the TL505

CONTROL INPUTS		SWITCHES CLOSED	FUNCTION
A	B		
0	0	1,4,5,6	Auto Zero
0	1	1,3	Integration of reference voltage
1	0	1	Hold
1	1	2,4	Integration of input voltage

Figure 11-132. Function of the A and B Control Inputs of the TL505

switched through S2 and C_Z to the high-impedance input; therefore, an additional buffer stage is not required. In the following down-integration phase, A1 is used as an inverting integrator. A positive reference voltage is connected to the input through S3 so that a negative-going waveform appears at the output. This phase lasts until the switching threshold of the comparator A2 is reached and the control supplies a logic low signal to both the A and B inputs of the TL505 device. Figure 11-133 shows the conversion process timing diagram and its function table.

External Component Selection Guide

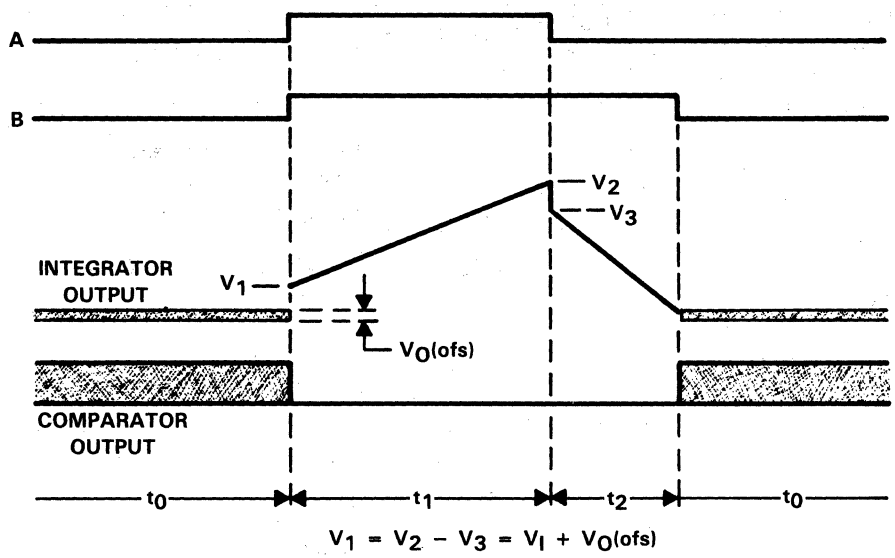
The suggestions given on component selection for the TL500 and TL501 circuits are also valid for the TL505 A/D converter. Figure 11-134 shows the TL505 device wiring diagram. Capacitor C_Z must be a low-leakage type with a minimum capacitance of 150 nF. Capacitor C_X must also be a low-leakage type. Ceramic or electrolytic capacitors should not be used. Resistance R_X is not critical and a carbon film resistor in the range of 0.5 to 2.0 MΩ is adequate. The value of capacitor C_X may be calculated using the following formula:

$$C_X \geq \frac{V_{EMAX} \times t_1}{R_X(V_{CC} - V_{EMAX} - 2\ V)}$$

V_{EMAX} is the maximum input voltage and a value of 2 V should be assumed if the TL502 or TL503 devices are used as the control logic. For safe operation, the maximum input voltage must not exceed 4 V when the TL505 device is used in other applications not involving the TL502 and TL503 devices. The factor ($V_{CC} - V_{EMAX} - 2$ V) represents the maximum voltage variation at the integrator output and time t_1 represents the duration of the V_E integration phase. The internal resistance of the reference voltage source connected to pin 4 should be as low as possible because this resistance will influence the conversion result due to the operation of the TL505 device.

If the value of R_X lies within the range of 0.5 to 2.0 MΩ, the output impedance of the reference voltage source should not exceed 2 kΩ. In most cases when the TL502 or TL503 device is used as the control logic, a reference voltage will be 1 V and the total resistance of the reference voltage divider must not exceed 10 kΩ.

Resistor R_E and capacitor C_E constitute a protection circuit for the input similar to the TL500 and TL501 devices.



FUNCTION TABLE

CONTROLS		ANALOG
A	B	SWITCHES CLOSED
L	L	S1, 4, 5, 6
H	H	S2, 4
L	H	S1, 3

H = V_{IH}, L = V_{IL}

Figure 11-133. Conversion Process Timing Diagrams

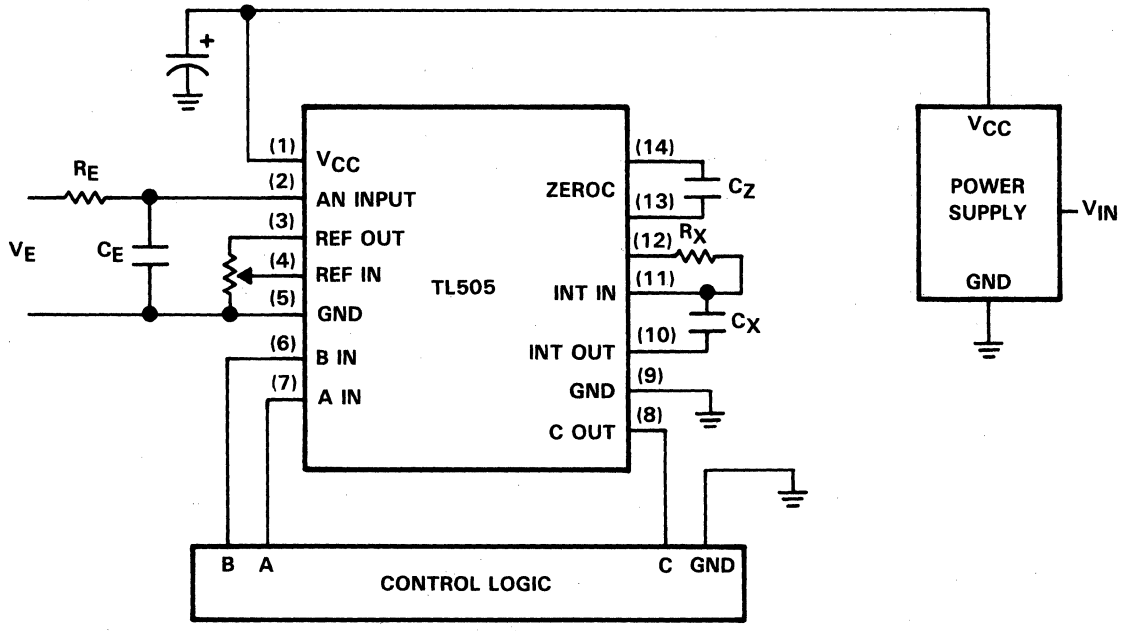


Figure 11-134. TL505 Wiring Diagram

It should be noted that the logic inputs of the TL505 device are not TTL compatible. Figure 11-135 shows a simple interface circuit which should be used with the TL505, TL502, and TL503 device combination.

Digital Panel Meter Using the TL505 and TL502 Devices

A typical application of the TL505 device is given in Figure 11-136 and shows a digital panel meter for positive input voltages. The single-point ground method is the best way to ensure acceptable results.

The values shown are for a maximum input voltage of 2 V and a conversion rate of approximately 2.5 conversions per second. The RC time constant circuit protection network connected to the input is optional. The

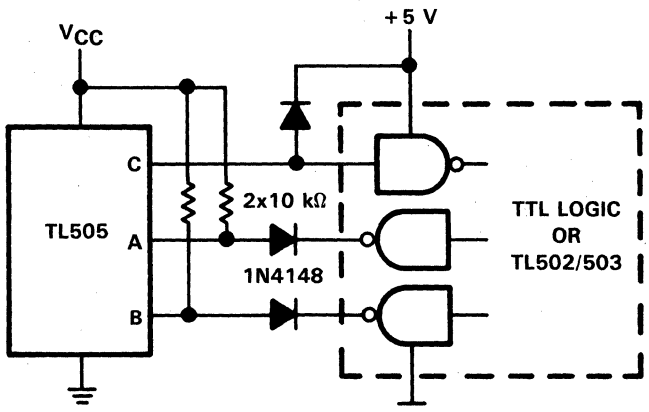


Figure 11-135. TL505C — TTL Interface

diodes in the A and B control lines ensure that the input voltage limits on the A and B inputs of the TL505 device are not exceeded. The diode at the comparator input of the TL502 device prevents any spurious initiation of the display test mode.

TL505 to TMS1000 Interface

Figure 11-137 shows an application of a TL505 device to TMS1000 device series interface. The microcomputer may be any one of the TMS1000 series requiring a 15-V power supply. A 6.8-V zener diode is used as an interface between the comparator output and the TMS1000 input. This results in the minimum possible standing current in the low state while maintaining a high noise immunity in the high state. The two 1N914 diodes prevent the TL505 device inputs from going below 0.2 V and may be omitted when using the TL505A device. The 2N2222 transistor pulls the inputs of the TMS1000 low during the start period.

The selection of external components for the TL505 device is dependent on the required input voltage range. The calculations are shown in the data sheet.

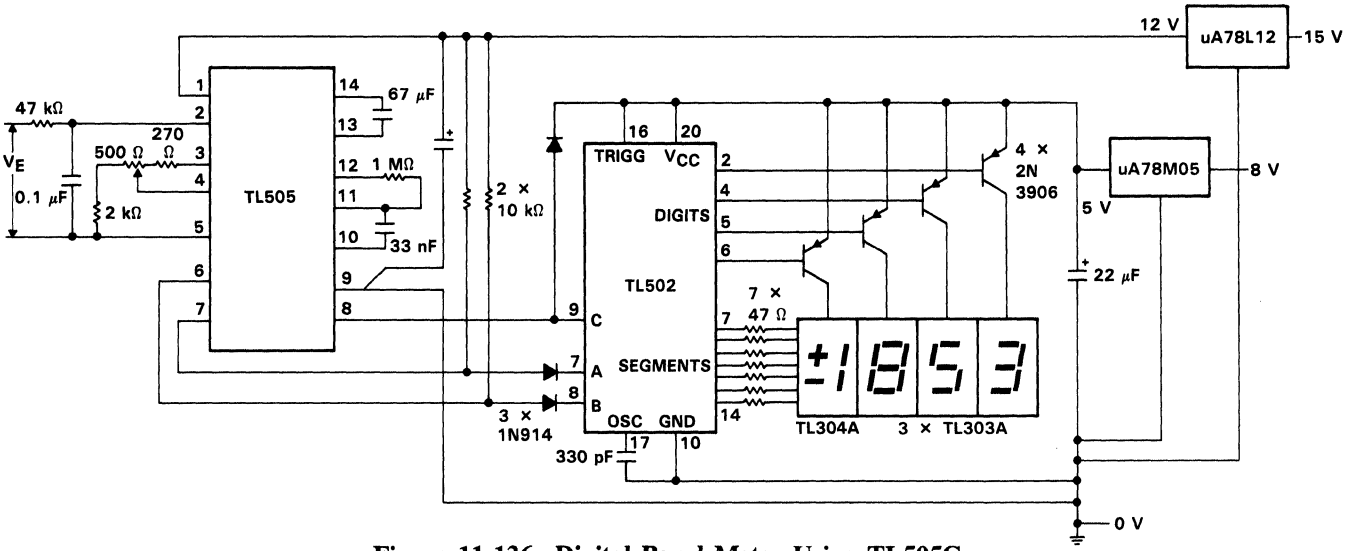


Figure 11-136. Digital Panel Meter Using TL505C

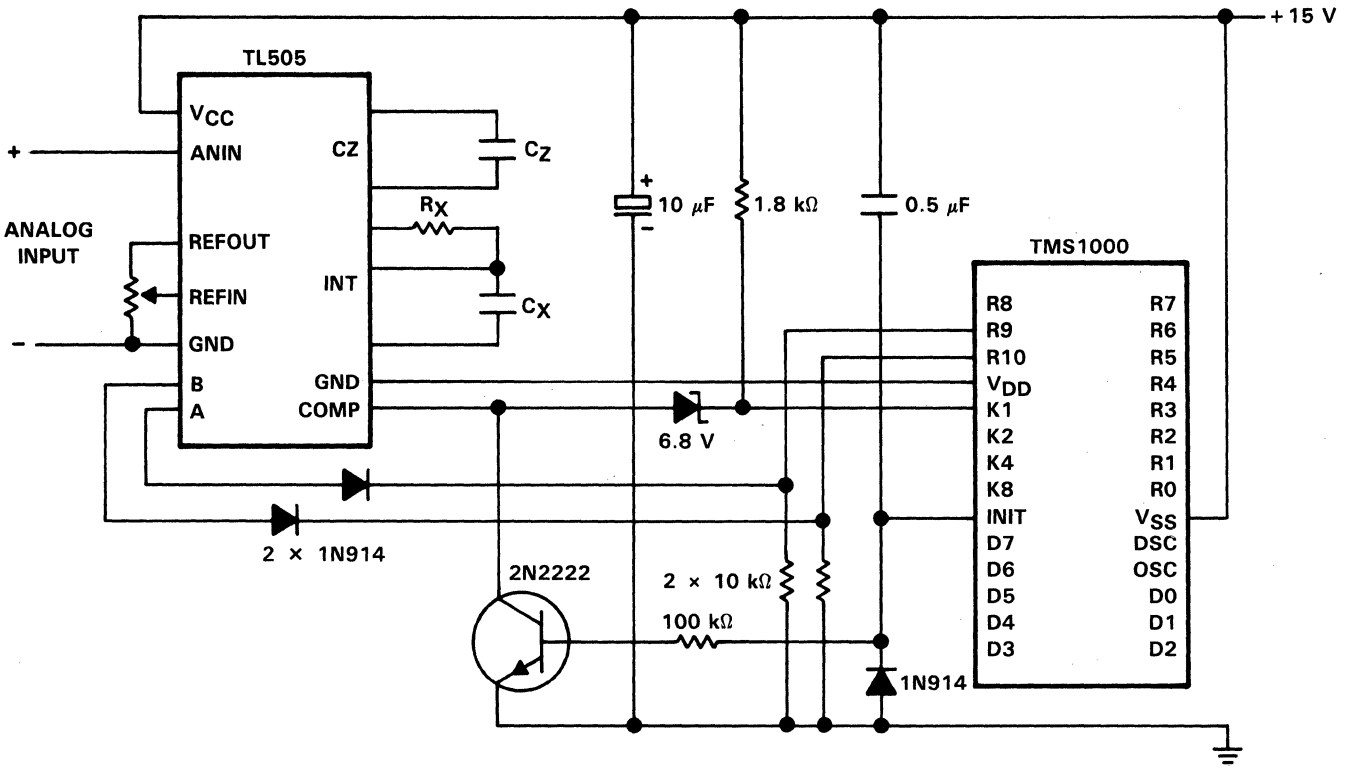


Figure 11-137. TL505C — TMS1000 Interface

TL507 A/D CONVERTER APPLICATIONS

TL507 Device Description

The TL507 device is a low-cost single-slope A/D converter which converts analog input voltages into a pulse-width-modulated (PWM) output code. In other words, the TL507 device is a voltage or current-to-time converter and the user can select the time reference by selection of the clock frequency. The operation of the TL507 device is explained with the block diagram in Figure 11-138 and the timing diagram in Figure 11-139.

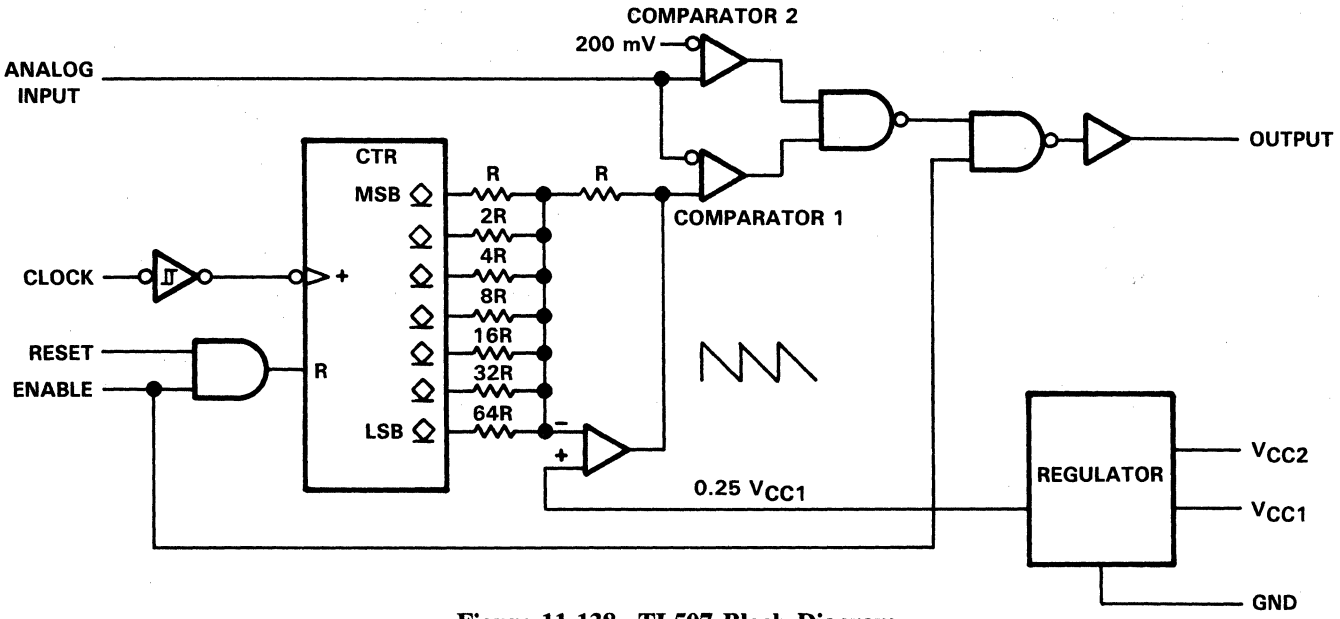


Figure 11-138. TL507 Block Diagram

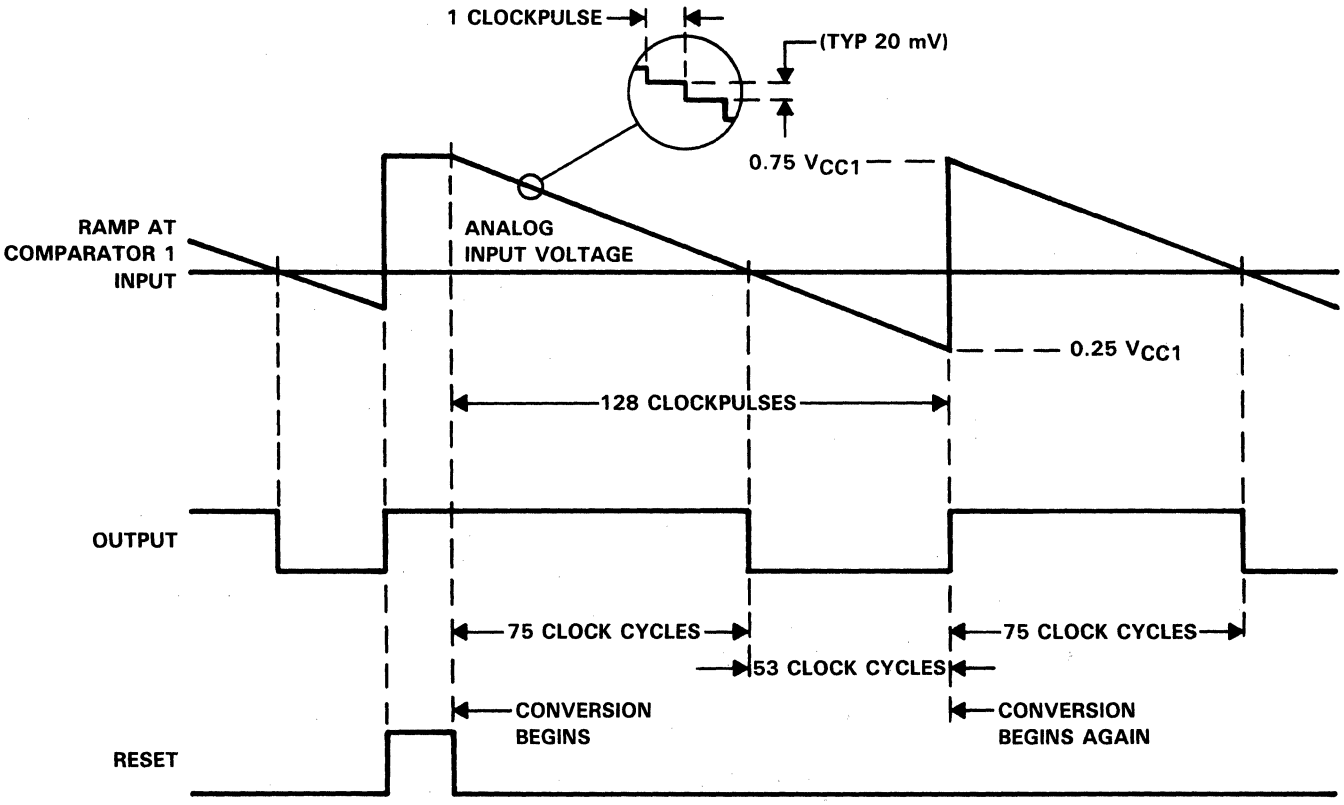


Figure 11-139. TL507 Timing Diagram

The internal 7-bit counter drives a binary-weighted resistor network to produce a monotonically negative-going ramp as the circuit is clocked. Comparator 1 compares the analog input voltage with the ramp and produces a low state at the output when the ramp voltage is less than the analog input voltage. This function happens when the enable input is high and the reset input is low.

The reset and enable inputs are inputs to an AND gate and are TTL voltage-level compatible. When the reset and enable inputs are at a high level, the counter is reset and the ramp is at its maximum value (0.75 V_{CC1}). When the reset input pin goes low, the TL507 device starts the A/D conversion cycle.

A conversion can begin by taking the reset input low or by clocking the circuit after the end of the previous conversion cycle as shown in Figure 11-139. The ramp input to the comparator is always at its highest voltage at the beginning of a conversion and the TL507 device output is high. The ramp voltage decreases with each succeeding clock cycle and the TL507 device output remains high until the ramp voltage becomes less than the analog input voltage; then, the output goes low. Thus, the number of clock cycles that occur during the period when the TL507 device output is low is directly proportional to the analog input voltage. A convenient method for obtaining a clock count, which is directly proportional to the analog input voltage, can be obtained with the simple NOR gate circuit in Figure 11-140.

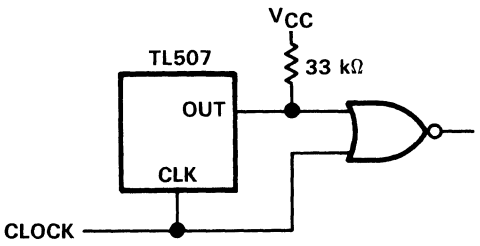


Figure 11-140. Circuit for Obtaining Clock Count Proportional to the Analog Input Voltage

The lower limit of the ramp is set by an internal voltage divider at 0.25 V_{CC1}. This lower limit corresponds to the highest possible count which is $2^7 - 1 = 127$. Since the counter outputs are open-collector transistors that are off at the highest count, no current flows through the binary-weighted resistor network. Thus, the output of the operational amplifier is equal to the voltage (0.25 V_{CC1}) at its positive input. The upper limit of the ramp corresponds to a count of zero when the binary-weighted resistor network is grounded. The output of the operational amplifier is calculated as follows:

$$V_{RAMPmax} = 0.25\ V_{CC1}\ (1 + R\ [1/R + - - - 1/64R])$$

$$\approx 0.75\ V_{CC1}$$

The counter is decreased by one least significant bit for each clock pulse; thus, the ramp voltage decreases by $V_{CC1}/256$ as illustrated in Figure 11-139 and as calculated below:

$$\Delta V_{RAMP} = 0.25\ V_{CC1}\ (R)\ (1/64R)$$

$$= \frac{V_{CC1}}{256} \approx 20\ \text{mV, typically.}$$

The input voltage, as illustrated in Figure 11-139, resulted in the device output being low for 53 clock cycles. The value of this input voltage is therefore

$$V_{IN} = \frac{\text{low clock count}}{\text{total clock count}} \times \frac{V_{CC1}}{2}$$

(where $V_{CC1} = 5$ V)

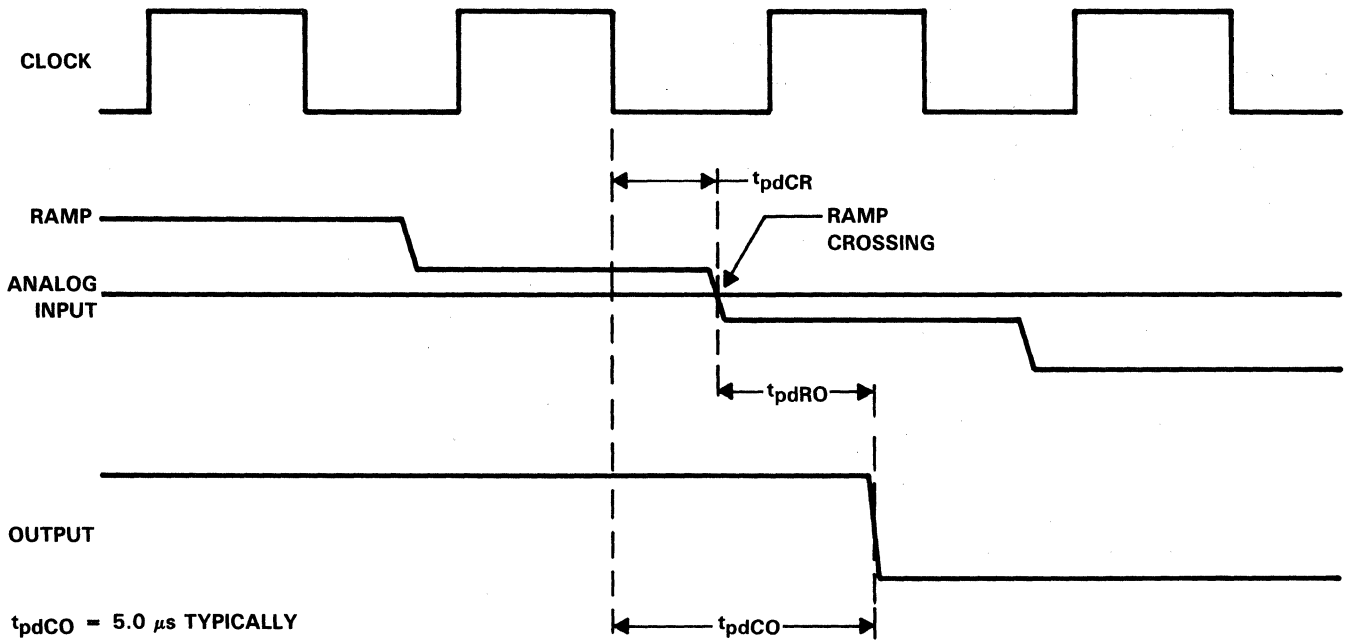
$$= \frac{53}{128} \times 2.5\ \text{V} \approx 1\ \text{V.}$$

TL507 Device Inputs and Outputs

When the enable input, pin 1, is held low, the TL507 device output is forced high regardless of all other input states. Since the TL507 device output is an open-collector transistor, multiple TL507 outputs can be wire ORed together, and the enable input functions as a multiplexer. When the enable input of one of the wire ORed TL507s goes high, the circuit performs the conversion operation and only its output controls the bus. The enable input is TTL compatible and is active high.

The clock input, pin 2, is connected to the counter input through a Schmitt-trigger gate that provides a large amount of hysteresis for noise immunity; therefore, the clock input can accept inputs with slow rise and fall times. Because of the hysteresis, the clock input is not compatible with TTL voltage levels and a pull-up resistor of approximately 4.7 kΩ must be used when this input is driven from a TTL output. The counter is clocked on the negative edge of the clock waveform as shown in Figure 11-141. The propagation delay time t_{pdCO}, as illustrated in Figure 11-141, is from the clock's negative edge to an output level change and is made up of two parts. One is the shift register delay (t_{pdCR}) and is from the clock input's negative edge to the analog input-ramp voltage crossing. The other (t_{pdRO}) is from the analog input-ramp voltage crossing to the output changing state. Although t_{pdRO} is a fixed value of about 3 μs, the value of t_{pdCR} may vary, depending on the value of the analog input voltage, from 1 μs to about 3 μs. Total delay, $t_{pdCO} = t_{pdCR} + t_{pdRO}$, must be less than one clock period. The recommended operating clock frequency is 125 kHz for an 8 μs time period. The maximum recommended clock frequency of 150 kHz yields a 6.67 μs time period.

The TL507 output at pin 4 is an open-collector transistor, and it must be pulled up with a suitable resistor determined by the load current and voltage requirements. The typical output characteristic of the TL507 device is shown in Figure 11-142 to aid in selecting the pull-up resistor



t_{pdCR} = Delay from the negative clock edge to the ramp crossing.
t_{pdRO} = Delay from the analog input-ramp crossing to the output changing state.
t_{pdCO} = Total delay time from the negative clock edge to the output changing state.

Figure 11-141. Typical TL507 Propagation Delay

value. Although the output acts like a current source at loads of about 4 mA, this characteristic should not be used to limit the output current when driving a low impedance load such as an optical coupler input diode. Also, the low state voltage should not exceed 5.5 V to keep from exceeding the power dissipation limits.

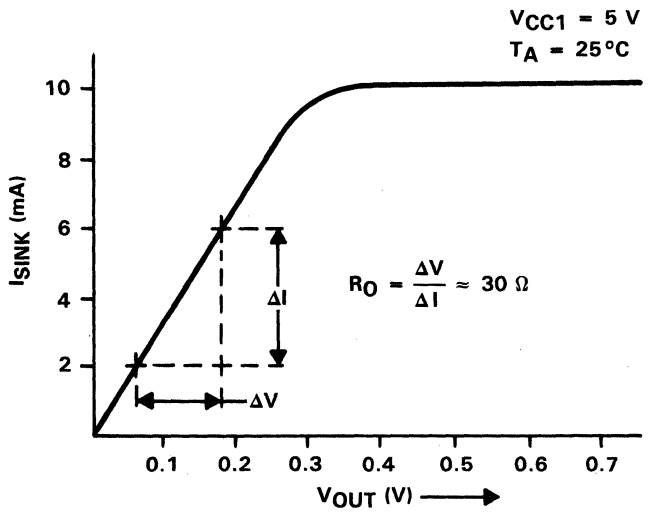


Figure 11-142. Typical TL507 Output Characteristic

The analog input, pin 5, is buffered by an emitter follower prior to being connected to the inputs of the comparators, and the buffer reduces the worst-case analog input current to 300 nA. The circuit or transducer, which drives the analog input, must have a low enough input impedance to minimize the effects of the input current or it will create an input offset. Comparator 2 has a nominal offset voltage of 200 mV as indicated in Figure 11-138. When the analog input voltage is less than 200 mV, the output is forced to a low state to indicate that the analog input voltage is out of range. Since the offset voltage has a ±50% tolerance, it is not suitable for measurement purposes. When the analog input exceeds the upper ramp voltage of 0.75 V_{CC1}, the output goes low again as an indication of overrange. Since the analog input current of the TL507 device is typically 10 nA, it can be used in a sample-hold configuration as shown in Figure 11-143.

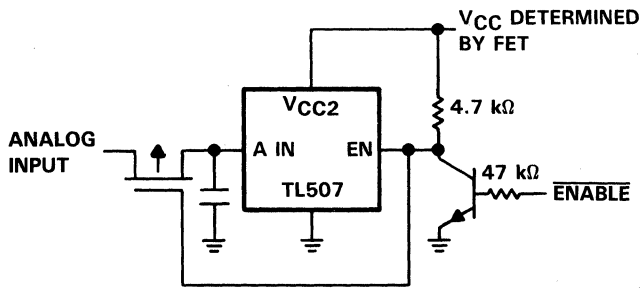


Figure 11-143. Sample Hold Circuit

The TL507 device has an internal regulator that converts an unregulated 8 V to 18 V input into a regulated 5 V. The unregulated input, pin 7, is called V_{CC2}. The regulated voltage is available on pin 6 as V_{CC1}. If more current is needed, pin 7 can be left open and a regulated voltage between 3.5 Vand 6 V can be applied to pin 6. The

typical output characteristic for the regulator is shown in Figure 11-144. Additional loading on the regulated V_{CC1} should not exceed 5 mA. When the internal regulator is used, both the V_{CC1} and V_{CC2} pins should be decoupled with a 10 μF capacitor to ground.

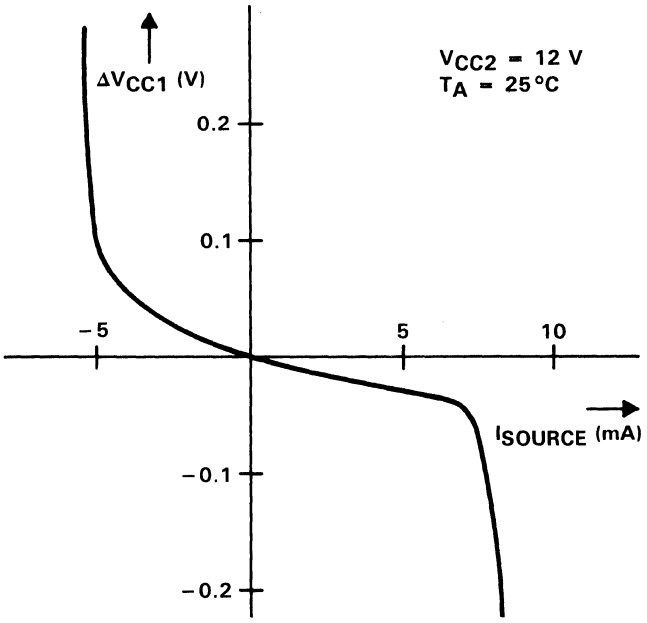


Figure 11-144. Typical V_{CC1} Characteristic

Single-Wire Power, Data, and Clock Cycle Transmitter

In this application, a remote sensor and the TL507 are used to provide a pulse-width-modulated signal representing a sensed analog input level. Connection between the remote location and a central control logic unit is over a single wire and common ground. This wire carries the clock pulses and unregulated power to the remote location and also returns the PWM signal.

Figures 11-145 and 11-146 show the basic circuitry and resulting waveforms. Q1 is used to chop the supply voltage and provide clock pulses to the remote location. The clock signal is fed directly to the TL507 clock input. It is also connected to diode D1 and capacitor C1 for filtering to provide the dc power for the TL507 A/D converter and the TLC271 signal conditioner. Adjusting the TLC271 gain provides the proper input levels for conversion by the TL507, allowing calibration of the output in degrees Celsius or Fahrenheit. Since the TL507 is continuously clocked, without any reset or enable, it continuously converts the analog input signal as illustrated in Figure 11-146. The pulse-width-modulated output signal from the TL507 is fed back over the wire and through a filter (R1 and C2) to remove the clock pulses. A TL331 comparator detects the PWM signal produced by the TL507. The comparator output, along with SN7400 and SN74ALS109A control logic, controls the TIL307 intelligent display.

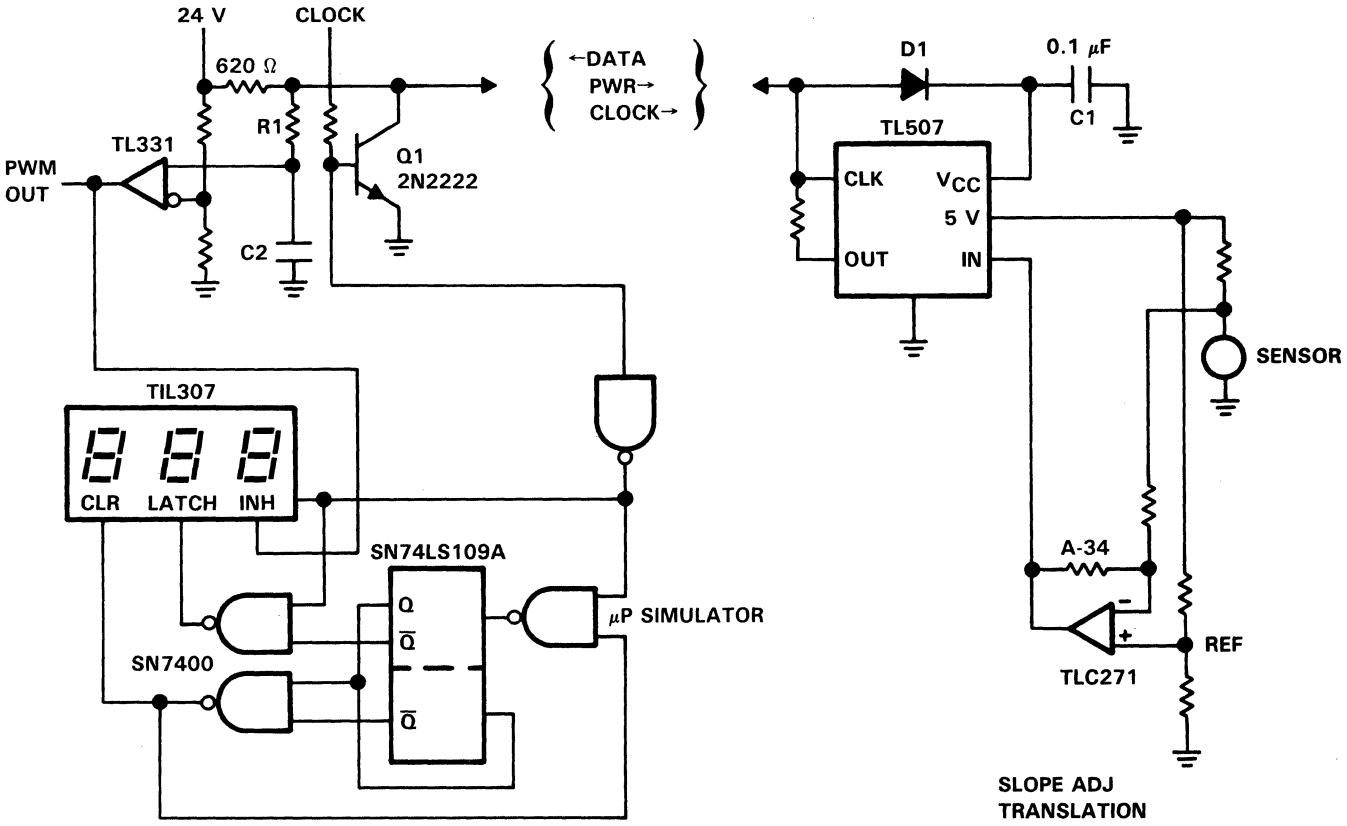


Figure 11-145. Remote-Sensor, Single-Wire A/D Converter

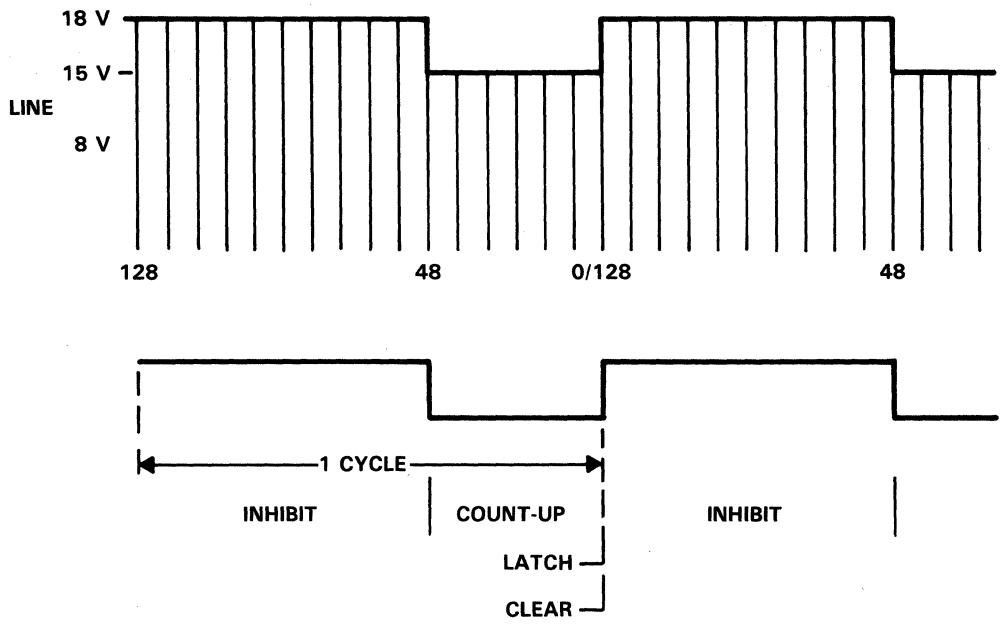


Figure 11-146. TL507 Waveforms

TL507 High Voltage Isolation Application and Signal Coupling

The circuit in Figure 11-147 illustrates the use of an opto-coupler interface between a microprocessor and the TL507 device. In this circuit, the TL507 may be located at a high voltage point while the TIL125 devices provide isolation for the microprocessor. This design is intended to minimize the opto-coupler switching times as much as possible without sacrificing conversion performance.

TL507 to TMS1000 Interface

In some applications, the TL507 device is used with a single-chip microprocessor such as the TMS1000. Figure 11-148 shows a TL507 device used with the PMOS TMS1000NLP microprocessor. Control of the single TL507 device is accomplished using serial control. Using parallel control would allow direct control of 4 TL507 devices. If necessary, up to 15 TL507s may be controlled if the 4 kΩ inputs of the TMS1000 are expanded using an external TMS1025 integrated circuit. The organization of the inputs and outputs of the TMS1000 microprocessor shown in Figure 11-148 is given only as an example and may be changed as required.

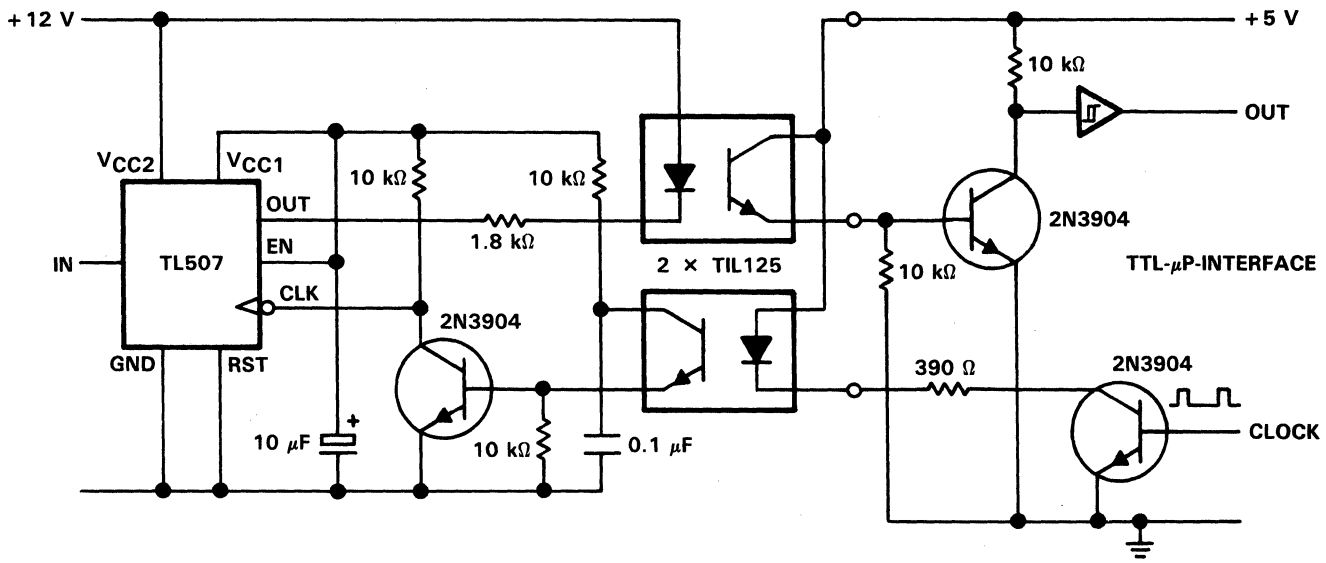


Figure 11-147. Example of High Voltage Isolation and Signal Coupling

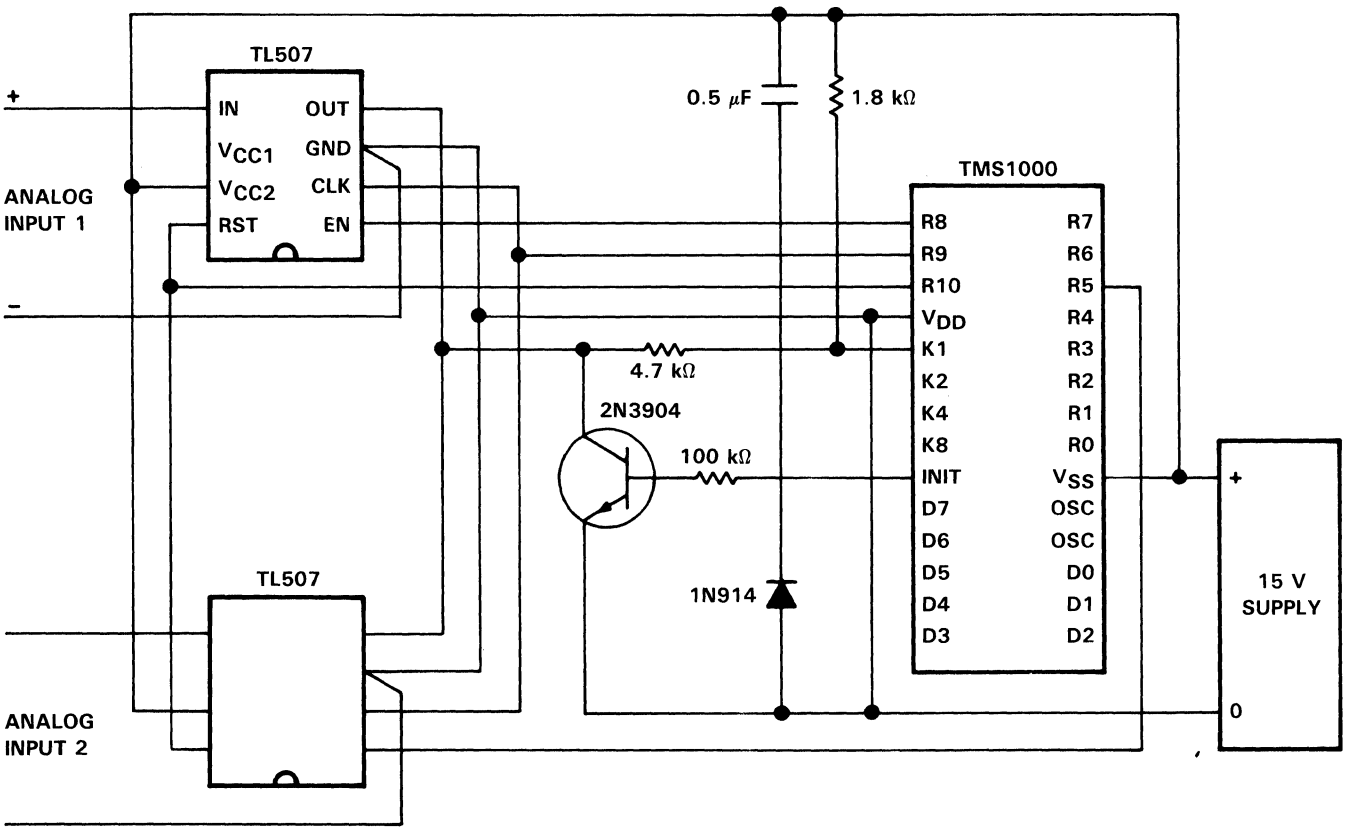


Figure 11-148. TL507 — TMS1000 Interface

TL507 to TMS1000C Interface

Figure 11-149 shows the interface between a TL507 device and a TMS1000C microprocessor. This is the CMOS version of the single-chip TMS1000 microprocessor. This circuit is particularly relevant for applications requiring low power consumption. Since the current requirement of the TMS1000C microprocessor is less than 3 mA, it may be supplied from the V_{CC1} regulator of the TL507 device. Since the total current requirement of the circuit is less than 10 mA, it can be powered from a single 9 V battery. The transistor in parallel with the TL507 output may be omitted if the undefined state of the TL507 output is taken into account during initialization.

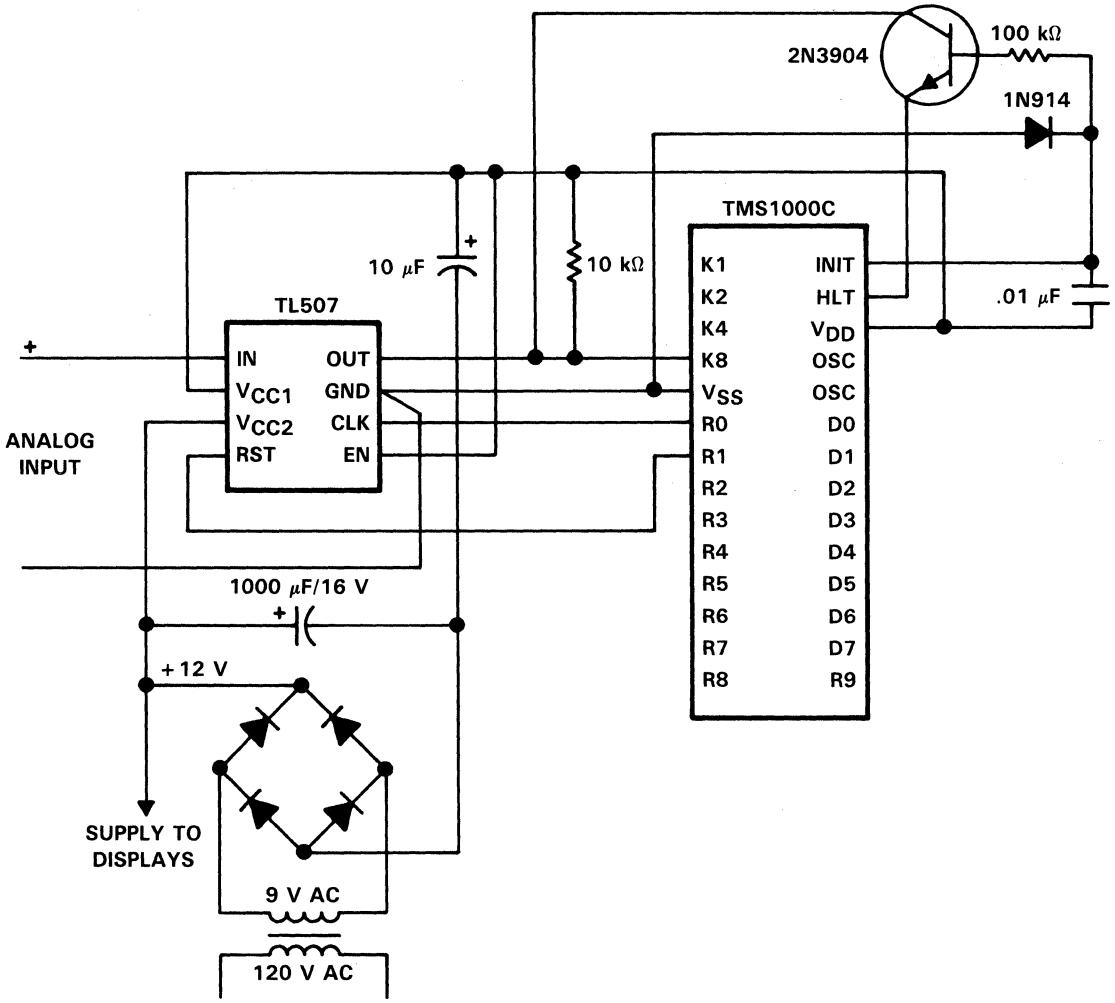


Figure 11-149. TL507 — TMS1000C Interface

Summary

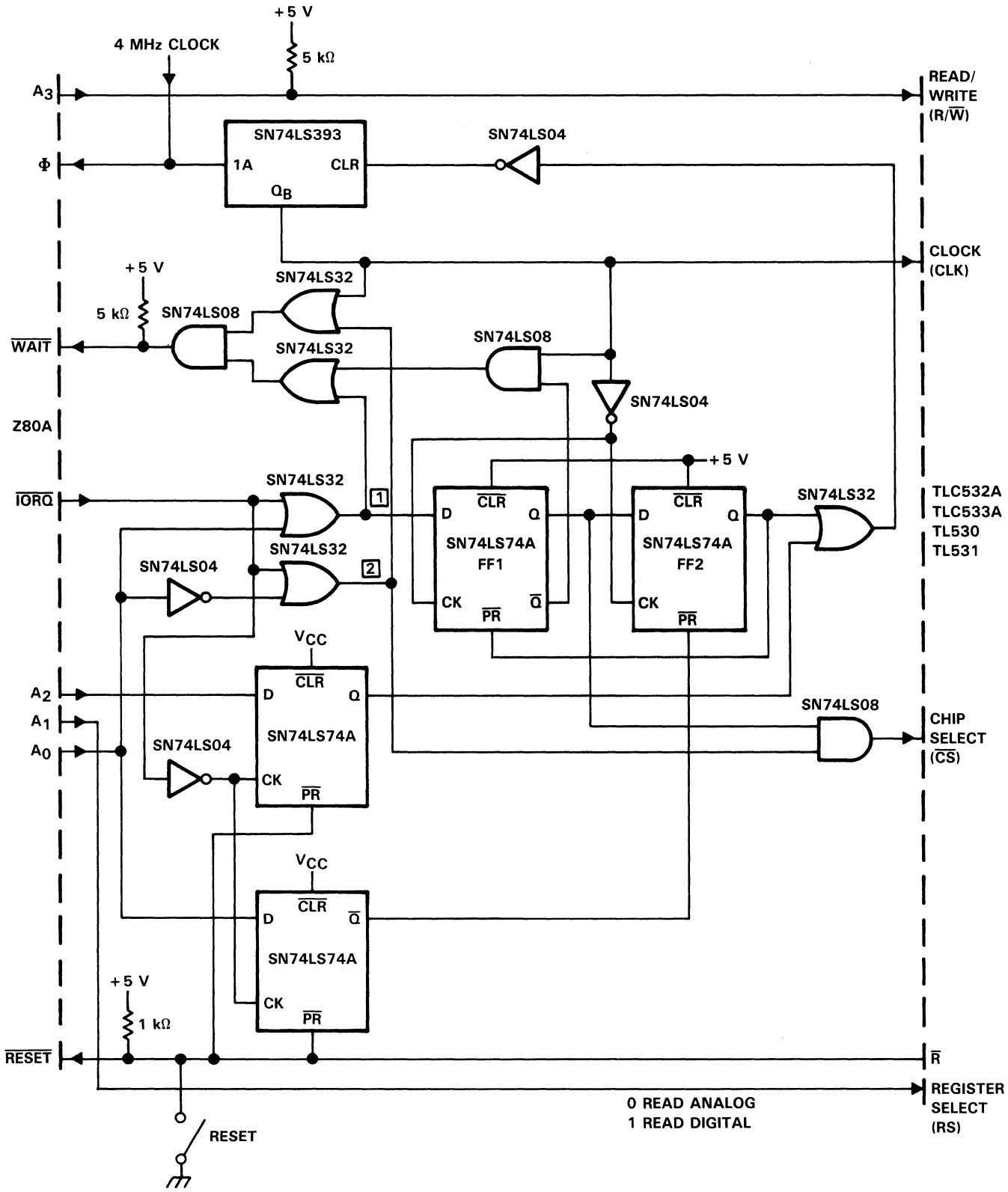
The low cost of the TL507 device allows it to be used in almost any 7-bit application. By converting the analog signal to a stream of digital pulses, where the number of pulses is directly proportional to the analog input, the TL507 device can be used with many different data transmission schemes. Simple coding of the clock frequency or ac power line polarity can be combined with the TL507 device to achieve unique, noise-immune, inexpensive data transmission systems.

INTERFACE FOR TLC532A, TLC533A, TL530, AND TL531 DEVICES TO ZILOG Z80A AND Z80 MICROPROCESSORS

The TLC532A device provides a direct interface to a microprocessor-based system. It contains three 16-bit internal registers: control register, analog conversion register, and digital data register. Control signals enter on an 8-line, TTL compatible, 3-state data bus with read/write, register select, and chip select control inputs.

The interface circuitry is shown in Figure 11-150. This circuitry is powerful since it allows the microprocessor to write to and read from the A/D converters quickly and efficiently via the bus. Since these devices are bus-oriented, the interface circuitry uses them in an optimum fashion by providing microprocessor bus write-and-read capability. This interface circuitry allows the microprocessor to fully use all of the A/D converter's write-read instructions. One-byte instructions can be used to initiate the A/D conversion by setting the SC bit and to determine the end of conversion by monitoring the EOC bit.

The circuitry uses a Z80A microprocessor. However, the same circuitry could use a Z80 microprocessor by changing the clock frequency from 4 MHz to 2 MHz. Such a change will double the A/D conversion time since the frequency of the clock signal into the A/D converter is halved. The 4 MHz clock signal can be changed to any frequency with the provision that the resulting A/D converter clock frequency, whose frequency is the microprocessor clock frequency divided by 4, does not exceed the A/D upper clock frequency limit. Also, a microprocessor clock signal whose frequency is greater than 4 MHz may be used. In this case the resulting A/D converter clock frequency must not exceed the upper frequency limit for the A/D converter.



NOTE: Interface has been tested with TTL-LS parts only, however interface should work with HCMOS ICs.

Figure 11-150. Z80A Microprocessor Interface Diagram, TLC532A, TLC533A, TL530, and TL531

Input/Output Mapping

Table 11-39 shows the Input/Output (I/O) map which allows the microprocessor to write or read to the A/D converter in any of the possible modes. If other microcomputer I/O interfaces are required in addition to the A/D converter, the $\overline{IORQ}$ signal must be blocked in the interface circuitry during non-A/D write or read operations. $\overline{IORQ}$ is the signal that drives the interface circuitry and causes a write or read to occur. Failure to mask or block the $\overline{IORQ}$ signal will allow the A/D converter and other I/O devices to access the microprocessor bus at the same time and cause a data collision. If a 2-byte write or read is desired, each of the two bytes must be written or read completely. Partial execution of a 2-byte write or read operation will leave chip select (CS) low and prevent A/D conversion from taking place.

Although not tested, this interface circuitry might be memory mapped, rather than I/O mapped, by substituting MREQ in place of $\overline{IORQ}$.

Timing Diagram

Figure 11-151 shows the timing diagram. The microprocessor's WAIT input is used to slow down the microprocessor to synchronize the A/D converter and microprocessor bus communications. Note that the A/D converter's chip select (CS) is kept low during an entire 2-byte write or read cycle. If chip select (CS) were allowed to go high between the 2-byte operations, the microprocessor would write or read the A/D converters most significant byte twice.

Software

The following software program listings can be used for both A/D write and read operations. The first routine uses an initial 2-byte write to start the A/D conversion, to address analog input A0, to select a 1-byte read test loop or a delay to allow completion of the A/D conversion, and uses a 2-byte read to obtain the A/D conversion result in the least significant or second byte. Note that a 2-byte write or read is necessary to access the A/D converter's least significant byte.

Two more listings present software routines that can be used to read the digital data registers in 2- and 1-byte formats, respectively. These read instructions do not have to be preceded by an A/D conversion delay period, since these registers provide digital information only.

Table 11-39. TLC532A I/O Map

		A_3	A_2	A_1	A_0	NO. OF BYTES COMMUNICATED
Control Register Write	MSB	0	0	1	0	2
	LSB	0	0	1	1	
	MSB	0	1	1	0	1
Analog Data Register Read	MSB	1	0	0	0	2
	LSB	1	0	0	1	
	MSB	1	1	0	0	1
Digital Data Register Read	MSB	1	0	1	0	2
	LSB	1	0	1	1	
	MSB	1	1	1	0	1

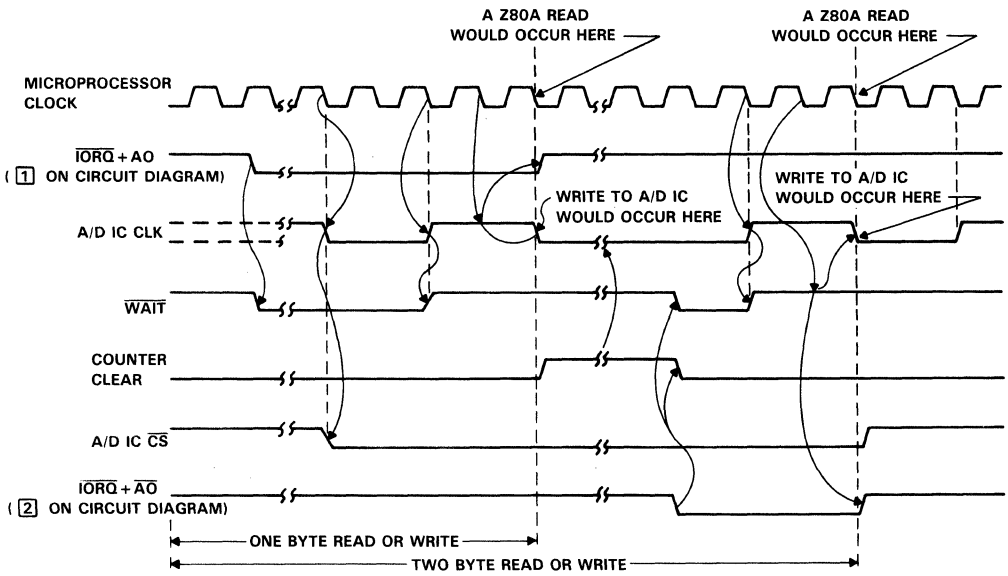


Figure 11-151. Timing Diagram for the Z80A/Z80 Interface to the TLC532A, TLC533A, TL530, and TL531

```
                                ; Software for A/D Conversion Using the TLC532A,
                                  TLC533A, TL530 and TL531
                                ;
0000                            ORG 00H             ;(used by cross-assembler)
0000    3E 01                   LD A,01H            ;01H into accumulator
0002    03 02                   OUT (02H),A         ;write MSB (STRT CONV = 1)
0004    3E 00                   LD A,00H            ;00H into accumulator
0006    D3 03                   OUT (03H),A         ;write LSB (ADDR = 0)
                                ;
0008    DB 0C           TEST:   IN A,(OCH)          ;read MSB analog register
000A    F2 08 00                JP P,TEST           ;branch if not END OF CONVERSION = 0
                                ;
                                ;The above test loop can be substituted by any delay
                                ;which meets the A/D IC's time requirements for A/D
                                ;conversion.
                                ;
0000    DB 08                   IN A,(08H)          ;read analog register MSB
000F    DB 09                   IN A,(09H)          ;read analog register LSB,
                                                    ;conversion result is in accumulator
                                ;
                                ;
-------------------------------------------------------------------------------------------------------------------------------
                                ;
                                ; Software for Digital Data Register 2-Byte Read
                                ;
0100                            ORG 100H            ;(used by cross assembler)
0100    DB 0A                   IN A,(0AH)          ;fetch MSB
0102    47                      LD B,A              ;store MSB
0103    DB 0B                   IN A,(0BH)          ;fetch LSB, MSB is in B and
                                                    ;LSB is in A
                                ;
                                ;
-------------------------------------------------------------------------------------------------------------------------------
                                ;
                                ; Software for Digital Data Register 1-Byte Read
                                ;
0200                            ORG 200H            ;(used by cross assembler)
0200    DB 0E                   IN A,(0EH)          ;fetch MSB, MSB is in A
0202    47                      END                 ;(used by cross-assembler)
```

Additional Comments

The time required for analog-to-digital conversion for the A/D converters in this application are presented in Table 11-40. It is necessary that the microprocessor allow these time periods for A/D conversion, either through a test loop, where the microprocessor reads the end of conversion (EOC) bit, or a delay period that may be obtained in any convenient manner by the microprocessor.

Table 11-40. A/D Conversion Times for the Z80A/Z80 Interface to the TLC532A, TLC533A, TL530 and TL531

	A/D IC CLOCK CYCLE'S REQUIRED FOR CONVESION (See Note 1)	CONVERSION TIME (μs) USING AN A/D IC CLOCK FREQUENCY OF 1 MHz (See Note 2)
TLC532A	29½	29.5
TLC533A	29½	29.5
TL530	290½	290.5
TL531	290½	290.5

NOTES: 1. Time 0 is the first rising edge of the first write cycle of a 2-byte write operation.
2. The interface circuitry will generate an A/D IC clock signal of 1 MHz when using a 4 MHz microprocessor clock signal.

INTERFACE FOR TLC532A, TLC533A, TL530, AND TL531 DEVICES TO INTEL 8048 AND 8049 AND INTEL 8051 AND 8052 MICROPROCESSORS

This application covers all the possible interface combinations for these parts. These interfaces offer the following advantages:

1. Fast complete cycle times for loading the A/D address, performing conversion, and retrieving the conversion
2. Flexible use of A/D converter pins for either A/D conversion or input of digital data
3. Low cost.

These Intel microprocessor families consist of the following:

INTEL 8048 and 8049 Family

8035AHL	8048AH	8748H
8039AHL	8049AH	8749H
8040AHL	8050AH	80C49

INTEL 8051 and 8052 Family

8031AH	8051AH	8751H
8032AH	8052AH	80C51

Because of differences in timing, two different circuit configurations are required for interfacing these A/D converters and microprocessor families. For reference, these two configurations are called Interface 1 and Interface 2.

Interface 1 is more desirable than Interface 2 since it does not constrain the microprocessor's data bus operations. It also allows the microprocessor to use the A/D converter software in external program memory. Unfortunately, different timing specifications prevent Interface 1 from being used for Interface 2 (8051 and 8052 to TL530, TL531, and TLC533A interface).

Hardware — Interface 1

Figure 11-152 shows the circuit configuration for Interface 1. This circuit can be used for the 8051 and 8052 devices interface to the TLC532A device, and the 8048 and 8049 devices interface to the TL530, TL531, and TLC533A devices.

The system clock for the A/D converter is obtained from the microprocessor crystal oscillator. To assure proper operation of the crystal oscillator, a high impedance buffer must be used to prevent overloading the oscillator. An important design detail is that the low and high level input requirements of the buffer must lie within the range of the oscillator signal. This compatibility will prevent missing edge transitions in the A/D converter's system clock signal. The buffered crystal oscillator signal must be frequency divided to assure that the resulting system clock frequency does not exceed the upper frequency limit of the A/D converter. Any convenient divider circuitry may be used to accomplish this task.

Timing Diagram — Interface 1

The timing diagrams for the 8051, 8052 and 8048, 8049 devices to TLC532A converter interface are presented in Figures 11-153 and 11-154, respectively. The timing diagrams cover a complete conversion cycle and the reading of the digital data registers. In Figure 11-154, the required number of conversion clocks will increase for the TL530, TL531, and TLC533A devices due to a lower clock frequency operating range and the higher number of conversion clock cycles that are required by the TL530 and TL531 converters.

Software — Interface 1

The software listing for the interface between the 8051 and 8052 devices and the TLC532A device follows. The software listing for the 8048 and 8049 to the TL530, TL531, TLC532A, and TLC533A interface is also included. The conversion software program or the digital data register software program can be incorporated into a subroutine so the designer can easily access the software with a simple subroutine call. Also, the conversion software assumes that the A/D converter address has been placed in register R2 and, upon completion of A/D conversion, stores the conversion result in register R2. The digital data register software stores the most significant (MS) byte and the least significant (LS) byte in registers R2 and R3, respectively.

```
                        ; Software for Intel 8051/52 Family to
                        ; TLC532A Interface 1
                        ;
                        ;               Software for Conversion
                        ;
0000                                    ORG 000H
0000    43 90 0C                        ORL P1,#0CH         ;CS, RS = 1
0003    C2 90                           CLR P1.0            ;Counter clear = 0
0005    7F 01                           MOV R7,#01H         ;Do delay to allow 3 system clocks
0007    DF FE           D1CSEQ1:        DJNZ R7,D1CSEQ1     ;to occur so A/D IC will
                                                            ;recognize CS = 1
0009    B2 90                           CPL P1.0            ;Counter clear = 1
000B    53 90 FS                        ANL P1,#F5H         ;CS, R/W(bar) = 0
000E    74 01                           MOV A,#01H          ;Write MSByte (Set SC=1)
0010    F2                              MOVX @R0,A
0011    EA                              MOV A,R2            ;Get A/D IC address, which is
                                                            ;assumed to be in R2
0012    F2                              MOVX @R0,A          ;Write LSByte or A/D IC address
0013    43 90 0A                        ORL P1,#0AH         ;CS, R/W(bar) = 1
0016    C2 90                           CRL P1.0            ;Counter clear = 0
                        ;
                        ;               A delay must occur here to allow the A/D IC to
                        ;               complete conversion. The delay must allow at least
                        ;               29.5 A/D IC system clock cycles to occur.
                        ;
0018    B2 90                           CPL P1.0            ;Counter clear = 1
001A    53 90 F3                        ANL P1,#F3H         ;CS, RS = 0
001D    E2                              MOVX A,@R0          ;Read Analog Conversion Register MSByte
001E    E2                              MOVX A,@R0          ;Read Analog Conversion Register LSByte
                                                            ;or conversion result
001F    FA                              MOV R2,A            ;Store conversion result
0020    B2 93                           CPL P1.3            ;CS = 1
0022    C2 90                           CLR P1.0            ;Counter clear = 0
                        ;
-------------------------------------------------------------------------------------------------------------------------------
                        ; Software for Reading Digital Data Registers
                        ;
0100                                    ORG 0100H
0100    43 90 0E                        ORL P1,#0EH         ;CS, RS, R/W(bar) = 1
0103    C2 90                           CLR P1.0            ;Counter clear = 0
0105    7F 01                           MOV R7,#01          ;Do delay to allow 3 system clocks
0107    DF FE           D2CSEQ1:        DJNJ R7,D2CSEQ1     ;to occur so A/D IC will
                                                            ;recognize CS = 1
0109    B2 90                           CPL P1.0            ;Counter clear = 1
010B    C2 93                           CLR P1.3            ;CS = 0
010D    E2                              MOVX A,@R0          ;Read Digital Data Register MSByte
010E    FA                              MOV R2,A            ;Store Digital Data Register MSByte
010F    E2                              MOVX A,@R0          ;Read Digital Data Register LSByte
0110    FB                              MOV R3,A            ;Store Digital Data Register LSByte
0111    B2 93                           CPL P1.3            ;CS = 1
0113    C2 90                           CLR P1.0            ;Counter clear = 0
0115                                    END
```

```
                        ; Software for Intel 8048/49 Family —
                        ; TL530, TL531, TLC532A, and TLC533A Interface 1
                        ;
;                                       Software for Conversion
                        ;
                                        ORG 000H
0000    89 0C                           ORL P1,#0CH         ;CS, RS = 1
0002    99 FE                           ANL P1,#FEH         ;Counter clear = 0
0004    BF 01                           MOV R7,#01H         ;Do delay to allow 3 system clocks
0006    EF 06           D1CSEQ1:        DJNZ R7,D1CSEQ1     ;to occur so A/D IC will
                                                            ;recognize CS = 1
0008    89 01                           ORL P1,#01H         ;Counter clear = 1
000A    99 F5                           ANL P1,#F5H         ;CS, R/W(bar) = 0
000C    23 01                           MOV A,#01H          ;Write MSByte (Set SC=1)
000E    90                              MOVX @R0,A
000F    FA                              MOV A,R2            ;Get A/D IC address, which is
                                                            ;assumed to be in R2
0010    90                              MOVX @R0,A          ;Write LSByte or A/D IC address
0011    89 0A                           ORL P1,#0AH         ;CS, R/W(bar) = 1
0013    99 FE                           ANL P1,#FEH         ;Counter clear = 0
                        ;
                        ;               A delay must occur here to allow the A/D IC to
                        ;               complete conversion. The delay must allow at least
                        ;               29.5 A/D IC system clock cycles to occur for the
                        ;               TLC532A and TLC533A. The TL530 and TL531 require
                        ;               290.5 system clock cycles.
                        ;
0015    89 01                           ORL P1.#01H         ;Counter clear = 1
0017    99 F3                           ANL P1,#F3H         ;CS, RS = 0
0018    80                              MOVX A,@R0          ;Read Analog Conversion Register MSByte
0019    80                              MOVX A,@R0          ;Read Analog Conversion Register LSByte
                                                            ;or conversion result
001A    AA                              MOV R2,A            ;Store conversion result
001B    89 08                           ORL P1,#08H         ;CS = 1
001D    99 FE                           ANL P1,#FEH         ;Counter clear = 0
                        ;
-------------------------------------------------------------------------------------------------------------------------------
                        ;               Software for Reading Digital Data Registers
                        ;
                                        ORG 0100H
0100    89 0E                           ORL P1,#0EH         ;CS, RS, R/W(bar) = 1
0102    99 FE                           ANL P1,#FEH         ;Counter clear = 0
0104    BF 01                           MOV R7,#01          ;Do delay to allow 3 system clocks
0106    EF 06           D2CSEQ1:        DJNZ R7,D2CSEQ1     ;to occur so A/D IC will
                                                            ;recognize CS = 1
0108    89 01                           ORL P1,#01H         ;Counter clear = 1
010A    99 F7                           ANL P1,#F7H         ;CS = 0
010C    80                              MOVX A,@R0          ;Read Digital Data Register MSByte
010D    AA                              MOV R2,A            ;Store Digital Data Register MSByte
010E    80                              MOVX A,@R0          ;Read Digital Data Register LSByte
010F    AB                              MOV R3,A            ;Store Digital Data Register LSByte
0110    89 08                           ORL P1,#08H         ;CS = 1
0112    99 FE                           ANL P1,#FEH         ;Counter clear = 0
                                        END
```

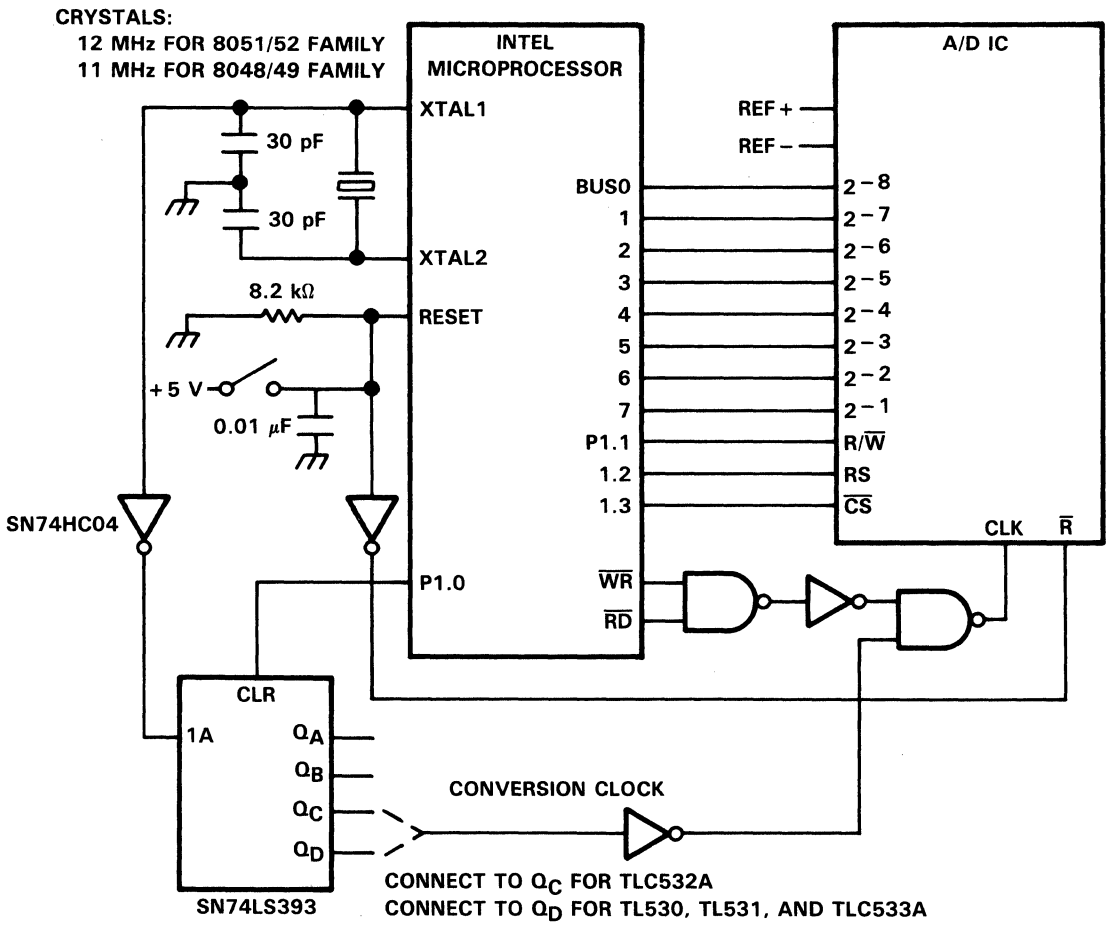


Figure 11-152. Intel 8051/52 Family to TLC532A Interface 1 and Intel 8048/49 Family to TL530, TL531, TLC532A, and TLC533 Interface 1

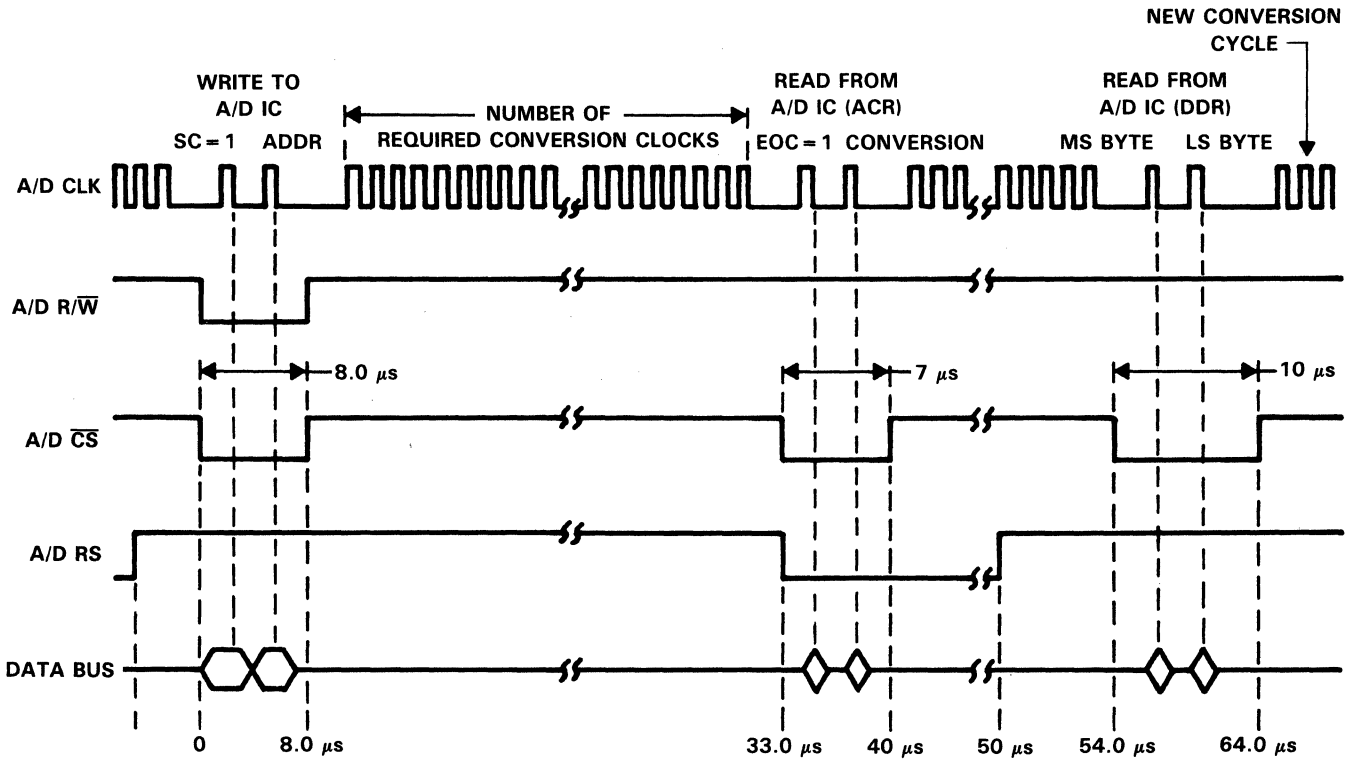


Figure 11-153. Timing Diagram of A/D Conversion Cycle for Intel 8051/52 Family — TLC532A Interface 1

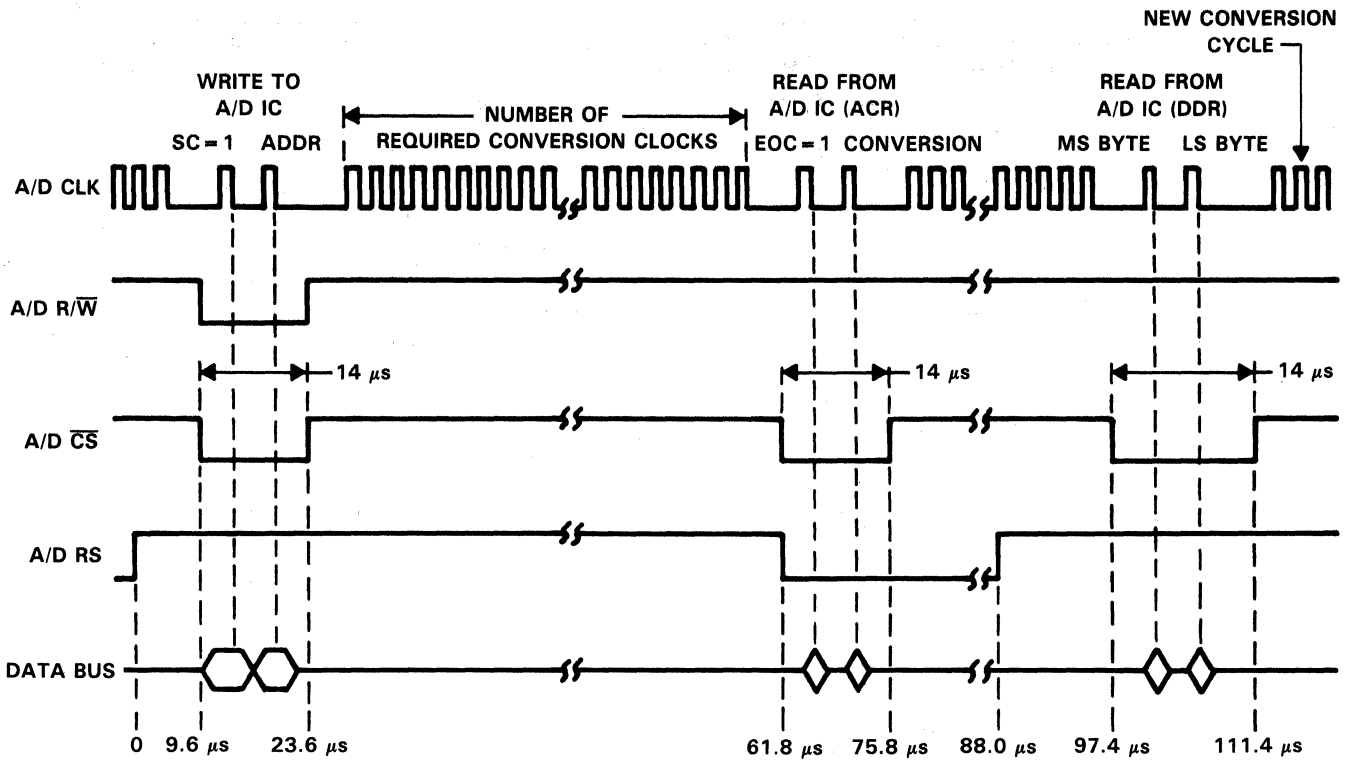


Figure 11-154. Timing Diagram of A/D Conversion Cycle for Intel 8048/49 Family — TLC532A

Hardware — Interface 2

Figure 11-155 presents the circuit configuration for Interface 2. This circuit can be used for the 8051 and 8052 devices interface to the TL530, TL531, and TLC533A devices.

The A/D converter's data port can be connected to any of the microprocessor's ports. However, if the connection is made to Port 0, the interface circuitry prevents the incorporation of the A/D software into the external program memory. As seen in the following software listings, three microprocessor instructions are required to read a byte of information from the A/D converter. Unfortunately, the first of the three instructions causes the A/D converter to drive the microprocessor bus in a non-3-state mode that prevents the microprocessor from retrieving any subsequent instructions. Refer to the Hardware — Interface 1 paragraph for a description of how the A/D converter system conversion clock is generated.

Timing Diagram — Interface 2

The timing diagram for the 8051 and 8052 devices interface to the TLC533A device is presented in Figure 11-156. The timing diagram covers a complete conversion cycle and the reading of the digital data registers. The required number of conversion clocks will increase for the TL530 and TL531 devices due to the higher number of conversion clock cycles that are required by the TL530 and TL531 converters.

Software — Interface 2

The software listings for Interface 2 follow. Unlike Interface 1, the microprocessor write (WR) and read (RD) pins are not used to generate the A/D converter clock during write and read operations. Instead, the clock is generated by toggling the P1.4 pin. This change between Interface 1 and Interface 2 was made to accommodate the different timing specifications of the 8051 and 8052 devices and the TL530, TL531, and TLC533A converters. (See the Interface 1 paragraph for further description of the software listings.)

```
                        ; Software Conversion for Intel 8051/52
                        ; Family — TL530, TL531, TLC533A Interface 2
                        ;
0000                                    ORG 000H
0000    43 90 0C                        ORL P1,#0CH         ;CS, RS = 1
0003    53 90 EE                        ANL P1,#EEH         ;Counter clear, Slow clock = 0
0006    7F 02                           MOV R7,#02H         ;Do delay to allow 3 system clocks
0008    DF FE           D1CSEQ1:        DJNZ R7,D1CSEQ1     ;to occur so A/D IC will
                                                            ;recognize CS = 1
000A    B2 90                           CPL P1.0            ;Counter clear = 1
000C    53 90 F5                        ANL P1,#F5H         ;CS, R/W(bar) = 0
000F    75 B0 01                        MOV P3,#01H         ;Write MSByte (Set SC=1) to Port 3
0012    B2 94                           CPL P1.4            ;Raise slow clock
0014    B2 94                           CPL P1.4            ;Lower slow clock
0016    8A B0                           MOV P3,R2           ;Write A/D IC address, which is
                                                            ;assumed to be in R2, to Port 3
0018    B2 94                           CPL P1.4            ;Raise slow clock
001A    B2 94                           CPL P1.4            ;Lower slow clock
001C    75 B0 FF                        MOV P3,#FFH         ;Put Port 3 pins to input mode
001F    43 90 0A                        ORL P1,#0AH         ;CS, R/W(bar) = 1
0022    C2 90                           CLR P1.0            ;Counter clear = 0
                        ;
                        ;               A delay must occur here to allow the A/D IC to
                        ;               complete conversion. The delay must allow at least
                        ;               29.5 A/D IC system clock cycles to occur for the
                        ;               TLC533A. Similarly, at least 290.5 clock cycles
                        ;               must occur for the TL530 and TL531. Further the
                        ;               frequency of the clock signal must not exceed
                        ;               the specification for the A/D IC.
                        ;
0024    B2 90                           CPL P1.0            ;Counter clear = 1
0026    53 90 F3                        ANL P1,#F3H         ;CS, RS = 0
0029    B2 94                           CPL P1.4            ;Raise slow clock
002B    AA B0                           MOV R2,P3           ;Read MSByte of the analog
                                                            ;conversion register
002D    B2 94                           CPL P1.4            ;Lower slow clock
002F    B2 94                           CPL P1.4            ;Raise slow clock
0031    AA B0                           MOV R2,P3           ;Read and store LSByte of the analog
                                                            ;conversion register or conversion
0033    B2 94                           CPL P1.4            ;Lower slow clock
0035    B2 93                           CPL P1.3            ;CS = 1
0037    C2 90                           CLR P1.0            ;Counter clear = 0
                        ;
                        ;
```

```
                        ;
                        ;
                        ; Software for Reading Digital Data Registers
                        ;
0100                                ORG 0100H
0100    43 90 0E                    ORL P1,#0EH       ;CS, RS, R/W(bar) = 1
0103    53 90 EE                    ANL P1,#EEH       ;Counter clear, Slow clock = 0
0106    7F 02                       MOV R7,#02        ;Do delay to allow 3 system clocks
0108    DF FE           D2CSEQ1:    DJNZ R7,D2CSEQ1   ;to occur so A/D IC will
                                                      ;recognize CS = 1
010A    B2 90                       CPL P1.0          ;Counter clear = 1
010C    75 B0 FF                    MOV P3,#FFH       ;Put Port 3 pins to input mode
010F    C2 93                       CLR P1.3          ;CS = 0
0111    B2 94                       CPL P1.4          ;Raise slow clock
0113    AA B0                       MOV R2,P3         ;Read and store MSByte of the digital
                                                      ;data register
0115    B2 94                       CPL P1.4          ;Lower slow clock
0117    B2 94                       CPL P1.4          ;Raise slow clock
0119    AB B0                       MOV R3,P3         ;Read and store LSByte of the digital
                                                      ;data register
011B    B2 94                       CPL P1.4          ;Lower slow clock
011D    B2 93                       CPL P1.3          ;CS = 1
011F    C2 90                       CLR P1.0          ;Counter clear = 0
0121                                END
```

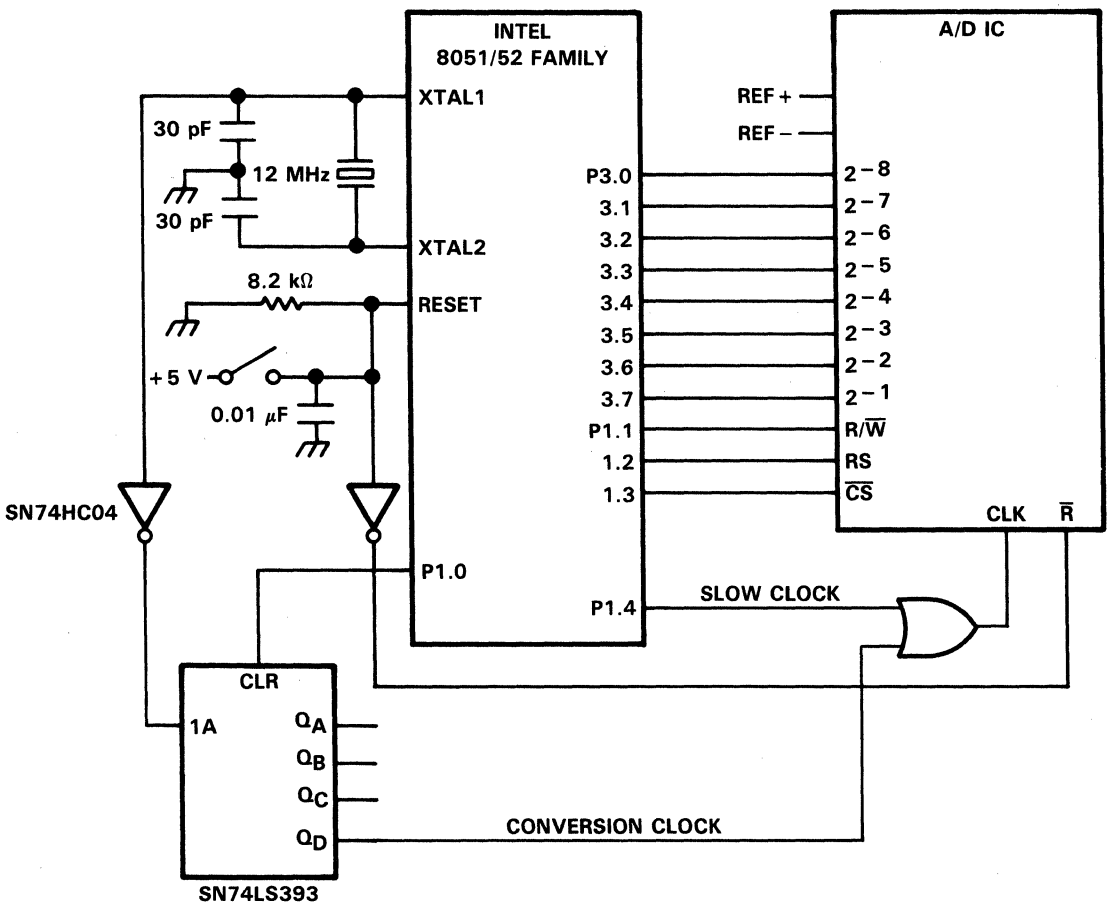


Figure 11-155. Intel 8051/52 Family — TL530, TL531, TLC533A Interface 2

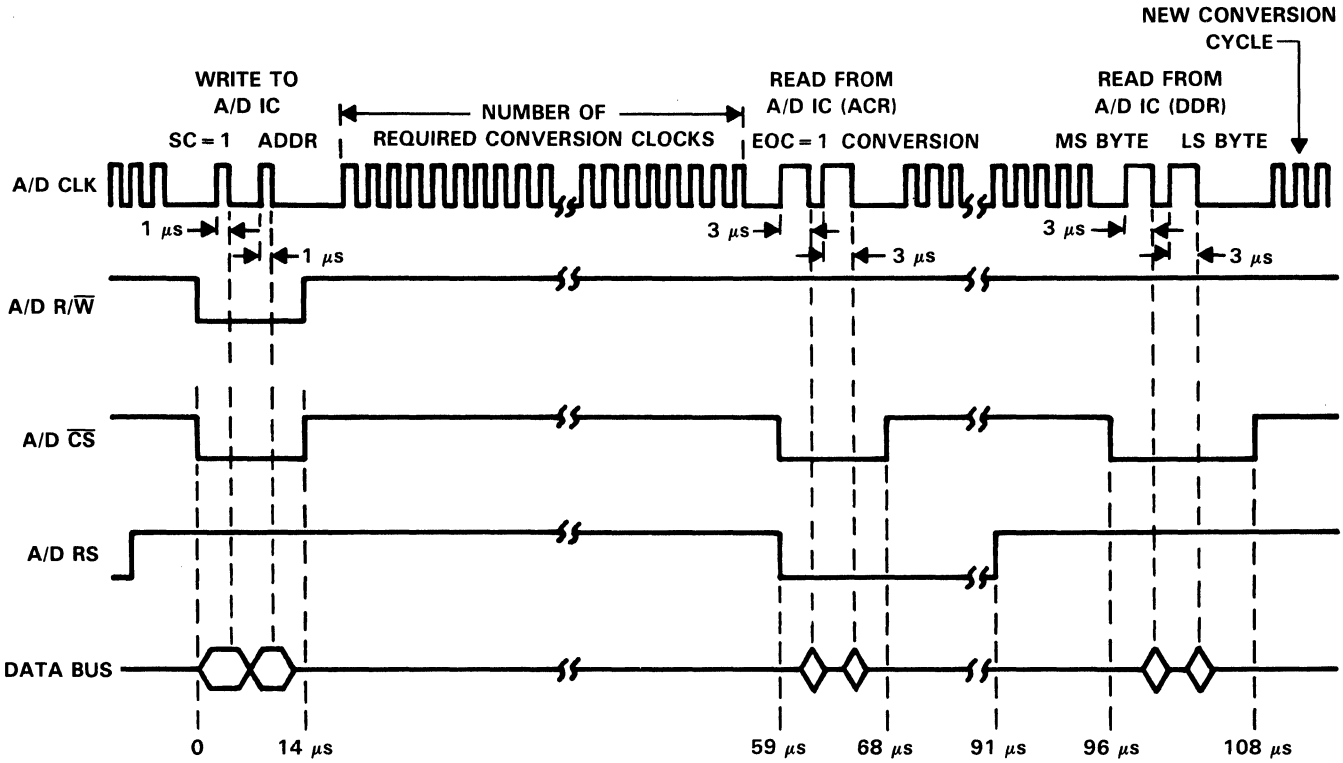


Figure 11-156. Timing Diagram of A/D Conversion Cycle for Intel 8051/52 Family to TLC533A Interface 2

Additional Comments

The A/D converter clock signal should not be interrupted during A/D conversion because of the possible loss of electrical charge on the A/D converter's internal capacitors. Interruption of the clock signal during an A/D converter write or read operation presents no problem. All of the software offered for use with these interfaces complies with the above requirement since the conversion clock is not stopped until after the A/D conversion is completed.

INTERFACE FOR TLC532A, TLC533A, AND TL530 DEVICES TO THE ROCKWELL 6502 MICROPROCESSOR

This application describes techniques for interfacing the TLC532A converter device and compatible peripheral chips to the Rockwell 6502 microprocessor. The TLC532A family of A/D converters consists of chips offering combinations of conversion speed and number of analog inputs. The interface presented deals specifically with the TLC532A, TLC533A, and the TL530 devices. Other members of the TL/TLC53x family are not included because the bus timing specification cannot be guaranteed. It is important that SN74S00 or SN74AS00 NAND gates be used to guarantee operation of this interface circuit.

Principles of Operation

The TLC532A device to 6502 device interface circuit and timing diagrams are shown in Figures 11-157 and 11-158, respectively. A listing of the control software necessary to operate the interface follows.

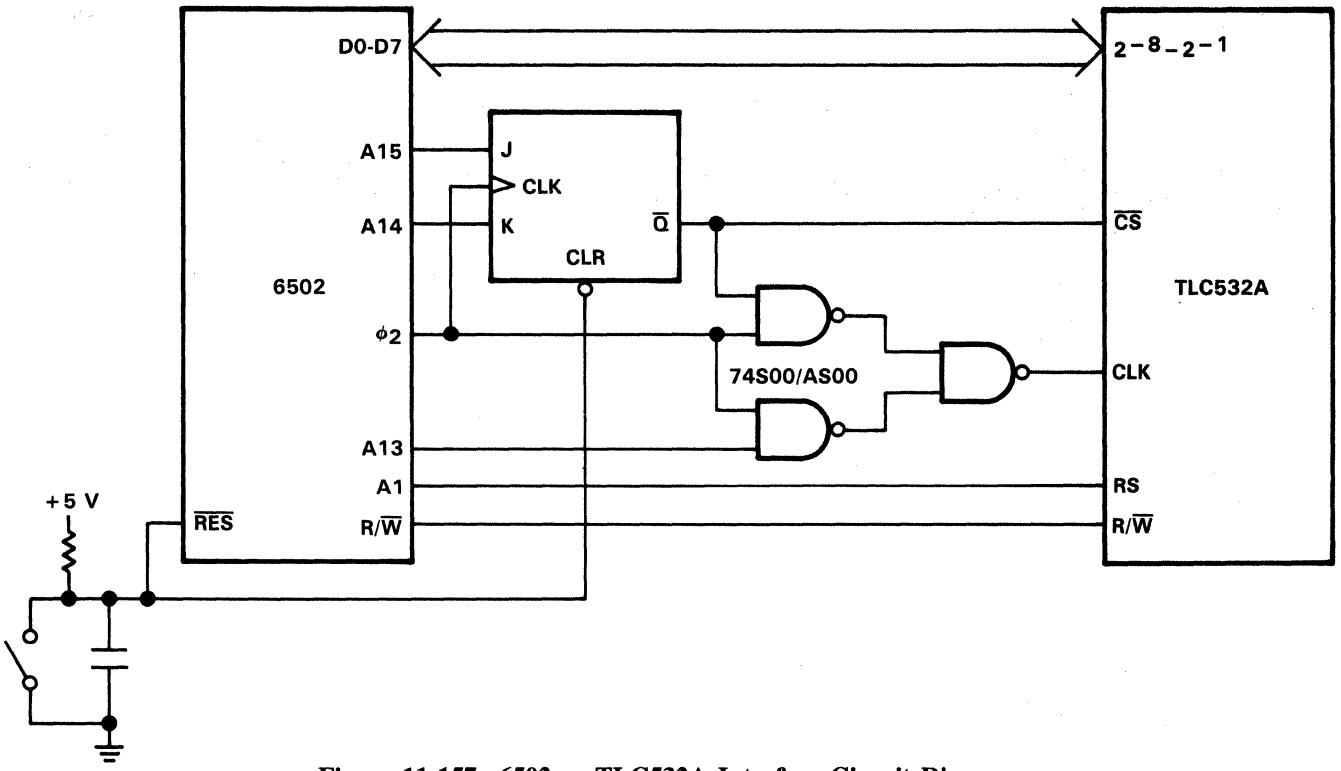


Figure 11-157. 6502 — TLC532A Interface Circuit Diagram

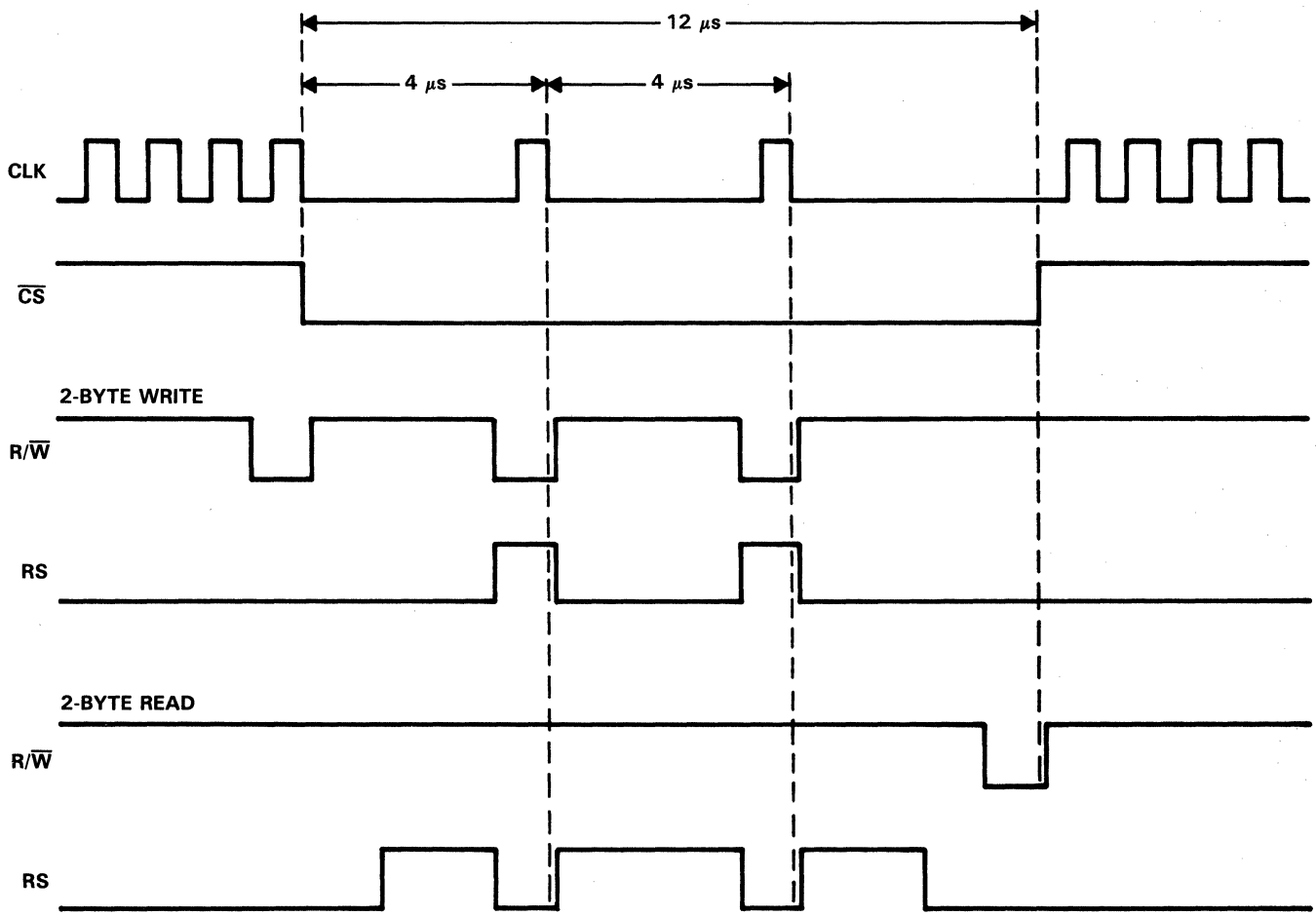


Figure 11-158. 6502 — TLC532A Interface Timing Diagram

```
;
;ADDRESS ASSIGNMENTS
;
ANALYZER:   .EQU 0000H
ACMSB:      .EQU 2400H
ACLSB:      .EQU 2401H
CRMSB:      .EQU 2402H
CRLSB:      .EQU 2403H
DDMSB:      .EQU 2502H
DDLSB:      .EQU 2503H
SETCS:      .EQU 4400H
CLRCS:      .EQU 8400H
;
;
;
            LDX #$01        ; SET SC BIT
            LDA #$00        ; SELECT MUXADDRESS
            STA CLRCS       ; BRING CHIP SELECT LOW
            STX CRMSB       ; LOAD CONTROL REG MSB
            STA CRLSB       ; LOAD CONTROL REG LSB, START CONV.
            LDA SETCS       ; BRING CHIP SELECT HIGH
            LDY #$07        ;
LOOP:       DEY             ; DELAY UNTIL CONVERSION COMPLETE
            BNE LOOP        ;
            LDA CLRCS       ; BRING CHIP SELECT LOW
            LDA ACMSB       : READ CONV. REG MSB (EOC BIT)
            LDA ACLSB       ; READ CONV. REG LSB (RESULT)
            STA SETCS       ; BRING CHIP SELECT HIGH
```

A conversion cycle begins by bringing chip select ($\overline{CS}$) low. This is accomplished by clocking a high into the J input of the flip-flop on the trailing edge of PH 2, bringing $\overline{Q}$ low. A low on $\overline{Q}$ also inhibits the PH 2 clock from reaching the TLC532A device. When the first byte of a 2-byte write cycle is being written, address bit A13 goes high. This allows one PH 2 pulse to reach the TLC532A device and clock in the byte. The write cycle for the second byte is exactly the same as the first. Chip select ($\overline{CS}$) is then brought high by clocking a high into the K input of the flip-flop to bring $\overline{Q}$ high again. Analog-to-digital conversion requires 29 clock cycles. Therefore, a delay loop is included in the software listing to allow for this conversion time.

The 2-byte read cycle operation is similar to that of the write cycle since it uses address bit A13 as a gating signal for the clock input to the TLC532A device. One- or 2-byte reads of either the analog conversion registers or the digital data registers may be performed with the proper register select signals. The software listing shows the necessary software for a 2-byte read of the analog conversion register, and leaves the A/D conversion result in the accumulator. One complete data acquisition cycle can be performed every 66 microseconds.

INTERFACE FOR TLC532A, TLC533A, TL530, AND TL531 DEVICES TO THE MOTOROLA 6800, 6802, 6809, AND 6809E MICROPROCESSORS

Since these A/D converters are bus oriented, the interface circuitry uses these converters in an optimum way by providing microprocessor bus write and read capability. Two interface circuits are presented: Interface 1 in Figure 11-159 and Interface 2 in Figure 11-160 that provide 1- and 2-byte write/read communications capability between the microprocessor and the A/D converter. Only the 2-byte capability is demonstrated in this application. To use the 1-byte capability of the A/D converter, 1-byte external memory write/read instructions can be used.

Input/Output Mapping

Table 11-41 presents the I/O map that allows the microprocessor to write or read to the A/D converter. This I/O map is intended as a guide and does not preclude other mapping possibilities.

Table 11-41. I/O Map

	A15	A14	A13*	R/$\overline{W}$
Control Register Write	0	1	1	0
Analog Data Register Read	0	0	1	1
Digital Data Register Read	0	1	1	1
ROM Program	1	X	X	X

*A13 = 1 to prevent the 6802 from reading its internal RAM and the A/D IC simultaneously.

Timing Diagram

A timing diagram for Interface 1 with a 1 MHz microprocessor clock cycle is shown in Figure 11-161. The microprocessor write and read timing diagrams for Interface 2 are shown in Figures 11-162 and 11-163.

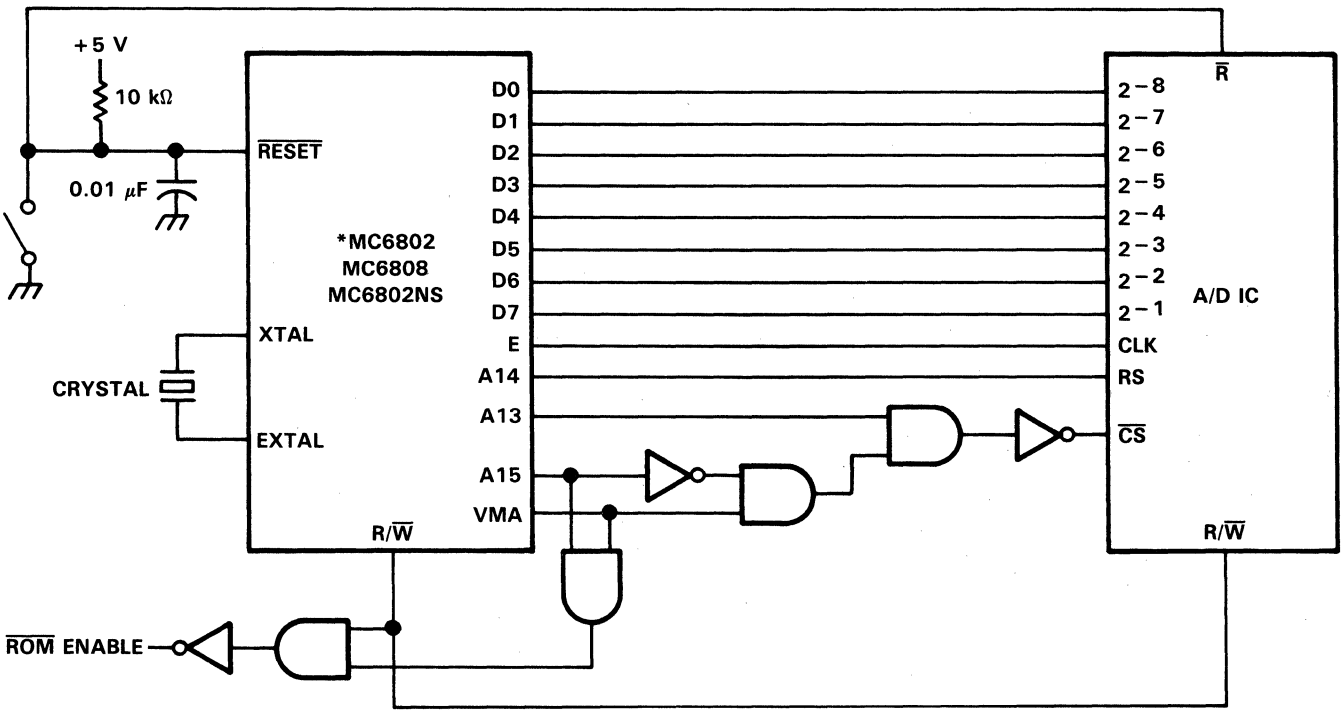
Software

The following software listings can be used for both interface circuits. These listings show the software for conversion and for reading the digital data registers, respectively. For conversion, the software must determine the end of conversion by monitoring the end of conversion bit (EOC) in the most significant (MS) byte of the analog conversion register or by allowing a delay so the A/D converter can complete conversion. The length of the delay can be computed by referring to Table 11-42. This table shows the number of clock cycles required for each A/D converter to complete conversion.

Table 11-42. A/D Conversion Time

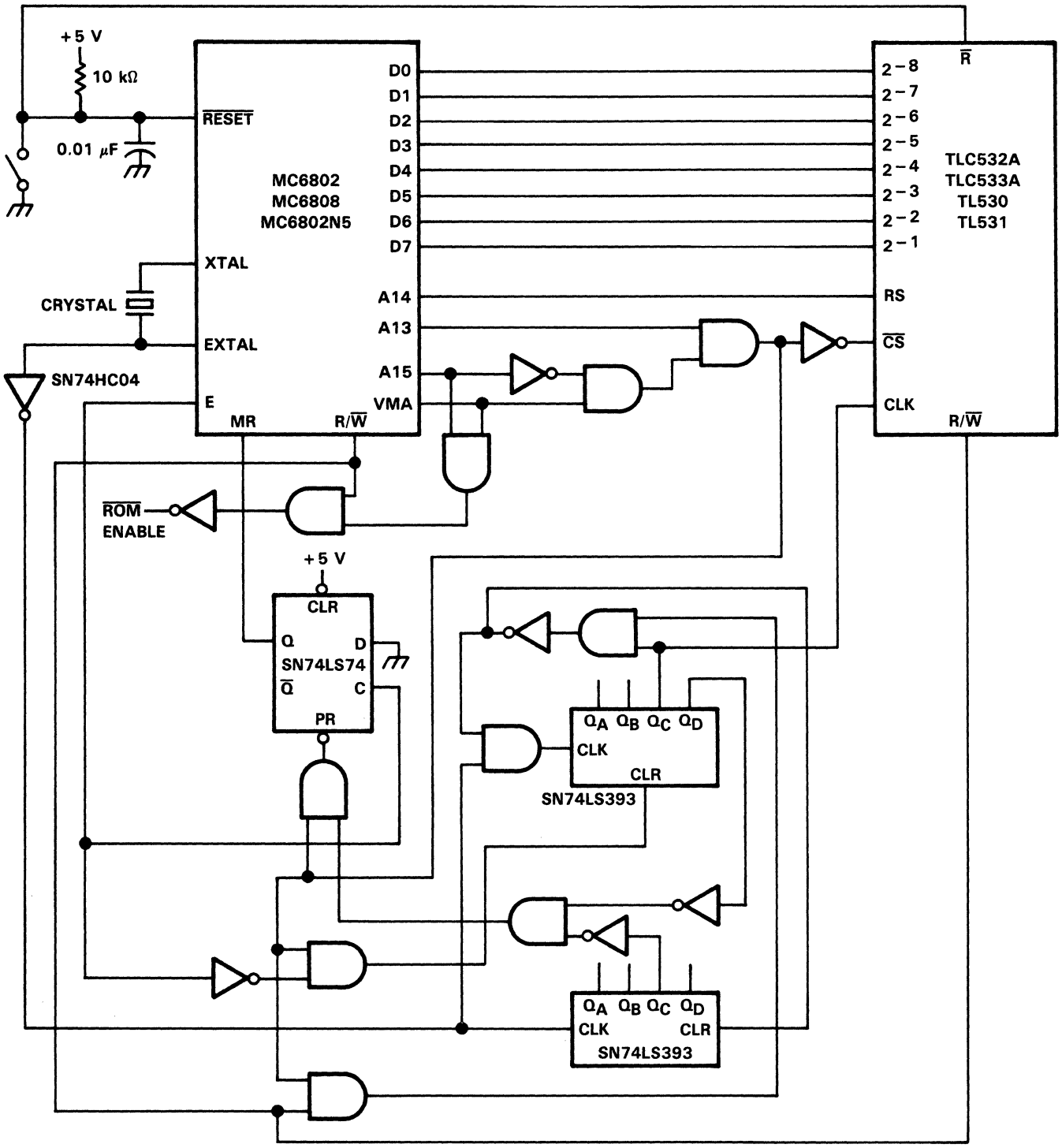
A/D IC	A/D IC CLOCK CYCLES REQUIRED FOR CONVERSION (See Note)
TLC532A	29½
TLC533A	29½
TL530	290½
TL531	290½

NOTE: Time 0 is the first rising edge of the first write cycle of a 2-byte write operation.



*See Table 11-43

Figure 11-159. Interface 1 Hardware Circuitry



*See Table 11-43 for information about other microprocesor configurations.

Figure 11-160. Interface 2 Hardware Circuitry

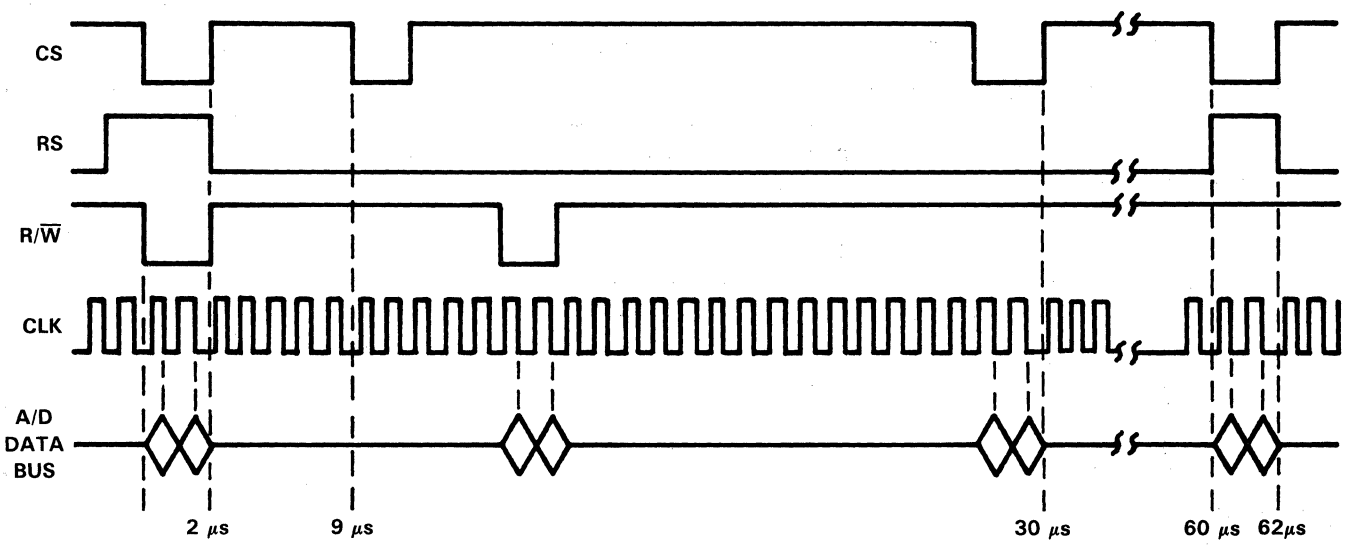


Figure 11-161. Timing Diagram
(Interface 1 and 6802 Microprocessor with a 1 MHz Clock Cycle)

```
                    ; Software for 6800 Family —
                    ; TL530, TL531, TLC532A, TLC533A Interface
                    ;
                    ;              Software for Conversion
                    ;
07FE  80                                        ;Microprocessor reset, branch
07FF  00                                        ;to 8000H. 2716 UVPROM was used
                                                ;for this test.
8000                          ORG 8000H         ;A15 = 1 enables ROM memory
8000  CE 01 05               LDX #0105H        ;SC = 1 in MSB, Address analog
                                                ;channel #5 in LSB
8003  FF 60 00               STX $6000H        ;Write MSB and LSB to A/D IC
8006  01          STILLC:   NOP               ;Allow I A/D clock cycle to
8007  01                    NOP               ;occur so that A/D recognizes
                                                ;CS51
8008  FE 20 00               LDX $2000H        ;Read MSB and LSB from Analog
                                                ;Conversion Register
800B  DF 00                 STX $0000H        ;Store MSB & LSB in 0000H & 0001H
                                                ;RAM memory
800D  96 00                 LDAA $0000H       ;Load A with MSB
800F  85 80                 BITA $80H         ;If EOC bit = 0; set microprocessor
                                                ;condition code Z bit
8011  27 F3                 BEQ STILLC        ;If EOC = 0; branch and re-test EOC bit.
                                                ;If EOC = 1; conversion result is in
                                                ;the LSB of the X register.
                    ;
                    ;The loop within the statements STILLC: NOP and BEQ STILLC can
                    ;be replaced with a delay, which can be obtained in any way
                    ;which is convenient to the designer. After the delay, the
                    ;software must execute a LDX $2000H instruction and the con-
                    ;version result will lie in the LSB of the X register. Table 1142
                    ;shows the delays which are required for each A/D IC.
                    ;              Software for Reading Digital Data Registers
                    ;
8013  FE 60 00               LDX $6000H        ;Read MSB and LSB from Digital Data
                                                ;Register. These bytes are now in the
                                                ;X register.
8016                          END
```

Considerations for Different Microprocessors

Table 11-43 lists the factors to be considered when using the Motorola microprocessors. The crystal oscillator and E pin considerations in column 1 apply to both Interface 1 and 2. Considerations such as slowing the microprocessor (in column 2) apply only to Interface 2. All of the microprocessors can be easily adapted to Interface 1. Table 11-43 and Figure 11-162 enable the designer to readily adapt all of the microprocessors except the 6800 to Interface 2. For the 6800 device with a clock frequency greater than 1 MHz to the A/D converter, an external clock generator which can be slowed down must be used.

Table 11-43. Considerations for Using Other Microprocessors

MICROPROCESSOR	CRYSTAL OSCILLATOR AND E PIN	SLOWING THE MICROPROCESSOR*
6800	ϕ_2 is equivalent to the 6802/6809 E pin	Need an external circuit to slow the microprocessor
6802/6808/6802ns	See Figure 11-159	See Figure 11-159
6809	See Figure 11-159	See Figure 11-159 Substitute MRDY for MR
6809E/68HC09E	See Figure 11-159	Need an external circuit to slow the microprocessor

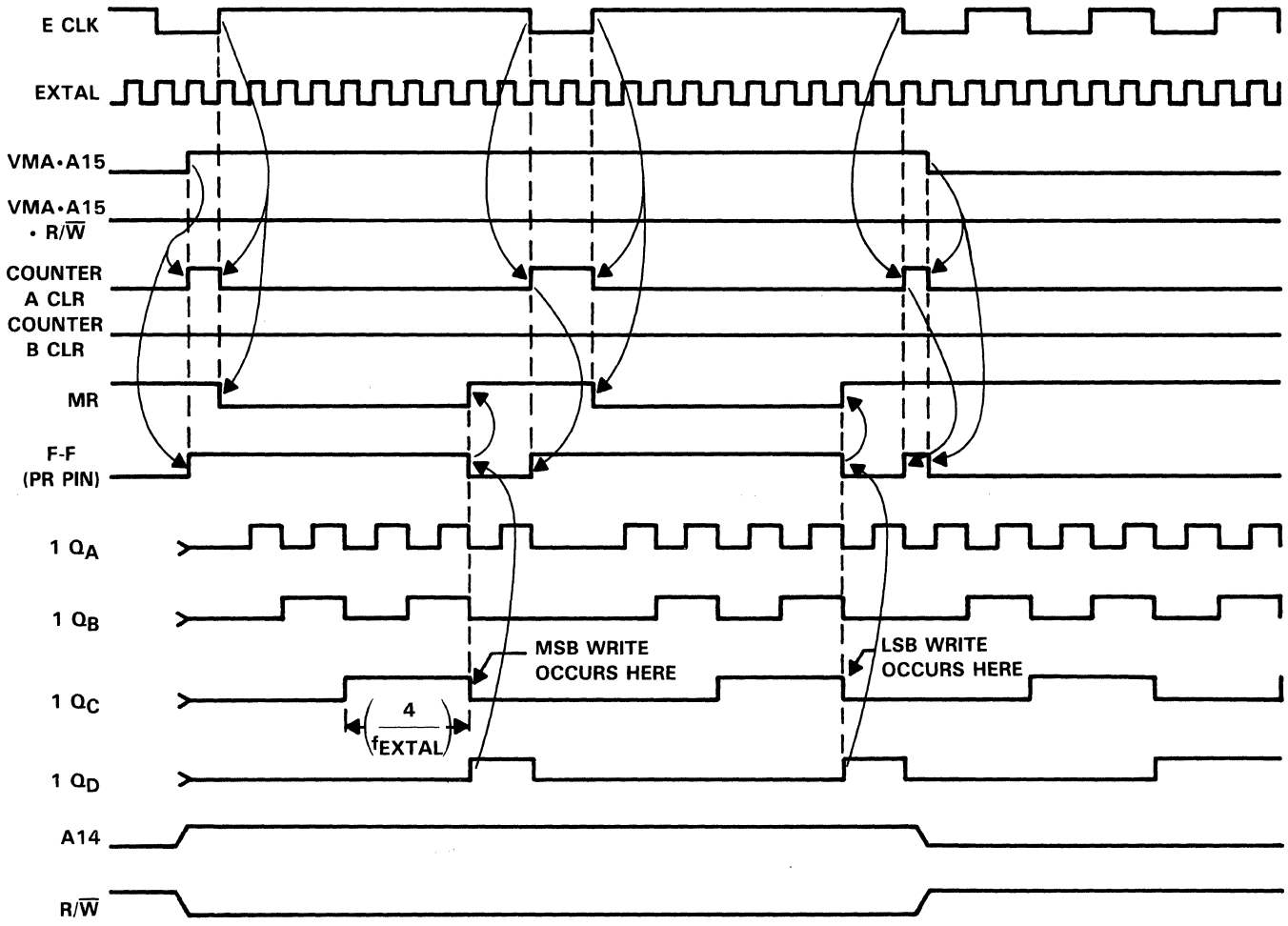


Figure 11-162. Interface 2 Microprocessor Write Timing Diagram

Interface Selection

In general, microprocessors whose clock frequency is less than or equal to 1 MHz can use Interface 1. The TL530, TL531, and TLC533A device specifications are very closely matched but not completely with 1 MHz microprocessor operation and Interface 1. The TLC532A device works satisfactorily with 1 MHz microprocessor operation and Interface 1, although even faster microprocessor clock speeds can be used. If the 68AOX and 68BOX microprocessors are run at full speed, Interface 2 must be used to assure matching between A/D converter and microprocessor specifications. Interface 2 will work with a microprocessor clock frequency that is greater than 2 MHz; however, 2 MHz is generally the upper limit for Motorola microprocessors. Figure 11-164 shows the pertinent timing considerations.

Additional Comments

Although Interface 2 appears complicated, an examination of its write and read timing diagrams in Figures 11-162 and 11-163 reveal the simple strategy of the interface design. This strategy is twofold. First, the lowering of the clock signal during an A/D write causes the microprocessor to leave its temporarily frozen or halted state. This action assures that the necessary data is written into the A/D converter before the microprocessor continues. Thus, a write is guaranteed. Second, the microprocessor's reading of the A/D converter must occur before the clock signal is lowered. Thus, a read is guaranteed. This inexpensive interface allows the designer to take full advantage of these flexible A/D devices.

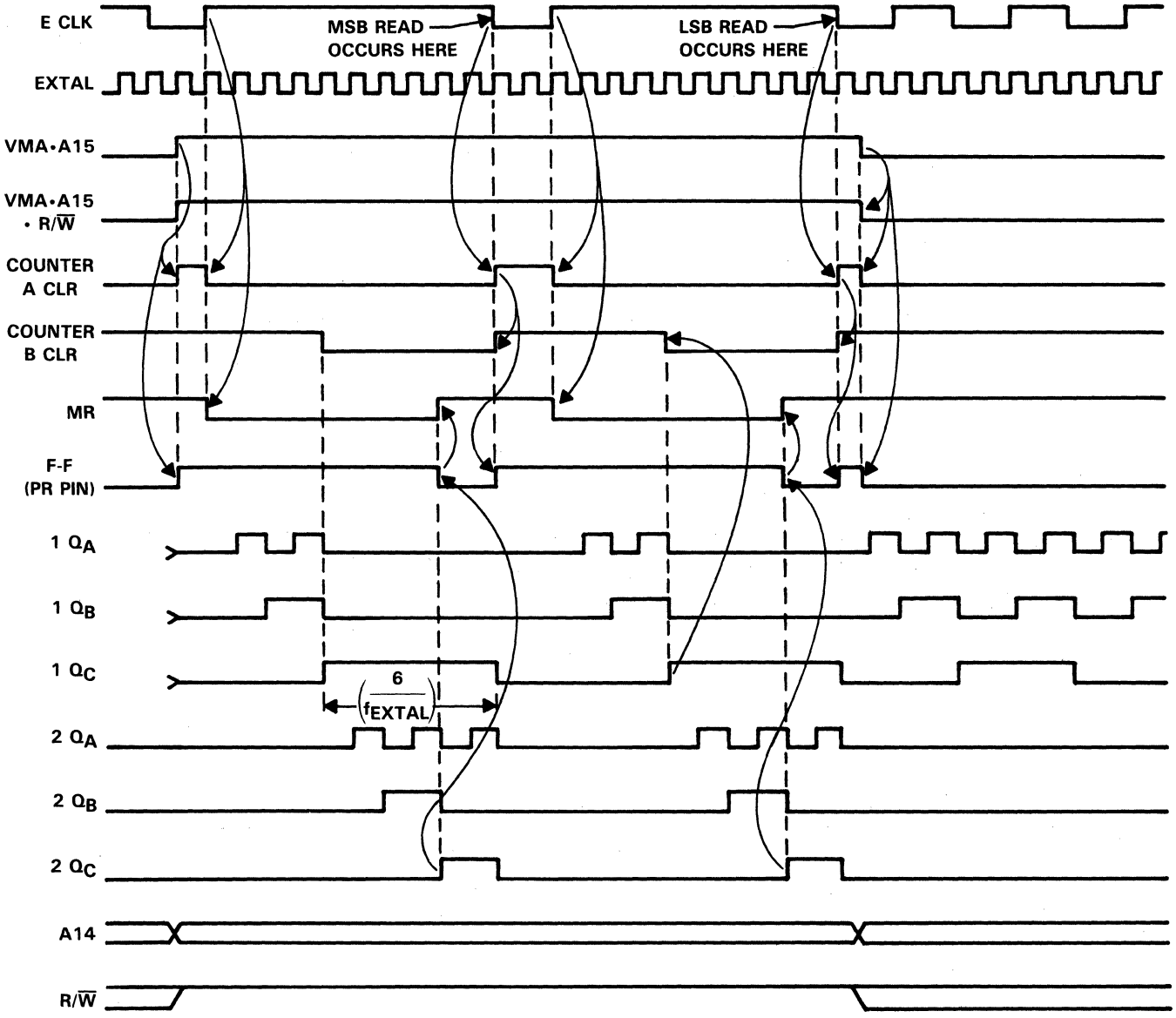
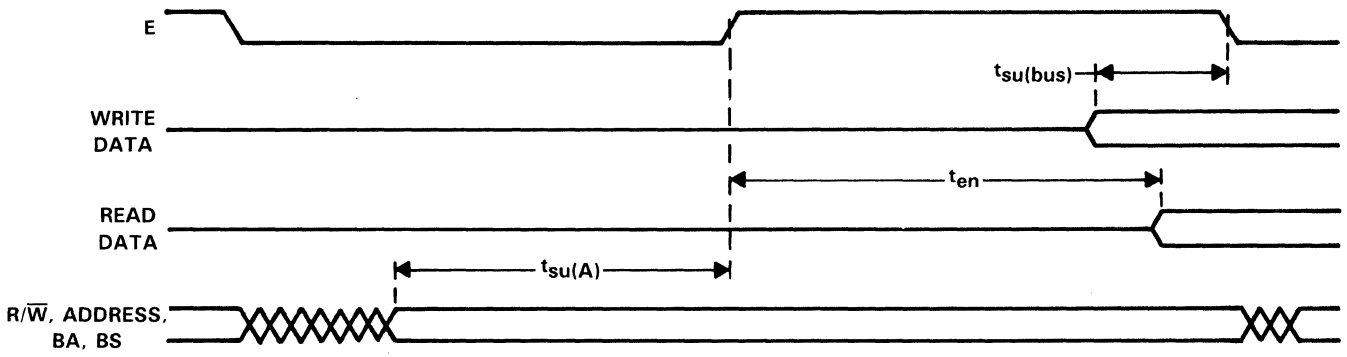


Figure 11-163. Microprocessor Read Timing Diagram



	$t_{su(bus)}$ (ns—MIN)	t_{en} (ns—MAX)	$t_{wH(CLK)}$ (ns—MIN)	$t_{su(A)}$ (ns—MIN)	
TL530	185	335	440	145	A/D IC SPECIFICATIONS
TL531	185	335	440	145	
TLC532A	140	250	230	100	
TLC533A	185	335	440	145	
6800	225	300	450	180	COMPARABLE MICROPROCESSOR SPECIFICATIONS WITH THE ASSUMPTION THAT THE MICROPROCESSOR CLOCK CYCLE IS THE FASTEST POSSIBLE.
68A00	80	170	280	100	
68B00	60	140	220	85	
6802	225	350	450	160	
68A02	110	210	280	100	
68B02	50	150	220	50	
6809	475	370	450	265	
68A09	280	220	280	165	
68B09	220	180	220	120	

Figure 11-164. Timing Considerations

INTERFACE FOR THE TLC540 DEVICE TO ZILOG Z80A AND Z80 MICROPROCESSORS

The TLC540 is a complete data acquisition system on a chip. It includes an analog multiplexer, sample-and-hold, 8-bit A/D converter, three 16-bit registers, and microprocessor control inputs. These inputs are chip select ($\overline{CS}$), address in, system clock, and I/O clock. The system clock and I/O clock do not require any special speed or phase relationship, and are normally used independently. This allows the system clock to run at up to 4 MHz, which ensures a conversion time of less than 9 μs, while the I/O clock runs at up to 2.048 MHz to allow a maximum data transfer rate.

Two different interfaces are shown in this application. While both are TLC540 to Z80 interfaces, the two differ as follows:

1. The control signals are generated by additional hardware for Interface 1, but the control signals for Interface 2 are generated through software
2. Interface 1 is about five times faster than Interface 2
3. Interface 1 has less complicated software than Interface 2
4. Interface 1 costs more than Interface 2, but Interface 2 requires less PC board space.

Interface 1

The circuit shown in Figure 11-165 initiates conversion with an OUT instruction. The timing diagram for this circuit is shown in Figure 11-166. When $\overline{IORQ}$ and $\overline{WR}$ go low, $\overline{CS}$ is brought low while the universal shift register is placed in the load data mode and the system clock is enabled to the clock input to latch in the multiplexer address. The rising edge of $\overline{IORQ}$ enables the I/O clock to the shift register to shift the multiplexer address out while shifting the previous conversion result in. Sampling begins at the falling edge of the fourth I/O clock pulse and continues until the eighth falling edge. At this time the I/O clock is disabled and $\overline{CS}$ is brought high to ensure that the TLC540 device will remain undisturbed during the conversion. Conversion of the addressed analog input requires 36 system clock cycles. During this time, previous conversion results may be read by using an IN instruction. A typical interrupt service routine is shown in the software listing that follows.

```
ISR     PUSH AF
        IN A,(LS299)        ; READ PREVIOUS CONV. RESULT
        LD (DATA), A        ; STORE RESULT
        LD A,D              ; LOAD NEW MUX ADDRESS
        OUT (LS299),A       ; SAMPLE CHANNEL [ INITIATE CONV.
        POP AF
        EI
        RETI
```

NOTE: Register D contains the analog multiplexer address.

At least 36 system clock cycles must occur between interrupts to ensure proper operation. If a new multiplexer address is shifted in while a conversion is in progress, the ongoing conversion will be aborted and a new conversion will be initiated by the falling edge of the eighth I/O clock pulse.

Another software approach is to initiate a new conversion, wait in a delay loop until the conversion is complete and then read in the previous conversion results. A simple program segment using the delay loop method is shown in the software listing that follows. Using this method it is possible to complete a conversion cycle in 21.5 μs.

```
        LD A,D              ; LOAD MUX ADDRESS
        OUT (LS299),A       ; SAMPLE CHANNEL [ INITIATE CONV.
        LD C,03H            ; INITIALIZE COUNTER
WAIT:   DEC C               ; DECREMENT COUNTER
        JP NZ, WAIT         ; IF NOT ZERO KEEP WAITING
        OUT (LS299),A       ; CLOCK RESULTS INTO LS299
        IN A,(LS299)        ; READ CONV RESULTS
```

NOTE: A count of 03H will produce a delay of 10.50 microseconds, suitable for 4 MHz operation, while a count of 05H produces a delay of 17.50 microseconds, suitable for 2.5 MHz operation.

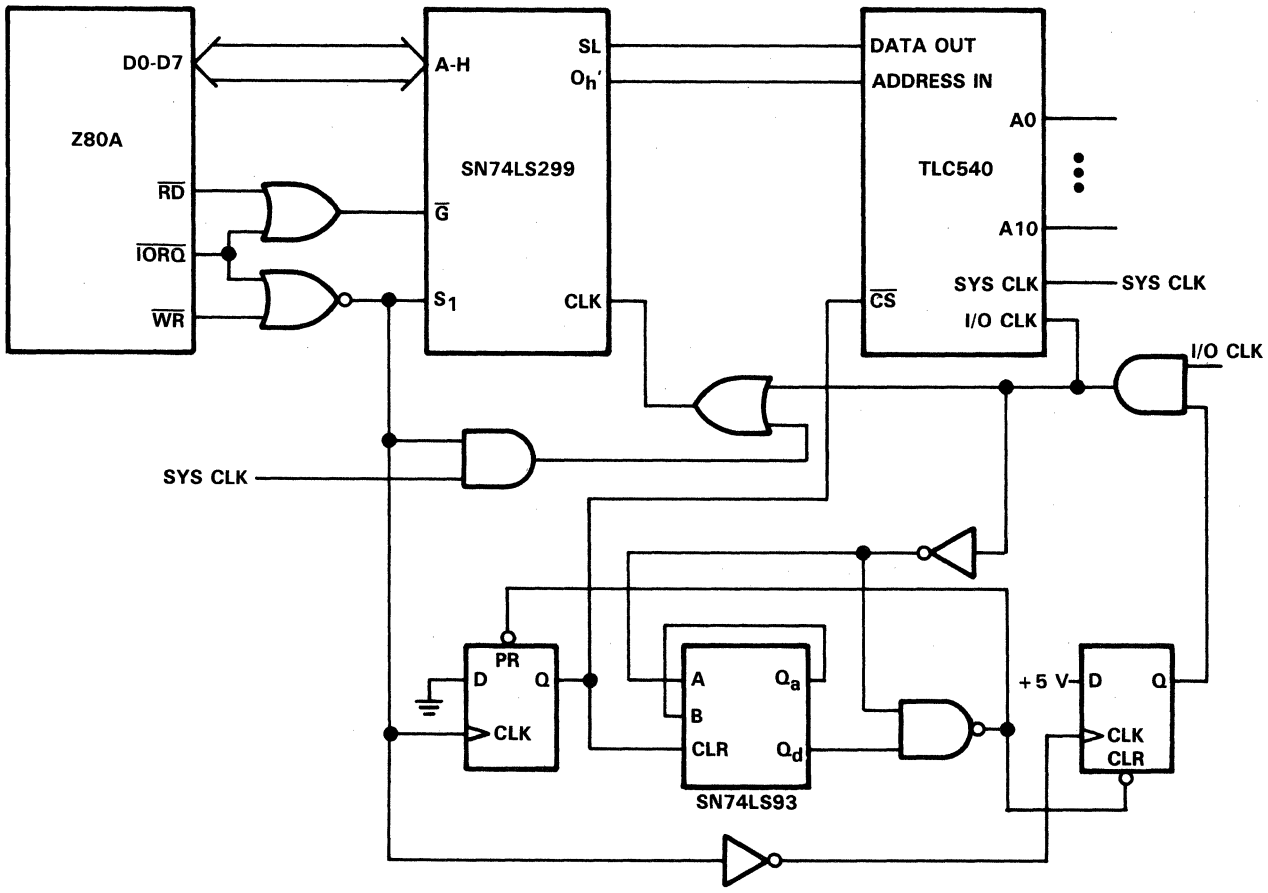


Figure 11-165. Z80A to TLC540 Interface Circuit Diagram

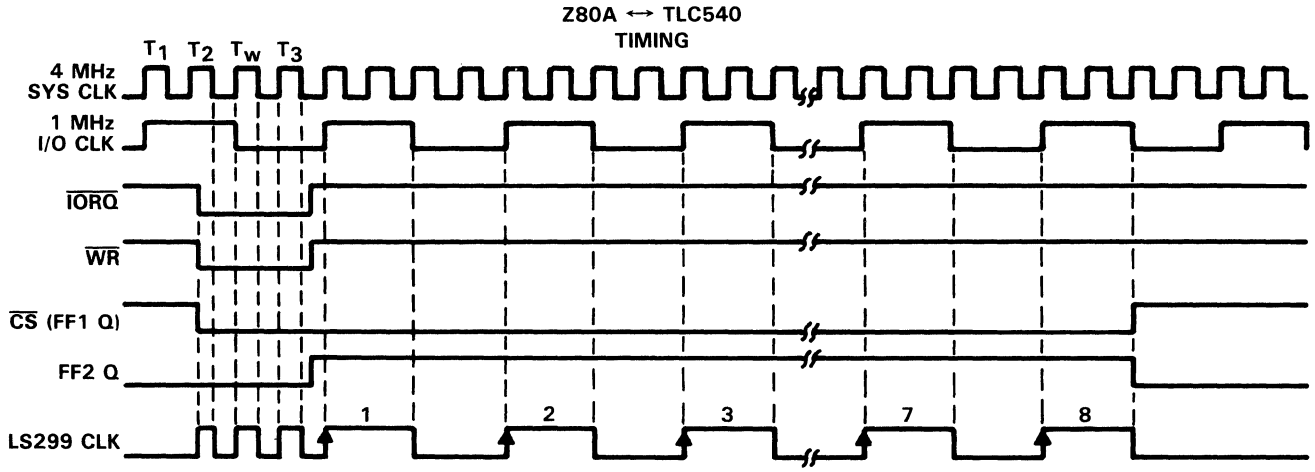


Figure 11-166. Z80A to TLC540 Interface Timing Diagram

Interface 2

The circuit diagram for Interface 2 shows the software controlled TLC540 to Z80A interface and is shown in Figure 11-167. Circuit timing is shown in Figure 11-168.

Execution of an IN instruction causes the $\overline{RD}$ line and the $\overline{IORQ}$ line to become active to shift an address bit into the TLC540 device and a data bit out of the TLC540 device. $\overline{CS}$ is brought low by latching in a low from address bit A0 on the positive going edge of the $\overline{WR}$ signal. A simple program segment that shifts out a new analog multiplexer address while also shifting in previous conversion results is shown in the software listing that follows.

This program segment uses the B register to store the conversion result, the C register as a bit counter, and the D register to hold the analog multiplexer address. The analog multiplexer address is shifted left out of the D register; therefore, the 4-bit address must be placed in the most significant 4-bits of the byte. Conversion results are read in one bit at a time and then shifted left to the proper position in the B register. Sampling of the addressed input begins at the falling edge of the fourth I/O clock pulse and continues until the falling edge of the eighth I/O clock pulse starts the time conversion. Conversion requires 36 system clock cycles; therefore, an appropriate software delay must be included. The amount of the delay depends on the system clock frequency. If a new multiplexer address is shifted in before a conversion has been completed, the ongoing conversion will be aborted and a new conversion cycle will begin at the eighth falling edge of the I/O clock. $\overline{CS}$ is brought high after the eighth falling edge of the I/O clock to ensure that extraneous noise or glitches on the I/O clock line are not interpreted as the beginning of a new cycle. Using this program segment with the system clock at 4 MHz, it is possible to initiate a new conversion cycle and read the results of the previous conversion in 138 μs.

```
        LD C,08             ; INITIALIZE BIT COUNTER
        LD B,00             ; CLEAR RESULT REGISTER
        OUT (CSLOW),A       ; BRING CHIP SELECT LOW
LOOP    RLC B               ; ROTATE RESULT LEFT
        LD (HL),D           ; LATCH ADDRESS BIT INTO D FF
        IN A. (BIT)         ; READ IN DATA BIT
        AND 01H             ; MASK OFF BIT 0
        OR B                ; OR NEW BIT INTO RESULT REG.
        LD B,A              ; STORE IN RESULT REGISTER
        RLC D               ; SHIFT ADDRESS LEFT
        DEC C               ; DECREMENT BIT COUNTER
        JP NZ,LOOP          ; GET ANOTHER BIT IF NOT ZERO
        OUT (CSHIGH),A      ; BRING CHIP SELECT HIGH
```

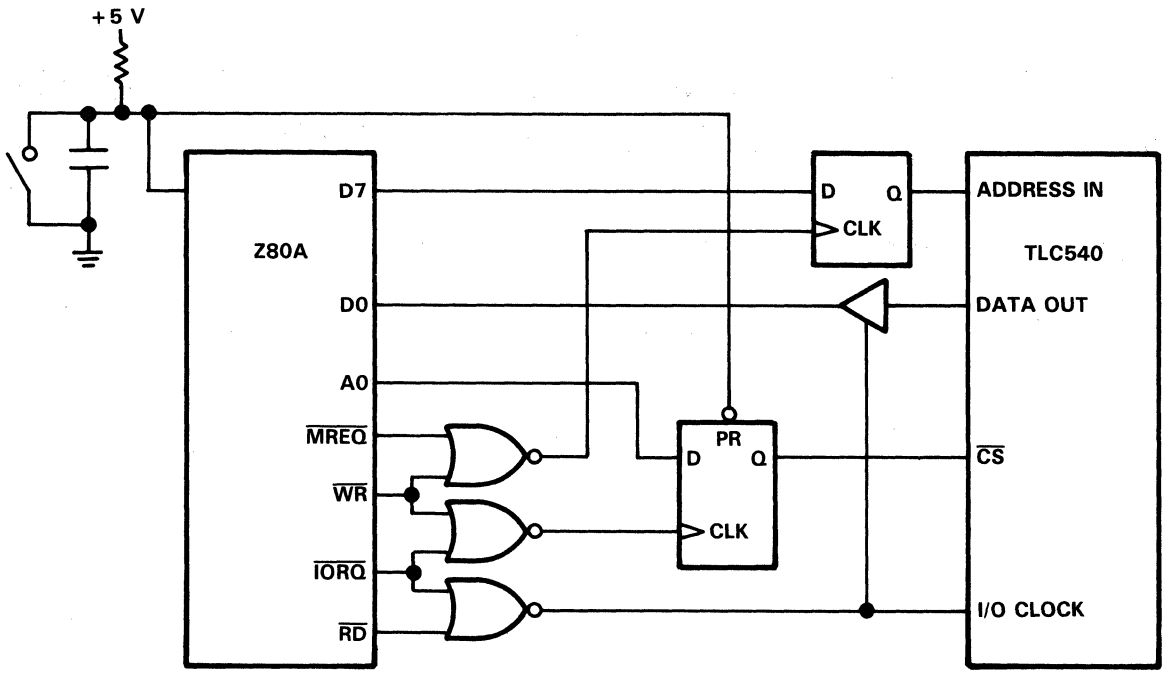


Figure 11-167. Z80A to TLC540 Interface Circuit Diagram

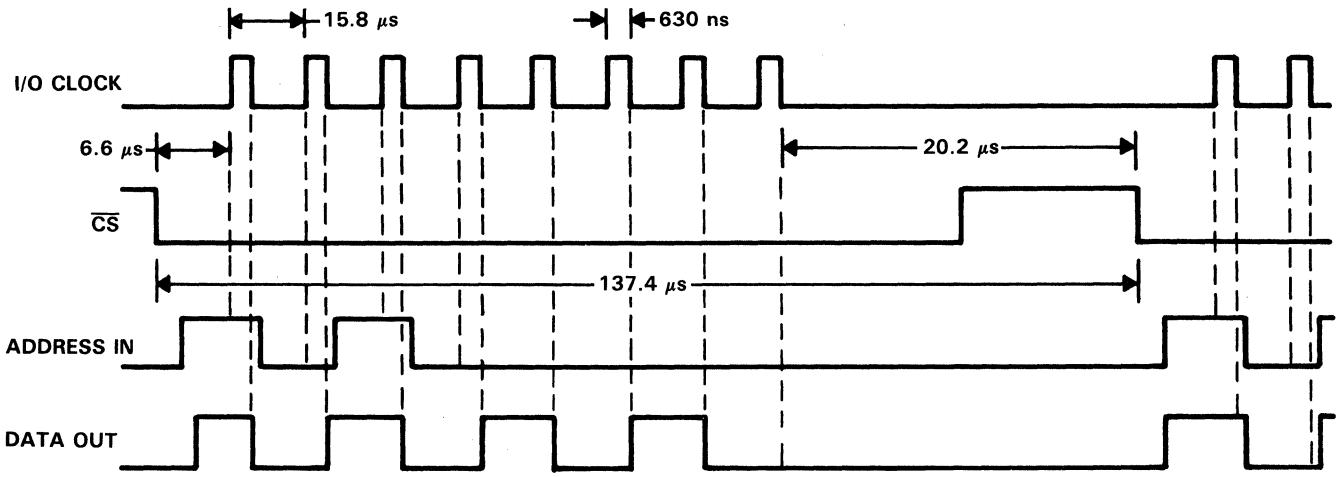


Figure 11-168. Z80A to TLC540 Interface Timing Diagram

INTERFACE FOR THE TLC540 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING THE 6522 VIA

Interfacing the TLC540 A/D converter to the 6502 microprocessor can be accomplished by several methods. This application presents the design of an interface using the 6522 VIA. A method using TTL gates is described in the next application. Cost and performance are the basic trade-offs between the two designs. The 6522 device interface is faster, but the TTL method costs less.

Principles of Operation

The interface circuit diagram is shown in Figure 11-169. Timing for a data read cycle and an address write cycle is shown in Figures 11-170 and 11-171, respectively. A software listing that initializes the 6522 device is shown below. Interface control software is also listed below.

The interface makes use of the serial port available on port B pins CB1 and CB2. Since the serial port is not capable of full duplex communication, the port is configured to function as an output port for the address write cycle and as an input port during the data read cycle. This requires the use of a SN74LS126 3-state buffer. The D-type flip-flops are used to delay the I/O clock to ensure that the set up and hold times for shifting data in and out are met. Port B pins PB0 and PB1 are used to generate $\overline{CS}$ and the output enable signal for the 3-state buffer.

A data conversion cycle begins by bringing $\overline{CS}$ low. This is accomplished by writing a low to PB0. The analog multiplexer address is shifted out by writing to the SR register of the 6522. A delay loop is inserted to wait until the

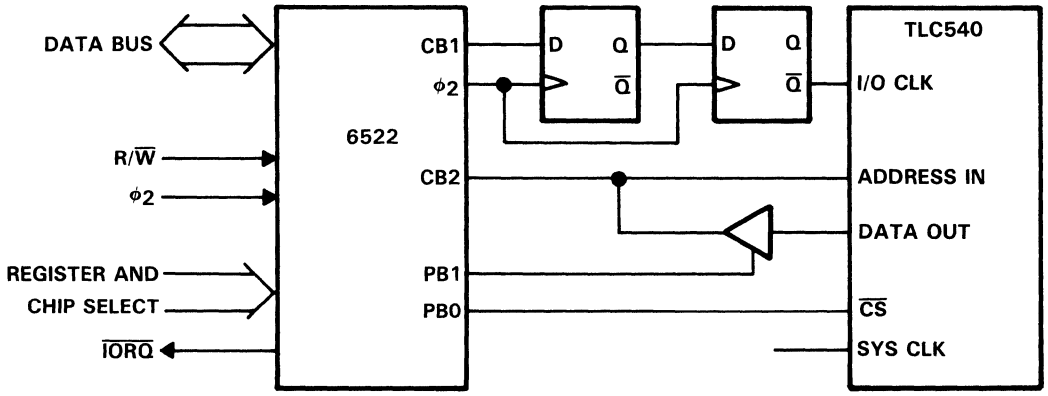


Figure 11-169. 6502 to TLC540 Interface Circuit Diagram (6522 VIA)

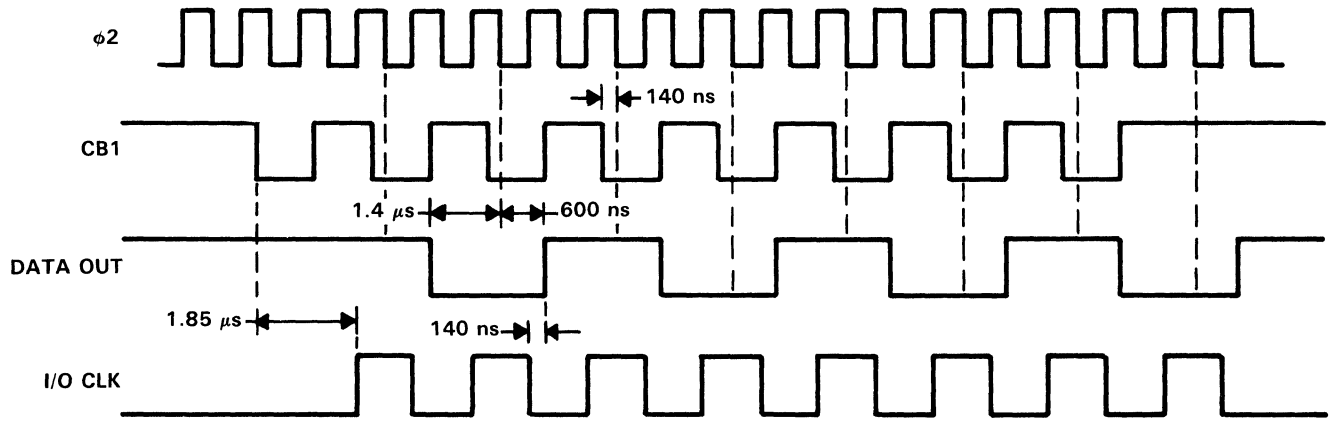


Figure 11-170. 6522 to TLC540 Data Read Cycle Timing Diagram

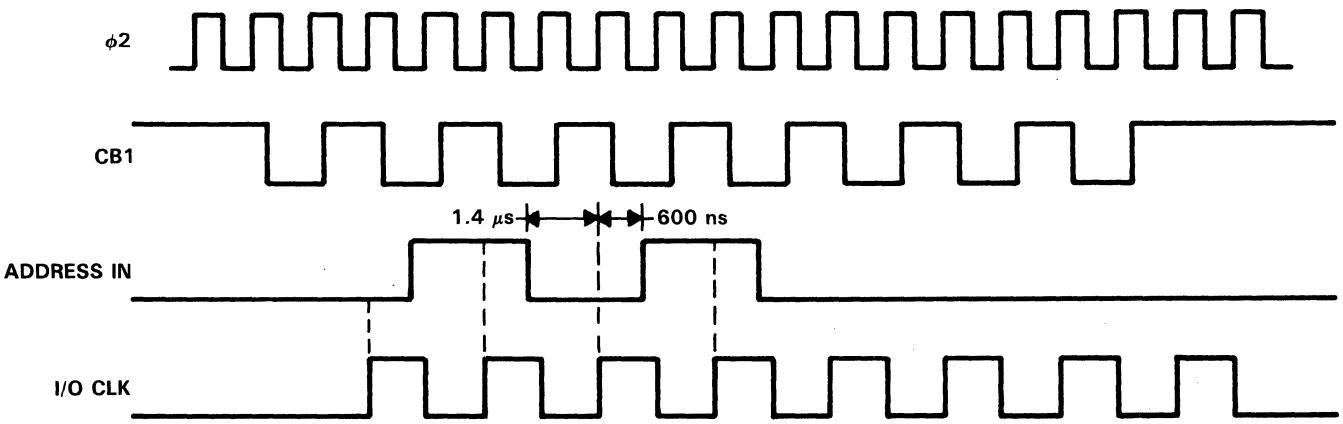


Figure 11-171. 6502 to TLC540 Address Write Cycle Timing Diagram (6522 VIA)

multiplexer address has been shifted out. The serial port is then configured as an input port in order to shift in the A/D conversion results. The output of the 3-state buffer is enabled by writing a high to PB1, and data is shifted into the SR register of the 6522. Again, a delay loop is included to wait until the data is shifted in. $\overline{CS}$ is then brought high, and the 3-state buffer is disabled, completing one data acquisition cycle in 55 μs.

```
;                REGISTER ASSIGNMENTS
;
ORB              .EQU 0000H
DDRB             .EQU 0002H
SR               .EQU 000AH
ACR              .EQU 000BH
PCR              .EQU 000CH
IFR              .EQU 000DH
IER              .EQU 000EH
;
;
                 LDA  #$03          ;
                 STA  DDRB          ; INITIALIZE PORT B I/O PINS
                 LDA  #$01          ;
                 STA  ORB           ; BRING CHIP SELECT HIGH
                 LDX  #$00          ; INITIALIZE MUXADDRESS


                 LDA  #$18          ; SHIFT OUT ON PHI 2
                 STA  ACR           ;
                 LDA  #$00          ;
                 STA  ORB           ; DISABLE DATA OUT, BRING /CS LOW
                 STX  R             ; SHIFT OUT MUXADDRESS TO 540
                 LDY  #$02          ; LOAD DELAY LOOP COUNTER
DELAY1           DEY                ; DECREMENT DELAY COUNTER
                 BNE  DELAY1        ; BRANCH IF NOT ZERO
                 NOP                ;
                 LDX  #$02          ;
                 LDA  #$08          ;
                 STA  ACR           ; SHIFT IN ON PHI 2
                 STX  ORB           ; ENABLE OUTPUT OF 74LS126
                 LDA  SR            ; DUMMY LOAD TO SHIFT RESULTS IN
                 LDY  #$03          ; LOAD DELAY LOOP COUNTER
DELAY2           DEY                ; DECREMENT DELAY LOOP COUNTER
                 BNE  DELAY2        ; BRANCH IF NOT ZERO
                 LDA  #$01          ;
                 STA  ORB           ; DISABLE DATA OUT, BRING /CS HIGH
                 LDA  SR            ; READ CONVERSION RESULTS INTO 6502
```

INTERFACE FOR THE TLC540 DEVICE TO THE ROCKWELL MICROPROCESSOR USING TTL GATES

This application shows an interface between the 6502 microprocessor and the TLC540 A/D converter using TTL gates. The previous application showed an interface between these same two parts using the 6522 VIA. Cost and performance are the basic trade-offs between the two designs. The 6522 device interface is faster, but the TTL method costs less.

Principles of Operation

The basic premise of the interface circuit shown in Figure 11-172 is that all timing control signals are generated under the control of software. Circuit timing is shown in Figure 11-173 and interface control software is listed below.

A data conversion cycle is initiated by bringing $\overline{CS}$ low. This is accomplished by latching a low into the D-type flip-flop from address line A1 on the positive edge of system clock Phi 2. Address bit A14 is used as a gating signal to prevent the TLC540 device from being inadvertently selected during normal program execution. After $\overline{CS}$ is brought low, I/O clock pulses shift in the multiplexer address while shifting out the previous conversion results. The I/O clock is enabled by gating the positive going pulse of Phi 2 to the TLC540 I/O CLK input. This gating occurs by addressing a location so A15 is high. The high on A15 also enables the 3-state buffer output onto the data bus. Address bit A0 determines whether the multiplexer address bit being written is a high or a low. This multiplexer address bit is shifted into the TLC540 device on the positive edge of Phi 2.

Once the data is loaded into the accumulator, it is rotated into the carry bit and then rotated into memory. $\overline{CS}$ is brought high again by writing a high into the D-type flip-flop by placing a high on address bit A1. This cycle can be completed every 172 μs.

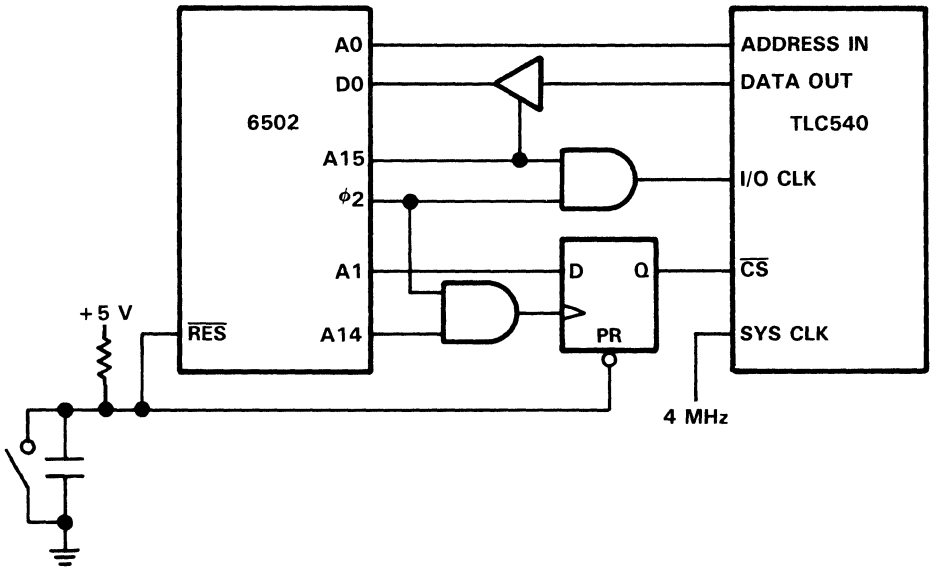


Figure 11-172. 6502 to TLC540 Interface Circuit Diagram (TTL Gates)

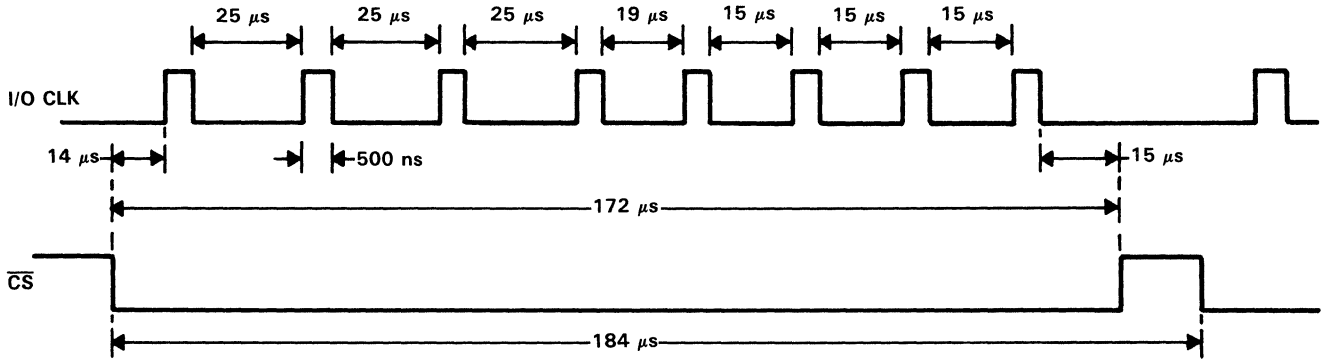


Figure 11-173. 6502 to TLC540 Interface Timing Diagram (TTL Gates)

This interface circuit uses an address decoding scheme that requires a minimum of decoding hardware. Small modifications of the address decoding scheme may be necessary in order to fit the interface to a particular application.

```
CSLOW        .EQU 4000H
CSHIGH       .EQU 4002H
ADDLOW       .EQU 8000H
ADDHIGH      .EQU 8001H
MUXADDRESS   .EQU 0000H
RESULT       .EQU 0001H
;
;
;
             STA  CSLOW        ; BRING /CS LOW
             LDX  #$04         ; SET BIT COUNTER FOR FIRST 4 BITS
LOOP1:       ROL  MUXADDRESS   ; ROTATE MUXADDRESS BIT INTO CARRY
             BCS  HIGH         ; BRANCH IF BIT IS SET
             LDA  ADDLOW       ; WRITE OUT A LOW ON A0, CLOCK DATA IN
             JMP  CONTINUE     ; SKIP NEXT INSTRUCTION
HIGH:        LDA  ADDHIGH      ; WRITE OUT A HIGH ON A0, CLOCK DATA IN
CONTINUE:    ROR  A            ; ROTATE DO INTO CARRY
             ROL  RESULT       ; ROTATE CARRY INTO RESULT
             DEX               ; DECREMENT BIT COUNTER
             BNE  LOOP1        ; GO BACK FOR ANOTHER BIT
             LDX  #$04         ; SET COUNTER FOR SECOND 4 BITS
LOOP2:       LDA  ADDLOW       ; READ IN DATA BIT
             ROR  A            ; ROTATE INTO CARRY
             ROL  RESULT       ; ROTATE CARRY INTO RESULT
             DEX               ; DECREMENT BIT COUNTER
             BNE  LOOP2        ; GET ANOTHER BIT
             STA  CSHIGH       ; BRING /CS HIGH
```

INTERFACE FOR TLC540 AND TLC541 DEVICES TO THE MOTOROLA 6805 MICROPROCESSOR

This application describes techniques for using software controlled interfaces between the TLC540 and TLC541 devices and the 6805 microprocessor. Interfaces for the 6805 microprocessor to the TLC540 and TLC541 devices may be accomplished using either of two methods:

1. Generating all necessary control signals under software control by toggling the output port pins
2. Using the serial peripheral interface (SPI) to generate necessary control signals for data transfer.

The TLC540 and TLC541 devices are particularly well suited for use with the SPI, however, not all 6805 microprocessors include the SPI on the chip. Therefore, the software controlled interface has the advantage although it is less efficient.

Both the TLC540 and TLC541 devices comprise a complete data acquisition system on a chip. The system includes functions such as an analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and microprocessor-compatible control logic. The four control inputs are $\overline{CS}$, I/O clock, system clock, and address input.

The I/O clock and system clock need no special speed or phase relationship, and are normally used independently. This allows the system clock to run up to 4 MHz for the TLC540 device and up to 2.1 MHz for the TLC541 device. This ensures conversion times of less than 9 and 17 μs, respectively. The I/O clock runs up to 2.048 MHz and 1.1 MHz, respectively, to allow a maximum data transfer rate.

Principles of Operation

The circuit diagram for the software controlled 6805 microprocessor to TLC540 and TLC541 device interface is shown in Figure 11-174. Circuit timing is shown in Figure 11-175. The software controlled interface makes use of four pins on port A of the 6805 microprocessor. Three of these pins are used as outputs to generate the $\overline{CS}$, I/O clock and, multiplexer address inputs. The remaining pin is used as an input to receive the conversion results from the

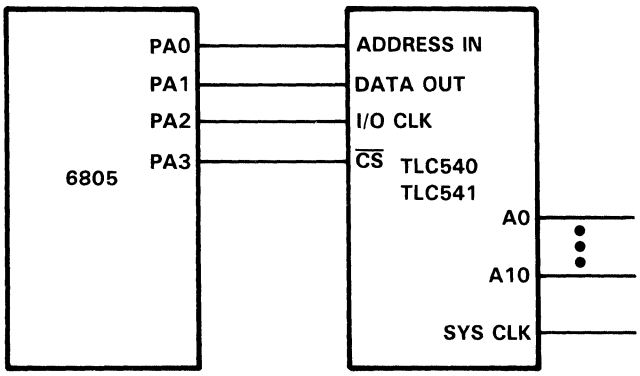


Figure 11-174. 6805 to TLC540 and TLC541 Interface Circuit Diagram

TLC540 and TLC541 devices. A short program segment which can be used to initialize the input/output pins is listed below.

A program listing which controls the actual transfer of data is also given below. This program block sends out the 4-bit analog multiplexer address that is shifted into the TLC540 and TLC541 devices on the first four I/O clock rising edges. Sampling of the addressed input begins at the falling edge of the fourth I/O clock and continues until the falling edge of the eighth I/O clock occurs. Conversion requires 36 clock cycles of the system clock, which can run at up to 4 MHz to allow conversion in only 9 μs. Conversion results are shifted out of the TLC540 and TLC541 devices on the negative edge of the I/O clock with the program block leaving these results in the accumulator. With the 6805 device running at 5 MHz and the TLC540 device system clock at 4 MHz, one conversion cycle can load an analog multiplexer address and read the results from the previous conversion. This cycle can be completed in 270 μs. All 11 analog inputs can be consecutively converted in 3.25 ms.

```
PORTA        .EQU   0000H
DDRA         .EQU   0004H
MUXADDRESS   .EQU   0010H
             .ORG   0100H

START:       LDA    #0DH            ;
             STA    DDRA            ; INITIALIZE PORT A I/O PINS
             BSET   3,PORTA         ; BRING CHIP SELECT HIGH
             LDA    #0DH            ;
             STA    MUXADDRESS      ; INITIALIZE MULTIPLEXER ADDRESS


             LDX    #04             ; LOAD COUNTER FOR FIRST 4 BITS
             BCLR   3,PORTA         ; BRING CHIP SELECT LOW
;
LOOP1:       ROL    MUXADDRESS      ; ROTATE MUXADD BIT INTO CARRY BIT
             BCS    SET             ; GO TO SET IF MUXADD BIT IS 1
             BCLR   0,PORTA         ; WRITE OUT A 0 TO TLC540 ADDRESS IN
             JMP    SKIP            ; SKIP NEXT INSTRUCTION
SET:         BSET   0,PORTA         ; WRITE OUT A 1 TO TLC540 ADDRESS IN
SKIP:        BSET   2,PORTA         ; BRING I/O CLOCK HIGH
             BRSET  1,PORTA,LABEL1  ; READ DATA BIT INTO CARRY BIT
LABEL1:      ROLA                   ; ROTATE NEW DATA BIT INTO ACCUM
             BCLR   2,PORTA         ; BRING I/O CLOCK LOW
             DECX                   ; DECREMENT COUNTER
             BNE    LOOP1           ; CONTINUE IF COUNTER IS NOT ZERO
;
             LDX    #04             ; LOAD COUNTER FOR LAST 4 DATA BITS
;
LOOP2:       BSET   2,PORTA         ; BRING I/O CLOCK HIGH
             BRSET  1,PORTA,LABEL2  ; READ DATA BIT INTO CARRY BIT
LABEL2:      ROLA                   ; ROTATE NEW DATA BIT INTO RESULT
             BCLR   2,PORTA         ; BRING I/O CLOCK LOW
             DECX                   ; DECREMENT COUNTER
             BNE    LOOP2           ; CONTINUE IF COUNTER IS NOT ZERO
;
             BSET   3,PORTA         ; BRING CHIP SELECT HIGH
```

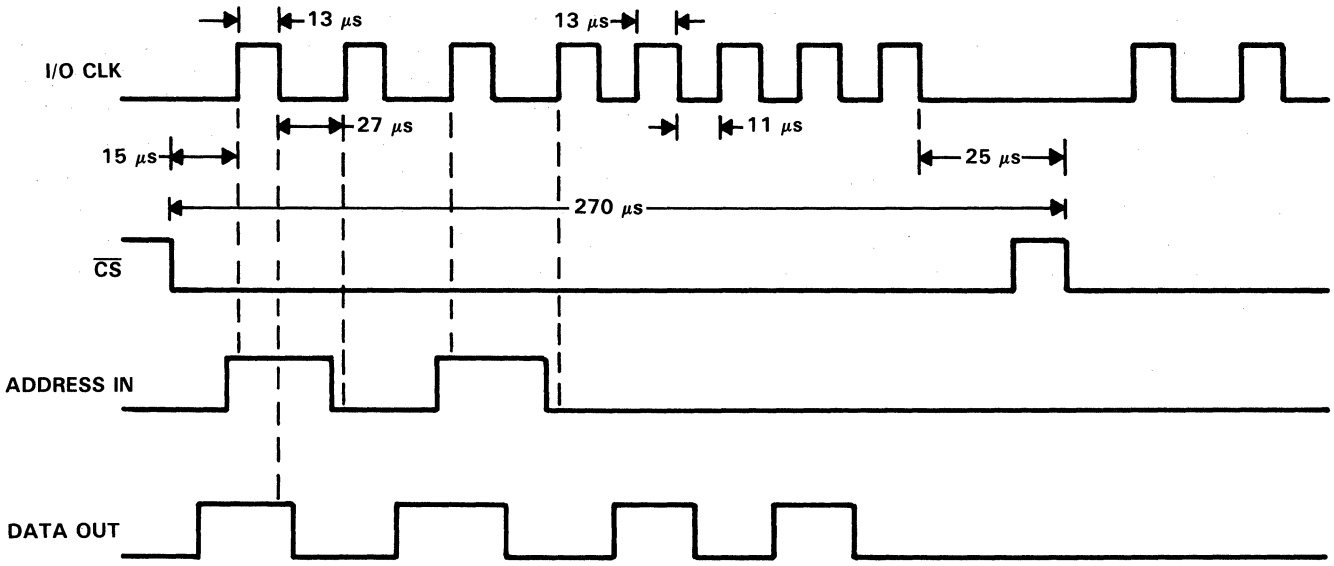
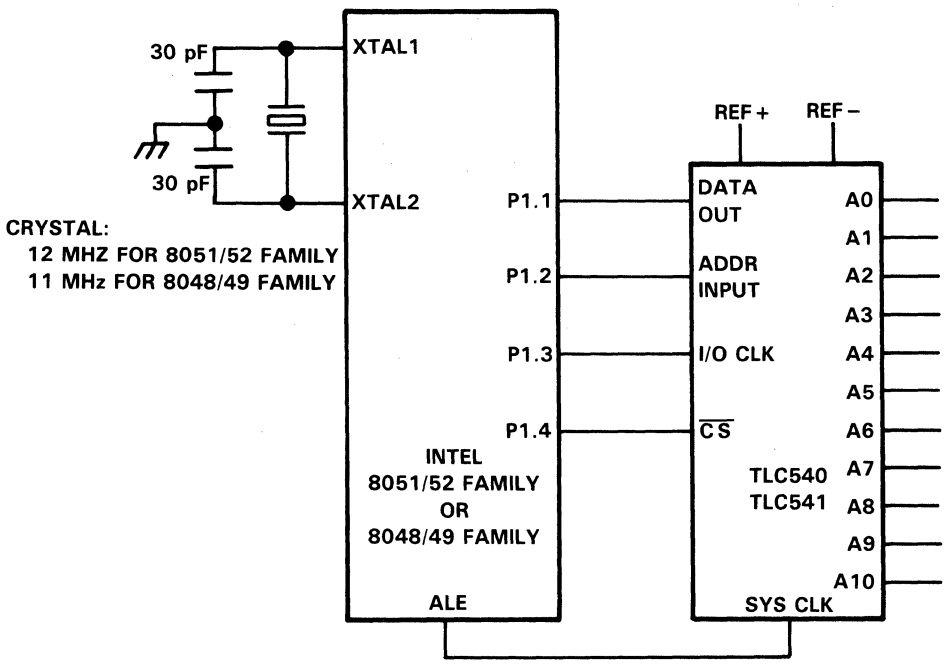


Figure 11-175. 6805 to TLC540 and TLC541 Interface Timing

SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS

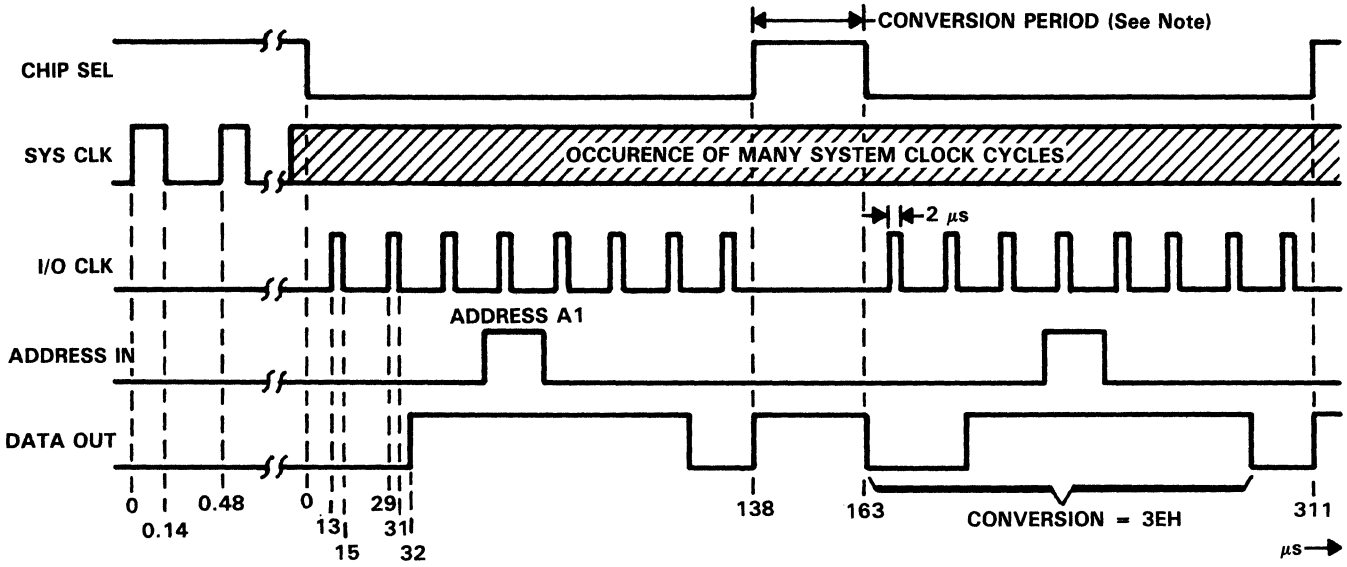
Two types of interfaces are presented. Figures 11-176 and 11-177, and the following software listing supports Interface 1. In this interface, the A/D converter clock signal is derived from the microprocessor ALE clock. In Interface 2, the A/D converter clock signal is derived from the microprocessor crystal oscillator. This interface is supported by Figures 11-178 and 11-179, and a software listing.

These interfaces minimize the hardware and rely extensively on software techniques. Although the amount of hardware and associated cost is reduced, the use of more software increases the time required to load the address into and retrieve the conversion data from the A/D converter. However, the trade-off of minimum hardware versus longer conversion time may benefit many designs.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751H/80C51
INTEL 8048/49 FAMILY: 8048AH/8748H/8035AHL/8049AH/8749H/8039AHL/8050AH/8040AHL/80C49

Figure 11-176. TLC540 and TLC541 — Intel 8051/52 and 8048/49 Microprocessor Interface 1 Diagram



NOTE: Conversion period requires 36 system clock cycles after 8th I/O clock goes low upon clocking in the address.

Figure 11-177. Timing Diagram of an A/D Conversion Cycle for TLC540 and TLC541 to Intel 8051/52 Interface 1

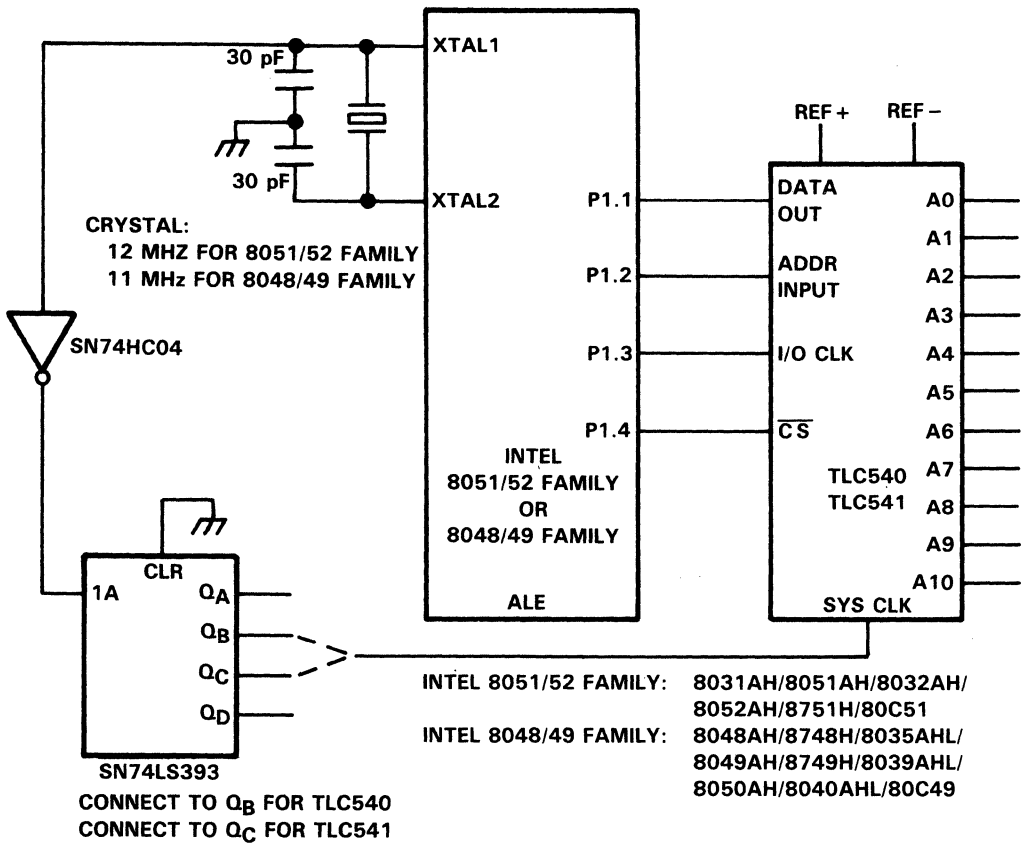
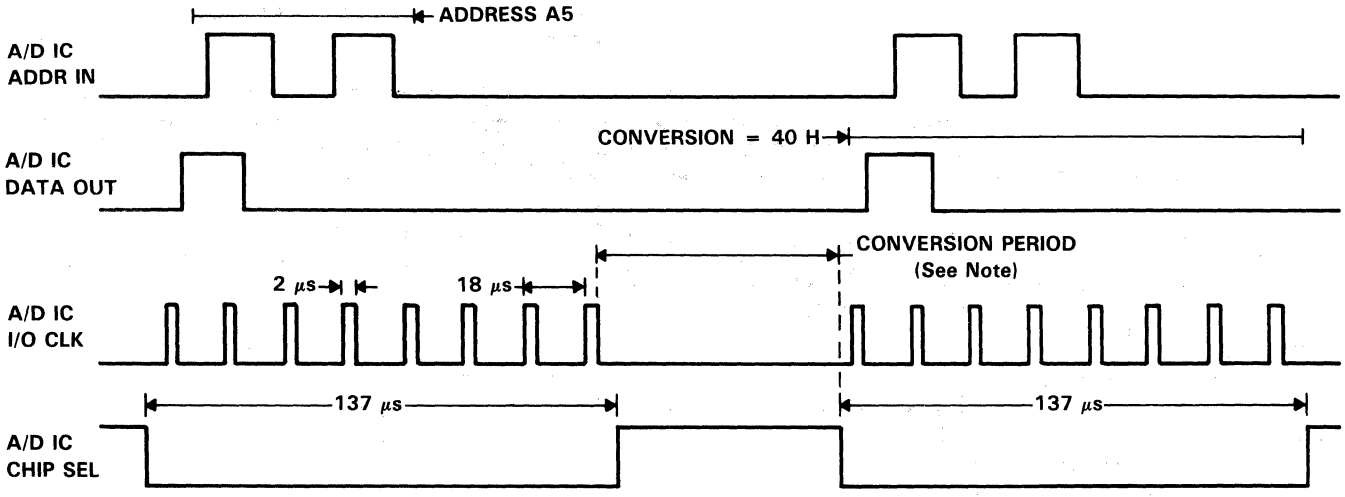


Figure 11-178. TLC540 and TLC541 — Intel 8051/52 and 8048/49 Microprocessor Interface 2 Diagram



NOTE: Conversion period requires 36 system clock cycles after 8th I/O clock goes low upon clocking in the address.

Figure 11-179. Timing Diagram of A/D Conversion Cycle for TLC540 and TLC541 — Intel 8051/52 Interface 2

Circuit — Interface 1 (ALE CLOCK)

The interface shown in Figure 11-176 will always work with the TLC540 device, but will not work with the TLC541 device at the higher microprocessor clock frequencies. Before using the TLC541 device, the designer must verify that the high and low pulse widths of the ALE clock signal meet the requirements of the TLC541 device. These pulse widths are dependent on the microprocessor instruction cycle clock frequency.

Circuit — Interface 2 (CRYSTAL CLOCK)

As shown in Figure 11-178, the system clock for the A/D converter is obtained from the microprocessor crystal oscillator. To assure proper operation of the crystal oscillator, a high impedance buffer must be used to tap the signal from the oscillator. An important detail is that the low and high level input requirements of the buffer must lie within the range of the oscillator signal. This compatibility will prevent missing edge transitions in the A/D converter's system clock signal. In addition, the buffered crystal oscillator signal must be frequency divided to assure that the resulting system clock signal does not exceed the upper frequency limit of the A/D converter. Any convenient divider circuitry may be used for this task.

Timing Diagrams

Figures 11-177 and 11-179 show the timing diagrams for the A/D conversions of Interfaces 1 and 2, respectively. Loading the new address and retrieving the conversion for the previous address requires 137 μs. The conversion period requires 36 system clocks. This time period is longer for the TLC541 device since the microprocessor clock frequency (see software listing) or A/D clock frequency (see software listing) must be lower to satisfy the TLC541 device specifications.

Software

The software listings for Interface 1 and Interface 2 follow. These software programs use a subroutine, ACALL, that simultaneously loads the A/D converter with a new address and retrieves the conversion result for the previous address. This subroutine can be used any time the designer desires to load a new address and retrieve a conversion value. Simultaneous loading and retrieving makes this subroutine very effective for continuous monitoring of A/D converter analog inputs. The subroutine assumes that the new address has been previously placed in the R2 register. Upon completion of the subroutine, the conversion result for the previous address is left in the accumulator.

```
                    ; Software Listing for Intel 8051/52 - TLC540/541 Interface 1
                    ;
0000    C2 93               CLR P1.3        ;Lower I/O clock
0002    7A 10               MOV R2, # 10H   ;Load A/D analog input address. Note
                                            ;that to send address = 1, R2 = 10h.
0004    11 0E               ACALL S540D     ;Load 540 address, assumes the address
                                            ;is currently in R2.
                    ;
```

```
0006    7B 09                MOV R3,#09H      ;This software loop allows a
                                              ;conservative 40 A/D system clocks,
                                              ;since only 36
0008    DB FE       DELAY:   DJNZ R3,DELAY    ;clocks are required to perform
                                              ;conversion, to be emitted from the
                                              ;microprocessor ALE pin
                    ;
000A    7A 10                MOV R2,#10H      ;Load A/D analog input address. Note
                                              ;that to send address = 1, R2 = 10h.
000C    11 0E                ACALL S540D      ;Load new 540 address, assumes this
                                              ;address is in R2; leaves the
                                              ;conversion result for the previous
                                              ;address in A
                    ;
                    ;        Subroutine ACALL
                    ;
000E    7E 08       S540D:   MOV R6,#08H      ;Set bit counter to 8
0010    C2 94                CLR P1.4         ;Lower chip select
0012    C3          S540DL:  CLR C            ;Initialize C = 0
0013    30 91 01             JNB P1.1,S540DI  ;If 540 Data Out = 0; branch
0016    B3                   CPL C            ;540 Data Out = 1; set C = 1
0017    EA          S540DI:  MOV A,R2         ;Get serial buffer
0018    33                   RLC A            ;Shift Data Out bit into serial
                                              ;buffer and shift 540 address
0019    FA                   MOV R2,A         ;Store serial buffer
001A    50 05                JNC S540DWO      ;If 540 address bit = 0; branch
001C    43 90 04             ORL P1,#04H      ;Set 540 branch line to 1
001F    80 03                SJMP S540DWE     ;Go and raise the I/O clock
0021    53 90 FB    S540DWO: ANL P1,#FBH      ;Set 540 address line to 0
0024    00          S540DWE: NOP              ;Allow address line to setup
0025    B2 93                CPL P1.3         ;Raise I/O clock
0027    00                   NOP              ;Delay to slow I/O clock
0028    C2 93                CLR P1.3         ;Lower I/O clock
002A    DE E6                DJNZ R6,S540DL   ;Do all 8 bits
002C    B2 94                CPL P1.4         ;Raise chip select
002E    EA                   MOV A,R2         ;Get serial buffer
                    ;
0023    33                   RLC A            ;6543210C 7; b7 is now in carry
0024    33                   RLC A            ;543210C7 6; b6 is now in carry
0025    92 E1                MOV ACC.1,C      ;54321067 6; put b6 into ACC.1
0027    A2 E2                MOV C,ACC.2      ;54321067 0; put b0 into C
0029    33                   RLC A            ;43210670 5; b5 is now in carry
002A    92 E3                MOV ACC.3,C      ;43215670 5; put b5 into ACC.3
002C    A2 E4                MOV C,ACC.4      ;43215670 1; put b1 into C
002E    33                   RLC A            ;32156701 4; b4 is now in carry
002F    92 E5                MOV ACC.5,C      ;32456701 4; put b4 into ACC.5
0031    A2 E6                MOV C,ACC.6      ;32456701 2; put b2 into C
0033    33                   RLC A            ;24567012 3; b3 is now in carry
0034    92 E7                MOV ACC.7,C      ;34567012 3; put b3 into ACC.7
0036    23                   RL A             ;45670123  ; prepare for SWAP A
0037    C4                   SWAP A           ;01234567  ; bits are ordered
                                              ;correctly
                                              ;conversion result is in accumulator
0038                         END
```

```
                        ;  Software Listing for Intel 8051/52 Family -
                        ;  TC540/541 Serial Interface 2
                        ;
0000    74 0A           SR540L:     MOV A,#0AH          ;A/D IC address of 5 in this example
                        ;
                        ;The serial port will send 0A(00001010) with the least
                        ;significant bit first. Therefore, the A/D IC will see
                        ;(01010000), which will load an address of 5 into the control
                        ;register.
                        ;
0002    C2 97                       CLR P1.7            ;Disable 125
0004    B2 97                       CPL P1.7
0006    C2 96                       CLR P1.6            ;Lower chip select
0008    53 98 ED                    ANL SCON,#EDH       ;Reset REN & TI flags
000B    F5 99                       MOV SBUF,A          ;Send 540 address (LSB FIRST)
000D    30 99 FD        SNDTST:     JNB SCON.1,SNDTST   ;TI flag not set; branch
                                                        ;until transmission is complete
                        ;
                        ;A delay must occur here to allow the A/D IC to complete
                        ;conversion. The delay must llow 36 A/D IC system clock
                        ;cycles to occur.
                        ;
0010    B2 97                       CPL P1.7            :Enable 125
0012    43 98 10                    ORL SCON,#10H       :Set REN
0015    53 98 FE                    ANL SCON,#FEH       :Reset RI
0018    30 98 FD        RCVTST:     JNB SCON.0,RCVTST   :RI FLAG not set; branch
                                                        :until reception is complete
001B    B2 96                       CPL P1.6            ;Raise chip select
001D    E5 99                       MOV A,SBUF          ;Get SBUF
                        ;
                        ;The serial port read reverses the data conversion bits coming
                        ;to the microprocessor so that they are in the following order:
                        ;b0(1sb),b1,b2,b3,b4,b5,b6,b7(msb). These bits (01234567) along
                        ;with the carry bit (C) in the following instruction comments
                        ;are presented so that the reader will understand the technique,
                        ;which is used to place the bits in their proper order.
                        ;
001F    33                          RLC A               ;6543210C 7; b7 is now in carry
0020    33                          RLC A               ;543210C7 6; b6 is now in carry
0021    92 E1                       MOV ACC.1,C         ;54321067 6; put b6 into ACC.1
0023    A2 E2                       MOV C,ACC.2         ;54321067 0; put b0 into C
0025    33                          RLC A               ;43210670 5; b5 is now in carry
0026    92 E3                       MOV ACC.3,C         ;43215670 5; put b5 into ACC.3
0028    A2 E4                       MOV C,ACC.4         ;43215670 1; put b1 into C
002A    33                          RLC A               ;32156701 4; b4 is now in carry
002B    92 E5                       MOV ACC.5,C         ;32456701 4; put b4 into ACC.5
002D    A2 E6                       MOV C,ACC.6         ;32456701 2; put b2 into C
002F    33                          RLC A               ;24567012 3; b3 is now in carry
0030    92 E7                       MOV ACC.7,C         ;34567012 3; put b3 into ACC.7
0032    23                          RL A                ;45670123 ; prepare for SWAP A
0033    C4                          SWAP A              ;01234567 ; bits are ordered
                                                        ;correctly
                                                        ;conversion result is in accumulator
0034                                END
```

Hardware

The circuit for Interface 1, which obtains the clock signal from the ALE pin, is shown in Figure 11-180. The circuit for Interface 2, which obtains the clock signal from the crystal oscillator, is illustrated in Figure 11-182. The signal at the microprocessor TXD pin must be inverted so the communication protocols for the microprocessor and the A/D converter are compatible. Use of a SN74LS125 3-state buffer allows the microprocessor serial port to be used for both transmission and reception. Although this method does not permit simultaneous loading of a new address while retrieving the conversion of a previously loaded address, the time loss is small. This is because the serial port can quickly load an address and retrieve the resulting conversion.

Timing Diagrams

Figures 11-181 and 11-183 show the timing diagrams for an A/D conversion for each of the two circuits. Loading the address, waiting for conversion, and retrieving the conversion result requires 56 μs for Interface 1 and 48 μs for Interface 2 when using the TLC540 device. This time period is longer for the TLC541 device because the system clock frequency must be lower for this device.

Software

The software routines for Interface 1 and Interface 2 were listed earlier. The serial port mode 0 is used. If desired, the software can be incorporated into a subroutine so the designer can address the software with a simple subroutine call. Careful attention must be exercised when placing the address bits in the serial buffer since the serial port sends the least significant bit first and the A/D converter accepts this bit as the most significant bit of the address. A similar process occurs when the serial port receives the conversion result.

SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8048 AND 8049 MICROPROCESSORS

Hardware

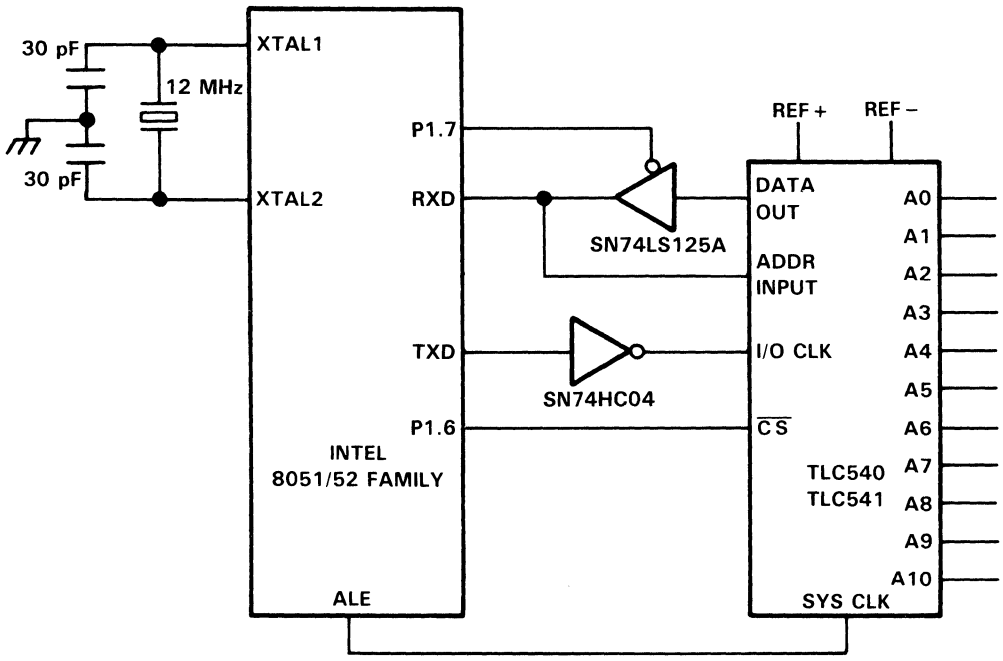
Figures 11-176 and 11-178 show the circuit diagrams for this application. Also refer to the SOFTWARE INTERFACE FOR TLC540 and TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS application.

Timing Diagram

Figure 11-184 of this application shows the timing of an A/D conversion. Loading the new address and retrieving the conversion for the previous address requires 250 μs. The conversion period requires 36 system clocks, however, this period is longer for the TLC541 device because the system clock frequency must be lower for this device.

Software

Software listings are attached below. Also refer to the SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS application.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751H/80C51
CONNECT TO Q_B FOR TLC540
CONNECT TO Q_C FOR TLC541

Figure 11-180. TLC540 and TLC541 — Intel 8051/52 Microprocessor Interface 1 Diagram (Clock Signal from ALE)

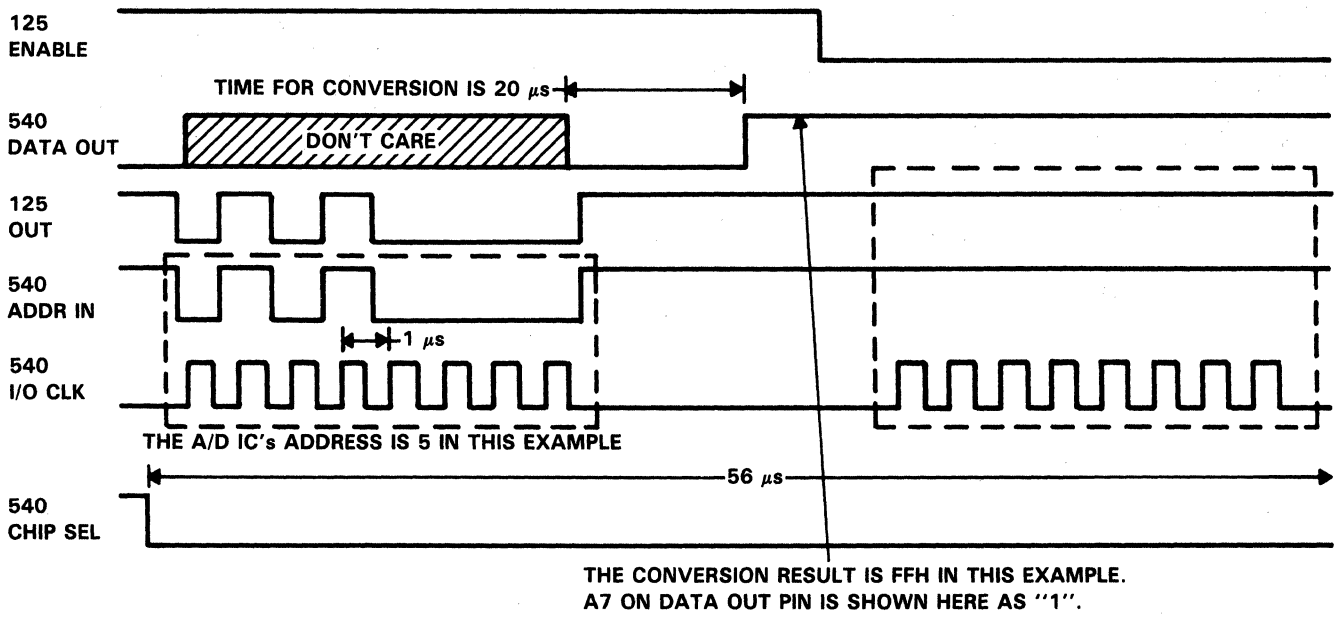
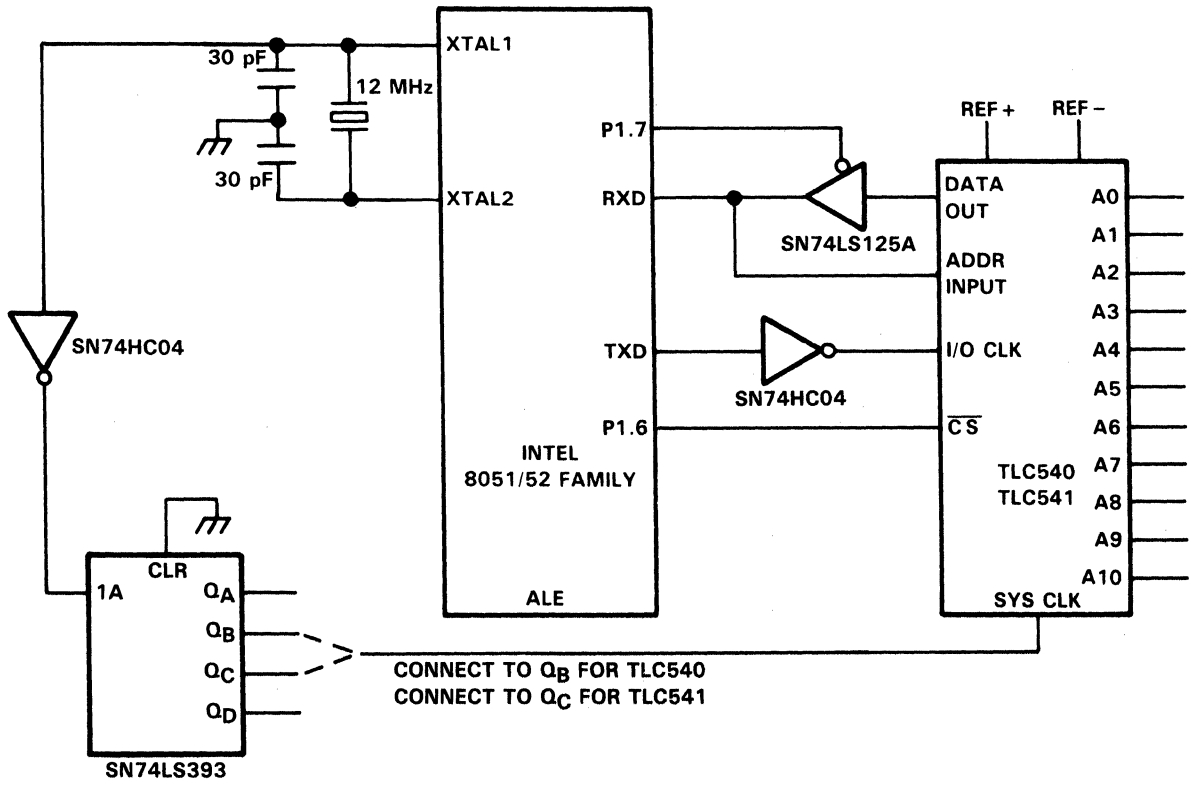


Figure 11-181. Timing Diagram for an A/D Conversion for the TLC540 and TLC541 — Intel 8051/52 Microprocessor Serial Port Interface 1



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751H/80C51

Figure 11-182. TLC540 and TLC541 — Intel 8051/52 Microprocessor Serial Port Interface 2 Diagram (Clock Signal from Crystal Oscillator)

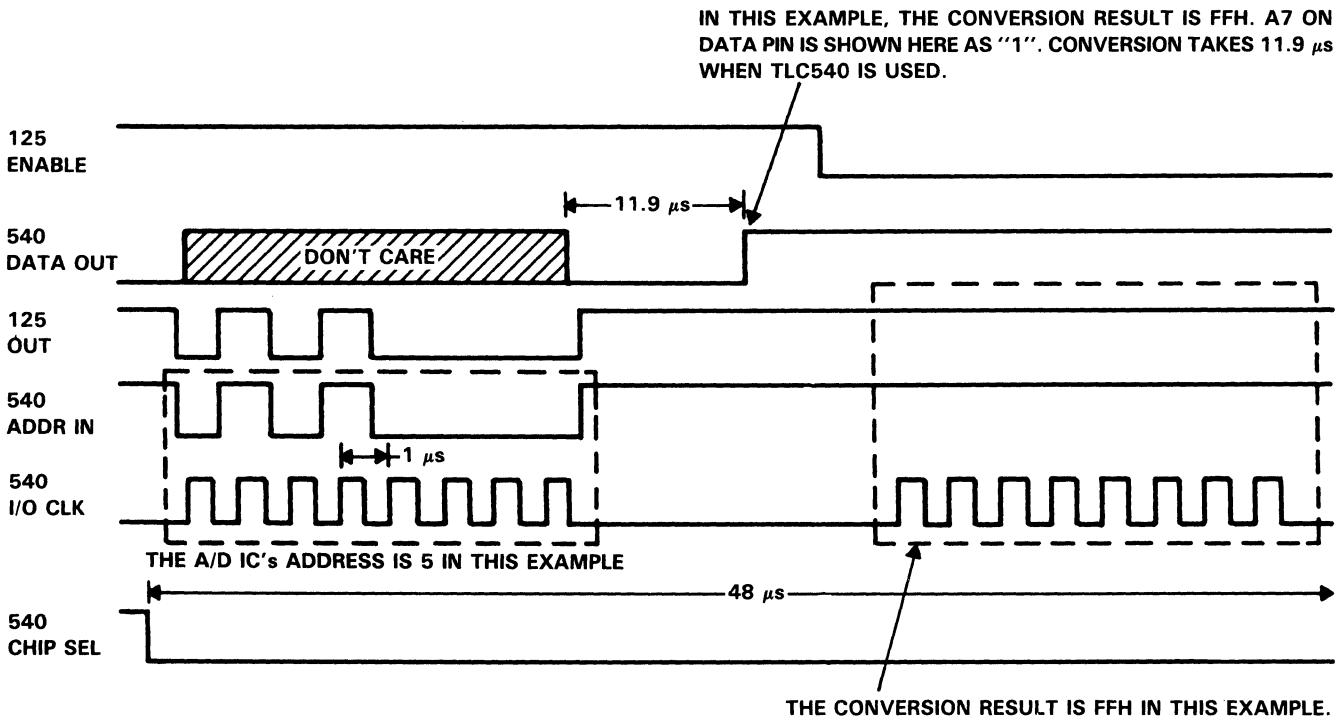
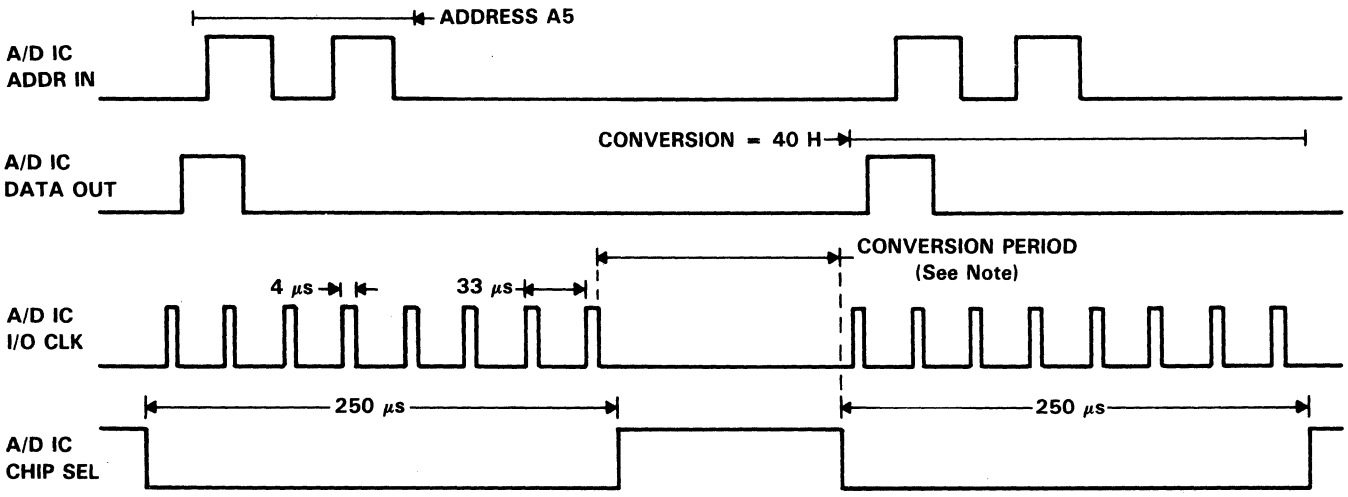


Figure 11-183. Timing Diagram for an A/D Conversion for the TLC540 and TLC541 — Intel 8051/8052 Microprocessor Serial Port Interface 2



NOTE: Conversion period requires 36 system clock cycles after 8th I/O clock goes low upon clocking in the address.

Figure 11-184. Timing Diagram of A/D Conversion Cycle for TLC540 and TLC541 — Intel 8048/49 Microprocessor Interface 2

```
                        ;  Software Listings for Intel 8048/49 Family -
                        ;  TLC540/541 Interface 1
                        ;
0000    99 F7                       ANL P1,#F7H         ;Lower I/O clock
0002    B8 10                       MOV R0,#10H         ;Load A/D analog input address. Note
                                                        ;that to send address = 1, R2 = 10h.
0004    14 0A                       CALL S540D          ;Load 540 address, assumes the address
                                                        ;is currently in R0. Note that to send
                                                        ;address = 1, R0 = 10h.
                        ;
0006    BB 13                       MOV R3,#13H         ;This software loop allows a
                                                        ;conservative 40 A/D system clocks,
                                                        ;since only 36
0008    EB 08           DELAY:      DJNZ R3,DELAY       ;clocks are required to perform
                                                        ;conversion, to be emitted from the
                                                        ;microprocessor ALE pin
                        ;
000A    B8 10                       MOV R0,#10H         ;Load A/D analog input address. Note
                                                        ;that to send address = 1, R2 = 10h.
000C    14 0A                       CALL S540D          ;Load new 540 address, assumes this
                                                        ;address is in R0; leaves the
                                                        ;conversion result for the previous
                                                        ;address in A
                        ;
                        ;           Subroutine S540D
                        ;
000E    BA 08           S540D:      MOV R2,#08H         ;Set bit counter to 8
0010    99 EF                       ANL P1,#EFH         ;Lower chip select
0012    97              S540DL:     CLR C               ;Initialize C = 0
0013    09                          IN A,P1             ;Get Port 1
0014    37                          CPL A               ;Complement accumulator
0015    32 17                       JB1 S540DI          ;If 540 Data Out = 0; branch
0017    A7                          CPL C               ;540 Data Out = 1; set C = 1
0018    F8              S540DI:     MOV A,R0            ;Get serial buffer
0019    F7                          RLC A               ;Shift Data Out bit into serial
                                                        ;buffer and shift 540 address
                                                        ;bit into C
001A    A8                          MOV R0,A            ;Store serial buffer
001B    E6 20                       JNC S540DWO         ;If 540 address bit = 0; branch
001D    89 04                       ORL P1,#04H         ;Set 540 branch line to 1
001F    04 21                       JMP S540DWE         ;Go and raise the I/O clock
0021    99 FB           S540DWO:    ANL P1,#FBH         ;Set 540 address line to 0
0023    00              S540DWE:    NOP                 ;Allow address line to setup
0024    89 08                       ORL P1,#08H         ;Raise I/O clock
0026    00                          NOP                 ;Delay to slow I/O clock
0027    99 F7                       ANL P1,#F7H         ;Lower I/O clock
0029    EA 11                       DJNZ R2,S540DL      ;Do all 8 bits
002B    89 10                       ORL P1,#10H         ;Raise chip select
002D    F8                          MOV A,R0            ;Get serial buffer
002E    83                          RET
```

```
                        ;  Software Listings for Intel 8048/49 Family -
                        ;  TLC540/541 Interface 2
                        ;
0000    99 F7                       ANL P1,#F7H         ;Lower I/O clock
0002    B8 10                       MOV R0,#10H         ;Load A/D analog input address. Note
                                                        ;that to send address = 1, R2 = 10h.
0004    14 06                       CALL S540D          ;Load 540 address, assumes the address
                                                        ;is currently in R0. Note that to send
                                                        ;address = 1, R0 = 10h.
                        ;
                        ;A delay must occur here to allow the A/D IC to complete
                        ;conversion. The delay must allow 40 A/D IC system clock
                        ;cycles to occur.
                        ;
0006    B8 10                       MOV R0,#10H         ;Load A/D analog input address. Note
                                                        ;that to send address = 1, R2 = 10h.
0008    14 06                       CALL S540D          ;Load new 540 address, assumes this
                                                        ;address is in R0; leaves the
                                                        ;conversion result for the previous
                                                        ;address in A
                        ;
                        ;           Subroutine S540D
                        ;
000A    BA 08           S540D:      MOV R2,#08H         ;Set bit counter to 8
000C    99 EF                       ANL P1,#EFH         ;Lower chip select
000E    97              S540DL:     CLR C               ;Initialize C = 0
000F    09                          IN A,P1             ;Get Port 1
0010    37                          CPL A               ;Complement accumulator
0011    32 14                       JB1 S540DI          ;If 540 Data Out = 0; branch
0013    A7                          CPL C               ;540 Data Out = 1; set C = 1
0014    F8              S540DI:     MOV A,R0            ;Get serial buffer
0015    F7                          RLC A               ;Shift Data Out bit into serial
                                                        ;buffer and shift 540 address
                                                        ;bit into C
0016    A8                          MOV R0,A            ;Store serial buffer
0017    E6 1D                       JNC S540DWO         ;If 540 address bit = 0; branch
0019    89 04                       ORL P1,#04H         ;Set 540 branch line to 1
001B    04 1F                       JMP S540DWE         ;Go and raise the I/O clock
001D    99 FB           S540DWO:    ANL P1,#FBH         ;Set 540 address line to 0
001F    00              S540DWE:    NOP                 ;Allow address line to setup
0020    89 08                       ORL P1,#08H         ;Raise I/O clock
0022    00                          NOP                 ;Delay to slow I/O clock
0023    99 F7                       ANL P1,#F7H         ;Lower I/O clock
0025    EA 0E                       DJNZ R2,S540DL      ;Do all 8 bits
0027    89 10                       ORL P1,#10H         ;Raise chip select
0029    F8                          MOV A,R0            ;Get serial buffer
002A    83                          RET
```

INTERFACE FOR THE TLC549 DEVICE TO THE ZILOG Z80A MICROPROCESSOR

This application describes a technique for interfacing the TLC549 A/D converter to the Z80A microprocessor. The TLC549 device is a complete data acquisition system on a chip. It differs from the TLC540 device since the TLC549 device has one analog input and an on-chip system clock while the TLC540 device has 11 analog inputs and requires an external system clock input. These differences allow the TLC549 device to be packaged in an 8-pin DIP to reduce size and cost. Timing is the same as the TLC540 device except that it does not require an analog multiplexer address since it is a single channel data acquisition system. The I/O clock may run at any frequency up to 2.048 MHz.

Principles of Operation

The circuit diagram for the TLC549 device to Z80A microprocessor interface is shown in Figure 11-185. The circuit timing is shown in Figure 11-186.

$\overline{CS}$ is brought low by latching a low from address bit A0. Execution of an IN instruction causes $\overline{RD}$ and $\overline{IORQ}$ to become active and generate one I/O clock pulse. A data bit is read before the falling edge of the I/O clock and the falling edge shifts out the next data bit. Sampling of the analog input begins at the falling edge of the fourth I/O clock and continues until the falling edge of the eighth I/O clock. At that time, conversion begins and $\overline{CS}$ is brought high. Since $\overline{CS}$ high disables all inputs and outputs, conversion may proceed. Conversion requires 17 μs. A simple program segment that starts a conversion and reads in previous conversion results is shown in the software listing. If this program segment is placed in a loop, it is possible to initiate a conversion and read previous results in 111 μs.

Figure 11-185 presents a software controlled interface for the Z80A and the TLC549 devices. It is possible to increase performance by introducing additional hardware into the interface. For more description of such an interface, refer to the TLC540 DEVICE INTERFACE FOR THE TLC540 DEVICE TO ZILOG Z80A AND Z80 MICROPROCESSORS application.

```
                LD C,08H            ; Load bit counter
                LD B,00H            ; Initialize result register
                OUT (CSLOW),A       ; Bring chip select low
LOOP            RLC B               ; Rotate result reg. left
                IN A, (BIT)         ; Read in a bit & clock next
                AND 01H             ; Mask off bit 0
                OR B                ; Or new bit with result
                LD B,A              ; Store in results register
                DEC C               ; Decrement bit counter
                JP NZ,LOOP          ; Get another bit if not zero
                OUT (CSHIGH),A      ; Bring chip select high
```

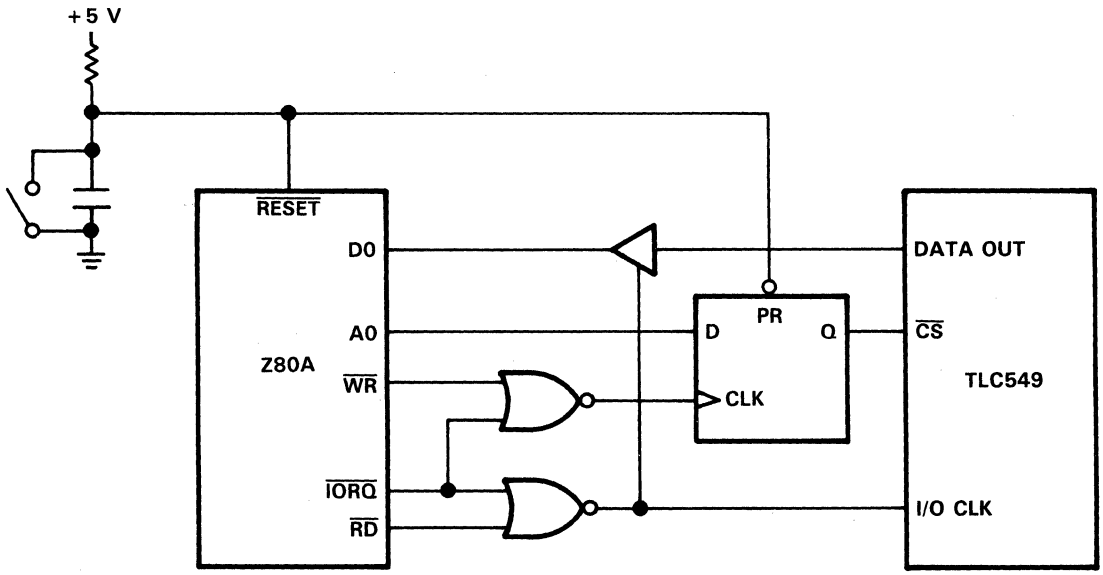


Figure 11-185. Z80A to TLC549 Interface Circuit Diagram

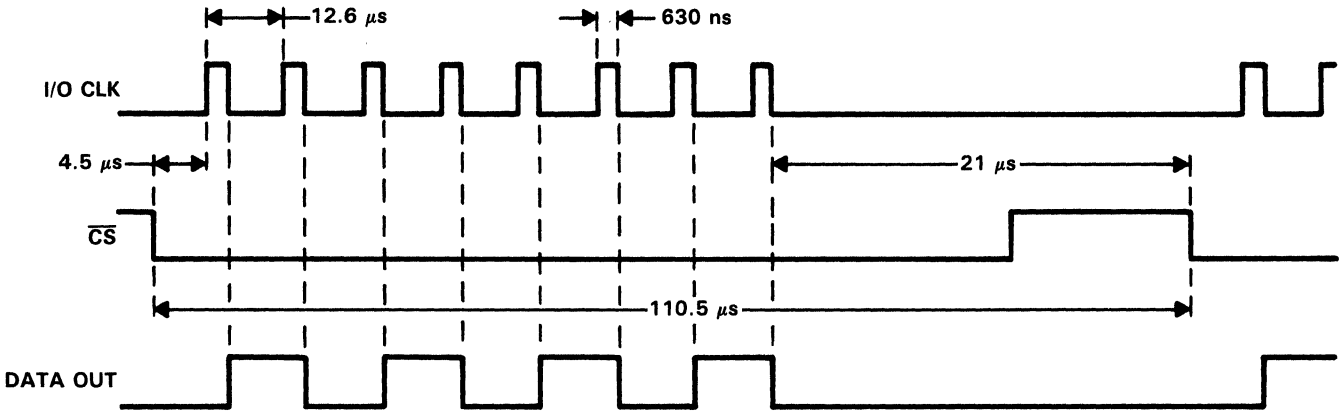


Figure 11-186. Z80A to TLC549 Interface Timing Diagram

INTERFACE FOR THE TLC549 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING TTL GATES

This application presents the design of an interface for the TLC549 A/D converter to the 6502 microprocessor. Interfacing techniques for the TLC549 device are similar to those of the TLC540 A/D peripheral chip. The interface uses a small number of TTL gates similar to the INTERFACE FOR THE TLC540 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING TTL GATES presented in a previous application. Since the TLC549 device converts only one analog input channel, no multiplexer address is required. This reduces the amount of software code and execution time required.

Principles of Operation

The TLC549 device to 6502 microprocessor interface circuit is shown in Figure 11-187. The timing diagram is shown in Figure 11-188. A data conversion cycle is initiated when $\overline{CS}$ is brought low. This occurs when a low on address line A0 is latched into the D-type flip-flop on the positive edge of clock Phi 2. Address bit A14 is used as a gating signal to prevent the TLC549 device from inadvertently being selected during normal program execution.

Data is shifted out of the TLC549 device on the positive edge of the I/O clock which is generated by gating the positive going edge of clock Phi 2 with address line A15. When A15 goes high, the output of the 3-state buffer is enabled onto the data bus and the conversion result bit is shifted into the 6502 device on the trailing edge of clock Phi 2. Once the data is in the accumulator, it is rotated into the carry bit, and then rotated into memory. $\overline{CS}$ is then brought high by latching a high into the D-type flip-flop. This is done by placing a high on address bit A0. This cycle can be completed every 133 μs.

It should be noted that this circuit uses an address decoding scheme that requires a minimum of decoding hardware. Small modifications to the decoding scheme may be necessary to match the interface properly to a particular application. The software listing for this application follows.

```
CSHIGH      .EQU 4001H
CSLOW       .EQU 4000H
RESULT      .EQU 0000H
CLOCK       .EQU 8000H
;
;
;
            STA  SLOW       ; Bring /CS low
            LDX  #$08       ; Initialize bit counter
LOOP        LDA   LOCK      ; Clock in data bit
            ROR  A          ; Rotate do into carry bit
            ROL  RESULT     ; Rotate carry bit into result
            DEX             ; Decrement bit counter
            DNE  LOOP       ; Get another bit if not zero
            STA  CSHIGH     ; Bring /CS high
```

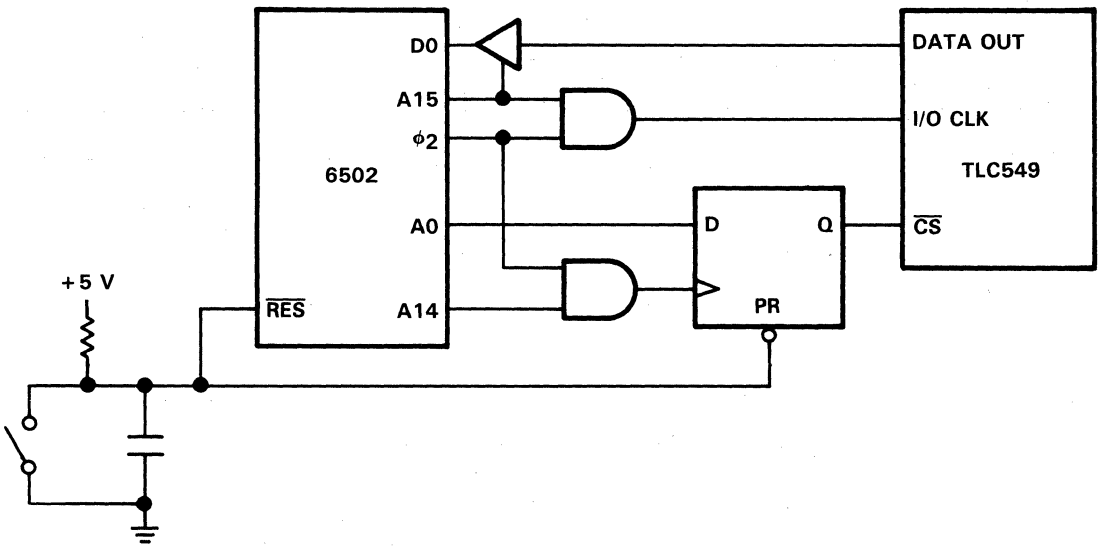


Figure 11-187. 6502 to TLC549 Interface Circuit Diagram

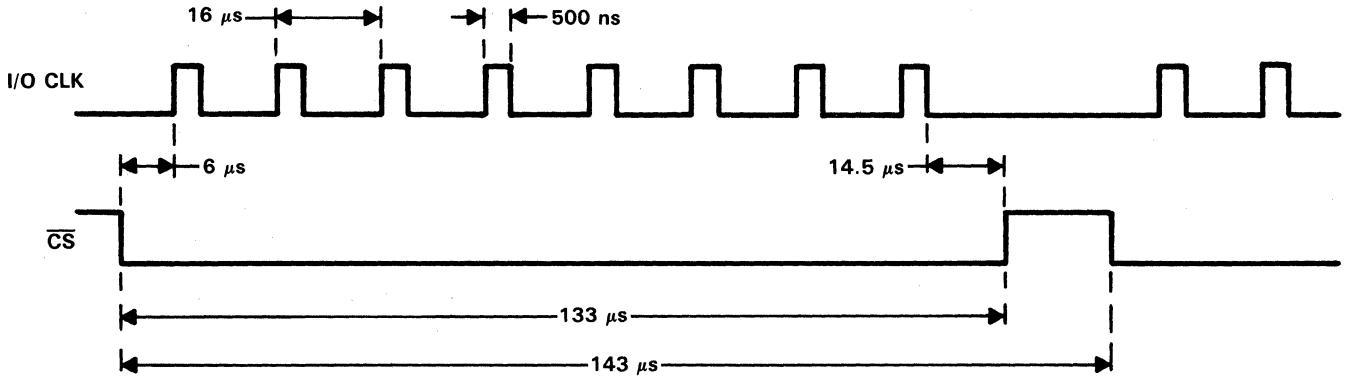


Figure 11-188. 6502 to TLC549 Interface Timing Diagram

INTERFACE FOR THE TLC549 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING THE 6522 VIA

This application presents the design of an interface circuit for the TLC549 A/D to the 6502 microprocessor through the 6522 VIA. Interfacing techniques for the TLC549 are very similar to those for the TLC540. The interface presented in this application utilizes the 6522 VIA, and is similar to the INTERFACE FOR THE TLC549 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING THE 6522 VIA presented in a previous application. Since the TLC549 converts only one analog input, no multiplexer address is required, thus, less software is required to control the interface.

Principles of Operation

The TLC549 to 6522 interface circuit is shown in Figure 11-189. The timing diagram is shown in Figure 11-190. An initialization software listing and an interface control software listing are included below.

A data conversion cycle begins by bringing $\overline{CS}$ low. This is accomplished by writing a low to port B output pin PBO. Previous conversion results are shifted in by reading the SR (Figure 11-188). The D-type flip-flops (Figure 11-186) are included to effectively delay the I/O clock in order to meet all of the set up and hold time requirements for shifting the data. A delay loop is included (Figure 11-188) to allow for the data to be shifted in. On the eighth falling edge of the I/O clock, conversion of the analog input begins, and is completed in 17 μs. $\overline{CS}$ is then brough high by writing a high to PBO. Previous conversion results can then be read into the 6502 from the 6522 while a new conversion is in progress. One cycle as described here can be completed in 48 μs.

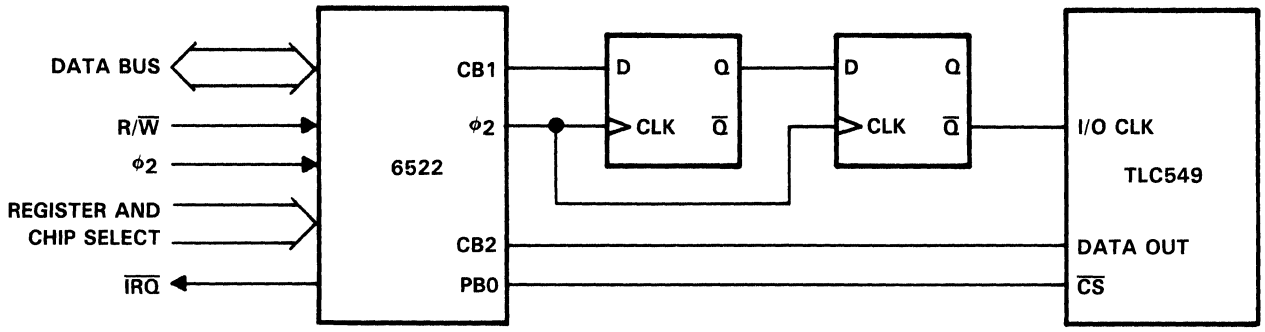


Figure 11-189. 6522 to TLC549 Interface Circuit Diagram

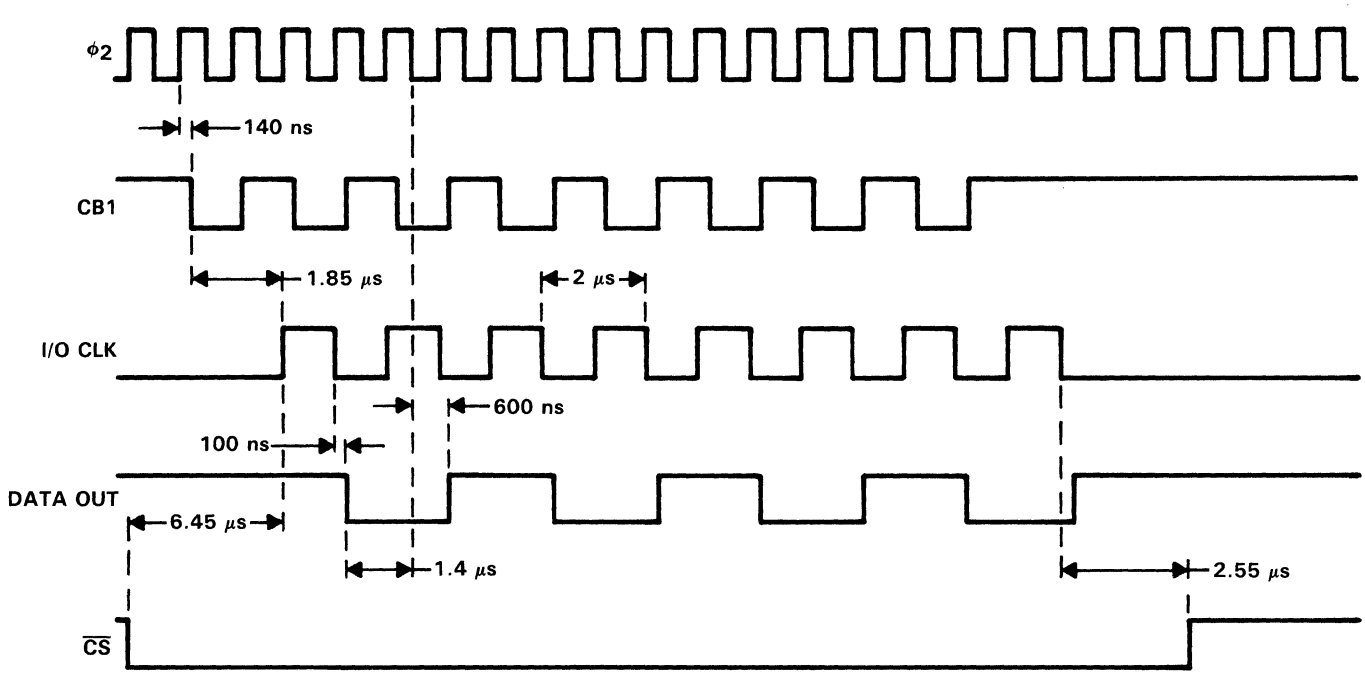


Figure 11-190. 6522 to TLC549 Interface Timing Diagram

```
                    REGISTER ASSIGNMENTS
;
;
ORB             .EQU 0000H
DDRB            .EQU 0002H
SR              .EQU 000AH
ACR             .EQU 000BH
;
;
                LDA  #$01       ;
                STA  DDRB       ; Initialize port B I/O pins
                LDA  #$01       ;
                STA  ORB        ; Bring chip select high
                LDA  #$08       ; Shift in on phi 2
                STA  ACR        ;


                LDX  #$00       ;
                STX  ORB        ; Bring /CS low
                LDA  SR         ; Clock in previous results
DELAY:          LDY  #$03       ;
                DEY             ; Delay while results clocked in
                BNE  DELAY      ;
                LDX  #$01       ;
                STX  ORB        ; Bring /CS high
                LDA  SR         ; Load previous results into acc
```

INTERFACE FOR THE TLC549 DEVICE TO THE MOTOROLA 6805 MICROPROCESSOR

This application describes techniques for operating the TLC549 A/D peripheral chip with the 6805 microprocessor. This can be accomplished by either of two methods:

1. Generating all necessary control signals under software control by toggling output port pins
2. Using the serial peripheral interface (SPI) to generate necessary control signals for data transfer.

The TLC549 device is well suited for use with the SPI, however, not all 6805 microprocessors include the SPI on the chip. Therefore, the software controlled interface has the advantage although it is less efficient.

The TLC549 device is a complete data acquisition system on a chip. The system includes functions such as sample-and-hold, 8-bit A/D converter, on-chip oscillator, and microprocessor-compatible control logic. Data can be acquired with only three I/O lines: $\overline{CS}$, I/O clock, and a serial data line. Conversion requires 17 μs, and the I/O clock can run up to 2.048 MHz.

Principles of Operation

The circuit diagram for the software controlled TLC549 device to 6805 microprocessor interface is shown in Figure 11-191. Circuit timing is shown in Figure 11-192. The software controlled interface makes use of three pins on port A of the 6805 microprocessor. Two of these lines are used as outputs to generate $\overline{CS}$ and I/O clock. The other pin is used as an input to receive the conversion results from the TLC549 device. A short program listing that can be used to initialize the input/output pins is given below.

A program listing that controls the actual transfer of data is also shown below. This program block brings $\overline{CS}$ low and generates the I/O clock that shifts the previous conversion results out of the TLC549 device. Sampling of the analog input begins at the falling edge of the fourth I/O clock and continues until the falling edge of the eighth I/O clock occurs. When sampling ends, conversion begins and is completed in 17 μs. With the 6805 device running at 5 MHz, one conversion cycle that initiates a new conversion and reads the results of the previous conversion can be completed in 204 μs.

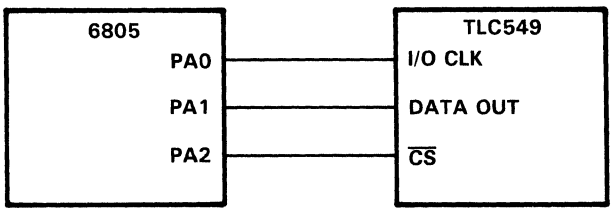


Figure 11-191. 6805 to TLC549 Interface Circuit Diagram

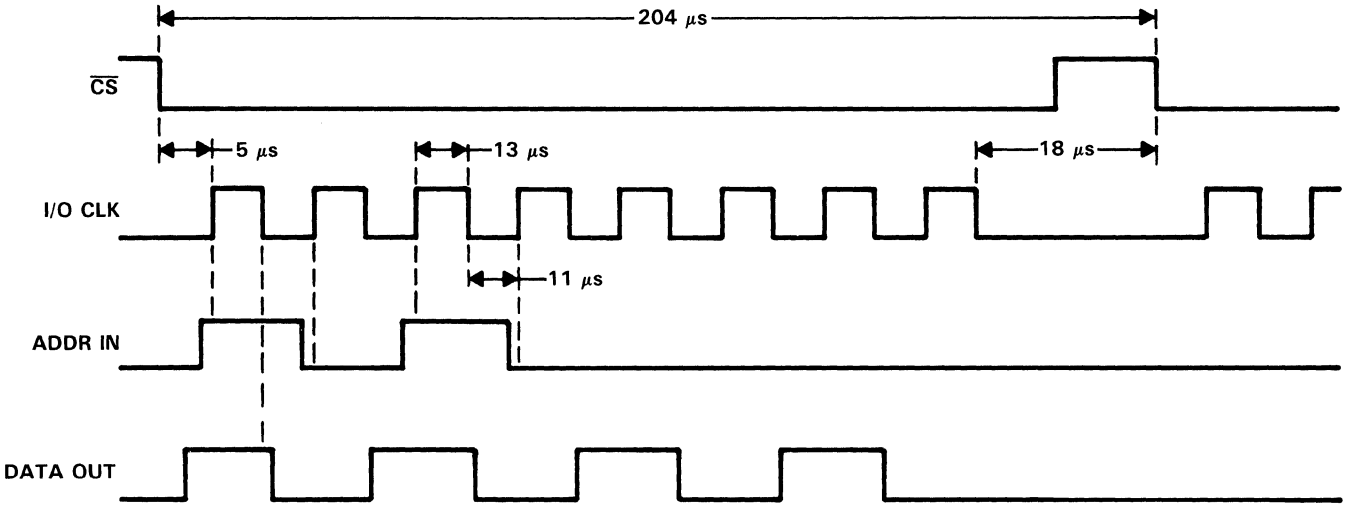


Figure 11-192. 6805 to TLC549 Interface Timing Diagram

```
PORTA     .EQU  0000H
DDRA      .EQU  0004H
          .ORG  0100H
START:    LDA   #05H          ;
          STA   DDRA          ; Initialize port a I/O pins
          BSET  2,PORTA       ; Bring chip select high

          LDX   #08           : Initialize counter
          BCLR  2,PORTA       ; Bring chip select low
LOOP:     BSET  0,PORTA       ; Bring I/O clock high
          BRSET 1,PORTA,LABEL ; Read data bit into carry bit
LABEL:    ROLA                ; Rotate carry into accumulator
          BCLR  0,PORTA       ; Bring I/O clock low
          DECX                ; Decrement counter
          BNE   LOOP          ; Continue if counter is not zero
          BSET  2,PORTA       ; Bring chip select high
```

SOFTWARE INTERFACE FOR THE TLC549 DEVICE TO INTEL 8048 AND 8049 MICROPROCESSORS

The operation of the TLC549 device is similar to the more complex TLC540 and TLC541 devices. The TLC549 device provides an on-chip system clock that operates typically at 4 MHz. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing. This independence permits manipulation of the TLC549 device for a wide range of software and hardware requirements.

This software interface application features:

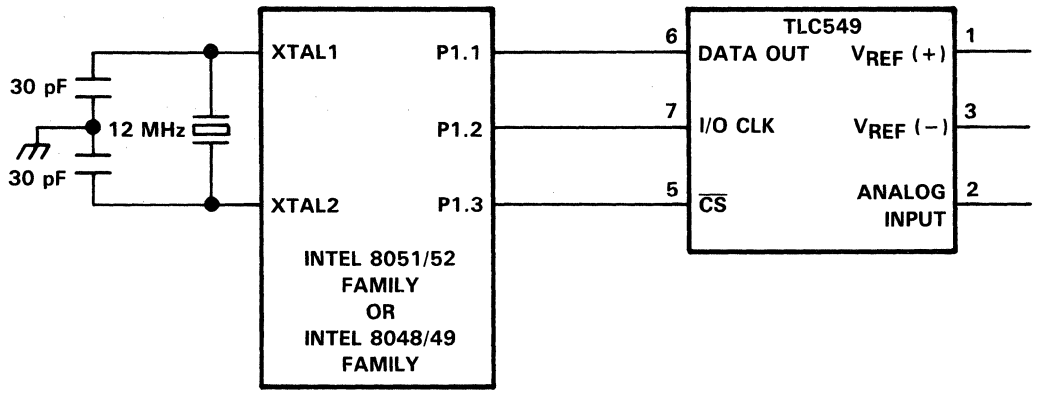
1. A low-cost A/D converter
2. Minimum hardware requirement
3. Remote control of serial A/D converters.

Hardware

Figure 11-193 shows the circuit for the 8048 and 8049 microprocessor to TLC549 device software interface. This interface uses only three port pins of the microprocessor. While the TLC549 device internal sample-and-hold circuitry is accessing and holding the new analog signal, Port 1.3 and $\overline{CS}$ must be low. I/O clock is transmitted through port 1.2 to pin 7 of the TLC549 device. Port 1.1 acquires the conversion data from the data output pin of the TLC549 device.

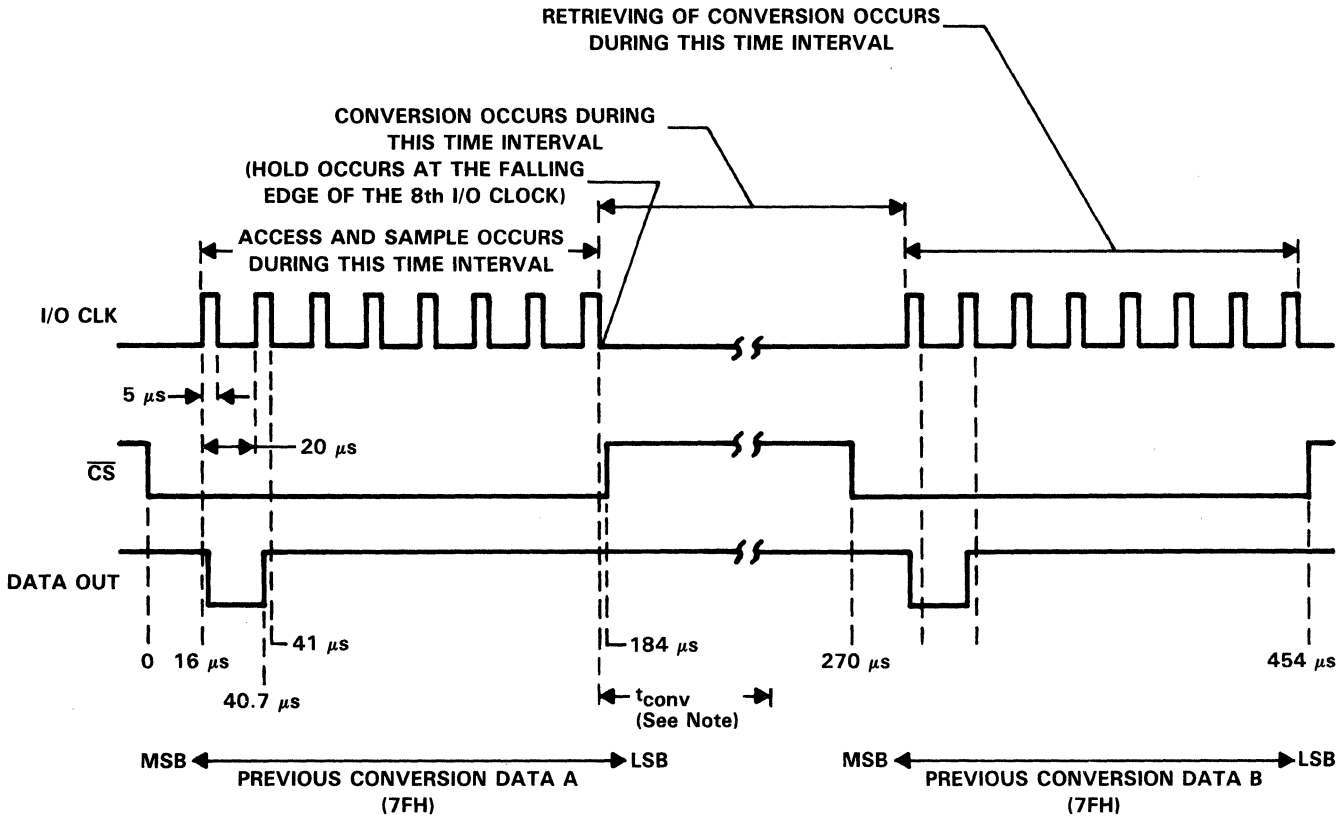
Timing Diagram

Figure 11-194 shows the timing diagram for the interface. The timing diagram indicates that one complete conversion cycle requires 454 μs.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751AH/80C51
INTEL 8048/49 FAMILY: 8048AH/8748H/8035AHL/8049AH/8749H/8039AHL/8050AH/8040AHL/80C49

Figure 11-193. The Intel 8051/52 or 8048/49 to TLC549 Software Interface



NOTE; t_{conv}: The conversion cycles, which requires 36 internal system clock periods, is initiated with the 8th I/O clock↓ after $\overline{CS}$↓. Conversion time requires a minimum of 17μs.

Figure 11-194. Timing Diagram for the Intel 8048/49 — TLC549 Software Interface

After $\overline{CS}$ goes low, eight I/O clocks access and sample the new analog signal from the analog input. At the same time, I/O clock falling edges shift out the previous conversion result. This conversion result is only valid for the previous analog signal sample.

Conversion occurs in the time interval starting when the eighth I/O clock goes low. The conversion time interval requires 36 internal system clock cycles. The designer cannot see the system clock, but the designer can obtain the conversion time from the data sheets. Typically, a time interval of 17 μs is required for conversion.

See the SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8048 AND 8049 MICROPROCESSORS application for more information.

Software

The interface software program listing follows. Also see the SOFTWARE INTERFACE FOR THE TLC549 DEVICE TO INTEL 8051 AND 8052 MICROPROCESSORS application. There are differences between the software for the 8051 and 8052 devices and for the 8048 and 8049 devices. The JB1 instruction is used to detect the polarity of the conversion result bits for the 8048 and 8049 device interface. If desired, the software can be incorporated into a subroutine so the designer can access the software with a simple subroutine call.

```
                        ; Software Listing for Intel 8048/49
                        ; Interface — TLC549
                        ;
                        ;
                        ;
        CALL S549D      ; Access, sample and hold the new
                        ; analog signal.
                        ;
                        ; A delay must occur here to allow the A/D
                        ; chip to complete conversion. The delay
                        ; must allow 36 A/D chip internal system
                        ; clock cycles to occur. Conversion time
                        ; requires a minimum of 17 microseconds.
                        ;
        CALL S549D      ; Access, sample and hold the new
                        ; analog signal. Bring out the previous
                        ; conversion result.
                        ;
                        ; Subroutine CALL
                        ;
S549D   ANL P1, #FBH    ; Lower I/O clock
        MOV R0, #08H    ; Set bit counter to 8
        ANL P1, #F7H    ; Lower Chip Select
S549H   CLR C           ; Initialize C = 0
        IN A,P1         ; Get Port 1
        CPL A           ; Compliment Accumulator
        JB1 S549J       ; If 549 data out = 0; branch
        CPL C           ; 549 data out = 1; Set C = 1
S549J   MOV A,R1        ; Get serial buffer
        RLC A           ; Shift data out bit into serial buffer
        MOV R1,A        ; Store serial buffer
        ORL P1, #04H    ; Raise I/O clock
        NOP             ; Delay to slow I/O clock
        ANL P1, #FBH    ; Lower I/O clock
        DJNZ R0,S549H   ; Do 8 times
        ORL P1, #08H    ; Raise Chip Select
        MOV A,R1        ; Conversion data in A
        RET             ;
        END             ;
```

SERIAL PORT INTERFACE FOR THE TLC549 DEVICE TO INTEL 8051 AND 8052 MICROPROCESSORS

The operation of the TLC549 device is similar to that of the more complex TLC540 and TLC541 devices. The TLC549 device provides an on-chip system clock that operates typically at 4 MHz. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing to permit manipulation of the TLC549 device for a wide range of software and hardware requirements.

Since the TLC549 device needs only the I/O clock input and $\overline{CS}$ input for data control, this serial port interface offers the simplest interface example. It has excellent performance and uses a most economical LinCMOS converter chip. This serial interface application features:

1. Low-cost A/D converter
2. Minimum hardware requirement
3. Fast conversion and communication speed between the A/D converter and the microprocessor
4. Remote control of the A/D converters.

This is an excellent interface if the Intel microprocessor's serial port does not have to be used for another purpose. Even if another purpose is required, the serial port can be multiplexed through good design so both the A/D converter and the additional purpose can be accommodated by the serial port.

Hardware

Figure 11-195 shows the 8051 and 8052 device serial port to the TLC549 device interface circuit. By using the inverted TXD shift clock as an I/O clock for the A/D converter, previous conversion data can be transferred serially from the TLC549 device to the RXD pin of the microprocessor.

Timing Diagram

Figure 11-196 shows the timing diagram for a complete A/D conversion. The timing diagram shows that one complete conversion cycle requires 78.98 μs.

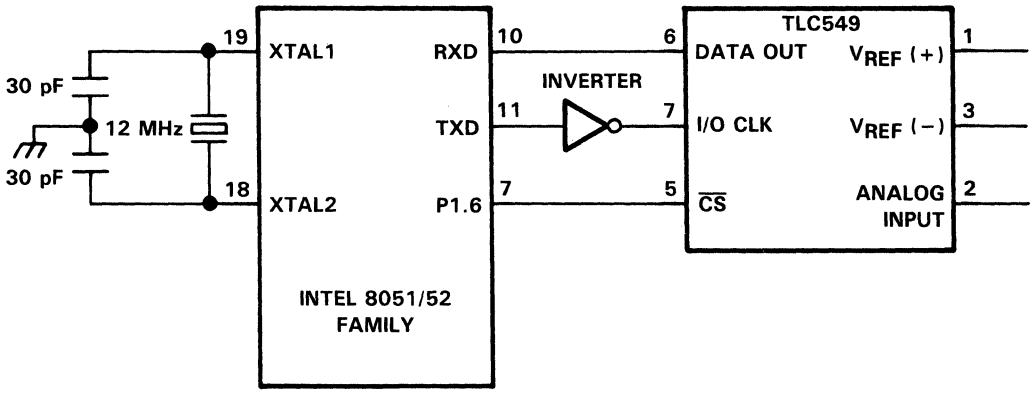
After $\overline{CS}$ goes low, eight I/O clocks access and sample the new analog input. At the same time, I/O clock falling edges shift out the previous conversion result. This conversion result is valid only for the previous analog signal sample.

Conversion occurs in the time interval starting when the eighth I/O clock goes low. The conversion time interval requires 36 internal system clock cycles. The designer cannot see the system clock, but can obtain the conversion time from the data sheets. Typically, a time interval of 17 μs is required for conversion.

See the SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS application for more information.

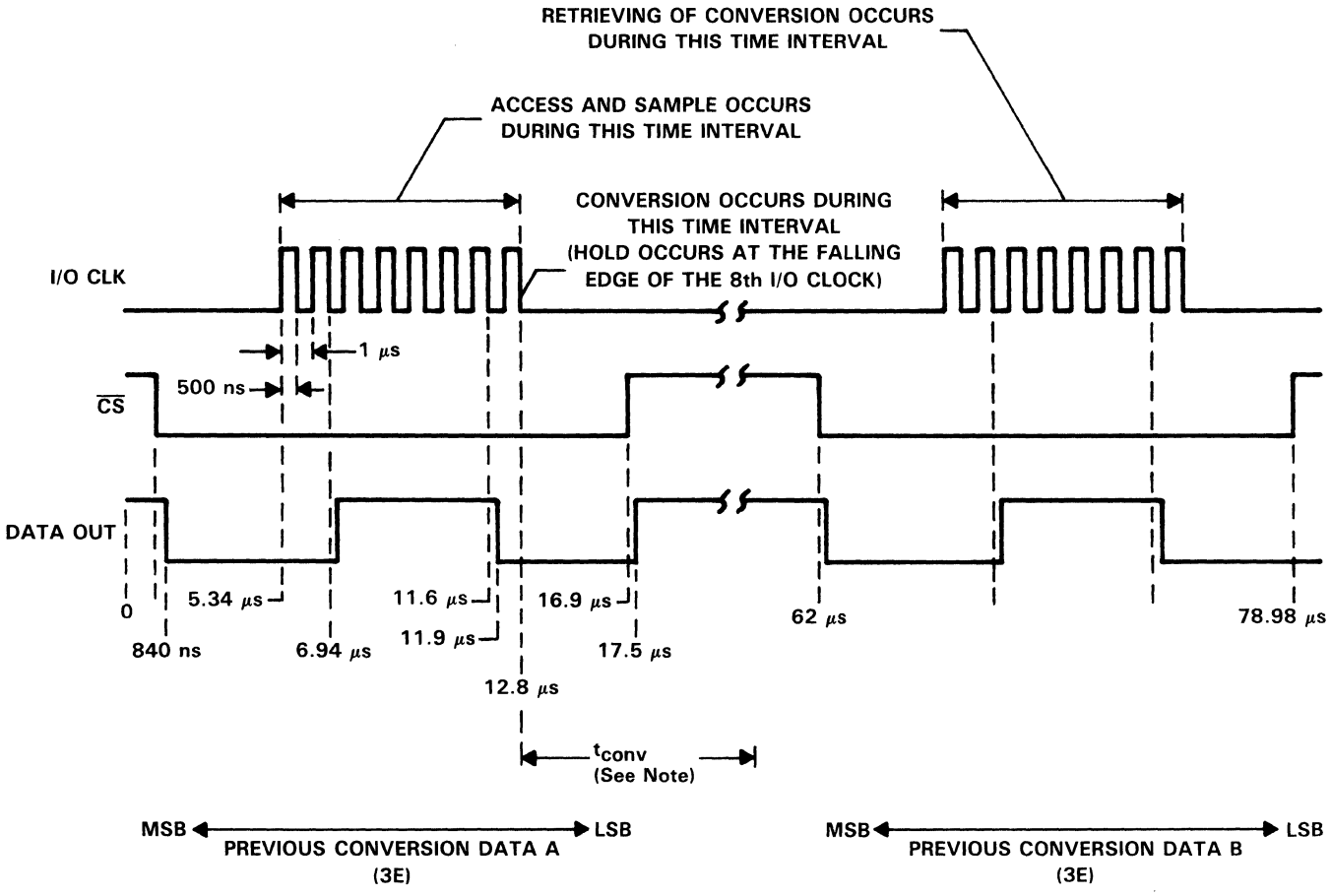
Software

The interface software listing follows. The serial port Mode 0 state is used to permit 8-bit transmission and reception. Note that the A/D converter device sends the most significant bit of the conversion result first and the serial buffer receives this bit as the least significant bit. The latter part of the software program is responsible for reversing the conversion bits and placing them in the proper order.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751H/80C51
INVERTER: 74HC04, 74LS04

Figure 11-195. The Intel 8051/52 Serial Port to TLC549 Interface



NOTE; t_{conv}: The conversion cycles, which requires 36 internal system clock periods, is initiated with the 8th I/O clock↓ after $\overline{CS}$↓. Conversion time requires a minimum of 17μs.

Figure 11-196. Timing Diagram for the Intel 8051/52 Serial Port to TLC549 Interface

```
                    ; Software Listing for Intel 8051/52
                    ; Serial Port — TLC549
                    ;
ACALL SR549D        ; Access and sample and hold the new
                    ; analog signal.
                    ;
                    ; A delay must occur here to allow the A/D
                    ; chip to complete conversion. The delay
                    ; must allow 36 A/D chip internal system
                    ; clock cycles to occur. Conversion time
                    ; requires a minimum of 17 microseconds.
                    ;
ACALL SR549D        ; Access and sample and hold the new
                    ; analog signal. Bring out the previous
                    ; conversion result.
```

```
                        ;
                        ; The serial port read reverses the data con-
                        ; version bits coming to the microprocessor
                        ; so that they are in the following order:
                        ; b0(LSB),b1,b2,b3,b4.b5.b6.b7
                        ; (MSB). These bits (01234567) along with
                        ; the Carry bit (C) in the following
                        ; instruction comments are presented so
                        ; that the reader will understand the
                        ; technique, which is used to place the
                        ; bits in their proper order.
                        ;
            RLC A       ; 6543210C 7; b7 is now in Carry
            RLC A       ; 543210C7 6; b6 is now in Carry
            MOV ACC.1,C ; 54321067 6; put b6 into ACC.1
            MOV C,ACC.2 ; 54321067 0; put b0 into C
            RLC A       ; 43210670 5; b5 is now in Carry
            MOV ACC.3,C ; 43215670 5; put b5 into ACC.3
            MOV C,ACC.4 ; 43215670 1; put b1 into C
            RLC A       ; 32156701 4; b4 is now in Carry
            MOV ACC.5,C ; 32456701 4; put b4 into ACC.5
            MOV C,ACC.6 ; 32456701 2; put b2 into C
            RLC A       ; 24567012 3; b3 is now in Carry
            MOV ACC.7,C ; 34567012 3; put b3 into ACC.7
            RL A        ; 45670123  ; prepare for SWAP A
            SWAP A      ; 01234567  ; bits are ordered correctly
                        ; Conversion result is in Accumulator
                        ;
                        ; Subroutine ACALL
SR549D      CLR P1.6    ; Lower Chip Select
            ORL SCON,#10H ; Set REN
            ANL SCON,#FEH ; Reset RI
            JNB SCON.0,RCV ; RI flag not set; BRANCH
                        ; until reception is complete
            CPL P1.6    ; Raise Chip Select
            RET         ; Conversion is in SBUF
            END         ;
```

SOFTWARE INTERFACE FOR THE TLC549 DEVICE TO INTEL 8051 AND 8052 MICROPROCESSORS

The operation of the TLC549 device is similar to the more complex TLC540 and TLC541 devices. The TLC549 device provides an on-chip system clock that operates typically at 4 MHz. The on-chip system clock allows internal device operation to proceed independently of serial input/output data timing to permit manipulation of the TLC549 device for a wide range of software and hardware requirements. This software interface application features:

1. Low-cost A/D converter
2. Minimum hardware requirement
3. Remote control of serial A/D converters.

Hardware

Figure 11-197 shows the circuit for the 8051 and 8052 device to TLC549 device software interface. This application requires only three port pins of the microprocessor. While the TLC549 device internal sample-and-hold circuitry is accessing and holding the new analog signal, Port 1.3 and $\overline{CS}$ must be low. The I/O clock is transmitted through port 1.2 to pin 7 of the TLC549 device. Port 1.1 acquires the conversion data from the data output pin of the TLC549 device.

Timing Diagram

Figure 11-198 shows the timing diagram for the interface. The timing diagram shows that one complete conversion cycle requires 245 μs.

After $\overline{CS}$ goes low, eight I/O clocks access and sample the new analog input. At the same time, I/O clock falling edges shift out the previous conversion result. This conversion result is valid only for the previous analog signal sample.

Conversion occurs in the time interval starting when the eighth I/O clock goes low. The conversion time interval requires 36 internal system clock cycles. The designer cannot

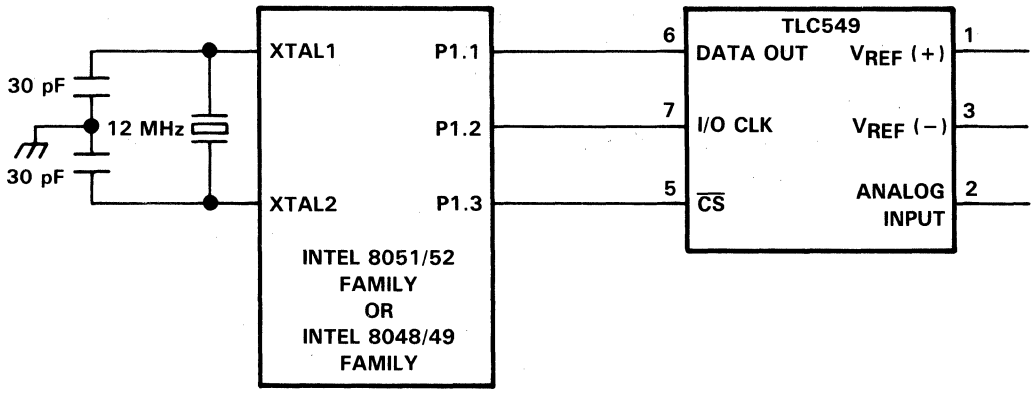
see the system clock, but can obtain the conversion time from the data sheets. Typically, a time interval of 17 μs is required for conversion.

See the SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS application for more information.

Software

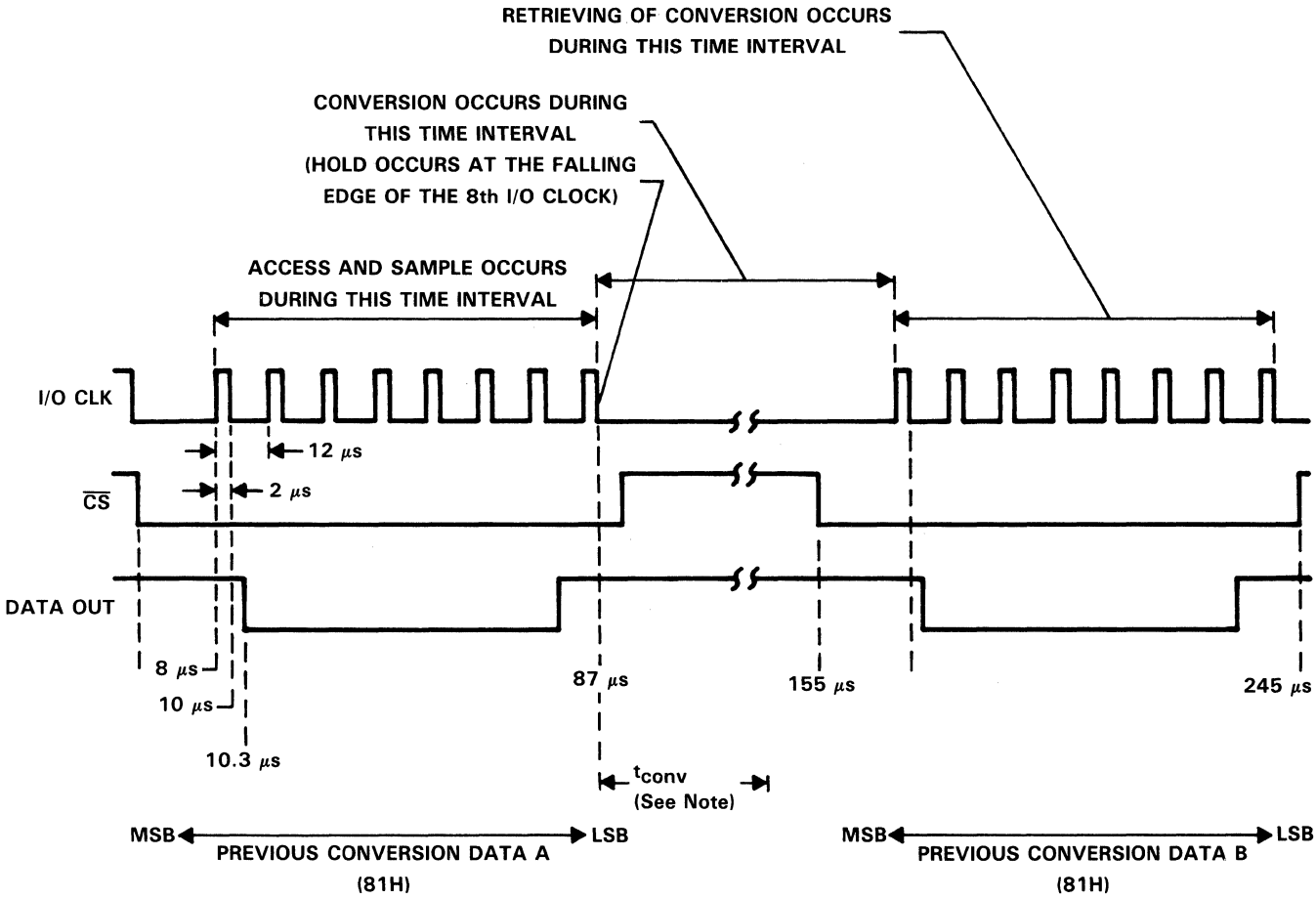
The internal software program follows. As shown in the SOFTWARE INTERFACE FOR TLC540 AND TLC541 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS application, the instruction RLC A (Rotate Accumulator Left through the Carry flag) loads each conversion bit successively into the accumulator from the data output of the TLC549 device. If desired, the software can be incorporated into a subroutine so the designer can access the software with a simple subroutine call.

```
                        ; Software Listing for Intel 8051/52
                        ; Interface — TLC549
                        ;
                        ;
        ACALL S549D     ; Access, sample and hold the new
                        ; analog signal.
                        ;
                        ; A delay must occur here to allow the A/D
                        ; chip to complete conversion. The delay
                        ; must allow 36 A/D chip internal system
                        ; clock cycles to occur. Conversion time
                        ; requires a minimum of 17 microseconds.
                        ;
        ACALL S549D     ; Access, sample and hold the new analog
                        ; signal. Bring out the previous
                        ; conversion result.
                        ;
                        ; Subroutine ACALL
S549D   CLR P1.2        ; Lower I/O Clock
        MOV R0, #08H    ; Set bit counter to 8
        CLR P1.3        ; Lower Chip Select
S549I   CLR C           ; Initialize C = 0
        JNB P1.1,S549J  ; If 549 data out = 0; BRANCH
        CPL C           ; 549 data out = 1; set C = 1
S549J   MOV A,R1        ; Get serial buffer
        RLC A           ; Shift data out bit into serial buffer
        MOV R1,A        ; Store serial buffer
        CPL P1.2        ; Raise I/O clock
        NOP             ; Delay to slow I/O clock
        CLR P1.2        ; Lower I/O clock
        DJNZ R0,S549I   ; Do 8 times
        CPL P1.3        ; Raise Chip Select
        MOV A,R1        ; Conversion data in A
        RET             ;
        END             ;
```



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751AH/80C51
INTEL 8048/49 FAMILY: 8048AH/8748H/8035AHL/8049AH/8749H/8039AHL/8050AH/8040AHL/80C49

Figure 11-197. The Intel 8051/52 or 8048/49 to TLC549 Software Interface



NOTE; t_{conv}: The conversion cycles, which requires 36 internal system clock periods, is initiated with the 8th I/O clock↓ after $\overline{CS}$↓. Conversion time requires a minimum of 17μs.

Figure 11-198. Timing Diagram for the Intel 8051/52 — TLC549 Software Interface

INTERFACE FOR TLC1540 AND TLC1541 DEVICES TO THE ZILOG Z80A MICROPROCESSOR

This application describes a technique for interfacing the Z80A microprocessor to the TLC1540 10-bit A/D converter using software control. The TLC1540 device is a complete data acquisition system on a chip. It includes an analog multliplexer, sample-and-hold, 10-bit successive-approximation A/D converter, and microprocessor-compatible control inputs. These inputs are chip select, address input, system clock, and I/O clock. The system clock and I/O clock need no special speed or phase relationship and are normally operated independently. This allows the system clock to run up to 2.1 MHz to ensure conversion in 21 μs while the I/O clock runs up to 1.1 MHz to allow a maximum data transfer rate.

Principles of Operation

A circuit diagram for the software controlled Z80A microprocessor to TLC1540 device interface is shown in Figure 11-199. A timing diagram for the interface is shown in Figure 11-200. The control software routine listing follows the illustrations.

A data conversion cycle is initiated by bringing $\overline{CS}$ low. This is accomplished by latching a low on address line A0 into the D-type flip-flop. Execution of an IN instruction causes the RD line and the $\overline{IORQ}$ line to become active and generate one I/O clock pulse.

A multiplexer address bit is shifted in on the rising edge of the I/O clock pulse and a conversion result data bit is shifted out on the trailing edge of the pulse. The I/O clock pulse also connects the output of the SN74126 3-state buffer onto the data bus that allows a data bit to be read into the Z80A accumulator. Once in the accumulator, the data bit is rotated through the carry bit location and into register B or C. Register B contains the eight most significant bits while register C contains the two least significant bits so the data is left justified. Register D contains the multiplexer address in the 4 most significant bit positions and is shifted out to the left. On the falling edge of the fourth I/O clock pulse, sampling of the addressed analog input begins and continues until the falling edge of the tenth I/O clock pulse occurs. At that time, $\overline{CS}$ is brought high and conversion begins. Conversion requires 44 system clock cycles, and $\overline{CS}$ should remain high until conversion is complete. If these conditions change, the ongoing conversion will be aborted and a new conversion cycle will begin. It is possible to read conversion results every 141 μs.

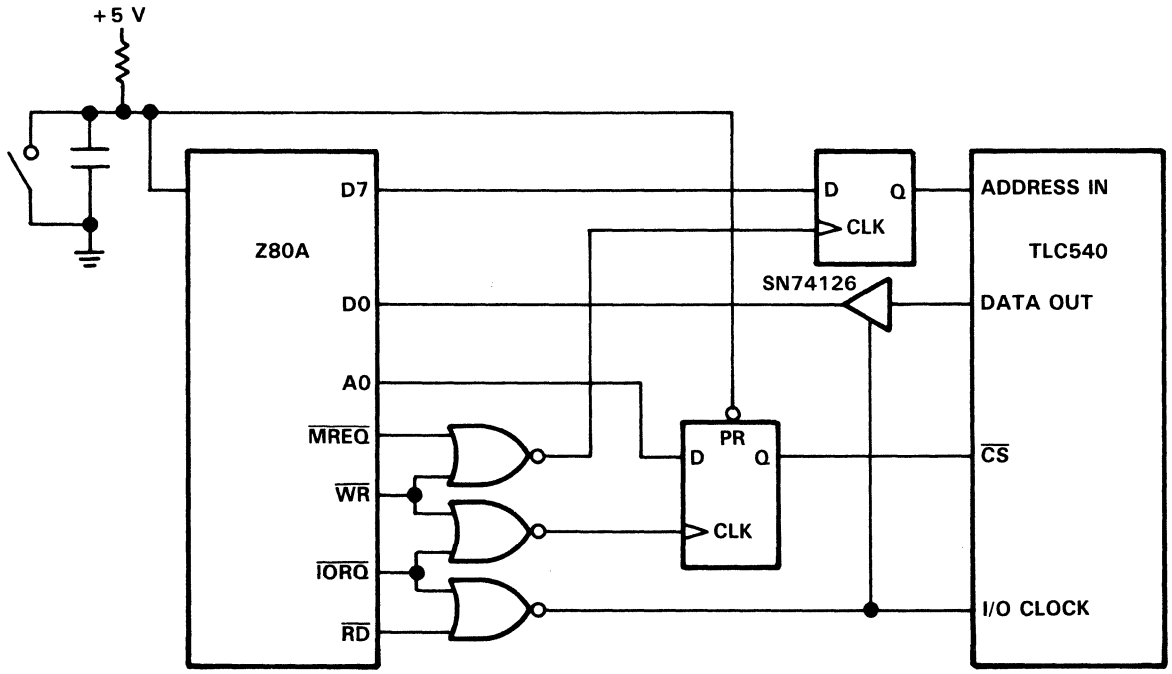


Figure 11-199. Z80A to TLC1540 Interface Circuit Diagram

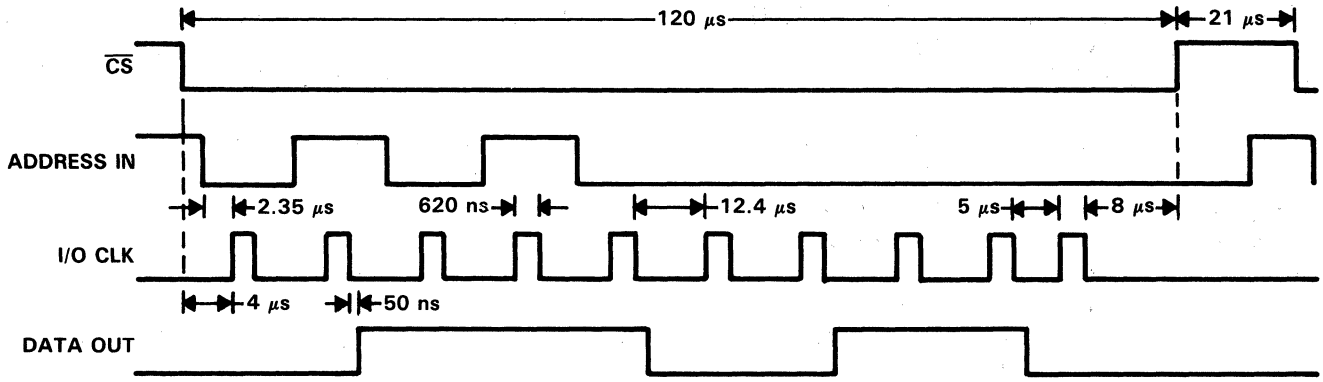


Figure 11-200. Z80A to TLC1540 Interface Timing Diagram

Software for Z80A to TLC1540
and TLC1541 Interface

```
        LD   E,08H          ; Load bit counter
        LD   D,50H          ; Initialize muxaddress to Ch 5
        OUT  (CSLOW),A      ; Bring /CS low
LOOP:   LD   (HL),D         ; Write out muxaddress bit
        IN   A,(BIT)        ; Read in a bit & clock next bit
        RRA                 ; Rotate bit into carry
        RL   B              ; Rotate into result register B
        RLC  D              ; Rotate muxaddress left
        DEC  E              ; Decrement bit counter
        JP   NZ,LOOP        ; Get another bit if not zero
        IN   A,(BIT)        ; Read in bit 1 of result
        RRA                 ; Rotate into carry
        RL   C              ; Rotate into result register C
        IN   A,(BIT)        ; Read in bit 0 of result
        RRA                 ; Rotate into carry
        RR   C              ; Rotate result register C
        RR   C              ; Rotate result register C
        OUT  (CSHIGH),A     ; Bring /CS high
```

INTERFACE FOR TLC1540 AND TLC1541 DEVICES TO THE ROCKWELL 6502 MICROPROCESSOR

This application describes a technique for operating the TLC1540 10-bit A/D converter with the 6502 microprocessor software generated control signals. These signals are $\overline{CS}$, I/O clock, address input, and system clock. The system clock signal is required to drive the successive-approximation conversion process. Reference inputs allow ratiometric conversion, however, they are normally tied to V_{CC} and ground. One of 11 analog inputs or a self-test mode is selected with the on-board analog multiplexer. The TLC1540 device is pin-for-pin compatible with the TLC540 device, allowing easy system upgrade.

Hardware

A circuit diagram for the 6502 microprocessor to TLC1540 device interface is shown in Figure 11-201. I/O clock pulses are generated by enabling the positive going pulse of the $\phi 2$ clock to the TLC1540 device. Address input bits are latched into the TLC1540 device on the leading edge of the $\phi 2$ pulse and data bits are shifted out of the TLC1540 device on the trailing edge of the pulse. Address lines A1, A10, and A11 are decoded to enable the output of the SN74126 3-state buffer onto the data bus and the data bit is read by the 6502 microprocessor on the negative edge of $\phi 2$. $\overline{CS}$ is controlled by clocking the level of A2 into the D-type flip-flop. Thus, by writing to the proper address, $\overline{CS}$ can be lowered or raised. A simple address decoding scheme is presented in this application. Small modifications may be necessary to fit a particular application.

Timing Diagram

A conversion cycle is initiated by bringing $\overline{CS}$ low. This is accomplished by writing to an address so that A2 is low. The multiplexer address should be placed in the most significant 4 bits of the MUXADDRESS memory location. A multiplexer address is rotated left into the carry, and then tested and written out. The LDA instruction causes one I/O clock pulse to be generated and one data bit to be read. Once the data bit is read in, it is rotated into the carry bit location, and then into RAM. The conversion result is stored in a left

justified format in memory locations 0001H and 0002H. After the tenth I/O clock pulse, $\overline{CS}$ is brought high and conversion starts. Conversion requires 44 system clock cycles, and a delay loop may be needed to allow enough time for conversion when using low system clock frequencies. When conversion is complete, $\overline{CS}$ is brought low. The time for one conversion cycle, 209 μs, is indicated in Figure 11-202.

Software

All control signals are directly or indirectly under control. A control software listing follows.

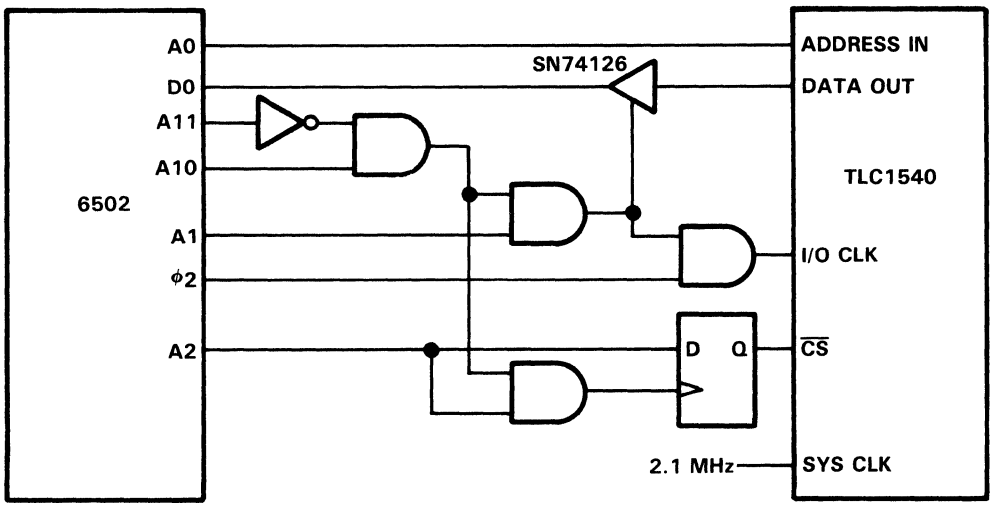


Figure 11-201. 6502 to TLC1540 Interface Circuit Diagram

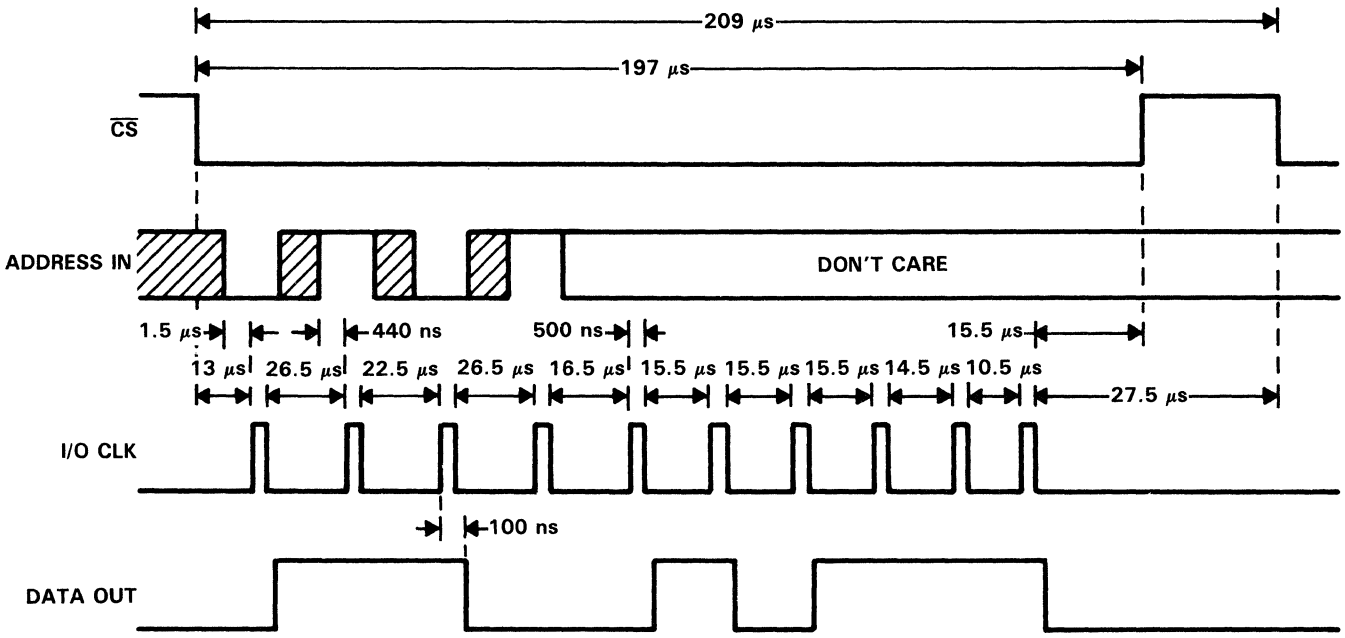


Figure 11-202. 6502 to TLC1540 Interface Timing Diagram

Software Listings for TLC1540 and TLC1541
to Rockwell 6502 Interface

```
;                *** Register Assignments ***
;
CSLOW            .EQU 0400H
CSHIGH           .EQU 0404H
ADDLOW           .EQU 0402H
ADDHIGH          .EQU 8403H
MUXADDRESS       .EQU 0000H
MSB              .EQU 0001H
LSB              .EQU 0002H
;
;                *** Main Program ***
;
START:           STA  CSHIGH        ; Make sure chi select is high
                 LDA  #$50          ;
                 STA  MUXADDRESS    ; Initialize muxaddress to Ch 5
                 STA  CSLOW         ; Bring chip select low
                 LDX  #$04H         ; Load counter

LOOP1:           ROL  MUXADDRESS    ; Rotate muxaddress into carry
                 BCS  HIGH          ; Branch if bit is set
                 LDA  ADDLOW        ; Write out A low on A0, clock data in
                 JMP  OVER          ; Skip next instruction
HIGH:            LDA  ADDHIGH       ; Write out A high on A0, clock data in
OVER:            ROR  A             ; Rotate do into carry
                 ROL  MSB           ; Rotate carry into MSB result
                 DEX                ; Decrement counter
                 BNE  LOOP1         ; Go back for another bit

                 LDX  #$04H         ; Load counter

LOOP2:           LDA  ADDLOW        ; Read in data bit
                 ROR  A             ; Rotate into carry
                 ROL  MSB           ; Rotate into MSB result
                 DEX                ; Decrement counter
                 BNE  LOOP2         ; Go back for another bit

                 LDA  ADDLOW        ; Read in bit 1 of result
                 ROR  A             ; Rotate into carry
                 ROL  LSB           ; Rotate into LSB result
                 LDA  ADDLOW        ; Read in bit 0 of result
                 ROR  A             ; Rotate into carry
                 ROR  LSB           ; Rotate LSB result
                 ROR  LSB           ; Rotate LSB result
                 STA  CSHIGH        ; Bring chip select high
```

INTERFACE FOR TLC1540 AND TLC1541 DEVICES TO THE MOTOROLA 6802 MICROPROCESSOR

This application describes a technique that uses software control in a 6802 microprocessor to TLC1540 10-bit A/D converter interface. The TLC1540 device is a complete data acquisition system on a chip. It contains an analog multiplexer, sample-and-hold, 10-bit successive-approximation A/D converter, and microprocessor-compatible control inputs. These inputs are $\overline{CS}$, I/O clock, address input, and system clock. The system clock and the I/O clock need no special speed or phase relationship and are normally operated independently. This allows the system clock to run up to 2.1 MHz to ensure conversion in 21 μs, while the I/O clock runs up to 1.1 MHz to allow a maximum data transfer rate.

Principles of Operation

A circuit diagram for the software controlled TLC1540 device to 6802 microprocessor interface is shown in Figure 11-203. The timing diagram is shown in Figure 11-204. A control software routine listing follows.

A data conversion cycle is initiated by bringing $\overline{CS}$ low. This is accomplished by latching a low from data bus line DO into the D-type flip-flop. Executing a STAA instruction latches a multiplexer address bit into the D-type flip-flop to ensure that set-up time requirements are met. Execution of an LDAB instruction enables the E clock to the TLC1540 device to generate one I/O clock pulse. It also enables the output of the 3-state buffer onto the data bus to read in a data bit on the trailing edge of the E clock. The trailing edge of E clock also shifts out the next bit of the conversion result. Once a data bit is read into accumulator B, it is rotated into the carry bit and then rotated into accumulator A. This rotates the multiplexer address one bit to the left. Since the eight most significant bits are stored in the first byte of RAM and the two least significant bits are stored in the second byte of RAM, the data is left justified. Conversion of the addressed channel begins on the falling edge of the tenth I/O clock pulse and requires 44 system clock cycles. $\overline{CS}$ is brought high at the beginning of conversion and should remain high until conversion is complete. A 2 MHz system clock can be obtained by tapping off the EXTAL pin into an SN74HC04 inverter and frequency divide-by-two circuit. The high impedance of the HCMOS device prevents the oscillator from being loaded excessively. It should be noted that many of the gates in this interface are used for the address decoding scheme for the control software presented. One data conversion cycle may be completed in 225 μs as indicated in Figure 11-204.

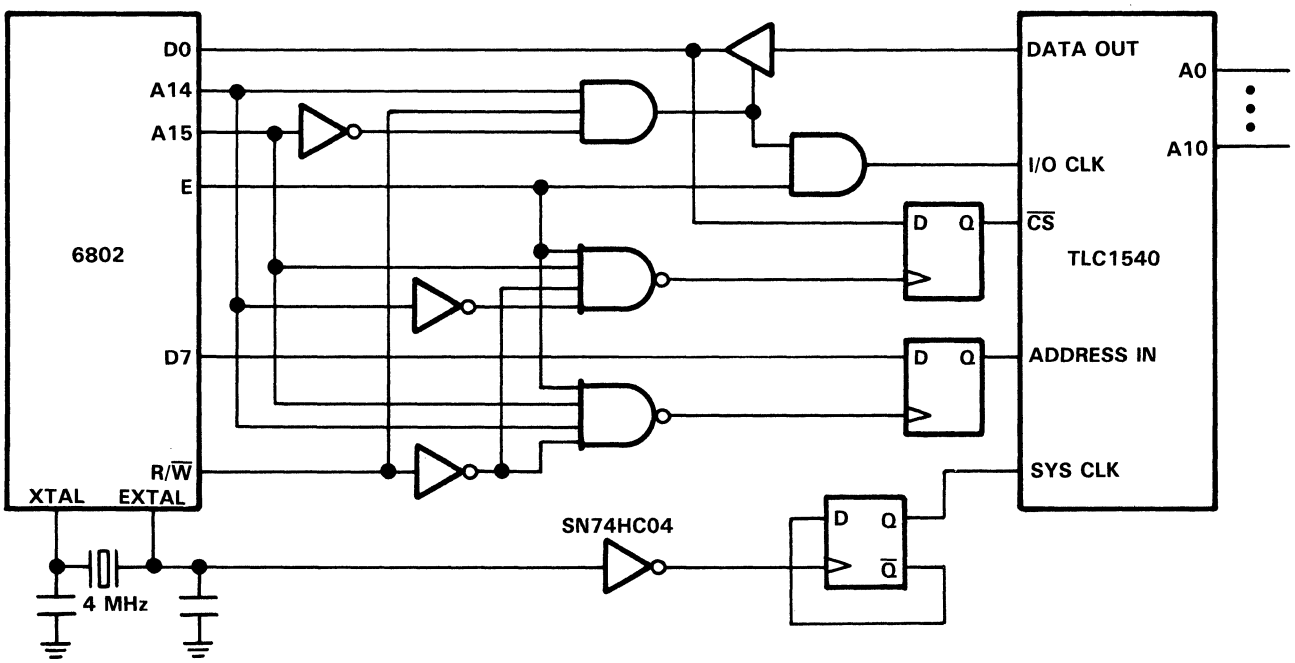


Figure 11-203. 6802 to TLC1540 Interface Circuit Diagram

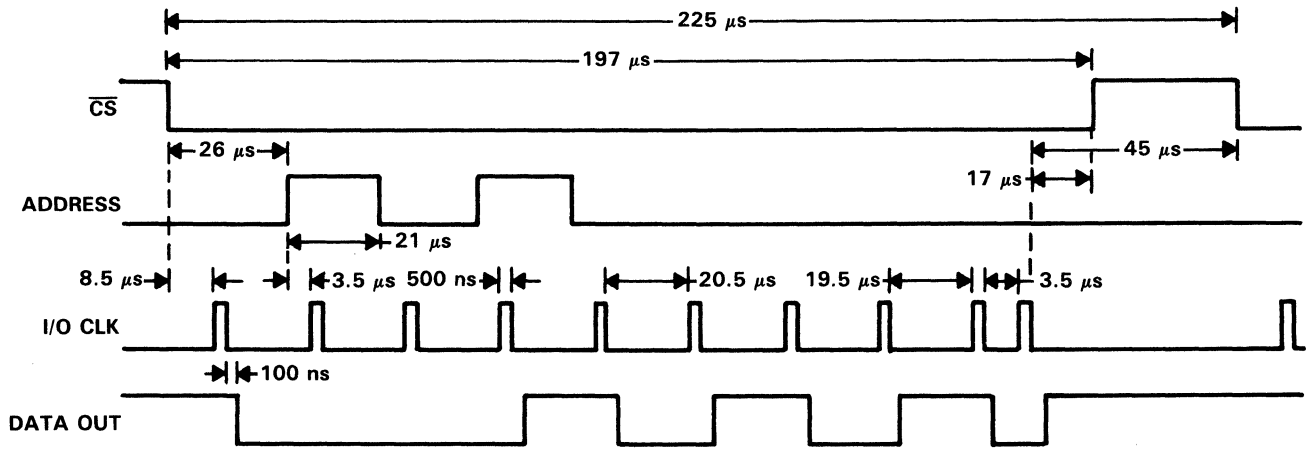


Figure 11-204. 6802 to TLC1540 Interface Timing Diagram

```
;
;                    Register Assignments for a TLC1540 or TLC1541 to
                                Motorola 6802 Interface

;
ADDRESS     .EQU    $C000H      ; Address to select address FF
DATA        .EQU    $4000H      ; Address to select 3-state buff
CS          .EQU    $8000H      ; Address to select CS FF
;
;
;
START:      LDAA    #50H        ; Initialize muxaddress to channel 5
            LDX     #08H        ; Load counter
            LDAB    #00H        ;
            STAB    CS          ; Bring chip select low
LOOP:       STAA    ADDRESS     ; Write out muxaddress bit
            LDAB    DATA        ; Read data bit and clock
            RORB                ; Rotate data bit into carry
            ROLA                ; Rotate carry into result
            DEX                 ; Decrement counter
            BNE     LOOP        ; Go back for another bit
            STAA    $0000H      ; Store 8 MSB'S in RAM
            LDAB    DATA        ; Read bit 1
            LDAA    DATA        ; Read bit 0
            RORA                ; Rotate bit 0 into carry
            RORB                ; Rotate bits 0 & 1
            RORB                ; Rotate bits 0 & 1
            STAB    $0001H      ; Store LSB'S in RAM
            LDAA    #01H        ;
            STAA    CS          ; Bring chip select high
```

SOFTWARE INTERFACE FOR TLC1540 AND TLC1541 DEVICES TO THE MOTOROLA 6805 MICROPROCESSOR

This application describes an interface for the 6805 microprocessor to TLC1540 10-bit A/D converter using software generated control signals. These signals are $\overline{CS}$, I/O clock, address input, and system clock. The system clock signal is required to drive the successive-approximation conversion process. Reference inputs allow ratiometric conversion, however, they are normally tied to V_{CC} and ground. One of 11 analog inputs or a self-test mode is selected with the on-board analog multiplexer. The TLC1540 device is pin-for-pin compatible with the TLC540 device to allow easy system upgrade.

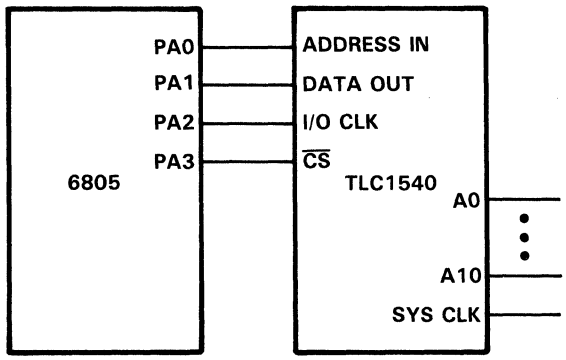


Figure 11-205. 6805 to TLC1540 Interface Circuit Diagram

Hardware

A circuit diagram for the 6805 microprocessor to TLC1540 device interface is shown in Figure 11-205. Four port pins in PORTA are used to transfer control signals and data. A system clock signal may be obtained by tapping off the oscillator input into a high impedance buffer or inverter, such as a SN74HC04, to prevent loading of the oscillator. The signal can then be divided to the required frequency. Care should be used to ensure that system clock pulse width requirements of the TLC1541 device are met.

Software

All interface control signals are generated through software manipulation of port pins. The single loop control software listing follows.

The multiplexer address should be loaded in the most significant 4 bits of the accumulator during initialization. A data bit is read into the carry bit location, rotated into the accumulator, which then rotates a multiplexer address bit out. One I/O clock pulse is then generated by toggling bit 2 of PORTA. The multiplexer address bit is latched in on the

leading edge of the I/O clock, and a data bit is shifted out on the trailing edge of the I/O clock. This procedure is placed in a loop and repeated eight times. The most significant bits are then stored in the first byte of the on-board RAM. The last two result bits are read in and stored in the second byte of RAM causing the data to be stored in a left justified format. After the results are read in, $\overline{CS}$ is brought high and should remain high until conversion is complete. Conversion requires 44 system clock cycles and a possible time delay depending on the system clock frequency. Using this program, a conversion cycle can be completed in 360 μs.

A timing diagram for a 2-loop control program is shown in Figure 11-206. The 2-loop control program listing follows Figure 11-206. This program has a loop to shift out the four multiplexer address bits and has another loop to shift in the next four bits. There are two individual clock cycles for the last two bits. Although this program uses a few more bytes of program memory, cycle time can be reduced to 312 μs. It is also possible to write a brute-force routine that uses no loops and generates 10 individual clock pulses. This routine reduces cycle time to 260 μs but requires more than twice as much program memory space.

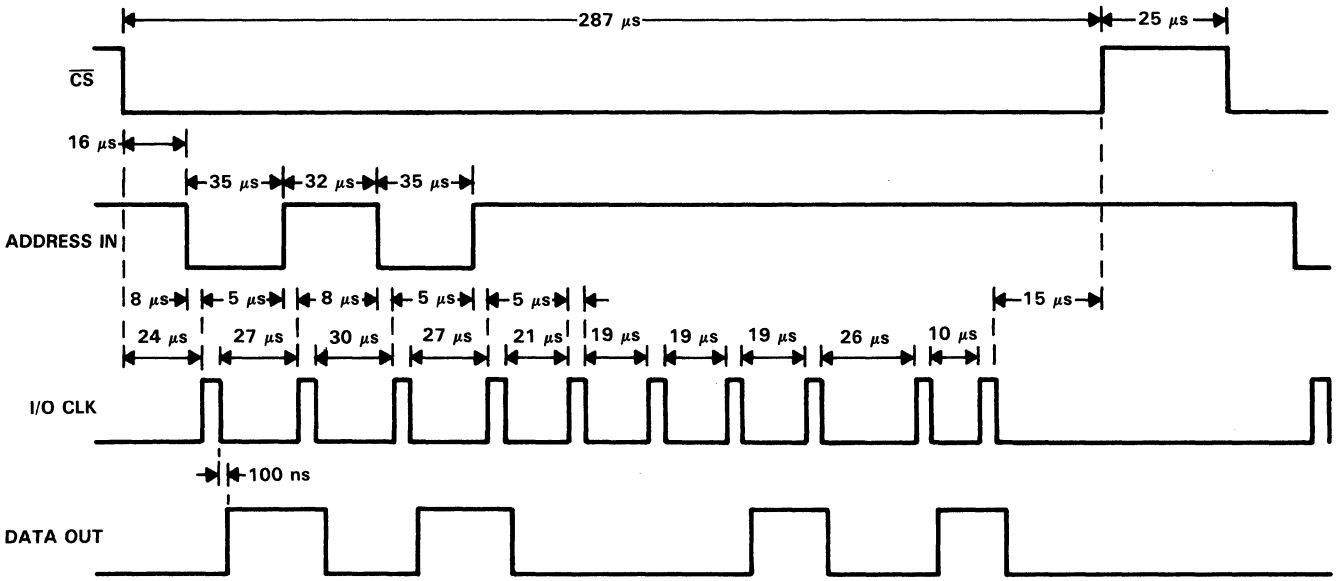


Figure 11-206. 6805 to TLC1540 Interface Timing Diagram

```
;                    Software Listing for TLC1540 and TLC1541 to
                              Motorola 6805 Interface
                    *** Register Assignments***
;
PORTA       .EQU  0000H          ; Port A I/O pins
DDRA        .EQU  0004H          ; Data direction register A
MSBS        .EQU  0010H          ; Conversion result MSB'S
LSBS        .EQU  0011H          ; Conversion result LSB'S
;
;           *** MAIN PROGRAM ***
;
START:      LDA   #0DH           ;
            STA   DDRA           ; Initialize port A I/O pins
            BSET  3,PORTA        ; Make sure /CS is high
            LDA   #50H           ; Initialize muxadd to channel 5
            LDX   #08H           ; Initialize counter
            BCLR  3,PORTA        ; Bring /CS low
```

```
;
LOOP:    BRSET 1,PORTA,LABEL1 ; Read data bit into carry
LABEL1   ROLA                 ; Rotate into accumulator
         BCS   HIGH           ; Go to high if muxadd bit is 1
         BCLR  0,PORTA        ; Write a 0 to TLC1540 address in
         JMP   CLOCK          ; Skip next instruction
HIGH:    BSET  0,PORTA        ; Write a 1 to TLC1540 address in
CLOCK:   BSET  2,PORTA        ; Bring I/O clock high
         BCLR  2,PORTA        ; Bring I/O clock low
         DECX                 ; Decrement counter
         BNE   LOOP           ; Go back for another bit
;
         STA   MSBS           ; Store MSB'S in RAM
         BRSET 1,PORTA,LABEL2 ; Read bit 1 into carry
LABEL2   ROLA                 ; Rotate into accumulator
         BSET  2,PORTA        ; Bring I/O clock high
         BCLR  2,PORTA        ; Bring I/O clock low
         BRSET 1,PORTA,LABEL3 ; Read bit 0 into carry
LABEL3   BSET  2,PORTA        ; Bring I/O clock high
         BCLR  2,PORTA        ; Bring I/O clock low
         RORA                 ; Rotate accumulator
         RORA                 ; Rotate accumulator
         STA   LSBS           ; Store LSB'S in RAM
         BSET  3,PORTA        ; Bring /CS high
```

SOFTWARE INTERFACE FOR TLC1540 AND TLC1541 DEVICES TO THE INTEL 8051 AND 8052 MICROPROCESSORS

This application describes a technique for operating the TLC1540 10-bit A/D converter with the 8051 microprocessor using software generated control signals. These signals are $\overline{CS}$, I/O clock, address input, and system clock. The system clock signal is required to drive the successive-approximation conversion process. Reference inputs allow ratiometric conversion, however, they are normally tied to V_{CC} and ground. One of 11 analog inputs or a self-test mode is selected with the on-board multiplexer. The TLC1540 device is pin-for-pin compatible with the TLC540 device to allow easy system upgrade.

Hardware

The system clock is derived from the ALE signal of the 8051 device. Another method uses a signal that is tapped off the oscillator through a high impedance buffer or inverter and divided down to the appropriate frequency. Care should be taken when using the ALE signal for the TLC1541 system clock to ensure that the high and low pulse widths are within specifications. The ALE signal is dependent upon the oscillator frequency and may not meet pulse width specifications at high oscillator frequencies. A circuit diagram is shown in Figure 11-207.

Timing Diagram

A timing diagram for the interface is shown in Figure 11-208. The subroutine can be executed in 79 μs. With a system clock of 2.1 MHz from the ALE pin, conversion results may be read every 101 μs.

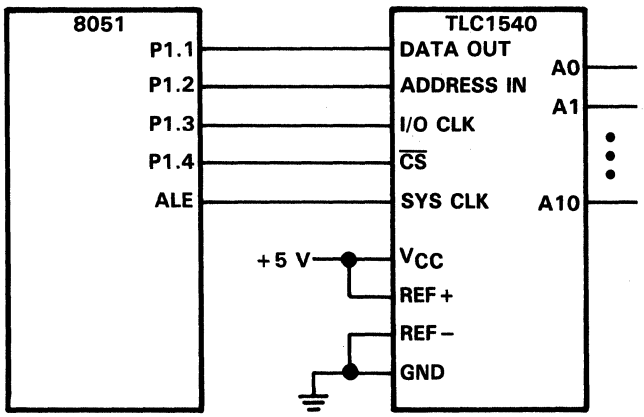


Figure 11-207. 8051 to TLC1540 Interface Circuit Diagram

Software

All interface control signals are generated through software manipulation of port pins. A subroutine is used to load a new multiplexer address and retrieve a previous conversion result. A listing of the subroutine follows the discussion.

A multiplexer address should be loaded into the most significant 4 bits of the accumulator before calling the subroutine. Previous conversion results are returned left justified, with R2 holding the eight most significant bits and R3 holding the two least significant bits. After returning from the subroutine, a delay loop is executed to allow time for the conversion. Conversion requires 44 system clock cycles, therefore, delay loops of appropriate length should be included according to the system clock frequency.

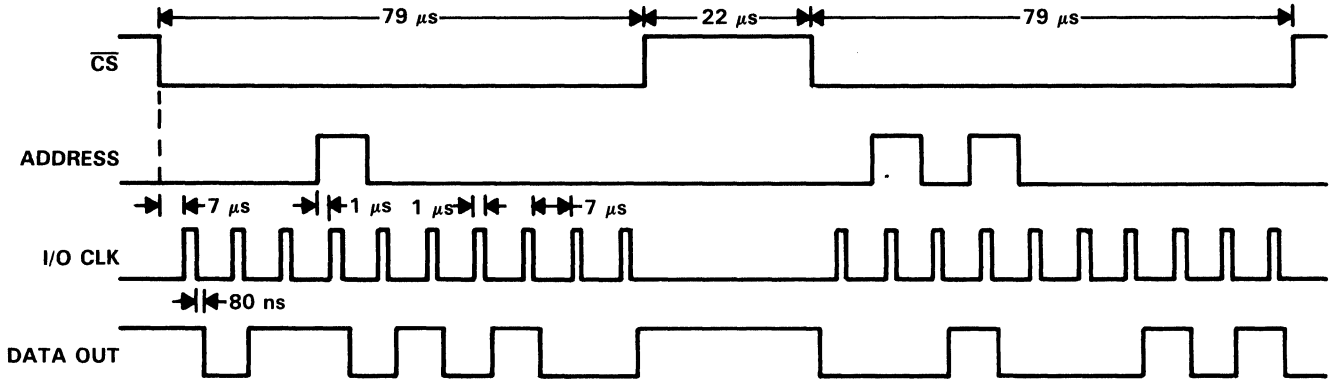


Figure 11-208. 8051 to TLC1540 Interface Timing Diagram FIGURE

```
;                Software List for TLC1540 and TLC1541 to
                      Intel 8051 and 8052 Microprocessors
            *** Main Program ***
;
START:      MOV   P1,#02H      ; Initialize port 1 I/O pins
            CLR   P1.3         ; Make sure I/O CLK is low
            SETB  P1.4         ; Make sure /CS is high
CONTINUE:   MOV   A,#10H       ; Initialize muxaddress to channel 1
            ACALL TLC1540      ; Shift muxaddress/results
            MOV   R5,#07H      ; Load counter
DELAY1:     DJNZ  R5,DELAY1    ; Delay for conversion
            MOV0A,#0H          ; Initialize muxaddress to channel 5
            ACALL TLC1540      ; Shift muxaddress/results
            MOV   R5,#07H      ; Load counter
DELAY2:     DJNZ  R5,DELAY2    ; Delay for conversion

;           *** Subroutine ***
;
TLC1540     MOV   R4,#08       ; Load counter
            CLR   P1.4         ; Bring /CS low
            NOP                ; Delay for /CS to go low
            NOP                ;
LOOP:       MOV   C,P1.1       ; Read data bit into carry
            RLC   A            ; Rotate into accumulator
            MOV   P1.2,C       ; Write muxadd bit out
            SETB  P1.3         ; I/O clock high
            CLR   P1.3         ; I/O clock low
            DJNZ  R4,LOOP      ; Go back and get another bit
            MOV   R2,A         ; Store MSB'S in R2
            MOV   C,P1.1       ; Read data bit into carry
            CLR   A            ; Clear accumulator
            RLC   A            ; Rotate data bit into accumulator
            SETB  P1.3         ; I/O clock high
            CLR   P1.3         ; I/O clock low
            MOV   C,P1.1       ; Read data bit into carry
            RRC   A            ; Rotate right into accum MSB
            RRC   A            ; Rotate right into accum MSB
            MOV   R3,A         ; Store LSB'S in R3
            SETB  P1.3         ; I/O clock high
            CLR   P1.3         ; I/O clock low
            SETB  P1.4         ; Bring /CS high
            RET                ; Return to main program
```

HARDWARE INTERFACE FOR THE TLC545 DEVICE TO THE ZILOG Z80A MICROPROCESSOR

This application describes a technique for interfacing the TLC545 A/D converter to the Z80A microprocessor. The TLC545 device is a complete data acquisition system on a chip. The system includes an analog multiplexer, sample-and-hold, 8-bit A/D converter, and microprocessor control inputs. These inputs are $\overline{CS}$, address in, system clock, and I/O clock. The system clock and I/O clock require no special speed or phase relationship, and are normally used independently. This allows the system clock to run up to 4 MHz to ensure a conversion time of less than 9 μs while the I/O clock runs up to 2.1 MHz to allow a maximum data transfer rate.

Principles of Operation

The circuit shown in Figure 11-209 initiates conversion with an OUT instruction. The timing diagram for this circuit is shown in Figure 11-210. When $\overline{IORQ}$ and $\overline{WR}$ go low, $\overline{CS}$ is brought low while the universal shift register is placed in the load data mode and the system clock is enabled to the clock input to latch in the multliplexer address. The multiplexer address should occupy the five most significant bits of the shift register since the data is shifted out to the left. The rising edge of $\overline{IORQ}$ enables the I/O clock to the shift register, which shifts the multiplexer address out while shifting in the previous conversion result. Sampling begins at the falling edge of the fourth I/O clock cycle and continues until the eighth falling edge occurs. At this time the I/O clock is disabled and $\overline{CS}$ is brought high to ensure that the TLC545 device will remain undisturbed during the conversion. Conversion of the addressed analog input requires 36 system clock cycles. During conversion time, previous conversion results may be read by using an IN instruction. A typical interrupt service routine is shown below.

At least 36 system clock cycles must be used for conversion to ensure proper operation. If a new multiplexer address is shifted in while a conversion is in progress, the ongoing conversion will be aborted and a new conversion will be initiated at the falling edge of the eighth I/O clock cycle. Another software approach is to initiate a new conversion, wait in a delay loop until the conversion is complete, and then read in the previous conversion results. A sample program segment using the delay loop method follows this discussion. Using this method, a conversion cycle can be completed in 21.5 μs.

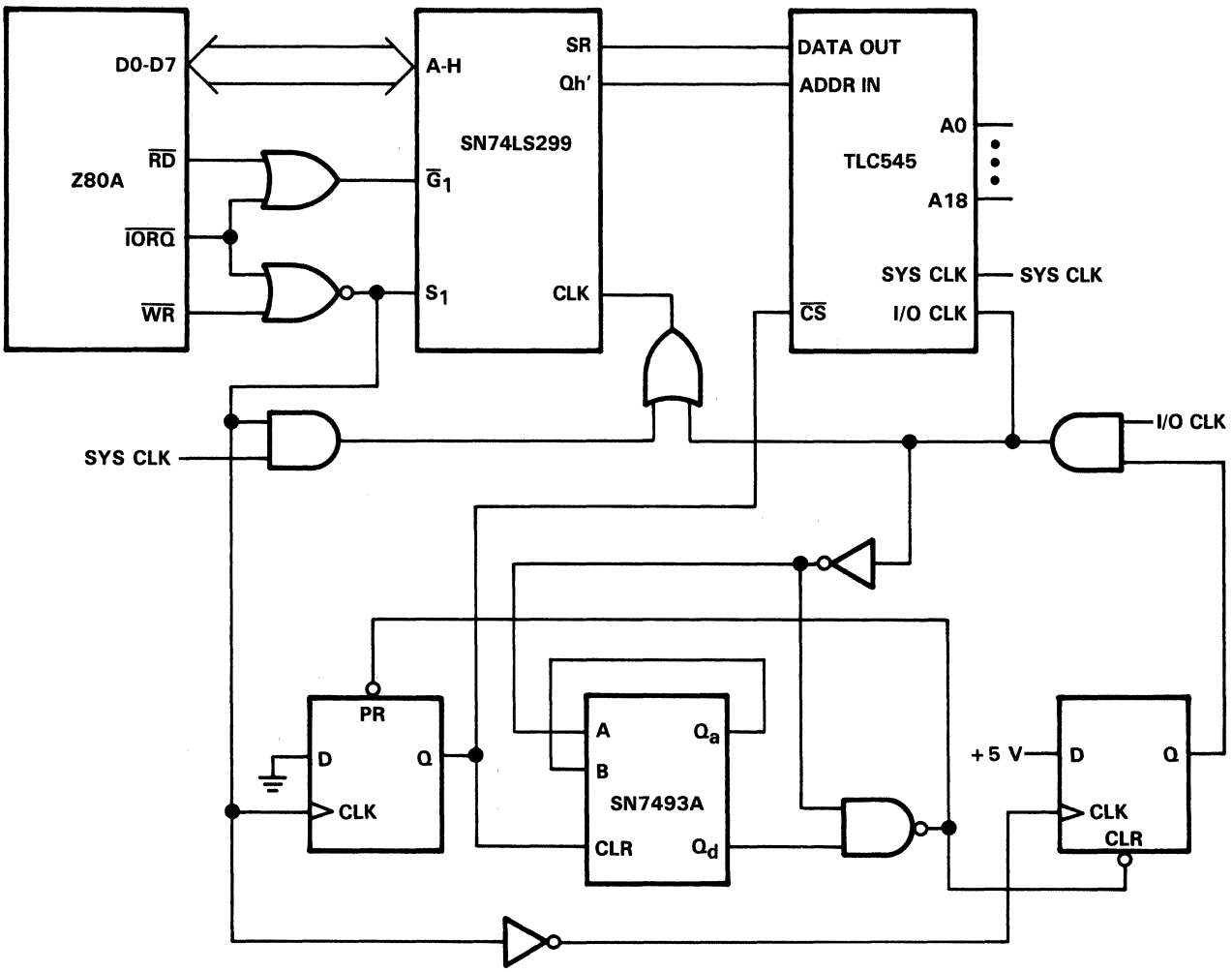


Figure 11-209. Z80A to TLC545 Interface Circuit Diagram

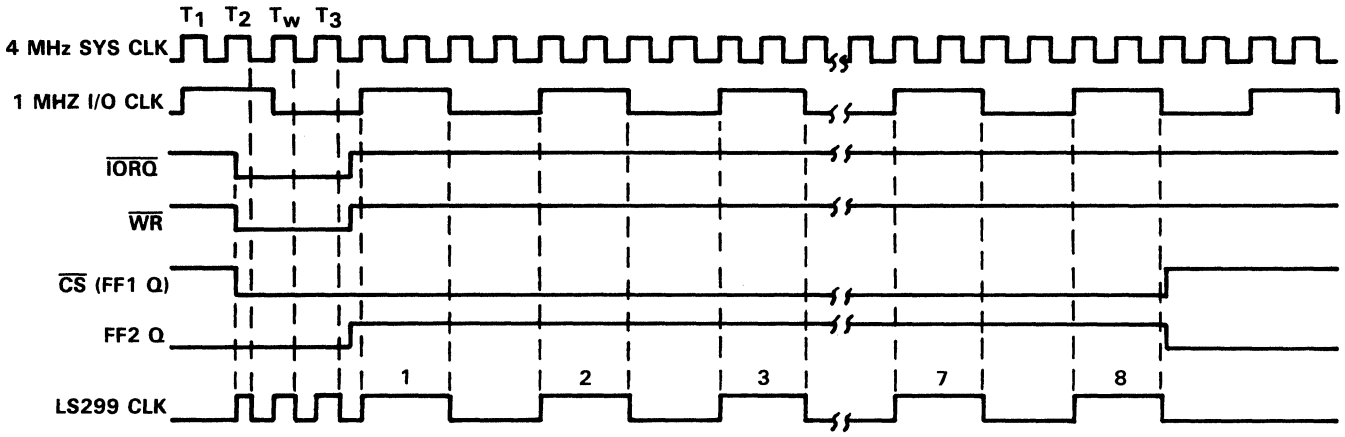


Figure 11-210. Z80A to TLC545 Interface Timing Diagram

```
ISR     EX AF,AF                ; Save accumulator
        IN A,(LS299)            ; Read previous conv. result
        LD (DATA), A            ; Store result
        LD A, (MUXADDRESS)      ; Load new mux address from RAM
        OUT (LS299),A           ; Initiate new conversion cycle
        EX AF,AF'               ; Restore accumulator
        EI
        RETI

        LD A, (MUXADDRESS)      ; Load mux address from RAM
        OUT (LS299),A           ; Sample channel & initiate conv.
        LD C,03H                ; Initialize counter
WAIT:   DEC C                   ; Decrement counter
        JP NZ, WAIT             ; If not zero keep waiting
        OUT (LS299),A           ; Shift results into LS299
        IN A,(LS299)            ; Read conv results
```

NOTE: A count of 03H will produce a delay of 10.50 μs, suitable for 4 MHz operation, while a count of 05H produces a delay of 17.50 μs, suitable for 2.5 MHz operation.

SOFTWARE INTERFACE FOR THE TLC545 DEVICE TO THE ZILOG Z80A MICROPROCESSOR

This application describes a technique for operating the TLC545 A/D converter with the Z80A microprocessor using software generated control signals. These signals are $\overline{CS}$, address in, I/O clock, and system clock. The system clock is needed to drive the successive-approximation conversion process. The system clock and the I/O clock require no special speed or phase relationship and are normally used independently. This allows the system clock to run up to 4 MHz to ensure conversion in less than 9 μs while the I/O clock runs up to 2.1 MHz to allow a maximum data transfer rate. Reference inputs allow ratiometric conversion; however, they are normally tied to V_{CC} and ground. One of 19 analog inputs or a self-test mode is selected with the on-board analog multiplexer. Timing for the TLC545 device is identical to the TLC540 device with the exception that one additional multiplexer address bit must be shifted out to address the additional analog inputs.

Principles of Operation

The circuit diagram for the software controlled Z80A microprocessor to TLC545 device interface is shown in Figure 11-211. Circuit timing is shown in Figure 11-212.

Execution of an IN instruction causes the $\overline{RD}$ line and the $\overline{IORQ}$ line to become active and shift an address bit in and a data bit out of the TLC545 device. $\overline{CS}$ is brought low by latching in a low from address bit A0 on the positive going edge of the $\overline{WR}$ signal. A simple program segment listing that shifts out a new analog multiplexer address while also shifting in previous conversion results follows the discussion.

This program segment uses the B register to store the conversion result, the C register as a bit counter, and the D register to hold the analog multiplexer address. The analog multiplexer address is shifted left out of the D register, therefore, the 5-bit address must be placed in the five most significant bits of the byte.

Conversion results are read in one bit at a time and then shifted left to the proper position in the B register.

Sampling of the addressed input begins at the falling edge of the fifth I/O clock and continues until the falling edge of the eighth I/O clock when conversion begins. Conversion requires 36 system clock cycles, therefore, an appropriate software delay that depends upon the system clock frequency must be included. If a new multiplexer address is shifted into the TLC545 device before a conversion has been completed, the ongoing conversion will be aborted and a new conversion cycle will begin at the eighth falling edge of the I/O clock. $\overline{CS}$ is brought high after the eighth falling edge of the I/O clock to ensure that extraneous noise or glitches on the I/O clock line are not interpreted as the begining of a new cycle. Using the program segment just presented with the system clock at 4 MHz, it is possible to initiate a new conversion cycle and read the results of the previous conversion in 138 μs as indicated in Figure 11-212.

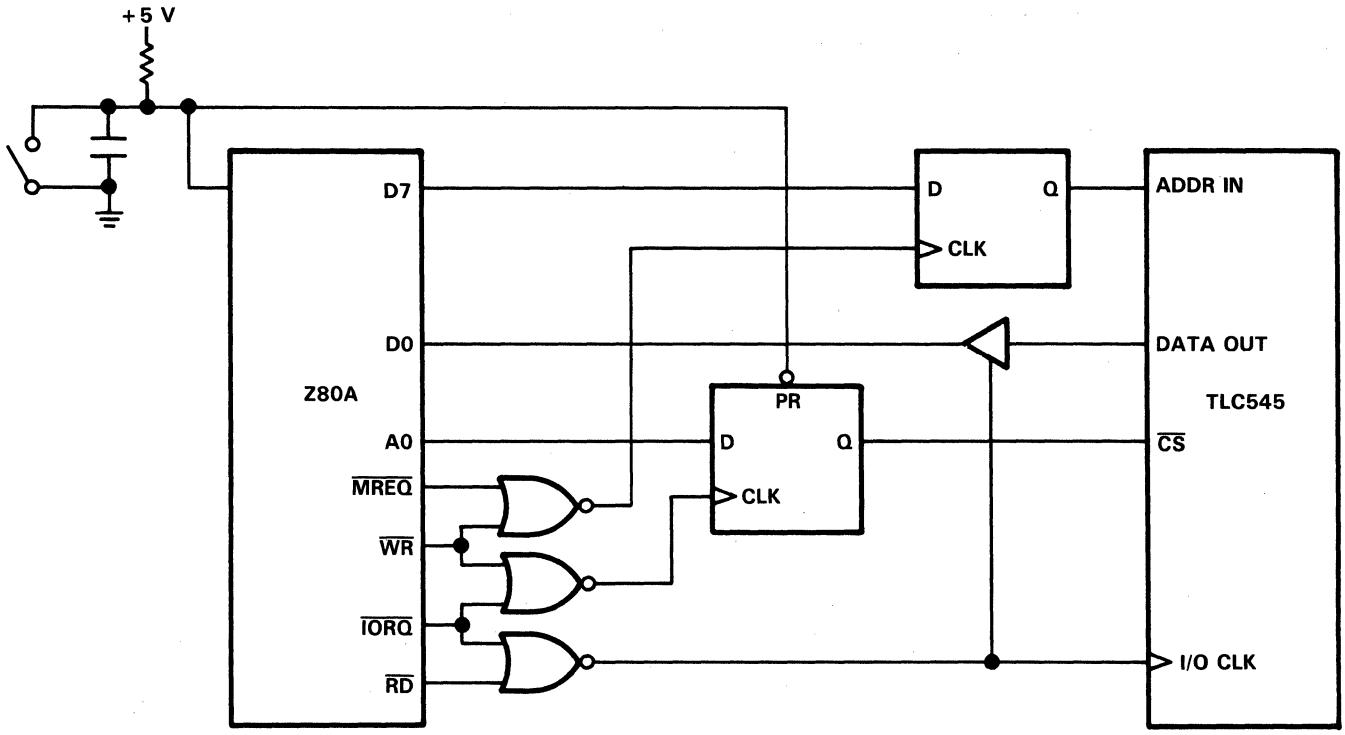


Figure 11-211. Z80A to TLC545 Software Interface Circuit Diagram

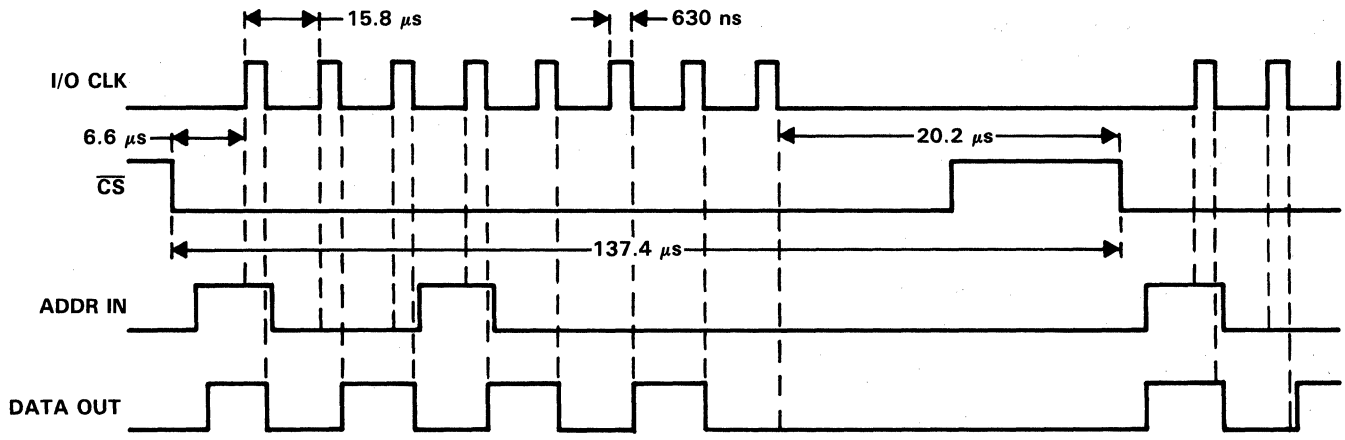


Figure 11-212. Z80A to TLC545 Software Interface Timing Diagram

```
;          *** REGISTER ASSIGNMENTS ***
;
CSLOW      .EQU 0100H        ; A0=0
CSHIGH     .EQU 0101H        ; A0=1
BIT        .EQU 00FFH        ; Arbitrary address
;
;          *** MAIN PROGRAM ***
;
           LD C,08           ; Initialize bit counter
           LD B,00           ; Clear result register
           OUT (CSLOW),A     ; Bring chip select low
LOOP       RLC B             ; Rotate result left
           LD (HL),D         ; Latch address bit into D FF
           IN A, (BIT)       ; Read in data bit
           AND 01H           ; Mask off bit 0
           OR B              ; Or new bit into result reg.
           LD B,A            ; Store in result register
           RLC D             ; Shift address left
           DEC C             ; Decrement bit counter
           JP NZ,LOOP        ; Get another bit if not zero
           OUT (CSHIGH),A    ; Bring chip select high
```

SOFTWARE INTERFACE FOR THE TLC545 AND TLC546 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS

Two interface circuits are discussed in this application. The Interface 1 circuit diagram and associated timing diagram are shown in Figure 11-213 and Figure 11-214, respectively. A software listing of Interface 1, in which the A/D clock signal is derived from the microprocessor ALE clock, follows the illustrations.

Figure 11-215 and Figure 11-216 show the Interface 2 circuit diagram and associated timing diagram. The software listing for this interface follows the illustrations.

These interfaces minimize the amount of hardware and rely mainly upon software techniques. Although the amount of hardware and its cost are reduced, the use of more software increases the time required to load the address into, and retrieve the conversion data from, the A/D converter. However, the trade-off of minimum hardware versus longer conversion time may benefit many designs.

Hardware

The interface shown in Figure 11-213 will always work with the TLC545 device, but will not work with the TLC546 device at the higher microprocessor instruction cycle frequencies. Before using the TLC546 device, the designer must verify that the high and low pulse widths of the ALE clock signal meet the specifications of the TLC546 device. These pulse widths are dependent upon the microprocessor instruction cycle frequency.

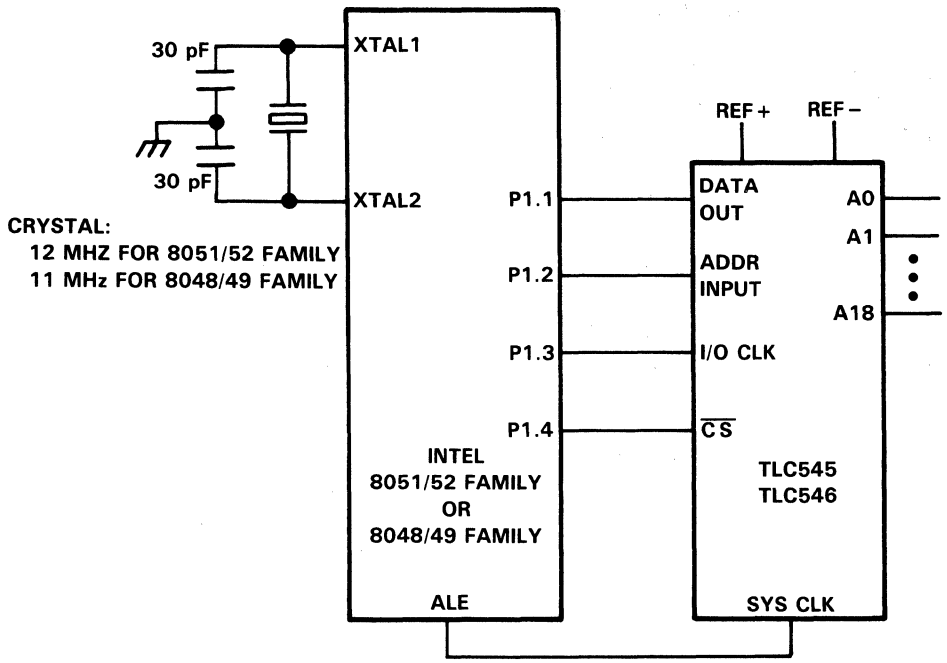
In the A/D converter of Figure 11-215, the system clock for the A/D converter is obtained from the microprocessor crystal oscillator. To assure proper operation of the crystal oscillator, a high impedance buffer must be used to tap the signal from the oscillator. An important detail is that low and high level input buffer requirements must lie within the range of the oscillator signal. This compatibility will prevent missing edge transitions in the A/D converter's system clock signal. Subsequently, the buffered crystal oscillator signal must be frequency divided to assure that the resulting system clock signal does not exceed the upper frequency specification of the A/D converter. Any convenient divider circuitry may be used to accomplish this task.

Timing Diagrams

Figures 11-214 and 11-216 show the timing diagrams for the A/D conversions of Interfaces 1 and 2, respectively. Loading the new address and retrieving the conversion for the previous address requires 137 μs maximum. The conversion period requires 36 system clocks. This period is longer for the TLC546 device since the microprocessor clock frequency (see Figure 11-213) or the A/D clock frequency (see Figure 11-215) must be lower to satisfy the TLC546 device specifications.

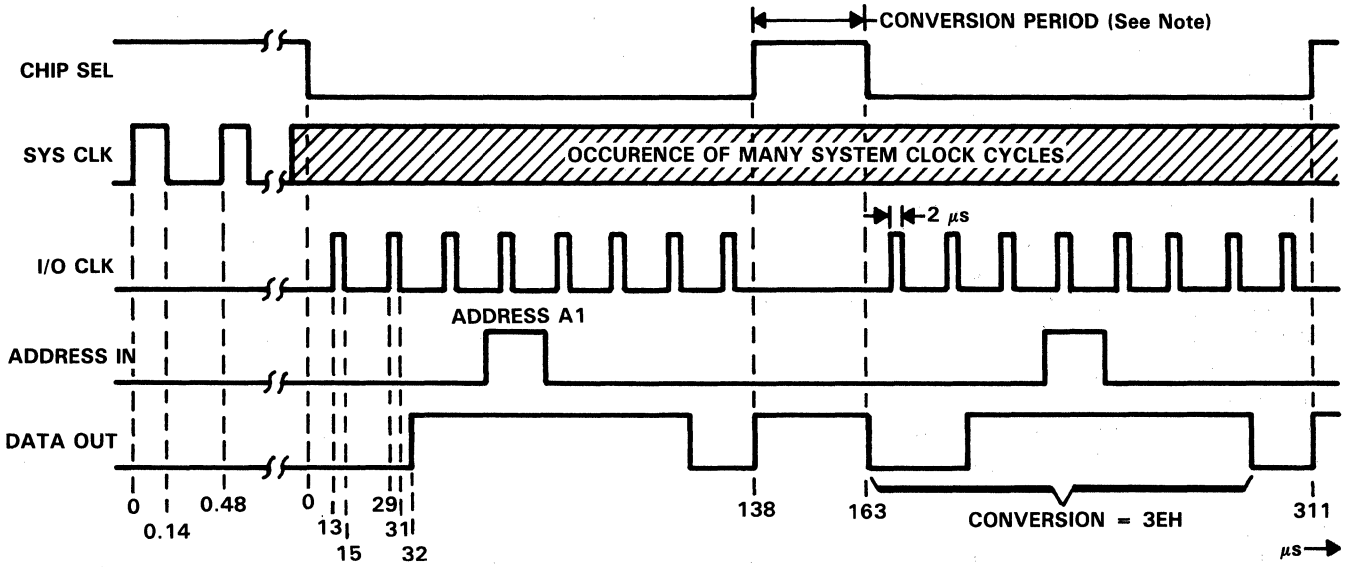
Software

Refer to the software listings for Interfaces 1 and 2 for the following discussion. The software uses a subroutine, ACALL that simultaneously loads the A/D converter with a new address and retrieves the conversion result for the previous address. This subroutine can be used any time the designer desires to load a new address and retrieve a conversion value. This simultaneous loading and retrieving makes the subroutine very appropriate for continuous monitoring of several A/D converter analog inputs. The subroutine assumes that the new address has been prevously placed in the five most significant bits of register R2. Upon completion of the subroutine, the conversion result for the previous address is left in the accumulator.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751H/80C51
INTEL 8048/49 FAMILY: 8048AH/8748H/8035AHL/8049AH/8749H/8039AHL/8050AH/8040AHL/80C49

Figure 11-213. TLC545 and TLC546 to Intel Microprocessor Interface 1 Diagram



NOTE: Conversion period requires 36 system clock cycles after 8th I/O clock goes low upon clocking in the address.

Figure 11-214. Timing Diagram of an A/D Conversion Cycle for TLC545 and TLC546 to Intel 8048/8049 and 8051/8052

```
; Software Listing for Intel 8051/52 to TLC545/546 Interface 1
;
                CLR P1.3            ;Lower I/O clock
                MOV R2,#10H         ;Load A/D analog input address. Note
                                    ;that to send address = A2, R2 = 10H.
                ACALL S545D         ;Load 545 address, assumes the address
                                    ;is currently in R2.
;
                MOV R3,#09H         ;This software loop allows a
                                    ;conserative 40 A/D system clocks,
                                    ;since only 36
DELAY:          DJNZ R3,DELAY       ;clocks are required to perform
                                    ;conversion, to be emitted from the
                                    ;microprocessor ALE pin
;
                MOV R2,#10H         ;Load A/D analog input address. Note
                                    ;that to send address = A2, R2 = 10H.
                ACALL S545D         ;Load new 545 address, assumes this
                                    ;address is in R2; leaves the
                                    ;conversion result for the previous
                                    ;address in A
;
;               Subroutine ACALL
;
S545D           MOV R6,#08H         ;Set bit counter to 8
                CLR P1.4            ;Lower chip select
S545DL:         CLR C               ;Initialize C = 0
                JNB P1.1,S545DI     ;If 545 Data Out = 0; branch
                CPL C               ;545 Data Out = 1; set C = 1
S545DI:         MOV A,R2            ;Get serial buffer
                RLC A               ;Shift Data Out bit into serial
                                    ;buffer and shift 545 address
                MOV R2,A            ;Store serial buffer
                JNC S545DWO         ;If 545 address bit = 0; branch
                ORL P1,#04H         ;Set 545 address line to 1
                SJMP S545DWE        ;Go and raise the I/O clock
S545DWO:        ANL P1,#FBH         ;Set 545 address line to 0
S545DWE:        NOP                 ;Allow address line to setup
                CPL P1.3            ;Raise I/O clock
                NOP                 ;Delay to slow I/O clock
                CLR P1.3            ;Lower I/O clock
                DJNZ R6,S545DL      ;Do all 8 bits
                CPL P1.4            ;Raise chip select
                MOV A,R2            ;Get serial buffer
                RET
                END
```

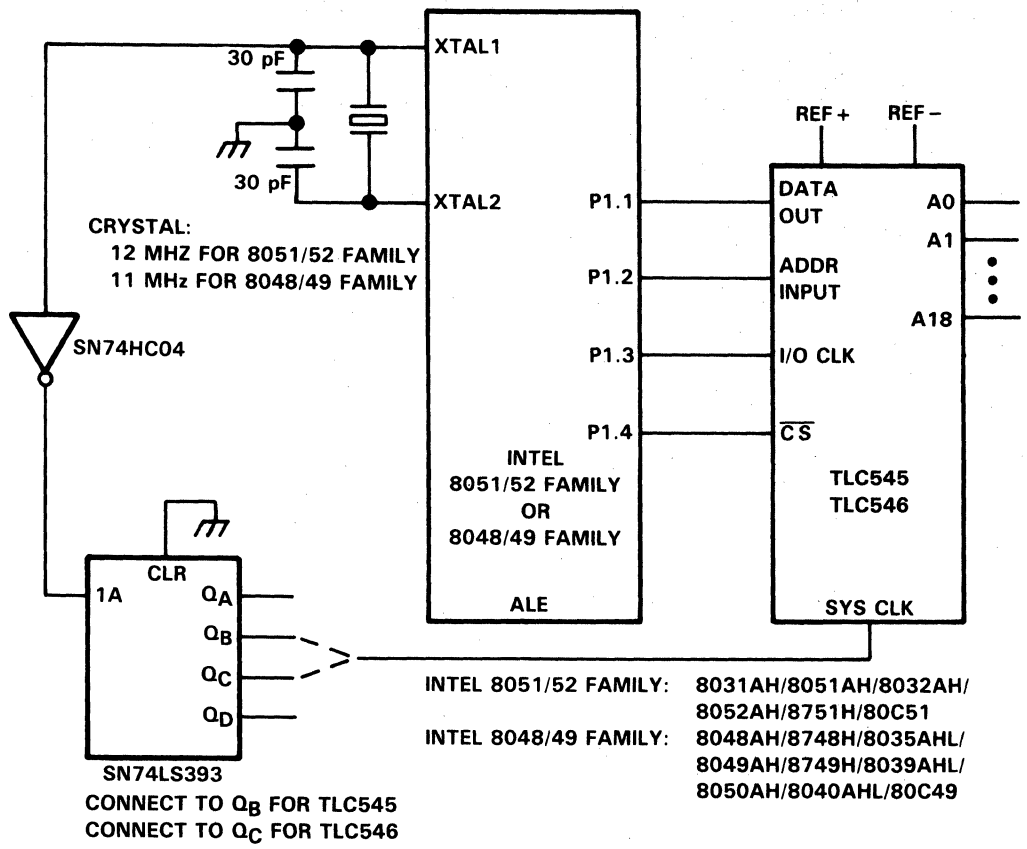
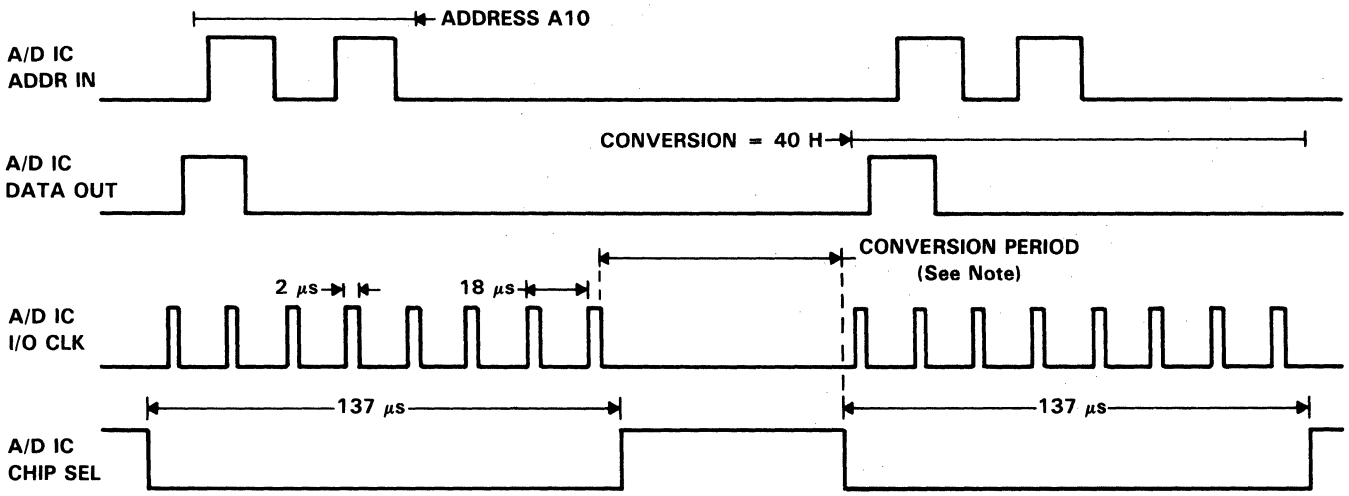


Figure 11-215. TLC545 and TLC546 to Intel Microprocessor Interface 2 Diagram



NOTE: Conversion period requires 36 system clock cycles after 8th I/O clock goes low upon clocking in the address.

Figure 11-216. Timing Diagram of an A/D Conversion Cycle for TLC545 and TLC546 to Intel 8048/8049 and 8051/8052

```
; Software Listing for Intel 8051/31 - TLC545/546 Interface 2
;
                CLR P1.3            ;Lower I/O clock
                MOV R2, #50H        ;Load A/D analog input address. Note
                                    ;that to send address = A10, R2 = 50H.
                ACALL S545D         ;Load 545 address, assumes the address
                                    ;is currently in R2.
;
;               A delay must occur here to allow the A/D IC to complete
;               conversion. The delay must allow 36 A/D IC system clock
;               cycles to occur.
;
                MOV R2, #50H        ;Load A/D analog input address. Note
                                    ;that to send address = 10, R2 = 50H.
                ACALL S545D         ;Load new 545 address, assumes this
                                    ;address is in R2; leaves the
                                    ;conversion result for the previous
                                    ;address in A
;
;               Subroutine ACALL
;
S545D           MOV R6, #08H        ;Set bit countr to 8
                CLR P1.4            ;Lower chip select
S545DL:         CLR C               ;Initialize C = 0
                JNB P1.1,S545DI     ;If 545 Data Out = 0; branch
                CPL C               ;545 Data Out = 1; set C = 1
S545DI:         MOV A,R2            ;Get serial buffer
                RLC A               ;Shift Data Out bit into serial
                                    ;buffer and shift 545 address
                MOV R2,A            ;Store serial buffer
                JNC S545DWO         ;If 545 address bit = 0; branch
                ORL P1, #04H        ;Set 545 address line to 1
                SJMP S545DWE        ;Go and raise the I/O clock
S545DWO:        ANL P1, #FBH        ;Set 545 address line to 0
S545DWE:        NOP                 ;Allow address line to setup
                CPL P1.3            ;Raise I/O clock
                NOP                 ;Delay to slow I/O clock
                CLR P1.3            ;Lower I/O clock
                DJNZ R6,S545DL      ;Do all 8 bits
                CPL P1.4            ;Raise chip select
                MOV A,R2            ;Get serial buffer
                RET
                END
```

SERIAL PORT INTERFACE FOR TLC545 AND TLC546 DEVICES TO INTEL 8051 AND 8052 MICROPROCESSORS

Two interface circuits are presented for this application. Figures 11-217, 11-218, and a software listing support Interface 1 in which the A/D clock signal is derived from the microprocessor ALE clock. Figures 11-219, 11-220, and a software listing support Interface 2 in which the A/D clock signal is derived from the microprocessor crystal oscillator. These interfaces not only use a low cost A/D converter, but also require minimal hardware and provide quick conversion and A/D microprocessor communications. They also provide the remote location possibilities of a serial A/D converter. This application is an excellent one if the Intel microprocessor's serial port does not have to be used for another purpose. Even if another purpose is required, the serial port may be multiplexed through good design so both the A/D converter and the additional purpose may be accommodated by the serial port.

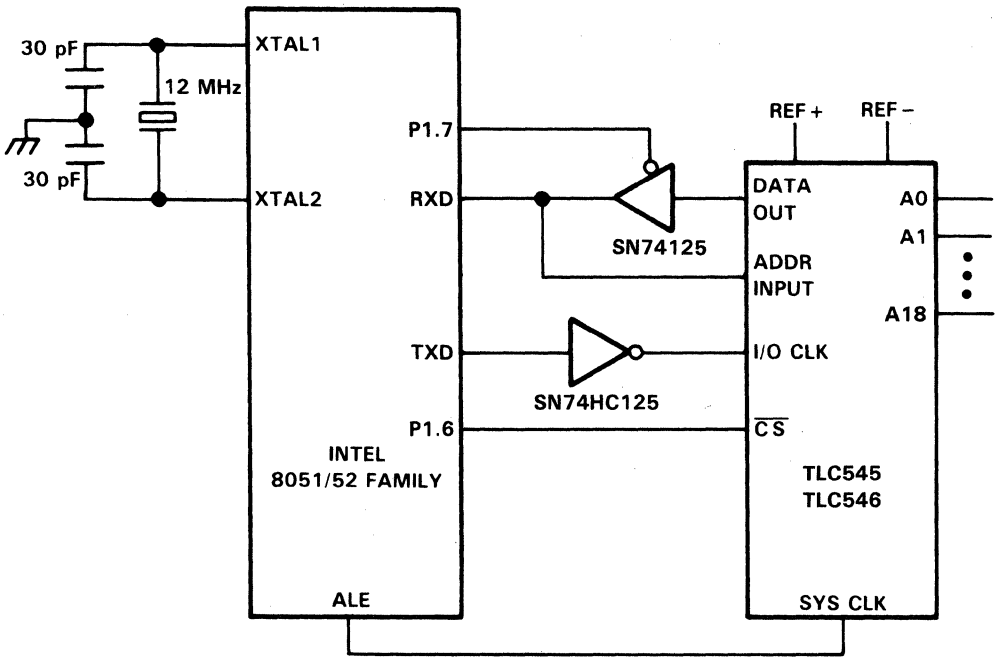
Hardware

The circuit is presented in Figures 11-217 and 11-219. The signal at the microprocessor's TXD pin must be inverted so the communication protocols for the microprocessor serial port and the A/D converter are compatible. Use of an SN74125 3-state buffer allows the microprocessor serial port

to be used for both transmission and reception. Use of the 3-state buffer prevents the simultaneous loading of a new address while retrieving the conversion of a previously loaded address. However, this time loss is small because the serial port can quickly load an address and retrieve the resulting conversion.

Timing Diagram

Figures 11-218 and 11-220 are the timing diagrams for an A/D conversion for each of the two circuits. With the TLC545 device, loading the address, waiting for conversion, and retrieving the conversion result requires 56 μs for Interface 1 and 48 μs for Interface 2. This time period is longer for the TLC546 device since the system clock frequency must be lower for this device.



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751AH/80C51

Figure 11-217. TLC545 and TLC546 to Intel Microprocessor Interface 1 Diagram

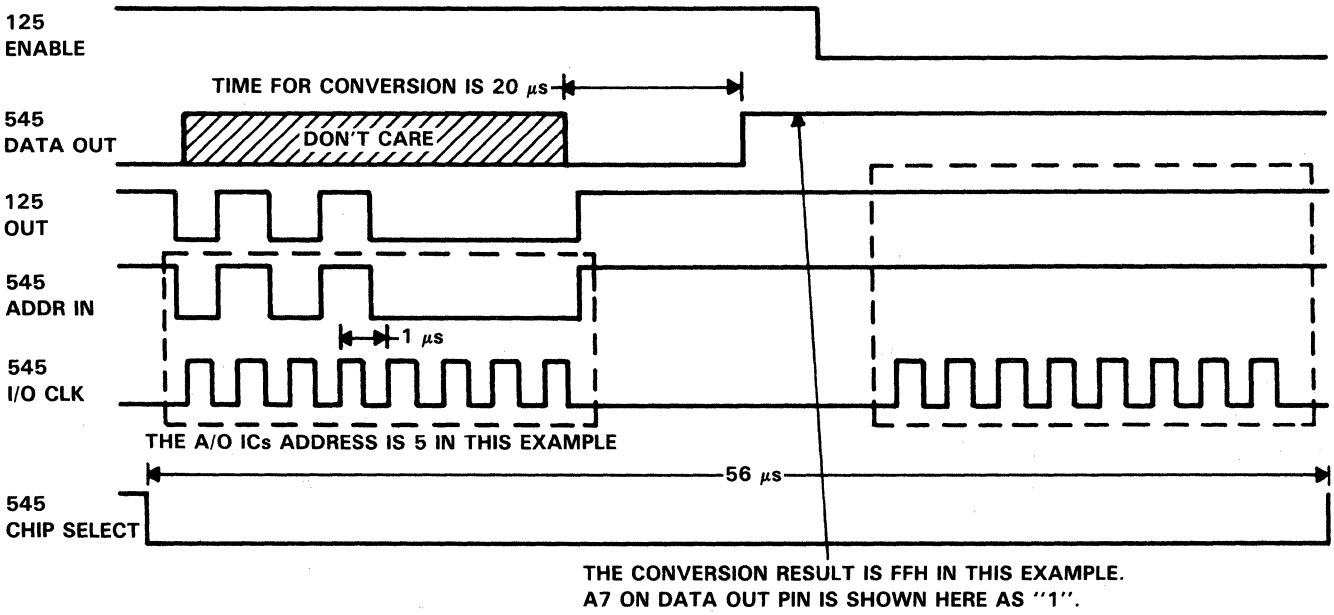
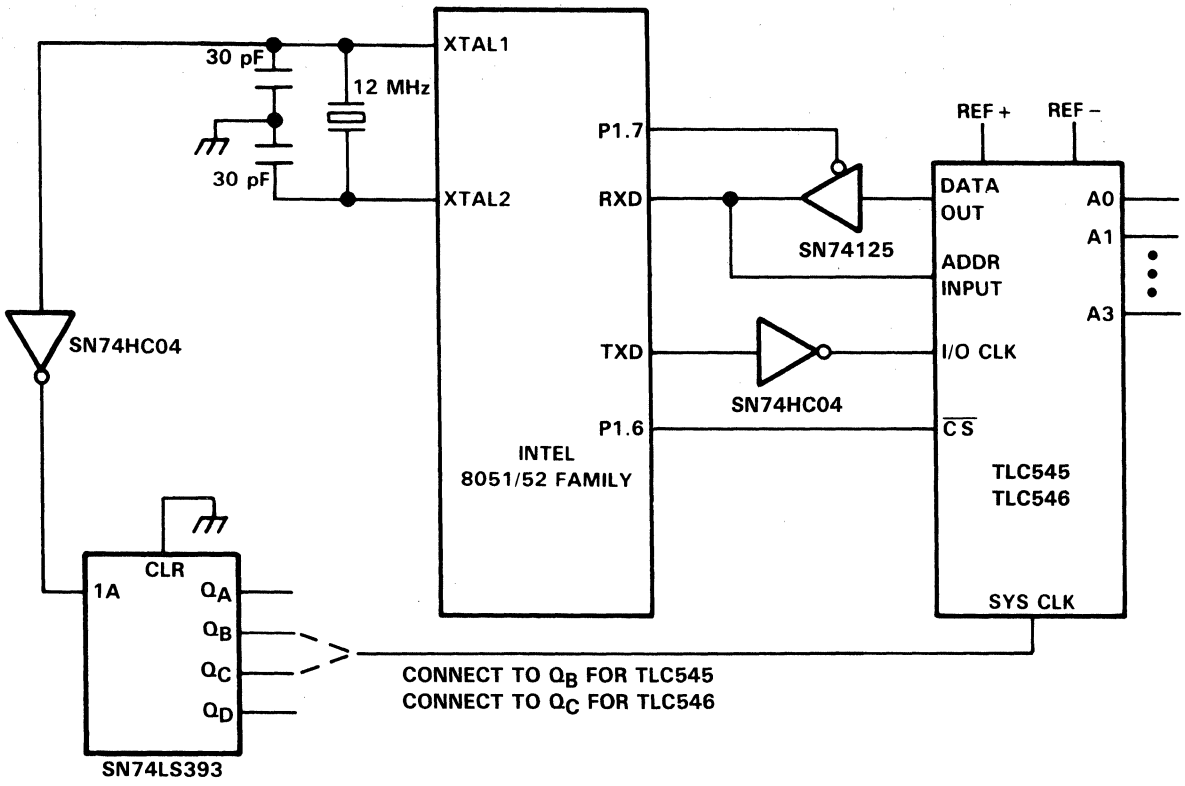


Figure 11-218. Timing Diagram for an A/D Conversion

Software

Refer to the interface software listings presented earlier. The serial port mode 0 is used. If desired, the software can be incorporated into a subroutine so the designer can address the software with a simple subroutine call. Particular attention must be exercised when placing the address bits in the serial buffer since the serial port sends the least significant bit of the address first and the A/D converter accepts this bit as the most significant bit of the address. A similar process occurs when the serial port receives the conversion result.

```
; Software Listing for Intel 8051/52 Family - TLC545/546 Interface 1
;
SR545L;         MOV A, #0AH          ;A/D IC address of A16 in this example
;
;The serial port will send 0A(00001010) with the least significant
;bit first. Therefore, the A/D IC will see (01010000), which
;will load an address of A16 into the control register.
;
                CLR P1.7             ;Disable 125
                CPL P1.7
                CLR P1.6             ;Lower chip select
                ANL SCON,#4EDH       ;Reset REN & TI flags
                MOV SBUF,A           ;Send 545 address (LSB FIRST)
SNDTST:         JNB SCON.1,SNDTST    ;TI flag not set; branch
                                     ;until transmission is complete
;
;A delay must occur here to allow the A/D IC to complete
:conversion. The delay must allow 36 A/D IC system clock
;cycles to occur.
;
                CPL P1.7             ;Enable 125
                ORL SCON, #10H       ;Set REN
                ANL SCON, #FEH       ;Reset RI
RCVTST:         JNB SCON.0,RCVTST    ;RI FLAG not set; branch
                                     ;until reception is complete
                CPL P1.6             ;Raise chip select
                MOV A,SBUF           ;Set SBUF
;
;The serial port read reverses the data conversion bits coming
;to the microprocessor so that they are in the following order:
;b0(lsb),b1,b2,b3,b4,b5,b6,b7(msb). These bits (01234567) along
;with the carry bit (C) in the following instruction comments are
;presented so that the reader will understand the technique, which
;is used to place the bits in their proper order.
;
                RLC A                ; 6543210C 7; b7 is now in carry
                RLC A                ; 543210C7 6; b6 is now in carry
                MOV ACC.1,C          ; 54321067 6; put b6 into ACC.1
                MOV C,ACC.2          ; 54321067 0; put b0 into C
                RLC A                ; 43210670 5; b5 is now in carry
                MOV ACC.3,C          ; 43215670 5; put b5 into ACC.3
                MOV C,ACC.4          ; 43215670 1; put b1 into C
                RLC A                ; 32156701 4; b4 is now in carry
                MOV ACC.5,C          ; 32456701 4; put b4 into ACC.5
                MOV C,ACC.6          ; 32456701 2; put b2 into C
                RLC A                ; 24567012 3; b3 is now in carry
                MOV ACC.7,C          ; 34567012 3; put b3 into ACC.7
                RL A                 ; 45670123  ; prepare for SWAP A
                SWAP A               ; 01234567  ; bits are ordered correctly
                                     ; conversion result is in accumulator
```



INTEL 8051/52 FAMILY: 8031AH/8051AH/8032AH/8052AH/8751AH/80C51

Figure 11-219. TLC545 and TLC546 to Intel Microprocessor Interface 2 Diagram

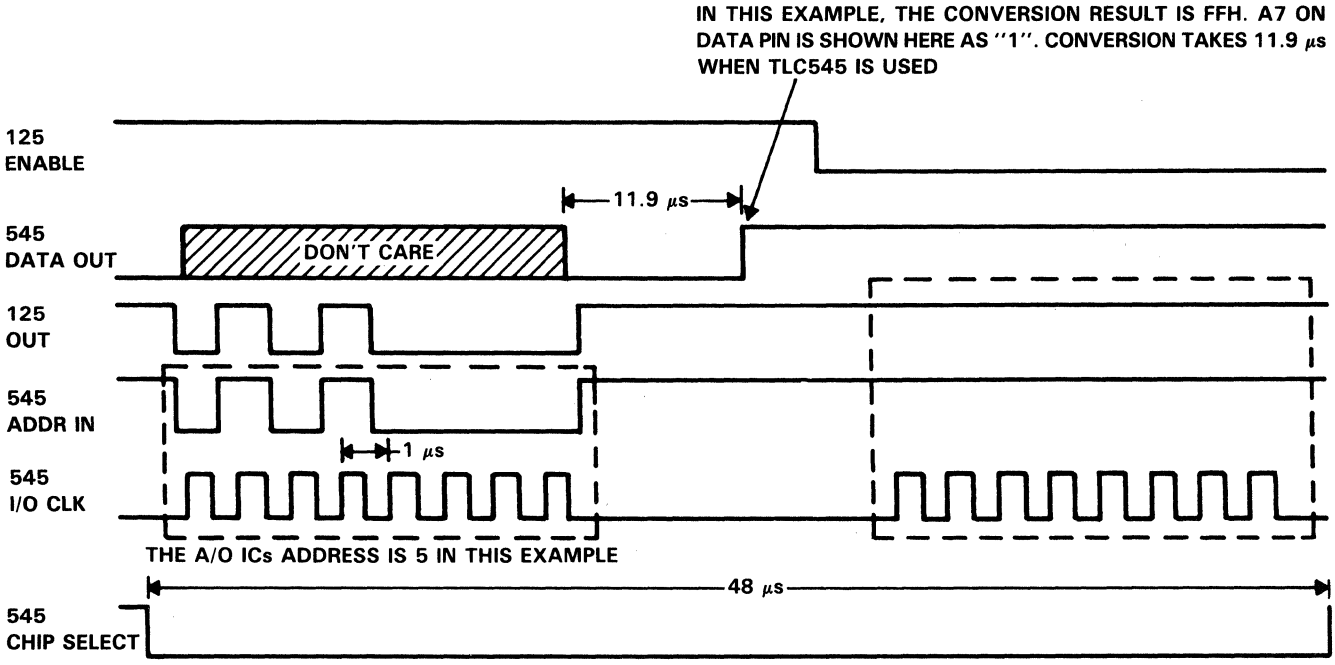


Figure 11-220. Timing Diagram for an A/D Conversion

```
; Software Listing for Intel 8051/52 Family - TLC545/546 Interface 2
;
SR545L;         MOV A, #0AH          ;A/D IC address of A16 in this example
;
;The serial port will send 0A(00001010) with the least significant bit first. Therefore, the A/D
;IC will see (01010000), which will load an address of A16 into the control register.
;
                CLR P1.7             ;Disable 125
                CPL P1.7
                CLR P1.6             ;Lower chip select
                ANL SCON, #EDH       ;Reset REN & TI flags
                MOV SBUF,A           ;Send 545 address (LSB FIRST)
SNDTST:         JNB SCON.1,SNDTST    ;TI flag not set; branch
                                     ;until transmission is complete
;
                MOV R3, #09H         ;This software loop allows a
                                     ;conservative 40 A/D system clocks,
                                     ;since only 36
DELAY:          DJNZ R3,DELAY        ;clocks are required to perform
                                     ;conversion, to be emitted from the
                                     ;microprocessor ALE pin
;
                CPL P1.7             ;Enable 125
                ORL SCON, #10H       ;Set REN
                ANL SCON, #FEH       ;Reset RI
RCVTST:         JNB SCON.0,RCVTST    ;RI FLAG not set; branch
                                     ;until reception is complete
                CPL P1.6             ;Raise chip select
                MOV A,SBUF           ;Set SBUF
;
;The serial port read reverses the data conversion bits coming
;to the microprocessor so that they are in the following order:
;b0(lsb),b1,b2,b3,b4,b5,b6,b7(msb). These bits (01234567) along
;with the carry bit (C) in the following instruction comments are
;presented so that the reader will understand the technique, which
;is used to place the bits in their proper order.
;
                RLC A                ; 6543210C 7; b7 is now in carry
                RLC A                ; 543210C7 6; b6 is now in carry
                MOV ACC.1,C          ; 54321067 6; put b6 into ACC.1
                MOV C,ACC.2          ; 54321067 0; put b0 into C
                RLC A                ; 43210670 5; b5 is now in carry
                MOV ACC.3,C          ; 43215670 5; put b5 into ACC.3
                MOV C,ACC.4          ; 43215670 1; put b1 into C
                RLC A                ; 32156701 4; b4 is now in carry
                MOV ACC.5,C          ; 32456701 4; put b4 into ACC.5
                MOV C,ACC.6          ; 32456701 2; put b2 into C
                RLC A                ; 24567012 3; b3 is now in carry
                MOV ACC.7,C          ; 34567012 3; put b3 into ACC.7
                RL A                 ; 45670123  ; prepare for SWAP A
                SWAP A               ; 01234567  ; bits are ordered correctly
                                     ; conversion result is in accumulator
```

INTERFACE FOR THE TLC545 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING TTL GATES

The TLC545 A/D converter can be operated with the 6502 microprocessor using several methods. This application presents the design of an interface using TTL gates. Another method using the 6522 VIA is described in the next application. Cost and performance are the basic trade-offs between the two designs. The 6522 device interface is faster, but the TTL method costs less.

Principles of Operation

The basic premise of the interface circuit shown in Figure 11-221 is that all timing control signals are generated under software control. Circuit timing is shown in Figure 11-222. This is followed by the control software listing.

A data conversion cycle is initiated by bringing $\overline{CS}$ low. This is accomplished by latching a low into the D-type flip-flop from address line A1 on the positive edge of system clock $\phi 2$. Address bit A14 is used as a gating signal to prevent the TLC545 device from being inadvertently selected during normal program execution. After $\overline{CS}$ is brought low, I/O clock pulses shift in the multiplexer address that is stored in the five most significant bits of a byte in RAM while shifting out the previous conversion results. The I/O clock is enabled by gating the positive going pulse of $\phi 2$ to the TLC545 device I/O CLK input. The gating occurs by addressing a location so A15 is high. The high on A15 also enables the output of the 3-state buffer onto the data bus. Address bit A0 determines whether the multiplexer address bit is a high or a low. This multiplexer address bit is shifted into the TLC545 device on the positive edge of clock $\phi 2$ and a data bit is placed onto the data bus at this time by the TLC545 device. The data bit is latched into the 6502 device on the negative edge of clock $\phi 2$.

Once the data is loaded into the accumulator, it is rotated into the carry bit and then into memory. $\overline{CS}$ is brought high again by writing a high into the D-type flip-flop. This is done by placing a high on address bit A1. This cycle can be completed every 176 μs.

This interface circuit uses an address decoding scheme that requires a minimum of decoding hardware. Small modifications to the address decoding scheme may be necessary to fit the interface to a particular application.

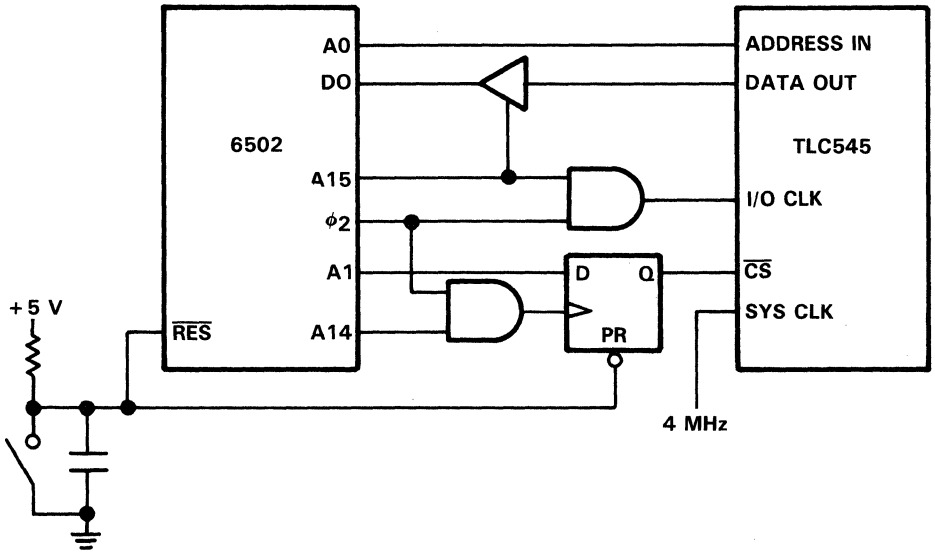


Figure 11-221. 6502 to TLC545 Interface Circuit Diagram

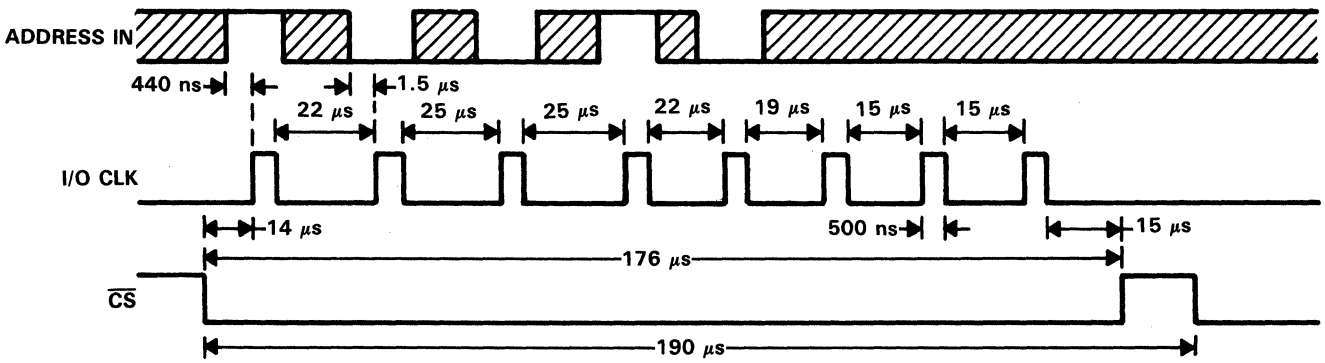


Figure 11-222. 6502 to TLC545 Interface Timing Diagram

```
CSLOW        .EQU 4000H
CSHIGH       .EQU 4002H
ADDLOW       .EQU 8000H
ADDHIGH      .EQU 8001H
MUXADDRESS   .EQU 0000H
RESULT       .EQU 0001H
;
;
;
             LDA   #$90          ; Initialize muxaddress
             STA   MUXADDRESS    ; To 10010=channel 18
             STA   CSLOW         ; Bring /CS low
             LDX   #$05          ; Set bit counter for 5 MSB'S

LOOP1:       ROL   MUXADDRESS    ; Rotate muxaddress bit into carry
             BCS   SET           ; Branch if bit is set
             LDA   ADDLOW        ; Write out A low on A0, clock data in
             JMP   CONTINUE      ; Skip next instruction
SET:         LDA   ADDHIGH       ; Write out A high on A0, clock data in

CONTINUE:    ROR   A             ; Rotate do into carry
             ROL   RESULT        ; Rotate carry into result
             DEX                 ; Decrement bit counter
             BNE   LOOP1         ; Go back for another bit

             LDX   #$03          ; Set counter for 3 LSB'S

LOOP2:       LDA   ADDLOW        ; Read in data bit
             ROR   A             ; Rotate into carry
             ROL   RESULT        ; Rotate carry into result
             DEX                 ; Decrement bit counter
             BNE   LOOP2         ; Get another bit

             STA   CSHIGH        ; Bring /CS
```

INTERFACE FOR THE TLC545 DEVICE TO THE ROCKWELL 6502 MICROPROCESSOR USING THE 6522 VIA

This application presents the design of an interface using the 6522 VIA. Another method using TTL gates is described in the previous application. Cost and performance are the basic trade-offs between the two designs. The 6522 device interface is faster, but the TTL method costs less.

Principles of Operation

The interface circuit diagram is shown in Figure 11-223. Timing for a data read cycle and an address write cycle is shown in Figures 11-224 and 11-225, respectively. Software listings for the initialization of the 6522 device and interface control follow the timing diagrams.

The interface makes use of the serial port available on port B pins CB1 and CB2. Since the serial port is not capable of full duplex communication, previous conversion results cannot be read in while a new multiplexer address is being shifted out. Thus, the interface can be used only for individual conversion cycles where the port is configured dynamically; that is, as an output port for the address write cycle, and as an input port during the data read cycle. This requires the inclusion of an SN74LS126 3-state buffer. The D-type flip-flops are used to effectively delay the I/O clock to ensure that the set up and hold times for shifting data in and out are met. Port B pins PB0 and PB1 are used to generate $\overline{CS}$ and the output enable signal for the 3-state buffer.

A data conversion cycle begins by bringing $\overline{CS}$ low. This is accomplished by writing a low to PB0. The analog

multiplexer address, which is stored in the five most significant bits of the X index register, is shifted out by writing to the SR register of the 6522 device. A delay loop is inserted to wait until the multiplexer address has been shifted out. The serial port is then configured as an input port to shift in the A/D conversion results. Conversion requires 36 system clock cycles, therefore, an appropriate delay loop dependent upon system clock frequency may be required. The output of the 3-state buffer is enabled by writing a high to PB1, and data is shifted into the SR register of the 6522 device. Again, a delay loop is included to wait until the data is shifted in. $\overline{CS}$ is then brought high, and the 3-state buffer is disabled to complete one data acquisition cycle. A data acquisition cycle can be completed in 55 μs.

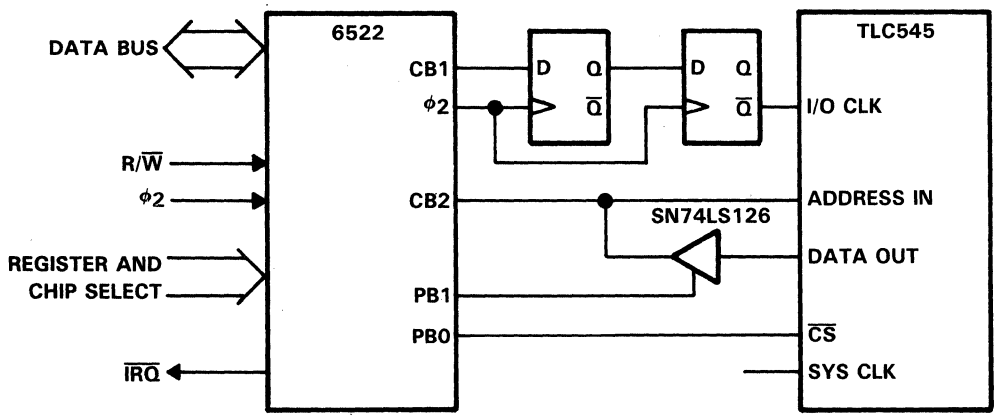


Figure 11-223. 6522 to TLC545 Interface Circuit Diagram

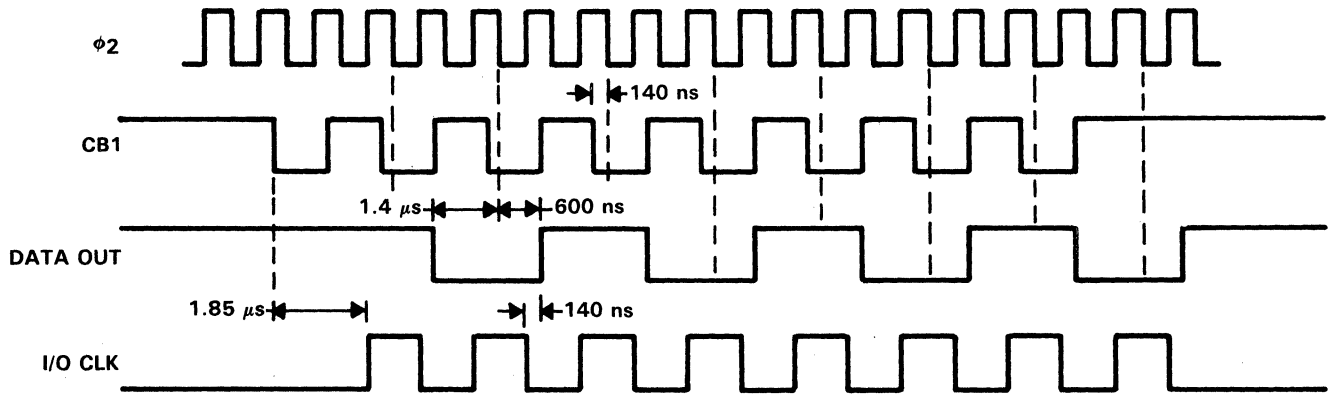


Figure 11-224. 6522 to TLC545 Data Read Cycle Timing Diagram

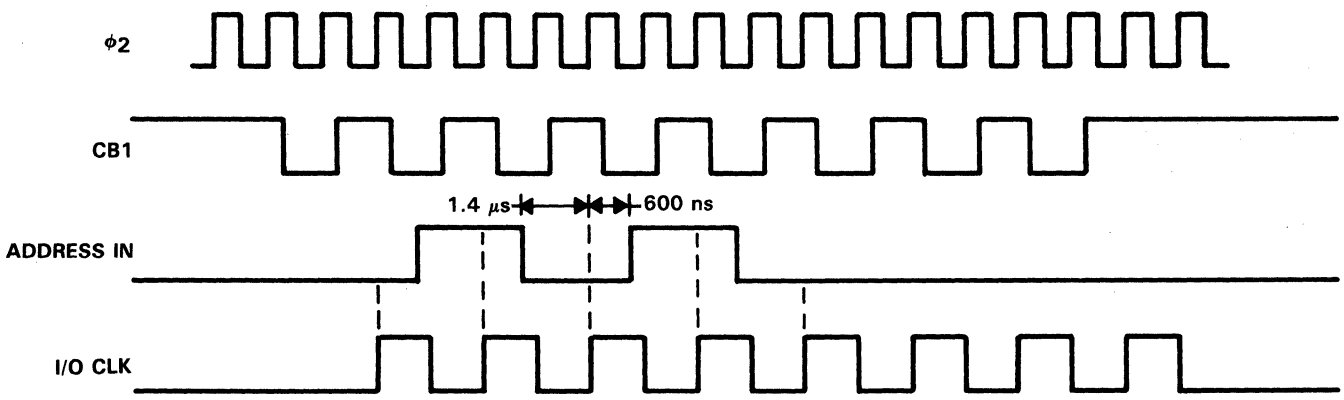


Figure 11-225. 6522 to TLC545 Address Write Cycle Timing Diagram

```
;                REGISTER ASSIGNMENTS
;
ORB              .EQU 0000H
DDRB             .EQU 0002H
SR               .EQU 000AH
ACR              .EQU 000BH
PCR              .EQU 000CH
IFR              .EQU 000DH
IER              .EQU 000EH
;
;

                 LDA  #$03          ;

                 STA  DDRB          ; Initialize port B I/O pins
                 LDA  #$01          ;
                 STA  ORB           ; Bring chip select high
                 LDX  #$50          ; Initialize muxaddress = 01010


                 LDA  #$18          ; Shift out under phi 2 control
                 STA  ACR           ;
                 LDA  #$00          ;
                 STA  ORB           ; Disable data out, bring /CS low
                 STX  SR            ; Shift out muxaddress to 545
                 LDY  #$02          ; Load delay loop counter
DELAY1           DEY                ; Decrement delay counter
                 BNE  DELAY1        ; Branch if not zero
                 NOP                ;
                 LDX  #$02          ;
                 LDA  #$08          ;
                 STA  ACR           ; Shift in under phi 2 control
                 STX  ORB           ; Enable output of 74LS126
                 LDA  SR            ; Dummy load to shift results in
                 LDY  #$03          ; Load delay loop counter
DELAY2           DEY                ; Decrement delay loop counter
                 BNE  DELAY2        ; Branch if not zero
                 LDA  #$01          ;
                 STA  ORB           ; Disable data out, bring /CS high
                 LDA  SR            ; Read conversion results into 6502
```

INTERFACE FOR THE TLC545 AND TLC546 DEVICES TO THE MOTOROLA 6805 MICROPROCESSOR

This application describes techniques for operating the TLC545 and TLC546 A/D converters with the 6805 microprocessor using software control. This can be accomplished by two methods:

1. Generating all necessary control signals under software control by toggling output port pins
2. Using the serial peripheral interface (SPI) to generate necessary control signals for data transfer.

The TLC545 and TLC546 devices are particularly well suited for interfacing to the SPI, however, not all 6805 microprocessors include the SPI on chip. Thus, the software controlled interface has the advantage although it is less efficient.

Both the TLC545 and TLC546 devices comprise a complete data acquisition system on a chip. The system includes such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, and microprocessor-compatible control logic. The four control inputs are $\overline{CS}$, I/O clock, system clock, and address input.

The I/O and system clock require no special speed or phase relationship, and are normally used independently. This allows the system clock to run up to 4 MHz for the TLC545 device and up to 2.1 MHz for the TLC546 device to ensure conversion times of less than 9 and 17 μs, respectively. The I/O clock runs up to 2.1 MHz and 1.1 MHz, respectively, to allow a maximum data transfer rate.

Principles of Operation

Circuit diagram for the software controlled 6805 microprocessor to TLC545 and TLC546 device interface is shown in Figure 11-226. Circuit timing is shown in Figure 11-227. The software controlled interface makes use of four pins on port A of the 6805 microprocessor. Three of these pins are used as outputs to generate the $\overline{CS}$, I/O clock, and multiplexer address input. The remaining pin is used as an input to receive the conversion results from the TLC545 and TLC546 devices. A software program segment illustrates a method that can be used to initialize the input/output pins.

A program listing which controls actual transfer of data follows the initialization method. This program block sends out the 5-bit analog multiplexer address that is shifted into the TLC545 and TLC546 devices on the first five I/O clock rising edges. Sampling of the addressed input begins at the falling edge of the fifth I/O clock and continues until the falling edge of the eighth I/O clock occurs. Conversion requires 36 clock cycles of the system clock, which can run up to 4 MHz to allow conversion in as little as 9 μs. Conversion results are shifted out of the TLC545 and TLC546 devices on the negative edge of the I/O clock and the program block leaves these results in the accumulator. With the 6805 device running at 5 MHz and the TLC545 device system clock at 4 MHz, one conversion cycle loads an analog multiplexer address and reads the results from the previous conversion. This can be completed in 248 μs.

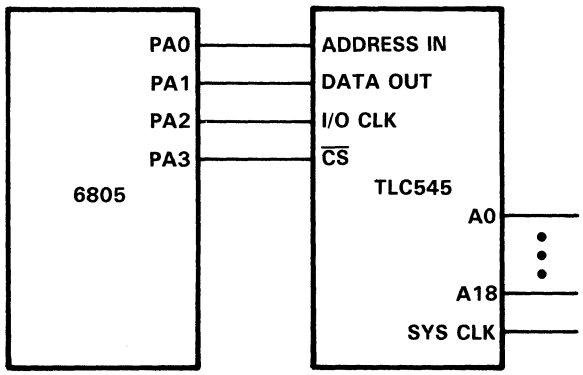


Figure 11-226. 6805 to TLC545 Interface Circuit Diagram

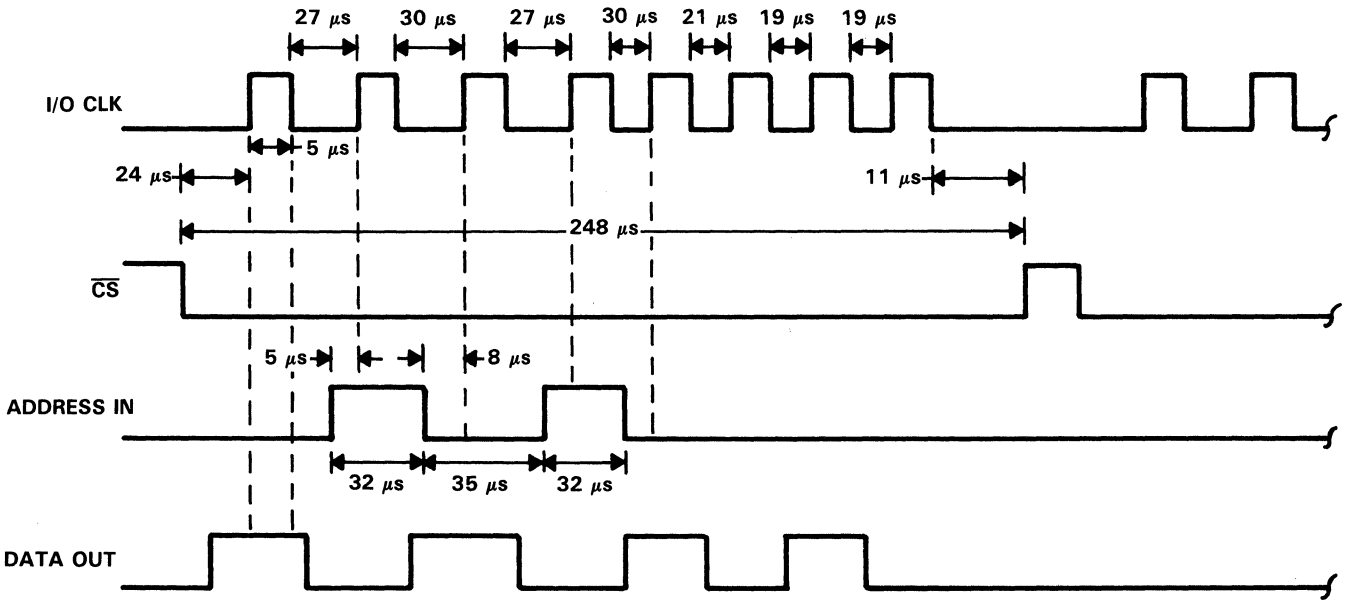


Figure 11-227. 6805 to TLC545 Interface Timing

```
PORTA       .EQU 0000H
DDRA        .EQU 0004H
            .ORG 0100H

START:      LDA   #0DH              ;
            STA   DDRA              ; Initialize port A I/O pins
            BSET  3,PORTA           ; Bring chip select high
            LDA   #50               ; Initialize multiplexer address


            LDX   #05               ; Load counter for first 5 bits
            BCLR  3,PORTA           ; Bring chip select low

LOOP1:      BRSET 1,PORTA,LABEL1    ; Read data bit into carry bit
LABEL1:     ROL   A                 ; Rotate muxadd bit and result bit
            BCS   SET               ; Go to set if muxadd bit is 1
            BCLR  0,PORTA           ; Write out A 0 to TLC545 address in
            JMP   CLOCK             ; Skip next instruction
SET:        BSET  0,PORTA           ; Write out A 1 to TLC545 address in
CLOCK:      BSET  2,PORTA           ; Bring I/O clock high
            BCLR  2,PORTA           ; Bring I/O clock low
            DECX                    ; Decrement counter
            BNE   LOOP1             ; Continue if counter is not zero
;
            LDX   #03               ; Load counter for last 3 data bits
;
LOOP2:      BRSET 1,PORTA,LABEL2    ; Read data bit into carry bit
LABEL2:     ROL   A                 ; Rotate new data bit into result
            BSET  2,PORTA           ; Bring I/O clock high
            BCLR  2,PORTA           ; Bring I/O clock low
            DECX                    ; Decrement counter
            BNE   LOOP2             ; Continue if counter is not zero
;
            BSET  3,PORTA           ; Bring chip select high
```

INTRODUCTION TO DATA ACQUISITION FOR DIGITAL SIGNAL PROCESSORS

Digital Signal Processing (DSP) involves the representation, transmission, and manipulation of signals using numerical techniques and digital processors. It has been a fast growing technology during the past few years, with the impact of programmability and VLSI broadening the range of problems that can be served with DSP. Its applications have been expanded to encompass not only traditional radar signal processing but also today's image processing, speech processing, and telecommunications.

Both the theoretical and practical aspects of DSP have made tremendous progress. While more DSP algorithms are being discovered, better tools are also being developed to implement these algorithms. One of the most important recent breakthroughs in electronic technology is the high-speed digital signal processor. These single-chip processors are now commercially available in very large-scale integration (VLSI) circuits from semiconductor suppliers. Digital signal processors are essentially high-speed microprocessors/ microcomputers, designed specifically to perform the computation-intensive algorithms. By taking advantage of the advanced architecture, parallel processing, and dedicated DSP instruction sets, these devices can execute millions of DSP operations per second.

With the advantages offered by VLSI, innovative engineers are discovering more and more applications where digital signal processors efficiently provide better solutions than their analog counterparts for reasons of reliability, flexibility, repeatibility, compactness, and long-term stability. Digital signal processors do, however, require accurate analog-to-digital (A/D) and digital-to-analog (D/A) converters. These converters interface the inputs and outputs of the DSP to the analog world.

Texas Instruments has developed a state-of-the-art analog interface IC, the TLC32040, to interface Texas Instruments TMS320 family of digital signal processors to the analog world. In addition to the A/D and D/A converters, the TLC32040 also contains filters for reducing noise and aliasing, which is an undesired sampled-data phenomenon. The TLC32040 also contains a serial port, which allows direct interface to most TMS320 digital signal processors. More information on the TLC32040 is presented in the following pages.

INTERFACING THE TLC32040 TO THE TMS320 FAMILY OF DIGITAL SIGNAL PROCESSORS

Description

The TLC32040 is a complete analog-to-digital and digital-to-analog input/output system on a single monolithic CMOS chip. This device integrates a band-pass, switched-capacitor, antialiasing input filter, a 14-bit resolution A/D converter, four microprocessor-compatible serial port modes, a 14-bit resolution D/A converter, and a low-pass, switched-capacitor, output-reconstruction filter. The device offers numerous combinations of Master Clock input frequencies and conversion/sampling rates, which can be changed via digital processor control.

Typical applications for this IC include modems (7.2-, 8-, 9.6-, 14.4-, and 19.2-kHz sampling rates), analog interface for digital signal processors, speech recognition/storage systems, industrial process control, biomedical instrumentation, acoustical signal processing, spectral analysis, data acquisition, and instrumentation recorders. Four serial modes, which allow direct interface to the TMS32011, TMS32020, and TMS320C25 digital signal processors, are provided. Also, when the transmit and receive sections of the Analog Interface Circuit (AIC) are operating synchronously, it will interface to two SN54299 or SN74299 serial-to-parallel shift registers. These shift registers can then interface in parallel to the TMS32010, other digital signal processors, or to external FIFO circuitry. Output data pulses are emitted to inform the processor that data transmission is complete, or to allow the DSP to differentiate between two transmitted bytes. A flexible control scheme is provided so that the functions of the IC can be selected and adjusted coincidentally with signal processing via software control.

The antialiasing input filter comprises seventh-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively, and a fourth order equalizer. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When no filtering is desired, the entire composite filter can be switched out of the signal path. A selectable, auxiliary, differential analog input is provided for applications where more than one analog input is required.

The A/D and D/A converters each have 14 bits of resolution with 10 bits of integral linearity guaranteed over any 10-bit range. Currently the AIC is being evaluated from the perspective of offering several different versions of the AIC. These AICs would be screened at the factory for enhanced performance in areas such as total harmonic distortion or A/D and D/A accuracy. One of these devices may provide integral linearity greater than 10 bits.

The A/D and D/A architectures guarantee no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage is brought out to a pin and is available to the designer. Separate analog and digital voltage supplies and grounds are provided to minimize noise and ensure a wide dynamic range. Also, the analog circuit path contains only differential circuitry to keep noise to an absolute minimum. The only exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The output-reconstruction filter is a seventh-order CC-type (Chebyshev/elliptic transitional low-pass filter with a fourth-order equalizer) and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the digitally encoded signal.

Principles of Operation

As shown in Figures 11-228 and 11-229, the AIC is easily interfaced to the TMS32020, TMS320C25, TMS320C17 and TMS32011 serial ports. The TMS32020/C25 can communicate with the AIC either synchronously or asynchronously depending on the information in the control register. If d5 in the AIC control register is a 0, the transmit and receive sections of the AIC will operate asynchronously; if d5 is a 1, these sections will operate synchronously. The operating sequence for synchronous communication with the TMS32020 and TMS320C25 is shown in Figure 11-230. For asynchronous communication, the operating sequence is similar but $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$, in general, do not occur at the same time (see Figure 11-231). For proper operation, the TXM bit in the TMS32020/C25 control register should be set to 0 so that the $\overline{\text{FSX}}$ pin of the TMS32020/C25 is configured as an input, the format status bit (FO) of the TMS32020/C25 should be set to 0, and the AIC WORD/$\overline{\text{BYTE}}$ pin should be at a logic high. After each receive and transmit operation, the TMS32020/C25 asserts an internal receive (RINT) and transmit (XINT) interrupt which may be used to control program execution.

The interface to the TMS32011 and TMS320C17 also requires no external circuitry and, like the TMS32020 interface, can operate either synchronously or asynchronously. The operating sequence for synchronous communication is shown in Figure 11-232. In this case, the AIC must transmit data in two 8-bit bytes and therefore the WORD/$\overline{\text{BYTE}}$ pin must be held low. As with the TMS32020/C25, the TMS32011/C17 control register should be configured to respond to external framing pulses ($\overline{\text{FSX}}$ and $\overline{\text{FSR}}$) and an external Shift Clock. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ interrupts may be used to control program execution.

Since the TMS32010 and the TMS320C15 have no serial port, a direct connection to the AIC is not possible. However, as shown in Figure 11-233, the AIC can interface to two 74LS299 Serial-to-Parallel shift registers which can then be connected to the data bus of the TMS32010 or the TMS320C15. The AIC must be operated synchronously and in 16-bit (word) mode. The operating sequence is shown in Figure 11-234. In this configuration, the device labeled A1 represents a data-delay. The data-delay may be realized with three cascaded AND gates connected between "I" and "O" ("C" is not connected), or a single D-type flip-flop with the

D-input connected to "I", the Q-output connected to "O" and the noninverting clock input connected to "C". All of the logic circuitry excluding the two 74LS299s and the 74LS138 3-to-8-line decoder may be replaced with a single PAL. Data is written to the AIC with an OUT instruction, specifying port address 1; a read is accomplished with an IN instruction specifying port address 0.

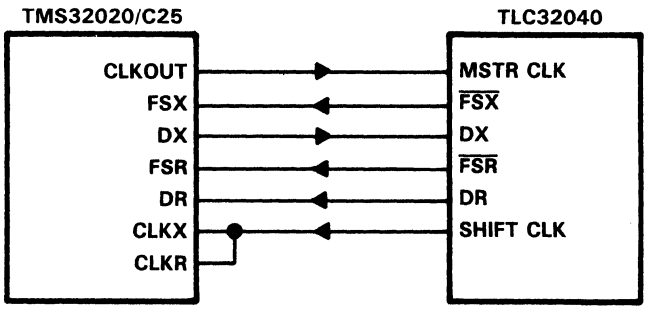


Figure 11-228. AIC Interface to TMS32020/C25

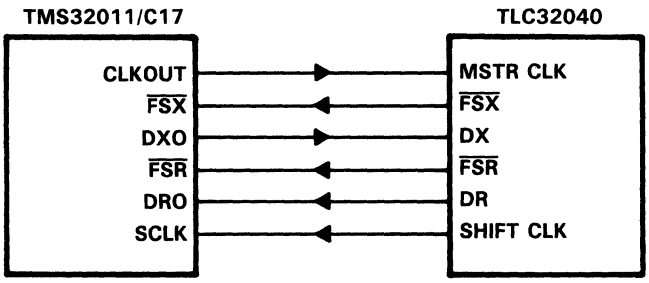
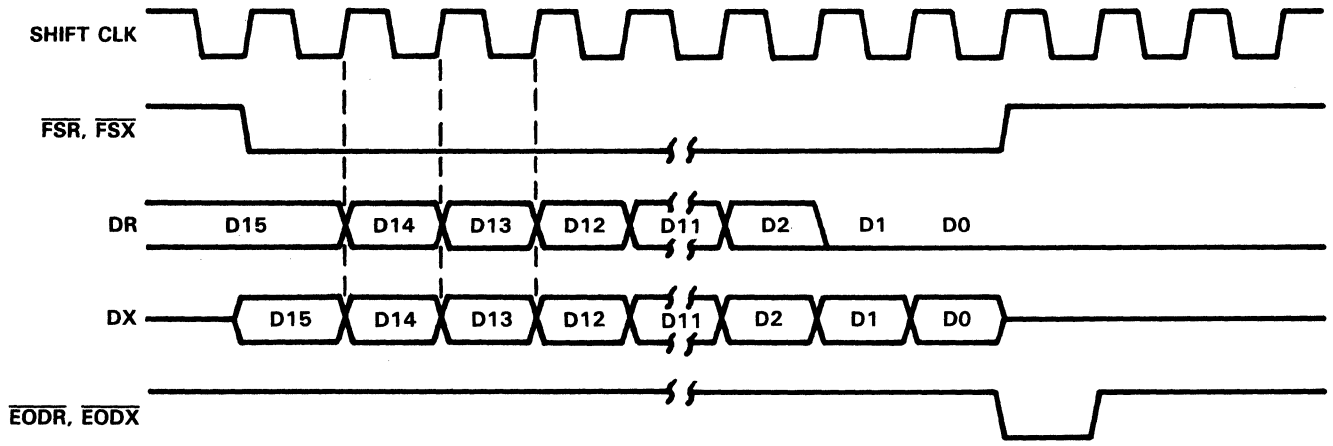


Figure 11-229. AIC Interface to TMS32011/C17



The sequence of operation is:

1. The FSX or FSR pin is brought low.
2. One 16-bit word is transmitted or one 16-bit byte is received.
3. The FSX or FSR pin is brought high.
4. The EODX or EODR pin emits a low-going pulse as shown.

Figure 11-230. Operating Sequence for AIC-TMS32020/C25 Interface—Synchronous

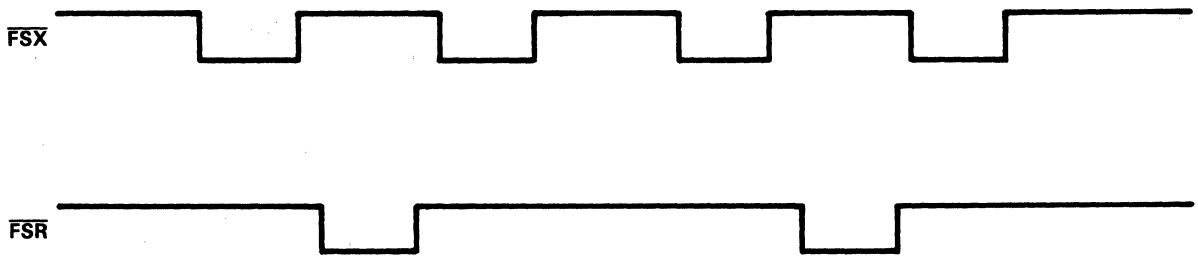
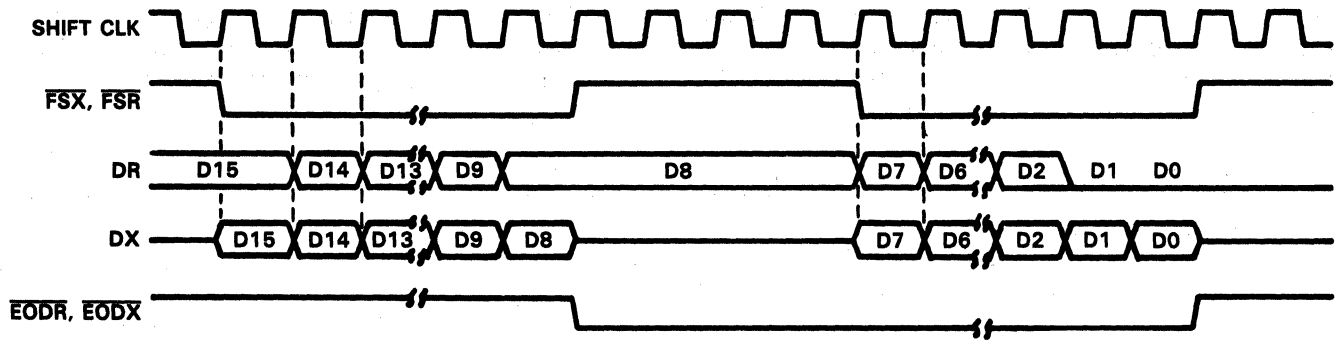


Figure 11-231. Asynchronous Communication: AIC-TMS32020/C25 Interface



The sequence of operation is:

1. The $\overline{FSX}$ or $\overline{FSR}$ pin is brought low.
2. One 8-bit is transmitted and one 8-bit byte is received.
3. The $\overline{EODX}$ and $\overline{EODR}$ pins are brought low.
4. The $\overline{FSX}$ and $\overline{FSR}$ emit a positive frame-sync pulse that is four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The $\overline{EODX}$ and $\overline{EODR}$ pins are brought high.
7. The $\overline{FSX}$ and $\overline{FSR}$ pins are brought high.

Figure 11-232. Operating Sequence for AIC-TMS32011/C17 Interface—Synchronous

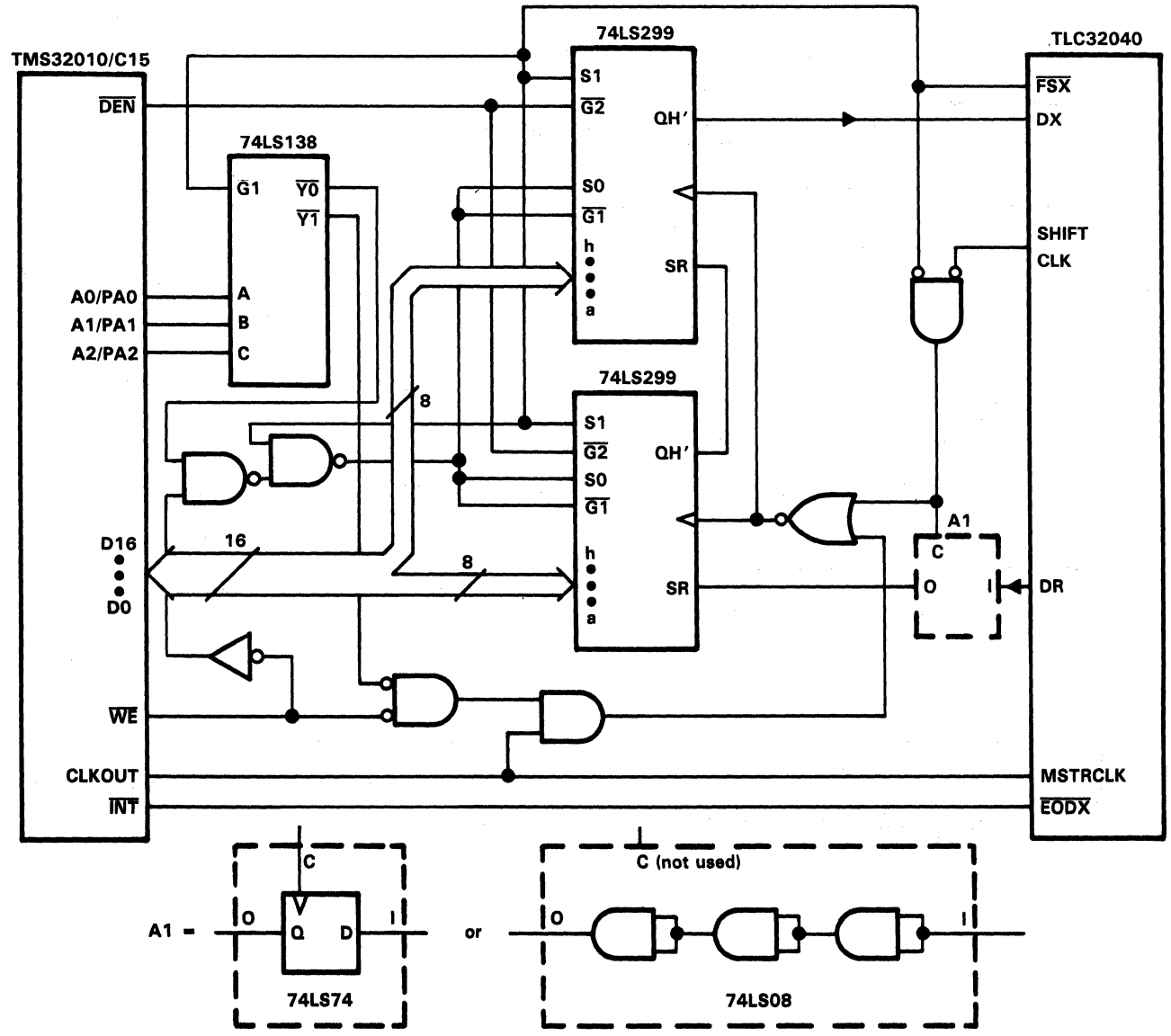


Figure 11-233. AIC Interface to TMS32010/C15

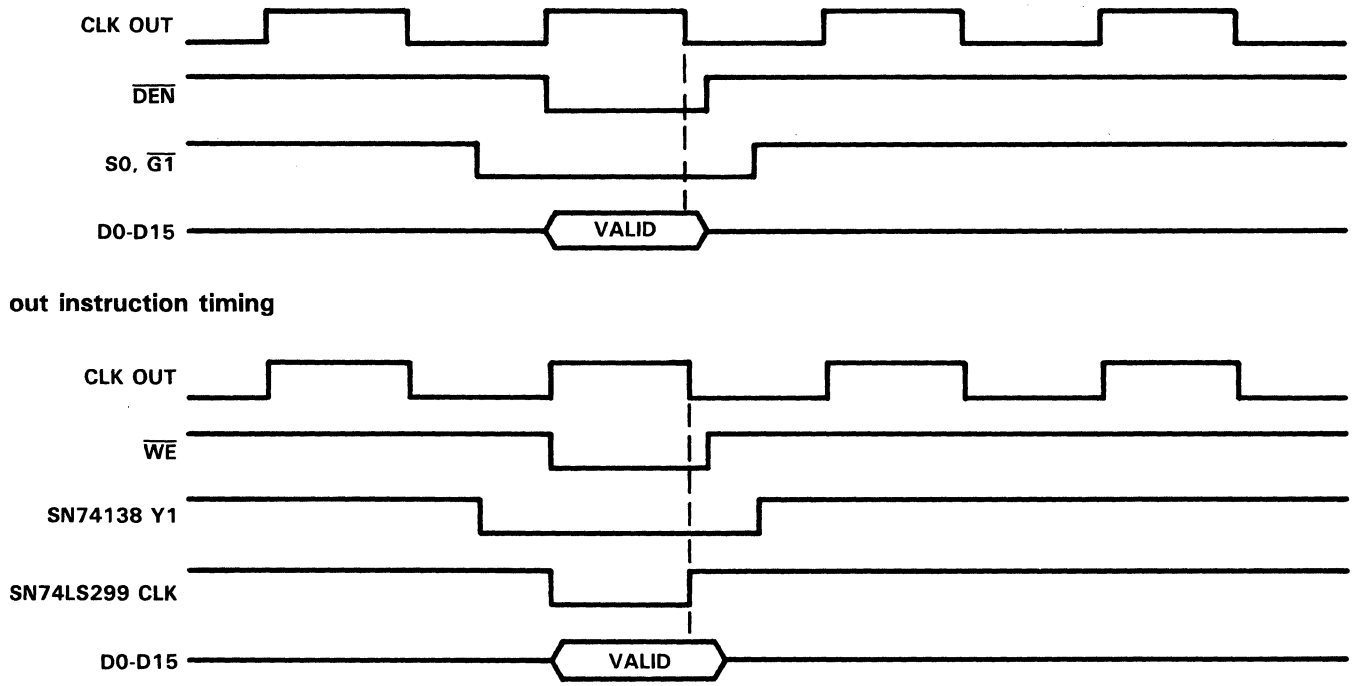


Figure 11-234. TMS32010/C15-TLC32040 Interface Timing

INTERFACING THE TLC7524 TO THE TMS32010

Hardware

Due to the high-speed operation of the internal logic circuitry of the TLC7524 8-bit digital-to-analog converter, the interface to the TMS32010 Digital Signal Processor requires a minimum of external circuitry. As shown in Figure 11-235, the interface circuitry consists of logic to decode the address of the peripheral. Here we have used one SN74ALS679 12-bit Address Comparator.

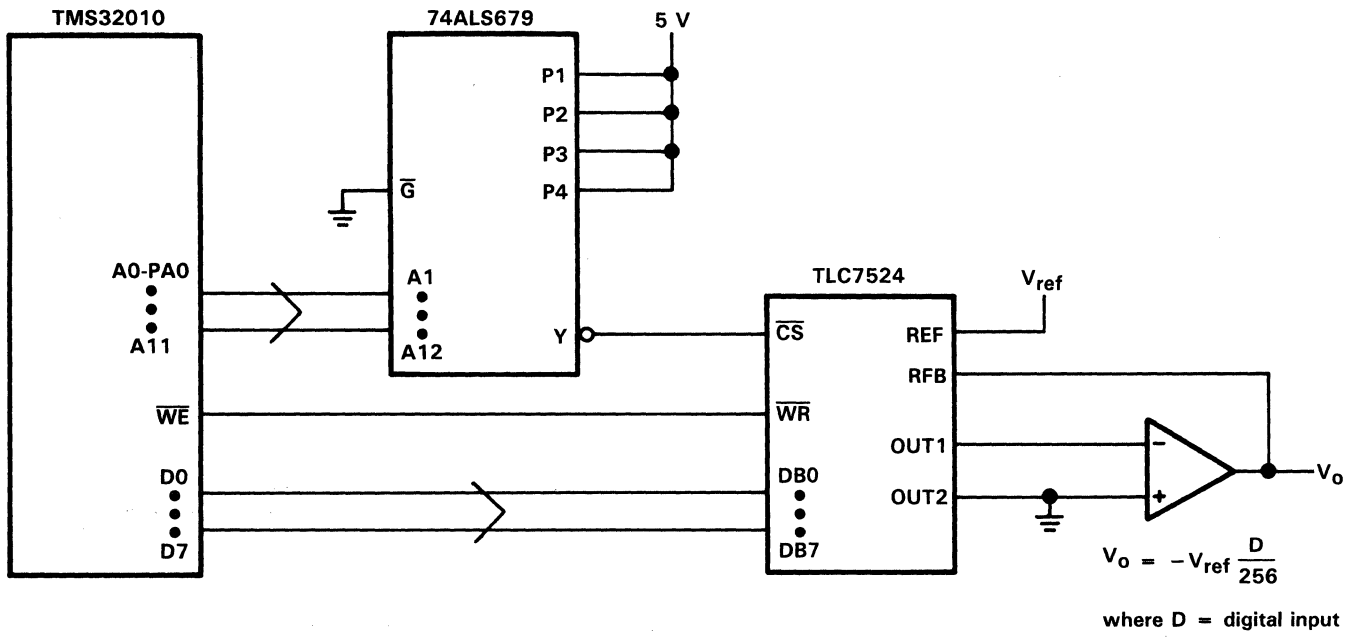


Figure 11-235. TLC7524 to TMS32010 Interface

Principles of Operation

As shown in Figure 11-236, when the TMS32010 executes an OUT instruction, the $\overline{MEN}$ output remains high and the address of the peripheral specified by the instruction is placed on the address bus. The three-bit port address will appear on pins A0 through A2, and pins A3 through A11 will be driven low.

The P-inputs of the SN74ALS679 Address Comparator should be hard wired with the preprogrammed address of the I/O port which corresponds to the TLC7524. For example, if the TLC7524 is at I/O port 0, all of the P-inputs of the 74ALS679 should be tied to logic high. If however the TLC7524 is at I/O port address 1, input P2 of the 74ALS679 should be tied to logic low and P1, P3 and P4 should be tied to logic high (detailed information on the 74ALS679 may be found in the ALS/AS Logic Data Book).

When the address appearing at the address bus of the TMS32010 corresponds to the address programmed into the 74ALS679, the output of the 74ALS679 will be driven low, enabling the TLC7524 (see Figure 11-236, the timing diagram). The data to be written to the TLC7524 should then be on the data bus of the TMS32010 so that when $\overline{WE}$ goes low, the data can be latched into the TLC7524. The controlling software follows.

```
*
* Software for TLC7524 to TMS32010 Interface
*
*
*
*
DAT     EQU     0       DAT is defined to be data-memory address zero.
*
        AORG    0
        LDPK    0       Set Data-Memory Page Pointer to 0.
*
START   OUT     DAT,0   Place the contents of data-memory address 0 in
*                       the data latch of the DAC. The TLC7524 is at port address 0.
*       B       START
        END
```

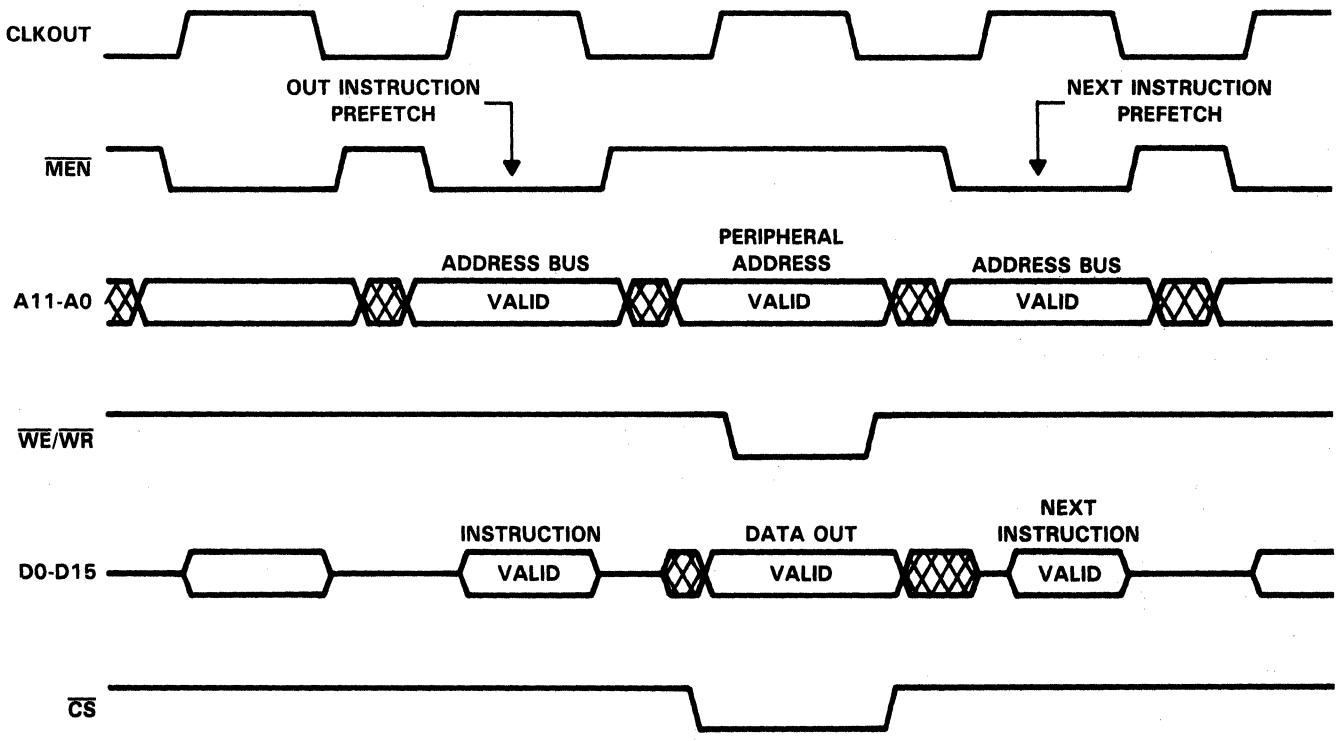


Figure 11-236. OUT Instruction Timing for TMS32010

INTERFACING THE TLC0820 TO THE TMS32010

Hardware

Because the control circuitry of the TLC0820 8-bit A/D converter operates much more slowly than the TMS32010, it cannot be directly interfaced. The following describes in detail the circuit shown in Figure 11-237. All of the logic functions are implemented with 74ALS and 74LS Low-power Schottky Logic. The devices used are:

1	SN74ALS679	12-bit Address Comparator
1	SN74LS74	Dual Positive-edge Triggered D-type Flip-flops
1	SN74ALS465	Octal Buffer with 3-state Output
1	SN74LS32	Quad 2-Input OR-Gate

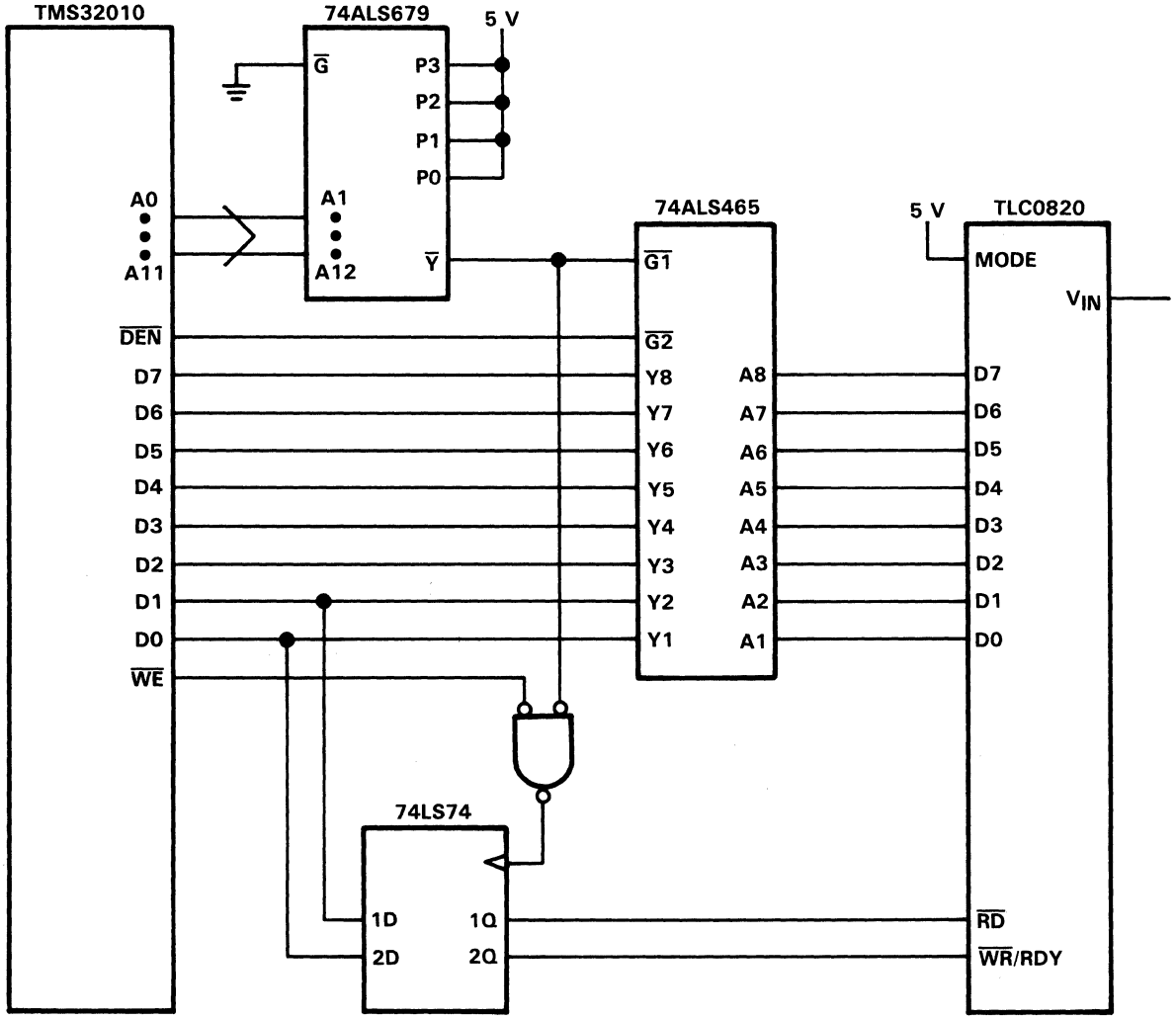


Figure 11-237. TLC0820 to TMS32010 Interface

Principles of Operation

The TMS32010 Digital Signal Processor operates the TLC0820 by writing to the D flip-flops the necessary states of the $\overline{WR}$ and $\overline{RD}$ pins. The $\overline{WR}$ and $\overline{RD}$ signals must initially be at a logic high level, corresponding to a high level at the output of both flip-flops. To begin conversion, $\overline{WR}$ must be lowered for a minimum of 600 nanoseconds and then raised. The conversion begins on the rising edge of the $\overline{WR}$ pulse, and approximately 600 nanoseconds later, the conversion is complete. Since the OUT instruction requires two CLKOUT cycles (each of which lasts 200 ns when the TMS32010 is running at 20 MHz), the write pulse may be implemented with the following code (also shown in the software listing).

```
OUT     <dma1>,<PA>
NOP                     or any 1-cycle instruction
OUT     <dma2>,<PA>     2-cycle instruction
```

where <dma1> is a data-memory address of a 16-bit word in which the bit assigned to $\overline{WR}$ is a logic-0 and the bit assigned to $\overline{RD}$ is a logic-1.

<PA> is the port address assigned to the TLC0820 and programmed into the 12-bit address comparator. The port address appears on pins A2 through A0 of the address bus during an OUT or an IN operation, pins A3 through A11 are driven low.

<dma2> is a data-memory address of a 16-bit word in which the bits assigned to both $\overline{WR}$ and $\overline{RD}$ are logic 1s.

After conversion has begun, the TLC0820 must have time to complete the A/D conversion before the result can be read by the DSP. There are two possible ways in which the TMS32010 may operate the TLC0820 (See Figures 2 and 3 of TLC0820 datasheet). In the first method, the $\overline{RD}$ pin is lowered at the end of conversion (600 ns after the rising edge of $\overline{WR}$), before the TLC0820 signals that the conversion result is ready. The $\overline{RD}$ pin may be lowered in the following manner:

```
NOP                     any 1-cycle instruction for 200 ns delay
OUT     <dma3>,<PA>     2-cycle instruction
```

where <dma3> is the data-memory address of a 16-bit word in which the bit assigned to $\overline{RD}$ is a logic 0 and the bit assigned to $\overline{WR}$ is a logic 1.

<PA> is the port address assigned to the TLC0820 and programmed into the 12-bit address comparator. The port address appears on pins A2 through A0 of the address bus during an OUT or an IN operation, pins A3 through A11 are driven low.

No more than 300 ns after the $\overline{RD}$ pin is lowered, the conversion result will appear on the data bus of the TLC0820, where it can then be read by the TMS32010. Since the IN instruction requires 400 ns to execute, no additional delay is necessary. The data may be read and the $\overline{RD}$ pin subsequently raised in the following manner:

```
IN      <dma4>,<PA>     2 cycles
OUT     <dma2>,<PA>     2 cycles
```

where <dma4> is the data-memory address where the conversion result will be stored.

<PA> is the port address of the TLC0820.

<dma2> is the data-memory address of a 16-bit word in which both the bits assigned to $\overline{RD}$ and $\overline{WR}$ are logic 1s.

After the conversion result has been read it will be necessary to mask the data to obtain the 8-bits of interest. The interface timing is shown in Figure 11-238.

INTERFACING THE TLC7524 TO THE TMS32020

Hardware

Due to the high-speed operation of the internal logic circuitry of the TLC7524 8-bit digital-to-analog converter, the interface to the TMS32020 Digital Signal Processor requires a minimum of external circuitry.

As shown in Figure 11-239, the interface circuitry consists of logic to decode the address of the peripheral. Here we have used one SN74ALS138 3-to-8-Line Decoder.

Principles of Operation

As shown in Figure 11-240, when the TMS32020 executes an OUT instruction, the peripheral address is placed on the address bus and the $\overline{IS}$ line goes low, indicating that

```
*
*
* Software for TLC0820 Interface to TMS32010
*
*
        AORG   0
        LDPK   0        Set Data-Memory Page-Pointer to 0.
*
* Data memory locations 1, 2, and 3 should be initialized as follows:
*
*    ADDRESS   DATA
*       1      0001H
*       2      0002H
*       3      0003H
*
* This is necessary because the LSB of the data will be written to the /WR line of the TLC0820
* and the next-to-LSB will be written to the /RD line of the TLC0820.
*
* The following program segment manipulates the /WR and /RD control inputs of the TLC0820.
*
*
START   OUT    3,0      Raise /WR and /RD.
        NOP
        OUT    2,0      Lower /WR.
        NOP
        OUT    3,0      Raise /WR.
        NOP
        OUT    1,0      Lower /RD.
        IN     0,0      Read conversion result and store in data-memory location 0.
        OUT    3,0      Raise /RD.
        B      START
        END
```

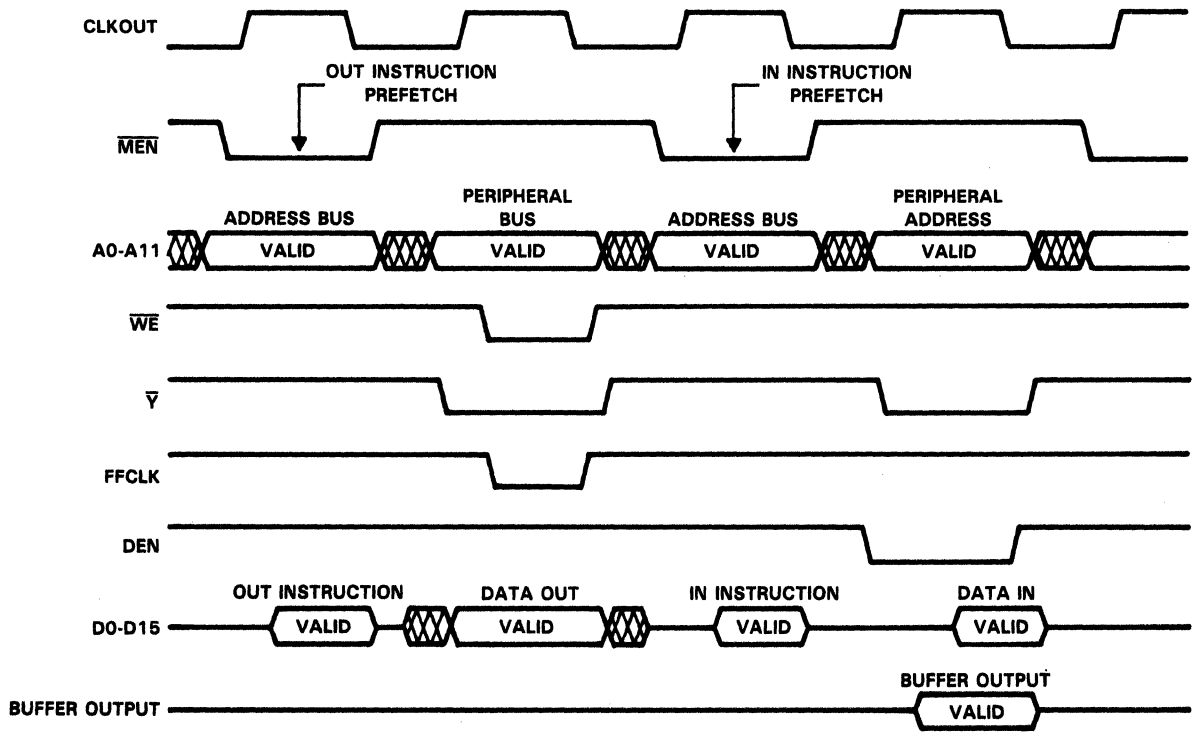


Figure 11-238. TLC0820 to TMS32010 Interface Timing

the address on the bus corresponds to an I/O port and not external program or data memory. A low level at $\overline{IS}$ will enable the 74ALS138 decoder, and the Y-output, corresponding to the address on the bus, is brought low.

When the Y-output is brought low, the TLC7524 is enabled and the data appearing on the databus will be latched into the D/A converter by $\overline{STRB}$. The controlling software is shown in the following listing.

```
*
*
* Software for TLC7524 to TMS32020 Interface
*
*
          AORG   >0
          LDPK   >0        Set data memory page pointer to 0.
*
* The following program segment transfers the data in the lower 16 bits of the accumulator to the
* data latches of the TLC7524 digital-to-analog converter.

*
START     SACL   >60       Save low accumulator in >60.
          OUT    >60,0     Move contents of >60 to TLC7524.
          B      START
          END
```

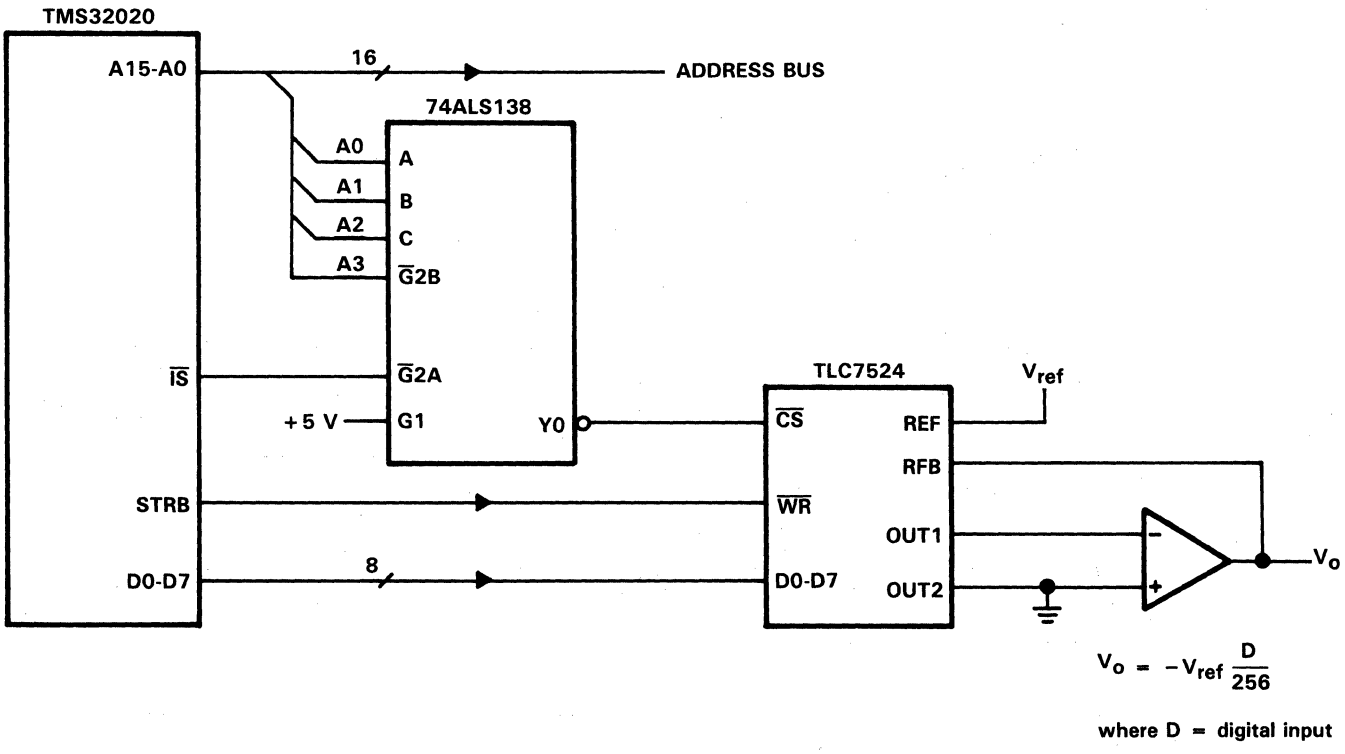


Figure 11-239. TLC7524 to TMS32020 Interface

INTERFACING THE TLC0820 TO THE TMS32020

Hardware

Because the control circuitry of the TLC0820 8-bit A/D converter operates much more slowly than the TMS32020, it cannot be directly interfaced. The following describes in detail the interface circuit shown in Figure 11-241. As drawn, the interface circuitry employs the following logic devices.

1	SN74LS138	3-Line to 8-Line Decoder
1	SN74LS00	Quad 2-Input NAND Gate
1	SN74LS04	Hex Inverters
1	SN74LS32	Quad 2-Input OR Gate
1	SN74LS175	Quad D-type Flip-flop

Principles of Operation

The 74LS138 decodes the addresses assigned to the TLC0820. One of the addresses is used when performing a write operation; the other, for a read. The two different addresses are necessary to ensure that the correct number of wait states is provided for the write and read operations.

The controlling software is shown in the following listing. To begin conversion, the TMS32020 must supply the TLC0820 with a write pulse ($\overline{WR}$) of at least 600 ns. With the TMS32020 running at 20 MHz and the TLC0820 configured as slow memory, three wait states are necessary to provide a write pulse of sufficient length.

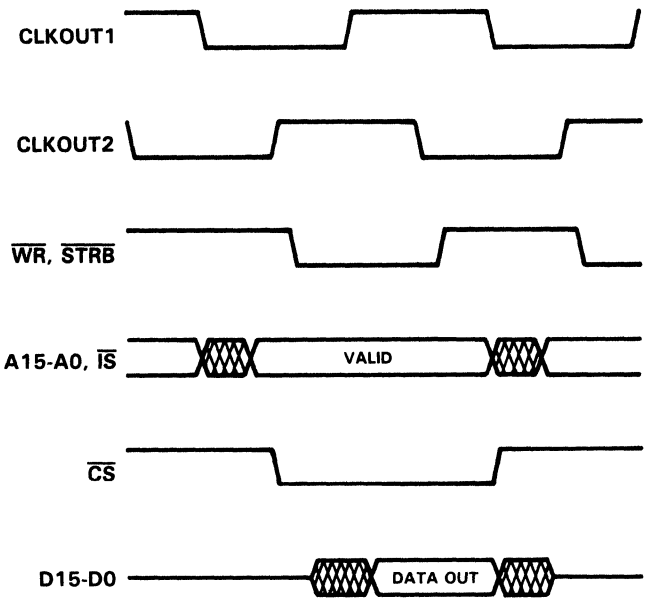


Figure 11-240. TMS32020 OUT Instruction Cycle

```
OUT     *,0     output the data word specified by the current auxiliary register
                to peripheral on port address 0. A low at Y0 of the
                74ALS138 will allow 3 wait states.
```

After conversion has begun (with the rising edge of the $\overline{WR}$ signal), the TMS32020 must wait at least 600 ns before the conversion result can be read. Sufficient delay should be provided in software.

To read the conversion result, sufficient wait states should be provided to allow for the data access time (320 ns minimum) of the TLC0820. As shown in the timing diagram of Figure 11-242, two wait states are provided when accessing port 1.

```
IN      <dma>,1     read a data word from peripheral on port address 1. Store in
                    data memory location <dma>. A low at Y1 of the
                    74ALS138 will provide 2 wait states.
```

```
*
*
* Software for the TLC0820 to TMS32020 Interface
*
*
          AORG    >0
          LDPK    >0        Set Data-Memory Page Pointer to >0.
*
* The following statement writes the data contained in the data-memory location specified by the
* current address-register pointer to the TLC0820. The data is not important* the write pulse is.
* The interface provides for 3 wait states.
*
START     OUT     *,0
*
* The following instructions provide a 600 ns delay between the rising edge of the write pulse to
* the falling edge of the subsequent read.
*
          NOP
          NOP
*
* The following IN instruction reads the conversion result and stores the result in data-memory
* location >60. The interface provides for 2 wait states.
*
          IN      >60,1
          B       START
          END
```

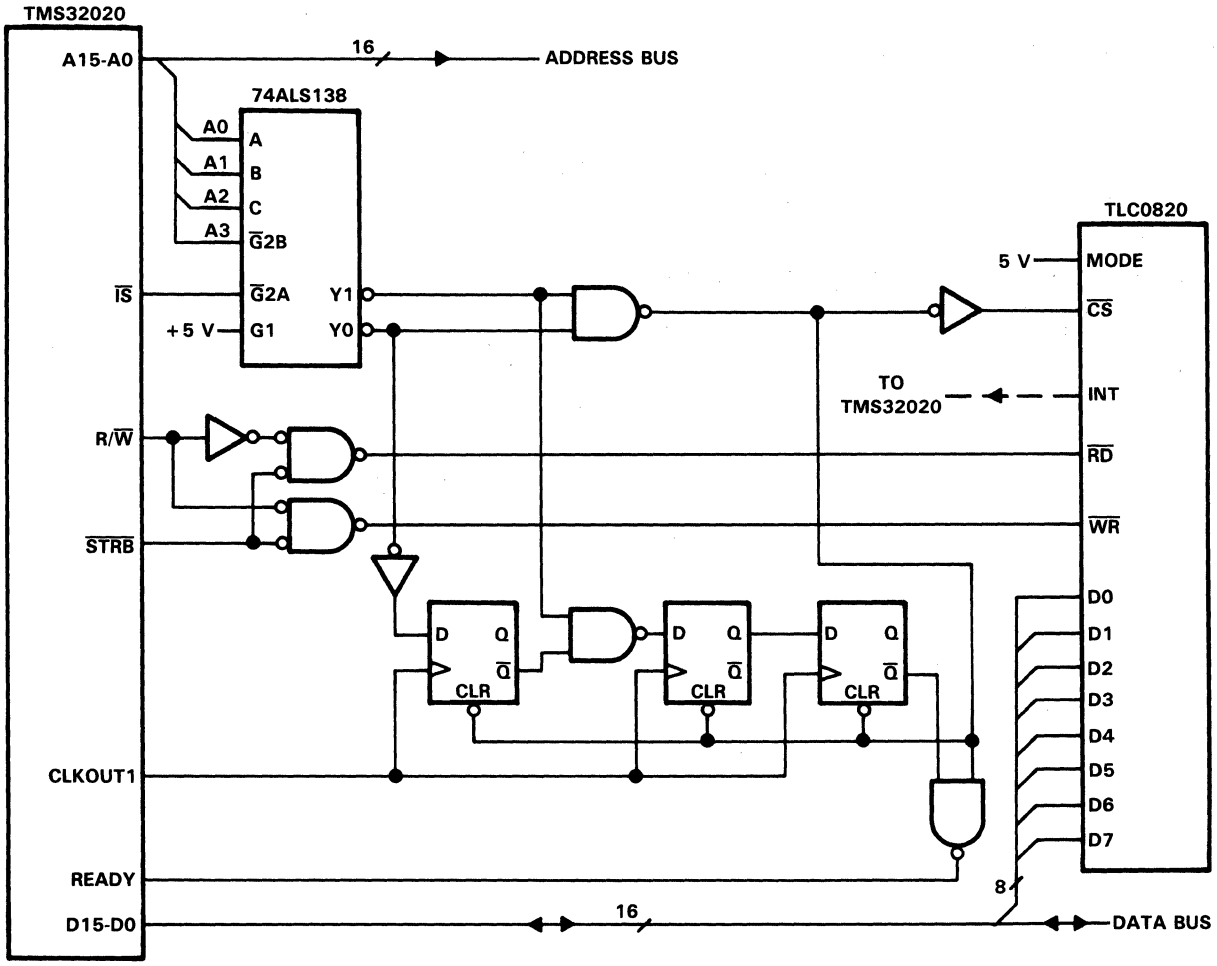


Figure 11-241. TLC0820 to TMS32020 Interface

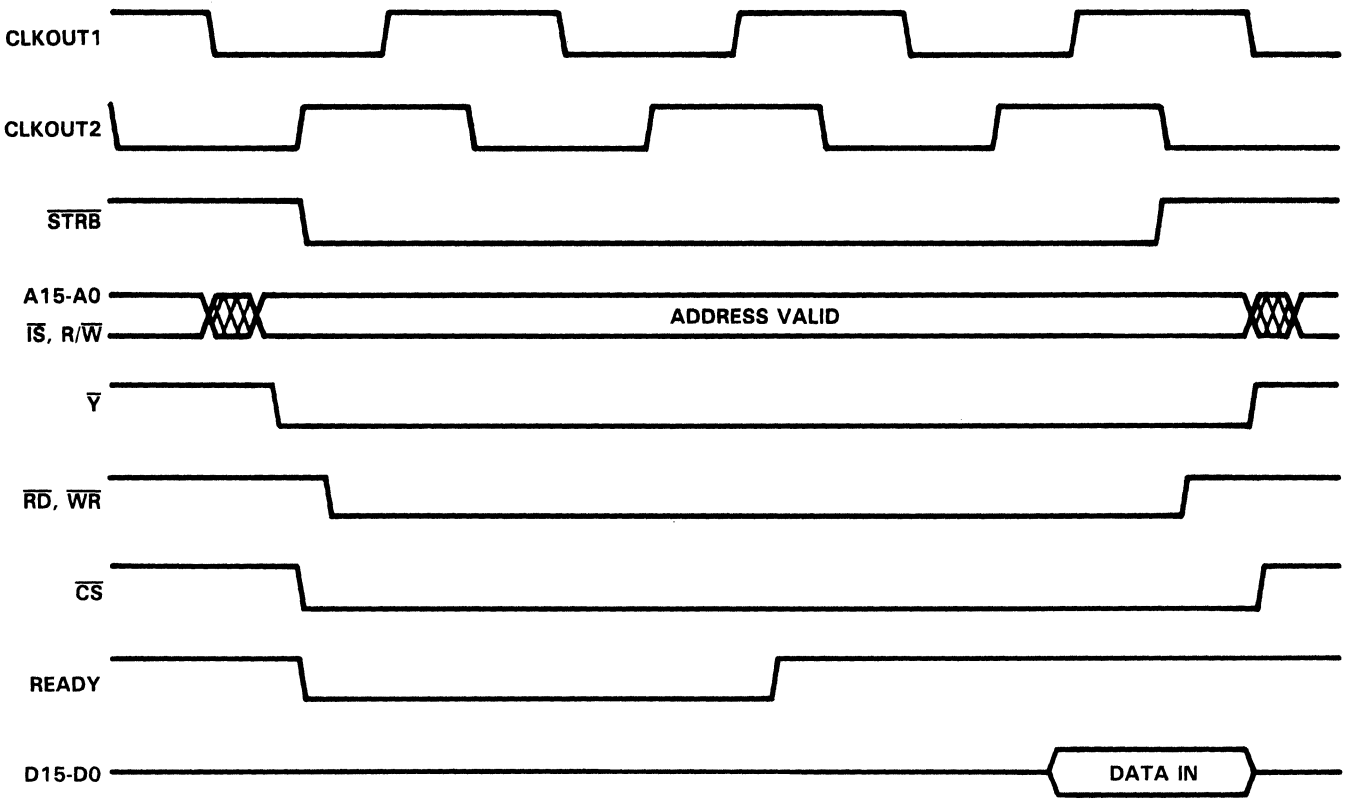


Figure 11-242. TLC0820 IN Instruction Timing — Two Wait States

INTERFACING THE TLC1540, TLC1541, TLC540 AND TLC541 TO THE TMS32020 AND TMS320C25

The TMS32020/C25 can be easily interfaced to the TLC154X and TLC54X family of data acquisition devices via the serial port. The TLC1540/1 and TLC540/1 are multiple-analog-input devices that are useful in cases where more than one analog signal needs to be monitored. The TLC540/1 contains an 8-bit ADC with 11 external analog inputs. If more precision is required, the TLC1540/1 contains a 10-bit ADC with 11 external analog inputs. These devices contain separate input and output serial ports. The input port is used for selecting which analog input is to be monitored. The host processor simply sends the address of the desired analog input. The output port is used for transmitting the digital representation of the processor.

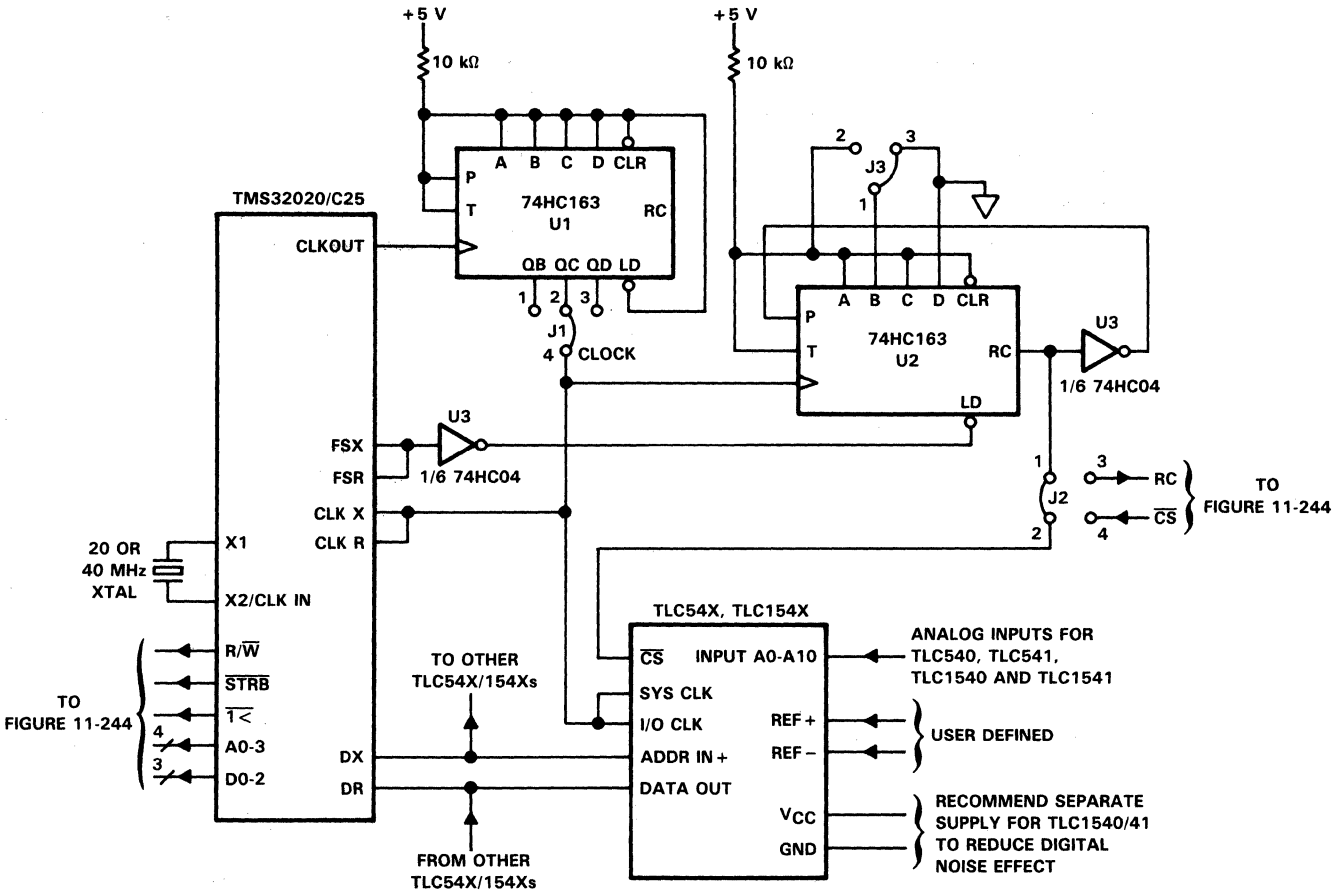
Hardware

As shown in Figure 11-243, glue logic is required to generate the clock for the serial interface and the chip select for the TLC54X/154X. A total of three packages is required: two 74HC163 synchronous counters and two inverters from a 74HC04. Timing is not critical, therefore other technologies such as S, LS, AS, ALS, F, and ACl can be used. In this application, the glue logic can be replaced by one PAL.. A '16R8 would be appropriate.

Please refer to Figure 11-243 for the following explanation. U1 divides the CLKOUT signal from the TMS32020/C25 to provide the clock for the serial interface. The TMS32020/C25 internally divides the input crystal clock by four. In the case of a TMS320C25 using a 40 MHz crystal, U1 divides by eight and by sixteen to provide a 1.25 MHz and 625 kHz clock, respectively. The 1.25 MHz clock can be used for the TLC540, and the 625 kHz clock can be used for the TLC541 and TLC1540/1. The TMS32020/C25 generates a framing signal on pin FSX that is used to trigger a chip-select from U2. When triggered, U2 provides a chip-select 8 and 10 clocks wide for the TLC540/1 and TLC1540/1, respectively. The ripple carry signal from U2 is used as the chip-select signal. Triggering occurs when the load input is driven low. This occurs when the FSX signal from the TMS32020/C25 goes high. On the next rising clock edge, U2 is loaded with the values on its preset inputs. When U2 is loaded, ripple carry goes low until a count of 15 is reached. Then, ripple carry goes high, disabling the count. The count disable is accomplished by connecting the inverted ripple carry to ENABLE P input. The preset input values are 7 and 5 to generate a chip-select 8 and 10 clocks wide, respectively.

If several devices need to be networked together, multiple TLC54X and TLC154Xs can be connected together on the same serial bus. This is possible because the serial output ports are in a high-impedance state when not selected.

Additional glue logic is required for this application. A latched decoder such as a 74HCT137 (U4) as shown in Figure 11-244 is a possible solution. The appropriate device is selected by writing a device value to U4. The device value is the address of the output pin on U4 that routes the chip-select to the desired device. U4 is I/O mapped in this application. Memory mapping is possible by using the data-space select (-DS) rather than the I/O-space select (-IS) on the TMS32020/C25.



TMS32020/C25-TLC54X, TLC154X INTERFACE:

- Data transfer software initiated on TMS32020/C25
- TMS32020/C25 using burst mode for transfers on serial port
- 3 packages used for glue logic: 74HC04 and 2X 74HC163
- Glue logic can be replaced with one PAL, 16R8

J1 – TMS32020 operation:
Connect 1 and 4 for 1.25 MHz clock
Connect 2 and 4 for 625 kHz clock
TMS320C25 operation:
Connect 2 and 4 for 1.25 MHz clock
Connect 3 and 4 for 625 kHz clock

J2 – Connect 1 and 2 for single TLC54X/154 X operation
Connect 1 and 3, 2 and 4 for multiple TLC54X/154X operation

J3 – Connect 1 and 3 for TLC154X
Connect 1 and 2 for TLC540/1.

Figure 11-243. TLC54X, TLC154X to TMS32020/C25 Interface

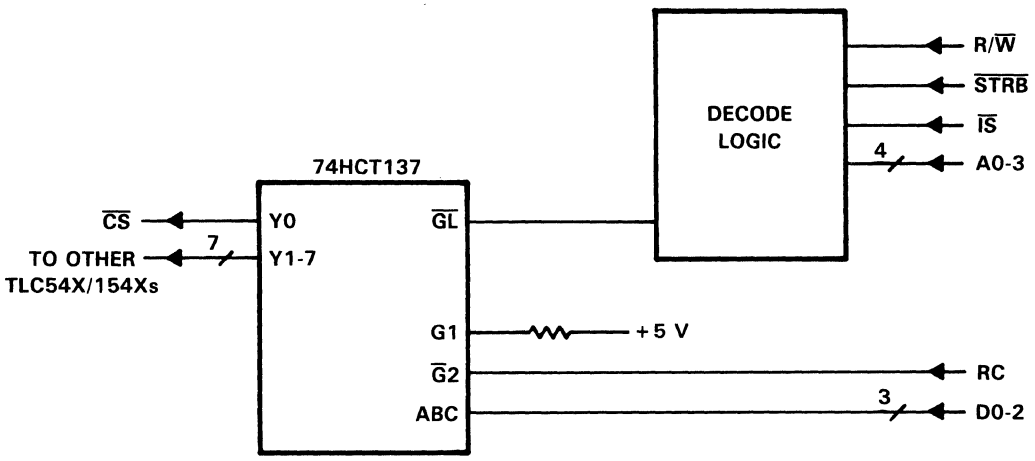


Figure 11-244. Expansion Circuitry for TMS32020/C25 to TLC154X/54X Interface

Software

For proper operation of the TMS32020/C25 with the hardware, two of its status bits, TXM and FO, must be correctly set as shown in the following software listing. TXM is the transmit mode bit that configures the FSX pin as an input or an output. This application requires FSX to be an output. Consequently, the TXM bit must be set high. The value of the TXM bit can be modified by using the STXM or RTXM instructions. Note that TXM is set low upon reset. The TXM bit should be set high using the STXM instruction during the reset initialization routine. FO is the serial I/O format bit that defines the data transfer to be either 8 or 16-bit formats. This application requires data transfers to be in a 16-bit format. Therefore, the FO bit must be set low. The FO bit can be modified using the FORT instruction. Note that the FO bit is correctly set low at reset. TLM and FO can also be modified using the LST1 instruction.

Attention must be paid to the bit positions of the data in the 16-bit word on the TMS32020/C25. Bit positions are skewed as a result of the 2.5 system clock delay in the TLC54X/154X to recognize a chip-select. The TMS32020/C25 must embed the analog input address at the proper bit locations to be correctly recognized by the TLC540/1 and TLC1540/1. Similarly, the TMS32020/C25 must correctly interpret the proper bit locations of the data sent by the TLC54X/154X. The timing diagrams (see Figure 11-245) illustrate the skew in the bit locations. Bit manipulations are easily performed using logical operators and bit shifting such as the AND, ANDK, OR, ORK, XOR, XORK, LAC and LACT instructions. Table 11-44 shows the proper bit locations.

Table 11-44. TMS320/C25 Data Bit Positions

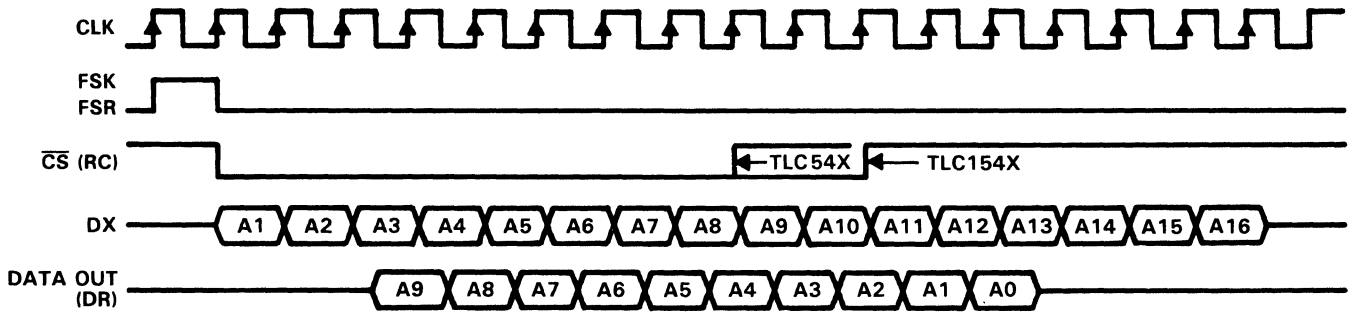
BIT POSITIONS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLC540/1 AND TLC1540/1 ADDRESS IN			B3	B2	B1	B0										
TLC154XDATA OUT				A9	A8	A7	A6	A5	A4	A3	A2	A1	A0			
TLC54X DATA OUT				A7	A6	A5	A4	A3	A2	A1	A0					

Other Considerations

Data transfers between the TMS32020/C25 and the TLC54X/154X are initiated under software control. External stimulus for these transfers is possible by using the TMS32020/C25 external interrupt inputs ($\overline{INT}$) and the branch control input ($\overline{BIO}$).

The TLC54X/154X require a minimum number of system clock cycles to occur between valid transfers to allow for ADC conversion. Conversion time periods are specified on the TLC54X/154X data sheets. Be sure to wait the conversion time period between transfers to obtain valid data. Wait periods can be timed by using the timer function in the TMS32020/C25.

```
* Software for TLC54X/154X to TMS32020/C25
* Interface
*
*
          AORG   >0
          B      INIT
*
* Interrupt Service Routine:
* After the conversion data has been transferred to the
* TMS32020/C25 Data Receive Register, the Receive Interrupt
* causes the processor to branch to location 26.
*
          AORG   26
          ZALS   >0       Save unshifted result.
          ANDK   >1FFF    Mask receive bits.
          RPTK   2        Shift receive bits.
          SFR
          SACL   >60      Save conversion result in >60.
          RPTK   127      Delay for conversion.
          NOP
          RPTK   127
          NOP
          RPTK   127
          NOP
          B      TXRX     Get new conversion result.
*
* Initialization Routine:
*
INIT      DINT            Disable interrupts.
          LDPK   >0       Set Data-Memory Page Pointer to >0.
          LACK   >10      Enable (RINT) interrupt.
          SACL   >4
          STXM            Set transmit mode (FSX is an output).
          FORT   0        Set data format to 16 bits.
*
* Data Transfer Routine:
*
TXRX      LACK   >5       Load Accumulator with address (channel 5).
          RPTK   9        Shift address 10 places to the left.
          SFL
          SACL   >1       Place channel address in Transmit Register.
          EINT            Enable Interrupts.
WAIT      B      WAIT     Wait for receive interrupt.
```



TMS32020/C25

NOTES: • Burst mode for serial data transfer
- FSX is an output, TXM status bit set to "1"
- 16-bit word transfers required, FO status bit set to "0"

Figure 11-245. Timing Diagram for TLC154X

INTERFACING THE TLC548/9 TO THE TMS32020

Hardware

The interface circuit employs three packages:

1	SN74LS175	Quad Positive-edge Triggered D-type Flip-flop with Common Clock and Clear
1	SN74LS02	Quad Positive-NOR Gate
1	SN74LS74	Dual Positive-edge Triggered D-type Flip-flop with Independent Clocks, Clear and Preset.

Note: One 74LS175 may be substituted for the 74LS74.

The 74LS74 (or, 1/2 of a 74LS175) is used to implement a ring counter which divides the frequency of the CLKOUT signal, provided by the TMS32020, by four and yields four separate output phases. For example, if the frequency of CLKOUT is 5 MHz, then the output frequency of the counter is 1.25 MHz. If the 74LS74 is used, the clocks should be tied together and all PRESET and CLEAR inputs should be tied to the positive supply voltage. If the 74LS175 is used, only two of the four flip-flops are needed and the common CLEAR should be tied to the positive supply. The complete interface circuit is shown in Figure 11-246.

Principles of Operation

As shown in Figure 11-247, the timing diagram, XF is normally high and is brought low under software control (an RXF instruction as shown in the software listing). Since XF is tied to $\overline{CS}$ of the TLC549, $\overline{CS}$ is also brought low. The TLC548/9 requires a maximum of 1.4 microseconds of delay from the falling edge of $\overline{CS}$ until valid data appears at the output. This is implemented with a 74LS175 which provides 2 microseconds of delay between the falling edge of $\overline{CS}$ and the falling edge of FSR, which begins data transfer.

After the falling edge of FSR, the first data bit is clocked into the DRR (Data Receive Register) of the TMS32020 on the falling edge of CLKR. Two-hundred nanoseconds later, the TLC548/9 sees a falling edge of I/O CLOCK and places the next bit on the DATA OUT pin. As shown in Figure 11-247, the phase relationship between CLKR and I/O CLOCK allows 600 ns from the falling edge of I/O CLOCK (which clocks-out the next data bit) and the next falling edge of CLKR (which clocks the bit into the DRR register of the TMS32020).

Since the TLC548/9 is an 8-bit A/D converter, the serial port of the TMS32020 should be configured to read 8-bits at a time. This is accomplished by setting FO, the internal format bit, equal to 1. On the eighth falling edge of CLKR after FSR goes low, the last data bit (the LSB) is clocked into the DRR register, and the TMS32020 generates RINT, the serial port read interrupt. If the interrupt is enabled (i.e. the TMS32020 has been instructed to recognize the interrupt), the TMS32020 executes the instruction residing in memory location 26, which should be a branch to a routine which reads the data in the DRR register and raises XF (with an SXF instruction).

If the interrupt (RINT) has been disabled, XF should be raised (with an SXF instruction) after the eighth falling edge of I/O CLOCK (i.e. a minimum of 44 CLKOUT cycles after it was initially lowered).

Because the eighth falling edge of I/O CLOCK initiates the hold-mode of the TLC548/9's internal sample-and-hold and starts the next conversion, it is important that the eighth falling edge of I/O CLOCK occur before XF is raised. XF should be kept high for a minimum of 17 microseconds (85 CLKOUT cycles) before the next RXF instruction, thus allowing the TLC548/9 enough time to complete the next conversion.

If XF is lowered before the conversion is complete, the TLC548/9 will halt conversion and the results of the previous conversion will be transferred to the DRR register of the TMS32020.

```
*
*
* Software for TLC548/9 to TMS32020 Interface
*
*
          AORG   >0
          B      INIT     Branch to initialization routine
*
* Interrupt Service Routine:
* After the conversion data has been transferred to the
* TMS32020 Data Receive Register, the Receive Interrupt
* causes the processor to branch to location 26.
*
          AORG   26
          SXF             Raise /CS (XF pin of TMS32020).
          LAC    >0       DRR is data-memory location 0.
          SACL   >60      Save result in data-memory address >60.
          RPTK   85       Delay for conversion.
          NOP
          B      GETDAT
*
* Initialization Routine:
*
INIT      DINT            Disable interrupts.
          SXF             Raise /CS.
          LDPK   >0       Set data-memory page pointer.
          LACK   >10      Load Interrupt Mask Register
          SACL   >4       with correct data to enable RINT.
          FORT   1        Set data format to 8 bits.
*
* Data Transfer Routine:
* This routine lowers /CS of the TLC548 and begins data transfer.
*
GETDAT    RXF             Lower /CS.
          EINT            Enable Interrupts.
WAIT      B      WAIT     Wait for Receive Interrupt.
          END
```

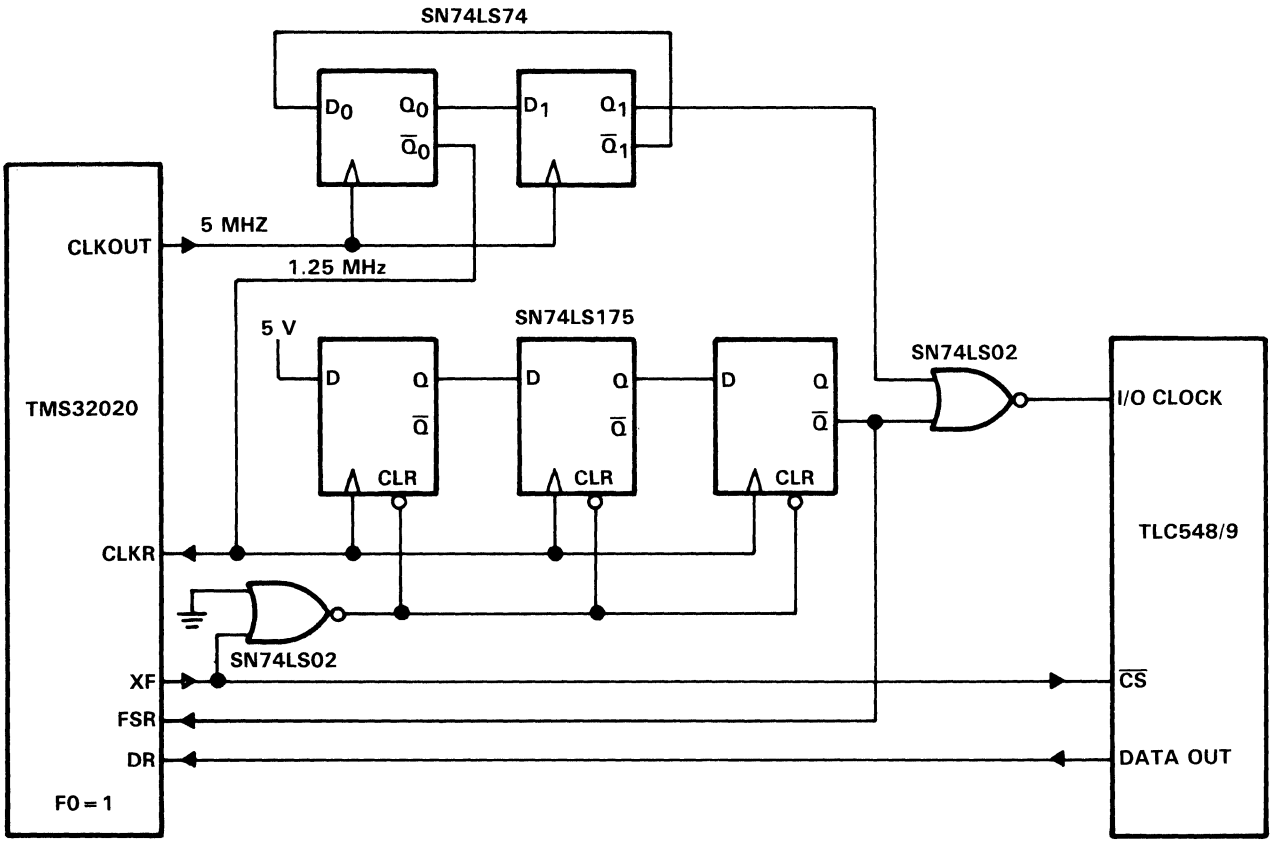


Figure 11-246. TLC549-TMS32020 Interface

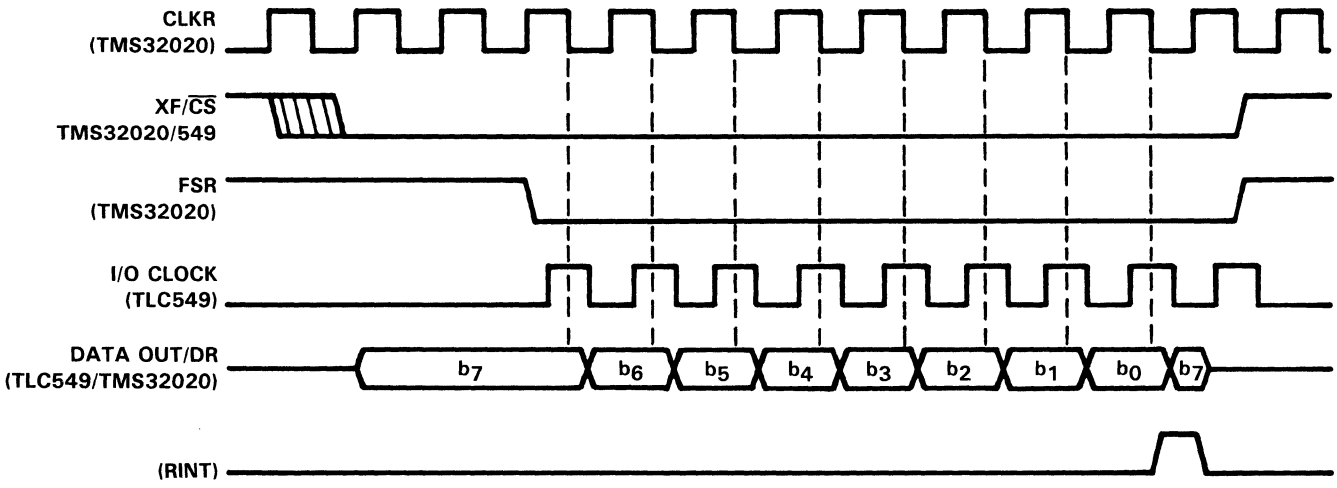


Figure 11-247. TLC548/9 to TMS32020 Interface Timing

Section 12

Special Functions

THE HALL EFFECT

Edwin Hall first noted the effect that bears his name at Johns Hopkins University in 1879. He was investigating the effects of a steady magnetic field on current in a thin gold foil. He observed a small voltage at the edges of a current-carrying gold foil when a magnetic field was applied that was perpendicular to the foil.

THE HALL EFFECT IN SILICON

The Hall effect occurs as current flows through a semiconductor material in the presence of a magnetic field. As electrons or holes flow through the material, their path depends on the charge density and velocity of the majority carriers as well as the magnetic flux. In Figure 12-1, if current (I) flows from left to right with magnetic flux (B) in the direction shown, the force (F) applies downward on the majority carriers, whether holes or electrons. Charge carriers collect near the bottom surface of the semiconductor material and generate the Hall voltage. In n-type material, the majority carriers are electrons and the polarity of the Hall voltage becomes negative on the bottom surface with respect

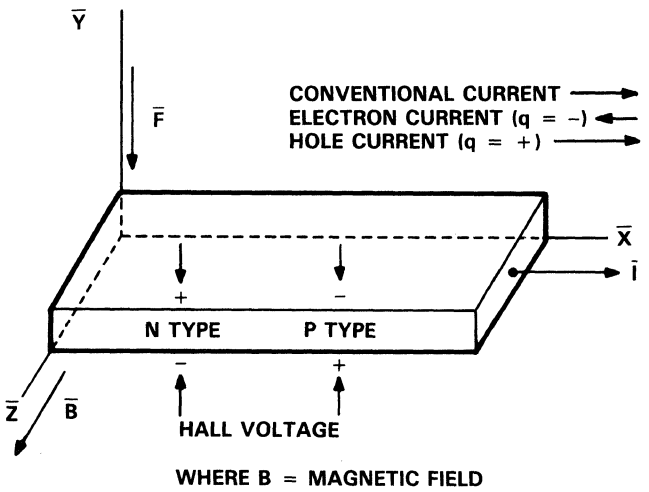


Figure 12-1. Hall-Effect Current Flow

to the top. The converse is true for p-type material because holes are the majority carriers. Accurate diffusion of a specific impurity into silicon determines the mobility of the majority carriers and the charge density. The Hall effect ideally produces a repeatable Hall voltage that is linearly proportional to the external magnetic field.

However, in addition to magnetic-field intensity, there are other semiconductor-material factors that govern the Hall voltage, including temperature, mechanical stress, and current. Both mechanical stress and temperature changes affect mobility of the majority carriers. Also changes in current flow cause nonlinear fluctuations in the Hall voltage. A constant-current generator eliminates current changes, and temperature-compensation circuits offset the thermal effects. The nonlinearity caused by mechanical stress is not easily corrected. The most desirable approach for minimizing the effects of mechanical stress utilizes the architecture of the sensor. Figure 12-2 shows the geometric layout of the orthogonal cross-coupled Hall cell. The cell with four sensors

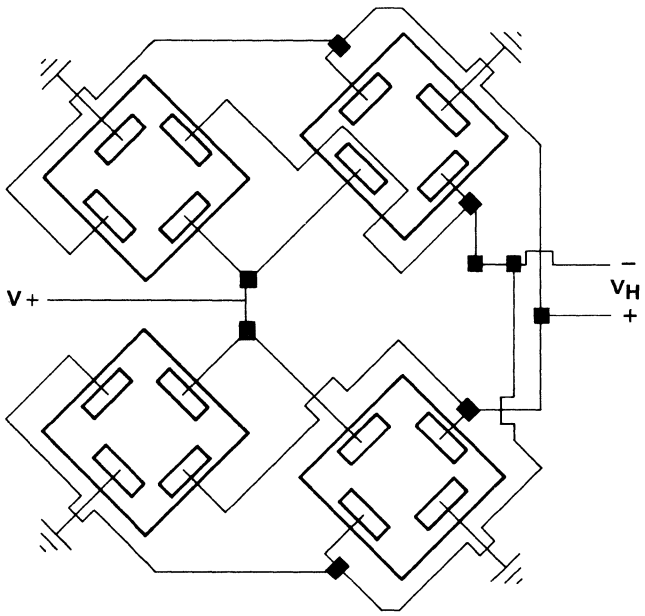


Figure 12-2. Hall-Effect Sensor Layout

connected in an orthogonal manner, reduces the effect of mechanical stress and also improves sensitivity to magnetic fields. The cross coupling of devices also reduces process-related variations and reduces the offset by a factor of 16.

HALL-EFFECT DEVICES

A Hall-effect device is a circuit consisting of a Hall-effect cell, signal conditioning functions which may include hysteresis, and an output transistor integrated into a monolithic chip. The three basic types of Hall-effect devices are the switch, the latch, and the linear device. The switch and latch are digital devices while the linear Hall device provides a voltage output that is linear with respect to changes in magnetic flux density. The unit of magnetic flux density in the International System of Units is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten, e.g., 50 millitesla = 500 gauss.

SWITCHING DEVICES

The typical switching device is used in applications calling for a normally OFF Hall-effect switch. This device turns ON in the presence of a positive magnetic field and turns OFF when the field is removed. A typical transition diagram for this type of device is shown in Figure 12-3. Note that both the operate point (B_{OP}) and the release point (B_{RP}) are positive values. The hysteresis provides stable switching characteristics. The operating and release values, and the

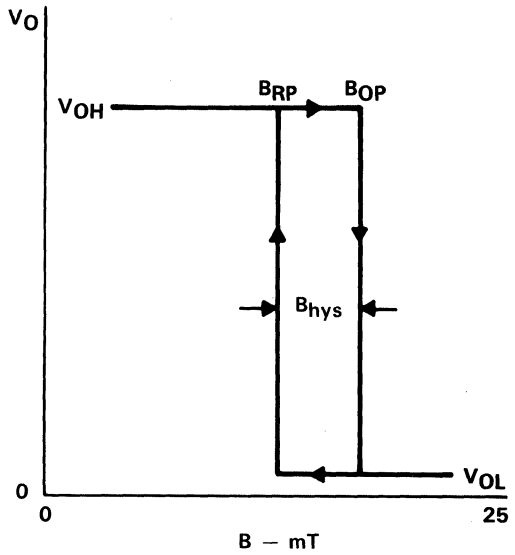


Figure 12-3. Representative Curve of V_O vs B

width of the hysteresis, are parameters that should be considered when choosing a device and magnet for a specific application. The functional block diagram for a switching device is shown in Figure 12-4.

LATCHING DEVICES

A Hall-effect latch is a switch that turns on in the presence of a positive magnetic field and off in the presence of a negative magnetic field. The maximum positive field strength required to turn ON a typical latch is 25 mT. The minimum field to turn a typical latch OFF is -25 mT. See Figure 12-5 for a hysteresis-loop characteristic diagram. The

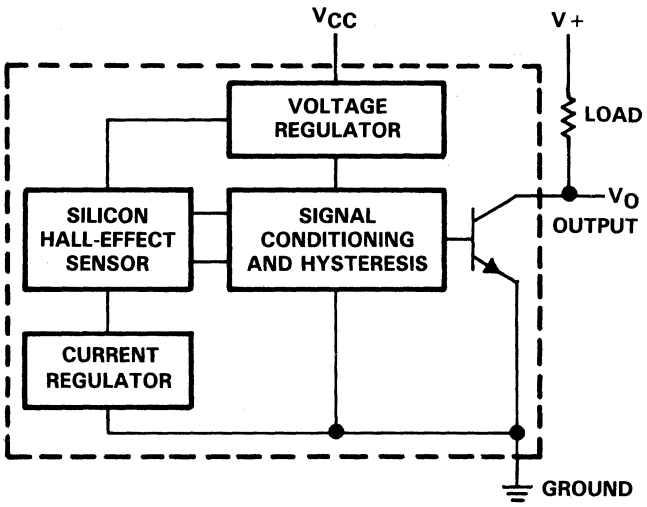


Figure 12-4. Functional Block Diagram of Hall-Effect Switch

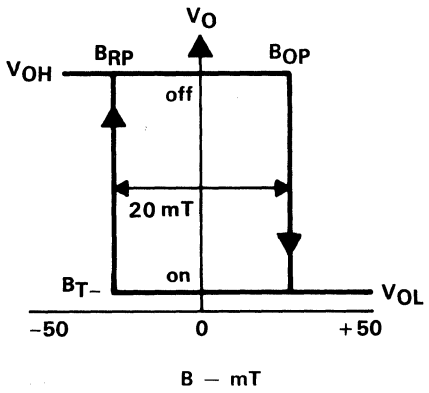


Figure 12-5. Representative Curve of V_O vs B

output transistor is turned on when a positive field of sufficient magnitude is present and remains on until a negative magnetic field of sufficient magnitude is present.

LINEAR HALL DEVICES

A linear Hall-effect device may be defined as a magnetic field sensor designed to provide an output voltage change that is linearly proportional to a change in the applied magnetic field. Not all applications involve strictly ON/OFF switch conditions; sometimes you must know the strength of a magnetic field and its polarity. Linear Hall-effect devices contain no hysteresis circuitry, but their sensitivity (approximately 16 mV/mT) facilitates accurate magnetic-field-strength measurement.

You may also utilize such a linear sensor to determine a magnetic field's polarity if you know the device's intercept value (the point at which the sensor's output voltage characteristic crosses the zero magnetic field strength line). An output voltage greater than the intercept value indicates the presence of a north magnetic pole, while a smaller output denotes a south pole.

Figure 12-6 shows the functional block diagram of a TL3103 linear Hall-effect device. This circuit incorporates a Hall element as the primary sensor along with a voltage reference and a precision amplifier.

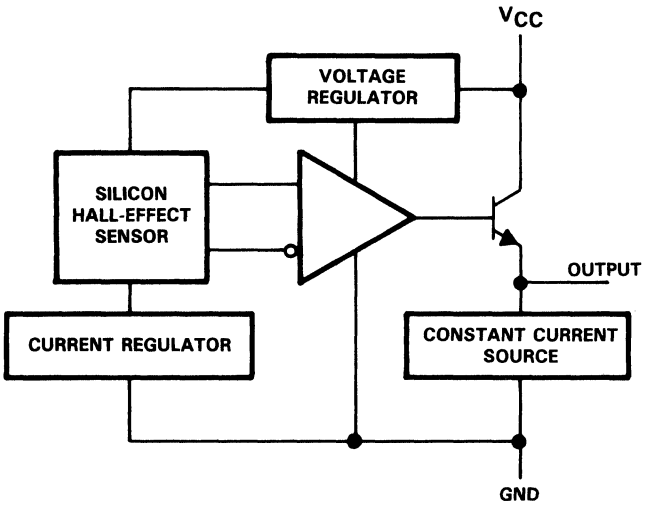


Figure 12-6. TL3103 Functional Block Diagram

Temperature stabilization and internal trimming circuitry provide a device that features high overall sensitivity accuracy with less than 5% error over its operating temperature range. The Hall voltage is amplified to provide a convenient voltage level that is proportional to the magnetic field sensed. The nominal output voltage in the presence of a zero magnetic field is 6 V. The output voltage increases 16 mV/mT with a positive magnetic field and decreases 16 mV/mT with a negative magnetic field as shown in Figure 12-7.

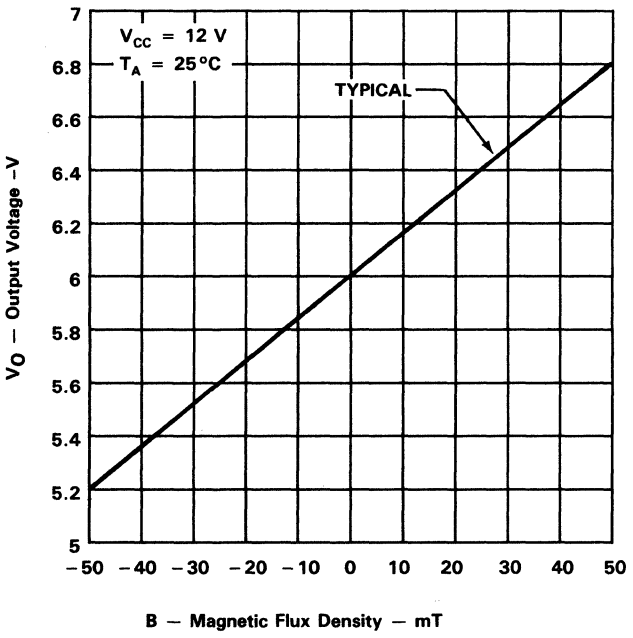


Figure 12-7. TL3103 V_O vs Magnetic Flux Density

ADVANTAGES OF HALL-EFFECT DEVICES

Hall-effect devices give distinct advantages over mechanical and optoelectronic switches. For example, switching thresholds in Hall-effect devices do not degrade with time, as they do in emitter/sensor pairs. Additionally, while stray light affects photosensors in some applications, stray magnetic fields do not generally trigger Hall-effect sensors. As another advantage, you can isolate magnetically activated Hall-effect devices from environmental hazards such as dirt, dust, light, water, or vapor. You cannot as readily seal mechanical and optical switches and relays against contamination. Where moisture is a problem or where a switch spark might ignite explosive vapors, a specially sealed mechanical switch entails high cost. Further Hall-effect advantages over mechanical switches and relays include no contacts to wear, pit, or weld. No-contact switching implies a low failure rate and no maintenance. An internal hysteresis circuit in Hall-effect switches also eliminates contact bounce, a serious problem where mechanical switches must interface directly to a microprocessor.

HALL-EFFECT DEVICE SELECTION

It is helpful to understand that two conventions are used by manufacturers in specifying the magnetic properties of today's devices. The definitions "into" and "out of" the cell cause confusion because both are defined in terms of the orientation of a bar magnet relative to the cell. If the magnet is perpendicular to the cell and the north pole is closest to the sensor, the field is "into the cell" when using the north-pole positive convention. If the south pole is closest to the sensor, the field is "out of" the cell. (See Figure 12-8.) The south-pole positive convention reverses this definition. It is important to take note of the orientation of the magnet with respect to the face of the Hall-effect unit when selecting a device for a specific application.

The TL31xx series uses the north-pole positive convention, as opposed to other similar devices that use the south-pole positive convention. Also, TI second sources UGN30xx parts with the TL30xx series, and these devices are south-pole positive. Therefore, you should check the specifications carefully before selecting a device. Table 12-1 shows a list of Hall-effect devices with respect to their electrical and magnetic properties.

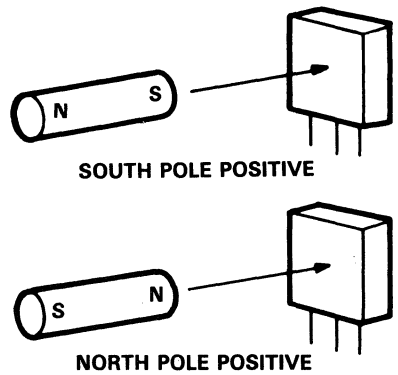


Figure 12-8. Determining Polarity

Table 12-1. Electrical and Magnetic Properties of Hall-Effect Devices

NORTH POLE POSITIVE DEVICES

DEVICE	TYPE	V_{CC} SUPPLY	V_{OUT}	I_{OUT}	HYSTERESIS (TYPICAL mT)	SENSITIVITY (mT)
TL3101	General-purpose switch	5 V	30 V	20 mA	20	+25/−25
TL3103	Linear	12 V	5.8 to 6.2 V (B = 0)	Sink 0.5 mA Source 2 mA	------	(Typical) 16 V/T

SOUTH POLE POSITIVE SWITCHES

DEVICE	TYPE	V_{CC} SUPPLY	V_{OUT}	I_{OUT}	HYSTERESIS (TYPICAL mT)	SENSITIVITY (mT)
TL3013	N.O.	4.5 to 40 V	40 V	30 mA	7.5	45/25
TL3019	N.O.	4.5 to 40 V	40 V	30 mA	12	50/12.5
TL3020	N.O.	4.5 to 40 V	40 V	30 mA	5.5	35/5
TL3030	General Purpose	4.5 to 40 V	40 V	30 mA	5	+25/−25
TL3040	N.O.	4.5 to 40 V	40 V	30 mA	5	20/5

N.O. = Normally open.

HALL-EFFECT APPLICATIONS

Although the key feature of a silicon Hall-effect device is its ability to sense magnetic fields, applications are not limited to magnetic-field-related uses. You can utilize them to sense virtually any type of movement by incorporating magnetic material in the moving object. While environmental conditions such as moisture and vibration can adversely affect optical and mechanical devices, Hall-effect units are immune to most environmental conditions.

Traditionally, engineers have not used Hall-effect devices because their cost was much higher than opto or mechanical components. The cost of Hall components has dropped significantly in the past five years so this is not a significant factor in most designs. Designers can now consider using Hall sensors in many applications where mechanical or optical sensors have been used.

The following applications demonstrate methods of using Hall-effect sensors in isolated feedback applications and to sense motion or position.

TL3103 LINEAR HALL-EFFECT DEVICE IN ISOLATED SENSING APPLICATIONS

For several years, opto coupler devices have been used for isolated sensing in power supplies. This application demonstrates how the TL3103 Hall-effect device can provide isolated sensing. The TL3103 senses the presence of either a positive or a negative magnetic field with a sensitivity of 16 mV/mT. In the absence of a magnetic field, the TL3103 output voltage is typically 6 V.

Because the output of the TL3103 varies proportionally to the magnetic flux density, the device can be used with a toroid to sense current or voltage. Current can be measured as shown in Figure 12-9. When the toroid terminals A and B are connected in series with the circuit to be measured, a change in current changes the magnetic flux density in the toroid gap and causes a voltage change in the TL3103 output. Whether the change is an increase or decrease depends on the direction of current flow through the toroid. The output of the TL3103 can be used to drive an amplifier as shown in Figure 12-9. The TL3103 output is 6 V in the absence of toroid current and flux. One input of the amplifier is therefore referenced to 6 V, allowing a level shift to 0 V at its output for zero sense current.

A similar arrangement provides an isolated voltage measurement. This is accomplished by connecting a resistor in series with the toroid as illustrated in Figure 12-10. The voltage to be measured is between terminals C and D. In this configuration, the current in the toroid is determined by the output voltage (Is = Vout/Rs). Thus, the output variations of the TL3103 are proportional to the sensed output voltage variations.

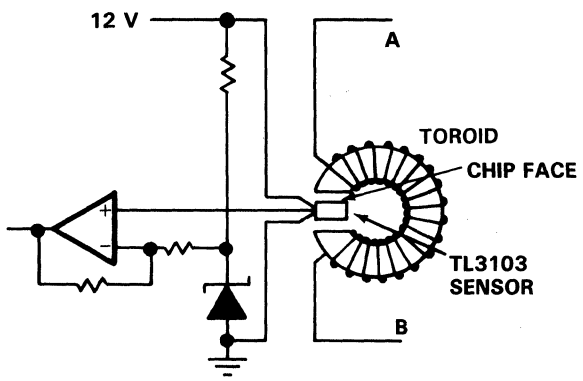


Figure 12-9. Current Measuring Circuit

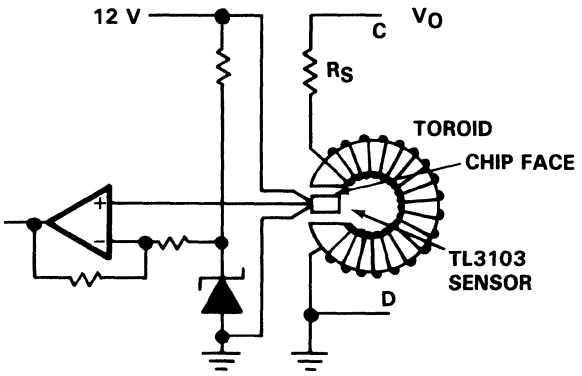


Figure 12-10. Voltage Measuring Circuit

Toroid Design

A variety of soft magnetic materials can be used in manufacturing cores for use with Hall-effect devices. These include manganese-zinc based ferrites, Molypermalloy powder cores, high flux powder cores, and strip wound tape cores.

The choice of the core to be gapped and used with a Hall-effect device depends upon the core characteristics required, cost, and stability over temperature. The effective permeability of the material is a function of the air gap made in the core and the initial permeability of the starting material. Permeability (μ) is defined as the ratio of magnetic flux density (B) in gauss to magnetic field intensity (H) in oersteds. (μ = B/H).

When the gap in a core exceeds a few thousandths of an inch, the effective permeability is determined essentially by the air gap. The magnetic field intensity (H) of a toroid is given by the expression NI/L where:

NI = number of turns (N) x current (I)
L = mean length of the toroid

The expression for the magnetic flux density then becomes:

$$B = (\mu)\ (NI/L)$$

With an air gap, the expression is altered to:

Bgap = μ (NI/L+Kg) K
μ_o = permeability of air (12.57×10^{-7} W/Am)
K = relative permeability of the toroid (μ/μ_o)
g = length of the air gap
W/Am = Webers/amp-meter

As previously discussed, the output of the TL3103 is:

$$V_{sense} = 6 \text{ volts} + (16\text{mV/mT})(\mu_o\ NI/g)$$

This shows how the output of the TL3103 varies with the amp-turns of the toroid. The applications in Figures 12-9 and 12-10 use an Arnold toroid #A393163-2 with a 0.165 inch air gap which is sufficient for an LU package. The magnetic flux density in the air gap is:

$$B(\text{gauss}) = 1.92\ NI\ (\text{amp-turns})$$

Thus, the variation in the output of the TL3103 is:

$$V\ \text{sense (mV)} = (1.6)(1.92\ NI)$$

Therefore, the sensitivity of the TL3103 device to the current in the winding is determined by the number of turns in the winding.

V sense	N	I
614 mV	20	10 A
614 mV	200	1 A
614 mV	2000	100 mA

The features of this approach are:

1. Minimum power loss in the sensing element
   P loss = I^2R in the toroid
   (R < 0.01 for 20 turns)
2. Isolated feedback, no passive connection required.

TL594 ISOLATED FEEDBACK POWER SUPPLY

Figure 12-11 is a power supply circuit using the isolated feedback capabilities of the TL3103 for both current and voltage sensing. (See Figures 12-9 and 12-10). This supply is powered from the ac power line and has an output of 5 V at 1.5 A. Both output voltage and current are sensed and the error voltages are applied to the error amplifiers of the TL594 PWM control IC.

The 24 V transformer produces about 35 V at the 1000 μF filter capacitor. The 20 kHz switching frequency is set by the 6 kΩ resistor and the 0.01 μF capacitor on pins 6 and 5, respectively. The TL594 is set for push-pull operation by tying pin 13 high.

The 5 V reference on pin 14 is tied to pin 15 which is the reference for the current error amplifier. The 5 V reference is also tied to pin 2 which is the reference for the output voltage error amplifier. The output voltage and current limit are set by adjustment of the 10 kΩ pots in the TL3103 error sensing circuits. A pair of TIP31E npn transistors are used as switching transistors in a push-pull circuit. The transformer design information is given in Figure 12-12.

TACHOMETER AND DIRECTION OF ROTATION CIRCUIT

In machine and equipment design, some applications require measurement of both the shaft speed and the direction of rotation. Figure 12-13 shows the circuit of a tachometer which also indicates the direction of rotation.

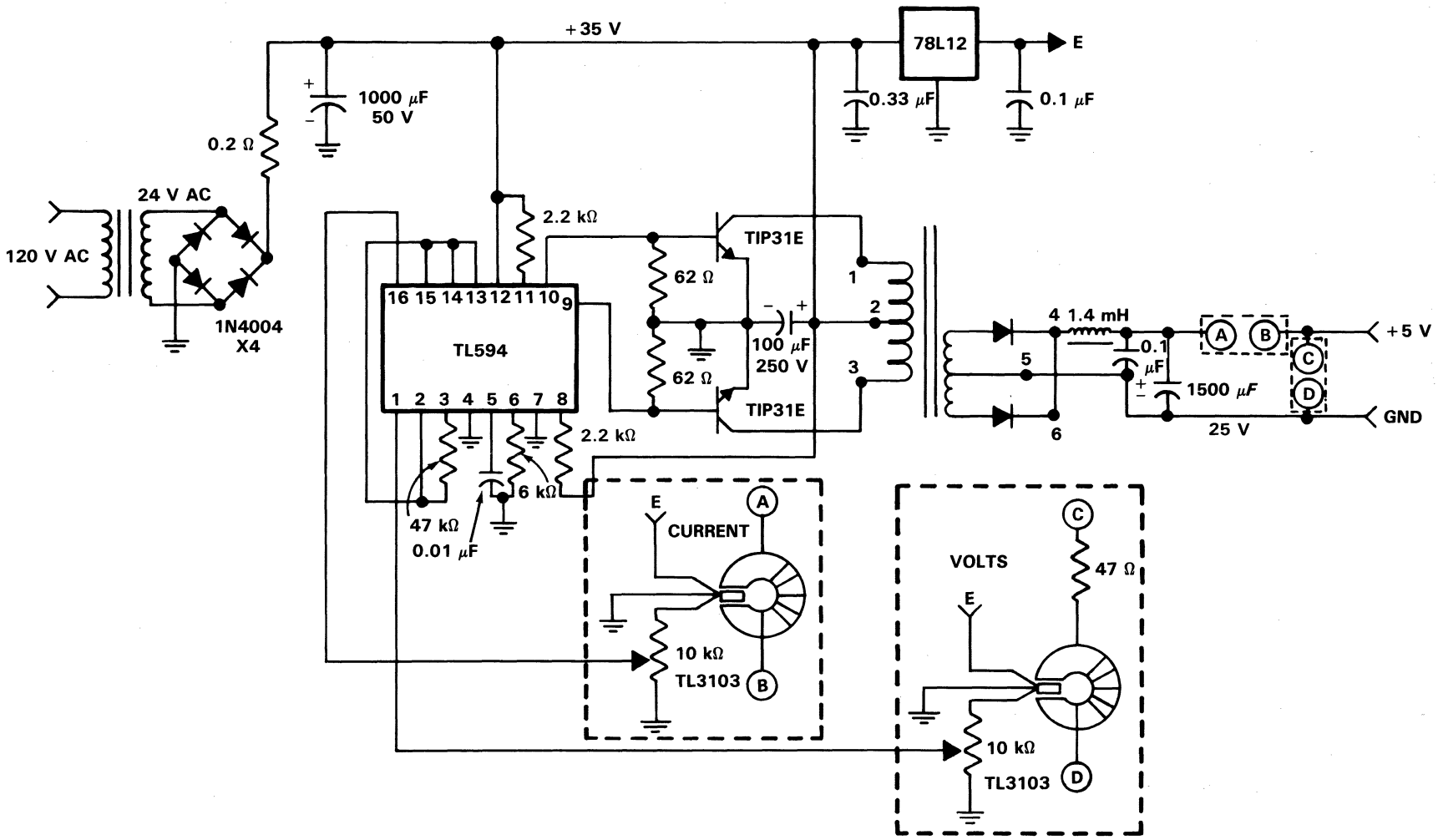


Figure 12-11. TL594 Isolated Feedback Power Supply

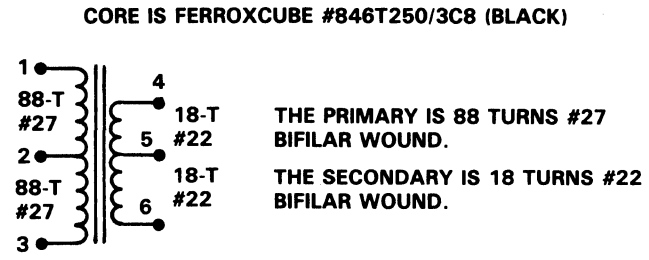


Figure 12-12. Transformer Design Data

Tachometer Operation

The flywheel sensor is a TL3101 Hall-effect switch selected for latch operation. The flywheel has two magnets embedded in the outer rim about 45 ° apart. One magnet has the north pole toward the outside and the other magnet has the south pole toward the outside rim of the flywheel. Due to the magnet spacing, a short ON pulse is produced by the TL3101 in one direction and a long ON pulse in the other direction. A 0–50 μA meter is used to monitor the flywheel speed while the LEDs indicate the direction of rotation.

The output from the TL3101 is applied to pin 3 (CLR 1) of an SN74LS123 one-shot multivibrator. The one-shot output pulse, at pin 13 (Q), goes high with a high input pulse. The output pulse duration is set to about 3 μs with the 1 μF capacitor and the 10 kΩ resistor on pins 14 and 15. The pulses at the output go through a low-pass filter, through diode D2, and to the 0–50 μA meter which is the tachometer. Since the TTL low-level output for the SN74LS123 is still about 0.3 V above ground, the meter would read slightly above zero when the flywheel is not moving. The purpose of the germanium diode, D2, is to produce a 0.3 V drop to correct for the 0.3 V low-level output. The meter may be calibrated in revolutions per minute (rpm), or as the user desires.

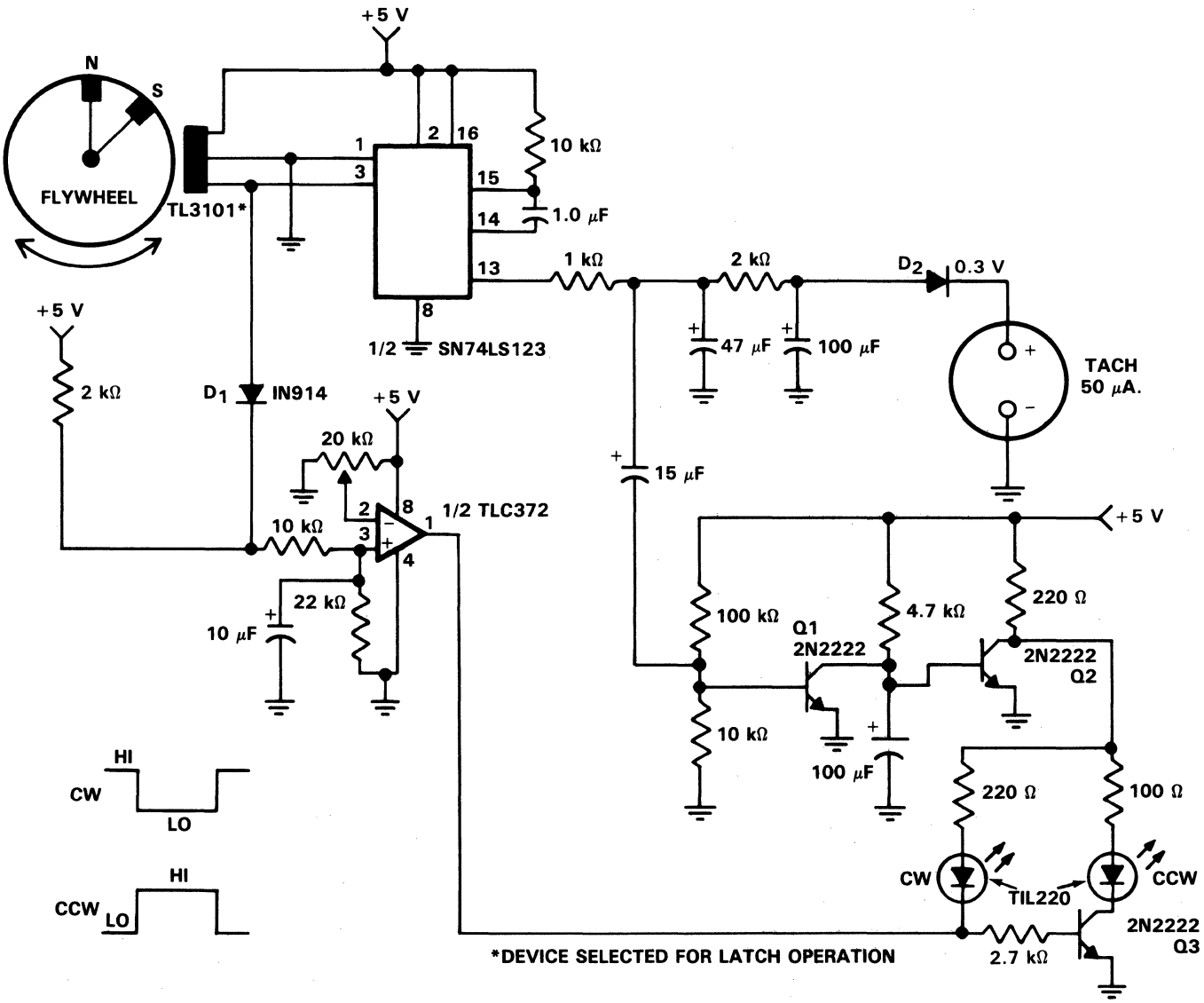


Figure 12-13. Tachometer and Direction of Rotation Circuit

Direction of Rotation Circuit

The direction of rotation circuit can be divided into three parts:

1. TLC372 device for input conditioning and reference adjustment
2. Two 2N2222 transistors which apply the V_{CC} to the two LEDs when needed.
3. The two TIL220 LEDs which indicate clockwise (CW) or counterclockwise (CCW) direction of rotation.

The input pulses going to the SN74LS123 one-shot multivibrator are also applied through diode D1 to the noninverting input of the TLC372 device. The inverting input is connected to a 20 kΩ potentiometer, providing an adjustable reference. When the flywheel is rotating in a clockwise direction, a short-high and a long-low pulse train is produced. This causes the output of the TLC372 device to be low, turning on the CW LED and holding the CCW LED off by turning the 2N2222, Q3, off.

In the counterclockwise direction, a short-low and a long-high pulse train is produced. This gives a high output from the TLC372 device which turns the CW LED off and turns on the 2N2222 transistor and the CCW LED. The 20 kΩ reference potentiometer is set between the average voltage level of the high-level pulses and the average voltage level of the low-level pulses. The speed of the flywheel will not make any difference in the calibration of the circuit because the ratio of the high- and low-pulse lengths stays the same.

LED V_{CC} Supply Control

This circuit keeps the LEDs off when the flywheel is not rotating. The circuit consists of two 2N2222 transistor switches, Q1 and Q2, which remove the 5 V supply voltage from the LED circuit when the flywheel is not turning. When the flywheel is stopped, there are no output pulses on the SN74LS123 output pin 13. At this time, there is only about 0.5 V bias voltage on the base of transistor Q1, holding it off. This causes the base of transistor Q2 to be high, which turns it on, prohibiting the supply voltage from being applied to the LEDs. With the wheel in motion, a train of pulses appears at the SN74LS123 output that passes through the 15 μF capacitor to turn transistor Q1 on. This turns off transistor Q2, allowing the collector to go high. This allows the 5 V supply voltage to activate the LED circuit.

ANGLE OF ROTATION DETECTOR

Figure 12-14(a) shows two TL3103 linear Hall-effect devices used for detecting the angle of rotation. The TL3103s are centered in the gap of a U-shaped permanent magnet. The angle that the south pole makes with the chip face of unit #1 is defined as angle θ. Angle θ is set to 0° when the chip face of unit #1 is perpendicular to the south pole of the magnet. As the south pole of the magnet sweeps through a 0° to 90° angle, the output of the sensor increases from 0° value of V_{OQ} to a peak value of +Vp at 90°. As the magnet continues to rotate to 180°, the output of the sensor retraces its path to V_{OQ}.

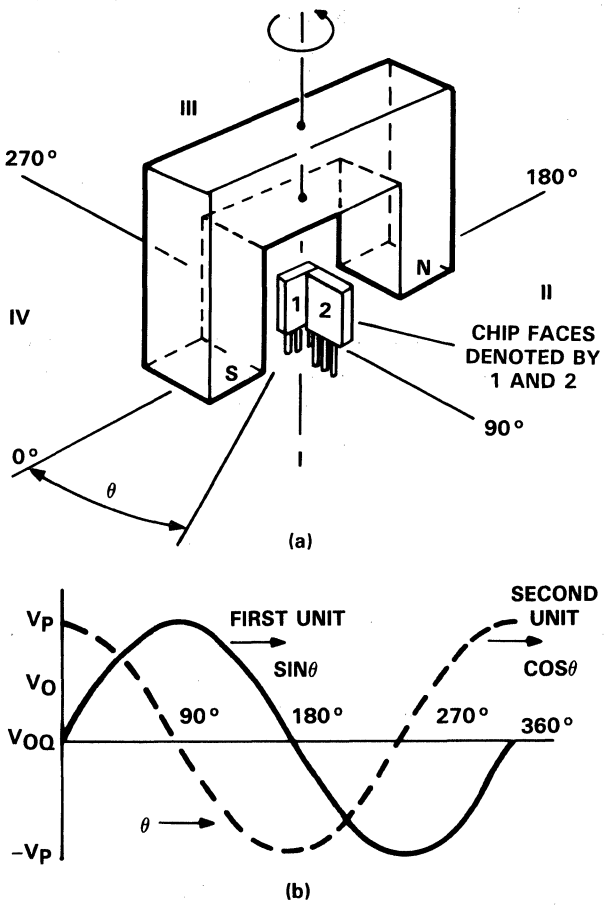


Figure 12-14. Two Linear Hall-Effect Devices Detect Angle of Rotation

Sensor unit #2 decreases from its peak value of +Vp at 0° to a value V_{OQ} at 90°. So, the output of sensor unit #1 is a sine function of θ and the output of unit #2 is a cosine function of θ as shown in Figure 12-14(b). Thus, the first sensor yields the angle of rotation and the second sensor indicates the quadrant location.

HALL-EFFECT COMPASS

The TL3103 linear Hall-effect device may be used as a compass. By definition, the north pole of a magnet is the pole that is attracted by the magnetic north pole of the earth. The north pole of a magnet repels the north-seeking pole of a compass. By convention, lines of flux emanate from the north pole of a magnet and enter the south pole. (See Figure 12-15.) The circuit of the compass is shown in Figure 12-16. By using two TL3103 devices instead of one, we achieve twice the sensitivity. With each device facing the opposite direction, device A would have a positive output while the output of device B would be negative with respect

to the zero magnetic field level. This gives us a differential signal to apply to the TLC251 op amp. The op amp is connected as a difference amplifier with a gain of 20. Its output is applied to a null meter or a bridge balance indicator circuit.

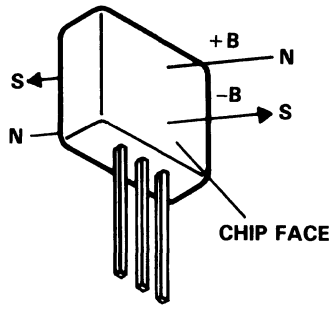


Figure 12-15. Definition of Magnetic Flux Polarity

SECURITY DOOR AJAR ALARM

In security systems for buildings, a switch of some type is installed on each door to be monitored. These may be mechanical switches or reed relay type switches operated by a permanent magnet placed in the door. A TL3019 is a normally open, south-pole-positive Hall-effect device, which may be used in this type of application. Figure 12-17 shows the basic circuit.

In operation, the TL3019 device will activate, or go low, when a south pole of a magnet comes near the chip face of the device. The example shows five doors. Each door has a magnet embedded in its edge with the south pole facing the outer surface. At the point where the magnet is positioned with the door closed, a TL3019 sensor is placed in the door jamb. With the door closed, the Hall devices will be in a logic low state. This design has five doors and uses five TL3019 devices. Each TL3019 has a 4 kΩ resistor in series with it and all door sensor and resistor sets are in parallel and connected to the inverting input of an LM393 comparator. With all doors closed, the effective resistance will be about 800 Ω and produce 2.2 V at the inverting input. The noninverting input goes to a voltage divider network which sets the reference voltage. The 1.5 kΩ potentiometer is adjusted so the indicator goes out with all doors closed. This will cause 2.35 V to appear at the noninverting input of the comparator. When a door opens, the voltage at the inverting input will go to 2.5 V which is greater than Vref, and the LED will light.

A large number of doors and windows may be monitored with this type of circuit. Also, it could be expanded to add an audible alarm in addition to the visual LED.

MULTIPLE POSITION CONTROL SYSTEM

In machine equipment design, it is sometimes necessary to select an operation or perform steps of another operation in a specific sequence. This application allows a drill press operator to choose a certain size bit, use it, and go to another selection.

Figure 12-18 shows the circuit of a multiple position sensor system. Eight TL3019 Hall devices are positioned outside the rim of a rotating disc for use in a drill-turret control application. Each of the normally OFF switches activates when aligned with the south (S) magnetic pole of the magnet, allowing a computer to stop the turret at any switch location. For example, if the computer chooses drill bit 4, and the turret reaches the bit 4 position, the output of sensor 4 turns on and sets an output latch. This latch output stops the turret motor. When an operator depresses the START pushbutton, the output latch resets and the turret rotates to the next selected drill bit.

There are many variations of this application that may be used in other designs. A comparatively new application is the brushless dc motor. Brushless dc motors are essentially brush-type dc motors turned inside out. Power is fed directly to the armature windings while a permanent magnet field is

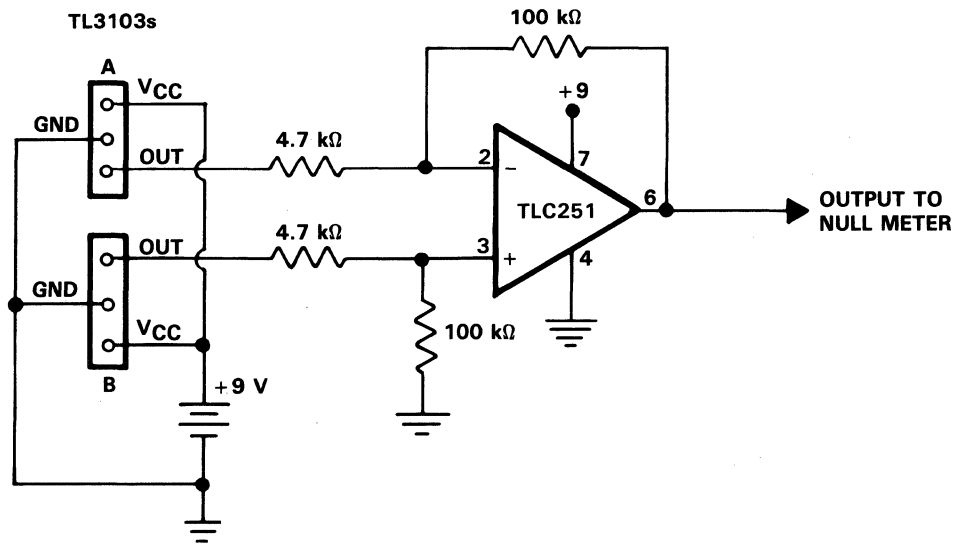


Figure 12-16. Linear Hall-Effect Compass

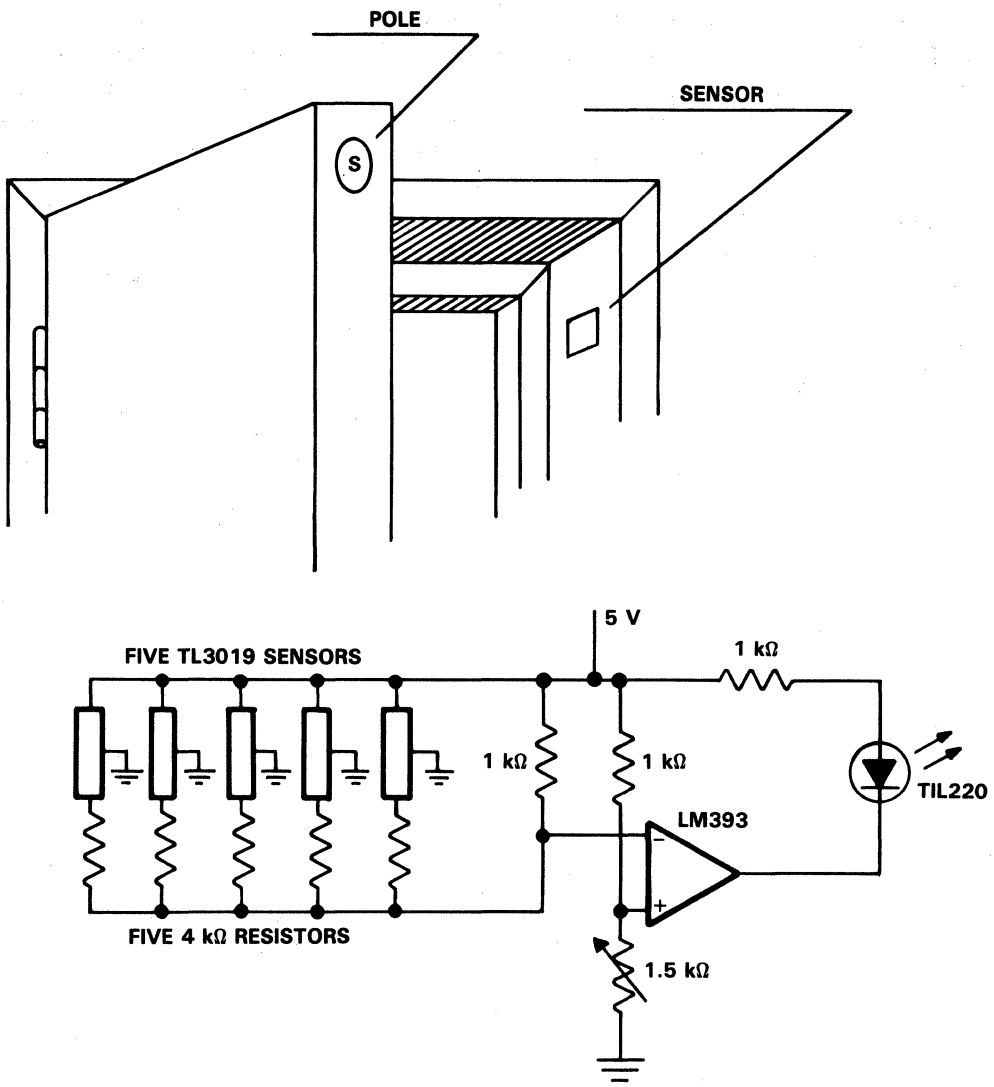


Figure 12-17. Security Door Ajar Alarm

the rotating member. In this type of motor, a Hall-effect sensor senses the position of the rotating magnet and excites the proper windings using a logic and driver circuit.

DOOR OPEN ALARM

Door open alarms are used chiefly in automotive, industrial, and appliance applications. This type of circuit can sense the opening of a refrigerator door. When the door opens, a triac could be activated to control the inside light.

Figure 12-19 shows a door position alarm. When the door is opened, an LED turns on and the the piezo alarm sounds for approximately 5 seconds. This circuit uses a TL3019 Hall-effect device for the door sensor. This normally open switch is located in the door frame. The magnet is mounted in the door. When the door is in the closed position, the TL3019 output goes to logic low, and remains low until the door is opened.

This design consists of a TLC555 monostable timer circuit. The 1 μF capacitor and 5.1 MΩ resistor on pins 6 and 7 set the monostable RC time constant. These values allow the LED and piezo alarm to remain on about 5 seconds when triggered. One unusual aspect of this circuit is the method of triggering. Usually a 555 timer circuit is triggered by taking the trigger, pin 2, low which produces a high at the output, pin 3. In this configuration with the door in the closed position, the TL3019 output is held low. The trigger, pin 2, is connected to 1/2 the supply voltage V_{CC}. When the door opens, a positive high pulse is applied to control pin 5 through a 0.1 μF capacitor and also to reset pin 4. This starts the timing cycle. Both the piezo alarm and the LED visual indicator are activated.

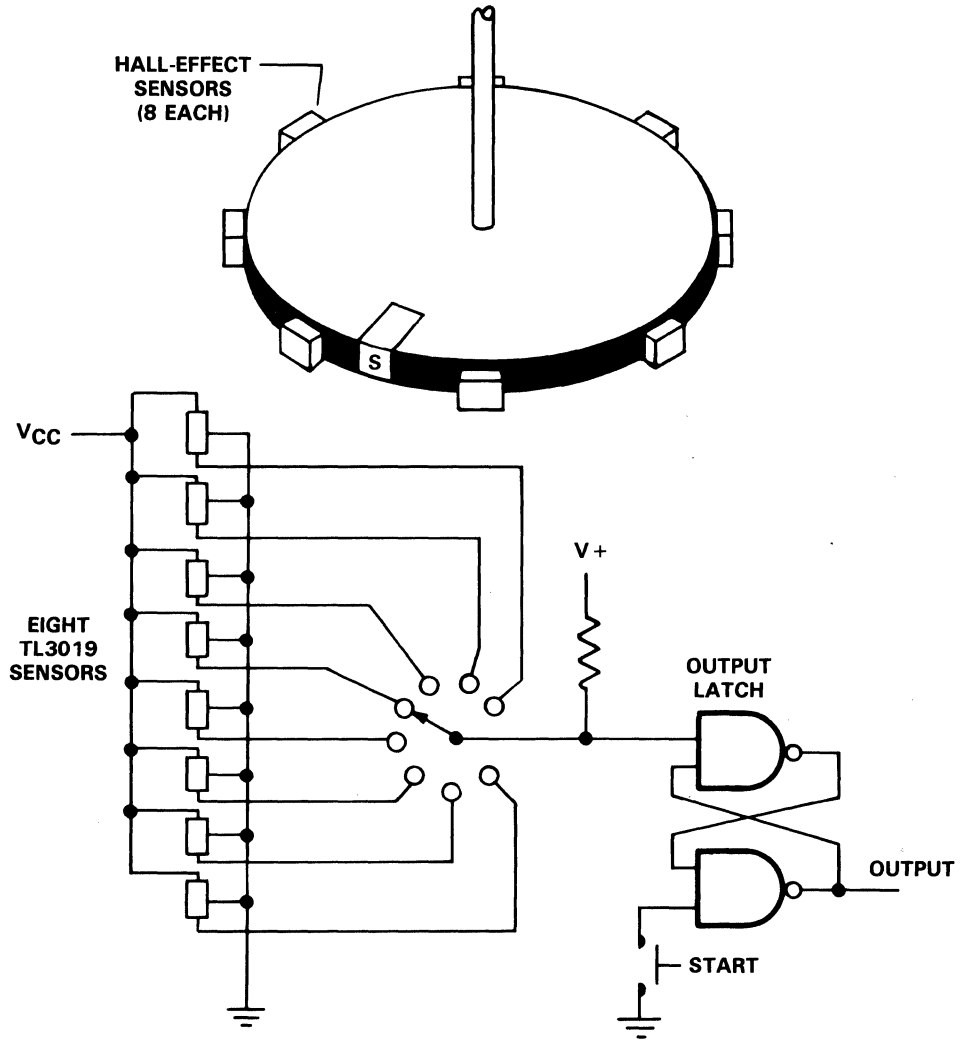


Figure 12-18. Multiple Position Sensor System

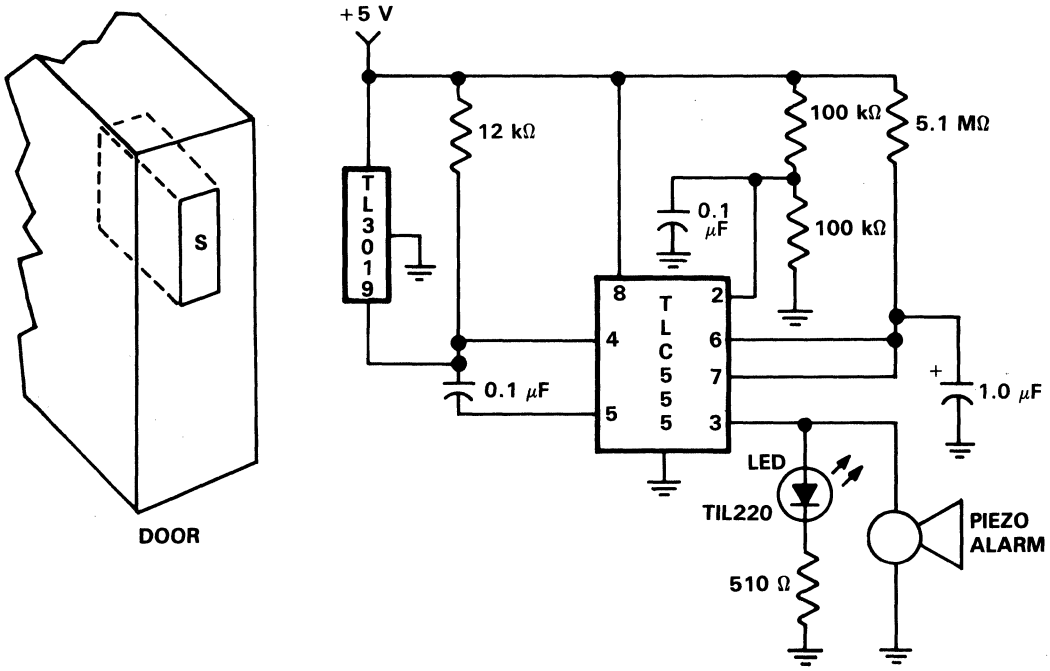


Figure 12-19. Door Open Alarm

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