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Volume 2: Line Circuits, Display Drivers

TEXAS INSTRUMENTS

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Volume 2

Line Circuits and Display Drivers

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TEXAS INSTRUMENTS

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Preface

This is the second volume in a three-volume series of Linear and Interface Circuit Applications books. To maintain overall continuity in the series, the section numbers in this book follow those in Volume 1. Volume 1 presented information on operational amplifiers, voltage regulators, and timers. Volume 2 provides information on display drivers and data line drivers, receivers, and transceivers. Volume 3 will provide information on peripheral drivers, data acquisition circuits, and special functions.

The purpose of this series of books is to present linear and interface circuit applications in a manner that will give the reader a basic understanding of the products and provide simple but practical examples for typical applications. Care has been taken to choose illustrations which are of interest, at least by analogy, to a wide class of readers. This material is written for not only the design engineer but also for engineering managers, engineering technicians, system designers, and marketing or sales people with some technical background. The authors have attempted to avoid lengthy mathematical analyses for technical elegance, so that the important points may be clearly emphasized and not obscured by distracting derivations. In cases where a rigorous derivation has been omitted, an attempt has been made to state the results precisely and to emphasize limitations that are practically significant.

To facilitate their use, the sections have been made basically independent. The primary goal of the books is to assist the user in selecting the proper device for a particular application. To accomplish this, key features of devices are presented along with discussions of device or system theory and requirements.

Potential uses of the devices are demonstrated in circuit applications. These applications are not intended to be a how-to for specific circuits but to be examples of how the device might be used to solve your specific design requirements. In each case, a data book or data sheet should be referred to for complete device characteristics and operating limits. The circuit examples selected for this book have accrued from numerous customer inquiries and related laboratory simulations.

This series of books has been written primarily by two members of the Linear Applications Staff. They would like to express their appreciation for the helpful inputs and assistance from members of the Linear Applications Lab, Product Engineering Staff, Field Application Engineering, and the European Applications Staff.

Section 8

Display Drivers

INTRODUCTION TO DISPLAY DRIVER TECHNOLOGY

Visual displays exist in a wide range of complexities from the simple incandescent bulb or light emitting diode (LED) indicators to complex full digital read-out or large flat-screen display panels. Until recently, many discrete transistors were required to drive the more complex visual display systems.

As the complexity of display systems grew, alternatives to discrete transistor drivers became imperative. An increasing number of monolithic integrated circuits are becoming available for driving many types of display systems, some of which were not considered practical until recently. Monolithic ICs that have been developed to drive digital and more complex displays include:

Light Emitting Diode Display Drivers
DC Plasma (Gas Discharge) Display Drivers
AC Plasma Display Drivers
Vacuum Fluorescent Display Drivers
Electroluminescent Display Drivers
Electrophoretic Display Drivers

Reliability of the higher voltage display drivers (all except LED drivers) has been poor in the past. In fact, ac plasma and electroluminescent display drivers were considered impractical because their complexity and high voltage required the use of many discrete power transistors and logic circuits. "BIDFET"* technology has made monolithic IC drivers possible by providing the voltage capability and complexity required for 64 power output transistors and control logic on a single chip.

*Bipolar, double diffused, N-Channel and P-Channel MOS transistors on the same chip — a patented process.

BIDFET is a rugged, low-cost wafer processing technology which merges precision control, self-isolated CMOS logic and high-voltage interface circuitry on a common monolithic substrate. It is manufactured using standard junction isolation techniques (see Figure 8-1). Many multitechnology processes have been developed, but BIDFET is the only merged process which alleviates the high voltage limitations of conventional integrated circuits while retaining their LSI logic capabilities. BIDFET devices are being produced with working voltages to 250 V and breakdown voltages exceeding 300 V. This has been achieved by replacing the conventional bipolar output stage with a Double-Diffused MOS (DMOS) transistor structure. The two output stage structures are compared in the following paragraphs.

First let us consider the limitations imposed by operating a bipolar switch within the Reverse Bias Safe Operating Area (RBSOA).

Figure 8-2 shows the typical load line characteristics of a switch operated within the device's RBSOA and $V_{CES(SUS)}$ ratings. If the load line penetrates the RBSOA, a destructive condition occurs. Thus, reliable operation may be limited to the $V_{BR(CEO)}$ rating of the switch.

With common topologies used in conventional integrated circuits, breakdown voltages [$V_{BR(CEO)}$] are limited by the thickness of the epitaxial layer. Practical limitations on the thickness of conventional junction isolated integrated circuits limits $V_{BR(CEO)}$ to 70 V.

The DMOS structure, on the other hand, is a surface (lateral) device whose breakdown characteristic is limited only by bulk junction avalanching and horizontal topology (channel length). Breakdown ratings are governed by doping levels and surface area, which is an economic consideration, instead of a physical limitation. Unlike NPN transistors,

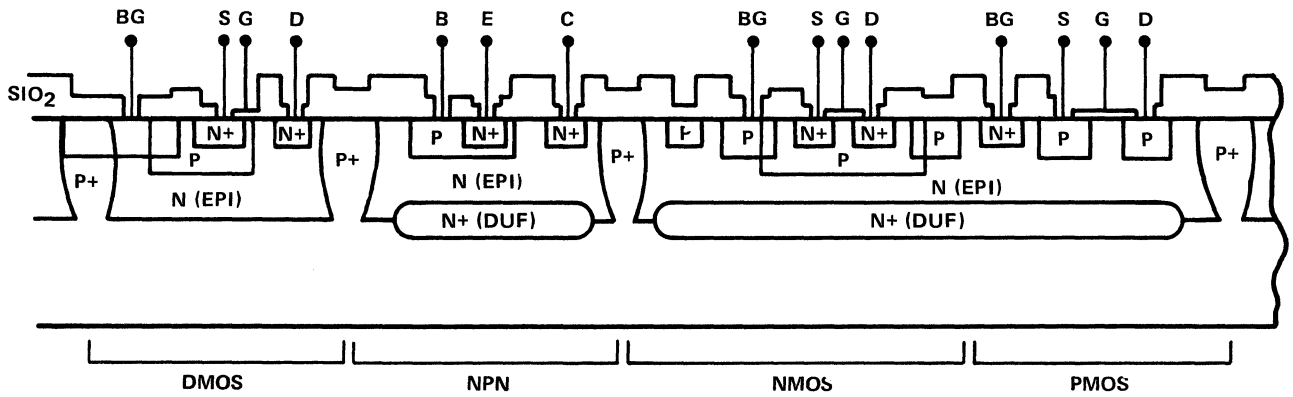


Figure 8-1. BIDFET Cell Cross Section

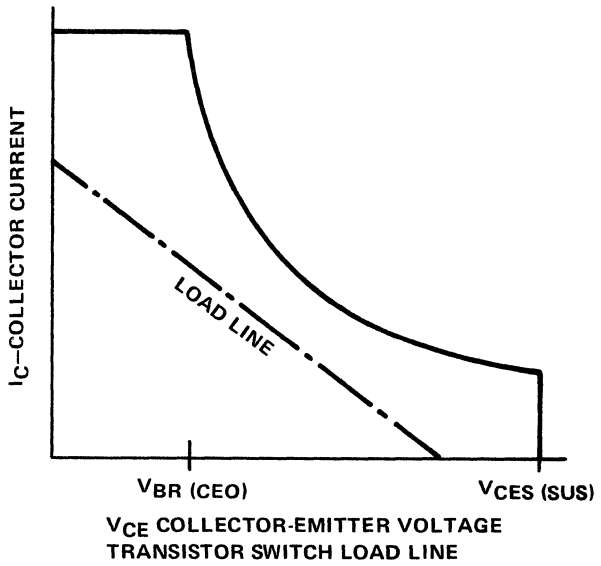


Figure 8-2. RBSOA Curve and Load Line

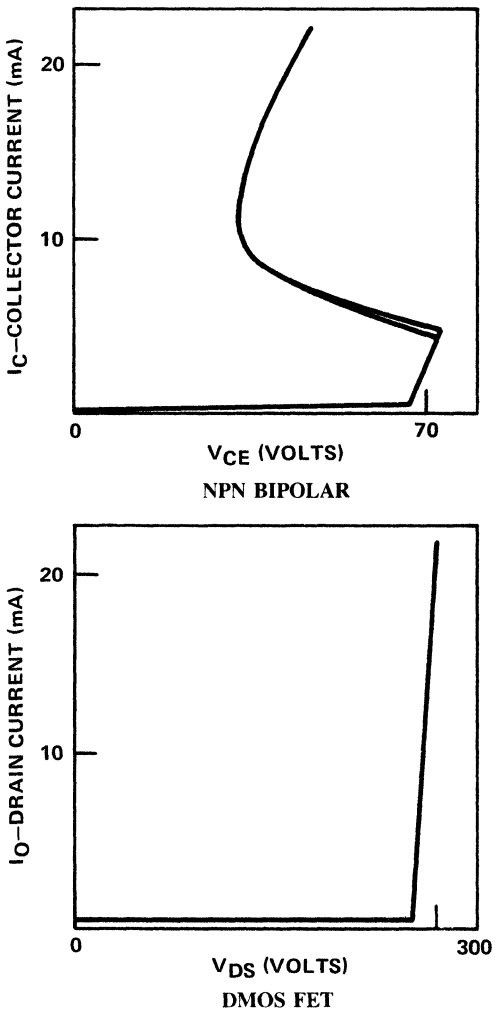


Figure 8-3. Breakdown Characteristics

DMOS can operate safely to its breakdown voltage limit without risk of destructive secondary breakdown or sacrifice of reliability. Figure 8-3 shows the superior breakdown characteristics of the DMOS structure as compared to the bipolar structure.

Characteristic waveforms (Figure 8-4) show the virtual independence of the output current to the output voltage of a DMOS structure. The Early voltage, as well as the stored charge characteristics of the DMOS structure, is superior to that of the bipolar transistor in switching applications.

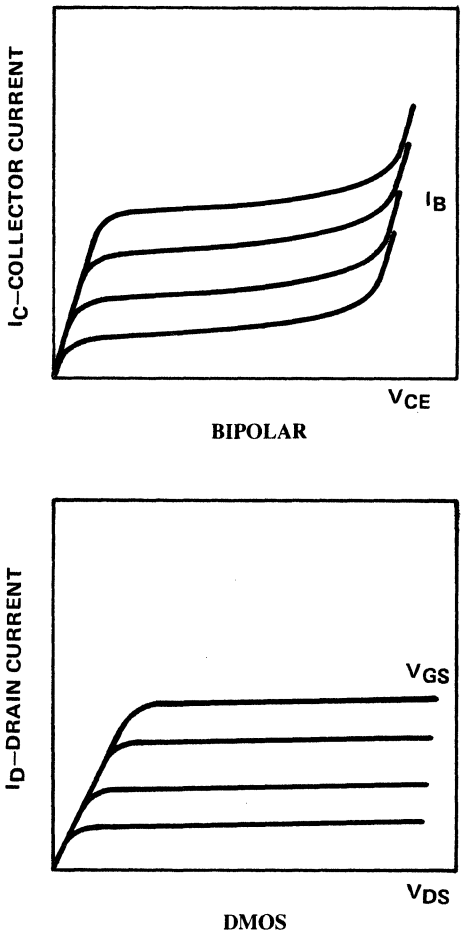


Figure 8-4. Characteristic Waveforms

Using the variety of structures offered by the BIDFET process, design engineers can optimize high voltage circuits by partitioning them and using the optimum technologies for the various sections. The bipolar structure offers durability and is very forgiving of input conditions. CMOS allows increased circuit complexity while requiring minimal power consumption and bar area. The DMOS structure's benefits have been presented herein. The result is a high-voltage interface circuit which is capable of performing data registration, manipulation or decoding functions to reduce the requirements on system electronics.

LED DISPLAY DRIVERS

LED displays have generally been fairly simple systems. Applications vary from one or two discrete LEDs to small arrays and digital displays. A variety of multichannel drivers have evolved that allow easy implementation of the drives required. Some examples of these devices follow:

SN75491 AND SN75491A QUAD LED SEGMENT DRIVERS (Figure 8-5)

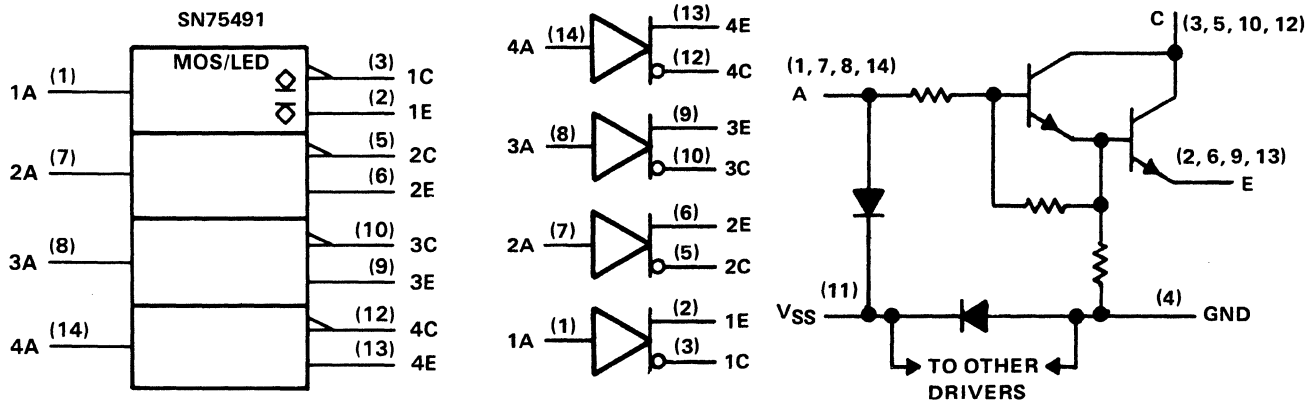
Features

- 50 mA source or sink capability
- '491 rated for 10 V operation
- '491A rated for 20 V operation
- MOS compatible inputs
- Low standby power
- High gain Darlington circuits

SN75492 AND SN75492A HEX LED DIGIT DRIVERS (Figure 8-6)

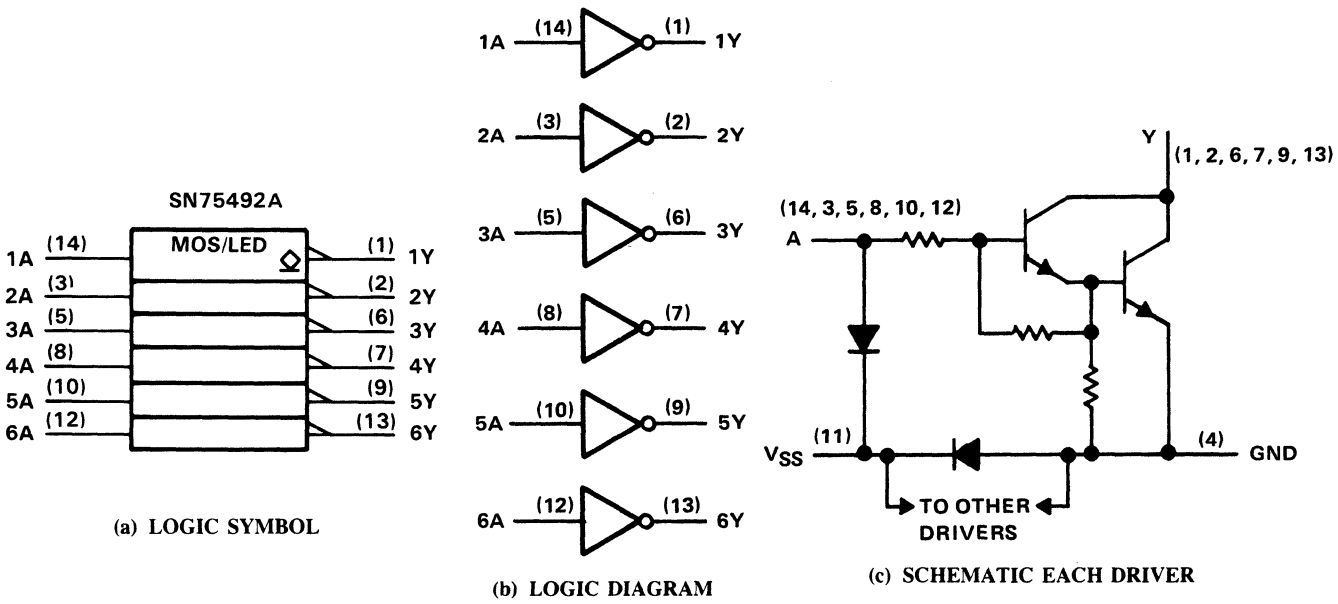
Features

- 250 mA sink capability
- '492 rated for 10 V operation
- '492A rated for 20 V operation
- MOS compatible inputs
- Low standby power
- High-gain Darlington circuits



(a) LOGIC SYMBOL (b) LOGIC DIAGRAM (c) SCHEMATIC EACH DRIVER

Figure 8-5. SN75491 and SN75491A



(a) LOGIC SYMBOL (b) LOGIC DIAGRAM (c) SCHEMATIC EACH DRIVER

Figure 8-6. SN75492 and SN75492A

SN75494 HEX LED DIGIT DRIVER

The SN75494 (Figure 8-7) provides the same basic function as the SN75492 but with some key differences:

- Operates from lower V_{CC} voltages; as low as 3.2 V.
- In addition to V_{SS} and ground the '494 provides access to predriver collectors via its V_{CC} pin thus allowing good saturation of output transistors for low-voltage applications.
- An enable input is provided to allow display blanking.

SN75497 7-CHANNEL and SN75498 9-CHANNEL LED DRIVERS (Figure 8-8)

Features:

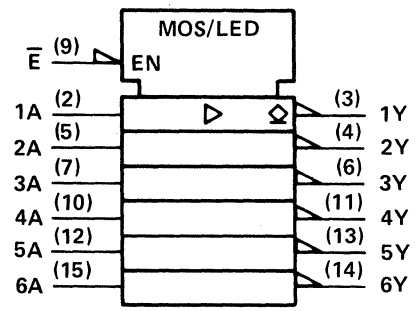
- 100 mA output sink capability
- Low-voltage operation (2.7 V min)
- MOS and TTL compatible inputs
- Low standby power

DRIVING LED DISPLAYS

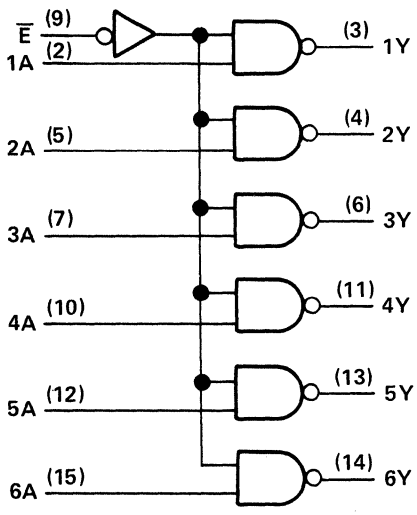
Light emitting diodes exist in a variety of sizes and operating current requirements. Typical digital displays require 10 to 20 mA forward current for normal operating brightness levels.

Digital displays are usually driven using time-multiplex techniques to minimize the number of drivers required. A segment-address selection and digit-scan method of multiplexing is used in the application (Figure 8-9) for a 12-digit display.

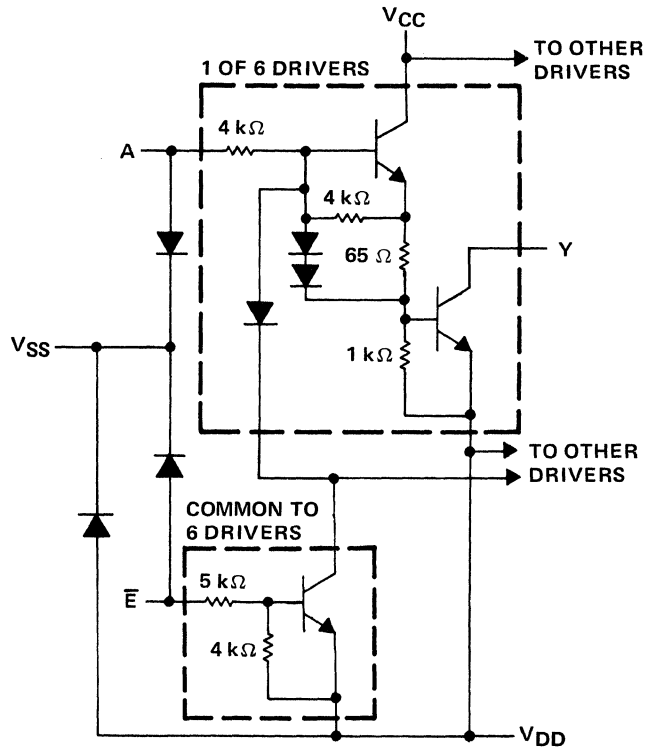
The TIL804 used in this application is a 12-digit numeric LED display with right-hand decimal points. It consists of common-cathode red LED digits. Twenty tab connections allow control of the 84 segments and 12 decimal points. The segments, and decimal points, are addressed by the "0" outputs of a TMS1200 microcomputer chip. Each digit of the display is connected in a common-cathode configuration and the anodes of like-position segments of all digits are connected together for multiplex drive. Normal operation of each digit is 8.3% (1/12) duty cycle. For an average



(a) LOGIC SYMBOL



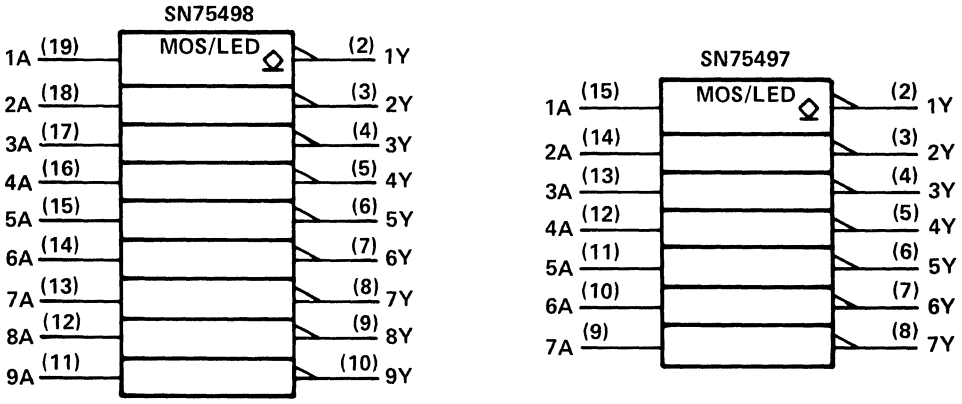
(b) LOGIC DIAGRAM



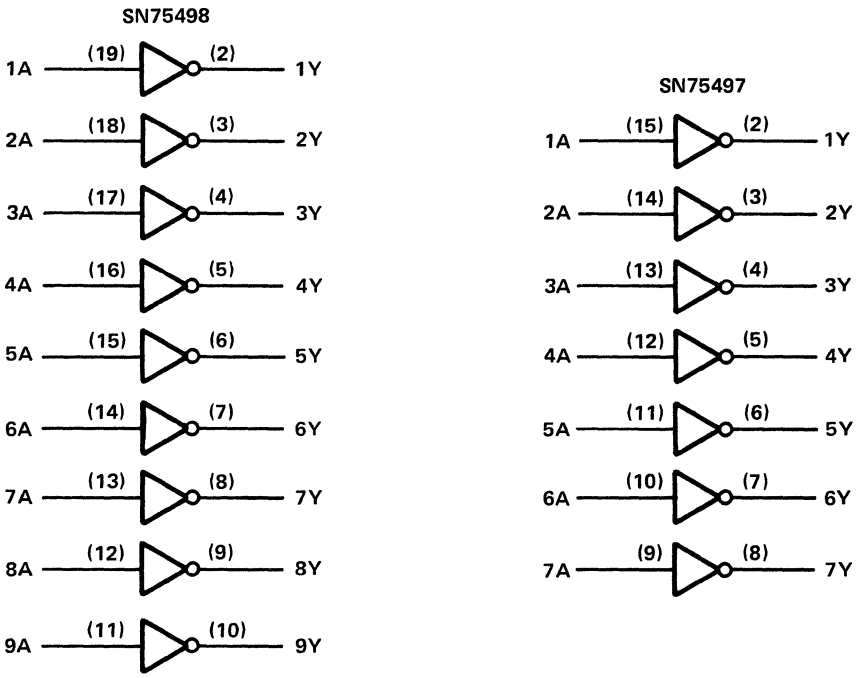
NOTES: 1. THE V_{SS} TERMINAL MUST BE CONNECTED TO THE MOST POSITIVE VOLTAGE THAT IS APPLIED TO THE DEVICE.
2. RESISTOR VALUES SHOWN ARE NOMINAL AND IN OHMS.

(c) SCHEMATIC EACH DRIVER

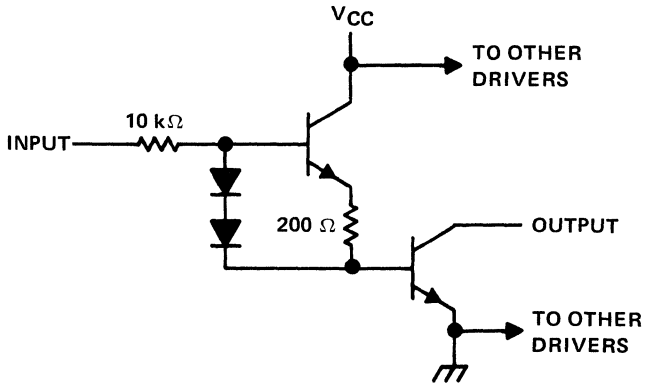
Figure 8-7. SN75494



(a) LOGIC SYMBOLS



(b) LOGIC DIAGRAMS



(c) SCHEMATIC EACH DRIVER

Figure 8-8. SN75497 and SN75498

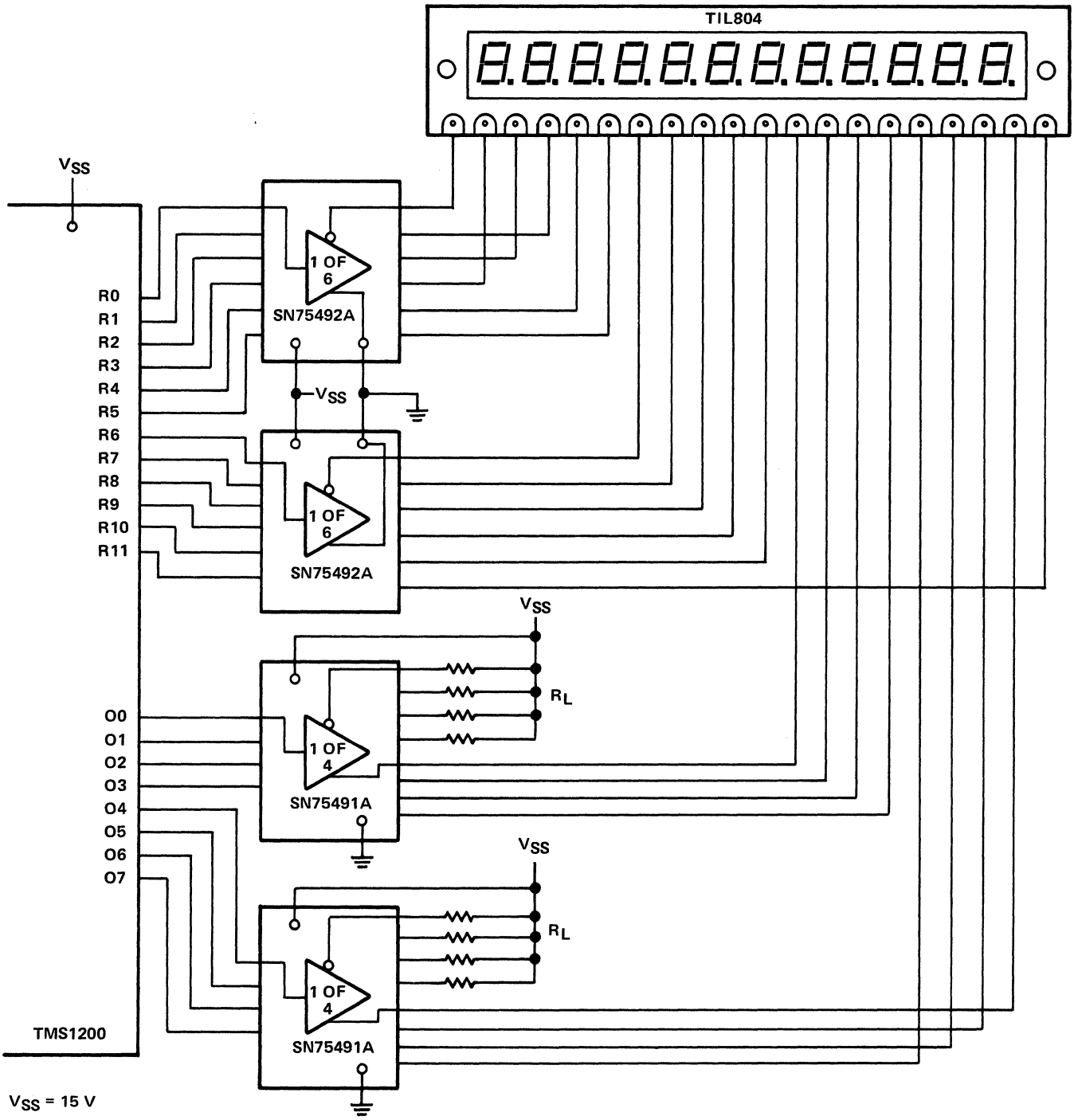


Figure 8-9. 12-Digit LED Numeric Display and Drive

forward current of 5 mA a pulse current of 60 mA will be required. System operation may be from a single 15 V supply as shown, or the SN75491A source drivers may be operated from a separate supply of typically 5 V. The current limit resistors, R_L may be calculated as follows:

$$R_L = \frac{V_{SS} - V_{CE(ON)(SN75491A)} - V_{OL(SN75492A)} - V_{F(LED)}}{I_{FM(LED)}}$$

Typical Parameters

V_{SS} = 12 V
$V_{CE(ON)}$ = 1.2 V
V_{OL} = 1.2 V
V_F = 1.7 V
I_{FM} = 60 mA
R_L = 130 Ω

OTHER APPLICATIONS

Although the multichannel drivers shown here were designed specifically for driving light emitting diodes, they are basically Darlington transistor drivers and as such they have many other uses. The circuits shown in Figure 8-10 through 8-17 are examples of the variety of applications that may be implemented with these devices.

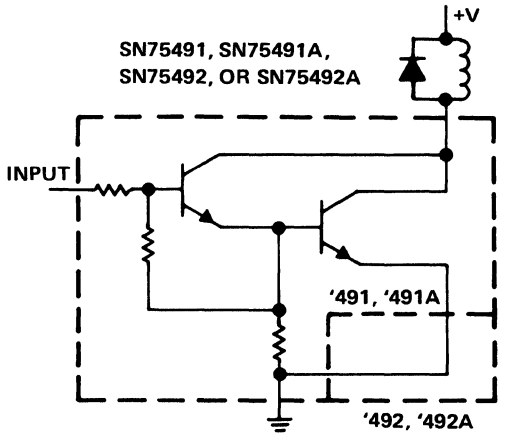


Figure 8-10. Quad or Hex Relay Driver

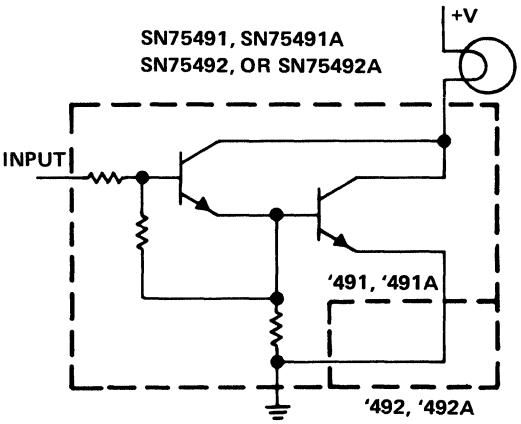


Figure 8-11. Quad or Hex Lamp Driver

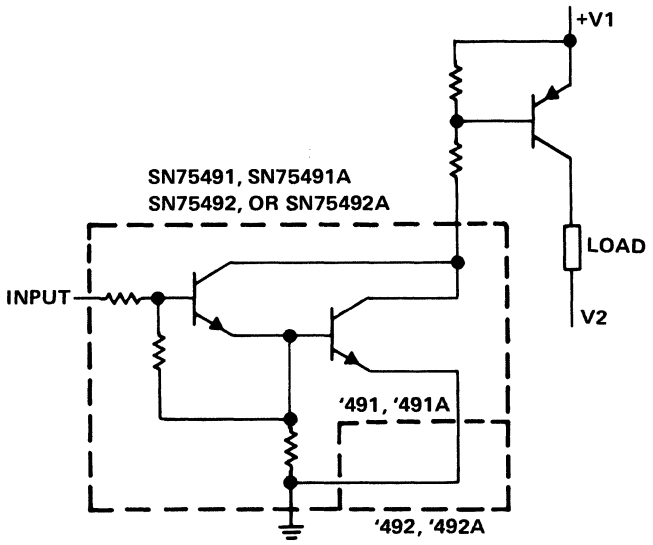


Figure 8-12. Quad or Hex High-Current P-N-P Transistor Driver

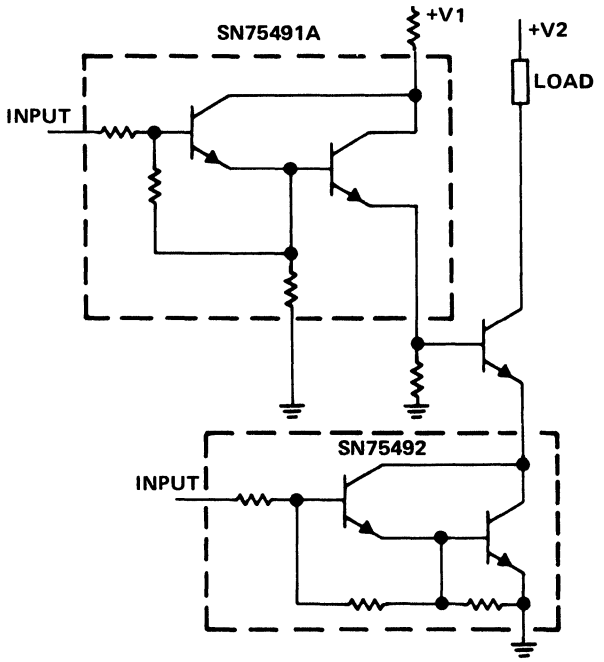


Figure 8-13. Base/Emitter Select N-P-N Transistor

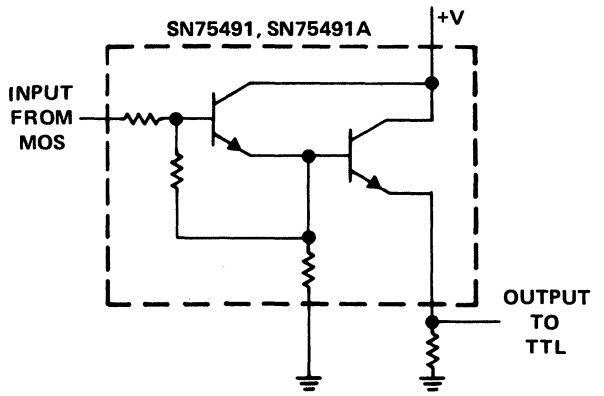


Figure 8-14. MOS to TTL Level Shifter

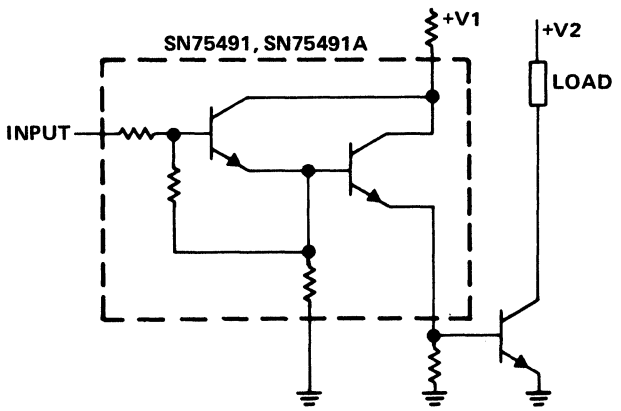


Figure 8-15. Quad High-Current N-P-N Transistor Driver

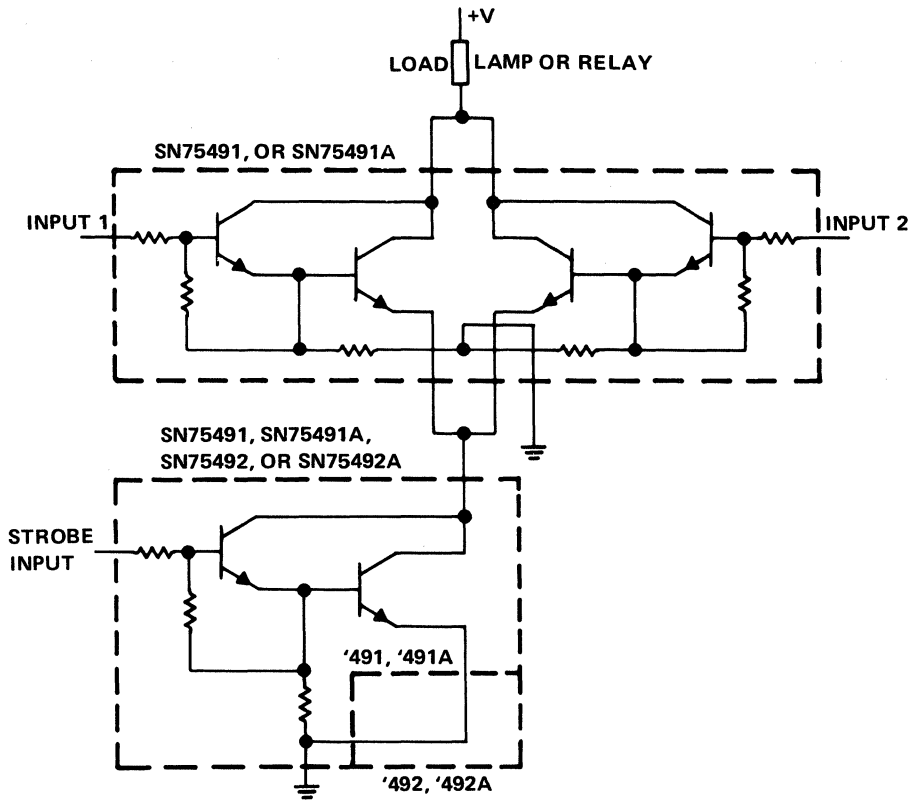


Figure 8-16. Strobed NOR Driver

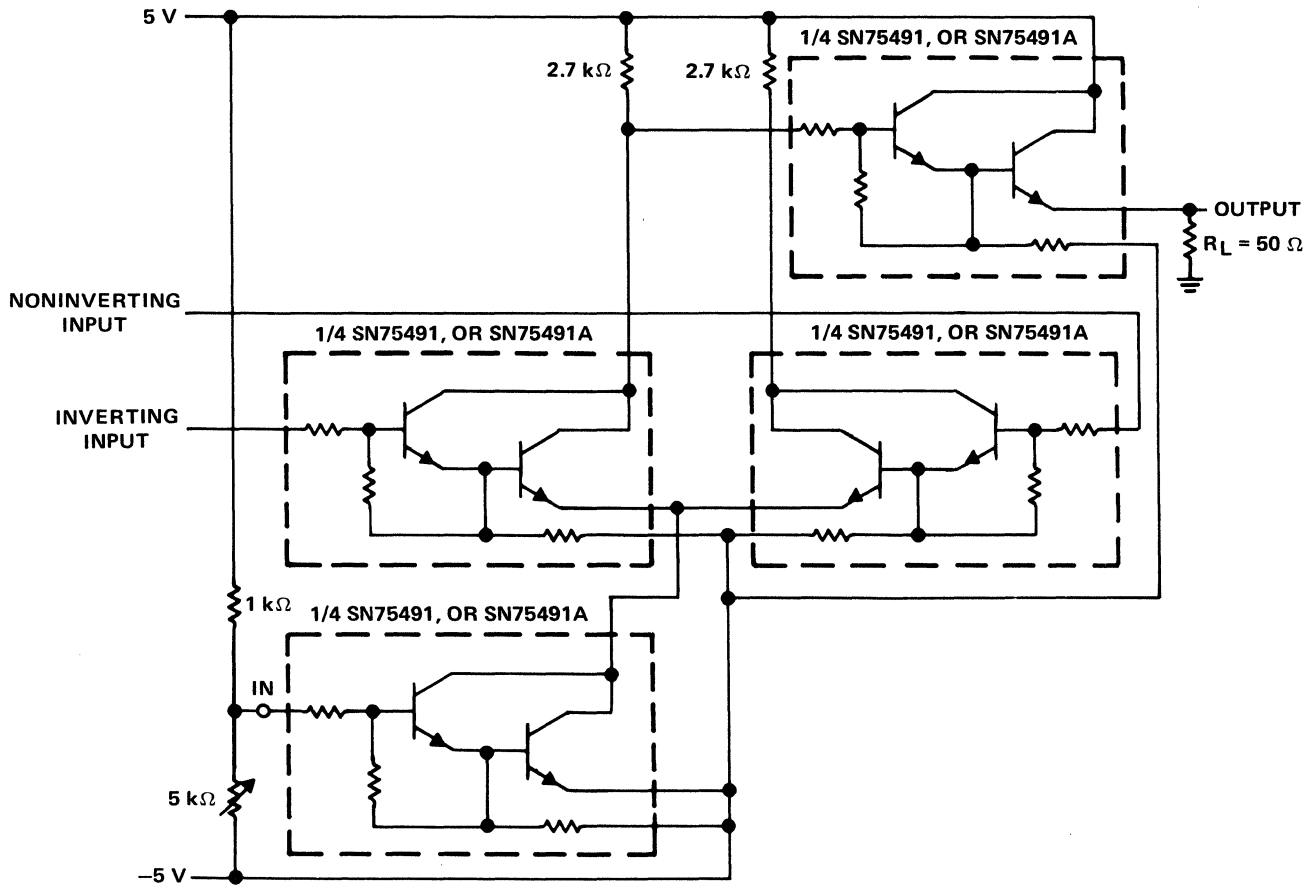
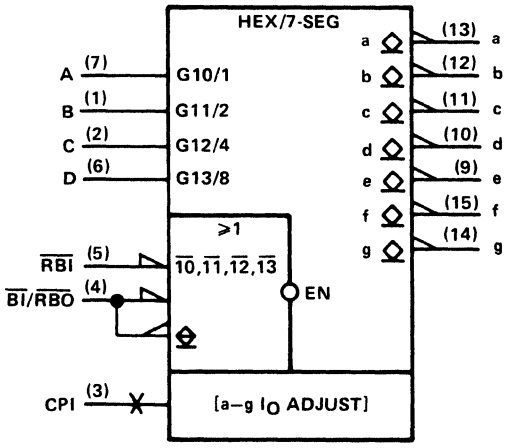


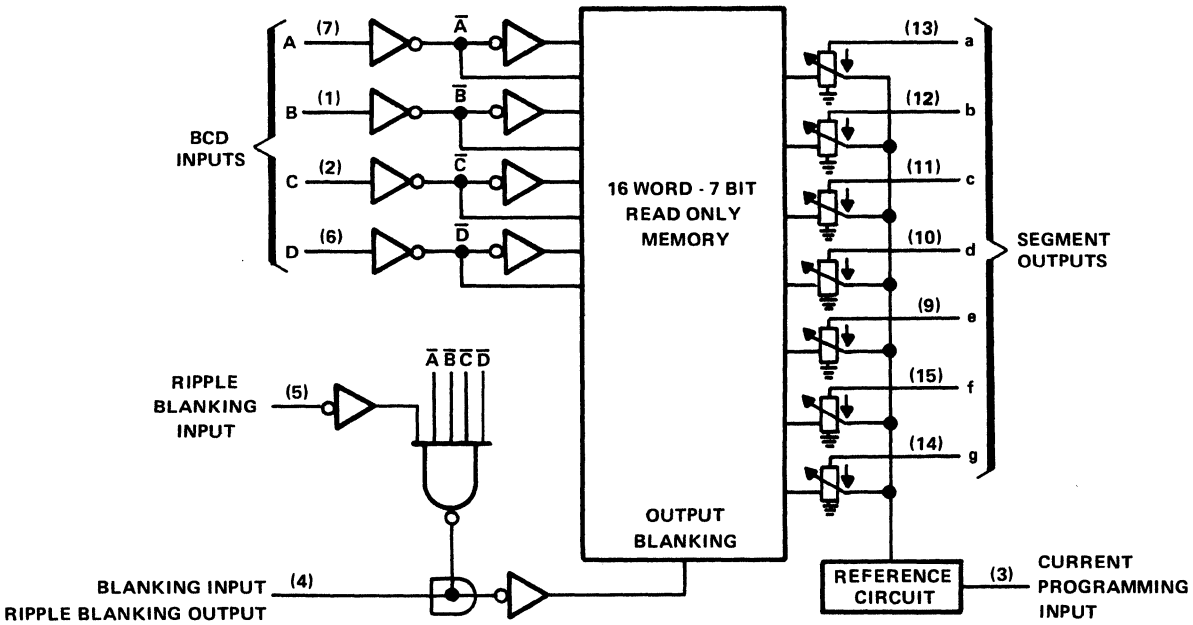
Figure 8-17. SN75491/SN75491A Used as an Interface Circuit Between the Balanced 30-MHz Output of an RF Amplifier and a Coaxial Cable

DC PLASMA DISPLAY DRIVERS

DC plasma has been popular for many years as the media for digital displays. DC plasma provides a relatively bright display ideal for panel meters and various types of test equipment. Numerical 7-segment displays are used in most cases, and therefore the display drivers for dc plasma are configured specifically for this application. DC plasma displays require a rather high voltage to fire (ionize) the gas and maintain conduction. Firing voltages are generally in excess of 100 V and operating current levels are from 0.2 mA to 3 or 4 mA depending on the display's physical size and the brightness required. Multiplexing may be used in some applications to minimize the number of parts required.



(a) LOGIC SYMBOL

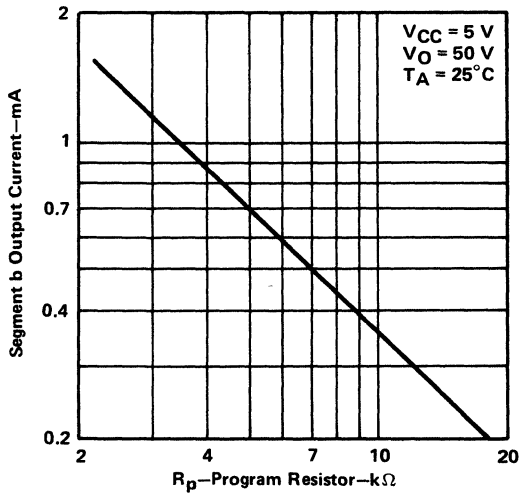


(b) LOGIC DIAGRAM

SN75480 DC PLASMA DRIVER

The SN75480 (Figure 8-18) is a bipolar high-voltage 7-segment decoder/cathode driver for dc plasma displays. Off-state output voltage capability is 80 V minimum. It is designed to decode four lines of hexadecimal input and drive a seven-segment Panaplex II* type gas-filled (dc plasma) display tube. The SN75480 employs a 112 bit read only memory to provide input decoding and output segment on or off control in accordance with the function table (Figure 8-19).

Segment drive outputs are constant-current sinks with adjustable operating levels. The current sink level is adjustable by connecting an external program resistor (R_p) from V_{CC} to the current programming input in accordance with the curve shown in Figure 8-18(c). Output current may be adjusted from nominally 0.2 mA up to 1.5 mA in order to drive various tube types and permit multiplex operation.

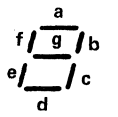


(c) SEGMENT OUTPUT CURRENT vs PROGRAMMING RESISTOR

Figure 8-18. SN75480 DC Plasma Driver

*Trademark of Burroughs Corporation

Output sink currents for other segments are proportional to the b-segment current to provide even illumination of all segments. Each sink output (Figure 8-18) is regulated to ensure a constant brightness level across the display even with fluctuating supply voltages. Typical on-state currents are within 1% for voltage changes from 3 to 50 V. Off-state voltages can vary from 3 to 80 V. The blanking input (pin 4) provides unconditional blanking of all outputs, while the A through D inputs (pins 1, 2, 6 and 7) and the ripple blanking input (pin 5) into the blanking circuit, allow simple leading or trailing zero blanking.



SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	INPUTS					BI/RBO	SEGMENT OUTPUTS							DISPLAY
	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	0
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	2
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	3
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	4
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	5
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	6
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	7
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	8
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	9
10	X	H	L	H	L	H	ON	ON	ON	OFF	ON	ON	ON	A
11	X	H	L	H	H	H	OFF	OFF	ON	ON	ON	ON	ON	b
12	X	H	H	L	L	H	ON	OFF	OFF	ON	ON	ON	OFF	C
13	X	H	H	L	H	H	OFF	ON	ON	ON	ON	OFF	ON	d
14	X	H	H	H	L	H	ON	OFF	OFF	ON	ON	ON	ON	E
15	X	H	H	H	H	H	ON	OFF	OFF	OFF	ON	ON	ON	F
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
RBI	L	L	L	L	L	L†	OFF	OFF	OFF	OFF	OFF	OFF	OFF	

H = high level, L = low level, X = irrelevant

†BI/RBO is wired AND logic serving as a blanking input (BI) and/or ripple-blanking output (RBO). When RBI and inputs A, B, C, and D are all low, all segment outputs go off and RBO goes to a low-level (response condition).

Figure 8-19. SN75480 Function Table

SN75480 Application

In the basic application circuit, Figure 8-20, a serial count from a controller or microprocessor is fed to the "A" input of an SN7493A binary counter. The SN7493A output is a BCD representation of the decimal number to be displayed. To hold the last input until time for an update, an SN7475 4-bit latch is used. The BCD input is decoded by the SN75480 to provide proper segment drive resulting in a displayed hexadecimal value in accordance with the function table (Figure 8-19).

SN75581 GAS DISCHARGE SOURCE DRIVER

The SN75581 (Figure 8-21) is a high-voltage (150 V), 7-channel, source output monolithic BIDFET integrated circuit designed to drive a dot matrix or segmented display. Its output characteristics make this driver compatible to several display types including vacuum fluorescent and dc plasma displays.

All device inputs are diode-clamped pnp inputs and, when left open, assume a high logic level. The nominal input threshold is 1.5 V. Outputs are open source DMOS transistors for excellent high voltage characteristics and reliability.

The device consists of a 7-bit shift register, seven latches, and seven output AND gates. Serial data is entered into the shift register on the low-to-high transition of the Clock input. When the Latch Enable input is high, data is transferred from the shift registers to the latch outputs. When Latch Enable makes a high-to-low transition, the shift register is cleared. Taking the Output Enable input high enables all outputs simultaneously. The Serial Output is not affected by the Output Enable input. See Figures 8-22 and 8-23.

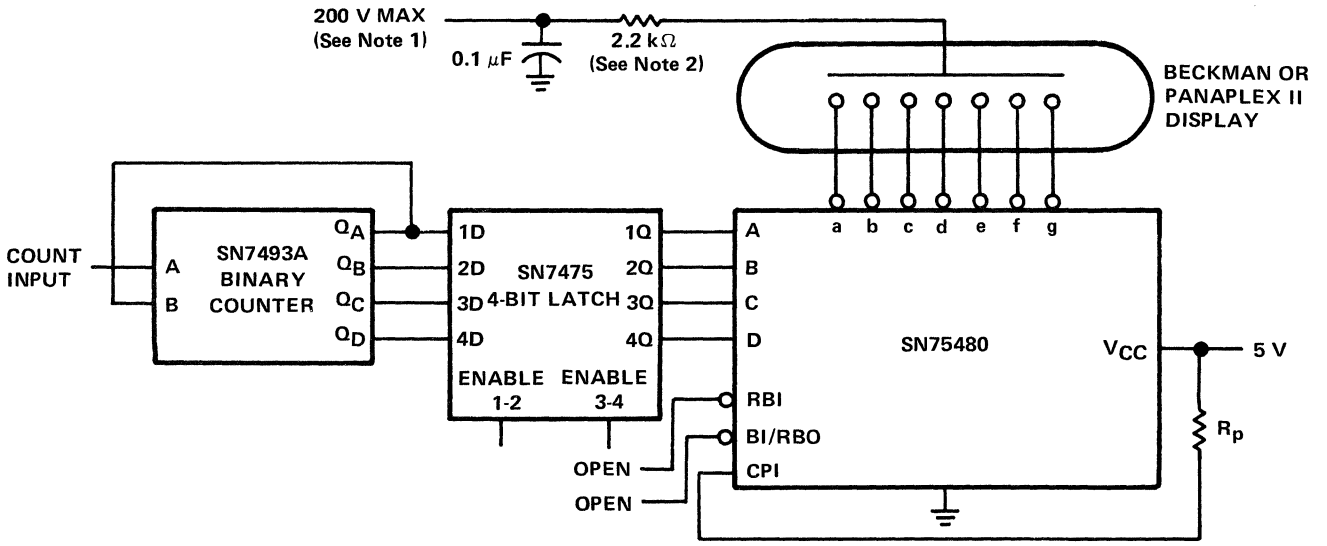
SN75581 Application

A typical SN75581 gas discharge display driver application is shown in Figure 8-23. Serial data is clocked into the SN75581 under microprocessor control. When the latch enable input is high, the data is transferred from input shift registers to the latches. The latches store the data until output enable goes high, which enables all outputs (pins 9 through 16). The outputs are connected to a seven segment display (a through g). Individual segments (a through g) will fire if a data bit turns on the corresponding DMOS output transistor connected to that segment. Serial output is not utilized.

SN75584A HIGH-VOLTAGE 7-SEGMENT LATCH/DECODER/CATHODE DRIVER

The SN75584A is a BIDFET integrated circuit and has high voltage DMOS outputs. The SN75584A (Figure 8-24) is designed to decode four lines of BCD data and drive a seven segment (plus decimal point) gas display tube such as the Beckman and Panaplex II displays. Latches are provided to store the four data and decimal point inputs while the enable input is at a low logic level voltage.

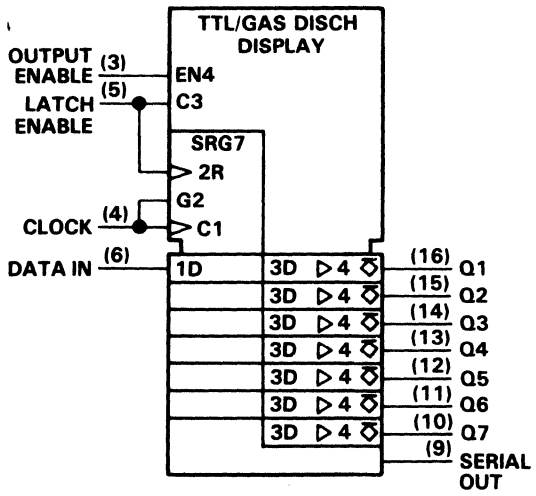
This circuit employs a read only memory to provide output decoding for the BCD input digits 0 to 9. For input data codes greater than 9, the segment outputs are blanked. Each sink output is a constant current, regulated to ensure uniform brightness of the display even with fluctuating supply voltage. On-state output current is essentially constant over the output voltage range of 4 V to 100 V. Each current sink is normalized to the "b" segment output current as required for even illumination of all segments. Output currents may be varied from 0.1 mA to 4 mA for driving various displays.



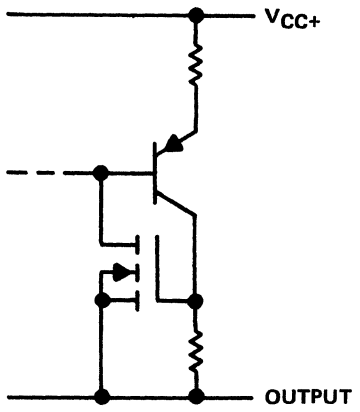
NOTES: 1. This voltage will be different for different displays. It must be set to ensure that the on-state and off-state voltages do not exceed 55 V and 80 V at the SN75480.

2. In all applications peak transient segment current must be limited to 50 mA. This may be accomplished by connecting a 2.2 kΩ resistor as shown or current limiting in an anode driver in multiplex applications.

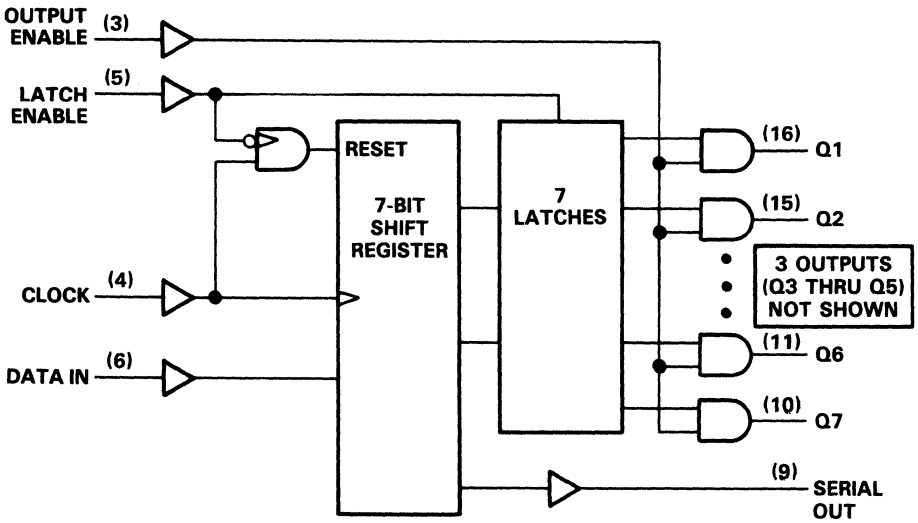
Figure 8-20. Basic Digital Display Drive



(a) LOGIC SYMBOL



(b) SCHEMATIC (EACH DRIVER) OUTPUT



(c) LOGIC DIAGRAM (POSITIVE LOGIC)

Figure 8-21. SN75581 Gas Discharge Driver

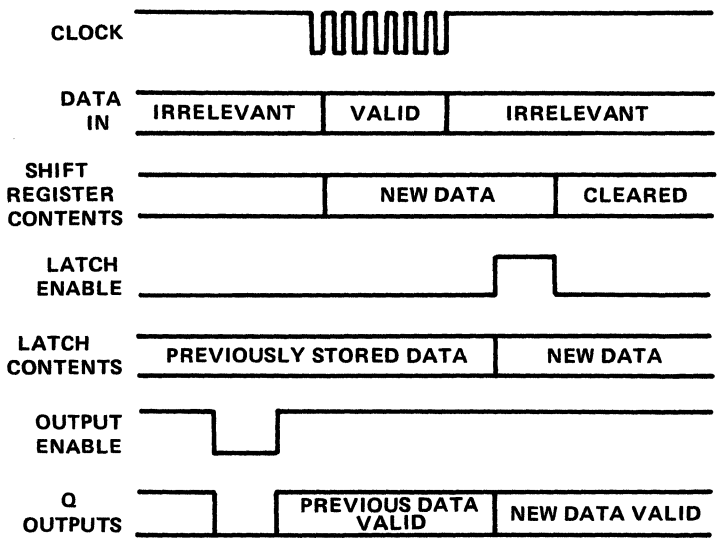


Figure 8-22. SN75581 Typical Operating Sequence

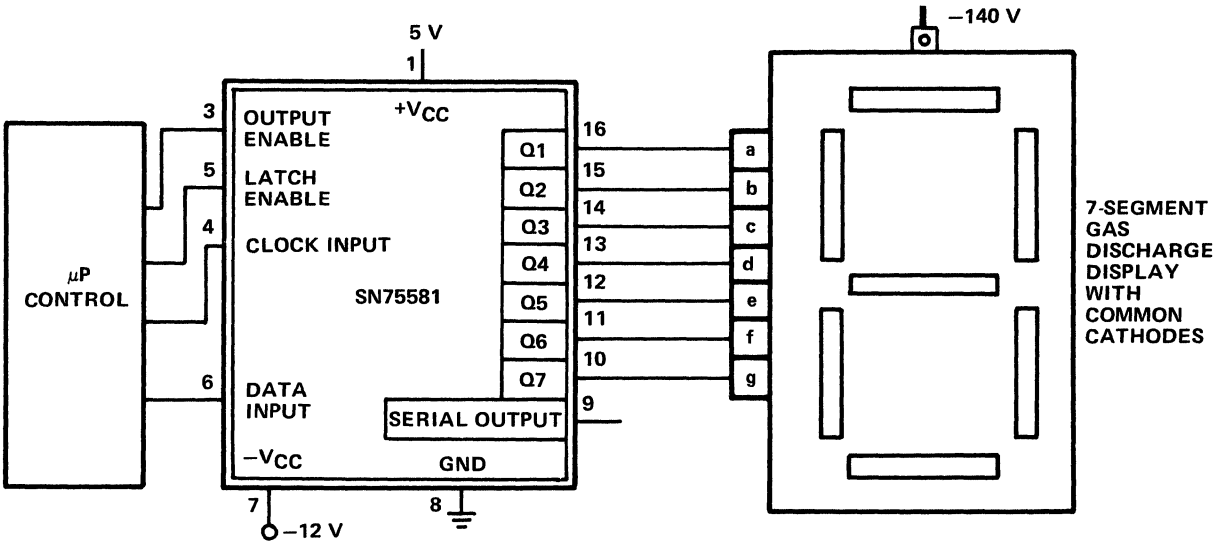
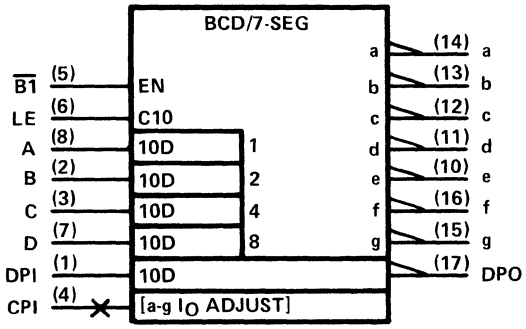
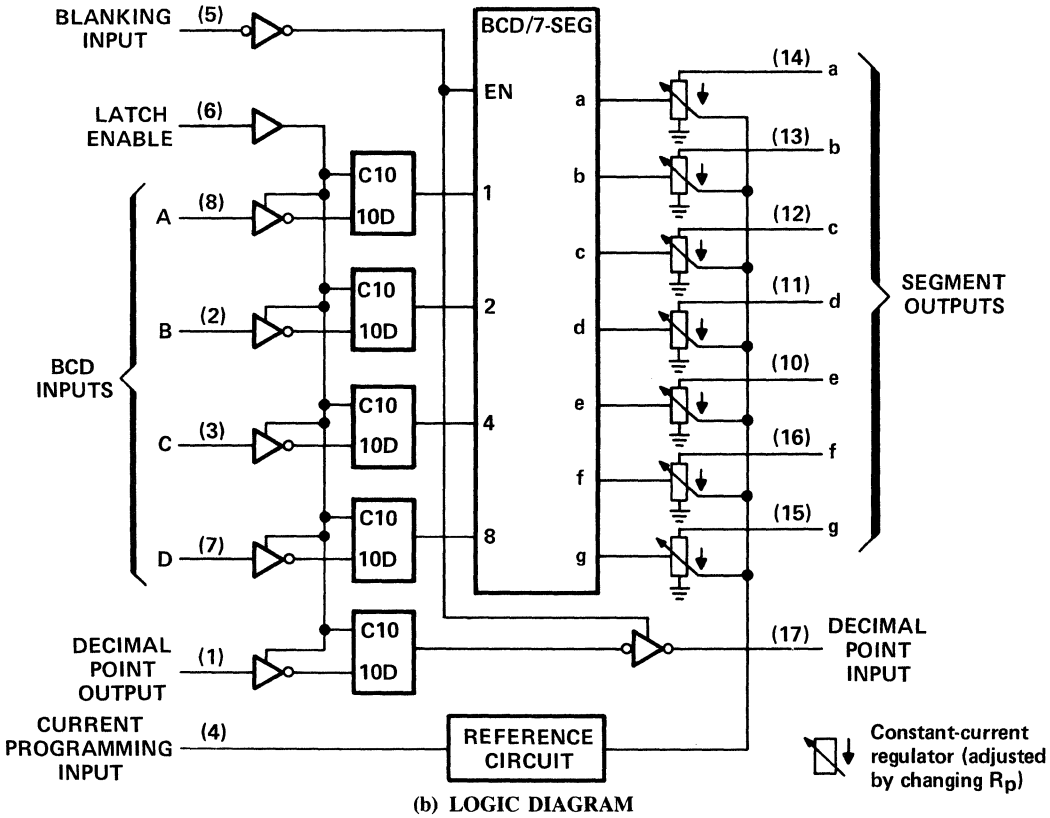


Figure 8-23. Typical SN75581 Application



(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM

Figure 8-24. SN75584A DC Plasma Segment Driver

The output current is adjusted by connecting an external programming resistor (R_p) from the current programming input to ground. Figure 8-25 shows the "b" segment output current versus programming resistance. $I_{O(b)}$ in mA = $3.616/R_p$ in kΩ. The blanking input provides unconditional blanking of all segment outputs including the decimal point output. The enable input allows data to be stored internally while input data is changing. When enable is at a high level voltage, the outputs will reflect conditions on the A, B, C, D, and DP inputs in accordance with the function table in Figure 8-26. A transition from a high level voltage to a low level voltage at enable will cause the input data set up prior to the transition to be latched. In the latched state, the A, B, C, D, and DP inputs are in a high-impedance state to minimize input loading.

Thermal protection circuitry will blank the display, regardless of input conditions, whenever junction temperature exceeds approximately 150°C.

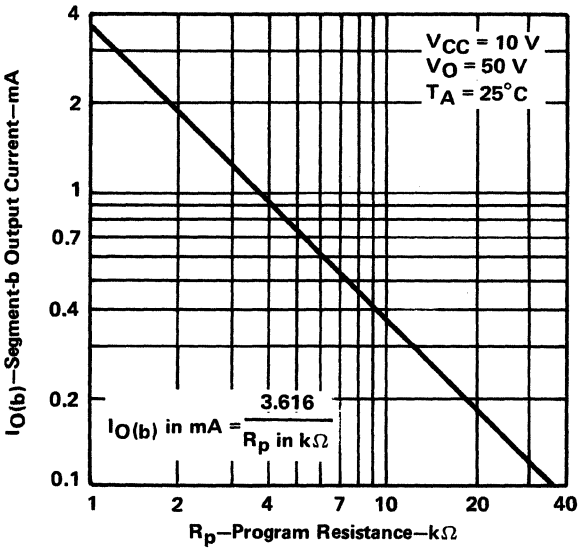


Figure 8-25. SN75584A Segment Output Current vs Program Resistance

SEGMENT IDENTIFICATION

DECIMAL OR FUNCTION	DP INPUT†	BCD INPUTS†				BI	SEGMENT OUTPUTS							DP OUT-PUT	DISPLAY
		D	C	B	A		a	b	c	d	e	f	g		
0	X	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	X	
1	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	X	
2	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	X	
3	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	X	
4	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	X	
5	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	X	
6	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	X	
7	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	X	
8	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	X	
9	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	X	
10	X	H	L	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
11	X	H	L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
12	X	H	H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
13	X	H	H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
14	X	H	H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
15	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	X	
BI	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
DP	H	X	X	X	X	H	X	X	X	X	X	X	X	ON	
DP	L	X	X	X	X	H	X	X	X	X	X	X	X	OFF	

H = high level, L = low level, X = irrelevant

†Table is valid for the indicated BCD and decimal point inputs while enable is high. See description.

Figure 8-26. SN75584A Function Table

SN75584A Application

A basic circuit (Figure 8-27) that automatically counts 0 through 9, resets and counts through again is used to demonstrate the SN75584A's ease of operation and drive capabilities.

The display is a 3-digit display with decimal points requiring a 180 V supply and typical segment operating currents of 1 mA.

The TLC555 provides clock pulses at about 1.6 Hz to an SN7493A 4-bit binary counter which in turn drives the A, B, C and D inputs of the SN75584A display driver in accordance with its count sequence. Sequencing through the binary input codes results in the output segment drivers cycling from 0 through 9. For all input codes over 9 all segment outputs are blanked off. Thus the display will be blanked off for about four seconds before the count sequence

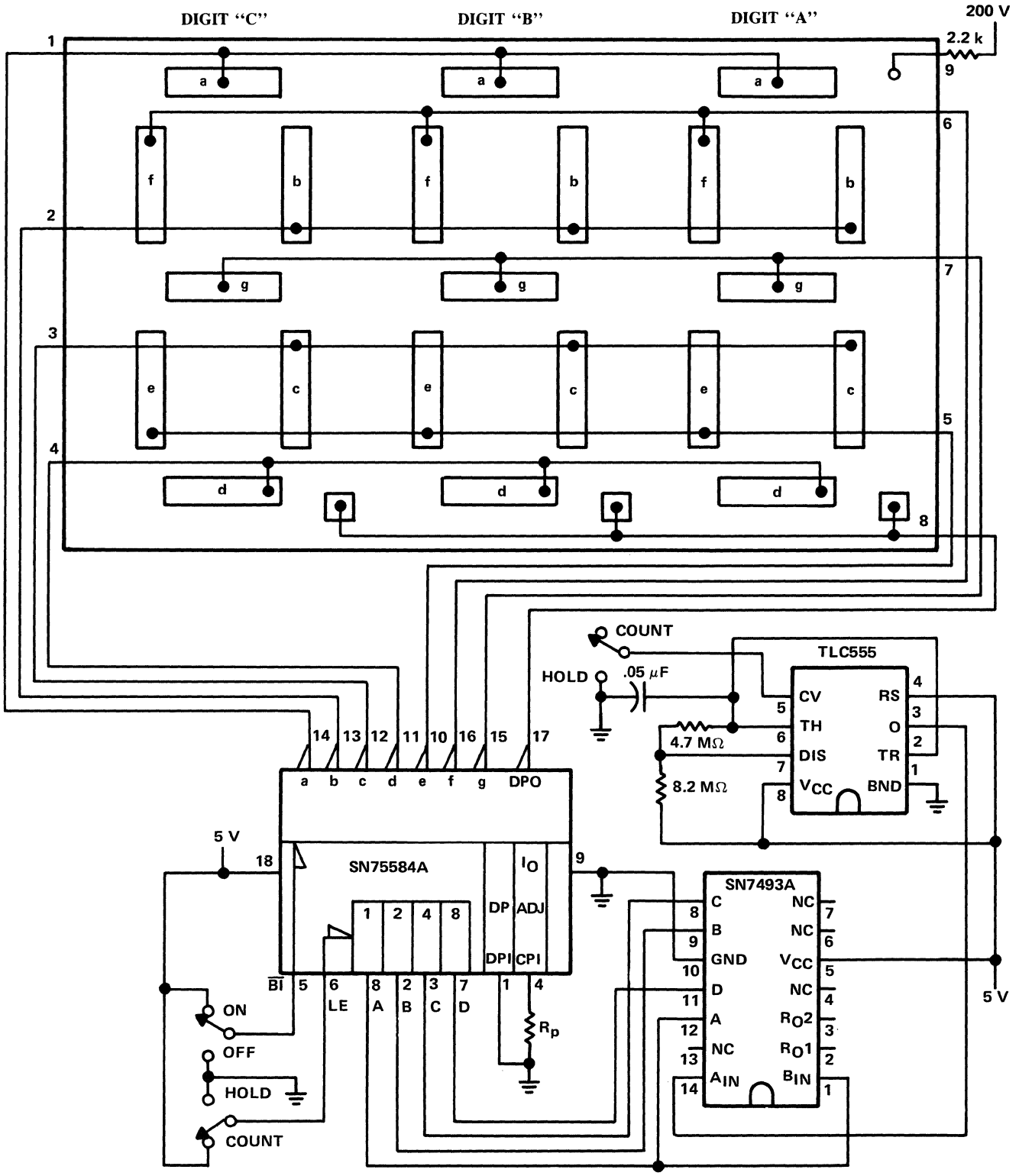


Figure 8-27. Three-Digit Display Driver Application

starts over with zero. Blanking of all output drives (including decimal point) is accomplished by switching pin 5, the blanking input, to ground. If the latch enable input, pin 6, is connected to 5 V the SN75584A continues to sequence. Switching the latch enable to ground prevents further transferring of data to the 584A outputs and the segment outputs are held (latched) in the mode they were in just prior to switching. Setting pin 6 high again allows data present in the 584A memory to again control the outputs. The driver output may also be held by simply stopping the clock. This is accomplished by switching pin 5, control voltage input, of the TLC555 to ground. In this application, pin 4 of the SN75584A, (the current programming input) is connected through a 3.3 kΩ resistor to ground allowing about 1 mA of segment drive current. The decimal point input, pin 1, is grounded which leaves the decimal point on at all times except when blanked. A TTL logic high level at pin 1 could turn off the decimal point output.

AC PLASMA DISPLAY DRIVERS

The persistent interest in flat panel information displays has stimulated development of the gas discharge display. Their safety, thinness, durability, and compact screen size have been the primary advantages over conventional display technologies. The following sections discuss ac plasma gas discharge displays and display drivers.

AC PLASMA DISPLAY TECHNOLOGY

The ac plasma display is an X-Y matrix gas discharge display. The basic display element is the gas discharge that occurs at the intersection of selected electrodes when the applied voltage between the electrodes exceeds the breakdown voltage of the media gas with which the display is filled. When the breakdown voltage of the gas is exceeded, the gas is ionized and the discharge that occurs emits a visible spot of light at the intersection of the selected electrodes. Once initiated, the display element can be maintained active without further selective control. The data retention property of the ac plasma display eliminates the necessity of a memory map for simple information displays.

Construction

The simple construction techniques employed are another feature encouraging the development of the ac plasma display panel. The panel envelope is essentially two flat pieces of ordinary glass spaced apart and sealed around the peripheral edges as shown in Figure 8-28.

The electrodes are deposited on the internal surfaces of the glass plates and then covered by an insulating dielectric layer prior to their joining. The space between the glass plates is evacuated and filled with a media gas under low pressure (approximately one-fifth atm.). Unlike the dc plasma display panel where the electrodes are immersed in the media gas, the electrodes of the ac plasma panel are isolated from the media gas by the dielectric layer. This dictates ac operation utilizing capacitive coupling to the insulated ac plasma display cell.

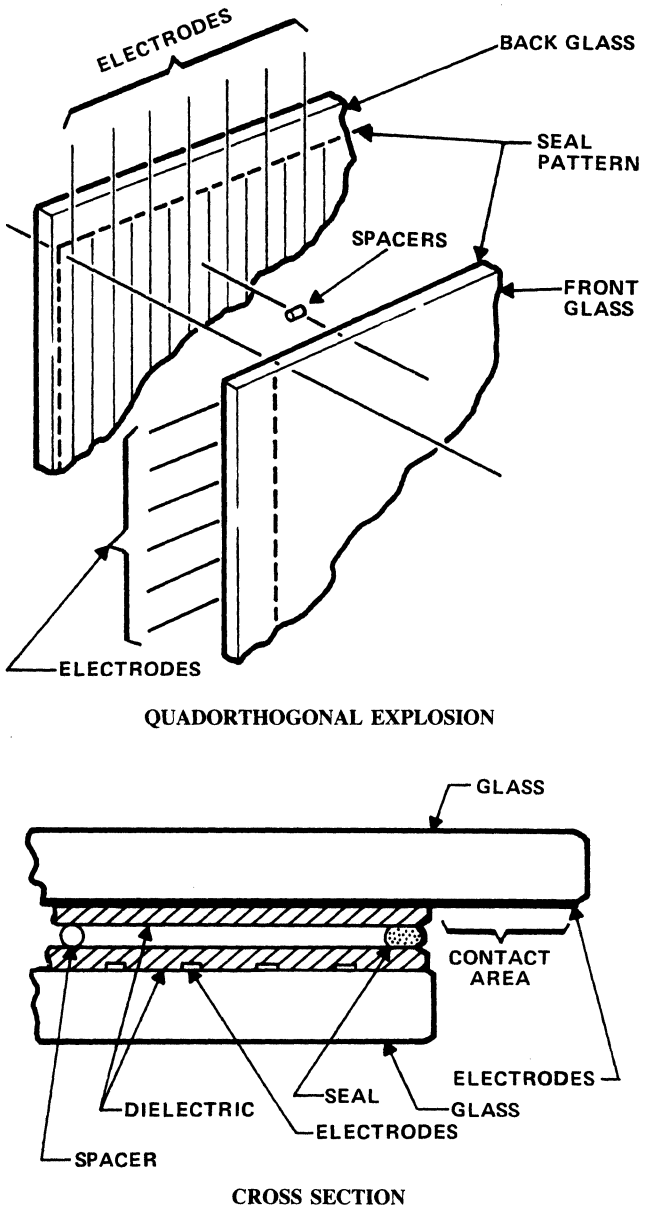


Figure 8-28. Panel Construction

Early panels utilized a third piece of perforated glass, which defined the individual display cell or pixel. Current panels, however, use an open-cell structure which eliminates the masking glass. Individual cells thus constructed are defined by properly ratioed media gas pressure, electrode width and resolution, glass spacing, and excitation and sustaining potentials. Individual cells are defined as the area located at the intersection of the mutually perpendicular electrodes of the front and back plates. The parallel electrodes of each plate of the panel are usually divided, every other electrode exiting from

opposing edges of the plate, to allow easier access for the mechanical interface required to connect the electrodes to the control circuitry. The simple construction of the ac plasma panel yields a rugged sandwich containing only a few cubic centimeters of inert gas. There is no danger of implosion as found with conventional vacuum tube displays, and no danger of contact with high voltages through the glass faceplate. In addition to the low cost of the ac plasma display panel, the construction techniques yield one of the safest display panels in today's marketplace.

The Functional Cell

Light is emitted from the ac plasma cell as a result of the energy release that occurs when the media gas is ionized. This is accomplished by simply applying sufficient potential across the cell to break down the media gas. Since the actual cell is only capacitively coupled to the electrode potential, the voltage waveform, frequency and amplitude are interdependent for reliable plasma display operation.

When ionization of the gas occurs, a charge buildup is created by the high-electron and ion currents present in the ionization discharge sequence. This charge buildup, or wall charge as it is commonly identified, plays an important role in the ability of the ac plasma panel to maintain display information without further selective control. Figure 8-29 shows a typical applied ac waveform and the wall charge waveforms of an active and extinguished cell. These relationships are observed at all cell locations during that period of time in which no panel information is being altered (written or erased). This is normally identified as the sustain mode.

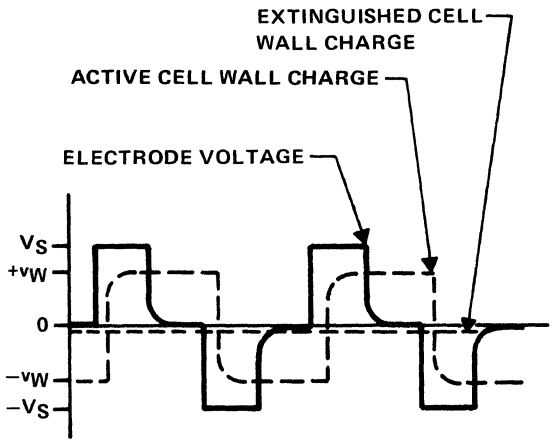


Figure 8-29. Cell Waveforms

A typical write-sustain cycle waveform is shown in Figure 8-30. The electrode potential and resulting wall charge are plotted to show their interdependence in writing (initializing) and sustaining a selected cell.

Prior to the cycle in which the selected cell will be written, the cell being exercised exhibits zero wall charge. Therefore, the potential seen by the cell (the cell voltage) is solely the potential applied to the electrodes (the electrode voltage). When the electrode voltage exceeds the breakdown voltage of the media gas, the gas ionizes and the wall charge is deposited such that its polarity opposes the applied cell voltage. Once created, the wall charge remains even after the ionization discharge extinguishes and the electrode potential decays to zero. In the next half-cycle, the electrode potential reverses, thus the wall charge that opposed the electrode voltage in the previous half-cycle now is additive. The cell voltage is therefore the sum of the wall voltage and the electrode voltage. This allows the electrode voltage to be reduced and still create a cell voltage of sufficient amplitude to cause the cell to fire. Stable operation exists when the sum of the electrode potential and wall charge create a cell voltage (V_{W2}) which is sufficient to create ample excess charge ($2\ V_W$) to cause the wall voltage to invert. Thus the cell can be maintained indefinitely by an alternating electrode potential which is actually less than the potential required to fire the cell. The ability to do this is attributed chiefly to the nonlinear charge transfer characteristics of the ac plasma cell, as illustrated in Figure 8-31. Since the sustaining electrode potential is less than the required firing potential of the extinguished cell, application of this voltage will have no effect on cells which have not been fired previously. With this in mind, operation of the ac plasma display is relatively simple. A background signal is applied to the entire display panel. This is usually called the sustain signal. Select circuitry superimposes the write pulse required to initially fire a cell on the X and Y-axis electrodes common to the cell to be written into. Once fired, the background signal will maintain the integrity of a cell until the cell is extinguished by another selective control signal, normally called the erase pulse. This is accomplished by application of a single pulse to the cell electrodes whose amplitude (V_{W1}) and duration are only sufficient to create enough excess charge to counterbalance the wall charge. Thus the wall charge is removed and the sustain chain sequence is broken. An illustration of this operation is shown in Figure 8-32.

Control Circuitry Implementation with the SN75500A and SN75501C

Actual circuitry may vary based on the specific application being addressed so long as the net result, the differential electrode potential waveforms, yields reliable control. One such approach utilizes the principle of the H-Bridge. This reduces the requirements on the power supply and enables the two drivers to share in the generation of the functional waveforms. Additional approaches will be presented primarily to illustrate the variety of acceptable drive schemes.

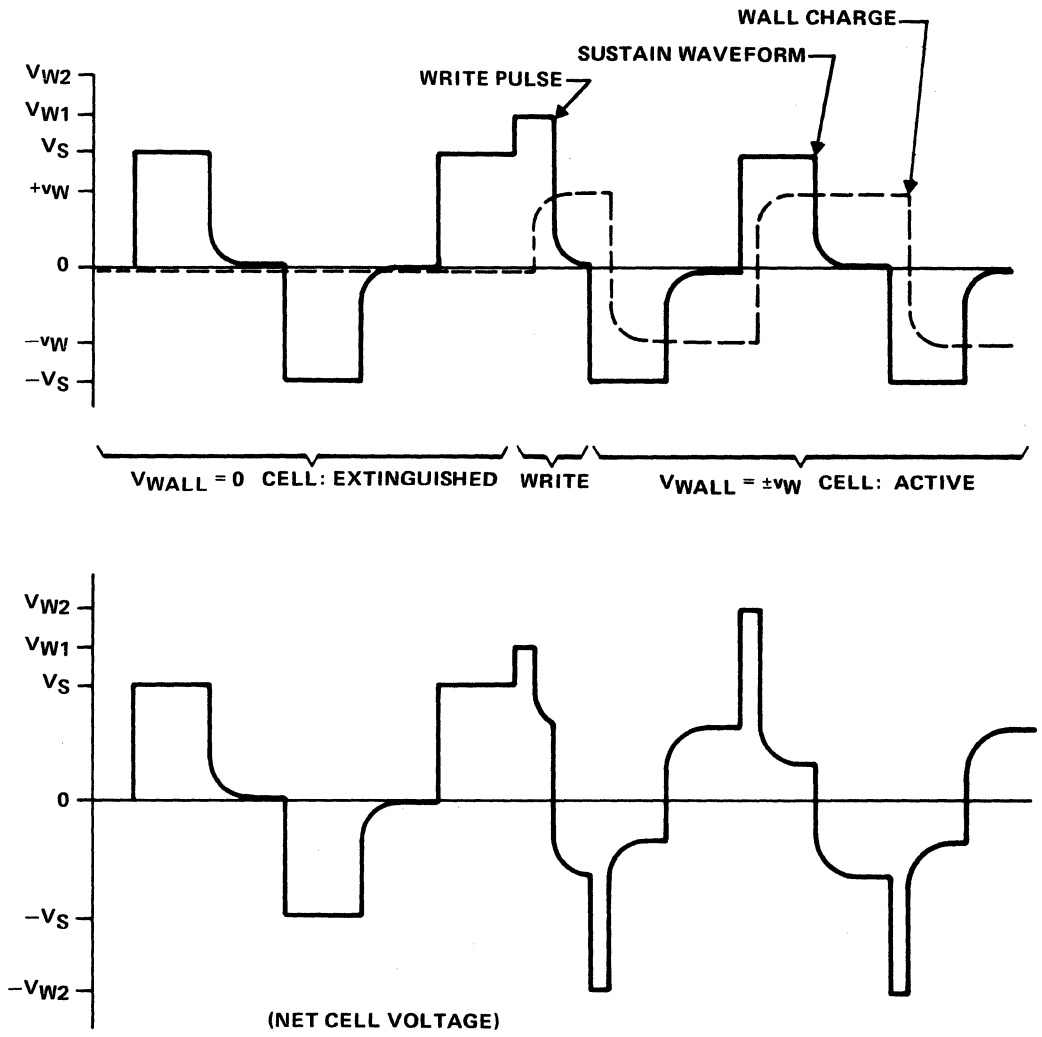


Figure 8-30. Write-Sustain Cycle Cell Waveforms

The high voltage BIDFET drivers used in these approaches are the SN75500A and SN75501C ac plasma display drivers. Designed specifically for ac plasma display applications, the SN75500A and SN75501C mark a significant milestone in the development of the ac plasma display technology. Prior to their development, the high voltage requirements of the plasma panel prevented the use of conventional integrated circuits as electrode drivers. This meant that the electrode interface must employ discrete components for proper control. This is quite prohibitive on larger panels without a more sophisticated drive scheme. The SN75500A and SN75501C drivers each provide circuitry required for active control of 32 electrodes. Interface to a 256-line by 256-line panel can now be achieved with a total of 16 integrated circuits (eight SN75500A and eight SN75501C). Use of these devices allows a significant reduction in the complexity and cost of the system electronics required to operate the ac plasma display.

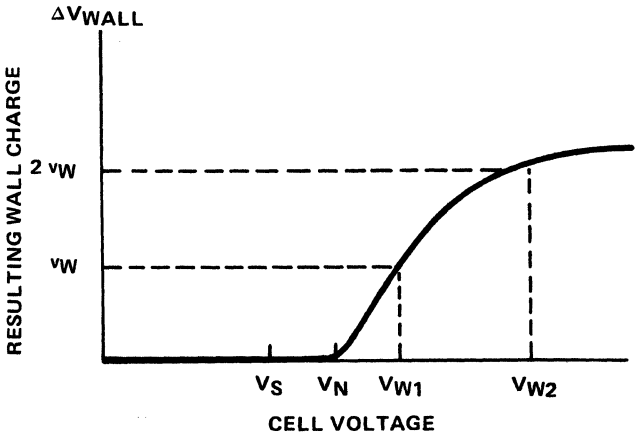


Figure 8-31. Charge Transfer Characteristics of AC Plasma Cell

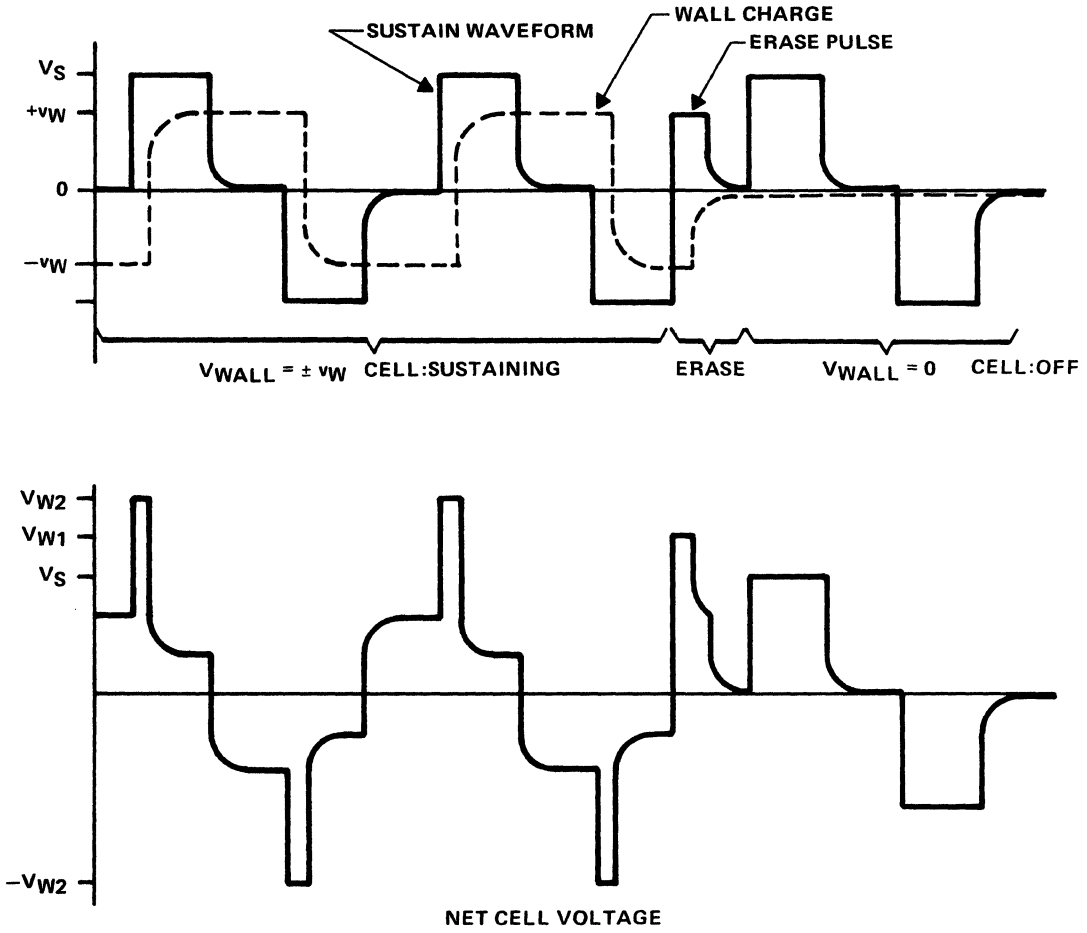


Figure 8-32. Sustain-Erase Cycle Cell Waveforms

The Functional Waveforms

The functional waveforms developed are the primary waveforms which provide the basic functions required in the operation of an ac plasma panel display: sustain, write, erase, and blanking. These waveforms are only one of several approaches, all of which may provide satisfactory operation. The main intent of this application section is to present the methods used to develop the waveforms and the implementation of the SN75500A and SN75501C drivers.

Figure 8-33(a) illustrates the basic waveforms for write, sustain, erase, and blanking. This is the net differential waveform created between the X and Y-axis electrodes by excursions on the X-axis or Y-axis or both. Figure 8-33(b) shows the composition of the differential waveform and identifies the origin of the components.

The first sequence of waveforms to consider is the sustain waveform. Review of Figure 8-33 shows the sustain waveform to be composed of two parts: the base pulse applied to the X-axis and a negative excursion on the Y-axis. It is important to note that this basic waveform is found in all other waveforms which require the retention of the panel data (selective write, selective erase). Additionally, this signal is nonselective, it must appear at all electrode nodes where the cell data is to be maintained. Any cell not experiencing this differential signal will fail to retain its active status. The first component of the sustain waveform, the base pulse, is generated *external* of the X-axis drivers, and is applied to all electrodes addressed along the X-axis. Thus it is identified as the X-axis sustain. Additionally, since the drivers for all the X-axis electrodes share common circuitry, the X-axis sustain is commonly called the bulk sustain. The second component of the sustain waveform, the negative pulse appearing on the Y-axis is not considered a bulk-sustain signal since it is created by the Y-axis drivers and each electrode addressed along the Y-axis is driven by its associated driver output circuitry. Supplemental pulses thus created are identified with their axis, Y-axis sustain. Together, the bulk (X-axis) sustain minus the Y-axis sustain combine to compose the basic sustain waveform. The SN75501A ac plasma driver was specifically designed to provide the Y-axis driver function. Additional control of the output circuitry allows all outputs (32) to be switched low, independent of the select control circuitry employed in selective output operations such as write and erase. All the outputs of the SN75501A switch low when the sustain input is taken low, thus all electrodes addressed along the Y-axis experience the Y-axis sustain signal.

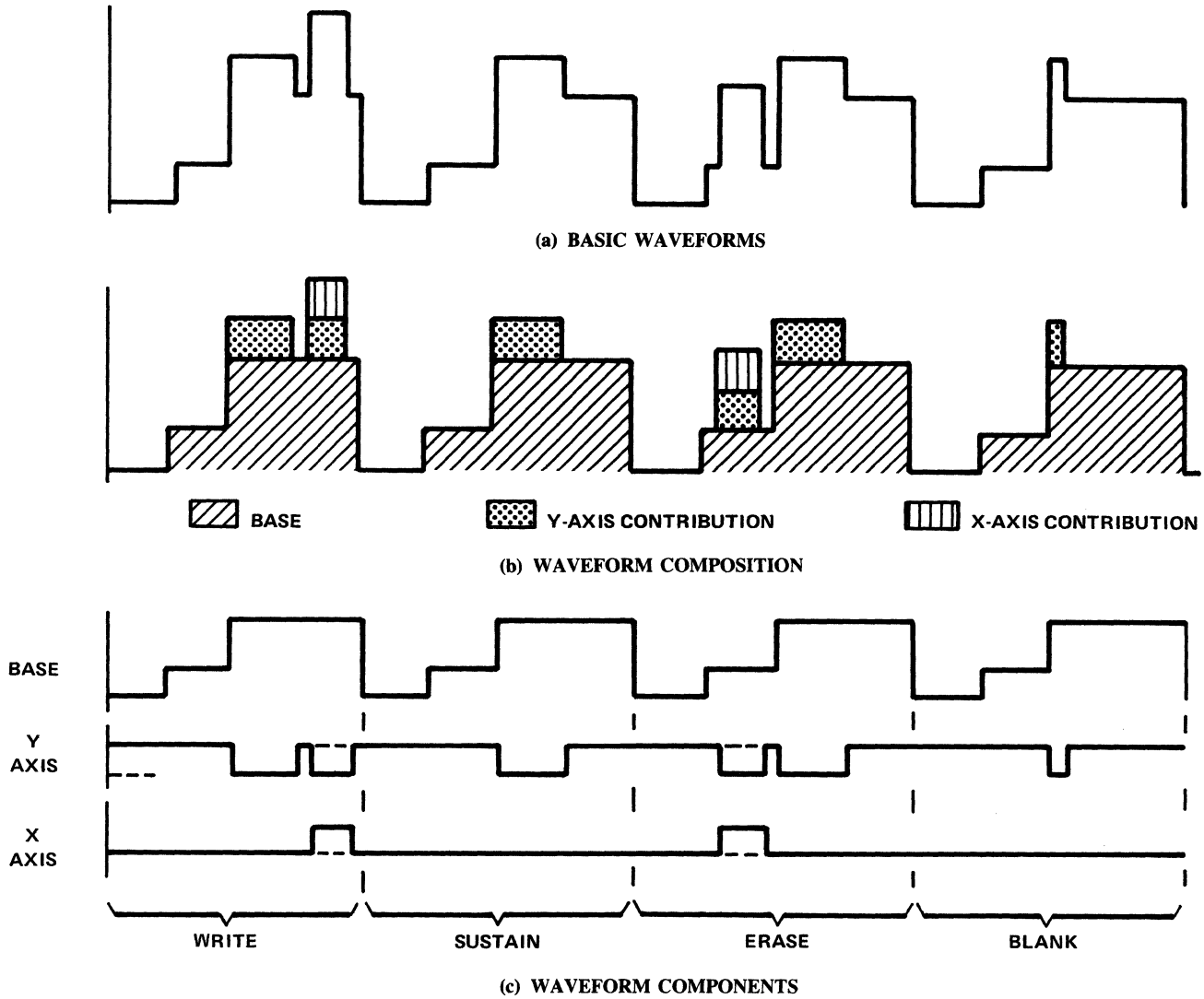


Figure 8-33. Functional Waveforms

The blanking waveform is also a nonselective waveform as it is used to blank the entire panel. Composed of the same components as the basic sustain waveform, it is similarly created.

The write and erase operations are selective operations. In other words, the pedestals superimposed on the basic sustain waveform, which create the write and erase waveforms, appear only at the pixels (electrode intersections) whose information is to be altered. This is accomplished by superimposing half the required pedestal on each of the associated X and Y-axis electrodes. This is illustrated in Figure 8-34. Note the importance of timing in these selective operations.

All other nodes experience either a standard sustain waveform or a half-select waveform. Standard sustain waveforms appear at all nodes where neither of the associated electrodes (X-axis or Y-axis) exhibit a half-select pulse. A half-select waveform appears at all nodes where only one of the associated electrodes exhibits a half-select pulse. The pedestal created by a single electrode excursion in a half-select waveform is insufficient to ionize the media gas and initiate a write-sustain sequence. The half-select pulses appearing on the X and Y-axis are created by the X and Y-axis drivers respectively. The SN75500A X-axis and SN75501C Y-axis drivers are designed to provide these functions. Both devices contain circuitry for selective control of their outputs. The specifics of this circuitry are discussed in their respective sections. Let it be sufficient to say at this time that with proper data controls established, the selected outputs of the SN75500A switch positive and the selected outputs of the SN75501C switch negative when the strobe input of both devices is pulled low. The determination of a write or erase operation depends on the timing of the strobe. Figure 8-35 illustrates use of the sustain and strobe inputs in the generation of the basic operational waveforms.

As mentioned previously, a variety of approaches for driving the ac plasma panel can be employed. The previous approach utilized the half-select principle for selective operations with an X-axis bulk sustain and a Y-axis supplemental sustain. Additionally, the X-axis drivers floated on the bulk sustain signal while the Y-axis

remained ground based. The following example incorporates split sustain and uses a common driver for both axes. Selective operations are performed using the blanking principle.

A split axis sustain merely says both axes employ an externally generated bulk sustain signal of opposite polarities. Figure 8-36 illustrates how the basic sustain waveform is created using this approach. The write technique for selective operations superimposes a full-select pedestal of opposite polarity on both axes. Locations along the selected electrode which are not to be altered are not affected by a single pulse on either axis. Only the pixel at the intersection of the selected electrodes is affected. Both axes require a selective pulse of the opposite polarity for the write operation. Figure 8-37 illustrates the array of waveforms created using this approach and their origin.

SN75500A AC PLASMA DISPLAY AXIS DRIVER

The operation of the SN75500A on the horizontal or vertical electrodes is primarily dependent on the panel's application. The outputs of the SN75500A are normally low and switch high selectively when the strobe input is low. The SN75500A thus provides the positive select pulses. The logic symbol, functional block diagram, and output structure of the SN75500A is shown in Figure 8-38. Selection of the outputs (32) is accomplished with the select and data inputs. The 32 outputs of the SN75500A

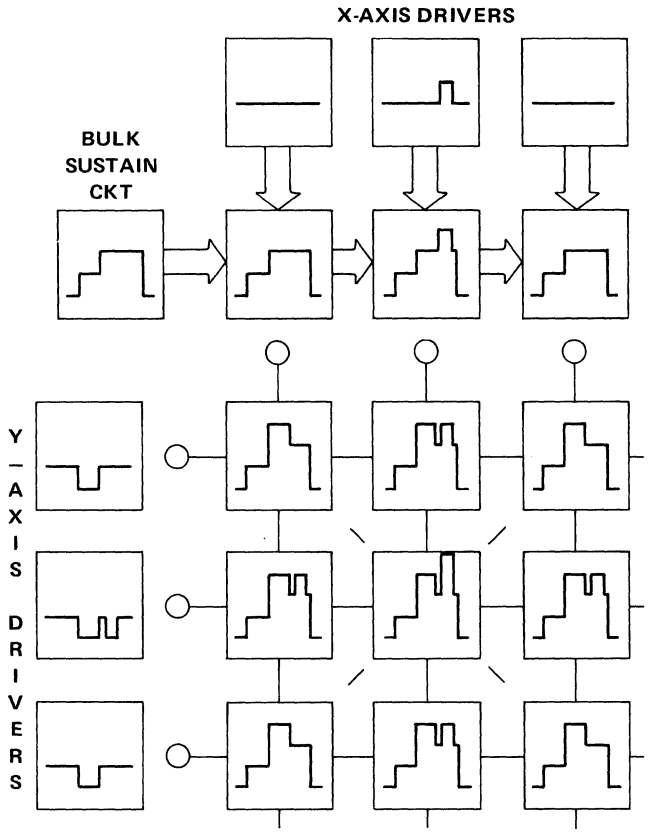


Figure 8-34. Write Waveform Array and Origin

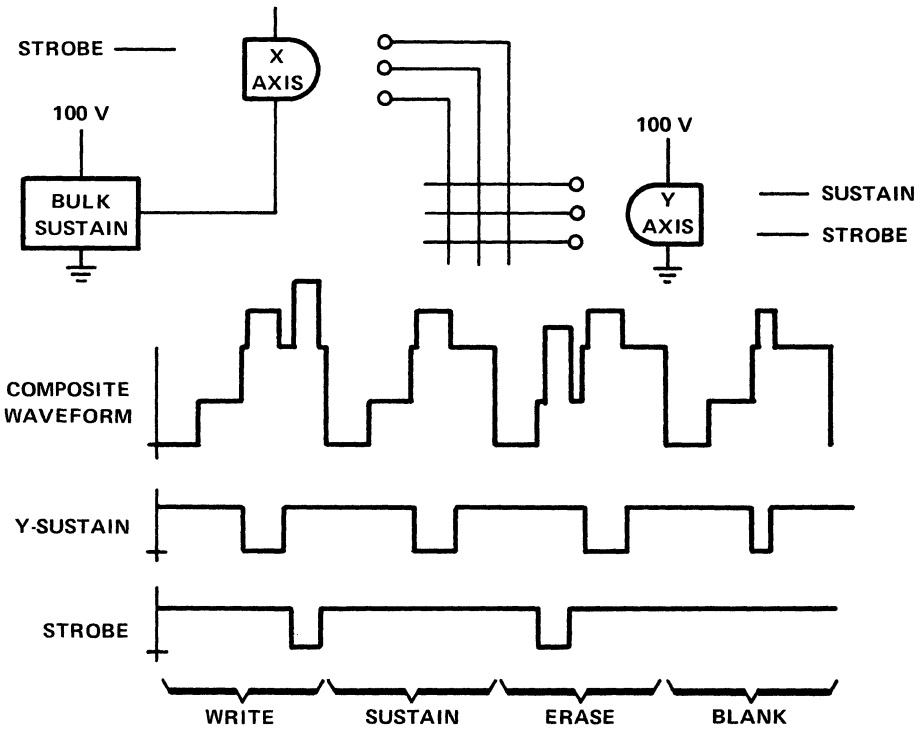


Figure 8-35. Control Signal Timing

are divided into four sections (1QX, 2QX, 3QX, 4QX) of eight outputs each. Only one of the four sections can be activated at one time (eight outputs). All other outputs (24) remain low. For this reason most systems use the SN75500A to scan the electrodes along which the information is written.

Selection of the specific section is determined by the select inputs S0 and S1 (Table 8-1). When selected, the state of the eight outputs of the section is determined by the data stored in the 8-bit storage register. Data is shifted into the storage register in a serial fashion on the positive transition of the clock. The maximum guaranteed data

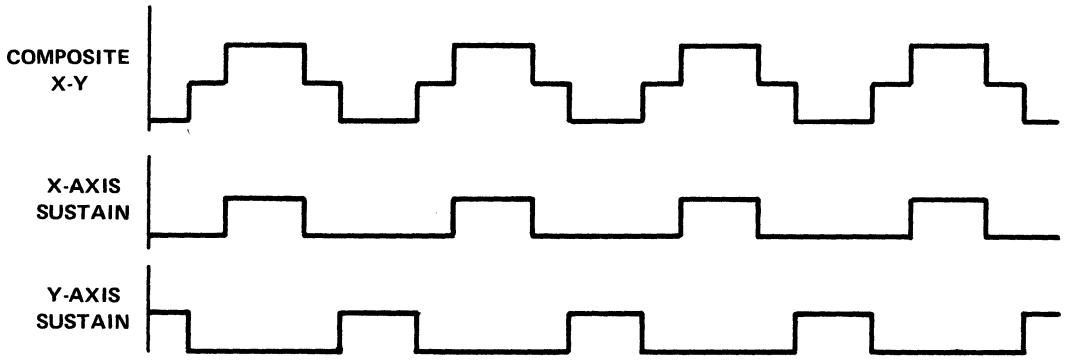


Figure 8-36. Split Axis Sustain

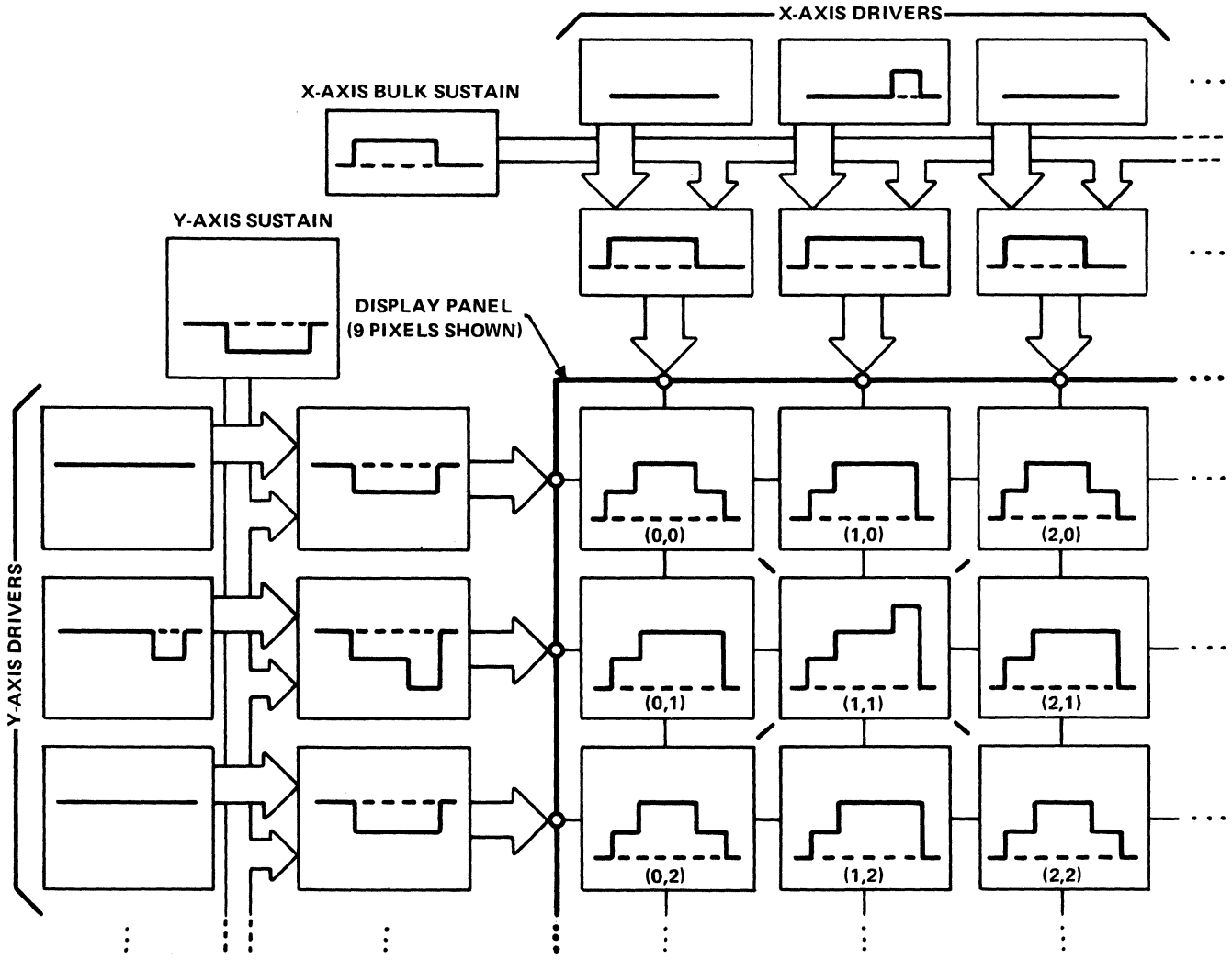


Figure 8-37. Write Waveform Array and Origin Split Axis Sustain — Blanking Select

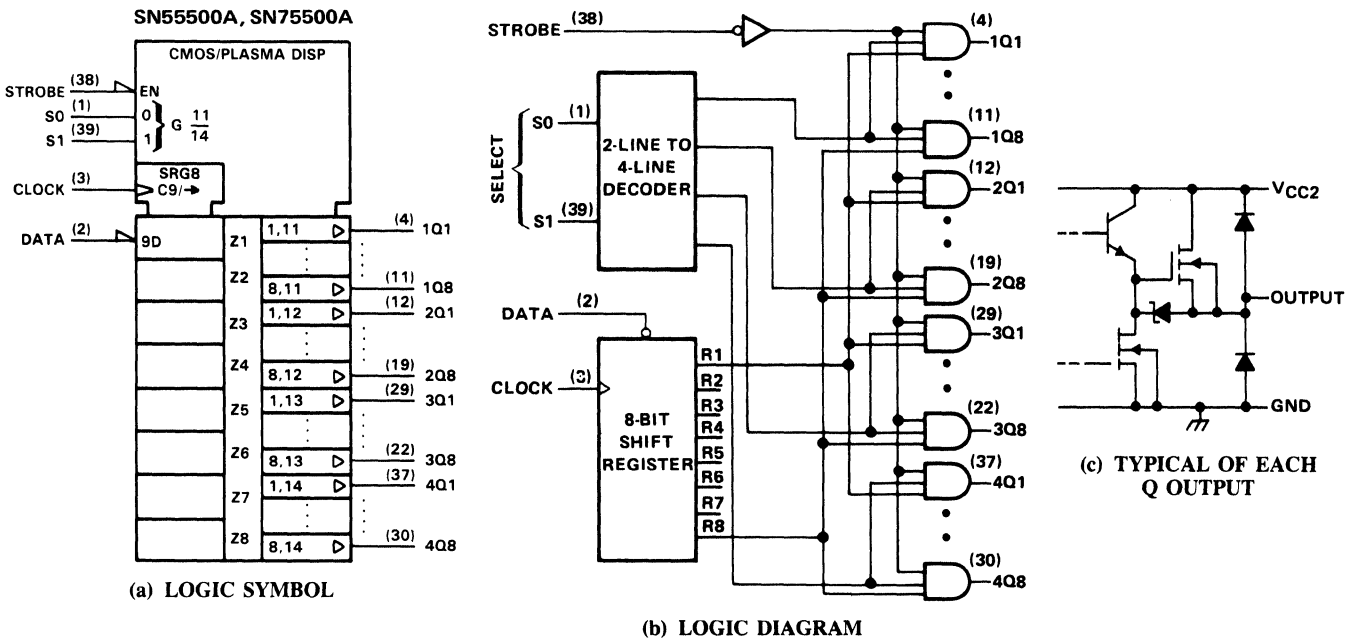


Figure 8-38. SN55500A and SN75500A

rate is 4 MHz. Data is shifted into the Q1 register and progresses to the Q8 register. A logic zero previously entered in the serial data input stream determines which of the outputs will switch high when the SN75500A is strobed (pulsed low). All outputs of the SN75500A contain clamp diodes to the V_{CC2} and GND supply inputs. This allows it to be operated on a base waveform where required. These diodes play an important role as discussed in the following

Table 8-1. Select Input Truth Table

S0	S1	Outputs Enabled
0	0	1Q1 thru 1Q8
1	0	2Q1 thru 2Q8
0	1	3Q1 thru 3Q8
1	1	4Q1 thru 4Q8

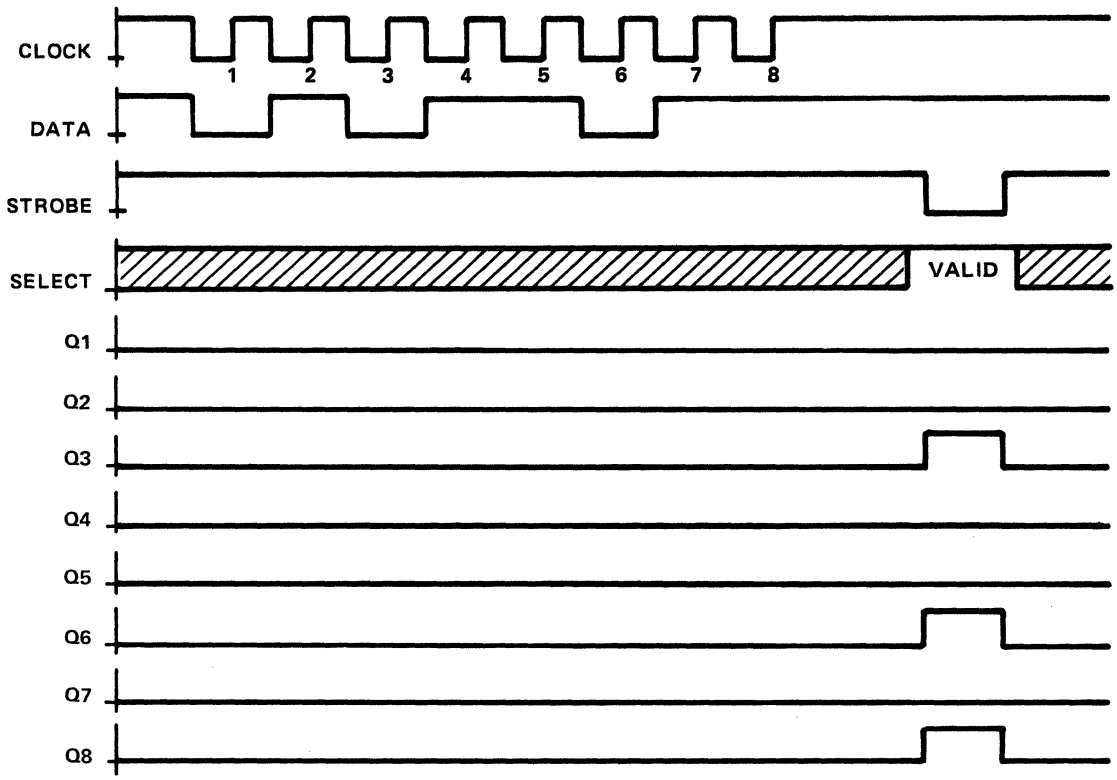


Figure 8-39. Typical Operating Sequence — SN75500A

section on Functional Adaptation of the SN75500A and SN75501C. Push-pull circuitry on each output provides active switching between the GND and V_{CC2} supplies. All inputs of the SN75500A are CMOS compatible (V_{TH} = 5 V) and assume a logical 1 if left open. A typical operating sequence is shown in Figure 8-39.

SN75501C AC PLASMA DISPLAY AXIS DRIVER

The SN75501C is designed to generate the negative select pulses. In addition, the internal control circuitry provides for all outputs to be switched low independent of the stored data when the sustain input is taken low. This feature is provided primarily for the purpose of creating a supplemental sustain signal. Unlike the SN75500A, the SN75501C can operate on all 32 of its outputs at one time. The logic symbol, functional block diagram, and output structure of the SN75501C are shown in Figure 8-40. Control of the output gates is established in the internal 32-bit shift register. A logic zero previously entered in the serial data input stream determines which of the outputs will switch low when the strobe input is taken low. Data enters the serial shift register on the positive transition of the clock input. The maximum data rate is 4 MHz. All outputs of the SN75501C contain clamp diodes to the V_{CC2} and GND supply terminals. This allows it to be operated on a base waveform where required. The push-pull output circuitry provides positive switching of all outputs between the V_{CC2} and GND supplies. The CMOS compatible inputs (V_{TH} = 5V) assume a logical 1 if left open. A typical operating sequence is shown in Figure 8-41.

FUNCTIONAL ADAPTATION OF THE SN75500A AND SN75501C

In the previous text, functional waveforms were discussed. It is the intent of this section to discuss the adaptation of the SN75500A and SN75501C to these drive techniques and to identify specific considerations which must be observed for satisfactory operation.

Strobing and Sustaining

The output gate circuitry for the SN75500A [Figure 8-38(c)] and SN75501C [Figure 8-40(c)] is virtually identical. Both devices contain a pair of DMOS output transistors for active control of the output. The lower DMOS transistor receives its drive from the low voltage supply, V_{CC1} (12 V). Thus the power consumption of the gate drive circuitry is minimal. The gate drive of the upper DMOS structure however experiences the full high voltage bias (100 V). To minimize its power dissipation, the gate circuitry incorporates a dynamic drive scheme which coincides with the dynamic output current requirements of the panel. In other words, the drive circuitry initially provides a large gate drive capable of saturating the upper DMOS transistor during the transition period of the output when the current demand is large. As the panel capacitance is charged and the current requirements decrease, so does the gate drive. This kick current occurs every time the output of the drivers is required to switch high.

The kick current is approximately 60 mA with a duration of 300 ns. If operated in a system whose V_{CC2} is 100 V, the resulting power consumption is 1.8 μJ. The average power dissipation then depends on the frequency at which the kick circuit is employed. In a system operating at a 50 kHz (period = 20 μs), this equates to an average dc power of 90 mW.

This causes a 7°C rise in the chip temperature over the ambient. The kick circuit being discussed here is activated every time the output is strobed regardless of whether or not the data causes the output to switch. For this reason, a selective strobe architecture is preferable in

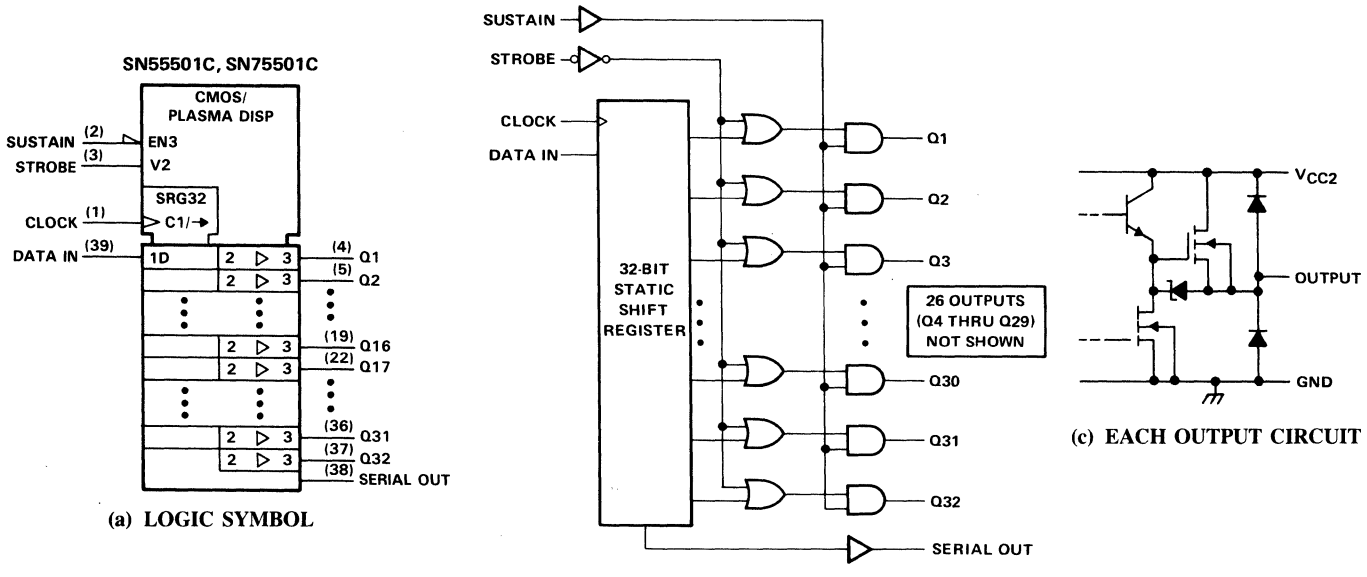


Figure 8-40. SN55501C and SN75501C

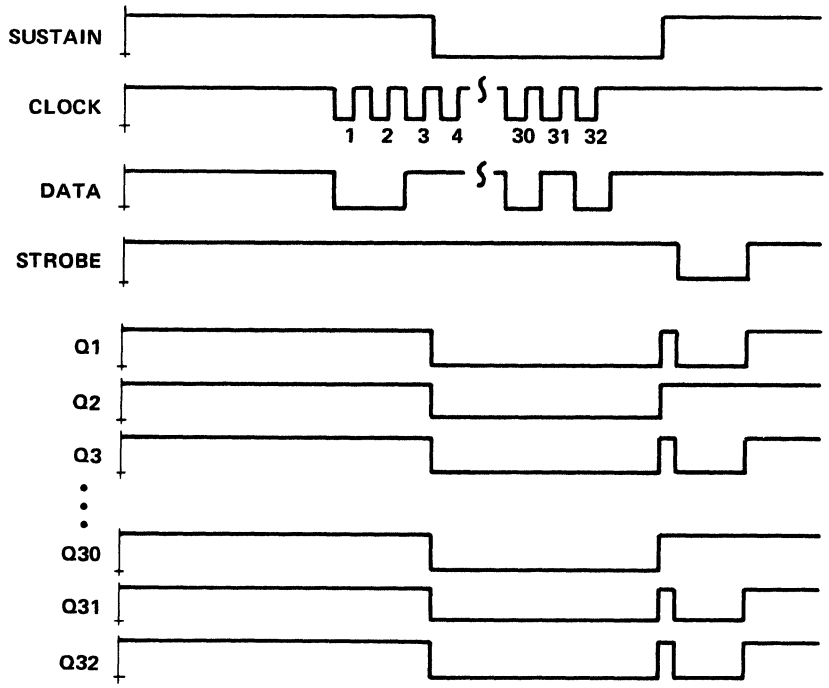


Figure 8-41. Typical Operating Sequence — SN75501C

a system that updates panel information every cycle. Thus, each driver experiences only the additional power dissipation while it is actively performing the panel operations (writing or erasing) thus reducing the duty cycle and effective dc power. In a 512-line panel (16 drivers: 8/side), this represents an 88% reduction in power due to data operations. Panels which fill an entire line or column with data to be written in parallel also reduce the effective dc power. With a maximum data rate of 4 MHz, it requires 64 μs to enter 256 serial data bits (8 drivers × 32 bits). If the information is then written on the panel in the fifth cycle, the effective power resulting from the data operations on the panel is reduced by 80%.

These strobing techniques affect only the kick circuit power associated with the data operations of the devices. In the case of the SN75500A, this is its only contribution. With the SN75501C, however, the kick circuit not only applies to strobed response of the driver but also to the sustain response. The sustain feature of the SN75501C is employed as in the initial example, the SN75501C output is pulsed twice in each cycle and the average power increases to 180 mW. This causes a 14°C rise in the chip temperature over the ambient.

Floating Driver Considerations

In most applications, one or both axis drivers will be required to operate (float) on a base waveform. Output clamp diodes have been provided on each output to accommodate this requirement. Figure 8-42 shows the output structure which is common to both driver circuits, SN75500A and SN75501C.

In the case of the SN75501C, the output is normally high, therefore Q1 is normally on. A base pulse applied to the SN75501C is therefore applied to the V_{CC2} terminal. As shown in Figure 8-43, positive excursions on the V_{CC2} terminal are passed through the output transistor Q1 while negative excursions are coupled through the catch diode D_1. Since the data retention and decode circuitry receive their bias from the V_{CC1} supply (12 V), variations in the V_{CC2} supply will be reflected at all outputs but will not affect the stored data present in the SN75501C's register. If the outputs of the SN75501C are not required to switch below ground, the SN75501C may be operated ground-

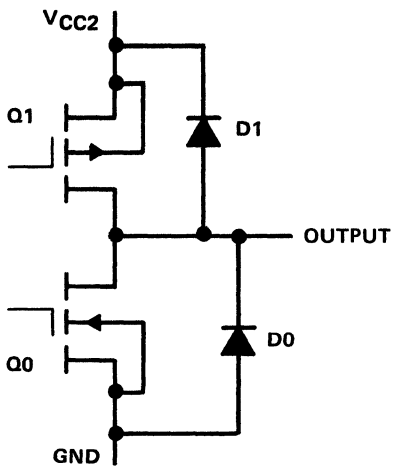


Figure 8-42. SN75500A and SN75501C Output Structure

based even though the V_{CC2} incorporates a base signal. Figure 8-44 illustrates a typical application which behaves in this manner. The only limitations are:

1. V_{CC2} must never be less than GND or greater than 100 volts above GND
2. The strobed data pulse occurs while V_{CC2} is at any potential other than GND.
3. The strobed data output pulse is always required to switch to 0 volts (GND).

If the data pulse is required to occur at various levels on the base pulse or switch to a potential other than GND (0V), the SN75501C must float with the base pulse waveform. This can be accomplished with floating V_{CC2} and V_{CC1} supplies referenced to the base waveform or by utilizing a capacitive storage bridge like that shown in Figure 8-45.

The SN75500A output is normally low, thus the output transistor Q0 of Figure 8-42 is normally on. A base pulse applied to the SN75500A is therefore applied to the

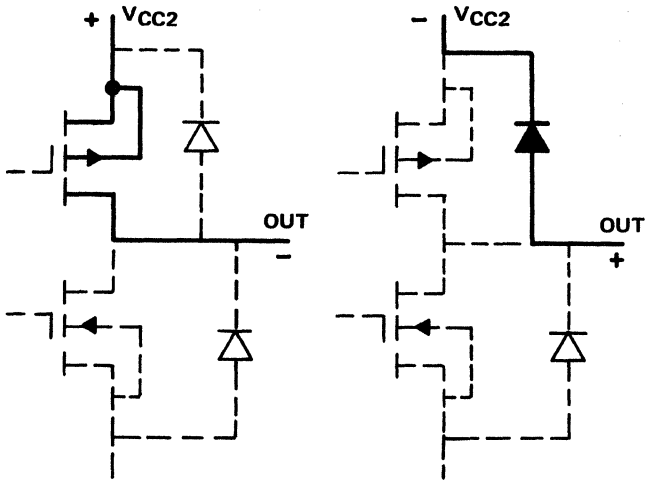


Figure 8-43. Floating SN75501C Current Paths

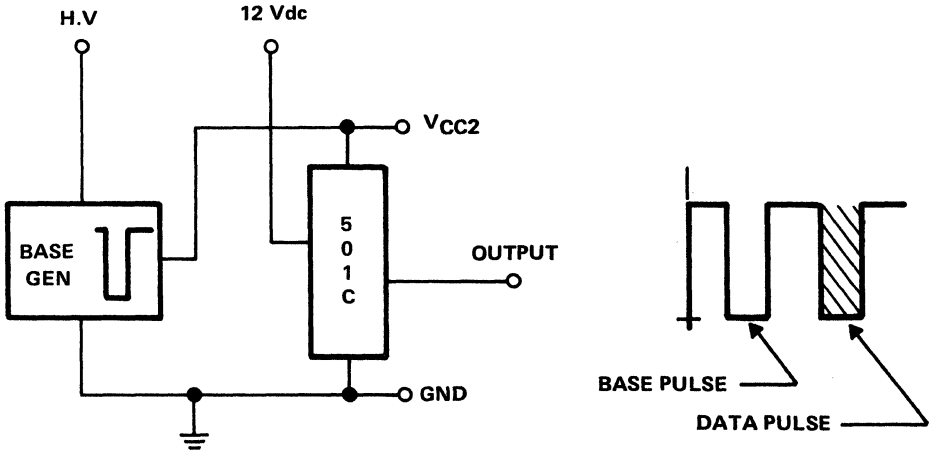


Figure 8-44. SN75501C with Pulsed V_{CC2}

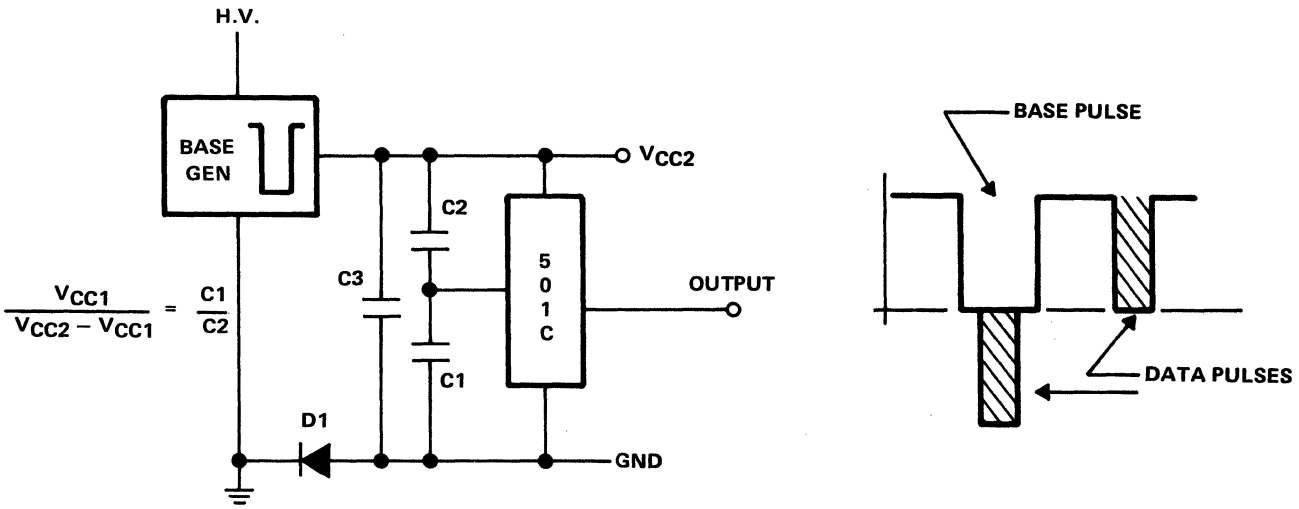


Figure 8-45. Floating SN75501C Fixed Bias

GND terminal. As shown in Figure 8-46, negative excursions on the GND terminal are passed through the output transistor Q0 while positive excursions are coupled through the catch diode D0. When utilizing this feature of the SN75500A, caution must be taken to assure proper retention of the data and to prevent excessive power consumption. When the lower clamp diode D0 is forward biased as is the case during the positive transition of the GND terminal, the SN75500A substrate also becomes forward biased. In this condition the output current demand is supplied in part from the high-voltage supply. Even though the current is small (typically 200 mA) when drawn from the high-voltage supply (100 V), it represents a significant power dissipation.

$$200\ \text{mA} \times 100\ \text{V} \times 1\ \mu\text{s} = 20\ \mu\text{J}$$

The average power consumed depends on the operating frequency of the system.

$$\text{at 50 kHz} : 20\ \mu\text{J} \times 50\ \text{kHz} = 1\ \text{W}$$

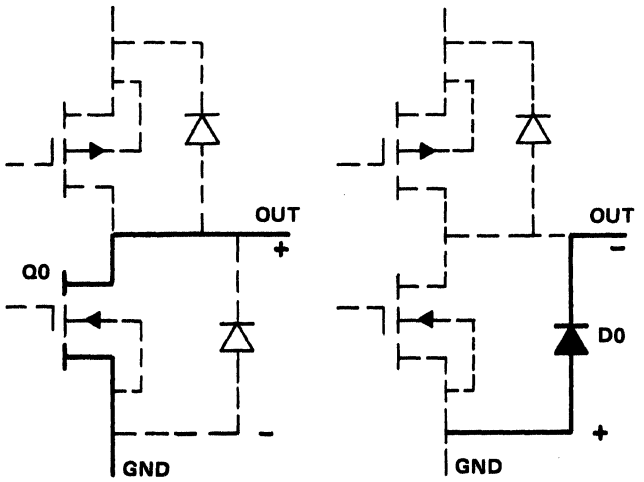


Figure 8-46. Floating SN75500A Current Paths

The SN75500A is designed such that the data registration and retention circuitry are powered from the V_{CC1} supply (12 V). The high-voltage supply, V_{CC2} is required only to provide pull-up of the SN75500A outputs when a positive output pulse is desired. It is most beneficial therefore to blank the V_{CC2} input except for the period of time the outputs of the SN75500A are switched high (strobed). Utilization of this feature (strobing the high voltage) allows lower power dissipation and improved performance with the SN75500A. Figure 8-47 shows a typical circuit which provides for strobed application of the V_{CC2} supply and a regulated 12 V supply for V_{CC1}. Figure 8-48 shows a circuit using an FET to strobe V_{CC2}. It is also possible to use a simple series impedance to limit the current from the high-voltage supply.

Data Coupling Considerations

If operated ground-based, all inputs are CMOS compatible (V_{TH} = 5 V). If, however, either driver is floated on a base, signal entry of data into that device must be given due consideration.

One approach that is not necessarily cost effective, but simple, employs the use of coupling transformers on all data lines: clock, serial data in, strobe, sustain, select. In this configuration, data can be entered into the device regardless of the state of the base signal. This provides the maximum utilization of the drivers by minimizing the time required to shift data into the drivers' storage registers. Another approach requires gating of the data but creates a totally solid-state interface. In this approach, data is gated into the drivers when they reside at ground. Figure 8-49 in which a base pulse is employed, illustrates the timing of the gated clock which registers the data in the respective driver. Considering 4 MHz as the maximum data rate, 8 μs is required to fill the 32-bit shift register of the SN75501A. The frequency and duty cycle of the base pulse then decide whether the data can be entered in a single cycle. The limiting factor in most applications is the speed of the source from which the data is received.

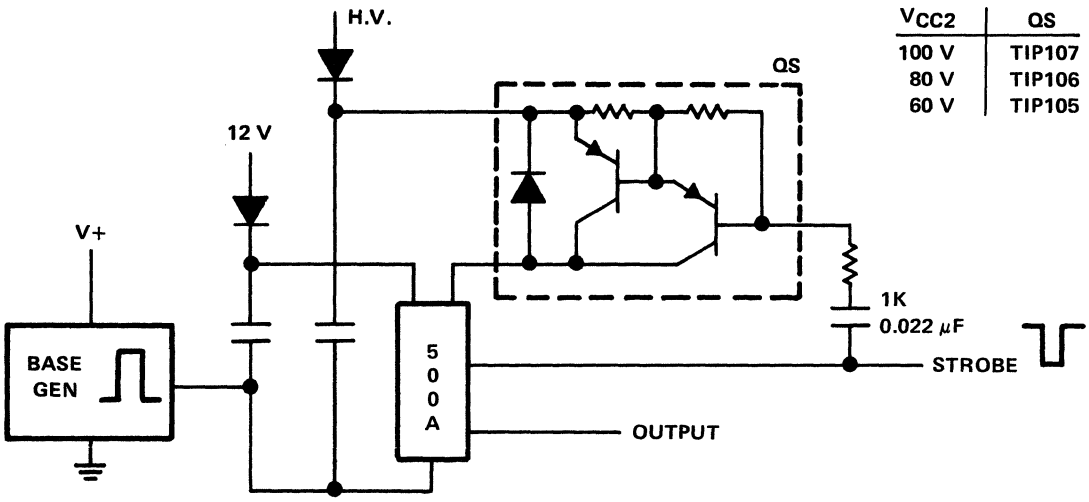


Figure 8-47. Floating SN75500A with Pulsed V_{CC2}

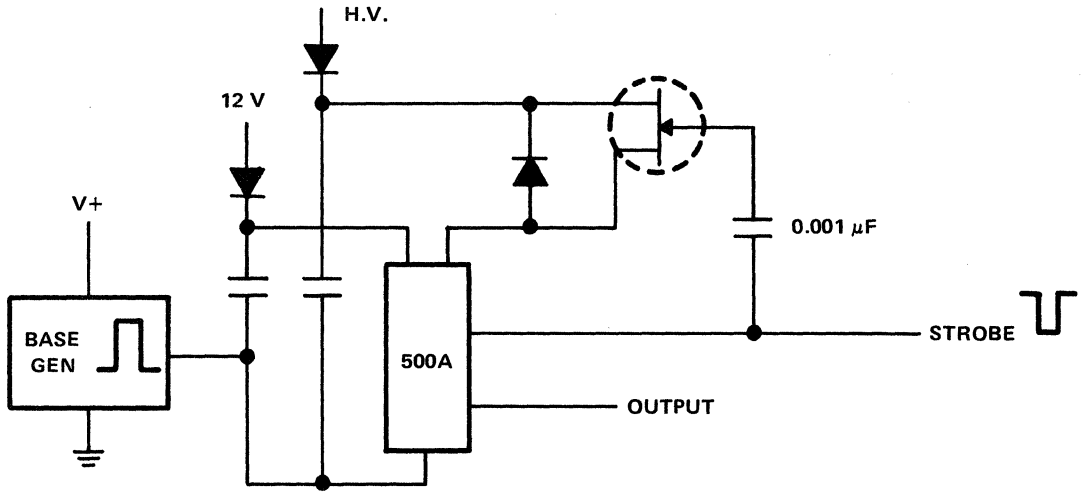


Figure 8-48. Floating SN75500A with FET Pulsed V_{CC2}

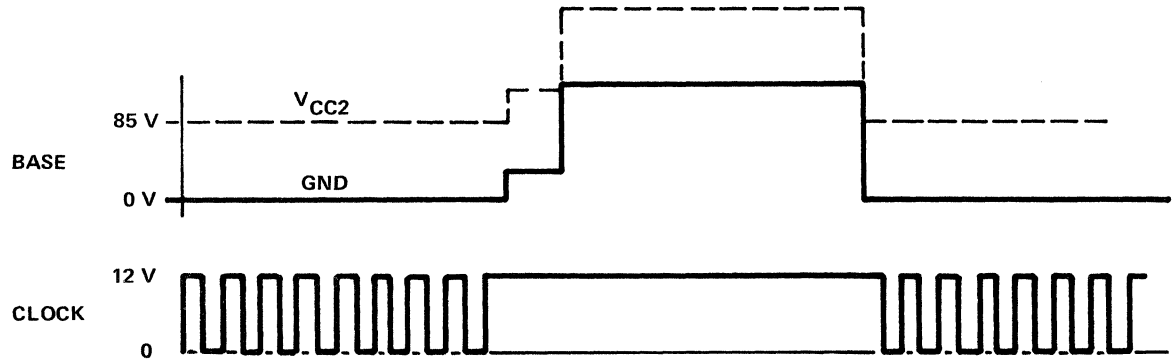


Figure 8-49. Gated Clock for Floating Applications

Figure 8-50 shows a circuit for use with positive base signals. When the base pulse is at ground, the input signal operates as a pull-up to the input of the CMOS buffer through the blocking diode. As the ground bias of the buffer circuit rises with its associated plasma driver, the diode becomes reverse biased and the resistive termination of the input maintains a logic zero at its input. With this circuit, transitions in the floating bias applied to the buffer gate are not detectable at its output, providing the input signal is low.

Figure 8-51 shows a similar interface circuit for use with negative base signals. Note the reversal of the blocking diode. This circuit uses a normally high (logic 1) input signal. While ground based, the buffer gate will respond to logic zero transitions at its input. As the ground and V_{CC} inputs of the buffer circuit go below ground, the blocking diode becomes reverse biased and the terminating resistor establishes a logic 1 (high) on the gate input. Thus, provided that the input is at a logic 1, transitions in the ground and V_{CC} bias inputs concurrent

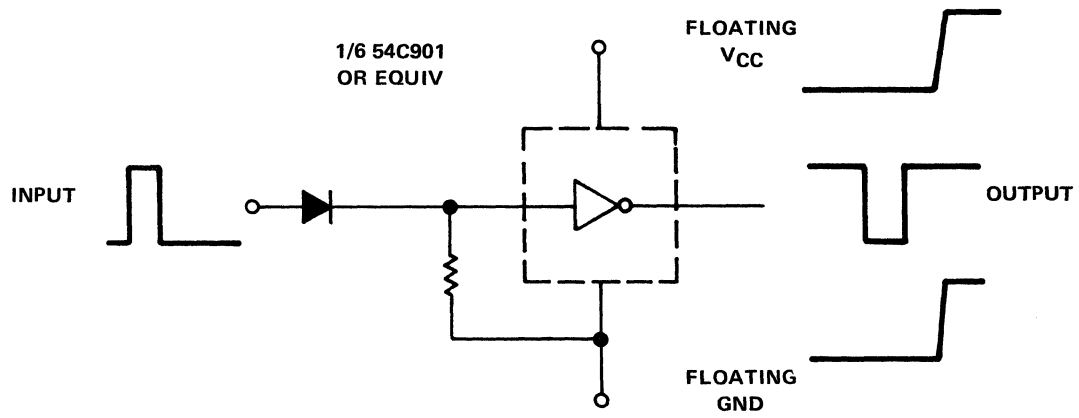


Figure 8-50. Positive Base Signal Data Buffer Circuit

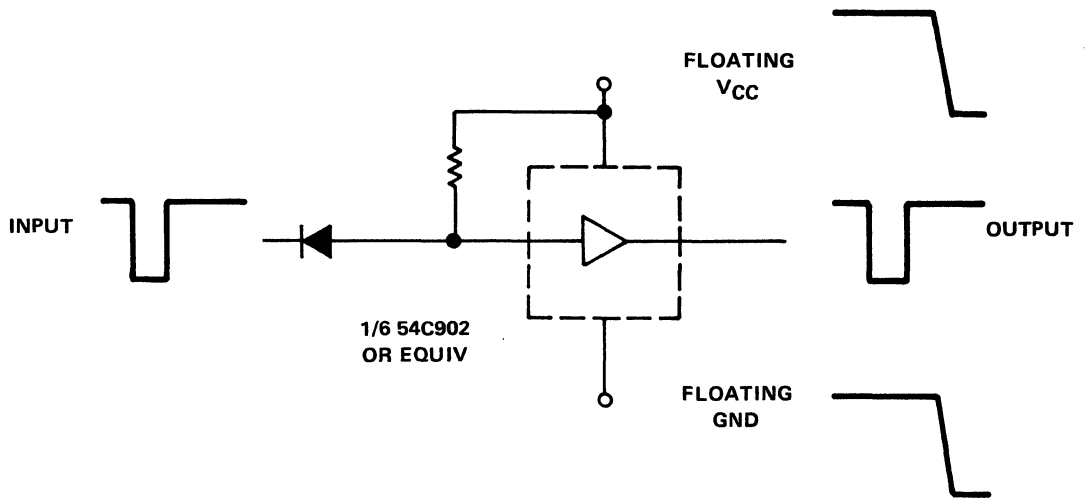


Figure 8-51. Negative Base Signal Data Buffer Circuit

with the respective plasma driver will not affect the output of the buffer. The use of the inverting or noninverting buffer gate is determined primarily on the preferred status of the output signal during the period of time the driver is floating. Both circuits of Figures 8-50 and 8-51 create normally high (logic 1) signals. This is the preferred state of the positive edge triggered clock circuits of the SN75500A and SN75501C plasma drivers.

VACUUM FLUORESCENT DISPLAYS

INTRODUCTION

A vacuum fluorescent display (VFD) operates on the same basic principles as a triode vacuum tube. It is composed of a grid, cathode, and an anode that has been coated with phosphor. The anode will emit light when electrons from the cathode strike it with sufficient energy. The blue-green color light emitted is bright, yet clear and pleasing to the human eye.

The VFD comes in a wide variety of sizes in dot matrix, segmented, or dot character arrangements. Its flat panel construction, relatively low operating voltage, and low power consumption make VFDs an attractive option in many display applications.

THE VFD PANEL

Construction

The VFD is contained in a glass envelope which provides the vacuum environment required for proper operation (Figure 8-52).

The cathode is an oxide-coated tungsten filament that emits free electrons when heated by a current. The display is controlled by the bias conditions placed on the grid and anodes. Column or character selection is provided by the grid while individual segment control is governed by the anodes. Electrons from the cathode pass through the grid when it is at a positive potential and are blocked when it is at a negative potential. Electrons passing through the grid are attracted by anodes with positive potentials and are repelled by anodes with negative potentials (Figure 8-53). The applied voltages vary depending on the display format. Table 8-2 shows the range of element voltages and currents required by the majority of VFDs.

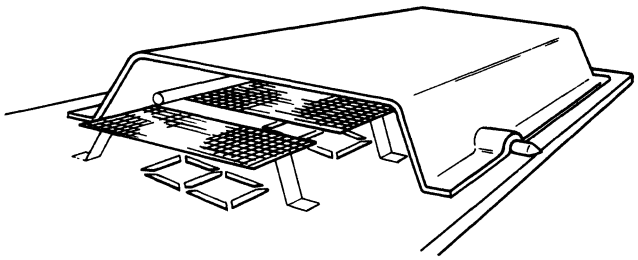


Figure 8-52. Vacuum Fluorescent Display Construction

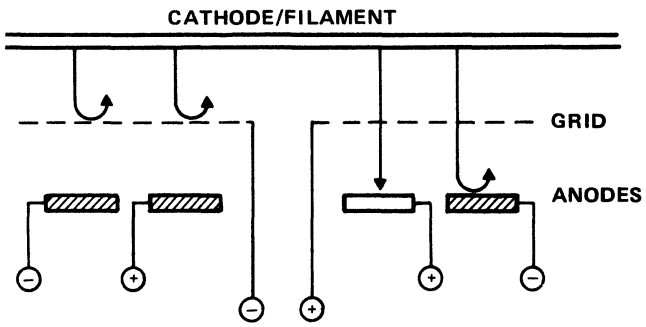


Figure 8-53. Vacuum Fluorescent Display Electron Flow

Table 8-2. VFD Operating Ranges

Parameter	Min	Max
Cathode Voltage	2.4 V ac	10 V ac
Grid/Anode Voltages	24 V p-p	70 V p-p
Cathode Current	20 mA ac	250 mA ac
Grid Current	2.5 mA p-p	30 mA p-p
Anode Current	2.5 mA p-p	30 mA p-p
Power Dissipation	14 mW/Char.	125 mW/Char.

Panel Performance

Higher resolution VFDs pose problems. As higher resolution is pursued the mechanical and electrical properties of the VFD require special considerations. The grid is a fine screen mesh with practical limitations on grid spacing and durability. Additionally, as neighboring display elements are brought closer, the fields created by their grids affect the display site being activated. The fringe field effect causes a nonuniformity in the luminance of the display. Most character displays employ a common grid for each character or column of characters. Thus the character spacing prevents this problem (Figure 8-54). Dot matrix displays, however, have no such space, thus grid/anode multiplexing is required so that no two adjacent cells are on at the same time. Figure 8-55 shows several arrangements of anode/grid connections used in dot matrix VFDs.

Except for the format shown in Figure 8-55(a), the configurations shown in Figure 8-55 provide good illumination. The particular style chosen depends on the application. Table 8-3 shows the total control pin count and cycle time required to complete one frame for various panel sizes.

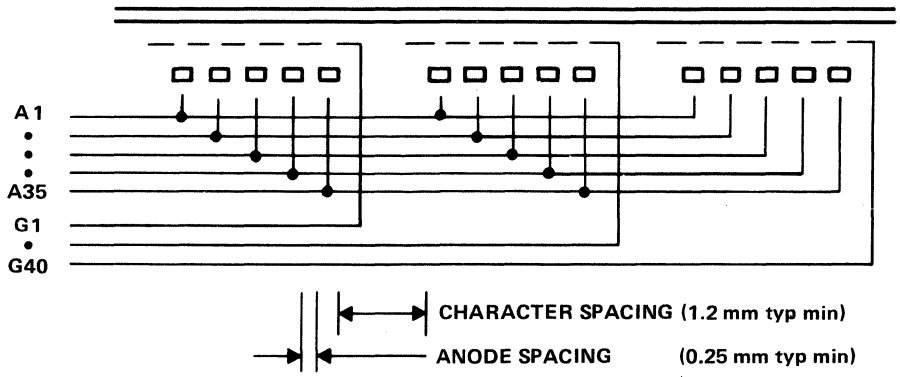


Figure 8-54. A 40: 5 × 7 Dot Character VFD

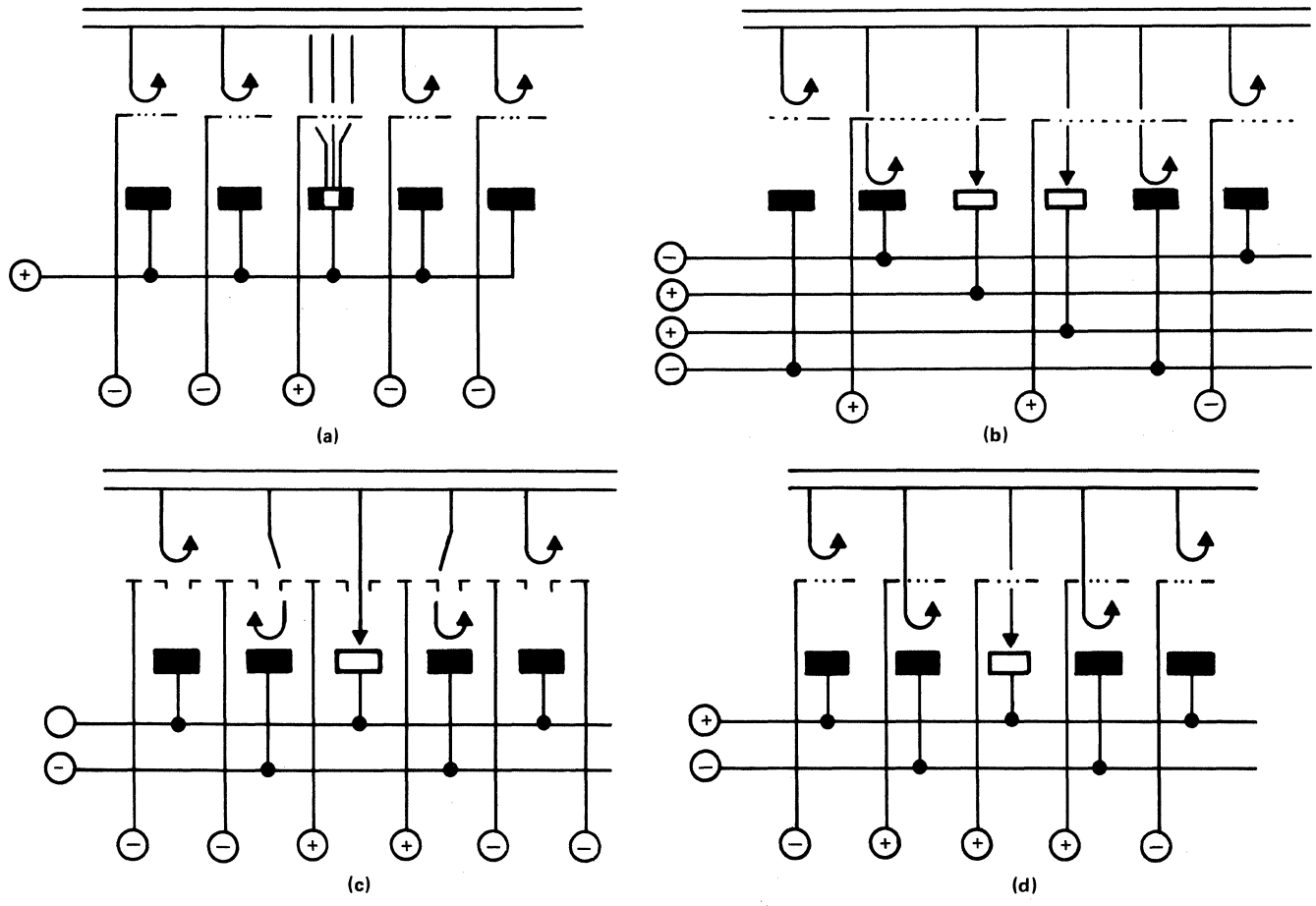


Figure 8-55. Grid-Anode Configurations of Dot Matrix VFDs

Table 8-3. VFD Configuration Comparison

Parameter \ Panel size	128 X 64				128 X 128				256 X 64			
Config.	A	B	C	D	A	B	C	D	A	B	C	D
Anode Lines	64	256	128	128	128	512	256	256	64	256	128	128
Grid Lines	128	64	128	128	128	64	128	128	256	128	256	256
Total Lines	192	320	256	256	256	576	384	384	320	384	384	384
Cycles/Frame	128	64	128	128	128	64	128	128	256	128	256	256

VFD Timing Requirements

The VFD from a timing standpoint, is very forgiving. A typical cycle is shown in Figure 8-56.

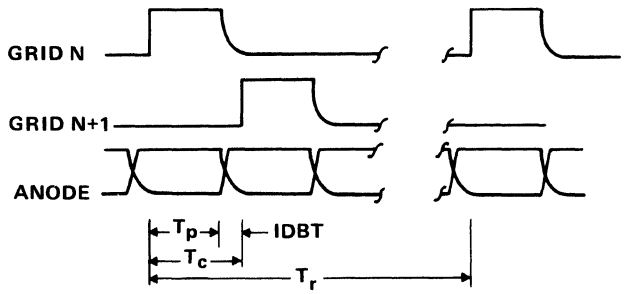


Figure 8-56. VFD Timing Diagram

The actual timing is governed largely by the application and panel size. The minimum panel refresh rate with undetectable flicker is 60 Hz. This defines the time (T_r) allotted to write the entire display one time (one frame). The amount of time allowed for each character or grid operation (T_c) is determined by the number of character or grid control lines (N) external to the display ($T_c = T_r/N$). To prevent noticeable degradation in the display intensity, each display site should be exercised at a minimum duty cycle of 1:150 ($T_p = T_r \times$ DUTY CYCLE). Neglecting any inter-digit-blanking time (IDBT), a display could contain as many as 150 grid or character control lines. However, to prevent ghosts, some time must be allotted for inter-digit-blanking. The allowable dead-time between strobes (IDBT) is the difference between the character cycle time T_c and the character or grid strobe width T_p. As the number of grid or character control lines approach 150, the IDBT approaches zero (0).

$$IDBT = \frac{T_r}{N} - \frac{T_r}{150}$$

Conventional drivers with resistive pull-down require an IDBT as large as 30 μs (20 μs typically). Thus the maximum allowable number of grid or character control lines must realistically be less than 150. Most displays limit this parameter to 128 (a convenient binary number < 150).

For a panel refresh rate of 100 Hz:
T_r = 10 ms
For an 80 character display
T_c = 10 ms/80 = 125 μs
For a 1:100 character duty cycle
T_p = 10 ms/100 = 100 μs
The allowable IDBT is:
IDBT = $T_c - T_p$ = 25 μs

Some applications may be limited by the excessive IDBT requirements of the resistive pull-down driver:
For a 128 grid display
$T_c = T_r/128$
For a 1:150 duty cycle operation
$T_p = T_r/150$
For a driver requiring 20 μs IDBT
IDBT = $T_c - T_p$ = 20 μs
T_r = 17.5 ms
The maximum panel refresh rate is:
R = $1/T_r$ = 57 Hz (MARGINAL)

DRIVE ELECTRONICS

The following discussion on drive techniques will be limited primarily to the interface drivers for the display, and their requirements and performance characteristics. Because the characteristics of the various display grid-anode configurations change (see Figure 8-55), interface-driver circuit requirements differ. Texas Instruments offers a selection of VFD drivers with a variety of features.

The UCN4810A 10-Bit VFD Driver

Figure 8-57 shows the block diagram, logic symbol and output circuit of the UCN4810A. The UCN4810A is a 10-bit active-high VFD driver. Input data is stored in a 10-bit serial shift register on the positive transition of the clock. Parallel data is presented to the output buffers through a 10-bit parallel D-type latch. Data at the respective output of the shift register will be transferred through the 10-bit latch while the strobe (latch enable) input is high. Data present at the latch inputs during a negative transition of the strobe will be stored regardless of subsequent changes, if the strobe input is low. A blanking control is provided which inhibits all output gates and assures they are low when the blanking input is high. All outputs [Figure 8-57(c)] are capable of sourcing 40 mA

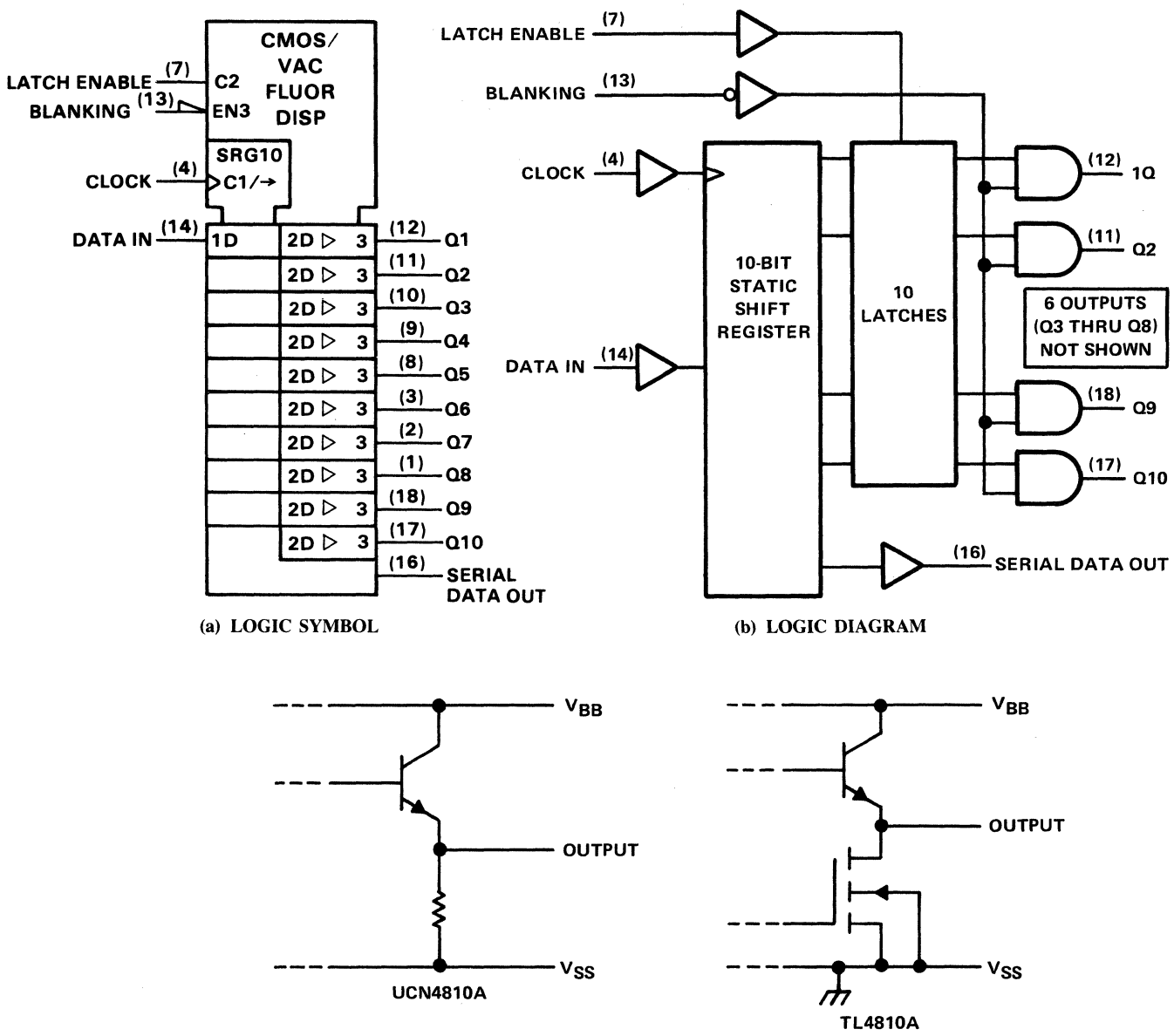


Figure 8-57. UCN4810A and TL4810A VFD Display Drivers

each from a V_{BB} supply voltage of 60 V, if the maximum allowable package power limitation of 1.3 W is not exceeded. This limits the duty cycle of the on time for various load requirements (Figure 8-58). All inputs are CMOS compatible but require the addition of a pull-up resistor to V_{DD} when driven by standard TTL logic.

The TL4810A 10-Bit VFD Driver

The TL4810A can be used as a direct replacement for the UCN4810A. The TL4810A utilizes an active totem-pole output to improve the sink current capability (1 mA minimum versus 400 μA) without sacrificing the resulting power consumption as conventionally experienced in a passive pull-down structure. The totem-pole output is composed of an npn emitter follower (source) and double-diffused MOS (DMOS) (sink) transistors [Figure 8-57(c)]. This improvement decreases the inter-digit-blanking time required and the overall device power consumption.

Unlike most VFD Drivers which are limited to an 85% duty cycle at 50°C, the TL4810A will sustain 25 mA in as many as six outputs per output load at a 100% duty cycle over its entire operating temperature range of 0°C to 70°C.

All device inputs are diode-clamped and compatible with standard MOS, CMOS and DMOS logic. Designed to control 10 VFD inputs, the TL4810A provides a positive edge triggered 10-bit serial shift register and a serial data output of the display information. A 10-bit D-type latch accepts parallel data from the serial shift register when the strobe (latch enable) input is high. The data stored in the latch circuitry when the strobe input is taken low remains unaltered regardless of subsequent changes in the data

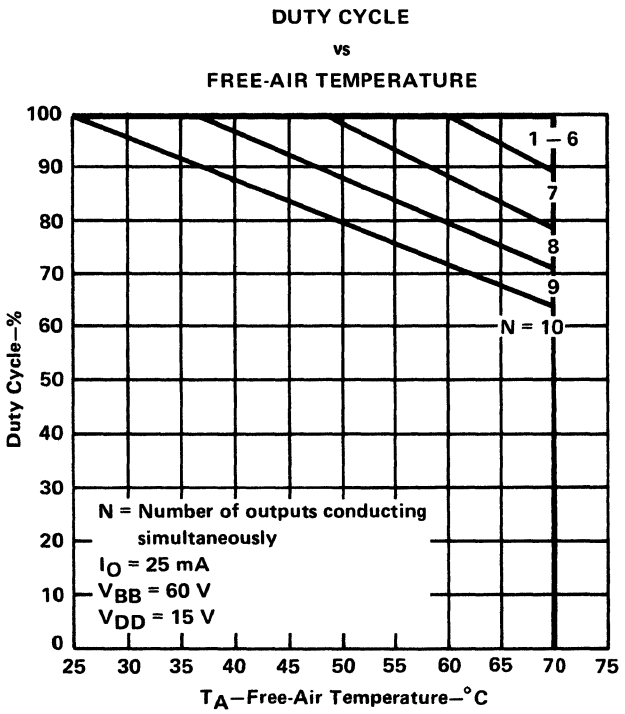


Figure 8-58. UCN4810A Operational Duty Cycle

present in the serial shift register. The latched information is then transferred to the output through the gated output buffers when the blanking output is low. A logic high on the blanking input causes all outputs to go low. All outputs are capable of sourcing 40 mA at 60 V.

The SN75512A 12-Bit VFD Driver

Figure 8-59 shows a logic symbol, logic diagram and output circuit of the SN75512A. The SN75512A is a 12-bit VFD driver with totem-pole outputs. The totem-pole outputs minimize the required IDBT to less than 1 μs. Input data is stored in the 12-bit serial shift register on the positive transition of the clock input. Parallel data is presented to the output buffers through a 12-bit D-type latch. Data at the respective output of the serial shift register is transferred through the 12-bit latch while the latch enable is high. Data present at the latch inputs during the negative transition of the latch is stored regardless of subsequent changes, providing the latch input remains low. The active-low strobe input enables all output gates. Each output is capable of sourcing 25 mA at a supply voltage of 60 V, providing the maximum package power dissipation of 1150 mW is not exceeded. Based on the maximum allowable voltage drop across the output at 25 mA sink current, the total package capabilities are as shown in Table 8-4. All inputs of the SN75512A are TTL compatible. A serial data-out is also available for cascading additional drivers.

The SN75513A 12-Bit VFD Driver

Figure 8-60 shows the logic symbol, logic diagram and driver output circuit of the SN75513A. The SN75513A is a 12-bit VFD driver with totem-pole outputs which minimize the required IDBT to less than 1 μs. Input data is shifted into a 12-bit serial shift register on the positive transition of the clock. Data appearing at the corresponding outputs of the shift register is presented directly to the output gates and is transferred to the Q outputs when the strobe input is low. Data in the shift register can be cleared with the reset input. A logic 0 on the reset input clears the shift register contents to a logic 0. Each output is capable of supplying 25 mA of source current at a V_{CC2} supply voltage of 60 V, providing the absolute maximum package power limitation of 1150 mW is not exceeded. Table 8-4 reflects the derating resulting from this consideration. All inputs are TTL compatible and assume a logic high if left open. A serial data output allows cascading of several devices without additional circuitry.

The SN75514 High Voltage 12-Bit VFD Driver

The SN75514 (Figure 8-61) is similar to the SN75512A except it is capable of operating at up to 125 instead of 60 V. Although not limited to high density applications, the SN75514 was designed to accommodate the specific requirements of large, high resolution (dot matrix) VF displays: high anode driver voltages, high-speed data reception and short inter-digit-blanking times (higher duty cycle).

As with the SN75512A, the 12-bit serial-in, parallel-out shift register is loaded on the positive edge of clock transition. However, the SN75514 combines the latch enable and output strobe functions of the 60 V device in one control line (strobe). Valid data is transferred from the shift register to the parallel latch outputs when the active-high strobe line is taken low. This is truly an edge-triggered data transfer as changes in the shift register contents while the strobe is held low will have no effect on the latch contents. With the strobe held low, high-voltage output lines go low (disabled state) and remain low until the strobe goes high. Upon raising the strobe line to a logic one, the latch contents are presented to the display through the high-voltage outputs (enabled state).

Another difference between SN75514 and the SN75512A lies in the high voltage supply requirements. Whereas a single supply of up to 70 V (V_{CC2}) was sufficient with the lower voltage device, the SN75514 requires two high-voltage supplies to deliver the maximum 25 mA per channel current drive capability. V_{CC2} (130 V, absolute maximum) provides the actual current to the display load through a high-voltage transistor in the output totem-pole structure. However the bias of that DMOS switch requires a slightly higher voltage (V_{CC2} + 10 V) to be applied to the V_{CC3} input. Often, these two voltages can be obtained from one supply and a few passive components. In addition, it is possible to operate the device with V_{CC2} and V_{CC3} in common, with the only penalty being reduced current source capabilities on the high voltage outputs.

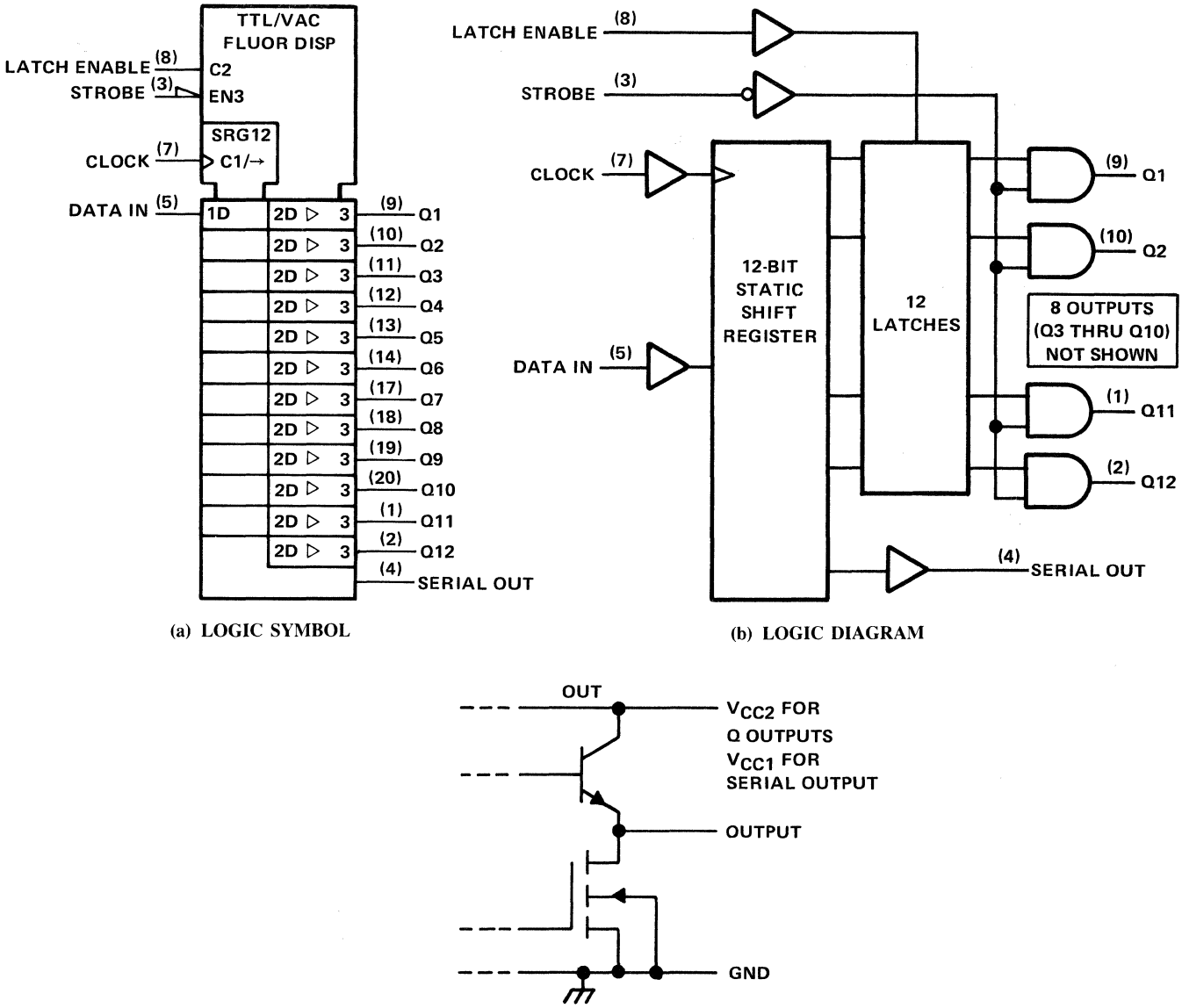


Figure 8-59. SN75512A 12-Bit VFD Driver

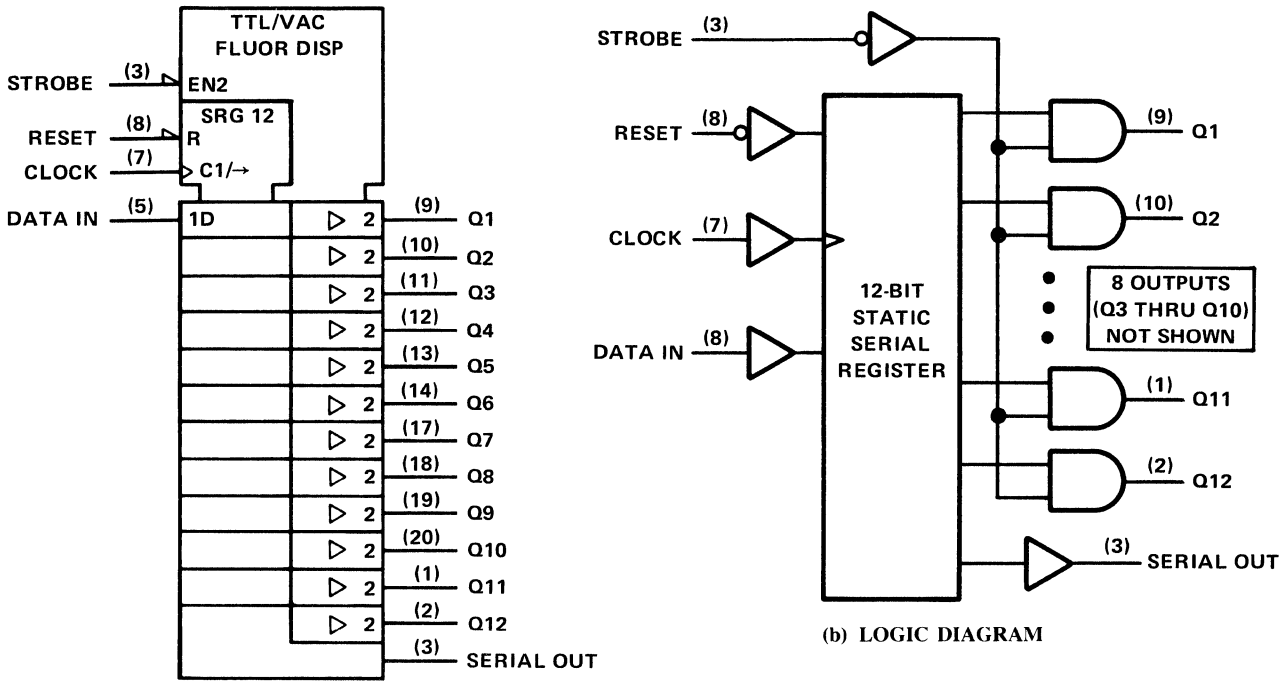
The inputs are directly compatible with CMOS logic and can be interfaced with TTL with the addition of pull-up resistors.

The SN75518 32-Bit VFD Driver (Figure 8-62)

The most cost-effective driver for large displays with many anodes and grids is the SN75518. It is comprised of the same elements as the SN75512A, except it is 32 bits wide rather than only 12: a 32-bit serial-in, parallel-out shift register, 32 bits of parallel latches and 32 DMOS, totem-pole output stages capable of operation to 70 V (absolute maximum). The logical relationships of input clocking, latch enable and output strobe are also identical to the SN75512A. However, the SN75518 has been designed for direct CMOS input compatibility with TTL signals requiring the addition of resistive pull-ups. Power dissipation cannot exceed the 1650 mW limit of the 40-pin plastic package.

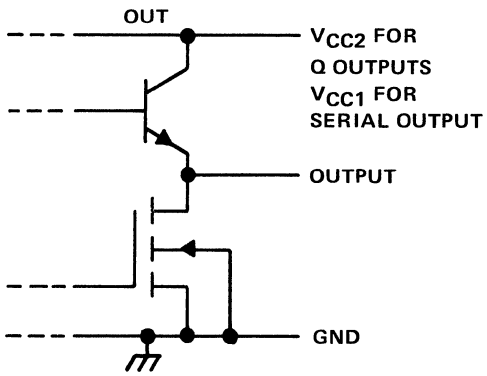
Table 8-4. SN75512A—SN75513A Operational Duty Cycle

Number of Outputs on I_O = 25 mA	Max. Allowable Duty Cycle at Ambient Temperature				
	25°C	40°C	50°C	60°C	70°C
12	77%	68%	62%	55%	48%
11	84	75	67	60	52
10	92	82	74	66	58
9	100	91	82	73	61
8	|	100	93	83	73
7	|	|	100	94	82
6	|	|	|	100	96
5	|	|	|	|	100
1	100	100	100	100	100



(a) LOGIC SYMBOL

(b) LOGIC DIAGRAM



(c) TYPICAL OF ALL OUTPUTS

Figure 8-60. SN75513A 12-Bit VFD Driver

The SN75501C as a 32-Bit High-Voltage VFD Driver

Although designed originally for ac plasma applications, the SN75501C can be used to drive VFDs. The SN75501C is a 32-bit high-voltage display driver. A logic diagram of the SN75501C is shown in Figure 8-63(b). When used as a VFD driver, the strobe input is grounded and the sustain input is operated as an active high strobe input. The 32-bit serial shift register, capable of 4 MHz operation, registers the data on the positive edge of the clock. A logical "1" stored in the register will cause the respective output to pulse high when the sustain input is pulsed high. The outputs of the SN75501C are totem-pole outputs and a serial data output is provided for use in cascading multiple drivers. The use of the SN75501C as a VFD driver should be limited to applications where the IDBT (sustain high) inputs are 74 μs or greater.

VFD DRIVER APPLICATIONS

Driving a Vacuum Fluorescent Character Display

The following application uses a 5 × 7 40-digit VFD by Noritake. Each character is written in a single cycle since all 35 anodes (A1 through A35) of the 5 × 7 matrix are pinned out. The characters (1 through 40) are scanned by selective control of their respective grid, each of which is pinned out (G1 through G40). Respective anodes of all characters (A1 of Char 1 through Char 40) are connected. This format is common to most dot character or segment character displays (Figure 8-64). Multirow displays require additional control. This is usually provided through parallel access to the anodes of each additional row (Table 8-5).

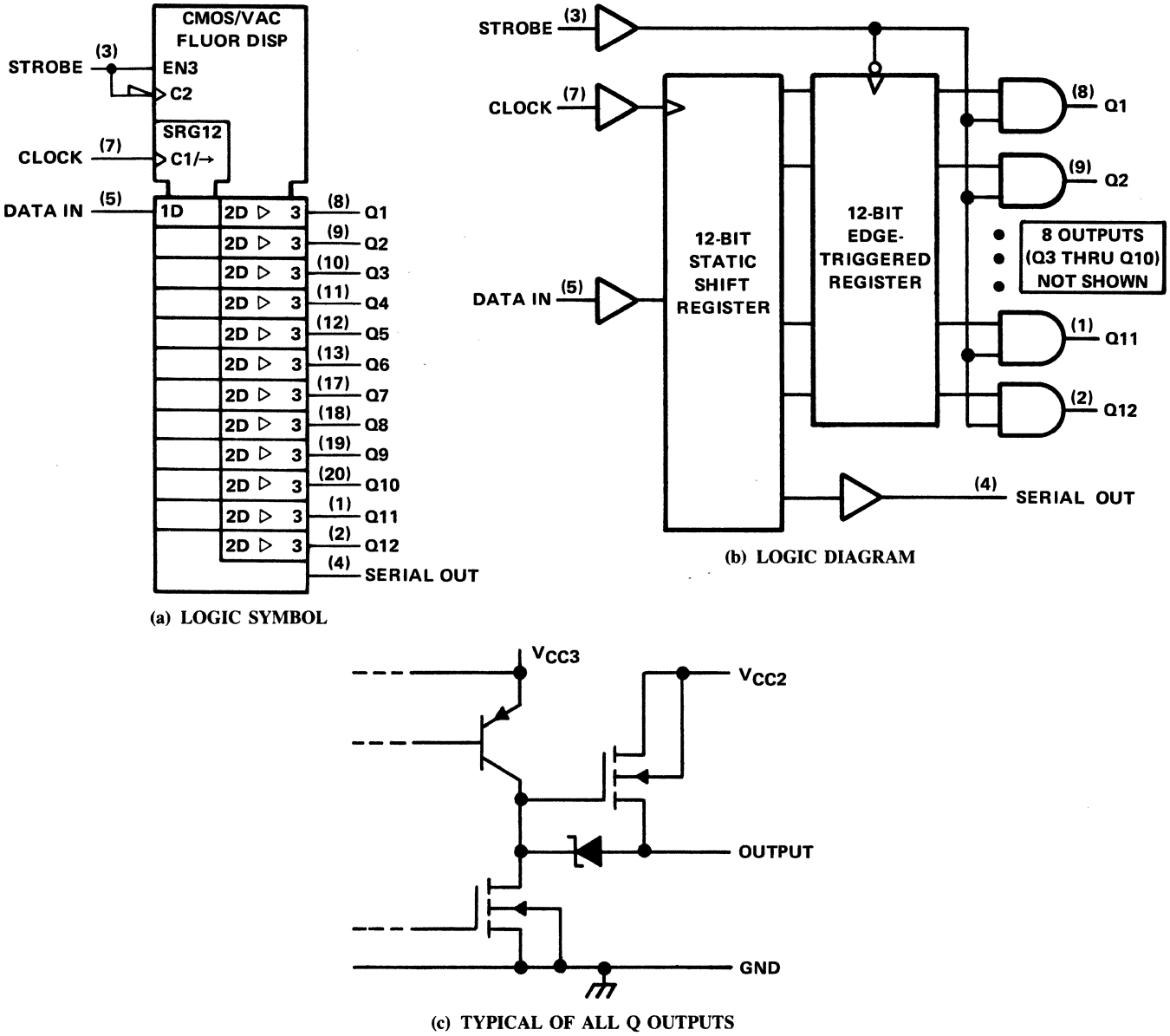


Figure 8-61. SN75514 12-Bit VFD Driver

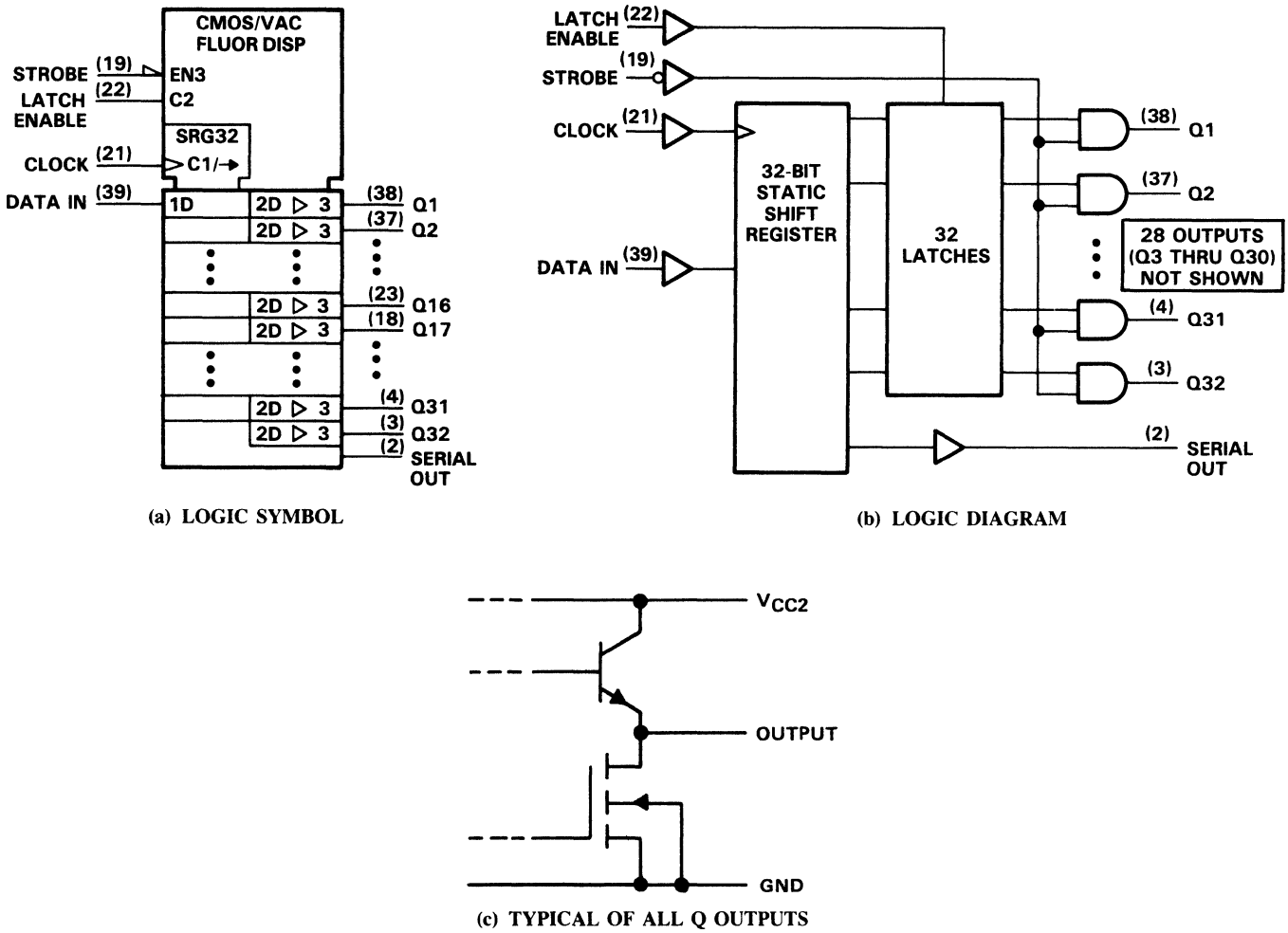
A typical driver scheme for a single line 40:5 × 7 dot character VFD is shown in Figure 8-65.

Whether or not the anode drivers require latched outputs depends on the circuit timing. Figure 8-66 shows a typical timing diagram for the display as shown in Figure 8-65. The drivers remain inactive for 183 μs (IDBT) prior to each character registration. This is more than sufficient time to load the 35 bits of data required for each character. With a 1 MHz data rate, the SN75513A requires only 35 μs to load this information. Modification of the timing to take advantage of the latch capability of the SN75512A for this particular application (1 line — 40:5 × 7 character VFD) will produce only minor improvement in display aesthetics. This is not the case for larger displays. Take for example, a six-line display of similar format (Table 8-5). A six-line display (DC40066A) requires control of 210 anodes (6 × 5 × 7). Thus, unless received in parallel format, this requires 210 μs loading time. With a latched driver however, this presents no problem as new data can be entered independent of the IDBT. Figure 8-67 illustrates a typical timing diagram incorporating this design.

The latch function virtually extends the time allotted for data registration in the anode drivers to the full character cycle time. For a 100 Hz panel refresh rate (T_r = 10 ms) and 1:150 minimum character duty cycle, the minimum character cycle time is 67 μs ($T_p = T_r XDC$ = 10 ms/150). The larger the panel the more complex the anode/grid configuration, the more beneficial the latch feature (as that available with the SN75512A) becomes.

Driving a Dot Matrix Display

As discussed in a preceding section of Panel Performance, several variations of grid/anode configurations exist. The following will present the panel



(a) LOGIC SYMBOL

(b) LOGIC DIAGRAM

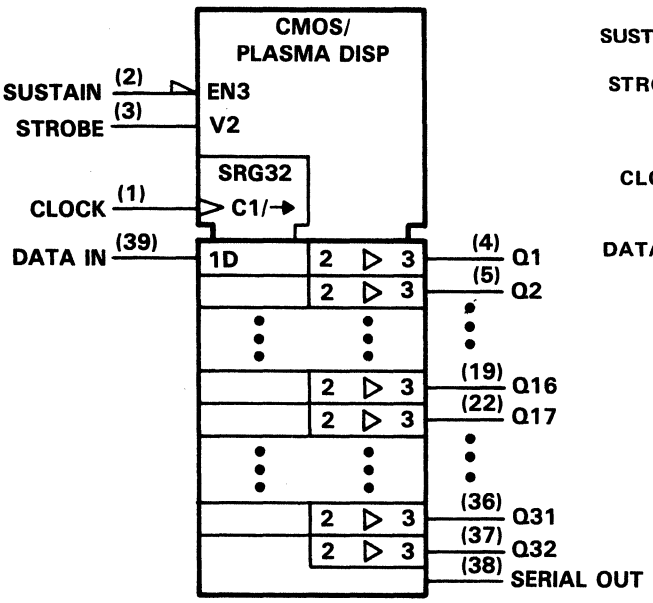
(c) TYPICAL OF ALL Q OUTPUTS

Figure 8-62. SN75518 VFD Driver

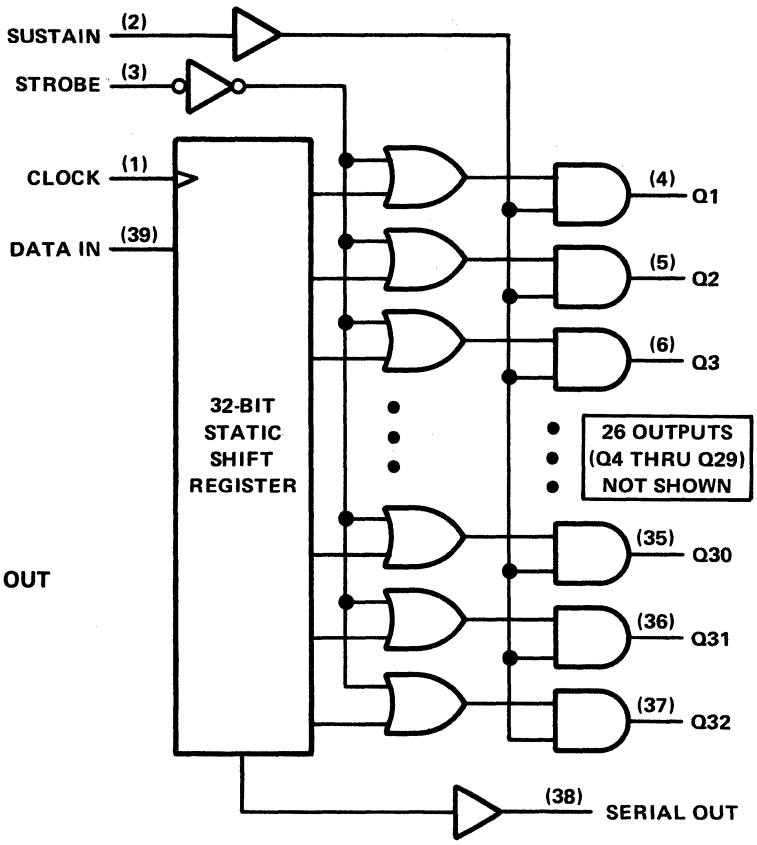
requirements and suggested drive techniques for the displays shown in Figures 8-55(b), (c), and (d).

Figure 8-68 illustrates the VFD grid/anode arrangement for a DM256X64A. This is a 256 × 64 dot matrix VFD by Noritake whose grid/anode configuration is as illustrated in Figure 8-55. Figure 8-69 shows the required timing of the anode and grid signals to properly operate the DM256X64A. As can be seen in Figures 8-68 and 8-69, the active columns are composed of anodes which are between the activated grids. When grids 1 and 2 are activated, columns 2 and 3 are between them, and columns 1 and 4 are outside them. The purpose of this arrangement is to eliminate fringing effects of neighboring grids and thus achieve uniform intensity. Analysis of this configuration also shows requirements on panel drive electronics which are common to the previous examples. If the total panel refresh rate is held to 100 Hz, the total panel period (T_r) is 10 ms. With 128 write cycles required, each write cycle is 78 μs (T_c). Maintaining the 1:150 duty cycle, each strobe signal is 66 μs (T_p). This allows only 12 μs dead time or IDBT which dictates the use of an active pull-down driver. The time between the strobe signals of a particular anode group is 90 μs. This opens options in the VFD driver architecture. Each group of anode drivers requires 64 bits of data and two groups (A & D or B & C) must be loaded during each column write cycle (128 bits). If the SN75512A is used, its latch feature allows use of total strobe cycle period (156 μs), and a 1 MHz data rate allows the data to be received in a serial format. If the SN75513A is used, the A(B) group and D(C) group data must be loaded in parallel (64 μs), since it must be loaded during the dead time between strobe signals. Also available is the SN75501C. Since the strobe signal duty cycle is less than 50%, the SN75501C can also be used. With a 4 MHz data rate, all 128 bits of data can be registered serially in a 32 μs dead time between strobes.

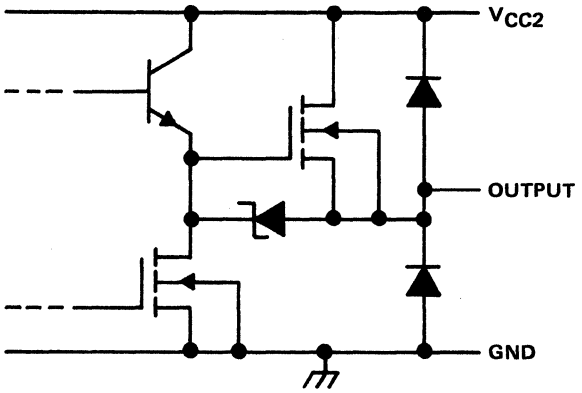
Figures 8-70 through 8-73 illustrate the dot matrix pinout and timing diagrams for the anode/grid configurations shown in Figures 8-55(c) and 8-55(d). Table 8-6 identifies applicable anode and grid drivers and the number required for each of the configurations presented.



(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM



(c) TYPICAL OF ALL Q OUTPUTS

Figure 8-63. SN75501C VFD Driver

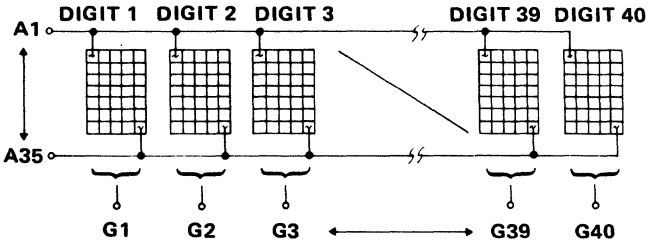


Figure 8-64. A 40: 5 × 7 Dot Character VFD Configuration

Table 8-5. Dot Character VFD Driver Requirements

Control Pins					Required Drivers	
Anode	Grid	Rows	Char	Matrix	10 Bit	12 Bit
35	10	1	10	5 X 7	5	4
	40		40	5 X 7	8	7
60	10		10	5 X 12	7	6
	40		40	5 X 12	10	9
70	10	2	10	5 X 7	8	7
	40		40	5 X 7	11	10
140	10	4	10	5 X 7	15	13
	40		40	5 X 7	18	16
210	10	6	10	5 X 7	22	19
	40		40	5 X 7	25	22

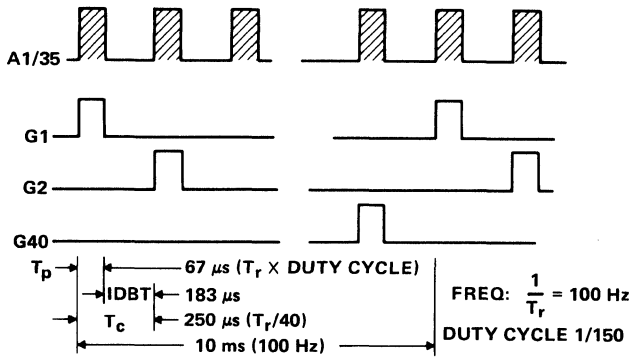


Figure 8-66. A 40 Character VFD Timing Diagram

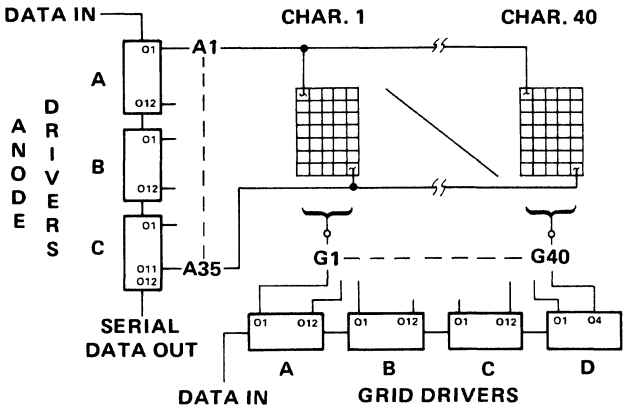


Figure 8-65. A 40: 5 × 7 Dot Character VFD Drive Scheme

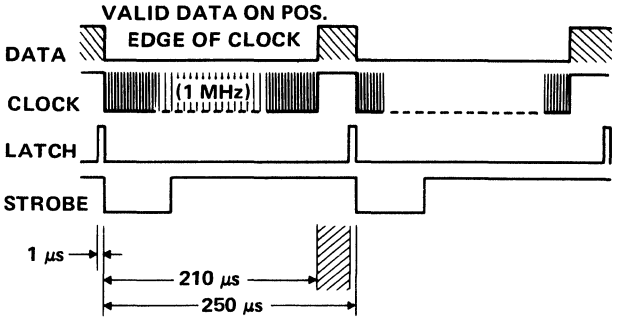


Figure 8-67. Data Registration of an SN75512 12-Bit VFD with Latch

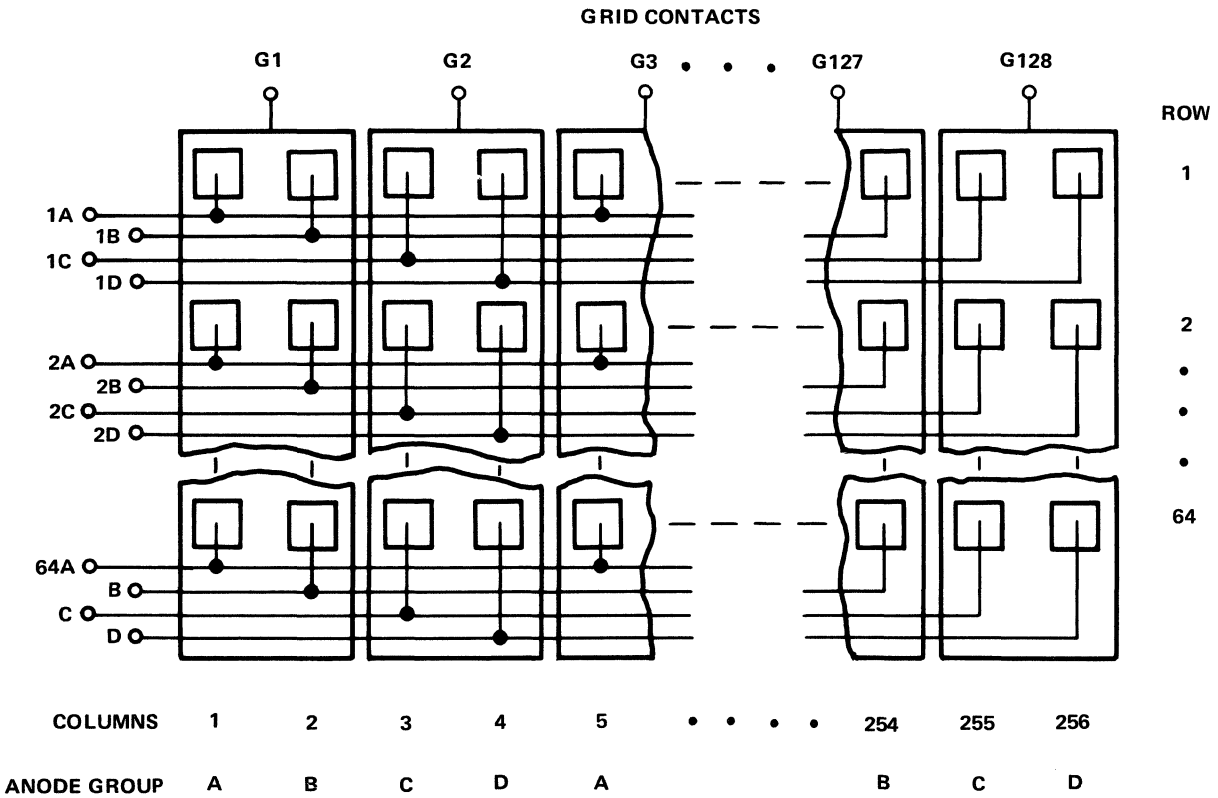


Figure 8-68. A 256 × 64 Dot Matrix VFD Pinout

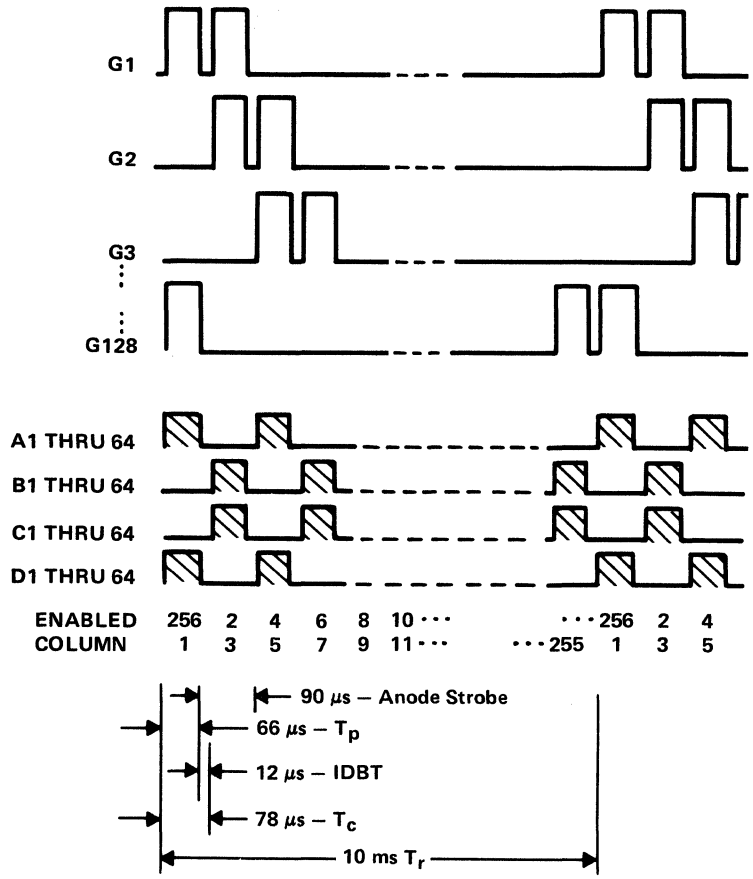


Figure 8-69. Timing Diagram for VFD of SN75512

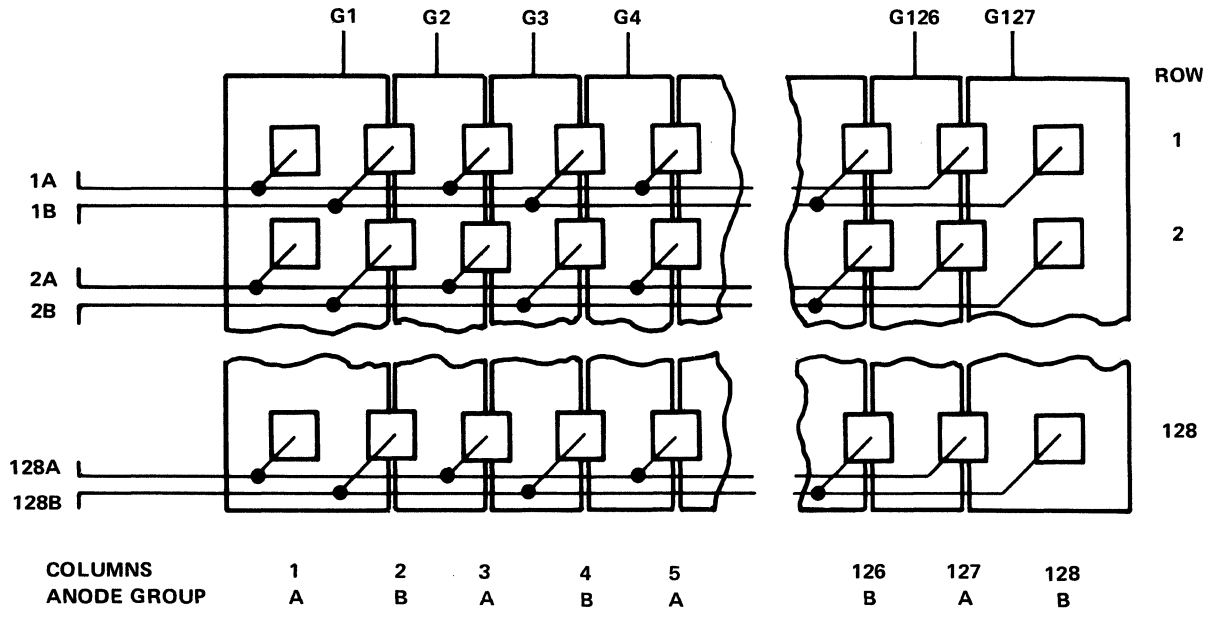


Figure 8-70. A 128 × 128 Dot Matrix VFD Pinout

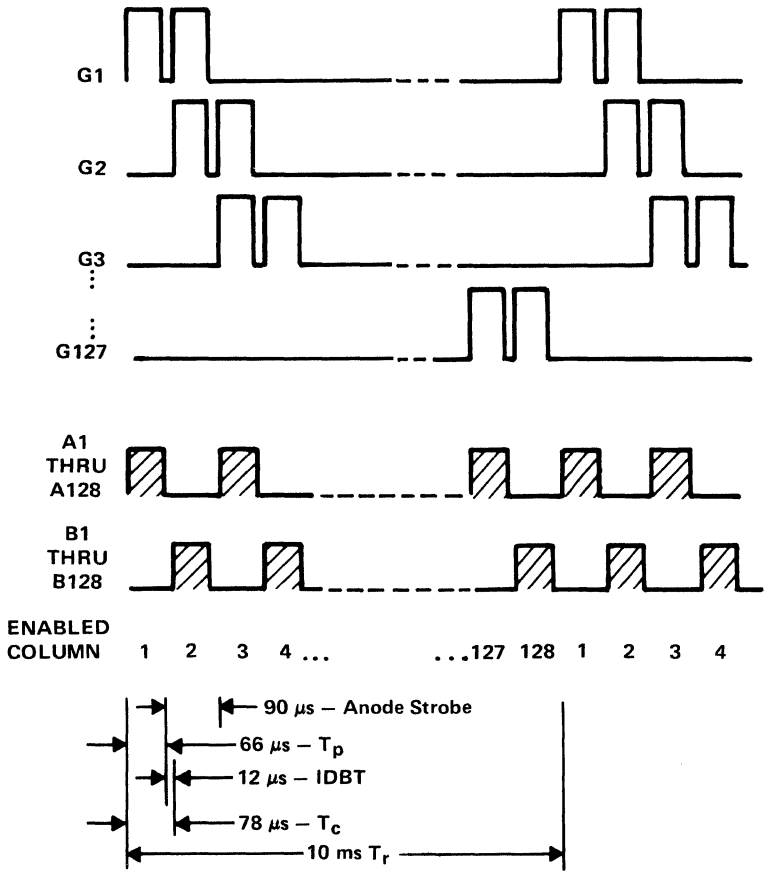


Figure 8-71. Timing Diagram for VFD 1128 × 128 Dot Matrix

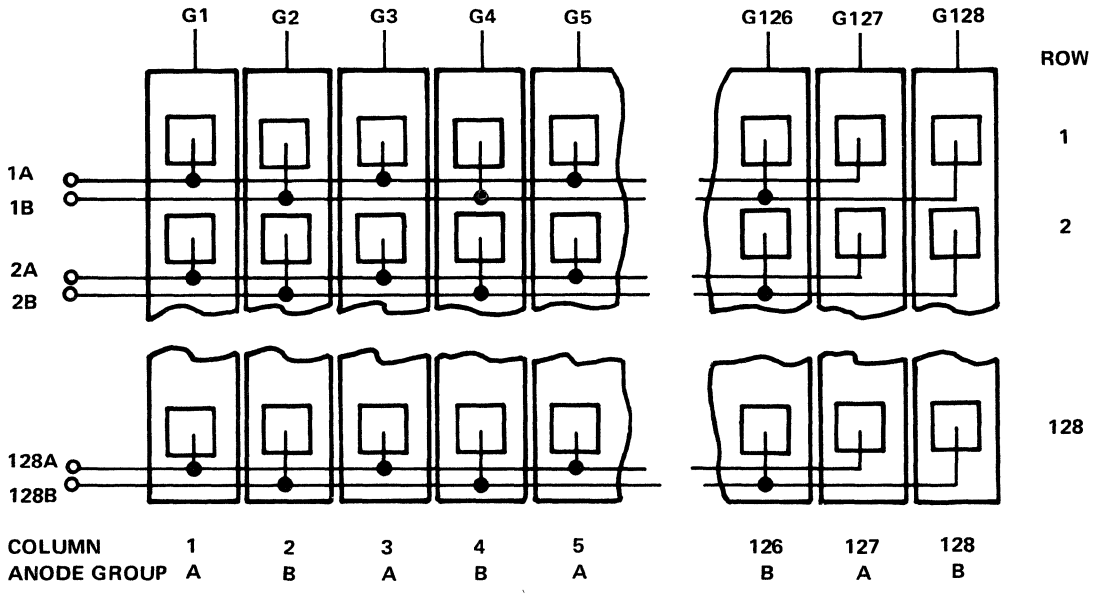


Figure 8-72. A 128 × 128 Dot Matrix VFD Pinout

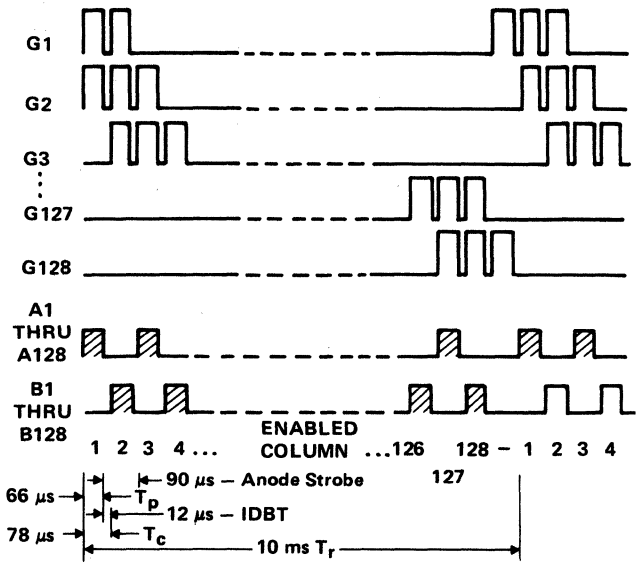


Figure 8-73. Timing Diagram for VFD of 128 × 128 Dot Matrix Pinout

Table 8-6. Dot Matrix VFD Driver Requirements

Display Size	Format Figure	Control Lines Anode	Grid	No. Drivers Required '4810	'512	'513	'518
128×64	8-68	256	64	26+7	22+6	24+6	8+2
	8-70	128	128	14+13	12+11	12+11	4+4
	8-72	128	128	14+13	12+11	12+11	4+4
128×128	8-68	512	64	52+7	44+6	NA 6	16+2
	8-70	256	128	26+13	22+11	NA 11	8+4
	8-72	256	128	26+13	22+11	NA 11	8+4
256×64	8-68	256	128	26+13	22+11	24+11	8+4
	8-70	128	256	14+26	12+22	12+22	4+8
	8-72	128	256	14+26	12+22	12+22	4+8

AC THIN FILM ELECTROLUMINESCENT DISPLAY DRIVERS

AC TFEL DISPLAY TECHNOLOGY

Due to technical advances in the past decade, AC Thin Film Electroluminescent (TFEL) Display technology has matured to the extent that the production of cost-effective reliable displays is a reality. TFEL displays' thinness, durability, compact screen size, and low power requirements are the primary advantages over other display technologies. X-Y matrix panels have been built with line resolutions up to 100 lines per inch and as large as 500 lines per axis. The following sections outline the technology, operation and drive circuitry of TFEL displays.

The AC TFEL display is a solid state device. It is available in several different formats, i.e., segmented character, dot matrix character, large X-Y dot matrix and custom graphic shapes. The basic mode of operation applies an alternating voltage across any two crossing electrodes. When this voltage exceeds the threshold voltage, light is emitted from the luminescent layer. The threshold is considered to be the potential at which any visible light is emitted. A bright yellow light, with a relatively broad spectrum, is emitted. TFEL devices exhibit a view angle of up to 180 degrees and contrast ratios of up to 60:1.

The typical TFEL device is a sandwich structure as shown in Figure 8-74. All layers are transparent except for possibly the back electrodes. If a reflecting back electrode is utilized, the light output will be nearly doubled but the optimum contrast will be lost. A back cover which is sealed to the front glass at the edges of the display is not shown.

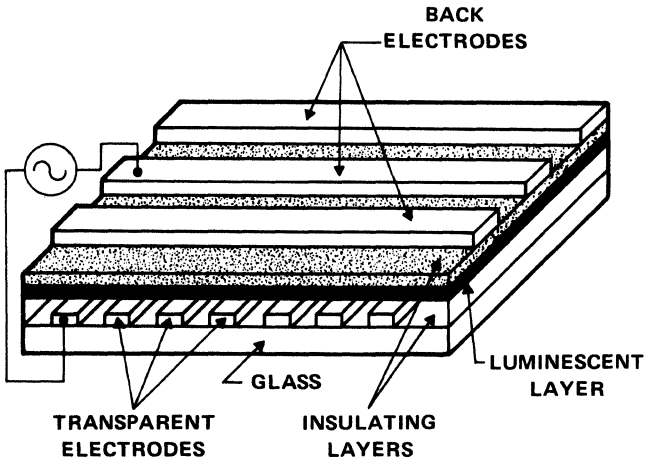


Figure 8-74. TFEL Construction

Mn doped ZnS is most often used for the luminescent layer. It is believed that the Mn centers emit light when excited by high energy electrons. The typical emission spectrum of a Mn doped ZnS TFEL display is shown in Figure 8-75.

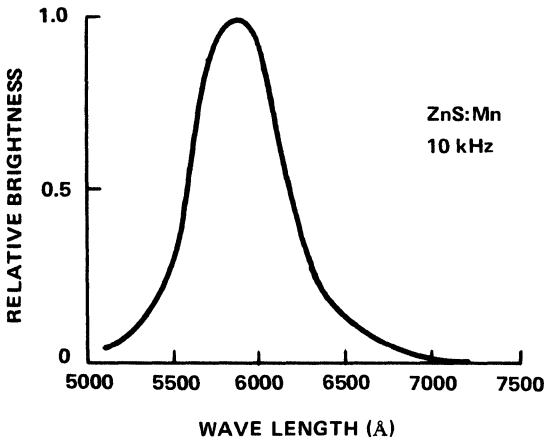


Figure 8-75. TFEL Emission Spectrum

Factors Affecting TFEL Display Brightness

The brightness of TFEL devices is very dependent on the polarity, pulse amplitude, frequency and pulse width of the drive voltages. The brightness of a TFEL

display is very dependent on the polarity of drive voltages, as can be seen in Figure 8-76. Little light is emitted during the second of two emissions if the threshold voltage is exceeded twice in one polarity. If the next pulse is of opposite polarity however, the effective field is increased and electrons are accelerated in the opposite direction (faster than before) resulting in a greater light emission. The dependence of TFEL brightness on voltage and its characteristic hysteresis is shown in Figure 8-77(a).

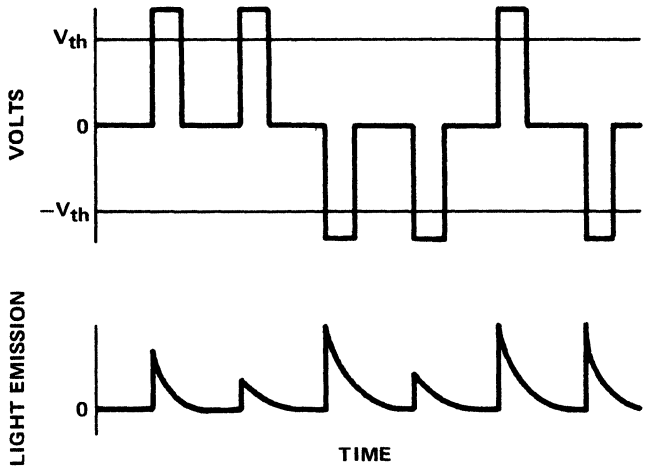


Figure 8-76. Brightness Dependence on Polarity

Simply stated, once the applied voltage pulse exceeds the threshold voltage, the polarity of the next pulse must be reversed to obtain a consistent brightness.

Most TFEL devices are built without the hysteresis feature. The brightness can be altered by operating along the B-V curve as shown in Figure 8-77(b).

Figure 8-77(c) shows the relationship of brightness to pulse width. Once the threshold voltage is exceeded, increasing the width of the excitation pulse causes a dramatic increase in brightness.

Figure 8-78 shows the B-V characteristics of a TFEL panel at different operating frequencies. At frequencies less than 500 Hz, brightness is linear with variations in excitation frequency.

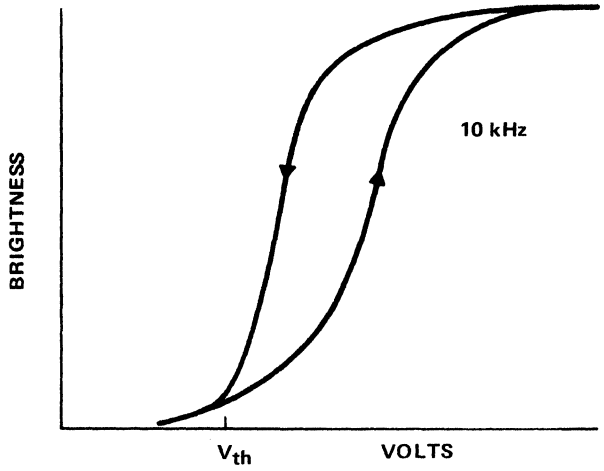
Inasmuch as many applications typically employ a low-frequency refresh drive scheme (60 — 500 Hz), the panel brightness is usually directly proportional to the refresh rate.

AC TFEL Pixel Equivalent Circuit

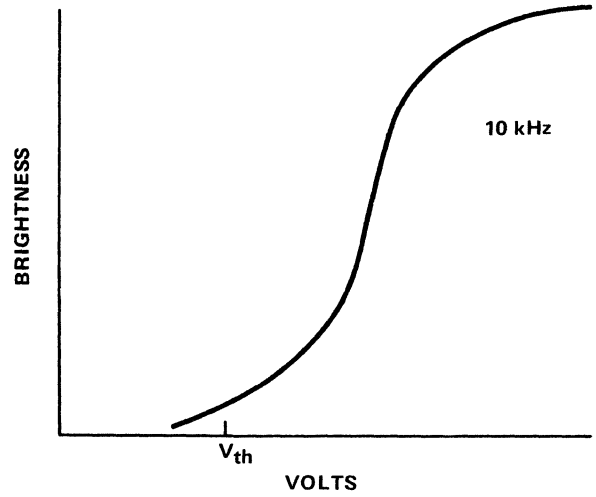
Figure 8-79 is an approximate model for the TFEL pixel. The pixel is highly capacitive due to its physical construction of conductors separated by insulators. The capacitor shunted by a variable resistor represents the luminescent layer where the energy is converted to light.

DRIVERS FOR AC TFEL PANELS

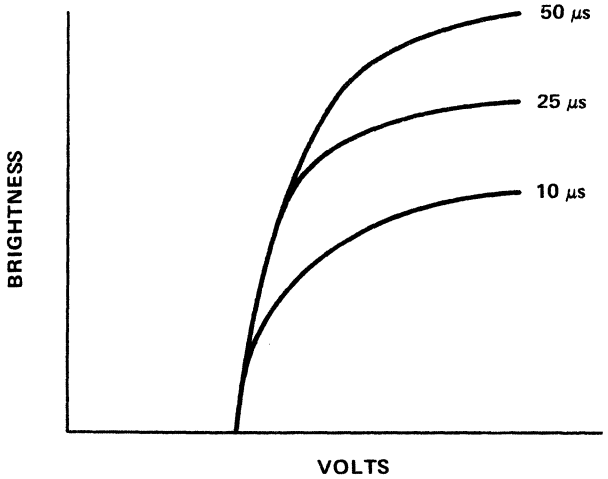
With the pixels organized in X-Y dot matrix configurations most TFEL panels require row (or X axis) drivers and column (or Y axis) drivers. Slightly different control schemes are used for each type of driver resulting in the row and column drivers having somewhat different input logic characteristics.



(a) BRIGHTNESS VOLTAGE HYSTERESIS



(b) BRIGHTNESS VOLTAGE CURVE



(c) BRIGHTNESS DEPENDENCE ON PULSE WIDTH

Figure 8-77. TFEL Device Characteristics

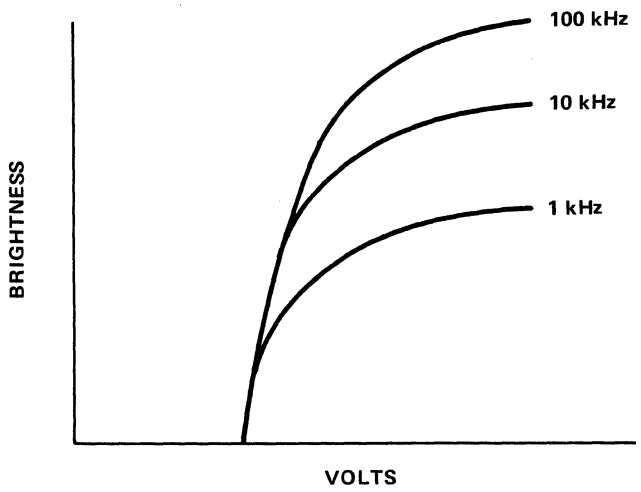


Figure 8-78. Brightness Dependence on Frequency

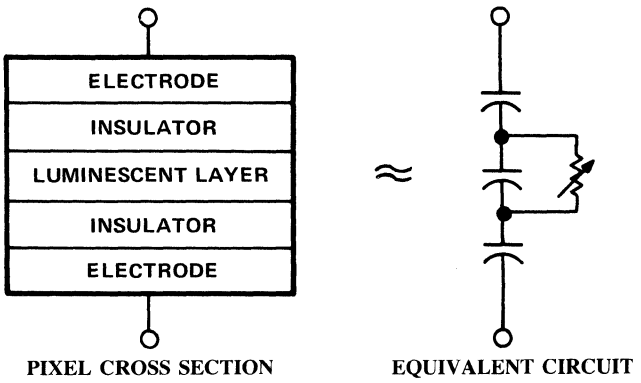


Figure 8-79. Pixel Equivalent Circuit

SN75551 and SN75552 Electroluminescent Row Drivers

The SN75551 and SN75552 (Figure 8-80) are monolithic BIDFET integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence has been reversed from the SN75551 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to the Substrate Common terminal. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high Enable input allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When the Strobe input is low, all output transistors are turned on. The Serial Data output from the shift register may be used to cascade additional devices. This output is not affected by the Enable or Strobe inputs.

SN75553 and SN75554 Electroluminescent Column Drivers

The SN75553 and SN75554 (Figure 8-81) are monolithic BIDFET integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN75554 output sequence has been reversed from the SN75553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

DRIVING AC TFEL PANELS

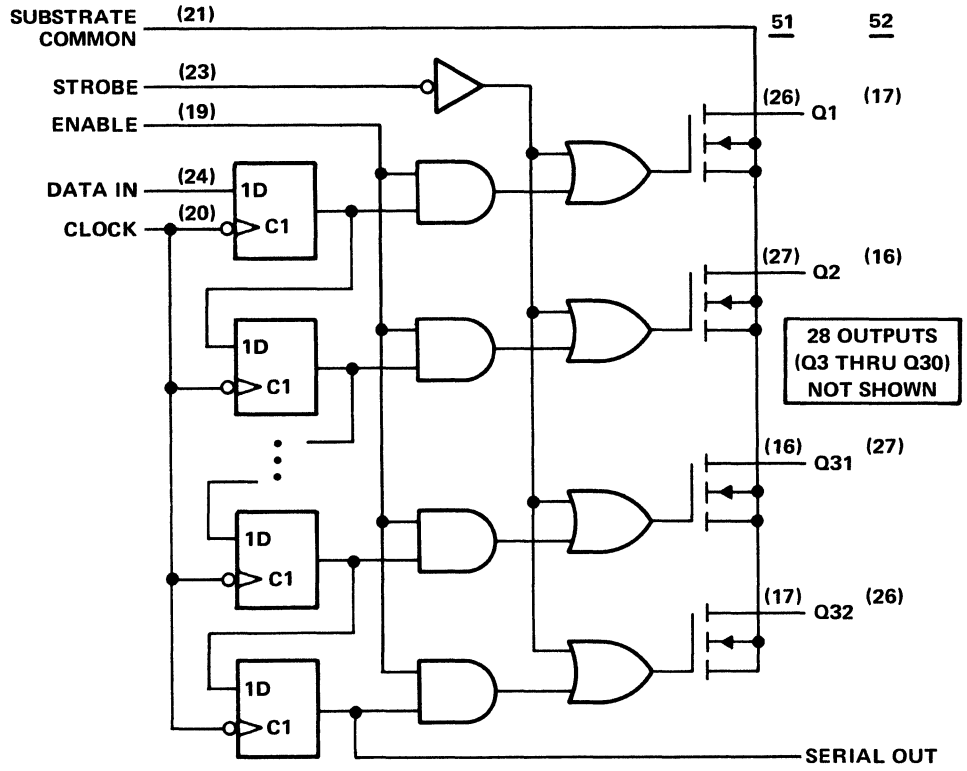
The refresh approach is presently the most popular drive scheme for X-Y matrix panels. Due to the large capacitance of electroluminescent (EL) devices and the energy lost in charging and discharging the capacitive pixel elements, drive frequency has a large effect on power requirements. The refresh approach operates a panel typically at a frequency of 60 to 500 Hz. Most drive schemes operate the EL cells in binary fashion, either off or on. Brightness control or "Grey Scaling" is not incorporated into most simple refresh approaches.

Practical Refresh Drive Scheme

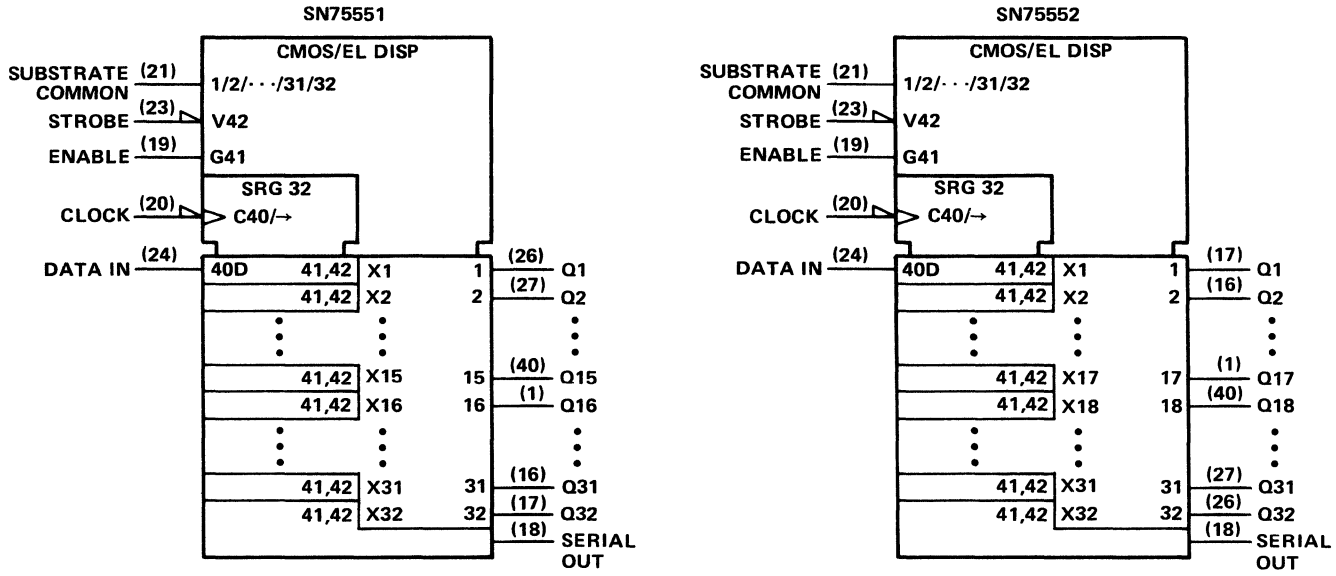
Figure 8-82 shows a block diagram of the drive scheme for a typical EL panel and Figure 8-83 shows the associated waveforms. The Texas Instruments SN75551 and SN75552 EL drivers are used to drive the rows and the SN75553 and SN75554 EL drivers are used to drive the columns. The column drivers are referenced to ground while the substrate common pin of the row drivers is connected to the composite row drive signal and therefore all row signals are relative to the composite signal.

Theory of Operation

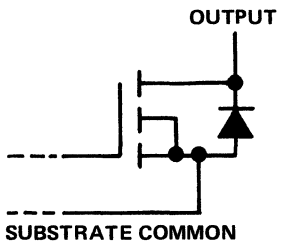
Suppose no light is emitted from a display element when driven by a 200 V pulse followed by a -140 V pulse, but light is emitted when the initial 200 V pulse is followed by a -200 V pulse. Then selective operation can be achieved by applying a pulse train (200 V, -140 V) to the selected row, and coincident to the negative pulse, applying -60 V to the selected columns and 0 V to the nonselected columns. Light will be emitted at the intersection of the selected row and columns. This is due to the selected column potential adding to the selected row potential to effectively create the 200 V, -200 V pulse train. Each row sees a positive pulse (200 V refresh pulse) at the beginning of each scan. The delay between this initial positive pulse and the following negative pulse has little effect upon the brightness.



(a) LOGIC DIAGRAM

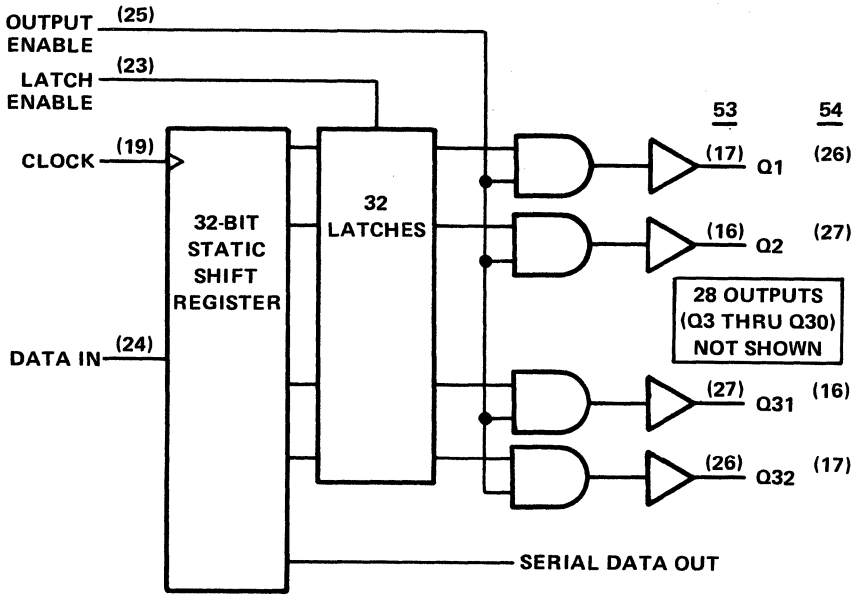


(b) LOGIC SYMBOLS

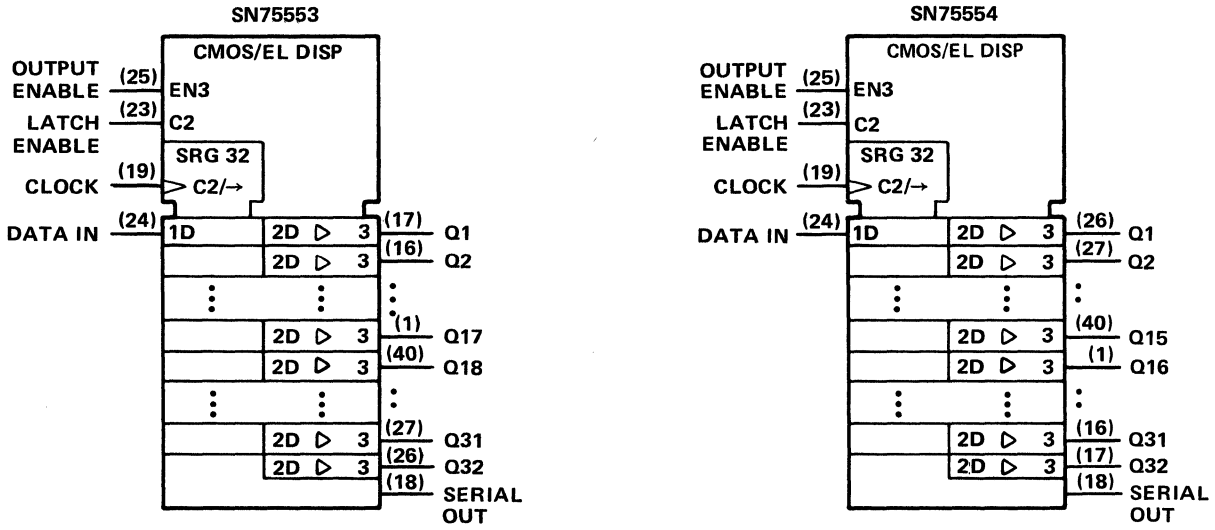


(c) TYPICAL EACH Q OUTPUT STRUCTURE

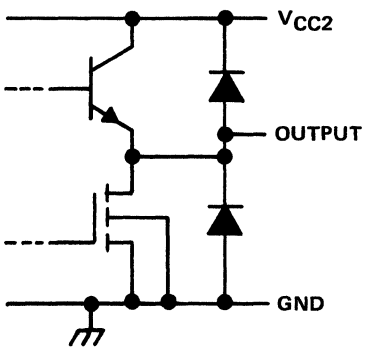
Figure 8-80. SN75551 and SN75552 Electroluminescent Row Drivers



(a) LOGIC DIAGRAM



(b) LOGIC SYMBOLS



(c) TYPICAL OF ALL Q OUTPUTS

Figure 8-81. SN75553 and SN75554 Electroluminescent Column Drivers

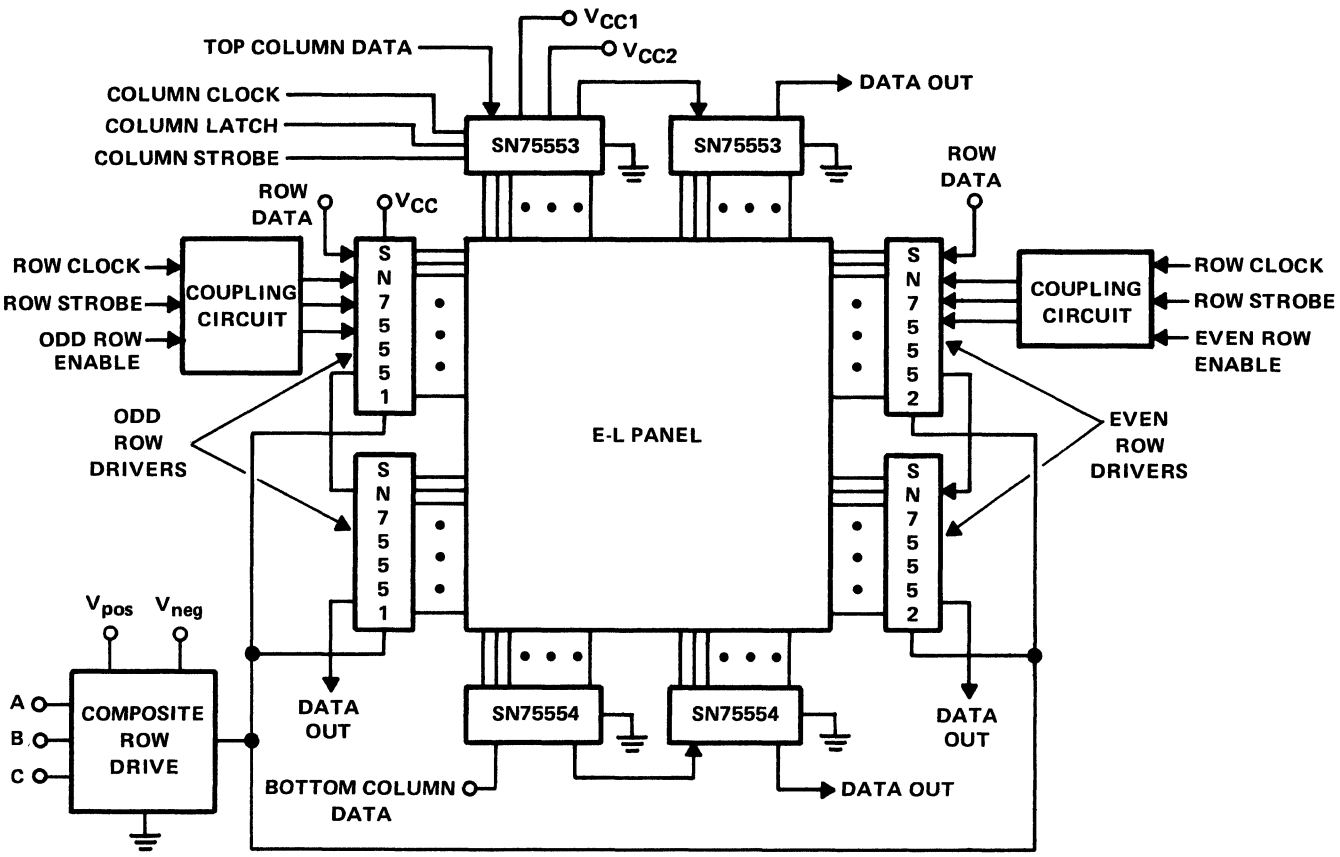


Figure 8-82. Display Block Diagram

Interconnecting the Drivers to the Panel

On most X-Y matrix panels, row electrodes are brought out alternately on opposite sides of the display. The SN75551 and SN75552 devices are identical except that the high-voltage outputs are pinned out clockwise on one and counterclockwise on the other to aid interconnections along the edges of the display. In much the same way, column electrodes are brought out alternately on the top and bottom of the display with the SN75553 and SN75554 column drivers varying only in opposite high voltage output pinouts.

Row Driver Operation

At the beginning of each scan a refresh pulse is applied to all rows. The positive pulse is applied to all rows due to the output structure of the row drivers [Figure 8-80(c)]. When the composite row drive signal goes positive, the clamp diode of each row driver output is forward biased and pulls all of the rows up to follow the composite row drive. Next, the row drivers are strobed, turning on each output's DMOS FET. As the composite row drive returns to ground, the diodes are reverse biased and the rows are pulled to ground with the capacitor discharge current flowing through the DMOS transistors. After a delay to allow the rows to return to ground potential, strobe is removed leaving the rows floating. Each row will continue to float until it is selected. When a row is selected, the associated DMOS FET is turned on to allow the selected row to follow the composite row drive negative transition. Successive rows are selected by clocking one bit of data into the register of the first row driver on each side of the display. (See Figure 8-82) The odd side of the drivers is enabled first, followed by the even side. Then the row drivers are clocked one time and the next even/odd pair is selected.

Column Driver Operation

Before a row is selected, all the data for that line must be clocked into the column drivers and latched. The data for the next lines can be clocked into the column registers as soon as the previous data is latched into the output latches. (See Figure 8-83). The column drivers must be enabled during the time the selected row composite signal goes negative.

Row and Column Driver Requirements

The data signals to the row drivers must be coupled through proper isolation circuitry since the devices are referenced to the composite row drive waveform. An optical isolator can be used as shown in Figure 8-84. The row strobe, row clock and row enable would likely be coupled using an optical isolator. The opposing odd and even row enable signal could be implemented as shown in Figure 8-85. The row data could be generated as shown in Figure 8-86.

The column drivers are referenced to ground. Therefore no special coupling is required for column data signals. It should be noted, however, that even and odd column data must be clocked, latched, and enabled simultaneously.

Row Driver Voltage Supply

The V_{CC} for the row drivers can be created, as shown in Figure 8-87, by using a 12 V regulator. The regulator reference is connected to the composite row drive so that the row supply, V_{CC}, is floating on the composite row drive waveform.

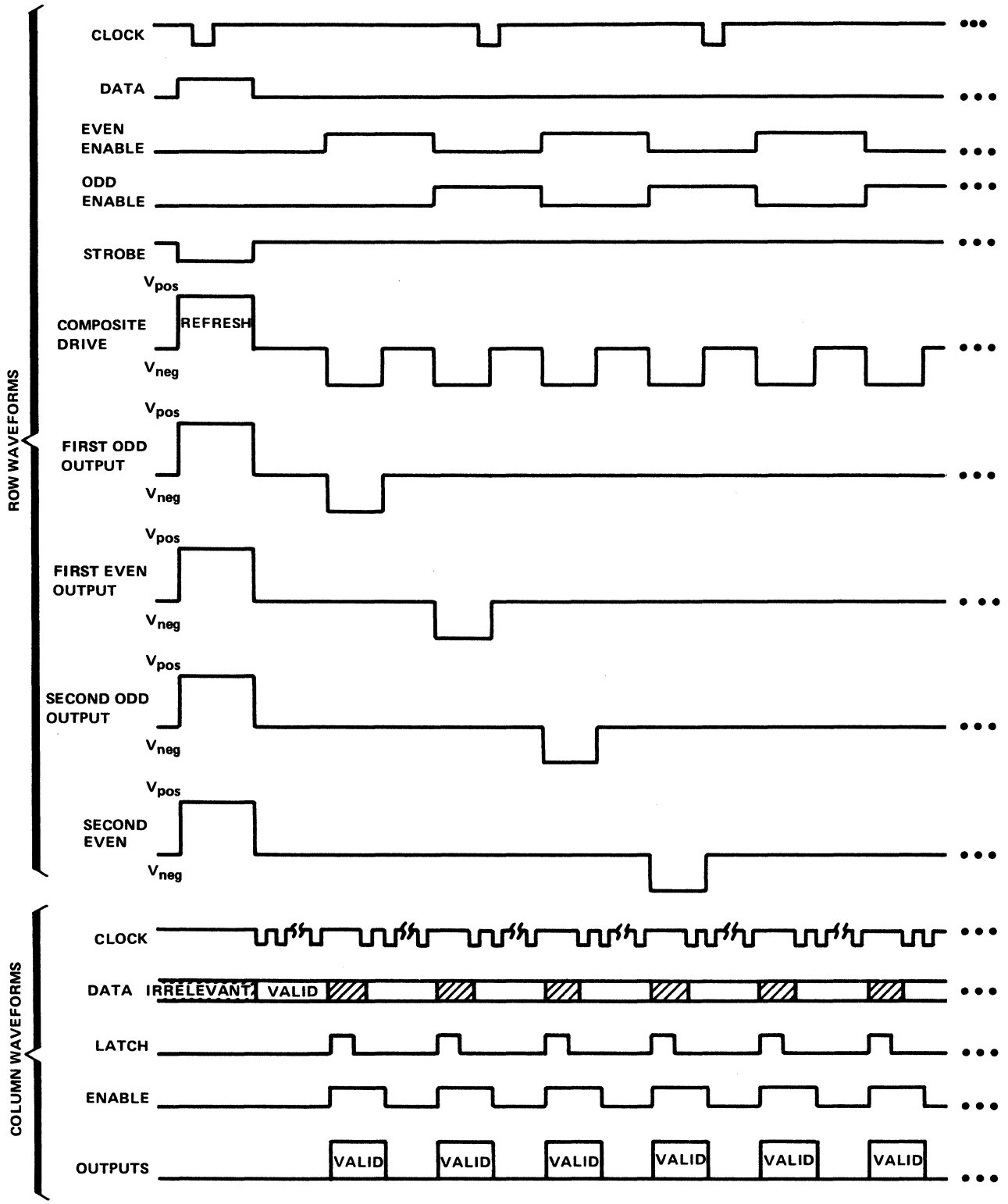


Figure 8-83. Refresh Operation Waveforms

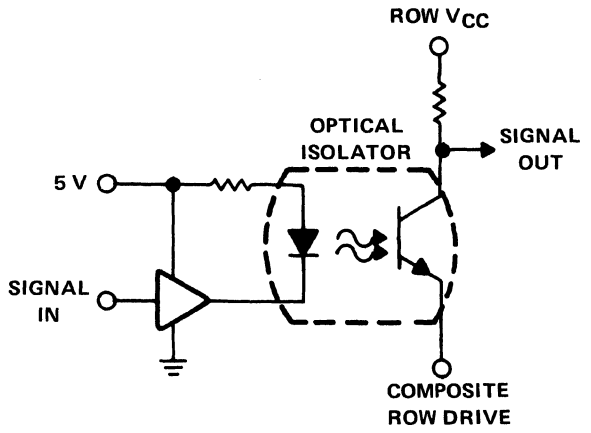


Figure 8-84. Coupling Circuit

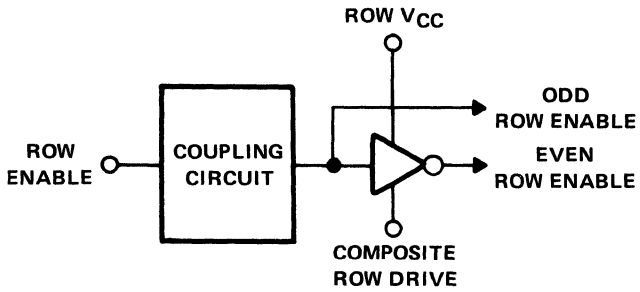


Figure 8-85. Odd and Even Enable Circuits

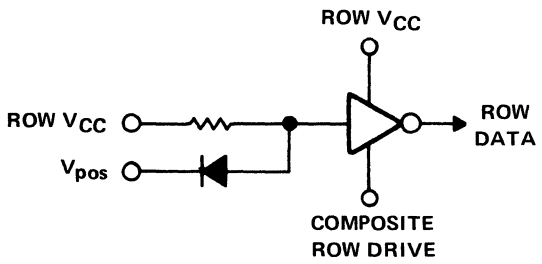


Figure 8-86. Row Data Circuit

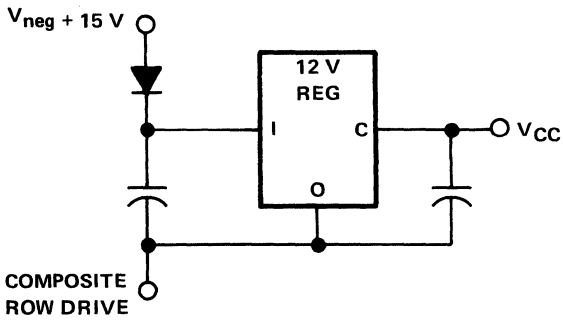
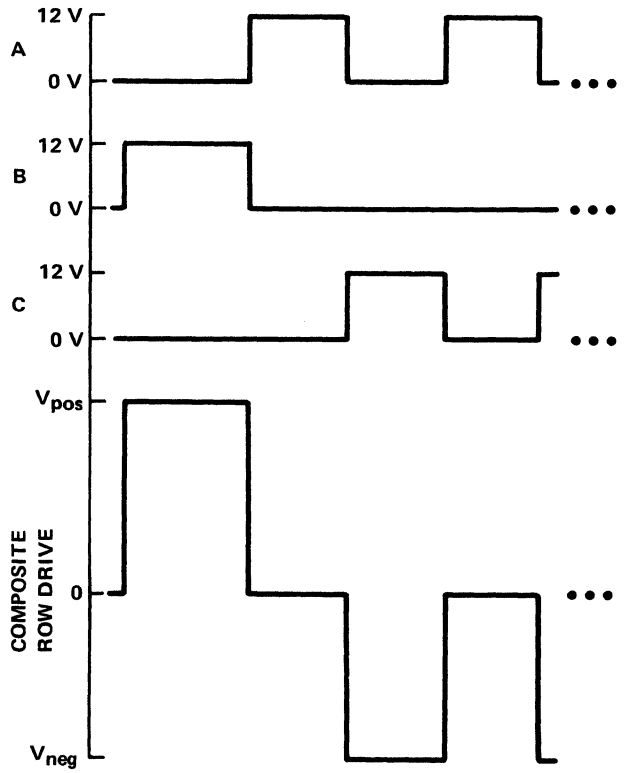


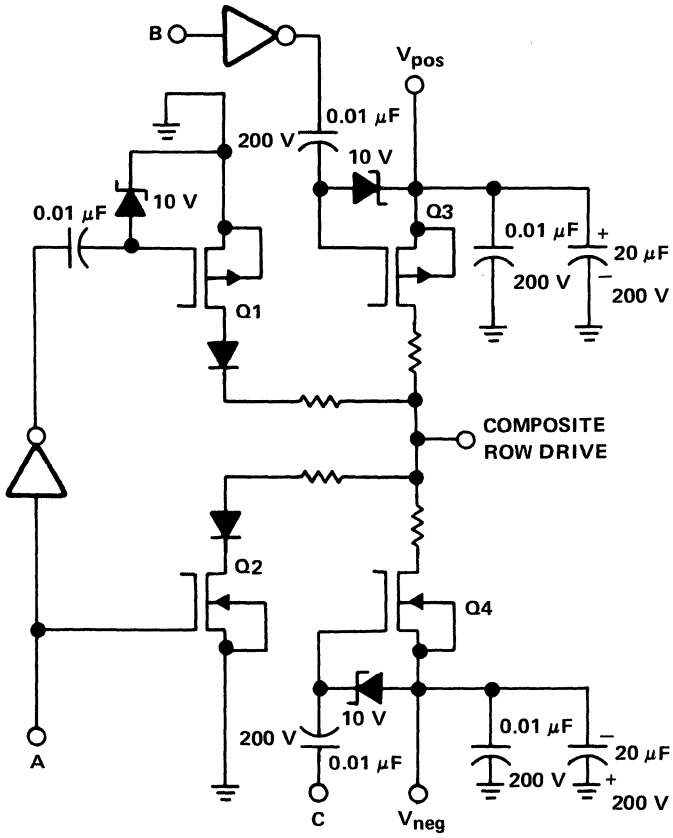
Figure 8-87. Row V_{CC}

COMPOSITE ROW DRIVER

The composite row drive can be generated using four high voltage FETs as shown in Figure 8-88. Q3 pulls the output up to V_{pos} and Q4 pulls the output down to



(a) CONTROL SIGNALS



(b) ROW DRIVE CIRCUIT

Figure 8-88. Composite Row Drive Generation

V_{neg}. Q1 and Q2 are used to bring the output back to ground: Q1 when the output is negative and Q2 when the output is positive. The entire circuit is controlled by using inputs A, B, and C with appropriate non-overlapping control signals.

SPECIFYING DRIVER REQUIREMENTS

When designing an EL drive scheme, it is essential to model the characteristics of the EL device, taking into consideration the drive scheme. The EL designer needs to pay close attention to the current levels required to drive his display and make sure that the drivers can sink and/or source the required levels. The drive current requirements for the refresh drive scheme can be determined by examining worst-case voltage excursions and estimated display capacitance. As reported in *Proceedings of the SID*, vol 23/2, 1982, page 87, the equivalent circuit shown in Figure 8-89 can be used in the analysis of the drive requirements. For purposes of discussion, some simplifying assumptions are made. First, each display element (pixel) is purely capacitive with C = C_e, C_e being the same for all pixels. Next, all points that are at the same potential are treated as if they were connected together.

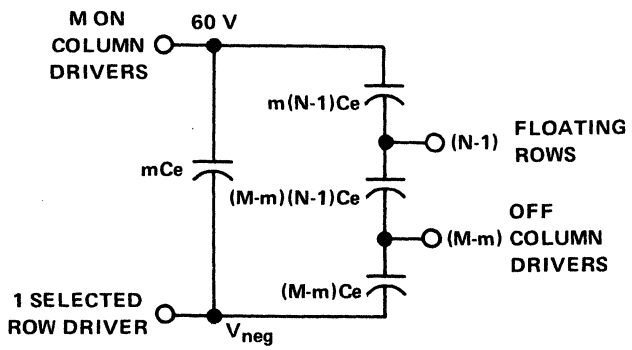


Figure 8-89. Panel Equivalent Circuit

The equivalent circuit shown in Figure 8-89 is for a panel having N rows and M columns. This circuit ignores the negligible capacitance between adjacent rows and between adjacent columns. The panel is driven one row at a time by selecting one of the N rows and m of the M elements in that row. If one row and m columns are selected, the m elements are turned on and the m columns are capacitively coupled to the N minus 1 floating rows. Each of these N minus 1 floating rows is coupled to M minus m off columns which are again coupled to the one selected row. Consider the following example:

Row switch voltage = 200 V
Pull down time = 10 μs
Number of rows = 240
Number of columns = 320
C_e = 4 pF

The worst-case capacitance is when all columns are on. This reduces the equivalent circuit to:

$$MC_e = 320 \times 4 \text{ pF} = 1280 \text{ pF}.$$

Therefore, to satisfy this requirement, the row driver must be able to sink at least:

$$i = C\frac{dv}{dt} = (1280 \text{ pF} \times 200 \text{ V})/10 \text{ μs} = 25.6 \text{ mA}.$$

During the refresh, the row driver would be required to source current through the clamp diode. Since all the N rows are pulled up, the equivalent circuit is as shown in Figure 8-90. The worst case is when all the rows are at zero volts and all are switched to V_{pos}. Suppose V_{pos} is 200 V and a 10 μs rise time is required, then the clamp diode must be able to deliver at least:

$$i = C\frac{dv}{dt} = (4 \text{ pF} \times 320 \times 200)/10 \text{ μs} = 25.6 \text{ mA}.$$

The current requirements for the column drivers can also be calculated as above.

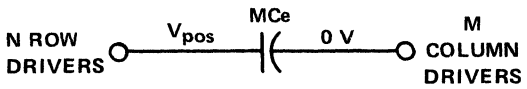


Figure 8-90. Refresh Equivalent Circuit

Section 9

Data Transmission

GENERAL PURPOSE DATA TRANSMISSION

The ever increasing use of computers, microprocessors, and elaborate logic control systems constantly present designers with the problem of transmitting digital data from one system to another. Digital communications between components of systems ranging from machine controls in a factory to consumer appliances and automotive systems have made data line drivers and receivers as prevalent as power supplies.

Many systems use a central computer or controller with several remote terminals or control points. Remote stations may be a few feet or thousands of feet from the central computer. Even small independent systems will usually have one or more pieces of peripheral hardware such as a printer located at some, usually short, distance away. The need for dedicated data transmission products became more apparent as the industry matured. At first, simple single-ended data transmission was used; products were basic and often tailored for each specific system. Then widespread data transmission required system compatibility, and industry standards were adopted. Before addressing the standards and their applications, we will look at the basic line circuit requirements and general purpose data line drivers and receivers.

GENERAL REQUIREMENTS

Basic requirements for a good data transmission system include:

Speed: Data capabilities of up to 10 MHz are desirable for most systems. Frequency of operation is often expressed as data frequency (bits per second). Each cycle has both logic levels, so bps is twice the frequency in hertz. Data transmission speeds in this text are generally expressed in bps.

Power Supplies: Single 5 V supplies are the most popular although dual ±5 V, ±9 V and ±12 V are sometimes required.

Logic Compatibility: TTL compatibility is understood although many devices are also compatible with low-power/low-level CMOS.

Drivers: Capable of driving low-impedance transmission lines. Able to withstand line voltages up to the V_{CC} supply levels.

Receivers: Good input sensitivity, typically less than 500 mV. Provide immunity to noise either with common-mode rejection capabilities or threshold hysteresis.

Lines: Uniform impedance characteristics over the length of the line allowing proper termination for high speed transmission without error-generating reflections.

TYPES OF TRANSMISSION LINES

Transmission lines are often the key to successful data communications. Popular line types include coax cable, twisted pairs, shielded twisted pairs, flat or ribbon cable and discrete wires for short line applications.

Single Wire and Ground Plane

A single wire connection between a driver and receiver (see Figure 9-1) may be satisfactory in some simple system applications. For example, the output of one gate is driving the input of another located on the same PC board or a board nearby. Distances between drivers and receivers must be short and the system relatively free from switching transients or similar electrical noise. Distance limitations, dependent on system noise levels and operating speeds, are approximately three to six inches for most applications.

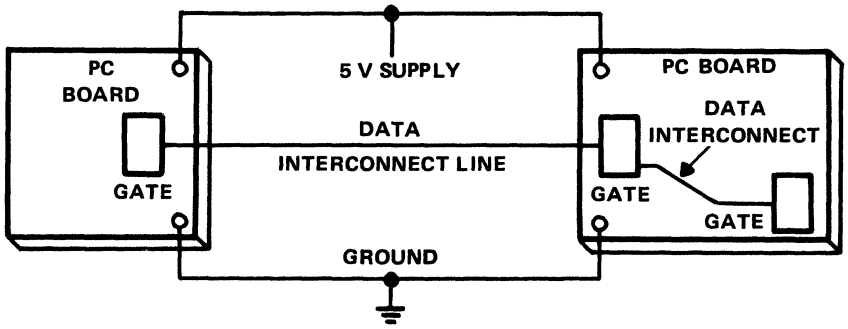


Figure 9-1. Single Wire and Ground Plane

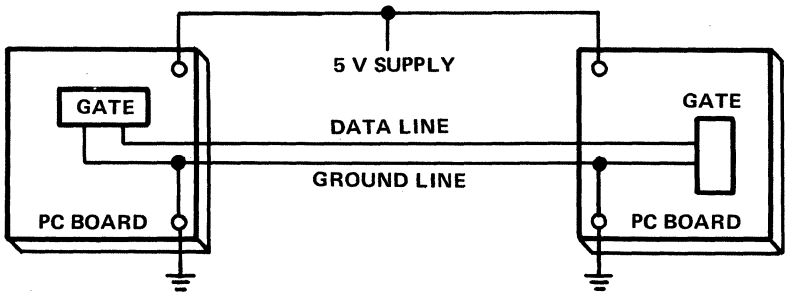


Figure 9-2. Double Wire

Two Wire Interconnect

Nontwisted-dual-wire interconnects (see Figure 9-2) are seldom used. The second wire serves as ground and application limitations are similar to those for single wires. A variation of the two wire interconnect is found in ribbon cable (Figure 9-3). Two adjacent wires are used, one as the signal lead and the other as ground.

Because of the uniform characteristics of ribbon cable, grounding every other wire results in a uniform impedance for all signal wires. Proper termination will then allow relatively high data rates without ringing or bad reflections.

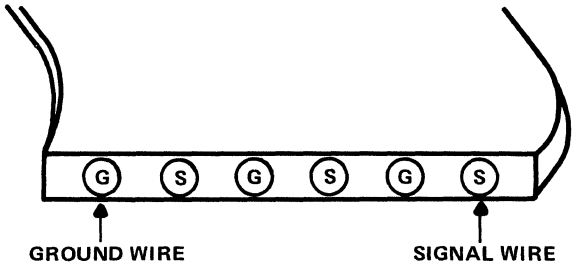


Figure 9-3. Ribbon Cable

Twisted Pair

When two wires are uniformly twisted, the result is a definite impedance characteristic that is uniform along the length of the line (Figure 9-4).

System noise is reduced by the mutual coupling of the twisted wires. It should be noted that grounding both ends of the ground wire may result in little magnetic field protection due to ground loop noise currents. Grounding the high impedance (receiver) end only, as shown, will result in good noise reduction. Twisted pair lines are also used in balanced transmission applications where both wires serve as signal leads (Figure 9-5).

As data rates approach 100 kHz or greater and line lengths are longer, over 50 ft, twisted pair lines have proven to be advantageous over the other types. Following are a few advantages of twisted pair lines:

1. Cancellation of noise due to mutual coupling of adjacent lines in the twisted pair.
2. Both wires in the pair are equally affected by electromagnetically and electrostatically coupled noise resulting in a net common-mode noise voltage with respect to ground. This is easily rejected by balanced differential receiver inputs.
3. Voltage differences between driver/receiver locations will appear as common-mode signals and be rejected by the receiver.
4. Uniform impedance characteristics along the line make it easy to terminate.
5. Twisted pair lines are low cost with long life, and are mechanically very rugged.

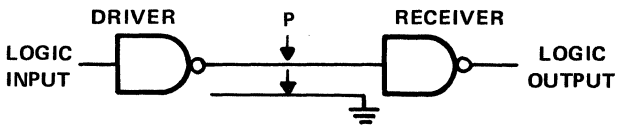


Figure 9-4. Twisted Pair Lines

The voltage across an impedance terminating a transmission line is a function of the real and imaginary components of the impedance, the characteristic impedance of the line, and the incident power. When the line terminating impedance is purely resistive (in practice, the reactive components of impedance can usually be neglected) the transmission line may be described by the following equations (see Figure 9-6):

$$P_R = P_I \left(\frac{R_L - Z_O}{R_L + Z_O} \right)^2 \quad (1)$$

$$P_L = P_I - P_R = P_I \left[1 - \left(\frac{R_L - Z_O}{R_L + Z_O} \right)^2 \right] \quad (2)$$

$$V_L = \sqrt{P_L R_L} = \sqrt{I_L^2 R_L^2} \quad (3)$$

Where:

P_I = Incident Power
P_R = Reflected Power
P_L = Power Delivered to R_L
R_L = Load Resistance
Z_O = Line Characteristic Impedance

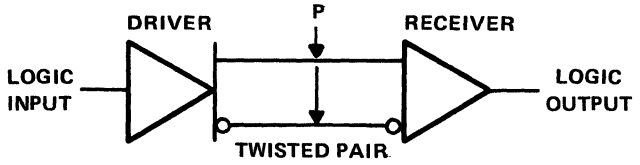


Figure 9-5. Balanced (Differential) Driven Twisted Pair

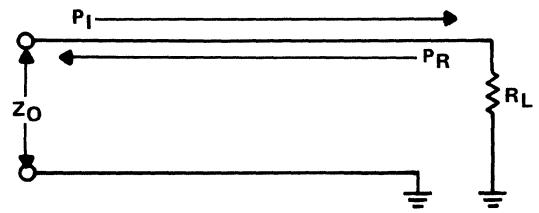


Figure 9-6. Line Incident (P_I) and Reflected (P_R) Power

When $R_L = Z_O$, the numerators of the fractional terms in equations 1 and 2 become zero and the reflected power is zero. With reflections reduced to zero, a major source of signal distortion and noise is eliminated.

In line circuits design R_L is actually a lumped value representing the combination of termination resistor (R_T) and the input resistance of a line receiver, R_{IN}, (Note Figure 9-7). When $R_{IN} >> R_T$, large induced power transients are shunted to ground by R_T, decreasing the maximum power absorbed by the input of the receiver.

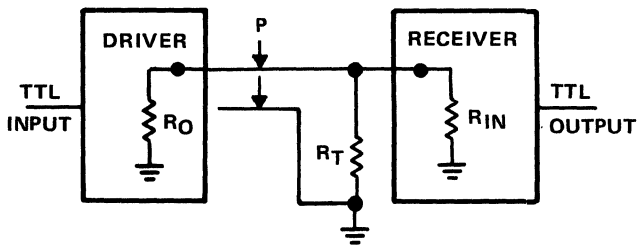


Figure 9-7. Basic, Single Ended, Line Terminations

Figure 9-7 illustrates the basic resistive termination of a single-ended data transmission line. The values of R_O and R_T have a definite effect on circuit performance as is seen in Figure 9-8.

The line used is a 100 Ω twisted pair line. Case A is correctly terminated and results in best performance. Irregularities in other case examples are a result of reflections on the data line due to mismatched termination values.

Figure 9-9 shows the results of a Case C operation at a line length of 50 ft and data rate of 5.4 Mbps. Although the bit rate achievable with this type of mismatched termination is high, reflections result in ringing on the line and false triggering of the receiver.

Noise sources and interference that result in lost or improper data are produced in many ways. Induced pickup on the line, as seen by the receiver, may result in distortion and general interference. Balanced or differential line techniques greatly reduce the effects of common-mode noise but proper line terminations are critical to good operation.

CASE	R_O	R_T
A	100 Ω	100 Ω
B	∞	100 Ω
C	∞	122 Ω
D	∞	205 Ω

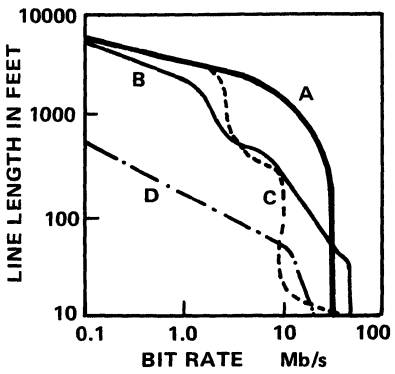


Figure 9-8. Effects of Line Terminations

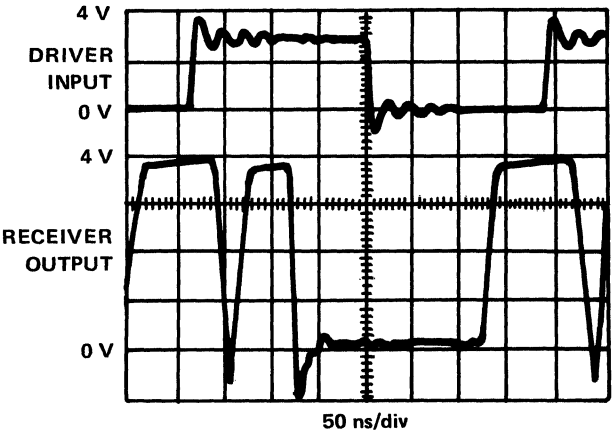


Figure 9-9. Case C Voltage Waveform

Noise induced into the line from electromagnetic or electrostatic sources is an energy source that will generate interference voltage amplitudes proportional to the line to ground impedance. In short lines with low interference energy levels, the typical termination for balanced lines (Figure 9-10) is directly from Line A to Line B. Line termination value (R_T) should equal the characteristic impedance of the line (Z_O) assuming a receiver input resistance (R_{IN}) that is much larger than Z_O. As can be seen from the equivalent circuit in Figure 9-10, the resistance path from each line to ground is very high. With relatively high line to ground impedance the resulting induced noise voltage levels will be high.

The termination technique shown in Figure 9-11 splits the line termination by placing a resistor from each line to ground with a value of 1/2 Z_O. Now the resistance to ground is low, approximately equal to R_{T1} or R_{T2}, and the resulting common-mode voltage is much lower than that generated in the circuit shown in 9-10. A typical twisted pair line has a characteristic impedance of about 120 Ω and typically $R_{T1} = R_{T2} = 62$ Ω.

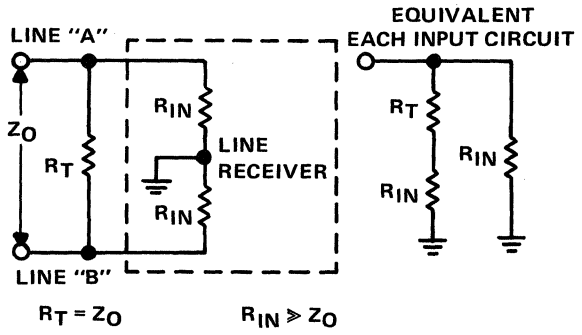


Figure 9-10. Line-to-Line Termination

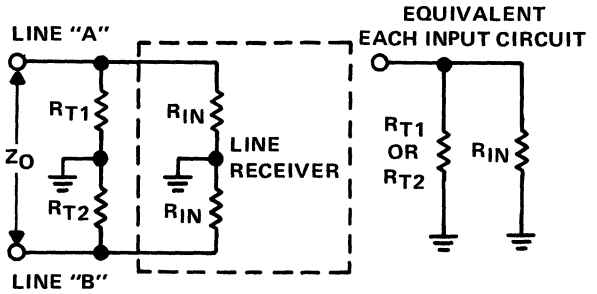


Figure 9-11. Termination to Ground

Noise induced into the balanced twisted pair lines may result in significant levels of noise voltage, but it is common to both lines. This type of noise voltage is referred to as common-mode noise having the same amplitude, at any instant, on both lines. Differential line drivers and receivers will reject common-mode voltages. Further discussion of this will occur later in the text. Twisted pairs are available in ribbon cable (Figure 9-3) as well as discrete pairs and shielded pairs. Shielding yields better noise immunity, if grounded properly, but results in much higher distributed capacitance which significantly attenuates the transmitted signal at high frequencies. If a shielded twisted pair is used (Figure 9-12) grounding the shield at the receiver end only will provide the least signal attenuation and the best rejection of unwanted signals.

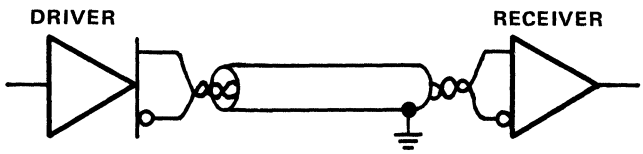
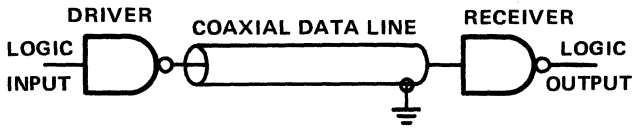


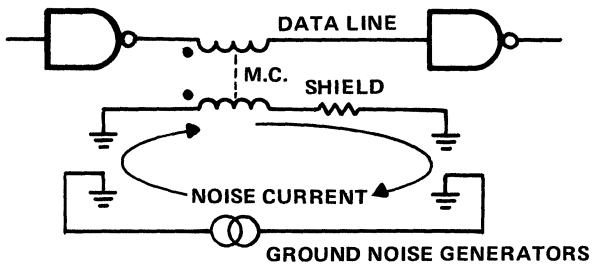
Figure 9-12. Shielded Twisted Pair Transmission

Coaxial Lines

Popular 50 to 200 Ω coaxial cables [Figure 9-13(a)] have a very uniform and definite impedance and offer the best transmission line characteristics for single-ended applications. Primary advantages are low loss and good shielding against magnetically induced interference. As with the shielded twisted pair lines, the coax line's shield should be grounded at the receiver end only. If the shield is grounded at both ends, very little magnetic field protection is possible due to mutual coupling of noise currents in the shield [Figure 9-13(b)].



(a) CORRECT SHIELD GROUNDING



(b) INCORRECT SHIELD GROUNDING

Figure 9-13. Coaxial Data Lines

LINE DRIVERS

Probably the most common single-ended application is the transmission of data from one logic gate directly to another. Standard TTL gates can operate at frequencies up to 20 MHz. However, interconnects must be short (a few inches), and special care taken to assure adequate noise margin and minimum line reflections. The higher speeds of ECL and Schottky TTL gates place even more emphasis on properly terminated, well-shielded lines.

Driving directly from a TTL type gate has several limiting factors. Output currents are too small for long lines terminated in their characteristic impedance.

Another factor to consider in the use of gates is the environmental noise level. It can be seen in Figure 9-14 that negative-going noise peaks greater than 0.4 V and positive-going noise peaks greater than 0.4 V may result in false triggering. The guaranteed noise margin is therefore ±0.4 V when using standard TTL gates.

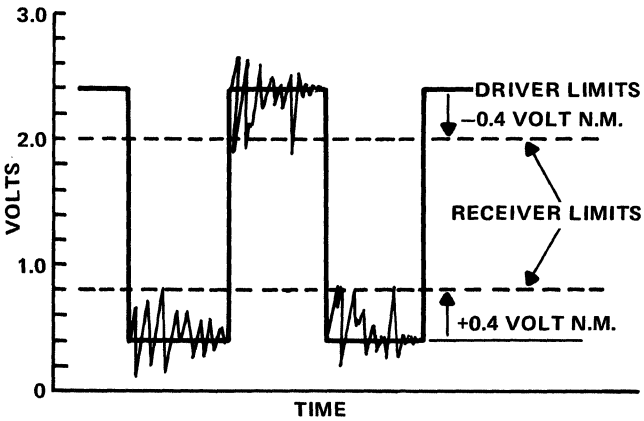


Figure 9-14. TTL Gate Noise Margins

Basic Driver Modes

Data line drivers operate as voltage-mode or current-mode devices. Voltage-mode drivers are active switches used to transfer a voltage from a supply line to the transmission line directly (Figure 9-15) or to switch the transmission line to ground, (Figure 9-16) removing voltage that has been supplied through a termination resistor. In each case the primary drive current required is determined by the termination resistance and voltage drive levels required. Drive current requirements typically range from 25 mA to as high as 100 mA, depending on the application. The three basic types of voltage-mode driver outputs are active pull-up (Figure 9-15), active pull-down (Figure 9-16), and a combination referred to as "totem-pole" (Figure 9-17).

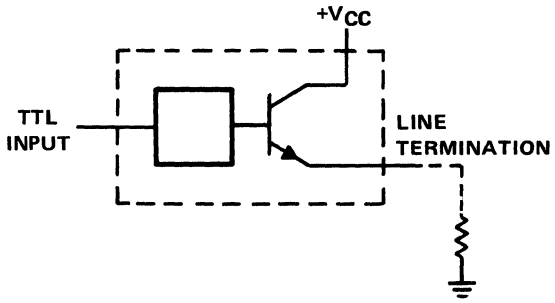


Figure 9-15. Active Pull-Up Configuration

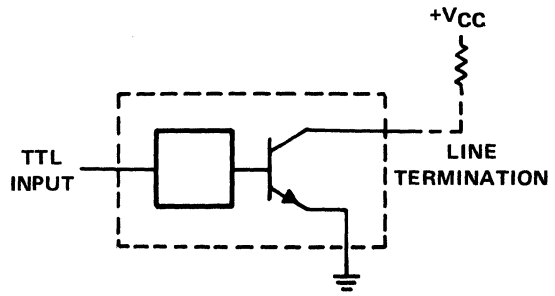


Figure 9-16. Active Pull-Down Configuration

Current-mode drivers are also active switches but they switch a constant current onto the data line. Most current-mode drivers are current sinks. An open-collector transistor (Figure 9-18) is used to switch the data transmission line to a current generator operating from a negative supply rail. Thus the line voltage generated will be negative and is a product of the output current and the line termination resistance. Some advantages of this mode of operation are:

- Output may be shorted without damage to the circuit.
- Line RFI radiation levels are low due to the fact that there are no large surge currents.
- Low impedance data lines can be driven without additional supply power.

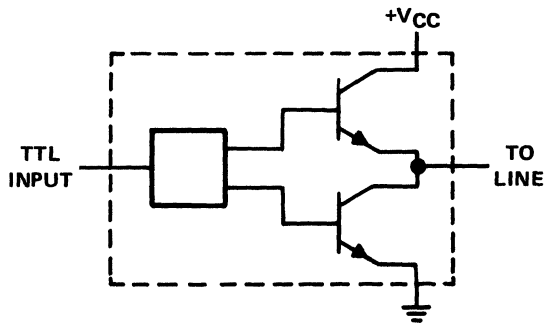


Figure 9-17. Totem-Pole Configuration

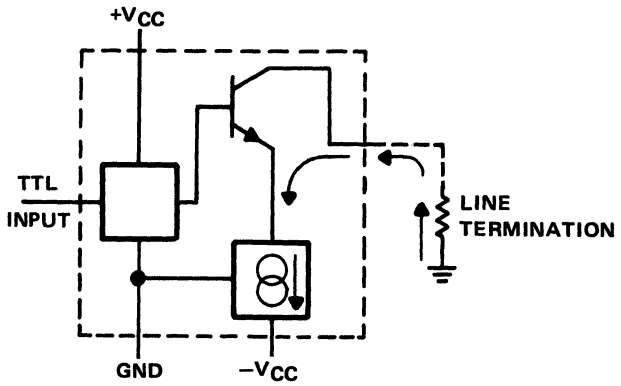


Figure 9-18. Current-Mode Configuration

TYPES OF TRANSMISSION

Whether the driver is voltage-mode or current-mode, it may drive single-ended data transmission lines or dual differential (balanced) transmission lines. Single-wire, dual-wire, twisted pair and coax lines are used for single-ended applications. Discrete single-wire or dual-wire lines are seldom employed, although they can be used where data rates are low and line lengths are short. Normally coax lines or more economical twisted pair lines are used in single-ended transmission. For differential data transmission, a twisted pair line is normally used.

Single-Ended Transmission

Numerous integrated circuit devices are available for driving single-ended data transmission lines. Some are general purpose and others have been designed to meet specific industrial standards. Tables 9-1, 9-2, and 9-3 list drivers, receivers and transceivers designed for single-ended transmission.

Advantages and disadvantages of single-ended drivers:

Advantages

Simplicity: easy to understand and minimum connections.

Low cost.

Usually only one power supply required.

Disadvantages

Radiates RFI easily.

Poor noise immunity.

Coax improves noise but is expensive.

Limited line lengths and data rates due to susceptibility to interference signals.

Table 9-1. Single-Ended Drivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
SN55/75121	2	Emitter-follower outputs to 75 mA	General purpose
SN75361A	2	Totem-pole outputs to 100 mA	General purpose
SN75451B	2	Open-collector to 300 mA	General purpose
DS78/8831	4	3-state diode clamped outputs	General purpose
DS78/8832	4	3-state outputs to 40 mA	General purpose
SN75150	2	Totem-pole dual polarity	RS-232-C
SN75156	2	Totem-pole dual polarity	RS-232-C/423-A
uA9636	2	Totem-pole dual polarity	RS-232-C/423-A
SN75186	4	Totem-pole dual polarity	RS-232-C
SN75187	4	Totem-pole dual polarity	RS-423-A
SN75123	2	Emitter-follower output to 60 mA	IBM 360
SN75126	4	Emitter-follower output to 60 mA	IBM 360/370
SN75130	4	Emitter-follower to 60 mA with fault flag	IBM 360/370

Table 9-2. Single-Ended Receivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
SN55/75122	3	Input hysteresis	General purpose
SN55/75140	2	100 mV sensitivity, common reference	General purpose
SN55/75141	2	100 mV sensitivity, common reference, diode protected	General purpose
SN55/75142	2	100 mV sensitivity, internal reference	General purpose
SN55/75143	2	100 mV sensitivity, internal reference, diode protected	General purpose
SN75152	2	Adjustable hysteresis	General purpose MIL-STD 188 & RS-232-C
SN75154	4	Adjustable hysteresis	RS-232-C
SN75189	4	Response control	RS-232-C
SN75189A	4	Wide hysteresis, response control	RS-232-C
SN75157	2	Fixed hysteresis	RS-232-C/423-A
uA9637AC	2	Fixed hysteresis	RS-232-C/423-A
AM26LS32AC	4	±7 V CMR with ±200 mV sensitivity	RS-422-A/423-A
AM26LS33AC	4	±15 V CMR with ±500 mV sensitivity	RS-422-A/423-A
MC3486	4	±200 mV sensitivity ±7 V CMIV	RS-422-A/423-A
SN75173	4	±200 mV sensitivity 12 kΩ min R_{IN}	RS-422-A/423-A
SN75175	4	±200 mV sensitivity 12 kΩ min R_{IN}	RS-422-A/423-A
SN75124	3	Hysteresis, independent strobes	IBM 360
SN75125	7	7 kΩ min input resistance	IBM 360/370
SN75127	7	7 kΩ min input resistance	IBM 360/370
SN75128	8	Strobe active high	IBM 360/370
SN75129	8	Strobe active low	IBM 360/370

Table 9-3. Single-Ended Transceivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
AM26S10M/C	4	High speed, 100 mA, inverting driver	General purpose
AM26S11M/C	4	High speed, 100 mA, noninverting driver	General purpose
N8T26	4	3-state outputs, 40 mA I_{OL}	General purpose
N8T26A	4	3-state outputs, 48 mA I_{OL}	General purpose
SN75136	4	3-state outputs, 40 mA I_{OL}	General purpose
SN55/75138	4	Open-collector drive to 100 mA	General purpose
SN75163A	4	High speed, receiver hysteresis, 48 mA driver	General purpose
SN75160A	8	High speed, receiver hysteresis, 48 mA driver	IEEE 488
SN75161A	8	For single controller MGMT transceiver	IEEE 488
SN75162A	8	For multiple controller MGMT transceiver	IEEE 488
MC3486	4	3-state outputs, receiver hysteresis, 48 mA driver	IEEE 488

The output voltage from a single-ended driver, although typically at TTL compatible levels, may produce high-level output voltages to help override high noise conditions. An application example (Figure 9-19) uses the SN75361A driver. The SN75361A is a TTL to MOS driver that can provide up to 23 V output swing. Figure 9-19 illustrates an application to provide up to 11 V, V_{OH}, and 0.5 V, V_{OL}, for a resulting output peak-to-peak swing of 10.5 V.

A good receiver to use in this application would be one with 12 V or greater input capability and with adjustable hysteresis to take maximum advantage of noise rejection capabilities. The dual channel SN75152 is such a device.

Features of the SN75152 include:

- ±25 V common-mode input voltage range.
- Adjustable hysteresis.
- Adjustable threshold.
- Standard TTL output.

The receiver circuit is illustrated in Figure 9-20 with a receiver input signal of 0 to 10.5 V. A threshold center of about 5.0 V may be set using one external resistor from the 12 V rail to the inverting input of the receiver (point D). Since the input resistance is about 9 kΩ and we want a 5.0 V reference at that location, the reference pull-up resistor R_r may be calculated as follows:

$$R_r = \left(\frac{V_{CC+}}{V_r} - 1 \right) r_{in}$$

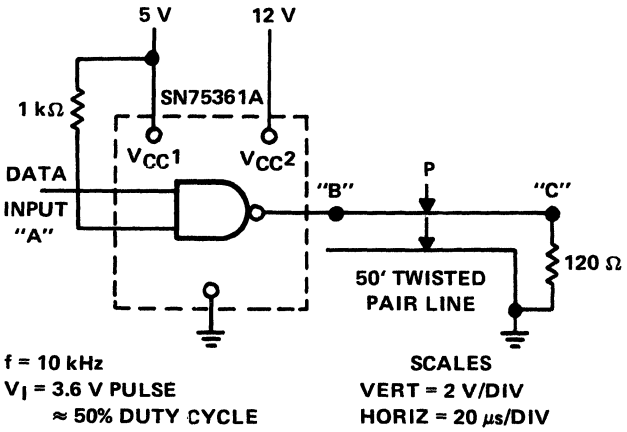
Where:

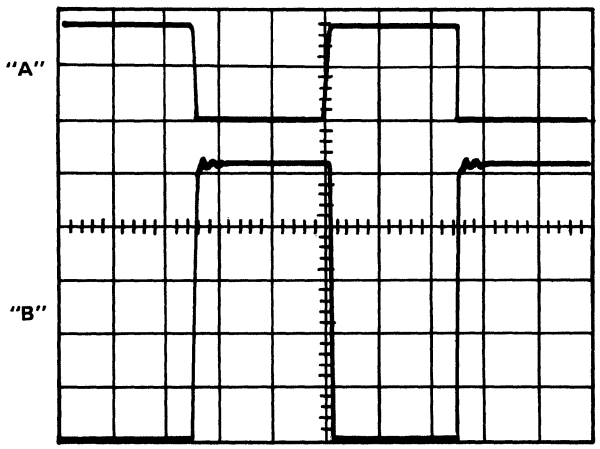
R_r = the reference resistor
V_{CC+} = 12 V
V_r = 5.0 V
r_{in} = 9 kΩ

$$R_r = \left(\frac{12}{5.0} - 1 \right) 9\ k\Omega,\ R_r = 12.6\ k\Omega$$

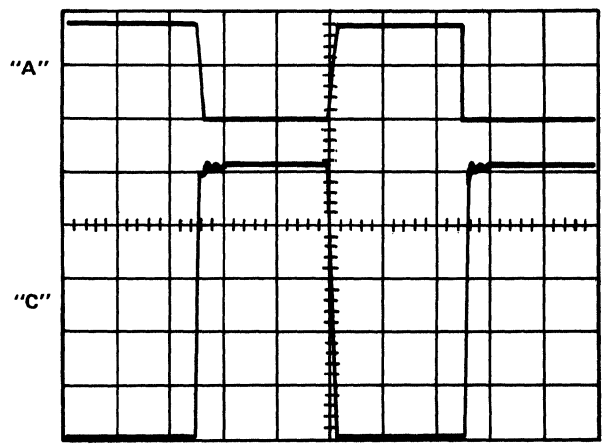
Standard values of 12.0 kΩ and 620 Ω in series may be used.

With 0 V, V_{IL}, and 10.5 V, V_{IH}, levels at point C and a 5 V reference at point D, the threshold hysteresis is selected to be ±3.5 V. A 620 Ω resistor from the hysteresis adjust pin to the −12 V rail will give a ±3.5 V hysteresis. The resulting high level, positive going, threshold (V_{TH}) will be 5 V + 3.5 V, or 8.5 V. The noise margin, when in the low input level state will be about $V_{TH} - V_{IL}$ = 8.5 V − 0 V = 8.5 V. The noise margin when in the high input level state will be $V_{IH} - V_{TL}$ = 10.5 V − 1.5 V = 9 V.





(a) INPUT VERSUS DRIVER OUTPUT



(b) INPUT VERSUS LINE OUTPUT

Figure 9-19. High Level Driver

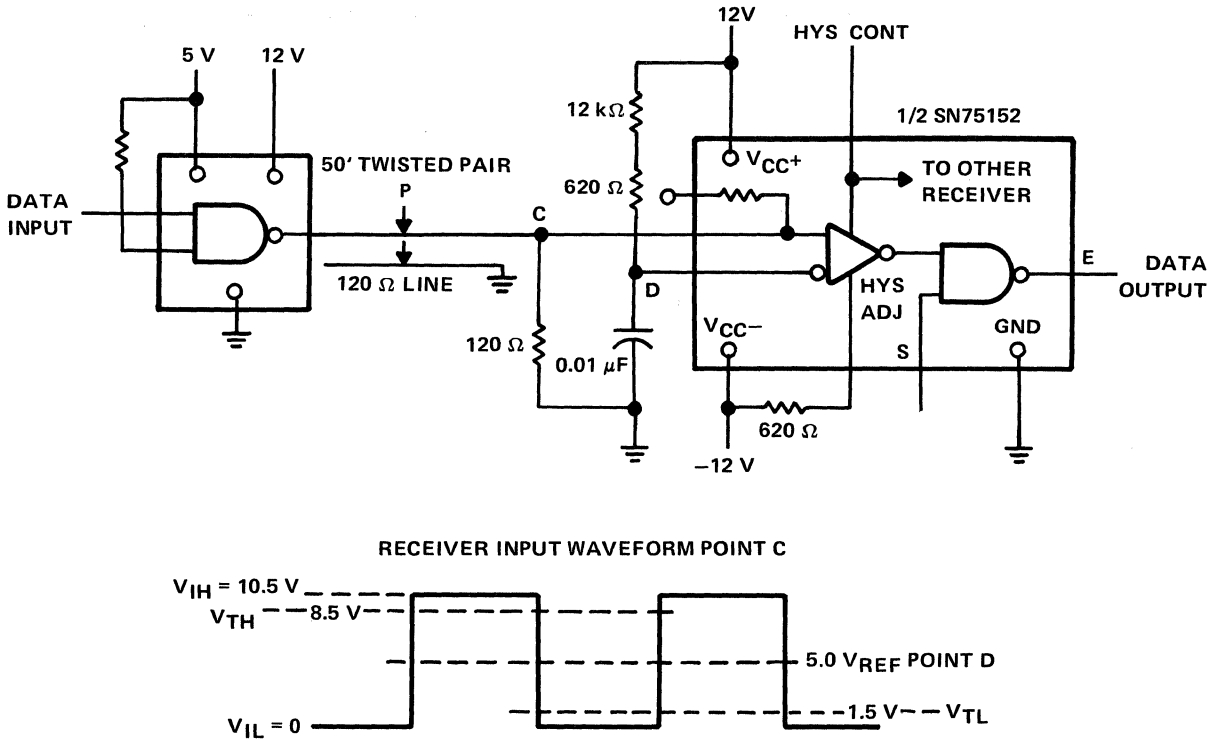


Figure 9-20. Single-Ended Transmission with Receiver Adjusted for High Noise Immunity

Single-Ended Application for High-Speed Bus Communication

In applications where communication between several pieces of equipment over a single data line or bus is required, and the data rates are as high as 1 Mbps, the following device characteristics will be desired:

- Propagation delays of ≤25 ns (accomplished by using high-speed Schottky or similar technology) allowing operation at frequencies up to 2 Mbps.
- Three-state or open-collector outputs for party-line (data bus) operation. This allows several stations to be connected to a single data bus.
- Relatively high output current (≥40 mA) to charge the line capacitance quickly for high-speed requirements.
- Low off-state leakage current (≤200 μA) for minimum loading of the bus line allowing several devices to be connected to a single bus without adversely loading the line.

Several transceiver devices are available for this type of application. Two examples are the AM26S10/S11 quad Schottky bus transceivers and the SN75163A octal low-power Schottky bus transceiver. The AM26S10 and AM26S11 have 100 mA open-collector outputs and typical propagation times of 12 ns. The SN75163A outputs may be full totem-pole or open-collector. An output sink current of 48 mA, and typical propagation delays of 14 ns allow operating speeds up to 2 Mbps. Figures 9-21 and 9-22 illustrate the AM26S10 and SN75163A functional diagrams.

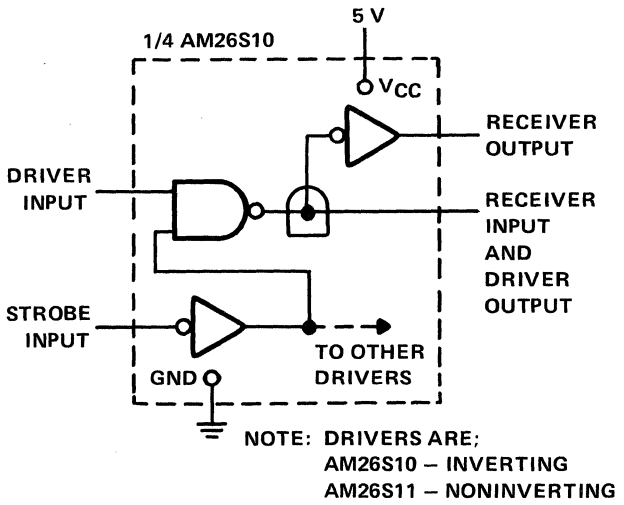


Figure 9-21. AM26S10 Functional Diagram

Figure 9-23 is an example of a 4 line interconnect between several terminal stations. The bus lines are 100 Ω twisted pairs but could be coax. Only the extreme ends of the lines are terminated to 5 V which provides matched termination and the pull-up required for the open-collector driver outputs. Typical V_{OL} levels from the driver outputs are 0.35 V and V_{OH} levels are 4.95 V. Receiver low level requirements of 0.8 V or less and high levels greater than 2.25 V result in error-free operation even over relatively long lines (greater than 200 ft).

The SN75121 driver and SN75122 receiver can be used in another type of popular single-ended application, party-

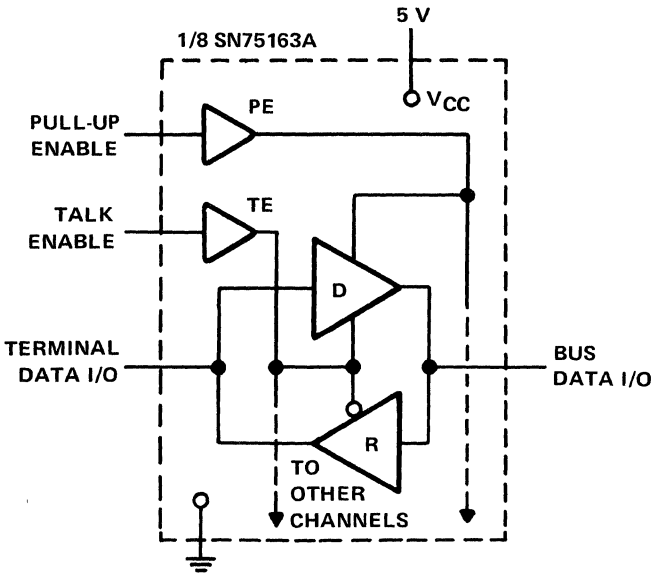


Figure 9-22. SN75163A Functional Diagram

line operation over low-impedance coax lines. Some aircraft and military applications require 50 Ω or 75 Ω coax lines. Because the SN75121 drivers have emitter-follower outputs, which result in high output in the off condition, use in party-line or bus applications is possible. Figure 9-24 illustrates the SN75121 and SN75122 in a party-line application. SN75122 receivers have a typical 0.6 V input threshold hysteresis. Typical negative going threshold is 1.1 V and the positive going threshold is 1.7 V. SN75121 driver outputs are typically 3.7 V V_{OH} and 0 V V_{OL} when operating into a 75 Ω load. The resulting noise margins are 1.7 V and −2.6 V.

Combining a quad SN75365 driver with two SN75152 dual receivers provides for four line independent communication with very good noise immunity (see Figure 9-25). Connecting the SN75365 V_{CC2} pin to the 5 V supply provides an output V_{OH} of 4.5 V and a V_{OL} of 0.5 V. The inverting inputs of the SN75152 are referenced to the midpoint between the driver V_{OH} and V_{OL} levels (2.5 V). This allows for a wide hysteresis range to be set by connecting 1.5 k Ω resistors from the hysteresis adjust pins to $-V_{CC}$. The resulting hysteresis is ±1.7 V from the reference for a high level threshold of 4.2 V and a low level threshold of 0.8 V. The resulting noise margins are ±3.7 V. For additional noise immunity, 125 Ω coax, RG-63B/U, is recommended for the transmission line.

Another receiver that may be used for this application is the SN75154. It may be operated from a single 5 V supply rather than the 12 V and −12 V supplies required by the SN75152. Also the SN75154 is a quad receiver requiring only one package instead of two. There is some reduction in noise margin as it would be 1.7 V and −3.0 V rather than ±3.7 V.

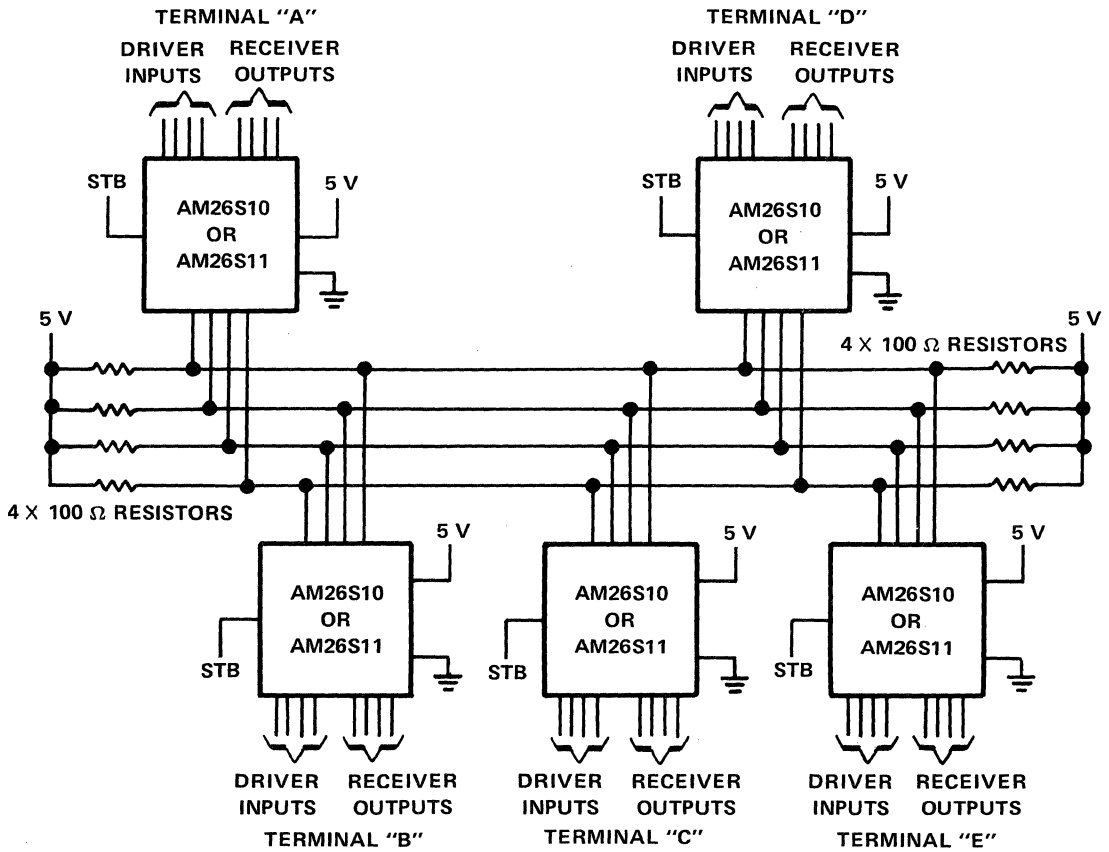


Figure 9-23. Single-Ended Party-Line Bus Application

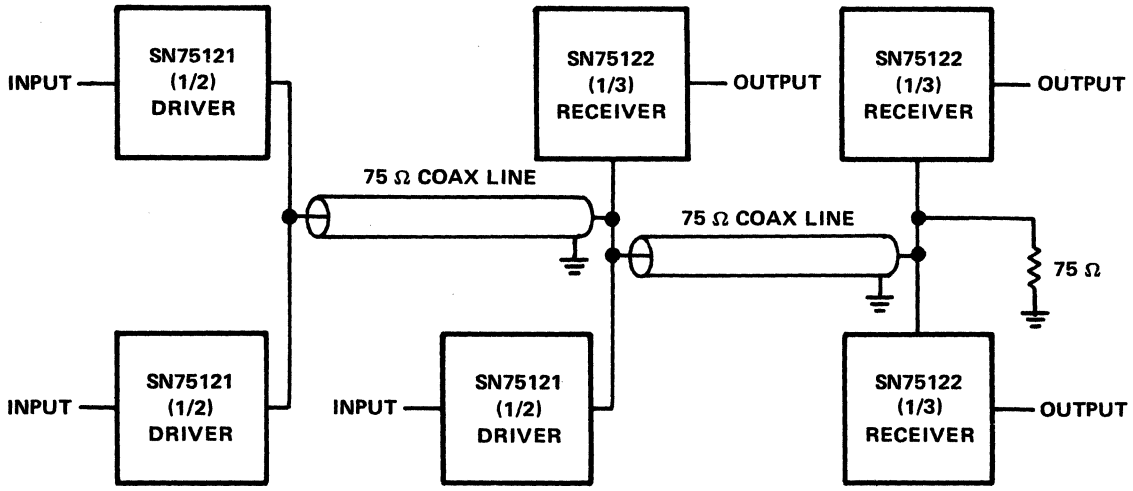


Figure 9-24. Single-Ended Party-Line Application

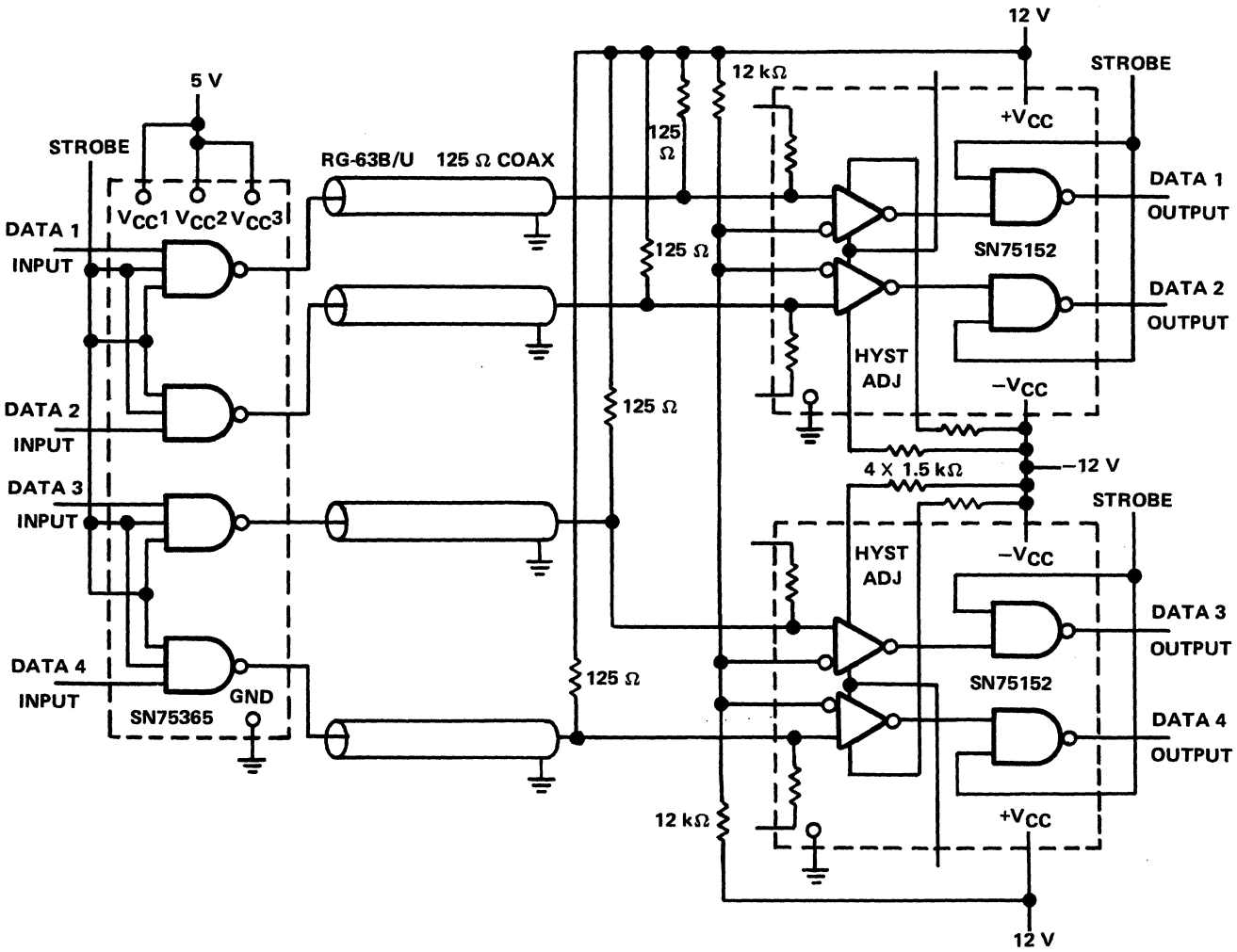


Figure 9-25. Quad Transmission System with High Noise Immunity

Differential Line Drivers and Receivers

The ability to transmit data from one location to another without errors requires immunity to noise. At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage because it is more immune to noise interference than single-ended transmission. Figure 9-26 illustrates the basic sources of noise voltage impressed on a differential, or balanced, data transmission line.

Voltages induced onto the data lines by ground noise or switching transients appear as common-mode signals at the receiver input. Since the receiver has a differential input it responds only to the differential data signal (see Figure 9-26). Differential drivers and receivers can operate safely within specified common-mode voltage ranges. Differential line drivers are designed for general purpose applications as well as specific standards. Tables 9-4 through 9-6 list drivers, receivers and transceivers designed for differential data transmission.

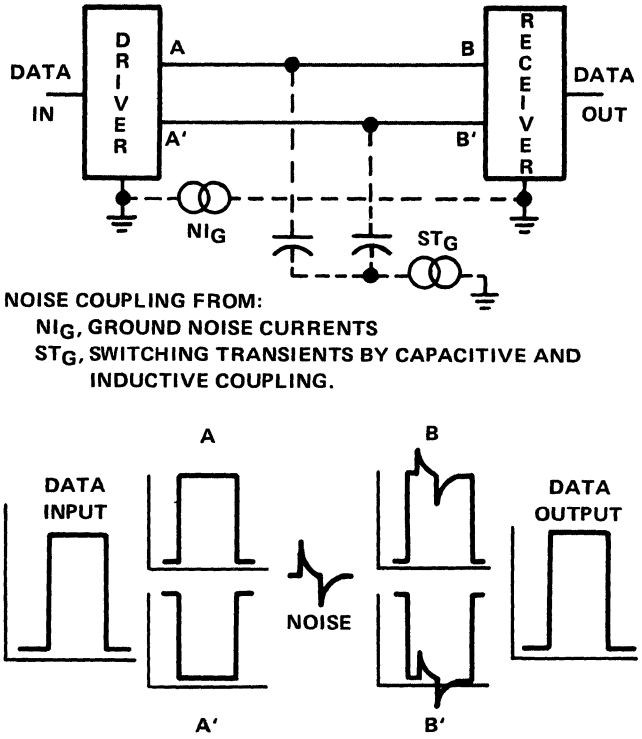


Figure 9-26. Basic Noise Sources and Results

Table 9-4. Differential Drivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
DS78/8831	2	Totem-pole output to 40 mA, and diode clamped	General purpose
SN78/8832	2	Totem-pole output to 40 mA	General purpose
SN55/75109A	2	Current-mode drive 6 mA	General purpose
SN55/75110A	2	Current-mode drive 12 mA	General purpose
SN75112	2	Current-mode drive 27 mA	General purpose
SN55/75113	2	3-state output to 40 mA	General purpose
SN55/75114	2	Totem-pole output to 40 mA	General purpose
SN55/75183	2	Totem-pole output to 40 mA	RS-422-A
SN55/75158	2	Totem-pole output to 40 mA	RS-422-A
SN75159	2	3-state output to 40 mA	RS-422-A
uA9638C	2	Totem-pole output to 50 mA	RS-422-A
AM26LS31C	4	Totem-pole output to 20 mA	RS-422-A
MC3487	4	3-state output to 48 mA	RS-422-A
SN55/75151	4	3-state, individual enable 40 mA	RS-422-A
SN55/75153	4	3-state, common enable 40 mA	RS-422-A
SN75172B	4	3-state, common enable 60 mA	RS-422-A
SN75172B	4	3-state, common enable, 60 mA	RS-485
SN75174B	4	3-state, dual enable, 60 mA	RS-422-A
SN75174B	4	3-state, dual enable, 60 mA	RS-485

Table 9-5. Differential Receivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
SN55/75107A	2	Totem-pole output, V_{ID} ±25 mV	General purpose
SN55/75108A	2	Open-collector output V_{ID} ±25 mV	General purpose
SN55/75107B	2	107A with input power off protected	General purpose
SN55/75108B	2	108A with input power off protected	General purpose
SN75207/207B	2	107A & B with V_{ID} ±10 mV	General purpose
SN75208/208B	2	107A & B with V_{ID} ±10 mV	General purpose
SN55/75115	2	Split totem-pole output V_{ID} ±500 mV	General purpose
SN55/75182	2	Totem-pole output V_{ID} ±500 mV	General purpose
SN55/75157	2	Input hysteresis V_{ID} ±7 V CMR	RS-422-A
uA9637AAC	2	Input hysteresis V_{ID} ±200 mV ±7 V CMR	RS-422-A
AM26LS32AC	4	Input hysteresis V_{ID} ±200 mV ±7 V CMR	RS-422-A
AM26LS33AC	4	Input hysteresis V_{ID} ±500 mV ±15 V CMR	RS-422-A
MC3486	4	3-State output V_{ID} ±200 mV ±7 V CMR	RS-422-A
SN75173A	4	Input hysteresis V_{ITH} ±200 mV ±12 V CMR	RS-422-A
SN75173A	4	Input hysteresis V_{ITH} ±200 mV ±12 V CMR	RS-485
SN75175A	4	Input hysteresis V_{ITH} ±200 mV ±12 V CMR	RS-422-A
SN75175A	4	Input hysteresis V_{ITH} ±200 mV ±12 V CMR	RS-485

Table 9-6. Differential Transceivers

TYPE NUMBER	CIRCUITS/PACKAGE	DESCRIPTION	APPLICATION
SN55/75116	2	3-state split totem-pole 40 mA driver, ±0.5 threshold	General purpose
SN55/75117	2	3-state totem-pole, 40 mA driver threshold	General purpose
SN55/75118	2	'116 with 3-state receiver output	General purpose
SN55/75119	2	'117 with 3-state receiver output	General purpose
SN75176B	2	60 mA 3-state driver, 200 mV sensor with hysteresis	RS-485
SN75177B	2	'176 configured as bus repeater	RS-485
SN75178B	2	'177 with inverted enable	RS-485
SN75179	2	Full duplex '176 type	RS-485

Advantages and disadvantages of differential (balanced) data transmission, relative to single-ended transmission are:

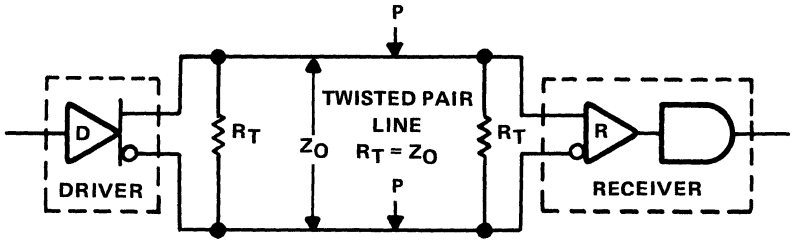
Advantages
- High common-mode noise voltage rejection.
- Reduced line radiation — less RFI.
- Improved speed capabilities.
- Drive longer line lengths.

Disadvantages
- Slightly higher costs (sometimes).
- Must be used with twisted pair or other types of balanced transmission lines.

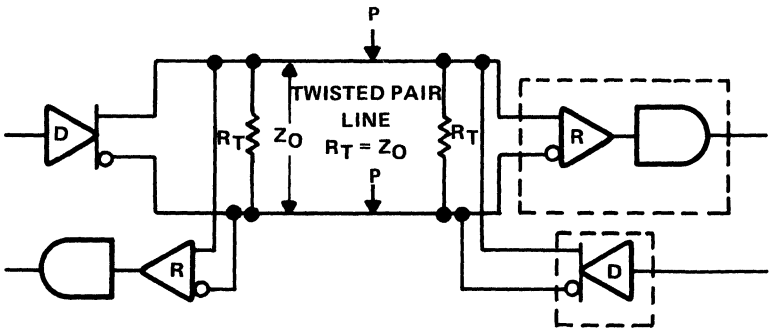
Terminating Differential Data Transmission Lines

As with single-ended data transmission lines, it is necessary to terminate balanced lines properly to prevent ringing and errors in transmitted data. To properly absorb a signal on the line, a termination value equal to the characteristic impedance of the line must be used at the receiving end of the line [See Figure 9-27(a)]. If stray signals and noise are introduced to the line from radiation or other sources, it may be desirable to terminate both the driver and receiver ends of the line to prevent reflections, ringing or oscillations. When multiple drivers are involved the line must be terminated at the extreme ends only as shown in Figure 9-27(b). In party-line systems, termination at each location of a driver or receiver should be avoided because these extra terminations will only adversely load the line. Circuits (a) and (b) use line-to-line termination with a single resistor at each termination point. Line-to-line termination is often the desirable method because it requires minimum power from the drivers. The circuit in Figure 9-27(c) uses line-to-ground termination where the value of R_T is $Z_O/2$. With each line terminated to ground with $Z_O/2$, the total termination line-to-line is still Z_O. However more output drive power will be required from the data transmitters when this type of termination is used.

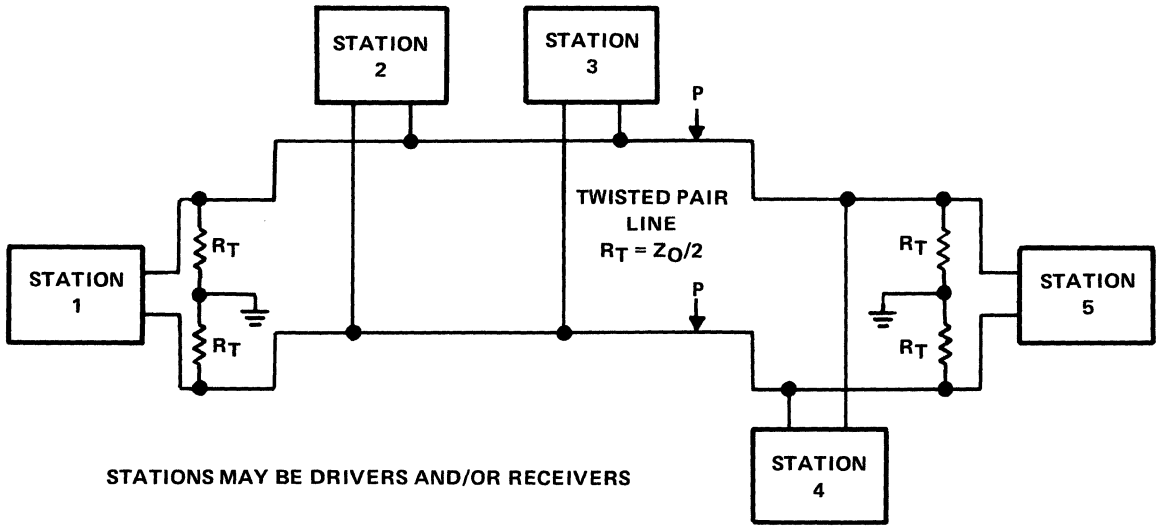
A problem arises with direct line-to-line termination [Figure 9-27(a), Figure 9-27(b)] if noise energy is induced into the transmission line. Noise induced into the data line is common-mode and the noise voltage level, V_N, is a product of the noise current, I_N, and resistance, R_G, from each line to ground. The lowest resistance path to ground is the receiver input resistance, which for the SN75115 is typically about 12 kΩ. If line termination is to ground [Figure 9-27(c)], then the resistance is $Z_O/2$ which may be around 50 Ω. Line noise voltage levels are therefore greatly reduced with the latter termination, resulting in much better common-mode rejection capability. In noisy or long line applications, line-to-ground terminations are preferred.



(a) DEDICATED SINGLE DRIVER; LINE TERMINATED AT RECEIVER



(b) MULTIPLE DRIVERS; LINE TERMINATED AT EXTREME ENDS ONLY



(c) MULTIPLE STATIONS; EACH LINE TERMINATED TO GROUND; TERMINATE EXTREME ENDS ONLY

Figure 9-27. Terminating Balanced Twisted Pair Lines

Current-Mode Drivers in Differential Data Line Transmission

The following problems, typical with voltage-mode drive, can be minimized with current-mode drive.

1. Amount of power required to drive properly terminated low-impedance lines.
2. Large output surge currents during pulse transitions (Figure 9-28) which result in radiation and possible cross talk.

The data line current spikes, illustrated in Figure 9-28, result from charging the distributed capacitance of the line. At low data rates these high speed current surges will result in radiation of RFI. At higher data rates, the surge time remains the same but becomes a large percentage of the overall duty cycle, resulting in excessive power dissipation that can, at some point, lead to deterioration of driver performance or permanent damage.

Examples of current mode drivers include the following dual channel devices:

−55 to 125°C DEVICE	0 to 70°C DEVICE	TYPICAL CONSTANT CURRENT OUTPUT LEVEL
SN55109A	SN75109A	6 mA
SN55110A	SN75110A	12 mA
	SN75112	27 mA

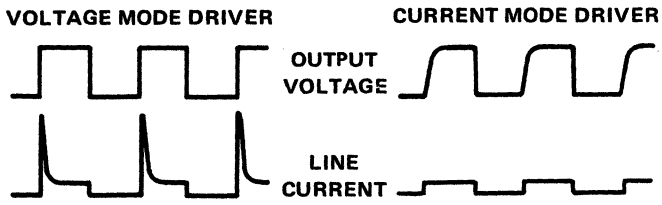


Figure 9-28. Line Current Comparisons

Figures 9-29 and 9-30 show their basic input and output circuit configurations. Driver inputs are basic TTL and followed by a converter circuit (transistors Q2 and Q3) to provide differential control of the output. The differential voltage applied to the bases of Q13 and Q14 (output transistors) is large enough to switch them completely on and off alternately. When on, the output transistor (Q13 or Q14) will sink an amount of current supplied by the constant current generator consisting of Q15, Q16, Q17, Q18, Q19, and R9. Thus, an output when switched on will be a fixed current sink at the level set by the current generator.

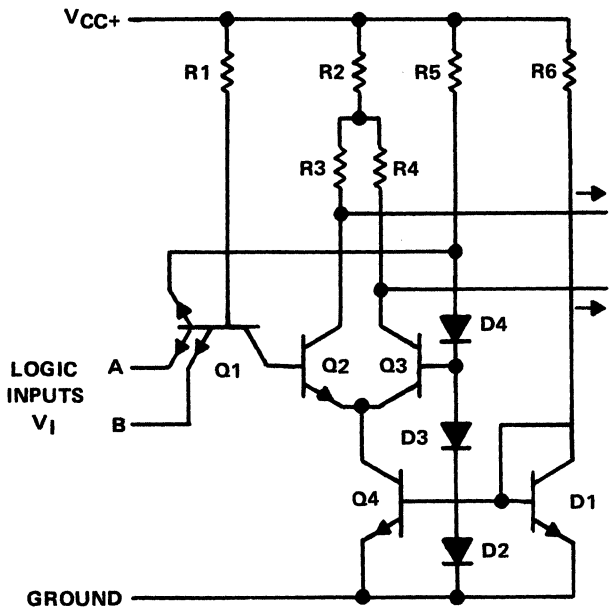


Figure 9-29. Input Circuit

Output current sink is to the device's −5 V rail which generates an output voltage that is a product of this current and the output terminal resistance to ground. Figure 9-31 shows a typical SN75110A input-to-output transfer curve for a 50 Ω termination. In this example 600 mV is generated by each output for a total differential swing of 1.2 V. Outputs may be shorted to ground or either supply rail without damage to the device. The recommended operating output common-mode range is 10 V to −3 V. Exceeding these levels will result in output saturation and possible improper operation. Figure 9-32 shows the logic diagram and function table for a typical current-mode driver.

The receivers recommended for use with current-mode drivers are those with very good sensitivity levels (less than or equal to 25 mV).

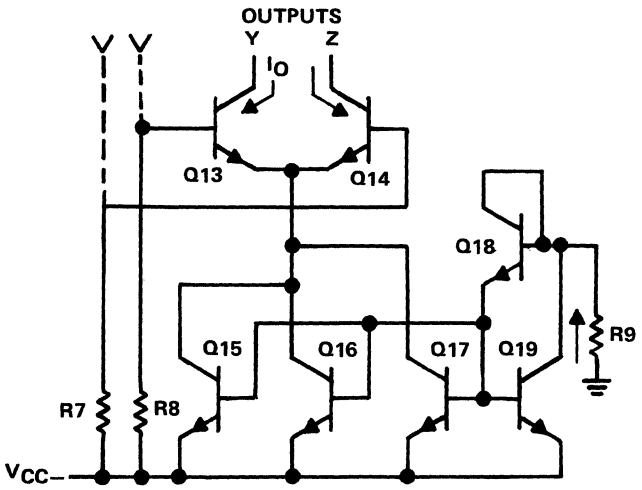


Figure 9-30. Output Circuit

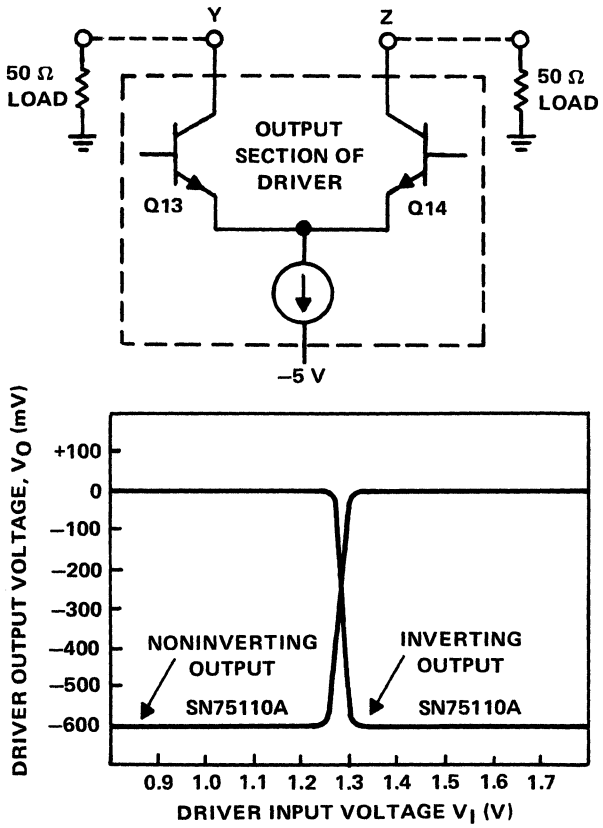
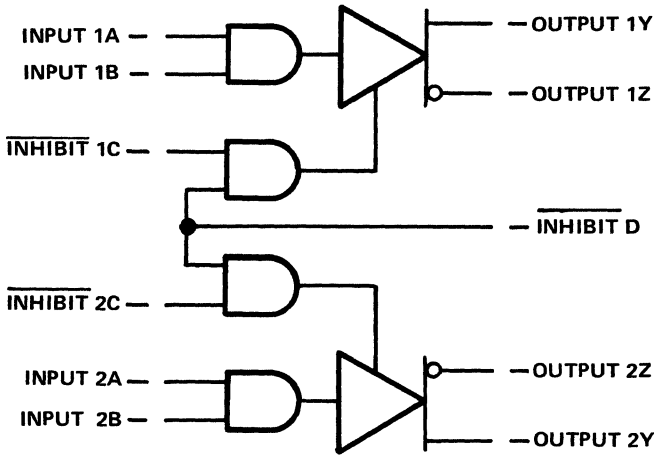


Figure 9-31. Typical Voltage Plot for SN75110A Driver

Following is a list of recommended receivers:

−55 to 125°C Device	0 to 70°C Device	Input Sensitivity	Receiver Output Type
SN55107A	SN75107A	±25mV	Totem-pole
SN55107B	SN75107B	±25mV	Totem-pole
SN55108A	SN75108A	±25mV	Open-collector
	SN75207	±10mV	Totem-pole
	SN75207B	±10mV	Totem-pole
	SN75208	±10mV	Open-collector
	SN75208B	±10mV	Open-collector



(a) LOGIC DIAGRAM

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level, X = irrelevant

(b) FUNCTION TABLE

Figure 9-32. Current-Mode Driver Logic Diagram and Function Table

Figures 9-33 and 9-34 show typical receiver equivalent input and output circuits.

The receiver input is differential and provides a common-mode input voltage range of ±5 V absolute maximum and ±3 V recommended operating maximum. The outputs differ slightly as is shown in Figure 9-34. SN75107A type devices have standard TTL totem-pole outputs while the SN75108A type devices have open-collector outputs. Open-collector outputs allow wired-OR connection of multiple outputs to a single line.

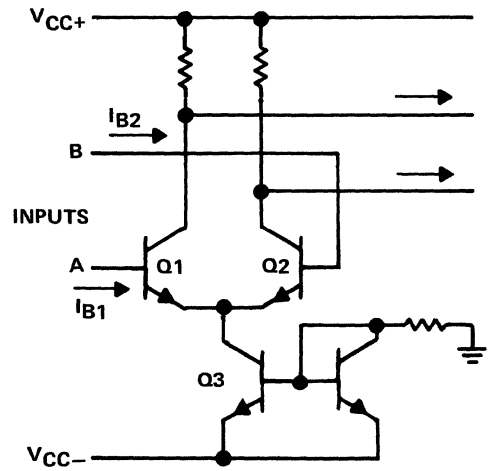


Figure 9-33. Receiver Input Stage, Input Current Source, and Bias Circuit

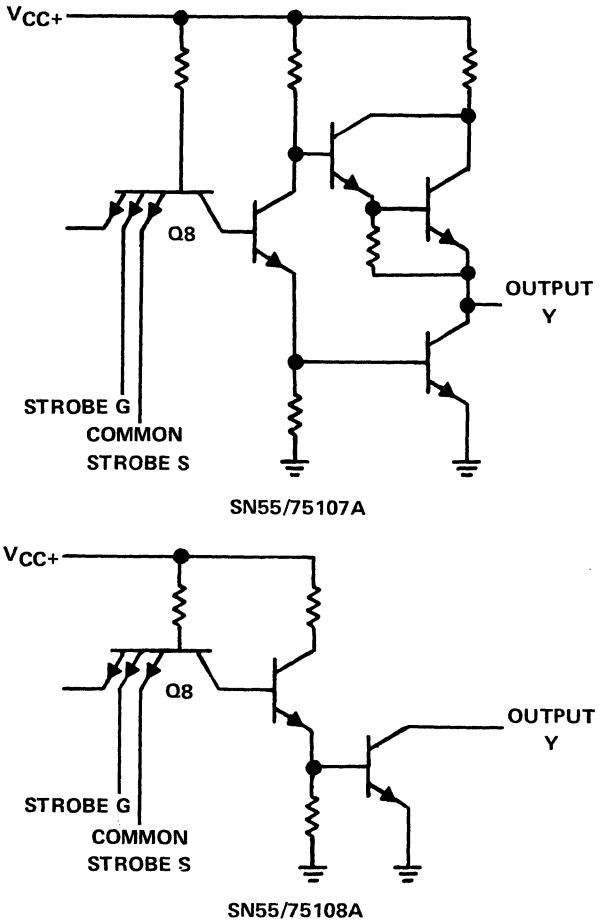


Figure 9-34. Output Gates of SN55/75107A and SN55/75108A Compared

RECEIVER PERFORMANCE

The SN55/75107A receiver circuit has a nominal propagation delay of 17 ns, making it ideal for use in high-speed systems. The receiver delay is almost completely insensitive to overdrive voltages of 10 mV. The circuit responds to input signals with repetition rates as high as 20 Mbps.

Input Sensitivity

The input sensitivity is defined here as the differential dc voltage required at the inputs of the receiver to force the output to the logic gate threshold voltage level. The input sensitivity of the receivers is nominally 3 mV. This feature is particularly important when data is transmitted over a long line and the pulse is deteriorated due to line effects. A receiver with this sensitivity also finds many other applications such as comparators, sense amplifiers, and level detectors.

Common-Mode Voltage Range

The common-mode voltage range or CMVR is defined here as that voltage applied simultaneously to both input terminals which, if exceeded, does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely

noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if precautions are not taken to reduce ground and power supply noise, as well as cross talk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors which will be compatible with the particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation time, the power dissipation, and in some cases the input impedance (depending upon the selected resistor values), therefore reducing the versatility of the receiver.

The ability of the receiver to operate with a ±15 V common-mode voltage at the inputs has been demonstrated using the circuit shown in Figure 9-35. Dividers with three different values presenting a 5-to-1 ratio were used so as to operate the differential inputs under ±3 V common-mode voltage. Careful matching of the two attenuators is needed to balance the overdrive at the input stage. The resistances used were:

Attenuator 1: R1 = 2 kΩ, R2 = 0.5 kΩ
Attenuator 2: R1 = 6 kΩ, R2 = 1.5 kΩ
Attenuator 3: R1 = 12 kΩ, R2 = 3.0 kΩ

Table 9-7 shows some of the typical switching results obtained under such conditions.

Table 9-7. Typical Propagation Delays for Receiver with Attenuator Test Circuit Shown in Figure 9-35

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
SN55/75107A	$t_{pd(1)}$	1	20
		2	32
		3	42
	$t_{pd(0)}$	1	22
		2	31
		3	33
SN55/75108A	$t_{pd(1)}$	1	36
		2	47
		3	57
	$t_{pd(0)}$	1	29
		2	38
		3	41

NOTE: Output load R_L = 390 Ω.

Input Termination Resistors

To prevent reflections, the transmission line should be terminated in its characteristic impedance. Matched termination resistances normally in the range of 25 to 200 Ω are required not only to terminate the transmission line in a desired impedance, but also to provide a necessary dc path

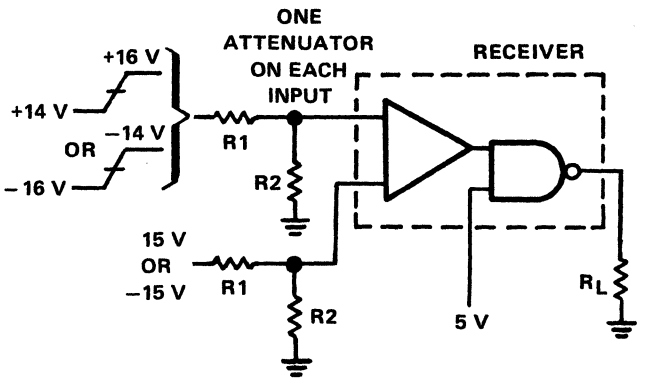


Figure 9-35. Common-Mode Circuit for Testing Input Attenuators

for the receiver input bias. Careful matching of the resistor pairs should be observed or the effective common-mode rejection ratio will be reduced.

The input circuit of the receivers must meet the requirements for low input currents (30 μA typical) and high input impedance. These requirements provide for low loading on the lines, an important consideration for "party-line" applications.

Reference Voltage

The receiver can be used as a single-ended line receiver or comparator by referencing one input as shown in Figure 9-36. The operating threshold voltage level is established by (and is approximately equal to) the applied reference input voltage, V_{ref}, selected within the operating range.

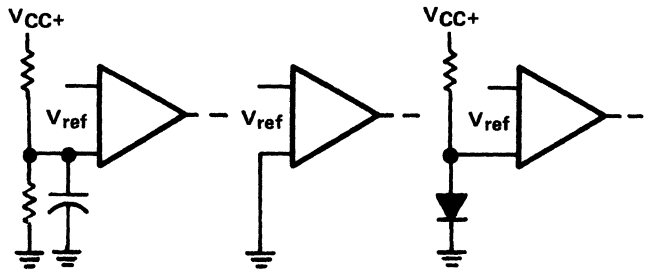


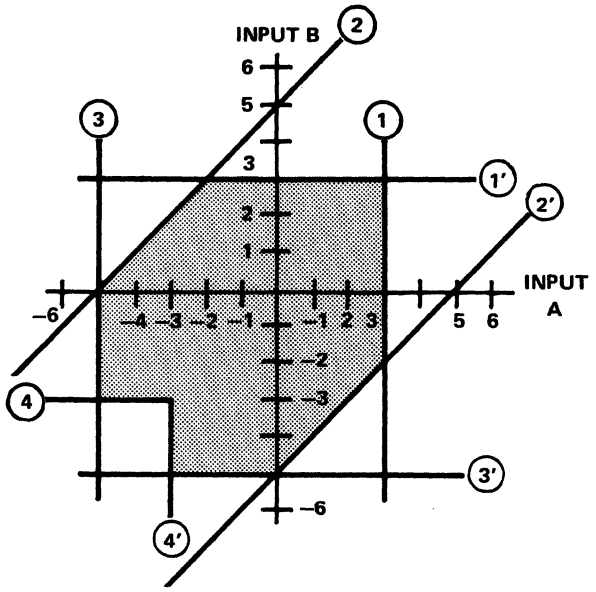
Figure 9-36. Some Methods of Referencing Receiver Inputs

A simple method of generating the reference voltage is the use of a resistor voltage divider from either the V_{CC+} or V_{CC-} supply as in Figure 9-36(a). The reference can also be obtained by a diode [Figure 9-36(c)] or a reference supply or just ground [Figure 9-36(b)]. The bias current required at the referenced input is low (nominally 30 μA). Therefore, voltage dividers of this type may normally be operated with very low current requirements and may be used also to supply a number of paralleled reference inputs. In noisy environments, the use of a filter capacitor may be recommended as indicated in Figure 9-36(a).

Input Limitations

Figure 9-37 shows the "safe operating region" of voltages at the two receiver inputs. Coordinates within the shaded area are considered safe operating conditions. As an example:

1. If B is 2 V, A may be any value from −3 V to 3 V.
2. If B is −2 V, A may be any value from −5 V to 3 V.
3. If A is 0 V, B may be any value from −5 V to 3 V.



LINES	DESCRIPTION
1 AND 1'	MAXIMUM POSITIVE INPUT SIGNAL IS +3.0 V.
2 AND 2'	MAXIMUM DIFFERENTIAL SIGNAL $\lvert A-B \rvert$ IS 5.0 V.
3 AND 3'	MAXIMUM NEGATIVE INPUT SIGNAL IS −5.0 V.
4 AND 4'	MAXIMUM COMMON MODE IS ±3.0 V.

Figure 9-37. "Safe Operating Region" for Receiver Inputs

SN55/75107A SERIES APPLICATIONS

Connection of Unused Inputs and Outputs

In any application of SN55/75107A series devices, there are two important precautions to be observed. First, when only one receiver in a package is being used, at least one of the differential inputs of the other receiver should be terminated at some voltage between 3 V and −3 V, preferably at ground. Failure to do so causes improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Second, when only one driver in a package is used, the outputs of the other driver must either be tied to ground or inhibited. Otherwise, excessive power dissipation may result.

There are some other equally basic but less critical recommendations concerning unused driver gate inputs. Where these inputs are left open-circuited, the propagation delay to a logic low level is increased by about one nanosecond per input. In high-speed systems this could be a significant factor.

For faster switching times, unused gate inputs can be tied to a positive voltage source of about 2.4 V. This disposition greatly reduces the distributed capacitance associated with the emitter. It also ensures that no additional degradation occurs in the propagation delay times.

An alternative solution is to tie the unused gate inputs to V_{CC} through a resistor. The value of the resistor should not be less than 1 kΩ or the transient voltages could damage the inputs. The upper resistor value is determined by the voltage drop caused by logic high level input currents and by the minimum supply voltage. The best solution is to join the unused input to the used input on the same gate. This method provides the fastest switching speeds since the stray capacitances are driven by the preceding gate, and it also provides protection against excessive supply surges since the 54/74 TTL outputs at a logic high level are typically 3.5 V and are current-limited.

One-Channel Balanced Transmission System

SN55107A series dual line circuits are designed for use in high-speed data transmission systems that utilize balanced, terminated transmission media such as twisted pair lines. Such a system operates in the balanced mode, so that noise induced on one line is also induced in the other. The noise appears as common-mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and line receiver is not part of the signal circuit, so that system performance is not affected by circulating ground currents and ground noise. Figure 9-38 illustrates the ability of the receivers to reject common-mode noise.

The unique output circuit of the driver allows terminated transmission lines to be driven at normal line impedances. High-speed operation of the system is ensured since line reflections are virtually eliminated when terminated lines are used. Cross talk is minimized because of the low signal amplitude, low line impedances, and because the total current in a line pair remains constant.

A basic balanced transmission system using SN55107A series devices is shown in Figure 9-39. Data is impressed on the twisted pair line by unbalancing the line voltages by means of the driver output current. Line termination resistors labeled R_T are required only at the extreme ends of the line. For short lines, termination resistors only at the receiver end may prove adequate. Signal phasing depends on the driver output and receiver input polarities on the line.

Differential Party-Line Systems

When several stations must communicate with each other it is generally more economical for all stations in the system to share a single transmission line rather than to use many dedicated lines. The strobe feature of the receivers and the inhibit feature of the drivers allow the SN55107A series dual line circuits to be used in party-line (also called data bus) applications. Examples are shown in Figures 9-40, 9-41, and 9-42. In each of these examples, one driver is enabled and

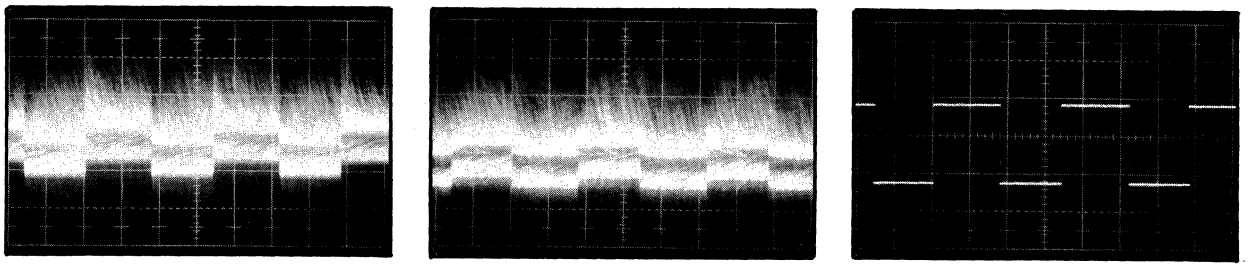


Figure 9-38. Oscilloscope Displays of Typical Noisy Inputs and Noise-Free Output of SN75108 Line Receiver (Test Frequency: 10 kHz. Input Signal: 50 mV Peak-to-Peak. Input Noise: 4.0 V Peak-to-Peak)

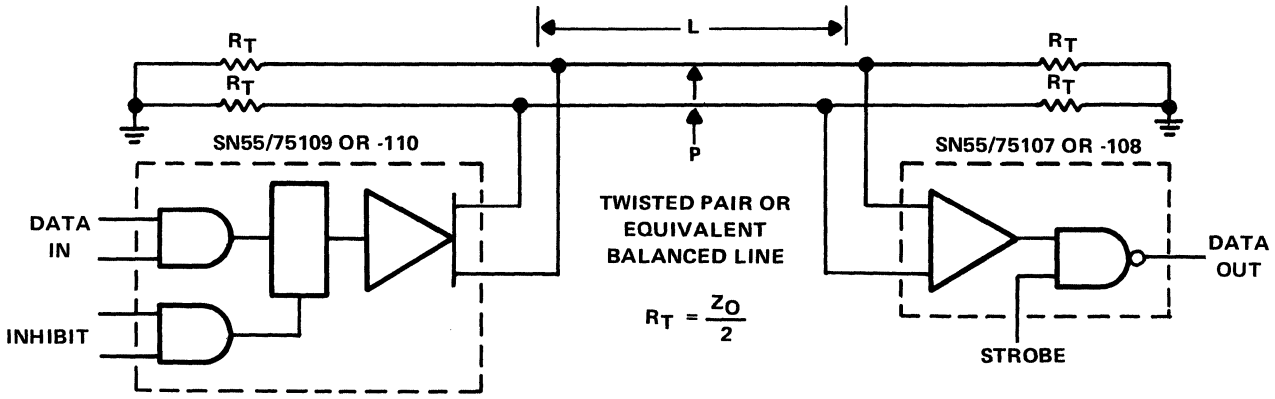


Figure 9-39. Use of SN55107 Series Devices in a Typical Single-Driver, Single-Receiver Transmission System

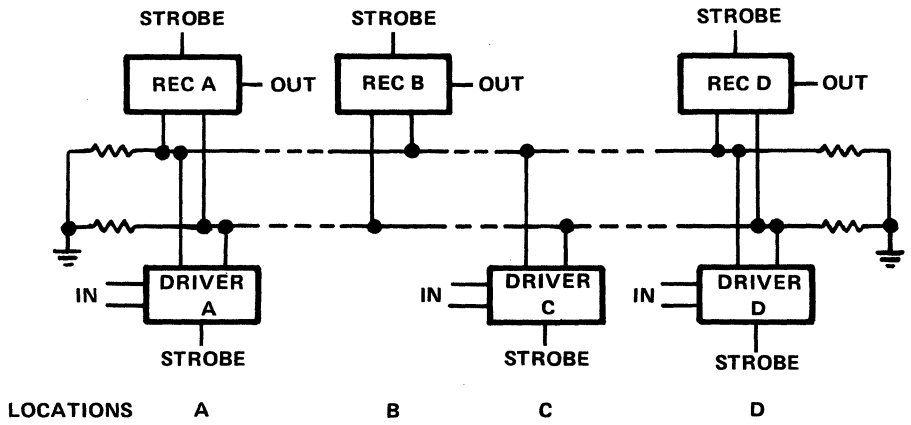


Figure 9-40. Simple Party-Line System with Driving and Receiving Stations Scattered Along the Receiving Stations Scattered Along the Line

transmits to the receivers on the line, while all other drivers are disabled. Data from the various drivers can therefore be time multiplexed on the transmission line.

Figure 9-43 illustrates an eight-channel party-line application similar to that in Figure 9-42, including the clocking arrangements. This method uses two twisted pair lines: one for data transmission and the other for clocking and control information. Details of the clocking and control circuits appear in Figures 9-44 and 9-45. Careful matching of the line delays is necessary to ensure synchronized clocking.

Repeaters for Long Lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large for good reception. In such a case, a simple application of a driver and receiver as a repeater [(shown in Figure 9-46(a)] restores the signal level and allows an adequate signal level at the receiving end. If multi-channel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 9-46(b). In most cases, two twisted pair lines suffice, one for the information and the other for the clock pulses.

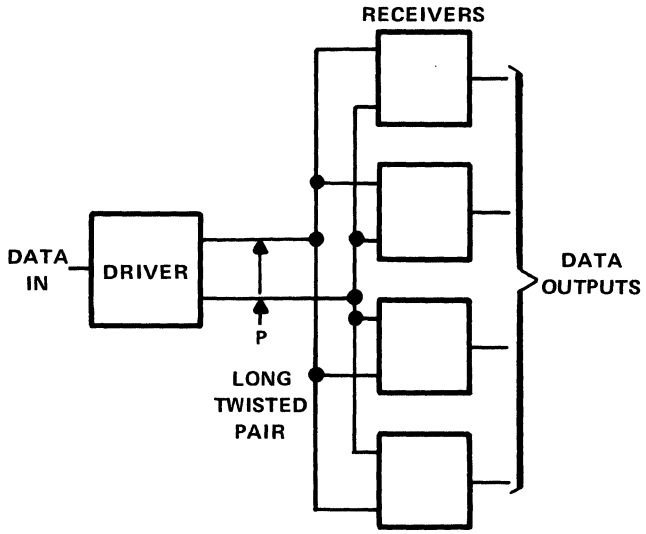


Figure 9-41. Party-Line Concept of One Driver Transmitting to One of Many Receivers

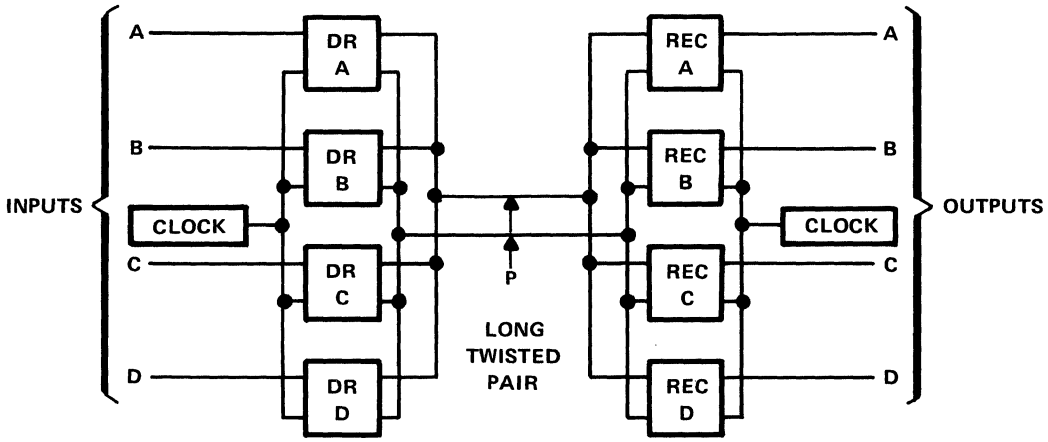


Figure 9-42. Conceptual Diagram of Four Transmission Channels Sharing the Same Party Line

STANDARD VOLTAGE-MODE DIFFERENTIAL DRIVERS AND RECEIVERS

Voltage-mode drivers are not without positive features to make them desirable in differential data line transmission. These features include the following:

- Will operate from single (usually 5 V) supplies.
- Exhibit high common-mode voltage capabilities.
- Less circuit complexity allows four drivers or four receivers in one package.

The following discussion includes only devices in the SN75113 through SN75119 family but is equally applicable to many of the other popular voltage-mode data line drivers and receivers.

SN75113 and SN75114 dual differential line drivers are almost identical. The SN75113 has three-state outputs allowing operation with other drivers on a party line. These drivers are designed to work with the SN75115 dual receiver and each device operates from a single 5 V supply. For dedicated single drive applications, the SN75114 may be preferred for its triple input gate control, but if multiple drivers are on the line a three-state output SN75113 would be used (see Figure 9-47). A capacitor may be connected in series with Z_O to reduce power dissipation. Also, the SN75115 receiver outputs are three-state. This allows a wired-OR connection of several receivers by using a common pull-up resistor.

Differential voltage levels at the most remote receiver will be dependent on the driver output voltage swing ($V_{OD} = V_{OH} - V_{OL}$), termination loading, and line attenuation. Assuming a worst-case input voltage swing (V_I) requirement at the receiver of 500 mV, the maximum theoretical line length may be derived as follows: $V_{OD} = V_{OH} - V_{OL}$ where V_{OH} and V_{OL} are determined by the dc loading. A typical 120 Ω line terminated rail to

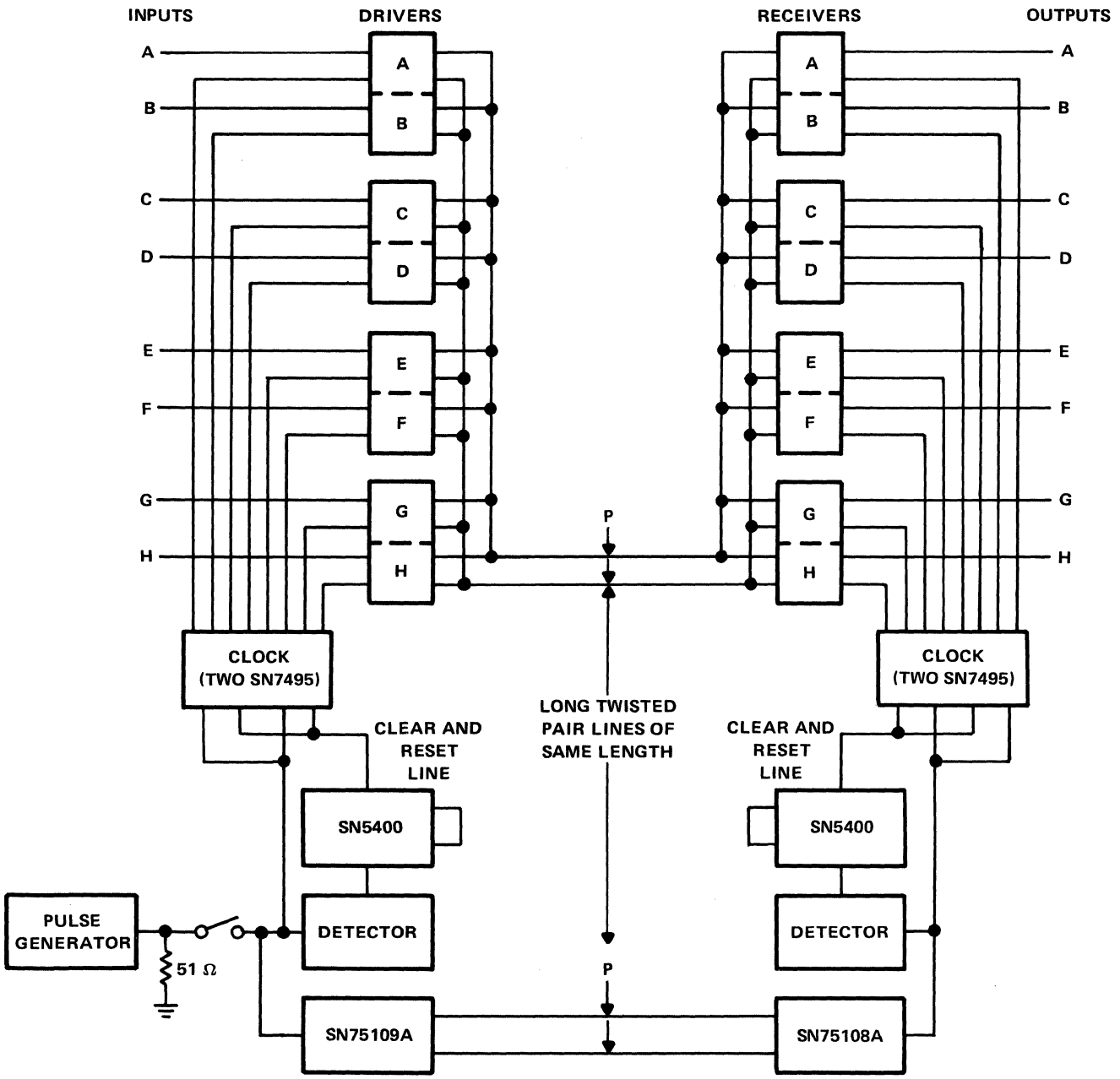


Figure 9-43. A Multi-Channel System with Clocking
(See Details of Detector, Clock, and Test Circuit in Following Figures)

rail as illustrated in Figure 9-47 will allow a V_{OH} of 3.2 V, a V_{OL} of 0.17 V and a resulting V_{OD} of 3.03 V. The maximum attenuation allowable is:

$$A_{MAX} = 20 \log_e (V_{OD} - V_{ID})$$
$$= 20 \log_e (3030\text{-}500)$$
$$A_{MAX} = 20 \log_e 2530 = 68 \text{ dB}.$$

Termination at the two extreme ends of the line will result in an additional 6 dB loss, therefore the maximum allowable line loss is 62 dB. For a clock frequency of 1.8 MHz (see Figure 9-48) the attenuation of a typical twisted pair transmission line (AWG 22 solid wire with 0.060 inch plastic cover, twisted 4.5 times per foot) will be 1.25 dB per 100 feet.

Line length is therefore 62 dB divided by 1.25 dB per 100 feet which yields 4960 feet maximum. This calculated value correlates closely with the measured line length versus frequency curves, Figure 13 - page 289, in the Line Driver and Line Receiver Data Book, 1981.

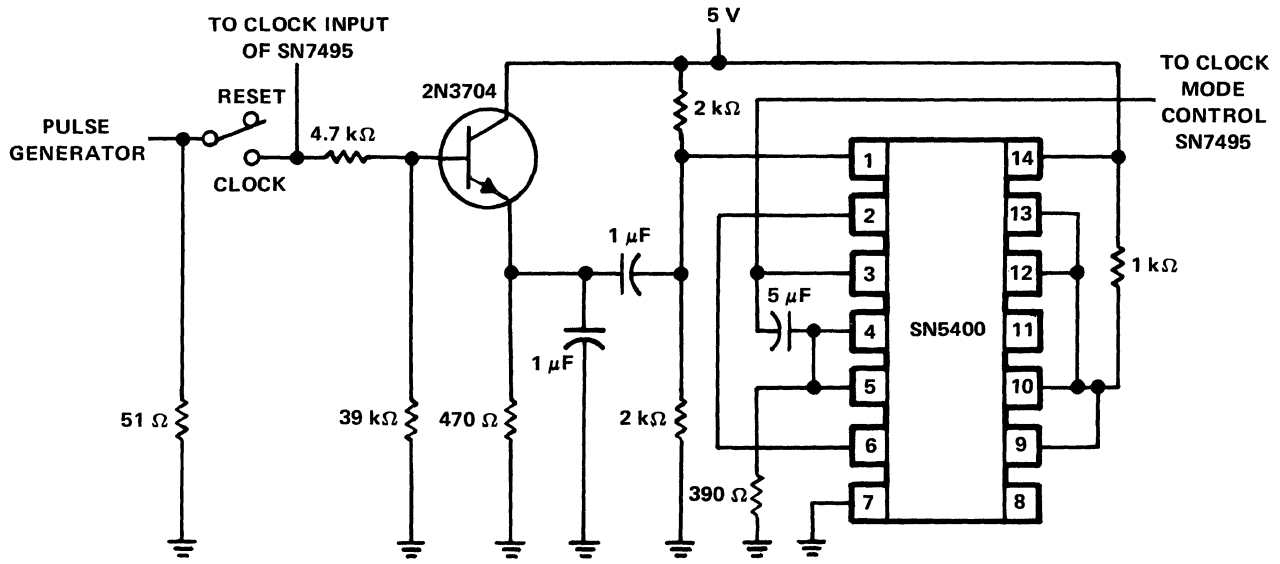
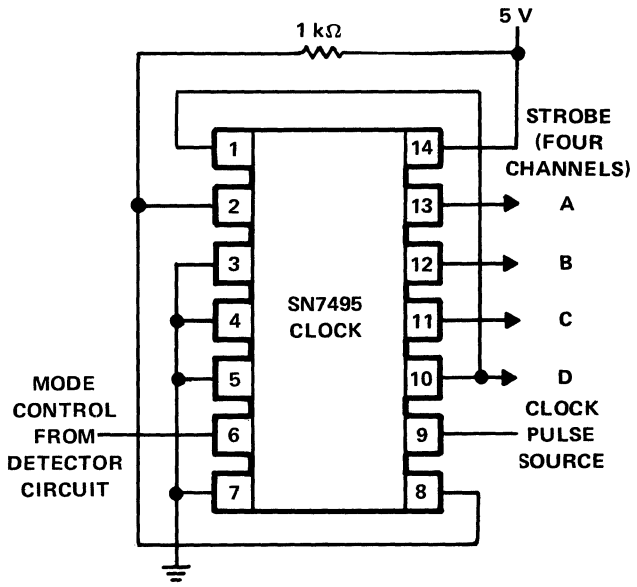
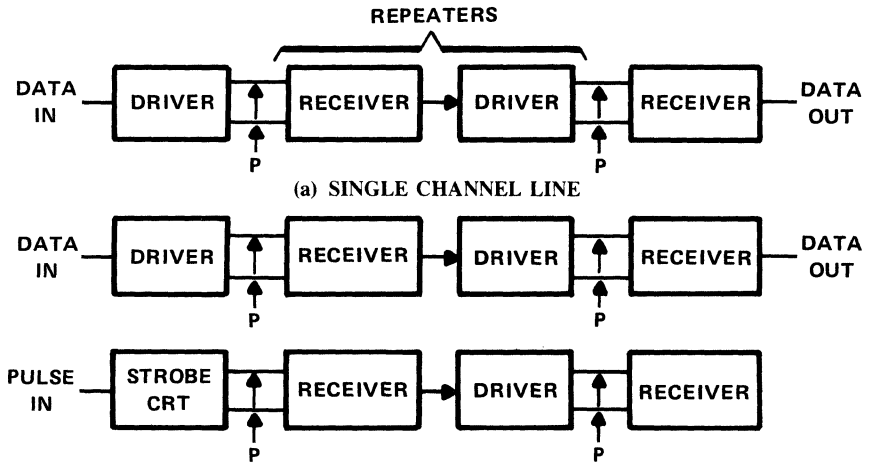


Figure 9-44. Detector Circuit for Clearing SN7495 Clock in Figure 9-43



NOTE: IF MORE THAN FOUR CHANNELS ARE NEEDED, USE ADDITIONAL SN7495's CONNECT "D" (PIN 10) TO THE SERIAL INPUT (PIN 1) OF THE SECOND CLOCK AND THE "D" (PIN 10) OUTPUT OF THE LAST CLOCK BACK TO PIN 1 OF THE FIRST CLOCK.

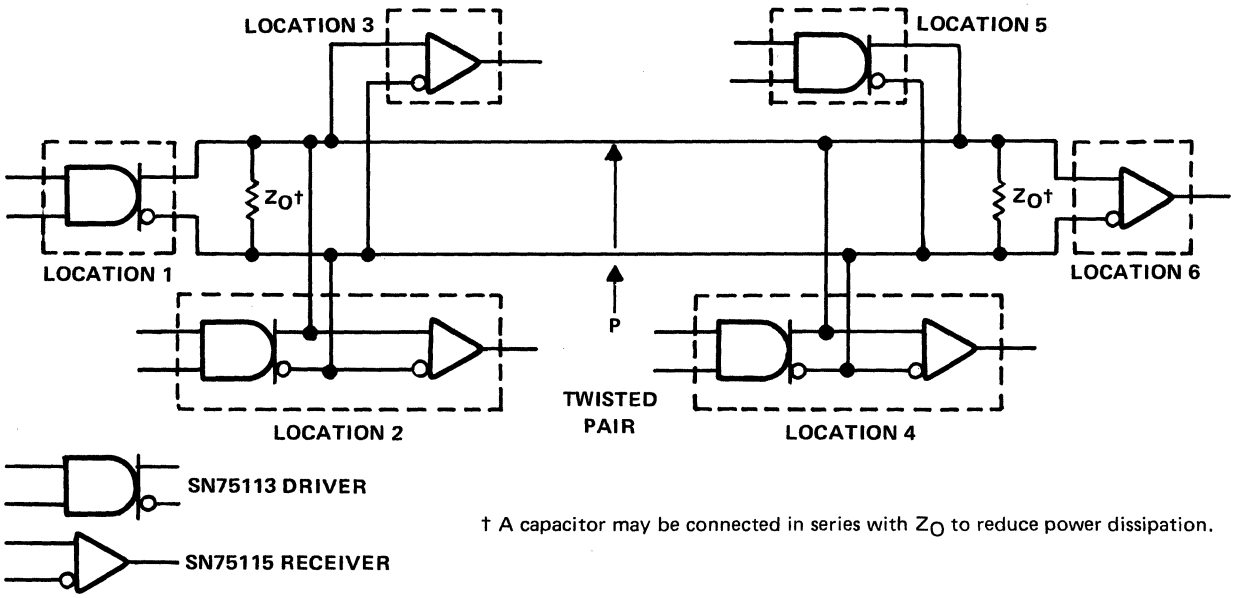
Figure 9-45. SN7495 Clock for Strobing Drivers and Receivers in Figure 9-43



(a) SINGLE CHANNEL LINE

(b) MULTI-CHANNEL LINE WITH STROBE

Figure 9-46. Driver-Receiver Repeaters



† A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 9-47. Basic Party-Line Differential Data Transmission

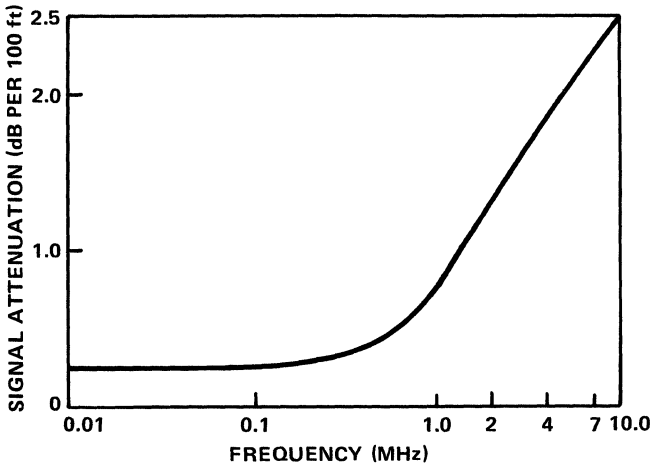


Figure 9-48. Signal Attenuation with Frequency in Twisted Pair Transmission Line (AWG 22 Solid Wire with 0.060-in Plastic Cover, Twisted 4.5 Times Per Foot)

EIA STANDARD RS-232-C CIRCUITS AND APPLICATIONS

The Electronic Industries Association (EIA) introduced the RS-232 standard in 1962 for the purpose of standardizing the interface between data terminal equipment (DTE) and data communication equipment (DCE). See Figure 9-49. Although emphasis was then, and still is, on interfacing between a modem unit and data terminal equipment, this standard is also applicable to serial binary interfacing between various types of data terminal equipment. The revised EIA standard RS-232-C introduced in August 1969 is widely accepted for single-ended data transmission over short distances with low data rates. Several types of drivers and receivers have been developed for use in RS-232-C interfacing applications. Basic requirements for RS-232-C type data line drivers and receivers are shown in Table 9-8 and Table 9-9.

TYPICAL DRIVERS FOR EIA RS-232-C APPLICATIONS

SN75150 Dual Data Line Driver

The SN75150 dual line driver (Figure 9-50) is an RS-232-C type driver with the following features:

- Withstands sustained output short circuit to any low impedance voltage between −25 V and 25 V.
- Operates from ±12 V supplies.
- 2 μs max transition time through the 3 V to −3 V transition region under a full 2500 pF load.
- TTL compatible inputs.
- Common strobe input.
- Slew rate controllable with an external capacitor at the output.

SN75156/uA9636 Dual Line Driver

The SN75156/uA9636 (Figure 9-51) is a dual line driver having the following features:

- Wide supply range (±7.5 V to ±15 V).
- Low supply current required (4.5 mA max./channel).
- Wave shaping with external resistor.
- TTL or low level CMOS compatible inputs.
- Source and sink output current limiting.

The SN75156 is a single-ended line driver designed for EIA RS-232-C requirements and also EIA RS-423-A, European standard CCITT recommendations V.10, V.28, X.26, and the U.S. Federal Standard FIPS 1030. This device maintains regulated high and low output levels of 5.5 V and −5.5 V, respectively, over a wide range of power supply voltages. The output transition time for both drivers can be

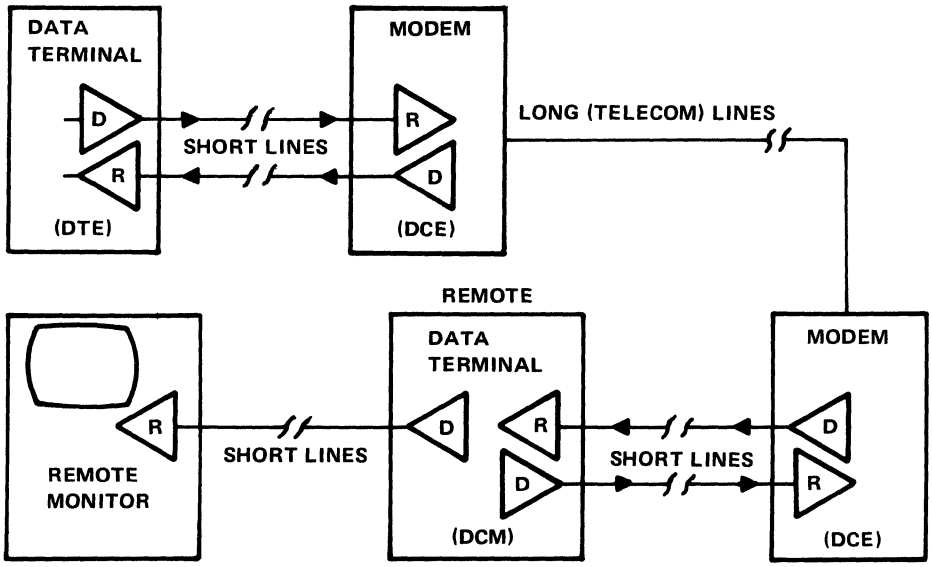
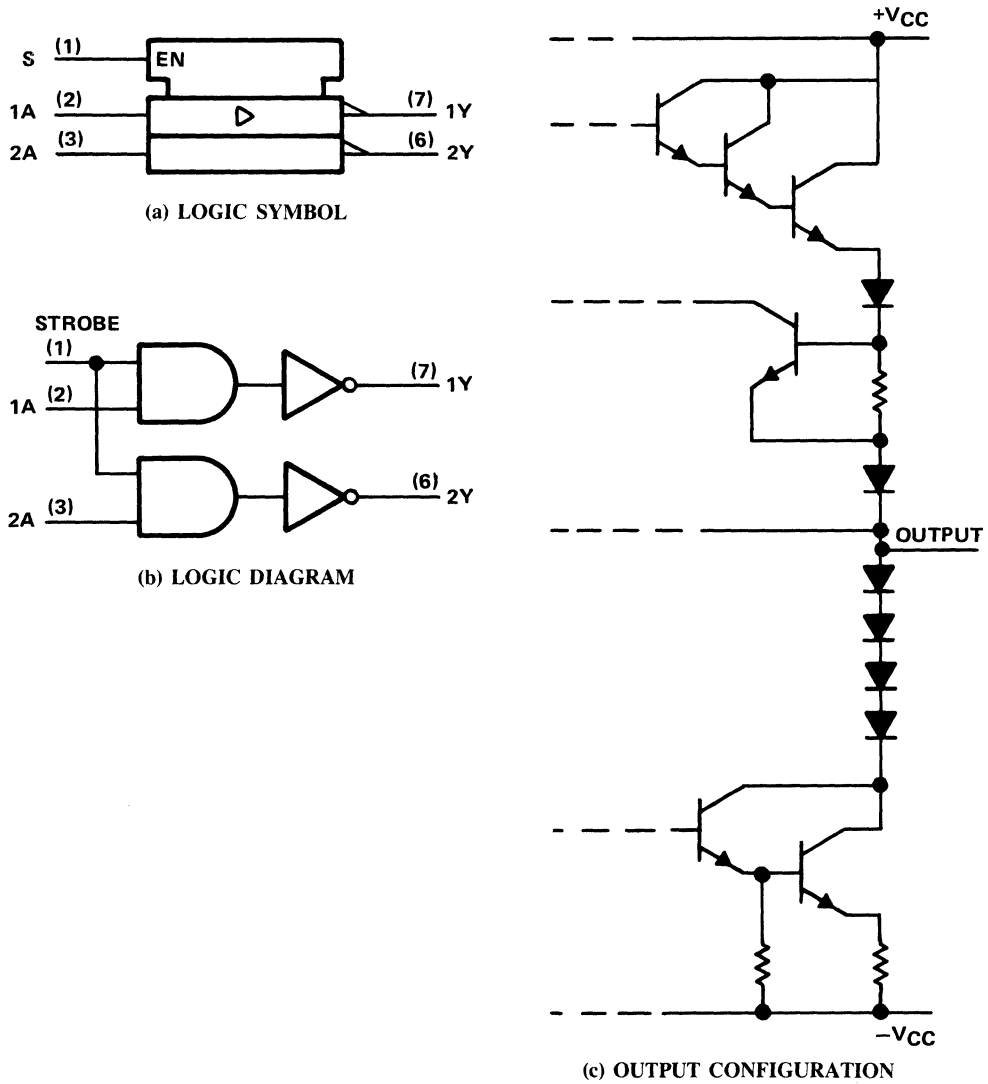


Figure 9-49. RS-232-C Drivers and Receivers in a Basic Data Communications System



(a) LOGIC SYMBOL

(b) LOGIC DIAGRAM

(c) OUTPUT CONFIGURATION

Figure 9-50. SN75150 Dual Line Driver

Table 9-8. RS-232-C Driver Requirements

Output short circuit	Must withstand short to either supply ground, or any conductor in the interface cable. Output current shall be <500 mA.
Output "power off" resistance	>300 Ω
Output open circuit voltage handling capability	0 to ±25 V
Output drive voltage 3 kΩ to 5 kΩ load	>5 V and <15 V
Output slew rate	<30 V per μs
Output rise and fall times within the transitional limits of 3 V and −3 V	≤1 ms or ≤4% of nominal signal duration; (whichever is less)
Maximum data rate	20,000 bits per second (bps)

adjusted by means of an external resistor (Figure 9-52) at the wave shaping (ws) pin. The transition time of the drivers can be adjusted from 1 μs to 100 μs.

SN75188/MC1488 Quad Line Driver

The SN75188 and MC1488 (Figure 9-53) are designed for use in conformance with EIA Standard RS-232-C. Following are key features of these devices:

- Current limited output — typically 10 mA.
- Power off output impedance — 300 Ω min.
- Slew rate control with load capacitor.
- Flexible supply voltage range (±9 V to ±12 V).
- TTL compatible inputs.

TYPICAL RECEIVERS FOR EIA RS-232-C APPLICATIONS

SN75152 Dual Data Line Receiver

The SN75152 (Figure 9-54) is a dual differential line receiver designed to meet the requirements of EIA standard RS-232-C or MIL-STD-188C interfacing. It is also used in other single-ended applications. A single control (pin 1) allows selection of input hysteresis for the desired application. In addition, the hysteresis may be adjusted to any range between ±0.3 V typical and ±5 V typical by means of the hysteresis adjust terminals (pins 4 and 13). Other key features include:

- Independent strobes.
- ±25 V common-mode input voltage range.
- Continuously adjustable hysteresis.
- Stable threshold voltages over supply and/or temperature.

For RS-232-C operation (Figure 9-55) the hysteresis control (pin 1) is connected directly to the negative V_{CC} rail (pin 9). This provides ±2.2 V thresholds at the input. To provide the correct input resistance, R_T(pin 6 channel 1 or pin 11 channel 2) is connected to the inverting line input (pin 5 channel 1 or pin 12 channel 2). Hysteresis adjust pins are left open and the strobes are connected to a logic high level when the channel is to be operational. Figure 9-55(a) illustrates typical circuit connections and Figure 9-55(b) shows the resulting input threshold hysteresis curve.

Table 9-9. RS-232-C Receiver Requirements

Input resistance	>3 kΩ and <7 kΩ
Input capacitive loading including connected cable	<2500 pF
Input voltage limits	±25 V
Input open circuit voltage	<2.0 V
Maximum data rate	20,000 bps

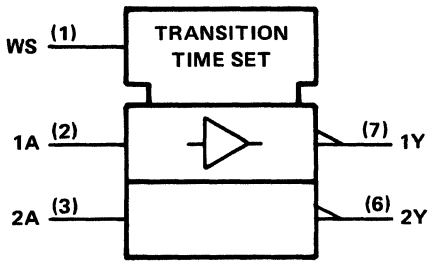
For MIL-STD-188C operation [Figure 9-56(a)], the hysteresis control (pin 1) and hysteresis adjust (pins 4 and 13) are left open. The resulting thresholds are ±0.3 V as illustrated in Figure 9-56(b). R_T, pins 6 and 11, are also left open to allow the input resistance to be about 9 kΩ, a MIL-STD-188C requirement.

A unique characteristic of the SN75152 is its capability of sensing input voltages above or below ground with a wide variety of hysteresis ranges. An example is the circuit, Figure 9-57(a), designed to detect input signals centered around −3.0 V with thresholds at −1.5 V and −4.5 V.The ability to maximize the receiver input hysteresis allows clean signal reception with minimum interference from noise signals. Figure 9-57(b) shows the input hysteresis for this application.

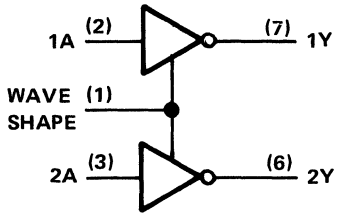
The SN75152 input hysteresis may be any value from ±0.3 V to ±5.0 V with thresholds anywhere from −25 V to 25 V (less the hysteresis value).

The value required for the hysteresis adjust resistor is selected from the graph, Figure 9-58. A 1.7 kΩ threshold adjust resistor provides the ±1.5 V hysteresis desired. The inverting input is biased to −3 V providing a basic reference level.

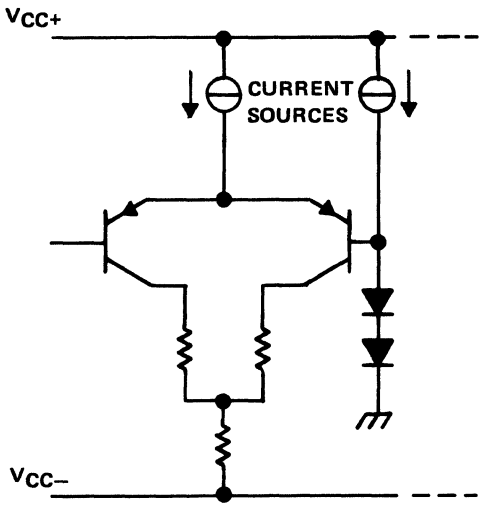
A typical application, combining the SN75150 dual driver and SN75152 dual receiver, is shown in Figure 9-59.



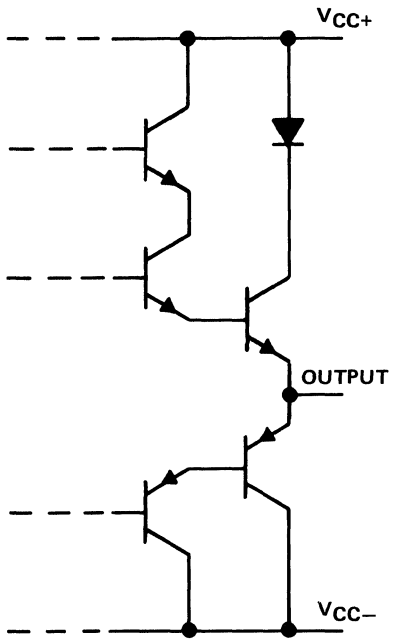
(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM



(c) EQUIVALENT OF EACH INPUT



(d) TYPICAL OF ALL OUTPUTS

Figure 9-51. SN75156 and uA9636 Dual Channel Line Drivers

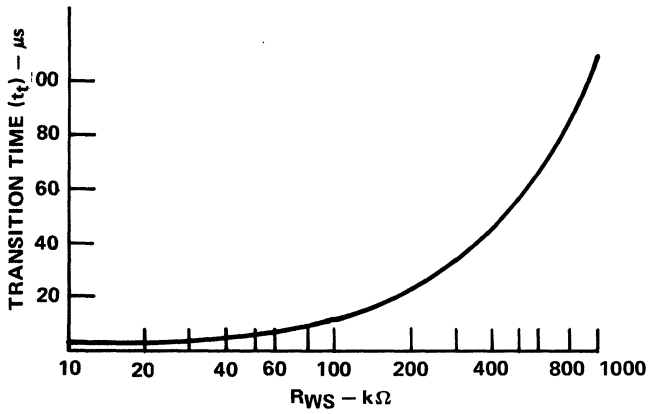


Figure 9-52. SN75156 Transition Time vs R_{WS}

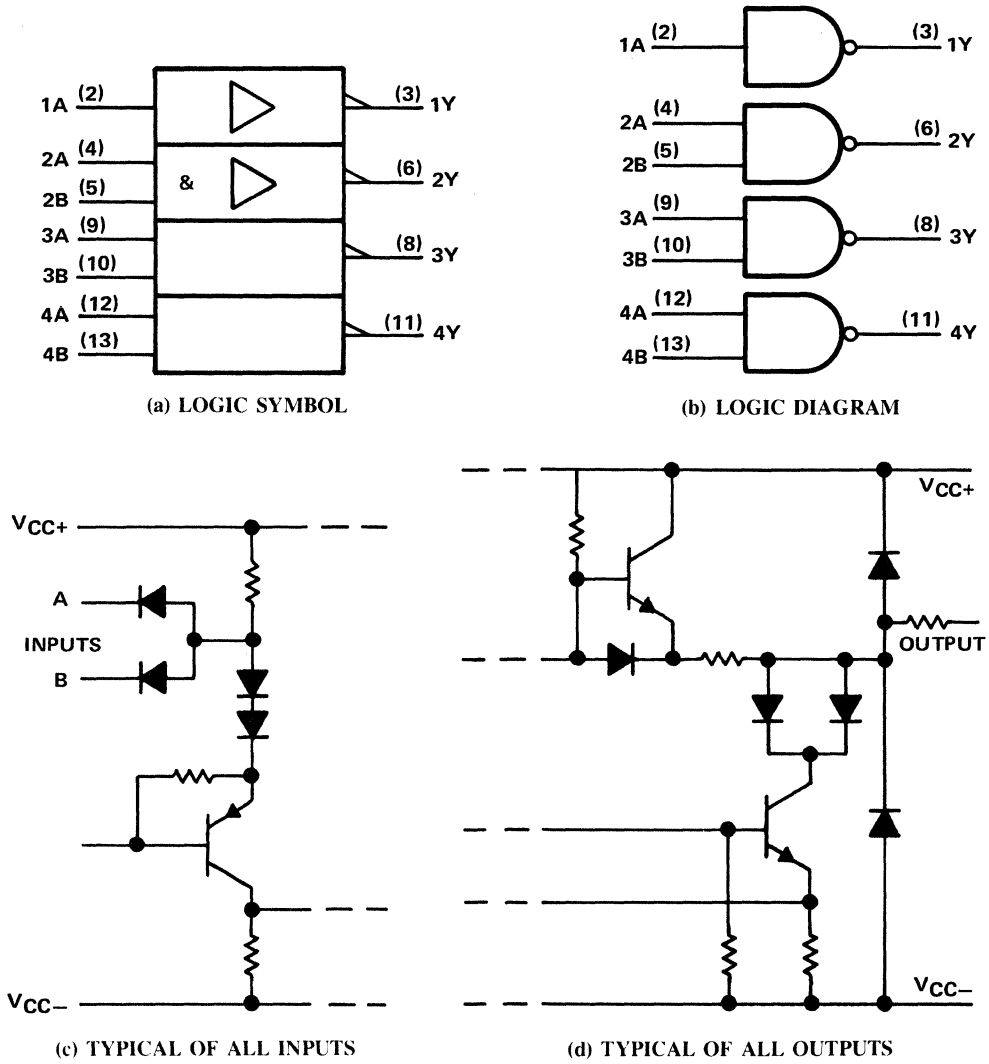


Figure 9-53. SN75188/MC1488 Quad Drivers

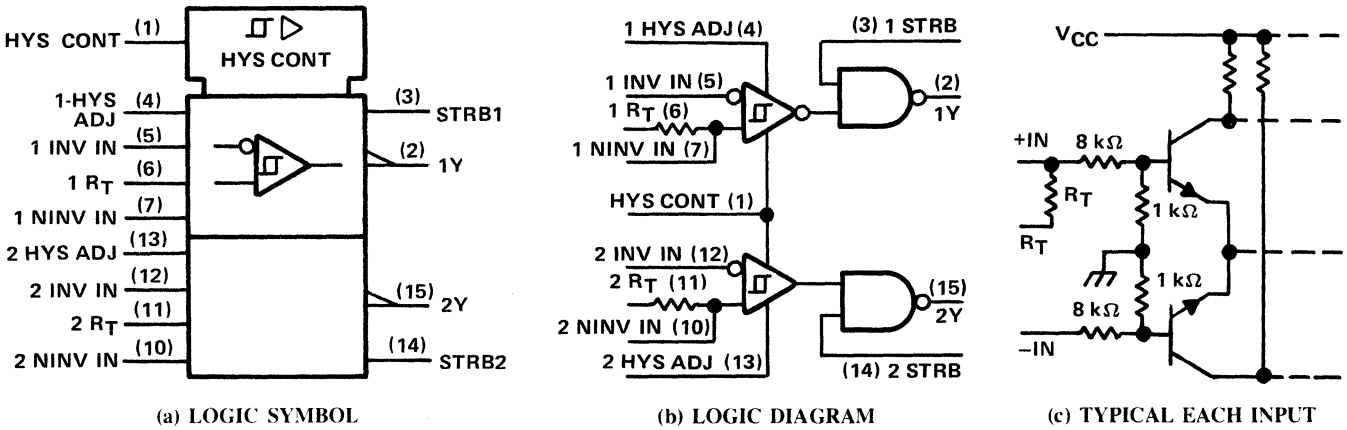
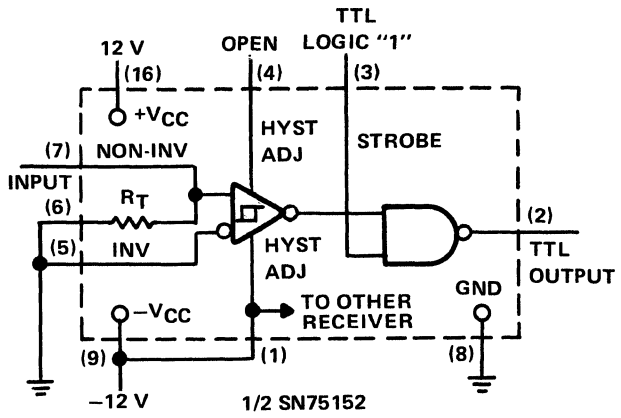
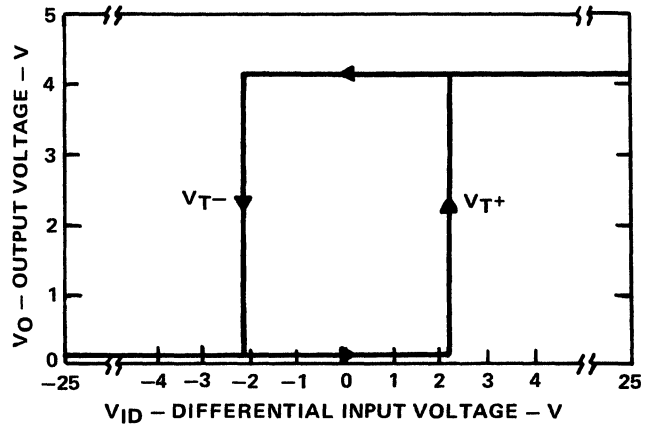


Figure 9-54. SN75152 Dual Line Receiver

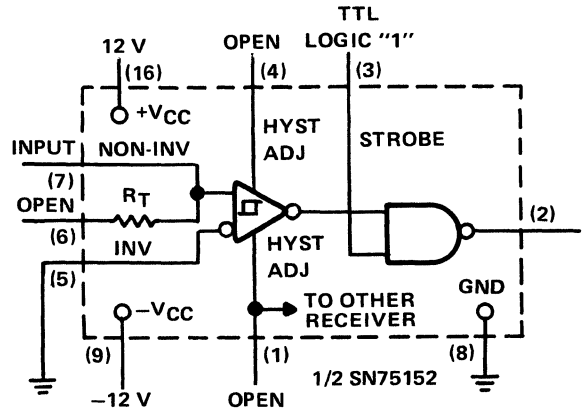


(a) EIA RS-232-C CIRCUIT CONFIGURATION

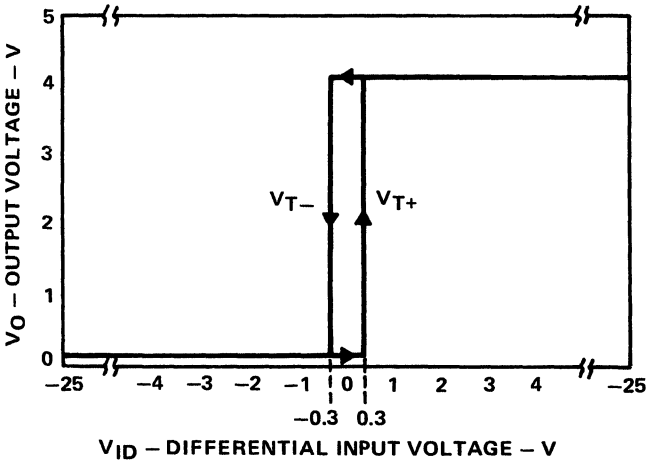


(b) V_{ID} VERSUS V_O in RS-232-C CONFIGURATION

Figure 9-55. SN75152 Circuit Connections and Results for EIA RS-232-C Application

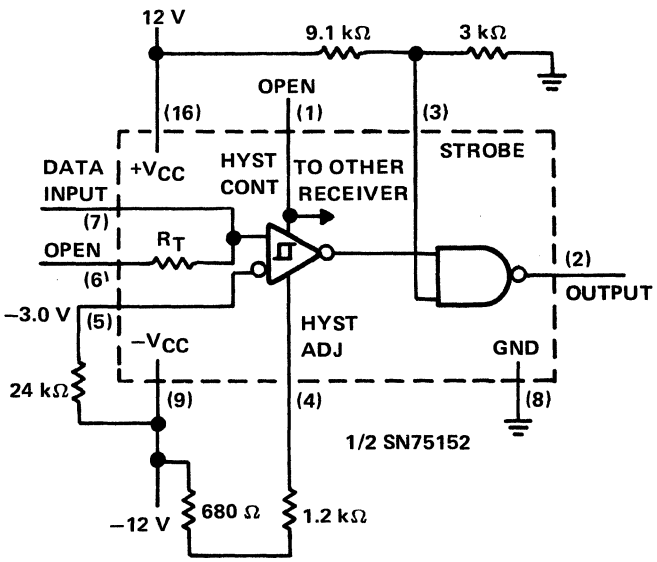


(a) MIL-STD-188C CIRCUIT CONFIGURATION

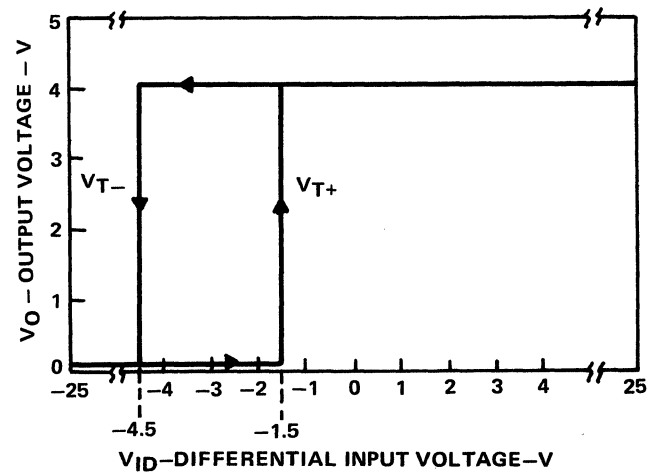


(b) V_{ID} VERSUS V_O in MIL-STD-188C CONFIGURATION

Figure 9-56. SN75152 Circuit Connections and Results for MIL-STD-188C Application



(a) −3 V THRESHOLD, ±1.5 V HYSTERESIS CIRCUIT CONFIGURATION



(b) RESULTING V_{ID} VERSUS V_O

Figure 9-57. Circuit Connections and Results for a Positive-Going Threshold of −1.5 V and a Negative-Going Threshold of −4.5 V

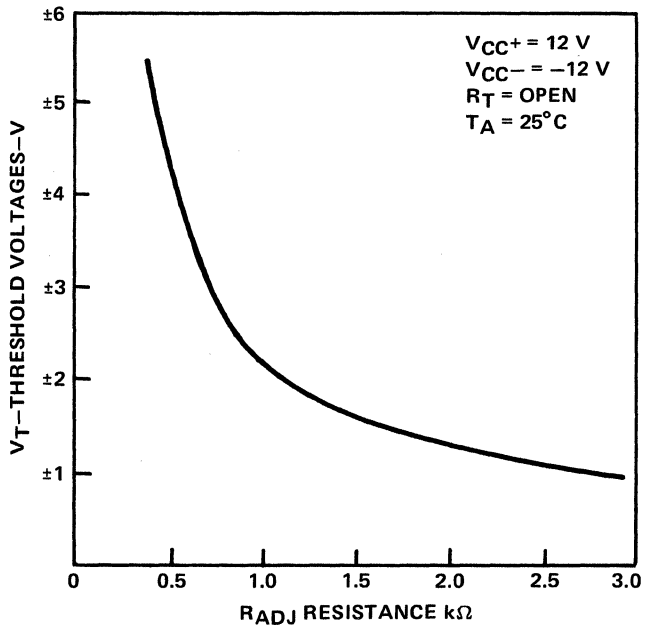


Figure 9-58. Threshold Voltage Versus Hysteresis Adjust Resistance

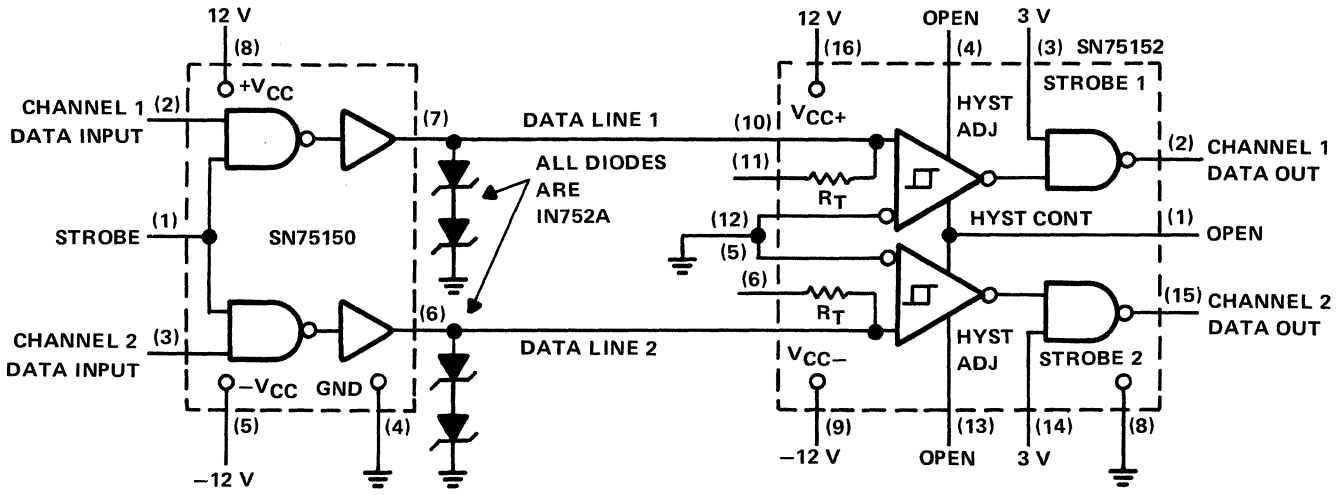


Figure 9-59. MIL-STD-188C Dual Channel Application with SN75150 and SN75152

As a MIL-STD-188C interface, this circuit meets paragraph 7.2 of the the standard governing the driver output and receiver input characteristics.

Back-to-back 1N752A zener diodes clamp the normally ±9 V driver output peaks to within the ±6 V required. The SN75152 input resistor terminal "R_T" is left open resulting in the 9 kΩ input resistance required. With the hysteresis control (pin 1) and the hysteresis adjust terminals (pins 4 and 13) open, the SN75152 will exhibit the ±0.3 V hysteresis condition desired for MIL-STD-188C.

Additional capacitance may be required at the driver outputs to ensure proper rise (t_r) and fall (t_f) times. Wave shaping capacitors must be within 8 inches of the driver output (as close as possible) and provide t_r and t_f values that are to ≤15% and ≥5% of a unit interval as described in Figure 9-60.

SN75154 Quad Data Line Receiver

The SN75154 (Figure 9-61) quad receiver is designed to satisfy EIA RS-232-C requirements as a data receiver in the interface applications between data terminal equipment and data communications equipment. It is also useful for relatively low frequency, short line, point-to-point data receiver applications and for logic level translations. Key features include:

- 3 kΩ to 7 kΩ input resistance.
- Input threshold adjustable.
- Built-in hysteresis.
- TTL compatible outputs.
- Operates from 5 V or 12 V supplies.

In normal operation, the threshold control terminals are connected directly to the V_{CC1} terminal, pin 15, even if power is being applied via the alternate V_{CC2} terminal,

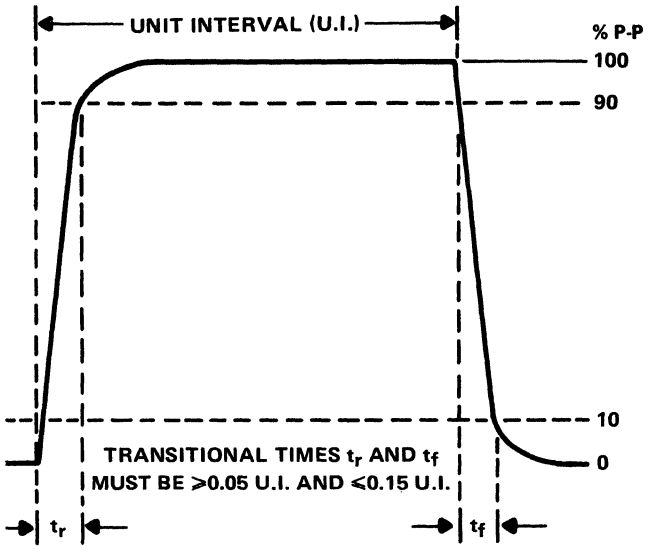


Figure 9-60. MIL-STD-188C Wave Shape Requirements

pin 16. This provides a wide hysteresis loop, [Figure 9-62(a)]. In this operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold terminals are left open [Figure 9-62(b)]. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero, (typically 1.4 V). The positive-going threshold voltage remains above zero, at typically 2.2 V, as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Figure 9-62(c) shows the specific condition of near zero negative-going threshold voltage achieved by connecting the threshold terminal (T) to R1 (pin 9). This places a 5 kΩ resistor between T and V_{CC1}. By using an external resistor, and connecting it between the threshold control pin and V_{CC1}, the negative-going threshold may be adjusted to various levels as shown in Figure 9-62(d).

SN75189, SN75189A, MC1489, and MC1489A Quad Line Receivers

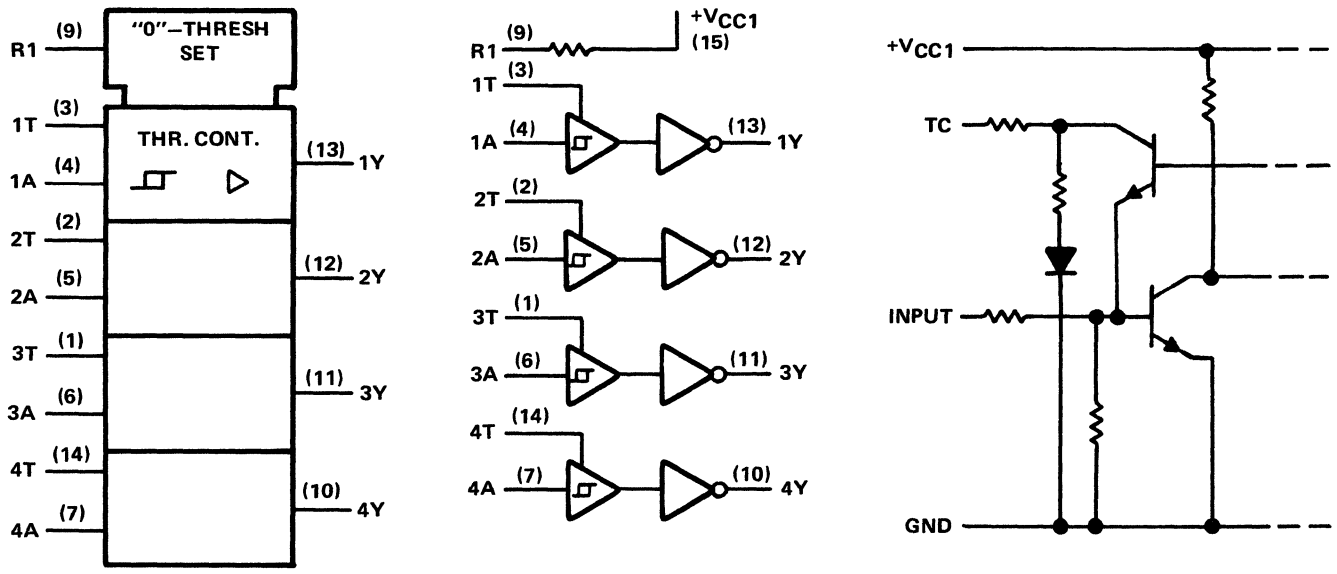
The SN75189 and SN75189A receivers (Figure 9-63) are designed to conform with EIA standard RS-232-C. Following are their key features:

- Satisfies EIA RS-232-C requirements.
- Built-in input hysteresis.
- Response control provides: input threshold shifting, input noise filtering.
- Operates from a single 5 V supply.
- TTL compatible outputs.

The SN75189 and SN75189A are quadruple line receivers designed to interface between data terminal equipment and data communication equipment in accordance with EIA standard RS-232-C. Each receiver has a response control terminal allowing adjustment of threshold levels and noise filtering.

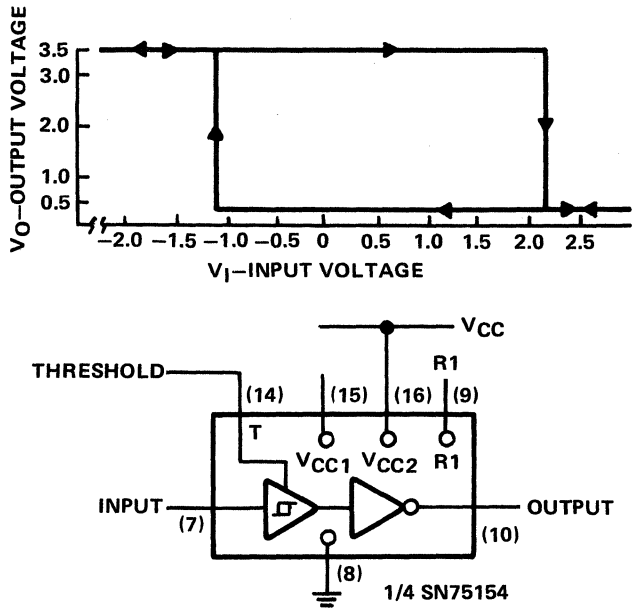
Without level shifting the SN75189 will have about 240 mV hysteresis with a positive-going threshold of 1.3 V and a negative-going threshold 1.06 V. Under the same conditions the SN75189A will have 930 mV hysteresis with typical thresholds at 1.9 V and 0.97 V. With wider hysteresis the SN75189A provides more immunity to noise than the SN75189. The threshold level may be adjusted by connecting a resistor from the receiver response control to the positive or negative V_{CC} rail. Figure 9-64 illustrates the effects of different resistor values on threshold level.

For normal EIA RS-232-C applications no bias resistor is used. A frequency compensating capacitor can be used to filter out noise spikes. Figure 9-65 shows the capacitor

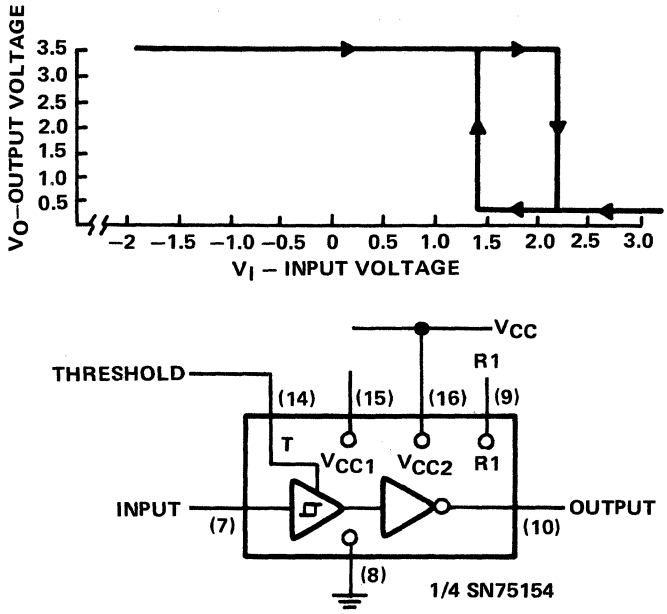


(a) LOGIC SYMBOL (b) LOGIC DIAGRAM (c) TYPICAL EACH INPUT

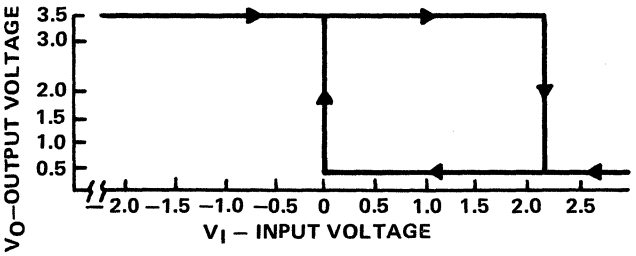
Figure 9-61. SN75154 Quad Data Line Receiver

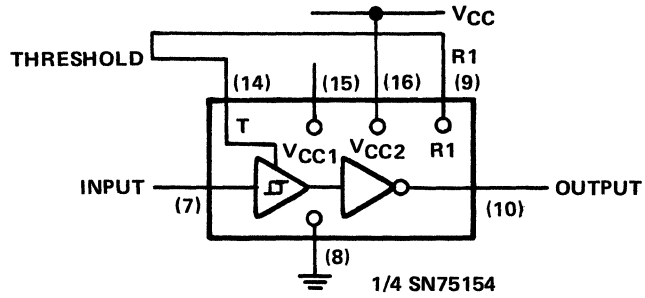


(a) NORMAL (EIA RS-232-C) OPERATION

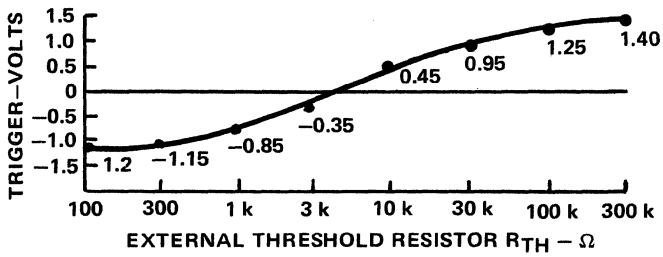


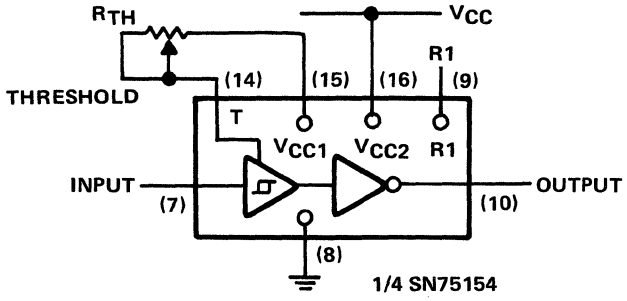
(b) FAIL-SAFE OPERATION





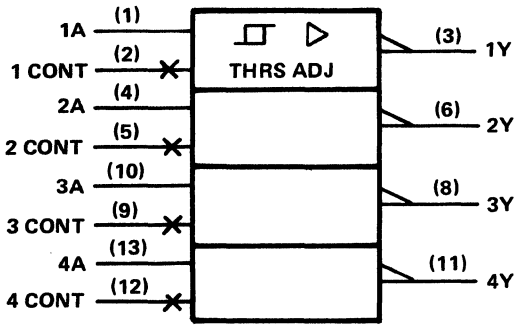
(c) ZERO NEGATIVE-GOING THRESHOLD



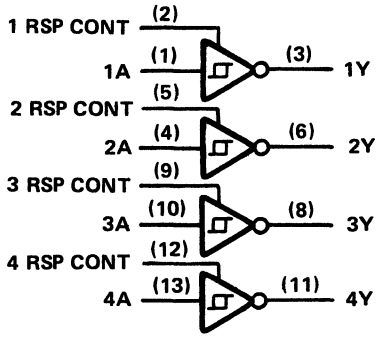


(d) NEGATIVE-GOING T_H VERSUS ADJUSTABLE HYSTERESIS R_{TH}

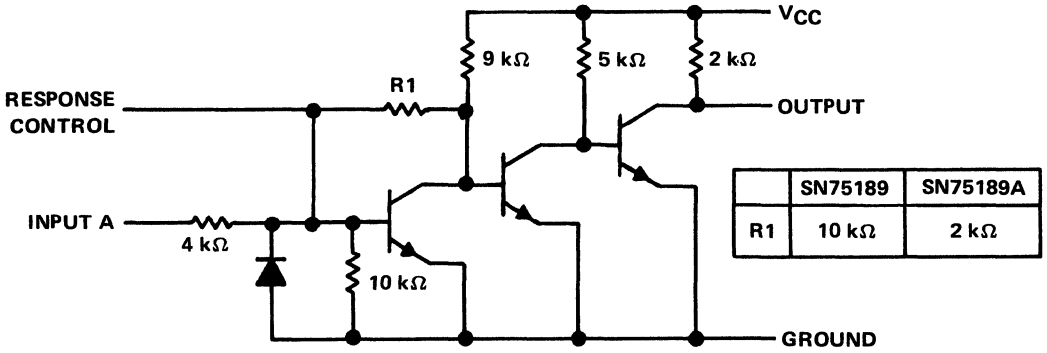
Figure 9-62. SN75154 Hysteresis Modes of Operation



(a) LOGIC SYMBOL

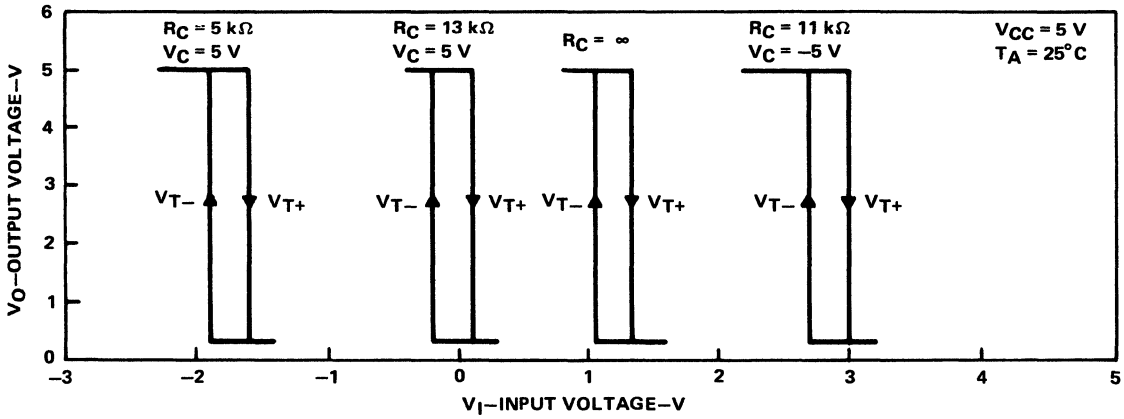


(b) LOGIC DIAGRAM

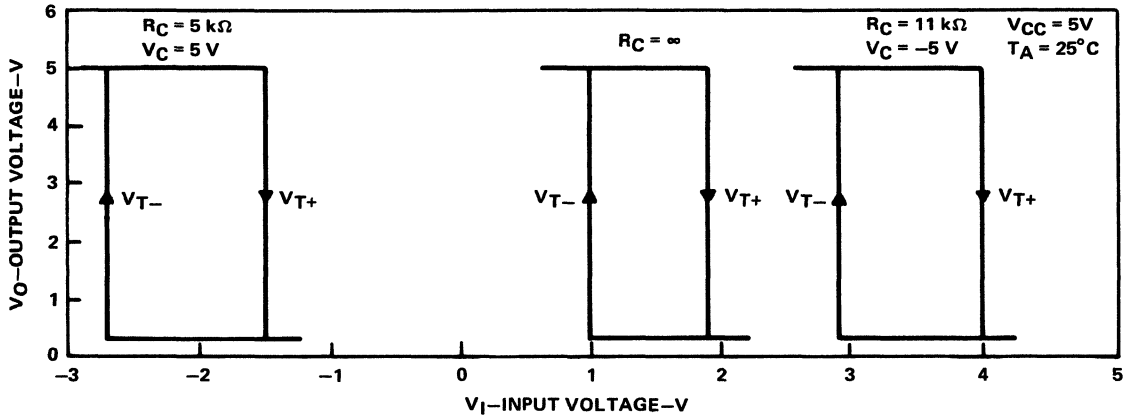


(c) SCHEMATIC (EACH RECEIVER)

Figure 9-63. SN75189/189A Quad Receiver

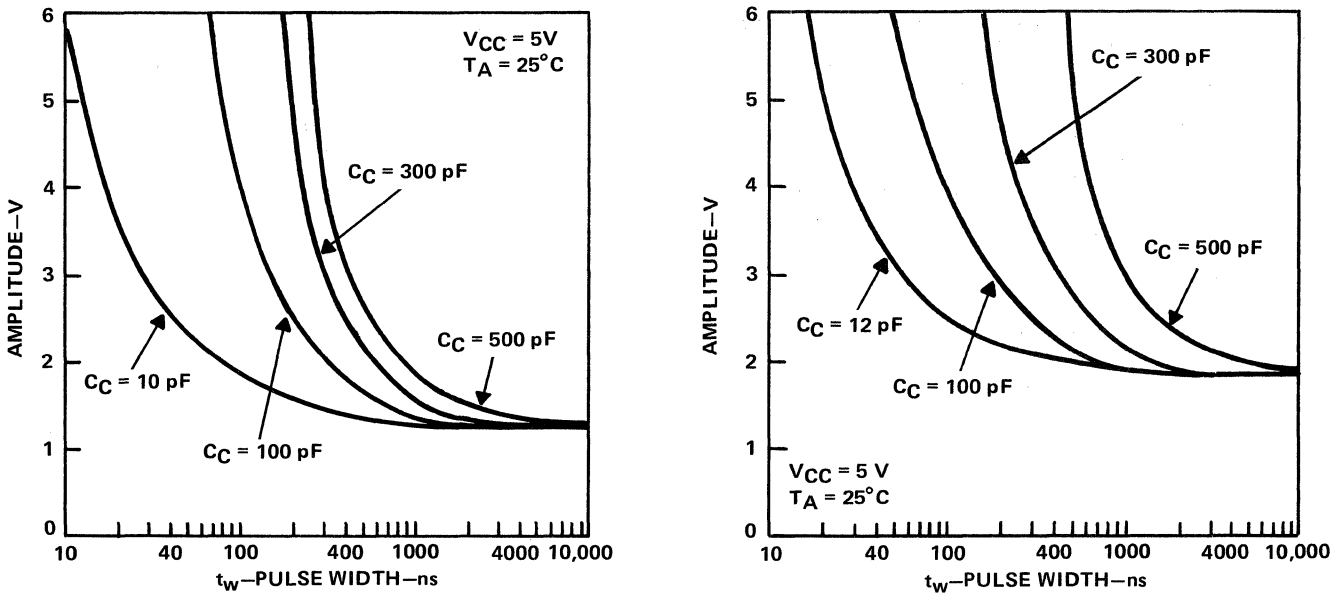


(a) SN75189



(b) SN75189A

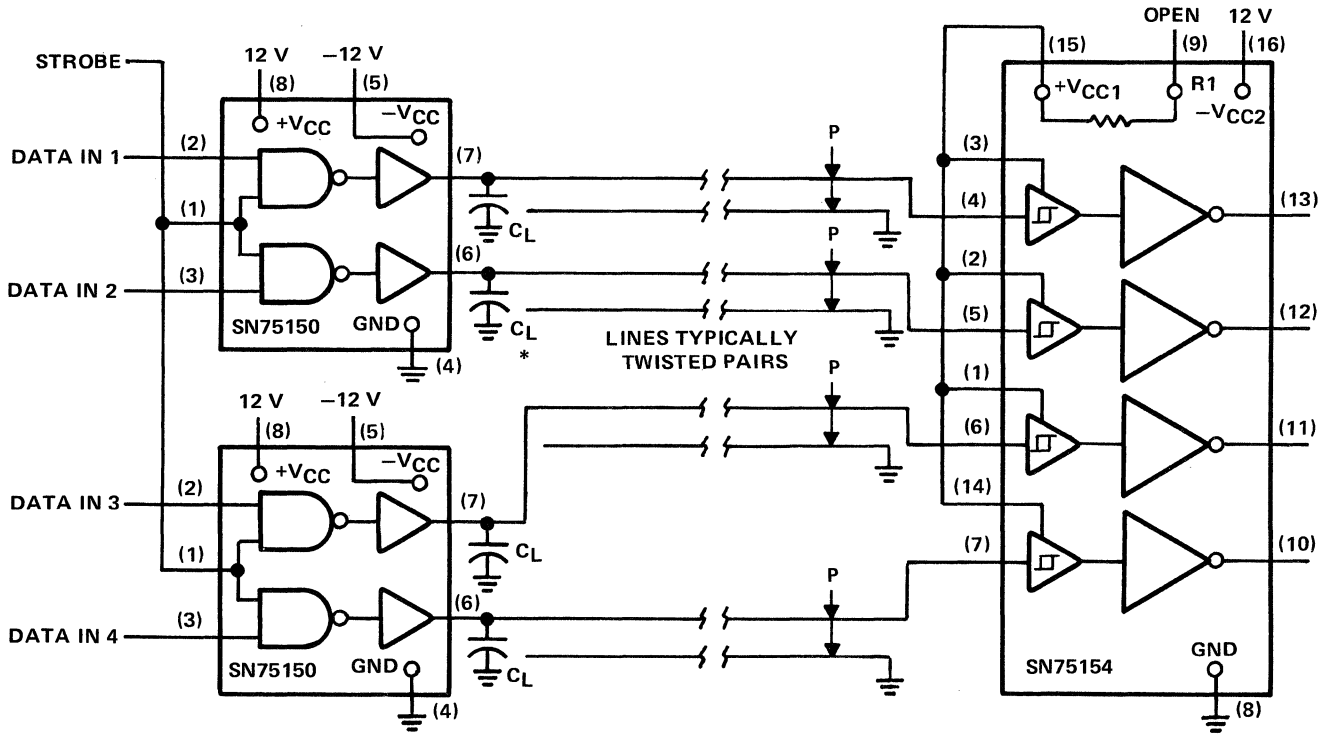
Figure 9-64. Output Voltage Versus Input Voltage for Various Control Pin Terminations



(a) SN75189 NOISE REJECTION

(b) SN75189A NOISE REJECTION

Figure 9-65. Noise Rejection Versus Compensation Capacitance for SN75189 and SN75189A



*C_L IS ONLY REQUIRED IF LINE CAPACITANCE IS INSUFFICIENT FOR PROPER WAVE SHAPING.

Figure 9-66. Basic RS-232-C Data Line Interface Using SN75150 and SN75154

value required to eliminate a noise spike knowing its amplitude and pulse width. These curves show the maximum input pulse amplitude that will not cause a change in the output level, for various pulse widths and response control capacitor values.

RS-232-C APPLICATIONS

Interface Using SN75150 and SN75154

Figure 9-66 illustrates a basic EIA RS-232-C interface configuration using SN75150 drivers and SN75154 receivers. Note that capacitive loads may be necessary at the driver

outputs to ensure compliance with the standard's wave shaping requirements. The RS-232-C defined transitional region is from −3 V to 3 V. Rising or falling transition times shall not be less than 0.2 μs. Transition speed maximum is therefore 6 V/0.2 μs or 30 V/μs. The maximum transitional time shall not exceed 1 ms. Figure 9-67 illustrates the permissible operating areas for driver transitions versus pulse rates. Figure 9-68 shows the SN75150 output transition times as a function of total load capacitance.

Typical Interface Using SN75188 and SN75189A

Figure 9-69 shows a typical EIA RS-232-C application using the SN75188 quad driver and the SN75189A quad receiver. In this application it is desirable to operate at data rates up to 4800 bps. Noise pulses of up to 4 V amplitude with pulse widths as wide as 300 ns may be experienced. From Figure 9-65 a C_C of 390 pF is chosen to provide the necessary noise rejection. Compensation of 390 pF will not adversely affect the circuit response to the desired signal.

The line used in this application has a capacitance of 230 pF. From Figure 9-70 we can see that the resulting slew rate would be a little over 40 V/μs. The EIA RS-232-C maximum is 30 V/μs. It is desirable to operate within the limit and therefore 20 V/μs is chosen. From Figure 9-70, 20 V/μs will require a total load capacitance of 500 pF. An external capacitor of 270 pF is connected directly from the driver output to ground to properly limit the output slew rate.

EIA STANDARD RS-423-A CIRCUITS AND APPLICATIONS

RS-423-A STANDARD

This standard specifies the electrical characteristics of unbalanced voltage-mode digital interface circuits normally used for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). Values are given for both the driver and receiver characteristics. Devices designed to meet EIA RS-423-A are used for low speed data communication or control functions. They may be used, under certain conditions, with drivers and receivers of other digital interface standards such as EIA RS-232-C and MIL-STD 188C. Figure 9-71 shows the basic unbalanced digital interface configuration typical of EIA RS-423-A systems. RS-423-A allows one driver and up to 10 receivers on a single data line. Basic requirements for RS-423-A type data line drivers and receivers are in Table 9-10 and Table 9-11.

RS-423-A DEVICES

RS-423-A Drivers

The SN75156 and uA9636 are good examples of EIA RS-423-A drivers. These parts are shown in Figures 9-51 and 9-52 and discussed in the section on RS-232-C drivers

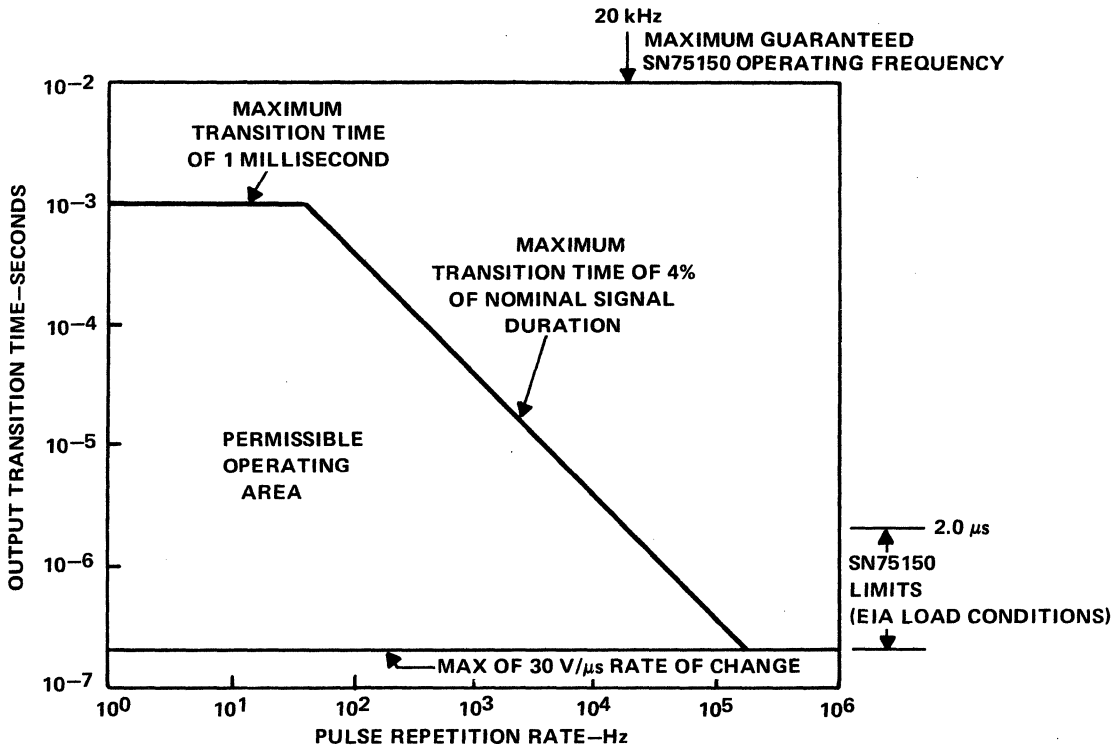


Figure 9-67. Pulse Repetition Rate Versus Output Transition Time of SN75150

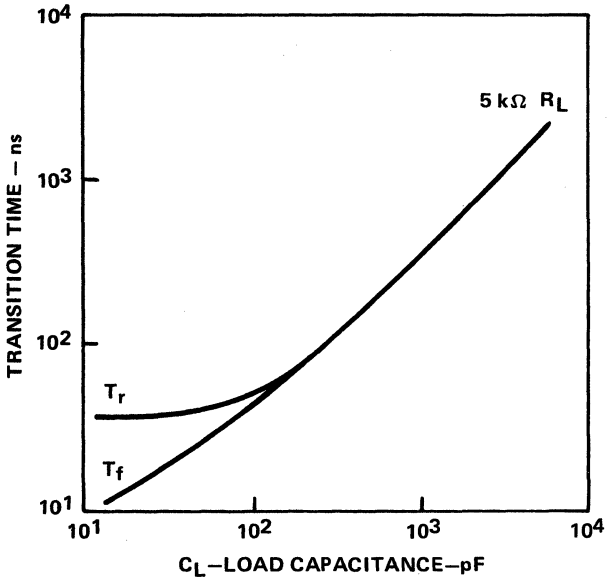


Figure 9-68. Output Transition Times Versus Total Load Capacitance

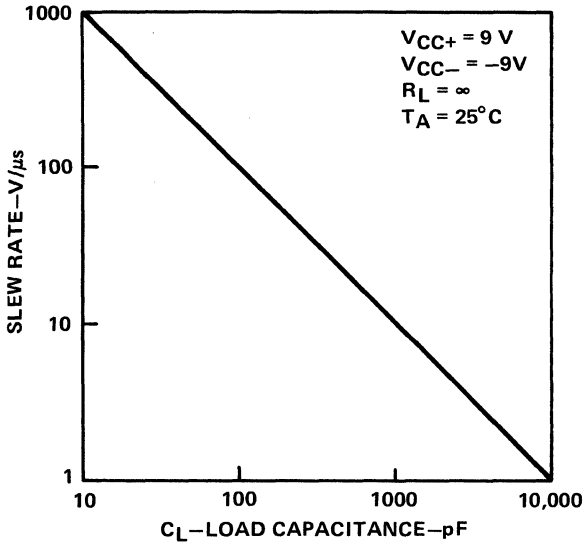


Figure 9-70. Slew Rate Versus Load Capacitance

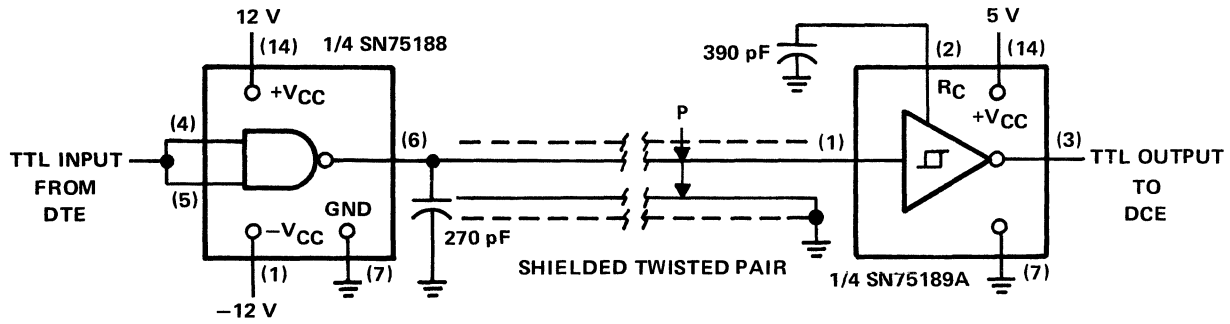


Figure 9-69. Typical EIA RS-232-C Interface Using SN75188 and SN75189A

Table 9-10. RS-423-A Driver Requirements

Output drive voltage open circuited output	V_O	±4 V to ±6 V.
Output drive voltage terminated in 450 Ω	V_t	≥ 0.9 V_O.
Output short circuit current	I_S	< 150 mA with output in either logic state.
Output leakage current (with power off)	I_X	< 100 μA with output voltage of –6 V to 6 V.
Output slew rate	S_R	Shall not exceed 15 V/μs at any point during the transitional period.
Output monoticity		The output shall be monotonic between 0.1 and 0.9 V_{SS} (See Figure 9-72).
Transitional time	t_r	For pulse widths of 1 ms or greater, the transitional time measured between 0.1 and 0.9 V_{SS} shall be between 100 μs and 300 μs.
Ringing (overshoot or undershoot)		After completing a transition from one logic state to the other, the signal voltage should not vary more than 10% of V_{SS} from the steady state value until the next transition occurs (See Figure 9-72).

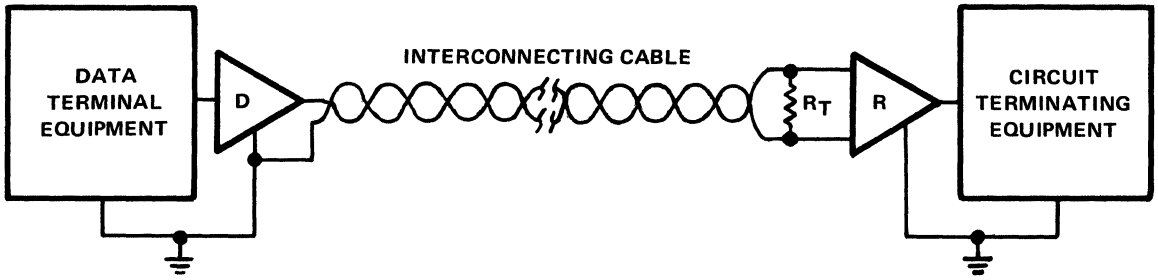


Figure 9-71. Basic RS-423-A Unbalanced Digital Interface

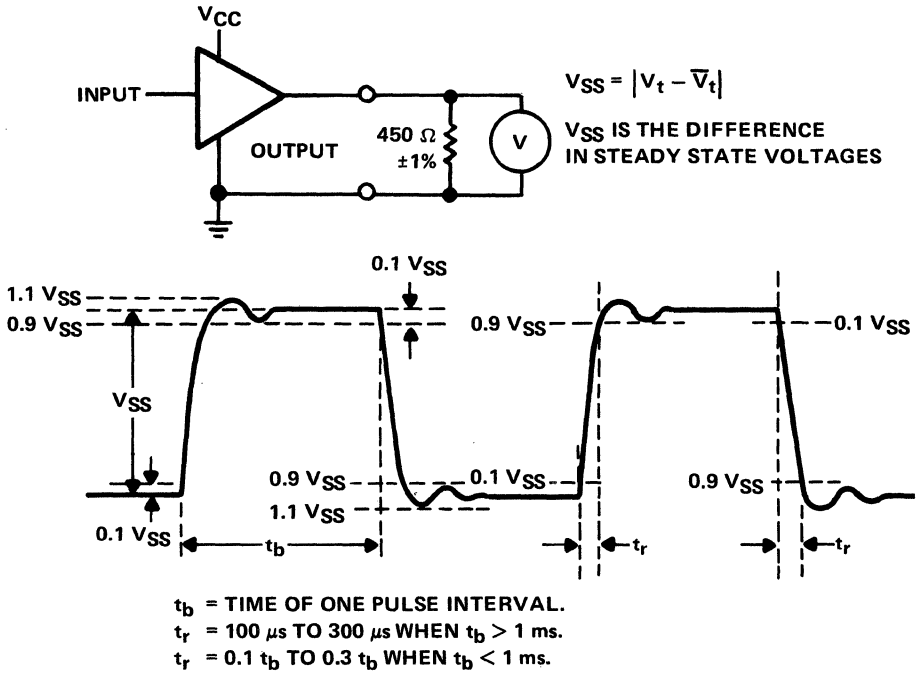


Figure 9-72. Signal Wave Shaping Requirement

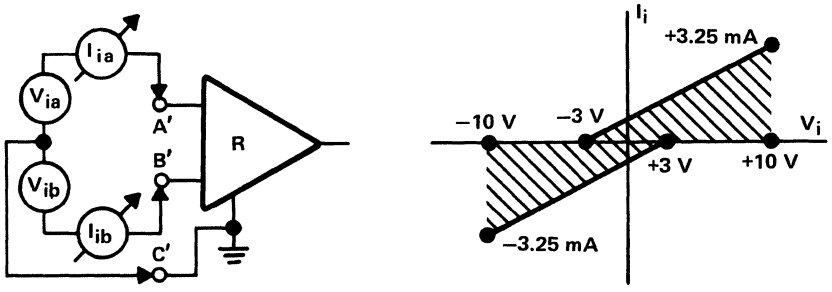


Figure 9-73. Receiver Input Current-Voltage Measurement

Table 9-11. RS-423-A Receiver Requirements

Input current at either input with the other input grounded and an applied input voltage of −10 V to 10 V.	I_{IN}	The input current shall remain within the shaded area of the graph in Figure 9-73.
Input resistance	R_{IN}	4 kΩ minimum under power on or power off conditions.
Input sensitivity over an input common-mode range of −7 V to 7 V. Referred to as differential input threshold voltage. (Figure 9-74)	V_{TH}	The differential input required to ensure the receiver will correctly assume the intended binary output state is 200 mV. The receiver must also maintain correct operation for differential input voltages from 200 mV to 6 V.
Differential input voltage maximum	V_{ID} (max)	The maximum V_{ID} without resulting in damage to the receiver is 12 V.
Input balance with any common-mode voltage from −7 to 7 V		Input voltage balance characteristics shall be such that the receiver will remain in its intended state with a differential voltage of 400 mV applied through 500 Ω (±1%) to each input (See Figure 9-75). V_{ID} polarity is reversed for the opposite binary state.
Multiple receivers and total loading		Up to 10 receivers may be connected on a single line. Total loading of multiple receivers and added fail safe circuits must have a resistance of 400 Ω or greater.
Recommended grounding		The signal ground wire, or common, should be grounded only at the driver end of the data line (See Figure 9-77).

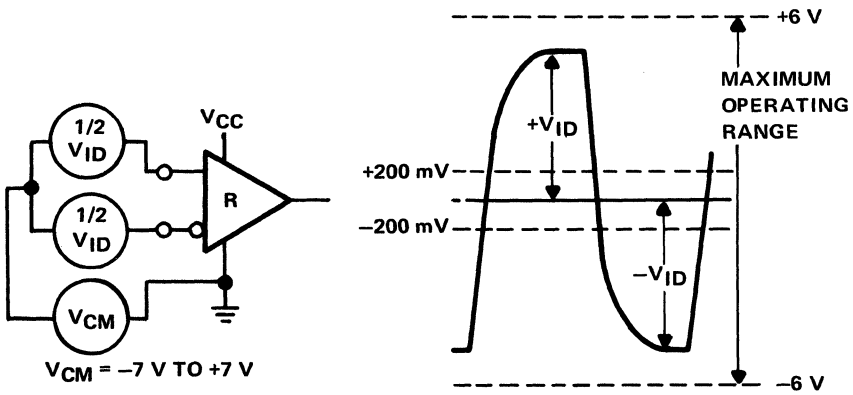


Figure 9-74. Receiver Input Sensitivity Test

as they were designed to meet both standards. In addition these drivers meet CCITT recommendations V.10, V.28 and X.26 as well as the Federal Standard FIPS 1030.

RS-423-A Receivers

Receivers designed to meet RS-423-A requirements normally have differential inputs. Thus they are generally compatible with EIA standard RS-422-A as well.

The SN75157 and uA9637A are examples of devices that fit both EIA standards RS-422-A and RS-423-A as well as Federal Standards 1020 and 1030. Figure 9-76 illustrates the logic diagram and symbol, package pinouts and equivalent input circuit for these devices.

BASIC RS-423-A APPLICATION

Figure 9-77 is an example of a Data Terminal with a remote monitor and printer using EIA RS-423-A circuits to interface data and control signals. The SN75156 dual driver and SN75157 dual receiver are used to provide the RS-423-A interfacing.

In this application, the data rate is to be 5 kilobaud resulting in a pulse width, t_b, of 200 μs. From Figure 9-72, the required transitional times must be between 0.1 and 0.3 t_b or between 20 and 60 μs. A driver waveshaping resistor of 330 kΩ (selected from Figure 9-52) provides about 40 μs transitional times.

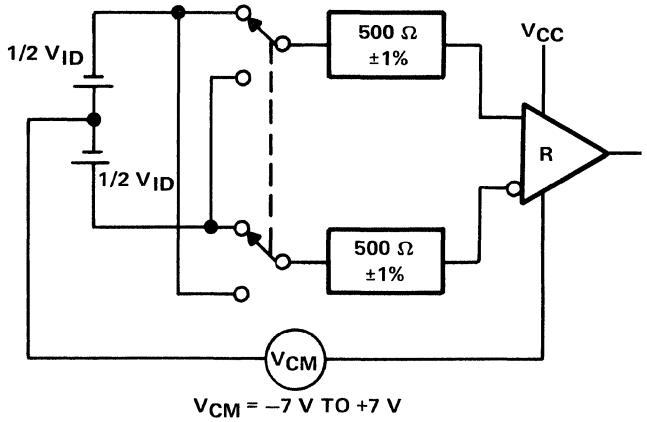


Figure 9-75. Receiver Input Balance Test

In this type of application, the data transmission line ground lead is connected to ground at the driver end of the line only. Each line is terminated in its characteristic impedance at the most remote end of the line. In this example 120 Ω resistors are used.

Although this application requires only two receiver stations per data line, as many as 10 receiver stations per line may be employed in an RS-423-A system.

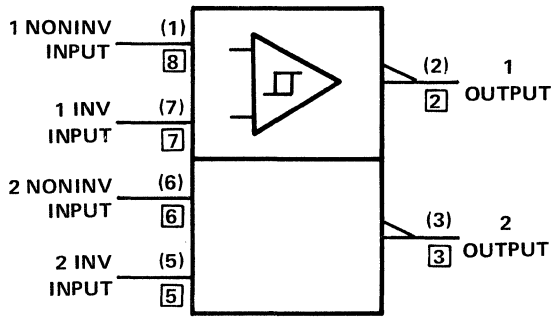
EIA STANDARD RS-422-A AND RS-485 CIRCUITS AND APPLICATIONS

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements. As was seen with general purpose balanced data transmission, the ability to cope with common-mode voltages allows a differential (balanced) receiver to receive and reproduce signals that otherwise would be unusable.

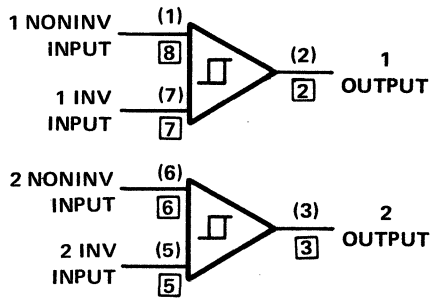
A comparison of the single-ended EIA RS-232-C and RS-423-A standards with the differential EIA RS-422-A and RS-485 standards is shown in Table 9-12. The balanced system of data transmission incorporates a differential driver transmitting on balanced interconnecting lines to a receiver with differential inputs.

RS-422-A STANDARD

The balanced voltage digital interface circuit is normally used for data, timing or control lines where the signaling

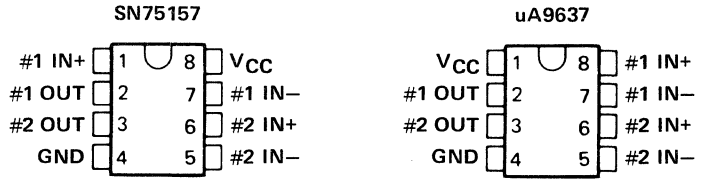


(a) LOGIC SYMBOL

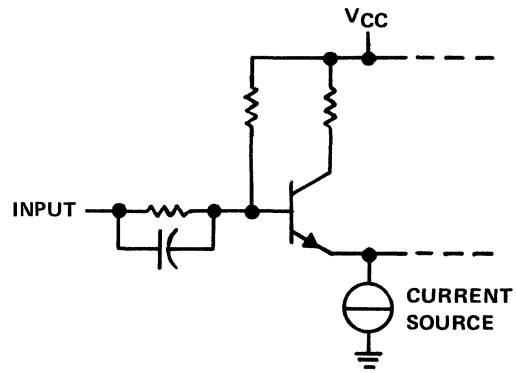


(b) LOGIC DIAGRAM

( ) SN75157 PIN NUMBERS
□ uA9637 PIN NUMBERS



(c) PACKAGE PINOUTS



(d) EQUIVALENT OF EACH INPUT

Figure 9-76. SN75157 and uA9637 Dual RS-423-A Receivers

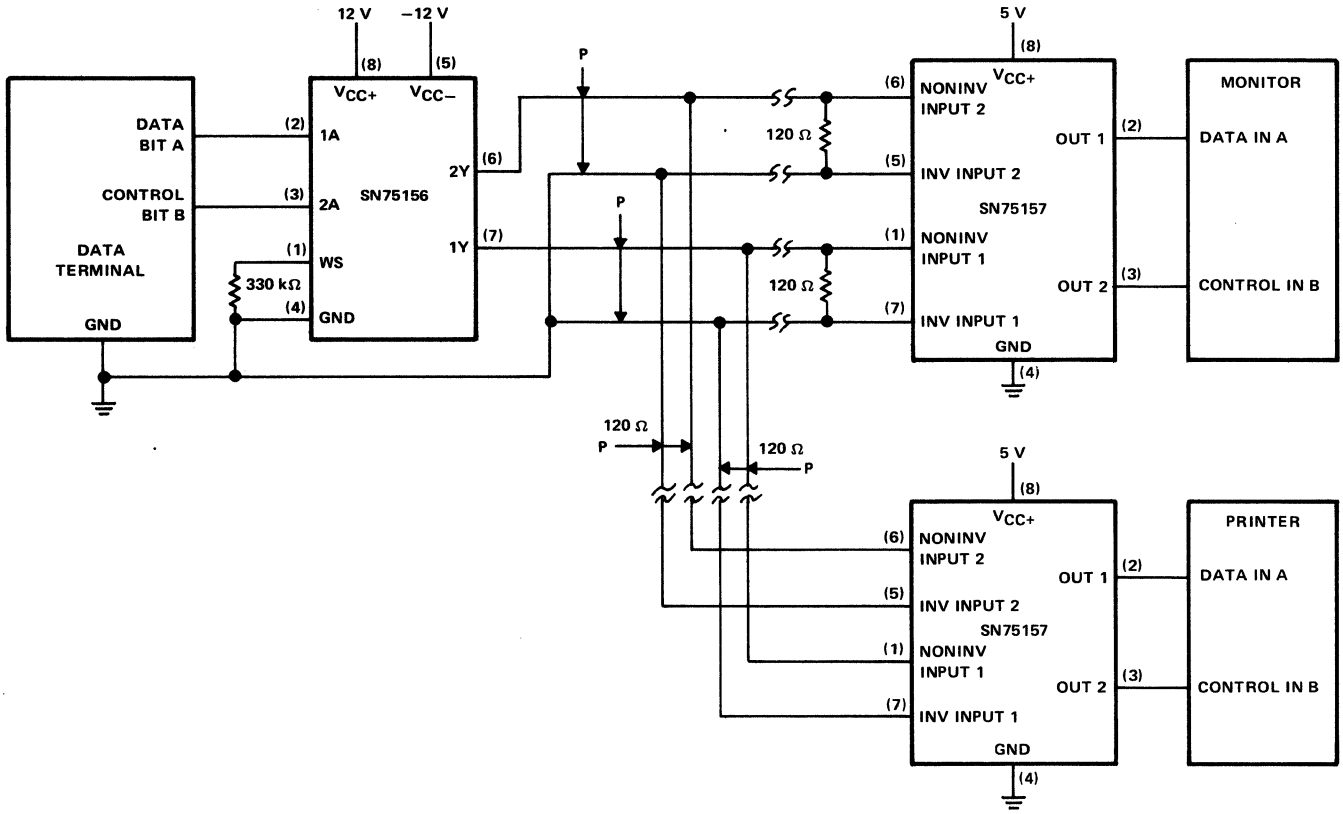
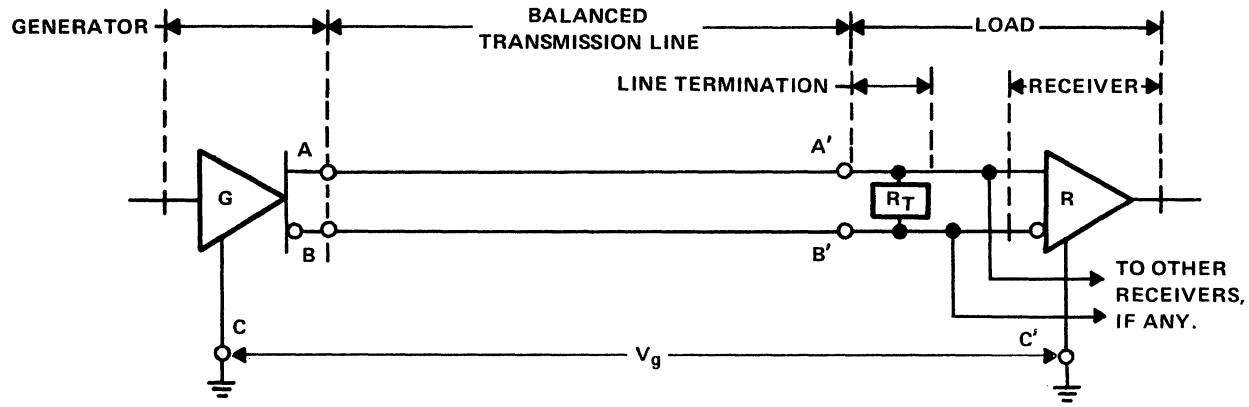


Figure 9-77. Basic EIA RS-423-A Application

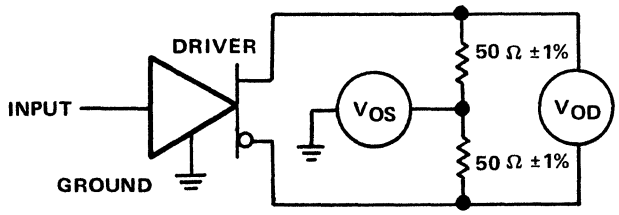
Table 9-12. Popular General Purpose EIA Line Circuit Standards

PARAMETER		RS-232-C	RS-423-A	RS-422-A	RS-485
Mode of operation		Single-ended	Single-ended	Differential	Differential
Number of drivers and receivers allowed		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum cable length (ft)		50	4000	4000	4000
Maximum data rate bits per second		20k	100k	10M	10M
Maximum common-mode voltage		±25 V	±6 V	6 V −0.25 V	12 V −7 V
Driver output		±5 V min ±15 V max	±3.6 V min ±6.0 V max	±2 V min	±1.5 V min
Driver load		3 kΩ to 7 kΩ	450 Ω min	100 Ω min	60 Ω min
Driver slew rate		30 V/μs max	Externally controlled	NA	NA
Driver output short circuit current limit		500 mA to V_{CC} or GRD	150 mA to GRD	150 mA to GRD	150 mA to GRD 250 mA to −8 V or 12 V
Driver output resistance (High Z state)	Power on	NA	NA	NA	120 kΩ
	Power off	300 Ω	60 kΩ	60 kΩ	120 kΩ
Receiver input resistance Ω		3 kΩ to 7 kΩ	4 kΩ	4 kΩ	12 kΩ
Receiver sensitivity		±3 V	±200 mV	±200 mV	±200 mV



LEGEND: R_T = Terminating resistance, V_g = Ground voltage difference
A, B = Generator-Line Interface, A', B' = Load-Line interface
C = Generator ground C' = Load ground.

Figure 9-78. Balanced Digital Interface



V_{OD} = DIFFERENTIAL OUTPUT VOLTAGE
V_{OS} = DRIVER OUTPUT OFFSET VOLTAGE

Figure 9-79. Driver Output Voltage Test Circuit

rates are from 100 kbps to 10 Mbps. RS-422-A specifications do not place restrictions on minimum or maximum operating frequencies but rather on the relationship of transitional speeds to a unit interval.

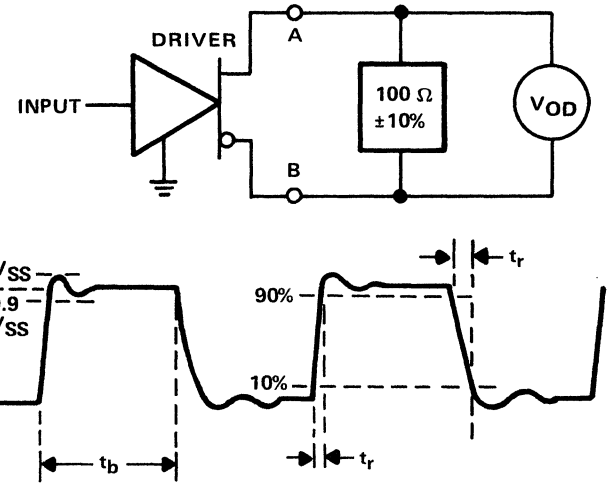
Although single-ended transmission circuits are normally used at lower frequencies, differential transmission on balanced lines may be preferred under the following conditions:

A. Interconnecting lines too long for effective unbalanced operation.
B. Transmission lines exposed to large electrostatic or electromagnetic noise levels.
C. When simple inversion of the signals may be desired (obtained by reversing the balanced lines).

A basic balanced digital interface circuit (seen in Figure 9-78) consists of three parts:

A. The generator (G) or data line driver.
B. A balanced transmission line.
C. The loads, where a load may consist of one or more receivers (R) and the line termination resistor (R_T).

The RS-422-A type of driver has a balanced (differential) output voltage source with an impedance of 100 Ω or less. Its output differential voltage is in the range of 2.0 V minimum to 6.0 V maximum. Additionally, the output voltage of either output, with respect to ground, shall not exceed 6.0 V.



t_b = time of one unit interval
t_r = transitional times between the 10% and 90% of V_{SS} levels.
$t_r \leq 0.1\ t_b$ when t_b is greater than 200 ns.
$t_r \leq 20$ ns when t_b is less than 200 ns.
V_{SS} = difference between output steady state levels ($V_{OD}-\overline{V}_{OD}$)

Figure 9-80. Driver Transitional Characteristics

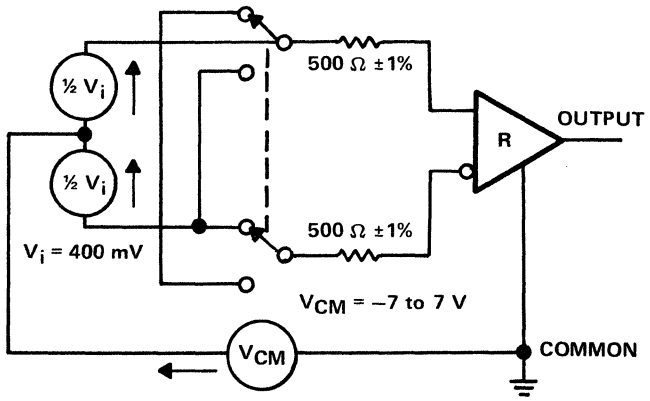


Figure 9-81. Receiver Input Balance Test

Output voltage balance is defined as follows:

The output differential voltage (V_{OD}) shall not be less than 2.0 V with two 50 Ω (±1%) termination resistors connected in series between the outputs. The difference between opposite polarity differential output voltages must be less than 0.4 V (see Figure 9-79).

The driver output offset voltage (V_{OS}), measured from the junction of the two 50 Ω terminators and

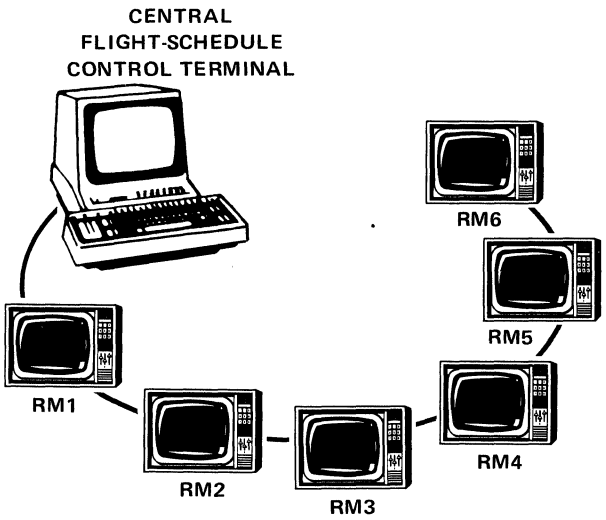


Figure 9.82. Basic RS-422-A Application

driver ground, shall not exceed 3.0 V (either polarity). The magnitude of the change in V_{OS} must be less than 0.4 V for opposite polarity differential output voltages.

Drive output current, with either output shorted to ground, shall not exceed 150 mA. Output off-state leakage

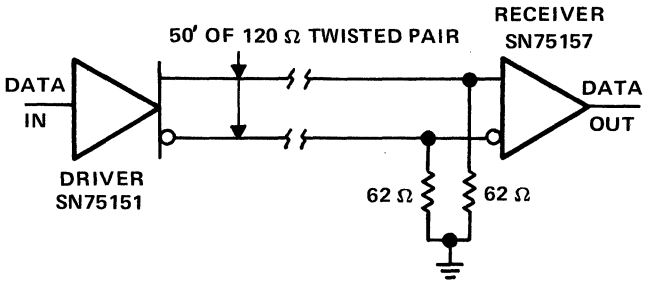


Figure 9-83. Short Line RS-422-A Application

current, with any voltage between −0.25 V and 6.0 V applied to either output, shall not exceed 100 μA.

As illustrated in Figure 9-80, output voltage transition times (t_r) are the transitional times between 0.1 and 0.9 of V_{SS} and must occur within 10% of a unit interval (t_b) or 20 ns, whichever is greater.

Ringing and resulting overshoot and undershoot shall not, as illustrated in Figure 9-80, exceed 10% of V_{SS} where V_{SS} is defined as the difference between the two steady-state values of the output.

RS-422-A receiver characteristics for balanced-line applications are basically the same as those for the RS-423-A single-ended applications. Basic receiver input requirements are as follows:

Differential data input threshold sensitivity of ±200 mV over a common-mode (V_{CM}) range of −7 to 7 V. Input impedance of greater than or equal to 4 kΩ.

The receiver's input voltage-current characteristics shall be balanced such that its output remains in the intended binary state with a differential input of 400 mV applied, (through 500 Ω ±1% to each input terminal as illustrated in Figure 9-81), and V_{CM} is varied between −7 V and 7 V.

An RS-422-A receiver shall not be damaged, when powered-on or powered-off under the following conditions:

1. Driver output off (open circuit).
2. A short across the data line.
3. A short from either, or both, lines to ground.

RS-422-A drivers and receivers are compatible with CCITT recommendation V.11 and X.27. RS-422-A drivers and receivers are not intended for operation with RS-232-C, MIL-STD-188C, MIL-STD-188-100, or CCITT recommendations V.28 and V.25.

RS-422-A APPLICATIONS

Typical Application

A typical application of an RS-422-A is its use in communicating data from a central computer to multiple remote monitors or stations, such as airport arrival and departure monitors (see Figure 9-82).

In this application, a single twisted pair line is used to connect the central control terminal with several remote monitors distributed throughout the airport. Line termination would be at the most remote end from the control terminal (remote monitor 6). To minimize line noise it may be desirable to use two terminating resistors, with values of $R_T/2$, one from each line to ground.

Short-Line Application

Even in less complex applications the good noise rejection capability of RS-422-A type circuits may be advantageous. Figure 9-83 illustrates a simple, short-line, dedicated single driver and single receiver application with very good noise handling capability.

This combination of RS-422-A driver and receiver will provide −0.25 to 6.0 V common-mode capability and operate at speeds up to 20 Mbps. For improved negative noise voltage rejection capability it would be necessary to use a driver with more negative common-mode capability. The SN75172B driver is such a device with −7 to 7 V common-mode range. The SN75175 receiver also has a −7 to 7 V input capability, allowing very good overall noise performance for the pair.

EIA RS-485 STANDARD

EIA standard RS-485, introduced in 1983, is an upgraded version of EIA RS-422-A. Increasing use of

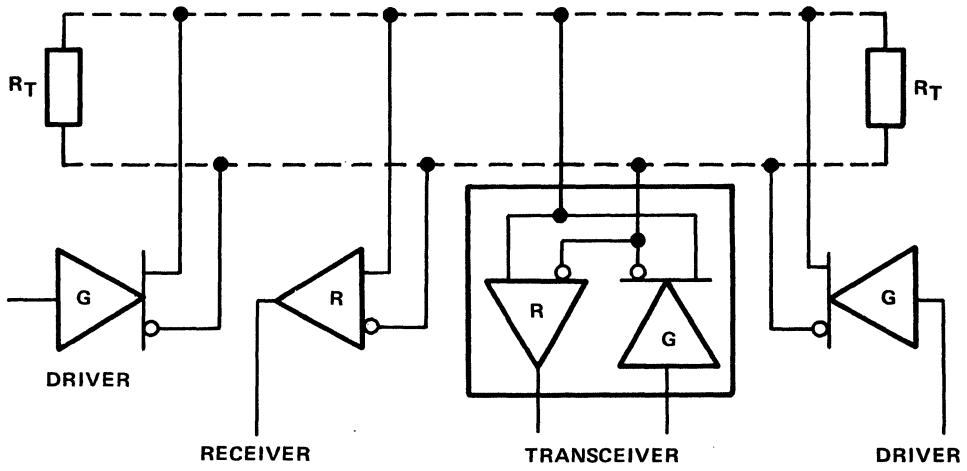


Figure 9-84. Multipoint Balanced Digital Interface

balanced data transmission lines in distributing data to several system components and peripherals over relatively long lines brought about the need for multiple driver/receiver combinations on a single twisted pair line.

EIA RS-485 takes into account RS-422-A requirements for balanced-line transmission plus additional features allowing for multiple drivers and receivers. Figure 9-84 illustrates an application similar to that of Figure 9-78, but with multiple drivers and receivers.

Standard RS-485 differs from the RS-422-A standard primarily in the features that allow reliable multipoint communications. For the drivers these features are:

- One driver can drive as many as 32 unit loads and a total line termination resistance of 60 Ω or more (one unit load is typically one passive driver and one receiver).
- The driver output, off-state, leakage current shall be 100 μA or less with any line voltage from −7 V to 7 V.
- The driver shall be capable of providing a differential output voltage of 1.5 V to 5 V with common-mode line voltages from −7 V to 12 V.
- Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time). That is, no driver damage shall occur when its outputs are connected to a voltage source of −7 V to 12 V whether its output state is a binary 1, binary 0 or passive.

For receivers these features are:

- High receiver input resistance, 12 kΩ minimum.
- A receiver input common-mode range of −7 V to 12 V.
- Differential input sensitivity of ±200 mV over a common-mode range of −7 V to 12 V.

Unit Load Concept

The maximum number of drivers and receivers that may be placed on a single communication bus depends on their loading characteristics relative to the definition of a "UNIT LOAD" (U.L.). RS-485 recommends a maximum of 32 unit loads (U.L.) per line.

One U.L. is defined (at worst case) as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V (for a more detailed definition refer to the EIA Standard RS-485, page 4). The loads may consist of drivers and/or receivers but do not include the line termination resistors which may present an additional load as low as 60 Ω total.

Example: Early production SN75172 drivers and SN75173 receivers.

- Driver output leakage current in the off state with 12 V output voltage is 0.1 mA max.
- Receiver input current at a V_{in} of 12 V is 1 mA max.
- The driver represents 0.1 mA/1.0 mA or 0.1 U.L.
- The receiver represents 1.0 mA/1.0 mA or 1 U.L.
- As a pair they represent 1.1 mA/1.0 mA or 1.1 U.L. Therefore, 32/1.1 or 29 pairs would represent the maximum recommended 32 unit loads.

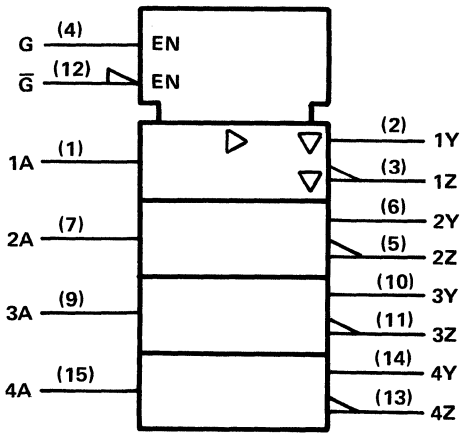
Example: 1984 production SN75172B drivers and SN75173A receivers.

- Driver I_O off at 12 V is 0.1 mA max
- Receiver I_{IN} at 12 V is 0.6 mA max

Although there were no changes in the driver loading, the receiver now represents only 0.6 U.L. A driver-receiver pair represents 0.7 U.L. and therefore 32 U.L./0.7 U.L. per pair or 45 of these driver-receiver stations could be handled on one twisted pair data transmission line.

DRIVERS AND RECEIVERS

Driver types SN75172B and SN75174B and receivers SN75173A and SN75175A were specifically designed for RS-422-A and RS-485 applications. These parts were designed to be direct plug-in replacements for popular RS-422-A circuits (see Figures 9-85, -86, -87 and -88).



QUAD DIFFERENTIAL LINE DRIVER

AM26LS31 MEETS EIA STANDARD RS-422-A AND FEDERAL STANDARD 1020

SN75172B MEETS EIA STANDARDS RS-422-A AND RS-485. ALSO MEETS CCITT RECOMMENDATIONS V.11 AND X.27

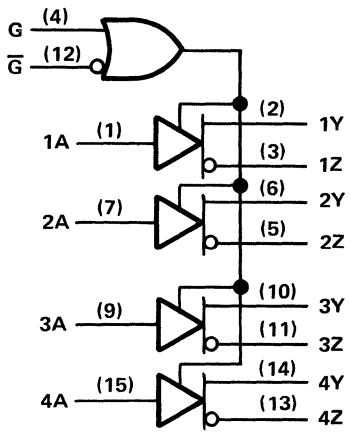


Figure 9-85. Quad Differential Line Driver AM26LS31 and SN75172B

Converting from an RS-422-A system is easy if the AM26LS31 or MC3487 drivers and AM26LS32 or MC3486 receivers were previously being used. Conversion from a dedicated station-to-station line to a party line does not require rewiring of printed circuit boards, only the substitution of RS-485 circuits in the boards.

Driver Details

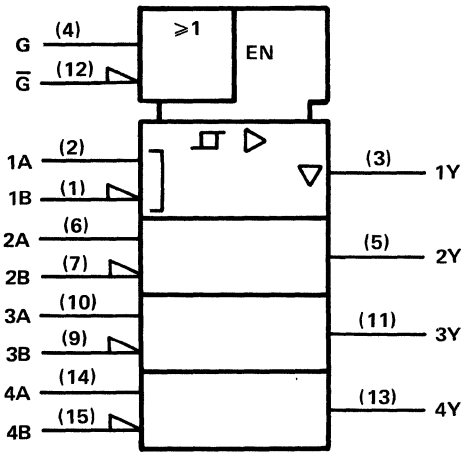
SN75172B series driver inputs are TTL compatible as previously mentioned. Figure 9-89 shows some additional features.

Using a pnp input transistor provides a relatively high input impedance and allows the input to be both TTL and low-level CMOS compatible. The maximum input high-level current of 20 μA and maximum low-level current of -360 μA are well within the capability of low-power Schottky or low-power CMOS gates. Input diodes will clamp any negative voltages at or below -1.5 V.

The basic driver output circuit configuration in Figure 9-90 is a totem-pole with both source and sink current limiting. High-speed Schottky output pull-up and pull-down transistors provide up to 60 mA of output drive current.

The pull-up output transistor receives its current from the V_{CC} rail through a resistor that is connected across the base-emitter junction of a current sensing transistor. Excessive high-level output current will turn on the current sensing transistor providing shut down drive to an output predrive transistor (not shown).

The pull-down transistor has a different type of current sensing. Its base is connected to the base of a current-sensing transistor. As the output sink transistor current reaches operating limits its V_{BE} rises to a level high enough to turn on the current-sense transistor. The current-sense transistor draws (by bypassing) base drive current from the output thus limiting the output sink current.



QUAD DIFFERENTIAL LINE RECEIVER

AM26LS32A MEETS EIA STANDARDS RS-422-A AND RS-423-A

SN75173A MEETS EIA STANDARDS RS-422-A, RS-423-A AND RS-485. ALSO MEETS CCITT RECOMMENDATIONS V.10, V.11, X.26 AND X.27

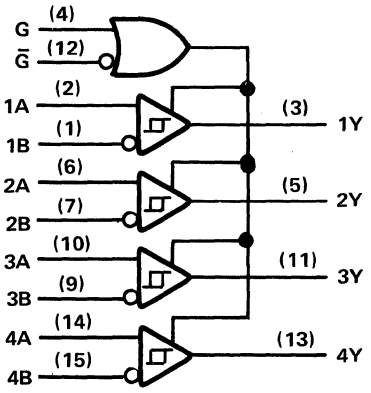
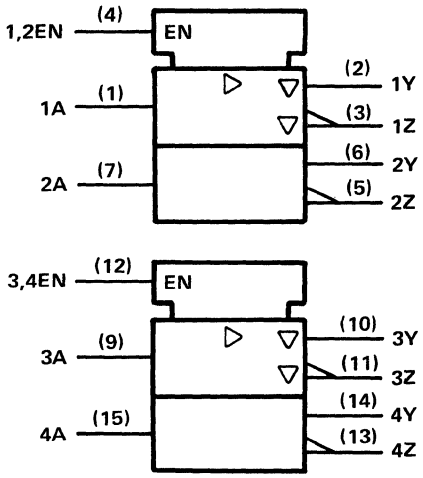


Figure 9-86. Quad Differential Line Receiver AM26LS32A and SN75173A



QUAD DIFFERENTIAL LINE DRIVER

MC3487 MEETS EIA STANDARDS RS-422-A AND FEDERAL STANDARD 1020.

SN75174B MEETS EIA STANDARDS RS-422-A AND RS-485. ALSO MEETS CCITT RECOMMENDATIONS V.11 AND X.27

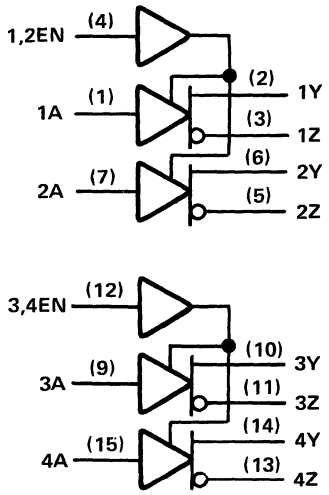


Figure 9-87. Quad Differential Line Driver MC3487 and SN75174B

The differential outputs will typically provide 3.5 V V_{OH} and 1.1 V V_{OL} levels for a 2.6 V differential drive (V_{OD}). If operating into a typical 120 Ω line-to-line termination, Figure 9-91, the resulting drive current is about 22 mA. If termination is to ground, resistor values are half of the line impedance, Figure 9-92. Output high-level currents would typically be: $V_{OH}/R_L/2$ or 3.5 V/62 Ω = 56 mA.

Driver Speed Characteristics

The SN75172B and SN75174B drivers exhibit a differential output transition time of 75 ns maximum. This particular parameter is key to the maximum speed at which the driver may operate in accordance with EIA RS-485 specifications.

EIA RS-485 defines the device transition time, "t_r", relative to one unit interval, "t_b". See Figure 9-93.

If transition time for the device is known then the maximum operating data rate for RS-485 conditions can be calculated as follows:

$$t_r = 0.3\ t_b \text{ and } t_b = \frac{t_r}{0.3}$$

The data rate is

$$f_b = \frac{1}{t_b} \quad \text{or} \quad f_b = \frac{0.3}{t_r}$$

For example, the SN75172B or 174B drivers have a specified maximum t_r of 75 ns. At the worst-case level the maximum data rate would be:

$$f_b = \frac{0.3}{t_r} = \frac{0.3}{75 \times 10^{-9}}$$

$$f_b = 4 \text{ Mbps}$$

QUAD DIFFERENTIAL LINE DRIVER

MC3486 MEETS EIA STANDARDS RS-422-A, RS-423-A AND FEDERAL STANDARDS 1020 AND 1030

SN75175A MEETS EIA STANDARDS RS-422-A RS-423-A AND RS-485. ALSO MEETS CCITT RECOMMENDATIONS V.10, V.11, X.26 AND X.27

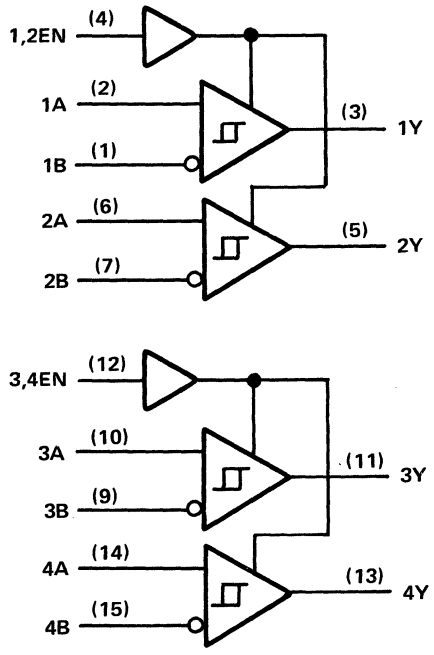


Figure 9-88. Quad Differential Line Receiver MC3486 and SN75175A

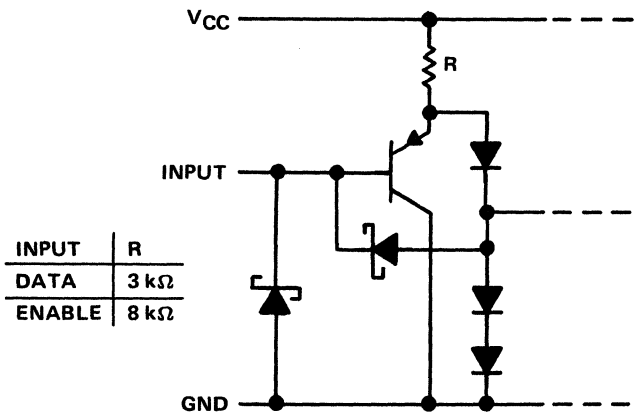


Figure 9-89. Equivalent Driver Input Circuit

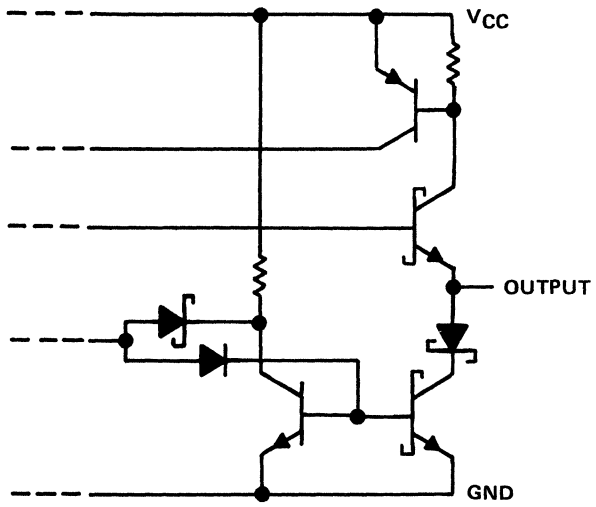


Figure 9-90. Equivalent Each Driver Output

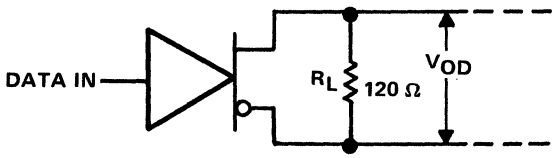


Figure 9-91. Line-to-Line Termination

A typical t_r value for the SN75172B and SN75174B is 50 ns and would result in a max f_b of $0.3/50 \times 10^{-9}$ or 6 Mbps.

Receiver Details

The SN75173A or SN75175A receiver data input circuit is shown in Figure 9-94.

Series input resistance and active impedances provide a typical input resistance of 20 kΩ. An input common-mode voltage range of 12 V to −12 V and 50 mV of input threshold hysteresis provide excellent noise immunity. Differential input threshold voltage is ±200 mV or less allowing the reception of signals that have been attenuated over long line lengths.

The receiver output has typical TTL output characteristics. The equivalent output circuit of the SN75173A/175A is shown in Figure 9-95.

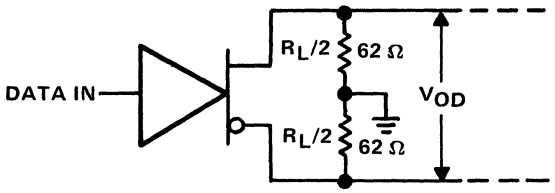
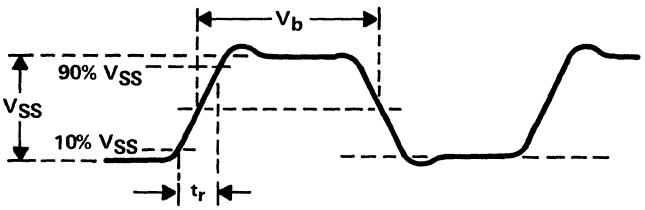


Figure 9-92. Line-to-Ground Termination



V_{SS} = difference in steady-state voltage levels
t_b = time duration of one unit interval, measured between successive 0.5 V_{SS} levels.
t_r = transitional time from 10% of V_{SS} to 90% of V_{SS}
t_r is also defined as being less than, or equal to, 0.3 t_b

Figure 9-93. Driver Output Waveform

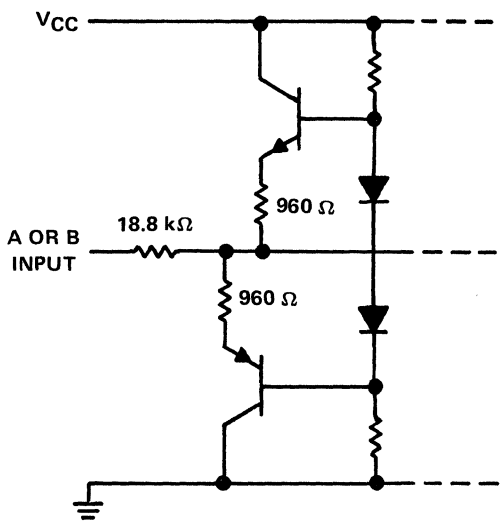


Figure 9-94. Equivalent Receiver A or B Input

In addition, the output has a high impedance when disabled or powered down. Output leakage current, when disabled, is less than 20 μA. High level output current is limited to 85 mA maximum when the output is shorted to ground.

The SN75173A and SN75175A are built with low-power Schottky technology resulting in propagation delay times of only about 20 ns (see Figure 9-96).

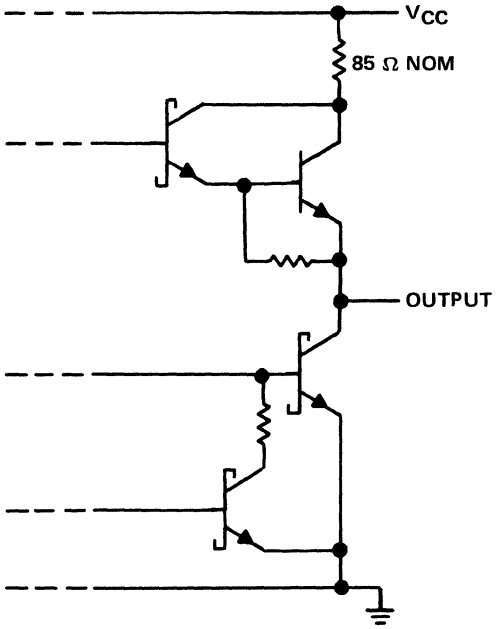


Figure 9-95. Equivalent Receiver Output

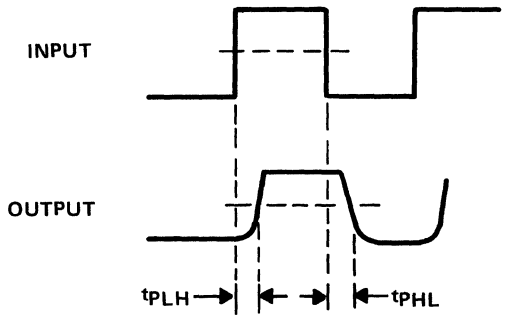


Figure 9-96. Receiver Propagation Delays

TRANSCEIVERS

Some EIA RS-485 type circuit applications require only one driver and one receiver at each location. Point-of-sale terminals is an example. In such applications a transceiver would be desirable. The SN75176B, SN75177B, SN75178B and SN75179B are types of devices used for this purpose. See Figures 9-97, -98, -99 and -100.

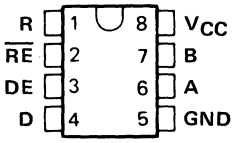
SN75176B, SN75177B, SN75178B, and SN75179B Transceivers Features

- Meet EIA Standard RS-485
- Meet EIA Standard RS-422-A, and CCITT V.11 and X.27
- 3-State Drivers (Except SN75179B)
- Wide Positive and Negative Bus Voltage Ranges
- Thermal Shutdown Protection
- Positive and Negative Driver Current Limiting
- Driver Output Current Capability ±60 mA
- Receiver Input Resistance . . . 20 kΩ Minimum
- Receiver Input Sensitivity ±200 mV
- Receiver Input Hysteresis 50 mV Typical
- Operate from Single 5 V Supply

In addition to the features listed, the SN75176B also provides individual driver and receiver enable pins and can be used as a basic transceiver for EIA RS-485 or EIA RS-422-A applications.

Basic Transceiver Application

Figure 9-101 shows transceivers distributed along a transmission line. Each station may transmit or receive data



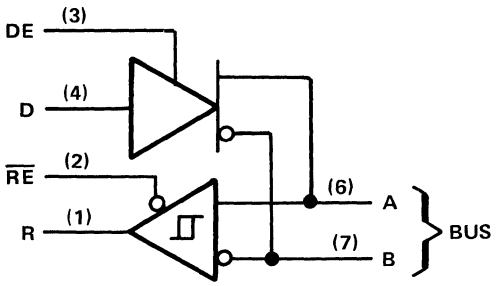
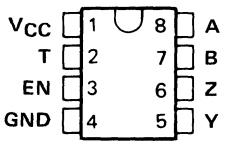


Figure 9-97. SN75176B



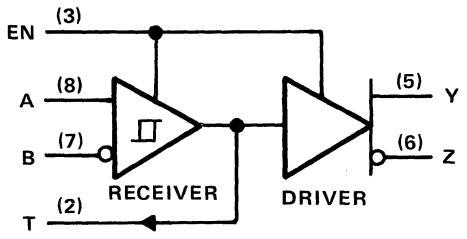


Figure 9-98. SN75177B

which is typical of point-of-sale terminals communicating with a central computer. The central computer handles the protocol conversion which is generally over a control line that is separate from the data bus.

In multipoint communication the transmission line is taken directly to each station, eliminating the use of long stubs or feeder lines. This is necessary to prevent adverse loading

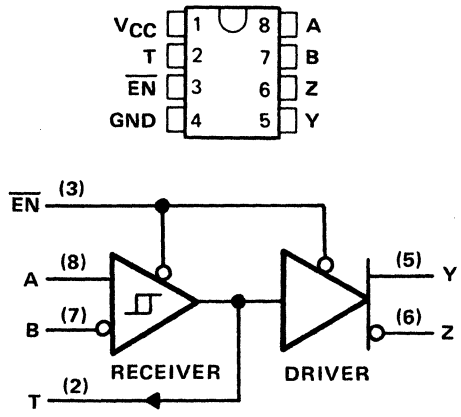


Figure 9-99. SN75178B

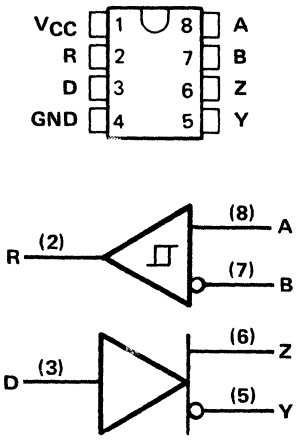


Figure 9-100. SN75179B

on the bus. Use of 3-inch or longer stubs may present a load to the main bus which will reduce signal amplitudes and can result in reflections and unwanted ringing.

The SN75176B represents only 0.7 unit loads and as many as 45 pairs could be connected to a single data transmission line.

Long-Line Application

In long-line applications of several thousand feet, signal attenuation and noise pickup may result in signal deterioration and possible data errors at the receiver. The SN75177B and SN75178B (Figures 9-98, 9-99) which require only one control line, may be used to provide bidirectional signal boosting. Figure 9-102 is an example of such a system. SN75177B and SN75178B boosters allow bidirectional transmission of signals between the CPU and a remotely connected CRT and keyboard.

SN75179B Application

Another device available in the SN75172 series is the SN75179B. The SN75179B provides an independent driver and receiver in the small 8-pin package. This device would be used in RS-422-A or RS-485 type applications (Figure 9-103) where separate transmit and receive lines are required by the terminal or station.

IEEE 488-1978 TRANSMISSION SYSTEMS

THE IEEE-488 STANDARD

The information in this section is intended as an overview of the IEEE-488 Interface System Standard. Brief definitions of some of the interface functions are presented to help you understand the basics of the system.

General Information

The IEEE Std 488-1978 defines a standard digital interface for programmable instrumentation dealing with systems that use a byte-serial bit-parallel method of transferring data between various instruments and/or system components. This interface system is optimized for communication over relatively short data lines and allows for party-line bus operation. The IEEE Std 488-1978 is often referred to by other names or abbreviations. Some examples are: "GPIB" (general purpose interface bus), "HPIB" (Hewlett-Packard interface bus), "ASCII bus" (American standard code for information interchange bus) and sometimes simply the "488 interface". Because the 488 interface system is easy to use, this standard has been widely accepted. As a result, the system designer may select various test instruments and control devices, from different manufacturers, that are 488 interface bus compatible and

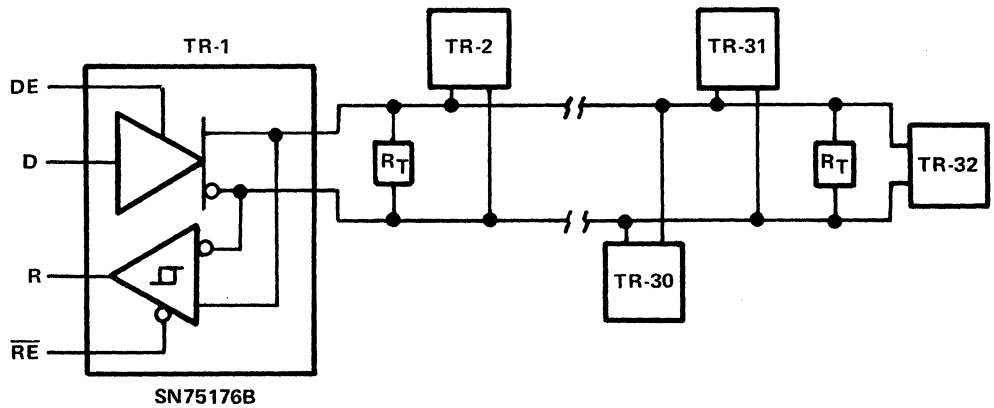


Figure 9-101. SN75176B Transceivers on Multi-Station Bus

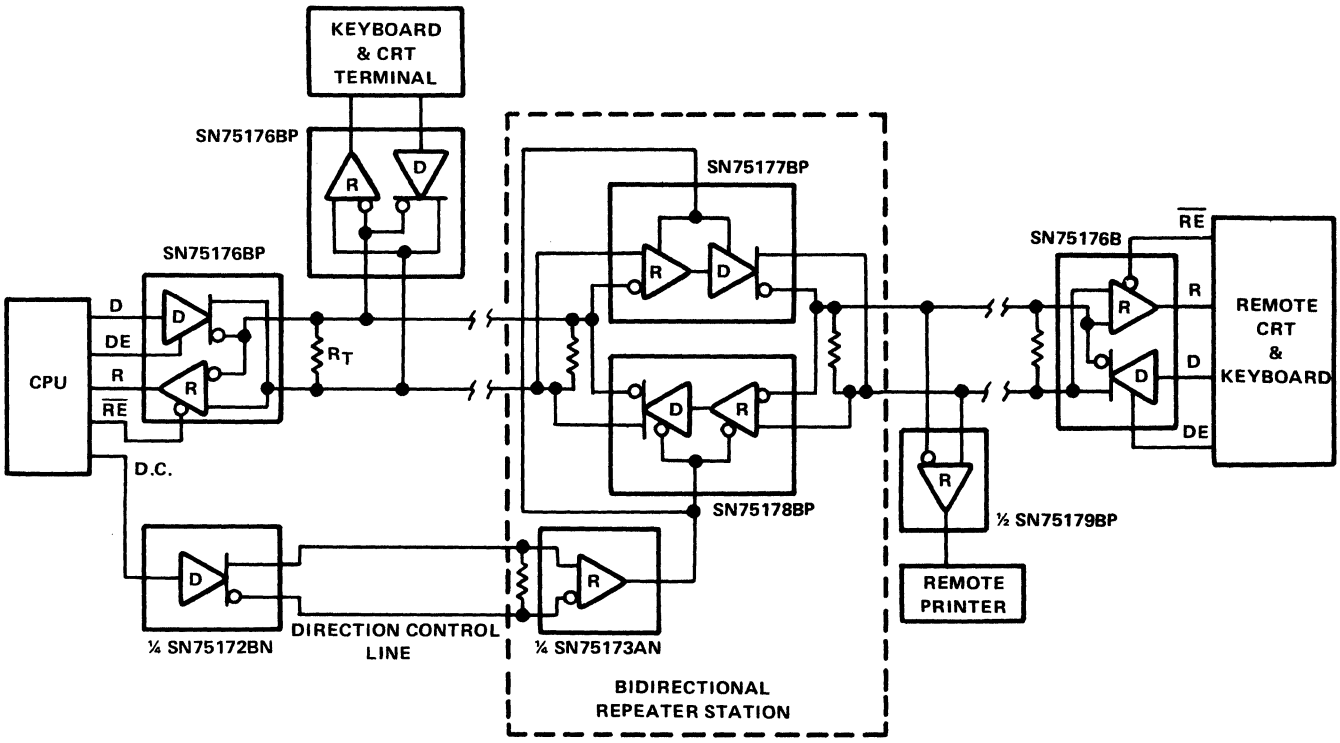


Figure 9-102. SN75177B and SN75178B Allow Bidirectional Long Line Communication

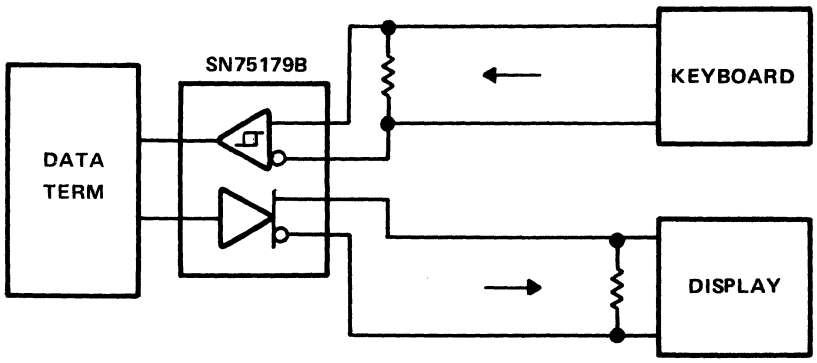


Figure 9-103. SN75179B Independent Driver and Receiver

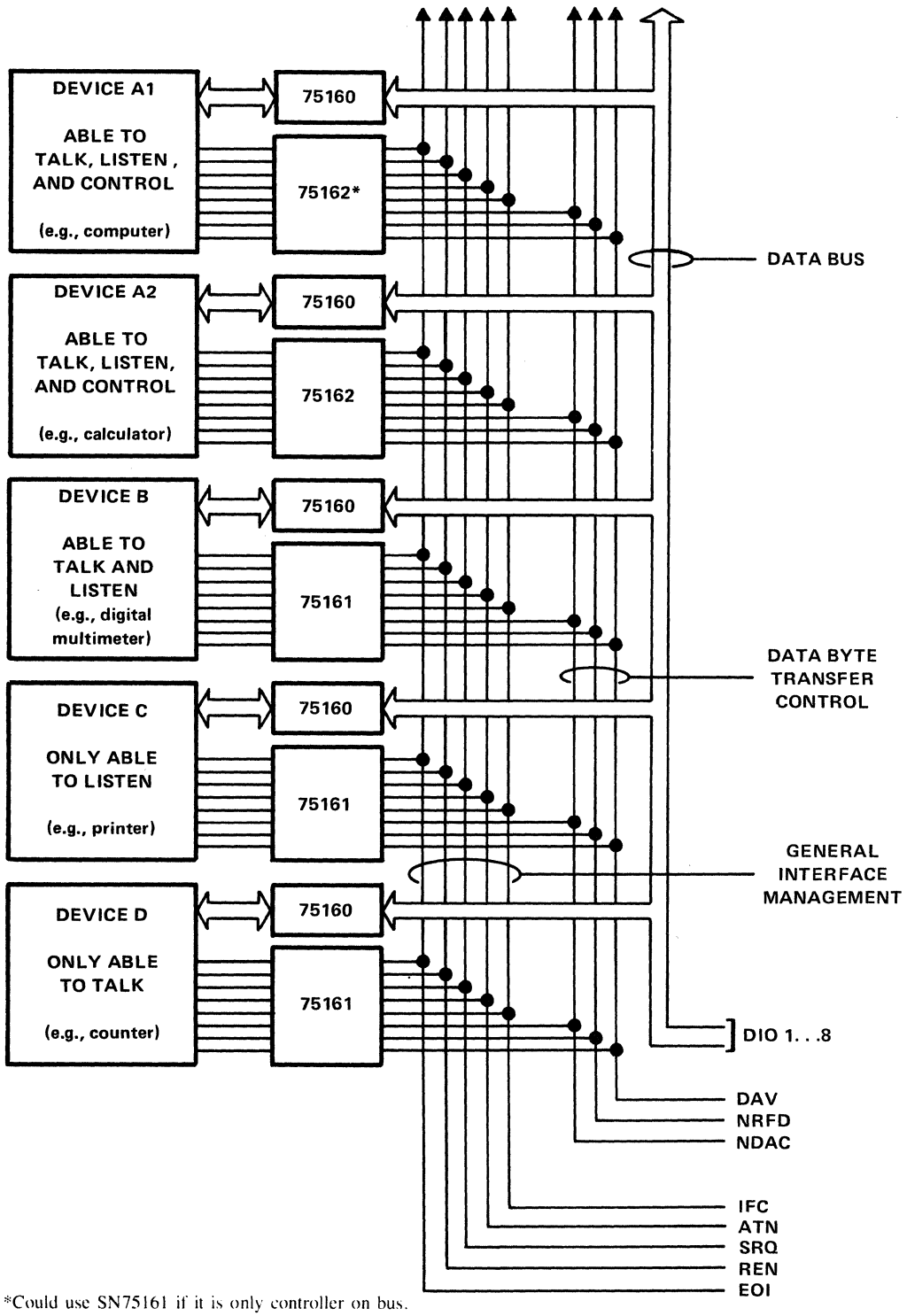
know that they can work together. The situation was quite different in the mid 1960s when the Hewlett Packard Company began working on an interface standard for its future instruments. This original effort evolved into the IEEE Std 488-1975 which was revised to become the IEEE Std 488-1978 as we know it today.

The IEEE-488 standard defines an instrument interface system that allows up to 15 instruments within a localized area to communicate with each other over a common bus. Each device has a unique address, read from external switches at power-on, to which it responds. Information is transmitted in byte-serial, bit-parallel format and may consist of either data or interface control instructions.

Data may be sent by any one device (the Talker) and received by one or more of the other devices (Listeners). Instructions such as select range, select function, or measurement data for processing or printing may be sent in this way. One of the devices on the bus, designated the Controller, may send interface control messages. It can assign an instrument to the bus as a listener or talker by sending its unique talk or listen address. The controller can also set the instrument for remote or local control.

The bus itself consists of 24 lines: eight lines carry data, eight are control lines, and eight are system ground lines. The block diagram in Figure 9-104 illustrates a basic IEEE-488 interface. The 16 signal lines shown allow for eight data lines, three hand shaking lines and five control lines.

1. The Data Lines: The eight data input/output lines carry the basic data, or information, to and from the instruments.



*Could use SN75161 if it is only controller on bus.

Figure 9-104. Typical IEEE-488 Interface System

2. The Handshaking Lines: The three data-transfer control lines are identified as "Data Valid" (DAV), "Not Ready For Data" (NRFD), and "Data Not Accepted" (NDAC).
3. The Management Lines: The five general management lines are identified as "Interface Clear" (IFC), "Attention" (ATN), "Service Request" (SRQ), "Remote Enable" (REN), and "End or Identify" (EOI).

Connectors

The pin connection assignments, physical dimensions, and mechanical mounting of the connector are given in the mechanical specifications of the IEEE-488 standard. Figure 9-105 illustrates the 24 pin interface connector and identifies each pin assignment. This type of connector is available from sources of Microribbon (Amphenol or Cinch series 57) or Champ (Amp) type connectors.

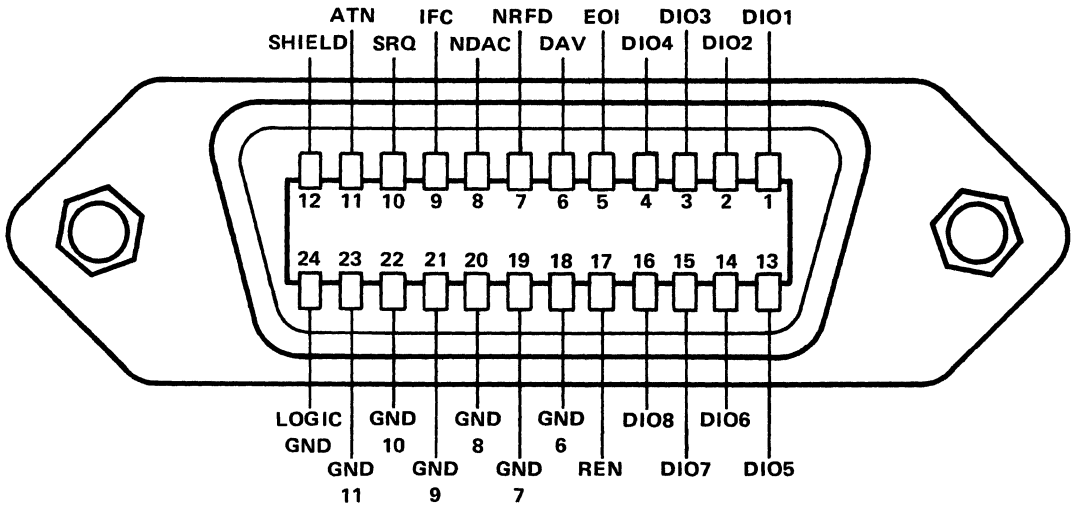


Figure 9-105. Interface Connector

The IEEE Std 488-1978 is very similar to its international counterpart, IEC publication 625-1. The IEC document specifies a connector system identical to that used with the EIA RS-232-C data communications interface. It should be noted, therefore, that component damage due to incompatible voltage levels is possible if data communication (EIA RS-232-C) and instrument (IEEE-488 or IEC 625-1) interfaces are interconnected. If interconnection between IEEE-488 and IEC 625-1 interfaces is required, mechanical differences in the connectors may be accommodated by use of special adapters.

Cable

The cable consists of at least 24 conductors: 16 signal lines and 8 logic ground returns. All lines are contained in a braided shield of 36 AWG wire or equivalent, providing 85% coverage. Line capacitance at 1 kHz on any signal line, with all other lines (signal, ground, and shield) grounded shall not exceed 150 pF per meter. Each signal line DAV, NRFD, NDAC, IFC, ATN, EOI, REN, and SRQ shall be twisted with a ground line or isolated in some other manner so as to minimize cross talk. A cable meeting these requirements is available from several major cable manufacturers. The total cable length in a system is limited to 2 meters times the number of instruments and shall not exceed a maximum of 20 meters without the aid of a booster or bus extender. The instruments may be unevenly spaced along the line but caution should be taken if any individual cable length exceeds 4 meters. Cables may be connected in a linear (daisy-chain) configuration, a star configuration, or combinations of these.

For best operation, the instruments should be at the same frame potential. Differences in frame potentials may result in excessive ground currents or possible system failure.

The maximum resistance of the cable conductors, per meter of cable length, is:

1. Each signal line (data or control) — 0.14 Ω.
2. Individual signal ground return — 0.14 Ω.
3. Common logic ground return — 0.085 Ω.
4. Overall shield — 0.0085 Ω.

Logic Convention

Many data transmission systems use positive logic on the bus lines. However, the IEEE-488 bus uses negative logic. That is, a voltage greater than 2 V on the signal line is considered a logic zero or false, while a voltage of 0.8 V is referred to as a logic one or true.

Three of the signal lines SRQ, NRFD, and NDAC must be driven from open-collector drivers. If any one of the line drivers is on, that line will be in a logic low or true condition. This is referred to as a "wired-OR" configuration and is necessary for these handshaking lines. Other bus lines may be driven by either three-state or open-collector drivers depending on the system application.

Bus lines are connected to three different types of devices. They are:

1. The Talker, which is any device that, when addressed, can transmit device dependent data over the bus.
2. The Listener, which is any device that, when addressed, can receive device dependent data from the bus.
3. The Controller, which can transmit data, receive data, and issue commands. The Controller manages the bus by designating listeners and talkers and by programming the other devices.

Functions

Instrument interface functions are covered in detail in the IEEE-488 standard. Each function may also have some options. Some of the basic functions are defined as follows:

Source Handshake (SH) Interface Function

The SH function provides a device the capability to guarantee the transfer of multiline messages. Asynchronous transfer of each multiline message is accomplished with an interlocked handshake sequence between the SH function and one or more of the AH (acceptor handshake) functions. The SH function controls the initiation and termination of a multiline message byte. To effect each message byte transfer,

the SH function uses the DAV (data valid), RFD (ready for data), and DAC (data accepted) messages.

Acceptor Handshake (AH) Interface Function

The AH function provides a device the capability to guarantee proper reception of remote multiline messages. An interlocked handshake sequence between an SH function and one or more AH functions guarantees asynchronous transfer of each message byte. An AH function may delay either the initiation of, or termination of, a multiline message transfer until prepared to continue. The AH function uses the DAV, RFD, and DAC messages to effect each message byte transfer.

Talker (T) Interface Function

The T function provides a device the capability to send device dependent data (including status data during a serial poll sequence) over the interface to other devices when it is addressed. The normal T function uses a 1 byte address. The T with address extension is called the Extended Talker Function (TE) and uses a 2 byte address. Only one of the functions, T or TE, needs to be implemented in a specific device.

Listener (L) Interface Function

The L interface function provides a device the capability to receive device dependent data (including status) from other devices when addressed to listen. The normal L function uses a 1 byte address while the extended listener (LE), with address extension, uses a 2 byte address.

Service Request (SR) Interface Function

The SR interface function provides a device the capability to request service asynchronously from the interface controller. The SR interface function also synchronizes the content of the RQS (request service) message of the status byte present during a serial poll. Thus the SRQ (service request) message can be removed from the interface once the RQS message is received.

Remote Local (RL) Interface Function

The RL interface function provides a device the capability to select between the two sources of input information by indicating to the device which one is to be used, local (from the front panel) or remote (from the interface).

Parallel Poll (PP) Interface Function

The PP interface function provides a device the capability to present a PPR (parallel poll reply) message to the controller without being addressed to talk. A parallel poll enables the transfer of status data from multiple devices concurrently.

Device Clear (DC) Interface Function

The DC interface function provides a device the capability to be cleared (initialized) either individually or with a group of devices.The group may be either a subset or all addressed devices in one system.

Device Trigger (DT) Interface Function

The DT interface function provides a device the capability to have its basic operation started either individually or as a part of a group of devices. The group may be either a subset or all addressed devices in one system.

Controller (C) Interface Function

The C interface function provides a device the capability to send device addresses, universal commands and addressed commands to other devices over the interface. It also provides the capability to conduct parallel polls to determine which devices require service. A device with a C function can exercise its capabilities only when it is sending the ATN message over the interface.

If more than one device on the interface has a C function, then all but one of them shall be in the CIDS (controller idle state) at any given time. The device containing the C function which is not in the CIDS is called the controller-in-charge. IEEE-488 protocol allows devices with a C function to take turns as the controller-in-charge of the interface.

Only one of the devices with a C function that is connected to an interface can exist in the SACS (system control active state). It remains in this state throughout operation of the interface and has the capability to send the IFC and REN messages over the interface at any time whether or not it is the controller-in-charge. This device is called the system controller.

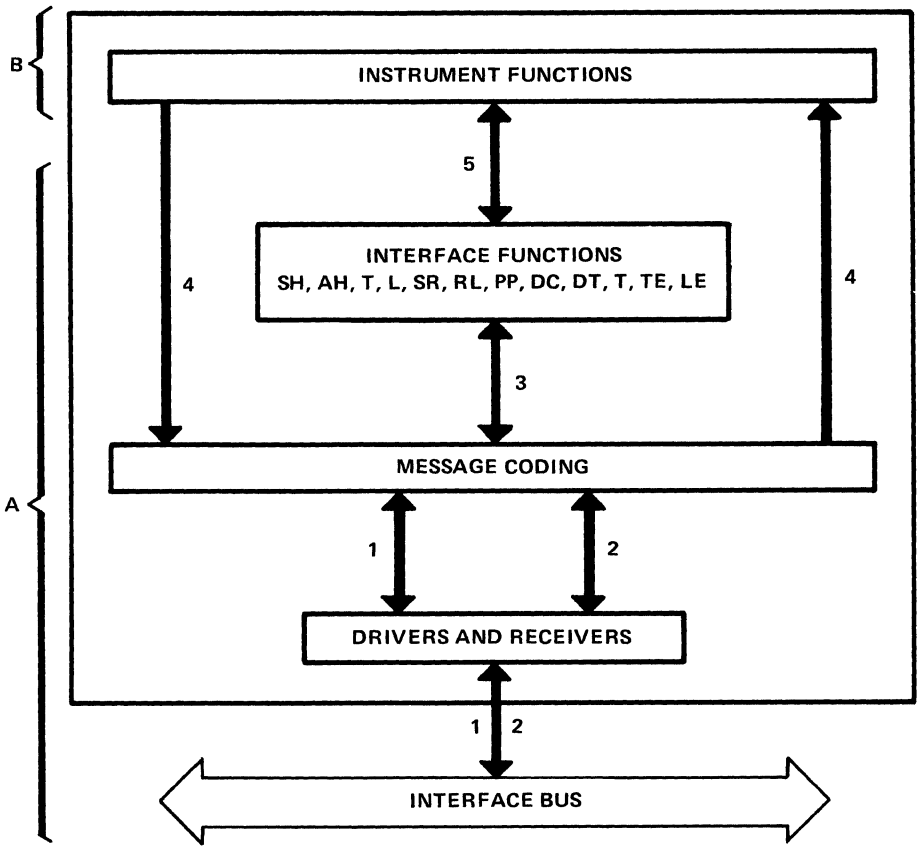
Messages or Commands

All communication between an interface function and its environment is accomplished through messages sent or received. Figure 9-106 illustrates the partitioning of an instrument or apparatus and shows the message flow between device functions and interface functions. Details on message conventions are given in the IEEE Std-488 and will not be covered in this text.

Single-Line Messages

Five interface signal lines are used to manage an orderly flow of information across the interface. Each line carries a specific message and is referred to as a single-line message (or command). These lines are the general management lines and are identified as follows:

1. ATN (attention) is used by a controller to specify how data on the Data I/O signal lines are to be interpreted and which devices must respond to the data. The ATN command causes all devices to cease their activity and listen to the controller.ATN commands are issued only by the controller.
2. IFC (interface clear) is used by a controller to place the entire interface system in a known state. This clears the interface bus and idles all the devices. The IFC command causes all data



NOTES: A. Capability defined by IEEE Standard 488
B. Capability defined by designer
1. Interface bus data lines
2. Interface bus handshake and management lines
3. Remote interface messages to and from interface functions
4. Device dependent messages to and from device functions
5. Local messages between device functions and interface functions

Figure 9-106. Functional Partitioning Within an Instrument or Apparatus

transmission and all polls, to stop, and unaddresses all devices.

3. SRQ (service request) This command is given by a device, not a controller, to indicate the need for service and request interruption of current activity. The controller will then do a serial poll to determine which device has requested service and switch to a service routine.
4. REN (remote enable) is used by the controller to select device programming data from either the front panel (local) or the interface bus (remote).
5. EOI (end or identify) is used by a talker to indicate the end of a message string or byte sequence. EOI is used by a controller, in conjunction with ATN, to perform a polling sequence.

Multiline Messages

Multiline messages are interpreted as device dependent or interface messages, based on the state of ATN. Four classes of interface messages that may be accepted when the ATN command is true are:

1. The Universal commands are obeyed by all devices whether they have been told to listen or not.
2. Addressed commands are obeyed by those devices addressed to listen.
3. Unaddress commands remove the talker and all listeners from the bus.
4. Address commands designate the talkers and listeners.

BUS INTERFACE DEVICES

Interfacing between the instrument (or apparatus) interface functions and the system bus is accomplished with line driver and receiver circuits generally configured as transceivers. Since IEEE-488 systems consist of eight data lines and eight control lines, interfacing to the bus is often accomplished with octal transceivers. Details concerning the characteristics of these devices are covered in the following section on Electrical Specifications.

Electrical Specifications

Electrical specifications for driver output and receiver input voltage levels are the same as TTL voltage levels. However, a negative logic convention is used and is defined as follows:

LOGIC STATE	VOLTAGE LEVEL
ZERO	>2.0 V (high state)
ONE	<0.8 V (low state)

For this discussion, current flow into a node carries a positive sign and current flow out of a node carries a negative sign.

Driver Requirements

Drivers with open-collector outputs shall be used to drive the SRQ, NRFD, and NDAC signal lines. Drivers with open-collector or three-state outputs may be used to drive data I/O (lines 1—8), DAV, IFC, ATN, REN, and EOI signal lines with the following exception: Data I/O (lines 1—8) shall be driven by open-collector output drivers for parallel polling applications. Three-state driver outputs are used for systems where maximum operating speeds are required. A three-state driver output is also recommended to drive the ATN signal line if the controller is intended to be used in a system where other devices are implemented with three-state drivers on the DIO, DAV, and EOI signal lines.

Driver Specifications

Driver outputs shall meet the following specifications:

Low state output voltage (three-state or open-collector output) <0.5 V at 48 mA sink current.

The driver shall be capable of sinking 48 mA continuously.

High state output voltage (three-state) >2.4 V at −5.2 mA.

High state output voltage (open-collector) dependent on resistive load termination.

Receiver Specifications

Required input signal levels, necessary to provide nominal noise margins, shall be as follows:

Low state input voltage <0.8 V

High state input voltage >2.0 V

Preferred input signal characteristics, necessary to provide added noise margin and improved reliability, are as follows:

Receiver input hysteresis, V_t pos − V_t neg, shall be >0.4 V

Low state negative going threshold voltage V_t neg >0.8 V

High state positive going threshold voltage V_t <2.0 V

Composite Load Requirements

The total dc load characteristics primarily result from resistive line terminations and receiver input characteristics. Negative voltage clamp circuits and driver high-impedance output state characteristics result in some slight additional loading.

Figure 9-107 illustrates a typical circuit configuration whose specifications are as follows:

R_{L1} (line to V_{CC}) is 3 kΩ ±5%

R_{L2} (line to ground) is 6.2 kΩ ±5%

Driver output leakage current:

open-collector driver is 0.25 mA maximum

three-state driver is ±40 μA maximum at V_O = 2.4 V

Receiver input current:

−1.6 mA maximum at V_O = 0.4 V

Receiver input leakage current:

40 μA maximum at V_O = 2.4 V

1.0 mA maximum at V_O = 5.25 V

V_{CC}: 5.0 V ±5%

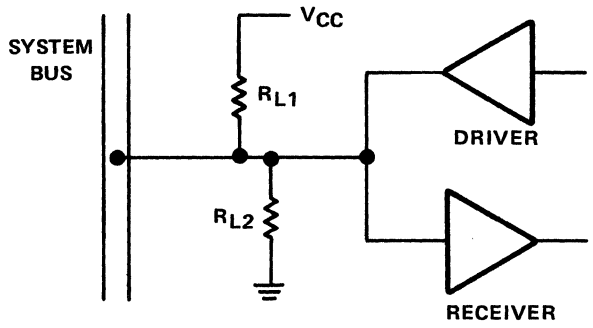


Figure 9-107. Typical Signal Line I/O Circuit

Device DC Load Line Boundaries

The load conditions of a device assume that the driver, receiver and termination network are internal to the device and that the driver is in its high-impedance state. The signal line interface to the device shall have a dc load characteristic that falls within the unshaded area illustrated in Figure 9-108. The load line boundary limits are defined as follows:

1. If I <0 mA, V is <3.7 V.
2. If I >0 mA, V is >2.5 V.
3. If I > −12.0 mA, V is > −1.5 V.
4. If V <0.4 V, I is < −1.3 mA.
5. If V >0.4 V, I is > −3.2 mA.
6. If V <5.5 V, I is <2.5 mA.
7. If V >5.0 V, I is >0.7 mA

Device AC Load Line Limit

The small-signal load impedance shall be <2.0 kΩ at 1 MHz.

Device Capacitive Load Limit

Each device shall present an internal capacitive load of <100 pF to each of its signal lines.

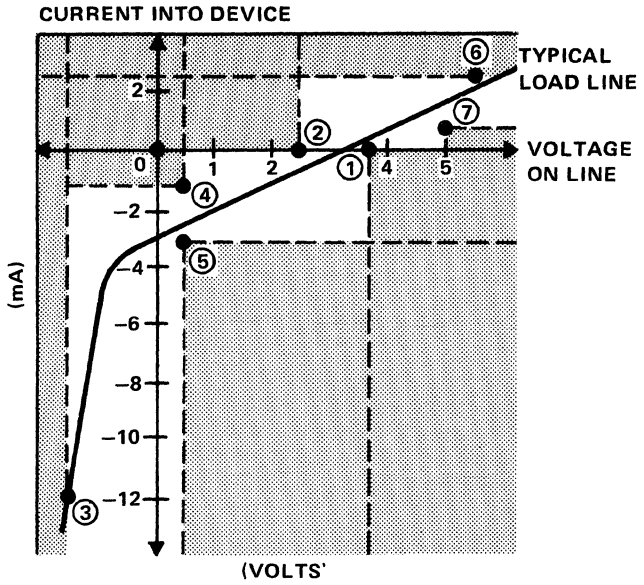


Figure 9-108. DC Load Line Permissible Operating Area

Timing Values

Definite relationships between critical signal inputs and outputs are required for successful interconnection of devices. Consideration of propagation delays, transition times and system response times is necessary for reliable operation.

Table 9-13 lists several of the required limits on these timing values. The longer time values shown allow for the inherently long propagation delays of the transmission lines as well as device circuit delays. The IEEE-488 Standard has a detailed discussion of these timing requirements.

Table 9-13. Time Values

FUNCTION	DESCRIPTION	VALUE
SH	Settling time for multiline messages	>2 μs
SH,AH,T,L,LE,TE	Response to ATN	<200 ns
AH	Interface message accept time	>0
T,TE,L,LE,C,RL	Response to IFC or REN false	<100 μs
PP	Response to ATN with EOI	<200 ns
C	Parallel poll execution time	>2 μs
C	Controller delay to allow current talker to see ATN message	>500 ns
C	Length of IFC or REN false	>100 μs
C	Delay for EOI	>1.5 μs

Data Rates

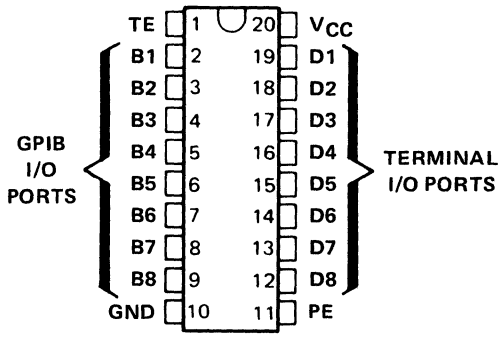
Open-collector drivers will operate at a maximum of 250,000 bytes per second. Three-state drivers with equivalent standard loads will operate at a maximum of 500,000 bytes per second. With special precautions (three-state drivers, short signal lines and minimum capacitive loading) data rates up to 1 megabyte per second are possible.

INTERFACING TO THE IEEE STANDARD 488 BUS

The General-Purpose Interface Bus (GPIB) defined by the IEEE Standard 488 has received wide acceptance, and many commercially available instruments now use it. This allows a user to purchase instruments from several different manufacturers and connect them together using off-the-shelf cable. The TI SN75160 family of bus transceivers is designed to provide the interface between the bus and the bus controller of the instrument. These transceivers may be used with the TMS9914A or any other 488 bus controller. The SN75160 family of transceivers provides the simplest method of interfacing because each part is tailored to either the 8-line data bus or the 8-line control bus, and they require no extra logic or complicated board layout.

SN75160A Octal GPIB Transceiver

The SN75160A is an 8-channel, bidirectional, GPIB transceiver which is designed to meet the IEEE Standard 488-1978. This transceiver features driver outputs that can be operated in either the open-collector or three-state mode. See Figure 9-109 for the pinout and function tables.



FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z‡
X	L	X	Z‡

EACH RECEIVER

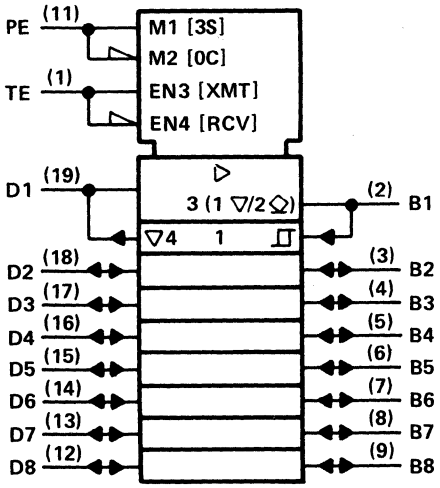
INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

‡ This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

Figure 9-109. SN75160A Pinout and Function Tables

If the Talk Enable (TE) input is high and the Pull-up Enable (PE) is low, the output ports have an open-collector characteristic, and when the PE input is high the outputs are three-state. Taking the TE low places these ports in the high-impedance state. The driver outputs are designed to handle up to 48 mA sink current loading. An active-turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. See Figure 9-110 for the logic symbol and functional block diagram.



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

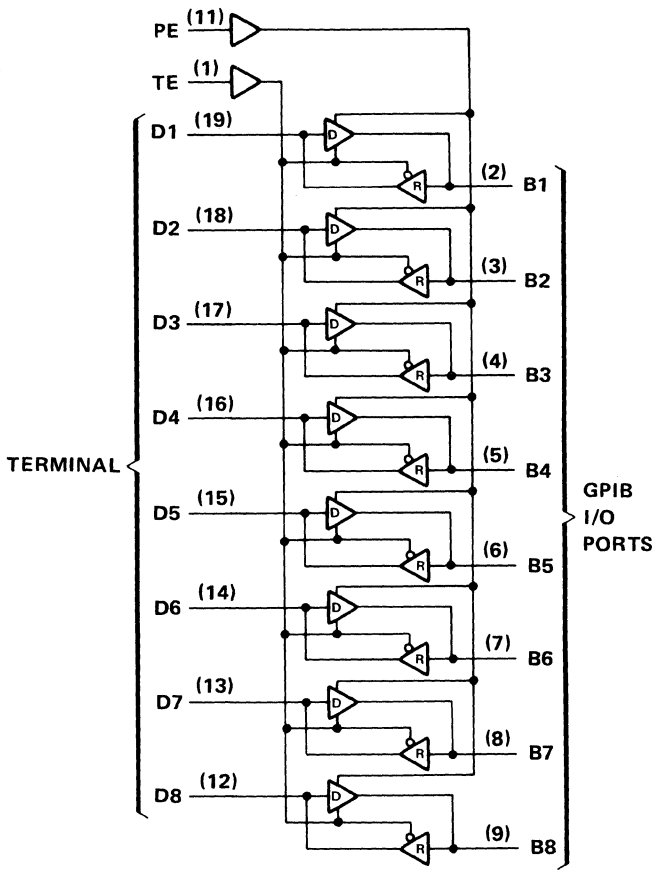


Figure 9-110. SN75160A Logic Symbol and Logic Diagram (Positive Logic)

Some additional features of the SN75160A are as follows:

PNP inputs for low drive requirements suitable for CMOS as well as TTL levels.

Totem-pole outputs on driver and receiver (open-collector option on driver).

Receiver hysteresis — 650 mV typical.

Low power dissipation — 66 mW per channel.

Fast propagation times — 22 ns maximum.

Figure 9-111 shows the totem-pole outputs on the driver and receiver sections. Notice the open-collector driver output option on the output port.

SN75163A Octal GPIB Transceiver

The SN75163A octal transceiver is functionally similar to the SN75160A but is not dedicated to a specific standard as is the SN75160A. The SN75163A does not have the built-in terminating resistors and as a result may be used to drive low impedance coax lines or other lines with impedances that differ from the IEEE-488 specification. Otherwise, the SN75163A shares the same features as the SN75160A.

SN75161A and SN75162A Octal GPIB Transceiver

The SN75161A and SN75162A eight-channel GPIB transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE-488. Each transceiver is designed to handle the bus-management, data-transfer and control signals of a single- or multiple-controller instrumentation system. When combined with the SN75160A, the SN75161A or SN75162A provides the complete 16-wire interface for the IEEE-488 bus. The pinouts and table of abbreviations are given in Figure 9-112.

The SN75161A and SN75162A each feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and instrument sides. The direction of data through the driver-receiver pairs is determined by the DC, TE, and SC (on SN75162A) enable signals. The SC input on the SN75162A allows the REN and IFC transceivers to be controlled independently. The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when $V_{CC} = 0$. See Figure 9-113 for the logic symbols for each device and Figure 9-114 for the functional block diagram of each device.

Table 9-14 shows the receive/transmit functions of the SN75161A and SN75162A.

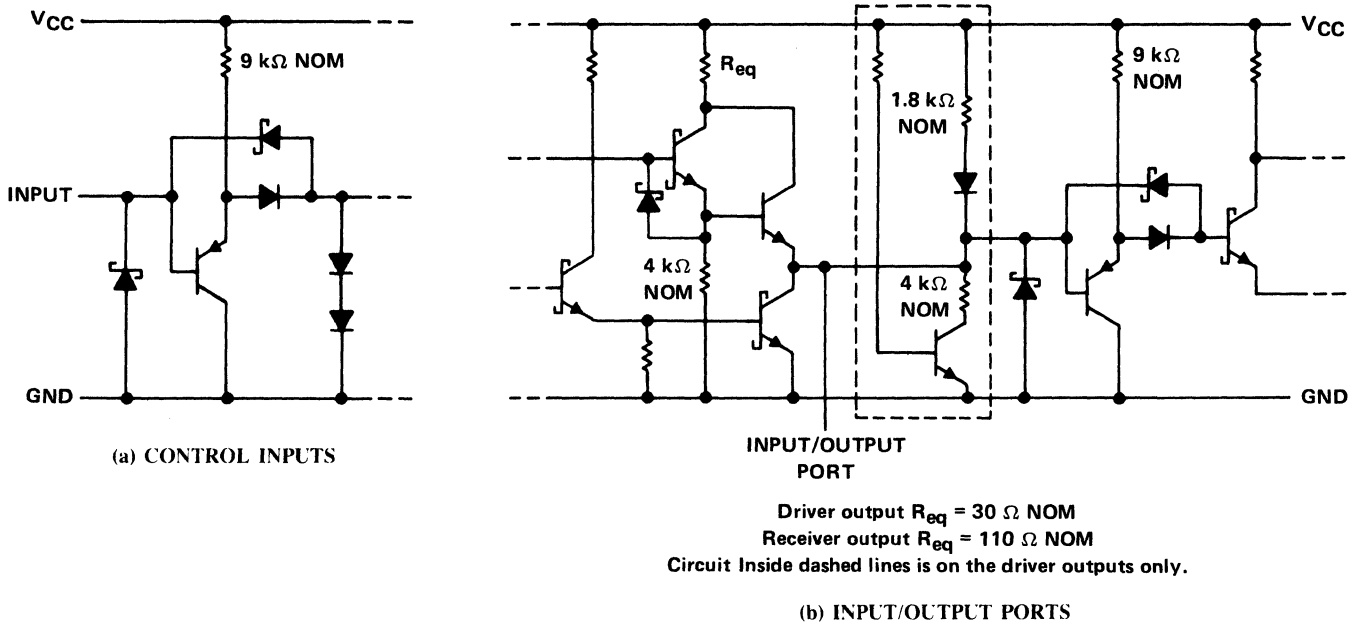
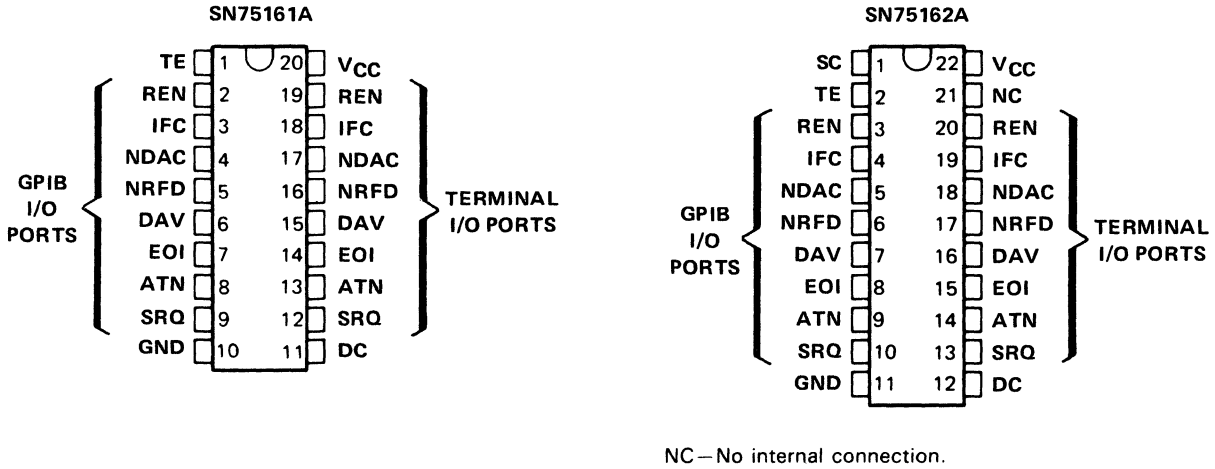


Figure 9-111. Equivalent Schematics of SN75160A Input and Output Sections

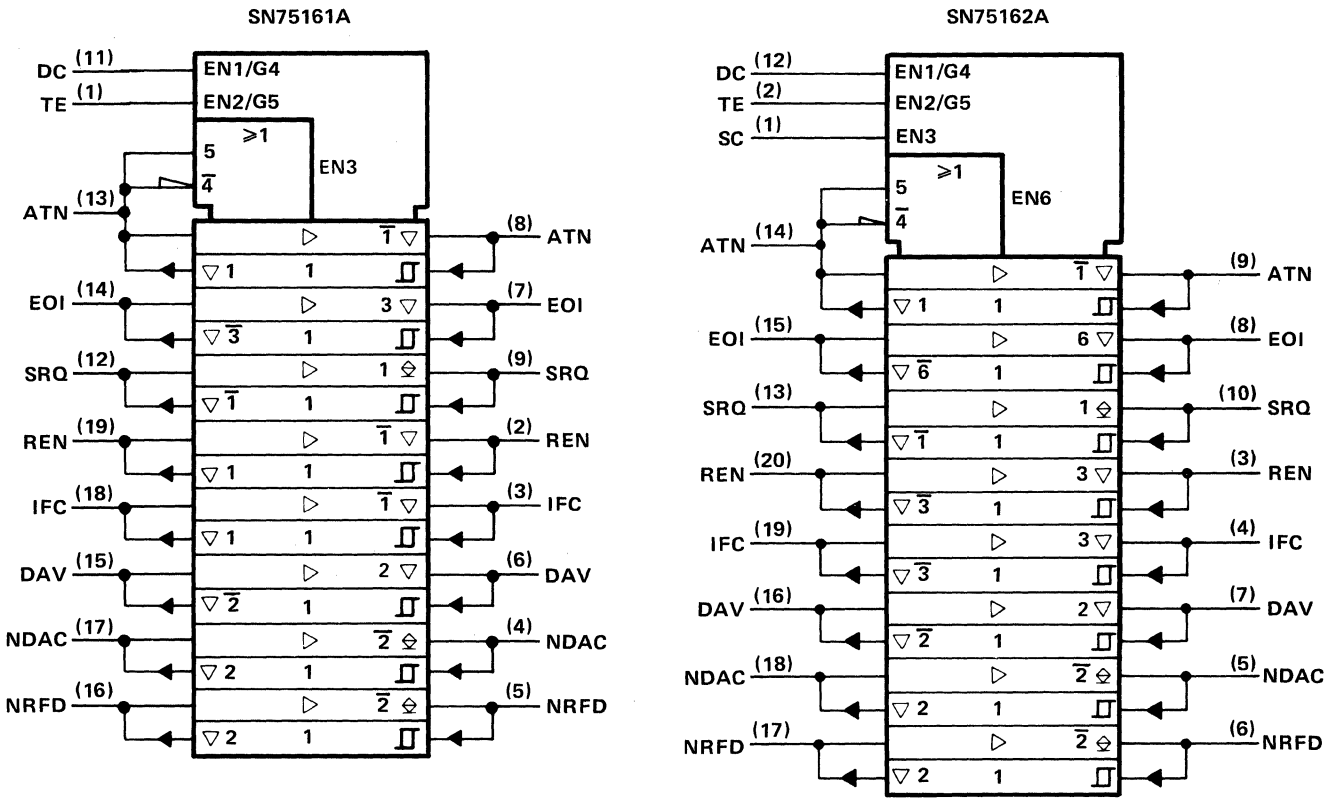


NC—No internal connection.

TABLE OF ABBREVIATIONS

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162 only)	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Edentify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

Figure 9-112. SN75161A and SN75162A Pinouts and Table of Abbreviations



▽Designates 3-state output, ⏀designates open-collector outputs. These symbols are in accordance with IEEE Std 91-1984 and IEC publication 617-12.

Figure 9-113. Logic Symbols for SN75161A and SN75162A

Figure 9-115 shows the equivalent schematics of the inputs and outputs of the SN75161A and the SN75162A.

MC3446 Quad Bus Transceiver

This device is a quad, single-ended line transceiver designed for bidirectional flow of data and instructions. See Figure 9-116 for pinout and function table.

Each driver output is tied to the junction of an internal voltage divider that sets the no-load output voltage and provides bus termination. The driver outputs are guaranteed to be off during power up and power down if either input is high. The receivers feature 950 mV typical hysteresis for noise immunity. The MC3446 is designed to meet IEEE Standard 488 — 1975 requirements.

Equivalent schematics of the device inputs and outputs are shown in Figure 9-117. The MC3446 drivers feature open-collector outputs for party-line operation. Like the SN75160 family, the driver outputs stay off during power up and power down sequencing.

TYPICAL APPLICATIONS

To use the SN75160 family of bus transceivers effectively, a bus controller or interface device should be used. The Texas Instruments TMS9914A is designed to perform the interface function between the IEEE 488 — 1975/1978 GPIB and a microprocessor. IEEE 488 — 1975/1978 standard protocol is handled automatically in Talker, Listener, or Controller operational modes. The TMS9914A is used when an intelligent instrument is required to communicate with the IEEE-488 bus. It performs the interface function between the microprocessor and bus and relieves the processor of the task of maintaining IEEE-488 protocol. By utilizing the interrupt capabilities of the device the bus does not have to be continually polled, and fast responses to changes in the interface configuration can be achieved. A block diagram showing the TMS9914A in a typical application is given in Figure 9-118.

The TMS9914A input/output pins are connected to the IEEE-488 bus via bus transceivers. The direction of data flow is controlled by the TE and Controller outputs generated in the TMS9914A. The SN75160A, SN75161A, and SN75162A are designed specifically as bus interfaces. The TE and Controller signals are routed within the devices so that the transceivers on particular lines are controlled as required by the TMS9914A. Other transceivers may be used but they may require additional external logic, particularly around the EOI line transceiver.

Communication between the microprocessor and TMS9914A is carried out via memory-mapped registers. There are 13 registers within the TMS9914A: six are read only registers and seven are write only registers. They are used both to pass control data to, and get status information from, the instrument.

The three least significant address lines from the MPU are connected to the register select lines RS0, RS1, and RS2 and determine the particular register selected. The high order

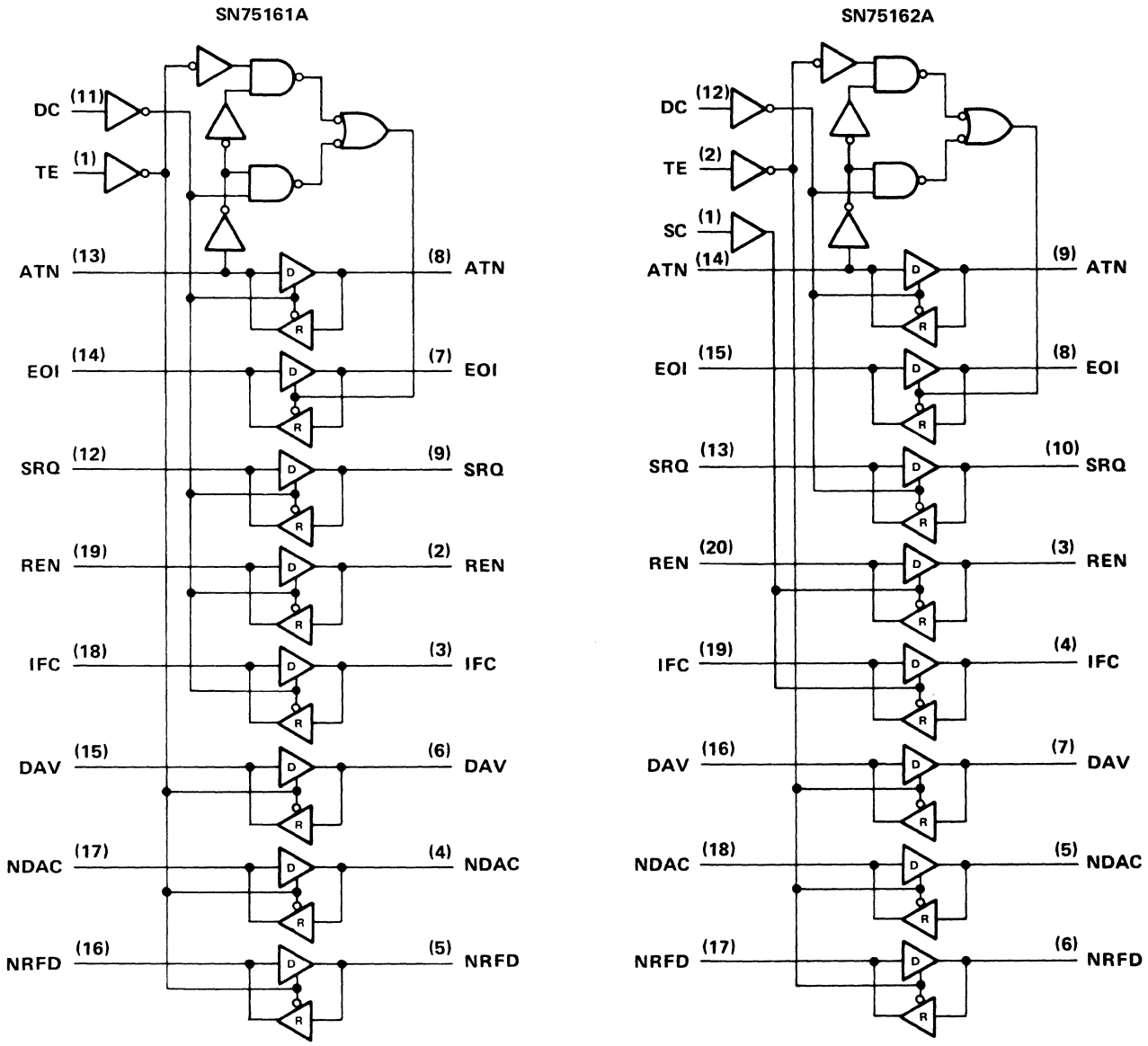


Figure 9-114. Logic Diagrams (Positive Logic) of SN75161A and SN75162A

address lines are decoded by external logic to cause the CE input to the TMS9914A to be pulled low when any one of eight consecutive addresses is selected. Thus, the internal registers appear to be situated at eight consecutive locations within the MPU address space. Reading or writing to these locations transfers information between the TMS9914A and the microprocessor. Note that reading and writing to the same location will not access the same register within the TMS9914A since they are either read only or write only registers. For example, a read operation with RS2 – RS0 = 011 gives the current status of the GPIB interface control lines, whereas a write to this location loads the auxiliary command register.

Each device on the bus is given a 5-bit address enabling it to be addressed as a talker or listener. This address is set on an external DIP switch (usually at the rear of an instrument) before power-on and is both read by the microprocessor and written into the register as part of the initialization procedure. The TMS9914A responds by causing a MA (My Address) interrupt and entering the required addressed state when this address is detected on the GPIB data lines.

A TYPICAL IEEE-488 SYSTEM APPLICATION

Figure 9-119 shows a possible transceiver connection between the TMS9914A and a remote station. This station could be a printer, digital multimeter, frequency counter, or other equipment of this type. The remote stations may talk only, listen only, or talk and listen. In the case of the SN75162A the remote station may, in addition to being able to talk and listen, be able also to assume control of the system. This is done by the System Control pin (SC) on the SN75162A.

The SN75160A is a 20-pin device used to communicate with the IEEE-488 data lines [DIO(1-8)] in all applications. Its mode of operation is controlled by the Talk Enable (TE) output of the TMS9914A. This active high signal becomes true whenever there is an interface function of the

Table 9-14. SN75161A and SN75162A Receive/Transmit Function Tables

SN75161A

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162A

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

TMS9914A not sending the NUL message on DIO(1-8), that is when the device is in TACS, CACS, SPAS, or PPAS. The Pull-Up Enable (PE) input of the SN75160A is an active high input which selects whether the DIO(1-8) lines are driven by open-collector or totem-pole outputs. A totem-pole driver output is required for faster data rates. Open-collector outputs must be used if parallel polling is required. If only one of these features is desired the PE input may be hard wired. Otherwise, it must be derived from ATN and EOI, as shown in Figure 9-119.

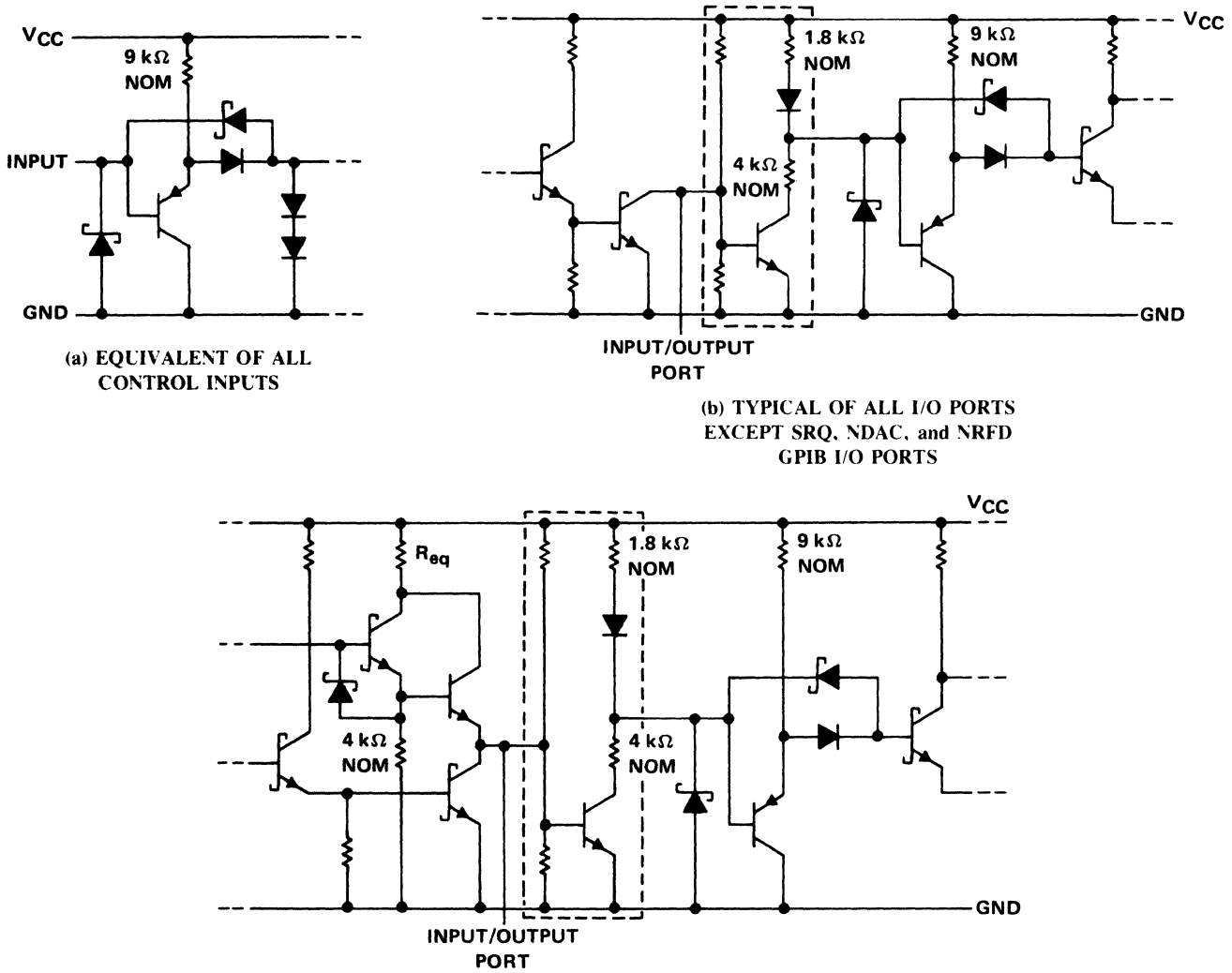
The SN75161A is a 20-pin device used with the IEEE-488 interface management lines. It may be used for a talker/listener device or for a controller which does not pass control. The direction of the handshake line transceivers NRFD, NDAC, DAV are again controlled by the TE signal. However, the SRQ, ATN, REN, and IFC transceivers are controlled by the DC input of the SN75161A, which connects to the Controller Active (CONT) output of the TMS9914A. CONT is low whenever the TMS9914A is an active controller, that is, when it is not in DIDS or CADS. The SN75161A also includes the logic to control the direction of the EOI transceiver. This is dependent on the TE signal when ATN is false (high) and on the DC signal when ATN is true (low).

The SN75162A is a 22-pin device which may be used to interface with the IEEE-488 interface management lines in all applications including devices which pass control. The SN75162A has a separate pin to control the direction of the REN and IFC transceivers, but is otherwise identical to the SN75161A. This input is the System Controller (SC) input which may be hard wired or switchable to determine whether the instrument in question is a controller. The REN and IFC outputs of the TMS9914A are controlled by the auxiliary commands "sre" and "sic". These should never be used by the host MPU unless it is the system controller.

IBM SYSTEM 360/370 INTERFACING CIRCUITS

The purpose of the interface is to provide a ready physical connection to System/360 and System/370 control units. Information, in the form of data, status and sense information, control signals, and I/O addresses is transmitted over the time- and function-shared lines of this interface. The I/O interface (channel to control unit) is the communication link between a channel, or line, and the various I/O control units in the IBM System/360 and System/370. Information on the complete design of this interface is available from:

IBM SYSTEM PRODUCTS DIVISION
PRODUCT PUBLICATIONS DEPT. B98
PO BOX 390
POUGHKEEPSIE, N.Y. 12602



(a) EQUIVALENT OF ALL CONTROL INPUTS

(b) TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS

(c) TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORTS

Figure 9-115. Input/Output Sections of SN75161A and SN75162A

The design of the interface provides several important features:

1. A degree of consistency in input/output programming for a wide range of control units.
2. Ready physical connection to System/360 and System/370 control units designed by any manufacturer.
3. Ability to physically accommodate future control units designed to meet the parameters of this interface specification.
4. An interlocked interface operation that is, in most cases, time independent: this feature increases the variety of control units that may be attached.
5. An operation applicable to both multiplex and burst mode operations as well as many control operations and channel-to-channel transmissions.
6. Up to eight control units may be serviced per set of lines.

DRIVER AND RECEIVER REQUIREMENTS

Driver Requirements

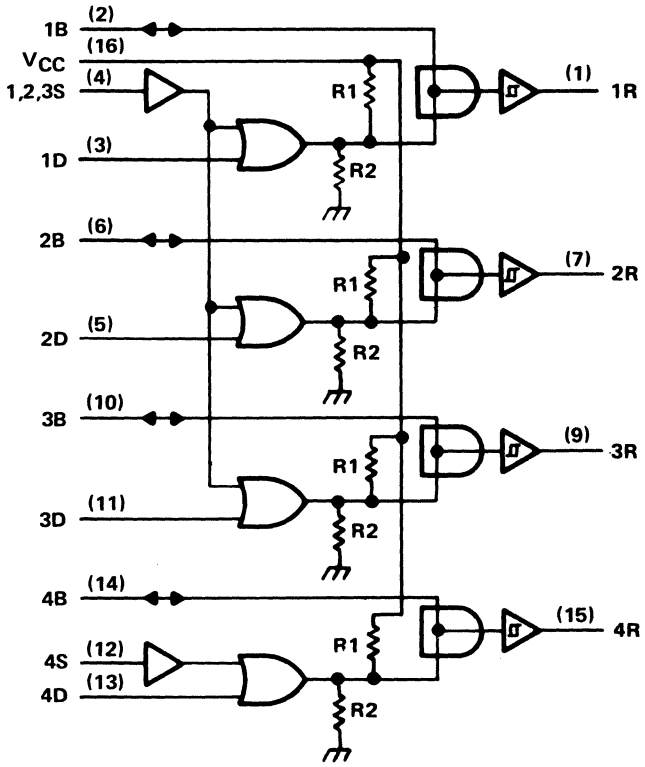
A driver at one extreme end of the data line must be able to drive up to 10 receivers. Up to 10 drivers must be able to be wire-OR connected to drive one receiver. The receiver would be located at one extreme end of the data line.

In the logic zero state:

1. The driver output voltage must not exceed 0.15 V at a load of 240 μA. (See Figure 9-120 for the definition of driver current polarity.)

In the logic one state:

1. The driver output voltage must be 3.11 V or greater at a load of 59.3 mA.



R1 = 2.4 kΩ NOM, R2 = 5 kΩ NOM

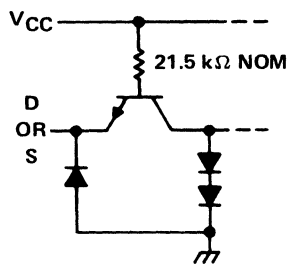
FUNCTION TABLE (TRANSMITTING)

INPUTS		OUTPUT	
S	D	B	R
L	H	H	H
L	L	L	L

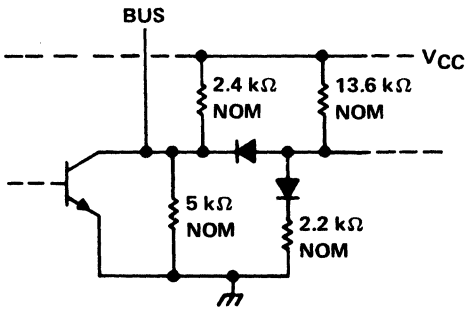
FUNCTION TABLE (RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	H
H	L	X	L

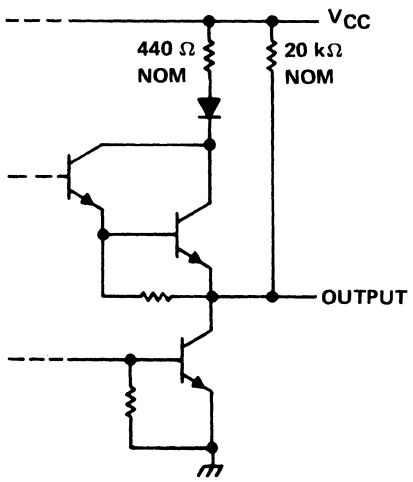
Figure 9-116. MC3446 Logic Diagram and Function Tables



(a) DRIVER AND STROBE INPUT



(b) DRIVER OUTPUTS/RECEIVER INPUTS



(c) RECEIVER OUTPUTS

Figure 9-117. MC3446 Input and Output Equivalent Circuits

2. The output voltage must not exceed 5.85 V at a load of 30 μA.
3. The output voltage must not exceed 7.0 V at a load of 123.0 mA during an overvoltage internal to the driver.

Drivers must be designed to ensure that no spurious noise is generated on the line during a normal power-up or power-down sequence. For the driver this may be accomplished by one of the following methods:

1. Sequencing the power supplies.
2. Building noise suppression into the circuit.
3. Providing an externally controlled gate. (See Figure 9-121.)

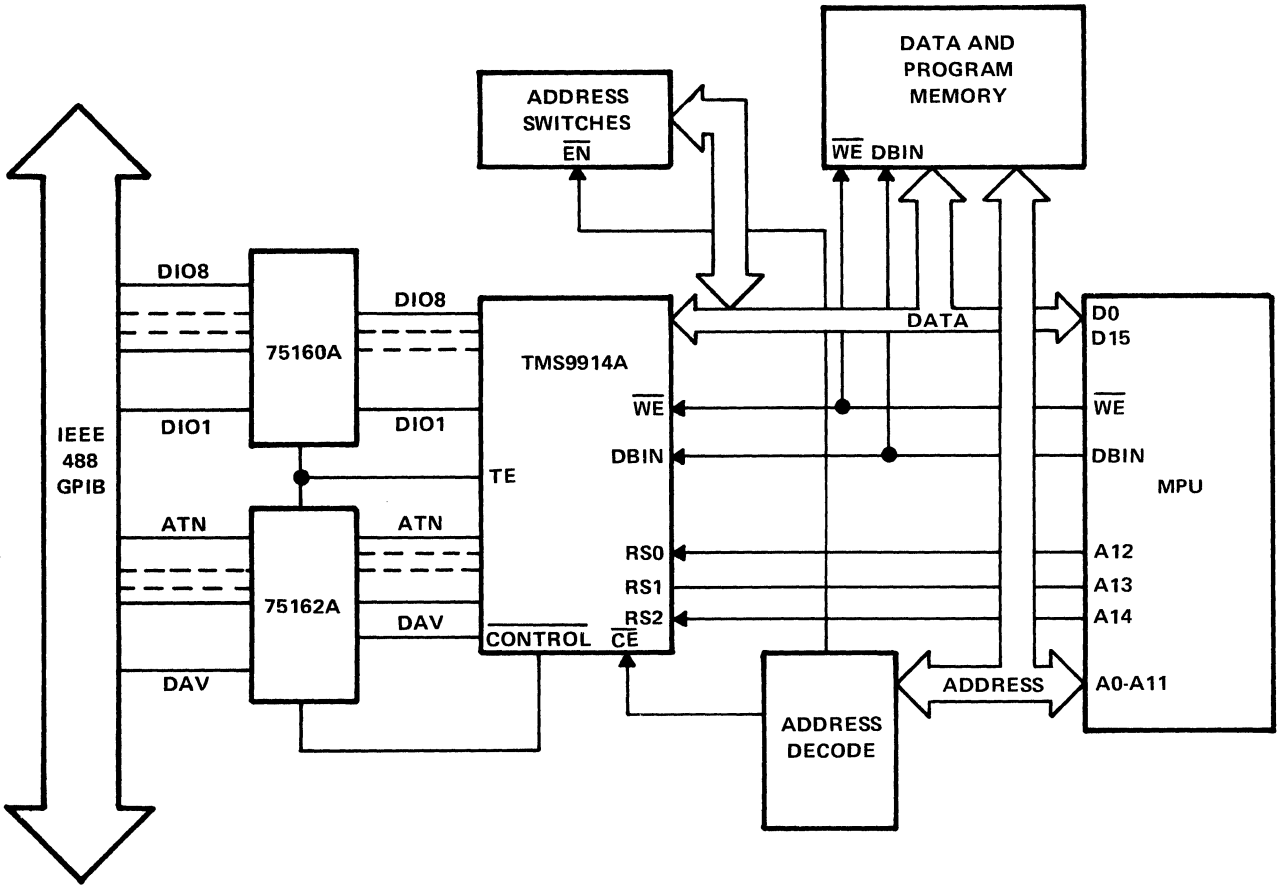


Figure 9-118. Typical TMS9914A Application Block Diagram

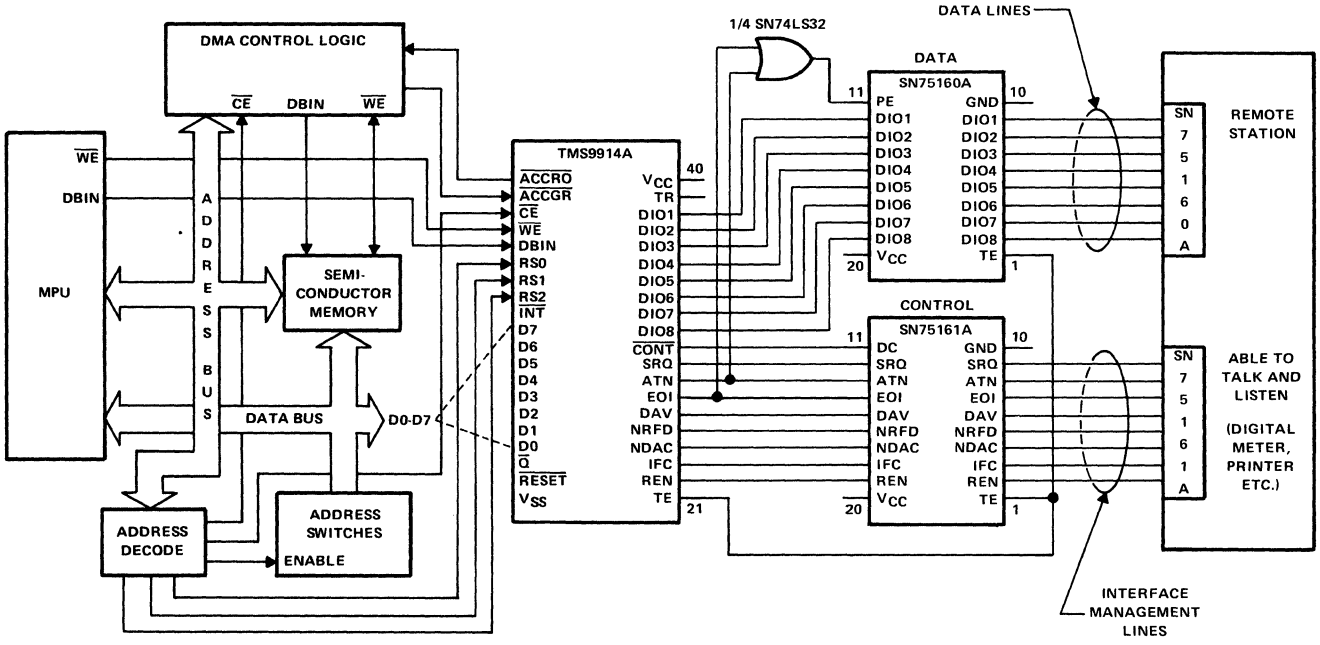


Figure 9-119. Typical IEEE-488 System Application

For a normal power-down sequence:

1. Logically ensure that the driver is in the zero state.
2. Close contact S. (See Figure 9-121.)
3. Turn power off.

For a normal power-up sequence:

1. Ensure that contact S is closed.
2. Turn power on.
3. Logically ensure that the input level will cause the driver output to be in the zero state.
4. Open contact S.

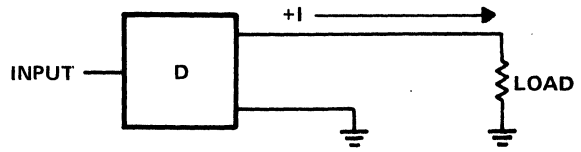


Figure 9-120. Driver Current Polarity

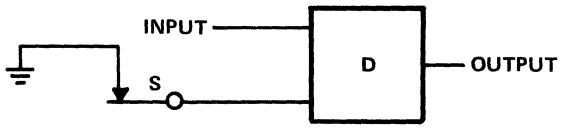


Figure 9-121. Driver Control Gate Switch (S)

Receiver Requirements

If there are multiple receivers on a single data line they must be spaced a minimum of 3 feet apart.

An input voltage (relative to receiver circuit ground) of 1.7 V or greater is interpreted as a logic one; an input of 0.70 V or less is interpreted as a logic zero.

The receiver should not be damaged by:

1. A dc input of 7.0 V with the receiver power on.
2. A dc input of 6.0 V with the receiver power off.
3. A dc input of −0.15 V with power on or off.

To reduce the loading effect on the line, the receiver input resistance must be greater than 7400 Ω with any input voltage from 0.15 V to 3.9 V, and the negative receiver input current must not exceed −0.24 mA at an input voltage of 0.15 V. (See Figure 9-122 for the definition of receiver current polarity.)

Receivers must be designed to ensure that no spurious noise is generated on the line during a normal power-up or power-down sequence.

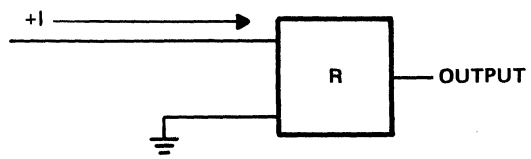


Figure 9-122. Receiver Input Current Polarity

GENERAL PHYSICAL AND ELECTRICAL REQUIREMENTS

Line Terminations

The terminating network must present a resistance of 95 Ω ±2.5% between the signal line and ground, and must be capable of dissipating 390 mW. An end-of-line driver or receiver may be placed beyond the terminator. In this case the distance between the end-of-line driver or receiver and the terminator must be less than 6 inches. No minimum requirement is set for the spacing between drivers. No minimum requirement is set for the spacing between a terminator and driver or receiver if the terminator is placed on the extreme end of the line. The maximum stub length from the line to a driver or receiver on the circuit card is 6 inches.

Voltage Levels

There are two logic voltage levels. A dc line voltage of 2.25 V or more denotes a logic one state, and a dc voltage of 0.15 V or less denotes a logic zero state. These voltages are relative to the driver ground.

Cable

All data lines must have a characteristic impedance of 92 Ω ± 10% and, with the exception of "select out", must be terminated at each extreme end in their characteristic impedance by a terminating network. For "select out/select in" see Select Out Circuitry in following paragraphs. Cable length may be limited under special conditions, but is never to exceed a maximum line resistance of 33 Ω. The 33 Ω limit includes all contact resistance, internal line resistance and interunit line resistance.

Ground Shift and Noise

The maximum noise (measured at the receiver input) coupled onto any signal line must not exceed 400 mV.

The maximum allowable ground shift, between an active driver and any receiver on the same interface line, is 150 mV. Therefore the maximum shift (coupled noise plus ground shift) allowed on any line is 550 mV. The line logic levels and receiver threshold levels allow for a 550 mV shift. That is, a worst-case 550 mV shift during a logic one state of 2.25 V (minimum) still guarantees a receiver input of at least 1.7 V. (See Figure 9-123.) Also during a logic zero state of 0.15 V (maximum) there is a guaranteed receiver input of less than 700 mV. (See Figure 9-124)

Fault Conditions

A grounded signal line must not result in damage to drivers, receivers, or line terminators. With one driver transmitting a logic one, loss of power in any other driver or receiver on the line must not result in any damage to circuits on that line. Data transmission must not be affected by a power-off condition of any driver or receiver on the line.

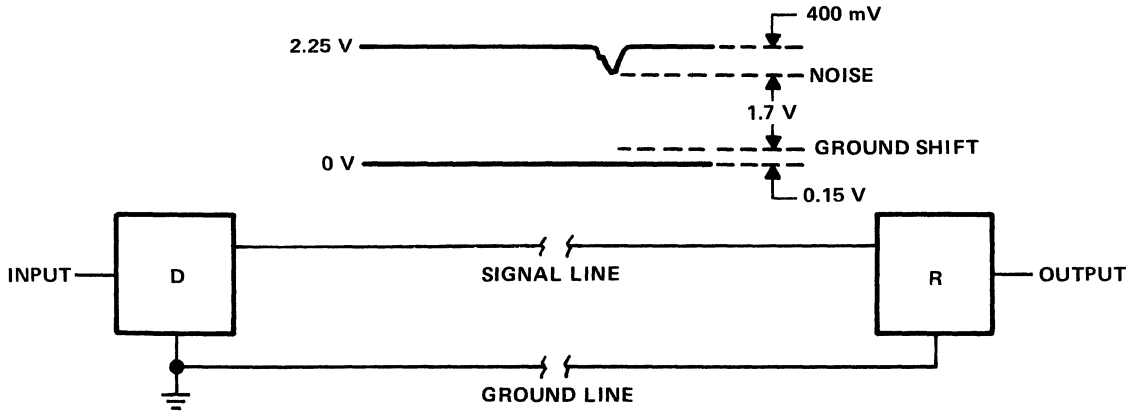


Figure 9-123. Negative Noise Spikes

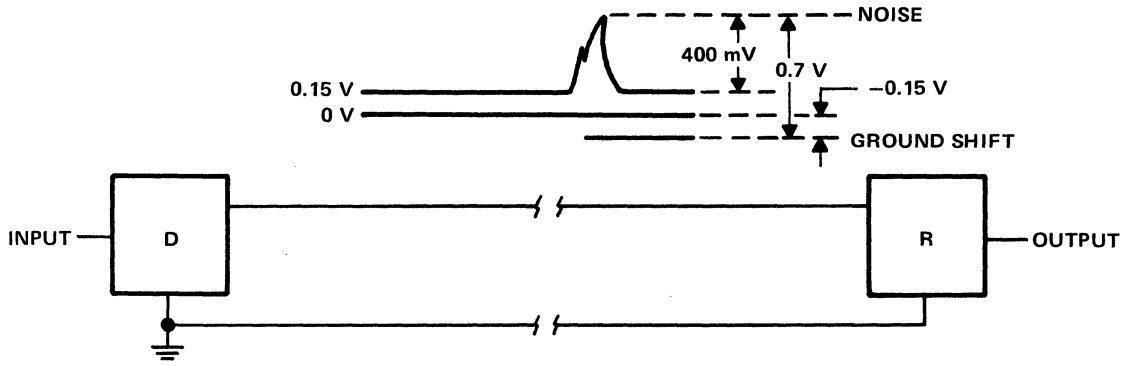


Figure 9-124. Positive Noise Spikes

ELECTRICAL CHARACTERISTICS FOR SELECT OUT INTERFACE

General

The "Select" line has a single-driver to single-receiver configuration, with only the receiver end of the line terminated in its characteristic impedance. A dc line voltage of 1.85 V or greater denotes a logic one state, and a dc line voltage of 0.15 V or less denotes a logic zero state. These voltages are relative to the driver ground. Because of the nature of the select out/select in line, negative noise tolerance has been neglected. All data line requirements not covered here are also applicable to the Select line.

Receiver Requirements

The Select line receiver must meet all the requirements given for the data line receivers.

Driver Requirements

The Select line driver must be capable of withstanding an output short to ground, while in the logic one or logic zero state, without damage to the driver circuit.

For the Select line logic zero state:

1. The driver output voltage must not exceed 0.15 V at a load of 1.0 mA.

For the Select line logic one state:

1. The driver output voltage must exceed 3.7 V at a load of 41 mA.
2. The driver output must not exceed 5.8 V at a load of 0.3 mA.
3. The driver output must not exceed 7.0 V at a load of 72 mA during an overvoltage internal to the driver.

IBM SYSTEM/360 AND SYSTEM/370 DATA LINE DRIVERS

SN75123 Dual Line Driver

The SN75123 dual line driver is designed to meet IBM System/360 requirements. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN75123 will drive terminated lines such as coaxial or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 V. All of the inputs are conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced onto the line.

Figure 9-125 illustrates the logic symbol, logic diagram, package pin-out and equivalent driver output circuit. Features of the SN75123 include the following:

1. Meets IBM System/360 interface requirements.
2. Operates from a single 5 V supply.

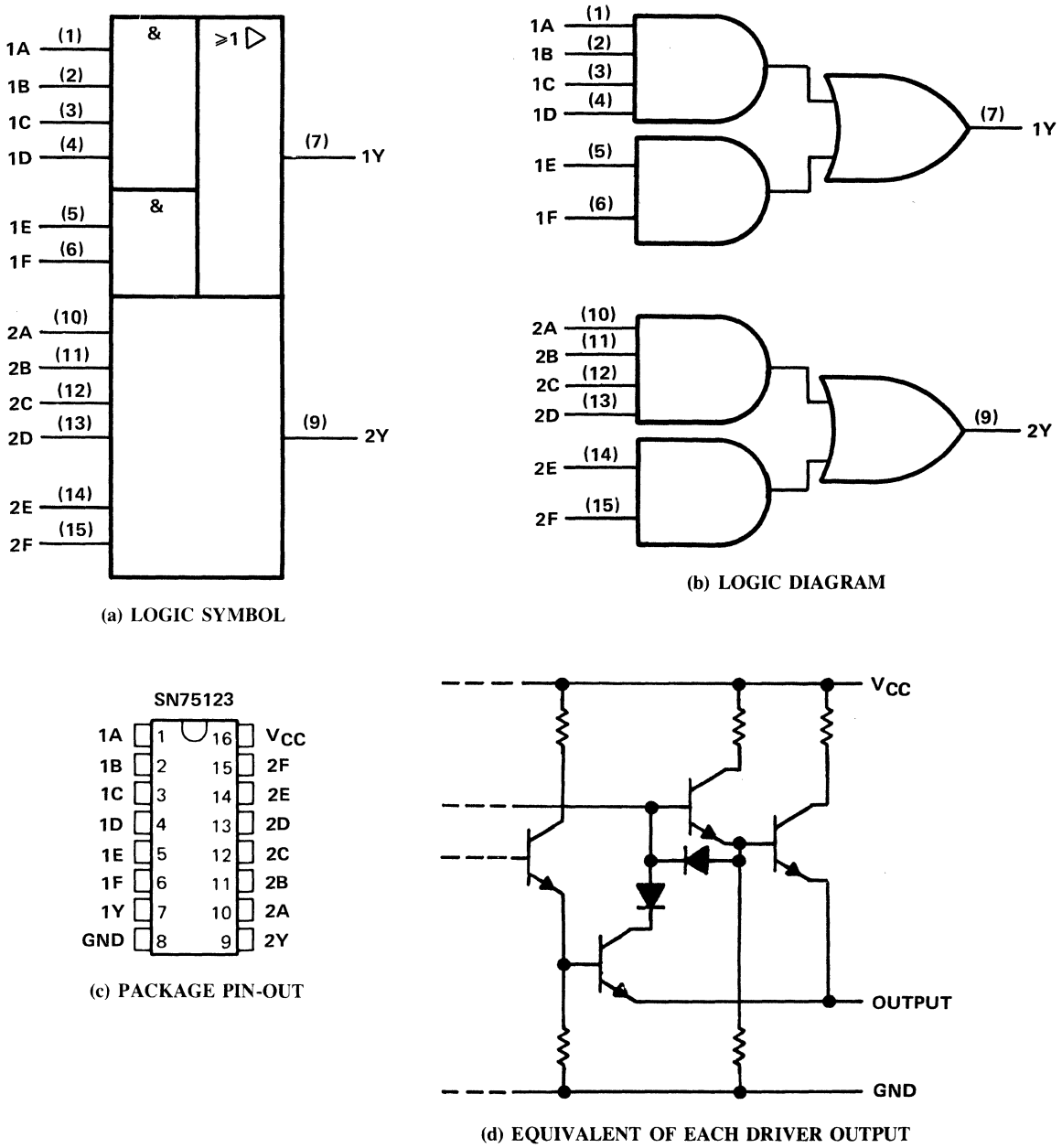


Figure 9-125. SN75123 Dual Line Driver

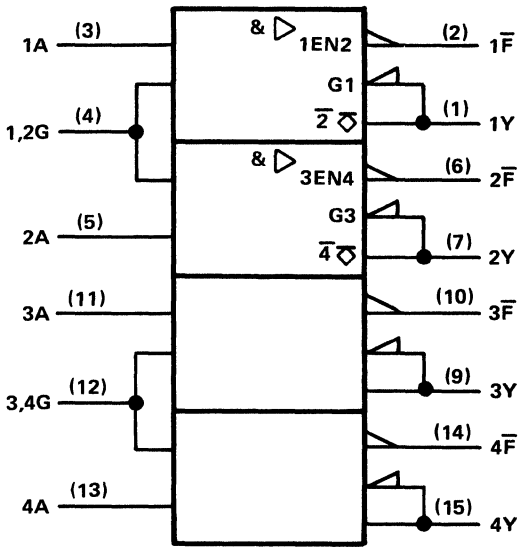
3. Plug-in replacement for the Signetics N8T23 dual driver.
4. 3.11 V output at $I_{OH} = -59.3$ mA.
5. Uncommitted emitter output structure for party-line operation.
6. Short-circuit protection.
7. Multiple input AND gates.

SN75126 Quadruple Line Driver

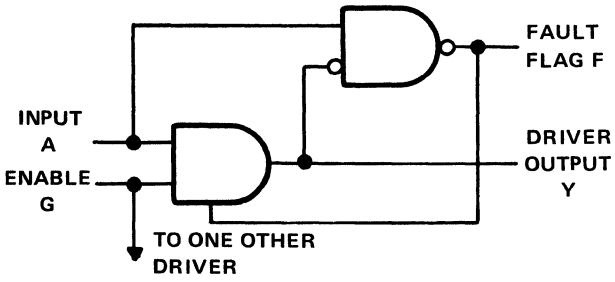
The SN75126 quadruple line driver is designed to meet the IBM System/360 and System/370 I/O specifications GA22-6974-3. The output voltage is 3.11 V minimum (at $I_{OH} = -60$ mA) over the recommended ranges of supply voltage (4.5 V to 5.5 V) and temperature (0 °C to 70 °C). This device is compatible with standard TTL logic and supply levels. Fabrication techniques employ low-power Schottky technology to achieve fast switching and low power dissipation. The data bus is not disturbed during power-up or power-down sequencing. Fault flag circuitry is designed to sense a line short on any Y output line, output a low logic level, and reduce the output current to a safe level.

The SN75126 is designed for use with the SN75125 or SN75127 seven-channel receivers, or the SN75128 or SN75129 eight-channel receivers. Figure 9-126 illustrates the logic symbol, logic diagram, package pin-out, and equivalent driver output circuit. Features of the SN75126 include:

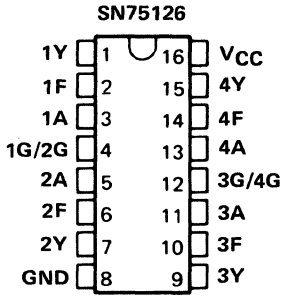
1. Meets IBM 360/370 I/O interface specifications GA22-6974-3.



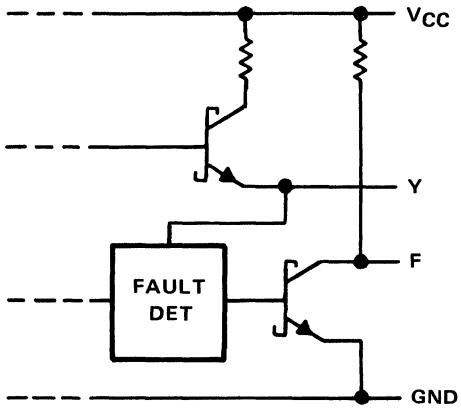
(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM FOR EACH DRIVER



(c) PACKAGE PIN-OUT



(d) EQUIVALENT OF EACH DRIVER OUTPUT

Figure 9-126. SN75126 Quad Line Driver

2. Output voltage of 3.11 V minimum at $I_{OH} = -60$ mA.
3. Overload protection with foldback current limiting.
4. High-speed, low-power Schottky circuitry.
5. Functionally interchangeable with the MC3481.

SN75130 Quadruple Line Driver

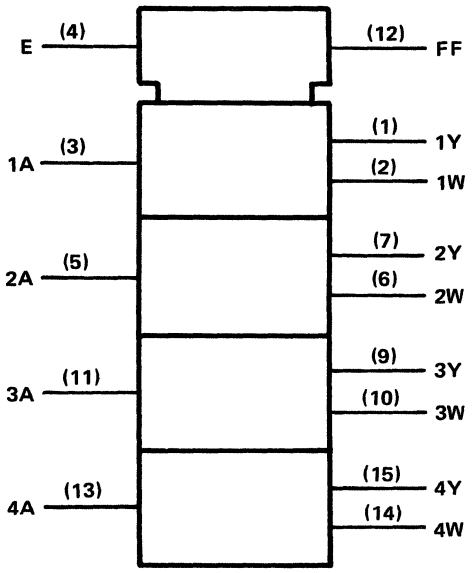
The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 V minimum (at $I_{OH} = -60$ mA) over the recommended ranges of supply voltage (4.5 V to 5.5 V) and temperature (0 °C to 70 °C). This device is compatible with standard TTL logic and supply voltages. Fabrication techniques employ low-power Schottky technology to achieve fast switching and low power dissipation. The data bus will not be disturbed during power-up or power-down sequencing. Fault flag circuitry is designed to sense a short on any of the Y output lines, output a logic zero level, and reduce the output current on the shorted line to a safe level. Figure 9-127 illustrates the SN75130 logic symbol, logic diagram, package pin-out and equivalent output circuitry. SN75130 features include the following:

1. Meets IBM 360/370 I/O interface specification GA22-6974-3.
2. Output voltage of 3.11 V minimum at $I_{OH} = -60$ mA.
3. Overload protection with foldback current limiting.
4. Common enable and common fault flag.
5. High-speed, low-power Schottky circuitry.
6. Functionally interchangeable with MC3485.

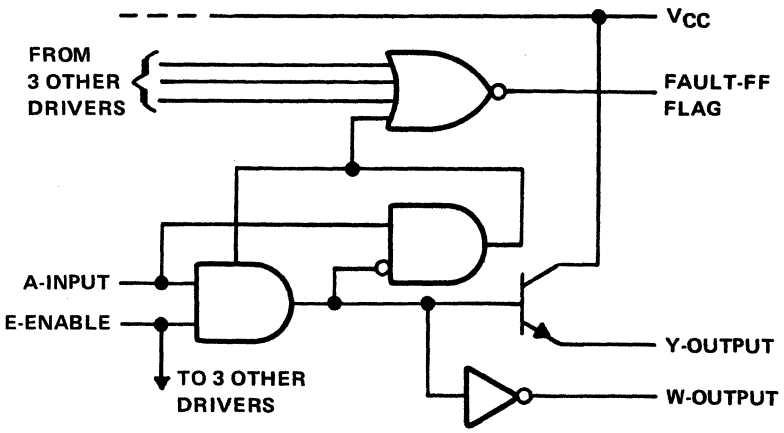
IBM SYSTEM/360 AND SYSTEM/370 DATA LINE RECEIVERS

SN75124 Triple Line Receiver

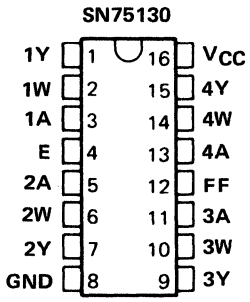
The SN75124 is designed to meet the IBM System 360 interface specifications. It is also compatible with standard TTL logic and supply voltage levels. The inputs have built-in hysteresis to provide increased noise margin for single-ended applications. An open line will affect the receiver input



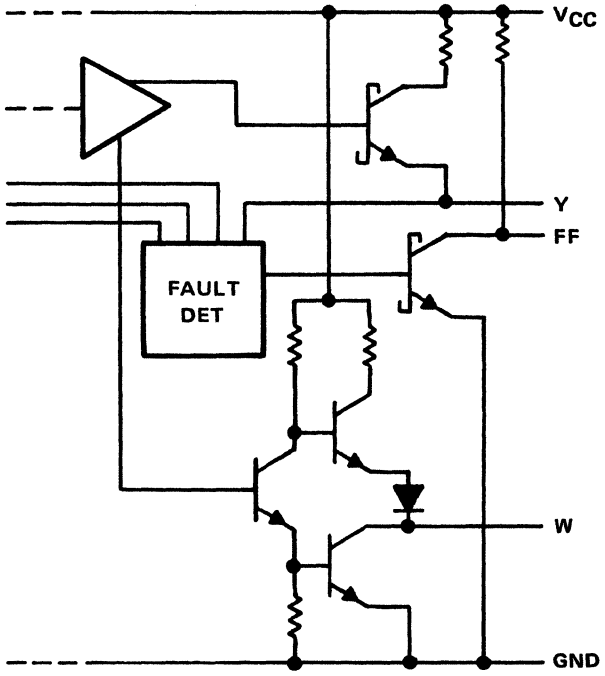
(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM FOR EACH DRIVER



(c) PACKAGE PIN-OUT



(d) EQUIVALENT OF EACH DRIVER OUTPUT

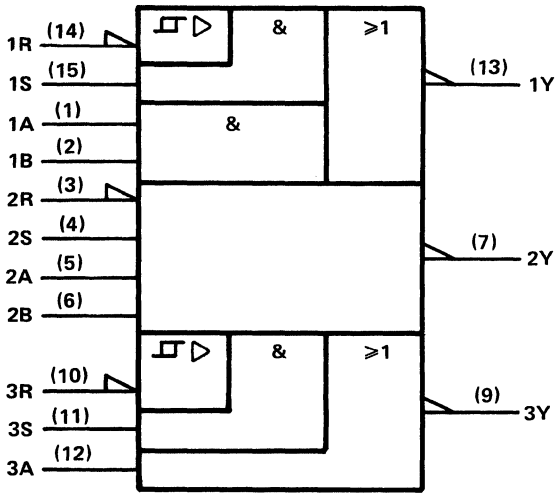
Figure 9-127. SN75130 Quad Line Driver

the same way as a low-level input voltage and the receiver input can withstand a level of −0.15 V with power on or off. The S input must be a logic high to enable the receiver input. Two of the receivers have A and B inputs which, if both are high, will hold the output low. The third receiver has only an A input which, if high, will hold the output low. Figure 9-128 shows the logic symbol, logic diagram, package pin-out and equivalent receiver input circuit. Features of the SN75124 include the following:

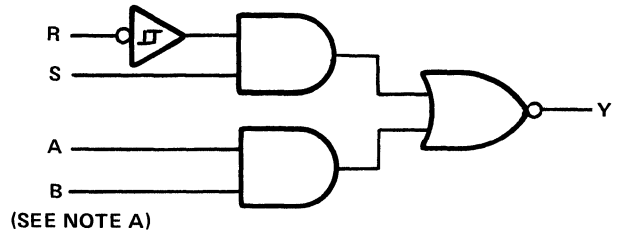
1. Meets IBM System/360 interface requirements.
2. Operates from a single 5 V supply.
3. TTL compatible output.
4. Plug-in replacement for the N8T24 triple receiver.
5. Built-in input threshold hysteresis.
6. High speed — Typical propagation delay time of 20 ns.
7. Independent channel strobes.

SN75125 and SN75127 Seven-channel Line Receivers

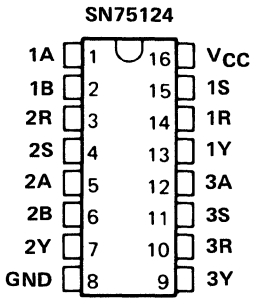
The SN75125 and SN75127 are single-ended, seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 interface specifications. Special low-power design and Schottky-clamped transistors allow for low supply current requirements while maintaining fast switching speeds. The SN75125 and SN75127 are characterized for operation from 0 °C to 70 °C. These receivers are identical in performance and differ only in their



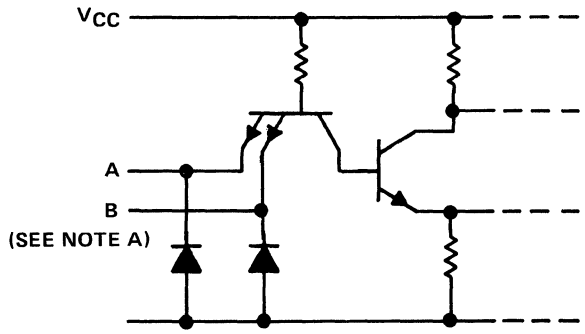
(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM FOR EACH RECEIVER



(c) PACKAGE PIN-OUT



(d) EQUIVALENT OF EACH RECEIVER INPUT

NOTE A: Channel 3 has only one data input.

Figure 9-128. SN75124 Triple Line Receiver

package pin-outs as shown in Figure 9-129. Figure 9-129 also illustrates the logic symbol, logic diagram and equivalent input circuit for these devices. Additional key features include the following:

1. Meet IBM 360/370 I/O specifications.
2. Input resistance of 7 kΩ to 20 kΩ.
3. TTL compatible outputs.
4. Operate from a single 5 V supply.
5. High speed and low propagation delays.
6. Low-to-high/high-to-low propagation delay ratios are specified.

SN75128 and SN75129 Octal Line Receivers

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy IBM 360/370 system I/O interface requirements. Both devices feature common strobes for each group of four receivers. The SN75128 has an active-high strobe; the SN75129 has an active-low strobe. Low-power Schottky-diode-clamped transistors allow low supply current requirements while maintaining fast switching speeds and high current TTL outputs. These receivers are characterized for operation from 0 °C to 70 °C. Figure 9-130 illustrates the device package pin-outs, logic symbol, logic diagram, and equivalent input circuit. SN75128 and SN75129 features include the following:

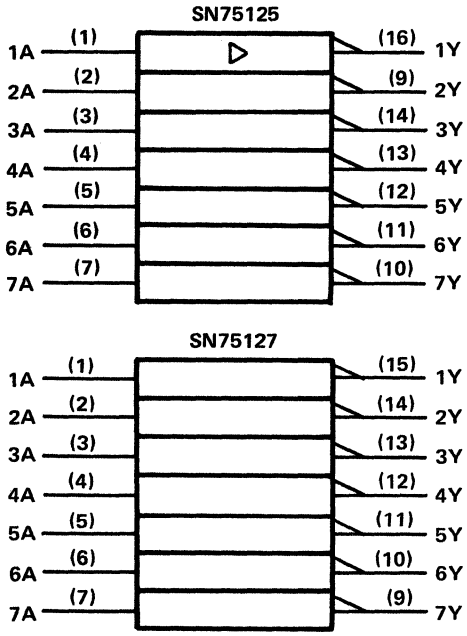
1. Meet IBM 360/370 I/O specifications.
2. Input resistance from 7 kΩ to 20 kΩ.
3. Outputs compatible with TTL.
4. Operate from a single 5 V supply.
5. High speed and low propagation delay.
6. Low-to-high and high-to-low propagation delay ratios specified.
7. Common strobe for each group of four receivers.

IBM SYSTEM 370 APPLICATION

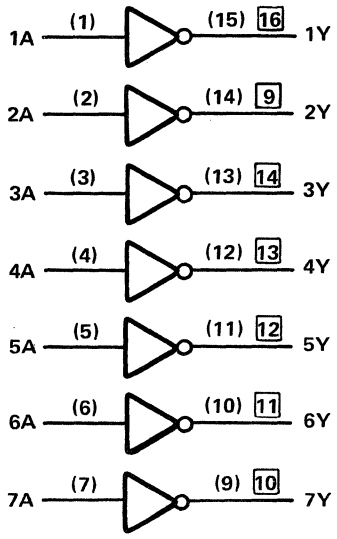
A typical application is shown in Figure 9-131. An output from a 370-type computer provides addressing and control information to eight remote test stations and an input is used to receive data back on status and test results.

Drivers

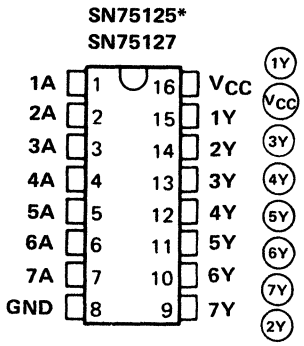
The SN75126 quad line driver is selected to provide sufficient drive to meet 370 requirements and a fault flag output. The fault flag output can be used to warn the host computer of line shorts and minimize driver power dissipation. The driver power supply must be 5.0 V ± 10%



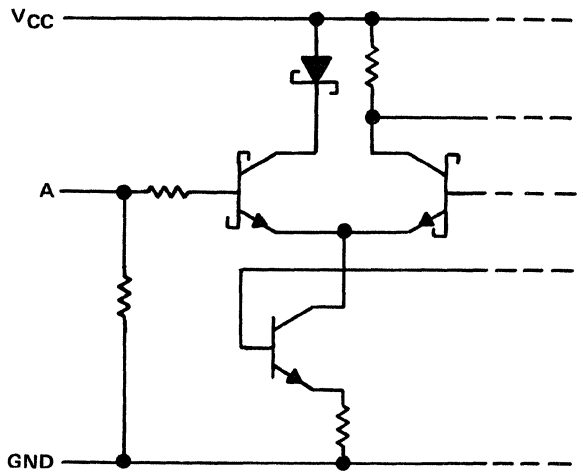
(a) LOGIC SYMBOL



(b) LOGIC DIAGRAM



(c) PACKAGE PIN-OUT



(d) EQUIVALENT OF EACH RECEIVER INPUT

Figure 9-129. SN75125/SN75127 Seven-Channel Receivers

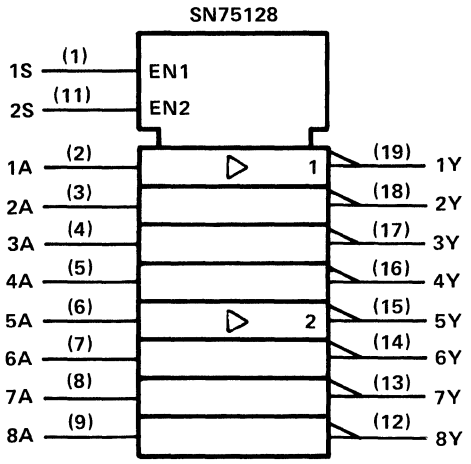
and output drive will meet the 3.11 V minimum at an I_{OH} of −60 mA. Fault flag outputs are standard TTL levels and may be used to interface with special fault detection circuitry or directly with the 370 as illustrated.

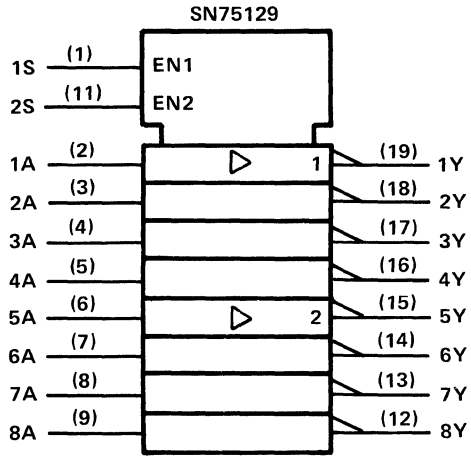
Cable

The cable selected is type 62AU coax (Belden 9269). The signal conductor is #22 solid copper with a dc resistance of 0.0412 Ω per foot. Shield coverage is 95% and has a dc resistance of 0.0026 Ω per foot. Allowing 3 Ω for contact resistance and internal connections we are left with 30 Ω maximum line resistance. The resulting overall line length for the system is therefore 30/0.0412 or 728 feet maximum. It should be remembered that stubs from the main line must be kept as short as possible (less than six inches) and spacing between receiver stations must be in excess of 3 feet.

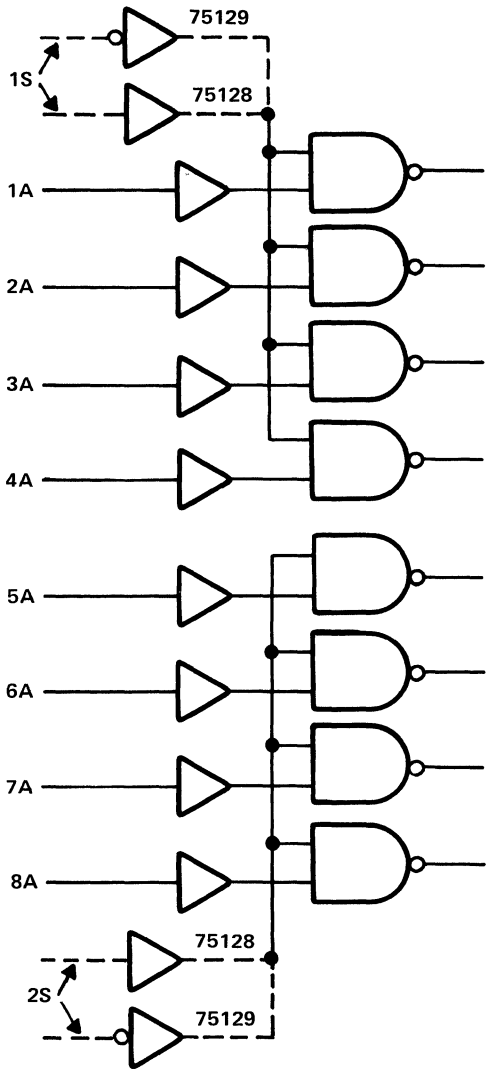
Receivers

The receivers selected for this application are SN75128 octal receivers with strobes. Receiver input resistance is guaranteed to be greater than 7 kΩ and as many as 10 receivers may be connected to a single line. In this application there are eight receivers on the clock/control line resulting in a total (worst-case) receiver dc loading of 875 Ω.

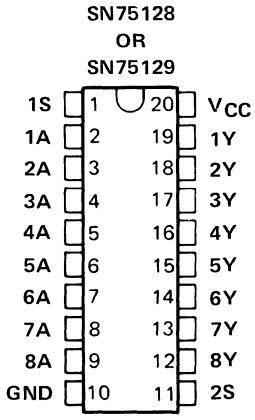




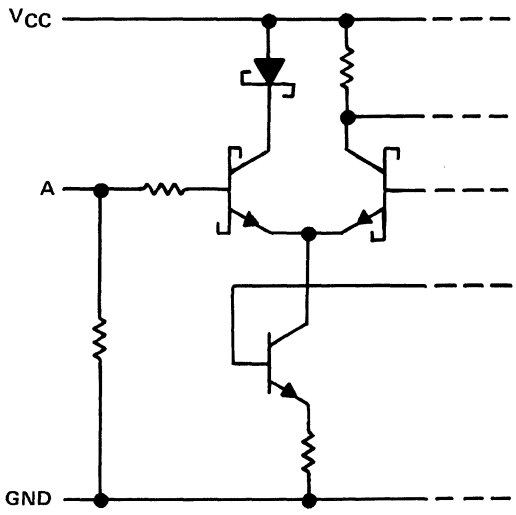
(a) LOGIC SYMBOLS



(b) LOGIC DIAGRAM



(c) PACKAGE PIN-OUT



(d) EQUIVALENT OF EACH RECEIVER INPUT

Figure 9-130. SN75128/SN75129 Eight-Channel Line Receivers

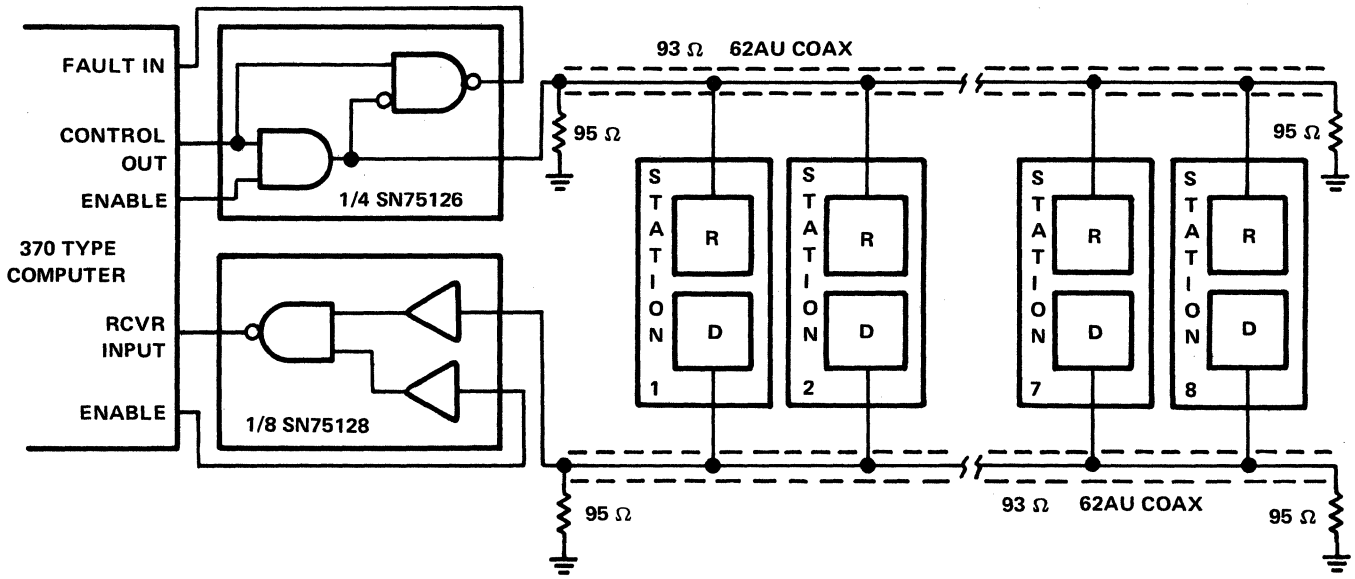


Figure 9-131. Typical IBM 370 Interface Application

APPENDIX

Device Numbering System

Table A-1, an overview of the device numbering system, shows the meaning of the various characters in Texas Instruments Linear and Interface circuit device numbers. Texas Instruments devices that are direct alternate sources for other manufacturers' parts carry the original part number including its prefix. Alteration in device characteristics from the original data sheet specifications, generally to improve performance, results in a new number with the appropriate SN55, SN75, TL, or TLC prefix. The type of package is also included in the device number. Table A-2 lists the package suffixes and their definitions.

Table A-1. Linear and Interface Circuits

XXX XXXXX XX — Package Type (See Table A-2)

ORIGINAL MANUFACTURER	TI PREFIX	DEVICE NUMBER	TEMP* RANGE
TI	TL or TLC	XXXC	COM
		XXXI	IND
		XXXM	MIL
	SN	75XXX	COM
		55XXX	MIL
NATIONAL	LM	1XXX	MIL
		2XXX	IND
		3XXX	COM
	ADC	XXXX	COM
	DS	78XX	MIL
		88XX	COM
RAYTHEON	RC	4XXX	COM
	RM	4XXX	MIL
SIGNETICS	NE	5/55XX	COM
	SA	5/55XX	AUTO
	SE	5/55XX	MIL
	N8T	XX	COM
FAIRCHILD	uA	7XXXC	COM
		7XXXI	IND
		7XXXM	MIL
	uA	9XXX	COM
MOTOROLA	MC	13/33XX	IND
		14/34XXX	COM
		15/35XX	MIL
SPRAGUE	UCN	XXX	COM
	UDN	XXXX	COM
	ULN	XXXX	COM
AMD	AM	XXXXXM	MIL
		XXXXXC	COM
SILICON GENERAL	SG	15XX	MIL
		25XX	IND
		35XX	COM
PMI	OP-	XX	COM

*Temperature ranges:

COM = 0°C to 70°C
IND = −25°C to 85°C
AUTO = −40°C to 85°C
MIL = −55°C to 125°C

Table A-2. Packages

TYPE	PACKAGE DESCRIPTION
N	Plastic DIP
NE, NG	Plastic DIP, copper lead frame
NF	Plastic DIP, 28 pin, 400 mil
NT	Plastic DIP, 24 pin, 300 mil
P	Plastic DIP, 8 pin
D	Plastic SO, small outline
J	Ceramic DIP
JD	Ceramic DIP, side braze
JG	Ceramic DIP, 8 pin
FE,FG	Ceramic chip carrier, rectangular
FH, FK	Ceramic chip carrier, square
FN	Plastic chip carrier, square
KA	TO-3 metal can
KC	TO-220 plastic, power tab
LP	TO-226 plastic
U	Ceramic flatpack, square
W, WC	Ceramic flatpack, rectangular

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