The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

# The Peripheral Driver Data Book

## for

## Design Engineers

1981

TEXAS INSTRUMENTS
INCORPORATED

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## IMPORTANT NOTICES

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Information contained herein supersedes previously published data on Peripheral Driver Interface Circuits, including data books CC415, *The Peripheral Driver Data Book 1977* (LCC4280), and portions of *The Interface Circuits Data Book*, first edition (LCC4330).

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## ALPHANUMERIC INDEX

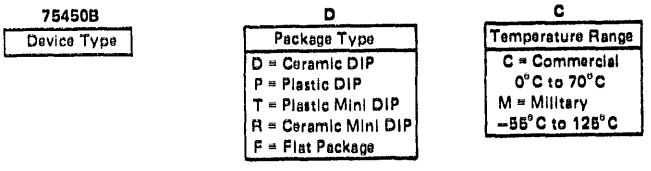
## INTERCHANGEABILITY GUIDE
## (MANUFACTURERS ARRANGED ALPHABETICALLY)

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

## FAIRCHILD

**EXAMPLE OF NOMENCLATURE**




| FAIRCHILD | TI DIRECT REPLACEMENT |
|---|---|
| 55450A | SN55450B |
| 55450B | SN55450B |
| 55451A | SN55451B |
| 55451B | SN55451B |
| 55452A | SN55452B |
| 55452B | SN55452B |
| 55453A | SN55453B |
| 55453B | SN55453B |
| 55454A | SN55454B |
| 55454B | SN55454B |
| 55460 | SN55460 |
| 55461 | SN55461 |
| 55462 | SN55462 |
| 55463 | SN55463 |
| 55464 | SN55464 |
| 55470 | SN55470 |
| 55471 | SN55471 |
| 55472 | SN55472 |
| 55473 | SN55473 |
| 55474 | SN55474 |
| 75430 | SN75430 |
| 75431 | SN75431 |
| 75432 | SN75432 |
| 75433 | SN75433 |
| 75434 | SN75434 |

| FAIRCHILD | TI DIRECT REPLACEMENT |
|---|---|
| 75450A | SN75450B |
| 75450B | SN75450B |
| 75451A | SN75451B |
| 75451B | SN75451B |
| 75452A | SN75452B |
| 75452B | SN75452B |
| 75453A | SN75453B |
| 75453B | SN75453B |
| 75454A | SN75454B |
| 75454B | SN75454B |
| 75460 | SN75460 |
| 75461 | SN75461 |
| 75462 | SN75462 |
| 75463 | SN75463 |
| 75464 | SN75464 |
| 75470 | SN75470 |
| 75471 | SN75471 |
| 75472 | SN75472 |
| 75473 | SN75473 |
| 75474 | SN75474 |
| 9665 | ULN2001A |
| 9666 | ULN2002A |
| 9667 | ULN2003A |
| 9668 | ULN2004A |

## ITT

EXAMPLE OF NOMENCLATURE:

| ITT | 55450 | −1 | D |
|---|---|---|---|
| Prefix | Device Type | Temperature Range<br>−1 = −55°C to 125°C<br>−5 = 0°C to 70°C | Package<br>D = Ceramic DIP<br>N = Plastic DIP |

| ITT | TI DIRECT REPLACEMENT | ITT | TI DIRECT REPLACEMENT |
|---|---|---|---|
| ITT55450 | SN55450B | ITT75450 | SN75450B |
| ITT55451 | SN55451B | ITT75451 | SN75451B |
| ITT55452 | SN55452B | ITT75452 | SN75452B |
| ITT55453 | SN55453B | ITT75453 | SN75453B |
| ITT55454 | SN55454B | ITT75454 | SN75454B |
| ITT55461 | SN55461 | ITT75461 | SN75461 |

## MOTOROLA

EXAMPLE OF NOMENCLATURE:

| MC | 75152 | P |
|---|---|---|
| Prefix | Type Number | Package<br>L = Ceramic DIP<br>P = Plastic DIP |

| MOTOROLA | TI DIRECT REPLACEMENT | MOTOROLA | TI DIRECT REPLACEMENT |
|---|---|---|---|
| MC75450 | SN75450B | MC75460 | SN75460 |
| MC75451 | SN75451B | MC75461 | SN75461 |
| MC75452 | SN75452B | MC75462 | SN75462 |
| MC75453 | SN75453B | MC75463 | SN75463 |
| MC75454 | SN75454B | MC75464 | SN75464 |

## NATIONAL

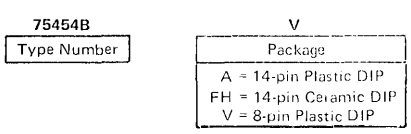
EXAMPLE OF NOMENCLATURE:

| DS | 75 | 463 | N |
|---|---|---|---|
| Prefix | Temperature Range<br>55 = −55°C to 125°C<br>75 = 0°C to 70°C | Type Number | Package<br>N = Plastic DIP<br>J = Ceramic DIP |

| NATIONAL | TI DIRECT REPLACEMENT | NATIONAL | TI DIRECT REPLACEMENT |
|---|---|---|---|
| DS55450 | SN55450B | DS75450 | SN75450B |
| DS55451 | SN55451B | DS75451 | SN75451B |
| DS55452 | SN55452B | DS75452 | SN75452B |
| DS55453 | SN55453B | DS75453 | SN75453B |
| DS55454 | SN55454B | DS75454 | SN75454B |
| DS55460 | SN55460 | DS75460 | SN75460 |
| DS55461 | SN55461 | DS75461 | SN75461 |
| DS55462 | SN55462 | DS75462 | SN75462 |
| DS55463 | SN55463 | DS75463 | SN75463 |
| DS55464 | SN55464 | DS75464 | SN75464 |

## SIGNETICS

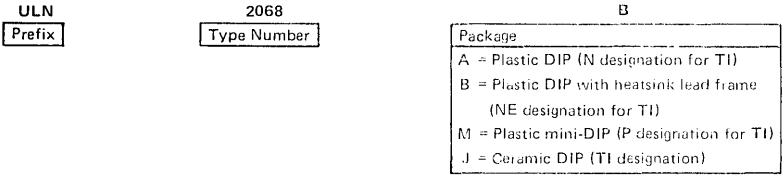
**EXAMPLE OF NOMENCLATURE:**




| SIGNETICS | TI DIRECT REPLACEMENT | SIGNETICS | TI DIRECT REPLACEMENT |
|---|---|---|---|
| 55450B | SN55450B | 75450B | SN75450B |
| 55451B | SN55451B | 75451B | SN75451B |
| 55452B | SN55452B | 75452B | SN75452B |
| 55453B | SN55453B | 75453B | SN75453B |
| 55454B | SN55454B | 75454B | SN75454B |

## SPRAGUE

**EXAMPLE OF NOMENCLATURE:**




| SPRAGUE | TI DIRECT REPLACEMENT | SPRAGUE | TI DIRECT REPLACEMENT |
|---|---|---|---|
| UDN2841 | UDN2841 | ULN2003A | ULN2003A |
| UDN2845 | UDN2845 | ULN2004A | ULN2004A |
| UDN3611 | SN75471 | ULN2005A | ULN2005A |
| UDN3612 | SN75472 | ULN2064 | ULN2064 |
| UDN3613 | SN75473 | ULN2065 | ULN2065 |
| UDN3614 | SN75474 | ULN2066 | ULN2066 |
| UDN5711 | SN75476 | ULN2067 | ULN2067 |
| UDN5712 | SN75477 | ULN2068 | ULN2068 |
| UDN5713 | SN75478 | ULN2069 | ULN2069 |
| UDN5714 | SN75479 | ULN2074 | ULN2074 |
| ULN2001A | ULN2001A | ULN2075 | ULN2075 |
| ULN2002A | ULN2002A | | |

# SELECTION GUIDE

## DRIVERS WITH LOGIC GATES

### Military Temperature Range (–55°C to 125°C)

| SWITCHING VOLTAGE | MAX RECOMMENDED OUTPUT CURRENT | DRIVERS PER PACKAGE | INTERNAL CLAMP DIODES | LOGIC GATE FUNCTION | | | | PACKAGE OPTIONS |
|---|---|---|---|---|---|---|---|---|
| | | | | AND | NAND | OR | NOR | |
| 20 V | 300 mA | 2 | – | SN55450B | | | | J |
| | | | | SN55451B | SN55452B | SN55453B | SN55454B | JG |
| 30 V | 300 mA | 2 | – | SN55460 | | | | J |
| | | | | SN55461 | SN55462 | SN55463 | SN55464 | JG |
| 55 V | 300 mA | 2 | – | SN55470 | | | | J |
| | | | | SN55471 | SN55472 | SN55473 | SN55474 | JG |

### Commercial Temperature Range (0°C to 70°C)

| SWITCHING VOLTAGE | MAX RECOMMENDED OUTPUT CURRENT | DRIVERS PER PACKAGE | INTERNAL CLAMP DIODES | LOGIC GATE FUNCTION | | | | PACKAGE OPTIONS |
|---|---|---|---|---|---|---|---|---|
| | | | | AND | NAND | OR | NOR | |
| 15 V | 300 mA | 2 | – | SN75430 | | | | J, N |
| | | | | SN75431 | SN75432 | SN75433 | SN75434 | JG, P |
| 20 V | 100 mA | 2 | – | | | SN75441 | | J, N |
| | 300 mA | 2 | – | SN75450B | | | | J, N |
| | | | | SN75451B | SN75452B | SN75453B | SN75454B | JG, P |
| 30 V | 300 mA | 2 | – | SN75460 | | | | J, N |
| | | | | SN75461 | SN75462 | SN75463 | SN75464 | JG, P |
| | 500 mA | 2 | – | SN75401 | SN75402 | SN75403 | SN75404 | NE |
| 35 V | 500 mA | 4 | YES | | SN75437 | | | NE |
| 55 V | 300 mA | 2 | – | SN75470 | | | | J, N |
| | | | | SN75471 | SN75472 | SN75473 | SN75474 | JG, P |
| | | | YES | SN75476 | SN75477 | SN75478 | SN75479 | JG, P |
| | 350 mA | 2 | YES | SN75446 | SN75447 | SN75448 | SN75449 | JG, P |
| | 500 mA | 2 | – | SN75411 | SN75412 | SN75413 | SN75414 | NE |
| | | | YES | SN75416 | SN75417 | SN75418 | SN75419 | NE |





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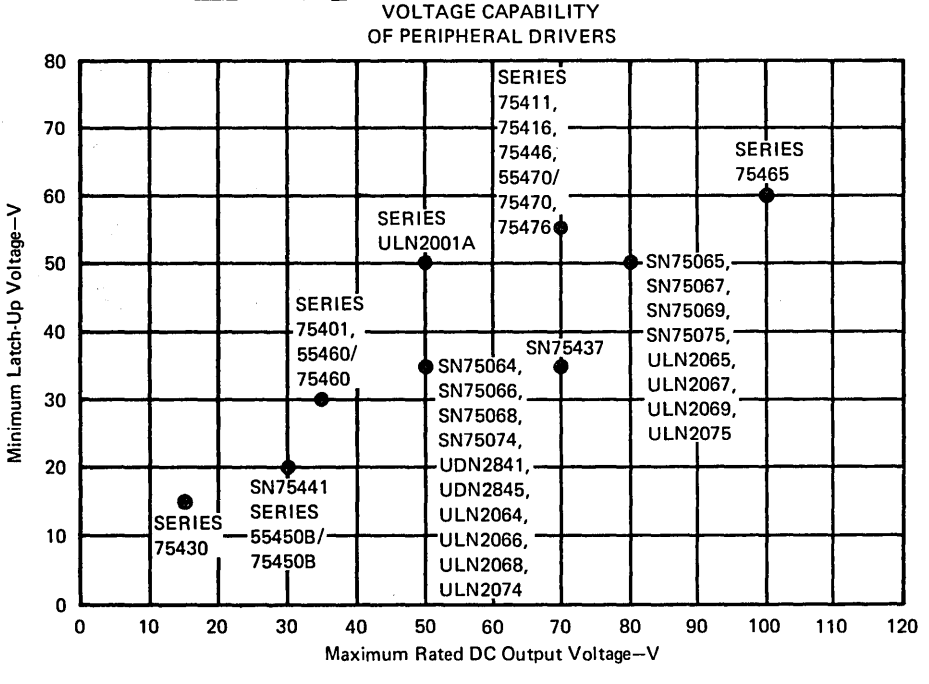
## DRIVERS WITHOUT LOGIC GATES

### Commercial Temperature Range (0°C to 70°C)

| SWITCHING VOLTAGE | MAX RECOMMENDED OUTPUT CURRENT | DRIVERS PER PACKAGE | INTERNAL CLAMP DIODES | DEVICE TYPES | | | PACKAGE OPTIONS |
|---|---|---|---|---|---|---|---|
| 35 V | 1.25 A | 4 | YES | ULN2064 | ULN2066 | ULN2068 | NE |
| | | | YES | SN75064 | SN75066 | SN75068 | NE |
| | | | – | ULN2074 | SN75074 | | NE |
| | 1.5 A | 4 | – | UDN2841 | UDN2845 | | NE |
| 50 V | 350 mA | 7 | YES | ULN2001A | ULN2002A | ULN2003A | J,N |
| | | | YES | ULN2004A | ULN2005A | | J,N |
| | 1.5 A | 4 | YES | ULN2065 | ULN2067 | ULN2069 | NE |
| | | | YES | SN75065 | SN75067 | SN75069 | NE |
| | | | – | ULN2075 | SN75075 | | NE |
| 60 V | 500 mA | 7 | YES | SN75465 | SN75466 | SN75467 | J,N |
| | | | YES | SN75468 | SN75469 | | J,N |



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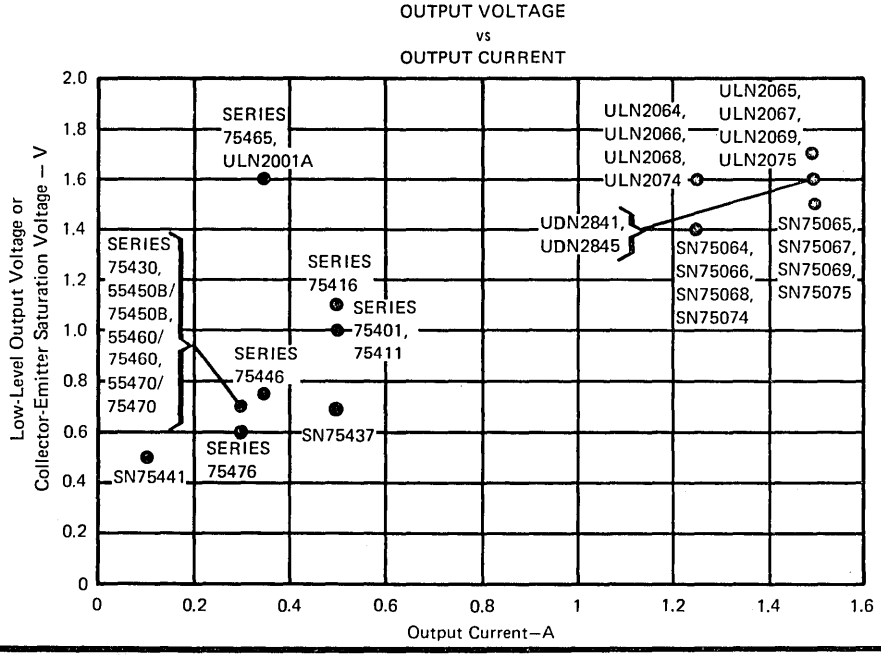
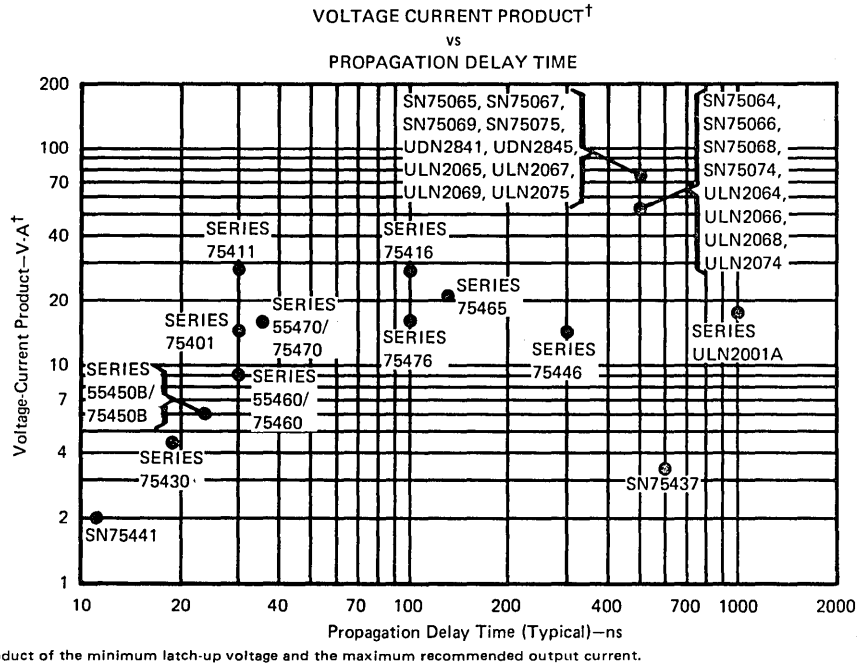
# PERIPHERAL DRIVER SELECTION GUIDE




†This is the product of the minimum latch-up voltage and the maximum recommended output current.



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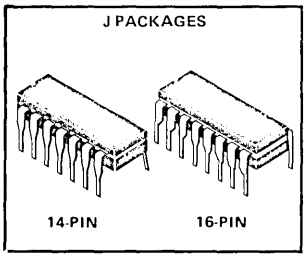
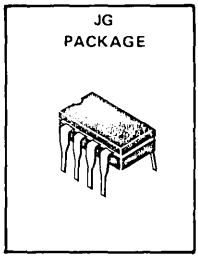
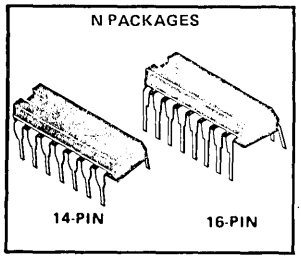
## THERMAL RESISTANCE

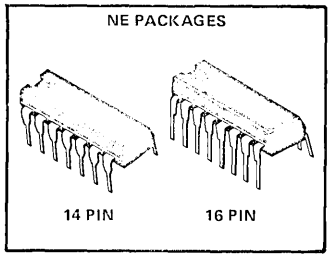
| PACKAGE | PINS | JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W) | JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W) |
|---|---|---|---|
| J ceramic dual-in-line (glass-mounted chips) | 14, 16 | 60 | 122 |
| J ceramic dual-in-line† (alloy-mounted chips) | 14, 16 | 29† | 91† |
| JG ceramic dual-in-line (glass-mounted chips) | 8 | 58 | 151 |
| JG ceramic dual-in-line† (alloy-mounted chips) | 8 | 26† | 119† |
| N plastic dual-in-line | 14, 16 | 44 | 108 |
| NE plastic dual-in-line | 14, 16 | 10 | 60 |
| P plastic dual-in-line | 8 | 45 | 125 |

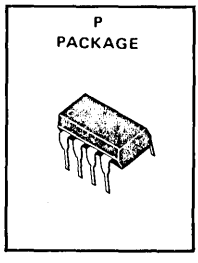
†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM," or a suffix of "/883" have alloy-mounted chips.



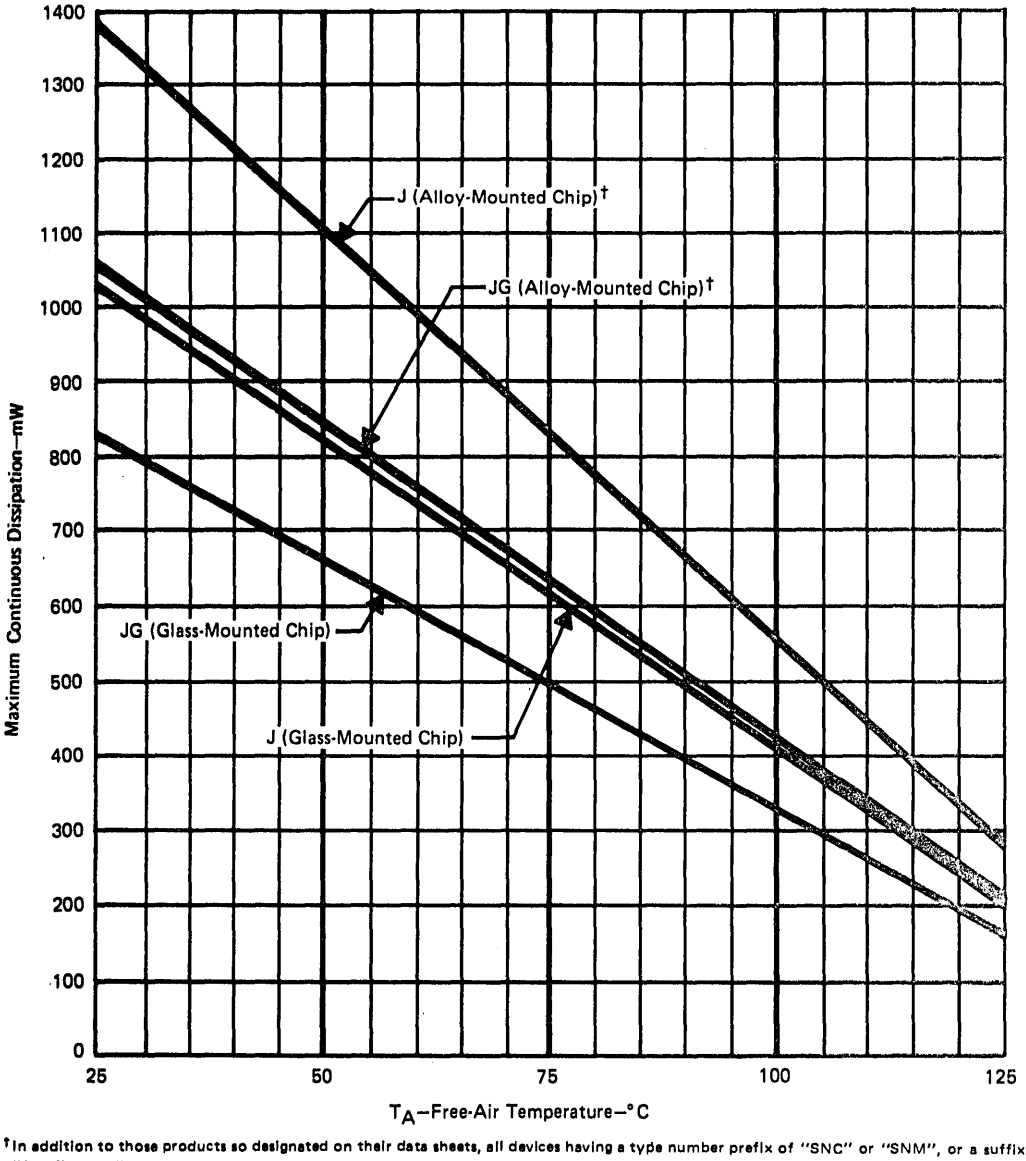



# THERMAL INFORMATION

## CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE




†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883" have alloy-mounted chips.



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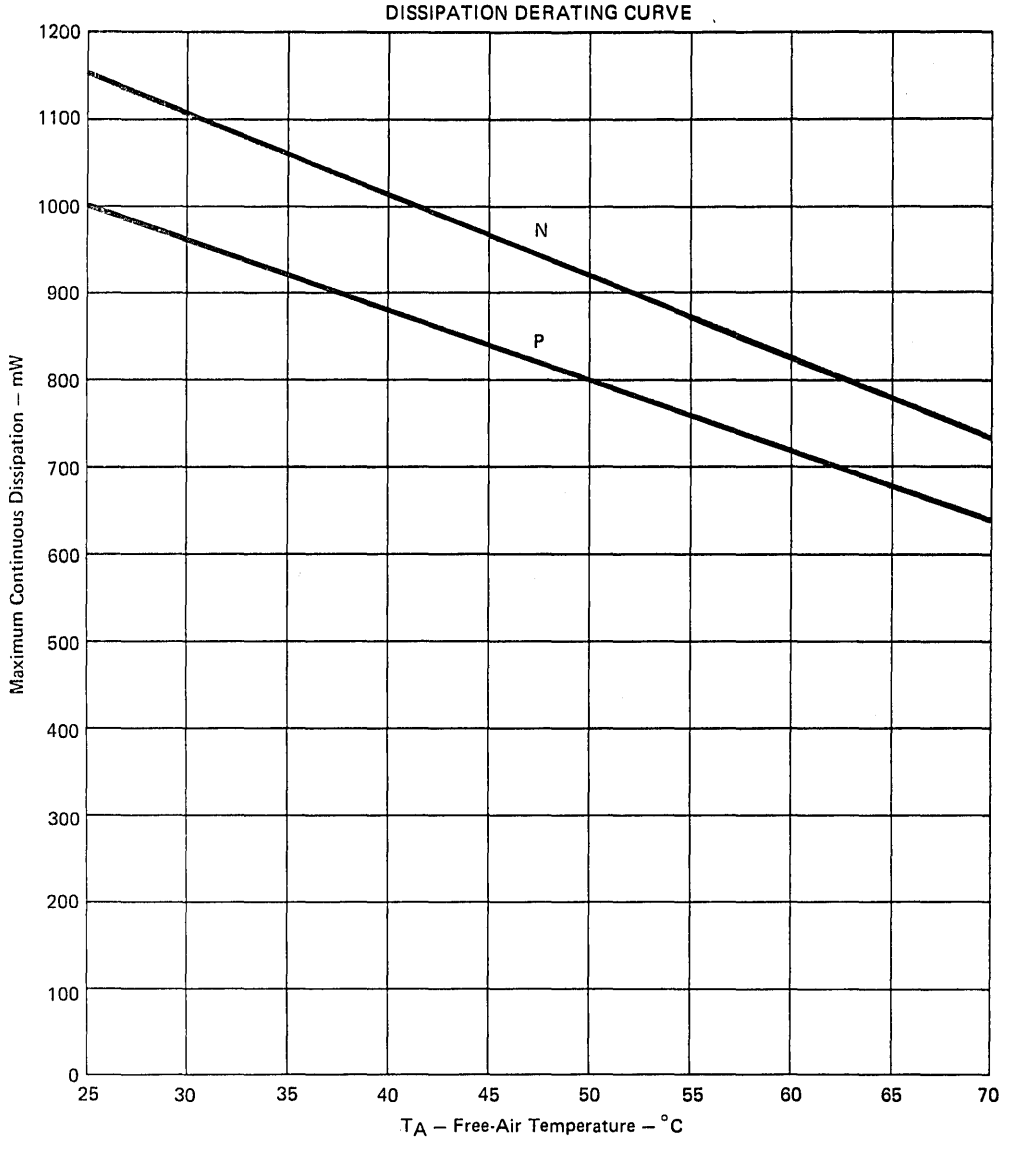
## PLASTIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.



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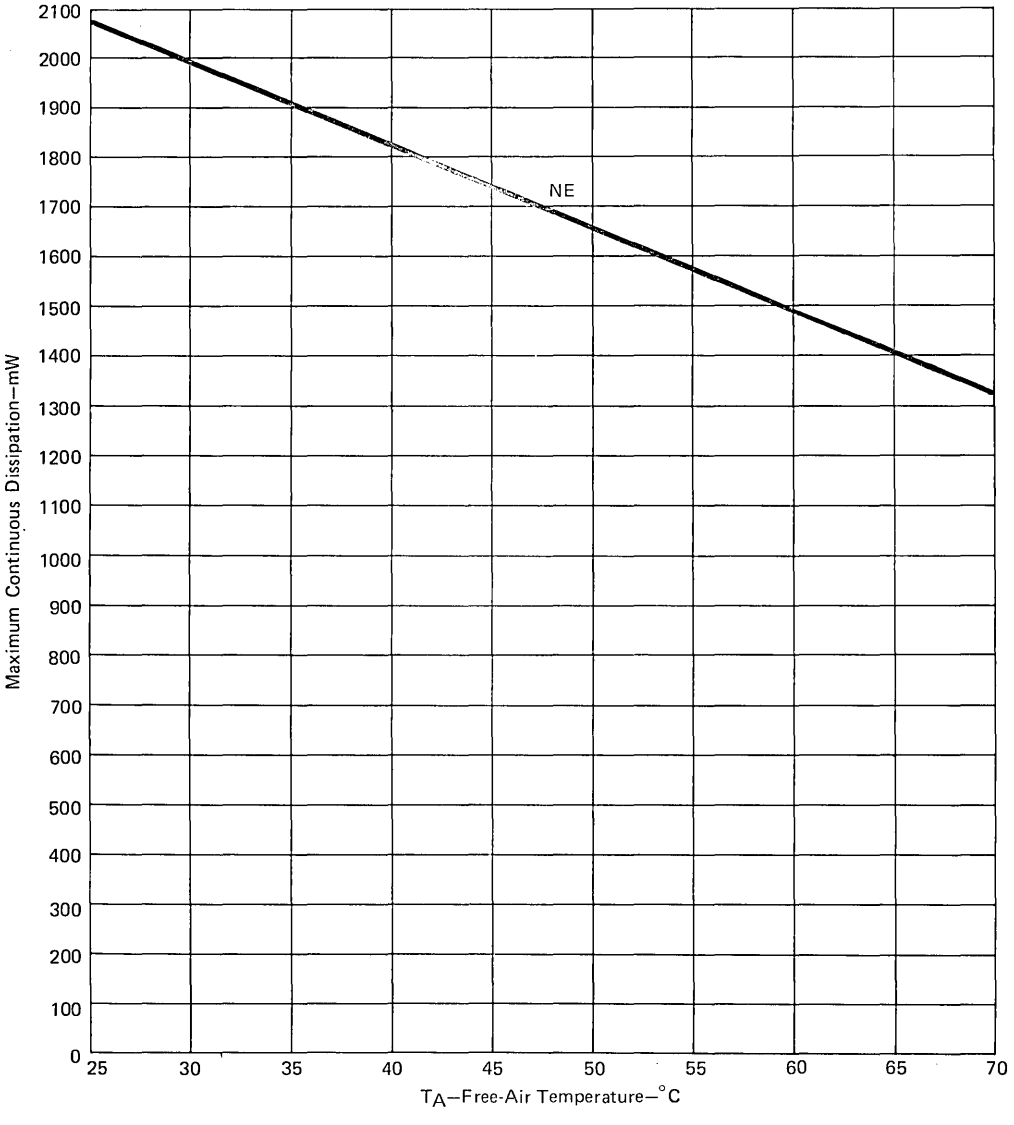
# THERMAL INFORMATION

## PLASTIC MEDIUM-POWER DUAL-IN-LINE PACKAGE

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



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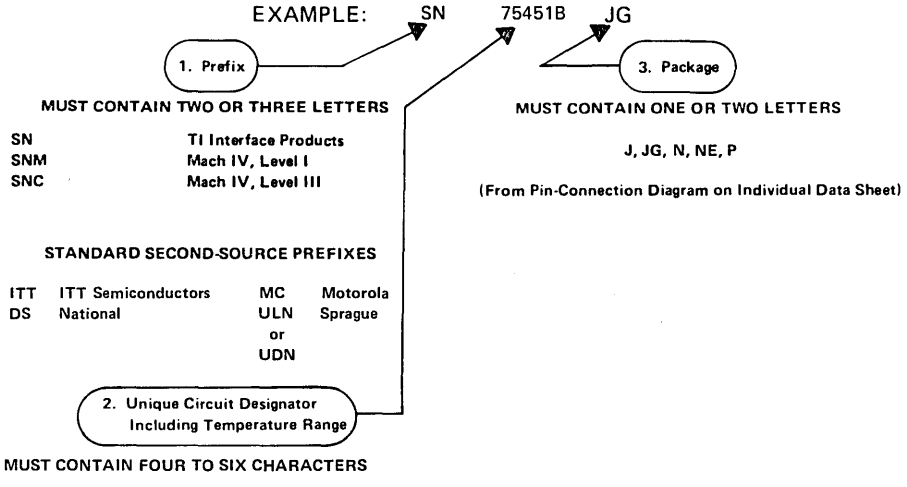
## ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book apply for the circuit type(s) listed in the page heading, unless otherwise noted, regardless of package. The availability of a circuit function in a particular package is indicated by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.




Examples: 9665
75473
75450B
2005AC

Circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

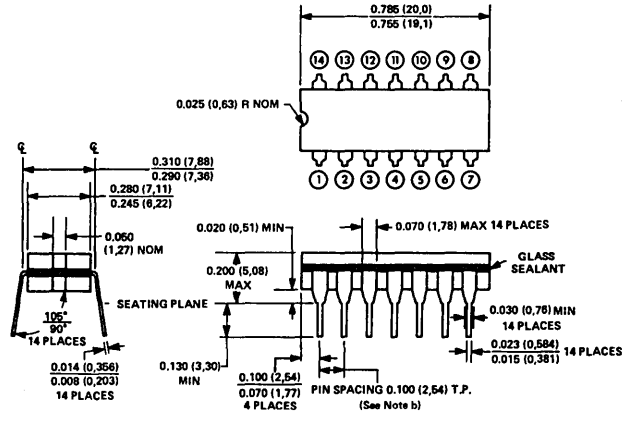
–Slide Magazines
–A-Channel Plastic Tubing
–Sectioned Cardboard Box
–Individual Plastic Box

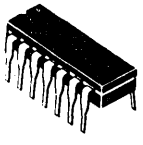
# ORDERING INSTRUCTIONS AND MECHANICAL DATA

## J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14- or 16-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

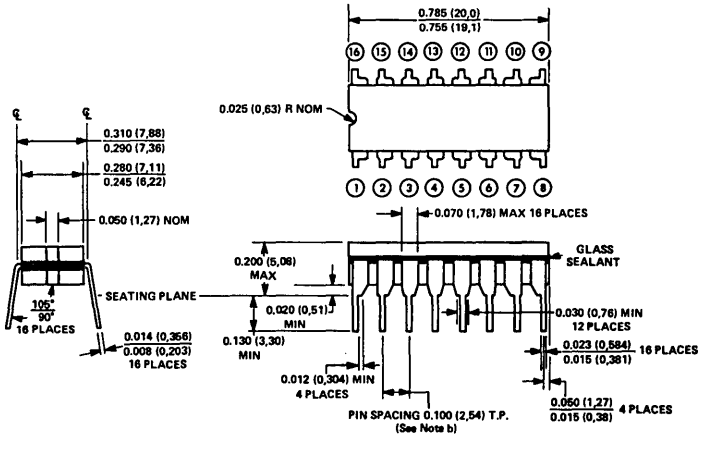
**14-PIN J CERAMIC**

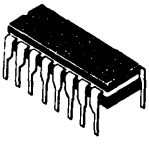


Falls within JEDEC TO-116 and MO-001AA Dimensions

**16-PIN J CERAMIC**



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.



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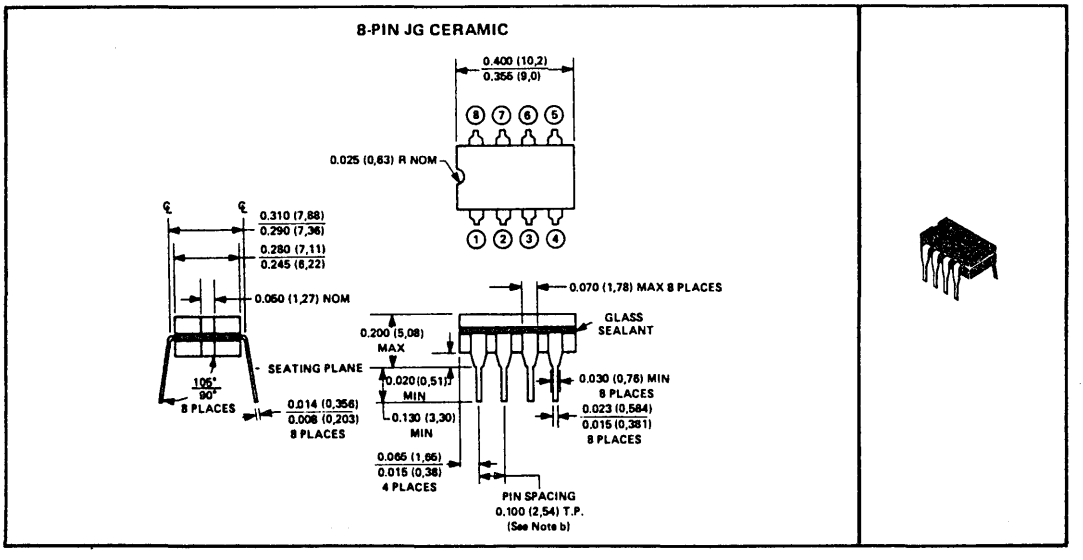
### JG ceramic dual-in-line package

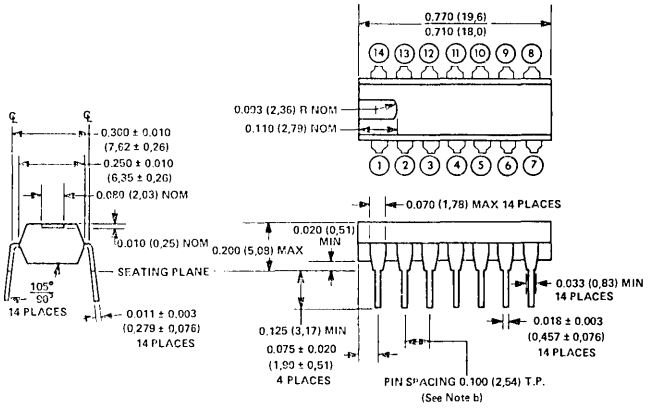
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



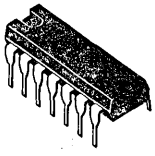
## N and NE plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14- or 16-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly. The NE package has internal metal tabs connecting the two or three central leads on each side for better heat dissipation.

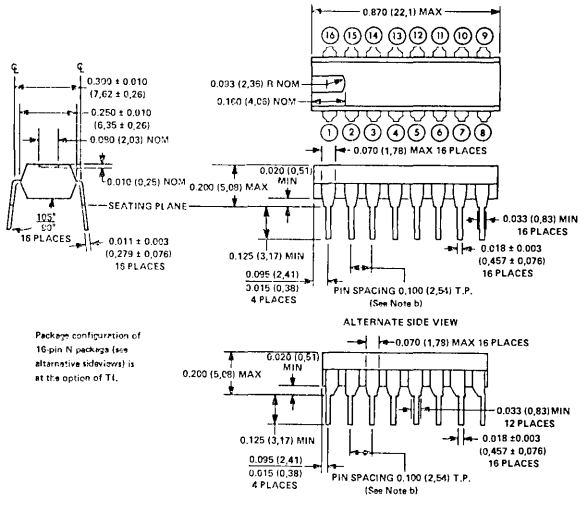
### 14-PIN N AND NE PLASTIC

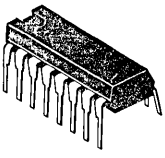



Falls Within JEDEC TO-116 and MO-001AA Dimensions



### 16-PIN N AND NE PLASTIC



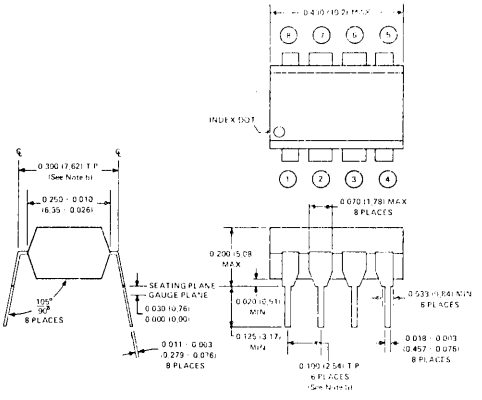
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

## P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated in an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated under high-humidity conditions. This package is intended for insertion in mounting hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

8-PIN P PLASTIC




NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is within 0.005 (0,127) radius of true position at the gauge plane with maximum material condition and unit installed.

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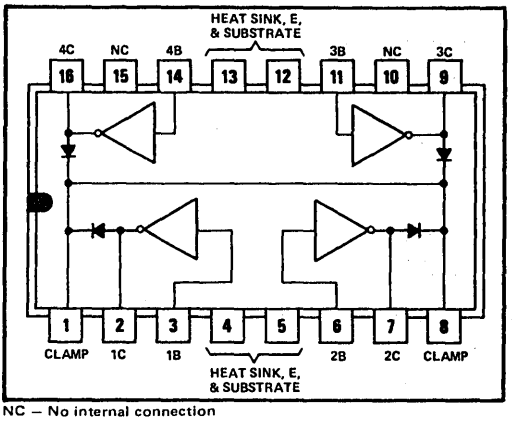
# TYPES SN75064, SN75065, SN75066, SN75067 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12788, NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- SN75064 and SN75065 Have TTL-and DTL-Compatible Inputs
- SN75066 and SN75067 Have CMOS-and PMOS-Compatible Inputs
- Improved Versions of Types ULN2064 thru ULN2067, Respectively

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



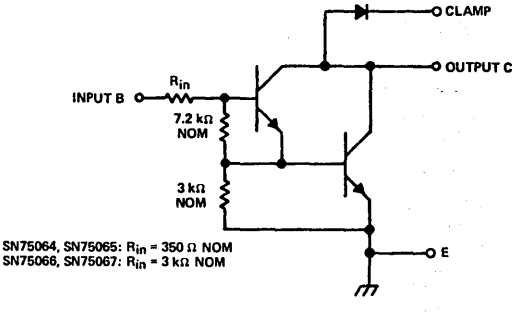

NC – No internal connection

## description

The SN75064, SN75065, SN75066, and SN75067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The SN75064 and SN75065 are intended for use with TTL, DTL, and 5-volt MOS logic. The SN75066 and SN75067 are intended for use with PMOS and higher voltage CMOS logic.

## schematic (each darlington pair)




SN75064, SN75065: $R_{in}$ = 350 Ω NOM
SN75066, SN75067: $R_{in}$ = 3 kΩ NOM

The SN75064 thru SN75067 are designed for lower saturation voltages than the ULN2064 thru ULN2067. Therefore they dissipate less power at the same currents and operate cooler with a corresponding increase in reliability. They are characterized for operation from 0°C to 70°C.

## absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

| | SN75064 | SN75065 | SN75066 | SN75067 | UNIT |
|---|---|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | 50 | 80 | V |
| Input voltage (see Note 1) | 15 | 15 | 30 | 30 | V |
| Peak collector current (see Figures 11, 12, and 13) | 1.5 | 1.5 | 1.5 | 1.5 | A |
| Input current | 25 | 25 | 25 | 25 | mA |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 2075 | 2075 | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | –55 to 150 | –55 to 150 | –55 to 150 | –55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

1180

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75064 | | SN75065 | | SN75066 | | SN75067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | 2 | 4.3 | 2 | 4.3 | | | | | mA |
| | | | $V_I$ = 3.75 V | 4.5 | 9.6 | 4.5 | 9.6 | | | | | |
| | | | $V_I$ = 5 V | | | | | 0.9 | 1.8 | 0.9 | 1.8 | |
| | | | $V_I$ = 12 V | | | | | 2.75 | 5.2 | 2.75 | 5.2 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1 A | | 2 | | 2 | | 6.5 | | 6.5 | V |
| | | | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 3 | | 2.5 | | 2.5 | | 10 | | 10 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.1 | | 1.1 | | 1.1 | | 1.1 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.2 | | 1.2 | | 1.2 | | 1.2 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.3 | | 1.3 | | 1.3 | | 1.3 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | | 1.4 | | | | 1.4 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | | 1.5 | | | | 1.5 | |
| $I_R$ | Clamp-diode reverse current | 6 | $V_R$ = 50 V | | 50 | | | | 50 | | | μA |
| | | | $V_R$ = 50 V, $T_A$ = 70°C | | 100 | | | | 100 | | | |
| | | | $V_R$ = 80 V | | | | 50 | | | | 50 | |
| | | | $V_R$ = 80 V, $T_A$ = 70°C | | | | 100 | | | | 100 | |
| $V_F$ | Clamp-diode forward voltage | 7 | $I_F$ = 1 A | | 1.75 | | 1.75 | | 1.75 | | 1.75 | V |
| | | | $I_F$ = 1.5 A, See Note 3 | | 2 | | 2 | | 2 | | 2 | |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. $t_w$ = 10 ms, duty cycle ≤ 10%.

## switching characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 8 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

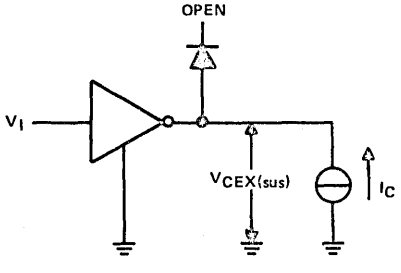



FIGURE 1–$V_{CEX(sus)}$

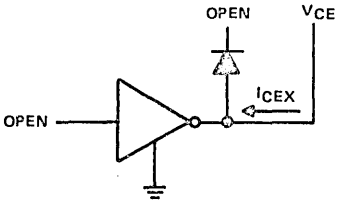



FIGURE 2–$I_{CEX}$



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## PARAMETER MEASUREMENT INFORMATION

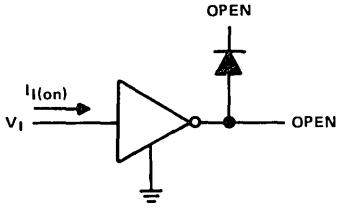



FIGURE 3–$I_{I(on)}$

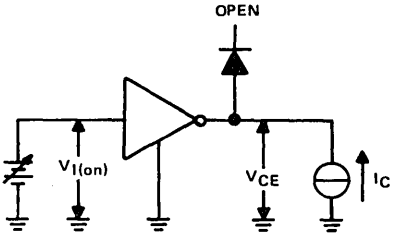



FIGURE 4–$V_{I(on)}$

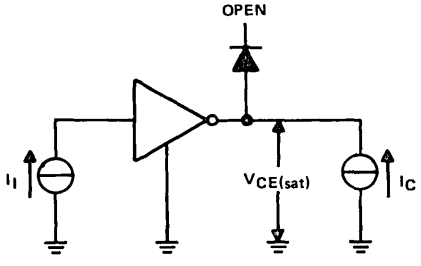



FIGURE 5–$V_{CE(sat)}$

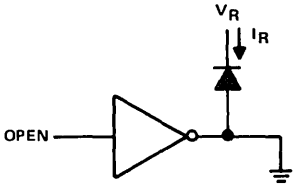



FIGURE 6–$I_R$

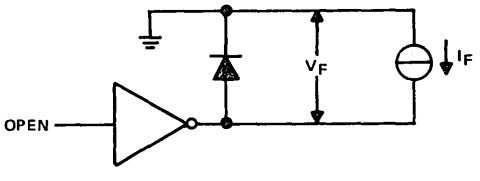
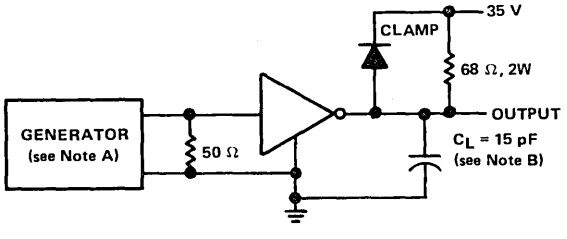
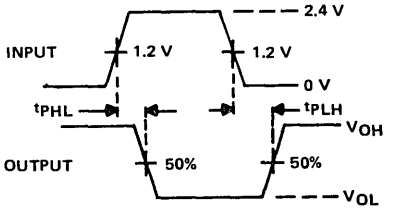



FIGURE 7–$V_F$




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_O$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 8 – SWITCHING TIMES

## ELECTRICAL CHARACTERISTICS

SN75064, SN75065
INPUT CURRENT
vs
INPUT VOLTAGE

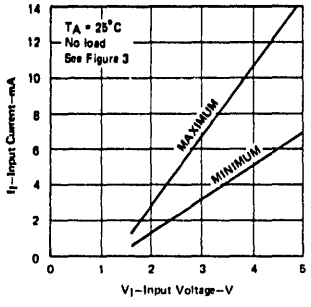



FIGURE 9

SN75066, SN75067
INPUT CURRENT
vs
INPUT VOLTAGE

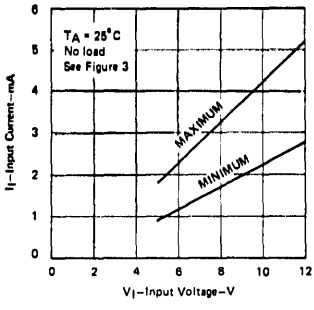



FIGURE 10

COLLECTOR CURRENT
vs
BASE CURRENT

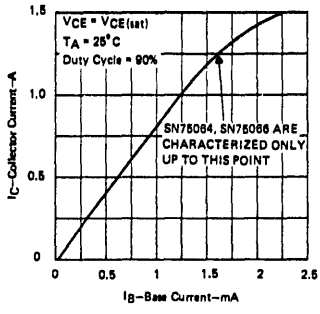



FIGURE 11

## THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

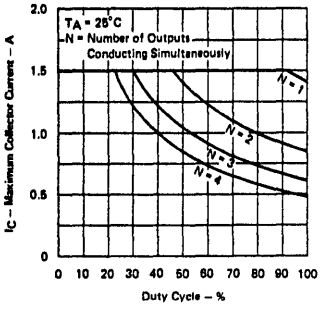



FIGURE 12

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

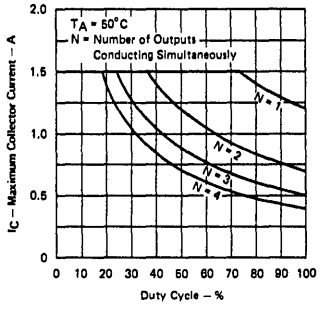



FIGURE 13

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

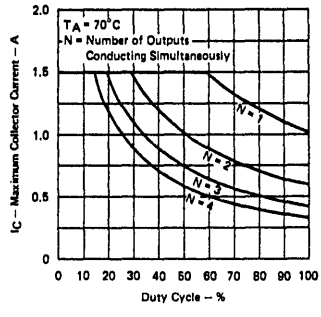



FIGURE 14

## TYPICAL APPLICATION DATA

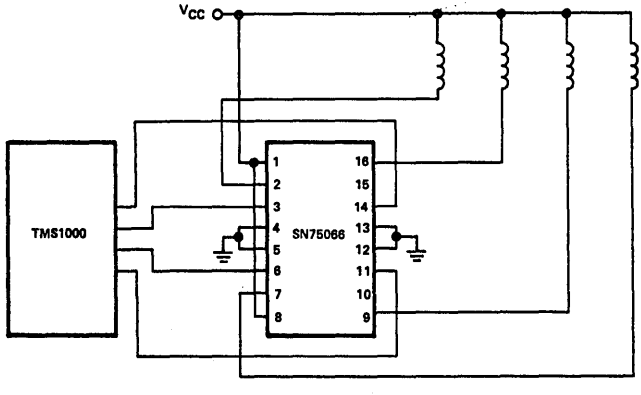



FIGURE 15 – RELAY DRIVER INTERFACE



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# UPDATE

FEBRUARY 1981

## SN75064, SN75065, SN75066, SN75067, SN75068, SN75069, SN75074, SN75075

The following changes for the ULN2064 thru ULN2069, ULN2074, and ULN2075 are being made to maintain interchangeability with other suppliers. To avoid the duplication of specifications created by these changes, the SN75064 thru SN75069, SN75074, and SN75075 are also being changed as shown below and on the following page.

**revised electrical characteristics for pages 122 and 130**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2064 ULN2074 | | ULN2065 ULN2075 | | ULN2066 | | ULN2067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.1 | | 1.1 | | 1.1 | | 1.1 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.2 | | 1.2 | | 1.2 | | 1.2 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.3 | | 1.3 | | 1.3 | | 1.3 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | | 1.4 | | | | 1.4 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | | 1.5 | | | | 1.5 | |

**revised electrical characteristics for pages 22 and 30**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75064 SN75074 | | SN75065 SN75075 | | SN75066 | | SN75067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.13 | | 1.13 | | 1.13 | | 1.13 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.25 | | 1.25 | | 1.25 | | 1.25 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.4 | | 1.4 | | 1.4 | | 1.4 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | | 1.6 | | | | 1.6 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | | 1.7 | | | | 1.7 | |

**revised electrical characteristics for page 126**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2068 | | ULN2069 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.1 | | 1.1 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.2 | | 1.2 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.3 | | 1.3 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.4 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.5 | |

**revised electrical characteristics for page 26**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75068 | | SN75069 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.13 | | 1.13 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.25 | | 1.25 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.4 | | 1.4 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.6 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.7 | |

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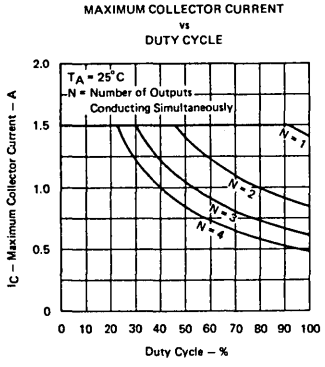
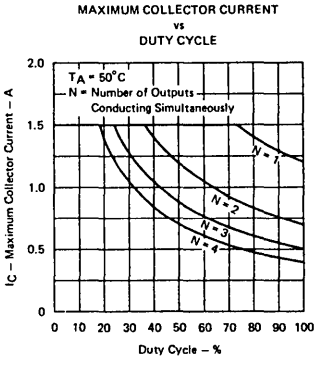
FEBRUARY 1981

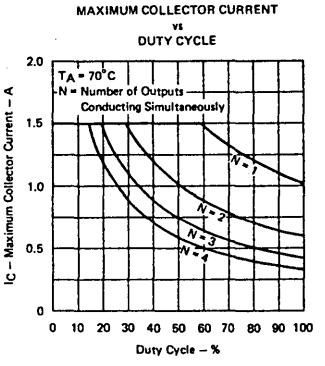
# UPDATE

(continued from previous page)

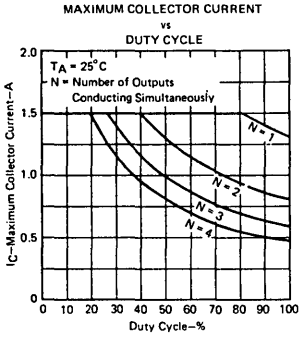
## REVISED THERMAL INFORMATION FOR ULN2064 THRU ULN2069, ULN2074, AND ULN2075
(replaces corresponding data on pages 124, 128, and 132)

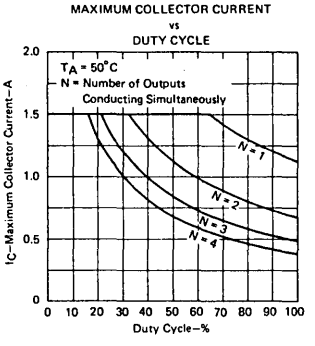


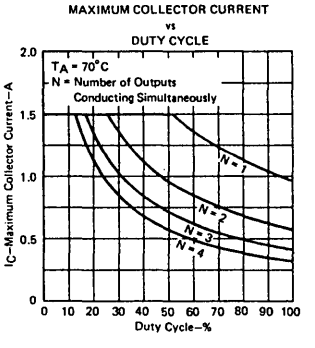




## REVISED THERMAL INFORMATION FOR SN75064 THRU SN75069, SN75074, AND SN75075
(replaces corresponding data on pages 24, 28, and 32)

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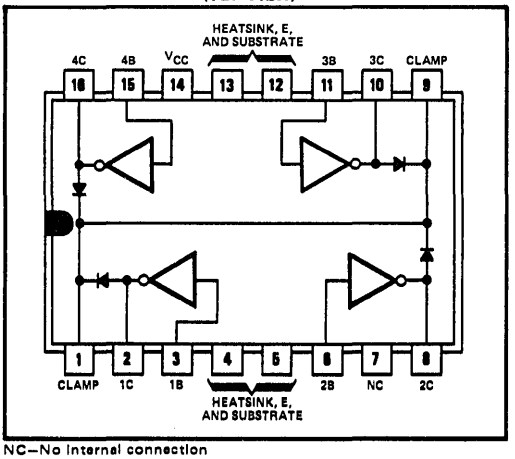
# TYPES SN75068, SN75069
# QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12789, NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible with TTL and 5-Volt CMOS
- Improved Versions of Types ULN2068 and ULN2069

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)




NC—No internal connection

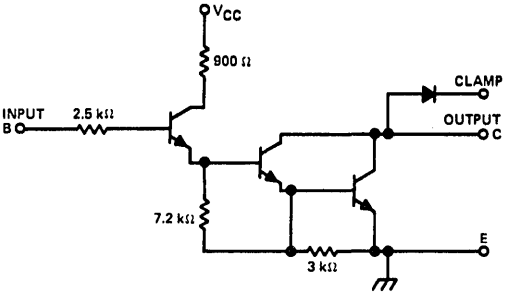
## description

The SN75068 and SN75069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-volt CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The SN75068 and SN70569 can sink up to 1.5 amperes per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge).

The SN75068 and SN75069 are designed for lower saturation voltages than the ULN2068 and ULN2069. Therefore they dissipate less power at the same currents, and operate cooler with a corresponding increase in reliability. They are characterized for operation from 0°C to 70°C.

## schematic (each switch)




Resistor values shown are nominal.

## absolute maximum ratings at 25° C free-air temperature for each switch (unless otherwise noted)

| | SN75068 | SN75069 | UNIT |
|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | V |
| Supply voltage, $V_{CC}$ (see Note 1) | 10 | 10 | V |
| Input voltage | 15 | 15 | V |
| Peak collector current (see Figures 10, 11, and 12) | 1.5 | 1.5 | A |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | −55 to 150 | −55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.





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## electrical characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75068 MIN | SN75068 MAX | SN75069 MIN | SN75069 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | | 250 | | 250 | μA |
| | | | $V_I$ = 3.75 V | | 1000 | | 1000 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 3 | | 2.4 | | 2.4 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.1 | | 1.1 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.2 | | 1.2 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.3 | | 1.3 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.4 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.5 | |
| $I_R$ | Clamp-diode reverse current | 6 | $V_R$ = 50 V | | 50 | | | μA |
| | | | $V_R$ = 50 V, $T_A$ = 70°C | | 100 | | | |
| | | | $V_R$ = 80 V | | | | 50 | |
| | | | $V_R$ = 80 V, $T_A$ = 70°C | | | | 100 | |
| $V_F$ | Clamp-diode forward voltage | 7 | $I_F$ = 1 A | | 1.75 | | 1.75 | V |
| | | | $I_F$ = 1.5 A, See Note 3 | | 2 | | 2 | |
| $I_{CC}$ | Supply current (only one switch conducting) | 8 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 6 | | 6 | mA |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. $t_w$ = 10 ms, duty cycle ≤ 10%.

## switching characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 9 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

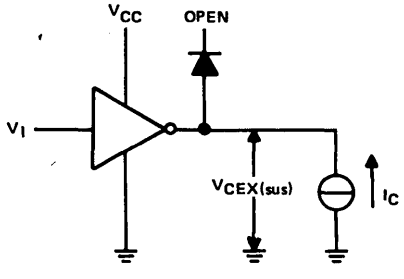


FIGURE 1–$V_{CEX(sus)}$

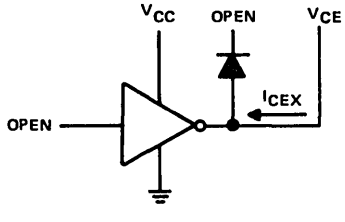


FIGURE 2–$I_{CEX}$



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## PARAMETER MEASUREMENT INFORMATION

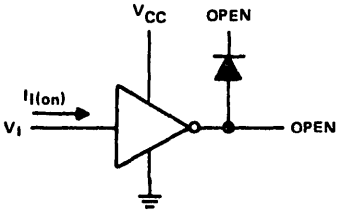



FIGURE 3–$I_{I(on)}$

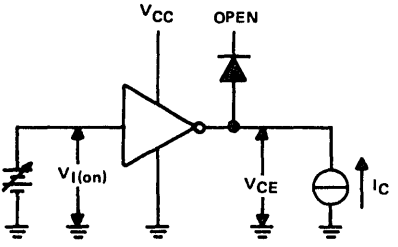



FIGURE 4–$V_{I(on)}$

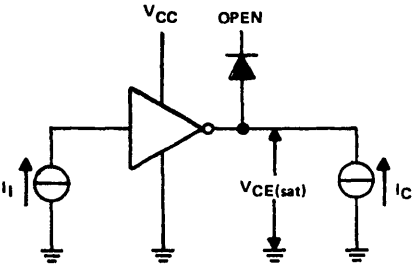



FIGURE 5–$V_{CE(sat)}$

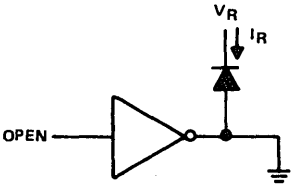



FIGURE 6–$I_R$

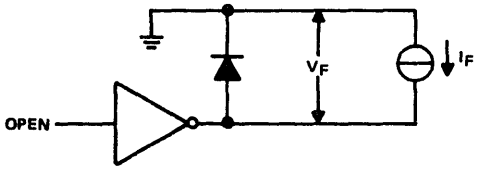



FIGURE 7–$V_F$

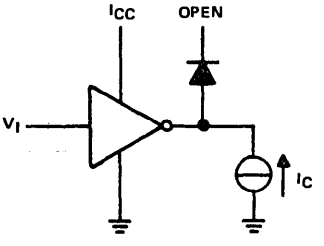
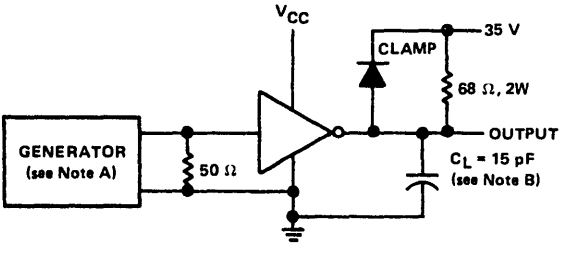
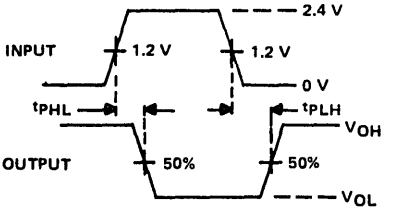



FIGURE 8–$I_{CC}$




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_o$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 9–SWITCHING TIMES

## THERMAL INFORMATION

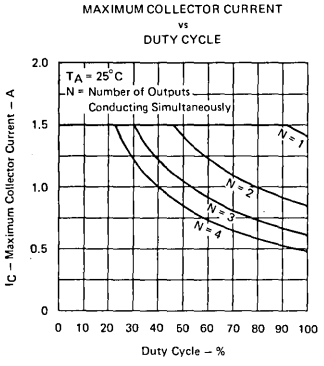



FIGURE 10

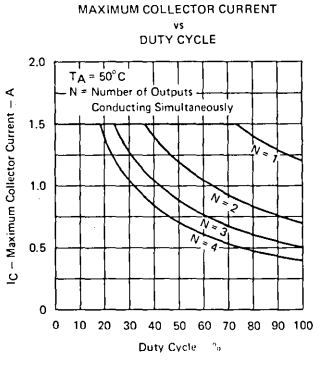



FIGURE 11

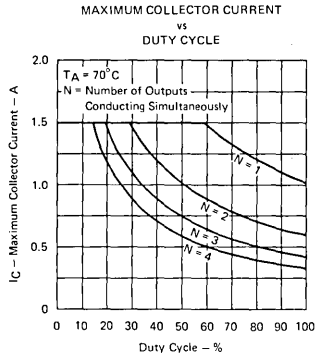



FIGURE 12

## TYPICAL APPLICATION DATA

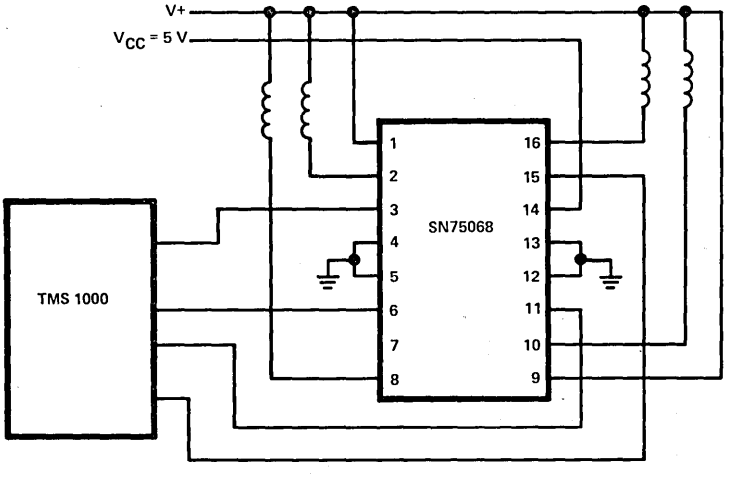



FIGURE 13–RELAY DRIVER INTERFACE



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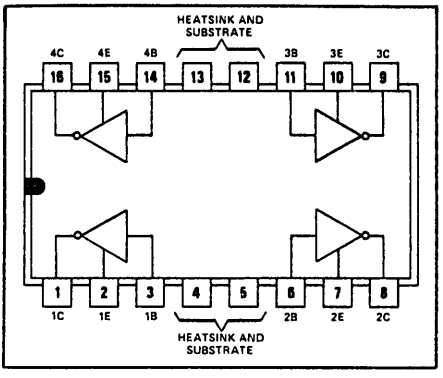
# TYPES SN75074, SN75075
# QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12792, NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible With TTL or 5-V CMOS
- Improved Versions of Types ULN2074 and ULN2075

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



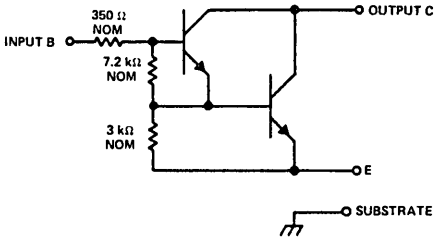

## description

The SN75074 and SN75075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 amperes for each darlington pair.

The SN75074 and SN75075 are unique general purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

The SN75074 and SN75075 are designed for lower saturation voltages than the ULN2074 and ULN2075, therefore they dissipate less power at the same currents, and operate cooler with a corresponding increase in reliability. They are characterized for operation from 0°C to 70°C.

## schematic (each switch)




## absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

| | ULN2074 | ULN2075 | UNIT |
|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | V |
| Input voltage with respect to substrate | 30 | 60 | V |
| Peak collector current (see Figures 9, 10, and 11) | 1.5 | 1.5 | A |
| Input current | 25 | 25 | mA |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 1) | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | −55 to 150 | −55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | °C |

NOTE 1: For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.





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## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75074 MIN | SN75074 MAX | SN75075 MIN | SN75075 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | 2 | 4.3 | 2 | 4.3 | mA |
| | | | $V_I$ = 3.75 V | 4.5 | 9.6 | 4.5 | 9.6 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1 A | | 2 | | 2 | V |
| | | | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 2 | | 2.5 | | 2.5 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.1 | | 1.1 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.2 | | 1.2 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.3 | | 1.3 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 2 | | 1.4 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 2 | | | | 1.5 | |

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, $t_w$ = 10 ms, duty cycle ≤ 10%.

## switching characteristics at 25°C free-air temperature

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 6 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

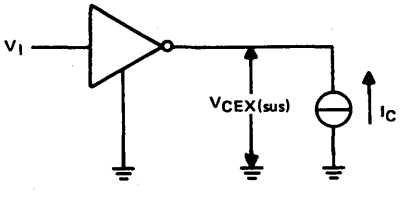



FIGURE 1–$V_{CEX(sus)}$

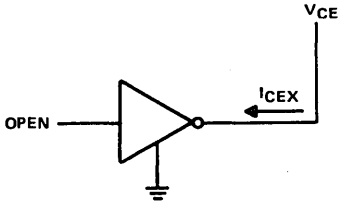



FIGURE 2–$I_{CEX}$

## PARAMETER MEASUREMENT INFORMATION

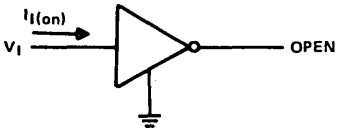



FIGURE 3–$I_{I(on)}$

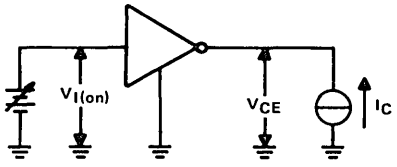



FIGURE 4–$V_{I(on)}$

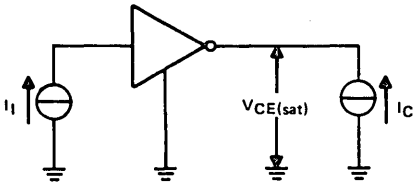
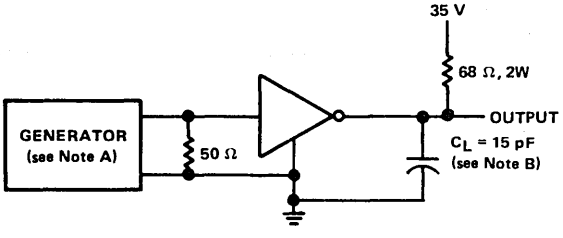
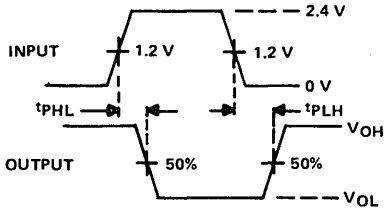



FIGURE 5–$V_{CE(sat)}$




TEST CIRCUITS




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_o$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 6–SWITCHING CHARACTERISTIC

## ELECTRICAL CHARACTERISTICS

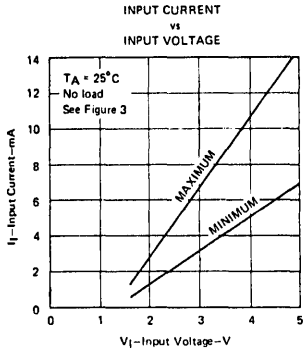



FIGURE 7

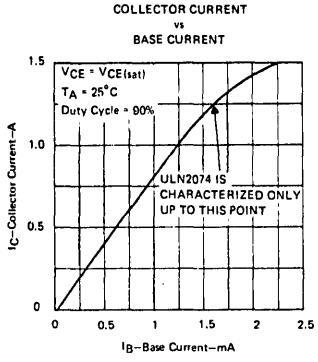



FIGURE 8

## THERMAL INFORMATION

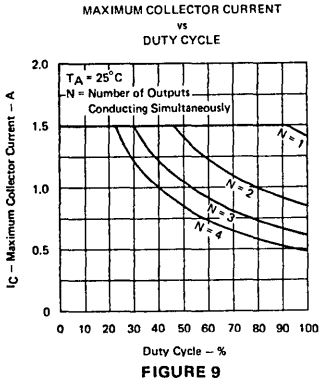



FIGURE 9

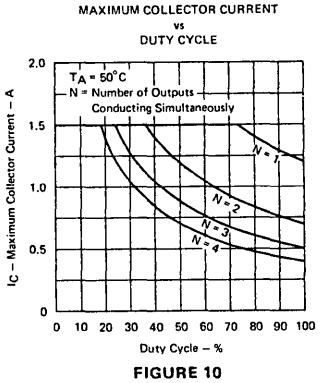



FIGURE 10

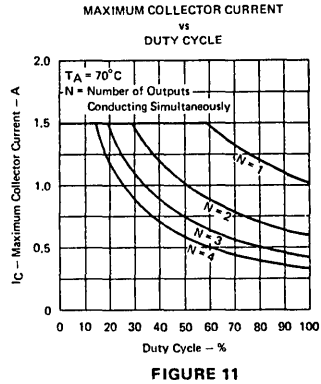



FIGURE 11

## TYPICAL APPLICATION DATA

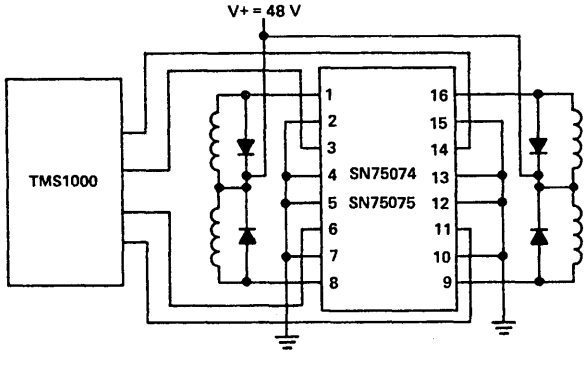



FIGURE 12–RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES



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# SERIES 75401 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12239, APRIL 1975 – REVISED DECEMBER 1976

## PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, VERY HIGH-CURRENT DRIVER APPLICATIONS

### performance

- 2-W Dissipation Rating
- Characterized for Use to 500 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

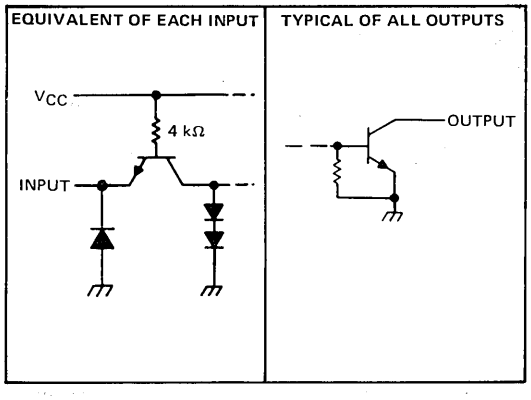
### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltage

### description

Series 75401 dual peripheral drivers are a family of versatile devices designed for use in systems that employ DTL or TTL logic. SN75401, SN75402, SN75403, and SN75404 provide AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) and are identical to SN75461 through SN75464 except that the package allows the output current capability to be increased to 500 mA. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 75401 drivers are characterized for operation from 0°C to 70°C.

### schematics of inputs and output

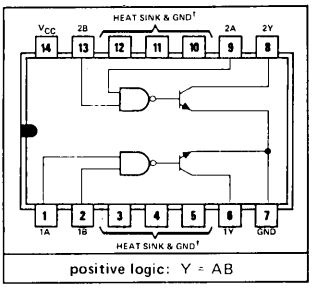



**SN75401** — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH AND DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = high-level
L = low-level



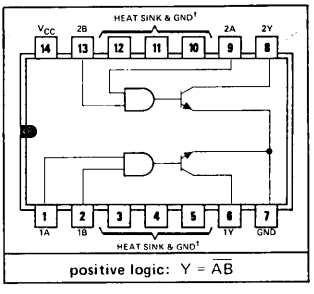

positive logic: $Y = AB$

**SN75402** — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NAND DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = high-level
L = low-level



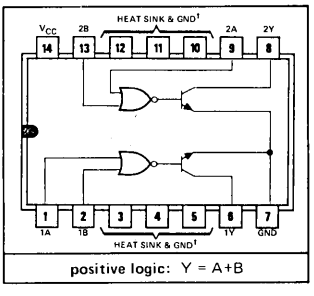

positive logic: $Y = \overline{AB}$

**SN75403** — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH OR DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = high-level
L = low-level



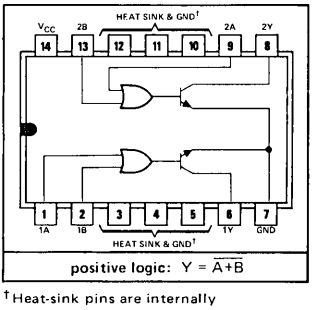

positive logic: $Y = A+B$

**SN75404** — NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NOR DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = high-level
L = low-level




positive logic: $Y = \overline{A+B}$

† Heat-sink pins are internally connected to pin 7.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Off-state output voltage | 35 V |
| Continuous output current (see Note 3) | 550 mA |
| Peak output current ($t_w \leq 10$ ms, duty cycle $\leq 40\%$, see Note 3) | 1000 mA |
| Continuous total power dissipation at (or below) 30°C free-air temperature (see Note 4) | 2 W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1/16 inch from case for 10 seconds | 260°C |

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
4. For operation above 30°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 11.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.75 V, | $I_I$ = −12 mA | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $V_{OH}$ = 35 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 100 mA | | 0.15 | 0.4 | V |
| | | | | $I_{OL}$ = 300 mA | | 0.36 | 0.7 | |
| | | | | $I_{OL}$ = 500 mA | | 0.5 | 1 | |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = 5.25 V, | $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | SN75401 | $V_{CC}$ = 5.25 V | $V_I$ = 5 V | | 8 | 11 | mA |
| | | SN75402 | | $V_I$ = 0 | | 13 | 17 | |
| | | SN75403 | | $V_I$ = 5 V | | 8 | 11 | |
| | | SN75404 | | $V_I$ = 0 | | 14 | 19 | |
| $I_{CCL}$ | Supply current, outputs low | SN75401 | $V_{CC}$ = 5.25 V | $V_I$ = 0 | | 61 | 76 | mA |
| | | SN75402 | | $V_I$ = 5 V | | 65 | 76 | |
| | | SN75403 | | $V_I$ = 0 | | 63 | 76 | |
| | | SN75404 | | $V_I$ = 5 V | | 72 | 85 | |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.



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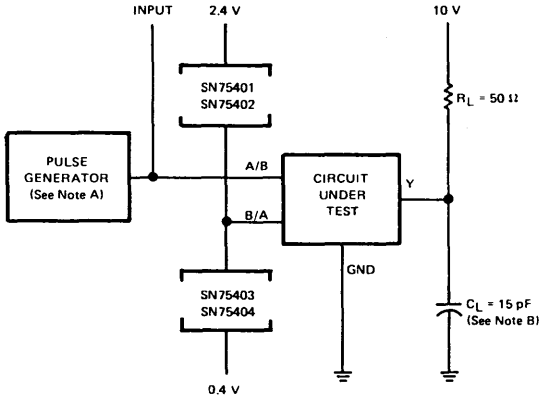
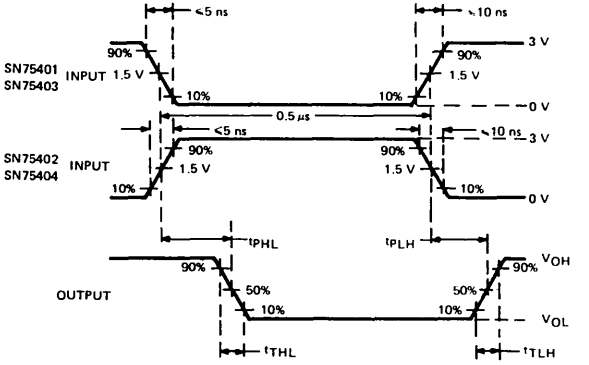
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | SN75401 | | | SN75402 | | | SN75403 | | | SN75404 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx 200$ mA, | | 30 | 55 | | 45 | 65 | | 30 | 55 | | 40 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $C_L$ = 15 pF, | | 25 | 40 | | 30 | 50 | | 25 | 40 | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | $R_L$ = 50 Ω, | | 8 | 20 | | 13 | 25 | | 8 | 25 | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | See Figure 1 | | 10 | 20 | | 10 | 20 | | 10 | 25 | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–10 | | | $V_S$–10 | | | $V_S$–10 | | | $V_S$–10 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

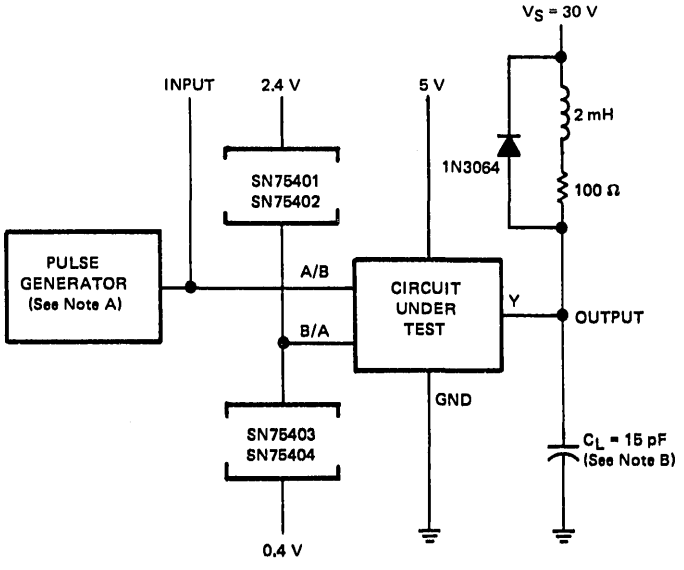



VOLTAGE WAVEFORMS

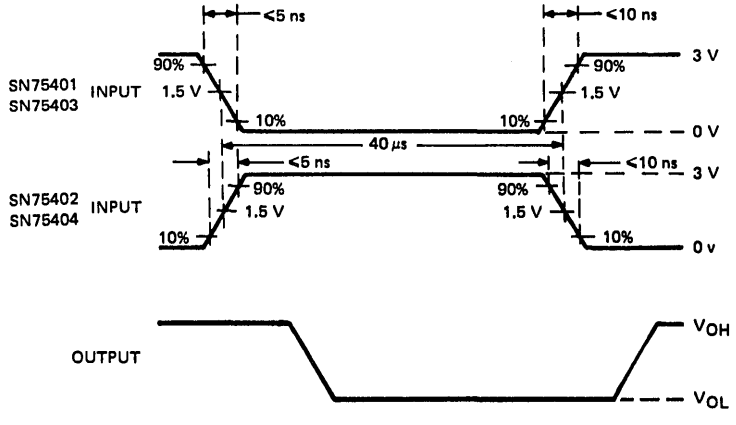
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST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# SERIES 75411
# DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12364, MARCH 1976 – REVISED DECEMBER 1976

## PERIPHERAL DRIVERS
## FOR HIGH-VOLTAGE, VERY HIGH-CURRENT DRIVER APPLICATIONS

### performance

- 2-W Dissipation Rating
- Characterized for Use to 500 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching

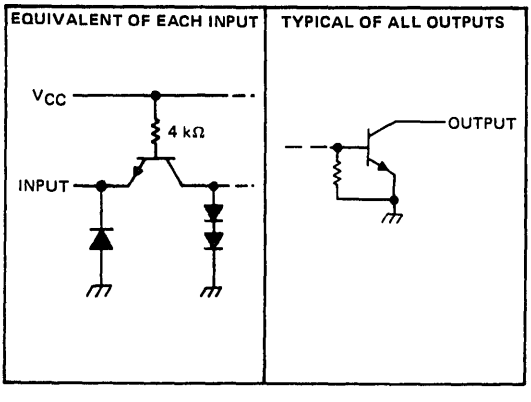
### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL or DTL Compatible Diode-Clamped Inputs
- Standard Supply Voltage

### description

Series 75411 dual peripheral drivers are a family of versatile devices designed for use in systems that employ DTL or TTL logic. SN75411, SN75412, SN75413, and SN75414 provide AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) and are identical to SN75471 through SN75474 except that the package allows the output current capability to be increased to 500 mA. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 75411 drivers are characterized for operation from 0°C to 70°C.

### schematics of inputs and output



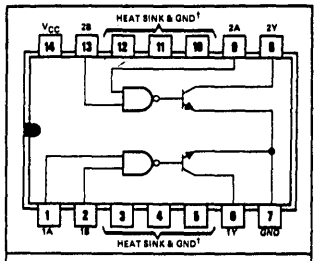

**SN75411**

FUNCTION TABLE (EACH AND DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = high-level
L = low-level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = AB

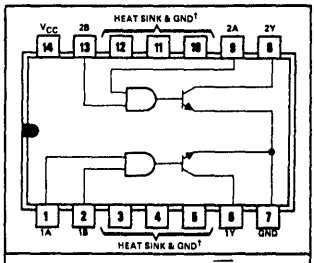
**SN75412**

FUNCTION TABLE (EACH NAND DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = high-level
L = low-level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = $\overline{AB}$

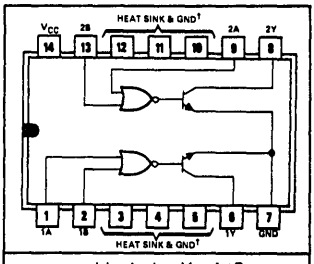
**SN75413**

FUNCTION TABLE (EACH OR DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = high-level
L = low-level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = A+B

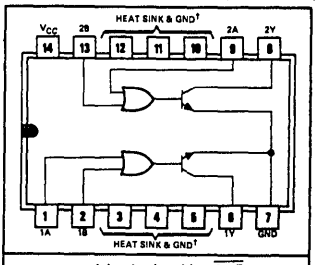
**SN75414**

FUNCTION TABLE (EACH NOR DRIVER)

| INPUTS A | INPUTS B | OUTPUT Y |
|---|---|---|
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = high-level
L = low-level

NE DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = $\overline{A+B}$

†Heat-sink pins are internally connected to pin 7.



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Off-state output voltage | 70 V |
| Continuous output current (see Note 3) | 550 mA |
| Peak output current ($t_w \leq 10$ ms, duty cycle $\leq 40\%$, see Note 3) | 1000 mA |
| Continuous total power dissipation at (or below) 30°C free-air temperature (see Note 4) | 2 W |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1/16 inch from case for 10 seconds | 260°C |

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
4. For operation above 30°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 11.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.75 V, | $I_I$ = −12 mA | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 100 mA | | 0.15 | 0.4 | V |
| | | | | $I_{OL}$ = 300 mA | | 0.36 | 0.7 | |
| | | | | $I_{OL}$ = 500 mA | | 0.5 | 1 | |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = 5.25 V, | $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = 5.25 V, | $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | | $V_{CC}$ = 5.25 V, | $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | SN75411 | $V_{CC}$ = 5.25 V | $V_I$ = 5 V | | 8 | 11 | mA |
| | | SN75412 | | $V_I$ = 0 | | 13 | 17 | |
| | | SN75413 | | $V_I$ = 5 V | | 8 | 11 | |
| | | SN75414 | | $V_I$ = 0 | | 14 | 19 | |
| $I_{CCL}$ | Supply current, outputs low | SN75411 | $V_{CC}$ = 5.25 V | $V_I$ = 0 | | 61 | 76 | mA |
| | | SN75412 | | $V_I$ = 5 V | | 65 | 76 | |
| | | SN75413 | | $V_I$ = 0 | | 63 | 76 | |
| | | SN75414 | | $V_I$ = 5 V | | 72 | 85 | |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.


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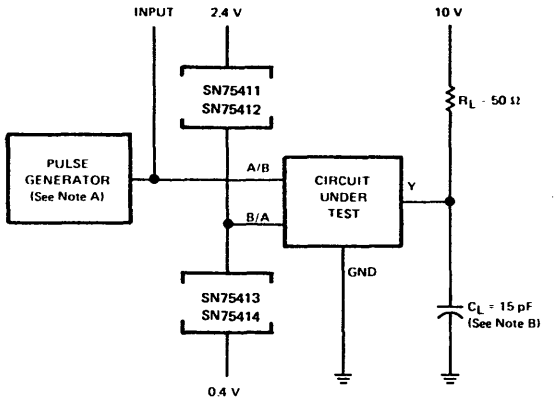
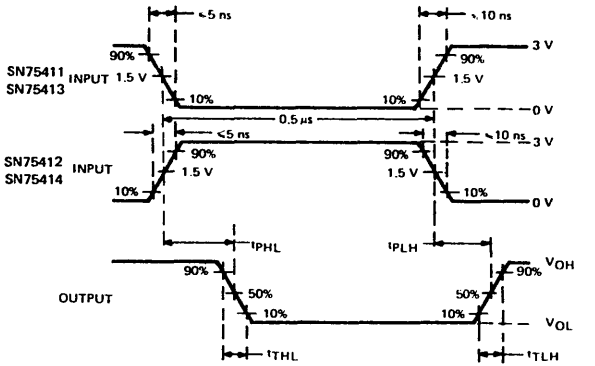
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | SN75411 | | | SN75412 | | | SN75413 | | | SN75414 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx 200$ mA, | | 30 | 55 | | 45 | 65 | | 30 | 55 | | 40 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $C_L$ = 15 pF, | | 25 | 40 | | 30 | 50 | | 25 | 40 | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | $R_L$ = 50 Ω, | | 8 | 20 | | 13 | 25 | | 8 | 25 | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | See Figure 1 | | 10 | 20 | | 10 | 20 | | 10 | 25 | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

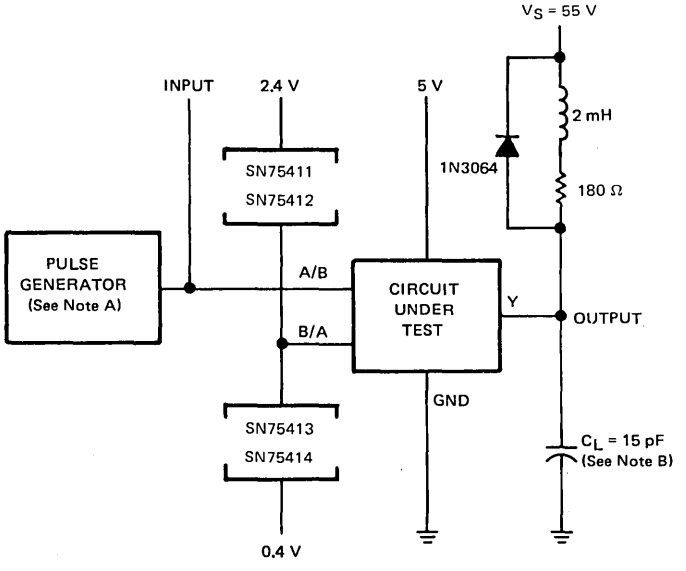



VOLTAGE WAVEFORMS

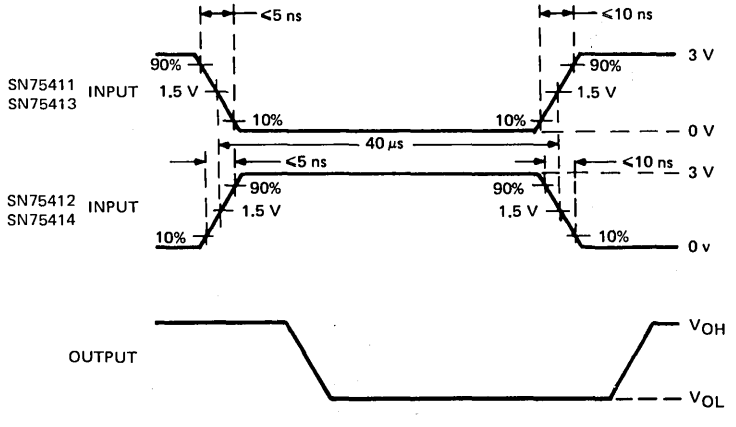
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST



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# SERIES 75416 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12481, DECEMBER 1976 – REVISED NOVEMBER 1980

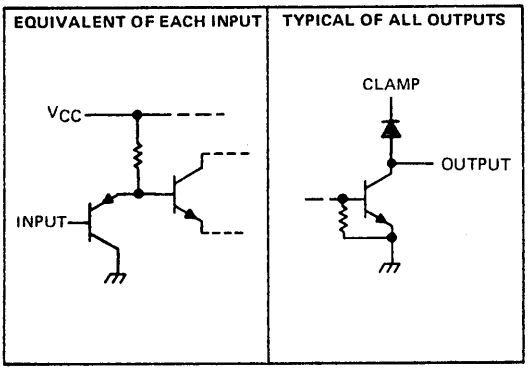
- Characterized for Use to 500 mA
- No Output Latch-Up at 55 V (After Conducting 500 mA)
- High-Voltage Outputs (100 V Typical)
- High-Speed Switching
- Output Clamp Diodes for Transient Suppression (500 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Available in the 14-Pin NE Package
- 2-Watt Power Dissipation Capability

## description

Series 75416 dual peripheral drivers are designed for use in systems that require high output voltage, high current, and fast switching times. The SN75416, SN75417, SN75418, and SN75419 provide AND , NAND, OR, and NOR functions respectively. The devices have diode-clamped inputs as well as high-current, high-voltage inductive clamp diodes on the outputs. Each device has a 2-watt power dissipation capability.

Series 75416 drivers are characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs



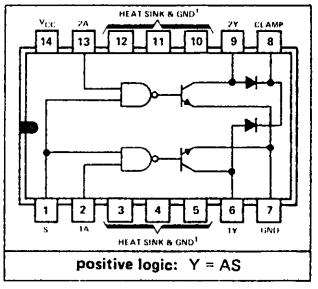

**SN75416**

NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH AND DRIVER)

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = high level
L = low level



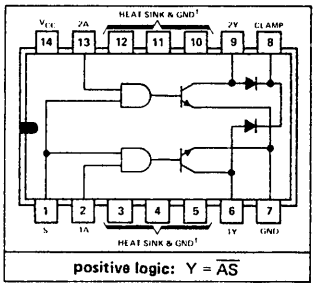

**SN75417**

NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NAND DRIVER)

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = high level
L = low level



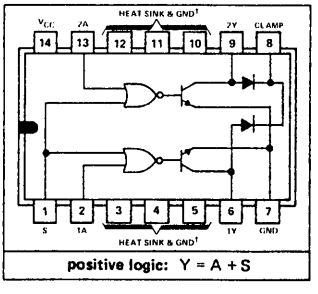

**SN75418**

NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH OR DRIVER)

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = high level
L = low level



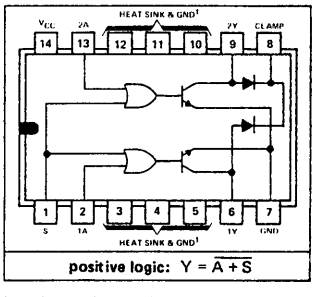

**SN75419**

NE DUAL-IN-LINE PACKAGE (TOP VIEW)

FUNCTION TABLE (EACH NOR DRIVER)

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = high level
L = low level




†Heat-sink pins are internally connected to pin 7.





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 550 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 40\%$ . . . . . 1 A
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 550 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2 W
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature | 0 | | 70 | °C |

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

3. For operation above 25°C free-air temperature, refer to Dissipation Derating curves in the Thermal Information Section, which starts on page 11.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $I_I = -12$ mA | | | −0.95 | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, | $V_{OH} = 70$ V | | 1 | 100 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, | $I_{OL} = 100$ mA | | 0.16 | 0.3 | V |
| | | | | $I_{OL} = 300$ mA | | 0.33 | 0.6 | |
| | | | | $I_{OL} = 500$ mA | | 0.5 | 1.1 | |
| $V_{(BR)O}$ | Output breakdown voltage | | $V_{CC} = 4.75$ V, | $I_{OH} = 100$ μA | 70 | 100 | | V |
| $V_{R(K)}$ | Output clamp diode reverse voltage | | $V_{CC} = 4.75$ V, | $I_R = 100$ μA | 70 | 100 | | V |
| $V_{F(K)}$ | Output clamp diode forward voltage | | $V_{CC} = 4.75$ V, | $I_F = 500$ mA | 0.8 | 1.25 | 1.6 | V |
| $I_{IH}$ | High-level input current | | $V_{CC} = 5.25$ V, | $V_I = 5.5$ V | | 0.01 | 10 | μA |
| $I_{IL}$ | Low-level input current | A input | $V_{CC} = 5.25$ V, | $V_I = 0.8$ V | | −80 | −110 | μA |
| | | Strobe S | | | | −160 | −220 | |
| $I_{CCH}$ | Supply current, outputs high | SN75416 | $V_{CC} = 5.25$ V | $V_I = 5$ V | | 20 | 35 | mA |
| | | SN75417 | | $V_I = 0$ | | 20 | 35 | |
| | | SN75418 | | $V_I = 5$ V | | 20 | 35 | |
| | | SN75419 | | $V_I = 0$ | | 20 | 35 | |
| $I_{CCL}$ | Supply current, outputs low | SN75416 | $V_{CC} = 5.25$ V | $V_I = 0$ | | 75 | 130 | mA |
| | | SN75417 | | $V_I = 5$ V | | 75 | 130 | |
| | | SN75418 | | $V_I = 0$ | | 75 | 130 | |
| | | SN75419 | | $V_I = 5$ V | | 75 | 130 | |

†All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.


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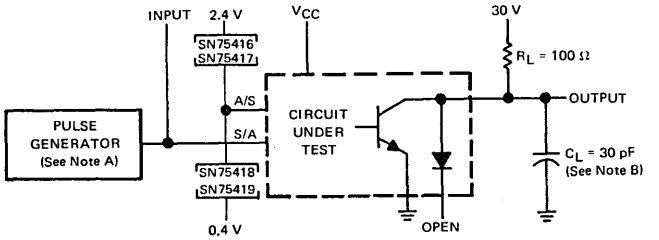
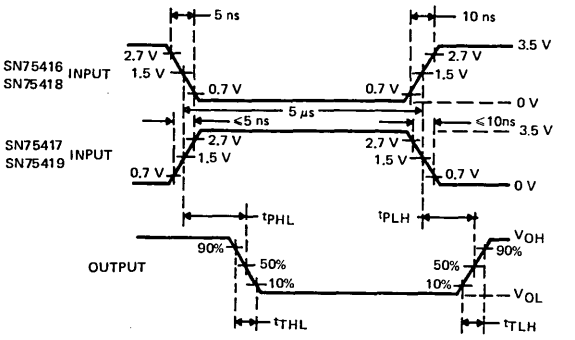
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | SN75416 | | | SN75417 | | | SN75418 | | | SN75419 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 30 pF, $R_L$ = 100 Ω, See Figure 1 | | 100 | 200 | | 100 | 200 | | 100 | 200 | | 100 | 200 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 200 | 300 | | 200 | 300 | | 200 | 300 | | 200 | 300 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O$ ≈ 500 mA, See Figure 2 | $V_S$–11 | | | $V_S$–11 | | | $V_S$–11 | | | $V_S$–11 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

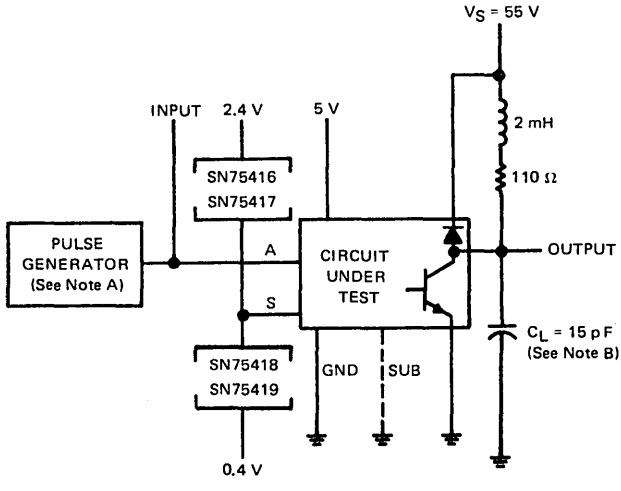



VOLTAGE WAVEFORMS

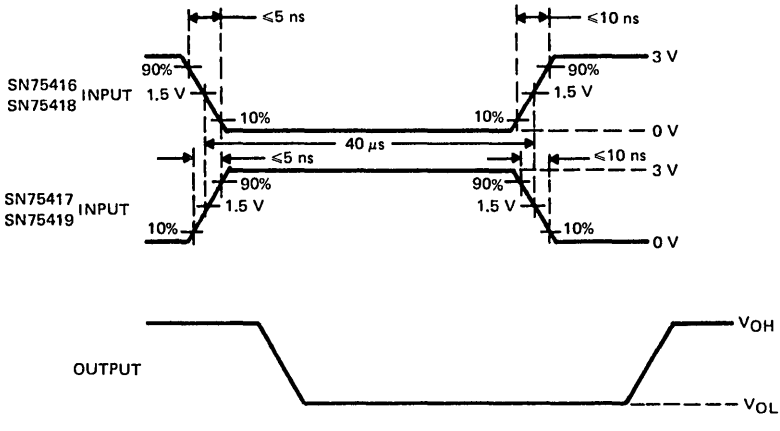
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST



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# SERIES 75430 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12367, MARCH 1976—REVISED AUGUST 1977

## PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

### performance

- Characterized for Use to 300 mA
- No Output Latch-Up at 15 V (After Conducting 150 mA)
- Very-High-Speed Switching

### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- P-N Junctions Protected by Silicon Nitride
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 75430

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---|---|---|
| SN75430 | Positive-AND† | J, N |
| SN75431 | Positive-AND | JG, P |
| SN75432 | Positive-NAND | JG, P |
| SN75433 | Positive-OR | JG, P |
| SN75434 | Positive-NOR | JG, P |

†With output transistor base connected externally to output of gate.

### description

Series 75430 dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. Diode-clamped inputs simplify circuit design. They are mechanically interchangeable with the popular Series 75450B, Series 75460, and Series 75470 peripheral drivers. Typical applications include very-high-speed logic buffers, line drivers, MOS drivers, memory drivers, and power drivers. Series 75430 drivers are characterized for operation from 0°C to 70°C.

The SN75430 is a unique general-purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. This device offers the system designer the flexibility of tailoring the circuit to the application.

The SN75431, SN75432, SN75433, and SN75434 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN75430 | SN75431 SN75432 SN75433 SN75434 | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | | 7 | 7 | V |
| Input voltage | | 5.5 | 5.5 | V |
| Interemitter voltage (see Note 2) | | 5.5 | 5.5 | V |
| $V_{CC}$-to-substrate voltage | | 15 | | V |
| Collector-to-substrate voltage | | 15 | | V |
| Collector-base voltage | | 15 | | V |
| Collector-emitter voltage (see Note 3) | | 15 | | V |
| Emitter-base voltage | | 5 | | V |
| Off-state output voltage | | | 15 | V |
| Continuous collector or output current (see Note 4) | | 400 | 400 | mA |
| Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4) | | 500 | 500 | mA |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5) | J package | 1025 | | mW |
| | JG package | | 825 | |
| | N package | 1150 | | |
| | P package | | 1000 | |
| Operating free-air temperature range | | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | | −65 to 150 | −65 to 150 | °C |
| Lead temperature 1/16 inch from case for 60 seconds | J or JG package | 300 | 300 | °C |
| Lead temperature 1/16 inch from case for 10 seconds | N or P package | 260 | 260 | °C |

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance ($R_{BE}$) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN75430 through SN75434 chips are glass-mounted.

## recommended operating conditions (see Note 6)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

NOTE 6: For the SN75430 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.





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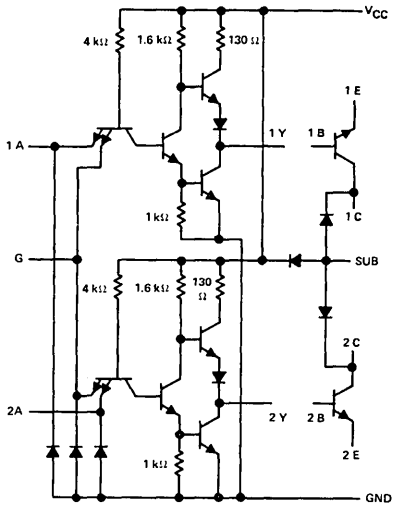
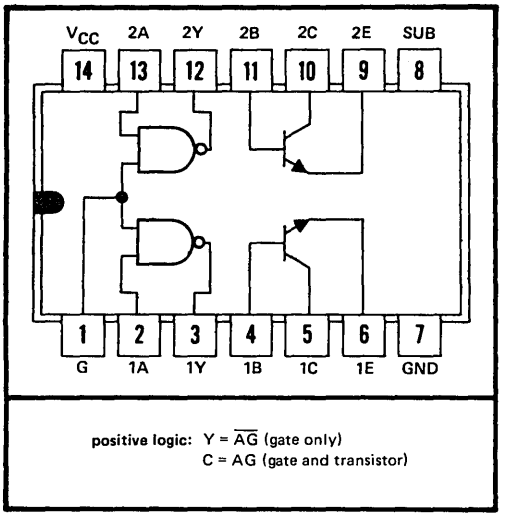
## schematic




Resistor values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

**TTL gates**

| PARAMETER | | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | 3.3 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $I_{OL}$ = 16 mA | | 0.22 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | input A | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| | | input G | | | | 2 | |
| $I_{IH}$ | High-level input current | input A | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| | | input G | | | | 80 | |
| $I_{IL}$ | Low-level input current | input A | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | | −1.6 | mA |
| | | input G | | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = 5.25 V | −18 | | −55 | mA |
| $I_{CCH}$ | Supply current, outputs high | | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 2 | 4 | mA |
| $I_{CCL}$ | Supply current, outputs low | | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 6 | 11 | mA |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### output transistors

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage | $I_C$ = 100 μA, $I_E$ = 0 | | 15 | | | V |
| $V_{(BR)CER}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 100 μA, $R_{BE}$ = 500 Ω | | 15 | | | V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | $I_E$ = 100 μA, $I_C$ = 0 | | 5 | | | V |
| $h_{FE}$ | Static Forward Current Transfer Ratio | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = 25°C | See Note 7 | 25 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = 25°C | | 30 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = 0°C | | 20 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = 0°C | | 25 | | | |
| $V_{BE}$ | Base-Emitter Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 7 | | 0.85 | 1 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 1.05 | 1.2 | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 7 | | 0.25 | 0.4 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 0.5 | 0.7 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 7: These parameters must be measured using pulse techniques. $t_w$ = 300 μs, duty cycle ≤ 2%.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

### TTL gates

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 1 | $C_L$ = 15 pF, $R_L$ = 400 Ω | | 9 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 7 | 13 | ns |

### output transistors

| PARAMETER | | TEST FIGURE | TEST CONDITIONS‡ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | 2 | $I_C$ = 100 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 7 | 14 | ns |
| $t_r$ | Rise time | | | | 10 | 19 | ns |
| $t_s$ | Storage time | | | | 7 | 15 | ns |
| $t_f$ | Fall time | | | | 6 | 15 | ns |

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

### gates and transistors combined

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 3 | $I_C$ ≈ 100 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 15 | 26 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 15 | 26 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 7 | 12 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 9 | 15 | ns |
| $V_{OH}$ | High-level output voltage after switching | 4 | $V_S$ = 15 V, $I_C$ ≈ 150 mA, $R_{BE}$ = 500 Ω | $V_S$−10 | | | mV |



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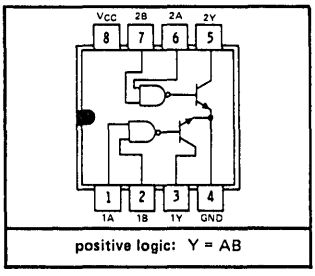
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

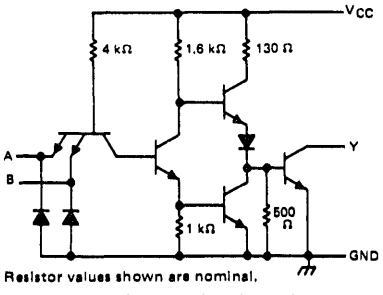
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = AB

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 V | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{OH}$ = 15 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 7 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 52 | 65 | mA |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 3 | $I_O \approx$ 100 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 10 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 17 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 8 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | 4 | $V_S$ = 15 V, $I_O \approx$ 150 mA | $V_S$−10 | | | mV |

# TYPE SN75432
# DUAL PERIPHERAL POSITIVE-NAND DRIVER

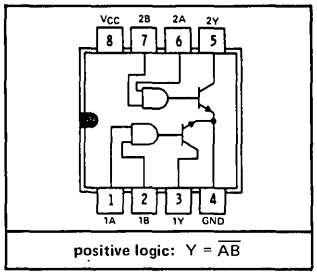
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

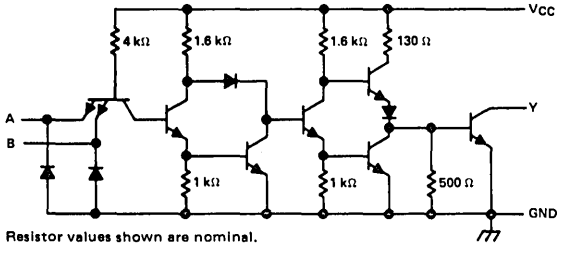
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AB}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 V | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 15 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 11 | 14 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 56 | 71 | mA |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 3 | $I_O \approx$ 100 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 15 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 19 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 8 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | 4 | $V_S$ = 15 V, $I_O \approx$ 150 mA | $V_S$−10 | | | mV |





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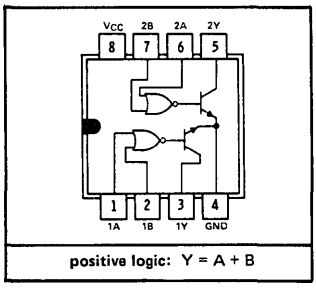
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

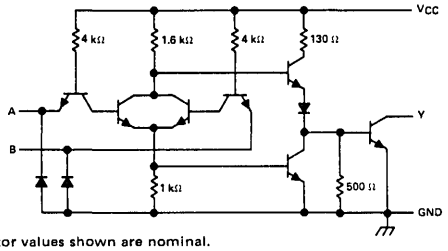
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = A + B

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 V | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{OH}$ = 15 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 54 | 68 | mA |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 3 | $I_O \approx$ 100 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 10 | 20 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 15 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 3 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 9 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | 4 | $V_S$ = 15 V, $I_O \approx$ 150 mA | $V_S$−10 | | | mV |



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# TYPE SN75434
# DUAL PERIPHERAL POSITIVE-NOR DRIVER

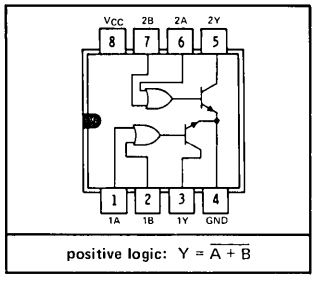
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | L (on state) |

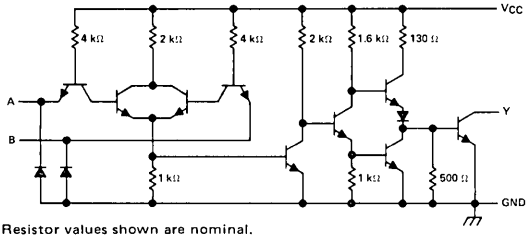
H = high level, L = low level

JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{A + B}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = −12 mA | | | −1.5 V | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 15 V | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 61 | 79 | mA |

‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | 3 | $I_O \approx$ 100 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω | | 13 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 17 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 8 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | 4 | $V_S$ = 15 V, $I_O \approx$ 150 mA | $V_S$−10 | | | mV |



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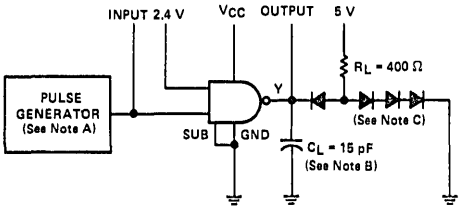
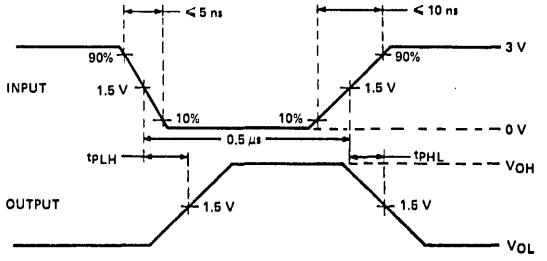
## PARAMETER MEASUREMENT INFORMATION



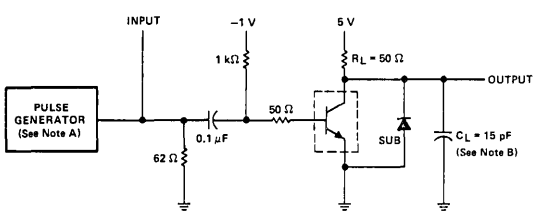

TEST CIRCUIT



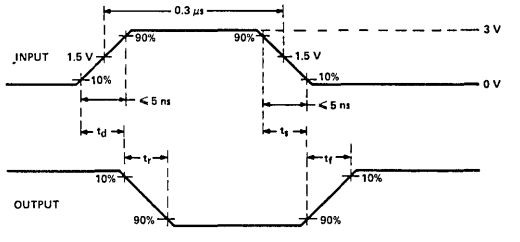

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN75430 ONLY)




TEST CIRCUIT

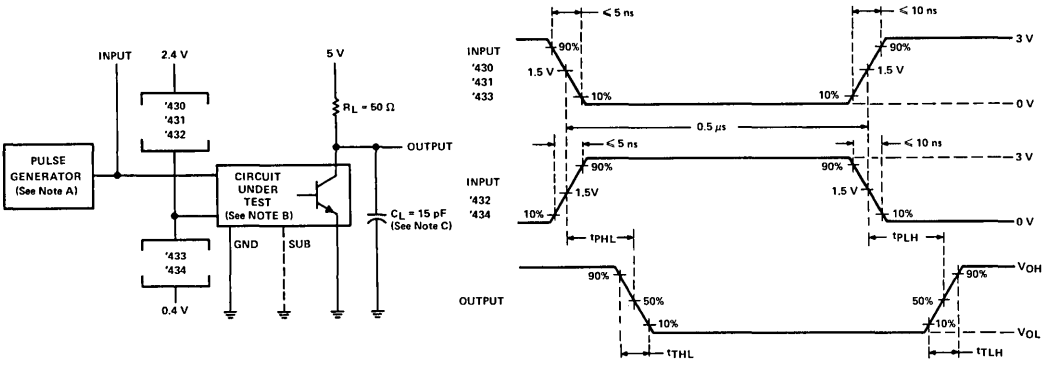



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN75430 ONLY)

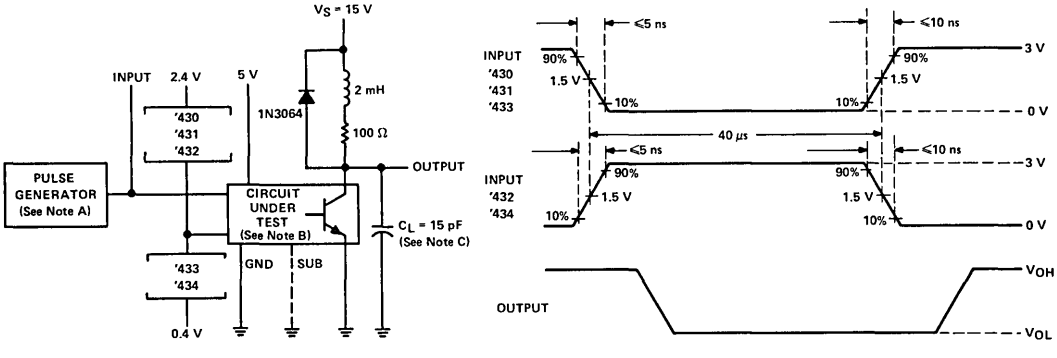
## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN75430, connect output Y to transistor base and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

**FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS**




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. When testing SN75430, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

**FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS**



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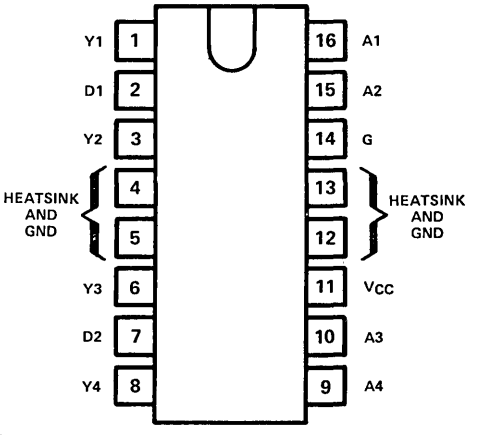
# TYPE SN75437
# QUADRUPLE PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12795, DECEMBER 1980

- Low Saturation Voltage
- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 500 mA
- No Output Latch-Up at 35 V (After Conducting 500 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (500 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- 2-W Power Package
  - Low $R_{\theta JA}$ . . . 60°C/W
  - Low $R_{\theta JC}$ . . . 10°C/W

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)




## description

The SN75437 Quad peripheral driver is designed for use in systems that require high current, high voltage, and high power. The SN75437 provides NAND drivers. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs.

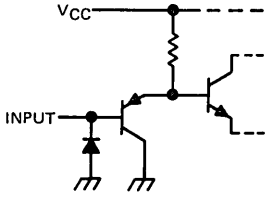
FUNCTION TABLE
(EACH NAND DRIVER)

| INPUTS | | OUTPUT |
|---|---|---|
| A | G | Y |
| L | X | H |
| X | L | H |
| H | H | L |

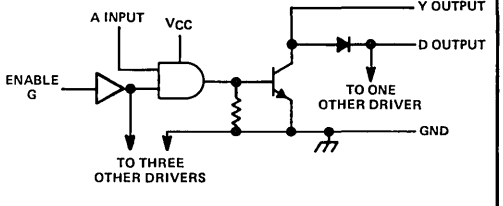
H = high level, L = low level
X = irrelevant

## schematic of inputs and functional block diagram

EQUIVALENT OF EACH INPUT




FUNCTIONAL BLOCK DIAGRAM



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 600 mA
Output clamp diode current . . . . . 600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2075 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 250°C

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

NOTES: 1. Voltage values are with respect to network ground terminal.
2. All sections of this quad circuit may conduct rated current simultaneously, however power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, | $I_I$ = 12 mA | | 0.9 | 1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | 1 | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V | $I_{OL}$ = 200 mA | | 0.15 | 0.5 | V |
| | | | $I_{OL}$ = 400 mA | | 0.30 | 0.6 | |
| | | | $I_{OL}$ = 500 mA | | 0.45 | 0.7 | |
| $V_{(BR)O}$ | Output breakdown voltage | $V_{CC}$ = 4.75 V, | $I_{OH}$ = 100 μA | 70 | 100 | | V |
| $V_{R(D)}$ | Output clamp diode reverse voltage | $V_{CC}$ = 4.75 V, | $I_R$ = 100 μA | 70 | 100 | | V |
| $V_{F(D)}$ | Output clamp diode forward voltage | $V_{CC}$ = 4.75 V, | $I_F$ = 500 mA | 0.6 | 1.2 | 1.6 | V |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, | $V_I$ = 5.25 V | | 0.01 | 10 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, | $V_I$ = 0.8 V | | −0.5 | −10 | μA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, | $V_I$ = 0 | | 40 | 65 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, | $V_I$ = 5 V | | 40 | 65 | mA |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| | PARAMETER¶ | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 30 pF, See Figure 1 | $R_L$ = 60 Ω, | | 750 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 750 | | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 200 | | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 200 | | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 35 V, See Figure 2 | $I_O \approx$ 500 mA, | $V_S$−10 | | | mV |


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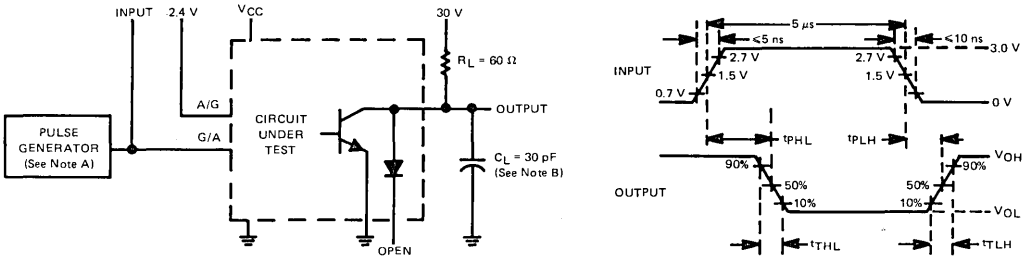
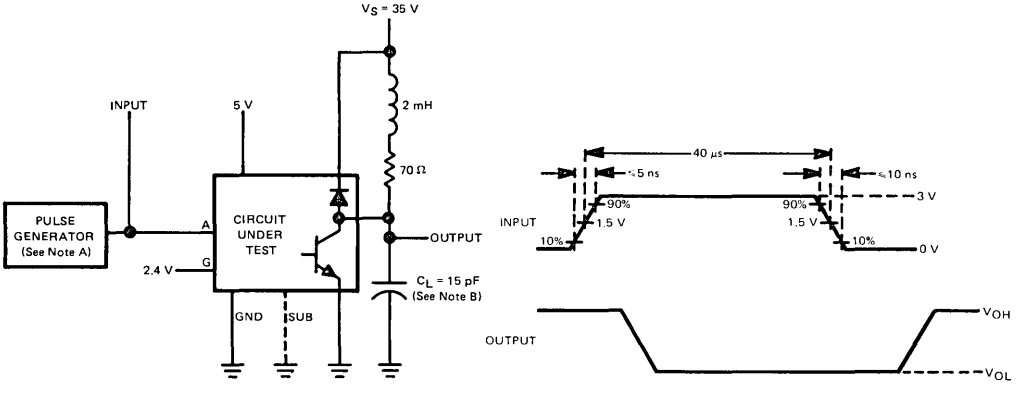
## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

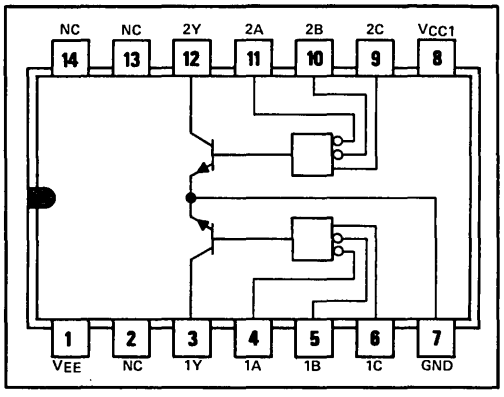
FIGURE 2–LATCH-UP TEST

# TYPE SN75441
# DUAL ECL-COMPATIBLE PERIPHERAL DRIVER

BULLETIN NO. DL-S 12479, DECEMBER 1976—REVISED AUGUST 1977

- Characterized For Use To 100 mA
- No Output Latch-Up at 20 V (After Conducting 100 mA)
- High-Speed Switching
- Positive OR Logic
- Versatile Interface Circuits for Use Between ECL and High-Current, High-Voltage Systems
- Inputs are Compatible with Series 10000 ECL and Other Similar ECL Families
- Standard Supply Voltages

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)




NC—No internal connection

## description

The SN75441 is a monolithic dual ECL-compatible peripheral driver and interface circuit. The device accepts standard input signals from ECL families and provides high-current and high-voltage output levels suitable for driving MOS and TTL circuits. Typical applications include high-speed logic buffers, line drivers, MOS drivers, and memory drivers.

The device has one in-phase and two out-of-phase ECL-compatible inputs per driver. By proper connections of the inputs, the SN75441 may be used three ways: positive-OR gate, differential ECL line receiver, or inverting gate. Some applications require one input per gate to be connected to an externally generated ECL reference voltage, $V_{BB}$.

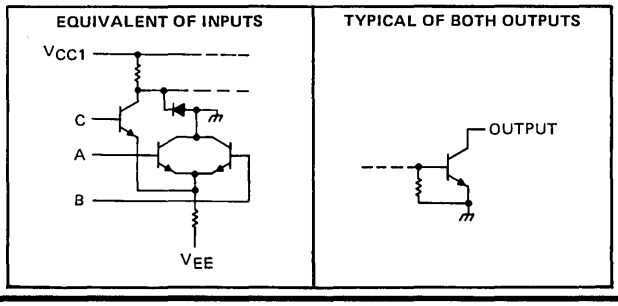
The SN75441 operates from two standard supplies, the TTL $V_{CC}$ supply and the ECL $V_{EE}$ supply, and is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| DIFFERENTIAL | LOGIC LEVEL | | | Y |
| (More positive of A or B)—C | A | B | C | |
| H ($V_{ID} \geq 150$ mV) | L | H | L | H |
| | H | L | L | |
| | H | H | L | |
| ? (−150 mV ≤ $V_{ID}$ ≤ 150 mV) | X | X | X | INDETERMINATE |
| L ($V_{ID} \leq -150$ mV) | L | L | H | L |

H = high level, L = low level, X = irrelevant
See additional function tables in Figure 3.

## schematics of inputs and outputs



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of $V_{CC}$ (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of $V_{EE}$ . . . . . −7 V to 0.5 V
Negative voltage at $V_{CC}$ with respect to $V_{EE}$ . . . . . −0.5 V
Input voltage range . . . . . −7 V to 0.5 V
Negative voltage at any input with respect to $V_{EE}$ . . . . . −1 V
Differential input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 30 V
Output current . . . . . 150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES : 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J package, the SN75441 chip is glass-mounted.

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Supply voltage, $V_{EE}$ | −4.68 | −5.2 | −5.72 | V |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## definition of input logic levels (see Note 3)

| | PARAMETER | B (Least Positive) | A (Most Positive) | UNIT |
|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage at any input | −1.5 | −0.7 | V |
| $V_{IL}$ | Low-level input voltage at any input | $V_{EE}$ | $V_{IH}$−150 mV | |
| $V_{IDH}$ | High-level differential input voltage (see Note 3) | 150 | | mV |
| $V_{IDL}$ | Low-level differential input voltage (see Note 3) | | −150 | mV |

NOTE 3: Differential input voltage is the voltage at the more positive inverting input (A or B) with respect to the noninverting input (C) of the same gate.

## electrical characteristics over recommended ranges of $V_{CC}$, $V_{EE}$, and operating free-air temperature (unless otherwise noted)

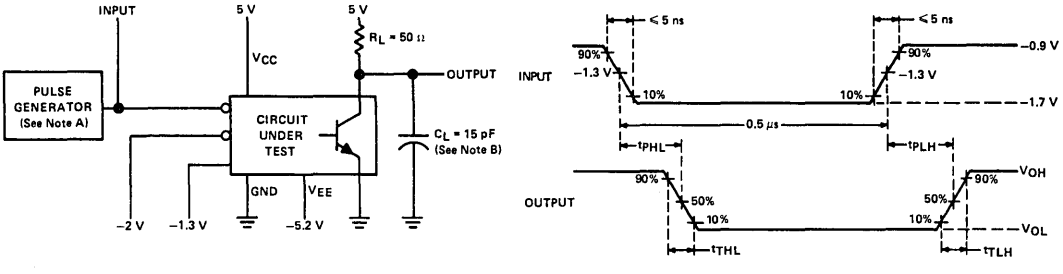
| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IDH}$ = 150 mV, $V_{OH}$ = 30 V | | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IDL}$ = −150 mV | $I_{OL}$ = 10 mA | | 0.15 | 0.3 | V |
| | | | $I_{OL}$ = 100 mA | | 0.35 | 0.5 | |
| $I_{IH}$ | High-level input current | $V_{EE}$ = −5.72 V, $V_I$ = −0.7 V, All other inputs at −5.72 V | | | 300 | 800 | μA |
| $I_{IL}$ | Low-level input current | $V_{EE}$ = −5.72 V, All other inputs at −0.7 V | $V_I$ = −2 V | | | −10 | μA |
| | | | $V_I$ = −5.72 V | | | −100 | |
| $I_{CC(H)}$ | Supply current from $V_{CC}$, all outputs high | $V_{CC}$ = 5.25 V, $V_{EE}$ = −5.72 V, All A and B inputs at −0.7 V, Both C inputs at −2 V, No load, $T_A$ = 25°C | | | 15 | 22 | mA |
| $I_{EE(H)}$ | Supply current from $V_{EE}$, all outpus high | | | | −21 | −30 | |
| $I_{CC(L)}$ | Supply current from $V_{CC}$, all outpus low | $V_{CC}$ = 5.25 V, $V_{EE}$ = −5.72 V, All A and B inputs at −2 V, Both C inputs at −0.7 V, No load, $T_A$ = 25°C | | | 40 | 56 | mA |
| $I_{EE(L)}$ | Supply current from $V_{EE}$, all outputs low | | | | −21 | −30 | |

† All typical values are at $V_{CC}$ = 5 V, $V_{EE}$ = −5.2 V, and $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $V_{EE}$ = −5.2 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{TLH}$ | Transition time, low-to-high-level output | $C_L$ = 15 pF, $R_L$ = 50 Ω, $I_O$ ≈ 100 mA, See Figure 1 | | 7 | 12 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 11 | 16 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | | | 19 | 25 | ns |
| $t_{PHL}$ | Propagation delay time high-to-low-level output | | | 22 | 30 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, $I_O$ ≈ 100 mA, See Figure 2 | $V_S$−20 | | | mV |

## PARAMETER MEASUREMENT INFORMATION

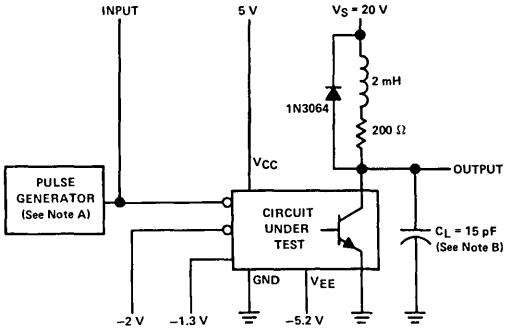



TEST CIRCUIT VOLTAGE WAVEFORMS

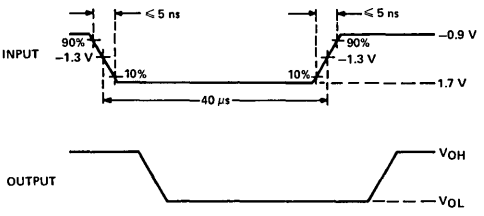
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out}$ ≈ 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1 – SWITCHING TIMES, EACH DRIVER

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT



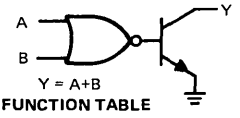

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST, EACH DRIVER

## TYPICAL APPLICATION DATA

### positive-OR gate

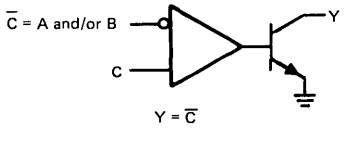



Y = A+B

FUNCTION TABLE

| CONFIGURATION | INPUTS | | | OUTPUT |
|---|---|---|---|---|
| | A | B | C | Y |
| C at $V_{BB}$ | L | L | $V_{BB}$ | L |
| | H | X | $V_{BB}$ | H |
| | X | H | $V_{BB}$ | H |

### differential ECL line receiver



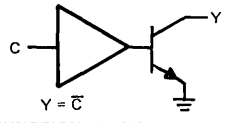

$Y = \overline{C}$

FUNCTION TABLE

| CONFIGURATION | INPUTS | | | OUTPUT |
|---|---|---|---|---|
| | A | B | C | Y |
| A and B connected together | H | H | L | H |
| | L | L | H | L |
| A not used but connected low | L | H | L | H |
| | L | L | H | L |
| B not used but connected low | H | L | L | H |
| | L | L | H | L |

H = high level, L = low level, X = irrelavant
$V_{BB}$ = Reference Supply voltage for SN10000 Series ECL.

### inverting gate




$Y = \overline{C}$

FUNCTION TABLE

| CONFIGURATION | INPUTS | | | OUTPUT |
|---|---|---|---|---|
| | A | B | C | Y |
| A and B at $V_{BB}$ | $V_{BB}$ | $V_{BB}$ | L | H |
| | $V_{BB}$ | $V_{BB}$ | H | L |
| A at $V_{BB}$, B connected low | $V_{BB}$ | L | L | H |
| | $V_{BB}$ | L | H | L |
| B at $V_{BB}$, A connected low | L | $V_{BB}$ | L | H |
| | L | $V_{BB}$ | H | L |

The one in-phase (C) and two out-of-phase (A and B) inputs per driver permit much flexibility when using the SN75441. By connecting the correct input to an externally generated $V_{BB}$ (ECL reference supply voltage), positive-OR gate or inverting gate functions may be obtained. The $V_{BB}$ reference voltage may be generated by connecting the output of any ECL gate to its out-of-phase input, by using the $V_{BB}$ pin of certain ECL devices such as SN10115, or by other methods. By driving the correct inputs differentially, these devices may be used as differential ECL line receivers and no $V_{BB}$ reference voltage is required. An unused out-of-phase input may be connected low or connected to the other out-of-phase input of the same gate in many applications.

FIGURE 3–FUNCTIONS



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# SERIES 75446
# DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12630, DECEMBER 1978 – REVISED NOVEMBER 1980

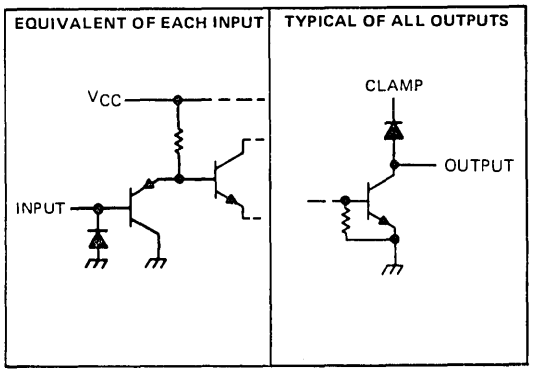
- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

## description

Series 75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series 75446 drivers are characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs

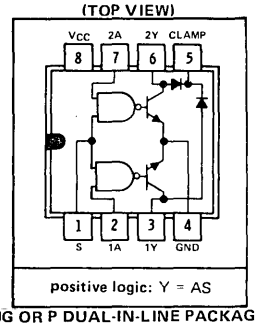



**SN75446**
**FUNCTION TABLE**
**(EACH AND DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

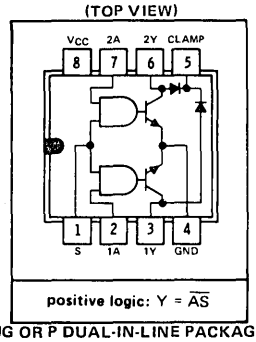



**SN75447**
**FUNCTION TABLE**
**(EACH NAND DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

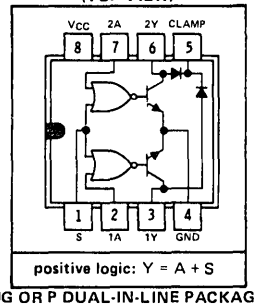



**SN75448**
**FUNCTION TABLE**
**(EACH OR DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

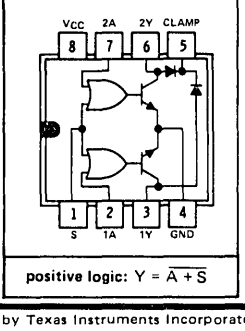



**SN75449**
**FUNCTION TABLE**
**(EACH NOR DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 400 mA
Output clamp diode current . . . . . 400 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature | 0 | | 70 | °C |

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 11. In the JG package, SN75446 through SN75449 chips are glass-mounted.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $I_I$ = −12 mA | | | −0.9 | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $V_{OH}$ = 70 V | | | 1 | 100 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 100 mA | | 0.10 | 0.3 | V |
| | | | | $I_{OL}$ = 200 mA | | 0.22 | 0.45 | |
| | | | | $I_{OL}$ = 300 mA | | 0.45 | 0.65 | |
| | | | | $I_{OL}$ = 350 mA | | 0.55 | 0.75 | |
| $V_{(BR)O}$ | Output breakdown voltage | | $V_{CC}$ = 4.75 V, $I_{OH}$ = 100 μA | | 70 | 100 | | V |
| $V_{R(K)}$ | Output clamp diode reverse voltage | | $V_{CC}$ = 4.75 V, $I_R$ = 100 μA | | 70 | 100 | | V |
| $V_{F(K)}$ | Output clamp diode forward voltage | | $V_{CC}$ = 4.75 V, $I_F$ = 350 mA | | 0.6 | 1.2 | 1.6 | V |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = 5.25 V, $V_I$ = 5.25 V | | | 0.01 | 10 | μA |
| $I_{IL}$ | Low-level input current | A input | $V_{CC}$ = 5.25 V, $V_I$ = 0.8 V | | | −0.5 | −10 | μA |
| | | Strobe S | | | | −1 | −20 | |
| $I_{CCH}$ | Supply current, outputs high | SN75446 | $V_{CC}$ = 5.25 V, | $V_I$ = 5 V | | 11 | 18 | mA |
| | | SN75447 | | $V_I$ = 0 | | 11 | 18 | |
| | | SN75448 | | $V_I$ = 5 V | | 18 | 25 | |
| | | SN75449 | | $V_I$ = 0 | | 18 | 25 | |
| $I_{CCL}$ | Supply current, outputs low | SN75446 | $V_{CC}$ = 5.25 V | $V_I$ = 0 | | 11 | 18 | mA |
| | | SN75447 | | $V_I$ = 5 V | | 11 | 18 | |
| | | SN75448 | | $V_I$ = 0 | | 18 | 25 | |
| | | SN75449 | | $V_I$ = 5 V | | 18 | 25 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.



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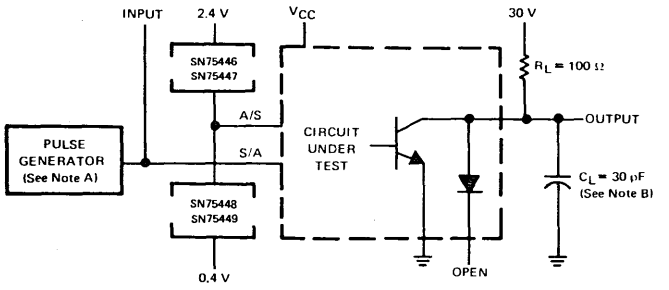
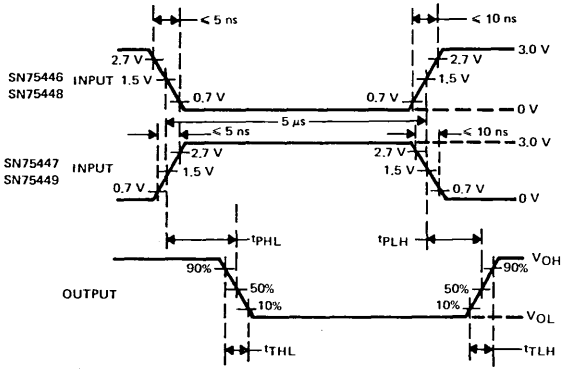
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | SN75446 | | | SN75447 | | | SN75448 | | | SN75449 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $C_L$ = 30 pF, $R_L$ = 100 Ω, See Figure 1 | | 300 | 750 | | 300 | 750 | | 300 | 750 | | 300 | 750 | ns |
| $t_{PHL}$ Propagation delay time, high-to-low-level output | | | 200 | 500 | | 200 | 500 | | 200 | 500 | | 200 | 500 | ns |
| $t_{TLH}$ Transition time, low-to-high-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $t_{THL}$ Transition time, high-to-low-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $V_{OH}$ High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

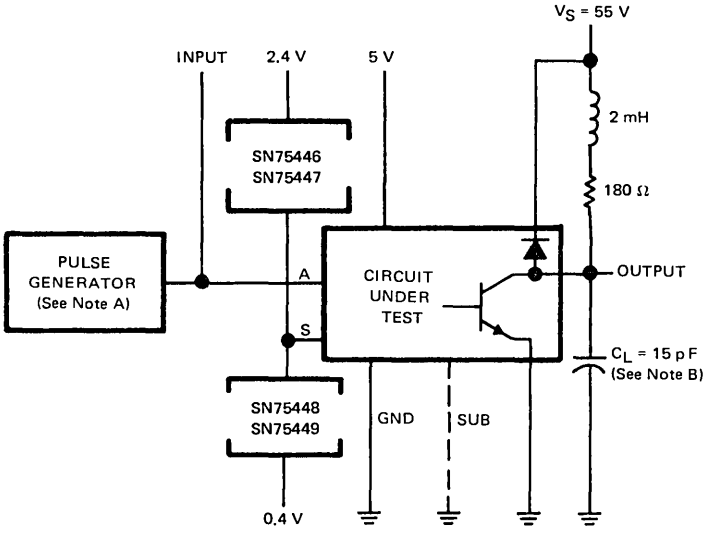



VOLTAGE WAVEFORMS

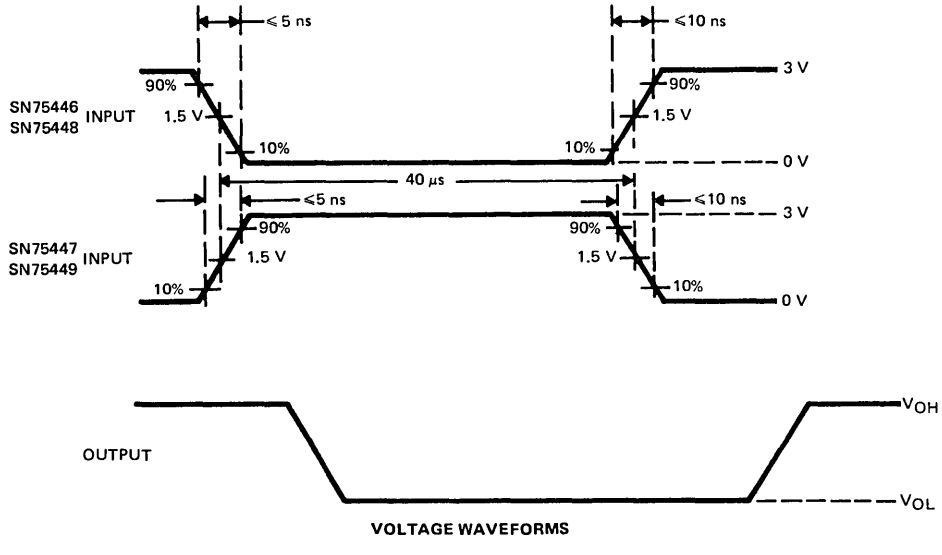
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST



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# SERIES 55450B/75450B DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12424, DECEMBER 1976 – REVISED AUGUST 1977

## PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT HIGH SPEEDS

### performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching

### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55450/75450

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---|---|---|
| SN55450B | AND† | J |
| SN55451B | AND | JG |
| SN55452B | NAND | JG |
| SN55453B | OR | JG |
| SN55454B | NOR | JG |
| SN75450B | AND† | J, N |
| SN75451B | AND | JG, P |
| SN75452B | NAND | JG, P |
| SN75453B | OR | JG, P |
| SN75454B | NOR | JG, P |

†With output transistor base connected externally to output of gate.

### description

Series 55450B/75450B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL or DTL logic. The 55450B/75450B family is functionally interchangeable with and replaces the 75450 family and the 75450A family devices manufactured previously. The speed of the 55450B/75450B family is equal to that of the 75450 family and a test to ensure freedom from latch-up has been added. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers. lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55450B drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75450B drivers are characterized for operation from 0°C to 70°C.

The SN55450B and SN75450B are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55450B | SN55451B SN55452B SN55453B SN55454B | SN75450B | SN75451B SN75452B SN75453B SN75454B | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | | 7 | 7 | 7 | 7 | V |
| Input voltage | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| Interemitter voltage (see Note 2) | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| $V_{CC}$-to-substrate voltage | | 35 | | 35 | | V |
| Collector-to-substrate voltage | | 35 | | 35 | | V |
| Collector-base voltage | | 35 | | 35 | | V |
| Collector-emitter voltage (see Note 3) | | 30 | | 30 | | V |
| Emitter-base voltage | | 5 | | 5 | | V |
| Off-state output voltage | | | 30 | | 30 | V |
| Continuous collector or output current (see Note 4) | | 400 | 400 | 400 | 400 | mA |
| Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4) | | 500 | 500 | 500 | 500 | mA |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5) | J package | 1375 | | 1025 | | mW |
| | JG package | | 1050 | | 825 | |
| | N package | | | 1150 | | |
| | P package | | | | 1000 | |
| Operating free-air temperature range | | −55 to 125 | −55 to 125 | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | | −65 to 150 | −65 to 150 | −65 to 150 | −65 to 150 | °C |
| Lead temperature 1/16 inch from case for 60 seconds | J or JG package | 300 | 300 | 300 | 300 | °C |
| Lead temperature 1/16 inch from case for 10 seconds | N or P package | 260 | 260 | 260 | 260 | °C |

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance ($R_{BE}$) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
5. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55450B through SN55454B chips are alloy-mounted; SN75450B through SN75454B chips are glass-mounted.

## recommended operating conditions (see Note 6)

| | SERIES 55450B | | | SERIES 75450B | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

NOTE 6: For the SN55450B and SN75450B only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.



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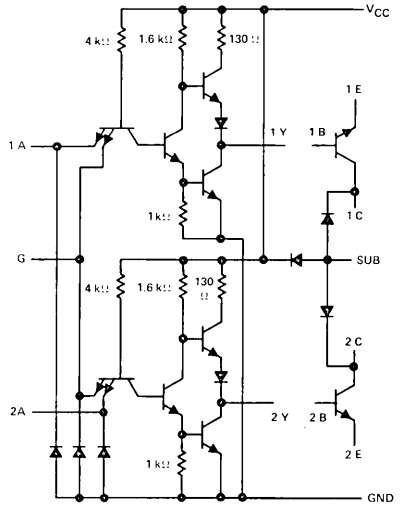
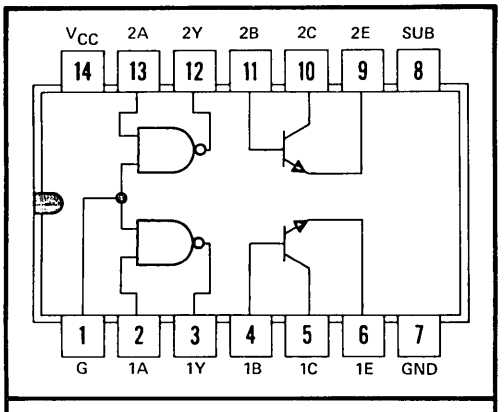
## schematic




Resistor values shown are nominal.

SN55450B . . . J
SN75450B . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### TTL gates

| PARAMETER | | | TEST CONDITIONS† | SN55450B MIN | SN55450B TYP‡ | SN55450B MAX | SN75450B MIN | SN75450B TYP‡ | SN75450B MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 16 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | input A | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | | input G | | | | 2 | | | 2 | |
| $I_{IH}$ | High-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| | | input G | | | | 80 | | | 80 | |
| $I_{IL}$ | Low-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| | | input G | | | | −3.2 | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | −18 | −35 | −55 | −18 | −35 | −55 | mA |
| $I_{CCH}$ | Supply current, outputs high | | $V_{CC}$ = MAX, $V_I$ = 0 | | 2.8 | 4 | | 2.8 | 4 | mA |
| $I_{CCL}$ | Supply current, outputs low | | $V_{CC}$ = MAX, $V_I$ = 5 V | | 7 | 11 | | 7 | 11 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.



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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### output transistors

| PARAMETER | | TEST CONDITIONS† | | SN55450B MIN | SN55450B TYP‡ | SN55450B MAX | SN75450B MIN | SN75450B TYP‡ | SN75450B MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage | $I_C$ = 100 μA, $I_E$ = 0 | | 35 | | | 35 | | | V |
| $V_{(BR)CER}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 100 μA, $R_{BE}$ = 500 Ω | | 30 | | | 30 | | | V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | $I_E$ = 100 μA, $I_C$ = 0 | | 5 | | | 5 | | | V |
| $h_{FE}$ | Static Forward Current Transfer Ratio | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = 25°C | See Note 7 | 25 | | | 25 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = 25°C | | 30 | | | 30 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = MIN | | 10 | | | 20 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = MIN | | 15 | | | 25 | | | |
| $V_{BE}$ | Base-Emitter Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 7 | | 0.85 | 1.2 | | 0.85 | 1 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 1 | 1.4 | | 1 | 1.2 | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 7 | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 0.45 | 0.8 | | 0.45 | 0.7 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 7: These parameters must be measured using pulse techniques. $t_w$ = 300 μs, duty cycle ≤ 2%.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

### TTL gates

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Figure 1 | | 12 | 22 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 8 | 15 | ns |

### output transistors

| PARAMETER | | TEST CONDITIONS‡ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_d$ | Delay time | $I_C$ = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 2 | | 8 | 15 | ns |
| $t_r$ | Rise time | | | 12 | 20 | ns |
| $t_s$ | Storage time | | | 7 | 15 | ns |
| $t_f$ | Fall time | | | 6 | 15 | ns |

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

### gates and transistors combined

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_C$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 20 | 30 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 20 | 30 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 7 | 12 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 9 | 15 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, $I_C$ ≈ 300 mA, $R_{BE}$ = 500 Ω, See Figure 4 | $V_S$−6.5 | | | mV |


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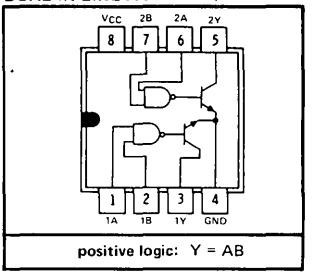
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

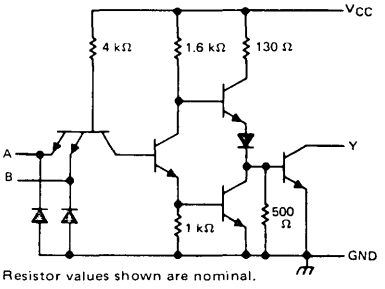
H = high level, L = low level

SN55451B . . . JG
SN75451B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = AB

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55451B | | | SN75451B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{OH}$ = 30 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 5 V | | 7 | 11 | | 7 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 0 | | 52 | 65 | | 52 | 65 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 18 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 18 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 7 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−6.5 | | | mV |

# TYPES SN55452B, SN75452B
# DUAL PERIPHERAL POSITIVE-NAND DRIVERS

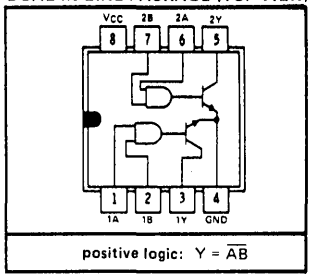
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

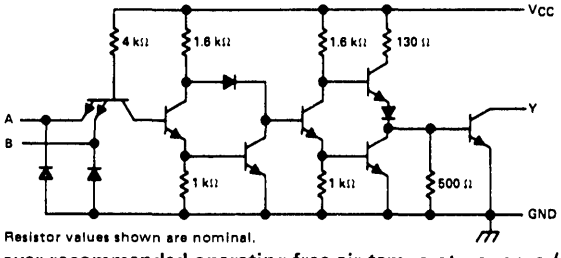
H = high level, L = low level

SN55452B . . . JG
SN75452B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AB}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN55452B | | | SN75452B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 30 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1.1 | −1.6 | | −1.1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 11 | 14 | | 11 | 14 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5V | | 56 | 71 | | 56 | 71 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 26 | 35 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 24 | 35 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 7 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−6.5 | | | mV |



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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

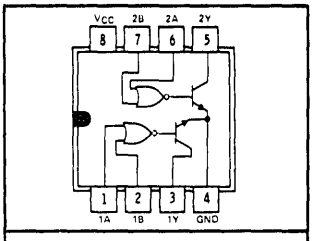
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

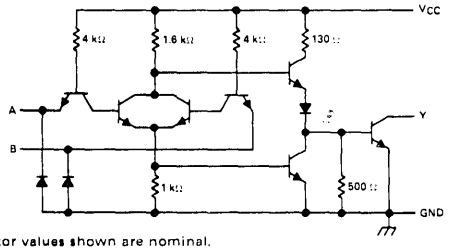
H = high level, L = low level

SN55453B . . . JG
SN75453B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = A + B

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN55453B | | | SN75453B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{OH}$ = 30 V | $V_{IH}$ = 2 V, | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $I_{OL}$ = 100 mA | $V_{IL}$ = 0.8 V, | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 300 mA | $V_{IL}$ = 0.8 V, | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, | $V_I$ = 5 V | | 8 | 11 | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, | $V_I$ = 0 | | 54 | 68 | | 54 | 68 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $R_L$ = 50 Ω, | $C_L$ = 15 pF, See Figure 3 | | 18 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 16 | 25 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | | 7 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, See Figure 4 | $I_O \approx$ 300 mA, | $V_S$−6.5 | | | mV |



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# TYPES SN55454B, SN75454B
# DUAL PERIPHERAL POSITIVE-NOR DRIVERS

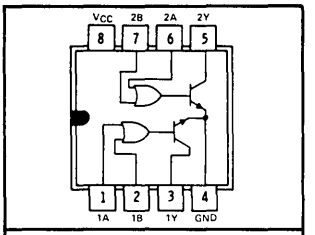
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | L (on state) |

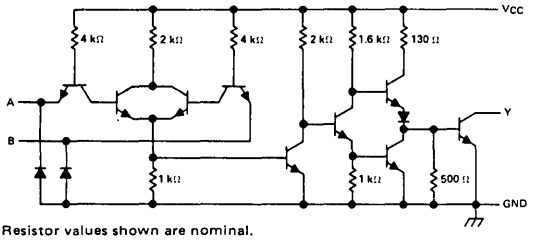
H = high level, L = low level

SN55454B . . . JG
SN75454B . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{A + B}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55454B | | | SN75454B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 30 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 13 | 17 | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5 V | | 61 | 79 | | 61 | 79 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 27 | 35 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 24 | 35 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 5 | 8 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 7 | 12 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 20 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−6.5 | | | mV |



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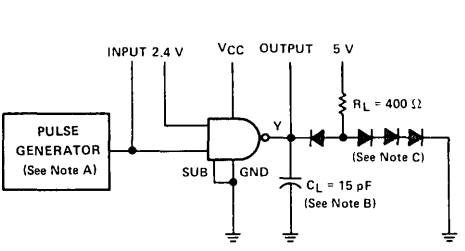
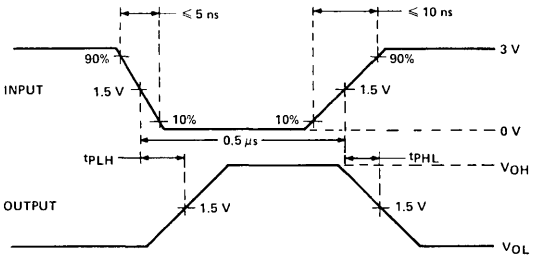
## PARAMETER MEASUREMENT INFORMATION



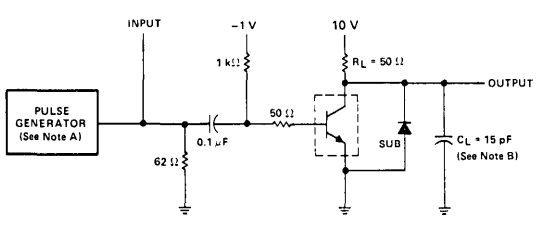

TEST CIRCUIT



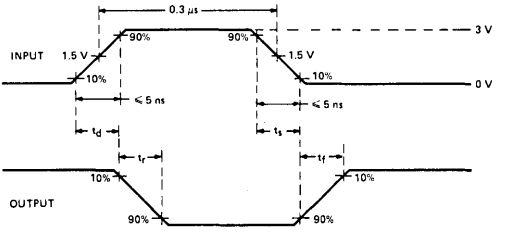

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ include probe and jig capacitance.
C. All diodes are 1N3064.

**FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55450B and SN75450B ONLY)**




TEST CIRCUIT

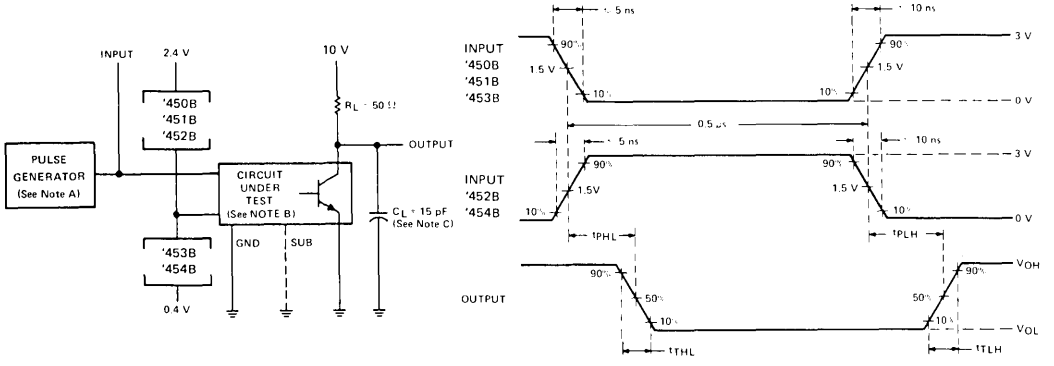



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

**FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55450B AND SN75450B ONLY)**

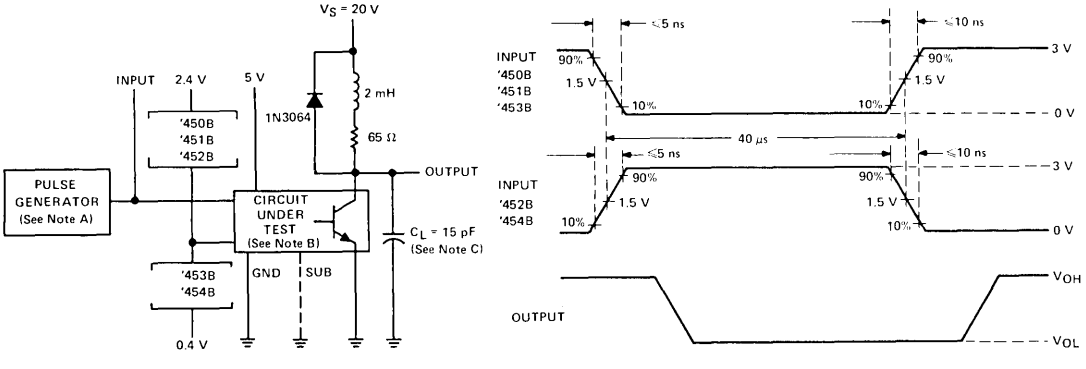
## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55450B or SN75450B, connect output Y to transistor base and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS




TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. When testing SN55450B or SN75450B, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS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## TYPICAL CHARACTERISTICS

**SN55450B, SN75450B**
TTL GATE
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

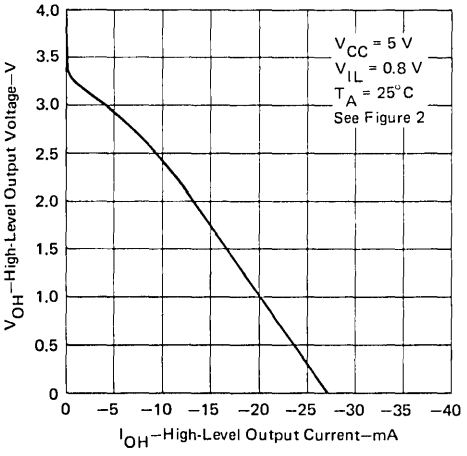


FIGURE 5

**SN55450B, SN75450B**
TRANSISTOR
STATIC FORWARD CURRENT TRANSFER RATIO
vs
COLLECTOR CURRENT

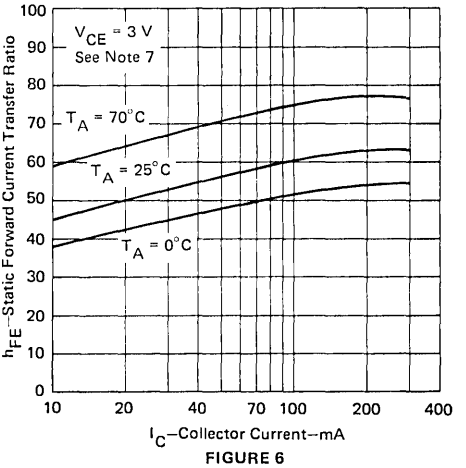


FIGURE 6

**SN55450B, SN75450B**
TRANSISTOR
BASE-EMITTER VOLTAGE
vs
COLLECTOR CURRENT

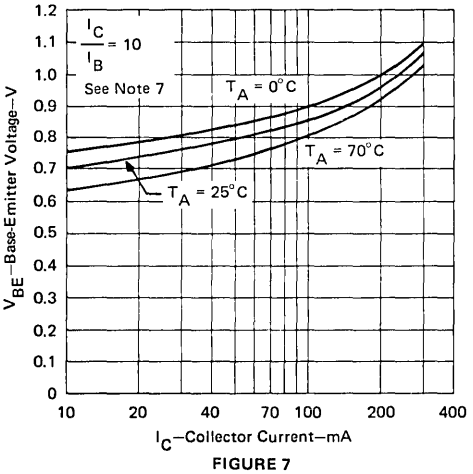


FIGURE 7

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT

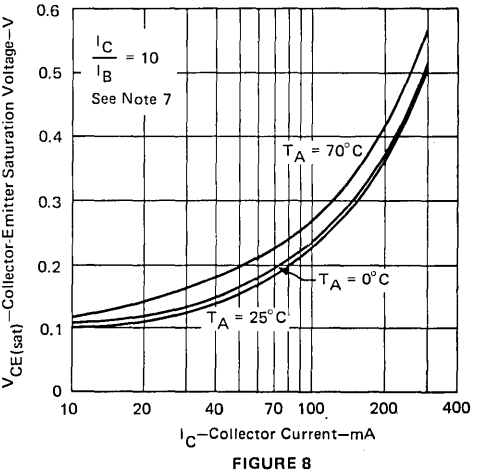


FIGURE 8

NOTE 7: These parameters must be measured using pulse techniques. $t_w$ = 300 μs, duty cycle ≤ 2%.

# SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12425, DECEMBER 1976—REVISED AUGUST 1977

## PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

### performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55460/75460

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---|---|---|
| SN55460 | AND† | J |
| SN55461 | AND | JG |
| SN55462 | NAND | JG |
| SN55463 | OR | JG |
| SN55464 | NOR | JG |
| SN75460 | AND† | J, N |
| SN75461 | AND | JG, P |
| SN75462 | NAND | JG, P |
| SN75463 | OR | JG, P |
| SN75464 | NOR | JG, P |

†With output transistor base connected externally to output of gate.

### description

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75460 drivers are characterized for operation from 0°C to 70°C.

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the gates internally connected to the bases of the n-p-n output transistors.

CONTENTS





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55460 | SN55461 SN55462 SN55463 SN55464 | SN75460 | SN75461 SN75462 SN75463 SN75464 | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | | 7 | 7 | 7 | 7 | V |
| Input voltage | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| Interemitter voltage (see Note 2) | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| $V_{CC}$-to-substrate voltage | | 40 | | 40 | | V |
| Collector-to-substrate voltage | | 40 | | 40 | | V |
| Collector-base voltage | | 40 | | 40 | | V |
| Collector-emitter voltage (see Note 3) | | 40 | | 40 | | V |
| Collector-emitter voltage (see Note 4) | | 25 | | 25 | | V |
| Emitter-base voltage | | 5 | | 5 | | V |
| Off-state output voltage | | | 35 | | 35 | V |
| Continuous collector or output current (see Note 5) | | 400 | 400 | 400 | 400 | mA |
| Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5) | | 500 | 500 | 500 | 500 | mA |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6) | J package | 1375 | | 1025 | | mW |
| | JG package | | 1050 | | 825 | |
| | N package | | | 1150 | | |
| | P package | | | | 1000 | |
| Operating free-air temperature range | | −55 to 125 | −55 to 125 | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | | −65 to 150 | −65 to 150 | −65 to 150 | −65 to 150 | °C |
| Lead temperature 1/16 inch from case for 60 seconds | J or JG package | 300 | 300 | 300 | 300 | °C |
| Lead temperature 1/16 inch from case for 10 seconds | N or P package | 260 | 260 | 260 | 260 | °C |

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance ($R_{BE}$) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55460 through SN55464 chips are alloy-mounted; SN75460 through SN75464 chips are glass-mounted.

## recommended operating conditions (see Note 7)

| | SERIES 55460 | | | SERIES 75460 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | C |

NOTE 7: For SN55460 and SN75460 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.



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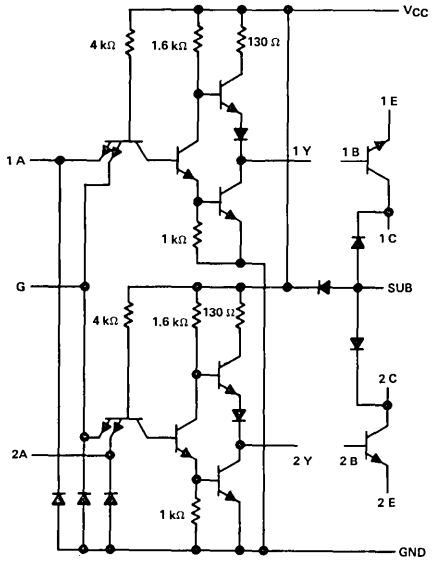
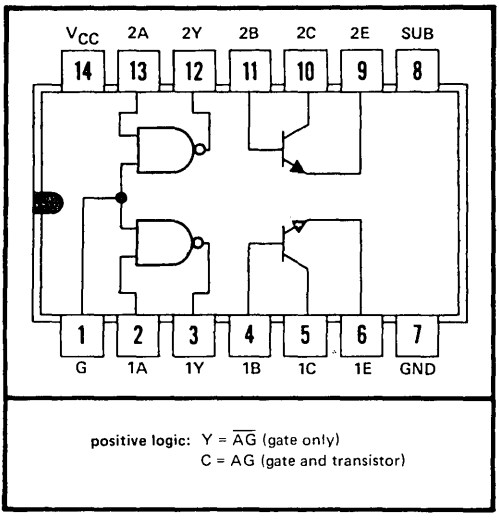
## schematic




Resistor values shown are nominal.

SN55460 . . . J
SN75460 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### TTL gates

| PARAMETER | | | TEST CONDITIONS† | SN55460 MIN | SN55460 TYP‡ | SN55460 MAX | SN75460 MIN | SN75460 TYP‡ | SN75460 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 16 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | input A | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | | input G | | | | 2 | | | 2 | |
| $I_{IH}$ | High-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| | | input G | | | | 80 | | | 80 | |
| $I_{IL}$ | Low-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| | | input G | | | | −3.2 | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | −18 | −35 | −55 | −18 | −35 | −55 | mA |
| $I_{CCH}$ | Supply current, outputs high | | $V_{CC}$ = MAX, $V_I$ = 0 | | 28 | 4 | | 28 | 4 | mA |
| $I_{CCL}$ | Supply current, outputs low | | $V_{CC}$ = MAX, $V_I$ = 5 V | | 7 | 11 | | 7 | 11 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### output transistors

| PARAMETER | | TEST CONDITIONS† | | SN55460 MIN | SN55460 TYP‡ | SN55460 MAX | SN75460 MIN | SN75460 TYP‡ | SN75460 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage | $I_C$ = 100 μA, $I_E$ = 0 | | 40 | | | 40 | | | V |
| $V_{(BR)CEO}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 10 mA, $I_B$ = 0, See Note 8 | | 25 | | | 25 | | | V |
| $V_{(BR)CER}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 100 μA, $R_{BE}$ = 500 Ω | | 40 | | | 40 | | | V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | $I_E$ = 100 μA, $I_C$ = 0 | | 5 | | | 5 | | | V |
| $h_{FE}$ | Static Forward Current Transfer Ratio | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = 25°C | See Note 8 | 25 | | | 25 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = 25°C | | 30 | | | 30 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = MIN | | 10 | | | 20 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = MIN | | 15 | | | 25 | | | |
| $V_{BE}$ | Base-Emitter Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 8 | | 0.85 | 1.2 | | 0.85 | 1 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 1 | 1.4 | | 1 | 1.2 | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 8 | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 0.45 | 0.8 | | 0.45 | 0.7 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 8: These parameters must be measured using pulse techniques. $t_w$ = 300 μs, duty cycle ≤ 2%.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

### TTL gates

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Figure 1 | | 22 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 8 | | ns |

### output transistors

| PARAMETER | | TEST CONDITIONS‡ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_d$ | Delay time | $I_C$ = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 2 | | 10 | | ns |
| $t_r$ | Rise time | | | 16 | | ns |
| $t_s$ | Storage time | | | 23 | | ns |
| $t_f$ | Fall time | | | 14 | | ns |

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

### gates and transistors combined

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_C$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 35 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 10 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_C$ ≈ 300 mA, $R_{BE}$ = 500 Ω, See Figure 4 | $V_S$−10 | | | mV |

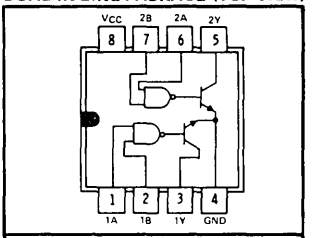
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

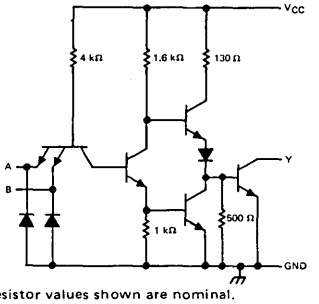
H = high level, L = low level

SN55461 . . . JG
SN75461 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = AB

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55461 MIN | SN55461 TYP‡ | SN55461 MAX | SN75461 MIN | SN75461 TYP‡ | SN75461 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{OH}$ = 35 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 5 V | | 8 | 11 | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 0 | | 56 | 76 | | 56 | 76 | mA |

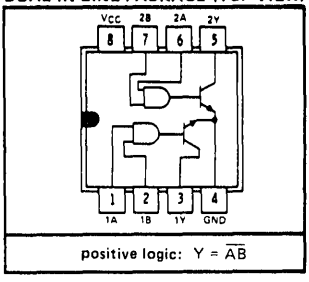
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 25 | 40 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−10 | | | mV |

# TYPES SN55462, SN75462
# DUAL PERIPHERAL POSITIVE-NAND DRIVERS

SN55462 . . . JG
SN75462 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AB}$

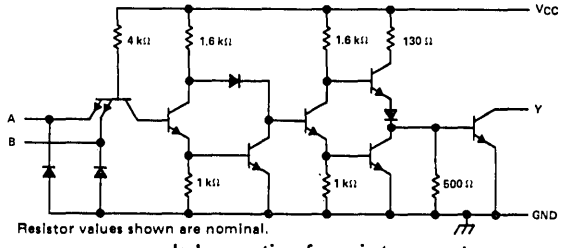
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

H = high level, L = low level

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN55462 | | | SN75462 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 35 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1.1 | −1.6 | | −1.1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 13 | 17 | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5V | | 61 | 76 | | 61 | 76 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 13 | 25 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−10 | | | mV |



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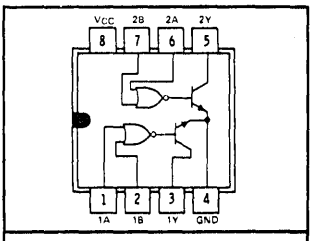
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

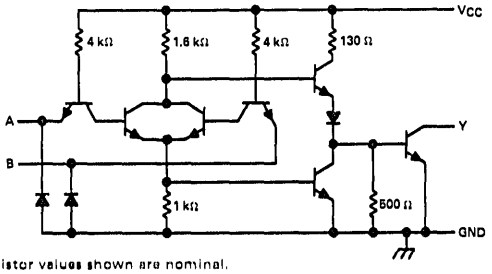
H = high level, L = low level

SN55463 . . . JG
SN75463 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = A + B

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55463 | | | SN75463 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{OH}$ = 35 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 5 V | | 8 | 11 | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 0 | | 58 | 76 | | 58 | 76 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 25 | 40 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 25 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 25 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_O$ ≈ 300 mA, See Figure 4 | $V_S$−10 | | | mV |

# TYPES SN55464, SN75464
# DUAL PERIPHERAL POSITIVE-NOR DRIVERS

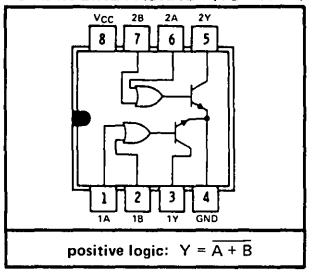
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | L (on state) |

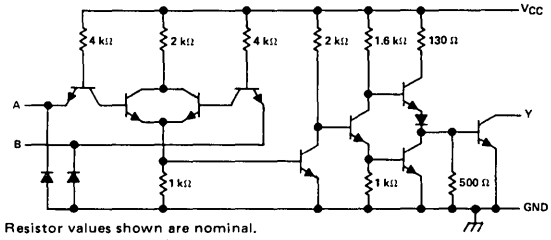
H = high level, L = low level

SN55464 . . . JG
SN75464 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{A + B}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55464 MIN | SN55464 TYP‡ | SN55464 MAX | SN75464 MIN | SN75464 TYP‡ | SN75464 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 25 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 14 | 19 | | 14 | 19 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5 V | | 67 | 85 | | 67 | 85 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 40 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 30 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−10 | | | mV |



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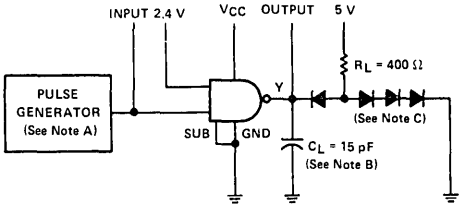
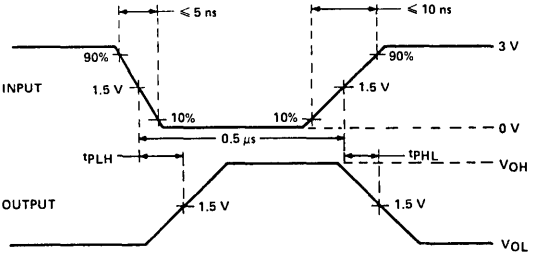
## PARAMETER MEASUREMENT INFORMATION



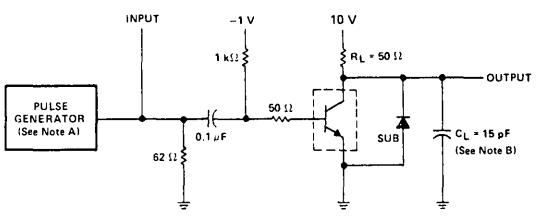

TEST CIRCUIT



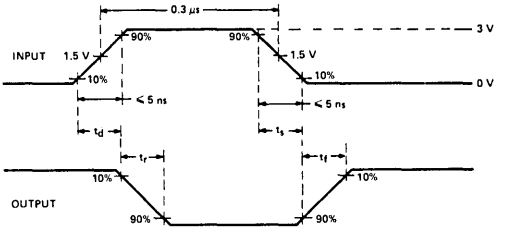

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ include probe and jig capacitance.
C. All diodes are 1N3064.

**FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55460 AND SN75460 ONLY)**




TEST CIRCUIT

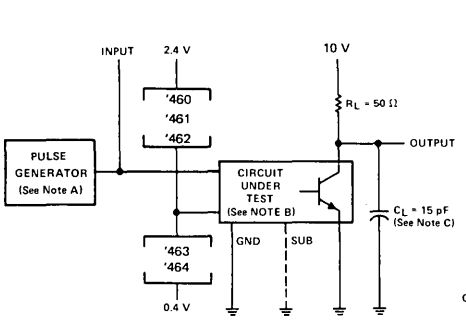



VOLTAGE WAVEFORMS

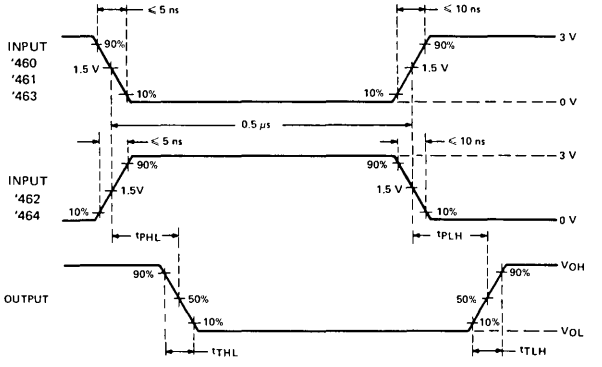
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

**FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55460 AND SN75460 ONLY)**

## PARAMETER MEASUREMENT INFORMATION



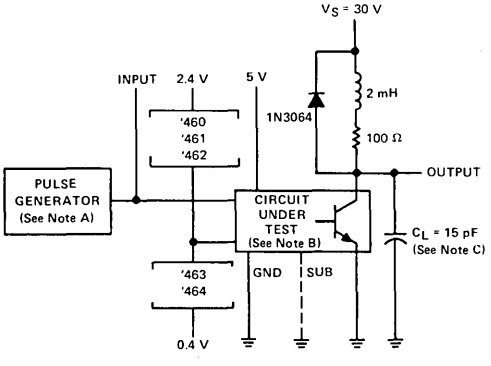

TEST CIRCUIT



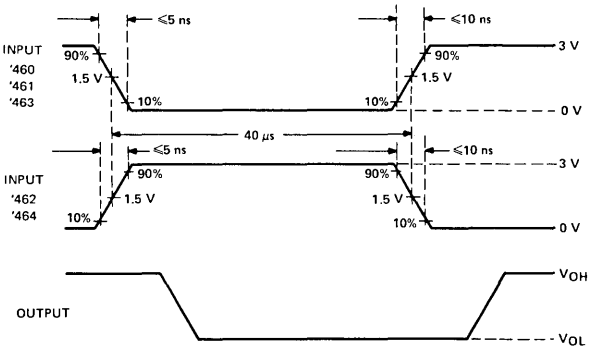

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55460 or SN75460, connect output Y to transistor base and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} \approx 50\ \Omega$.
B. When testing SN55460 or SN75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

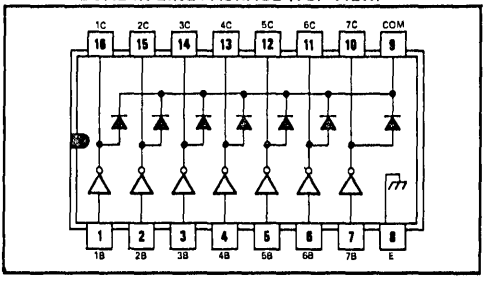
# SERIES 75465 DARLINGTON TRANSISTOR ARRAYS

BULLETIN NO. DL-S 12459, DECEMBER 1976 – REVISED DECEMBER 1980

## HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2005A, ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

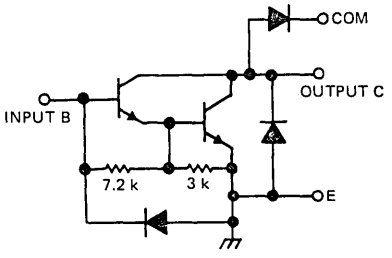



### description

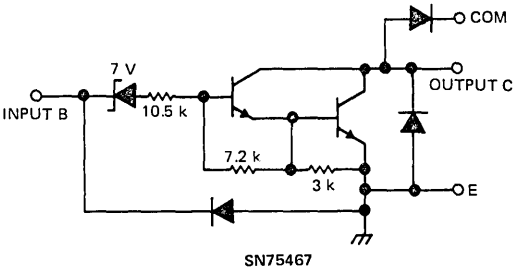
Series 75465 devices are monolithic high-voltage, high-current darlington transistor arrays. Each comprises seven n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The SN75465 has a 1.05-kΩ series base resistor and is especially designed for use with TTL where higher output current is required and loading of the driving source is not a concern. The SN75466 is a general-purpose array and may be used with DTL, TTL, P-MOS, CMOS, etc. The SN75467 is specifically designed for use with 14- to 25-volt P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a 2.7-kΩ series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The SN75469 has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the SN75468 while the required voltage is less than that required by the SN75467.

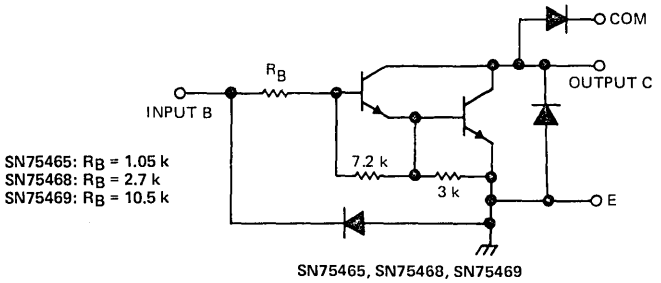
### schematics (each darlington pair)




SN75466




SN75467




SN75465: $R_B$ = 1.05 k
SN75468: $R_B$ = 2.7 k
SN75469: $R_B$ = 10.5 k

SN75465, SN75468, SN75469

All resistor values shown are nominal and in ohms.





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## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

| | |
|---|---|
| Collector-emitter voltage | 100 V |
| Input voltage (see Note 1): SN75465 | 15 V |
| SN75467, SN75468, SN75469 | 30 V |
| Peak collector current (see Figures 14 and 15) | 500 mA |
| Output clamp diode current | 500 mA |
| Continuous input current, SN75466 only | 25 mA |
| Total substrate-terminal current: J package | −500 mA |
| N package | −2.5 A |
| Continuous dissipation (total package) at (or below) 25°C free-air temperature (see Note 2): | |
| J package | 1025 mW |
| N package | 1150 mW |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −65°C to 150°C |
| Lead temperature 1/16 inch from case for 60 seconds, J package | 300°C |
| Lead temperature 1/16 inch from case for 10 seconds, N package | 260°C |

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 11. In the J package, SN75465 through SN75469 chips are glass-mounted.

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | | SN75465 MIN | SN75465 TYP | SN75465 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 100 V, | $I_I$ = 0 | | | | 50 | μA |
| | | | $V_{CE}$ = 100 V, | $I_I$ = 0, | $T_A$ = 70°C | | | 100 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 100 V, | $I_C$ = 500 μA, | $T_A$ = 70°C | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 3 V | | | | 1.5 | 2.4 | mA |
| $V_{I(on)}$ | On-state input voltage | 5 | $V_{CE}$ = 2 V, | $I_C$ = 350 mA | | | | 2.4 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 6 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | | 0.9 | 1.1 | V |
| | | | $I_I$ = 350 μA, | $I_C$ = 200 mA | | | 1.0 | 1.3 | |
| | | | $I_I$ = 500 μA, | $I_C$ = 350 mA | | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 100 V | | | | | 50 | μA |
| | | | $V_R$ = 100 V, | $T_A$ = 70°C | | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 350 mA | | | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | | 15 | 25 | pF |



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## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | SN75466 MIN | SN75466 TYP | SN75466 MAX | SN75467 MIN | SN75467 TYP | SN75467 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 100 V, | $I_I$ = 0 | | | 50 | | | 50 | μA |
| | | 1 | $V_{CE}$ = 100 V, | $I_I$ = 0 | | | 100 | | | 100 | |
| | | 2 | $T_A$ = 70°C | $V_I$ = 6 V | | | | | | 500 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, $T_A$ = 70°C | $I_C$ = 500 μA, | 50 | 65 | | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 17 V | | | | | | 0.85 | 1.3 | mA |
| $h_{FE}$ | Static forward current transfer ratio | 6 | $V_{CE}$ = 2 V, | $I_C$ = 350 mA | 1000 | | | | | | |
| $V_{I(on)}$ | On-state input voltage | 5 | $V_{CE}$ = 2 V, | $I_C$ = 300 mA | | | | | | 13 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 6 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | V |
| | | 6 | $I_I$ = 350 μA, | $I_C$ = 200 mA | | 1.0 | 1.3 | | 1.0 | 1.3 | |
| | | 6 | $I_I$ = 500 μA, | $I_C$ = 350 mA | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 100 V, | | | | 50 | | | 50 | μA |
| | | 7 | $V_R$ = 100 V, | $T_A$ = 70°C | | | 100 | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 350 mA | | | 1.7 | 2 | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | 15 | 25 | | 15 | 25 | pF |

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | SN75468 MIN | SN75468 TYP | SN75468 MAX | SN75469 MIN | SN75469 TYP | SN75469 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 100 V, | $I_I$ = 0 | | | 50 | | | 50 | μA |
| | | 1 | $V_{CE}$ = 100 V, | $I_I$ = 0 | | | 100 | | | 100 | |
| | | 2 | $T_A$ = 70°C | $V_I$ = 1 V | | | | | | 500 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, $T_A$ = 70°C | $I_C$ = 500 μA, | 50 | 65 | | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 3.85 V | | | 0.93 | 1.35 | | | | mA |
| | | 4 | $V_I$ = 5 V | | | | | | 0.35 | 0.5 | |
| | | 4 | $V_I$ = 12 V | | | | | | 1.0 | 1.45 | |
| $V_{I(on)}$ | On-state input voltage | 5 | $V_{CE}$ = 2 V | $I_C$ = 125 mA | | | | | | 5 | V |
| | | 5 | | $I_C$ = 200 mA | | | 2.4 | | | 6 | |
| | | 5 | | $I_C$ = 250 mA | | | 2.7 | | | | |
| | | 5 | | $I_C$ = 275 mA | | | | | | 7 | |
| | | 5 | | $I_C$ = 300 mA | | | 3 | | | | |
| | | 5 | | $I_C$ = 350 mA | | | | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 6 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | |
| | | 6 | $I_I$ = 350 μA, | $I_C$ = 200 mA | | 1.0 | 1.3 | | 1.0 | 1.3 | |
| | | 6 | $I_I$ = 500 μA, | $I_C$ = 350 mA | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 100 V | | | | 50 | | | 50 | μA |
| | | 7 | $V_R$ = 100 V, | $T_A$ = 70°C | | | 100 | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 305 mA | | | 1.7 | 2 | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | 15 | 25 | | 15 | 25 | pF |

## switching characteristics at 25°C free-air temperature

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_S$ = 50 V, | $R_L$ = 163 Ω, | | 130 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $C_L$ = 15 pF, | See Figure 9 | | 20 | | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 60 V, See Figure 10 | $I_O$ ≈ 300 mA, | $V_S$–20 | | | mV |

## PARAMETER MEASUREMENT INFORMATION

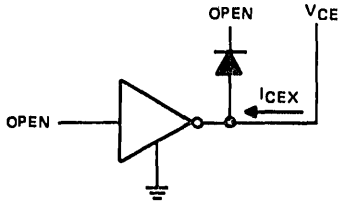



FIGURE 1–$I_{CEX}$

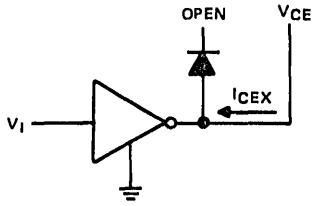



FIGURE 2–$I_{CEX}$

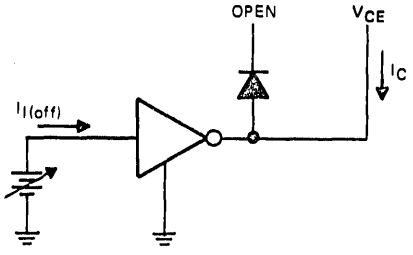



FIGURE 3–$I_{I(off)}$

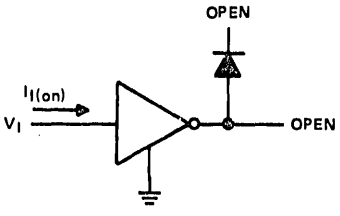



FIGURE 4–$I_I$

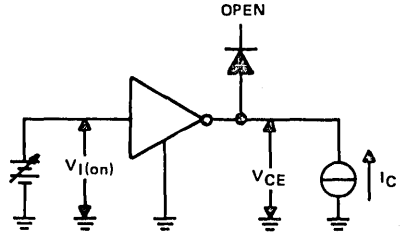
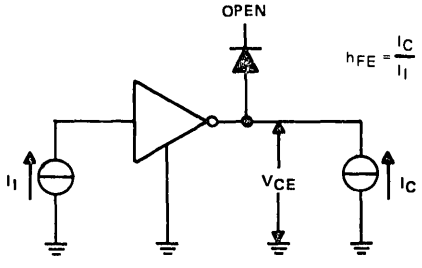



FIGURE 5–$V_{I(on)}$




NOTE: $I_I$ is fixed for measuring $V_{CE(sat)}$, variable for measuring $h_{FE}$.

FIGURE 6–$h_{FE}$, $V_{CE(sat)}$

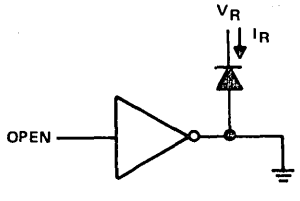



FIGURE 7–$I_R$

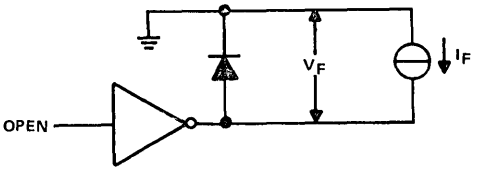



FIGURE 8–$V_F$



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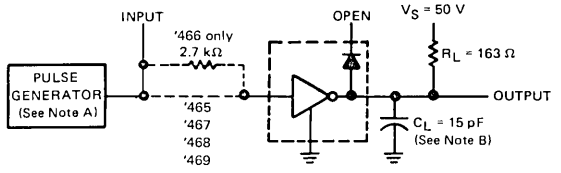
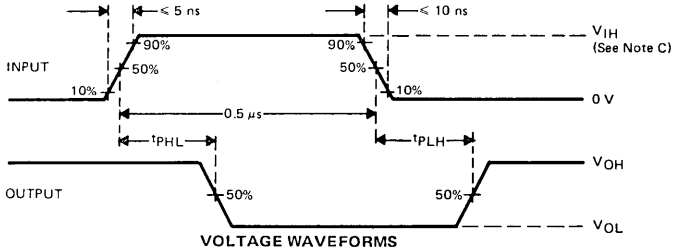
## PARAMETER MEASUREMENT INFORMATION



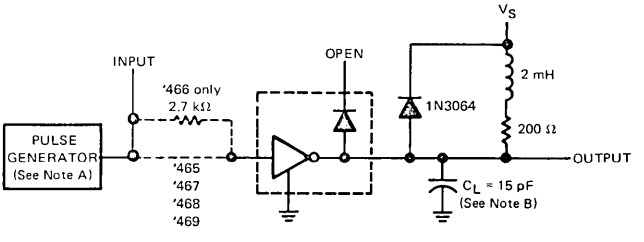

TEST CIRCUIT



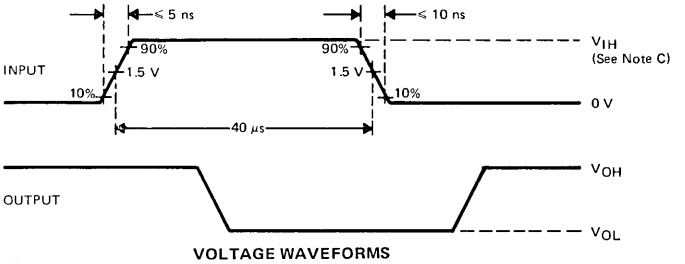

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.
C. For testing the '465, '466, and '468, $V_{IH}$ = 3 V; for the '467, $V_{IH}$ = 13 V; for the '469, $V_{IH}$ = 8 V.

**FIGURE 9—PROPAGATION DELAY TIMES**




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. For testing the '465, '466, and '468, $V_{IH}$ = 3 V; for the '467, $V_{IH}$ = 13 V; for the '469, $V_{IH}$ = 8 V.

**FIGURE 10—LATCH-UP TEST**

## TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

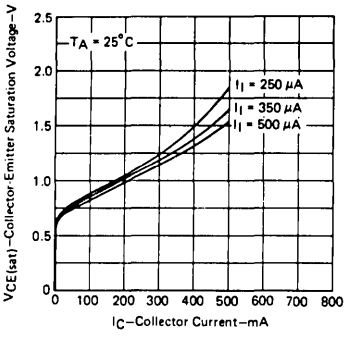



FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

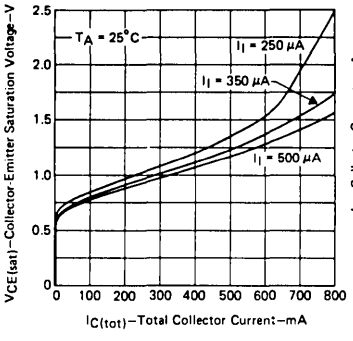



FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

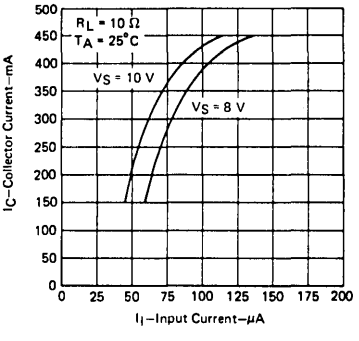



FIGURE 13

## THERMAL INFORMATION

J PACKAGE
MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

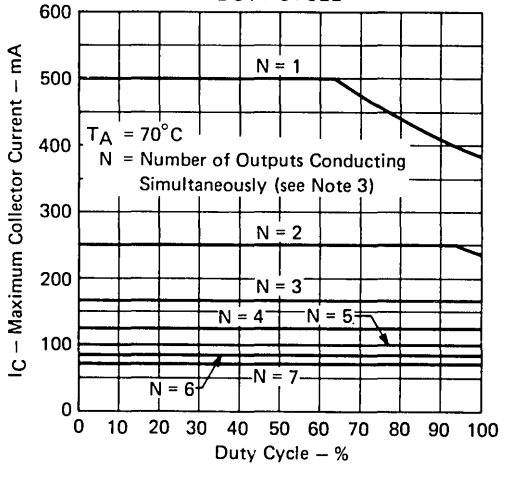



FIGURE 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

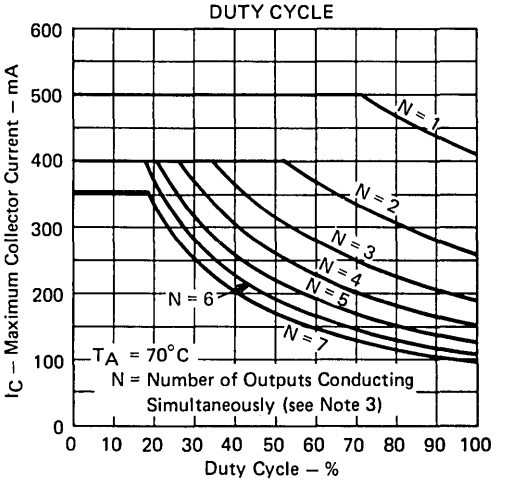



FIGURE 15

NOTE 3: For the J package, N x $I_C$ must not exceed 500 mA (maximum substrate current). For the N package N x $I_C$ must not exceed 2.5 A.



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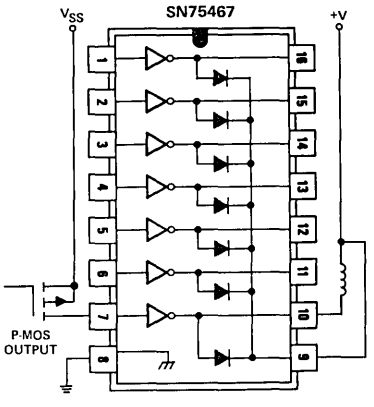
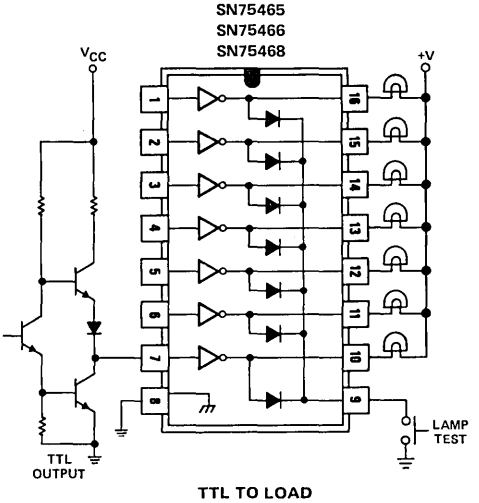
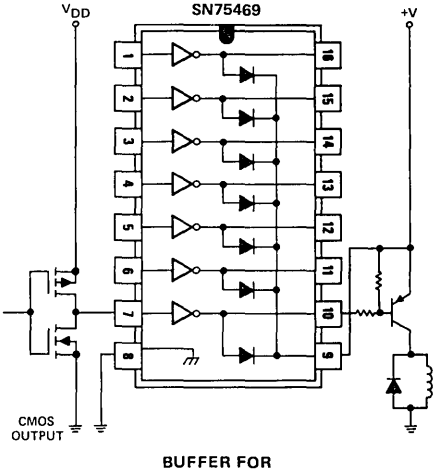
## TYPICAL APPLICATION DATA



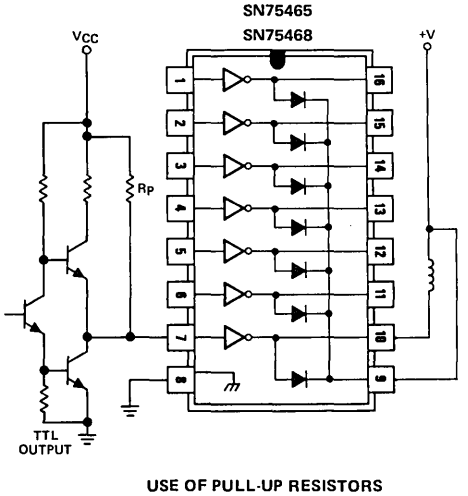

P-MOS TO LOAD




TTL TO LOAD




BUFFER FOR
HIGHER CURRENT LOADS




USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

1280

# SERIES 55470/75470 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12369, MARCH 1976 – REVISED AUGUST 1977

## PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

### performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching

### ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55470/75470

| DEVICE | LOGIC OF COMPLETE CIRCUIT | PACKAGES |
|---|---|---|
| SN55470 | AND† | J |
| SN55471 | AND | JG |
| SN55472 | NAND | JG |
| SN55473 | OR | JG |
| SN55474 | NOR | JG |
| SN75470 | AND† | J, N |
| SN75471 | AND | JG, P |
| SN75472 | NAND | JG, P |
| SN75473 | OR | JG, P |
| SN75474 | NOR | JG, P |

†With output transistor base connected externally to output of gate.

### description

Series 55470/75470 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 55450B/75450B (limits are the same as Series 55460/75460). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55470 drivers are characterized for operation over the full military temperature range of –55°C to 125°C; Series 75470 drivers are characterized for operation from 0°C to 70°C.

The SN55470 and SN75470 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55471/SN75471, SN55472/SN75472, SN55473/SN75473, and SN55474/SN75474 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS





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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | SN55470 | SN55471 SN55472 SN55473 SN55474 | SN75470 | SN75471 SN75472 SN75473 SN75474 | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | | 7 | 7 | 7 | 7 | V |
| Input voltage | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| Interemitter voltage (see Note 2) | | 5.5 | 5.5 | 5.5 | 5.5 | V |
| $V_{CC}$-to-substrate voltage | | 40 | | 40 | | V |
| Collector-to-substrate voltage | | 70 | | 70 | | V |
| Collector-base voltage | | 70 | | 70 | | V |
| Collector-emitter voltage (see Note 3) | | 70 | | 70 | | V |
| Collector-emitter voltage (see Note 4) | | 40 | | 40 | | V |
| Emitter-base voltage | | 5 | | 5 | | V |
| Off-state output voltage | | | 70 | | 70 | V |
| Continuous collector or output current (see Note 5) | | 400 | 400 | 400 | 400 | mA |
| Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5) | | 500 | 500 | 500 | 500 | mA |
| Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6) | J package | 1375 | | 1025 | | mW |
| | JG package | | 1050 | | 825 | |
| | N package | | | 1150 | | |
| | P package | | | | 1000 | |
| Operating free-air temperature range | | −55 to 125 | −55 to 125 | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | | −65 to 150 | −65 to 150 | −65 to 150 | −65 to 150 | °C |
| Lead temperature 1/16 inch from case for 60 seconds | J or JG package | 300 | 300 | 300 | 300 | °C |
| Lead temperature 1/16 inch from case for 10 seconds | N or P package | 260 | 260 | 260 | 260 | °C |

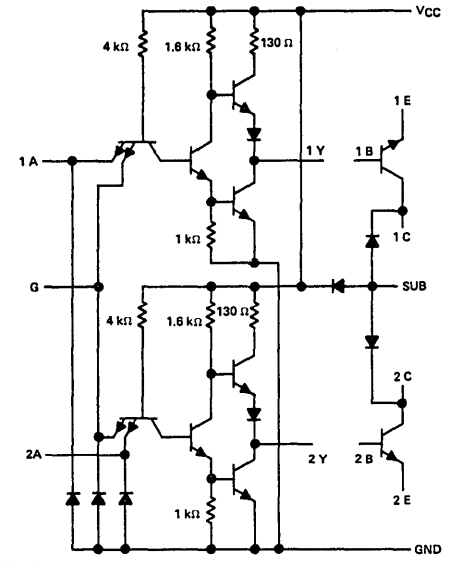
NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance ($R_{BE}$) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55470 through SN55474 chips are alloy-mounted; SN75470 through SN75474 chips are glass-mounted.

## recommended operating conditions (see Note 7)

| | SERIES 55470 | | | SERIES 75470 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

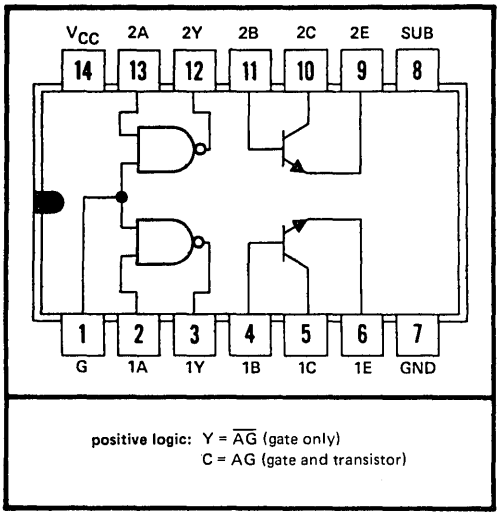
NOTE 7: For SN55470 and SN75470 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

## schematic




Resistor values shown are nominal.

SN55470 . . . J
SN75470 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)




## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### TTL gates

| PARAMETER | | | TEST CONDITIONS† | SN55470 MIN | SN55470 TYP‡ | SN55470 MAX | SN75470 MIN | SN75470 TYP‡ | SN75470 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OH}$ = −400 μA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 16 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | input A | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| | | input G | | | | 2 | | | 2 | |
| $I_{IH}$ | High-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| | | input G | | | | 80 | | | 80 | |
| $I_{IL}$ | Low-level input current | input A | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| | | input G | | | | −3.2 | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | −18 | −35 | −55 | −18 | −35 | −55 | mA |
| $I_{CCH}$ | Supply current, outputs high | | $V_{CC}$ = MAX, $V_I$ = 0 | | 2.8 | 4 | | 2.8 | 4 | mA |
| $I_{CCL}$ | Supply current, outputs low | | $V_{CC}$ = MAX, $V_I$ = 5 V | | 7 | 11 | | 7 | 11 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### output transistors

| PARAMETER | | TEST CONDITIONS† | | SN55470 MIN | SN55470 TYP‡ | SN55470 MAX | SN75470 MIN | SN75470 TYP‡ | SN75470 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage | $I_C$ = 100 μA, $I_E$ = 0 | | 70 | | | 70 | | | V |
| $V_{(BR)CEO}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 10 mA, $I_B$ = 0, See Note 8 | | 40 | | | 40 | | | V |
| $V_{(BR)CER}$ | Collector-Emitter Breakdown Voltage | $I_C$ = 100 μA, $R_{BE}$ = 500 Ω | | 70 | | | 70 | | | V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | $I_E$ = 100 μA, $I_C$ = 0 | | 5 | | | 5 | | | V |
| $h_{FE}$ | Static Forward Current Transfer Ratio | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = 25°C | See Note 8 | 25 | | | 25 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = 25°C | | 30 | | | 30 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 100 mA, $T_A$ = MIN | | 10 | | | 20 | | | |
| | | $V_{CE}$ = 3 V, $I_C$ = 300 mA, $T_A$ = MIN | | 15 | | | 25 | | | |
| $V_{BE}$ | Base-Emitter Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 8 | | 0.85 | 1.2 | | 0.85 | 1 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 1 | 1.4 | | 1 | 1.2 | |
| $V_{CE(sat)}$ | Collector-Emitter Saturation Voltage | $I_B$ = 10 mA, $I_C$ = 100 mA | See Note 8 | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $I_B$ = 30 mA, $I_C$ = 300 mA | | | 0.45 | 0.8 | | 0.45 | 0.7 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 8: These parameters must be measured using pulse techniques. $t_w$ = 300 μs, duty cycle ≤ 2%.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

### TTL gates

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Figure 1 | | 22 | | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 8 | | ns |

### output transistors

| PARAMETER | | TEST CONDITIONS‡ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_d$ | Delay time | $I_C$ = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 2 | | 10 | | ns |
| $t_r$ | Rise time | | | 16 | | ns |
| $t_s$ | Storage time | | | 23 | | ns |
| $t_f$ | Fall time | | | 14 | | ns |

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

### gates and transistors combined

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_C$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 35 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 10 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_C$ ≈ 300 mA, $R_{BE}$ = 500 Ω, See Figure 4 | $V_S$−18 | | | mV |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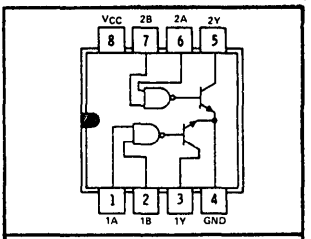
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | H (off state) |

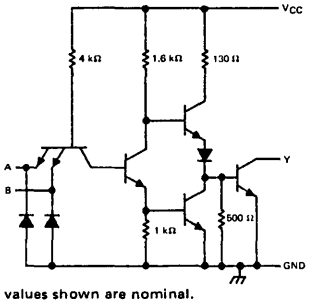
H = high level, L = low level

SN55471 . . . JG
SN75471 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: Y = AB

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55471 MIN | SN55471 TYP‡ | SN55471 MAX | SN75471 MIN | SN75471 TYP‡ | SN75471 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 5 V | | 8 | 11 | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 0 | | 56 | 76 | | 56 | 76 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 25 | 40 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−18 | | | mV |

# TYPES SN55472, SN75472
# DUAL PERIPHERAL POSITIVE-NAND DRIVERS

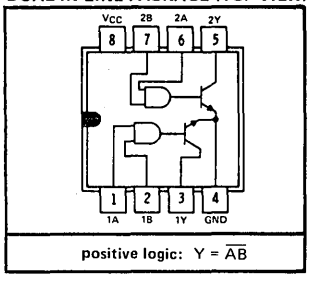
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | L (on state) |

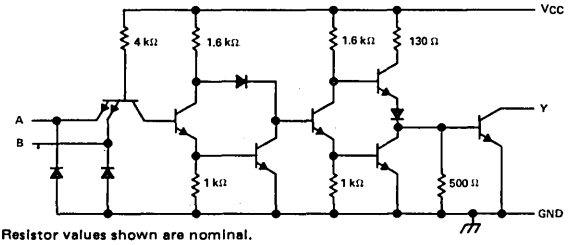
H = high level, L = low level

SN55472 . . . JG
SN75472 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{AB}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN55472 MIN | SN55472 TYP† | SN55472 MAX | SN75472 MIN | SN75472 TYP‡ | SN75472 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 70 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1.1 | −1.6 | | −1.1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 13 | 17 | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5V | | 61 | 76 | | 61 | 76 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 13 | 25 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−18 | | | mV |



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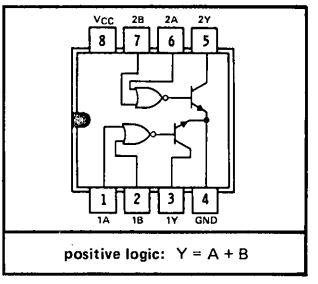
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | L (on state) |
| L | H | H (off state) |
| H | L | H (off state) |
| H | H | H (off state) |

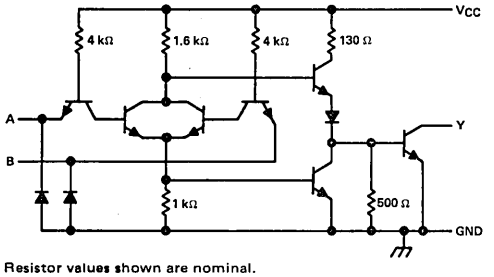
H = high level, L = low level

SN55473 . . . JG
SN75473 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = A + B$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55473 | | | SN75473 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 5 V | | 8 | 11 | | 8 | 11 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 0 | | 58 | 76 | | 58 | 76 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 30 | 55 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 25 | 40 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 25 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 25 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−18 | | | mV |

# TYPES SN55474, SN75474
# DUAL PERIPHERAL POSITIVE-NOR DRIVERS

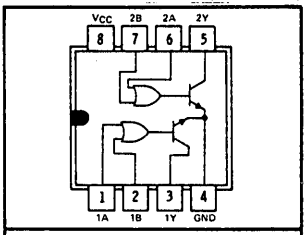
## logic

FUNCTION TABLE
(EACH DRIVER)

| A | B | Y |
|---|---|---|
| L | L | H (off state) |
| L | H | L (on state) |
| H | L | L (on state) |
| H | H | L (on state) |

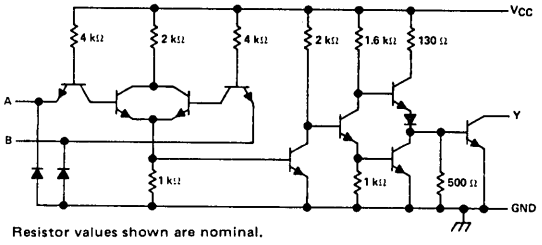
H = high level, L = low level

SN55474 . . . JG
SN75474 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)




positive logic: $Y = \overline{A + B}$

## schematic (each driver)




Resistor values shown are nominal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN55474 | | | SN75474 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | −1.2 | −1.5 | | −1.2 | −1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{OH}$ = 70 V | | | 300 | | | 100 | μA |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 100 mA | | 0.25 | 0.5 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $I_{OL}$ = 300 mA | | 0.5 | 0.8 | | 0.5 | 0.7 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | −1 | −1.6 | | −1 | −1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = MAX, $V_I$ = 0 V | | 14 | 19 | | 14 | 19 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = MAX, $V_I$ = 5 V | | 67 | 85 | | 67 | 85 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O \approx$ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, See Figure 3 | | 40 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | | | 8 | 20 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | | | 10 | 20 | ns |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 4 | $V_S$−18 | | | mV |



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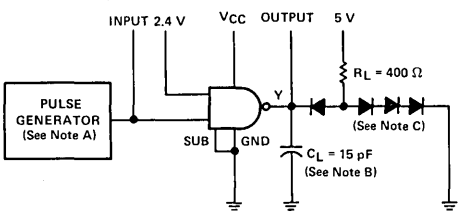
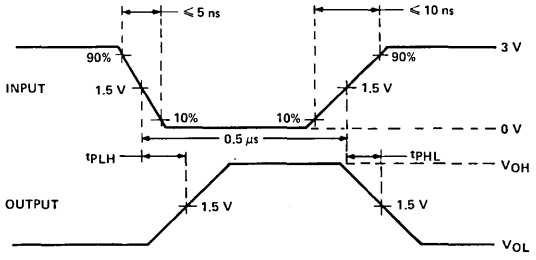
## PARAMETER MEASUREMENT INFORMATION



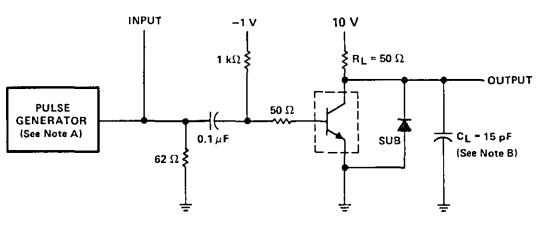

TEST CIRCUIT



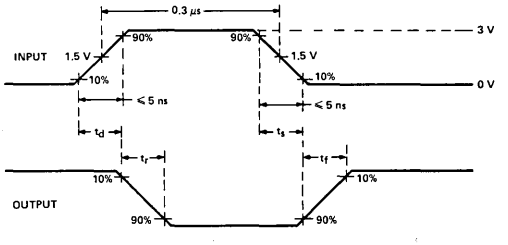

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55470 AND SN75470 ONLY)




TEST CIRCUIT

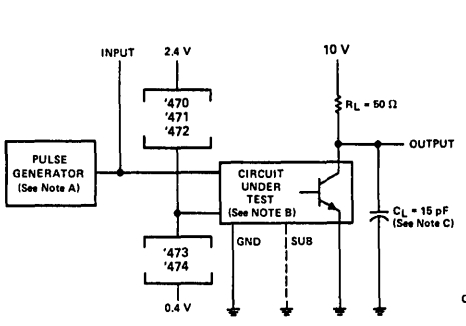



VOLTAGE WAVEFORMS

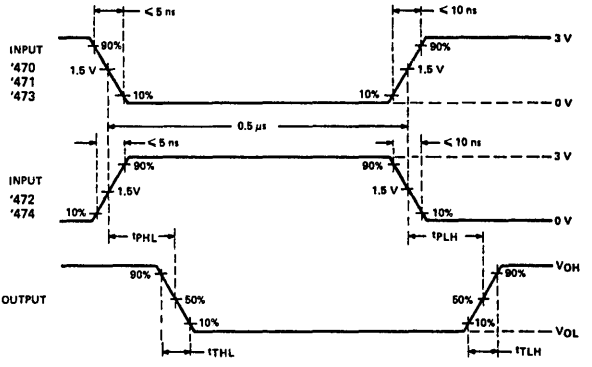
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55470 AND SN75470 ONLY)

## PARAMETER MEASUREMENT INFORMATION



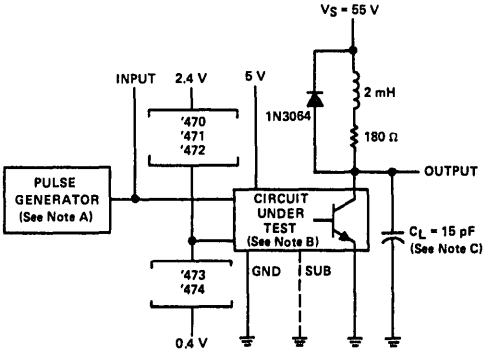

TEST CIRCUIT



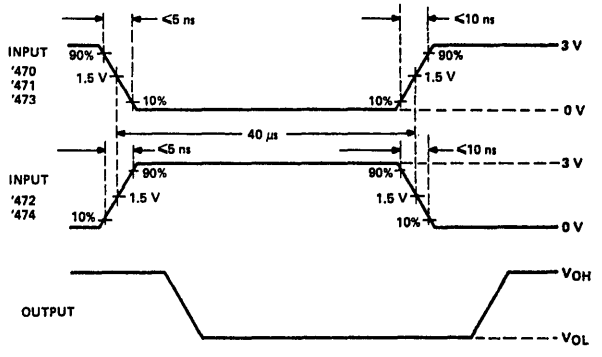

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55470 or SN75470, connect output Y to transistor base and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. When testing SN55470 or SN75470, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. $C_L$ includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

# SERIES 75476 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12480, DECEMBER 1976 – REVISED AUGUST 1977

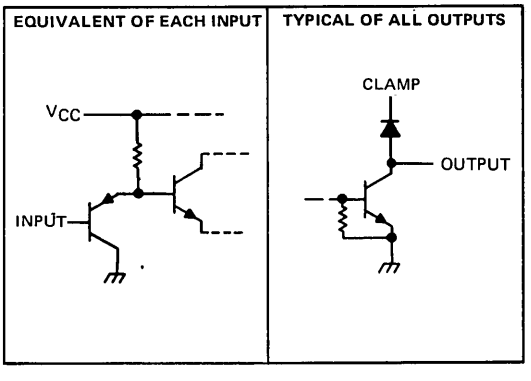
- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typical)
- High-Speed Switching
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

## description

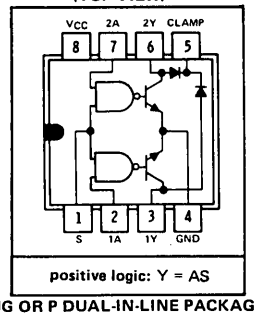
Series 75476 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series 75476 drivers are characterized for operation from 0°C to 70°C.

## schematics of inputs and outputs




JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

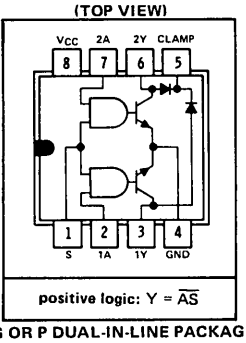



**SN75476**
**FUNCTION TABLE**
**(EACH AND DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

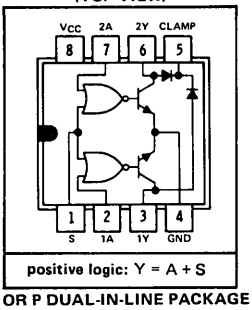



**SN75477**
**FUNCTION TABLE**
**(EACH NAND DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

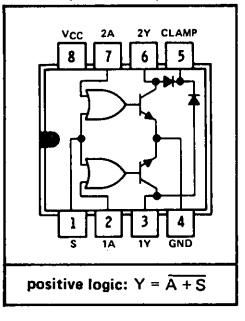



**SN75478**
**FUNCTION TABLE**
**(EACH OR DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)




**SN75479**
**FUNCTION TABLE**
**(EACH NOR DRIVER)**

| INPUTS | | OUTPUT |
|---|---|---|
| A | S | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = high level
L = low level

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_W \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_W \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 400 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: P package . . . . . 260°C

## recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | V |
| Operating free-air temperature | 0 | | 70 | °C |

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 11. In the JG package, SN75476 through SN75479 chips are glass-mounted.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $I_I$ = −12 mA | | | −0.95 | −1.5 | V |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.5 V, $V_{IL}$ = 0.8 V, | $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | 1 | 100 | μA |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 4.5 V, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V | $I_{OL}$ = 100 mA | | 0.16 | 0.3 | V |
| | | | | $I_{OL}$ = 175 mA | | 0.22 | 0.5 | |
| | | | | $I_{OL}$ = 300 mA | | 0.33 | 0.6 | |
| $V_{(BR)O}$ | Output breakdown voltage | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = 100 μA | 70 | 100 | | V |
| $V_{R(K)}$ | Output clamp diode reverse voltage | | $V_{CC}$ = 4.5 V, | $I_R$ = 100 μA | 70 | 100 | | V |
| $V_{F(K)}$ | Output clamp diode forward voltage | | $V_{CC}$ = 4.5 V, | $I_F$ = 300 mA | 0.8 | 1.15 | 1.6 | V |
| $I_{IH}$ | High-level input current | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | 0.01 | 10 | μA |
| $I_{IL}$ | Low-level input current | A input | $V_{CC}$ = 5.5 V, | $V_I$ = 0.8 V | | −80 | −110 | μA |
| | | Strobe S | | | | −160 | −220 | |
| $I_{CCH}$ | Supply current, outputs high | SN75476 | $V_{CC}$ = 5.5 V | $V_I$ = 5 V | | 10 | 17 | mA |
| | | SN75477 | | $V_I$ = 0 | | 10 | 17 | |
| | | SN75478 | | $V_I$ = 5 V | | 10 | 17 | |
| | | SN75479 | | $V_I$ = 0 | | 10 | 17 | |
| $I_{CCL}$ | Supply current, outputs low | SN75476 | $V_{CC}$ = 5.5 V | $V_I$ = 0 | | 54 | 75 | mA |
| | | SN75477 | | $V_I$ = 5 V | | 54 | 75 | |
| | | SN75478 | | $V_I$ = 0 | | 54 | 75 | |
| | | SN75479 | | $V_I$ = 5 V | | 54 | 75 | |

†All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.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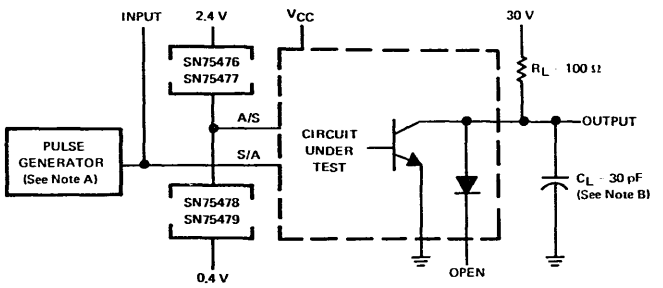
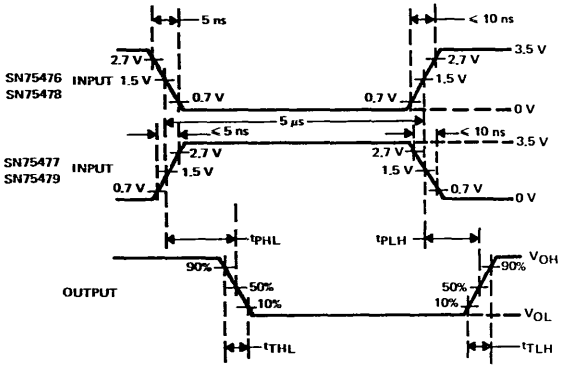
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | SN75476 | | | SN75477 | | | SN75478 | | | SN75479 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $C_L$ = 30 pF, $R_L$ = 100 Ω, See Figure 1 | | 100 | 200 | | 100 | 200 | | 100 | 200 | | 100 | 200 | ns |
| $t_{PHL}$ Propagation delay time, high-to-low-level output | | | 200 | 300 | | 200 | 300 | | 200 | 300 | | 200 | 300 | ns |
| $t_{TLH}$ Transition time, low-to-high-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $t_{THL}$ Transition time, high-to-low-level output | | | 50 | 100 | | 50 | 100 | | 50 | 100 | | 50 | 100 | ns |
| $V_{OH}$ High-level output voltage after switching | $V_S$ = 55 V, $I_O \approx$ 300 mA, See Figure 2 | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | $V_S$–18 | | | mV |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

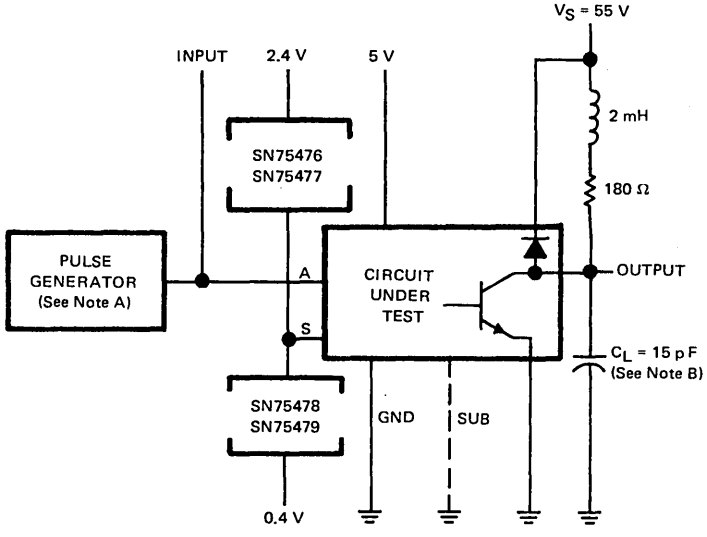



VOLTAGE WAVEFORMS

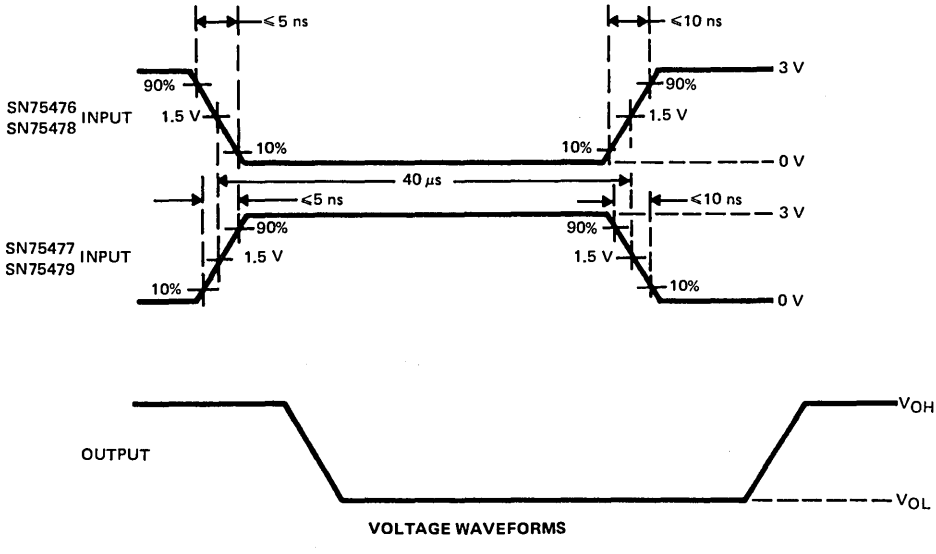
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out}$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.

FIGURE 2–LATCH-UP TEST



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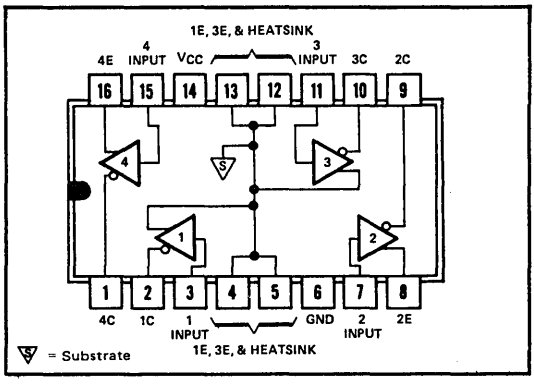
# TYPES UDN2841, UDN2845
# QUADRUPLE HIGH-CURRENT DARLINGTON DRIVERS

BULLETIN NO. DL-S 12791, DECEMBER 1980

- For Use with Negative Supplies
- Current Sink . . . UDN2841
- Sink or Source Combination . . . UDN2845
- Output Current Capability . . . 1.5 A
- High Output-Voltage Capability . . . 50 V
- Preamplifier for High Current Gain
- Inputs Compatible With TTL, DTL, and 5-V CMOS
- Reliable Monolithic Construction
- Designed to be Interchangeable with Sprague UDN2841 and UDN2845

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)

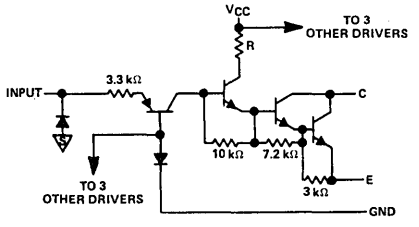



## description

The quadruple darlington switches are monolithic bipolar devices especially designed for high-current, high-voltage peripheral driver applications. The devices are designed to offer solutions to interface problems involving electronic-discharge printers, bipolar and unipolar dc motor drivers, telephone relays, LEDs, PIN diodes, and other high-current loads operating from negative power supplies.

The UDN2841 is intended for current-sink applications with the load connected to ground and the device switching the negative supply. The UDN2845 is a sink and source combination for use in bipolar switching applications where both ends of the load are floating. The UDN2841 and UDN2845 each feature inputs that are compatible with standard TTL, DTL, and 5-volt CMOS signals. The p-n-p input transistor serves as a level translator and the first n-p-n transistor stage is designed to provide sufficient current gain to drive the output darlington-connected pair.

## schematic diagram (each driver)




= Substrate

UDN2841: R = 15 kΩ each channel

UDN2845: R = 15 kΩ channels 1 and 3, R = 1 kΩ, channels 2 and 4

Resistor values shown are nominal.

Driver channels 2 and 4 have uncommitted collectors and emitters while channels 1 and 3 have emitters internally connected to the substrate. For proper operation these emitters and the substrate must be connected to the most-negative supply voltage.

The UDN2841 and UDN2845 are characterized for operation from 0°C to 70°C.

## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

| | |
|---|---|
| Collector-emitter voltage | 50 V |
| Supply voltage, $V_{CC}$ (see Note 1) | 10 V |
| Input voltage | 10 V |
| Substrate voltage | −50 V |
| Peak output current | 1.75 A |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 2075 mW |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | −55°C to 150°C |
| Lead temperature 1/16 inch from case for 10 seconds | 260°C |

NOTES: 1. All voltage values, except collector-emitter voltage, are with respect to the network ground terminal.
2. For operation above 25°C free-temperature, derate to 1328 mW at 70°C at the rate of 16.6 mW/°C.





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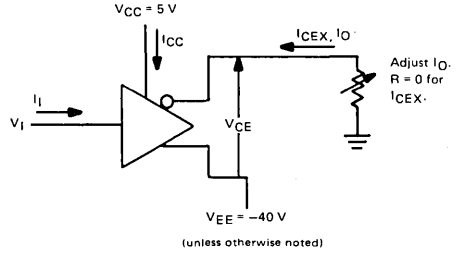
# TYPES UDN2841, UDN2845
# QUADRUPLE HIGH-CURRENT DARLINGTON DRIVERS

## electrical characteristics at 25°C free-air temperature (unless otherwise noted), $V_{CC}$ = 5 V, see figures 1 and 2

| PARAMETER | | TEST CONDITIONS | | UDN2841 | | | UDN2845 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{CEX(sus)}$ | Collector sustaining voltage | $V_{EE}$ = −50 V, $V_I$ = 0.4 V, $I_O$ = 100 mA | | 35 | 50 | | 35 | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | $V_{EE}$ = −50 V, $V_I$ = 0.4 V | | | | 100 | | | 100 | μA |
| | | $V_{EE}$ = −50 V, $V_I$ = 0.4 V, $T_A$ = 70°C | | | | 500 | | | 500 | |
| $I_{I(on)}$ | On-state input current | $I_O$ = 0.5 A | Drivers 1 and 3 | | 300 | 500 | | 300 | 500 | μA |
| | | | Drivers 2 and 4 | | 300 | 500 | | 350 | 525 | |
| $V_{I(on)}$ | On-state input voltage | $I_O$ = 1.5 A, See Note 3 | | | | 2.4 | | | 2.4 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_I$ = 2.4 V, See Note 3 | $I_O$ = 0.5 A | | | 1 | | | 1 | V |
| | | | $I_O$ = 1 A | | | 1.25 | | | 1.25 | |
| | | | $I_O$ = 1.5 A | | | 1.6 | | | 1.6 | |
| $I_{CC}$ | Supply current (each driver) | $I_O$ = 0.5 A, See Note 3 | Drivers 1 and 3 | | 2.5 | 3.75 | | 2.5 | 3.75 | mA |
| | | | Drivers 2 and 4 | | 2.5 | 3.75 | | 3.75 | 7.5 | |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, $t_w$ = 10 ms, duty cycle ≤ 10%.

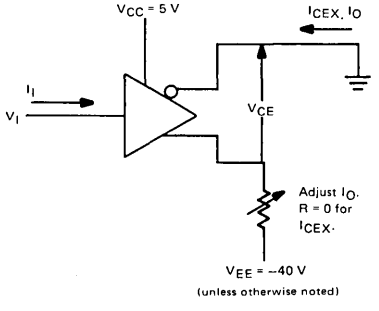
## PARAMETER MEASUREMENT INFORMATION




**TEST CIRCUIT**

NOTE: UDN2841 driver channels 1 through 4 and UDN2845 driver channels 1 and 3 only.

**FIGURE 1 – SINK-CURRENT DRIVER**




**TEST CIRCUIT**

NOTE: UDN2845 driver channels 2 and 4 only

**FIGURE 2 – SOURCE-CURRENT DRIVER**

## THERMAL INFORMATION

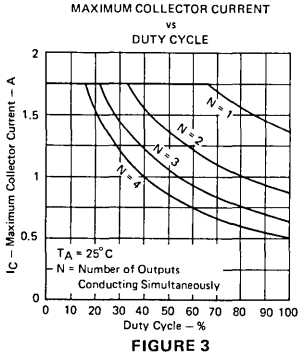



**FIGURE 3**

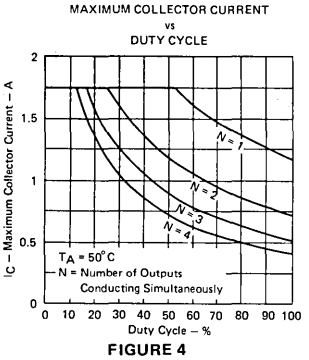



**FIGURE 4**

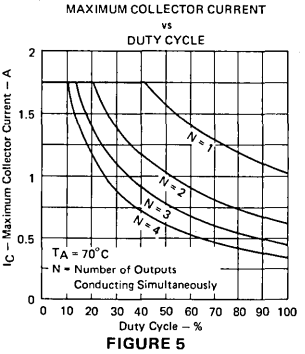



**FIGURE 5**



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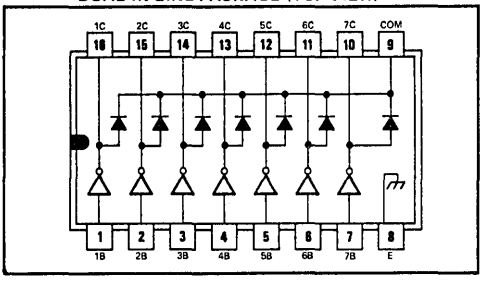
# TYPES ULN2001A THRU ULN2005A DARLINGTON TRANSISTOR ARRAYS

BULLETIN NO. DL-S 12467, DECEMBER 1976 – REVISED DECEMBER 1980

## HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500 mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Designed to be Interchangeable with Sprague ULN2001A Series

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

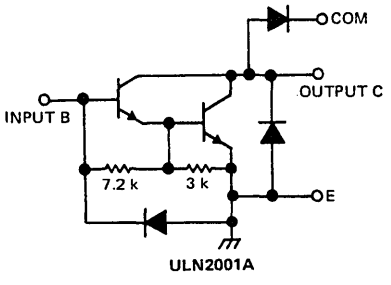



### description

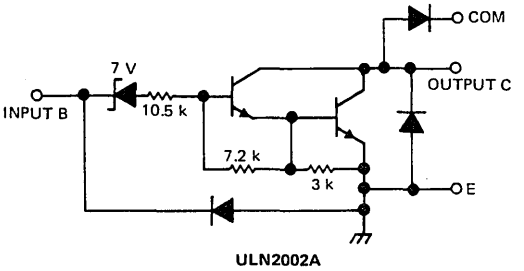
The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current darlington transistor arrays. Each comprises seven n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single darlington pair is 500 milliamperes. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-volt (otherwise interchangeable) versions, see the SN75465 through SN75469.

The ULN2001A is a general-purpose array and may be used with DTL, TTL, P-MOS, CMOS, etc. The ULN2002A is specifically designed for use with 14- to 25-volt P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor to each darlington pair. This allows operation directly with TTL or 5-volt CMOS. The ULN2004A has an appropriate series input resistor to allow its operation directly from CMOS or P-MOS utilizing supply voltages of 6 to 15 volts. The required input current is below that of the ULN2003A while the required voltage is less than that required by the ULN2002A. The ULN2005A has a 1.05-kΩ series base resistor and is especially designed for use with TTL where higher output current is required and loading of the driving source is not a concern.

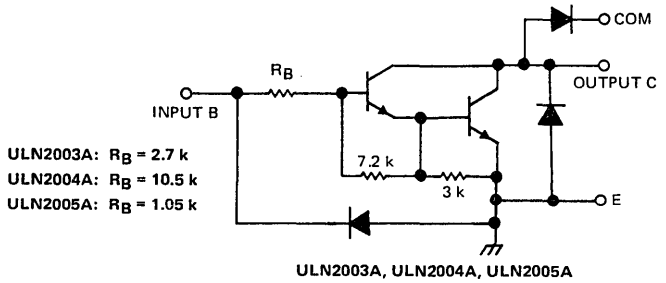
### schematics (each darlington pair)




ULN2001A




ULN2002A




ULN2003A: $R_B$ = 2.7 k
ULN2004A: $R_B$ = 10.5 k
ULN2005A: $R_B$ = 1.05 k

ULN2003A, ULN2004A, ULN2005A

All resistor values shown are nominal and in ohms.

## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage . . . . . 50 V
Input voltage (see Note 1): ULN2002A, ULN2003A, ULN2004A . . . . . 30 V
ULN2005A . . . . . 15 V
Peak collector current (see Figures 14 and 15) . . . . . 500 mA
Continuous input current, ULN2001A only . . . . . 25 mA
Total substrate-terminal current: J package . . . . . −500 mA
N package . . . . . −2.5 A
Continuous dissipation (total package) at (or below)
25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds, J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds, N package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal, E.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 11. In the J package, ULN2001A through ULN2005A chips are glass-mounted.

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | ULN2001A | | | ULN2002A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 50 | | | 50 | μA |
| | | | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 100 | | | 100 | |
| | | 2 | $T_A$ = 70°C | $V_I$ = 6 V | | | | | | 500 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, $T_A$ = 70°C | $I_C$ = 500 μA, | 50 | 65 | | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 17 V | | | | | | 0.82 | 1.25 | mA |
| $h_{FE}$ | Static forward current transfer ratio | 5 | $V_{CE}$ = 2 V, | $I_C$ = 350 mA | 1000 | | | | | | |
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE}$ = 2 V, | $I_C$ = 300 mA | | | | | | 13 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | V |
| | | | $I_I$ = 350 μA, | $I_C$ = 200 mA | | 1.0 | 1.3 | | 1.0 | 1.3 | |
| | | | $I_I$ = 500 μA, | $I_C$ = 350 mA | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 50 V | | | | 50 | | | 50 | μA |
| | | | $V_R$ = 50 V, | $T_A$ = 70°C | | | 100 | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 350 mA | | | 1.7 | 2 | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | 15 | 25 | | 15 | 25 | pF |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## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | ULN2003A MIN | ULN2003A TYP | ULN2003A MAX | ULN2004A MIN | ULN2004A TYP | ULN2004A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 50 | | | 50 | μA |
| | | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | 100 | | | 100 | |
| | | 2 | $T_A$ = 70°C | $V_I$ = 1 V | | | | | | 500 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, $T_A$ = 70°C | $I_C$ = 500 μA, | 50 | 65 | | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 3.85 V | | | 0.93 | 1.35 | | | | mA |
| | | 4 | $V_I$ = 5 V | | | | | | 0.35 | 0.5 | |
| | | 4 | $V_I$ = 12 V | | | | | | 1.0 | 1.45 | |
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE}$ = 2 V | $I_C$ = 125 mA | | | | | | 5 | V |
| | | 6 | | $I_C$ = 200 mA | | | 2.4 | | | 6 | |
| | | 6 | | $I_C$ = 250 mA | | | 2.7 | | | | |
| | | 6 | | $I_C$ = 275 mA | | | | | | 7 | |
| | | 6 | | $I_C$ = 300 mA | | | 3 | | | | |
| | | 6 | | $I_C$ = 350 mA | | | | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | 0.9 | 1.1 | | 0.9 | 1.1 | |
| | | 5 | $I_I$ = 350 μA, | $I_C$ = 200 mA | | 1.0 | 1.3 | | 1.0 | 1.3 | |
| | | 5 | $I_I$ = 500 μA, | $I_C$ = 350 mA | | 1.2 | 1.6 | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 50 V, | | | | 50 | | | 50 | μA |
| | | 7 | $V_R$ = 50 V, | $T_A$ = 70°C | | | 100 | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 305 mA | | | 1.7 | 2 | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | 15 | 25 | | 15 | 25 | pF |

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | | ULN2005A MIN | ULN2005A TYP | ULN2005A MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0 | | | | 50 | μA |
| | | 1 | $V_{CE}$ = 50 V, | $I_I$ = 0, | $T_A$ = 70°C | | | 100 | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE}$ = 50 V, | $I_C$ = 500 μA, | $T_A$ = 70°C | 50 | 65 | | μA |
| $I_I$ | Input current | 4 | $V_I$ = 3 V | | | | 1.5 | 2.4 | mA |
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE}$ = 2 V, | $I_C$ = 350 mA | | | | 2.4 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 250 μA, | $I_C$ = 100 mA | | | 0.9 | 1.1 | V |
| | | 5 | $I_I$ = 350 μA, | $I_C$ = 200 mA | | | 1.0 | 1.3 | |
| | | 5 | $I_I$ = 500 μA, | $I_C$ = 350 mA | | | 1.2 | 1.6 | |
| $I_R$ | Clamp diode reverse current | 7 | $V_R$ = 50 V | | | | | 50 | μA |
| | | 7 | $V_R$ = 50 V, | $T_A$ = 70°C | | | | 100 | |
| $V_F$ | Clamp diode forward voltage | 8 | $I_F$ = 350 mA | | | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | | $V_I$ = 0 V, | f = 1 MHz | | | 15 | 25 | pF |

## switching characteristics at 25°C free-air temperature

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 9 | | 0.25 | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 0.25 | 1 | μs |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 50 V, $I_O$ ≈ 300 mA, See Figure 10 | $V_S$–20 | | | mV |

## PARAMETER MEASUREMENT INFORMATION

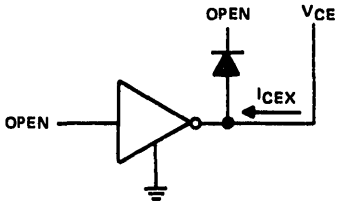



FIGURE 1–$I_{CEX}$

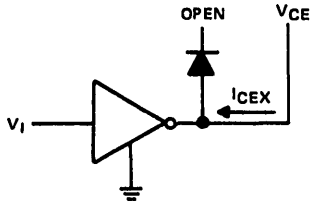



FIGURE 2–$I_{CEX}$

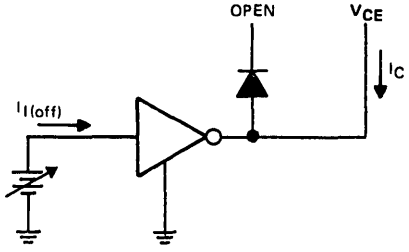



FIGURE 3–$I_{I(off)}$

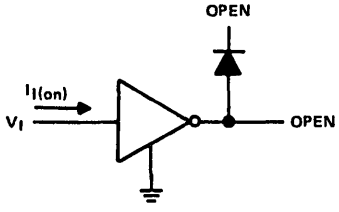
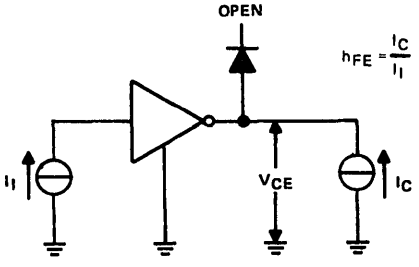



FIGURE 4–$I_I$




NOTE: $I_I$ is fixed for measuring $V_{CE(sat)}$, variable for measuring $h_{FE}$.

FIGURE 5–$h_{FE}$, $V_{CE(sat)}$

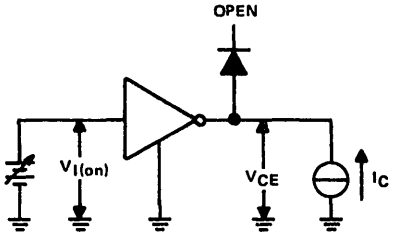



FIGURE 6–$V_{I(on)}$

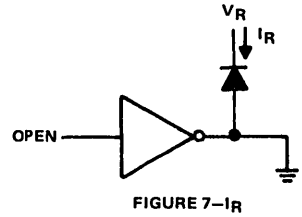



FIGURE 7–$I_R$

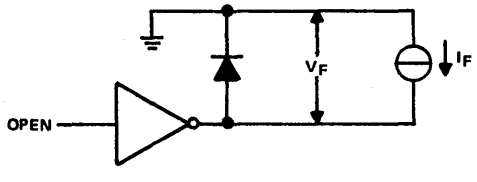



FIGURE 8–$V_F$



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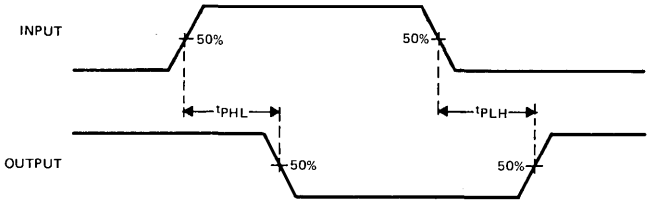
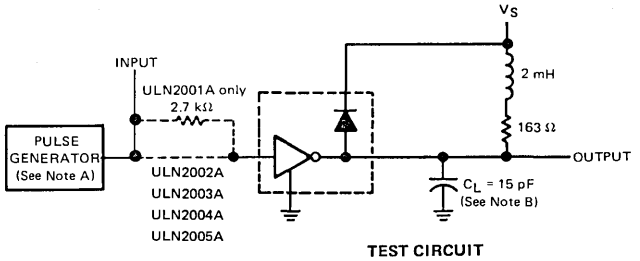
## PARAMETER MEASUREMENT INFORMATION

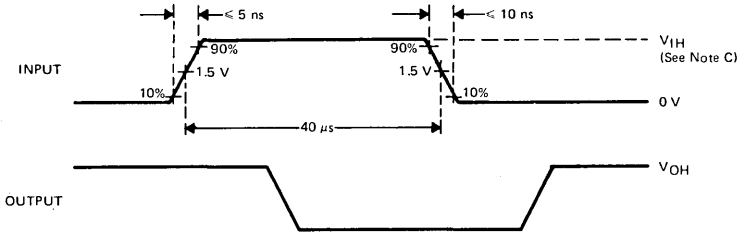



VOLTAGE WAVEFORMS

FIGURE 9–PROPAGATION DELAY TIMES




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} \approx 50\ \Omega$.
B. $C_L$ includes probe and jig capacitance.
C. For testing the ULN2001A, ULN2003A and the ULN2005A, $V_{IH}$ = 3 V; for the ULN2002A, $V_{IH}$ = 13 V; for the ULN2004A, $V_{IH}$ = 8 V.

FIGURE 10–LATCH-UP TEST

## TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

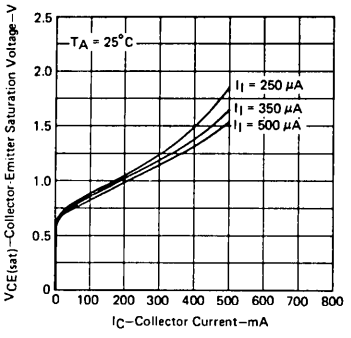



FIGURE 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

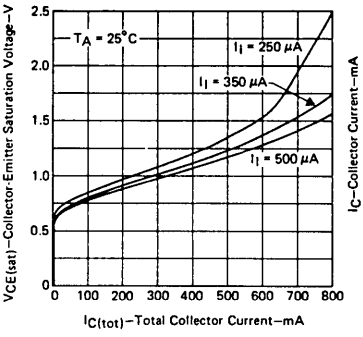



FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

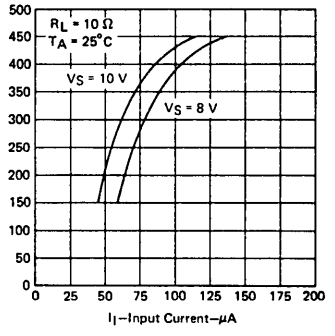



FIGURE 13

## THERMAL INFORMATION

J PACKAGE
MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

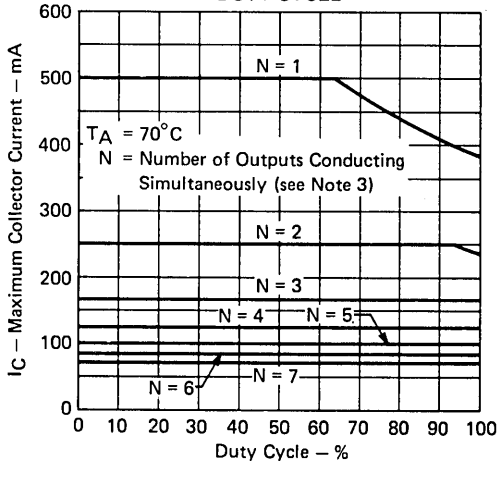



FIGURE 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

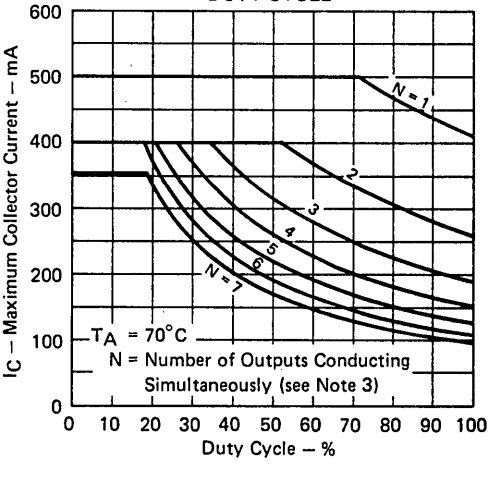



FIGURE 15

NOTE 3: For the J package, N x $I_C$ must not exceed 500 mA (maximum substrate-terminal current). For the N package N x $I_C$ must not exceed 2.5 A.



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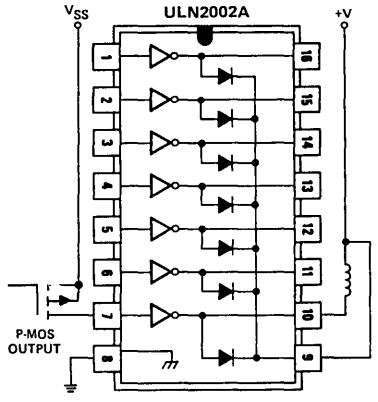
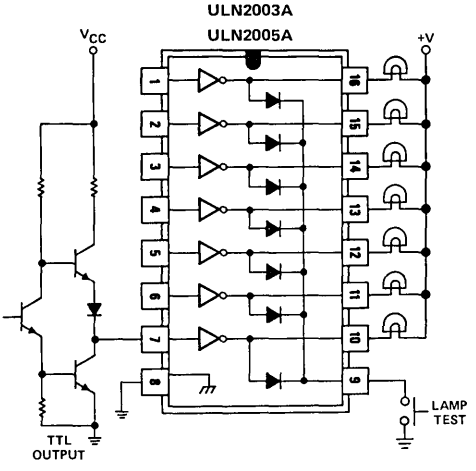
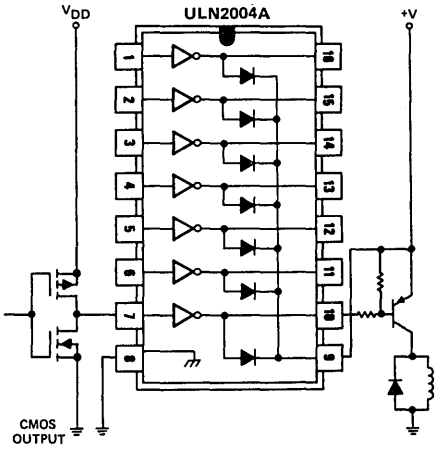
## TYPICAL APPLICATION DATA



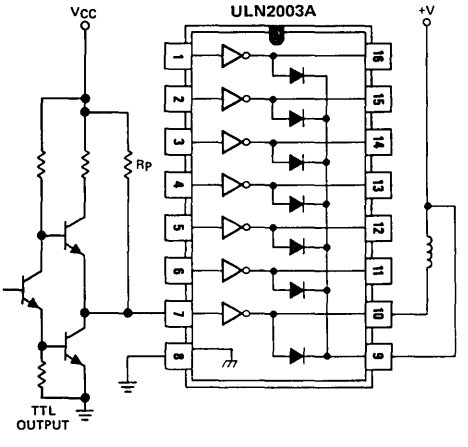

P-MOS TO LOAD




TTL TO LOAD




BUFFER FOR
HIGHER CURRENT LOADS




USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

# UPDATE

FEBRUARY 1981

## ULN2064, ULN2065,ULN2066, ULN2067, ULN2068, ULN2069, ULN2074, ULN2075

The following changes for the ULN2064 thru ULN2069, ULN2074, and ULN2075 are being made to maintain interchangeability with other suppliers. To avoid the duplication of specifications created by these changes, the SN75064 thru SN75069, SN75074, and SN75075 are also being changed as shown below and on the following page.

**revised electrical characteristics for pages 122 and 130**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2064 ULN2074 | | ULN2065 ULN2075 | | ULN2066 | | ULN2067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | 1.1 | | 1.1 | | 1.1 | | 1.1 | | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | 1.2 | | 1.2 | | 1.2 | | 1.2 | | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | 1.3 | | 1.3 | | 1.3 | | 1.3 | | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | 1.4 | | | | 1.4 | | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | 1.5 | | | | 1.5 | | |

**revised electrical characteristics for pages 22 and 30**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75064 SN75074 | | SN75065 SN75075 | | SN75066 | | SN75067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | 1.13 | | 1.13 | | 1.13 | | 1.13 | | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | 1.25 | | 1.25 | | 1.25 | | 1.25 | | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | 1.4 | | 1.4 | | 1.4 | | 1.4 | | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | 1.6 | | | | 1.6 | | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | 1.7 | | | | 1.7 | | |

**revised electrical characteristics for page 126**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2068 | | ULN2069 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.1 | | 1.1 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.2 | | 1.2 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.3 | | 1.3 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.4 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.5 | |

**revised electrical characteristics for page 26**

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | SN75068 | | SN75069 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.13 | | 1.13 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.25 | | 1.25 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.4 | | 1.4 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.6 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.7 | |

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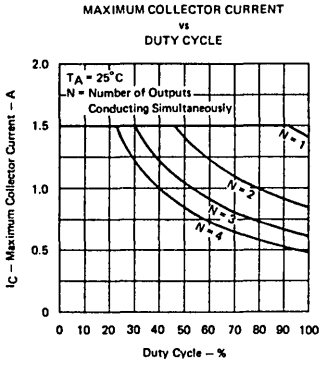
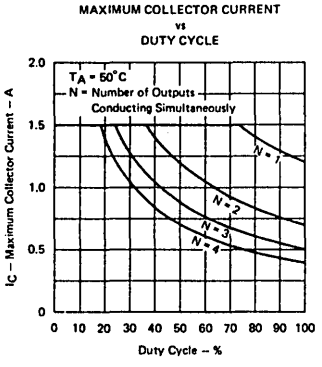
FEBRUARY 1981

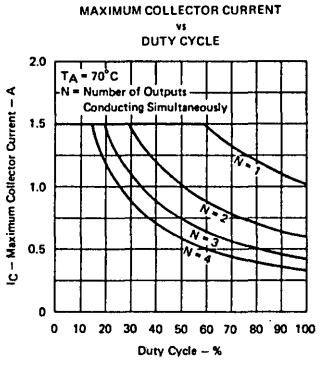
# UPDATE

(continued from previous page)

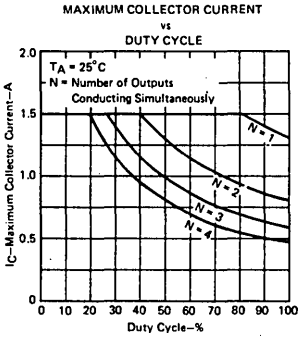
## REVISED THERMAL INFORMATION FOR ULN2064 THRU ULN2069, ULN2074, AND ULN2075
(replaces corresponding data on pages 124, 128, and 132)

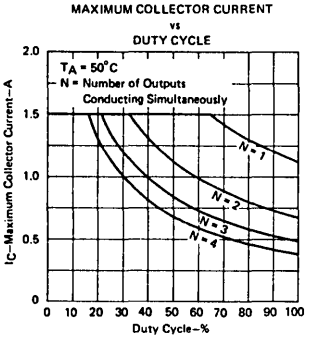


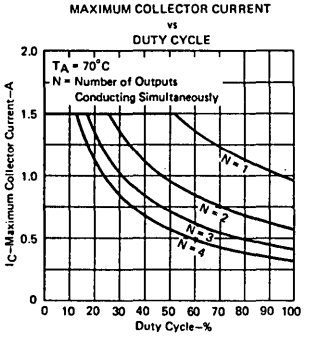




## REVISED THERMAL INFORMATION FOR SN75064 THRU SN75069, SN75074, AND SN75075
(replaces corresponding data on pages 24, 28, and 32)

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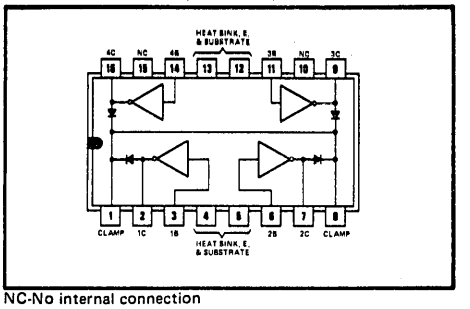
# TYPES ULN2064, ULN2065, ULN2066, ULN2067 QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12681, DECEMBER 1979 – REVISED NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- ULN2064 and ULN2065 Have TTL- and DTL-Compatible Inputs
- ULN2066 and ULN2067 Have CMOS- and PMOS-Compatible Inputs
- Designed for Interchangeability with Sprague ULN2064 thru ULN2067, Respectively

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



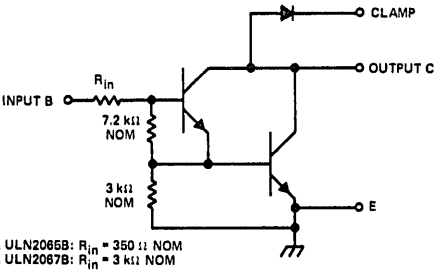

NC-No internal connection

## description

The ULN2064, ULN2065, ULN2066, and ULN2067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The ULN2064 and ULN2065 are intended for use with TTL, DTL, and 5-volt MOS logic. The ULN2066 and ULN2067 are intended for use with PMOS and higher voltage CMOS logic. The ULN2064, ULN2065, ULN2066, and ULN2067 are characterized for operations from 0°C to 70°C.

## schematic (each darlington pair)




ULN2064B, ULN2065B: $R_{in}$ = 350 Ω NOM
ULN2066B, ULN2067B: $R_{in}$ = 3 kΩ NOM

## absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

| | ULN2064 | ULN2065 | ULN2066 | ULN2067 | UNIT |
|---|---|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | 50 | 80 | V |
| Input voltage (see Note 1) | 15 | 15 | 30 | 30 | V |
| Peak collector current (see Figures 12, 13, and 14) | 1.5 | 1.5 | 1.5 | 1.5 | A |
| Input current | 25 | 25 | 25 | 25 | mA |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 2075 | 2075 | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | −55 to 150 | −55 to 150 | −55 to 150 | −55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.





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## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2064 | | ULN2065 | | ULN2066 | | ULN2067 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | 2 | 4.3 | 2 | 4.3 | | | | | mA |
| | | | $V_I$ = 3.75 V | 4.5 | 9.6 | 4.5 | 9.6 | | | | | |
| | | | $V_I$ = 5 V | | | | | 0.9 | 1.8 | 0.9 | 1.8 | |
| | | | $V_I$ = 12 V | | | | | 2.75 | 5.2 | 2.75 | 5.2 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1 A | | 2 | | 2 | | 6.5 | | 6.5 | V |
| | | | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 3 | | 2.5 | | 2.5 | | 10 | | 10 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.13 | | 1.13 | | 1.13 | | 1.13 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.25 | | 1.25 | | 1.25 | | 1.25 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.4 | | 1.4 | | 1.4 | | 1.4 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 3 | | 1.6 | | | | 1.6 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 3 | | | | 1.7 | | | | 1.7 | |
| $I_R$ | Clamp-diode reverse current | 6 | $V_R$ = 50 V | | 50 | | | | 50 | | | μA |
| | | | $V_R$ = 50 V, $T_A$ = 70°C | | 100 | | | | 100 | | | |
| | | | $V_R$ = 80 V | | | | 50 | | | | 50 | |
| | | | $V_R$ = 80 V, $T_A$ = 70°C | | | | 100 | | | | 100 | |
| $V_F$ | Clamp-diode forward voltage | 7 | $I_F$ = 1 A | | 1.75 | | 1.75 | | 1.75 | | 1.75 | V |
| | | | $I_F$ = 1.5 A, See Note 3 | | 2 | | 2 | | 2 | | 2 | |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. $t_w$ = 10 ms, duty cycle ⩽ 10%.

## switching characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 8 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

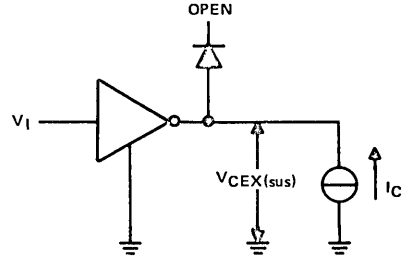


FIGURE 1–$V_{CEX(sus)}$

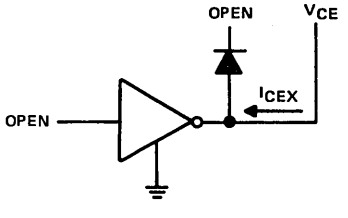


FIGURE 2–$I_{CEX}$



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## PARAMETER MEASUREMENT INFORMATION

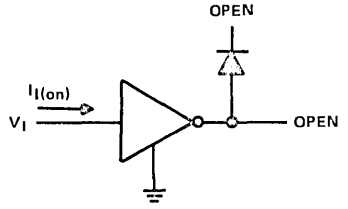



FIGURE 3–$I_{I(on)}$

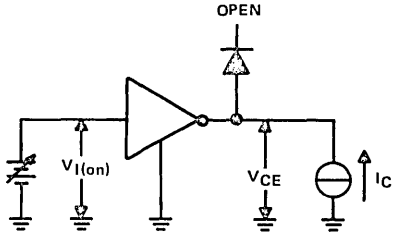



FIGURE 4–$V_{I(on)}$

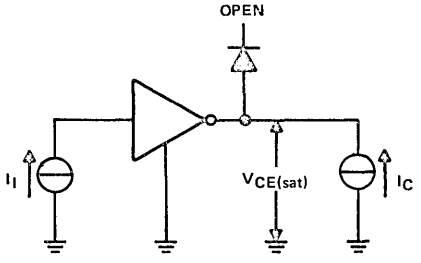



FIGURE 5–$V_{CE(sat)}$

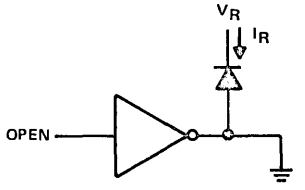



FIGURE 6–$I_R$

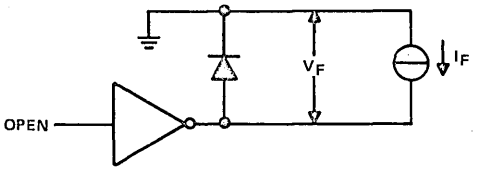
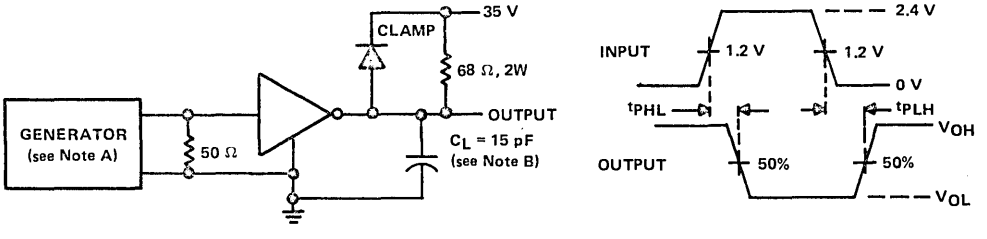



FIGURE 7–$V_F$




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_o$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 8 – SWITCHING TIMES

## ELECTRICAL CHARACTERISTICS

**ULN2064, ULN2065**

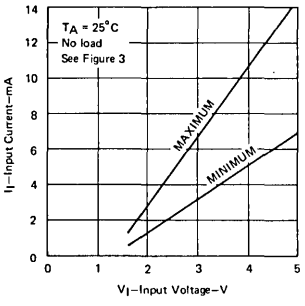



FIGURE 9

**ULN2066, ULN2067**

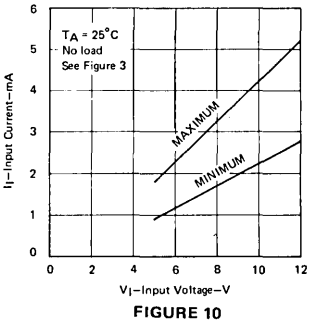



FIGURE 10

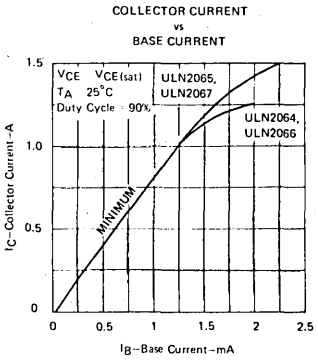



FIGURE 11

## THERMAL INFORMATION

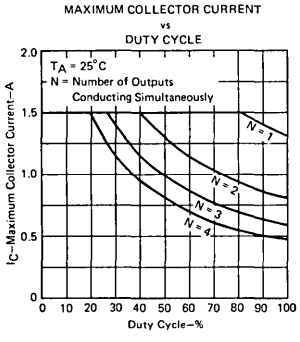



FIGURE 12

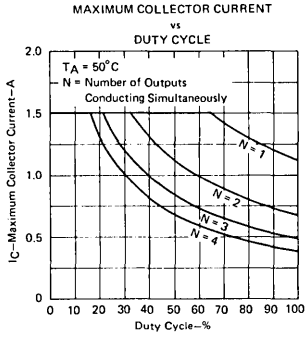



FIGURE 13

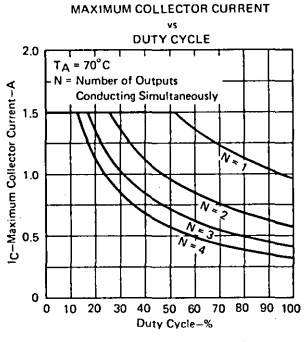



FIGURE 14

## TYPICAL APPLICATION DATA

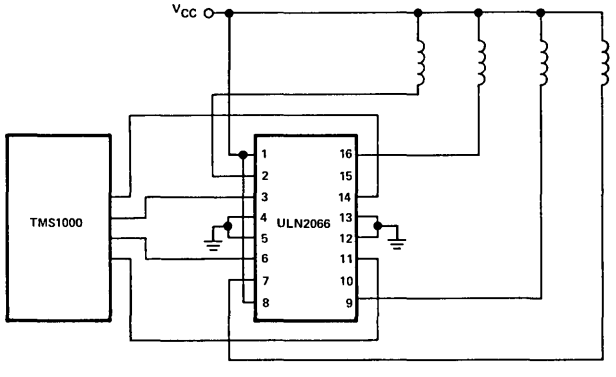



FIGURE 15–RELAY DRIVER INTERFACE



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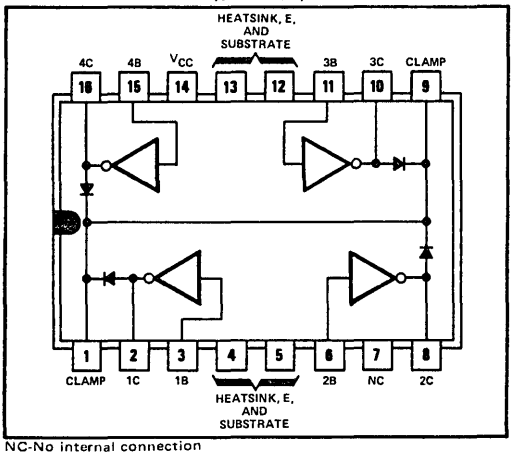
# TYPES ULN2068, ULN2069
# QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12751, MAY 1980—REVISED NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible with TTL and 5-Volt CMOS
- Designed for Interchangeability with Sprague ULN2068 and ULN2069

NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)



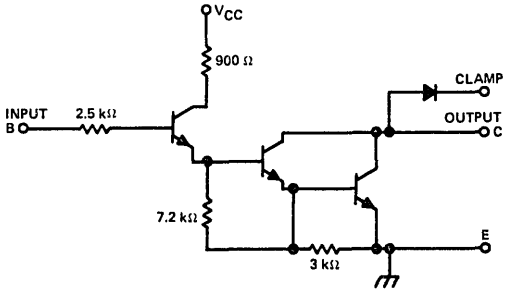

NC-No internal connection

## description

The ULN2068 and ULN2069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-volt CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The ULN2068 and ULN2069 can sink up to 1.5 amperes per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge). The ULN2068 and ULN2069 are characterized for operation from 0°C to 70°C.

## schematic (each switch)




Resistor values shown are nominal.

## absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

| | ULN2068 | ULN2069 | UNIT |
|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | V |
| Supply voltage, $V_{CC}$ (see Note 1) | 10 | 10 | V |
| Input voltage | 15 | 15 | V |
| Peak collector current (see Figures 10, 11, and 12) | 1.5 | 1.5 | A |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 2) | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | −55 to 150 | −55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | °C |

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.





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## electrical characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2068 MIN | ULN2068 MAX | ULN2069 MIN | ULN2069 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | | 250 | | 250 | μA |
| | | | $V_I$ = 3.75 V | | 1000 | | 1000 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 3 | | 2.4 | | 2.4 | V |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 1.13 | | 1.13 | V |
| | | | $V_I$ = 2.4 V, $I_C$ = 750 mA | | 1.25 | | 1.25 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1 A | | 1.4 | | 1.4 | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.25 A, See Note 3 | | 1.6 | | | |
| | | | $V_I$ = 2.4 V, $I_C$ = 1.5 A, See Note 3 | | | | 1.7 | |
| $I_R$ | Clamp-diode reverse current | 6 | $V_R$ = 50 V | | 50 | | | μA |
| | | | $V_R$ = 50 V, $T_A$ = 70°C | | 100 | | | |
| | | | $V_R$ = 80 V | | | | 50 | |
| | | | $V_R$ = 80 V, $T_A$ = 70°C | | | | 100 | |
| $V_F$ | Clamp-diode forward voltage | 7 | $I_F$ = 1 A | | 1.75 | | 1.75 | V |
| | | | $I_F$ = 1.5 A, See Note 3 | | 2 | | 2 | |
| $I_{CC}$ | Supply current (only one switch conducting) | 8 | $V_I$ = 2.4 V, $I_C$ = 500 mA | | 6 | | 6 | mA |

NOTE 3: These parameters must be measured on one output at a time using pulse techniques. $t_w$ = 10 ms, duty cycle ≤ 10%.

## switching characteristics at 25°C free-air temperature, $V_{CC}$ = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 9 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

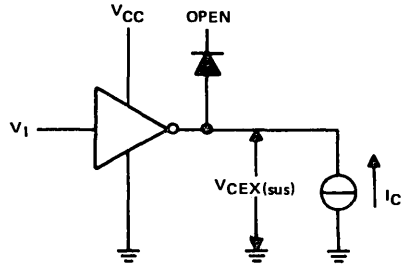


FIGURE 1–$V_{CEX(sus)}$

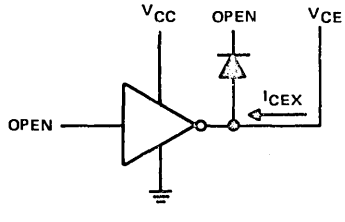


FIGURE 2–$I_{CEX}$



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## PARAMETER MEASUREMENT INFORMATION

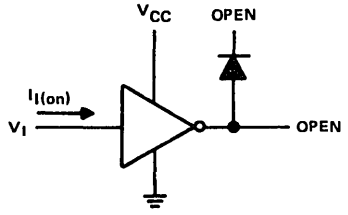



FIGURE 3–$I_{I(on)}$

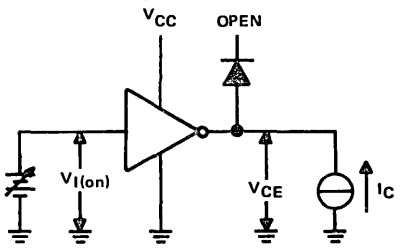



FIGURE 4–$V_{I(on)}$

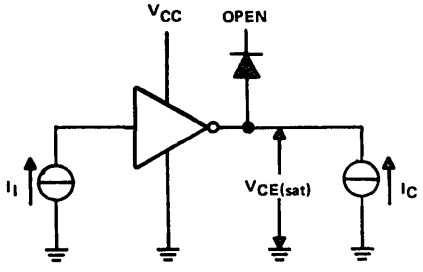



FIGURE 5–$V_{CE(sat)}$

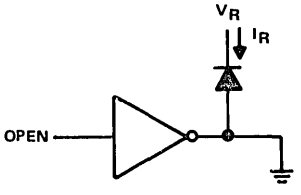



FIGURE 6–$I_R$

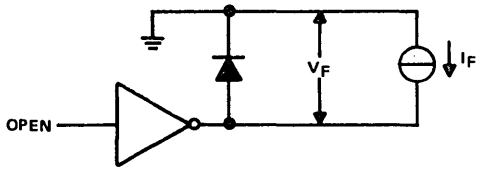



FIGURE 7–$V_F$

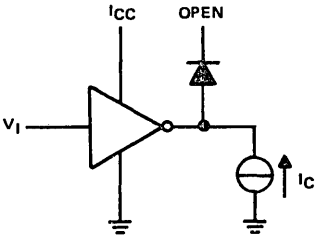
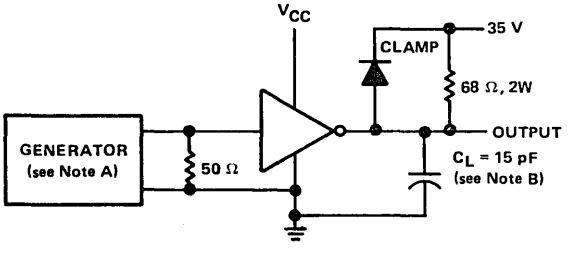
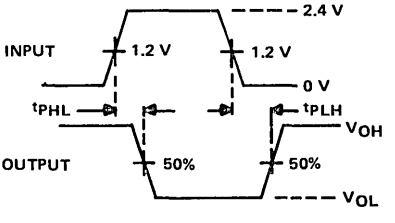



FIGURE 8–$I_{CC}$




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_o$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 9–SWITCHING TIMES

## THERMAL INFORMATION

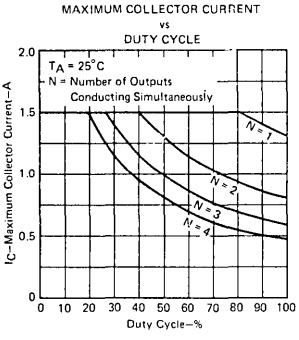



FIGURE 10

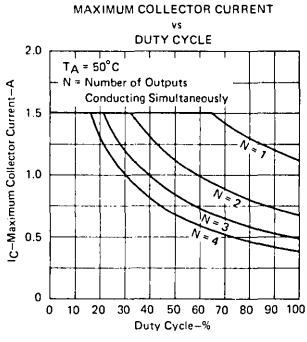



FIGURE 11

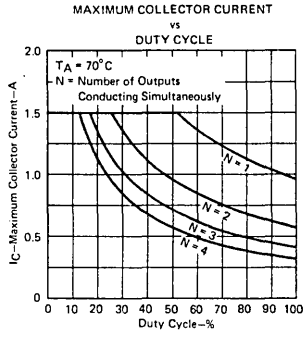



FIGURE 12

## TYPICAL APPLICATION DATA

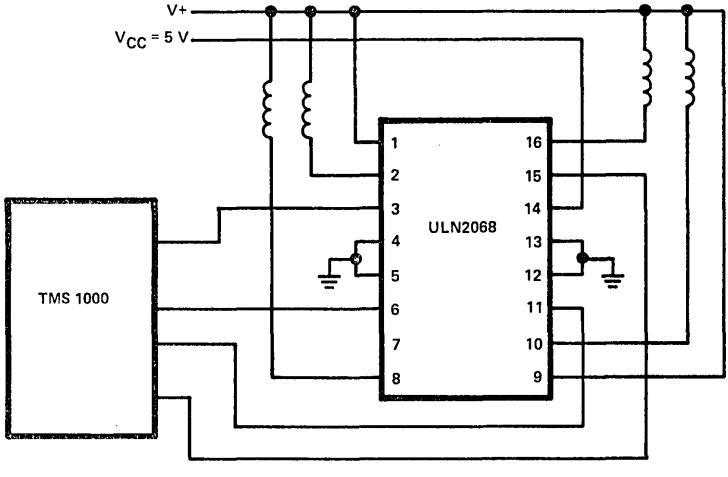



FIGURE 13–RELAY DRIVER INTERFACE



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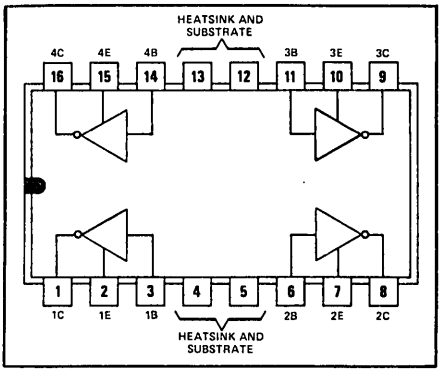
# TYPES ULN2074, ULN2075
# QUADRUPLE HIGH-CURRENT DARLINGTON SWITCHES

BULLETIN NO. DL-S 12750, MAY 1980—REVISED NOVEMBER 1980

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible With TTL or 5-V CMOS
- Designed for Interchangeability with Sprague ULN2074 and ULN2075

• NE
DUAL-IN-LINE PACKAGE
(TOP VIEW)




## description

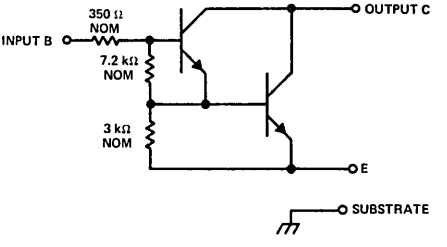
The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 amperes for each darlington pair.

The ULN2074 and ULN2075 are unique general-purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

For proper operation, the substrate must be connected to the most negative voltage.

The ULN2074 and ULN2075 are characterized for operation from 0°C to 70°C.

## schematic (each switch)




## absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

| | ULN2074 | ULN2075 | UNIT |
|---|---|---|---|
| Collector-emitter voltage | 50 | 80 | V |
| Input voltage with respect to substrate | 30 | 60 | V |
| Peak collector current (see Figures 9, 10, and 11) | 1.5 | 1.5 | A |
| Input current | 25 | 25 | mA |
| Total power dissipation at (or below) 25°C free-air temperature (see Note 1) | 2075 | 2075 | mW |
| Operating free-air temperature range | 0 to 70 | 0 to 70 | °C |
| Storage temperature range | −55 to 150 | −55 to 150 | °C |
| Lead temperature 1/16 inch (1,6 mm) from the case for 10 seconds | 260 | 260 | °C |

NOTE 1: For operation above 25°C free-air temperature, derate total power to 1328 mW at 70°C at the rate of 16.6 mW/°C.

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | ULN2074 MIN | ULN2074 MAX | ULN2075 MIN | ULN2075 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{CEX(sus)}$ | Collector sustaining voltage | 1 | $V_I$ = 0.4 V, $I_C$ = 100 mA | 35 | | 50 | | V |
| $I_{CEX}$ | Collector output cutoff current | 2 | $V_{CE}$ = 50 V | | 100 | | | μA |
| | | | $V_{CE}$ = 50 V, $T_A$ = 70°C | | 500 | | | |
| | | | $V_{CE}$ = 80 V | | | | 100 | |
| | | | $V_{CE}$ = 80 V, $T_A$ = 70°C | | | | 500 | |
| $I_{I(on)}$ | On-state input current | 3 | $V_I$ = 2.4 V | 2 | 4.3 | 2 | 4.3 | mA |
| | | | $V_I$ = 3.75 V | 4.5 | 9.6 | 4.5 | 9.6 | |
| $V_{I(on)}$ | On-state input voltage | 4 | $V_{CE}$ = 2 V, $I_C$ = 1 A | | 2 | | 2 | V |
| | | | $V_{CE}$ = 2 V, $I_C$ = 1.5 A, See Note 2 | | 2.5 | | 2.5 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I$ = 625 μA, $I_C$ = 500 mA | | 1.13 | | 1.13 | V |
| | | | $I_I$ = 935 μA, $I_C$ = 750 mA | | 1.25 | | 1.25 | |
| | | | $I_I$ = 1.25 mA, $I_C$ = 1 A | | 1.4 | | 1.4 | |
| | | | $I_I$ = 2 mA, $I_C$ = 1.25 A, See Note 2 | | 1.6 | | | |
| | | | $I_I$ = 2.25 mA, $I_C$ = 1.5 A, See Note 2 | | | | 1.7 | |

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, $t_w$ = 10 ms, duty cycle ≤ 10%.

## switching characteristics at 25°C free-air temperature

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | See Figure 6 | | | 1 | μs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | | 1.5 | μs |

## PARAMETER MEASUREMENT INFORMATION

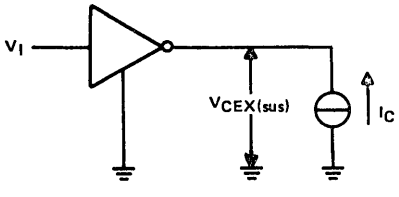



FIGURE 1–$V_{CEX(sus)}$

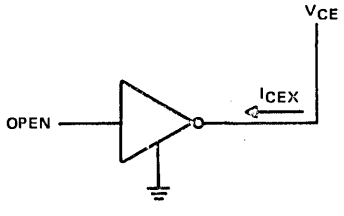



FIGURE 2–$I_{CEX}$



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## PARAMETER MEASUREMENT INFORMATION

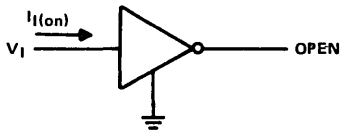



FIGURE 3–$I_{I(on)}$

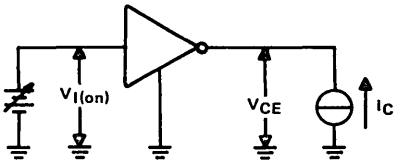



FIGURE 4–$V_{I(on)}$

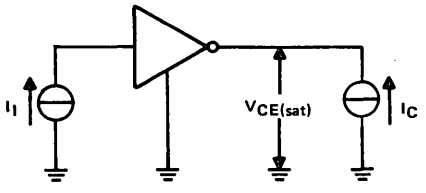
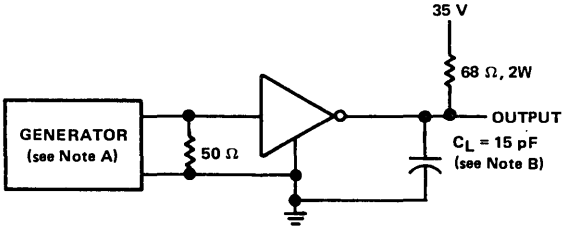
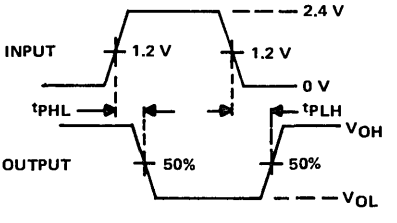



FIGURE 5–$V_{CE(sat)}$




TEST CIRCUITS




VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, $Z_o$ = 50 Ω.
B. $C_L$ includes all probe and stray capacitance.

FIGURE 6–SWITCHING CHARACTERISTIC

## ELECTRICAL CHARACTERISTICS

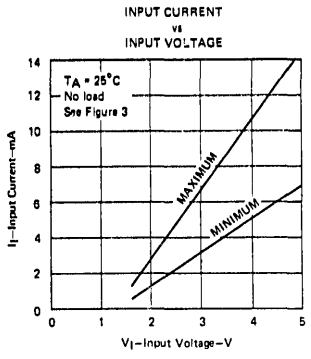



FIGURE 7

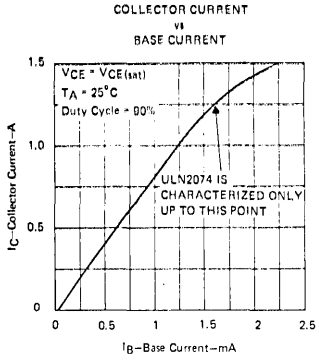



FIGURE 8

## THERMAL INFORMATION

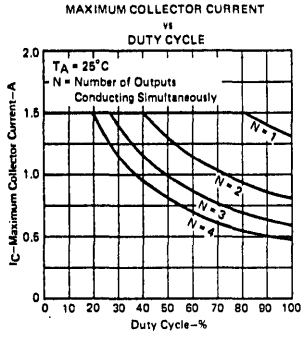



FIGURE 9

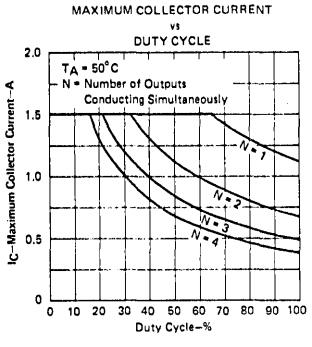



FIGURE 10

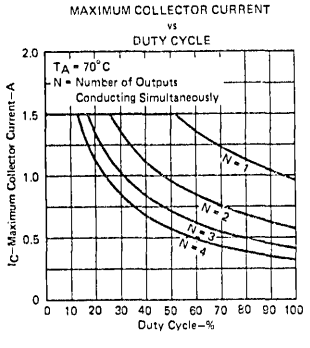



FIGURE 11

## TYPICAL APPLICATION DATA

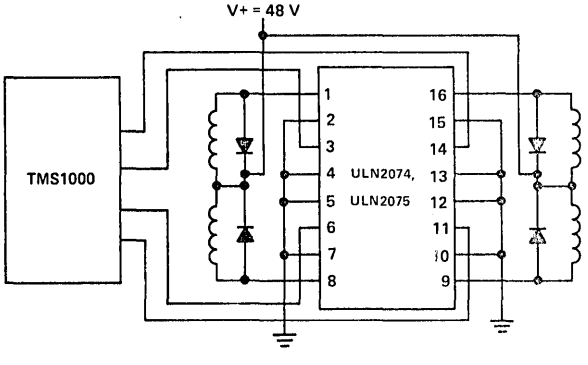



FIGURE 12–RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES



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## general

The applications have been divided into several categories. Even though a particular device is shown in a given application, that does not mean it is the only device that can be used. For example, the SN75451B is shown as a lamp driver. Depending on the voltage and current requirements, other devices may be used such as the SN75401, SN75411, SN75431, SN75461, SN75471, and so forth.

The categories into which the applications have been divided are as follows:

Lamp drivers
Relay/solenoid drivers
Hammer drivers
Core memory driver and inhibit control
Digital comparators
Detectors
TTL-to-MOS and MOS-to-TTL drivers
Inverting buffers for high-current loads
Miscellaneous applications

## lamp drivers

Figures 1 and 2 show basic lamp driver applications.

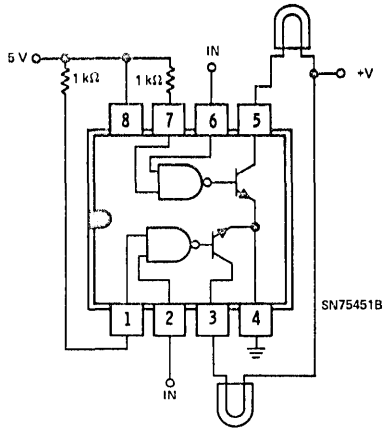


FIGURE 1 – LAMP DRIVER

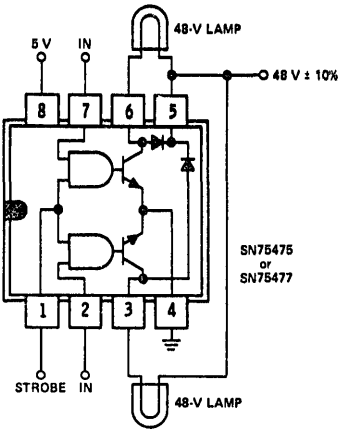


FIGURE 2 – HIGH-VOLTAGE LAMP DRIVER WITH INDUCTIVE CLAMP-DIODE PROTECTION

Note that in any lamp-driver application the turn-on surge current of a cold lamp may be as much as 10 times the normal on current; a 100-mA lamp may have a 1-amp turn-on surge. Peripheral drivers can handle 100-mA operating currents, but a 1-amp surge is far more demanding. The normal maximum continuous collector current rating is 300 or 500 mA, although a 500 or 1000 mA (maximum) surge current may be sustained for duty cycles not to exceed 50% or 40%, respectively, with on time less than 10 milliseconds. Current peaks exceeding these maximums may cause device deterioration.

## lamp drivers (continued)

Several methods can be employed to limit surge currents when using peripheral drivers. These methods allow 200- to 300-mA lamps to be driven without exceeding the surge limits of the devices. One method that can be used employs "keep alive" resistors as shown in Figure 3. These resistors maintain off-state current at approximately 10%. This will reduce the surge current.

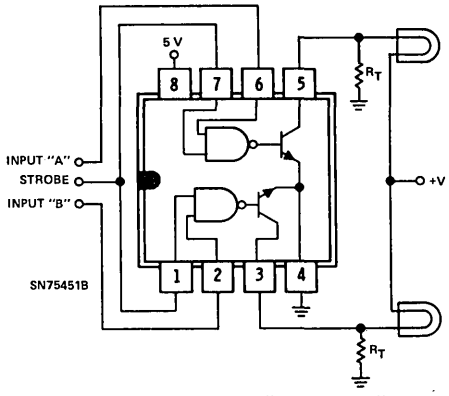


FIGURE 3 – LAMP DRIVERS WITH "KEEP ALIVE" RESISTORS

With the basic SN75450B, SN75460, or SN75470, the availability of the gate output and base leads, as well as the emitter lead, allows use of several methods of current limiting. One method is to place a current-limiting resistor between the gate output and the transistor base, as shown in Figure 4. With an operating load current of 100 mA, a typical $h_{FE}$ of 50 for the output transistor, and selecting 250 mA as the peak surge, the value of the base resistor can be determined from the following equation:

$$R = \frac{V_{OH} - V_{BE}}{I_{B\ (limit)}}$$

where:

$V_{OH}$ = 3.3 V (typical)

$V_{BE}$ = 0.85 V (typical)

$$I_{B\ (limit)} = \frac{I_{C\ (limit)}}{h_{FE}} = \frac{250\ mA}{50} = 5\ mA$$

Therefore:

$$R = \frac{3.3 - 0.85}{0.005} \approx 500\ \Omega$$

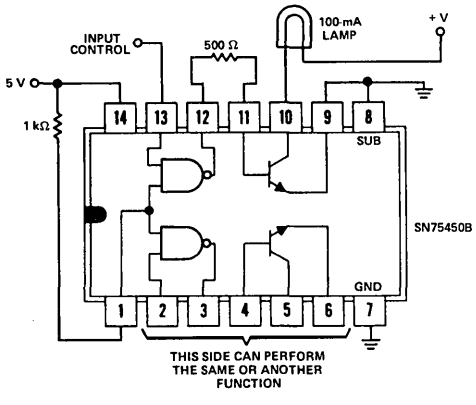


FIGURE 4 – LAMP DRIVER WITH BASE RESISTOR SURGE LIMITING

This method is not the best because of lack of control over critical parameters. A worst-case condition of low $V_{BE}$, high $h_{FE}$, and high gate output would result in peak surges in excess of 500 mA.



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Figure 5 shows a configuration that is less susceptible to variations in parameters. The emitter resistor is small enough to be of little significance at the steady-state on level, but will limit the peak levels. In this example, a GE1815 lamp was used and the actual steady-state current was 191 mA. With a typical gate $V_{OH}$ of 3.3 volts and a $V_{BE}$ of 0.95 volt, (at 200 mA) the transistor will saturate and limit when its emitter voltage reaches $V_{OH} - V_{BE}$, or 2.35 volts; this occurs at $V_E/R_E$, or about 345 mA. Figure 6 shows the output current waveform.

## lamp drivers (continued)

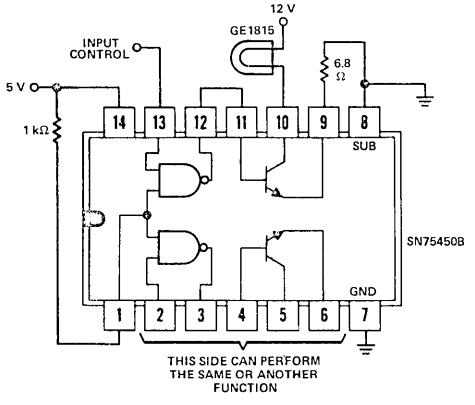



FIGURE 5 – LAMP DRIVER WITH EMITTER RESISTOR SURGE LIMITING

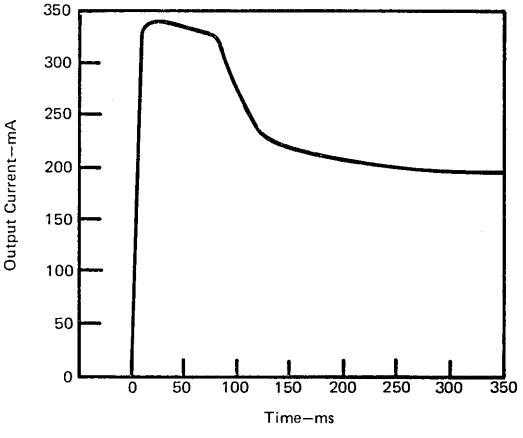



FIGURE 6 – OUTPUT CURRENT vs TIME FOR CIRCUIT IN FIGURE 5

In this example the peak surge is sustained for about 150 milliseconds. As the lamp warms, its impedance rises and the load current drops rapidly to the steady-state level. Even with worst-case parameters the surge current would be under 500 mA. The efficient performance of this type of current limiting explains its popularity for lamp-driver applications.

Improved accuracy and consistent performance can be achieved by utilizing one of the output transistors as a current-sensing device to clamp the lamp driver as shown in Figure 7. In this circuit the lamp current must flow through the 1.9-ohm resistor in the emitter of the lamp driver. The first advantage is that the resistor is smaller than that required in the previous circuit, and has even less effect on the steady-state operating level. The base-emitter junction of Q2 is connected across the 1.9-ohm resistor, with its collector tied to the base of Q1 in a typical current-limiting mode. A $V_{BE}$ of only about 0.6 volt begins to turn Q2 on, clamping the base drive into Q1. Clamping occurs at an output current equal to $V_{BE}/1.9\ \Omega$, or $0.6\ V/1.9\ \Omega$; the output clamp level is then 316 mA. As in the previous application, the surge current lasts for about 100 milliseconds before decreasing rapidly to the quiescent level of 190 to 200 mA.

Two important precautions should be kept in mind when using this type of surge protection; (1) surge currents should not be allowed to exceed the driver surge rating under any conditions; and (2) current limiting must not take place during steady-state operations, as this would increase driver power dissipation and could cause failure.

# TYPICAL APPLICATIONS

## lamp drivers (continued)

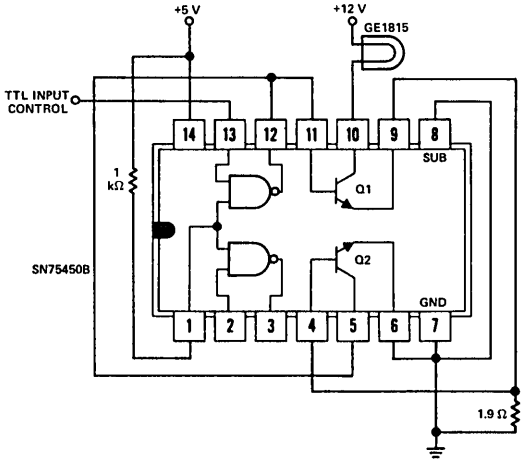



FIGURE 7 – LAMP DRIVER WITH CURRENT-SENSING SURGE PROTECTION

Another method is basically to use two switches; one to turn on the lamp with current limiting and the second to take over, after a delay, without current limiting. This eliminates the effects of parameter variation without reducing the quiescent operating level of the lamp. Such a circuit using the SN75452B is shown in Figure 8. A high-level input turns Q1 on immediately, while Q2 is delayed by the input RC network, allowing about 200 milliseconds of limited-current warm-up before turning the lamp on fully. Figure 9 shows the current levels versus time, and the effect of the warm-up mode on resulting peak levels.

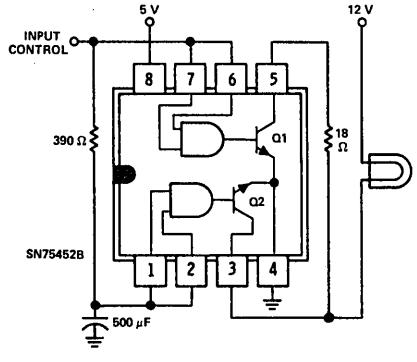



FIGURE 8 – LAMP DRIVER WITH WARM-UP CIRCUIT

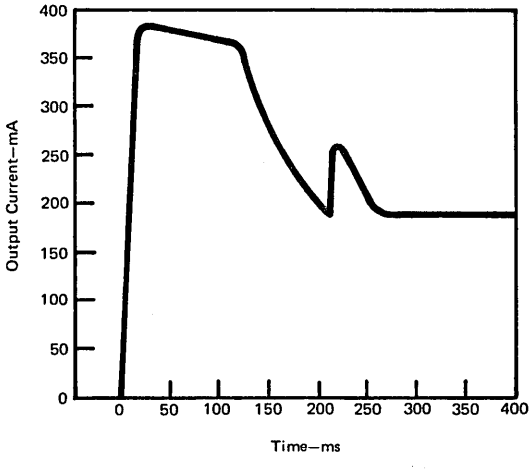



FIGURE 9 – OUTPUT CURRENT vs TIME FOR CIRCUIT IN FIGURE 8

## lamp drivers (continued)

Another interesting lamp-driver application is depicted in Figure 10, showing the SN75450B as a panel-light intensity control. Controllable feedback around the gate allows its operation in the linear region, thus providing variable drive to the output transistor. An emitter resistor as shown may be used to limit initial turn-on surges. In this application a large amount of power will be dissipated in the output transistor at half-power operating levels.

Care must be taken not to exceed the total power-dissipation capability of the drivers. In a typical application the gate output will be only about 2.2 volts because of operation within the linear region. A control setting of about 280 ohms puts the gate in its linear region. A control setting of 100 to 150 ohms turns off the lamp, and a setting of 700 to 800 ohms will yield a full-on condition.

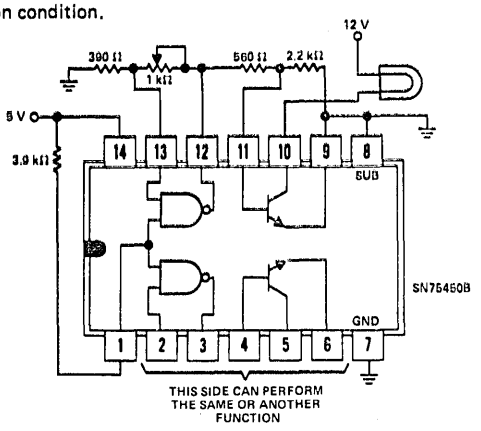



FIGURE 10 – PANEL-LIGHT INTENSITY CONTROL

## relay/solenoid drivers

Figures 11 and 12 show typical relay/solenoid driver applications. Note that when using drivers that do not have output clamp diodes provided internally, these diodes should be provided externally across the inductive load as shown in Figure 12.

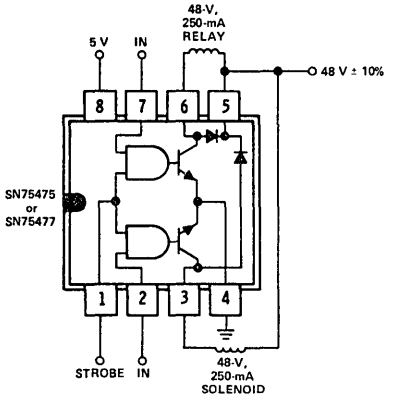



FIGURE 11 – HIGH-VOLTAGE RELAY/SOLENOID DRIVER

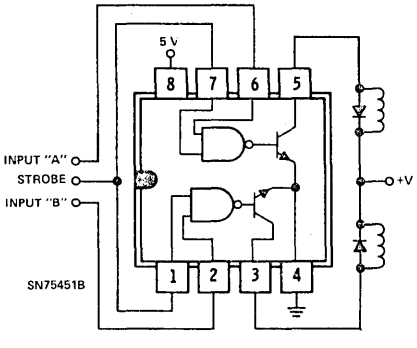



FIGURE 12 – RELAY/SOLENOID DRIVER WITH EXTERNAL CLAMP DIODES

# TYPICAL APPLICATIONS

## relay/solenoid drivers (continued)

In some applications involving the switching of inductive loads, the fast rise time and high-voltage transient occurring during turn-off can force the output transistor into a secondary breakdown condition. In such cases the collector voltage reaches $V_{CC2}$ levels within a few nanoseconds. To prevent undesired breakdown, the collector-voltage slew rate should be reduced to 1 volt per nanosecond or less. This gives the gate sufficient time to provide a low base-to-ground impedance before the collector voltage is extremely high, and collector-to-emitter breakdown is prevented. To accomplish this, a 500- to 1000-pF capacitor from the collector of the output transistor to ground is usually adequate (see Figure 13).

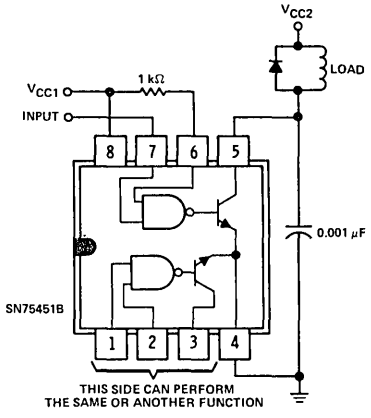



FIGURE 13–CAPACITOR PREVENTS PREMATURE COLLECTOR-TO-EMITTER BREAKDOWN

In some systems, power-supply failure or sequencing may result in the output $V_{CC2}$ collector supply being on while the gate supply $V_{CC1}$ is off. Under this condition the collector-to-emitter breakdown is generally lower because of the increase in base-terminating impedance resulting from the gate being off. Figure 14 shows a practical method of preventing complete loss of gate power while $V_{CC2}$ is on; the zener diode yields a 4- to 5-volt supply level to the gate during $V_{CC1}$ power failure.

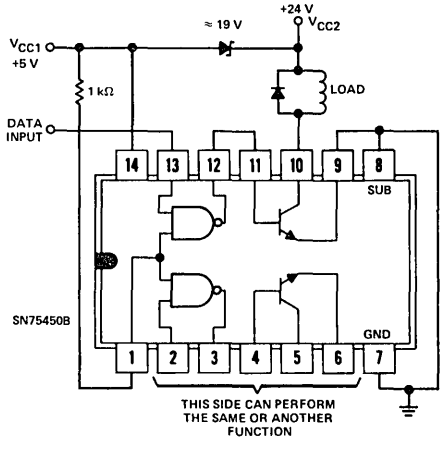



FIGURE 14–PROTECTION AGAINST LOSS OF $V_{CC1}$

## hammer drivers

Figure 15 shows a typical hammer-driver application. If the type of driver used does not have internal output clamp diodes, a 1N3064 or similar diode should be connected across the inductive load in order to provide this protection.

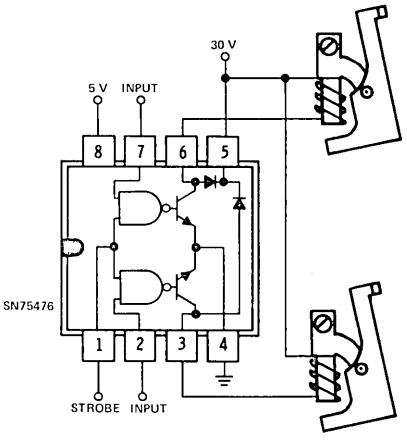
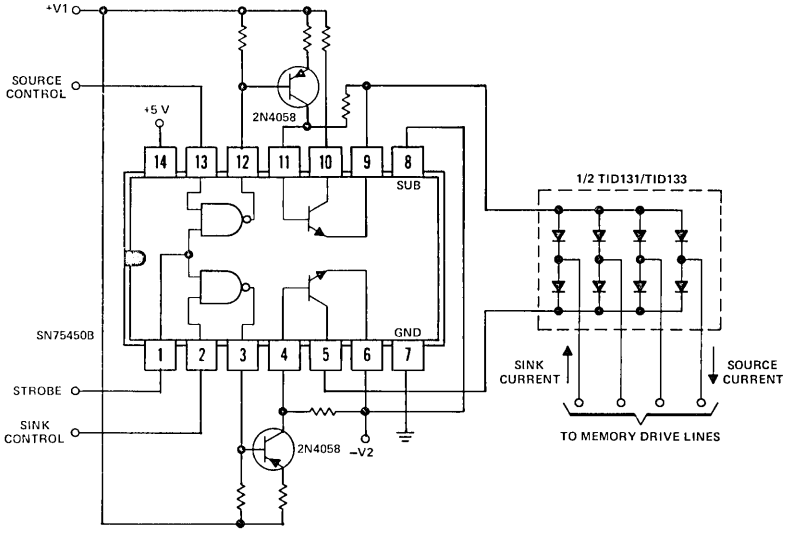



FIGURE 15 – DUAL HAMMER DRIVER

## core memory driver and inhibit control

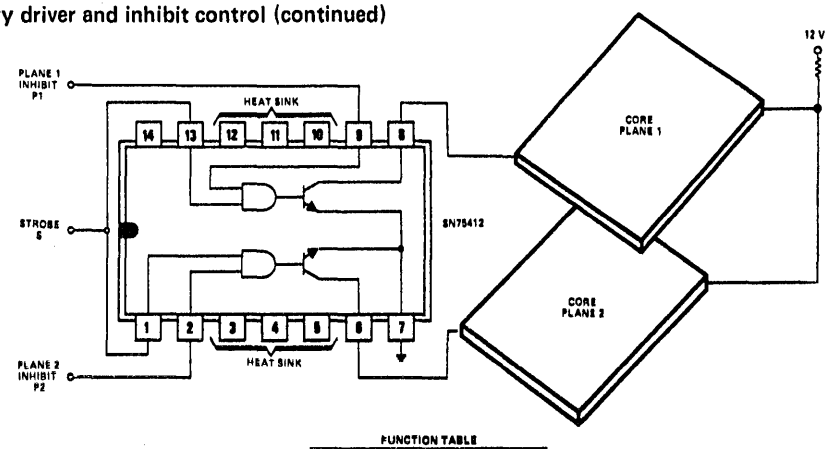



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2$ V)

FIGURE 16 – CORE MEMORY DRIVER

# TYPICAL APPLICATIONS

## core memory driver and inhibit control (continued)




FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| P1 | P2 | S | PLANE 1 | PLANE 2 |
| X | X | L | Enabled | Enabled |
| H | L | H | Inhibited | Enabled |
| L | H | H | Enabled | Inhibited |
| H | H | H | Inhibited | Inhibited |
| L | L | H | Enabled | Enabled |

H = high level, L = low level, X = irrelevant

**FIGURE 17–CORE MEMORY INHIBIT CONTROL**

## digital comparators

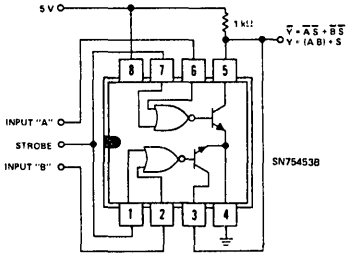



**FIGURE 18–LOGIC SIGNAL COMPARATOR**

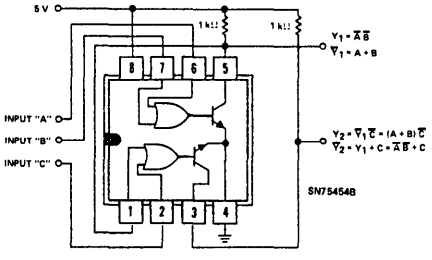



**FIGURE 19–MULTIFUNCTION LOGIC-SIGNAL COMPARATOR**

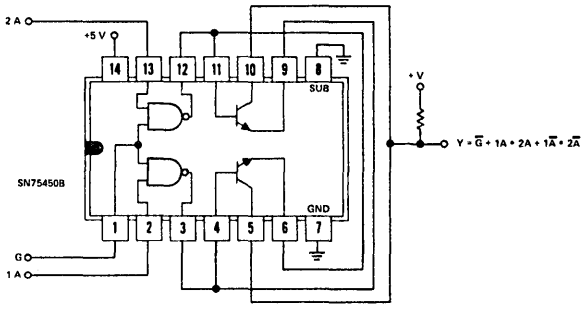



**FIGURE 20–GATED COMPARATOR**



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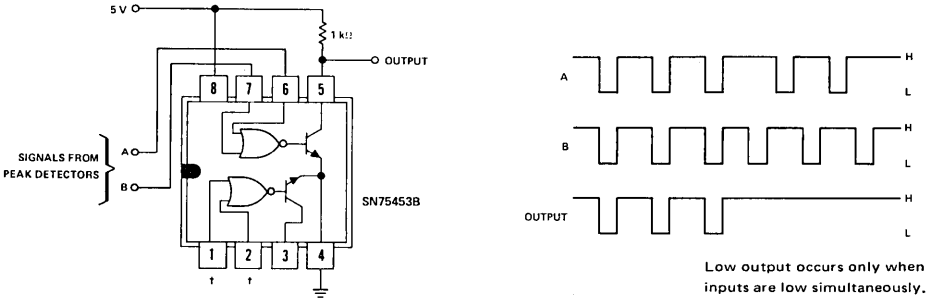
## detectors




Low output occurs only when inputs are low simultaneously.

†If inputs are unused, they should be connected to +5 V through a 1 kΩ resistor.

FIGURE 21—IN-PHASE DETECTOR

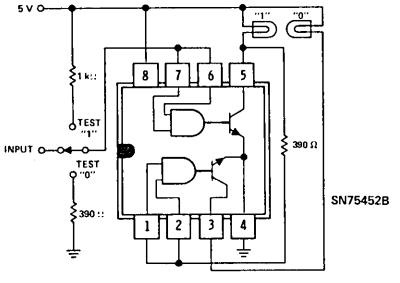
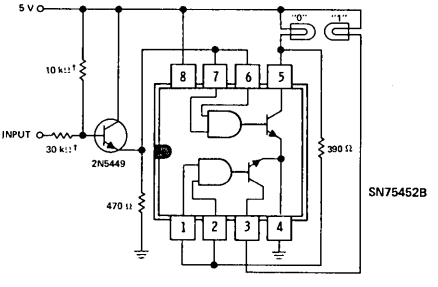



FIGURE 22—TTL OR DTL POSITIVE LOGIC-LEVEL DETECTOR




†The two input resistors must be adjusted for the level of MOS input.

FIGURE 23—MOS NEGATIVE-LOGIC-LEVEL DETECTOR

## TTL-to-MOS and MOS-to-TTL drivers

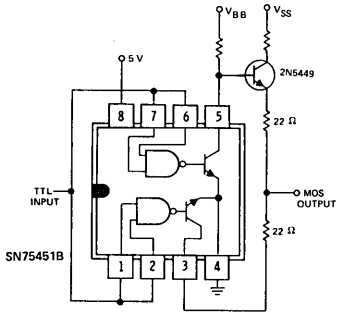
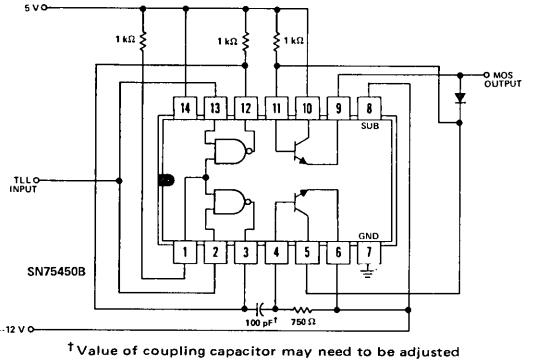



FIGURE 24—TTL-TO-MOS CLOCK DRIVER




†Value of coupling capacitor may need to be adjusted for frequency of operation.

FIGURE 25—TTL-TO-MOS CLOCK DRIVER

# TYPICAL APPLICATIONS

## TTL-to-MOS and MOS-to-TTL drivers (continued)

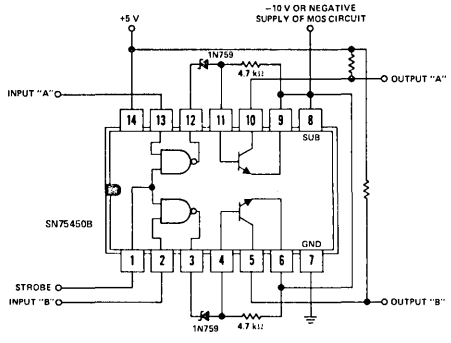



FIGURE 26—DUAL TTL-TO-MOS DRIVER

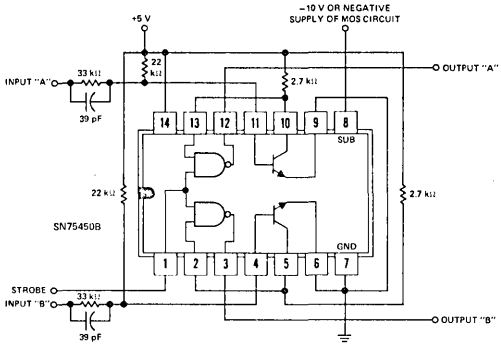



FIGURE 27—DUAL MOS-TO-TTL DRIVER

## inverting buffers for high-current loads

SN75467
or
ULN2002A

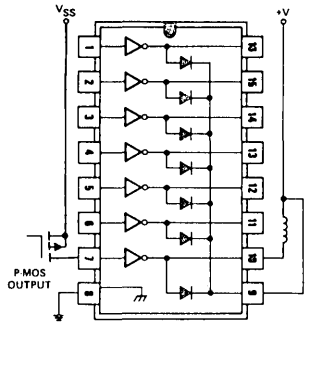



FIGURE 28—P-MOS TO LOAD

SN75468
or
ULN2003A

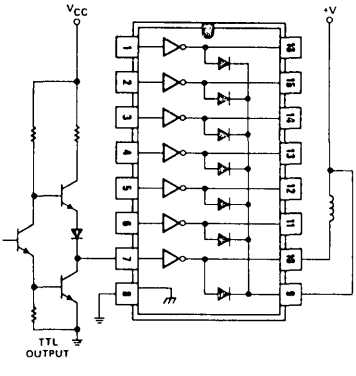



FIGURE 29—TTL TO LOAD

SN75469
or
ULN2004A

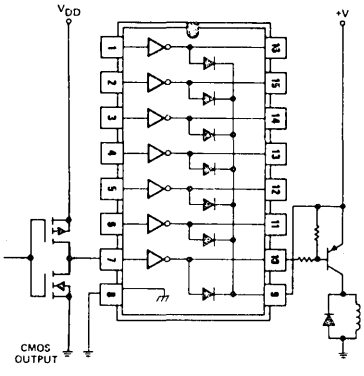



FIGURE 30—CMOS TO HIGHER CURRENT LOAD



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## miscellaneous applications

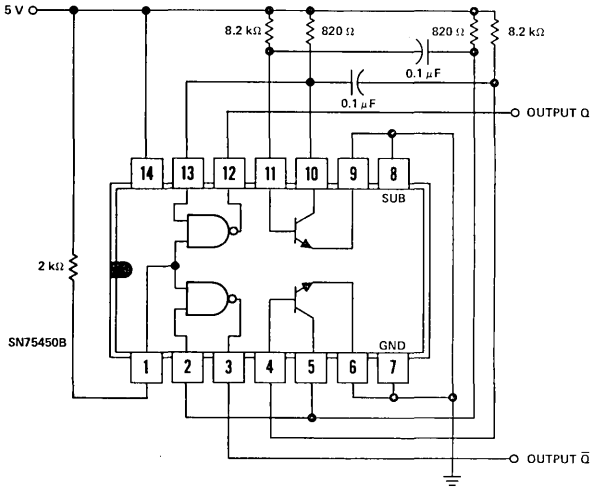



FIGURE 31–SQUARE-WAVE GENERATOR

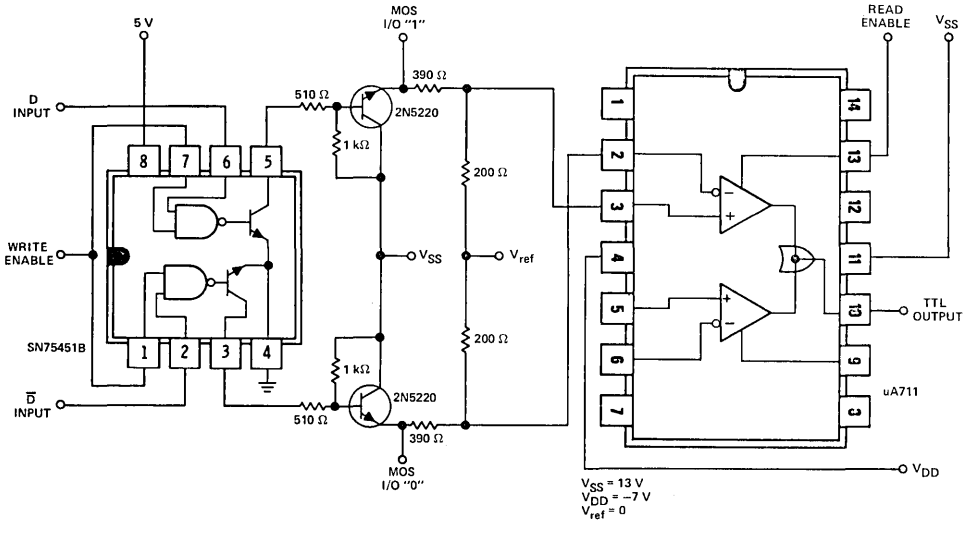



FIGURE 32–TTL COMPATIBLE DRIVER AND SENSE AMPLIFIER INTERFACE TO MOS MEMORY I/O LINES

# TYPICAL APPLICATIONS

## miscellaneous applications (continued)

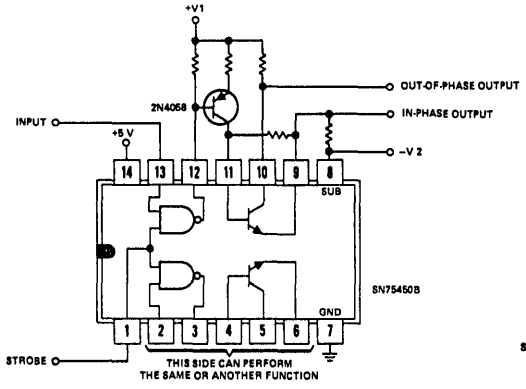



FIGURE 33–FLOATING SWITCH

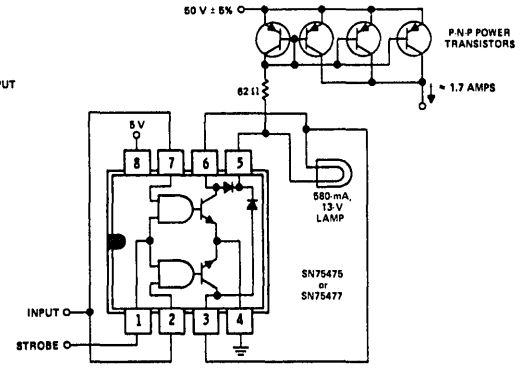



FIGURE 34–SWITCHABLE CURRENT SOURCE WITH INDICATOR LAMP

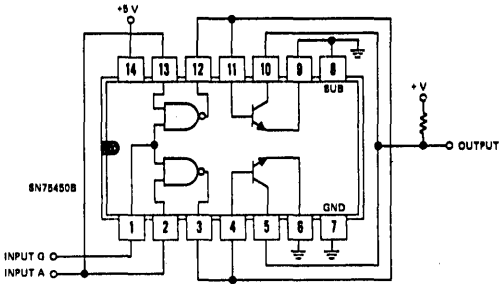



FIGURE 35–500-mA SINK

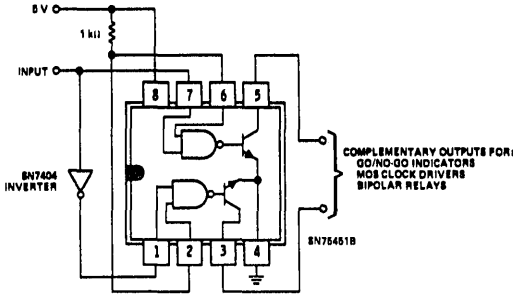
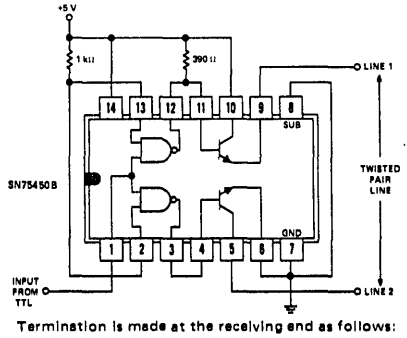



FIGURE 36–COMPLEMENTARY DRIVER




Termination is made at the receiving end as follows:
Line 1 is terminated to ground through $Z_O/2$;
Line 2 is terminated to +5 volts through $Z_O/2$;
where $Z_O$ is the line impedence.

FIGURE 37–BALANCED LINE DRIVER

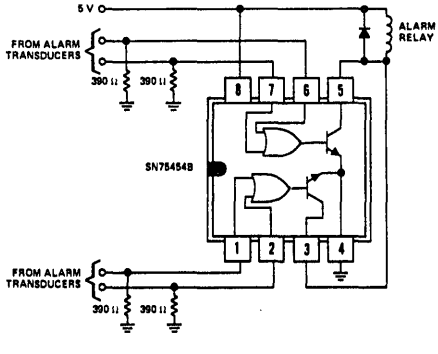



FIGURE 38–ALARM DETECTOR



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