The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

CMOS Logic Circuits

for Design Engineers

Third Edition

TEXAS INSTRUMENTS
INCORPORATED

CMOS
Logic Circuits

for
Design Engineers

Third Edition

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TABLE OF CONTENTS

		PAGE
Alphanumeric Index		5
Interchangeability Guide		6
Glossary		8
Logic Graphic Symbols		11
Explanation of Function Tables		16
Introduction		18
"B" Series Information		19
"B" Series Common Electrical Specifications		24
TF4000B, TP4000B*	Dual 3-Input NOR Gates plus Inverters	26
TF4001B, TP4001B	Quad 2-Input NOR Gates	26
TF4002B, TP4002B*	Dual 4-Input NOR Gates	26
TF4009B, TP4009B	Hex Inverting Buffers/Converters	27
TF4010B, TP4010B	Hex Noninverting Buffers/Converters	27
TF4011B, TP4011B	Quad 2-Input NAND Gates	29
TF4012B, TP4012B*	Dual 4-Input NAND Gates	29
TF4013B, TP4013B	Dual D-Type Edge-Triggered Flip-Flops (with Clear and Preset)	30
TF4014B, TP4014B*	8-Bit Static Shift Registers	31
TF4015B, TP4015B*	Dual 4-Bit Static Shift Registers	33
TF4016B, TP4016B	Quad Bilateral Switches	34
TF4018B, TP4018B	Presettable Divide-by-N Counters	37
TF4021B, TP4021B*	8-Bit Static Shift Registers	39
TF4023B, TP4023B*	Triple 3-Input NAND Gates	41
TF4025B, TP4025B*	Triple 3-Input NOR Gates	41
TF4029B, TP4029B*	Presettable Up/Down Binary/Decade Counters	42
TF4030B, TP4030B	Quad Exclusive-OR Gates	44
TF4035B, TP4035B*	4-Bit Parallel-In/Parallel-Out Shift Registers	45
TF4042B, TP4042B	Quad D-Type Latches	47
TF4043B, TP4043B	Quad S-R Latches with 3-State Outputs	48
TF4044B, TP4044B	Quad $\overline{S}$-$\overline{R}$ Latches with 3-State Outputs	48
TF4049B, TP4049B	Hex Inverting Buffers/Converters	50
TF4050B, TP4050B	Hex Noninverting Buffers/Converters	50
TF4051B, TP4051B	8-Channel Analog Multiplexers/Demultiplexers	52
TF4052B, TP4052B	Dual 4-Channel Analog Multiplexers/Demultiplexers	52
TF4053B, TP4053B	Triple 2-Channel Analog Multiplexers/Demultiplexers	52
TF4069B, TP4069B	Hex Inverting Buffers	55
TF4070B, TP4070B	Quad Exclusive-OR Gates	56
TF4071B, TP4071B	Quad 2-Input OR Gates	57
TF4072B, TP4072B*	Dual 4-Input OR Gates	57
TF4073B, TP4073B*	Triple 3-Input AND Gates	57
TF4075B, TP4075B*	Triple 3-Input OR Gates	57
TF4081B, TP4081B	Quad 2-Input AND Gates	57
TF4082B, TP4082B*	Dual 4-Input AND Gates	57
TF4085B, TP4085B*	Dual 3-Wide 2-2-1-Input AND-OR-Invert Gates	57
TF4376B, TP4376B	Quad S-R Latches	58
TF4377B, TP4377B	Quad $\overline{S}$-$\overline{R}$ Latches	59
"A" Series Information		60
"A" Series Common Electrical Specifications		62
TF4000A, TP4000A	Dual 3-Input NOR Gates plus Inverters	64
TF4001A, TP4001A	Quad 2-Input NOR Gates	64
TF4002A, TP4002A	Dual 4-Input NOR Gates	64
TF4007A, TP4007A	Dual Complementary Pairs plus Inverters	65
TF4008A, TP4008A	Four-Bit Full Adders	67
TF4009A, TP4009A	Hex Inverting Buffers/Converters	69
TF4010A, TP4010A	Hex Noninverting Buffers/Converters	69
TF4011A, TP4011A	Quad 2-Input NAND Gates	71
TF4012A, TP4012A	Dual 4-Input NAND Gates	72

*To be announced.

TABLE OF CONTENTS (Continued)

		PAGE
TF4013A, TP4013A	Dual D-Type Edge-Triggered Flip-Flops (with Clear and Preset)	73
TF4014A, TP4014A	8-Bit Static Shift Registers	75
TF4015A, TP4015A	Dual 4-Bit Static Shift Registers	77
TF4016A, TP4016A	Quad Bilateral Switches	79
TF4017A, TP4017A	Decade Counters/Dividers	82
TF4018A, TP4018A	Presettable Divide-by-N Counters	85
TF4019A, TP4019A	Quad AND-OR Select Gates	87
TF4020A, TP4020A	Asynchronous 14-Bit Binary Counters	89
TF4021A, TP4021A	8-Bit Static Shift Registers	91
TF4022A, TP4022A	Octal Counters/Dividers	93
TF4023A, TP4023A	Triple 3-Input NAND Gates	96
TF4024A, TP4024A	Asynchronous 7-Bit Binary Counters	97
TF4025A, TP4025A	Triple 3-Input NOR Gates	99
TF4027A, TP4027A	Dual J-K Flip-Flops (with Preset and Clear)	100
TF4028A, TP4028A	BCD-to-Decimal Decoders	102
TF4029A, TP4029A	Presettable Up/Down Binary/Decade Counters	104
TF4030A, TP4030A	Quad Exclusive-OR Gates	109
TF4040A, TP4040A	Asynchronous 12-Bit Binary Counters	111
TF4042A, TP4042A	Quad D-Type Latches	113
TF4043A, TP4043A	Quad S-R Latches with 3-State Outputs	115
TF4044A, TP4044A	Quad $\overline{S}$-$\overline{R}$ Latches with 3-State Outputs	115
TF4049A, TP4049A	Hex Inverting Buffers/Converters	117
TF4050A, TP4050A	Hex Noninverting Buffers/Converters	117
TF4051A, TP4051A	8-Channel Analog Multiplexers/Demultiplexers	119
TF4052A, TP4052A	Dual 4-Channel Analog Multiplexers/Demultiplexers	119
TF4053A, TP4053A	Triple 2-Channel Analog Multiplexers/Demultiplexers	119
TF4301A, TP4301A	Quad 2-Input NOR Buffers	122
TF4302A, TP4302A	4-2-3-2-Input AND-OR-Invert Gates	123
TF4303A, TP4303A	4-2-4-1-Input AND-OR-Invert Gates	123
TF4304A, TP4304A	Hex Schmitt-Trigger Inverters	124
TF4311A, TP4311A	Quad 2-Input NAND Buffers	125
TF4315A, TP4315A	Hex Inverting Buffers	126
TF4316A, TP4316A	Quad Bilateral Switches	127
TF4320A, TP4320A	16-Channel Data Selectors with 3-State Outputs	130
TF4321A, TP4321A	Dual 8-Channel Data Selectors with 3-State Outputs	132
TF4360A, TP4360A	Synchronous Decade Counters with Direct Clear	134
TF4361A, TP4361A	Synchronous 4-Bit Binary Counters with Direct Clear	134
TF4362A, TP4362A	Fully Synchronous Decade Counters	134
TF4363A, TP4363A	Fully Synchronous 4-Bit Binary Counters	134
TF4370A, TP4370A	Quad D-Type Edge-Triggered Flip-Flops	139
TF4376A, TP4376A	Quad S-R Latches	141
TF4377A, TP4377A	Quad $\overline{S}$-$\overline{R}$ Latches	141
TF4380A, TP4380A*	256-Bit Random-Access Memories with 3-State Outputs	143
TF4507A, TP4507A	Quad Exclusive-OR Gates	147
TF4512A, TP4512A	8-Channel Data Selectors with 3-State Outputs	149
TF4518A, TP4518A	Dual Decade Counters	152
TF4519A, TP4519A	4-Bit AND-OR Select Gates	154
TF4520A, TP4520A	Dual Binary Counters	156
TF4522A, TP4522A	Decade Divide-by-N Counters	158
TF4526A, TP4526A	4-Bit Binary Divide-by-N Counters	158
TF4531A, TP4531A	12-Bit Parity Trees	161
TF4581A, TP4581A	Arithmetic Logic Units/Function Generators	162
TF4582A, TP4582A	Look-Ahead Carry Generators	167
Parameter Measurement Information		170
Mechanical Data and Ordering Instructions		171

*To be announced.

ALPHANUMERIC INDEX

TYPE NUMBER	PAGE	TYPE NUMBER	PAGE	TYPE NUMBER	PAGE	TYPE NUMBER	PAGE
TF4000A	64	TF4044B	48	TP4000A	64	TP4044B	48
TF4000B*	26	TF4049A	117	TP4000B*	26	TP4049A	117
TF4001A	64	TF4049B	50	TP4001A	64	TP4049B	50
TF4001B	26	TF4050A	117	TP4001B	26	TP4050A	117
TF4002A	64	TF4050B	50	TP4002A	64	TP4050B	50
TF4002B*	26	TF4051A	119	TP4002B*	26	TP4051A	119
TF4007A	65	TF4051B	52	TP4007A	65	TP4051B	52
TF4008A	67	TF4052A	119	TP4008A	67	TP4052A	119
TF4009A	69	TF4052B	52	TP4009A	69	TP4052B	52
TF4009B	27	TF4053A	119	TP4009B	27	TP4053A	119
TF4010A	69	TF4053B	52	TP4010A	69	TP4053B	52
TF4010B	27	TF4069B	55	TP4010B	27	TP4069B	55
TF4011A	71	TF4070B	56	TP4011A	71	TP4070B	56
TF4011B	29	TF4071B	57	TP4011B	29	TP4071B	57
TF4012A	72	TF4072B*	57	TP4012A	72	TP4072B*	57
TF4012B*	29	TF4073B*	57	TP4012B*	29	TP4073B*	57
TF4013A	73	TF4075B*	57	TP4013A	73	TP4075B*	57
TF4013B	30	TF4081B	57	TP4013B	30	TP4081B	57
TF4014A	75	TF4082B*	57	TP4014A	75	TP4082B*	57
TF4014B*	31	TF4085B*	57	TP4014B*	31	TP4085B*	57
TF4015A	77	TF4301A	122	TP4015A	77	TP4301A	122
TF4015B*	33	TF4302A	123	TP4015B*	33	TP4302A	123
TF4016A	79	TF4303A	123	TP4016A	79	TP4303A	123
TF4016B	34	TF4304A	124	TP4016B	34	TP4304A	124
TF4017A	82	TF4311A	125	TP4017A	82	TP4311A	125
TF4018A	85	TF4315A	126	TP4018A	85	TP4315A	126
TF4018B	37	TF4316A	127	TP4018B	37	TP4316A	127
TF4019A	87	TF4320A	130	TP4019A	87	TP4320A	130
TF4020A	89	TF4321A	132	TP4020A	89	TP4321A	132
TF4021A	91	TF4360A	134	TP4021A	91	TP4360A	134
TF4021B*	39	TF4361A	134	TP4021B*	39	TP4361A	134
TF4022A	93	TF4362A	134	TP4022A	93	TP4362A	134
TF4023A	96	TF4363A	134	TP4023A	96	TP4363A	134
TF4023B*	41	TF4370A	139	TP4023B*	41	TP4370A	139
TF4024A	97	TF4376A	141	TP4024A	97	TP4376A	141
TF4025A	99	TF4376B	58	TP4025A	99	TP4376B	58
TF4025B*	41	TF4377A	141	TP4025B*	41	TP4377A	141
TF4027A	100	TF4377B	59	TP4027A	100	TP4377B	59
TF4028A	102	TF4380A*	143	TP4028A	102	TP4380A*	143
TF4029A	104	TF4507A	147	TP4029A	104	TP4507A	147
TF4029B*	42	TF4512A	149	TP4029B*	42	TP4512A	149
TF4030A	109	TF4518A	152	TP4030A	109	TP4518A	152
TF4030B	44	TF4519A	154	TP4030B	44	TP4519A	154
TF4035B*	45	TF4520A	156	TP4035B*	45	TP4520A	156
TF4040A	111	TF4522A	158	TP4040A	111	TP4522A	158
TF4042A	113	TF4526A	158	TP4042A	113	TP4526A	158
TF4042B	47	TF4531A	161	TP4042B	47	TP4531A	161
TF4043A	115	TF4581A	162	TP4043A	115	TP4581A	162
TF4043B	48	TF4582A	167	TP4043B	48	TP4582A	167
TF4044A	115			TP4044A	115		

*To be announced

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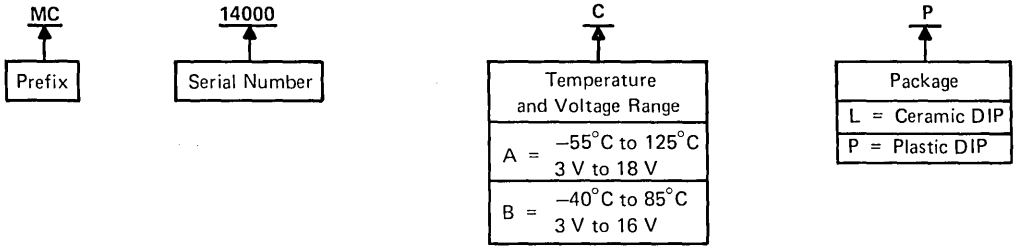
INTERCHANGEABILITY GUIDE

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

MOTOROLA INTERCHANGEABILITY



TEMPERATURE RANGE AND PACKAGE COMBINATION EQUIVALENTS	MOTOROLA	TI
	MC14___CP	TP4___AN
	MC14___CL	TP4___AJ
	MC14___AL	TF4___AJ

MOTOROLA TYPE	TI DIRECT REPLACEMENT
MC14000__	T_4000A_
MC14001__	T_4001A_
MC14002__	T_4002A_
MC14007__	T_4007A_
MC14008__	T_4008A_
MC14009__	T_4009A_
MC14010__	T_4010A_
MC14011__	T_4011A_
MC14012__	T_4012A_
MC14013__	T_4013A_
MC14014__	T_4014A_
MC14015__	T_4015A_
MC14016__	T_4016A_
MC14017__	T_4017A_
MC14018__	T_4018A_
MC14019__	T_4019A_
MC14020__	T_4020A_
MC14021__	T_4021A_
MC14022__	T_4022A_
MC14023__	T_4023A_
MC14024__	T_4024A_
MC14025__	T_4025A_
MC14027__	T_4027A_
MC14028__	T_4028A_

MOTOROLA TYPE	TI DIRECT REPLACEMENT
MC14029__	T_4029A_
MC14030__	T_4030A_
MC14040__	T_4040A_
MC14042__	T_4042A_
MC14043__	T_4043A_
MC14044__	T_4044A_
MC14049__	T_4049A_
MC14050__	T_4050A_
MC14051__	T_4051A_
MC14052__	T_4052A_
MC14053__	T_4053A_
MC14507__	T_4507A_
MC14512__	T_4512A_
MC14518__	T_4518A_
MC14519__	T_4519A_
MC14520__	T_4520A_
MC14522__	T_4522A_
MC14526__	T_4526A_
MC14531__	T_4531A_
MC14581__	T_4581A_
MC14582__	T_4582A_

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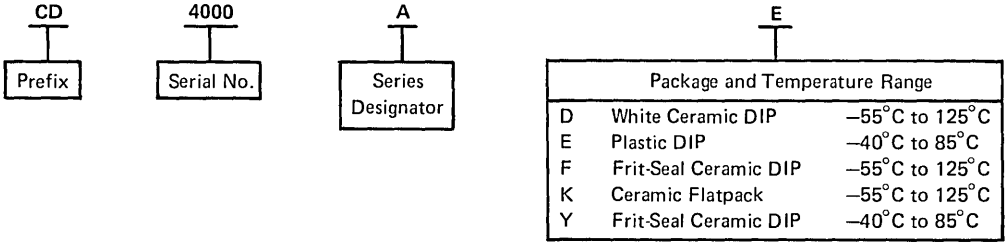
RCA INTERCHANGEABILITY



TEMPERATURE RANGE AND PACKAGE COMBINATION EQUIVALENTS

RCA	TI
CD4___AE	TP4___AN
CD4___AF	TF4___AJ
CD4___AY	TP4___AJ

RCA TYPE	TI DIRECT REPLACEMENT
CD4000A_	T_4000A_
CD4001A_	T_4001A_
CD4002A_	T_4002A_
CD4007A_	T_4007A_
CD4008A_	T_4008A_
CD4009A_	T_4009A_
CD4010A_	T_4010A_
CD4011A_	T_4011A_
CD4012A_	T_4012A_
CD4013A_	T_4013A_
CD4014A_	T_4014A_
CD4015A_	T_4015A_
CD4016A_	T_4016A_
CD4017A_	T_4017A_
CD4018A_	T_4018A_
CD4019A_	T_4019A_
CD4020A_	T_4020A_
CD4021A_	T_4021A_

RCA TYPE	TI DIRECT REPLACEMENT
CD4022A_	T_4022A_
CD4023A_	T_4023A_
CD4024A_	T_4024A_
CD4025A_	T_4025A_
CD4027A_	T_4027A_
CD4028A_	T_4028A_
CD4029A_	T_4029A_
CD4030A_	T_4030A_
CD4040A_	T_4040A_
CD4042A_	T_4042A_
CD4043A_	T_4043A_
CD4044A_	T_4044A_
CD4049A_	T_4049A_
CD4050A_	T_4050A_
CD4051A_	T_4051A_
CD4052A_	T_4052A_
CD4053A_	T_4053A_
CD4518A_	T_4518A_
CD4520A_	T_4520A_

GLOSSARY
LETTER SYMBOLS, TERMS, AND DEFINITIONS

LETTER SYMBOLS, TERMS, AND DEFINITIONS

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified that is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified that is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-level output voltage
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

CURRENTS

I_{CC}, I_{DD}, I_{EE}, I_{SS} supply current
The current into*, respectively, the V_{CC}, V_{DD}, V_{EE}, or V_{SS} supply terminal of an integrated circuit.

I_{IH} High-level input current
The current into* an input when a high-level voltage is applied to that input.

I_{IL} Low-level input current
The current into* an input when a low-level voltage is applied to that input.

I_{OH} High-level output current
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

*Current out of a terminal is given as a negative value.

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I_{OL} Low-level output current
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

I_{OZ} Off-state (high-impedance-state) output current (of a three-state output)
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

SWITCHING CHARACTERISTICS

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

t_a Access time (of a memory)
The time between the application of a specific input pulse and the availability of valid data signals at an output.

t_h Hold time
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

$t_{h(min)}$ Minimum hold time
The shortest hold time for which correct operation is obtained.

t_{PHL} Propagation delay time, high-to-low-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} Output disable time (of a three-state output) from high level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} Propagation delay time, low-to-high-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} Output disable time (of a three-state output) from low level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} Output enable time (of a three-state output) to high level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

*Current out of a terminal is given as a negative value.

t_{PZL} Output enable time (of a three-state output) to low level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low-level.

t_{su} Setup time
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

$t_{su(min)}$ Minimum setup time
The shortest setup time for which correct operation is obtained.

t_{TLH} Transition time, low-to-high-level output
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} Transition time, high-to-low-level output
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w Average pulse width
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

$t_{w(min)}$ Minimum pulse width
The shortest pulse width for which correct operation is obtained.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration
A concept whereby a complete subsystem function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration
Integrated circuits of less complexity than medium-scale integration (MSI).

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LOGIC GRAPHIC SYMBOLS

The logic graphic symbols used in this book are in accordance with American National Standard Graphic Symbols for Logic Diagrams (Two-State Devices) ANSI Y32.14-1973 (IEEE Std. 91-1973) which supersedes ASA Y32.14-1962, MIL-STD-806B, and MIL-STD-806C. The following is only a brief explanation of the more common symbols used in this book.

basic logic concepts

The binary numbers 1 and 0 are used in pure logic where 1 represents true, yes, or active and 0 represents false, no, or inactive. These terms should not be confused with the physical quantity (e.g., voltage) that may be used to implement the logic, nor should the term "active" be confused with a level that turns a device on or off. A truth table for a relationship in logic shows (implicitly or explicitly) all the combinations of true and false input conditions and the result (output). There are only two basic logic relationships, AND and OR. The following illustrations assume two inputs (A and B), but these can be generalized to apply to more than two inputs.

AND Y is true if and only if A is true and B is true (or more generally, if all inputs are true).

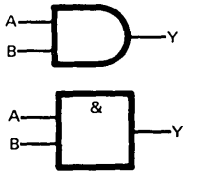
Y = 1 if and only if A = 1 and B = 1.

$Y = A \cdot B$

TRUTH TABLE

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

SYMBOLS



OR Y is true if and only if A is true or B is true (or more generally, if one or more input(s) is (are) true.

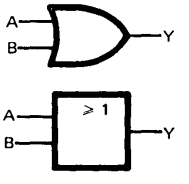
Y = 1 if and only if A = 1 or B = 1.

$Y = A + B$

TRUTH TABLE

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

SYMBOLS



Y32.14-1973 continues the use of both distinctive-shape and rectangular symbols for the simpler logic functions. Both forms are shown here for AND and OR; however, throughout the rest of this section, and in the data sheets in this book, usually only the distinctive shapes will be used for these functions. The rectangular symbols are most useful when making up complex combinations of logic functions.

negation

In logic symbology, the presence of the negation indication symbol ○ provides for the representation of logic function inputs and outputs in terms independent of their physical values, the 0-state of the input or output being the 1-state of the symbol referred to by the symbol description.

EXAMPLE 1

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 2

TRUTH TABLE

A	B	Z
1	1	0
1	0	1
0	1	1
0	0	1

EXAMPLE 3

TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

EXAMPLE 4

TRUTH TABLE

A	B	Z
1	1	0
1	0	0
0	1	0
0	0	1

Example 1 says that Z is not true if A is true and B is true or that Z is true if A and B are not both true. $\overline{Z} = AB$ or $Z = \overline{AB}$. This is frequently referred to as NAND (for NOT AND).

Example 2 says that Z is true if A is not true or if B is not true. $Z = \overline{A} + \overline{B}$. Note that this truth table is identical to that of Example 1. The logic equation is merely a De Morgan's transformation of the equations in Example 1. The symbols are equivalent.

Example 3, $\overline{Z} = A + B$ or $Z = \overline{A + B}$, and **Example 4,** $Z = \overline{A} \cdot \overline{B}$, also share a common truth table and are equivalent transformations of each other. The NOT OR form (Example 3) is frequently referred to as NOR.

logic implementation and polarity indication

Devices that can perform the basic logic functions, AND and OR, are called gates. Any device that can perform one of these functions can also be used to perform the other if the relationship of the input and output voltage levels to the logic variables 1 and 0 is redefined suitably.

In describing the operation of electronic logic devices, the symbol H is used to represent a "high level," which is a voltage within the more-positive (less-negative) of the two ranges of voltages used to represent the binary variables. L is used to represent a "low level," which is a voltage within the less-positive (more-negative) range.

A function table for a device shows (implicitly or explicitly) all the combinations of input conditions and the resulting output conditions.

In graphic symbols, inputs or outputs that are active when at the high level are shown without polarity indication. The polarity indicator symbol ◺ denotes that the active state of an input or output *with respect to the symbol to which it is attached* is the low level.

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EXAMPLE 5

Assume two devices having the following function tables.

DEVICE #1
FUNCTION TABLE

A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

DEVICE #2
FUNCTION TABLE

A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

By assigning the relationships H = 1, L = 0 at both input and output, Device #1 can perform the AND function and Device #2 can perform the OR function. Such a consistent assignment is referred to as positive logic. The corresponding logic symbols would be:

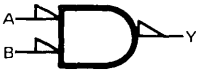
DEVICE #1

DEVICE #2

Alternatively, by assigning the relationships H = 0, L = 1 at both input and output, Device #1 can perform the OR function and Device #2 can perform the AND function. Such a consistent assignment is referred to as negative logic. The corresponding logic symbols would be:

DEVICE #1

DEVICE #2

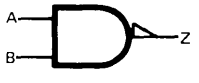


The use of the polarity indicator symbol (◺) automatically invokes a mixed-logic convention. That is, positive logic is used at the inputs and outputs that do not have polarity indicators, negative logic is used at the inputs and outputs that have polarity indicators.

EXAMPLE 6
FUNCTION TABLE

A	B	Z
H	H	L
H	L	H
L	H	H
L	L	H

This may be shown either of two ways:



Note the equivalence of these symbols to examples 1 and 2 and the fact that the function table is a positive-logic translation (H = 1, L = 0) of the NAND truth table, and also note that the function table is the negative-logic translation (H = 0, L = 1) of the NOR truth table, given in Example 3.

EXAMPLE 7
FUNCTION TABLE

A	B	Z
H	H	L
H	L	L
L	H	L
L	L	H

This may be shown either of two ways:

Note the equivalence of these symbols to examples 3 and 4 and the fact that the function table is a positive-logic translation (H = 1, L = 0) of the NOR truth table, and also note that the function table is the negative-logic translation (H = 0, L = 1) of the NAND truth table, given in Example 1.

It should be noted that one can easily convert from the symbology of positive logic merely by substituting a polarity indicator (◺) for each negation indicator (○) while leaving the distinctive shapes alone. To convert from the symbology of negative logic, a polarity indicator (◺) is substituted for each negation indicator (○) and the OR shape is substituted for the AND shape or vice versa.

CMOS
LOGIC GRAPHIC SYMBOLS

choice of AND/OR symbols

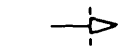
The preceding material stated and demonstrated that any device that can perform OR logic can also perform AND logic and vice versa. De Morgan's transformation is illustrated in Examples 1 through 7. The rules of the transformation are:

1. At each input or output having a negation (O) or polarity (◺) indicator, delete the indicator.
2. At each input or output not having an indicator, add a negation (O) or polarity (◺) indicator.
3. Substitute the AND symbol (⊐) for the OR symbol (⊃) or vice versa.

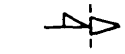
These steps do not alter the assumed convention; positive logic stays positive, negative logic stays negative, and mixed logic stays mixed.

The choice of symbol may be influenced by these considerations: (1) The operation being performed may best be understood as AND or OR. (2) In a function more complex than a basic gate, the inputs will usually be considered as inherently active high or active low (e.g., the J and $\overline{K}$ inputs of a J-$\overline{K}$ flip-flop are active high and active low, respectively). (3) In a chain of logic, understanding and the writing of logic equations are often facilitated if active-low or negated outputs feed into active-low or negated inputs.

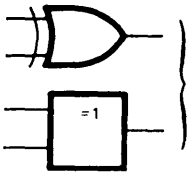
other symbols



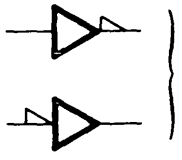
Dynamic input activated by transition from a low level to a high level. The opposite transition has no effect at the output.



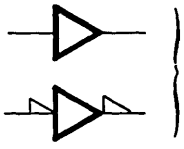
Dynamic input activated by transition from a high level to a low level. The opposite transition has no effect at the output.



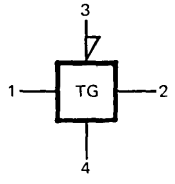
Exclusive OR function. The output will assume its indicated active level if and only if one and only one of the two inputs assumes its indicated active level.



Inverting function. The output is low if the input is high and it is high if the input is low. The two symbols shown are equivalent.



Noninverting function. The output is high if the input is high and it is low if the input is low. The two symbols shown are equivalent.



Transmission gate. Serves as a closed switch between lines 1 and 2 only when lines 3 and 4 are active, i.e., low and high, respectively. Complementary signals are always presented to lines 3 and 4.

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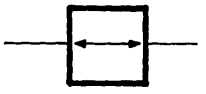
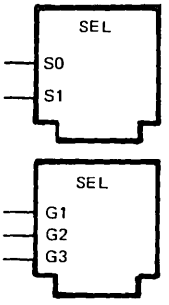
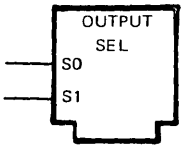


Bilateral switch. When the switch is on, signals can be transmitted in either direction.

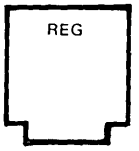
control blocks



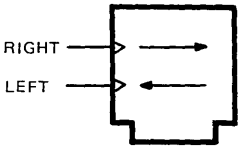
Selector control block. These symbols are used with an array of OR symbols to provide a point of placement for selection (S) or gating (G) lines. The selection lines enable the input designated 0, 1, ... n of each OR function by means of a binary code where S0 is the least-significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used. The gating lines have an AND relation with the respective input of each OR function: G1 with the inputs numbered 1, G2 with the inputs numbered 2, and so forth. If the enabling levels of these lines is low, polarity indicators (◺) will be used. For example applications, see '4051A and '4321A for the first symbol; '4019A and '4519A for the second symbol.



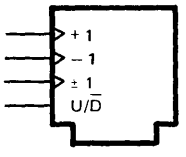
Output selector control block. This symbol is used with a block symbol having multiple outputs to form a decoder. The selection lines enable the output designated 0, 1, ... n of each block by means of a binary code where S0 is the least significant digit. If the 1 level of these lines is low, polarity indicators (◺) will be used. For example application of this symbol, see '4028A.



Register control block. This symbol is used with an associated array of flip-flop symbols to provide a point of placement for common function lines, such as a common clear.



Shift register control block. These symbols are used with an array of flip-flop symbols to form a shift register. An active transition at the inputs causes left or right shifting as indicated. For example applications of this symbol, see '4014A, '4015A, and '4021A.



Counter control block. This symbol is used with an array of flip-flops or other circuits serving as a binary or decade counter. An active transition at the +1 or −1 input causes the counter to increment one count upward or downward, respectively. An active transition at the ±1 input causes the counter to increment one count upward or downward depending on the input at an up/down control. For example applications of these symbols, see '4017A, '4029A, '4360A, and '4522A.

EXPLANATION OF FUNCTION TABLES

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were establsihed
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎏	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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The most complex function tables in this book are those of the shift registers. These embody all of the symbols used in any of the other function tables, plus more. Below is the function table of an 8-bit static shift register, e.g. type TF4021.

FUNCTION TABLE

INPUTS				INTERNAL OUTPUTS (2 OF 5)		OUTPUTS		
CONTROL P/$\overline{S}$	CLOCK	PARALLEL A-H	SERIAL	Q_A	Q_B	Q_F	Q_G	Q_H
H	X	a-h	X	a	b	f	h	h
L	↑	X	H	H	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	↑	X	L	L	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	L	X	X	Q_{A0}	Q_{B0}	Q_{F0}	Q_{G0}	Q_{H0}

The first line of the table represents asynchronous parallel loading of the register and says that if P/$\overline{S}$ is high then, without regard to the serial input or the clock, the data entered at A will be at internal output Q_A, data entered at B will be at Q_B, and so forth.

The second and third lines represent the loading of high-and low-level data, respectively, from the serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_E, Q_F, and Q_G and now at Q_F, Q_E, and Q_H, respectively, and the data previously at Q_H is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when P/$\overline{S}$ is low and the levels at inputs A through H have no effect.

The fourth line simply states that so long as the clock remains low while P/$\overline{S}$ is low, no other input has any effect and the outputs maintain the levels they assumed on the last rising transition of the clock.

Since only the rising transition of the clock has been shown to be active, the fourth line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

CMOS LOGIC CIRCUITS

INTRODUCTION

This booklet contains descriptive information on CMOS integrated circuits manufactured by Texas Instruments. Included are data sheets providing electrical and switching characteristics. The circuits designated with 40XXA numbers are plug-in replacements for the RCA family of CMOS devices. The 43XXA devices are unique Texas Instruments functions. The 45XXA devices are plug-in replacements for the Motorola family of CMOS devices.

Circuits designated with an "A" suffix are those devices having an operating voltage range of 3 to 15 volts with specifications at 5 to 10 volts.

The circuits designated with a "B" suffix are those devices whose voltage range is 3 to 18 volts with specifications at 5, 10, and 15 volts. Additionally the data sheets on the "B" parts more clearly define the product in a system-oriented manner. The specific areas where the "B" data sheets are more descriptive than the "A" data sheets are:

- Input and Output Characteristics
- Noise Immunity
- Drive Capability
- Specifications at 15 volts

The "B" series (including all "B" series data sheets) is presented first, then the "A" series; for most type numbers there is both an "A" series device and a "B" series device. Within each series the data sheets are arranged in type-number sequence.

Texas Instruments CMOS offers the design engineer:

- Choice of two packages . . .
  Plastic dual-in-line
  Ceramic hermetically sealed dual-in-line
- Choice of temperature ranges . . .
  Series TF . . .–55°C to 125°C (full military range)
  Series TP . . .–40°C to 85°C
- Protective network on each input
- Low power dissipation (quiescent)
- High noise immunity
- Threshold voltage, input and supply current stability
- Easy interface capability to
  TTL (including low-power and low-power Schottky)
  Linear
  N-Channel MOS
  P-Channel MOS

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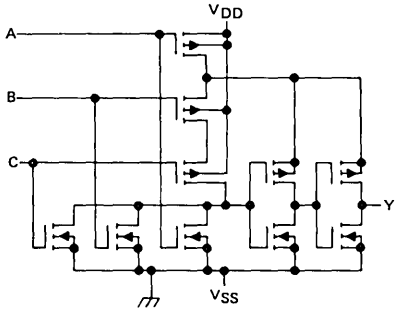
"B" SERIES INFORMATION

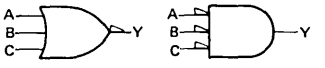
BUFFERED CIRCUITS

Most 4XXXXB digital circuits will have double- or triple-buffered output stages to attain:

- Uniform dynamic performance
- Uniform input characteristics
- Uniform output characteristics
- Improved noise immunity
- Improved capacitance drive
- Lower input capacitance
- Lower over-all system CV^2f power

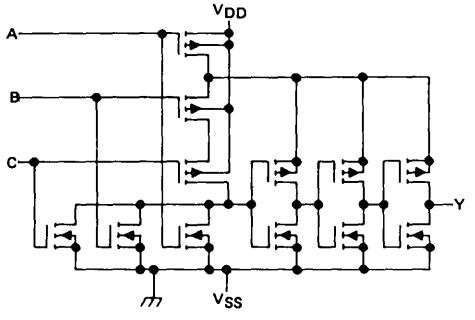
Figure 1 shows typical three-input NOR, OR, and NAND gate circuits. The input transistor sizes are minimized to reduce input capacitance and are buffered from the large output transistors, which are designed to give symmetrical output characteristics.

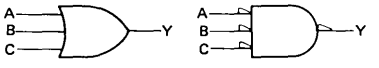




positive logic:

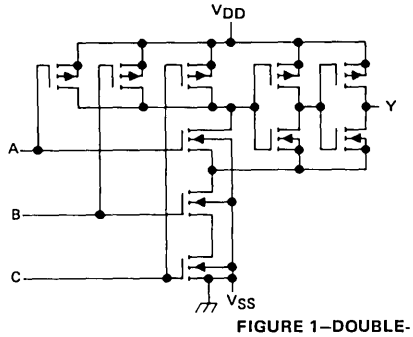
$Y = \overline{A + B + C}$ or $Y = \overline{A}\,\overline{B}\,\overline{C}$

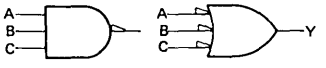




positive logic:

$Y = A + B + C$ or $Y = \overline{\overline{A}\,\overline{B}\,\overline{C}}$





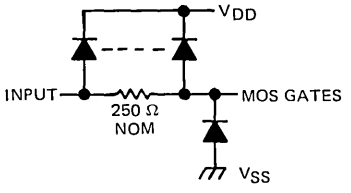
positive logic:

$Y = \overline{ABC}$ or $Y = \overline{A} + \overline{B} + \overline{C}$

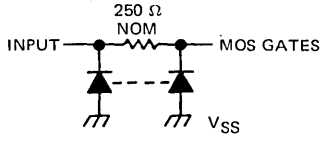
FIGURE 1–DOUBLE- AND TRIPLE-BUFFERED CMOS CIRCUITS

INPUT PROTECTION

Input protection networks have been standardized to the two configurations below:



CONFIGURATION 1



CONFIGURATION 2

Configuration 1 is used on the whole family except for the '4049B and '4050B, which use configuration 2. In each case the diodes to V_{SS} have a reverse breakdown of approximately 22 to 28 volts. These networks are incorporated as protection against occassional electrostatic overstress. It is not recommended that units be subjected to continuously repeated overstress. CMOS is much less sensitive to electrostatic overstress than other MOS technologies; however, care should be taken in handling these networks much the same as is required for other high-impedance integrated circuits:

1) Equipment should be properly grounded.
2) Work surfaces should be electrically conductive and connected to earth ground.
3) Handling should be minimized.

INPUT CHARACTERISTICS

For input voltages between V_{SS} and V_{DD} the protective networks are in reverse-biased, low-current states. Typically the input current at 25°C will be on the order of a few picoamps. Because such small currents are difficult to measure, inputs are specified at only V_{DD} = 15 volts. The maximum limit is the sum of all inputs simultaneously measured in parallel.

The 4XXXB devices have input capacitances of typically 3 to 5 pF.

OUTPUT CHARACTERISTICS

Digital CMOS inputs represent such small loads to CMOS driving units that the outputs will typically equal either V_{SS} or V_{DD} in a quiescent logic state. However for most system applications, one must specify the logic output levels under a load to indicate interface capabilities of the output to other circuits, the output transient drive capability, and the susceptability to noise. It is intended to guarantee a standard "B" series output to drive one Low-Power Schottky TTL input and to have nearly symetrical output impedances. For these reasons the output source and sink currents are specified at output voltages that are symetrically related; that is at V_{DD} = 5 V, $V_O = V_{DD}-0.4$ V and 1/2 V_{DD} for I_{OH} and V_O = 0.4 V and 1/2 V_{DD} for I_{OL}.

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NOISE IMMUNITY

Noise immunity is the inherent ability of a device to receive electrical noise at its inputs without propagating signals that would cause erroneous logic levels subsequently in the system. Noise immunity does not imply that no output transient will occur. It does mean that the amplitude of such a transient will be reduced as it is propagated through the system. The "A" series noise immunity is typically 30% of $V_{DD}-V_{SS}$. Because the "B" series has internal buffers, this noise immunity is increased to typically 45% of the supply voltage. Noise margin is a specific measure of noise immunity under specific conditions of load, supply voltage, and temperature. High-level noise margin is defined as V_{OH} min – V_{IH} min and low-level noise margin is defined as V_{IL} max – V_{OL} max, where the following definitions apply:

V_{IH} min The minimum value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} max The maximum value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} min The minimum high-level output voltage that will occur under specific conditions of input voltage, supply voltage, load, and temperature.

V_{OL} max The maximum low-level output voltage that will occur under specific conditions of input voltage, supply voltage, load, and temperature.

Historically the CMOS industry has applied these definitions of noise margins under the conditions of no output load with the units stressed one input at a time while the other inputs are at V_{DD} or V_{SS}. A more realistic system application would require all inputs to be stressed simultaneously in a worst case combination and the outputs to be loaded. Under guaranteed data sheet conditions of V_{OH} min, V_{IH} min, V_{IL} max, and V_{OL} max, Texas Instruments guarantees worst-case noise margins of:

LOGIC LEVEL	V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 15 V
High	0.6 V	1.5 V	1.5 V
Low	0.6 V	1.5 V	1.5 V

These noise margins are equivalent to the following under conditions of no load and one input stressed at a time.

LOGIC LEVEL	V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 15 V
High	1.5 V	3.0 V	4.0 V
Low	1.5 V	3.0 V	4.0 V

SERIES '4000B
GENERAL INFORMATION

POWER DISSIPATION

CMOS power dissipation is defined primarly by two contributing factors; a steady-state "leakage" current contribution and dynamic power dissipation. The dynamic power is normally the major factor and consists of two components: the capacitive term (CV^2f) and the "through" current, which results when both the N-channel and the P-channel transistors are simultaneously on. The curves of Figure 2 show CMOS power of a two-input NOR circuit as compared to equivalent circuits in the three most popular TTL families. From this comparison one can clearly see that CMOS offers the optimum power versus frequency for system frequencies less than 100 kHz. From 1 MHz up, the trade-off favors Low-Power Schottky TTL.

CMOS quiescent supply current specified in subsequent detailed specifications is primarily reverse current of diodes and off-state current of MOS transistors. Since CMOS logic functions consist of series and parallel combinations of MOS transistors, one must measure the reverse current in sufficient logic states to ensure that all junctions and transistors are stressed. For example a two-input NOR gate would require an I_{DD} measurement with both inputs low to stress both n-channel transistors. Then, one must apply a high, low combination to stress one p-channel transistor followed by a low, high combination to stress the other. This method of measurement is being used on all Texas Instruments CMOS products.

SPECIFICATION GROUPING

The products in this book are classified into two groups each having common characteristics. The first group (SSI, small-scale integration) comprises the basic gate functions, buffers, and small analog functions, the second group (CSSI, complex small-scale integration, and MSI, medium-scale integration) comprises the dual flip-flops and the more complex functions. The type numbers in each group of the "B" series are shown below.

GROUP 1 (SSI)	GROUP 2 (CSSI and MSI)
4000B♦	4013B
4001B	4014B♦
4002B♦	4015B♦
4009B	4018B
4010B	4021B♦
4011B	4029B♦
4012B♦	4035B♦
4016B	4042B
4023B♦	4043B
4025B♦	4044B
4030B	4051B
4049B	4052B
4050B	4053B
4069B	4376B
4070B	4377B
4071B	
4072B♦	
4073B♦	
4075B♦	
4081B	
4082B♦	
4085B♦	

♦Future products to be announced

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POWER DISSIPATION PER GATE
vs
FREQUENCY FOR TTL AND CMOS

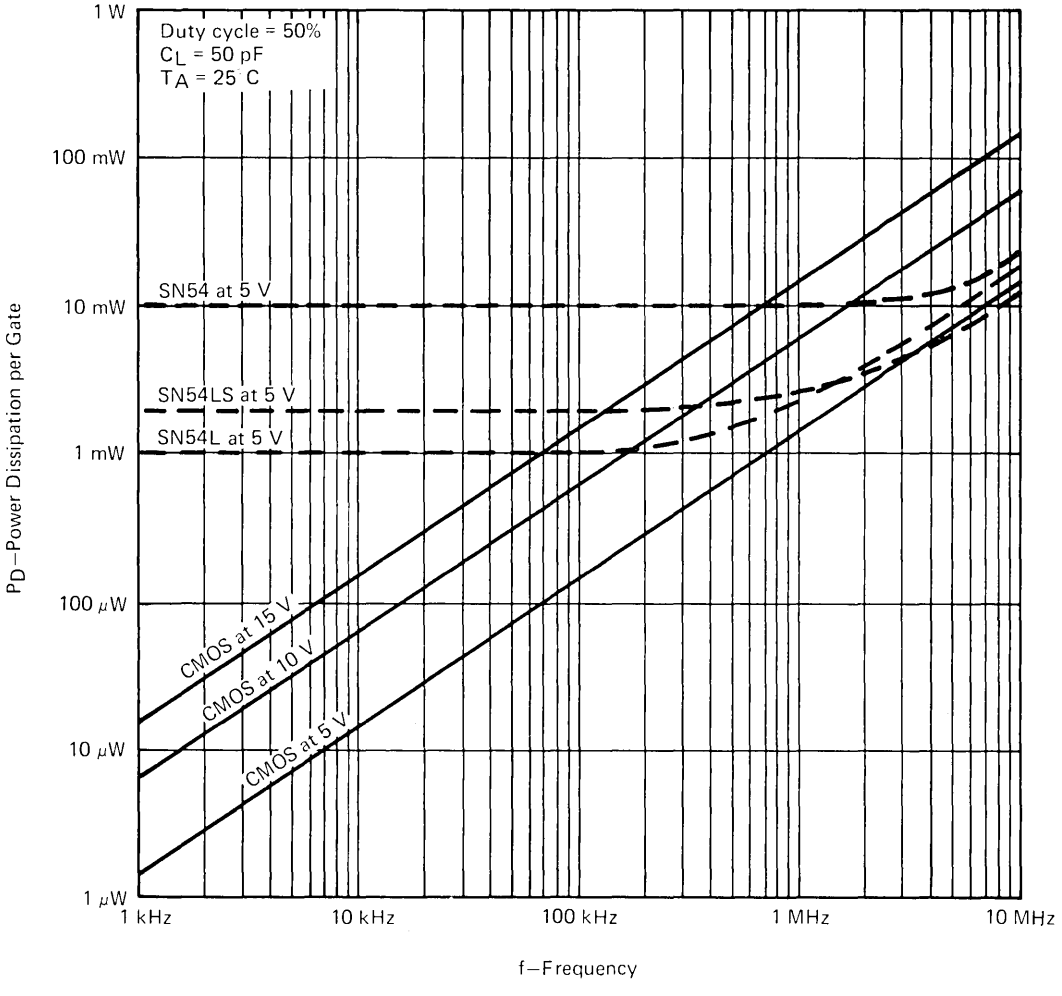

FIGURE 2

SERIES '4000B
COMMON ELECTRICAL SPECIFICATIONS

SEPTEMBER 1975

The following electrical specifications apply for most series '4000B CMOS products. Each individual product specification references the appropriate sections of this common specification and lists exceptions if there are any.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input current . . . . . ±10 mA
Continuous total dissipation (see Note 2) . . . . . 200 mW
Operating free-air temperature range: TF4000B Series . . . . . −55°C to 125°C
TP4000B Series . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Throughout this page, the following page, and the individual product specifications, voltage values are with respect to the V_{SS} terminal unless otherwise noted.
2. Power dissipation averaged over a 1-second interval must fall within the continuous dissipation rating.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		3	18	V
Input voltage, V_I		0	V_{DD}	V
Operating free-air temperature, T_A	TF4000B Series	−55	125	°C
	TP4000B Series	−40	85	°C
Rise time, any input, t_r			15	μs
Fall time, any input, t_f			15	μs

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TF4000B Series

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage				4		8		12		V
V_{IL}	Low-level input voltage					1		2		3	V
V_{OH}	High-level output voltage		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, See Note 3	I_O = I_{OH} min	4.6		9.5		13.5		V
V_{OL}	Low-level output voltage			I_O = I_{OL} min		0.4		0.5		1.5	V
I_{OH}	High-level output current		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OH} min	T_A = −55°C	−0.5		−1.1		−3.8		mA
				T_A = 25°C	−0.4		−0.9		−3		
				T_A = 125°C	−0.4		−0.65		−2.3		
			V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −55°C	−2		−7.5		−11		
				T_A = 25°C	−1.6		−6		−9		
				T_A = 125°C	−1.2		−4		−6		
I_{OL}	Low-level output current		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −55°C	0.5		1.1		3.8		mA
				T_A = 25°C	0.4		0.9		3		
				T_A = 125°C	0.4		0.65		2.3		
			V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −55°C	2		7.5		11		
				T_A = 25°C	1.6		6		9		
				T_A = 125°C	1.2		4		6		
I_I	Input current		V_I = V_{DD} or 0 V							±1	μA
I_{DD} or $-I_{SS}$	Quiescent supply current	Group 1† products	V_I = V_{DD} or 0 V, All logic states, No load	T_A = −55°C or 25°C	0.5		1		2		μA
				T_A = 125°C	30		60		120		
		Group 2† products		T_A = −55°C or 25°C	5		10		20		
				T_A = 125°C	300		600		1200		

NOTE 3: The output voltage limits are guaranteed for any appropriate combination of high and low inputs.
†See group designation on individual product specifications and page 22 for a list of all products by group.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TP4000B Series

PARAMETER			TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage				4		8		12		V
V_{IL}	Low-level input voltage					1		2		3	V
V_{OH}	High-level output voltage		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, See Note 3	I_O = I_{OH} min	4.6		9.5		13.5		V
V_{OL}	Low-level output voltage			I_O = I_{OL} min		0.4		0.5		1.5	V
I_{OH}	High-level output current		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OH} min	T_A = −40°C	−0.45		−1		−3.4		mA
				T_A = 25°C	−0.4		−0.9		−3		
				T_A = 85°C	−0.4		−0.75		−2.7		
			V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −40°C	−1.8		−6.7		−10		
				T_A = 25°C	−1.6		−6		−9		
				T_A = 85°C	−1.3		−5		−7.2		
I_{OL}	Low-level output current		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −40°C	0.45		1		3.4		mA
				T_A = 25°C	0.4		0.9		3		
				T_A = 85°C	0.4		0.75		2.7		
			V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −40°C	1.8		6.7		10		
				T_A = 25°C	1.6		6		9		
				T_A = 85°C	1.3		5		7.2		
I_I	Input current		V_I = V_{DD} or 0 V							±1	μA
I_{DD} or $-I_{SS}$	Quiescent supply current	Group 1† products	V_I = V_{DD} or 0 V, All logic states, No load	T_A = −40°C or 25°C		5		10		20	μA
				T_A = 85°C		70		140		280	
		Group 2† products		T_A = −40°C or 25°C		50		100		200	
				T_A = 85°C		700		1400		2800	

NOTE 3: The output voltage limits are guaranteed for any appropriate combination of high and low inputs.
†See group designation on individual product specifications and page 22 for a list of all products by group.

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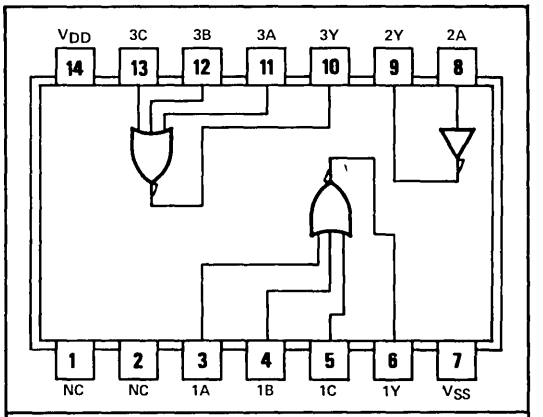
TYPES TF4000B, TF4001B, TF4002B, TP4000B, TP4001B, TP4002B NOR GATES

SEPTEMBER 1975

'4000B . . . Dual 3-Input NOR Gates Plus Inverter◊
'4001B . . . Quad 2-Input NOR Gates
'4002B . . . Dual 4-Input NOR Gates◊

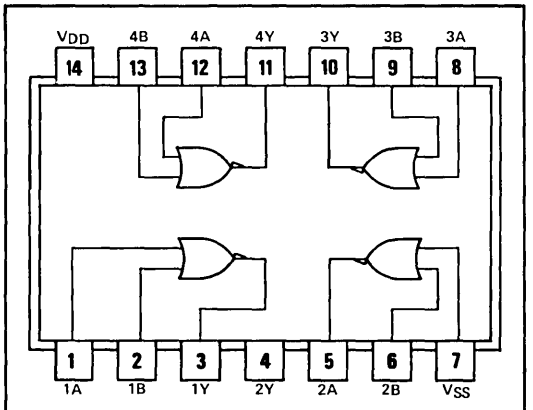
TF4000B, TP4000B◊
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: NOR gates: $Y = \overline{A+B+C}$
Inverters: $Y = \overline{A}$

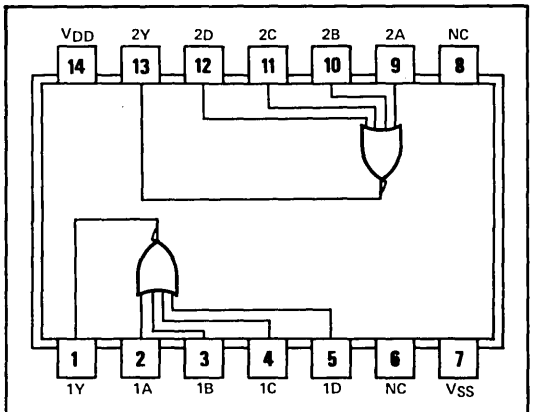
NC—No internal connection

TF4001B, TP4001B
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A+B}$

TF4002B, TP4002B◊
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A+B+C+D}$

NC—No internal connection

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25° C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	175		50		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		175		50		40		
t_{TLH}	Transition time, low-to-high-level output		95		35		30		
t_{THL}	Transition time, high-to-low-level output		95		35		30		

NOTE 1: See load circuit and voltage waveforms on page 170.

◊Future products to be announced.

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TYPES TF4009B, TF4010B, TP4009B, TP4010B
HEX INVERTING AND NONINVERTING BUFFERS/CONVERTERS

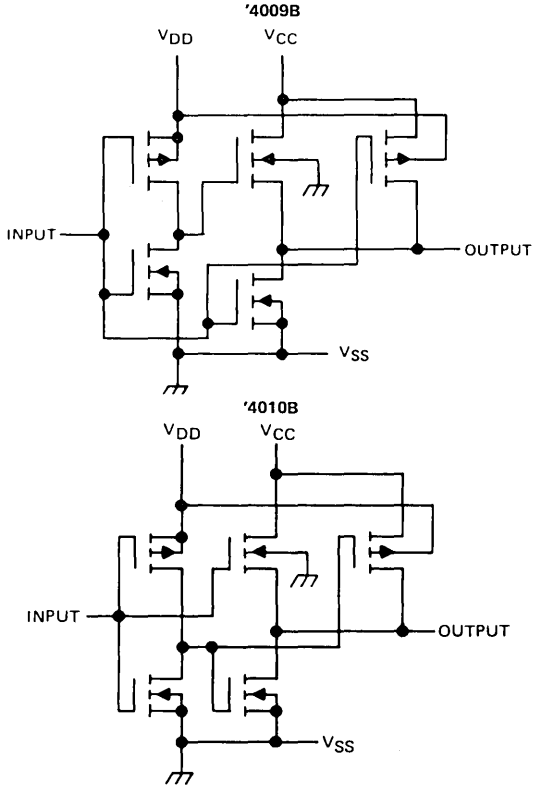
SEPTEMBER 1975

- High Current Sinking Capability

description

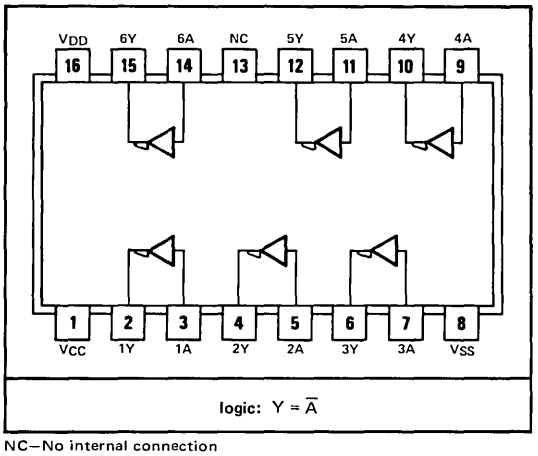
The '4009B and '4010B hex CMOS inverting and noninverting buffers may be used as current sinks for source drivers, hex CMOS drivers, or CMOS to DTL or TTL logic-level converters. Conversion ranges are from CMOS logic operating at supply levels to 18 volts to DTL or TTL operating at supply levels of 3 volts to 18 volts. Conversion to logic output levels greater than 6 volts is permitted provided that the V_{CC} supply voltage is not higher than the V_{DD} supply voltage (see Note 1).

schematic (each buffer)



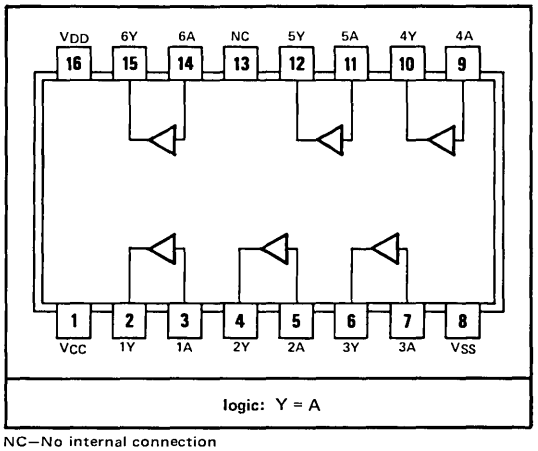
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

TF4009B, TP4009B



NC—No internal connection

TF4010B, TP4010B



NC—No internal connection

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24 and below	Page 24	Pages 24 and 25, group 1, except as on following page

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} (see Note 1) . . . . . V_{DD}
Minimum rise time of supply voltages . . . . . 10 μs
Output load capacitance if V_{CC} exceeds 10.5 V . . . . . 5000 pF

NOTE 1: If V_{CC} is allowed to exceed V_{DD}, the device may latch up and draw sufficient current to cause permanent damage.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = V_{DD}$

TF4009B and TF1010B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level output voltage			4		8		12		V
V_{IL}	Low-level output voltage		TF4009B		1		2		2	V
			TF4010B		1		2		3	
V_{OH}	High-level output voltage	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $I_O = 0$		4.6		9.5		13.5		V
		$V_{IH} = V_{DD}$, $V_{IL} = 0$, $I_O = I_{OH}$ min		4.6		9.5		13.5		
V_{OL}	Low-level output voltage	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $I_O = 0$			0.4		0.5		1.5	V
		$V_{IH} = V_{DD}$, $V_{IL} = 0$, $I_O = I_{OL}$ min			0.4		0.5		1.5	
I_{OL}	Low-level output current	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $V_O = V_{OL}$ max	$T_A = -55°C$	3.75		10		30		mA
			$T_A = 25°C$	3.2		8		24		
			$T_A = 125°C$	2.1		5.6		17		
		$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $V_O = ½ V_{DD}$	$T_A = -55°C$	11		36		53		
			$T_A = 25°C$	9.2		29		42		
			$T_A = 125°C$	6		20		30		

TP4009B and TP4010B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			4		8		12		V
V_{IL}	Low-level input voltage		TP4009B		1		2		2	V
			TP4010B		1		2		3	
V_{OH}	High-level output voltage	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $I_O = 0$		4.6		9.5		13.5		V
		$V_{IH} = V_{DD}$, $V_{IL} = V_{IL} = 0$, $I_O = I_{OH}$ min		4.6		9.5		13.5		
V_{OL}	Low-level output voltage	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $I_O = 0$			0.4		0.5		1.5	V
		$V_{IH} = V_{DD}$, $V_{IL} = 0$, $I_O = I_{OL}$ min			0.4		0.5		1.5	
I_{OL}	Low-level output current	$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $V_O = V_{OL}$ max	$T_A = -40°C$	3.6		9.6		28		mA
			$T_A = 25°C$	3.2		8		24		
			$T_A = 85°C$	2.5		6.6		19		
		$V_{IH} = V_{IH}$ min, $V_{IL} = V_{IL}$ max, $V_O = ½ V_{DD}$	$T_A = -40°C$	10		34		49		
			$T_A = 25°C$	9.2		29		42		
			$T_A = 85°C$	7.1		24		33		

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{CC} = V_{DD}$, $C_L = 50$ pF, $R_L = 200$ kΩ, See Note 2	55		40		35		ns
t_{PHL}	Propagation delay time, high-to-low-level output		50		28		23		
t_{TLH}	Transition time, low-to-high-level output		135		110		100		
t_{THL}	Transition time, high-to-low-level output		30		28		25		
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{CC} = ½ V_{DD}$, $C_L = 50$ pF, $R_L = 200$ kΩ, See Note 2			25				ns
t_{PHL}	Propagation delay time, high-to-low-level output				25				

NOTE 2: See load circuit and voltage waveforms on page 170.

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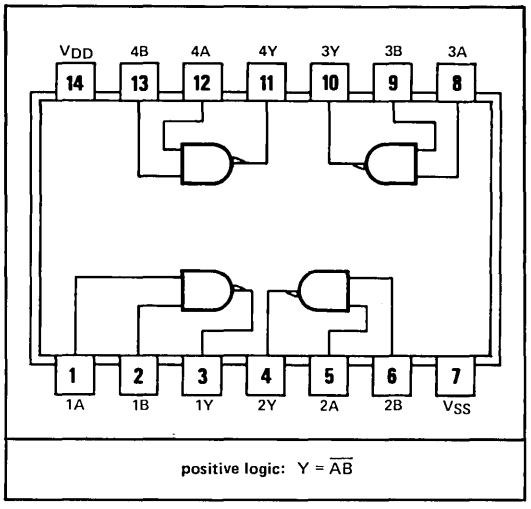
TYPES TF4011B, TF4012B, TP4011B, TP4012B
NAND GATES

SEPTEMBER 1975

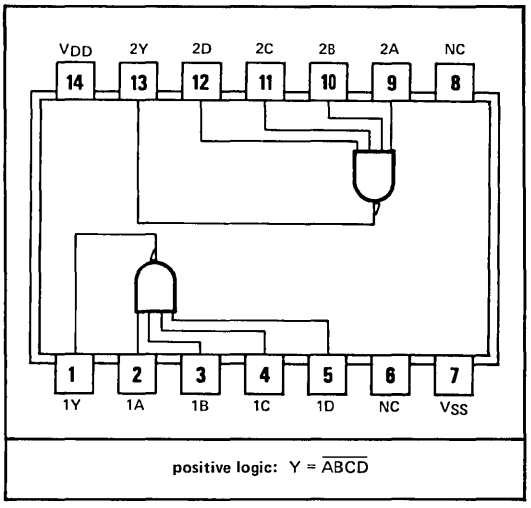
'4011B . . . Quad 2-Input NAND Gates
'4012B . . . Dual 4-Input NAND Gates◇

TF4011B, TP4011B
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

TF4012B, TP4012B◇
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC—No internal connection

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25° C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	175		50		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		175		50		40		
t_{TLH}	Transition time, low-to-high-level output		95		35		30		
t_{THL}	Transition time, high-to-low-level output		95		35		30		

NOTE 1: See load circuit and voltage waveforms on page 170.

◇Future product to be announced.

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TYPES TF4013B, TP4013B
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SEPTEMBER 1975

- Toggle Rate . . . 12 MHz Typical at V_{DD} = 15 V

description

These circuits are dual D-type transition-operated master-slave flip-flops with buffered outputs, independent direct overriding preset and clear inputs, and D and clock inputs. While the clock is low, the data at the D input is entered into the master section, which is isolated from the slave section. On the rising transition of the clock, the D input is disabled and data previously set up in the master section is transferred to the slave section and appears in true form at the Q output.

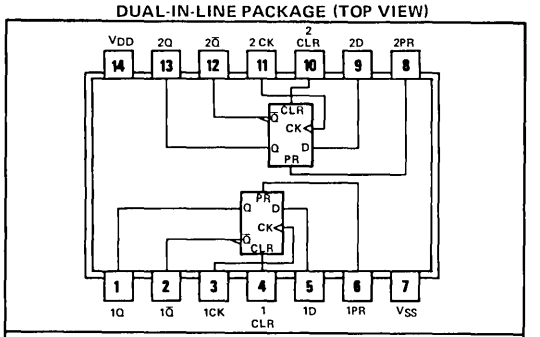
Presetting and clearing are independent of the clock and are accomplished by a high-level voltage at the respective input. The $\overline{Q}$ output is complementary to the Q output except for the nonstable situation that exists when both preset and clear inputs are simultaneously high.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CK	D	Q	$\overline{Q}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H*	H*
L	L	↑	L	L	H
L	L	↑	H	H	L
L	L	L	X	Q_0	$\overline{Q}_0$

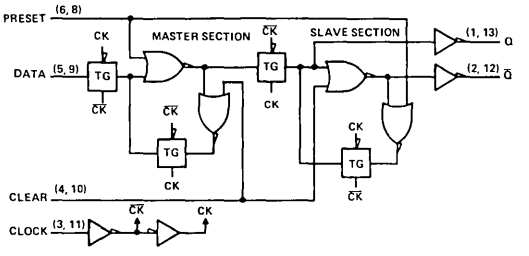
See explanation of function tables on pages 16 and 17.
*This configuration is nonstable; that is, it will not presist when preset and clear return to their inactive (low) level.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

functional block diagram



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

switching characteristics at 25° C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 200 kΩ, See Note 1	4		10		12		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock, preset, or clear		225		95		85		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock, preset, or clear		225		95		85		ns
t_{TLH}	Transition time, low-to-high-level output		95		35		30		ns
t_{THL}	Transition time, high-to-low-level output		95		35		30		ns
$t_{w(min)}$	Minimum pulse width, clock high, clock low, preset, or clear		125		50		40		ns
$t_{su(min)}$	Minimum setup time		25		10		8		ns
$t_{h(min)}$	Minimum hold time		0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

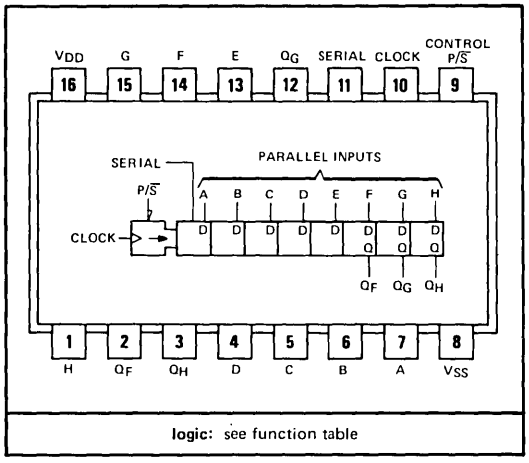
FUTURE CMOS PRODUCT TO BE ANNOUNCED

TYPES TF4014B, TP4014B 8-BIT STATIC SHIFT REGISTERS

SEPTEMBER 1975

- Synchronous Parallel or Serial Input, Serial Output
- Parallel Outputs from Sixth, Seventh, and Eighth Bits
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These 8-bit synchronous registers have a single serial input and parallel-in access to each stage. D-type master-slave flip-flops are used for each stage with parallel access to the outputs of bits F, G, and H.

Both serial and parallel entry are made synchronously on the low-to-high transition of the clock input and under the control of the parallel-load/serial-shift input, P/$\overline{S}$. When the P/$\overline{S}$ input is high, data is broadside loaded into the register from the parallel inputs. When the P/$\overline{S}$ input is low, data is entered at the serial input and each bit shifts one bit position in the direction Q_A through Q_H.

The TF4021B and TP4021B are similar to these registers, except for having asynchronous parallel inputs.

specifications

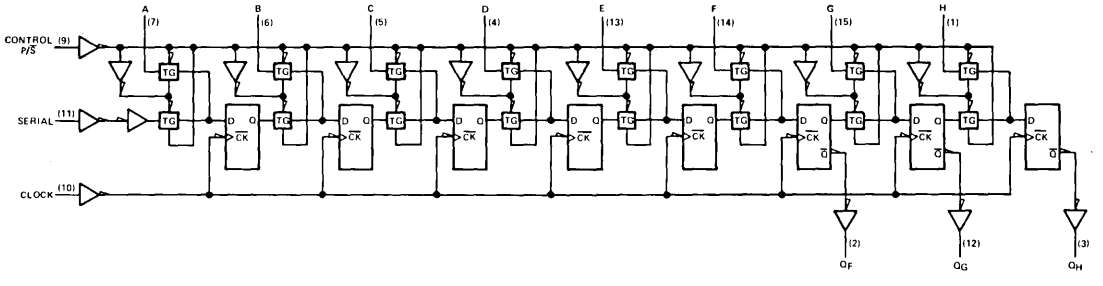
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

FUNCTION TABLE

INPUTS				INTERNAL OUTPUTS (2 of 5)		OUTPUTS		
CONTROL P/$\overline{S}$	CLOCK	PARALLEL A-H	SERIAL	Q_A	Q_B	Q_F	Q_G	Q_H
H	↑	a-h	X	a	b	f	g	h
L	↑	X	H	H	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	↑	X	L	L	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
X	L	X	X	Q_{A0}	Q_{B0}	Q_{F0}	Q_{G0}	Q_{H0}

See explanation of function tables on pages 16 and 17.

functional block diagram



switching characteristics at 25° C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		5		7		MHz
t_{PLH}	Propagation delay time, low-to-high-level output		300		125		90		ns
t_{PHL}	Propagation delay time, high-to-low-level output		300		125		90		ns
t_{TLH}	Transition time, low-to-high-level output		95		35		30		ns
t_{THL}	Transition time, high-to-low-level output		95		35		30		ns
$t_{w(min)}$	Minimum pulse width, clock high or clock low		200		100		100		ns
$t_{su(min)}$	Minimum setup time		100		50		50		ns
$t_{h(min)}$	Minimum hold time		0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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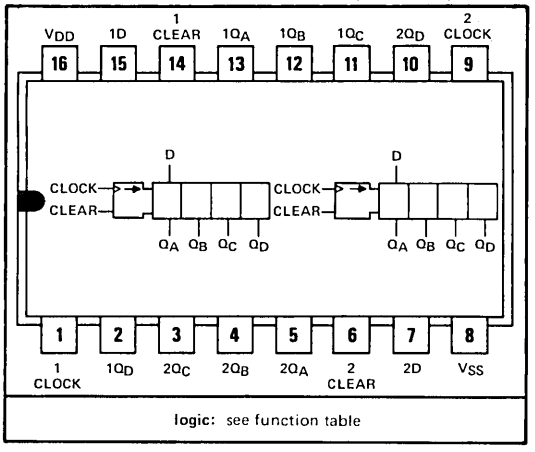
FUTURE CMOS PRODUCT TO BE ANNOUNCED

TYPES TP4015B, TP4015B DUAL 4-BIT STATIC SHIFT REGISTERS

SEPTEMBER 1975

- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

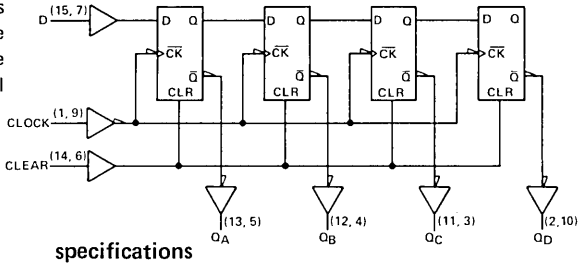


logic: see function table

description

These dual 4-bit static shift registers consist of two identical, independent, 4-stage serial-input, parallel-output registers. Each register has independent clock and clear inputs as well as a single serial data input. The register stages are D-type master-slave flip-flops with Q outputs available from each of the four bits on both registers. Data is shifted from one bit to the next during the low-to-high-level transition of the clock. A high level applied to the clear line sets all outputs of the associated registers to the low level.

functional block diagram (each register)



FUNCTION TABLE (EACH REGISTER)

INPUTS			OUTPUTS			
CLEAR	CLOCK	D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	L	L	L
L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

See explanation of function tables on pages 16 and 17.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

switching characteristics at 25° C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency		C_L = 50 pF, R_L = 200 kΩ, See Note 1	3		5		7		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			250		100		80		ns
t_{PHL}	Propagation delay time, high-to-low-level output	from clock		250		100		80		ns
		from clear		300		125		100		
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width	clock high or low		165		100		75		ns
		clear		125		50		50		
$t_{su(min)}$	Minimum setup time			100		50		50		ns
$t_{h(min)}$	Minimum hold time			0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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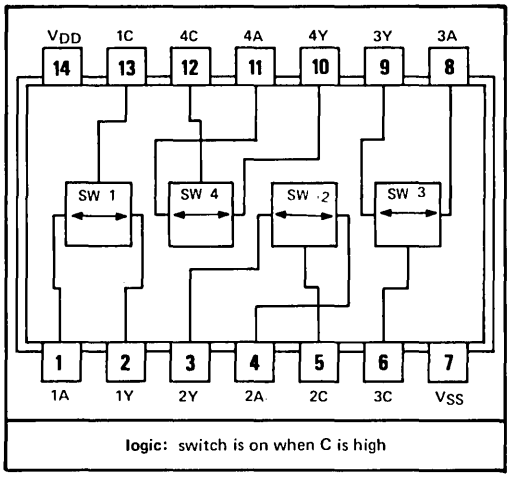
TYPES TF4016B, TP4016B
QUAD BILATERAL SWITCHES

SEPTEMBER 1975

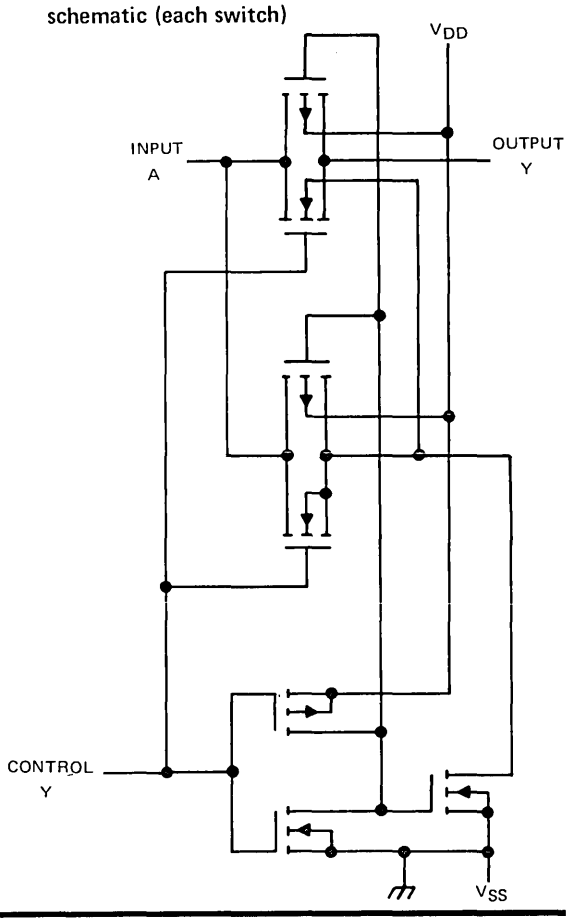
- Difference in r_{on} between Switches in One Package Typically 10 Ω when $V_I = V_{SS}$ or V_{DD}
- High Degree of Linearity . . . < 0.5% Distortion Typical at 1 kHz
- Switches Can Transmit Signals in Either Direction at Frequencies of up to 50 MHz Typically
- Extremely Low Off-State Switch Current Resulting in Very High Effective Off-State Resistance . . . 10 pA Typical at $V_{DD}-V_{SS} = 10$ V
- Maximum Control Input Frequency . . . 10 MHz Typical at $V_{DD} = 10$ V, $C_L = 15$ pF, $R_L = 1$ kΩ
- High On/Off Output Voltage Ratio . . . 65 dB Typical
- Extremely High Control-Input Impedance (Control Circuit Isolated from Switch Circuit) . . . 10^{12} Ω Typical
- Low Crosstalk Between Switches . . . 50 dB Typical at 0.9 MHz, $R_L = 1$ kΩ
- Control Input Current . . . < 10 pA Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: switch is on when C is high

schematic (each switch)



description

The '4016B is a quadruple bilateral switch constructed with P-channel and N-channel enhancement-type devices in a monolithic structure, and finds primary use where low power dissipation and/or high noise immunity is desired.

Applications include digital switching and multiplexing; analog-to-digital and digital-to-analog conversion; digital control of frequency, impedance, phase and analog-signal gain; signal gating; and use as a squelch control, chopper, modulator, demodulator, or commutating switch.

The P^- well of the analog transmission gate is connected to V_{SS} when the control input is low (gate off) and is switched to the analog input when the control input is high (gate on). This provides a more uniform on-state resistance with varying analog input voltages.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	See the following page. Electrical characteristics on pages 24 and 25 do not apply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TF4016B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			3		4		4		V
V_{IL}	Low-level control input voltage				0.9		0.9		0.9	V
V_{OH}	High-level output voltage	A at 0 V, C at V_{IL} max, I_O = 10 μA		4.5		9		12		V
V_{OL}	Low-level output voltage	A at 0 V, C at V_{IH} min, I_O = 10 μA			0.5		1		1	V
	Input-to-output off-state current	A at 0 V to V_{DD}, C at 0 V, Y at 5 V	T_A = 25°C				±125			nA
	Small-signal on-state resistance	A at V_{DD}, ½ V_{DD}, or 0 V, C at V_{DD}, R_L = 10 kΩ to ½ V_{DD}	T_A = −55°C or 25°C				660		400	Ω
			T_A = 125°C				960		600	
I_I	Input current	V_I = V_{DD} or 0 V							±1	μA
	Total Quiescent Current†	A at 0 V to V_{DD}, C at 0 V, Y at 0 V to V_{DD}	T_A = −55°C or 25°C		0.5		1		2	μA
			T_A = 125°C		30		60		120	
		A = Y = 0 V to V_{DD}, C at V_{DD}	T_A = −55°C or 25°C		0.5		1		2	μA
			T_A = 125°C		30		60		120	

TP4016B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level control input voltage			3		4		4		V
V_{IL}	Low-level control input voltage				0.9		0.9		0.9	V
V_{OH}	High-level output voltage	A at 0 V, C at V_{IL} max, I_O = 10 μA		3.5		7		10		V
V_{OL}	Low-level output voltage	A at 0 V, C at V_{IH} min, I_O = 10 μA			1.5		3		5	V
	Input-to-output off-state current	A at 0 V to V_{DD}, C at 0 V, Y at 5 V	T_A = 25°C				±125			nA
	Small-signal on-state resistance	A at V_{DD}, ½ V_{DD}, or 0 V, C at V_{DD}, R_L = 10 kΩ to ½ V_{DD}	T_A = −40°C or 25°C				660		400	Ω
			T_A = 85°C				960		600	
I_I	Input current	V_I = V_{DD} or 0 V							±1	μA
	Total Quiescent Current†	A at 0 V to V_{DD}, C at 0 V, Y at 0 V to V_{DD}	T_A = −40°C or 25°C		5		10		20	μA
			T_A = 85°C		70		140		280	
		A = Y = 0 V to V_{DD}, C at V_{DD}	T_A = −40°C or 25°C		5		10		20	μA
			T_A = 85°C		70		140		280	

†This is the total of supply current, control input current, and input-to-output off-state current.

switching characteristics at 25°C free-air temperature

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
					TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	A	Y	R_L = 10 kΩ,	C_L = 50 pF,	30		15		12		ns
t_{PHL}	A	Y	C at V_{DD},	See Figure 1	30		15		12		
t_{PLH}	C	Y	C_L = 50 pF,	R_L = 10 kΩ to 0 V	80		30		25		ns
t_{PHL}	C	Y	See Figure 2	R_L = 10 kΩ to V_{DD}	80		30		25		

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

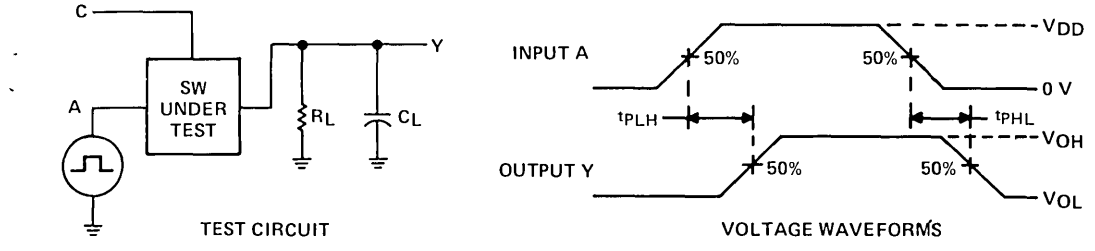

FIGURE 1–PROPAGATION DELAY TIME, SWITCH INPUT A TO OUTPUT Y

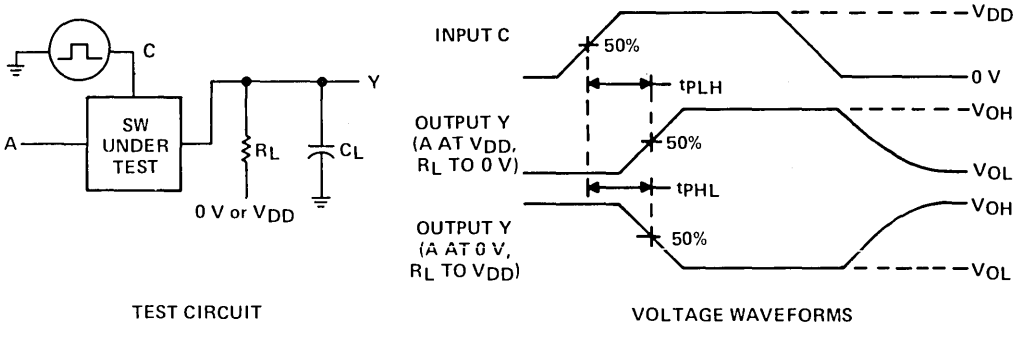

FIGURE 2–PROPAGATION DELAY TIMES, CONTROL INPUT C TO OUTPUT Y

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
B. C_L includes probe and jig capacitance.
C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 1$ MΩ.

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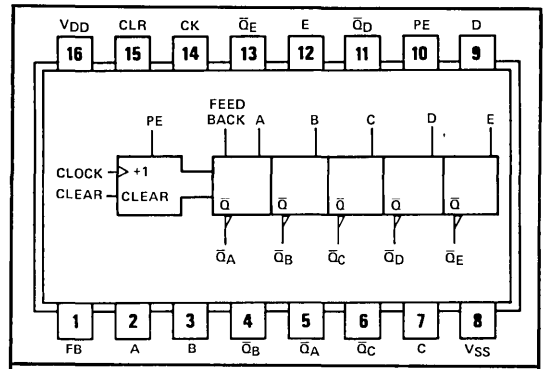
TYPES TF4018B, TP4018B
PRESETTABLE DIVIDE-BY-N COUNTERS

SEPTEMBER 1975

- Maximum Clock Frequency . . . 5 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4018B consist of five Johnson counters, buffered $\overline{Q}$ outputs from each stage, and preset control gating. Clear, preset enable, clock, feedback, and five parallel load inputs are provided.

A high clear signal asynchronously clears the counter so that all $\overline{Q}$ outputs are high. A high preset enable signal asynchronously loads the counter and the $\overline{Q}$ outputs will take on the complements of the parallel inputs. The counter is advanced one count on the low-to-high transition of the clock input.

Various counter configurations may be implemented as follows:

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

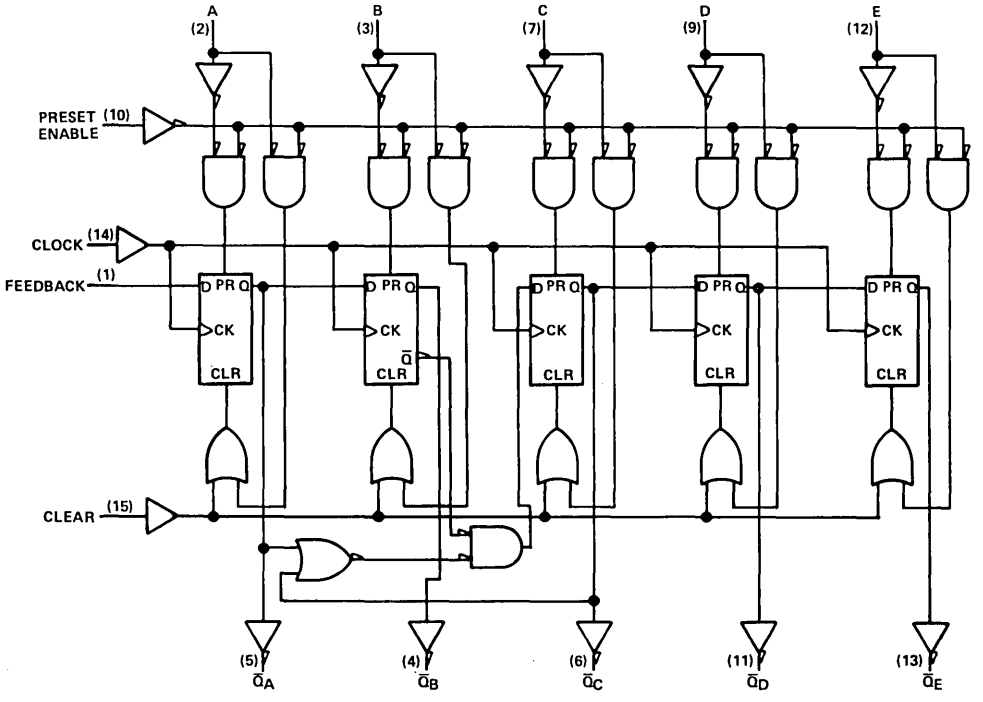
Divide by	Connect These Outputs to Feedback Input	Via	Results from Each $\overline{Q}$ Output (See Timing Diagram)
10	$\overline{Q}_E$	direct	5 counts high, 5 counts low
9	$\overline{Q}_D$, $\overline{Q}_E$	AND gate	5 counts high, 4 counts low
8	$\overline{Q}_D$	direct	4 counts high, 4 counts low
7	$\overline{Q}_C$, $\overline{Q}_D$	AND gate	4 counts high, 3 counts low
6	$\overline{Q}_C$	direct	3 counts high, 3 counts low
5	$\overline{Q}_B$, $\overline{Q}_C$	AND gate	3 counts high, 2 counts low
4	$\overline{Q}_B$	direct	2 counts high, 2 counts low
3	$\overline{Q}_A$, $\overline{Q}_B$	AND gate	2 counts high, 1 count low
2	$\overline{Q}_A$	direct	1 count high, 1 count low

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	V_{DD} = 15 V TYP	V_{DD} = 15 V MAX	UNIT
f_{max}	Maximum clock frequency		C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		5		7		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock, clear, or preset enable	to $\overline{Q}_A$, $\overline{Q}_B$, $\overline{Q}_C$, $\overline{Q}_D$,		500		200		150		ns
		to $\overline{Q}_E$		350		125		100		
t_{PHL}	Propagation delay time, high-to-low-level output from clock, clear, or preset enable	to $\overline{Q}_A$, $\overline{Q}_B$, $\overline{Q}_C$, $\overline{Q}_D$		500		200		150		ns
		to $\overline{Q}_E$		350		125		100		
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width	clock high or low		200		100		75		ns
		clear or preset enable		200		100		75		
$t_{su(min)}$	Minimum setup time	feedback input		75		75		65		ns
		clear or preset enable inactive state		300		100		100		
$t_{h(min)}$	Minimum hold time at feedback input			0		0		0		ns

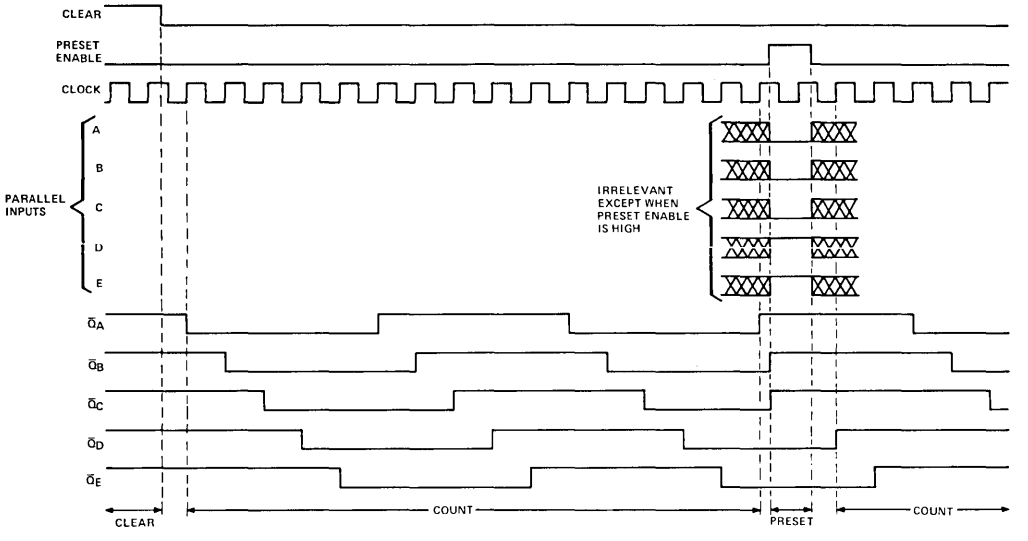
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



typical clear, count, and preset sequence

SHOWN IN DIVIDE-BY-TEN CONFIGURATION, $\overline{Q}_E$ TIED DIRECTLY TO FEEDBACK INPUT



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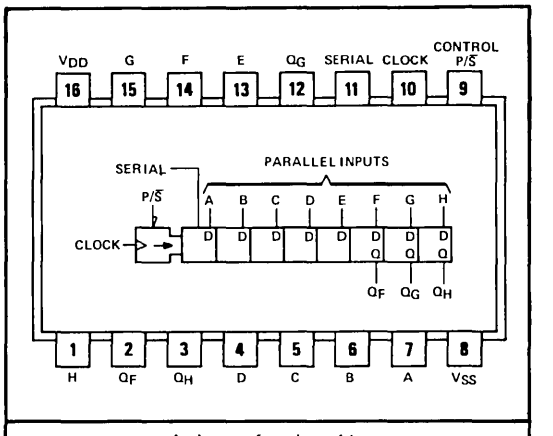
FUTURE CMOS PRODUCT TO BE ANNOUNCED

TYPES TF4021B, TP4021B 8-BIT STATIC SHIFT REGISTERS

SEPTEMBER 1975

- Asynchronous Parallel or Synchronous Serial Input, Serial Output
- Parallel Outputs from Sixth, Seventh, and Eighth Bits
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These 8-bit registers have a single serial input and parallel-in access to each stage. D-type master-slave flip-flops are used for each stage with parallel access to the outputs of bits F, G, and H.

When the parallel-load/serial-shift input, P/$\overline{S}$ is high, data is broadside loaded into the register from the parallel inputs independently of the clock. When the P/$\overline{S}$ input is low, data is synchronously entered at the serial input and each bit shifts one bit position in the direction Q_A toward Q_H. Serial operations occur on the low-to-high transition of the clock input.

The TF4014B and TP4014B are similar to these registers, except for having synchronous parallel inputs.

specifications

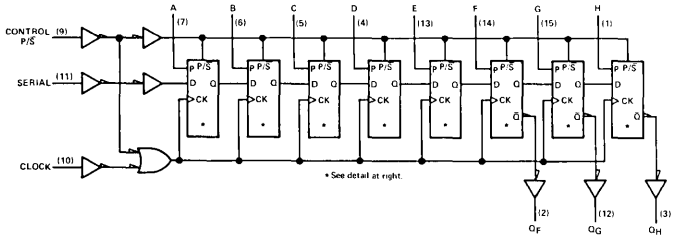
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

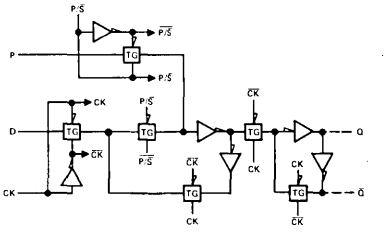
FUNCTION TABLE

INPUTS				INTERNAL OUTPUTS (2 OF 5)		OUTPUTS		
CONTROL P/$\overline{S}$	CLOCK	PARALLEL A-H	SERIAL	Q_A	Q_B	Q_F	Q_G	Q_H
H	X	a-h	X	a	b	f	g	h
L	↑	X	H	H	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	↑	X	L	L	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	L	X	X	Q_{A0}	Q_{B0}	Q_{F0}	Q_{G0}	Q_{H0}

See explanation of function tables, pages 16 and 17.

functional block diagram





DETAIL OF EACH STAGE

TEXAS INSTRUMENTS
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switching characteristics at 25° C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency		C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		5		7		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			300		125		75		ns
t_{PHL}	Propagation delay time, high-to-low-level output			300		125		75		ns
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width	clock high or low		200		100		100		ns
		P/$\overline{S}$ high		200		100		100		
$t_{su(min)}$	Minimum setup time			100		50		50		ns
$t_{h(min)}$	Minimum hold time			0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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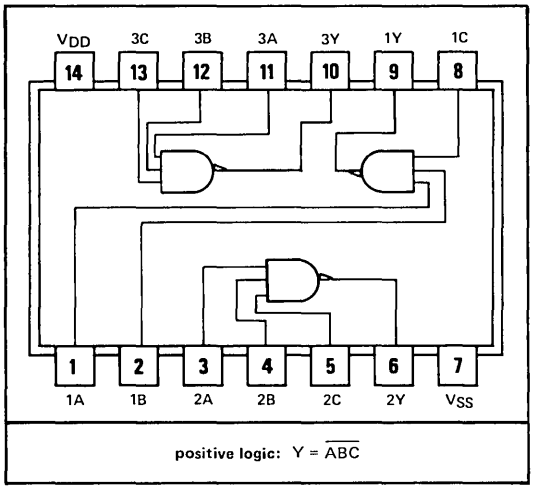
TYPES TF4023B, TF4025B, TP4023B, TP4025B
NAND AND NOR GATES

SEPTEMBER 1975

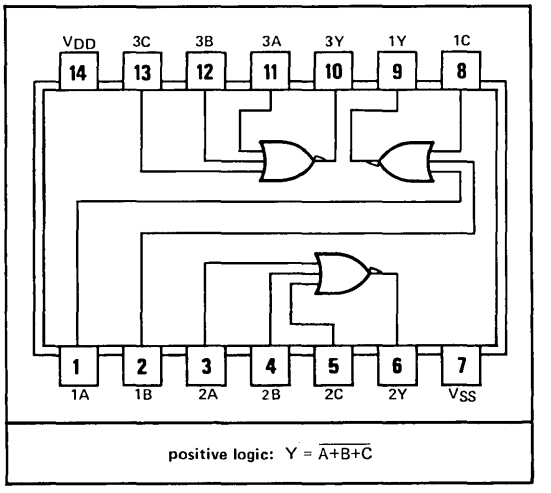
'4023B . . . Triple 3-Input NAND Gates◇
'4025B . . . Triple 3-Input NOR Gates◇

TF4023B, TP4023B◇
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABC}$

TF4025B, TP4025B◇
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A+B+C}$

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	175		50		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		175		50		40		
t_{TLH}	Transition time, low-to-high-level output		95		35		30		
t_{THL}	Transition time, high-to-low-level output		95		35		30		

NOTE 1: See load circuit and voltage waveforms on page 170.

◇Future products to be announced.

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FUTURE CMOS PRODUCT TO BE ANNOUNCED

TYPES TF4029B, TP4029B PRESETTABLE UP/DOWN BINARY/DECADE COUNTERS

SEPTEMBER 1975

- Medium Speed Operation . . . 5 MHz Typical at V_{DD} = 10 V
- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode

description

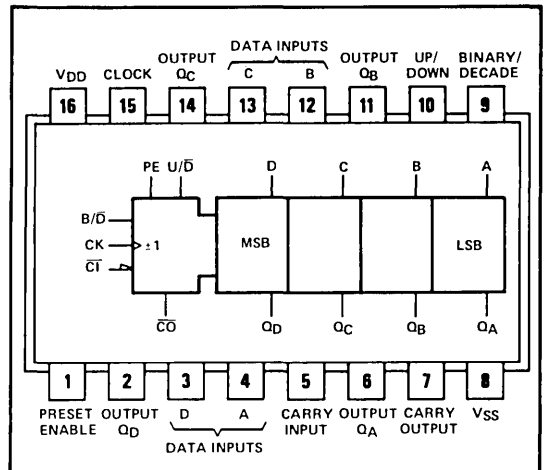
The '4029B counter consists of a four-stage binary or BCD-decade up/down counter with provision for look-ahead carry in both counting modes. The inputs consist of a single clock, carry input (clock enable), binary/decade, up/down, preset enable, and four individual parallel data inputs. Four separate buffered data outputs and a carry output are provided.

A high at the preset-enable input allows information at the parallel inputs to preset the counter to any count independently of the clock. A low at each parallel input, when the preset-enable input is high, resets the counter to its zero count. The counter is advanced one count at the low-to-high transition of the clock when the carry input and preset-enable input are low. Advancement is inhibited when the carry input or preset-enable input is high. The carry output is normally high and goes low when the counter reaches its maximum count in the up mode or its minimum count in the down mode, provided the carry input is low. The carry input terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the binary/decade input is high; the counter counts in the decade mode when the binary/decade input is low. The counter counts up when the up/down input is high, and down when the up/down input is low.

Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Figure 1 of the '4029A data. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple clocking permits longer clock input rise and fall times.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

SUMMARY OF CONTROL INPUT FUNCTIONS
(COMPLETE COUNTER)

CONTROL INPUT	LOGIC LEVEL	FUNCTION
Binary/Decade (B/$\overline{D}$)	H	Binary count
	L	Decade count
Up/Down (U/$\overline{D}$)	H	Count up
	L	Count down
Preset enable (PE)	H	Parallel load
	L	Enable counting
Carry input ($\overline{CI}$)	H	Inhibit counting
	L	Enable counting

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

The waveforms and typical application data given for '4029A on pages 107 and 108 also apply for '4029B.

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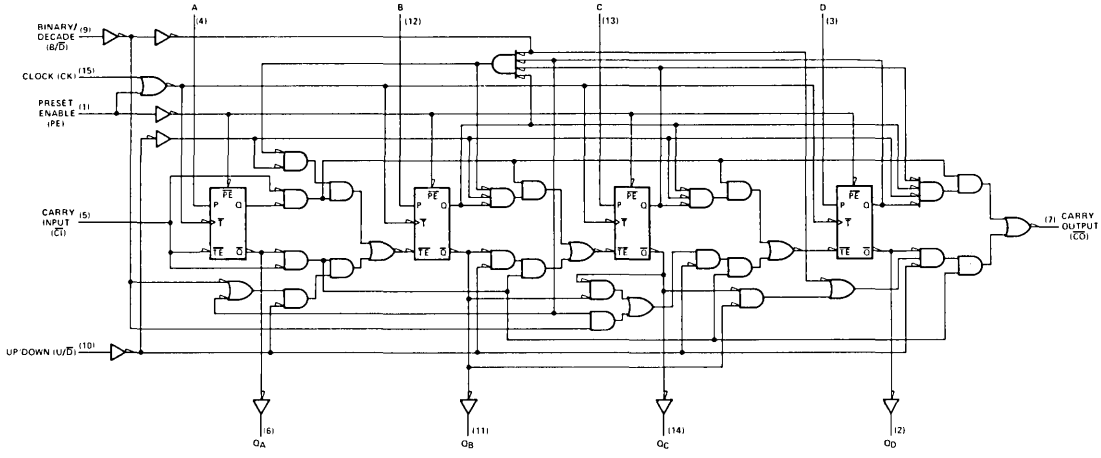
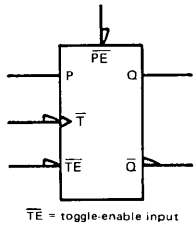
functional block diagram



EACH FLIP-FLOP

SYMBOL



$\overline{TE}$ = toggle-enable input
P = parallel data input
T = toggle input

FUNCTION TABLE
(NOT INCLUDING GATING EXTERNAL TO THE FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PE}$	$\overline{TE}$	$\overline{T}$	P	Q	$\overline{Q}$
L	X	L	H	H	L
L	X	L	L	L	H
H	H	↓	X	Q_n	$\overline{Q}_n$
H	L	↓	X	$\overline{Q}_n$	Q_n
X	X	H	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
Q_n = the level of Q before the most-recent ↓ transition of $\overline{T}$.
Q_0 = the level of Q before the indicated steady-state conditions were established

switching characteristics at 25° C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency		C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		5		7		MHz
t_{PLH} or t_{PHL}	Propagation delay time, low-to-high-level or high-to-low-level output	CK to any Q		325		115		100		ns
		CK to $\overline{CO}$		425		150		125		
		PE to any Q		325		115		100		
		PE to $\overline{CO}$		425		150		125		
		$\overline{CI}$ to $\overline{CO}$		175		50		45		
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width	CK high or low		200		100		75		ns
		PE		115		80		80		
$t_{su(min)}$	Minimum setup time	B/$\overline{D}$, U/$\overline{D}$, or CI		325		115		100		ns
		PE inactive state		325		115		100		
$t_{h(min)}$	Minimum hold time	B/$\overline{D}$, U/$\overline{D}$, or CI		0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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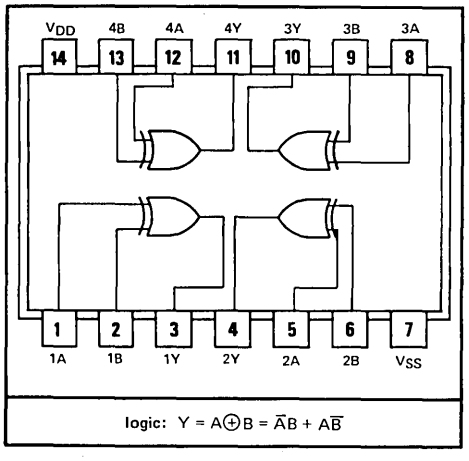
TYPES TF4030B, TP4030B
QUAD EXCLUSIVE-OR GATES

SEPTEMBER 1975

APPLICATIONS INCLUDE:

- Even- and Odd-Parity Generators and Checkers
- Logical Comparators
- Adders and Subtractors
- True/Complement Gating

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



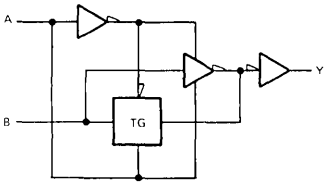
logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

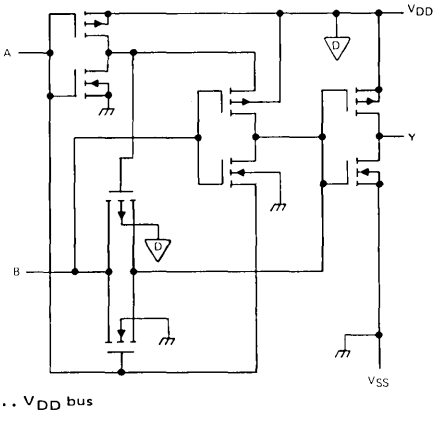
INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

H = high level, L = low level

functional block diagram (each gate)



schematic (each gate)



▽ .... V_{DD} bus

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	110		50		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		110		50		40		ns
t_{TLH}	Transition time, low-to-high-level output		95		35		30		ns
t_{THL}	Transition time, high-to-low-level output		95		35		30		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4035B, TP4035B
4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTERS

SEPTEMBER 1975

- J/$\overline{K}$ Serial Input to First Stage

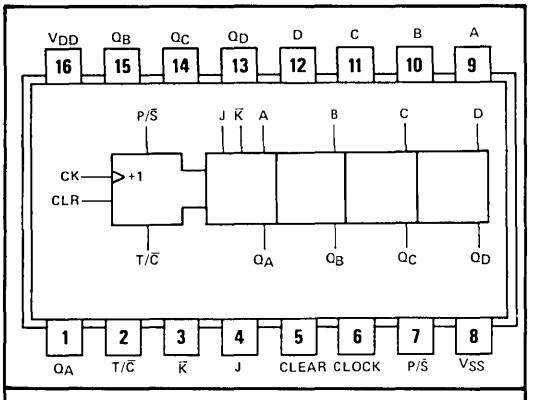
description

These 4-bit synchronous registers have J-$\overline{K}$ serial inputs and parallel access to each stage. D-type master-slave flip-flops are used for each stage with parallel access to the outputs of each stage.

Both serial and parallel entry are made synchronously on the low-to-high transition of the clock input and under the control of the parallel-load/serial-shift input, P/$\overline{S}$. When the P/$\overline{S}$ input is high, data is broadside loaded into the register from the parallel inputs. When the P/$\overline{S}$ is low, data is entered serially from the J and $\overline{K}$ inputs and each bit shifts one bit position in the direction Q_A towards Q_D. The J-$\overline{K}$ inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

When the true/complement input, T/$\overline{C}$, is high, data out is not inverted relative to the inputs, but when T/$\overline{C}$ is low, the data out is inverted.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

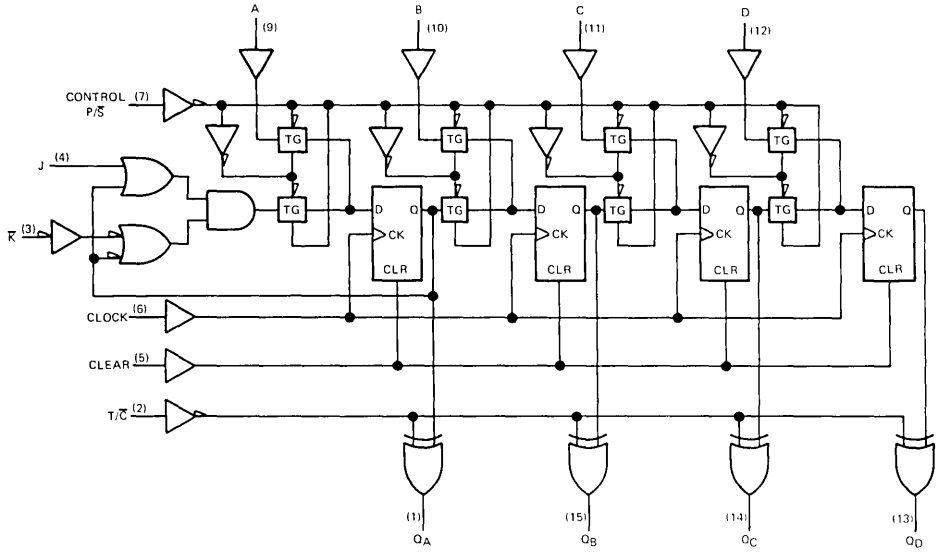
FUNCTION TABLE

INPUTS							OUTPUTS†			
CLEAR	P/$\overline{S}$	CLOCK	PARALLEL A B C D				SERIAL J	SERIAL $\overline{K}$	Q_A	Q_B	Q_C	Q_D
H	X	X	X	X	X	X	X	X	L	L	L	L
L	H	↑	a	b	c	d	X	X	a	b	c	d
L	L	↑	X	X	X	X	L	H	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}
L	L	↑	X	X	X	X	L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
L	L	↑	X	X	X	X	H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	L	↑	X	X	X	X	H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†All output levels shown assume T/$\overline{C}$ is high. If T/$\overline{C}$ goes low, the internal operation of the register is not affected; however, when T/$\overline{C}$ is low, all output levels will be the complement of the data originally entered and of what they would have been if T/$\overline{C}$ had remained high.

See explanation of function tables, pages 16 and 17.

functional block diagram



switching characteristics at 25° C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
f_{max}	Maximum clock frequency		C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		5		7		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock or clear			250		100		80		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock or clear			250		100		80		ns
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width	clock high or low		200		100		75		ns
		clear		125		50		50		
$t_{su(min)}$	Minimum setup time	parallel inputs		100		50		45		ns
		J or $\overline{K}$ inputs		250		100		80		
$t_{h(min)}$	Minimum hold time	parallel inputs		0		0		0		ns
		J or $\overline{K}$ inputs		0		0		0		

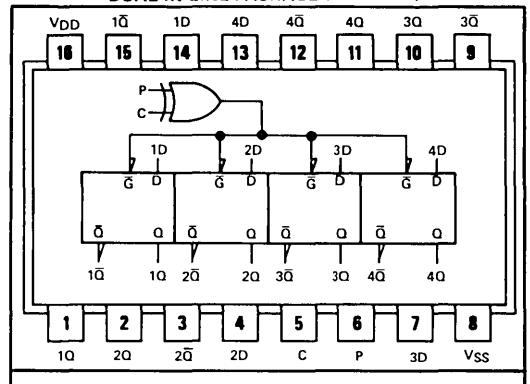
NOTE 1: See load circuit and voltage waveforms on page 170.

TYPES TF4042B, TP4042B
QUAD D-TYPE LATCHES

SEPTEMBER 1975

- Control and Polarity Inputs
- Complementary Outputs

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

The '4042B is a quadruple D-type latch with common control and polarity inputs, C and P. Complementary buffered outputs are available from each latch.

When P is high, C determines the state of all the latches. If C is high, the latches pass data from their D inputs to their Q outputs and the data complement to their $\overline{Q}$ outputs. If C is low, the data is latched.

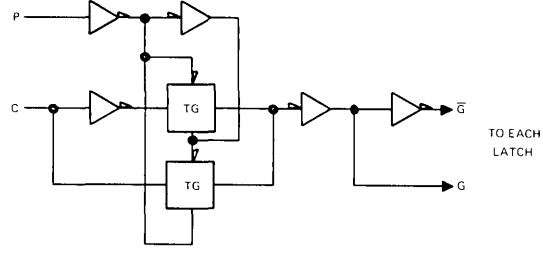
When P is low, C still determines the state of all the latches, but now data is passed when C is low and is latched when C is high.

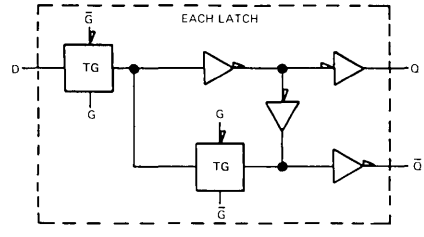
FUNCTION TABLE

P	C	FUNCTION
H	H	Pass data
H	L	Latch data
L	H	Latch data
L	L	Pass data

H = high level, L = low level

functional block diagram





specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

switching characteristics at 25°C free-air temperature

PARAMETER			TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	from C	C_L = 50 pF, R_L = 200 kΩ, See Note 1	150		75		65		ns
		from D		120		40		30		
t_{PHL}	Propagation delay time, high-to-low-level output	from C		150		75		65		ns
		from D		120		40		30		
t_{TLH}	Transition time, low-to-high-level output			95		35		30		ns
t_{THL}	Transition time, high-to-low-level output			95		35		30		ns
$t_{w(min)}$	Minimum pulse width, control input set to pass data			150		50		50		ns
$t_{su(min)}$	Minimum data setup time before latching			50		25		25		ns
$t_{h(min)}$	Minimum data hold time after latching			0		0		0		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4043B, TF4044B, TP4043B, TP4044B
QUAD S-R AND $\overline{S}$-$\overline{R}$ LATCHES
WITH 3-STATE OUTPUTS

SEPTEMBER 1975

- 3-State Outputs with Common Enable

description

The '4043B and '4044B are quadruple S-R and $\overline{S}$-$\overline{R}$ latches, respectively, with three-state outputs. Each latch has separate active-high ('4043B) or active-low ('4044B) set and reset inputs. The three-state outputs are controlled by a common output control. When high, this control permits each output to assume the state of the cross-coupled NOR-gate or NAND-gate latch. When the output control is low, all the outputs are in a high-impedance state.

FUNCTION TABLES
(EACH LATCH)
TF4043B, TP4043B

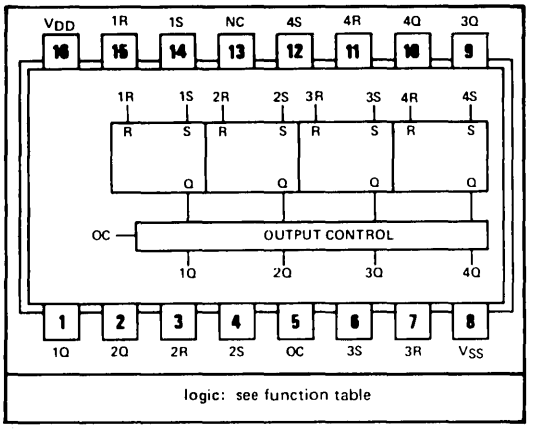
OUTPUT CONTROL	INPUTS S	INPUTS R	OUTPUT Q
L	X	X	Hi-Z
H	L	L	No change
H	H	L	H
H	L	H	L
H	H	H	H*

TF4044B, TP4044B

OUTPUT CONTROL	INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
L	X	X	Hi-Z
H	H	H	No change
H	L	H	H
H	H	L	L
H	L	L	L*

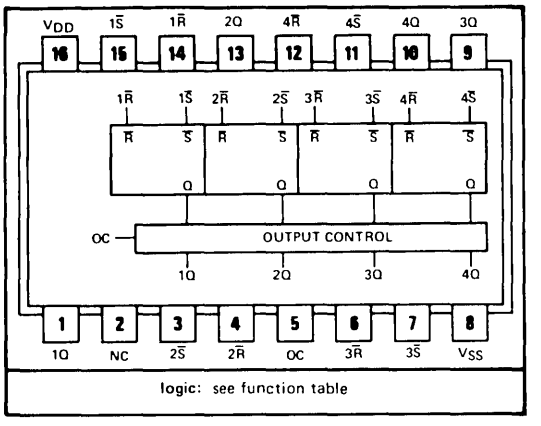
This output level is psuedo stable; that is, it may not persist when the S and R inputs return to their inactive (low) level or the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level. See explanation of function tables, pages 16 and 17.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4043B, TP4043B



NC—No internal connection

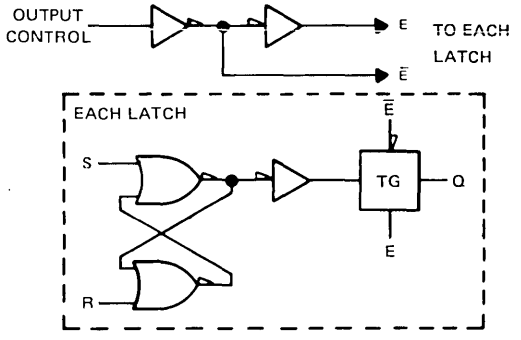
TF4044B, TP4044B



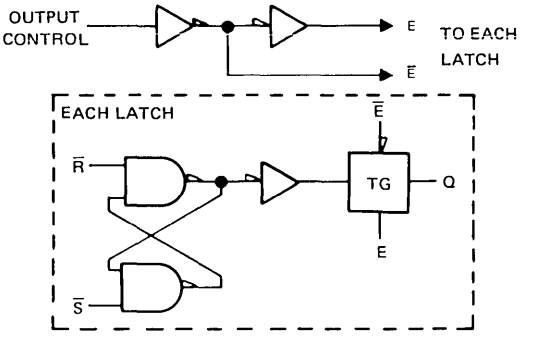
NC—No internal connection

functional block diagrams

TF4043B, TP4043B



TF4044B, TP4044B



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specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2, except as below

electrical characteristics over recommended operating free-air temperature range

TF4043B and TF4044B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OH} min	T_A = −55°C	−0.25		−0.55		−1.9		mA
			T_A = 25°C	−0.2		−0.45		−1.5		
			T_A = 125°C	−0.2		−0.33		−1.2		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −55°C	−1		−3.7		−5.5		
			T_A = 25°C	−0.8		−3		−4.5		
			T_A = 125°C	−0.6		−2		−3		
I_{OL}	Low-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −55°C	0.4		0.8		1.9		mA
			T_A = 25°C	0.3		0.6		1.5		
			T_A = 125°C	0.2		0.45		1.2		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −55°C	1		3.7		5.5		
			T_A = 25°C	0.8		3		4.5		
			T_A = 125°C	0.6		2		3		
I_{OZH}	Off-state output current, high-level voltage applied	OC at V_{SS}, V_O = V_{DD}	T_A = −55°C or 25°C		−0.5		−1		−2	µA
			T_A = 125°C		−7		−14		−28	
I_{OZL}	Off-state output current, low-level voltage applied	OC at V_{SS}, V_O = 0 V	T_A = −55°C or 25°C		0.5		1		2	µA
			T_A = 125°C		7		14		28	

TP4043B and TP4044B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OH} min	T_A = −40°C	−0.22		−0.5		−1.7		mA
			T_A = 25°C	−0.2		−0.45		−1.5		
			T_A = 85°C	−0.2		−0.37		−1.3		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −40°C	−0.9		−3.3		−5		
			T_A = 25°C	−0.8		−3		−4.5		
			T_A = 85°C	−0.65		−2.5		−3.6		
I_{OL}	Low-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −40°C	0.35		0.75		1.7		mA
			T_A = 25°C	0.3		0.6		1.5		
			T_A = 85°C	0.25		0.5		1.3		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −40°C	0.9		3.3		5		
			T_A = 25°C	0.8		3		4.5		
			T_A = 85°C	0.65		2.5		3.6		
I_{OZH}	Off-state output current, high-level voltage applied	OC at V_{SS}, V_O = V_{DD}	T_A = −40°C or 25°C		−0.5		−1		−2	µA
			T_A = 85°C		−7		−14		−28	
I_{OZL}	Off-state output current, low-level voltage applied	OC at V_{SS}, V_O = 0 V	T_A = −40°C or 25°C		0.5		1		2	µA
			T_A = 85°C		7		14		28	

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TEXAS INSTRUMENTS
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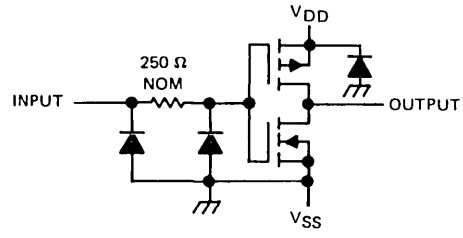
TYPES TF4049B, TF4050B, TP4049B, TP4050B
HEX INVERTING AND NONINVERTING BUFFERS

SEPTEMBER 1975

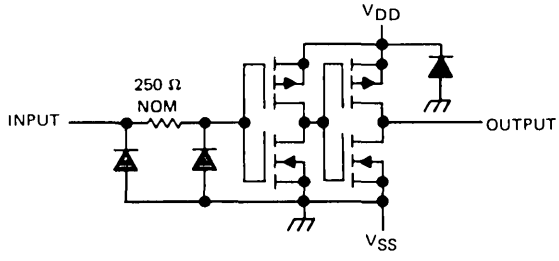
- High Current Sinking Capability

schematic (each buffer)

'4049B



'4050B



description

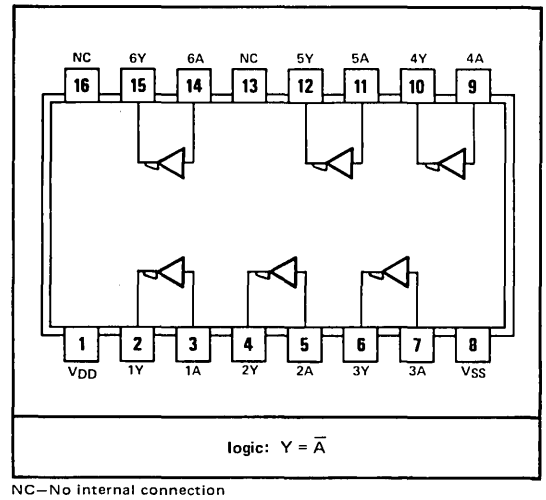
The '4049B and '4050B hex CMOS inverting and noninverting buffers may be used as current sinks or source drivers, hex CMOS drivers, or high-to-low-logic-level (e.g., CMOS to DTL or TTL) converters. Logic-level conversion is accomplished using only one supply voltage (V_{DD}). The high-level input signal (V_{IH}) can exceed the V_{DD} supply voltage when this device is used for logic-level conversions. Table 1 shows the range of voltage levels that can be utilized in these applications. Conversions to logic levels greater than six volts are permitted provided that V_{DD} is less than or equal to V_{IH}.

Since these devices require only one power supply, V_{DD}, they should be used in place of the '4009B and '4010B in all current driver or logic-level conversion applications. They are interchangeable with '4009B and '4010B, respectively, and can be substituted in existing as well as new designs. Pin 16 of the '4049B and '4050B is not internally connected; therefore, any external connection to this pin does not affect circuit operation.

TABLE 1

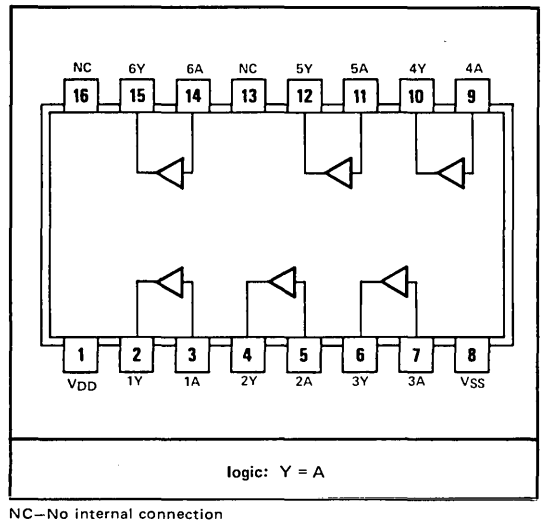
FUNCTION	INPUT HIGH-LEVEL VOLTAGE RANGE	OUTPUT HIGH-LEVEL VOLTAGE RANGE	POWER SUPPLY VOLTAGE RANGE (V_{DD})
Level Shifter	3 to 18 V	3 to 6 V	3 to 6 V
Buffer	3 to 18 V	3 to 18 V	3 to 18 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4049B, TP4049B



NC—No internal connection

TF4050A, TP4050B



NC—No internal connection

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page24	Page 24	Pages 24 and 25, group 1, except as on following page

TEXAS INSTRUMENTS
INCORPORATED
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electrical characteristics over recommended operating free-air temperature range

TF4049B and TF4050B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level output voltage			4		8		12		V
V_{IL}	Low-level output voltage		TF4049B		1		2		2	V
			TF4050B		1		2		3	
V_{OH}	High-level output voltage	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, I_O = 0		4.6		9.5		13.5		V
		V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OH} min		4.6		9.5		13.5		
V_{OL}	Low-level output voltage	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, I_O = 0			0.4		0.5		1.5	V
		V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OL} min			0.4		0.5		1.5	
I_{OL}	Low-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −55°C	3.75		10		30		mA
			T_A = 25°C	3.2		8		24		
			T_A = 125°C	2.1		5.6		17		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −55°C	11		36		53		
			T_A = 25°C	9.2		29		42		
			T_A = 125°C	6		20		30		

TP4049B and TP4050B

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			4		8		12		V
V_{IL}	Low-level input voltage		TP4049B		1		2		2	V
			TP4050B		1		2		3	
V_{OH}	High-level output voltage	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, I_O = 0		4.6		9.5		13.5		V
		V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OH} min		4.6		9.5		13.5		
V_{OL}	Low-level output voltage	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, I_O = 0			0.4		0.5		1.5	V
		V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OL} min			0.4		0.5		1.5	
I_{OL}	Low-level output current	V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = V_{OL} max	T_A = −40°C	3.6		9.6		28		mA
			T_A = 25°C	3.2		8		24		
			T_A = 85°C	2.5		6.6		19		
		V_{IH} = V_{IH} min, V_{IL} = V_{IL} max, V_O = ½ V_{DD}	T_A = −40°C	10		34		49		
			T_A = 25°C	9.2		29		42		
			T_A = 85°C	7.1		24		33		

'4049B switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	80		50		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output		30		20		15		ns
t_{TLH}	Transition time, low-to-high-level output		80		40		30		ns
t_{THL}	Transition time, high-to-low-level output		35		25		20		ns

'4050B switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	100		60		45		ns
t_{PHL}	Propagation delay time, high-to-low-level output		70		40		30		ns
t_{TLH}	Transition time, low-to-high-level output		80		40		30		ns
t_{THL}	Transition time, high-to-low-level output		35		25		20		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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TEXAS INSTRUMENTS
INCORPORATED
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TYPES TF4051B, TF4052B, TF4053B, TP4051B, TP4052B, TP4053B ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SEPTEMBER 1975

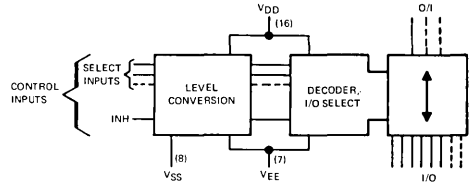
- Difference in r_{on} Between Switches in One Package Typically 5 Ω at $V_{DD}-V_{EE}$ = 15 V
- High Degree of Linearity . . . < 0.1% Distortion Typical at 1 kHz, $V_{DD}-V_{EE}$ = 15 V
- Switches Can Transmit Signals in Either Direction at Frequencies of up to 40 MHz Typically at $V_{DD}-V_{EE}$ = 10 V
- Extremely Low Off-State Switch Current Resulting in Very High Effective Off-State Resistance . . . 10 pA Typical at $V_{DD}-V_{SS}$ = 10 V
- Low Crosstalk Between Switches . . . 40 dB Typical at 1 MHz, R_L = 1 kΩ

description

These devices are analog multiplexers/demultiplexers incorporating built-in level shifting. Any combination of supply voltages is permissable provided that V_{SS} and V_{EE} are each within the range of −3 to −18 volts with respect to V_{DD}. The level shifting is between V_{SS} and V_{EE}. The control input range is V_{SS} to V_{DD} and the analog signal range is V_{EE} to V_{DD}. The common situation of positive digital signals controlling the multiplexing of both positive and negative analog signals can be accommodated. The table indicates some of the possible combinations of supply, input, and output voltages.

TYPICAL SUPPLY AND SIGNAL VOLTAGES

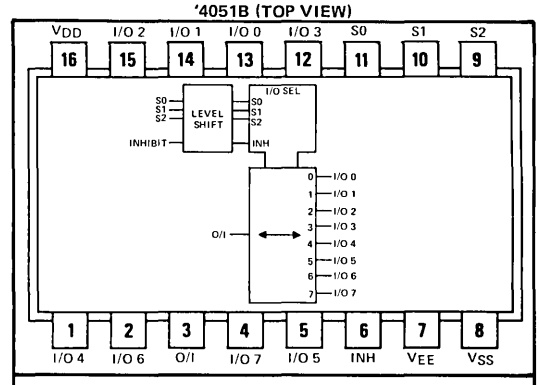
V_{DD}	15 V	10 V	7.5 V	7.5 V
V_{SS}	0 V	0 V	0 V	−7.5 V
V_{EE}	0 V	−5 V	−7.5 V	−7.5 V
Control Inputs	0 to 15 V	0 to 10 V	0 to 7.5 V	−7.5 to 7.5 V
Analog Signals	0 to 15 V	−5 to 10 V	−7.5 to 7.5 V	−7.5 to 7.5 V



INTERNAL POWER SUPPLY CONNECTIONS

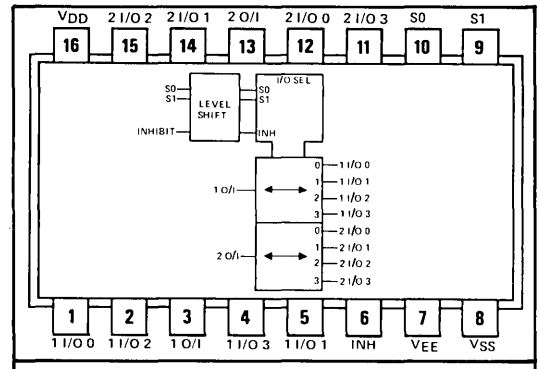
J OR N DUAL-IN-LINE PACKAGES

'4051B (TOP VIEW)



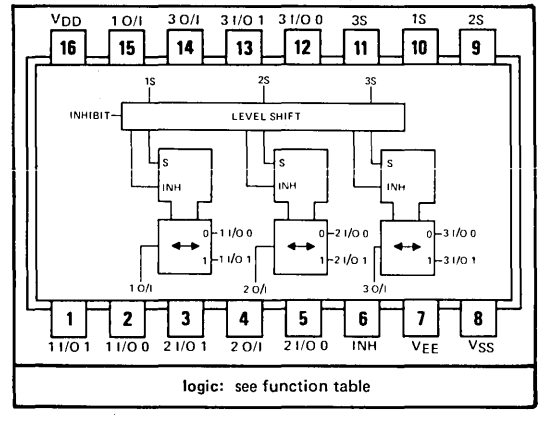
logic: see function table

'4052B (TOP VIEW)



logic: see function table

'4053B (TOP VIEW)



logic: see function table

TEXAS INSTRUMENTS
INCORPORATED
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description (continued)

These digitally controlled bilateral analog switches have low on-state impedance and very low off-state current. When the inhibit input terminal is high, all channels are off.

The '4051B is a single eight-channel multiplexer having three binary control inputs (S0, S1, and S2) and an inhibit input. The three binary signals select one of eight channels to be turned on.

The '4052B is a dual four-channel multiplexer having two binary control inputs (S0 and S1) and an inhibit input. The two binary signals select one of four channels in each of the two sections and the selected channels are respectively paired between the independent sections.

The '4053B is a triple two-channel multiplexer having three separate control inputs (1S, 2S, and 3S) and a common inhibit input. Each input independently selects one of two channels in one of the three sections so that any of eight combinations may be selected.

'4051B
FUNCTION TABLE

INPUTS				CHANNEL
INH	S2	S1	S0	TURNED ON
H	X	X	X	None
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7

'4052B
FUNCTION TABLE
(EACH BILATERAL SWITCH)

INPUTS			CHANNEL
INH	S1	S0	TURNED ON
H	X	X	None
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3

'4053B
FUNCTION TABLE
(EACH BILATERAL SWITCH)

INPUTS		CHANNEL
INH	S	TURNED ON
H	X	None
L	L	0
L	H	1

H = high level, L = low level, X = irrelevant

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24 and below	Page 24	Pages 24 and 25, group 2, except as below. I_{OH} and I_{OL} do not apply

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{EE} (with respect to V_{DD}) . . . . . −18 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted), $V_{EE} = V_{SS} = 0$ V

PARAMETER		TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	Control inputs at V_{IH} min or V_{IL} max, I/O at 0 V, I_O = 10 μA	Channel off,	4.6		9.5		13.5		V
V_{OL}	Low-level output voltage	Control inputs at V_{IH} min or V_{IL} max, I/O at 0 V, I_O = 10 μA	Channel on,		0.4		0.5		1.5	V
	Input-to-output off-state current	Control inputs at 0 V or V_{DD}, I/O at 5 V, O/I at 0 V to V_{DD},	Channel off, T_A = 25°C				±125			nA

on-state resistance at 25°C free-air temperature, R_L = 10 kΩ to 0 V

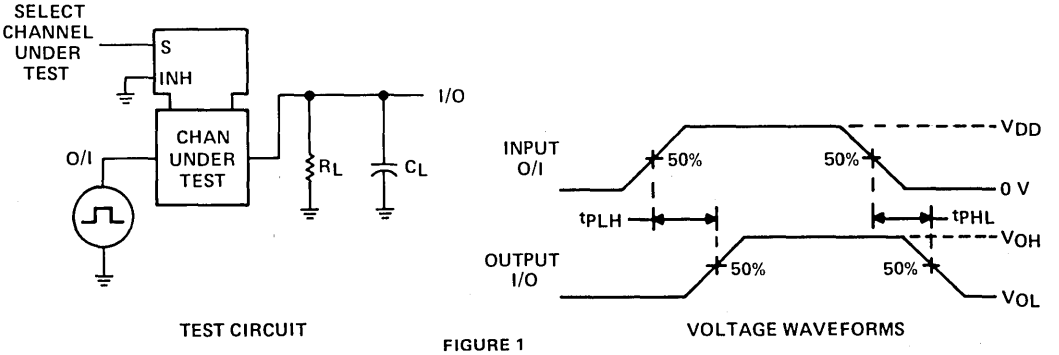
TEST CONDITIONS			TYP	MAX	UNIT
V_{DD} = 7.5 V	V_{EE} = −7.5 V,	V_{SS} = 0 V	80		Ω
V_{DD} = 15 V,	V_{EE} = 0 V,	V_{SS} = 0 V			
V_{DD} = 5 V,	V_{EE} = −5 V,	V_{SS} = 0 V	120		Ω
V_{DD} = 10 V,	V_{EE} = 0 V,	V_{SS} = 0 V			
V_{DD} = 5 V,	V_{EE} = 0 V,	V_{SS} = 0 V	270		Ω

switching characteristics at 25°C free-air temperature, $V_{EE} = V_{SS} = 0$ V

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
					TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	O/I	I/O	R_L = 10 kΩ, C_L = 50 pF,		25		10		8		ns
t_{PHL}	O/I	I/O	See Figure 1		25		10		8		
t_{PLH}	S	I/O	C_L = 50 pF,	R_L = 10 kΩ to 0 V	400		200		170		ns
t_{PHL}	S	I/O	See Figure 2	R_L = 10 kΩ to V_{DD}	400		200		170		
t_{PLH}	INH	I/O	C_L = 50 pF,	R_L = 10 kΩ to 0 V	600		300		250		ns
t_{PHL}	INH	I/O	See Figure 2	R_L = 10 kΩ to V_{DD}	600		300		250		

¶ t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output.

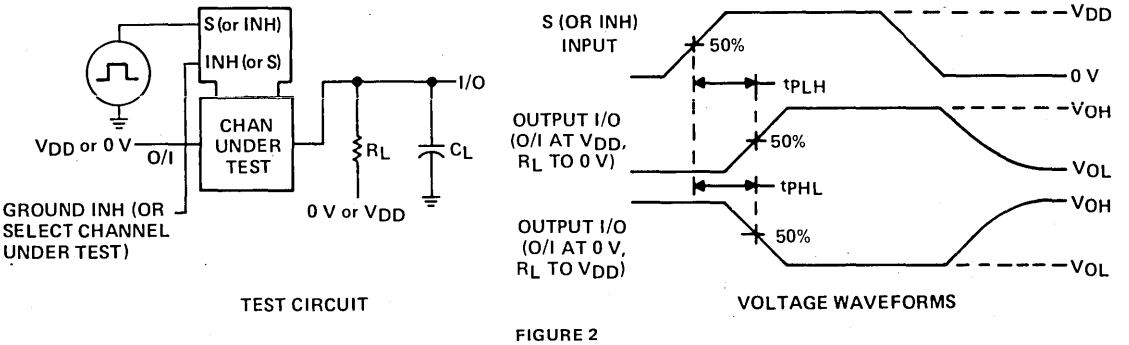
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 1



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 2

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
B. C_L includes probe and jig capacitance.
C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 20$ ns, $R_{in} \geq 1$ MΩ.

TEXAS INSTRUMENTS
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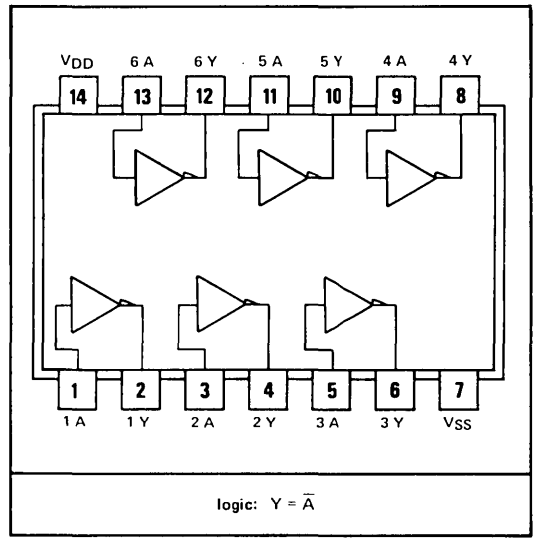
TF4069B, TP4069B
HEX INVERTING BUFFERS

SEPTEMBER 1975

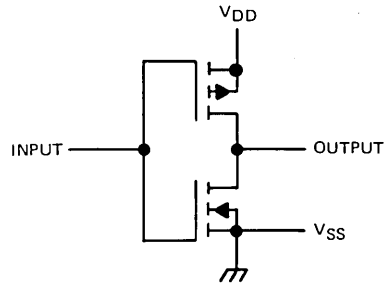
- Designed to be Interchangeable with RCA CD4069B
- Medium Speed Operation $t_{PHL} = t_{PLH} = 40$ ns typ at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: $Y = \overline{A}$

schematic (each buffer)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		125		80		70	ns
t_{PHL}	Propagation delay time, high-to-low-level output			125		80		70	
t_{TLH}	Transition time, low-to-high-level output			200		100		80	ns
t_{THL}	Transition time, high-to-low-level output			200		100		80	

NOTE 1: See load circuit and voltage waveforms on page 170.

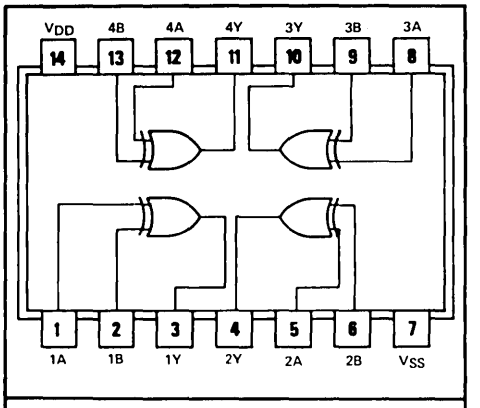
TYPES TF4070B, TP4070B
QUAD EXCLUSIVE-OR GATES

SEPTEMBER 1975

APPLICATIONS INCLUDE:

- Even- and Odd-Parity Generators and Checkers
- Logical Comparators
- Adders and Subtractors
- True/Complement Gating

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



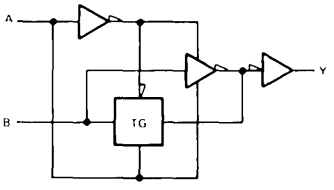
logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

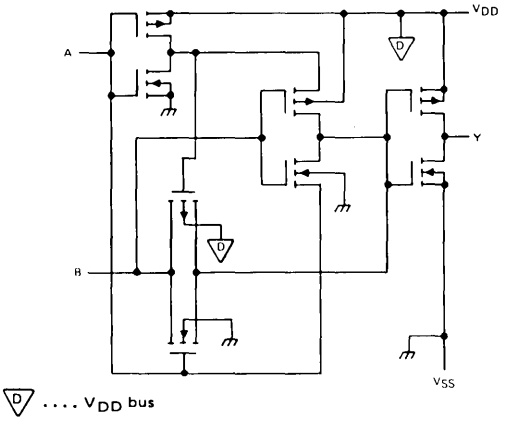
INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

H = high level, L = low level

functional block diagram (each gate)



schematic (each gate)



▽ .... V_{DD} bus

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	175		70		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output		175		70		50		ns
t_{TLH}	Transition time, low-to-high-level output		100		50		40		ns
t_{THL}	Transition time, high-to-low-level output		100		50		40		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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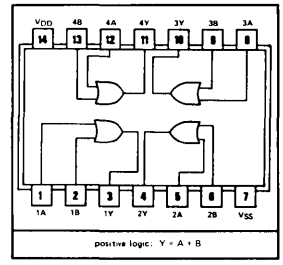
TYPES '4071B, '4072B, '4073B, '4075B, '4081B, '4082B, '4085B OR, AND, AND AND-OR-INVERT GATES

SEPTEMBER 1975

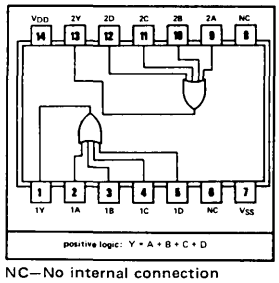
- All Products Available in J or N Dual-In-Line Packages

'4071B . . . Quad 2-Input OR Gates
'4072B . . . Dual 4-Input OR Gates◊
'4073B . . . Triple 3-Input AND Gates◊
'4075B . . . Triple 3-Input OR Gates◊
'4081B . . . Quad 2-Input AND Gates
'4082B . . . Dual 4-Input AND Gates◊
'4085B . . . Dual 3-Wide 2-2-1 Input AND-OR-Invert Gates◊

TF4071B, TP4071B (TOP VIEW)

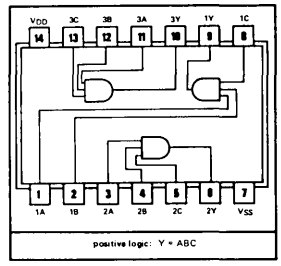


TF4072B, TP4072B (TOP VIEW)◊

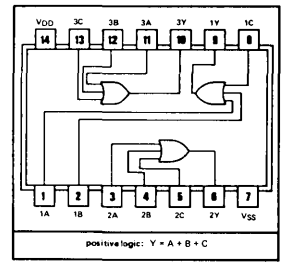


NC—No internal connection

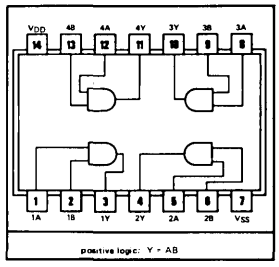
TF4073B, TP4073B (TOP VIEW)◊



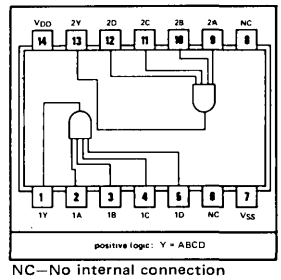
TF4075B, TP4075B (TOP VIEW)◊



TF4081B, TP4081B (TOP VIEW)

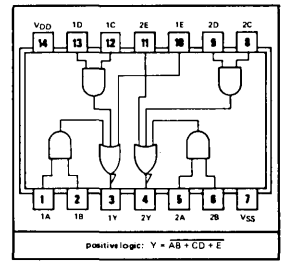


TF4082B, TP4082B (TOP VIEW)◊



NC—No internal connection

TF4085B, TP4085B (TOP VIEW)◊



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	225		65		50		ns
t_{PHL}	Propagation delay time, high-to-low-level output		225		65		50		
t_{TLH}	Transition time, low-to-high-level output		95		35		30		
t_{THL}	Transition time, high-to-low-level output		95		35		30		

NOTE 1: See load circuit and voltage waveforms on page 170.

◊Future products to be announced.

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TYPES TF4376B, TP4376B
QUAD S-R LATCHES

SEPTEMBER 1975

- Same as TF4043B and TP4043B except with Normal 2-State Totem-Pole Outputs

description

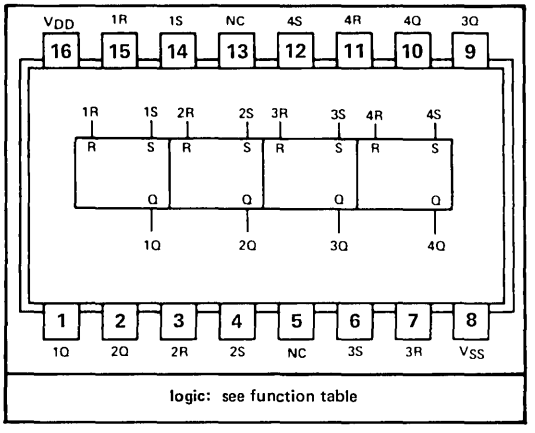
The '4376B is a quadruple S-R latch with normal two-state totem-pole outputs. Each latch has separate active-high set and reset inputs.

FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUT
S	R	Q
L	L	No change
H	L	H
L	H	L
H	H	H*

*This output level is psuedo stable; that is, it may not persist when the S and R inputs return to their inactive (low) level.
See explanation of function tables, pages 16 and 17.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



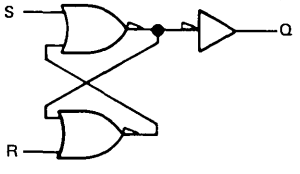
logic: see function table

NC—No internal connection

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

functional block diagram (each latch)



switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 15 V		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	165		70		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output		165		70		60		ns
t_{TLH}	Transition time, low-to-high-level output		85		30		25		ns
t_{THL}	Transition time, high-to-low-level output		85		30		25		ns
$t_{w(min)}$	Minimum R and S pulse width		80		40		35		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4377B, TP4377B
QUAD $\overline{S}$-$\overline{R}$ LATCHES

SEPTEMBER 1975

- Same as TF4044B and TP4044B except with Normal 2-State Totem-Pole Outputs

description

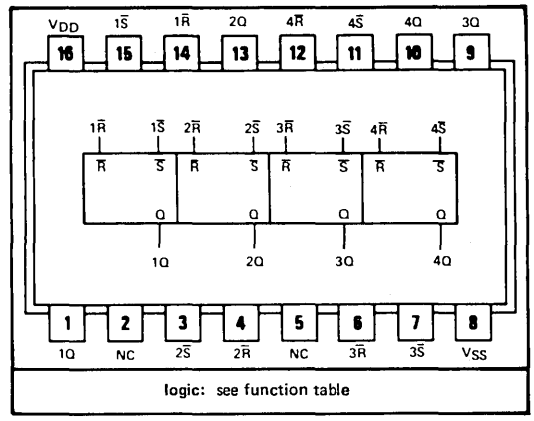
The '4377B is a quadruple $\overline{S}$-$\overline{R}$ latch with normal two-state totem-pole outputs. Each latch has separate active-low set and reset inputs.

FUNCTION TABLE
(EACH LATCH)

INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
H	H	No change
L	H	H
H	L	L
L	L	H*

*This output level is psuedo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
See explanation of function tables, pages 16 and 17.

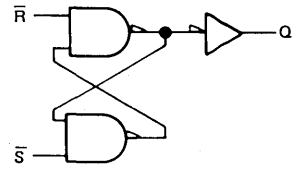
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

NC—No internal connection

functional block diagram (each latch)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 24	Page 24	Pages 24 and 25, group 2

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	V_{DD} = 15 V TYP	V_{DD} = 15 V MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1	165		70		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output		165		70		60		ns
t_{TLH}	Transition time, low-to-high-level output		85		30		25		ns
t_{THL}	Transition time, high-to-low-level output		85		30		25		ns
$t_{w(min)}$	Minimum $\overline{R}$ and $\overline{S}$ pulse width		80		40		35		ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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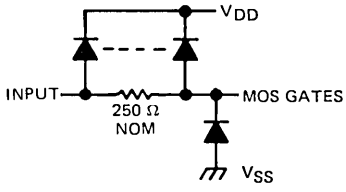
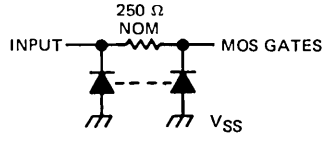
"A" SERIES INFORMATION

INPUT PROTECTION

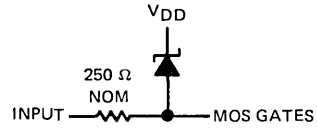
Input protection networks have been standardized to the three configurations below:



CONFIGURATION 1



CONFIGURATION 2



CONFIGURATION 3

Configuration 1 is used on the whole family except for the '4049A and '4050A (which use configuration 2) and the '4518A and '4520A (which use configuration 3). In configurations 1 and 2 the diodes to V_{SS} have a reverse breakdown of approximately 22 to 28 volts. In configuration 3, the breakdown voltage of the zener diode is approximately 25 volts.. These networks are incorporated as protection against occassional electrostatic overstress. It is not recommended that units be subjected to continuously repeated overstress. CMOS is much less sensitive to electrostatic overstress than other MOS technologies; however, care should be taken in handling these networks much the same as is required for other high-impedance integrated circuits:

1) Equipment should be properly grounded.
2) Work surfaces should be electrically conductive and connected to earth ground.
3) Handling should be minimized.

INPUT CHARACTERISTICS

For input voltages between V_{SS} and V_{DD}, the protective networks are in reverse-biased, low-current states. Typically, this reverse current is in the picoampere range at 25°C. When quiescent supply current is measured, all inputs are connected in such a manner that the current through all the inputs is included. The input capacity is typically 3 to 7 pF except for the '4049A for which 15 pF is typical. All unused inputs must be connected to V_{SS} or V_{DD}, whichever is appropriate.

OUTPUT CHARACTERISTICS

The data sheets should be consulted for drive capabilities. Typically, the dc fan-out to other CMOS is 50, but reduced switching speeds are caused by adding capacitive loading. TI data sheets specify switching speeds for C_L = 50 pF or a typical load of 10 CMOS inputs. With 15 pF loads these devices switch at speeds similar to their respective RCA and Motorola equivalents.

NOISE MARGINS

The '4000A series is specified in such a manner as to measure noise immunity by applying V_{IH} min or V_{IL} max to one input at a time while all other inputs are at V_{DD} or V_{SS}, as appropriate. The output is not loaded in this test and is allowed to deviate to the value of V_{OH} min or V_{OL} max in the data sheet.

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SPECIFICATION GROUPING

The products in this book are classified into three groups each having common characteristics. The first group (SSI, small-scale integration) comprises the basic gate functions, the second group (CSSI, complex small-scale integration) comprises the dual flip-flops, buffers, and small analog functions, and the third group (MSI, medium-scale integration) comprises the more complex functions. The type numbers in each group of the "A" series are shown in the following table.

GROUP 1 (SSI)	GROUP 2 (CSSI)	GROUP 3 (MSI)
4000A	4009A	4008A
4001A	4010A	4014A
4002A	4013A	4015A
4007A	4016A	4017A
4011A	4019A	4018A
4012A	4027A	4020A
4023A	4030A	4021A
4025A	4049A	4022A
4301A	4050A	4024A
4302A	4304A	4028A
4303A	4316A	4029A
4311A	4507A	4040A
4315A	4519A	4042A
		4043A
		4044A
		4051A
		4052A
		4053A
		4320A
		4321A
		4360A
		4361A
		4362A
		4363A
		4370A
		4376A
		4377A
		4380A♦
		4512A
		4518A
		4520A
		4522A
		4526A
		4531A
		4581A
		4582A

♦Future products to be announced

SERIES '4000A
COMMON ELECTRICAL SPECIFICATIONS

SEPTEMBER 1975

The following electrical specifications apply for most series '4000A CMOS products. Each individual product specification references the appropriate sections of this common specification and lists exceptions if there are any.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Input current . . . . . ±10 mA
Continuous total dissipation . . . . . 200 mW
Operating free-air temperature range: TF4000A Series . . . . . −55°C to 125°C
TP4000A Series . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Throughout this page, the following page, and the individual product specifications, voltage values are with respect to the V_{SS} terminal unless otherwise noted.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		3	15	V
Input voltage, V_I		0	V_{DD}	V
Operating free-air temperature, T_A	TF4000A Series	−55	125	°C
	TP4000A Series	−40	85	°C
Rise time, any input, t_r			15	μs
Fall time, any input, t_f			15	μs

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electrical characteristics at V_{DD} = 5 V and 10 V

PARAMETER			TEST CONDITIONS†		TF4000A SERIES		TP4000A SERIES		UNIT
					V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
					MIN MAX	MIN MAX	MIN MAX	MIN MAX	
V_{IH}	High-level input voltage			T_A = MIN, 25°C or MAX	3.5	8	3.5	8	V
V_{IL}	Low-level input voltage			T_A = MIN, 25°C, or MAX	1.5	2	1.5	2	V
V_{OH}	High-level output voltage		V_{IH} = V_{DD}, V_{IL} = 0, I_O = 0	T_A = MIN, 25°C, or MAX	4.95	9.95	4.95	9.95	V
			One input at V_{IH} min or V_{IL} max, All other inputs at V_{DD} or 0 V, I_O = 0	T_A = MIN, 25° C, or MAX	4.5	9	4.5	9	
			V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OH} min	T_A = MIN, 25°C, or MAX	2.5	9.5	2.5	9.5	
V_{OL}	Low-level output voltage		V_{IH} = V_{DD}, V_{IL} = 0, I_O = 0	T_A = MIN, 25°C, or MAX	0.05	0.05	0.05	0.05	V
			One input at V_{IH} min or V_{IL} max, All other inputs at V_{DD} or 0 V, I_O = 0	T_A = MIN, 25°C, or MAX	0.5	1	0.5	1	
			V_{IH} = V_{DD}, V_{IL} = 0, I_O = I_{OL} min	T_A = MIN, 25°C, or MAX	0.4	0.5	0.4	0.5	
I_{OH}	High-level output current		V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−0.65	−0.65	−0.35	−0.3	mA
				T_A = 25°C	−0.5	−0.5	−0.3	−0.25	
				T_A = MAX	−0.35	−0.35	−0.25	−0.2	
I_{OL}	Low-level output current		V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	0.5	1.1	0.35	0.75	mA
				T_A = 25°C	0.4	0.9	0.3	0.6	
				T_A = MAX	0.3	0.65	0.25	0.5	
I_{DD} or $-I_{SS}$	Quiescent supply current	Group 1‡ Products	No load, V_I = V_{DD} or 0 V	T_A = MIN or 25°C	0.05	0.1	0.5	5	μA
				T_A = MAX	3	6	15	30	
		Group 2‡ Products		T_A = MIN or 25°C	1	2	10	20	
				T_A = MAX	60	120	140	280	
		Group 3‡ Products		T_A = MIN or 25°C	5	10	50	100	
				T_A = MAX	300	600	700	1400	

electrical characteristics at V_{DD} = 15 V

PARAMETER			TEST CONDITIONS†		TF4000A SERIES		TP4000A SERIES		UNIT
					MIN	MAX	MIN	MAX	
I_I	Input current		V_I = V_{DD} or 0 V	T_A = MIN, 25°C, or MAX		±1		±1	μA
I_{DD} or $-I_{SS}$	Quiescent supply current	Group 1‡ Products	No load, V_I = V_{DD} or 0 V	T_A = MIN or 25°C		1		15	μA
				T_A = MAX		18		90	
		Group 2‡ Products		T_A = MIN or 25°C		6		60	
				T_A = MAX		360		840	
		Group 3‡ Products		T_A = MIN or 25°C		30		300	
				T_A = MAX		1800		4200	

†T_A = MIN or MAX refers to the respective value specified under recommended operating conditions.
‡See group designation on individual product specifications and page 61 for a list of all products by group.

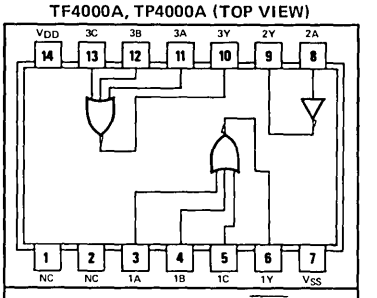
CMOS LOGIC CIRCUITS

TYPES TF4000A, TF4001A, TF4002A, TP4000A, TP4001A, TP4002 AND OTHER NOR GATES

SEPTEMBER 1975

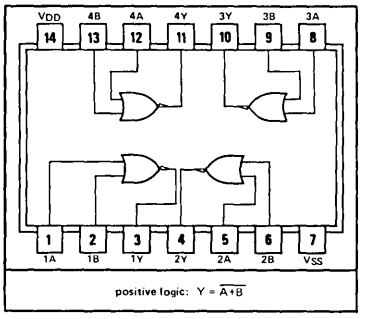
- Designed to be Interchangeable with RCA CD4000A, CD4001A, CD4002A, and CD4025A
- All Products Available in J or N Dual-in-Line Packages
  - '4000 . . . Dual 3-Input NOR Gates Plus Inverters
  - '4001 . . . Quadruple 2-Input NOR Gates
  - '4002 . . . Dual 4-Input NOR Gates
  - '4025 . . . Triple 3-Input NOR Gates

TF4000A, TP4000A (TOP VIEW)

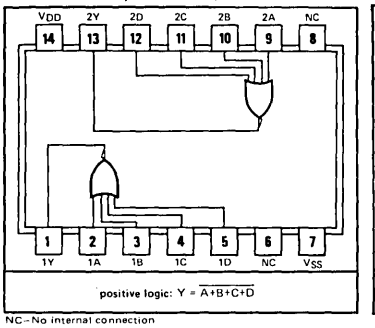


NC–No internal connection

TF4001A, TP4001P (TOP VIEW)

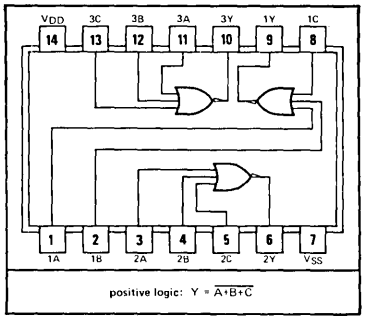


TF4002A, TP4002A (TOP VIEW)

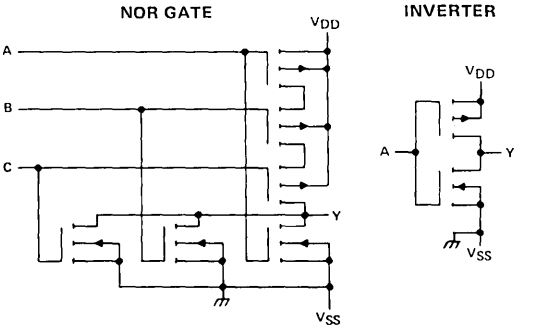


NC–No internal connection

TF4025A, TP4025A (TOP VIEW)



typical schematics



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TF4000A, TF4001A TF4002A, TF4025A				TP4000A, TP4001A TP4002A, TP4025A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF §, R_L = 200 kΩ, See Note 1		150		100		200		130	ns
t_{PHL} Propagation delay time, high-to-low-level output			150		100		200		130	ns
t_{TLH} Transition time, low-to-high-level output			350		175		450		300	ns
t_{THL} Transition time, high-to-low-level output			350		175		450		300	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4000A, CD4001A, CD4002A, and CD4025A, respectively.

NOTE 1: See load circuit and voltage waveforms on page 170.

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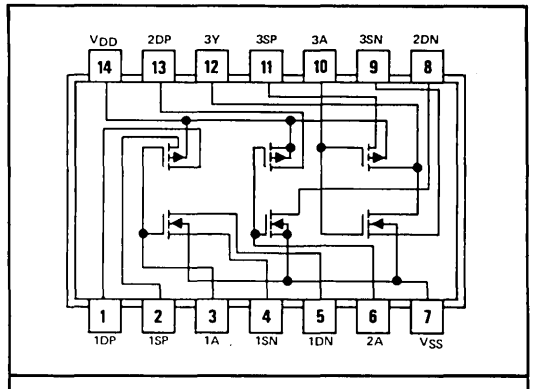
TYPES TF4007A, TP4007A
DUAL COMPLEMENTARY PAIRS PLUS INVERTERS

SEPTEMBER 1975

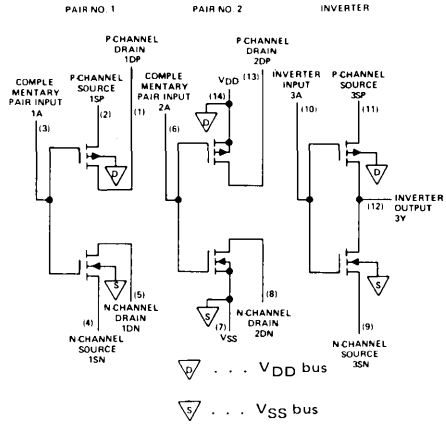
- Designed to be Interchangeable with RCA CD4007A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic with SP connected to V_{DD}, DP to DN (designated "Y"), SN to V_{SS}:
$Y = \overline{A}$

schematic



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1, except as below

electrical characteristics (see note 1)

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4007A				TP4007A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−1.75		−1.35		−1.3		−0.65		mA
			T_A = 25°C	−1.4		−1.1		−1.1		−0.55		
			T_A = MAX	−1		−0.75		−0.9		−0.45		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.75		1.6		0.35		1.2		mA
			T_A = 25°C	0.6		1.3		0.3		1		
			T_A = MAX	0.4		0.95		0.25		0.8		
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C		0.05		0.1		0.5		1	μA
			T_A = MAX		3		6		15		30	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4007A		TP4007A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C		1		3	μA
			T_A = MAX		18		90	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.
NOTE 1: All measurements are made with each pair of transistors connected to form an inverter.

TYPES TF4007A, TP4007A
DUAL COMPLEMENTARY PAIRS PLUS INVERTERS

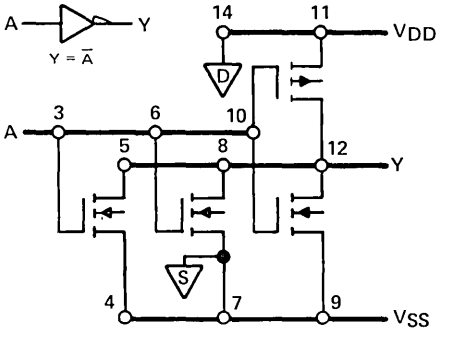
switching characteristics at 25°C free-air temperature (see note 1)

PARAMETER	TEST CONDITIONS	TF4007A				TP4007A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 2		110		90		135		125	ns
t_{PHL} Propagation delay time, high-to-low-level output			110		90		135		125	ns
t_{TLH} Transition time, low-to-high-level output			160		95		220		120	ns
t_{THL} Transition time, high-to-low-level output			160		95		220		120	ns

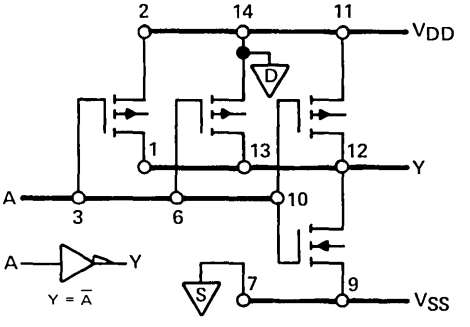
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4007A.

NOTES: 1. All measurements are made with each pair of transistors connected to form an inverter.
2. See load circuit and voltage waveforms on page 170.

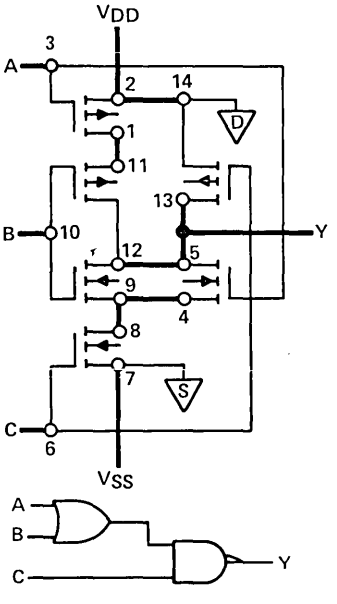
TYPICAL APPLICATION DATA



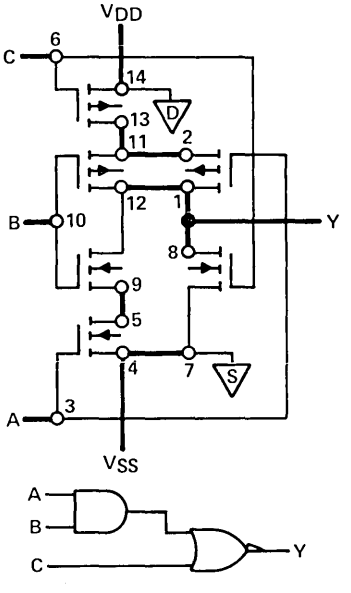
HIGH-SINK-CURRENT DRIVER



HIGH-SOURCE-CURRENT DRIVER

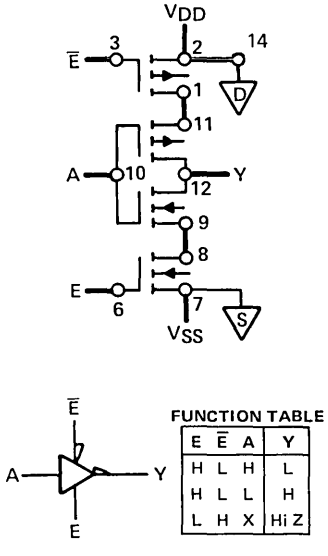


$Y = \overline{AB+C} = \overline{(A+B)C}$



$Y = (\overline{A+B})\overline{C} = \overline{AB+C}$

AOI FUNCTIONS USING RELAY (TREE) LOGIC



FUNCTION TABLE

E	Ē	A	Y
H	L	H	L
H	L	L	H
L	H	X	Hi Z

Y = Ā when E is high
Y = hi Z when E is low

3-STATE BUFFER

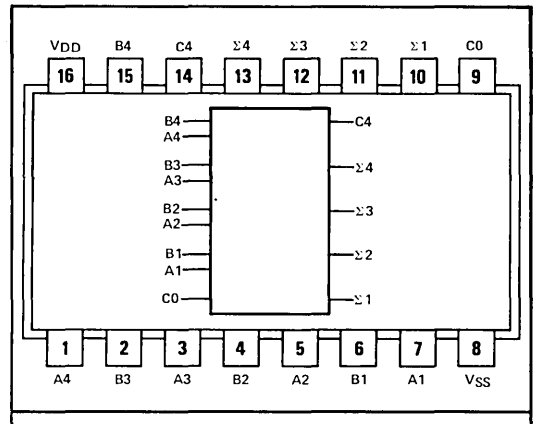
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES TF4008A, TP4008A
FOUR-BIT FULL ADDERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4008A
- High-Speed Operation
- Look-Ahead Carry Output

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion. These circuits feature full look ahead across four bits to achieve partial look-ahead performance with the economy of ripple carry.

FUNCTION TABLE
(EACH BIT)

INPUTS			OUTPUTS	
A_i	B_i	C_{i-1}	C_i	Σ_i
L	L	L	L	L
H	L	L	L	H
L	H	L	L	H
H	H	L	H	L
L	L	H	L	H
H	L	H	H	L
L	H	H	H	L
H	H	H	H	H

H = high level; L = low level;
i = bit number 1, 2, 3, or 4

specifications

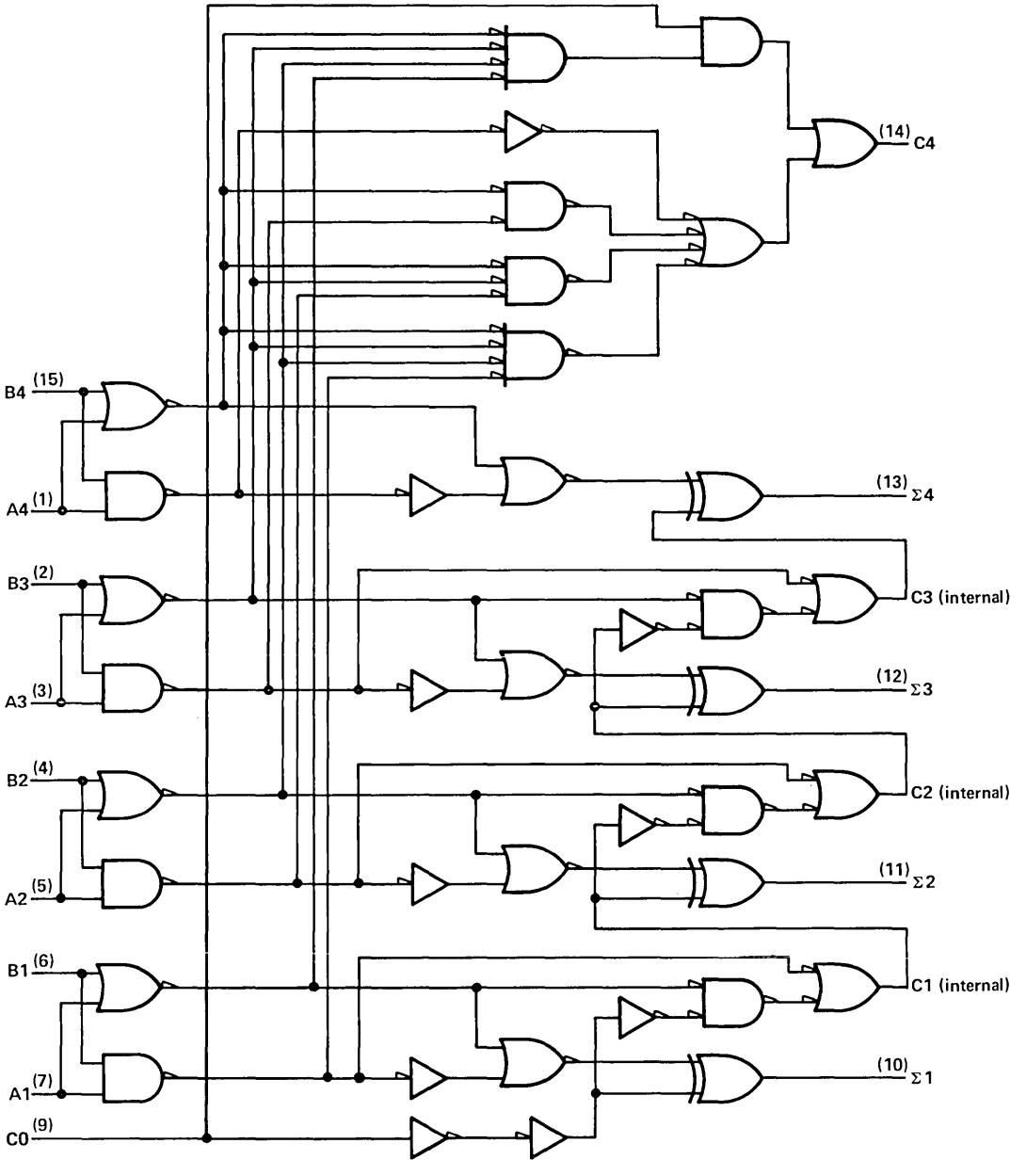
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4008A				TP4008A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A_i or B_i	Σ_i	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		1000		350		1400		500	ns
t_{PHL}					1000		350		1400		500	
t_{PLH}	Any A or B	C4			750		300		1000		350	ns
t_{PHL}					750		300		1000		350	
t_{PLH}	C0	Any Σ			900		325		1200		400	ns
t_{PHL}					900		325		1200		400	
t_{PLH}	C0	C4			350		150		450		200	ns
t_{PHL}					350		150		450		200	
t_{TLH}		C4 or Any Σ			350		150		400		220	ns
t_{THL}					350		150		400		220	

‡t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{TLH} = Transition time, low-to-high-level output
t_{THL} = Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4008A.
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



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TYPES TF4009A, TF4010A, TP4009A, TP4010A
HEX INVERTING AND NONINVERTING BUFFERS/CONVERTERS

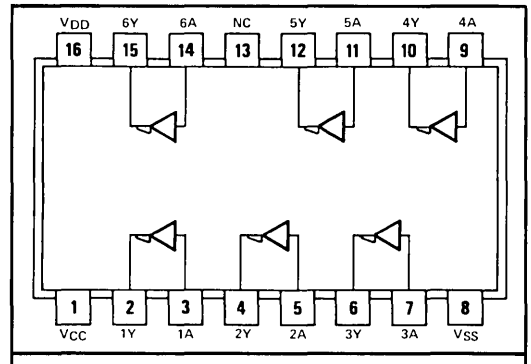
SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4009A and RCA CD4010A
- High Current Sinking Capability . . . 8 mA Minimum at V_{OL} = 0.5 V, V_{DD} = 10 V, T_A = 25°C

description

The '4009A and '4010A hex CMOS inverting and noninverting buffers may be used as current sinks for source drivers, hex CMOS drivers, or CMOS to DTL or TTL logic-level converters. Conversion ranges are from CMOS logic operating at supply levels of 3 volts to 15 volts to DTL or TTL operating at supply levels of 3 volts to 15 volts. Conversion to logic output levels greater than 6 volts is permitted provided that the V_{CC} supply voltage is not higher than the V_{DD} supply voltage (see Note 1).

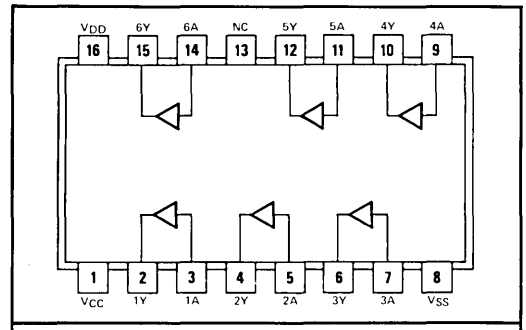
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4009A, TP4009A



logic: $Y = \overline{A}$

NC—No internal connection

TF4010A, TP4010A

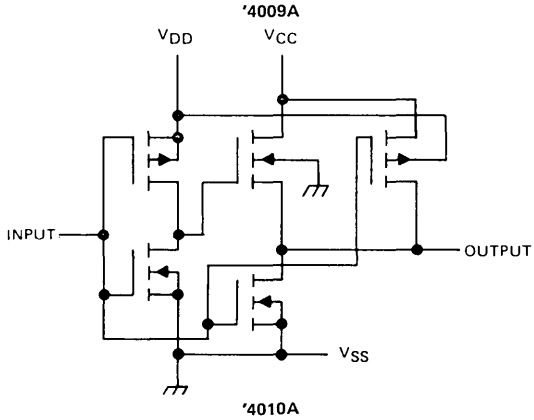


logic: Y = A

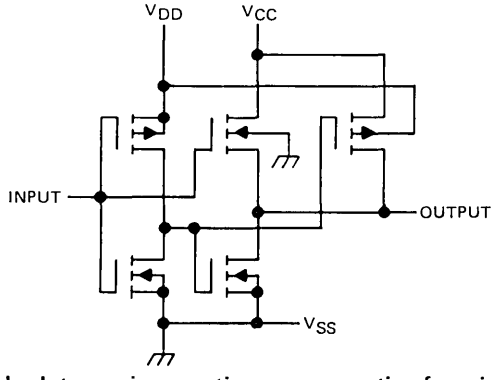
NC—No internal connection

schematic (each buffer)

'4009A



'4010A



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62 and below	Page 62	Page 63, Group 2, except as on following page

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} (see Note 1) . . . . . V_{DD}
Minimum rise time of supply voltages . . . . . 10 μs
Output load capacitance if V_{CC} exceeds 10.5 V . . . . . 5000 pF

NOTE 1: If V_{CC} is allowed to exceed V_{DD}, the device may latch up and draw sufficient current to cause permanent damage.

electrical characteristics, $V_{CC} = V_{DD}$

'4009A only

PARAMETER		TEST CONDITIONS†		TF4009A		TP4009A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
V_{IL}	Low-level input voltage		T_A = MIN or 25°C	1	2	1	2	V
			T_A = MAX	0.9	1.9	0.9	1.9	

'4009A and '4010A at V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4009A, TF4010A		TP4009A, TP4010A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, V_{IL} = 0, $V_O = V_{OH}$ min	T_A = MIN	−1.85	−0.9	−1.5	−0.75	mA
			T_A = 25°C	−1.25	−0.6	−1.25	−0.6	
			T_A = MAX	−0.9	−0.4	−1	−0.5	
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, V_{IL} = 0, $V_O = V_{OL}$ max	T_A = MIN	3.75	10	3.6	9.6	mA
			T_A = 25°C	3	8	3	8	
			T_A = MAX	2.1	5.6	2.4	6.4	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C	0.3	0.5	3	5	μA
			T_A = MAX	20	30	42	70	

'4009A and '4010A at V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4009A, TF4010A	TP4009A, TP4010A	UNIT
				MIN MAX	MIN MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C	1.5	15	μA
			T_A = MAX	90	210	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4009A, TF4010A		TP4009A, TP4010A		UNIT
			V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{CC} = V_{DD}$, C_L = 50 pF§, R_L = 200 kΩ, See Note 2	110	80	140	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output		100	55	125	75	
t_{TLH}	Transition time, low-to-high-level output		270	220	350	270	ns
t_{THL}	Transition time, high-to-low-level output		60	55	80	70	
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{CC} = ½ V_{DD}$, C_L = 50 pF§, R_L = 200 kΩ, See Note 2		45		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			45		65	

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4009A and RCA CD 4010A respectively.
NOTE 2: See load circuit and voltage waveforms on page 170.

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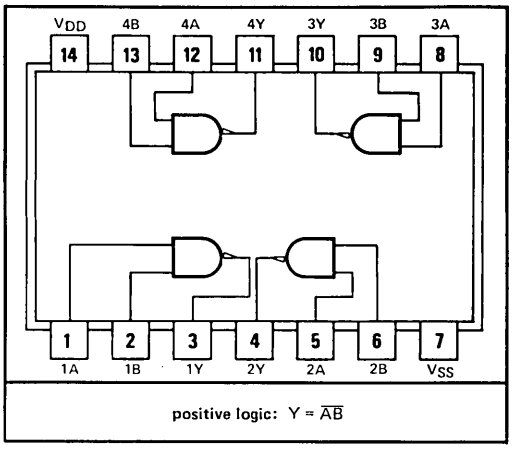
TYPES TF4011A, TP4011A
QUAD 2-INPUT NAND GATES

SEPTEMBER 1975

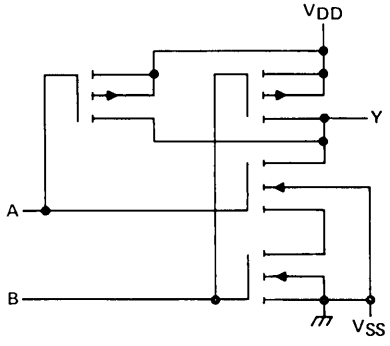
- Designed to be Interchangeable with RCA CD4011A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

schematic (each gate)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1, except as below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4011A		TP4011A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.65	−0.75	−0.35	−0.35	mA
			T_A = 25°C	−0.5	−0.6	−0.3	−0.3	
			T_A = MAX	−0.35	−0.4	−0.25	−0.25	
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.5	1.1	0.25	0.6	mA
			T_A = 25°C	0.4	0.9	0.2	0.5	
			T_A = MAX	0.3	0.65	0.16	0.4	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4011A		TP4011A		UNIT
			V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	150	100	200	130	ns
t_{PHL}	Propagation delay time, high-to-low-level output		150	100	200	130	ns
t_{TLH}	Transition time, low-to-high-level output		350	175	450	300	ns
t_{THL}	Transition time, high-to-low-level output		350	175	450	300	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4011A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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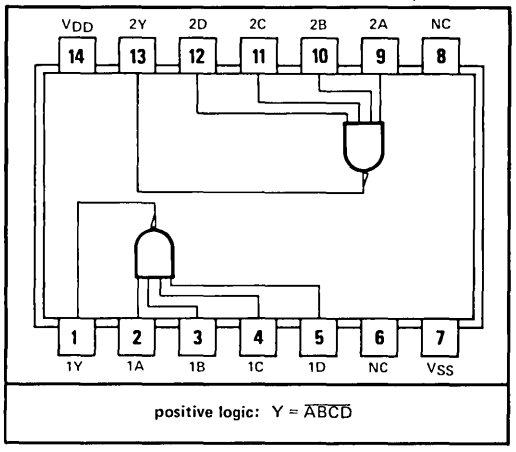
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES TF4012A, TP4012A
DUAL 4-INPUT NAND GATES

SEPTEMBER 1975

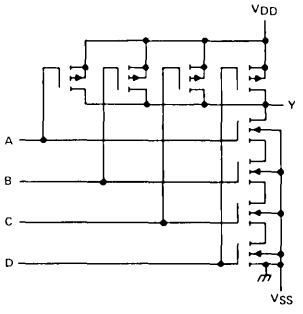
- Designed to be Interchangeable with RCA CD4012A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

schematic (each gate)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1, except as below

electrical characteristics

PARAMETER	TEST CONDITIONS†		TF4012A		TP4012A		UNIT
			V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OL} Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.5	1.1	0.25	0.6	mA
		T_A = 25°C	0.4	0.9	0.2	0.5	
		T_A = MAX	0.3	0.65	0.18	0.4	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TF4012A		TP4012A		UNIT
		V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	150	80	200	110	ns
t_{PHL} Propagation delay time, high-to-low-level output		250	150	400	200	ns
t_{TLH} Transition time, low-to-high-level output		350	175	470	250	ns
t_{THL} Transition time, high-to-low-level output		500	300	670	400	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4012A.
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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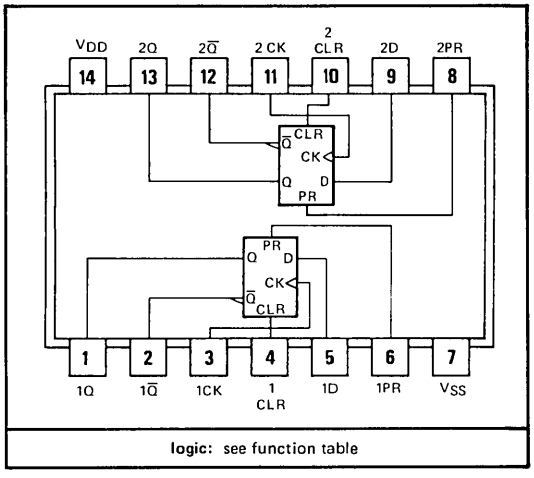
TYPES TF4013A, TP4013A
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4013A
- Toggle Rate . . . 10 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



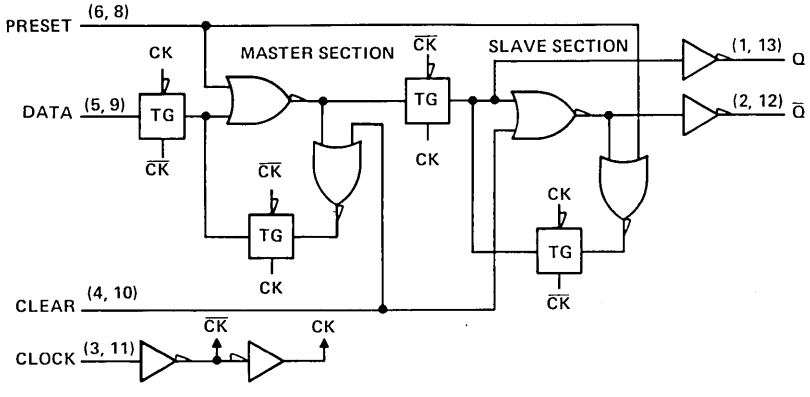
logic: see function table

description

These circuits are dual D-type transition-operated master-slave flip-flops with buffered outputs, independent direct overriding preset and clear inputs, and D and clock inputs. While the clock is low, the data at the D input is entered into the master section which is isolated from the slave section. On the rising transition of the clock, the D input is disabled and data previously set up in the master section is transferred to the slave section and appears in true form at the Q output.

Presetting and clearing are independent of the clock and are accomplished by a high-level voltage at the respective input. The $\overline{Q}$ output is complementary to the Q output except for the nonstable situation that exists when both preset and clear inputs are simultaneously high.

functional block diagram (each flip-flop)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, Group 2, except as on following page

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CK	D	Q	Q̄
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H*	H*
L	L	↑	L	L	H
L	L	↑	H	H	L
L	L	L	X	Q_0	$\overline{Q}_0$

See explanation of function tables on pages 16 and 17.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (low) level.

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recommended operating conditions

		TF4013A				TP4013A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w (C_L = 50 pF)	Clock high or low	200		80		500		100		ns
	Preset or clear	250		100		500		125		
Setup time, t_{su}		40		20		50		25		ns

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4013A				TP4013A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−0.65		−0.8		−0.35		−0.4		mA
			T_A = 25°C	−0.5		−0.65		−0.3		−0.35		
			T_A = MAX	−0.35		−0.45		−0.25		−0.3		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	0.5		1.25		0.35		0.75		mA
			T_A = 25°C	0.4		1		0.3		0.6		
			T_A = MAX	0.3		0.75		0.25		0.5		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4013A				TP4013A				UNIT
				V_{DD} = 5		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	2.5		7		1		5		MHz
t_{PLH} or t_{PHL}	Clock	Q or $\overline{Q}$			420		185		550		250	ns
t_{PLH} or t_{PHL}	Preset or Clear	Q or $\overline{Q}$			420		185		550		250	ns
t_{TLH} or t_{THL}		Any			235		130		300		175	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4013A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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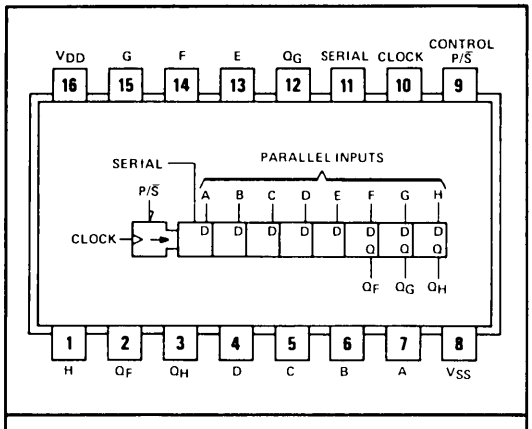
TYPES TF4014A, TP4014A
8-BIT STATIC SHIFT REGISTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4014A
- Synchronous Parallel or Serial Input, Serial Output
- Parallel Outputs from Sixth, Seventh, and Eighth Bits
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These 8-bit synchronous registers have a single serial input and parallel-in access to each stage. D-type master-slave flip-flops are used for each stage with parallel access to the outputs of bits F, G, and H.

Both serial and parallel entry are made synchronously on the low-to-high transition of the clock input and under the control of the parallel-load/serial-shift input, P/$\overline{S}$. When the P/$\overline{S}$ input is high, data is broadside loaded into the register from the parallel inputs. When the P/$\overline{S}$ input is low, data is entered at the serial input and each bit shifts one bit position in the direction Q_A toward Q_H.

The TF4021A, and TP4021A are similar to these registers, except for having asynchronous parallel inputs.

specifications

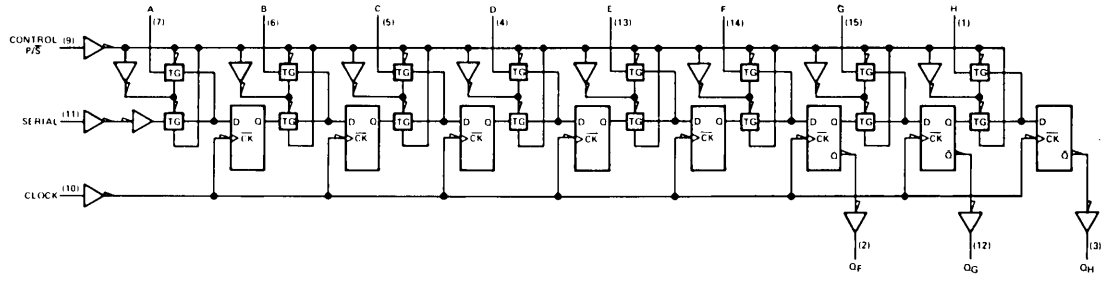
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, Group 3, except as on following page

FUNCTION TABLE

INPUTS				INTERNAL OUTPUTS (2 of 5)		OUTPUTS		
CONTROL P/$\overline{S}$	CLOCK	PARALLEL A-H	SERIAL	Q_A	Q_B	Q_F	Q_G	Q_H
H	↑	a-h	X	a	b	f	g	h
L	↑	X	H	H	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	↑	X	L	L	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
X	L	X	X	Q_{A0}	Q_{B0}	Q_{F0}	Q_{G0}	Q_{H0}

See explanation of function tables, pages 16 and 17.

functional block diagram



recommended operating conditions

		TF4014A				TP4014A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Width of clock pulse, $t_{w(clock)}$	Clock high or low	500		175		830		200		ns
Setup time, t_{su}		350		80		500		100		ns

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4014A				TP4014A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.25		−0.25		−0.12		−0.12		mA
			T_A = 25°C	−0.2		−0.2		−0.1		−0.1		
			T_A = MAX	−0.14		−0.14		−0.08		−0.08		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.15		0.31		0.072		0.12		mA
			T_A = 25°C	0.12		0.25		0.06		0.1		
			T_A = MAX	0.085		0.175		0.05		0.08		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4014A				TP4014A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1		3		0.6		2.5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			975		300		1300		400	ns
t_{PHL}	Propagation delay time, high-to-low-level output			975		300		1300		400	ns
t_{TLH}	Transition time, low-to-high-level output			550		225		700		300	ns
t_{THL}	Transition time, high-to-low-level output			550		225		700		300	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4014A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4015A, TP4015A
DUAL 4-BIT STATIC SHIFT REGISTERS

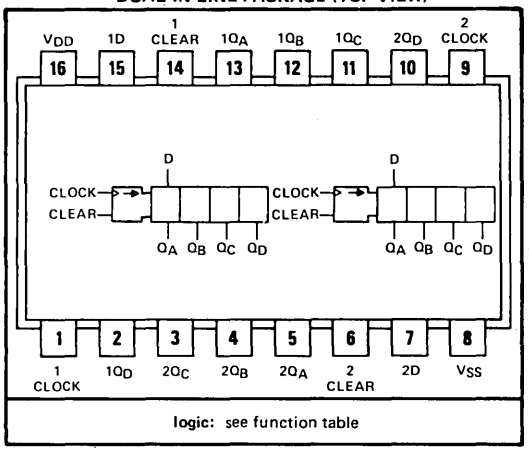
SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4015A
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

description

These dual 4-bit static shift registers consist of two identical, independent, 4-stage serial-input, parallel-output registers. Each register has independent clock and clear inputs as well as a single serial data input. The register stages are D-type master-slave flip-flops with Q outputs available from each of the four bits on both registers. Data is shifted from one bit to the next during the low-to-high-level transition of the clock. A high level applied to the clear line sets all outputs of the associated register to the low level.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

specifications

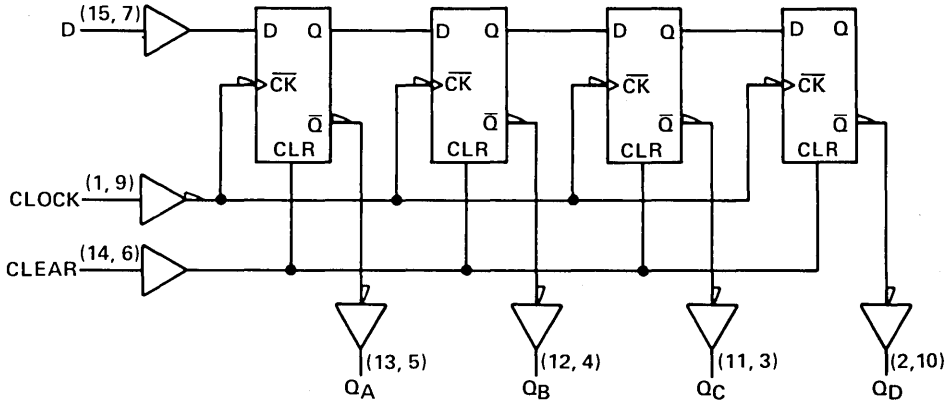
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, group 3

FUNCTION TABLE
(EACH REGISTER)

INPUTS			OUTPUTS			
CLEAR	CLOCK	D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	L	L	L
L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}
L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

See explanation of function tables on pages 16 and 17.

functional block diagram (each register)



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recommended operating conditions

		TF4015A				TP4015A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	500		175		830		200		ns
	Clear	500		175		830		200		
Setup time, t_{su}		350		80		500		100		ns

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4015A				TP4015A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1		3		0.6		2.5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			750		225		1000		300	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock or clear			750		225		1000		300	
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4015A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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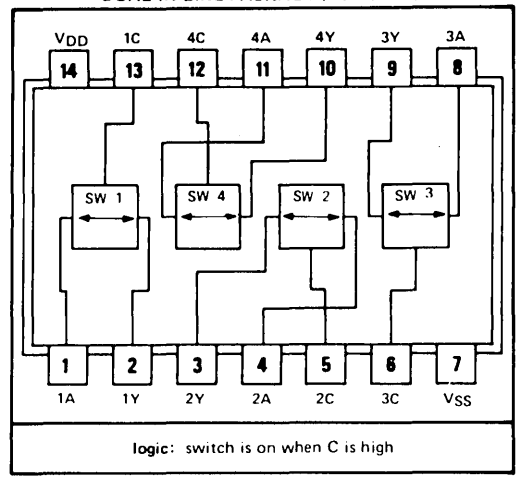
TYPES TF4016A, TP4016A
QUAD BILATERAL SWITCHES

SEPTEMBER 1975

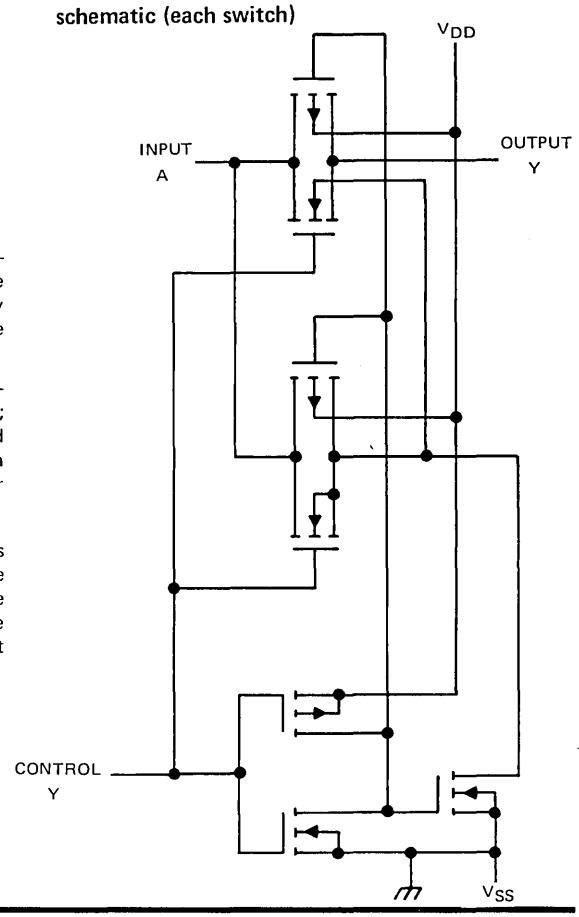
- Designed to be Interchangeable with Motorola MC14016A, Similar to RCA CD4016A (See TF4316A)
- Difference in r_{on} between Switches in One Package Typically 10 Ω when $V_I = V_{SS}$ or V_{DD}
- High Degree of Linearity . . . < 0.5% Distortion Typical at 1 kHz
- Switches Can Transmit Signals in Either Direction at Frequencies of up to 50 MHz Typically
- Extremely Low Off-State Switch Current Resulting in Very High Effective Off-State Resistance . . . 10 pA Typical at $V_{DD}-V_{SS} = 10$ V
- Maximum Control Input Frequency . . . 10 MHz Typical at $V_{DD} = 10$ V, $C_L = 15$ pF, $R_L = 1$ kΩ
- High On/Off Output Voltage Ratio . . . 65 dB Typical
- Extremely High Control-Input Impedance (Control Circuit Isolated from Switch Circuit) . . . 10^{12} Ω Typical
- Low Crosstalk Between Switches . . . 50 dB Typical at 0.9 MHz, $R_L = 1$ kΩ
- Control Input Current . . . < 10 pA Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: switch is on when C is high

schematic (each switch)



description

The '4016A is a quadruple bilateral switch constructed with P-channel and N-channel enhancement-type devices in a monolithic structure, and finds primary use where low power dissipation and/or high noise immunity is desired.

Applications include digital switching and multiplexing; analog-to-digital and digital-to-analog conversion; digital control of frequency, impedance, phase and analog-signal gain; signal gating; and use as a squelch control, chopper, modulator, demodulator, or commutating switch.

The P^- well of the analog transmission gate is connected to V_{SS} when the control input is low (gate off) and is switched to the analog input when the control input is high (gate on). This provides a more uniform on-state resistance with varying analog input voltages.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	See the following page. Page 63 does not apply.

electrical characteristics over recommended operating free-air temperature range

V_{DD} = 5 V and 10 V

PARAMETER	TEST CONDITIONS†		V_{DD} = 5	TF4016A	TP4016A	UNIT
				V_{DD} = 10 V		
			MIN MAX	MIN MAX	MIN MAX	
V_{IH} High-level control input voltage			3	4	4	V
V_{IL} Low-level control input voltage			0.9	0.9	0.9	V
V_{OH} High-level output voltage	A at 0 V, C at V_{IL} max,	I_O = 10 μA	4.5	9	9	V
V_{OL} Low-level output voltage	A at 0 V, C at V_{IH} min,	I_O = 10 μA	0.5	1	1	V
Input-to-output off-state current	A at 0 V to V_{DD}, C at 0 V, Y at 5 V	T_A = 25°C		±125	±125	nA
Total Quiescent Current¶	A at 0 V to V_{DD}, C at 0 V, Y at 0 V to V_{DD}	T_A = MIN or 25°C		1	1	μA
		T_A = MAX		60	16	
	A = Y = 0 V to V_{DD}, C at V_{DD}	T_A = MIN or 25°C		1	1	μA
		T_A = MAX		60	16	

V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TF4016A	TP4016A	UNIT
			MIN MAX	MIN MAX	
I_I Input current	V_I = 0 or V_{DD}		±1	±1	μA
I_{DD} or $-I_{SS}$ Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C	3	3	μA
		T_A = MAX	180	48	

†T_A = MIN or MAX refers to the respective values of free-air temperature specified under recommended operating conditions.
¶This is the total of supply current, control input current, and input-to-output off-state current.

on-state resistance at specified free-air temperature, C at V_{DD}, R_L = 10 kΩ to 0 V

TEST CONDITIONS			TF4016A	TP4016A	UNIT
			MIN MAX	MIN MAX	
V_{DD} = 5 V, A at 5, 0.25, −0.25 or −5 V	V_{SS} = −5 V,	T_A = MIN	600	610	Ω
		T_A = 25°C	660	660	
		T_A = MAX	960	840	
V_{DD} = 7.5 V, A at 7.5, 0.25, −0.25, or −7.5 V	V_{SS} = −7.5 V,	T_A = MIN	360	370	Ω
		T_A = 25°C	400	400	
		T_A = MAX	600	520	
V_{DD} = 10 V, A at 10, 5.6, or 0.25 V	V_{SS} = 0 V,	T_A = MIN	600	610	Ω
		T_A = 25°C	660	660	
		T_A = MAX	960	840	
V_{DD} = 15 V, A at 15, 9.3, or 0.25 V	V_{SS} = 0 V,	T_A = MIN	360	370	Ω
		T_A = 25°C	400	400	
		T_A = MAX	600	520	

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		TF4016A		TP4016A		UNIT
					V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
					MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH}	A	Y	R_L = 10 kΩ,	C_L = 50 pF§,	85	45	125	70	ns
t_{PHL}	A	Y	C at V_{DD},	See Figure 1	85	45	125	70	
t_{PLH}	C	Y	C_L = 50 pF§,	R_L = 10 kΩ to 0 V	150	75	225	115	ns
t_{PHL}	C	Y	See Figure 2	R_L = 10 kΩ to V_{DD}	150	75	225	115	

‡t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4016A.

PARAMETER MEASUREMENT INFORMATION

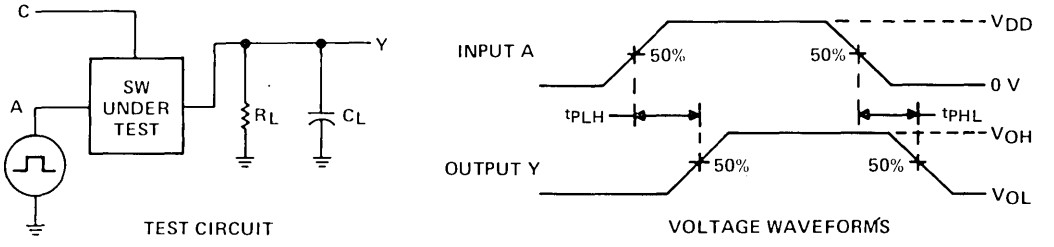


FIGURE 1–PROPAGATION DELAY TIME, SWITCH INPUT A TO OUTPUT Y

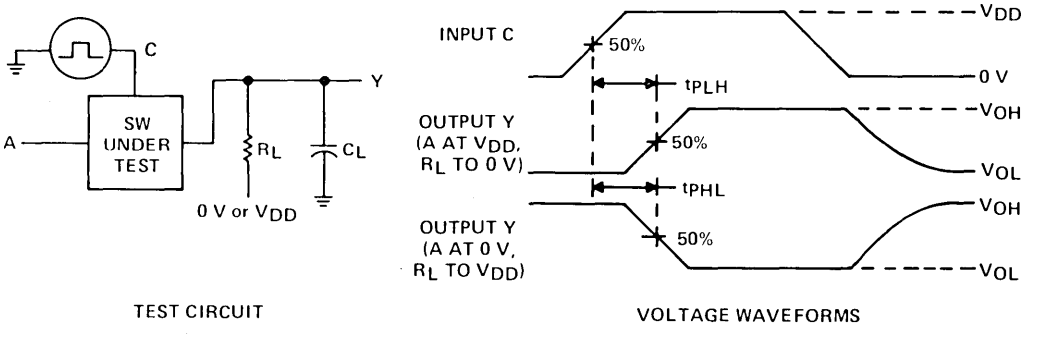


FIGURE 2–PROPAGATION DELAY TIMES, CONTROL INPUT C TO OUTPUT Y

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
B. C_L includes probe and jig capacitance.
C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 1$ MΩ.

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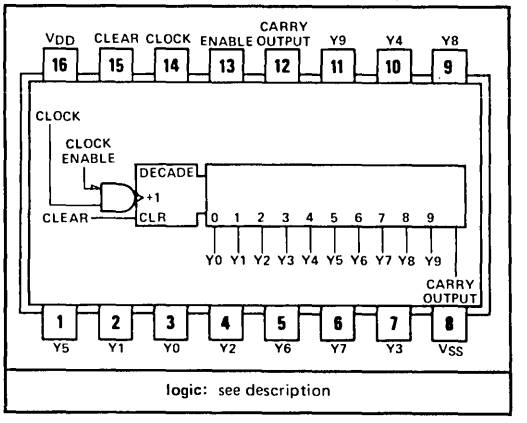
TYPES TF4017A, TP4017A
DECADE COUNTERS/DIVIDERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4017A
- Medium-Speed Operation . . . 5 MHz Typical Maximum Clock Frequency at V_{DD} = 10 V
- Fully Static Operation
- Carry Output for Cascading

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4017A is a five-stage Johnson decade counter and an output decoder that converts the Johnson binary code to a decimal number. High-speed operation and spike-free outputs are obtained by use of the Johnson decade counter configuration.

The ten decoded outputs are normally low and go high only at their respective decimal time period. A high clear signal asynchronously clears the decade counter and sets the carry output and Y0 high. With enable low, the count is advanced on a low-to-high transition at the clock input. Alternatively if the clock input is high, the count is advanced on a high-to-low transition at enable. The carry output is high while Y0, Y1, Y2, Y3, or Y4 is high, then is low while Y5, Y6, Y7, Y8, or Y9 is high.

This device can be used in frequency-division applications as well as decade-counter or decimal-decode display applications.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, Group 3, except as on following page

recommended operating conditions

		TF4017A				TP4017A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	500		170		830		250		ns
	Clear	500		170		830		250		ns
Setup time, t_{su}	Enable	500		200		700		300		ns
	Clear inactive state	750		225		1000		275		ns

TEXAS INSTRUMENTS
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electrical characteristics

PARAMETER			TEST CONDITIONS†		TF4017A				TP4017A				UNIT
					V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output-current	Y outputs	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−120		−120		−85		−85		μA
				T_A = 25°C	−100		−100		−70		−70		
				T_A = MAX	−70		−70		−55		−55		
		Carry output		T_A = MIN	−450		−450		−300		−300		μA
				T_A = 25°C	−350		−350		−240		−240		
				T_A = MAX	−250		−250		−200		−200		
I_{OL}	Low-level output current	Y outputs	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	60		120		30		85		μA
				T_A = 25°C	50		100		25		70		
				T_A = MAX	35		70		20		55		
		Carry output		T_A = MIN	185		450		95		300		μA
				T_A = 25°C	150		350		80		250		
				T_A = MAX	105		250		65		200		

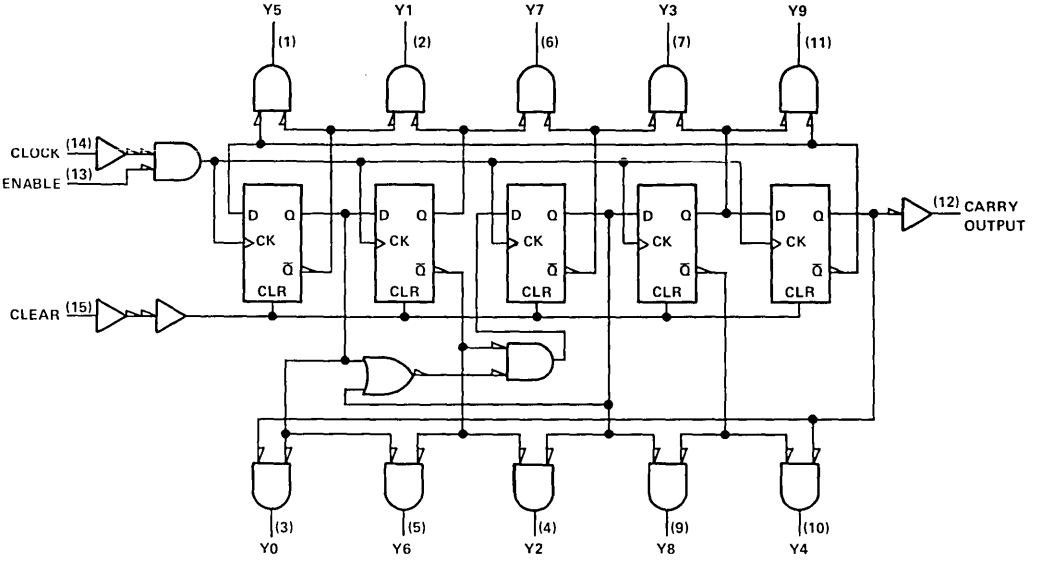
†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

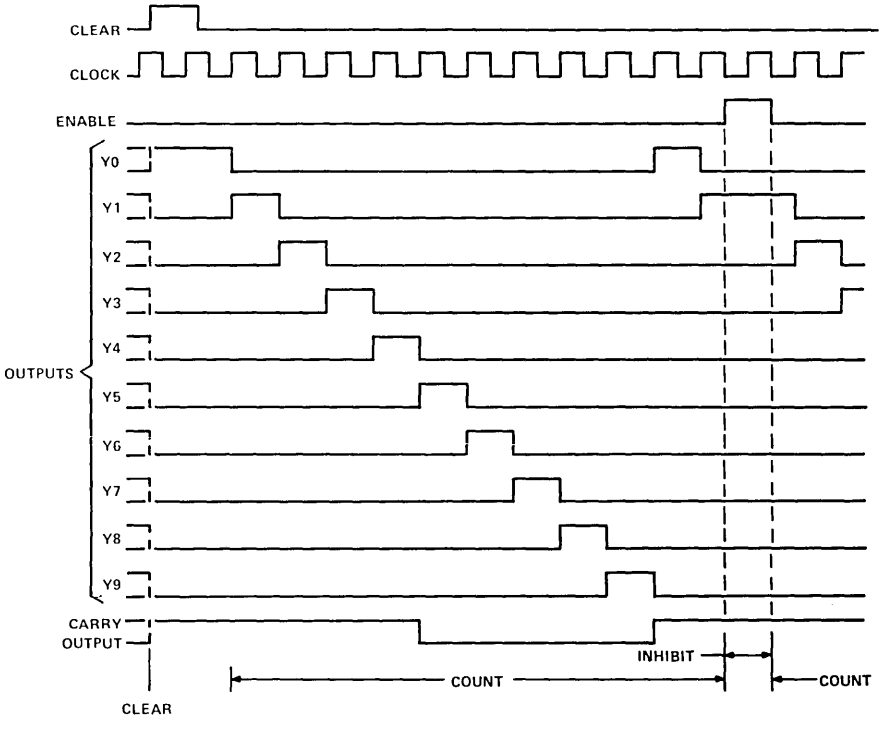
PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4017A				TP4017A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1		3		0.6		2		MHz
t_{PLH}	Clock or clear	Any Y output			2000		600		2500		750	ns
t_{PHL}					2000		600		2500		750	
t_{PLH}	Clock or clear	Carry output			1300		400		1600		500	ns
t_{PHL}					1300		400		1600		500	
t_{TLH}		Any Y output			1800		700		2400		900	ns
t_{THL}					1800		700		2400		900	
t_{TLH}		Carry output			600		300		700		400	ns
t_{THL}					600		300		700		400	

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4017A.
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



typical clear, count, and inhibit sequences



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TEXAS INSTRUMENTS
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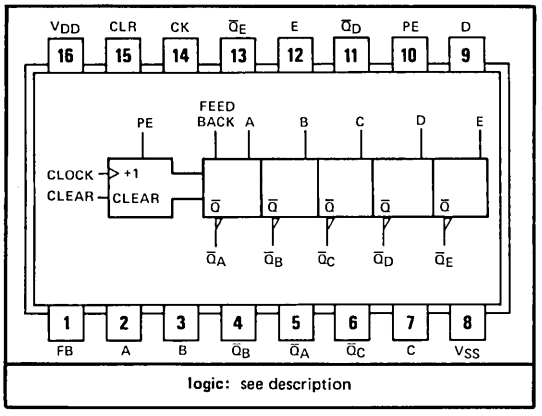
TYPES TF4018A, TP4018A
PRESETTABLE DIVIDE-BY-N COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4018A
- Maximum Clock Frequency . . . 5 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3

description

The '4018A consist of five Johnson counters, buffered $\overline{Q}$ outputs from each stage, and preset control gating. Clear, preset enable, clock, feedback, and five parallel load inputs are provided.

A high clear signal asynchronously clears the counter so that all $\overline{Q}$ outputs are high. A high preset enable signal asynchronously loads the counter and the $\overline{Q}$ outputs will take on the complements of the parallel inputs. The counter is advanced one count on the low-to-high transition of the clock input.

Various counter configurations may be implemented as follows:

Divide by	Connect These Outputs to Feedback Input	Via	Results from Each $\overline{Q}$ Output (See Timing Diagram)
10	$\overline{Q}_E$	direct	5 counts high, 5 counts low
9	$\overline{Q}_D$, $\overline{Q}_E$	AND gate	5 counts high, 4 counts low
8	$\overline{Q}_D$	direct	4 counts high, 4 counts low
7	$\overline{Q}_C$, $\overline{Q}_D$	AND gate	4 counts high, 3 counts low
6	$\overline{Q}_C$	direct	3 counts high, 3 counts low
5	$\overline{Q}_B$, $\overline{Q}_C$	AND gate	3 counts high, 2 counts low
4	$\overline{Q}_B$	direct	2 counts high, 2 counts low
3	$\overline{Q}_A$, $\overline{Q}_B$	AND gate	2 counts high, 1 count low
2	$\overline{Q}_A$	direct	1 count high, 1 count low

recommended operating conditions

		TF4018A				TP4018A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	500		170		830		250		ns
	Clear or preset enable	500		170		830		250		ns
Setup time, t_{su}	Feedback	500		200		700		300		ns
	Clear or preset enable inactive state	750		225		1000		275		

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INCORPORATED
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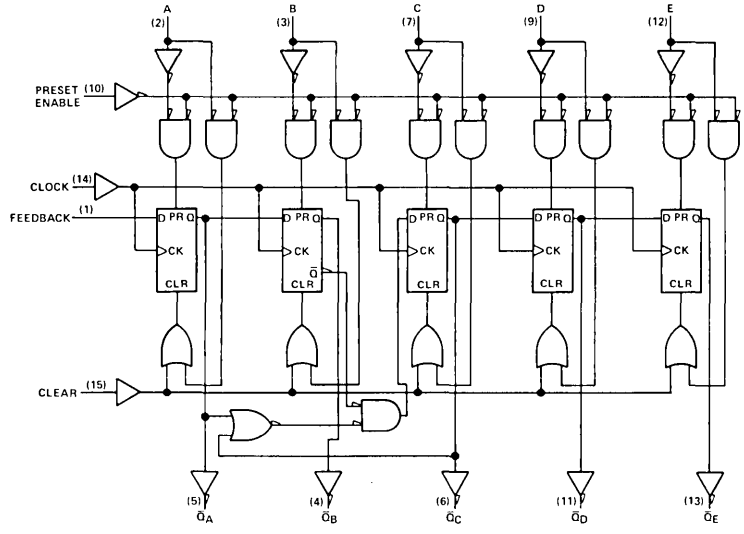
switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4018A				TP4018A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1		3		0.6		2		MHz
t_{PLH} or t_{PHL}	Clock, clear, preset enable	$\bar{Q}_A, \bar{Q}_B, \bar{Q}_C, \bar{Q}_D$			1375		475		1800		610	ns
t_{PLH} or t_{PHL}		$\bar{Q}_E$			1175		325		1500		410	ns
t_{TLH} or t_{THL}		Any			350		150		400		225	ns

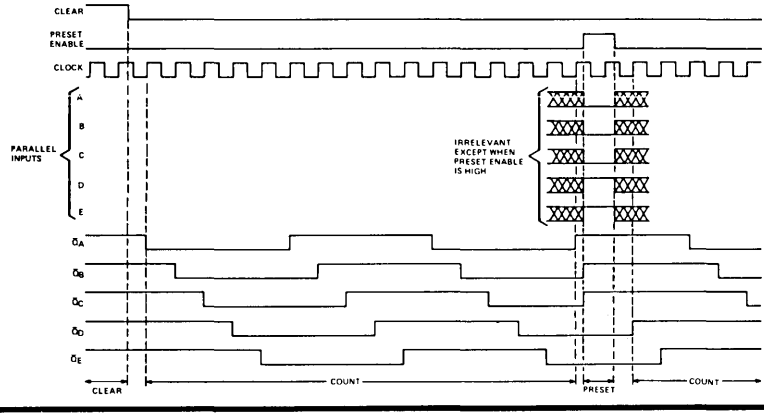
‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4018A
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



typical clear, count, and preset sequence

SHOWN IN DIVIDE-BY-TEN CONFIGURATION, $\bar{Q}_E$ TIED DIRECTLY TO FEEDBACK INPUT



TEXAS INSTRUMENTS
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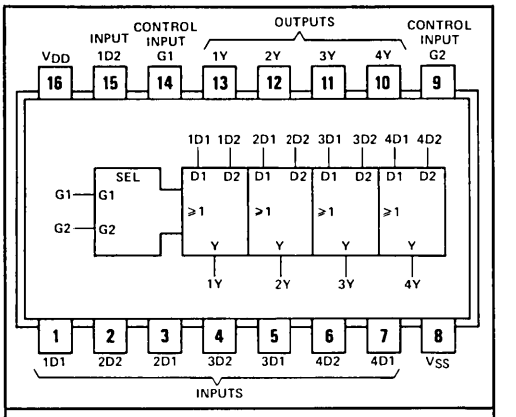
TYPES TF4019A, TP4019A
QUAD AND-OR SELECT GATES

SEPTEMBER 1975

- **Designed to be Interchangeable with RCA CD4019A**

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These devices consist of four AND-OR select gate configurations, each with two two-input AND gates driving a single two-input OR gate. Selection is determined by control inputs G1 and G2.

specifications

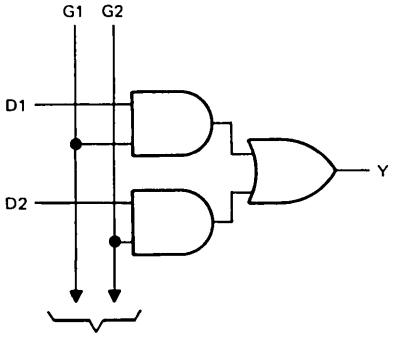
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2, except as on following page

FUNCTION TABLE
(EACH GATE)

INPUTS				OUTPUT Y
CONTROL		DATA		
G1	G2	D1	D2	
L	L	X	X	L
H	L	H	X	H
H	L	L	X	L
L	H	X	H	H
L	H	X	L	L
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = high level, L = low level, X = irrelevant

functional block diagram (each gate)



electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4019A				TP4019A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.95		−0.95		−0.6		−0.6		mA
			T_A = 25°C	−0.7		−0.7		−0.5		−0.5		
			T_A = MAX	−0.5		−0.5		−0.4		−0.4		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.6		0.9		0.37		0.8		mA
			T_A = 25°C	0.45		0.75		0.3		0.65		
			T_A = MAX	0.3		0.55		0.23		0.5		
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C		5		10		50		100	μA
			T_A = MAX		300		600		700		1400	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4019A		TP4019A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C		30		300	μA
			T_A = MAX		1800		4200	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4019A				TP4019A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		375		170		500		220	ns
t_{PHL}	Propagation delay time, high-to-low-level output			375		170		500		220	ns
t_{TLH}	Transition time, low-to-high-level output			350		130		475		165	ns
t_{THL}	Transition time, high-to-low-level output			350		130		475		165	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4019A.
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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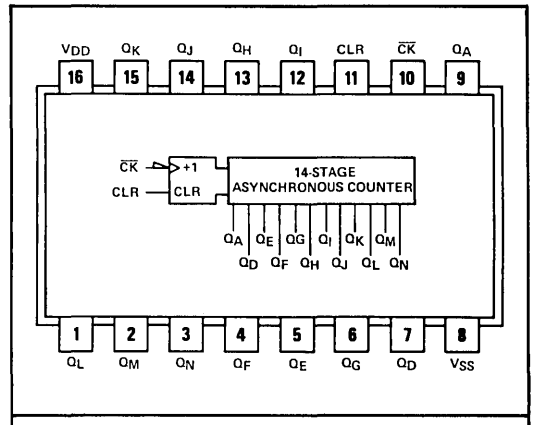
TYPES TF4020A, TP4020A
ASYNCHRONOUS 14-BIT BINARY COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4020A
- Maximum Clock Frequency . . . 7 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4020A is an asynchronous 14-stage binary counter designed with an input pulse-shaping circuit. The outputs of all stages except Q_B and Q_C are externally available. A high clear signal asynchronously clears the counter and resets all outputs low. The count is advanced on the high-to-low transition of the clock pulse. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3

recommended operating conditions

		TF4020A				TP4020A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	335		125		500		165		ns
	Clear	2500		475		3000		550		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4020A				TP4020A				UNIT
				V_{DD} = 5		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		4		1		3		MHz
t_{PLH} or t_{PHL}	Clock	Q_A			775		300		850		350	ns
t_{PLH} or t_{PHL}	Clock	Q_N			5600		2000		8400		3000	ns
t_{PHL}	Clear	Any			3200		850		3700		1000	ns
t_{TLH} or t_{THL}		Any			350		150		400		225	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4020A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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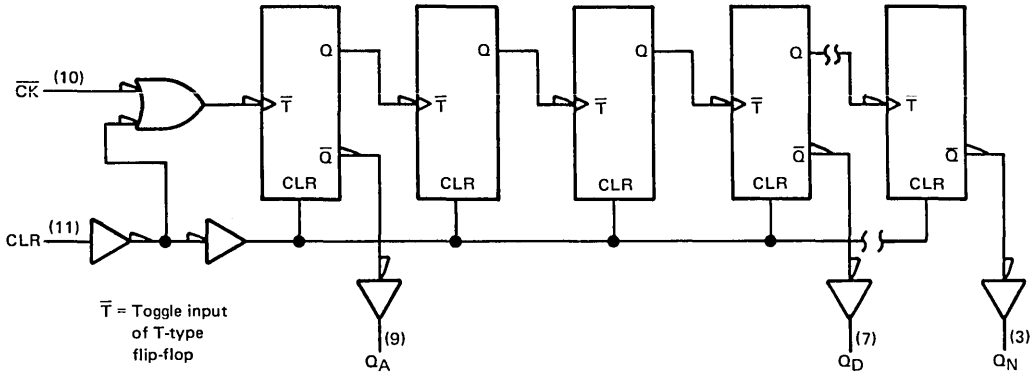
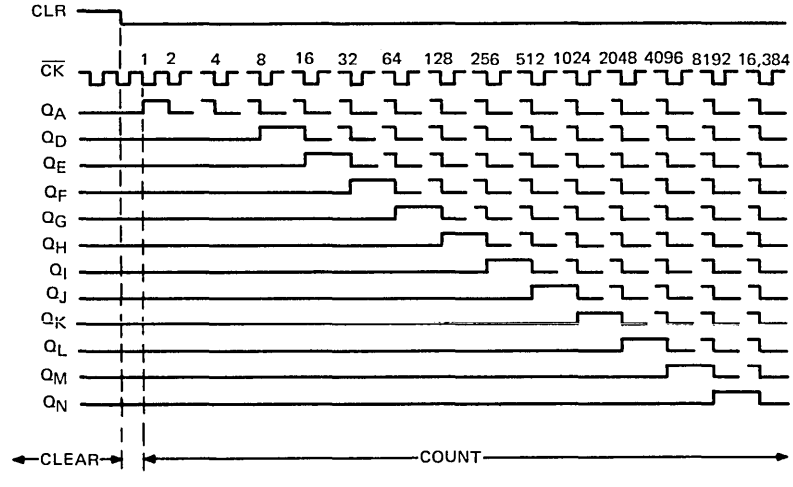
functional block diagram



typical clear and count sequence



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TYPES TF4021A, TP4021A
8-BIT STATIC SHIFT REGISTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4021A
- Asynchronous Parallel or Synchronous Serial Input, Serial Output
- Parallel Outputs from Sixth, Seventh, and Eighth Bits
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

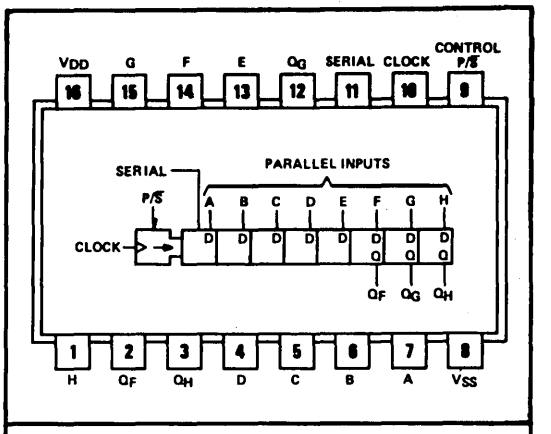
description

These 8-bit registers have a single serial input and parallel-in access to each stage. D-type master-slave flip-flops are used for each stage with parallel access to the outputs of bits F, G, and H.

When the parallel-load/serial-shift input, P/$\overline{S}$, is high, data is broadside loaded into the register from the parallel inputs independently of the clock. When the P/$\overline{S}$ input is low, data is synchronously entered at the serial input and each bit shifts one bit position in the direction Q_A toward Q_H. Serial operations occur on the low-to-high transition of the clock input.

The TF4014A and TP4014A are similar to these registers, except for having synchronous parallel inputs.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

specifications

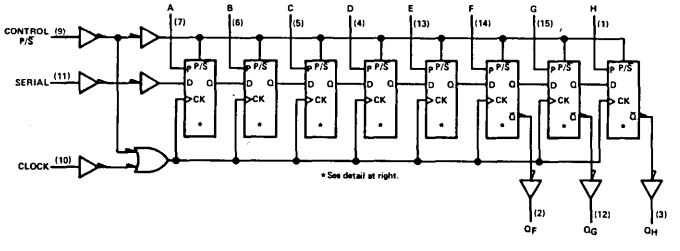
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, group 3, except as on following page

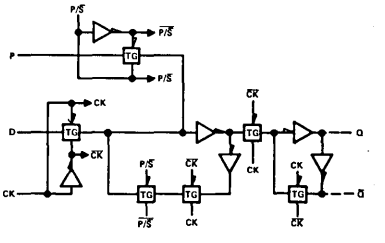
FUNCTION TABLE

INPUTS				INTERNAL OUTPUTS (2 OF 5)		OUTPUTS		
CONTROL P/$\overline{S}$	CLOCK	PARALLEL A-H	SERIAL	Q_A	Q_B	Q_F	Q_G	Q_H
H	X	a-h	X	a	b	f	g	h
L	↑	X	H	H	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	↑	X	L	L	Q_{An}	Q_{En}	Q_{Fn}	Q_{Gn}
L	L	X	X	Q_{A0}	Q_{B0}	Q_{F0}	Q_{G0}	Q_{H0}

See explanation of function tables, pages 16 and 17.

functional block diagram





DETAIL OF EACH STAGE

recommended operating conditions

		TF4021A				TP4021A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	500		175		830		200		ns
	P/$\overline{S}$ high	500		175		830		200		ns
Setup time, t_{su}		350		80		500		100		ns

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4021A				TP4021A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.25		−0.25		−0.12		−0.12		mA
			T_A = 25°C	−0.2		−0.2		−0.1		−0.1		
			T_A = MAX	−0.14		−0.14		−0.08		−0.08		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.15		0.31		0.072		0.12		mA
			T_A = 25°C	0.12		0.25		0.06		0.1		
			T_A = MAX	0.085		0.175		0.05		0.08		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4021A				TP4021A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1		3		0.6		2.5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			975		300		1300		400	ns
t_{PHL}	Propagation delay time, high-to-low-level output			975		300		1300		400	ns
t_{TLH}	Transition time, low-to-high-level output			550		225		700		300	ns
t_{THL}	Transition time, high-to-low-level output			550		225		700		300	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4014A.
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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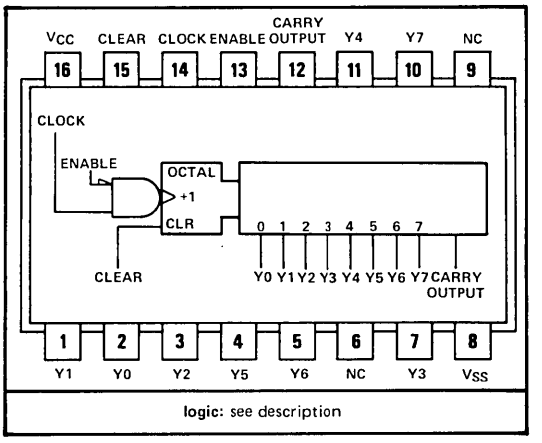
TYPES TF4022A, TP4022A
OCTAL COUNTERS/DIVIDERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4022A
- Medium-Speed Operation . . . 5 MHz Typical Maximum Clock Frequency at V_{DD} = 10 V
- Fully Static Operation
- Carry Output for Cascading

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

NC—No internal connection

description

The '4022A is a four-stage divide-by-8 Johnson counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of the Johnson octal counter configuration.

The eight decoded outputs are normally low and go high only at their respective octal time period. A high clear signal asynchronously clears the octal counter and sets the carry output and Y0 high. With enable low, the count is advanced on a low-to-high transition at the clock input. Alternatively, if the clock input is high, the count is advanced on a high-to-low transition at enable. The carry output is high while Y0, Y1, Y2, or Y3 is high, then is low while Y4, Y5, Y6, or Y7 is high.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3, except as on following page

recommended operating conditions

		TF4022A				TP4022A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	500		170		830		250		ns
	Clear	500		170		830		250		ns
Setup time, t_{su}	Enable	350		150		700		300		ns
	Clear inactive state	500		200		750		275		ns

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4022A		TP4022A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OH} High-level output-current	Y outputs	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−120	−120	−85	−85	μA
			T_A = 25°C	−100	−100	−70	−70	
			T_A = MAX	−70	−70	−55	−55	
	Carry output		T_A = MIN	−450	−450	−300	−300	μA
			T_A = 25°C	−350	−350	−240	−240	
			T_A = MAX	−250	−250	−200	−200	
I_{OL} Low-level output current	Y outputs	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	60	120	30	85	μA
			T_A = 25°C	50	100	25	70	
			T_A = MAX	35	70	20	55	
	Carry output		T_A = MIN	185	450	95	300	μA
			T_A = 25°C	150	350	80	250	
			T_A = MAX	105	250	65	200	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4022A		TP4022A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
f_{max}				1	3	0.6	2	MHz
t_{PLH}	Clock or clear	Any A output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	2000	600	2500	750	ns
t_{PHL}				2000	600	2500	750	
t_{PLH}	Clock or clear	Carry output		1300	400	1600	500	ns
t_{PHL}				1300	400	1600	500	
t_{TLH}		Any Y		1800	700	2400	900	ns
t_{THL}				1800	700	2400	900	
t_{TLH}		Carry output		600	300	700	400	ns
t_{THL}				600	300	700	400	

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4022A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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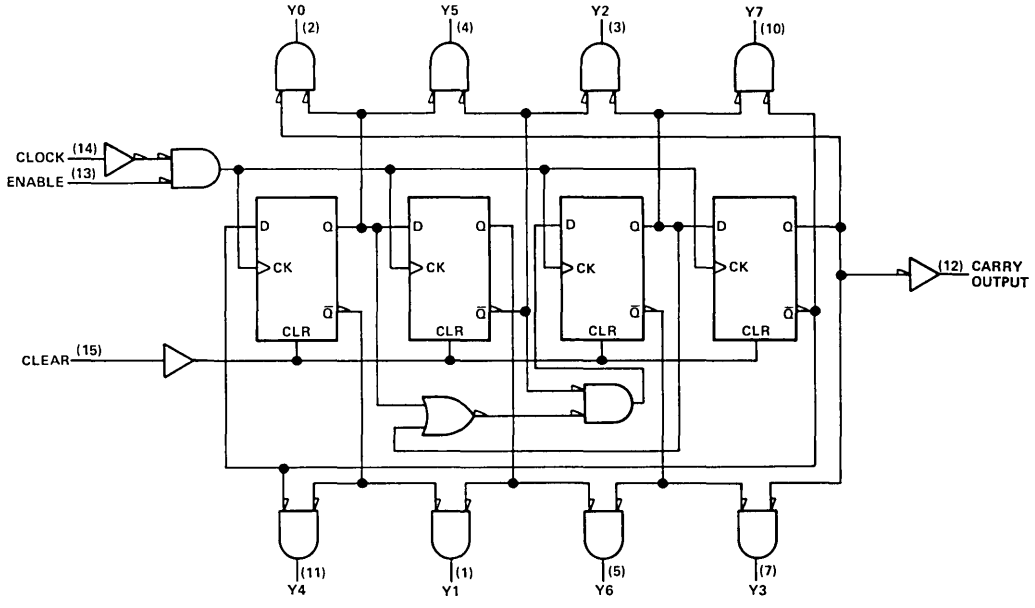
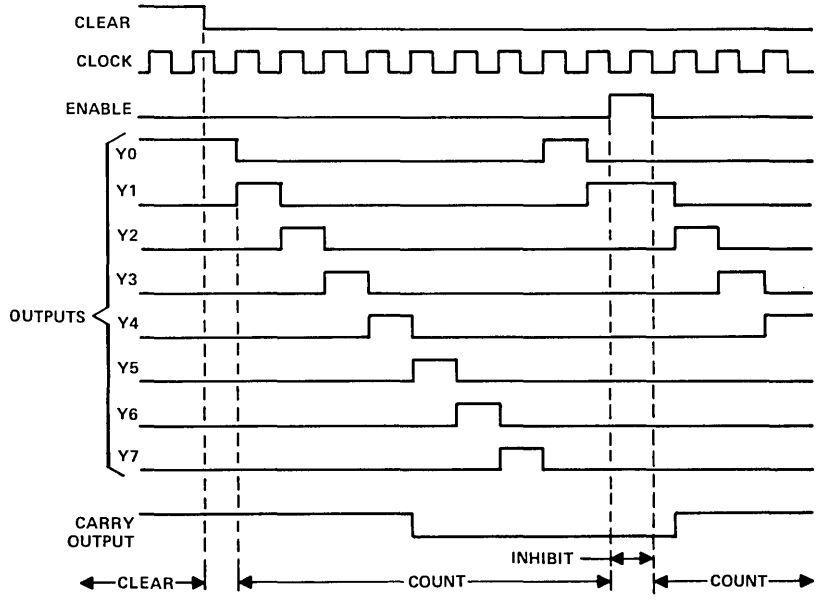
functional block diagram



typical clear, count, and inhibit sequences



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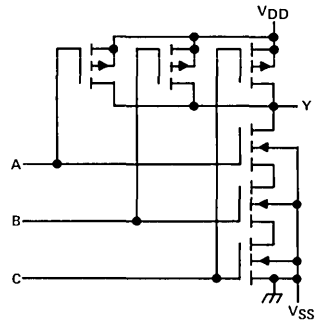
TYPES TF4023A, TP4023A
TRIPLE 3-INPUT NAND GATES

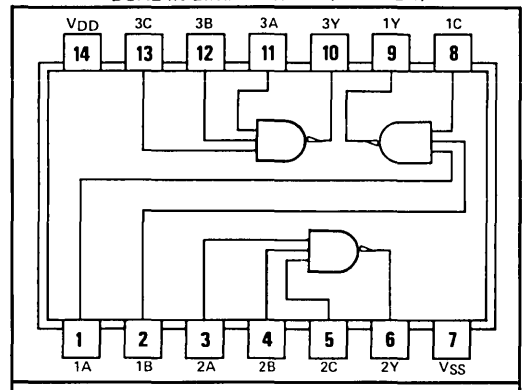
SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4023A

schematic (each gate)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABC}$

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1, except as below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4023A		TP4023A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_O = V_{OH}$ min	V_{IL} = 0, T_A = MIN	−0.65	−0.75	−0.35	−0.35	mA
			T_A = 25°C	−0.5	−0.6	−0.3	−0.3	
			T_A = MAX	−0.35	−0.4	−0.25	−0.25	
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_O = V_{OL}$ max	V_{IL} = 0, T_A = MIN	0.5	1.1	0.35	0.6	mA
			T_A = 25°C	0.4	0.9	0.3	0.5	
			T_A = MAX	0.3	0.65	0.25	0.4	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4023A		TP4023A		UNIT
			V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1	150	80	200	110	ns
t_{PHL}	Propagation delay time, high-to-low-level output		150	80	200	110	ns
t_{TLH}	Transition time, low-to-high-level output		350	175	470	250	ns
t_{THL}	Transition time, high-to-low-level output		450	200	600	275	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4023A.
NOTE 1: See load circuit and voltage waveforms on Page 170.

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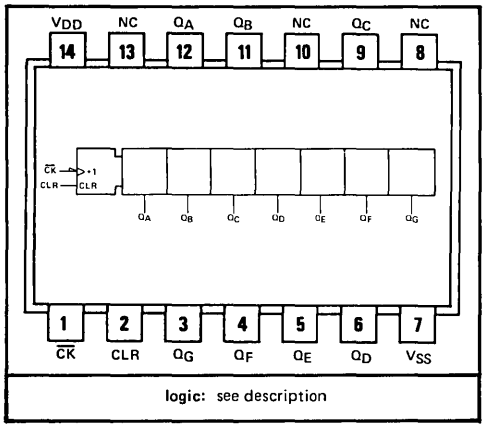
TYPES TF4024A, TP4024A
ASYNCHRONOUS 7-BIT BINARY COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4024A
- Maximum Clock Frequency . . . 7 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



NC—No internal connection

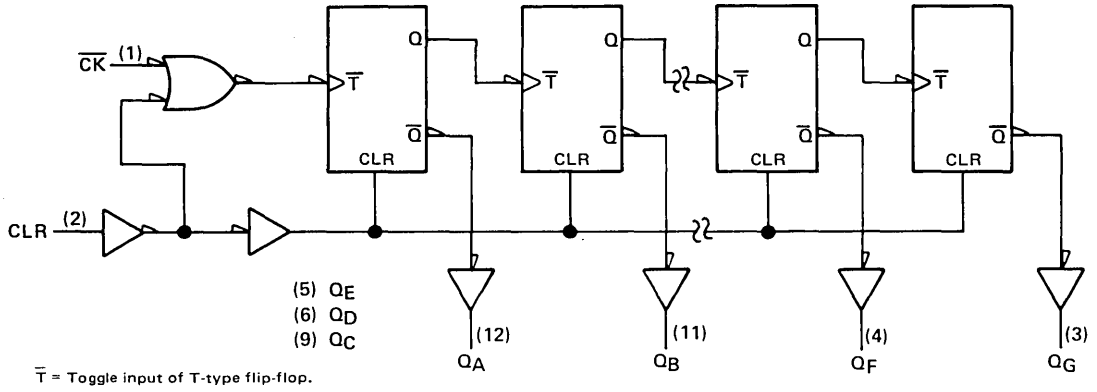
description

The '4024A is an asynchronous 7-stage binary counter designed with an input pulse-shaping circuit. The outputs of all stages are available externally. A high clear signal asynchronously clears the counter and resets all outputs low. The count is advanced on the high-to-low transition of the clock pulse. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

specifications

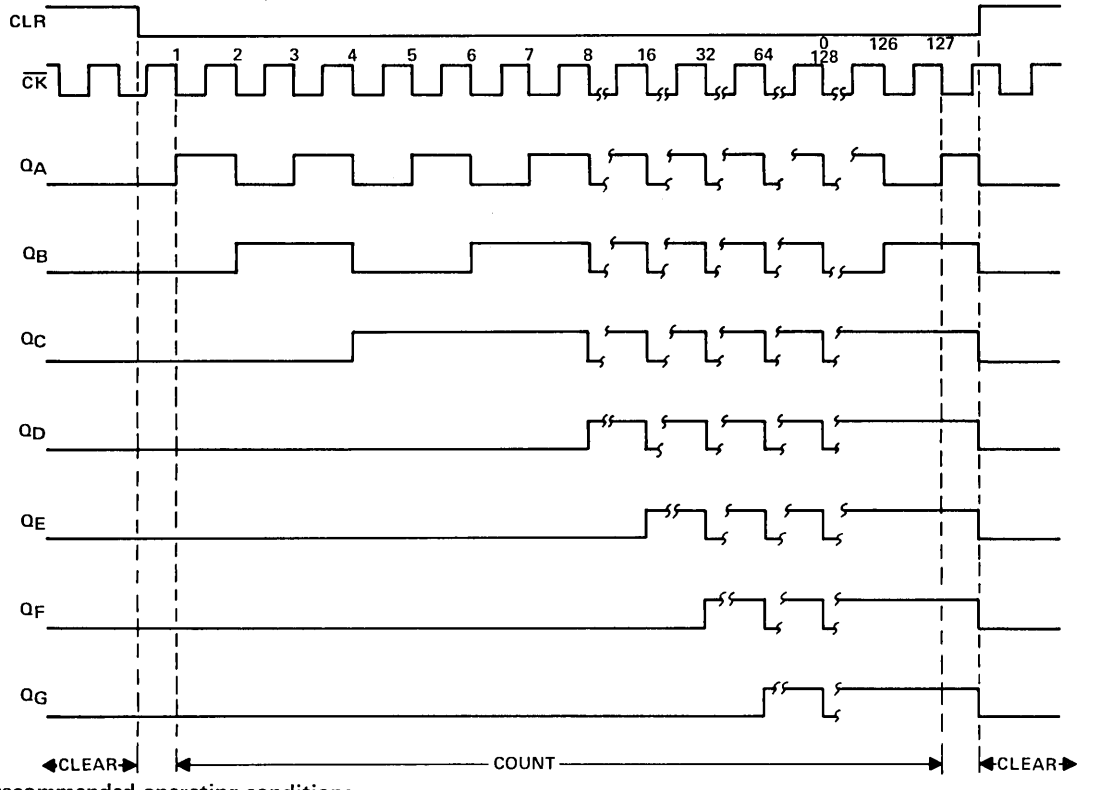
MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, Group 3

functional block diagram



T = Toggle input of T-type flip-flop.

typical clear and count sequences



recommended operating conditions

		TF4024A				TP4024A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	330		125		500		165		ns
	Clear	500		300		600		350		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4024A				TP4024A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		4		1		3		MHz
t_{PLH} or t_{PHL}	Clock	Q_A			600		225		700		300	ns
t_{PLH} or t_{PHL}	Clock	Q_G			2000		700		3000		900	ns
t_{PHL}	Clear	Any			900		425		1000		525	ns
t_{TLH} or t_{THL}		Any			350		150		400		225	ns

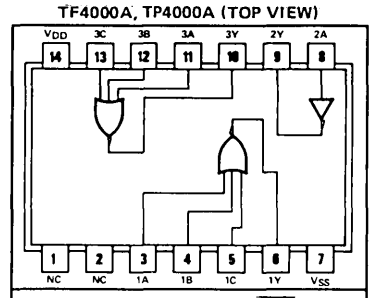
‡ f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§ With a 15-pF load, these devices switch with times similar to those of the RCA CD4024A.
NOTE 1: See load circuit and voltage waveforms on page 170.

TYPES TF4025A, TP4025A AND OTHER NOR GATES

SEPTEMBER 1975

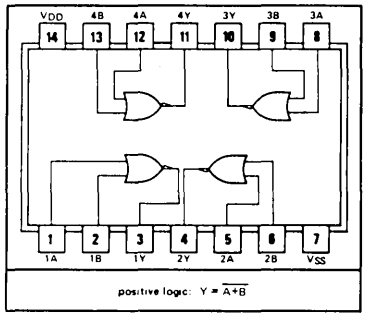
- Designed to be Interchangeable with RCA CD4000A, CD4001A, CD4002A, and CD4025A
- All Products Available in J or N Dual-in-Line Packages
  - '4000 . . . Dual 3-Input NOR Gates Plus Inverters
  - '4001 . . . Quadruple 2-Input NOR Gates
  - '4002 . . . Dual 4-Input NOR Gates
  - '4025 . . . Triple 3-Input NOR Gates

TF4000A, TP4000A (TOP VIEW)

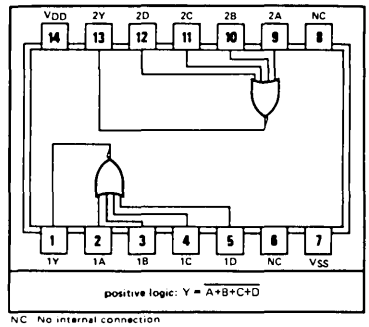


NC—No internal connection

TF4001A, TP4001P (TOP VIEW)

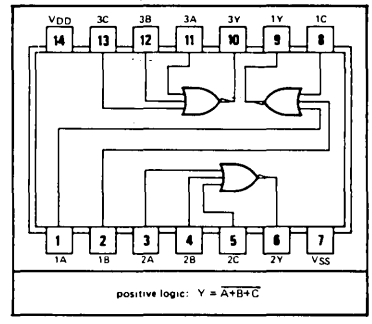


TF4002A, TP4002A (TOP VIEW)

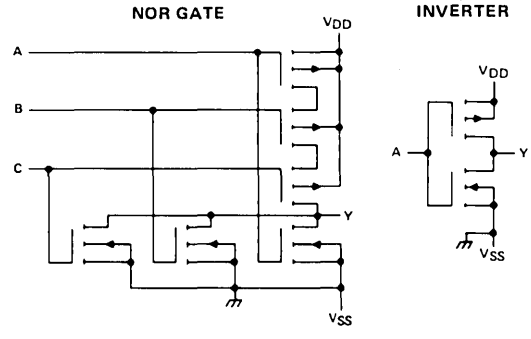


NC—No internal connection

TF4025A, TP4025A (TOP VIEW)



typical schematics



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, Group 1

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TF4000A, TF4001A TF4002A, TF4025A				TP4000A, TP4001A TP4002A, TP4025A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		150		100		200		130	ns
t_{PHL} Propagation delay time, high-to-low-level output			150		100		200		130	ns
t_{TLH} Transition time, low-to-high-level output			350		175		450		300	ns
t_{THL} Transition time, high-to-low-level output			350		175		450		300	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4000A, CD4001A, CD4002A, and CD4025A, respectively.
NOTE 1: See load circuit and voltage waveforms on page 170.

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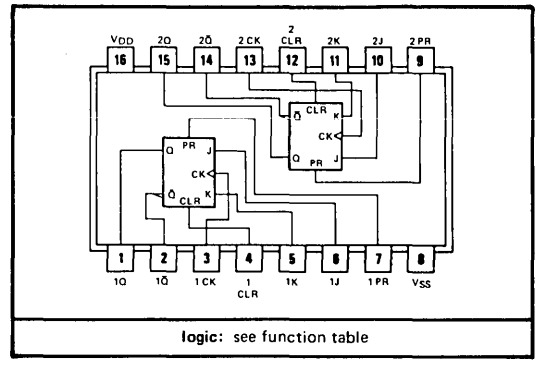
TYPES TF4027A, TP4027A
DUAL J-K FLIP-FLOPS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4027A
- Toggle Rate . . . 8 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These circuits are dual J-K-type transition-operated master-slave flip-flops with buffered outputs, independent direct overriding preset and clear inputs, and J, K, and clock inputs. While the clock is low, the data at the J and K inputs is entered into the master section, which is isolated from the slave section. On the rising transition of the clock, the J and K inputs are disabled and data previously set up in the master section is transferred to the slave section. Circuit logic for various input configurations is shown in the function table.

Presetting and clearing are independent of the clock and are accomplished by a high-level voltage at the respective input. The $\overline{Q}$ output is complementary to the Q output except for the nonstable situation that exists when both preset and clear inputs are simultaneously high.

FUNCTION TABLE
(EACH FLIP-FLOP)

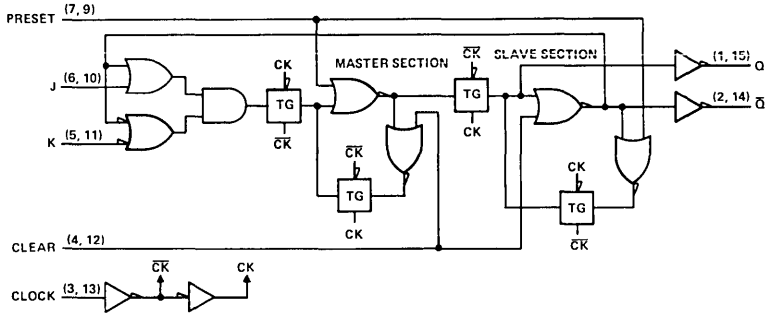
INPUTS					OUTPUTS	
PRESET	CLEAR	CK	J	K	Q	$\overline{Q}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H*	H*
L	L	↑	L	L	Q_0	$\overline{Q}_0$
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	TOGGLE	
L	L	L	X	X	Q_0	$\overline{Q}_0$

See explanation of function tables on pages 16 and 17.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (low) level.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, Group 2, except as on following page

functional block diagram



recommended operating conditions

		TF4027A				TP4027A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	330		110		500		165		ns
	Preset or clear	200		80		300		120		
Setup time, t_{su}		150		50		200		75		ns

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4027A				TP4027A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_O = V_{OH}$ min	V_{IL} = 0, T_A = MIN	−0.65		−0.8		−0.35		−0.4		mA
			T_A = 25°C	−0.5		−0.65		−0.3		−0.35		
			T_A = MAX	−0.35		−0.45		−0.25		−0.3		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_O = V_{OL}$ max	V_{IL} = 0, T_A = MIN	0.5		1.25		0.35		0.75		mA
			T_A = 25°C	0.4		1		0.3		0.6		
			T_A = MAX	0.3		0.75		0.25		0.5		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4027A				TP4027A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		4.5		1		3		MHz
t_{PLH} or t_{PHL}	Clock	Q or $\overline{Q}$			420		185		550		250	ns
t_{PLH} or t_{PHL}	Preset or Clear	Q or $\overline{Q}$			320		185		450		250	ns
t_{TLH} or t_{THL}		Any			235		130		300		175	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4027A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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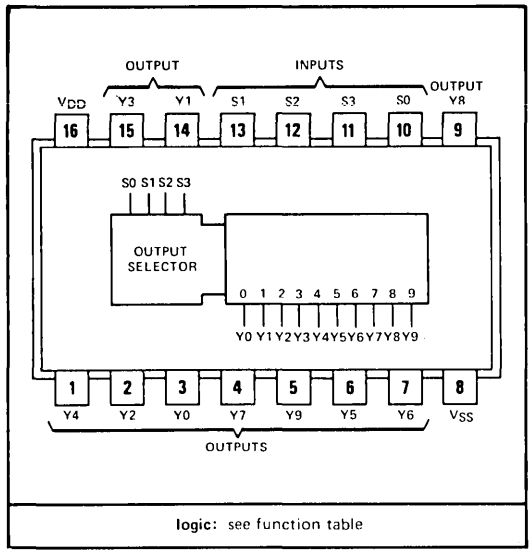
TYPES TF4028A, TP4028A
BCD-TO-DECIMAL DECODERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4028A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3

description

These circuits are BCD-to-decimal or binary-to-octal decoders with ten buffered outputs. An 8-4-2-1 BCD code applied to the four inputs provides a decimal (one of ten) decoded output. With the S3 input held at a low level, a 3-bit binary input provides a decoded octal (one of eight) code output. The selected output is high, all others are low. These devices have applications including code conversion, address decoding, memory selection control, and demultiplexing or readout decoding.

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	S3	S2	S1	S0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
0	L	L	L	L	H	L	L	L	L	L	L	L	L	L
1	L	L	L	H	L	H	L	L	L	L	L	L	L	L
2	L	L	H	L	L	L	H	L	L	L	L	L	L	L
3	L	L	H	H	L	L	L	H	L	L	L	L	L	L
4	L	H	L	L	L	L	L	L	H	L	L	L	L	L
5	L	H	L	H	L	L	L	L	L	H	L	L	L	L
6	L	H	H	L	L	L	L	L	L	L	H	L	L	L
7	L	H	H	H	L	L	L	L	L	L	L	H	L	L
8	H	L	L	L	L	L	L	L	L	L	L	L	H	L
9	H	L	L	H	L	L	L	L	L	L	L	L	L	H
INVALID	H	L	H	L	L	L	L	L	L	L	L	L	L	L
	H	L	H	H	L	L	L	L	L	L	L	L	L	L
	H	H	L	L	L	L	L	L	L	L	L	L	L	L
	H	H	L	H	L	L	L	L	L	L	L	L	L	L
	H	H	H	L	L	L	L	L	L	L	L	L	L	L
	H	H	H	H	L	L	L	L	L	L	L	L	L	L

H high level, L low level

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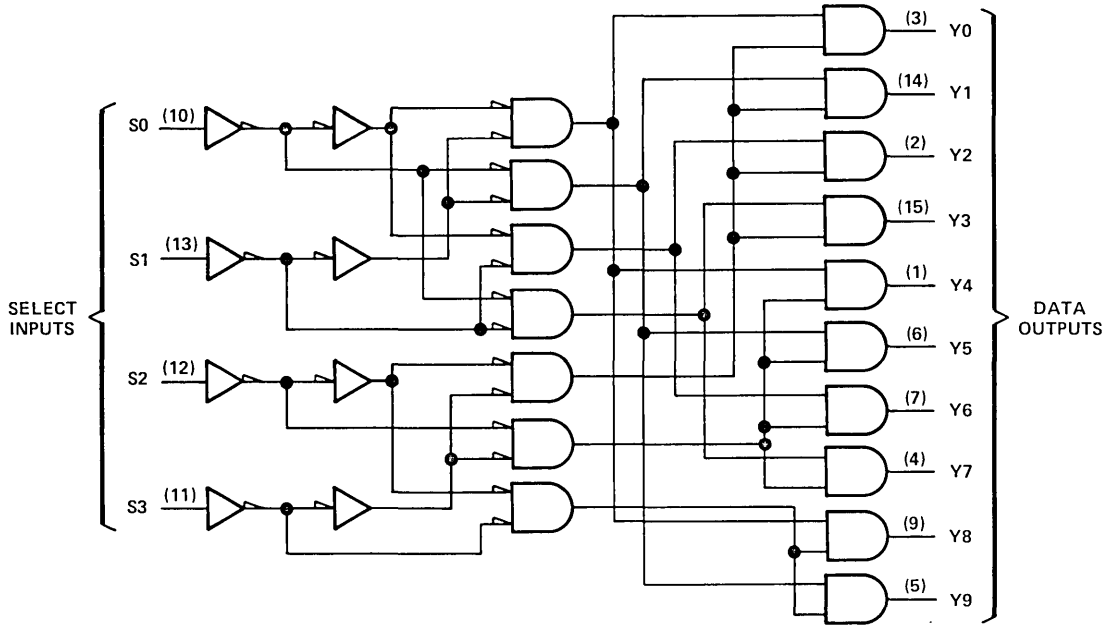
functional block diagram



switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4028A				TP4028A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		630		250		900		400	ns
t_{PHL}	Propagation delay time, high-to-low-level output			630		250		900		400	ns
t_{TLH}	Transition time, low-to-high-level output			300		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			300		150		400		220	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4028A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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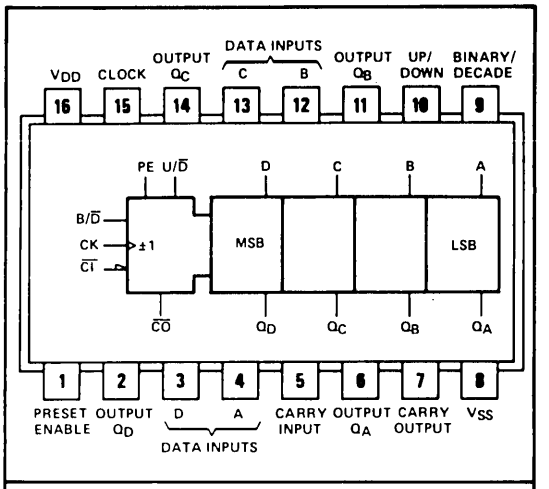
TYPES TF4029A, TP4029A
PRESETTABLE UP/DOWN
BINARY/DECADE COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4029A
- Medium Speed Operation . . . 5 MHz Typical at V_{DD} = 10 V
- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4029A counter consists of a four-stage binary or BCD-decade up/down counter with provision for look-ahead carry in both counting modes. The inputs consist of a single clock, carry input (clock enable), binary/decade, up/down, preset enable, and four individual parallel data inputs. Four separate buffered data outputs and a carry output are provided.

A high at the preset-enable input allows information at the parallel inputs to preset the counter to any count independently of the clock. A low at each parallel input, when the preset-enable input is high, resets the counter to its zero count. The counter is advanced one count at the low-to-high transition of the clock when the carry input and preset-enable input are low. Advancement is inhibited when the carry input or preset-enable input is high. The carry output is normally high and goes low when the counter reaches its maximum count in the up mode or its minimum count in the down mode, provided the carry input is low. The carry input terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the binary/decade input is high; the counter counts in the decade mode when the binary/decade input is low. The counter counts up when the up/down input is high, and down when the up/down input is low.

Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Figure 1. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple clocking permits longer clock input rise and fall times.

SUMMARY OF CONTROL INPUT FUNCTIONS
(COMPLETE COUNTER)

CONTROL INPUT	LOGIC LEVEL	FUNCTION
Binary/Decade ($B/\overline{D}$)	H	Binary count
	L	Decade count
Up/Down ($U/\overline{D}$)	H	Count up
	L	Count down
Preset enable (PE)	H	Parallel load
	L	Enable counting
Carry input ($\overline{CI}$)	H	Inhibit counting
	L	Enable counting

specification

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, group 3, except as on following page

TEXAS INSTRUMENTS
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recommended operating conditions

		TF4029A				TP4029A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	340		170		500		250		ns
	Preset enable	330		160		660		320		
Setup time, t_{su}	Binary/Decade	650		230		1300		460		ns
	Up/Down	650		230		1300		460		
	Carry input	650		230		1300		460		
	Preset enable inactive state	650		230		1300		460		

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4029A				TP4029A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH} High-level output-current	Q outputs	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−300		−300		−140		−140		μA
			T_A = 25°C	−200		−200		−100		−100		
			T_A = MAX	−140		−140		−80		−80		
	Carry output		T_A = MIN	−150		−150		−70		−70		μA
			T_A = 25°C	−100		−100		−50		−50		
			T_A = MAX	−70		−70		−40		−40		
I_{OL} Low-level output current	Q outputs	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	500		740		240		360		μA
			T_A = 25°C	400		600		200		300		
			T_A = MAX	280		420		160		240		
	Carry output		T_A = MIN	100		400		50		190		μA
			T_A = 25°C	80		320		40		160		
			T_A = MAX	60		220		30		130		

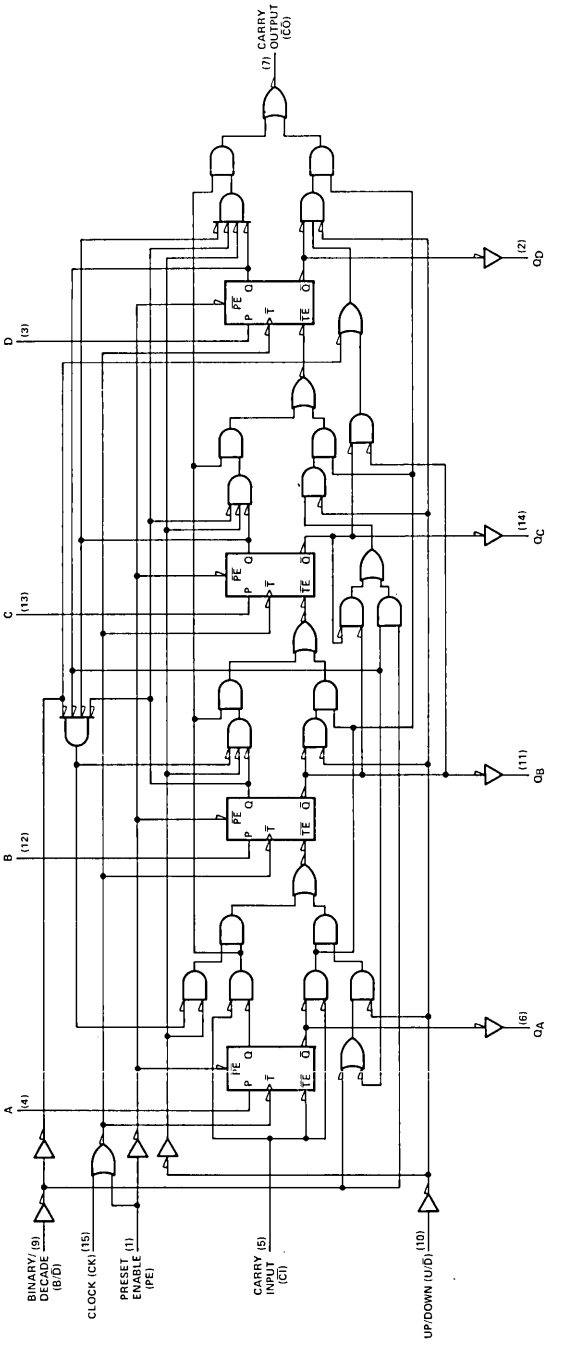
†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4029A				TP4029A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See load circuit and voltage waveforms on page 170.	1.5		3		1		2		MHz
t_{PLH} or t_{PHL}	Clock	Any Q output			900		350		1800		700	ns
t_{PLH} or t_{PHL}	Clock	Carry output			1300		550		2600		1100	ns
t_{PLH} or t_{PHL}	Preset enable	Any Q output			900		350		1800		700	ns
t_{PLH} or t_{PHL}	Preset enable	Carry output			1300		550		2600		1100	ns
t_{PLH} or t_{PHL}	Carry input	Carry output			800		350		1600		700	ns
t_{TLH} or t_{THL}		Any Q output			450		225		900		450	ns
t_{TLH} or t_{THL}		Carry output			850		450		1700		900	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4029A.

functional block diagram



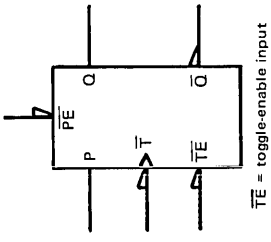
EACH FLIP-FLOP

FUNCTION TABLE
(NOT INCLUDING GATING EXTERNAL TO THE FLIP-FLOP)

INPUTS				OUTPUTS	
$\overline{PE}$	$\overline{TE}$	$\overline{T}$	P	Q	$\overline{Q}$
L	X	L	H	H	L
L	X	L	L	L	H
H	H	↓	X	Q_n	$\overline{Q}_n$
H	L	↓	X	$\overline{Q}_n$	Q_n
X	X	H	X	Q_0	$\overline{Q}_0$

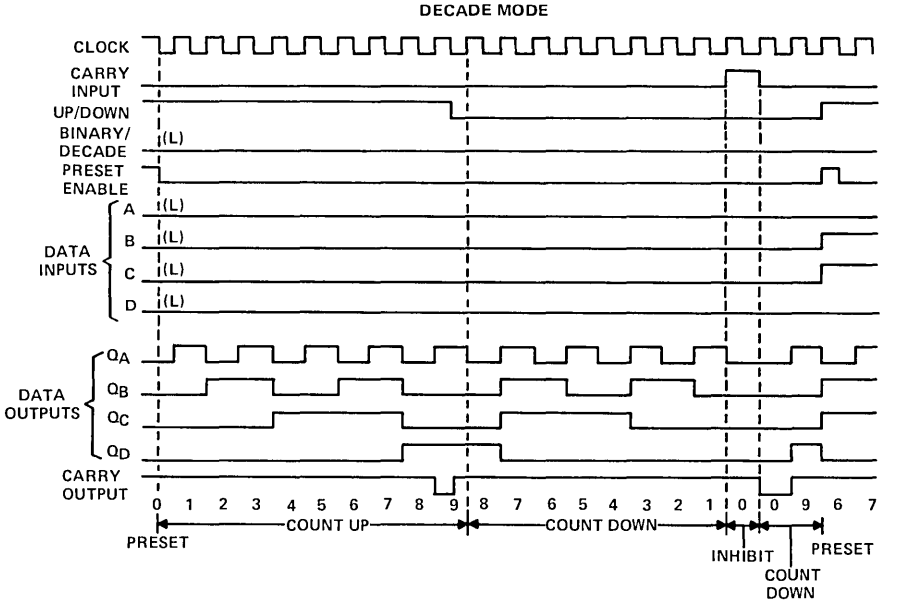
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
Q_n = the level of Q before the most-recent ↓ transition of $\overline{T}$
Q_0 = the level of Q before the indicated steady-state conditions were established

SYMBOL

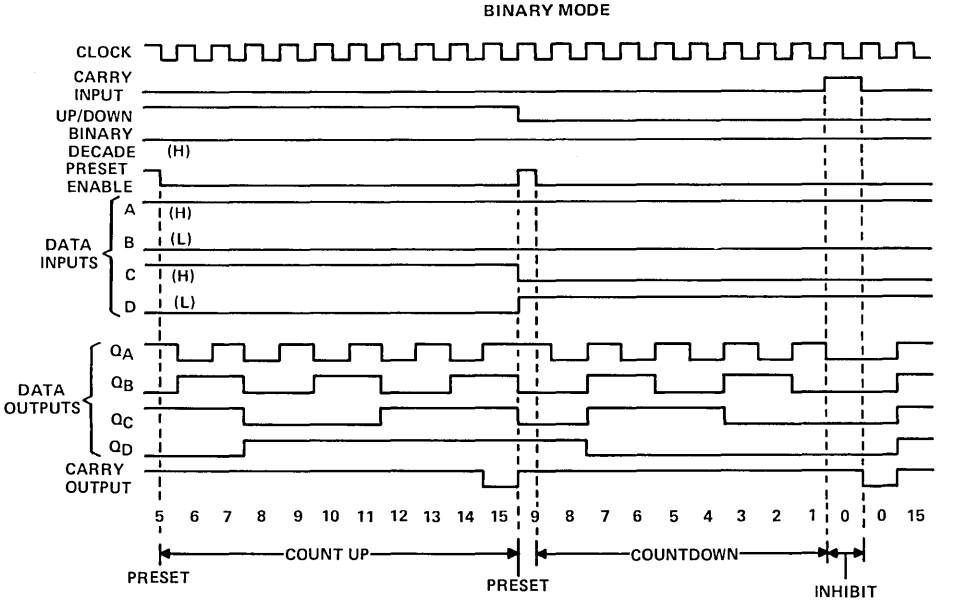


$\overline{TE}$ = toggle-enable input
P = parallel data input
$\overline{T}$ = toggle input

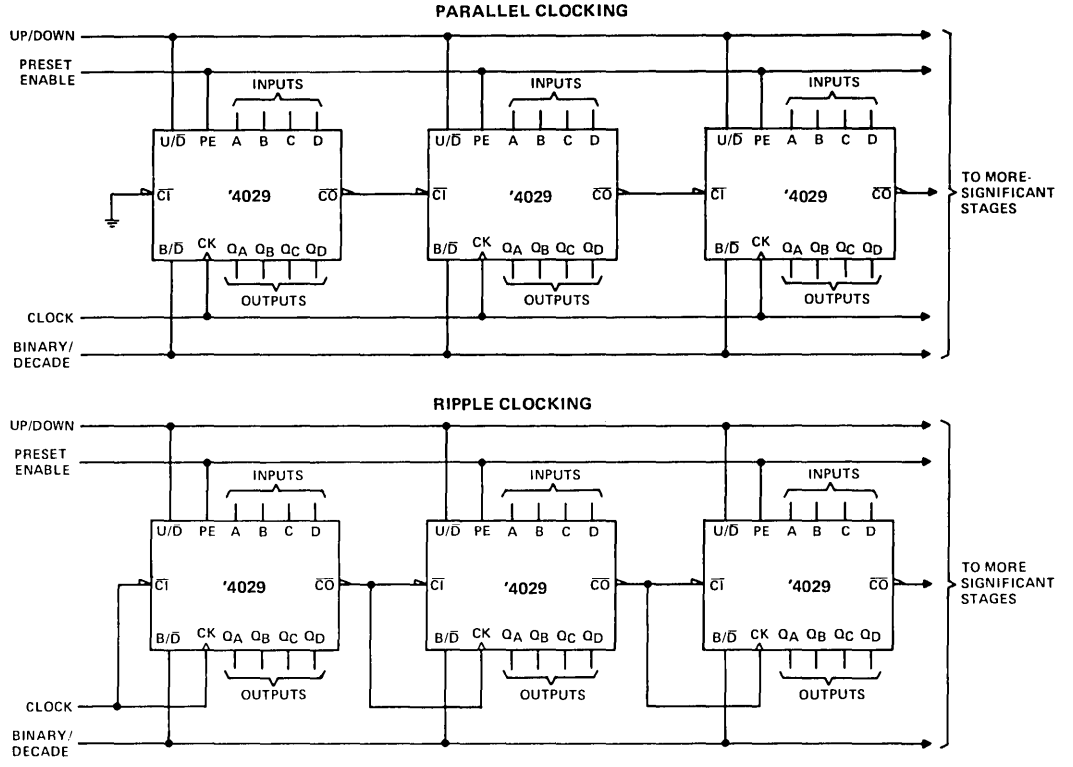
typical count up, count down, inhibit, and preset sequences



typical count up, preset, count down, and inhibit sequences



TYPICAL APPLICATION DATA



NOTE A: The up/down control can be changed at any count. The only restriction is that in the ripple-clocked application, the clock input (including $\overline{CI}$) of the first counting stage must be high when the up/down control is changed.

FIGURE 1–CASCADING COUNTER PACKAGES

The '4029 clock and up/down inputs are used directly in most applications. In applications where clock-up and clock-down inputs are provided, conversion to the '4029 clock and up/down inputs can easily be realized by use of the circuit shown below. The '4029 changes count on the low-to-high transitions of the clock-up or clock-down inputs. For the gate configuration shown below, when counting up the clock-down input must be maintained high and conversely, when counting down the clock-up input must be maintained high.

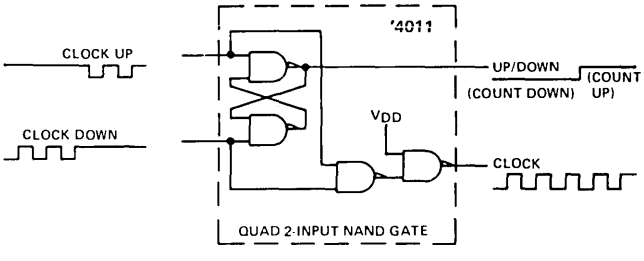


FIGURE 2–CONVERSION OF CLOCK-UP AND CLOCK-DOWN INPUT SIGNALS TO CLOCK AND UP/DOWN INPUT SIGNALS

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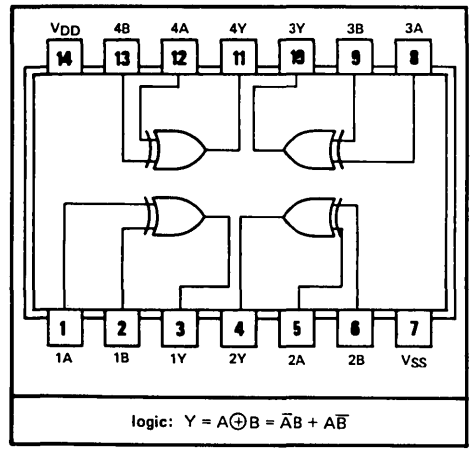
TYPES TF4030A, TP4030A
QUAD EXCLUSIVE-OR GATES

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4030A and Motorola MC14507
- Even- and Odd-Parity Generators and Checkers
- Logical Comparators
- Adders and Subtractors
- True/Complement Gating

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

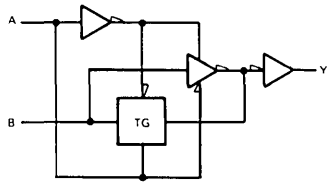


FUNCTION TABLE

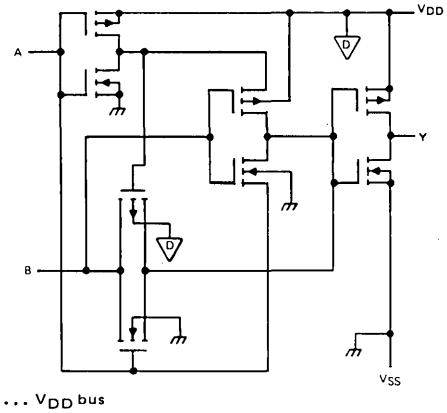
INPUTS A	INPUTS B	OUTPUT Y
L	L	L
H	L	H
L	H	H
H	H	L

H = high level, L = low level

functional block diagram (each gate)



schematic (each gate)



D .... V_{DD} bus

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2, and on following page

electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4030A				TP4030A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−0.95		−0.95		−0.45		−0.45		mA
			T_A = 25°C	−0.65		−0.65		−0.32		−0.32		
			T_A = MAX	−0.45		−0.45		−0.25		−0.25		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	0.75		1.5		0.35		0.7		mA
			T_A = 25°C	0.6		1.2		0.3		0.6		
			T_A = MAX	0.45		0.9		0.25		0.5		
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		0.5		1		5		10	μA
			T_A = MAX		30		60		70		140	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4030A		TP4030A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		3		30	μA
			T_A = MAX		180		420	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4030A				TP4030A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		350		175		475		250	ns
t_{PHL}	Propagation delay time, high-to-low-level output			350		175		475		250	ns
t_{TLH}	Transition time, low-to-high-level output			300		150		450		225	ns
t_{THL}	Transition time, high-to-low-level output			300		150		450		225	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4030A and Motorola MC14507.
NOTE 1: See load circuit and voltage waveforms on page 170.

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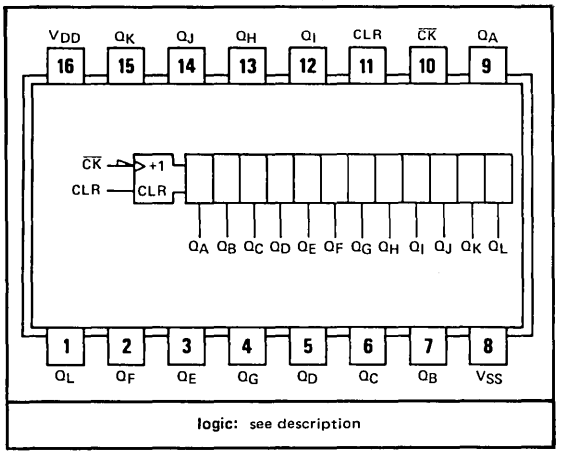
TYPES TF4040A, TP4040A
ASYNCHRONOUS 12-BIT BINARY COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4040A
- Maximum Clock Frequency . . . 7 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4040 is an asynchronous 12-stage binary counter designed with an input pulse-shaping circuit. The outputs of all stages are available externally. A high clear signal asynchronously clears the counter and resets all outputs low. The count is advanced on the high-to-low transition of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3

recommended operating conditions

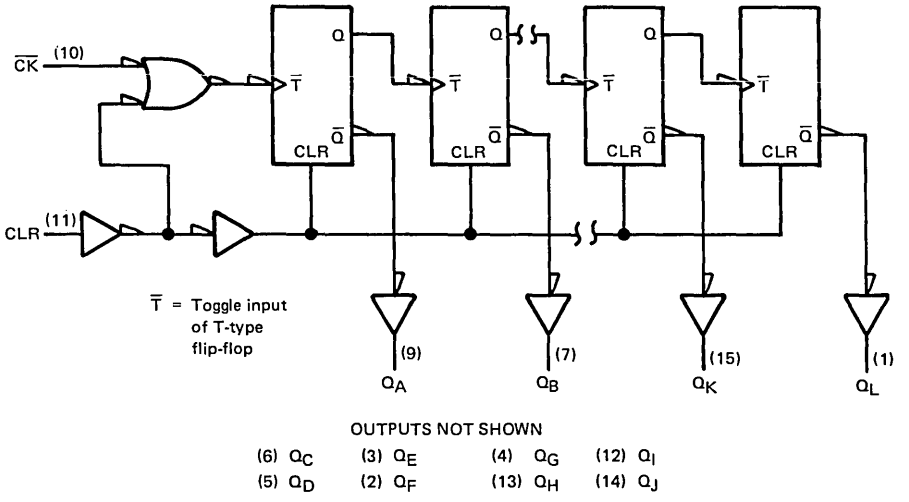
		TF4040A				TP4040A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	335		110		500		125		ns
	Clear	1000		500		1250		600		ns

switching characteristics at 25°C free-air temperature

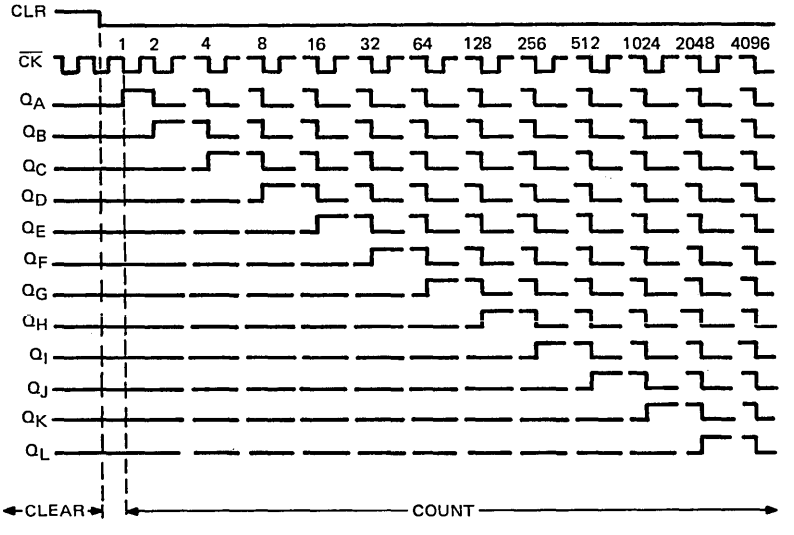
PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4040A				TP4040A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		4		1		3		MHz
t_{PLH} or t_{PHL}	Clock	Q_A			775		300		850		350	ns
t_{PLH} or t_{PHL}	Clock	Q_L			5000		1800		7500		2700	ns
t_{PHL}	Clear	Any			1200		475		1800		725	ns
t_{TLH} or t_{THL}		Any			350		150		400		225	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the RCA CD4040A.
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



typical clear and count sequence



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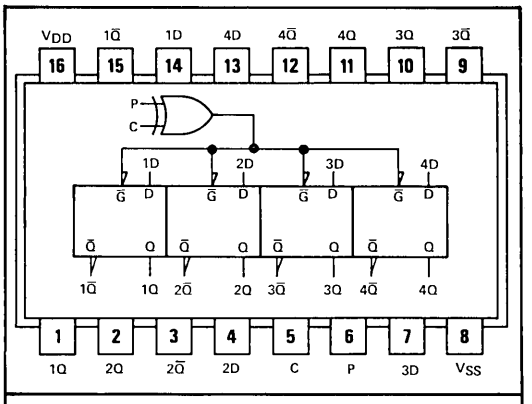
TYPES TF4042A, TP4042A
QUAD D-TYPE LATCHES

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4042A
- Control and Polarity Inputs
- Complementary Outputs

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

The '4042A is a quadruple D-type latch with common control and polarity inputs, C and P. Complementary buffered outputs are available from each latch.

When P is high, C determines the state of all the latches. If C is high, the latches pass data from their D inputs to their Q outputs and the data complement to their $\overline{Q}$ outputs. If C is low, the data is latched.

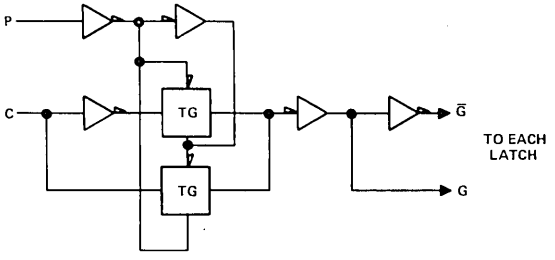
When P is low, C still determines the state of all the latches, but now data is passed when C is low and is latched when C is high.

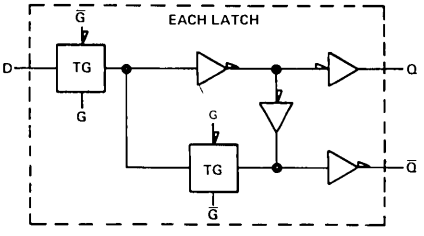
FUNCTION TABLE

P	C	FUNCTION
H	H	Pass data
H	L	Latch data
L	H	Latch data
L	L	Pass data

H = high level, L = low level

functional block diagram





specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3, except as on following page

recommended operating conditions

	TF4042A				TP4042A				UNIT
	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Width of control pulse (high or low), $t_{w(control)}$	250		75		350		175		ns
Data setup time before latching, $t_{su(data)}$	100		50		125		60		ns

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electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4042A			TP4042A			UNIT
				V_{DD} = 5 V		V_{DD} = 10 V	V_{DD} = 5 V		V_{DD} = 10 V	
				MIN	MAX	MIN MAX	MIN	MAX	MIN MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN, or 25°C		1	2		10	20	μA
			T_A = MAX		60	120		140	280	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4042A		TP4042A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		6		60	μA
			T_A = MAX		360		840	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4042A				TP4042A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		475		200		600		300	ns
t_{PHL}	Propagation delay time, high-to-low-level output			475		200		600		300	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4042A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4043A, TF4044A, TP4043A, TP4044A
QUAD S-R AND $\overline{S}$-$\overline{R}$ LATCHES
WITH 3-STATE OUTPUTS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4043A and CD4044A
- 3-State Outputs with Common Enable

description

The '4043A and '4044A are quadruple S-R and $\overline{S}$-$\overline{R}$ latches, respectively, with three-state outputs. Each latch has separate active-high ('4043A) or active-low ('4044A) set and reset inputs. The three-state outputs are controlled by a common output control. When high, this control permits each output to assume the state of the cross-coupled NOR-gate or NAND-gate latch. When the output control is low, all the outputs are in a high-impedance state.

FUNCTION TABLES
(EACH LATCH)
TF4043A, TP4043B

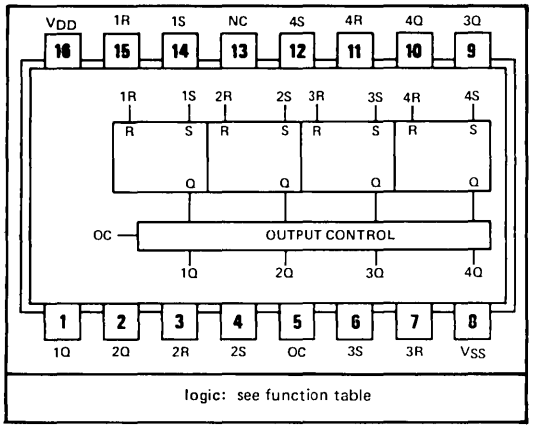
OUTPUT CONTROL	INPUTS S	INPUTS R	OUTPUT Q
L	X	X	Hi-Z
H	L	L	No change
H	H	L	H
H	L	H	L
H	H	H	H*

TF4044A, TP4044A

OUTPUT CONTROL	INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
L	X	X	Hi-Z
H	H	H	No change
H	L	H	H
H	H	L	L
H	L	L	L*

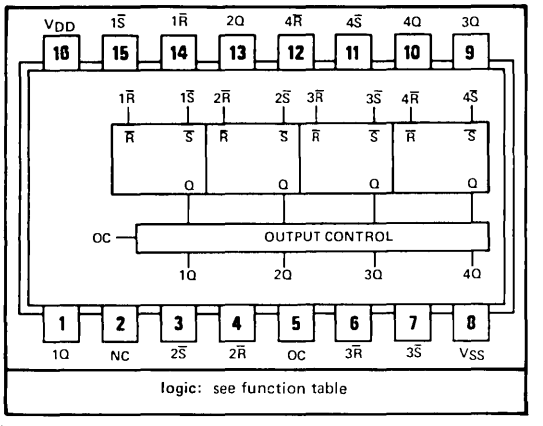
*This output level is psuedo stable; that is, it may not persist when the S and R inputs return to their inactive (low) level or the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level. See explanation of function tables, pages 16 and 17.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4043A, TP4043A



NC—No internal connection

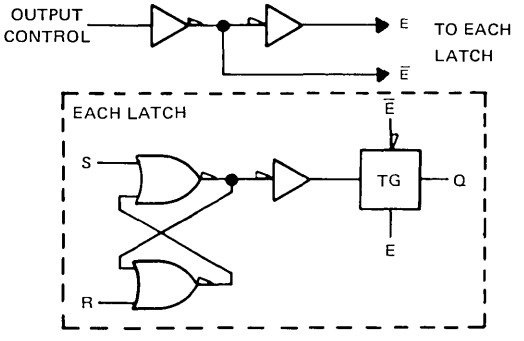
TF4044A, TP4044A



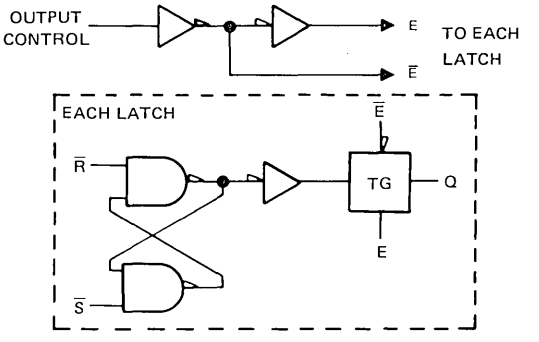
NC—No internal connection

functional block diagrams

TF4043A, TP4043A



TF4044A, TP4044A



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3, except as below

recommended operating conditions

	TF4043A, TF4044A				TP4043A, TP4044A				UNIT
	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, set or reset, t_w	200		100		225		110		ns

electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4043A, TF4044A				TP4043A, TP4044A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OZH}	Off-state output current, high-level voltage applied	OC at V_{SS}, $V_O = V_{DD}$	T_A = MIN or 25°C		0.05		0.1		0.5		1	μA
			T_A = MAX		3		6		7		14	
I_{OZL}	Off-state output current, low-level voltage applied	OC at V_{SS}, V_O = 0 V	T_A = MIN or 25°C		−0.05		−0.1		−0.5		−1	μA
			T_A = MAX		−3		−6		−7		−14	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN, or 25°C		1		2		10		20	μA
			T_A = MAX		60		120		140		280	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS		TF4043A, TF4044A		TP4043A, TP4044A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	$V_I = V_{DD}$ or 0, No load	T_A = MIN or 25°C		6		60	μA
			T_A = MAX		360		840	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4043A, TF4044A				TP4043A, TP4044A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		525		250		600		310	ns
t_{PHL}	Propagation delay time, high-to-low-level output			525		250		600		310	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4043A and CD4044A.
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

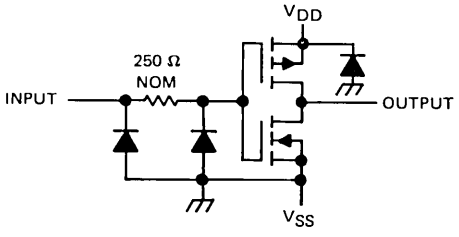
TYPES TF4049A, TF4050A, TP4049A, TP4050A
HEX INVERTING AND NONINVERTING BUFFERS

SEPTEMBER 1975

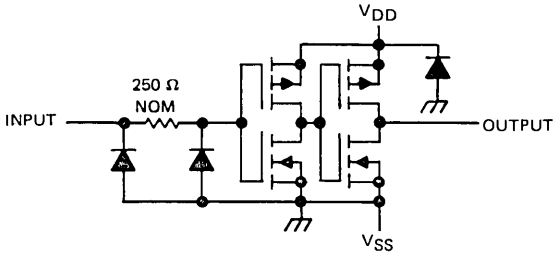
- Designed to be Interchangeable with RCA CD4049A and RCA CD4050A
- High Current Sinking Capability . . . 8 mA Minimum at V_{OL} = 0.5 V, V_{DD} = 10 V, T_A = 25°C

schematic (each buffer)

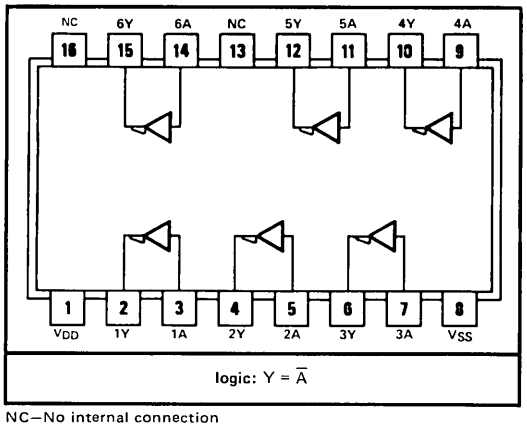
'4049A



'4050A

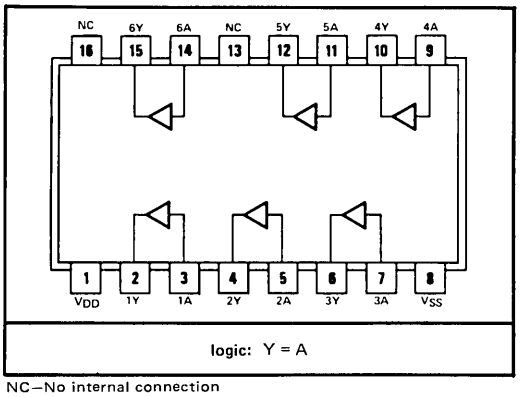


J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4049A, TP4049A



NC—No internal connection

TF4050A, TP4050A



NC—No internal connection

description

The '4049A and '4050A hex CMOS inverting and noninverting buffers may be used as current sinks or source drivers, hex CMOS drivers, or high-to-low-logic-level (e.g., CMOS to DTL or TTL) converters. Logic-level conversion is accomplished using only one supply voltage (V_{DD}). The high-level input signal (V_{IH}) can exceed the V_{DD} supply voltage when this device is used for logic-level conversions. Table 1 shows the range of voltage levels that can be utilized in these applications. Conversions to logic levels greater than six volts are permitted provided that V_{DD} is less than or equal to V_{IH}.

Since these devices require only one power supply, V_{DD}, they should be used in place of the '4009A and '4010A in all current driver or logic-level conversion applications. They are interchangeable with '4009A and '4010A, respectively, and can be substituted in existing as well as new designs. Pin 16 of the '4049A and '4050A is not internally connected; therefore, any external connection to this pin does not affect circuit operation.

TABLE 1

FUNCTION	INPUT HIGH-LEVEL VOLTAGE RANGE	OUTPUT HIGH-LEVEL VOLTAGE RANGE	POWER SUPPLY VOLTAGE RANGE (V_{DD})
Level Shifter	3 to 15 V	3 to 6 V	3 to 6 V
Buffer	3 to 15 V	3 to 15 V	3 to 15 V

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2, except as on following page

electrical characteristics

'4049 only

PARAMETER		TEST CONDITIONS†		TF4049A				TP4049A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IL}	Low-level input voltage		T_A = MIN or 25°C		1		2		1		2	V
			T_A = MAX		0.9		1.9		0.9		1.9	

'4049A and '4050A at V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4050A				TP4050A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−1.85		−1.85		−1.5		−1.5		mA
			T_A = 25°C	−1.25		−1.25		−1.25		−1.25		
			T_A = MAX	−0.9		−0.9		−1		−1		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL}	T_A = MIN	3.75		10		3.6		9.6		mA
			T_A = 25°C	3		8		3		8		
			T_A = MAX	2.1		5.6		2.5		6.6		
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		0.3		0.5		3		5	μA
			T_A = MAX		20		30		42		70	

'4049A and '4050A at V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4049A, TF4050A		TP4049A, TP4050A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		1.5		15	μA
			T_A = MAX		90		210	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

'4049A switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4049A				TP4049A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		120		95		160		125	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100		55		125		75	ns
t_{TLH}	Transition time, low-to-high-level output			170		85		225		120	ns
t_{THL}	Transition time, high-to-low-level output			70		55		90		75	ns

'4050A switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4050A				TP4050A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		180		125		250		160	ns
t_{PHL}	Propagation delay time, high-to-low-level output			155		80		200		110	ns
t_{TLH}	Transition time, low-to-high-level output			170		85		225		120	ns
t_{THL}	Transition time, high-to-low-level output			70		55		90		75	ns

§With a 15-pF load, these devices switch with times similar to those of the RCA CD4049A and RCA CD4050A respectively.
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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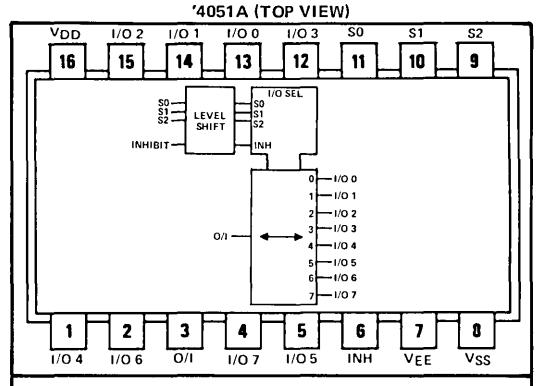
TYPES TF4051A, TF4052A, TF4053A, TP4051A, TP4052A, TP4053A
ANALOG MULTIPLEXERS/DEMULTIPLEXERS

SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4051A, CD4052A, and CD4053A
- Difference in r_{on} Between Switches in One Package Typically 5 Ω at $V_{DD}-V_{EE}$ = 15 V
- High Degree of Linearity . . . < 0.1% Distortion Typical at 1 kHz, $V_{DD}-V_{EE}$ = 15 V
- Switches Can Transmit Signals in Either Direction at Frequencies of up to 40 MHz Typically at $V_{DD}-V_{EE}$ = 10 V
- Extremely Low Off-State Switch Current Resulting in Very High Effective Off-State Resistance . . . 10 pA Typical at $V_{DD}-V_{SS}$ = 10 V
- Low Crosstalk Between Switches . . . 40 dB Typical at 1 MHz, R_L = 1 kΩ

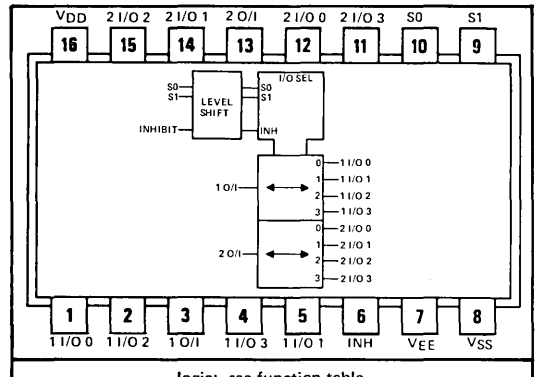
J OR N DUAL-IN-LINE PACKAGES

'4051A (TOP VIEW)



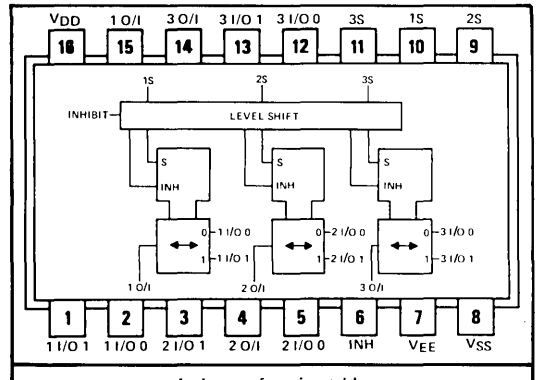
logic: see function table

'4052A (TOP VIEW)



logic: see function table

'4053A (TOP VIEW)



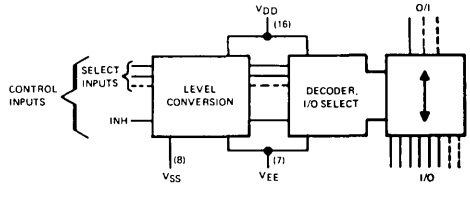
logic: see function table

description

These devices are analog multiplexers/demultiplexers incorporating built-in level shifting. Any combination of supply voltages is permissable provided that V_{SS} and V_{EE} are each within the range of −3 to −15 volts with respect to V_{DD}. The level shifting is between V_{SS} and V_{EE}. The control input range is V_{SS} to V_{DD} and the analog signal range is V_{EE} to V_{DD}. The common situation of positive digital signals controlling the multiplexing of both positive and negative analog signals can be accommodated. The table indicates some of the possible combinations of supply, input, and output voltages.

TYPICAL SUPPLY AND SIGNAL VOLTAGES

V_{DD}	15 V	10 V	7.5 V	7.5 V
V_{SS}	0 V	0 V	0 V	−7.5 V
V_{EE}	0 V	−5 V	−7.5 V	−7.5 V
Control Inputs	0 to 15 V	0 to 10 V	0 to 7.5 V	−7.5 to 7.5 V
Analog Signals	0 to 15 V	−5 to 10 V	−7.5 to 7.5 V	−7.5 to 7.5 V



INTERNAL POWER SUPPLY CONNECTIONS

TEXAS INSTRUMENTS
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POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

These digitally controlled bilateral analog switches have low on-state impedance and very low off-state current. When the inhibit input terminal is high, all channels are off.

The '4051A is a single eight-channel multiplexer having three binary control inputs (S0, S1, and S2) and an inhibit input. The three binary signals select one of eight channels to be turned on.

The '4052A is a dual four-channel multiplexer having two binary control inputs (S0 and S1) and an inhibit input. The two binary signals select one of four channels in each of the two sections and the selected channels are respectively paired between the independent sections.

The '4053A is a triple two-channel multiplexer having three separate control inputs (1S, 2S, and 3S) and a common inhibit input. Each input independently selects one of two channels in one of the three sections so that any of eight combinations may be selected.

'4051A
FUNCTION TABLE

INPUTS				CHANNEL
INH	S2	S1	S0	TURNED ON
H	X	X	X	None
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7

'4052A
FUNCTION TABLE
(EACH BILATERAL SWITCH)

INPUTS			CHANNEL
INH	S1	S0	TURNED ON
H	X	X	None
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3

'4053A
FUNCTION TABLE
(EACH BILATERAL SWITCH)

INPUTS		CHANNEL
INH	S	TURNED ON
H	X	None
L	L	0
L	H	1

H = high level, L = low level, X = irrelevant

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62 and below	Page 62	Page 63, group 3, except as below. I_{OH} and I_{OL} do not apply.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{EE} (with respect to V_{DD}) . . . . . −15 V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted), $V_{EE} = V_{SS} = 0$ V

PARAMETER	TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		UNIT
			MIN	MAX	MIN	MAX	
V_{OH} High-level output voltage	Control inputs at V_{IH} min or V_{IL} max, I/O at 0 V, I_O = 10 μA	Channel off,	4.5		9		V
V_{OL} Low-level output voltage	Control inputs at V_{IH} min or V_{IL} max, I/O at 0 V, I_O = 10 μA	Channel on,		0.5		1	V
Input-to-output off-state current	Control inputs at 0 V or V_{DD}, I/O at 5 V, O/I at 0 V to V_{DD},	Channel off, T_A = 25°C				±125	nA

on-state resistance at 25°C free-air temperature, R_L = 10 kΩ to 0 V

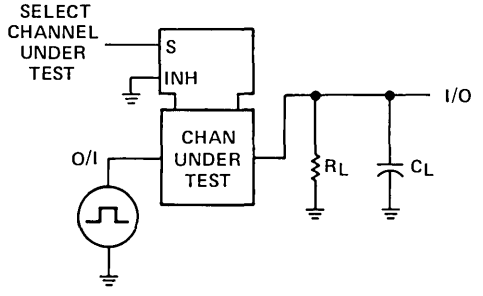
TEST CONDITIONS			TYP	MAX	UNIT
V_{DD} = 7.5 V	V_{EE} = −7.5 V,	V_{SS} = 0 V	80		Ω
V_{DD} = 15 V,	V_{EE} = 0 V,	V_{SS} = 0 V			
V_{DD} = 5 V,	V_{EE} = −5 V,	V_{SS} = 0 V	120		Ω
V_{DD} = 10 V,	V_{EE} = 0 V,	V_{SS} = 0 V			
V_{DD} = 5 V,	V_{EE} = 0 V,	V_{SS} = 0 V	270		Ω

switching characteristics at 25°C free-air temperature, $V_{EE} = V_{SS} = 0$ V

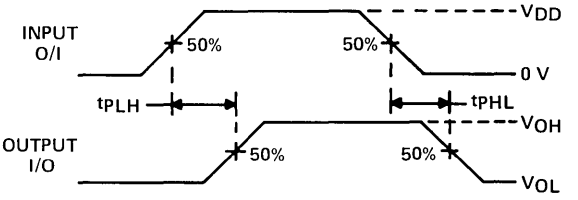
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDTIONS		V_{DD} = 5 V		V_{DD} = 10 V		UNIT
					TYP	MAX	TYP	MAX	
t_{PLH}	O/I	I/O	R_L = 10 kΩ,	C_L = 50 pF,	25		10		ns
t_{PHL}	O/I	I/O	See Figure 1,	$V_{EE} = V_{SS}$ = 0 V	25		10		
t_{PLH}	S	I/O	C_L = 50 pF,	R_L = 10 kΩ to 0 V	400		200		ns
t_{PHL}	S	I/O	See Figure 2	R_L = 10 kΩ to V_{DD}	400		200		
t_{PLH}	INH	I/O	R_L = 10 kΩ,	C_L = 50 pF,	600		300		ns
t_{PHL}	INH	I/O	See Figure 2		600		300		

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output.
t_{PHL} ≡ Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT

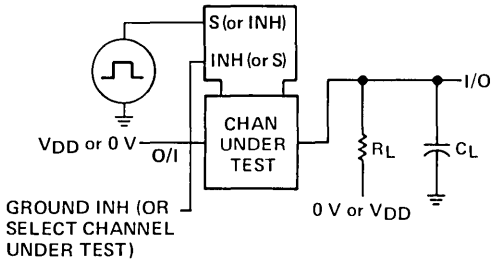


TEST CIRCUIT

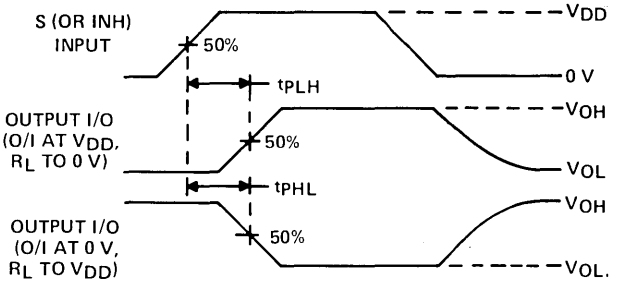


VOLTAGE WAVEFORMS

FIGURE 1



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
B. C_L includes probe and jig capacitance.
C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 20$ ns, $R_{in} \geq 1$ MΩ.

TEXAS INSTRUMENTS
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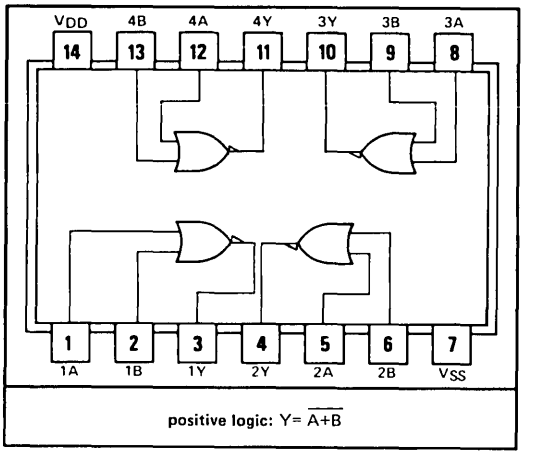
TYPES TF4301A, TP4301A
QUAD 2-INPUT NOR BUFFERS

SEPTEMBER 1975

- Buffer Circuit Designed to be Plug-In Replacement for RCA CD4001A
- Improved Static and Dynamic Drive Characteristics

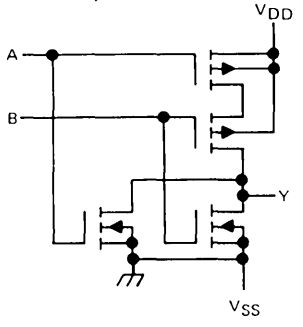
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 1, and below

schematic (each buffer)



electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4301A				TP4301A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	2		4		1.6		3.2		mA
			T_A = 25°C	1.6		3.2		1.3		2.6		
			T_A = MAX	1.1		2.2		0.9		1.8		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4301A				TP4301A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		120		80		160		110	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100		70		130		100	ns
t_{TLH}	Transition time, low-to-high-level output			300		150		400		200	ns
t_{THL}	Transition time, high-to-low-level output			220		110		300		150	ns

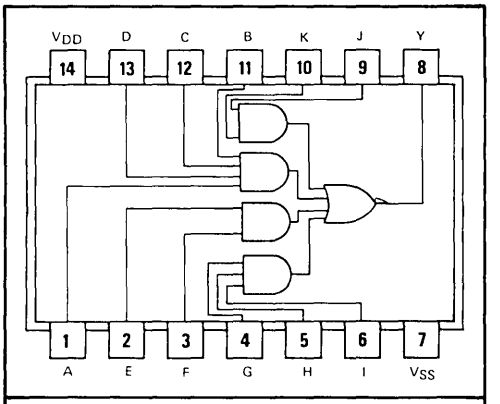
NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES TF4302A, TF4303A, TP4302A, TP4303A
AND-OR-INVERT GATES

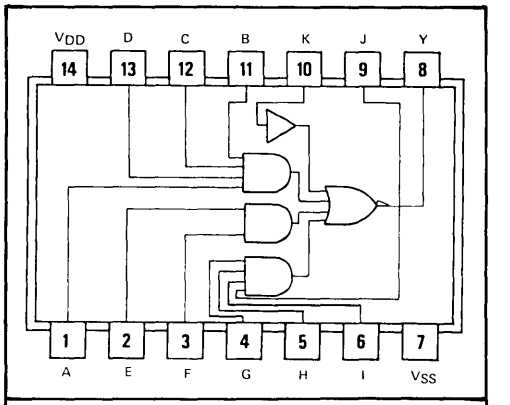
SEPTEMBER 1975

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4302A, TP4302A



positive logic: $Y = \overline{ABCD + EF + GHI + JK}$

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)
TF4303A, TP4303A



positive logic: $Y = \overline{ABCD + EF + GHIJ + K}$

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4302A, TF4303A				TP4302A, TP4303A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		500		200		675		275	ns
t_{PHL}	Propagation delay time, high-to-low-level output			500		200		675		275	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		225	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		225	ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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TEXAS INSTRUMENTS
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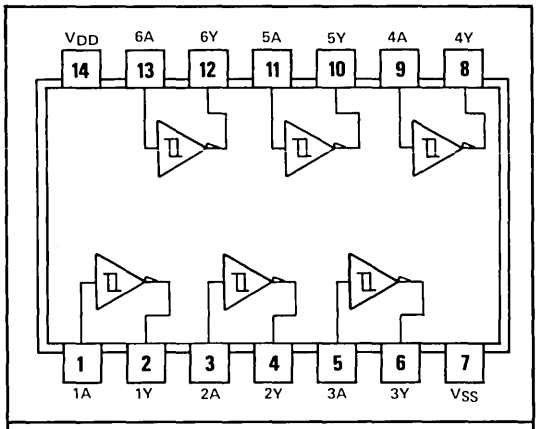
TYPES TF4304A, TP4304A
HEX SCHMITT TRIGGER

SEPTEMBER 1975

- No External Components Required for Schmitt Trigger Action
- No Limit on Input Rise and Fall Times
- Typical Hysteresis . . . 0.6 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

description

These circuits are hex inverting Schmitt triggers for use where low power dissipation and/or high noise immunity is desired. Applications include the speedup of a slow waveform edge in interface receivers, level detectors, etc.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2 except as below

electrical characteristics (see note 1)

PARAMETER		TEST CONDITIONS		TF4304A				TP4304A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{T+}	Positive-going threshold voltage		T_A = 25°C	2.3	3.5	4.5	7	2.3	3.5	4.5	7	V
V_{T-}	Negative-going threshold voltage		T_A = 25°C	1.5	2.7	3	5.5	1.5	2.7	3	5.5	V
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = 0 or V_{DD}, No load	T_A = MIN or 25°C		0.5		1		5		10	μA
			T_A = MAX		30		60		70		140	

†T_A = MIN or MAX refers to the respective values of free-air temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4304A				TP4304A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 2		630		250		900		400	ns
t_{PHL}	Propagation delay time, high-to-low-level output			630		250		900		400	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		225	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		225	ns

NOTES: 1. When testing V_{OH} at T_A = 25°C, V_{T+} min and V_{T-} min replace V_{IL} max. When testing V_{OL} at T_A = 25°C, V_{T+} max and V_{T-} max replace V_{IH} min. Minimum and maximum levels of V_{T+} are set by applying an input voltage below V_{IL} max and then increasing it to the specified level. Minimum and maximum levels of V_{T-} are set by applying an input voltage above V_{IH} min and then decreasing it to the specified level.

2. See load circuit and voltage waveforms on page 170.

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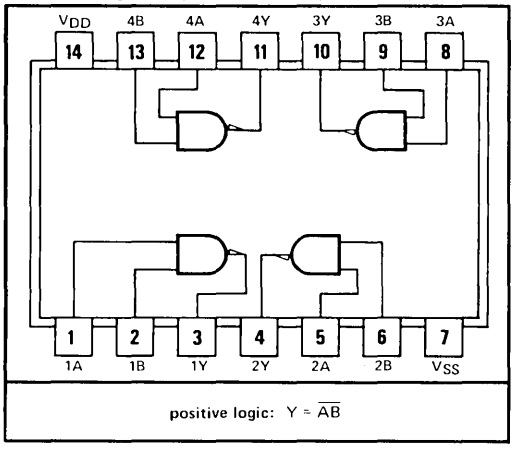
TYPES TF4311A, TP4311A
QUAD 2-INPUT NAND BUFFERS

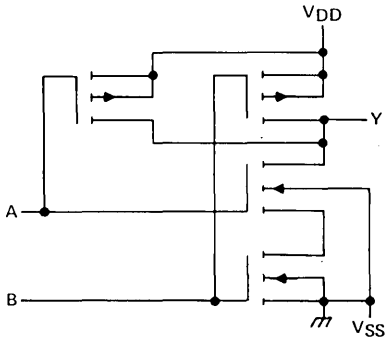
SEPTEMBER 1975

- Buffer Circuit Designed to be Plug-In Replacement for RCA CD4011A
- Improved Static and Dynamic Drive Characteristics

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each buffer)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 1, except as below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4311A				TP4311A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−0.65		−0.75		−0.35		−0.35		mA
			T_A = 25°C	−0.5		−0.6		−0.3		−0.3		
			T_A = MAX	−0.35		−0.4		−0.25		−0.25		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	1		2		0.8		1.6		mA
			T_A = 25°C	0.75		1.6		0.65		1.3		
			T_A = MAX	0.55		1.1		0.45		0.9		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4311A				TP4311A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		100		70		130		100	ns
t_{PHL}	Propagation delay time, high-to-low-level output			120		80		160		110	ns
t_{TLH}	Transition time, low-to-high-level output			220		110		300		150	ns
t_{THL}	Transition time, high-to-low-level output			300		150		400		200	ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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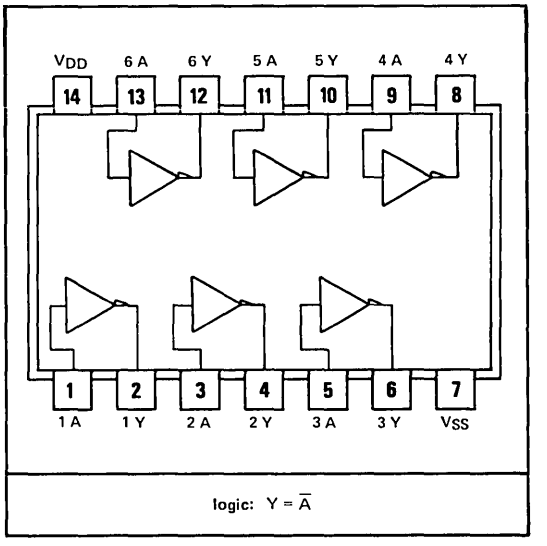
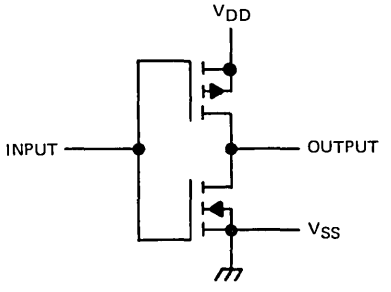
TYPES TF4315A, TP4315A
HEX INVERTING BUFFERS

SEPTEMBER 1975

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each buffer)



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 1

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4315A				TP4315A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		135		75		180		100	ns
t_{PHL}	Propagation delay time, high-to-low-level output			135		75		180		100	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	ns

NOTE 1: See load circuit and voltage waveforms on page 170.

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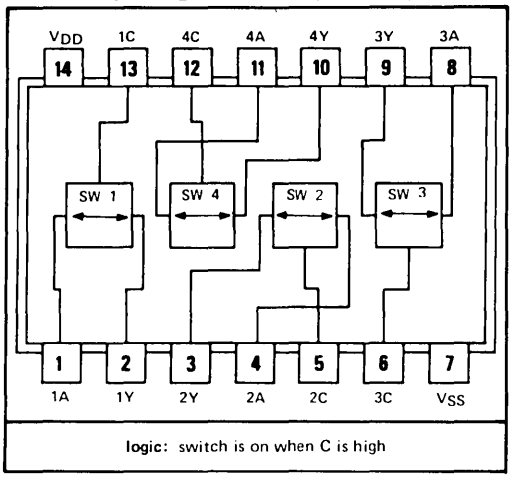
TYPES TF4316A, TP4316A
QUAD BILATERAL SWITCHES

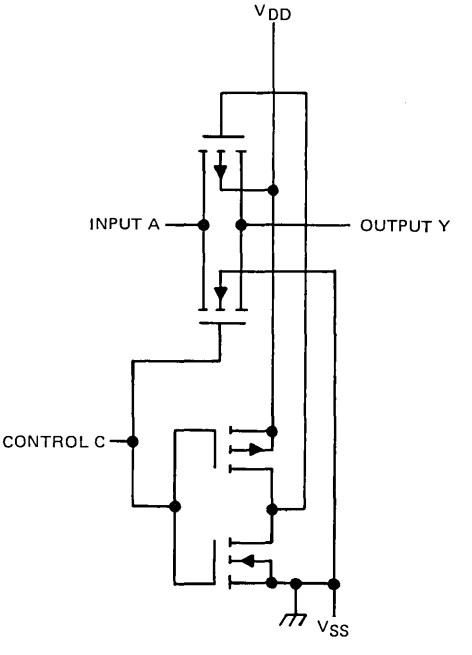
SEPTEMBER 1975

- Designed to be Interchangeable with RCA CD4016A
- Difference in r_{on} between Switches in One Package Typically 10 Ω when $V_I = V_{SS}$ or V_{DD}
- High Degree of Linearity . . . < 0.5% Distortion Typical at 1 kHz
- Switches Can Transmit Signals in Either Direction at Frequencies of up to 50 MHz Typically
- Extremely Low Off-State Switch Current Resulting in Very High Effective Off-State Resistance . . . 10 pA Typical at $V_{DD}-V_{SS} = 10$ V
- Maximum Control Input Frequency . . . 10 MHz Typical at $V_{DD} = 10$ V, $C_L = 15$ pF, $R_L = 1$ kΩ
- High On/Off Output Voltage Ratio . . . 65 dB Typical
- Extremely High Control-Input Impedance (Control Circuit Isolated from Switch Circuit) . . . 10^{12} Ω Typical
- Low Crosstalk Between Switches . . . 50 dB Typical at 0.9 MHz, $R_L = 1$ kΩ
- Control Input Current . . . < 10 pA Typical

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each switch)



description

The '4316A is a quadruple bilateral switch constructed with P-channel and N-channel enhancement-type devices in a monolithic structure, and finds primary use where low power dissipation and/or high noise immunity is desired.

Applications include digital switching and multiplexing; analog-to-digital and digital-to-analog conversion; digital control of frequency, impedance, phase and analog-signal gain; signal gating; and use as a squelch control, chopper, modulator, demodulator, or commutating switch.

The P^- well is permanently connected to V_{SS}. This results in a higher average on-state resistance than the '4016A has but lower transient current into input A.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	See the following page. Page 63 does not apply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		V_{DD} = 5	TF4316A	TP4316A	UNIT
					V_{DD} = 10 V		
				MIN MAX	MIN MAX	MIN MAX	
V_{IH}	High-level control input voltage			3	4	4	V
V_{IL}	Low-level control input voltage			0.9	0.9	0.9	V
V_{OH}	High-level output voltage	A at 0 V, C at V_{IL} max,	I_O = 10 μA	4.5	9	9	V
V_{OL}	Low-level output voltage	A at 0 V, C at V_{IH} min,	I_O = 10 μA	0.5	1	1	V
	Input-to-output off-state current	A at 0 V to V_{DD}, C at 0 V, Y at 5 V	T_A = 25°C		±125	±125	nA
	Total Quiescent Current¶	A at 0 V to V_{DD}, C at 0 V, Y at 0 V to V_{DD}	T_A = MIN or 25°C		1	1	μA
			T_A = MAX		60	16	
		A = Y = 0 V to V_{DD}, C at V_{DD}	T_A = MIN or 25°C		1	1	μA
			T_A = MAX		60	16	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4016A	TP4016A	UNIT
				MIN MAX	MIN MAX	
I_I	Input current	V_I = 0 or V_{DD}		±1	±1	μA
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C	3	3	μA
			T_A = MAX	180	48	

†T_A = MIN or MAX refers to the respective values of free-air temperature specified under recommended operating conditions.
¶This is the total of supply current, control input current, and input-to-output off-state current.

on-state resistance at specified free-air temperature, C at V_{DD}, R_L = 10 kΩ to 0 V

TEST CONDITIONS†				TF4316A	TP4316A	UNIT
				MIN MAX	MIN MAX	
V_{DD} = 5 V,	V_{SS} = −5 V	A at 5 V or −5 V	T_A = MIN	600	610	Ω
			T_A = 25°C	660	660	
			T_A = MAX	960	840	
		A at 0.25 V or −0.25 V	T_A = MIN	1870	1900	Ω
			T_A = 25°C	2000	2000	
			T_A = MAX	2600	2380	
V_{DD} = 7.5 V,	V_{SS} = −7.5 V	A at 7.5 V or −7.5 V	T_A = MIN	360	370	Ω
			T_A = 25°C	400	400	
			T_A = MAX	600	520	
		A at 0.25 V or −0.25 V	T_A = MIN	775	790	Ω
			T_A = 25°C	850	850	
			T_A = MAX	1230	1080	
V_{DD} = 10 V,	V_{SS} = 0 V	A at 10 V or 0.25 V	T_A = MIN	600	610	Ω
			T_A = 25°C	660	660	
			T_A = MAX	960	840	
		A at 5.6 V	T_A = MIN	1870	1900	Ω
			T_A = 25°C	2000	2000	
			T_A = MAX	2600	2380	
V_{DD} = 15 V,	V_{SS} = 0 V	A at 15 V or 0.25 V	T_A = MIN	360	370	Ω
			T_A = 25°C	400	400	
			T_A = MAX	600	520	
		A at 9.3 V	T_A = MIN	775	790	Ω
			T_A = 25°C	850	850	
			T_A = MAX	1230	1080	

†T_A = MIN or MAX refers to the respective values of free-air temperature specified under recommended operating conditions.

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switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{DD} = 5 V		V_{DD} = 10 V		UNIT
					TYP	MAX	TYP	MAX	
t_{PLH}	A	Y	R_L = 10 kΩ, C at V_{DD},	C_L = 50 pF, See Figure 1	30		15		ns
t_{PHL}	A	Y			30		15		
t_{PLH}	C	Y	C_L = 50 pF, See Figure 2	R_L = 10 kΩ to 0 V	80		30		ns
t_{PHL}	C	Y		R_L = 10 kΩ to V_{DD}	80		30		

‡t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

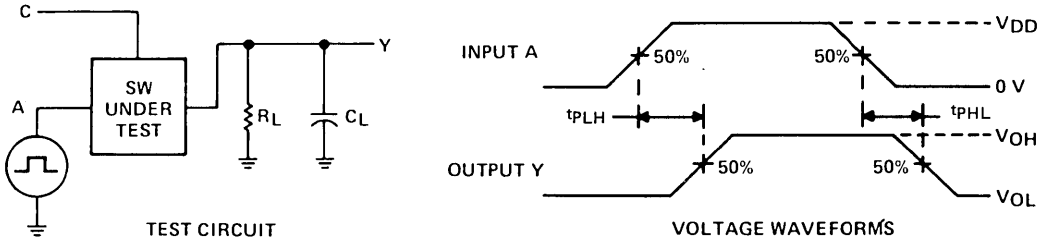


FIGURE 1–PROPAGATION DELAY TIME, SWITCH INPUT A TO OUTPUT Y

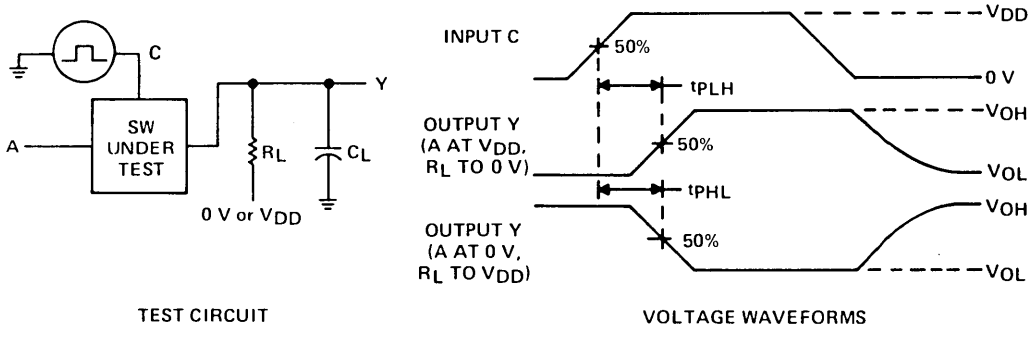


FIGURE 2–PROPAGATION DELAY TIMES, CONTROL INPUT C TO OUTPUT Y

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
B. C_L includes probe and jig capacitance.
C. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 1$ MΩ.

TYPES TF4320A, TP4320A
16-CHANNEL DATA SELECTORS WITH 3-STATE OUTPUTS

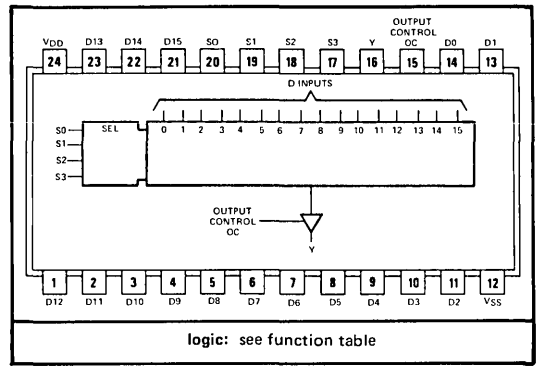
SEPTEMBER 1975

- 3-State Output

description

These circuits are single 16-channel data selectors having four digital select inputs, S0, S1, S2, and S3, and an output control. When the output control is low, the output will be in the high-impedance (off) state. Applications of this device include signal multiplexing, data routing, and number sequence generation.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

FUNCTION TABLE

INPUTS					OUTPUT
OUTPUT CONTROL	S3	S2	S1	S0	Y
L	X	X	X	X	Z
H	L	L	L	L	D0
H	L	L	L	H	D1
H	L	L	H	L	D2
H	L	L	H	H	D3
H	L	H	L	L	D4
H	L	H	L	H	D5
H	L	H	H	L	D6
H	L	H	H	H	D7
H	H	L	L	L	D8
H	H	L	L	H	D9
H	H	L	H	L	D10
H	H	L	H	H	D11
H	H	H	L	L	D12
H	H	H	L	H	D13
H	H	H	H	L	D14
H	H	H	H	H	D15

H = high level, L = low level, X = irrelevant, Z = high-impedance (off)
D0 . . . D15 = the logic level of the indicated D input.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3, and below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4320A				TP4320A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.5		−0.5		−0.25		−0.25		mA
			T_A = 25°C	−0.4		−0.4		−0.2		−0.2		
			T_A = MAX	−0.3		−0.3		−0.17		−0.17		
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.3		0.6		0.2		0.35		mA
			T_A = 25°C	0.25		0.5		0.15		0.3		
			T_A = MAX	0.2		0.4		0.12		0.25		
I_{OZH}	Off-state output current, high-level voltage applied	OC at V_{SS}, $V_O = V_{DD}$	T_A = MIN or 25°C		0.05		0.1		0.5		1	μA
			T_A = MAX		3		6		7		14	
I_{OZL}	Off-state output current, low-level voltage applied	OC at V_{SS}, V_O = 0 V	T_A = MIN or 25°C		−0.05		−0.1		−0.5		−1	μA
			T_A = MAX		−3		−6		−7		−14	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

TEXAS INSTRUMENTS
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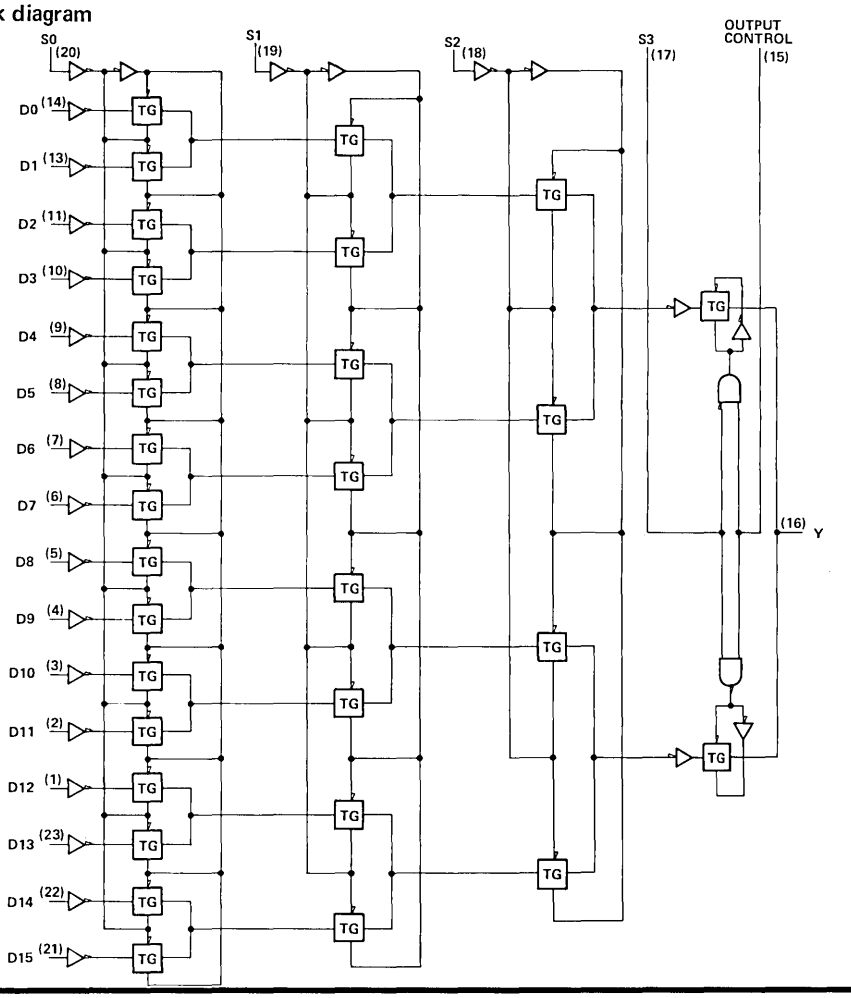
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4320A				TP4320A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		750		325		1000		375	ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		325		1000		375	ns
t_{TLH}	Transition time, low-to-high-level output			500		250		600		300	ns
t_{THL}	Transition time, high-to-low-level output			500		250		600		300	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, R_L = 10 kΩ, See Note 1		430		150		500		200	ns
t_{PZL}	Output enable time to low level			250		130		300		170	
t_{PHZ}	Output disable time from high level			260		170		320		240	ns
t_{PLZ}	Output disable time from low level			160		140		220		200	

NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



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TYPES TF4321A, TP4321A
DUAL 8-CHANNEL DATA SELECTORS WITH 3-STATE OUTPUTS

SEPTEMBER 1975

- 3-State Output

description

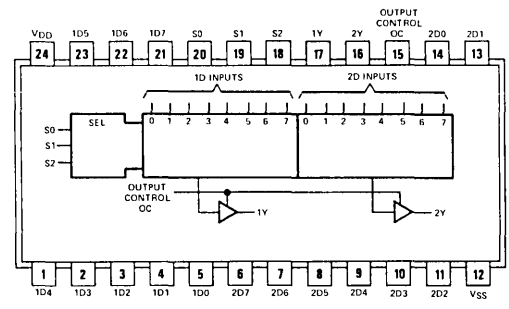
These circuits are dual 8-channel data selectors having three digital select inputs, S0, S1, and S2, and an output control. When the output control is low, both outputs will be in the high-impedance (off) state. Applications of this device include signal multiplexing, data routing, and number sequence generation.

FUNCTION TABLE
(EACH SELECTOR)

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT S2	S1	S0	
L	X	X	X	Z
H	L	L	L	D0
H	L	L	H	D1
H	L	H	L	D2
H	L	H	H	D3
H	H	L	L	D4
H	H	L	H	D5
H	H	H	L	D6
H	H	H	H	D7

H = high level, L = low level, X = irrelevant, Z = high-impedance (off).
D0 . . . D7 = the logic level of the indicated D input.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3, and below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4321A		TP4321A		UNIT
				V_{DD} = 5 V	V_{DD} = 10 V	V_{DD} = 5 V	V_{DD} = 10 V	
				MIN MAX	MIN MAX	MIN MAX	MIN MAX	
I_{OH}	High-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OH}$ min	T_A = MIN	−0.5	−0.5	−0.25	−0.25	mA
			T_A = 25°C	−0.4	−0.4	−0.2	−0.2	
			T_A = MAX	−0.3	−0.3	−0.17	−0.17	
I_{OL}	Low-level output current	$V_{IH} = V_{DD}$, $V_{IL} = 0$, $V_O = V_{OL}$ max	T_A = MIN	0.3	0.6	0.2	0.35	mA
			T_A = 25°C	0.25	0.5	0.15	0.3	
			T_A = MAX	0.2	0.4	0.12	0.25	
I_{OZH}	Off-state output current, high-level voltage applied	OC at V_{SS}, $V_O = V_{DD}$	T_A = MIN or 25°C	0.05	0.1	0.5	1	μA
			T_A = MAX	3	6	7	14	
I_{OZL}	Off-state output current, low-level voltage applied	OC at V_{SS}, V_O = 0 V	T_A = MIN or 25°C	−0.05	−0.1	−0.5	−1	μA
			T_A = MAX	−3	−6	−7	−14	

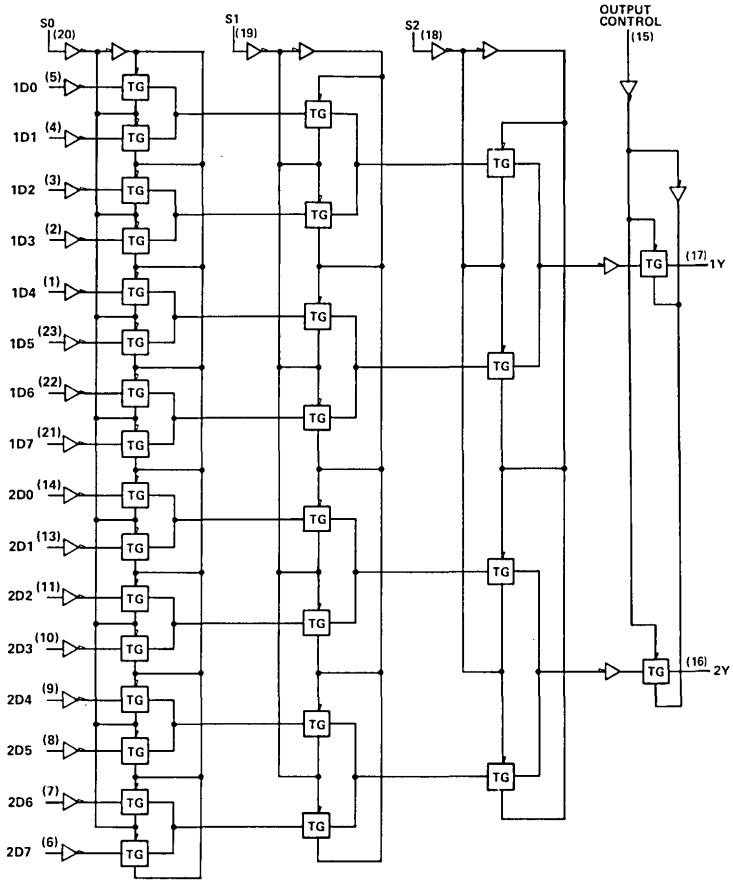
†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4321A				TP4321A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		750		325		1000		375	ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		325		1000		375	ns
t_{TLH}	Transition time, low-to-high-level output			500		250		600		300	ns
t_{THL}	Transition time, high-to-low-level output			500		250		600		300	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, R_L = 10 kΩ, See Note 1		430		150		500		200	ns
t_{PZL}	Output enable time to low level			250		130		300		170	
t_{PHZ}	Output disable time from high level			260		170		320		240	ns
t_{PLZ}	Output disable time from low level			160		140		220		200	

NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



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TEXAS INSTRUMENTS
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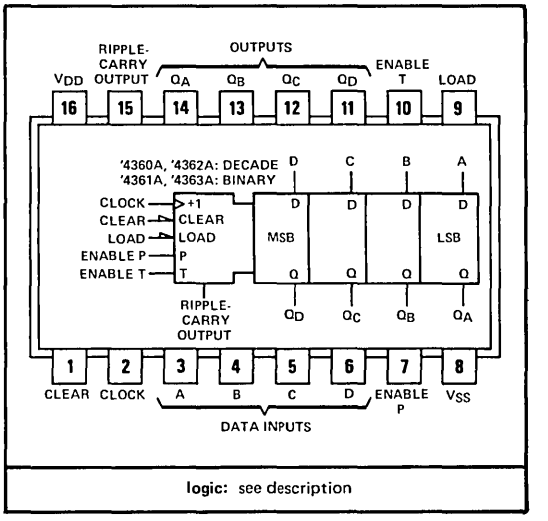
TYPES TF4360A THRU TF4363A, TP4360A THRU TP4363A SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

SEPTEMBER 1975

'4360A DECADE COUNTER WITH ASYNCHRONOUS CLEAR
'4361A BINARY COUNTER WITH ASYNCHRONOUS CLEAR
'4362A DECADE COUNTER WITH SYNCHRONOUS CLEAR
'4363A BINARY COUNTER WITH SYNCHRONOUS CLEAR

- Designed to be Interchangeable with National Semiconductor MM54C160, MM74C160, MM54C161, MM74C161, MM54C162, MM74C162, MM54C163, and MM74C163
- Counting Rate . . . 8 MHz Typical at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

These synchronous presettable up counters feature an internal carry look-ahead for cascading packages without additional gating in high-speed counting systems.

A low level at the load input disables the counter and causes the outputs to agree with the setup data after the next low-to-high transition of the clock. The clear function of the '4360A and '4361A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. The clear function of the '4362A and '4363A is synchronous and a low level at the clear input sets all four outputs low after the next low-to-high transition of the clock regardless of the levels of the load or enable inputs. Both count-enable inputs (P and T) must be high to count, and T is fed forward to enable the ripple-carry output. The ripple-carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

TEXAS INSTRUMENTS
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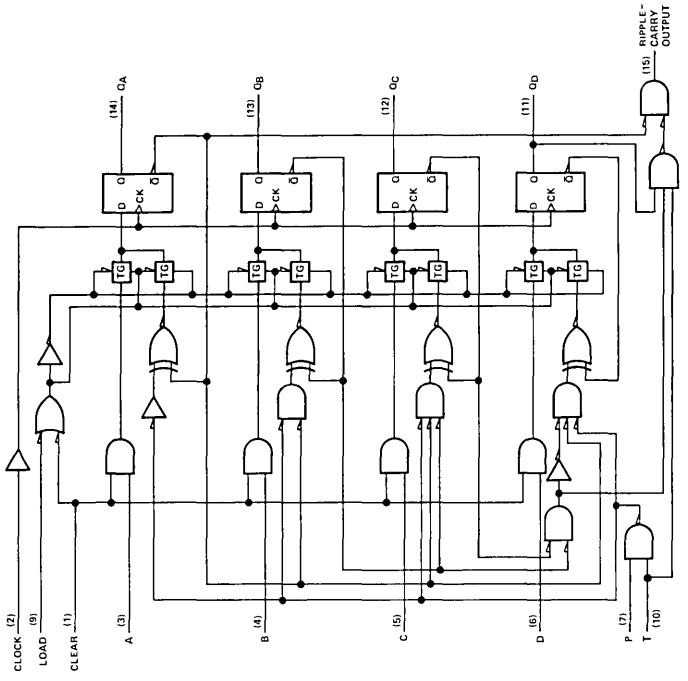
functional block diagrams

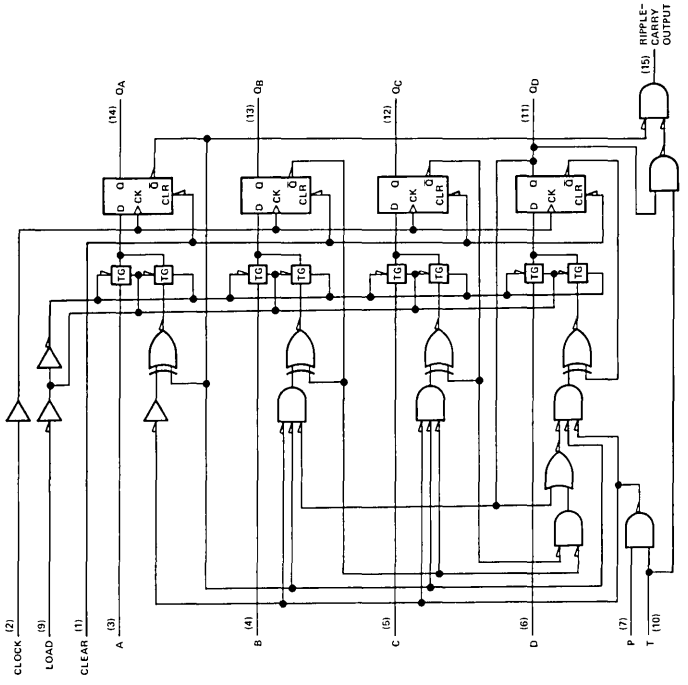
'4363A BINARY COUNTER WITH SYNCHRONOUS CLEAR

'4361A binary counters are similar; however, the clear is direct (asynchronous) as shown for the '4360A decade counters at left.



'4360A DECADE COUNTER WITH ASYNCHRONOUS CLEAR

'4362A decade counters are similar; however, the clear is synchronous as shown for the '4363A binary counters at right.

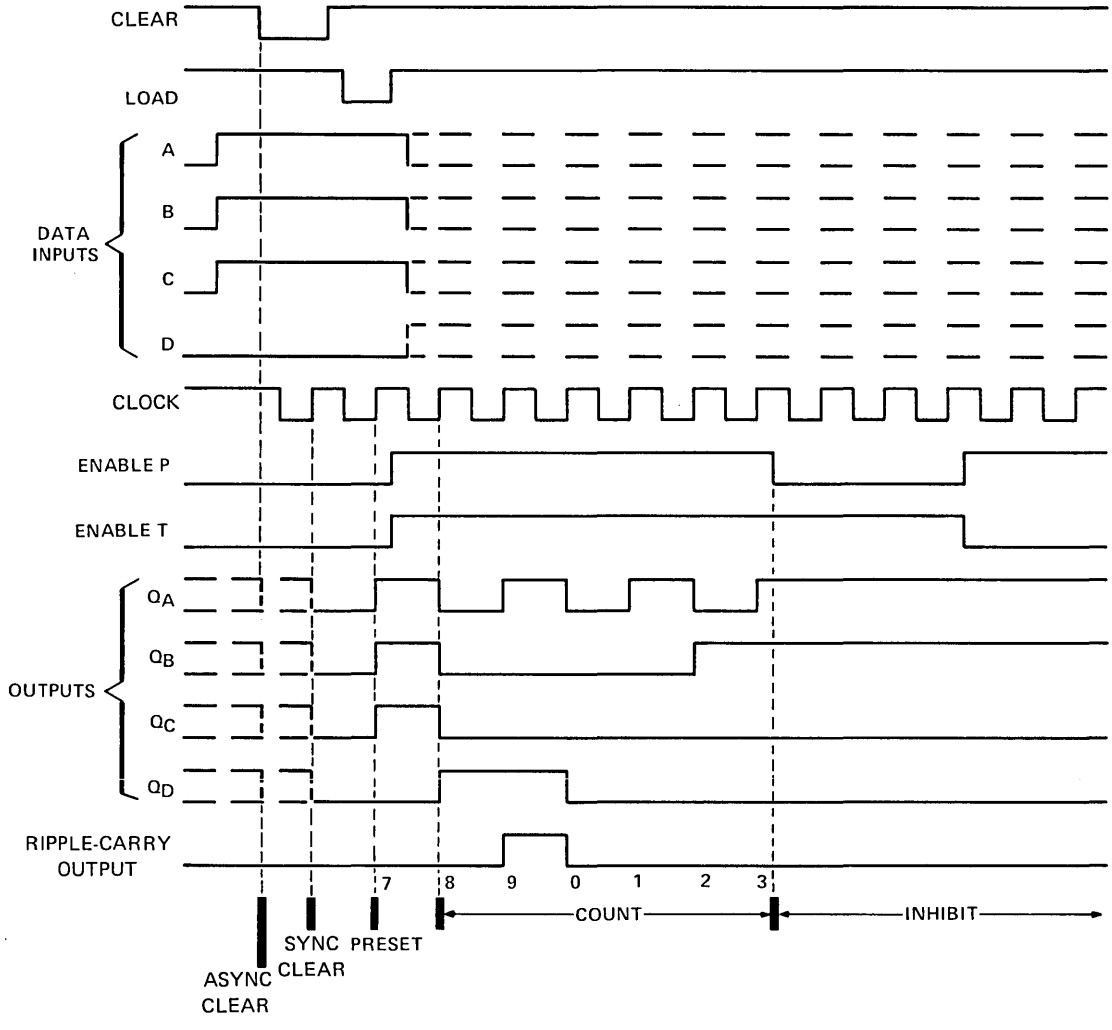


'4360A AND '4362A DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear output to zero ('4360A is asynchronous, '4362A is synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



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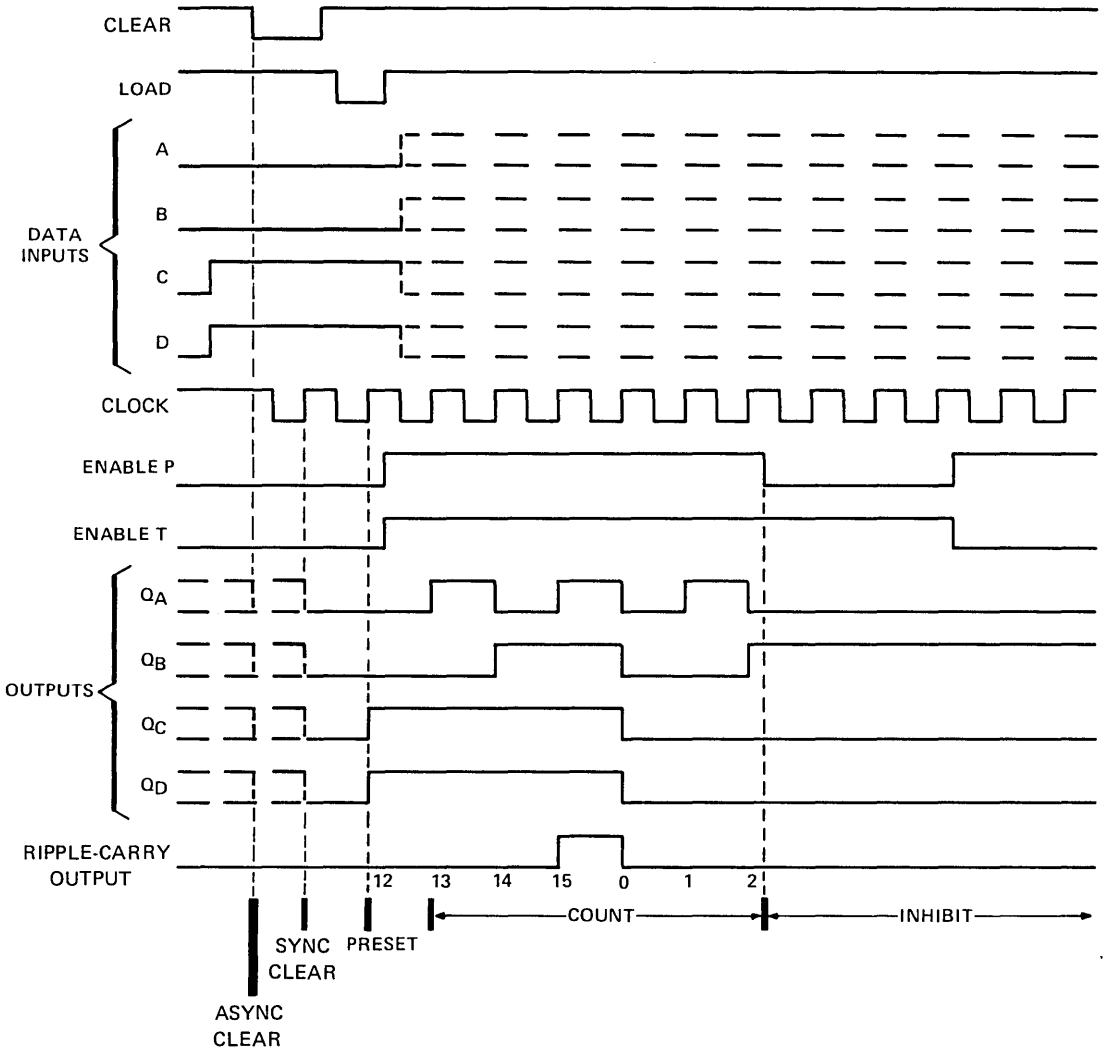
'4361A AND '4363A BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('4361A is asynchronous, '4363A is synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3

recommended operating conditions

		TF4360A, TF4361A TF4362A, TF4363A				TP4360A, TP4361A TP4362A, TP4363A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Width of clock pulse, $t_{w(clock)}$	Clock high or low	200		90		300		150		ns
Setup time, t_{su}	Data or load	200		80		300		110		ns
	Enable P or T	375		150		500		200		
	Clear◇	250		100		350		135		

◇This applies only for '4362A and '4363A, which have synchronous clear inputs.

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4360A, TF4361A TF4362A, TF4363A				TP4360A, TP4361A TP4362A, TP4363A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF, R_L = 200 kΩ, See Note 1	1		3		0.6		2.5		MHz
t_{PLH}	Clock	Any Q			550		200		750		275	ns
t_{PHL}					550		200		750		275	
t_{PLH}	Clock	Ripple-carry output			650		250		850		350	ns
t_{PHL}					650		250		850		350	
t_{PLH}	Enable T	Ripple-carry output			350		175		490		240	ns
t_{PHL}					350		175		490		240	
t_{PHL}□	Clear	Any Q			400		250		550		350	ns
t_{TLH}		Any			300		150		400		220	ns
t_{THL}					300		150		400		220	

‡f_{max} = Maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{TLH} = Transition time, low-to-high-level output
t_{THL} = Transition time, high-to-low-level output

□This applies only for '4360A and '4361A, which have asynchronous clear inputs.

NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4370A, TP4370A
QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SEPTEMBER 1975

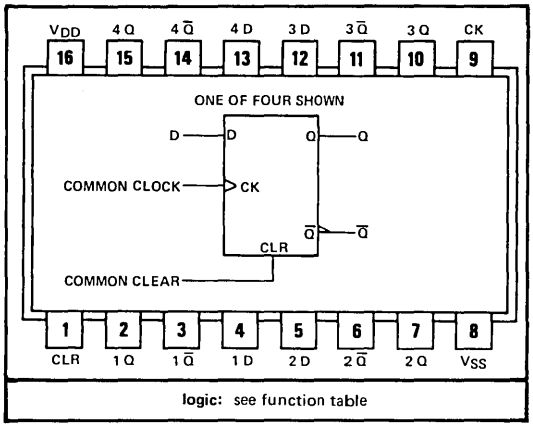
- Maximum Clock Frequency . . . 10 MHz Typical at 10 V

description

These circuits are quad D-type transition-operated master-slave flip-flops with buffered outputs, common direct overriding clear input, and D and clock inputs. While the clock is low, the data at the D input is entered into the master section, which is isolated from the slave section. On the rising transition of the clock, the D input is disabled and data previously set up in the master section is transferred to the slave section and appears in true form at the Q output and in complementary form at the $\overline{Q}$ output.

Clearing is independent of the clock and is accomplished by a high-level voltage at the clear input.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

FUNCTION TABLE
(EACH FLIP-FLOP)

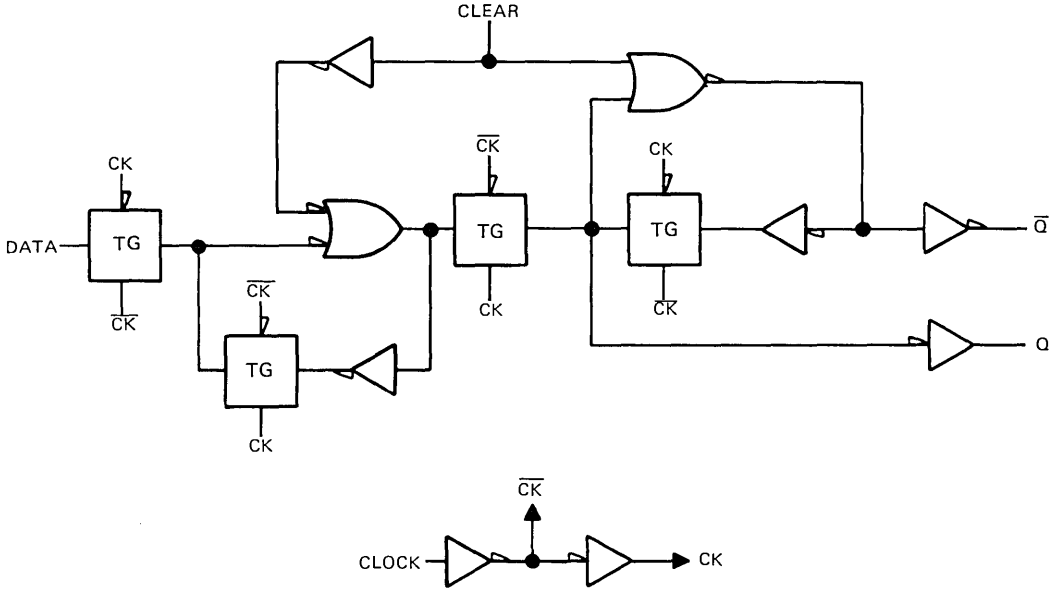
INPUTS			OUTPUTS	
Clear	CK	D	Q	$\overline{Q}$
H	X	X	L	H
L	↑	L	L	H
L	↑	H	H	L
L	L	X	Q_0	$\overline{Q}_0$

See explanation of function tables on pages 16 and 17.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 63 and on following page	Page 63, group 3

functional block diagram (each flip-flop)



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recommended operating conditions

		TF4370A				TP4370A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	200		80		500		100		ns
	Clear	250		100		500		125		ns
Setup time, t_{su}		60		20		120		30		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4370A				TP4370A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF, R_L = 200 kΩ, See Note 1	2.5		7		1		5		MHz
t_{PLH} or t_{PHL}	Clock	Any Q or $\overline{Q}$			475		185		500		235	ns
t_{PLH} or t_{PHL}	Clear	Any Q or $\overline{Q}$			475		185		550		235	ns
t_{TLH} or t_{THL}		Any			350		150		400		220	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4376A, TF4377A, TP4376A, TP4377A
QUAD S-R AND $\overline{S}$-$\overline{R}$ LATCHES

SEPTEMBER 1975

- **Same as TF4043A, TF4044A, TP4043A, and TP4044A, Respectively, except with Normal 2-State Totem-Pole Outputs**

description

The '4376 and '4377A are quadruple S-R and $\overline{S}$-$\overline{R}$ latches, respectively, with normal two-state totem-pole outputs. Each latch has separate active-high ('4376A) or active-low ('4377A) set and reset inputs.

FUNCTION TABLES
(EACH LATCH)

TF4376A, TP4376A

INPUTS		OUTPUT
S	R	Q
L	L	No change
H	L	H
L	H	L
H	H	H*

TF4377A, TP4377A

INPUTS		OUTPUT
$\overline{S}$	$\overline{R}$	Q
H	H	No change
L	H	H
H	L	L
L	L	L*

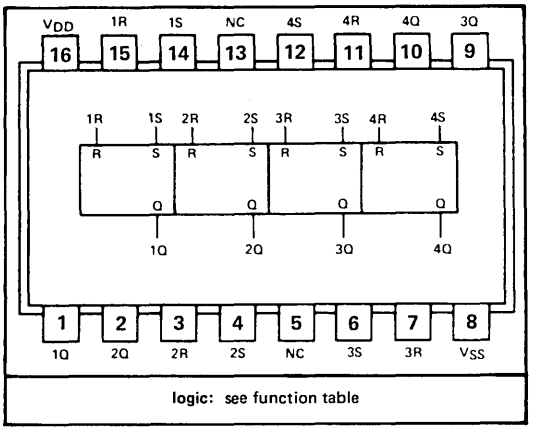
*This output level is psuedo stable; that is, it may not persist when the S and R inputs return to their inactive (low) level or the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level. See explanation of function tables, pages 16 and 17.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3, except as on following page

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

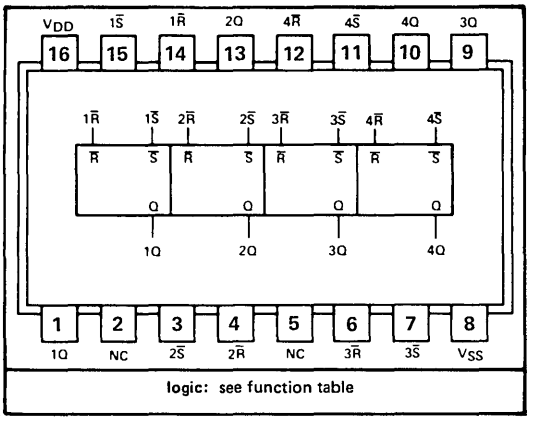
TF4376A, TP4376A



logic: see function table

NC—No internal connection

TF4377A, TP4377A

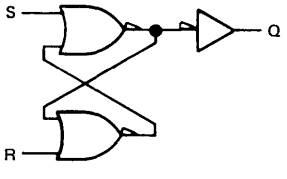


logic: see function table

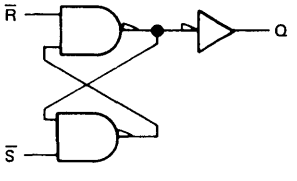
NC—No internal connection

functional block diagrams (each latch)

TF4376A, TP4376A



TF4377A, TP4377A



TEXAS INSTRUMENTS
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recommended operating conditions

	TF4376A, TF4377A				TP4376A, TP4377A				UNIT
	V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, set or reset, t_w	200		100		225		110		ns

electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER	TEST CONDITIONS†		TF4376A, TF4377A				TP4376A, TP4377A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$ Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		1		2		10		20	μA
		T_A = MAX		60		120		140		280	

V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TF4376A, TF4377A		TP4376A, TP4377A		UNIT
			MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$ Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		6		60	μA
		T_A = MAX		360		840	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER	TEST CONDITIONS	TF4376A, TF4377A				TP4376A, TP4377A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 200 kΩ, See Note 1		500		235		575		300	ns
t_{PHL} Propagation delay time, high-to-low-level output			500		235		575		300	ns
t_{TLH} Transition time, low-to-high-level output			325		135		375		200	ns
t_{THL} Transition time, high-to-low-level output			325		135		375		200	ns

NOTE 1: See load circuit and voltage waveforms on page 170.

TEXAS INSTRUMENTS
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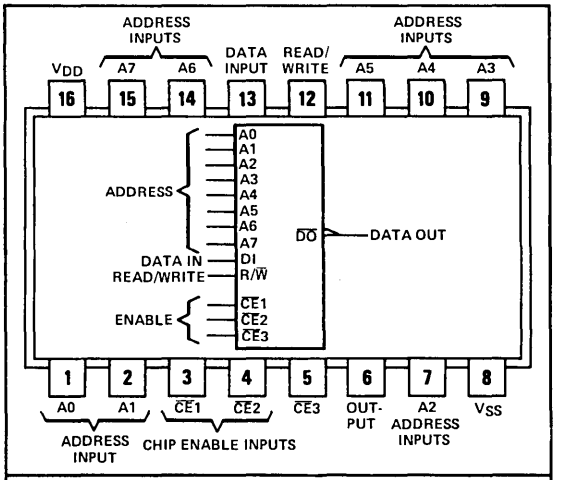
FUTURE CMOS PRODUCT TO BE ANNOUNCED

TYPES TF4380A, TP4380A 256-BIT RANDOM-ACCESS MEMORIES WITH 3-STATE OUTPUTS

SEPTEMBER 1975

- Static Memory
- Fully Decoded, Organized as 256 Words of 1 Bit Each
- Multiple Chip Enables
- 3-State Output
- High-Speed Operation

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

This 256-bit active-element memory is a monolithic CMOS array organized as 256 words of one bit each. It is fully decoded and has three gated chip-enable inputs to simplify decoding required to achieve the desired system organization. At least one chip enable input must be high whenever the address is changed to avoid erroneous alteration of stored data. The '4380A features a three-state output to facilitate word expansion.

write cycle

Information to be stored in the memory is written into the selected address location when all chip-enable inputs and the read/write input are low. While the read/write input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

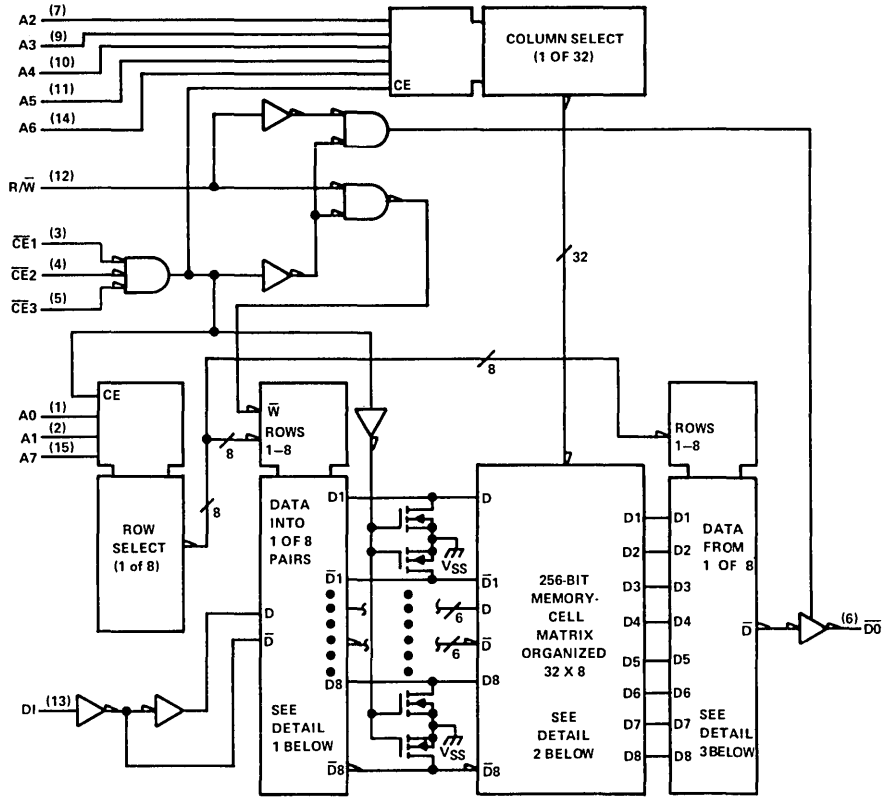
The complement of information applied at the data input during the wirte cycle is available at the output when the read/write input is high and the three chip-enable inputs are low. When any one of the chip-enable inputs is high, the output will be in the high-impedance state.

FUNCTION TABLE

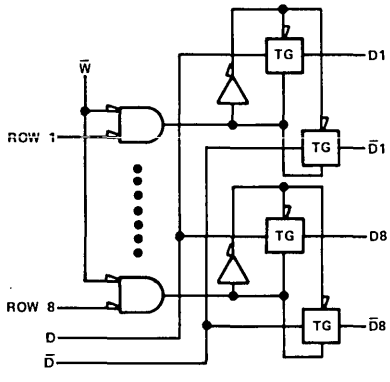
FUNCTION	INPUTS		OUTPUT
	CHIP ENABLE	READ/ WRITE	
Write	LLL	L	High Impedance
Read	LLL	H	Complement of Data Entered
Inhibit	HXX	X	High Impedance

H = high level, L = low level, X = irrelevant,
LLL = all $\overline{CE}$ inputs low,
HXX = one or more $\overline{CE}$ inputs high.

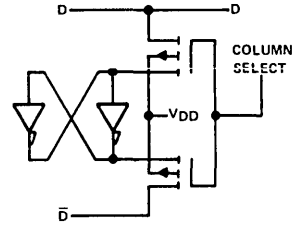
functional block diagram



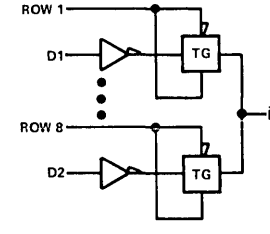
DETAIL 1
2 ROWS SHOWN OF 8



DETAIL 2
1 CELL SHOWN OF 256



DETAIL 3
2 ROWS SHOWN OF 8



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specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3 except as below

recommended operating conditions (see figures 1, 2, and 3)

		TF4380A				TP4380A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Write pulse width, $t_{w(wr)}$		*		*		*		*		ns
Setup time	Address before $\overline{CE}$ low, $t_{su(ad)}$	*		*		*		*		ns
	Data before end of write, $t_{su(da)}$	*		*		*		*		
	Read before $\overline{CE}$ low, $t_{su(rd)}$	*		*		*		*		
Hold time	Address after $\overline{CE}$ high, $t_{h(ad)}$	*		*		*		*		ns
	Data after end of write, $t_{h(da)}$	*		*		*		*		
	Read after $\overline{CE}$ high, $t_{h(rd)}$	*		*		*		*		

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4380A				TP4380A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	*		*		*		*		mA
			T_A = 25°C	*		*		*		*		
			T_A = MAX	*		*		*		*		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL}	T_A = MIN	*		*		*		*		mA
			T_A = 25°C	*		*		*		*		
			T_A = MAX	*		*		*		*		

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4380A				TP4380A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CE)}$	Access times from chip enable	C_L = 50 pF, R_L = 200 kΩ, See Figures 1 and 3 and Note 1		*		*		*		*	ns
t_{PXZ}	Output disable time			*		*		*		*	ns

*These specifications for this product have not been determined. It is planned to specify values where asterisks appear above.
NOTE 1: See load circuit on page 170.

PARAMETER MEASUREMENT INFORMATION

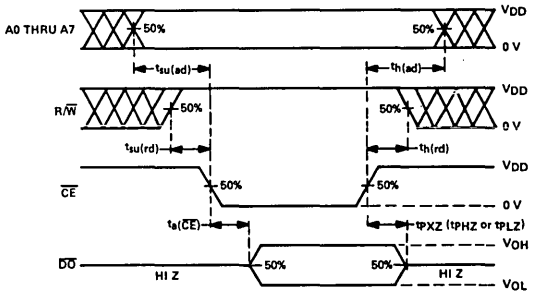

FIGURE 1–READ CYCLE VOLTAGE WAVEFORMS

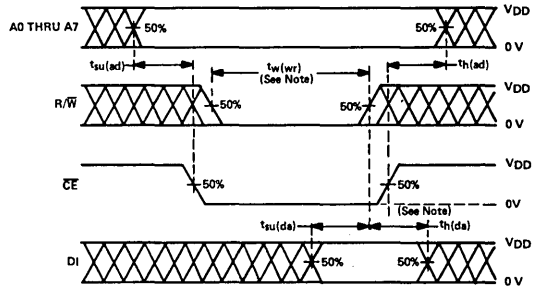

FIGURE 2–WIRTE CYCLE VOLTAGE WAVEFORMS

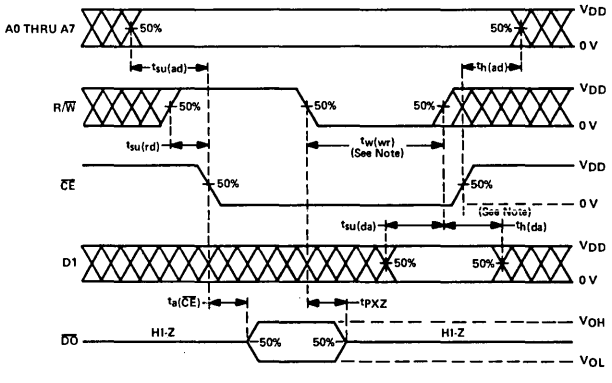

FIGURE 3–READ-WRITE (READ, MODIFY WRITE) CYCLE VOLTAGE WAVEFORMS

NOTE: The effective width of the write pulse is the interval in which R/$\overline{W}$ and $\overline{CE}$ are simultaneously low. The data setup and hold times are with respect to the low-to-high transition of either R/$\overline{W}$ or $\overline{CE}$, whichever occurs first.

TEXAS INSTRUMENTS
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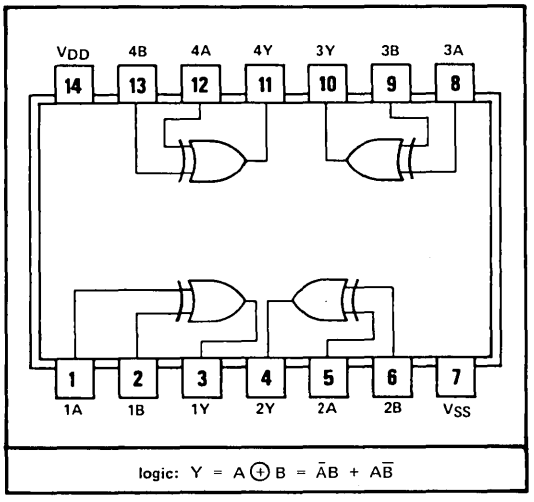
TYPES TF4507A, TP4507A
QUAD EXCLUSIVE-OR GATES

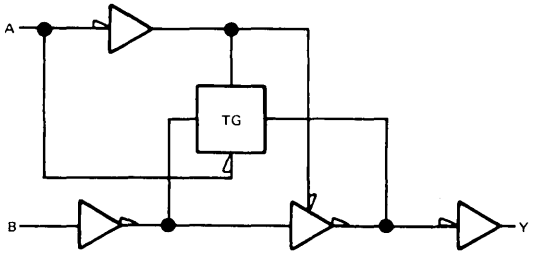
SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14507 and RCA CD4030A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



functional block diagram (each gate)

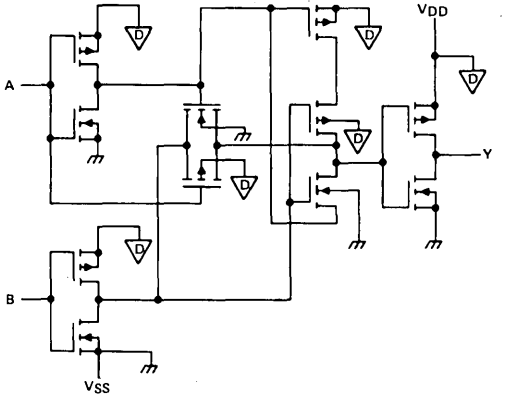


FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

H = high level, L = low level

schematic (each gate)



D . . . V_{DD} bus

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2, and on following page

electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS†		TF4507A				TP4507A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	High-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OH} min	T_A = MIN	−0.95		−0.95		−0.45		−0.45		mA
			T_A = 25°C	−0.65		−0.65		−0.32		−0.32		
			T_A = MAX	−0.45		−0.45		−0.25		−0.25		
I_{OL}	Low-level output current	V_{IH} = V_{DD}, V_{IL} = 0, V_O = V_{OL} max	T_A = MIN	0.75		1.5		0.35		0.7		mA
			T_A = 25°C	0.6		1.2		0.3		0.6		
			T_A = MAX	0.45		0.9		0.25		0.5		
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		0.5		1		5		10	μA
			T_A = MAX		30		60		70		140	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4507A		TP4507A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		3		30	μA
			T_A = MAX		180		420	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4507A				TP4507A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		350		175		475		250	ns
t_{PHL}	Propagation delay time, high-to-low-level output			350		175		475		250	ns
t_{TLH}	Transition time, low-to-high-level output			300		150		450		225	ns
t_{THL}	Transition time, high-to-low-level output			300		150		450		225	ns

§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14507 and RCA CD4030A.
NOTE 1: See load circuit and voltage waveforms on page 170.

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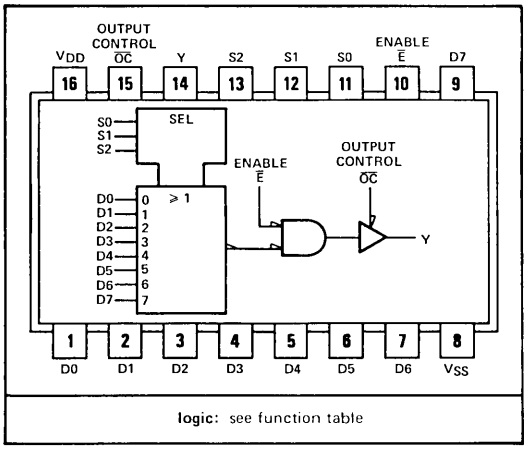
TYPES TF4512A, TP4512A
8-CHANNEL DATA SELECTORS WITH 3-STATE OUTPUTS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14512

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see function table

description

These circuits are single 8-channel data selectors having three digital select inputs, S0, S1, and S2, an enable input, $\overline{E}$, and an output control. When the output control, $\overline{OC}$, is high, the output will be in the high-impedance (off) state. Applications of this device include signal multiplexing, data routing, and number sequence generation.

FUNCTION TABLE

INPUTS					OUTPUT Y
OUTPUT CONTROL	ENABLE $\overline{E}$	SELECT S2	S1	S0	
H	X	X	X	X	Z
L	H	X	X	X	L
L	L	L	L	L	D0
L	L	L	L	H	D1
L	L	L	H	L	D2
L	L	L	H	H	D3
L	L	H	L	L	D4
L	L	H	L	H	D5
L	L	H	H	L	D6
L	L	H	H	H	D7

H = high level, L = low level, X = irrelevant, Z = high-impedance (off)
D0 . . . D7 = the logic level of the indicated D input.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3, and below

electrical characteristics

PARAMETER		TEST CONDITIONS†		TF4512A				TP4512A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{OC}$ at V_{DD}, $V_O = V_{DD}$	T_A = MIN or 25°C		0.05		0.1		0.5		1	μA
			T_A = MAX		3		6		7		14	
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{OC}$ at V_{DD}, V_O = 0 V	T_A = MIN or 25°C		−0.05		−0.1		−0.5		−1	μA
			T_A = MAX		−3		−6		−7		−14	

†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

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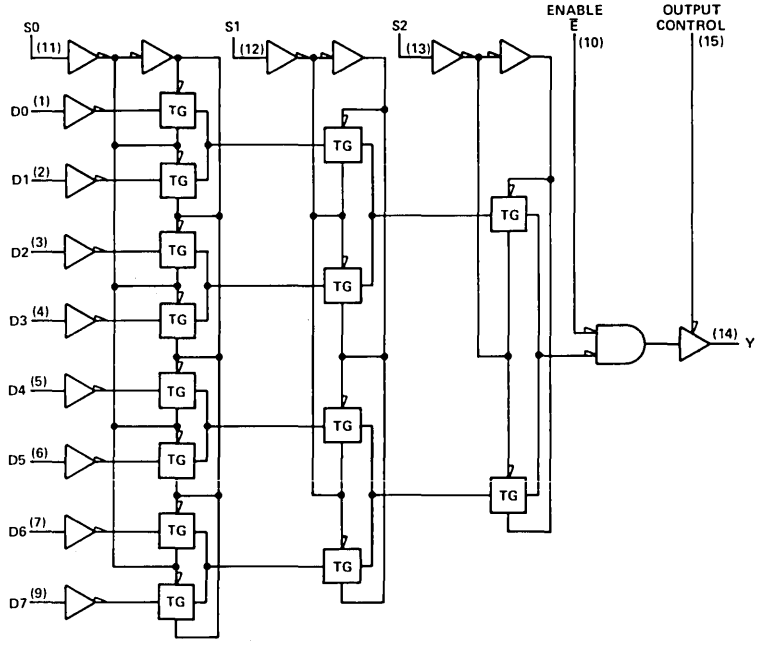
switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4512A				TP4512A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		750		325		1000		375	ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		325		1000		375	ns
t_{TLH}	Transition time, low-to-high-level output			500		250		600		300	ns
t_{THL}	Transition time, high-to-low-level output			500		250		600		300	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF¶, R_L = 10 kΩ, See Note 1		430		150		500		200	ns
t_{PZL}	Output enable time to low level			250		130		300		170	
t_{PHZ}	Output disable time from high level			260		170		320		240	ns
t_{PLZ}	Output disable time from low level			160		140		220		200	

§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14512.
¶With a 15-pF, 1-kΩ load, these devices switch with times similar to those of the Motorola MC14512.
NOTE 1: See load circuit and voltage waveforms on page 170.

functional block diagram



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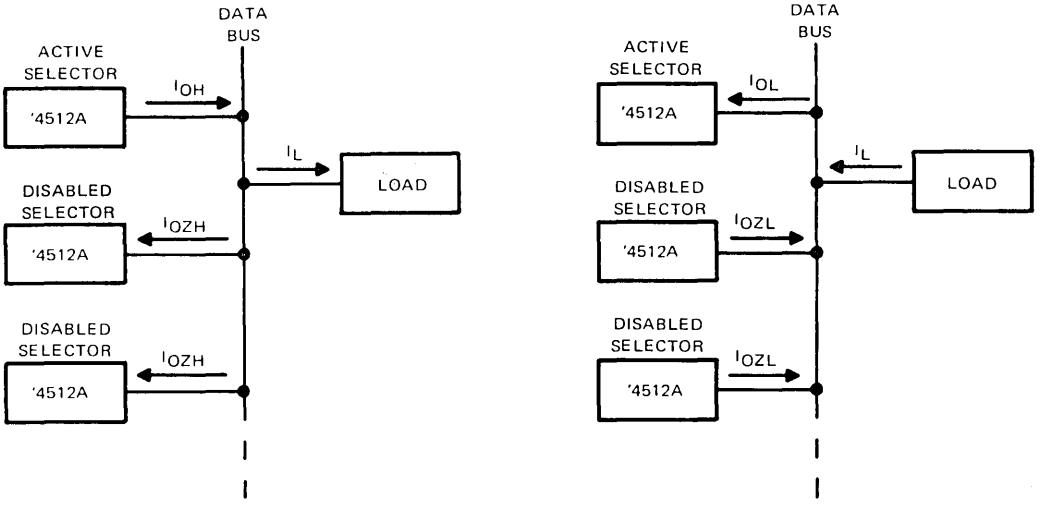
TYPICAL APPLICATION DATA

The output terminals of several '4512A 8-bit data selectors can be connected to a single data bus as shown. One output is placed in the active state (output control low) and the remaining outputs are disabled (output controls high). The number of outputs, N, that may be connected to a bus line is determined from the output drive current I_{OH} or I_{OL}, the off-state output current, I_{OZH} or I_{OZL}, and load current required to drive the bus line (including fan-out to other device inputs), I_L. N can be calculated for the high-level and low-level logic states, respectively, by:

$$N = \frac{I_{OH} - I_L}{I_{OZH}} + 1 \text{ and } N = \frac{I_{OL} - I_L}{I_{OZL}} + 1.$$



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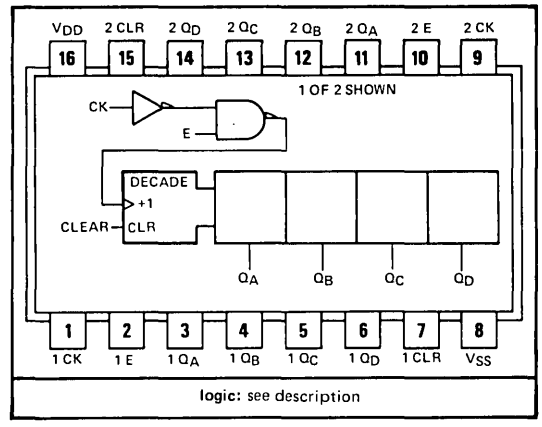
TYPES TF4518A, TP4518A
DUAL DECADE COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14518
- Medium-Speed Operation . . . 6 MHz Typical Maximum Clock Frequency at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

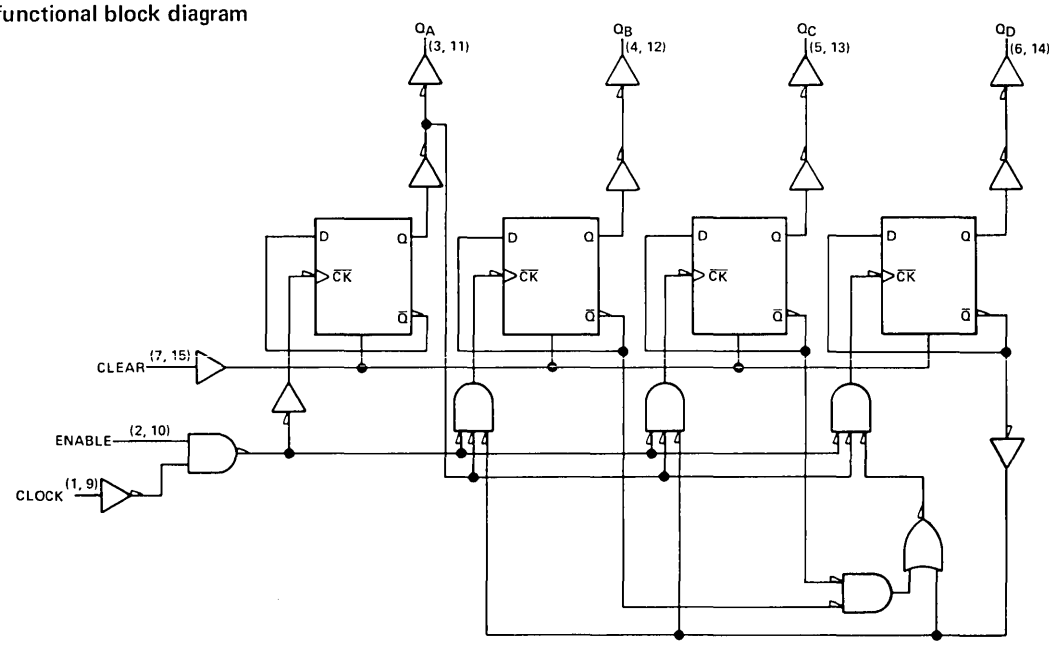
description

The '4518A dual decade counter consists of two identical, independent synchronous 4-stage counters. The counter stages are D-type flip-flops with interchangeable clock and enable lines. With enable high, the count is advanced on a low-to-high transition at the clock input. Alternatively, if the clock input is low, the count is advanced on a high-to-low transition at enable. If clock is high or enable is low, changes at the other input (enable or clock) have no effect. A high clear signal asynchronously clears the counters and resets all outputs low.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, group 3

functional block diagram



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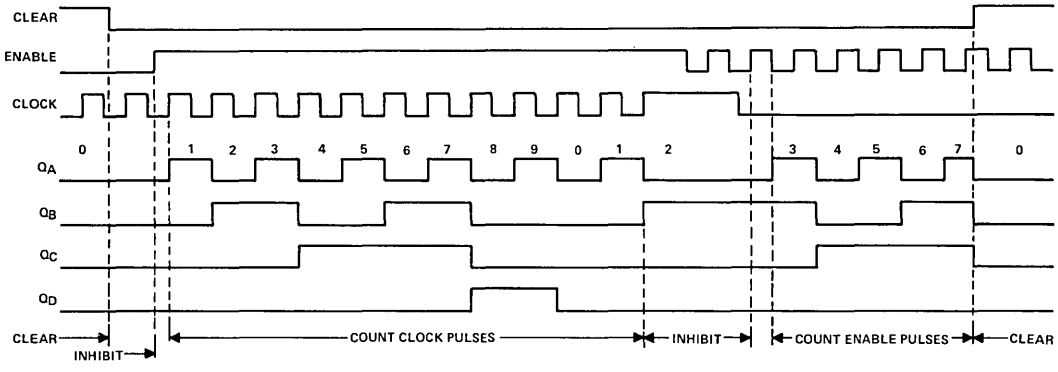
typical clear, count, and inhibit sequences



recommended operating conditions

		TF4518A				TP4518A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	200		100		300		120		ns
	Clear	325		100		500		125		ns
Enable setup time, t_{su}		440		220		660		260		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4518A				TP4518A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		3		1		2.5		MHz
t_{PLH} or t_{PHL}	Clock or enable	Any Q			825		300		1200		410	ns
t_{PHL}	Clear	All			825		300		1200		410	ns
t_{TLH} or t_{THL}		All			350		150		400		220	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14518.
NOTE 1: See load circuit and voltage waveforms on page 170.

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TYPES TF4519A, TP4519A
4-BIT AND-OR SELECT GATES

SEPTEMBER 1975

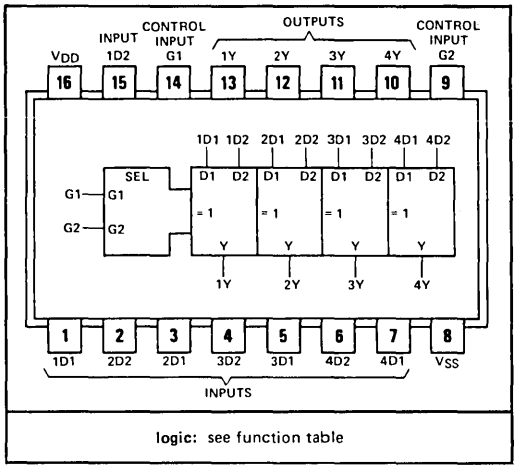
- Designed to be Interchangeable with Motorola MC14519

FUNCTION TABLE

INPUTS				OUTPUT
CONTROL		DATA		
G1	G2	D1	D2	Y
L	L	X	X	L
H	L	H	X	H
H	L	L	X	L
L	H	X	H	H
L	H	X	L	L
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

H = high level, L = low level, X = irrelevant

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

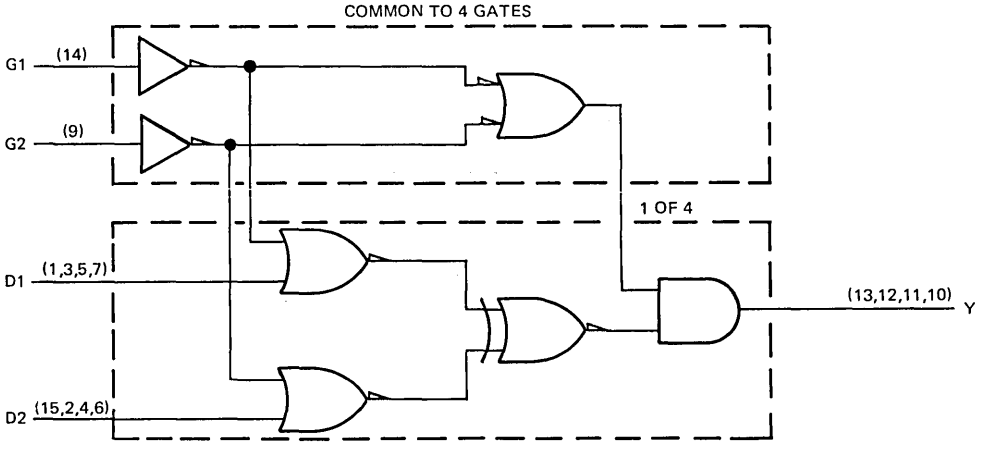


logic: see function table

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 2

functional block diagram



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electrical characteristics

V_{DD} = 5 V and 10 V

PARAMETER		TEST CONDITIONS		TF4519A				TP4519A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		0.5		1		5		10	μA
			T_A = MAX		30		60		150		300	

V_{DD} = 15 V

PARAMETER		TEST CONDITIONS†		TF4519A		TP4519A		UNIT
				MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$	Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		3		30	μA
			T_A = MAX		180		900	

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4519A				TP4519A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		450		225		600		300	ns
t_{PHL}	Propagation delay time, high-to-low-level output			450		225		600		300	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	ns

§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14519.
NOTE 1: See load circuit and voltage waveforms on page 170.

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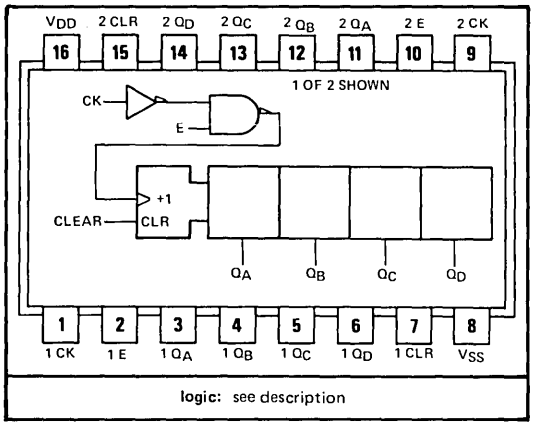
TYPES TF4520A, TP4520A
DUAL BINARY COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14520
- Medium-Speed Operation . . . 6 MHz Typical Maximum Clock Frequency at V_{DD} = 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

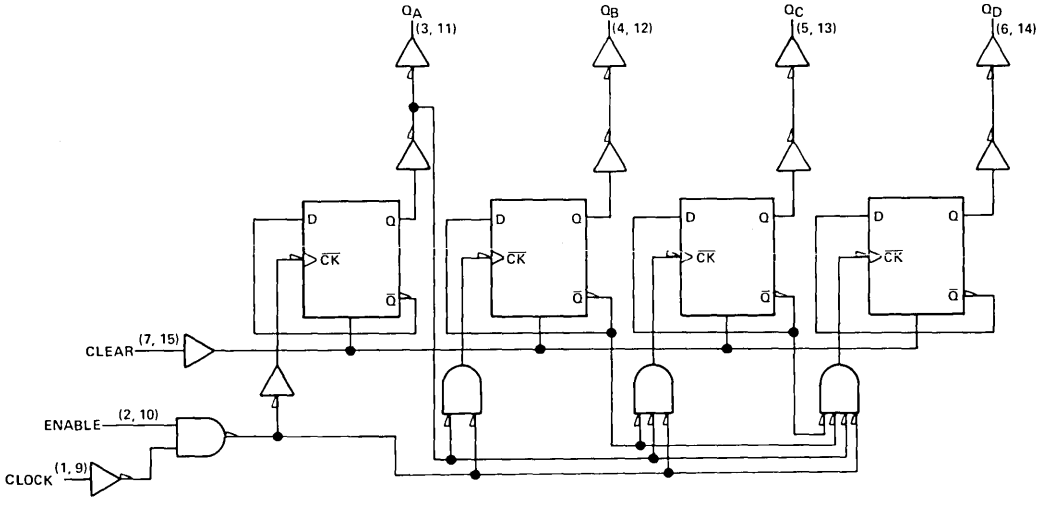
description

The '4520A dual binary counter consists of two identical, independent, synchronous 4-stage counters. The counter stages are D-type flip-flops with interchangeable clock and enable lines. With enable high, the count is advanced on a low-to-high transition at the clock input. Alternatively, if the clock input is low, the count is advanced on a high-to-low transition at enable. If clock is high or enable is low, changes at the other input (enable or clock) have no effect. A high clear signal asynchronously clears the counters and resets all outputs low.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and on following page	Page 63, group 3

functional block diagram



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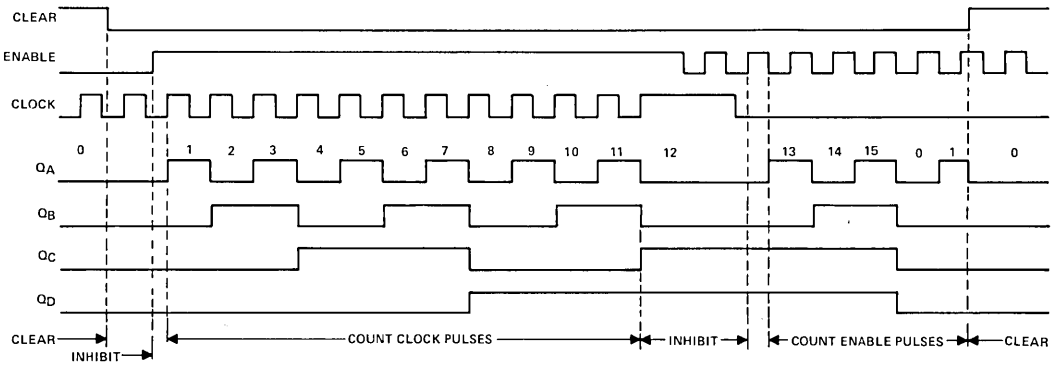
typical clear, count, and inhibit sequences



recommended operating conditions

		TF4520A				TP4520A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	200		100		300		120		ns
	Clear	325		100		500		125		ns
Enable setup time, t_{su}		440		220		660		260		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4520A				TP4520A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		3		1		2.5		MHz
t_{PLH} or t_{PHL}	Clock or enable	Any Q			825		300		1200		410	ns
t_{PHL}	Clear	All			825		300		1200		410	ns
t_{TLH} or t_{THL}		All			350		150		400		220	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14520.
NOTE 1: See load circuit and voltage waveforms on page 170.

175 PRINTED IN U.S.A.

TEXAS INSTRUMENTS
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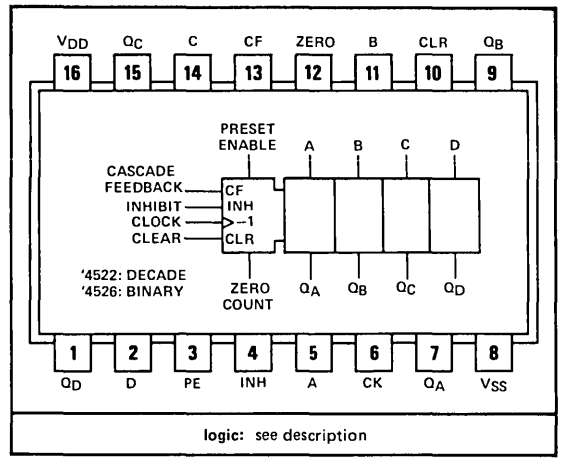
TYPES TF4522A, TF4526A, TP4522A, TP4526A
DECADE AND BINARY DIVIDE-BY-N COUNTERS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14522, MC14526
- Maximum Clock Frequency . . . 5 MHz Typical at 10 V

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The '4522A and '4526A are presettable decade and binary down counters with a decoded zero-state output for divide-by-N applications. While the counter is at minimum count (all outputs low), the zero-count output will be high if the cascade feedback input is high, otherwise, it remains low. The counters may be preset by taking preset enable (PE) high after setting up the desired data at the parallel inputs A, B, C, and D. Parallel loading is asynchronous and the clock input has no effect while PE is high. The count is decreased by 1 on the low-to-high transition of the clock but the clock signal is only effective if the inhibit input is low. Transitions of the inhibit input from high to low should be made while the clock is low in order to avoid causing one extra down count triggered by the inhibit transition. A high clear signal asynchronously clears the counter and resets all outputs low.

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62 and below	Page 63, group 3

Applications include frequency synthesizers, phase-locked loops, and other frequency-division applications.

recommended operating conditions

		TF4522A, TF4526A				TP4522A, TP4526A				UNIT
		V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Pulse width, t_w	Clock high or low	250		100		300		150		ns
	Preset enable	250		100		300		150		ns
	Clear	300		250		350		300		ns
Data hold time after preset enable		125		50		150		75		ns

switching characteristics at 25°C free-air temperature

PARAMETER‡	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TF4522A, TF4526A				TP4522A, TP4526A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 50 pF§, R_L = 200 kΩ, See Note 1	1.5		3		1		2.5		MHz
t_{PLH} or t_{PHL}	A, B, C, D	Q			1000		425		1300		550	ns
t_{PLH} or t_{PHL}	Clock	Zero-count			450		350		600		450	ns
t_{TLH} or t_{THL}		Any			500		250		600		300	ns

‡f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14522 and MC14526.
NOTE 1: See load circuit and voltage waveforms on page 170.

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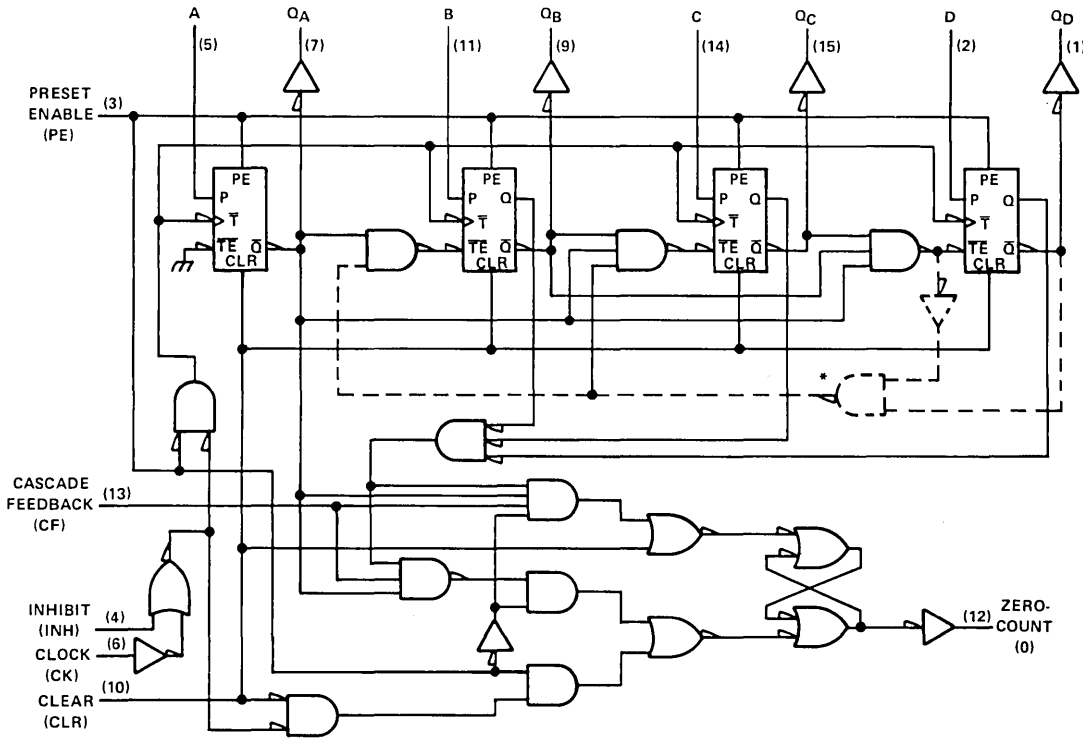
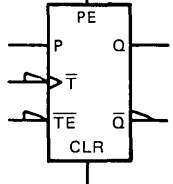
functional block diagram



*THE DOTTED LINES AND GATES ARE OMITTED ON THE '4526A

EACH FLIP-FLOP

SYMBOL



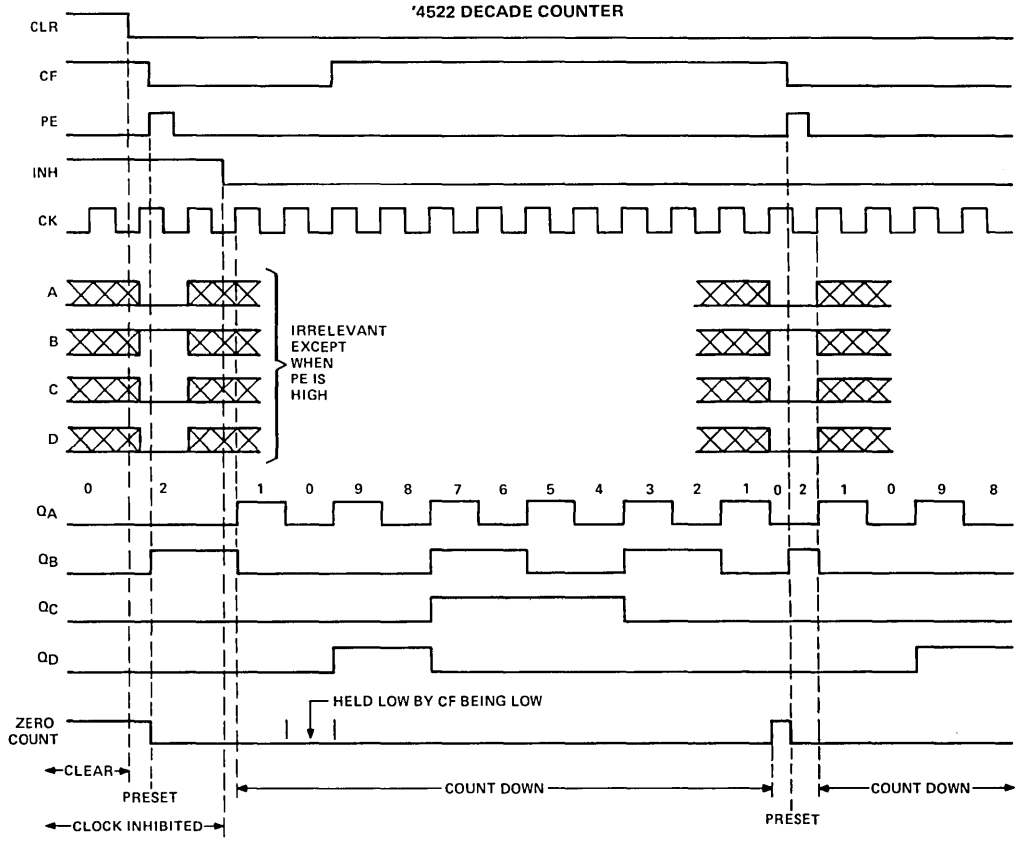
$\overline{TE}$ = toggle enable input
P = parallel date input
$\overline{T}$ = toggle input

FUNCTION TABLE
(NOT INCLUDING EXTERNAL GATING TO THE FLIP-FLOPS)

INPUTS					OUTPUTS	
CLR	PE	$\overline{TE}$	$\overline{T}$	P	Q	$\overline{Q}$
H	X	X	X	X	L	H
L	H	X	L	H	H	L
L	H	X	L	L	L	H
L	L	H	↓	X	Q_n	$\overline{Q}_n$
L	L	L	↓	X	$\overline{Q}_n$	Q_n
L	X	X	H	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
Q_n = the level of Q before the most-recent ↓ transition of $\overline{T}$.
Q_0 = the level of Q before the indicated steady-state conditions were established

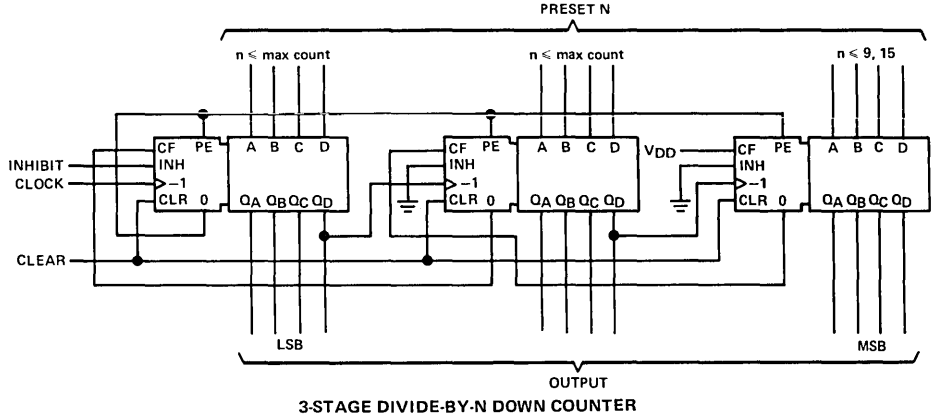
typical clear, asynchrously load, and count down sequence



CF has effect only during the zero count. It is shown changing as if driven by the zero output of a more significant bit in a divide-by-12 cascade.

A sequence for the '4526A binary counter would be similar except that 15 (HHHH) instead of 9 (HLLH) would follow 0 (LLLL), with counting down proceeding from there.

TYPICAL APPLICATION DATA



3-STAGE DIVIDE-BY-N DOWN COUNTER

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TYPES TF4531A, TP4531A
12-BIT PARITY TREES

SEPTEMBER 1975

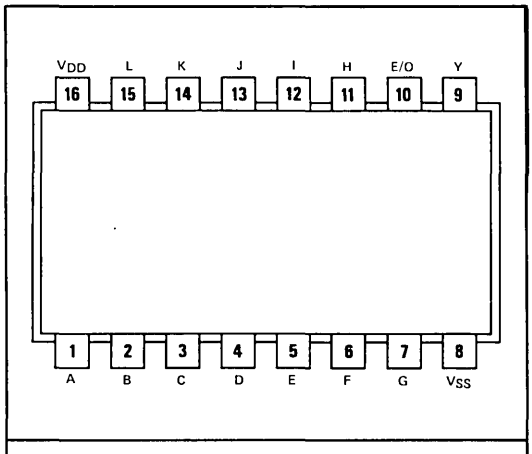
- Designed to be Interchangeable with Motorola MC14531

description

These circuits consist of 12 data-bit inputs (A thru L), an even or odd parity selection input (E/O) and an output. The parity selection input can be considered as an additional bit. With an even number of inputs (including E/O) high, the output is low; with an odd number high, the output is high. Words of greater than 12 bits can be accomodated by cascading other '4351A devices by using the E/O input.

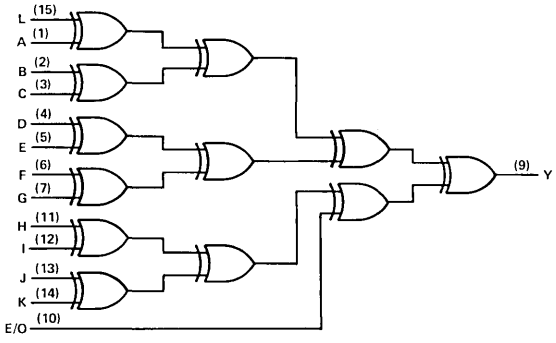
Applications include checking or including a redundant (parity) bit of a word for error detection/correction systems, controlling remote digital sensors or switches (digital event detection/correction), or use as a multiple input adder without carries.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

functional block diagram



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3

switching characteristics at 25°C free-air temperature

PARAMETER‡		TEST CONDITIONS	TF4531A				TP4531A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} or t_{PHL}	from A-L	C_L = 50 pF§,		1050		425		1500		635	ns
	from E/O	R_L = 200 kΩ,		675		275		950		410	
t_{TLH} or t_{THL}		See Note 1		350		150		400		220	ns

‡t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14531.
NOTE 1: See load circuit and voltage waveforms on page 170.

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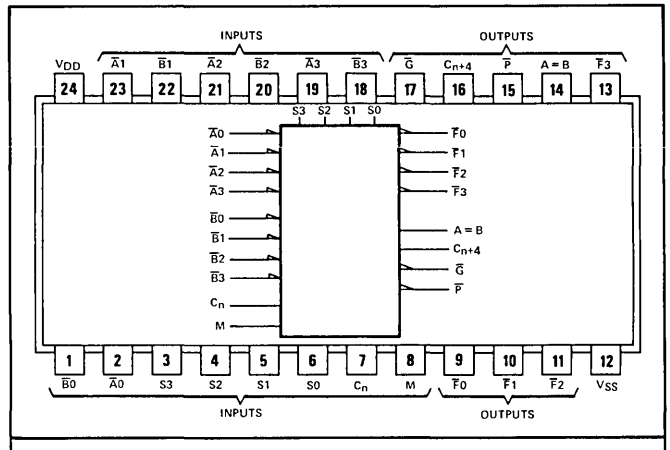
TYPES TF4581A, TP4581A
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14581
- All Outputs Buffered
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see tables 1 and 2

description

The TF4581A and TP4581A are arithmetic logic units (ALU)/function generators that have a complexity of 89 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the TF4582A or TP4582A full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading '4582 circuits and these ALU's to provide multi-level full carry look ahead is illustrated under typical applications data for the '4582A.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The '4581A will accommodate active-low or active-high data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	P	G

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1, which requires an end-around or forced carry to provide A−B.

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description (continued)

The '4581A can also be utilized as a comparator. The A = B output is internally decoded from the function outputs ($\overline{F}0$, $\overline{F}1$, $\overline{F}2$, $\overline{F}3$) so that when two words of equal magnitude are applied at the $\overline{A}$ and $\overline{B}$ inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	$A \geqslant B$	$A \leqslant B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leqslant B$	$A \geqslant B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

signal designations

The '4581A and '4582A can be used with the signal designations of either Figure 1 or Figure 2. The polarity indicators (▷) and the bars over the terminal letter symbols (e.g., $\overline{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\overline{C}$ means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2. Because the terminals have been renamed between Figures 1 and 2, the equations in both tables are actually in positive logic. For negative logic, the equations in Table 1 may be used with the terminal nomenclature of Figure 2 or the equations of Table 2 may be used with the terminal nomenclature of Figure 1.

signal designations (continued)

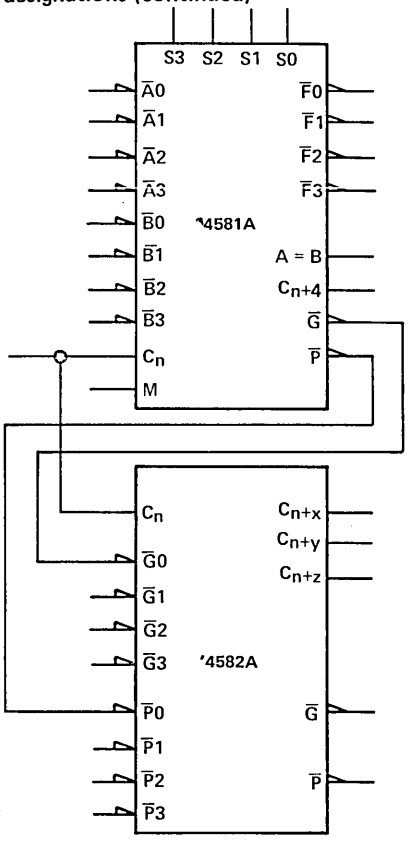


FIGURE 1
(Use with Table 1 for positive logic, with Table 2 for negative logic)

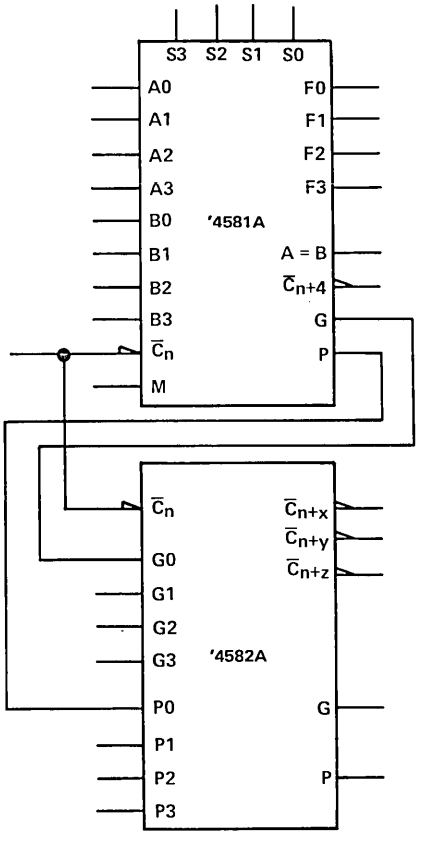


FIGURE 2
(Use with Table 2 for positive logic, with Table 1 for negative logic)

TABLE 1

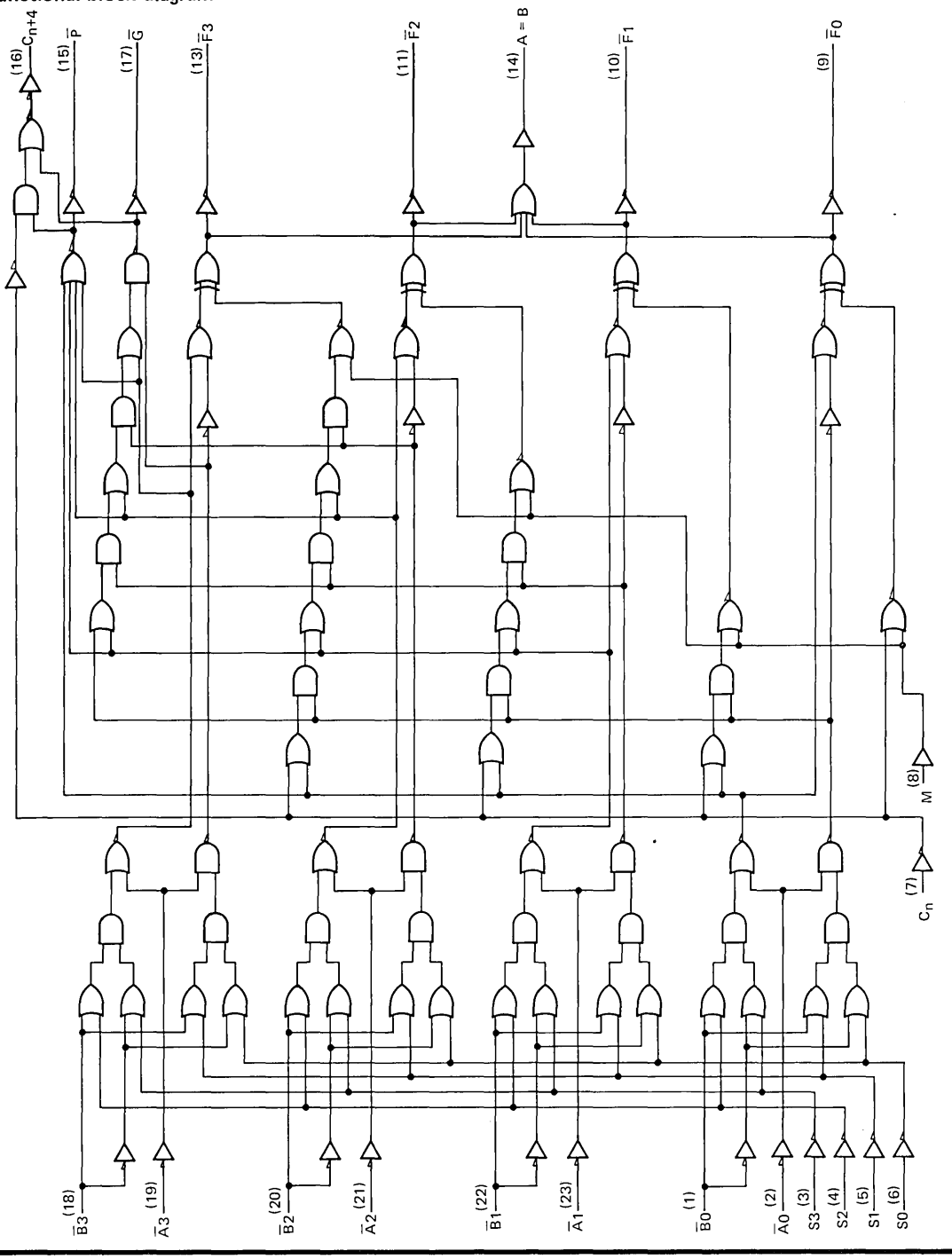
SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = $A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{AB}$	F = A PLUS $A\overline{B}$	F = A PLUS $A\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS $A\overline{B}$	F = (A + B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = $A\overline{B}$	F = $A\overline{B}$ MINUS 1	F = $A\overline{B}$
H	L	L	L	F = A + $\overline{B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

functional block diagram



specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3

switching characteristics at $T_A = 25°C$, $C_L = 50$ pF§, $R_L = 200$ kΩ (See Note 1)

PARAMETER‡	FROM	TO	MODE¶	TF4581A				TP4581A				UNIT
				V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} or t_{PHL}	Sum In ($\overline{A}$0)	Sum Out (Any $\overline{F}$)	Add		1200		425		2200		810	ns
t_{PLH} or t_{PHL}	Sum In ($\overline{A}$0)	$\overline{P}$	Add		825		300		1500		560	ns
t_{PLH} or t_{PHL}	Sum In ($\overline{B}$0)	$\overline{G}$	Add		825		300		1500		560	ns
t_{PLH} or t_{PHL}	Sum In ($\overline{B}$0)	C_{n+4}	Add		1200		425		1900		710	ns
t_{PLH} or t_{PHL}	C_n	Sum Out (Any $\overline{F}$)	Add		625		235		1200		460	ns
t_{PLH} or t_{PHL}	C_n	C_{n+4}	Add		550		210		950		380	ns
t_{PLH} or t_{PHL}	Sum In ($\overline{A}$0)	A = B	Sub		1700		575		3200		1100	ns
t_{PLH} or t_{PHL}	Sum In (All $\overline{B}$)	Sum Out (Any $\overline{F}$)	Exclusive OR		1200		425		1900		710	ns
t_{TLH} or t_{THL}		Any	Any		350		150		400		220	ns

TEST SETUP TABLE

FROM	TO	MODE¶	CONNECTION OF OTHER INPUTS	
			To V_{SS}	To V_{DD}
Sum In ($\overline{A}$0)	Sum Out (Any $\overline{F}$)	Add	Remaining $\overline{A}$, C_n	All $\overline{B}$
Sum In ($\overline{A}$0)	$\overline{P}$	Add	Remaining $\overline{A}$, C_n	All $\overline{B}$
Sum In ($\overline{B}$0)	$\overline{G}$	Add	All $\overline{A}$, C_n	Remaining $\overline{B}$
Sum In ($\overline{B}$0)	C_{n+4}	Add	All $\overline{A}$, C_n	Remaining $\overline{B}$
C_n	Sum Out (Any $\overline{F}$)	Add	All $\overline{A}$	All $\overline{B}$
C_n	C_{n+4}	Add	All $\overline{A}$	All $\overline{B}$
Sum In ($\overline{A}$0)	A = B	Sub	All $\overline{B}$, Remaining A	C_n
Sum In (All $\overline{B}$)	Sum Out (Any $\overline{F}$)	Exclusive OR	All $\overline{A}$	M

‡t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{TLH} ≡ Transition time, low-to-high-level output
t_{THL} ≡ Transition time, high-to-low-level output
§With a 15-pF load, these devices switch with times similar to those of Motorola MC14581.
¶For Add mode: M = 0 V, S3 = V_{DD}, S2 = 0 V, S1 = 0 V, S0 = V_{DD}
For Subtract mode: M = 0 V, S3 = 0 V, S2 = V_{DD}, S1 = V_{DD}, S0 = 0 V
Exclusive-OR mode: M = V_{DD}, S3 = V_{DD}, S2 = 0 V, S1 = 0 V, S0 = V_{DD}
NOTE 1: See load circuit and voltage waveforms on page 170.

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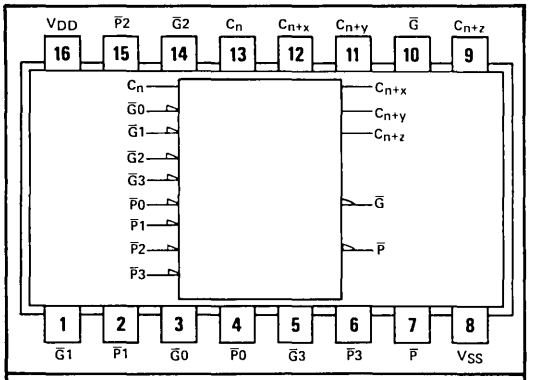
TYPES TF4582A, TP4582A
LOOK-AHEAD CARRY GENERATORS

SEPTEMBER 1975

- Designed to be Interchangeable with Motorola MC14582
- Expandable to Any Number of Bits
- Buffered Inputs and Outputs

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The TF4582A and TP4582A are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the function tables.

When used in conjunction with the '4581A arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '4582A generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '4582A circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and outputs of the '4581A ALU are in their true form and the carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions explained on the '4581A data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the '4582A are:

$$Cn+x = G0 + P0Cn$$
$$Cn+y = G1 + G0P1 + P1P0Cn$$
$$Cn+z = G2 + G1P2 + G0P2P1 + P2P1P0Cn$$
$$\overline{G} = \overline{G3 + G2P3 + G1P3P2 + G0P3P2P1}$$
$$\overline{P} = \overline{P3P2P1P0}$$

specifications

MAXIMUM RATINGS	RECOMMENDED OPERATING CONDITIONS	ELECTRICAL CHARACTERISTICS
Page 62	Page 62	Page 63, group 3, except as on page 169

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TYPES TF4582A, TP4582A
LOOK-AHEAD CARRY GENERATORS

FUNCTION TABLE
FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE
FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE
FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+z} OUTPUT

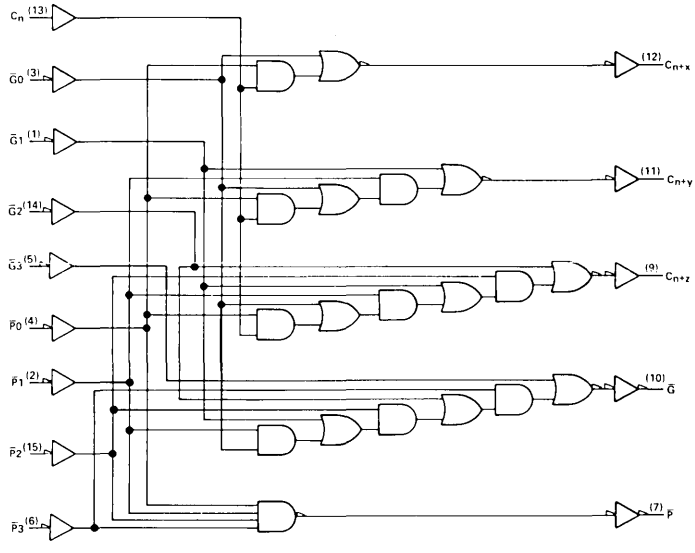
INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

functional block diagram



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electrical characteristics

V_{DD} = 5 and 10 V

PARAMETER	TEST CONDITIONS†		TF4582A				TP4582A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$ Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		0.5		1		5		10	µA
		T_A = MAX		30		60		150		300	

V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TF4582A		TP4582A		UNIT
			MIN	MAX	MIN	MAX	
I_{DD} or $-I_{SS}$ Quiescent supply current	V_I = V_{DD} or 0, No load	T_A = MIN or 25°C		3		30	µA
		T_A = MAX		180		900	

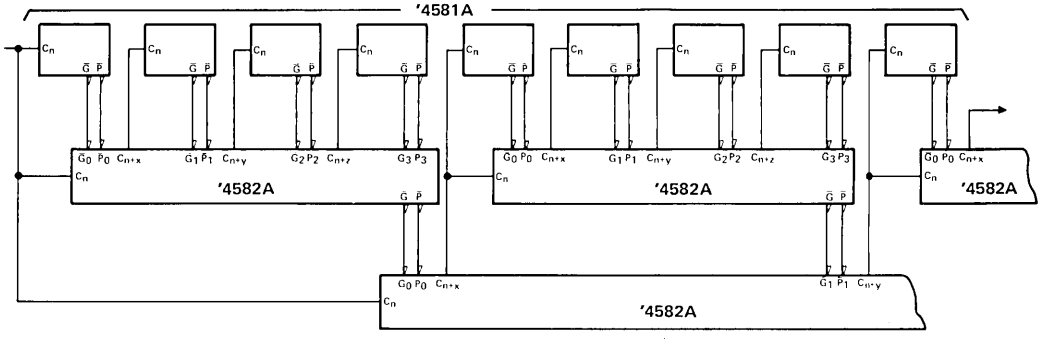
†T_A = MIN or MAX refers to the respective values of temperature specified under recommended operating conditions.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TF4582A				TP4582A				UNIT
			V_{DD} = 5 V		V_{DD} = 10 V		V_{DD} = 5 V		V_{DD} = 10 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF§, R_L = 200 kΩ, See Note 1		550		225		950		410	ns
t_{PHL}	Propagation delay time, high-to-low-level output			550		225		950		410	ns
t_{TLH}	Transition time, low-to-high-level output			350		150		400		220	ns
t_{THL}	Transition time, high-to-low-level output			350		150		400		220	ns

§With a 15-pF load, these devices switch with times similar to those of the Motorola MC14582.
NOTE 1: See load circuit and voltage waveforms on page 170.

TYPICAL APPLICATION DATA



$\bar{A}$ and $\bar{B}$ inputs and $\bar{F}$ outputs of '4581A are not shown.

64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

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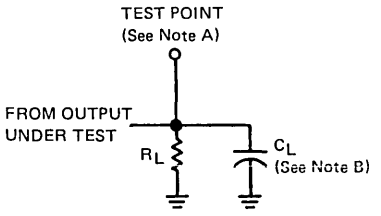
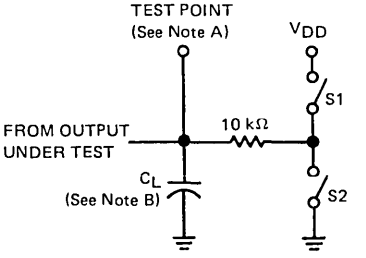
PARAMETER MEASUREMENT INFORMATION

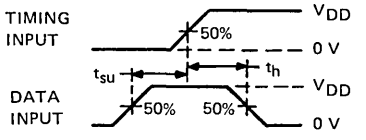


LOAD CIRCUIT FOR PROPAGATION DELAY AND TRANSITION TIMES

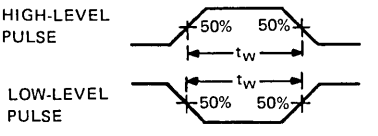


LOAD CIRCUIT FOR ENABLE AND DISABLE TIMES OF THREE-STATE OUTPUTS

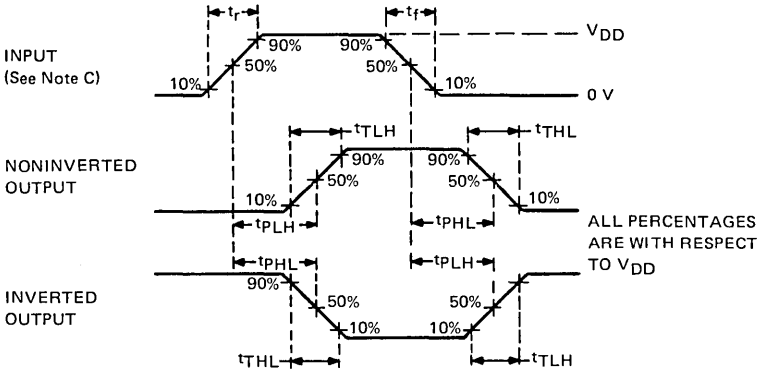
NOTES: A. The waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 1$ MΩ.
B. C_L includes probe and jig capacitance.



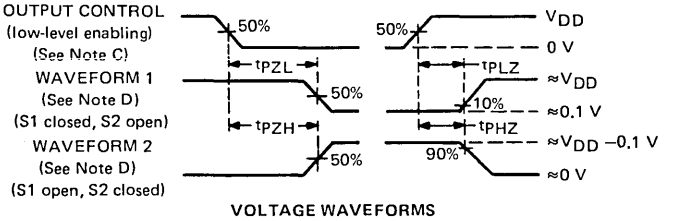
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY AND TRANSITION TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES: C. Input pulse is supplied by a generator having the following characteristics: $Z_{out} = 50\ \Omega$, PRR = 10 kHz, $t_r \leq 20$ ns, $t_f \leq 20$ ns.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

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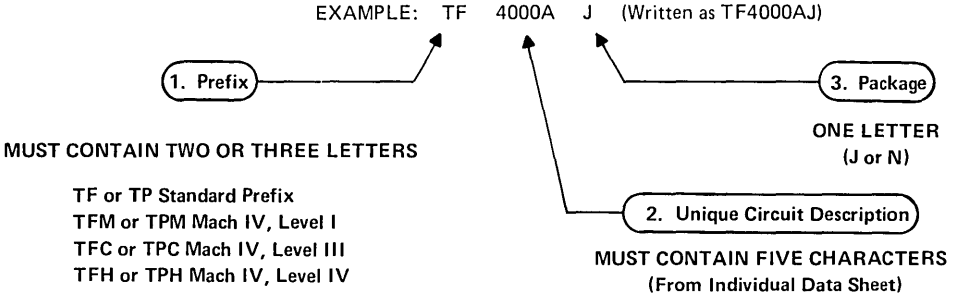
CMOS ORDERING INSTRUCTIONS AND MECHANICAL DATA

general

All CMOS circuits in this book are available in the ceramic dual-in-line package (outline J). Circuits with type number prefix TP are also available in the plastic dual-in-line package (outline N). Factory orders for these circuits should include a three-part type number as explained in the following example.

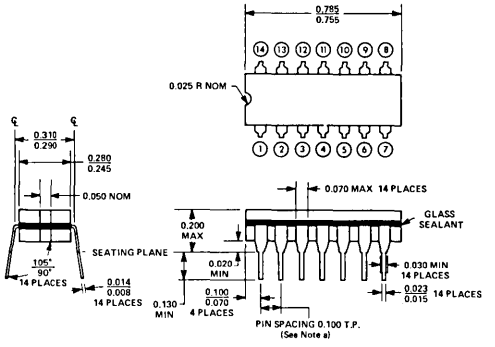


CMOS ORDERING INSTRUCTIONS AND MECHANICAL DATA

J ceramic dual-in-line packages (inch dimensions, see page 174 for metric dimensions)

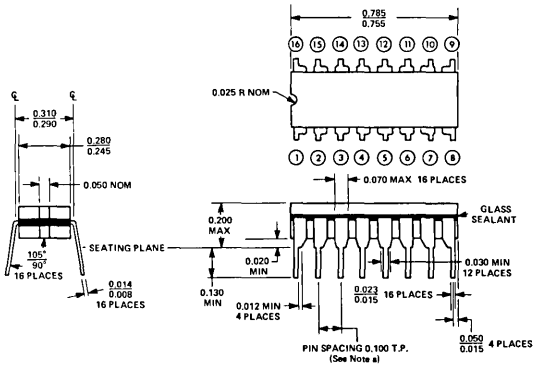
These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC
(INCH)

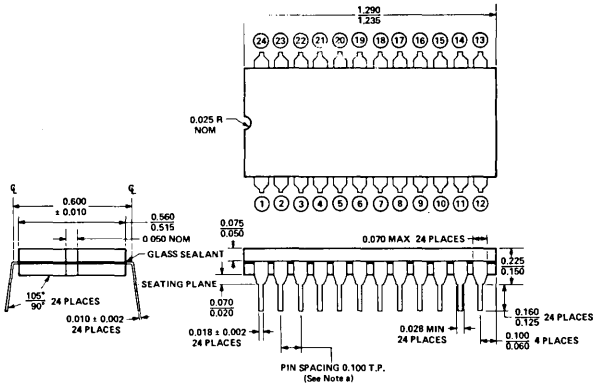


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC
(INCH)

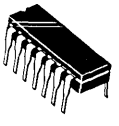


24-PIN J CERAMIC
(INCH)

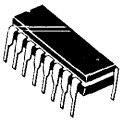


Falls Within JEDEC MO-015AA Dimensions

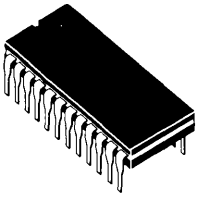
NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



14-PIN



16-PIN



24-PIN

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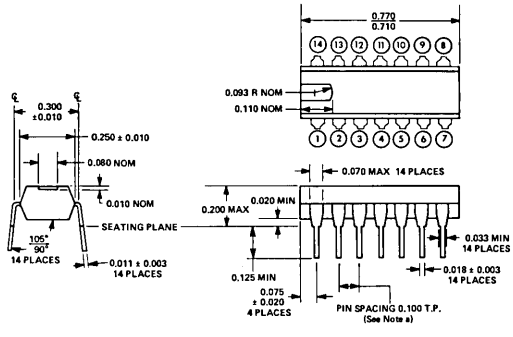
N plastic dual-in-line packages (inch dimensions, see page 175 for metric dimensions)

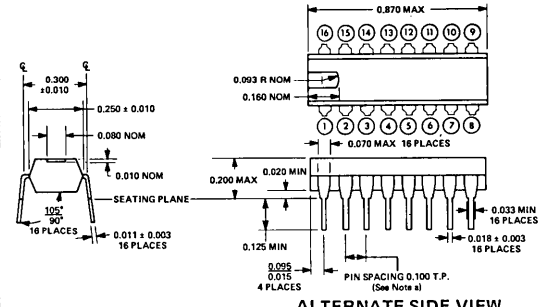
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300-inch or 0.600-inch centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC (INCH)



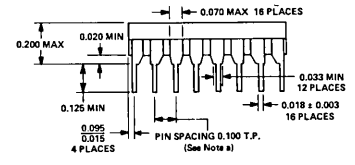
Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN N PLASTIC (INCH)

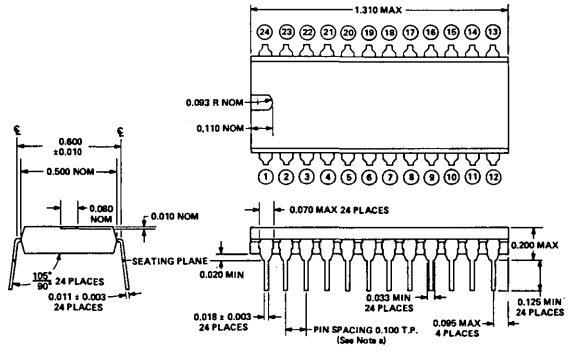


Package configuration of 16-pin N package (see alternative side-views) is at the option of TI.

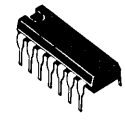
ALTERNATE SIDE VIEW



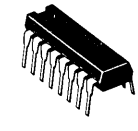
24-PIN N PLASTIC (INCH)



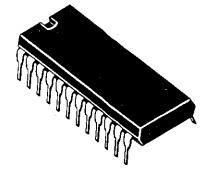
NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



14-PIN



16-PIN

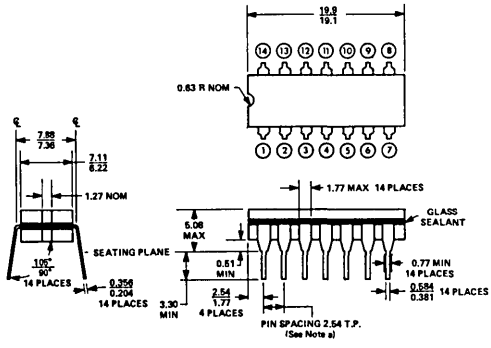


24-PIN

J ceramic dual-in-line packages (metric dimensions, see page 172 for inch dimensions)

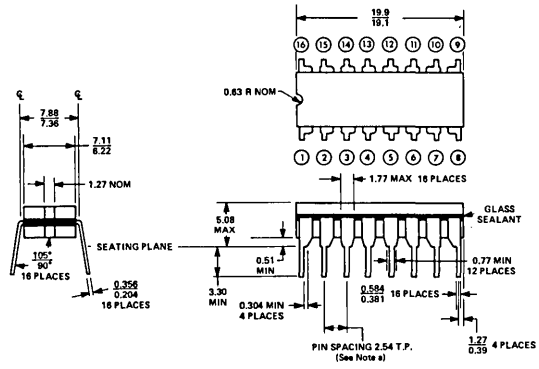
These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The packages are intended for insertion in mounting-hole rows on 7.62-mm or 15.24-mm centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC (METRIC)

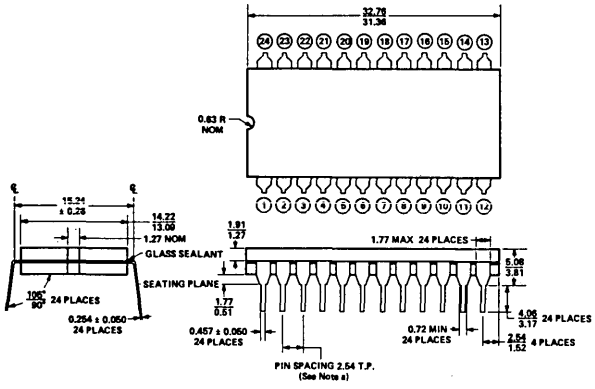


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC (METRIC)



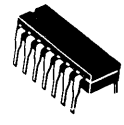
24-PIN J CERAMIC (METRIC)



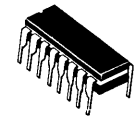
Falls Within JEDEC MO-015AA Dimensions

NOTES: a. Each pin centerline is located within 0.26 mm of its true longitudinal position.

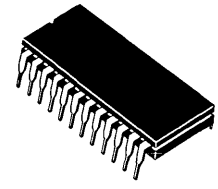
b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.



14-PIN



16-PIN



24-PIN

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N plastic dual-in-line packages (metric dimensions, see page 173 for inch dimensions)

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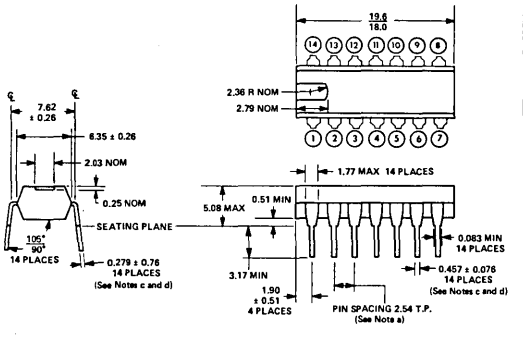
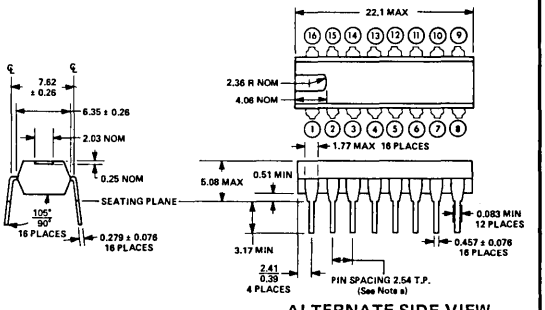
14-PIN N PLASTIC (METRIC)



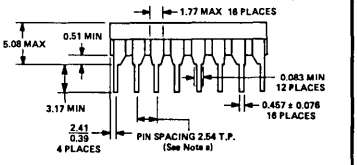
Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN N PLASTIC (METRIC)

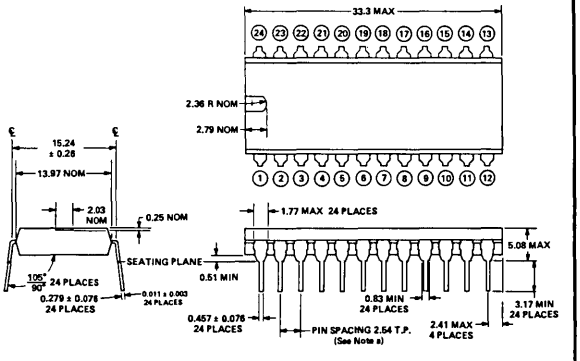


Package configuration of 16-pin N package (see alternative side-views) is at the option of TI.

ALTERNATE SIDE VIEW

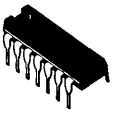


24-PIN N PLASTIC (METRIC)

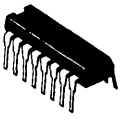


NOTES: a. Each pin centerline is located within 0.26 mm of its true longitudinal position.

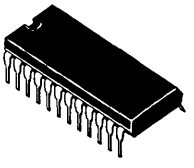
b. All dimensions are in millimeters unless otherwise noted. These dimensions are for reference only. Inch dimensions govern.



14-PIN



16-PIN



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