MOS/LSI Circuits

CONTENTS

TEXAS INSTRUMENTS
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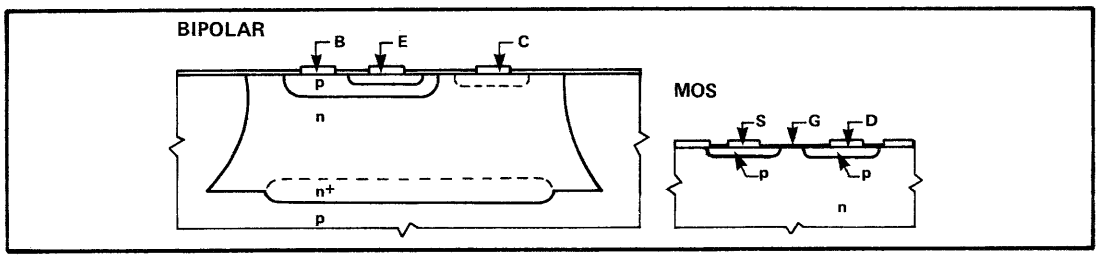
CONTENTS

MOS . . . . . an innovative technology

Many types of equipment previously not suitable for electronic control can now take full advantage of the latest electronics technology. Equipment costs can be kept low, and equipment size can be reduced easily. MOS (Metal Oxide Semiconductor) circuits are ideal for digital applications including timers and counters, data transmission and switching equipment, recorders, calculators, controls and computer equipment. MOS is also suitable for analog applications such as telemetry and test equipment.

MOS technology can be applied to hundreds of equipment types at costs usually lower than for other technologies with significant improvements in reliability.

The introduction of MOS/LSI into new classes of equipments is possible because the basic MOS device combines the best attributes of the pentode vacuum tube with all the advantages of the transistor. MOS devices have high-input impedance, they are small, simple to fabricate, and consume little power; consequently they offer the highest complexity of large-scale-integrated circuits.



COMPARISON OF TRANSISTOR CROSS SECTIONS

WHAT IS MOS?

MOS ICs require only one-third of the process steps needed for the standard double-diffused bipolar IC. But the most significant feature is the large number of semiconductor circuit elements that can be put on a small chip. This high circuit density means large-scale integration, and permits TI to put up to 5000 devices on a silicon chip only 150- x 150-mils square. Each transistor in the MOS/LSI array requires as little as 1 square mil of chip area – a great reduction over the bipolar transistors requiring 49 to 50 square mils.

Inherent advantages of MOS/LSI include:

- increased circuit complexity per package
- lower cost per circuit function
- fewer subsystems to test
- fewer parts to assemble and inspect
- lower power-drain per function
- a choice of standard or custom products

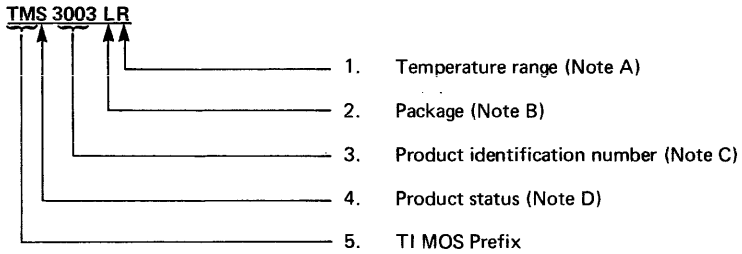
From the design standpoint, MOS/LSI is a two-dimensional layout rather than three dimensional. Mathematically its operation can be predicted, and mathematical models lend themselves to Computer-Aided Design analysis. Therefore the circuit can be laid out and its operation checked before it is built.

MOS/LSI NUMBERING SYSTEM

TEXAS INSTRUMENTS MOS/LSI DEVICE NUMBERING SYSTEM

Electrical characteristics presented in this catalog, unless otherwise noted, apply for circuit type(s) listed in the page heading, regardless of package. Factory orders for circuits described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM



NOTE A **Temperature Range**

C	−25°C to +85°C (commercial)
M	−55°C to +125°C (military)
R	−55°C to +85°C (reduced military)
S	Special range (as designated by customer)

NOTE B **Package**

F	Flat package
J	Ceramic dual-in-line
N	Plastic dual-in-line
L	Plug-in package
U	Unencapsulated (beam lead, etc.)

NOTE C **Product Identification Number**

Part number unique to each device type

NOTE D **Product Status**

S	Standard devices
X	Prototype or experimental
C	Custom design
T	High reliability

Because of the high complexity of MOS/LSI, TI has had to innovate in the packaging area. The packages selected by TI are standards of the industry. Accessories for these packages are readily available.

All standard MOS/LSI devices supplied in ceramic dual-in-line packages and most of those mounted in plug-in-type packages are now available in plastic.

1) Dual-in-line package

a) Pin-to-pin spacing

A pin-to-pin spacing of 100 mils has been selected for all dual-in-line packages.

b) Row-to-row spacing

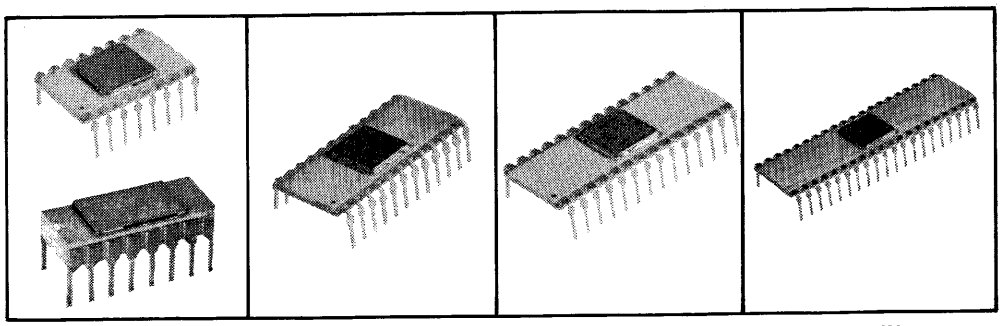
Two spacings are used for mounting-hole rows — 300 mils and 600 mils

c) Ceramic package types

TI uses several hermetically sealed ceramic dual-in-line packages, which consist of a ceramic base, gold-plated cap and gold-plated leads.

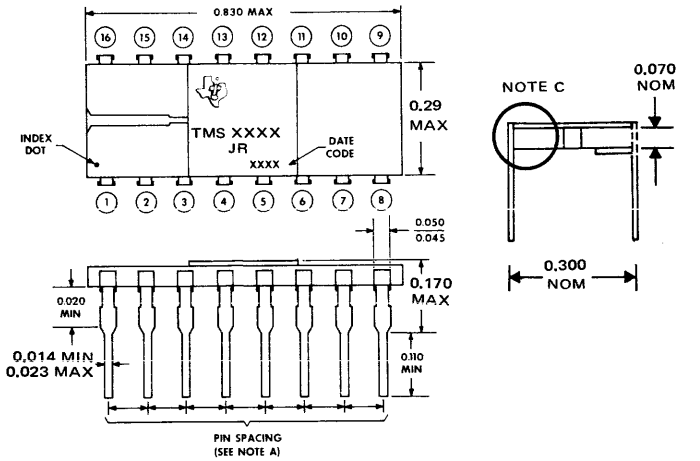
The following packages are presently in use:

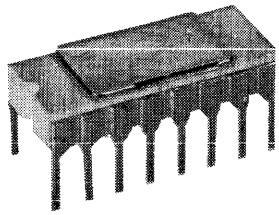
	16 PIN	24 PIN	26 PIN	40 PIN
300 MILS BETWEEN ROWS	X			
600 MILS BETWEEN ROWS	X	X	X	X



16 PIN | 24 PIN | 28 PIN | 40 PIN

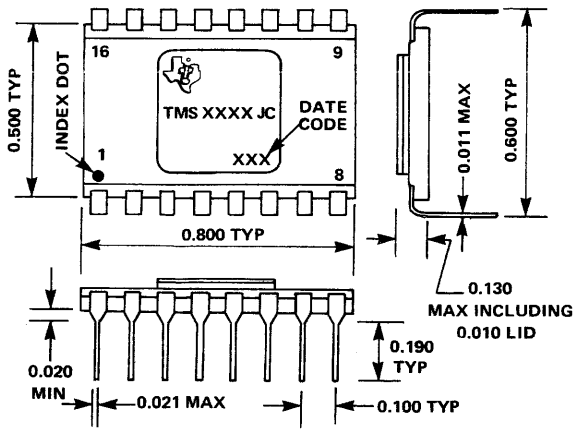
16-pin package (300-mil row spacing)

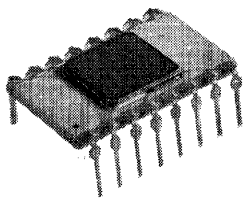




A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.
C. LEADS MAY BE BRAZED TO SIDES OR BOTTOM OF PACKAGE

16-pin package (600-mil row spacing)





NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located with ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions are in inches.

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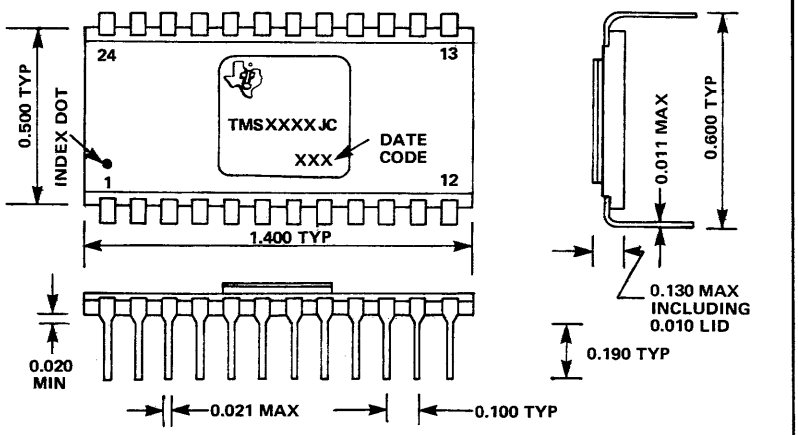
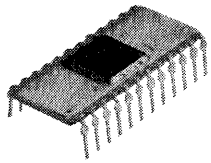
24-pin package

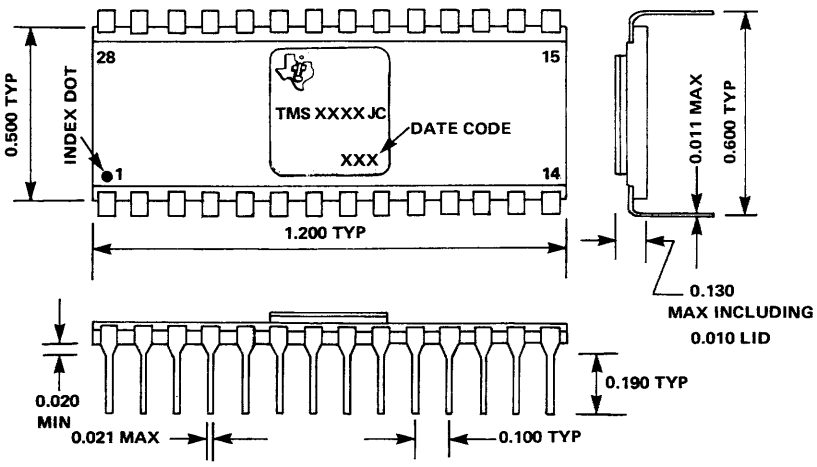


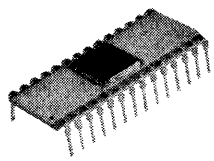


NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.

B. All dimensions are in inches.

28-pin package





NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 28.

B. All dimensions are in inches.

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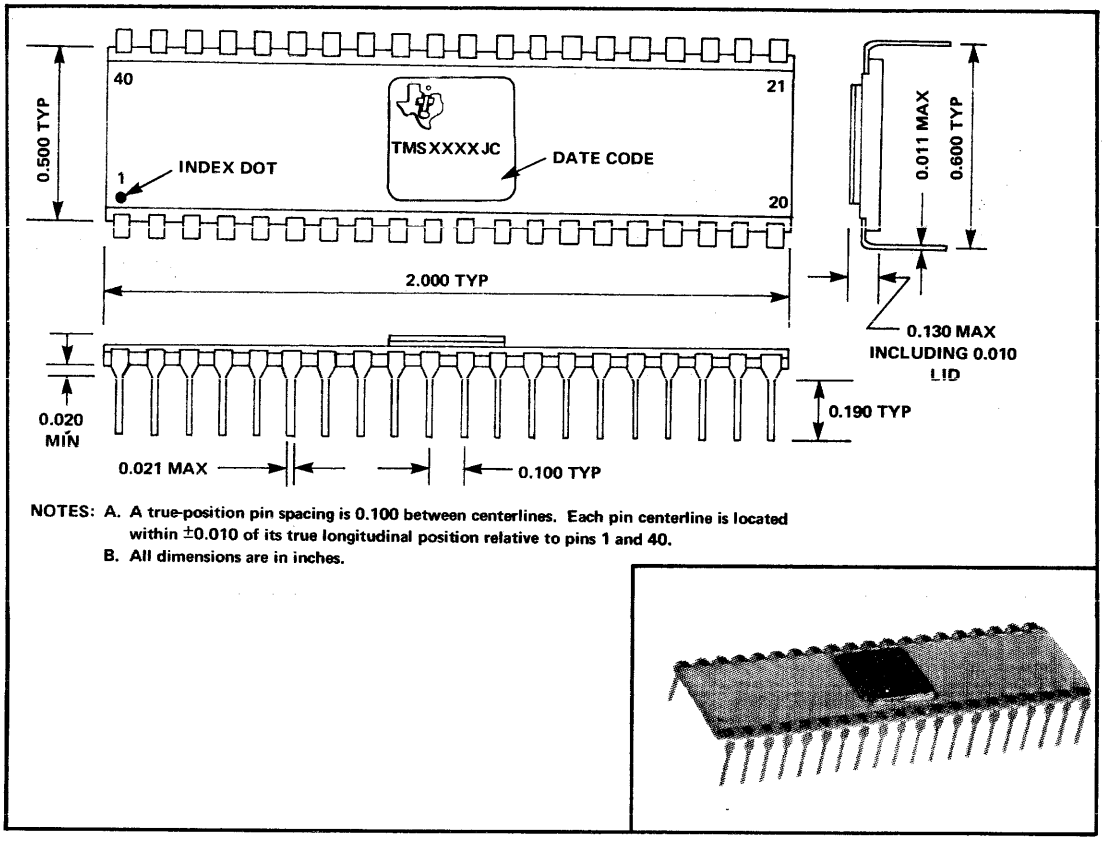
40-pin package



NOTES: A. A true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches.

d) Plastic packages

Over the last two years TI has developed methods of plastic encapsulation specially adapted to MOS/LSI circuits. A proprietary plastic compound and proprietary methods are employed to ensure a level of reliability comparable to that of hermetically sealed packages and at substantial cost savings. A reliability report available from TI (Bulletin CB-132) describes the results obtained after several million plastic-packaged-device hours of life test.

The following plastic packages are presently in use:

	16 PIN	18 PIN	24 PIN	28 PIN	40 PIN
300 MILS BETWEEN ROWS	X	X			
600 MILS BETWEEN ROWS	X		X	X	X

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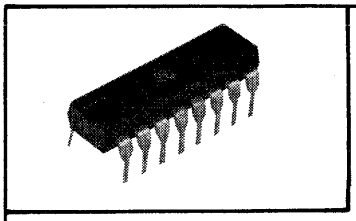
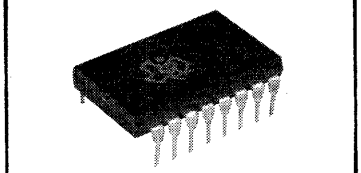
The spacing between leads and between rows as well as the physical dimensions of the packages are identical to those of the ceramic packages. The pin configuration in plastic and in ceramic is always the same. The users who have designed in TI's standard devices over the years can now take advantage of the considerable cost savings provided by plastic without having to modify their systems.

16-pin package (300-mil row spacing)



NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 16.
B. All dimensions in inches unless otherwise noted.

16-pin package (600-mil row spacing)



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.
B. All dimensions are in inches unless otherwise noted.

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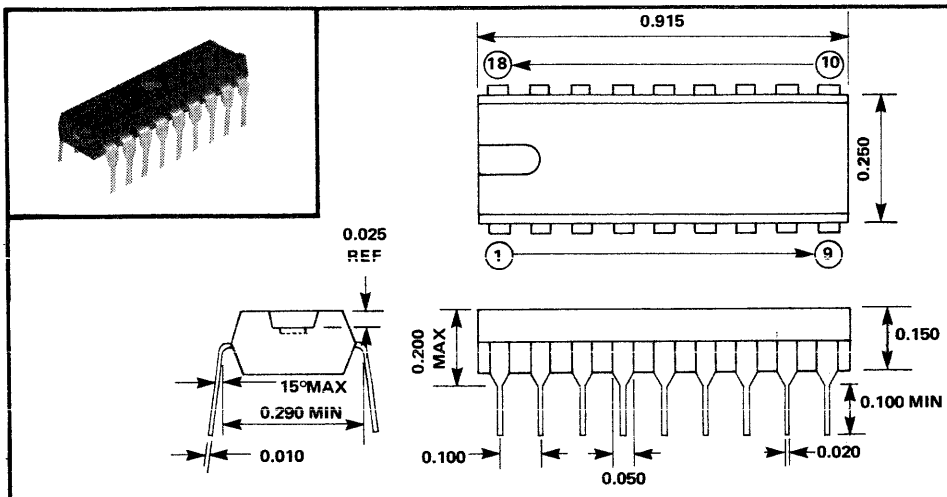
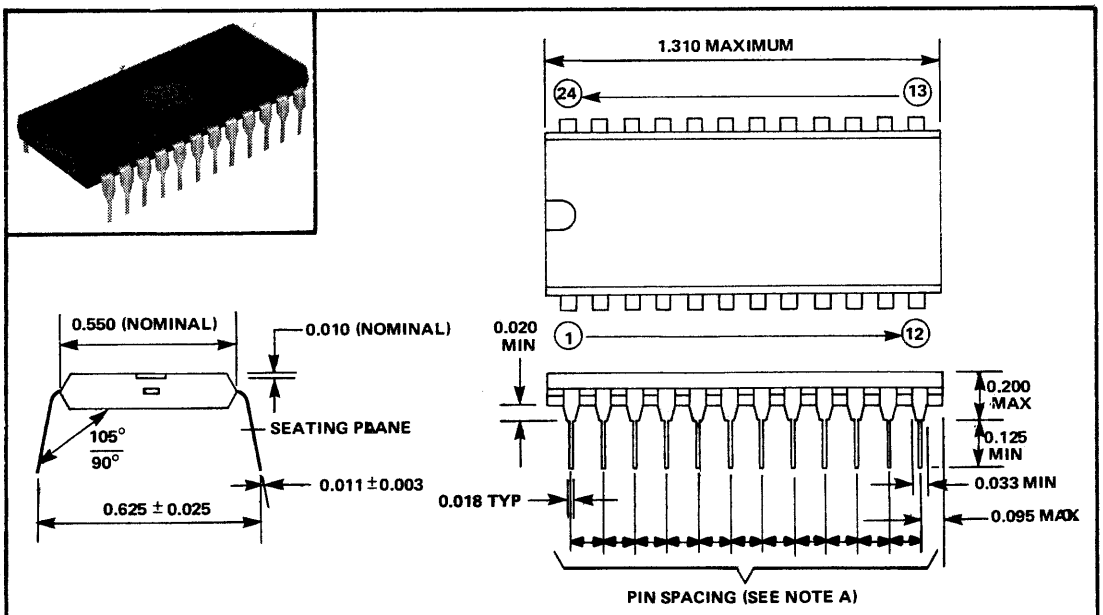
18-pin package



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 18.
B. All dimensions in inches unless otherwise noted.

24-pin package



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 24.
B. All dimensions are in inches unless otherwise noted.

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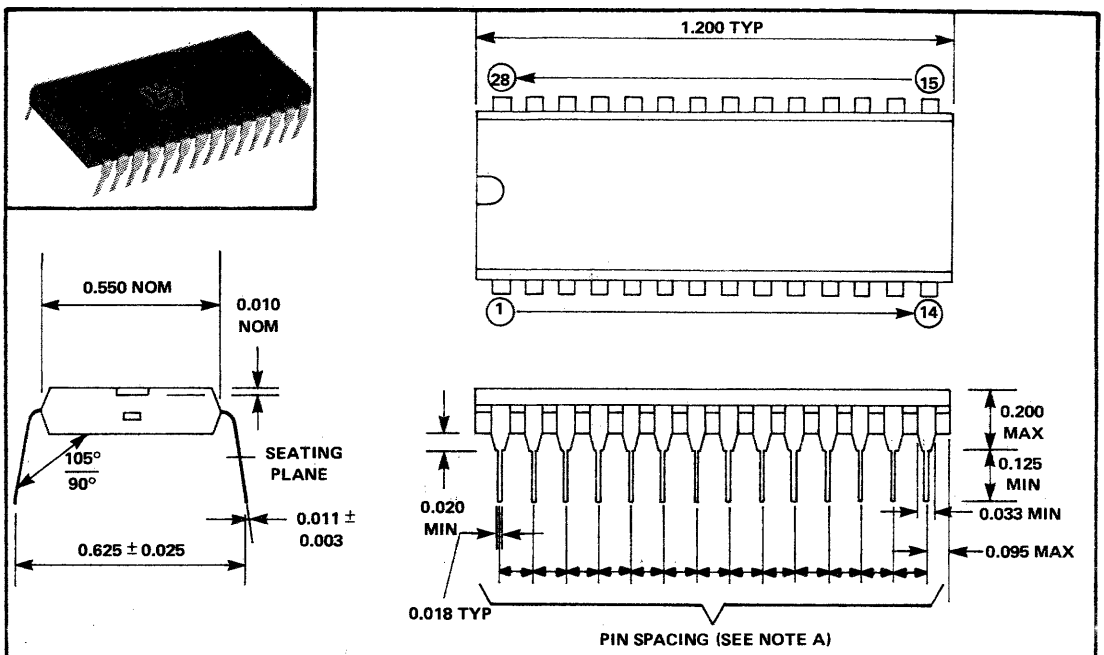
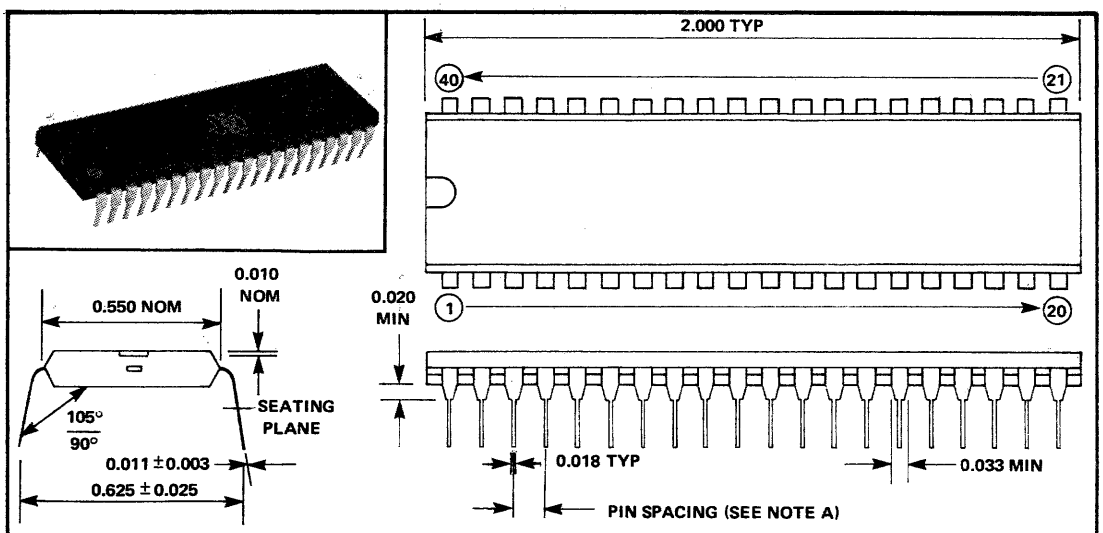
28-pin package



NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 28.
B. All dimensions are in inches unless otherwise noted.

40-pin package



NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins 1 and 40.
B. All dimensions are in inches unless otherwise noted.

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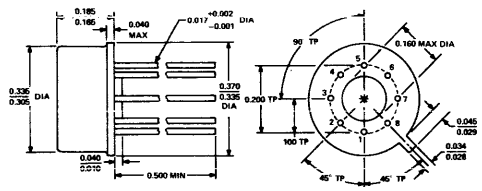
3) Plug-in-type packages

For devices such as shift registers requiring few inputs and outputs, TI uses two plug-in type packages.

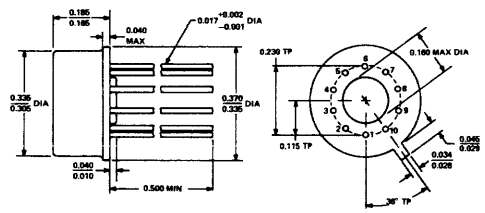
8-PIN PLUG-IN PACKAGE



Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

10-PIN PLUG-IN PACKAGE



Same as JEDEC TO-100 and MO-006AD except for diameter of standoff

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

4) Manufacturing information

a) Alloying

Alloying is performed under inert atmosphere. A silicon gold eutectic is formed during the alloying operation.

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b) Bonding

Thermal compression bonding is used. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any bond strength of less than 2½ grams causes rejection of the entire lot of devices.

c) Sealing

TI uses a low temperature gold-tin brazing to seal ceramic packages.

Plug-in-type packages are welded.

Glass leaks are eliminated by using an etheylene glycol solution heated to +150°C.

Fine-leak elimination is performed through mass spectrometer techniques.

All MOS/LSI devices produced by TI are capable of withstanding 5 x 10^{-7} ppm fine-leak inspection, and may be screened to 5 x 10^{-8} ppm fine leak if desired by the customer for special applications.

d) Shock and Vibration

All packages are capable of withstanding a shock of 3,000 Gs.

All devices are capable of passing a 20,000-G acceleration (centrifuge) test in the Y axis.

Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

MOS/LSI SYSTEM COMPATIBILITY

MOS/LSI circuits have proven conclusively in the past few years their value to system designers. Most designs presently under consideration use both MOS/LSI and bipolar technologies in order to take full advantage of the low cost and high packaging density of MOS/LSI, as well as the flexibility of bipolar techniques for low complexity functions. With present MOS/LSI devices the task of the designer has been greatly simplifier. The devices do not require separate interface circuits between MOS and MOS circuits nor between bipolar and MOS circuits. MOS/MOS and MOS/bipolar compatibility is demonstrated in each of the data sheets included in this catalog. The following information is general and applicable to all TI MOS/LSI devices.

1) POWER SUPPLIES

Two manufacturing technologies are common in MOS/LSI and common throughout the industry: High-threshold MOS and Low-threshold MOS. The power supply requirements generally are:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	0	−12 V	−24 V
Low Threshold	0	−5 V	−17 V

Where

V_{SS} is the substrate supply

V_{DD} is the drain supply

V_{GG} is the gate supply

The drain supply will draw most of the current. Some circuits are designed to use only one power supply (saturated logic). V_{DD} and V_{GG} are then common.

To use MOS in a system it is often convenient to translate all the power supply voltages by a certain voltage. The common arrangement is:

	V_{SS}	V_{DD}	V_{GG}
High Threshold	+12 V	0 V	−12 V
Low Threshold	+5 V	0 V	−12 V

NOTE: Some high-threshold devices are specified at V_{GG} = −28 V and V_{DD} = −14 V.

2) COMPATIBILITY

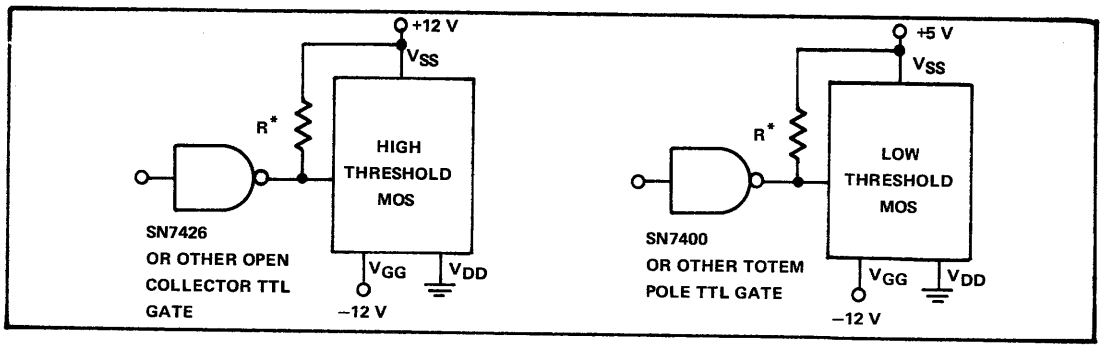
Referencing all voltages to V_{SS}, the input swing on most MOS circuits is as follows:

	High Level	Low level
High Threshold	0 to −3 V	−9 V to −24 V
Low Threshold	0 to −1.5 V	−4.2 V to −17 V

Relating to the translated power supplies as above this becomes:

	High Threshold	Low Threshold
V_{SS}	+12 V	+5 V
V_{DD}	0 V	0 V
V_{GG}	−12 V	−12 V
High level	+9 V to +12 V	+3.5 V to +5 V
Low level	+3 V to −12 V	0.8 V to −12 V

In all cases the input of the MOS circuit will look like a very high impedance. The input compatibility is easily achieved.



* The value of the R resistor varies depending on speed-power requirements. In many cases this resistor is diffused on the MOS chip. For low-threshold MOS the resistor assures that the worst-case TTL output is pulled up to at least 3.5 V for proper MOS circuit operation.

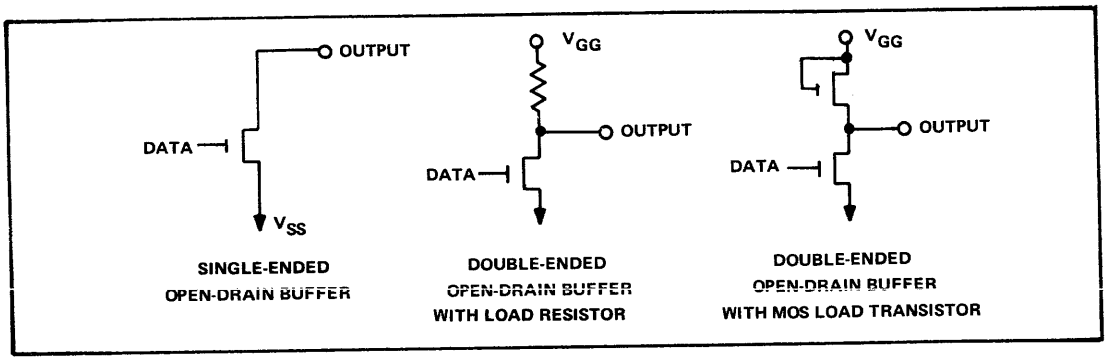
3) OUTPUT COMPATIBILITY

Three types of buffers are commonly used on MOS devices:

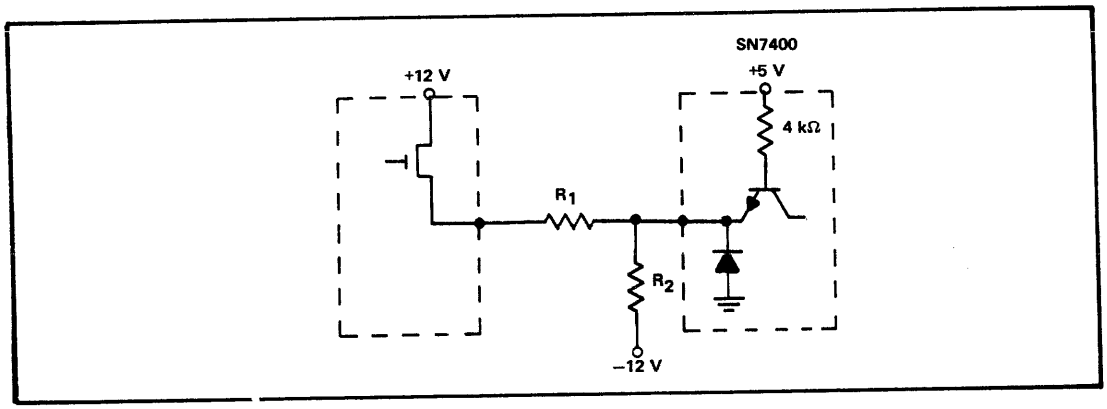
- Single-ended open-drain
- Double-ended
- Push-pull

a) Single-ended open-drain and double-ended

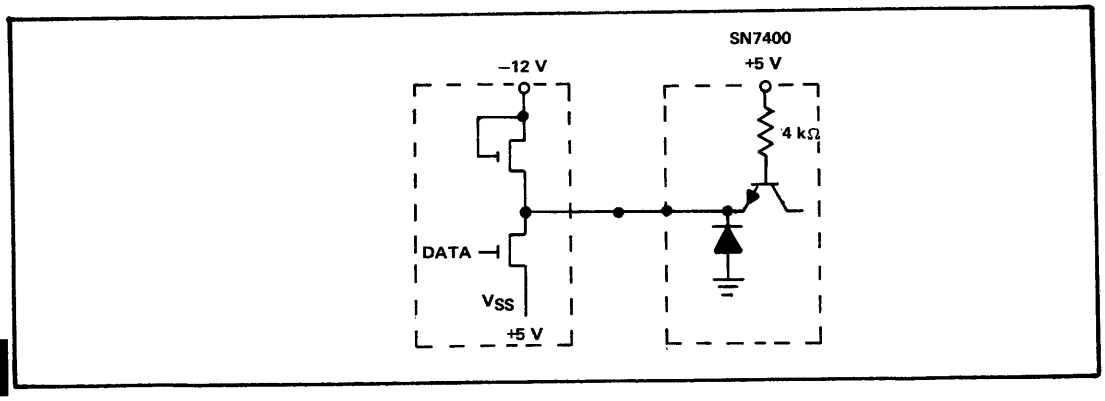
The buffer is simply a current switch. In the "off" state the impedance of the buffer is extremely large, while in the "on" state it is typically under 1 kΩ. A discrete resistor or an MOS transistor may be used as a load with a single-ended open-drain buffer. This resistor or the transistor may be internal to the MOS circuit. When the load transistor is internal to the MOS circuit, the buffer is called a double-ended buffer.



In every case compatibility with MOS is easily achieved. For instance, a single-ended buffer with high-threshold MOS:

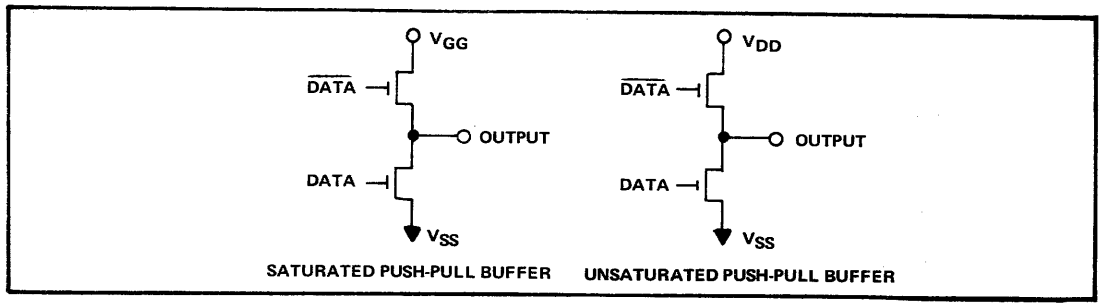


R_2 provides the necessary current sink for the TTL input; R_1 limits the positive excursion to +5 V. If used for low-threshold MOS, V_{SS} is translated up to +5 V instead of +12 V and R_1 can be eliminated. If R_2 is on the chip, no external components are necessary.



b) Push-pull buffer

Two types are common:



The unsaturated push-pull buffer is the most commonly used for low-threshold circuits. It permits direct TTL compatibility without external components. It will also drive directly other low-threshold MOS circuits. This buffer type is used on most of the new MOS/LSI circuits produced by TI.

4) CLOCKS

Depending on the circuit type, there are different clock requirements:

No clocks – Static RAMs, ROMs, etc.

1 clock – with other clocks generated internally

2 clocks – most shift registers

4 clocks – very high-speed low-power-dissipation shift registers

a) One external clock

An internal circuit generates the clocks from a single outside clock signal. The outside clock signal has the same swing as the data input signal and the compatibility is identical (see preceeding paragraph 3).

Single-clock low-threshold MOS circuits will accept a TTL clock without adding components.

b) Two or four clocks

The clock signals must swing between V_{SS} and V_{GG}. To go from a single-TTL-level clock to a multiple-MOS-level clock, two circuits are required: 1) a clock generator to generate the necessary clock pulses, and 2) a clock driver to bring the clock levels to the required values. In most cases only one clock circuit is needed for an entire MOS/LSI system.

SHIFT REGISTERS

In all digital equipment there is a need to temporarily store and transfer data. MOS shift registers are ideally suited for these applications, because they can store economically very large amounts of information.

1) Basic Configuration

MOS shift registers can be supplied in the following configurations:

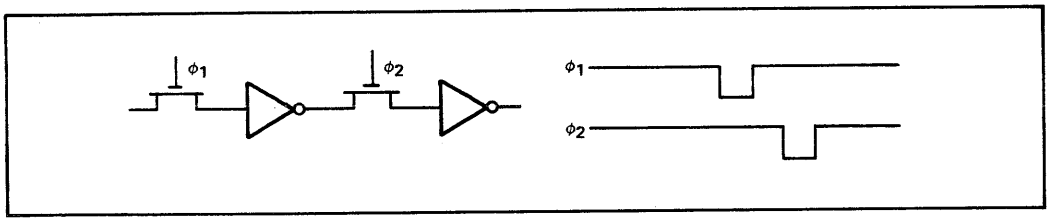
Serial-in/Serial-out

Parallel-in/Serial-out

Serial-in/Parallel-out

The serial-in/serial-out configuration is by far the most popular.

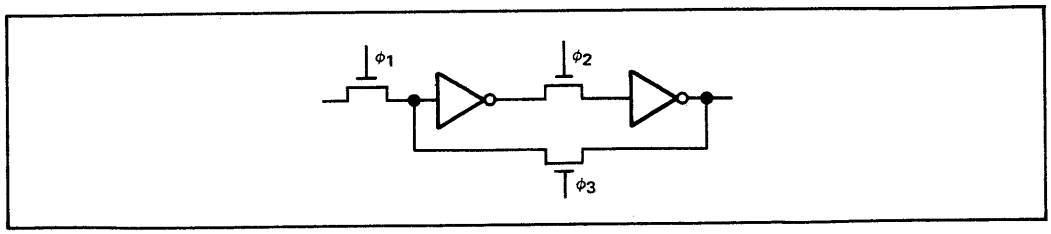
An MOS shift register will be able to store N bits. Each bit is stored on a basic cell consisting of two MOS inverters and timing devices.



2) Static or Dynamic

Dynamic shift registers use two independent inverters (not cross-coupled). The data is temporarily stored on a capacitor inherent to an MOS device. The device can not be operated below a certain clock frequency, or the data storage will be lost.

A static shift register operates the same way a dynamic shift register does, as long as the frequency is high. The two inverters used in a static shift register are the static type (unclocked loads). When the frequency falls below a certain level, a third phase is generated internally and this signal is used to close a feedback loop between the output of the second inverter and the input of the first one.



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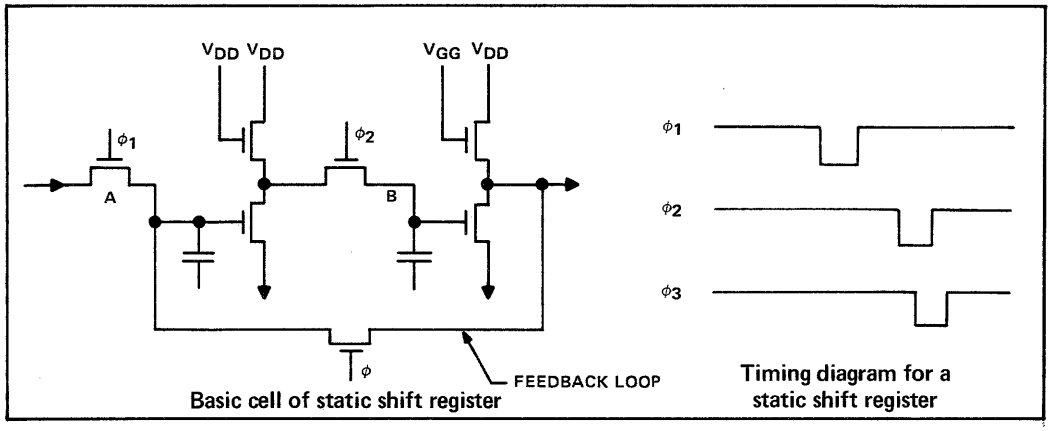
Dynamic shift registers are faster than static registers and dissipate less power. They are not as flexible to use in a system.

a) **Static Shift Registers**

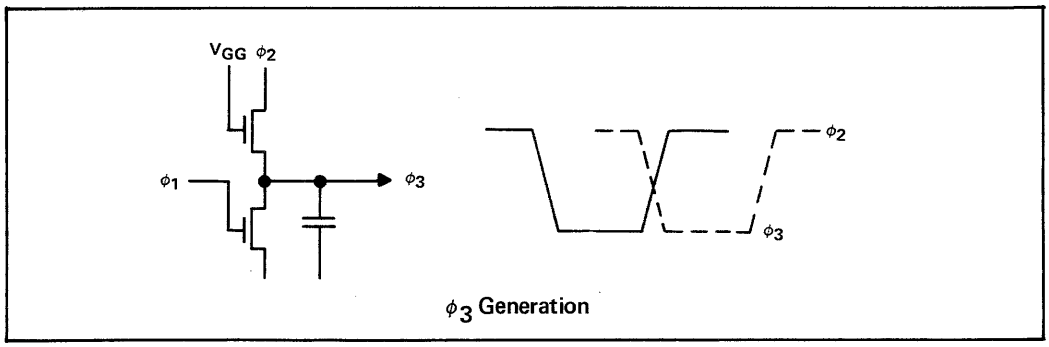
A static shift register uses two static MOS inverters. Three phases (clocks) are necessary for operation. The third-phase clock is always generated internally. The third phase times the feedback loop. The second-clock phase is often generated internally.



Basic cell of static shift register

Timing diagram for a static shift register

A and B are storage nodes. The device operates dynamically except when ϕ_3 is On. ϕ_3 is On when $\phi_1 = 0$ and $\phi_2 = 1$ for more than 10 microseconds. ϕ_3 is delayed ϕ_2 generated by an inverter. Load devices are On all the time. The third phase is generated whenever ϕ_1 stays at a logic 0 and ϕ_2 at a logic 1 for more than 10 microseconds.



ϕ_3 Generation

Static shift registers operate in the 0- to 2.5-MHz clock range. They are extremely flexible and data can be held indefinitely, as long as power is supplied.

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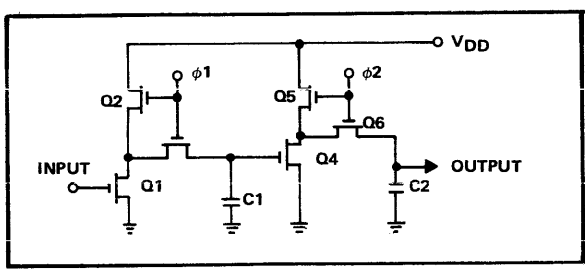
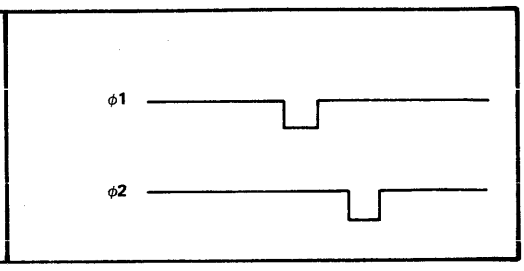
b) Dynamic Shift Registers

Dynamic shift registers use either two or four phases (clocks). These phases can be generated on the chip or be supplied externally. Two-phase shift registers can be classified as ratio and ratioless circuits.

The two-phase ratio-type shift register consists of two simple dynamic inverters and of timing devices.



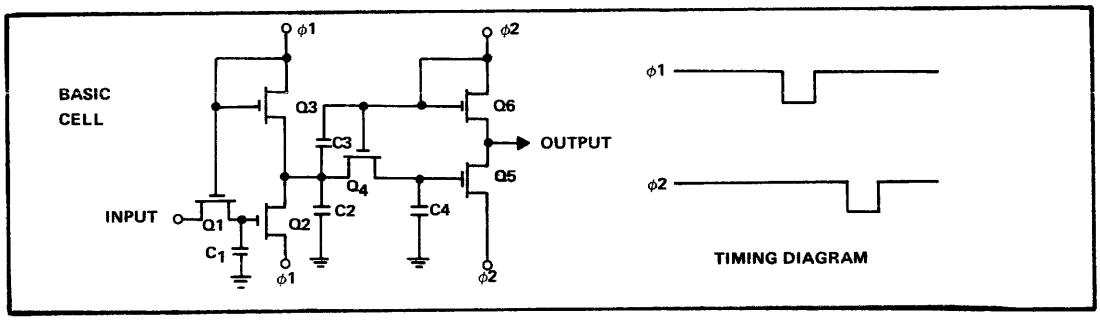
Basic cell for a dynamic shift register



Timing diagram for a 2 phase dynamic shift register

When ϕ_1 is at a logic level 1 (low) the capacitance C_1 charges at the inverse of the data input. Data is transferred out when ϕ_2 goes to 1.

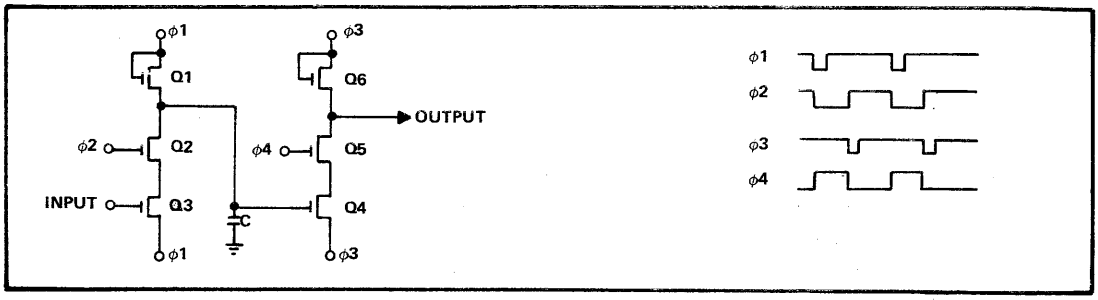
The two-phase ratioless dynamic shift register has been designed to decrease the power dissipation and the chip area. In a ratio-type circuit, current flows through the inverter when the clock and data input are simultaneously at a logic 1. There must be a certain minimum ratio between the size of the two MOS transistors in the inverters (typically>5:1). This will require more chip area than in a ratioless shift register, in which the MOS devices used are usually identical in size.



Two-phase ratioless dynamic shift register

The two-phase ratioless dynamic shift register uses identical transistors throughout and can therefore work at higher clock rates because the precharging paths are of lower impedance than those in the ratio circuit. When ϕ_1 goes to '1' C_2 charges to '1' via Q_3, and C_1 charges to the data input level via Q_1. When ϕ_1 returns to '0', transistor Q_2 turn On if the Input level was a '1' and discharges C_2. For a '0' input, Q_2 stays Off and C_2 is not discharged. Now ϕ_2 goes to a '1' and turns on Q_4 so that C_2 shares any charge it has with C_4. C_3 is used to compensate for the loss of potential across C_2 by introducing a small extra charge on the negative edge of ϕ_2. It does not introduce enough to destroy a logic '0' on C_2. When ϕ_2 returns to a '0', the charge on C_4 transfers the data-input level to the Output.

Four-phase shift registers are used for very high density circuits operated at very high speed.



Four-phase shift register basic cell and timing diagram

In the basic four-phase dynamic shift register, C is precharged via Q_1 during ϕ_1. After ϕ_1, ϕ_2 holds Q_2 On, so C takes a level which is the inverse of the input. The process is repeated by the Slave section $Q_4 - Q_6$ so that the Input level is transferred to the Output after ϕ_3 and during ϕ_4. The stage uses similar transistors throughout, giving high package density. Power dissipation is low, speed can be high, but a relatively complex clock drive circuit is required.

3) MOS Shift Registers from TI

	CLOCK	LOGIC	POWER SUPPLY	FREQUENCY	NUMBER OF BITS
TMS 3000 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 25
TMS 3001 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 32
TMS 3002 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 50
TMS 3003 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 100
TMS 3012 JR/NC	1	Static	+14 V, −14 V	0 – 1 MHz	2 X 128 (Accumulator)
TMS 3016 LR	2	Static	+14 V, −14 V	0 – 1 MHz	2 X 16
TMS 3028 LR	1	Static	+14 V, −14 V	0 – 1 MHz	2 X 128
TMS 3101 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 100
TMS 3102 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 80
TMS 3103 LC/NC	2	Static	+5 V, −12 V	0 – 2.5 MHz	2 X 64
TMS 3112 JC/NC	1	Static	+5 V, −12 V	0 – 1 MHz	6 X 32
TMS 3113 JC/NC		Static	+5 V, −12 V	0 – 2.0 MHz	2 X 133
TMS 3114 JC/NC		Static	+5 V, −12 V	0 – 7.0 MHz	2 X 128
TMS 3304 LR	2	Dynamic	+14 V, −14 V	10 kHz – 5 MHz	3 X 66
TMS 3305 LR	2	Dynamic	+14 V, −14 V	10 kHz – 5 MHz	3 X 64
TMS 3309 LR	4	Dynamic	+12 V, −12 V	10 kHz – 10 MHz	2 X 512
TMS 3314 JR	2	Dynamic	+14 V, −14 V	10 kHz – 2 MHz	3(60 + 4)
TMS 3401 LC	2	Dynamic	+5 V, −12 V	20 kHz – 5 MHz	1 X 512
TMS 3402 LC	2	Dynamic	+5 V, −12 V	20 kHz – 5 MHz	1 X 500
TMS 3404 LC/NC	2	Dynamic	+5 V, −12 V		2 X 512
TMS 3409 JC/NC	1	Dynamic	+5 V, −12 V	10 kHz – 25 MHz	4 X 80
TMS 3412 JC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	4 X 256
TMS 3413 LC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	2 X 512
TMS 3414 LC/NC	2	Dynamic	+5 V, −5 V	10 kHz – 6 MHz	1 X 1024

4) Application

MOS shift registers have met a very wide market acceptance. They have become extremely price competitive and are widely used for memories as well as to replace magneto-stricture and glass-delay lines.

Typical Applications are:

- Data handling
- Refresh memories
- Buffer memories
- Scratch-pad memories
- Delay line
- Desk-top calculators
- Display systems
- Peripherals
- Radar systems

The advantages of MOS shift registers over conventional delay lines and core storage are:

- Price
- Modularity
- Speed
- Physical size
- Physical integrity
- Temperature range

In data handling applications, MOS shift registers can be used either in digit-serial/bit-serial mode or in digit-serial/bit-parallel mode. The latter offers the highest speed of operation but increases the cost of hardware.

In the digit-serial/bit-parallel mode it is convenient to store one digit in a small separate register for operations such as carry correction, loop equalization, and shift. This is achieved in devices such as the TMS 3314 JR triple-60 plus triple-4 shift register.

Any N-bit shift register can be used as a refresh memory by returning outputs to inputs as shown. A particular bit of information is available at the output every

$$\frac{N}{\text{clock frequency}} \text{ seconds.}$$

This is particularly useful for renewing fading displays such as CRT character-generator systems. New data is written in via a 2-way input gate circuit.

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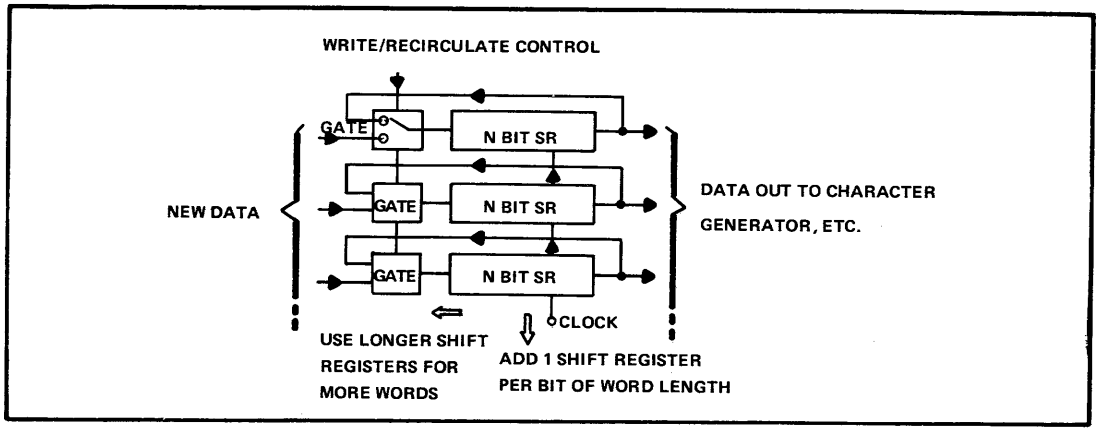
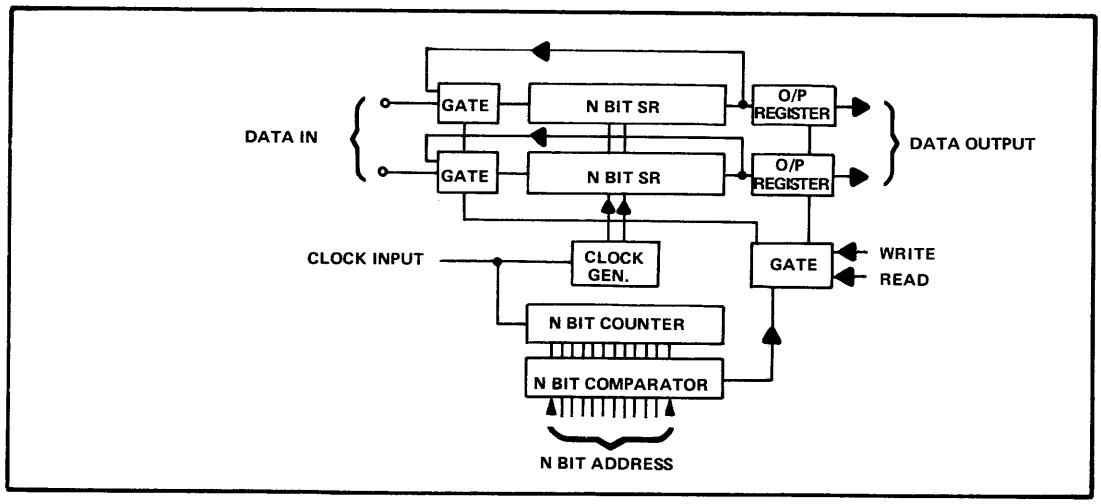


Shift registers used as refresh memory

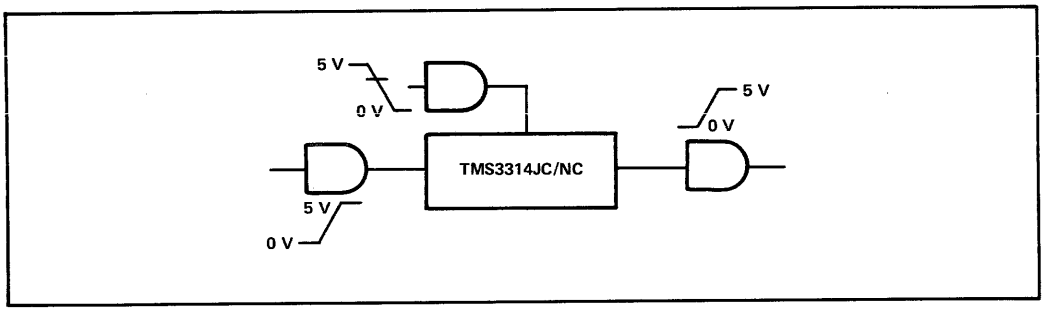
By adding an address counter and comparator in the refresh memory, it becomes a "scratch pad" memory. Data can be written into and read out of any point specified by the input address code. An output register is necessary to store the required output data and to provide a 1-bit delay so that the Read address is the same as the Write address because there is a 1-bit delay between output and input.



Shift registers used as scratch pad memory

5) Clocking the Shift Registers

Most of the new shift registers designed by Texas Instruments feature *total TTL compatibility*. A clock driver is included on the chip and the clock line is driven directly by TTL. For examples of this configuration, see the specifications for the TMS 3314 JC/NC and the TMS 3409 JC/NC.



Older circuits use two clock lines with a V_{GG} swing. The user must:

- Generate the clocks
- Level shift the clocks

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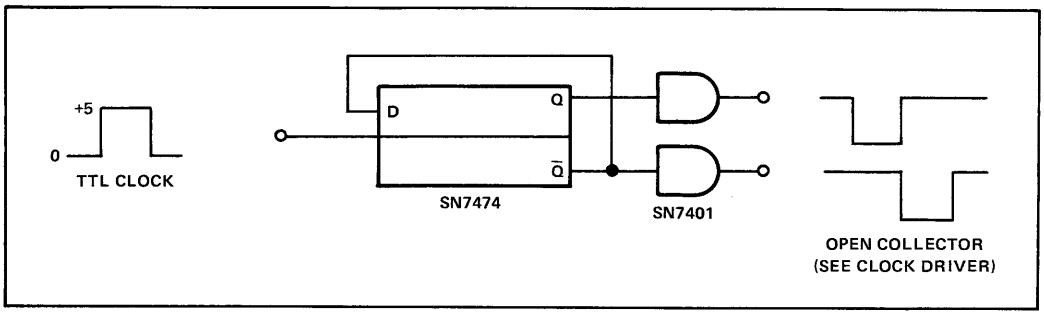
Generating the two nonoverlapping clocks is a simple matter, easily accomplished through a D-type flip-flop.

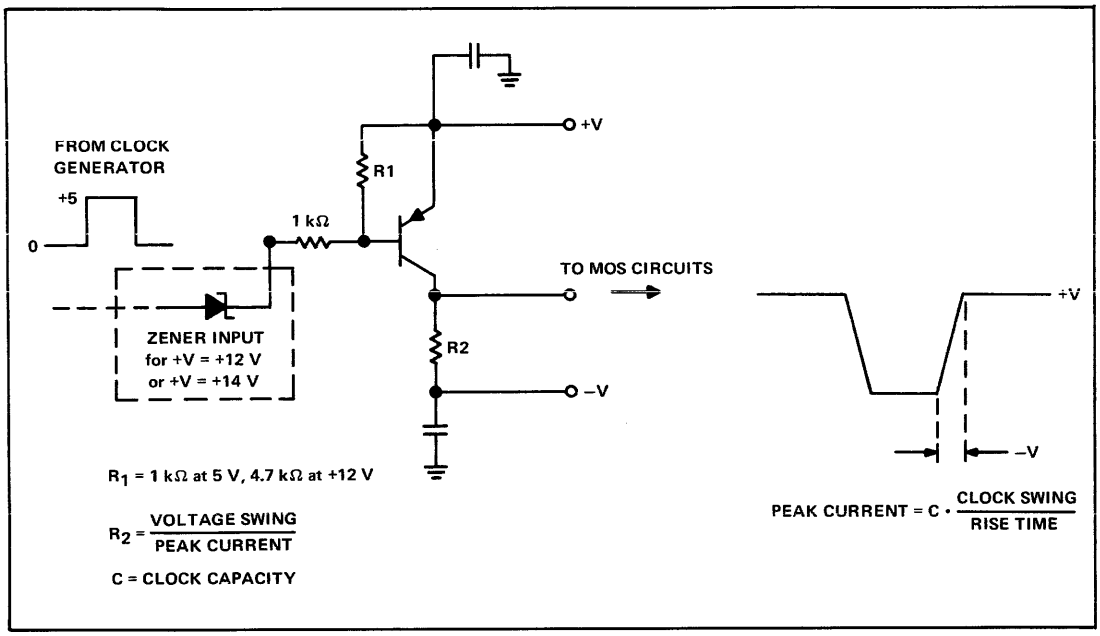


This arrangement is favorable because Q and $\overline{Q}$ will be of opposite polarities when the TTL clock is stopped and this allows static storage in static shift registers.

Should four phases be generated, the user would connect two D-type flip-flops as a Johnson counter.

Once the clocks are generated, the voltage level must be shifted to the appropriate value.

This can be achieved easily as shown in the illustration below. The clock driver circuit is used to drive a capacitive load (clock lines capacitance) between +V and −V.



Typical clock driver circuits

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MOS
LSI

TMS 3000 LR-DUAL 25-BIT STATIC SHIFT REGISTER
TMS 3001 LR-DUAL 32-BIT STATIC SHIFT REGISTER

FEBRUARY 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

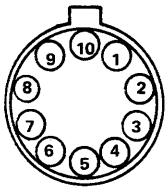
description

The TMS 3000 LR and TMS 3001 LR are dual static shift registers. Each device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. Transistors in the device are P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low-output-impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The TMS 3000 LR and TMS 3001 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input 1	6	Clock ϕ_2
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	GND (V_{SS})	10	No connection

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

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PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)	0		5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See waveforms and Note 5)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See waveforms and Note 5)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.

3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock during which period the data to be recognized must be maintained at the input to ensure its recognition.

5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -20$ V, $T° = 25°C$			0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	$V_I = -28$ V, $V_{GG} = 0$ V, $T° = 25°C$			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA, $C_L = 20$ pF		0.3	−1	V
		$I_O = 2$ mA, $C_L = 20$ pF		−2.6	−5	V
		$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V		−0.5	−1	V
V_{OL}	Logic 1 output voltage	$I_O = 0$, $C_L = 20$ pF	−12	−13.5	−14	V
		$I_O = 0.5$ mA	−10.5	−12.5	−14	V
		$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V, $V_\phi, V_{\phi L} = -24$ V, $C_L = 20$ pF, $V_{in(1)} = -8.5$ V, $V_{in(0)} = -2$ V	−8.8	−10.5	−12	V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA		1.5	2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = 0.5$ mA		1.5	7	kΩ
I_{DD}	Supply current from V_{DD} terminal*	TMS 3000 LR, $T° = 25°C$		−14	−20	mA
		TMS 3001 LR, $T° = 25°C$		−16	−24	mA
I_{GG}	Supply current from V_{GG} terminal*	TMS 3000 LR, $T° = 25°C$		−2	−3.5	mA
		TMS 3001 LR, $T° = 25°C$		−2	−3.5	mA
f_{max}	Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$.
* Current into a terminal is a positive value.

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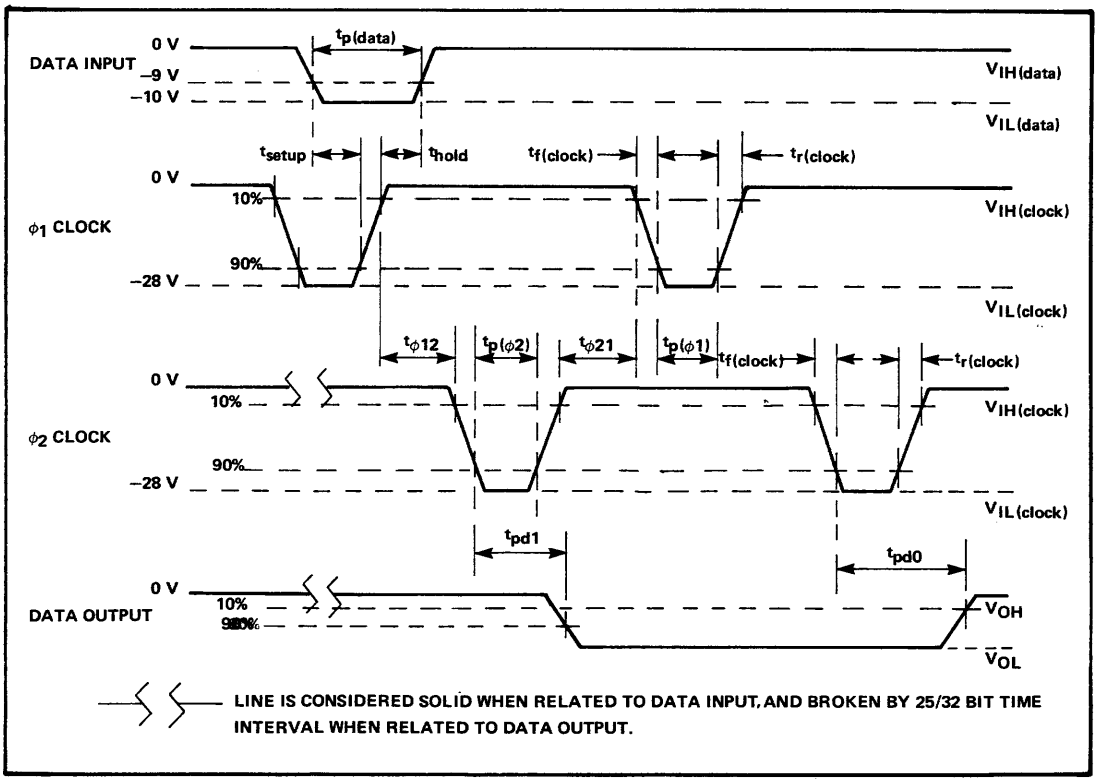
switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms			325	475	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3000 LR		8	12	pF
			TMS 3001 LR		11	15	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3000 LR		15	20	pF
			TMS 3001 LR		20	30	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

* $C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

voltage waveforms



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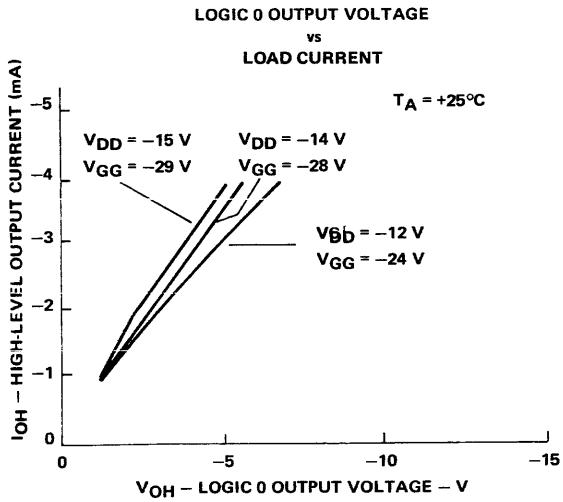
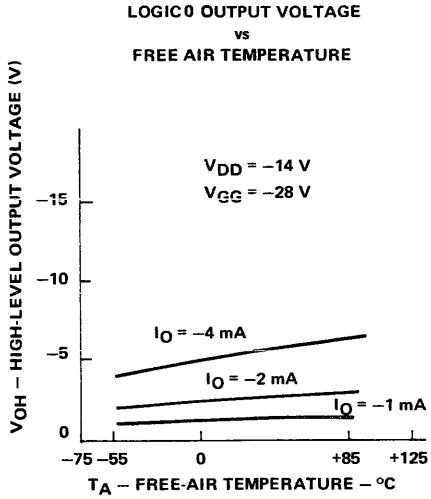
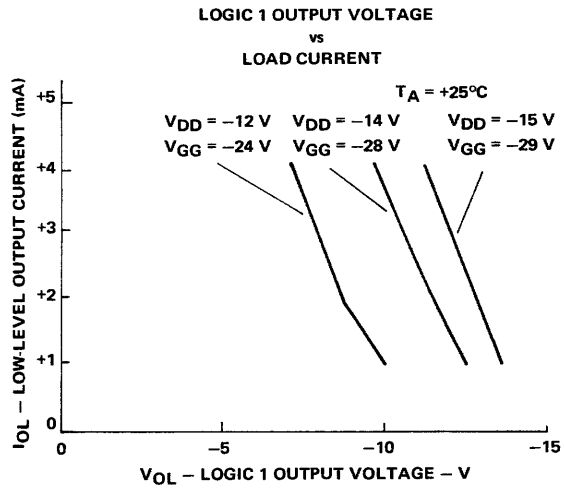
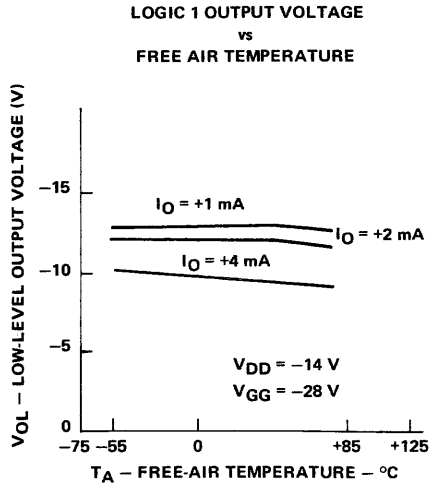
typical characteristics









typical application data

1) MOS/TTL interface

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With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.

An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements — values as low as 1 kΩ can be used for high-speed operation, while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

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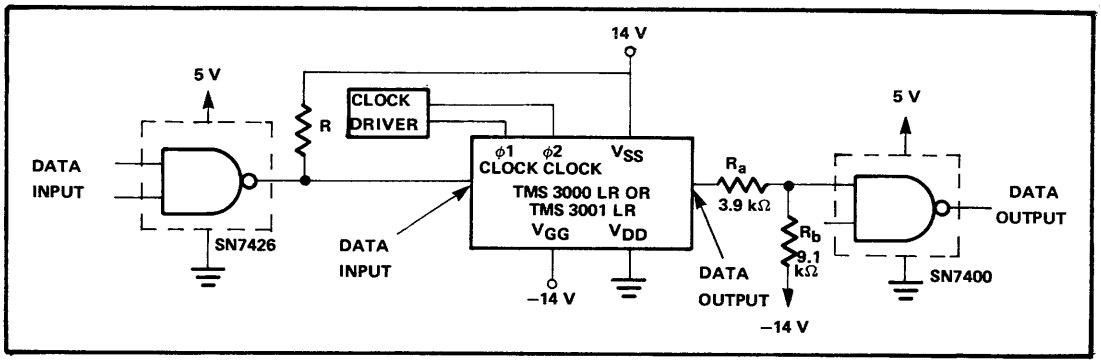
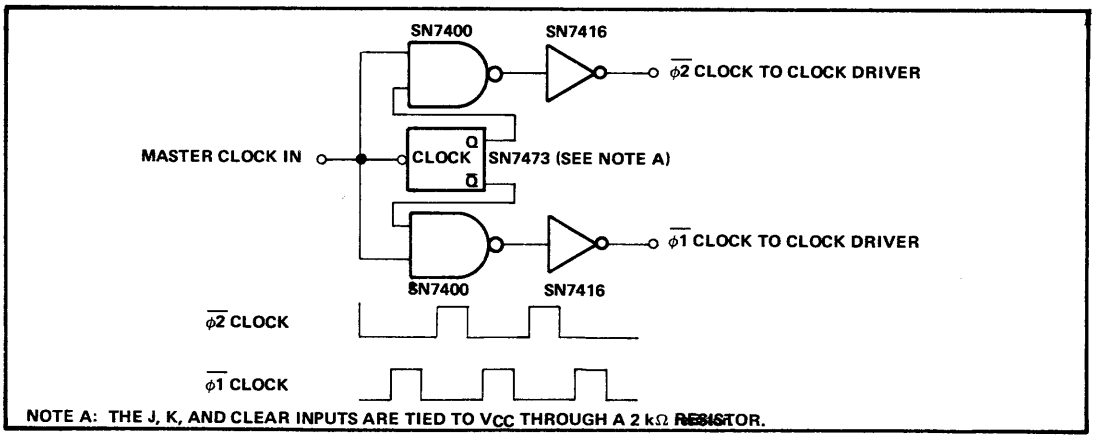
typical application data (continued)



At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9-kΩ resistor and the 9.1-kΩ resistor, to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

2) Two-phase clock generator



NOTE A: THE J, K, AND CLEAR INPUTS ARE TIED TO V_{CC} THROUGH A 2 kΩ RESISTOR.

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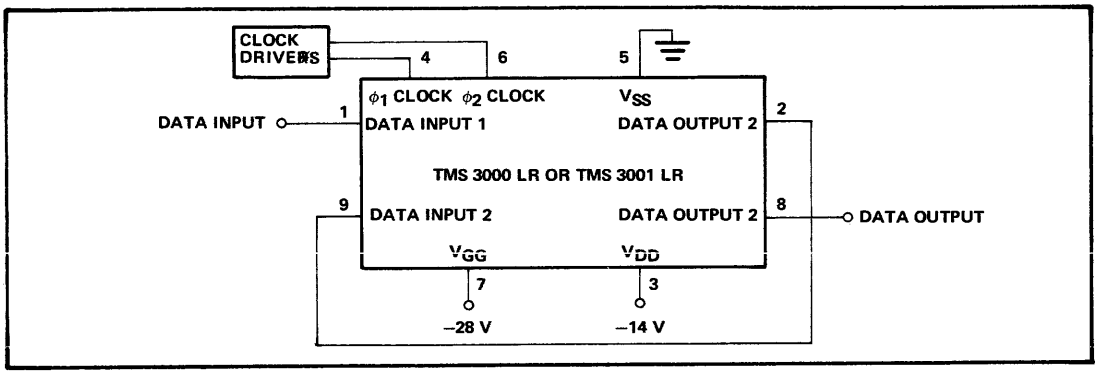
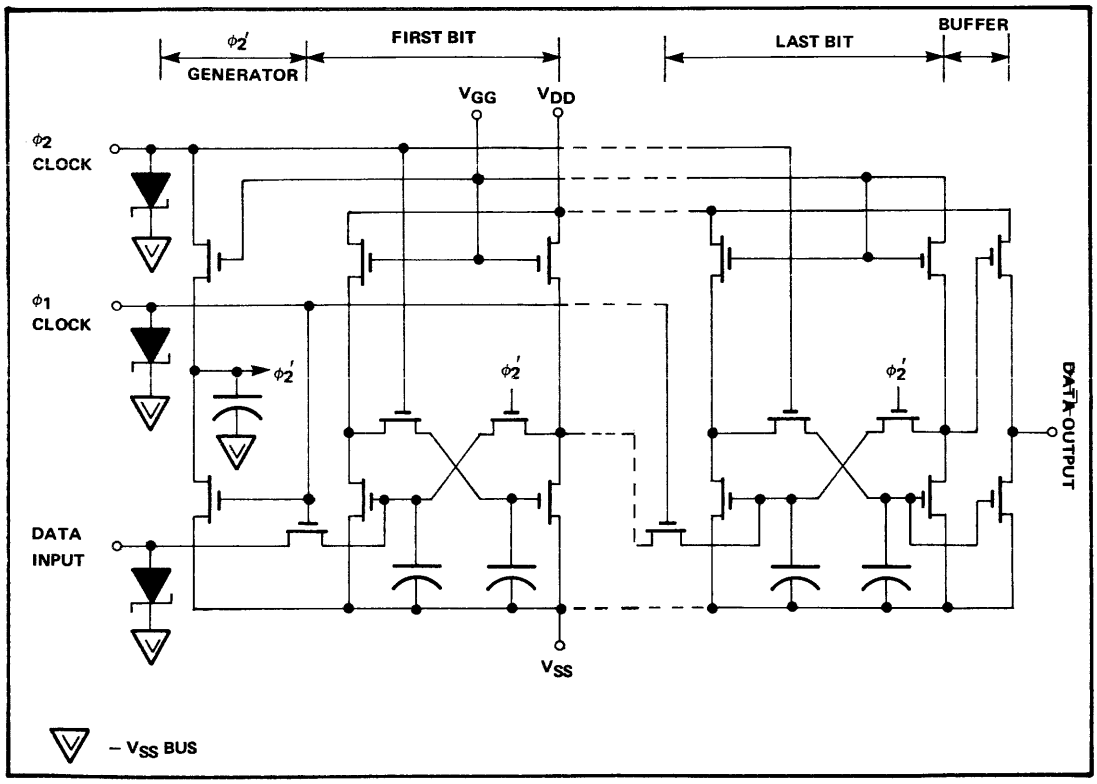
expansion to single 50- or 64-bit register



schematic (each register)



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MOS
LSI

TMS 3002 LR-DUAL 50-BIT SHIFT REGISTER
TMS 3003 LR-DUAL 100-BIT SHIFT REGISTER

JANUARY, 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

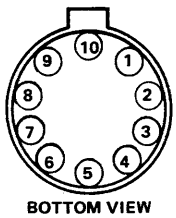
description

The TMS 3002 LR and TMS 3003 LR are dual static shift registers. Each device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low-output-impedance non-inverting push-pull output buffers.

Two power-supply levels and two clocks are required for operation, with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long-term storage, the ϕ_1 clock must be held at logic 0 and the ϕ_2 clock at logic 1.

mechanical data and pin configuration

The TMS 3002 LR and TMS 3003 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	6	Clock ϕ_2
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	GND (V_{SS})	10	No connection

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

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recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Note 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Note 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Note 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See waveforms and Note 5)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See waveforms and Note 5)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL} Logic 1 input current into data input	$V_I = -20$ V, $T° = 25°C$			0.5	μA
$I_{IL(\phi)}$ Logic 1 input current into either clock input	$V_I = -28$ V, $V_{GG} = 0$ V, $T° = 25°C$			50	μA
V_{OH} Logic 0 output voltage	$I_O = 0$ mA, $C_L = 20$ pF		0.3	−1	V
	$I_O = 2$ mA, $C_L = 20$ pF		−2.6	−5	V
	$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V		−0.5	−1	
V_{OL} Logic 1 output voltage	$I_O = 0$ mA, $C_L = 20$ pF	−12.0	−13.5	−14	V
	$I_O = 0.5$ mA	−10.5	−12.5	−14	V
	$I_O = 0$ mA, $V_{dd} = -12$ V, $V_{gg} = -24$ V, $V_\phi, V_{\phi L} = -24$ V, $C_L = 20$ pF, $V_{in(1)} = -8.5$ V, $V_{in(0)} = -2$ V	−8.8	−10.5	−12	V
R_{OH} Output resistance, logic 0	$I_O = -2.0$ mA		1.5	2.5	kΩ
R_{OL} Output resistance, logic 1	$I_O = 0.5$ mA		1.5	7	kΩ
I_{DD} Supply current from V_{DD} terminal§	TMS 3002 LR, $T° = 25°C$		−8.5	−15	mA
	TMS 3003 LR, $T° = 25°C$		−16	−26	mA
I_{GG} Supply current from V_{GG} terminal§	TMS 3002 LR, $T° = 25°C$		−2	−3	mA
	TMS 3003 LR, $T° = 25°C$		−2	−3	mA
f_{max} Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$.
§ Current into a terminal is a positive value.

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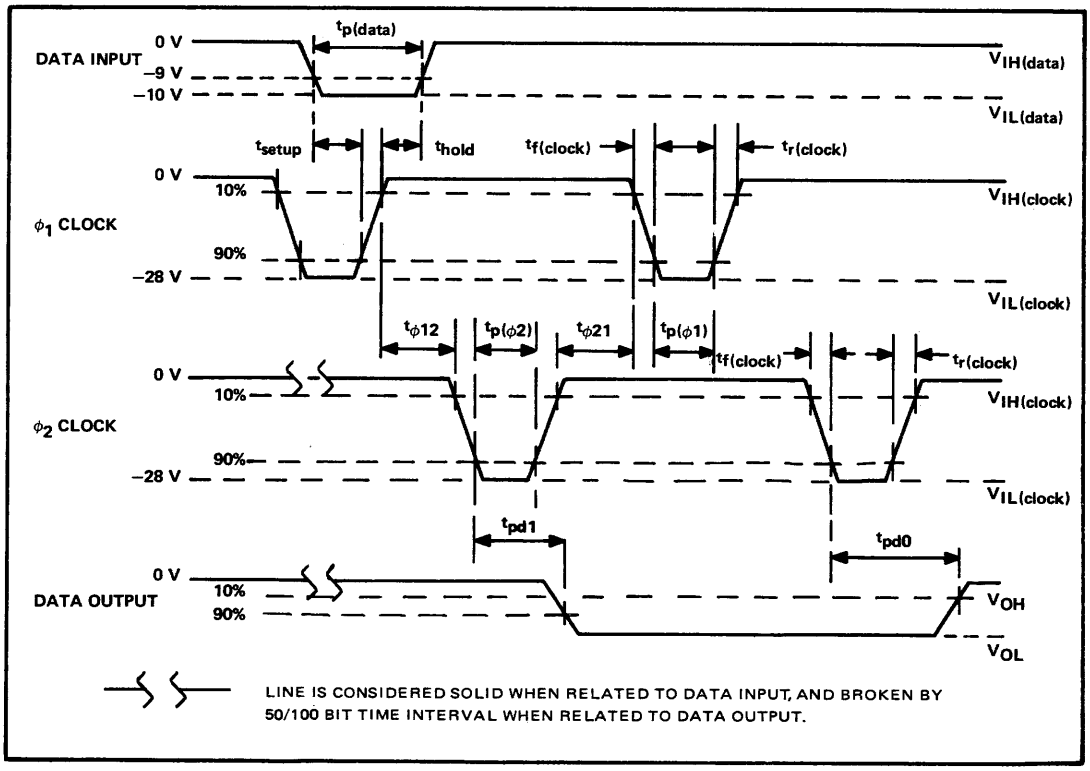
switching characteristics, V_{DD} = −14 V, V_{GG} = −28 V, R_L = 10 mΩ, C_L = 20 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms			250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock	See voltage waveforms			250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	V_I = 0 V, $V_{I(\phi2)}$ = 0 V, f = 1 MHz	TMS 3002 LR		18	23	pF
			TMS 3003 LR		28	33	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	V_I = 0 V, $V_{I(\phi1)}$ = 0 V, f = 1 MHz	TMS 3002 LR		30	35	pF
			TMS 3003 LR		53	60	pF
C_{in}	Capacitance of data input	V_I = 0,	f = 1 MHz		5	7	pF

$C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2' clock.

voltage waveforms



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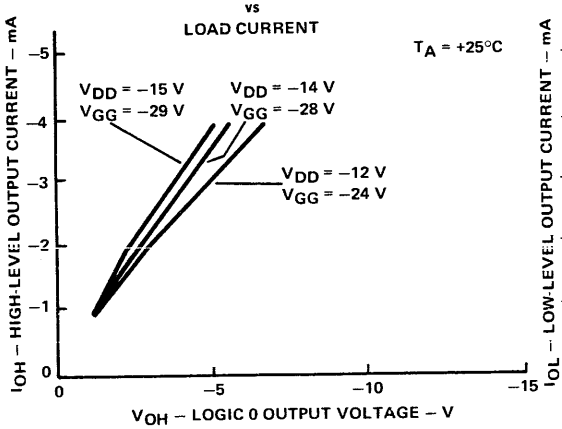
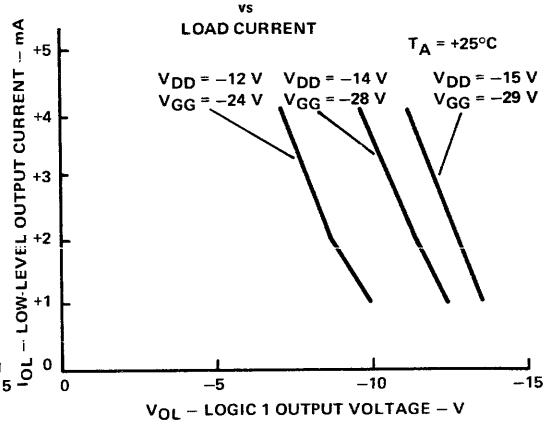
typical characteristics

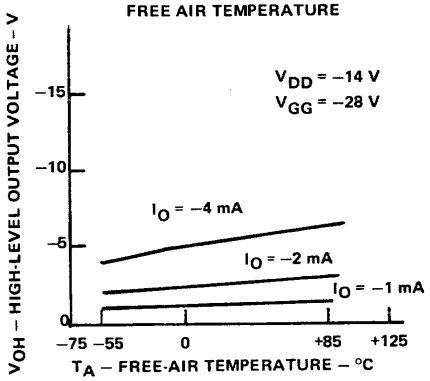
LOGIC 0 OUTPUT VOLTAGE
vs
LOAD CURRENT



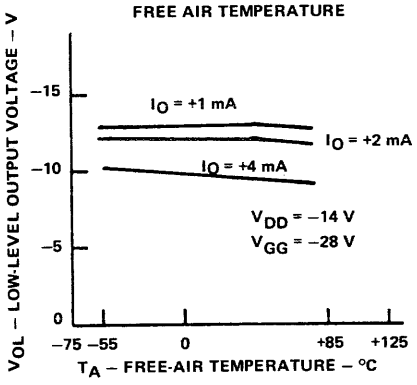
LOGIC 1 OUTPUT VOLTAGE
vs
LOAD CURRENT



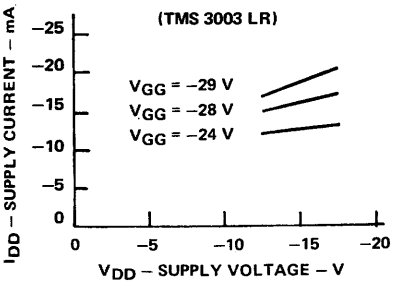
LOGIC 0 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



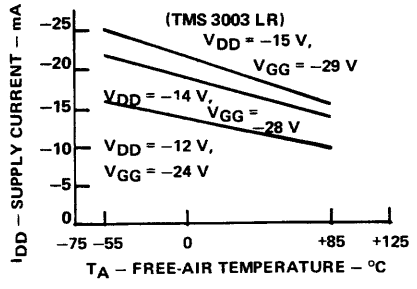
LOGIC 1 OUTPUT VOLTAGE
vs
FREE AIR TEMPERATURE



SUPPLY CURRENT
FROM V_{DD} SUPPLY
vs
DRAIN POWER SUPPLY VOLTAGE
(TMS 3003 LR)



SUPPLY CURRENT
FROM V_{DD} SUPPLY
vs
FREE-AIR TEMPERATURE



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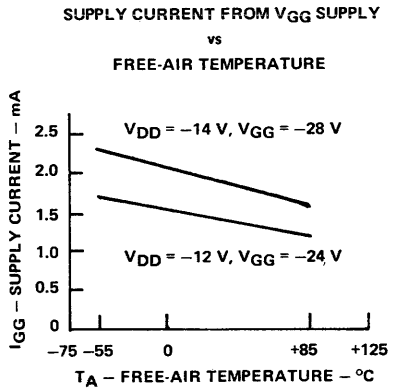
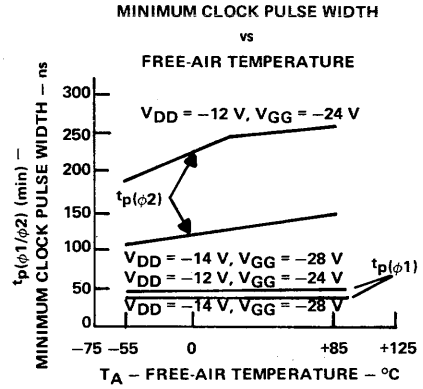
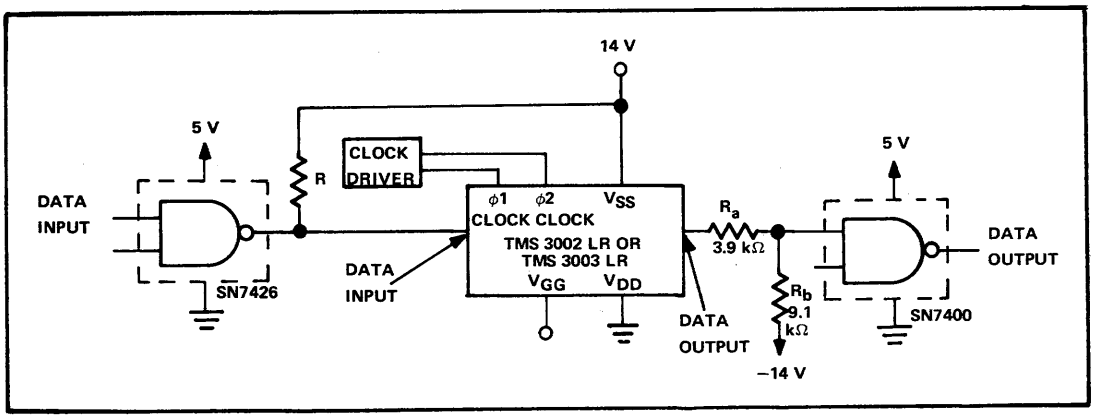
typical characteristics (continued)





typical application data

With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements — values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9-kΩ resistor and the 9.1-kΩ resistor to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

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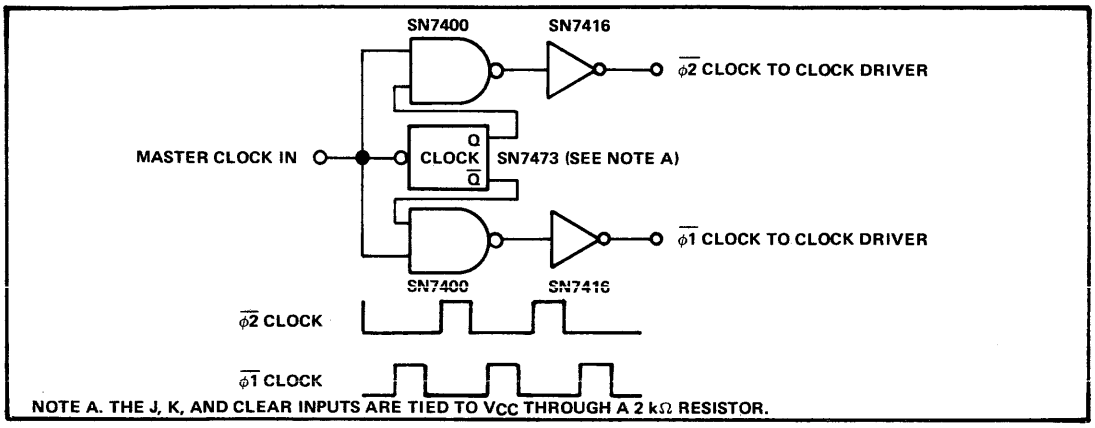
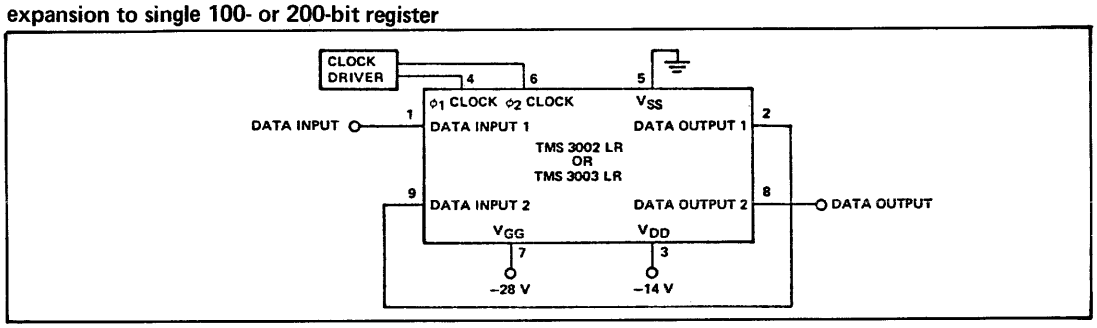
TMS 3002 LR-DUAL 50-BIT SHIFT REGISTER
TMS 3003 LR-DUAL 100-BIT SHIFT REGISTER

two-phase clock generator

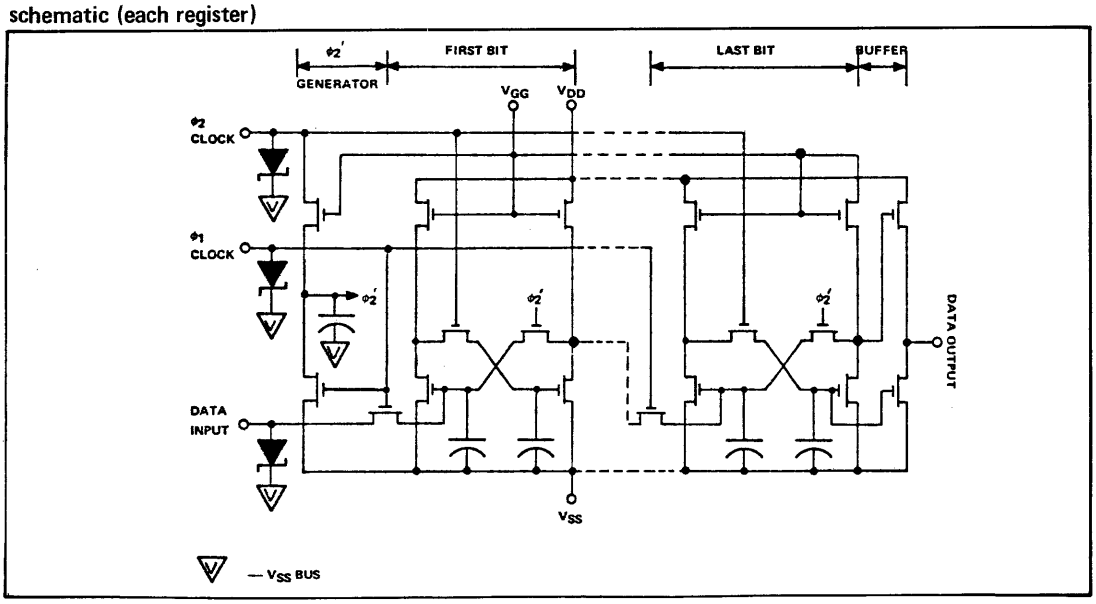


NOTE A. THE J, K, AND CLEAR INPUTS ARE TIED TO V_{CC} THROUGH A 2 kΩ RESISTOR.

expansion to single 100- or 200-bit register



schematic (each register)



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MOS
LSI

TMS 3012 JC, NC - DUAL 128-BIT ACCUMULATOR
TMS 3028 LC - DUAL 128-BIT SHIFT REGISTER

FEBRUARY, 1971

features

- 256 bits of storage
- Single clock phase
- Static logic
- TTL compatible
- DC to 1 MHz operation
- Push-pull output buffers
- 16-pin dual-in-line package (TMS 3012 JC/NC)
- Recirculating control logic (TMS 3012 JC/NC)

description

The TMS 3012 JC/NC consists of two separate 128-bit static shift registers with independent input and output terminals and logic, within the circuit, for loading and recirculating information. Two power supplies and one external clock are required for operation. Three clocks are generated internally. Cross-coupled flip-flops are used to implement each bit of delay and enable data to be stored indefinitely between two clock pulses. The entire device is constructed on a single monolithic chip using thick-oxide techniques and MOS P-channel enhancement-mode transistors. A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "JC". "NC" is the designation for a unit mounted in a 16-pin plastic package.

The TMS 3028 LC is identical to the TMS 3012 JC/NC except for the fact that recirculate logic is not included on the chip and that the device is mounted in a TO-100 package instead of a dual-in-line package.

operation

Transferring data into the register and shifting the data in the register are accomplished when the ϕ_{IN} clock is at a logic 1; for long-term data storage, the ϕ_{IN} clock must be held at logic 0. Output appears on the positive-going edge of the ϕ_{IN} clock pulse.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range*	−30 V to 0.3 V
Supply voltage V_{GG} range*	−30 V to 0.3 V
Clock and data input voltage ranges*	−30 V to 0.5 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

* These voltage values are with respect to substrate terminal.

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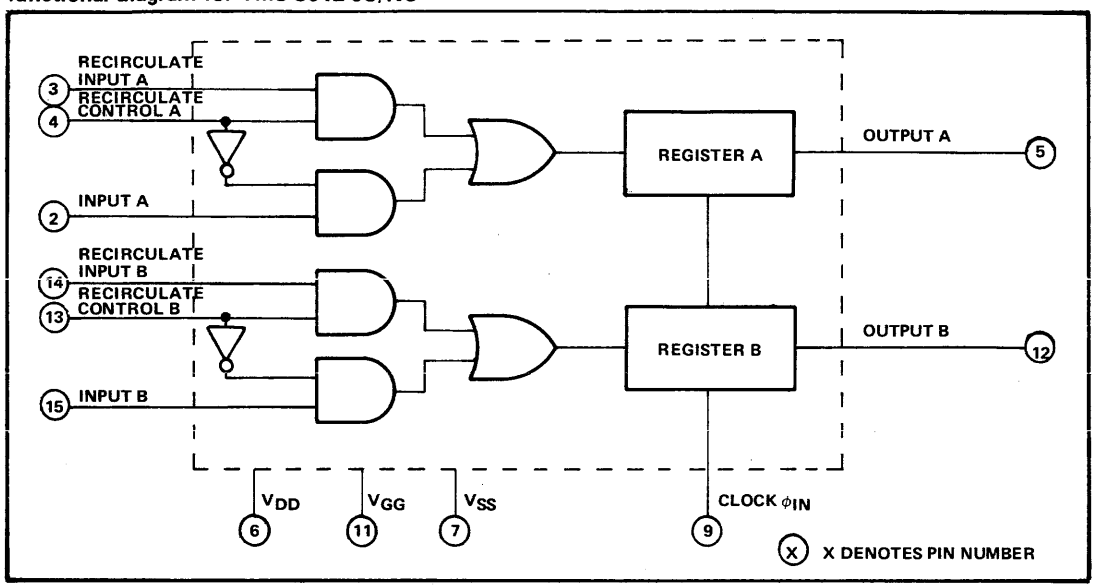
functional diagram for TMS 3012 JC/NC



recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−13	−14	−15	V
Supply voltage V_{GG}	−27	−28	−29	V
Width of data pulse, $t_{(data)}$ (See voltage waveforms)	0.4		10	μs
Width of clock pulses: $t_{p(Logic\ 1)}$ See voltage waveforms	0.4		5	μs
$t_{p(Logic\ 0)}$ See voltage waveforms	0.4		∞	μs
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)			5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			1	μs
Clock repetition rate	0		1	MHz
$V_{in(1)}$* Data/Recirculate Control Logic 1 voltage	−9	−14	−15	V
$V_{in(0)}$* Data/Recirculate Control Logic 0 voltage	0	0	−2	V
$V_{in(1)\phi}$* Logic 1 clock input voltage	−9	−14	−15	V
$V_{in(0)\phi}$* Logic 0 clock input voltage	0	0	−2	V
Data change time before clock change to 0 (t_{db})	0.2			μs
Data change time after clock change to 0 (t_{da})	0.2			μs
Recirculate control change time before clock change to 0 (t_{rb}) (See Note 2)	0.3			μs
Recirculate control change time after clock change to 0 (t_{ra}) (See Note 2)	0.3			μs

NOTES: 1. All voltages are with respect to V_{SS}.
2. TMS 3012 JR only.

* To ensure correct data loading, the input should reach the desired level at least time t_{db} before the clock goes to logic 0, and should remain at that level for a time t_{da} after the clock has changed to 0. Similarly, the recirculate control input should not change state for a period t_{rb} before and t_{ra} after the clock change from logic 1 to logic 0.

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electrical characteristics at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
$V_{out(1)}$	Logic 1 output voltage	R_L = 10 kΩ to V_{SS}	−11	−13		V
$V_{out(0)}$	Logic 0 output voltage	R_L = 10 kΩ to V_{SS}		−0.3	−1	V
$I_{in(1)}$	Data input, leakage current	V_{in} = −20 V			−0.5	μA
$I_{in(1)\phi}$	Clock input, leakage current	$V_{in\phi}$ = −20 V, V_{GG} = 0			0.5	μA
Z_{out}	Output impedance to ground	V_{out} = 0 to −1 V		0.7	1.5	kΩ
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−23	−30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −15 V, V_{GG} = −29 V		−3	−5.5	mA

† Unless otherwise noted, R_L = 10 kΩ, and C_L = 10 pF.

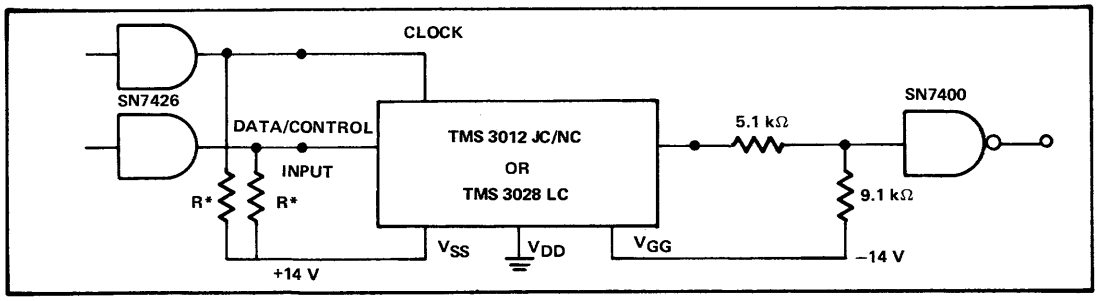
‡ All other pins are at V_{SS}

dynamic electrical characteristics, V_{DD} = −14 V, V_{GG} = −28 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logic 1 level from clock φ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		500	700	ns
t_{pd0}	Propgation delay time to logic 0 level from clock φ to data output	R_L = 10 kΩ to ground, C_L = 10 pF		400	600	ns
C_{in}	Capacitance of data input	V_{in} = 0, f = 1 MHz, T_A = 25°C		3	5	pF
$C_{in\phi}$	Capacitance of clock input	$V_{in\phi}$ = 0, f = 1 MHz, T_A = 25°C		5	7	pF

interface circuits

a) TTL/DTL



* Select R for speed and power requirements.

b) MOS

No external components are required.

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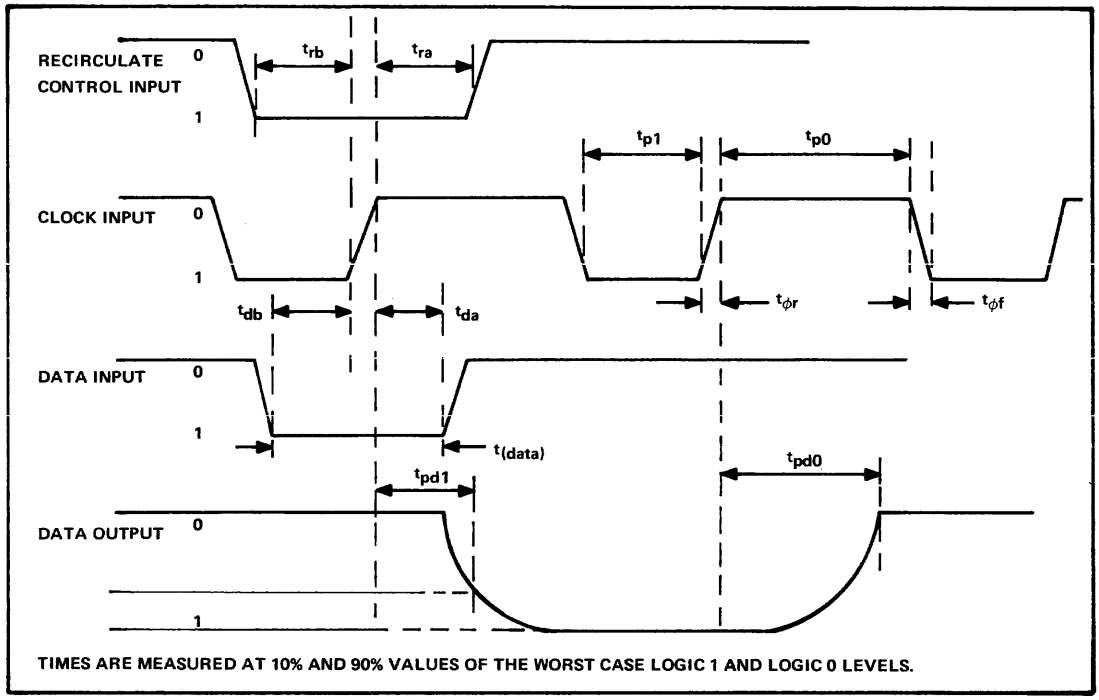
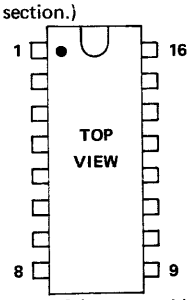
voltage waveforms (TMS 3012 JC/NC only)



TIMES ARE MEASURED AT 10% AND 90% VALUES OF THE WORST CASE LOGIC 1 AND LOGIC 0 LEVELS.

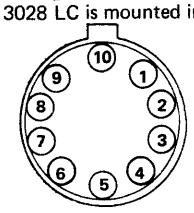
mechanical data

The TMS 3012 is available in both a 16-pin hermetically sealed ceramic dual-in-line package (JC) and a 16-pin plastic package (NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	9	Clock ϕ
2	Input A	10	No connection
3	Recirculate Input A	11	V_{GG}
4	Recirculate Control A	12	Output B
5	Output A	13	Recirculate Control B
6	V_{DD}	14	Recirculate Input B
7	V_{SS}	15	Input B
8	No connection	16	No connection

The TMS 3028 LC is mounted in a TO-100 package. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	6	V_{SS}
2	Output 1	7	V_{GG}
3	V_{DD}	8	Output 2
4	Clock ϕ_1	9	Input 2
5	V_{SS}	10	No connection

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TMS 3016 LR
DUAL 16-BIT STATIC SHIFT REGISTER

JANUARY 1971

features

- Static logic
- DC to 1 MHz operation
- Low power dissipation
- Push-pull output buffers
- TTL compatible

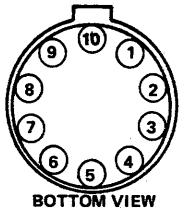
description

The TMS 3016 LR is a dual static shift register. This device contains two dc-to-1-MHz shift registers with independent input and output terminals and common clocks and power. MOS thick-oxide technology is used to fabricate cross-coupled flip-flops for each register bit so that data can be stored indefinitely. The transistors in the device are the P-channel enhancement-mode type. All input leads have zener network protection and all outputs contain low output impedance, non-inverting push-pull output buffers.

Two power supply levels and two clocks are required for operation with a third clock generated internally. Data is transferred into the register when the ϕ_1 clock is pulsed to logic 1. Data is shifted when the ϕ_1 clock is returned to logic 0 and the ϕ_2 clock is pulsed to logic 1. Output data appears on the logic 0 to logic 1 transition of the ϕ_2 clock. For long term storage, the ϕ_1 clock must be held at a logic 0 and the ϕ_2 clock at a logic 1.

mechanical data and pin configuration

The TMS 3016 LR is mounted in a TO-100 package. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	No connection	6	V_{GG}
2	Clock ϕ_2	7	Output 2
3	Input 1	8	Clock ϕ_1
4	Input 2	9	Output 1
5	GND (V_{SS})	10	V_{DD}

logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Phase one clock input voltage $V_{\phi 1}$ range (See Note 1)	−30 V to 0.3 V
Phase two clock input voltage $V_{\phi 2}$ range (See Note 1)	−30 V to 0.3 V
Data input voltage V_I range (See Note 1)	−30 V to 0.3 V
Power dissipation	450 mW
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal, V_{SS}.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−15	V
Supply voltage V_{GG}	−24	−28	−29	V
Logic 0 data input voltage $V_{i(0)}$ (See Note 2)	0.3	0	−2	V
Logic 1 data input voltage $V_{i(1)}$ (See Notes 2)	−9.5	−14	−29	V
Width of data pulse, $t_{p(data)}$ (See voltage waveforms)	0.4†			μs
Data setup time, t_{setup} (See voltage waveforms and Note 3)	100			ns
Data hold time, t_{hold} (See voltage waveforms and Note 4)	20			ns
Logic 0 clock input voltage $V_{\phi 0(clock)}$ (See Notes 2 and 5)	0.3	0	−2	V
Logic 1 clock input voltage $V_{\phi 1(clock)}$ (See Notes 2 and 5)	−24	−28	−29	V
Rise time of clock pulse, $t_{r(clock)}$ (See voltage waveforms)		0	5	μs
Fall time of clock pulse, $t_{f(clock)}$ (See voltage waveforms)			5	μs
ϕ_1 clock pulse width, $t_{p(\phi 1)}$ (See voltage waveforms)	0.3†		10†	μs
ϕ_2 clock pulse width, $t_{p(\phi 2)}$ (See voltage waveforms)	0.4†		∞†	μs
Time interval from ϕ_1 clock to ϕ_2 clock input pulse, $t_{\phi 12}$ (See voltage waveforms)	0.01		10	μs
Time interval from ϕ_2 clock to ϕ_1 clock input pulse, $t_{\phi 21}$ (See voltage waveforms)	0.01		10	μs
Clock repetition rate	0		1	MHz

NOTES: 2. These voltage values are with respect to network ground terminal, V_{SS}.
3. Setup time is the interval immediately preceeding the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the phase 1 clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
5. The two clock pulses must never be simultaneously more than 3 volts more negative than V_{SS}.

† These values are at $V_{DD} = -14$ V, $V_{GG} = -28$ V, and $T_A = 25°C$.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNITS
I_{IL}	Logic 1 input current into data input	$V_I = -20$ V, $T° = 25°C$			0.5	μA
$I_{IL(\phi)}$	Logic 1 input current into either clock input	$V_I = -28$ V, $V_{GG} = 0$ V, $T° = 25°C$			50	μA
V_{OH}	Logic 0 output voltage	$I_O = 0$ mA, $C_L = 20$ pF		0.3	−1	V
		$I_O = 2$ mA, $C_L = 20$ pF		−2.6	−5	V
		$I_O = 0$ mA, $V_{DD} = -12$ V, $V_{GG} = -24$ V		−0.5	−1	V
V_{OL}	Logic 1 output voltage	$I_O = 0$ mA, $C_L = 20$ pF	−12.0	−13.5	−14	V
		$I_O = 0.5$ mA	−10.5	−12.5	−14	V
		$I_O = 0$ mA, $V_{DD} = -12$ V, $V_{GG} = -24$ V, $V_\phi, V_{\phi 2} = -24$ V, $C_L = 20$ pF, $V_{in(1)} = -8.5$ V, $V_{in(0)} = -2$ V	−8.8	−10.5	−12	V
R_{OH}	Output resistance, logic 0	$I_O = -2.0$ mA		1.5	2.5	kΩ
R_{OL}	Output resistance, logic 1	$I_O = 0.5$ mA		1.5	7	kΩ
I_{DD}	Supply current from V_{DD} terminal*			−8	−12	mA
I_{GG}	Supply current from V_{GG} terminal*			−1.6	−2.5	mA
f_{max}	Maximum clock frequency		1			MHz

† Unless otherwise noted, voltages are as shown in the nominal column of the recommended operating conditions (nominal operating voltages).
‡ All typical values are at $T_A = 25°C$. * Current into a terminal is a positive value.

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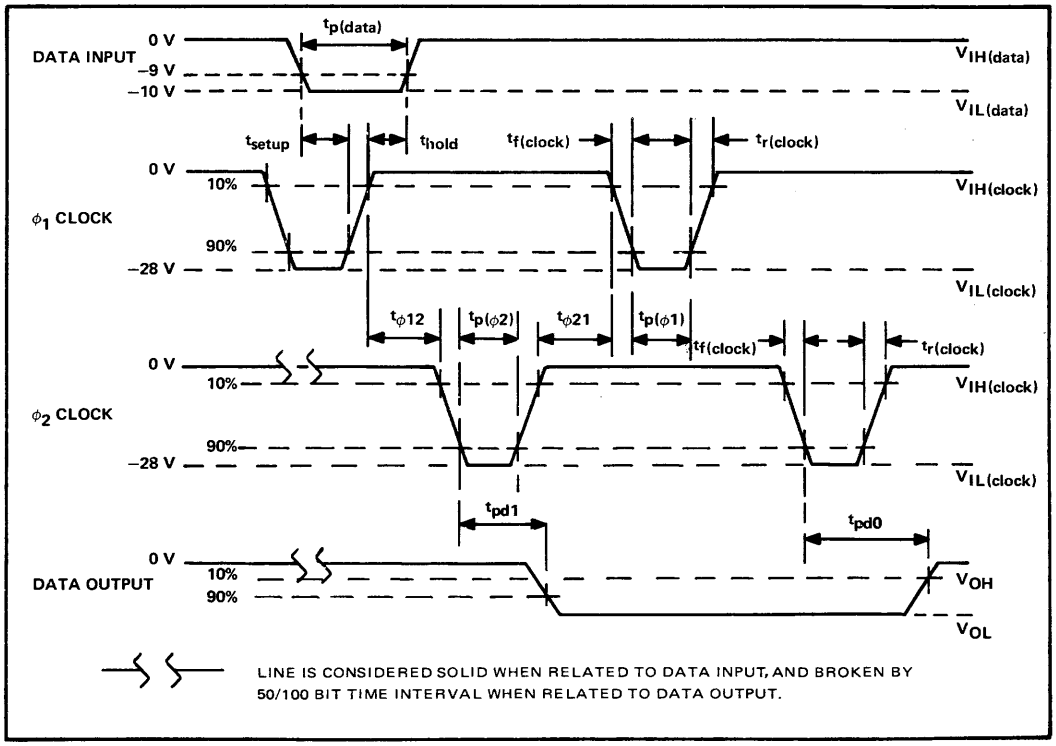
switching characteristics, $V_{DD} = -14$ V, $V_{GG} = -28$ V, $R_L = 10$ mΩ, $C_L = 20$ pF, $T_A = 25°C$

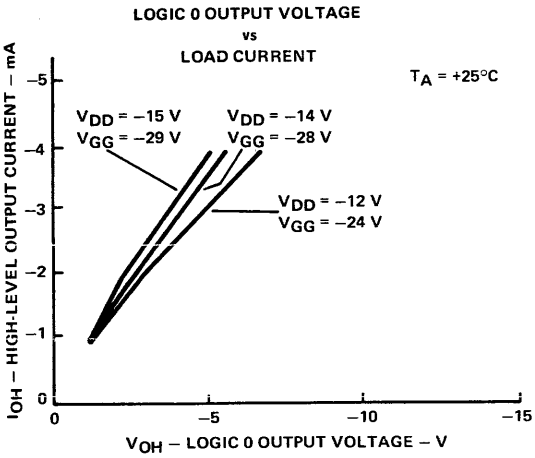
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation delay time to high level from ϕ_2 clock to data output	See voltage waveforms		250	400	ns
t_{pd1}	Propagation delay time to low level from ϕ_2 clock to data output	See voltage waveforms		250	350	ns
$C_{in(\phi1)}$	Capacitance of ϕ_1 clock input	$V_I = 0$ V, $V_{I(\phi2)} = 0$ V, f = 1 MHz		6	10	pF
$C_{in(\phi2)}$	Capacitance of ϕ_2 clock input*	$V_I = 0$ V, $V_{I(\phi1)} = 0$ V, f = 1 MHz		15	20	pF
C_{in}	Capacitance of data input	$V_I = 0$, f = 1 MHz		2	14	pF

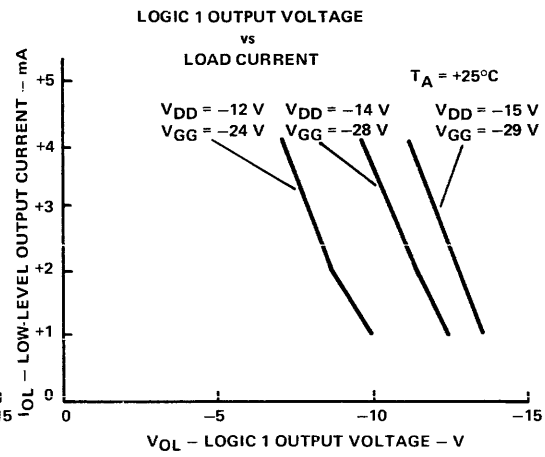
*$C_{in(\phi2)}$ includes the capacitance of the internal ϕ_2 clock.

voltage waveforms



typical characteristics

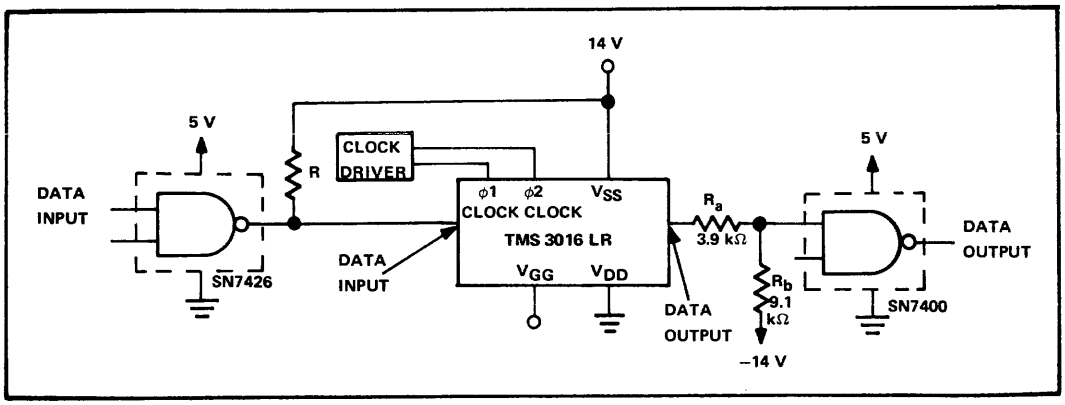




typical applications data

1) MOS/TTL interface

With proper supply voltages, interfacing can be achieved with only three resistors. A typical MOS/TTL interface is shown below.



An input pull-up resistor is required to provide the necessary input voltage swing. The value of this resistor (R) depends on the actual circuit requirements – values as low as 1 kΩ can be used for high-speed operation while values as high as 15 kΩ can be used when low power consumption is important rather than high-speed.

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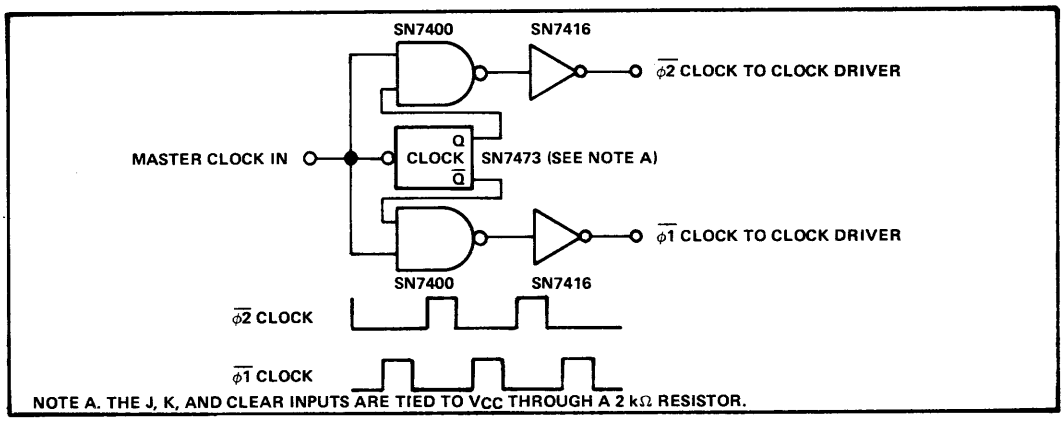
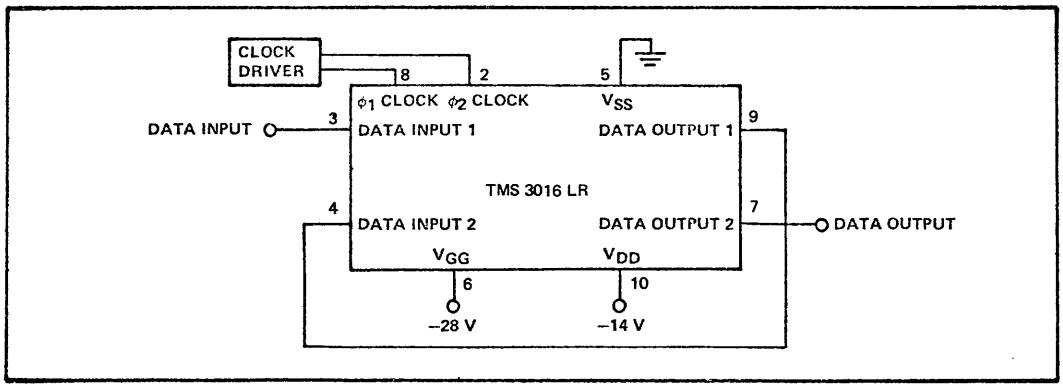
typical applications data (continued)

At the output interface, the 9.1-kΩ resistor sinks the 1.6 mA of TTL-gate current when 0 volts is required on the TTL input. When 3 volts is required on the TTL input, the MOS output device supplies current from 14 volts, through the 3.9 kΩ resistor and the 9.1-kΩ resistor to −14 volts. The 3.9-kΩ resistor limits the voltage at the TTL gate input to 5 volts maximum.

2) Two-phase clock generator



expansion to single 32 register



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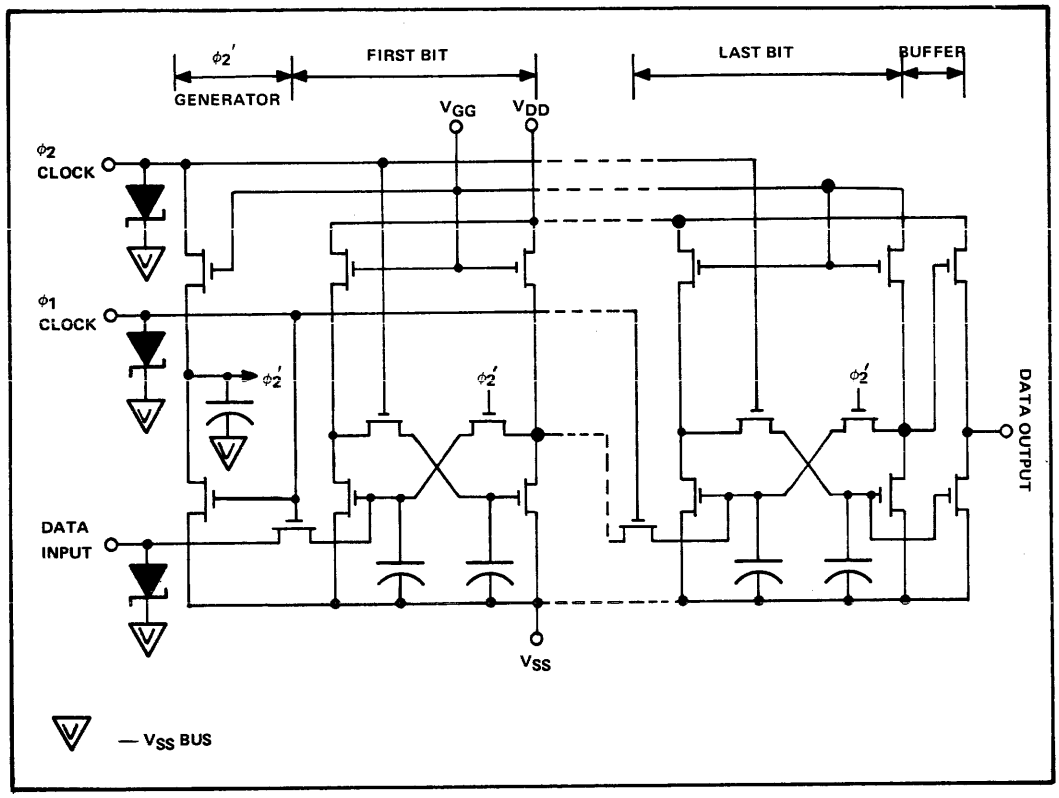
schematic (each register)



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TEXAS INSTRUMENTS
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MOS
LSI

TMS 3101 LC, NC - DUAL 100-BIT STATIC SHIFT REGISTER
TMS 3102 LC, NC - DUAL 80-BIT STATIC SHIFT REGISTER
TMS 3103 LC, NC - DUAL 64-BIT STATIC SHIFT REGISTER

JANUARY, 1971

features

- DC to 2.5-MHz operation
- Low power dissipation
- Direct interface with DTL/TTL
- Static operation
- Push-pull output buffer
- Low-threshold technology

description

The TMS 3101 LC/NC is a dual 100-bit static shift register; the TMS 3102 LC/NC is a dual 80-bit static shift register; and the TMS 3103 LC/NC is a dual 64-bit static shift register. These circuits are constructed on a single monolithic chip using thick-oxide techniques and P-channel enhancement-mode transistors. Each register has independent input and output terminals, common clocks and power, and can operate from dc to 2.5 MHz. The inputs, which are zener protected, can be driven directly from DTL/TTL levels, and the register outputs can drive DTL/TTL circuits without the addition of external components.

The TMS 3100 series is a family of static shift registers, the lengths of which are programmable from 4 to 100 bits, through a single-mask-level change. The 100-, 80-, and 64-bit lengths are available from stock.

Units mounted in 10-lead TO-100 packages are designated "LC". Mounted in 16-pin dual-in-line plastic packages, the devices are designated "NC".

logic definition

Positive logic is assumed.

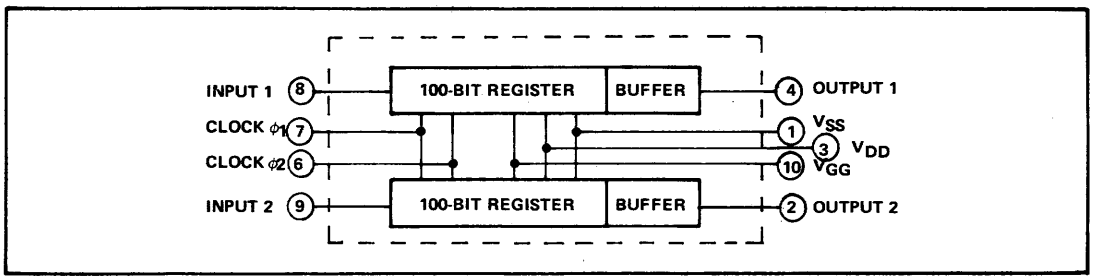
a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between clock pulses. Two external clock pulses are required for operation. Data is transferred into the register when the clock pulse ϕ_1 is at a Low level. Data is shifted when clock pulse ϕ_1 is returned to a High level and clock pulse ϕ_2 is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse ϕ_2. For long-term storage, clock pulse ϕ_1 must be held at a High level and clock pulse ϕ_2 at a Low level.

functional block diagram and pin configuration



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels (Note 2)				
Input High level V_{IH}	+3.5		+5.25	V
Input Low level V_{IL}	−13	−12	0.8	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	+3		+5.25	V
Clock Low level $V_{\phi L}$	−13		−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			3	μs
Clock pulse width 1 (See waveforms) $PW_{\phi 1}$	0.150		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.150		∞	μs
Pulse Spacing				
Clock delay $t_{D\phi 12}$			10	μs
Clock delay $t_{D\phi 21}$			10	μs
Data setup t_{DS}	150			ns
Data hold t_{DH}	10			ns
Pulse Overlap				
Clock (See Note 2)				
Pulse Repetition Rate PRR				
Data (See Note 2)	0		2.5	MHz
Clock (See Note 3)	0		2.5	MHz

NOTES: 2. Both clocks should not be simultaneously more than 2 V below V_{SS}.
3. C_L = 10 pF, one TTL load.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input current	V_I = 0 V, V_{SS} = +5 V			500	μA
$I_{\phi L}$	Clock current	V_I = −12 V, V_{SS} = +5 V			20	μA
Output Voltage Levels						
V_{OL}	Output LOW level	(See Note 4) 1 TTL load			+0.4	V
V_{OH}	Output HIGH level	(See Note 4) 1 TTL load	+3.0	+3.5		V
V_{OL}	Output LOW level	(See Note 4) MOS load (3101)			+0.4	V
V_{OH}	Output HIGH level	(See Note 4) MOS load (3101)	3.6			V

NOTE 4: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and 20 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

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static electrical characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Current						
I_{OSC}	Short circuit				30	mA
Power Supply Current Drain						
I_{SS}	Substrate supply	$V_{out} = V_{OH}$ (See Note 5)		16	20	mA
I_{DD}	Drain supply	See Note 6			0.5	mA
I_{GG}	Gate supply	$V_{out} = V_{OH}$ (See Note 5)		−16	−20	mA
P_D	Power dissipation			270	360	mW

NOTES: 5. The device uses saturated logic. The current sourced by the 5-V power supply is sunk by the −12-V power supply.

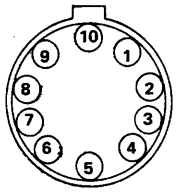
6. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current. In the TTL load mode the current is the current sunk by the TTL (up to 1.6 mA).

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DLH_1}	Output LOW level	C_L = 10 pF,	TTL gate load		50	75	ns
t_{DHL_1}	Output HIGH level	C_L = 10 pF,	TTL gate load		100	125	ns
t_{DLH_2}	Output HIGH level	C_L = 10 pF,	MOS load		60	85	ns
t_{DHL_2}	Output LOW level	C_L = 10 pF,	MOS load		120	150	ns
Capacitance							
C_{IN}	Input	V_I = 0 V,	f = 1 MHz		9	12	pF
C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		48	55	pF

mechanical data and pin configuration

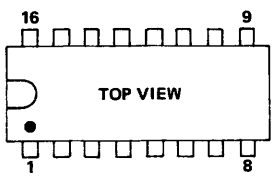
Units mounted in 10-lead TO-100 packages are designated "LC" (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	V_{SS}	6	Clock ϕ_2
2	Output 2	7	Clock ϕ_1
3	V_{DD}	8	Input 1
4	Output 1	9	Input 2
5	No connection	10	V_{GG}

Mounted in 16-pin dual-in-line plastic packages, the devices are designated "NC" The package is designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	ϕ_2	9	V_{SS}
2	No connection	10	No connection
3	ϕ_1	11	No connection
4	Input 1	12	Output 2
5	Input 2	13	V_{DD}
6	No connection	14	Output 1
7	No connection	15	No connection
8	V_{GG}	16	No connection

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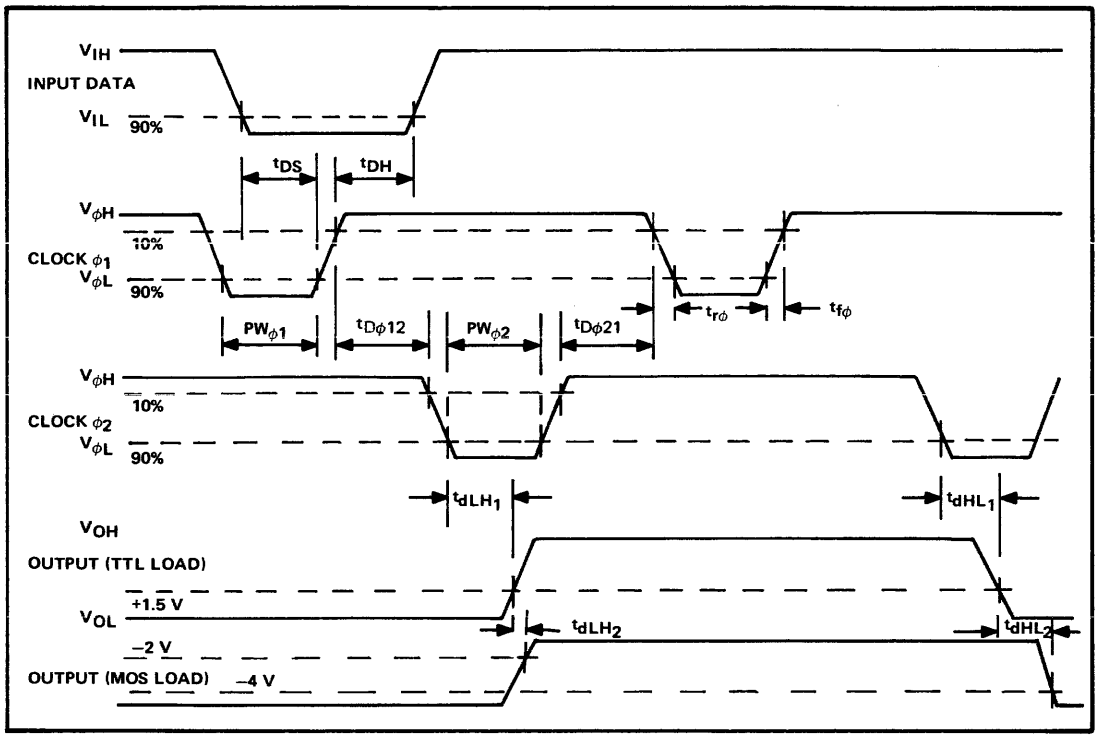
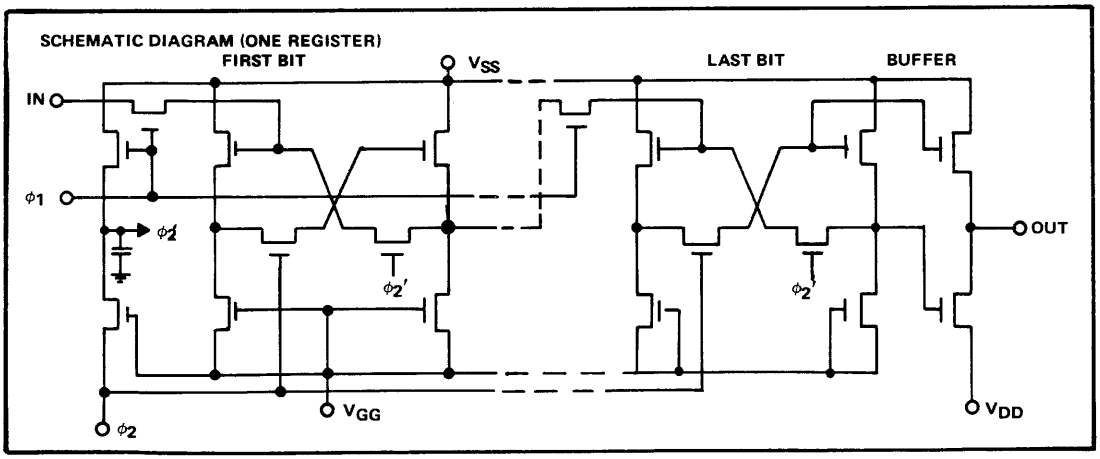
timing diagram and voltage waveforms



circuit diagram



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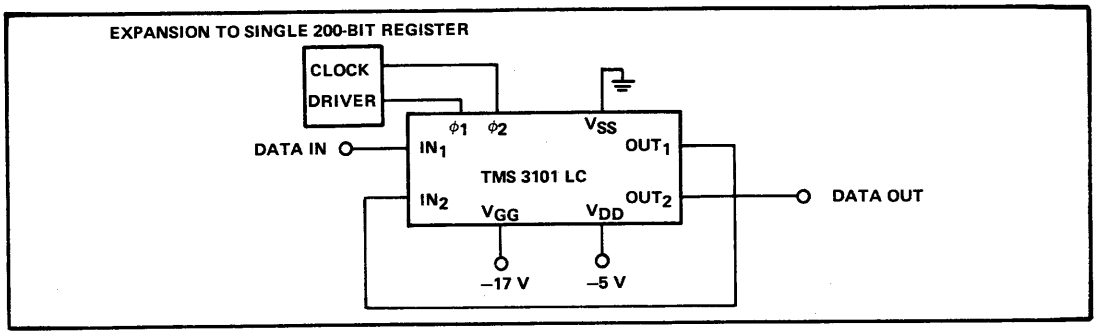
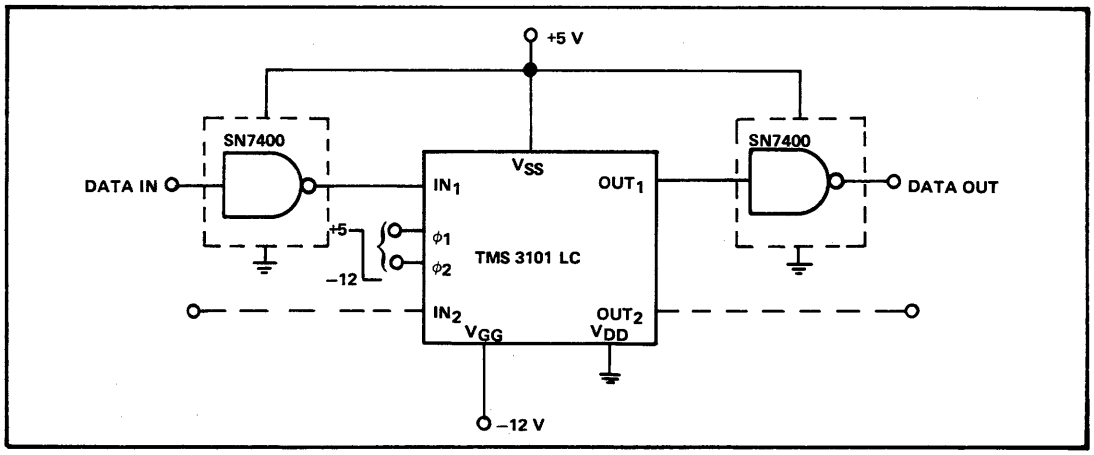
interface circuits

a) MOS



b) TTL



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TMS 3112 JC, TMS 3112 NC
HEX 32-BIT STATIC SHIFT REGISTER

JANUARY, 1971

features

- Single clock (TTL levels)
- DTL/TTL compatible
- DC to 1 MHz
- Static operation
- Loading and recirculating control logic
- Gated-output control logic
- Dual-in-line package
- Single-ended (open drain) buffer
- Low-threshold technology

description

The TMS 3112 JC/NC contains six separate 32-bit static shift registers constructed on a single monolithic chip, using thick-oxide techniques and P-channel enhancement-mode low-threshold MOS transistors.

A single clock is required for operation. The clock and all inputs can be driven directly from DTL/TTL logic levels and each register output can drive DTL/TTL circuits. The device also contains common control logic for loading, recirculation, and output enable.

"TMS 3112 JC" is the part number for a unit mounted in a 24-pin hermetically sealed dual-in-line package. Mounted in a 24-pin plastic package the device is numbered "TMS 3112 NC".

logic definition

Positive logic is assumed.

a) Logic 1 = most positive (High) voltage

b) Logic 0 = most negative (Low) voltage

operation

Cross-coupled flip-flops are used to implement each register bit and permit data to be stored indefinitely between internal clock pulses. A single external clock pulse is required for operation. Data is transferred into the register when the clock pulse and recirculate control are at a Low level. Output data appears on the Low-to-High transition of the clock pulse. Data can be read out when the output gate control is held at a Low level. Recirculating data occurs when the recirculation control is at a High level.

The registers can drive DTL/TTL loads by using a 7.5-kΩ pull-down resistor connected between the output terminal and the V_{GG} supply.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{GG} range (See Note)	−20 V to 0.3 V
Clock input voltage range (See Note)	−20 V to 0.3 V
Data input voltage range (See Note)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE: These voltage values are with respect to V_{SS} (substrate).

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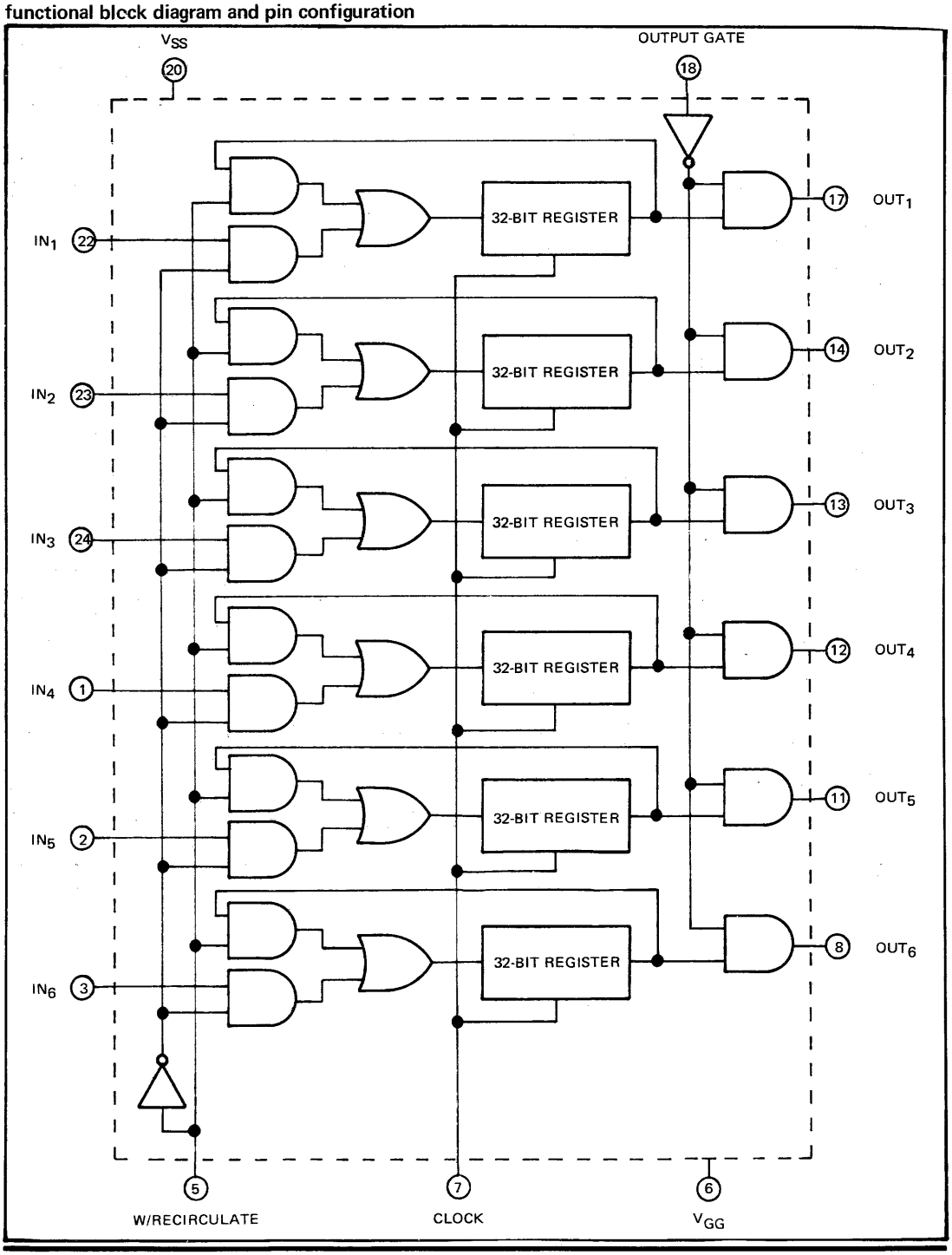
functional block diagram and pin configuration



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recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Gate supply V_{GG}	−11	−12	−13	V
Input High level V_{IH}	+3.5			V
Input Low level V_{IL}			+0.6	V
Clock High level $V_{\phi H}$	+3.5			V
Clock Low level $V_{\phi L}$			+0.6	V
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5000	ns
Clock High level $PW_{\phi H}$	600			ns
Clock Low level $PW_{\phi L}$	300			ns
Recirculate PW_s	600			ns
Output gate hold time t_{DGS}		180	250	ns
Output gate release time t_{DGR}		180	250	ns
Data setup t_{DS}	300			ns
Data hold t_{DH}	300			ns
Clock to store/recirculate t_{DCS}	300			ns
Clock PRR	0		1	MHz

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current	V_I = +0.6 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current	V_ϕ = +0.6 V,	V_{SS} = +5 V			500	nA
V_{OL}	Output Low level	R_L = 7.5 kΩ to V_{GG},	I_{sink} = 1.6 mA			+0.5	V
V_{OH}	Output High level	R_L = 7.5 kΩ to V_{GG}		+4			V
I_{SS}	Substrate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
I_{GG}	Gate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15	20	mA
P_D	Power dissipation				255	340	mW
t_{dLH}	Output Low level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	450	600	ns
t_{dHL}	Output High level	R_L = 7.5 kΩ,	C_L = 10 pF, TTL gate	350	500	600	ns
C_{IN}	Input	V_I = 0 V,	f = 1 MHz		5	7	pF
C_ϕ	Clock	V_I = 0 V,	f = 1 MHz		6	7	pF

mechanical data and pin configuration

The device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 3112 JC) and a 24-pin plastic package (TMS 3112 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

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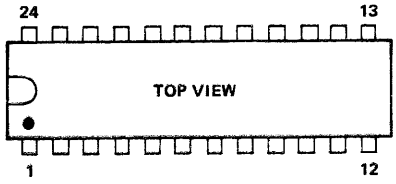
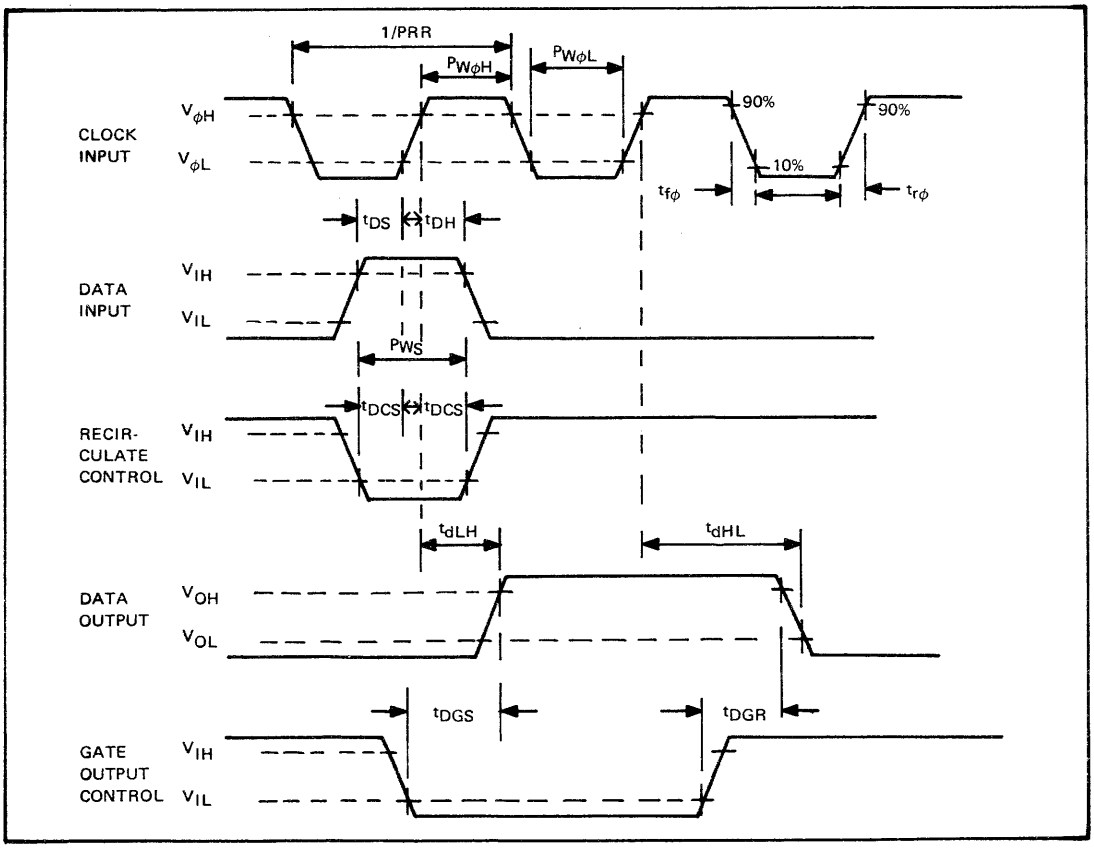
mechanical data and pin configuration (continued)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input 4	13	Output 3
2	Input 5	14	Output 2
3	Input 6	15	No connection
4	No connection	16	No connection
5	W/Recirculate Cont.	17	Output 1
6	V_{GG}	18	Output gate Cont.
7	Clock	19	No connection
8	Output 6	20	V_{SS}
9	No connection	21	No connection
10	No connection	22	Input 1
11	Output 5	23	Input 2
12	Output 4	24	Input 3

timing diagram and voltage waveforms



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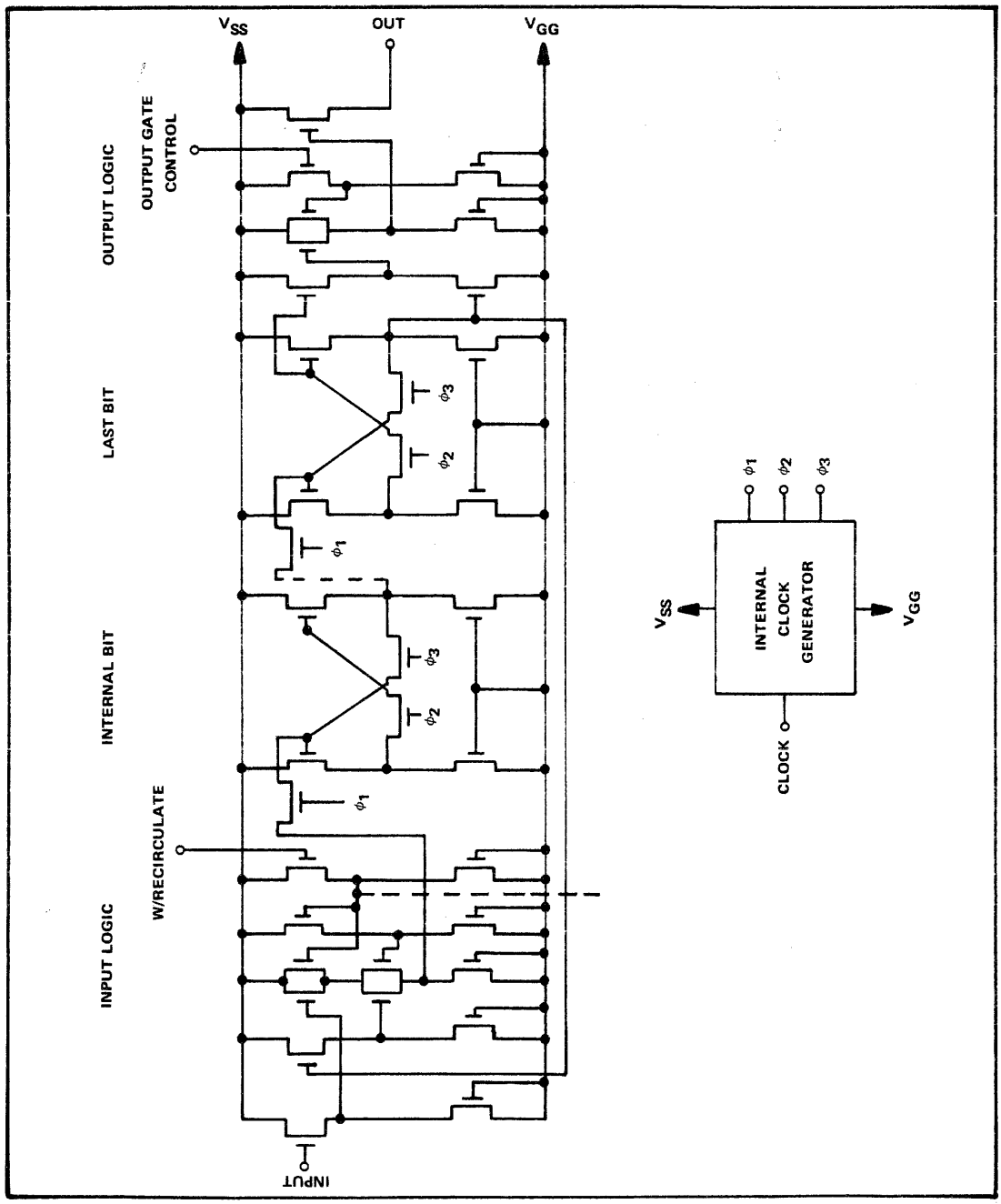
circuit diagram



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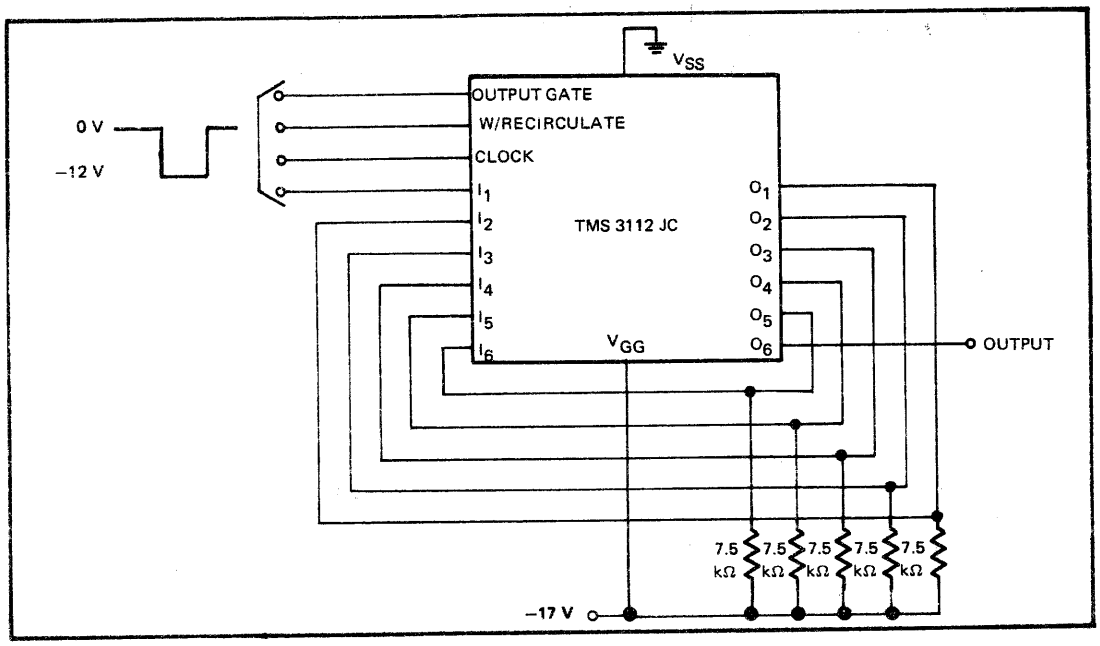
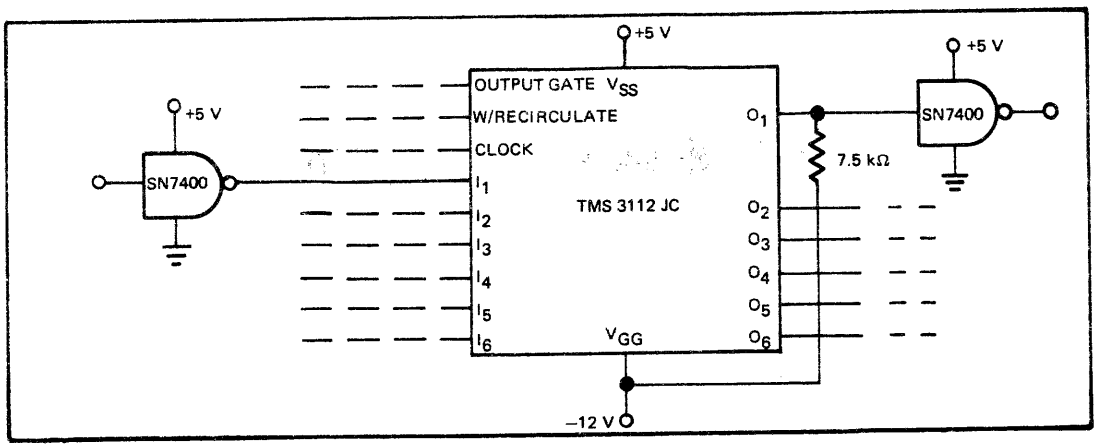
interface circuits

a) MOS



b) TTL



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MOS
LSI

TMS 3113 JC, NC - DUAL 133-BIT STATIC ACCUMULATOR
TMS 3114 JC, NC - DUAL 128-BIT STATIC ACCUMULATOR

features

- Single-clock TTL level
- Loading and recirculate logic
- DC to 2-MHz operation
- Full TTL compatible (including clock)
- Static logic
- 16-pin dual-in-line package
- Low-threshold technology

description

The TMS 3113 JC/NC and TMS 3114 JC/NC are static accumulators, each consisting of two separate static shift registers with independent input and output terminals and logic for loading or recirculating information. The two shift registers in the TMS 3113 JC/NC are 133-bit devices. Two 128-bit shift registers compose the TMS 3114 JC/NC.

A single clock is required for operation. The clock and all inputs can be driven directly from DTL/TTL logic levels and each register output can drive DTL/TTL circuits. Three clocks are generated internally. Cross-coupled flip-flops are used to implement each bit of delay and enable data to be stored indefinitely between clock pulses.

The entire device is constructed on a single monolithic chip using thick-oxide techniques and low-threshold MOS P-channel enhancement-mode transistors.

Units mounted in 16-pin hermetically sealed ceramic dual-in-line packages are designated "JC". "NC" is the designation for units in 16-pin dual-in-line plastic packages.

logic definition

Positive logic is assumed.

a) LOGIC 1 = most positive voltage (high)

b) LOGIC 0 = most negative voltage (low)

operation

Transferring data into the register is accomplished when the clock and recirculate control are at logic 0. For long-term data storage the clock must be held at a logic 1.

Recirculate occurs when the recirculate control is at a logic 1. Output data appears on the 0-to-1 transition of the clock pulse.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−6 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−15 V to 0.3 V
Data input voltage range (See Note 1)	−15 V to 0.3 V
Operating free-air temperature range	−25°C to +85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

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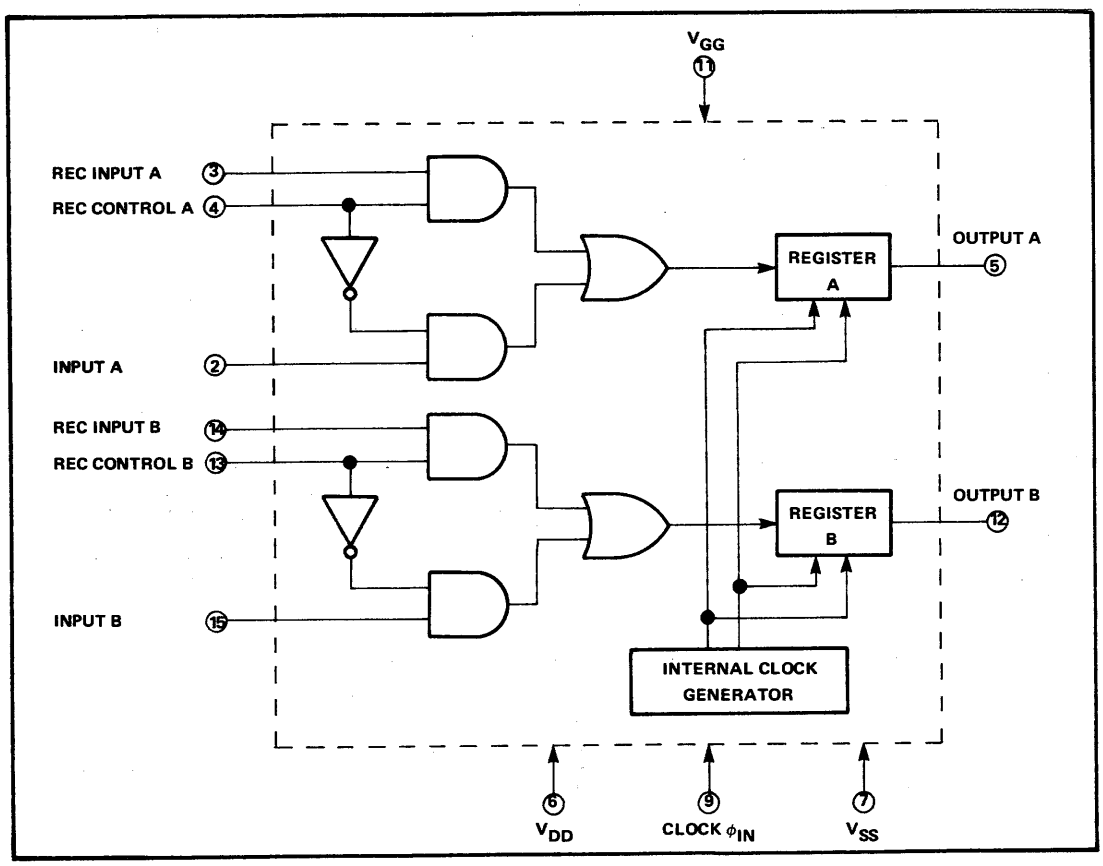
functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Drain Supply V_{DD} (Output supply only)		0		V
Gate supply V_{GG}	−11	−12	−13	V
Logic Levels				
Input High level V_{IH}	+3.5			V
Input Low level V_{IL}			+0.6	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	+3.5			V
Clock Low level $V_{\phi L}$			+0.6	V

— continued

recommended operating conditions (continued)

PARAMETER	MIN	NOM	MAX	UNITS
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5	μs
Clock pulse width PW_{ϕ} (Clock cycle time)	500			ns
Clock pulse width High level $PW_{\phi H}$	330			ns
Clock pulse width Low level $PW_{\phi L}$	130			ns
Recirculate PW_R	250			ns
Pulse Spacing				
Data setup t_{DB}	100			ns
Data hold t_{DA}	100			ns
Clock to store/recirculate t_{RB}	100			ns
Clock to store/recirculate t_{RA}	150			ns
Pulse Repetition Rate PRR				
Data	0		2.0	MHz
Clock	0		2.0	MHz

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_I = +0.6 V				500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = +0.6 V				500	nA
Output Voltage Levels (See Note 2)							
V_{OL}	Output LOW level	I_{SINK} = 1.6 mA				+0.5	V
V_{OH}	Output HIGH level	I_{LOAD} = 0.20 mA		+4.0			V
Power Supply Current Drain							
I_{SS}	Substrate supply	V_{SS} = +5 V,	V_{GG} = −12 V		15		mA
I_{GG}	Gate supply	V_{SS} = +5 V,	V_{GG} = −12 V		17		mA
P_D	Power Dissipation	V_{SS} = +5 V,	V_{GG} = −12 V		280		mW

NOTE 2: For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and 20 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

dynamic electrical characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DL}	Output Low level	C_L = 10 pF,	TTL gate		300	350	ns
t_{DH}	Output High level	C_L = 10 pF,	TTL gate		300	350	ns
Capacitance							
C_{IN}	Input	V_I = 0 V,	F = 1.0 MHz		8	12	pF
C_{ϕ}	Clock	V_I = 0 V,	F = 1.0 MHz		9	13	pF

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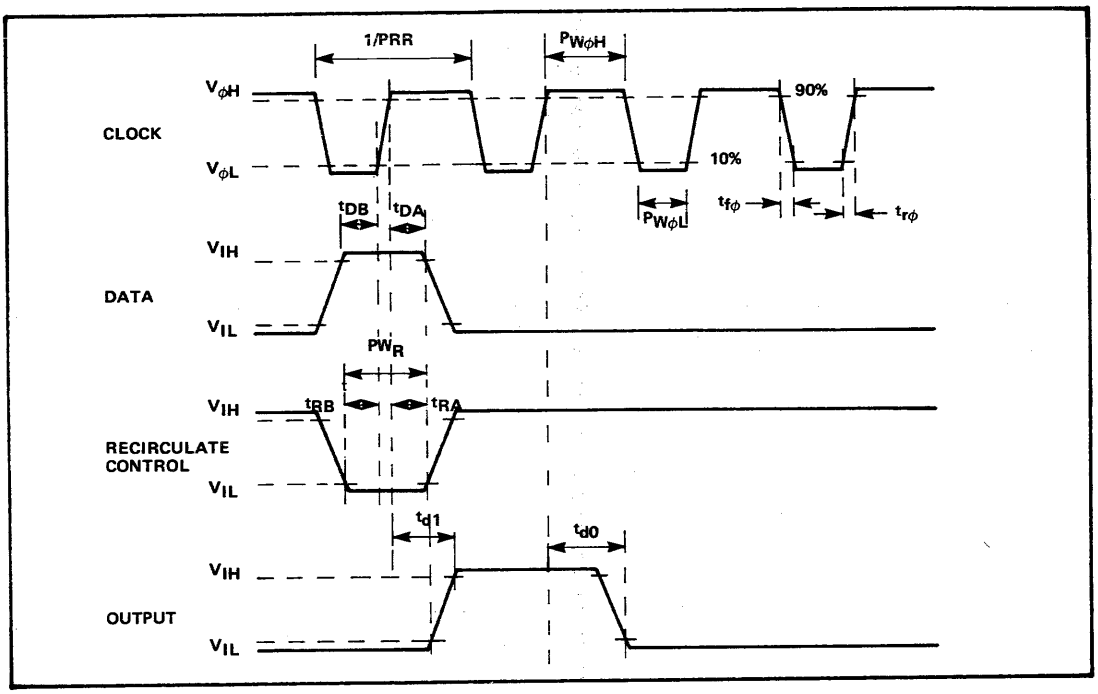
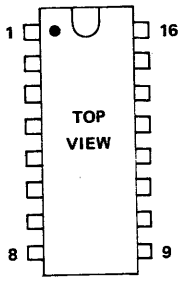
timing diagram and voltage waveforms



mechanical data

The devices are available both in 16-pin hermetically sealed ceramic dual-in-line package (TMS 3113 JC, TMS 3114 JC) and in 16-pin dual-in-line plastic packages (TMS 3113 NC, TMS 3114 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	16	No connection
2	Input A	15	Input B
3	Recirculate Input A	14	Recirculate Input B
4	Recirculate Control A	13	Recirculate Control B
5	Output A	12	Output B
6	V_{DD}	11	V_{GG}
7	V_{SS}	10	No connection
8	No connection	9	Clock ϕ_{IN}

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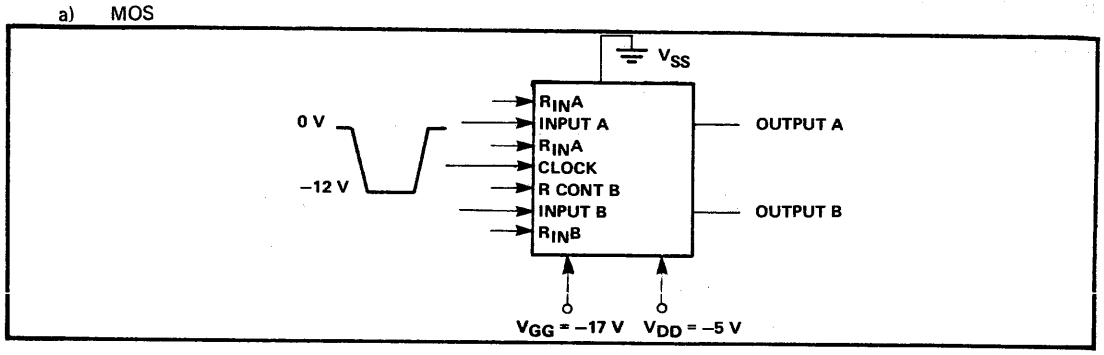
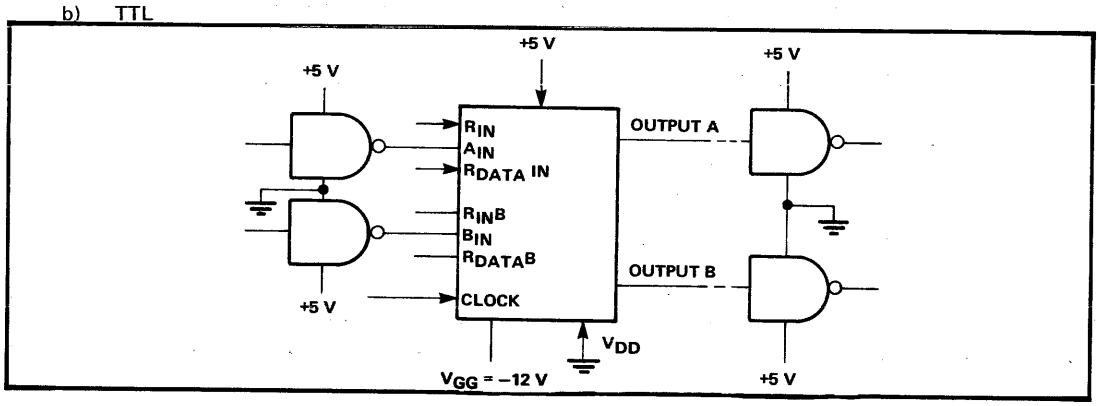
TMS 3113 JC, NC - DUAL 133-BIT STATIC ACCUMULATOR
TMS 3114 JC, NC - DUAL 128-BIT STATIC ACCUMULATOR

interface circuits

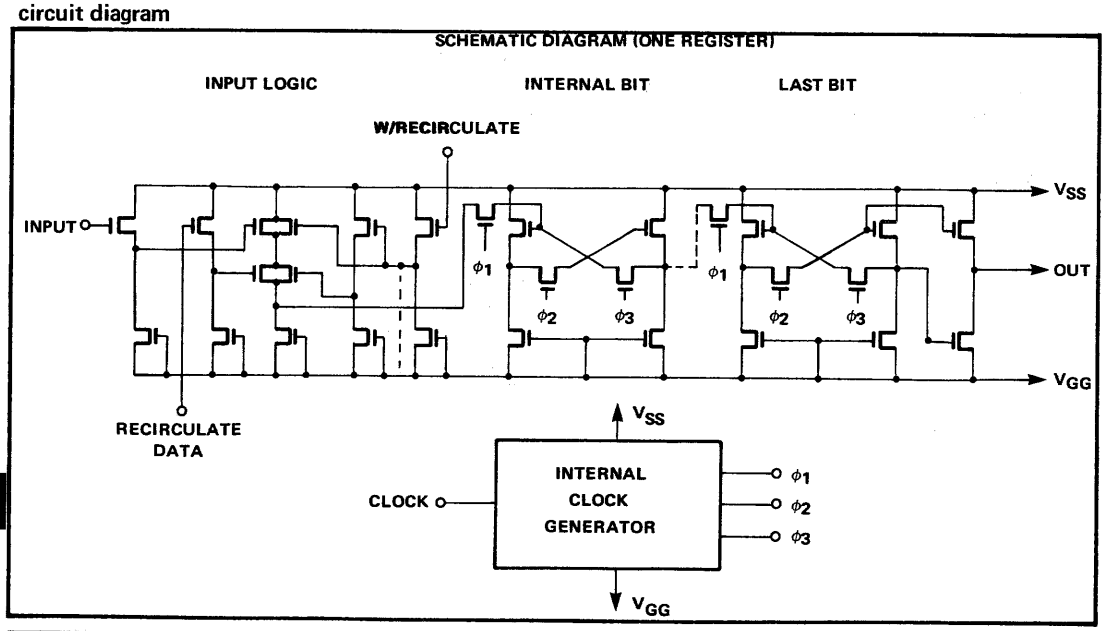
a) MOS



b) TTL



circuit diagram



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MOS
LSI

TMS 3304 LR - TRIPLE 66-BIT DYNAMIC SHIFT REGISTER
TMS 3305 LR - TRIPLE 64-BIT DYNAMIC SHIFT REGISTER

JANUARY 1971

features

- 5-MHz operation
- TTL compatibility
- Single-ended (open-drain) output buffers
- Low power dissipation

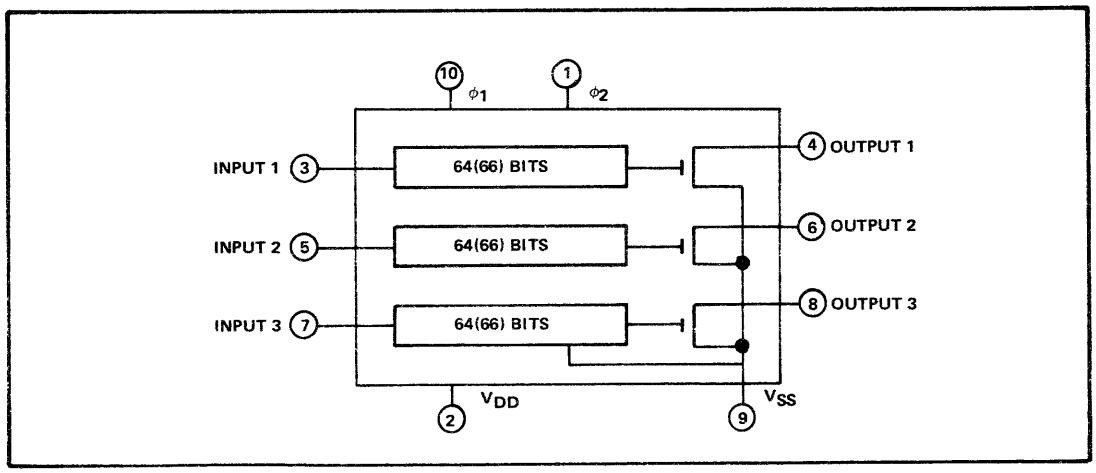
description

The TMS 3304 LR (TMS 3305 LR) consists of three separate 66(64) bit dynamic shift registers with independent input and output terminals and common clocks, power and ground. The gate capacitance of an MOS transistor is used for temporary storage of information between clock pulses. Each register has an unclocked single-ended output buffer to provide an output inverted from the input. The output level is determined by the external load resistor and load power supply.

operation

Transfer of data into the register is accomplished when the ϕ_1 clock is at a logic 1. Data shifting occurs when the ϕ_2 clock is momentarily pulsed to a logic 1, and the ϕ_1 clock to a logic 0. Output data appears on the negative going edge of the ϕ_2 clock pulse.

functional block diagram



logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

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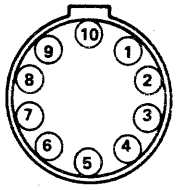
mechanical data and pin configuration

The TMS 3304 LR and TMS 3305 LR are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Clock ϕ_2	6	Out_2
2	V_{DD}	7	In_3
3	In_1	8	Out_3
4	Out_1	9	V_{SS}
5	In_2	10	Clock ϕ_1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_0 range (See Note 1) . . . . . −30 V to 0.3 V
Clock and data input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Power dissipation . . . . . 350 mW at T_A = 25°C
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−18	V
Supply voltage V_0	−5	−14	−29	V
Clock logic 0 voltage $V_{\phi(0)}$	0.3	0	−3	V
Clock logic 1 voltage $V_{\phi(1)}$	−20	−28	−29	V
Data logic 0 voltage $V_{in(0)}$	0.3	0	−3	V
Data logic 1 voltage $V_{in(1)}$	−8	−14	−29	V
Clock Overlap voltage (See Figure)			−3	V
Clock pulse width, t_p $V_{\phi 1}$ = −24 V V_{DD} = −12 V	0.1		50	μs
Clock pulse width, t_p V_ϕ = −28 V, V_{DD} = −14 V	0.08		50	μs
Data pulse width P_W	0.15			μs
Clock delay time, t_d (See Voltage Waveforms)			200	μs
Clock rise and fall times, t_r, t_f (See Voltage Waveforms)			5	μs
Clock repetition rate†	0.002	2	5	MHz
Data lead time, t_b (See Voltage Waveforms)	0.08			μs
Data delay time, t_a (See Voltage Waveforms)	0.01			μs

† V_{DD} = −14 V, $V_{\phi(1)}$ = −28 V, normal or extended with TTL output interface.

Nominal values of power supply and clock swing will result in maximum speed of operation. The device has been designed to operate over a broad range that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0 V, −12 V).

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electrical characteristics at 25°C and nominal operating conditions unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{out}	Output voltage level logic 0 (V_ϕ between −20 V and −30 V)	V_0 = −14 V, R_L = 10 kΩ		−0.8	−1.2	V
$V_{(1)}$	Output voltage level logic 1 (See Note 1)	V_0 = −14 V, R_L = 10 kΩ	−9.0			V
$I_{out(1)}$	Output current logic 1	V_{out} = −14 V, V_ϕ = −28 V V_{out} = −12 V, V_ϕ = −24 V	8 5	12 10		mA mA
I_{dd}	Power supply current drain	V_{DD} = −14 V, V_ϕ = −28 V 20% clock duty cycle V_{DD} = −12 V, V_ϕ = −26 V 20% clock duty cycle		6 5	12 10	mA mA
$I_{\phi L}$	Clock leakage current	$V_{in\phi}$ = −28 V			10	μA
I_{in}	Input leakage current	V_{in} = −28 V			0.5	μA
	Power dissipation			100	350	mW

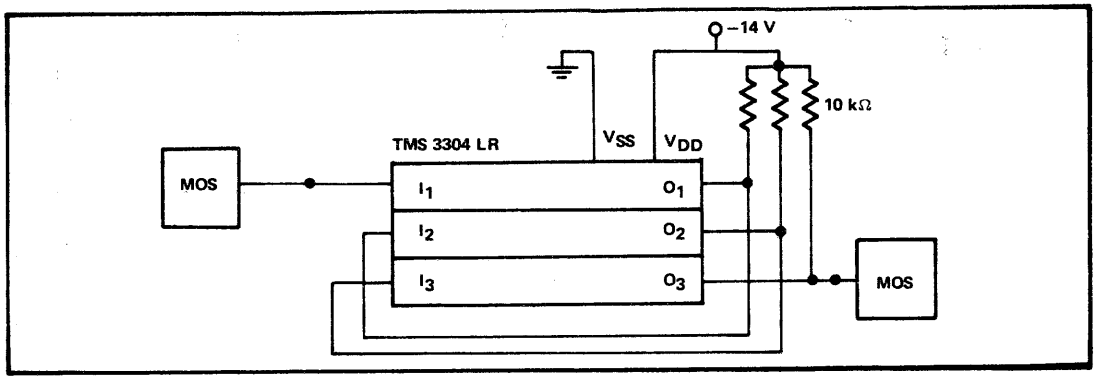
NOTE 1: For an output logic 1 the single ended MOS buffer transistor is "off" and the output voltage is equal to this output voltage power supply V_0.

dynamic electrical characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{d0}	Output logic delay MOS interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		60	150	ns
t_{d1}	Output logic delay MOS interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		120	250	ns
t_{d0}	Output logic delay TTL interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		50	100	ns
t_{d1}	Output logic delay TTL interface (See voltage waveforms)	R_L = 10 kΩ, C_L = 20 pF		60	120	ns
C_I	Data input capacitance	V_I = 0 V		5		pF
C_ϕ	Clock input capacitance	V_ϕ = 0 V		45		pF

interface circuits

a) MOS



To demonstrate MOS interface the register has been connected as a 198-bit shift register.

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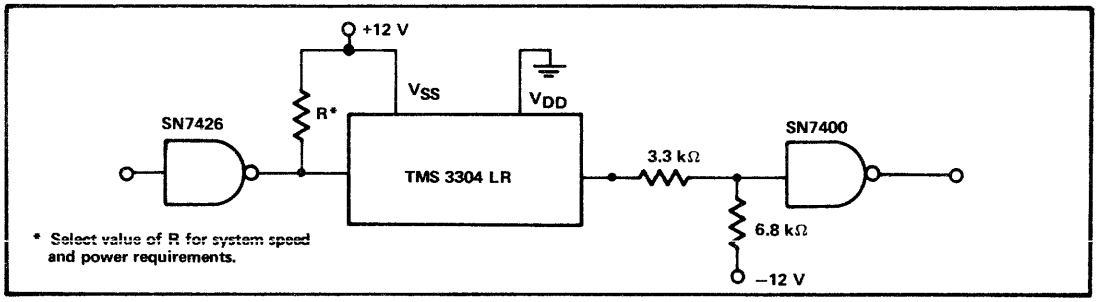
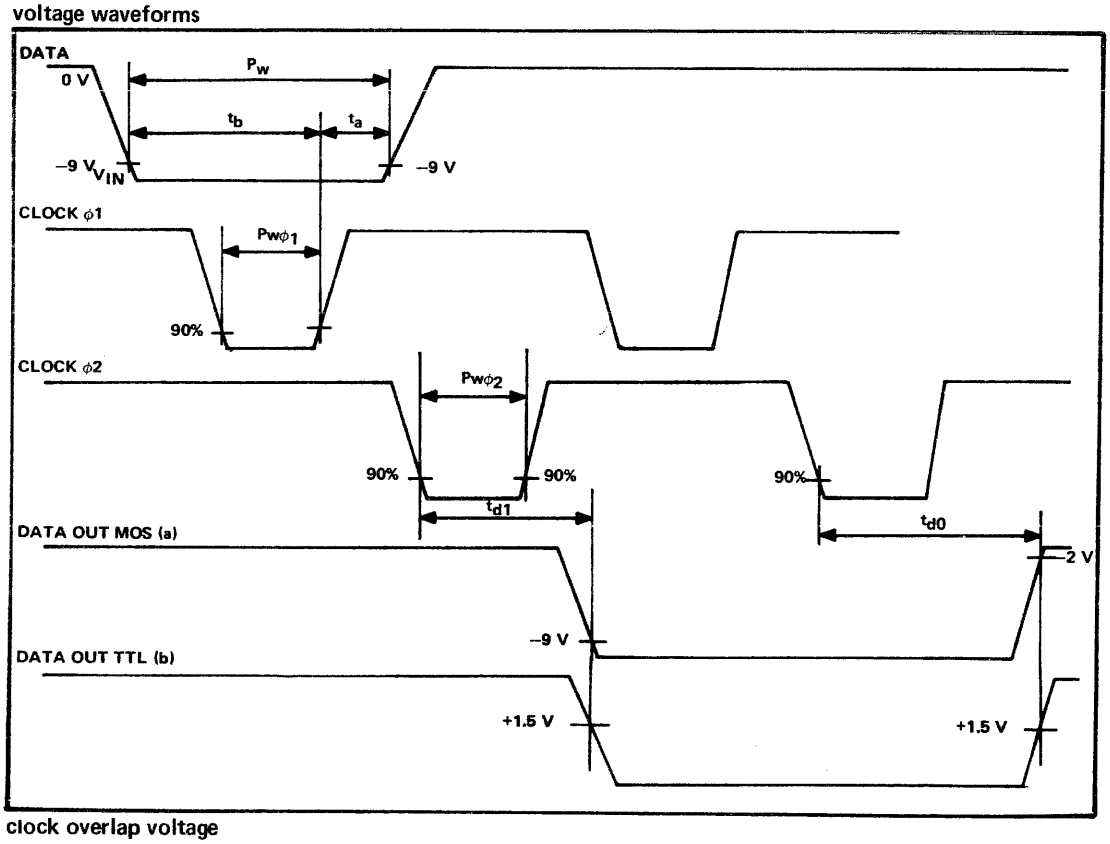
interface circuits (continued)

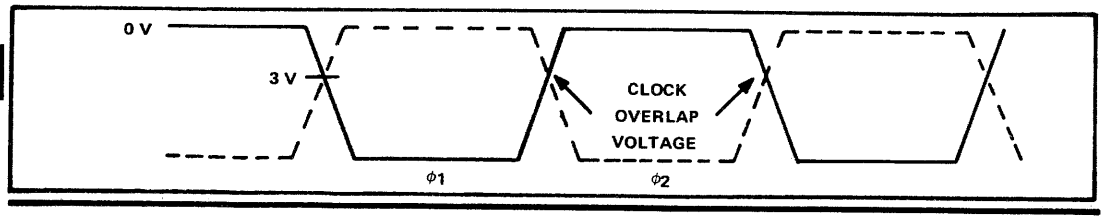
b) TTL



voltage waveforms



clock overlap voltage



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TMS 3309 JC
TWIN 512-BIT DYNAMIC SHIFT REGISTER/ACCUMULATOR

JANUARY, 1971

features

- Two independent registers/accumulators
- 10-MHz guaranteed operating frequency
- Low power dissipation (typical 90 μW/bit at 1 MHz)
- TTL/DTL compatible
- Recirculate logic on the chip

description

The TMS 3309 JC is a twin 512-bit 4-phase dynamic shift register/accumulator, constructed on a monolithic chip, using thick-oxide P-channel enhancement mode transistors. The device contains two separate register/accumulators with independent control logic for recirculating information, and separate clock lines. The register/accumulators operate at pulse repetition rates from 10 kHz to 5 MHz. A 10-MHz speed of operation is obtained by multiplexing the two registers. Power dissipation is less than 100 μW/bit at 1 MHz.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

operation

Four clocks are required for operation of the register/accumulators. Input data is transferred into the register after the end of clock pulse ϕ_1 and before the end of clock pulse ϕ_2. True output data appears after the end of clock pulse ϕ_4 and before the start of the next ϕ_4 clock pulse. Recirculate control is functional when the store pulse overlaps the trailing edge of clock pulse ϕ_3.

The registers may be connected in cascade without external components. The circuit will interface with TTL/DTL and other bipolar logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Clock input voltage range (See Note 1)	−30 V to 0.3 V
Data input voltage range (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

mechanical data

The TMS 3309 JC is mounted in a 16-pin hermetically sealed dual-in-line package consisting of a ceramic base, gold-plated cap, and gold-plated leads. The package is designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

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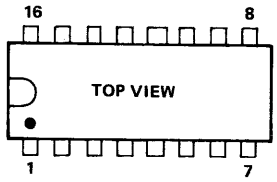
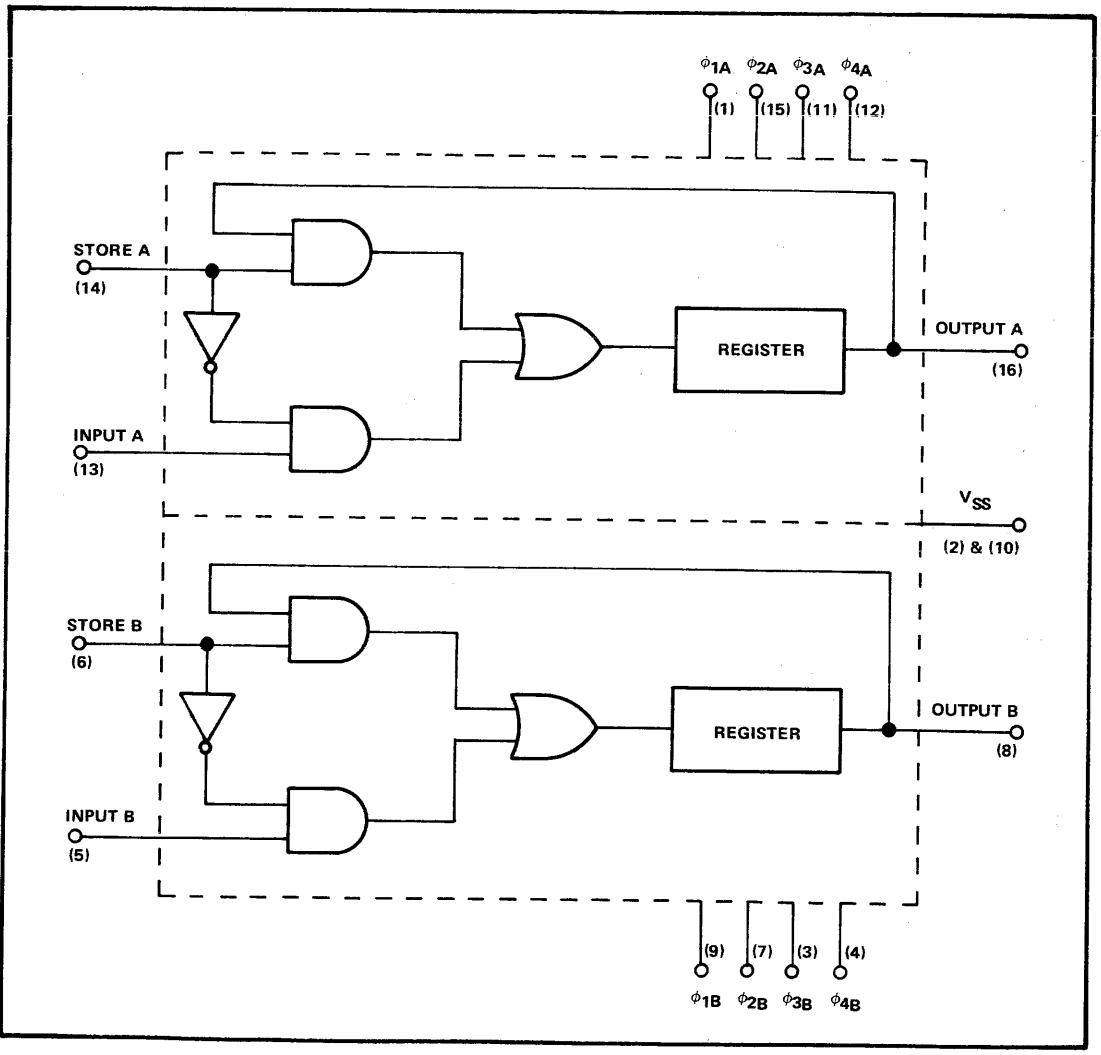
TMS 3309 JC
TWIN 512-BIT DYNAMIC SHIFT REGISTER/ACCUMULATOR

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	ϕ_1 A	9	ϕ_1 B
2	V_{SS}	10	V_{SS}
3	ϕ_3 B	11	ϕ_3 A
4	ϕ_4 B	12	ϕ_4 A
5	IN B	13	IN A
6	REC B	14	REC A
7	ϕ_2 B	15	ϕ_2 A
8	OUT B	16	OUT A

functional block diagram



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TEXAS INSTRUMENTS
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recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Logic Levels					
Store and Input Logic 0 $V_{IN(0)}$		+0.3	0	−3.0	V
Store and Input Logic 1 $V_{IN(1)}$		−9	−12	−26	V
Clock Voltage Levels					
Clock Low Logic Level $V_{\phi(0)}$		0.3	0	−2	V
Clock High Logic Level $V_{\phi(1)}$		−22	−24	−26	V
Pulse Timing					
Clock pulse transition, $t_{r\phi}$, $t_{f\phi}$				10	μs
Clock pulse width 1 $PW_{\phi1}$	V_ϕ = −24 V	25			ns
Clock pulse width 2 $PW_{\phi2}$	V_ϕ = −24 V	75		25000	ns
Clock pulse width 3 $PW_{\phi3}$	V_ϕ = −24 V	25			ns
Clock pulse width 4 $PW_{\phi4}$	V_ϕ = −24 V	75		25000	ns
Store PW_S		50			ns
Pulse Spacing					
Clock delay $t_{D\phi23}$	V_ϕ = −24 V	0		25	μs
Clock delay $t_{D\phi41}$	V_ϕ = −24 V, C_L = 10 pF	0		25	μs
Data setup t_{DS}		10			ns
Data hold t_{DH}		10			ns
Store/recirculate setup t_{DCS}		30			ns
Store recirculate hold t_{DCH}		30			ns
Pulse Overlap (See Note 2)					
Clock − Clock $t_{D\phi12}$, $t_{D\phi34}$	V_ϕ = −24 V	60		10000	ns
Pulse Repetition Rate (See Note 3)					
Data PRR	V_ϕ = −24 V	0.01		5	MHz
Clock PRR	V_ϕ = −24 V	0.01		5	MHz

NOTES: 2. Only clock pulse pairs ϕ_1, ϕ_2 or pairs ϕ_3, ϕ_4 may be simultaneously more than 2 volts below V_{SS}.
3. The maximum operating frequency pertains to each shift register operated independently. If multiplexing is used, double the maximum operating frequency.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_L	Input Current (Leakage)	V_I = −20 V			500	nA
ϕ_L	Clock Current (Leakage)	V_{IN} = −26 V, Output Open			100	μA
Output Voltage Levels						
$V_{OUT(0)}$	Output Level (0)	$V_{\phi(0)}$ = −1.5 V, $V_{IN(0)}$ = −3.5 V		1.5	2.5	V
$V_{OUT(1)}$	Output Level (1)	$V_{\phi(1)}$ = −22 V, $V_{IN(1)}$ = −9 V	−10	−16		V
Power Dissipation/Bit		PRF = 1 MHz, V_ϕ = −24 V, C_L = 10 pF		90		μW
Output Logic Delay						
$t_{D(1)}$	Output Logical 1 Level				0	ns
$t_{D(0)}$	Output Logical 0 Level				20	ns
Capacitance (See Note 4)						
C_{IN}	Input	V_ϕ = 0 V		5		pF
C_ϕ	Clock $C_{\phi1} = C_{\phi3}$	V_ϕ = 0 V		90		pF
C_ϕ	Clock $C_{\phi2} = C_{\phi4}$	V_ϕ = 0 V		40		pF

NOTE 4: The capacitance pertains to each register.

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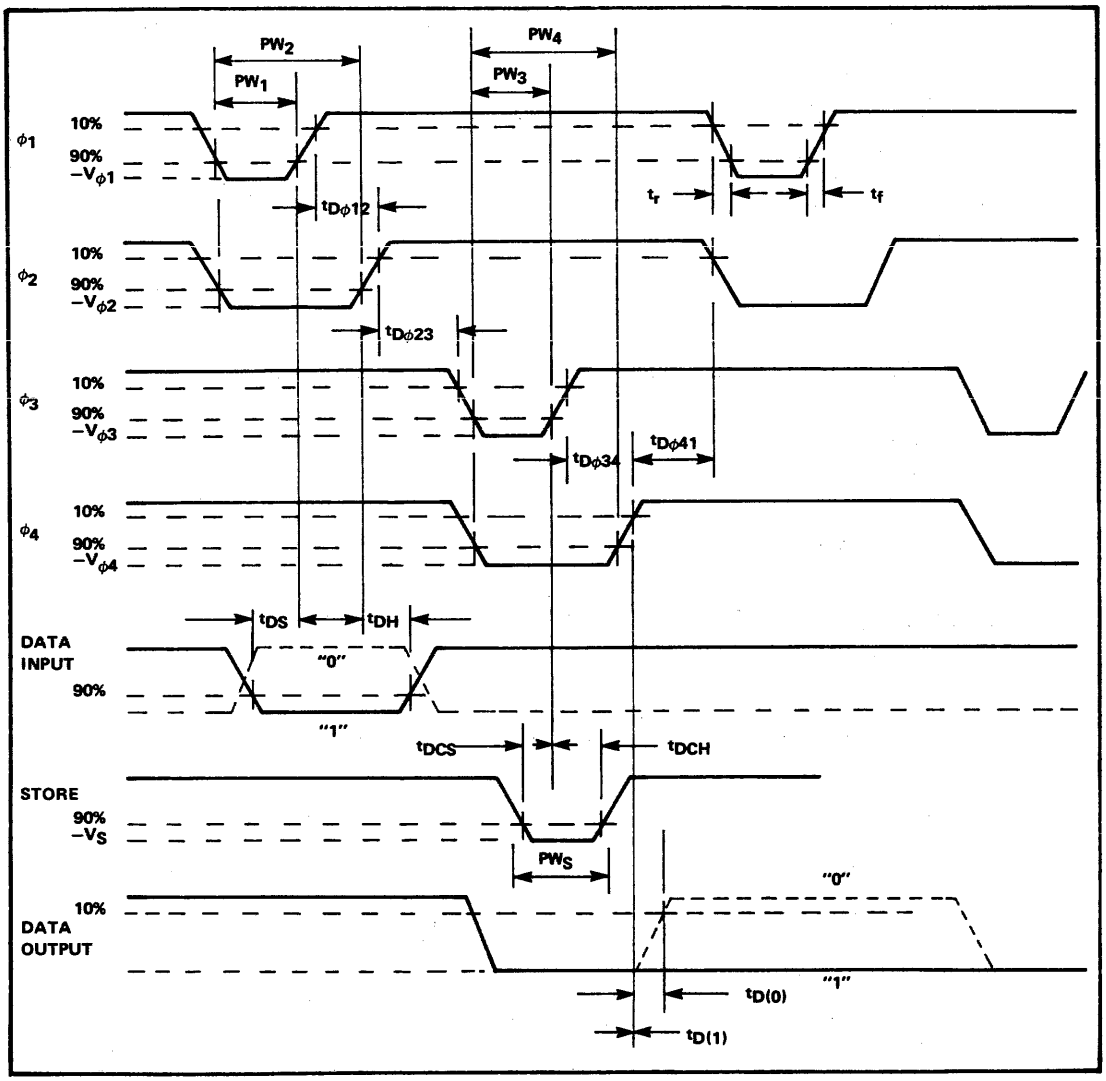
timing diagram and voltage waveforms



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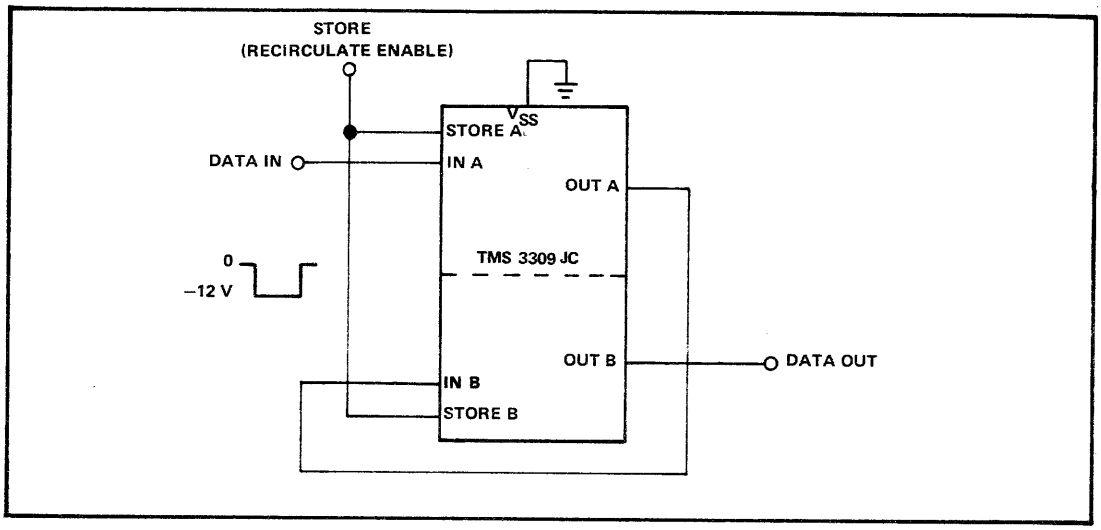
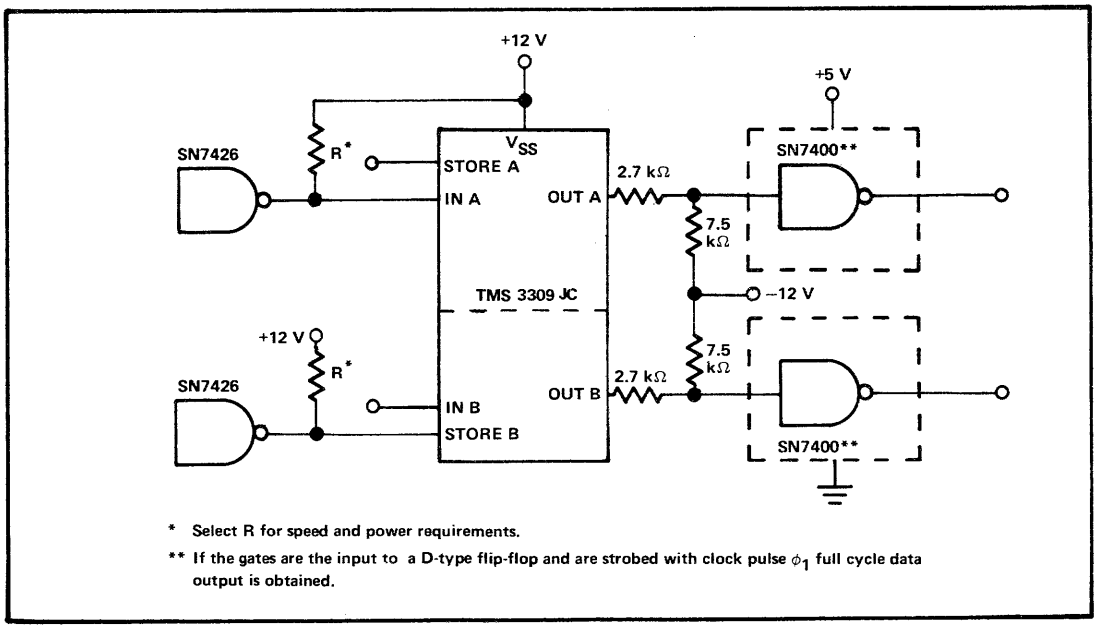
interface circuits

a) MOS interface



NOTE: In this figure the register has been connected as a 1024-bit shift register.

b) TTL interface



* Select R for speed and power requirements.

** If the gates are the input to a D-type flip-flop and are strobed with clock pulse ϕ_1 full cycle data output is obtained.

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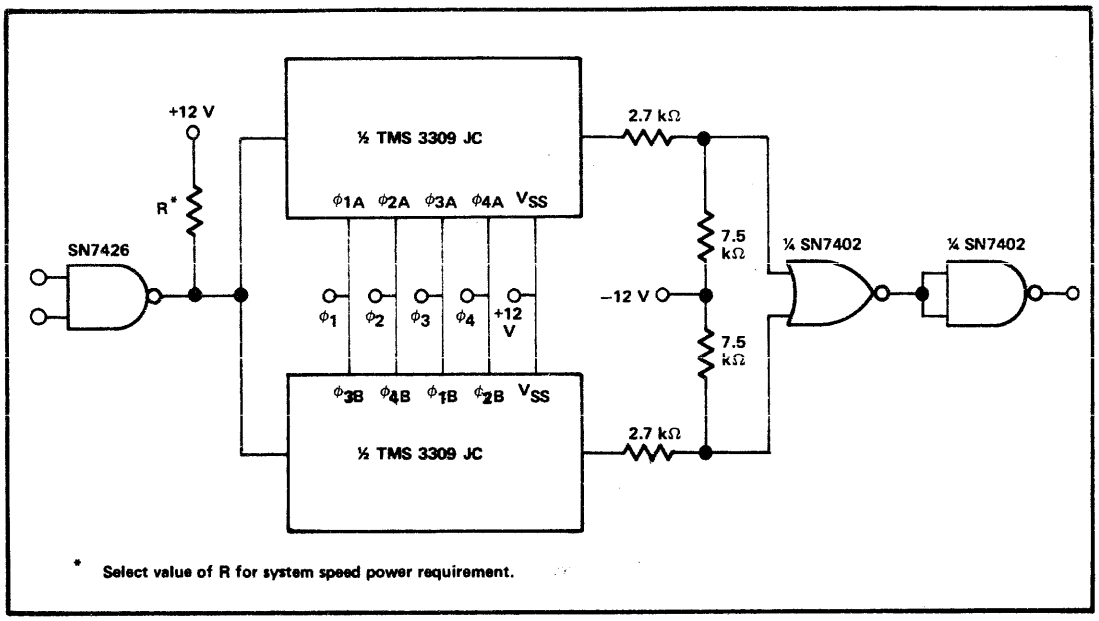
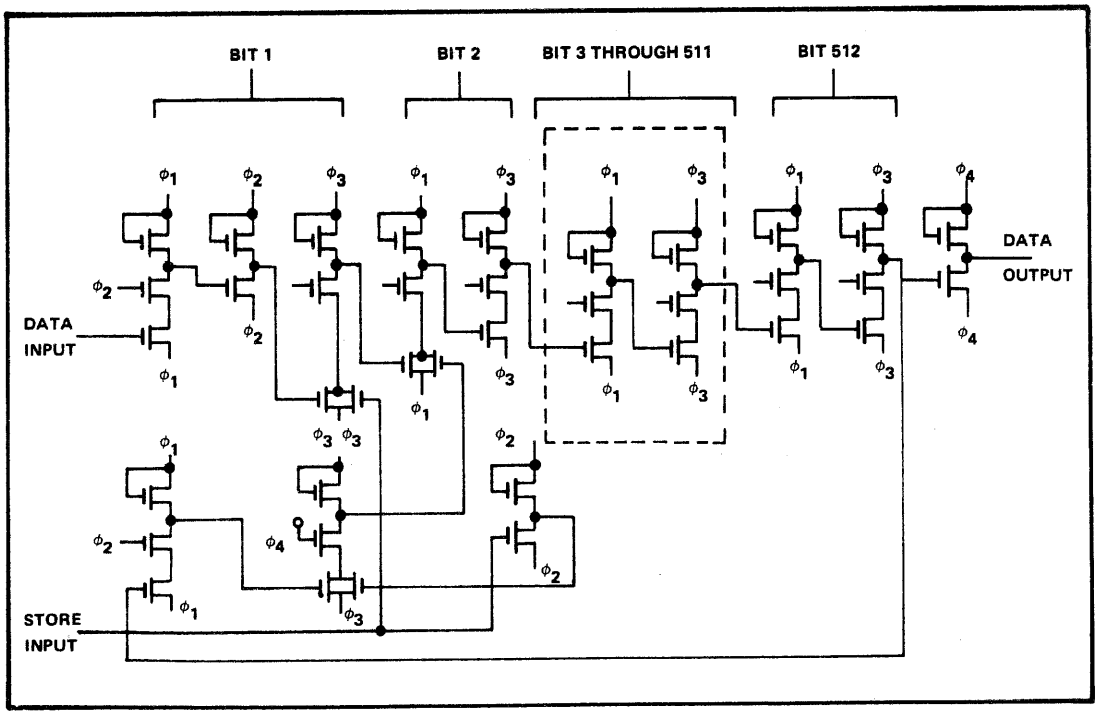
multiplexing of TMS 3309 JC 10-MHz operation



* Select value of R for system speed power requirement.

circuit diagram



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TMS 3314 JC, TMS 3314 NC
TRIPLE (60+4) DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- 2-MHz operation
- TTL compatible
- Open-drain output buffers
- Three 60-bit registers
- Three 4-bit registers
- Dual-in-line package

description

The TMS 3314 JC/NC contains three separate 60-bit, and three separate 4-bit dynamic shift registers constructed on a single monolithic chip, using thick-oxide enhancement-mode P-channel MOS transistors.

Each register has independent input and output terminals and common clock and power lines. Each has an unlocked open-drain output buffer to provide an output inverted from the input. The inputs and outputs terminals of the registers are oriented for optimum printed-circuit-board layout.

The TMS 3314 JC/NC is ideal for data-handling applications in desk calculators, terminals, and peripheral equipment.

"TMS 3314 JC" is the part number for a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic package is designated "TMS 3114 NC."

logic definition

Negative logic is assumed:

a) Logic 1 = most negative (LOW) voltage

b) Logic 0 = most positive (HIGH) voltage

operation

Two clock pulses are required for operation of the registers. The pulses should not simultaneously be at Low levels. Data is transferred into the registers when clock pulse ϕ_1 is pulsed to a Low level. Data shift occurs when clock pulse ϕ_2 is pulsed to a Low level. Output data appears on the High-to-Low transition of clock pulse ϕ_2.

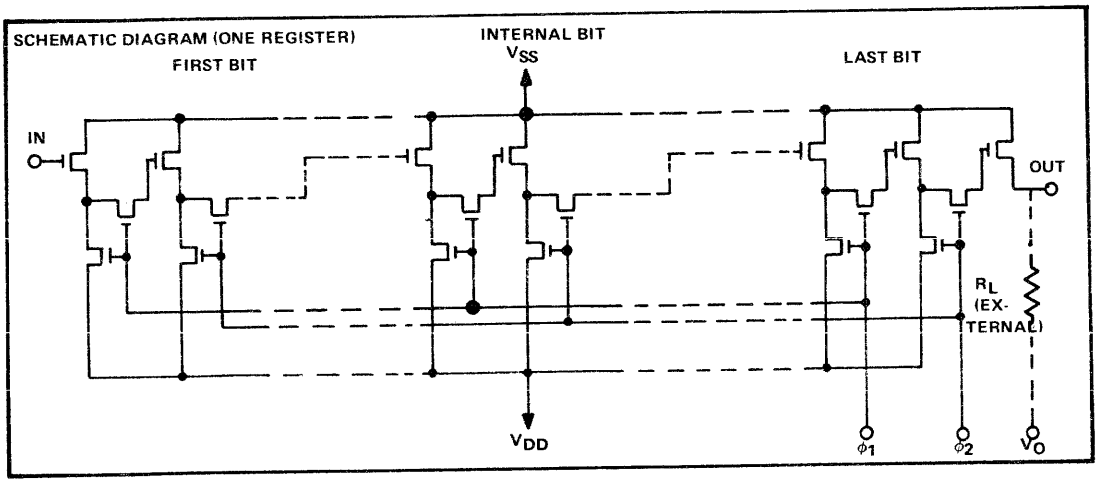
The registers can drive DTL/TTL gate loads by means of a pull-down resistor, connected between the output terminal and the V_{DD} supply.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{DD} range (See Note 1)	−30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−30 V to 0.3 V
Clock input voltage range (See Note 1)	−30 V to 0.3 V
Data input voltage range (See Note 1)	−30 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

circuit diagram



recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Drain supply V_{DD}	−11	−14	−16	V
Output supply V_O	−11	−14	−16	V
Logic Levels				
Input HIGH level (logic 0) V_{IH}	−3	0	+0.3	V
Input LOW level (logic 1) V_{IL}	−8	−14	−29.0	V
Clock Voltage Levels				
HIGH level (logic 0) $V_{\phi H}$	−3	0	+0.3	V
LOW level (logic 1) $V_{\phi L}$	−22	−28	−29.0	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			5	μs
Clock pulse width 1 $PW_{\phi 1}$	0.22		10	μs
Clock pulse width 2 $PW_{\phi 2}$	0.22		10	μs
Pulse Spacing				
Clock delay $t_{D\phi 12}$	0.01		100	μs
Clock delay $t_{D\phi 21}$	0.01		100	μs
Data setup t_{DS}	75			ns
Data hold t_{DH}	75			ns
Clock Pulse Overlap (See Note 2)		(NOTE 2)		ns
Pulse Repetition Rate (Note 3) PRR				
Data	0.01		2	MHz
Clock	0.01		2	MHz

NOTES: 2. The two clock pulses should not be simultaneously more than 3 V below V_{SS}.
3. R_L = 13 kΩ, C_L = 10 pF.

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Maximum speed of operation will be obtained when operating at nominal conditions. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

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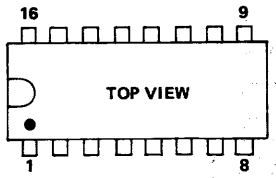
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current (Leakage)	$V_I = -14$ V			500	nA
$I_{\phi L}$	Clock Current (Leakage)	$V_I = -29$ V			100	μA
Output Voltage Levels						
V_{OL}	Output LOW level (logic 1)	R_L = 13 kΩ to V_{DD}, C_L = 10 pF	−9	−10		V
V_{OH}	Output HIGH level (logic 0)	R_L = 13 kΩ to V_{DD} C_L = 10 pF			−2.5	V
Output Current						
I_O	Logic 0	−14 V applied to output			10	μA
I_O	Logic 1	−14 V applied to output	2			mA
Power Supply Current Drain						
I_{DD}	Drain supply	R_L = 13 kΩ to V_{DD}, $PW_{\phi 1} = PW_{\phi 2}$ = 200 ns, PRF = 2 MHz		15	20	mA
P_D	Power dissipation			210	280	mW
Output Logic Delay						
t_{DLH}	Output Low level (logic 1)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −24 V		80	150	ns
t_{DHL}	Output High level (logic 0)	R_L = 13 kΩ, C_L = 10 pF, V_ϕ = −25 V		225	300	ns
Capacitance						
C_{IN}	Input	V_ϕ = 0 V, f = 1 MHz		3	5	pF
C_ϕ	Clock	V_ϕ = 0 V, f = 1 MHz		55	65	pF

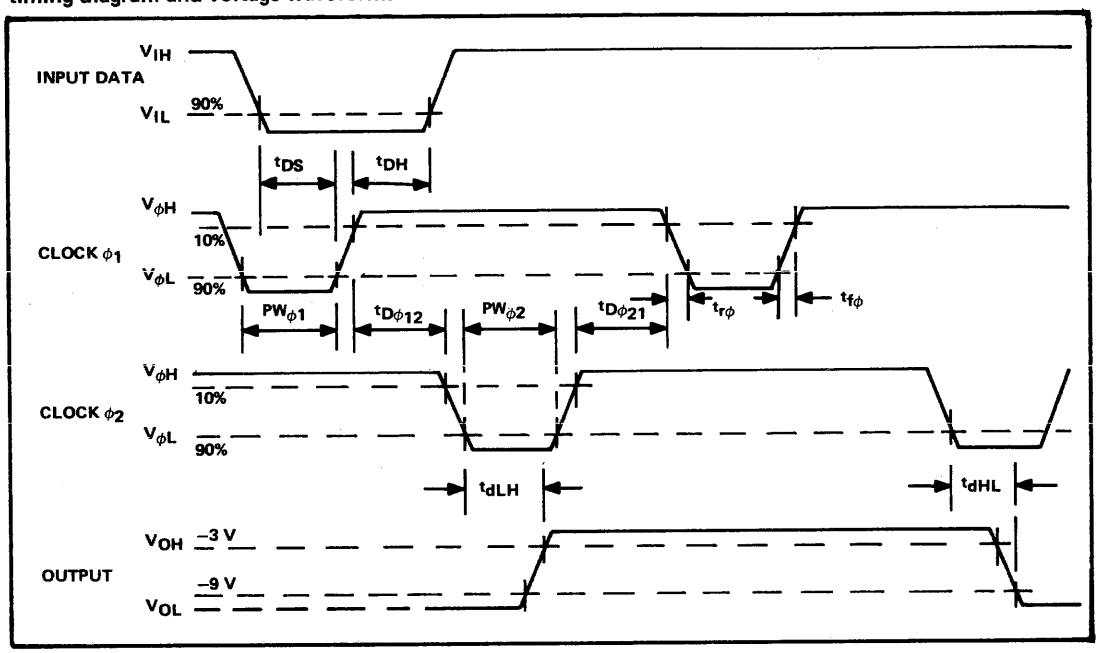
mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 3314 JC) and a 16-pin dual-in-line plastic package (TMS 3314 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



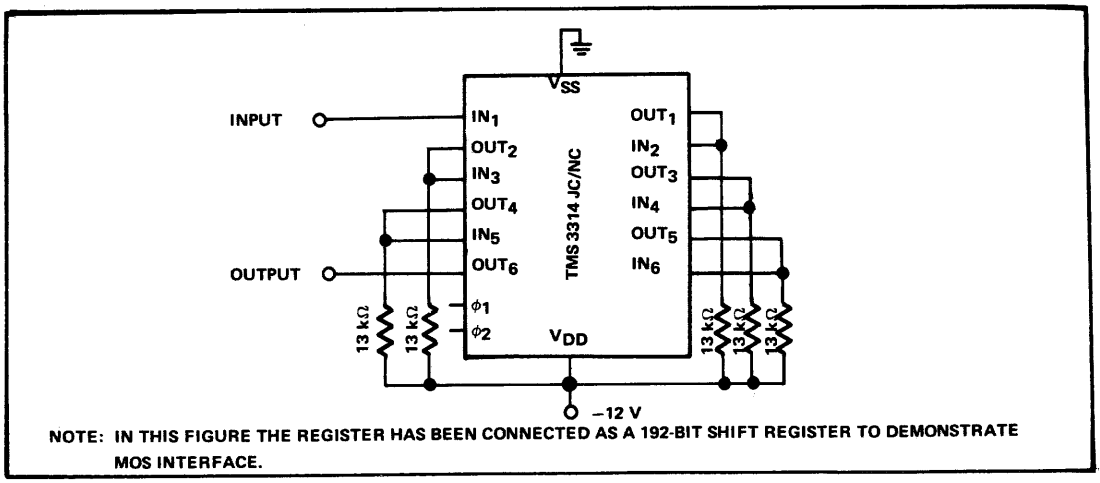
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	IN_1	9	ϕ_2
2	OUT_2	10	IN_6
3	IN_3	11	OUT_5
4	OUT_4	12	IN_4
5	IN_5	13	OUT_3
6	OUT_6	14	IN_2
7	ϕ_1	15	OUT_1
8	V_{SS}	16	V_{DD}

timing diagram and voltage waveforms



interface circuits

a) MOS



NOTE: IN THIS FIGURE THE REGISTER HAS BEEN CONNECTED AS A 192-BIT SHIFT REGISTER TO DEMONSTRATE MOS INTERFACE.

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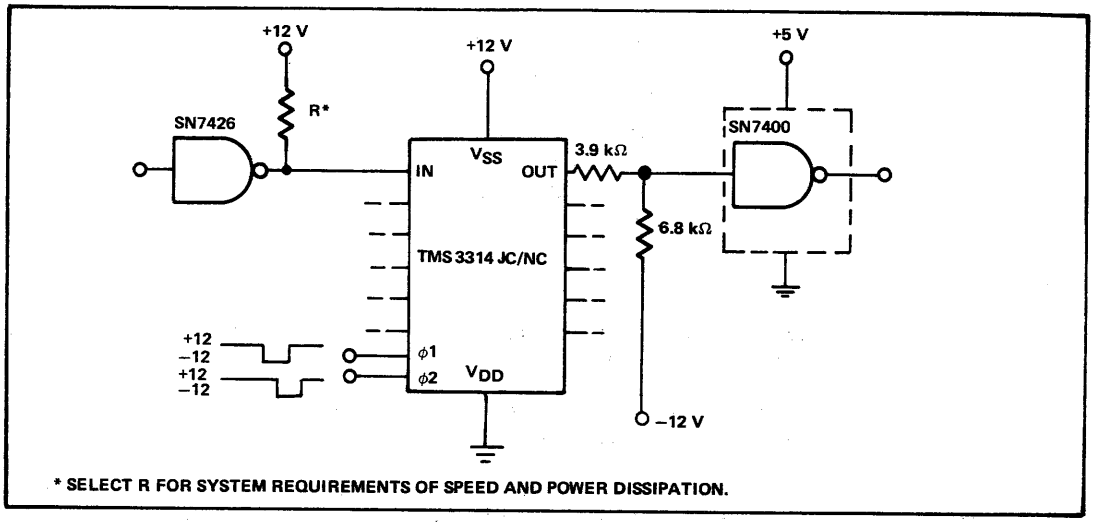
interface circuits (continued)

b) TTL



* SELECT R FOR SYSTEM REQUIREMENTS OF SPEED AND POWER DISSIPATION.

14

MOS
LSI

TMS 3401 LC, NC - 512-BIT DYNAMIC SHIFT REGISTER
TMS 3402 LC, NC - 500-BIT DYNAMIC SHIFT REGISTER

features

- Two-phase dynamic logic
- 5-MHz operation
- Directly TTL compatible at input and output
- No external resistors required
- Low power dissipation — 0.2 mW/bit 1 MHz
- Output delay — 50 ns
- Low-threshold technology
- Power supplies — +5 V, −12 V
- Push-pull output buffer

description

The 512-bit TMS 3401 LC/NC and the 500-bit TMS 3402 LC/NC are high-speed dynamic shift registers. A ratioless two-phase design has been employed to minimize power consumption.

Because both input and output are TTL compatible without the use of external resistors, these registers can be strung together directly and can interface directly with bipolar systems.

The circuits are constructed using MOS P-channel thick-oxide and low-threshold technologies to implement low-threshold MOS devices. The design uses programmable techniques, and the number of bits may be altered through single-level programming for a nominal charge.

logic definition

Positive logic is assumed.

a) Logic 1 = most positive (HIGH) voltage

b) Logic 0 = most negative (LOW) voltage

operation

Data is transferred into the register when the ϕ_1 clock is Low (−12 V). The data must be held steady for at least 30 nanoseconds before the clock goes to the High state (+5 V). One of two internal resistors (1.5 kΩ or 6 kΩ) can be connected to assist in pulling up the logic 1 level provided by DTL or TTL.

Output delay time is defined as the period required for the output to reach the DTL or TTL changeover threshold after the ϕ_2 clock reaches 90% of its Low voltage. This time is faster than 50 nanoseconds.

programming

The device has been so designed that by changing only one level of artwork the designer can obtain any bit length between 233 and 512 bits. The 512-bit length (TMS 3401 LC/NC) and the 500-bit length (TMS 3402 LC/NC) are available off the shelf. Other bit lengths are obtained through use of computer-aided design methods, providing fast, accurate and economical turnaround. The electrical characteristics and pin configuration are the same for the whole family of devices.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −20 V to 0.3 V
Clock input voltage range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage range (See Note 1) . . . . . −20 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C
Input pull-up resistor voltage range . . . . . −6 V to 0.3 V

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

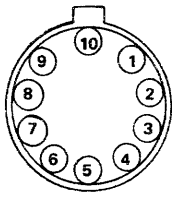
recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.5	+5	+5.5	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input HIGH level V_{IH}	V_{SS} −1.5		V_{SS}	V
Input LOW level V_{IL}	−13		+0.8	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$ (See Note 2)	V_{SS} −1		V_{SS}	V
Clock LOW level $V_{\phi L}$	−14	−12	−11	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			1	μs
Clock pulse width 1 (5 MHz) $PW_{\phi 1}$	0.075		10	μs
Clock pulse width 2 (5 MHz) $PW_{\phi 2}$	0.075		10	μs
Pulse Spacing				
Clock delay $t_{d\phi 12}$			50	μs
Clock delay $t_{d\phi 21}$			50	μs
Data setup t_{DS}	50			ns
Data hold t_{DH}	10			ns
Pulse Repetition Rate PRR				
Data	0.02		5	MHz
Clock	0.02		5	MHz

NOTE 2: Both clock pulses should not be simultaneously more than 2 V below V_{SS}.

mechanical data and pin configuration

The TMS 3401 LC and the 3402 LC are mounted in TO-100 packages. (See MOS/LSI packaging section.)



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	V_{DD}	6	Input pull-up resistor (1.5 kΩ)
2	Output	7	Input
3	V_{GG}	8	Input pull-up resistor (6 kΩ)
4	V_{SS}	9	Clock ϕ_2
5	No connection	10	Clock ϕ_1

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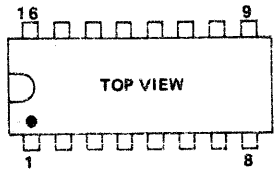
— continued

mechanical data and pin configuration (continued)

The TMS 3401 NC and the TMS 3402 NC are mounted in 16-pin dual-in-line plastic packages designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Input	9	V_{GG}
2	R_2 (6 kΩ)	10	No connection
3	$\phi 2$	11	No connection
4	No connection	12	No connection
5	$\phi 1$	13	No connection
6	V_{DD}	14	No connection
7	No connection	15	R_1 (1.5 kΩ)
8	Output	16	V_{SS}

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input current (leakage)	V_I = 0 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock current (leakage)	V_ϕ = 0 V,	V_{SS} = +5 V			50	μA
Output Voltage Levels							
V_{OL}	Output LOW level (Note 3)	TTL load, f = 5 MHz	C_L = 10 pF,		+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	TTL load, f = 5 MHz	C_L = 10 pF,	+3.6	+4.5		V
V_{OL}	Output LOW level (Note 3)	I_O = +1.6 mA			+0.15	+0.4	V
V_{OH}	Output HIGH level (Note 3)	I_O = −1 mA		+4.5	+4.7		V
Power Supply Current Drain							
I_{DD}	Drain supply (Note 4)	V_{SS} = 0,	V_{GG} = 17 V			0.1	mA
I_{GG}	Gate supply (Note 4)	V_{DD} = 5 V			3.5	7	mA
P_D	Power dissipation				350		mW

NOTES: 3. For final test purposes, a worst-case TTL load is simulated by a load of 2.7 kΩ and a capacitance of 10 pF. A worst-case MOS load is simulated by a load of 20 kΩ and 20 pF. All loads are connected between output and V_{SS}.

4. Does not include output stage load or transient current. In the MOS load mode, the current will consist of transients due to capacitor discharge and/or leakage current.

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Delay							
t_{DLH}	Output LOW level	TTL load, f = 5 MHz	C_L = 10 pF,		10	50	ns
		R_L = 10 MΩ, f = 5 MHz	C_L = 10 pF,		15	50	ns
t_{DHL}	Output HIGH level	TTL load, f = 5 MHz	C_L = 10 pF,		11	50	ns
		R_L = 10 MΩ, f = 5 MHz	C_L = 10 pF,		4	30	ns
Capacitance							
C_{IN}	Input	$V_I = V_{SS}$,	f = 1 MHz		5	7	pF
C_ϕ	Clock	$V_\phi = V_{SS}$,	f = 1 MHz		220	280	pF

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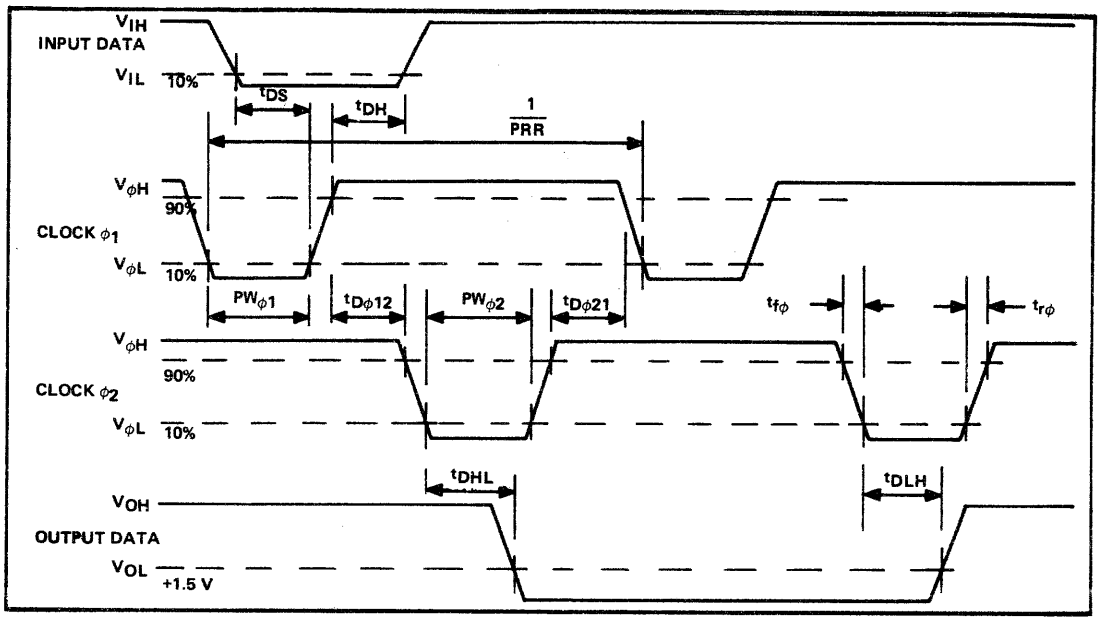
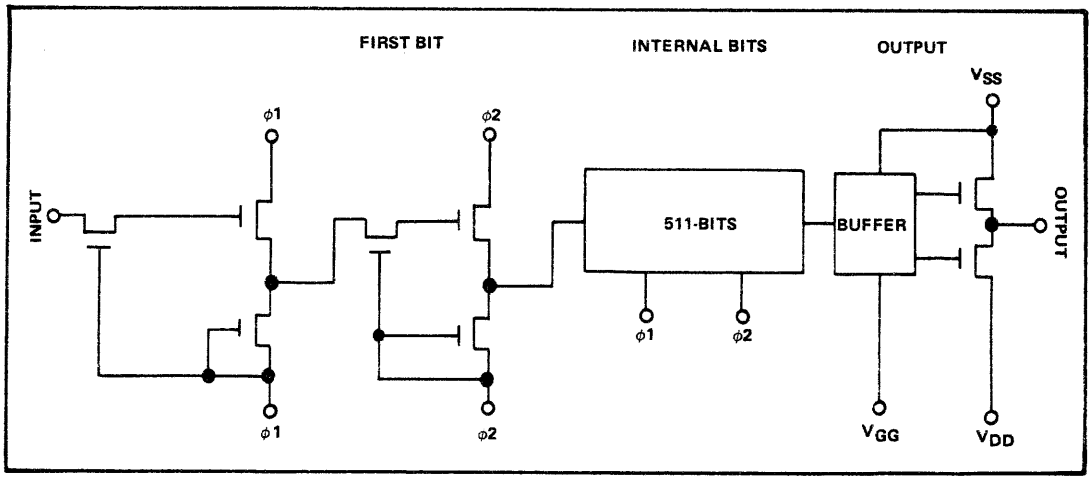
timing diagram and voltage waveforms



internal diagram



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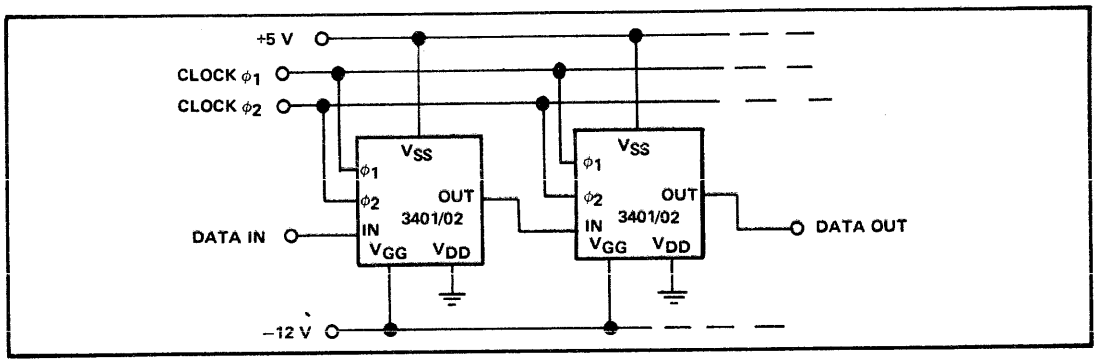
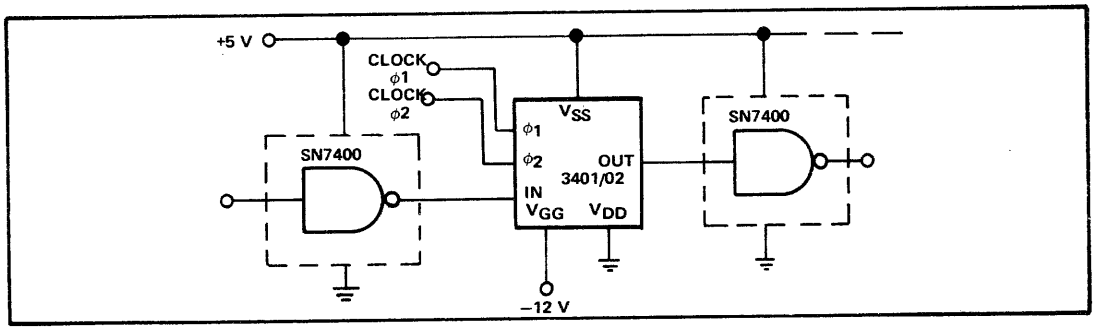
interface circuits

a) MOS



b) TTL



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TMS 3404 JC, TMS 3404 NC
DUAL 512-BIT DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- Two-phase dynamic logic
- 5-MHz shift rate
- Low power – 0.1 mW/bit at 1 MHz
- Power supplies – +5 V, –12 V
- Single-ended output
- TTL compatible – without external components
- Low-threshold technology

description

The TMS 3404 JC/NC consists of two high-speed 512-bit dynamic shift registers. The bits are implemented by a ratioless two-phase design to minimize power consumption. Inputs and outputs are TTL compatible—without use of external components.

The entire device is constructed on a single monolithic chip using thick-oxide techniques and low-threshold MOS P-channel enhancement-mode transistors.

TMS 3404 JC is the part number for this device mounted in a 16-pin ceramic dual-in-line package. Mounted in a 16-pin plastic package the device is designated TMS 3404 NC.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Data is transferred into the register when the ϕ_1 clock is Low (–12 V). The data must be set up at least 100 nanoseconds before the clock ϕ_1 goes to the high state (+5 V) and held steady at least 20 nanoseconds after ϕ_1 reaches this state.

Output delay time is defined as the time required for the output to reach the DTL or TTL changeover threshold after the ϕ_2 clock reaches 90% of its Low voltage. This time is faster than 100 nanoseconds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	–20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	–20 V to 0.3 V
Clock input voltage range (See Note 1)	–20 V to 0.3 V
Data input voltage range (See Note 1)	–20 V to 0.3 V
Operating free-air temperature range	–25°C to 85°C
Storage temperature range	–55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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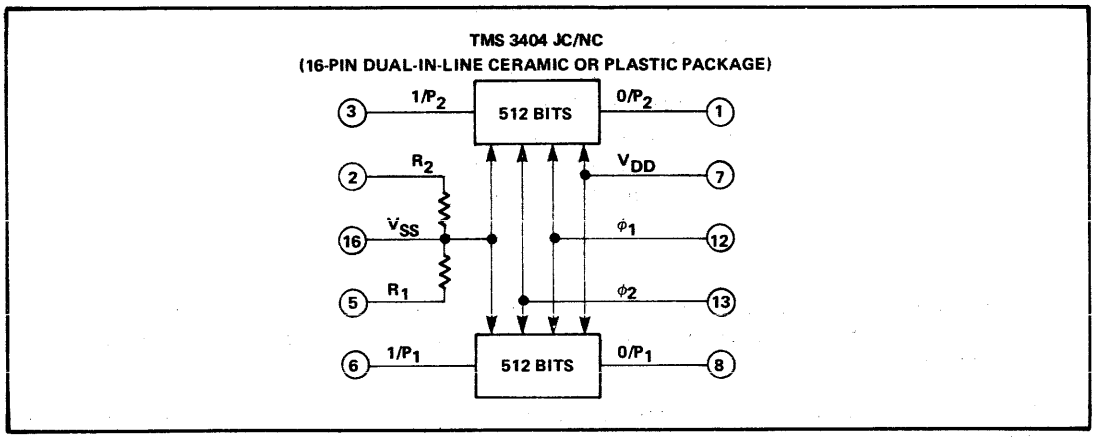
TMS 3404 JC, TMS 3404 NC
DUAL 512-BIT DYNAMIC SHIFT REGISTER

functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5	+5.25	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input High level V_{IH}	V_{SS} −1.6		V_{SS}	V
Input Low level V_{IL}	V_{SS} −18		V_{SS} −4.2	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	V_{SS} − 1.0		V_{SS}	V
Clock LOW level $V_{\phi L}$	V_{SS} −19		V_{SS} −16	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			1	μs
Clock pulse width $PW_{\phi 1}$	0.080		10	μs
Clock pulse width $PW_{\phi 2}$	0.080		10	μs
Pulse spacing				
Clock delay $t_{d\phi 12}$	0.010		50	μs
Clock delay $t_{d\phi 21}$	0.010		50	μs
Data setup t_{DS}	0.100			μs
Data hold t_{DH}	0.020			μs
Pulse Repetition Rate PRR				
Data	0		5.0	MHz
Clock	.01		5.0	MHz

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static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

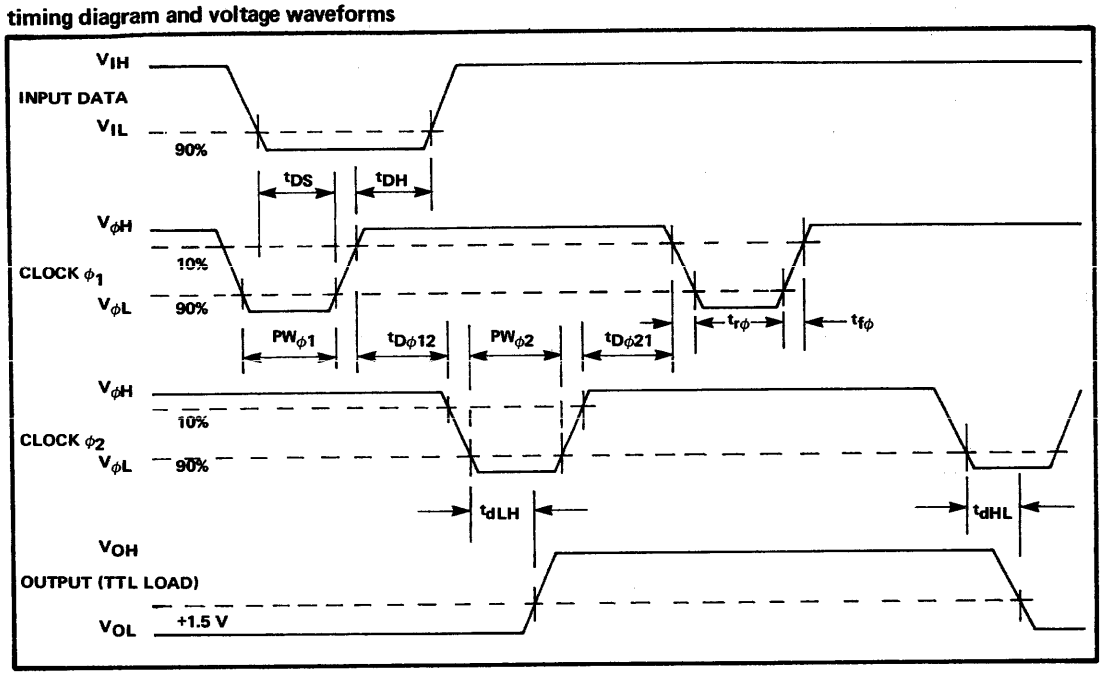
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = −12 V, V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = −12 V, V_{SS} = +5 V			10	μA
Output Voltage Levels						
V_{OL}	Output LOW level	TTL load	V_{SS} −4.6			V
V_{OH}	Output HIGH level		V_{SS} −1.8		V_{SS}	V
Supply Current Drain						
I_{GG}	Gate supply	V_{SS} = 0 V, V_{GG} = −17 V			3	mA

NOTE 1: Power dissipation (mW) = 80 + 90 x F_{ϕ} (MHz) + 0.5 x [$PW_{\phi 1}$(ns) + $PW_{\phi 2}$(ns)] x F_{ϕ} (MHz).

dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Transition Time						
t_r	Rise			50		ns
t_f	Fall			50		ns
Output Logic Delay						
t_{DL}	Output Low level	TTL load		100		ns
t_{DH}	Output High level	TTL load		100		ns
Capacitance						
C_{IN}	Input			8		pF
C_{ϕ}	Clock			350		pF

timing diagram and voltage waveforms



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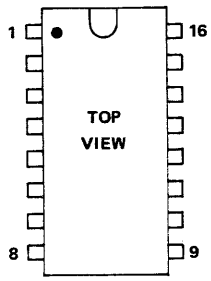
mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 3404 JC) and a 16-pin plastic package (TMS 3404 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

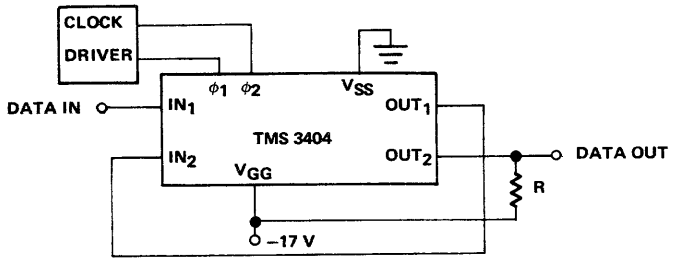


PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Output 2	9	Clock 1
2	NC	10	NC
3	NC	11	NC
4	Input 2	12	NC
5	Input 1	13	NC
6	V_{GG}	14	Clock 2
7	NC	15	NC
8	Output	16	V_{SS}

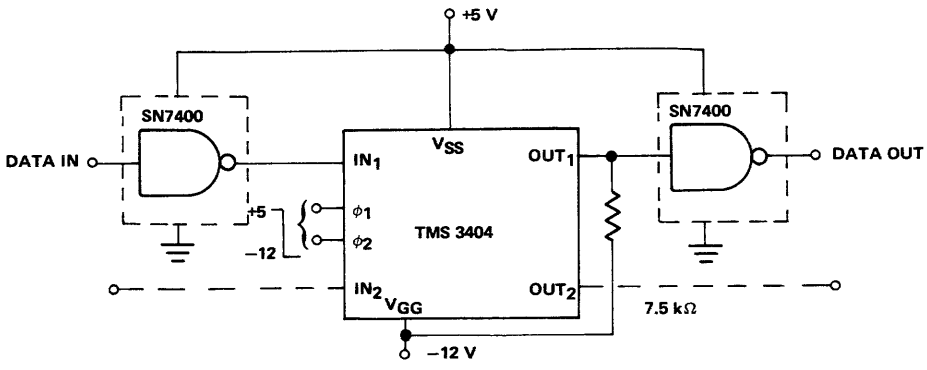
interface circuits

a) MOS

Note: In this figure the TMS 3404 has been connected as a single 1024-bit register to demonstrate MOS interface



b) TTL



TEXAS INSTRUMENTS
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TMS 3406 LR
DUAL 100-BIT DYNAMIC SHIFT REGISTER

JANUARY, 1971

features

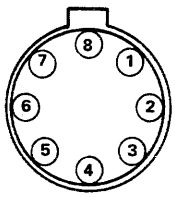
- Low power dissipation – 0.4 mW/bit typical at 1 MHz
  – 1 mW/bit typical at 2 MHz
- High-frequency operation – 2.5 MHz guaranteed
- TTL/DTL compatible
- Single-ended output buffer
- Low-threshold technology

description

The Texas Instruments TMS 3406 LR consists of two separate 100-bit dynamic shift registers with independent input and output terminals. Only one power supply and two clock phases are required for operation. Low-threshold, thick-oxide, MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMS 3406 LR and Bipolar integrated circuits.

mechanical data and pin configuration

The TMS 3406 LR is mounted in a TO-99 package (see MOS/LSI packaging section).



BOTTOM VIEW

LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Input 1	5	Input clock (ϕ_1)
2	Output 1	6	Output 2
3	Input clock (ϕ_2)	7	Input 2
4	V_{SS}	8	V_{DD}

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . –20 V to 0.3 V
Clock voltage V_ϕ (See Note 1) . . . . . –20 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . –20 V to 0.3 V
Power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . –55°C to 85°C
Storage temperature range . . . . . –55°C to 150°C

recommended operating conditions (–55°C to 85°C)

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD} (See Note 1)	–9	–10	–12	V
Clock voltage $V_{\phi L}$ (See Note 1) logic 0	–15	–16	–18	V
Clock voltage $V_{\phi H}$ (See Note 1) logic 1	+0.3	–0.5	–1.5	V
Width of clock pulse t_{p1} (See voltage waveforms)	150			ns
Width of clock pulse t_{p2} (See voltage waveforms)	150			ns
Transient time of clock pulse, t_r, t_f (See voltage waveforms)			5	μs
Clock delay time, t_d (See voltage waveforms)	20			ns
Width of data pulse, t_p (See voltage waveforms)	170			ns
Data pulse before clock change t_{p0} (See voltage waveforms)	150			ns
Clock repetition rate	0.01		2.5	MHz

NOTE 1: These are voltage values with respect to most positive supply voltage, V_{SS}.

TEXAS INSTRUMENTS
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logic definition

Positive logic is assumed

a) Logic 1 = most positive (high) voltage

b) Logic 0 = most negative (low) voltage

electrical characteristics (at nominal operating conditions and 25°C)

V_{DD} = −5 V, V_{SS} = +5 V, $V_{\phi H}$ = −11 V, $V_{\phi L}$ = +5 V, and C_L = 10 pF, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{in(1)}$	Logic 1 data input voltage		+3.0	+5	+5.3	V
$V_{in(0)}$	Logic 0 data input voltage		−10	+0.2	+0.8	V
$V_{out(1)}$	Logic 1 output voltage	Load = 3.3 kΩ, t_{p1} = 150 ns	+3.5			V
$V_{out(0)}$	Logic 0 output voltage	Load = 3.3 kΩ, Load = 3.3 kΩ, I_L = 1.6 mA			−3.0 +0.4	V V
R_{out}	Output resistance	Output at logic 0		300	450	Ω
$I_{R(in)}$	Input leakage current	V_{in} = −5 V, T_A = 25°C			0.5	μA
C_{in}	Capacitance of input	V_{in} = +5 V, T_A = 25°C f = 1 MHz		5	7	
$C_{\phi 1,2}$	Capacitance of clock input	V_ϕ = +5 V, T_A = 25°C f = 1 MHz		40	50	
$I_{DD(1)}$	Average supply current (See Note 2)	f = 1 MHz (t_{p1} = 200 ns, t_{p2} = 200 ns) f = 1 MHz (t_{p1} = 150 ns, t_{p2} = 150 ns)		6 4.5	12 10	mA mA
$I_{\phi 1,2}$	Average supply current for clock mode	f = 1 MHz (t_{p1} = t_{p2} = 200 ns) f = 1 MHz (t_{p1} = t_{p2} = 150 ns)		0.5 0.4	1.5 1.2	mA mA

NOTE 2: These values do not include the current flowing through the load resistor.

switching characteristics

V_{DD} = −5 V, V_{SS} = +5 V, $V_{\phi H}$ = −11 V, $V_{\phi L}$ = +5 V, and C_L = 10 pF, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from clock ϕ_1 to data output	See Voltage Waveforms Load = 3.3 kΩ		100	150	ns
t_{pd0}	Propagation delay time to logical 0 level from clock ϕ_1 to data output	See Voltage Waveforms Load = 3.3 kΩ		120	180	ns

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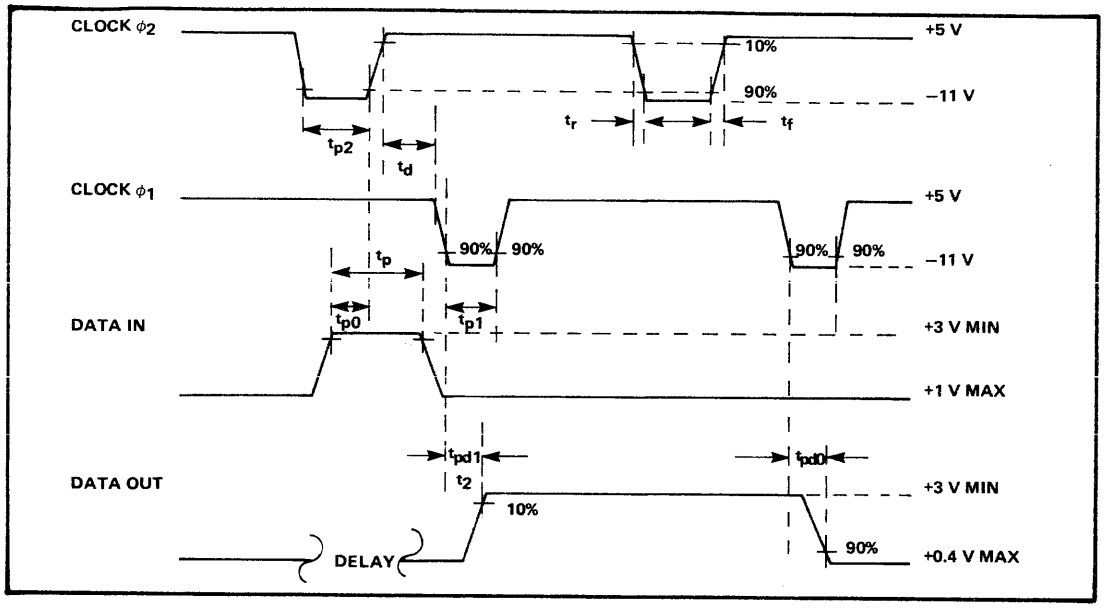
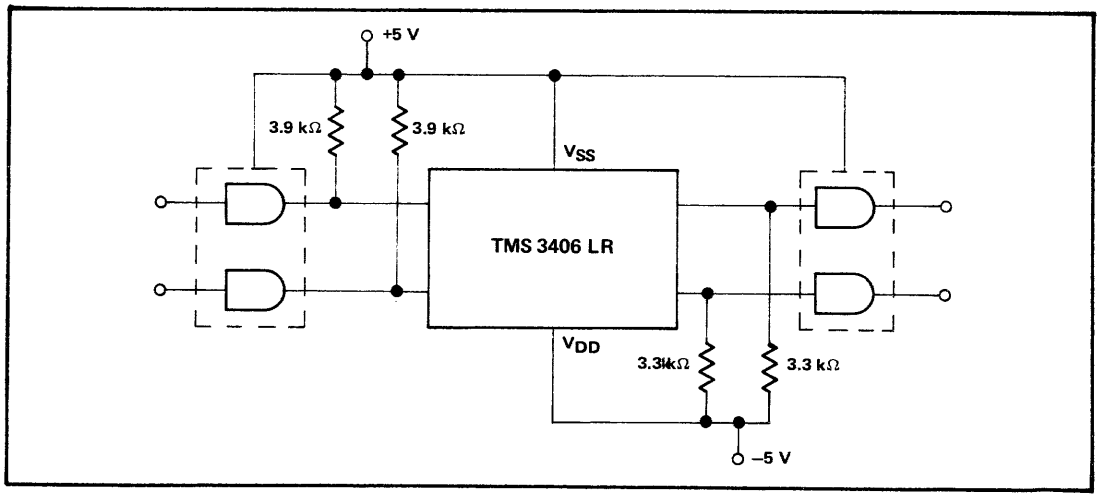
timing diagram



TTL interface



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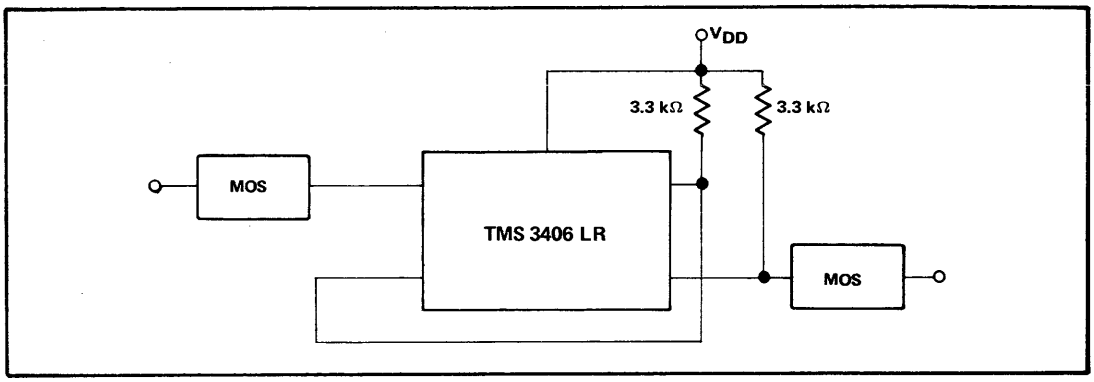
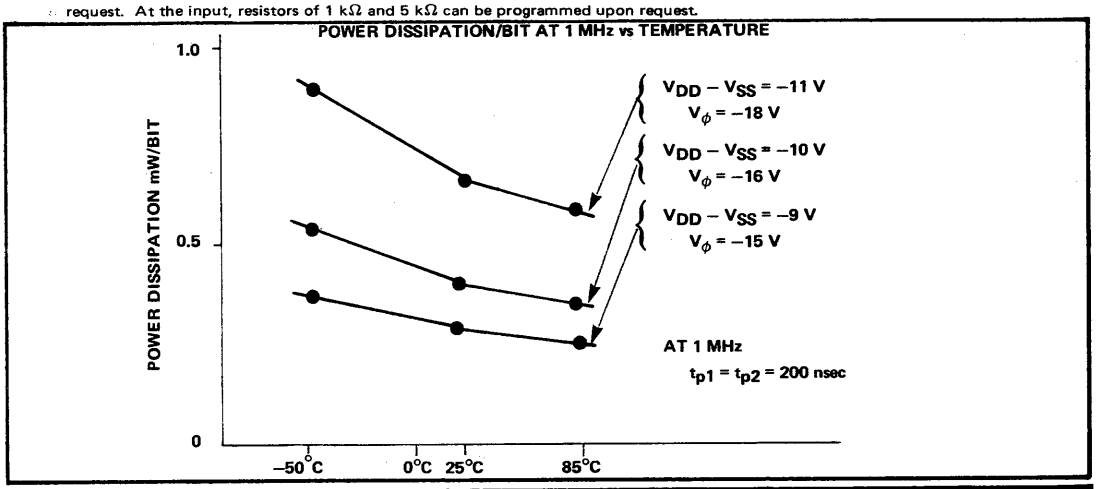
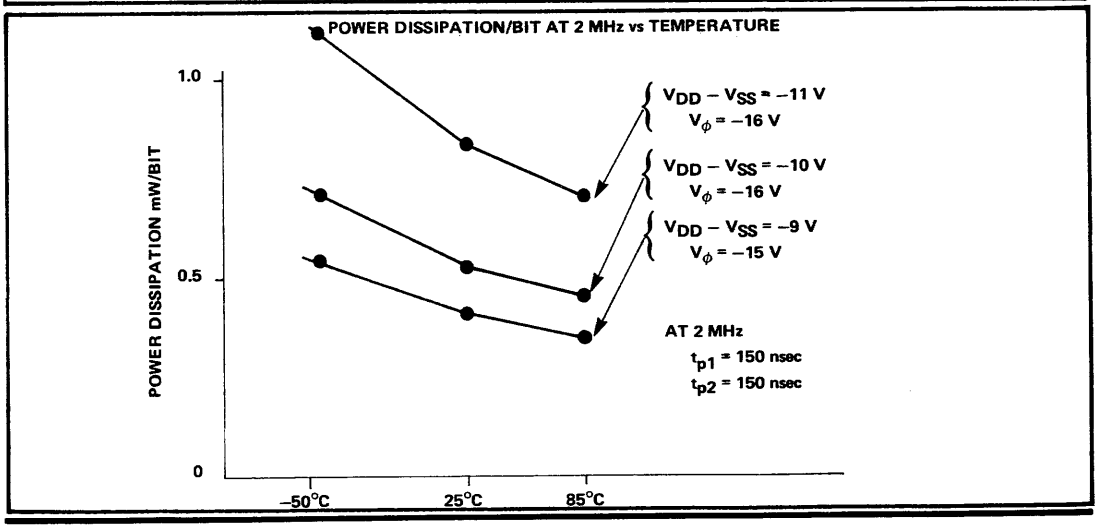
MOS interface



NOTE: The TMS 3406 LR features an open-ended buffer; however, load resistors of 3.3 kΩ and 20 kΩ can be programmed on the chip, upon request. At the input, resistors of 1 kΩ and 5 kΩ can be programmed upon request.





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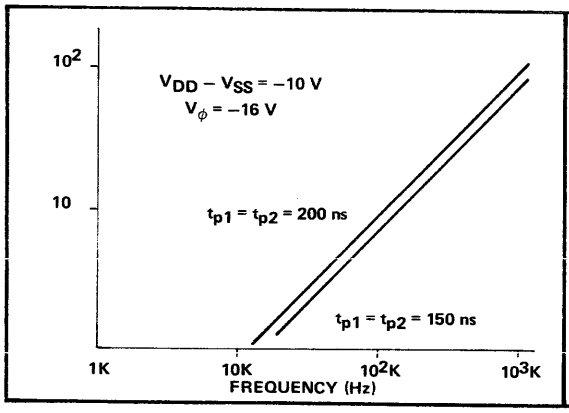
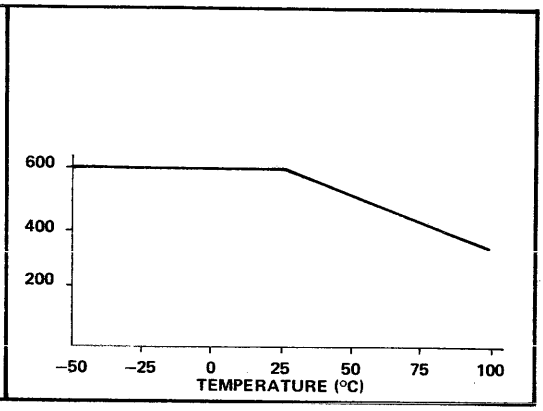
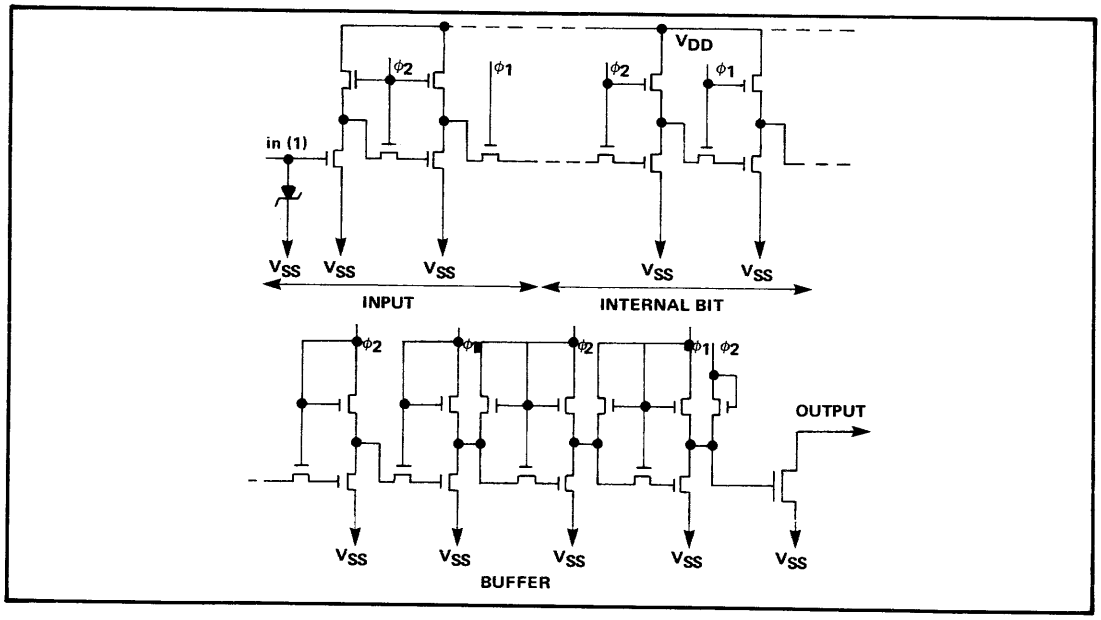
POWER DISSIPATION vs FREQUENCY



PACKAGE POWER DISSIPATION vs TEMPERATURE



SCHEMATIC OF TMS 3406 LR INTERNAL ORGANIZATION



TEXAS INSTRUMENTS
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MOS
LSI

TMC 3409 JC, TMC 3409 NC
QUADRUPLE 80-BIT DYNAMIC SHIFT REGISTER

FEBRUARY, 1971

features

- 2.5-MHz shift rate
- Recirculate logic
- Power supplies – +5 V, 0 V, –12 V
- All inputs TTL compatible
- Single TTL compatible clock
- TTL compatible outputs
- Low power – 300 mW
- Low-threshold technology
- Dual-in-line package

description

The TMC 3409 JC/NC consists of four 80-bit shift registers with separately controlled logic for recirculating data in each register. A single-clock generator provides two clock phases to all four registers. Data, recirculate-control and clock inputs are all TTL compatible. Each output interfaces directly with TTL without the use of external components.

Low-threshold, thick-oxide MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMC 3409 JC/NC and bipolar integrated circuits.

"TMC 3409 JC" is the part number for a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic package is designated "TMC 3409 NC".

logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage (High)

b) Logical 0 = most negative voltage (Low)

operation

Data is transferred into the register when the internal clock $\phi 1$ is on. The internal clock is on when the external clock input is high, but the changes of level occur some 100 nanoseconds behind the external drive. To be entered, data must be held true at least 100 nanoseconds after the external clock drive has changed state.

True output data becomes available about 100 nanoseconds after the TTL clock goes to Low.

Information in the register during the recirculate mode continues to be read out.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	–20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	–20 V to 0.3 V
Clock input voltage range (See Note 1)	–20 V to 0.3 V
Data input voltage range (See Note 1)	–20 V to 0.3 V
Operating free-air temperature range	–25°C to 85°C
Storage temperature range	–55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

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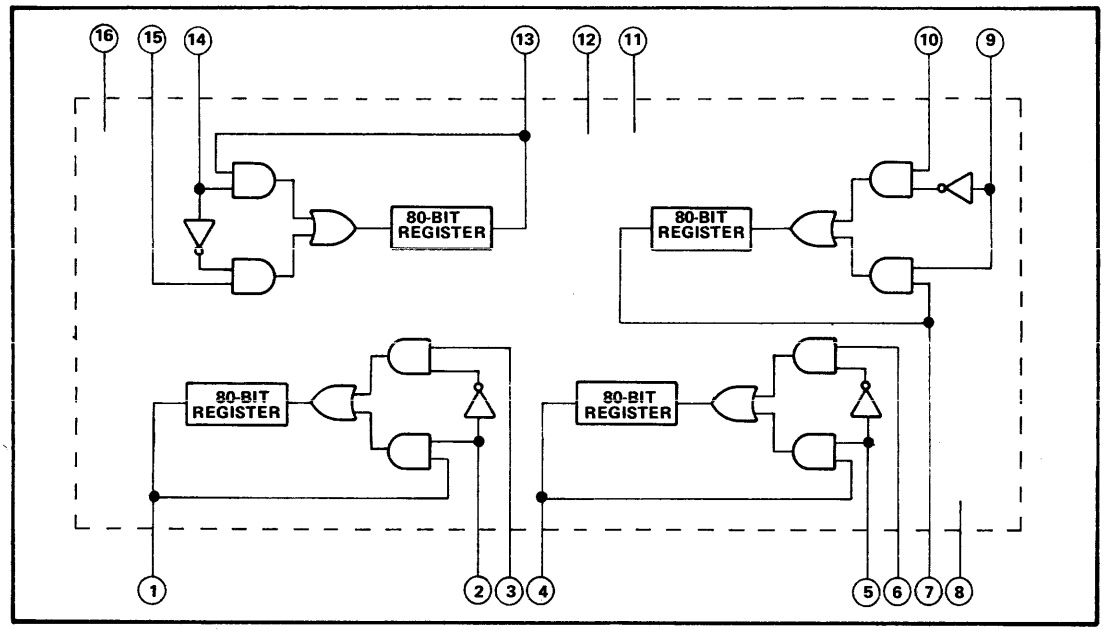
PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TMC 3409 JC, TMC 3409 NC
QUADRUPLE 80-BIT DYNAMIC SHIFT REGISTER

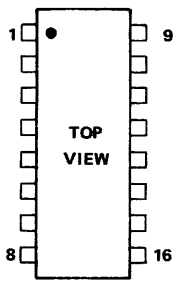
functional block diagram



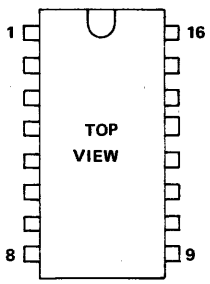
pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMC 3409 JC) and a 16-pin plastic package (TMC 3409 NC).

The package for TMC 3409 JC is designed for insertion in mounting-hole rows on 0.300-inch centers. For the TMC 3409 NC the package is designed for mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



TMS 3409 JC



TMS 3409 NC

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Data Out A	9	Recirc Enable C
2	Recirc Enable A	10	Input C
3	Input A	11	Clock
4	Data Out A	12	V_{GG}
5	Recirc Enable B	13	Data Out D
6	Input B	14	Recirc Enable D
7	Data Out C	15	Input D
8	V_{CC}	16	V_{SS}

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Supply V_{SS}	+4.75	+5.0	+5.25	V
Drain supply V_{DD}	0	0	0	V
Gate supply V_{GG}	−13	−12	−11	V
Logic Levels				
Input High level V_{IH}	V_{SS} −2.0		V_{SS}	V
Input Low level V_{IL}	−13		+0.8	V
Clock Voltage Levels				
Clock High level $V_{\phi H}$	V_{SS} −2.0		V_{SS}	V
Clock Low level $V_{\phi L}$	−13		+0.8	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$		10	100	ns
Clock pulse width High $PW_{\phi H}$	150		50000	ns
Clock pulse width Low $PW_{\phi L}$	150		50000	ns
$PW_{\phi H} \div PW_{\phi L}$	.02		50	
Pulse Spacing				
Data setup t_{DS}	100			ns
Data hold t_{DH}	100			ns
Recirculate Enable setup t_{RS}	200			ns
Recirculate Enable hold t_{RH}	100			ns
Pulse Repetition Rate PRR				
Data f_D	0		2.5	MHz
Clock f_ϕ	.01		2.5	MHz

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = 0			100	nA
$I_{\phi L}$	Clock Current	V_ϕ = 0			100	nA
Output Voltage Levels						
V_{OL}	Output Low level	I_{SINK} = 1.6 mA		0.3	0.4	V
V_{OH}	Output High level	I_{LOAD} = 0.5 mA	V_{SS} −1.0	V_{SS} −0.5	V_{SS}	V
Power Supply Current Drain						
I_{SS}	Substrate supply	25°C		25	30	mA
I_{DD}	Drain supply	25°C		15		mA
I_{GG}	Gate supply	25°C		10	12	mA
P_D	Power Dissipation	25°C		250	300	mW

dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Transition Time						
t_r	Rise			30	50	ns
t_f	Fall			30	50	ns
Output Logic Delay						
t_{OL}	Output Low level			100	150	ns
t_{OH}	Output High level			100	150	ns
Capacitance						
C_{IN}	Input (Data and Recirc Enable)	V_{IN} = V_{SS}			10	pF
C_ϕ	Clock	V_ϕ = V_{SS}			25	pF

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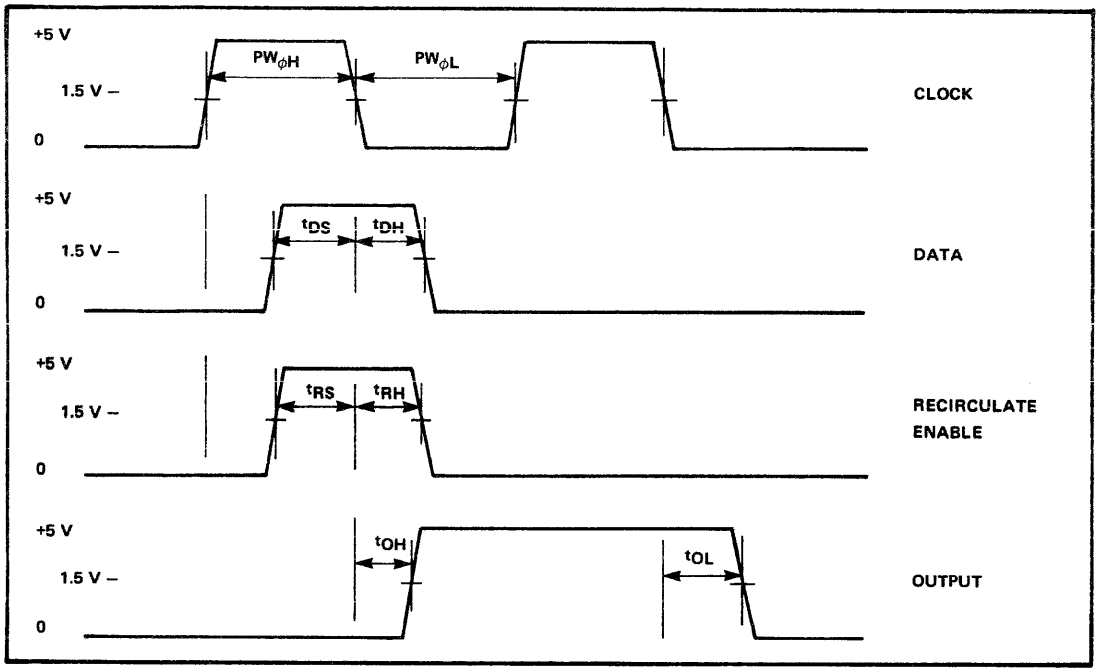
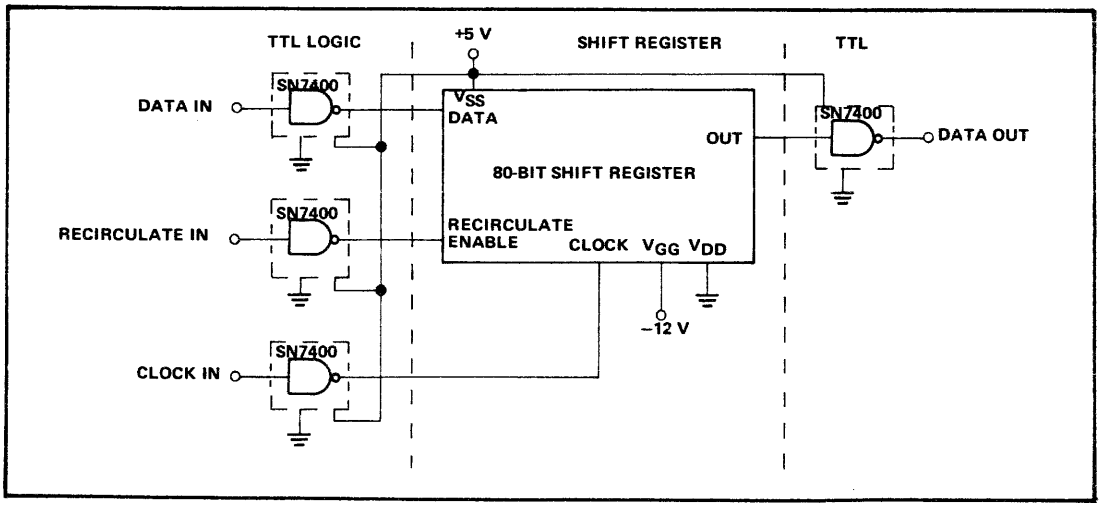
timing diagram and voltage waveforms



TTL interface



TEXAS INSTRUMENTS
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MOS
LSI

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

FEBRUARY 1971

features

- 0.01-MHz to 6-MHz operation
- Low power dissipation
- Open-drain output buffer
- DTL, TTL compatible
- Low clock capacitance (70 pF typ)
- Low-threshold silicon-gate multilevel technology
- 4 x 256 bits TMS 3412
- 2 x 512 bits TMS 3413
- 1 x 1024 bits TMS 3414
- Dual-in-line or plug-in package

description

The circuits TMS 3412 JC/NC, TMS 3413 LC/NC and TMS 3414 LC/NC are a family of two-phase dynamic shift registers. Each device is constructed on a single monolithic chip by use of silicon-gate technology and P-channel enhancement-mode transistors. Input and output terminals in the multiple register circuits are independent; clocks and power are common. Internal multiplexing results in a data shift rate twice the clock rate. Each clock pulse on the phase-1 or phase-2 line shifts the data one bit.

A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "JC". "LC" is the designation for a device mounted in an 8-lead TO-99 package. A unit mounted in a 16-pin dual-in-line plastic package is designated "NC".

logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

operation

Two clock pulses are required for operation of the registers. The pulses should not be at low level simultaneously or data errors will occur.

Data is transferred into the register when the clock pulse, phase 1 or phase 2, is at the low level. Output data appears after the high-to-low transition of the clock pulse, phase 1 or phase 2.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

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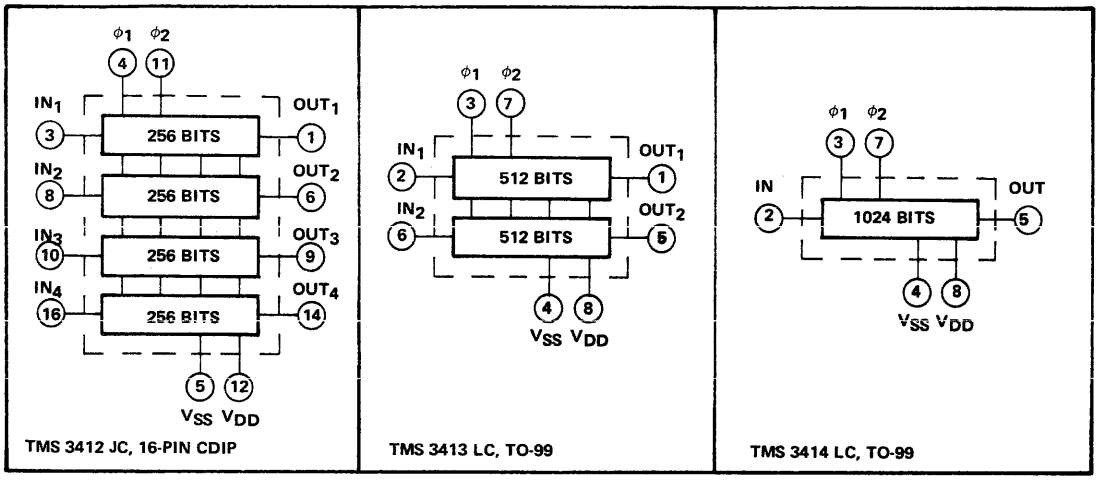
PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

TMS 3412 JC, NC; TMS 3413 LC, NC; TMS 3414 LC, NC
1024-BIT DYNAMIC SHIFT REGISTER

functional block diagram



recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Operating Voltage					
Substrate supply V_{SS}	V_{DD} = −5 V ± 5%	+4.75	5	5.25	V
Drain supply V_{DD}	V_{SS} = +5 V ± 5%	−4.75	−5	−5.25	V
Logic Levels					
Input High level V_{IH}		V_{SS}−1.7		V_{SS}+0.3	V
Input Low level V_{IL}		V_{SS}−4.2		V_{SS}−10	V
Clock Voltage Levels					
Clock High level $V_{\phi H}$		V_{SS}−1.0		V_{SS}+0.3	V
Clock Low level $V_{\phi L}$		V_{SS}−15.0		V_{SS}−17.0	V
Pulse Timing					
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$				1000	ns
Clock pulse width 1 $PW_{\phi 1}$		100			ns
Clock pulse width 2 $PW_{\phi 2}$		100			ns
Pulse spacing					
Clock delay $t_{D\phi 12}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Clock delay $t_{D\phi 21}$	$PW_{\phi 1}$ = $PW_{\phi 2}$ = 100 ns	40			ns
Data setup t_{DS}		40			ns
Data hold t_{DH}		40			ns
Pulse Repetition Rate PRR					
Data				6	MHz
Clock				3	MHz

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static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Current	V_{IN} = −5 V,	V_{SS} = +5 V			500	nA
$I_{\phi L}$	Clock Current	V_{ϕ} = −10 V,	V_{SS} = +5 V			1000	nA
Output Voltage Levels							
V_{OL}	Output Low level	R_L = 3 kΩ, V_{SS} = +5 V	I_L = 1.6 mA,			0.5	V
V_{OH}	Output High level	Driving TTL, V_{SS} = 4.75 V	R_L = 3 kΩ,	2.5			V
Power Supply Current Drain							
I_{DD}	Drain supply	V_{SS} = +5 V, V_{ϕ} = −12 V	V_{DD} = −5 V,		35	50	mA
P_D	Power Dissipation	5-MHz Data Rate,	35% Duty Cycle			600	mW

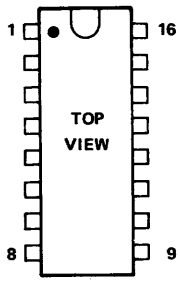
dynamic electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Delay						
t_{DLH1}	Output Low level	1 TTL load (See Note 2)			80	ns
t_{DHL1}	Output High level	1 TTL load (See Note 2)			80	ns
Output Logic Delay						
t_{DLH2}	Output Low level	MOS load (See Note 3)			80	ns
t_{DHL2}	Output High level	MOS load (See Note 3)			80	ns
Capacitance						
C_{IN}	Input	(See Note 4)	2.5		5	pF
C_{ϕ}	Clock		60	70	80	pF

NOTES: 2. V_{SS} = +5 V ± 5%, V_{DD} = −5 V ± 5%, $V_{\phi L}$ = −10 V
3. V_{SS} = 0 V, V_{DD} = −10 V ± 10%, $V_{\phi L}$ = −15 V
4. 16-pin CDIP – C_{IN} min, 7 pF; C_{IN} max, 8 pF

mechanical data and pin configuration

The TMS 3412 is available in both a 16-pin hermetically sealed ceramic dual-in-line package (JC) and a 16-pin plastic package (NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	OUT_1	9	OUT_3
2	NC	10	IN_3
3	IN_1	11	ϕ_2
4	ϕ_1	12	V_{DD}
5	V_{CC} (V_{SS})	13	NC
6	OUT_2	14	OUT_4
7	NC	15	NC
8	IN_2	16	IN_4

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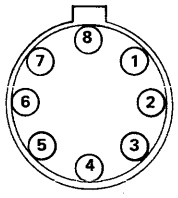
— continued

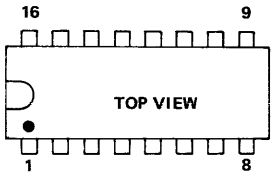
mechanical data and pin configuration (continued)

The TMS 3413 and TMS 3414 are available both in 8-lead TO-99 packages (LC) and in 16-pin dual-in-line plastic packages (NC) designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



BOTTOM VIEW

TMS 3413 LC		TMS 3414 LC	
LEAD NO.	FUNCTION	LEAD NO.	FUNCTION
1	Output 1	1	NC
2	Input 1	2	Input
3	ϕ_1	3	ϕ_1
4	V_{CC} (V_{SS})	4	V_{CC} (V_{SS})
5	Output 2	5	Output
6	Input 2	6	NC
7	ϕ_2	7	ϕ_2
8	V_{DD}	8	V_{DD}



TMS 3413 NC		TMS 3414 NC	
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	1	NC
2	NC	2	NC
3	Input 1	3	Input
4	ϕ_1	4	ϕ_1
5	V_{SS}	5	V_{SS}
6	Output 2	6	Output
7	NC	7	NC
8	NC	8	NC
9	NC	9	NC
10	Input 2	10	NC
11	ϕ_2	11	ϕ_2
12	V_{DD}	12	V_{DD}
13	NC	13	NC
14	Output 1	14	NC
15	NC	15	NC
16	NC	16	NC

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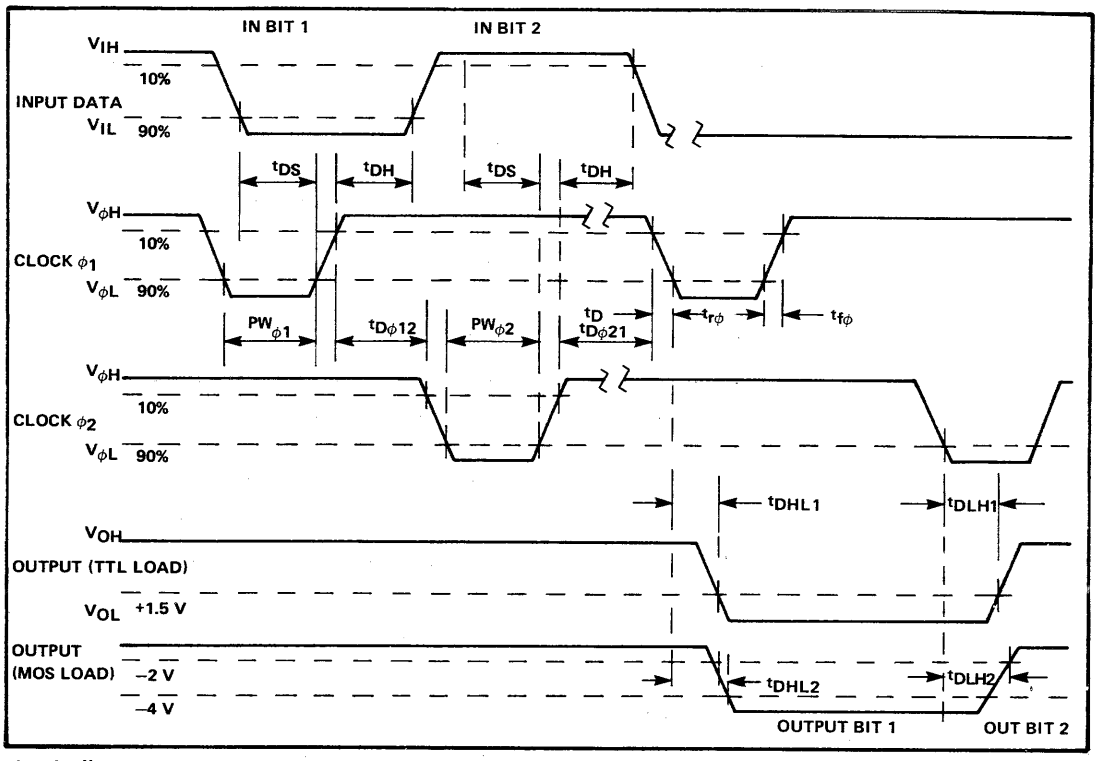
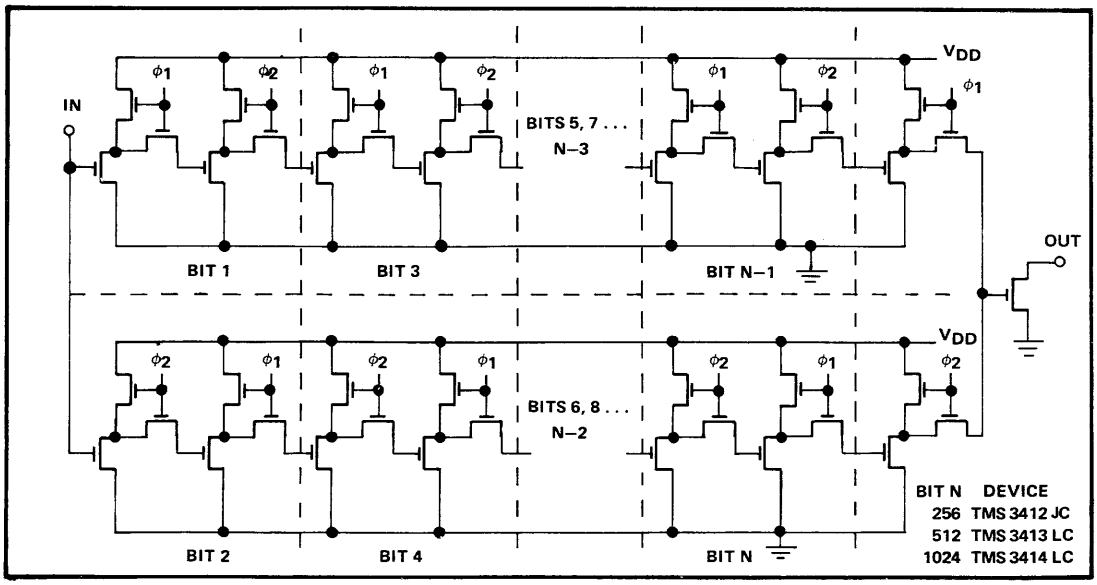
timing diagram and voltage waveforms



circuit diagram



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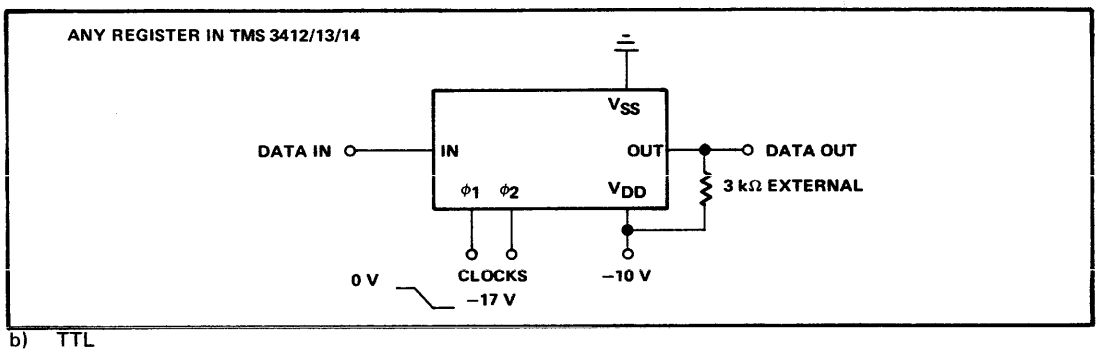
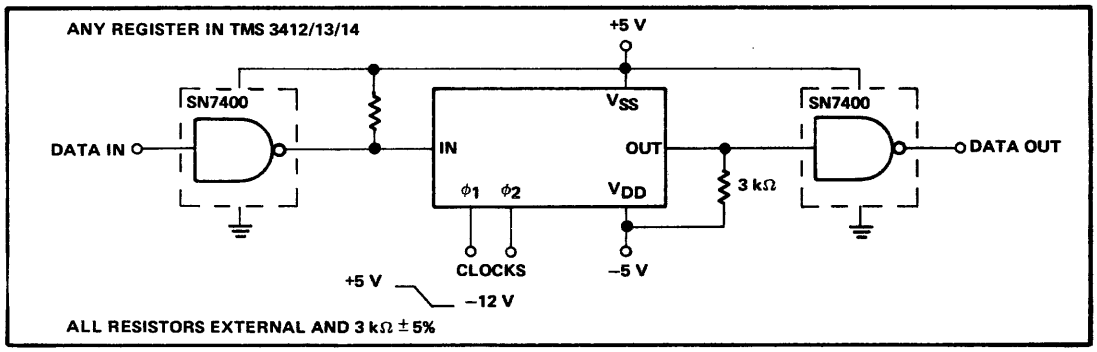
interface circuits

a) MOS



b) TTL



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1) Introduction

The information stored in a Read-Only Memory (ROM) is permanently programmed into the circuit at the time of its manufacture. Once the information is entered it cannot be changed – it can, however, be read out as often as desired. Before MOS circuits became available, the only practical means of realizing a ROM were with discrete-diode matrices, or core memories. The most obvious advantages of MOS ROMs are:

Cost – MOS typically one tenth that of diode matrix

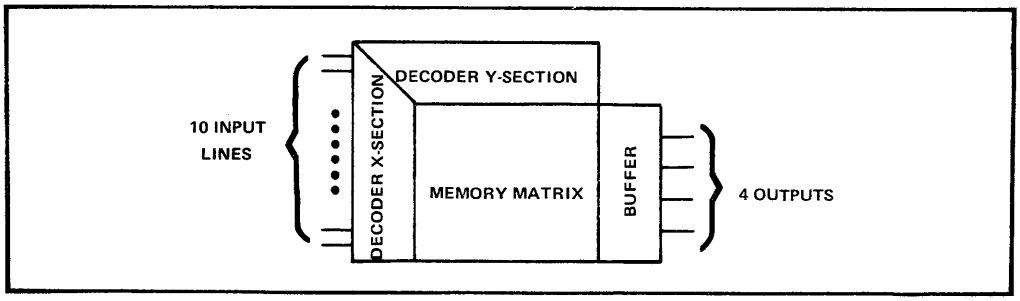
Size – MOS can put 4096 bits in a 24-pin package (chip size is 120 X 110 mil)

Speed – New MOS techniques can provide access times as low as 50 nsec.

2) Structure of an MOS ROM

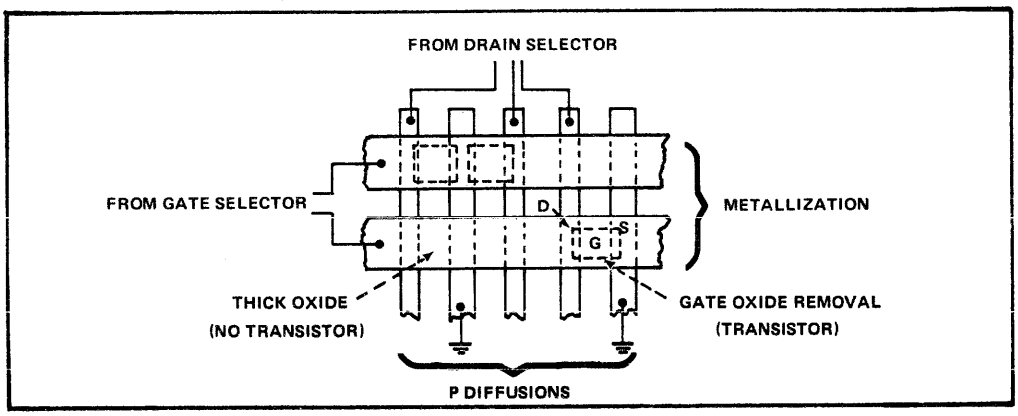
A single MOS ROM device will be made up of three sections:

- DECODER — in which the binary address is decoded and X-Y pairs of lines going to the memory matrix are enabled (one pair of X-Y lines if there is one bit per output word; two pairs of X-Y lines if there are two bits per output word, etc.)
- MEMORY MATRIX — containing as many MOS-transistor locations as there are bits in the memory.
- BUFFER — which supplies output levels for the external circuitry.



EXAMPLE 1024 x 4 ROM

Consider for example a 4096-bit ROM organized as 1024 words of 4 bits. At the intersection of every X-line and Y-line, an MOS transistor can be either constructed or omitted by growing either a thin-gate oxide or a thick-gate oxide. The absence of an MOS transistor will be interpreted by the buffer as a logic 0, and the presence of a thin-gate MOS transistor will be interpreted as a logic 1. The programming of the memory (placement of the thin-gate oxide transistors) is performed during the manufacturing process.



3) Static or Dynamic?

Aside from the organization of the ROM, which defines its bit capacity, the most important parameter in most applications is probably access time. Access time is defined as the time required for a valid output to appear after a valid input has been applied.

In a static ROM there are no clocks required. If a valid input address is applied to the memory, after the expiration of the required access time, a valid output will appear. The output will remain valid as long as the input address remains unchanged. The use of static read-only memories is very straightforward and TI has developed a complete line.

In a conventional dynamic read-only memory, the information is clocked in and clocked out. The output will only remain valid for a certain period. Dynamic read-only memories are advantageous to implementing synchronous logic. To take advantage of their logic flexibility and to allow the output to be kept valid as long as desired, TI has designed in latches on the outputs of all dynamic ROMs presently in production. TI's dynamic ROMs do not require clock drivers since these have been incorporated on the chip.

4) Typical Applications

Now that economical ROMs are available, the logic designer is taking advantage of this element. The most common areas of applications are found in:

- DISPLAYS
- COMPUTER TERMINALS
- COMPUTERS
- CALCULATORS

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The most common applications are:

a) LOOK-UP TABLES – where the output is a mathematical function of the input. In computers for military applications, trigonometric functions are commonly used. A ROM can be used to obtain the sine of an angle instead of having to compute it by algorithm.

ROM as Trigonometric Look-Up Table

Some calculators also employ Look-up tables in performing arithmetic:

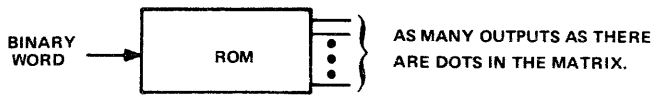
ROM as Arithmetic Look-Up Table

b) CODE CONVERSION – many applications require translating between one code and another. This is a common requirement of display manufacturers, computer terminal equipment manufacturers, and persons involved with punched card reading and processing. For example, a ROM can be designed to accept input words in EBCDIC code and convert to words of USASCII code at the output.

ROM Used for Code Conversion

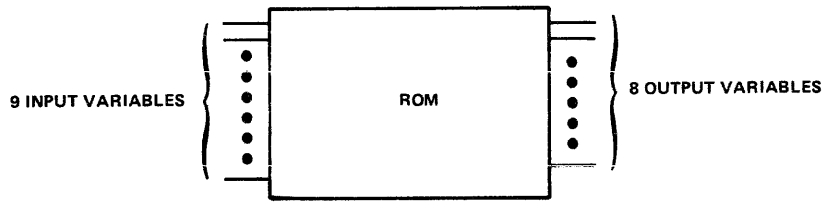
c) MICROPROGRAMMING – where a routine can be programmed directly (hard-wired programs), instead of being described (microprogram) on a stack of punched cards and then stored in the main memory. This technique is becoming more and more popular in medium-sized computers.

d) CHARACTER GENERATOR – where an alphanumeric character is represented by a binary word. The characters can be visually represented by use of nixie tubes, a dot matrix, or a segment display. An example of a ROM used as a dot-matrix character generator is shown below.



ROM Used as Character Generator

e) RANDOM LOGIC – ROMs can also be utilized to perform Boolean algebra. For example, a 4096-bit ROM organized as 512 words of 8 bits, has 9 inputs and 8 outputs. The ROM can be programmed to provide the outputs (which are Boolean functions of the input variables). The user needs only to develop the truth table for the desired logic function.



ROM USED IN PERFORMING RANDOM LOGIC

$$0_1 = f_1 (A, B, C, \ldots)$$

$$0_2 = f_2 (A, B, C, \ldots)$$

To perform sequential logic the outputs would be fed back to the inputs.

5) **TI ROMS**

a) General Purpose Static ROMs

TMS 2800 JC/NC	1024-bit capacity	256 X 4 organization
TMS 2600 JC/NC	2048-bit capacity	512 X 4 or 256 X 8 organization
TMS 2700 JC/NC	3072-bit capacity	256 X 12 organization
TMS 4400 JC/NC	4096-bit capacity	1024 X 4 or 512 X 8 organization

b) General Purpose Dynamic ROM

TMS 2300 JC/NC	2560-bit capacity	256 X 10 organization

c) Static character Generators (5 X 7 dot matrix)

TMS 2400 JC/NC	64 characters row output
TMS 4100 JC/NC	64 characters column output

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For each series of devices TI has programmed at least one off-the-shelf device. This device can be used for evaluation by customers. For instance, in the TMS 2400 JC series the TMS 2403 JC is an off-the-shelf ASCII row-output character generator and the TMS 2404 JC is an off-the-shelf EBCDIC character generator.

CUSTOM BIT PATTERNS

The programming of a single photomask permits the user to choose:

- Organization of the read-only memory
- Programming of the decode section
- Memory content
- Buffer configuration
- Chip-enable polarities

All other masks used during the processing are fixed and are common to a series of devices. For instance, all devices of the TMS 2600 JC series (2048-bit static ROM) use the same masks except for the gate-oxide-removal mask, which contains the custom pattern.

TI uses computer methods to assure a quick and foolproof implementation of a custom bit pattern. This also reduces the cost of the implementation. A "SOFTWARE PACKAGE" bulletin is used to transmit the customer inputs to TI, for each series of devices, these packages are available from the TI Sales Office. The Software Package describes the format in which the inputs should be transmitted for best interface with the computer. For character generators the Software Package includes grid on which the customer can map the desired outputs. For read-only memories the Software Package describes the format used for writing the truth table of the ROM on punched cards. Once the Software Package is received by TI, it can be directly fed into a computer, or punched cards can be prepared from it and the cards can be fed into the computer.

The first computer output is a checkprint. For a read-only memory the checkprint is a reconstitution of the truth table. In the case of a character generator, an overlay is produced. The overlay is in the same scale as the map included in the Software Package and permits easy verification of the punched cards. The checkprint is used for TI verification and a copy is sent to the customer.

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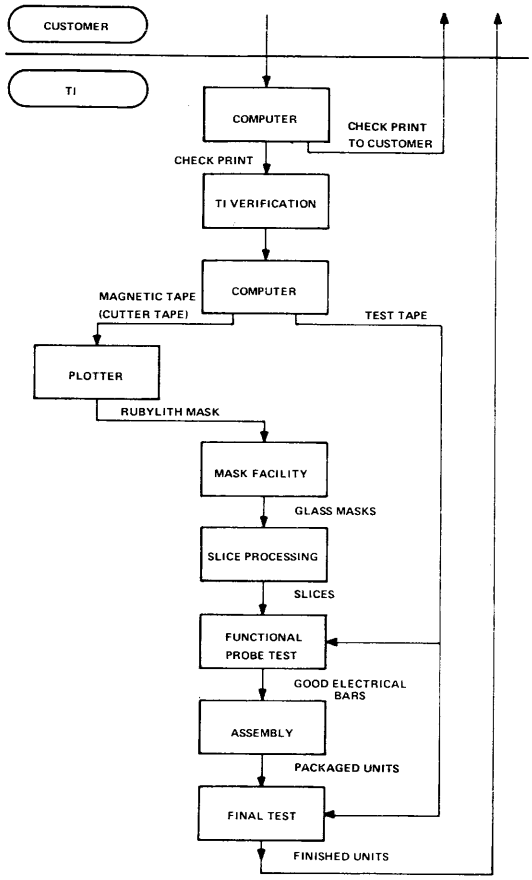

Once the verification has been performed, the computer generates a magnetic tape that will be used to drive a plotter, and a testing tape to be used for probe test and at final test.

The magnetic tape (cutter tape) is used to drive a plotter which cuts a film of rubylith mask. The rubylith mask, when pealed, is an enlargement of the gate-oxide-removal mask, which is used to store the custom bit pattern. A glass mask is then made from the rubylith by a photographic process (reduction, step and repeat). This mask is used in production of the slice.

A slice contains many individual chips. Each chip is individually tested on a probe tester which uses the test tape generated by the computer.

The chips are packaged and the completed units are final tested (logic and parametric tests). Finished units are then delivered to the customer.

TMS 2300 JC, TMS 2300 NC
2560-BIT DYNAMIC READ-ONLY MEMORY

FEBRUARY, 1971

features

- **2560-bit capacity (256 x 10)**
- **Dynamic operation and static storage**
- **Maximum access time — 550 ns**
- **Maximum cycle time — 550 ns**
- **Full TTL/DTL compatible without external components**
- **TTL-level single clock**
- **Push-pull output buffers**
- **24- or 28-pin CDIP or plastic package**
- **Chip enable**

description

The TMS 2300 JC/NC series is a family of dynamic read-only memories, each having a capacity of 2560 bits.

Programming the memory contents is accomplished by changing a single mask during device fabrication. The memory contents consist of 256 words of 10 bits.

A chip enable input is available.

A single clock pulse line is required (TTL level).

Low-threshold, thick-oxide, MOS P-channel enhancement-mode circuitry has been employed to reduce power dissipation and permit easy interface between the TMS 2300 JC/NC and bipolar integrated circuits (no external pull-up resistors required).

"TMS 2300 JC" designates a unit mounted in a hermetically sealed ceramic dual-in-line package. A unit mounted in a dual-in-line plastic package is numbered "TMS 2300 NC".

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The TMS 2300 JC/NC features dynamic operation; the output data is synchronized by an externally provided clock pulse.

By means of a dc output storage register, this device also performs a static operation; the output data will remain valid as long as a new clock pulse is not provided (even if the input address has changed in the meantime).

Access time is defined as the time between a change of data on any address input and the change of data on the output of the device.

Cycle time is defined as the period of the clock. The minimum cycle time corresponds to the minimum time interval between two address signals.

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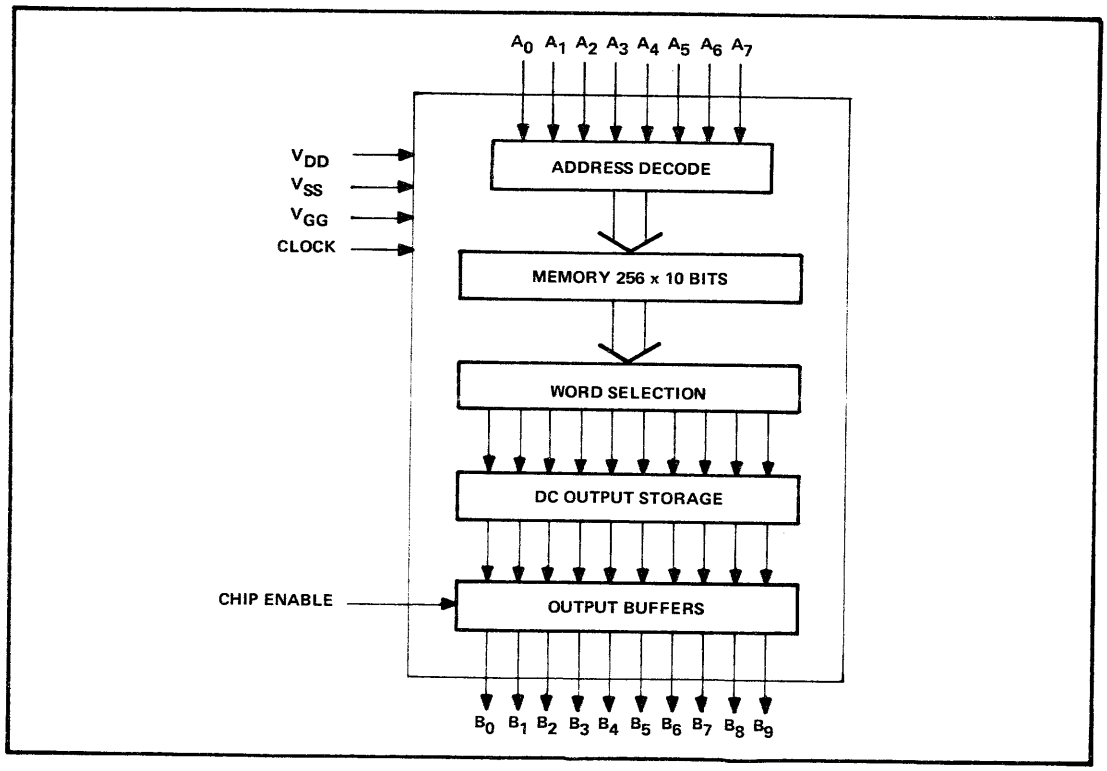
operation (continued)

A logical 0 on the Chip-Enable input will cause the outputs to become open-circuits. The number of words per output is increased by hardwiring together the outputs of different devices. The internal operation of the device is not inhibited by the 0 state of Chip-Enable; any change of the address inputs results in the selection of a new 10-bit word, which is then transferred into the dc output register by the next clock pulse. The data outputs are up-dated as soon as the Chip-Enable signal goes back to logical 1.

functional block diagram and pin breakout



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{GG} range (See Note 1)	−20 V to 0.3 V
Clock input voltage range (See Note 1)	−20 V to 0.3 V
Data input voltage range (See Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to +85°C
Storage temperature range	−55°C to +150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	4.75	5.0	5.5	V
Drain supply V_{DD}	0.0	0	0.0	V
Gate supply V_{GG}	−11.0	−12.0	−13.0	V
Logic Levels (Data Inputs)				
Input HIGH level (logical 1) V_{IH}	3.5			V
Input LOW level (logical 0) V_{IL}			0.6	V
Clock Voltage Levels				
Clock HIGH level (logical 1) $V_{\phi H}$	3.5			V
Clock LOW level (logical 0) $V_{\phi L}$			0.6	V
Pulse Timing				
Clock pulse transition $t_{r\phi}$, $t_{f\phi}$			100	μs
Clock pulse width PW_{ϕ}	0.250		100	μs
Minimum clock frequency	0			MHz
Pulse Spacing				
Data setup (Note 1) t_{DS} at 25°C		240	290	ns
Data setup (Note 1) t_{DS} at 85°C		320	380	ns
Data Pulse Overlap Clock				
t_{DOC}	150			ns

NOTE 1: The clock input has to be at logic 0 during the minimum data setup (t_{DS} see timing diagram).

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{IL}	Input Leakage Current	−15 V applied to input			1	μA
Output Voltage Levels (See Note 2)						
V_{OL}	Output LOW level (logic 0)	1 TTL gate, C_L = 20 pF			0.45	V
V_{OH}	Output HIGH level (logic 1)	1 TTL gate, C_L = 20 pF	4.0			V
V_{OL}	Output LOW level (logic 0)	MOS load, C_L = 20 pF			0.3	V
V_{OH}	Output HIGH level (logic 1)	MOS load, C_L = 20 pF	4.0			V
Output Current						
I_{OSC}	Short circuit	Output shorted to ground			2.8	mA
R_{out}	Output resistance	Chip enable = 1, V_{out} = logic 0			300	Ω
R_{out}	Output resistance	Chip enable = 0	1			MΩ
Power Supply Current Drain (See Note 3)						
I_{SS}	Substrate supply			13.0		mA
I_{DD}	Drain supply			0		mA
I_{GG}	Gate supply			−13.0		mA
P_D	Power dissipation			225		mW

NOTE 2: For the final test purposes, worst-case TTL load is simulated by a resistor of 3.3 kΩ and 20 pF. An MOS load is simulated by a resistor of 20 kΩ and a capacitance of 20 pF.

NOTE 3: The current sink by the V_{SS} supply is sourced by the V_{GG} supply.

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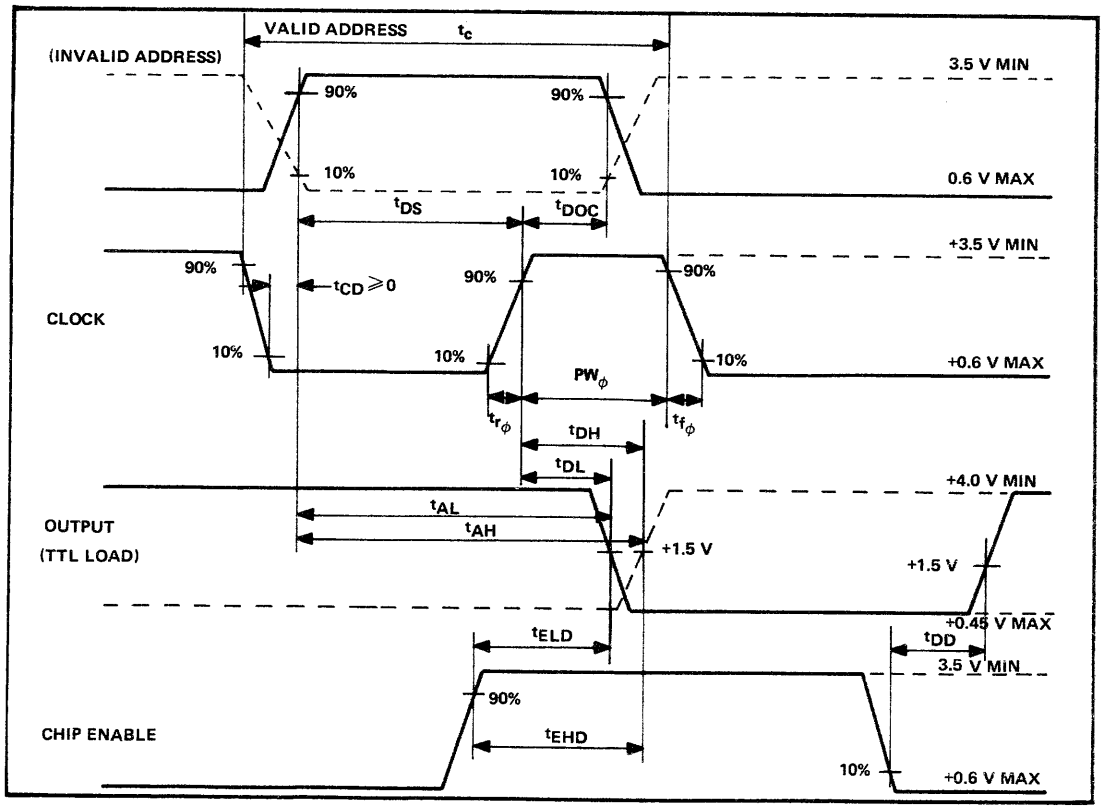
dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Cycle Time t_c		Load: 1 TTL gate, 20 pF		490	550	ns
Output Logic Delay (See Note 4)						
t_{DL}	Output LOW level	Load: 1 TTL gate, 20 pF			170	ns
t_{DH}	Output HIGH level	Load: 1 TTL gate, 20 pF			250	ns
Access Time (See Note 4)						
t_{AL}	Output LOW level	Load: 1 TTL gate, 20 pF		400	500	ns
t_{AH}	Output HIGH level	Load: 1 TTL gate, 20 pF		470	550	ns
Capacitance						
C_{IN}	Input	V_{in} = +5.0 V, f = 2 MHz		3	7	pF
C_ϕ	Clock	V_{in} = +5.0 V, f = 2 MHz		5	8	pF
Chip Enable Delay						
t_{ELD}	Enable output delay LOW level	Load = 20 pF to V_{DD}			150	ns
t_{EHD}	Enable output delay HIGH level	Load = 20 pF to V_{DD}			150	ns
t_{DD}	Disable output delay	Load = 20 pF to V_{DD}, 3.6 kΩ to V_{SS}			240	ns

NOTE 4: Output delay and access time are defined for V_{OUT} = +1.5 V (see timing diagram).

timing diagram and voltage waveforms



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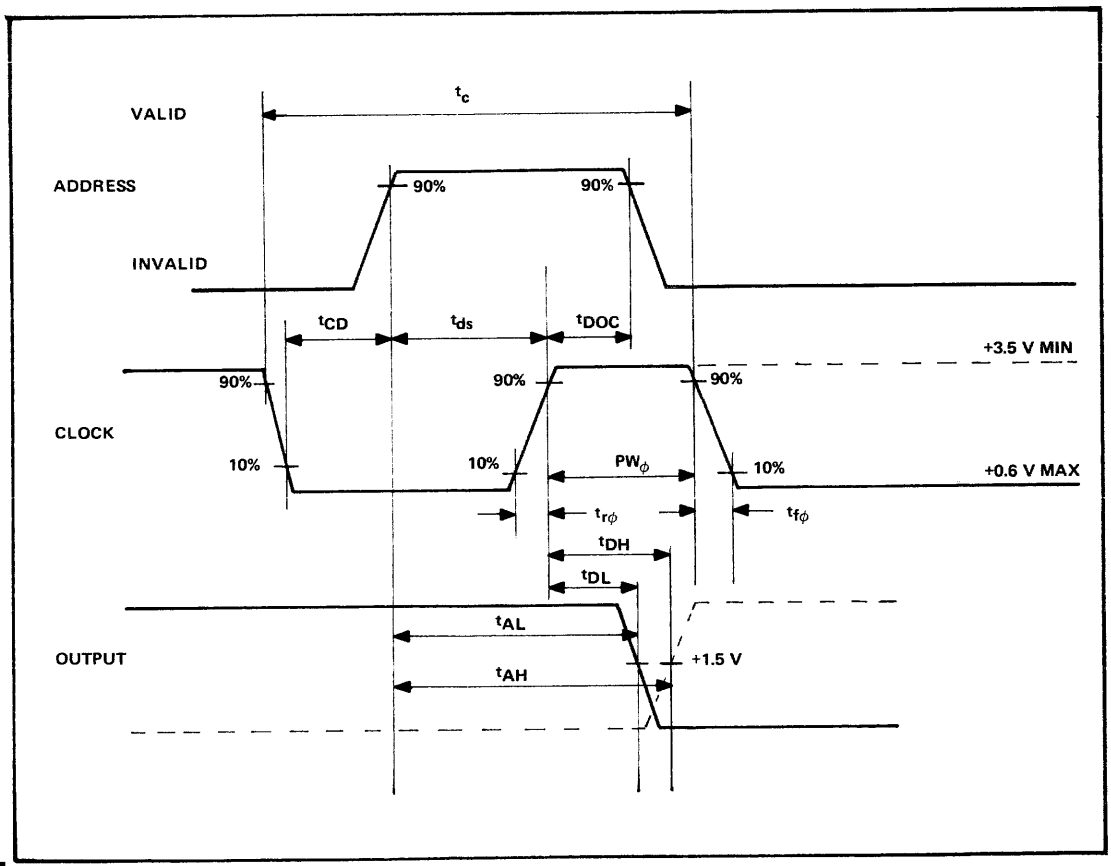
timing diagram and voltage waveforms (continued)

For specific applications the following timing scheme may be used for a t_{CD} (clock-to-address delay) of at least 150 ns and a t_{ds} (data set-up time) of at least 150 ns.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_c	Cycle Time	Load: 1 TTL gate, 20 pF		490	550	ns
Output Logic Delay (See Note 5)						
t_{DL}	Output LOW level	Load: 1 TTL gate, 20 pF		180	250	ns
t_{DH}	Output HIGH level	Load: 1 TTL gate, 20 pF		290	240	ns

NOTE 5: This timing scheme does not affect chip enable timing.



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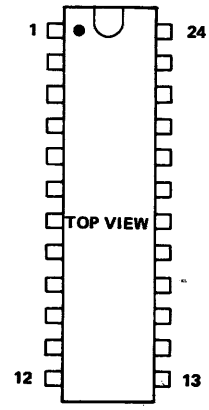
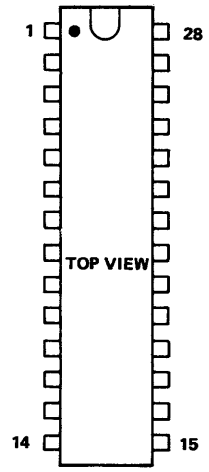
mechanical data and pin configuration

The device is normally mounted in a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2300 JC) or a 24-pin plastic dual-in-line package (TMS 2300 NC), with pin configuration as follows:



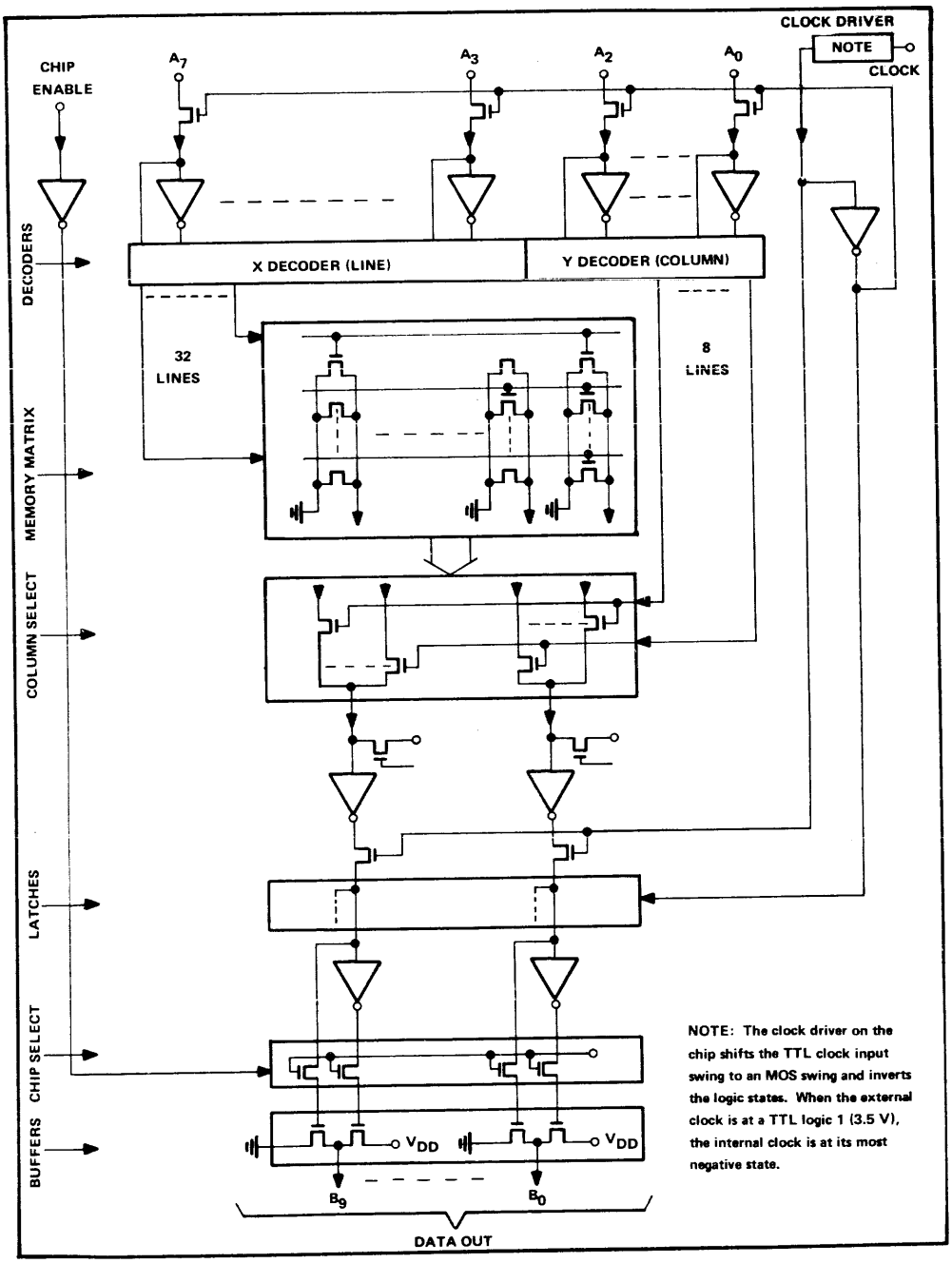
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{SS}	13	Chip Enable
2	V_{GG}	14	V_{DD}
3	Input A_1	15	Output B_0
4	Input A_0	16	Output B_1
5	Input A_2	17	Output B_2
6	Input A_7	18	Output B_3
7	Input A_6	19	Output B_4
8	Input A_5	20	Output B_5
9	Input A_4	21	Output B_6
10	Clock	22	Output B_7
11	Input A_3	23	Output B_8
12	No Connection	24	Output B_9

Upon special request the device may be mounted in a 28-pin hermetically sealed ceramic dual-in-line package (TMS 2300 JC) or a 28-pin plastic dual-in-line package (TMS 2300 NC). (See MOS/LSI packaging section.) In this case the pin configuration is:



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	15	No Connection
2	No connection	16	Chip Enable
3	V_{SS}	17	V_{DD}
4	V_{GG}	18	Output B_0
5	Input A_1	19	Output B_1
6	Input A_0	20	Output B_2
7	Input A_2	21	Output B_3
8	Input A_7	22	Output B_4
9	Input A_6	23	No Connection
10	Input A_5	24	Output B_5
11	Input A_4	25	Output B_6
12	No Connection	26	Output B_7
13	Clock	27	Output B_8
14	Input A_3	28	Output B_9

The packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



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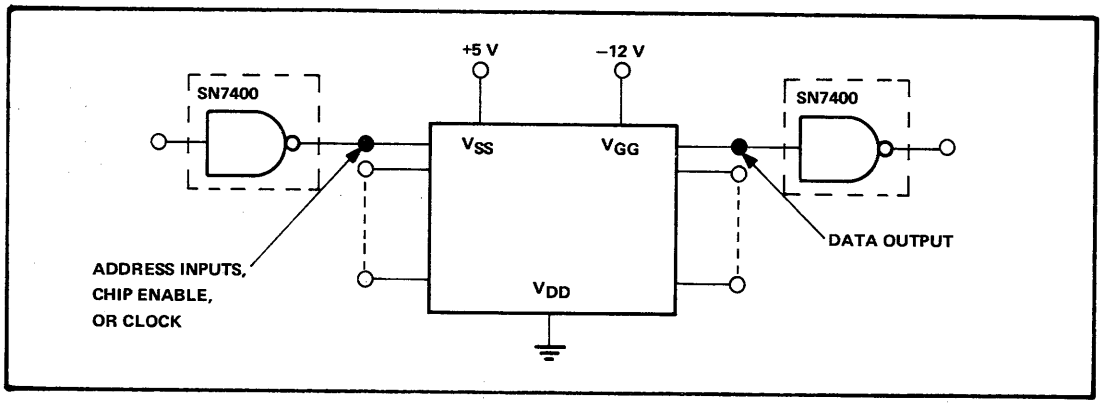
interface circuits

a) TTL interface

No components are needed for TTL interface



b) Increase of noise margin

Noise margin may be increased by use of pull-up resistors to +5 V on the inputs (see schematic on page 7).

off-the-shelf devices

The TMS 2301 JC/NC has been programmed by TI to demonstrate the capabilities of the TMS 2300 JC/NC series. It is available off-the-shelf as a sample device.

truth table, TMS 2301 JC/NC

INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$	INPUT ADDRESS	$B_9B_8B_7B_6B_5B_4B_3B_2B_1B_0$
0	0000000000	64	1110000000	128	1111110000	192	1111111110
1	0000000000	65	1110000000	129	1111110000	193	1111111110
2	0000000000	66	1110000000	130	1111110000	194	1111111110
3	0000000000	67	1110000000	131	1111110000	195	1111111100
4	0000000000	68	1110000000	132	1111100000	196	1111111100
5	0000000000	69	1110000000	133	1111100000	197	1111111100
6	0000000000	70	1100000000	134	1111100000	198	1111111100
7	0000000000	71	1100000000	135	1111100000	199	1111111100
8	1000000000	72	1110000000	136	1111110000	200	1111111110
9	1000000000	73	1110000000	137	1111110000	201	1111111110
10	0000000000	74	1110000000	138	1111110000	202	1111111110
11	0000000000	75	1110000000	139	1111110000	203	1111111110
12	0000000000	76	1110000000	140	1111110000	204	1111111100
13	0000000000	77	1110000000	141	1111110000	205	1111111100
14	0000000000	78	1110000000	142	1111100000	206	1111111100
15	0000000000	79	1110000000	143	1111100000	207	1111111100
16	1000000000	80	1111000000	144	1111110000	208	1111111110
17	1000000000	81	1111000000	145	1111110000	209	1111111110
18	1000000000	82	1110000000	146	1111110000	210	1111111110
19	1000000000	83	1110000000	147	1111110000	211	1111111110
20	0000000000	84	1110000000	148	1111110000	212	1111111110
21	0000000000	85	1110000000	149	1111110000	213	1111111110
22	0000000000	86	1110000000	150	1111110000	214	1111111100
23	0000000000	87	1110000000	151	1111110000	215	1111111100
24	1000000000	88	1111000000	152	1111111000	216	1111111100
25	1000000000	89	1111000000	153	1111111000	217	1111111110
26	1000000000	90	1111000000	154	1111110000	218	1111111110
27	1000000000	91	1111000000	155	1111110000	219	1111111110
28	1000000000	92	1110000000	156	1111110000	220	1111111110
29	1000000000	93	1110000000	157	1111110000	221	1111111110
30	0000000000	94	1110000000	158	1111110000	222	1111111110
31	0000000000	95	1110000000	159	1111110000	223	1111111110
32	1000000000	96	1111000000	160	1111111000	224	1111111111
33	1000000000	97	1111000000	161	1111111000	225	1111111111
34	1000000000	98	1111000000	162	1111111000	226	1111111110
35	1000000000	99	1111000000	163	1111111000	227	1111111110
36	1000000000	100	1111000000	164	1111110000	228	1111111110
37	1000000000	101	1111000000	165	1111110000	229	1111111110
38	1000000000	102	1110000000	166	1111110000	230	1111111110
39	1000000000	103	1110000000	167	1111110000	231	1111111110
40	1100000000	104	1111000000	168	1111111000	232	1111111111
41	1100000000	105	1111000000	169	1111111000	233	1111111111
42	1000000000	106	1111000000	170	1111111000	234	1111111111
43	1000000000	107	1111000000	171	1111111000	235	1111111111
44	1000000000	108	1111000000	172	1111111000	236	1111111110
45	1000000000	109	1111000000	173	1111111000	237	1111111110
46	1000000000	110	1111000000	174	1111110000	238	1111111110
47	1000000000	111	1111000000	175	1111110000	239	1111111110
48	1100000000	112	1111100000	176	1111111000	240	1111111111
49	1100000000	113	1111100000	177	1111111000	241	1111111111
50	1100000000	114	1111000000	178	1111111000	242	1111111111
51	1100000000	115	1111000000	179	1111111000	243	1111111111
52	1000000000	116	1111000000	180	1111111000	244	1111111111
53	1000000000	117	1111000000	181	1111111000	245	1111111111
54	1000000000	118	1111000000	182	1111111000	246	1111111110
55	1000000000	119	1111000000	183	1111111000	247	1111111110
56	1100000000	120	1111100000	184	1111111100	248	1111111111
57	1100000000	121	1111100000	185	1111111100	249	1111111111
58	1100000000	122	1111100000	186	1111111000	250	1111111111
59	1100000000	123	1111100000	187	1111111000	251	1111111111
60	1100000000	124	1111000000	188	1111111000	252	1111111111
61	1100000000	125	1111000000	189	1111111000	253	1111111111
62	1000000000	126	1111000000	190	1111111000	254	1111111111
63	1000000000	127	1111000000	191	1111111000	255	1111111111

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data encoding – software format

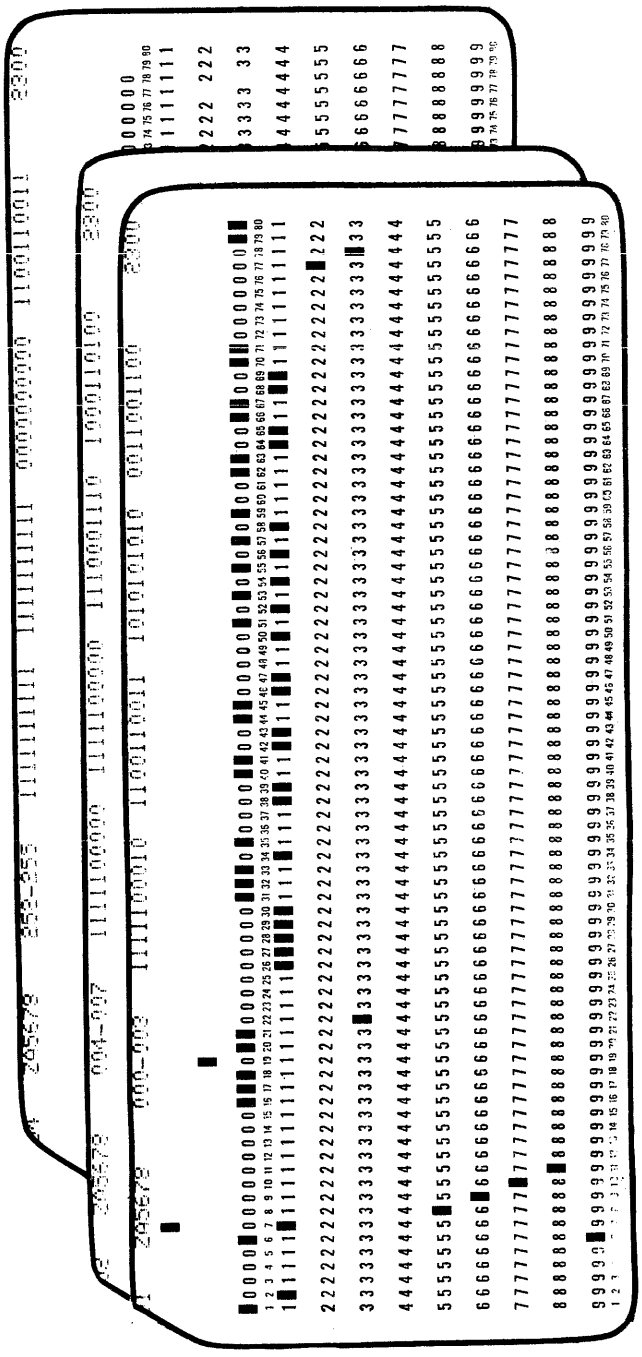
Programming information for the TMS 2300 JC/NC should be transmitted to TI in the form of a DECK OF 64 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Each card in the data deck describes the outputs for four input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

Column Nos.

1–2	Punch the sequential card starting with 01 and ending with 64 (I2).
3–5	Blank
6–11	Punch either TM or ZA followed by a four digit number as supplied by MOS Marketing (TI part number.
12–15	Blank
16–18	Punch the address associated with the first output word described on the card (I3).
19	Punch a – (minus).
20–22	Punch the address associated with the last output word described on the card (I3).
	NOTE: Address locations are the numbers 000 through 255 and are derived from the binary-to-decimal conversion of the input address A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0. A_0 is considered the least-significant binary bit.
23–25	Blank
26–35	Punch the data associated with the outputs of the first memory location described on the card (10I1).
36–37	Blank
38–47	Punch the data associated with the outputs of the second memory location described on the card (10I1).
48–49	Blank
50–59	Punch the data associated with the outputs of the third memory location described on the card (10I1).
60–61	Blank
62–71	Punch the data associated with the outputs of the fourth memory location described on the card (10I1).
	NOTE: Outputs are defined in groups of ten. The order is B_9, B_8, B_7, B_6, B_5, B_4, B_3, B_2, B_1, B_0.
72–76	Blank
77–80	Punch 2300
	NOTE: For both inputs and outputs logic levels are punched in the form of 1s and 0s. Positive logic is assumed throughout. A logic 1 is the most positive voltage level and a logic 0 is the most negative voltage level.

TMS 2300 JC/NC — first, second and last cards



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TMS 2400 JC, TMS 2400 NC
ROW OUTPUT CHARACTER GENERATOR

JANUARY 1971

features

- Static operation
- 2240-bit capacity
- 64 characters of 35 bits (5 x 7)
- 7-Input character decoder
- 3-Input row decode
- 800-ns character access time
- Chip enable
- Open-drain or double-ended buffers
- TTL compatible
- Dual-in-line package

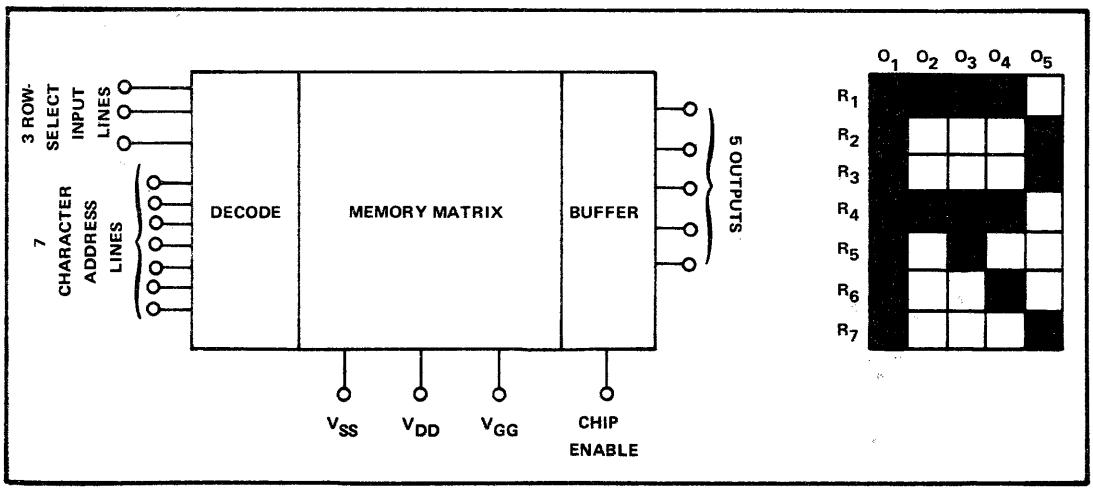
description

The TMS 2400 JC/NC series is a family of read-only-memory subsystem components manufactured using MOS P-channel enhancement-mode technology. All components in the series contain a 7-bit parallel-input character-address decoder and a 3-bit parallel-input row-address decoder, both complete with input inverters. Either open-drain or double-ended output buffers are provided for flexibility in external interfaces. The memory organization and data are permanently stored by programming a single mask during manufacture.

The memory is organized to function primarily as a row-output character generator. The five outputs represent a row in a 5 x 7 dot matrix.

"TMS 2400 JC" designates a unit mounted in a 28-pin hermetically sealed ceramic dual-in-line package, and "TMS 2400 NC" is used for a unit mounted in a 28-pin plastic package.

functional diagram



operation

The TMS 2400 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip enable) remains unchanged.

"Access time" is defined as the time required for all outputs to reach the minimum 1 level or maximum 0 level with the correct data. This time is measured from the point at which all address inputs and chip enable inputs are valid.

character scanning

The output character appears as a 7-word sequence on each of the five output lines. The sequence is controlled by the 3 row-select lines. The five outputs represent a row in a 5 x 7 character matrix. The row address can remain fixed while the character address changes (raster scan), or the character address may remain fixed while the row address changes (vertical or character scan).

row select truth table

ROW SELECT (NEGATIVE LOGIC)			SELECTS ROW
R_{s3}	R_{s2}	R_{s1}	
0	0	0	None
0	0	1	R 1
0	1	0	R 2
0	1	1	R 3
1	0	0	R 4
1	0	1	R 5
1	1	0	R 6
1	1	1	R 7

output buffers

The output buffers of the TMS 2400 JC/NC may be programmed to be either single-ended (open drain) to drive TTL/DTL logic, or double-ended to drive MOS logic.

The number of characters is increased by hardwiring together the outputs of different chips. Note that when using the hardwired output technique, all the chips that are hardwired together at the output should be single-ended chips.

chip enable

The chip enable may be programmed to be either a 1 or a 0.

The decoder will accept a 7-bit parallel input. Because only 6 bits are required in order to give out the 64 input words, the seventh bit may be used as an extra chip enable in single-ended operations.

A disable input on the chip enable input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

logic definition

Negative logic is assumed on the inputs.

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

An output blank is defined as the logic 1 output level, while an output dot is defined as the logic 0 output level.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−11	−14	−16	V
Supply voltage V_{GG}	−22	−28	−29	V
Input, row select and enable, logic 1	−9	−14	−16	V
Input, row select and enable, logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER (See Note 1)		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(1)}$	Output blank current (open drain)	−14 V applied to output			10	μA
$I_{out(0)}$	Output dot current (open drain)	−14 V applied to output	3	5		mA
$I_{out(0)}$	Output dot current (open drain)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	2	3		mA
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 0.5 mA		−0.7	−2	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1 mA		−1.4	−2.5	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 1.5 mA		−2.0	−4	V
$V_{out(0)}$	Output dot voltage (open drain)	I_O = 2 mA		−3	−5	V
$V_{out(1)}$	Output blank voltage (push-pull)	R_L = 1 mΩ	−10			V
$V_{out(0)}$	Output dot voltage (push-pull)	R_L = 1 mΩ			−2	V
	Power dissipation (Note 2)			450		mW
	Input leakage	−14 V applied to input			1	μA
I_{DD}	Drain current			20	30	mA
I_{GG}	Gate current			5	8.5	mA
	Input capacitance				10	pF

NOTES: 1. All voltages are measured with respect to V_{SS}.
2. Open-drain buffer, all outputs blank.

switching characteristics, under nominal operating conditions and at 25°C unless otherwise noted (refer to switching diagram)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character access time (open drain) TTL load			550	900	ns
Character access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		650	1200	ns
Row access time (open drain) TTL load			450	750	ns
Row access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		500	900	ns
Chip enable access time (open drain) TTL load			100	250	ns
Chip enable access time (open drain) TTL load	V_{SS} = +12 V, V_{DD} = −0 V, V_{GG} = −12 V		125	300	ns

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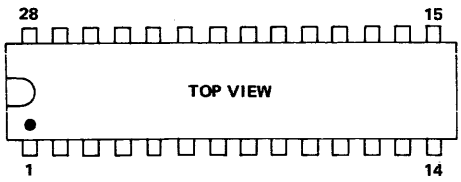
TMS 2400 JC, TMS 2400 NC
ROW OUTPUT CHARACTER GENERATOR

mechanical data

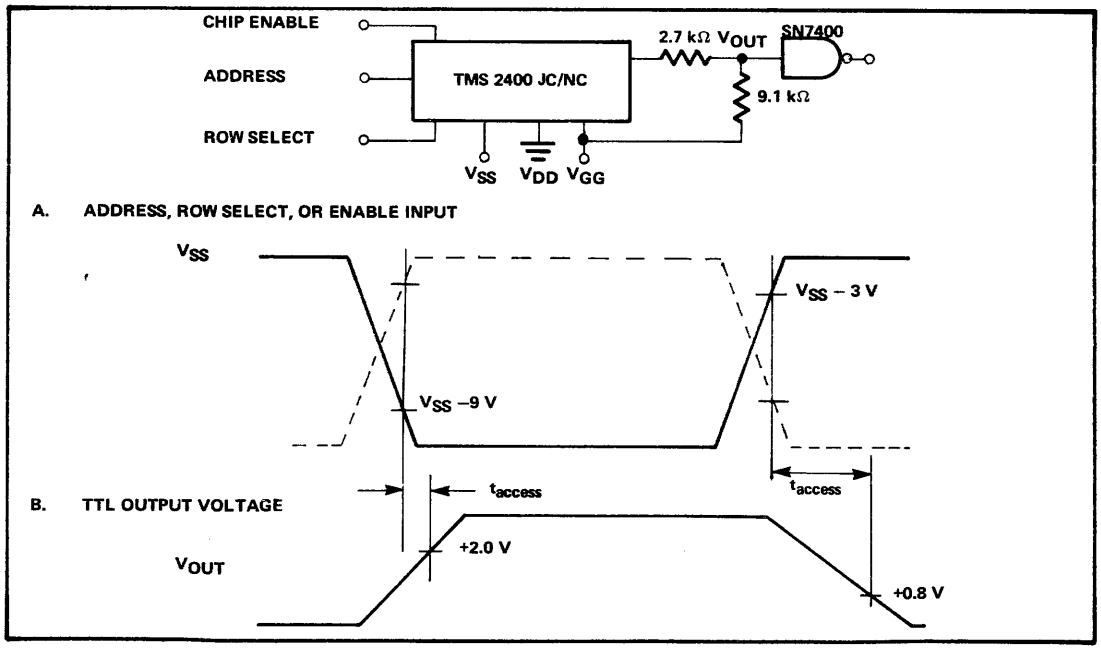
This device is available in both a 28-pin hermetically sealed ceramic dual-in-line package (TMS 2400 JC) and a 28-pin plastic package (TMS 2400 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	No connection	15	V_{SS}
2	RS_1	16	No connection
3	RS_2	17	V_{DD}
4	RS_3	18	No connection
5	No connection	19	I_1
6	O_1	20	I_2
7	O_2	21	I_3
8	O_3	22	I_4
9	O_4	23	I_5
10	O_5	24	I_7
11	No connection	25	No connection
12	Enable	26	V_{GG}
13	No connection	27	No connection
14	No connection	28	I_6

switching circuit and timing diagram (open-drain buffer, TTL load)



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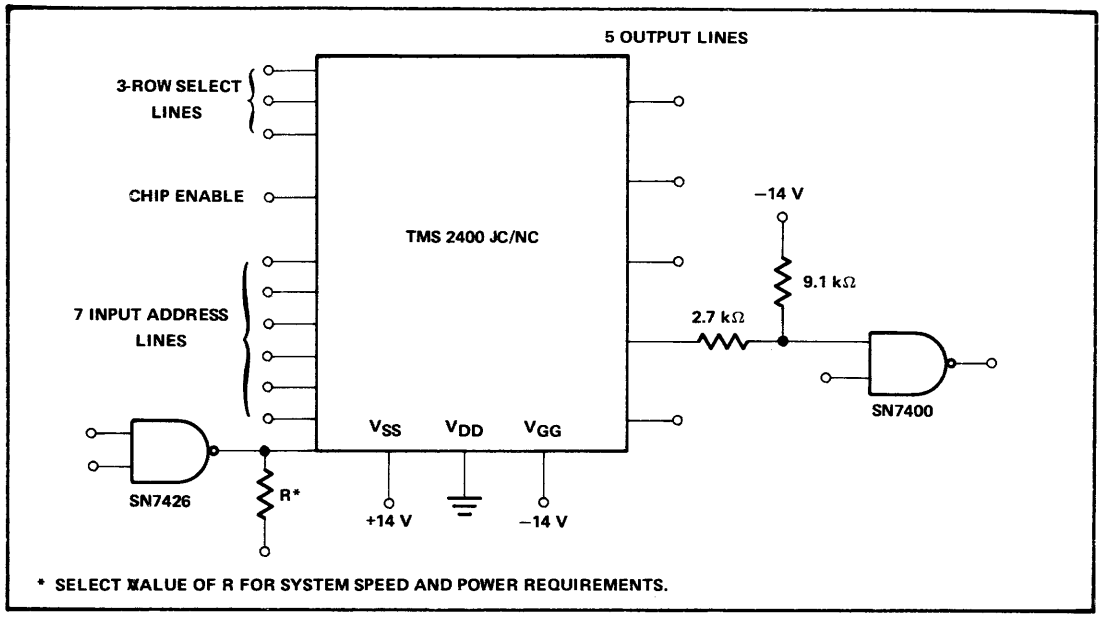
interfacing TMS 2400 JC/NC in a TTL system



custom circuits

The TMS 2400 JC/NC series is programmed during the gate oxide removal stage of manufacturing. Only one mask per unique design need be created and all other processing steps remain the same for all devices. Options available to the customer during programming are:

- Character Format
- Enable Logic Polarity
- Single- or Double-ended Outputs

The TMS 2400 JC/NC series may also be used in microprogramming applications wherever a 448-word x 5-bit ROM may be useful.

Encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets (Software Package) are used. These encoding sheets are available from the TI sales offices.

standard circuits

Because certain codes are widely used, TI has created a series of standard devices that are available off-the-shelf and for which there is no coding charge. The most widely used standard device is: TMS 2403 JC/NC USASCII CODE (See attached character format).

standard circuits (continued)

Organization:

64-Character Storage

35-Bit Character Matrix

Chip Enable = 1

Open-Drain outputs

Other Available Standard Circuits:

TMS 2404 JC/NC – EBCDIC Character Generator (See attached character format)

64-Character Storage

35-bit Character Matrix

Chip Enable = 1

Open-Drain outputs

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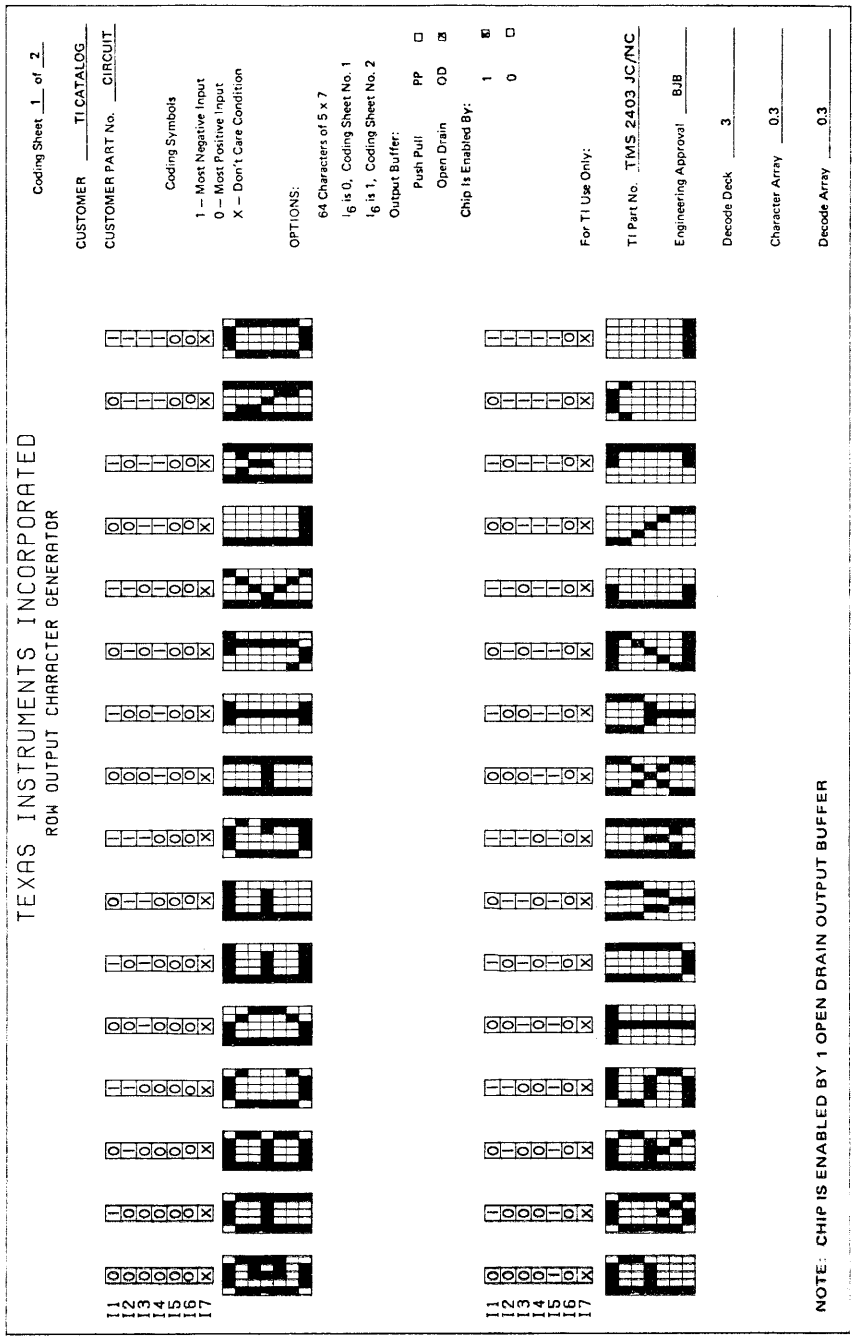

TMS 2403 JC/NC Character Font

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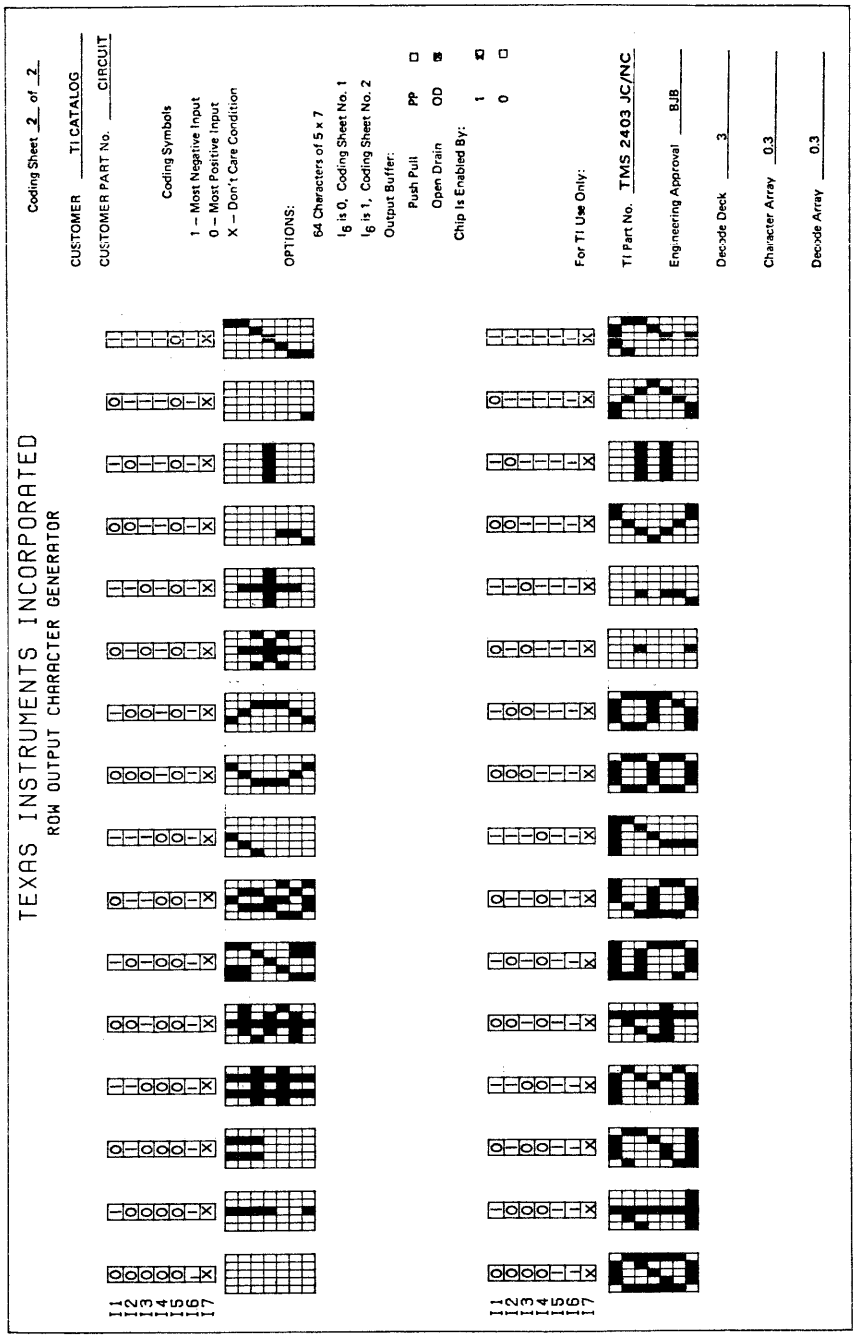

TMS 2403 JC/NC Character Font

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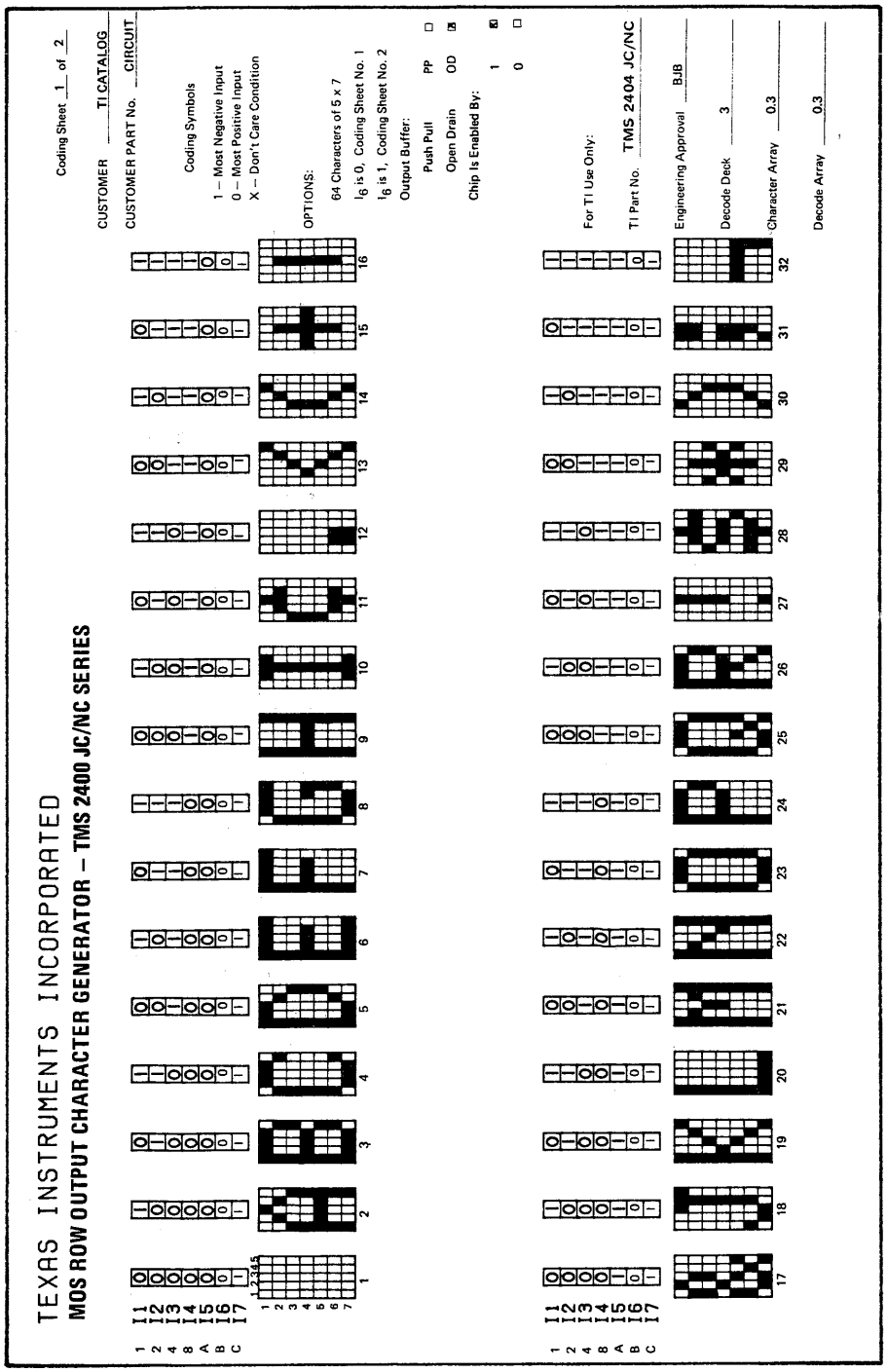

TMS 2404 JC/NC Character Font

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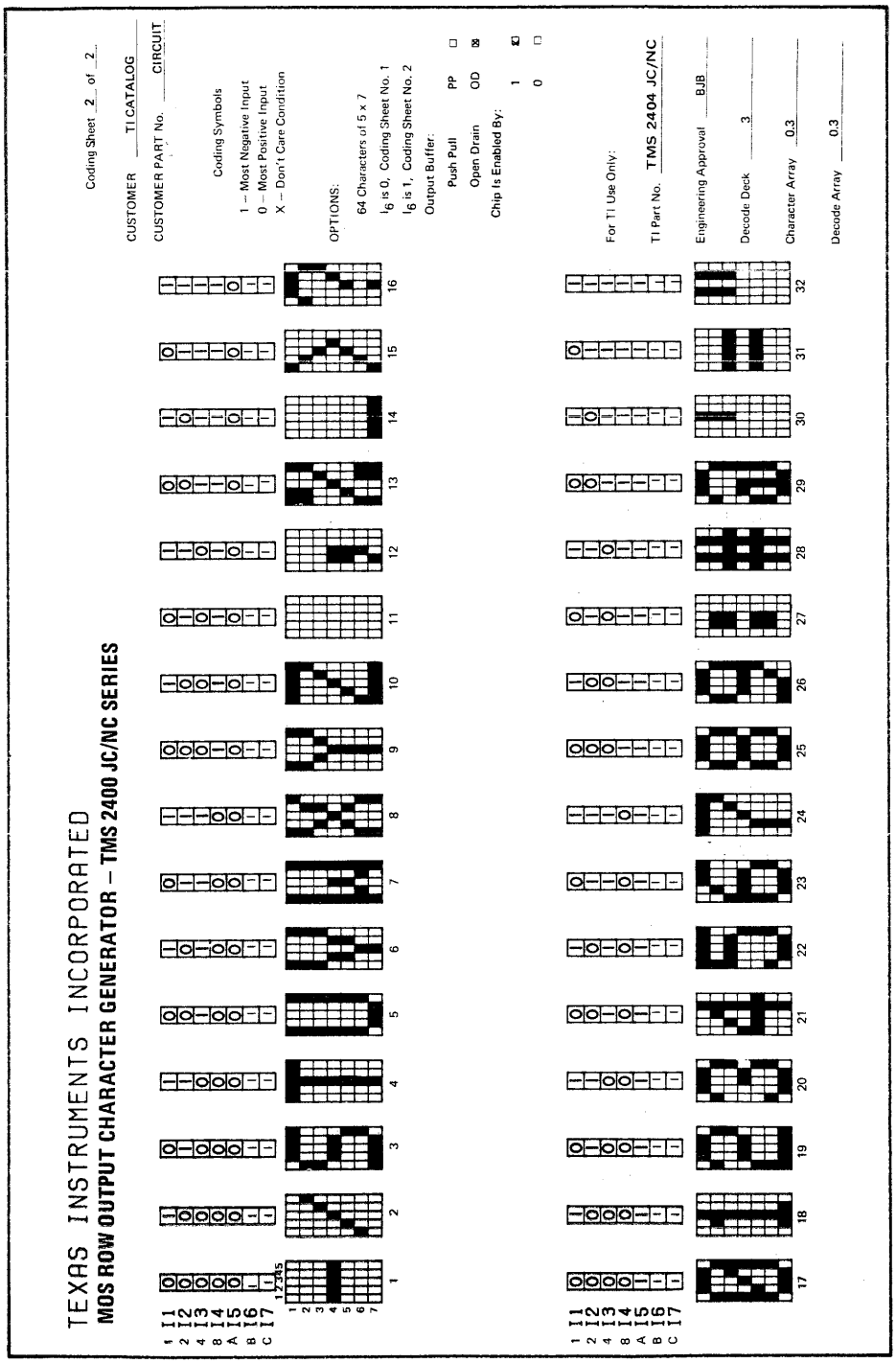

TMS 2404 JC/NC Character Font

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TMS 2500 JC, TMS 2500 NC
2560-BIT STATIC READ-ONLY MEMORY

features

- **Full TTL compatibility**
- **Two organizations available**
  - **512 words of 5 bits; 64 characters of 40 bits (5 x 8)**
  - **256 words of 10 bits; 32 characters of 80 bits (8 x 10)**
- **Static operation**
- **6-input character decoder**
- **3-input column or row-select decoder**
- **Typical access time — 350 ns**
- **Two programmable chip select inputs**
- **Push-pull output buffers**
- **Low threshold technology**
- **24-pin CDIP or 24-pin plastic package**

description

The TMS 2500 JC/NC series is a family of static character generators. Each of these devices has 2560-bit capacity.

Programming the memory content, chip organization and chip select is accomplished by changing a single mask during device fabrication.

In character generator applications, the 6-input decoder is employed for character address and the 3-input decoder is used for column/row select. In ROM applications all 9 inputs are used as a single decoder.

The output buffer is capable of driving one 74 series TTL gate or eight 74L series gates — with no external components.

"TMS 2500 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 2500 NC" is used for a unit mounted in a 24-pin plastic package.

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Featuring static operation, the TMS 2500 JC/NC requires no clocks. The output data remains valid as long as the input address (including chip select) remains unchanged. Access time is defined as the duration from the time the data on all logic inputs and chip select lines is valid to the time the output of a TTL gate is valid. (See switching circuit.)

In the 512 x 5 configuration there are two chip-select lines. The user chooses which logic input combination in these two lines enables the chip. For any other logic combination on these chip-select lines, the chip will be disabled (floating outputs).

In the 256 x 5 configuration the input I_9 may be used as a third chip select.

Any or all of the chip select inputs may be programmed as Don't Care.

The number of characters available is increased by hardwiring together the outputs of different devices.

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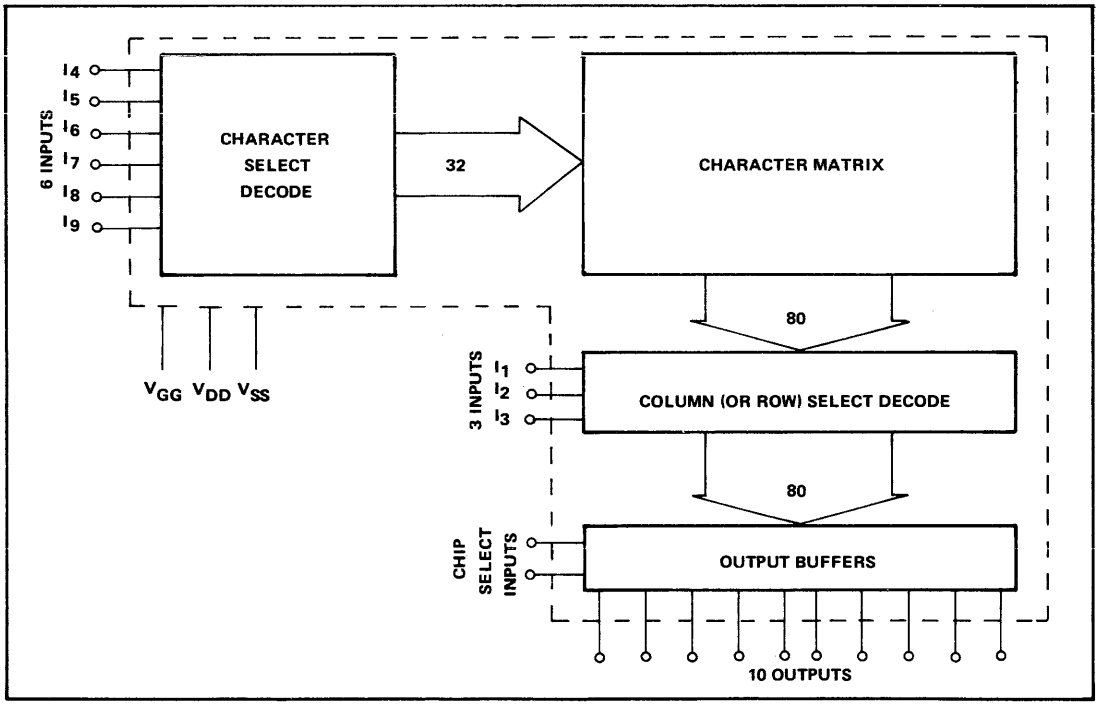
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	−25 V to 0.3 V
Supply voltage V_{GG} range (Note 1)	−25 V to 0.3 V
Clock input voltage range (Note 1)	−25 V to 0.3 V
Data input voltage range (Note 1)	−25 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

functional block diagram



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	+4.75	+5.00	5.25	V
Drain supply V_{DD}		0.00		V
Gate supply V_{GG}	−10	−12	−14	V
Logic Levels (See Note 1)				
Input level logic 0			1.0	V
Input level logic 1	3.5			V

NOTE 1: These input levels are given for V_{SS} = 5.0 V. If V_{SS} is other than 5.0 V the input levels must track V_{SS}.

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static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels (Notes 2 and 3)					
Output logic 0 level V_{OL}	Load is one series 74 TTL gate		0.4	0.8	V
Output logic 1 level V_{OH}		3.0	4.5		V
Output Current					
Output logic 0	Output voltage of 0.5	−2		−3	mA
Output logic 1, case 1	Output voltage of 3.0	+1		+1.3	mA
Output logic 1, case 2	Output voltage of 4.5	+0.3		+0.4	mA
Power Supply Current Drain					
Substrate supply I_{SS}	Under static conditions.	10	12	15	mA
Drain supply I_{DD}	All outputs at logic 0.	20	24	30	mA
Gate supply I_{GG}	Under static conditions.	10	12	15	mA
Power Dissipation	All outputs at logic 0.	180	220	270	mW

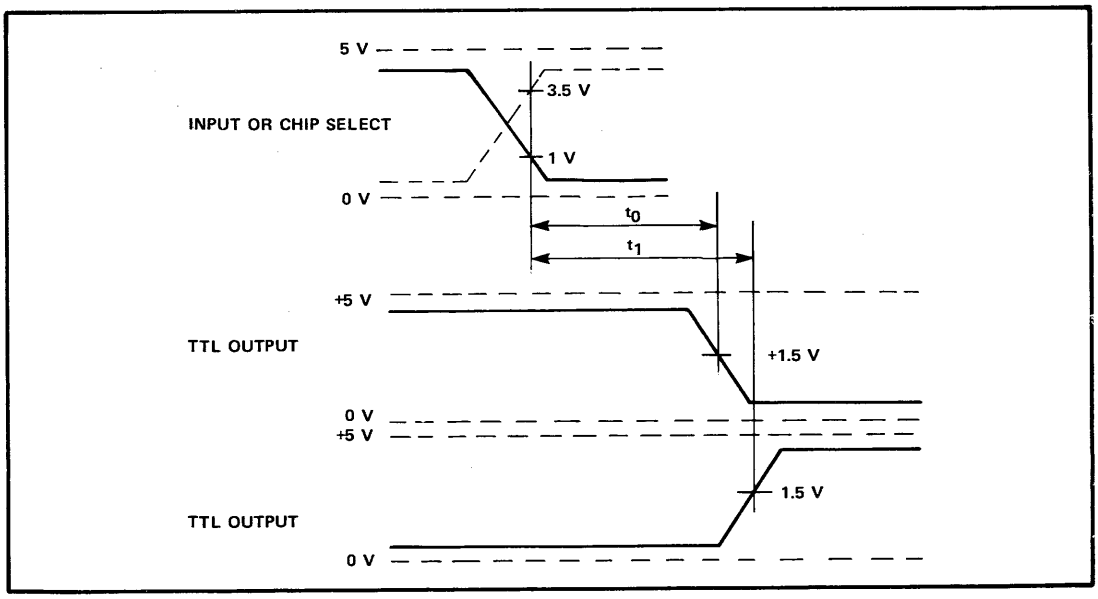
NOTES: 2. For V_{SS}, other than nominal output levels track V_{SS}.

3. For final test purposes, a worst-case TTL load is simulated by a load of 2.5 kΩ and a capacitance of 20 pF. All loads are connected between output and V_{SS}.

dynamic electrical characteristics (over −25°C to +70°C temperature range)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Access Time					
Output logic 0 level t_0	Load is one series 74 TTL gate	150	350	550	ns
Output logic 1 level t_1	C_L = 20 pF	150	350	550	ns
Input Capacitance C_{IN}	f = 100 kHz			5	pF

timing diagram and voltage waveforms



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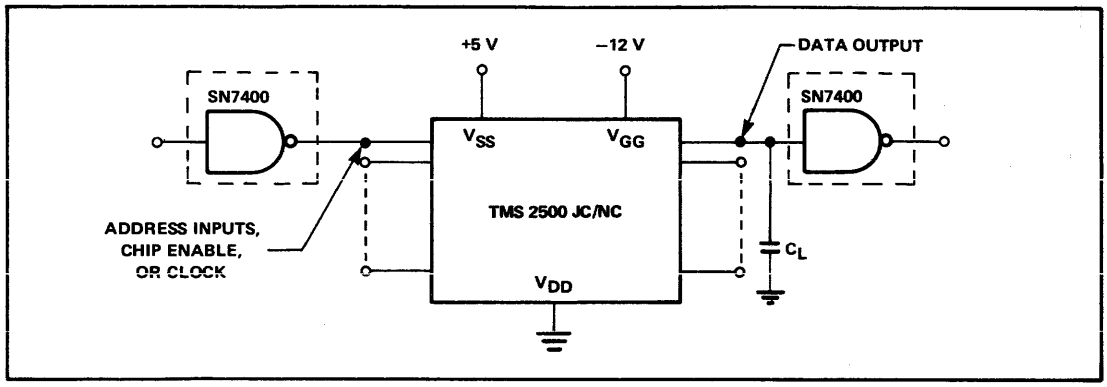
TTL interface and switching circuit

No components are needed for TTL interface.

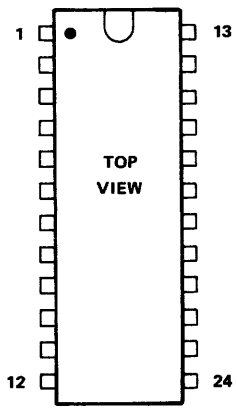


The load capacitance is used in the switching circuit to simulate parasitic capacitance loading in actual use.

mechanical data

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2500 JC) and a 24-pin plastic package (TMS 2500 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{GG}	13	CS1
2	O_1	14	CS2
3	O_2	15	I_9
4	O_3	16	I_8
5	O_4	17	I_7
6	O_5	18	I_6
7	O_6	19	I_5
8	O_7	20	I_4
9	O_8	21	I_3
10	O_9	22	I_2
11	O_{10}	23	I_1
12	V_{DD}	24	V_{SS}

For organization of 512 x 5, outputs are hardwired together as follows:

O_1 and O_2
O_3 and O_4
O_5 and O_6
O_7 and O_8
O_9 and O_{10}

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TMS 2600 JC, TMS 2600 NC
2048-BIT STATIC READ-ONLY MEMORY

JANUARY, 1971

features

- 2048-bit capacity
- Static operation
- Maximum access time under 1 microsecond
- Two organizations available
- Open-drain output buffers or double-ended buffers
- TTL compatible
- 24-pin dual-in-line package

description

The TMS 2600 JC/NC series is a family of static read-only memories,each with capacity of 2048 bits.

Programming the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

Inputs are available for enabling the chip and for selecting between a memory organization of 512 words of four bits or 256 words of eight bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground (substrate).

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

"TMS 2600 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 2600 NC" is used for a unit mounted in a 24-pin plastic package.

logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2600 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times. Access time is defined as the time between a change of data on any logic input or chip select line and a change of data on the output of a TTL gate. (See switching circuit).

operation (continued)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

organizational control logic

		OUTPUTS	
		B_1 B_3 B_5 B_7	B_2 B_4 B_6 B_8
256 words of 8 bits (MC = Logical 0):	A_9 = Logical 1	Enabled	Enabled
512 words of 4 bits (MC = Logical 1):	A_9 = Logical 0	Enabled	Logical 1
	A_9 = Logical 1	Logical 1	Enabled

To use the device as a 512 words of 4 bits, connect B_1 to B_2, B_3 to B_4, B_5 to B_6, B_7 to B_8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−16	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−16	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	650			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

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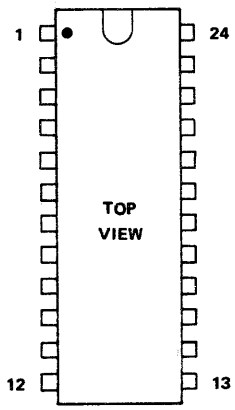
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Notes 1 and 3)	See switching circuit		600	1000	ns
t_{A2}	Access time (Notes 1 and 3)	See switching circuit		550	1000	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		180		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		15		mA
I_{GG}	Gate current			1.0		μA

NOTES: 1. Open drain buffer
2. Push-pull buffer
3. See Switching Diagram
4. Either open-drain or push-pull configuration

mechanical data and pin configuration

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 2600 JC) and a 24-pin plastic package (TMS 2600 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	13	A_9
2	A_2	14	CS
3	A_1	15	MC
4	B_1	16	V_{GG}
5	B_2	17	A_8
6	B_3	18	A_7
7	B_4	19	A_6
8	B_5	20	A_5
9	B_6	21	A_4
10	B_7	22	NC
11	B_8	23	NC
12	V_{SS}	24	V_{DD}

A – input
B – output
MC – mode control
CS – chip select

V_{DD} – drain power supply
V_{GG} – ground power supply
V_{SS} – substrate

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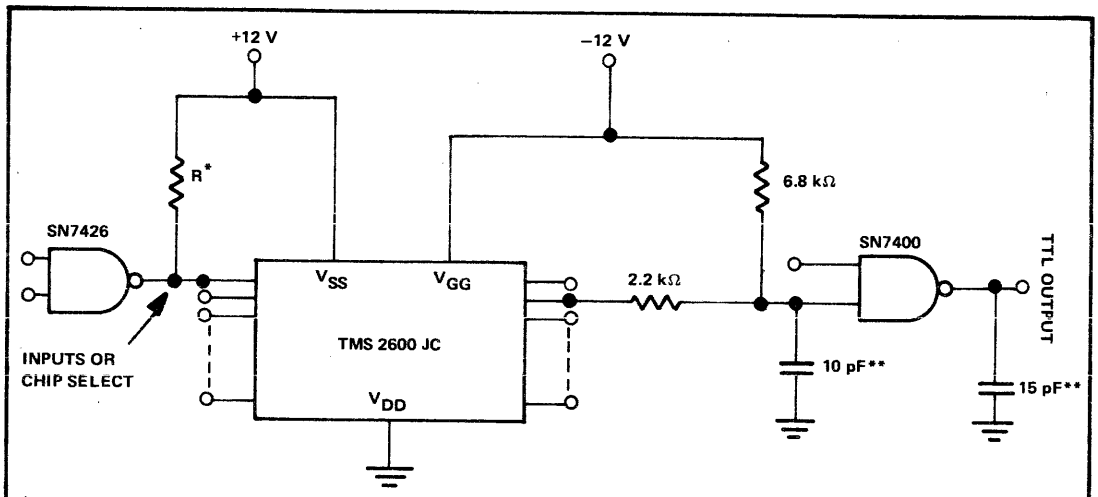
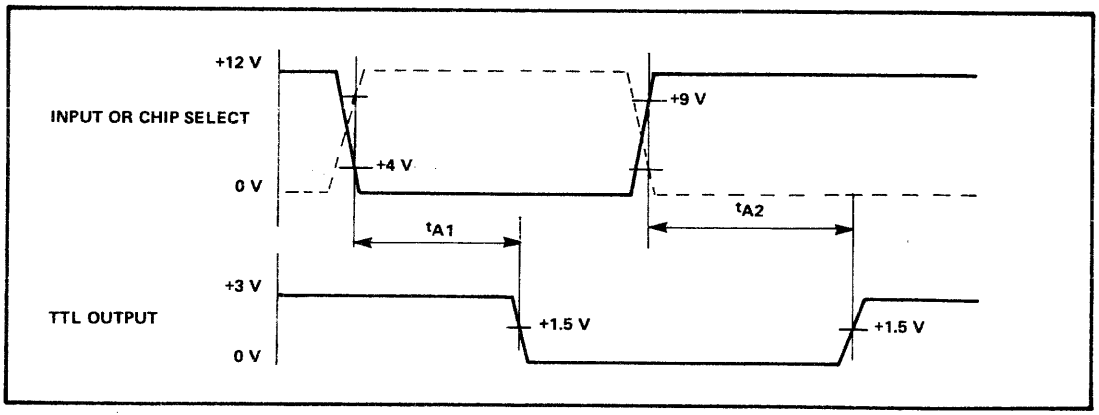
switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

switching diagram



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off the shelf devices

These devices have been programmed by TI and are available off the shelf:

1) TMS 2601 JC/NC

   This device has been programmed to demonstrate the capabilities of the TMS 2600 JC/NC series. It is used as a sample device. The buffers are single ended.

2) TMS 2602 JC/NC Code Converter

   This device converts the USASCII code into the selectric line code and vice versa.

3) TMS 2603 JC/NC Code Converter

   This device converts the full EBCDIC code into the USASCII code.

Truth tables for the TMS 2602 JC/NC and 2603 JC/NC are available upon request.

TRUTH TABLE, TMS 2601 JC/NC

INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1	INPUT ADDRESS	0_8	0_7	0_6	0_5	0_4	0_3	0_2	0_1
0	1	1	1	1	1	1	1	1	64	1	1	1	1	1	1	0	0	128	1	1	1	1	0	0	0	0	192	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	65	1	1	1	1	1	1	0	0	129	1	1	1	1	0	0	0	0	193	1	1	0	0	0	0	0	0
2	1	1	1	1	1	1	1	1	66	1	1	1	1	1	1	0	0	130	1	1	1	1	0	0	0	0	194	1	1	0	0	0	0	0	0
3	1	1	1	1	1	1	1	1	67	1	1	1	1	1	1	0	0	131	1	1	1	1	0	0	0	0	195	1	1	0	0	0	0	0	0
4	1	1	1	1	1	1	1	1	68	1	1	1	1	1	1	0	0	132	1	1	1	1	0	0	0	0	196	1	1	0	0	0	0	0	0
5	1	1	1	1	1	1	1	1	69	1	1	1	1	1	1	0	0	133	1	1	1	1	0	0	0	0	197	1	1	0	0	0	0	0	0
6	1	1	1	1	1	1	1	1	70	1	1	1	1	1	1	0	0	134	1	1	1	1	0	0	0	0	198	1	1	0	0	0	0	0	0
7	1	1	1	1	1	1	1	1	71	1	1	1	1	1	1	0	0	135	1	1	1	1	0	0	0	0	199	1	1	0	0	0	0	0	0
8	1	1	1	1	1	1	1	0	72	1	1	1	1	1	0	0	0	136	1	1	1	0	0	0	0	0	200	1	0	0	0	0	0	0	0
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14	1	1	1	1	1	1	1	1	78	1	1	1	1	1	1	0	0	142	1	1	1	1	0	0	0	0	206	1	1	0	0	0	0	0	0
15	1	1	1	1	1	1	1	1	79	1	1	1	1	1	1	0	0	143	1	1	1	1	0	0	0	0	207	1	1	0	0	0	0	0	0
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18	1	1	1	1	1	1	1	0	82	1	1	1	1	1	0	0	0	146	1	1	1	0	0	0	0	0	210	1	0	0	0	0	0	0	0
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20	1	1	1	1	1	1	1	1	84	1	1	1	1	1	1	0	0	148	1	1	1	1	0	0	0	0	212	1	1	0	0	0	0	0	0
21	1	1	1	1	1	1	1	1	85	1	1	1	1	1	1	0	0	149	1	1	1	1	0	0	0	0	213	1	1	0	0	0	0	0	0
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23	1	1	1	1	1	1	1	1	87	1	1	1	1	1	1	0	0	151	1	1	1	1	0	0	0	0	215	1	1	0	0	0	0	0	0
24	1	1	1	1	1	1	1	0	88	1	1	1	1	1	0	0	0	152	1	1	1	0	0	0	0	0	216	1	0	0	0	0	0	0	0
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28	1	1	1	1	1	1	1	0	92	1	1	1	1	1	0	0	0	156	1	1	1	0	0	0	0	0	220	1	0	0	0	0	0	0	0
29	1	1	1	1	1	1	1	0	93	1	1	1	1	1	0	0	0	157	1	1	1	0	0	0	0	0	221	1	0	0	0	0	0	0	0
30	1	1	1	1	1	1	1	1	94	1	1	1	1	1	1	0	0	158	1	1	1	1	0	0	0	0	222	1	1	0	0	0	0	0	0
31	1	1	1	1	1	1	1	1	95	1	1	1	1	1	1	0	0	159	1	1	1	1	0	0	0	0	223	1	1	0	0	0	0	0	0
32	1	1	1	1	1	1	1	0	96	1	1	1	1	1	0	0	0	160	1	1	1	0	0	0	0	0	224	1	0	0	0	0	0	0	0
33	1	1	1	1	1	1	1	0	97	1	1	1	1	1	0	0	0	161	1	1	1	0	0	0	0	0	225	1	0	0	0	0	0	0	0
34	1	1	1	1	1	1	1	0	98	1	1	1	1	1	0	0	0	162	1	1	1	0	0	0	0	0	226	1	0	0	0	0	0	0	0
35	1	1	1	1	1	1	1	0	99	1	1	1	1	1	0	0	0	163	1	1	1	0	0	0	0	0	227	1	0	0	0	0	0	0	0
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37	1	1	1	1	1	1	1	0	101	1	1	1	1	1	0	0	0	165	1	1	1	0	0	0	0	0	229	1	0	0	0	0	0	0	0
38	1	1	1	1	1	1	1	0	102	1	1	1	1	1	0	0	0	166	1	1	1	0	0	0	0	0	230	1	0	0	0	0	0	0	0
39	1	1	1	1	1	1	1	0	103	1	1	1	1	1	0	0	0	167	1	1	1	0	0	0	0	0	231	1	0	0	0	0	0	0	0
40	1	1	1	1	1	1	0	0	104	1	1	1	1	1	0	0	0	168	1	1	0	0	0	0	0	0	232	0	0	0	0	0	0	0	0
41	1	1	1	1	1	1	0	0	105	1	1	1	1	1	0	0	0	169	1	1	0	0	0	0	0	0	233	0	0	0	0	0	0	0	0
42	1	1	1	1	1	1	1	0	106	1	1	1	1	1	0	0	0	170	1	1	1	0	0	0	0	0	234	1	0	0	0	0	0	0	0
43	1	1	1	1	1	1	1	0	107	1	1	1	1	1	0	0	0	171	1	1	1	0	0	0	0	0	235	1	0	0	0	0	0	0	0
44	1	1	1	1	1	1	1	0	108	1	1	1	1	1	0	0	0	172	1	1	1	0	0	0	0	0	236	1	0	0	0	0	0	0	0
45	1	1	1	1	1	1	1	0	109	1	1	1	1	1	0	0	0	173	1	1	1	0	0	0	0	0	237	1	0	0	0	0	0	0	0
46	1	1	1	1	1	1	1	0	110	1	1	1	1	1	0	0	0	174	1	1	1	0	0	0	0	0	238	1	0	0	0	0	0	0	0
47	1	1	1	1	1	1	1	0	111	1	1	1	1	1	0	0	0	175	1	1	1	0	0	0	0	0	239	1	0	0	0	0	0	0	0
48	1	1	1	1	1	1	0	0	112	1	1	1	1	1	0	0	0	176	1	1	0	0	0	0	0	0	240	0	0	0	0	0	0	0	0
49	1	1	1	1	1	1	0	0	113	1	1	1	1	1	0	0	0	177	1	1	0	0	0	0	0	0	241	0	0	0	0	0	0	0	0
50	1	1	1	1	1	1	0	0	114	1	1	1	1	1	0	0	0	178	1	1	0	0	0	0	0	0	242	0	0	0	0	0	0	0	0
51	1	1	1	1	1	1	0	0	115	1	1	1	1	1	0	0	0	179	1	1	0	0	0	0	0	0	243	0	0	0	0	0	0	0	0
52	1	1	1	1	1	1	1	0	116	1	1	1	1	1	0	0	0	180	1	1	1	0	0	0	0	0	244	1	0	0	0	0	0	0	0
53	1	1	1	1	1	1	1	0	117	1	1	1	1	1	0	0	0	181	1	1	1	0	0	0	0	0	245	1	0	0	0	0	0	0	0
54	1	1	1	1	1	1	1	0	118	1	1	1	1	1	0	0	0	182	1	1	1	0	0	0	0	0	246	1	0	0	0	0	0	0	0
55	1	1	1	1	1	1	1	0	119	1	1	1	1	1	0	0	0	183	1	1	1	0	0	0	0	0	247	1	0	0	0	0	0	0	0
56	1	1	1	1	1	1	0	0	120	1	1	1	1	1	0	0	0	184	1	1	0	0	0	0	0	0	248	0	0	0	0	0	0	0	0
57	1	1	1	1	1	1	0	0	121	1	1	1	1	1	0	0	0	185	1	1	0	0	0	0	0	0	249	0	0	0	0	0	0	0	0
58	1	1	1	1	1	1	0	0	122	1	1	1	1	1	0	0	0	186	1	1	0	0	0	0	0	0	250	0	0	0	0	0	0	0	0
59	1	1	1	1	1	1	0	0	123	1	1	1	1	1	0	0	0	187	1	1	0	0	0	0	0	0	251	0	0	0	0	0	0	0	0
60	1	1	1	1	1	1	0	0	124	1	1	1	1	1	0	0	0	188	1	1	0	0	0	0	0	0	252	0	0	0	0	0	0	0	0
61	1	1	1	1	1	1	0	0	125	1	1	1	1	1	0	0	0	189	1	1	0	0	0	0	0	0	253	0	0	0	0	0	0	0	0
62	1	1	1	1	1	1	1	0	126	1	1	1	1	1	0	0	0	190	1	1	1	0	0	0	0	0	254	1	0	0	0	0	0	0	0
63	1	1	1	1	1	1	1	0	127	1	1	1	1	1	0	0	0	191	1	1	1	0	0	0	0	0	255	1	0	0	0	0	0	0	0

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SOFTWARE PACKAGE

input format

Programming information for the TMS 2600 JC/NC should be transmitted to TI in the form of a DECK of 43 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI should be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the various circuit options desired will be transmitted on a special form supplied by TI.

The main memory array can be so programmed that for any binary input of A_8 through A_1 (0 to 255), the outputs B_8 through B_1 are uniquely determined. Since A_9 and MC are used to select output paths, the internal storage of data in the array is the same regardless of organization – 256 x 8 or 512 x 4.

Each card in the data deck describes the outputs for six or twelve input addresses, depending on whether eight or four outputs are desired. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

data card format

Column	
1-2	Punch the sequential card number (01 through 43)
3	Blank
4-5	Punch a "26" to signify TMS 2600 JC
6-11	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers)
12	Blank (a space for the revision letter if necessary)
13	Punch a "8" if using the 256 x 8 configuration, or punch a "4" if using the 512 x 4 configuration
14	Punch a "D" for open-drain type output buffers, or punch a "P" for push-pull type output buffers
15-17	Punch a right-justified integer representing the binary input address (0-255 if 8 outputs, 0-511 if only 4 outputs) for the first set of outputs described on the card
18	Punch a "–" (minus sign)
19-21	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card
22	Blank
23-80	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0

For a 256 x 8 configuration each card will describe 6 output sets. The 43rd card will contain only 4 output sets.

23-30	Punch the outputs desired for B_8, B_7, B_6, B_5, B_4, B_3, B_2, and B_1, in that order, for the first address specified on the card
33-40	Punch the outputs desired for the second address
43-50	Punch the outputs desired for the third address

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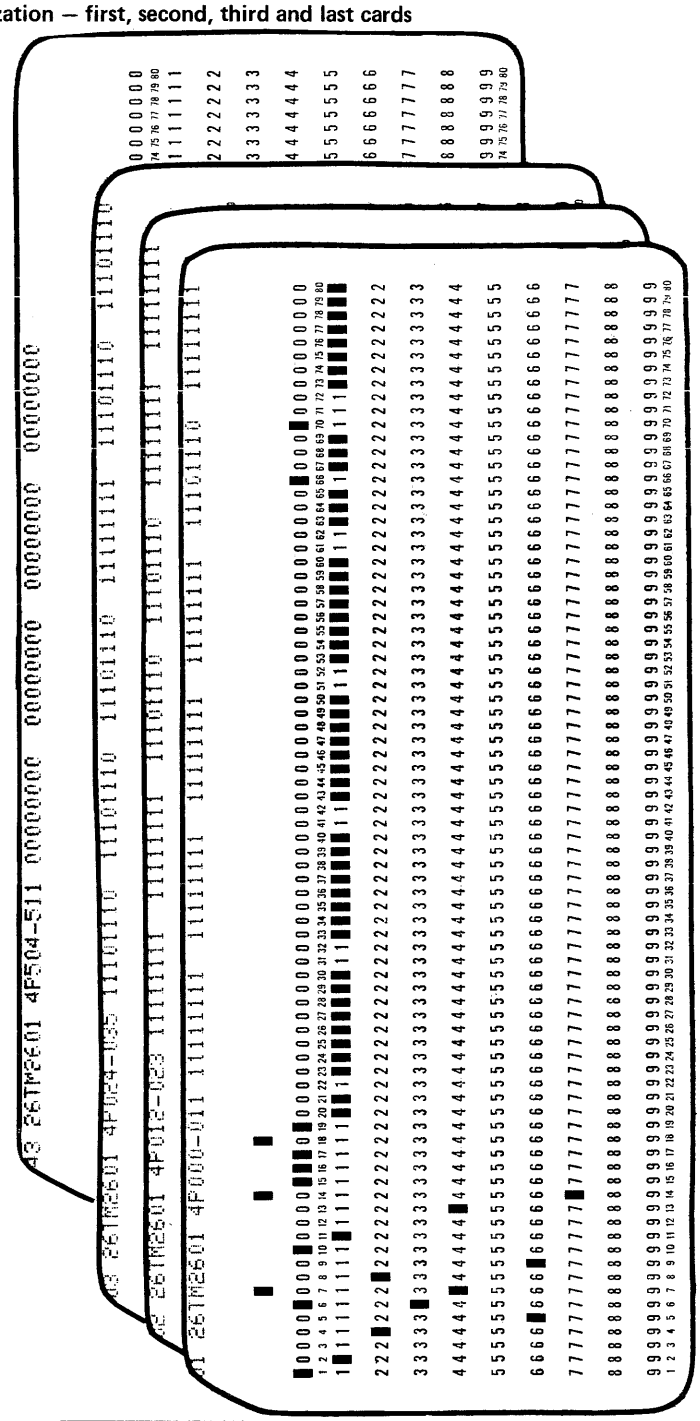
data card format (continued)

Column	
53-60	Punch the outputs desired for the fourth address
63-70	Punch the outputs desired for the fifth address
73-80	Punch the outputs desired for the sixth address

For a 512 x 4 configuration, each card will describe 12 output sets. The 43rd card will contain only 8 output sets.

23-26	Punch the outputs desired for B_8 or B_7, B_6 or B_5, B_4 or B_3, B_2 or B_1, in that order, for the first address specified on the card.
27-30	Punch the outputs desired for the second address
33-36	Punch the outputs desired for the third address
37-40	Punch the outputs desired for the fourth address
43-46	Punch the outputs desired for the fifth address
47-50	Punch the outputs desired for the sixth address
53-56	Punch the outputs desired for the seventh address
57-60	Punch the outputs desired for the eighth address
63-66	Punch the outputs desired for the ninth address
67-70	Punch the outputs desired for the tenth address
73-76	Punch the outputs desired for the eleventh address
77-80	Punch the outputs desired for the twelfth address

512 x 4 organization — first, second, third and last cards



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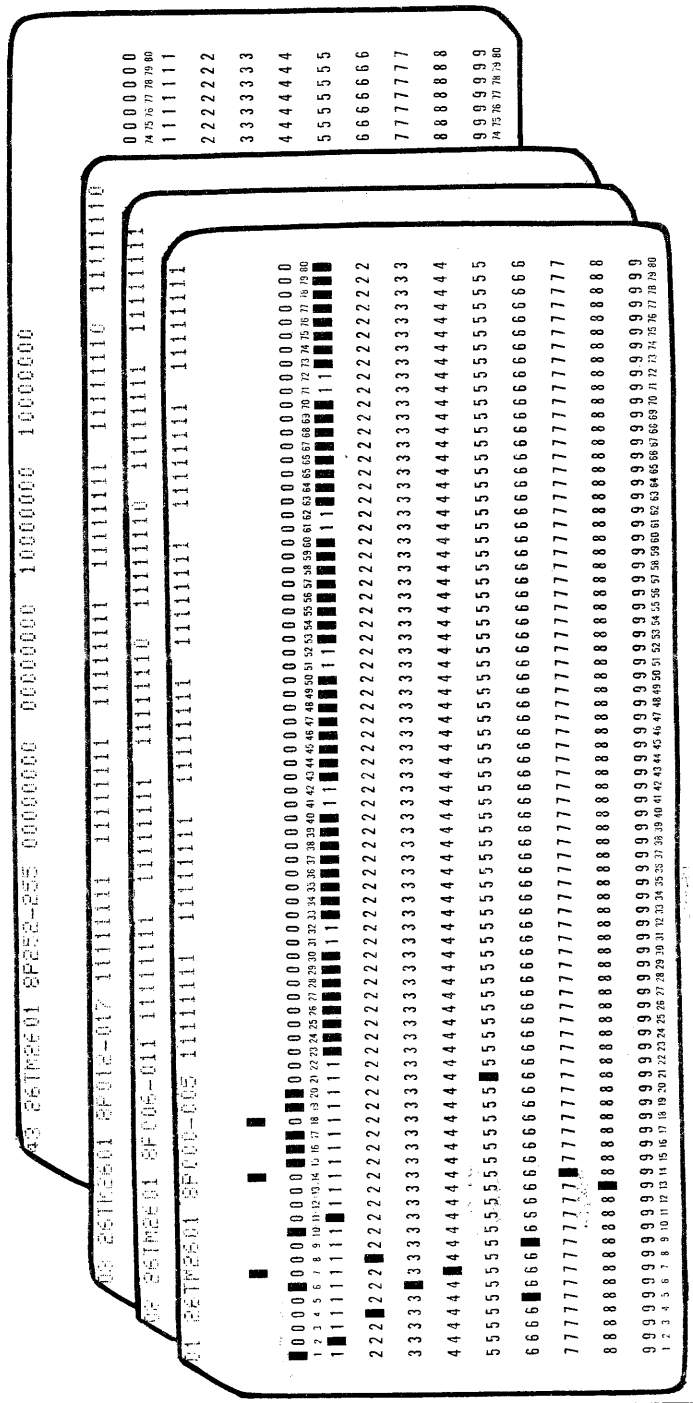
256 x 8 organization – first, second, third and last cards



TMS 2602 JC, TMS 2602 NC
USASCII-TO-SELECTRIC/SELECTRIC-TO-USASCII CODE CONVERTER

description

The TMS 2602 JC/NC is programmed TMS 2600 JC/NC ROM capable of converting both USASCII to Selectric Line Code, and Selectric Line Code to USASCII. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_7, and Outputs O_2 through O_8 of the ROM correspond to the two codes as follows:

ROM INPUT	SELECTRIC BIT	USASCII BIT	ROM OUTPUT
I_1	1	b_1	O_2
I_2	2	b_2	O_3
I_3	4	b_3	O_4
I_4	8	b_4	O_5
I_5	A	b_5	O_6
I_6	B	b_6	O_7
I_7	S	b_7	O_8

mode selection

Output O_1 is even parity for the 7-bit output word.

Input I_8 at logic 0 — USASCII is converted to Selectric Line Code

Input I_8 at logic 1 — Selectric Line Code is converted to USASCII

logic definition

As with the TMS 2600 JC/NC, negative logic is assumed.

Logical 1 = most negative voltage

Logical 0 = most positive voltage

code definition

The standard USASCII table is used as the USASCII code. The selectric code used is the IBM Correspondence Selectric Line Code. The following tables show the mapping from USASCII to Selectric and vice versa.

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SELECTRIC TO USASCII (I_8 = logic 1)

SELECTRIC / USASCII

S→ B→ A→	000	001	010	011	100	101	110	111
8 4 2 1 ↓ / COL→ ROW↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE1 / SPACE	t / t	¢ / !	j / j	SPACE2 / SPACE	T / T	o / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /]	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	' / /	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / >	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,
1 0 0 0	8	4 / 4	l / l	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	O / O	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / RS	② / VT	③ / RS	Z / Z	④ / RS	⑤ / FF	⑥ / RS
1 0 1 1	11	9 / 9	b / b	w / w	— / —	(/ (	B / B	W / W	— / —
1 1 0 0	12	PN1 / DC2	BY1 / SUB	RES1 / EM	PF1 / DC4	PN2 / DC2	BY2 / FS	RES2 / GS	PF2 / DC4
1 1 0 1	13	RS1 / DC3	LF1 / LF	NL1 / CR	HTI / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / SO	EOB1 / ETX	BS1 / BS	LC1 / BEL	UC2 / ENQ	EOB2 / ETB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / ESC	IL1 / NUL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

TMS 2602 JC, TMS 2602 NC
USASCII-TO-SELECTRIC/SELECTRIC-TO-USASCII CODE CONVERTER

USASCII TO SELECTRIC (I_8 = logic 0)

USASCII / SELECTRIC

b7 → b6 → b5 →				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	COL / ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL / IL1	DLE / PRE2	SPACE / SPACE1	0 / 0	@ / @	P / P	\ / '	p / p
0	0	0	1	1	SOH / b	DC1 / RS2	! / !	1 / 1	A / A	Q / Q	a / a	q / q
0	0	1	0	2	STX / 9	DC2 / PN1	" / "	2 / 2	B / B	R / R	b / b	r / r
0	0	1	1	3	ETX / EOB1	DC3 / RS1	# / #	3 / 3	C / C	S / S	c / c	s / s
0	1	0	0	4	EOT / EOT1	DC4 / PF1	$ / $	4 / 4	D / D	T / T	d / d	t / t
0	1	0	1	5	ENQ / UC2	NAK / !	% / %	5 / 5	E / E	U / U	e / e	u / u
0	1	1	0	6	ACK / –	SYN / IL2	& / &	6 / 6	F / F	V / V	f / f	v / v
0	1	1	1	7	BEL / LC1	ETB / EOB2	/ / '	7 / 7	G / G	W / W	g / g	w / w
1	0	0	0	8	BS / BS1	CAN / !	(/ (	8 / 8	H / H	X / X	h / h	x / x
1	0	0	1	9	HT / HT1	EM / RES1	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1	0	1	0	10	LF / LF1	SUB / BY1	* / *	: / :	¢ / J	Z / Z	j / j	z / z
1	0	1	1	11	VT / ②	ESC / PRE1	+ / +	; / ;	K / K	[/ ±	k / k	[/ ±
1	1	0	0	12	FF / ⑤	FS / BY2	, / ,	< / °	L / L	\ / ±	l / l	; / ±
1	1	0	1	13	CR / HL1	GS / RES2	– / –	= / =	M / M	] / ±	m / m	] / ±
1	1	1	0	14	SO / UC1	RS / RES2	. / .	> / ¢	N / N	⁀ / ±	n / n	~ / ±
1	1	1	1	15	SI / LC2	US / BY2	/ / /	? / ?	O / O	— / —	o / o	DEL / DEL1

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TMS 2603 JC, TMS 2603 NC
EBCDIC-TO-USASCII CODE CONVERTER

JANUARY, 1971

description

The TMS 2603 JC/NC is a programmed TMS 2600 JC/NC ROM capable of converting 8-bit EBCDIC to standard USASCII. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_8 and outputs O_2 through O_8 of the ROM correspond to the codes as follows:

ROM OUTPUT	EBCDIC BIT	USASCII BIT	ROM OUTPUT*
I_1	B_7 (LSB)	b_2	O_2
I_2	B_6	b_3	O_3
I_3	B_5	b_4	O_4
I_4	B_4	b_5	O_5
I_5	B_3	b_6	O_6
I_6	B_2	b_7	O_7
I_7	B_1	b_8	O_8
I_8	B_0 (MSB)		

* Output O_1 is even parity for the 7-bit USASCII output word.

logic definition

As with the TMS 2600 JC/NC negative logic is assumed.

Logic 1 = most negative voltage

Logic 0 = most positive voltage

code definition

Standard EBCDIC and USASCII codes are used for the conversion. The following table shows the mapping from EBCDIC to USASCII.

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EBCDIC TO USASCII

EBCDIC / USASCII

0 → 1 → 2 → 3 →					0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1
4 ↓	5 ↓	6 ↓	7 ↓	COL → / ROW ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL / NUL	DLE / DLE	DS / NUL		SP / SP	& / &		
0	0	0	1	1	SOH / SOH	DC1 / DC1	SOS / NUL				/ /	
0	0	1	0	2	STX / STX	DC2 / DC2	FS / NUL	SYN / SYN				
0	0	1	1	3	ETX / ETX	DC3 / DC3						
0	1	0	0	4	PF / NUL	RES / NUL	BYP / NUL	PN / NUL				
0	1	0	1	5	HT / HT	NL / NUL	LF / LF	RS / NUL				
0	1	1	0	6	LC / NUL	BS / BS	EOB / ETB	UC / NUL				
0	1	1	1	7	DEL / DEL	IL / NUL	PRE / ESC	EOT / EOT				
1	0	0	0	8		CAN / CAN						
1	0	0	1	9		EM / EM						
1	0	1	0	10	SMM / NUL	CC / NUL	SM / NUL		¢ / NUL	! / !		: / :
1	0	1	1	11	VT / VT				. / .	$ / $	, / ,	# / #
1	1	0	0	12	FF / FF	IFS / FS		DC4 / DC4	< / <	* / *	% / %	@ / @
1	1	0	1	13	CR / CR	IGS / GS	ENQ / ENQ	NAK / NAK	(/ (	) /)	— / —	' / /
1	1	1	0	14	SO / SO	IRS / RS	ACK / ACK		+ / +	; / ;	> / >	= / =
1	1	1	1	15	SI / SI	IUS / US	BEL / BEL	SUB / SUB	| / :	¬ / NUL	? / ?	" / "

— Continued

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EBCDIC TO USASCII (Continued)

EBCDIC / USASCII

0 1 2 3 →	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
4 5 6 7 ↓ / ROW ↓ COL →	0	1	2	3	4	5	6	7
0 0 0 0	0							0 / 0
0 0 0 1	1	a / a	j / j			A / A	J / J		1 / 1
0 0 1 0	2	b / b	k / k	s / s		B / B	K / K	S / S	2 / 2
0 0 1 1	3	c / c	l / l	t / t		C / C	L / L	T / T	3 / 3
0 1 0 0	4	d / d	m / m	u / u		D / D	M / M	U / U	4 / 4
0 1 0 1	5	e / e	n / n	v / v		E / E	N / N	V / V	5 / 5
0 1 1 0	6	f / f	o / o	w / w		F / F	O / O	W / W	6 / 6
0 1 1 1	7	g / g	p / p	x / x		G / G	P / P	X / X	7 / 7
1 0 0 0	8	h / h	q / q	y / y		H / H	Q / Q	Y / Y	8 / 8
1 0 0 1	9	i / i	r / r	z / z		I / I	R / R	Z / Z	9 / 9
1 0 1 0	10								
1 0 1 1	11								
1 1 0 0	12								
1 1 0 1	13								
1 1 1 0	14								
1 1 1 1	15								

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TMS 2604 JC, TMS 2604 NC
USASCII-TO-EBCDIC/SELECTRIC-TO-EBCDIC CODE CONVERTER

description

The TMS 2604 JC/NC is a programmed TMS 2600 JC/NC ROM capable of converting both USASCII and Selectric Line Code to EBCDIC. **Electrical and mechanical characteristics, interfacing, and timing are identical to those of the TMS 2600 JC/NC.**

Inputs I_1 through I_7 and Outputs O_1 through O_8 of the ROM correspond to the 3 codes as follows:

ROM OUTPUT	USASCII BIT	SELECTRIC BIT	EBCDIC BIT	ROM OUTPUT
I_1	b_1	1	B_7	O_1
I_2	b_2	2	B_6	O_2
I_3	b_3	4	B_5	O_3
I_4	b_4	8	B_4	O_4
I_5	b_5	A	B_3	O_5
I_6	b_6	B	B_2	O_6
I_7	b_7	S	B_1	O_7
			B_0	O_8

mode selection

Input I_8 at logical 0 – USASCII is converted to EBCDIC.

Input I_8 at logical 1 – Selectric is converted to EBCDIC.

logic definition

As with the TMS 2600 JC/NC, negative logic is assumed.

Logic 1 = most negative voltage

Logic 0 = most positive voltage

code definition

Standard USASCII and EBCDIC are used along with IBM correspondence Selectric Line Code to produce the following conversion table:

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USASCII TO EBCDIC
($I_8 = 0$)

USASCII / EBCDIC

b_7 b_6 b_5 →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1 ↓ COL → / ROW ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL / NUL	DLE / DLE	SP / SP	0 / 0	@ / @	P / P	↑ / ↑	p / p
0 0 0 1	1	SOH / SOH	DC1 / DC1	! / SP	1 / 1	A / A	Q / Q	a / a	q / q
0 0 1 0	2	STX / STX	DC2 / DC2	" / "	2 / 2	B / B	R / R	b / b	r / r
0 0 1 1	3	ETX / ETX	DC3 / DC3	# / #	3 / 3	C / C	S / S	c / c	s / s
0 1 0 0	4	EOT / EOT	DC4 / DC4	$ / $	4 / 4	D / D	T / T	d / d	t / t
0 1 0 1	5	ENQ / ENQ	NAK / NAK	% / %	5 / 5	E / E	U / U	e / e	u / u
0 1 1 0	6	ACK / ACK	SYN / SYN	& / &	6 / 6	F / F	V / V	f / f	v / v
0 1 1 1	7	BEL / BEL	ETB / EOB	' / '	7 / 7	G / G	W / W	g / g	w / w
1 0 0 0	8	BS / BS	CAN / CAN	(/ (	8 / 8	H / H	X / X	h / h	x / x
1 0 0 1	9	HT / HT	EM / EM	) /)	9 / 9	I / I	Y / Y	i / i	y / y
1 0 1 0	10	LF / LF	SUB / SUB	* / *	: / :	J / J	Z / Z	j / j	z / z
1 0 1 1	11	VT / VT	ESC / PRE	+ / +	; / ;	K / K	[/ (	k / k	[/ (
1 1 0 0	12	FF / FF	FS / IFS	, / ,	< / <	L / L	\ / /	l / l	; / ;
1 1 0 1	13	CR / CR	GS / IGS	– / –	= / =	M / M	] /)	m / m	] /)
1 1 1 0	14	SO / SO	RS / IRS	. / .	> / >	N / N	^ / ¬	n / n	~ / ¢
1 1 1 1	15	SI / SI	US / IUS	/ / /	? / ?	O / O	— / —	o / o	DEL / DEL

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SELECTRIC TO EBCDIC
(i8 = 1)

S → B → A →		0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
8 4 2 1 ↓	COL → / ROW ↓	0	1	2	3	4	5	6	7
0 0 0 0	0	SPACE 1 / SPACE	t / t	¢ / !	j / j	SPACE 2 / SPACE	T / T	? / <	J / J
0 0 0 1	1	1 / 1	x / x	m / m	g / g	± /)	X / X	M / M	G / G
0 0 1 0	2	2 / 2	n / n	. / .	= / =	@ / @	N / N	. / .	+ / +
0 0 1 1	3	3 / 3	u / u	v / v	f / f	# / #	U / U	V / V	F / F
0 1 0 0	4	5 / 5	e / e	' / '	p / p	% / %	E / E	" / "	P / P
0 1 0 1	5	7 / 7	d / d	r / r	; / ;	& / &	D / D	R / R	: / :
0 1 1 0	6	6 / 6	k / k	i / i	q / q	¢ / ¢	K / K	I / I	Q / Q
0 1 1 1	7	8 / 8	c / c	a / a	, / ,	* / *	C / C	A / A	, / ,
1 0 0 0	8	4 / 4	l / l	o / o	/ / /	$ / $	L / L	O / O	? / ?
1 0 0 1	9	O / O	h / h	s / s	y / y	) /)	H / H	S / S	Y / Y
1 0 1 0	10	z / z	① / IRS	② / VT	③ / RS	Z / Z	④ / IRS	⑤ / FF	⑥ / IRS
1 0 1 1	11	9 / 9	b / b	w / w	– / –	(/ (	B / B	W / W	— / —
1 1 0 0	12	PN1 / PN	BY1 / SUB	RES1 / RES	PF1 / PF	PN2 / DC2	BY2 / IFS	RES2 / IGS	PF2 / DC4
1 1 0 1	13	RS1 / IRS	LF1 / LF	NL1 / NL	HTI / HT	RS2 / DC1	LF2 / LF	NL2 / CR	HT2 / HT
1 1 1 0	14	UC1 / UC	EOB1 / EOB	BS1 / BS	LC1 / LC	UC2 / ENQ	EOB2 / EOB	BS2 / BS	LC2 / SI
1 1 1 1	15	EOT1 / EOT	PRE1 / PRE	IL1 / IL	DEL1 / DEL	EOT2 / EOT	PRE2 / DLE	IL2 / NUL	DEL2 / NUL

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TMS 2605 JC, TMS 2605 NC
USASII, BAUDOT, SELECTRIC, EBCDIC CODE GENERATOR

FEBRUARY 1971

features

- 2048-bit capacity
- Static operation
- Maximum access time of 900 nsec
- Open-drain output buffers or double-ended buffers
- TTL compatible

description

The TMS 2605 JC/NC is a multiple-code generator designed to exercise and test keyboards, data communication links, and typing mechanisms, by generating the "Quick Brown Fox" message.

Six inputs of the TMS 2605 JC/NC are fed from a 6-bit binary count. The seventh and eighth inputs are used as code selects. The message can be generated in the four codes listed below:

I_7	I_8	CODE GENERATED
0	0	Selectric (7 bits plus parity)
1	0	EBCDIC (8 bits)
0	1	Baudot (5 bits)
1	1	ASCII (7 bits plus parity)

For normal operation of this device, Chip Enable (pin 14) must be at logic 1, I_9 (pin 13) at logic 1, and Mode Control (pin 15) at logic 0.

The outputs of the ROM correspond as follows:

ROM OUTPUT	SELECTRIC	EBCDIC	BAUDOT	ASCII
O_1	1	B_7	1	B_1
O_2	2	B_6	2	B_2
O_3	4	B_5	3	B_3
O_4	8	B_4	4	B_4
O_5	A	B_3	5	B_5
O_6	B	B_2	—	B_6
O_7	S	B_1	—	B_7
O_8	Parity	B_0	—	Parity

In typical applications the TMS 2605 JC/NC will be connected to a 6-bit binary counter. As the counter counts from 0 to 63, the following message will be generated in the selectric code.

THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG 1234567890 DE

electrical characteristics

All electrical and mechanical characteristics of this device are identical to those of the TMS 2600 JC/NC. "TMS 2605 JC" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package. Mounted in a 24-pin plastic package the device is numbered "TMS 2605 NC." (See MOS/LSI packaging section.)

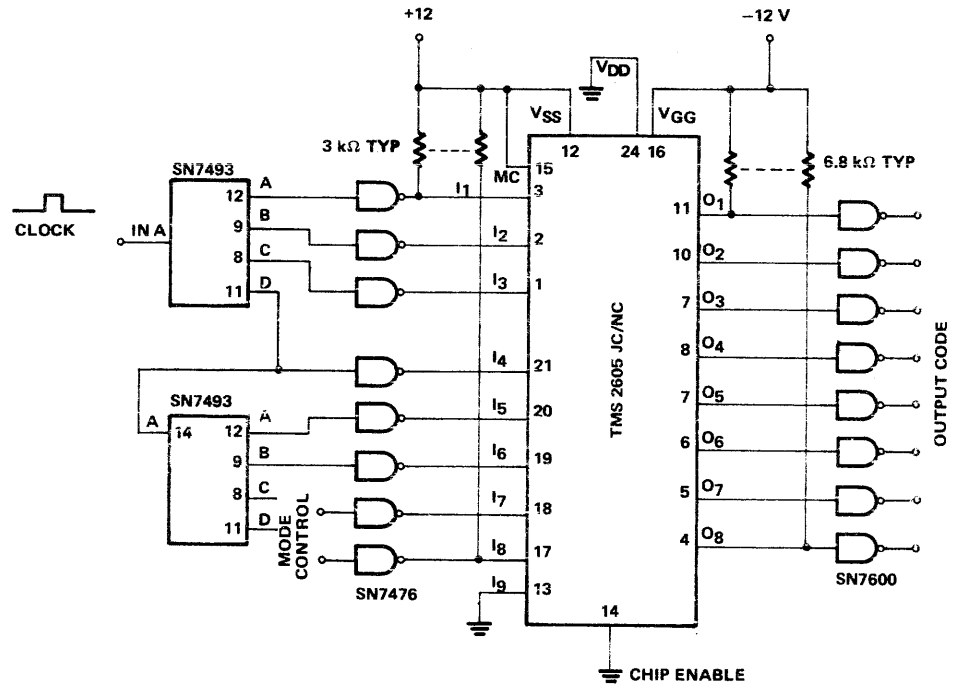
logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

interface and typical applications data



NOTE: A BINARY COUNTER FURNISHES THE INPUTS FOR THE ROM. THE SELECTED CODE WORD APPEARS IN INVERTED FORM (NEGATIVE MOS LOGIC) AT THE OUTPUT OF THE ROM, AND IN INVERTED FORM (POSITIVE TTL LOGIC) AT THE OUTPUT OF THE TTL GATES.

truth table

The truth table of the TMS 2605 JC/NC is given for the 4 selected codes:

ADDRESS	CODE	I_7	I_8
0 – 63	Selectric	0	0
64 – 127	EBCDIC	1	0
128 – 191	Baudot	0	1
192 – 255	USASCII	1	1

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truth table (continued)

		O_8 PARITY	O_7	O_6	O_5	O_4	O_3	O_2	O_1
		SELECTRIC							
		Y	S	B	A	8	4	2	1
0	IL1	0	1	0	1	0	0	0	0
1	NL	1	1	0	1	0	0	1	0
2	IL1	0	1	0	1	0	0	0	0
3	IL1	0	1	0	1	0	0	0	0
4	T	1	0	1	0	1	1	1	1
5	H	1	0	1	0	0	1	1	0
6	E	0	0	1	0	1	0	1	1
7	SP	1	1	1	1	1	1	1	1
8	Q	0	0	0	0	1	0	0	1
9	U	1	0	1	0	1	1	0	0
10	I	1	0	0	1	1	0	0	1
11	C	0	0	1	0	1	0	0	0
12	K	1	0	1	0	1	0	0	1
13	SP	1	1	1	1	1	1	1	1
14	B	0	0	1	0	0	1	0	0
15	R	1	0	0	1	1	0	1	0
16	O	0	0	0	1	0	1	1	1
17	W	0	0	0	1	0	1	0	0
18	N	0	0	1	0	1	1	0	1
19	SP	1	1	1	1	1	1	1	1
20	F	0	0	0	0	1	1	0	0
21	O	0	0	0	1	0	1	1	1
22	X	0	0	1	0	1	1	1	0
23	SP	1	1	1	1	1	1	1	1
24	J	0	0	0	0	1	1	1	1
25	U	1	0	1	0	1	1	0	0
26	M	0	0	0	0	1	1	1	0
27	P	1	0	0	0	0	1	0	1
28	S	1	0	0	1	0	1	1	0
29	SP	1	1	1	1	1	1	1	1
30	O	0	0	0	1	0	1	1	1
31	V	1	0	0	1	1	1	0	0
32	E	0	0	0	1	0	1	0	1
33	R	1	0	0	1	1	0	1	0
34	SP	1	1	1	1	1	1	1	1
35	T	1	0	1	0	1	1	1	1
36	H	1	0	1	0	0	1	1	0
37	E	0	0	1	0	1	0	1	1
38	SP	1	1	1	1	1	1	1	1
39	L	0	0	1	0	0	1	1	1
40	A	0	0	0	1	1	0	0	0
41	Z	0	0	1	1	0	1	0	1
42	Y	0	0	0	0	0	1	1	0
43	SP	1	1	1	1	1	1	1	1
44	D	1	0	1	0	1	0	1	0
45	O	0	0	0	1	0	1	1	1
46	G	1	0	0	0	1	1	1	0
47	SP	1	1	1	1	1	1	1	1
48	1	0	1	1	1	1	1	1	0
49	2	0	1	1	1	1	1	0	1
50	3	1	1	1	1	1	1	0	0
51	4	0	1	1	1	0	1	1	1
52	5	0	1	1	1	1	0	1	1
53	6	1	1	1	1	1	0	0	1
54	7	1	1	1	1	1	0	1	0
55	8	0	1	1	1	1	0	0	0
56	9	0	1	1	1	0	1	0	0
57	0	1	1	1	1	0	1	1	0
58	SP	1	1	1	1	1	1	1	1
59	D	1	0	1	0	1	0	1	0
60	E	0	0	1	0	1	0	1	1
61	SP	1	1	1	1	1	1	1	1
62	DEL	1	1	0	0	0	0	0	0
63	DEL	1	1	0	0	0	0	0	0

		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
		EBCDIC							
		B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
NULL	64	1	1	1	1	1	1	1	1
CR	65	1	1	1	1	0	0	1	0
CA	66	1	1	1	1	0	0	0	1
LF	67	1	1	0	1	1	0	1	0
T	68	0	0	0	1	1	1	0	0
H	69	0	0	1	1	0	1	1	1
E	70	0	0	1	1	1	1	0	1
SP	71	1	0	1	1	1	1	1	1
Q	72	0	0	0	1	0	1	1	1
U	73	0	0	0	1	1	1	0	1
I	74	0	0	1	1	0	1	1	0
C	75	0	0	1	1	1	1	0	0
K	76	0	0	1	0	1	1	0	1
SP	77	1	0	1	1	1	1	1	1
B	78	0	0	1	1	1	1	0	1
R	79	0	0	1	1	0	1	1	0
O	80	0	0	1	1	0	1	1	1
W	81	0	0	0	1	0	1	0	1
N	82	0	0	1	0	1	1	0	1
SP	83	1	0	1	1	1	1	1	1
F	84	0	0	1	1	1	0	0	1
O	85	0	0	1	1	0	1	1	1
X	86	0	0	1	0	1	1	0	0
SP	87	1	0	1	1	1	1	1	1
J	88	0	0	1	0	1	1	1	0
U	89	0	0	1	1	1	0	1	1
M	90	0	0	1	0	1	0	1	1
P	91	0	0	1	0	1	0	0	0
S	92	0	0	1	0	1	1	0	1
SP	93	1	0	1	1	1	1	1	1
O	94	0	0	1	0	1	1	1	1
V	95	0	0	1	1	1	0	1	0
E	96	0	0	1	1	1	0	1	1
R	97	0	0	1	1	0	1	1	0
SP	98	1	0	1	1	1	1	1	1
T	99	0	0	0	1	1	1	0	0
H	100	0	0	1	1	0	1	1	0
E	101	0	0	1	1	1	0	1	0
SP	102	1	0	1	1	1	1	1	1
L	103	0	0	1	1	0	1	1	0
A	104	0	0	1	1	1	1	1	0
Z	105	0	0	1	1	0	1	1	0
Y	106	0	0	0	1	0	1	1	1
SP	107	1	0	1	1	1	1	1	1
D	108	0	0	1	1	1	0	1	1
O	109	0	0	1	1	0	1	0	1
G	110	0	0	1	1	1	1	0	0
SP	111	1	0	1	1	1	1	1	1
1	112	0	0	0	0	1	1	1	0
2	113	0	0	0	0	1	1	0	1
3	114	0	0	0	0	1	1	0	0
4	115	0	0	0	0	1	0	1	1
5	116	0	0	0	0	1	0	1	0
6	117	0	0	0	0	1	0	0	1
7	118	0	0	0	0	1	0	0	0
8	119	0	0	0	0	0	1	1	1
9	120	0	0	0	0	0	1	1	0
0	121	0	0	0	0	0	1	0	1
SP	122	1	0	1	1	1	1	1	1
D	123	0	0	1	1	1	0	1	1
E	124	0	0	1	1	1	0	0	1
SP	125	1	0	1	1	1	1	1	1
DEL	126	1	1	1	1	1	1	0	0
DEL	127	1	1	1	1	1	1	0	0

		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
		BAUDOT							
		–	–	–	5	4	3	2	1
128	CR	1	1	1	1	0	1	1	1
129	CR	1	1	1	1	0	1	1	1
130	LF	1	1	1	1	1	1	0	1
131	LTR	1	1	1	0	0	0	0	0
132	T	1	1	1	0	1	1	1	1
133	H	1	1	1	0	1	0	1	1
134	E	1	1	1	1	1	1	1	0
135	SP	1	1	1	1	1	1	0	1
136	Q	1	1	1	0	1	0	0	0
137	U	1	1	1	1	1	1	0	0
138	I	1	1	1	1	1	0	0	1
139	C	1	1	1	1	0	0	0	1
140	K	1	1	1	1	0	0	0	0
141	SP	1	1	1	1	1	0	1	1
142	B	1	1	1	0	0	1	1	0
143	R	1	1	1	1	0	1	0	1
144	O	1	1	1	0	0	0	1	1
145	W	1	1	1	0	1	1	0	0
146	N	1	1	1	1	0	0	1	1
147	SP	1	1	1	1	1	0	1	1
148	F	1	1	1	1	0	0	1	0
149	O	1	1	1	0	0	1	1	1
150	X	1	1	1	0	0	0	1	0
151	SP	1	1	1	1	1	0	1	1
152	J	1	1	1	1	0	1	0	0
153	U	1	1	1	1	1	0	0	0
154	M	1	1	1	0	0	0	1	1
155	P	1	1	1	0	1	0	0	1
156	S	1	1	1	1	1	0	1	0
157	SP	1	1	1	1	1	0	1	1
158	O	1	1	1	0	0	1	1	1
159	V	1	1	1	1	0	0	0	1
160	E	1	1	1	1	1	1	1	0
161	R	1	1	1	1	0	1	0	1
162	SP	1	1	1	1	1	1	0	1
163	T	1	1	1	0	1	1	1	1
164	H	1	1	1	0	1	0	1	1
165	E	1	1	1	1	1	1	1	0
166	SP	1	1	1	1	1	0	1	1
167	L	1	1	1	0	1	1	0	1
168	A	1	1	1	1	1	1	0	0
169	Z	1	1	1	0	1	1	1	0
170	Y	1	1	1	0	1	0	1	0
171	SP	1	1	1	1	1	0	1	1
172	D	1	1	1	1	0	1	1	0
173	O	1	1	1	0	0	1	1	1
174	G	1	1	1	1	0	0	1	0
175	SP	1	1	1	1	1	0	1	1
176	FIG	1	1	1	0	0	1	0	0
177	1	1	1	1	0	1	0	0	0
178	2	1	1	1	0	1	1	0	0
179	3	1	1	1	1	1	1	1	0
180	4	1	1	1	1	0	1	0	1
181	5	1	1	1	0	1	1	1	1
182	6	1	1	1	0	1	0	1	0
183	7	1	1	1	1	1	0	0	0
184	8	1	1	1	1	1	0	0	1
185	9	1	1	1	0	0	1	1	1
186	0	1	1	1	0	1	0	0	1
187	SP	1	1	1	1	1	0	1	1
188	LTR	1	1	1	0	0	0	0	0
189	D	1	1	1	1	0	1	1	0
190	E	1	1	1	1	1	1	1	0
191	SP	1	1	1	1	1	0	1	1

		PARITY	B_7	B_6	B_5	B_4	B_3	B_2	B_1
		USASCII							
		Y							
192	NULL	0	0	0	0	0	0	0	0
193	CR	0	1	1	1	0	0	1	0
194	CR	0	1	1	1	0	0	1	0
195	LF	1	1	1	1	0	1	0	1
196	T	0	0	1	0	1	0	1	1
197	H	1	0	1	1	0	1	1	1
198	E	0	0	1	1	1	1	0	1
199	SP	0	1	0	1	1	1	1	1
200	Q	0	0	1	0	1	1	1	0
201	U	1	0	1	0	1	0	1	0
202	I	0	0	1	1	0	1	1	0
203	C	0	0	1	1	1	1	0	0
204	K	1	0	1	1	0	1	0	0
205	SP	0	1	0	1	1	1	0	1
206	B	1	0	1	1	1	1	0	1
207	R	0	0	1	0	1	1	0	1
208	O	0	0	1	1	0	0	0	0
209	W	0	0	1	0	1	0	0	0
210	N	1	0	1	1	0	0	0	1
211	SP	0	1	0	1	1	1	1	1
212	F	0	0	1	1	1	0	0	1
213	O	0	0	1	1	0	0	0	0
214	X	0	0	1	0	1	1	1	1
215	SP	0	1	0	1	1	1	1	1
216	J	0	0	1	1	0	1	0	1
217	U	1	0	1	0	1	0	1	0
218	M	1	0	1	1	0	0	1	0
219	P	1	0	1	0	1	1	1	1
220	S	1	0	1	0	1	1	0	0
221	SP	0	1	0	1	1	1	0	1
222	O	0	0	1	1	0	0	0	0
223	V	1	0	1	0	1	0	0	1
224	E	0	0	1	1	1	0	1	0
225	R	0	0	1	0	1	1	0	1
226	SP	0	1	0	1	1	1	0	1
227	T	0	0	1	0	1	0	1	1
228	H	1	0	1	1	0	0	1	1
229	E	0	0	1	1	1	0	1	0
230	SP	0	1	0	1	1	1	1	1
231	L	0	0	1	1	0	0	1	1
232	A	1	0	1	1	1	1	1	0
233	Z	1	0	1	0	0	1	0	1
234	Y	1	0	1	0	0	1	1	0
235	SP	0	1	0	1	1	1	1	1
236	D	1	0	1	1	1	0	1	1
237	O	0	0	1	1	1	0	0	0
238	G	1	0	1	1	1	1	0	0
239	SP	0	1	0	1	1	1	1	1
240	1	0	1	0	0	0	1	1	0
241	2	0	1	0	0	0	1	0	1
242	3	1	1	0	0	0	1	0	0
243	4	0	1	0	0	0	1	1	1
244	5	1	1	0	0	0	1	1	0
245	6	1	1	0	0	0	1	0	1
246	7	0	1	0	0	0	1	0	0
247	8	0	1	0	0	0	0	1	1
248	9	1	1	0	0	0	0	1	0
249	0	1	1	0	0	0	1	1	1
250	SP	0	1	0	1	1	1	1	1
251	D	1	0	1	1	1	0	1	1
252	E	0	0	1	1	1	0	1	0
253	SP	0	1	0	1	1	1	1	1
254	DEL	0	0	0	0	0	0	0	0
255	DEL	0	0	0	0	0	0	0	0

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TMS 2700 JC, TMS 2700 JM, TMS 2700 NC
3072-BIT STATIC READ-ONLY MEMORY

FEBRUARY, 1971

features

- 256 x 12 organization
- Static operation
- Direct TTL compatibility
- Single-ended output buffers
- 28-lead dual-in-line package
- 3-line programmable chip select
- Chip enable
- 900-ns access time
- Low-threshold technology
- Full military temperature range (TMS 2700 JM)

description

The TMS 2700 is a static read-only memory with a capacity of 256 12-bit words. The device is constructed on a single monolithic chip, with MOS P-channel enhancement-mode low-threshold technology. Single-ended output buffers and a 3-line chip select allow the user to wire OR up to eight of these static ROMs, with no additional logic.

Programming of the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

The TMS 2700 JC and JM are mounted in 28-pin ceramic dual-in-line packages. TMS 2700 NC is mounted in a 28-pin plastic package.

The temperature range is −25°C to +85°C for the TMS 2700 JC and the TMS 2700 NC, and −55°C to +125°C for the TMS 2700 JM.

logic definition

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

operation

The TMS 2700 series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged.

"Access time" is defined as the maximum time required for all outputs to reach the minimum logic 1 levels or maximum logic 0 levels with the correct data. This duration is measured from that point in time at which all address inputs and chip-select inputs are valid.

A disable input on the chip-enable input will cause the outputs to become open circuits. The memory will be enabled when the chip select is at logic 0.

The output buffers are single ended, open drain and allow the wired-OR connection.

Three chip-select lines (CS_0, CS_1. CS_2) allow the user to wire OR up to eight TMS 2700 devices. The memory will be selected for one and only one chip-select word. This word is selected by the user and programmed in the memory when the memory content is programmed.

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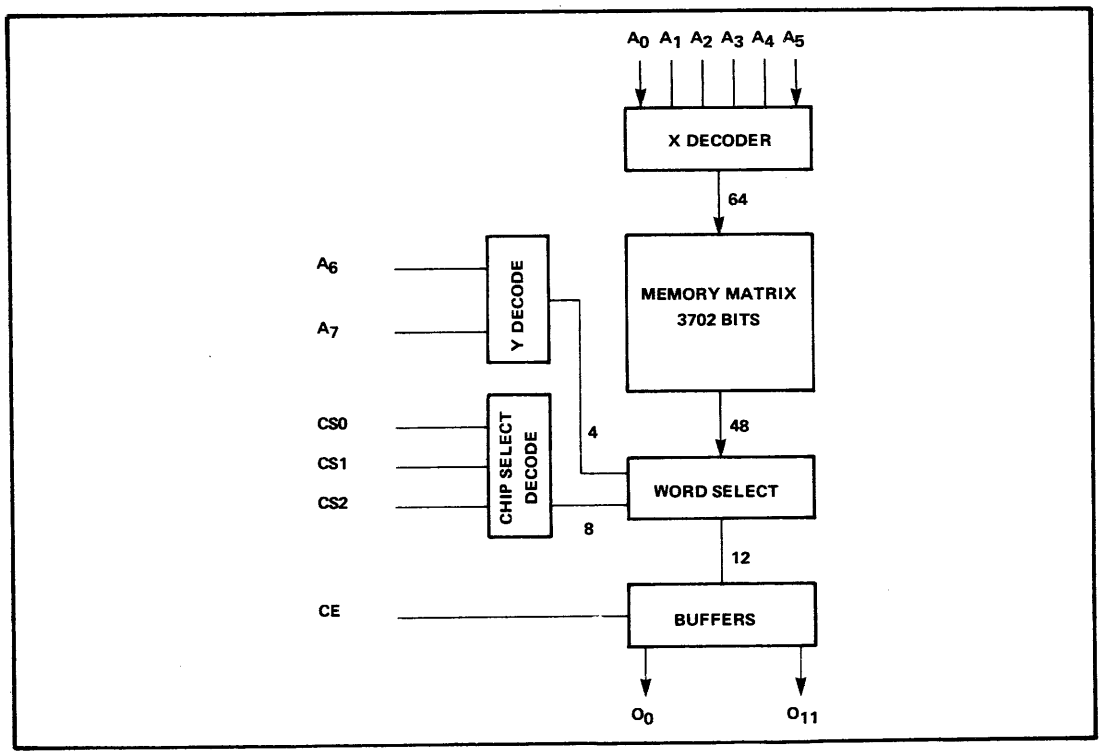
data encoding

Information concerning memory content and chip select should be submitted on the TMS 2700 Software Package. Data to be stored in the memory should be entered on punched cards in the format described by the Software Package.

functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{GG} range (See Note 1) . . . . . −22 V to 0.3 V
Chip enable voltage range (See Note 1) . . . . . −22 V to 0.3 V
Address and chip select voltage range . . . . . −22 V to 0.3 V
Operating free-air temperature range
- TMS 2700 JC/NC . . . . . −25 V to 85 V
- TMS 2700 JM . . . . . −55 V to 125 V

Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate supply V_{SS}	4.75	5.00	5.25	V
Gate supply V_{GG}	−13.5	−15	−16.5	V
Logic Levels				
Input HIGH level (1) V_{IH}	2.6		5.00	V
Input LOW level (0) V_{IL}			0.5	V

static electrical characteristics (under nominal operating conditions over operating temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL} Input Current	V_{IN} = 0 V			2	μA
Output Voltage Levels					
V_{OL} Output LOW level (0)	See Note 3				V
V_{OH} Output HIGH level (1)	I_{SOURCE} = 2.5 μA, V_{SS} = 4.75 V	2.4			V
V_{OL} Output LOW level (0)	Load 20 kΩ to −15 V (Note 4)	−13.5	−14.5		V
V_{OH} Output HIGH level (1)	Load 20 kΩ to −15 V (Note 4)	+3.5	+4.0		V
Power Supply Current Drain					
I_{SS} Substrate supply				32	mA
I_{GG} Gate supply				32	mA
P_D Power dissipation	Chip enable logic 1			350	mW
	Chip enable logic 0			650	mW

NOTES: 3. For an output logic 0, the output buffer transistor is Off and the impedance between the output terminal and V_{SS} is of several MΩ (leakage current $<$10 μA).

4. Recommended for MOS interface.

dynamic electrical characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Access Time (Notes 5 and 6)					
t_{AC}	−10°C to +70°C			900	ns
t_{AR}	−55°C to +125°C			1150	ns
Capacitance					
Input and chip select				5	pF

NOTES: 5. Load is one TTL gate plus a 20 pF capacitance. For final test purposes a worst-case TTL load is simulated by a 2.7-kΩ resistor and a 20 pF capacitance.

6. See timing diagram.

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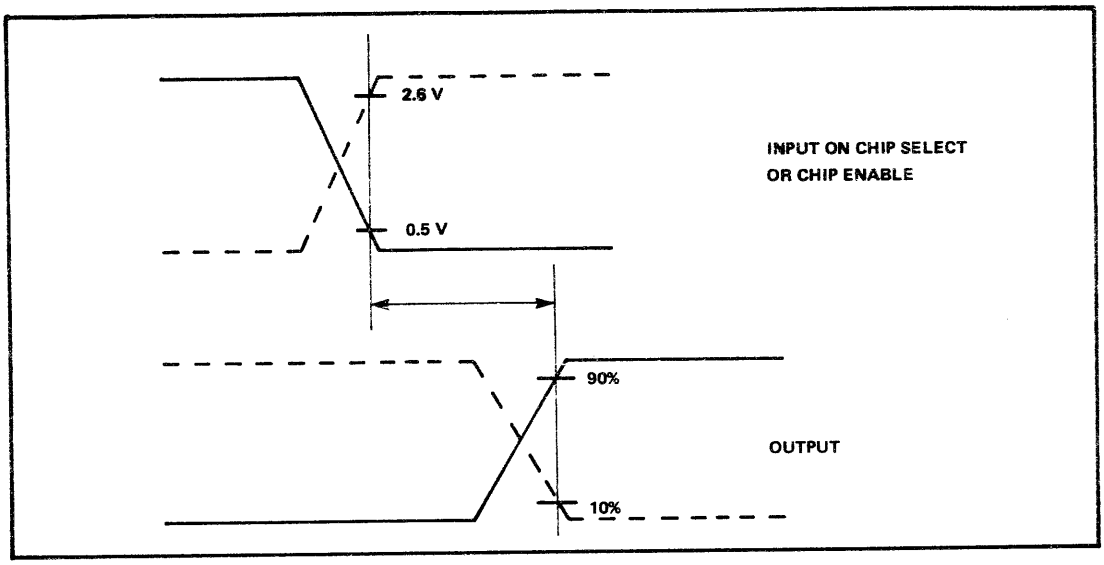
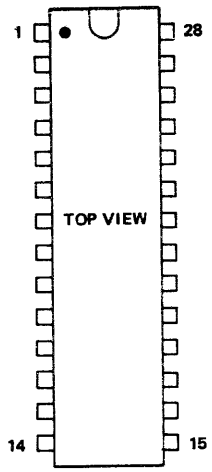
timing diagram and voltage waveforms



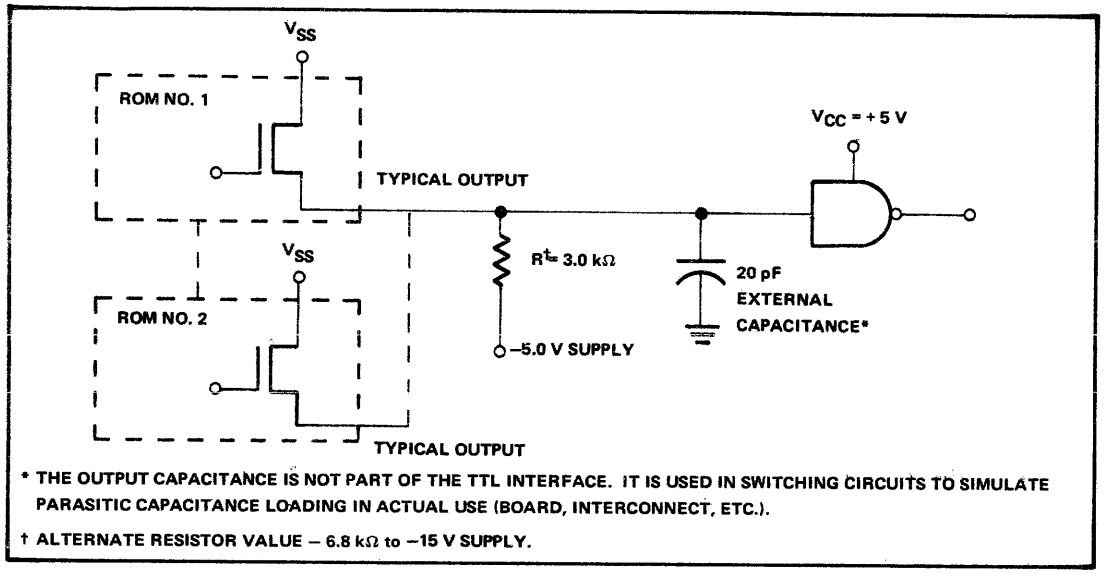
mechanical data and pin configuration

The TMS 2700 JC and TMS 2700 JM are mounted in 28-pin hermetically sealed dual-in-line packages consisting of a ceramic base, gold-plated cap, and gold-plated leads. The TMS 2700 NC is mounted in a 28-pin plastic dual-in-line package. The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	O_{10}	15	CS_1
2	O_9	16	CE
3	O_8	17	A_5
4	O_7	18	A_4
5	O_6	19	A_3
6	O_5	20	A_2
7	O_4	21	A_1
8	O_3	22	A_0
9	O_2	23	A_6
10	O_1	24	A_7
11	O_0	25	No connection
12	V_1	26	V_{SS}
13	CS_3	27	No connection
14	CS_2	28	O_{11}

TTL interface circuit



* THE OUTPUT CAPACITANCE IS NOT PART OF THE TTL INTERFACE. IT IS USED IN SWITCHING CIRCUITS TO SIMULATE PARASITIC CAPACITANCE LOADING IN ACTUAL USE (BOARD, INTERCONNECT, ETC.).

† ALTERNATE RESISTOR VALUE – 6.8 kΩ to –15 V SUPPLY.

SOFTWARE PACKAGE

Programming information for the TMS 2700 should be transmitted to TI in the form of a DECK OF 64 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Each card in the data deck describes the outputs for four input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

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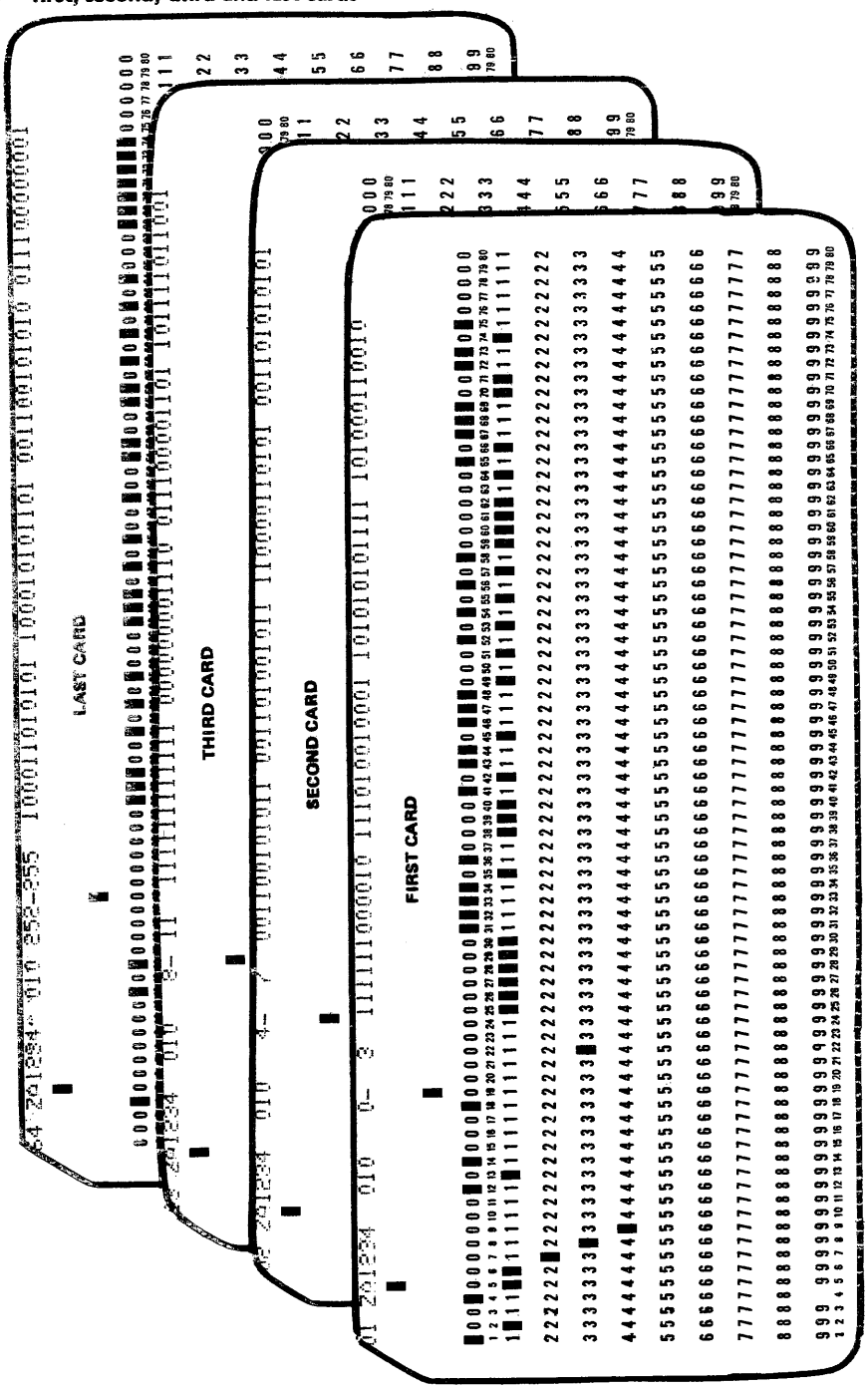
TMS 2700 — first, second, third and last cards



data card format

COLUMN	
1–2	Punch the sequential card number (01 through 64).
3	Blank
4–9	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers).
10	Blank (a space for the revision letter if necessary)
11	Blank
12–14	Punch chip-select logic CS0, CS1, CS2. A "1" for a logical 1 and a "0" for a logical 0.
15	Blank
16–18	Punch a right-justified integer representing the binary input address (0-255) for the first set of outputs described on the card
19	Punch a "–" (minus sign)
20–22	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card.
23–24	Blank
25–75	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0. Each card will describe 4 output sets.
25–36	Punch the outputs desired for O_{11}, O_{10}, O_9, O_8, O_7, O_6, O_5, O_4, O_3, O_2, O_1, O_0, in that order, for the first address specified on the card.
38–49	Punch the outputs desired for the second address.
51–62	Punch the outputs desired for the third address.
64–75	Punch the outputs desired for the fourth address.

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TMS 2800 JC, TMS 2800 NC
1024-BIT STATIC READ-ONLY MEMORY

JANUARY, 1971

features

- 1024-bit capacity
- Static operation
- Maximum access time under 1 microsecond
- Open-drain output buffers or double-ended buffers
- TTL compatible
- 16-pin dual-in-line package

description

The TMS 2800 JC/NC series is a family of static read-only memories, each having a capacity of 1024 bits.

Programming of the memory content and output buffer configuration is accomplished by changing a single mask during device fabrication.

A chip-select input is available.

The memory contents consist of 256 words of four bits.

Two types of output buffers are available:

- Single-Ended (open drain)

  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.

- Double-Ended

  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

"TMS 2800 JC" designates a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package, and "TMS 2800 NC" is used for a unit mounted in a 16-pin plastic package.

logic definition

Negative logic is assumed.

a) Logical 1 = most negative voltage

b) Logical 0 = most positive voltage

operation

The TMS 2800 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

Access time is defined as the time between a change of data on any logic input or chip-select line and the change of data on the output of a TTL gate. (See timing diagram)

— continued

operation (continued)

A logical 0 on the chip select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. Note that, when using the hardwired output technique, all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 4)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−9		−12	V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ	0		−2.0	V
t_{A1}	Access time (Note 3)	See switching circuit		600	900	ns
t_{A2}	Access time (Note 3)	See switching circuit		620	900	ns
P_d	Power dissipation (Note 2)	All outputs at Logical 0		170		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		5		pF
I_{DD}	Drain current	All outputs @ Logical 0		15		mA
I_{GG}				1.0		μA

NOTES: 1. Open-drain buffer
2. Push-pull buffer
3. See switching diagram
4. Either open-drain or push-pull configuration

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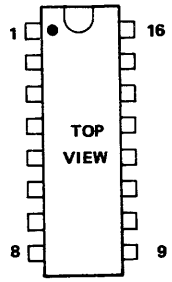
mechanical data and pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 2800 JC) and a 16-pin plastic package (TMS 2800 NC). These packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

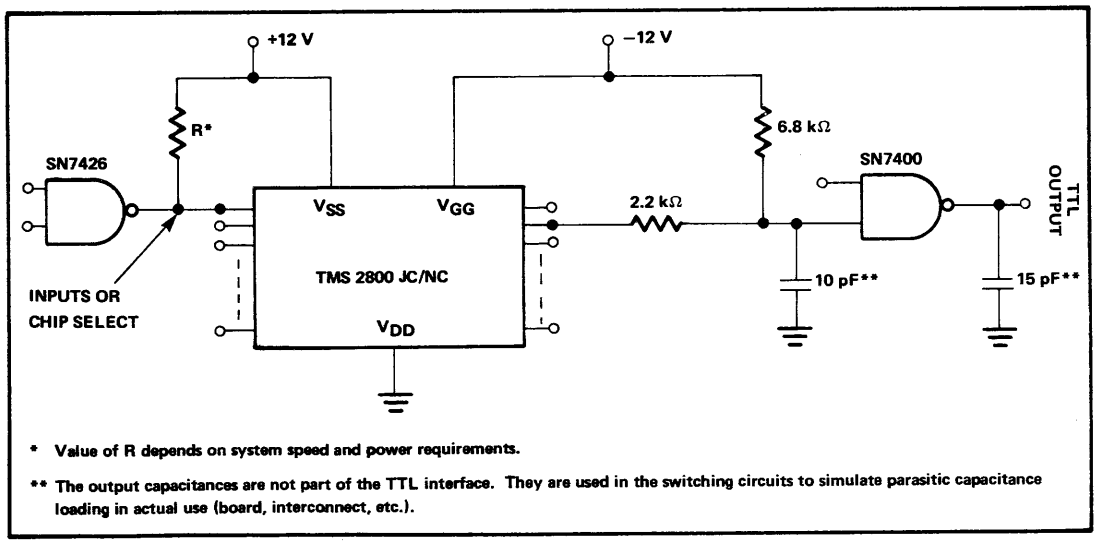


PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	9	A_8
2	A_2	10	CS
3	A_1	11	V_{GG}
4	B_1	12	A_7
5	B_2	13	A_6
6	B_3	14	A_5
7	B_4	15	A_4
8	V_{SS}	16	V_{DD}

A – input
B – output
V_{SS} – substrate

V_{DD} – drain supply
V_{GG} – gate supply

switching circuit and TTL interface



* Value of R depends on system speed and power requirements.

** The output capacitances are not part of the TTL interface. They are used in the switching circuits to simulate parasitic capacitance loading in actual use (board, interconnect, etc.).

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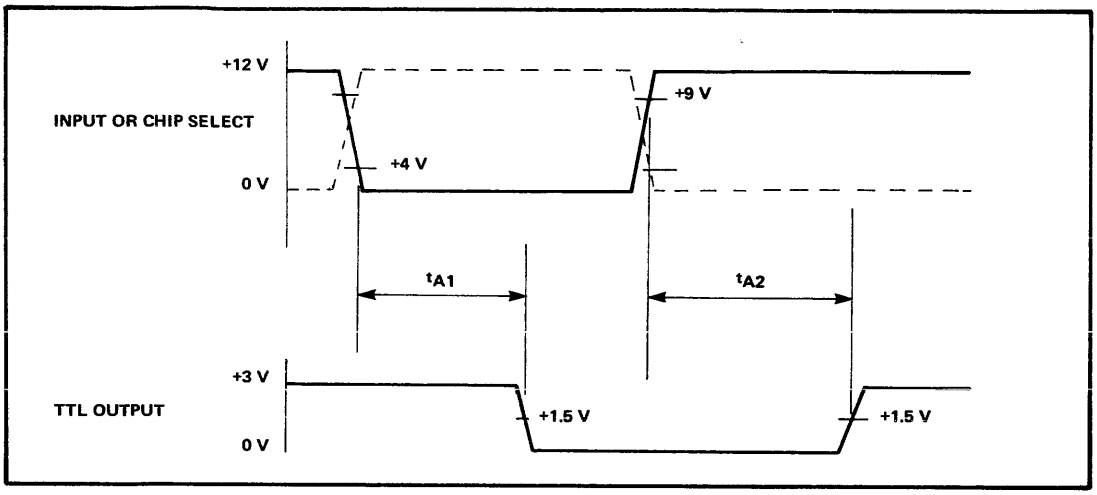
switching diagram



SOFTWARE PACKAGE

input format

Programming information for the TMS 2800 JC/NC should be transmitted to TI in the form of a DECK of 22 STANDARD 80-COLUMN COMPUTER CARDS, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI should be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the buffer option desired will be transmitted on a special form supplied by TI.

Each card in the data deck describes the outputs for twelve input addresses. All addresses must have their outputs defined. The addresses must also be placed in consecutive order. Cards should be punched according to the following format.

data card format

Column	
1-2	Punch the sequential card number (01 through 22)
3	Blank
4-5	Punch a "28" to signify TMS 2800 JC/NC
6-11	Punch the Z identification number supplied by TI MOS Marketing (2 letters, 4 numbers)

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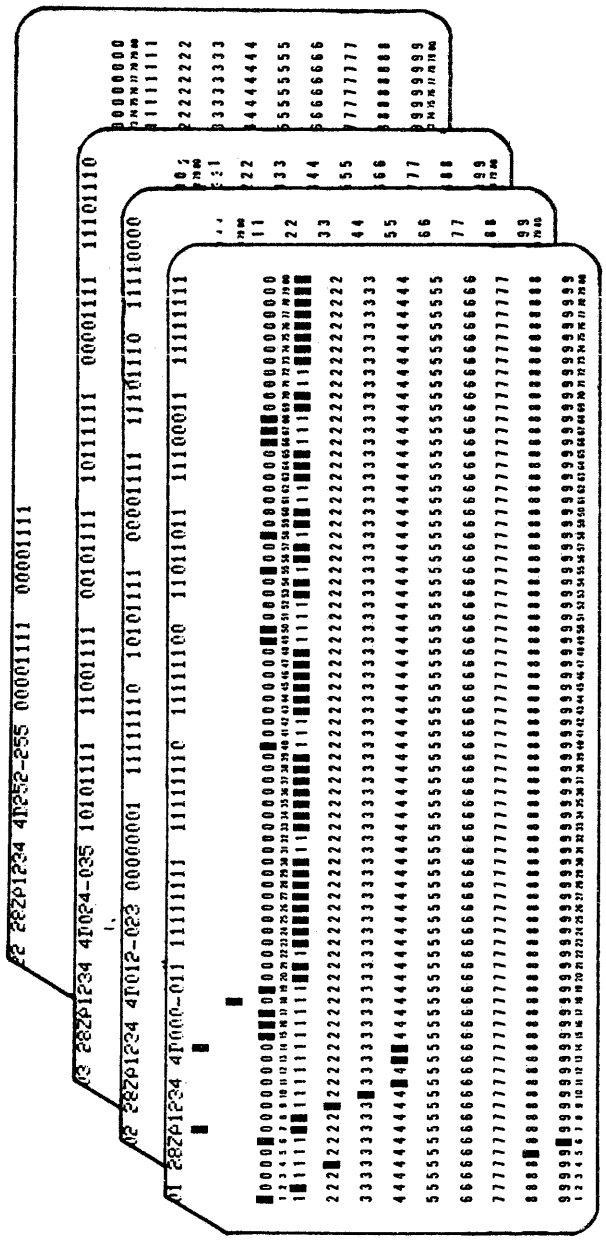
data card format (continued)

Column	
12	Blank (a space for the revision letter if necessary)
13	Punch a "4" to signify four outputs
14	Punch a "D" for open-drain type output buffers or punch a "P" for push-pull type output buffers
15-17	Punch a right-justified integer representing the binary input address (0-255) for the first set of outputs described on the card
18	Punch a "–" (minus sign)
19-21	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card
22	Blank
23-80	Punch a description of the output sets selected for the range of input addresses specified on the card. A "1" for a logical 1 and a "0" for a logical 0. Each card will describe 12 output sets. The 22nd card will contain only 4 output sets.
23-26	Punch the outputs desired for B_4, B_3, B_2, B_1 in that order, for the first address specified on the card.
27-30	Punch the outputs desired for the second address
33-36	Punch the outputs desired for the third address
37-40	Punch the outputs desired for the fourth address
43-46	Punch the outputs desired for the fifth address
47-50	Punch the outputs desired for the sixth address
53-56	Punch the outputs desired for the seventh address
57-60	Punch the outputs desired for the eighth address
63-66	Punch the outputs desired for the ninth address
67-70	Punch the outputs desired for the tenth address
73-76	Punch the outputs desired for the eleventh address
77-80	Punch the outputs desired for the twelfth address

TMS 2800 JC — first, second, third and last cards



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TMS 2801 JC, TMS 2801 NC
EIGHT-LEVEL PRIORITY ENCODER

FEBRUARY, 1971

features

- 1024-bit capacity
- static operation
- maximum access time under 1 microsecond
- open-drain output buffers
- TTL compatible

description

The TMS 2801 JC/NC is a programmed TMS 2800 JC/NC. All electrical and mechanical characteristics of the TMS 2800 JC/NC apply (See MOS product brochure CB-126) to this 1024-bit MOS read-only memory.

Programmed as a priority encoder, the TMS 2801 JC/NC generates an output code according to the priority levels present at its inputs. Each input corresponds to a priority level. The highest priority line that is "true" produces its characteristic output code, regardless of the state of the lower priority input lines. Although one TMS 2800 JC/NC has only enough inputs for eight priority levels, the chip-select input can be used to cascade devices for as many priority levels as necessary.

"TMS 2801 JC" designates a unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package. A unit mounted in a 16-pin plastic dual-in-line package is numbered "TMS 2801 NC".

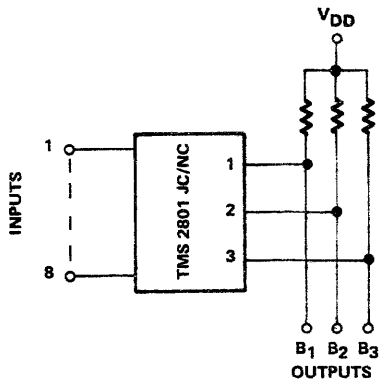
logic definition

Positive logic is assumed.

a) Logical 1 = most positive voltage

b) Logical 0 = most negative voltage

TMS 2801 JC/NC truth table for 8 priority levels



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS		
	B_3	B_2	B_1
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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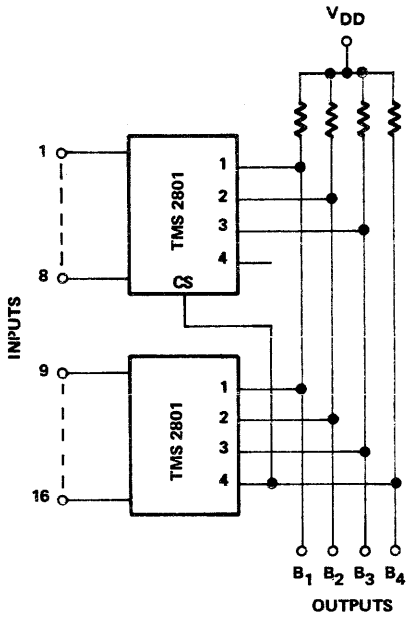
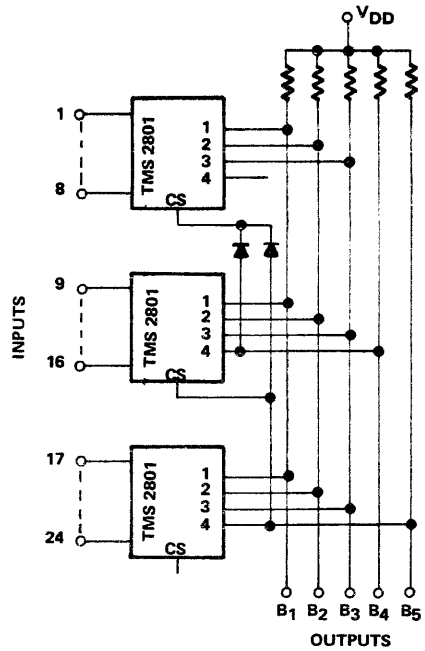
extension to 16-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS			
	B_4	B_3	B_2	B_1
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

extension to 24-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS				
	B_5	B_4	B_3	B_2	B_1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0
22	1	0	1	0	1
23	1	0	1	1	0
24	1	0	1	1	1

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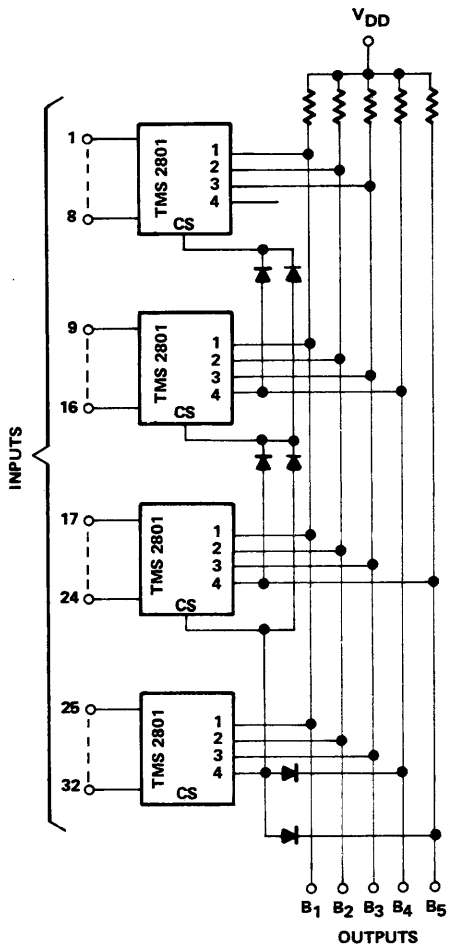
extension of 32-level priority encoder



MOST SIGNIFICANT INPUT AT A LOGICAL 1	OUTPUTS				
	B_5	B_4	B_3	B_2	B_1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0
22	1	0	1	0	1
23	1	0	1	1	0
24	1	0	1	1	1
25	1	1	0	0	0
26	1	1	0	0	1
27	1	1	0	1	0
28	1	1	0	1	1
29	1	1	1	0	0
30	1	1	1	0	1
31	1	1	1	1	0
32	1	1	1	1	1

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TMS 4100 JC, TMS 4100 NC
SERIES CHARACTER GENERATOR

FEBRUARY, 1971

features

- Static operation
- 2240-bit capacity
- 64 Characters of 35 bits (5 x 7) or
- 32 Characters of 70 bits (5 x 14)
- TTL compatible
- 700-ns maximum access time
- 7-bit input address
- Single-ended open-drain output buffers

description

The TMS 4100 JC/NC series is a family of MOS read-only memories, each with a capacity of 2240 bits. Two organizations are available:

1) 64 words of 35 bits (5 x 7)

2) 32 words of 70 bits (5 x 14)

The memory is organized to function primarily as a character generator. The seven outputs represent a column in a 5 x 7 dot matrix.

The output word appears as a 5-word sequence on each of the output lines. Sequence is controlled by 5 strobe lines (column select), which feed directly into the buffer section of the memory. By enabling the first strobe line, the first group of 7 bits (first column) is obtained at the output. Then the second, third, fourth, and fifth strobe lines are enabled. The column select can remain fixed while the character address changes, or the character address may remain fixed while the column select changes.

The decoder will accept a 7-bit parallel input. Because only six bits are required in order to decode the 64 input words, the seventh bit may be used as a chip enable. If the memory is organized as 32 words of 70 bits, it is possible to have two chip-enable lines.

The TMS 4100 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V_{GG} supply may be clocked to reduce power consumption without affecting access times.

Output buffers are single ended, open drain and allow the wired-OR connection.

The number of words per output is increased by hardwiring together the outputs of different devices. Hardwiring outputs perform the AND function in negative logic.

"TMS 4100 JC" designates a unit mounted in a 28-pin hermetically sealed ceramic dual-in-line package, and "TMS 4100 NC" is the part number for the unit mounted in a 28-pin plastic package.

logic definition

Negative logic is assumed for all inputs.

a) Logic 1 = most negative voltage (−14 V)

b) Logic 0 = most positive voltage (0 V)

An output dot is defined as the "on" state of the output MOS transistor and an output blank as the "off" state.

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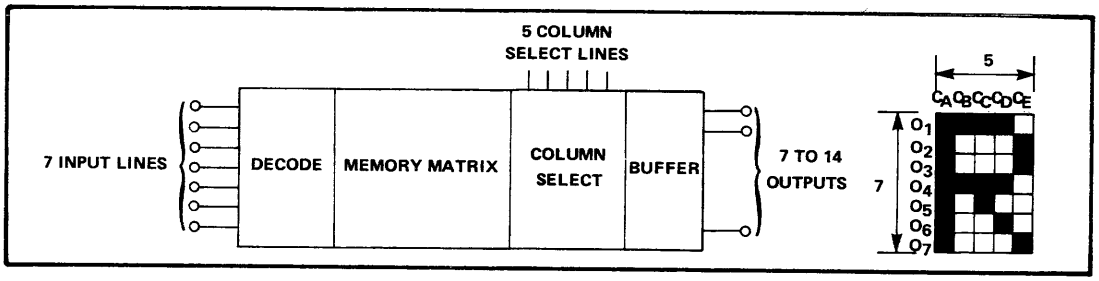
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−12	−14	−16	V
Supply voltage V_{GG}	−24	−28	−29	V
Input, column select and enable logic 1	−9	−14	−16	V
Input, column select and enable logic 0	+0.3	0	−3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V).

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

	PARAMETER (See Note 1)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{(1)}$	Output Blank Current (Note 2)	−14 V applied to output			10	μA
$I_{(0)}$	Output Dot Current (Note 2)	−14 V applied to output	1	2		mA
$I_{(0)}$	Output Dot Current (Note 2)	V_{DD} = −12 V, V_{GG} = −24 V, −12 V applied to output	0.5	1		mA
$V_{(0)}$	Output Voltage for a Dot (Note 2)	I_O = 0.5 mA		−1.3	−2.8	V
$V_{(1)}$	Output Voltage for a Dot (Note 2)	I_O = 1 mA		−2.5	−6	V
	Input and Column Select Leakage Current	−14 V applied to input			1	μA
I_{DD}	Drain Supply Current			14	25	mA
I_{GG}	Gate Supply Current				1	mA
	Power Dissipation			250	400	mW
	Address Input Capacitance			6	15	pF

NOTES: 1. These voltage values are with respect to network ground terminal (V_{SS}).
2. An output dot is defined as the On state of the MOS output transistor. An output blank is defined as the Off state.

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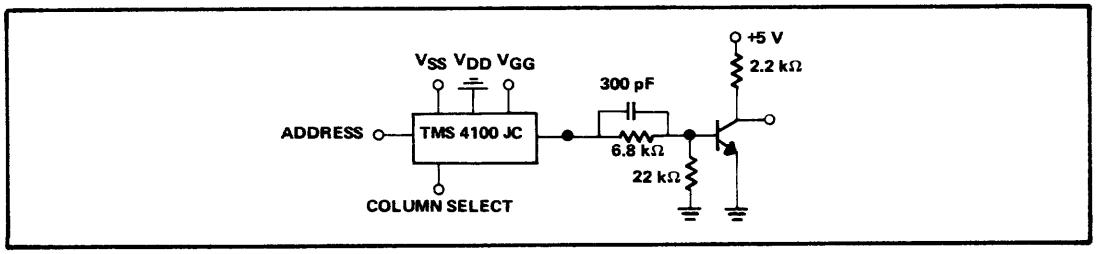
switching characteristics (at nominal operating conditions and 25°C unless otherwise noted)

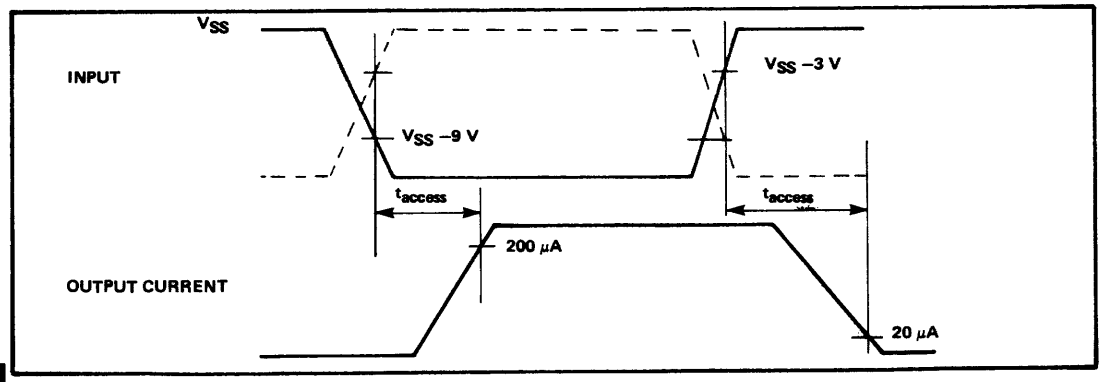
PARAMETER (Refer to Switching Diagram)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character Access Time, Bipolar Load			400	700	ns
Character Access Time, Bipolar Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		500	700	ns
Column-Select Access Time Bipolar Load			150	300	ns
Column-Select Access Time, Bipolar Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		200	350	ns
Character Access Time, Low Power TTL Load			500	850	ns
Character Access Time, Low Power TTL Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		600	950	ns
Column-Select Access Time, Low Power TTL Load			200	400	ns
Column-Select Access Time, Low Power TTL Load	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		300	500	ns

switching circuit and switching diagram

a) Bipolar load



address or column-select input voltage



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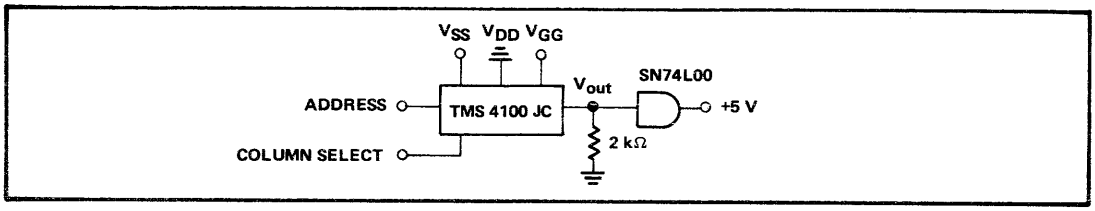
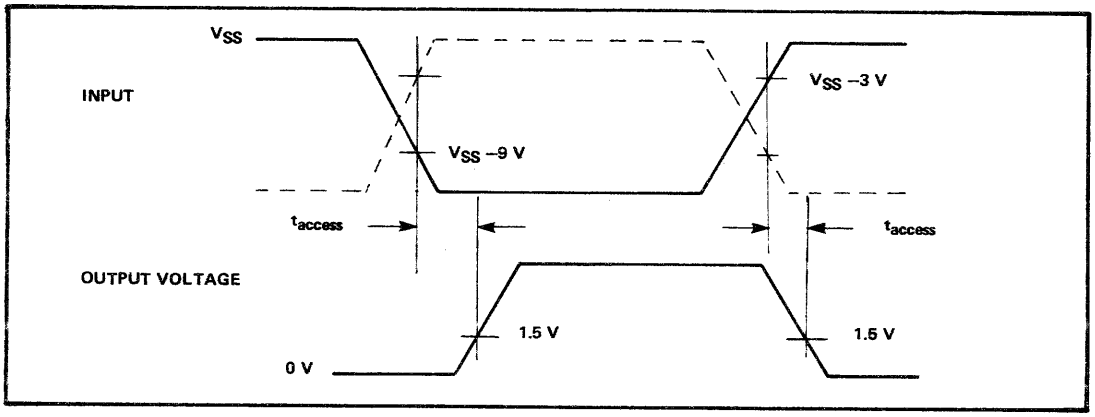
switching circuit and switching diagram (continued)

b) Low power TTL load



address or column select voltage



custom programmed devices

The TMS 4100 JC/NC series is programmed at the gate-oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate oxide removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization
- character format
- enable logic polarity (or permanently enabled)

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets are used. These encoding sheets (SOFTWARE PACKAGE) are available from the TI sales office.

mechanical data

This device is available in both a 28-pin hermetically sealed ceramic dual-in-line package (TMS 4100 JC) and a 28-pin plastic package (TMS 4100 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

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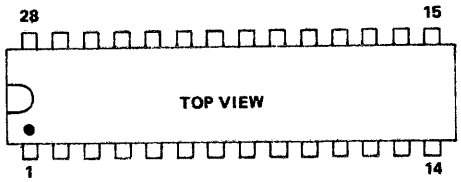
pin configuration

Depending on the organization of the memory, three pin configurations may be used.

Package Pin Configuration, TMS 4100 JC/NC

PIN NO.	CONFIGURATION A — TOTAL OUTPUTS— 7 OR FEWER	CONFIGURATION B — TOTAL OUTPUTS— MORE THAN 7, FEWER THAN 14	CONFIGURATION C — TOTAL OUTPUTS— 14
1	O_1	O_1	O_1
2	NC	O_2	O_2
3	O_2	O_3	O_3
4	NC	O_4	O_4
5	O_3	O_5	O_5
6	NC	O_6	O_6
7	O_4	O_7	O_7
8	NC	O_8	O_8
9	O_5	O_9	O_9
10	NC	O_{10}	O_{10}
11	O_6	O_{11}	O_{11}
12	NC	O_{12}	O_{12}
13	O_7	O_{13}	O_{13}
14	V_{DD}	V_{DD}	O_{14}
15	V_{GG}	V_{GG}	V_{DD}
16	I_6	I_6	V_{GG}
17	V_{SS}	V_{SS}	I_6
18	C_A	C_A	V_{SS}
19	C_B	C_B	C_A
20	C_C	C_C	C_B
21	C_D	C_D	C_C
22	C_E	C_E	C_D
23	I_5	I_5	C_E
24	I_4	I_4	I_5
25	I_3	I_3	I_4
26	I_2	I_2	I_3
27	I_1	I_1	I_2
28	I_7	I_7	I_1

NC – NOT CONNECTED O – OUTPUT I – INPUT
C – COLUMN SELECT



standard devices

Because certain codes are widely used, TI has created a series of standard devices that are available off the shelf and for which there is no coding charge. The most widely used standard device is: TMS 4103 JC/NC USASCII CODE (See attached character format).

Organization:
64-Character Storage
35-Bit Character Matrix
6-Parallel Character-Address Input
Chip Enabled by Logic 1 Applied to I_7

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standard devices (continued)

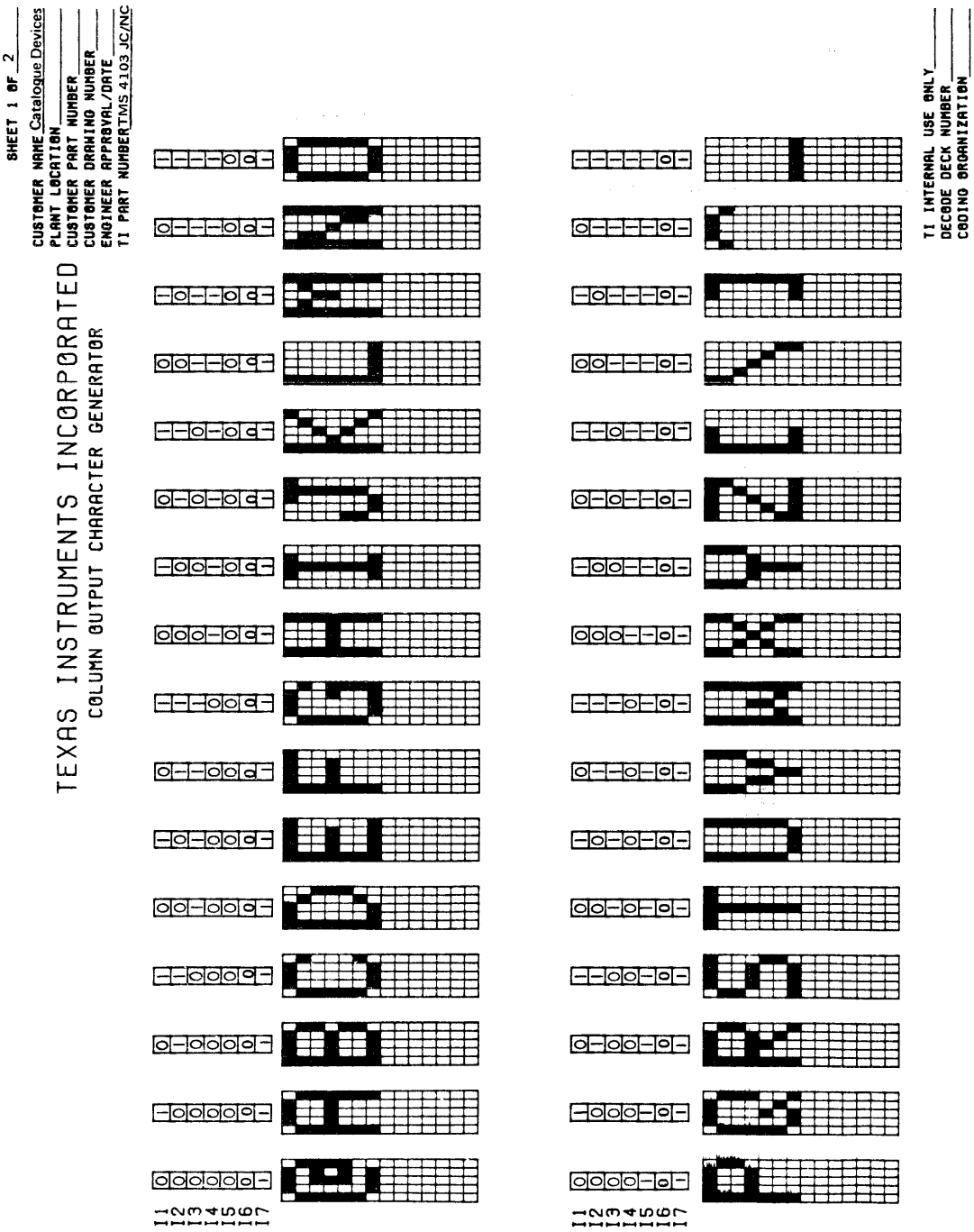
Other Available Standard Circuits:

- TMS 4177 JC/NC and TMS 4178 JC/NC. These two devices are used as a unit to implement a 7 x 10 row output character generator. The two devices are wired OR and are scanned in succession.
  - USASCII Code
  - 64-Character Storage
  - 7-Bit Parallel Input

  See attached character format.

- TMS 4179 JC/NC
  - EBCDIC Code
  - 64-Character Storage
  - 7-Bit Parallel Input

  See attached character format.



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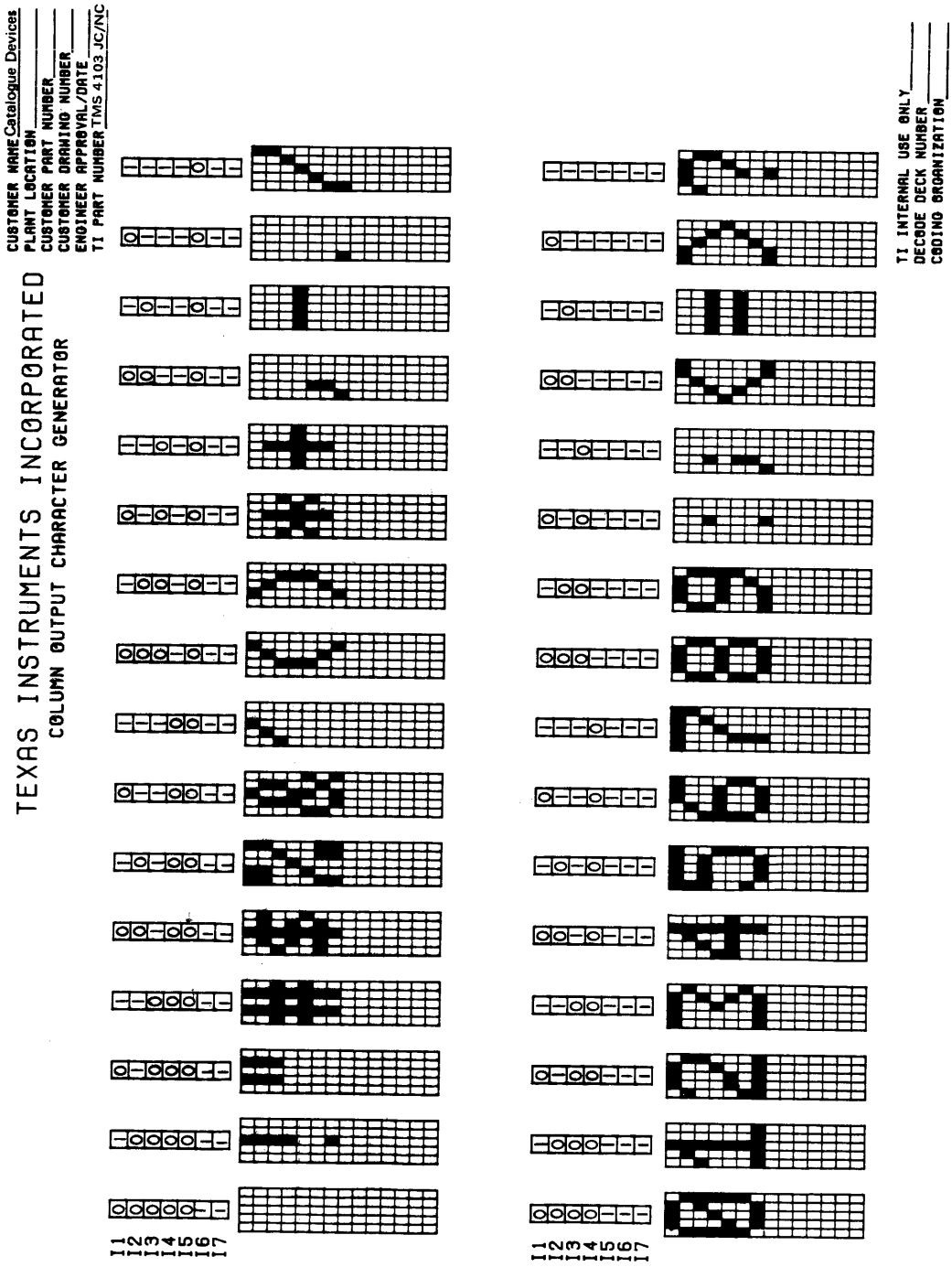
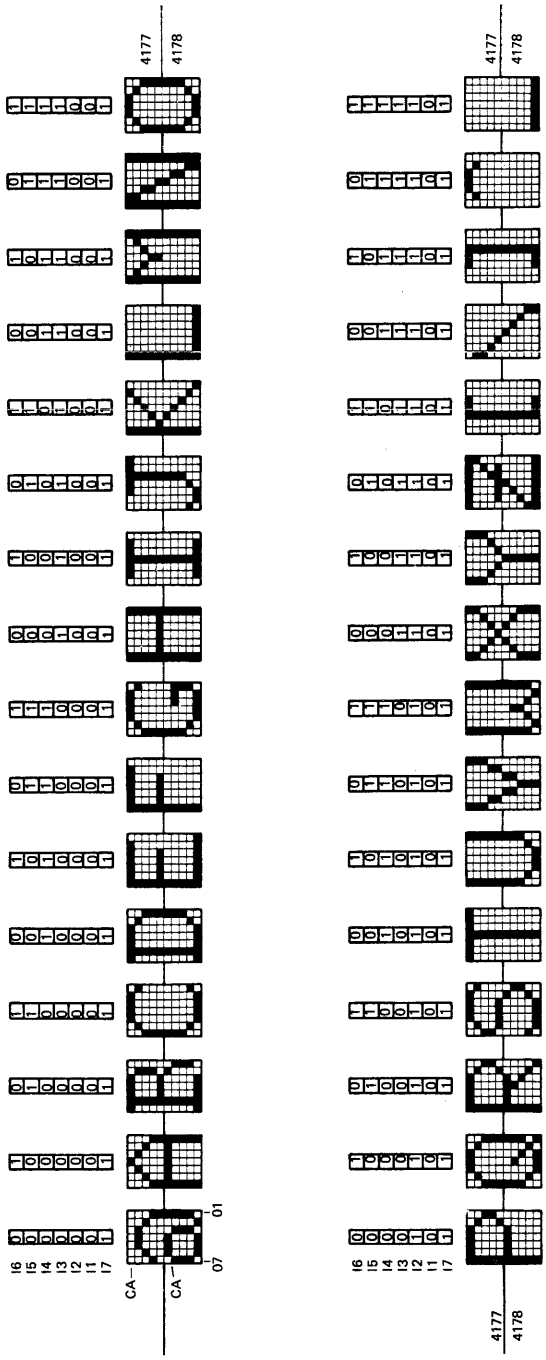

SHEET 2 OF 2
CUSTOMER NAME Catalogue Devices
PLANT LOCATION
CUSTOMER PART NUMBER
CUSTOMER DRAWING NUMBER
ENGINEER APPROVAL/DATE
TI PART NUMBER TMS 4103 JC/NC
TEXAS INSTRUMENTS INCORPORATED
COLUMN OUTPUT CHARACTER GENERATOR
TI INTERNAL USE ONLY
DECODE DECK NUMBER
CODING ORGANIZATION
I1 I2 I3 I4 I5 I6 I7
I1 I2 I3 I4 I5 I6 I7

TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC/NC – TMS 4178 JC/NC (Sheet 1 of 2)
7 x 10 USASCII CHARACTER DISPLAY



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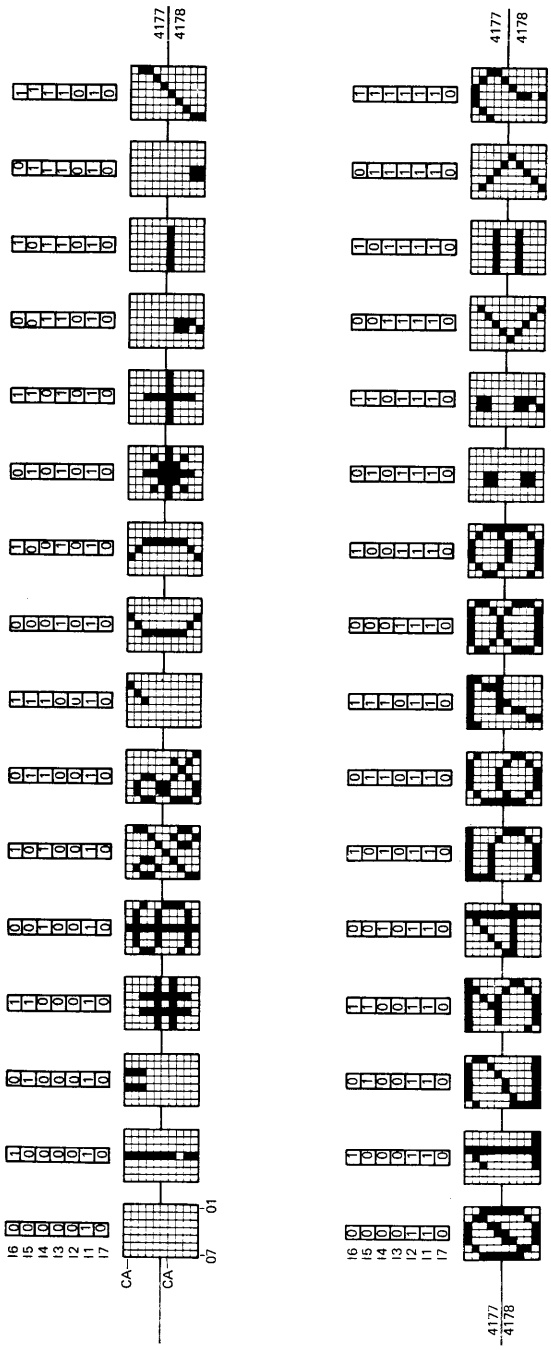
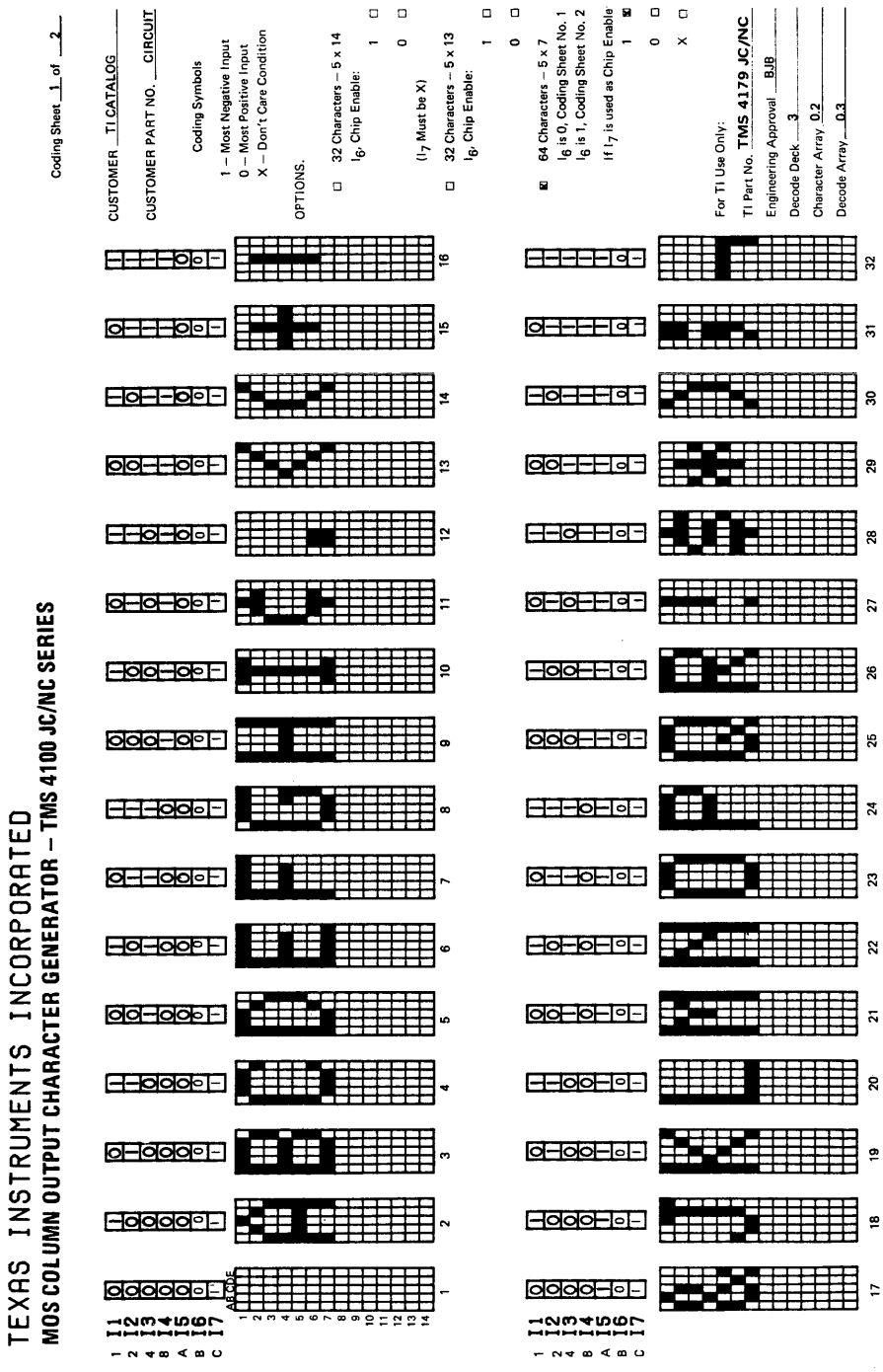
TEXAS INSTRUMENTS INCORPORATED
TMS 4177 JC/NC – TMS 4178 JC/NC (Sheet 2 of 2)
7 x 10 USASCII CHARACTER DISPLAY





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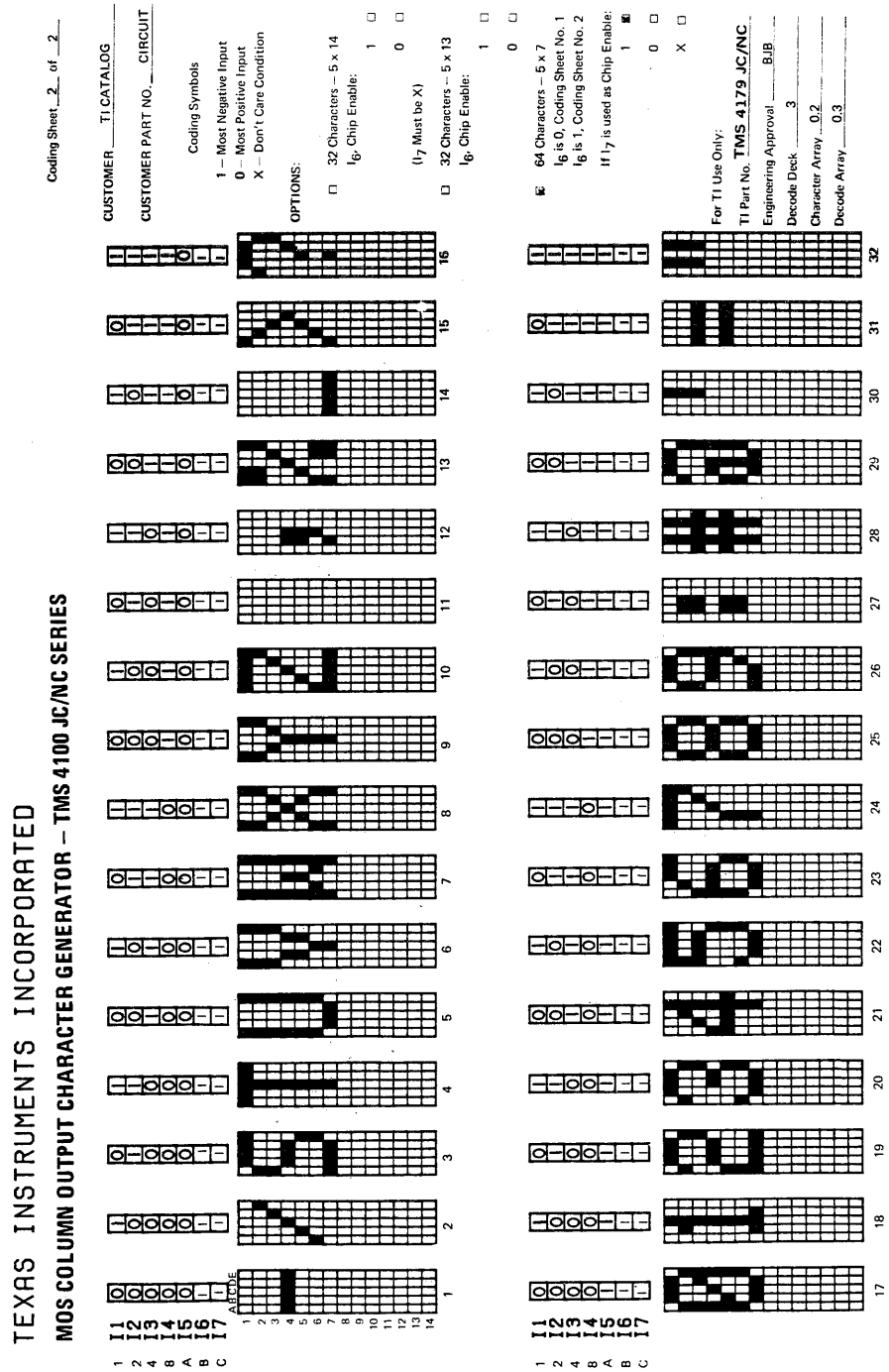

14

TMS 4400 JC, TMS 4400 NC
4096-BIT STATIC READ-ONLY MEMORY

features

- 4096-bit capacity
- Static operation
- Access time less than 1 microsecond (typical)
- Two organizations available
- Open-drain output buffers or double-ended buffers
- TTL compatible
- Three chip-select lines available
- 24-pin dual-in-line package
  ceramic – TMS 4400 JC
  plastic – TMS 4400 NC

description

The TMS 4400 JC/NC series is a family of static read-only memories, each with a capacity of 4096 bits. Two memory organizations and two output buffer configurations are provided through single-level mask programming.

The memory may be organized as 1024 words of four bits, or 512 words of eight bits.

"TMS 4400 JC" designates a unit mounted in a 24-pin ceramic dual-in-line package, and "TMS 4400 NC" is used for a unit mounted in a 24-pin plastic package.

Two types of output buffers are available:

- Single-Ended (open drain)
  Designed for driving TTL, this output has one MOS device with its drain at the output and its source at chip ground.
- Double-Ended
  Designed for driving the inputs to other MOS integrated circuits and devices, this version has its own MOS load resistor provided internally. It requires no additional external circuitry.

Depending on the device organization chosen by the user, there are either three chip selects (1024 words by 4 bits) or four (512 words by 8 bits).

Each bit of the chip select address may be programmed as a logic 1, a logic 0, or a "don't care" (unused) input.

logic definition

Negative logic is assumed.

a) Logic 1 = most negative voltage.

b) Logic 0 = most positive voltage.

operation

The TMS 4400 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged.

– continued

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operation (continued)

"Access time" is defined as the maximum time required for all outputs to reach the minimum logic 1 levels or maximum logic 0 levels with the correct data. This time is measured from that point in time at which all address inputs and chip-select inputs are valid.

A disable input word on the chip-select input will cause the outputs to become open circuits on the "single-ended" (open-drain) type output buffer and will cause the outputs to go to V_{DD} on the double-ended (push-pull) type output buffer.

The number of words per output is increased by hardwiring together the outputs of different devices. This means that if the 512 x 8 chip configuration is used, a memory system may be built using 16 TMS 4400 JC/NC devices for a 8192-words-of-8-bits memory without additional external logic. If the 1024 x 4 organization is chosen, eight TMS 4400 JC/NC devices may be hardwired without additional logic. When using the hardwired output technique, note that all devices should have single-ended buffers. Hardwiring outputs performs the AND function in negative logic.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1) . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range (See Note 1) . . . . . −30 V to 0.3 V
Data input voltage ranges (See Note 1) . . . . . −30 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−9	−12	−22	V
Supply voltage V_{GG}	−18	−24	−29	V
Input, chip select logic 1	−8	−12	−22	V
Input, chip select logic 0	+0.3	0	−3	V
Input pulse width	550			ns

The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, −12 V). Larger power supplies (e.g., +14 V, −14 V) may be used.

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{out(0)}$	Logical 0 output current (Note 1)	−12 V applied to output	3	7		mA
$I_{out(1)}$	Logical 1 output current (Note 1)	−12 V applied to output			10	μA
$Z_{out(1)}$	Logical 1 output impedance (Note 2)	V applied = V_{DD} + 3		18	25	kΩ
$Z_{out(0)}$	Logical 0 output impedance (Note 3)	V applied = V_{SS} −3		0.8	1.1	kΩ
$V_{out(1)}$	Logical 1 output voltage (Note 2)	R_L = 1 mΩ	−10			V
$V_{out(0)}$	Logical 0 output voltage (Note 2)	R_L = 1 mΩ			−2.0	V

NOTES: 1. Open-drain buffer
2. Double-ended buffer
3. Either open-drain or double-ended configuration

— continued

electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted) — continued

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
P_d	Power dissipation (Note 2)	All outputs at Logical 0		250		mW
I_L	Input leakage current	−12 V applied to input			1	μA
C_{in}	Input capacitance	V_{in} = 0 V, f = 1 MHz		10		pF
I_{DD}	Drain current (Note 2)	All outputs = Logical 0		20		mA
I_{GG}	Gate current			1.0		μA

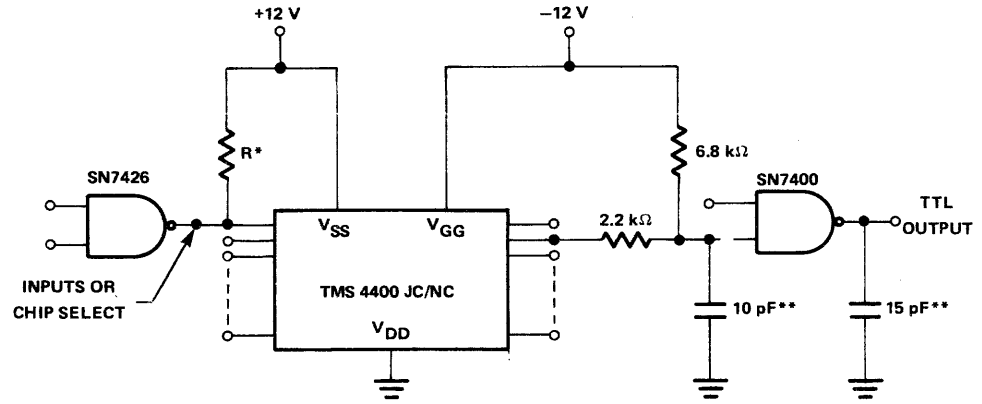
NOTE 2: Double-ended buffer

dynamic electrical characteristics (under nominal operating conditions and at 25°C unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{A1}	Access time TTL load (Notes 1 & 2)	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		900	1500	ns
t_{A2}	Access time TTL load (Notes 1 & 2)	V_{SS} = +12 V, V_{DD} = 0 V, V_{GG} = −12 V		700	1300	ns
t_{A1}	Access time (Notes 2 & 3)	V_{GG} = −24 V, V_{DD} = −12 V		1.5	2.0	μs
t_{A2}	Access time (Notes 2 & 3)	V_{GG} = −24 V, V_{DD} = −12 V		0.8	1.5	μs

NOTES: 1. Open ended buffer
2. See Switching Diagram
3. Double-ended buffer R_L = 1 MΩ, C = 20 pF

switching circuit and TTL interface



* VALUE OF R DEPENDS ON SYSTEM SPEED AND POWER REQUIREMENTS.

** THE OUTPUT CAPACITANCES ARE NOT PART OF THE TTL INTERFACE. THEY ARE USED IN THE SWITCHING CIRCUITS TO SIMULATE PARASITIC CAPACITANCE LOADING IN ACTUAL USE (BOARD, INTERCONNECT, ETC.).

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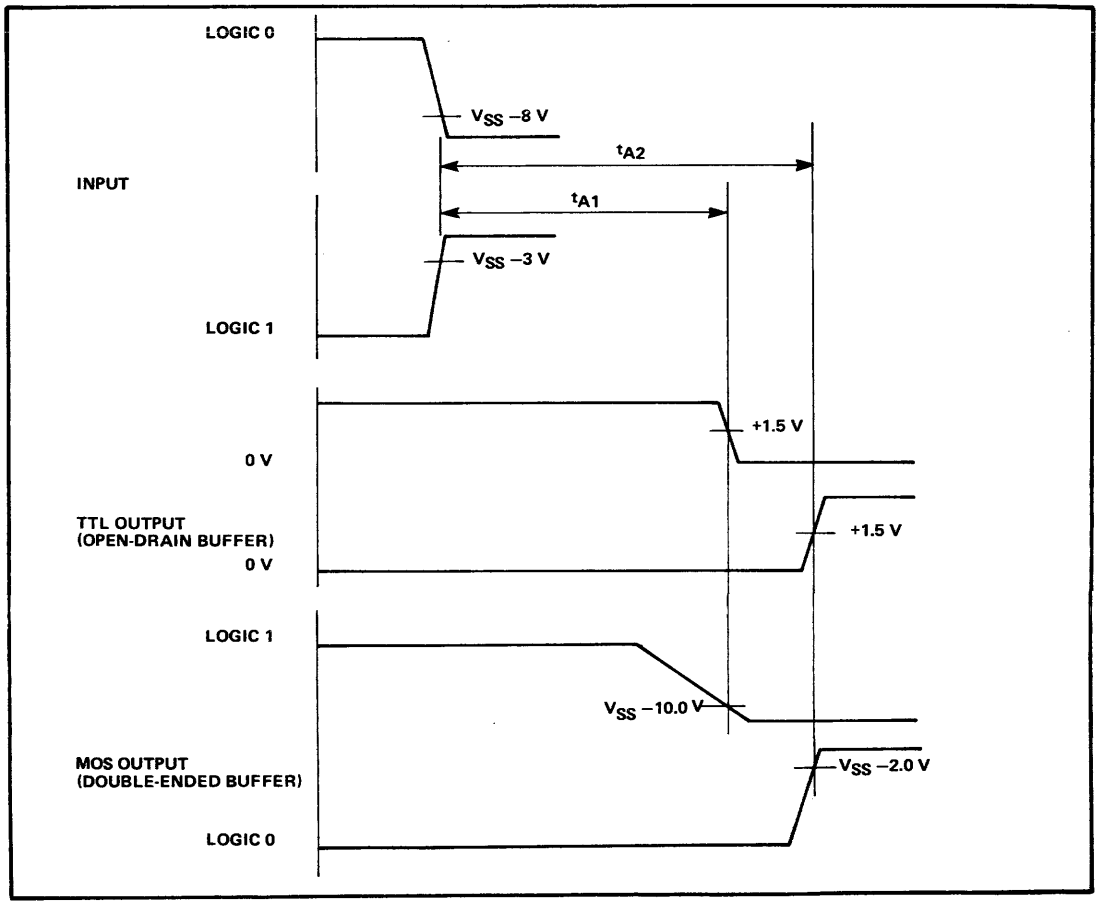
switching diagram (TTL load)



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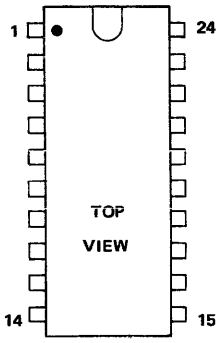
mechanical data and pin configuration

The device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 4400 JC) and a 24-pin plastic package (TMS 4400 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

Depending on the organization of the memory, 2 pin configurations may be used:



PIN NO.	512 x 8	1024 x 4	PIN NO.	512 x 8	1024 x 4
1	I_1	I_1	13	O_4	O_2
2	I_0	I_0	14	O_3	O_1
3	CS1	CS1	15	O_2	NC
4	CS2	CS2	16	O_1	NC
5	CS3	CS3	17	V_{SS}	V_{SS}
6	CS4	I_9	18	I_8	I_8
7	V_{GG}	V_{GG}	19	I_7	I_7
8	V_{DD}	V_{DD}	20	I_6	I_6
9	O_8	NC	21	I_5	I_5
10	O_7	NC	22	I_4	I_4
11	O_6	O_4	23	I_3	I_3
12	O_5	O_3	24	I_2	I_2

I	INPUT	NC	NO CONNECTION
O	OUTPUT	CS	CHIP SELECT

custom programmed devices

The TMS 4400 JC/NC series is programmed at the gate-oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate-oxide-removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization – 512 x 8 or 1024 x 4
- memory contents
- chip-select word
- output buffer type

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

input format

Programming information for the TMS 4400 JC/NC will be transmitted to TI in the form of a *deck of 64 standard 80-column computer cards*, accompanied by a listing of these cards. This method eliminates many chances for error and guarantees the fastest delivery schedule of ROMs. Upon receipt of each deck, a computer run will be made and a copy of the computer-generated truth table sent back to the customer. This copy should be checked carefully. If any errors are discovered, TI must be notified immediately so that work can be stopped and the necessary adjustments made.

Information on the various circuit options desired will be transmitted on a special form supplied by TI. A copy of the form is included in this bulletin.

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DATA CARD FORMAT

Column No.

1-2	Punch a right-justified integer for the card number (1-64).
3-6	Punch the ZA identification number supplied by TI MOS Marketing (4 numbers).
7	Blank
8-11	Punch a right-justified integer representing the binary input address for the first set of outputs described on the card.
12	Blank
13-16	Punch a right-justified integer representing the binary input address for the last set of outputs described on the card.
17-80	Punch the desired output data for the range of addresses specified on the card — a "1" for a logical 1 and a "0" for a logical 0.

Input addresses and output data are dependent upon the configuration.

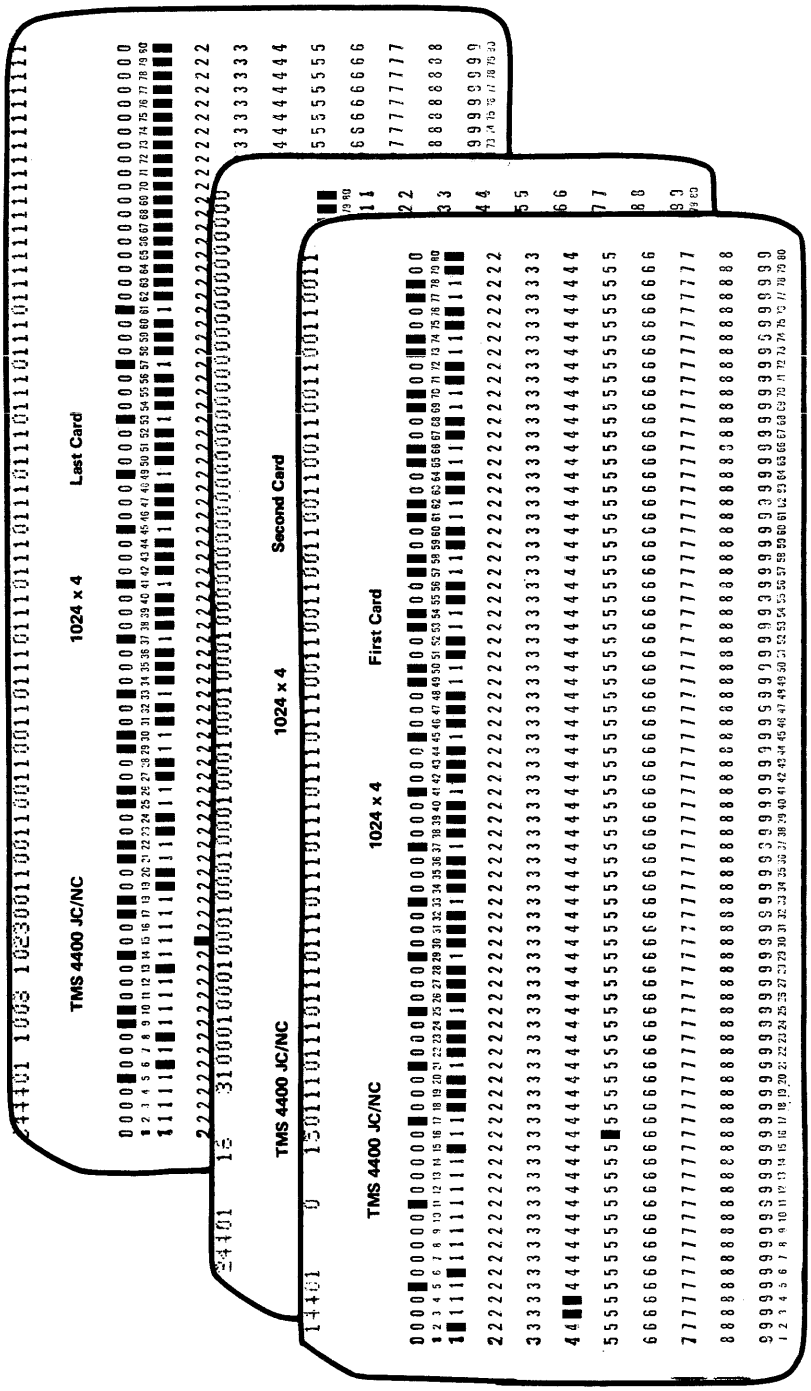
512 Word x 8-Bit Organization

Each card will describe 8 sets of output data. The address words will be sequential from 0 to 511. The output data sets will each be 8 columns long and describe the outputs O_1, O_2, O_3, O_4, O_5, O_6, O_7, and O_8, in that order.

1024 Word x 4-Bit Organization

Each card will describe 16 sets of output data. The address words will be sequential from 0 to 1023. The output data sets will each be 4 columns long and describe the outputs O_1, O_2, O_3 and O_4 in that order.

data cards



TEXAS INSTRUMENTS
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TMS 4400 JC/NC CUSTOM CODING INFORMATION

ZA Identification:_____ Date:_____

Customer _____

Address _____ _____

_____

Customer Part Number:_____

Chip Organization

512 x 8 ☐ (8) 1024 x 4 ☐ (4)

Chip Address

512 x 8

	CS1	CS2	CS3	CS4
Pin Nos.	3	4	5	6

1024 x 4

	CS1	CS2	CS3
Pin Nos.	3	4	5

NOTE: 0 – Logical zero level (negative logic)
1 – Logical one level (negative logic)
X – Do not wish to use

Output Buffer Type

Open Drain, TTL Compatible ☐ (OD)

Push-Pull, MOS Compatible ☐ (PP)

truth table, TMS 4401 JC/NC (sheet 1 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
0	0	1	1	1	64	1	1	1	1	128	1	1	1	1	192	1	1	1	1
1	0	1	1	1	65	0	1	1	1	129	0	1	1	1	193	0	1	1	1
2	0	1	1	1	66	0	1	1	1	130	0	1	1	1	194	0	1	1	1
3	0	1	1	1	67	0	1	1	1	131	0	1	1	1	195	0	1	1	1
4	0	1	1	1	68	0	1	1	1	132	0	1	1	1	196	0	1	1	1
5	0	1	1	1	69	0	1	1	1	133	0	1	1	1	197	0	1	1	1
6	0	1	1	1	70	0	1	1	1	134	0	1	1	1	198	0	1	1	1
7	0	1	1	1	71	0	1	1	1	135	0	1	1	1	199	0	1	1	1
8	0	0	1	1	72	0	0	1	1	136	0	0	1	1	200	0	0	1	1
9	0	0	1	1	73	0	0	1	1	137	0	0	1	1	201	0	0	1	1
10	0	0	1	1	74	0	0	1	1	138	0	0	1	1	202	0	0	1	1
11	0	0	1	1	75	0	0	1	1	139	0	0	1	1	203	0	0	1	1
12	0	0	1	1	76	0	0	1	1	140	0	0	1	1	204	0	0	1	1
13	0	0	1	1	77	0	0	1	1	141	0	0	1	1	205	0	0	1	1
14	0	0	1	1	78	0	0	1	1	142	0	0	1	1	206	0	0	1	1
15	0	0	1	1	79	0	0	1	1	143	0	0	1	1	207	0	0	1	1
16	0	0	0	1	80	0	0	0	1	144	0	0	0	1	208	0	0	0	1
17	0	0	0	1	81	0	0	0	1	145	0	0	0	1	209	0	0	0	1
18	0	0	0	1	82	0	0	0	1	146	0	0	0	1	210	0	0	0	1
19	0	0	0	1	83	0	0	0	1	147	0	0	0	1	211	0	0	0	1
20	0	0	0	1	84	0	0	0	1	148	0	0	0	1	212	0	0	0	1
21	0	0	0	1	85	0	0	0	1	149	0	0	0	1	213	0	0	0	1
22	0	0	0	1	86	0	0	0	1	150	0	0	0	1	214	0	0	0	1
23	0	0	0	1	87	0	0	0	1	151	0	0	0	1	215	0	0	0	1
24	0	0	0	0	88	0	0	0	0	152	0	0	0	0	216	0	0	0	0
25	0	0	0	0	89	0	0	0	0	153	0	0	0	0	217	0	0	0	0
26	0	0	0	0	90	0	0	0	0	154	0	0	0	0	218	0	0	0	0
27	0	0	0	0	91	0	0	0	0	155	0	0	0	0	219	0	0	0	0
28	0	0	0	0	92	0	0	0	0	156	0	0	0	0	220	0	0	0	0
29	0	0	0	0	93	0	0	0	0	157	0	0	0	0	221	0	0	0	0
30	0	0	0	0	94	0	0	0	0	158	0	0	0	0	222	0	0	0	0
31	0	0	0	0	95	0	0	0	0	159	0	0	0	0	223	0	0	0	0
32	0	0	0	0	96	0	0	0	0	160	0	0	0	0	224	0	0	0	0
33	0	0	0	0	97	0	0	0	0	161	0	0	0	0	225	0	0	0	0
34	0	0	0	0	98	0	0	0	0	162	0	0	0	0	226	0	0	0	0
35	0	0	0	0	99	0	0	0	0	163	0	0	0	0	227	0	0	0	0
36	0	0	0	0	100	0	0	0	0	164	0	0	0	0	228	0	0	0	0
37	0	0	0	0	101	0	0	0	0	165	0	0	0	0	229	0	0	0	0
38	0	0	0	0	102	0	0	0	0	166	0	0	0	0	230	0	0	0	0
39	0	0	0	0	103	0	0	0	0	167	0	0	0	0	231	0	0	0	0
40	0	0	0	1	104	0	0	0	1	168	0	0	0	1	232	0	0	0	1
41	0	0	0	1	105	0	0	0	1	169	0	0	0	1	233	0	0	0	1
42	0	0	0	1	106	0	0	0	1	170	0	0	0	1	234	0	0	0	1
43	0	0	0	1	107	0	0	0	1	171	0	0	0	1	235	0	0	0	1
44	0	0	0	1	108	0	0	0	1	172	0	0	0	1	236	0	0	0	1
45	0	0	0	1	109	0	0	0	1	173	0	0	0	1	237	0	0	0	1
46	0	0	0	1	110	0	0	0	1	174	0	0	0	1	238	0	0	0	1
47	0	0	0	1	111	0	0	0	1	175	0	0	0	1	239	0	0	0	1
48	0	0	1	1	112	0	0	1	1	176	0	0	1	1	240	0	0	1	1
49	0	0	1	1	113	0	0	1	1	177	0	0	1	1	241	0	0	1	1
50	0	0	1	1	114	0	0	1	1	178	0	0	1	1	242	0	0	1	1
51	0	0	1	1	115	0	0	1	1	179	0	0	1	1	243	0	0	1	1
52	0	0	1	1	116	0	0	1	1	180	0	0	1	1	244	0	0	1	1
53	0	0	1	1	117	0	0	1	1	181	0	0	1	1	245	0	0	1	1
54	0	0	1	1	118	0	0	1	1	182	0	0	1	1	246	0	0	1	1
55	0	0	1	1	119	0	0	1	1	183	0	0	1	1	247	0	0	1	1
56	0	1	1	1	120	0	1	1	1	184	0	1	1	1	248	0	1	1	1
57	0	1	1	1	121	0	1	1	1	185	0	1	1	1	249	0	1	1	1
58	0	1	1	1	122	0	1	1	1	186	0	1	1	1	250	0	1	1	1
59	0	1	1	1	123	0	1	1	1	187	0	1	1	1	251	0	1	1	1
60	0	1	1	1	124	0	1	1	1	188	0	1	1	1	252	0	1	1	1
61	0	1	1	1	125	0	1	1	1	189	0	1	1	1	253	0	1	1	1
62	0	1	1	1	126	0	1	1	1	190	0	1	1	1	254	0	1	1	1
63	1	1	1	1	127	1	1	1	1	191	1	1	1	1	255	1	1	1	1

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CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

TEXAS INSTRUMENTS
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truth table, TMS 4401 JC/NC (sheet 2 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
256	1	1	1	1	320	1	1	1	1	384	1	1	1	1	448	1	1	1	1
257	1	1	1	1	321	1	1	1	1	385	1	1	1	1	449	1	1	1	1
258	0	1	1	1	322	0	1	1	1	386	1	1	1	1	450	1	1	1	1
259	0	1	1	1	323	0	1	1	1	387	1	1	1	1	451	1	1	1	1
260	0	1	1	1	324	0	1	1	1	388	0	1	1	1	452	0	1	1	1
261	0	1	1	1	325	0	1	1	1	389	0	1	1	1	453	0	1	1	1
262	0	1	1	1	326	0	1	1	1	390	0	1	1	1	454	0	1	1	1
263	0	1	1	1	327	0	1	1	1	391	0	1	1	1	455	0	1	1	1
264	0	1	1	1	328	0	1	1	1	392	0	1	1	1	456	0	1	1	1
265	0	1	1	1	329	0	1	1	1	393	0	1	1	1	457	0	1	1	1
266	0	1	1	1	330	0	1	1	1	393	0	1	1	1	458	0	1	1	1
267	0	1	1	1	331	0	1	1	1	394	0	1	1	1	459	0	1	1	1
268	0	0	1	1	332	0	0	1	1	395	0	1	1	1	460	0	0	1	1
269	0	0	1	1	333	0	0	1	1	396	0	0	1	1	461	0	0	1	1
270	0	0	1	1	334	0	0	1	1	397	0	0	1	1	462	0	0	1	1
271	0	0	1	1	335	0	0	1	1	398	0	0	1	1	463	0	0	1	1
272	0	0	1	1	336	0	0	1	1	399	0	0	1	1	464	0	0	1	1
273	0	0	1	1	337	0	0	1	1	400	0	0	1	1	465	0	0	1	1
274	0	0	1	1	338	0	0	1	1	401	0	0	1	1	466	0	0	1	1
275	0	0	1	1	339	0	0	0	1	402	0	0	1	1	467	0	0	1	1
276	0	0	0	1	340	0	0	0	1	403	0	0	1	1	468	0	0	0	1
277	0	0	0	1	341	0	0	0	1	404	0	0	0	1	469	0	0	0	1
278	0	0	0	1	342	0	0	0	1	405	0	0	0	1	470	0	0	0	1
279	0	0	0	1	343	0	0	0	1	406	0	0	0	1	471	0	0	0	1
280	0	0	0	1	344	0	0	0	1	407	0	0	0	1	472	0	0	0	1
281	0	0	0	1	345	0	0	0	1	408	0	0	0	1	473	0	0	0	1
282	0	0	0	1	346	0	0	0	1	409	0	0	0	1	474	0	0	0	1
283	0	0	0	1	347	0	0	0	1	410	0	0	0	1	475	0	0	0	1
284	0	0	0	0	348	0	0	0	0	411	0	0	0	1	476	0	0	0	0
285	0	0	0	0	349	0	0	0	0	412	0	0	0	0	477	0	0	0	0
286	0	0	0	0	350	0	0	0	0	413	0	0	0	0	478	0	0	0	0
287	0	0	0	0	351	0	0	0	0	414	0	0	0	0	479	0	0	0	0
288	0	0	0	0	352	0	0	0	0	415	0	0	0	0	480	0	0	0	0
289	0	0	0	0	353	0	0	0	0	416	0	0	0	0	481	0	0	0	0
290	0	0	0	0	354	0	0	0	0	417	0	0	0	0	482	0	0	0	0
291	0	0	0	0	355	0	0	0	0	418	0	0	0	0	483	0	0	0	0
292	0	0	0	1	356	0	0	0	1	419	0	0	0	0	484	0	0	0	1
293	0	0	0	1	357	0	0	0	1	420	0	0	0	1	485	0	0	0	1
294	0	0	0	1	358	0	0	0	1	421	0	0	0	1	486	0	0	0	1
295	0	0	0	1	359	0	0	0	1	422	0	0	0	1	487	0	0	0	1
296	0	0	0	1	360	0	0	0	1	423	0	0	0	1	488	0	0	0	1
297	0	0	0	1	361	0	0	0	1	424	0	0	0	1	489	0	0	0	1
298	0	0	0	1	362	0	0	0	1	425	0	0	0	1	490	0	0	0	1
299	0	0	0	1	363	0	0	0	1	426	0	0	0	1	491	0	0	0	1
300	0	0	1	1	364	0	0	1	1	427	0	0	0	1	492	0	0	1	1
301	0	0	1	1	365	0	0	1	1	428	0	0	1	1	493	0	0	1	1
302	0	0	1	1	366	0	0	1	1	429	0	0	1	1	494	0	0	1	1
303	0	0	1	1	367	0	0	1	1	430	0	0	1	1	495	0	0	1	1
304	0	0	1	1	368	0	0	1	1	431	0	0	1	1	496	0	0	1	1
305	0	0	1	1	369	0	0	1	1	432	0	0	1	1	497	0	0	1	1
306	0	0	1	1	370	0	0	1	1	433	0	0	1	1	498	0	0	1	1
307	0	0	1	1	371	0	0	1	1	434	0	0	1	1	499	0	0	1	1
308	0	1	1	1	372	0	1	1	1	435	0	0	1	1	500	0	1	1	1
309	0	1	1	1	373	0	1	1	1	436	0	1	1	1	501	0	1	1	1
310	0	1	1	1	374	0	1	1	1	437	0	1	1	1	502	0	1	1	1
311	0	1	1	1	375	0	1	1	1	438	0	1	1	1	503	0	1	1	1
312	0	1	1	1	376	0	1	1	1	439	0	1	1	1	504	0	1	1	1
313	0	1	1	1	377	0	1	1	1	440	0	1	1	1	505	0	1	1	1
314	0	1	1	1	378	0	1	1	1	441	0	1	1	1	506	0	1	1	1
315	0	1	1	1	379	0	1	1	1	442	0	1	1	1	507	0	1	1	1
316	0	1	1	1	380	0	1	1	1	443	0	1	1	1	508	1	1	1	1
317	0	1	1	1	381	0	1	1	1	444	1	1	1	1	509	1	1	1	1
318	1	1	1	1	382	1	1	1	1	445	1	1	1	1	510	1	1	1	1
319	1	1	1	1	383	1	1	1	1	446	1	1	1	1	511	1	1	1	1

CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

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truth table, TMS 4401 JC/NC (sheet 3 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
512	1	1	1	1	576	1	1	1	1	640	1	1	1	1	704	1	1	1	1
513	1	1	1	1	577	1	1	1	1	641	1	1	1	1	705	1	1	1	1
514	1	1	1	1	578	1	1	1	1	642	1	1	1	1	706	1	1	1	1
515	1	1	1	1	579	1	1	1	1	643	1	1	1	1	707	1	1	1	1
516	1	1	1	1	580	1	1	1	1	644	1	1	1	1	708	1	1	1	1
517	1	1	1	1	581	1	1	1	1	645	1	1	1	1	709	1	1	1	1
518	1	1	1	1	582	1	1	1	1	646	1	1	1	1	710	1	1	1	1
519	1	1	1	1	583	1	1	1	1	647	1	1	1	1	711	1	1	1	1
520	0	1	1	1	584	0	1	1	1	648	0	1	1	1	712	0	1	1	1
521	0	1	1	1	585	0	1	1	1	649	0	1	1	1	713	0	1	1	1
522	0	1	1	1	586	0	1	1	1	650	0	1	1	1	714	0	1	1	1
523	0	1	1	1	587	0	1	1	1	651	0	1	1	1	715	0	1	1	1
524	0	1	1	1	588	0	1	1	1	652	0	1	1	1	716	0	1	1	1
525	0	1	1	1	589	0	1	1	1	653	0	1	1	1	717	0	1	1	1
526	0	1	1	1	590	0	1	1	1	654	0	1	1	1	718	0	1	1	1
527	0	1	1	1	591	0	1	1	1	655	0	1	1	1	719	0	1	1	1
528	0	0	1	1	592	0	1	1	1	656	0	0	1	1	720	0	0	1	1
529	0	0	1	1	593	0	0	1	1	657	0	0	1	1	721	0	0	1	1
530	0	0	1	1	594	0	0	1	1	658	0	0	1	1	722	0	0	1	1
531	0	0	1	1	595	0	0	1	1	659	0	0	1	1	723	0	0	1	1
532	0	0	1	1	596	0	0	1	1	660	0	0	1	1	724	0	0	1	1
533	0	0	1	1	597	0	0	1	1	661	0	0	1	1	725	0	0	1	1
534	0	0	1	1	598	0	0	1	1	662	0	0	1	1	726	0	0	1	1
535	0	0	1	1	599	0	0	1	1	663	0	0	1	1	727	0	0	1	1
536	0	0	0	1	600	0	0	0	1	664	0	0	0	1	728	0	0	0	1
537	0	0	0	1	601	0	0	0	1	665	0	0	0	1	729	0	0	0	1
538	0	0	0	1	602	0	0	0	1	666	0	0	0	1	730	0	0	0	1
539	0	0	0	1	603	0	0	0	1	667	0	0	0	1	731	0	0	0	1
540	0	0	0	1	604	0	0	0	1	668	0	0	0	1	732	0	0	0	1
541	0	0	0	1	605	0	0	0	1	669	0	0	0	1	733	0	0	0	1
542	0	0	0	1	606	0	0	0	1	670	0	0	0	0	734	0	0	0	0
543	0	0	0	1	607	0	0	0	1	671	0	0	0	0	735	0	0	0	0
544	0	0	0	1	608	0	0	0	0	672	0	0	0	0	736	0	0	0	0
545	0	0	0	1	609	0	0	0	1	673	0	0	0	0	737	0	0	0	0
546	0	0	0	1	610	0	0	0	1	674	0	0	0	1	738	0	0	0	1
547	0	0	0	1	611	0	0	0	1	675	0	0	0	1	739	0	0	0	1
548	0	0	0	1	612	0	0	0	1	676	0	0	0	1	740	0	0	0	1
549	0	0	0	1	613	0	0	0	1	677	0	0	0	1	741	0	0	0	1
550	0	0	0	1	614	0	0	0	1	678	0	0	0	1	742	0	0	0	1
551	0	0	0	1	615	0	0	0	1	679	0	0	0	1	743	0	0	0	1
552	0	0	1	1	616	0	0	1	1	680	0	0	1	1	744	0	0	1	1
553	0	0	1	1	617	0	0	1	1	681	0	0	1	1	745	0	0	1	1
554	0	0	1	1	618	0	0	1	1	682	0	0	1	1	746	0	0	1	1
555	0	0	1	1	619	0	0	1	1	683	0	0	1	1	747	0	0	1	1
556	0	0	1	1	620	0	0	1	1	684	0	0	1	1	748	0	0	1	1
557	0	0	1	1	621	0	0	1	1	685	0	0	1	1	749	0	0	1	1
558	0	0	1	1	622	0	0	1	1	686	0	0	1	1	750	0	0	1	1
559	0	0	1	1	623	0	0	1	1	687	0	0	1	1	751	0	0	1	1
560	0	1	1	1	624	0	1	1	1	688	0	1	1	1	752	0	1	1	1
561	0	1	1	1	625	0	1	1	1	689	0	1	1	1	753	0	1	1	1
562	0	1	1	1	626	0	1	1	1	690	0	1	1	1	754	0	1	1	1
563	0	1	1	1	627	0	1	1	1	691	0	1	1	1	755	0	1	1	1
564	0	1	1	1	628	0	1	1	1	692	0	1	1	1	756	0	1	1	1
565	0	1	1	1	629	0	1	1	1	693	0	1	1	1	757	0	1	1	1
566	0	1	1	1	630	0	1	1	1	694	0	1	1	1	758	0	1	1	1
567	0	1	1	1	631	0	1	1	1	695	0	1	1	1	759	0	1	1	1
568	1	1	1	1	632	1	1	1	1	696	1	1	1	1	760	1	1	1	1
569	1	1	1	1	633	1	1	1	1	697	1	1	1	1	761	1	1	1	1
570	1	1	1	1	634	1	1	1	1	698	1	1	1	1	762	1	1	1	1
571	1	1	1	1	635	1	1	1	1	699	1	1	1	1	763	1	1	1	1
572	1	1	1	1	636	1	1	1	1	700	1	1	1	1	764	1	1	1	1
573	1	1	1	1	637	1	1	1	1	701	1	1	1	1	765	1	1	1	1
574	1	1	1	1	638	1	1	1	1	702	1	1	1	1	766	1	1	1	1
575	1	1	1	0	639	1	1	1	1	703	1	1	1	1	767	1	1	1	1

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CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

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truth table, TMS 4401 JC/NC (sheet 4 of 4)

ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4	ADDRESS NO.	OUTPUTS 1	2	3	4
768	1	1	1	1	832	1	1	1	1	896	1	1	1	1	960	1	1	1	1
769	1	1	1	1	833	1	1	1	1	897	1	1	1	1	961	1	1	1	1
770	1	1	1	1	834	1	1	1	1	898	1	1	1	1	962	1	1	1	1
771	1	1	1	1	835	0	1	1	1	899	1	1	1	1	963	1	1	1	1
772	0	1	1	1	836	0	1	1	1	900	0	1	1	1	964	0	1	1	1
773	0	1	1	1	837	0	1	1	1	901	0	1	1	1	965	0	1	1	1
774	0	1	1	1	838	0	1	1	1	902	0	1	1	1	966	0	1	1	1
775	0	1	1	1	839	0	1	1	1	903	0	1	1	1	967	0	1	1	1
776	0	1	1	1	840	0	1	1	1	904	0	1	1	1	968	0	1	1	1
777	0	1	1	1	841	0	1	1	1	905	0	1	1	1	969	0	1	1	1
778	0	1	1	1	842	0	1	1	1	906	0	1	1	1	970	0	1	1	1
779	0	1	1	1	843	0	1	1	1	907	0	1	1	1	971	0	1	1	1
780	0	0	1	1	844	0	0	1	1	908	0	0	1	1	972	0	0	1	1
781	0	0	1	1	845	0	0	1	1	909	0	0	1	1	973	0	0	1	1
782	0	0	1	1	846	0	0	1	1	910	0	0	1	1	974	0	0	1	1
783	0	0	1	1	847	0	0	1	1	911	0	0	1	1	975	0	0	1	1
784	0	0	1	1	848	0	0	1	1	912	0	0	1	1	976	0	0	1	1
785	0	0	1	1	849	0	0	1	1	913	0	0	1	1	977	0	0	1	1
786	0	0	1	1	850	0	0	1	1	914	0	0	1	1	978	0	0	1	1
787	0	0	1	1	851	0	0	1	1	915	0	0	1	1	979	0	0	1	1
788	0	0	0	1	852	0	0	0	1	916	0	0	0	1	980	0	0	0	1
789	0	0	0	1	853	0	0	0	1	917	0	0	0	1	981	0	0	0	1
790	0	0	0	1	854	0	0	0	1	918	0	0	0	1	982	0	0	0	1
791	0	0	0	1	855	0	0	0	1	919	0	0	0	1	983	0	0	0	1
792	0	0	0	1	856	0	0	0	1	920	0	0	0	1	984	0	0	0	1
793	0	0	0	1	857	0	0	0	1	921	0	0	0	1	985	0	0	0	1
794	0	0	0	1	858	0	0	0	1	922	0	0	0	1	986	0	0	0	1
795	0	0	0	1	859	0	0	0	1	923	0	0	0	1	987	0	0	0	1
796	0	0	0	0	860	0	0	0	0	924	0	0	0	0	988	0	0	0	0
797	0	0	0	0	861	0	0	0	0	925	0	0	0	0	989	0	0	0	0
798	0	0	0	0	862	0	0	0	0	926	0	0	0	0	990	0	0	0	0
799	0	0	0	0	863	0	0	0	0	927	0	0	0	0	991	0	0	0	0
800	0	0	0	0	864	0	0	0	0	928	0	0	0	0	992	0	0	0	0
801	0	0	0	0	865	0	0	0	0	929	0	0	0	0	993	0	0	0	0
802	0	0	0	0	866	0	0	0	0	930	0	0	0	0	994	0	0	0	0
803	0	0	0	0	867	0	0	0	0	931	0	0	0	0	995	0	0	0	0
804	0	0	0	1	868	0	0	0	1	932	0	0	0	1	996	0	0	0	1
805	0	0	0	1	869	0	0	0	1	933	0	0	0	1	997	0	0	0	1
806	0	0	0	1	870	0	0	0	1	934	0	0	0	1	998	0	0	0	1
807	0	0	0	1	871	0	0	0	1	935	0	0	0	1	999	0	0	0	1
808	0	0	0	1	872	0	0	0	1	936	0	0	0	1	1000	0	0	0	1
809	0	0	0	1	873	0	0	0	1	937	0	0	0	1	1001	0	0	0	1
810	0	0	0	1	874	0	0	0	1	938	0	0	0	1	1002	0	0	0	1
811	0	0	0	1	875	0	0	0	1	939	0	0	0	1	1003	0	0	0	1
812	0	0	1	1	876	0	0	1	1	940	0	0	1	1	1004	0	0	1	1
813	0	0	1	1	877	0	0	1	1	941	0	0	1	1	1005	0	0	1	1
814	0	0	1	1	878	0	0	1	1	942	0	0	1	1	1006	0	0	1	1
815	0	0	1	1	879	0	0	1	1	943	0	0	1	1	1007	0	0	1	1
816	0	0	1	1	880	0	0	1	1	944	0	0	1	1	1008	0	0	1	1
817	0	0	1	1	881	0	0	1	1	945	0	0	1	1	1009	0	0	1	1
818	0	0	1	1	882	0	0	1	1	946	0	0	1	1	1010	0	0	1	1
819	0	0	1	1	883	0	0	1	1	947	0	0	1	1	1011	0	0	1	1
820	0	1	1	1	884	0	1	1	1	948	0	1	1	1	1012	0	1	1	1
821	0	1	1	1	885	0	1	1	1	949	0	1	1	1	1013	0	1	1	1
822	0	1	1	1	886	0	1	1	1	950	0	1	1	1	1014	0	1	1	1
823	0	1	1	1	887	0	1	1	1	951	0	1	1	1	1015	0	1	1	1
824	0	1	1	1	888	0	1	1	1	952	0	1	1	1	1016	0	1	1	1
825	0	1	1	1	889	0	1	1	1	953	0	1	1	1	1017	0	1	1	1
826	0	1	1	1	890	0	1	1	1	954	0	1	1	1	1018	0	1	1	1
827	0	1	1	1	891	0	1	1	1	955	0	1	1	1	1019	0	1	1	1
828	1	1	1	1	892	1	1	1	1	956	1	1	1	1	1020	1	1	1	1
829	1	1	1	1	893	1	1	1	1	957	1	1	1	1	1021	1	1	1	1
830	1	1	1	1	894	1	1	1	1	958	1	1	1	1	1022	1	1	1	1
831	1	1	1	1	895	1	1	1	1	959	1	1	1	1	1023	1	1	1	1

CS1 = 1 CS2 = 1 CS3 = 1 push-pull outputs

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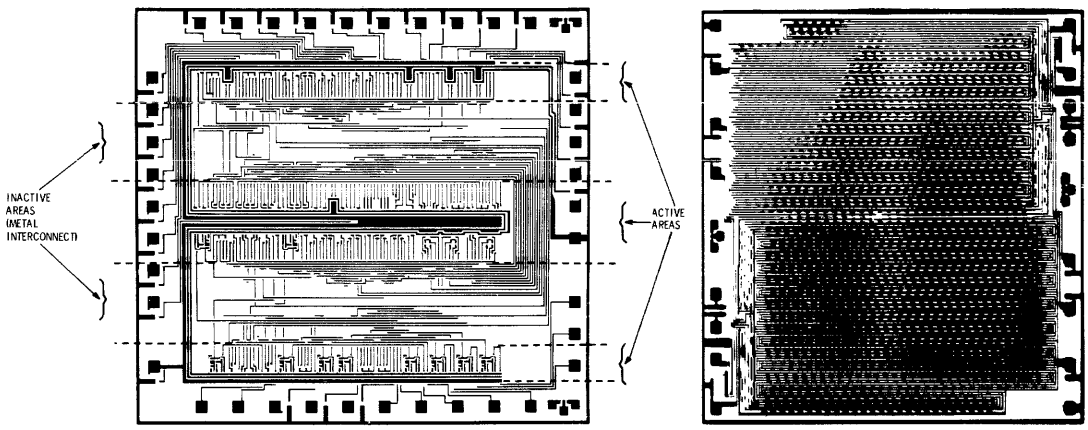
Programmable logic arrays represent an economical and efficient method to implement random logic using programmable techniques. "Random Logic" means a logic circuit that is not strongly structured, as opposed to circuits such as shift registers, read-only memories, etc. When a random-logic circuit is implemented in MOS, a large part of the chip area is used for interconnection between the cells, as can be seen from the pictures below. This area is essentially wasted.

Random-Logic Chip **Shift-Register Chip**



1) Some Economics

A customer who wants to build a random-logic circuit can choose any of three approaches: bipolar, relatively low-complexity integrated circuits; a custom MOS circuit; a programmable MOS circuit (such as a read-only memory or a PLA).

A custom MOS circuit will be designed from scratch. The customer's logic will be implemented on a piece of silicon. TI will reduce the size of the chip as much as possible, but there will still be a large inactive area for interconnections. With the programmable approach, TI starts with a circuit that is already designed. In order to program the device, only one photomask is modified and this is accomplished easily and economically.

2) PLA Structure

The PLA structure is extremely simple. Any logic equation can be written as a sum of products or as a product of sums, and that is exactly what has been implemented on the array.

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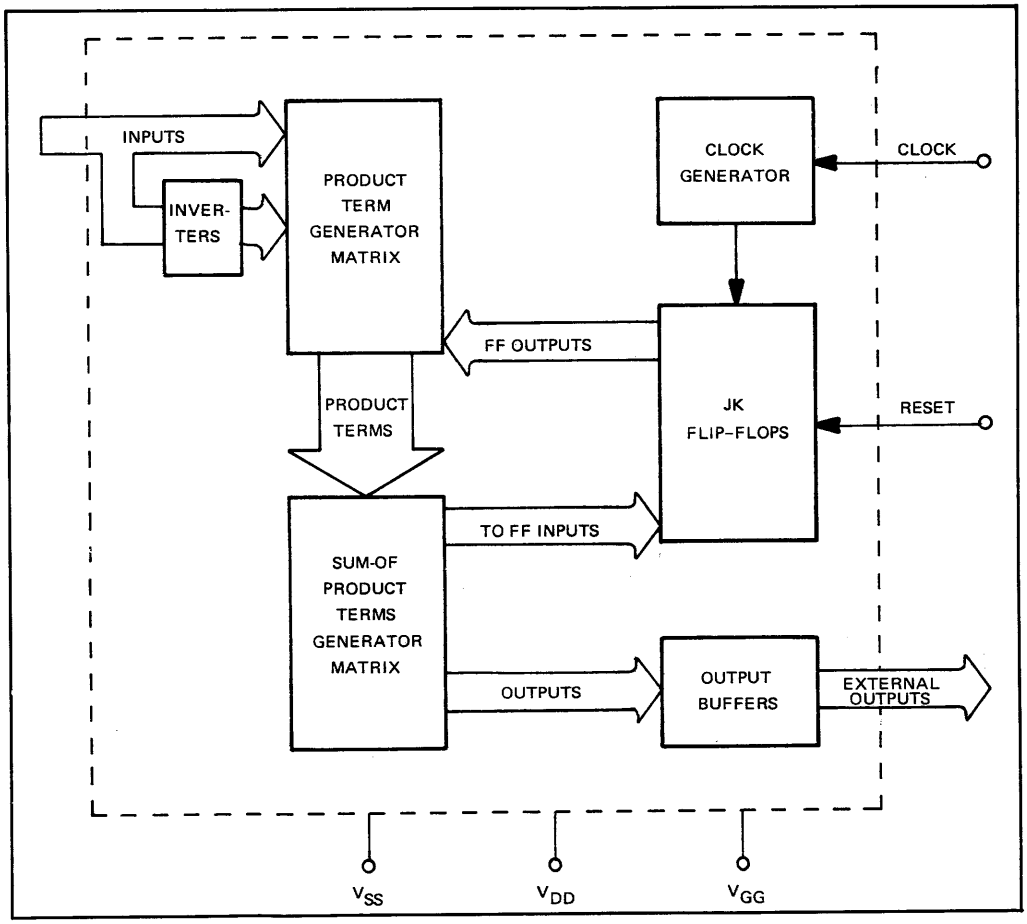
The logic expression is written as a sum of products:

- A first programmable matrix generates the products terms (AND matrix)
- A second programmable matrix generates the sum of products (OR matrix)
- Flip-flops are used in feedback loops to permit implementation of sequential logic.



a) **AND Matrix**

The role of the AND matrix is to form the product terms of the input terms, and their complements.

The number of product terms has been arrived at by heuristic methods. We have set a limit of 60 product terms for the TMS 2000 JC, and 72 for the TMS 2200 JC.

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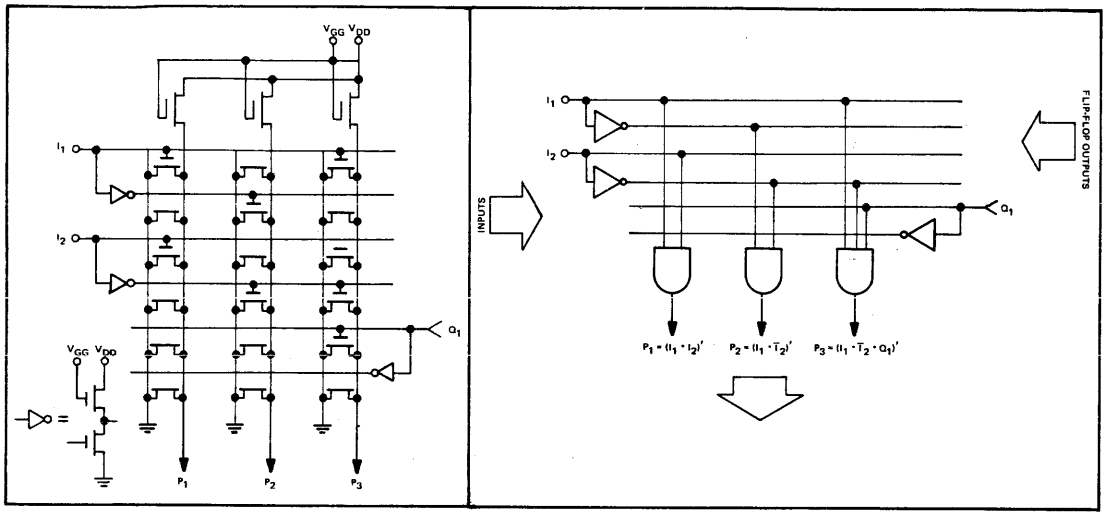
PLA 'AND' MATRIX

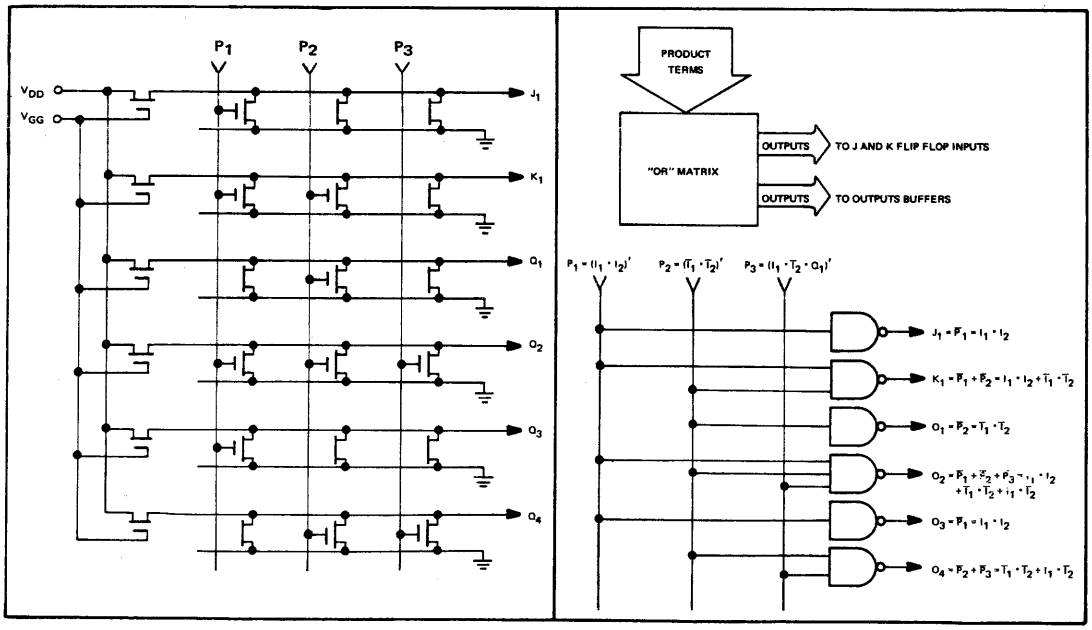
LOGIC EQUIVALENT OF PLA 'AND' MATRIX



b) OR Matrix (Sum of Products)

PLA 'OR' MATRIX

LOGIC EQUIVALENT OF PLA 'OR' MATRIX



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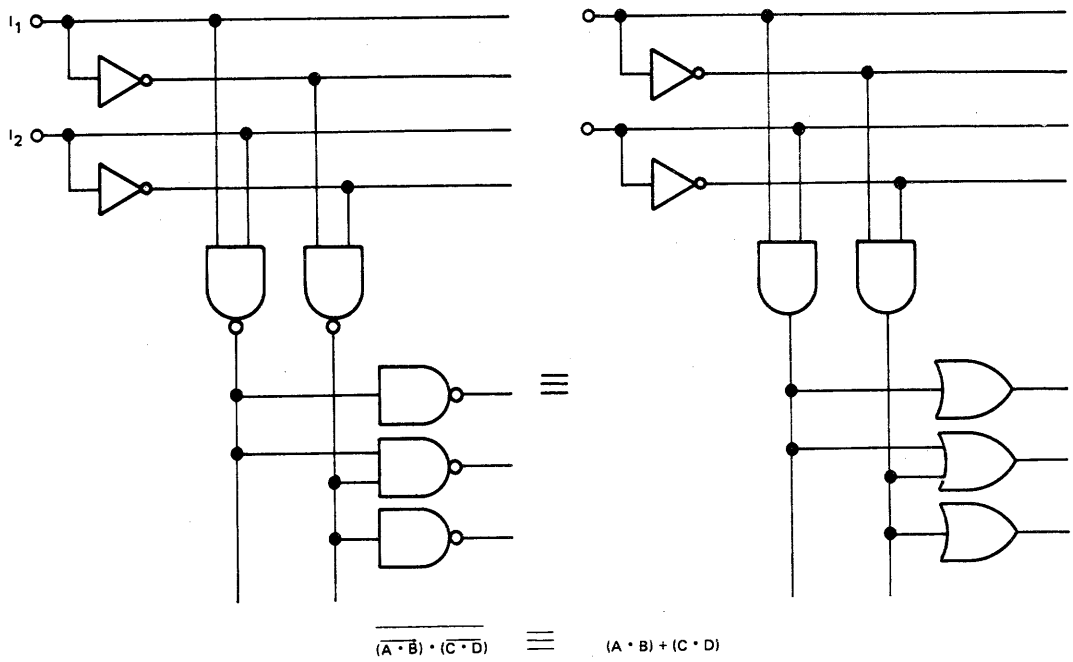
The AND matrix feeds into the OR matrix. The OR matrix generates sums of product terms. Some of the outputs of the OR matrix are fed to the outside while others are fed back to the first matrix (AND) through flip-flops.

Both matrices are programmable. A product term can be of as many of the inputs and their complements as the designer wants. By this same token a sum of product terms can be of as many of the products as the designer wishes.

LOGIC EQUIVALENT OF PLA ORGANIZATION



c) Feedback Loops, Flip-Flops

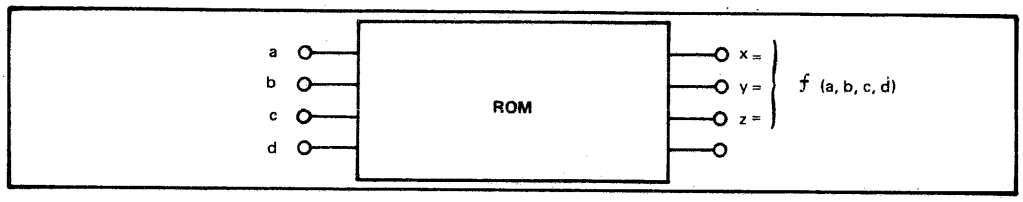
In order to implement sequential logic, feedback loops are necessary. These feedback loops must be timed. If we fed back directly the outputs of this second matrix (OR matrix) to the inputs of the first matrix (AND), a race condition could develop. We use one JK master-slave flip-flop per feedback loop to take care of this timing. We are able to reset all these flip-flops to initialize the logic. The designer is free to choose which and how many outputs are fed back to the first matrix.

3) PLA versus ROM

A PLA is actually a big Read Only Memory with a non-exhaustive decode section that has been adapted to the implementation of random logic. How does a PLA differ from a ROM and what are the advantages?

a) Combinational Logic

Combinational logic is easily implemented on a read-only memory. The truth table is written in such a way that the outputs are logic functions of the inputs.



The main drawback to this scheme is that every time an input variable is added, the size of the ROM is doubled. This is because the decode scheme of the read-only memory is exhaustive. All the product terms are generated, and that soon becomes prohibitive. To do what our PLA TMS 2000 JC does through straight read-only-memory techniques would take 2^{25} words (17 external inputs and 8 inputs from the flip-flops), that is 8,288,608 words of 26 bits (18 external outputs and 8 feedback loops) – or a total capacity of 218,103,808 bits which is a ludicrous size for any read-only memory.

In a PLA all the product terms are not generated. TI has set the limit at 60 product terms for the TMS 2000 JC and to 72 for the TMS 2200 JC. These numbers have been arrived at through heuristic methods and have proven to be sufficiently large. It is not often that an equation is presented with 60 terms, each one being a product of up to 25 variables.

b) Sequential Logic

To perform sequential logic with a read-only memory, the outputs must be fed back to the inputs through a gating arrangement.

This is comparatively easy to do but has drawbacks:

- For each feedback loop two package pins are wasted.
- The gating arrangement has to be provided.
- Initialization of the logic is difficult.

In the PLAs the feedback loops are never brought outside, which saves a number of pins. The initialization is easy because JK flip-flops are used.

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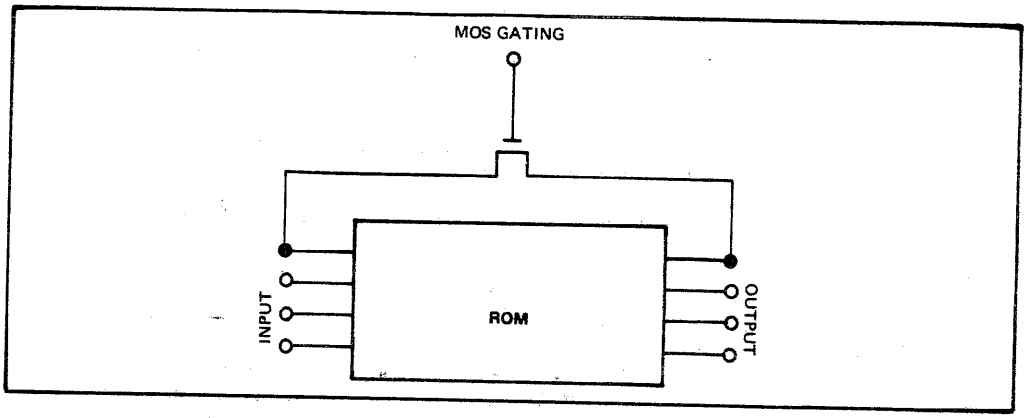
ROM CONNECTED TO PERFORM SEQUENTIAL LOGIC



4) **Catalog PLAs**

TI presently markets two catalog PLAs:

TMS 2000 JC	TMS 2200 JC
40 pins	28 pins
17 external inputs	13 external inputs
18 outputs	10 outputs
8 flip-flops	10 flip-flops
60 product terms	72 product terms

These devices are produced using silicon nitride technology, which permits easy interface with TTL/DTL.

5) **Design Considerations**

a) **Logic Design**

Logic design with PLAs is easy. With the PLA approach the designer writes down the logic equations of each of the outputs in terms of the external inputs and feedback inputs.

Once this is done the programming of the matrices is handled by a computer program. A SOFTWARE PACKAGE bulletin describes in detail the mechanical aspects of the operation.

b) **Design Efficiency**

The PLA is an extremely powerful tool. The designer must be careful to use as fully as possible the capability of the PLAs. To help him do that TI has published a SOFTWARE PACKAGE bulletin and application report which includes design considerations. The PLA technique is extremely efficient from a silicon real-estate point of view.

TMS 2000 JC, NC; TMS 2200 JC, NC
PROGRAMMABLE LOGIC ARRAYS

features

- Low-threshold MOS/bipolar technology
- Static operation
- Push-pull or single-ended output buffers
- Optional internal MOS pull-up resistor on inputs
- TTL compatible
- CDIP or plastic package

description

The programmable logic array (PLA) is a device that is programmable by gate-oxide mask. It is used to perform sequential and combinational logic.

The TMS 2000 JC/NC and TMS 2200 JC/NC series are groups of programmable logic arrays manufactured using P-channel enhancement-mode low-threshold MOS and NPN bipolar techniques.

A PLA is a unique combination of master-slave JK flip-flops and static read-only memories on a single MOS/LSI chip. The programmable logic arrays have been designed to permit the implementation of custom random logic with the same low cost and quick turnaround provided by a read-only memory. Sequential and combinational logic may be implemented in a PLA. The logic is described in the form of Boolean equations, which are converted by TI software routines into the gate-oxide mask.

In the TMS 2000 JC/NC seventeen external inputs and the eight flip-flop outputs are combined by a product term generator into 60 product terms. These are then combined by a sum-of-product-terms generator into 16 lines for the 8J and 8 K inputs to the 8 JK master-slave flip-flops and into 18 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

In the TMS 2200 JC/NC thirteen external inputs and the ten flip-flop outputs are combined by a product term generator into 72 product terms. These are then combined by a sum-of-product-terms generator into 20 lines for the 10 J and 10 K inputs to the 10 JK master-slave flip-flops and into 10 external outputs. The flip-flop operation is controlled by a common reset input and a single clock.

The device inputs have optional internal pull-up resistors for easy interface. The output buffers incorporate bipolar NPN transistors and either push-pull or open-ended buffers may be chosen. These features facilitate interfacing the PLAs in TTL systems.

The PLAs are designated TMS 2000 JC and TMS 2200 JC when mounted in hermetically sealed ceramic dual-in-line packages. In dual-in-line plastic packages the units are numbered TMS 2000 NC and TMS 2200 NC.

organization

	TMS 2000 JC/NC	TMS 2200 JC/NC
Number of product terms	60	72
Number of external inputs	17	13
Number of external outputs	18	10
Number of JK flip-flops	8	10

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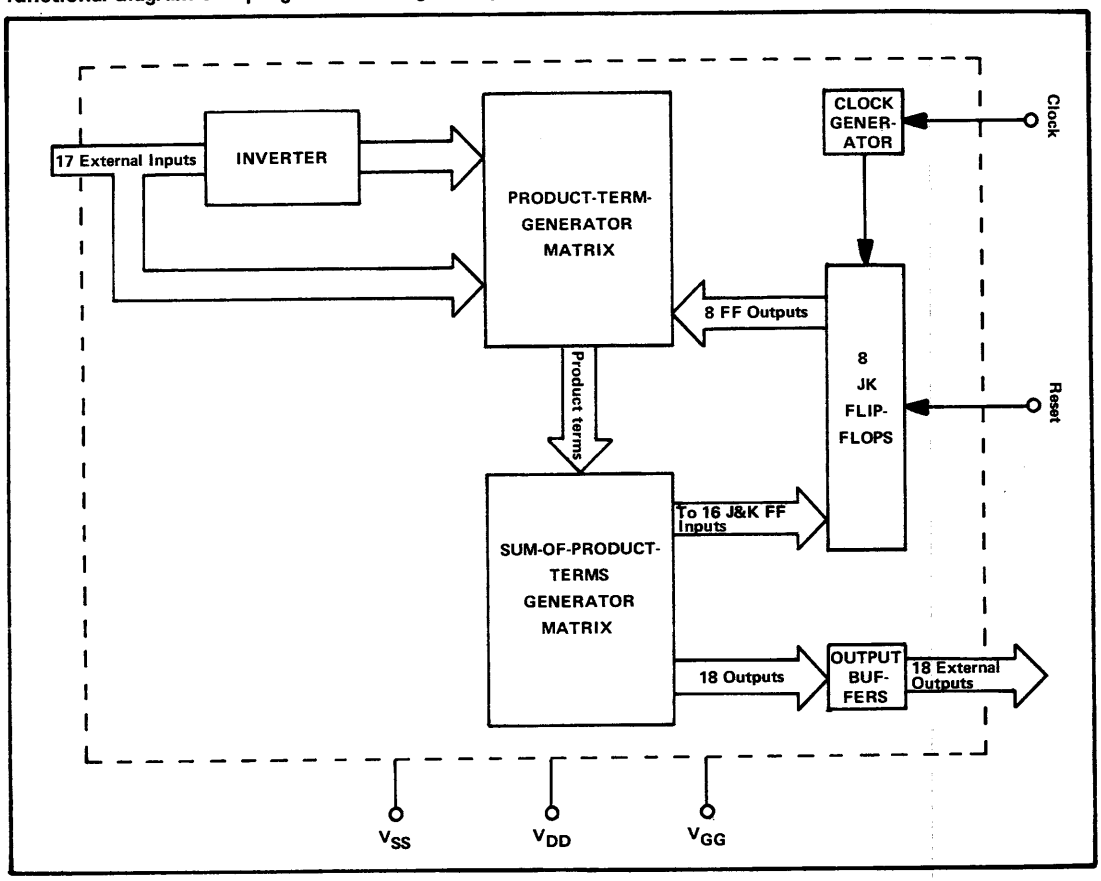
functional diagram of a programmable logic array (TMS 2000 JC/NC)



operation

1) Input

The present external inputs and the previous flip-flop outputs control the state of the internal flip-flops.

2) Internal

Data is entered into the master flip-flop during the positive edge of the clock inputs, while the slave flip-flop is set during the negative edge.

The flip-flops may be reset at any time by applying a low voltage on the reset input. However, if the reset input is taken high while the clock is high, an indeterminate flip-flop state may result.

3) Output

The external outputs can be a function of the present inputs or the present flip-flop outputs, or a function of both.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See note) . . . . . −15 V to 0.3 V
Supply voltage V_{GG} range (See note) . . . . . −25 V to 0.3 V
Clock and data input voltage ranges (See note) . . . . . −15 V to 0.3 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C
Power dissipation . . . . . 300 mW

NOTE: These voltage values are with respect to V_{SS}.

logic definition

Positive logic is assumed.

a) Logic 1 = most positive voltage

b) Logic 0 = most negative voltage

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{DD}	−4.7	−10	−11	V
Supply voltage V_{GG}	−15	−17	−18.5	V
$V_{in(0)}$ with internal resistor (TTL)	−4	−5	−5.25	V
$V_{in(1)}$ with internal resistor (TTL)	0	−5	−1.5	V
$V_{in(0)}$ without internal resistor (MOS)	−4	−5	−11	V
$V_{in(1)}$ without internal resistor (MOS)	+0.3	−0.5	−1.5	V

NOTE: All voltages are with respect to V_{SS}.

The design of the unit permits a broad range of operations that allows the user to take advantage of readily available power supplies (e.g., +5 V, −5 V, −12 V).

electrical characteristics at nominal operating conditions and 25°C

PARAMETER		TEST CONDITIONS†	MIN	NOM	MAX	UNITS
$V_{out(1)}$	Logical 1 output voltage	R_L = 10 kΩ to V_{DD} (See Note 1)	0	−0.7	−1.0	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 10 kΩ to V_{SS} (See Note 1)	−8	−9	−10	V
$V_{out(1)}$	Logical 1 output voltage	R_L = 6.8 kΩ to V_{GG} (Note 2)	0	−1.0	−1.5	V
$V_{out(0)}$	Logical 0 output voltage	R_L = 6.8 kΩ to V_{GG} (Note 1)	−10	−11	−17	V
$I_{in(0)}$	Input leakage current	V_{IN} = −10 V (See Note 3)			−1.0	μA
$I_{in(0)}$	With internal resistor (TTL)		−0.8	−0.9	−1.1	mA
$I_{in(1)}$	With internal resistor (TTL)		0	−40	−125	μA

† Unless otherwise noted, R_L = 10 kΩ to V_{SS}.

NOTES: 1. Push-pull output buffers used
2. Single-ended output buffer used
3. Optional input resistors not used

— continued

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electrical characteristics at nominal operating conditions and 25°C (continued)

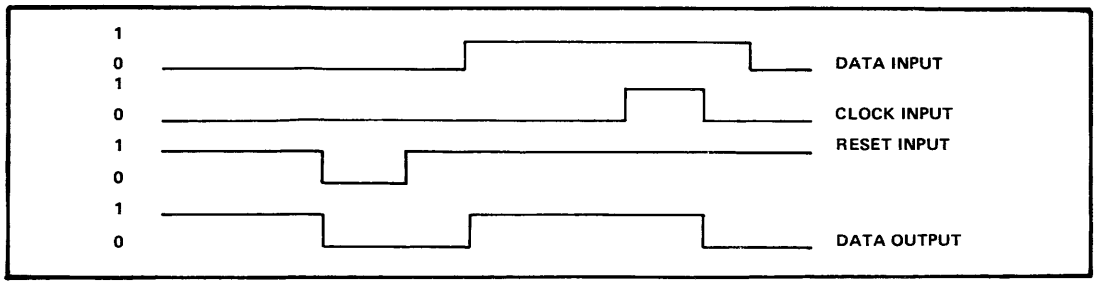
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNITS
R_{in}	Input impedance	V_{IN} = 0 V to −10 V (Note 4)	5	7	12	kΩ
C_{in}	Input Capacitance	V_{IN} = 0, f = 1 MHz		3	5	pF
I_{DD}	Supply current into V_{DD} terminal			18	25	mA
I_{GG}	Supply current into V_{GG} terminal			1.0	4.0	mA
I_{GG}	Supply current into V_{GG} terminal	(See Note 5)		15	20	mA

NOTES: 4. Optional input resistors used
5. All outputs at logic 1

switching characteristics at nominal operating conditions and 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{p(data)}$	Width of data pulse	C_L = 30 pF, R_L = 1 MΩ	2.0			μs
$t_{p(clock)}$	Width of clock pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
$t_{p(reset)}$	Width of reset pulse	C_L = 30 pF, R_L = 1 MΩ	0.5			μs
f	Clock repetition rate	C_L = 30 pF, R_L = 1 MΩ	0		200	kHz
t_{di}	Propagation delay time from input to output with no clock	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{dr}	Propagation delay time from reset input to a change in external output	C_L = 30 pF, R_L = 1 MΩ		1.1	1.4 (25°C) 1.9 (85°C)	μs μs
t_{df}	Propagation delay time from clock input to a change in external output	C_L = 30 pF, R_L = 1 MΩ	0.9	1.1	1.4 (25°C) 2.1 (85°C)	μs μs
t_{db}	Delay time required between data input and positive edge of clock	C_L = 30 pF, R_L = 1 MΩ	1.9			μs
t_{da}	Input hold time after negative edge of clock	C = 30 pF, R_L = 1 MΩ	0.1			μs
t_{or}	Output rise time (single-ended output)	6.8 kΩ to V_{GG}	20	60	200	ns
t_{of}	Output fall time (single-ended output)	6.8 kΩ to V_{GG}	100	250	350	ns
t_{or}	Output rise time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	20	60	200	ns
t_{of}	Output fall time (push-pull output)	C_L = 30 pF, R_L = 1 MΩ	100	200	300	ns

timing diagram



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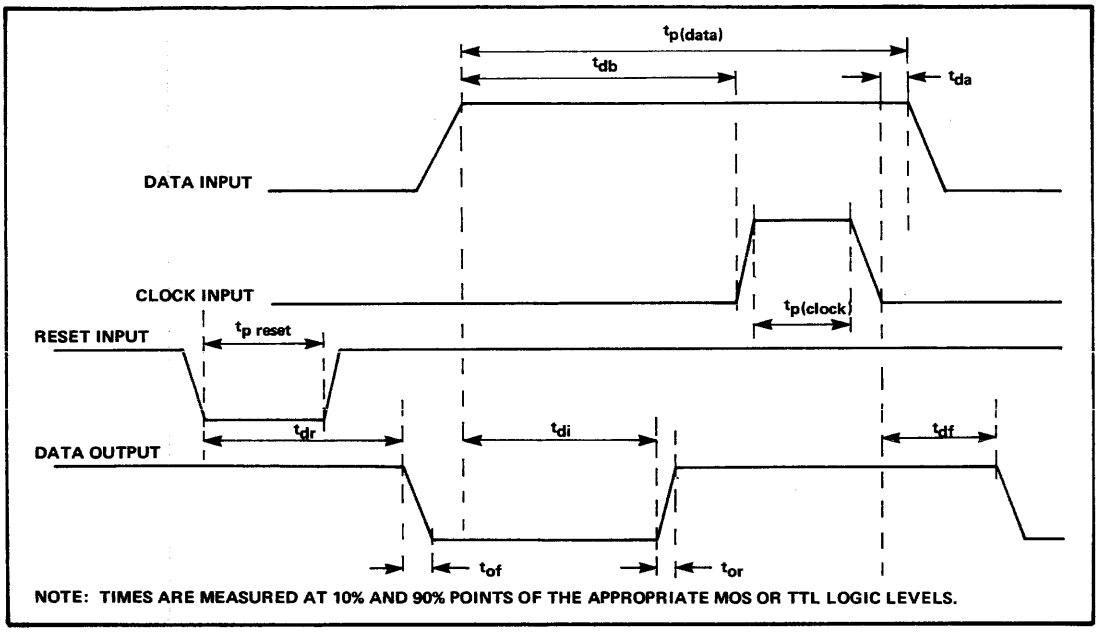
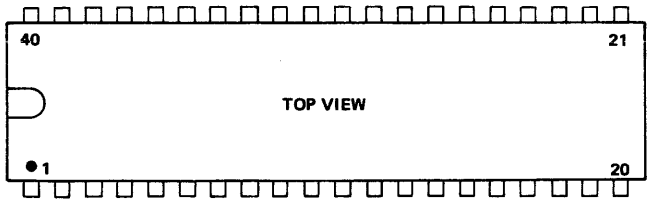
voltage waveforms



NOTE: TIMES ARE MEASURED AT 10% AND 90% POINTS OF THE APPROPRIATE MOS OR TTL LOGIC LEVELS.

pin configuration — TMS 2000 JC/NC

"TMS 2000 JC" is the part number for a unit mounted in a 40-pin hermetically sealed dual-in-line package. Mounted in a 40-pin dual-in-line plastic package, the unit is designated TMS 2000 NC.



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	11	O_{10}	21	RESET	31	I_{10}
2	O_1	12	O_{11}	22	I_1	32	I_{11}
3	O_2	13	O_{12}	23	I_2	33	I_{12}
4	O_3	14	O_{13}	24	I_3	34	I_{13}
5	O_4	15	O_{14}	25	I_4	35	I_{14}
6	O_5	16	O_{15}	26	I_5	36	I_{15}
7	O_6	17	O_{16}	27	I_6	37	I_{16}
8	O_7	18	O_{17}	28	I_7	38	I_{17}
9	O_8	19	O_{18}	29	I_8	39	CLOCK
10	O_9	20	V_{SS}	30	I_9	40	V_{GG}

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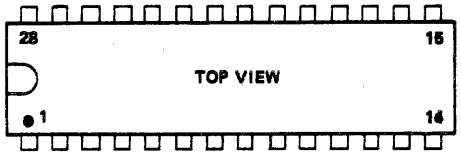
mechanical data and pin configuration — TMS 2200 JC/NC

"TMS 2200 JC" is the part number for this device mounted in a 28-pin hermetically sealed ceramic dual-in-line package. Mounted in a 28-pin dual-in-line plastic package, the unit is designated TMS 2200 NC. The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	V_{DD}	8	O_6	15	I_1	22	I_8
2	V_{GG}	9	O_7	16	I_2	23	I_9
3	O_1	10	O_8	17	I_3	24	I_{10}
4	O_2	11	O_9	18	I_4	25	I_{11}
5	O_3	12	O_{10}	19	I_5	26	I_{12}
6	O_4	13	V_{SS}	20	I_6	27	I_{13}
7	O_5	14	RESET	21	I_7	28	CLOCK

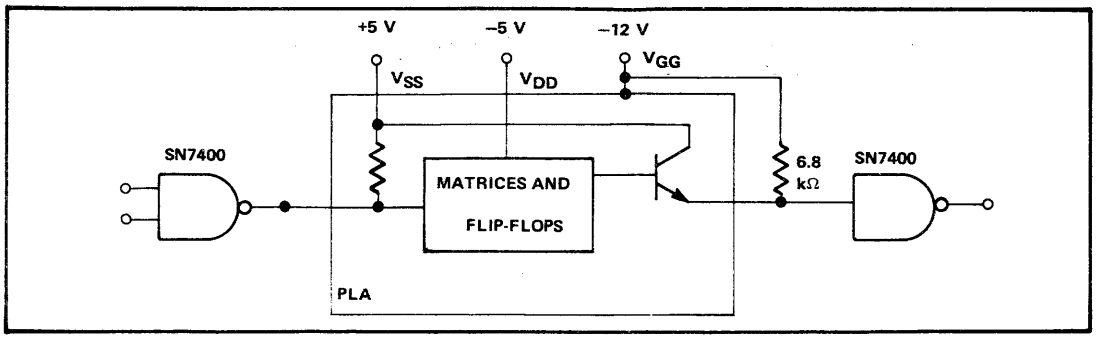
interfacing

a) To TTL system

Each external input of the PLA has an optional internal MOS pull-up resistor available for interfacing with TTL. With V_{SS} at +5 volts, this internal resistor serves to pull up a logic 1 from the TTL specified level of 2.4 V to V_{SS}.

The output buffer may be chosen at its programming stage as either push-pull or open-ended. To interface with TTL systems or when the wired-OR capability is required, the open-ended buffer would be used with an external resistor.

INTERFACE CIRCUITS WITH TTL SYSTEMS



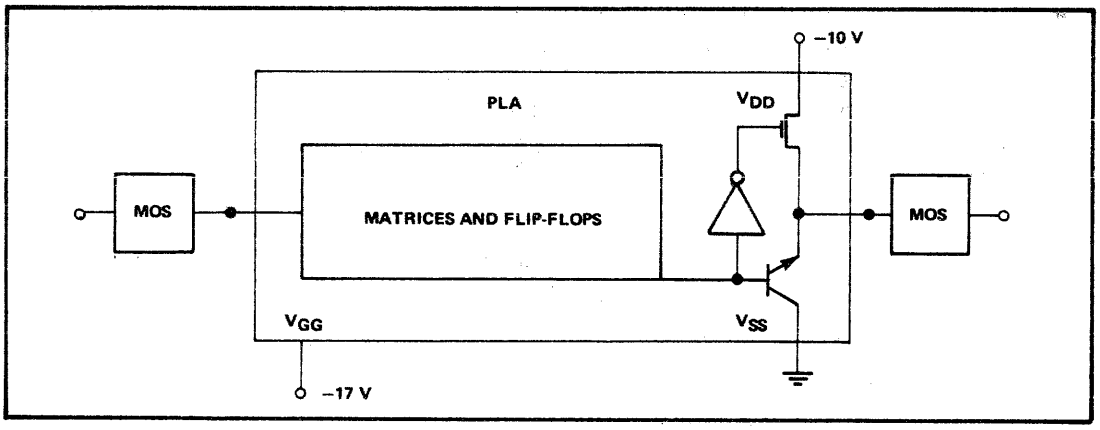
interfacing (continued)

b) To MOS systems

For input interfacing from other MOS devices, the internal pull-up resistors are not required.

The output buffer is selected as a push-pull type to provide a high-capacitive drive without the need of an external resistor.

INTERFACING WITHIN MOS SYSTEMS



custom programming

The logic functions performed by the PLA are controlled by programming or coding the product-terms-generator matrix and the sum-of-product-terms-generator matrix.

The number of different product terms is limited to 60 (TMS 2000 JC/NC) or 72 (TMS 2200 JC/NC).

The logic equations define the sum of product terms. There will be one equation for each output and for each flip-flop input. A computer program is used to implement the logic equations on the chip.

Complete information on programming Texas Instruments MOS/LSI programmable logic arrays is contained in a PLA SOFTWARE PACKAGE available from the TI field sales office.

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The rapid evolution of MOS technology has resulted in MOS memories that are competitive in cost with core memories and superior in performance. From 256 to 2000 bits, and for static or dynamic operation, MOS memories can be used for applications covering the entire spectrum of data handling systems from scratch-pad to computer main-frame memories.

1) Characteristics

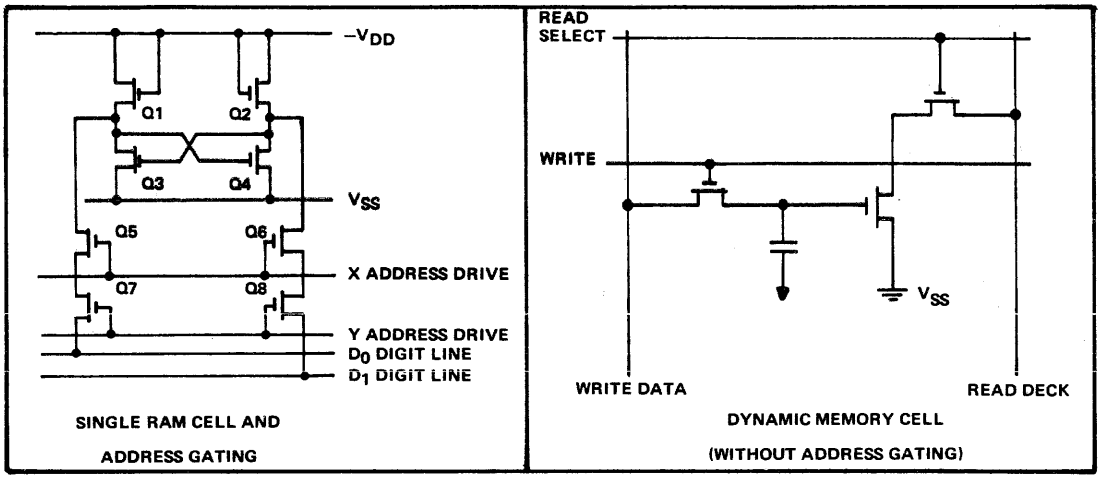
MOS RAMs are ideally suited for those applications requiring high speeds and low power dissipation. They can replace core memories used for scratch pads or for computers, while offering faster access times and a simpler drive circuitry. Their low access times make them attractive in applications where other semiconductor memories were considered, but found unsatisfactory for reasons of cost, power dissipation, or package count. For small systems, fully-decoded memories are easier to use. However, the speed of a fully decoded random-access memory is less than the speed of an off-the-chip bipolar decode X-Y select memory.

Random-access memories presently on the market are either static or dynamic.

- STATIC – An MOS flip-flop is used to store the information. Clocks are not needed. The data will stay in storage as long as the power is maintained.
- DYNAMIC – MOS capacitors are used as data storage elements. Data must be refreshed to assure integrity.

Random-access memories can also be defined as:

- Fully-Decoded Memories – A binary address determines the location in which the Write or Read operation is performed.
- Two-Dimensional Decode – The address of the word is given by an X-Y select.



SINGLE RAM CELL AND ADDRESS GATING

DYNAMIC MEMORY CELL (WITHOUT ADDRESS GATING)

2) Features

Whatever type of MOS RAM is considered, the following features are inherent:

- Nondestructuve Read out – In an MOS RAM the reading of information does not affect the content stored. So it is not necessary to perform a Write after every Read operation as is normal for magnetic memories. This is why the important parameter in an MOS memory is the access time rather than cycle time.
- Speed – Speeds of 150 ns with separate decoding, or 300 ns with decoding on the chip are typical.
- Power Dissipation – Power dissipation is typically less than 1-tenth mW per bit.
- Flexibility – MOS memories are available in much smaller sizes than the equivalent core memories. The memory configuration is very flexible and can be altered without appreciably increasing the basic price.

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- Environmental Characteristics (temperature range, mechanical, etc.) – Semiconductors are able to work in much more rugged environment than cores with much greater reliability.
- Cost – MOS memories are already more economical than magnetic memory cores for small- and medium-size systems. Mass assembly techniques, such as beam-lead MOS devices are being used to manufacture MOS memory systems and to further reduce the cost.

3) TI Devices

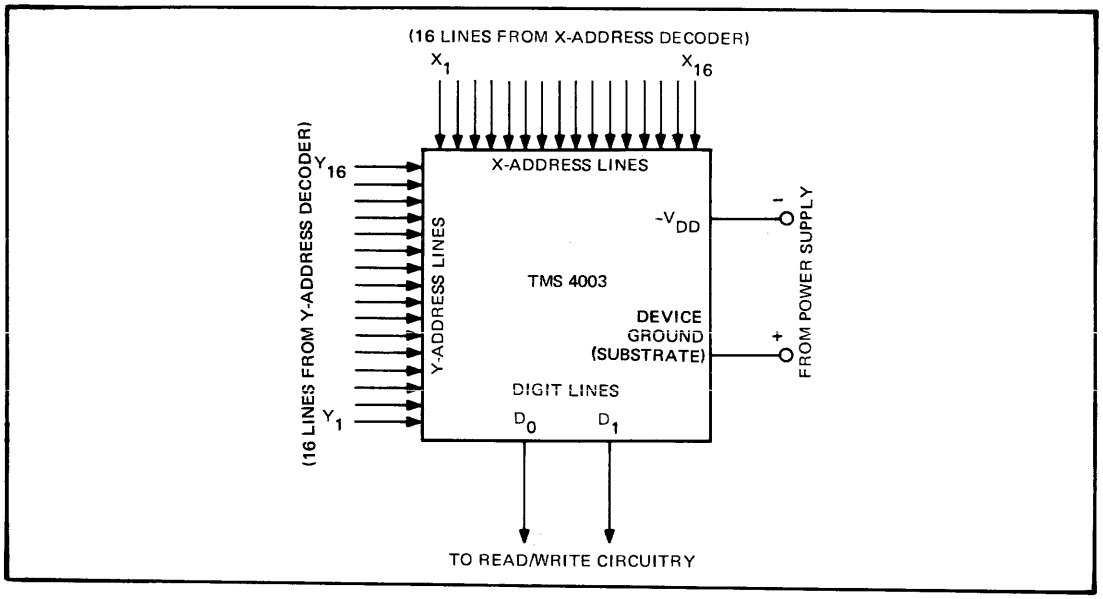
TI produces seven MOS RAM memory elements:

- TMS 1101 NC – 256-bit static RAM with decode
- TMS 4003 JR/NC – 256-bit high-speed random-access memory (with separate decode)
- TMS 1103 NC – 1024-bit dynamic RAM with decode
- TMS 4020 NC – 2048-bit dynamic RAM, high-speed, two external clocks
- TMS 4023 NC – 1024-bit dynamic RAM, medium-speed, low cost
- TMS 4025 NC – 2048-bit dynamic RAM, high-speed, low power
- TMS 4000 JC/NC – 128-bit content addressable (associative) memory

TMS 4003 JC – 256-bit high-speed random-access memory

The TMS 4003 JC/NC is a direct-address memory, having 16 X-address and 16 Y-address lines. Any one of the 256 bits in the memory can be selected by driving one X- and one Y-address line in coincidence. Sensing the logical state of the selected bit is achieved by differentially observing two outputs, D_0 and D_1, digit lines. The same digit lines are used to write information into an addressed bit. A block diagram of the TMS 4003 is shown on the following page.

DESCRIPTIVE BLOCK DIAGRAM OF THE TMS 4003 MOS RAM



No clock signals are required to operate the TMS 4003 JC/NC or to retain information. Such a design is referred to as static as distinguished from dynamic which requires the continuous application of single or multiple clock signals to function properly.

The memory organization of the TMS 4003 JC/NC is referred to as 256-words-by-1-bit, because an address can only select one bit at a time. Larger memory systems can be constructed using this 256 X 1 memory as a basic cell.

Paralleling address lines can increase word size. For example, if eight memories were connected by tying their respective X- and Y-address lines together, a 256-word by 8-bit memory would be formed. A single X-Y address applied to this system would produce eight separate digital outputs.

The number of words can be increased by paralleling digit lines. For instance, to make a 1024-word by 1-bit memory plane, four 256 X 1 memories are used, resulting in 32 X-address and 32 Y-address lines and a single output consisting of two digit lines.

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Memory planes like the one described can be paralleled in the same manner as individual memories. If eight 1024 X 1 planes, for example, had their corresponding X- and Y-address lines connected together, a 1024 X 8 memory system would result. A total of 32 TMS 4003 JC/NC MOS RAMs would be necessary for such a system. Even larger systems are possible, the ultimate size being limited by the drive capabilities of the external address and write circuitry.

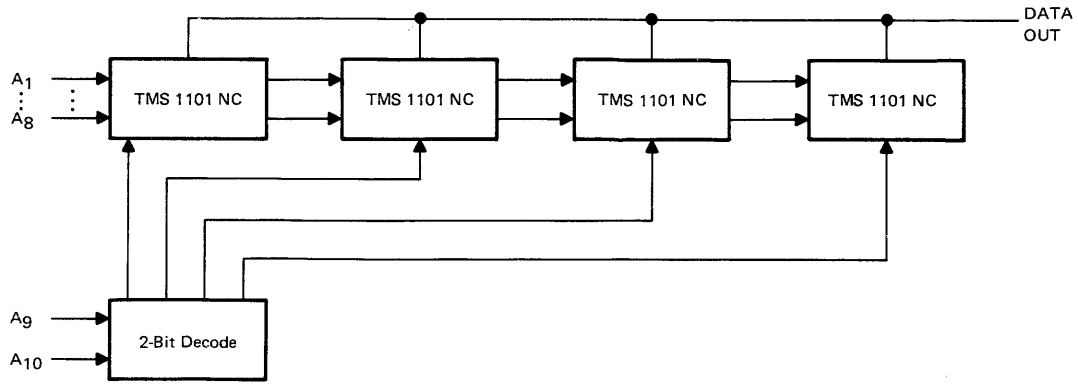
TMS 1101 NC – 256-bit random-access memory with decode

The TMS 1101 NC is a 256-bit fully decoded static random-access memory. Any one of the 256 bits in the memory can be selected by properly addressing the eight address lines. All inputs and outputs of TMS 1101 NC, including addresses and control logics, are fully TTL/DTL compatible; this will minimize interface problems in system designs.

The TMS 1101 NC is a full static circuit; no clock signals are required in operating the circuit.

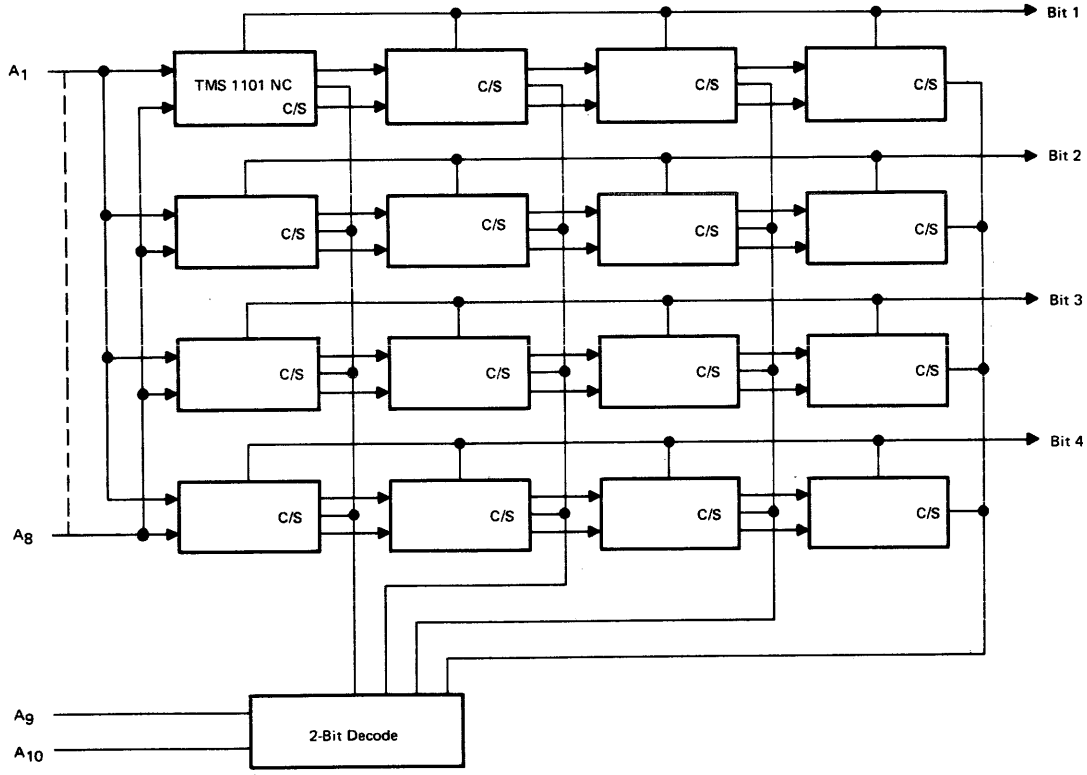
A chip-select control provided by the TMS 1101 NC allows several circuits to be wired-OR together, which makes the expanded organization of the memory a very simple operation.

The TMS 1101 NC can be considered to have a 251-words-by-1-bit organization. To expand the bit length of a word from 1 bit to n bits, it is only necessary to connect all address lines and control logics of n circuits in parallel. To increase the word size from 256 words to as many as m times 256 words, a decoder must be provided to select one out of m circuits which are all wired-OR together. Chip select controls of the circuits provide the means for the above expansion. A memory size of 1K words X 1 bit using TMS 1101 NC is illustrated in the following block diagram.



ORGANIZATION OF 1K-X-1 MEMORY USING TMS 1101 NC

To expand the 1K-X-1 memory into 1K X 4, the 2-bit decode can be shared by the four 1K planes as shown:



ORGANIZATION OF 4K-X-4 MEMORY USING TMS 1101 NC

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By the same approach, memory size of any word length and bit length can be organized easily using TMS 1101 NC.

There are several common factors in the following circuits:

- TMS 1103 NC – 1024-bit dynamic RAM
- TMS 4020 NC – 2048-bit dynamic RAM
- TMS 4023 NC – 1024-bit dynamic RAM
- TMS 4025 NC – 2048-bit dynamic RAM

For example, they are all dynamic; all provide an output sense current. However, there are also many characteristics which distinguish one circuit from the other. The table below lists key parameters of each memory circuit.

RAM Key Parameters

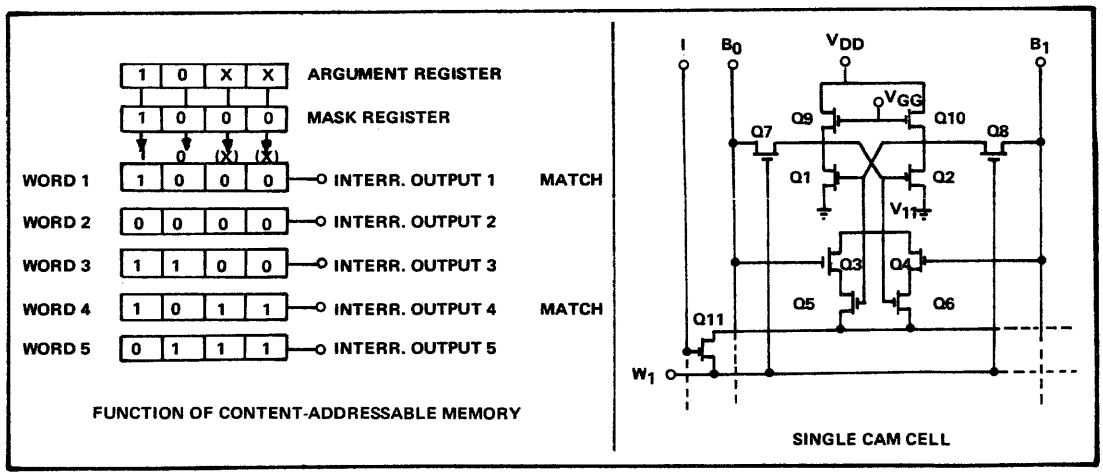
PARAMETER	UNITS	TMS 1103 NC	TMS 4020 NC	TMS 4023 NC	TMS 4025 NC
Total Bits	Bits	1024	2048	1024	2048
Organization	Bits	1024 X 1	1024 X 2	1024 X 1	1024 X 2
Access Time (min)	ns	300	320	650	280
Cycle Time (min)	ns	580	640	900	640
Power per bit at minimum cycle time and 25°C	mW/bit	0.3	0.15	0.08	0.07
Sense Current (min)	mA	0.6	1.2	1.0	1.2
Process		Si-Gate	S-A Gate	Nitride	S-A Gate
Refresh Period	μs	2	2	2	2
Read Cycle/Refresh Period		32	16	32	16
Chip Select/1K bit		1	2	1	1
Package		18-pin PDIP	24-pin PDIP	24-pin PDIP	24-pin PDIP

All dynamic memory cells use MOS capacitance and PN junction capacitance (parasitic) as temporary charge storage elements. However, due to the leakage property of PN junctions, charges stored in the capacitances must be restored periodically to assure the integrity of the information. This refreshing rate is temperature dependent, and must be performed once every two μs at 70°C. At room temperature the refreshing rate can be once every 50 μs.

In the dynamic RAM circuits, a refreshing operation is always performed during a Read cycle. The minimum number of Read cycles that must be performed in each refreshing period is dependent upon the organization of memory arrays. By considering the digit lines as a memory matrix or columns, and the Read or Write select lines as rows, all cells in the row selected during a Read cycle will be refreshed. Therefore, the minimum number of Read cycles required in each refresh period is the same as the number of rows in the memory matrix. For example, TMS 1103 NC is organized 32 rows X 32 columns; 32 Read cycles are required in each refresh cycle. TMS 4025 NC is organized 16 rows X 64 columns; therefore only 16 Read cycles are required.

All the dynamic RAMs (TMS 1103 NC, TMS 4020 NC, TMS 4023 NC, and TMS 4025 NC) have one or more chip-select controls; therefore, expansion of memory organization into any size can be achieved easily as shown in the preceding paragraphs on TMS 1101 NC.

The concept of a content-addressable memory has been around for many years but because of cost has not previously been practical. However, the performance and economics of MOS integrated circuits now make the concept highly desirable from both technical and cost standpoints. MOS integrated-circuit technology has finally made practical the content-addressable memory.



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A content-addressable memory (CAM) is a cell in which the words contained can all be matched simultaneously against an argument word, and outputs given wherever a true match is obtained. Each word has a Write input which can also be used to interrogate that word for a match. Two bit lines run through each column of cells allowing the word data to be written in. They may also be used for reading the contents of a word or for masking parts of the argument word where a "Don't Care" state exists.

In the basic CAM cell transistors, Q_1, Q_2, Q_9 and Q_{10} compose a flip-flop for data storage. Q_7 and Q_8 are selection transistors which, when turned On by the application of a negative voltage to the W line, connect the flip-flop nodes to the B_0 and B_1 bit lines. When the W line is at a 0, Q_7 and Q_8 are Off, isolating the flip-flop from the bit lines. Transistors Q_3, Q_4, Q_5, Q_6 and Q_{11} perform the Interrogate logic. For this mode each W line is grounded through a small resistor and Q_{11} is turned On. Transistors Q_3, Q_4, Q_5 and Q_6 compare the state of the memory cell flip-flop with the voltages externally applied to the bit lines. Thus the Word lines are controls for Write and Read operations but outputs for the Interrogate operation. The bit lines are inputs for Write and Interrogate, but outputs for Read.

TMS 1101 JC, TMS 1101 NC
256-BIT RANDOM-ACCESS MEMORY

features

- Low power dissipation
- 600-nsec access time (typ), 750 nsec (max)
- Direct DTL and TTL compatibility
- Wire-OR capability
- Fully decoded on chip
- Inputs fully protected
- Data Out and $\overline{\text{Data Out}}$ available
- Single chip-select line
- Single Read/Write line

description

The TMS 1101 JC/NC is a 256-bit RAM, organized as 256 one-bit words and using P-channel enhancement-mode (normally Off) MOS transistors. The TMS 1101 JC/NC will interface directly with standard TTL and DTL bipolar integrated circuits. A separate chip-select lead allows easy selection of an individual package when outputs are used in a wire-OR fashion.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

An 8-bit address code selects any one of 256 bits for either Read or Write operation — all address input levels being TTL or DTL logic levels.

A logic 0 level applied to the R/W control will result in a Read operation, and may be presented simultaneously or before application of the address code. Read-out is non-destructive.

A logic 1 level applied to the R/W control will create the condition for the Write operation. The duration of the Write command must be at least 400 nanoseconds to ensure that the data is written into the memory. The Write command should be Off by the time the address code is changed. The input data should coincide with at least the last 300 nanoseconds of the Write command.

The memory is inhibited with the application of a logic 1 to the chip-select line. This action renders the Read/Write line and data inputs ineffective. The address decode will not be inhibited. Also, the output leads are open when the array is inhibited, allowing many chips to be wired-OR together.

A unit mounted in a 16-pin hermetically sealed ceramic dual-in-line package is designated "TMS 1101 JC". Mounted in a 16-pin plastic dual-in-line package, the device is numbered "TMS 1101 NC".

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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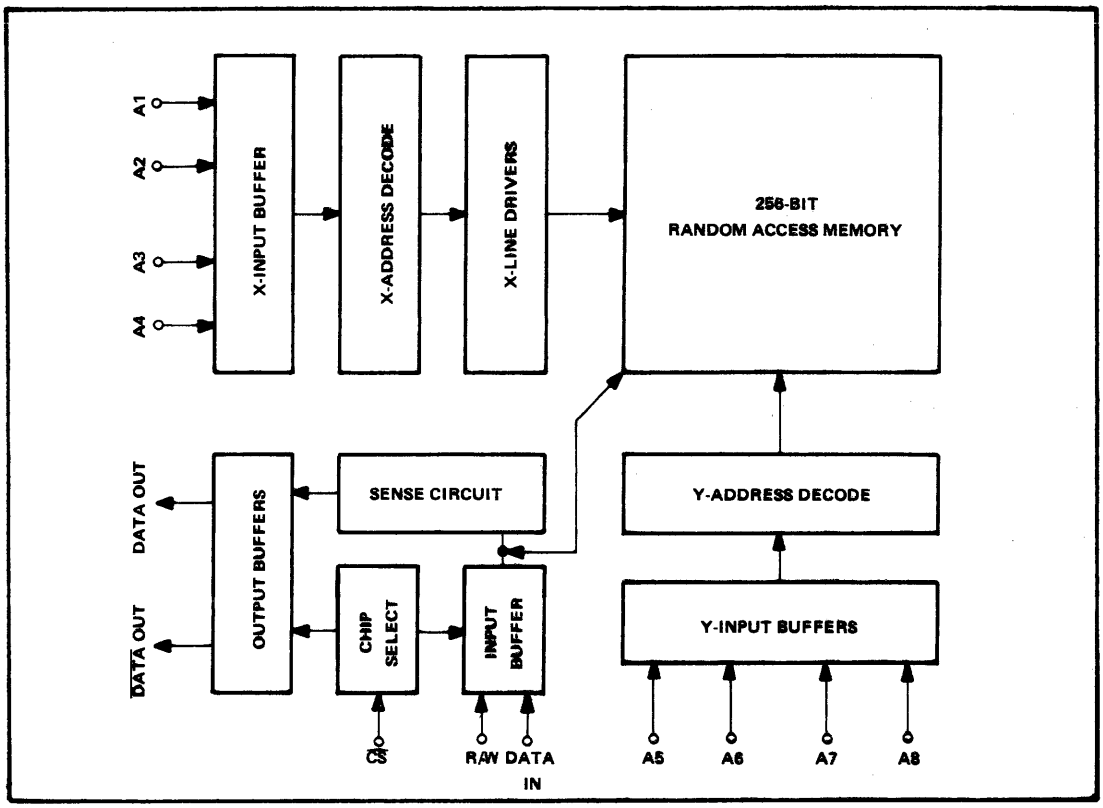
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_D range (See Note 1)	−20 V to 0.3 V
Supply voltage V_{DD} range (See Note 1)	−20 V to 0.3 V
Data input voltage range (Note 1)	−20 V to 0.3 V
Storage temperature range	−55°C to 150°C
Operating free-air temperature range	−25°C to 85°C

NOTE 1: These voltage values are with respect to V_{SS} (substrate).

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNITS
Operating Voltage					
	Substrate supply V_{SS}	+4.75	+5.0	+5.25	V
	Supply V_{DD}	−9.50	−10.0	−10.50	V
	Supply V_D	−9.50	−10.0	−10.50	V
Logic Levels					
	Input HIGH level V_{IH}	+3.5			V
	Input LOW level V_{IL}			+0.6	V
Pulse Timing					
	Write Pulse Width t_{WP}		400		ns
	Write Delay t_{Wd}		0		ns
	Write Time t_W	300			ns
	Data Overlap t_{DO}	100			ns

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Current				500	nA
Output Current						
I_{LO}	Leakage current				1000	nA
I_{OL}	Sink current	V_{OUT} = 0.4 V	1.6			mA
	Source current	V_{OUT} = 0.0 V		0.1		mA
Output Voltage						
V_{OL}	Output LOW voltage				+0.4	V
V_{OH}	Output HIGH voltage		+4.0			V
Capacitance						
C_{IN}	Input	V_{IN} = +5 V, F = 1 MHz			10	pF
C_{OUT}	Output	V_{IN} = +5 V, F = 1 MHz			10	pF
Power Supply Current						
V_{DD}	Supply				13	mA
V_D	Supply				19	mA

dynamic electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS
Access Time					
t_{AL}	Output LOW level		600	750	ns
t_{AH}	Output HIGH level		600	750	ns

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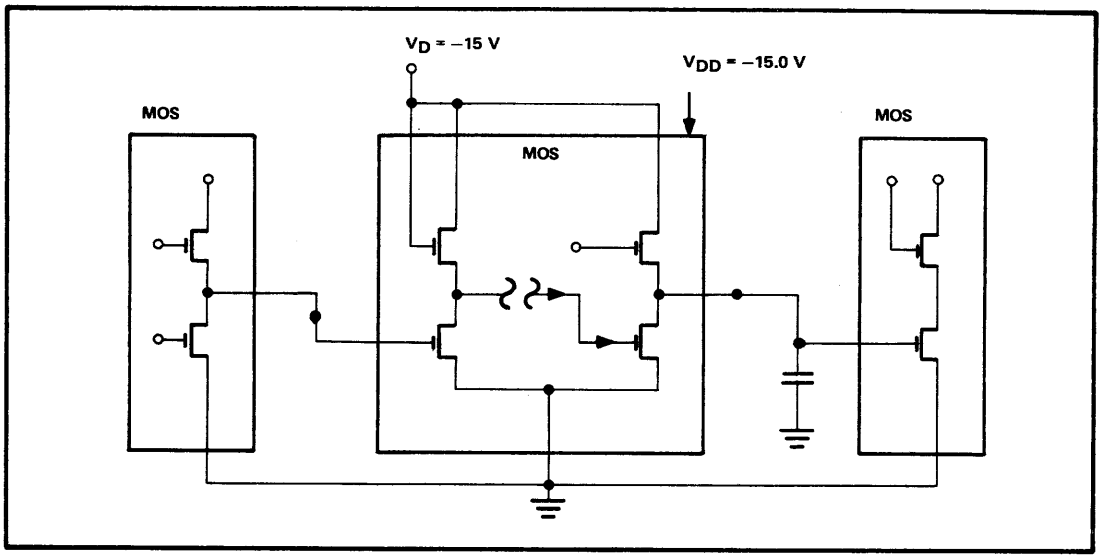
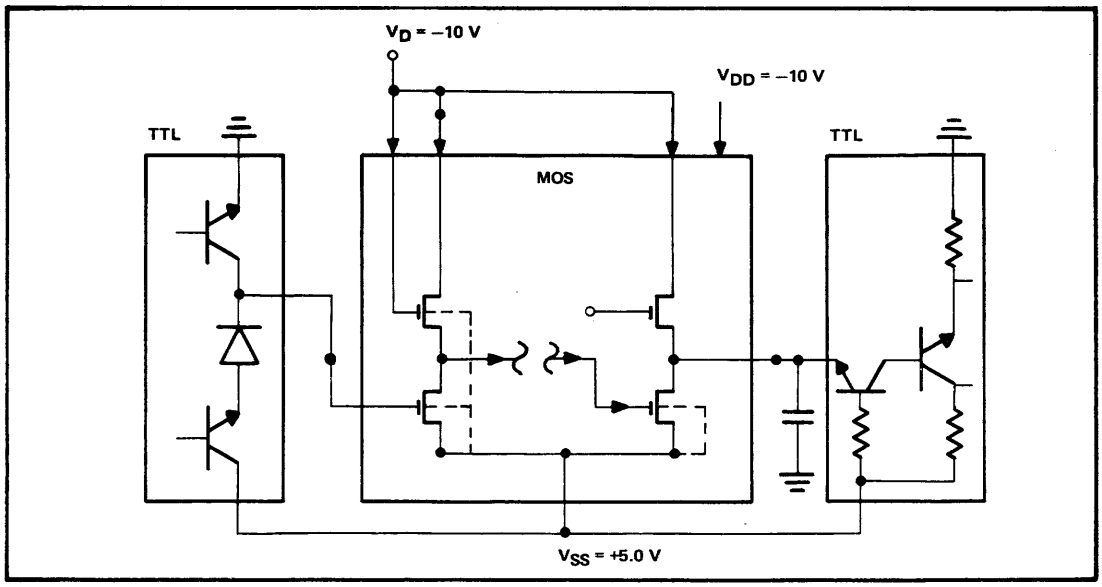
interface circuits

a) MOS



b) TTL



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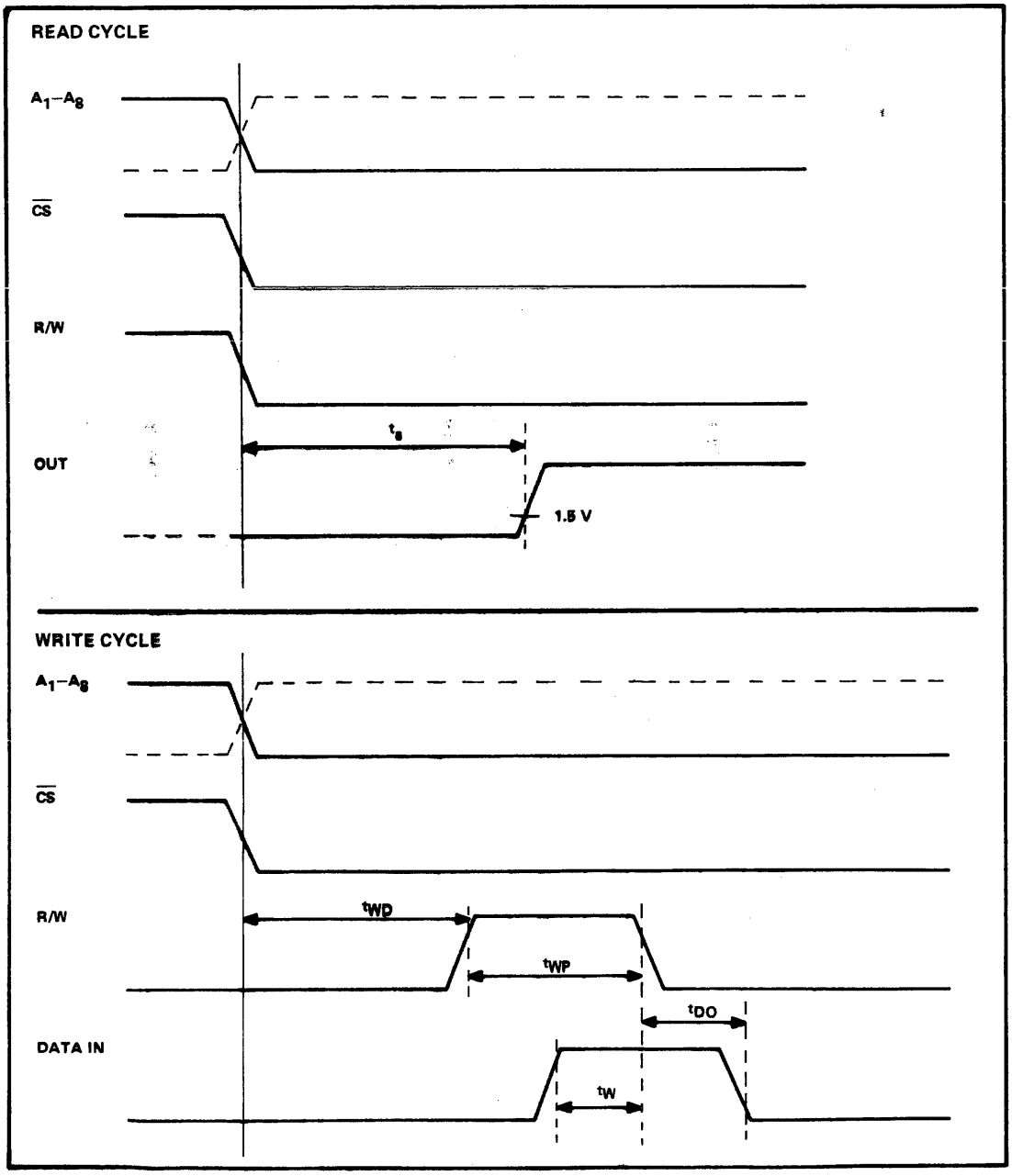
timing diagram and voltage waveforms



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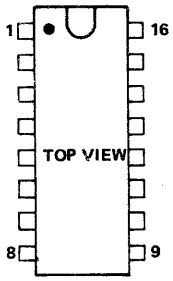
mechanical data and pin configuration

The device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 1101 JC) and in a 16-pin plastic dual-in-line package (TMS 1101 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	Address 6	9	Address 3
2	Address 8	10	Address 2
3	Address 7	11	Address 4
4	V_D	12	Data in
5	V_{SS}	13	Data out
6	Address 5	14	$\overline{\text{Data out}}$
7	Address 1	15	Read/Write
8	V_{DD}	16	$\overline{\text{Chip Select}}$

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TMS 1103 NC
FULLY-DECODED 1024-BIT RAM

features

- Low power dissipation
- Cycle time – 500 nsec
- Access time – 300 nsec
- Expansion capability
- Fully decoded
- Static charge protection
- 18-lead plastic package

description

The TMS 1103 NC is a low-cost main-frame memory design used for large-storage high-performance applications.

Organized as a 1024- by 1-bit random access memory, the TMS 1103 NC is a fully decoded monolithic array. This feature permits the use of an 18-pin dual-in-line package.

This dynamic memory has nondestructive readout, and refreshes all 1024 bits in 32 Read cycles.

Utilizing the latest silicon-gate low-threshold technology makes possible a high functional density.

logic definition

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

Refer to functional block diagram and timing diagram. Access begins time t_{AC} before the negative transistion of chip enable. In this duration the precharge is active and the row and column decoders settle out. Next, during the period t_{OV}, the contents of the 32 cells along the selected row are written into the refresh amplifiers. One is required at each column of the array. During the overlap interval, the data output is held high by the selected column amplifier. At the positive transistion of precharge, the contents of the refresh amplifiers are rewritten into their respective columns and the data output is valid t_{PO} later. A suitable time t_{PW} after precharge, the state of the In Data line may be copied into the selected cell using a Write pulse of minimum time t_{WP}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range (See Note 1)	–24 V to 0.3 V
Clock input voltage range (See Note 1)	–24 V to 0.3 V
Data input voltage range (See Note 1)	–24 V to 0.3 V
Operating free-air temperature range	–25°C to 70°C
Storage temperature range	–55°C to 150°C

NOTE 1: These voltage values are with respect to V_{BB} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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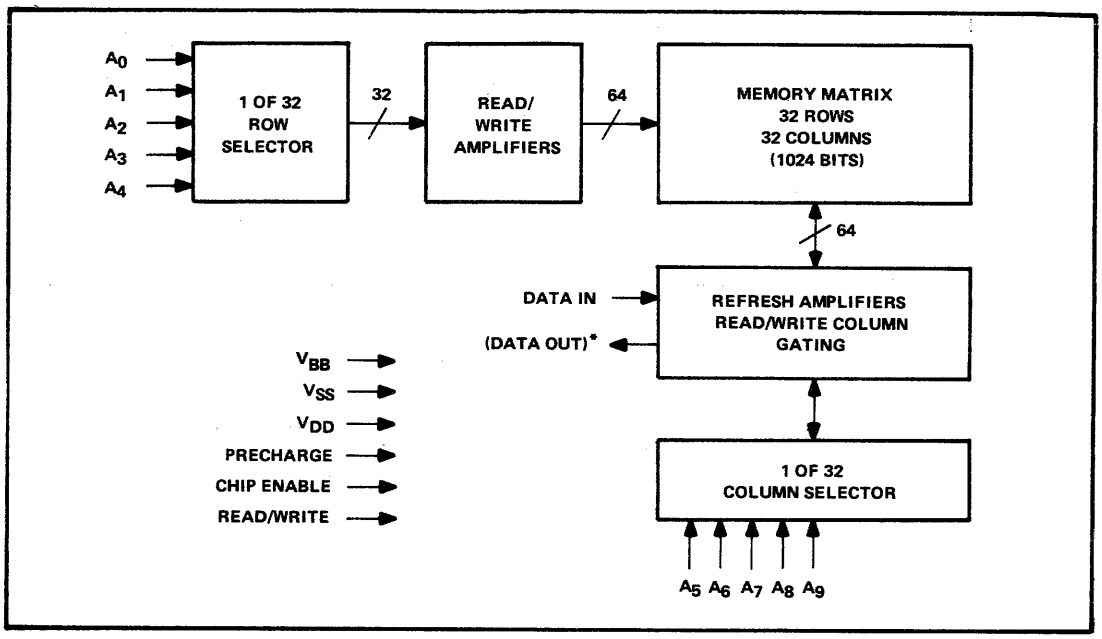
functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
System ground V_{SS}	+15	+16	+17	V
Drain supply V_{DD}		0		
Substrate bias supply V_{BB}	$V_{SS}+3$	$V_{SS}+3.5$	$V_{SS}+4$	V
Pulse Timing				
Precharge pulse width t_{PC}	240	250	315	ns
Precharge and Chip Enable overlap t_{OV}	0	10	100	ns
Address set-up time to Chip Enable t_{AC}	150			ns
Precharge to Read/Write t_{PW}	200		500	ns
Read/Write pulse width (Note 1) t_{WP}	70			ns
Address to valid output t_{ACC1}	300			
Precharge to valid output t_{ACC2}	390			
Refresh interval t_{REF}			2	ms
Precharge to end of Chip Enable t_{POV}	200		600	ns
Precharge to valid output t_{PO}		110	150	ns
Write or Read/Write Cycle t_{WC} or t_{RWC}	580			
Read Cycle t_{RC}	580			

NOTE: 1. Data IN must be stable during t_{WP} and remain stable for at least 20 ns after t_{WP}.

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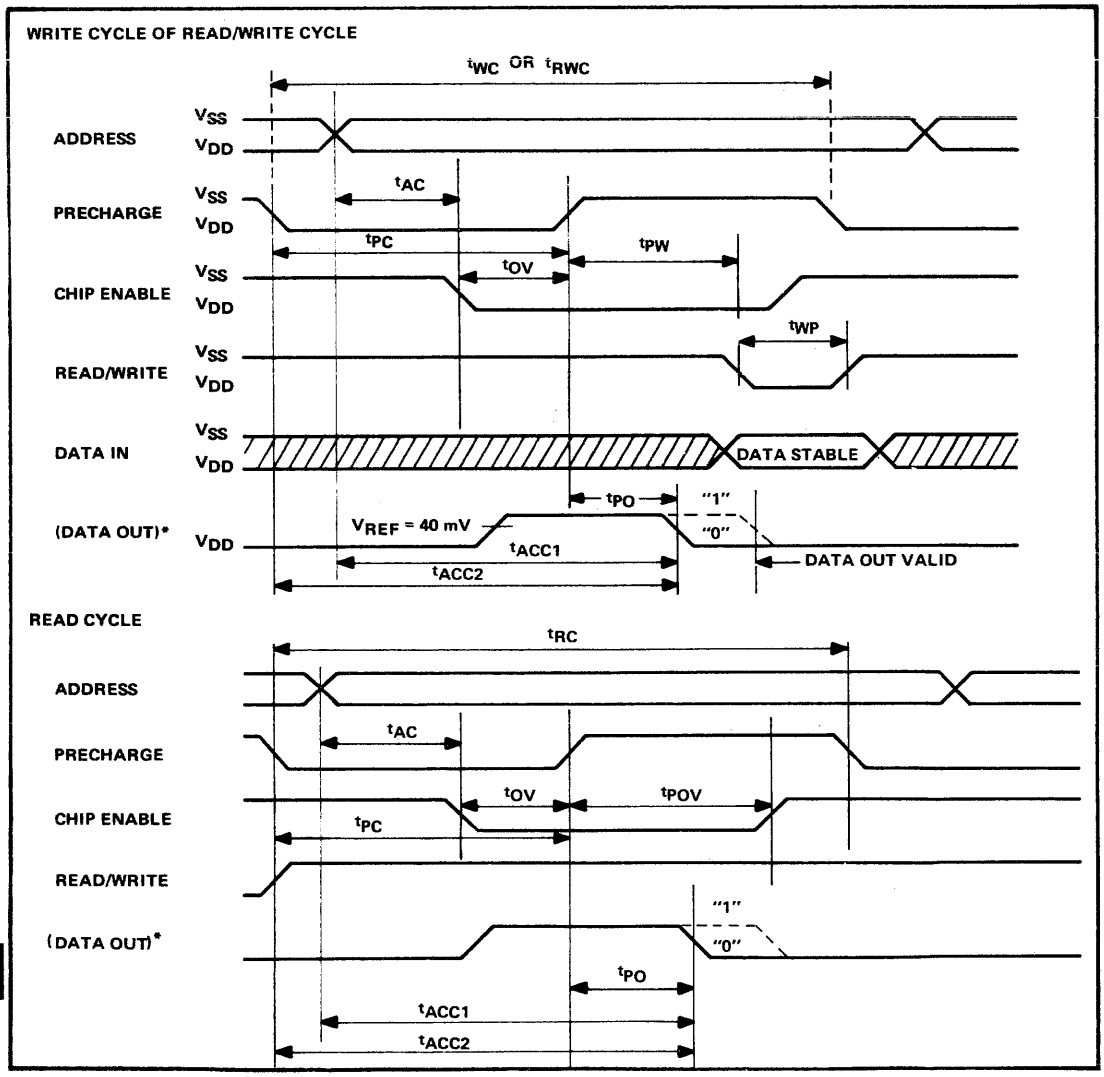
electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
V_{IL}	Input LOW voltage		$V_{SS}-17$	$V_{SS}-16$	$V_{SS}-15$	
V_{IH}	Input HIGH voltage		$V_{SS}-1$	V_{SS}	$V_{SS}+1$	
I_{IN}	Input Load Current				1	μA
I_{OH}	Output HIGH Current		700	900		μA
I_{OL}	Output Leakage Current				1	μA
I_{DD}	Average V_{DD} Current	t_{PC} = 240 ns		14	20	mA

timing diagram and voltage waveforms



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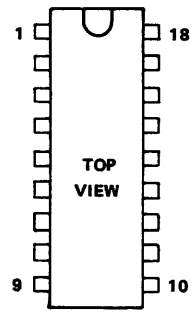
mechanical data and pin configuration

The TMS 1103 NC is mounted in an 18-pin plastic dual-in-line package. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_3	10	V_{BB}
2	A_2	11	V_{DD}
3	A_1	12	Data In
4	A_0	13	A_8
5	Precharge	14	(Data Out)*
6	A_9	15	A_4
7	A_6	16	Chip Enable
8	A_5	17	V_{SS}
9	A_7	18	Read/Write

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TMS 4000 JC, TMS 4000 NC
HIGH-SPEED CONTENT-ADDRESSABLE MEMORY

features

- Static operation
- Nondestructive readout and interrogation
- High-speed operation — 250-ns typical system cycle time
- Low standby power dissipation
- Masked write and interrogation capability
- Low threshold technology

description

The TMS 4000 JC/NC is a high-speed content-addressable memory organized as 16 eight-bit words. The entire device is constructed on a single monolithic chip using low-threshold MOS P-channel enhancement-mode transistors. Active-element design permits nondestructive readout and interrogation of memory contents. Bit lines can be wire-OR connected to obtain memory planes greater than 16 words. Word lines can be wire-OR connected to achieve word lengths of greater than eight bits per word. Selection of a given word for reading or writing is accomplished by connecting the selected word line to a negative voltage while holding all other word lines at ground. The common interrogation control 1, when returning to a negative voltage, allows all sixteen words to be interrogated simultaneously.

Memory writing is accomplished by addressing a desired word and bringing the appropriate bit lines to ground while holding the other bit lines at a negative potential. If both lines of a selected bit are held at the negative potential, the information in the bit will be unchanged during a writing cycle. Masked writing therefore can be achieved.

Reading each bit content of an addressed word requires sensing differential current between the two bit lines. Both lines should be held near a logic 1.

Interrogation of memory content is accomplished by activating the interrogation command I, bringing bit lines to appropriate voltages, and simultaneously sensing the current in each word line. If both bit lines of a particular bit are held at ground potential during an interrogation cycle, that bit will be excluded from the interrogation. If a word perfectly matches the interrogation information, no current will flow through the word lines. One or more mismatches will cause at least 200 μA to flow in the word line.

"TMS 4000 JC" designates a unit mounted in a 40-pin hermetically sealed dual-in-line package, and "TMS 4000 NC" is the number for a unit mounted in a 40-pin dual-in-line plastic package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −14 V
Operating free-air temperature range . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage V_{GG}	−11	−12	−13	V
Supply voltage V_{DD}	−11	−12	−13	V
Supply voltage V_{II}	2.7	−3	−13	V
Write time (t_W)	60			ns
Settling time (t_s)	50			ns

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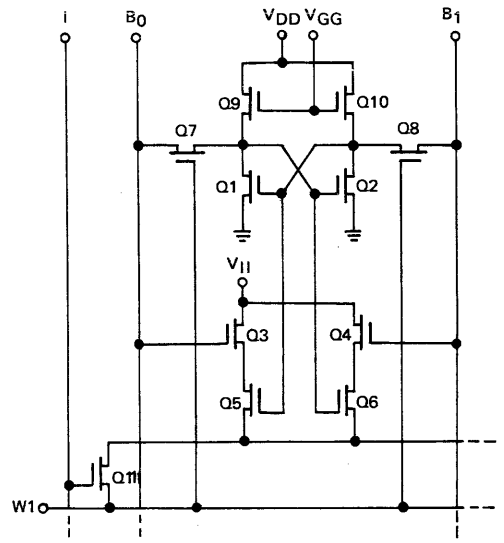
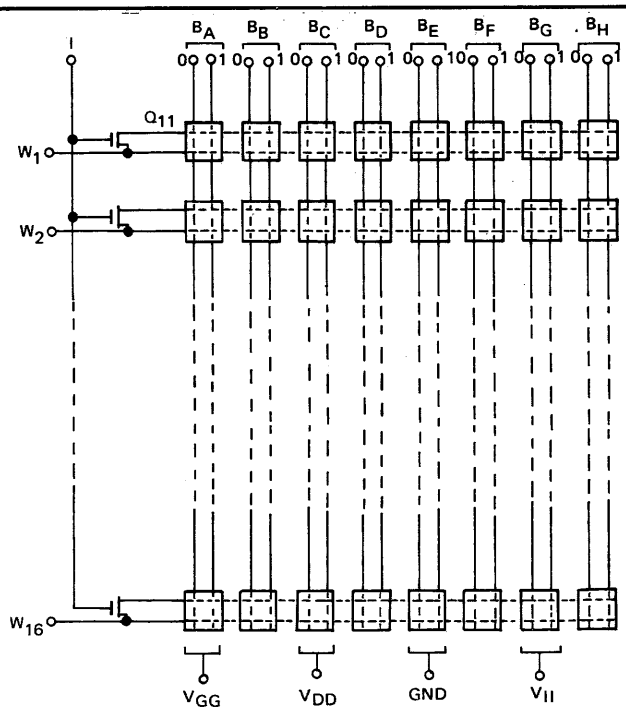
CONTENT-ADDRESSABLE MEMORY CELL



CONTENT-ADDRESSABLE MEMORY ORGANIZATION



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logic definition

Negative logic is assumed

a) Logic 1 = most negative voltage

b) Logic 0 = most positive voltage

OPERATION	INPUT VOLTAGE				OUTPUT SIGNALS
	I	W	B_0	B_1	
Write 0	0	1	1	0	
Write 1	0	1	0	1	
Masked Write	0	1	1	1	
Read 0	0	1	1	1	Current in B_1 (200 μA minimum)
Read 1	0	1	1	1	Current in B_0 (200 μA minimum)
Interrogate 0	1	0	1	0	Current in W indicates mismatch (200 μA minimum)
Interrogate 1	1	0	0	1	
Masked Interrogate	1	0	0	0	No current in W from this bit
Standby	0	0	X	X	(See Note 1)

NOTE 1: X = 1 or 0 (don't care)

electrical characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

R_L = 100 Ω (See CAM operational requirements)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
	Read-mode sense current	Logic 0 stored in a bit cell	B_0			−10	μA
			B_1	−200	−400		
		Logic 1 stored in a bit cell	B_0	−200	−400		
			B_1			−10	
	Interrogate-mode sense current	Matched				−10	μA
		One bit mismatched		−200	−400		
		All bits (8) mismatched			−2000	−3000	
I_B	Bit-line leakage current	16 in parallel @ −12 V				10	μA
I_W	Word-line leakage current	16 in parallel @ −12 V				10	μA
I_I	Interrogate line leakage current	At −12 V				100	μA
I_{DD}	Drain supply current				3.0	5.0	mA
I_{II}	Interrogation supply current per word	One bit mismatched		-0.2	−0.4		mA
		All bits (8) mismatched			−2.0	−3.0	
	Total power dissipation	Standby			40	60	mW
		Read or Write				100	
		Interrogation				200	
C_B	Bit-line capacitance	V_B = 0 V,	f = 1 MHz		13		pF
C_W	Word-line capacitance	V_W = 0 V,	f = 1 MHz		12		pF
C_I	Interrogate-line capacitance	V_I = 0 V,	f = 1 MHz		40		pF

switching characteristics (under nominal operating conditions at 25°C, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_s	Settling time				50	ns
t_{ai}	Interrogate access time			50	80	ns
t_{ar}	Read access time			30	60	ns

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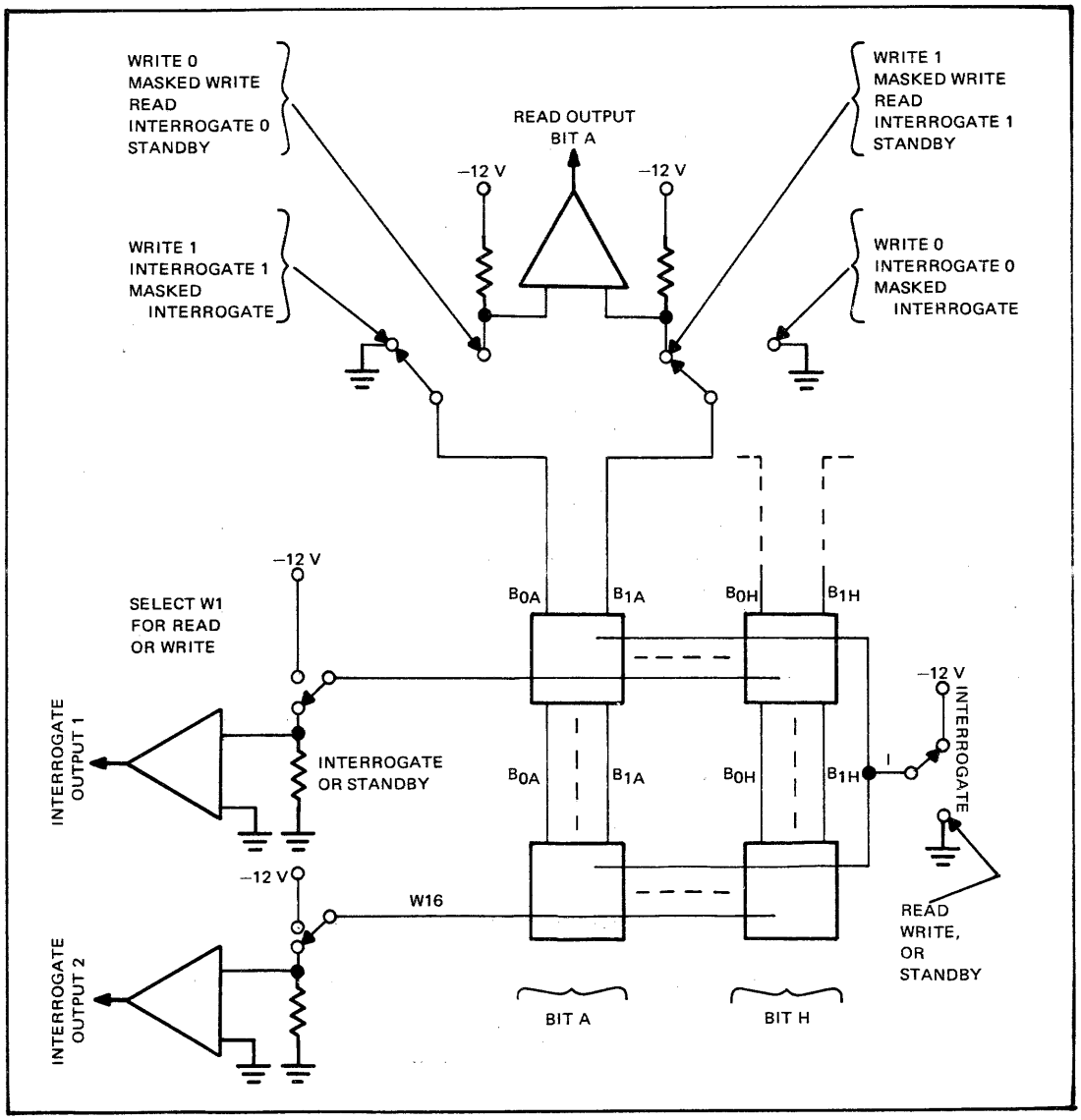
content-addressable memory operational requirements



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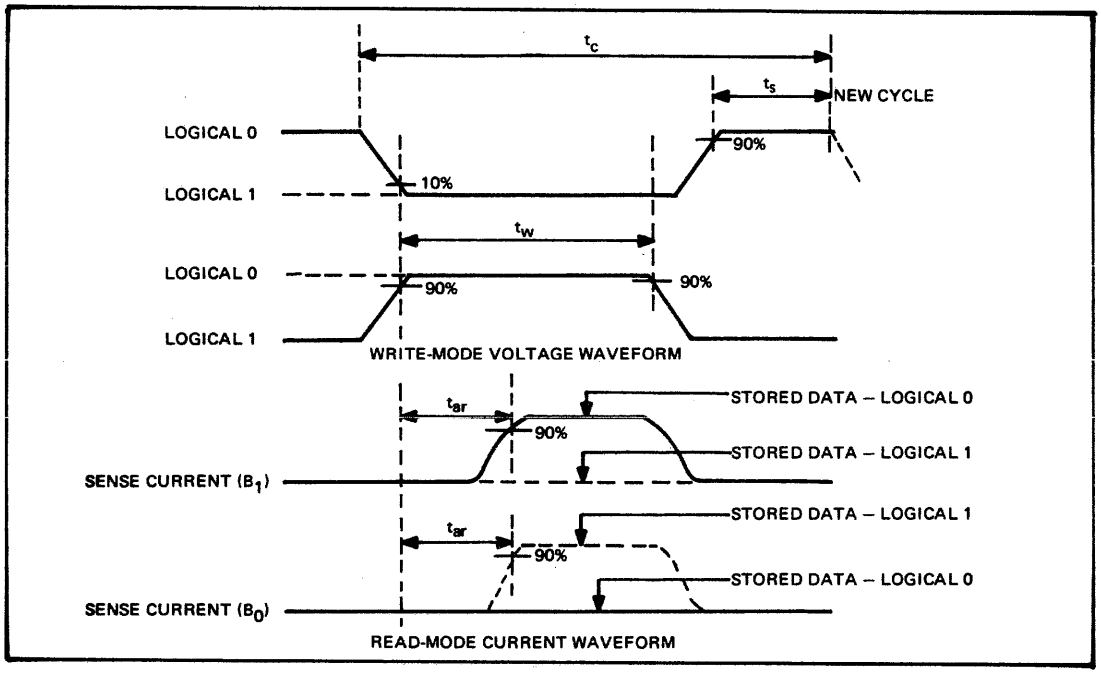
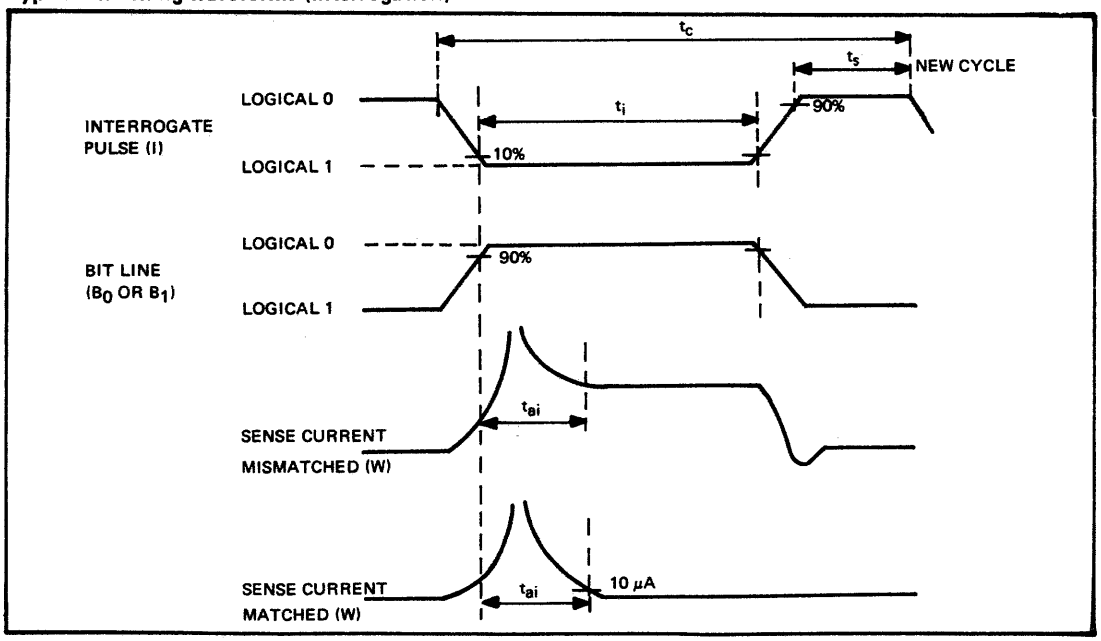
typical switching waveforms (read and write)



typical switching waveforms (interrogation)



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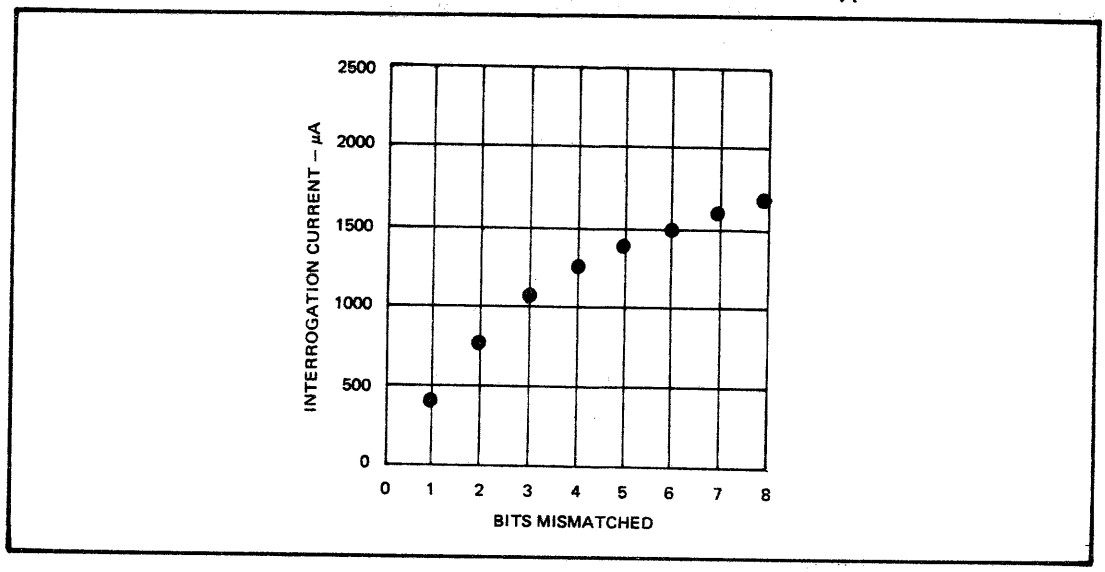
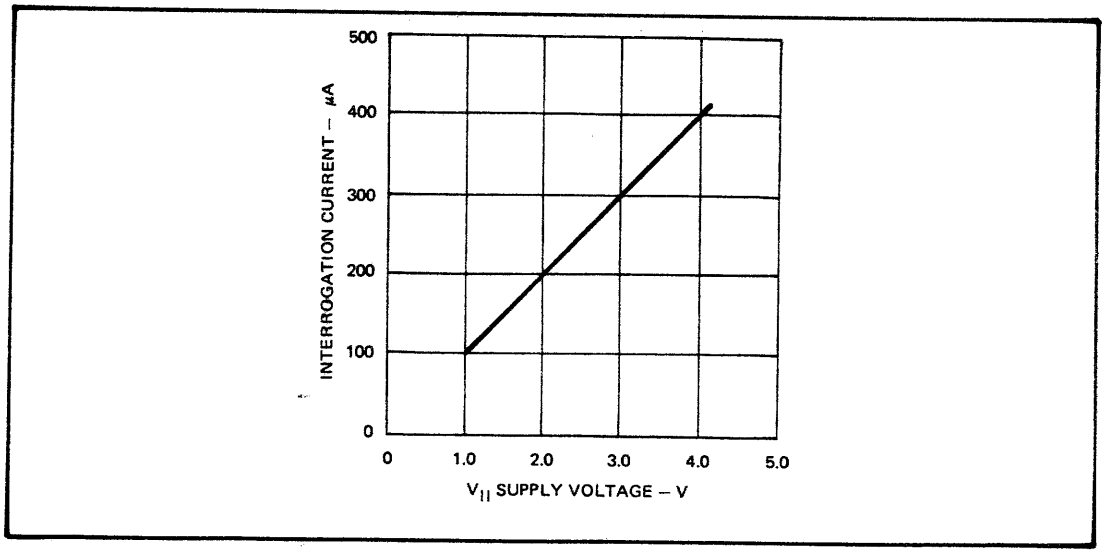
Interrogation Current vs Number of Bits Mismatched, And vs V_{II} Supply Voltage

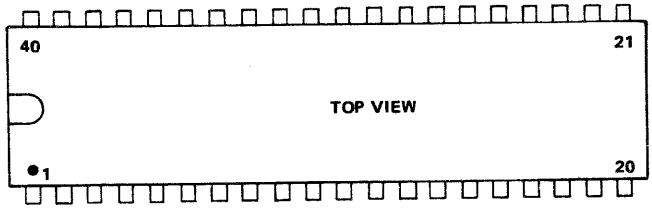
($R = 100\ \Omega$, $V_{DD} = -12$ V, $V_{GG} = -12$ V, Logical 1 = −12 V, $T_A = 25°C$)





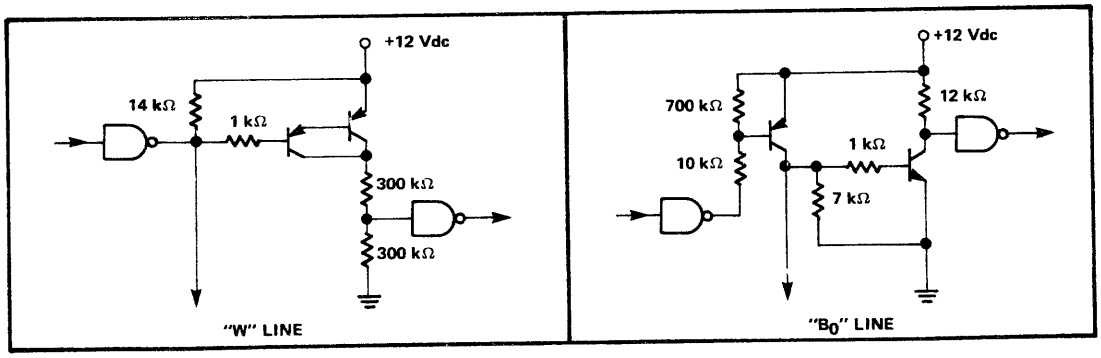
mechanical data and pin configuration

The device is available in both a 40-pin hermetically sealed ceramic dual-in-line package (TMS 4000 JC) and a 40-pin dual-in-line plastic package (TMS 4000 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers.



PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	0 } B_6	11	W_8	21	1 } B_3	31	W_9
2	1 } B_6	12	W_6	22	0 } B_3	32	W_{11}
3	0 } B_8	13	W_4	23	1 } B_1	33	W_{13}
4	1 } B_8	14	W_2	24	0 } B_1	34	W_{15}
5	I	15	V_{GG}	25	V_{DD}	35	NC
6	GND	16	NC	26	NC	36	V_{II}
7	W_{16}	17	1 } B_5	27	W_1	37	0 } B_2
8	W_{14}	18	0 } B_5	28	W_3	38	1 } B_2
9	W_{12}	19	1 } B_7	29	W_5	39	0 } B_4
10	W_{10}	20	0 } B_7	30	W_7	40	1 } B_4

typical read/write interface for one-microsecond operation



NOTE: All gates = SN7400

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TMS 4003 JR, TMS 4003 NC
256-BIT RANDOM-ACCESS MEMORY

FEBRUARY, 1971

FOR MEMORY APPLICATIONS REQUIRING HIGH-SPEED READ/WRITE CAPABILITY

- **Nondestructive readout**
- **Static operation**
- **System access time under 200 ns**
- **Low power dissipation**

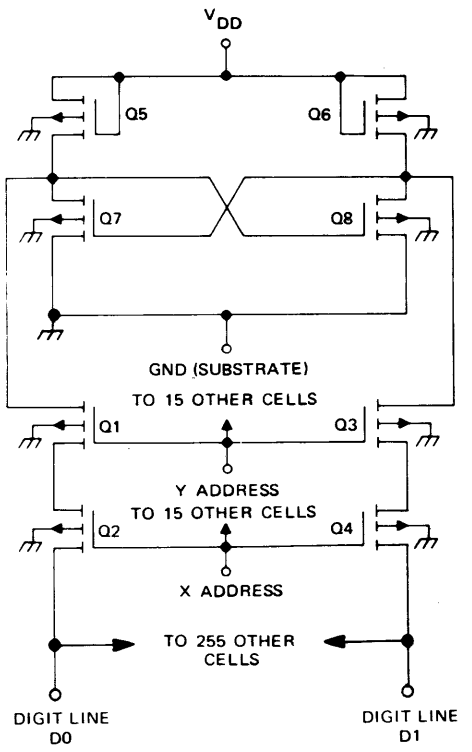
description

The TMS 4003 JR/NC is a high-speed random-access memory consisting of 256 cross-coupled flip-flops organized as 256 one-bit words. The entire device is constructed on a single monolithic chip using thick-oxide techniques to produce MOS P-channel enhancement-type transistors. Active-element design permits nondestructive readout, because addressing each bit tends to reinforce its existing state. Digit lines can be wire-OR connected to obtain memory planes greater than 256 words. External decoding circuitry can be used for additional planes to achieve desired word length. Selection of a given bit for reading or writing is accomplished by the coincident addressing of one of 16 X lines and one of 16 Y lines. These two lines are taken to V_{DD} while all other X and Y lines are held at ground.

Memory writing is accomplished by externally addressing the desired cell and bringing the appropriate digit line to ground while holding the other digit line at its nominal V_{DD} potential.

Reading an addressed cell requires sensing a differential current between the two digit lines. Both digit lines should be held near their nominal value of V_{DD}. This causes addressing transistors Q1, Q2, Q3, and Q4 to act as additional load resistors in parallel with standby load resistors Q5 and Q6, (see Figure 1). Depending on the flip-flop state, current will flow in one of the digit lines and not the other.

Maximum speed of the circuit is limited by the propagation delay of the Y address voltage through a series of P-diffused tunnels. The write or read cycle time, including this delay and the TTL address-decode delay, will be under 200 nanoseconds (see Figure 2).



CELL SCHEMATIC (1 OF 256 CELLS)

FIGURE 1

Power dissipation is typically 0.6 mW per bit when the memory is operated with an 18-volt dc power supply. Significantly lower average power dissipation may be obtained without sacrifice of system performance by synchronously or asynchronously pulsing the V_{DD} power supply. This feature is a result of the temporary data storage provided by the gate capacitance of transistors Q7 and Q8.

— continued

description (continued)

A unit mounted in a 40-pin hermetically sealed ceramic dual-in-line package is designated "TMS 4003 JR". Mounted in a 40-pin plastic dual-in-line package the device is numbered "TMS 4003 NC".

logic

Logic levels for this memory are defined in terms of standard NEGATIVE LOGIC where:

−16 V to −20 V = LOGICAL 1
+0.3 V to −2 V = LOGICAL 0

OPERATING MODE	ADDRESS LINES OF SELECTED CELL		DIGIT-LINE TERMINALS	
	X	Y	D1	D0
Read	1	1	1	1
Write a zero	1	1	1	0
Write a one	1	1	0	1

A selected cell has both its X and Y address lines at logical 1. During read and write operations, only one cell should be selected at a time. An unselected cell is a cell which has at least one of its address lines at logical 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any terminal relative to substrate (GND) . . . . . +0.3 V to −22 V
Operating free-air temperature range . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	−16	−18	−20	V
Write access time, t_{aw} (See Note 1 and Figure 3)	80			ns
Write pulse width, t_{pw} (See Figure 3)	30			ns

NOTE: 1. Write access time is the delay between the application of address voltages at the X and Y inputs and the start of the write pulse. Premature application of the write pulse may cause undesired writing into cells other than the addressed cell.

operating characteristics (unless otherwise noted T_A = 25°C)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Read-mode sense current	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 0 stored in cell nm	D0	−200	−400		μA
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -16$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−200	−400		
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 0 stored in cell nm	D0	−300	−500		
		D1		−0.1	−10	
	$V_{Xn} = V_{Ym} = V_{in(D0)} = V_{in(D1)} = V_{DD} = -18$ V, Logical 1 stored in cell nm	D0		−0.1	−10	
		D1	−300	−500		
Address-line current (16 lines in parallel)	V_X or V_Y = −20 V, $V_{in(D0)} = V_{in(D1)} = V_{DD}$ = 0 V				−10	μA
Total power dissipation	One cell addressed, V_{DD} = −18 V			150	300	mW
	One cell addressed, V_{DD} = −20 V, T_A = −55°C				500	

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operating characteristics, continued (unless otherwise noted $V_{DD} = -18$ V, $T_A = 25°C$)

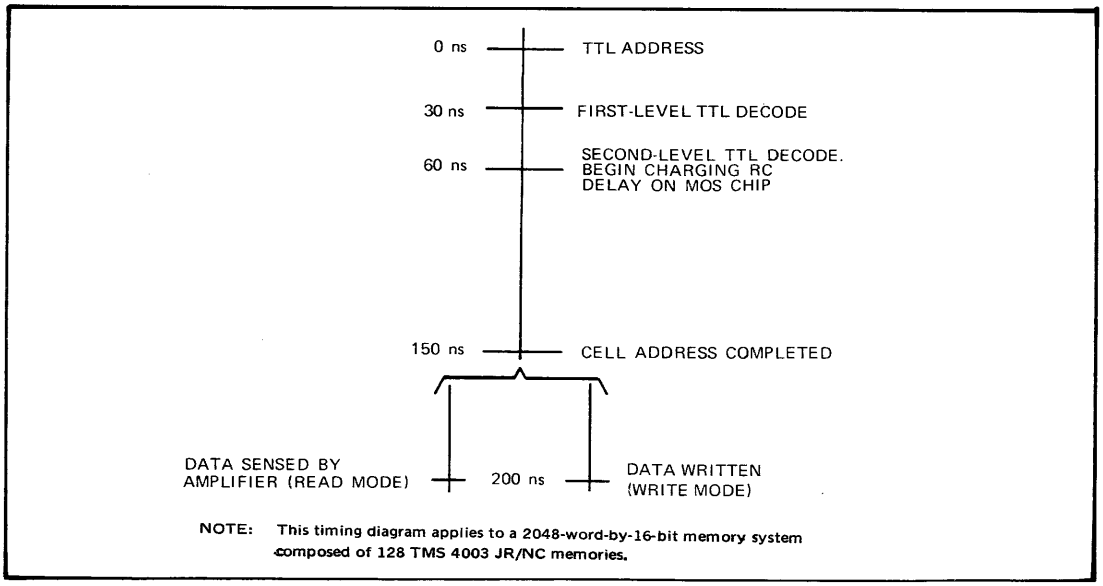
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitance between digit-line terminal and substrate	$V_{in(D0)} = V_{in(D1)} = 0$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		50		pF
	$V_{in(D0)} = V_{in(D1)} = -18$ V, f = 140 kHz, $V_X = V_Y = 0$ V (or one cell addressed), See Note 2		30		
Capacitance between digit-line terminal and physically adjacent address terminal (D0-to-X2 or D1-to-Y1, see Note 3)	$V_{in(D0)} = V_{in(X2)} = 0$ to -18 V, $V_{in(D1)} = V_{in(Y1)} = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between address terminal and substrate	$V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		8†		pF
Capacitance between V_{DD} terminal and substrate	$V_{DD} = V_X = V_Y = 0$ to -18 V, f = 140 kHz, See Note 2		50†		pF
Read access time, t_{ar} (see Note 4)	See Figure 3, $R_L = 51\ \Omega$		30	60	ns

NOTES: **2. All capacitances are measured with all other elements ac grounded.**

3. Typical capacitance between digit-line terminals and all other address lines will be less than that shown for the adjacent address lines.

4. Read access time is the delay between the application of address voltages at the X and Y inputs and the availability of differential current between the digit lines.

†These typical values are the average for the voltage range 0 to −18 V.



NOTE: This timing diagram applies to a 2048-word-by-16-bit memory system composed of 128 TMS 4003 JR/NC memories.

FIGURE 2 – TYPICAL SYSTEM CYCLE TIME

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PARAMETER MEASUREMENT INFORMATION

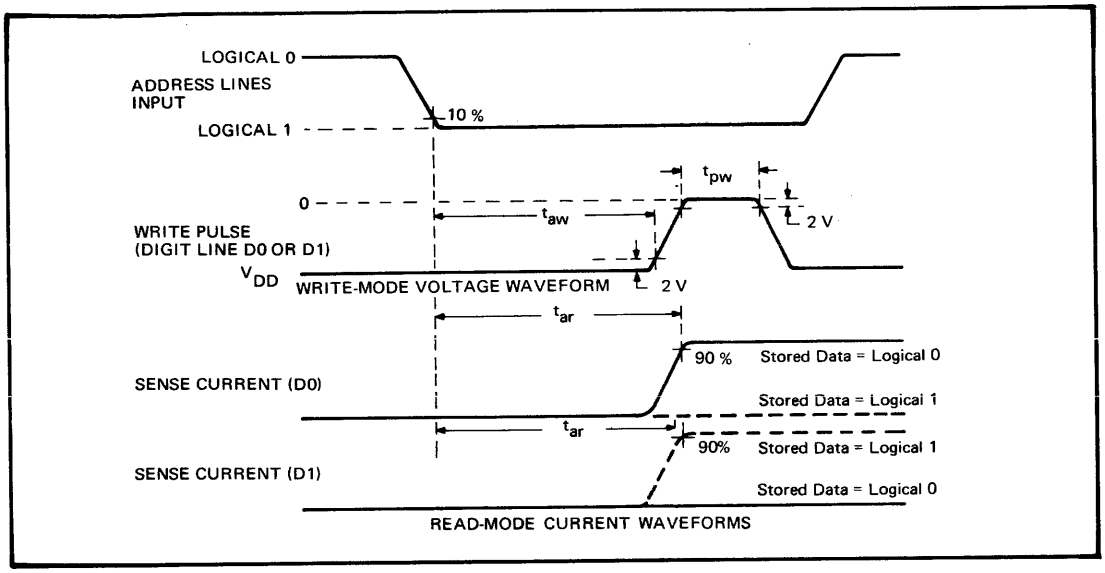

FIGURE 3 – TYPICAL SWITCHING WAVEFORMS

TYPICAL CHARACTERISTICS

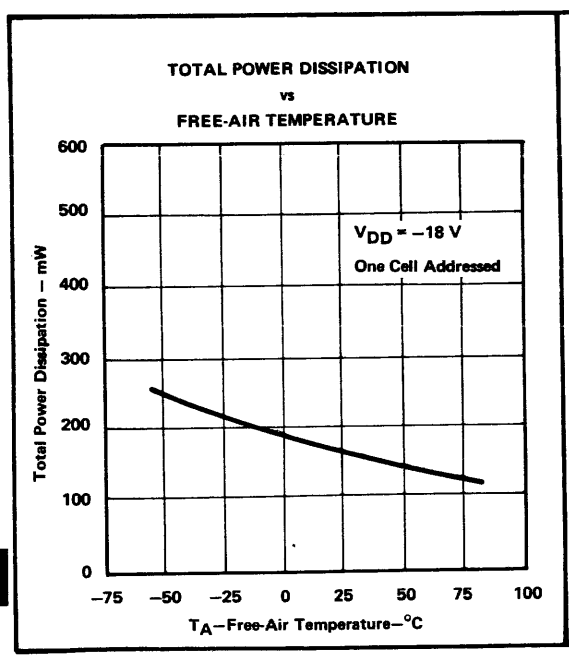

FIGURE 4

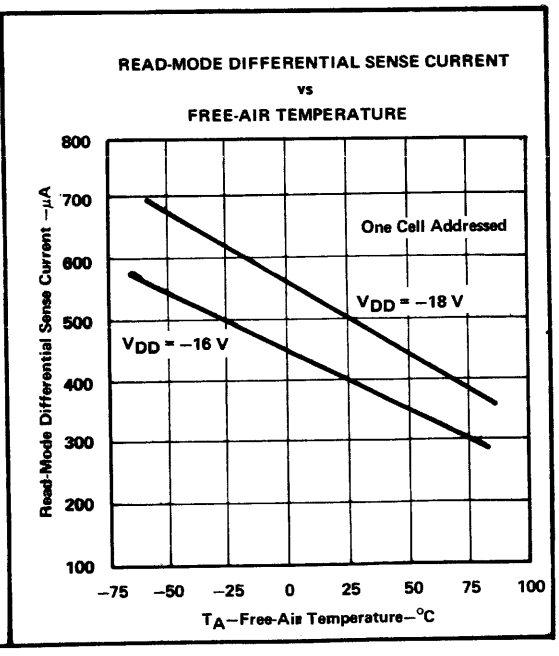

FIGURE 5

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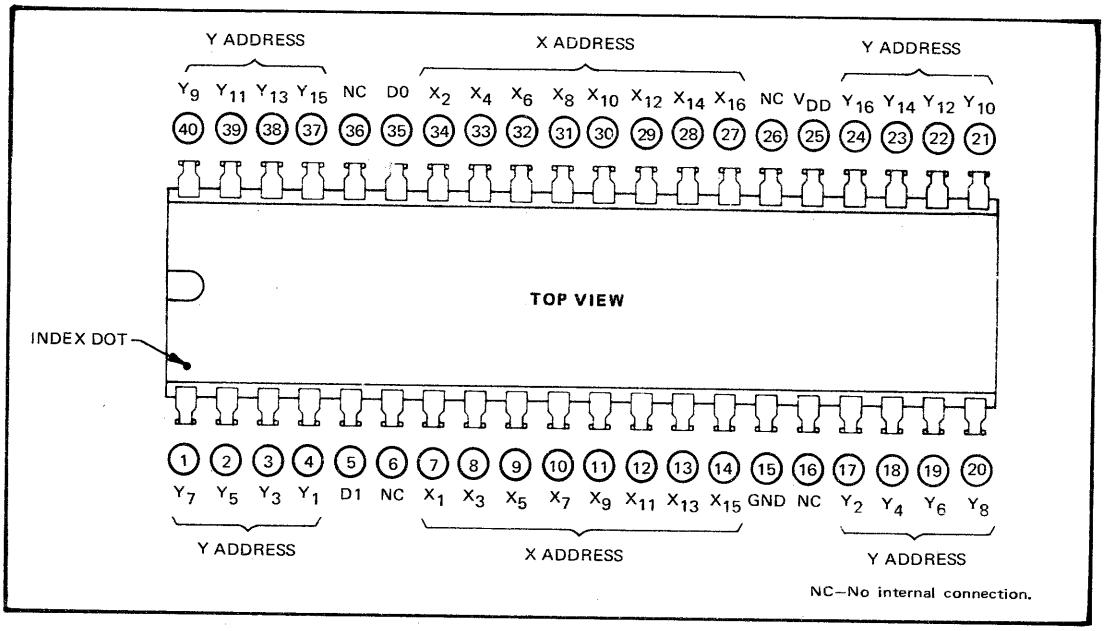
mechanical data and pin configuration

The device is available in both a 40-pin hermetically sealed ceramic dual-in-line package (TMS 4003 JR) and a 40-pin plastic dual-in-line package (TMS 4003 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



TYPICAL APPLICATION DATA

An actual negative supply for V_{DD} is not necessary. The V_{DD} terminal can be returned to system ground with a positive potential equal in magnitude to the voltage specified for V_{DD} applied to device ground (pin 15). This simplifies external circuitry, particularly when using bipolar systems such as TTL. The MOS device ground V_{SS}, is nominally +18 V while the V_{DD} terminal is at system ground. Addressing occurs when one X-address line and one Y-address line are pulled to ground. Unselected address lines should remain at V_{SS}.

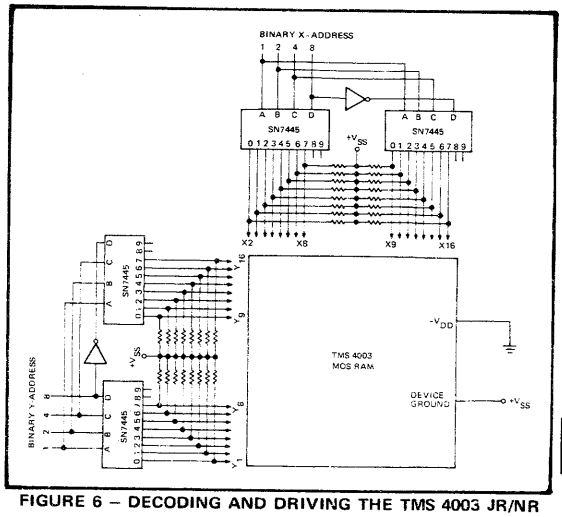


FIGURE 6 – DECODING AND DRIVING THE TMS 4003 JR/NR BY USE OF THE SN74154

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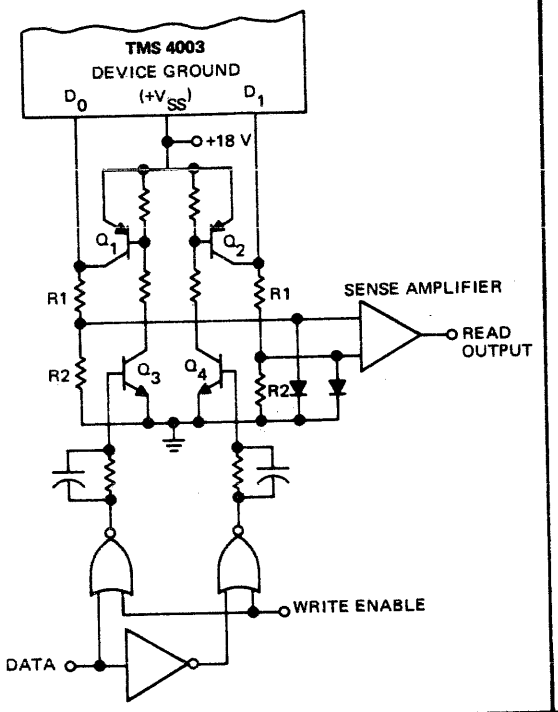
TYPICAL APPLICATION DATA (Continued)

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES

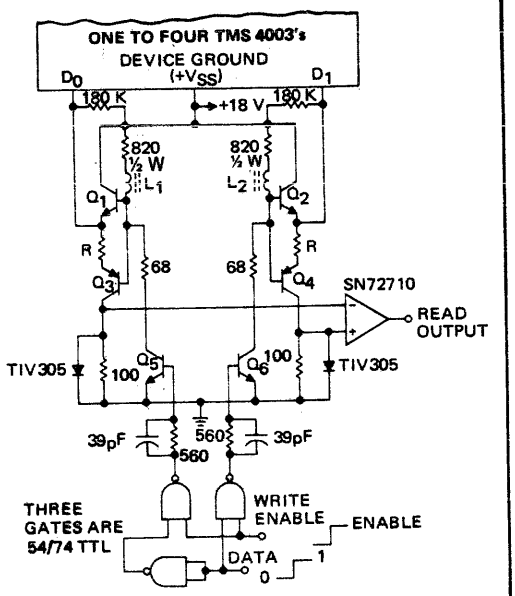


CIRCUIT COMPONENTS INFORMATION

Q1 and Q2: 2N3629
Q3 and Q4: 2N3014

FIGURE 7 – BASIC READ/WRITE CIRCUIT LIMITED TO LOW-SPEED OPERATION

TMS 4003 JR/NC MEMORIES WITH PARALLEL CONNECTED DIGIT LINES



CIRCUIT COMPONENTS INFORMATION

L1 and L2: 2 1/2 T, No. 30 wire on Ferrite Bead (Allen-Bradley No. T0 135G144A or equivalent)
Q1, Q2, Q5, and Q6: 2N3014
Q3 and Q4: 2N3829

$$\text{R1 and R2: } \frac{180\ \Omega}{\text{No. of TMS 4003 JR memories}}$$

FIGURE 8 – HIGH-SPEED READ/WRITE CIRCUIT

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TMS 4020 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

FEBRUARY 1971

features

- Low power dissipation
- Full decode
- Access time – 320 nsec max
- Cycle time – 640 nsec max
- High output-current capability (2 mA typ)
- Low-threshold technology
- 24-pin plastic package

description

The TMS 4020 NC is a 1024-word by 2-bit random-access memory, constructed on a single chip, with MOS P-channel enhancement-mode transistors. The device has two 1024-bit storage arrays with a 10-bit address decode common to both. There are four input chip selects – two for each array.

The address decode as well as the memory arrays are implemented with dynamic circuitry, thus enabling low power dissipation. Data stored in memory is nondestructively read. Refreshing of stored data is required every two milliseconds and refreshing the entire 2048 bits is accomplished with 16 Read cycles.

The outputs of the device are open ended, allowing several circuits to be wired-OR. The information read from the array is opposite in polarity to the write input.

The TMS 4020 NC is fabricated with a thick-oxide, low-threshold, self-aligned gate process.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The Precharge Cycle ϕ_1 is used to set up the dynamic decode logic for address selection, which occurs during Generate Time ϕ_2.

During the Generate Time ϕ_2 the address decode is propagated and the memory arrays are precharged. With the return of ϕ_2 to the most positive voltage, the propagation of selected X-rows (1 of 16) of both arrays is initiated. The information in the two bits selected by the Y decode is then available at the output in 100 nsec.

If a Read cycle is required, the data can be sampled at this time. An additional 100 nsec is required in the cycle to assure the completion of the refresh cycle. If a Write cycle is required, the Write strobe should be initiated 130 nsec after the termination of the Generate ϕ_2 signal concurrent with the new information being written. The remaining positions in the X-row (not being written into) will complete the refresh cycle.

All X-rows not read during a 2-msec period should be refreshed via Read cycle to assure the integrity of the data.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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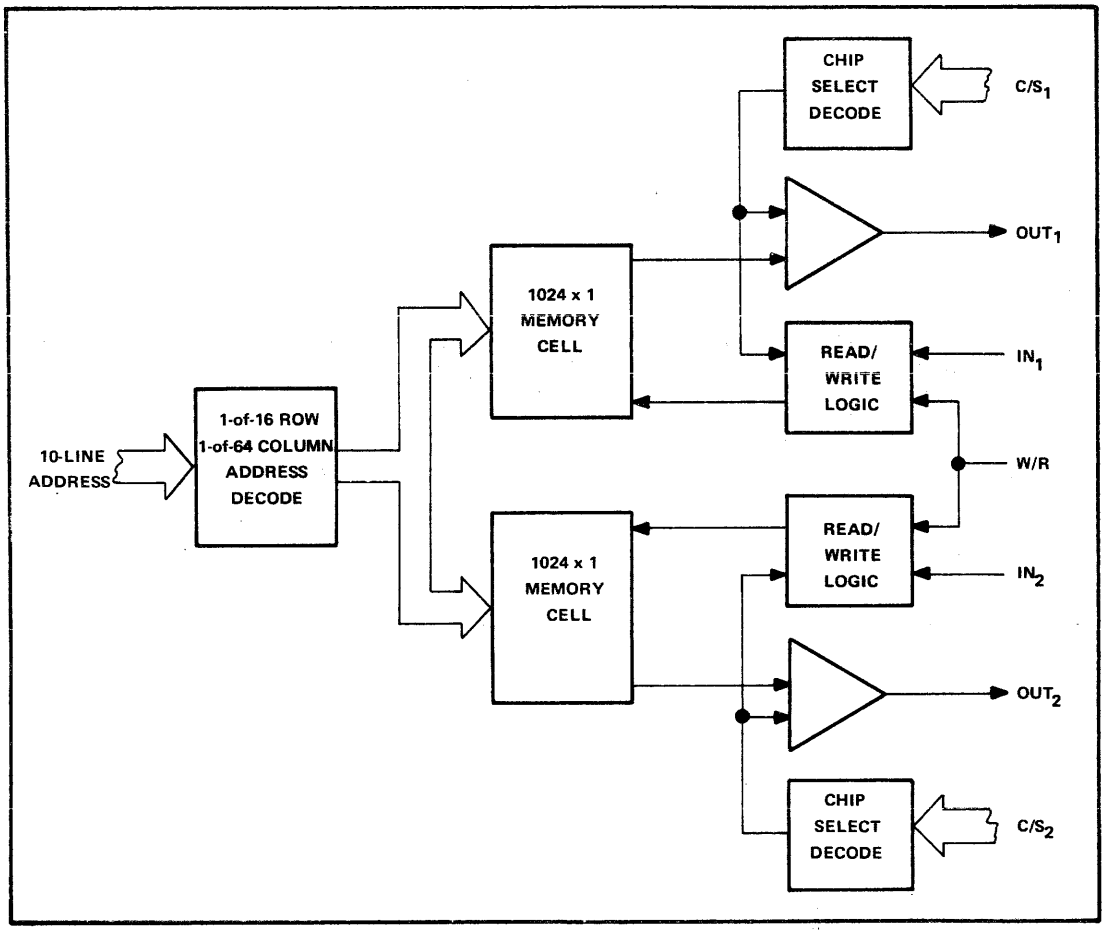
functional block diagram and pin configuration



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−25°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

TEXAS INSTRUMENTS
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recommended operating conditions (see note 2)

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Voltage V_{SUB}	1.5	2.0	2.5	V
Drain supply V_{DD}	−17	−16	−15	V
Logic Levels				
Input HIGH level V_{IH}	−1.5	0	+0.3	V
Input LOW level V_{IL}	−17	−16	−15	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	−1.0	0	+0.3	V
Clock LOW level $V_{\phi L}$	−17	−16	−15	V
Pulse Timing				
Pulse transition t_r, t_ϕ			1000	ns
Clock pulse width of ϕ_1 PW_1	90			ns
Clock pulse width ϕ_2 PW_2	170			ns
Clock delay from ϕ_1 to ϕ_2 P_{d1}	0			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Read and Refresh)	200			ns
Clock delay from ϕ_2 to ϕ_1 P_{d2} (Write)	310			ns
Address set-up time P_{AS}	0			ns
Address hold time P_{AH}	0			ns
ϕ_2-to-write pulse delay time P_{dW}	130			ns
Write pulse width P_{WW}	150			ns
Pulse Spacing				
Data set-up time P_{DS}	10			ns
Data hold time P_{DH}	10			ns
Chip select set-up time P_{CS}	0			ns
Chip select hold time P_{CH}	0			ns
Cycle time (Read and Refresh)	530			ns
Cycle time (Write)	640			ns
Strobe data width P_0	100			ns
Refreshing Time P_{REF}			2	ms

NOTE 2: These voltage values are with respect to V_{SS}.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Current					
$I_{OS(H)}$ Sense	Load = 100 Ω	1.2	2.0		mA
Output Leakage Current $I_{L(out)}$	V_{OUT} = −16 V			1	μA
Input (Load) Current $I_{L(in)}$	V_{IN} = −16 V			1	μA
Substrate Leakage Current I_{SUB}	V_{SUB} = +2 V			100	μA
Supply Current I_{DD}					
During PW_1			15	20	mA
During PW_2			26	34	mA
During P_{d2}			1.5	2	mA
Average Supply Current $I_{DD(AV)}$			13	18	mA

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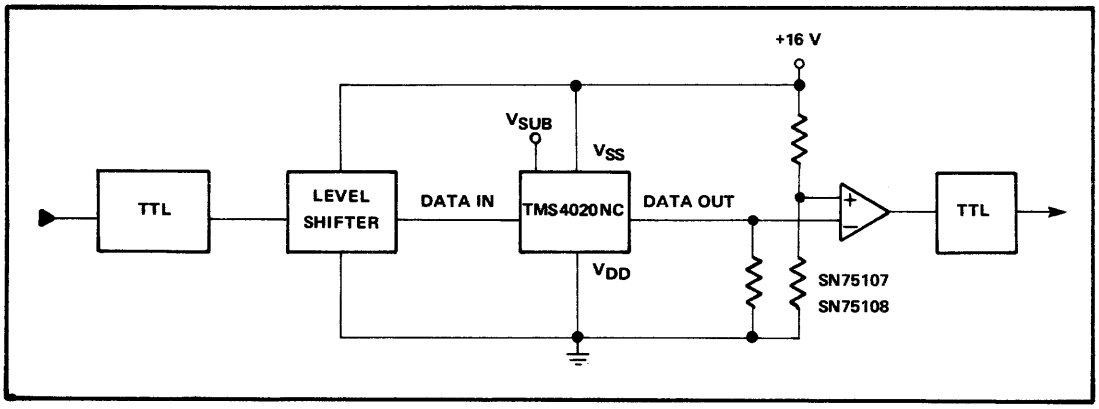
dynamic electrical characteristics (under nominal operating conditions from 0°C to +70°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
End of ϕ_2 to output delay P_{d0}	LOAD = 100 Ω		70	100	ns
Address to output access time P_{ACC1}	$I_{OS(HIGH)}$ = 0.8 mA min		290	320	ns
ϕ_1 to output access time P_{ACC2}	$I_{OS(LOW)}$ = 0.2 mA min		410	440	ns
Address Capacitance					
A_0 through A_3			8	11	pF
A_4 through A_8	F = 1 MHz at 25°C,		6	8	pF
A_9	$V_{AF} = V_{SS}$		4	6	pF
Clock Capacitance					
ϕ_1	F = 1 MHz,		18	22	pF
ϕ_2	$V_\phi = V_{SS}$ at 25°C		30	38	pF
Read/Write Capacitance					
Chips selected	F = 1 MHz,		27	33	pF
Chips not selected	$V_{R/W} = V_{SS}$ at 25°C		15	20	pF
Data Input Capacitance					
Chips selected	F = 1 MHz,		20	25	pF
Chips not selected	$V_{in} = V_{SS}$ at 25°C		5	7	pF
Data Output Capacitance					
Chips selected	F = 1 MHz,		8	12	pF
Chips not selected	$V_{out} = V_{SS}$ at 25°C		3	5	pF

TTL interface



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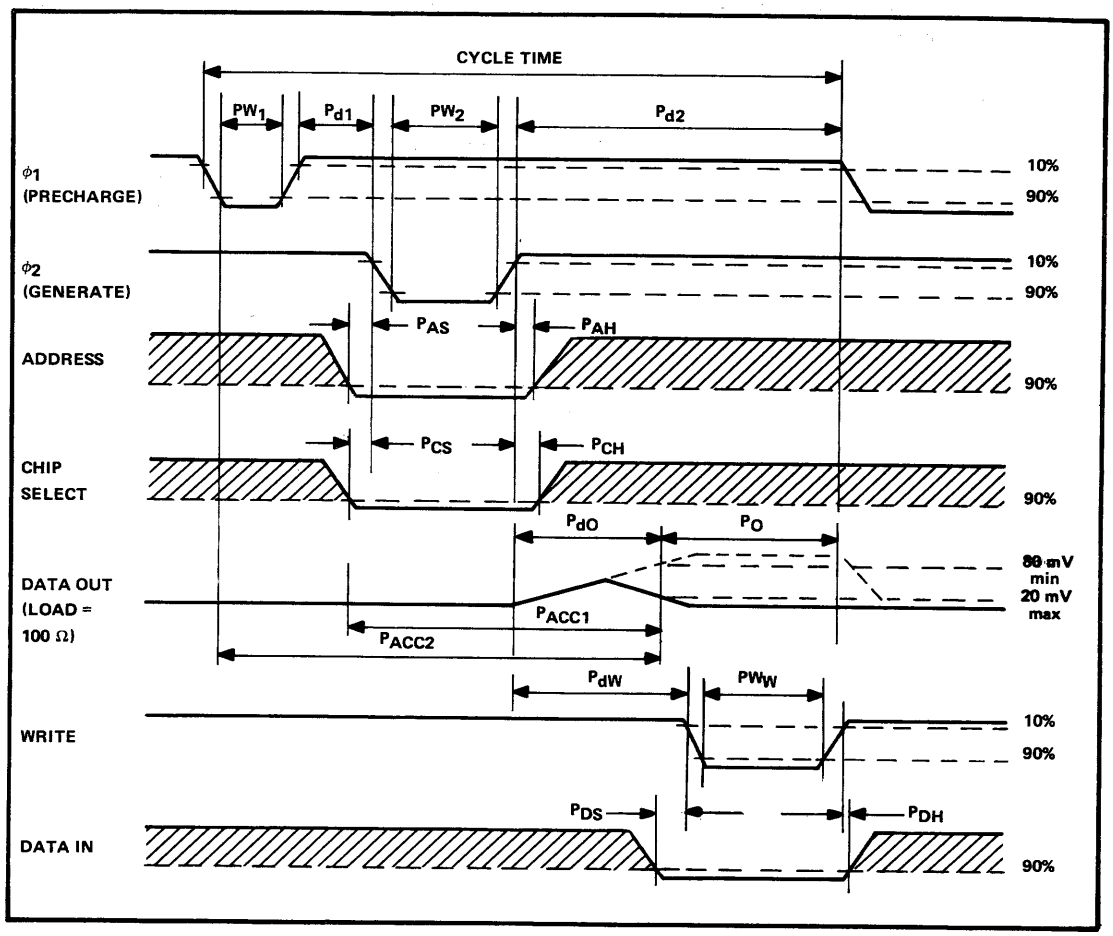
timing diagram and voltage waveforms



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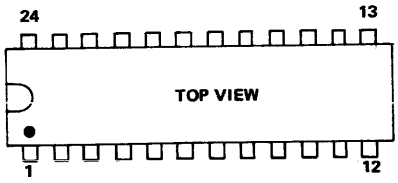
mechanical data

The TMS 4020 NC is mounted in a 24-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

pin configuration



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_6	13	A_1
2	A_5	14	A_0
3	A_4	15	ϕ_2
4	$\overline{IN_1}$	16	C/S_2
5	OUT_1	17	C/S_2
6	C/S_1	18	R/W
7	C/S_1	19	OUT_2
8	ϕ_1	20	$\overline{IN_2}$
9	A_3	21	A_9
10	A_2	22	A_8
11	V_{SUB}	23	A_7
12	V_{DD}	24	V_{SS}

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TMS 4023 NC
1024-BIT RANDOM-ACCESS MEMORY

FEBRUARY 1971

features

- Low power dissipation
- Access time – 650 nsec (maximum)
- Cycle time – 900 ns (maximum
- Refresh Period – 2 ms for 0°C–70°C
- Fully decoded
- Wired-OR capability
- Inputs fully protected
- 24-lead plastic package

description

The TMS 4023 NC is a 1024-bit RAM, organized as 1024 one-bit words, using P-channel enhancement-mode transistors. A fully decoded monolithic array, the device is available in a low-cost, standard, 24-pin dual-in-line plastic package. The dynamic memory has nondestructive readout and refreshes all 1024 bits in 32 read cycles (or 32 microseconds). The TMS 4023 NC is designed as a low-cost main-frame memory for large-storage high-performance operations.

logic definition

Negative logic is assumed.

a) LOGICAL 1 = most negative voltage

b) LOGICAL 0 = most positive voltage

operation (refer to functional block diagram and timing diagram)

A 10-bit address code selects any one of the 1024 bits for either Read or Write operation. A Read or Write operation may be performed with the application of a logic 1 on the chip-enable line. The memory is inhibited with the application of a logic 0 to the chip-select line. This renders the data Input/Output line open and ineffective, which allows wired-OR operation. The address decode is not inhibited however.

Application of a logic 0 to the Read/Write line will result in a Read operation. This may be presented simultaneously with or before application of the address code. Read-out is nondestructive.

A logic 1 applied to the Read/Write and chip enable will result in a Write operation. Duration of the Write command must be at least 560 nanoseconds to ensure that the data is written into memory.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (substrate).

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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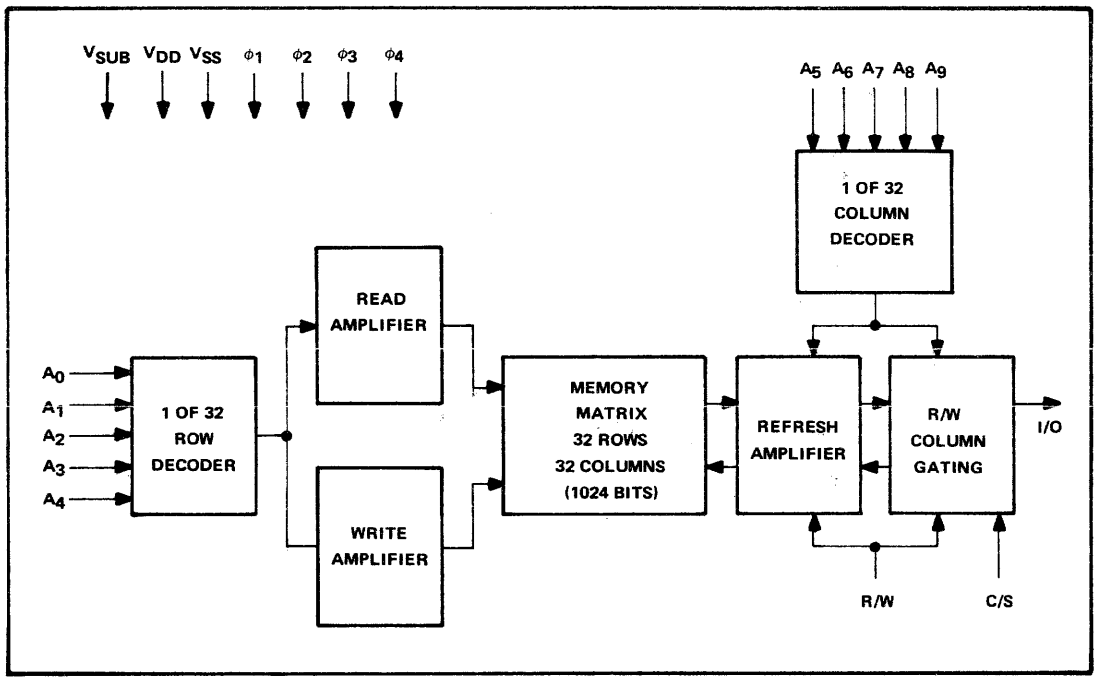
functional block diagram and pin configuration



recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage (See Note 1)				
Substrate Supply V_{SUB}	+1.5	+2.0	+2.5	V
V_{SS}		0		V
V_{DD}	−19	−20	−21	V
Logic Levels (See Note 1)				
Input HIGH level V_{IH}	−1.5		+0.3	V
Input LOW level V_{IL}	−19	−20	−21	V
Clock Voltage Levels (See Note 1)				
Clock HIGH level $V_{\phi H}$	−1.5		+0.3	V
Clock LOW level $V_{\phi L}$	−19	−20	−21	V
Pulse Timing				
Pulse widths				
Clock pulse width 1 $PW_{\phi 1}$	120			ns
Clock pulse width 2 $PW_{\phi 2}$	130			ns
Clock pulse width 3 $PW_{\phi 3}$	380			ns
Clock pulse width 4 $PW_{\phi 4}$	110			ns
Pulse Spacing				
Clock delay $t_{d\phi 1}$, $t_{d\phi 2}$, $t_{d\phi 3}$, $t_{d\phi 4}$	0			ns

NOTE 1: These voltage values are with respect to V_{SS}.

— continued

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recommended operating conditions (continued)

PARAMETER		MIN	NOM	MAX	UNITS
Pulse Spacing (continued)					
	Address setup t_{AS}	10			ns
	Address hold t_{AH}	10			ns
	Chip-select setup time t_{CS}	0			ns
	Chip-select hold time t_{CH}	0			ns
	R/W overlap C/S t_{WS} and t_{WH}	10			ns
	Data setup t_{DS}	10			ns
	Data hold t_{DH}	10			ns
Refreshing time T_{REF}				2	ms

static electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current						
	Substrate				100	μA
	Address Input				1	μA
	Clock Input				1	μA
C/S	Chip Select				1	μA
R/W	Read/Write				1	μA
I/O	Input/Output				1	μA
Output High Current						
I_{OS}	Sense	R_{LOAD} = 200 Ω	1.1			mA
Supply Current Drain						
I_{DD}	Drain Supply			1.0		mA

dynamic electrical characteristics (under recommended operating conditions and for T_A = 0°C to 70°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Cycle Time	C_{LOAD} = 100 pF, R_{LOAD} = 200 Ω, V_{REF} = 180 mV	900			ns
t_{OD}	Output Delay				350	ns
t_{ACC}	Access time (Note 2)	C_{LOAD} = 100 pF, R_{LOAD} = 200 Ω, V_{REF} = 180 mV		650		ns
t_{AD}	Available data on output		50			ns
Capacitance						
C_{IN}	Address Input			5	8	pF
$C_{\phi1}$, $C_{\phi2}$ $C_{\phi3}$, $C_{\phi4}$	Clock			17	20	pF
C/S	Chip Select			9	11	pF
R/W	Read/Write			8	10	pF
I/O	Input/Output					
	Chip Selected			24	27	pF
	Chip Not Selected			7	9	pF

NOTE 2: Access time is given for rise and fall times of input signals of no more than 15 ns.

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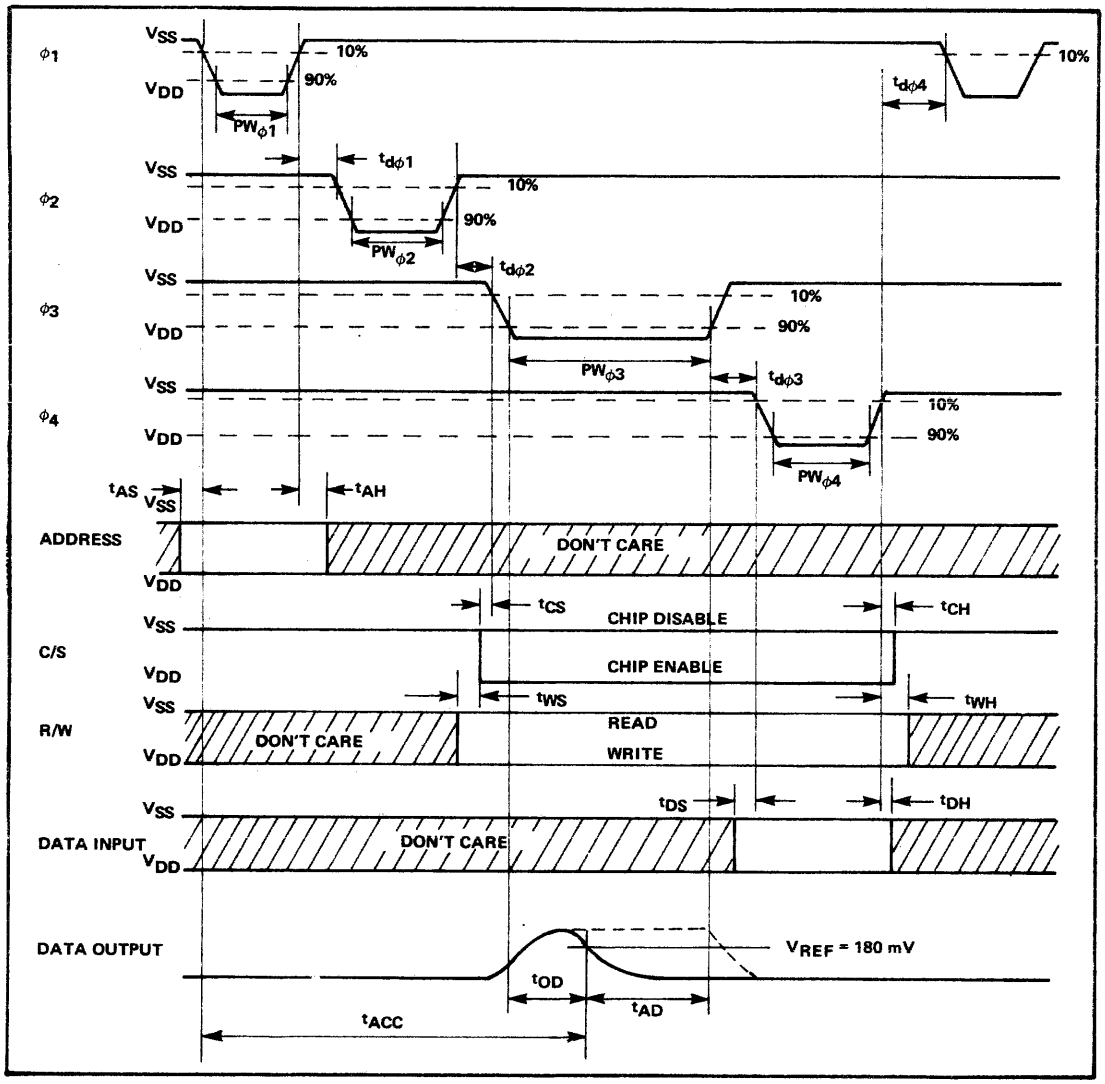
timing diagram and voltage waveforms



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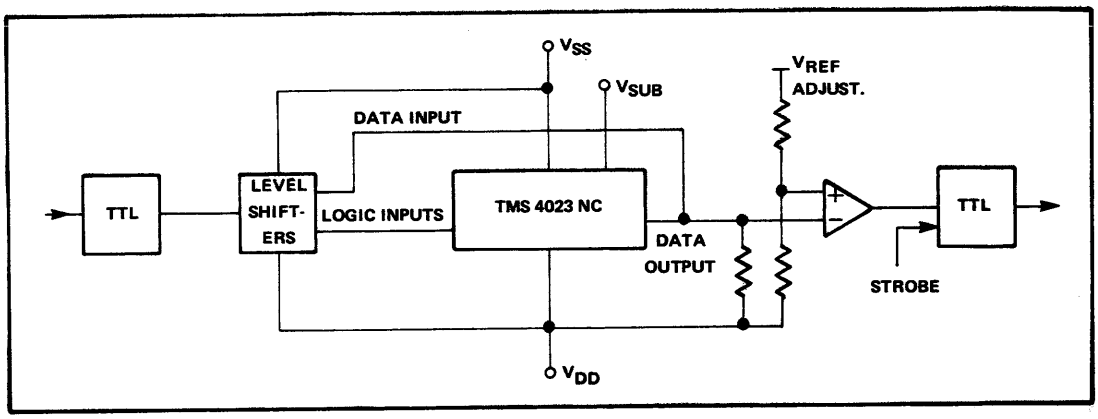
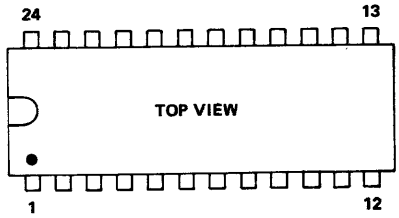
TTL interface



mechanical data and pin configuration

The TMS 4023 NC is mounted in a 24-pin dual-in-line plastic package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	–	13	–
2	A_9	14	I/O
3	A_8	15	C/S
4	A_7	16	R/W
5	V_{SS}	17	A_1
6	A_6	18	A_0
7	A_5	19	ϕ_3
8	A_4	20	V_{DD}
9	A_3	21	ϕ_4
10	A_2	22	ϕ_1
11	–	23	ϕ_2
12	–	24	V_{SUB}

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TMS 4025 NC
2048-BIT DYNAMIC RANDOM-ACCESS MEMORY

features

- Low power dissipation
- Full decode
- Access time – 280 nsec max
- Cycle time – 640 nsec max
- High output-current capability (2 mA typ)
- Low-threshold technology
- 24-pin plastic package

description

The TMS 4025 NC is a 1024-word by 2-bit random-access memory, constructed on a single chip, with MOS P-channel enhancement-mode transistors. The device has two 1024-bit storage arrays with a 10-bit address decode common to both. There are two input chip selects – one for each array.

The address decode as well as the memory arrays are implemented with dynamic circuitry, thus enabling low power dissipation. Data stored in memory is nondestructively read. Refreshing of stored data is required every two milliseconds and refreshing the entire 2048 bits is accomplished with 16 Read cycles.

The outputs of the device are open ended, allowing several circuits to be wired-OR. The information read from the array is opposite in polarity to the write input.

The TMS 4025 NC is fabricated with a thick-oxide, low-threshold, self-aligned gate process.

logic definition

Positive logic is assumed.

a) LOGICAL 1 = most positive voltage

b) LOGICAL 0 = most negative voltage

operation

The Precharge Cycle ϕ_1 is used to set up the dynamic decode logic for address selection, which occurs during Generate Time ϕ_2.

During the Generate Time ϕ_2 the address decode is propagated and the memory arrays are precharged. With the return of ϕ_2 to the most positive voltage, the propagation of selected X-rows (1 of 16) of both arrays is initiated. During the Read/Write time ϕ_3 the information in the two bits selected by the Y decode is then available at the output in 60 nsec.

If a Read cycle is required, the data can be sampled at this time. An additional 180 nsec is required in the cycle to assure the completion of the refresh cycle. If a Write cycle is required, the Write strobe should be initiated 90 nsec after the ϕ_3 signal concurrent with the new information being written. The remaining positions in the X-row (not being written into) will complete the refresh cycle.

All X-rows not read during a 2-msec period should be refreshed via Read cycle to assure the integrity of the data.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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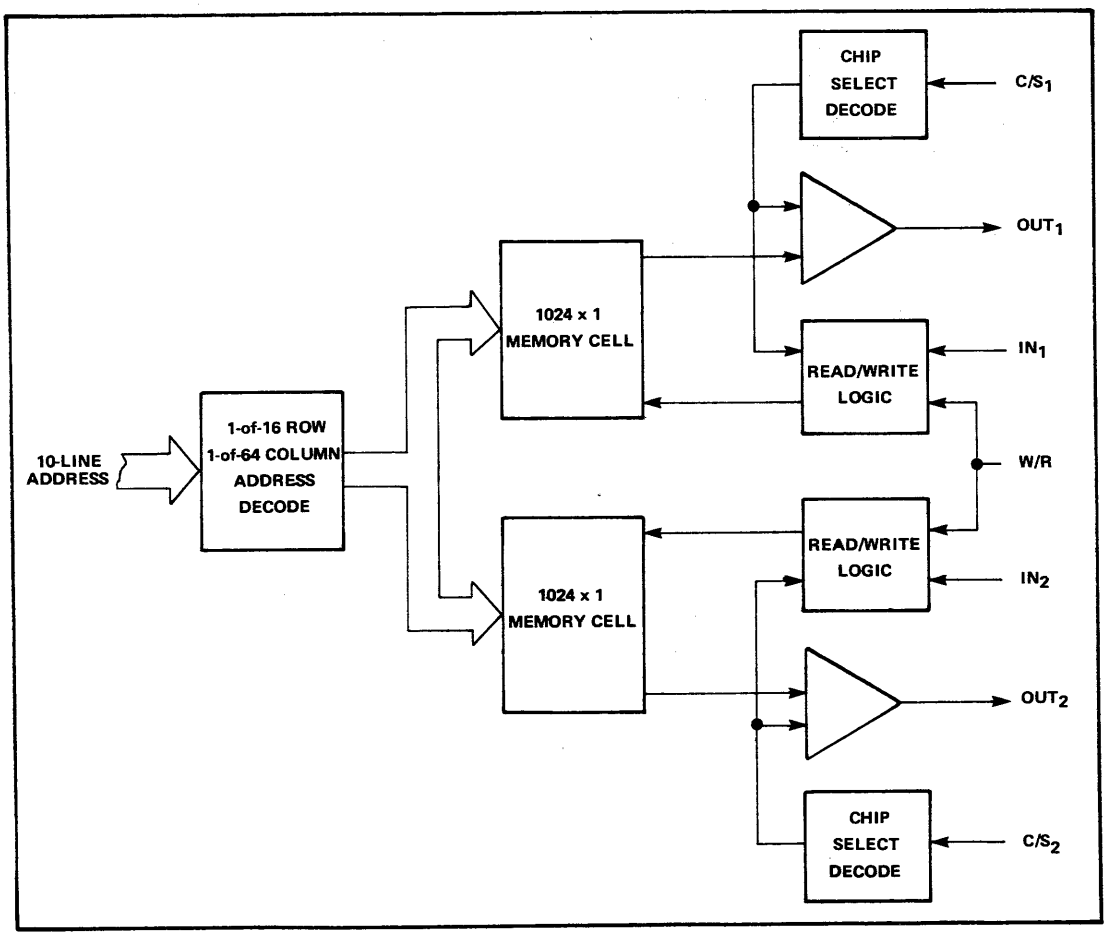
functional block diagram and pin configuration



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} and V_{SS} range (See Note 1)	−24 V to 0.3 V
Clock input voltage range (See Note 1)	−24 V to 0.3 V
Data input voltage range (See Note 1)	−24 V to 0.3 V
Operating free-air temperature range	−25°C to 70°C
Storage temperature range	−25°C to 150°C

NOTE 1: These voltage values are with respect to V_{SUB} (Substrate).

TEXAS INSTRUMENTS
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recommended operating conditions (see note 2)

PARAMETER	MIN	NOM	MAX	UNITS
Operating Voltage				
Substrate Voltage V_{SUB}	1.5	2.0	2.5	V
Drain supply V_{DD}	−17	−16	−15	V
Logic Levels				
Input HIGH level V_{IH}	−1.5	0	+0.3	V
Input LOW level V_{IL}	−17	−16	−15	V
Clock Voltage Levels				
Clock HIGH level $V_{\phi H}$	−1.0	0	+0.3	V
Clock LOW level $V_{\phi L}$	−17	−16	−15	V
Pulse Timing				
Pulse transition t_r, t_ϕ			1000	ns
Clock pulse width of ϕ_1 PW_1	90			ns
Clock pulse width of ϕ_2 PW_2	170			ns
Clock pulse width of ϕ_3 PW_3				
(READ and REF)	220			ns
(WRITE)	280			ns
Clock delay from ϕ_1 to ϕ_2 P_{d1}	0			ns
Clock delay from ϕ_2 to ϕ_3 P_{d2}	0			ns
Clock delay from ϕ_3 to ϕ_1 P_{d3}	0			ns
Address set-up time P_{AS}	0			ns
Address hold time P_{AH}	0			ns
ϕ_3-to-write pulse delay time P_{dW}	90			ns
Write pulse width P_{WW}	150			ns
Pulse Spacing				
Data set-up time P_{DS}	10			ns
Data hold time P_{DH}	10			ns
Chip select set-up time P_{CS}	0			ns
Chip select hold time P_{CH}	0			ns
Cycle time (Read and Refresh)	580			ns
Cycle time (Write)	640			ns
Strobe data width P_0	150			ns
Refreshing Time P_{REF}			2	msec

NOTE 2: These voltage values are with respect to V_{SS}.

static electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Current Sense $I_{OS(H)}$	Load = 100 Ω	1.2	2.0		mA
Output Leakage Current $I_{L(OUT)}$	V_{OUT} = −16 V			1	μA
Input (Load) Current $I_{L(IN)}$	V_{IN} = −16 V			1	μA
Substrate Leakage Current I_{SUB}	V_{SUB} = +2 V			100	μA
Supply Current I_{DD}					
during PW_1			3	5	mA
during PW_2			6	9	mA
during PW_3			2.5	4	mA
Average Supply Current $I_{DD(AV)}$			3.5	6	mA

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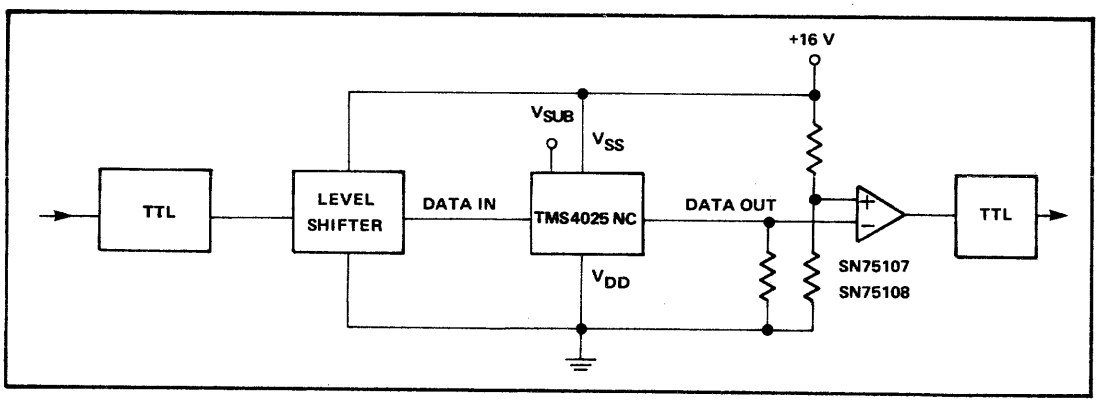
dynamic electrical characteristics (under nominal operating conditions from 0°C to 70°C unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
End of ϕ_2 to output delay P_{d0}	Load = 100 Ω		45	60	ns
Address-to-output access time P_{ACC1}	$I_{OS(HIGH)}$ = 0.8 mA min,		265	280	ns
ϕ_1-to-output access time P_{ACC2}	$I_{OS(LOW)}$ = 0.2 mA min		385	400	ns
Address Capacitance					
A_0 through A_3	F = 1 MHz at 25°C,		8	11	pF
A_4 through A_8	$V_A = V_{SS}$		6	8	pF
A_9			4	6	pF
Clock capacitance ϕ_1			18	22	pF
Clock capacitance ϕ_2	F = 1 MHz, $V_\phi = V_{SS}$ at 25°C		30	38	pF
Clock capacitance ϕ_3			35	42	pF
Read/Write Capacitance					
Chips selected	F = 1 MHz,		27	33	pF
Chips not selected	$V_{R/W} = V_{SS}$ at 25°C		15	20	pF
Data Input Capacitance					
Chips selected	F = 1 MHz,		20	25	pF
Chips not selected	$V_{in} = V_{SS}$ at 25°C		5	7	pF
Data Output Capacitance					
Chips selected	F = 1 MHz,		8	12	pF
Chips not selected	$V_{out} = V_{SS}$ at 25°C		3	5	pF

TTL interface



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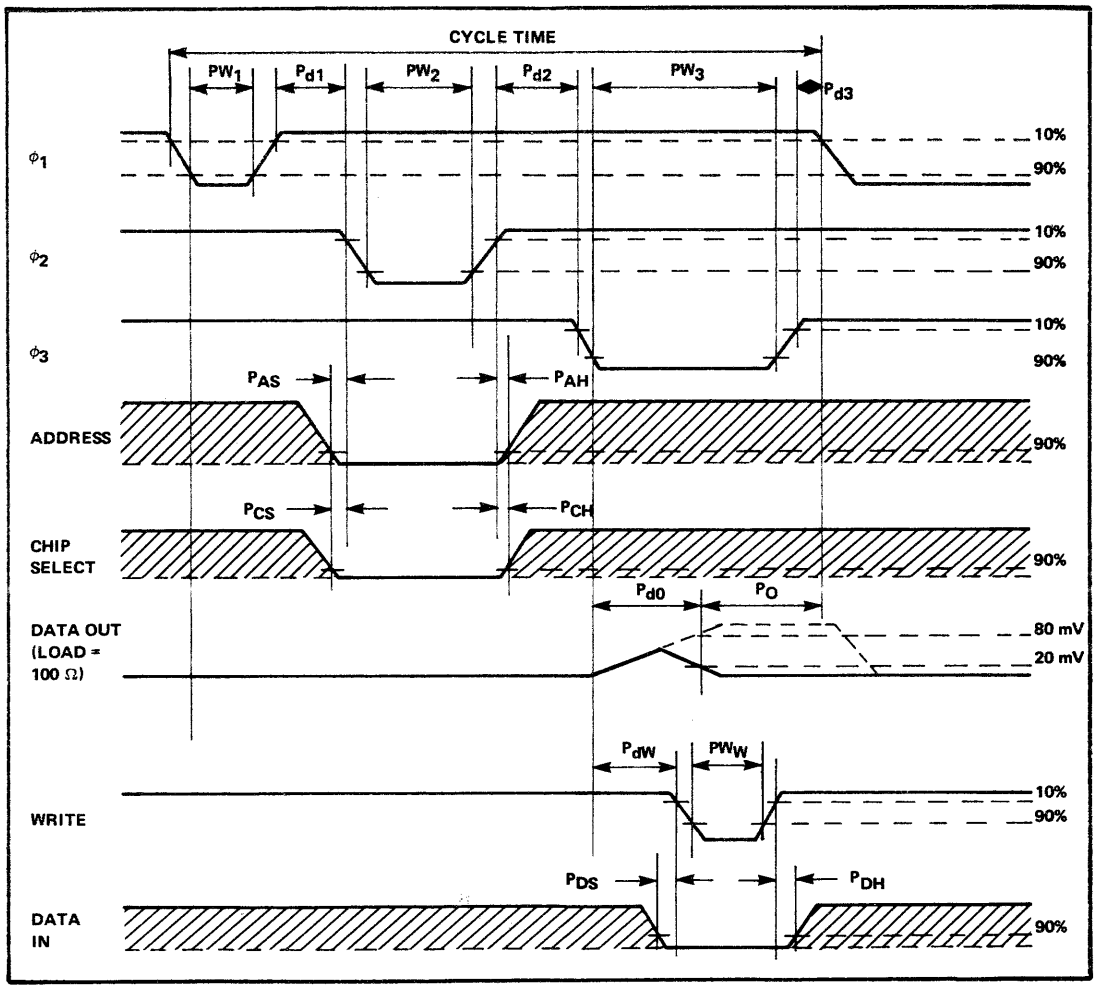
timing diagram and voltage waveforms

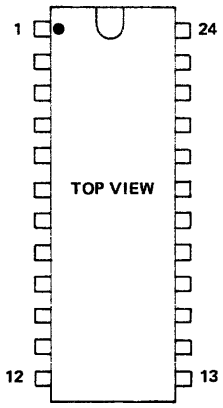


mechanical data

The TMS 4025 NC is mounted in a 24-pin plastic dual-in-line package, designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

— continued

mechanical data (continued)



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	A_6	13	A_1
2	A_5	14	A_0
3	A_4	15	ϕ_2
4	$\overline{IN_1}$	16	NC
5	ϕ_3	17	C/S_2
6	OUT_1	18	R/W
7	C/S_1	19	OUT_2
8	ϕ_1	20	$\overline{IN_2}$
9	A_3	21	A_9
10	A_2	22	A_8
11	V_{SUB}	23	A_7
12	V_{DD}	24	V_{SS}

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This section presents special-purpose devices produced by TI.

1) Analog Switches

The MOS transistor takes its place among the many techniques available to the designer for analog switching, which include:

- Mechanical choppers
- Bipolar transistors
- FETs
- Photoelectrical devices

It has several definite advantages over other techniques:

a) If there is no activating signal, the resistance between drain and source is extremely large and all inputs are insulated.

b) The MOS transistor is completely symmetrical with respect to its source and drain (the more positive terminal is called the source). Depending on the voltage applied, either side of the transistor can act as source or drain.

c) The gate of the transistor is completely insulated and does not draw current.

TI presently manufactures the following devices.

TMS 6000 JC/NC	10-channel common-source analog switch
TMS 6002 JC/NC	6-channel common-drain analog switch
TMS 6005 JC/NC	6-channel common-source analog switch
TMS 6009 JC/NC	6-channel common-source analog switch

2) Digital-Storage Buffers

The TMS 4006 JC is a first-in first-out store, particularly useful in communication applications. It allows the user to buffer digital information coming from a transmission line.

TMS 4006 JC, TMS 4006 NC
DIGITAL STORAGE BUFFER

features

- Asynchronous input and output clocks
- Serial or parallel input capability
- No minimum clock rate (long-term storage)
- Low output impedance
- Double-ended buffer
- 28-pin CDIP or dual-in-line plastic package
- Memory expansion by cascading units

description

The TMS 4006 JC/NC is a data storage register with a capacity of 11 or 13 words of 6 bits each. It performs storage on a first-in first-out basis. The device employs a method of storage commonly referred to as "silo" mode.

Input and output of the digital storage buffer operate entirely independently. A word is transferred into the TMS 4006 JC/NC on the positive-going edge of the data input clock (DIC). A word is transferred out of the register on the positive going edge of the data output clock (DOC).

The input and output clocks are completely independent of each other. There is no minimum clock rate. Logic used in the TMS 4006 JC/NC is purely static and the device has long-term retention.

Once a character is entered it will be stored temporarily in the first available register. A control logic associated with the next register will indicate whether or not that register already contains a valid word. If the next register is full, the input word will stay in the first register. If the next register is empty the word will fall down in parallel and be transferred. This operation will be repeated time after time until a full register is met. The operation is completely independent of the input, output clocks, and of all terminals.

The input word can be loaded either in serial or in parallel.

To load the device in parallel, the serial parallel (S/P) control must be at a logic 1.

To load in serial, the S/P control must be at a logical 0. A marker bit will be loaded concurrently with the first shift pulse (data input clock). This marker bit will be a logical 0. In serial mode the input word will then be 7 bits (1 marker bit and 6 data bits). Parallel inputs should be held at less than −10 volts or left floating. In parallel operation, the serial input should be held greater than −1.5 volts or left floating.

The TMS 4006 JC/NC can store 11 words when operating in the serial mode and 13 words when operating in the parallel mode.

When in serial mode a word cannot be "all zero"; at least one of the data bits must be a 1.

Several outputs will allow the user to find out how much data is stored in the TMS 4006 JC/NC:

A Flag 1 output will indicate whether the first (first-in word) register is full.

A Flag 10 output will indicate whether the 10th register is full.

A Flag 13 output will indicate whether the 13th register is full.

Flag outputs may be used to generate a readout command when a certain number of registers are full.

An ADIS (any data-in storage) output allows the user to detect lock-up, which may occur if power supplies are disconnected. Different outputs on ADIS and Flag 1 indicate lock-up. The register must then be cleared.

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description (continued)

A Clear input will allow the user to clear all the registers of the TMS 4006 JC/NC simultaneously.

TMS 4006 JC/NC can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: a next-register input clock (NRC), which provides the input clock signal to the next register in a cascaded string, and a previous-register output clock (PRC) which provides the output clock signal to the previous register in a cascaded string.

"TMS 4006 JC" is the part number for a unit mounted in a 28-pin ceramic dual-in-line package. In a 28-pin plastic package the device is numbered "TMS 4006 NC".

operation

Transferring data into the device occurs on the positive-going edge of DIC. Output data appears on the positive-going edge of the DOC and resets to one on the negative-going edge of the DOC.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{DD} range* . . . . . −30 V to 0.3 V
Supply voltage V_{GG} range* . . . . . −30 V to 0.3 V
Clock and data input voltage ranges* . . . . . −30 V to 0.5 V
Operating free-air temperature ranges . . . . . −25°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

* These voltages are with respect to network ground terminal.

recommended operating conditions

CHARACTERISTICS	MIN	NOM	MAX	UNIT
Supply voltage V_{GG}	−23	−24	−28	V
Supply voltage V_{DD}	−13	−14	−18	V
Data input voltage				
$V_{in(0)}$ logical 0	0	−2.0	−3.0	V
$V_{in(1)}$ logical 1	−11	−12	−16	V
Clock input voltage				
$V_{\phi(0)}$ logical 0	0	−2.0	−3.0	V
$V_{\phi(1)}$ logical 1	−11	−12	−16	V
S/P input				
Serial mode	−0.3	0	−1.5	V
Parallel mode	−23	−24	−28	V
Clear command				
Logical 0	+0.3	0	−1.5	V
Logical 1	−23	−24	−28	V
Marker bit for serial input	0	−2.0	−3.0	V
Width of data pulse $t_{p(data)}$†	10			μsec
Rise-time of clock pulses, $t_{r(clock)}$†			2	μsec
Fall-time of clock pulses, $t_{f(clock)}$†			2	μsec
Clock repetition rate†	0		25.0	kHz
Width of clock pulses, $t_{p(clock)}$†	5			μsec
Overlap of data to clock, t_{OV}†	0	1.0		μsec

† See Timing Diagram

NOTE: Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies.

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electrical characteristics (under nominal operating conditions at 25°C unless otherwise specified)

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage		−11		−16	V
$V_{out(0)}$	Logical 0 output voltage		−2.0	−2.5	−3.0	V
Z_{out}	Output impedance	V_{out} = 0 to 3 V		700	1000	Ω
	All flag outputs*	$R_L \leq$ 50 kΩ to GND	45			μA
PRC (1)	Previous register clock logical 1 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−8	−10	−12	V
PRC (0)	Previous register clock logical 0 level	$R_L \geq$500 kΩ to GND, $C_L \leq$20 pF	−2.0	−2.5	−3.0	V
NRC (1)	Next register clock logical 1 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−8	−10	−12	V
NRC (0)	Next register clock logical 0 level	$R_L \geq$500 kΩ to GND $C_L \leq$20 pF	−2.0	−2.5	−3.0	V
$I_{in(1)}$	Logical 1 level input leakage current	V_{in} = −15 V, V_{DD} = 0 V, V_{GG} = 0 V			6.0	μA
$I_{in(1)\phi}$	Logical 1 level input leakage current into the clock input	$V_{in\phi}$ = −20 V, V_{DD} = 0 V, V_{GG} = 0 V			10.0	μA
C_{in}	Capacitance of data input	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
$C_{in\phi}$	Capacitance of clock inputs	V_{in} = 0 V, T_A = 25°C, $F_{(clock)}$ = 25 kHz		3.0	5.0	pF
I_{DD}	Supply current into V_{DD} terminal	V_{DD} = −14 V, V_{GG} = −24 V		20	30	mA
I_{GG}	Supply current into V_{GG} terminal	V_{DD} = −14 V, V_{GG} = −24 V		4	10	mA
	Power dissipation			250		mW

* Includes SYNC, 1st Flag, 10th Flag, 13th Flag and ADIS.

switching characteristics

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pd0}	Propagation delay time to logical 0 level from DIC to appearance of data at output of empty register (13 register levels of delay)	(See Timing Diagram)		5	7	μsec
t_{pda}	Propagation delay time to Flag 10 turn-on from DIC to appearance of data at level 10 (4 register levels of delay).	(See Timing Diagram)		1	2	μsec
t_{pdb}	Propagation delay time to Flag 10 turn-off from DOC to disappearance of data at level 10 (10 register levels of delay)	(See Timing Diagram)		3	5	μsec
t_{pdc}	Propagation delay time to Flag 13 turn-off from DOC to disappearance of data at level 13 (13 register levels of delay).	(See Timing Diagram)		5	7	μsec

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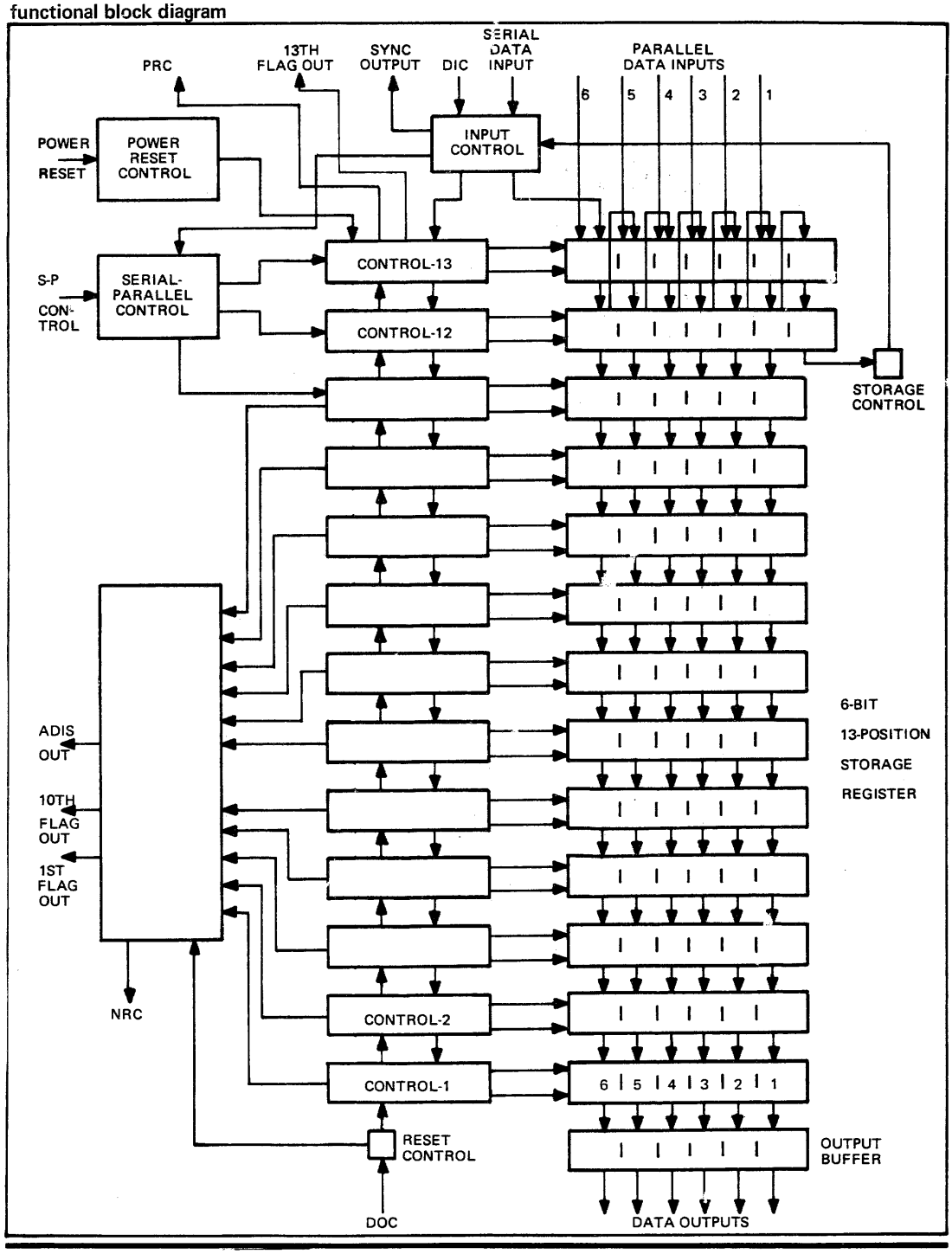
functional block diagram



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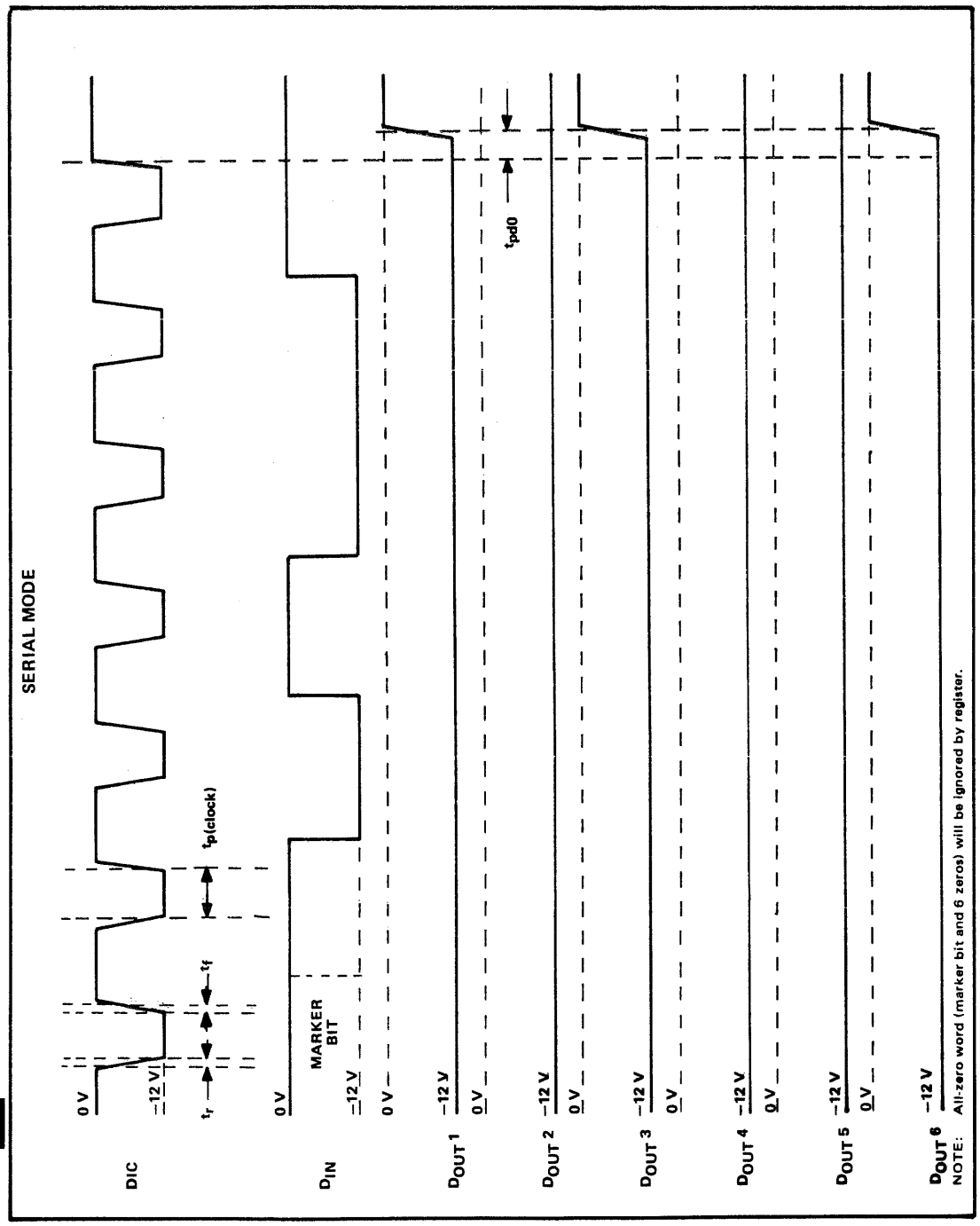
timing diagram and waveforms



NOTE: All-zero word (marker bit and 6 zeros) will be ignored by register.

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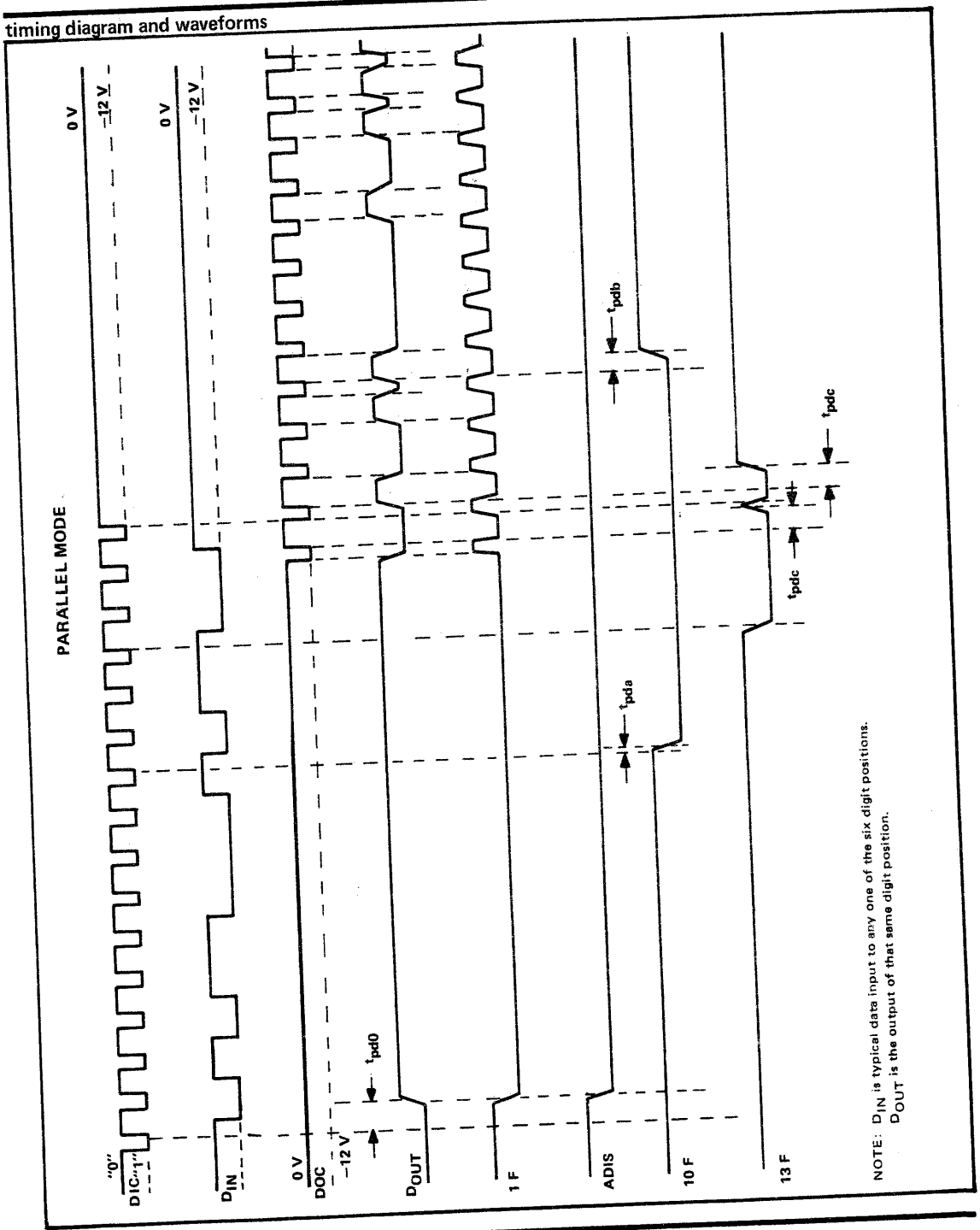
timing diagram and waveforms



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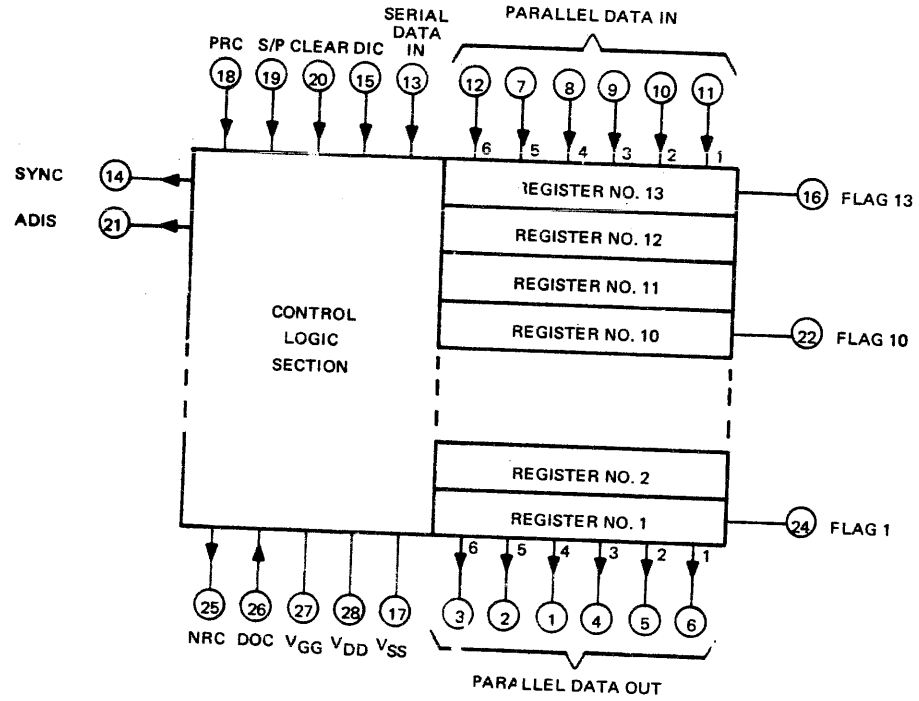
TMS 4006 JC, TMS 4006 NC
DIGITAL STORAGE BUFFER

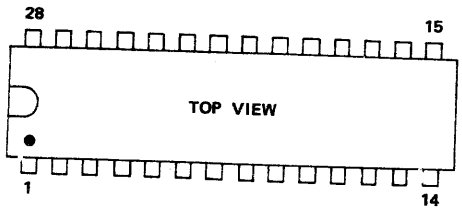
mechanical data

The digital storage buffer is available in both a 28-pin hermetically sealed dual-in-line package (TMS 4006 JC) and a 28-pin dual-in-line plastic package (TMS 4006 NC). The package is designed for insertion in mounting hole rows on 0.600-inch centers. (See MOS/LSI packaging section.).

pin configuration



PRC	–	PREVIOUS-REGISTER CLOCK
NRC	–	NEXT-REGISTER CLOCK
ADIS	–	ANY DATA IN STORAGE
S/P	–	SERIAL/PARALLEL CONTROL
DIC	–	DATA-INPUT CLOCK
DOC	–	DATA-OUTPUT CLOCK
V_{SS}	–	SUBSTRATE
V_{DD}	–	DRAIN POWER SUPPLY
V_{GG}	–	GATE POWER SUPPLY



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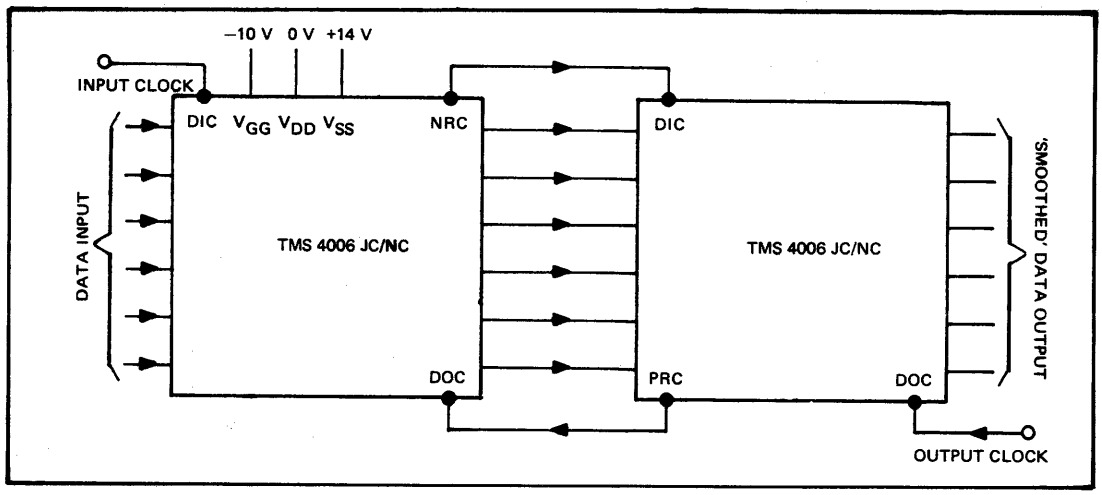
memory expansion

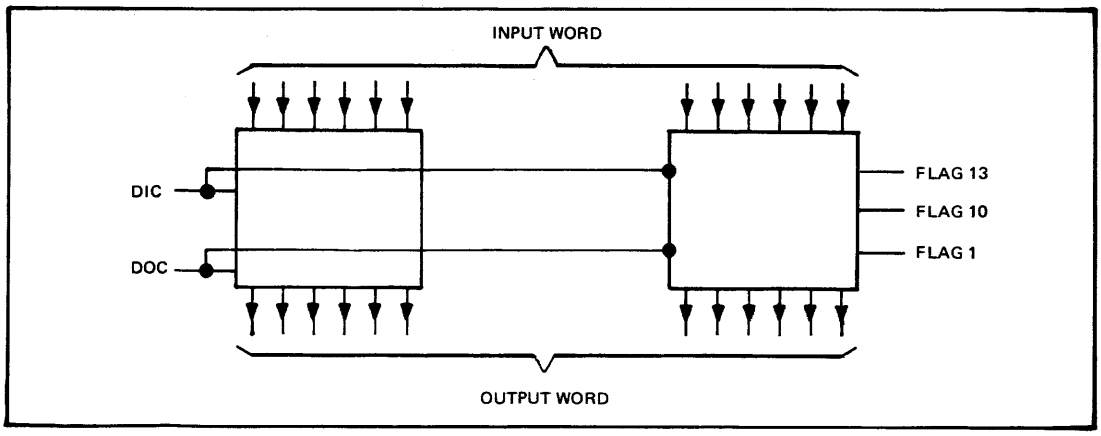
DSBs can be connected in cascade or in parallel to extend system storage capacity in increments of six digits and/or 13 characters. To extend the character positions, two controls are provided: an NRC which provides the input clock signal to the next register in a cascaded string, and a PRC which provides the output clock signal to the previous register in a cascaded string. There is no limit, in terms of performance, to the number of registers in a cascaded string. To extend the digit positions, the input and output control signals of a number of registers are tied in parallel. N registers tied in this fashion to store 6N digit characters can only accept characters serially in 6-bit sub-characters with the restriction that a marker pulse must proceed each 6-bit sub-character. There are no restrictions on input character format in the parallel mode.

a) Cascading



Digital storage buffers can be cascaded very simply to provide extra capacity since all the control clocks and gating are generated internally permitting direct connection of one DSB to the next.

b) Paralleling



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MOS
LSI

TMS 6000 JR, TMS 6000 NC
COMMON-SOURCE 10-CHANNEL ANALOG SWITCH

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line package
- $R_{DS(ON)}$ = 200 Ω

description

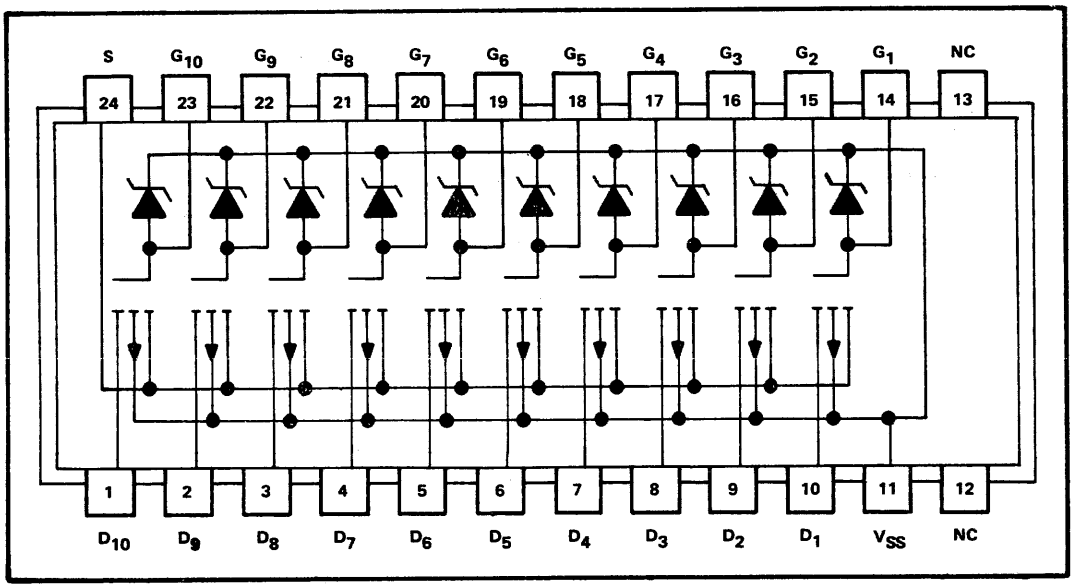
The TMS 6000 JR/NC analog switch is a P-channel enhancement-mode MOS monolithic integrated circuit, designed for high-speed multiplexing applications. It consists of ten MOS transistors having all ten sources interconnected.

A gate input impedance greater than 10^{10} ohms coupled with low-source-cutoff current, zero inherent offset voltage, and low on-state resistance ideally suits these switches for time-division multiplexing of analog and digital signals.

"TMS 6000 JR" designates a unit mounted in a 24-pin hermetically sealed ceramic dual-in-line package, and "TMS 6000 NC" is the part number for a unit mounted in a 24-pin dual-in-line plastic package.

schematic and pin configuration

TOP VIEW



D = Drain G = Gate S = Source V_{SS} = Substrate NC = No Connection

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Drain-source voltage	−30 V
Gate-source voltage	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Operating free-air temperature range	−55°C to 85°C
Storage temperature range	−55°C to 150°C

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electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$,	$V_{GS} = 0$ V	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$,	$V_{DS} = 0$ V	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$,	$V_{GD} = 0$ V	−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V,	$V_{DS} = 0$ V		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V,	$V_{GS} = 0$ V			−3	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V,	$V_{GD} = 0$			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DS} = 0$ V,	$I_D = -10\ \mu A$	−2.5	−4	−6	V
$r_{DS(on)}$	Static-drain-source on-state resistance	$V_{GS} = -20$ V,	$I_D = -100\ \mu A$		140	200	Ω
$\lvert Y_{fs} \rvert$	Small-signal common-source forward transadmittance	$V_{DS} = -10$ V, f = 1 kHz	$V_{GS} = -10$ V,		3		mmho
$C_{(in)}$	Input capacitance (See Note 1)	$V_{DS} = -5$ V,	$V_{GS} = 0$ V		4	7	pF
$C_{(out)}$	Output capacitance (See Note 2)	$V_{SD} = -5$ V, f = 1 MHz	$V_{GS} = -5$ V,		13	20	pF
C_{gs}	Gate-source capacitance (See Note 3)	$V_{DS} = 0$ V, f = 1 MHz	$V_{GS} = 0$ V,		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 3)	$V_{DS} = 0$ V, f = 1 MHz	$V_{GS} = 0$ V		2	3	pF
$t_{d(on)}$	Turn on delay time	See Switching Circuit			22	33	ns

NOTES: 1. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
2. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
3. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate, respectively, are connected to the guard terminal of the bridge.

mechanical data

This device is available in both a 24-pin hermetically sealed ceramic dual-in-line package (TMS 6000 JR) and a 24-pin plastic package (TMS 6000 NC). The packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

switching characteristics

PARAMETER MEASUREMENT INFORMATION

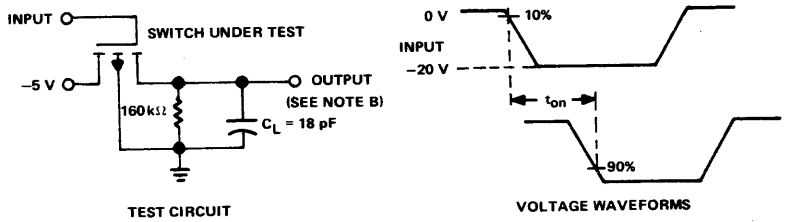

FIGURE 1

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leqslant 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leqslant 10$ ns, $R_{in} \geqslant 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS

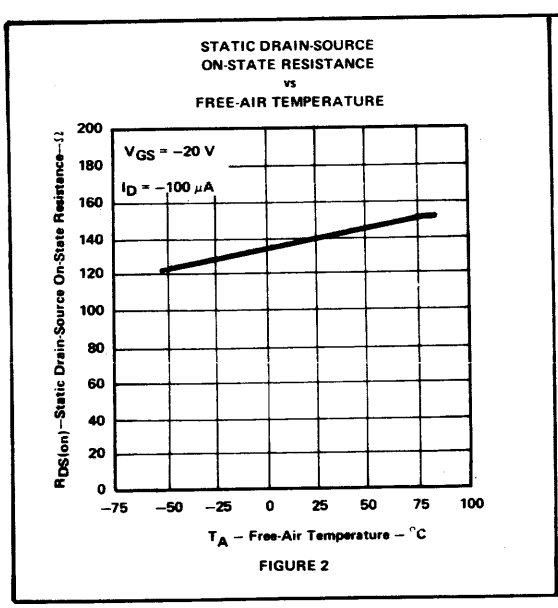

FIGURE 2

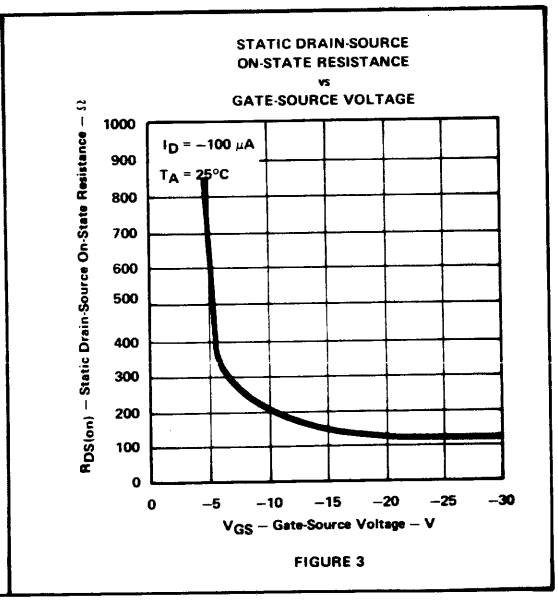

FIGURE 3

typical applications data

In the following circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a PNP transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, –20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to

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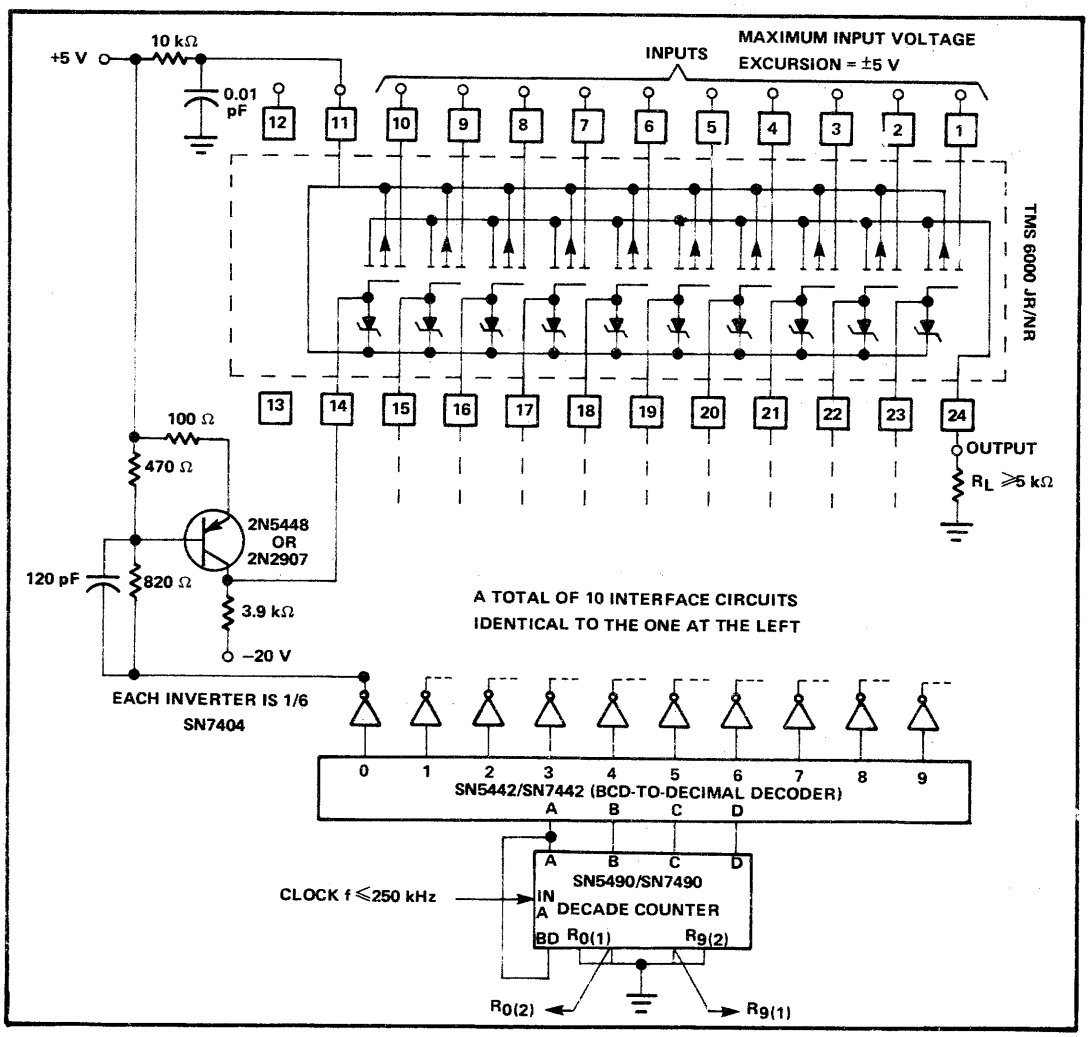
typical applications data (continued)

allow the previous MOS switch to turn off comp.. tely before the next one turns on. Cloc < frequency, t_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +12 V to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, so the simple RC filter shown is sufficient to prevent noise from the +12 volt supply from interfering with switch operation.

DIRECT-COUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



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TMS 6002 JR, TMS 6002 NC
SIX-CHANNEL ANALOG SWITCHES

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line ceramic or plastic package
- $R_{DS(on)}$ . . . 200 Ω maximum

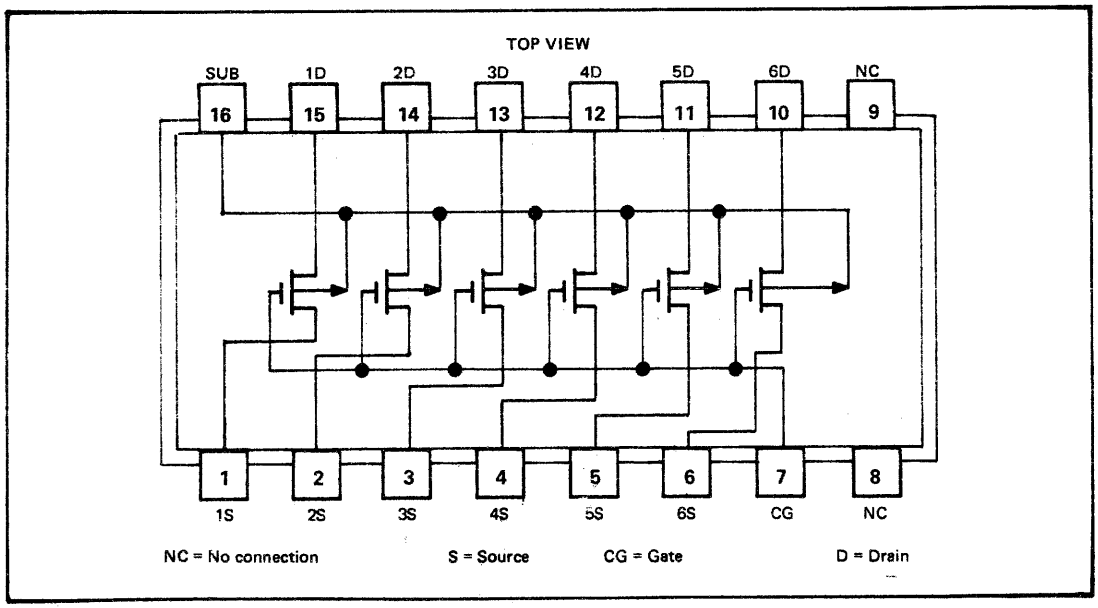
description

The TMS 6002 JR/NC analog switch is a P-channel enhancement-mode MOS monolithic integrated circuit, utilizing thick-oxide technology. This general-purpose device consists of six MOS transistors having all six gates interconnected. The common gate is protected by a diode circuit and must be switched by an external driver. The analog switch is packaged in 16-pin dual-in-line ceramic package.

A gate input impedance greater than 10^{10} ohms coupled with low source-cutoff current, zero inherent offset voltage, and low on-state resistance ideally suits this switch for time-division multiplexing.

schematic and pin configuration

This device is available in both a 16-pin hermetically sealed ceramic dual-in-line package (TMS 6000 JR) and a 16-pin plastic package (TMS 6002 NC). The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)



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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage . . . . . −30 V
Forward gate-source voltage (See Note 1) . . . . . −30 V
Gate-drain voltage . . . . . −30 V
Drain current . . . . . −50 mA
Gate-terminal reverse current (forward direction for zener clamp) . . . . . 0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 500 mW
Operating free-air temperature range (See Note 3) . . . . . −55°C to 85°C
Storage temperature range . . . . . −55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.
3. Operating free-air temperature for TMS 6002 NC is −25°C to +85°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			V
I_{GSSF}	Gate-terminal forward current 6 gates	$V_{GS} = -20$ V, $V_{DS} = 0$		0.3	6.0	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			3.0	nA
I_{SDS}	Zero-gate-voltage source current	$V_{SD} = -20$ V, $V_{GS} = 0$			6.0	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	V
$R_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common gate forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3		mmho
$C_{(in)}$	Input capacitance (See Note 3)	$V_{DS} = -5$ V, $V_{GS} = 0$, f = 1 MHz		4	7	pF
$C_{(out)}$	Output capacitance (See Note 4)	$V_{SD} = -5$ V, $V_{GS} = -5$ V, f = 1 MHz		4	7	pF
C_{gs}	Gate-source capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5	pF
C_{gd}	Gate-drain capacitance (See Note 5)	$V_{DS} = 0$, $V_{GS} = 0$,		2	3	pF
t_{don}	Turn on delay time	See Switching Circuit		50	75	ns

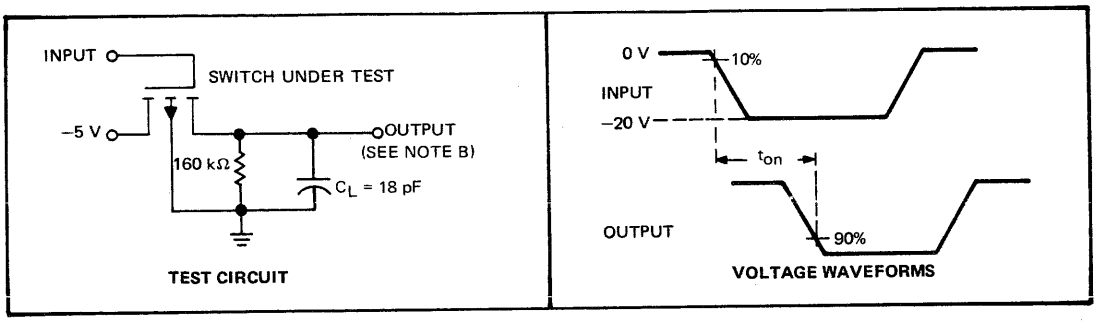
NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

† The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

14

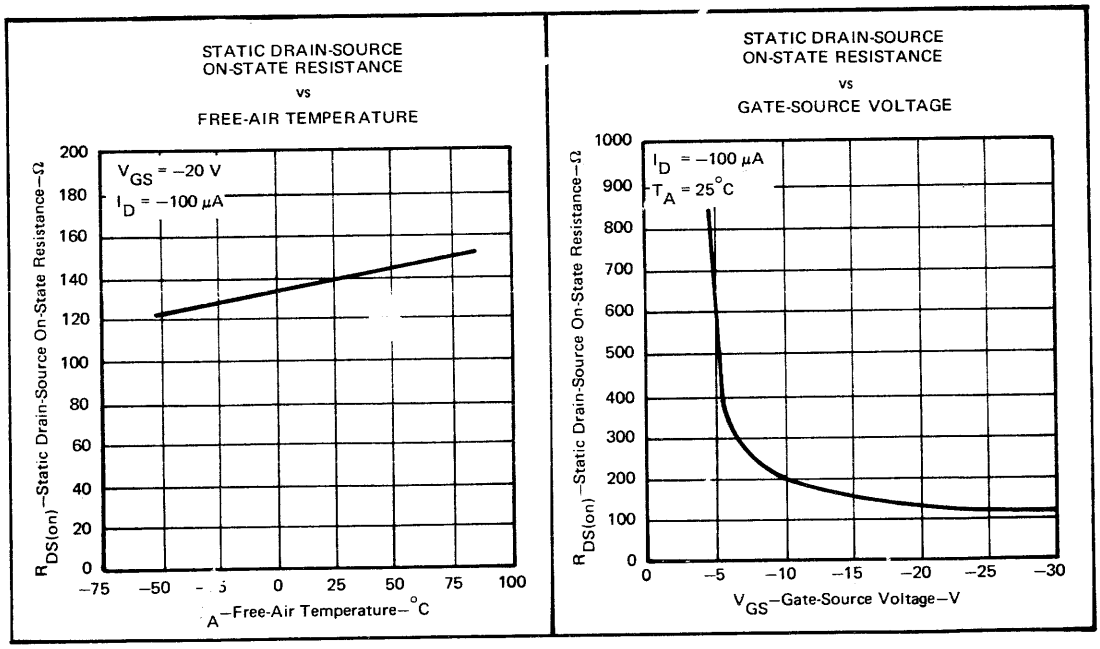
switching characteristics

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$, C_L includes oscilloscope input capacitance plus stray capacitance.

TYPICAL CHARACTERISTICS



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TMS 6005 JR, NC; TMS 6009 JR, NC
SIX-CHANNEL ANALOG SWITCHES

FEBRUARY, 1971

DESIGNED FOR HIGH-SPEED MULTIPLEXING APPLICATIONS

- Dual-in-line package
- $r_{DS(on)}$ . . . 200 Ω max

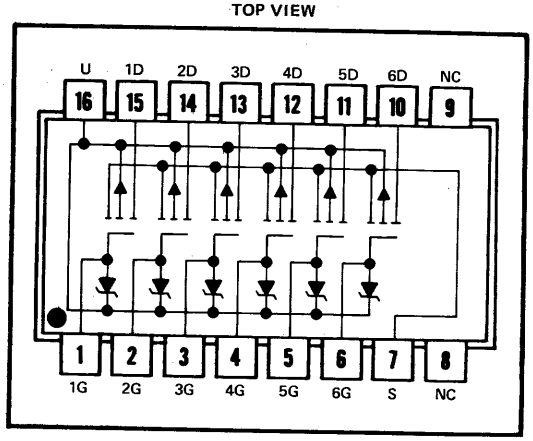
description

The TMS 6005 JR/NC and TMS 6009 JR/NC analog switches are P-channel enhancement-mode MOS monolithic integrated circuits utilizing thick-oxide technology. Each consists of six MOS transistors having all six sources interconnected. The gate of each MOS device is protected by a diode circuit and must be switched by an external driver. The analog switches are packaged in 16-pin dual-in-line ceramic packages or 16-pin plastic packages.

The TMS 6009 JR/NC is intended for applications requiring extremely low leakage currents. The TMS 6005 JR/NC is a general-purpose device.

A gate input impedance greater than 10^{10} ohms coupled with low source cutoff current, zero inherent offset voltage, and low on-state resistance makes these switches ideally suited for time-division multiplexing of analog and digital signals.

TOP VIEW



G — Gate S — Source D — Drain
NC — No Internal connection

mechanical data

Mounted in a 16-pin hermetically sealed ceramic dual-in-line package the analog switches are numbered TMS 6005 JR, and TMS 6009 JR. In 16-pin plastic packages the devices are designated TMS 6005 NC and TMS 6009 NC. The packages are designed for insertion in mounting-hole rows on 0.300-inch centers. (See MOS/LSI packaging section.)

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Drain-source voltage	−30 V
Forward gate-source voltage (see Note 1)	−30 V
Gate-drain voltage	−30 V
Drain current	−50 mA
Gate-terminal reverse current (forward direction for zener clamp)	0.1 mA
Continuous dissipation at (or below) 25°C free-air temperature (see Note 2)	500 mW
Operating free-air temperature range (see Note 3)	−55°C to 85°C
Storage temperature range	−55°C to 150°C

NOTES: 1. Forward gate-source voltage is of such polarity that an increase in its magnitude above a threshold level causes the channel resistance to decrease.
2. Derate linearly to 85°C free-air temperature at the rate of 8.3 mW/°C.
3. Operating temperature range for TMS 6005 NC and TMS 6009 NC is −25 to +85°C.

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electrical characteristics at 25°C free-air temperature

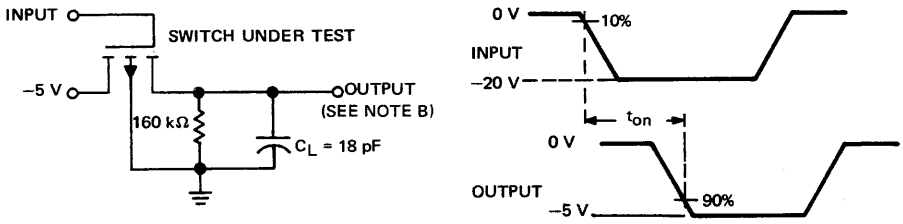
PARAMETER		TEST CONDITIONS†	TMS6005JR			TMS6009JR			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = -10\ \mu A$, $V_{GS} = 0$	−30			−30			V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = -10\ \mu A$, $V_{DS} = 0$	−30			−30			V
$V_{(BR)SDS}$	Source-drain breakdown voltage	$I_S = -10\ \mu A$, $V_{GD} = 0$	−30			−30			V
I_{GSSF}	Gate-terminal forward current	$V_{GS} = -20$ V, $V_{DS} = 0$			−5		−0.05	−1	nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -20$ V, $V_{GS} = 0$			−10			−3	nA
I_{SDS}	Zero-gate-voltage source current (total for six switches)	$V_{SD} = -20$ V, $V_{GD} = 0$			−30			−6	nA
$V_{GS(th)}$	Gate-source threshold voltage	$V_{DG} = 0$, $I_D = -10\ \mu A$	−2.5	−4	−6	−2.5	−4	−6	V
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{GS} = -20$ V, $I_D = -100\ \mu A$		140	200		140	200	Ω
$\lvert y_{fs} \rvert$	Small-signal common-source forward transfer admittance	$V_{DS} = -10$ V, $V_{GS} = -10$ V, f = 1 kHz		3			3		mmho
$C_{(in)}$	Input capacitance (see Note 3)	$V_{DS} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		4	7		4	7	pF
$C_{(out)}$	Output capacitance (see Note 4)	$V_{SD} = -5$ V, $V_G = V_S = V_{SS}$ f = 1 MHz		13	20		13	20	pF
C_{gs}	Gate-source capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		3	4.5		3	4.5	pF
C_{gd}	Gate-drain capacitance (see Note 5)	$V_{DS} = 0$, $V_{GS} = 0$, f = 1 MHz		2	3		2	3	pF
t_{on}	Turn-on time	See Figure 1		50	75		50	75	ns

NOTES: 3. $C_{(in)}$ is the capacitance between the drain terminal and all other terminals of the transistor under test.
4. $C_{(out)}$ is the capacitance between the source terminal and all other terminals of the transistor under test.
5. C_{gs} and C_{gd} measurements employ a three-terminal capacitance bridge incorporating a guard circuit. The drain and substrate or the source and substrate, respectively, are connected to the guard terminal of the bridge.

†The body (substrate) terminal is grounded to the reference terminal unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input waveform is supplied by a generator with the following characteristics: $t_r \leq 10$ ns, $Z_{out} = 50\ \Omega$.
B. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 10$ ns, $R_{in} \geq 10\ M\Omega$. C_L includes oscilloscope input capacitance plus stray capacitance.

FIGURE 1

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TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

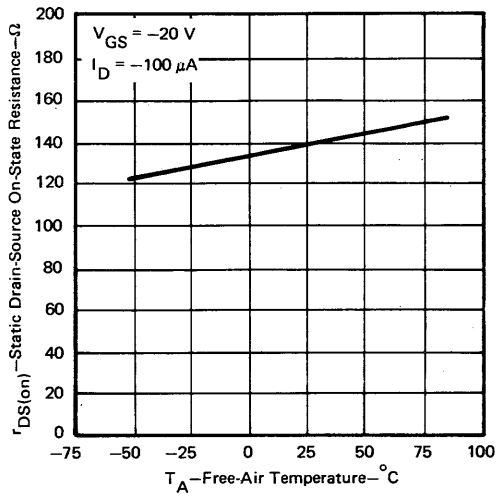


FIGURE 2

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs GATE-SOURCE VOLTAGE

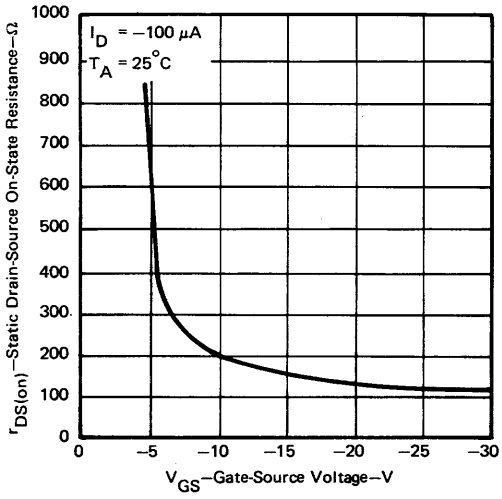


FIGURE 3

TYPICAL APPLICATION DATA

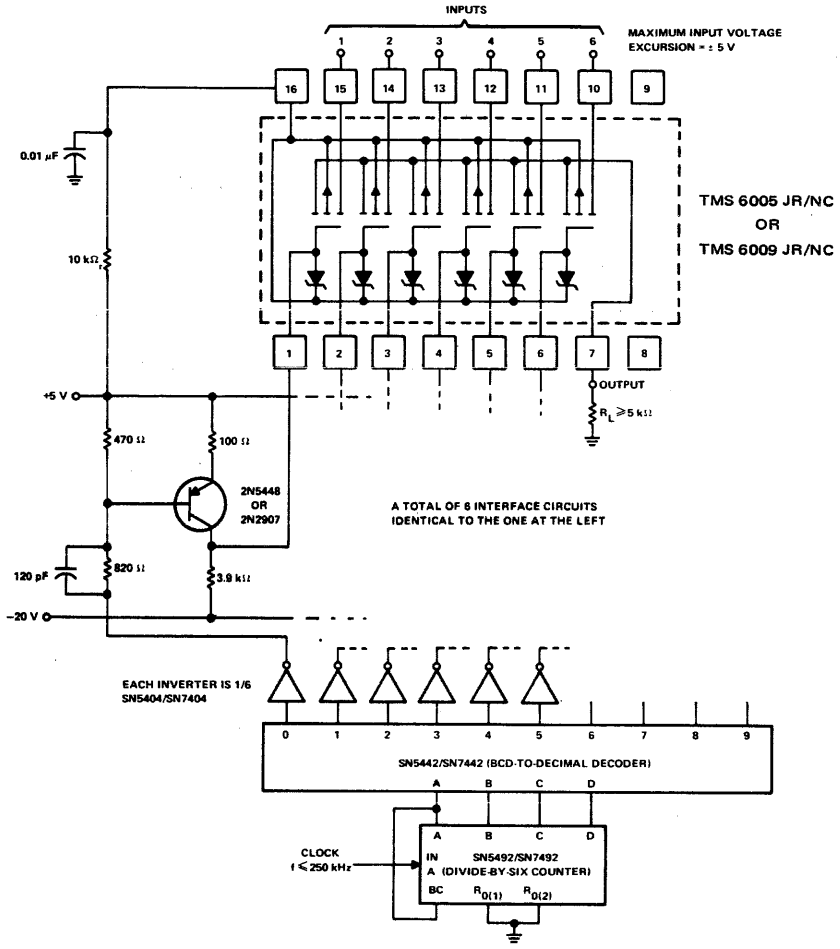
In the following circuit, each input is sequentially connected through an MOS switch to an output circuit represented by load resistance R_L. A Series 54/74 TTL counter and decimal decoder are used to obtain sequential driving from a single clock.

An interface circuit using a PNP transistor translates TTL output voltage levels to those required by the MOS switch. In this circuit, +5 volts is used to turn the switch off, −20 volts is used to turn it on. Because the transistor saturates, a storage time exists which delays turn-off. This delay (about 150 to 300 ns) is used in the interface circuit shown to allow the previous MOS switch to turn off completely before the next one turns on. Clock frequency, f_{clock}, is limited by interface circuit storage and fall times to about 250 kHz before these times become an appreciable fraction of a clock cycle.

The substrate is biased at +5 volts to allow the drains and sources of the MOS switches to go positive without forward-biasing the drain-substrate and source-substrate diffused diodes. Only leakage current flows into the substrate, therefore the simple RC filter shown is sufficient to prevent noise from the +5 volts supply from interfering with switch operation.

TYPICAL APPLICATION DATA

DIRECT-COUPLED MULTIPLEXER ADDRESSED FROM SERIES 54/74 TTL



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CUSTOM MOS/LSI

MOS/LSI is very well suited for custom design:

High level of integration	*lower package count* *lower cost*
Two dimensional design	*easy simulation* *fast turnaround times*
Simple process	*high reliability* *low cost*

To respond to the large demand for MOS/LSI custom subsystems, TI has geared its operations to handle hundreds of custom designs each year.

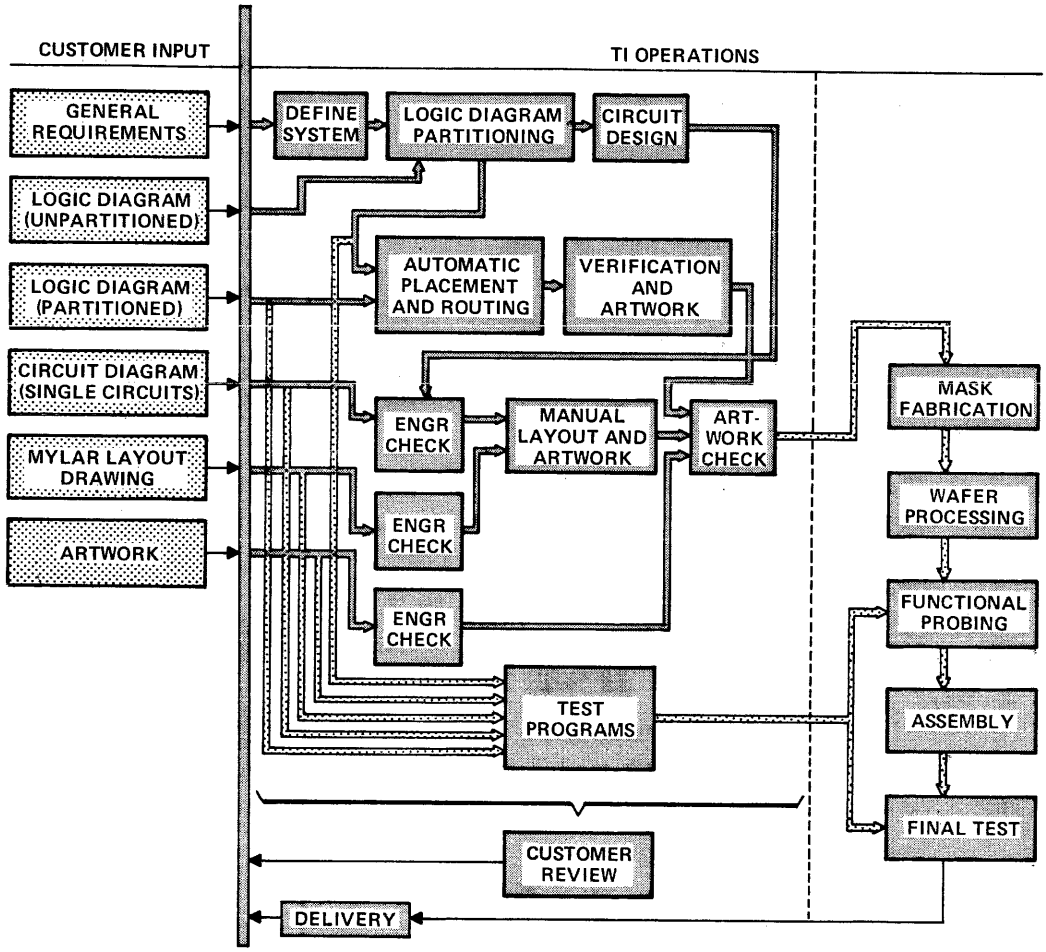
The level of complexity of MOS/LSI subsystems design is very high. Circuit designs are assisted by other specialists. A typical team approach to multichip system design will consist of

- Systems Engineers
- Circuit Designers
- Software Specialists
- Test and Reliability Engineers

In order to optimize design and minimize cost, many computer programs have been developed. In a typical MOS/LSI multichip design the following computer-aided design will be used to optimize the design:

- Subsystem simulation
- Circuit analysis
- Circuit simulation
- Automatic placement and routing (mask design)
- Manually assisted placement and routing (CRT implementation of mask design)
- Computer drawing
- Mask cutting
- Test pattern generation and grading

TI's involvement in custom MOS/LSI is complete. The TI-customer interface is very flexible. Inputs may range from general requirements ("Black Box" specifications) to finished working glass photomasks. Experience has shown that the best interface point is with partitioned logic diagrams; however, TI can also partition your logic diagrams or convert TTL/DTL implemented logic to MOS/LSI.



For more information on custom MOS/LSI design please contact the nearest TI sales office .

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SEMICONDUCTOR MEMORY ARRAYS

Multichip memory arrays are an extension of the line of memory products presently available in both MOS/LSI and bipolar technologies. Only TI has the full range of semiconductor technologies, including MOS/LSI, TTL and ECL, that permit selection of the right technologies to provide optimum memory performance.

Economy, high performance, low power requirements, high packaging density, and improved reliability are among the obvious advantages of multichip memory arrays. The standard arrays use beam leaded circuit chips thermo-compression bonded to thick film ceramic substrates for highest reliability. Standard arrays use MOS/LSI random access memory chips with TTL chips performing the decoding. MOS decoding is also available. Texas Instruments provides the total semiconductor capability required to produce complex storage functions using the best combination of technologies to meet system performance requirements.

2048 - BIT
SEMICONDUCTOR RAM STORAGE ARRAY

FEATURES:

- High density semiconductor storage
- Adaptable to a wide variety of memory systems
- Isolated sense line
- Minimum of 200 microamperes of sense current
- Static operation — no refresh requirements
- 12 V operation
- Ceramic flat pack

description

This specification defines the SMA 1001 256 x 8 MOS Memory Array to be used as building blocks in a large Active Element Memory. The 256 x 8 MOS Memory Array is packaged as eight individual 256 x 1 MOS Memory Chips beam-leaded to a multilayer ceramic substrate.

organization

The Memory Array is organized as a 256-word by 8-bit memory. The Array has four power connections, sixteen X-address connections, sixteen Y-address connections, eight sense line connections, and sixteen digit line connections.

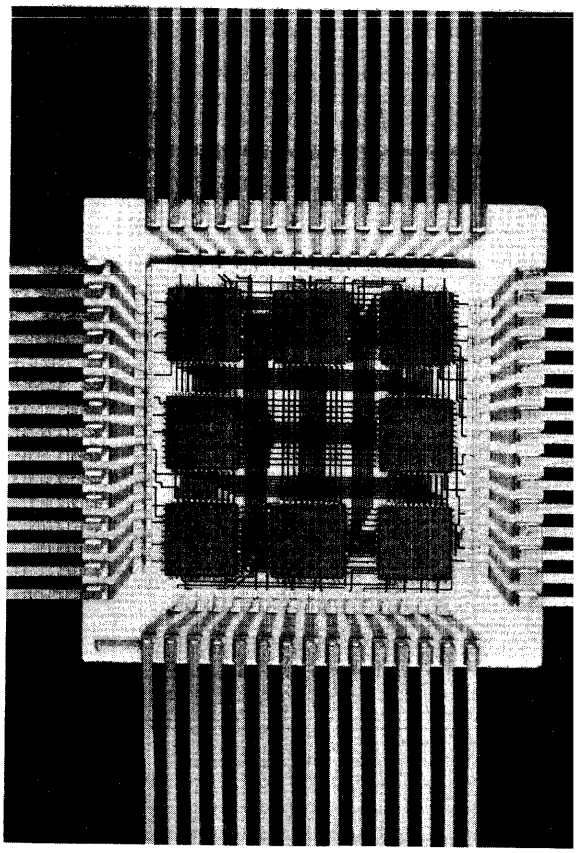
operations

Read Mode –

The contents of 8 memory cells may be non-destructively read from any of the 256 addressable cells on a single memory cycle. The digit lines will be held to the most negative level during a read operation.

Write Mode –

The contents of one to eight memory cells may be forced to a "1" or "0" state by raising the corresponding bit digit-1 or digit-0 line to the most positive voltage level. Placing a high level on both digit-1 and digit-0 lines simultaneously will not cause damage to the array. A high level on the digit-1 line corresponds to a sense current ($I_{S(1)}$) at the sense output during a read.



SMA 1001 SEMICONDUCTOR MEMORY ARRAY

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operations (continued)

Addressing –

A single memory cell in each of the 8 bits will be addressed by driving one X line and one Y line to the most negative voltage level. All other X and Y lines will be held at the most positive voltage level. A simultaneous address of up to 256 words by driving multiple X and/or Y lines to the most negative voltage level will not degrade data stored at any location if all digit lines are held low.

recommended operating conditions

	MIN	TYP	MAX	UNITS
V_{SS}	8	10	15	V
Operating temperature range with 700 FPM air flow	0	25	70	(°C)

static characteristics (V_{SS} = 12 V, T_A = 0 - 70°C)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C_A	Address line capacitance	V_A = 0 V		95		pF
C_D	Digit line capacitance	V_D = 0 V		32		pF
C_D	Digit line capacitance	$V_D = V_{SS}$		60		pF
C_S	Sense line capacitance	V_S = 0		35		pF
$V_{A(0)}$	Address line voltage for unaddressed state	$I_{S(00)}$ = 2.5 μA MAX	6-13*			
$V_{A(1)}$	Address line voltage for addressed state	$I_{S(1)}$ = 200 μA			0.4	V
$V_{D(0)}$	Digit line write voltage	V_A = 0.4 V,	6-13*		8.5-15.5†	V
$V_{D(1)}$	Digit line non-destructive read voltage	V_A = 0.4 V,	0		1.0	V
$I_{S(0)}$	Sense line current when addressed cell contains a (0)	V_A = 0.4 V, R_S = 1 K			2.5	μA
$I_{S(1)}$	Sense line current when addressed cell contains a (1)	R_S = 1 K or less, V_A = 0.4 V	200			μA
$I_{A(2)}$	Address line leakage current	V_A = 0 V			10	μA
I_{SS}	Power supply current	V_{SS} = 12.0 V ± 5%, $V_A = V_{SS}$			85	

* The gate to source voltage must be 2 volts or less for any V_{SS}.
† This voltage must not be greater than V_{SS} + 0.5 V.

dynamic characteristics (V_{SS} = 12 V, T_A = 25°C)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_W	Digit line pulse width for writing into an addressed cell	V_A = 0.4 V, V_D = 0.9 V_{SS}		50		ns
T_A	Time for sense line current to reach 90% of final value after addressing	V_A = 0.2 V		25		ns

mechanical data

This semiconductor memory array consists of 8 individual beam leaded MOS memory chips thermocompression bonded to a multi-level interconnect system and contained in a epoxy sealed ceramic package.

The MOS chips are processed using low threshold nitride process. Beam leads and the internal interconnections are corrosion resistant and all contacts are gold to gold.

The package has a flat pack lead configuration with 60 leads on four sides on 50 mil centers.

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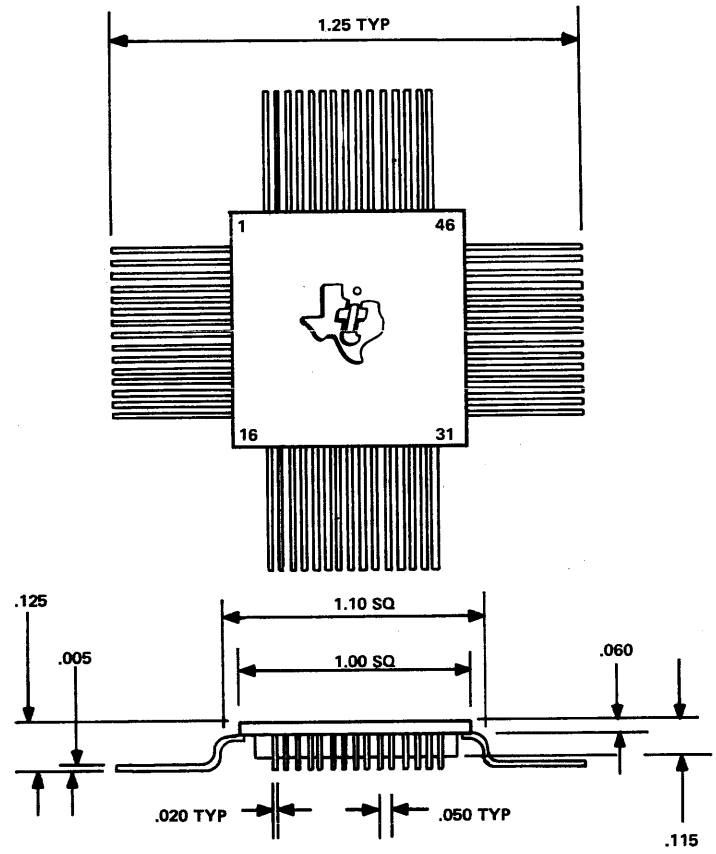
mechanical data (continued)



OUTLINE DIMENSIONS

pin configuration

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Y_{15}	11	X_7	21	D_{0-6}	31	S_8	41	S_7	51	D_{0-1}
2	Y_{16}	12	X_6	22	Y_8	32	Y_1	42	V_{SS2}	52	Y_9
3	S_5	13	X_5	23	Y_7	33	V_{SS1}	43	X_{11}	53	Y_{10}
4	X_8	14	X_4	24	Y_6	34	X_9	44	X_{12}	53	Y_{11}
5	D_{1-5}	15	X_3	25	Y_5	35	X_{10}	45	S_1	55	Y_{12}
6	V_{DD1}	16	S_6	26	Y_4	36	S_2	46	X_{13}	56	Y_{13}
7	D_{0-5}	17	D_{1-6}	27	D_{0-8}	37	D_{1-2}	47	X_{14}	57	S_3
8	S_4	18	V_{DD2}	28	D_{1-8}	38	D_{0-2}	48	X_{15}	58	D_{1-3}
9	D_{1-4}	19	X_2	29	Y_3	39	D_{0-7}	49	X_{16}	59	Y_{14}
10	D_{0-4}	20	X_1	30	Y_2	40	D_{1-7}	50	D_{1-1}	60	D_{0-3}

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PRELIMINARY
PRODUCT SPECIFICATION

SMA 2001
2048-BIT SEMICONDUCTOR MEMORY ARRAY

2048-BIT
HIGH PERFORMANCE SEMICONDUCTOR RAM ARRAY

description

This specification defines a 2048-bit memory array to be used as a building block for organizing larger memory systems. The memory array is a multi-chip array made up of beam leaded MOS storage chips and beam leaded bipolar decoding, sense, write and control chips. This total array is packaged in a ceramic dual-in-line 28 pin package for the commercial temperature range (0 – 70°C).

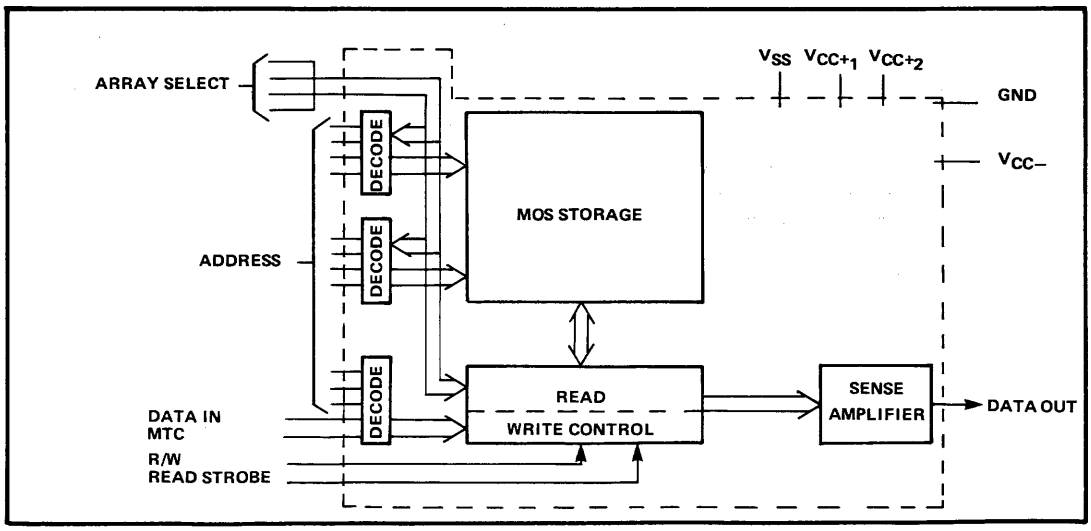
features

- Fast read access time . . . . . 125 ns typical
- Fast write time . . . . . 125 ns typical
- Fast cycle time . . . . . 150 ns typical
- Low memory power dissipation . . . . . 0.65 mW/bit typical
- Open collector output for OR tie
- Directly compatible with DTL and TTL logic circuits
- Easy memory expansion through 4 chip select inputs
- Read strobe control
- Standard TTL loading
- +5 V, GND, –5 V operation
- DIP packaging

organization

The memory array is organized as a 2K x 1 fully decoded memory.

block diagram



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operation

Read Mode – Binary levels are applied to address lines (TTL levels) and data appears at output at access time (125 ns) when READ STROBE is LOW and R/W is HIGH in the READ MODE.

Write Mode – Binary levels are applied to address lines (TTL levels). Data is present at DATA IN. R/W is LOW for the WRITE mode. READ STROBE is HIGH. MTC is LOW until indicated time in WRITE cycle.

Array Select – All four array selects must be LOW to have array selected. When array is not selected, array output is HIGH and data cannot be written into the array.

Timing – Waveform timing is shown on attached timing diagram.

absolute maximum ratings (over operating temperature range unless otherwise noted)†

V_{SS} (See Note 7)	7 V
$V_{CC}+$ (See Note 7)	7 V
$V_{CC}-$ (See Note 7)	–7 V
Input voltage (See Note 8)	5.5 V
Operating Ambient Temperature with 700 FPM of air flow	0 to 70°C
Storage temperature range	–65 to 150°C
Output sink current (Note 9)	20 mA

† Maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.

recommended operating conditions

	MIN	NOM	MAX
V_{SS}	4.75	5.0	5.25
$V_{CC}+$	4.75	5.0	5.25
$V_{CC}-$	–4.75	–5.0	–5.25
Output sink current (See Note 9)			16 mA
Operating Ambient Temperature with 700 FPM of air flow	0°C		70°C

NOTES:
1. All array selects must be LOW for array to be selected.
2. Unselected array data out at HIGH level.
3. Read strobe should be LOW for data out only during read cycle.
4. HIGH data in gives HIGH data out.
5. R/W is HIGH for read, LOW for write.
6. MTC must be LOW at all times except at end of write cycle.
7. With respect to network ground terminal.
8. Input signals must be zero or positive with respect to network ground terminal.
9. Output 1 equals output 2.

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electrical characteristics (over ambient temperature range unless otherwise noted)

PARAMETERS	TEST CONDITIONS†		MIN	TYP*	MAX	UNITS
Inputs						
I_{IH} (All inputs except R/W and Array Selects)	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			40	μA
I_{IL} (All inputs except R/W and Array Selects)	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−1.6	mA
V_{IH} (All inputs except R/W and Array Selects)		$V_{CC}+$ = MIN	2.0			V
V_{IL} (All inputs except R/W and Array Selects)		$V_{CC}+$ = MIN			0.8	V
Inputs						
I_{IH} (R/W and Array Select inputs only)	V_{IH} = 2.4 V,	$V_{CC}+$ = MAX			80	μA
I_{IL} (R/W and Array Select inputs only)	V_{IL} = 0.4 V,	$V_{CC}+$ = MAX			−3.2	mA
V_{IH} (R/W and Array Select inputs only)		$V_{CC}+$ = MIN	2.0			V
V_{IL} (R/W and Array Select inputs only)		$V_{CC}+$ = MIN			0.8	V
Outputs						
V_{OH}	Open Collector					
V_{OL}	I_{sink} = 16 mA,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			0.4	V
I_{OH}	V_{OH} = 5.25 V,	$V_{CC}-$ = MIN, $V_{CC}+$ = MIN			250	μA
Supply Currents						
$I_{CC}+$ (Includes I_{SS})				248		
$I_{CC}-$				20		
Power Dissipation						
Total				1340		mW
Per Bit				0.65		mW
Dynamic Characteristics (See Timing Diagram)						
Read Access				125		ns
50% input address line change to 50% data output with read strobe LOW and R/W signal HIGH	R_{OUT} = 330 Ω ± 5%, C_{OUT} = 30 pF					
Write Cycle				150		ns
50% input address line change to start of next cycle						

* All typical values are at $V_{CC}+ = V_{SS} = -V_{CC}- = +5$ V and $T_A = 25°C$.

† $V_{CC}+ = V_{CC_1} = V_{CC_2}$

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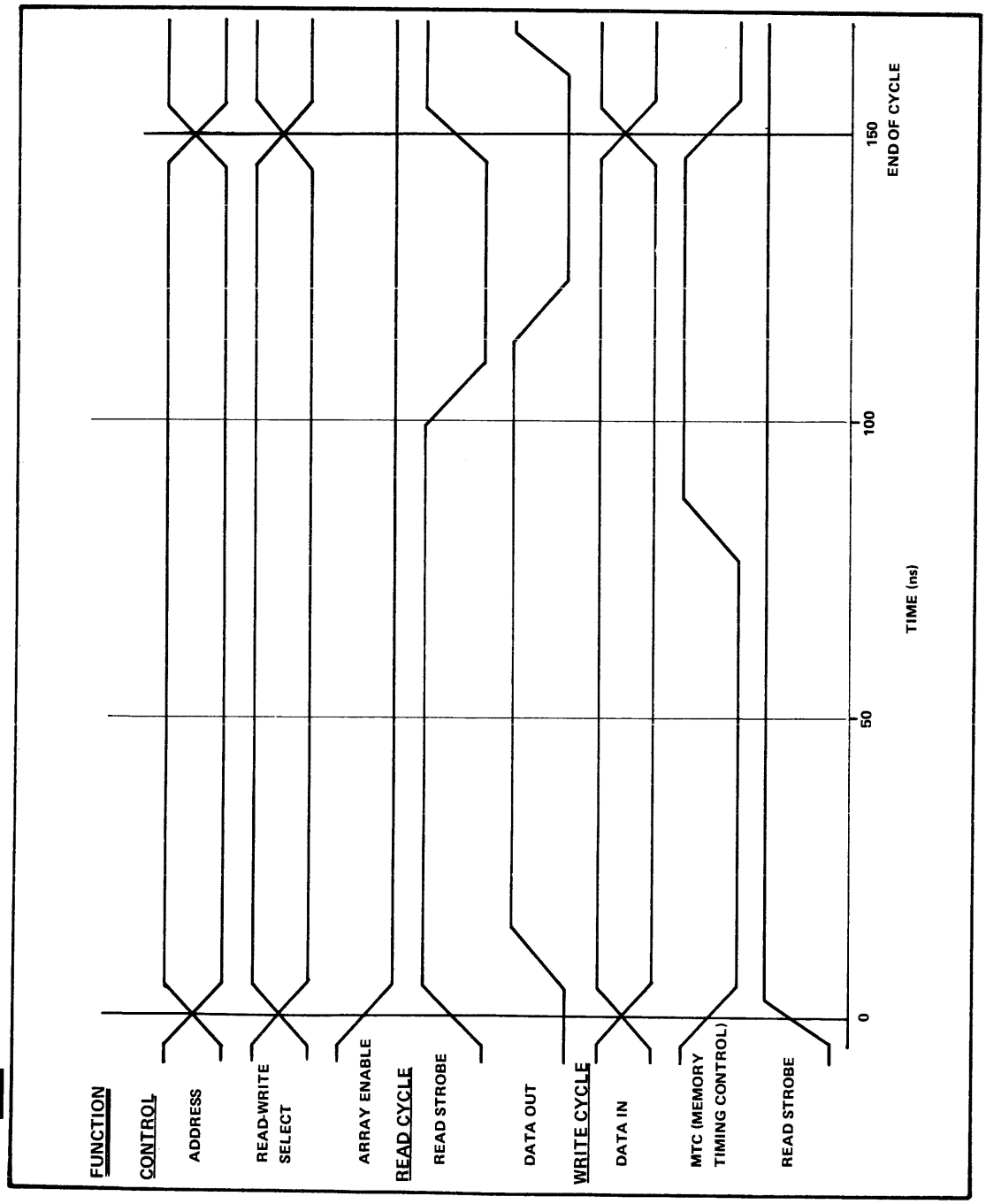
timing diagram



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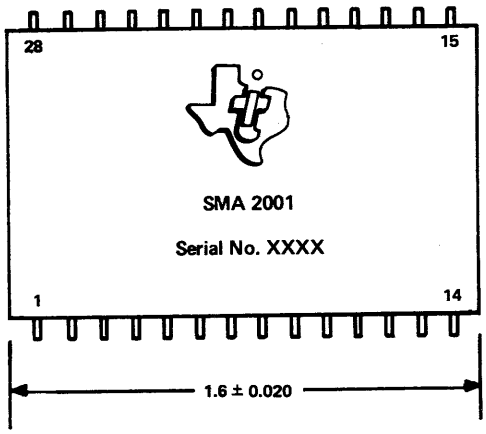
mechanical data

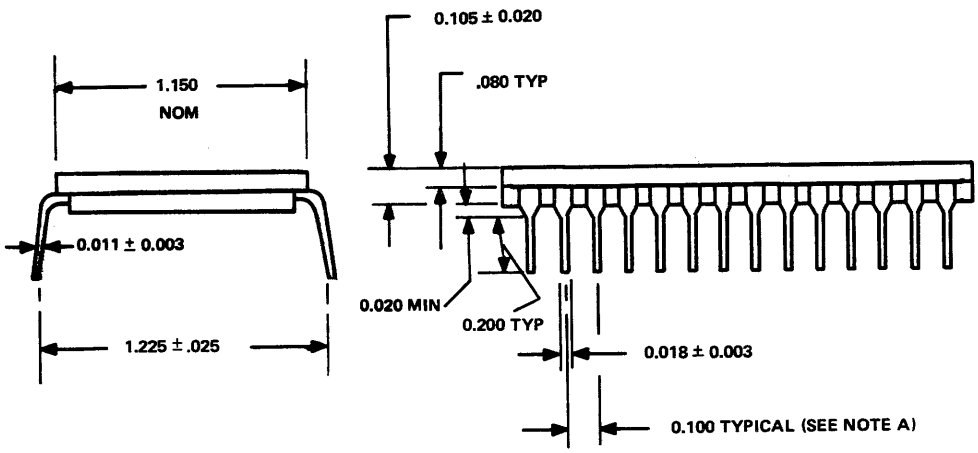
This semiconductor memory array consists of individual beam leaded MOS memory and bipolar interface chips thermocompression bonded to a multilevel interconnect system and contained in an epoxy sealed ceramic package.

The package has a dual-in-line configuration with 28 leads on 100 mil centers. This package is intended for insertion in mounting-hole rows on 1.200 inch centers.

pin configuration

1. GND	15. GND
2. A_{10}	16. NC
3. A_9	17. AS4—ARRAY SEL
4. A_8	18. AS3—ARRAY SEL
5. DATA IN 1	19. A_0
6. MTC—TIMING CONTROL	20. A_1
7. READ STROBE	21. A_2
8. OUTPUT 1 } See Note 9 Page 2	22. A_3
9. OUTPUT 2 }	23. AS2—ARRAY SEL
10. R/W—READ/WRITE	24. AS1—ARRAY SEL
11. $-V_{CC}$	25. A_4
12. V_{CC_2}	26. A_5
13. V_{CC_1}	27. A_6
14. V_{SS}	28. A_7





NOTES: A. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins (1) and (28).

B. All dimensions in inches.

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SMA 2002
2048-BIT SEMICONDUCTOR MEMORY ARRAY

2048-BIT
HIGH PERFORMANCE SEMICONDUCTOR RAM ARRAY

description

This specification defines a 2048-bit memory array to be used as a building block for organizing larger memory systems. The memory array is a multi-chip array made up of beam leaded MOS storage chips and beam leaded bipolar decoding, sense, write and control chips. This total array is packaged in a ceramic dual-in-line 28 pin package for the commercial temperature range (0 – 70°C).

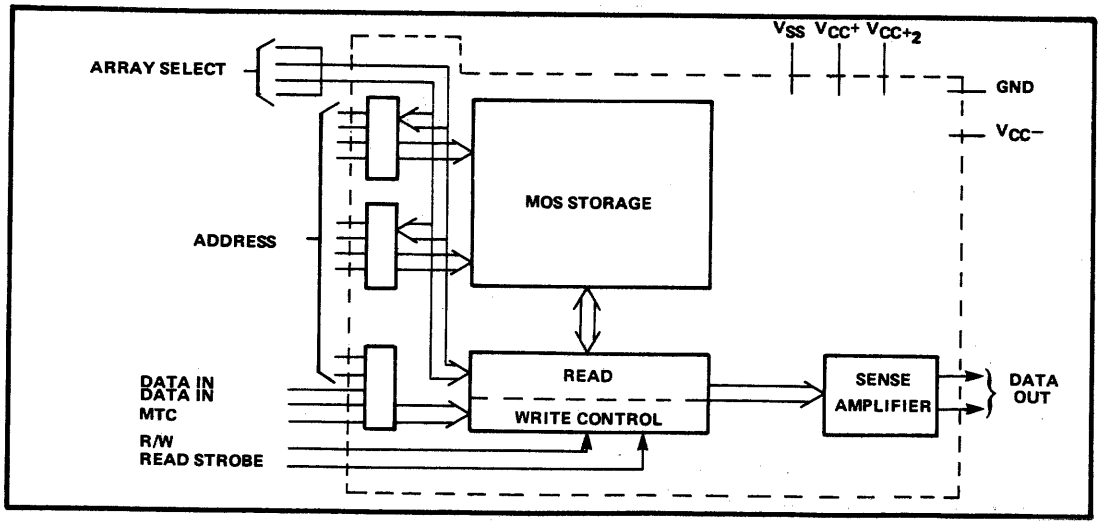
features

- Fast read access time . . . . . 125 ns typical
- Fast write time . . . . . 125 ns typical
- Fast cycle time . . . . . 150 ns typical
- Low memory power dissipation . . . . . 0.65 mW/bit typical
- Open collector output for OR tie
- Directly compatible with DTL and TTL logic circuits
- Easy memory expansion through 4 chip select inputs
- Read strobe control
- Standard TTL loading
- +5 V, GND, –5 V operation
- DIP packaging

organization

The memory array is organized as a 1K x 2 fully decoded memory.

block diagram



TEXAS INSTRUMENTS
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operation

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Write Mode – Binary levels are applied to address lines (TTL levels). Data is present at DATA IN. R/W is LOW for the WRITE mode. READ STROBE is HIGH. MTC is LOW until indicated time in WRITE cycle.

Array Select – All four array selects must be LOW to have array selected. When array is not selected, array output is HIGH and data cannot be written into the array.

Timing – Waveform timing is shown on attached timing diagram.

absolute maximum ratings (over operating temperature range unless otherwise noted)†

V_{SS} (See Note 7)	7 V
V_{CC+} (See Note 7)	7 V
V_{CC-} (See Note 7)	–7 V
Input voltage (See Note 8)	5.5 V
Operating Ambient Temperature with 700 FPM of air flow	0 to 70°C
Storage temperature range	–65 to 150°C
Output sink current	20 mA

† Maximum ratings are limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing.

recommended operating conditions

	MIN	NOM	MAX
V_{SS}	4.75	5.0	5.25
V_{CC+}	4.75	5.0	5.25
V_{CC-}	–4.75	–5.0	–5.25
Output sink current			16 mA
Operating Ambient Temperature with 700 FPM of air flow	0°C		70°C

NOTES:
1. All array selects must be LOW for array to be selected.
2. Unselected array data out at HIGH level.
3. Read strobe should be LOW for data out only during read cycle.
4. HIGH data in gives HIGH data out.
5. R/W is HIGH for read, LOW for write.
6. MTC must be LOW at all times except at end of write cycle.
7. With respect to network ground terminal.
8. Input signals must be zero or positive with respect to network ground terminal.

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electrical characteristics (over ambient temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP*	MAX	UNITS
Inputs							
I_{IH}	All inputs	V_{IH} = 2.4 V,	V_{CC+} = MAX			40	μA
I_{IL}	except	V_{IL} = 0.4 V,	V_{CC+} = MAX			−1.6	mA
V_{IH}	R/W and		V_{CC+} = MIN	2.0			V
V_{IL}	Array Selects		V_{CC+} = MIN			0.8	V
Inputs							
I_{IH}	R/W and	V_{IH} = 2.4 V,	V_{CC+} = MAX			80	μA
I_{IL}	Array Select	V_{IL} = 0.4 V,	V_{CC+} = MAX			−3.2	mA
V_{IH}	inputs		V_{CC+} = MIN	2.0			V
V_{IL}	only		V_{CC+} = MIN			0.8	V
Outputs							
V_{OH}		Open Collector					
V_{OL}		I_{sink} = 16 mA,	V_{CC-} = MIN, V_{CC+} = MIN			0.4	V
I_{OH}		V_{OH} = 5.25 V,	V_{CC-} = MIN, V_{CC+} = MIN			250	μA
Supply Currents							
I_{CC+} (Includes I_{SS})					248		
I_{CC-}					20		
Power Dissipation							
Total					1340		mW
Per Bit					0.65		mW
Dynamic Characteristics (See Timing Diagram)							
Read Access		R_{OUT} = 330 Ω ± 5%			125		ns
	50% input address line change to 50% data output with read strobe LOW and R/W signal HIGH	C_{OUT} = 30 pF					
Write Cycle							
	50% input address line change to start of next cycle				150		ns

* All typical values are at $V_{CC+} = V_{SS} = -V_{CC-} = +5$ V and $T_A = 25°C$.

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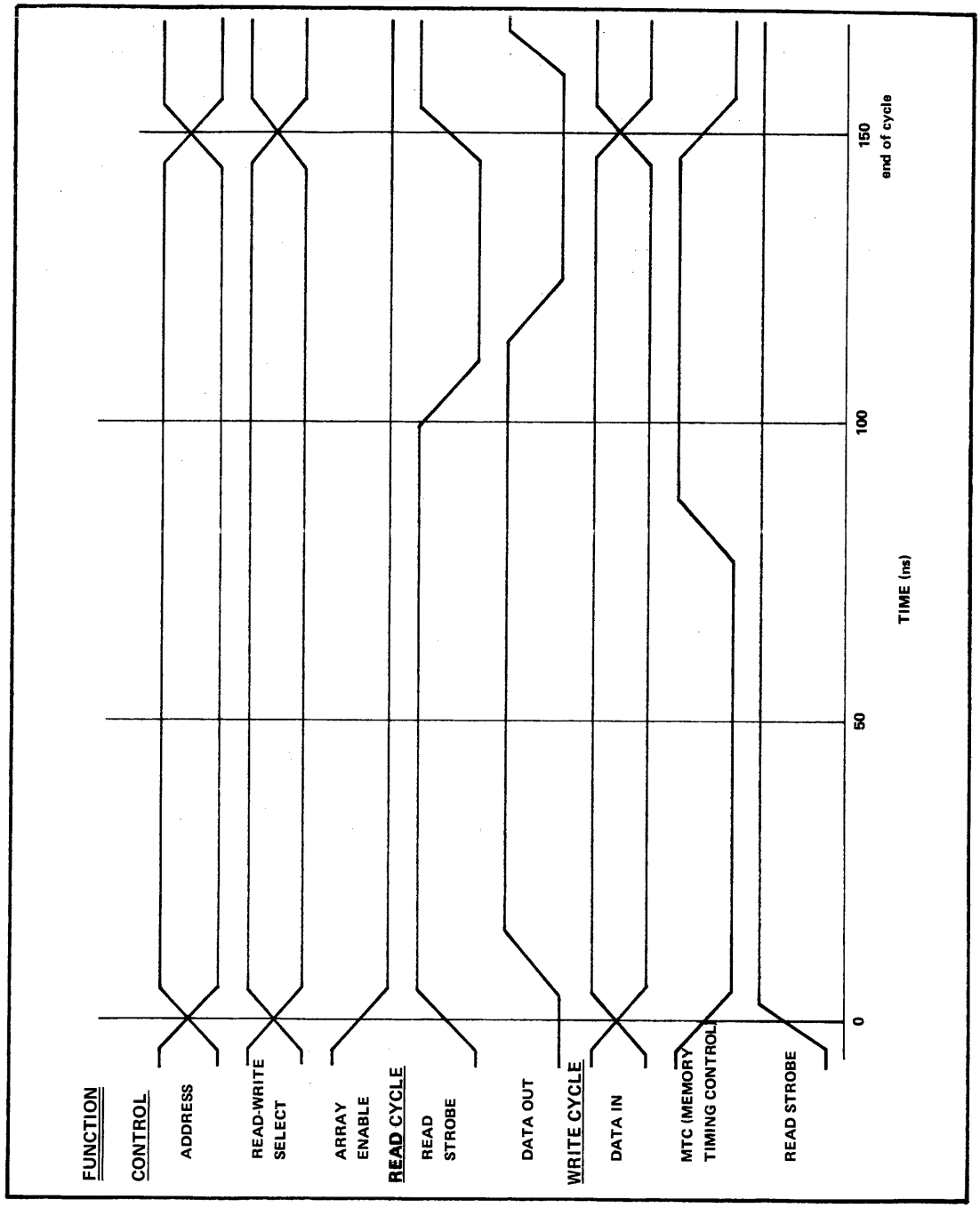
timing diagram



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SMA 2002
2048-BIT SEMICONDUCTOR MEMORY ARRAY

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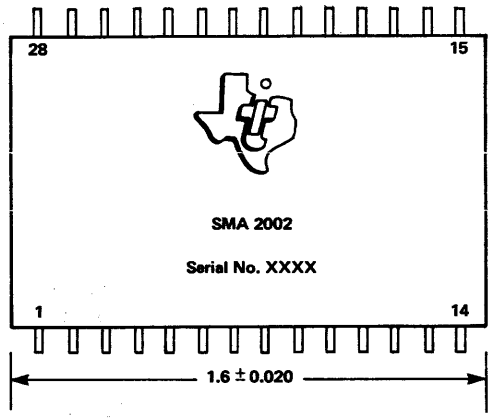
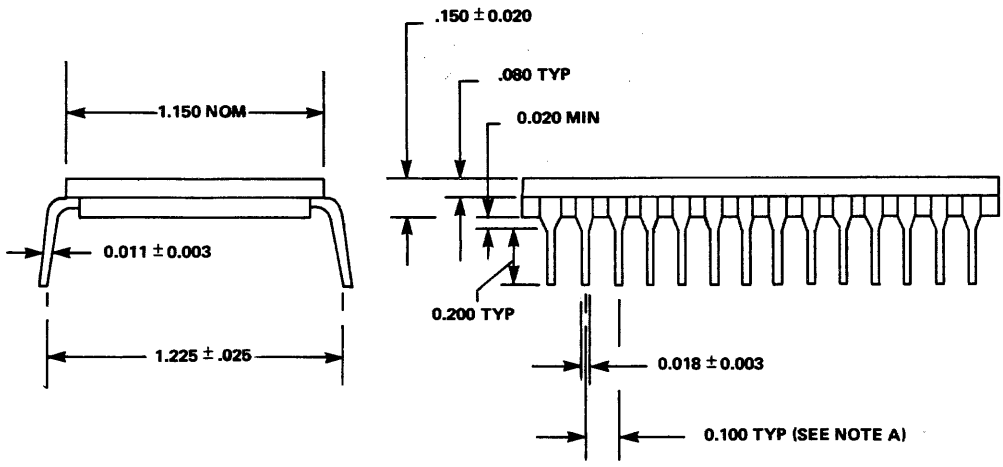
8. OUTPUT 1	22. A_3
9. OUTPUT 2	23. AS2–ARRAY SEL
10. R/W–READ/WRITE	24. AS1–ARRAY SEL
11. $-V_{CC}$	25. A_4
12. V_{CC_2}	26. A_5
13. V_{CC_1}	27. A_6
14. V_{SS}	28. A_7





NOTES: A. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (28).

B. All dimensions in inches.

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