Series 54L/74L Circuits

Series 54L/74L
Low Power TTL
Integrated Circuits

- Over 14 MSI Functions
- All Popular Package Configurations
- Fast Delivery to MIL-STD-883 for Military and Space Applications.

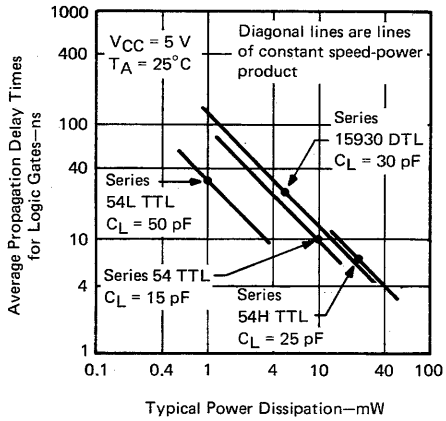
LOW-POWER TRANSISTOR-TRANSISTOR LOGIC CIRCUITS FOR AEROSPACE, MILITARY, OR INDUSTRIAL COMPUTER AND CONTROL SYSTEM APPLICATIONS

description

Series 54L/74L integrated circuits have been designed for aerospace, military, and industrial applications where high d-c noise margin, low power dissipation, improved speed-power relationships, and high reliability are important system considerations. This logic family includes small-scale integration (SSI) circuits and medium-scale integration (MSI) circuits needed to perform most functions of general-purpose digital systems. Definitive specifications for Series 54L/74L SSI circuits (gates and flip-flops) are provided in this section, and 54L/74L MSI circuits are included in Section 9.

Series 54L circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and Series 74L circuits are characterized for operation over the temperature range of 0°C to 70°C.

SPEED-POWER RELATIONSHIPS OF DIGITAL IC FAMILIES†



†Typical saturated logic gate from the indicated families

features

CHOICE OF PACKAGES

- available in flat (T) and dual-in-line package (J or N)
- maximum number of circuits per package through use of 14-lead package

OPTIMUM CIRCUIT PERFORMANCE

- very low power dissipation—typically 1 mW per gate at 50% duty cycle
- relatively high speed—typically gate propagation delay time of 33 ns
- high d-c noise margin—typically one volt at T_A = 25°C
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- fan-out—10 Series 54L loads
  - —1 Series 54 load and 2 Series 54L loads
  - —1 Series 54H load
- a standard Series 54 output will drive 40 Series 54L loads
- logic levels are compatible with most bipolar saturated integrated circuits

8

SERIES 54L/74L
FEATURING 1 mW AND 33 ns PER GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			SEC.-PAGE
	–55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	
NAND/NOR GATES						
Quadruple 2-Input Positive NAND Gates	SN54L00	SN74L00	J	N	T	8-4
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L01	SN74L01	J	N	T	8-5
Quadruple 2-Input Positive NOR Gates	SN54L02	SN74L02	J	N	T	8-6
Quadruple 2-Input Positive NAND Gates (with Open-Collector Output)	SN54L03	SN74L03	J	N	T	8-5
Hex Inverters	SN54L04	SN74L04	J	N	T	8-9
Triple 3-Input Positive NAND Gates	SN54L10	SN74L10	J	N	T	8-10
Dual 4-Input Positive NAND Gates	SN54L20	SN74L20	J	N	T	8-11
8-Input Positive NAND Gates	SN54L30	SN74L30	J	N	T	8-12
AND-OR-INVERT GATES						
Dual 2-Wide AND-OR-INVERT Gates	SN54L51	SN74L51	J	N	T	8-13
4-Wide 3-2-2-3-Input AND-OR-INVERT Gates	SN54L54	SN74L54	J	N	T	8-14
2-Wide 4-Input AND-OR-INVERT Gates	SN54L55	SN74L55	J	N	T	8-15
FLIP-FLOPS						
R-S Master-Slave Flip-Flops	SN54L71	SN74L71	J	N	T	8-16
J-K Master-Slave Flip-Flops	SN54L72	SN74L72	J	N	T	8-19
Dual J-K Master-Slave Flip-Flops	SN54L73	SN74L73	J	N	T	8-22
Dual D-Type Edge-Triggered Flip-Flops	SN54L74	SN74L74	J	N	T	8-25
Dual J-K Master-Slave Flip-Flops (Common Clock)	SN54L78	SN74L78	J	N	T	8-28
Retriggerable Monostable Multivibrators with Clear	SN54L122	SN74L122	J	N	T	8-31

8

SEE PAGES 9-1, 9-2, AND 9-3 FOR LISTING OF TTL MSI CIRCUITS

*For outline drawings of all packages, see Section 1.

–SEE ORDERING INSTRUCTIONS PAGE 1-1–

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	8 V
Input Voltage, V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54L	−55°C to 125°C
Series 74L	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54L and 74L logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

HIGH VOLTAGE = LOGICAL 1

LOW VOLTAGE = LOGICAL 0

unused gates

Inputs of unused gates should be connected to ground. This sets the gate output to logical 1 to ensure minimum power dissipation.

unused inputs of NAND/AND gates

Unused inputs, including preset and clear, must be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V.

Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.4 V and 3.5 V.
b. Connect unused inputs, except preset or clear, to a used input of the same gate if maximum fan-out of the driving output will not be exceeded.
c. Connect unused inputs to the logical 1 output of an unused gate.
d. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistor requires no more than a 0.18-mA flow out of the input at a logical 0 voltage level; therefore, one load (N=1) is −0.18 mA maximum. Each input, except the clock inputs of the flip-flops, requires current into the terminal at a logical 1 voltage level. This current is 10 μA maximum for each. See fan-out capabilities (below) and typical characteristics (page 8-47) for flip-flop clock input current requirements. Currents into the input terminals are specified as positive values.

8

fan-out capability

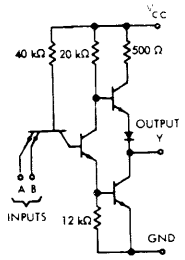
Fan-out (N) reflects the ability of an output to sink current from a number of Series 54L and 74L loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each Series 54L output is capable of sinking current or supplying current to 10 Series 54L loads (N=10), or one Series 54/74 load and two 54L loads. Each Series 74L output is capable of sinking current or supplying current to 20 Series 74L loads (N=20), or two Series 54/74 loads and two 74L loads. Load currents (out of the output terminal) are specified as negative values.

A Series 54 or 74 output is capable of sinking current or supplying current to 40 Series 54L or 74L loads (N=40). The Series 54/74 buffer gate circuit (SN5440/SN7440) is capable of driving 120 Series 54L/74L loads. The carry outputs of the Series 54/74 adders are capable of driving 20 Series 54L/74L loads and the A★ and B★ nodes of the SN5480/SN7480 may be used to drive 12 loads.

When fanning out into Series 54L/74L flip-flop clock inputs, no load current (I_{load}) is drawn at $V_{in(clock)}$ = 2.4 V. Therefore, the fan-out limitation is the I_{sink} capability of the driving output. A Series 54/74 output will sink sufficient current to drive 44 clock inputs (88 loads), and the SN5440/SN7440 circuit will sink sufficient current to drive 133 clock inputs (266 loads). The Series 54L output is capable of driving five 54L clock inputs and one additional load. The Series 74L output is capable of driving ten 74L clock inputs.

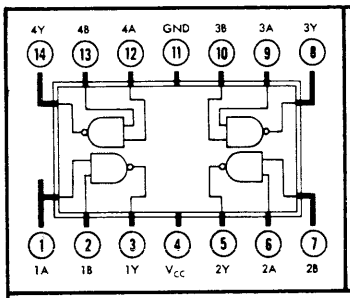
CIRCUIT TYPES SN54L00, SN74L00
QUADRUPLE 2-INPUT POSITIVE NAND GATES

schematic (each gate)

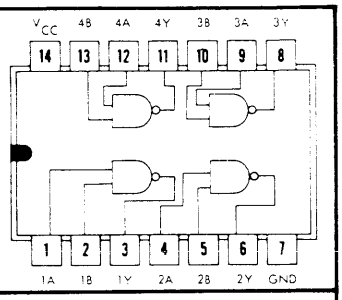


NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L00 Circuits	4.5	5	5.5	V
SN74L00 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L00 Circuits	−55	25	125	°C
SN74L00 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

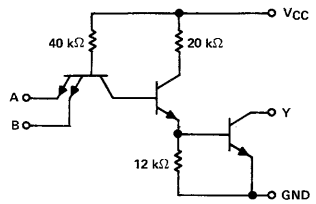
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

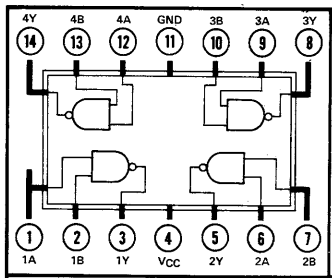
CIRCUIT TYPES SN54L01, SN54L03, SN74L01, SN74L03
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

schematic (each gate)

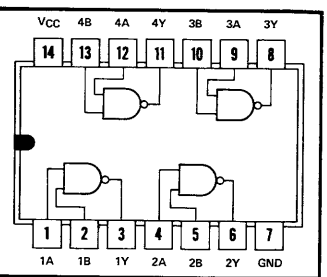


Resistor values shown are nominal.

SN54L01, SN74L01
T FLAT PACKAGE
(TOP VIEW)



SN54L03, SN74L03
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

	SN54L01 SN54L03			SN74L01 SN74L03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.6	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.6 V, V_{OH} = 5.5 V		50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs grounded		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

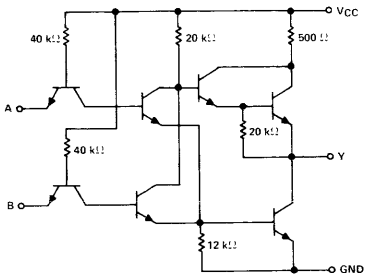
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 35		90	ns
t_{PHL}	Propagation delay time, high-to-low-level output			60	

8

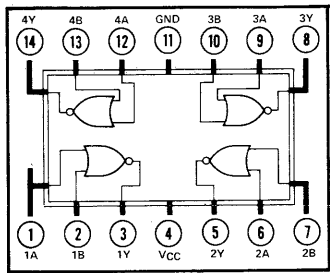
CIRCUIT TYPES SN54L02, SN74L02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

schematic (each gate)

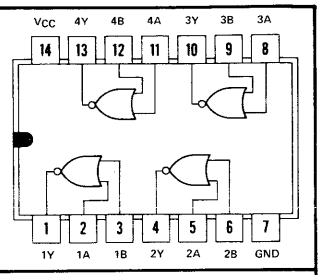


Resistor values shown are nominal.

T FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

	SN54L02			SN74L02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, See Note 3		0.4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, See Note 4		0.65	mA

NOTES: 3. I_{CCH} is measured with all inputs grounded and outputs open.
4. I_{CCL} is measured with one input of each gate at 5 V, the remaining inputs grounded, and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 35		31	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	

8

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine Series 54L/74L loads. When no other open-collector gates are paralleled, this gate may be used to drive ten Series 54L/74L loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

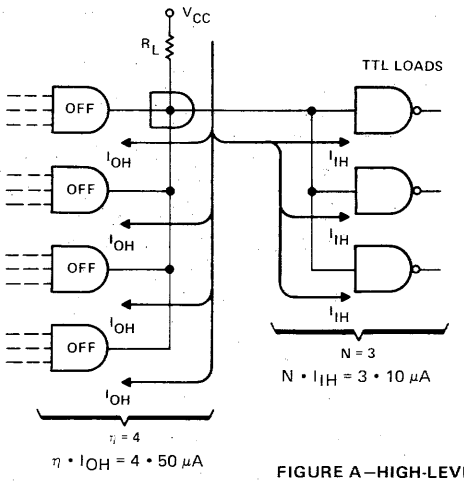
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of Series 54L/74L loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.0002 + 0.00003}\ \Omega = \frac{2.6}{0.00023}\ \Omega = 11\,300\ \Omega$$

FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

8

SERIES 54L/74L
OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

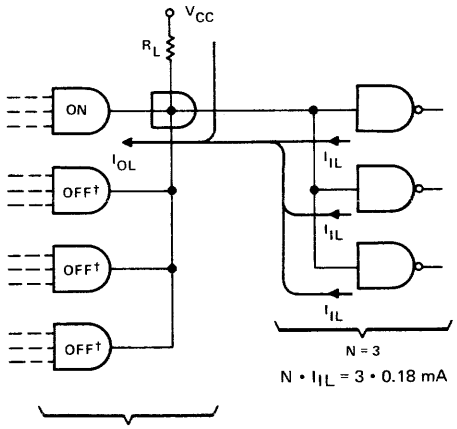
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to 2 mA, the maximum current which will ensure a low-level maximum of 0.3 volt.

Also, fan-out must be considered. Part of the 2 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$

$$R_{L(min)} = \frac{5 - 0.3}{0.002 - 0.00054}\ \Omega = \frac{4.7}{0.00146}\ \Omega = 3\,220\ \Omega$$

†Current into OFF outputs is negligible at the low logic level.

FIGURE B—LOW-LEVEL CIRCUIT CONDITIONS

driving series 54L/74L loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten Series 54L/74L loads and wire-AND connecting two to ten parallel outputs. Each value shown for one wire-AND output is determined by the fan-out plus the cutoff current of a single output transistor. Extension beyond ten wire-AND connections is permitted with fan-outs of five or less if a valid minimum and maximum R_L is possible. When fanning-out to ten Series 54L/74L loads, the calculation for the minimum value of R_L indicates that a value greater than the maximum value of R_L should be used; however, the use of a resistor having a value between 15.6 kΩ and 17.3 kΩ in this case will satisfy the high level condition and limit the low level to less than 0.31 volt.

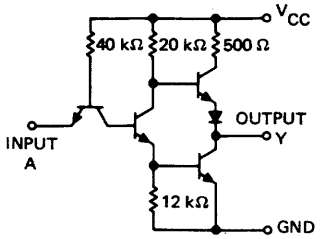
TABLE 1

FAN-OUT TO 54L/74L LOADS	WIRE-AND OUTPUTS										
	1	2	3	4	5	6	7	8	9	10	1 TO 10
1	43.3	23.6	16.2	12.4	10.0	8.38	7.22	6.34	5.65	5.10	2.55
2	37.2	21.6	15.3	11.8	9.63	8.13	7.03	6.20	5.53	6.00	2.87
3	32.5	20.0	14.5	11.3	9.29	7.88	6.85	6.05	5.42	4.90	3.22
4	28.9	18.6	13.7	10.8	8.96	7.65	6.67	5.91	5.31	4.82	3.67
5	26.0	17.3	13.0	10.4	8.66	7.44	6.50	5.78	5.20	4.73	4.29
6	23.6	16.2	12.4	10.0	8.38	7.22	6.34	5.65	X	X	5.20
7	21.6	15.3	11.8	9.63	8.13	7.03	X	X	X	X	6.35
8	20.0	14.5	11.3	9.29	X	X	X	X	X	X	8.40
9	18.6	13.7	X	X	X	X	X	X	X	X	12.4
10	17.3	X	X	X	X	X	X	X	X	X	15.6§
	MAXIMUM										MIN
	LOAD, RESISTOR VALUE IN KILOHMS										

All values in the table are based on:
High-level condition: V_{CC} = 5 V, $V_{OH\ min}$ = 2.4 V
Low-level condition: V_{CC} = 5 V, $V_{OL\ max}$ = 0.3 V
X—Not recommended or not possible
§The theoretical value is 23.5 kΩ. See explanation in text.

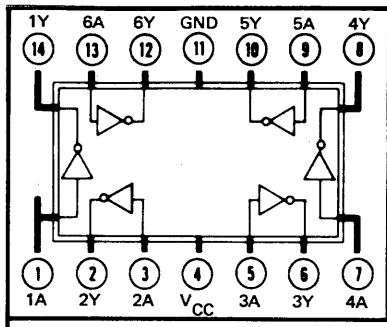
8

schematic (each inverter)

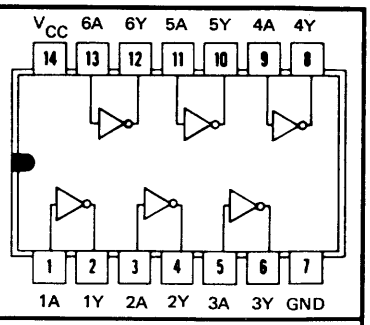


Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic
$Y = \overline{A}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN54L04 Circuits	4.5	5	5.5	V
	SN74L04 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN54L04 Circuits	−55	25	125	°C
	SN74L04 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	7		2		V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 level at output	8			0.7	V
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = − 100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current	9	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current	10	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	
I_{OS}	Short-circuit output current	11	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (Average per inverter)	12	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

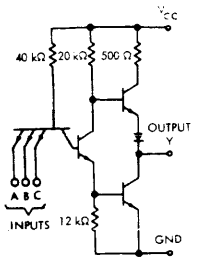
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

8

CIRCUIT TYPES SN54L10, SN74L10
TRIPLE 3-INPUT POSITIVE NAND GATES

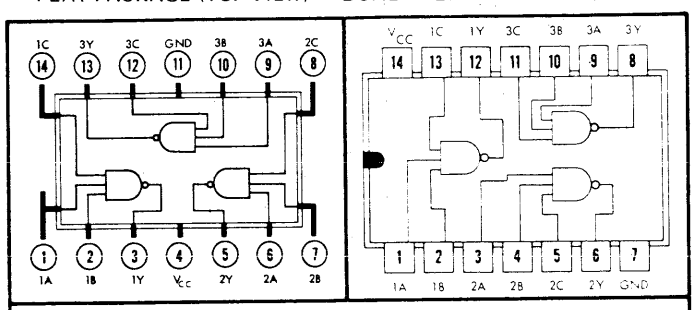
schematic (each gate)



NOTE: Component values shown are nominal.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABC}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L10 Circuits	4.5	5	5.5	V
SN74L10 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L10 Circuits	−55	25	125	°C
SN74L10 Circuits	0	25	70	°C

8

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

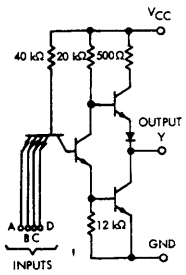
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

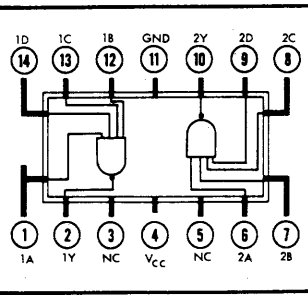
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

schematic (each gate)

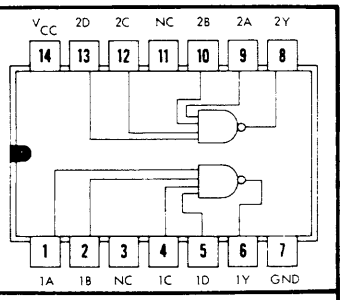


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L20 Circuits	4.5	5	5.5	V
SN74L20 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L20 Circuits	−55	25	125	°C
SN74L20 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1		2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 5 V		0.51	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	6	V_{CC} = MAX, V_{in} = 0		0.2	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

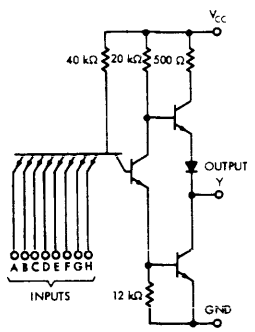
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

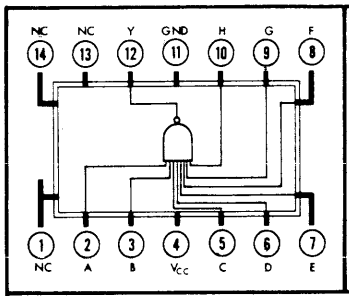
CIRCUIT TYPES SN54L30, SN74L30
8-INPUT POSITIVE NAND GATES

schematic

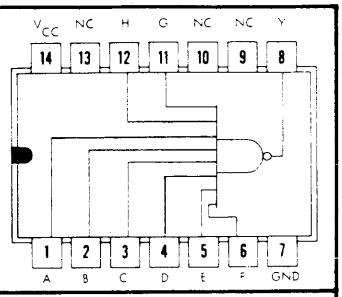


NOTES: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L30 Circuits	4.5	5	5.5	V
SN74L30 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L30 Circuits	−55	25	125	°C
SN74L30 Circuits	0	25	70	°C

8

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

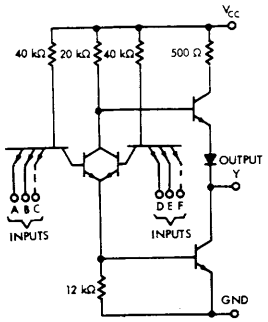
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2		V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.7	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA		2.4		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
			V_{CC} = MAX, V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX, V_{in} = 0, V_{out} = 0		−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V			0.51	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0	SN54L30		0.33	mA
				SN74L30		0.2	

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		70	100	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns

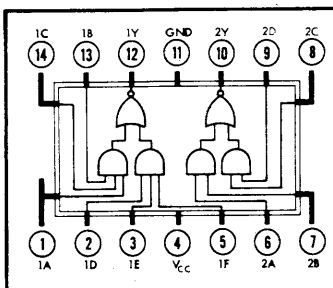
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

schematic (each gate)

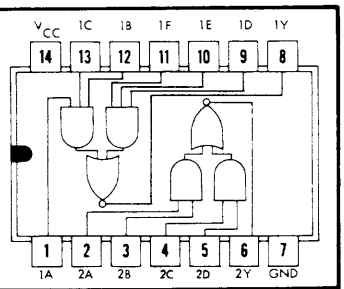


NOTES: 1. Component values shown are nominal.
2. Inputs C and F are available on gate 1 only.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L51 Circuits	4.5	5	5.5	V
SN74L51 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L51 Circuits	−55	25	125	°C
SN74L51 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current (average per gate)	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

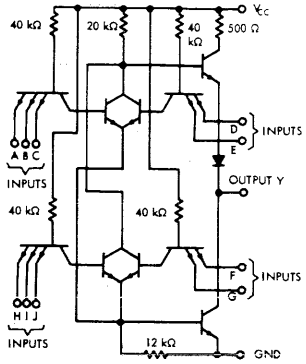
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

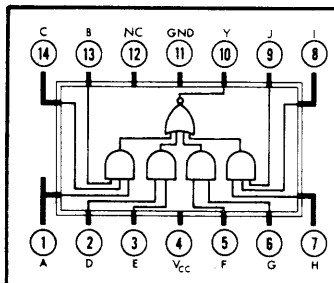
CIRCUIT TYPES SN54L54, SN74L54
4-WIDE 3-2-2-3-INPUT AND-OR-INVERT GATES

schematic



NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

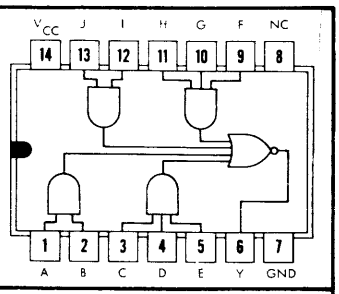
T
FLAT PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABC) + (DE) + (FG) + (HIJ)}$

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic:

$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L54 Circuits	4.5	5	5.5	V
SN74L54 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L54 Circuits	−55	25	125	°C
SN74L54 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

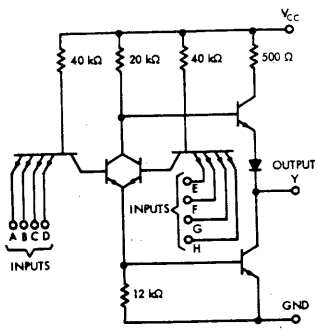
PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals of one AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$ Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$ Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$ Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$ Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
		V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS} Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$ Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.99	mA
$I_{CC(1)}$ Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1} Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

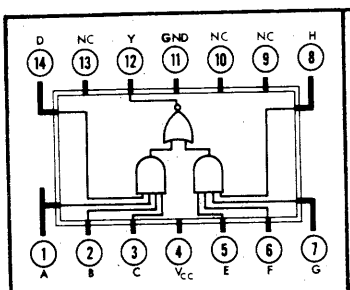
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

schematic

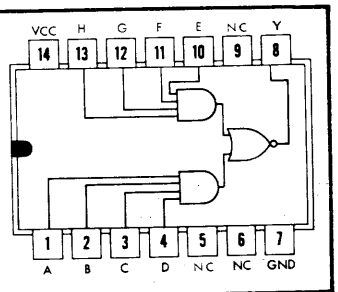


NOTE: 1. Component values shown are nominal.
2. NC — No internal connection

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

$Y = \overline{(ABCD) + (EFGH)}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L55 Circuits	4.5	5	5.5	V
SN74L55 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L55 Circuits	−55	25	125	°C
SN74L55 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	13		2		V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	14			0.7	V
$V_{out(1)}$	Logical 1 output voltage	14	V_{CC} = MIN, V_{in} = 0.7 V, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	13	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	15	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	16	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
I_{OS}	Short-circuit output current	17	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
$I_{CC(0)}$	Logical 0 level supply current	18	V_{CC} = MAX, V_{in} = 5 V		0.65	mA
$I_{CC(1)}$	Logical 1 level supply current	18	V_{CC} = MAX, V_{in} = 0		0.4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	35	C_L = 50 pF, R_L = 4 kΩ		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	35	C_L = 50 pF, R_L = 4 kΩ		50	90	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

8

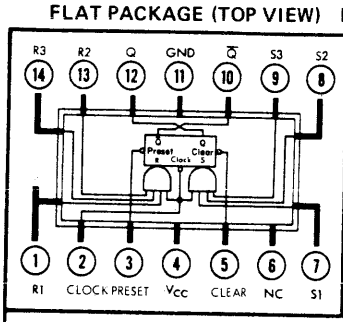
CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

logic

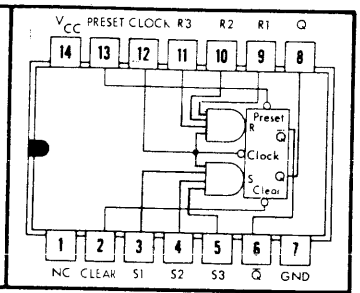
TRUTH TABLE		
t_n		t_{n+1}
R	S	Q
0	0	Q_n
0	1	1
1	0	0
1	1	indeterminate

NOTES: 1. R = R1 • R2 • R3
2. S = S1 • S2 • S3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

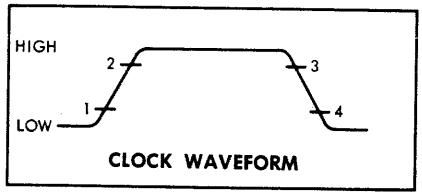


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These R-S flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L71 Circuits	4.5	5	5.5	V
SN74L71 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	100			ns
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L71 Circuits	−55	25	125	°C
SN74L71 Circuits	0	25	70	°C

8

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	19 and 20		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	19 and 20			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	19 and 20			0.6	V
$V_{out(1)}$	Logical 1 output voltage	19	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	20	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at R1, R2, R3, S1, S2, or S3	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	21	V_{CC} = MAX, V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at R1, R2, R3, S1, S2, or S3	22	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	22	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	22	V_{CC} = MAX, V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200∫	μA
I_{os}	Short-circuit output current	23	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	22	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
∫For typical clock input current see page 8-47.

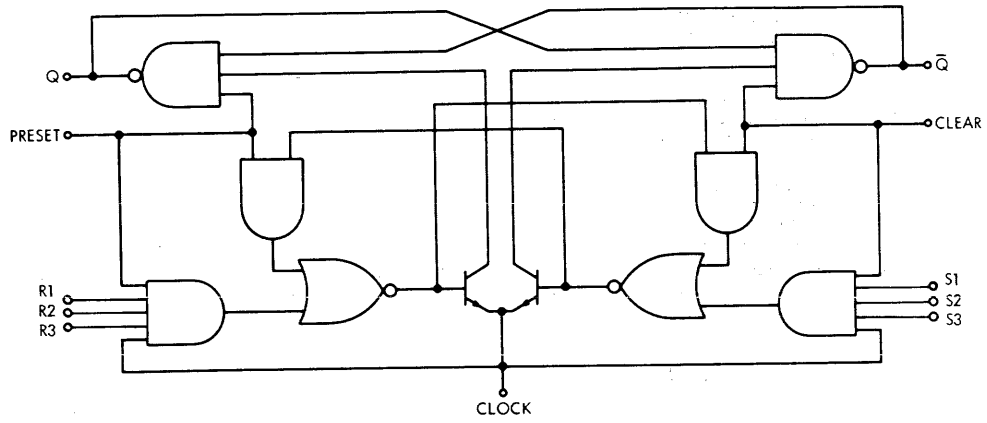
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

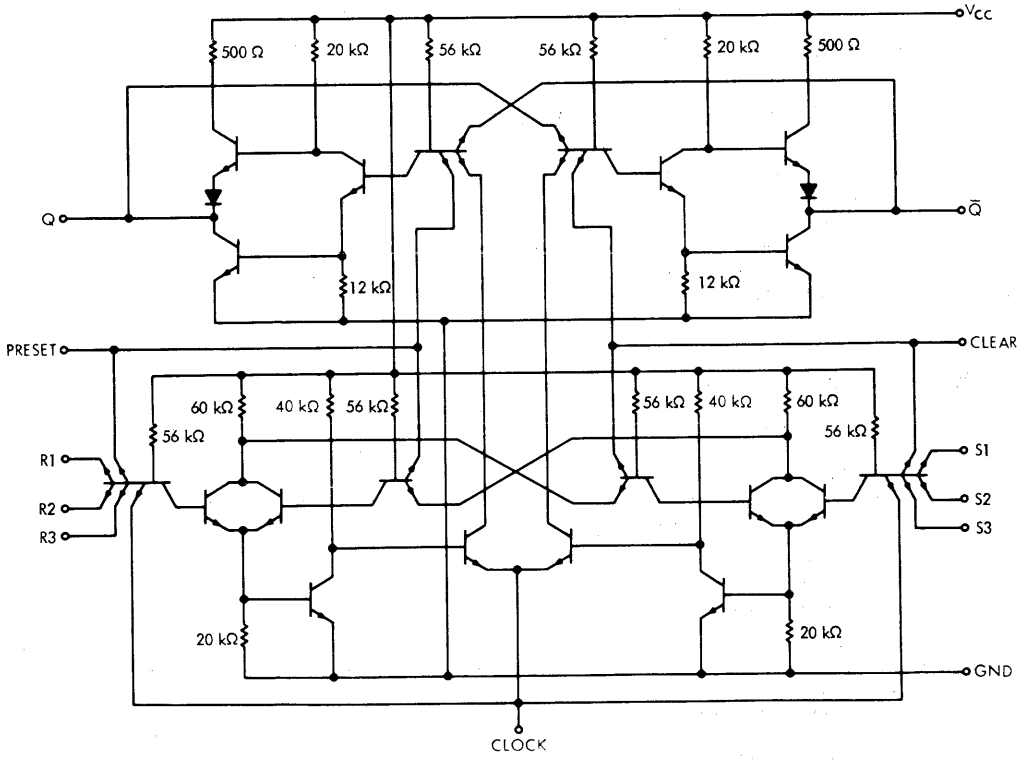
8

CIRCUIT TYPES SN54L71, SN74L71
R-S MASTER-SLAVE FLIP-FLOPS

functional block diagram



schematic



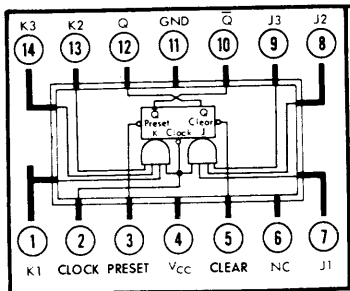
Component values shown are nominal.

logic

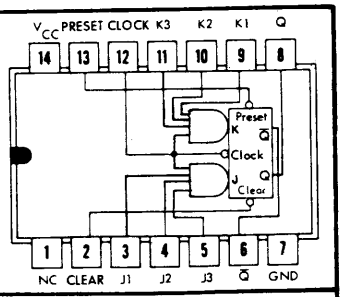
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \bullet J2 \bullet J3$
2. $K = K1 \bullet K2 \bullet K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. NC — No internal connection.

T
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



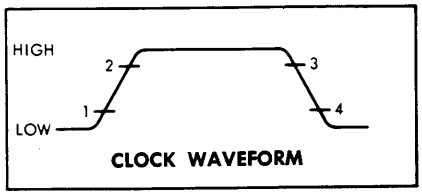
positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L72 Circuits	4.5	5	5.5	V
SN74L72 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 37)	100			ns
Input Setup Time, t_{setup} (See figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L72 Circuits	−55	25	125	°C
SN74L72 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	24 and 25		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	24 and 25			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	24 and 25			0.6	V
$V_{out(1)}$	Logical 1 output voltage	24	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	25	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	26	V_{CC} = MAX, V_{in} = 0.3 V		−0.36‡	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	27	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	27	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	27	V_{CC} = MAX, V_{in} = 2.4 V		−0.2‡	mA
			V_{CC} = MAX, V_{in} = 5.5 V		200‡	μA
I_{os}	Short-circuit output current	28	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current	27	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

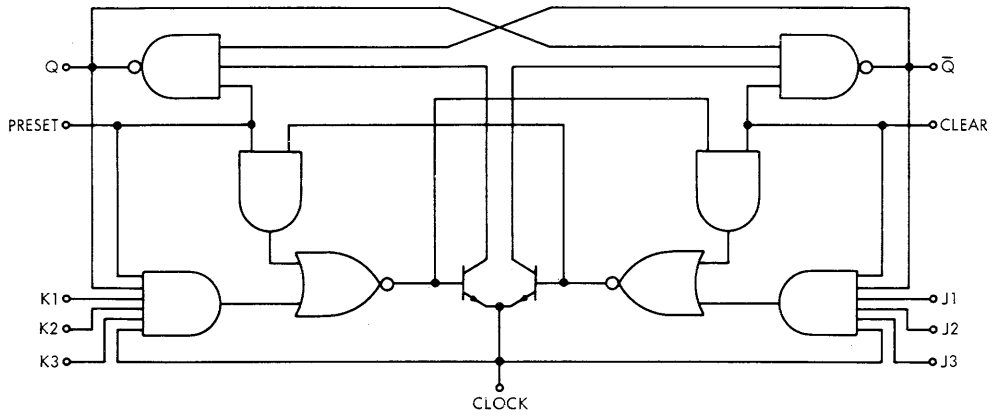
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

‡For typical clock input current see page 8-47.

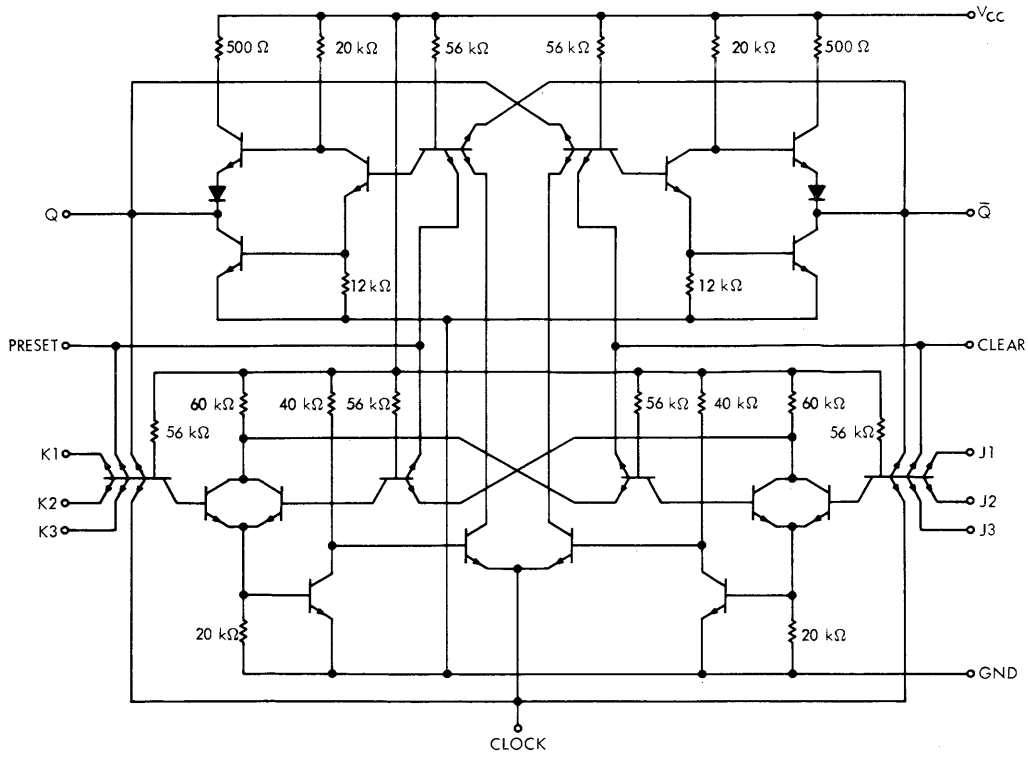
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

functional block diagram



schematic



Component values shown are nominal.

8

CIRCUIT TYPES SN54L73, SN74L73
DUAL J-K MASTER-SLAVE FLIP-FLOPS

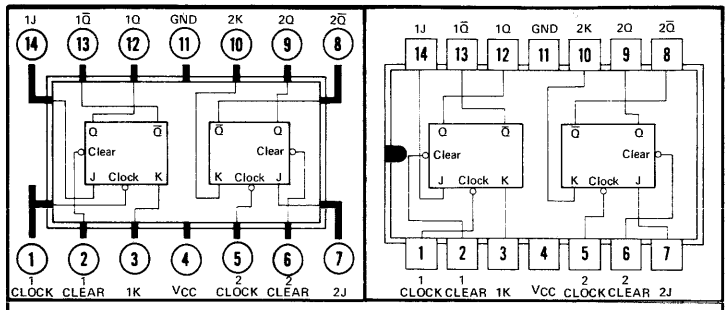
logic

TRUTH TABLE		
t_n		$t_n + 1$
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. $t_n + 1$ = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



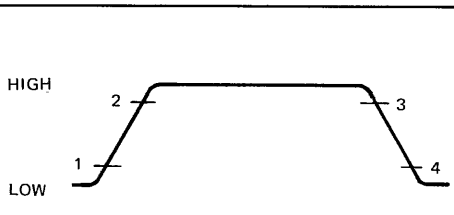
positive logic:
Low input to clear sets Q to logical 0
Clear is independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	SN54L73			SN74L73			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 36)	200			200			ns
Width of preset pulse, $t_{p(preset)}$ (See Figure 37)	100			100			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 37)	100			100			ns
Input setup time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30			2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30				0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30				0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN,	I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN,	I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX,	V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX,	V_{in} = 0.3 V		−0.36∫	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX,	V_{in} = 2.4 V		10	μA
			V_{CC} = MAX,	V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX,	V_{in} = 2.4 V		20	μA
			V_{CC} = MAX,	V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX,	V_{in} = 2.4 V	0∫	−0.2∫	mA
			V_{CC} = MAX,	V_{in} = 5.5 V		200∫	μA
I_{OS}	Short-circuit output current	33	V_{CC} = MAX,	V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current (average per flip-flop)	32	V_{CC} = MAX,	$V_{in(clock)}$ = 0		1.44	mA

†For conditons shown as MIN or MAX, use the appropriate value specified under recommended operating conditons for the applicable circuit type.

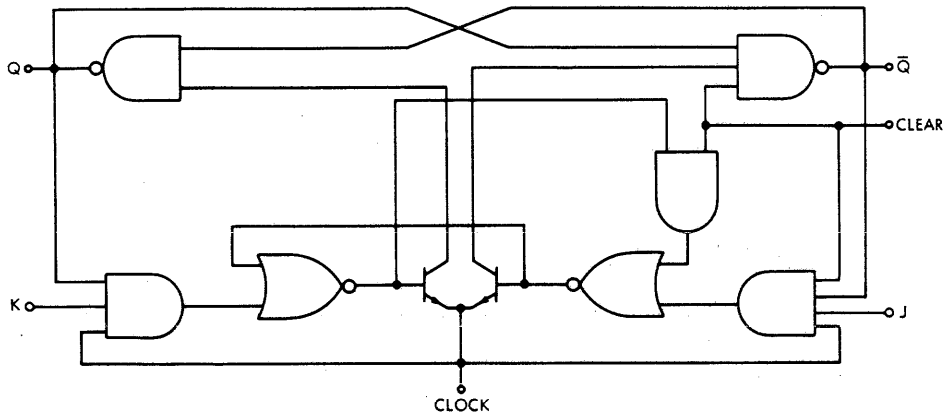
∫For typical clock input current see page 8-47.

8

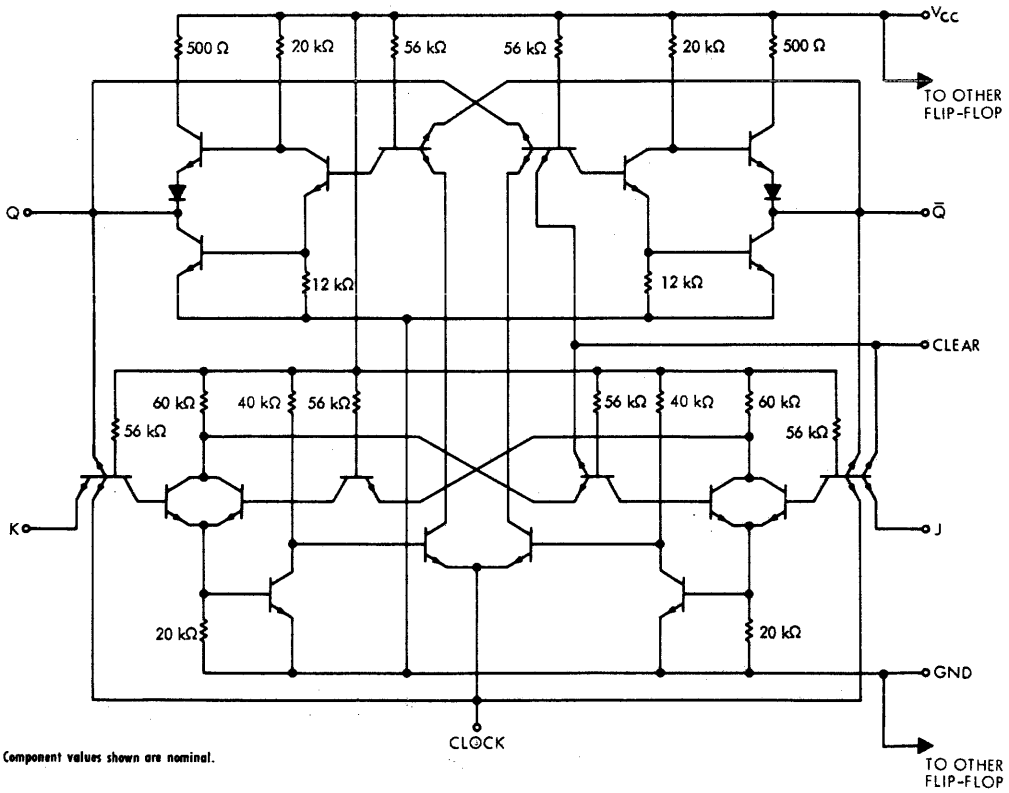
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF,	R_L = 4 kΩ		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF,	R_L = 4 kΩ		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ,	$V_{in(clock)}$ = 2.4 V		60	150	ns
				$V_{in(clock)}$ = 0 V			200	
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF,	R_L = 4 kΩ	10	60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF,	R_L = 4 kΩ	10	35	75	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

- Typical Maximum Clock Frequency . . . 3 MHz
- Positive-Edge Triggering
- Fully Compatible with Most TTL and DTL Circuits
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs

logic

TRUTH TABLE (Each Flip-Flop)

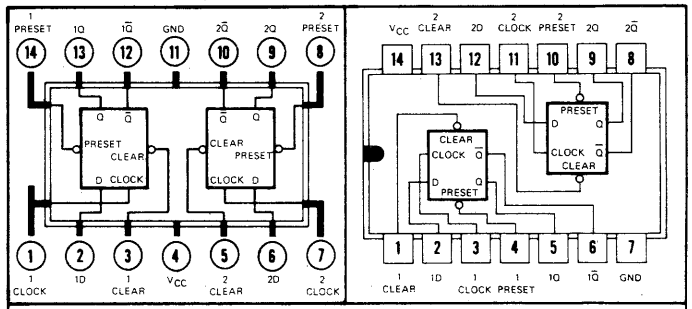
t_n	t_{n+1}	
INPUT	OUTPUTS	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

description

These monolithic, low-power, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54L/74L loads is available from each of the outputs. Maximum clock frequency is typically 3 megahertz, with a typical power dissipation of 4.25 milliwatts per flip-flop.

The SN54L74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L74 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	8 V
Input voltage (see Notes 1 and 2)	5.5 V
Operating free-air temperature range: SN54L74 Circuits	−55°C to 125°C
SN74L74 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L74			SN74L74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$ (see Figure 7 or 8)	200			200			ns
Width of preset pulse, $t_{w(preset)}$ (see Figure 6)	100			100			ns
Width of clear pulse, $t_{w(clear)}$ (see Figure 6)	100			100			ns
Input setup time for either high- or low-level data, t_{setup} (see Note 3 and Figure 7 and 8)	30			30			ns
Input hold time, t_{hold} (See Note 3 and Figure 7 and 8)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡	MIN	MAX	UNIT
V_{IH}	High-level input voltage	35, 36		2		V
V_{IL}	Low-level input voltage	35, 36			0.7	V
V_{OH}	High-level output voltage	35	V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	36	V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_{IH}	High-level input current into D	37	V_{CC} = MAX, V_I = 2.4 V		10	μA
			V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current into preset or clock	37	V_{CC} = MAX, V_I = 2.4 V		20	μA
			V_{CC} = MAX, V_I = 5.5 V		200	μA
I_{IH}	High-level input current into clear	37	V_{CC} = MAX, V_I = 2.4 V		30	μA
			V_{CC} = MAX, V_I = 5.5 V		300	μA
I_{IL}	Low-level input current into preset or D	38	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{IL}	Low-level input current into clear or clock	38	V_{CC} = MAX, V_I = 0.3 V		−0.36	mA
I_{OS}	Short-circuit output current§	39	V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current (each flip-flop)	37	V_{CC} = MAX		1.5	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

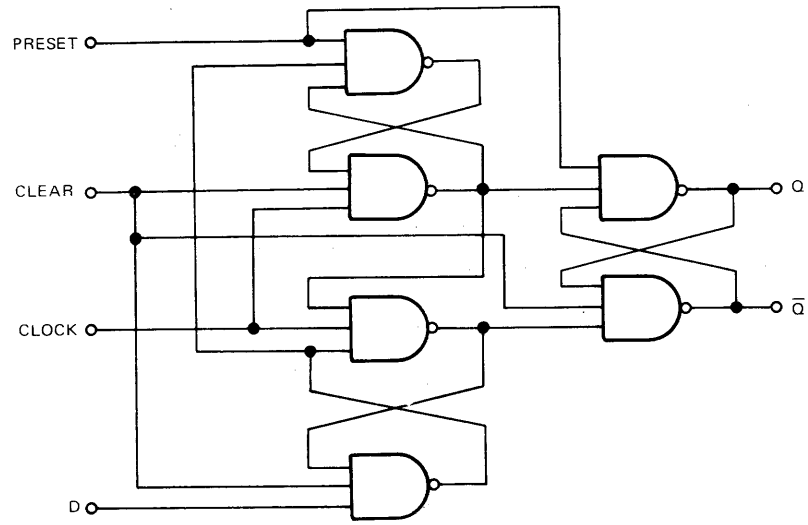
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

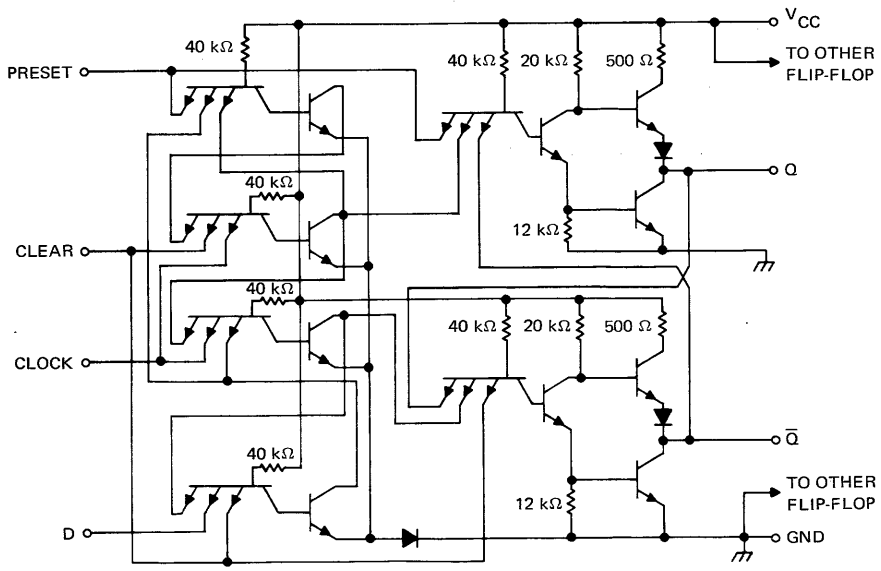
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	44, 45	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset inputs	43			50	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset inputs	43			80	150	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock input	44, 45		10	65	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock input	44, 45		10	65	150	ns

8

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

8

CIRCUIT TYPES SN54L78, SN74L78
DUAL J-K MASTER-SLAVE FLIP-FLOPS

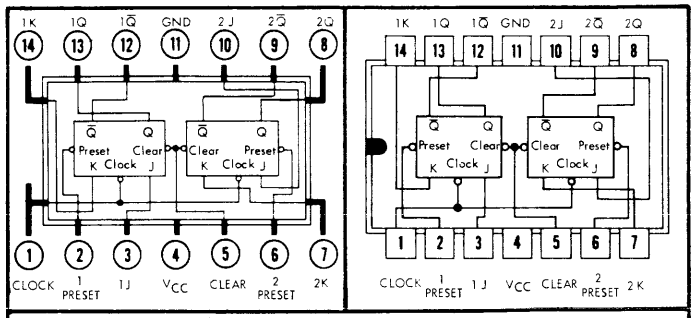
logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

T
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



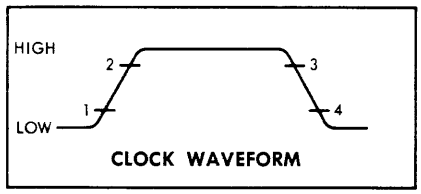
positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

These J-K flip-flop circuits are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

8

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L78 Circuits	4.5	5	5.5	V
SN74L78 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 36)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 37)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 37)	100			ns
Input Setup Time, t_{setup} (See Figure 36)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}	0			
Operating Free-Air Temperature Range, T_A: SN54L78 Circuits	−55	25	125	°C
SN74L78 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	29 and 30		2		V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	29 and 30			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	29 and 30			0.6	V
$V_{out(1)}$	Logical 1 output voltage	29	V_{CC} = MIN, I_{load} = −100 μA	2.4		V
$V_{out(0)}$	Logical 0 output voltage	30	V_{CC} = MIN, I_{sink} = 2 mA		0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.36	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	31	V_{CC} = MAX, V_{in} = 0.3 V		−0.72	mA
$I_{in(1)}$	Logical 1 level input current at J or K	32	V_{CC} = MAX, V_{in} = 2.4 V		10	μA
			V_{CC} = MAX, V_{in} = 5.5 V		100	μA
$I_{in(1)}$	Logical 1 level input current at preset	32	V_{CC} = MAX, V_{in} = 2.4 V		20	μA
			V_{CC} = MAX, V_{in} = 5.5 V		200	μA
$I_{in(1)}$	Logical 1 level input current at clear	32	V_{CC} = MAX, V_{in} = 2.4 V		40	μA
			V_{CC} = MAX, V_{in} = 5.5 V		400	μA
$I_{in(1)}$	Logical 1 level input current at clock	32	V_{CC} = MAX, V_{in} = 2.4 V	0§	−0.4§	mA
			V_{CC} = MAX, V_{in} = 5.5 V		400§	μA
I_{os}	Short-circuit output current	34	V_{CC} = MAX, V_{in} = 0, V_{out} = 0	−3	−15	mA
I_{CC}	Supply current (average per flip-flop)	32	V_{CC} = MAX, $V_{in(clock)}$ = 0		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

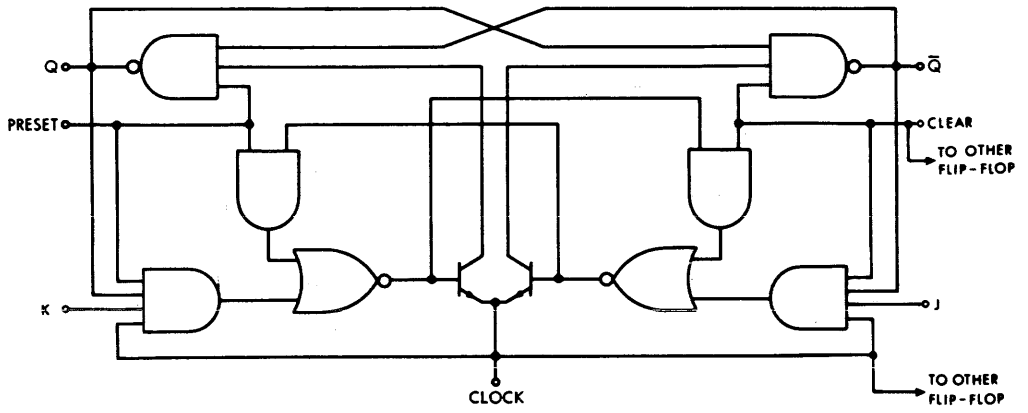
§For typical clock input current see page 8-47.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

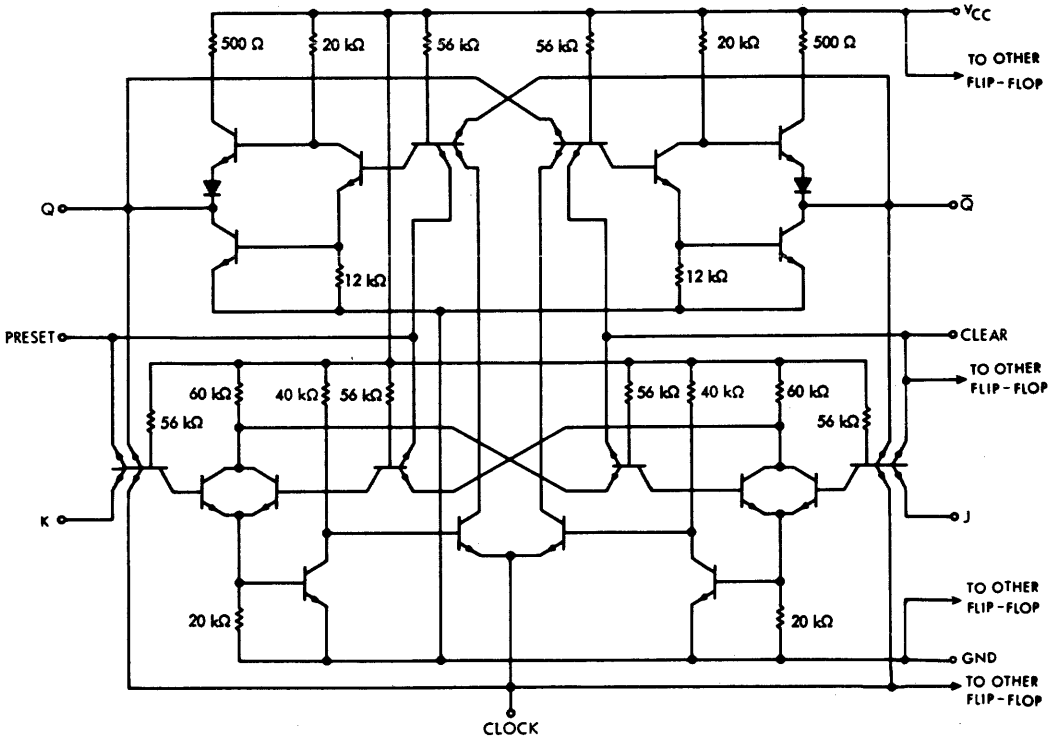
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	36	C_L = 50 pF, R_L = 4 kΩ		3		MHz
t_{pd0}	Propagation delay time to logical 0 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 2.4 V		60	150	ns
			C_L = 50 pF, R_L = 4 kΩ, $V_{in(clock)}$ = 0 V			200	ns
t_{pd1}	Propagation delay time to logical 1 level from clear to output	37	C_L = 50 pF, R_L = 4 kΩ		35	75	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	36	C_L = 50 pF, R_L = 4 kΩ	10	60	150	ns

8

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

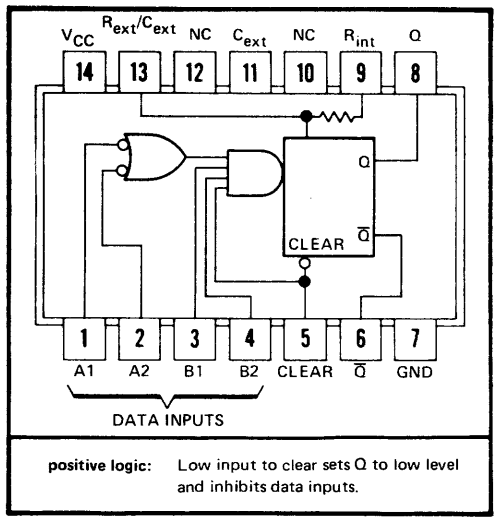
CIRCUIT TYPES SN54L122, SN74L122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- D-C Triggered from High- or Low-Level Gated Logic inputs
- Typical Power Dissipation, 50% Duty Cycle . . . . 55 mW
- Typical Average Propagation Delay to Output Q . . . . 40 ns
- Diode-Clamped Inputs
- Fully Compatible with Most TTL and DTL Circuits

TRUTH TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

J OR N DUAL-IN-LINE OR
T FLAT PACKAGE (TOP VIEW)†
(See Note B thru F)



positive logic: Low input to clear sets Q to low level and inhibits data inputs.

†Pin assignments for these circuits are the same for all packages.

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = no internal connection.
C. To use the internal timing resistor of SN54L122/SN74L122 (20 kΩ), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
E. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
F. To obtain variable pulse width, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

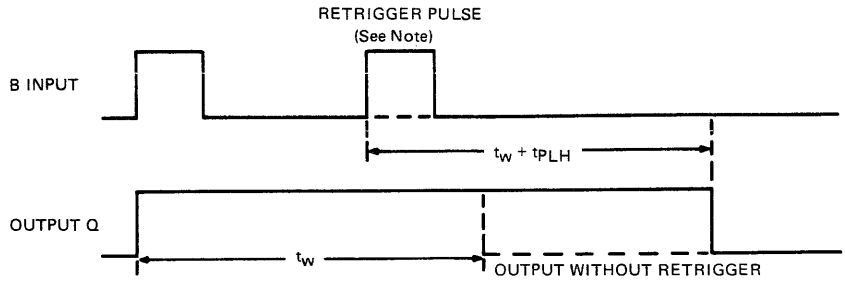
8

CIRCUIT TYPES SN54L122, SN74L122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

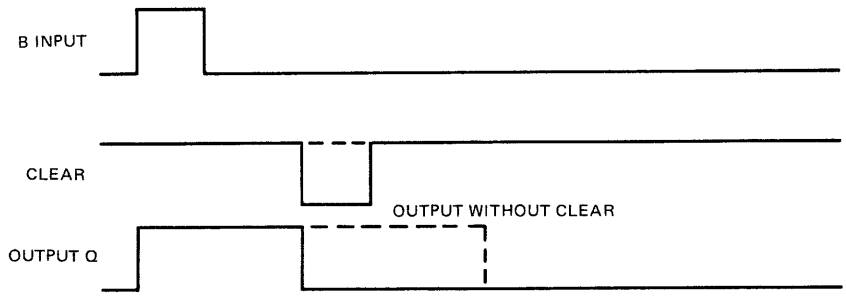
description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 40 normalized Series 54L/74L gate loads is available from each of the outputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



OUTPUT PULSE CONTROL USING RETRIGGER PULSE



OUTPUT PULSE CONTROL USING CLEAR INPUT

FIGURE A–TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

description (continued)

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The SN54L122/SN74L122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\ R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leqslant 1000$ pF, see Figure 2.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one-shot is 55 milliwatts; typical average propagation delay time to the Q output is 40 nanoseconds. The SN54L122 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L122 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage, SN54L122 Circuits only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L122 Circuits . . . . . −55°C to 125°C
SN74L122 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

8

			SN54L122			SN74L122			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	Series 54L/74L Gates				40			40	
	Series 54L/74L Gates with 8-kΩ base resistors¶	High logic level			20			20	
		Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3 and Figure 1)			50			50			ns
Input data hold time, t_{hold} (see Note 4 and Figure 1)			50			50			ns
Width of clear pulse, $t_{w(clear)}$			50			50			ns
External timing resistance			5		25	5		50	kΩ
External capacitance			No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal					50			50	pF
Operating free-air temperature, T_A			−55		125	0		70	°C

¶This applies for all data inputs of circuit types SN54L122 and SN74L122.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the SN54L122/SN74L122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = −400 μA,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 8 mA,			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			20	μA
		clear input					40	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.8	mA
		clear input					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 5	−5		−2.0	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX,	See Notes 6 and 7		11	14	mA

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

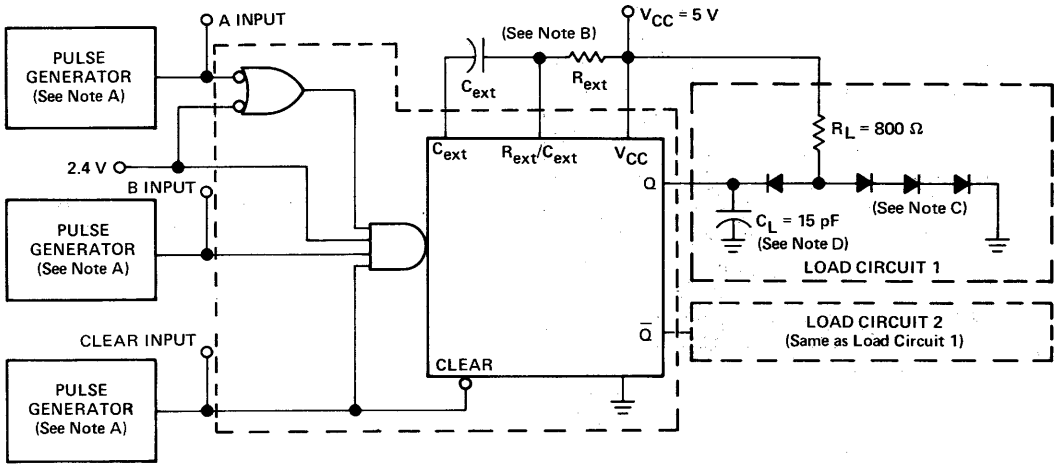
8

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Figure 1	R_{ext} = 5 kΩ, R_L = 800 Ω,		44	66	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				38	56	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				60	80	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				54	72	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				36	54	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				60	80	ns
$t_{w(min)}$	Minimum width of Q output pulse				90	130	ns
t_w	Width of Q output pulse	C_{ext} = 400 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 800 Ω	1.7	1.9	2.1	μs

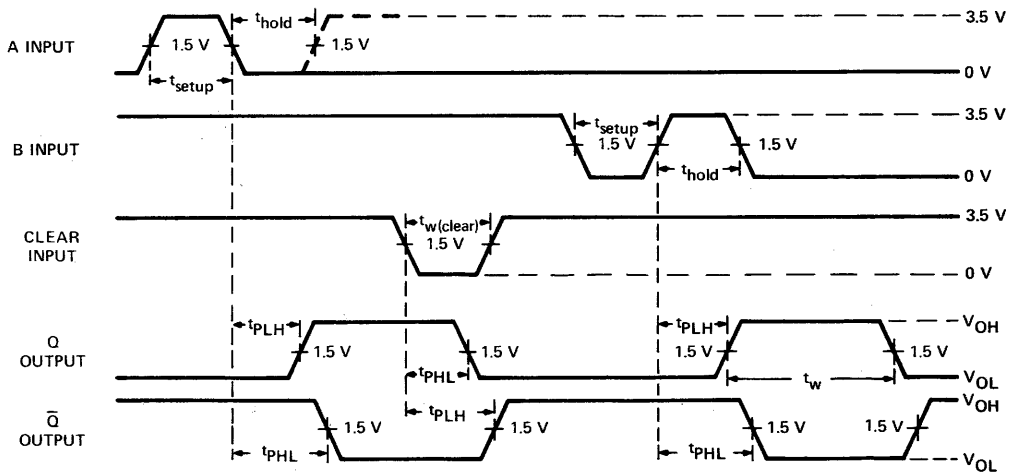
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns (10% to 90% level), $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. See Test Conditions, switching characteristics table, page 3, for values of R_{ext} and C_{ext}.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

8

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

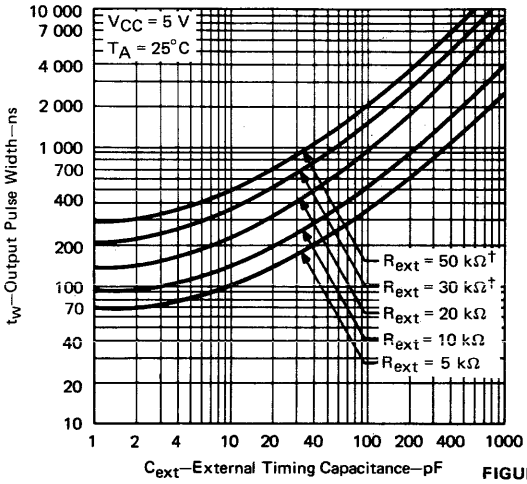
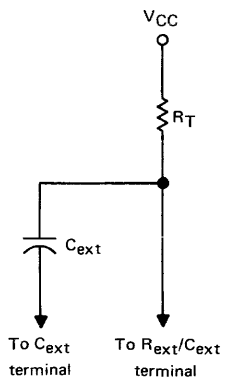


FIGURE 2

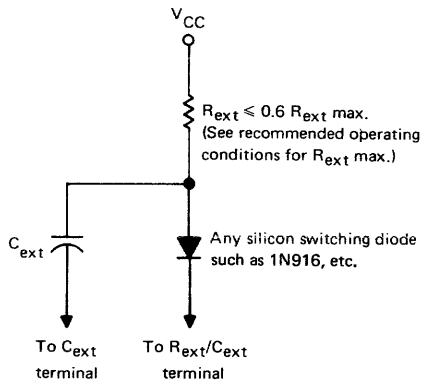
†These values of resistance exceed the maximums recommended for use over the full temperature range of the SN54L122.

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} \leq$ 1000 pF

FIGURE B



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

FIGURE C

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure C be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

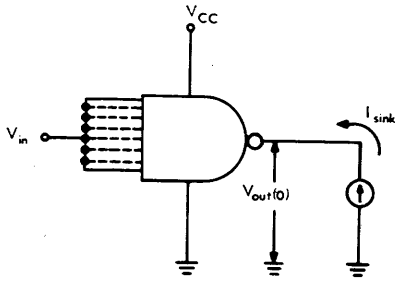
$$t_w = 0.28\ R_{ext}C_{ext}\left(1 + \frac{0.7}{R_{ext}}\right)$$

where

R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

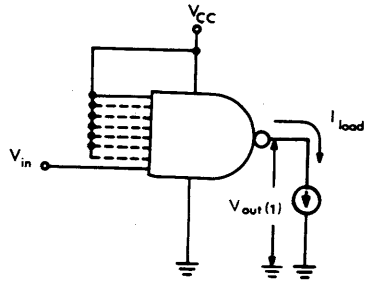
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



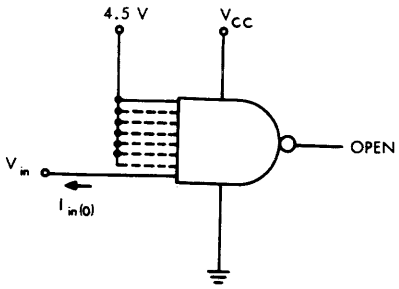
1. All inputs are tested simultaneously.

FIGURE 1



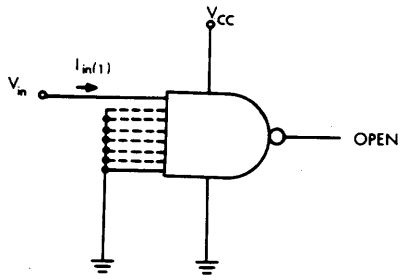
1. Each input is tested separately.

FIGURE 2



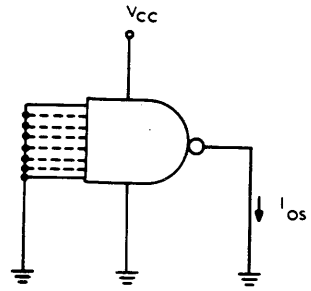
1. Each input is tested separately.

FIGURE 3



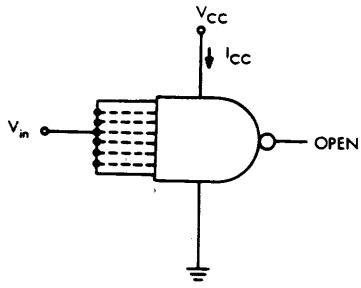
1. Each input is tested separately.

FIGURE 4



1. Each gate is tested separately.

FIGURE 5



1. Logical 0 and logical 1 conditions are tested.
2. All gates are tested simultaneously.

$$\text{Average-per-gate value} = \frac{I_{CC\ total}}{\text{number of gates in package}}.$$

FIGURE 6

§Arrows indicate actual direction of current flow.

8

PARAMETER MEASUREMENT INFORMATION

d-c test circuits §

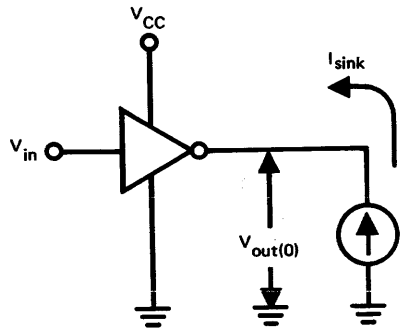


FIGURE 7

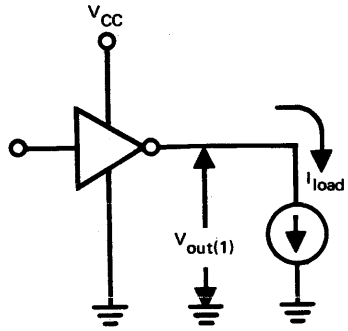


FIGURE 8

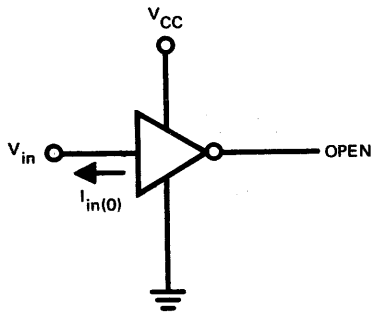


FIGURE 9

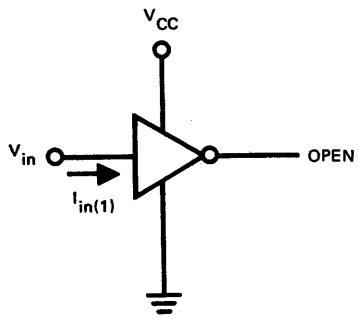
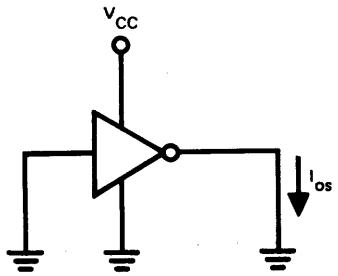
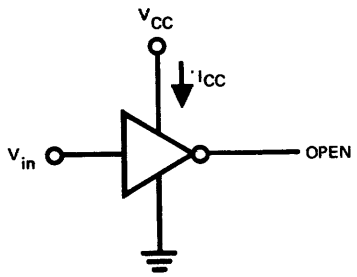


FIGURE 10



1. Each inverter is tested separately.

FIGURE 11



1. All inverters are tested simultaneously.
2. For SN54L04/SN74L04 the average-per-inverter value = $\frac{I_{CC}\text{ total}}{\text{number of inverters in package}}$

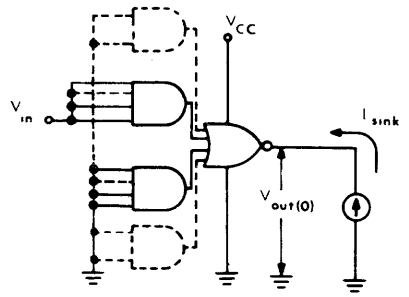
FIGURE 12

§Arrows indicate actual direction of current flow.

8

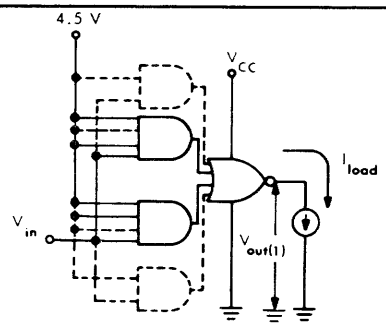
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



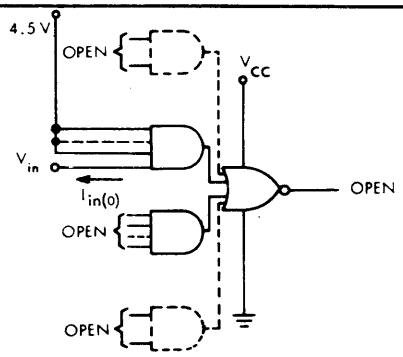
1. Each AND section is tested separately.

FIGURE 13



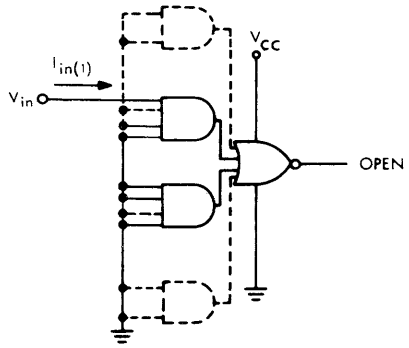
1. Each set of inputs is tested separately.

FIGURE 14



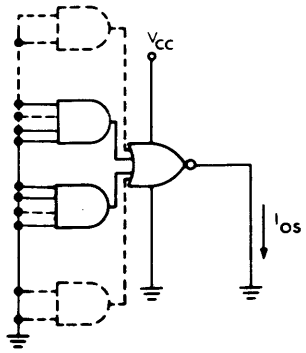
1. Each input is tested separately.

FIGURE 15



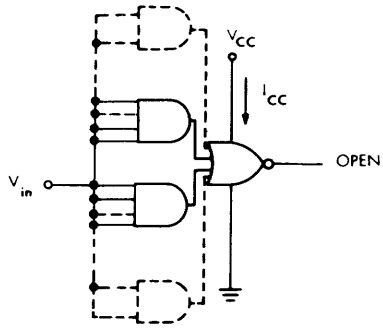
1. Each input is tested separately.

FIGURE 16



1. Each gate is tested separately.

FIGURE 17



1. All gates are tested simultaneously.

$$\text{Average-per-gate value} = \frac{I_{CC}\ \text{total}}{\text{number of gates in package}}$$

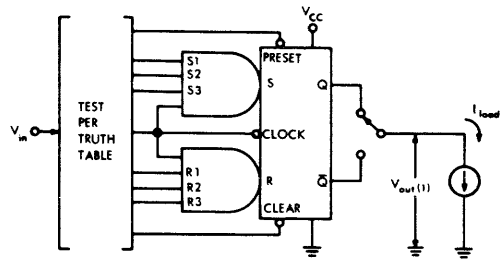
FIGURE 18

§Arrows indicate actual direction of current flow.

8

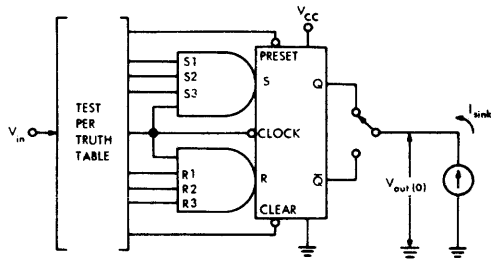
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



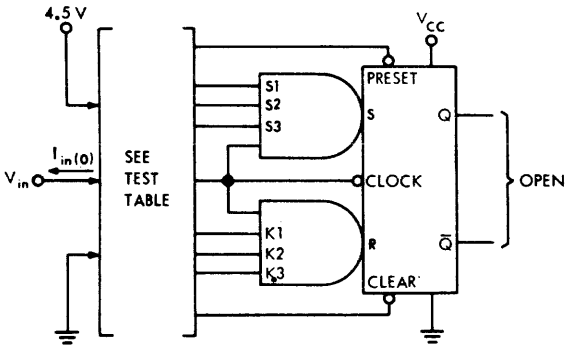
1. Each output is tested separately.

FIGURE 19



1. Each input is tested separately.

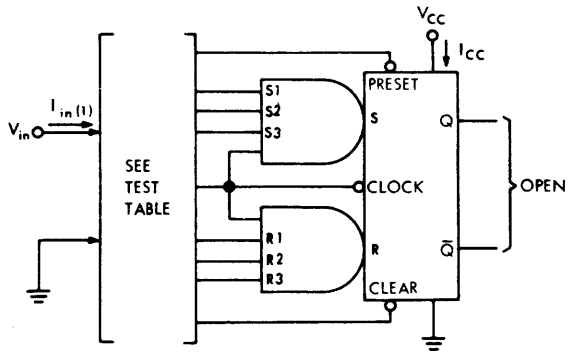
FIGURE 20



TEST TABLE	
Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V
Clock	Preset, R1, R2, R3, S1, S2, and S3
Clock	Clear, R1, R2, R3, S1, S2, and S3
Preset	R1, R2, R3, S1, S2, and S3
Clear	R1, R2, R3, S1, S2, and S3
R1	Preset, Clock, R2, and R3
R2	Preset, Clock, R1, and R3
R3	Preset, Clock, R1, and R2
S1	Clear, Clock, S2, and S3
S2	Clear, Clock, S1, and S3
S3	Clear, Clock, S1, and S2

1. Each input is tested separately.

FIGURE 21



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, R1, R2, R3, S1, S2, and S3
Preset	Clock, R1, R2, and R3
Clear	Clock, S1, S2, and S3
R1	Clock, Preset, R2, and R3
R2	Clock, Preset, R1, and R3
R3	Clock, Preset, R1, and R2
S1	Clock, Clear, S2, and S3
S2	Clock, Clear, S1, and S3
S3	Clock, Clear, S1, and S2

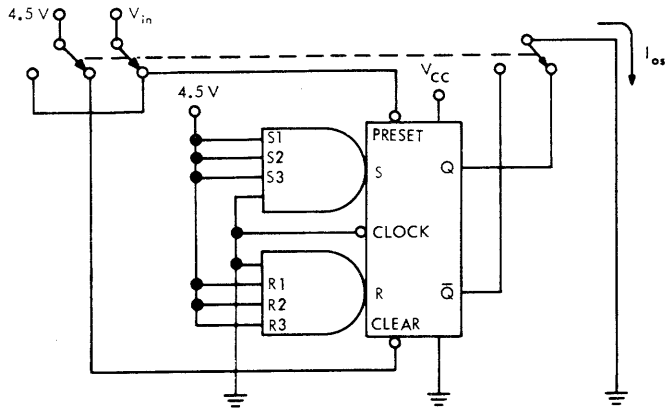
1. Each input is tested separately.

FIGURE 22

§Arrows indicate actual direction of current flow.

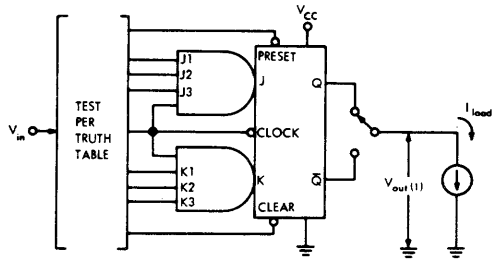
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)



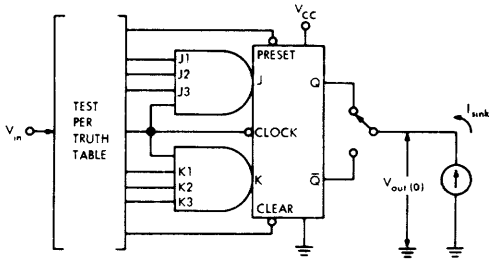
1. Each output is tested separately.

FIGURE 23



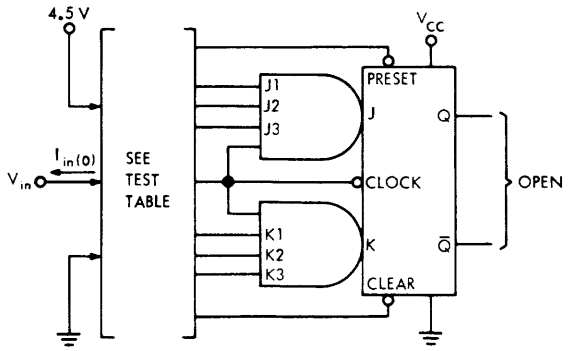
1. Each output is tested separately.

FIGURE 24



1. Each output is tested separately.

FIGURE 25



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

1. Each input is tested separately.

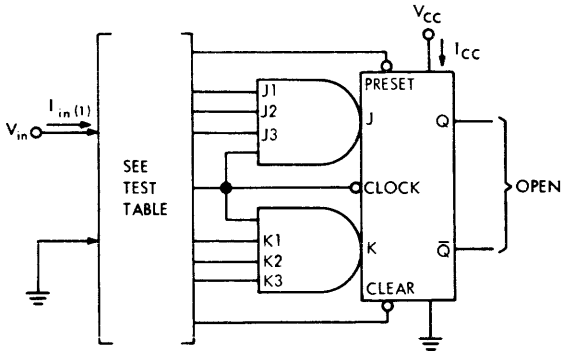
FIGURE 26

§Arrows indicate actual direction of current flow.

8

PARAMETER MEASUREMENT INFORMATION

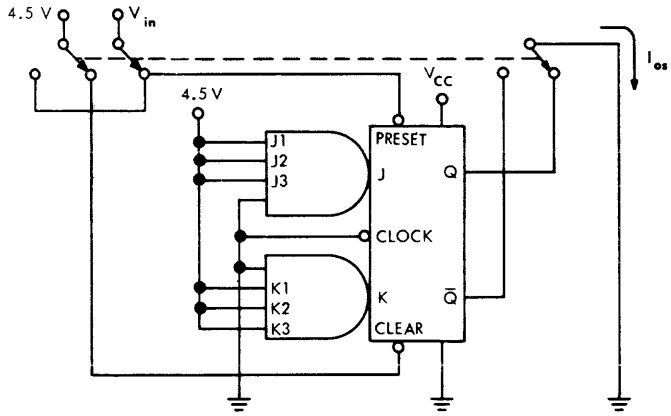
d-c test circuits § (continued)



TEST TABLE	
Apply V_{in} (Test $I_{in(1)}$)	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

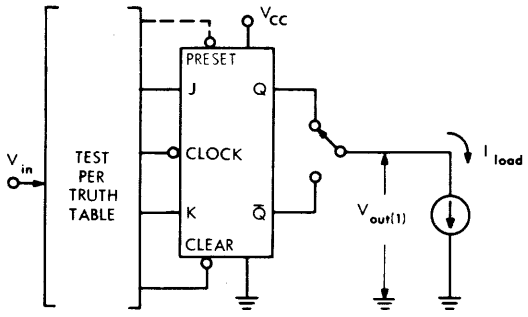
1. Each input is tested separately.

FIGURE 27



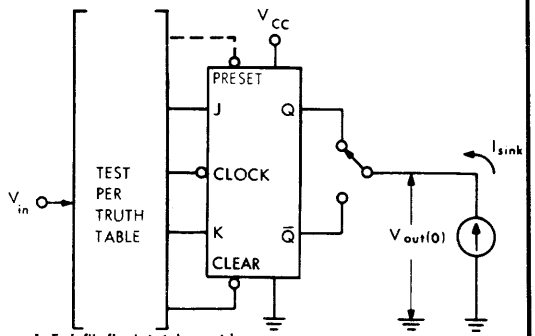
1. Each output is tested separately.

FIGURE 28



1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 29



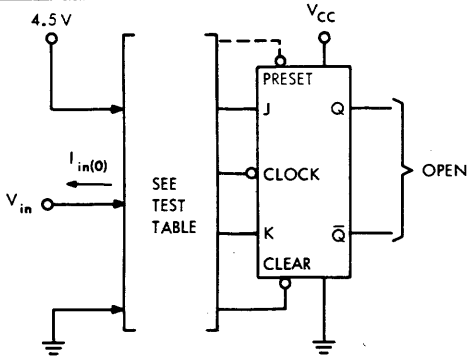
1. Each flip-flop is tested separately.
2. Each output is tested separately.
3. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 30

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

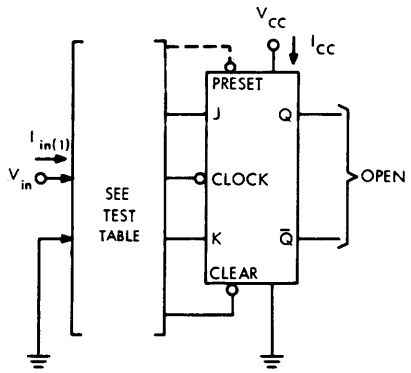
d-c test circuits§ (continued)



TEST TABLE		
Apply V_{in} (Test $I_{in(0)}$)	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
Preset	None (See Note 5)	Clock and K
J	Q (See Note 3)	Clock and Clear
K	$\overline{Q}$ (See Note 3)	Clock and Clear

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and $\overline{Q}$ are left floating.
4. Ground all inputs of the unused flip-flop.
5. Preset is applicable for SN54L78/SN74L78 circuits only.

FIGURE 31

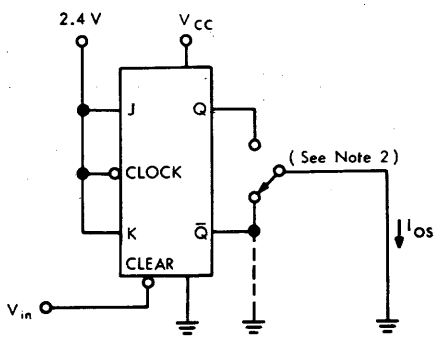


TEST TABLE		
Apply V_{in} (Test $I_{in(1)}$)	Ground	Apply Momentary GND, then 4.5 V
Clock	Clear, J, and K	None
Clear	Clock and J	None
Preset (See Note 1)	Clock and K	None
J (See Note 1)	Clock and Clear	Preset
K (See Note 3)	Clock and Preset	Clear

1. Preset is applicable for SN54L78/SN74L78 circuits only.
2. I_{CC} is measured (simultaneously for both flip-flops) for the following conditions:
   a. J = K = Clock = Clear = Gnd. For SN54L78/SN74L78, Preset = 4.5 V.
   b. For SN54L73/SN74L73: J = Clear = 4.5 V, K = Gnd, and apply momentary 4.5 V, then Gnd, to Clock.
   For SN54L78/SN74L78: J = K = Clock = Preset = Gnd and Clear = 4.5 V.

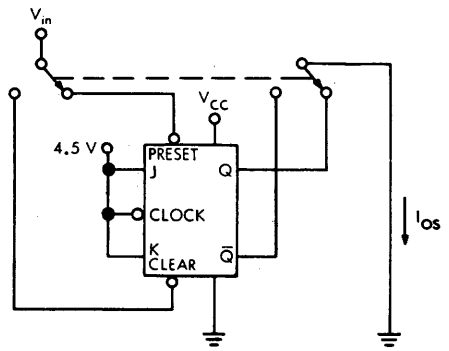
   Average per flip-flop = $\frac{I_{CC\ total}}{2}$.
3. Each flip-flop is tested separately for $I_{in(1)}$

FIGURE 32



1. Each flip-flop is tested separately.
2. Test circuit shows setup for testing $\overline{Q}$. When testing Q, open all inputs and ground $\overline{Q}$.

FIGURE 33

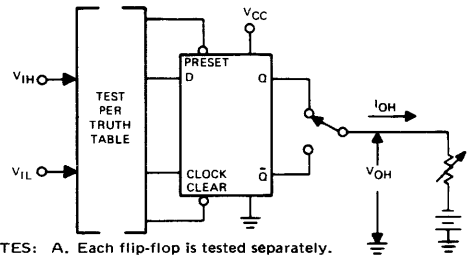


1. Each flip-flop is tested separately.

FIGURE 34

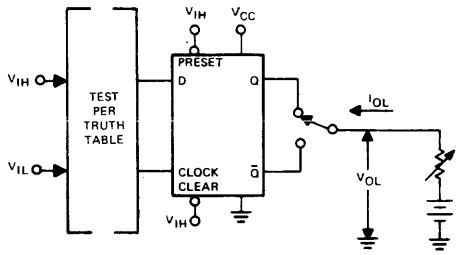
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



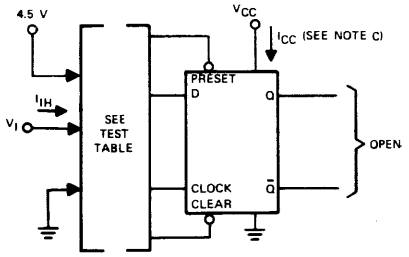
NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.
C. V_{OH} is also tested using Clear and Preset inputs.

FIGURE 35–V_{IH}, V_{IL}, V_{OH}



NOTES: A. Each flip-flop is tested separately.
B. Each output is tested separately.

FIGURE 36–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

APPLY V_I (TEST I_{IH})	APPLY 4.5 V	APPLY GND
Clock	Clear and D	Preset
Clock	Preset and D	Clear
Preset	Clear and D	Clock (See Note B)
Clear	Preset	Clock, D, and Q
Clear	Preset	D and Clock (See Note B)
D	Preset and Clock	Clear

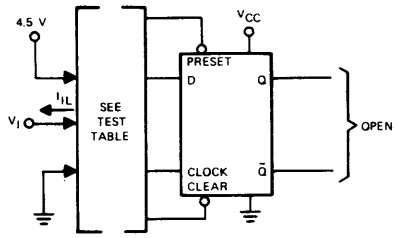
NOTES: A. Each input of each flip-flop is tested separately for I_{IH}.
B. GND is momentarily applied to Clock, then 4.5 V.
C. I_{CC} is measured simultaneously for both flip-flops with D, Clock, and Preset at GND; then with D, Clock, and Clear at GND.

FIGURE 37–I_{IH}, I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



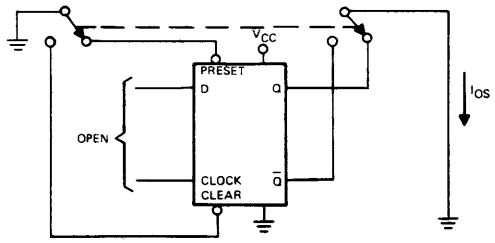
TEST TABLE

APPLY V_I (TEST I_{IL})	APPLY 4.5 V	APPLY GND
Clock	Clear	Preset and D
Preset	Clear	Clock and D
Clear	Clock, D, and Preset	None
D	Clear and Clock	Preset

NOTES: A. Each flip-flop is tested separately.
B. Each input is tested separately.

FIGURE 38–I_{IL}

8



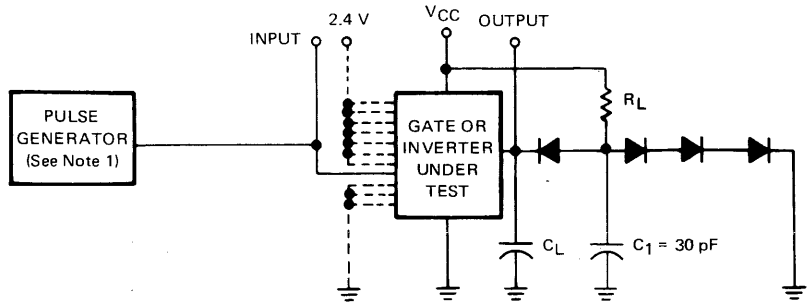
NOTE: Each output is tested separately.

FIGURE 39–I_{OS}

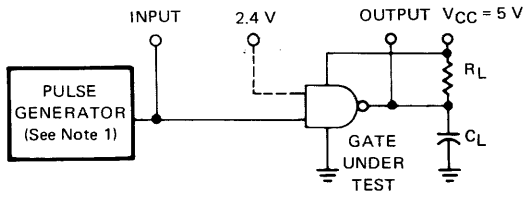
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

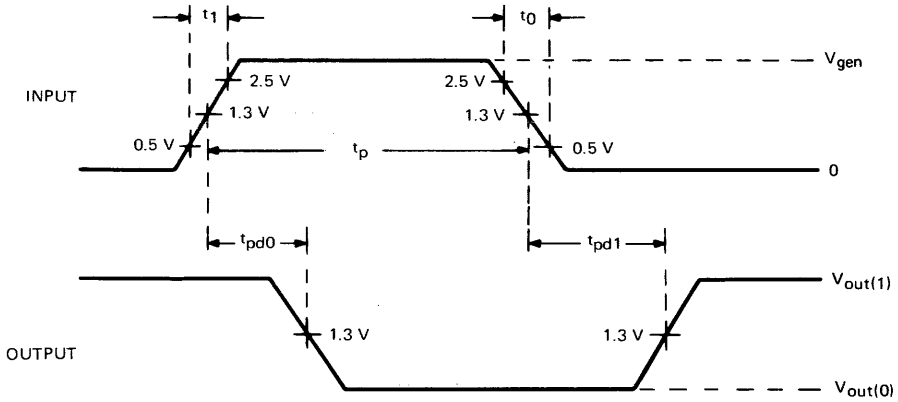
switching characteristics



TEST CIRCUIT FOR SN54L00, SN54L02, SN54L04, SN54L10, SN54L20, SN54L30, SN54L51, SN54L54, SN54L55, SN74L00, SN74L02, SN74L04, SN74L10, SN74L20, SN74L30, SN74L51, SN74L54, AND SN74L55



TEST CIRCUIT FOR SN54L01, SN54L03, SN74L01, SN74L03



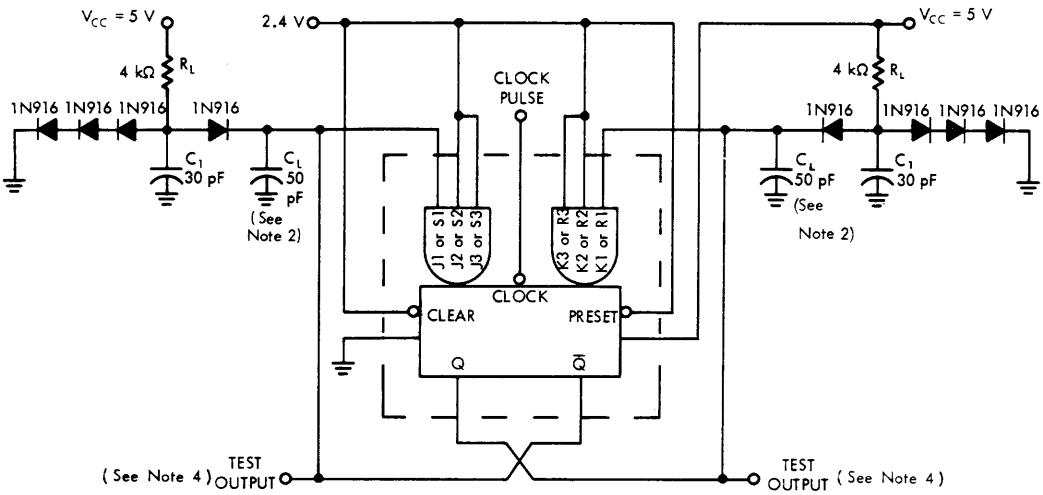
VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristic: V_{gen} = 3 V, t_0 = 60 ns, t_1 = 60 ns, t_p = 1 µs, PRR ≤ 500 kHz, Z_{out} ≈ 50 Ω.
2. All diodes are 1N916 or equivalent.
3. $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
4. C_L includes probe and jig capacitance.
5. When testing the SN54L00/SN74L00 through SN54L30/SN74L30 (except SN54L02/SN74L02), connect all unused inputs to 2.4 V. When testing the SN54L02/SN74L02 or SN54L51/SN74L51 through SN54L55/SN74L55, apply the input pulse to one input of one AND section and 2.4 V to all unused inputs of that AND section. All inputs of unused AND sections are grounded.

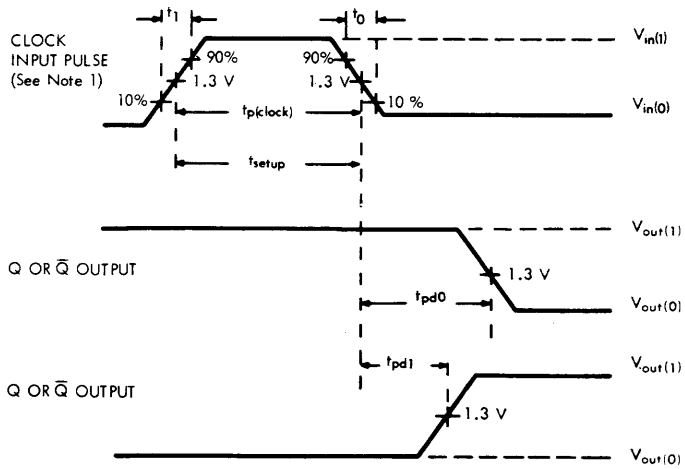
FIGURE 40–GATE PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

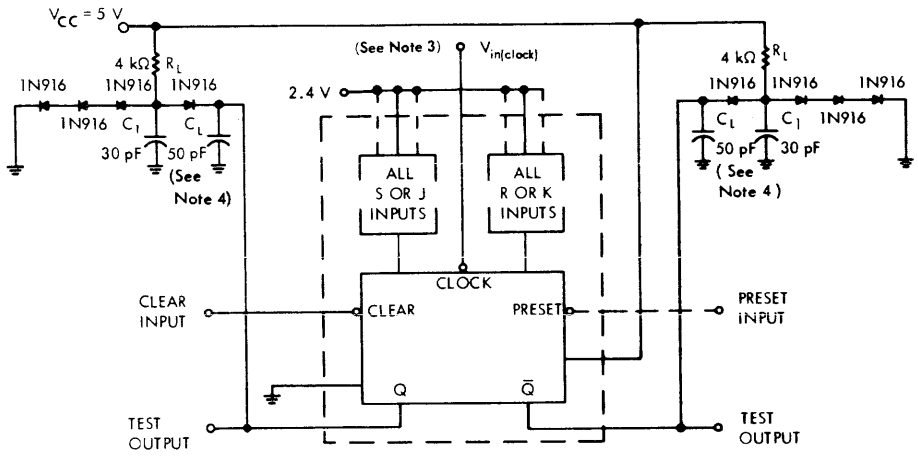
NOTES: 1. Clock input characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_p \geq 200$ ns, and PRR = 500 kHz. When testing f_{max}, vary PRR.
2. C_L includes probe and jig capacitance.
3. For SN54L73/SN74L73 and SN54L78/SN74L78, J = K = 2.4 V.
4. Load is applied only to output under test.

FIGURE 41—FLIP-FLOP CIRCUITS SYNCHRONOUS INPUTS SWITCHING TIMES

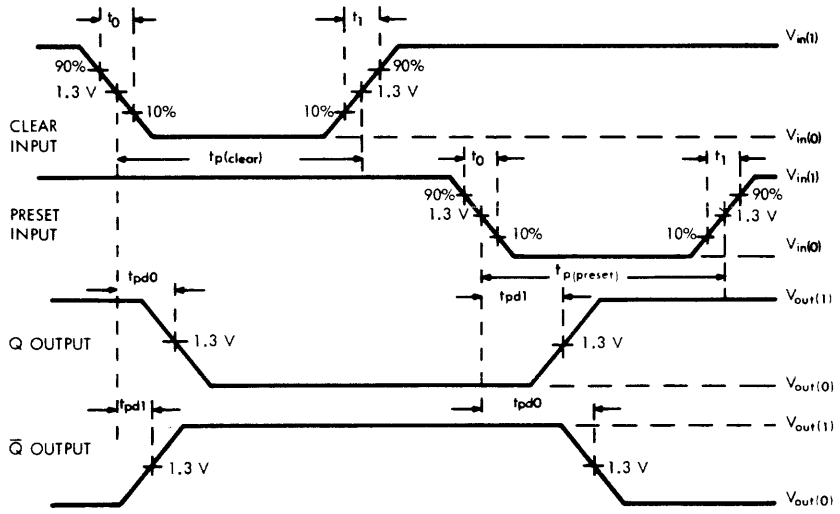
8

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



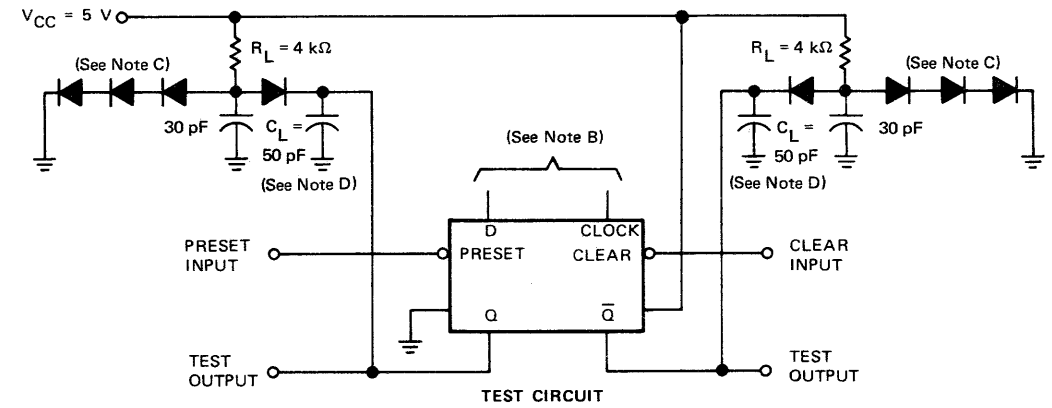
VOLTAGE WAVEFORMS

NOTES: 1. Clear or preset inputs dominate regardless of the state of clock or logic inputs.
2. Clear or preset input pulse characteristics: $V_{in(0)} \leq 0.4$ V, $V_{in(1)} \geq 2.4$ V, $t_1 = t_0 = 15$ ns, $t_{p(clear)} = t_{p(preset)} \geq 100$ ns, and PRR $\leq$ 500 kHz.
3. See applicable circuit type for actual synchronous and asynchronous input configurations.
4. C_L includes probe and jig capacitance.

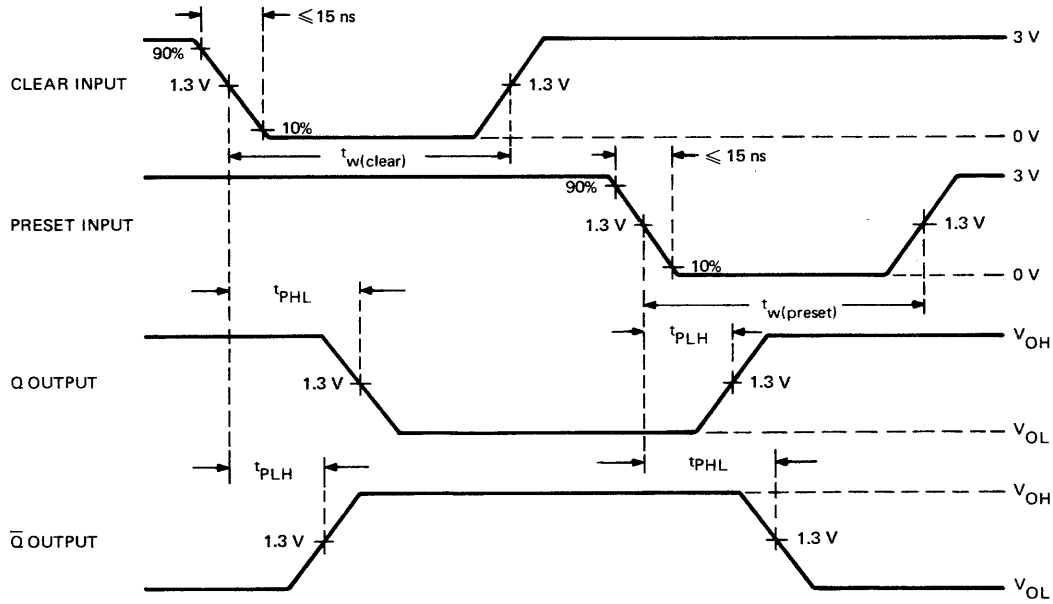
FIGURE 42–FLIP-FLOP CIRCUITS ASYNCHRONOUS INPUTS SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

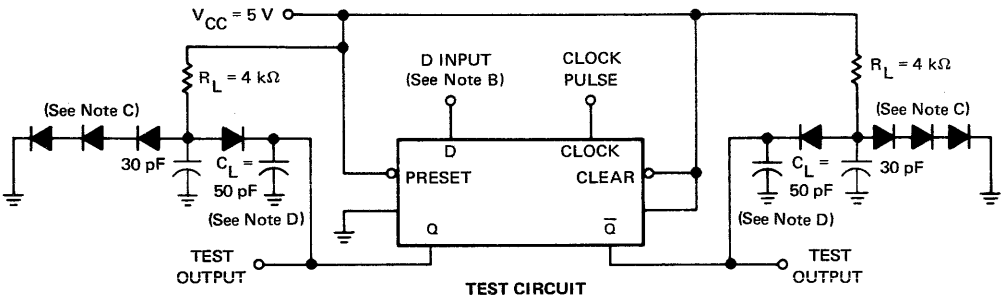
NOTES: A. Clear or Preset input pulse characteristics: $t_{w(clear)} = t_{w(preset)} \geqslant 100$ ns, PRR $\leqslant$ 500 kHz.
B. Clear and Preset inputs dominate regardless of the state of Clock or D inputs.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 43–ASYNCHRONOUS INPUTS SWITCHING CHARACTERISTICS

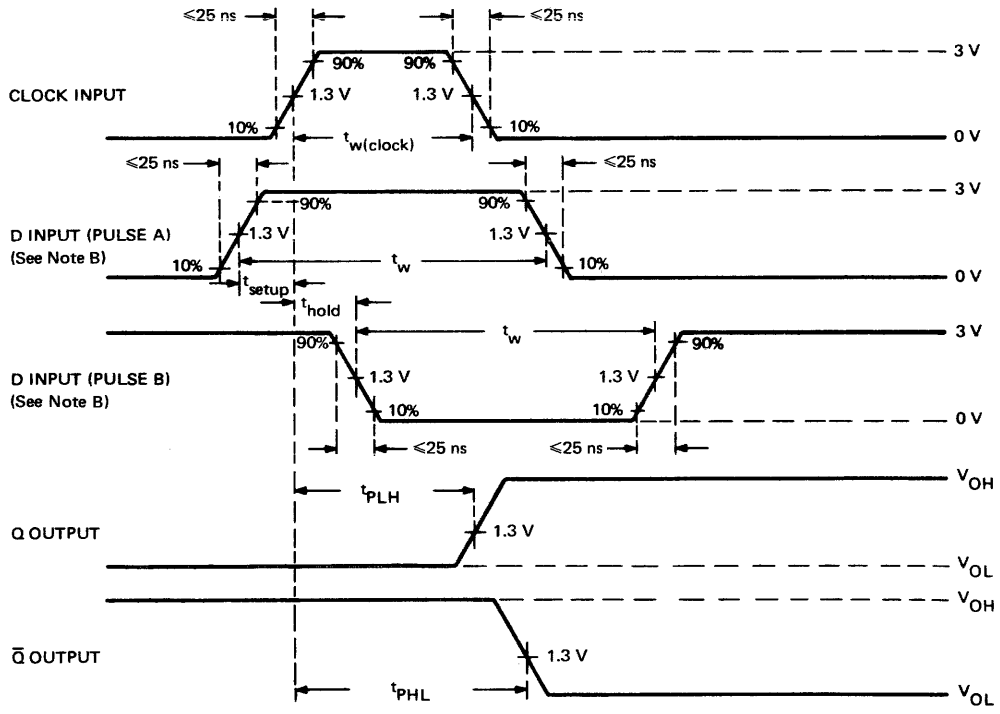
8

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



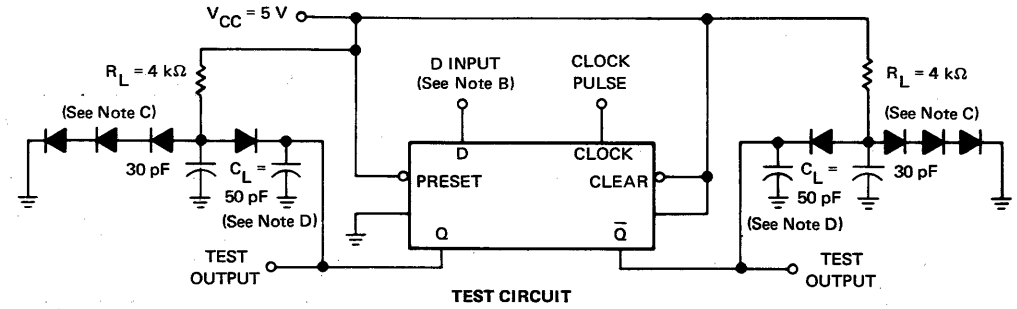
VOLTAGE WAVEFORMS

NOTES: A. Clock input pulse has the following characteristics: $t_{w(clock)} \geq 200$ ns and PRR $\leq$ 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

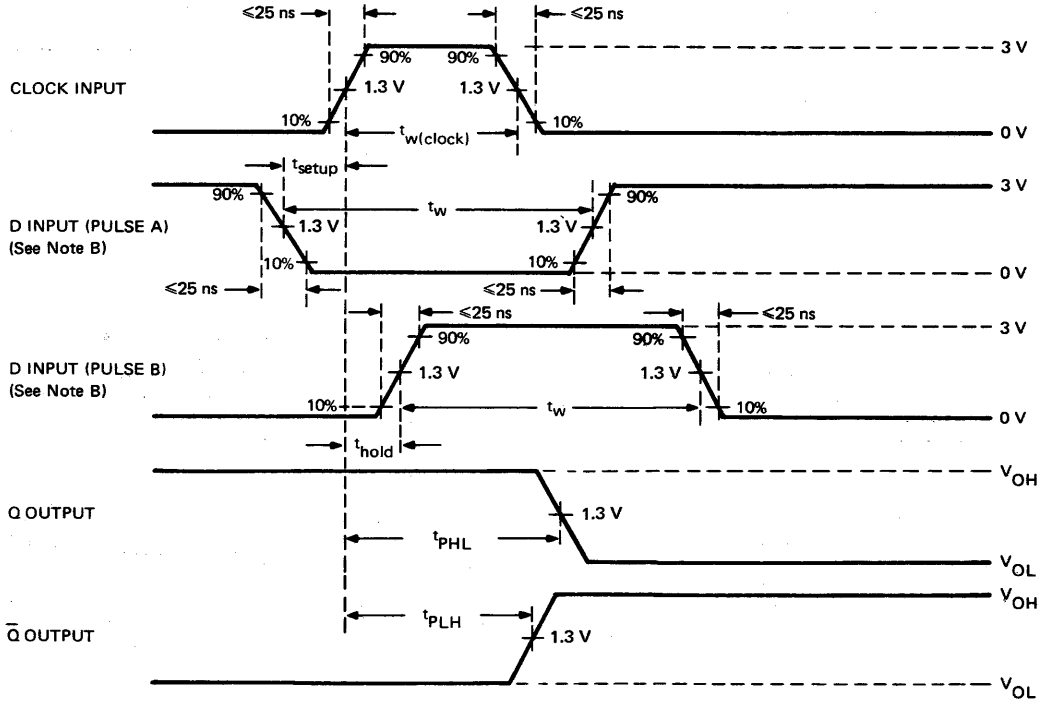
FIGURE 44–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (HIGH-LEVEL DATA)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

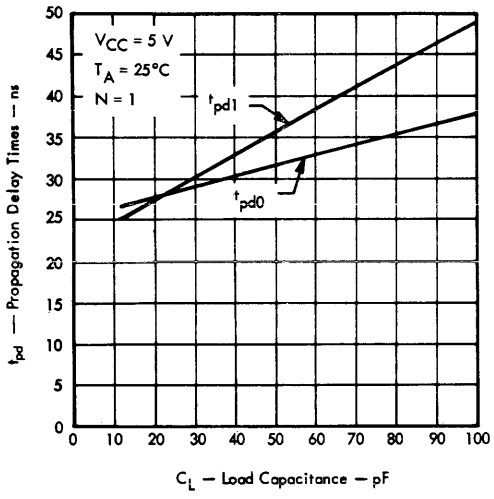
NOTES: A. Clock input pulse has the following characteristics: $t_w \geq 200$ ns and PRR $\leq$ 500 kHz. When testing f_{max}, vary PRR.
B. D input (pulse A) has the following characteristics: t_{setup} = 30 ns, t_w = 100 ns, and PRR is 50% of the clock PRR. D input (pulse B) has the following characteristics: t_{hold} = 0 ns, t_w = 80 ns, and PRR is 50% of the clock PRR.
C. All diodes are 1N916.
D. C_L includes probe and jig capacitance.

FIGURE 45–SWITCHING CHARACTERISTICS, CLOCK AND SYNCHRONOUS INPUTS (LOW-LEVEL DATA)

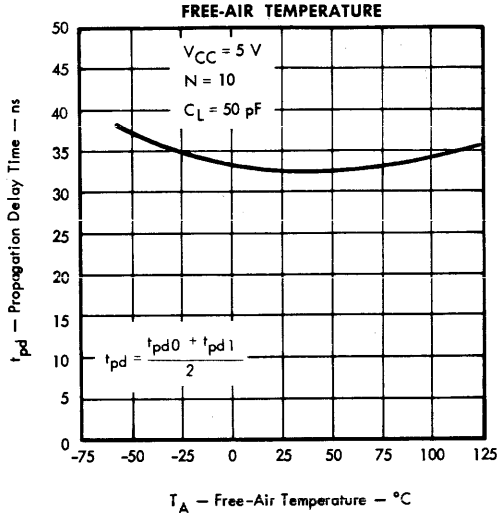
8

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES vs LOAD CAPACITANCE

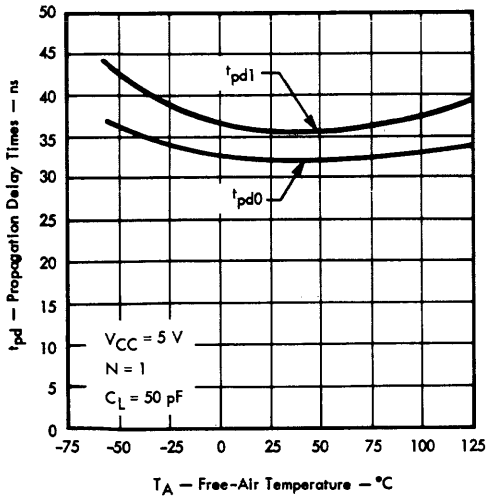


PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

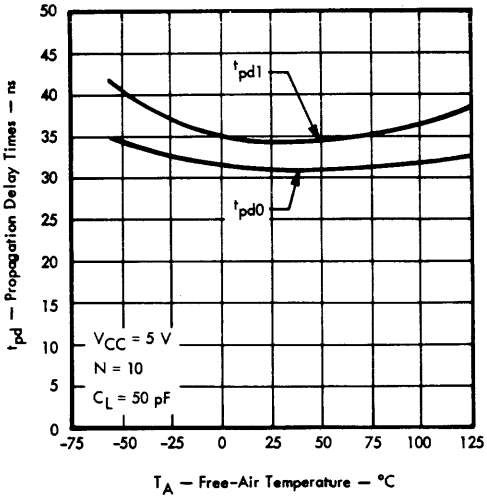


8

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE



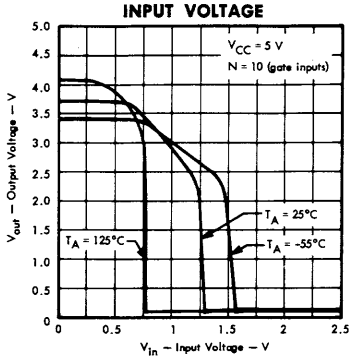
PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE



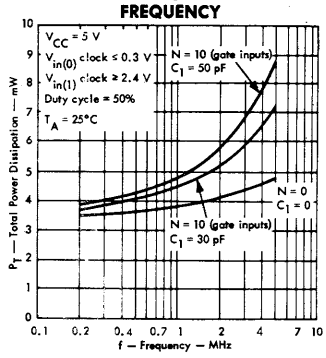
†SN54L00/SN74L00, SN54L10/SN74L10, and SN54L20/SN74L20. Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

TYPICAL CHARACTERISTICS†

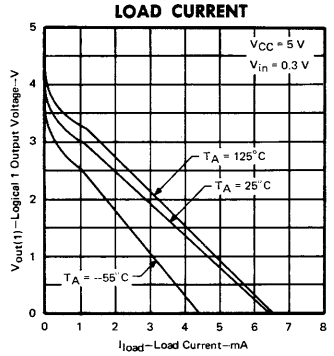
OUTPUT VOLTAGE vs INPUT VOLTAGE



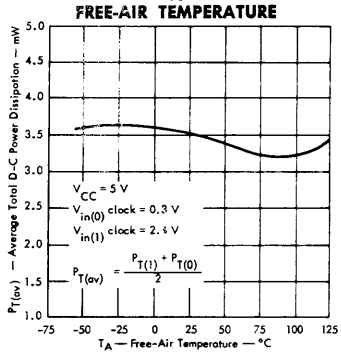
TOTAL POWER DISSIPATION‡ vs FREQUENCY



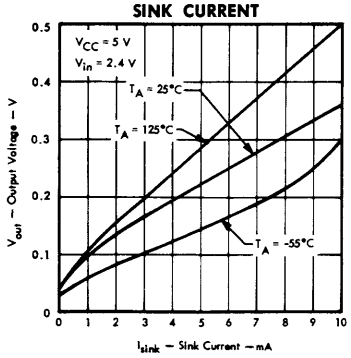
OUTPUT VOLTAGE vs LOAD CURRENT



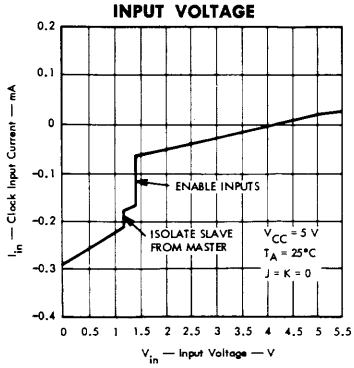
AVERAGE TOTAL D-C POWER DISSIPATION‡ § vs FREE-AIR TEMPERATURE



OUTPUT VOLTAGE vs SINK CURRENT



CLOCK INPUT CURRENT ‡ § vs INPUT VOLTAGE



† Data for temperatures below 0°C and above 70°C is applicable to Series 54L circuits only.

‡Each flip-flop.
§Value of I_{in} for SN54L78 and SN74L78 is twice the amount shown.

8

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222