Manual Update

Document Title: TMS380 Adapter Chipset User's Guide
TMS380 Adapter Chipset User's Guide Supplement

Document Number: SPWU001D, SPWU003 Revision: F

This document updates the TMS380 Adapter Chipset User's Guide, Revision D, document number SPWU001D, dated July 1986, and the TMS380 Adapter Chipset User's Guide Supplement (which includes Revision E), document number SPWU003, dated August 1987.

TMS380 Adapter Chipset User's Guide, SPWU001D

Page	Change or Add
2-9	Section 2.4, PC AT Adapter Card Example. The schematic supports standard 6-MHz PC AT buses. For higher-speed buses, when the TMS380 is in 16-bit mode, 8-bit DIO using SBHE and A0 should be used. This is to avoid timing problems with IOCHRDY for wait state generation.
2-11	Figure 2-5 should be replaced with the new Figure 2-5 on page 12 of this manual update.
3-8	Add the following paragraph to the bottom of section 3.4.2. Also shown in Figure 3-3 is a structure called an abort delimiter. The abort delimiter consists of a Starting Delimiter and Ending Delimiter sequence. The abort delimiter is transmitted by the TMS380 Adapter whenever the Adapter detects a 'false free token' as described in Section 3.10.2.
3-8	Add the following to Figure 3-3.

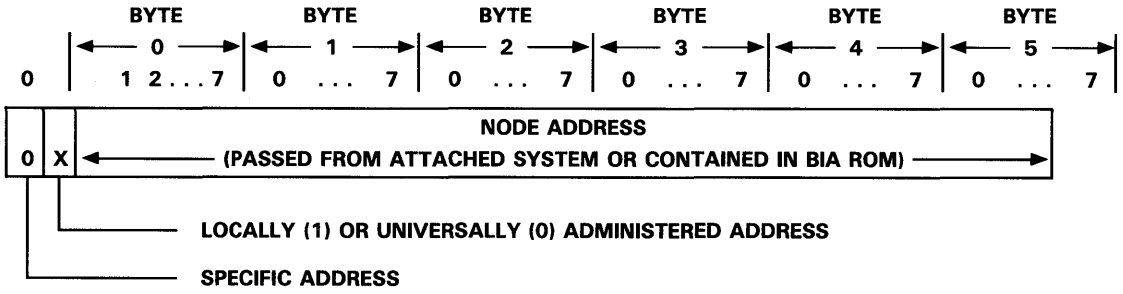
ABORT DELIMITER:

SDEL 1 BYTE	EDEL 1 BYTE

3-14	The last paragraph on this page should be changed to read as follows: A ring station address assigned by the attached system or contained in the BIA ROM must conform to the format shown in Figure 3-14. Note that bit 0 of byte 0 must be set to zero. Bit 1 of byte 0 may be set to either 0 or 1 when the TMS38021 Protocol Handler is used but must be set to 1 when the TMS38020 Protocol Handler is used. Violating these conditions causes the Adapter to reject the address assignment with a node address error.

TEXAS INSTRUMENTS

3-14 Figure 3-14 should be replaced with the following figure:



3-15 Section 3.5.2, Source Routing, has been updated per recent IEEE 802.5 activity. Section 7.1.3 of the TMS380 Adapter Chipset User's Guide Supplement should be consulted in lieu of this section. Please reference the IEEE 802.5 source routing proposals for current developments regarding source routing specifications.

3-42 Add the following note to the end of Section 3.8.5.2.

> **Note:**
>
> When the TMS38021 Protocol Handler ROM code is used or when the DLC Software is used, the Adapter will execute the Beacon Transmit Autoremoval Test after 16 seconds have passed during beacon if the adapter has not proceeded to Monitor Contention mode during beacon transmit.

3-47 Add the following note to the end of Section 3.8.7.2.

> **Note:**
>
> When the TMS38021 Protocol Handler ROM code is used or when the DLC Software is used, the Lobe Media Test MAC frame is 1048 bytes in length, and the frame will be transmitted 511 times for this phase of insertion.

4-7 Figure 4-5, sheet 1. The R24 resistor connected to the $\overline{\text{CHPTST}}$ pin (pin J10) and the $\overline{\text{TEST}}$ pin (pin G8) of the TMS38030 should be removed. These two pins should be left unconnected.

4-9 Figure 4-5, sheet 3 of the Adapter Chipset Interconnect Schematic should be replaced with the new sheet 3 on page 13 of this update.

4-10 Figure 4-5 sheet 4. The value for capacitor C3 should be changed to 22,000 pF ± 10%, and a Note 4 reference added. The following should be added to the bottom of the page as Note 4:

NOTE 4: For additional noise immunity, the value for C3 has been increased to 22,000 pF. For existing designs, the original 6,800 pF value may be used.

4-22 Replace (A1) and (A0) in Table 4-6 with (A2) and (A1), respectively.

4-43 The second sentence of the top paragraph should be changed to read as follows:

Two address-latch-enable signals, system address latch enable (SALE) and extended address latch enable (SXAL), are provided by the SIF.

4-68 Table 4-19. Replace the description for BIT 2, SSB__CLEAR, with the following:

SSB__CLEAR. This interrupt request is used by the system to acknowledge adapter-to-host interrupts and to notify the Adapter that the System Status Block (SSB) is available for posting additional status information, even if the SSB was not used for that particular interrupt (e.g., SCB__CLEAR interrupt).

4-68 Table 4-19. Under the description of BIT 8, remove the last sentence.

4-71 Section 4.4.2.3. Replace the third paragraph with the following:

Only the address range >0800 through >0FFF can be read through the data registers unless an Adapter Check interrupt occurs, in which case only the address range >0000 through >07FF can be read.

4-77 In section 4.4.6.1, remove sub-item b, SSB CLEAR (bit 2), from list item 2.

4-77 Replace the last paragraph on this page with the following:

If the SCB_REQUEST bit (bit 4) of the Adapter Interrupt Register is set to one, an SCB_CLEAR interrupt will also be posted when the SCB is available for additional commands. To acknowledge this interrupt, the attached system must set the INTERRUPT_ADAPTER and SSB_CLEAR bits in the Interrupt Register. In addition, the RESET_SYSTEM_INTERRUPT bit should be set to zero to clear the adapter-to-host hardware reset line. It is recommended that SCB_REQUEST be set coincident with EXECUTE if the SCB_CLEAR interrupt is desired.

4-83 Table 4-26. Under the description for BIT 1, the 110 seconds reference should be 10 seconds. The sentence should read:

This can be a result of parity errors in excess of the parity abort threshold set during initialization, bus errors in excess of the bus error abort threshold also set during initialization, or if the Adapter times out (10 seconds) waiting for the completion of DMA bus operation (with or without an error).

4-87 Table 4-28. The last two sentences in the description for BYTES 2-7 should be replaced with the following:

When using the TMS38020 Protocol Handler, bits 0,1 must be set to "01". When using the TMS38021 Protocol Handler, bit 0 must be set to zero. Bit 1 can be set to either zero or one.

4-88 Table 4-28. Under the description of BYTES 22-23, the fifth sentence should be replaced with the following:

The RAM start address must be on an eight-byte boundary minus two bytes (bits 13 and 14 are "11") and must be less than >8000; otherwise, an expansion RAM OPEN error will result.

4-88 Table 4-28. Under the description of BYTES 24-25, add the following sentence:

The value of this field must be even.

4-89 Add the following note to the bottom of the page:

Note:

Under heavy ring loading conditions, especially when the heavy traffic is broadcast address frames or frames addressed to the inserting adapter, the OPEN command will fail due to a ring poll failure during the insertion process. This failure will occur due to excessive receive loading on the inserting station. The OPEN command should be attempted again after a short delay. If the problem persists, the source of the receive traffic to the inserting adapter should be identified and stopped or removed from the ring before attempting another OPEN command.

4-92 Under *Buffer Allocation,* add the following paragraph:

To avoid the possibility of transmit congestion, causing transmit operations to suspend, it is highly recommended that a RECEIVE command and corresponding valid receive lists be issued as soon as possible following the OPEN command.

4-92 Under *Buffer Size*, change the second sentence to read as follows:

The default TRANSMIT MAXIMUM COUNT is six, allowing a transmit frame maximum information field size of 592 bytes, which includes a 32-byte frame header.

4-99 Table 4-34. Under the description of bit 0, change the last sentence to read:

The COMMAND COMPLETE and FRAME COMPLETE bits are not set at the same time.

4-100 After the seventh paragraph add the following:

When the last list in a chain contains an odd FORWARD POINTER, the adapter performs the following operations in order:

1. Updates the CSTAT field of the last start of frame list.
2. Posts the FRAME COMPLETE status if requested.
3. Rereads the FORWARD POINTER field of the list containing the odd FORWARD POINTER.
4. If FORWARD POINTER is still odd, the adapter posts a COMMAND COMPLETE status.

Because the adapter rereads the FORWARD POINTER after posting the FRAME COMPLETE status, the host software should not modify the FORWARD POINTER of the last list unless it is to add another transmit list to the chain. Therefore, this list containing the odd FORWARD POINTER should not be considered "free" until one of the following occurs:

- A COMMAND COMPLETE status is received for this list, or
- Any transmit status (i.e., FRAME COMPLETE, COMMAND COMPLETE, or LIST ERROR) occurs specifying a list further down the chain.

4-109 Section 4.4.7.5, CLOSE Command. The following sentence should be added to the first paragraph in this section:

After issuing the CLOSE command, the Adapter should be reinitialized before re-issuing the OPEN command.

4-119 Table 4-44. The value for capacitor C3 should be changed to 22,000 pF ± 10%. See Note 4 added to Figure 4-5 on page 2 of this update.

A-1 Add feature bullet as follows:

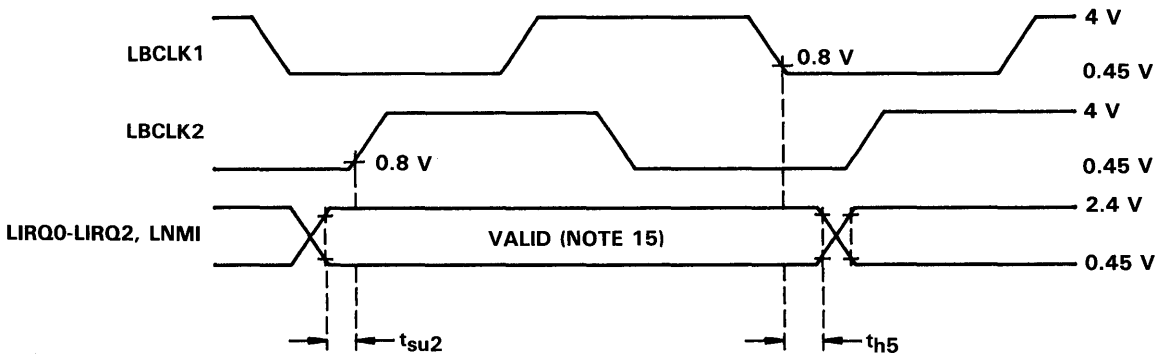
- Cost-Effective 48-Pin Plastic Dual-In-line Package

A-11 Under the table titled "recommended operating conditions", the reference to TEST0-TEST2 in the specifications for V_{IH} and V_{IL} should be removed. The TEST0-TEST2 pins now have the same V_{IH} and V_{IL} characteristics as all other inputs.

A-14 Add a Note 9A reference to specification for t_{d29}. Add the following note to the bottom of this page.

NOTE 9A. When the TMS38010 maintains bus mastership through the next bus cycle, the LR/$\overline{W}$ signal does not change state for 55 nanoseconds following LBCLK1 low.

A-20 The figure under "interrupt timing" should be replaced with the following new diagram:



A-20 Note 15 on this page should be replaced with the following:

NOTE 15. Inputs LIRQ0-LIRQ2 should not change state except during the window when LBCLK1 and LBCLK2 are both low. To meet this requirement, a latch, clocked by the falling edge of LBCLK1, should be added between the LIRQOUT0-LIRQOUT2 outputs of the TMS38030 and the LIRQ0-LIRQ2 inputs of the TMS38010. Parameter t_{h5} is to be met at the next falling edge of LBCLK1 following the rising edge of LBCLK2 in which t_{su2} was met.

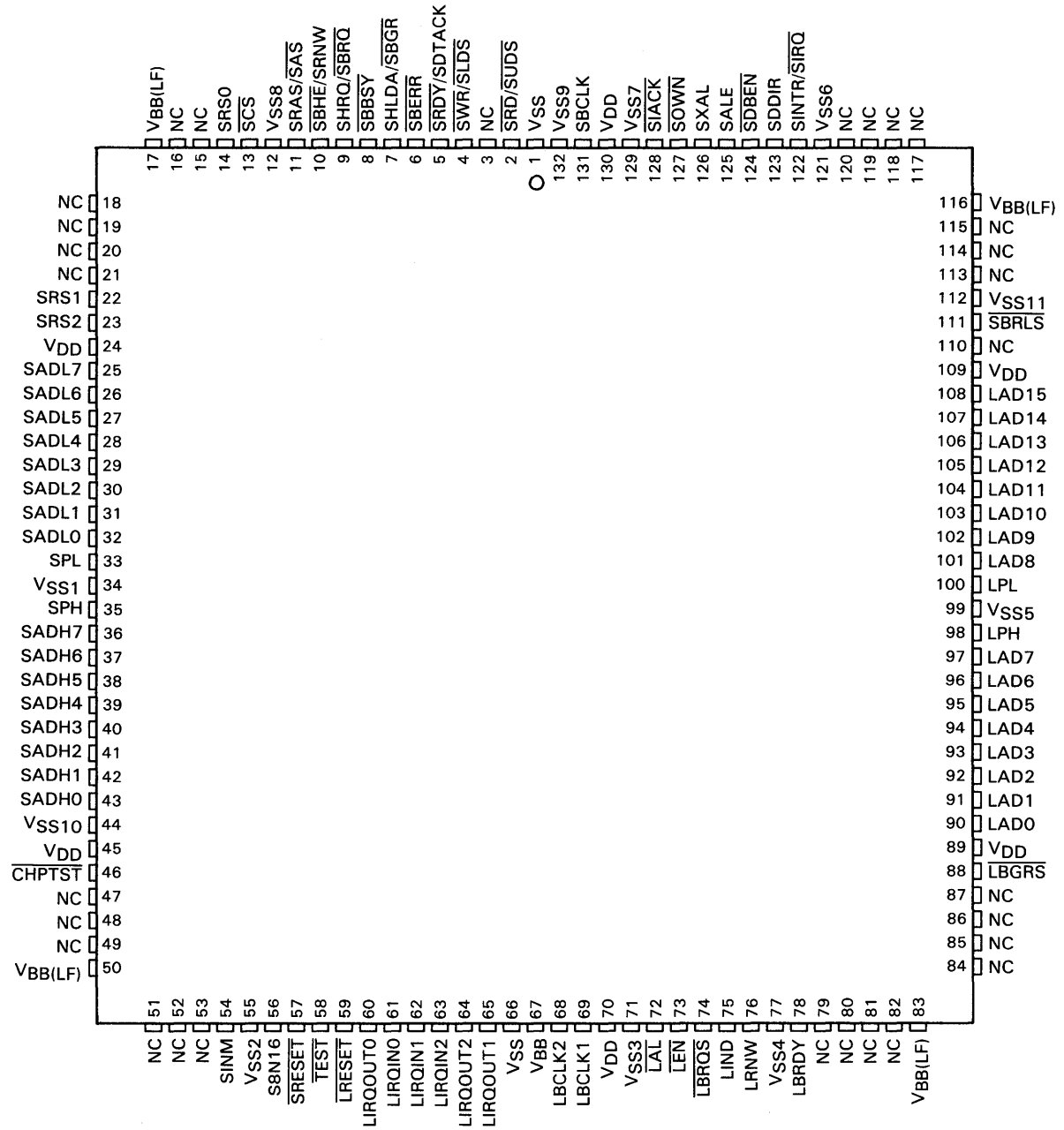
A-42 Add a Note 7A reference to specification for t_{d29}. Add the following note to the bottom of the page.

NOTE 7A. When the TMS38020 maintains bus mastership through the next bus cycle, the LR/$\overline{W}$ signal does not change state for 55 nanoseconds following LBCLK1 low.

A-53 Replace the seventh feature bullet with the following:

- 132-Pin Plastic Quad Flat Pack or 100-Pin Ceramic Pin Grid Array Package

Add the following pinout drawing:



Special Note: The user PC board design should include a connection from the V_{BB} pin (67) to one of the $V_{BB(LF)}$ pins (17, 50, 83, 116). This connection should be as short as possible. The $V_{BB(LF)}$ pins should be unconnected.

A-54 Add a dagger after "pin descriptions" and the following note at the bottom of the page:

†Pin numbers refer to the GB package only.

A-65 Add a Note 3A reference to the V_{IL} specification in the row labeled, "All other inputs". Add the following note to the bottom of the page:

NOTE 3A. $\overline{\text{SRESET}}$ is a hysteresis input and should be driven below 0.6 V during assertion to guarantee recognition.

A-67 I_{CC} supply current (V_{CC} = 5.5 V, T_A = 0°C) should be changed from 240 mA max to 260 mA max.

A-68 Add a Note 6A reference to specification for t_{d29}. Add the following note to the bottom of the page.

NOTE 6A. When the TMS38030 maintains bus mastership through the next bus cycle, the LR/$\overline{W}$ signal does not change state for 55 nanoseconds following LBCLK1 low.

A-74 Add the following sentence to Note 10:

The timing presented above is in reference to externally requested interrupts (those presented on LIRQIN0-LIRQIN2) only.

A-77 TMS38030-6 has been replaced by the TMS38030-8. Under the section titled "timing requirements over recommended supply voltage range and operating free-air temperature range", remove all references to the TMS38030-6.

A-101 Table 1. The value for capacitor C3 should be changed to 22,000 pF ± 10%. See Note 4 added to Figure 4-5 on page 9 in this update.

A-105 Under the section titled "energy detect", all references to C3 = 6800 pF should be changed to C3 = 22,000 pF.

A-108 Under the section titled "TTL input", remove the reference to FILTER under I_{IH}, I_{IL}, and I_I.

A-109 Under the section titled "transmitter", a note should be added to the "Output current, off" specifications as follows:

Output not under test is loaded with 75 Ω to V_{CC}.

A-110 Under the section titled "phantom driver", the test conditions under the I_{OH} specification should be changed such that NSRT = V_{IH}, and the parameter I_{OL} should be removed in its entirety.

A-111 Figure 5. The 240 Ω resistor should be changed to a 330 Ω resistor.

A-112 Under the section titled "energy detect", the test conditions under parameter V_{HYS} should be changed to $V_{HYS} = V_{IH} - V_{IL}$.

A-114 Note 19 should be replaced with the following:

Peak-to-peak voltage swing between EQUALA and EQUALB. RCVINA and RCVINB are unconnected.

A-114 Note 20 should be replaced with the following:

Peak-to-peak voltage swing between DROUTA and DROUTB. A differential between RCVINA and RCVINB is held to assure that noise on the receiver signal does not affect wrap mode.

A-114 Figure 8. The value 240 Ω assigned to the resistor should be changed to 330 Ω.

A-117 Figure 15 should be replaced with the following:

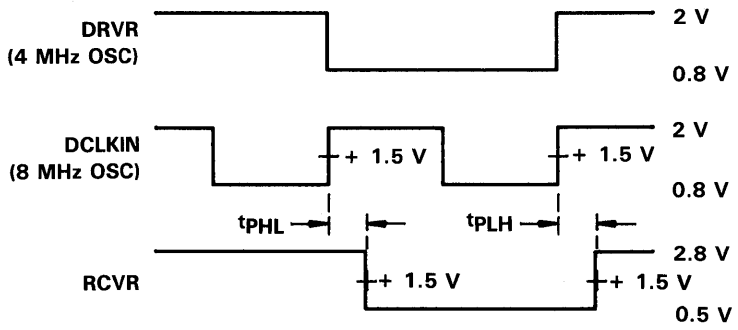
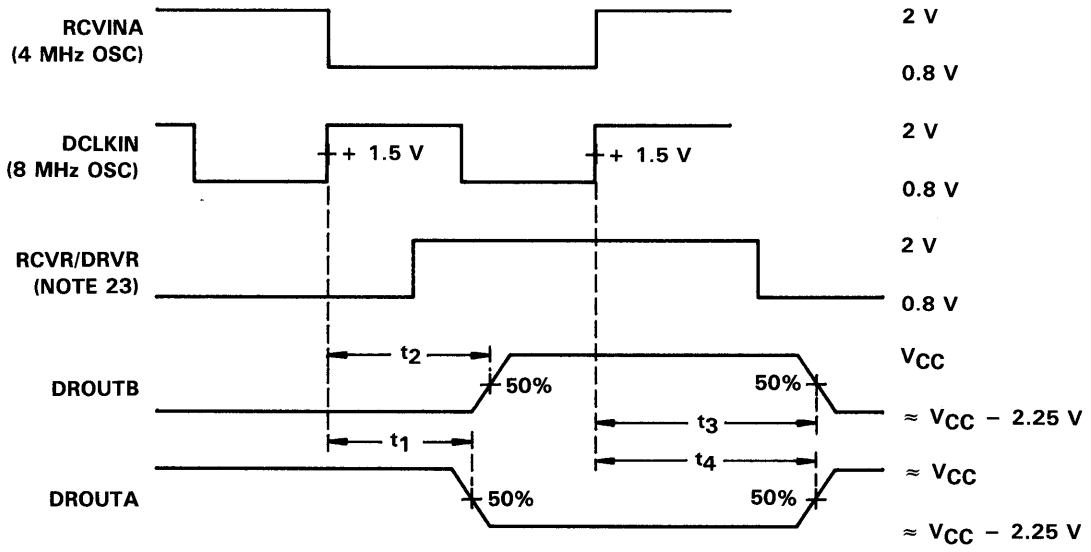


FIGURE 15. PROPAGATION DELAYS FROM DCLKIN TO RCVR WITH INTERNAL WRAP MODE

A-118 Figure 16 should be replaced with the following:



Note 23: For this test the RCVR output is tied directly to the DRVR input to test the asymmetry of the transmitter in a repeater configuration.

t_A	$\frac{t_1 + t_2}{2}$
t_B	$\frac{t_3 + t_4}{2}$

FIGURE 16. SKEW AND ASYMMETRY FROM DCLKIN TO DROUTA AND DROUTB

A-118 Figure 17 should be replaced with the following:

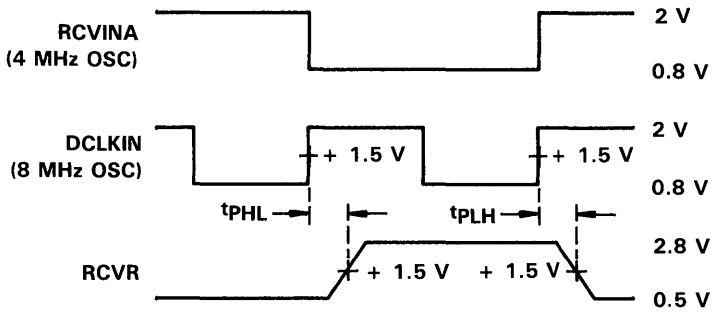


FIGURE 17. PROPAGATION DELAYS FROM DCLKIN TO RCVR

B-2 Under the Duplicate Address Test frame entry, include the following reference under column 2:

FC = >01

B-4 Under the Report New Monitor, Report SUA Change, and Report Ring Poll Failure frame entries, include the following under column 2:

FC = >01 for TMS38020 ROM code only. Otherwise FC = >00.

B-8 The paragraph under Section B.2.1 should be replaced with the following:

The burned-in address must conform to that shown in the figure below. Note that bit 0 must be set to zero. If the TMS38020 Protocol Handler is used, bit 1 must also be set to zero.

B-8 Replace Figure B-1 with the following:

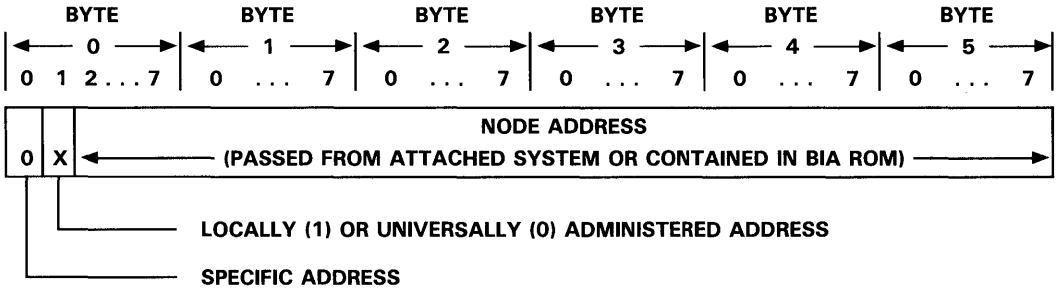
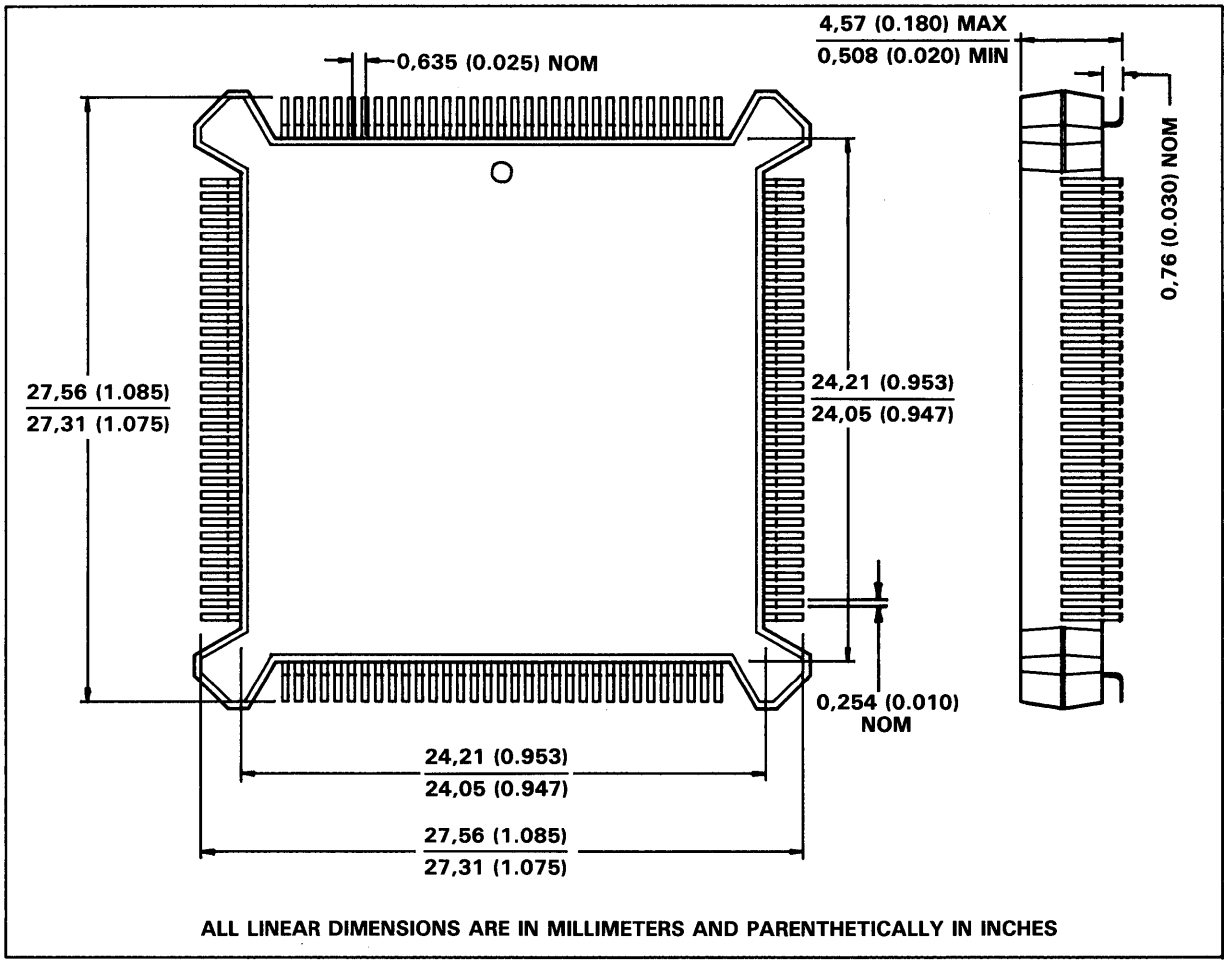


FIGURE B-1. BURNED-IN ADDRESS FORMAT

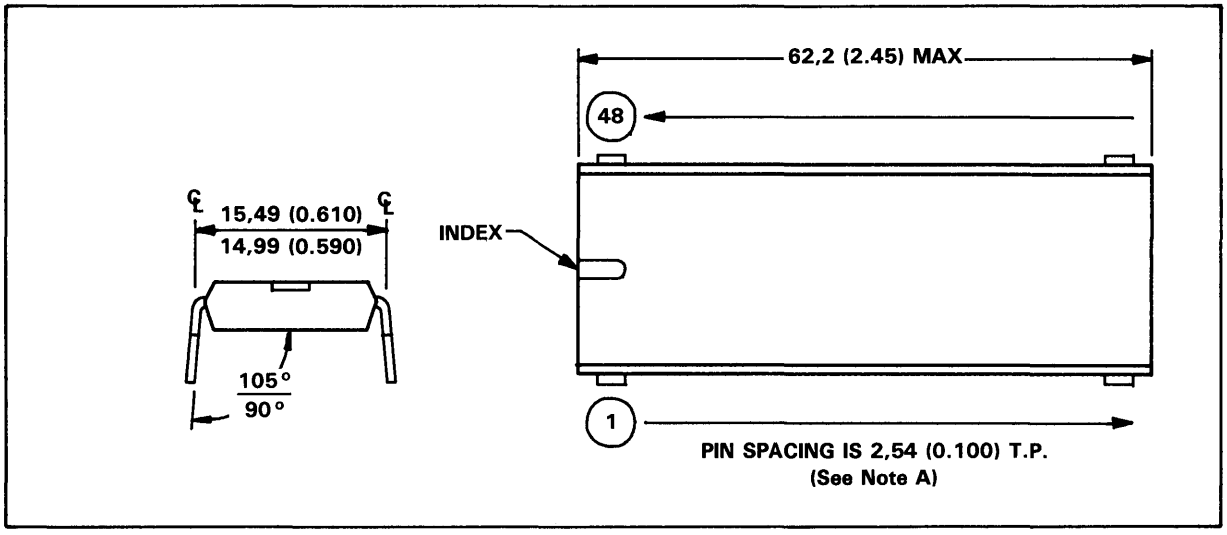
B-19 Section B.3.3.4. The bottom portion of the 100-pin GB pin-grid array drawing should be labeled "TOP VIEW".

B-19 Add the following mechanical drawings:

B.3.3.5 132-Pin Plastic Quad Flat Package (PQ Suffix)



B.3.3.6 48-Pin Dual-In-line Plastic Package (N suffix)



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

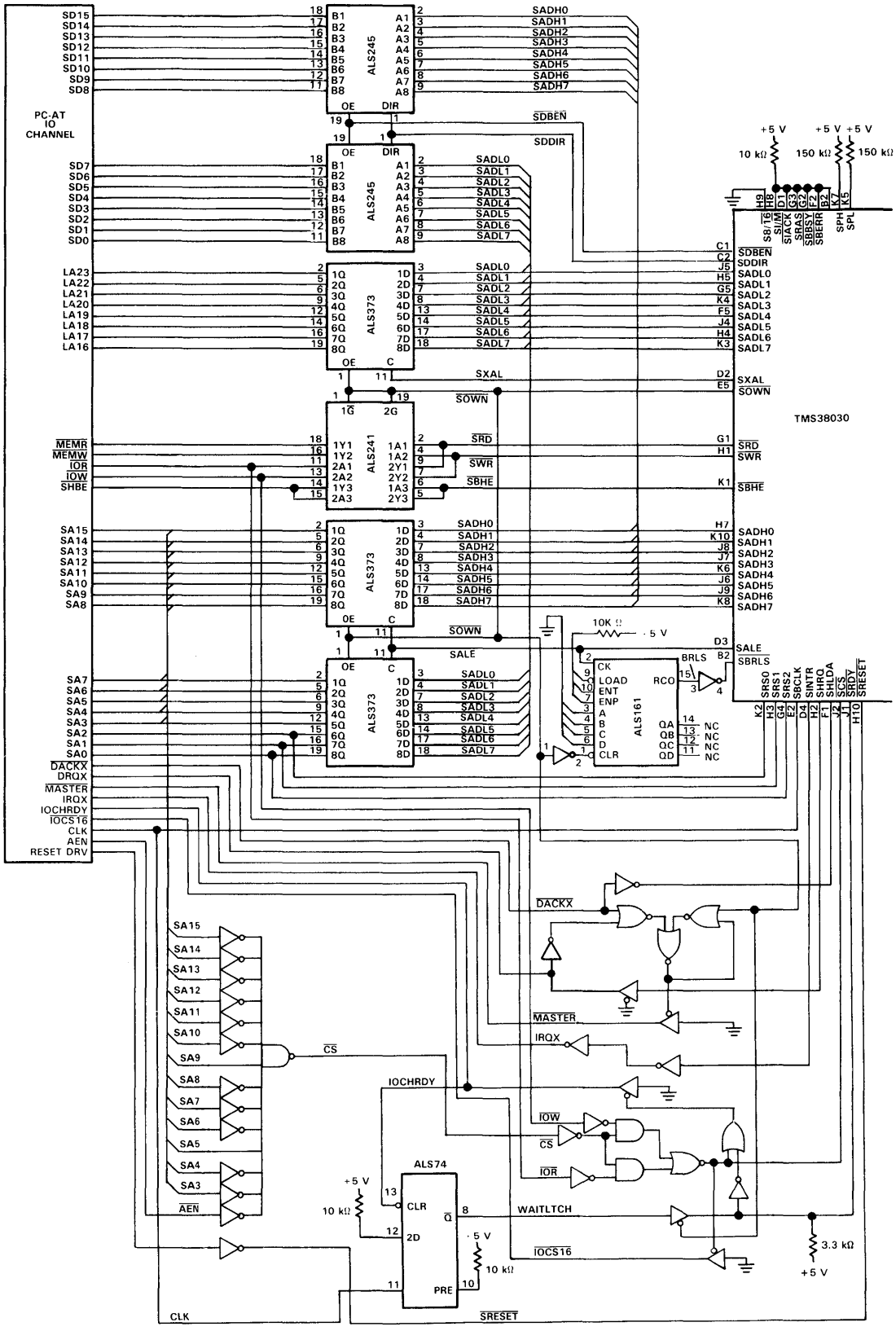
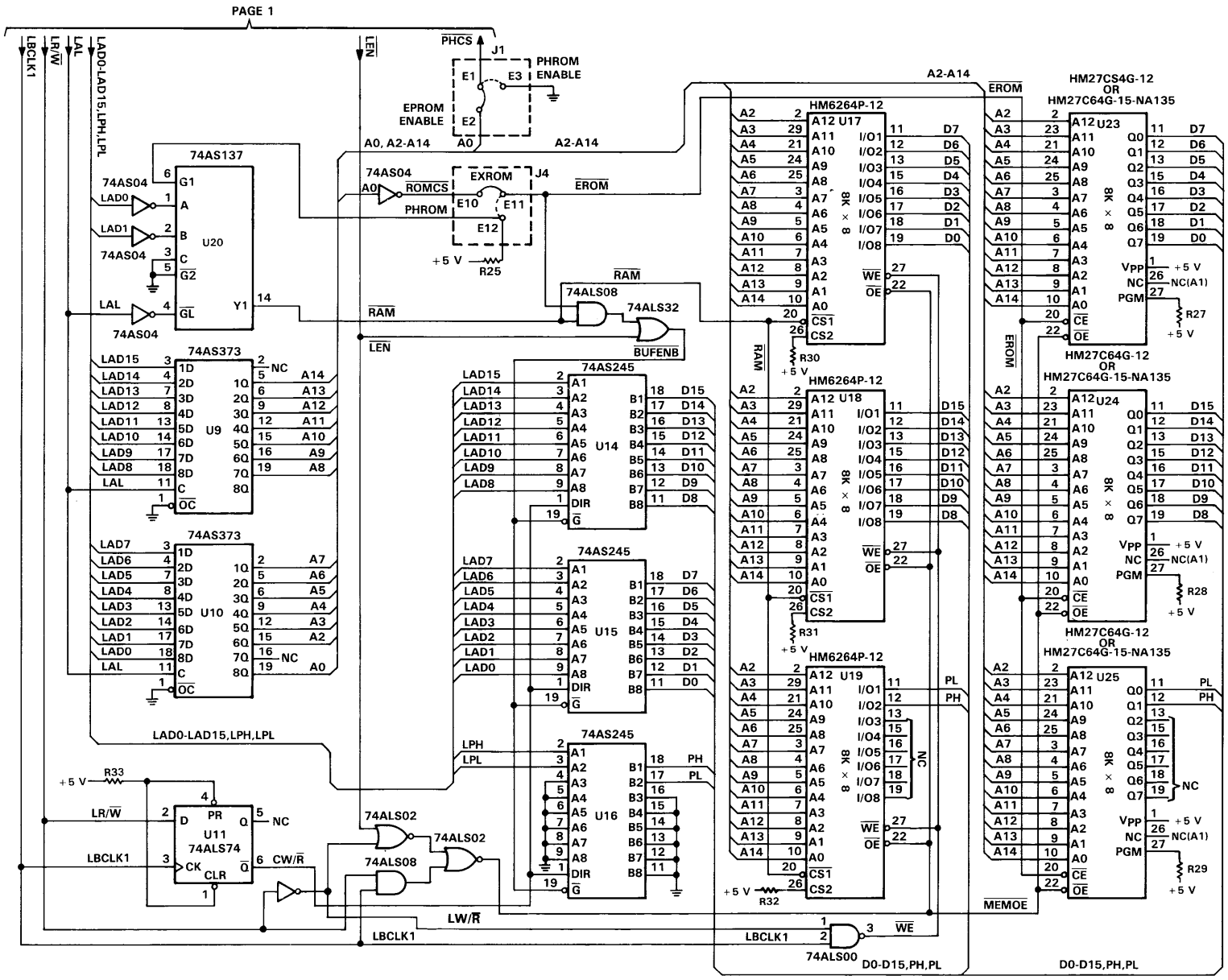


FIGURE 2-5. TMS380 INTERFACE TO IBM PC AT SYSTEM BUS



NOTE 4. For additional noise immunity, the value for C3 has been increased to 22,000 pF. For existing designs, the original 6,800 pF value may be used.

FIGURE 4-5. ADAPTER CHIPSET INTERCONNECT DIAGRAM (3 of 4)

Page	Change or Add
2-9	Change the last sentence in the first paragraph to read as follows: If a link station is in either a Checkpointing or Remote Busy state, then I-frame transmission is temporarily suspended.
2-29	The description for BIT 9, LLC_CTR_OVERFLOW, should be changed to read as follows: When set to one, indicates that one of the adapter's LLC error counters has reached half its maximum value.
2-73	The description for OPTIONS and BIT 0 should be changed to read: (reset) - If this bit is set to one, bytes 0-7 are reset to zero after this command is executed.
2-84	Table 2-29. Under the explanation for error code >28, remove the second line, which reads "An XID frame had too much data". Under the explanation for error code >41, remove the sentence which reads "this error code will be returned if an I-frame is issued before the DMA is ready," and place it under the explanation of error code >27.
2-86	After the second paragraph add the following: When the last list in a chain contains an odd FORWARD POINTER, the adapter performs the following operations in order: 1. Updates the CSTAT field of the last start of frame list. 2. Posts the FRAME COMPLETE status if requested. 3. Rereads the FORWARD POINTER field of the list containing the odd FORWARD POINTER. 4. If FORWARD POINTER is still odd, the adapter posts a COMMAND COMPLETE status. Because the adapter rereads the FORWARD POINTER after posting the FRAME COMPLETE status, the host software should not modify the FORWARD POINTER of the last list unless it is to add another transmit list to the chain. Therefore, this list containing the odd FORWARD POINTER should not be considered "free" until one of the following occurs: • A COMMAND COMPLETE status is received for this list, or • Any transmit status (i.e., FRAME COMPLETE, COMMAND COMPLETE, or LIST ERROR) occurs specifying a list further down the chain.
2-87	BIT 3. Remove the last sentence in this description.
2-87	BIT 4. Replace the description for BIT 4 with the following: (READY): Bit 4 will be used to indicate when a link station is ready to accept I-frames from the attached system. This bit will be set under either of two conditions. First, when a CONNECT.STATION command completes, the attached system should assume a not ready state, and wait for a READY transmit status interrupt. This interrupt will occur when the link station is ready for I-frame transmission, whether or not a TRANSMIT command has been issued. This interrupt may occur prior to receiving a command complete interrupt for the CONNECT.STATION command.

Second, after an I-frame has been DMA'ed into the adapter, and a CSTAT completion of >FE has been received, the link station is in a not ready state. When this condition clears, a READY transmit interrupt will be issued. If, after a >FE completion has been issued, another I-frame for that link station is passed to the adapter, the adapter will reject the I-frame with the error code >27, Link not Transmitting I-frames. Processing of the transmit lists will continue, and frames for other link stations will not be affected.

3-2 Figure 3-2 should be replaced with the new Figure 3-2 included on page 18 of this update.

4-3 The following paragraphs should be added after the last paragraph on this page.

The refresh of this DRAM is accomplished by a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle whenever the DRAM is not being accessed by any of the chipset bus masters. This occurs during Communications Processor internal processing cycles or whenever addresses below >1000 are accessed. Additionally, refresh occurs whenever sequential DRAM read or write cycles occur to each of the 256 DRAM row addresses. This occurs during normal DMA operations by the System Interface or Protocol Handler.

Analysis of the Communications Processor software characteristics and Protocol Handler and System Interface DMA loading characteristics guarantees that DRAM refresh timing is not violated.

4-4 Figure 4-4 should be replaced with the new Figure 4-4 included on page 19 of this update.

4-5 The top portion of Section 4.3 should be replaced in its entirety with the following:

The download of DLC Software is performed by:

1. Placing the adapter into download state.
2. Downloading and executing the Enable Memory (ENM) software.
3. Setting the PHDIS to one.
4. Downloading the DLC Software object code via direct I/O (DIO) operations.

The special download state of the adapter is entered via the following procedure:

1. Perform a hardware reset ($\overline{\text{SRESET}}$ driven low).
2. Verify normal completion of bring-up diagnostics (>0040 read in the Interrupt Register).
3. DIO write the data pattern >AA55 from location >0800 through >0FFE via the Address Register and Data Register with Autoincrement.
4. Apply a second hardware reset.
5. Write the value >8000 to the TMS38030 Interrupt Register immediately following reset but no later than 1.6 ms following the reset.

Following the write of >8000 to the Interrupt Register and a delay of 10 milliseconds, the Interrupt Register should be read. If the Interrupt Register is equal to zero, then the adapter is in the download state. The memory locations from >0800 through >0FFE should be cleared to zero.

After successfully entering the download state and clearing the RAM, the object file may be loaded into the adapter RAM. Before this procedure is discussed, the following provides a description of the format of the object file in which DLC Software and ENM Software is provided.

4-6 Section 4.3.2. Add the following sentences to the description of the WRITE Command (>E6):

This command takes nine microseconds to execute. No other command should be issued prior to this time.

4-6 Section 4.3.2. Add the following sentence to the description of the STEP Command (>FF):

This command takes seven microseconds to execute.

4-6 Section 4.3.2. Add the following sentence to the description of the EXECUTE Command (>C5):

This command takes 12 microseconds to get to the first instruction of the target code.

5-13 Under Section 5.2.5.1, the reference to the fail code of >7X should be deleted. The last paragraph should be deleted and replaced with the following:

No failure code is presented with the DMA tests. The source and destination data patterns must be compared to verify good completion of the DMA operation.

5-15 Under Section 5.2.6.1, the reference to the fail code of >7X should be deleted. The last paragraph should be deleted and replaced with the following:

No failure code is presented with the DMA tests. The source and destination data patterns must be compared to verify good completion of the DMA operation.

7-1 The Bridge Options Software, referenced throughout Section 7, has been replaced by the DLC Software. All functions contained in the Bridge Options Software are also contained in the DLC Software. For information on the DLC Software refer to Section 2.

7-4 Under the description for the Broadcast Bits, the definitions for bit codes "110" and "111" should be reversed.

7-14 The last paragraph on this page should be replaced with the following:

The bridge options are included in the DLC software.

7-15 The first paragraph on this page should be deleted in its entirety.

7-21 Replace the 41st equation with the following:

```
COMB2 = !(!A12 & A1314 & !GRPDLY & SAVE12 & STAT
        # A12 & A1314 & !GRPDLY & !SAVE12 & STAT);
```

A-3 Change the second to the last feature bullet to read:

- 48-Pin, 600-Mil, Plastic or Ceramic Dual-In-line Packaging

Change the package description above the pinout to read:

"N OR JD PACKAGE"

A-22 The units for I_{CC} supply current should be changed from μA to mA.

A-24 Add a Note 7A reference to specification for t_{d29}. Add the following note to the bottom of this page.

NOTE 7A: When the TMS38021 maintains bus mastership through the next bus cycle, the LR/$\overline{W}$ signal does not change state for 55 nanoseconds following LBCLK1 low.

A-37 The manual updates listed in the appendix are also included in this update.

B-3 Replace Figure B-2 with the new Figure B-2 on page 20 of this update.

C-1 Appendix C should be replaced in its entirety by the new download program included on pages 21 through 25 of this update.

D-2 Add the following information to Appendix D:

NOTE: For Developers of PC Adapters:

In TI's testing of the LLC software, we have discovered the following hardware dependency in IBM's APPC/PC program and IBM's 3270 Emulation Program.

These software programs read a register at I/O location h'A20' (primary adapter) and/or h'A24' (secondary adapter) to determine the interrupt level that the card is using. On the IBM card, the interrupt level is encoded in the two least significant bits of this register, as follows:

00 interrupt level 2
01 interrupt level 3
10 interrupt level 6
11 interrupt level 7

This register is described in Section 6 of the IBM Token-Ring PC Adapter Technical Reference. To avoid confusion, though, please note that if a switch is "on," the corresponding bit in the register will be 0. If a switch is "off," the bit will be 1.

These two software programs violate the IBM software interface to read these registers on the hardware. If the programs read bad data from the locations (either because there is nothing there, or because what is there is not what is expected), their operation will be unreliable. Designers should consider adding hardware to boards at these locations.

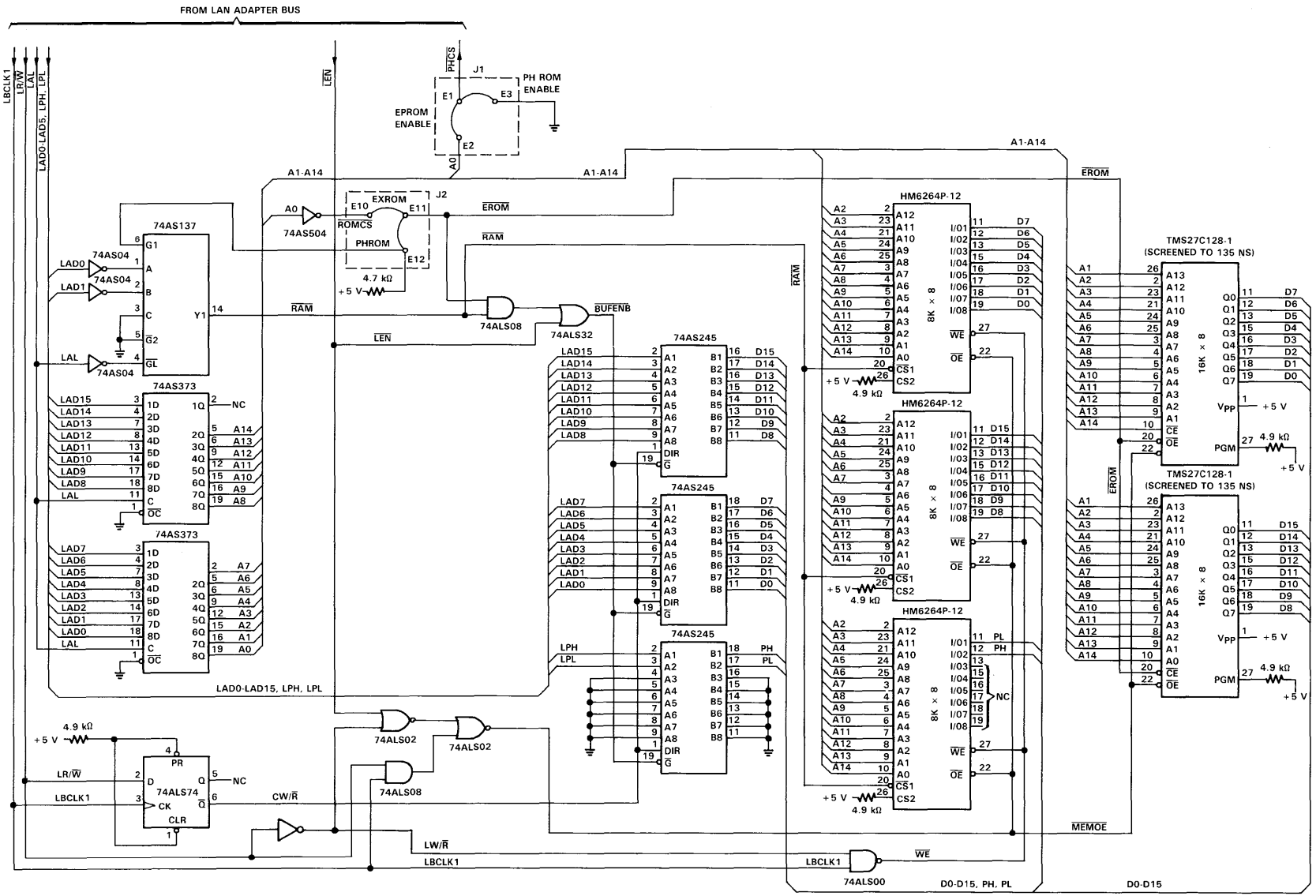
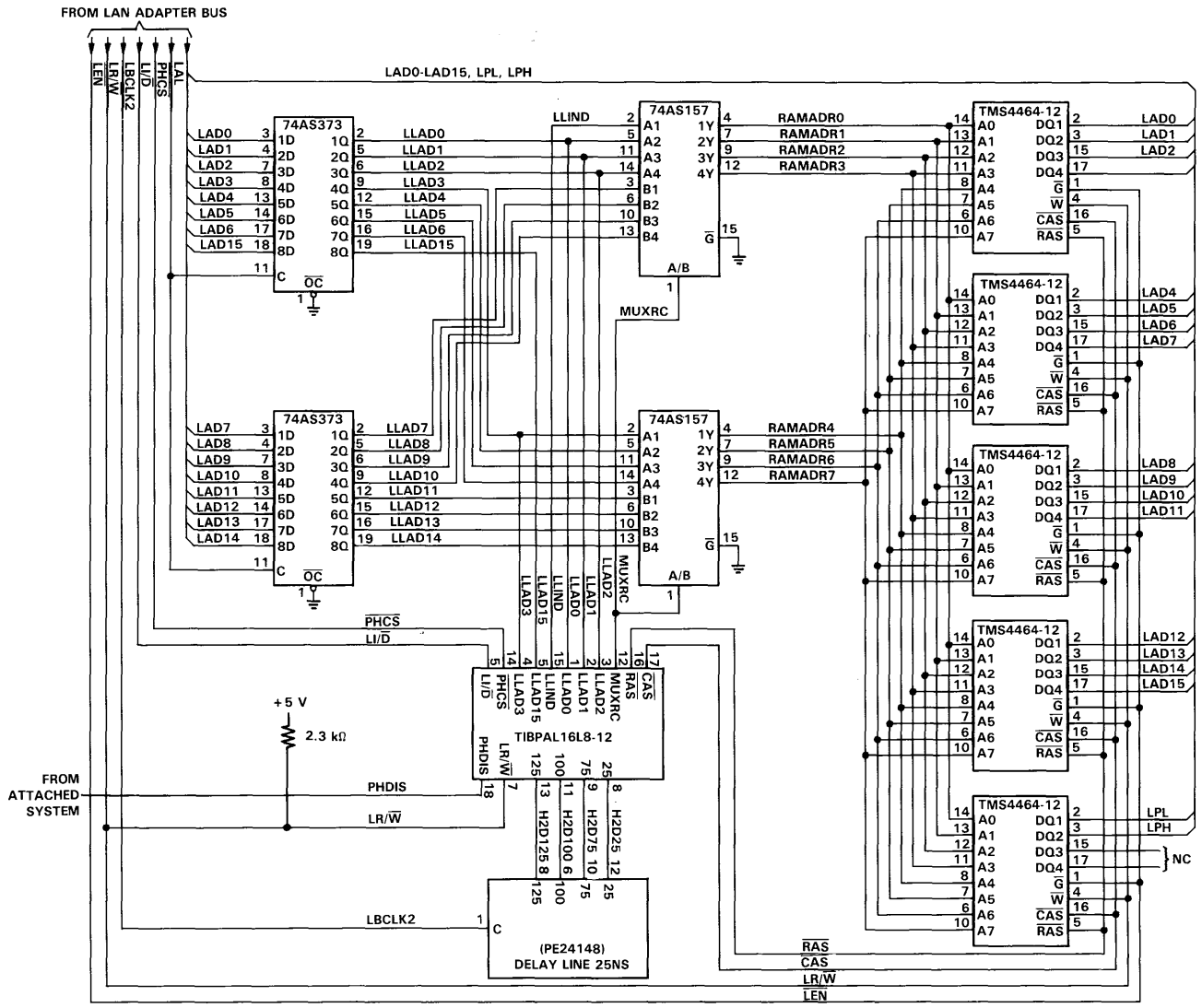


FIGURE 3-2. EPROM-Based Adapter Bus Schematic



REDUCED EQUATIONS FOR PAL

PHCS = !(LLAD0 & LLAD1 & !PHDIS + !LLAD0 & !LLAD1 & !LLAD2 & !LLAD3)

RAS = !(PHDIS & H2D75 & LLAD1 + H2D75 & !LLAD0 & LLAD1 + H2D75 & !LLAD1 & LLAD2 + H2D75 & !LLAD1 & LLAD3 + H2D125)

CAS = !(H2D125 & LLAD0 & LLAD1 & !PHDIS + H2D125 & LR/W + H2D75 & LLAD0 & LLAD1 & !PHDIS + H2D125 & !LLAD0 & !LLAD1 & !LLAD2 & !LLAD3 + H2D125 & !H2D25 + H2D75 & !LLAD0 & !LLAD1 & !LLAD2 & !LLAD3)

MUXRC = !(H2D100 + H2D125)

LLIND = !(LI/D & LLAD15)

NOTE: ! = Inverse

NOTE: PHDIS signal is controlled by host software to disable PHROM and enable DRAM from >C000 to >FFFE.

FIGURE 4-4. DRAM Schematic

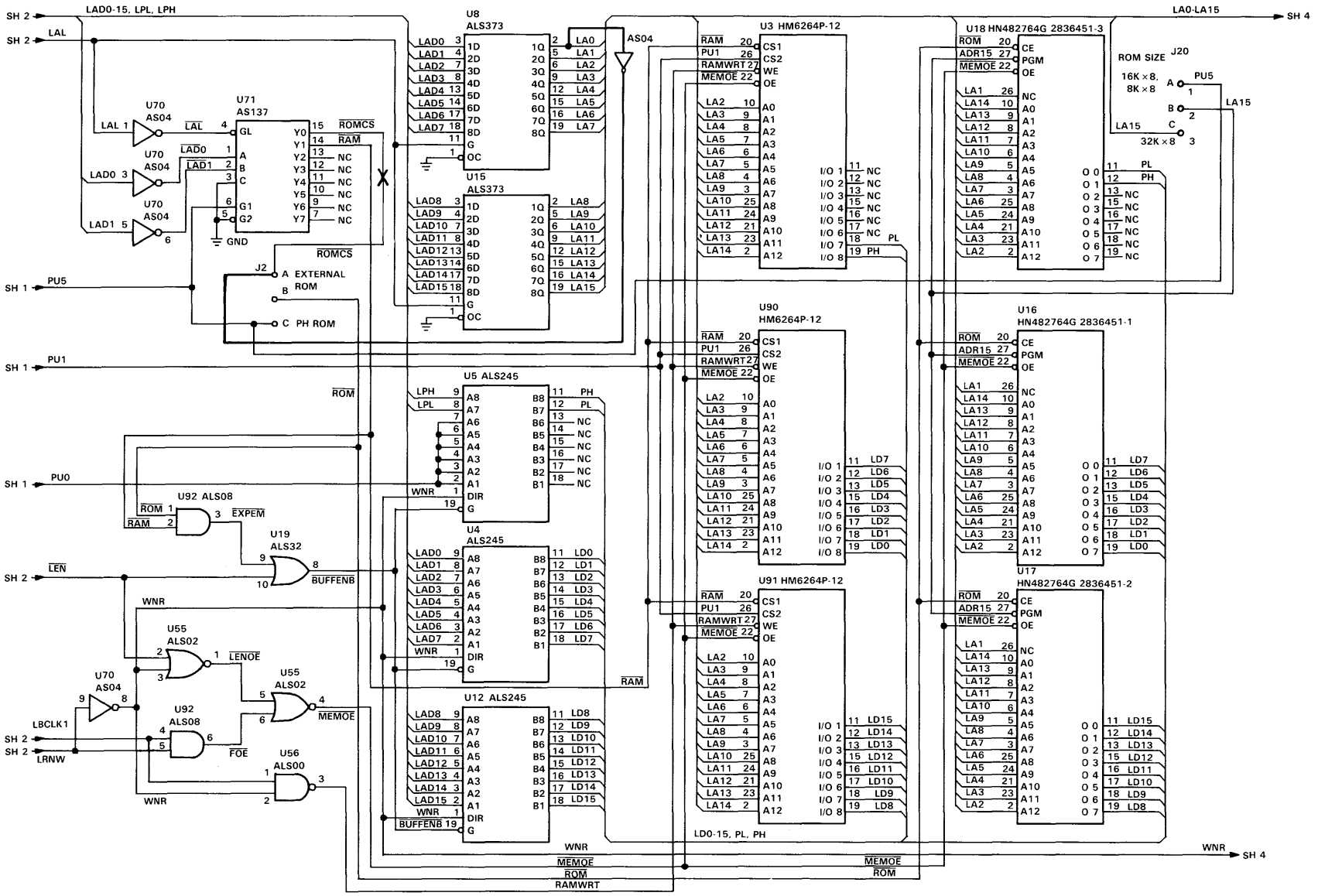


FIGURE B-2. PC Family Card Logic with Modifications

```
/*****************************************************/
/*              DOWNLOAD  PROGRAM                    */
/*                                                   */
/* This DOWNLOAD routine takes as input a TI tagged  */
/*  object file.  It places the adapter in the       */
/*  download state, and downloads the input software */
/*  into the adapter for execution.                  */
/*                                                   */
/* The adapter is assumed to be at locations >xx20   */
/*  thru >xx29 in PC I/O space, where >xx is set by  */
/*  the user on initiation of the software.          */
/*                                                   */
/* The DOWNLOAD routine assumes that the adapter     */
/*  software's starting point is at address >0600 on */
/*  the adapter bus.  >0600 is the starting address  */
/*  for both the Adapter Debug Software (ADS) B205,  */
/*  and the DLC software (OSI2).                     */
/*                                                   */
/* This listing is for illustration only.            */
/*                                                   */
/* Revision History:                                 */
/*   Initial release: 03/15/87                       */
/*   Modified for new memory map: 5/29/87            */
/*   Modified for PH disable    :11/03/87            */
/*   Modified for new download  :11/12/87            */
/*****************************************************/

#include        <stdio.h>
#include        <conio.h>
#include        <process.h>

#define CLS             printf("\033[2J")
#define DATA_LO         0x00+base_addr
#define DATA_HI         0x01+base_addr
#define DATAINC_LO      0x02+base_addr
#define DATAINC_HI      0x03+base_addr
#define ADDRESS_LO      0x04+base_addr
#define ADDRESS_HI      0x05+base_addr
#define INTERRUPT_LO    0x06+base_addr
#define INTERRUPT_HI    0x07+base_addr
#define CONBUF          0x09+base_addr
#define CONBUF2         0x0F+base_addr
#define PHDISABLE       0x40    /* PHDIS AND HW_INT_ENABLE */
#define HW_RESET        0x04
#define HW_RESET2       0x00
#define HW_INT_ENABLE   0x20    /*  enable interrupts from adapter */
#define DELAY           25      /*  500 usec delay loop constant   */
#define FD_STEP         0xFF    /*  Freezedump commands            */
#define FD_WRITE        0xE6
#define FD_EXECUTE      0xC5
#define CODE_START_LO   0x00    /*  Code entry point for ADS B205  */
#define CODE_START_HI   0x06    /*   or OSI2, DLC softare          */
#define ENMS_START_LO   0x00    /*  Code entry point for PHCS      */
#define ENMS_START_HI   0x0A    /*   disable and freeze dump code  */
#define ENM_DONE        0x70    /*  ENM code finished flag        */
#define YES             1
#define NO              0

unsigned int lineptr,adp_ad,linenum,try,temp,endflag,
             address,stepcnt,base_addr,done,ENMFILE;
char inline[90],yesno;
int numsteps;
```

```
main()
   {
   char blk_en;
   int temp;
   FILE  *OSI2;
   FILE  *ENM;

   try=1;
   ENMFILE = YES;
   CLS;
   base_addr=0x0A20;

   if (( OSI2 = fopen("OSI2.OBJ", "r")) == NULL)
      {
      printf("FILE OSI2 NOT FOUND. ");
      exit(1);
      }

   if ((ENM = fopen("ENM.OBJ", "r")) == NULL)
      {
      printf("FILE ENM NOT FOUND. ");
      printf("  DO YOU WISH TO CONTINUE? (Y/N):");
      gets(inline);
      sscanf(inline, "%c" ,&yesno);
      if((yesno == 'N') || (yesno == 'n'))
        exit(1);
       else
         ENMFILE=NO;
     }

/* Put the adapter in Freeze-Dump Mode  */

start:
   blk_en = inp(CONBUF) & 0x08;
   outp(CONBUF, HW_RESET);
   outp(CONBUF, HW_RESET2);
   try = 0;
   while ((temp = inp(INTERRUPT_LO)) != 0x40) {
      try++;
      if (try == 10) {
        printf("DOWNLOAD ABORTED\nPLEASE RESET THE ADAPTER\n");
        exit(1);
        }
      printf("\nRESET FAILED - INTERRUPT_LO = %x",temp);
      for(temp=10000;temp;temp--);
      }
   outp(ADDRESS_LO, 0x00);
   outp(ADDRESS_HI, 0x08);
   for (temp = 0x400; temp; temp--)  {
      outp(DATAINC_LO, 0x55);
      outp(DATAINC_HI, 0xAA);
      }
   outp(CONBUF, HW_RESET);
   outp(CONBUF, HW_RESET2);
   outp(CONBUF, (blk_en | HW_INT_ENABLE));
   outp(INTERRUPT_LO, 0x00);
   outp(INTERRUPT_HI, 0x80);

   for (temp = DELAY; temp; temp--) ;
   for (temp = DELAY; temp; temp--) ;
   for (temp = DELAY; temp; temp--) ;

   try = 0;
```

```
   if (inp(INTERRUPT_LO) || inp(INTERRUPT_HI))  {
      try++;
      outp(ADDRESS_LO, 0x00);
      outp(ADDRESS_HI, 0x08);
      for (temp = 0x400; temp; temp--) {
         outp(DATAINC_LO, 0x00);
         outp(DATAINC_HI, 0x00);
         }
      if(try < 5) {
        printf("\nDOWNLOAD MODE NOT ENTERED - RETRYING\n");
        goto start;
        }
       else {
        printf("DOWNLOAD ABORTED\nPLEASE RESET THE ADAPTER\n");
        exit(1);
        }
      }
   /* Clear RAM from 0x800 to 0xFFE   */
   outp(ADDRESS_LO, 0x00);
   outp(ADDRESS_HI, 0x08);
   for (temp = 0x400; temp; temp--) {
      outp(DATAINC_LO, 0x00);
      outp(DATAINC_HI, 0x00);
      }
   /* Write the starting address for the adapter into adapter  */
   /*  address >0000.                                          */

   outp(INTERRUPT_HI, FD_WRITE);    /* enable DIO writes      */

   if (ENMFILE == YES) {
      outp(DATA_LO,ENMS_START_LO);     /* write starting address */
      outp(DATA_HI,ENMS_START_HI);
      downcode(ENM);
      done=NO;
      while(done==NO) {
        if ((inp(INTERRUPT_LO) == ENM_DONE) && (inp(INTERRUPT_HI) == 0))
         done = YES;
        }
      outp(CONBUF2,PHDISABLE);
    }

   outp(ADDRESS_LO,0);              /* clear out SIF ADDRESS register */
   outp(ADDRESS_HI,0);
   outp(DATA_LO,CODE_START_LO);     /* write starting address */
   outp(DATA_HI,CODE_START_HI);
   downcode(OSI2);
   printf("ADAPTER IS EXECUTING LLC - CHECK FOR BUD CODE COMPLETION\n");
   exit(0);

}
downcode(OBJCODE)

 FILE  *OBJCODE;

 {

   /* Read input file and download the software    */

   adp_ad = 0;
   linenum = 0;
   while (fgets(inline, 90, OBJCODE) != NULL)  {
      linenum++;
      endflag = 0;
```

```
if (linenum == 1)  {
   if (!sscanf(inline, "%*13c9%4x", &adp_ad))  {
      printf("Illegal header in file.  Download aborted");
      exit(1);
      }
    else
      lineptr = 18;
   printf("\nDOWNLOADING.");
   }
else
   lineptr = 0;

if (inline[0] == ':')  {
   printf("\n END OF FILE REACHED");
   outp(INTERRUPT_HI,FD_EXECUTE);
   return;
   }

else {

  while (lineptr < 90 && !endflag)
    switch (inline[lineptr])
     {
     case '9':
        {
        sscanf(&inline[lineptr], "9%4x", &adp_ad);
        printf(".");
        lineptr += 5;
        break;
        }
     case 'B':
        {
        sscanf(&inline[lineptr], "B%4x", &temp);
        address = (inp(ADDRESS_HI) << 8) | inp(ADDRESS_LO);
        if (address != adp_ad)  {
          outp(ADDRESS_LO, adp_ad & 0xff);
          outp(ADDRESS_HI, adp_ad >> 8);
          numsteps = (adp_ad >> 11) - (address >> 11);
          if (numsteps < 0)
             numsteps += 32;
          for (stepcnt = 0; stepcnt < numsteps; stepcnt++)
            outp(INTERRUPT_HI, FD_STEP);
          }

        outp(DATAINC_LO, temp & 0xff);
        outp(DATAINC_HI, temp >> 8);
        lineptr += 5;
        adp_ad += 2;
        break;
        }
     case 'F':
        {
        endflag = 1;
        break;
        }
     default:
        {
        printf("\nILLEGAL TAG CHARACTER");
        printf("'%c' in line %u: ",
                inline[lineptr], lineptr);
        exit(1);
        }
```

```
        }         /* end of switch     */
      }           /* end of else       */

    if (!endflag)  {
      printf("\nILLEGAL FORMAT ON LINE %u", lineptr);
      exit(1);
      }

    }     /* end of while loop */

printf("\n FILE ERROR AT LINE %u: ", linenum);
exit(1);
}
```

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(714) 458-5395; Schweber (818) 999-4702;
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