TEXAS INSTRUMENTS

TMS320 Family Development Support

Reference Guide

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1989

1989 Digital Signal Processing Products

TMS320 Family Development Support Reference Guide

TEXAS INSTRUMENTS

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Section 1

Introduction

Texas Instruments, long recognized as a market leader in the area of digital electronics, continues to strengthen it's position with the expansion of the TMS320 family of Digital Signal Processors.

The TMS32010, the first digital signal processor in the TMS320 family, was introduced in 1983. During that year, the TMS32010 was named "Product Of The Year" by the magazine, Electronic Products. Since that time, the TMS320 family has expanded to include three generations of programmable DSPs (see Figure 1-1). The TMS320C14 (a first generation spinoff) was introduced in 1988. That same year, the TMS320C14 was named "Product Of The Year" and "The Best of 1988" by the magazines Electronic Products and Electronic Design respectively. The TMS320C30 realtime operating system, SPOX, was also named "The Best of 1988" by Electronic Design.

The powerful instruction sets, inherent flexibility, high-speed number crunching capabilities, and innovative architectures have made this high performance and cost effective processor family the ideal solution to many telecommunications, computer, commercial, industrial, and military applications.

Texas Instruments has demonstrated an unsurpassed dedication to the advancement of digital signal processing (DSP) and it's applications through extensive development support and expansion of the TMS320 family. The members of the three generations include:

- First-Generation Devices:
  - TMS32010, the first 20-MHz digital signal processor
  - TMS320C10, a CMOS 20-MHz version of the TMS32010
  - TMS320C10-14, a 14-MHz version of the TMS320C10
  - TMS320C10-25, a 25-MHz version of the TMS320C10
  - TMS320C14, a TMS320C15 with the on-chip peripherals of a microcontroller
  - TMS320E14, an EPROM version of the TMS320C14
  - TMS320C15, a TMS320C10 with expanded ROM and RAM
  - TMS320E15, an EPROM version of the TMS320C15
  - TMS320C15-25, a 25-MHz version of the TMS320C15
  - TMS320E15-25, an EPROM version of the TMS320C15-25
  - TMS320C17, a TMS320C15 with serial interface
  - TMS320E17, an EPROM version of the TMS320C17

- Second-Generation Devices:
  - TMS32020, a NMOS 20-MHz device capable of twice the performance of the first-generation devices
  - TMS320C25, a 40-MHz CMOS version of the TMS32020 with twice the performance of the TMS32020.
  - TMS320C25-50, a 50-MHz version of the TMS320C25

- TMS320E25, an EPROM version of the TMS320C25

- Third-Generation Devices:
  - TMS320C30, a high-performance CMOS 32-bit floating point device capable of executing up to 33 MFLOPS (millions of floating-point operations per second)

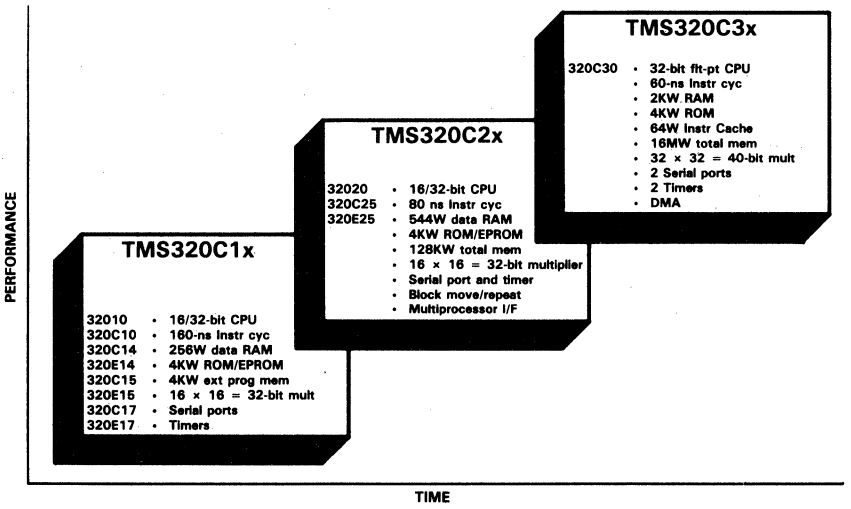

Figure 1-1. TMS320 Device Evolution

Plans for expansion of the TMS320 family include more spinoffs of the existing generations as well as more powerful future generations of digital signal processors.

The TMS320 family combines the high performance and specialized features necessary in DSP applications with an extensive program of development support, including hardware and software development products, product documentation, textbooks, newsletters, DSP design workshops, and a variety of application reports. Figure 1-2 shows the wide range of development tools available.

Figure 1-2. TMS320 Family Development Support

1.1 How to Use This Manual

The TMS320 Family Development Support Reference Guide details the vast development support available for the TMS320 family of digital signal processors. Information concerning all aspects is consolidated into this document making it an effective reference guide to assist the user in selecting the necessary tools for design and development of TMS320 applications. Note that TMS320 refers to all of the first, second, and third generations of DSP devices.

Sections 1 and 2 provide an overview of the TMS320 family and its capabilities for the user unfamiliar with digital signal processing and investigating it for the first time. Sections 3, 4, and 5 describe the software and hardware development products available to support each phase of DSP design. These sections also provide information that can assist in selecting which product(s) to use. Section 6 describes the seminar and workshops that provide hands-on experience using the development tools. Section 7 describes the extensive documentation available to support the wide range of applications using the TMS320 family. Section 8 gives information regarding the TI University Program. Section 9 describes various products manufactured by TI third parties, plus a list of DSP consultants.

The six appendices cover various areas of interest. Appendix A describes TI device packaging information and product part numbers. Appendix B covers TI policies and procedures for repair or exchange of a damaged system. Appendix C describes the TI program license agreement. Appendix D is a discussion of ROM code options. Appendix E gives TI criteria for evaluating product quality and reliability. Appendix F describes how to program the TMS320 EPROM cell.

Section 2. The TMS320 Digital Signal Processor Family. Description, key features, and block diagram of TMS320 family members. Lists of possible applications.

Section 3. TMS320 Development and Support Products. Discussion of TMS320 software and hardware development flow.

Section 4. Software Development and Support Products. Information on software development and the following products:

- TMS320 Macro Assembler/Linker
- TMS320 C-compiler
- TMS320 Simulator
- SoftWare Development System (SWDS)
- Digital Filter Design Package (DFDP)
- Digital Signal Processing Software Library
- TMS320 Bell 212A Modem Software.
- Data Encryption Standard Software
- SPOX: TMS320C3x DSP Operating System

Section 5. Hardware Development Tools. Information on hardware development and the following tools:

- TMS320 Evaluation Module (EVM)
- TMS320 Emulator (XDS)
- TMS320 XDS Upgrade Program
- TMS320 Analog Interface Board (AIB)

Section 6. RTC TMS320 Seminar and Workshops. Description of the three-day workshops offered by the TI Regional Technology Centers (RTC). Address list of the worldwide RTCs.

Section 7. TMS320 Documentation Support. Discussion of TMS320 documentation available, including data sheets, user's guides, application reports, textbooks, technical articles, newsletters, bulletin board, and hotline.

Section 8. TMS320 University Program. Information about the TMS320 hardware and software products offered at a discount to universities. List of textbooks written by university professors on DSP theories and applications using the TMS320 devices. Recommendations on establishing DSP lab workstations and research stations in universities.

Section 9. TMS320 Third-Party Support. Description of products manufactured by other companies, which can assist in TMS320 development. Address list of third parties. List of digital signal processing consultants.

Appendix A. TMS320 Product Order Information. Device packaging information and product part numbers. Explanation of TMS320 device and development support prefixes and nomenclature.

Appendix B. Texas Instruments Factory Repair and Exchange Policy. Outline of policies and procedures for repairing or exchanging a damaged system.

Appendix C. Texas Instruments Program License Agreement.

Appendix D. ROM Codes. Discussion of ROM codes and the procedure for implementation.

Appendix E. Quality and Reliability. Discussion of Texas Instruments quality and reliability criteria for evaluating performance.

Apppendix F. Programming The TMS320 EPROM Cell. Procedure for programming the TMS320 EPROM cell.

Section 2

The TMS320 Digital Signal Processor Family

The TMS320 family of 16/32-bit single-chip digital signal processors combines the flexibility of a high-speed controller with the numerical capability of an array processor, offering an inexpensive alternative to custom VLSI and multichip bit-slice processors.

The combination of the TMS320's internal busing and its specialized digital signal processing (DSP) instruction set provide speed and flexibility to produce a MOS microprocessor family capable of executing up to 33 MFLOPS (million floating-point operations per second). The TMS320 family optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides the design engineer with power previously unavailable on a single chip.

The TMS320 family consists of three generations of digital signal processors. The first generation contains the TMS32010, TMS320C10, and their spinoffs. These spinoffs include the TMS320C10-14, TMS320C10-25, TMS320C14/E14, TMS320C15/E15, TMS320C15-25, TMS320E15-25 and TMS320C17/E17. The second generation consists of the TMS32020, TMS320C25, and their spinoffs. These spinoffs include the TMS320C25-50 and TMS320E25. The third generation contains the TMS320C30 with spinoffs planned in much the same way as the first and second generation. Many features are common among the TMS320 processors. When the term TMS320 is used, it refers to all three generations of DSP devices. When referring to a specific member of the TMS320 family (i.e. TMS320C15), the name also implies enhanced speed versions and the associated EPROM. Some specific features are added in each processor to provide different cost/performance tradeoffs. Software compatibility is maintained throughout the family to protect the user's investment in architecture. Each processor has software and hardware tools to facilitate rapid design.

This section describes each member of the first, second, and third generations, lists key features, and provides functional block diagrams. Typical applications are also suggested. Two tables provide benchmark comparisons of device performance for some fundamental DSP operations. Included in this section are the following major topics:

- First-Generation Devices (Section 2.1 on page 2-4)
- Second-Generation Devices (Section 2.2 on page 2-9)
- Third-Generation Devices (Section 2.3 on page 2-12)
- Typical Applications (Section 2.4 on page 2-14)

Figure 2-1 shows the current generations of processors on a TMS320 family roadmap, plotted on a hypothetical performance versus technology scale. Table 2-1 provides an overview of the TMS320 family of processors with comparisons of memory, I/O, cycle timing, package type, technology, and military support.

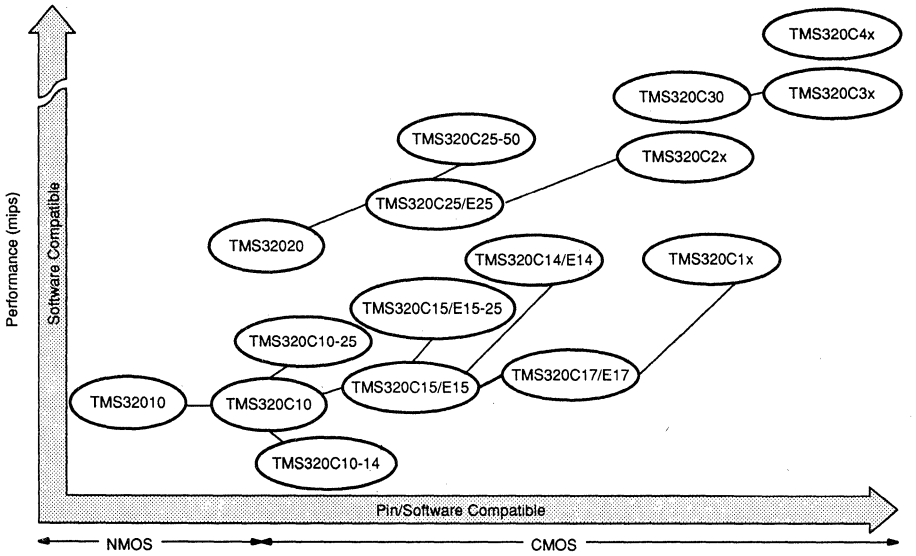

Figure 2-1. The TMS320 Family Roadmap

Table 2-1. TMS320 Family Overview

DEVICE	MEMORY ON-CHIP RAM	MEMORY ON-CHIP ROM	MEMORY OFF-CHIP PROG	MEMORY OFF-CHIP DATA	I/O* SER	I/O* PAR	ON-CHIP TIMER	CYCLE TIME (ns)	PACKAGE TYPE
TMS32010†	144	1.5K	4K			8x16		200	DIP
TMS320C10-14	144	1.5K	4K			8x16		280	DIP/PLCC
TMS320C10†	144	1.5K	4K			8x16		200	DIP/PLCC
TMS320C10-25	144	1.5K	4K			8x16		160	DIP/PLCC
TMS320C14†	256	4K	4K		1	7x16	4	160	PLCC
TMS320E14†	256	4K‡	4K		1	7x16	4	160	Cerquad
TMS320C15†	256	4K	4K			8x16		200	DIP/PLCC
TMS320C15-25	256	4K	4K			8x16		160	DIP/PLCC
TMS320E15†	256	4K‡	4K			8x16		200	DIP/Cerquad
TMS320E15-25.	256	4K‡	4K			8x16		160	DIP/Cerquad
TMS320C17	256	4K			2	6x16	1	100	DIP/PLCC
TMS320E17	256	4K‡			2	6x16	1	200	DIP/Cerquad
TMS32020†	544		64K	64K	1	16x16	1	200	PGA
TMS320C25†	544	4K	64K	64K	1	16x16	1	100	PGA/PLCC
TMS320C25-50	544	4K	64K	64K	1	16x16	1	80	PLCC
TMS320E25	544	4K‡	64K	64K	1	16x16	1	100	Cerquad
TMS320C30†	2K	4K	16M**		2		2	60	PGA

*SER = serial; PAR = parallel.
**Single logical memory space for program, data, and I/O
†Military version available/planned; contact nearest TI Field Sales Office for availability.
‡On-chip EPROM.

2.1 First-Generation Devices

The first generation of the TMS320 family includes the TMS32010 processed in NMOS technology, and the TMS320C10, TMS320C10-14, TMS320C10-25, TMS320C14/E14, TMS320C15/E15, TMS320C15-25, TMS320E15-25, and TMS320C17/E17 processed in CMOS technology. Note when referring to any member of the TMS320 family (i.e. TMS320C15), the name also implies enhanced speed versions and the associated EPROM product. TMS320C1x refers to the first generation family of devices.

The **TMS32010**, the first TMS320 family member, is a microprocessor capable of achieving a 16 x 16-bit multiply in a single 200-ns cycle. The instruction set consists of 60 general purpose and DSP-specific instructions, with most executing in a single cycle. On-chip data memory of 144 words is available. Full-speed execution from up to 4K words of off-chip program memory can be executed at full speed.

The **TMS320C10** has a 200-ns instruction cycle time and is object-code and pin-for-pin compatible with the TMS32010. The TMS320C10 is processed in CMOS technology, achieving a power dissipation less than one-sixth that of the NMOS device. Because of its lower-power dissipation (165 mW), the TMS320C10 is ideal for power-sensitive applications such as digital telephony and portable consumer products. The TMS320C10 is also available in a microcomputer version, with 1.5K words of program ROM on-chip and up to 2.5K words of off-chip program memory for a total of 4K words. This ROM-code version can also operate entirely from off-chip ROM for ease of prototyping, code update, and field upgradeability.

The **TMS320C10-14**, a 14-MHz version of the TMS320C10, provides a low-cost alternative for DSP applications not requiring the maximum operating frequency of the TMS320C10. The device can execute 3.5 million instructions per second and has a 280-ns instruction cycle time.

The **TMS320C10-25**, a 25-MHz version of the TMS320C10, has a 160-ns instruction cycle time. Its low power and higher speed make it well suited for high-performance DSP applications.

The **TMS320C14** and **TMS320E14** are fully object-code compatible with the TMS320C10, and offer the high-performance of a DSP with the on-chip peripherals of a microcontroller. The TMS320C14 incorporates 256 words of RAM, 4K words of ROM or EPROM and five major peripheral blocks optimized for control applications. These five blocks include four timer/counters (two 16-bit general purpose timer/counters, serial port timer, and watchdog timer), an event manager, 16-bit selectable I/O pins, and a synchronous/asynchronous serial port with codec compatible modes.

The **TMS320C15** and **TMS320E15** are fully object-code and pin-for-pin compatible with the TMS320C10 and offer expanded on-chip RAM of 256 words and on-chip program ROM (TMS320C15) or EPROM (TMS320E15) of 4K words. The devices are processed in CMOS technology. The TMS320C15 is also available in a 160-ns version, the **TMS320C15-25** and **TMS320E15-25**.

The **TMS320C17** and **TMS320E17** are dedicated microcomputers with 256 words of on-chip RAM and 4K words of on-chip ROM (TMS320C17) or EPROM (TMS320E17). The TMS320C17 features a dual-channel serial in-

terface, on-chip companding hardware (μ-law/A-law), a serial port timer, and a latched 16-bit coprocessor port for direct microprocessor I/O interface. The devices are processed in CMOS technology.

Some of the key features of the TMS320C1x family are listed below. Specific devices with a particular feature are enclosed in parentheses.

- Instruction cycle timing:
  - 160 ns (TMS320C10-25/C15-25/C14/E14/E15-25)
  - 200 ns (TMS32010/C10/C15/C17/E15/E17)
  - 280 ns (TMS320C10-14)
- 144/256-word on-chip data RAM
- 1.5K/4K-word on-chip program ROM
- 4K-word on-chip program EPROM (TMS320E14/E15/E17)
- EPROM code protection for copyright security
- 4K-word total external memory at full speed
- 16-bit bidirectional data bus at 50-Mbps transfer rate
- 32-bit ALU/accumulator
- 16 x 16-bit parallel multiplier with a 32-bit product
- 0 to 16-bit barrel shifter
- On-chip clock generator
- Eight input and eight output channels
- 2 general-purpose timer/counters (TMS320C14)
- Watchdog timer (TMS320C14)
- Event manager with 6 channel PWM D/A, plus up to 6 compare outputs and up to 4 capture inputs (TMS320C14)
- 16 individual bit selectable I/O pins (TMS320C14)
- Serial port with synchronous/asynchronous codec compatible modes (TMS320C14)
- Dual-channel serial port with timer (TMS320C17)
- Direct interface to combo-codecs (TMS320C14/C17)
- On-chip μ-law/A-law companding hardware (TMS320C17)
- 16-bit coprocessor interface (TMS320C17)
- Single 5-V supply (except for TMS320E14/E15/E17)
- 12.5-V supply additionally required for programming EPROM (TMS320E14/E15/E17)
- Device packaging:
  - 40-pin DIP (TMS32010/C10/C15/E15/C17/E17)
  - 44-pin PLCC (TMS320C10/C15/C17)
  - 44-pin Cerquad (TMS320E15/E17)
  - 68-pin PLCC (TMS320C14)
  - 68-pin Cerquad (TMS320E14)
- Technology:
  - NMOS (TMS32010)
  - CMOS (TMS320C10/C14/E14/C15/E15/C17/E17)
- Commercial and military versions available

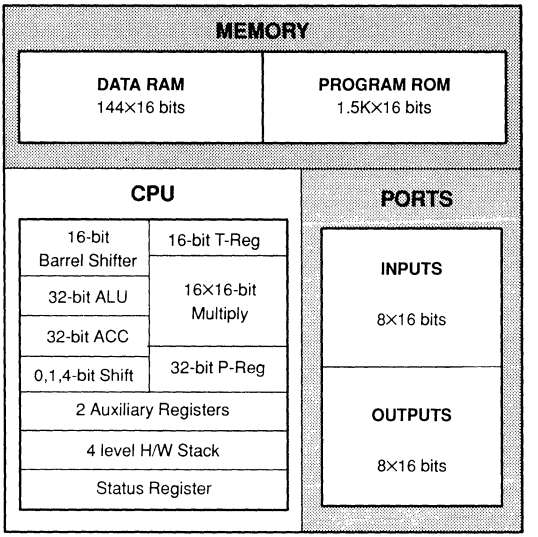

Figure 2-2. TMS320C10 Block Diagram

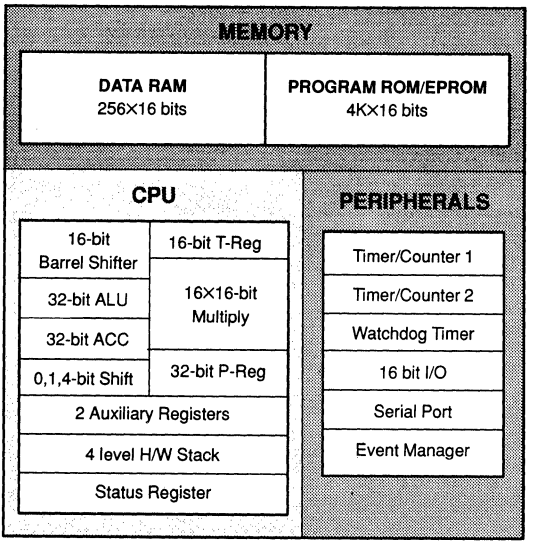

Figure 2-3. TMS320C14 Block Diagram

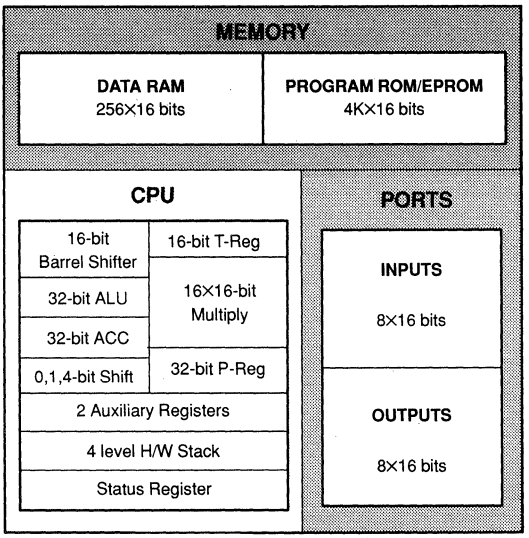

Figure 2-4. TMS320C15 Block Diagram

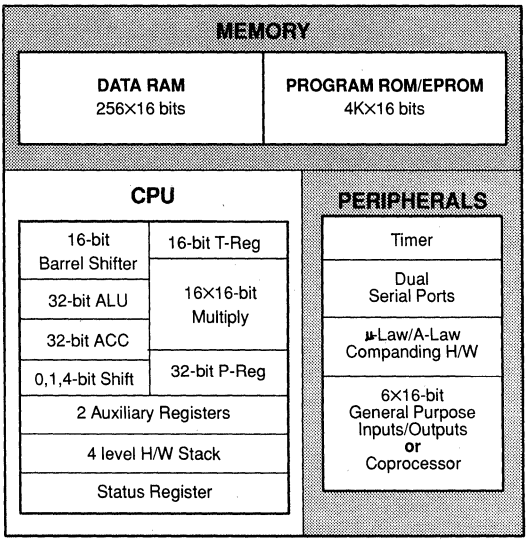

Figure 2-5. TMS320C17 Block Diagram

2.2 Second-Generation Devices

The second generation of the TMS320 family of digital signal processors includes, the TMS32020, TMS320C25/E25, and the TMS320C25-50. The architecture of these devices is extended from that of the TMS32010, the first member of the TMS320 family. This section briefly describes each device, lists key features, and provides a block diagram. Note when referring to any member of the TMS320 family (i.e. TMS320C25), , the name also implies enhanced speed versions and the associated EPROM product. TMS320C2x refers to the second generation family of devices.

The **TMS32020**, processed in NMOS technology, is source-code upward compatible with the TMS32010 and in many applications is capable of two times the throughput of the TMS320C1x devices. It provides an enhanced instruction set (109 instructions), indexed-addressing mode, large on-chip data memory (544 words), 64K-word program and data memory spaces, on-chip serial port, and a hardware timer.

The **TMS320C25** and **TMS320E25** are capable of an instruction cycle time of 100 ns. They are pin-for-pin and object-code upward compatible with the TMS32020. The TMS320C25's enhanced feature set greatly increases the functionality over the TMS32020. Enhancements include the 24 additional instructions (133 total), eight auxiliary registers, an eight-level hardware stack, 4K-words of on-chip program ROM (TMS320C25) or EPROM (TMS320E25), a bit-reversed indexed-addressing mode, and the low-power dissipation inherent to the CMOS process.

The **TMS320C25-50** is a 50 MHz version of the TMS320C25 capable of executing 12.5 MIPS (million instructions per second). The TMS320C25-50 is object code and pin compatible with the TMS320C25. Its higher speed makes it well suited for high-performance DSP applications.

Some of the key features of the TMS320C2x family are listed below. Specific devices with a particular feature are enclosed in parentheses.

- Instruction cycle timing:
  - 80 ns (TMS320C25-50)
  - 100 ns (TMS320C25/E25)
  - 200 ns (TMS32020)
- 544-word programmable on-chip data RAM
- 4K-word on-chip program ROM (TMS320C25)
- 4K-word on-chip program EPROM (TMS320E25)
- 128k-word total data/program memory space
- 32-bit ALU/accumulator
- 16 x 16-bit parallel multiplier with a 32-bit product
- Single-cycle multiply/accumulate instructions
- Repeat instructions for efficient use of program space and enhanced execution
- Block moves for data/program management
- On-chip timer for control operations
- Up to eight auxiliary registers with dedicated arithmetic unit
- Up to eight-level hardware stack

- 0 to 16-bit parallel shifter
- Wait states for communication to slower off-chip memories/peripherals
- Serial port for direct codec interface
- Synchronization input for synchronous multiprocessor configurations
- Global data memory interface
- TMS320C1x source-code upward compatibility
- Concurrent DMA using an extended hold operation (TMS320C25)
- Indexed-addressing mode
- Bit-reversed indexed-addressing mode for radix-2 FFTs (TMS320C25)
- On-chip clock generator
- Single 5-V supply (except for TMS320E25)
- 12.5-V supply additionally required for programming EPROM (TMS320E25)
- Device packaging:
  - 68-pin PGA (TMS32020, TMS320C25)
  - 68-pin PLCC (TMS320C25/C25-50)
  - 68-pin CerQuad (TMS320E25)
- Technology:
  - NMOS (TMS32020)
  - CMOS (TMS320C25)
- Commercial and military versions available

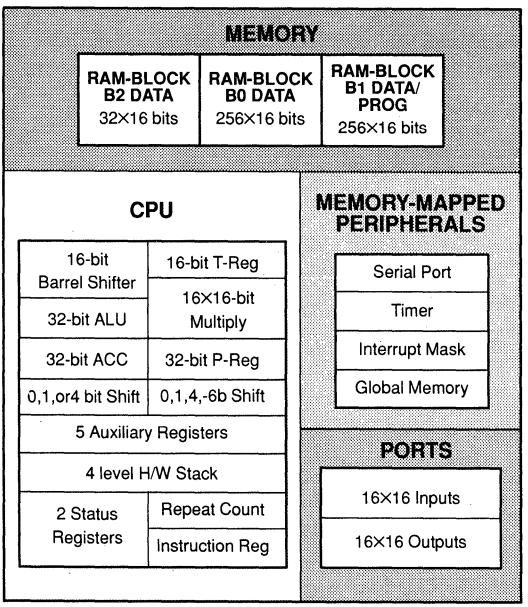

Figure 2-6. TMS32020 Block Diagram

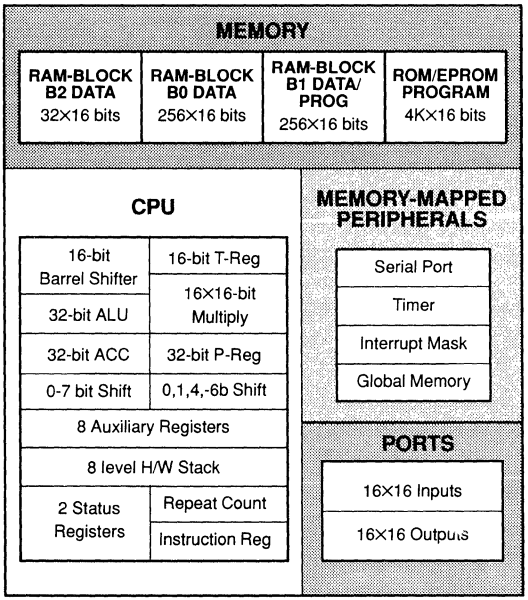

Figure 2-7. TMS320C25/E25 Block Diagram

2.3 Third-Generation Devices

The third generation of the TMS320 family of digital signal processors includes the TMS320C30. The TMS320C30 is a high-performance device capable of executing up to 33 MFLOPS (million floating-point operations per second). Higher performance and ease of use are achieved through greater parallelism, higher accuracy, and general-purpose features. General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, two timers, two serial ports, and multiple interrupt structure. The TMS320C30 supports a wide variety of system applications from host processor to dedicated coprocessor.

Some key features of the TMS320C30 are:

- 60-ns single-cycle instruction execution time
  - 33.3 MFLOPS (million floating-point operations per second)
  - 16.7 MIPS (million instructions per second)
- One 4K x 32-bit single-cycle dual-access on-chip ROM block
- Two 1K x 32-bit single-cycle dual-access on-chip RAM blocks
- 64 x 32-bit instruction cache
- 32-bit instruction and data words, 24-bit addresses
- 16M-word addressing space
- 32-bit barrel shifter
- Eight extended-precision registers (accumulators/product registers)
- Two address generators with eight auxiliary registers and two auxiliary register arithmetic units
- On-chip memory-mapped Direct Memory Access (DMA) controller for concurrent I/O and CPU operation
- Integer, floating point, and logical operations
- Two- and three-operand instructions
- Parallel ALU and multiplier instructions in a single cycle
- Block repeat capability
- Zero-overhead loops and single-cycle branches
- Conditional calls and returns
- Interlocked instructions for multiprocessing support
- Two memory-mapped serial ports to support 8/16/32-bit transfers
- Two memory-mapped 32-bit timers
- Two general-purpose external flags,four external interrupts
- 180-pin grid array (PGA) package; CMOS

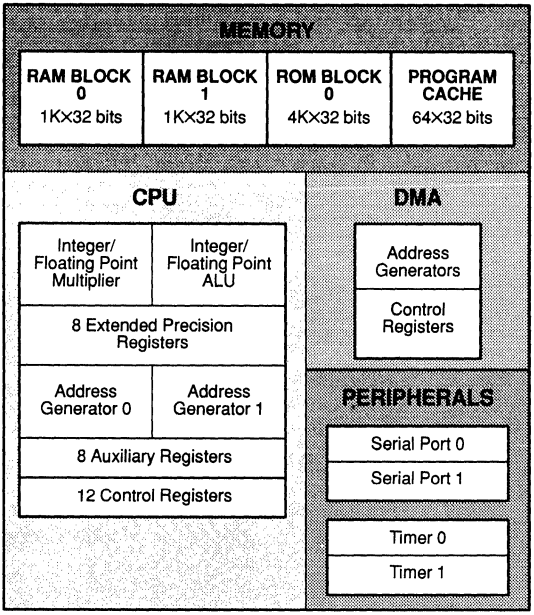

Figure 2-8. TMS320C30 Block Diagram

2.4 Typical Applications

The TMS320 family's unique versatility and realtime performance offer flexible design approaches in a variety of applications. In addition, TMS320 devices can simultaneously provide the multiple functions often required in those complex applications. Table 2-2 lists typical TMS320 family applications.

Table 2-2. Typical Applications of the TMS320 Family

GENERAL-PURPOSE DSP	GRAPHICS/IMAGING	INSTRUMENTATION
Digital Filtering Convolution Correlation Hilbert Transforms Fast Fourier Transforms Adaptive Filtering Windowing Waveform Generation Discrete Cosine Transforms Hartley Transforms	3-D Rotation Robot Vision Image Transmission/ Compression Pattern Recognition Image Enhancement Homomorphic Processing Workstations Animation/Digital Map	Spectrum Analysis Function Generation Pattern Matching Seismic Processing Transient Analysis Digital Filtering Phase-Locked Loops
VOICE/SPEECH	**CONTROL**	**MILITARY**
Voice Mail Speech Vocoding Speech Recognition Speaker Verification Speech Enhancement Speech Synthesis Text-to-Speech	Disk Control Servo Control Robot Control Laser Printer Control Engine Control Motor Control	Secure Communications Radar Processing Sonar Processing Image Processing Navigation Missile Guidance Radio Frequency Modems
TELECOMMUNICATIONS		**AUTOMOTIVE**
Echo Cancellation ADPCM Transcoders Digital PBXs Line Repeaters Channel Multiplexing 1200 to 19200-bps Modems Adaptive Equalizers DTMF Encoding/Decoding Data Encryption Low Speed Transcoders/Vocoders ISDN Basic/Primary Rate Interfaces	FAX Cellular Telephones Speaker Phones Digital Speech Interpolation (DSI) X.25 Packet Switching Video Conferencing Spread Spectrum Communications Answering Machines	Engine Control Vibration Analysis Antiskid Brakes Adaptive Ride Control Global Positioning Navigation Voice Commands Digital Radio Cellular Telephones Active Suspension Noise Suppression
CONSUMER	**INDUSTRIAL**	**MEDICAL**
Radar Detectors Power Tools Digital Audio/TV Music Synthesizer Educational Toys Answering Machines	Robotics Numeric Control Security Access Power Line Monitors	Hearing Aids Patient Monitoring Ultrasound Equipment Diagnostic Tools Prosthetics Fetal Monitors

Table 2-3 provides a comparison of performance for some of the fundamental DSP operations when using either a TMS320C1x, TMS320C2x, or a TMS320C3x. Table 2-4 shows benchmarks for each of the three generations. These performance figures can be further improved by additional optimization of the algorithms for specific design goals, such as CPU loading and program space requirements. Note that these benchmarks only offer an approximation of the system level performance that can be expected.

Table 2-3. TMS320 DSP Family Benchmarks†

BENCHMARK	TMS320C1x CYCLES	@160ns	TMS320C2x CYCLES	@80ns	TMS320C3x CYCLES	@60ns
FIR Filter						
20 Tap	49	127.5 KHz	29	431.03 KHz	25	667 KHz
64 Tap	133	47.0 KHz	73	171.73 KHx	73	228 KHz
67 Tap	139	45.0 KHz	76	164.47 KHz	76	219 KHz
IIR Filter						
4X Biquad	44	142.0 KHz	36	347.22 KHz	23	725 KHz
5X Biquad	56	111.6 KHz	43	284.09 KHz	27	617 KHz
Transpose Biquad	69	90.6 KHz	54	231.48 KHz	37	450 KHz
Dot Product	6	0.96 µs	6	0.48 µs	4	0.240 µs
Matrix Multiply						
2 x 2 Times 2 x 2	24	3.84 µs	21	1.7 µs	12	0.720 µs
3 x 3 Times 3 x 1	24	3.84 µs	22	1.8 µs	13	0.780 µs
Memory to Memory FFT						
64 Point Radix 2	3687	590 µs	3088	247 µs	2603	156 µs
256 Point Radix 2	41478	6.64 ms	17602	1.408 ms	12857	0.771 ms
1024 Point Radix 2	331237	53.0 ms	109755	8.784 ms	61511	3.67 ms
Port to Memory FFT						
64 Point Radix 2	2954	473 µs	1621	130 µs	1370	75 µs
256 Point Radix 2	41478	6.64 ms	8520	0.682 ms	6734	0.354 ms
1024 Point Radix 2	331237	53.0 ms	56286	4.503 ms	32354	1.67 ms

† More information available in EDN magazine September 29, 1988 pp. 126-148.

Table 2-4. TMS320 DSP System Benchmarks

Application	TMS320C1x	TMS320C2x	TMS320C3x†
	CPU Loading		
Echo cancellation (CCITT G.165) Echo length 16 mS	–	50%	22%
Data encryption (ANSI X3.92-1981) Data rate 42 kbps	100%	52%	<25%
Split-band modem (CCITT V.22/212A) full-duplex	64%	30%	<14%
32-kbps ADPCM (CCITT G.721) half-duplex	100%	50%	<25%
2400-bps LPC-10 (DOD 43) half-duplex	76%‡*	40%‡	<17%
2400-bps LPC-10 (DOD 52) half-duplex	–	87%‡*	<35%
16-kbps subband coder full-duplex	64%‡	35%	<16%

† Conservative benchmarks based on extrapolated data.
‡ Requires external data memory.
* Requires external program memory.

Section 3

TMS320 Development Support Products

Texas Instruments is dedicated to supporting designers in the complete development of their application from concept through production. An extensive line of development support products is offered to assist the user in all aspects of TMS320 design and development. These products range from development and application software to complete hardware development and integration systems such as the TMS320C3x XDS1000 Development Environment.

Figure 3-1 shows the typical application development flow. TMS320 system evaluation begins with the use of tools such as a simulator, TMS320 Evaluation Module (EVM), or Emulator (XDS). These support tools, plus an assembler/linker, allow the designer to evaluate the processor's performance, benchmark time-critical code, and determine the feasibility of using a TMS320 device to implement a specific algorithm. Extensive documentation provides information concerning device specifications and capabilities. The TI Regional Technology Centers (RTCs) offer three-day DSP design workshops that provide hands-on experience with TMS320 development tools (see Section 8.2).

Software and hardware design can be performed in parallel by using the macro assembler/linker and simulator for software development and the XDS for hardware development. The assembler/linker translates the system's assembly source program into an object module that can be executed by the simulator, SoftWare Development System (SWDS), XDS, or EVM. The XDS provides realtime in-circuit emulation and is a powerful tool for system debugging and integrating software and hardware modules. EPROM DSP's are available which provide for early prototype development, smoothing the transition to the production phase. Once the design cycle for a product is complete, TI offers three generations of DSPs to meet future application needs.

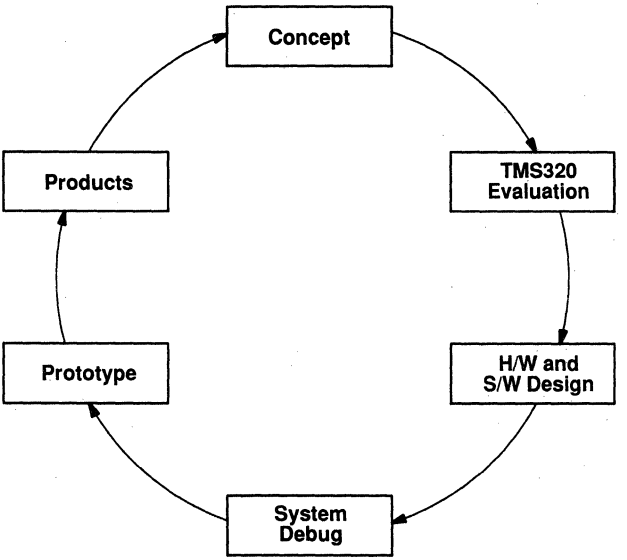

Figure 3-1. Typical TMS320 Application Development Flow

Figure 3-2 shows development product integration. The appropriate TMS320 support product is indicated for each stage of development. Table 3-1 provides a feature matrix of the TMS320 simulation/emulation development tools, comparing capabilities such as development purpose, software and hardware features, and amount of memory.

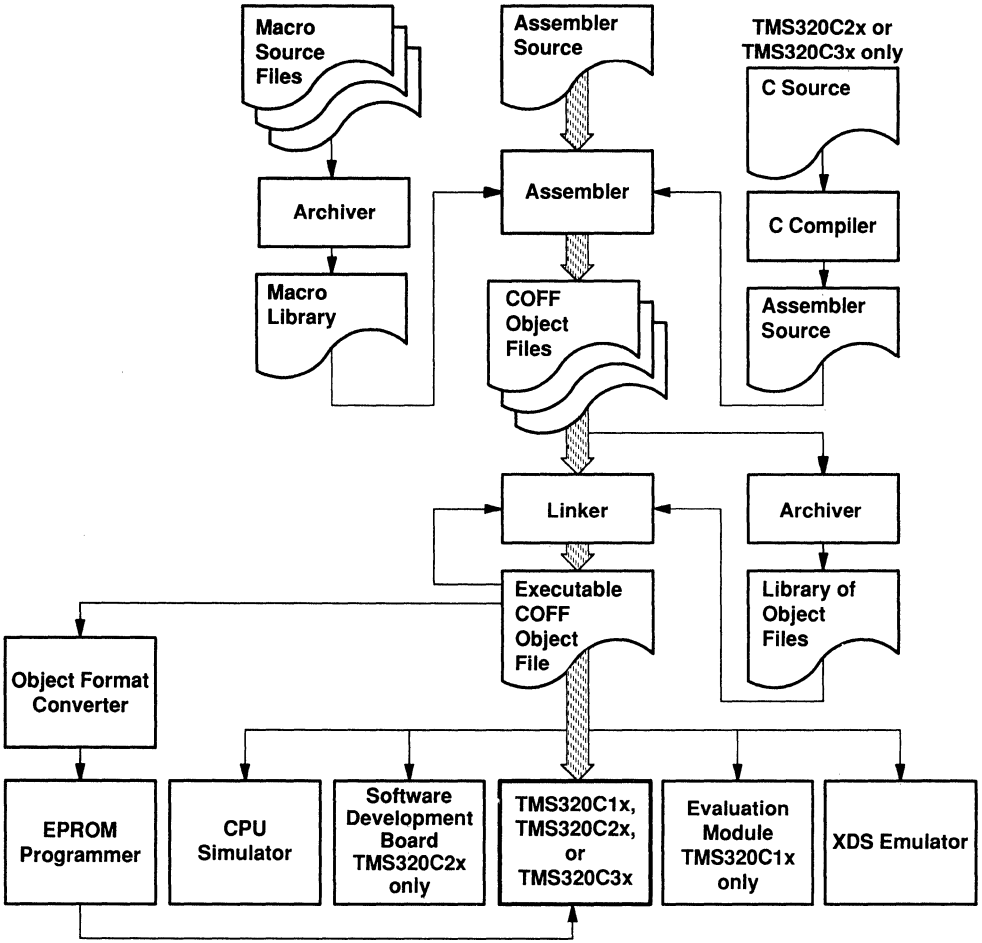

Figure 3-2. TMS320 Development Product Integration

Table 3-1. Feature Matrix of TMS320 Simulation/Emulation Development Tools

FEATURES	EVM	SIMULATOR	SWDS	XDS/22	XDS500	XDS1000
Development Purpose:						
Evaluation/benchmarking	Yes	Yes	Yes	Yes	Yes	Yes
Software development	No	Yes	Yes	Yes	Yes	Yes
Hardware design	No	No	No	Yes	Yes	Yes
Line-by-line assembler/reverse assembler	Yes	Yes (C30 only)	Yes	Yes	Yes	Yes
Modify/display memory and registers	Yes	Yes	Yes	Yes	Yes	Yes
Single-stepping	Yes	Yes	Yes	Yes	Yes	Yes
Breakpoint on Instruction Acquisition	Yes	Yes	Yes	Yes	Yes	Yes
Breakpoint on memory access/ read/write	No	Yes	No	Yes	No	No
Time-stamping/clock counter	No	Yes	No	Yes	Yes	Yes
Realtime trace samples	No	No	No	Yes	No	No
Multi-user system	No	Yes	No	No	No	No
Built-in system interface	No	No	Yes	No	Yes	Yes
Files associated to I/O ports	No	Yes	Yes	No	No	Yes (w/ SPOX)
Full-speed in-circuit emulation:						
From on-board memory	Yes	N/A	Yes	Yes	No	Yes
From target memory	No	N/A	No	Yes	Yes	Yes
Amount of memory:						
On-board program/data (TMS320C1x)	4K/-	N/A	N/A	4K/-	N/A	N/A
On-board program/data (TMS320C2x)	N/A	N/A	24K	4K/4K	N/A	N/A
Program/data expansion	N/A	N/A	N/A	64K*	N/A	16K
Static RAM/DRAM	N/A	N/A	N/A	N/A	N/A	32K/512K
Devices Supported	320C10/ C15	320C1x/ C2x/C3x	320C2x	320C1x /C2x	320C3x	320C3x

* Memory expansion board allows for memory expansion to 64K words total of program and data memory, configurable in 1K blocks.

Section 4

Software Development and Support Products

Many support products are offered for the TMS320 family of digital signal processors. This section discusses the software support products, which include Macro Assembler/Linkers, C Compilers, Simulators, a SoftWare Development System (SWDS), a Digital Filter Design Package (DFDP), a DSP Software Library, TMS320 Bell 212A Modem Software, Data Encryption Standard Software, and SPOX (the TMS320C3x operating system). These products are described in the sections listed below.

- TMS320 Macro Assembler/Linkers (Section 4.1 on page 4-2)
- TMS320 C Compilers (Section 4.2 on page 4-4)
- TMS320 Simulators (Section 4.3 on page 4-10)
- SoftWare Development System (SWDS) (Section 4.4 on page 4-28)
- Digital Filter Design Package (DFDP) (Section 4.5 on page 4-35)
- Digital Signal Processing Software Library (Section 4.6 on page 4-37)
- TMS320 Bell 212A Modem Software (Section 4.7 on page 4-39)
- Data Encryption Standard Software (Section 4.8 on page 4-40)
- SPOX: TMS320C3x DSP Operating System (Section 4.9 on page 4-41)

4.1 TMS320 Macro Assembler/Linker

The TMS320 Macro Assembler/Linker is a software development tool that converts TMS320 assembly language source files into executable object code. The TMS320 Macro Assembler/Linker is shipped with four programs to address specific software development needs. They are listed and described below:

The **assembler** translates assembly language source files into machine language object files. Source files can contain instructions, assembler directives, and macro directives. Assembler directives control various aspects of the assembly process such as the source listing format, symbol definition, and how the source code is placed into sections. The following versatile features distinquish the TMS320 assembler:

- Processes the source statements in a text file to produce a relocatable object file.
- Produces a source listing (if requested) and provides control over this listing.
- Appends a cross-reference listing to the source listing (if requested).
- Allows segmentation of users code.
- Maintains a SPC (section program counter) for each section of object code.
- Defines and references global symbols.
- Assembles conditional blocks.
- Supports macros, allowing user to define macros inline or in a macro library.

The **linker** combines object files into a single executable object module. As it creates the executable module, it performs relocation and resolves external references. The linker accepts COFF (common object file format) object files (created by the assembler) as input. It can also accept archive library members and modules created by a previous linker run. Linker directives allow the user to combine object file sections, bind sections or symbols to specific addresses, and define or redefine global symbols. These versitile features distinquish the TMS320 linker:

- Defines a memory model that conforms to target system memory.
- Combines object file sections.
- Allocates sections into specific areas in the target system memory.
- Defines or redefines global symbols to assign them specific values.
- Relocates sections to assign them to final addresses.
- Resolves undefined external references between input files.

The **archiver** allows collection of a group of files into a single archive file. For example, several macros can be collected together into a macro library. The assembler will search through the library and use the members that are called as macros by the source file. It is also possible to use the archiver to collect a group of object files into an object library. The linker will include the members in the library that resolve external references during the link.

Most EPROM programmers do not accept COFF object files as input. The **object format converter** converts a COFF object file into Intel, Tektronix, or TI tagged hex object format. The converted file can be downloaded to an EPROM programmer.

The TMS320 Macro Assembler/Linker is currently available for the first, second, and third generation TMS320 devices. The operating systems supported are PC/MS-DOS (in 5.25" DS/DD floppy), plus the VAX/VMS (in Backup format), VAX/ULTRIX (in TAR format), and SUN-3/UNIX (in TAR format) in 1600 bpi magnetic tape mediums.

For part number information, please reference Appendix A of this document. For pricing and availability, contact the nearest TI Field Sales Office.

4.2 TMS320 C Compiler

The TMS320 C compiler is a full implementation of the standard Kernighan and Ritchie C. The compiler accepts a source file containing a program module written in the widely used C language. It outputs TMS320 assembly language source code which is then processed by the assembler. This compiler also provides the enhancements of enumeration types, passing and returning structures to functions, and structure assignment.

This high-level language compiler allows time-critical routines written in assembly to be called within the C program. The converse is also available; assembly routines may call C functions. Assembly statements may also be introduced inline with the C source. The output of the compiler can be edited prior to assembly/link to further optimize the performance of the code.

The C compiler has three parts: a preprocessor, a parser, and a code generator. Figure 4-1 illustrates the three-step process of compiling a C program.

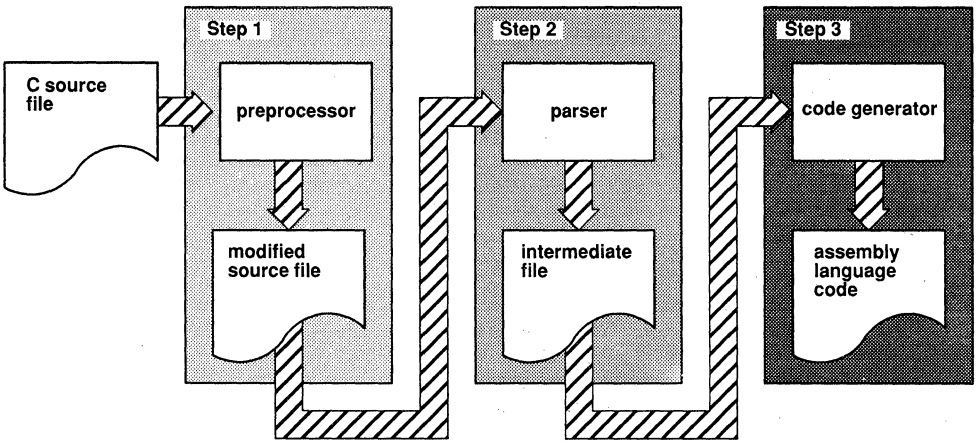

Figure 4-1. Compiling a C Program

Step 1: The input for the **preprocessor** is a C source file (as described in Kernighan and Ritchie). The preprocessor produces a modified version of the source file.

Step 2: The input for the **parser** is the modified source file produced by the preprocessor. The parser produces an intermediate file.

Step 3: The input for the **code generator** is the intermediate file produced by the parser. The code generator produces an assembly language source file.

Step 4: After the program is compiled, it must be assembled and linked. (Note that version 5.xx assembler/linker must be used for the TMS320C2x, version 1.xx assembler/linker for the TMS320C3x).

Some of the tasks that a C program must perform (such as memory allocation, string conversion, and string searches) are not part of the C language. The run-time-support functions, which are shipped with the C compiler, are standard functions that perform these tasks. The run-time-support library **rts.lib** contains the object code for these functions as well as other functions and routines.

> **Note:** The rts.src library contains EOF (end-of-file) markers which cannot be handled by some text editors. The archiver must be utilized to access this source code.

Some of the included header files that declare the run-time-support functions are listed below with a description.

1) **assert.h** - Defines the assert macro, which provides a standard method for allowing programs to create diagnostic failure messages at run-time.

   - Functions included as follows:
     - TMS320C2x - **assert ()**
     - TMS320C3x - **assert ()**

2) **ctype.h** - Declares functions and defines macros that test or convert ASCII characters.

   - The character testing functions have names with the format **isxxxx** (for example, **isdigit**). These functions return true (1) or false (0).
   - The character conversion functions have names with the format **toxxxx** (for example, **toupper**). They convert a character to lowercase, uppercase, or ASCII, and return the converted character.
   - Functions included for both the TMS320C2x and TMS320C3x are:
     - **isalnum(), isalpha(), isascii(), iscntrl(), isdigit(), isgraph(), islower(), isproint(), ispunct(), isspace(), isxdigit(), toascii(), tolower(), toupper()**

3) **float.h** and **limits.h** - Define macros that expand to useful limits and parameters of numeric representations. Table 4-1 and Table 4-2 list these macros and the limits with which they are associated.

Table 4-1. Macros That Supply Character and Integer Limits

Macro	Value		Description
	320C2x	320C3x	
CHAR_BIT	16	32	Maximum number of bits for the smallest object that is not a bit field
SCHAR_MIN	-32768	-2147483648	Minimum value for a signed character
SCHAR_MAX	32767	2147483647	Maximum value for a signed character
UCHAR_MAX	65535	4294967295	Maximum value for an unsigned character
CHAR_MIN	SCHAR_MIN		Minimum value for a character
CHAR_MAX	SCHAR_MAX		Maximum value for a character
SHRT_MIN	-32768	-2147483648	Minimum value for a short integer
SHRT_MAX	32767	2147483647	Maximum value for a short integer
USHRT_MAX	65535	4294967295	Maximum value for a short unsigned integer
INT_MIN	-32768	-2147483648	Minimum value for an integer
INT_MAX	32767	2147483647	Maximum value for an integer
UINT_MAX	65535	4294967295	Maximum value for an unsigned integer
LONG_MIN	-32768	-2147483648	Minimum value for a long integer
LONG_MAX	32767	2147483647	Maximum value for a long integer
ULONG_MAX	65535	4294967295	Maximum value for an unsigned long integer

Table 4-2. Macros That Supply Floating-Point Range Limits

Macro	Value		Description
	320C2x	320C3x	
FLT_RADIX	2	2	Base or radix of exponent representation
FLT_ROUNDS	1	1	Rounding mode for floating-point addition (rounds to nearest integer)
FLT_DIG DBL_DIG LDBL_DIG	6	6	Number of decimal digits of precision for a float, double or long double
FLT_MANT_DIG DBL_MANT_DIG LDBL_DIG	24	24	Number of base-FLT_RADIX digits in the mantissa of a float, double or long double
FLT_MIN_EXP DBL_MIN_EXP LDBL_MIN_EXP	-125	-126	Minimum negative integer such that FLT_RADIX raised to that power minus 1 is a normalized float, double, or long double
FLT_MAX_EXP DBL_MAX_EXP LDBL_MAX_EXP	128	128	Maximum integer such that FLT_RADIX raised to that power minus 1 is a representable finite float, double, or long double
FLT_EPSILON DBL_EPSILON LDBL_EPSILON	1.19209290E-07	1.19209290E-07	Minimum positive float, double, or long double χ such that $1.0 + \chi \neq 1.0$
FLT_MIN DBL_MIN LDBL_MIN	1.17549435E-38	5.8774717E-39	Minimum positive float, double, or long double
FLT_MAX DBL_MAX LDBL_MAX	3.4028235E+38	3.4028235E+38	Maximum float, double, or long double
FLT_MIN_10_EXP DBL_MIN_10_EXP LDBL_MIN_10_EXP	-37	-38	Minimum negative integer such that 10 raised to that power is in the range of normalized floats, doubles, long doubles
FLT_MAX_10_EXP DBL_MAX_10_EXP LDBL_MAX_10_EXP	38	38	Maximum integers such that 10 raised to that power is in the range of representable finite floats, doubles or long doubles

4) **math.h** - Defines several trigonmetric, exponential, and logarithmic functions.

   - Functions included for both the TMS320C2x and TMS320C3x are:
     - **acos(), asin(), atan(), atan2(), ceil(), cos(), cosh(), exp(), fabs(), floor(), fmod(), frexp(), ldexp(), log(), log10(), modf(), pow(), sin(), sinh(), sqrt(), tan(), tanh()**

5) **starg.h** - A function can be called with a variable number of arguments with different types. A variable-argument function can use the objects declared by **starg.h** to ascertain the number and types of the arguments that are passed to it.

   - Functions included for both the TMS320C2x and TMS320C3x are:
     - **va_arg(), va_end(), va_start()**

6) **stddef.h** - Defines types and macros used by several of the runtime-support functions.

7) **stdlib.h** - Declares several macros as well as types. The **stdlib.h** header declares several kinds of functions.

   - Memory management functions that allow the user to allocate and deallocate packets of memory.
   - String-conversion functions that convert strings to numeric representations.
   - Searching and sorting functions that allows the user to search and sort arrays.
   - Sequence-generation functions that allows the user to generate a pseudo-random sequence and choose a starting point for a sequence.
   - Function-exit functions that allows the user to terminate functions either normally or abnormally.
   - Functions included for both the TMS320C2x and TMS320C3x are:
     - **abs(), abort(), atexit(), atof(), atoi(), atol(), bsearch(), calloc(), exit(), free(), labs(), ltoa(), malloc(), movmem(), qsort(), rand(), realloc(), srand(), strtod(), strtol, strtoul()**
     - The TMS320C2x also includes the **minit()** function.
     - The TMS320C3x also includes the **div(), ldiv(), strspn()**, and **strstr()** functions.

8) **string.h** - Declares functions that allow the user to perform the following tasks with character arrays (strings):

   - Move or copy entire strings or portions of strings to another location.

- Concatenate strings.
- Compare strings.
- Search strings for characters or other strings.
- Find the length of a string.
- Functions included for both the TMS320C2x and TMS320C3 are:
  - **memchr(), memcmp(), memcpy(), memmove(), memset(), strcat(), strchr(), strcmp(), strcoll(), strcpy(), strcspn(), strerror(), strlen(), strncat(), strncmp(), strncpy(), strpbrk(), strrchr(), strtok()**
  - The TMS320C2x also includes the **strspn()**, and **strstr()** functions.

9) **ioports.h** - Declares functions that provide low-level access to the external I/O ports of the TMS320C2x.

- Functions included for the TMS320C2x are:
  - **inport(), outport()**

The C compiler is available from TI for the second and third generation TMS320 devices. High level language support for all three generations is available from TMS320 Third Parties (see Section 9). The TMS320 C compiler is supplied for the PC/MS-DOS (in 5.25" DS/DD floppy), plus the VAX/VMS (in Backup format), VAX/ULTRIX (in TAR format), and SUN-3/UNIX (in TAR format) in 1600 bpi magnetic tape mediums.

For part number information, refer to Appendix A. Contact the nearest TI Field Sales Office for pricing and availability.

4.3 TMS320 Simulator

The TMS320 Simulator is a software program that simulates the TMS320 microprocessor and microcomputer modes for cost-effective TMS320 software development and program verification in non-realtime. Using the inexpensive software simulator allows debugging without the requirement of hardware. Files may be associated with I/O ports so that specific I/O values may be used during test and debug. Time-critical code can be tested, as well as individual portions of the program. The clock counter allows loop timing during code optimization. Breakpoints can be established, based on read and write execution and instruction acquisition, with program and data memories.

The simulator uses TMS320 object code produced by the TMS320 Macro Assembler/Linker. Input and output files may be associated with the port addresses of the I/O instructions, simulating the I/O devices connected to the processor. The interrupt flag can be set periodically at programmed intervals to simulate an interrupt signal. Before initiating program execution, breakpoints and traces may be defined and enabled.

During program execution, the internal registers and memory of the simulated TMS320 are modified as the host computer interprets each instruction. Execution is suspended when a breakpoint or error is encountered, a branch to 'self' is detected, or a breakpoint from the keyboard is entered by the user.

Once program execution is suspended, the internal registers and both program and data memories can be inspected and/or modified. The trace memory can also be displayed. A record of the simulation session can be maintained in a journal file. This allows the session to be re-executed to regain the same machine state during a subsequent simulation session.

Before beginning a debugging session, TMS320 source code must first be written and assembled. If there are multiple modules, they must be linked. The linked absolute code is then loaded into the simulator and executed during simulation.

4.3.1 TMS320C1x Simulator

The TMS320C1x simulator is available for the IBM PC/MS-DOS (5.25" floppy) and the VAX/VMS (in Backup format on 1600 bpi magnetic tape) operating systems. The PC configuration requires a minimum of 256K-bytes RAM for the TMS320C1x simulator. Table 4-3 lists the commands, broken down by category, for the TMS320C1x simulator. Figure 4-2 shows an example TMS320C1x simulator screen display. These key features highlight simulator flexibility for effective TMS320C1x software development:

- Interrupt generation at user-defined intervals
- File-associated I/O with 8 ports
- Programmable breakpoints on:
  - Instruction acquisition
  - Memory reads or writes (data or program)
  - Data patterns on the D-bus or the P-bus
  - Error conditions
- Timing analysis relative to clock rate
- Trace on accumulator, program counter, and auxiliary registers

- Single stepping of instructions
- Data and program memory modification and display
- Modification and inspection of registers
- Error messages for:
  - Illegal opcodes
  - Invalid data entry
- Execution of commands from a journal file

For part number information, refer to Appendix A. Contact the nearest TI Field Sales Office for pricing and availability.

Table 4-3. TMS320C1x Simulator Commands

MAIN MENU COMMANDS	
Command	**Function†**
DM or <CR>	Display Main Menu
DT	Display Trace Buffer
JF	Select Journal File
ST	Display/Update Register Status
STR	Save Trace Buffer
TR	Toggle Trace
Z	Zero Clock Counter
HELP COMMANDS	
Command	**Function†**
BH	Breakpoint Help
IOH	Input/Output Help Menu
MH	Modify/Inspect Memory Help Menu
RH	Modify/Inspect Registers/Flags Help Menu
EXECUTION COMMANDS	
Command	**Function†**
C	Continue Simulation
ERAM	Expand RAM and ROM (TMS320C10)
EX	Execute Commands from Given File
L	Load New Object File
LC	Load New COFF File
NB	Set Number of Instructions Until Break (TMS320C10)
Q	Quit Simulation
R	Run Simulation
RS	Reset Simulator
SS	Perform Single-Step Execution
BREAKPOINT COMMANDS	
Command	**Function†**
BDP	Breakpoint on Data Pattern When Read/Write from/to Data RAM
BDR	Breakpoint on Data RAM Read
BDRW	Breakpoint on Data RAM Read and Write
BDW	Breakpoint on Data RAM Write
BER	Breakpoint on an Error Condition
BIAQ	Breakpoint on Instruction Acquisition
BPP	Breakpoint on Data Pattern When Read from Program ROM
BPR	Breakpoint on Program ROM Read
DB	Display Breakpoints
RB	Remove Breakpoint

† If a command pertains to one or two processors only, this is indicated in parentheses.

Table 4-3. TMS320C1x Simulator Commands (Concluded)

INPUT/OUTPUT COMMANDS	
Command	**Function†**
LF	List Files Assigned to Ports (TMS320C10)
RCVC	Close the RCV Channel File
RSI	Reset Selected Input Port File
SI	Select Input Port File
SO	Select Output Port File
INTERRUPT/TIMING COMMANDS	
Command	**Function†**
TIC	Specify Number of Clock Ticks Until Next Interrupt (TMS320C10)
ZTIC	Disable Tick Commands
MODIFY/INSPECT MEMORY COMMANDS	
Command	**Function†**
RAM	Modify/Inspect Individual Data RAM
RAMH	Display Data RAM in Hexidecimal
RAMI	Display Data RAM in Integer
ROM	Modify/Inspect Individual Program ROM
ROMH	Display Program ROM in Hexidecimal
ROMI	Display Program ROM in Integer
MODIFY/INSPECT REGISTER/FLAGS COMMANDS	
Command	**Function†**
ACC	Modify/Inspect Accumulator
AR	Modify/Inspect Auxiliary Registers
BIO	Modify/Inspect I/O Branch Control
CC	Modify/Inspect Clock Counter
INTF	Modify/Inspect Interrupt Flag Register (TMS320C10)
INTM	Modify/Inspect Interrupt Mode Register
P	Modify/Inspect P Register
PC	Modify/Inspect Program Counter
SK	Modify/Inspect Stack
T	Modify/Inspect T Register
MODIFY/INSPECT STATUS REGISTERS/PINS COMMANDS	
Command	**Function†**
ARP	Modify/Inspect Auxiliary Register Pointer
DP	Modify/Inspect Data Memory Page Pointer
INTM	Modify/Inspect Interrupt Mode Register
OV	Modify/Inspect Overflow Flag
OVM	Modify/Inspect Overflow Mode Register

† If a command pertains to one or two processors only, this is indicated in parentheses.

```
>>PC=   0    OPCODE=   0    ADD                    PREVIOUS PC=   0

          ARP      AR0      AR1     TREG      PREG      ACC       CLK
INTEGER    0        0        0        0         0         0         1
HEX        0        0        0        0         0         0         1

>>STK=   0    0    0    0          DP = 0    INTF= 0    OV = 0
                                   BIO= 1    INTM= 0    OVM= 0

ENTER <CR> TO CONTINUE
     "-" TO RETURN TO MAIN


>>PC=   1    OPCODE=   0    ADD                    PREVIOUS PC=   0

          ARP      AR0      AR1     TREG      PREG      ACC       CLK
INTEGER    0        0        0        0         0         0         2
HEX        0        0        0        0         0         0         2

>>STK=   0    0    0    0          DP = 0    INTF= 0    OV = 0
                                   BIO= 1    INTM= 0    OVM= 0

ENTER <CR> TO CONTINUE
     "-" TO RETURN TO MAIN
```

Figure 4-2. TMS320C1x Simulator Screen Example

4.3.2 TMS320C2x Simulator

The TMS320C2x simulator is available for the IBM PC/MS-DOS (5.25″ floppy) and the VAX/VMS (in Backup format on 1600 bpi magnetic tape) operating systems. The PC configuration requires a minimum of 640K-bytes RAM for the TMS320C2x simulator. Table 4-4 lists the commands, broken down by category, for the TMS320C2x simulator. Figure 4-3 shows an example TMS320C2x simulator screen display. These key features highlight simulator flexibility for effective TMS320C2x software development:

- Commands are provided to specifiy wait cycles for external data, program, and I/O memory. This provides a more flexible, accurate timing analysis for interrupt generation at user-specified intervals
- File associated I/O with 16 ports

- Programmable breakpoints on:
  - Instruction acquisition
  - Memory reads or writes (data or program)
  - Data patterns on the Data bus or Program bus
  - Error conditions
- Timing analysis relative to clock rate
- Trace on accumulator, program counter, and auxiliary registers
- Single stepping of instructions
- Data and program modification and display:
  - Change an entire block at any time
  - Initialize memory before a program is loaded
- Commands to modify and inspect registers as well as individual locations in a register
- Interrupt generation at user-defined intervals
- Error messages for:
  - Illegal opcodes
  - Invalid data entry
- Execution of commands from a journal file
- Save-states for restarting simulation
- File associated serial port for transmission and reception of ASCII data file

Table 4-4. TMS320C2x Simulator Commands

MAIN MENU COMMANDS	
Command	**Function**
DC	Display Variable Value and Format
DCL	Enable Digital Command Language
DM or <CR>	Display Main Menu
DT	Display Trace Buffer
JF	Select Journal File
SIM	Change Simulator Mode
ST	Display/Update Register Status
STR	Save Trace Buffer
SW	Switch from Screen to File
TR	Toggle Trace
Z	Zero Clock Counter
ZRAM	Set RAM contents to Zero
HELP COMMANDS	
Command	**Function†**
BH	Breakpoint Help
DH	Display Controller Help Menu
EH	Execution Help Menu
IOH	Input/Output Help Menu
MH	Modify/Inspect Memory Help Menu
RH	Modify/Inspect Registers/Flags Help Menu
STH	Modify/Inspect Status Register/Pins Help Menu
TH	Trace Help Menu
TICH	Interrupt/Timing Help Menu
UTLH	Utilities Help Menu
EXECUTION COMMANDS	
Command	**Function†**
C	Continue Simulation
EX	Execute Commands from Given File
L	Load New Object File
LC	Load New COFF File
NB	Set Number of Instructions Until Break
Q	Quit Simulation
R	Run Simulation
RS	Reset Simulator
SS	Perform Single-Step Execution

Table 4-4. TMS320C2x Simulator Commands (Continued)

BREAKPOINT COMMANDS	
Command	**Function**
BDP	Breakpoint on Data Pattern When Read/Write from/to Data RAM
BDR	Breakpoint on Data RAM Read
BDRW	Breakpoint on Data RAM Read and Write
BDW	Breakpoint on Data RAM Write
BER	Breakpoint on an Error Condition
BIAQ	Breakpoint on Instruction Acquisition
BPP	Breakpoint on Data Pattern When Read from Program ROM
BPR	Breakpoint on Program ROM Read
DB	Display Breakpoints
RB	Remove Breakpoint
INPUT/OUTPUT COMMANDS	
Command	**Function†**
LI	List Files Assigned to Input Ports
LO	List Files Assigned to Output Ports
RCV	Assign RCV Channel to File
RCVC	Close the RCV Channel File
RSI	Reset Selected Input Port File
SI	Select Input Port File
SO	Select Output Port File
XMT	Assign XMT Channel to File
XMTC	Close the XMT Channel File
INTERRUPT/TIMING COMMANDS	
Command	**Function†**
DWAIT	Specify Wait Cycles for External Data Memory
IOWAIT	Specify Wait Cycles for External I/O Memory
PWAIT	Specify Wait Cycles for External Program Memory
TIC0-TIC2	Specify Number of Clock Ticks (TIC0-TIC2) until interrupt
ZTIC	Disable Tick Commands

Table 4-4. TMS320C2x Simulator Commands (Continued)

MODIFY/INSPECT MEMORY COMMANDS	
Command	**Function**
LRAM	Load RAM Data from an External File
POP	Restore Simulator State
PUSH	Save Simulator State
RAM	Modify/Inspect Individual Data RAM
RAMH	Display Data RAM in Hexidecimal
RAMI	Display Data RAM in Integer
ROM	Modify/Inspect Individual Program ROM
ROMH	Display Program ROM in Hexidecimal
ROMI	Display Program ROM in Integer
SGN	Generate Test Data
SRAM	Store RAM Data to an External File
VIEW	Display Stack Contents
MODIFY/INSPECT REGISTER/FLAGS COMMANDS	
Command	**Function†**
ACC	Modify/Inspect Accumulator
AR	Modify/Inspect Auxiliary Registers
BIO	Modify/Inspect I/O Branch Control
CC	Modify/Inspect Clock Counter
FSM	Modify/Inspect Frame Sync Mode
INTFS	Modify/Inspect Interrupt Flags
INTM	Modify/Inspect Interrupt Mode Register
INTMS	Modify/Inspect Interrupt Masks
P	Modify/Inspect P Register
PC	Modify/Inspect Program Counter
RPTC	Modify/Inspect Repeat Instruction Counter
SK	Modify/Inspect Stack
T	Modify/Inspect T Register
TINT	Modify/Inspect Timer Interrupt Flag
TINTM	Modify/Inspect Timer Interrupt Mask

Table 4-4. TMS320C2x Simulator Commands (Concluded)

MODIFY/INSPECT STATUS REGISTERS/PINS COMMANDS	
Command	**Function**
ARB	Modify Auxiliary Register Pointer Buffer
ARP	Modify/Inspect Auxiliary Register Pointer
CNF	Modify/Inspect RAM Configuration Control Bit
CY	Modify/Inspect Carry Bit
DP	Modify/Ibspect Memory Page Pointer
FO	Modify/Inspect Format Bit
HM	Modify/Inspect Hold Mode Bit
INTM	Modify/Inspect Interrupt Mode Register
OV	Modify/Inspect Overflow Flag
OVM	Modify/Inspect Overflow Mode Register
PM	Modify/Inspect Product Shift Mode
RINTM	Modify/Inspect RINTM Bit
SXM	Modify/Inspect Sign-extension Mode Bit
TC	Modify/Inspect Test/Control Flag Bit
TXM	Modify/Inspect Mode Bit
XF	Modify/Inspect XF Pin
XINTM	Modify/Inspect XINTM Bit

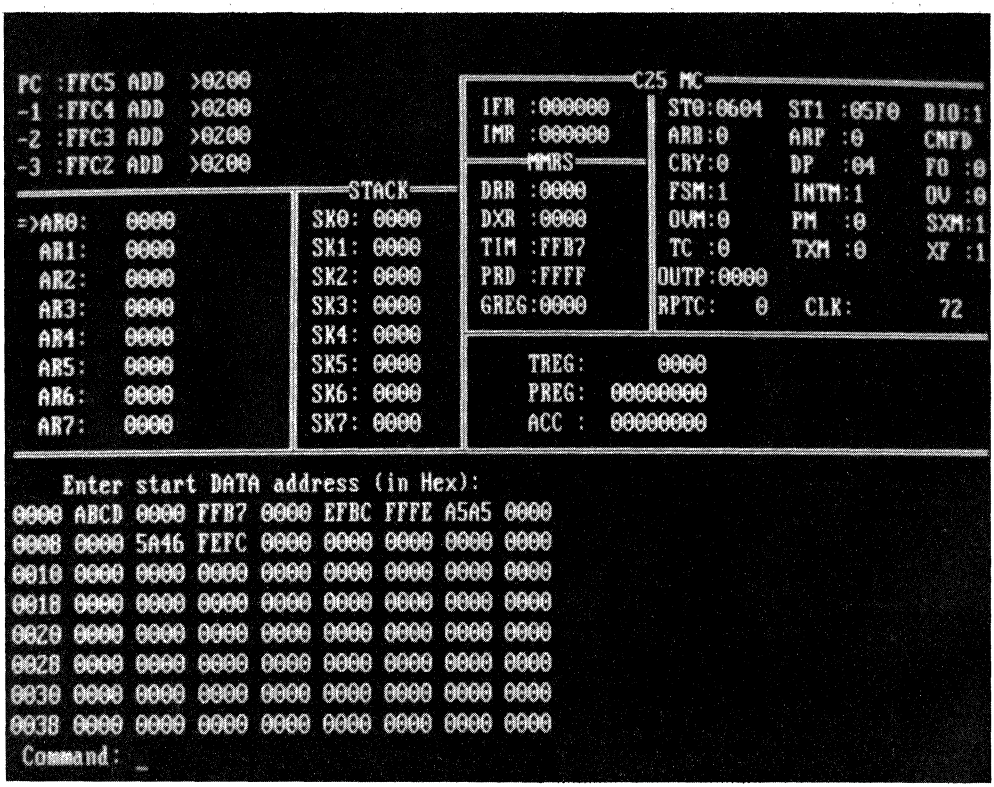

Figure 4-3. TMS320C2x Simulator Screen Example

4.3.3 TMS320C3x Simulator

The TMS320C3x simulator is available for the IBM PC/MS-DOS (5.25" floppy), the VAX/VMS (in Backup format on 1600 bpi magnetic tape), and the VAX/ULTRIX (in TAR format on 1600 bpi magnetic tape) operating systems. Support for the SUN-3/UNIX (in TAR format on 1600 bpi magnetic tape) operating system is available through a TMS320 third party (see Section 9). The PC configuration requires a minimum of 512K-bytes for the TMS320C3x simulator. Table 4-5 lists the commands, broken down by category, for the TMS320C3x simulator. Figure 4-4 shows an example TMS320C3x simulator screen display. These key features highlight simulator flexibility for effective TMS320C3x software development:

- Simulates the entire TMS320C3x digital signal processor instruction set
- Simulates the key TMS320C3x peripheral features (DMA, timers, and serial port)

- Command entry from either menu-driven keystrokes (menu mode) or from a batch file (line mode)
- Help menus for all screen modes
- Standard interface can be user customized
- Simulation parameters quickly stored/retrieved from files to facilitate preparation for individual sessions
- Reverse assembly allows editing and re-assembly of source statements
- Memory can be displayed (at same time) as:
  - Hexadecimal 32-bit values
  - Assembled source
- Execution modes include:
  - Single/multiple instruction count
  - Single/multiple cycle count
  - *until* condition is met
  - *while* condition exists
  - *for* set loop exists
  - Unrestricted run with halt by key input
- Easy to define trace expressions
- Trace execution with display choices of:
  - Designated expression values
  - Cache registers
  - Instruction pipeline for easy optimization of code
- Breakpoint conditions include:
  - Address read
  - Address write
  - Address read or write
  - Address valid
  - Expression valid
- Simulates cache utilization
- Cycle counting:
  - Display the number of clock cycles in single step or run mode
  - External mode can be configured with wait states for accurate cycle counting

The simulator allows verification and monitoring of the state of the processor. Simulation speed is on the order of thousands of instructions per second (VAX VMS, VAX ULTRIX, and SUN-3 UNIX) or hundreds of instructions per second (PC/MS-DOS).

For part number information, refer to Appendix A. Contact the nearest TI Field Sales Office for pricing and availability.

Table 4-5. TMS320C3x Simulator Commands

BREAKPOINT COMMANDS	
Command and Syntax	**Operation Description**
BAA <address>	Breakpoint Add All - Breakpoints occur as if commands BAE, BAR, and BAW are all set using value in <address>.
BAD <address>	Breakpoint at Data read or write - Breakpoint occurs if data is read from or written to <address>.
BAE <address>	Breakpoint at Execution - Breakpoint occurs if execution is to occur at <address>.
BAR <address>	Breakpoint at Read - Breakpoint occurs if <address> is to be read.
BAW <address>	Breakpoint at Write - Breakpoint occurs if data is to be written to <address>.
BAX <exp>	Breakpoint at Expression - Breakpoint occurs if expression found is evaluated as non-zero.
BD <id no.>	Breakpoint Delete - Delete breakpoint number <id no.>.
BL <filename>	Breakpoint Load - Load breakpoints stored in <filename> (e.g., loaded by BS command.
BR	Breakpoint(s) Remove - Remove all breakpoints.
BS <filename>	Breakpoint Save - Save all breakpoints in <filename>.
CONFIGURE MEMORY COMMANDS	
Command and Syntax	**Operation Description**
CC	Configure Colors - Set color, reversing, and blinking for screen fields.
CM	Configure Memory Mode - Enter mode: action defined by nmemonic's final letter and operand(s).
CMA <low addr>,<hi addr>,<wait st>	Configure Memory Add - Define memory from <low addr> to <hi addr> with a number of <wait> states.
CMD	Configure Memory Delete - Delete the memory defined by the id number assigned by the CMA command.
CML	Configure Memory Load - Load the memory configuration stored in <filename> e.g., stored by CMS command).
CMM <1|0>	Configure Memory Mode - Configure memory as set by a 1 or 0 level on the external MC/$\overline{MP}$ pin (1 = micro-computer mode, 0 = microprocessor mode).

Table 4-5. TMS320C3x Simulator Commands (Continued)

CONFIGURE MEMORY COMMANDS (Concluded)	
Command and Syntax	**Operation Description**
CMR	Configure Memory Reset - Reset configured memory to default initialization for RAM, I/O, and ROM.
CMS <filename>	Configure Memory Save - Save memory configuration in <filename>
CONFIGURE PORTS COMMAND	
CP	Configure Port Mode - Action is defined in this mode by command mnemonic's final letter and operand(s).
CPA <type>,<io>,<address>	Configure Port Add - Define port as to <type>,<io>(input or output), and it's location at <address>.
CPD <id no.>	Configure Port Delete - Delete the port defined by an <id no.> assigned by the CPA command.
CPL <filename>	Configure Port Load - Load the port configuration stored in <filename> by the CPA command.
CPR	Configure Port Reset - Deletes all port assignments (initialized state).
CPS <filename>	Configure Port Save - Save port configuration in <filename>.
DISPLAY COMMANDS (Display in lower-left window)	
Command and Syntax	**Operation Description**
DB <start position>	Display Breakpoints - Display breakpoint configuration as set by the breakpoint commands.
DC <start position>	Display Memory Configuration - Display memory configuration as set by the CMA command.
DE	Display Expressions
DF <filename>,<start position>	Display File - Show text file starting at <start position>(line number) of <filename>
DM <address>	Display Memory - Starting at <address>.
DP <start position>	Display Port Configuration - Display port configuration as set by CP command.
DS <start position>	Display Symbols - Show all or start at <start position>(line number).
DT <start position>	Display Trace Configuration - Display trace configuration as set by any of the trace commands.

Table 4-5. TMS320C3x Simulator Commands (Continued)

EXPRESSION COMMANDS	
Command and Syntax	**Operation Description**
EA <EXPR>,[NAME],[RADIX†],[B|W|D‡]	Expression Add - Add expression with optional descriptors.
ED <id no.>	Expression Delete - Delete expression identified by <id no.>.
EF <id no.>,[radix†]	Expression Format - Specify numerical parameters.
EL <filename>	Expression Load - Load from <filename>.
EN <id no.>,<name>	Expression Rename - Change to <name>.
ES	Expression Save - Store in <filename>.
† radix: A=ASCII, B=binary, D=decimal, F=floating point, H=hexidecimal, O=octal DG2. data word: B=byte(8 bit), W=short word (16 bit), D=double word (32 bit)	
JOURNAL COMMANDS	
Command and Syntax	**Operation Description**
JC <filename>	Journal Capture - In Command Mode, saves line commands in <filename> for batch operation.
JE <filename>	Journal Execute - Executes commands stored in <filename> by JC command.
JS	Journal Capture Stop - Halts JC command execution.
LOAD COMMANDS	
Command and Syntax	**Operation Decription**
LB <filename>	Load Breakpoint Configuration - Load from <filename>, the breakpoint configuration saved by SB command.
LC <filename>	Load Memory Configuration - Load from <filename>, the memory configuration saved by SC command.
LE <filename>	Load Expressions - Load from <filename>, the expressions saved by SE command.
LM <filename>	Load Memory Dump - Load <filename> into memory at locations set by SM command.
LO <filename>	Load COFF File - Load the COFF-type file named <filename>.
LP <filename>	Load Port Configuration - Load the port configuration stored in <filename>.
LR <filename>	Load Register Configuration - Load the registers with the configuration stored in <filename>.
LT <filename>	Load Trace Configuration - Load in the trace configuration stored in <filename>.

Table 4-5. TMS320C3x Simulator Commands (Continued)

MEMORY COMMANDS	
Command and Syntax	**Operation Description**
MA <address>,<statement>	Memory Assemble - Show source statement at <address>, also input/assemble new <statement>.
MF <start addr>,<end addr>,<value>	Memory Fill - Fill memory from <start addr> to <end addr> with <value>.
MM <address>,<value>	Memory Modify - Change location<address> to <value>.
OP SYS, QUIT, REGISTER/EXPRESSION COMMANDS	
Command and Syntax	**Operation Description**
O	Escape to Operating System - (Simulator retained in memory).
Q	Quit - Exit to operating system, simulator not retained.
R <register>,<value>	Fill <register> with <value> (could be expression results).
SAVE COMMANDS	
Command and Syntax	**Operation Description**
SB <filename>	Save Breakpoint configuration in <filename>.
SC <filename>	Save Memory configuration in <filename>.
SE	Save Expressions in <filename>.
SM <filename>,<start addr>,<end addr>	Save Memory dump from <start addr> to <end addr>. Save in <filename>.
SP <filename>	Save Port configuration in <filename>.
ST (filename>	Save Trace configuration in <filename>.
TRACE COMMANDS	
Command and Syntax	**Operation Description**
T	Trace Mode - Enter mode. Action defined by mnemonic's final letter and operand(s).
TB	Trace Bottom - Display bottom of trace file.
TD	Trace Disable - Halt collecting trace samples in a trace and close files opened by TE command.
TE <filename>,<expression>	Trace Enable - Enables collecting of trace samples in a trace as long as <expression> is nonzero, and opens <filename> as new file to collect samples.
TF <P | C | col. no.>,<expression>	Trace Format - Trace reportto show results of <expression> in format column specified by <P | C | col. no.>. <expression> not needed for column 0. P = pipeline, C =cache

Table 4-5. TMS320C3x Simulator Commands (Concluded)

TRACE COMMANDS (Concluded)	
Command and Syntax	**Operation Description**
TL <filename>	Trace Load - Load trace configuration saved in <filename>.
TP <sample no.>	Trace Position - Display trace beginning at <sample no.>.
TS <filename>	Trace Save Configuration - Save trace configuration in <filename> (e.g., configuration set by TF command.
TT	Trace Top - Display at top of trace file.
TU <id no.>	Trace Unformatted - Delete <id no.> expression from trace configuration.
TX	Trace Execute - Execute in format specified by operand. This is similat to operands for execute commands.
EXECUTION COMMANDS	
Command and Syntax	**Operation Description**
X	Execute Mode - Enter mode. Action is determined by mnrmonic's final letter operand(s).
XC <cycle count>	Execute Cycle - Execute for <cycle count> instruction cycles.
XF	Execute Function - PC = PC+1. Execute to new PC value (immediate call to subroutine executes through return to call).
XG	Execute Go - Execute beginning at present PC value.
XI <count>	Execute Instruction - Execute one (default) or <count> instructions beginning at present PC value until breakpoint, error, or <ESC> key.
XL <count>	Execute Loop - Repeatedly execute one (default) or <count> of coded loops beginning at present PC value.
XR	Execute Reset - Reset TMS320C30 as if pin $\overline{\text{RESET}}$ asserted.
XU	Execute Until - Execute until <expression> is a TRUE value.
XW	Execute While - Execute while <expression> is a TRUE value.

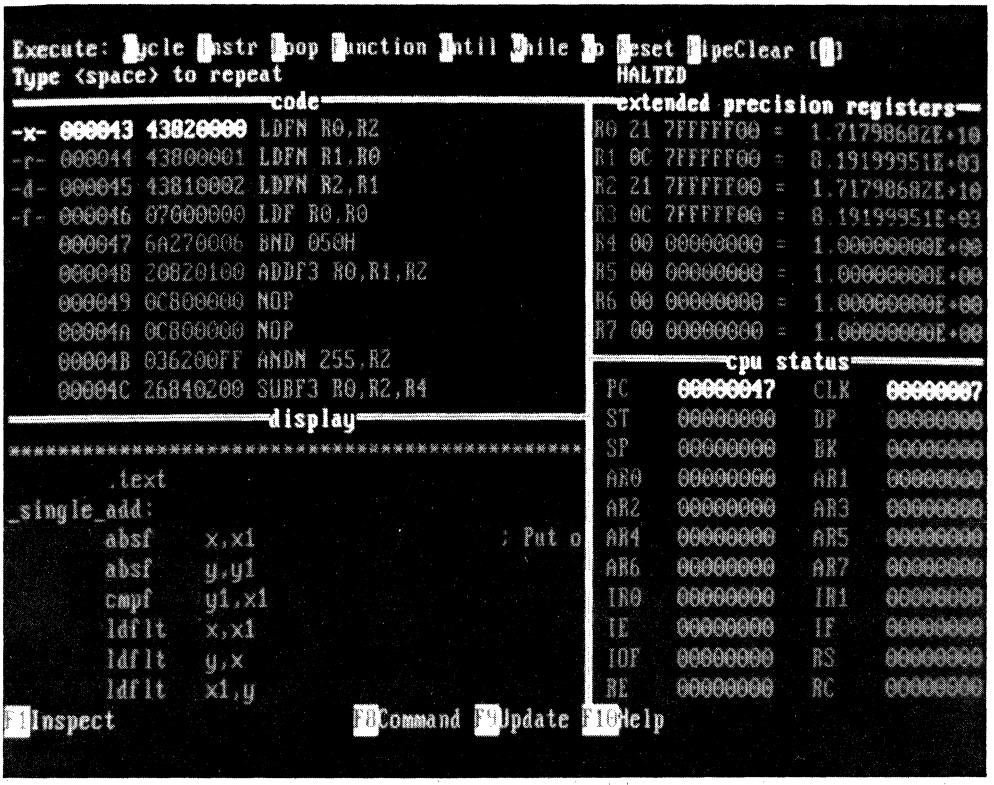

Figure 4-4. TMS320C3x Simulator Screen Example

4.4 SoftWare Development System (SWDS)

The SoftWare Development System (SWDS), shown in Figure 4-5, is a PC-resident tool that provides two functions: software simulation for the TMS320C2x and limited access to target I/O. Figure 4-6 provides an example of the SWDS screen display.

As a software tool, the SWDS allows the user to write, assemble and link, load, and debug the TMS320C2x code on a PC workstation in realtime. The SWDS is capable of single-stepping through code or setting software breakpoints for monitoring register or memory contents during execution. It can also associate files on the PC with I/O ports so that specific I/O values may be used during test and debug.

As a hardware tool, the SWDS provides access to target I/O via a connector cable and 68-pin PGA adapter socket. The SWDS provides single-stepping and software breakpoint capabilities for viewing the registers and the memory contents. It also performs the clocking, signalling, and control for parallel as well as serial port I/O with the target system. Unlike the XDS/22 emulator, the SWDS does not address target memory or allow hardware breakpoint, trace, and timing capabilities. The SWDS does provide the user a cost effective means of evaluation, software development, and limited hardware development.

These key features distinguish the SWDS:

- Window-oriented debugger screen displays machine state, memory, hardware monitor, and reverse assembly of currently executing program
- RAM configurable in software between program and data memory spaces
- 8 breakpoints on instruction acquisition, each with event count (non-realtime)
- Limited connections to target system for I/O operations
- Data logging that allows I/O operations to disk files for fast simulation of DSP algorithms
- Decimal/Hexadecimal conversion calculator
- Debug monitor suspension capabilities to return control to MS-DOS environment

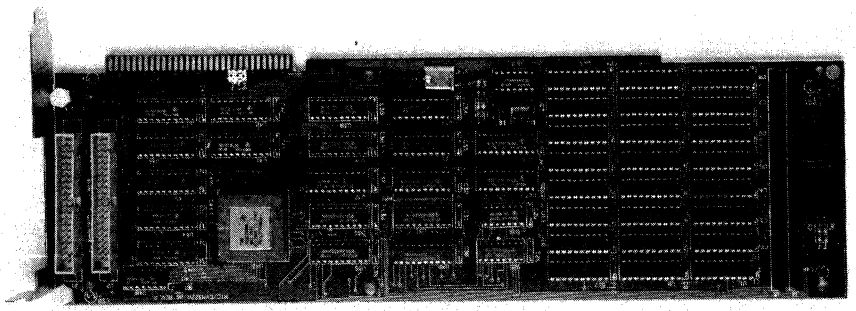

Figure 4-5. SoftWare Development System (SWDS)

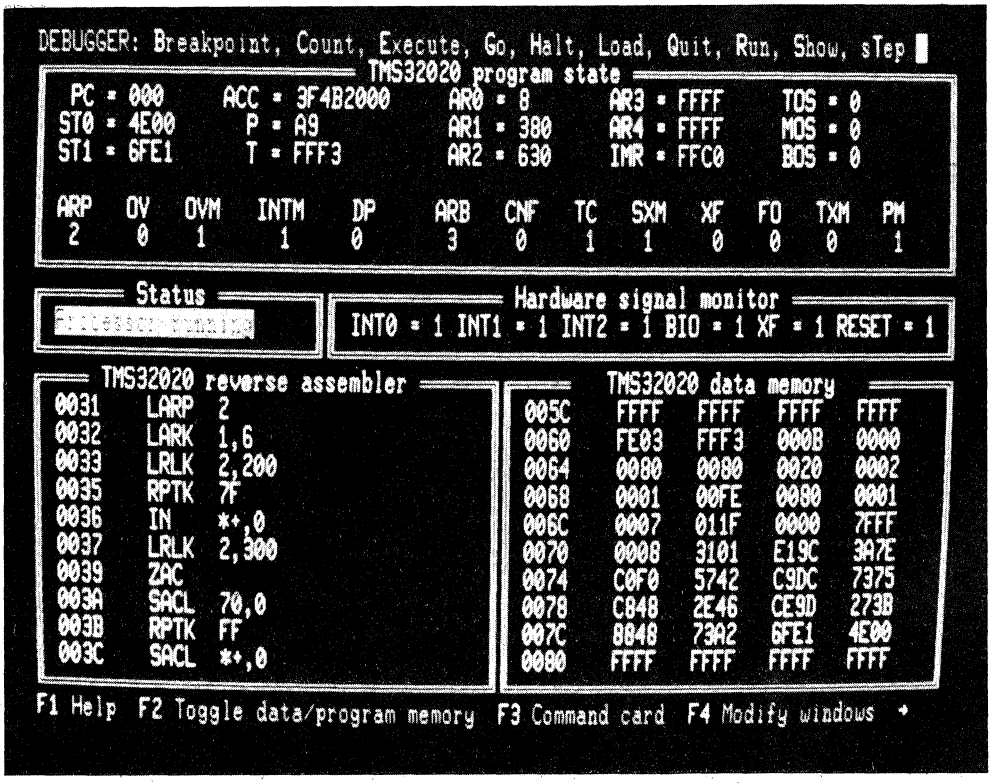

Figure 4-6. SWDS Screen Display

The SWDS Debug Monitor has two modes of operation: command-driven mode and menu-driven mode. The command-driven mode requires a command name at the **CMD>** prompt. A prompt for all parameters is given in the display area of the screen. The previous 10 commands executed are remembered on a command stack. The stack is accessed with the cursor **UP** and **DOWN** keys. The menu-driven mode is entered from command-driven mode function key **F1**. Menu-driven mode opens a window that allows the user to scroll through two lists of commands. The left window contains a list of eight major categories of commands. The right window contains a list of all primary commands grouped according to the major categories. Figure 4-7 lists the primary command name, the secondary command name(s) if any, and provides a brief summary of each command by major command category.

PRIMARY COMMAND NAME	SECONDARY COMMAND NAME	DESCRIPTION
	MS-DOS COMMANDS	
ASM	XASM, XA	Execute assembler
COPY	CF, CC	Copy a MS-DOS file
DIR	LD	Show MS-DOS directory
DOS	-	Exit to MS-DOS. EXIT command returns control to the Debug Monitor
EDIT	XE	Edit an MS-DOS text file
ERASE	DEL, DF, DELETE	Delete MS-DOS file
LINK	XLE	Link object files
PRINT	PF	Send a MS-DOS file to printer
RASM	XRA	Execute reverse assembler
SHOW	SF, TYPE	Show file command
TIME	-	Set MS-DOS time of day
	BREAKPOINT COMMANDS	
AOFF	-	Disable all 8 address breakpoints
AON	-	Enable all 8 breakpoints
BOFF	-	Disable single address breakpoints
BON	-	Enable single address breakpoint
CAB	CASB	Clear all software address breakpoints
CB	CBP, CSB	Clear software address breakpoint
DBP	DB, DSB	Display address breakpoints
MBP	BB, BPM	Modify address breakpoints
SB	SSB, CSB	Set software address breakpoint/event counter
	MEMORY DISPLAY/MODIFY COMMANDS	
CDM	-	Compare two different blocks of data memory
CPM	-	Compare two different blocks of program memory
DDM	-	Display data memory locations
DLOAD	-	Load object code from disk to data memory
DPM	-	Display program memory locations
DSAVE	-	Store data memory object code in disk file
FDM	-	Fill data memory with specified value
FPM	-	Fill program memory with specified value
FWDM	-	Find word in data memory
FWPM	-	Find word in program memory
LOAD	DL, PLOAD	Load object program disk file into program memory
MDM	IDM	Modify data memory locations
MPM	IPM	Modify program memory locations
MVD	-	Move block of data memory from one part memory to another
MVP	-	Move block of program memory from one part of memory to another
PDM	-	Send data memory locations to printer
PPM	-	Send program memory locations to printer
SAVE	UL, PSAVE	Save program memory object file to disk file

Figure 4-7. SWDS Commands Breakdown

PRIMARY COMMAND NAME	SECONDARY COMMAND NAME	DESCRIPTION
REGISTER DISPLAY/MODIFY COMMANDS		
ACC	A	Modify accumulator
AR0	–	Modify register AR0
AR1	–	Modify register AR1
AR2	–	Modify register AR2
AR3	–	Modify register AR3
AR4	–	Modify register AR4
AR5	–	Modify register AR5 (TMS320C25 only)
AR6	–	Modify register AR6 (TMS320C25 only)
AR7	–	Modify register AR7 (TMS320C25 only)
ARB	–	Modify auxiliary register buffer pointer (ST1)
ARP	–	Modify auxiliary register pointer (ST0)
BOS	–	Modify stack location (TMS32020 only)
C	–	Modify carry bit in ST1 (TMS320C25 only)
CNF	–	Modify configurations control bit in ST1
DP	–	Modify data page pointer in ST0
DRR	–	Modify data receive pointer
DXR	–	Modify data transmit register
FO	–	Modify format bit in ST1
FSM	–	Modify frame synchronization bit in ST1 (TMS320C25 only)
GREG	–	Modify global memory register (0 to FF hexadecimal)
HM	–	Modify hold bit in ST1
IMR	–	Modify interrupt mask register (TMS32020 only)
INTM	–	Modify interrupt mode in ST1
MOS	–	Modify stack locations (TMS32020 only)
OV	–	Modify overflow flag in ST0
OVM	–	Modify overflow mode in ST0
PC	–	Modify program counter (0 to FFFF hexadecimal)
PM	–	Modify product shift mode in ST1
PRD	–	Modify period register (0 to FFFF hexadecimal)
PREG	–	Modify product register (0 to FFFFFFFF hexadecimal)
REGS	REG,MR,IR	Gisplay modify registers
S1	–	Modify stack location (TMS320C25 only)
S2	–	Modify stack location
S3	–	Modify stack location
S4	–	Modify stack location
S5	–	Modify stack location
S6	–	Modify stack location
S7	–	Modify stack location
ST0	ST	Modify status register 0 (ST0)
ST1	–	Modify status register 1 (ST1)
SXM	–	Modify sign extension mode ST1
T	TREG	Modify T register
TC	–	Modify test/control bit in ST1
TIM	–	Modify timer register
TOS	–	Modify stack location (TMS32020 only)
TXM	–	Modify transmit mode control bit in ST1
XF	–	Modify XF pin status in ST1

Figure 4-7. SWDS Commands Breakdown (Continued)

PRIMARY COMMAND NAME	SECONDARY COMMAND NAME	DESCRIPTION
INPUT/OUTPUT PORT COMMANDS		
IN	DIO	Read from specified input port (0-9, A-F)
OUT	MIO	Write to specified output port (0-9, A-F)
PORTS	IO	Display I/O ports
PROCESSOR STATE COMMANDS		
CPS	CLEAR	Clear processor state
DEBUG	SS,RUN,SRR, EX	Execute debugger
DPS	STATE,DR	Display processor state
HALT	–	Halt program
INIT	–	Initialize parameters
RUN	–	Start execution of program
SRR	–	Software reset and run a program
SS	–	Execute single instruction
SIMULATOR COMMANDS		
LI	LO,LOG	List simulator input files in data logging mode
LO	–	List simulator output files in data logging mode
LOG	SIM	Enable data logging mode
RSI	–	Reset selected input port file
RSO	–	Reset selected output port file
SI	–	Select input port file
SO	–	Select output port file
UNLOG	UNSIM	Disable data logging mode
MISCELLANEOUS COMMANDS		
BELL	–	Enable/disable PC warning bell
CALL	–	Enable DEC/HEX calculator
CLS	–	Clear display window, area, and screen
COLOR	–	Redefine screen attributes
ID	–	Display revision level of debug monitor software
QUIT	SYSTEM	Return to MS-DOS
SEGMENT	–	Display/modify memory segment in PC memory address space
SETUP	–	Initialize pathnames
TEST	–	Enter test in progress message
USER	–	Executes user pathname specified in the SETUP command (e.g., object format converter DSPOROM.EXE -t)

Figure 4-7. SWDS Commands Breakdown (Concluded)

The SWDS comes complete with the following:

1) A circuit board containing the TMS320C2x device plus program and data memory.

2) Two small cable adapter boards which are connected to the SWDS via two 40-connector ribbon cables. The cable adapter boards included with the system are:

   a) The PGA Adapter Connector that connects the SWDS to a TMS320C2x target system via a 68-pin grid array footprint. This adapter provides connection directly to the AIB2.
   b) The Analog Interface Board 1 (AIB1) Adapter Connector that connects the SWDS directly to the TMS320 AIB1.

3) Software which includes the TMS320C2x Assembler/Linker, the DSP Software Library, and the SWDS monitor software. All appropriate documentation is included.

The SWDS is configured for TMS320C25 development running full-speed at 40 MHz upon shipment. A TMS32020 and a 20 MHz crystal are included with the system to accommodate TMS32020 development. The target system may supply a TTL clock source, in which case the upper limit of the clock speed is dictated by the speed of the processor on the PC board. If the user's target system provides a clock source, the use of the external clock is specified in the debug monitor initialization command and the target system's clock is connected to the SWDS.

The SWDS is currently available for the PC/MS-DOS operating environment and requires 348K-bytes of RAM. For part number information, refer to Appendix A. For more information on pricing and availability, contact the nearest TI Field Sales Office.

4.5 Digital Filter Design Package (DFDP)

The Digital Filter Design Package (DFDP) developed by Atlanta Signal Processors, Inc. (ASPI) is a user-friendly, menu-driven software package intended to speed design of digital filters with floating-point accuracy or fixed-point economy in a variety of filter structures.

The package consists of four interactive filter design modules capable of performing the following functions:

1) Designing FIR filters (Kaiser window)
2) Designing FIR filters (Parks-McClellan)
3) Designing IIR filters (Butterworth, Chebychev I and II, and elliptic)
4) Generating TMS320 assembly code by converting the ASCII file containing the filter coefficients into fully commented assembly language code for all generations of the TMS320 family.

Cascade and parallel structures as well as higher-performance lattice, normalized lattice, and orthogonal forms are included in the modules.

The DFDP can design filters to meet any piecewise linear response specification, evaluate filter characteristics before and after coefficient quantization, and design special-purpose FIR filters, such as multiband filters, differentiators, Hilbert transformers, and raised-cosine filters. The DFDP can also generate coefficients for filter implementations on any general-purpose processor or signal processing chip, as well as fully commented assembly language code for a variety of DSP chips. Magnitude, log magnitude, and impulse responses can be plotted for printer or screen display (see Figure 4-8); in addition, the phase, group delay, and pole-zero map can be plotted for IIR filters.

The DFDP design modules present menus and queries so that the designer can specify the type of filter, sampling frequency, and filter cutoff frequencies and attenuation requirements. The program estimates the required filter order or impulse response length and asks the user to select the filter length to be used. The program then attempts to calculate the coefficients; using these coefficients, it calculates the response characteristics of the realizable filter. A screen message may warn that specifications are unrealizable or that the designed filter does not meet specifications.

If the designed filter does not meet specifications, the user may examine the table of poles and zeros or impulse response coefficients of the filter generated by the program as well as the frequency response plots. The user may also examine the response over the full relevant spectrum (zero to one-half the sampling frequency) or over any narrower frequency limits chosen. Amplitude is automatically scaled within such a frequency band in order to utilize the full height of the graph. Every plot, whether of the full relevant spectrum or the expansion of a narrower band, is displayed on the monitor and may also be directed to the printer.

After the filter is designed, the user can generate code associated with the filter using the CGEN design module. The generated assembly language code is fully operational for all generations of the TMS320 family.

The DFDP runs on the IBM PS/2, IBM PC/XT/AT, and compatible systems. Operating systems must have 512K-bytes of memory available. For part number information, see Appendix A. For product information and availability,

contact the nearest TI Field Sales office or Atlanta Signal Processors, Inc. (refer to Section 9 for address and phone number).

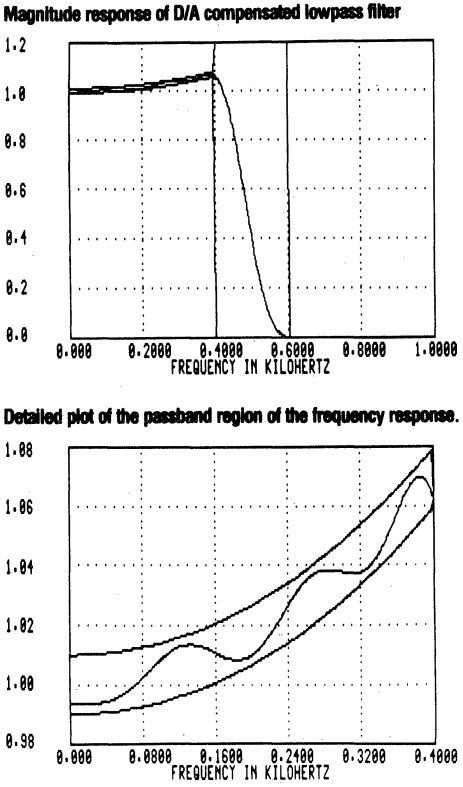

Figure 4-8. DFDP Plot Examples

4.6 Digital Signal Processing Software Library

The Digital Signal Processing Software Library contains the major DSP routines (FFT, FIR/IIR filtering, and floating-point operations) and application algorithms (echo cancellation, ADPCM, and DTMF coding/decoding) presented in the book, *Digital Signal Processing Applications with the TMS320 Family Volume 1* (SPRA012A). These routines and algorithms are written in either TMS320C1x and/or TMS320C2x source code. In addition, macros for the TMS320C1x are included in the library.

The software package consists of four diskettes for use with the IBM PC/MS-DOS (version 1.1 or later) or a 1600 bpi magnetic tape for the VAX(VMS) version. For the PC/MS-DOS version, Table 4-6 briefly describes the contents of each diskette. All the directories listed are contained on the magnetic tape for the VMS version. Each directory contains a README.LIS file briefly describing the contents of the files in the directory and the reference to the code. The book, *Digital Signal Processing Applications with the TMS320 Family, Volume 1,* is the major reference for the theory and algorithms, and also provides printed code in the appendices of each application report. Table 4-6 indicates the section in the applications book where the user can find the theory behind the source code.

All the software in the library is copyrighted by Texas Instruments (see Appendix C for the Program License Agreement). The library is continually being updated; therefore, check the TMS320 DSP Bulletin Board (see Section 7.7) for update information.

For part number information, refer to Appendix A. Contact the nearest TI Field Sales Office for pricing and availability.

Table 4-6. Software Library Contents

DISK #	DIRECTORY	# OF FILES†	DESCRIPTION	APP. BK. SECTION
1	README.LIS	1	Description of product	
	INSTALL.BAT	1	S/W installation procedures	
	LOAD.BAT	1	Loading S/W onto hard disk	
	FFT32010.DIR	10	FFT routines in TMS320C1x (source) code (from Burrus and Parks' *DFT/FFT and Convolution Algorithms*)	
	FFT32020.DIR	10	FFT routines in TMS320C2x(source) code	4
2	ADPCMCCI.DIR	9	CCITT-compatible ADPCM code in TMS320C1x	17
	ADPCMNON.DIR	5	Non-CCITT ADPCM code in TMS320C1x	17
	COMPND10.DIR	5	Companding routines in TMS320C1x	5
	COMPND20.DIR	4	Companding routines in TMS320C2x	5
	COMPNDHW.DIR	3	FORTRAN programs to generate companding tables for implementing companding in hardware	14
	DTMF10.DIR	4	Single-channel DTMF code in TMS320C1x	19
	ECHO128.DIR	2	16-ms echo cancellation code in TMS320C2x	15
	FIR-IIR.DIR	7	FIR/IIR filter code in TMS320C1x/C2x	3
	GRAPHICS.DIR	20	Graphics routines in TMS320C2x	23
3	FLTGPT10.DIR	3	Floating-point routines in TMS320C1x	6
	FLTGPT20.DIR	4	Floating-point routines in TMS320C2x	7
	MACROS.DIR	60	TMS320C1x Macros	
	MATRIX.DIR	3	Matrix multiplication routines in TMS320C1x/C2x	9
4	ADPTVFLT.DIR	2	Adaptive filter routine in TMS320C2x	
	DATAIO.DIR	2	Conversion routines from TMS320/ 9900/7000 code into binary format	
	MACROSRC.DIR	37	More TMS320C1x macros	

†Total: 4 disks, 18 directories, 191 files.

4.7 TMS320 Bell 212A Modem Software

Texas Instruments offers a software package containing source code and documentation for the design and implementation of a 1200-bps Bell 212A modem with the TMS320C17 digital signal processor and the TMS7041 microcontroller.

The documentation included in the package consists of two reports. One report discusses in detail the theory behind the design of the modem, as well as the functions implemented. The second report describes the hardware, algorithms, and coding techniques used in the implementation of a Bell 212A modem demonstration unit. This implementation has been built and tested to verify its operation. After reading this report, the user should be able to design and build a similar unit as well as understand some tradeoffs involved in making custom modifications.

The source code for the TMS320 Bell 212A Modem Software package is provided on a 5 1/4" floppy for PC/MS-DOS or compatible operating systems. For part number information, refer to Appendix A. Contact the nearest TI Field Sales Office for pricing and availability.

4.8 Data Encryption Standard Software

The Data Encryption Standard Software is the algorithm of data encryption selected by the United States federal government. It is available for implementation on the TMS320 family of digital signal processors. The encryption scheme operates on a stream of bits that represents text, computer files, or anything else presented in binary form. This encryption method, when used with speech coding, is considered to give secure communication over voice channels. Another example of Data Encryption Standard Software usage is the encryption of data supplied to a transmitting modem and decryption of the corresponding data stream coming out of the receiving modem.

There are restrictions related to the purchase of this algorithm. The following statement of restrictions concern the purchase and continue to apply after purchase:

Only United States of America owned and operated companies may purchase this code. Export of cryptographic devices and software is controlled under title 22 USC part 121 et seq by the U.S. Department of State, Office of Munitions Control (OMC).

The OMC can be contacted regarding exporting of any cryptographic commodity at the following address:

Office of Munitions Control
Bureau of Politico-Military Affairs
Department of State
Washinton, DC 20520

For more information, contact the National Bureau of Standards. For part number information, refer to Appendix A. For information on pricing and availability of the Data Encryption Standard Software for the TMS320 family, contact the nearest TI Field Sales Office.

4.9 SPOX: The TMS320C3x Operating System

SPOX is the industry's first realtime DSP operating system. The SPOX operating system is a powerful software tool developed by Spectron Microsysyems Inc. that provides a hardware-independent software base for realtime DSP applications. SPOX features a set of high-level C-callable software functions which are independent of the underlying hardware platform, thus insulating realtime DSP applications from many low-level system details. The SPOX operating system plays an integral role in application development, from concept of new algorithms to integration of application software onto production hardware.

SPOX differs from other operating systems in that it's capabilities are 'application-specific', augmenting high-level programming languages like C with functional components targeted especially for realtime DSP. Provided with SPOX is an extensible DSP math package, configurable hierarchical memory management capabilities, device-independent stream I/O, and a multi-tasking kernel. SPOX affords it's users two important benefits: software productivity and application portability.

Software productivity is achieved by providing application developers with a set of high-level software primitives that comprise a "virtual DSP machine". The instruction set of this conceptual machine, invoked through system calls to SPOX, parallel the capabilities of the TMS320C3x by means of a collection of high-level functions targeted especially for realtime DSP applications. At the same time, the system call interface provided by SPOX effectively shields realtime DSP application software from many details of the underlying physical hardware.

Other operating systems or realtime kernels (such as Unix) may insulate application software from underlying hardware through a high-level interface. SPOX differs from these products in much the same way as the TMS320C3x device differs from a general-purpose microprocessor. Both SPOX and the TMS320C3x device are *application-specific* system components that uniquely address the needs of realtime DSP through a collection of specialized functions used in conjunction with more generic capabilities.

The SPOX "virtual DSP machine" is equally important in achieving application portability. The same set of system calls (or instructions) currently implemented for the TMS320C3x will be available for future DSP microprocessors. Applications developed today using the SPOX software interface will track microprocessor technology and migrate easily onto the hardware of tomorrow.

SPOX also provides software portability between different hardware platforms incorporating the TMS320C3x processor. Recognizing that most realtime DSP software executes on custom hardware designed for specific applications, SPOX has been designed to handle each platforms unique memory and peripheral requirements. Packaged as a set of *generic software components*, SPOX can be easily reconfigured and integrated into production DSP systems by application developers.

4.9.1 Functional Components

The "virtual DSP machine" accessed via the SPOX software interface consists of four functional components:

1) *DSP Math*, which furnishes application software with a rich set of operations used for manipulating vectors, matrices, and filters

2) *Memory Management*, which gives the application explicit control in allocating data storage from different segments of system memory

3) *Stream I/O*, which presents a device-independent application interface used to input and output blocks of data from a variety of peripherals

4) *Realtime Kernel*, which provides primitives for scheduling and synchronizing multiple priortized tasks

The components of SPOX augment a standard programming language such as C with a set of functions targeted specifically towards realtime DSP applications. At the same time, SPOX insulates the application from some aspect of the underlying hardware platform. Figure 4-9 illustrates the functional components of SPOX.

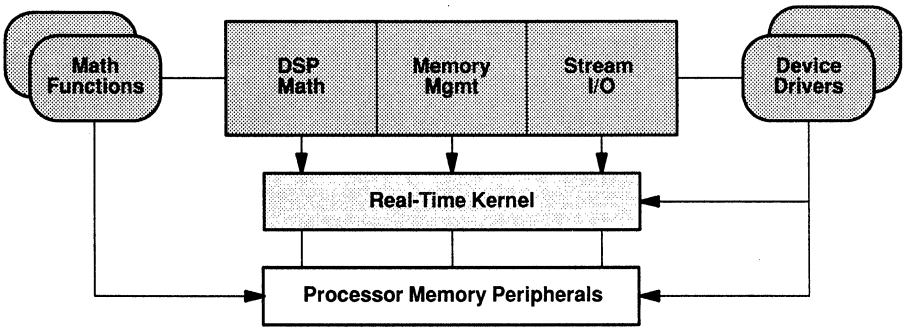

Figure 4-9. Internal SPOX Architecture

The DSP math component provides a set of high-level math functions (such as dot product or FFT) that encapsulate many of the DSP-specific capabilities

of the underlying TMS320C3x processor. The stream I/O component incorporates device drivers that manage hardware peripherals (such as an A/D converter) in conjunction with the realtime kernel. Since each DSP application has a unique set of requirements for computation and I/O, developers can integrate application-specific math functions and device drivers with the generic portions of SPOX. The SPOX memory management component can be configured to represent the different segments of physical memory actually present in the system.

4.9.2 SPOX Development Support

The SPOX software interface is supported in different execution environments, including Sun workstations, IBM personal computers, and VAX minicomputers. On these host systems, DSP application programs written in high-level languages such as C can be developed and debugged in familiar software engineering environments equipped with powerful tools and utilities. Afterward, these same programs can be recompiled with the TMS320C3x C compiler available for these same hosts, then benchmarked on the TMS320C3x software simulator for time and space using a version of SPOX designed specifically for use with the TMS320C3x simulator. By adhering to this methodology, users can easily write, debug, and benchmark complete DSP application programs without ever seeing production hardware. This same software, because of SPOX, will just as easily execute in realtime on a number of target TMS320C3x platforms.

Spectron supports a family of products known as the SPOX Development Package. This package allows TMS320C3x users to begin application development. This product package (available initially for Sun workstations and IBM PCs) includes support for SPOX execution on the host computer and TMS320C3x simulator, as well as a version of SPOX "ported" to an accompanying target board. This product also allows developers to integrate their own (assembly-language) math functions with the other components of SPOX.

Spectron also offers a SPOX Porting Kit. This product includes an "unbundled" version of SPOX whose generic components can be configured for the specific TMS320C3x application and integrated with system-dependent software (drivers, math functions, etc.) supplied by the developer. This product also contains a primer on writing SPOX device drivers, full documentation of the realtime kernels multi-tasking primitives, and source code for sample drivers.

SPOX is currently packaged with the TMS320C3x XDS1000 Development Environment (refer to Section 5). For more information regarding SPOX, contact Spectron Microsystems at (805) 967-0503 or call:

TI CUSTOMER RESPONSE CENTER (CRC) (800) 232-3200 X3510

request literature number **SPRT072.**

Section 5

Hardware Development Tools

The hardware development support tools for the TMS320 family of digital signal processors include the Evaluation Module (EVM), Emulator (XDS Extended Development Support System), and Analog Interface Board (AIB). These tools are described in the sections listed below.

- TMS320C1x Evaluation Module (EVM) (Section 5.1 on page 5-2)
- TMS320 Emulator (XDS) (Section 5.2 on page 5-8)
- TMS320 XDS Upgrade Package (Section 5.3 on page 5-34)
- TMS320 Analog Interface Board (AIB) (Section 5.4 on page 5-38)

5.1 TMS320C1x Evaluation Module (EVM)

The TMS320C1x Evaluation Module (EVM) is a stand alone low-cost development board used for full-speed in-circuit emulation and hardware debugging. The EVM consists of a single board that enables designers to evaluate certain characteristics of the TMS320C1x processor to determine if it meets the requirements of an application.

The powerful firmware package of the TMS320C1x EVM contains a debug monitor, assembler/reverse assembler, text editor, and PROM utility. The EVM can stand alone as a development system, using the on-board editor for creation of TMS320C1x assembly language test files, and the audio cassette tape interface (with a limited directory and file search capability) as a mass storage media. The EVM can also accept files from a host CPU through one of two RS-232C ports. In either situation, the resident assembler will convert the incoming text into executable code in one pass, resolving labels after assembly is complete.

The EVM firmware supports three ports for data (text and object code) input and output operations for purposes of storage and/or display. Two ports conform to RS-232C specifications and are called Port 1 and Port 2. The third port, Port 3, is an audio tape connection. The ports function as follows:

Port 1: User terminal

Port 2: Host CPU uplink/downlink or line printer connection

Port 3: Audio tape

The EVM supports the following first generation TMS320 DSP devices: TMS32010, TMS320C10, and TMS320C15/E15. These key features distinguish the TMS320C1x EVM.

- 20-MHz operation
- Event counter for one breakpoint
- Text editor
- On-board EPROM programmer
- Audio cassette interface
- 4K words of on-board program RAM
- Target connector for full-speed in-circuit emulation from EVM memory
- Debug monitor including commands with full prompting
- Line-by-line assembler/reverse assembler
- Transparency mode for host CPU upload/download
- Eight instruction breakpoints available
- Single-step execution with software trace
- Standalone or host CPU configurable.

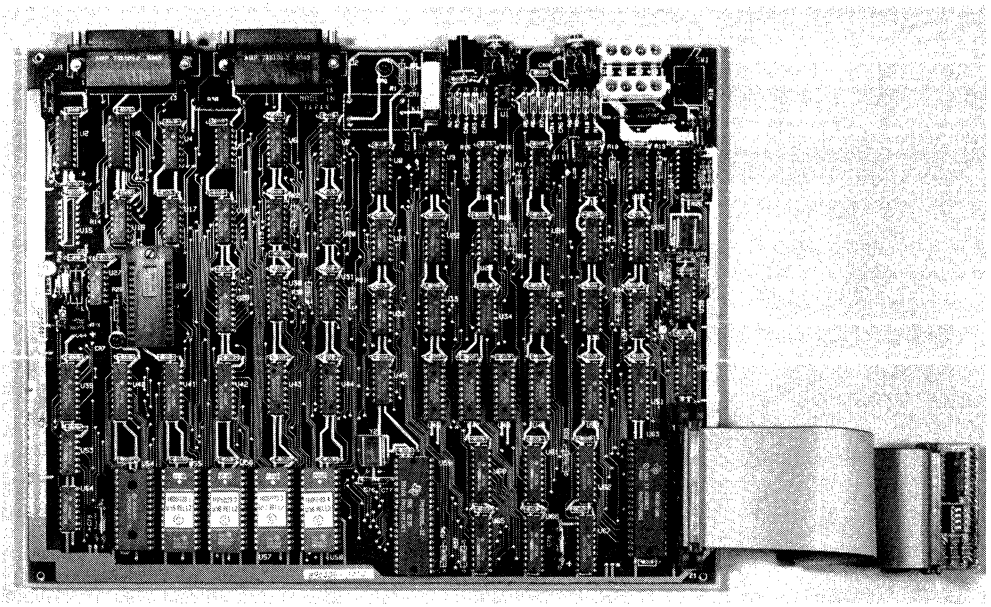

Figure 5-1. TMS320C1x Evaluation Module (EVM)

5.1.1 EVM System Configuration

The TMS320C1x EVM functions in two modes: host computer mode or PC mode (single-user system). In the host computer mode, object and source code can be uploaded/downloaded between the host computer and EVM, as shown in Figure 5-2.

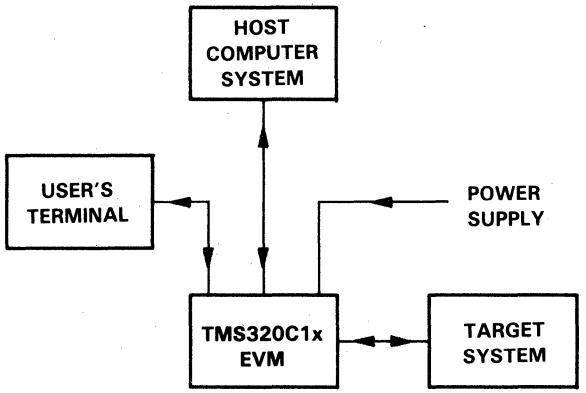

Figure 5-2. TMS320C1x EVM Host Computer Mode

In the PC mode, the TMS320C1x EVM can support host uploads/downloads over a single port to allow a single-user system, such as a IBM PC or compatible, to function as both a terminal and a host (see Figure 5-3). Terminal emulation software for the single-user system is required in this configuration. Communications software packages are commercially available, which allow an IBM PC or compatible to function as both a terminal and a host for the EVM.

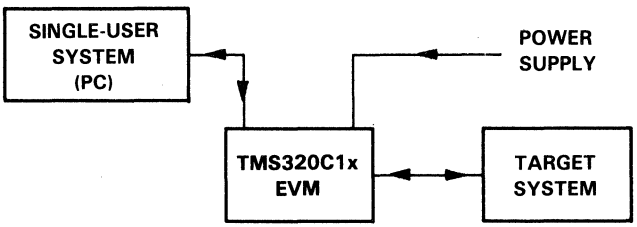

Figure 5-3. TMS320C1x EVM Single-User System

In addition, the TMS320C1x EVM can be configured as a standalone system with an interface to an audio cassette or EPROM to provide mass storage, as shown in Figure 5-4. However, the audio cassette device has limited directory and file search capabilities.

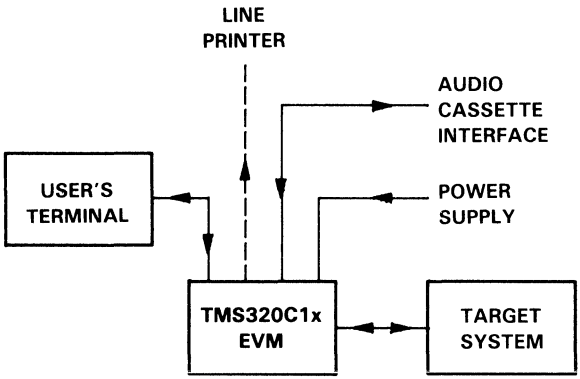

Figure 5-4. TMS320C1x EVM with Audio Cassette Interface

5.1.2 EVM Communication

The TMS320C1x EVM supports baud rates of 110, 300, 600, 1200, 4800, 9600, and 19200 bps. The baud rate of port 1 (terminal) is determined automatically at powerup. The baud rate of port 2 (host or printer) on the TMS320C1x EVM defaults to 9600 bps at reset, and baud rates of either ports 1 or 2 may be altered through monitor commands.

The transparency mode provides a means of communication between a host (a system connected to the EVM through port 2) and the EVM downlink software by allowing the user to logon to a host CPU and the EVM from one terminal. This mode allows the EVM terminal (connected through port 1) to emulate a host terminal and simulate the host to upload/download file to/from the EVM.

The TMS320C1x EVM supports three ports for communication with a designer's terminal, a host computer, a printing device, or audio cassette. In addition, the EVM also supports an onboard PROM utility for programming TMS27C64 EPROMs. TMS320 EPROM products may be programmed by using available EPROM adapter sockets. See Appendix F for more details. This utility programs an EPROM with the contents of memory, compares the contents of the EPROM to memory to verify the copy, reads the EPROM contents into memory, and verifies the EPROM has been erased. EPROMs are used for mass program storage.

The TMS320C1x EVM provides a text editor with line numbering and general editing features. This editor builds assembly language source files as well as general text files. TMS320 source code, object code, or the machine state may be uploaded/downloaded to the EVM from the terminal, host computer, or audio tape. (The machine state consists of the current contents of all the reg-

isters in the TMS320 and of a selected block of program memory.) When interfacing with an audio tape, the TMS320 prompts for a filename.

5.1.3 EVM Debugging

The following components of the TMS320C1x EVM firmware provide flexibility in evaluating TMS320 applications:

- Assembler/reverse assembler/patch assembler
- Debug monitor
- Text editor

The TMS320C1x EVM assembles source code created on a host computer or text editor. The EVM has a one-pass assembler, which resolves both forward and reverse labels and converts the incoming text into executable code. The TMS320C1x EVM does not support macro definitions or relocatable code, and is most suitable for benchmarking of critical segments of code in evaluating TMS320C1x performance. If macro capabilities are desired, the TMS320 assembler/linker can be used.

Object code produced by the TMS320C1x EVM assembler is stored in memory. The reverse assembler converts object code back to TMS320 assembly language mnemonics, and the patch assembler allows modification of the code. Source can be assembled line-by-line.

The TMS320C1x EVM's debug monitor has full prompting and contains commands with the following capabilities:

- Execution of assembler/reverse assembler
- Modification and display of memory
- Software breakpoint manipulation
- Software trace of up to six registers or memory locations
- Realtime code execution
- Single-step execution
- Decimal/hexadecimal number representation
- Scaling of numbers
- Commands for communication
- Execution of text editor and EPROM programmer
- Execution of command strings.

The TMS320C1x EVM's text editor is a line-numbered editor with character-editing capabilities. Assembly language source files can be written using the editor, then output to a host or audio tape, and finally re-input and assembled.

5.1.4 EVM Equipment List

The following equipment is required to use the TMS320C1x EVM:

Power Supply	+5 V @ 3 A -12 V @ 0.1 A +12 V @ 0.1 A
Terminal RS-232-C compatible	25-pin RS-232-C male plug, type DB25P
Cables	
For terminal/host or printer	Two standard RS-232-C cables with male connectors on the EVM end
For audio tape	Two standard mini-to-mini cables and one sub-mini-to-sub-mini cable
For power supply	Standard cable with four-prong male connector for EVM end
Audio Tape Recorder (optional)	Radio Shack CTR-71 or equivalent

5.2 TMS320 Emulator (XDS) Overview

Texas Instruments offers a complete line of development tools for hardware system design and hardware/software integration in the debug stage of system development. The TMS320 Emulator or Extended Development System (XDS) provides all the features necessary for full-speed in-circuit emulation. There are currently three models of the XDS available: the XDS/22 (used for the TMS320C1x and TMS320C2x) and the XDS500 and XDS1000 (used for the TMS320C3x).

The TMS320C1x or TMS320C2x XDS/22 is a self-contained emulator that provides hardware development support for a first- or second-generation TMS320 DSP device. This emulator provides full-speed target RAM for program memory. Sequential hardware breakpoints, full-speed trace, time-stamping capabilities, single-step execution, modification of I/O ports, memory, or registers, plus a reverse assembler,greatly enhance the XDS/22's debugging capabilities.

The TMS320C3x XDS500 Emulator is a user friendly, PC-based system that supports hardware development on the third-generation TMS320 DSP device family. This emulator provides a means for the designer to develop the software and hardware within a target system. Access is provided to every memory location and register of the TMS320C3x through the use of a revolutionary 4-wire interface. The XDS500 Emulator Board is responsible for interpreting commands and converting these commands into the appropriate signal sequences necessary to control the TMS320C3x in the user's target system.

The TMS320C3x XDS1000 Development Environment provides all the development tools necessary to bring the user from the beginning stages of development through full production. The XDS1000 consists of two full-size PC-XT/AT boards. The first is the XDS500 Emulator Board described in the previous paragraph. The second is the TMS320C3x Application Board. The Application Board is a predefined target board intended for high/low level software development in realtime plus hardware/software application support.

5.2.1 XDS/22

There are currently four different versions of the XDS/22; three for TMS320C1x and one for TMS320C2x. The individual version differences will be covered later in this section. There are many similarities between the four versions. These will be covered in the four following subsections.

5.2.1.1 TMS320 XDS/22 System Configurations

The XDS/22 can be configured to operate in one of four modes:

- Stand-alone mode
- Host computer mode
- PC mode (single-user system)
- Multiprocessor mode.

The standalone mode or minimal configuration requires only the XDS/22 and the user's terminal. However, the XDS/22 is best used with a host computer (see Figure 5-5), where TMS320 programs can be written on a familiar editor and then downloaded to the XDS/22. Once a debugging session is complete, TMS320 code can be uploaded to the host computer for storage.

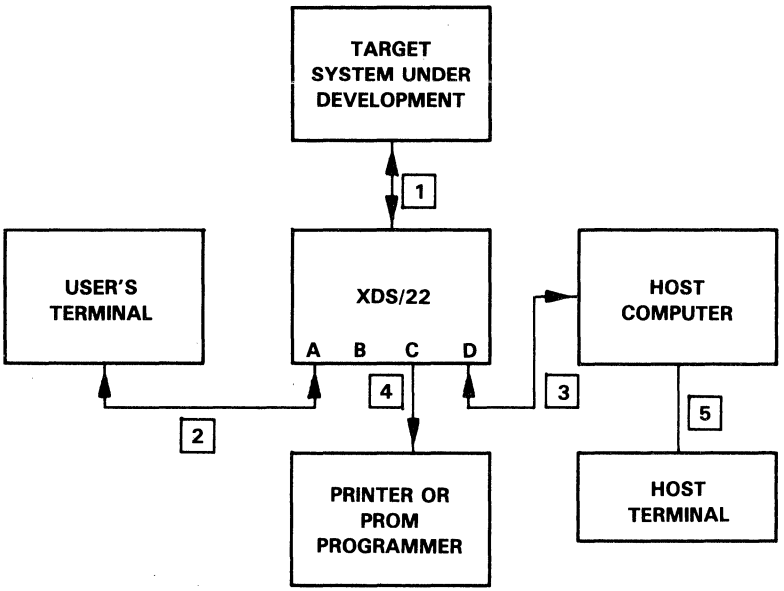

Figure 5-5. TMS320 XDS/22 Host Computer Mode

In the PC mode, the TMS320 XDS/22 can support host uploads/downloads over a single port to allow a single-user system, such as a IBM PC or compatible, to function as both a terminal and a host when connected to the XDS (see Figure 5-6). Terminal emulation software for the single-user system is required in this configuration. Communications software packages are commercially available, which allow an IBM PC or compatible to function as both a terminal and a host for the XDS/22.

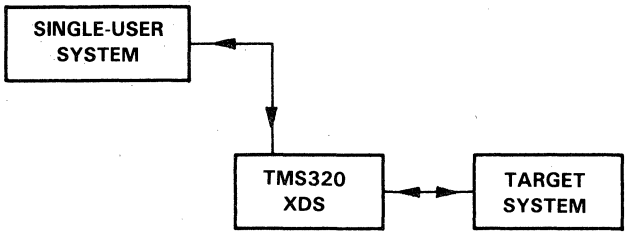

Figure 5-6. TMS320 XDS/22 Single-User System

The emulator's multiprocessor mode allows up to nine XDS/22s to be connected together in a daisy-chain fashion and controlled by a single terminal, as shown in Figure 5-7. A single host computer can also be connected.

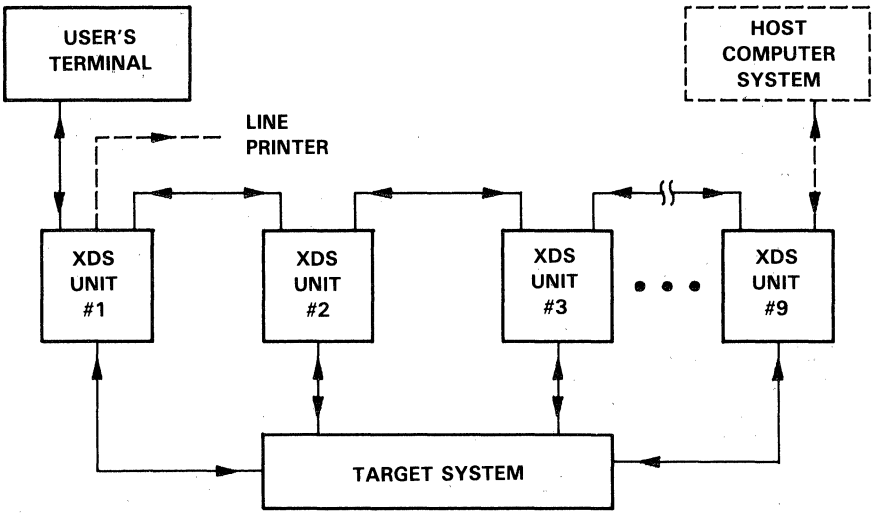

Figure 5-7. TMS320 XDS/22 Multiprocessor Mode

5.2.1.2 TMS320 XDS/22 Communication

The TMS320 XDS/22 Emulator provides communication links to standard RS-232C ports and debugging capabilities with a prompting XDS monitor and full-speed hardware breakpoints and trace. The communication system establishes linkage with the user's terminal, a PROM programmer or printer, and a host computer system. The functions of this communication link are:

- To transmit data files from the emulator to an external device (upload).
- To receive data files from an external device and store them in the emulator's memory (download).
- To pass downloaded data received from an external device to a PROM programmer or logging device.
- To transmit data stored in the emulator's memory to a PROM programmer or logging device.

Each TMS320 XDS/22 unit is equipped with four standard RS-232C ports for communication with external devices. Only three ports are used; the fourth port is reserved for future expansion.

5.2.1.3 TMS320 XDS/22 Debugging

The TMS320 XDS/22 monitor provides a simple yet powerful set of commands for full debug of the target system. Table 5-1 provides a summary of first- and second-generation TMS320 XDS/22 emulator commands grouped by function. Monitor commands provide complete control of both the emulator functions and the target system. The monitor uses extensive prompt menus for commands and parameter definition. Registers are readily accessible through the use of variable names assigned to each register. Debugging sessions can also be logged for further analysis via a line printer. The TMS320 XDS/22 monitor displays a menu of emulator commands and variables to guide the debugging session. As an example, Figure 5-8 shows the screen when the DPS command to display the processor status is entered on the TMS320C10 XDS/22.

```
DPS

  PC =022       AR0 =0000       T =0000          TOS  =000
  ST =3EFC      AR1 =0000       P =00000000      MOSH =000
  ACC=00000000                                   MOSL =000
                                                 BOS  =000

                 OV      OVM    INTM    ARP     DP
                  0       0      1       0       0
```

Figure 5-8. TMS320C10 XDS/22 Display Example

Table 5-1. TMS320 XDS/22 Emulator Commands Grouped by Function

Initialization		Memory	
DEC	Decimal Format	COPY	Copy Memory (TMS320C10 only)
HEX	Hexadecimal Format	DDM	Display Data Memory
ICC	Initialize Cursor Control	DPM	Display Program Memory
IHC	Initialize Host Control	FIFOx	Peripheral Register Commmand (TMS320C14/E14 only)
IMD	Initialize Multiprocessing	FILL	Fill Memory With Data
INIT	Initialize Emulation	FIND	Find Data In Memory
IPORT	Initialize RS-232C Port	IDM	Inspect Data Memory
IPRM	Initialize Parameters	IPM	Inspect Program Memory
ITR	Initialize Target RAM (TMS320C2x only)	MDM	Modify Data Memory
LOAD	Load Stored Parameters	MPM	Modify Program Memory
MAG	Magnitude Format	WRPT	Write Protect Program Memory (TMS320C14/E14 and TMS320C17/E17 only)
MAP	Map Expansion Memory		
RCC	Restore Cursor Controls		
RES	Restore µP Synchronization (TMS320C10 only)	**Registers**	
RESTART	Restart	DR	Display Registers
SNAP	Freeze Display	IR	Inspect
		MR	Modify Registers
Status		**Run**	
DES	Display Emulator Status (TMS320C2x only)	CRUN	Continue Run
DHS	Display Halt Status	GHALT	Group Halt (MP Mode)
DMAP	Display Memory Map (TMS320C2x only)	GRUN	Group Run (MP Mode)
DPS	Display Processor Status	RTR	Run On Target Reset
DTS	Display Trace Status	RUN	Continuous Execution
/n	Display Emulator MP Status	SRR	Software Reset, Run (TMS320C10 only)
Offload		SS	Single-Step Execution
DL	Download	STOP	Stop Alternate-Run Mode
UL	Upload	THALT	Total Halt (MP Mode)
		TRUN	Total Run (MP Mode)
Hardware Breakpoint/Trace		**Software Breakpoint**	
BTT	Set BTT Parameters	CASB	Clear Software Breakpoints
DBTT	Show BTT Parameters	CSB	Clear One Software Breakpoint
DT	Display Trace	DSB	Display All Breakpoints
DTIME	Show Time Settings	SSB	Set One Breakpoint
FT	Find Trace	**Mode**	
IBTT	Initialize BTT	ARM	Initiate Alternate-Run Mode
IT	Inspect Trace	BGND	Initiate Background Mode
XTIME	Time Analysis	DISARM	End Alternate-Run Mode
Assembler		HOST	Initiate Host Mode
XA	Execute Assembler	IMP	Initiate Multiprocessing Mode
XRA	Reverse Assembler	#n	Select Emulator #n
Communications		**Miscellaneous.**	
DIO	Display I/O	DV	Display Values
DIOR	Display I/O Register Contents (TMS320C14/E14 only)	HELP	Display Command Menu
		ID	Display Firmware Revision
MIO	Modify I/O	LOG	Print Commands And Response
		SAVE	Save Parameters

Emulator commands provide extraordinary flexibility in defining the test conditions for emulation sessions. Commands can be combined in a variety of ways to form short procedures that allow several commands to be executed sequentially. Repeat functions allow procedures or individual commands to be executed indefinitely until stopped by the user or a user-defined breakpoint condition.

The XDS/22 supports important breakpoint, trace, and time-stamping (BTT) capabilities. Up to ten software breakpoints and four sequential hardware breakpoints may be defined. This provides a method for testing and debugging small segments of programs. In the monitor mode, all registers and memory locations can be inspected and modified.

In addition to hardware breakpoints, the XDS/22 Emulators support full-speed trace capability. Each traceable machine cycle is sampled, recorded, and stored in the 2K-word trace buffer so that it can later be recalled for display or printing.

Time-stamping is a feature, in which a time value is associated with each trace sample so that the time between breakpoints can be calculated. This allows the user to determine the amount of time spent in a certain portion (e.g., a loop) of code.

5.2.1.4 TMS320 XDS/22 Equipment List

The following equipment is required for use with the TMS320 Emulator:

Terminal
RS-232-C compatible — 25-pin RS-232-C male plug, type DB25P

Cables
For terminal/host or printer — Two standard RS-232-C cables with male connectors on the XDS end

Host Computer (optional)
RS-232-C compatible

Line Printer or Other Logging Device (optional)

5.2.2 TMS320C10 Emulator (XDS/22)

The TMS320C10 Emulator (see Figure 5-9) has been designed to emulate operation of the following first-generation TMS320 family devices: TMS32010, TMS320C10, TMS320C10-14, TMS320C10-25, TMS320C15 /E15, TMS320C15-25 and TMS320E15-25. Other models are available to support the TMS320C14 and TMS320C17. To emulate any one of these devices requires the insertion of the appropriate device into the Emulator Board. The TMS320C10 Emulator is composed of:

- XDS/22 chassis
- Emulator Board (and appropriate device) with target connector cable
- Breakpoint, trace, and timing board with logic analyzer interface cable

- Communications Board
- RS-232C cable for connection between the XDS and PC
- Trace probe cable to connect the breakpoint, trace, and timing board to the target system
- All literature necessary for system development and debug

The **TMS320C10 Emulator Board** contains 4K-words of fast static RAM. This allows for operation in one of three memory modes:

- Software development mode (the entire 4K-words reside within the emulator)
- Microcomputer mode (on the TMS320C10, 1.5K-words of program memory reside within the emulator and 2.5K-words of program memory reside in the target system. On the TMS320C15, the mode is identical to the software development mode and all 4K-words of program memory reside within the emulator)
- Microprocessor mode (the entire 4K-words of program memory reside in the target system)

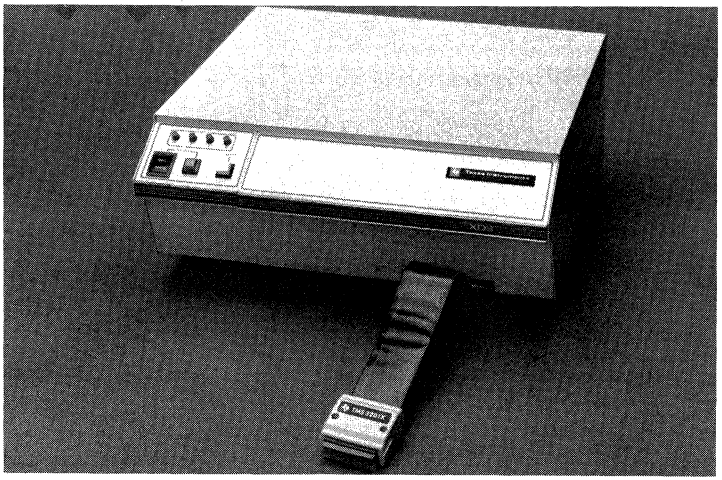

Figure 5-9. TMS320C10 Emulator (XDS/22)

The **Breakpoint, Trace, and Timing Board** (BTT) monitors various hardware activities. It can be programmed to take various actions triggered by the occurance of specified qualifiers, depending on the *state* of the board. This allows multilevel or sequenced breakpoints to be used for complex debugging solutions. The BTT board *trace sample function* provides "snap shot" storage of bus cycle activity. Up to 2,047 samples can be stored in a circular trace buffer. Timing statistics are provided, thus allowing the user to analyze a program's performance by displaying the actual execution time of a particular routine. It has the option of stopping an application program after collecting a selected number of cycles. This board allows the user to analyze a program's

performance by displaying actual execution time or time spent accessing selected memory locations.

The **Communications Board** receives all keyboard or host-computer input and generates RS-232C compatible output signals for the host computer, printer, EPROM programmer, and for screen display.

These key features distinquish the TMS320C10 Emulator:

- 25-MHz full-speed in-circuit emulation
- Dual-in-line target connector with optional PLCC target connector
- Single-step execution
- Line-by-line assembler/reverse assembler
- Enhanced decimal parameter entry and display
- All levels of stack available to user
- Use of target system crystal (with DIP target connector) or internal crystal
- Host-independent upload/download to/from program/data memory
- Ability to inspect/modify all internal registers, program/data
- Multiprocessing support
- Hardware breakpoint, trace, and timing (BTT) capabilities with logic analyzer interface cable
- Logic tracing with extended data/address probes

5.2.3 TMS320C14/E14 Emulator (XDS/22)

The TMS320C14/E14 Emulator provides the capabilities of the TMS320C10 Emulator with the addition of a **TMS320C14 Processor Module (PM)** to the TMS320C1x Base Emulator Board. The TMS320C14 Emulator allows emulation of all aspects of the TMS320C14/E14 device. Monitor commands supported by the TMS320C14 XDS/22 allow any of the TMS320C14 I/O registers to be displayed or modified.

5.2.4 TMS320C17/E17 Emulator (XDS/22)

The TMS320C17/E17 Emulator provides all the capabilities of the TMS320C10 Emulator with the addition of a **TMS320C17 Processor Module** to the base TMS320C1x Base Emulator Board. The TMS320C17 Emulator permits emulation of all aspects of the TMS320C17/E17 device. This includes serial port and co-processor port operations.

Due to the characteristics of the TMS320C17/E17, the Emulator functions in either the co-processor mode or microcomputer mode. The Emulator provides all 4K-words for both modes.

5.2.5 TMS320C2x Emulator (XDS/22)

The TMS320C2x Emulator has been designed to emulate operation of the following second-generation TMS320 family devices: TMS32020, TMS320C25, and TMS320E25. To emulate any one of these devices requires the insertion of the appropriate device in the Emulator Board. The TMS320C2x Emulator does not support the TMS320C25-50. Macrochip Research Inc., a TMS320 Third Party, offers full-speed in-circuit emulation up to 50-MHz to support the TMS320C25-50 (see Section 9). The TMS320C2x Emulator is composed of:

- XDS/22 chassis
- Emulator Board (and appropriate device) with target connector cable
- Breakpoint, trace, and timing board with a logic analyzer interface cable
- Memory expansion/communications board
- RS-232C cable for connection between the XDS and PC
- Trace probe to connect the breakpoint, trace, and timing board to the target system
- All literature necessary for system development and debug.

Figure 5-10. TMS320C2x Emulator (XDS/22)

The **TMS320C2x Emulator Board** contains 8K-words (4K-words program and 4K-words data) of high-speed static RAM (zero wait-state) for program and data memory. The **Memory Expansion/Communications Board** offers 64K-words of DRAM which can be configured (with wait states), as all program memory, all data memory, or a combination of both.

The **Breakpoint, Trace, and Timing Board** (BTT) monitors various hardware activities. It can be programmed to take various actions triggered by the occurance of specified qualifiers, depending on the *state* of the board. This allows multilevel or sequenced breakpoints to be used for complex de-

bugging solutions. The BTT board *trace sample function* provides "snap shot" storage of bus cycle activity. Up to 2,047 samples can be stored in a circular trace buffer. Timing statistics are provided, thus allowing the user to analyze a program's performance by displaying the actual execution time of a particular routine. It has the option of stopping an application program after collecting a selected number of cycles. This board allows the user to analyze a program's performance by displaying actual execution time or time spent accessing selected memory locations.

These key features distinguish the TMS320C2x Emulator:

- 40-MHz full-speed in-circuit emulation
- PLCC target connector with pin grid array adapter
- 4K-words each of program and data high-speed SRAM memory
- 64K-words DRAM memory expansion/communications board
- Hardware breakpoint, trace, and timing capabilities
- Single-step execution
- Line-by-line assembler/reverse assembler
- Enhanced decimal parameter entry and display
- Use of target system CLKIN signal or internal crystal
- Host-independent upload/download to/from program/data memory
- Ability to inspect/modify all internal registers, program/data memory
- Multiprocessing support
- Logic tracing with extended data/address probes
- Logic analyzer interface cable

5.2.6 TMS320C30 XDS500 Emulator

The TMS320C30 XDS500 Emulator is a user-friendly, PC-based development system which provides all the features necessary to perform full-speed in-circuit emulation with the TMS320C30. This emulator allows the user to perform software and hardware development, and to integrate the software and hardware with the target system. A revolutionary 4-wire interface provides control of, and access to, every location and register of the TMS320C30. Key features of the TMS320C30 include:

- Full-speed execution and monitoring of the TMS320C30 in the user's target system via a 12-pin target connector
- Thirty software breakpoints
- Software trace/timing
- Single-step execution
- Load/inspect/modify all registers
- Upload/download program data/memory
- Windowed user interface identical to TMS320C30 simulator
- Emulator portability
- Reconnectable for multiprocessing
- Benchmark of execution time clock cycles in realtime

Full-speed execution and monitoring of the target system is performed by the 4-wire interface (scan path) via a 12-pin target connector. This scan path controls the TMS320C30 in the target application and provides access to all the registers plus all internal and internal memory of the device. Since program execution takes place on the TMS320C30 in the target system, there are no timing differences during emulation. This new design offers significant advantages over traditional emulators. These advantages include:

- No cable length/transmission problems
- A non-intrusive system
- No loading problems on signals
- No artificial memory limitations
- A common screen interface for ease of use
- Easy installation
- 'In-system' emulation
- No variance from data sheet

Software breakpoints allow program execution to be halted at a specified instruction address. When a given breakpoint is reached, the program halts execution. At this point, the status of the registers and the CPU is available. Memory contents can be displayed with a single command.

Software trace allows the user to view the state of the TMS320C30 when a breakpoint is reached. This information can be saved in a file for future analysis. Software timing allows the user to track clock cycles between breakpoints for benchmarking of time critical code.

Single-step execution gives the user the capability to step through the program one instruction at a time. After each instruction, the status of the registers and CPU are displayed. This provides greater flexibility during software debug and helps reduce development time.

Object code can be downloaded to any valid TMS320C30 memory location (program or data) via the 4-wire interface. Downloading a 1K-byte object program typically takes 100 ms. In addition, by inspecting and modifying the registers while single-stepping through a program, the user can examine and modify program code or parameters.

The windowed user interface is identical to that of the TMS320C30 simulator, providing the designer an easy migration path from simulator-based development to emulator-based development. This user-friendly screen displays the program code in nmemonics and in equivalent hexadecimal code. Windowed displays are provided for extended precision registers, the CPU status, and memory locations.

Greater flexibility is achieved through emulator configurability. Both memory and screen color can be configured by the user. Address range, memory type, and access type allowed to each location may also be configured. The memory map, which may include EPROM, SRAM, DRAM, and on-chip memory and peripherals, can be configured by the designer to reflect the actual peripheral environment of the target system including wait states and access privileges.

The 12-pin target connector allows for emulation of multiprocessing applications. For example, if five TMS320C30s exist on one board, as shown in Figure 5-11, each device is emulated by simply moving the 12-pin target connector from one TMS320C30 connector to the next. Realtime emulation is still maintained, and the information of each processor is preserved.

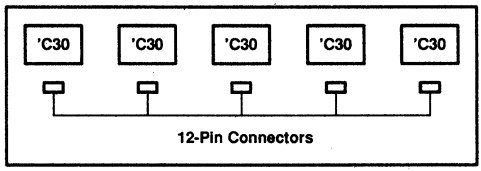

Figure 5-11. Multiprocessing Emulation

The TMS320 XDS500 Emulator includes:

- TMS320C30 Emulator PC Board
- TMS320C30 4-wire interface cable (12-pin connector)
- TMS320C30 Macro Assembler/Linker (MS-DOS)
- User interface software (5.25" floppy disk)
- Literature:
  - TMS320C30 User's Guide

- TMS320C30 Emulator User's Guide,
- TMS320C30 Assembly Language Tools User's Guide

Note: The user must provide a 12-pin signal interface for every TMS320C30 in the target system. Refer to Section 5.2.2.2 for the 12-pin header signal layout.

5.2.6.1 XDS500 Scan Path Interface

The TMS320C30 scan path provides access to a set of test registers internal to the TMS320C30 device. These registers can receive and transmit data through the emulation or scan path pins (EMU0-EMU3). The XDS500 Emulator Board is an interface to the TMS320C30 scan path. Through the 4-wire interface, the XDS500 Emulator is responsible for interpreting commands (sent from the PC via the supplied user interface software) and converting these commands into the appropriate signal sequences necessary to control the TMS320C30 in the user's target system. The emulation mode shown in Figure 5-12, is actually 'self emulation'. The PC is simply controlling the TMS320C30 through the emulator board and scan path registers. When in this mode, the TMS320C30 acts as its own emulator.

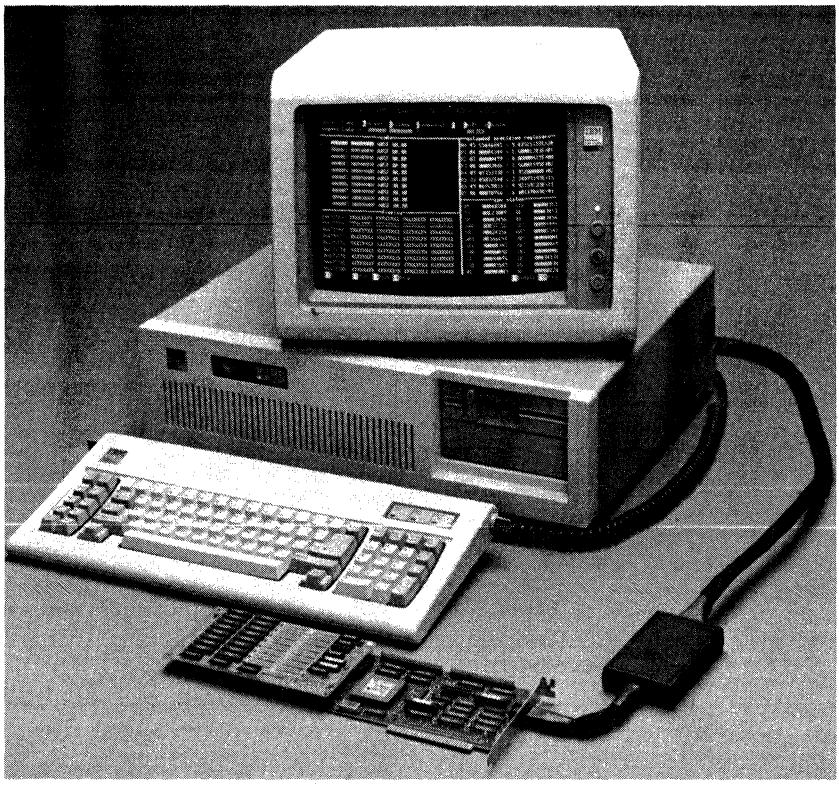

Figure 5-12. TMS320C30 XDS500 Emulation Mode

With the 12-pin connector, four pins transmit and control the information sent to the TMS320C30. This is the 4-wire interface. Additional power and ground pins have been added to preserve signal integrity. Through the 12-pin target connector, the emulator sends commands and receives data necessary to provide full-speed in-circuit emulation.

This revolutionary concept allows the emulator to act as an interface between the PC and the user's target system. Because the TMS320C30 on the target system is used, more reliable emulation is ensured. The 4-wire interface eliminates the need for traditional full pin-out target connectors and removes the problems associated with cable reliability, transmission effects, and timing differences.

5.2.6.2 XDS500 Emulation Target Design Considerations

To use the TMS320C30 XDS500 Emulator for realtime emulation, the user must provide a 12-pin signal interface for every TMS320C30 in the target system. Specifications for building this interface are provided in Figure 5-13, Table 5-2, and the following paragraph.

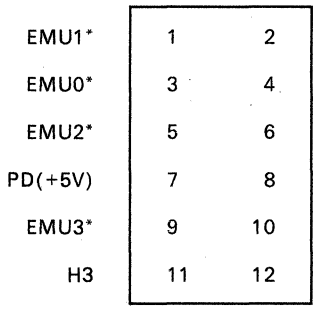

Figure 5-13. TMS320C30 XDS500 12-Pin Header Signals

Table 5-2. TMS320C30 Pin Function Assignment

Signal	Description	TMS320C30 Pin Number
EMU0	Emulation Pin 0	F14
EMU1	Emulation Pin 1	E15
EMU2	Emulation Pin 2	F13
EMU3	Emulation Pin 3	E14
PD	Presence Detect. Indicates that the cable is connected and the target system is powered up. PD should be tied to +5 volts in the target system.	

For unbuffered signals, the distance between the TMS320C30 emulation pins and the 12-pin header should be less than two inches. If the distance between the header is more than two inches and less than six, all transmit scan signals should be buffered. The buffer must be noninverting with a maximum buffer delay that is dependent on the length of the H3 period. For instance, if the H3 period is 50-ns, the maximum buffer delay is 6-ns.

If the distance between the TMS320C30 and the header is six or more inches, all scan signals must be buffered. The maximum allowable distance is determined by the PWB layout and the loading on the H3 clock. If both of these criteria are minimized, the maximum length can be no more than twelve inches. TI recommends that the distance be as short as possible, preferably less than four inches.

5.2.6.3 XDS500 Emulator User Interface

The windowed user interface is identical to that of the TMS320C30 simulator, providing the designer an easy migration path from simulator-based development to emulator-based development. This user-friendly screen displays the program code in mnemonics and in equivalent hexadecimal code. Windowed displays are provided for extended precision registers, CPU status, and memory locations.

There are various screen options used to access the capabilities of the TMS320C30 XDS500 Emulator. The first is the primary screen (see Figure 5-14), comparable to the appearance of the TMS320C30 Simulator screen.

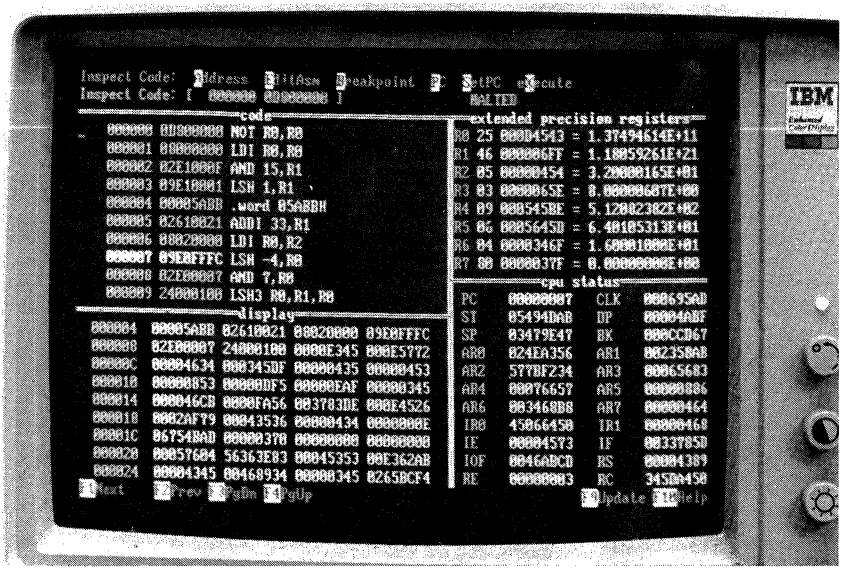

Figure 5-14. XDS500 Emulator Interface Screen

The primary screen includes:

- Command line displayed at top of screen
- Functions of special-function keys
- Four status windows which can be individually accessed using the F1 key
  1) Source code window
  2) Auxiliary display window

3) CPU status window
4) Extended precision registers window

Note - All windows allow the user to inspect/modify its contents.

5.2.6.4 XDS500 Commands

Commands can be entered in either of two ways: MENU mode or LINE mode. In the Menu Command Mode, a menu is provided at the top of the screen. This permits the user to view every option available while entering a single command. After each entry, further menus are displayed until the entire command has been entered. The Line Command Mode allows the user to enter an entire command expression. Table 5-3 gives a summary of available commands. These can be entered by either the LINE or MENU modes.

Table 5-3. Summary of XDS500 Emulator Commands

BREAKPOINT COMMANDS Command Syntax	Operation Description
BA *address*	Breakpoint on Acquisition - Breakpoint will occur when instruction has been loaded into the instruction register.
BD *id no.*	Breakpoint Delete - Delete breakpoint number *id no.*
BL *filename* (e.g., stored by BS command).	Breakpoint Load - Load breakpoints stored in *filename*
BR	Breakpoint(s) Remove - Remove all break-points.
BS *filename*	Breakpoint Save - Save all breakpoints in *filename*.
CONFIGURATION COMMANDS **Command Syntax**	**Operation Description**
CC	Configure Colors - Set color, reversing, and blinking for screen.
CM	Configure Memory mode - Enter mode; action defined by mnemonic's final letter and operand(s).
CMA *low addr, hi addr, type* {**R**|**R**/**W**}	Configure Memory Address - Designate a block of memory to be added to the memory configuration.
CMD *id no.*	Configure Memory Delete - Delete the memory defined by the *id no.* assigned by the CMA command.
CME *id no, low addr, high addr, type,* {**R**|**R**/**W**}	Configure Memory Edit - Edits the memory block defined by the *id no.* assigned by the CMA command.
CML *filename*	Configure Memory Load - Load the memory configuration stored in *filename* (e.g., stored by CMS command).
CMR	Configure Memory Reset - Reset configured memory to default initialization.
CMS *filename*	Configure Memory Save - Save memory configuration in *filename*.

Table 5-3. Summary of XDS500 Emulator Commands (Continued)

DISPLAY COMMANDS Display in lower-left corner Command Syntax	Operation Description
DB *start position*	Display Breakpoints - Display break-point configuration as set by the breakpoint command.
DC *start position*	Display memory Configuration - Display memory configuration as set by the CMA command.
DE	Display Expression.
DF *filename,[line no.]*	Display File - Display text file starting at *line no.*
DM *address*	Display Memory - starting at *address* .
DS *start position*	Display Symbols - Show all or start *start position* line number.
DV	Display Version - Clear display area, print banner.
EXPRESSION COMMANDS **Command Syntax**	**Operation Description**
EA *expr [name], [radix],* {**B**|**W**|**D**}	Expression Add -Add expression with optional descriptors.
ED *id no.*	Expression Delete - Delete expression identified by *id no.*.
EF *id no.* {**A**|**B**|**D**|**F**|**H**|**O**}	Expression Format - Specify numerical parameters.
EL *filename*	Expression Load - load from *filename.*
EH *id no., name*	Expression reName - Change to *name.*
ES *filename*	Expression Save - Store in *filename.*
JOURNAL COMMANDS **Command Syntax**	**Operation Description**
JC *filename*	Journal Capture - In command mode, saves in *filename.*
JE *filename*	Journal Execute - Executes commands stored in *filename* by JC command.
JS	Journal capture Stop - Halts JC command execution.

Table 5-3. Summary of XDS500 Emulator Commands (Continued)

LOAD COMMANDS	
Command Syntax	**Operation Description**
LB *filename*	Load Breakpoint configuration - Load from *filename* the breakpoint configuration saved by SB command.
LC *filename*	Load memory Configuration - Load from *filename* the memory configuration saved by SC command.
LE *filename*	Load Expressions - Load expressions from *filename* saved by SEcommand.
LM *filename*	Load Memory dump - load *filename* into memory at locations set by SM command.
LO	Load COFF file - Load the COFF-type file named *filename*.
LR *filename*	Load Register configuration - Load the registers with the configuration stored in *filename* .
MEMORY COMMANDS	
Command Syntax	**Operation Description**
MA *address, statement*	Memory Assemble - Show source statement at *address*. Also, input/assemble new *statement*.
MF *start addr, end addr, value*	Memory Fill - Fill memory from *start addr* to *end addr* with *value* .
MM *address, value*	Memory Modify - Change location *address* to *value*.
OP SYS, QUIT, REGISTER/EXPRESSION COMMANDS	
Command Syntax	**Operation Description**
O	Escape to Operating system - Emulator retained in memory.
Q	Quit; exit to operating system -Emulator not retained in memory.
R *register, value*	Fill *Register* withwith *value* - Could be expression results.

Table 5-3. Summary of XDS500 Emulator Commands (Concluded)

SAVE COMMANDS	
Command Syntax	**Operation Description**
SB *filename*	Save Breakpoint configuration in *filename*
SC *filename*	Save memory Configuration in *filename*
SE *filename*	Save Expressions in *filename*
SM *filename, start addr, end addr*	SaveMemory dump from *start addr* to *end addr* - Save in *filename*.
SR *filename*	Save Registers in *filename*.
EXECUTION COMMANDS	
Command Syntax	**Operation Description**
X	eXecute mode - Enter mode: action defined by mnemonic's final letter and operand(s).
XC *cycle count*	eXecute Cycle - Execute for *cycle count* (clock cycles).
XD	eXecute Disconnect - Puts the emulator in user run mode, thus, functionally disconnecting the emulator from the target system.
XG	eXecute Go - Execute beginning at present PC value.
XI *[count]*	eXecute Instruction - Execute one (default) or *count* instructions beginning at present PC value until breakpoint.
XO	eXecute cOnnect - Functionally connects the emulator to the target system.
XR	eXecute Reset - Reset TMS320C30 as if the pin RESET was asserted. The value of the the reset vector address (0x000000) is placed in the PC.

5.2.6.5 XDS500 System Requirements

Host	IBM PC-XT/AT
Slot	One and one-half 8- or 16-bit slots
Memory	Minimum of 640K-words
Storage	One floppy drive and one hard drive
Operating System	PC MS-DOS 2.0 or later version
Power Supply	Minimum approximately 3 amps @ 5 volts (150 watts)

Note:

The power supply requirements are such that some PC-XT configurations will not have sufficient power available. This is particularly true when the TMS320C30 XDS500 Emulator is used in conjunction with the TMS320C30 Application Board. Therefore Texas Instruments strongly recommends the use of an IBM PC-AT for the standard host. If the IBM PC-XT is preferred, ensure that it is fitted with a power supply that outputs a minimum of 150 watts.

5.2.6.6 XDS500 Installation

The TMS320C30 XDS500 Emulator is a single card which requires one and one-half 8- or 16-bit slots in an IBM PC-XT/AT. This provides emulator portability. Instead of carrying an emulator chassis from one area to another, the emulator board can be simply transferred to another PC.

To install the TMS320C30 XDS500 Emulator Board, simply insert the board into an 8- or 16-bit slot in the backplane bus of the PC. Installation of the User Interface Software is detailed in the TMS320C30 Emulator User's Guide.

The cable hookup is shown in Figure 5-15.

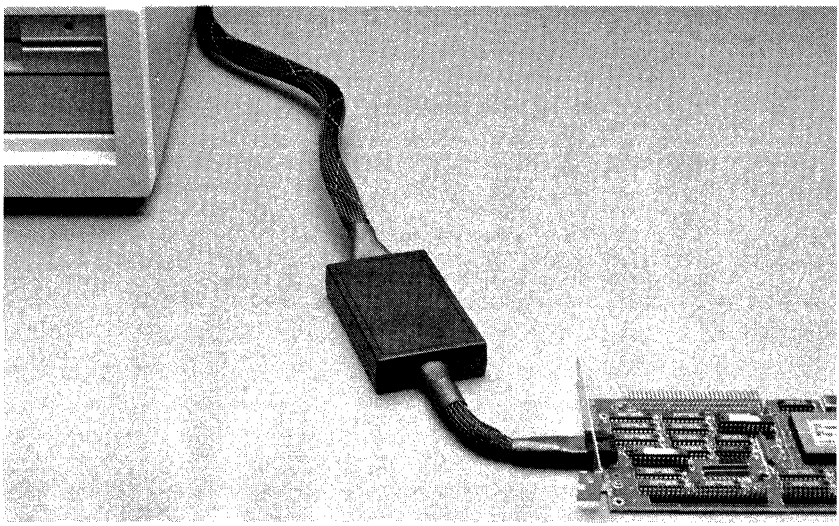

Figure 5-15. TMS320C30 XDS500 Target Connector Cable

5.2.7 TMS320C30 XDS1000 Development Environment

The TMS320C30 XDS1000 is a complete development environment that provides all the development tools necessary from the beginning stages of development through full production. The TMS320C30 XDS1000 consists of the TMS320C30 XDS500 described in the previous subsection plus an additional full-size PC-XT/AT board and associated software. The additional board is the TMS320C30 Application board.

The TMS320C30 Application board is a predefined target system, intended for software development in realtime as well as hardware/software application support. The XDS1000 operates in two modes: **emulation** and **algorithm development**. For a detailed description of the **emulation mode**, refer to Section 5.2.6.. The **algorithm development mode** is described in the next paragraph. A visual representation of the XDS1000's algorithm mode is shown in Figure 5-16

The **algorithm development mode** allows debug of TMS320C30 software at full-speed before the target system is complete. This is possible because code can be downloaded into the memory on the TMS320C30 Application Board and then executed at full speed by the TMS320C30 XDS500 Emulator via the 4-wire interface. In this configuration, the TMS320C30 Application Board can be used in place of the user's target system.

Figure 5-16. TMS320C30 XDS1000 Algorithm Development Configuration

Key features of the TMS320C30 Application Board include:

- PC-based Application Board (including an on-board TMS320C30 device)
- 16K x 32-bits full-speed (zero wait-state) SRAM on the primary bus
- Two selectable banks of 8K x 32-bits full-speed (zero wait-state) SRAM on the expansion bus
- 512K x 32-bits DRAM (user upgradable to 1M x 32-bits)

The large amount of on-board SRAM provides the user with realtime emulation capabilities and memory storage flexibility for a variety of algorithms. The zero wait-state capability implemented with SRAM allows for memory read/write in realtime.

Page mode DRAM is used to improve bulk storage performance. Three types of DRAM cycles are used on the TMS320C30 Application Board: Single-word read, single-word write, and page-mode read. These operations require four, two, and one wait-state per access respectively. Page-mode read cycles are automatically evoked when the TMS320C30 performs two or more back-

to-back read cycles on the same memory page. A page of memory is 256 words. This is the default memory bank size for the TMS320C30. Utilizing page-mode results in a decrease in wait-states when accessing emulator DRAM.

The TMS320 XDS1000 Development Environment includes:

- TMS320C30 Emulator PC Board (also part of the TMS320C30 XDS500 Emulator)
- TMS320C30 Application Board (includes on-board TMS320C30)
- TMS320C30 4-wire interface cable (12-pin connector) (also part of the TMS320C30 XDS500 Emulator)
- TMS320C30 Macro Assembler/Linker (MS-DOS) (also part of the TMS320C30 XDS500 Emulator)
- User interface software (5.25" floppy disk) (also part of the TMS320C30 XDS500 Emulator)
- TMS320C30 C compiler (MS-DOS)
- SPOX DSP operating system
- Literature:
  - TMS320C30 User's Guide (also part of the TMS320C30 XDS500 Emulator)
  - TMS320C30 Emulator User's Guide (also part of the TMS320C30 XDS500 Emulator)
  - TMS320C30 Application Board User's Guide
  - TMS320C30 Assembly Language Tools User's Guide (also part of the TMS320C30 XDS500 Emulator)
  - TMS320C30 C compiler User's Guide
  - Getting Started with SPOX
  - SPOX Programmer's Reference Manual

5.2.7.1 XDS1000 System Requirements

Host	IBM PC-XT/AT
Slot	Three full-size 8- or 16-bit slots
Memory	Minimum of 640K-words
Storage	One floppy drive and one hard drive
Operating System	PC MS-DOS 2.0 or later version
Power Supply	Minimum approximately 3 amps @ 5 volts (150 watts)

Note:

The power supply requirements are such that some PC-XT configurations will not have sufficient power available. Therefore Texas Instruments strongly recommends the use of an IBM PC-AT for the standard host. If the IBM PC-XT is preferred, ensure that it is fitted with a power supply that outputs a minimum of 150 watts.

5.2.7.2 XDS1000 Installation

The TMS320C30 XDS500 Emulator Board requires one and one-half 8- or 16-bit slots and the TMS320C30 Application Board requires one and one-half 8- or 16-bit slots in the backplane bus of the PC. The Application Board requires the additional half card space because of the 'piggy-back' board containing the DRAM expansion memory. Installation of these boards and the User Interface Software is described in the TMS320C30 Emulator User's Guide.

5.3 TMS320 XDS Upgrade Program

As Texas Instruments directs its efforts toward TMS320 family enhancement and expansion, development support must parallel. For this reason, TI not only offers newly enhanced first-, second-, and third-generation XDS Extended Development Support systems, but also offers upgrade kits for early systems. For a discussion of the new systems, see Section 5.2.

TMS320 XDS upgrade kits are intended to extend the functionality of existing development systems at a minimum of cost through an enhancement of current customer equipment. For example, an upgrade kit can enable a TMS32010 XDS/22 to emulate operation of all speed versions of the TMS320C10 and TMS320C15/E15. A second-generation upgrade kit can enable a TMS32020 XDS/22 to emulate the CMOS TMS320C25. Upgrade kits allow upgrade only within a generation, not from a first- to a second-generation XDS.

Figure 5-17 shows the addition of the upgrade kit to the early system to give an enhanced XDS system. Table 5-4 lists the part numbers for the early system, the upgrade kit, and the enhanced system to assist the user in understanding the procedure.

Table 5-4. TMS320 XDS Upgrade Process

EARLY SYSTEM	+	UPGRADE KIT	=	ENHANCED SYSTEM
TMS32010 XDS/22	+	TMS320C10 XDS/22 Upgrade Kit	=	TMS320C10/C15 XDS/22
(PN: TMDS3262210)		(PN: TMDX3282216)		(PN: TMDX3262211)
Accommodates the TMS32010				Accommodates all versions of the TMS320C10 and TMS320C15
TMS320C10/C15 XDS/22	+	TMS320C17 PM		
		(PN: TMDX3285014)		
	+	TMDS320C1x EMU	=	TMS320C17 XDS/22
(PN: TMDS3262111)		(PN: TMDX3285018)		(PN: TMDX3262217)
Accomodates all versions of the TMS320C10 and TMS320C15				Accomodates the TMS320C17
TMS320C10/C15 XDS/22	+	TMS320C14 PM		
		(PN: TMDX3285010)		
	+	TMS320C1x EMU	=	TMS320C14 XDS/22
(PN: TMDS3262211)		(PN: TMDX3285018)		(PN: TMDX3262214)
Accomodates all versions of the TMS320C10 and TMS320C15				Accomodates the TMS320C14
TMS32020 XDS/22	+	TMS320C25 XDS/22 Upgrade Kit	=	TMS320C25 XDS/22
(PN: TMDS3262220)		(PN: TMDX3282225)		(PN: TMDS3262221)
Accommodates the TMS32020				Accommodates the TMS32020 and TMS320C25

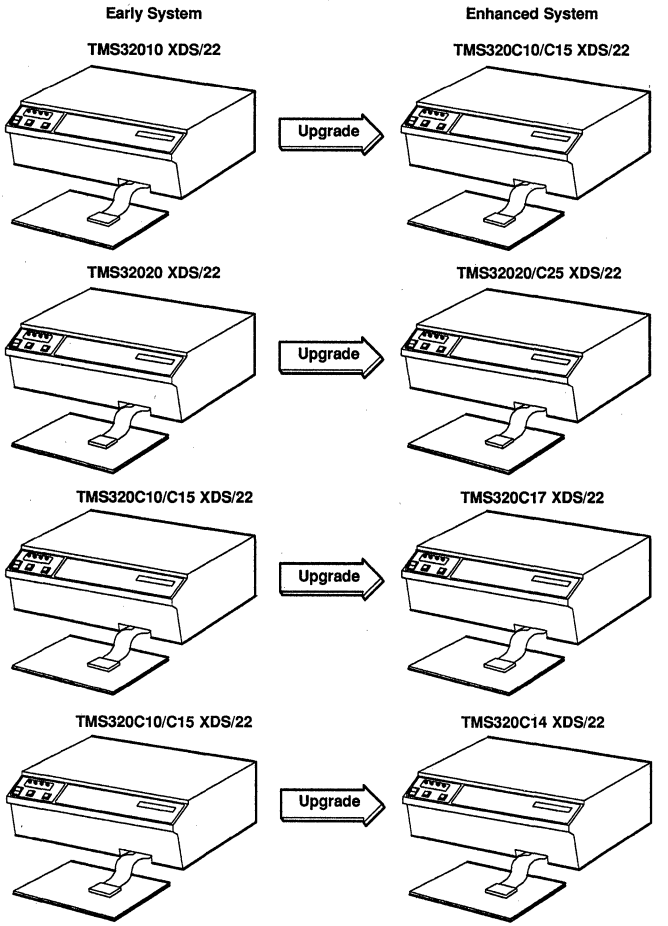

Figure 5-17. XDS Upgrade Configurations

Table 5-5 lists the contents of the upgrade kits for the XDS models.

Table 5-5. TMS320 XDS Upgrade Kit Contents

NEW DEVICE SUPPORTED	MODEL	CONTENTS
TMS320C10/C15	XDS/22	Emulator board, 40-MHz breakpoint, trace and timing board, plus DIP target connector.
TMS320C14	XDS/22	Emulator board, processor module, and PLCC target connector.
TMS320C17	XDS/22	Emulator board, processor module, and DIP target connector.
TMS32020/C25	XDS/22	2 PALs, 2 EPROMs, 2 RAMs, crystal, TMS320C25 40-MHz breakpoint, trace, and timing board, plus PGA/PLCC target connector.

5.3.1 Customer Upgrade

Standard upgrade procedures require that the customer makes the necessary modifications to the system with the TMS320 XDS customer upgrade kit. This is an advantage because it permits the customer to keep the XDS system in-house, thus eliminating the loss of valuable development time. There is a 30 day warranty on upgrades performed by the customer. A board level test is performed by the factory on each board prior to shipment of the customer upgrade kit.

Please note that the TI standard warranty does not allow for customer upgrade to a system still under the 90-day warranty period. According to that warranty, any change or modification to a system still under warranty voids that warranty. Repairs to customer-modified systems will be done at the current factory repair prices (see Section B.2, page B-3).

TMS320 XDS customer upgrade kits are available through authorized distributors or directly from TI. Contact the nearest TI Field Sales Office for further information.

5.4 TMS320 Analog Interface Board (AIB)

The TMS320 Analog Interface Board (AIB) is an analog-to-digital, digital-to-analog conversion board used as a preliminary target system with the TMS320C1x EVM, TMS320C2x SWDS, and TMS320C1x/C2x XDS/22. The AIB is an educational tool used to become familiar with digital signal processing (DSP) techniques.

The AIB allows testing of application programs with analog I/O by providing an interface to the TMS320. There are two versions of the AIB currently available.

5.4.1 Analog Interface Board Version 2

The Analog Interface Board Version 2 (AIB2) for both the first- and second-generation of DSP devices provides analog analog and digital I/O for algorithm development, using the XDS/22 EVM or SWDS development tools. It can operate in a stand-alone demonstration configuration after code development has been completed.

A variety of conversion devices are available to the algorithm developer including a 16-bit linear A/D and D/A, a TMC2916 codec, and the TLC32040 Analog Interface chip (AIC). The linear converters are mapped into the parallel I/O space of the DSP devices. The serial codec and AIC devices can be connected to the serial port interfaces of the TMS320C17 and TMS320C2x devices.

User programmable input and output filters are provided to band limit inputs, minimize aliasing effects, and smooth the output of the D/A. These filters can be jumper bypassed. A prototype area is provided, and is surrounded with daughter board connectors. A function generator is included that provides triangle, sine, and square wave outputs to the AIB2, as well as noise generation and frequency sweep capabilities. A flexible wait-state generator allows use of slower peripherals in the prototype area with full-speed DSP devices.

> **Note:** For all new designs, the AIB2 is recommended. The Analog Interface Board Version 1 (AIB1) supports first-generation hardware tools. Adding the TMS320 Family Adapter Board allows the AIB1 to support second generation hardware tools.

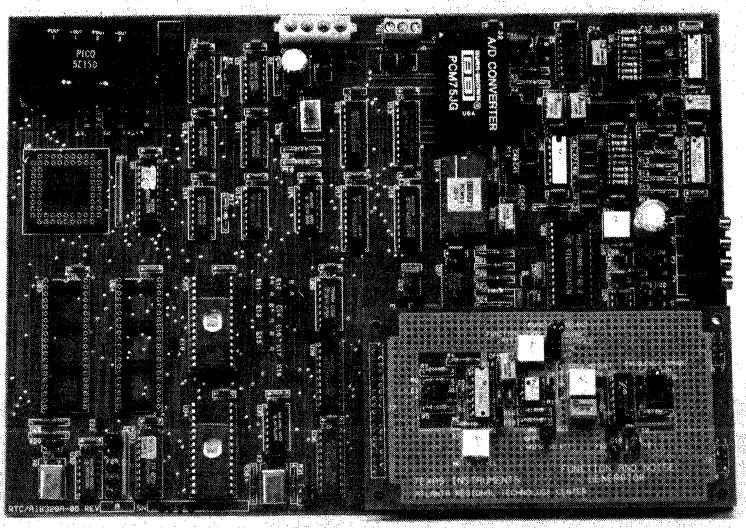

Figure 5-18. TMS320 Analog Interface Board Version 2

These key features distinguish the AIB2:

- 16-bit A/D (17-μsec) with sample/hold and antialiasing filter
- 16-bit D/A (3-μsec) with smoothing filter
- TLC32040 Analog Interface Chip (AIC) and 5.184-MHz crystal
- TCM2916 Codec and 2.048-MHz crystal
- Differential input amplifier
- Audio input amplifier
- Programmable sample rate clock
- Program memory sockets and oscillator for stand-alone demo operation
- +/- 15V DC/DC converter for +5V DC only operation
- 16-bit input/output port

The AIB2 is designed for 40-MHz operation offering 17 microsecond conversion of 16-bit samples. This allows algorithm development over the entire audio spectrum. The AIB2 includes:

- The Analog Interface Board 2
- The Function Generator Daughter Board (FGB)
- User's Guide
- Installation diskette
- Power supply cable.

For part number information, refer to Appendix A. For more information on pricing and availability, contact the nearest TI Field Sales Office.

5.4.2 Analog Interface Board Version 1

The original Analog Interface Board Version 1 (AIB1) for first-generation DSP devices provides analog and digital I/O algorithm development using the TMS320C1x EVM and TMS320C1x XDS/22. The AIB1 also supports a TMS320 Family Adapter Board that plugs into the AIB1, upgrading it for second-generation DSP algorithm and stand-alone operation.

> **Note:** The use of the TMS320 Family Adapter Board is intended to allow installed AIB1 units to support second-generation hardware tools. For all new designs, the AIB2 is recommended.

The AIB1 features 12-bit A/D and D/A linear converters, programmable sample rate clock, sample and hold anti-aliasing input filters, and output smoothing filters. All filters are user programmable. A prototype area is included and surrounded by all I/O control and data signals. One 16-bit I/O expansion port is also available.

These key features distinguish the AIB1:

- 12-bit A/D (25 μsec) with sample/hold and anti-aliasing filter
- 12-bit D/A (3 μsec) with smoothing filter
- 8K-words I/O mapped data memory expansion
- One 16-bit output port for additional D/A or user-defined application
- One 16-bit input port for additional A/D or user-defined application
- Programmable sample rate clock
- Prototype area with I/O expansion port

The AIB1 is designed for 20-MHz operation and provides a low cost target I/O system with 25 microsecond conversion of 12-bit samples, allowing for algorithm development over the entire speech band. The AIB1 includes:

- The Analog Interface Board Version 1
- User's Guide
- Power supply cable.

For part number information, refer to Appendix A. For more information on pricing and availability, contact the nearest TI Field Sales Office.

5.4.3 System Configuration

The AIB1 or AIB2 can be configured to operate as a preliminary target system with the TMS320 XDS/22, EVM, SWDS or other emulator. Figure 5-19 shows a typical AIB System configuration.

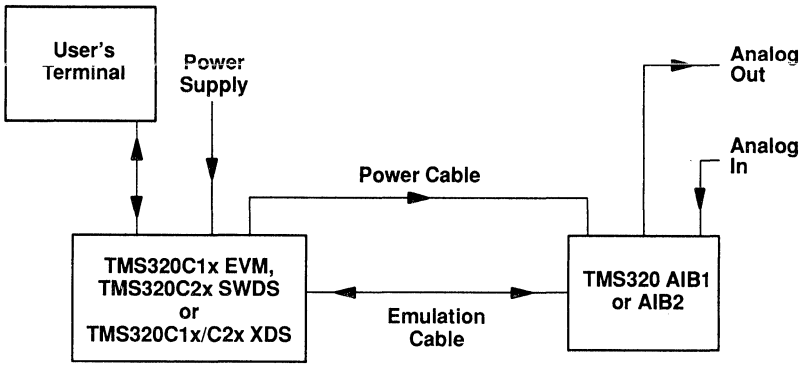

Figure 5-19. TMS320 AIB System Configuration

5.4.4 AIB Equipment List

The following equipment is required for use with the AIB:

Power Supply

+5 V @ 1.2 A
-12 V @ 0.25 A (For AIB1 only)
+12 V @ 0.25 A (For AIB1 only)

Terminal

RS-232-C compatible (for EVM or XDS)	25-pin RS-232-C male plug type DB25P

TMS320C1x EVM **TMS320C2x SWDS, or** **TMS320C1x/C2x XDS**	TMS320 development support system
Cables	
Emulation cable to AIB	Included with SWDS or XDS/22
Power cable from EVM	Included with AIB1

Section 6

RTC TMS320 Seminar and Workshops

The Texas Instruments Regional Technology Centers (RTC) in North America, Canada, Europe, and Asia are staffed with system analysts, providing technical information and assistance in the development of TMS320-based designs. The RTCs offer an unmatched array of up-to-date technical product seminars and design workshops.

The DSP design workshops give design engineers hands-on experience using the latest TMS320 products, development tools, and design techniques. These three-day workshops go beyond the standard lecture format. The exercises and lab experiments start with the basics and move quickly into realtime examples. The student interacts with expert instructors who teach design techniques gained from experience. In these workshops, the student learns by doing, not just listening or observing.

This section describes the seminar and workshops offered in North America. Further information can be obtained by contacting the nearest RTC. A list of the worldwide RTC locations is also provided so that the appropriate one can be contacted for information about the seminar and workshops offered abroad.

6.1 DSP Design Workshops

The Regional Technology Centers (RTC) offer three-day DSP Design Workshops, held either at the RTC location or at a customer-selected site to assist users in the development of TMS320-based designs. Each of the three different workshops covers a different member of the TMS320 DSP family.

The main objective of the workshop is to demonstrate hardware and software techniques for implementing current DSP algorithms using a TMS320 digital signal processor. Exercises provide hands-on experience with the development tools needed for a quick start in designing with the TMS320 family.

6.1.1 First Generation Design Workshop

The First Generation DSP Design Workshop is tailored for designers who have a working knowledge of, and some experience with, microcomputer based designs. It is appropriate, although not required, to have some background in DSP techniques.

Topics covered in the TMS320C1x DSP Design Workskop include:

- TMS320C1x architecture/instruction set
- Fractional binary arithmetic and scaling
- Coding of difference equations
- TMS320C1x development tools
- Using a PC-based TMS320C1x development system
- Digital filter design approaches
- FFT implementation techniques

6.1.2 Second Generation Design Workshop

The Second Generation DSP Design Workshop is tailored for design engineers in the early stages of TMS320C2x application development. The workshop enables the designer to more effectively use the second-generation digital signal processors through hands-on practice of design skills. The designer is introduced to numerous hardware and software techniques for application of current DSP algorithms. Previous experience with assembly language programming and DSP knowledge is necessary, and prior completion of the first-generation DSP workshop is desired. Topics covered in this workshop include:

- Using the PC-based TMS320C2x SoftWare Development System (SWDS)
- TMS320C2x architecture/instruction set
- Binary arithmetic, scaling, and difference equations
- Floating-point arithmetic
- System memory configurations
- Parallel interface timings
- Memory, I/O interfacing, interrupts, and multiprocessing.

6.1.3 Third Generation Design Workshop

The Third Generation DSP Design Workshop is tailored for the hardware and software design engineers and decision makers who will be designing and utilizing the TMS320C3x family of DSP devices. Hands-on exercises throughout the course give the designer a rapid start utilizing TMS320C3x design skills. Experience with digital design techniques is desirable, microprocessor/assembly language experience is required. C language programming experience is desirable. Prior completion of the First and/or Second Generation DSP Design Workshop is beneficial. Topics covered in the Third Generation DSP Design Workshop include:

- TMS320C3x architecture/instruction set
- Use of the PC-based TMS320C3x software simulator
- Floating-point and parallel operations
- Use of the TMS320C3x assembler/linker
- C programming environment
- System architecture considerations
- Memory and I/O interfacing
- TMS320C3x development support

6.1.4 Registration

Class size for these workshops is limited to ten students. To register, contact the nearest TI RTC. A 15-percent discount is available when three or more engineers from the same company enroll in the same course.

6.2 RTC Locations

Further information about the TMS320 DSP Design Workshops can be obtained by contacting the nearest Regional Technology Center (RTC). The following list gives the worldwide locations of the TI RTCs.

North American Locations:

Atlanta
5515 Spalding Drive
Norcross, GA 30092
(404) 662-7945

Boston
950 Winter Street
Suite 2800
Waltham, MA 01254
(617) 895-9196

Chicago
515 W. Algonquin Road
Arlington Heights, IL 60005
(312) 640-2909

Dallas
1001 E. Campbell Road
Richardson, TX 75081
(214) 680-5091

Denver
1400 S. Potomac Street
Suite 101
Aurora, CO 80012
(303) 368-8000

Santa Clara
(Northern California RTC)
5353 Betsy Ross Drive
Santa Clara, CA 95054
(408) 748-2220

Ottawa
301 Moodie Drive
Nepean Ontario
K2H 9C4 Canada
(613) 726-1970

Torrance
(Southern California RTC)
690 Knox Street
Torrance, CA 90502
(213) 217-7019

European Locations:

Holland
P.O. Box 12995
1100 AZ Amsterdam Zuid-Oost
Amsterdam, Holland
31-20-560-2911

France
8-10 Avenue Morane Saulinier
Boite Postale 67
Velizii-Villacoublay Cedex
Paris, France
33-13-0701133

Sweden
Box 30
S-16943
Kista, Sweden
46-8-752-5800

Germany
Haggertystrasse 1
8050 Freising, Germany
49-8161-804836

Italy
Viale Europa, 38/44
20093 Cologno Monzese
Milano, Italy
39-253001

United Kingdom
Manton Lane
Bedford, England MK417PA
(44) 0234-270-111

Asian Locations:

Osaka, Japan 541
Nissho Iwai Bldg 5F
30 Imabashi 3-Chome
Higashi-Ku
81-6-204-1884

Nagoya, Japan 450
Daini Toyota West Bldg. 7F
10-27 Meieki 4-Chome
Nakamura-Ku
81-52-583-8691

Tokyo, Japan 107
Aoyama Fuji Bldg. 4F
6-12 Kita-Aoyama 3-Chome
Minato-Ku
81-3-498-2111

Hong-Kong
8th Floor, World Shipping Centre
Harbour City 7, Canton Road
Kowloon
852-3-7221223

Section 7

TMS320 Documentation Support

Texas Instruments provides extensive documentation to support the TMS320 family from product announcement through applications development. Documents include product bulletins, data sheets, user's and reference guides, over 1000 pages of application notes, and textbooks offered by both Prentice-Hall and John Wiley and Sons. The latest product and documentation updates are given in the TMS320 quarterly newsletter, *Details on Signal Processing*, and the TMS320 DSP Bulletin Board Service. Technical questions regarding the TMS320 family may be directed to the TMS320 DSP hotline (see Section 7.8).

This section discusses the various documents listed below.

- Product Bulletins (Section 7.1 on page 7-2)
- User's Guides and Data Sheets (Section 7.2 on page 6-4)
- DSP Applications Book (Section 7.3 on page 7-4)
- University Textbooks (Section 7.4 on page 7-6)
- Technical Articles (Section 7.5 on page 7-9)
- TMS320 Quarterly Newsletter (Section 7.6 on page 7-34)
- TMS320 DSP Bulletin Board Service (Section 7.7 on page 7-35)
- TMS320 DSP Hotline (Section 7.8 on page 7-36)

To receive copies of available TMS320 literature, complete the literature request card at the back of this document or call:

CUSTOMER RESPONSE CENTER (CRC) (800) 232-3200 X3510

7.1 Product Bulletins

Product bulletins are the first documents published when a new product is being announced. Later these documents are replaced by the product user's guide.

Product bulletins are periodically published to give updated information on the TMS320 family of digital signal processors. They describe the device or devices, present key features, and suggest applications.

Table 7-1 lists the product bulletins available to support the TMS320 family. They can be ordered using the literature number indicated.

Table 7-1. TMS320 Product Bulletins

PRODUCT	DOCUMENT	LITERATURE NUMBER
TMS320C14	TMS320C14 Product Bulletin	3PRT068
TMS320	TMS320 Family Product Bulletin	SPRT056

7.2 User's Guides and Data Sheets

A user's guide for a TMS320 processor provides detailed information regarding the architecture of the device, its operation, assembly language instructions, and hardware and software applications. Data sheets are included in the user's guide as an appendix. Data sheets provide electrical specifications, timing, and mechanical data for the device. In some cases, data sheets are also published separately from the user's guide.

Table 7-2 lists the user's guides and data sheets available for the TMS320 family of processors.

Table 7-2. TMS320 User's Guides

PRODUCT	DOCUMENT	LITERATURE NUMBER
TMS320C1x	TMS320 First Generation User's Guide	SPRU013B
TMS320C14	TMS320C14 User's Guide	SPRU032
TMS320C2x	TMS320 Second Generation User's Guide	SPRU014A
TMS320C3x	TMS320 Third Generation User's Guide	SPRU031
TMS320	TMS320 Family Development Support Reference Guide	SPRU011A
TMS320C1x	TMS320 First Generation Data Sheet	SPRS009B
TMS320C2x	TMS320 Second Generation Data Sheet	SPRS010A

7.3 DSP Applications Book

The TMS320 engineers are constantly developing application reports as they assist customers in designing DSP applications using the TMS320 family. Currently there are over 1000 pages of application reports available to support the TMS320 family. New application reports are announced through the TMS320 DSP Bulletin Board Service (BBS) and in the TMS320 quarterly newsletter, *Details on Signal Processing*.

Over thirty application reports, which cover generic DSP routines, telecommunications, control, and computer applications are included in the book *Digital Signal Processing Applications with the TMS320 Family, Volume I* (SPRA012A) and on the TMS320 BBS. The BBS and application book combine application reports on the First, Second, and Third Generation TMS320 family DSPs, providing users with a source for the most common applications of the TMS320 family.

The materials included on the BBS and in the application book are primarily application reports, which have been generated by the DSP engineering staff of Texas Instruments Semiconductor Group. Some published articles and technical reports have been reprinted to supplement the application reports. This provides more complete coverage of the subject matter. The application reports contain complete theory and implementation(consisting of algorithms, TMS320 code, and/or schematics).

In addition to the application reports in *Digital Signal Processing Applications with the TMS320 Family Volume I*, there are several other application reports separately available. Table 7-3 lists the application subjects available on the BBS and in volume I of the application book as well as the separately published reports.

Table 7-3. Application Reports

DEVICE	SUBJECT	LOCATION†
	DSP Routines	
TMS320C1x/C2x	Floating-Point Arithmetic	1
TMS320C1x	Precision Digital Sine-Wave Generation	1
TMS320C1x/C2x/C3x	Companding Routines	1
TMS320C1x/C2x/C3x	FIR/IIR Filters	1
TMS320C1x/C2x/C3x	Matrix Multiplication	1
TMS320C1x/C2x	Self Test	BBS
TMS320C1x/C2x	FFT	1
TMS320C1x/C2x	Floating-Point Arithmetic	1
TMS320C3x	FFT	BBS
TMS320C2x/C3x	Adaptive Filter and Code Generation	BBS
TMS320C3x	Extended Precision Floating Point Math	BBS
	DSP Interface	
TMS320C1x	Asynchronous Input Interface	1
TMS320C1x	External Memory Interface	1
TMS320C2x	Hardware Interface	1
TMS320C2x	MC68000 Interface	1
TMS320C25	Hardware Interfacing	Lit # SPRA014A
TMS320	Interfacing the TLC32040 Family to the TMS320 Family	Lit # SLAU001
	Telecommunications	
TMS320C1x	ADPCM (CCITT/Non-CCITT)	1
TMS320C1x	Data Encryption	1
TMS320C1x	Telecommunications Interface	1
TMS32010	Theory and Implementation of a Splitband Modem Using the TMS32010	Lit # SPRA013
TMS320C2x	Digital Voice Echo Cancellation	1
TMS320C17	212A Modem Theory	BBS
TMS320C17	DTMF and Tone Decode	BBS
	Digital Control	
TMS320C1x	Control System Implementation	1
	Image/Graphics	
TMS320C2x	Graphics Implementation	1

NOTE:
† - Number 1 shown in this column refer to Digital Signal Processing with the TMS320 Family Volume I

Included in the Applications Book is the source code for the applications discussed. This code can be used to reduce design time and move TMS320-based products to market faster. Source code is also available on the TMS320 Bulletin Board Service (BBS). Refer to Section 7.7 on page 7-32 for more information.

7.4 University Textbooks

A series of DSP textbooks have been published to support digital signal processing research and education. These textbooks are designed to aid in the understanding of DSP applications and implementations using the TMS320 family. Table 7-4 provides a list by publisher and author(s). The following subsections give a brief description of each book.

Table 7-4. DSP Textbooks

TITLE	AUTHOR
John Wiley and Sons	
DFT/FFT and Convolution Algorithms	C.S. Burrus, T.W. Parks
Digital Filter Design	T.W. Parks, C.S. Burrus
Theory and Design of Adaptive Filters	M.G. Larimore, J.R. Treichler, C.R. Johnson, Jr.
Prentice-Hall	
A DSP Laboratory Using the TMS32010	T.W. Parks, D.L. Jones
Practical Approaches to Speech Coding	P. Papamichalis
Digital Signal Processing Applications with the TMS320 Family, Volume I (Floppy disk included)	K.S. Lin
First Generation TMS320 User's Guide	Texas Instruments
Second Generation TMS320 User's Guide	Texas Instruments

For ordering information, contact the publisher:

John Wiley and Sons,Inc.
605 Third Avenue
New York, NY 10158
(800) 526-5368

Prentice-Hall
Route 9W
Englewood Cliffs, NJ 07632
(201) 767-5937

7.4.1 DFT/FFT and Convolution Algorithms

DFT/FFT and Convolution Algorithms (C.S. Burrus and T.W. Parks) provides complete coverage of the theory and computation of Discrete Fourier Transforms (DFT). The three main approaches to Fast Fourier Transforms (FFT) (Cooley-Tukey, prime-factor, and Winograd) are also described in detail. TMS320 coding examples are included.

7.4.2 Digital Filter Design

Digital Filter Design (T. W. Parks and C. S. Burrus) is a comprehensive guide to digital filter design methodologies covering basic theory as well as working programs. Properties, design, approximations, and implementation of FIR and IIR filters are discussed in detail. Design examples using the TMS320 DSP are included.

7.4.3 Theory and Design of Adaptive Filters

The purpose of *Theory and Design of Adaptive Filters* (J. R. Treichler, C. R. Johnson, Jr., and M. G. Larimore) introduces the fundamental concepts, design techniques, and application guidelines of adaptive filters. This text discusses the analysis and design of the three basic classes of adaptive filters: FIR, IIR, and adaptive property restorative filters. Several TMS320 design examples are presented.

7.4.4 A Digital Signal Processing Laboratory Using the TMS32010

A Digital Signal Processing Laboratory Using the TMS32010, (D.L. Jones and T.W. Parks) is a comprehensive, self study manual that introduces students to realtime signal processing through programming of the TMS32010 DSP and use of the TMS32010 Evaluation Module (EVM) and Analog Interface Board 1 (AIB1). Examples and exercises (with solutions) are included. A demo disk from Atlanta Speech Processors Inc. (included) has been specially prepared to complement the text.

7.4.5 Practical Approaches to Speech Coding

Practical Approaches to Speech Coding (P. Papamichalis) presents a conceptual approach to speech coding techniques through practical examples of speech coding applications. Speech coding design considerations are discussed throughout the text.

7.4.6 Digital Signal Processing Applications with the TMS320 Family, Vol. I

Digital Signal Processing Applications with the TMS320 Family, Volume I (K.S. Lin, editor) is a reference guide for practicing engineers developing DSP applications. The guide consists of application reports, published articles, and technical reports covering a wide range of DSP application areas. Source code to the application algorithms is given in the text as well as on two floppy disks (included).

7.4.7 First-Generation TMS320 User's Guide

First Generation TMS320 User's Guide (Texas Instrument) is a useful reference for all the first-generation TMS320 digital signal processors. The guide introduces the TMS320 family, describes device pinouts, signals, architecture, assembly language instructions, plus software and hardware applications. Data sheets are included.

7.4.8 Second-Generation TMS320 User's Guide

Second-Generation TMS320 User's Guide is a useful reference for second-generation TMS320 digital signal processors. The guide introduces the second-generation TMS320 family, describes device pinouts, signals, and architecture, assembly language instructions, and software and hardware applications. Data sheets are included.

7.5 Technical Articles

Since the TMS32010 was disclosed in 1982, the TMS320 family has received an ever-increasing amount of recognition. The number of outside parties contributing to the extensive development support offered by Texas Instruments is rapidly growing. Many technical articles are being written about TMS320 applications in the field of digital signal processing.

The following articles and papers have been published since 1982 regarding the Texas Instruments TMS320 Digital Signal Processors. Readers who are interested in gaining further information about these processors and their applications may obtain copies of these articles/papers from their local or university library.

The articles are broken down into 12 different application categories. Articles in each category are in reverse chronological order (most recent first). Articles having the same publication date are shown in alphabetical order by authors name.

The application categories are:

1) General Purpose DSP
2) Graphics/Imaging
3) Instrumentation
4) Voice/Speech
5) Control
6) Military
7) Telecommunications
8) Automotive
9) Consumer
10) Industrial
11) Medical
12) Development Support

- **General Purpose DSP**

1) K. Rogers, "The Real-Time Thing. (Digital Signal Controller)" *Electronic Engineering Times*, (USA), No. 506, p. 85, (Oct 1988). *
2) G. Umamaheswari, C. Eswaran, A. Jhunjhunwala, "Signal Processing with a Dual-Bank Memory", *Microprocessor Microsystems*, (UK), Vol. 12, No. 4, pp. 206-210, (May 1988).
3) G. Castellini, P. Luigi, E. Liani, L. Pierucci, F. Pirri, S. Rocchi, "A Multiprocessor Structure Based on Commercial DSP", *Proceedings of ICASSP 88*, Vol. V, p. 2096, (April 1988).
4) M.R. Civanlar, R.A. Nobakht, "Optimal Pulse Shape Design Using Projections onto Convex Sets", *Proceedings of ICASSP 88*, Vol. D, p. 1874, (April 1988).
5) L.J. Eriksson, M.C. Allie, C.D. Bremigan, R.A. Greiner, "Active Noise Control Using Adaptive Digital Signal Processing", *Proceedings of ICASSP 88*, Vol. A, p. 2594, (April 1988).
6) G. Mirchandani, D.D. Ogden, "Experiments in Partitioning and Scheduling Signal Processing Algorithms for Parallel Processing", *Proceedings of ICASSP 88*, Vol. D, p. 1690, (April).
7) P. Papamichalis, "FFT Implementation on the TMS320C30", *Proceedings of ICASSP 88*, Vol. D, p. 1399, (April 1988).

8) A.C. Rotger-Mora, "An N-Dimensional SIMD Ring Architecture for Implementing Very Large Order Adaptive Digital Filters", *Proceedings of ICASSP 88*, Vol. V, p. 2140, (April 1988).

9) J. Santos, J. Parera, M. Veiga, "A Hypercube Multiprocessor for Digital Signal Processing Algorithm Research", *Proceedings of ICASSP 88*, Vol. D, p. 1698, (April 1988).

10) R. Simar, A. Davis, "The Application of High-Level Languages to Single-Chip Digital Signal Processors", *Proceedings of ICASSP 88*, Vol. D, p. 1678, (April 1988).

11) K. Bala.,"Running on Embedded Power. (Dedicated 32-Bit Microprocessors Used in New Microcontrollers)(Technology Trends: Microprocessors and Peripherals)", *Electronic Engineering Times*, (USA), No. 478, p. 34, (March 1988).

12) J. Cooper, "DSP Chip Speeds VME Transfer", *ESD, Electronic Systems Design Magazine* (USA), Vol. 18, No. 3, pp. 47,48,50,51, (March 1988).

13) L. Vieira de Sa, F. Perdigao, "A Microprocessing System for the TMS32020", *Microprocessing Microprogramming*, (Netherlands), Vol. 23, No. 1-5, pp. 221-225, (March 1988).

14) G. Wade, "Offset FFT and Its Implementation on the TMS320C25 Processor", *Microprocessing Microsystems*, (UK), Vol. 12, No. 2, pp. 76-82, (March 1988).

15) L.N. Bohs, R.C. Barr, "Real-Time Adaptive Sampling with the Fan Method", *Proceedings of the Ninth Annual Conference of the IEEE Engineering in Medicine and Biology Society*, Vol. 4, pp. 1850-1851, (Nov 1987).

16) T. Kimura, Y. Inabe, T.Hayashi, K. Uchimura, K. hamazato, " Dual-Chip SLIC Using VLSI Technology", *Conference Record of GLOBE COM Tokyo '87*, Vol.3, pp. 1766-1770, (Nov 1987).

17) W.S. Gass, R.T. Tarrant, T. Richard, B.I. Pawate, M. Gammel, P.K. Rajasekaran, R.H. Wiggins, C.D. Covington, "Multiple Digital Signal Processor Environment for Intelligent Signal Processing", *Proceedings of the IEEE*, (USA), Vol. 75, No. 9, pp. 1246-1259, (Sept 1987).

18) L. Johnson, R. Simar, Jr., "A High Speed Floating Point DSP", *Conference Record of MIDCON/87*, pp. 396-399, (Sept 1987).

19) K.S. Lin, G.A. Frantz, R. Simar, Jr., "The TMS320 Family of Digital Signal Processors", *Proceedings of the IEEE*, (USA), Vol. 75, No. 9, pp. 1143-1159, (Sept 1987).

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7.6 TMS320 Quarterly Newsletter

The TMS320 newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information. All aspects of the TMS320 family are presented including new TMS320 products, new documentation, third-party support, application boards, technical information about TMS320 products, mini application reports, development tool updates, contacts for support, design workshops, seminars, conferences, and the TMS320 university program.

To be added to the TMS320 mailing list and receive future copies of this newsletter, complete the literature request card at the back of this manual or call:

CUSTOMER RESPONSE CENTER (CRC) (800) 232-3200 X3510.

7.7 TMS320 DSP Bulletin Board Service (BBS)

The TMS320 Digital Signal Processor Bulletin Board Service is a telephone-line computer bulletin board that provides access to large amounts of information pertaining to the TMS320 family. The BBS is an excellent means of communicating specification updates for current or new TMS320 devices and development tools, and new DSP application reports as they become available. It also allows a means to trade programs with other TMS320 users.

The BBS contains TMS320 source code from the more than 1000 pages of application reports written to date. These programs include macro definitions, FFT algorithms, filter programs, ADPCM algorithms, echo cancelling, graphics, control, companding routines, and sine-wave generators.

The BBS can be accessed by users with a terminal or PC and a modem. The modem used must be able to communicate at a data rate of either 300, 1200, or 2400 bps. A character length of eight bits is required, with one stop bit and no parity. The telephone number of the bulletin board is (713) 274-2323. There is a 90-minute access limit on the bulletin board per day. The BBS is open 24 hours a day. ROM code algorithms may be submitted by secure electronic transfer via the TMS320 BBS.

To log on to the BBS, simply call the BBS using your modem. Once the connection has been established, the BBS responds by displaying a welcome message and asks for your first name, last name, and password. The user defines his or her own password the first time the BBS is accessed.

First time users of the BBS have limited access capabilities. To assure that access capabilities are increased, the first time user should answer the questionaire which is automatically displayed when the "A" command is selected from the main menu. This questionaire must be answered completely before the system operator (SYSOP) can upgrade the user id to higher access capabilities. Once the questionaire has been completed, the user id will be upgraded within 24 hours for non-restricted access to the BBS, including downloading of very useful TMS320 application programs, TMS320 updates, plus device and development tool information. Additional help about any menu may be obtained by using the "?" command.

To transfer a file from the BBS to your system, first enter the "F" (Files Area) command from the main menu. This allows access to the many files available to the BBS. To get a list and a brief description of the different file areas, enter the "A" command. Once a file area is decided upon, simply enter the appropriate number for that file area. To list the files contained in the file area, use the "F" command. Downloading of a file is done with the "D" command. Enter the "D" command and then choose the appropriate transfer protocol. The BBS supports the most popular protocols, including ASCII, XMODEM, XMODEM-CRC, ZMODEN, KERMIT, and TELINK. The BBS will then ask for a filename. Enter the filename of interest. If the MS-DOS wildcard characters "*" and "?" are used, it is possible to download several files in a row if the ZMODEM, TELINK, or KERMIT protocols are being used. Refer to the MS-DOS manual for the details on wildcard characters. Using the proper protocol, the BBS will wait for the user to start the file transfer.

To log off the BBS, use the "G" (Goodbye) command. The BBS will update your log-in data and wait for the next BBS user.

7.8 TMS320 DSP Technical Hotline

The TMS320 group at Texas Instruments offers a DSP Hotline to answer TMS320 technical questions. Specific questions regarding device problems, TMS320 development tools, third-party support, consultants, TMS320 documentation, upgrades, and new TMS320 products are handled.

To assure the maximum support from this service, first consult your product documentation. If your question is not answered there, gather all the information that applies to your problem. With your information, manuals, and products close at hand, call:

TMS320 DSP TECHNICAL HOTLINE (713) 274-2320

The TMS320 DSP Technical Hotline is open five days a week from 8:00 AM to 6:00 PM Central Time. The DSP Hotline is staffed with application engineers ready to provide the support needed for your TMS320 design or evaluation. Questions on pricing, delivery, and availability should be directed to the nearest TI Field Sales Office or:

CUSTOMER RESPONSE CENTER (CRC) (800) 232-3200 X3510

Section 8

TMS320 University Program

Texas Instruments believes it is important to provide training for future engineers and encourages universities to do advanced research in the area of DSP. To provide a university with the numerous resources that TI has to offer in the rapidly advancing field of digital signal processing, Texas Instruments has established the TMS320 University Program. The purpose of the program is to assist in incorporating the TMS320 family into electrical engineering research and course curricula. Universities have the opportunity to receive considerable cost savings and expert technical assistance. Hundreds of universities are already taking advantage of this program.

Assistance to universities through the TMS320 university program includes hardware and software price reductions, special lab package discounts, software donations, newsletter distribution, and engineering assistance in university research. TMS320 family documentation is also made available to universities.

In addition, two series of DSP textbooks, including a DSP lab manual and TMS320 User's Guides, are published to support digital signal processing research and education at the graduate and undergraduate levels.

8.1 Hardware/Software Available to Universities

TMS320 development hardware is available to universities at a discount. This includes DSP devices, the TMS320C1x Evaluation Module (EVM), the TMS320C2x SoftWare Development System (SWDS), first- and second-generation emulators (XDS/22), Analog Interface Boards (AIBs) and adapters.

Software available to universities includes TMS320 macro assemblers/linkers, simulators, the TMS320C2x and TMS320C3x C compiler packages (includes assembler/linker), and the Digital Filter Design Package (DFDP) produced by Atlanta Signal Processors Inc.. If a TI hardware tool is purchased, Texas Instruments will donate the associated assembler/linker free of charge.

8.2 DSP Station Recommendations

The **DSP lab workstation**, designed for use at the third- and fourth-year undergraduate or first-year graduate level, allows students to practice the theory learned in a DSP course. Students can design DSP systems using real-world examples and perform realtime DSP simulation. A DSP lab consists of 4 to 5 workstations. Workstations can be based on either the first- or second-generation TMS320 devices and should include the following:

Hardware:

PC or terminal
TMS320C1x EVM or TMS320C2x SWDS
Analog Interface Board (AIB)
AIB adapter (second-generation only)

Software:

TMS320C1x or TMS320C2x Assembler/Linker
TMS320C1x or TMS320C2x Simulator
Digital Filter Design Package (DFDP)
TMS320C2x C compiler package (second-generation only)

The following textbooks are recommended for first- and second-generation workstations:

- *First-Generation TMS320 User's Guide* (Prentice-Hall)
- *Second-Generation TMS320 User's Guide* (Prentice-Hall)
- Lab Manual: *A Digital Signal Processing Laboratory Using the TMS32010* , by Parks and Jones (Prentice-Hall)

Additional TMS320 DSP textbooks are available to further enhance the workstation.

8.3 DSP Research Workstation

A **DSP research station** is created by adding the following equipment to the DSP workstation:

Hardware:

TMS320C1x or TMS320C2x Emulator (XDS/22), TMS320C3x XDS500 Emulator or TMS320C3x XDS1000 Development Environment

Software:

DSP Software Library
TMS320C3x Assembler/Linker
TMS320C3x Simulator
TMS320C2x C compiler package
TMS320C3x C compiler package

The following documentation is recommended if the XDS500 or XDS1000 is selected for the research workstation:

- *Third-Generation TMS320 User's Guide*

Following the establishment of the DSP workstation or DSP research station, Texas Instruments will provide continued support to the university in the form of suggestions for DSP projects, up-to-date documentation, TMS320 Bulletin Board Service (BBS), hotline, newsletter, and the upgrade of TMS320 software and hardware with the latest version or generation.

For more information about the university program and associated pricing, contact the nearest TI Field Sales Office (listed in the back of this document) or write directly to:

University Program
Texas Instruments Incorporated
P.O. Box 655303 M/S 8338
Dallas, TX 75265
Phone (713) 274-2320

In Europe, contact:

Texas Instruments France
Boite Postale 5
06270 Villeneuve-Loubet
Nice, France
Attn: TMS320 University Program

In the Far East, contact:

Texas Instruments Japan Limited
MOS Logic Product Marketing
MS Shibaura Bldg
13 - 23, Shibaura 4-Chome
Minato-Ku
Tokyo 108, Japan
Phone: 03-769-8735

Note:

Texas Instruments reserves the right to make changes at any time in its TMS320 University Program policies.

Section 9

TMS320 Third-Party Support

The TMS320 family of digital signal processors is supported by product and service offerings from many independent vendors and consultants, known as third parties. These support products take many forms (both software and hardware) from cross assemblers, simulators, and DSP utility packages to logic analyzers and emulators. The expertise of those involved in support services ranges from speech encoding and vector quantization to software/hardware design and system analysis.

This section describes a number of tools and services that augment the TMS320 support provided by Texas Instruments. Inclusion of a product in this section does not constitute product endorsement on the part of Texas Instruments, but merely an attempt at product awareness. The products listed here are representative of independent vendor-supplied products that support the TMS320 family, and are not intended to be an all-inclusive list of independent vendor-supplied support tools. Many other products offered by third parties are not included in this document since they do not directly support the TMS320 family. If more information is desired about a product line, the third party can be contacted directly.

The information on the products presented in this section is based on that provided by the third party. All third parties were afforded the opportunity to submit information and encouraged to include photos. Due to space limitations, only a synopsis of each product is presented. Further information about a product may be obtained by contacting the third party directly. An attempt has been made to identify all trademarks and list them at the end of this section; any omissions have occurred inadvertently.

In addition to the third-party product descriptions, the following lists are provided:

- Third-Party Name, Address, and Phone Number (Section 9.1 on page 9-3)
- Third-Party Support Product Tables (Section 9.2 on page 9-8)
- Third-Party Support Product Descriptions (Section 9.3 on page 9-18)
- Third-Party Consultants (Section 9.4 on page 9-145)
- Trademarks (Section 9.5 on page 9-150)

All third parties are listed alphabetically in the first list (Name, Address, and Phone Number). They are broken down by product in the second set of lists (Product Tables). If they supply a product, they are broken into three categories (North America, the Far East, and Europe). Within each category, they

are listed alphabetically. If they supply a service, they are listed in the fourth subgrouping (Consultants), which is broken down into six geographic areas of North America (Eastern, Central, Mountain, Pacific SW, Pacific NW, and Canada), the Far East, and Europe. In each of the consultant geographic area lists, they are listed alphabetically and their area of expertise is given (if known).

A third party requesting to be included in updated versions of this document or in the quarterly newsletter may send the name, address, phone number, and information about the TMS320 development support to:

Texas Instruments Incorporated
P.O. Box 1443, MS 737
Houston, Texas 77001

Attn: TMS320 Marketing Third-Party Coordinator

9.1 Third-Party Name, Address, and Phone Number

Table 9-1 lists all the third parties mentioned in this section who provide a TMS320 support product. This is a comprehensive reference list that gives the company names, addresses, and phone numbers.

Table 9-1. Third-Party Name Address and Phone Number

COMPANY/ADDRESS/PHONE	COMPANY/ADDRESS/PHONE
Advanced Digitial Systems Industries Ltd 16/f Hong Kong Industrial and Commercial Bank Bldg 99-105 Des Voeux Rd. Central Hong Kong 5-448289	**AI/Ware Inc** 11000 Cedar Ave Suite 212 Cleveland,OH 44106 216-421-2380
Allen Ashley 395 Sierra Madre Villa Pasadena, CA 91107-2902 818-793-5748	**Ariel Corp** 433 River Road Highland Park, NJ 09804 201-249-2900
ASR International 1-19-9 Toranomon, Minato-Ku Tokyo, Japan 105 03-502-5550	**Athena Group Inc** 3424 N.W. 31st St Gainesville, FL 32605 904-371-2567
Atlanta Signal Processors, Inc 770 Spring St Atlanta, GA 30308 404-892-7265	**Avocet Systems** 120 Union St P.O. Box 490 Rockport, ME 04856 800-448-8500
Bedford Research 19 Crosby Drive Bedford, MA 01730 617-275-7246	**Burr-Brown Corp** P.O. Box 11400 Tucson, AZ 85734 602-746-1111
Burr-Brown Japan 6-14-15 Akasaka, Minato-Ku Tokyo, Japan 107 03-586-8141	**CGA Corporation** 3-22-8 Meieki, Nakamura-Ku Nagoya-City, Japan 450 052-561-6325
Chubu Denki 3-2-8 Tadaoki, Toyohashi-City Aichi-Pref, Japan 440 0532-61-9566	**Comdisco** 101 California St 38th Floor San Francisco, CA 94111 415-421-1800
Computalker Consultants 1119 Colorado Ave Santa Monica, CA 90401 213-393-7781	**Computer Solutions Ltd** Canada Road, Byfleet Surrey KT147HQ 09323-52744
Cybernetic Micro Systems P.O. Box 3000 San Gregorio, CA 94070 415-726-3000	**Daisy Systems Corp** 700 Middlefield Rd Mountainview, CA 94039 415-960-0123

Table 9-1. Third-Party Name Address and Phone Number (Continued)

COMPANY/ADDRESS/PHONE	COMPANY/ADDRESS/PHONE
Dalanco Spry 89 Westland Ave Rochester, NY 14618 716-473-3610	**Digital Audio Corp** 6512 Six Forks Rd Suite 203B Raleigh, NC 27615-6525 919-848-0845
Digital Signal Processing Software Inc (DSPS Inc) P.O. Box 5348 Station F Ottawa K2C3J1 613-825-5476	**Digital Sound Corp** 2030 Alameda Padre Serra Santa Barbara, CA 93103 805-569-0700
Discrete TimeSystems, Inc. 511 West Golf Road Arlington Heights, IL 60005 312-439-1335	**Distec Hard Und Software GMBH** Systeme Fur Digitale Signalverbeitung Robert-Bosch-Briete 3400 Goettingen, W. Germany 0551-65068 0551-65069
dSpace An der Schonen Aussicht 2 D-4790 Paderborn, W. Germany 05251-65074	**DSP Development Corp** One Kendall Square Cambridge, MA 02139 617-577-1133
The DSP Group Inc 1900 Powell St Suite 1120 Emeryville, CA 94608 415-655-7311	**DSP Technology Corp** 1325 Capitol Parkway Carrollton, TX 75006 214-245-8831
DSP Technology Inc 48500 Kato Rd Fremont, CA 94538 415-657-7555	**E I A** 236 Ave Victor Hugo 92140 Clamart France 46-44-63-49
Electro Rent 4209 Vanowen Place Burbank, CA 95105 800-423-2337 (outside CA) 800-232-2173 (CA only)	**Emona Enterprises Pty Ltd** 86 Parramatta Rd Camperdown N.S.W. 2050 Australia 02-519-3933
EMU-SYS Inc. 1313 Fifth Street, SE Minneapolis, MN 55414 612-379-3888	**Ensigma Ltd** Archway House Welsh Street Chepstow Gwent MP6 5LL, UK 02912-5422
FACs Inc Engineering Services 7031 Orchard Lake Rd Suite 303 West Bloomfield, MI 48322 313-737-0490	**FORTH Inc** 111 N. Sepulveda Blvd Manhattan Beach, CA 90266 213-372-8493

Table 9-1. Third-Party Name Address and Phone Number (Continued)

COMPANY/ADDRESS/PHONE	COMPANY/ADDRESS/PHONE
Fuchs Messetechnik GMBH Am Eichpoldlveda Blvd 17-8026 Bruchmuel, W. Germany 08062-1716	**Gas Light Software** 5211 Yarwell Houston, TX 77096 713-729-1257
Hewlett-Packard 8245 N. Union Blvd Colorado Springs, CO 80901-0617 800-447-3282	**Hyperception** 9550 Skillman LB 125 Dallas, TX 75243 214-343-8525
Intelligent Instrumentation Products Burr-Brown Corporation 1141 W. Grant Rd., #131 Tucson, AZ 85705 602-746-1111	**Joyce-Loebl Ltd** Dukesway, Team Valley Gateshead NE110PZ Great Britain 091-482-2111
Kay Elemetrics 12 Maple Ave Pine Brook, NJ 07058 201-227-2000	**Kontron Electronics** 630 Clyde Ave Mountainview, CA 94039-7230 800-227-8834
Logic Automation 19500 N.W. Gibbs Drive P.O. Box 310 Beaverton, OR 97075 503-690-6900	**Loughborough Sound Images Ltd** The Technology Centre Epinal Way, Loughborough Leics, England LE110QE 0509-231843
Macrochip Research Inc. 1301 Denton Drive Suite 204 Carrollton, TX 75006 214-446-9906	**Mathematical Systems Design, Inc** 11835 W. Olympic Blvd Suite 745 Los Angleles, CA 90064 213-479-7180
Metme Corp 4623 Morganford St. Louis, MO 63116 800-423-8387	**MicroCraft Corp** P.O. Box 513 Thiensville, WI 53092 414-241-8144
Micro WorkShop Inc 3340 Veterans Hwy Bohemia, NY 11716 516-737-5600	**Momentum Data Systems** 1666 Newport Blvd., #115 Costa Mesa, CA 92627 714-548-3257
MTT Corporation 1-19-6 Nishi-Shinjuku, Shinjuku-Ku Tokyo, Japan 160 03-348-8301	**Navtrol Company Inc.** 9204 Markville Dr Dallas, TX 75243 214-234-3319
OROS Chemin Des Pres-Zirst 38240 Meylan, France 76-90-62-36	**PC Electronics a.s.** P.O. Box 60 5578 Nedre Vats Norway 47-4-76-52-80
Pentek 10 Volvo Drive Rockleigh, NJ 07647 201-767-7100	**Pratica SRL** Via Valeggio, 18 Torino, IT I10128 11-503427-592989

Table 9-1. Third-Party Name Address and Phone Number (Continued)

COMPANY/ADDRESS/PHONE	COMPANY/ADDRESS/PHONE
Qualcomm Inc 10555 Sorrento Valley Rd San Diego, CA 92121 619-587-1121	**Racal Microelectronics Systems Ltd** Worton Grange Worton Grange Industrial Estates Reading, Berkshire England RG20SB 44-734-868601
Rapid Systems Inc 433 N. 34th St Seattle, WA 98103 206-547-8311	**Sarin** P.O. Box 36065 Baltimore, MD 21286 301-485-9529
Schlumberger Technologies 1601 Technology Drive San Jose, CA 95115 408-947-3626	**Signal Technology Inc** 5951 Encina Rd Goleta, CA 93117 800-235-5787
Signatec 357 Sheridan St., Suite 119 Corona, CA 91720 714-734-3001	**Signix Corp** 19 Pelham Island Rd Wayland, MA 01778 508-358-5955
Signum Systems 1820 14th St Santa Monica, CA 90404 213-450-6096	**Sky Computers** Foot of John St Lowell, MA 01852 617-454-6200
Sonitech International Inc 83 Fullerbrook Rd Wellesley, MA 02181 617-454-6200	**Spectron MicroSystems Inc** 600 Ward Drive Santa Barbara, CA 93111 805-967-0503
Spectrum Signal Processing 264 'H' Street P.O. Box 8110-25 Blaine, WA 98230 800-323-1842 (U.S.) 800-663-8986 (Canada)	**Structured Electronic Systems Inc** 650 Red Oak Lane Rochester, MI 48063 313-652-4809
Symmetric Research 15 Central Way Suite 9 Kirkland, WA 98033 206-828-6560	**System Engineering Corp** 2143 Sugao Kawasaki-City, Kanagawa-Ken 044-976-7743
Tartan Laboratories 461 Melwood Ave Pittsburgh, PA 15213 412-621-2210	**Teknic, Inc** 214 Andrews St Rochester, NY 14604 716-546-3212

Table 9-1. Third-Party Name Address and Phone Number (Concluded)

COMPANY/ADDRESS/PHONE	COMPANY/ADDRESS/PHONE
Tektronix 800-245-2036	**Telephoto Communications** 11722 Sorrento Valley Suite D San Diego, CA 92121-1084 619-452-0903
Televic Leo Bekaertlann 1 B-8701 Izegem Belgium 32-51-30-30-45	**Televic U.S. Representative** **Alante Corp** Suite 3210 5201 Great America Pkwy Santa Clara, CA 95054
Texas Instruments 800-527-3500	**TIAC Systems Inc** 3080 Spring St. Port Moody, B.C. Canada V3H1Z8 800-663-8710
Ultra Digital Systems 2 Ambercromby Square P.O. Box 147 Liverpool, England L693BX 051-708-9465	**Valid Logic Systems** 2820 Orchard Parkway San Jose, CA 95134 408-432-9400
Votan 4487 Technology Drive Fremont, CA 94538 415-490-7600	**Whitman Engineering** P.O. Box 9675 Fort Collin, CO 80525 303-493-2210
XCOM Zac Le Pre Milliet Montbonnett, St Martin France 76-52-00-46	

9.2 Third-Party Support Product Tables

These tables are a quick-reference listing of the third parties according to first-, second-, or third-generation products and the software operating systems and product types available.

To locate a particular software product using these tables, use the following sequence:

1) Locate the desired TMS320 generation heading in the tables.
2) Identify the appropriate tool type (i.e., application hardware, emulator, etc.).
3) Scan the vertical column listing for the desired functional system (i.e., PC, PDP-11, etc.), and locate the third party or parties offering that product.
4) Refer to Section 9.3 (starting on page 9-18) for a description of the product(s) of interest. The products are listed alphabetically by third-party name.
5) Refer to Section 9.1 (starting on page 9-3) for the address and phone number of the third-party offering the selected product.

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ALGORITHM DEVELOPMENT HARDWARE

	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
Advanced Digital Systems Industries Ltd	•																			
ASR International	•							•								•				
Atlanta Signal Processors Inc	•																			
Burr Brown Corp														•						
Chubu Denki Corp.																				•
Cybernetic MicroSystems																				•
Dalanco Spry	•																			
Digital Sound Corp								•						•		•	•	•		
Emona Enterprises Pty Ltd																				•
Hyperception																				•
Kontron Electronics																				•
Loughborough Sound Images	•																			
Microcraft Corp	•																			
Qualcomm																				•
Sarin	•																			
Schlumberger Technologies																				•
Sky Computers	•							•								•				
Sonitech Int'l Inc	•																			
Spectrum Signal Processing	•																			•
Structured Electronics Systems Inc																				•
Teknic Inc																				•
Tektronix																				•
Texas Instruments†	•																			•
TIAC Systems Inc	•																			•
Ultra Digital Systems	•						•													•

EMULATOR (IN-CIRCUIT)

	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
dSpace	•																			•
Electro-Rent	•	•	•	•		•	•	•	•			•	•	•	•	•				
Loughborough Sound Images	•																			
Macrochip Research Inc.	•		•				•													
MicroWorkshop Inc‡	•																			
Signum Systems	•																			
Spectrum Signal Processing	•																			
Texas Instruments†	•	•	•	•		•	•	•	•			•	•	•	•	•				

† *Refer to Section 5 for description.*

‡ *Numeric Data Processor may be required.*

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ASSEMBLER/LINKER

	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Allen Ashley	•											•			
ASR International	•								•						
Avocet Systems	•														
Computalker Consultants	•							•				•	•		
Cybernetic Micro Systems	•														
DSPS Inc.	•		•						•						
Loughborough Sound Images	•														
Microcraft Corp	•														
Practica SRL	•		•						•	•					•
Sarin	•														
Sky Computer	•								•						
Spectrum Signal Processing	•														
Televic	•		•												
Texas Instruments†	•	•	•	•											
Ultra Digital Systems	•						•								•

SIMULATOR

	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Allen Ashley	•														
Avocet Systems	•														
Computalker Consultants	•							•				•			
Loughborough Sound Images	•														
Sarin	•														
Spectrum Signal Processing	•														
Texas Instruments‡	•		•												
Ultra Digital Systems	•						•								•
Valid Logic Systems		•	•												

HIGH LEVEL LANGUAGE COMPILER

	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
ASR International (C language)	•							•							
Computalker Consultants (SPL language)	•														
Televic (Pascal language)	•		•												
Sky Computer (C language)	•							•							

† *Refer to Section 4 for description.*

‡ *Refer to Section 5 for description.*

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ALGORITHM DEVELOPMENT SOFTWARE	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Athena Group	•														•
Atlanta Signal Processors Inc	•														•
Bedford Research	•		•					•							
Burr Brown															•
Chubu Denki Corp															•
Comdisco			•			•									•
Daisy Systems Corp	•														•
dSpace	•														
DSP Development Corp	•	•	•		•										•
DSPS Inc	•		•					•							
Gas Light Software†	•														
Hyperception	•														
Loughborough Sound Images	•														
Microcraft Corp	•														
Momentum Data Systems	•														
Practica SRL	•		•			•		•	•					•	•
Sarin	•														
Signal Technology Inc	•		•			•		•	•	•					
Signix Corp†	•														
Sonitech Int'l Inc	•														
Televic	•		•												
TIAC Systems Inc	•														
Whitman Engineering†	•														

†*Numeric Data Processor may be required.*

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ALGORITHM DEVELOPMENT HARDWARE	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
ASR International														•						
Ariel Corp	•																			
Atlanta Signal Processors Inc	•																			
CGA Corporation																				•
Burr Brown Corp		•												•						
Computer Solutions Ltd	•																			
Chubu Denki	•													•						•
Dalanco Spry	•																			
dSpace	•																			
DSP Technology Inc																				•
FACs Inc																				•
Forth Inc	•																			
Hewlett Packard																				•
Hyperception																				•
Intelligent Instrumentation Products	•																			
Loughborough Sound Images	•																			
Metme Corp	•																			
Microcraft Corp	•																			
MTT Corporation	•													•						•
Navtrol Company Inc.	•																			
PC Electronics a.s.	•																			
Pentek														•	•					
Qualcomm																				•
Racal Microelectronics Systems Ltd														•						
Signatec	•																			
Schlumberger Technologies																				•
Sky Computers														•						
Sonitech Int'l Inc	•																			
Spectrum Signal Processing	•																			
Symmetric Research	•																			
System Engineering Corp																				•
Tektronix																				•
Telephoto Communications	•																			
Texas Instruments†	•																			
TIAC Systems Inc	•																			

EMULATOR (IN-CIRCUIT)	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
Electro-Rent	•	•	•	•		•	•	•	•			•	•	•	•	•				
Hewlett-Packard	•				•															
Macrochip Research Inc.	•		•				•													
Texas Instruments†	•	•	•	•		•	•	•	•			•	•	•	•	•				

† *Refer to Section 5 for description.*

TMS320C2x

ASSEMBLER/LINKER	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Allen Ashley	•														
Ariel Corp	•														
ASR International	•	•													•
Avocet Systems	•					•									
Computalker Consultants	•							•				•	•		
Forth Inc	•														
Hewlett-Packard	•				•										
MTT Corporation	•														•
Sky Computer	•	•													•
Spectrum Signal Processing	•														
Symmetric Research	•														
Televic	•		•												
Texas Instruments†	•	•	•	•											

SIMULATOR	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Avocet Systems	•														
MTT Corporation	•														•
Texas Instruments†	•		•												
Valid Logic Systems		•	•												

HIGH LEVEL LANGUAGE COMPILER	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
ASR International (C language)	•	•													•
CGA Corporation (C language)															•
Computalker Consultants (SPL language)	•														
Computer Solutions Ltd. (Forth langauge)	•														
Forth Inc (Forth language)	•														
Joyce-Loebl Ltd (Pascal language)	•														
Loughborough Sound Images (C language)	•														
Sky Computers (C language)	•	•													•
Spectrum Signal Processing (C language)	•														
Televic (Pascal language)	•		•												
Texas Instruments† (C language)	•	•	•	•											

† *Refer to Section 5 for description.*

TMS320C2x

ALGORITHM DEVELOPMENT SOFTWARE	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMB Bus	Apollo	Other
Ariel Corp	•																
Atlanta Signal Processors Inc	•																•
Athena Group Inc.	•																•
Bedford Research	•		•						•								
Burr Brown																	•
CGA Corporation																	•
Comdisco			•			•											
Daisy Systems Corp	•																•
dSpace	•																
DSP Development Corp	•	•															•
Forth Inc	•																
Hyperception	•																
Intelligent Instrumentation Products	•																
Logic Automation		•	•													•	
Loughborough Sound Images	•																
Metme	•																
Microcraft Corp	•																
Momentum Data Systems	•																
MTT Corporation	•													•			•
Pentek	•																•
Signatec	•																
Signix Corp†	•																
Sonitech Int'l Inc	•																
Spectrum Signal Processing	•																
TIAC Systems Inc	•																
Whitman Engineering†	•																

†*Numeric Data Processor may be required.*

TMS320C3x

ASSEMBLER/LINKER	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Texas Instruments†	•	•	•	•											

SIMULATOR	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Spectron MicroSystems Inc		•													
Texas Instruments†	•		•	•											
Valid Logic Systems		•	•												

HIGH LEVEL LANGUAGE COMPILER	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	Other
Tartan (ADA compiler)			•												
Texas Instruments (C compiler)†	•	•	•	•											

ALGORITHM DEVELOPMENT HARDWARE	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
Atlanta Signal Processors	•																			
Hyperception																				•
Qualcomm																				•
Spectrum Signal Processing	•																			
Sonitech Int'l	•																			

† *Refer to Section 4 for description.*

TMS320C3x

EMULATOR (IN-CIRCUIT)	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
Texas Instruments‡	•																			

ALGORITHM DEVELOPMENT SOFTWARE	PC	Sun-3 UNIX	VAX VMS	VAX Ultrix	HP	UNIX	MacIntosh	Apple II	PDP-11	RSX-11M	RT-11	CP/M-80	Amiga	Att 3B2	VMEbus	Multibus	Q-Bus	SCSI Bus	Unibus	Other
Athena Group Inc.	•																			•
Atlanta Signal Processors Inc.	•																			•
DSP Development Corp	•	•			•															•
Hyperception	•																			
Signix Corp§	•																			
Sonitech International Inc.	•																			
Spectron MicroSystems Inc.	•	•	•																	

§ *Numeric Data Processor may be required.*

‡ *Refer to Section 5 for description.*

TMS320 FAMILY
APPLICATION HARDWARE

	Audio	Analog I/O Control	FFT	Signal Processing	Speech	Video
AI/Ware			•			
Digital Audio Corp				•	•	
Discrete Timesystems Inc						•
DSP Group Inc					•	
dSpace		•				
DSP Technology Corp	•				•	
Joyce-Loebl Ltd				•		•
Kay Elemetrics				•		
Mathematical Systems Design		•		•		
Metme Corp				•		
Rapid Systems			•	•		
Texas Instruments					•	
Votan					•	

9.3 Third-Party Support Product Descriptions

This section lists third-party manufacturers and suppliers alphabetically by name, with their current products described on the page(s) devoted to that third-party. The listing is broken into three geographic areas: North America (the U.S. and Canada), the Far East, and Europe.

NORTH AMERICA

9.3.1 AI/Ware

Nature of Product(s): Application Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- MSP320

  With an on-board TMS32010 DSP, the MSP320 handles realtime processing in demanding instrumentation and control environments. It plugs directly into a single slot of an IBM PC and can compute a 1024-point complex FFT in under 70-ms. A standard library of signal-processing functions included with the board covers FFT, IFFT, power spectrum, digital filtering, missing data fill-in, and signal generation.

  An optional software program, called the **Signal Viewer**, operates as a post-processing data analyzer running under Microsoft Windows and is an interface to the MSP320 signal processing board.

9.3.2 Allen Ashley

Nature of Product(s): Assembler, Simulator, Disassembler
Functional System(s): IBM PC, CP/M-80
Device(s) Supported: TMS32010, TMS32020/C25

- MAC320 and MAC32020 Macro Assembler for TMS32010 and TMS32020/C25

  MAC320 enables any IBM/PC-DOS system to serve as a development station for the TMS32010. MAC32020 serves the same purpose for the TMS32020/C25. The software system features a macro assembler, cross-reference generator, hex file converter, screen editor, and offloading facilities. The assembler mnemonics adhere to the assembly language defined by Texas Instruments. The macro assembler includes full macro and conditional assembly features, as well as the ability to chain a series of source files together during a single assembly. Note that programs developed under MAC320 must be offloaded to the target processor for testing. A user-configurable downloader is provided, as well as a downloader configured specifically for the XDS development module. MAC320 and MAC32020 are available on IBM/PC-DOS or MS-DOS 8" (NEC APC) disks.

- SYSTEM-320 Macro Assembler for the TMS32010

  SYSTEM-320 operates under CP/M-80. It includes an interactive assembler/editor, macro assembler, text editor, cross-reference generator, and offloading facilities. The interactive assembler/editor is intended for the rapid creation, modification, storage, and testing of shorter programs or program modules. The macro assembler includes full macro and conditional assembly features, as well as the ability to chain a series of source files together during a single assembly. Facilities are provided to off-load the developed program as a direct transfer from memory, via a byte stream over a CPU port, or via COM or ·HEX files. An offloader for ·HEX files is included, as well as a downloader for the XDS development module. SYSTEM-320 is available on 8" SSSD disk or on a variety of 5-1/4" disk formats.

- DASM320 Disassembler for TMS32010

  This disassembler is available for the IBM/PC-DOS. It converts existing machine code into an assembly language source file for modification. The DASM320 features mnemonic disassembly with user-defined symbols and data areas. The disassembly produces an ASCII text source file suitable for input to the MAC320 cross assembler. It is provided on a 5-1/4" PC-DOS disk.

- EMU320 Simulator for TMS32010

  The EMU320 emulator is available for IBM/PC-DOS or IBM-compatible microcomputers. In conjunction with the MAC320 cross assembler, the EMU320 emulator provides a development environment for the creation and simulated execution of programs for the TMS32010 processor. The EMU320 features an inline assembler, up to 10 breakpoints, 64K program space, address trapping, single-step or free-run operation, mne-

monic instruction disassembly, symbolic debugging, and trace operation. Interrupts are not implemented, and the simulator is not optimized for testing I/O-intensive programs. The strength of the simulator lies in the representation and control of program logic. EMU320 provides an inexpensive alternative/adjunct to hardware emulation. It is available on IBM/PC-DOS 5-1/4" disk.

9.3.3 Ariel Corporation

Nature of Product(s): Assembler, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- DSP-16

  A single board data acquisition processor and development system for the IBM PC. This 16 bit integer processor (see Figure 9-1) has a maximum sample rate of 50 kHz on two channels for input and output, for a maximum aggregate of 200 kHz. Based on the TMS32020 or optional TMS320C25 DSP, the DSP-16 provides complete program development software, supporting a number of common languages. This allows the user or a third-party to modify the system to meet custom requirements.

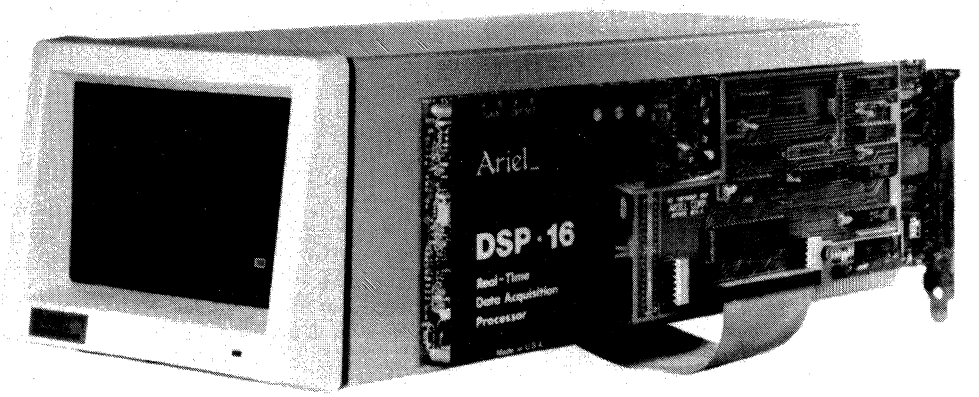

Figure 9-1. DSP-16 Algorithm Development Board from Ariel

- DSP-C25

  The DSP-C25 is based on a full-speed implementation of the TMS320C25. It may be used alone as a high-speed coprocessor/development system, or multiple boards may be linked via the TMS320C25 serial I/O channel. The outside world is accessible by a 16-bit bidirectional parallel data port. The port may be configured for

single or multiple port operation. In single mode, the port connector may be connected directly to 16 bits of external I/O via a ribbon cable or piggyback board. In multiple I/O mode, up to eight additional 16 bit I/O ports may be interfaced by adding additional circuitry to a piggyback board mounted on top of the DSP-C25.

An optional single-chip analog I/O, the TLC32040, is also available for plug-in installation. It gives concurrent input and output, built-in gain and sample rate selection, and tracking anti-alias filters in a single component.

The DSP-C25 is host interface compatible with the DSP-16, the full featured TMS320 development system with high-speed 16-bit analog I/O. The DSP-C25 provides general purpose serial and parallel I/O instead of the DSP-16's analog subsystem and buffer memory. In return, the DSP-C25 supports a full complement of zero wait-state memory, up to 256K-bytes. 16K-bytes of shared program/data RAM is standard, and RAM upgrades can be added at any time.

For program development, the DSP-C25 supports **ASM-320**, a TMS320 macro assembler, and **PDS-320**, a TMS320 Program Development System (description of these two products follow this product).

The DSP-C25 fits in a single full-size PC slot. DIP switches select the host I/O addresses and memory page used.

- ASM-320

  The ASM-320 is a high-performance, easy to use Macro Assembler for the TMS32020 or TMS320C25 DSP chips. The ASM-320 can be used with any IBM PC or compatible. ASM-320 generates hex files that are suitable for uploading to the DSP-16 or DSP-C25 boards. Additional utilities are provided to convert hex files to TI tagged format for downloading, or to binary files suitable for many EPROM programmers. The microprocessor instruction mnemonics (opcodes) adhere to those used by TI. The pseudo-operations, or assembler directives do not, as a rule, follow those defined by TI. ASM-320 is an absolute assembler, so no extra linking step is required. All ASM-320 commands and options are controlled by command line flags, simplifying batch mode operation.

- PDS-320

  The TMS320 Program Development System is included with the DSP-16, optional with the DSP-C25. It includes the ASM-320 assembler, DSP-BUG: an interactive monitor/debugger, the **PC/SAMPLER**, and high-level language support for the DSP-16 or DSP-C25 PC interface. DSP-BUG is a window oriented realtime debugger. It includes commands to move data, manipulate registers, acquire data and output data in realtime, reverse assemble, and patch assemble. PC/SAMPLER is a set of five complete applications for the DSP-16. The samplers are: Data Acquisition/Display, Digital Audio Effects, Digital Storage Oscilloscope, Loop Editor, and Waveform Synthesizer. The sampler programs are written in TMS320 assembly language and Microsoft C. All source code is included. PDS-320 provides complete high-level language support for the DSP-16 and DSP-C25, with linkable libraries and ex-

amples for over 15 languages and memory models. Interpreted and compiled BASIC, C, Pascal, Turbo Pascal, FORTRAN, and more are supported. Source code for all drivers is supplied.

9.3.4 Athena Group Inc.

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC, PS/2
Device(s) Supported: TMS320 family

- Monarch

  Monarch is a comprehensive, state-of-the-art DSP software package that meets all the user's design and simulation needs for all three generations of the TMS320. Monarch operates on IBM PC or PS/2 with 640K-bytes memory and either dual floppies or single floppy with hard disk. It takes a user-specified signal or filter from definition and analysis to implementation. Monarch's integrated system expands to include DSP microprocessor support and specialized enhancement tools.

  Monarch designs classic, modern, and arbitrary filters with 3 FIRs, 4 IIRs, State-Variable modeling and 4 Architectures. Designs are double-precision fixed-point and floating-point, with binary-point assistance for fixed-point.

  Monarch's signal laboratory (SIGLAB) is a unique interpretative language that eliminates weeks of tedious programming. With just a few simple commands, Monarch's built-in technology simulates and analyzes your signals instantly. It can display a virtually unlimited number of signals with SIGLAB's oscilloscope emulation.

  Monarch's 2-D and 3-D graphics are clean, clear, and easy-to-use. The user can monitor each step of the design process with options including zoom, color overlay, pole-zero, schematic diagram, data-point extraction, and more. It is possible to display up to six 2-D signals and spectra simultaneously and up to sixteen 3-D graphs as a true 3-D waterfall display with user-selectable angle and viewpoint.

  There are enhancement packages available which include Architectures, Spectral Analysis, Optional Filters, and Systems and Microprocessor Support.

9.3.5 Atlanta Signal Processors, Inc. (ASPI)

Nature of Product(s): Algorithm Development Software, Algorithm Development Hardware
Functional System(s): IBM PC/XT/AT, BIOS-compatibles
Device(s) Supported: TMS32010, TMS320C15, TMS320C17, TMS32020, TMS320C25, TMS320C30

- Digital Filter Design Package (DFDP)

  ASPI's Digital Filter Design Package (DFDP), operating on the IBM PC and BIOS, is a DSP software tool that supports the design of floating-point and fixed-point digital filters, including multiband filters, Hilbert transformers, and differentiators. Coefficients are provided for filter implementation using any CPU with signal-processing capability. The coefficient file may be converted to TMS320 assembly code using the Code Generator (CGEN) design module of the package.

  The CGEN, designed for use with the DFDP, automatically generates assembly language programs for the realization of digital filters on all three generations of the TMS320 family. See Section 4.5 for a more detailed description of the DFDP.

- Algorithm Development Package (ADP)

  The ASPI Algorithm Development Package (ADP) places a highly controlled algorithm development environment in an IBM PC. Single-channel analog data input and output plus direct access to selected data, address, and control lines are available to the developer. Integrated development software provides an engineer with the tools to perform complete algorithm development on the TMS32010 and TMS32020.

  The PC-bus resident hardware component of the Algorithm Development Package incorporates a TMS32010 or TMS32020 along with analog-to-digital and digital-to-analog conversion. A programmable clock, digital I/O, external flag and interrupt, synchronization, and (for TMS32020) serial port access are provided.

  The TMS32010 is supported with 4K words of dual-ported program memory; the TMS32020 is supported with up to 64K words of program memory and up to 64K words of data memory. Dual-ported program memory and utilities included in the package allow multiple-location algorithm changes. The absence of predetermined frequency roll-off characteristics has allowed the ADP to be used in applications such as control, signal simulation, signal analysis, medical instrumentation, and speech.

- Realtime Subband Coder Algorithm

  ASPI offers a full-duplex 16-kbit/s subband coder that can be implemented using a single TMS32010 (without external program memory) with a 1K-word off-chip RAM data buffer. Because of the compactness of the subband coding, it only requires 80 percent of the TMS32010 CPU utilization, thus allowing the processor to perform other tasks in addition to speech coding.

This realtime speech compression algorithm can be used in many applications, such as telecommunications and computers, which require high-quality voice response, medium-bit-rate digital voice transmission, digital radio, and secure communications. The subband coder provides an efficient tradeoff between speech quality and data rate. In addition, the use of a single TMS32010 coder allows a cost-effective system implementation.

- 320/PC Development System

  The 320/PC, together with the 320/PC-20 daughter board, converts the ADP for the TMS32010 into a full-fledged development system for the TMS32020. The 320/PC-20 daughter board plugs into the TMS32010 socket on the 320/PC board, so the same hardware/software system can be used to develop TMS32010 and TMS32020 programs.

  The **320/PC-C25 daughter board** plugs directly into the ADP 320/PC board offering a complete development system for the TMS320C25. The PC/320-C25 daughter board can access up to 128K-bytes of both program and data memory. A high-accuracy 12-bit linear A/D and D/A converter is included. Common clock and reset provisions accomodate multiprocessing. A parallel I/O expansion connector on the I/O expansion connector on the ADP 320/PC mother board allows for communication with custom I/O devices. Extensive software simplifies and expedites algorithm development.

  The **320/PC-15 mother board** plugs directly into the PC and offer a complete development system for the TMS320C15. The 320/PC-17 plugs into the 320/PC-10 or 320/PC-15 motherboard offering development support for the TMS320C17. The TMS320C15 and TMS320C17 are spinoffs of the industry-standard TMS320C10 with a 256-word RAM and a 4K-word ROM. The TMS320C17 also features a serial port and on-chip companding hardware.

- TMS320C25 Chimera System

  The TMS320C25 Chimera System is an IBM PC/AT board designed for prototyping, development, or applications with the TMS320C25 DSP. The mother/daughterboard architecture allows use of the Chimera in numerous custom and OEM systems in addition to DSP algorithm and program development. A user may use the basic Chimera system, a custom daughterboard, an ASPI daughterboard, or a custom interface using ASPI's wirewrap daughterboard. The hardware and software are designed for multiprocessor operation allowing up to 16 Chimera boards per host. An on-board TLC320C40 analog interface chip option offers a low cost A/D and D/A solution. The basic Chimera system comes with 32K-bytes of memory and development software, one of the options being the addition of A/D -D/A and 64K-byte pingpong buffer to the daughterboard.

- TMS320C30 Banshee System

  The TMS320C30 Banshee System (see Figure 9-2) is a IBM PC/AT board for algorithm and program development as well as for custom and OEM applications. A mother/daughterboard configuration offers the

user a wide range of memory and I/O options. The system is specifically designed for multiprocessor applications. Motherboard memory options include dual access memory (allowing access to either the AT host or the TMS320C30) and dual port memory (allowing simultaneous accesses by both the host and DSP with no wait states). The motherboard can contain 32K- to 512K-bytes of dual access memory and up to 8K-bytes of dual port memory. The daughterboard is offered with up to 8M-words of memory.

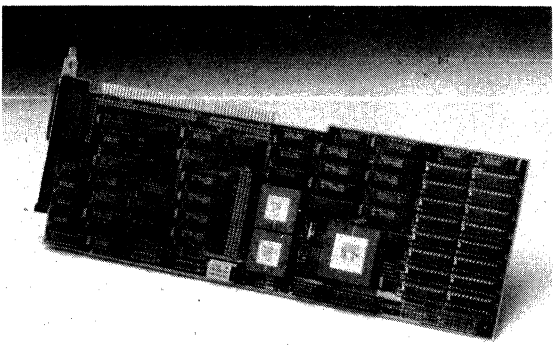

Figure 9-2. TMS320C30 Banshee System from ASPI

The Banshee is packaged with a powerful debugger and loader. Thus, as delivered, it is an excellent algorithm development tool. In addition, the Banshee's extremely flexible architecture makes it an excellent choice for custom and OEM applications.

The Banshee is interfaced to the host through a set of I/O status and control registers and through a movable memory window. The I/O and memory addresses required by the Banshee are switch-selectable. It can, therefore, co-exist in almost any host environment.

It can do high-speed data transfers with the host in four different ways: through direct register transfers, through dual port memory, through shared memory, and through DMA (direct memory access).

The Banshee can support three different types of memory: shared, dual port, and bulk. **Shared memory** is high-speed static RAM located on

the Banshee motherboard. It requires no wait states and is accessed through the memory window using a "cycle stealing" protocol. It is offered in 64K-, 128K-, 256K-, and 512K-bytes. **Dual Port Memory** is composed of high-speed register files also located on the motherboard. It can be accessed simultaneously by the host and TMS320C30. It is offered in 8K-bytes. **Bulk Memory** is dynamic memory available on an optional bulk memory daughter board. It requires one wait-state and an additional slot in the host. It is offered in 4M, 8M, 16M, and 32M-bytes.

There are three Banshee daughterboards: **WW** - Wire-wrap board, **AD16** - 16-Bit Dual-Channel A/D and D/A (see Figure 9-3), and **MP** - Multiprocessor Interface. The AD16 has two channels of 16-bit A/D, each with a maximum sampling rate of 200,000 samples per second. It also has two sample-and-holds and three independent sampling clocks. All Chimera I/O daughterboards will also operate on the Banshee.

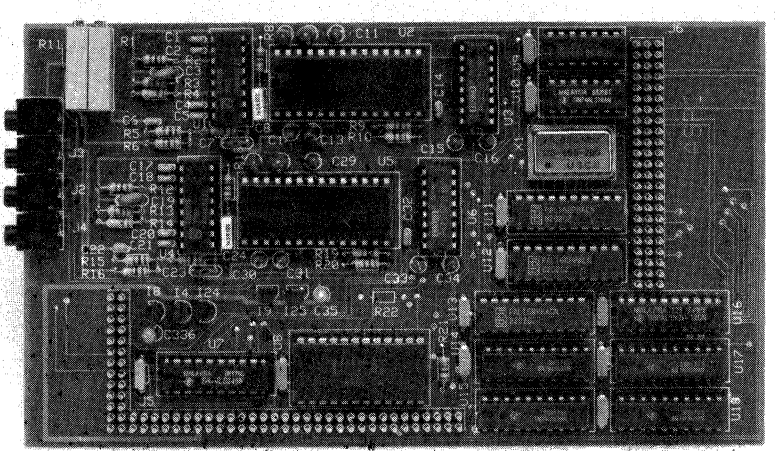

Figure 9-3. ASPI's AD16 Daughter Board for the Banshee System

9.3.6 Avocet Systems, Inc.

Nature of Product(s): Assembler, Simulator
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS320C10, TMS320C15, TMS32020, TMS320C25

- AVMAC Macro Assembler

  Avocet Systems offers the AVMAC321 and AVMAC322 macro assemblers, designed to aid in the development of TMS32010 and TMS32020 code, respectively. AVMAC's powerful macro facility offers a familiar architecture, augmented with modern structured control statements. The Advanced Object Format supports complex relocatable expressions and user-defined segments, with a full range of segment classes and attributes. Extensive command-line options give the user complete control over assembler operation. Informative error messages and cross-reference reports make debugging and documentation easy.

  AVMAC supports the TMS32010 and TMS32020 processors with instruction validation and detailed address space checking. A common underlying syntax makes it easy to switch from one AVMAC target version to another, while version-specific enhancements provide compatibility with TMS320 assembly language.

  AVMAC includes all the tools needed for assembly language development: AVLINK (linker), AVLIB (librarian), AVREF (cross-reference generator), and various utility programs such as HEXBIN that converts hexadecimal object files to binary. AVLINK combines relocatable object modules produced by the assembler, generating an executable file in Intel, Motorola, or Tektronix format. It can search relocatable libraries constructed with AVLIB, and gives the user complete control over segment combination and placement. AVREF generates cross-reference reports for debugging and documentation.

- AVSIM Simulator/Debugger

  Avocet Systems offers the AVSIM321 and AVSIM322 software simulator/debuggers for the IBM PC and compatibles. The AVSIM321 supports the TMS32010, TMS320C10, TMS320C15 and TMS320E15 DSPs. The AVSIM322 supports the TMS32020 and TMS320C25 DSPs. Both AVSIMs interpretively execute object code under control of a full-screen symbolic debugger. The interpretive approach eliminates the need for special hardware and makes them immune to target program crashes, thus resulting in powerful debugging tools at a low cost.

  Both AVSIMs are notable for their full-screen approach and ease of use. In operation, they turn the PC screen into a "visual CPU", with registers, flags, program and data memory all open to view. Editing keys manipulate these objects on-screen, while function keys control program flow for debugging. The user can edit memory and registers on-screen, even while simulation is running. A unique *undo* key uses the simulator's trace memory to back up one-at-a-time through recently-executed instructions, making it easy to determine where the program went wrong. Additional features, including an exceptionally flexible breakpoint facil-

ity, are accessed through screen menus and a command mode. The AVSIMs can replay a file to simulate a periodic waveform. Interrupt pins can also be driven from a file, or "random" interrupts can be generated from the keyboard.

The AVSIMs know the details of each chip in their family: ROM and RAM boundaries, mask options, instruction set, and timing. Illegal instructions, writes to ROM, and references to non-existant memory are all trapped. Control registers, I/O ports, timers, and associated interrupts are simulated and displayed.

9.3.7 Bedford Research

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC, PDP-11, VAX
Device(s) Supported: TMS32010, TMS32020

- I*S*P

  The I*S*P software package provides a fully integrated interactive signal processing system for developing customer-unique DSP application programs in a minimum amount of time. As an easy-to-use, high-level, signal processing programming language, I*S*P includes signal processing, graphics, and data management functions. Among the signal processing functions supported are transform functions, such as FFT and Walsh transforms, IIR and FIR filter design/implementation functions, linear-prediction functions, and all mathematical functions for standard array processing. I*S*P also supports real/complex floating-point and finite wordlength data formats.

  Graphics capabilities include parameter-driven 2D and 3D displays with automatic/manual scaling and labeling as well as zoom and histogram displays. Comprehensive data and file management functions allow easy access to data files and programs in the I*S*P files. New signal processing and graphics functions can be interactively designed by using the I*S*P command language.

  Bedford Research specializes in providing interactive signal-processing software for use in development and evaluation of advanced DSP products, such as the TMS320 family. Consulting and contract development support is also offered in the areas of theoretical and practical application of modern signal processing principles.

9.3.8 Burr-Brown Corp.

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): VMEbus, SUN-3/SUN-4 Workstations
Device(s) Supported: TMS32010, TMS32020, TMS320C25

- VMEdsp SPV100

  The VMEdsp SPV100 is a VMEbus DSP board that has as its core the TMS32010 digital signal processing chip. Two 4K x 16-bit "swinging" buffer memories speed operation by allowing one set of data to be manipulated in one buffer while data enters or exits the other. When data processing in one buffer is complete, the data from the second buffer is ready for processing. The maximum transfer rate for 16 bits into or out of the board's memory is 4M-word/second. Two separate program memories are provided. A 4K x 16-bit RAM allows user-developed programs to be downloaded onto the board, and a 4K-word x 16-bit PROM is used for specific application programs.

  Burr-Brown offers PROM-based routines for such functions as Fast Fourier Transforms (FFT), digital filtering (FIR), and auto- and cross-correlation. For complex data radix-4 FFTs, execution times as follows:

900.0 -µs	64-point FFT
7.2-ms	256-point FFT
17.6-ms	512-point FFT
36.4-ms	1024-point FFT

- VMEdsp SPV120

  The SPV120 is a general-purpose VMEbus DSP board incorporating the TMS32020. It contains memory which may be accessed by the TMS32020, the VMEbus, or auxiliary I/O ports. I/O ports are included to keep VMEbus traffic to a minimum and thus increase system output. The on-board debug monitor includes self-test firmware.

  The **DSPac** software development and DSP applications package is available for the SPV120 in VersaDOS-based systems. Cross-assemblers for the TMS32010 and TMS32020 processors can be used to develop, run, and debug software for the SPV120 board. The **DSP Applications Library** enables a variety of DSP algorithms. Comprehensive manuals are included with each product.

- VMEdsp SPV125

  The SPV125 (see Figure 9-4) operates on standard VME systems and is based on the TMS320C25. Extenders and adapters allow it to also work on the Sun-3 and Sun-4 workstations. The basic SPV125 board offers data transfer rates of 4M-bytes per second via two parallel ports operating under DMA control. Several memory options are available, including 16K-bytes of zero-wait-state PROM, data memory of 32K-bytes of SRAM, and local data memory of an additional 32K-bytes (expandable to 64K-bytes).

There are a variety of optional daughterboards available for memory expansion. Also available is an associated I/O motherboard and I/O expansion daughterboards. The SPV125 comes with software running under VersaDOS, including cross-assembler, monitor/debugger, and several application programs.

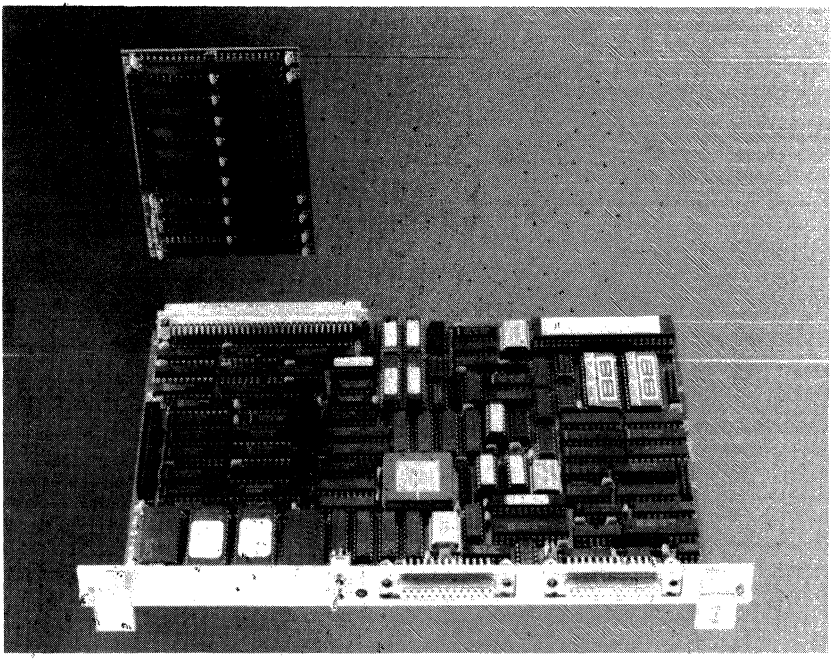

Figure 9-4. Burr-Brown's VMEdsp SPV125 Board

- VMEdsp MPV960

The VMEdsp MPV960 combines analog input with high-performance DSP functionality. It incorporates the TMS32010 digital signal processor onboard. Because the TMS32010 is significantly faster than traditional microprocessors, it allows the MPV960 to feature realtime digital signal processing of the analog input signals.

Some features of the VMEdsp MPV960 include:

- Simultaneous sampling on all four channels
- High-speed signal input (86 kHz max)
- Flexible triggering modes
- Dual-port memory for on-board data storage (8K-word x 16-bit)
- Optical isolation between analog signals and VMEbus
- 12-bit resolution.

Two 4K-word x 16-bit "swinging" buffer memories are included on the board to allow dual-port access. The board also contains a number of

PROM-based data acquisition and signal processing routines. An accessory daughter board (ACX960) provides downloadable program RAM for custom software development.

9.3.9 Comdisco

Nature of Product(s): Algorithm Development Software
Functional System(s): VAX (VMS), Apollo(Unix), Sun(Unix)
Device(s) Supported: TMS32010, TMS32020, TMS320C25

- Signal Processing Worksystem (SPW)

  The Signal Processing Worksystem package combines all the tools needed to interactively and graphically design, simulate, and test DSP systems. These systems can represent a variety of DSP applications such as communications, RADAR/SONAR, speech processing, image processing, adaptive signal processing, instrumentation, feedback control, etc.

  Under a common user interface, the SPW combines a signal flow Block Diagram Editor to capture DSP system designs and a proprietary Simultaneous Program Builder for signal flow simulation. Included are a Function Block Library and an instrument interface library. A closely-coupled interactive color Signal Display Editor provides the functions for signal creation, editing, display, and analysis.

  Dramatic productivity improvements are achieved by allowing the designer to concentrate on DSP algorithm design rather than the hand coding of a custom simulation program. The SPW automatically turns the signal flow block diagram (augmented from flow of control) into a simulation program with no limits on feedback complexity.

  SPW features include: powerful DSP system signal flow block diagram editor (BDE), rich DSP function block library (FBL), integrated instrument library (IIL), interactive solor signal display editor (SDE), proprietary signal flow simulation program builder (SPB), and industry standard platforms - VAX (VMS), Apollo (Unix), and SUN (Unix).

  The SPW employs the Block Diagram Editor, with a distributed database, to graphically capture a DSP system design as a signal flow diagram by using blocks from the Function Block Library and the Instrument Interface Library. The Signal Display Editor then synthesizes, edits, analyzes, and prepares input signals for the captured DSP design. The Simulation Program Builder then automatically compiles the block diagram with attached input signals into a simulation program and executes it. Finally, the resultant output signals are examined and analyzed by using the Signal Display Editor to verify the DSP system design.

9.3.10 Computalker Consultants

Nature of Product(s): Assembler, Simulator, and High Level Language Compiler
Functional System(s): IBM PC, CP/M, Apple II+/e/c, Amiga
Device(s) Supported: TMS32010, TMS32020, TMS320C25

- TASSM - TMS32010 Assembler
- TAS20 - TMS32020 Assembler
- TAS25 - TMS320C25 Assembler

These three assemblers for the TMS320 family of digital signal processors are fast, non-macro assemblers. They use standard Texas Instruments syntax and produce an object module file directly with no linking step. Full pathname support and many listing options are provided.

- S320 - TMS32010 Simulator

S320 is a complete interactive software simulation of the TMS32010, with a full-screen display of all registers during program execution or single-stepping. S320 includes a wide variety of breakpoint options, an execution cycle counter, a programmable simulated interrupt generator, and allows files to be assigned to I/O ports. S320 is not available for the Amiga. The CP/M-80 version requires a Z-80 processor.

- SPL - TMS320 Series Compiler

The SPL-function compiler is designed to be used with Computalker's TMS320 series of assemblers. It uses the Signal Processing Language (SPL), a concise, high-level programming language based on signal processing functions. The compiler allows rapid construction and modification of elaborate waveform processors or sound generators. Functions are compiled from a user-expandable macro-like library. The compiler handles all variable allocation and initialization, and builds the interrupt handler. An elapsed cycles report shows the percentage of interrupt time used. Available functions include a wide variety of waveform generators, filters, gain controls, arithmetic functions, and a means to execute blocks of code conditionally or under counter control. Assembly language may be intermixed with function statements. SPL is available for the IBM PC/XT/AT only.

Computalker has a variety of TMS320 series applications software, including Fourier transforms, telephone tone decoding, speech synthesizers of several varieties, speech analysis filter bank, and LPC speech analysis. Computalker provides programming services to adapt these programs to a specific application or to design custom signal processing routines.

9.3.11 Cybernetic Micro Systems

Nature of Product(s): Assembler, EPROM Programmer
Functional System(s): IBM PC
Device(s) Supported: TMS320C1x

- CYS320 Cross Assembler

  The CYS320 is an assembler package for development of TMS320C1x assembly language programs. It accepts TMS320C1x source code and outputs a list file and an Intel hexadecimal file. The assembler provides macros and nested conditional assembly directives as well as segment directives for symbol typing. Names and variables are not restricted in length, and the assembler is written in assembly language for fast execution (600 lines/minute). DOS commands can be issued within the cross assembler. The software package includes utility commands for saving hexadecimal files from internal memory, displaying internal memory, typing a file, and setting operating parameters.

- CYP-EPROM Programmer Board

  The CYS320 package provides support routines for the CYP-EPROM Programmer Board. The board is designed to program standard EPROMs for use as external program memory. It connects to the host computer via a RS-232 port, and uses the hexadecimal file generated by the assembler to program the EPROM.

9.3.12 Daisy Systems Corp.

Nature of Product(s): Algorithm Development Software
Functional System(s): LOGICIAN workstation, IBM PC/AT
Device(s) Supported: TMS320C1x, TMS320C2x

- LOGICIAN Workstation

  Daisy Systems Corporation supports the design of TMS320C1x-based applications on their LOGICIAN and Personal LOGICIAN workstations via the PMX (Physical Modeling Extension). The PMX unit functions as a systems engineering tool to accurately depict complex VLSI devices, such as the TMS320C1x and TMS320C2x, to the workstation for simulation. By using actual devices as models that are plugged into the PMX, designers can fully simulate microprocessor-based systems. The logical behavior is obtained directly from the processors and integrated into the LOGICIAN simulation.

9.3.13 Dalanco Spry

Nature of Product(s): Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS320C25, TMS320C25-50

- Model 10 Digital Signal Processor

  The Model 10 Digital Signal Processor is a coprocessor board that features the TMS32010 operating at 20 or 25 MHz, 4K words of dual-ported RAM, three 16-bit timers to provide sampling rates ranging from 0.001 Hz to 200 kHz, a two-way 16-bit register for communications between the TMS32010 and the IBM CPU, and mutual interrupt capabilities between the two processors. The board is available with or without on-board 12-bit 40-kHz A/D and D/A converters. An external I/O bus connector permits the addition of piggyback boards of varying functions and capabilities. A user can design and build his own modules to suit his application, e.g., a counter-driven MHz range A/D converter or a modem interface.

  Software includes a debugger, inline assembler, disassembler, signal and spectrum display software for the IBM Color Card, and applications examples, some of which are taken from TI Application Reports.

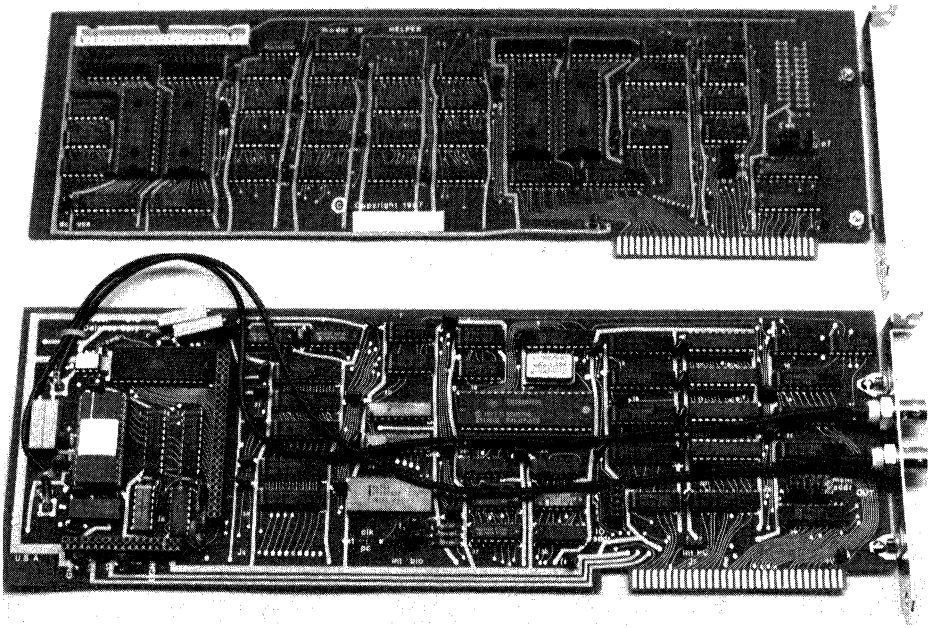

Figure 9-5. Dalanco Spry's Model 10 Digital Signal Processor

- Model 10 Helper

  The Model 10 Helper is an IBM PC (and compatibles) add-in memory board which extends the capabilities of the Model 10 DSP board. The Helper permits the Model 10 to act as an efficient array processor, and when used in conjunction with the Model 10's A/D-D/A converters, permits the continuous recording and playback of signals to hard disk at high sampling rates. A waveform display package accompanies the Helper.

- Model 25 Digital Signal Processor

  The Model 25 DSP is an IBM-PC/XT/AT (and compatibles) board featuring the TMS320C25, 4K-words of zero-wait-state clock circuitry, two-way 16-bit registers, and mutual interrupt capabilities. It possesses DMA capability to and from PC RAM (useful for data acquisition applications); the TMS320C25 serial port capabilities may also be used. A digital I/0 bus connector lets the user design his own external interface. The Model 25 DSP includes a debugger, in-line assembler/disassembler, signal/spectrum display,and applications examples. This product supports the TMS320C25-50.

9.3.14 Digital Audio Corp.

Nature of Product(s): Application Hardware
Functional System(s): N/A
Device(s) Supported: TMS32010

- RCW320 Laboratory Digital Signal Processor

  The RCW320 is a powerful multifunction voice-enchancement and signal-processing instrument, based on the TMS32010. It combines the high-speed 20-MHz microprocessor along with high-resolution analog conversion to produce outstanding signal-processing performance. With the RCW320, many DSP functions are directly implementable with TMS320 code.

  The RCW320 is completely controlled by the operator from the front panel. The desired function is selected and appropriate values set on the numeric LED displays. The displays precisely specify the instrument's operation, allowing the operator to accurately control processing. Some of the functions that can be performed are:

  1) Digital filters (highpass, lowpass, bandpass, and bandstop).
  2) Adaptive filters (33rd-order), which reduce time-correlated noises such as tones, soft music, microphone muffling, and room resonances on voice signals.
  3) Automatic gain control, thus allowing a signal free of distortion or annoying artifacts.
  4) Comb filters to cancel 50-Hz and 60-Hz powerline-induced hum.
  5) Peak and zero clippers to limit and reduce low-level background noise during signal silences.
  6) Expansion for up to eight additional modes of operation or custom signal processing functions by replacing plug-in PROMs.

  Multiple signal processing functions may be performed by a sequence of RCW320s. Rear-panel digital connectors allow direct cascading without degradations due to analog cabling.

9.3.15 Digital Signal Processing Software, Inc. (DSPS)

Nature of Product(s): Assembler, Algorithm Development Software, Application Software
Functional System(s): PDP-11, VAX (VMS), IBM PC
Device(s) Supported: TMS320C10

- DSPS-3 Tutorial Package

  The DSPS-3 software package provides a macro assembler and a program loader for the TMS320C10 Evaluation Module (EVM) and Emulator (XDS). Also included in the package is a 500-page, tutorially-oriented softcover book, *Digital Signal Processing Software* by L. Robert Morris, which provides numerous TMS320C10 program examples. To illustrate these examples, the package also contains a PDP-11 or IBM PC format floppy-disk with sources for all of the book's software (about 50 FORTRAN, PDP-11, and TMS320C10 programs). Algorithms for Linear Predictive Coding (LPC) of speech guide TMS320C10 users in applications such as LPC vocoders, parameter extraction for speech recognition, speaker verification, format and pitch tracking, and vocal tract estimation.

- DSPS-2 FFT Package

  The DSPS-2 software package is a combination of the DSPS-3 software package plus TMS320C10 FFT programs that use radix-4 for high precision. To supplement the macro assembler and TMS32010 algorithm examples provided in DSPS-3, DSPS-2 expands the range of applications to include spectral and cepstral analysis, DFT-based vocoders, speech scramblers, FFT modems, and frequency compression. For 64-, 128-, and 256-point complex DFT transforms, benchmarks are 0.54-, 2.4-, and 6.2-ms, respectively. It is also possible to effect time-efficient 64-, 128-, 256-, and 512-point real transforms.

- RSL Spectrogram Generator

  The RSL (Realtime Signal Lab) software package generates realtime, high-definition, multi-intensity, simultaneous wideband and narrowband speech spectrograms (two-dimensional displays of the changing intensity of the speech amplitude spectrum as a function of time). RSL samples up to two seconds of speech at an 8-kHz rate. It then processes and displays dual spectrograms, each consisting of 256 spectral cross-sections of 128 16-intensity spectral samples, in only 5 seconds. Times quoted include pre-emphasis to compensate for the spectral falloff of speech at higher frequencies and windowing to provide spectral smoothing and determination of effective filter analysis bandwidth. When the full two seconds of sampled speech is specified for analysis and display, RSL is indeed realtime.

The combination of the RSL software with the TMS32010-based TI-Speech PC plug-in board provides the speed and functionality of hardware devices that cost at least ten times more than the RSL package. The graphics board supported is the Tecmar Graphics Master for IBM PCs or compatibles. (RSL also runs on the older TI-Speech Command System board). The screen may be photographed or sent to an Epson FX-80/80+/85+/180/180+/185 or TI 850 series printer.

9.3.16 Digital Sound Corp.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): Unibus, Q-bus, VMEbus, and SCSI bus
Device(s) Supported: TMS32010

- DSC-200

  The DSC-200 is a unique computer peripheral subsystem specifically designed to provide accurate, convenient, and versatile input and output of audio data. The DSC-200 integrates 16-bit analog-to-digital (A/D) and digital-to-analog (D/A) converters, lowpass filters, audio amplifiers, a data-chaining DMA computer interface, and remote audio consoles in a low-noise and low-distortion system architecture. Unibus, Q-Bus, VME bus and SCSI bus interfaces available and in development.

  To illustrate the DSC-200's role in speech/voice development, assume that a new coding (compression) algorithm for a digital signal processing (DSP) chip, such as the TMS32010, is being developed. After conceptualization, a mathematical model of the algorithm is programmed for execution on a host computer simulating the operation of the target DSP, such as a TMS32010 simulator. A speech data base of sample vocabularies is created using the DSC-200's A/D converter(s). This test data is processed by the simulation program, and aurally evaluated (listened to) via the DSC-200's D/A converters. The test data, before and after processing, may also be transformed and visually analyzed using such software tools as ILS, SPIRE, and ISP. This process is repeated until satisfactory performance is achieved.

  Upon completion of the simulation, the DSP program is loaded into the ROM (or RAM) of the prototype speech module, and accessory circuits are attached (including the module's own A/D component). The original test data is output (D/A'd), again via the DSC-200, as input to the free-standing coder. The digital output of the encoder can be input to a matching decoder whose analog output may be fed back to the host CPU via the DSC-200 for further analysis (e.g., spectral) when testing has been completed.

9.3.17 Discrete TimeSystems, Inc.

Nature of Product(s): Application Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS320C25

1) CVP-2000 Hardware Product Family Overview

The CVP-2000 product line represents a breakthrough in image processing. Using a standard video camera or alternate video source, the CVP-2800 and CVP-2400 boards capture images and then compress them at ratios as high as 30:1. The images can then be stored on floppy or hard disks, CD-ROM, WORM or other optical media. They may also be transmitted to another PC. All of the board products can be used to retrieve images, decompressing and then displaying them on a monitor or reproducing them in hard copy format.

The design of the CVP series is based on compression technology which produces quality images that require less data to describe them. The end result is a more economical means for storing and transmitting images. Significant savings in both time and money can be realized.

- CVP-2800 Board

  The CVP-2800 Color Video Processor image compression board is versatile in nature and combines in one product features that include: image capture, image processing, compression, image archiving, telecommunications, graphics, text,image expansion, color look-up table, a mouse interface, filtering, zoom, and scaling. For a typical image, compressed at 15:1 ratio, image compression takes about one second. The expansion rate is five frames per second.

- CVP-2400 Board

  The CVP-2400, like the CVP-2800, is a single board that fits into the PC. The CVP-2400 helps users reduce the size of image data files, compressing the data for more economical storage and transmission. It features a single buffer that is designed as a complement to graphics products already in use, and for use in applications where dual buffers are not needed. Compression and expansion rates are the same as for the CVP-2800

- CVP2300 and CVP-2200 Boards

  The CVP-2300 and CVP-2200 are expansion-only boards. The CVP-2300 offers dual buffers, the CVP-2200 a single buffer. They are used in conjunction with the CVP-2800 and CVP-2400 boards in multiple site applications. The combination consists of a limited number of CVP-2800 or CVP-2400s used to capture, compress, and store images and multiple CVP-2300 or CVP-2200s used to "playback" compressed images.

  An example of an application for the CVP-2300 or CVP-2200 would be image storage of public access terminals: The stand-alone computer based systems from which tourists access local travel information.

2) CVP-2000 Software Overview

Compression produces images that require less data to describe them than did the originals. This increases the volume of images that can be stored in a stated memory space and decreases the time required to transmit them over ordinary telephone lines. For example, at a compression rate of 15:1, storage and transmission requirements are reduced about 93 percent, while image quality and integrity are maintained.

- CVP-2810 Software

  The CVP-2810, software package for the CVP-2800 board, features a complete library of calls including scaling, filtering, still image conferencing, mouse controller interface, color look-up table, single monitor plus paint capabilities of rubberband, box, rotate, flip, and drawing.

- CVP-2410 Software

  The CVP-2410 supports the CVP-2400 single buffer compression board and takes advantage of features available with CVP-2810.

- CVP-2310 and CVP-2210

  The CVP-2310 and CVP-2210 libraries complement the boards, CVP-2300 and CVP-2200, to retrieve, decompress, and display images that were originallu compressed and manipulated by the CVP-2800 and CVP-2400. The CVP-2310 and CVP-2210 support menu creation, image retrieval, and the activation of a printer or similar output device.

9.3.18 DSP Development Corp.

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC, SUN Workstations, HP 9000 Series 300, Masscomp Series 5000
Device(s) Supported: TMS320 Family

- DADiSP Worksheet

  DADiSP features a wide variety of functions for the transformation of data, including: FFT's, waveform generation, statistical analysis, signal arithmetic and calculus, peak analysis, signal cursoring and editing, plus "signal spreadsheet" operations. Signals of any size can be cursored, zoomed, expanded, and compressed with unprecedented ease. Individual signals of any size can be readily loaded from disk into window. Full background information on any signal can be displayed with the touch of a single key. Signals can be displayed in both graphic and tabular form.

  DADiSP supports user-defined functions through its macro definition facility, and can generate an endless variety of waveforms with its "G" functions. DADiSP Worksheet and Datasets are convieniently stored in individual DADiSP Labbooks to facilitate the separation of multiuser tasks.

9.3.19 DSP Group Inc.

Nature of Product(s): Application Hardware
Functional System(s): N/A
Device(s) Supported: TMS32010, TMS320C14, TMS320C17, TMS320C25, TMS320C30

The DSP Group offers a family of products in speech enhancement and speech coding. These products can be used independently or in combinations as building blocks. The products are packaged as stand-alone modular units, as printed circuit boards for system integration, or as microchips for board level integration. This allows the products to be designed into equipment by original equipment manufacturers.

- NOISE-X

  NOISE-X is a realtime noise reduction technique that detects and selectively screens dynamic noise in the presence of speech. It provides highly adaptive digital filtering over the entire audio spectrum based on proprietary speech detection and selective noise screening algorithms. The single channel NOISE-X, which requires no reference channel, is effective with many different types and levels of noise. It can be effective in many applications especially to improve speech perception.

- SMART-VOX

  SMART-VOX is a voice operated switch activated only when speech is detected. It uses an adaptive algorithm, based on the charactistics of speech, to accurately discriminate between speech and noise throughout the entire audio spectrum. It is activated even when the human ear may have difficulty comprehending because the speech is immersed in severe noise. Applications include hands-free transmitting, receiving stations, and voice storage systems. SMART-VOX is often combined with NOISE-X

- DENSI-SPEECH (compression)

  DENSI-SPEECH provides high quality realtime digital speech compression using sub-band coding. It provides near toll quality from 9.6K-bits/sec to 16K-bits/sec with a high immunity to background noise. High performance is also achieved even with multiple simultaneous voices. A major advantage is the fully adaptive bit allocation which substantially reduces quantification noise. DENSI-SPEECH provides significantly increased computer voice storage efficiency for voice mail and shorter transmission time for voice communications yielding increased line capacity.

- FLEXI-SPEECH

  FLEXI-SPEECH allows stored speech to be played back up to two and one half times its original speech, or slowed down to half the original speed, without any perceived distortion. Essentially this is a high quality speech compression and expansion technique. It can be used in both analog and digital audio communication recording systems. Applications include speech analysis and variable speed playback. FLEXI-SPEECH can be combined with DENSI-SPEECH.

9.3.20 DSP Technology Corp.

Nature of Product(s): Application Hardware
Functional System(s): N/A
Device(s) Supported: TMS32010

- DSP8501

  The DSP8501 is a digital DTMF detector based on the TMS32010. The single chip is capable of detecting four channels simultaneously, and directly interfaces with μ-law/A-law PCM data, thus avoiding the need for a codec used in conventional analog tone detection. The tone-detection algorithm uses an optimal signal-detection filter for each of the eight frequencies used in DTMF signaling. The tone-decode decision logic uses data-adaptive thresholds for reliable detection of the DTMF digit. The chip performs reliably in the presence of noise and dropouts, and requires no adjustments of external components. The DSP8051 is ideal for applications such as digital switching systems, PBX, central offices, key systems, and remote data entry.

- DSP8502

  The DSP8502 is a four-channel digital MF Decoder based on the TMS32010, which meets the Bell MFR1 and CCITT #5 specifications. Its features are similar to those of the DSP8501. It also provides coded output of the MF digit and error code for improper tone combination. Applications for this chip include central office, toll office, specialized common carrier switch, and equal access system.

- CONFER

  CONFER, a multiparty digital audio conferencing bridge, provides a full-duplex voice communication facility for interconnection of up to six parties. The bridge is used in conjunction with any of the electronic key systems. It is located on the trunk side of the key system control unit and is transparent to the key system's normal use. CONFER can be attached to any electronic key system that requires an advanced conferencing system.

  The conferencing bridge uses a TMS32010 to implement sophisticated digital signal processing algorithms, enabling the users to have a natural interactive conversation. It allows any speaker to interrupt at any time during the conversation. The voice levels are automatically adjusted for normal volume. This compensates for weak sound levels due to trunk loss encountered in long-distance connections, so that all the parties can hear each other clearly regardless of location.

9.3.21 DSP Technology Inc.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): N/A
Device(s) Supported: TMS320C25

- TRAQ P System

  The TRAQ P is a complete modular solution for multi-signal realtime processing applications. Based on the TMS320C25 digital processing chip, it is intended for factory, laboratory, and onboard vehicular requirements such as automotive combustion analysis, SONAR research, and stress monitoring. The system is uniquely designed for expandability, high-speed throughput, multichannel processing, and efficient software development.

  TRAQ P processes up to 256 analog and digital signal channels through one or more processing CPU boards, each containing a high-speed TMS320C25. Three separate high speed data busses optimize throughput to the signal channels, realtime processors, and external computer. Each processor board contains one TMS320C25 with 32K-bytes of zero wait state data memory and 16K-bytes of program memory. A resident 8K-byte EPROM contains a monitor for program development supplies various utilities for program downloading, code development (disassembler, single step, breakpoints, etc.) and system control. Programs can be downloaded directly from TI's family of support tools. All data busses are interfaced through 4K-byte FIFOs with special interrupt circuits to optimize throughput. Each board also contains D/As and TTL I/O lines.

  The system accomodates up to eight realtime processing modules which can be individually programmed to access and process any combination of data channels. A variety of A/D modules are available with sampling rates up to 2 megasamples/channel and 14 bits of resolution. Modules can be added as requirements change. A unique feature of the system allows digital information to be acquired simultaneously with the analog signals. TRAQ P also supports 16 megawords of modular memory for realtime data storage. This feature allows both post processing of data and a special trace capability allowing the user to single step through capured realtime data for algorithm and error analysis.

  A wide variety of programmable plug-in signal conditioning amplifiers, filters, and trigger generators can be used within the TRAQ P system to tailor its configuration for a particular application. The system housing is available as a 19" rack mount with 23 board slots and 500 watts of power. A smaller 12 slot housing, for portable requirements, is available with either AC input power or 12 VDC for automotive invehicle tests.

9.3.22 Electro Rent Corporation

Nature of Product(s): Leasing of TI XDS/22 Emulators
Functional System(s): N/A
Device(s) Supported: TMS320C1x and TMS320C2x

Electro Rent Corporation leases TI's TMS320C1x and TMS320C2x XDS/22 emulators. A variety of rent/lease plans are available. Equipment can be delivered and immediately put into use without bank financing or capital outlay. Support, repair, or replacement is provided at no charge. 11 sales and service locations nationwide ensure rapid pre- and post-sale response to customer questions and needs.

Electro Rent is the nation's largest rent/lease supplier of microprocessor development systems, logic analyzers, and PROM programmers. Additionally, Electro Rent's large inventory provides a wide variety of general purpose test equipment, data acquisition, RF and microwave, telecommunications, and data products.

9.3.23 EMU-SYS Inc.

Nature of Product(s): Application Hardware, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS320C1x, TMS320C2x

> **Note:**
>
> EMU-SYS Inc. is the exclusive representative for dSpace GmbH in North America. See separate listing in this section for descriptions of dSpace GmbHs hardware and software products for the TMS320 family of signal processors.

9.3.24 FACS Inc.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): N/A
Device(s) Supported: TMS320C25

- DSP3200 Evaluation Module

  The DSP3200 (see Figure 9-6) is designed for evaluation module control applications, including engine/ transmission control, DSP development in active suspension, high-speed data acquisition, digital filtering, spectral analysis, speech recognition/synthesis, I/O control, and noise cancellation. Small size and low power consumption make it ideal for battery powered operations in automotive, marine, military, or remote field applications. Using the TMS320C25 DSP, the DSP3200 allows high-speed control algorithms to be computed with higher throughput and more accuracy than traditional implementations of observer models, self-tuning regulators and state estimators.

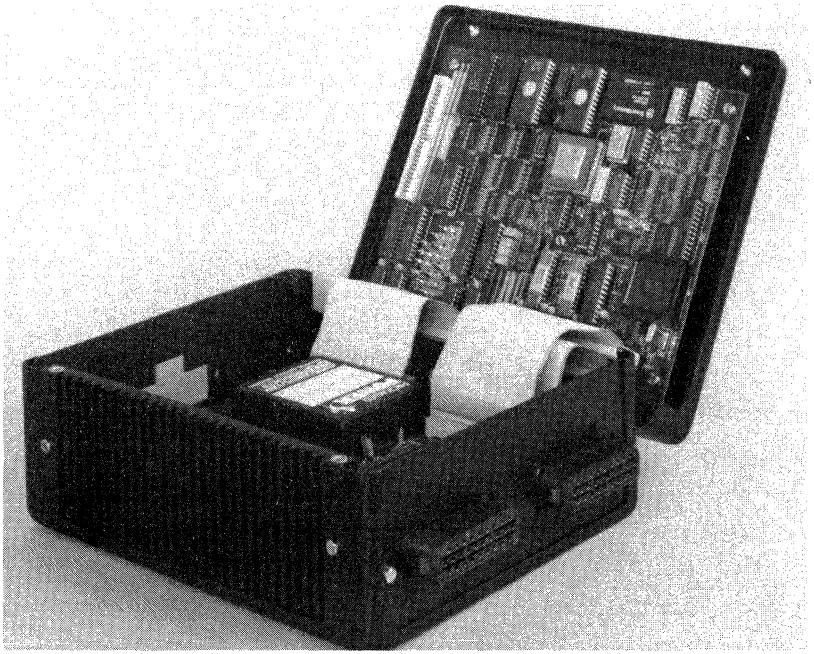

Figure 9-6. FACS Inc. DSP3200 Evaluation Module for Control Application

9.3.25 FORTH, Inc.

Nature of Product(s): Algorithm Development Software, Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32020,TMS320C25

- FB-320 Interactive DSP Software/Hardware Prototyping System

  Forth, Inc. offers a high-level software prototyping system for DSP applications. The system runs interactively and at full speed on the TMS32020 and TMS320C25. This shortens the time required to develop and test programs by as much as a factor of ten compared to traditional cross-development systems.

  The FB-320 includes a full multitasking polyFORTH operating system and a Spectrum Signal Processing IBM-PC/XT/AT plug-in board with either a TMS32020 or TMS320C25 chip.

  Key features of the prototyping system are:

  - Immediate compilation of source to executable code without separate steps for linking and downloading
  - A complete TMS32020/TMS320C25 macro assembler
  - Special high-speed implementation of the interactive high-level FORTH programming language
  - DSP extensions for waveform generation, FFTs, and digital filter design
  - Resident debugger, editor, and other programming aids
  - Use of an inexpensive host computer, such as the IBM-PC/XT/AT, for terminal and disk services to the target hardware.
  - Detailed examples of applications.
  - Full source code for the entire system.
  - Target compiler allows user to generate programs to run on custom hardware, including ROMable embedded operations.
  - Extensive math library includes 16-bit and 32-bit integer arithmetic, mixed 32/64-bit operations, 16/32-bit fast fixed-point fraction arithmetic, trigonometric, transcendental, and square-root operations, plus Fast Fourier Transform (FFT).
  - One year telephone Hot-Line support and updates.

  Key features of the hardware supplied are:

  - Full-length IBM-PC/XT/AT plug-in board.
  - Comes with 24K-words (16-bit) zero wait-state SRAM.
  - Supports up to 128K-words (16-bit) of on-board memory, link programmable for RAM or EPROM.
  - Analog input of 16-bit data at up to 60 kHz, 12-bit data at up to 100 kHz.
  - Sample-and-hold on input
  - Analog output of 16-bit data, settling time 3 μs.
  - Hardware expansion connector facilitates addition of extra hardware by the user.
  - Two separate 10-pin serial connectors for I/O and linking additional boards.

9.3.26 Gas Light Software

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- Z-EDIT Digital Filtering Program

  Gas Light Software offers a digital filter editing program, Z-EDIT, that may be used alone to manually design and edit digital filters or as a manual postediting system used in conjunction with any automatic filter design system. Z-EDIT allows either pole/zero or coefficient input and output in ASCII files for simple intrasystem communications. The 8087 coprocessor is also supported to allow faster root-factoring or FFT filter analysis on larger filters. User-friendly interface and HELP message options make this system easy to use.

  Z-EDIT allows an engineer to manually edit poles or zeros in either the S plane (analog domain) or Z plane (digital domain), and quickly observe spectral or temporal filter response changes in numeric or plotted form. Bilinear mapping in Z-EDIT allows conversion of an S-plane filter to a Z-plane filter. Root components in real or imaginary filters may independently be edited in either Cartesian or two-polar coordinate formats. Editing features include adding, deleting, copying, and radius inversion. Filters with up to 101 coefficients (in either numerator, denominator, or both) are allowed. A specially designed robust root-finder permits the factoring of coefficients where no poles or zeroes are given. Z-EDIT also allows filter inversion and/or stabilization. Final design coefficients may be converted to integer format (4 to 16 bits) and special stability verified to facilitate integer-arithmetic hardware implementations on the TMS32010.

9.3.27 Hewlett-Packard

Nature of Product(s): Assembler, Emulator, Disassembler
Functional System(s): HP 64000-UX, IBM PC
Device(s) Supported: TMS32020, TMS320C25

- HP 64786A/AL Emulation/Analyzer Subsystems

  Hewlett-Packard provides microprocessor support tools for development of TMS32020-based systems with emulation, analysis, and software tools for the HP 64000-UX systems, and IBM PCs. These emulators/analyzers are self-contained vehicles which can be integrated into the HP 64000-PC Personal Integration Environment by hosting the emulator on an IBM PC or compatible such as the HP Vectra PC. For large team-oriented designs, the emulators can be integrated into the even more powerful HP 64000-UX Advanced Integration Environment hosted on HP 9000 Series 300 computers. Two RS232-C serial ports are provided for connection to PCs, workstations, or basic terminals.

  The HP 64786A/AL Emulation Subsystems provide realtime, transparent emulation at up to 20 MHz with no wait-states. Nonintrusive, realtime emulation traces of all TMS32020 memory activity and instruction set desassembly further simplify development work. Other features include 64K-words of addressable emulation memory, 32 software breakpoints, built-in 48-channel emulation analyzer, software code coverage analysis, symbolic debug, and an optional integrated, 16-channel external state/timing analyzer. It can synchronize, cross-trigger, or be controlled by other emulators.

  The optional 16-channel external state/timing analyzer **(Model 64786AL)** can be configured for asynchronous 100 MHz timing analysis, 25 MHz state analysis, or for slave analysis coupled with the emulation analyzer. An optional user interface is available which provides symbolic debug and a friendly windowed user environment.

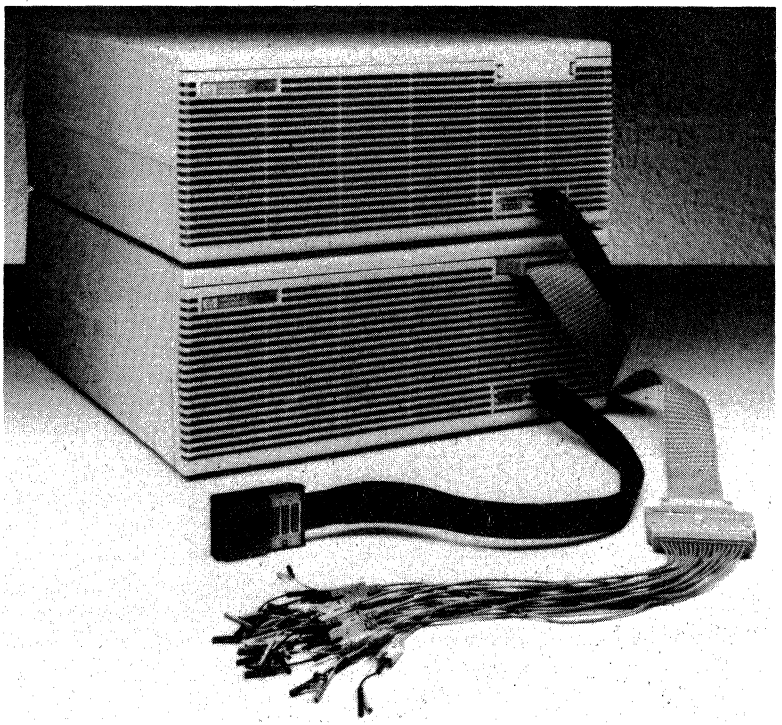

Figure 9-7. HP 64700 Series TMS32020/C25 Emulator

- HP 64787A/AL Emulation Subsystems

  The HP 64787A/AL Emulation Subsystems provide emulation for the TMS320C25 at speeds up to 40 MHz. They have the same capabilities as the HP 64786A/AL.

- HP 64867 Assembler/Linker

  The HP 64867 Assembler/Linker provides assembly language software development support for both the TMS32020 and TMS320C25. The assembler uses TMS32020/C25 instruction mnemonics, generates code for all instructions, and generates the necessary information for symbolic debug in emulation. Troubleshooting of code is accomplished using source program global symbols, thus eliminating the task of address lookup.

- HP TMS32020/C25 Preprocessor Interface and Disassembler

  The HP TMS32020/C25 Preprocessor Interface and Disassembler is designed for use with the HP 163X D/G, 1650A, 16510A Logic Analyzer or the 64620S Logic/State Analyzers (with 60 or more channels). The preprocessor interface provides a convenient connection between the analyzer and the user's target via a 68-pin PGA socket/probe. The dis-

assembler software supports the TMS32020 and TMS320C25 instruction sets and automates configuration of the analyzer.

9.3.28 Hyperception

Nature of Product(s): Algorithm Development Software, DSP Workstation,
Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS320 family

- Hypersignal-Plus Software

  Hypersignal-Plus is a general-purpose DSP software package which provides a complete signal processing environment on the IBM PC/XT/AT and compatibles. Menu-driven control organized in Time-Domain, and Utilities categories provide simplified ease of use. Time domain selections include waveform editing, autocorrelation, offer difference equations (with recursion), Fast FFT's, FIR and IIR Filter Construction, plus convolution and recursive filtering implementation. Code generation creates assembly language TMS320xx and TMS320C30 filter code with quantization and simulated impulse response. Frequency Domain functions include power spectra generation and inverse FFT. Waveform displays feature time, magnitude, and phase analysis, 2-D and 3-D spectrographic displays, pole-zero analysis (in S and Z planes), plus graphical IIR and FIR filter editors. Displays have dual-waveform capability, with pan, zoom, random access, and grid/color/background controls. Utility selections include a file acquisition function that can acquire TI Software Development System (SWDS), XDS emulator, and Evaluation Module (EVM) emulation format data files. An added feature is the direct PC-memory access capability that acquires SWDS dual-port data memory.

- Hypersignal-Workstation DSP Software

  Hypersignal-Workstation DSP software serves as an algorithm and code development environment for the TMS320 family. It downloads code, simulates/emulates/tests TMS320 family code, and acquires results for direct analysis. Hypersignal-Workstation software has all the features of Hypersignal-Plus, but provides realtime signal acquisition and generation. Accelerated FFT processing of sampled signals, including magnitude/phase calculations, can be configured to use TI SWDS PC-based hardware. A digital oscilloscope function allows file or signal acquisition board input, selectable trigger, variable timebase, single-trace, dual-trace, etc. A spectrum analyzer function allows dynamic monitoring of frequency components by using either disk files or an analog signal acquisition board. Options include various other A/D and accelerator boards.

- DSP Workstation

  The DSP Workstation is a 20 MHz 80386-based machine with a 20 MHz 80387 coprocessor and a TMS320C25 DSP processing/sampling board. Integration of popular TMS320 DSP hardware is accomplished through menu selections in Hypersignal-Workstation DSP software. This system allows Time-Domain and Frequency-Domain Analysis in a realtime environment. Powerful displays such as 2-D and 3-D spectrographic

analysis allow detailed study of frequency data, and include advanced features such as waveform storage and retrieval, topology and color control. Record and playback functions to/from the hard disk, digital oscilloscope, spectrum analyzer, accelerated FFT processing with control over parameters, and other DSP functions make this an ideal working environment for DSP development.

Included with the Workstation is a 640 x 480 16-color display, microphone, speakers, mouse, 40M-byte hard disk drive, internal tape backup, accelerator board, and Hypersignal-Workstation software. Other options are available.

Figure 9-8. DSP Workstation from Hyperception

9.3.29 Intelligent Instrumentation Products, Burr-Brown Corporation

Nature of Product(s): Algorithm Development Software, Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS320C25

- PCI-20202C-1 Smart Carrier
- PCI-20201M-1 Memory Module

The PCI-20202C-1 is a high performance "*smart*" Carrier designed for the IBM PC bus. This *smart* Carrier board is based upon the TMS320C25 processor. By using this high performance signal processor, it is possible to process data 20 to 200 times faster than by using the PC alone. Furthermore, true background processing is provided. When used as an "attached processor", both the control of the input/output process (ie., A/D and D/A conversion) and the desired mathematical analysis (ie., window, FFT, filter, etc.) can be performed independently on the host PC. The PC contributes just the human interface and supervisory functions. When used as a "co-processor", the *smart* Carrier can transfer a data array from the host computer's memory, process the data, and return the result to the PC's memory using Direct Memory Access (DMA). DSP or other multiply/accumulative intensive algorithms can greatly benefit from the Carrier's high speed capabilities.

As an example, here are representative execution speeds using the PCI-20202C-1 Smart Carrier:

FFT	64	point	0.4-msec
	256	point	2.2-msec
	1024	point	27.0-msec
FIR Filter	(80	taps)	13.0-µsec
1024 x 1024 Scalar Product			2.3-msec

The carrier plugs directly into an expansion slot of any IBM compatible PC. Each carrier can accept up to three plug-in modules. Two module locations are for I/O functions, while the third is for high-speed RAM expansion.

The RAM module, PCI-20201M-1, adds 64K-words of 55-ns memory. A family of 12 different I/O modules is now available to support a wide variety of "real-world" signals. Also available are 13 analog I/O modules that provide 12-bit conversions at rates up to 180 kHz. If desired more than one RAM module can be installed in the same computer.

The carrier itself carries 16K-words of program memory, along with 16K-words of data memory. While this is adequate for most applications, the optional expansion module increases the data memory to the full 64K-words allowed by the processor. At the same time, program memory is extended to 32K-words. All memory is accessed with zero wait-states. An up/down load feature allows the PC to directly read or write to this memory. This allows the system to operate without on-board ROM.

- Software Support

  The PCI-20202C-1 *Smart* Carrier is supported by a complete set of software products. The software packages were designed specifically for this carrier to aid the user in the complete software development cycle. The wide range of tools provides significant capabilities for all application and user levels.

  DSPview (PCI-20205S-1) is an FFT analyzer package that provides an introduction to typical applications and capabilities. Because it is menu-driven, DSPview brings a working demonstration of the system's key components to all users. Useful "instruments" include:

  - Display of Time Signal and its Spectrum.
  - Display of Power Spectrum in a One-Shot Waterfall format.
  - Display of Power Spectrum in a Running Waterfall format.

  An extensive DSP Library, **DSP Library Plus (PCI-20203S family)**, implements 75 functions, all callable from one of several popular high-level languages, including BASIC, C, TURBO PASCAL, and FORTRAN. This library allows the user to perform the following tasks very quickly:

  - Data Acquisition and Control
  - Transient Capture
  - Digital Filtering
  - Spectral Analysis
  - Waveform Generation
  - Data Compression and Interpolation

  Each function is performed with proven algorithms, without having to write any DSP-specific code. No detailed knowledge of the hardware is required, and no TMS320 code need be generated.

  The major Library functions include:

  - FFT Routines for 64 to 8192 data points
  - Windowing Functions
  - A/D and D/A Conversion including Triggering
  - FIR and IIR Filter and Execution
  - Auto- and Crosscorrelation
  - General Vector Operations
  - Data Compression and Interpolation

  The **DSP Software Development Package (PCI-20204S-1)** is available for those who wish to create their own algorithms. This package operates with the industry standard Microsoft Macro Assembler and includes:

  - TMS320C25 Crossassembler
  - Linker, Program Loader, and Disassembler
  - Monitor/Debugger with single-step and breakpoint functions

Figure 9-9. Intelligent Instrumentation Products' Smart Carrier Board and Software

Companion DSP Carrier Drivers (PCI-20206S family) assist the programmer in communicating with the *Smart* carrier and the modules from a high-level language.

The PCI-20206S series of DSP Carrier Drivers give the user a simple and consistent method of communicating with the *Smart* Carrier from a high-level language program. These drivers are useful for those who have created their own TMS320C25 programs using the PCI-20204S Software Development Pak. They provide an easy method of:

- Loading programs onto the carrier
- Starting and stopping program execution
- Passing parameters to and from the carrier's TMS program
- Transferring data between the PC and the carrier

The carriers act to minimize the need for a detailed knowledge of the *Smart* Carrier. Several of the most popular high-level languages are supported, including: BASIC, C, TURBO PASCAL, and FORTRAN. In addition to being available separately, the PCI-20206S DSP Carrier Drivers are also included in the DSP Library Plus.

9.3.30 Kay Elemetrics Corp.

Nature of Product(s): Application Hardware
Functional System(s): N/A
Device(s) Supported: TMS32020

- Kay DSP Sona-Graph Model 5500

  The Kay DSP Sona-Graph model 5500 is a TMS32020-based signal analysis workstation designed for the acquisition, processing, and display of time varying signals in the DC to 32-KHz bandwidth. The 5500 acquires, analyzes, and displays signals in realtime. It combines the features of a realtime spectrograph, a high-speed dual-channel FFT, and a computer-based data acquisition system.

  The 5500 includes digital anti-aliasing filters, A/D, dual-channel input, signal storage, realtime digital signal processing, high resolution display, a thermal printer, and 1.5M-bytes of program ROM. The 5500 performs dynamic signal analysis functions such as spectrographic and FFT spectrum analysis, waveform display, LPC analysis/synthesis, and contour display. IBM PC interface hardware and software is available.

9.3.31 Kontron Electronics

Nature of Product(s): Algorithm Development Hardware, Disassembler
Functional System(s): N/A
Device(s) Supported: TMS32010

- Logic Analyzer

  The Kontron Logic Analyzer (LA) is a general-purpose logic analyzer that features up to 64 channels, a memory depth up to 8K per channel, and a maximum clock rate of up to 100 MHz (500 MHz with an optional high-speed module). Capabilities include recording with four separate clocks (qualified by six external signals each), separate glitch memory, glitch triggering, sequential triggering with up to 14 levels, and transition/data-qualified recording. A trace disassembler option is particularly useful for microprocessor development.

- LA TMS32010 Disassembler

  The LA TMS32010 Disassembler converts the traced data recorded by the logic analyzer (LA) into TMS32010 mnemonics. The disassembler displays all instructions fetched from external program memory during the program execution. (Program modules contained in the on-chip masked program ROM of the TMS32010 microcomputer cannot be recorded and disassembled.) By doing a reverse assembly, sections of TMS32010 code pertaining to the triggered events can be examined for software/hardware analysis. The Kontron LA can only trigger on recorded clock-qualified data, user-specified with trigger words and sequence menus. Predefined trigger words set up the logic analyzer to search for a hardware reset, interrupt acknowledge, port read or write cycle, table read (TBLR), and/or an instruction fetch.

  When used in conjunction with the Kontron LA TMS32010 Disassembler, the TMS32010 Evaluation Module incorporates the powerful trace features of most emulators. With a Kontron Logic Analyzer already present in a development station, this configuration provides an inexpensive alternative for emulator capability and performance.

9.3.32 Logic Automation

Nature of Product(s): Algorithm Development Software
Functional System(s): Apollo, Sun, VAX
Device(s) Supported: TMS320C25

- TMS320C25 SmartModel

  The TMS320C25 SmartModel is a hardware verification behavioral model. Hardware verification SmartModels represent a microprocessor by simulating its bus cycles, rather than by executing assembly language instructions. Simple commands from the Logic Automation Processor Control Language (PCL) control the model. This allows the designer to simulate running a board or system under the control of a microprocessor without any assembly language coding, debugging, and loading. For Hardware system debugging, a Hardware Verification SmartModel and its PCL command file offer a major advantage over any other approach.

  The TMS320C25 SmartModel executes all TMS320C25 local bus cycles:

  - Program read
  - Program write
  - Data read
  - Data write
  - I/O read
  - I/O write
  - idle

  In addition, other TMS320C25 SmartModel functions include:

  - ST1 register can be configured to allow serial port transmission and reception via the DRR, DXR, RSR, and XSR registers).
  - TIM and PRD registers can be configured to cause an internal timer interrupt every PRD + 1 cycles).
  - Internal and external interrupts via IFR and IMR registers.
  - HOLD/HOLDA signals can be used to cause the CPU to release the bus.
  - READY signal can be used to delay the completion of a cycle to support slow peripheral devices.
  - RESET signal can be used to reset the processor any time during simulation.
  - SYNCH input can be used to cause the clock state to go to Q1.
  - Communication signals DS,PS,IS,RW, and STRB.
  - BR, MSC, IACK, XF, BIO, and MCMP pins are partially supported via the *load_pin* and *examine_pin* commands.
  - All supported internal registers can be accessed via the *load_reg, examine_reg, set_reg_bits, and clear_reg_bits.*

9.3.33 Macrochip Research Inc.

Nature of Product(s): Emulator
Functional System(s): MACINTOSH, IBM PC, VAX
Device(s) Supported: TMS320C10,TMS320C25

- 320C10 DSP ICE PAK In-Circuit Emulator

  Coupled with a MACINTOSH, IBM PC, or VAX, the 320C10 ICE PAK provides for a low cost, realtime development capability. The 320C10 ICE PAK contains a TMS320C10 device, 4K-byte x 16-bit of 70-ns program overlay static RAM memory, a microcomputer, and RS-232 communications port. It replaces the target TMS320C10 DSP chip in systems under development and connects to the host computer's (or terminal's) RS-232 port. With the ICE PAK, programs can be downloaded directly into the TMS320C10 device's program memory space and then executed in realtime. Program memory may be disassembled, and registers and accumulators can be examined and changed. In addition, breakpoints can be set on instruction fetches in order to examine and modify registers, accumulator, and stack contents at any point in program execution and single step operation. The standard ICE PAK features zero wait-state, nonintrusive realtime in-circuit emulation at clock speeds up to 20-MHz.

  The ICE PAK is "parasitic" in the sense that it requires the target's power supply and clock source present at the target DIP socket for proper operation. Being parasitic in operation, ICE PAK represents a true "plug 'n go" approach to in-circuit emulation. There are no hardware switches or jumpers to configure and no special cabling requirements with which to contend. Just plug the 40-pin DIP emulation plug into the target DIP socket and connect the 6-foot RS-232 cable to the host computer's RS-232 port, power up the target system and it's up and running. The user's favorite communications software may be used for communication with the ICE PAK's firmware monitor/debugger.

  With the exception of $\overline{WEN}$, $\overline{MEN}$, $\overline{RESET}$, and A0-A11, all signals presented at the ICE PAK 40-pin DIP emulation plug are the actual TMS320C10 pin signals, and are not impeded by logic. The 320C10 ICE PAK achieves 20-MHz operation because the TMS320C10 device is located in the DIP emulation plug, just 0.5" away from the target socket. The 70-ns emulation program overlay RAM memory is housed less than 3.5" away in the ICE PAK enclosure, thus minimizing capacitive and inductive loading. The ICE PAK consumes only 25-mA more than the TMS320C10 device, and satisfies all it's power requirements from the target socket. This eliminates any power supply differences between the target system and the emulator during operation.

- 320C25 ICE PAK In-Circuit Emulator

  The 320C25 ICE PAK performs the same function for the TMS320C25 that the 320C10 ICE PAK performs for the TMS320C10. The major differences are the program overlay memory, emulation plug, execution speed, and the signal differences noted below.

The 320C25 ICE PAK has 16K-bytes x 16-bits of 35-ns program overlay memory, a 68-pin PGA emulation plug, and performs at clock speeds up to 50-MHz. With the exception of $\overline{PS}$, $\overline{RESET}$, and $\overline{HOLD}$, all signals presented at the ICE PAK 68-pin PGA emulation plug are the actual TMS320C25 pin signals, and are not impeded by logic. $\overline{RESET}$ and $\overline{HOLD}$ go through one AHCT gate delay.

- Monitor/Debug Firmware Description

  Both the 320C10 ICE PAK and 320C25 ICE PAK feature a complete monitor/debug command set in firmware so that no special driver software is required for the host system to communicate with the ICE PAK. The monitor/debugger gives the user the ability to download, examine, modify, copy, and upload programs using the host PC or MACINTOSH as a smart terminal.

  A unique feature of the monitor/debugger is that the break handler may be modified by the user to satisfy special debugging requirements such as displaying the contents of any eight memory or I/O locations during a break in addition to the usual internal DSP registers and stack. Break points may be entered anywhere in program memory on code boundaries.

9.3.34 Mathematical Systems Design, Inc.

Nature of Product(s): Application Hardware
Functional System(s): Multibus
Device(s) Supported: TMS320C25

- Model RTP-25/102 Digital Signal Processor

  The RTP-25/102 is a Multibus I DSP board based on the TMS320C25. It is uniquely suited for applications involving realtime signals in analog or digital form. To avoid system slowdown due to data bus bottlenecks, signal input, array acquisition, and host transfers can occur simultaneously and independently of DSP program execution. The RTP-25/102 combines signal processing and analog conversion on a single board and occupies a single slot in a system. The **RTM-102 Module** is a plug-on board containing the A/D and D/A circuits, and allows for future options to satisfy various conversion or coprocessor requirements.

  Signal I/O is accommodated by separate input and output ports for 16-bit digital data, and coaxial connectors for analog input and output. The RTM-102 module provides 16-bit A/D and D/A systems for 50 kHz throughput, with sample rate programmable by on-board timers.

  The memory structure features a double-buffered memory (2K- x 2K-word) for signal acquisition and another for host transfer. A programmable timer, sequencer, and address counter provide automatic acquisition of data blocks from the digital port or A/D converter, without DSP intervention.

  Command and status registers for both host and DSP control are featured along with two user-definable mailbox registers. The sources for both the DSP and Multibus interrupts are jumper-configurable.

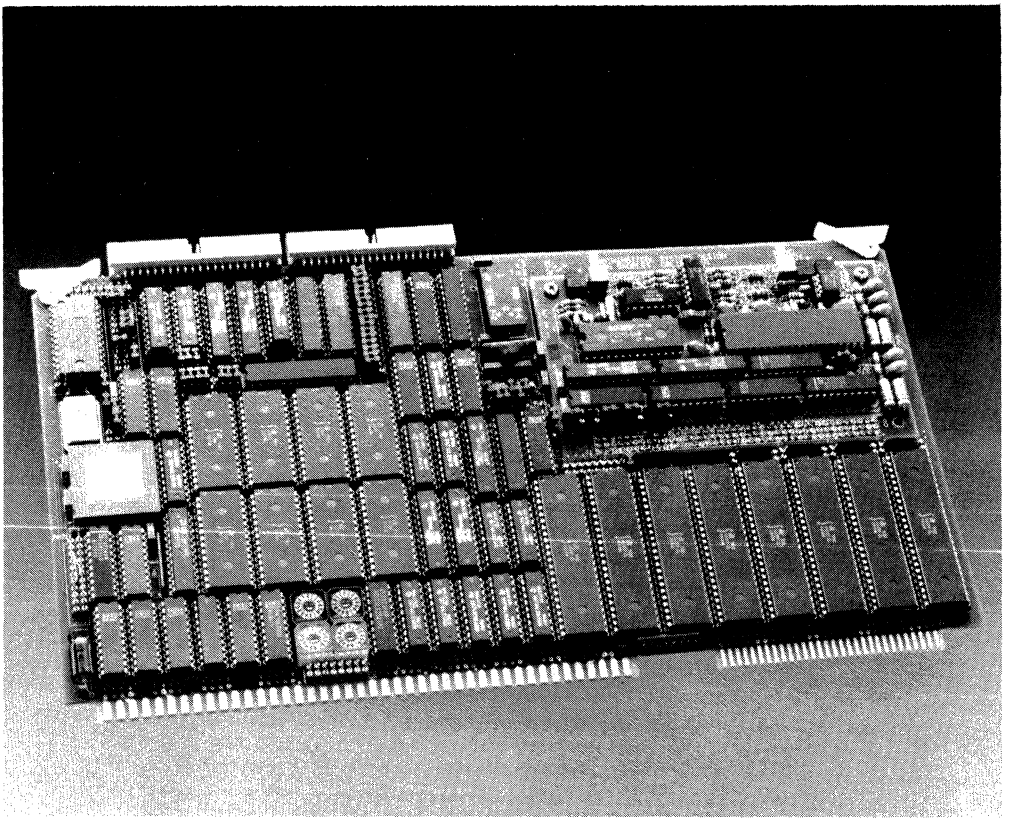

Figure 9-10. RTP-25/102 Digital Signal Processor from Mathematical System Design

9.3.35 Metme Corp.

Nature of Product(s): Algorithm Development Hardware, Application Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- Analog Applications Development System (AADS)

  The AADS was designed for TI DSP product development. AADS, together with a software development system, is everything needed to take a DSP product from conception to production.

  AADS exhibits the following qualities:

  - INTERCHANGEABILITY: Allows the choice of TMS32020 or TMS320C25 DSP engine, memory, and analog front end.
  - SHORTER DEVELOPMENT CYCLE: Two to four months can be saved in product development time due to the unique ability of the AADS to allow creation of any DSP algorithm interactively with final hardware.
  - FINAL HARDWARE EVALUATION: AADS allows quick implementation of the users specific hardware so the algorithm can be fine-tuned for optimal system performance and cost savings.
  - ACCELERATED ALGORITHM DEVELOPMENT: The secret to rapid algorithm development is this tool's exceptional ability to provide immediate positive feedback to the design engineer.

  DSP systems are composed of both hardware and software. The software, often called an algorithm, is developed on a software development system. The hardware and it's interface to the software is developed on the AADS. The AADS is an integrated software/hardware product development board system. It allows the user to easily select and install the specific DSP circuit components required for optimal product performance. In addition, the AADS provides immediate feedback on analog and digital signal behavior when the algorithm is modified.

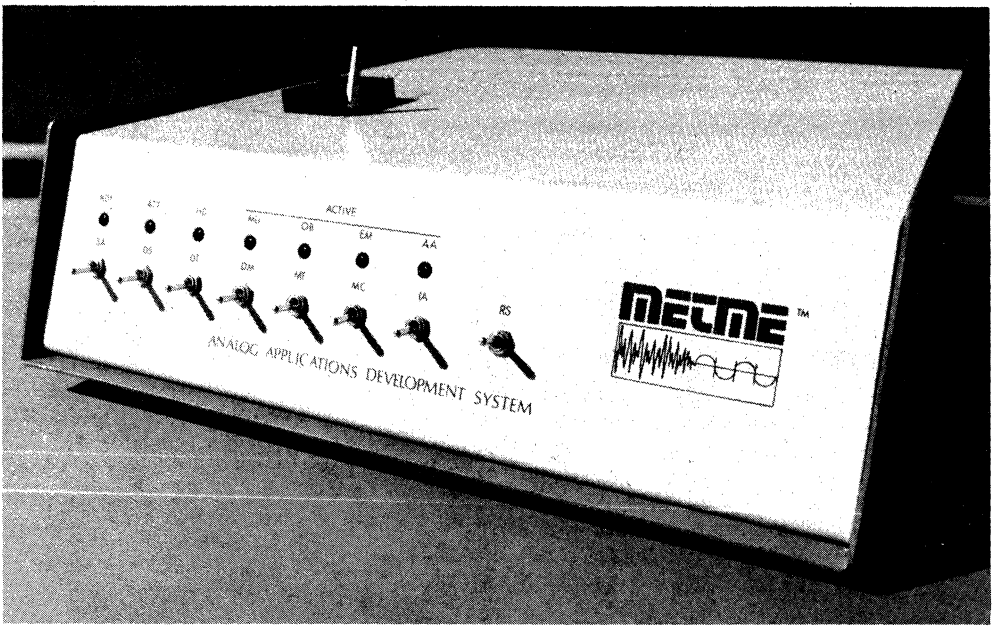

Figure 9-11. Analog Applications Development System (AADS) from Metme Corp.

- DSP Target Application Board (TAB)

  TAB is a complete TMS320 DSP system customized on a single 3" x 6" printed circuit board. The TAB incorporates all of the hardware required to allow an algorithm to process a realtime analog signal. The unit utilizes a TLC32040 Analog Interface Circuit (AIC) and either a TMS32020 or TMS320C25 DSP engine. The TAB provides the user with an immediate finished product, ideal for rapid product introduction.

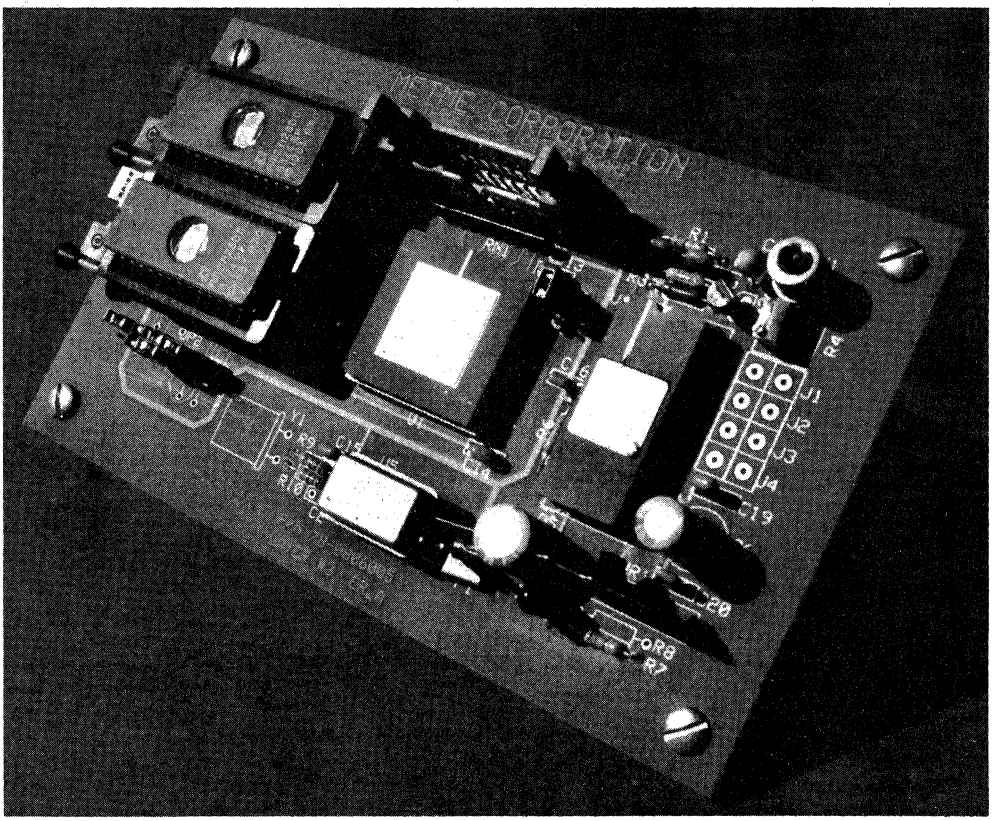

Figure 9-12. DSP Target Application Board (TAB) from Metme Corp.

- Custom DSP Circuits

  Metme also supports custom DSP circuit design. Submit a copy of the finished schematic including memory, I/O connectors, coprocessor connections, and specific device nomenclature.

9.3.36 Microcraft Corp.

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software, Assembler
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS32020, TMS320C25

- DSP-320 Development System

  The DSP-320 is a cost-effective DSP development system for the TMS32010, ideal for research labs, colleges, and universities desiring to explore and study DSP applications. A DSP-320 consists of a digital board **(DSP-D)** and an analog board **(DSP-A)**. A CRT terminal or personal computer, power supply, and other instruments such as signal sources and oscilloscopes are supplied by the user as needed. Comprehensive manuals are provided with the boards.

  The DSP-D contains all the relevant digital circuits to load, store, and run programs for the TMS32010. It incorporates an 8039 microprocessor, fast static RAM, and system ROM. Communications to the DSP-D via an RS-232 port and a three-wire connection (TX, RX, and GND) allow a variety of CRTs and PCs to communicate with the system. The DSP-D can be interfaced to analog subsystems via a 40-pin IDC connector.

  The DSP-A is an economical companion board to the DSP-D board. It enables the user to begin applications development immediately without the manufacturing delay associated with specialized analog interfaces. The DSP-A also includes low-resolution data converters and port decoders for expansion.

- DSP Experiment Manual (DSP-EM)

  The DSP-EM discusses hardware and software implementations of specific DSP concepts, including the equations needed to implement actual DSP tasks. Material covered includes signal generation, descrete Fourier Transforms (DFT) as well as IIR, FIR, and adaptive digital filters. All experiments are designed to run on the DSP-320 system.

- ASM-10 Assembler

  The ASM-10 assembler is written in C language and features TI mnemonics, PC-DOS compatibility and TI-compatible files. Object files are generated with the easy-to-use, low-cost ASM-10 can be directly downloaded to Microcraft's DSP-320 development system.

- Digital Filter Design (DFD)

  The DFD is ideal for design of FIR (multi-bandpass/stop, differentiator, and Hilbert transforms) and IIR (Butterworth, Chebychev I and II, and Elliptic) digital filters. The DFD designs a filter based on user-specified characteristics of the desired filter including filter type, sampling rate, cutoff frequency, passband ripple, or stopband ripple. The DFD provides on-screen frequency response plots and is compatible with CGA/EGA/HGA graphics adapters for CRT frequency response plots. Printer programs for hard copy output of CGA/HGA graphics are also

provided. The DFD manual includes design examples and sample TMS32010 implementations. It can also be used for designs involving the TMS32020 and TMS320C25.

9.3.37 MicroWorkshop

Nature of Product(s): Emulator
Functional System(s): IBM PC
Device(s) Supported: TMS320C10

- MicroWorkshop Series 16 Development System

  The Series 16 is a PC-based in-circuit emulator for the TMS320C1x. It simplifies code development and displays code, text, and captured waveform graphics simultaneously, an industry first for PCs. It consists of custom enhancement boards and editor/assembler/testing software written Microsoft Windows, the Series 16 turns any IBM PC/XT/AT, 386, or compatible into a highly advanced workstation.

  The MicroWorkshop is a complete development system offering in-circuit emulation and operation up to 40-MHz, allowing the user to test all functions at the full speed of the application. A signal capture capability permits the acquisition and storage of signals in digital form from either the 320 DSP or from an external source. This allows precisely repeatable validation tests from real data.

  An integrated waveform display function with autoranging is provided. Waveforms can be stacked or overlapped for easy comparison and evaluation. User selected portions of the displayed signal can be processed through an FFT algorithm to provide a spectral display.

  In-circuit emulation is accomplished by use of the target TMS320C10 processor in an external pod. This allows complete testing of the application hardware and software in the intended environment. The system is capable of emulating four processors simultaneously in a multi-processor configuration. In emulation mode, the inclusion of two programmable counters enhances the setting of complex and conditional brakpoints and traces. Program variables can be continuously displayed in user-selected "watch windows".

  Simulation capabilities allow the user to test applications without building hardware models. Since the target TMS320C10 is used for most instruction execution, the speed is much faster than development systems using only software simulation.

  With the integration of Microsoft Windows, The MicroWorkshop provides side-by-side on-screen display of waveforms and the related digital information. This feature eliminates the need for the designer to move back and forth between functions to completely evaluate various portions of the application program. In addition, the system makes full use of a graphical object/verb user interface, complete with icons, window, menus, and pointing devices, to simplify use of the development environment. This user interface is similar to those found on conventional engineering workstations.

  The MicroWorkshop has an internal communications link that permits data or programs developed on VAX or other mini-computers to be downloaded and accessed, even while in the development cycle. Data developed on the workstation can be uploaded for analysis to other computers.

A "turbo" assembler/editor with syntax checking is included in a single module. The in-memory editor/assembler reduces the time required to develop code by days, even weeks, over methods requiring separate editing, assembling, and testing. The direct assembly and download of code allows total symbolic reference during trace, breakpoint, and other debugging setup and display routines. Testing set-up is dependent upon the program rather than some artificial location within the system's memory.

9.3.38 Momentum Data Systems

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC, PS/2
Device(s) Supported: TMS320C1x, TMS320C2x

- Filter Design and Analysis System FDAS1 and FDAS2

  Both TMS320C1x and TMS320C2x code generation is available on the FDAS1 and FDAS2. FDAS1 features both FIR and IIR filter design and system analysis capability for the determination of transfer function characteristics. FDAS2 also incorporates advanced design capabilities for Hilbert Transform and Arbitrary Magnitude filters, IIR Bessel filters, a logarithmic frequency scale option, digitization of S-domain transfer functions as well as increased filter lengths. Both systems offer ease of use, menu-driven screens, 8- to 32-bit coefficient quantization, filter specification retention, and easy to read documentation. All design calculations are performed in 64-bit floating-point arithmetic.

9.3.39 Navtrol Company, Inc.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS320C25

- C25 DSP Prototyper

  This TMS320C25-based board offers 40-MHz operation and extensive prototyping area. It is designed specifically for sampled data applications. Volumes of data may be transferred in batches during each sample period (in either or both directions) through use of special I/O memory. The Prototyper offers a proven base system that allows designers to concentrate efforts on the design of hardware and software for a specific application. Debug software and disassembler are included.

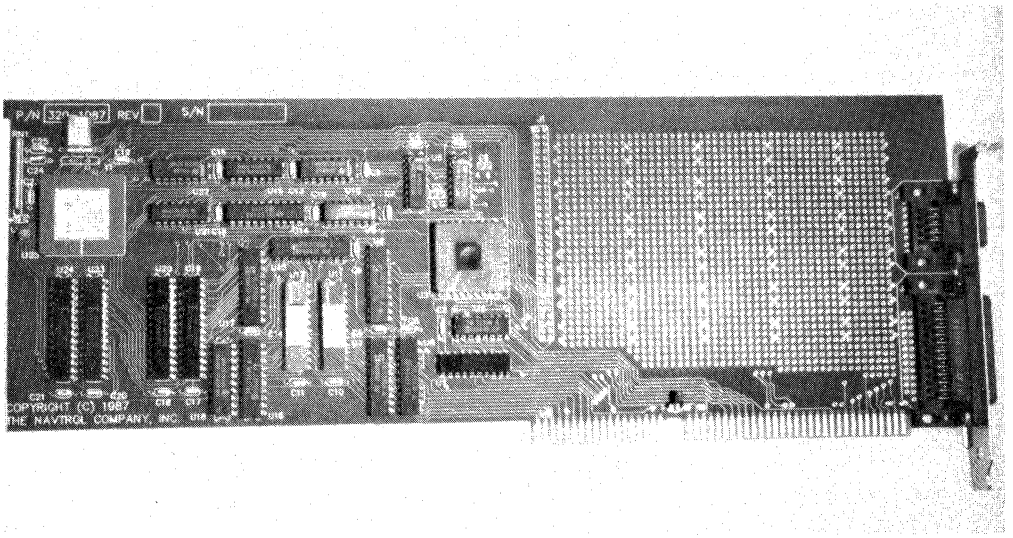

Figure 9-13. C25 DSP Prototyper from Navtrol Company, Inc.

9.3.40 Pentek, Inc.

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): Multibus, VME Bus, IBM PC
Device(s) Supported: TMS32020, TMS320C25

- Models 4081, 4182, and 4282 Digital Signal Multi-Processor Boards

  Models 4182 (Multibus I) and 4282 (VME Bus) digital signal multi-processor boards each has three TMS320C25 DSPs and no wait-state static CMOS RAMs. Both feature a flexible interrupt system for realtime applications, interprocessor serial communications bus, and stand-alone operation with 32K-word EPROM. The Model 4182 has a Multibus host interface via dual port RAM. The Model 4081 is the same as the Model 4182 except it uses TMS32020 DSPs.

- Models 4062 and 4262 Single Channel Analog I/O Boards

  Models 4062 (Multibus I) and 4262 (VME Bus) each feature high performance 7th-order anti-aliasing filter, 16-bit A/D converter with matching sample and hold plus 16-bit D/A converter with smoothing filter. They also have FIFO buffering for high processor efficiency and 50-kHz maximum programmable sampling rate.

- Model 4068 Eight Channel A/D Converter

  The features of the Model 4068 include 12-bit A/D converter for eight analog inputs, 100 kHz maximum programmable aggregate rate, and FIFO buffering for high processor efficiency.

- Model 4900 MON Debugging and Development Utility Software

  The MON development software has an in-line assembler and disassembler, set program breakpoints and run/single step functions. It also features inspect/fill/modify on-board memory, inspect/modify registers, and PROM programmer download. C source code is supplied with the software. MON greatly facilitates program development for Pentek's Multibus and VME DSP boards. It takes advantage of the capabilities of the IBM PC and the wealth of high-performance and reasonably-priced PC-based software packages written for the TMS320 family of DSP products.

  In a typical computer environment such as Multibus or VME bus board cage, there is usually a host CPU board which may or may not be supported by a disk operating system. In either case, it may not be desirable or possible to duplicate the PC-based development software on the host system.

  MON provides all the vital links between such a system and the installed Pentek DSP board and the IBM PC. MON includes the following items:

  - Disk Software for the IBM PC
  - Disk Software or EPROMs for the Host CPU
  - EPROMs for the System 4080

In this powerful but inexpensive system, all high-level operations such as program preparation, assembling and linking are performed on the IBM PC using a common word processor and cross software for the TMS32020 and TMS320C25. Compilers, simulators, assemblers, linkers, and loaders are all available from Texas Instruments and third-party vendors.

9.3.41 QUALCOMM, Inc.

Nature of Product(s): Digital Synthesizer Chip
Functional System(s): N/A
Device(s) Supported: TMS320 family

- Q2334 Dual Direct Digital Synthesizer (DDS)

  The Q2334 DDS chip spans the gap between TMS320 signal processing and the requirement to generate high precision, high frequency sine waveforms. It connects directly to the TMS320 address/data bus for control of the operating mode and frequency/phase control for generation of sine waveforms. The DDS synthesizes these waveforms by dividing a higher reference frequency and performing an on-chip high-precision digital sine lookup function. Reference frequencies as high as 30-MHz are supported, allowing the user to generate output frequencies up to the Nyquist limit of 15-MHz with a frequency resolution of 0.007-Hz. Phase truncation and amplitude truncation with signal-to-noise ratios of 76 dB and 72-dB, respectively, are provided. Additional synchronous modulation input signals allow the Q2334 to be used as a single-chip PSK, FSK, or MSK modulator with frequency and phase shift times of one sample period (ie., 33-ns) while maintaining phase coherence when changing frequencies. Two complete, independent DDS circuits are included on the Q2334 providing for very efficient implementations of full-duplex systems, quadrature oscillators, and spread spectrum modulators. It is also useful for implementations of very precise phase-locked loop (PLL) circuits. The Q2334 is packaged in a 68-pin PLCC.

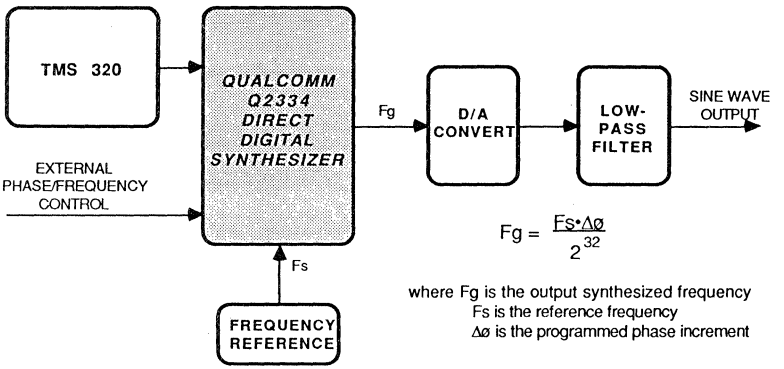

Figure 9-14. Dual Direct Digital Synthesizer (DDS) from QUALCOMM, Inc.

9.3.42 Rapid Systems, Inc.

Nature of Product(s): Application Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- Model R320 DSP Engine

  The R320 is a DSP engine (hardware and software) ideal for TMS32010 development or for integrating the TMS32010 into an OEM application. The TMS32010 is operated at 20-MHz, utilizing 4K-words of dual-ported RAM, also accessible to the PC, and direct I/O data transfer between the TMS32010 and the PC. Accompanying software contains extensive source code, examples of upload/download routines (digital filters, FFTs, signal averaging, etc.), and ready-to-run executable files in TURBO PASCAL and TMS32010 source code. Software features include a turnkey FFT algorithm with documentation and assembly language device drivers for high-speed screen display.

9.3.43 Sarin Incorporated

Nature of Product(s): Assembler, Simulator, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS320C10

- Software Development Package

  This package allows a designer to write and debug programs to be run on the TMS32010. It includes an assembler **(pAsm 10)**, simulator **(pSim 10)**, a full macro library and a comprehensive bundle of mathematical subroutines.

- µPipe 10 PC-Based Dual TMS320C10 Platform

  The µPipe 10 is designed to accept plug-in modules, the basic board features two processor nodes. Each node, in addition to the TMS320C10, contains 4K-words of high-speed RAM and 256-words of boot ROM.

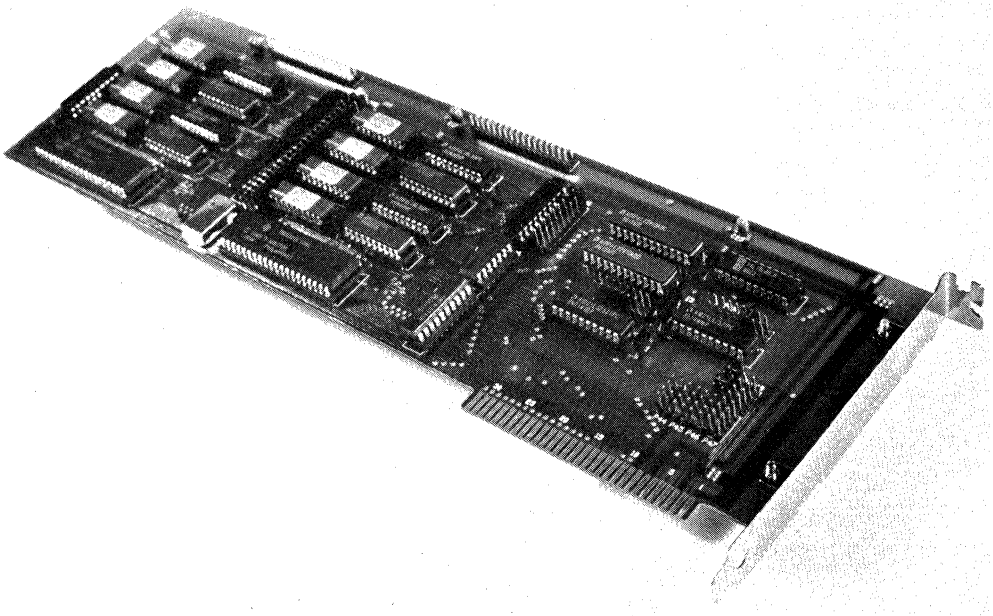

Figure 9-15. PC-Based Dual TMS320C10 Platform from Sarin

- Sarin Bulletin Board Service

  The Sarin bulletin board service offers on-line support, application notes and product updates. It operates from midnight to 6:00 p.m. (EST) Monday through Friday, and is accessed by dialing 301-356-4532.

9.3.44 Schlumberger Technologies

Nature of Product(s): Test Programs
Functional System(s): Sentry 7/8/10/20/21 test system
Device(s) Supported: TMS32010, TMS32020

- Sentry Test Programs

  Sentry Test Systems provides a ready-made solution to a TMS32010 or TMS32020 customer's incoming test procedure with TMS32010 and TMS32020 test programs for Sentry 7/8/10/20/21 test systems using either a 60- or 120-pin high-speed or high-voltage test head. The program tests DC parameters (V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{CC}, and input leakage current), and verifies device functionality at full frequency and V_{CC} extremes. Specific device attributes tested include the arithmetic logic unit (ALU), auxiliary registers (ARs), branch instructions, program counter (PC), status register, general registers, general I/O, interrupts, multiply, internal RAM, and device timings. TMS32020 features, such as the repeat (RPT) instruction, $\overline{\text{HOLD}}$, READY/$\overline{\text{HOLD}}$, READY, serial mode, and timer, are also tested. In addition, device functionality with an external 8-MHz crystal oscillator is verified.

  The TMS32010 and TMS32020 Sentry test software includes the test program, test patterns, performance board, and documentation.

9.3.45 Signal Technology, Inc. (STI)

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC, VAX VMS/UNIX, PDP-11, RT-11, RSX-11
Device(s) Supported: TMS32010

- ILS/DSP

  Signal Technology, Inc. (STI) offers two separate Interactive Laboratory System (ILS) packages tailored toward the specific application needs of digital signal processing and speech processing. The ILS/DSP package contains programs for advanced digital signal processing such as FFT, convolution, correlation, and spectral density estimation. The advanced DSP capabilities allow the processing and display of real and complex data types.

- ILS/Speech

  The ILS/Speech package consists of speech processing programs that provide various types of speech analysis, parameter editing, formant tracking, pitch extraction, spectrogram displays, and autoregressive spectral displays. It also allows the use of dynamic programming for template generation and distance evaluation in word recognition experiments.

- DACS

  DACS is a set of FORTRAN main programs and callable subroutines for analog-to-digital conversions directly to disk files, digital-to-analog conversions directly from disk files, and data compression/expansion for the efficient storage of digitized data. Both A-law and μ-255-law compression tables are provided with DACS.

9.3.46 Signatec

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS320C25

- DASP100 High Speed Data Acquisition and Signal Processing System

  The DASP100 is a powerful acquisition and signal processing system based on the TMS320C25 which combines a 100-MHz (maximum clock speed) 8-bit digitizer with a 16-bit signal processor capable of executing most instructions in a single 100-ns cycle. The DASP100 is a circuit board assembly designed for personal computers using the the PC/AT bus. The system provides 256K-bytes of data RAM memory and 16K-words of DSP RAM memory. These are expandable by use of an optional piggyback board (**MX1**). All memory is directly addressable by the PC through a block switching scheme.

  The DASP100 is useful for a wide range of signal acquisition and processing applications, and is optimized for those requiring high speed. Three operating modes are implemented: continuous, pretrigger, and burst. The burst mode is especially powerful as it stores information only while a signal is present and places separators in the data to distinquish signal end points. The DASP100 is designed for multi-processor applications. A board connector, internal to the PC, is used to mechanize an 8-bit parallel data communication port. Up to three processors may be connected in a master/slave arrangement. Handshake lines facilitate the passage of data and processor synchronization.

- MX1 Memory Expansion Board for DASP100

  The MX1 is a memory expansion board for the DASP100 which can expand the data RAM capacity up to 2M-bytes, and the signal processor memory up to 32K-words. This board is useful for transient recording applications where a long data record is necessary. It is also useful when more than 16K-words of DSP memory (the amount installed on the DASP100) is required. Memory expansion may also be needed for signal processing applications where a large amount of information must be acquired and dead time for signal processing or data transfer is not acceptable.

- dScope Digital Oscilloscope Software for the DASP100

  dScope is a software package which allows the DASP100 to be used in a manner similar to a digital oscilloscope. Although the real power of the DASP100 is unleashed through custom application programs written for the digital signal processor, dScope allows the user to obtain useful information within hours after receiving it. An optional version (**dScope/FFT**) adds frequency domain to the standard dScope package. This option allows the DASP100 to be used as both a digital oscilloscope and a spectrum analyzer.

dScope provides the means to control the operation of the DASP100 and to graphically display recorded signal data. The program has two main operating modes: setup and display.

The setup mode provides the ability to set the hardware parameters of the system and to activate one of the system operating modes. The display mode allows the operator to view signal data as an amplitude versus time plot. An extensive list of commands allows for quick access to signal data anywhere in RAM, and for expanding or compressing the displayed signal.

Because of the graphical nature of the program, dScope requires an EGA monitor and video adapter, or a board and monitor capable of operating in the Enhanced Graphics mode. While the software will operate on any IBM PC compatible system with at least 256K-bytes of memory, the DASP100 requires a 16-bit bus computer compatible with the PC/AT.

- cBuild Custom Applications Building Software

  cBuild is a software package which makes it possible for users of the DASP100 to write their own custom application programs in the shortest possible time. Application programs to operate the DASP100 as a near-realtime signal processor consist of software to operate the PC (286/386 code), and software to operate the DSP. cBuild provides functional modules written in C which greatly facilitate this process. Modules for developing PC software are written in Borland's Turbo C. Modules for the DSP are written in TI's C compiler for the TMS320C25. These modules minimize the need for understanding the intricacies of the hardware. Prerequisites for using this package are a working knowledge of the C language, Turbo C by Borland, and TMS320C25 C compiler by Texas Instruments.

- CA001 High Speed Compression Amplifier with 80 dB Dynamic Range

  The CA001 is an amplifier module designed for applications which require a large amplitude dynamic range. It has a compression characteristic which is very close to logarithmic. When used with the DASP100, it makes possible the recording of signals over an 80-dB amplitude range with an 8-bit digitizing system. Amplitude resolution is approximately 3.5 percent over the entire 4 decade amplitude range.

  The CA001 is a DC coupled device with a bandwidth of 40-MHz. It is built on a 2.7" by 2.6" circuit board which plugs directly onto the DASP100 in piggyback fashion.

  Every device is individually characterized to provide the greatest possible accuracy in converting the compressed data back to linear values. This characterization table is supplied with the CA001 both on disk and in hard copy form.

- LA001 Linear, Switched Gain Amplifier

  The LA001 should be used in situations which simulate the operation of a digital oscilloscope. This includes situations where the input signals have a dynamic range of 20:1 or less, or where the operator can change gain ranges interactively.

The LA001 is a linear amplifier module designed for applications which do not require a large amplitude dynamic range. It has four gain ranges which are software selectable to provide full scale display of signals with amplitudes from 60-mV to 2-V. Bandwidth is 40-MHz, but may be set at reduced values of 5-MHz or 1-MHz via jumpers. For some applications, it may be necessary to use external filters to prevent aliasing errors.

The LA001 is packaged as a circuit board assembly 2.7" wide by 2.6" high.

9.3.47 Signix Corp.

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC 7
Device(s) Supported: TMS320 family

- DISPRO

  The DISPRO software system provides the capability of designing, simulating, and evaluating digital filter operations for implementation on VLSI devices such as the members of the TMS320 family. The software system uses an IBM PC or compatible with CGA or EGA graphics and a 8087/80287 math coprocessor.

  DISPRO is completely interactive, making full use of color, custom-designed input screens with pull-down menus and pop-up dialogue boxes, and full screen parameter entry with redo capability. Retention of parameter values within modules aids in rapid exploration of designs and graphic plots. Full control over tradeoff between filter performance and filter order/length. All numeric output is in engineering notation format.

  The features of the DISPRO software system include:

  - *IIR Filters*: Butterworth, Chebyshev I and II, plus Elliptic filters up to order 30. LP, HP, BP, and BS characteristics. Coefficients are scaled to combat overflow in fixed-point arithmetic. Printout of pole and zero values for floating-point and quantized coefficients.
  - *FIR Linear-Phase Filters:* Parks-McClellan-Remez to length 430. LP, HP, BP, BS, and Multiband (up to seven bands). Warnings issued for parameter combinations which may cause design failure. Arbitrary magnitude response specification with frequency (Hz) and magnitude (linear or dB) point pairs input from keyboard or data file. Keyboard input can be saved to a data file. Filter response may also be compensated for the Sin(x)/x rolloff of a digital-to-analog converter. Kaiser-windowed to length 1023: LP, HP, BP, and BS characteristics. Complex filters, and lengths to 16,383 are available as options.
  - *Coefficient Wordlengths:* 32-bit floating-point, 3- to 24-bit integer.
  - *Frequency Response:* Graphical and numeric output for any coefficient wordlength. Independently specifiable ranges and scales for frequency and magnitude axes. Phase and delay plots for IIR. Transfer of screen graphics to Epson and IBM-graphics compatible printer.
  - *Time Response for IIR:* Impulse response and forced time response computation in floating-point and fixed-point arithmetic. Fixed-point arithmetic capabilities: wordlengths from 3- to 24-bits, single or double length accumulator, 2's complement or saturating accumulator, truncation or rounding, coefficient less than or equal to computational wordlength. Test signal ar sum of sinusoids and gaussian white noise. FFT-based spectral analysis for time data.

- *Time-Domain Plotting:* Impulse response for IIR and FIR; forced time response for IIR.
- *Benchmark Timings (10-MHz 80286 PC with 80287-8 Math Co-processor:*
  Equiripple FIR, length N: N=50, 13 sec.; N=100, 47 sec.; N=220, 5.5 min.; N=330, 16 min.
  Frequency Response IIR, 500 spectrum values, order N: N=10, 9 sec.; N=20, 15 sec.; N=30, 22 sec.
  Spectral Analysis (FFT): 1024 real points, 2 sec.; 8192 real points, 15 sec.

9.3.48 Signum Systems Inc.

Nature of Product(s): Emulator
Functional System(s): IBM PC
Device(s) Supported: TMS320C10, TMS320C15, TMS320C17

- ICE Model E-232-DSP-10 In-Circuit Emulator

  The ICE E-232-DSP-10 is an in-circuit emulator designed specifically for DSP systems. It promises to ease the development of products in medical electronics, computers, communication systems, and other DSP applications. This new model solves the performance deficiencies of earlier DSP ICEs. Under interactive control, it provides realtime transparent emulation of all functions of TI's TMS320C10 at up to 32-MHz, including EPROM,UART, and extended address internal RAM without restrictions of any sort. SSI's new instrument is the only emulator on the market capable of doing all that; others intrude on the target system by stealing one or more of it's stacks, or are unable to emulate the entire range of it's capabilities in realtime.

  SSI's DSP emulator offers highly sophisticated event definitions which, when the conditions are met, can be used as breakpoints or trace controls. Three simultaneous sets of events are defined in terms of any or all of the following parameters, in any combination:

  - ADDRESSES: Any of 8K addresses or ranges of addresses.
  - DATA PATTERNS: Vectors up to 8K-bits wide; less than, greater than, equal to, not equal to, or don't care combinations on sets of vectors.
  - CPU OPERATIONS including Read, Write, I/O, and OpCode fetch.
  - EXTERNAL INPUTS with programmable polarities and logic qualifiers.

  In addition, events can be counted and/or delayed by the use of two 16-bit pass counters. An eight-level hardware sequencer is available to sequentially trigger to, from, or between any breakpoint event sets or pass counter values. Still other breakpoints can be triggered in the events of trace-full condition, watchdog timer out, or an illegal op code fetch.

  Other important features of SSI's new DSP emulator include in-line symbolic assemblers and disassemblers; two banks of 4K-byte overlay program memory for virtual memory operation; an eight-channel user logic state analyzer, and performance analysis hardware and software that allows the target system to evaluate the target code's efficiency, with both graphic and tabular displays.

Model E-232-DSP-10 is especially easy to use, owing to it's unique pop-up window interface technique. The user calls up various windows to display:

- Internal registers
- Internal and external memory
- Source code with single step, breakpoints, fast calls, and skip calls
- Sixteen user-defined setups for breakpoints, tracing, and other events

9.3.49 SKY Computers, Inc.

Nature of Product(s): Assembler, High Level Language Compiler, Algorithm Development Hardware, Algorithm Development Hardware
Functional System(s): IBM PC, PDP-11 Q-bus, VMEbus, Sun-3, MicroVAX
Device(s) Supported: TMS32010, TMS32020

- SKY320-PC

  The SKY320-PC is a realtime DSP board that incorporates a TMS32010. The communication focus of this board is a four-ported 64K data memory connected to the TMS32010 block, two 16-bit parallel I/O auxiliary ports, and an IBM PC-bus. The IBM PC is used as an I/O processor to perform initialization, switch analog test points in process control, act as system manager for several SKY320-PCs, and provide display control. The PC is also used as an image system, process controller, fast fixed-point array processor, and speech analysis system. Data memory is mapped to appear as host memory for both program and data. When coupled to an A/D board, the SKY320-PC aids in the development of realtime experiments and products.

  The TMS32010 block on this board consists of the TMS32010 microprocessor with its program, data, and arithmetic sections, SKY-supplied 4K-word static program memory, along with some special function logic to augment the TMS32010 processor. The four-ported data memory uses a 200-ns cycle time to match TMS32010 performance. This fast cycle time eliminates the need to modify the TMS32010's clock impulses to hold back a cycle while a data memory access is in process. The SKY320 I/O auxiliary ports linked to the data memory provide the following flexibility:

  - Use of ports as local data memory at a 5M-word (16-bit word) rate
  - Special designs to interface with A/D and D/A conversion devices
  - Linkage to camera and special input devices
  - Ability to chain together a series of SKY320 signal processor boards (output of first board into input of second board).

  Included in the standard SKY320 package are complete diagnostic software and documentation. One of the most important tools is a C compiler that allows fast algorithm development in the high-level C language for direct use of many of the high-speed features in the TMS320. The C compiler allows access to hardware features by providing a set of built-in functions that are replaced by code when invoked. These are used to directly access the large external data memory and program memory, directly use the I/O ports and any of the internal TMS320 registers, and check the condition codes.

  The software package also includes a macro preprocessor, an assembler, a symbolic debugger, host and SKY320 operating environments, and a large library of common mathematical functions. The macro preprocessor may be used prior to either compilation or assembly to generate sophisticated code such as FFT or fast 2-D convolution routines. The assembler can accept input directly from an assembly language source,

the macro preprocessor, or the C compiler. The output of the assembler is directly executable TMS320 machine language code that can be downloaded to the SKY320. The debugger can be used interactively to debug both assembly language routines and C programs.

- SKY320-Q

  The SKY320-Q is a DSP board operating on the DEC Q-bus, which allows the use of a DEC PDP-11 computer as the host machine for initialization, process control, coordination, and display. The Q-bus interface for the SKY320-Q provides a realtime software environment for TMS32010 applications. All of the features of the SKY320-PC board, including the software package, apply to the SKY320-Q board.

- SKY Challenger

  SKY Computers also supports a VMEbus board, the SKY Challenger, which is a fixed-point digital signal processor especially designed for high-speed applications, such as speech and image processing, digital filtering, data compression, vibration analysis, and realtime control.

  The heart of the SKY Challenger's computation power is the TMS32020 DSP chip. The Challenger uses two TMS32020s and matches them with static RAMs to provide exceptionally high-speed arithmetic and signal processing power. The TMS32020s are configured in a master-slave arrangement. The master processor controls all the Challenger's operational functions in addition to providing arithmetic processing. The slave processor is dedicated to running arithmetic data and as such provides a flexible resource for other functions. In addition to the two TMS32020s, other hardware features include separate high-speed program and data memory (64K words each), bus interface, auxiliary ports for off-bus data acquisition, and a high-speed auxiliary bus for block data transfers.

  SKY Challenger comes fully software-supported with a C compiler and a host of well-described macros and subroutines. Helpful signal and image processing libraries are also included. The software environment of the Challenger consists of an assembler (SKYASM), a linker (SKYLINK), debugger (SKYDEB), and a macro preprocessor (SKYMPP).

- TMS32020 Software Development Tools

  Sky Computers now offers a set of TMS32020 software development tools. These tools include a C compiler and crossware which operate on the IBM PC/XT/AT, Sun-3 systems, MicroVAX-II, and larger VAX systems. In addition to the C compiler, the cross development package consists of a macro preprocessor and assembler/linker. The new tool kit is targeted at users needing realtime computation in commercial, industrial, and aerospace applications. The C compiler is compatible with Kerigan and Ritchie and generates TMS32020 assembly code. The macro preprocessor provides in-line code and conditional assembly.

9.3.50 Sonitech International Inc.

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS320 family

- TMS320C30 Applications and Development (A/D) System

  The TMS320C30 A/D System is a cost effective solution to begin hardware and software development. This IBM XT/AT half-size board is ideal for PC based or stand-alone applications.

  The A/D System hardware features include:

  - Two banks of fast dual-access static RAM.
  - Full control of TMS320C30 from the host.
  - Memory expansion on the I/O bus of up to 16K-bytes x 32-bits.
  - Full parallel I/O expansion port with address, data, and control lines.
  - On board serial analog I/O (using the TLC3204x).
  - Both serial ports available for multiprocessor communications
  - Stand-alone operations through EPROM.
  - Multiple boards can be cascaded (any combination of serial or parallel connections) to deliver up to 120M-FLOPS of performance.

  The A/D System Software and Applications Features include:

  - Window driven user-friendly **EDSP-30 Workstation** (debugger, plotter, monitor, etc.) environment for efficient program development (see more complete description below).
  - Board and realtime plotting drivers for embedded applications.
  - Also included are some applications from the Sonitech DSP 'C' Applications Library (realtime spectrum analysis and display, filtering, and other application notes).

- EDSP-30 Workstation (For Custom Development)

  This workstation can be easily ported to the user's custom hardware. The EDSP (Evaluation, Development, Debugging, and Realtime Digital Signal Processing) is an IBM PC/XT/AT window based DSP workstation software for the TMS320C30 based hardware/applications/development systems. The EDSP will greatly enhance the users productivity with the tranformation of their PC (with their hardware) into a DSP workstation.

  EDSP features include:

  - Plotting
  - Signal generation
  - Program development
  - Universal data formatting and movement
  - Symbolic manipulation of data
  - 3-D plotting (optional)

- DSP 'C' Applications Library (DSP/LIB-1)

  This applications library is for TMS320C30 and DSP software development. These algorithms are implemented using the latest trechniques and are available in Microsoft 'C' library or source code form. The following are some of the routines in the library:

  - 1- and 2-dimensional transforms (FFT, DCT, DST)
  - Modern spectral analysis techniques
  - Cepstral analysis
  - Speech analysis (LPC)
  - BCH encoding and decoding
  - Convolutional encoder/decoder
  - PN sequence generation
  - Noise generation
  - Windows for spectral analysis
  - Polynomial root finding
  - Digital half-toning

  The library source code can be easily compiled using the TMS320C30 'C' compiler. Included with the library is detailed documentation on algorithm functionality and test software.

- Digital Signal Processing/Analog Interface Board-1 (DSP/AIB-1)

  The DSP/AIB series of boards are designed for DSP applications. The DSP/AIB series interfaces with TMS320C14, TMS32020, TMS320C25, and TMS320C30 DSP processors, SWDS, and other TMS320 based development boards.

  The DSP/AIB series board features are:

  - 14 bits dynamic range ADC and DAC (uses the TLC3204x)
  - Variable sampling rate up to 20-KHz
  - Anti-aliasing input and reconstruction filter
  - Synchronous and asynchronous ADC and DAC and programmable sampling rates
  - Serial port with direct interface to the host DSP processors
  - Fully software programmable
  - Half-size board for IBM XT/AT
  - Cascadable up to five boards

  This board is ideally suited for DSP system prototyping, evaluation, development, multiple channel acquisition, and embedded applications. DSP/AIB applications includes telecommunications, voice synthesis/analysis, biomedical, process control, product testing, and instrumentation.

- Digital Signal Processing/Analog Board for IBM XT/AT (DSP/AIB-2)

  In addition to the DSP/AIB series features listed above, the DSP/AIB-2 can fully control the acquisition, storage, and retrieval of data on the IBM XT/AT. Up to three DSP/AIB-2s (six channels) can be used simultaneously for data acquisition. An added benefit of this feature is that transfer to the PC can take place while DSP board outputs the data to analog output. This is ideal if the user needs to selectively record the acquired or processed data. Other features include telephone hand-set interface and output volume control. Menu driven software (in 'C') and source code is provided for acquisition control.

- Introduction to Practical Signal Processing Volume 1

  This DSP lab course, based around the TMS320C30, is for professionals and students interested in learning elementary and advanced topics in Digital Signal Processing. The objective of the course is to see 'digital signal processing in action'. The course offers hands-on learning experience for DSP theory and application with the help of the Sonitech EDSP Workstation. Only an IBM XT/AT and Sontech's TMS320C30 Applications and Development System is required.

- Advanced Practical Digital Signal Processing Volume 2

  The follow up of Volume 1 to the "Practical DSP". The course offers hands-on learning experience for DSP theory and applications.

- Product and Applications Development Services

  Sonitech offers proven expertise in development of products and applications based around the TMS320 DSP family including TMS320C30 based products requiring hardware, software, and applications.

9.3.51 Spectron MicroSystems, Inc.

Nature of Product(s): Algorithm Development Software, Simulator
Functional System(s): Sun-3
Device(s) Supported: TMS320C30

- SPOX Realtime DSP Operating System for the TMS320C30

  The cost of developing software for advanced realtime DSP applications continues to escalate. Dramatic improvements in hardware price/performance have led to a 'software crisis' in which new, more sophisticated DSP processors become available than applications can be developed.

  Spectron is addressing the issue of rising DSP software costs through SPOX, an operating system for the TMS320C30 that offers developers two important benefits: software productivity and application portability.

  Gains in productivity are achieved through high-level software functions, supported by SPOX, which insulate realtime DSP applications from the details of the hardware. These functions are equally important in achieving applications portability, in that the same programming interface currently implemented atop the TMS320C30 will be available on TI's next-generation DSP processors as well.

  SPOX differs from other operating systems in that it's capabilities are *application-specific*, much as the TMS320C30. SPOX augments a high-level programming language like C with software components targeted especially for realtime DSP: an extensible math package, configurable memory management, device-independent stream I/O, and multi-tasking kernel.

- TMS320C30 Simulator and Software Development for the Sun-3

  Spectron MicroSystems, Inc. also supports a TMS320C30 simulator for the Sun-3 Workstation. Software development for the TMS320C30 is supported on the Sun-3 Workstation with the TI TMS320C30 assembler/linker and C compiler. The simulator user interface, capabilities, and features are similar to those of the TI TMS320C30 simulator for the IBM PC and VAX VMS.

9.3.52 Spectrum Signal Processing Inc.

Nature of Product(s): Assembler, Simulator, Algorithm Development Hardware, Algorithm Development Software, High Level Language Compiler
Functional System(s): IBM PC
Device(s) Supported: TMS320C1x, TMS320C25

- TMS320C1x Development System

  The TMS320C1x Development System provides a complete development system environment for any of Texas Instruments first-generation TMS320C1x digital signal processors. The Development System consists of a Software Development System (SDS) and optional hardware modules including an EPROM Programmer Module and full in-circuit emulator (ICE) Modules. This system supports the Texas Instruments TMS320C14 DSP microcontroller, as well as the TMS320C10, TMS320C15, TMS320C17, and their EPROM equivalents.

  The features of the Development System include:

  Software Development System (SDS)

  - Window-based monitor/debuffer software includes single-step, breakpoint, and file I/O.
  - Simulation of all members of TMS320C1x family.
  - LSI TMS320C1x Absolute Assembler and a text editor.
  - IBM-PC/XT/AT or true compatible plug-in board.

  Optional Hardware Modules

  - EPROM Programmer Module for the TMS320E14, TMS320E15, and TMS320E17 processors.
  - Full-featured in-curcuit emulator/trace (ICE) modules.

  The EPROM Programmer Module is designed for fast prototyping and algorithm proving in stand-alone target systems. Users may program EPROM variants of the TMS320C1x processors by connecting the Programmer Module to the PC plug-in board via ribbon cable. The Module includes sockets for the TMS320E14 (68-pin) and TMS320E15 and TMS430E17 (40-pin). There is an on-board V_{PP} generator. The module is directly controlled from the SDS, and software is included for programming TMS320E1x devices.

  ICE Modules for each member of the TMS320C1x are available. By connecting different ICE Modules to the PC plug-in board, the TMS320C1x Development System can be configured to emulate any of the TMS320C1x processors. Target connectors are provided for DIP or PLCC package options to give a true physical representation of the device on the hardware application. The full-speed ICE is compatible with all the SDS software and hardware described.

Each ICE Module has an 8K-byte by 64-trace RAM buffer to capture valuable hardware debug information from internal registers, busses, I/O pins/ and control signals independent of program execution. A real benefit to designers of realtime systems is the ICE module's ability to continue program execution after the trace capture is halted. The trace capture can be later displayed.

- TMS320C25 System Board

The TMS320C25 System Board is an IBM PC plug-in board based on the TMS320C25 single-chip digital signal processor. With software from Spectrum and Texas Instruments, the board provides a complete DSP development environment for a PC-based workstation.

Features of the board are:

- TMS320C25 16-bit 100-ns processor
- DSP LINK System Expansion Interface
- 128K-words of on-board memory capacity
- High-speed 16-bit A/D and D/A with sample-and-hold
- Global memory capability via DSP LINK
- 5M-bps full-duplex serial I/O
- Complete debug monitor
- 'C' board drivers

The system runs at full speed (100-ns instruction cycle) and comes with 16K-words of 35-ns static RAM for zero wait-state operation. Occupying only eight I/O locations in the PC's address space (relocatable to eight places), users may configure up to eight boards in one PC. There are on-board address counters for efficient block transfer operations. The PC has direct access to all external RAM, and can read and write programs while the processor is running.

In addition to the on-board analog interfaces, data can also be acquired via the DSP LINK system expansion interface. This 50-pin standardized expansion bus is featured on most Spectrum products including multichannel data acquisition boards, providing users with the flexibility of tailoring a system to match their analog I/O requirements.

A complete debug monitor is provided for software development and debugging. An optional monitor features include single-step, breakpoint, disassembly, program loading, data upload/download, register inspection/modification, and full speed operation. Sample programs familiarize the user with program development and give good examples of how the system can be used in the PC environment. These sample programs include a 128-point FFT, a realtime FIR filter, and a data logger. Source code for these programs is included as part of the system documentation.

A library of 'C' board drivers for the PC is provided which can be easily integrated into the user's own PC interface code using standard 'C' calling conventions.

Spectrum provides a simular board without analog I/O, the TMS320C25 Processor Board

- DSP LINK Peripherals

  Spectrum's DSP LINK peripherals are compatible with the DSP LINK system expansion interface and be connected to any DSP system or processor board. DSP LINK specifications are available for custom interfacing.

  Following are brief descriptions of Spectrum DSP LINK peripherals:

  - **4-Channel Analog I/O Board** - Four 12-bit input channels (58-KHz/channel) with quad synchronous sample-and-hold, two 12-bit output channels, third order low-pass resistor programmed filters on input and output, DSP LINK data transfer interface.
  - **32-Channel Analog Input Board** - 32 12-bit input channels (7-KHz/channel) with 4-channel synchronous sample-and-hold, 32 first order low-pass resistor programmed input filters, 32 input buffer amplifiers, DSP LINK data transfer interface.
  - Pro-Audio Board - AES/EBU interface, 48-,44.1-,32-KHz clock, word sync, DSP LINK data transfer interface.
  - Pro-Audio Board (with SONY PCM and MIDI Interface) - AES/EBU interface, SONY PCM interface, MIDI interface, 16x16 cascadable RAM, 48-/44.1-/32-KHz clock, word sync, DSP LINK data transfer interface.
  - DSP LINK Prototype Module - DSP LINK slave wire-wrap interface for easy design of custom peripherals, buffered data, decoded address,R/W strobes.
  - DSP LINK Dual-Processor Communications Module - Allows two processors to communicate via DSP LINK.

Note:

Spectrum Signal Processing, Inc. holds the exclusive North American rights for the distribution of Loughborough Sound Images (see separate listing in this section) TMS320 development systems. For ordering information in North America, contact Spectrum Signal Processing, Inc.

9.3.53 Structured Electronic Systems Inc

Nature of Product(s): Algorithm Development Hardware
Functional System(s): Stand-alone
Device(s) Supported: TMS320E14

- SES-320E14EVAL Prototyping and Controller Evaluation Board

  The SES-320E14EVAL is a low-cost, single-board computer designed for prototyping and the evaluation of high-speed digital controllers. Based on the Texas Instruments TMS320E14 microcontroller, this versatile board can operate at clock frequencies up to 24-MHz. Physically, the SES-320E14EVAL measures approximately 5.5 by 7.5 inches, and is interfaced to a serial terminal through a RS-232 port.

  Features of the SES-320E14EVAL include:

  - Processor: TMS320E14.
  - Memory: 8K-bytes of on-board EPROM, 16K-bytes of zero-wait-state RAM with Bank Switching Logic (two banks of 4K-words x 16).
  - Counter/Timers: Up to six compare outputs or four capture inputs.
  - Parallel I/O: 16 individually configured I/O pins.
  - Serial Port: One RS-232 compatible port (IBM compatible DB-9).
  - A/D Converter: AD7821 A/D with ADG506A 16 channel multiplexer 16 channels, 660 nanosecond/conversion. :Off-Board I/O: 16-bit data bus with six decoded addresses. 16-bit parallel I/O bus. 16 analog input channels with 8 bit resolution. Programming interface for on-board TMS320E14 EPROM.

9.3.54 Symmetric Research

Nature of Product(s): Assembler, Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- TMS32020 Coprocessor Board and ASM20 Assembler

  The board and assembler form a completely integrated development environment for the TMS32020 using the IBM PC/XT/AT and compatibles. The TMS32020 Coprocessor Board provides users with hardware development and debugging capabilities. A monitor/debugger, a utilities library, and a number of applications programs are included. The Coprocessor Board comes with on-board memory ranging from 3K- to 256K-bytes. The ASM20 Assembler for the TMS32020 supports a complete set of assembler directives.

- TMS320C25 Coprocessor Board and ASM25 Assembler

  The coprocessor board and assembler form a completely integrated development and debugging environment fot the TMS320C25 using the IBM PC and compatibles. A monitor/debugger, utilities environment, and many applications programs are included with the coprocessor board. Circuit diagrams are also included for I/O bus and serial port customization. Typical benchmarks for the board include 5-second fractal and 30-millisecond 1024-point FFT. The coprocessor comes with onboard memory ranging from 32K- to 256K-bytes.

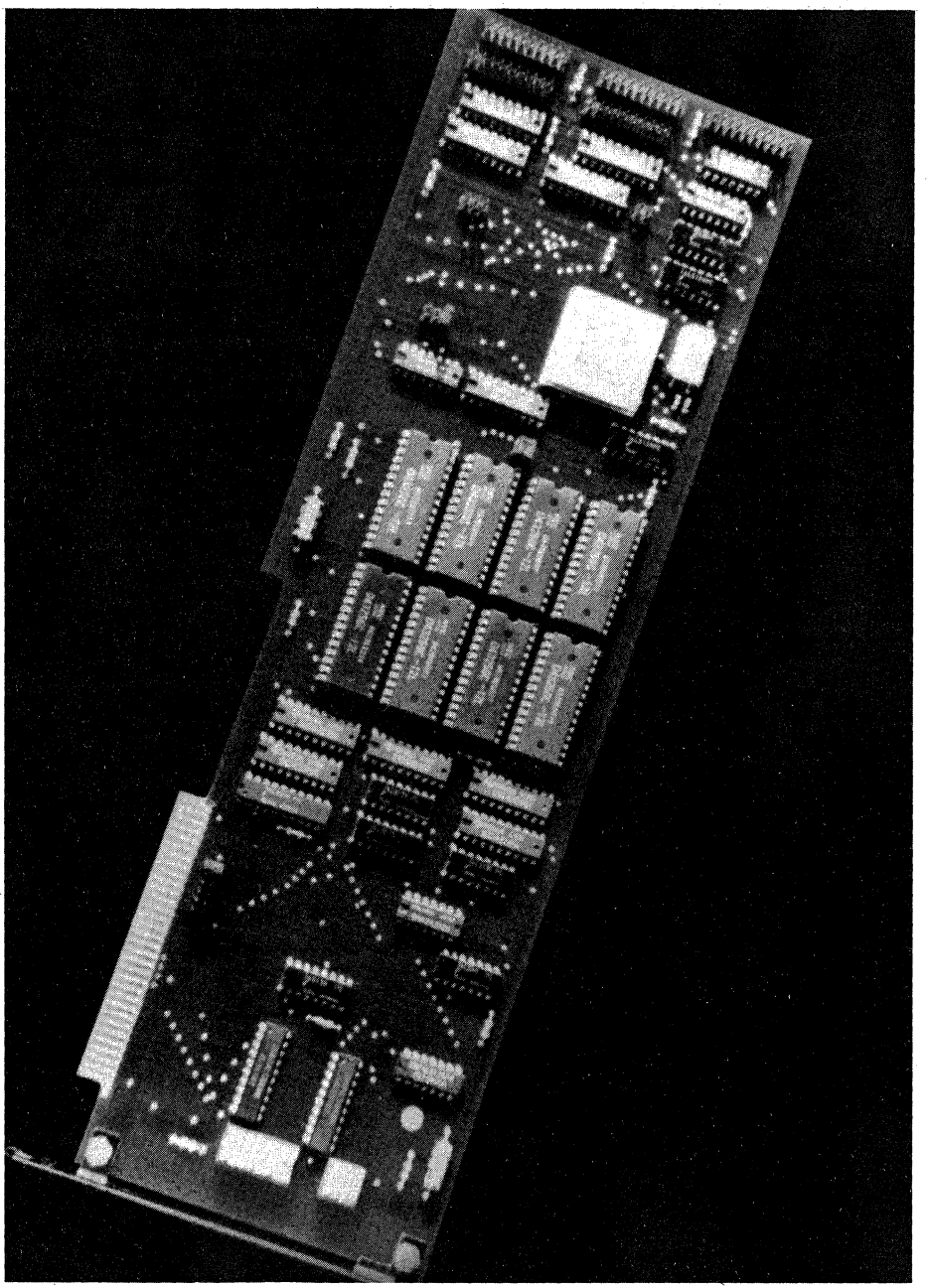

Figure 9-16. TMS320C25 Coprocessor Board and ASM25 Assembler from Symmetric Research

9.3.55 Tartan Laboratories, Inc

Nature of Product(s): High Level Language Compiler
Functional System(s): VAX (VMS)
Device(s) Supported: SMJ320C30

- ADA Compiler for the SMJ320C30

  Texas Instruments and Tartan Laboratories jointly developed an ADA compiler for the TMS320 DSP chip. The target processor for the compiler is TI's SMJ320C30, a third-generation DSP developed for military applications requiring advanced signal processing capabilities such as RADAR, SONAR, image processing, missile guidance and tracking, and communications. Completion of the compiler is expected in late-1989.

  The compiler, to be hosted on a Digital Equipment Corporation VAX (VMS) system, will implement ADA as defined in ANSI/MIL-STD-1815A-1983.

9.3.56 Teknic Inc.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): N/A
Device(s) Supported: TMS320C14

- TMS320C14 Evaluation Board/Servo Controller System

  The Teknic Evaluation System allows the user to develop motion control systems based on the TMS320C14 DSP quickly and easily. Reconfiguring the board for many different applications is simple and completely programmable.

  On-board power drivers, I/O, and signal conditioning eliminate any need for external fabrications, allowing the application to be prototyped immediately. This speeds development and frees the engineer to work on the control software. Software configurability minimizes DIP-switches and jumpers. This ensures the compatability of any application program with any evaluation board.

  Features of the TMS320C14 Evaluation Board/Servo Controller are:

  - Includes monitor/downloader
  - 8K-byte program memory
  - TMS320C14 may be evaluated without I/O logic, servoamps, or A/D if so desired
  - RS-232 connector included

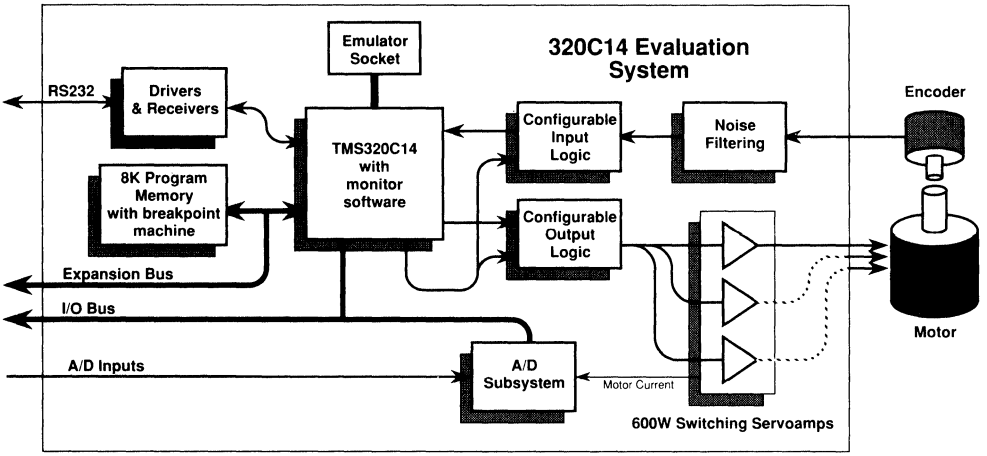

Figure 9-17. TMS320C14 Evaluation Board/Servo Controller System from Teknic Inc.

9.3.57 Tektronix

Nature of Product(s): Algorithm Development Hardware
Functional System(s): 1240/1241 Logic Analyzer
Device(s) Supported: TMS32010, TMS32020, TMS320C25

Tektronix supports TMS320 development on their 1240/1241 Logic Analyzer. The 1240/1241 Logic Analyzer provides complete state and timing analysis support for hardware, software, and integration applications. It is ideal for the testing and debugging of algorithms on TMS320 hardware. Powerful triggering, dual timebase, and mnemonic disassembly make the 1240/1241 a valuable tool for developing processor-based products.

- 12RM99 TMS320 Mnemonic Disassembly ROMPACK

  The 12RM99 TMS320 Mnemonic Disassembly support enables a Tektronix 1240/1241 Logic Analyzer equipped with 54 channels to capture and display TMS32010, TMS32020, and TMS320C25 DSP bus cycles. Disassembly is provided in absolute, hardware, and software formats.

- 12R01 Performance Analysis ROMPACK

  The 12R01 offers the software designer the ability to finetune a TMS32010, TMS32020, or TMS320C25 algorithm. The 12R01's histogram display eliminates the guesswork involved in diagnosing software inefficiencies by enabling the 1240/1241 to capture and display TMS320 bus cycles.

9.3.58 TelePhoto Communications

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32020

- TMS32020 Development System

  TelePhoto Communications' TMS32020 Development System is ideal for applications such as image processing (compression, overlay, merge, enhancement, and recognition), speech processing (pitch detection and phoneme recognition), natural language processing, and scientific and artificial intelligence research. The system consists of a single full-size board and the software required for loading, running, and debugging TMS32020 application programs. A powerful debugger offers the capabilities of a software simulator in hardware for realtime program execution.

  The development system, based on the TMS32020, offers 16K-bytes of high-speed (50-ns) RAM, expandable to 128K-bytes (64K-words of data memory). It also offers operation with no wait states. The TMS32020 RAM can be mapped into a 64K-byte address space in the IBM PC and accessed directly by the PC for program and data load. Data can be transferred to and from the TMS32020 RAM via an IBM PC DMA channel. An on-board selectable clock allows operation at 14 MHz and 20 MHz (other speeds attainable with a user-supplied crystal). A large prototyping area is available on the board for custom circuit development.

  The system supports the TMS32020 assembler/linker and object code, and includes a TMS32020 object code loader and executor. An optional debugger with single-step, breakpoint/trace, assembly/disassembly, and memory/ register dump capability is available. Color image compression software for the development system is also available.

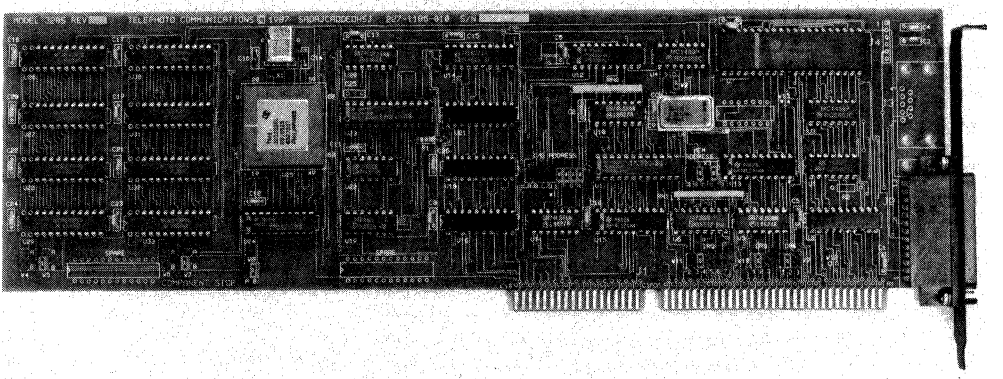

Figure 9-18. TMS32020 Development System from TelePhoto Communications

- ALICE Image Compression/Expansion System

  The ALICE system has been developed for the compression of high-resolution digitized images for picture database storage or transmission over standard telephone lines. The hardware/software package runs on the IBM-PC/XT/AT and compatibles and is based on the TMS32020.

9.3.59 Texas Instruments, Inc.

Nature of Product(s): Application Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- TI-Speech

  The Texas Instruments speech development system, TI-Speech, is an advanced voice interface and communications package that provides a base for sophisticated voice and data integration. The piggybacked, two-board speech processing system is built around the TMS32010, occupies one of the PC's expandable slots, and provides a combination of communications functions never before offered to a PC user. These functions include:

  - Speaker-dependent speech recognition
  - Voice store-and-forward at 2.4/9.6/16/32-kbps data rates
  - Text-to-speech
  - Speaker verification
  - Integrated telephone functions
  - Pulse or tone dialing
  - Dual-tone multifrequency decoding (DTMF)
  - Selection of communications channels.

  By combining these functions with the proper software, voice commands can be given to any application, thereby providing an intelligent telephone, a sophisticated telephone answering machine, or more.

  TI-Speech has three major components: system hardware, system software, and transparent keyboard software. These components work together to combine the functions described above into useful tools. In addition, TI offers a speech design kit to software developers for designing additional applications around the hardware component.

9.3.60 TIAC Systems, Inc.

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS32020, TMS320C25

- PC-320 Digital Signal Coprocessor

  The PC-320 is a complete digital signal processing mainframe that is capable of performing a wide variety of realtime digital signal processing tasks. Utilizing the TMS32010 technology, the system can be tailored to specific applications. The coprocessor nature of the PC-320 design allows the desired signal processing to be run in parallel with other PC applications. In some applications, the PC may act as a user interface that monitors the selection of processing tasks for the PC-320, the display of results, and the storage and retrieval of data. In other applications, once a task is loaded from the PC host onto the PC-320, the signal processing runs concurrently with the host machine.

- PC-325 Digital Signal Coprocessing System

  The PC-325 is a powerful general-purpose DSP system which plugs into an IBM PC or AT host. Utilizing the TMS32020 or TMS320C25 single-chip digital signal processor executing at up to 10-MIPS, the PC-325 is capable of performing a wide variety of realtime DSP tasks. The PC-325 was designed to provide users with a flexible, digital signal processing mainframe capable of satisfying a diverse range of DSP requirements. Expanded analog I/O, external global memory banks, and specialized communication interfaces are available on APC or IPC expansion boards which plug into the PC-325's expansion connector.

  Features of the PC-325 include:

  - TMS32020 or TMS320C25 versions.
  - User selectable 8-bit PC or 16-bit AT host interface.
  - 64K-word dual-port RAM, simultaneously accessible by the host and TMS320C25, with a fixed TMS320C25 access time.
  - 64K-word high-speed TMS320C25 RAM with zero wait-state accesses.
  - Dynamically mappable memory space allowing the user to define the base address and memory types (program or data) of the two 32K-word dual-port banks and two 32K-word high-speed memory banks.
  - On-board 8254 interval timer chip with three counter/timers.
  - On-board analog interface chip with 16-bit 19.2-KHz A/D and D/A converters.
  - Flexible, hardware-configurable interrupt, polling, and interval timer structure.
  - APC and IPC expansion ports containing TMS320C25 address, parallel and serial data, and control busses.
  - Inter-PC-325 communication port allowing for multiple PC-325 parallel processing.

- IPC-102 Data Acquisition Daughter Board

  The IPC-102, designed as a daughter board to plug into the PC-320. Features include:

  - Two analog input channels configurable to accept +/- volt bipolar, or 0 to 10 volts unipolar signals.
  - Two analog output channels configurable for similar bipolar and unipolar outputs.
  - A 16-bit digital input port and a 16-bit digital output port.

  Analog input signal conditioning options include plug-in filter modules and user-selectable/adjustable gain. Analog signals are converted via a 200-Ksample per second 12-bit A/D converter, which is connected directly or alternately to either input channel under user software control.

- SAB-320 Signal Analysis BIOS Software

  The signal analysis basic input/output system (SABIOS) is designed to simplify the creation of realtime signal analysis applications. The SABIOS is a set of driver calls that perform a complete set of signal processing functions. These functions vary from simple data movement operations, such as moving a block of sample data between the PC-320 and the host PC, to complex signal processing functions such as the FFT. SAB functions are invoked using software interrupts, thus providing simple interface compatibility for several application languages. Function classes contained in the package include correlation analysis, waveform generation, spectrum analysis, parameter array data management, and waveform display.

9.3.61 Valid Logic Systems

Nature of Product(s): Simulator
Functional System(s): Sun-3, Sun-4, and VAX
Device(s) Supported: TMS320 Family

- Realchip Hardware Modelling System

  The Realchip hardware modelling system accommodates VLSI devices with up to 128 active signals, such as the TMS320 family of digital signal processors. Included in its key features are:

  - Programmable clock rates up to 4 million clock edges per second.
  - Maximum capacity of 4096 bidirectional signal channels.
  - Simulations of 32 thousand clock edges (typical) for dynamic devices.
  - Networked resource for simultaneous access by multiple simulations.

- Realchip II Hardware Modelling System

  Realchip II is a second generation modelling system and accomodates VLSI devices with up to 256 active signals, such as the TMS320 DSP family. Printed circuit boards are also supported. Included in Realchip IIs key features are:

  - Programmable clock rates up to 16 million clock edges per second.
  - Maximum capacity of 1536 bidirectional signal channels.
  - Simulations of 2 million clock edges (typical) for dynamic devices.
  - Networked resource for simultaneous access by multiple simulations.

- Realfast Simulator Accelerator System

  The features of the simulator accelerator system, designed for use with Realchip include:

  - Up to 500,000 events/second simulation speed (equivalent to 1.25-million evaluations/second).
  - 1 million (2-input) primitives maximum capacity.
  - Transparent operation within Valids' simulation environment.

- Realmodel Simulation System

  Realmodel is a unique product that combines advanced hardware modelling and simulation acceleration in a single high performance unit. Direct communication between the accelerator and the hardware modeler allows Realmodel to provide unmatched performance in simulation of systems containing switch, gate, functional, behavioral, and hardware models. Included in it's key features are:

  - Programmable clock rates up to 16 million clock edges per second.
  - Maximum capacity of 1536 bidirectional signal channels.
  - Simulations of two million clock edges (typical) for dynamic devices.

- Up to 0.5M events/second simulation speed (1.25M evaluations/second)
- One million (2-input) primitives maximum capacity.
- Transparent operation within Valids' simulation environment.

9.3.62 Votan

Nature of Product(s): Application hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- VPC2100 Voice Board

  The VPC2100 Voice Board from Votan is a hardware and software system, based on the TMS32010. The voice board, featuring continuous speech recognition, enables the user to speak in a natural conversational flow rather than pausing between each word as required in most recognition systems.

  The VPC2100 consists of a printed circuit board, microphone, speaker, software, and documentation. It is designed to add voice I/O and telephone management capabilities to the IBM PC and compatibles. The voice board has the following capabilities:

  - Voice store-and-forward at 4 kbps to 16.4 bps (software selectable) data rates.
  - Speaker-independent speech recognition (0-9, YES, NO).
  - Continuous speaker-dependent speech recognition.
  - Integrated telephone functions, such as telephone interface, pulse or tone dialing, call progress, and DTMF. encoding/decoding.
  - Software for development, voice mail, telephone management, and VoiceKey.
  - High level applications generator software.

9.3.63 Whitman Engineering, Inc.

Nature of Product(s): Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32010, TMS32020

- Product Development System

  Whitman Engineering provides a PC-based product development system for both the TMS32010 and TMS32020. The basic software includes the MADCAP package, plus five preprogrammed links to the TMS32010 or TMS32020 assembler/linker/simulator software, ASPI's digital filter design package, and a standard MS-DOS text editor. A main menu selection is also labeled for linking in the software driver for the user's data acquisition hardware. Three user-defined module links allow interface of additional hardware and software. The TI-Speech board has been interfaced as one of these modules to allow the designer to download TMS32010 code and data to a plug-in peripheral. The option also provides the software for developing and interfacing an end product such as a TI-Speech board.

- MADCAP DSP Workstation

  The MADCAP software system is useful as a design station and for product development from design through production quality control. The system also serves as a basic signal processing workstation with the following main features:

  - Signal and special function generation
  - 32-bit floating-point FFT routines for forward and inverse transforms on real or complex data
  - Standard power-of-two and mixed-radix FFT algorithm with 94 extra transform lengths
  - High-resolution graphics, stripchart and numerical display options
  - Fully-automated filing for 3200 files and the ability to transfer files from outside sources.

  Using the mixed-radix FFT algorithm when developing TMS320 designs allows accurate measurement of the frequency response and quantization characteristics of the TMS320 code. Mixed-radix FFT filters can be placed in seven times as many locations as standard FFTs.

  The internal synthesizer, keyboard entry, external source, and FFT/IFFT selections from the main menu allow test sequences to be developed and test results to be analyzed and displayed for:

  - Software simulation
  - TMS32010 and TMS32020 code simulation
  - Code run on the TI-Speech board's TMS32010 chip
  - Code run on dedicated prototype hardware
  - Code run on production hardware.

Far East

9.3.64 Advanced Digital System Industries, Ltd.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32010

- ADS-2

  The ADS-2, an inexpensive IBM-PC board, can accelerate the PC for signal processing computations by almost 100 times. The ADS-2 allows a system to accept, process, and deliver analog signals, and contains a TMS32010 DSP, 4K words of program memory space, and almost 16K words of data memory space. A program disk containing various numeric subroutines, such as FFT algorithms, is included.

9.3.65 ASR International

Nature of Product(s): Assembler, High Level Language Compiler, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC, PDP-11 Q-bus, VMEbus, Sun-3, MicroVAX
Device(s) Supported: TMS32010, TMS32020

Note: ASR International is the Far East agent for Sky Computers (see separate listing in this section). Refer to Sky Computer's listing for a complete description of available products.

9.3.66 Burr-Brown Japan

Nature of Product(s): Algorithm Development Hardware
Functional System(s): VMEbus, SUN-3/SUN-4 Workstations
Device(s) Supported: TMS32010, TMS32020, TMS320C25

> **Note:**
>
> Burr-Brown Japan is the far eastern distributor for all Burr-Brown products. Refer to Burr-Brown's listing in the North America portion of this section for a complete description of their offerings.

9.3.67 CGA Corporation

Nature of Product(s): High Level Language Compiler, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): NEC PC-9801
Device(s) Supported: TMS32020, TMS320C25

- DSP-TURBO System

  The DSP-TURBO system consists of software and hardware. Some features of the software are:

  - Stand-alone development environment on the NEC-9801
  - Provides the C compiler made by CGA Corporation
  - Provides the C language's function-calls which make use of the micro-code program of the TMS320C25
  - Multiple memory handling between the host and the DSP board.

  There are three units of hardware for the DSP-TURBO: two units that contain the TMS320C25 and an optional memory board.

  The two TMS320C25 units are:

  - DSP-TURBO I Board - This is a plug-in board for the NEC PC-9801.
  - DSP-TURBO II - This is a box containing the power supply required if the added memory board is needed. It is connected as an external device to the NEC PC-9801.

  The optional memory board contains 64K-bytes of high-speed RAM. It plugs into the DSP-TURBO II.

9.3.68 Chubu Denki Corporation

Nature of Product(s): Algorithm Development Hardware, Algorithm Development Software
Functional System(s): NEC PC-9801
Device(s) Supported: TMS32010, TMS320C25

- DSP320 Board and Utility Software

  The DSP320 plug-in board and utility software for the NEC PC-9801 supports digital signal analysis with FFT/IFFT and Digital Filtering algorithms. Features of the software are:

  - Real FFT - 128 to 1024 points
  - Complex FFT - 128 to 1024 points
  - Windowing
  - Digital filtering
  - Inverse FFT with spectrum

- DSP320 Board using the TMS320C25

  This board offers all the features specified above, using the TMS320C25 in place of the TMS32010.

- DSP320AR Board and Utility Software

  The DSP-320AR plug-in board and utility software for the NEC PC-9801 supports spectral analysis with the FFT method and the Linear Predictive method. Some major functions of the software are:

  - 3-D spectral display with PCM data array or PARCOR coefficients.
  - Analyzed AR-model and display poles on an S-plane.

9.3.69 Emona Enterprises Pty Ltd.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): N/A
Device(s) Supported: TMS32010

- Telecommunications Instructional Modelling System (TIMS)

  TIMS is a laboratory teaching system used in technical schools and universities by students in both introductory and advanced telecommunications engineering courses. It is based on a highly successful university teaching system and has been designed in conjunction with telecommunications lecturers.

  TIMS is unique in that the teaching system allows any analog or digital modulation or coding technique to be modelled on the one system. TIMS is able to model such communications systems through its range of fundamental building blocks or modules. These modules are composed of basic electronic circuits on Eurocard boards which correspond to fundamental mathematical operations (adders, multipliers, etc.) and electrical functions (oscillators, filters, amplifiers, etc.). As a result of this modularity, the TIMS system is extremely flexible. Experiments can be selected to suit the objectives of each individual course.

  TIMS is ideal for teaching students the fundamental principles of telecommunications because the actual theories and equations are implemented in experiments. A benefit of the TIMS system is its fully self-contained design. The only other piece of equipment required is an oscilloscope. DSP modules are also incorporated which are specifically designed for the teaching environment. These modules allow DSP implementations to be demonstrated alongside traditional discrete telecommunications techniques. Prewritten programs illustrate the application of this technology in introductory lab courses. In advanced coursework, the student gains practical experience by actually developing and testing programs.

  The TIMS DSP processor modules utilize the TMS32010, running at 20 MHz, with high speed EPROM and RAM. An onboard microcomputer provides all program up and down load facilities via a serial link to the host computer. A monitor program facilitates data and I/O port manipulation . The Analog Interface Module provides high speed A/D (12 bits 5 µs) and D/A converters, plus digital I/O and other user interfaces.

9.3.70 MTT Corporation

Nature of Product(s): Assembler, Simulator, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): NEC PC-9801, NEC/IBM PC, VME-bus
Device(s) Supported: TMS320C25

- DSP1025 DSP Development Board

  The DSP1025 is a plug-in board for the NEC/IBM PC. It uses the TMS320C25 DSP. This is a hardware-only product that has the following features:

  - 2K-bytes of multiple two-port memory
  - 32K-words of data memory
  - 32K-words of no-wait high-speed memory

  A typical speed of execution for this product is 17.2-mS for a 1024 point complex FFT.

- MVME560C25 DSP Board

  The MVME560C25 is a DSP board for the VME-bus. It uses the TMS320C25 DSP. It is a hardware-only product designed for high-speed applications, such as speech and image processing, digital filtering, spectral analysis, data communications, and realtime controls.

- Software Development Tool Support

  MTT offers software development tool support for the NEC PC-9801, the IBM PC/AT, and the NEC/IBM PC. These tools include assembler, linker, simulator, and debugger.

9.3.71 System Engineering Corporation

Nature of Product(s): Algorithm Development Hardware
Functional System(s): NEC PC-9801
Device(s) Supported: TMS320C25

- TMC320C25 DSP Development Board

  The TMC320C25 is a plug-in DSP development board for the NEC PC-9801. It uses the TMS320C25 DSP. Board specifications include:

  - 64K-word program memory
  - 64K-word data memory with 4K-word dual-port memory
  - 14 channel I/O

Europe

9.3.72 Computer Solutions Ltd.

Nature of Product(s): High Level Language Compiler, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- polyFORTH DSP System

  The polyFORTH DSP System for the IBM PC contains the TMS32020 or TMS320C25 and is controlled by the FORTH language system. The speed of the DSP combined with the flexibility of the FORTH language makes this an ideal environment for developing signal processing applications. The polyFORTH DSP System includes a resident assembler, 16/32-bit fixed-point arithemetic (including trigonometric and logarithmic functions), multitasking with multi-terminal operation via the PC, and interrupt support. An example program is included with the package which demonstrates a data acquisition system in which the DSP board performs an FFT while the PC maintains a graphic display of the result.

- COMSOL DSP System

  COMSOL DSP System is a high-level programming environment for the TMS320C25. This DSP system combines the polyFORTH programming language with a TMS320C25 Loughborough Sound Images board interface (for IBM-PC). The system is intended for target hardware development as well as desktop signal processing. Included software allows the PC to access disk and graphics facilities while the TMS320C25 accesses I/O and processes the next data block or element.

  The polyFORTH compiler is a special high-speed implementation of the FORTH high-level programming language specifically developed for realtime control and instrumentation. It is characterized by fast execution and direct compilation of source code to executable code (without intermediate steps for linking and download).

  The COMSOL DSP System includes resident assembler/disassembler, trace/breakpoint buffer, fixed and floating point support, multitasking and interrupt support, plus DSP extensions for FFTs and waveform generation.

9.3.73 dSPACE GmbH

Nature of Product(s): Application Hardware, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM PC
Device(s) Supported: TMS320C1x, TMS320C2x

- DSP-CITpro Development Software

  The DSP-CITpro software is an advanced high-level development and programming tool for the implementation of high-speed multivariable controllers on the IBM PC/AT. While the development part is general for any target hardware, the programming part is tailored to automatically generate high-efficiency code for the TMS320 family DSP. The DSP-CITpro concentrates on linear, multivariable control systems, described in terms of subsystems. Every piece of information about the controller (sampling time, sampling delays, A/D-D/A and internal signal ranges, description of arithmetic) is incorporated. Multirate and nonlinear controller structures will be incorporated in a later version of this product.

  A choice of different digitization methods and analysis tools is provided to digitialize analog controller outputs with the highest degree of accuracy. The ability to select different controller structures is provided to decrease the number of controller coefficients, and the sensitivity of controller coefficients with respect to quanitization and internal signal quanitization. Automatic scaling fits the internal controller states, intermediate results, and controller coefficients into a desired value range.

  The effects of asynchronous sampling of controller I/O delays, as well as computational delays, can be examined for the open-loop and closed-loop system. This analysis tool may be used to analyze the stability of a closed loop system with known controller delays, but can also be used, for example, for finding the specification of the least expensive (slowest) I/O that will meet predetermined stability requirements.

  The DSP-CITpro provides a simulation tool that permits the closed-loop simulation of the analog circuit model with the discrete controller (including all delays, A/D-D/A and processor quanitization, overflow, sampling, and computational delays) before actual building of the circuit. All necessary data for the controller simulation is derived from the controller description.

- DSP-CITpro Programming Software

  After development is complete, the DSP-CITpro Programming Software provides task-specific automatic highly-efficient code generation which supports the TMS320C1x and TMS320C2x. The automatic code generation takes place in two steps: first, an intermediate DSP language representation is derived, and then this representation is compiled to ASM source.

  A high-level language **DSPL** is tailored to control and filtering applications with DSP. In addition to the normal set of control statement and expressions found in a high-level language, DSPL allows easy programming of multirate controllers and I/O communication. Language constructs for fractional arithmetic, scalar product computation with au-

tomatic scaling, overflow-handling, and optimal utilization of DSP storage and speed are very important features of DSPL for programming fixed-point DSP. After automatic code generation of linear controller subsystems in DSPL, multirate and nonlinear controller parts can be added in DSPL before ASM source is generated. A mechanism to include hand-programmed ASM or ASM produced by other high-level language compilers is also available.

- DSP-CITpro DS1001 Processor

  The DS1001 processor is a high-performance non-compromise PC-AT compatible board (check with dSpace regarding PC/XT compatibility) based on the TMS320C25 DSP.

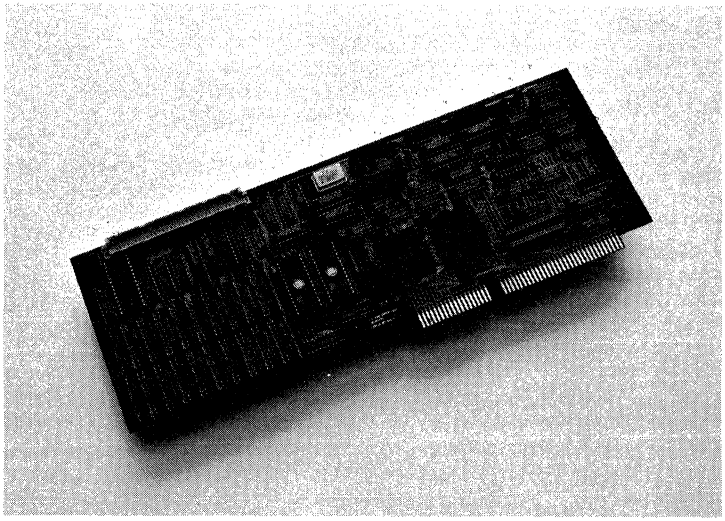

Figure 9-19. DSP-CITpro DS1001 Processor from dSPACE GmbH

Key features of the DS1001 are:

- No wait-states at 40-MHz - There is only one exception, when the host computer and DSP want to access the same dual-port memory word at the same time. When this happens, the host computer will go first.
- True dual-port RAM to host computer - 4K-words (16-bit) of data memory are accessible by both the DSP and host computer simultaneously. Only simultaneous access to the same memory word

may lead to wait-states for the DSP. Other boards frequently have simple dual-port RAMS which lead to several wait states at every host computer access.

- 16K-words of program RAM and 20K-words of data RAM in the basic version - It is possible, as an option, to upgrade up to 64K-words. All RAM is mapped into host computer space. There is automatic handling of host access and 16-bit transfers.
- 2K-words EPROM option - Sockets for zero-wait EPROMS are provided.
- No setup hardware jumpers - Complete setup control by host computer and DSP software.
- Watchdog - A watchdog recognizes power failure, peripheral failure (via I/O bus), and failure of the DSP to reset the watchdog timer. Watchdog action can be selected to be either (1) DSP reset and restart (*soft failures*) or (2) Reset of DSP and peripherals without restart (*hard failures*). Power failure is always considered a *hard failure*.
- Slow timer - The watchdog timer can be used as a large period timer (larger than the DSP's own timer).
- Diagnostic mode - In this mode, the host computer has access to everything to which the DSP has access: peripherals, interrupt-controller, etc..
- Autovector interrupt - A fast interrupt-controller overcomes the limitations of the DSP. There are eight interrupt channels available on-board. Peripheral boards can increase the number of autovectored interrupt channels to 64 by cascading. Typical interrupt latency is one microsecond.
- DSP may interrupt host computer and vice versa
- Memory-mapped I/O - Up to 256 I/O devices can be addressed.
- 32-bit full-speed I/O bus design - Allows for later replacement of the processor board by the TMS320C30 32-bit processor without the necessity of also replacing the I/O systems.
- Host computer may run in protected mode - DSP memory space (program and data) can be mapped into any portion of the PC-AT memory space up to it's 16M-byte limit.

- DSP-CITpro DS1101 Controller Board

The single-board DS1101 is based on the TMS320C14 or TMS320E14 DSP chip. The chip is surrounded by a set of off-chip peripherals (ADC, DAC, decoder). The DS1101 allows implementation of nontrivial multivariable control systems at high sampling rates. It is PC and PC-AT compatible, but can also be used stand-alone as an Evaluation Module (EVM). It is ideal for, but not restricted to, one or two axis motion control. The basic version of the board has two analog input channels, one analog output channel, and one incremental encoder input. An option doubles these inputs by filling the on-board sockets.

A line of low cost software tools for the DS1101 will be derived from the dSPACE DSP-CITpro control implementation toolset for easy implementation of nontrivial controllers. The software part of DSP-CITpro will also support the DS1101.

- DSP-CITpro DS2001 High Resolution ADC Board

  The DS2001 is a PC-AT compatible board (check with dSpace regarding PC/XT compatibility) incorporating five separate ADC channels with selectable analog ranges.

  Key features of the DS2001 are:

  - No multiplexer - Each channel has it's own converter for maximum flexibility and minimum delay. Simultaneous sampling is possible as well as any arbitrary and nonconstant sequence.
  - 16-bit resolution with 12-bit linearity
  - Five microseconds conversion time
  - Sample-hold - Each sample-hold circuit can be held in *transparent mode* (no-hold, buffer-only) for minimum signal delay. In *track-hold mode*, maximum settling time to 12-bits is about 1.5 microseconds.
  - Independent start of conversion - End of conversion may be signalled to the processor by either interrupt or polled-status flag.
  - Two's complement output - Aligned for fractional number range.
  - No hardware setup jumpers - Setup control (sample-hold mode, analog input ranges, etc.) is completely by DSP or host computer software.
  - Host computer access - The host computer has access to converter data for monitoring functions even while the DSP is running. There are no DSP code changes required for this.

- DSP-CITpro DS2101 DAC Board

  The DS2101 is a PC-AT compatible (please inquire about PC/XT compatibility) that incorporates five separate DAC channels with selectable analog ranges.

  Key features of the DS2101 are:

  - 12-bit resolution
  - Three microseconds settling time
  - Independent output from DSP
  - No hardware setup jumpers - Complete setup control (mode, analog output ranges, reset) by DSP or host computer software.
  - Two's complement data - Independent output will usually be used for control, but simultaneous (zero phase shift) output may be desired for other purposes.
  - Host computer access - The host computer has access to converter data for monitoring functions even while the DSP is running. There areno DSP code changes necessary for this.
  - Automatic DAC reset to zero in error situations - With respect to DSP, I/O or power failure.

- DSP-CITpro DS3001 Incremental Encoder Interface Board

  The DS3001 is a PC-AT compatible board (check with dSpace regarding PC/XT compatibility) incorporating six separate incremental position encoder channels.

  The key features of the DS3001 are:

  - 32-bit counters - A 32-bit processor may read the whole counter value in a single I/O operation. A 16-bit processor in two operations.
  - Pulse multiplication - The direction sensing logic performs fourfold pulse multiplication.
  - Index pulse input - Sets flag which may be polled by the host computer and DSP. In auto-reset mode, the user can select whether to have the index pulse reset the counter once or at each occurance. The user can also select the option of having a DSP interrupt generated by an index pulse.
  - Various counter reset modes - Reset may occur three ways: (1)DSP or computer host, (2) by index pulse once, (3) by index pulse always.
  - Regulated power supplies for encoders - Standard 5-V encoders drawing up to 200-mA each can be used without the need for an external power supply. Narrow tolerances of power supply voltage can be satisfied even over long cable through sense lines.
  - High noise immunity - Some encoders provide differential quadrature signals. Special logic makes use of this for improved common mode noise rejection.
  - Cable failure detection.
  - No hardware setup jumpers - Complete setup control by host computer and DSP software.
  - Host computer access - The host computer has access to converter data for monitoring functions even while the DSP is running. There are no DSP code changes required for this.
  - Two's complement data - Delivers fractional numbers as supported by the DSP.

Note:

EMU-SYS Inc. is the exclusive representative in North America for dSpace GmbH. For ordering information in North America, contact EMU-SYS Inc.

9.3.74 Joyce-Loebl Ltd.

Nature of Product(s): Application Hardware, High Level Language Compiler
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- Scientific and Industrial Applications

  Joyce-Loebl's IV/IAS vision boards provide state of the art image processing and analysis hardware which is plug compatible with PC XT/AT computers. Specific applications software can be developed using a comprehensive GENeral Image Analysis Library (GENIAL) of Microsoft Pascal/C callable routines. Information from a wide range of images can also be extracted automatically using the flexible image processing/analysis package GENIAS - GENeral Image Analysis Software. Data files containing object/feature measurements created by GENIAS may be analyzed numerically, statistically, and graphically using the data analysis program RESULTS.

  Component recognition applications are available using Robot Vision Control Software (RVCS), ranging from static parts (touching or overlapping) on pallets or in bins, to tracking and picking parts from a moving conveyor system. Systems have been configured for Bosch, Kuka, Unimation, and Cincinnati robots. Component measurement forms a major applications area for industrial machine vision inspection. Sub pixel measurement packages are available that can measure to within one tenth of a pixel.

  A large proportion of the imaging routines have been developed using Joyce-Loebl's own compiler, the JL320 Pascal Compiler. This compiler, which is available as an additional software package, generates code for the TMS32020 and TMS320C25 digital signal processors which are used in the products described above.

- Software

  Programmable I/O look up tables (IV/IAS25 only). Grey image operators (linear and nonlinear convolutions, image arithmetic, zooming, area of interest processing). Binary image operators (slicing, erosion, dilation, thinning, manual editing, logical operators AND, NOT, OR). Object detection (boundary and region tracing) and measurement (including area, length, breadth, center of gravity, integrated density, orientation, etc.). Statistical pattern recognition package for object identification and industrial inspection.

- IV20 and IAS20 Hardware

  - Two camera inputs - software selectable
  - Monochrome I/O
  - 256 x 256 x 8-bit frame stores
  - TMS32020 DSP technology
  - Realtime edge enhancement board (option on IAS20)
  - PC XT/AT plug compatible
  - Realtime binary image combined with gray input image

- IV25 and IAS25 Hardware
  - Three camera inputs - software selectable
  - Monochrome input, RGB color output
  - 256 x 8-bit I/O look up tables
  - 512 x 512 x 8-bit images with 256 gray levels
  - Three 512 x 512 x 8-bit frame stores
  - TMS320C25 DSP technology
  - Software selectable camera synchronization modes
  - Expansion port for special function boards
  - Automatic stage controller hardware option
  - PC AT plug compatible

9.3.75 Loughborough Sound Images Ltd.

Nature of Product(s): Assembler, Simulator, Algorithm Development Hardware, Algorithm Development Software, Emulator, EPROM Programmer, High Level Language Compiler
Functional System(s): IBM PC
Device(s) Supported: TMS320C1x, TMS320C2x

- TMS32020 Board

  The TMS32020 Board, designed as an IBM PC plug-in board, utilizes a bidirectional port to interface to the PC-bus, thus providing the ideal environment for speech, audio, and control applications. Turned-pin sockets are included so that 128 kilobytes of memory can be used as either program or data memory. In most situations, this will be populated with high-speed static RAM devices, allowing the processor to run without wait states. It is possible to replace the RAM with EPROM, thus allowing operation with one wait state. The memory is dual-ported to permit program loading, monitor access, and rapid interchange of large blocks of data.

  Sixteen-bit A/D and D/A converters are provided on the board, accessible via BNC sockets and supporting sampling rates up to 50 kHz. Clocking can be internal (crystal-controlled) or external. The serial input and output lines of the TMS32020 are brought to external connectors and arranged to facilitate the linking of two or more boards. An additional connector is provided to allow for global memory expansion and for full use of the 16 parallel input/output ports.

- TMS32020 Monitor Program

  Loughborough Sound Images provides a Monitor program for the TMS32020 Macro Assembler/Linker, which takes the output of the linker and loads it to the board. The Monitor program supports single-step, breakpoint, or full-speed operation. It permits the examination and changing of registers and memory using a variety of formats, and includes a disassembler. Also included in the package is software to convert the TMS32020 object code to Intel hexadecimal format for EPROM programming.

- LSI320/C1x Development System

  The LSI320/C1x Development System supports the TMS320C14/E14 DSP controllers featuring on-board peripherals of timers, capture pins, PWM outputs, USART, bit I/O, and watchdog. It also supports the previously released TMS32C10, TMS320C15/E15, and TMS320C17/E17.

  The LSI320C1x is composed of a macro assembler, a PC board for algorithm development and simulation, full featured in-circuit emulator/trace modules, target connectors, and a special module for programming the EPROM processors TMS320E14, TMS320E15, and TMS320E17.

The system's modular approach can satisfy a wide range of application and development objectives, from processor evaluation and software development/debugging to full speed emulation and trace capture in the target hardware. It is also possible to program an EPROM version of the TMS320C1x device from the same workstation to realize a final stand-alone solution.

A full-length PC board **Software Development Board (SDB)** provides the software development environment centered around a debug monitor from which the assembler and editor can be accessed for code generation. The user friendly monitor is screen based with windows displaying registers, data memory, and disassembled program memory. The user has full access to all processor resources. Debug facilities include breakpoint, single step, and I/O to PC files.

The **In Circuit Emulator (ICE)** modules use self emulation of the TMS320C1x device to extract the maximum 160-ns instruction cycle time performance. By connecting different ICE modules to the PC board, the LSI320/C1x can be configured to emulate any of the TMS320C1x processors. Target connectors are provided for DIP or PLCC package options to give a true physical representation of the device on the application hardware.

The ICE modules are further characterized by an 8K x 64 trace RAM buffer which captures valuable hardware debug information from internal registers, busses, I/O pins, and control signals independently of program execution. A distinctive feature of the ICE modules is the ability to continue program execution, when the trace capture has halted. This allows display afterwards, a real benefit to the designer of realtime systems.

The **EPROM Processor Programming** module allows the user to quickly program EPROM variants of the TMS320C1x processors by simply connecting the programming module to the PC board. This permits fast prototyping and proving of algorithms in stand-alone target systems. The programming module is directly controlled from the debug monitor.

- LSI C Compiler for the TMS320C25

  The LSI C compiler for the TMS320C25 is a full Kernighan and Ritchie implementation that provides complete high-level language capability. All code can be written in C for proof of concept, and later optimized in assembly language for speed-critical code. The compiler outputs TI-990 tagged format. A preprocessor and assembler/linker are included with the compiler.

Note:

Spectrum Signal Processing, Inc. (see separate listing in this section) holds the exclusive North American rights for the distribution of Loughborough Sound Images's TMS320 development systems. For ordering information in North America, contact Spectrum Signal Processing, Inc.

9.3.76 PC Electronics a.s.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): IBM PC
Device(s) Supported: TMS32020, TMS320C25

- Bugbust TMS32020 and TMS320C25 Development System

  Bugbust is ideal for realtime development of filters, FFTs, convolution, image processing, telecommunications and speech,as well as control applications. The Bugbust communicates with the host through shared memory. The host can also reset the board and interrupt a running TMS32020 or TMS320C25 program. The PC-board contains single-step and interrupt logic, and a fully buffered I/O backplane connector. One third of the board is laid out as a wire wrap area for application specific circuitry. All bus signals are made available at this area.

  Board memory consists of a total of 96K-words of RAM for program and data memory. Several Bugbust boards may be installed in a PC for increased signal processing performance. System software includes an assembler/ disassembler. The software can also accept object files generated by Texas Instruments TMS32020/C25 Cross Assembler and Link Editor. Debugging commands include breakpoints and single-stepping.

9.3.77 Pratica SRL

Nature of Product(s): Assembler, Algorithm Development Software
Functional System(s): Olivetti M20/21/24 PC, IBM PC, VAX (VMS), VAX (UNIX), PDP-11, RSX-11M/PLUS, ATT 3B2
Device(s) Supported: TMS32010

- PDS-20 Development System

  The PDS-20 universal microprocessor development system supports many 8- and 16-bit CPUs on systems compatible with the TMS32010 XDS Emulator. Emulation and programming of PROM memories is possible using external standalone systems. Software tools include a high-level editor, a cross assembler with nested macros, and symbols/arithmetic/logic expressions, a linker, and up/down loaders for emulators and PROM programmers.

9.3.78 Racal Microelectronics Systems Ltd.

Nature of Product(s): Algorithm Development Hardware
Functional System(s): VMEbus
Device(s) Supported: TMS32020

- RME320 DSP Board

  The RME320 from Racal Microelectronics Systems is a VME Rev C TMS32020-based board for digital signal processing applications. It has been designed to exploit the state-of-the-art features incorporated in the TMS32020 and is suitable for a wide range of DSP and arithmetic-intensive applications. The RME320 processor runs with a 200-ns instruction cycle.

  The board includes a 64-pin connector fitted to the front panel to provide direct access to all of the TMS32020 pins. This enables immediate connection of development systems or logic analyzers for development and diagnostics.

  Local interface is provided on the P2 connector for adding independent links into associated system components. The interface includes 16-bit data, 4-bit address, read/write, and handshake control lines, allowing up to 8 different operating modes. A data transfer rate of 2.5 Mwords/second is possible. In addition, the two TMS32020 serial lines are fully buffered to the P2 connector.

  The board is intended to be used as a secondary (slave) processor to which programs are downloaded from the master. However, a minimal system may consist of the RME320 board and an I/O board, with operation controlled by an on-board program resident in EPROM.

  The RME320 in basic form is equipped with 16K words of high-speed RAM (zero wait states). Upgrade kits are available to increase RAM size to 64K words. Sockets are provided for up to 8K words of program PROM.

9.3.79 Televic

Nature of Product(s): High Level Language Compiler, Algorithm Development Software
Functional System(s): VAX, IBM PC
Device(s) Supported: TMS32010, TMS32020

- DSPL 1010 Compiler

  Televic offers a compiler for DSPL, a high-level language for the TMS32010 and TMS32020. Some of the features of DSPL include:

  - All standard Pascal instructions
  - Most standard Pascal data types
  - Special constructs for signal processing, such as fast fractional arithmetic, shift operators, etc.
  - Internal and external data variables with initialization (tables)
  - Realtime facilities (interrupt procedures, implementation of regions)
  - Separate compilation units (including import and export of variables)

  The DSPL 1010 Compiler is written in Pascal and highly optimized for the TMS32010. It also provides a disassembler output facility.

- DSPL 1020 Linker

  The DSPL 1020 links DSPL and assembler modules (TI format), computes overlay for internal variables, and generates TI and Intel hexadecimal files.

- DSPL 1030 Library

  The DSPL 1030 Library provides the standard functions, such as sine, cosine, and floating-point routines.

> **Note:**
>
> Allante Corp is the U.S. representative for Televic. For ordering information in the U.S., contact Allante Corp.

9.3.80 Ultra Digital Systems Limited

Nature of Product(s): Assembler, Simulator, Algorithm Development Hardware, Algorithm Development Software
Functional System(s): IBM-PC, BBC, Macintosh
Device(s) Supported: TMS32010

- C3M TMS32010-Based DSP Development and Training System

  The C3M System, consisting of hardware, software (including cross-assembler, simulator, and monitor), and documentation is provided in both single- and dual-channel variants. It runs in conjunction with the IBM-PC and the BBC range of microcomputers.

  The C3M hardware, in a rugged case which also contains the C3M power supply, features 12 A/D and D/A converters, selectable filters on input and output, 16-bit digital I/O ports, 4K-words of external program RAM and 4K-words of EPROM. Ease of use is inherent; just plug the C3M into the host micro as an external device, and the system is up and running. C3M may be used for DSP development, in DSP education, or in an end application where it operates as a stand-alone device. It is ideal for the university and college environment, as well as for the telecommunications and electronics industries.

9.4 Third-Party Consultants

Many third parties serve as consultants, offering comprehensive technical support services to clients. They may custom design and develop hardware and software systems, contract research efforts, and/or offer general consulting services. Each third party consultant specializes in some area of digital signal processing applications. Table 9-2 lists the name, phone number, and area of expertise for those individuals and companies that offer consulting services. Consultants are listed alphabetically in one of six regional areas (five in the U.S. plus Canada):

1) Eastern
2) Central
3) Mountain
4) Pacific SW
5) Pacific NW
6) Canada

Table 9-2. Third-Party Consultant List

EASTERN	
NAME	**AREA(S) OF EXPERTISE**
Critical Path Engineering 404-926-8361 404-972-3072	Digital H/W Design Realtime Processing
Digital Audio Corp. Dr. J.E. Paul 919-848-0845	DSP H/W Development DSP S/W Development
Dragon Systems Mr. John Robbins 617-965-5200	Dependent Speech Recognition
DSP Associates Mr. Amnon Aliphas 617-964-3817	Voice Processing Compression Recognition DSP Seminars
DSP Software Engineering 617-932-8750	Realtime Speech Processing Algorithm s and Hardware Design Image Processing Array Processing and Microcode Development Computer Graphics and CAD workstation Design
C. Gold Associates Dr. Calman Gold 802-333-4769	Digital Signal Processing Instrumentation and Control
Kresse, Mr. Jim 609-985-3068	Speech Processing Telecommunications Audio
Kruger, Frederick M. 516-543-5392	Realtime Signal Processing
Langmann, Mr. David 202-232-7999	Digital Signal Processing H/W Digital Signal Processing S/W
Patnaik, Hare K. 313-977-0742	DSP-Based Instrumentation
David Sarnoff Research Center Subsidiary of SRI International Mr. Hugh E. White 609-734-2523	Communications
Signal Processing Technology Mr. William M. Norr 201-788-3034	Digital Signal Processing Radar, Sonar, Voice Image Processing

Table 9-2. Third-Party Consultant List (Continued)

EASTERN (cont.)	
NAME	**AREA(S) OF EXPERTISE**
Sky Computers, Inc. Dr. Gerald N. Shapiro 508-454-6200	Digital Signal Processing H/W Digital Signal Processing S/W
Sonitech International Mr. Yogendra Jain 617-235-6824	Implementation of DSP Algorithms H/W System Development S/W System Development
Stevens Institue of Technology Dept. of EE & Computer Science Mr. Dhadesugoor Vaman 201-420-5849	Signal Processing Speech Coding & Voice Data Switch Information Networks
Stow Computer Mr. George Otto 508-897-6838	DSP H/W Design Prototyping DSP S/W Design Prototyping
CENTRAL	
NAME	**AREA(S) OF EXPERTISE**
ADICON Consulting and Design Mr. Peter Miczek 414-276-8080	H/W, S/W and System Design Test Equipment
Gas Light Software Mr. Gary A. Sitton 713-729-1257	Digital Signal Processing Time Series Speech, Numerical Analysis
Gunn, James E. 214-669-9350	Modems Telecommunications
Meshkat, Mr. Saeid 612-557-0801	Digital Control Adaptive Control
Pandian, Paul 214-960-2747	Telecommunications Instrumentation
Voice Control Systems Mr. Frank Sharp 214-386-0300	Speech Processing
MOUNTAIN	
NAME	**AREA(S) OF EXPERTISE**
Aztek Engineering, Inc. Mr. J. Mark Elder 303-665-7250	Telecommunications

Table 9-2. Third-Party Consultant List (Continued)

PACIFIC SW	
NAME	**AREA(S) OF EXPERTISE**
Computalker Consultants Rice, D. Lloyd 213-393-7781	Speech Telecommunications
Computools Mr. James W. Collier 213-207-6640	Computer Systems Design & S/W Communication Signal Processing
Digital Sound Corp. Mr. Bob Kelly 805-569-0700	Audio Input/Output Hardware Speech/Acoustic Algorithms
Dr. Design Inc. Mr. Marco Jeffries Thompson 619-457-4545	Graphics & Video
DSP Systems Corp. Mr. Louis Schirm IV 714-630-1330	Realtime Signal Processing
FORTH, Inc. Mr. Jeff Mellinger 213-372-8493	DSP S/W Design and Prototyping
Minisystems Associates Mr. Bruce Flaxman 213-645-7600	Nationwide Temp. Help Agency Engineers, Programmers, Technical Writers
Parallel Processing, Inc. Mr. Paul Cronin 714-583-7899	Computer System Simulation Multiprocessor Design DSP & Graphic Application S/W
San Diego State University Electrical & Computer Engr Dept. 619-594-3702	Low Rate Speech & Image Encoding Vector Quantization Dr. Huseyin Abut
Signal Technology Dr. Steven B. Davis 805-683-3771	Signal Processing S/W, Filter Design Spectral Analysis, Wave Form Display/Edit Feature Extraction & Pattern Recognition
Sklar Technology Lab Mr. Horace J. Sklar 619-489-2809	DSP H/W & S/W Development DSP Systems Design
Sorrento Valley Associates Mr. Ed Nagy 619-452-0102	Speech & Image Processing Image Compression/Printing

Table 9-2. Third-Party Consultant List (Concluded)

PACIFIC NW	
NAME	**AREA(S) OF EXPERTISE**
DSP Consulting Mr. Dan Cox 415-961-4729	Voice & Telecom H/W & S/W Design Instructor for DSP Training
Hummingbird Software, Inc. Mr. Steven D. Cutcomb 415-965-2833	S/W Development & Simulation DSP Firmware Development
Lexington Engineering Mr. Doug Bourn 408-247-7909	Hardware Design for DSP Software Engineering Systems Design
Nysen,Mr. Paul 415-369-8741	Realtime Signal Processing
Redington, Dr. Dana 415-369-8741	Realtime Data Acquisition Realtime Signal Processing Biomedical Specialization
Sern Electronics, Inc. Mr. Steve Rosenberg 503-646-2411	DSP for Systems/Boards S/W & Microcomputer System Design Computer Architecture & Micro Programming
Teknekron Communications Systems Mr. Bill Eichen 415-548-4100	Modems.Facsimile Echo Cancellation Digital Radio Transmission
Telinnovation Mr. Charles Davis 408-37-0777	Telecommunications
CANADA NW	
NAME	**AREA(S) OF EXPERTISE**
Geoacoustics Inc. Mr. Jack Dodds 416-727-8207	Digital Signal Processing Geophysics Software

9.5 Trademarks

The trademarks that have been mentioned in this document are credited to the respective corporation in Table 9-3

Table 9-3. Trademark List

TRADEMARK	CORPORATION
Apple	Apple Computers, Inc.
AOS	Data General
Avocet	Avocet Systems, Inc.
AT, XT	International Business Machines Corp.
AVLIB, AVLINK, AVMAC	Avocet Systems, Inc.
Avocet, AVREF, AVSIM	Avocet Systems, Inc.
CP/M, CP/M-80, CP/M-86	Digital Research, Inc.
CROSSTALK, CROSSTALK XVI	Microstuf, Inc.
DEC, DEC-10	Digital Equipment Corp.
DFDP	Atlanta Signal Processors, Inc.
DISPRO, SPECTIM	Signix Corp.
DSPL	Televic
DSPS	Digital Signal Processing Software
HP 64000	Hewlett-Packard
IBM	International Business Machines Corp.
ILS	Signal Technology, Inc.
Intel	Intel Corp.
I*S*P	Bedford Research
LOGICIAN, PMX	Daisy Systems Corp.
Macintosh	Apple Computers, Inc.
Microstuf	Microstuf, Inc.
MICROVAX, MICRO-11	Digital Equipment Corp.
MP/M	Digital Research, Inc.
MS-DOS	Microsoft, Inc.
Multibus	Intel Corp
PC-DOS	International Business Machines Corp.
PDP, PDP-11, Q-Bus	Digital Equipment Corp.
RSL	Digital Signal Processing Software
RT-11, RSX-11M	Digital Equipment Corp.
SPIRE	Massachusetts Institute of Technology
SPOX	Spectron MicroSystems Inc.
Sun	Sun Microsystems, Inc.
SuPPort	Pacific Microcircuits, Ltd.
TEKHEX	Tektronix Corp.
TIMS	Emona Enterprises Pty Ltd.
TI-Speech	Texas Instruments, Inc.
TurboDos	Software 2000, Inc.
Ultrix	Digital Equipment Corp
Unibus	Digital Equipment Corp
UNIX	Bell Laboratories
VAX, VMS, VT-52, VT-100	Digital Equipment Corp.
VMEbus	Motorola, Inc.
VMEdsp	Burr-Brown Corp.
VoiceKey	Votan
Z-EDIT	Gas Light Software

Appendix A

Product Order Information

This section provides TMS320 family development support information, device part numbers, and support tool order information for all TMS320 products. Table A-1 lists important information about each DSP chip. Table A-2 and Table A-3 give the ordering information for all the TMS320 hardware and software support tools available. Table A-4 provides a list and description of the development tool connections to a target system.

A discussion of the TMS320 device prefix and suffix designators is included to assist in understanding the TMS320 product numbering system.

Table A-1. TMS320 Digital Signal Processor Part Numbers

DEVICE NAME	OPERATING FREQUENCY	PACKAGE TYPE	TYPICAL* DISSIPATION	TEMP RANGE
TMS32010NL†	20 MHz	Plastic 40-pin DIP	900 mW	0/70 C
TMS320C10NL-14 TMS320C10NL† TMS320C10NL-25.	14 MHz 20 MHz 25 MHz	Plastic 40-pin DIP	140 mW 165 mW 200 mW	0/70 C 0/70 C 0/70 C
TMS320C10FNL TMS320C10FNL25	20 MHz 25 MHz	Plastic 44-lead PLCC	165 mW 200 mW	0/70 C 0/70 C
TMS320C10NA	20 MHz	Plastic 40-pin DIP	165 mW	-40/85 C
TMS320C14FNL	25 MHz	Plastic 68-lead PLCC	275 mW	0/70 C
TMS320E14FZL	25 MHz	Ceramic 68-lead CerQuad	325 mW	0/70 C
TMS320C15NL‡ TMS320C15NL-25	20 MHz 25 MHz	Plastic 40-pin DIP	165 mW 200 mW	0/70 C 0/70 C
TMS320C15FNL TMS320C15FNL25	20 MHz 25 MHz	Plastic 44-lead PLCC	165 mW 200 mW	0/70 C 0/70 C
TMS320E15JDL‡ TMS320E15JDL25	20 MHz 25 MHz	Ceramic 40-pin DIP	275 mW 325 mW	0/70 C 0/70 C
TMS320E15FZL	20 MHz	Ceramic 44-lead CerQuad	275 mW	0/70 C
TMS320E15JDA	20 MHz	Ceramic 40-pin DIP	275 mW	-40/85 C

† Military version available
‡ Military version planned; contact nearest TI Field Sales Office for availability
* Typical dissapation calculated from typical I_{CC} current and nominal V_{CC} supply voltage

Table A-1. TMS320 Digital Signal Processor Part Numbers (Concluded)

DEVICE NAME	OPERATING FREQUENCY	PACKAGE TYPE	TYPICAL* DISSIPATION	TEMP RANGE
TMS320C17NL	20 MHz	Plastic 40-pin DIP	250 mW	0/70°C
TMS320C17FNL	20 MHz	Plastic 44-lead PLCC	250 mW	0/70°C
TMS320E17JDL	20 MHz	Ceramic 40-pin DIP	275 mW	0/70°C
TMS320E17FZL	20 MHz	Ceramic 44-lead CerQuad	275 mW	0/70°C
TMS320E17JDA	20 MHz	Ceramic 40-pin DIP	275 mW	-40/85°C
TMS32020GBL†	20 MHz	Ceramic 68-pin PGA	1250 mW	0/70°C
TMS320C25GBL†	40 MHz	Ceramic 68-pin PGA	500 mW	0/70°C
TMS320C25FNL	40 MHz	Plastic 68-lead PLCC	500 mW	0/70°C
TMS320C25GBA	40 MHz	Ceramic 68-pin PGA	500 mW	-40/85°C
TMS320C25-50	50 MHz	Plastic 68-lead PLCC	500 mW	0/70°C
TMS320E25FZL	40 MHz	Ceramic 68-lead CerQuad	500 mW	0/70°C
TMS320C30GBH‡	33 MHz	Ceramic 180-pin PGA C	1500 mW	0/70°C

† Military version available
‡ Military version planned; contact nearest TI Field Sales Office for availability
* Typical dissapation calculated from typical I_{CC} current and nominal V_{CC} supply voltage

Table A-2. TMS320 Software Development Support Tools

PRODUCT	PC/MS-DOS	VAX (VMS)†	VAX (ULTRIX)‡	SUN-3 UNIX‡
TMS320C1x				
Assembler/Linker	TMDS3242850-02	TMDS3242250-08	TMDS3242260-08	TMDS3242550-08
Simulator	TMDS3240811-02	TMDS3240211-08		
Digital Filter Design Package (DFDP)	DFDP-IBM002			
DSP Software Library	TMDC3240812-12	TMDC3240212-18		
TMS320 Bell 212A Modem Software	TMDX3240813-12			
Data Encryption Standard Software	TMDX3240814-12			
TMS320C2x				
Assembler/Linker	TMDS3242850-02	TMDS3242250-08	TMDS3242260-08	TMDS3242550-08
C compiler	TMDX3242855-02	TMDX3242255-08	TMDX3242265-08	TMDX3242555-08
Simulator	TMDS3242851-02	TMDS3242251-08		
SoftWare Development System (SWDS)	TMDX3268821			
Digital Filter Design Package (DFDP)	DFDP-IBM002			
DSP Software Library	TMDC3240812-12	TMDC3240212-18		
TMS320C3x				
Assembler/Linker	TMDX3243850-02	TMDX3243250-08	TMDX3243260-08	TMDX3243550-08
Simulator	TMDX3243851-02	TMDX3243251-08	TMDX3243261-08	
C compiler	TMDX3243855-02	TMDX3243255-08	TMDX3243265-08	TMDX3243555-08
Digital Filter Design Package (DFDP)	DFDP-IBM002			
DSP Software Library	TMDC3240812-12	TMDC3240212-18		
SPOX	Packaged with TMS320C3x XDS1000 Development Environment			

† in Backup format
‡ in TAR format

Table A-3. TMS320 Hardware Development Support Tools

PRODUCT	PART NUMBER
TMS320C1x	
EVALUATION TOOLS: Evaluation Module (EVM) Analog Interface Board 1 (AIB1) TMS320E15 EPROM DSP Starter Kit	 RTC/EVM320A-03 RTC/EVM320C-06 RTC/EVM320E-15
EMULATORS: TMS320C10/C15 XDS/22 TMS320C14 XDS/22 TMS320C17 XDS/22	 TMDS3262211 TMDX3262214 TMDX3262217
EPROM PROGRAMMING ADAPTER SOCKETS: TMS320E15/E17 40-pin to 28-pin conversion TMS320E14 68-pin to 28-pin conversion	 RTC/PGM320A-06 TMDX3270110
ADDITIONAL TARGET CONNECTOR: TMS320C10 44-pin PLCC	 TMDX3288810
TMS320C2x	
EVALUATION TOOLS: Analog Interface Board 2 (AIB2) Analog Interface Board Adapter (for use with AIB1)	 RTC/AIB320A-06 RTC/ADP320A-06
EMULATOR: TMS320C25 XDS/22†	 TMDS3262221
EPROM PROGRAMMING ADAPTER SOCKET: TMS320E25 68-pin to 28-pin conversion	 TMDX3270120
ADDITIONAL TARGET CONNECTORS: TMS320C25 68-pin PGA TMS320C25 68-pin PLCC TMS32020 68-pin PGA	 TMDX3288826 TMDX3288825 TMDX3288820
TMS320C3x	
EMULATORS: XDS500 Emulator XDS1000 Development Environment	 TMDX3260131 TMDX3261030

† - 50-MHz emulation is supported by Macrochip Research Inc. Refer to page 9-68 for more information.

Table A-4. Hardware Development Tool Upgrades

DESCRIPTION	PART NUMBER
TMS32010 XDS/22 to TMS320C10 XDS/22 User Upgrade	TMDX3282216
TMS32020 XDS/22 to TMS320C25 XDS/22 User Upgrade	TMDX3282226
TMS32010/C15 EVM User Upgrade (Firmware/TMS320C15)	RTC/EVM320U-15

A.1 Device and Development Support Tool Prefix Designators

To assist the user in understanding the stages in the product development cycle, Texas Instruments assigns prefix designators in the part number nomenclature. A device prefix designator has three options: TMX, TMP, and TMS, and a development support tool prefix designator has two options: TMDX and TMDS. These prefixes are representative of the evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices (TMS/TMDS). This development flow is defined below.

Device Development Evolutionary Flow:

TMX Experimental device that is not representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully qualified production device.

Support Tool Development Evolutionary Flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development support product.

TMDC Development support product that is unsupported or obsolete

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

> **Note:**
>
> Texas Instruments recommends that prototype devices (TMX or TMP) not be used in production systems since their expected end-use failure rate is undefined but predicted to be greater than standard qualified production devices.

TMS devices and TMDS development support tools have been fully characterized and the quality and reliability of the device has been fully demonstrated. Texas Instruments standard warranty applies.

A.2 Device and Development Support Tool Nomenclature

In addition to the prefix, the device nomenclature includes a suffix that follows the device family name. This suffix indicates the package type (e.g., N, FN, or GB) and temperature range (e.g., L). Figure A-1 provides a legend for reading the complete device name for any TMS320 family member.

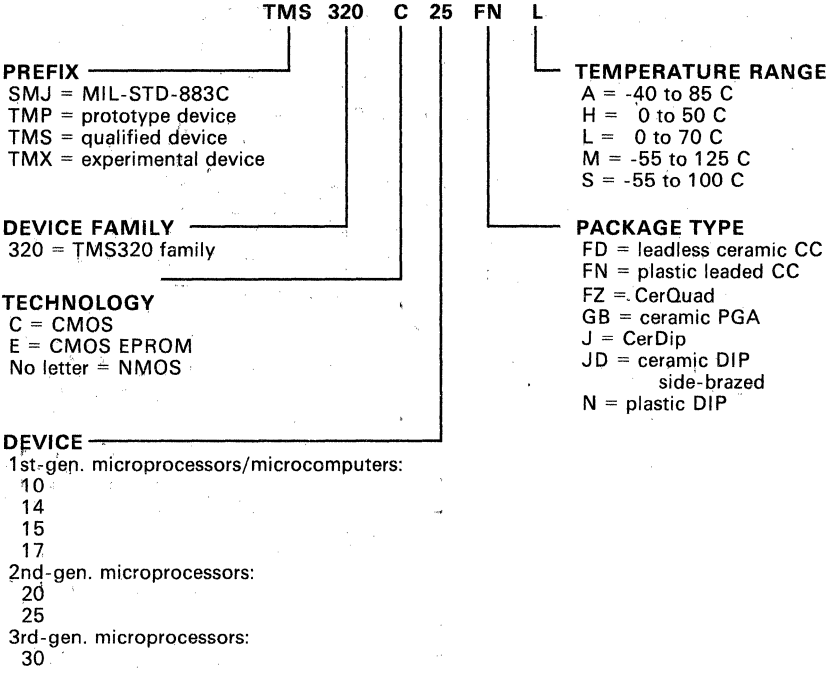

Figure A-1. TMS320 Device Nomenclature

Appendix B

Texas Instruments Factory Repair and Exchange Policy

This section specifies the conditions under which a TI Semiconductor Development Systems product may be returned by an end user for repair subject to the terms of the warranty for such product.

Before returning any product for repair, the Factory Repair Center must be contacted at (713) 274-2285, and a return authorization number obtained (and entered on the Exchange/Repair Questionnaire that must be completed and returned with the product).

Texas Instruments shall not be responsible for any product returned without prior authorization from the Factory Repair Center.

When a product returned to TI for repair is deemed acceptable for repair by TI and no request has been made for the return of the same numbered product, TI reserves the option to repair or exchange the product.

Exchanged products will be replaced with refurbished units that meet TI workmanship standards for refurbished products. Such products may have minor cosmetic blemishes.

Texas Instruments accepts no responsibility for EPROMs containing customer-generated software, which are part of any unit to be repaired.

B.1 Normal Warranty Exchange or Repair

Repair or exchange will be made free of charge, provided:

1) The customer notifies TI of product failure within the applicable warranty period (90 days from the date of shipment from TI or from a TI authorized distributor).

2) TI inspection discloses that the product is defective and that the defect is not the result of accident, misuse, neglect, alteration, improper installation, unauthorized repair, or improper testing.

3) The product is restored to the TI standard configuration for that product.

The customer shall be responsible for providing proof of the date of purchase.

B.2 Non-Warranty Exchange or Repair

Non-warranty factory repair or exchange is available on all "repairable" Development Systems products currently being manufactured; consult the factory for availability on discontinued products.

A product is deemed "repairable" when the cost of repair does not exceed cost of replacement. If a product is not "repairable", the customer will be advised that repair cannot be effected and the product returned to the customer at the customer's expense.

The minimum standard charge for non-warranty repairs, in North America, can be obtained by calling the Factory Repair Center (713) 274-2285. Outside North America, contact the closest TI Regional Technology Center (refer to Section 6.2 for a list). TI will contact the customer for approval prior to effecting any repair or replacement that exceeds the quoted minimum standard charge.

B.3 Shipping Instructions

The following shipping instructions should be followed to ensure the desired service:

1) Before returning any product for repair, the Factory Repair Center must be contacted at (713) 274-2285, and a return authorization number obtained (and entered on the Exchange/Repair Questionnaire).

   TI shall not be responsible for any product returned without prior authorization by the factory repair center.

2) The following information **must** accompany the returned product. The TI Factory Repair and Exchange Questionnaire should be used to ensure that the required information is provided:

   - Factory Repair Center return authorization number
   - Customer name and phone number
   - Purchase order number (if applicable)
   - Model number
   - Serial number
   - "Ship to" address; instruction for insurance and method of shipment (unless otherwise specified, TI will ship UPS insured for the minimum)
   - "Bill to" address
   - Description of symptoms of malfunction
   - Type of service requested.

> **Note:**
>
> The customer should retain a copy of the Exchange Questionnaire and shipping documentation in the event that tracing of the product should be necessary.

3) The product must be returned freight prepaid, to the appropriate Repair Center.

   - In the United States and Canada, contact:

     Texas Instruments Incorporated
     Semiconductor Group
     Factory Repair Center, M/S 730
     12203 Southwest Freeway
     Houston, Texas 77477

     (713) 274-2285

   - Outside of the United States and Canada, contact the closest TI Regional Technology Center (refer to Section 6.2 for a list).

4) If the customer has any questions regarding this policy or the returned product status, he may contact the Factory Repair Center directly.

B.4 System Configuration

Systems returned for repair or exchange will be upgraded to the latest revision, unless otherwise specified. When the customer has made modifications to the product, repair or replacement is considered "non-warranty."

TI will attempt the repair of such a product provided the customer has restored the product to its standard configuration. Labor and material will be charged at the TI then-current standard rate for all necessary removals or repairs to customer-made modifications, if such is required to test the returned product in accordance with the TI specification for that product. TI reserves the right to refuse the repair of any product that has been modified such that the configuration as changed is untestable.

TI DOES NOT ACCEPT RESPONSIBILITY FOR ADDITIONAL COMPONENTS (OR SOFTWARE PROGRAMMED INTO COMPONENTS) ADDED BY THE CUSTOMER TO A PRODUCT SUBMITTED FOR REPAIR.

B.5 Expedited Requests

Expedited requests will be accepted when the product submitted for exchange is available from Factory Repair Center inventory. Normal turnaround time for expedited requests is one (1) working day from receipt of the returned product at the Factory Repair Center.

Requests to ship replacement product prior to receipt of the returned unit by the Factory Repair Center will be honored if a purchase order is issued for the current retail price of the product (in addition to the appropriate exchange and shipping charges). Upon receipt of the returned unit at the Factory Repair Center and verification of repairability, credit will be issued in the amount of the price invoiced for the exchange product. A purchase order cannot be accepted for this purpose if the customer does not have credit established with Texas Instruments Incorporated, Semiconductor Group.

B.6 Warranty

Repaired or exchanged assemblies may contain either new parts or refurbished parts of like quality and are warranted to be free of defects in material and workmanship for a period of 30 days from date of shipment, provided such warranty repair shall not operate to reduce the original product warranty. The foregoing warranties for goods are in lieu of all warranties, express, implied, or statutory, including but not limited to, any implied warranties of merchantability and fitness for a particular purpose, and of any other warranty obligation on the part of TI.

Appendix C

Texas Instruments Program License Agreement

The following is an example of the program license agreement associated with software development tools available from Texas Instruments. It is included here for information only. Terms and conditions vary slightly depending on the medium of use (i.e., Professional Computer or VAX) and the country of distribution.

TEXAS INSTRUMENTS PROGRAM LICENSE AGREEMENT

This program license agreement is displayed conspicuously in the package so that you can read it before opening the package. Retaining possession of the package and using the program and materials contained in it indicates that you have agreed to the terms and conditions of this agreement. If you do not agree with them, you should promptly return the package unopened to the seller from whom you obtained possession and your money will be refunded.

LICENSE AND TERM

Texas Instruments Incorporated, its subsidiaries (TI), and any applicable licensors grant to you a nonexclusive, nontransferable license to use the software program and related documentation in this package (collectively referred to as the "Program") on a single computer. Any attempted sublicense, assignment, or other transfer of the Program or the rights or obligations of this Agreement without the prior written consent of TI shall be void. This license will terminate if you fail to comply with its terms.

Files designated with "RTS" (Run Time Support) Libraries,as a component of the pathname or the filename may be modified and/or merged into another program for your use on a single machine. Any part of the RTS libraries merged into another program will continue to be subject to the terms and conditions of this Agreement, except as expressly provided herein. RTS libraries may be used to create user programs. Such user programs may include copies of code derived from the RTS libraries and/or modifications of these libraries. Such user programs shall not be subject to any restrictions on copying or use.

The program and documentation are copyrighted. You may make two (2) copies of the program for backup, modification, and archival purposes. Unauthorized copying, or reverse compiling, and disassembling of programs in object format are prohibited. Title to the program is not transferred to you by this license.

PROGRAM LIMITATIONS

TI does not warrant that the Program will be free from error or will meet your specific requirements. You assume complete responsibility for decisions made or actions taken based on information obtained using the Program. Any statements made concerning the utility of the Program are not to be construed as expressed or implied warranties.

TI makes no warranty or condition, either expressed or implied, including, but not limited to, any implied warranties of merchantability and fitness for a particular purpose, regarding the program and makes the program available solely on an "as is" basis.

LIMITED WARRANTY ON MEDIA AND DAMAGES DISCLAIMER

The media (not the Program) is warranted to the original purchaser against defects in material and workmanship for a period of ninety (90) days from the date of original purchase.

Defective media under warranty will be replaced when it is returned postage paid with a copy of the purchase receipt to the TI Semiconductor Group located in Houston, Texas. The replacement media is warranted for three (3) months from date of replacement. Other than the postage requirement (when allowed by law), no charge will be made for the replacement. **This paragraph expresses TI's sole liability and your exclusive remedy.**

Neither TI nor any applicable licensor shall be responsible for incidental or consequential damages. This warranty gives you specific legal rights and you may also have other rights which vary from state to state. Some states do not allow the exclusion or limitations of incidental or consequential damages or limitations on how long an implied warranty lasts, so above limitations or exclusions may not apply to you.

EXPORT CONTROL

The re-export of United States origin software is subject to United States laws under the Export Administration Act of 1969 as amended. Any further sale of the program shall be in compliance with the United States Department of Commerce Administration Regulations. Compliance with such regulations is your responsibility and not the responsibility of TI.

Appendix D

ROM Codes

Size of a printed circuit board must be considered in many DSP applications. To fully utilize the board space, Texas Instruments offers two options which will reduce the chip count and provide a single-chip solution to its customers. these options incorporate 4K-words of on-chip program memory from either a mask programmable ROM or an EPROM. This allows the customer to use a code-customized processor for a specific application while taking advantage of the following:

- Greater memory expansion
- Lower system cost
- Less hardware and wiring
- Smaller PCB

A repetative routine or an entire algorithm can be programmed into the on-chip ROM of a TMS320 DSP. TMS320 programs can also be expanded by using external memory; this reduces chip count and allows for a more flexible program memory. Multiple functions are easily implemented by a single device, thus enhancing syste, capabilities.

TMS320 Development Tools are used to develop, test, refine, and finalize the algorithms. The microprocessor/microcomputer (MC/$\overline{\text{MP}}$ for TMS320C1x and TMS320C3x, MP/$\overline{\text{MC}}$ for TMS320C2x only) mode is available on all ROM-coded TMS320 DSP devices when accessing either on-chip or off-chip memory is required. The microprocessor mode is used to develop, test, and refine a system application. In this mode of operation, the TMS320 acts as a standard microprocessor by using external memory only. When the algorithm has been finalized, the designer may submit the code to Texas Instruments for masking into the on-chip program ROM. At that time, the TMS320 becomes a microcomputer which executes customized program out of the on-chip ROM. Should the code need changing or upgrading, the TMS320 may once be used in the microprocessor. This shortens the field upgrade time and avoids the possibility of inventory obsolescence.

Figure D-1 illustrates the procedural flow for TMS320 masked parts. When ordering, there is a one-time/non-refundable charge for mask-tooling. A minimum production order per year is required for any masked-ROM device. A ROM code will be deleted from the TI system after one year from the last delivery.

Digital signal processors with an EPROM option offer a solution for low-volume orders. The EPROM option allows for form-factor emulation. Field upgrades and changes are possible with the EPROM option.

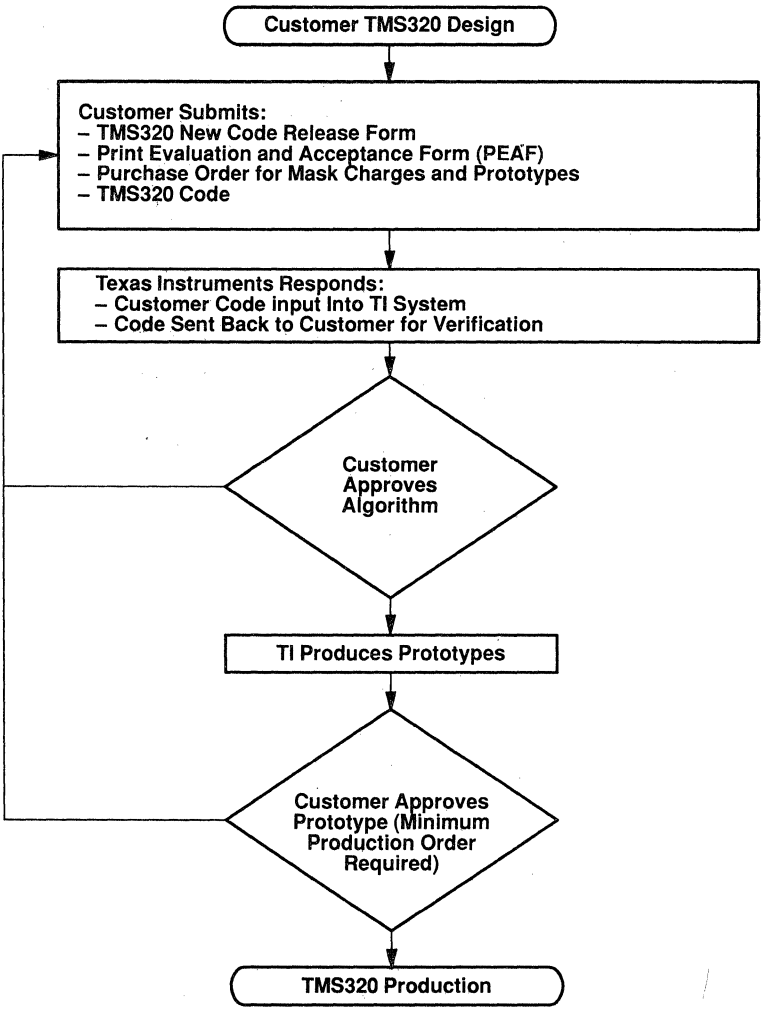

Figure D-1. TMS320 ROM Code Flowchart

A TMS320 ROM code may be submitted in one of the following formats (the preferred media is 5.25" floppies):

5.25" FLOPPY:	TI-tagged or COFF format from Cross-Assembler
EPROM (TMS320):	TMS320E14, TMS320E15, TMS320E17, TMS320C25
EPROM (others)	TMS27C64
PROM:	TBP28S86, TBP28S166
MODEM (BBS):	TI-tagged or COFF format from Cross-Assembler

When a code is submitted to Texas Instruments for masking, the code is reformatted to accommodate the TI mask generation system. System level verification by the customer is therefore necessary. Although the code has been reformatted, it is important that the changes remain transparent to the user and do not affect the execution of the algorithm. The formatting changes made involve the removal of address relocation information (the code address begins at the base address of the ROM in the TMS320 device and progresses without gaps to the last address of the ROM on the TMS320 device), and addition of data in the reserved locations of the ROM for device ROM test. Note that because these changes have been made, a checksum comparison is not a valid means of verification.

ROM code algorithms may also be submitted by secure electronic transfer via a modem. Contact the nearest TI Field Sales Office for further information.

With each masked device order, the customer must sign a disclaimer stating:

> "The units to be shipped against this order were assembled, for expediency purposes, on a prototype (i.e., non-production qualified) manufacturing line, the reliability of which is not fully characterized. Therefore, the anticipated inherent reliability of these prototype units cannot be expressly defined."

and a release stating:

> "Any masked ROM device may be resymbolized as TI standard product and resold as though it were an unprogrammed version of the device at the convenience of Texas Instruments."

Contact the nearest TI Field Sales Office for more information on procedures, leadtimes, and cost.

Appendix E

Quality and Reliability

The quality and reliability performance of Texas Instruments Microprocessor and Microcontroller Products, which includes the three generations of TMS320 digital signal processors, relies on feedback from:

- Our customers
- Our total manufacturing operation from front-end wafer fabrication to final shipping inspection
- Product quality and reliability monitoring.

Our customer's perception of quality must be the governing criterion for judging performance. This concept is the basis for Texas Instruments Corporate Quality Policy, which is as follows:

> "For every product or service we offer, we shall define the requirements that solve the customer's problems, and we shall conform to those requirements without exception."

Texas Instruments offers a leadership reliability qualification system, based on years of experience with leading-edge memory technology as well as years of research into customer requirements. Quality and reliability programs at TI are therefore based on customer input and internal information to achieve constant improvement in quality and reliability.

E.1 Reliability Stress Tests

Accelerated stress tests are performed on new semiconductor products and process changes to ensure product reliability excellence. The typical test environments used to qualify new products or major changes in processing are:

- High-temperature operating life
- Storage life
- Temperature cycling
- Biased humidity
- Autoclave
- Electrostatic discharge
- Package integrity
- Electromigration
- Channel-hot electrons (performed on geometries less than 2.0 μm).

Typical events or changes that require internal requalification of product include:

- New die design, shrink, or layout
- Wafer process (baseline/control systems, flow, mask, chemicals, gases, dopants, passivation, or metal systems)
- Packaging assembly (baseline control systems or critical assembly equipment)
- Piece parts (such as lead frame, mold compound, mount material, bond wire, or lead finish)
- Manufacturing site.

TI reliability control systems extend beyond qualification. Total reliability controls and management include product ramp monitor as well as final product release controls. MOS memories, utilizing high-density active elements, serve as the leading indicator in wafer-process integrity at TI MOS fabrication sites, enhancing all MOS logic device yields and reliability. TI places more than several thousand MOS devices per month on reliability test to ensure and sustain built-in product excellence.

Table E-1 lists the microprocessor and microcontroller reliability tests, the duration of the test, and sample size. The following defines and describes those tests in the table.

AOQ (Average Outgoing Quality) Amount of defective product in a population, usually expressed in terms of parts per million (PPM).

FIT (Failure In Time) Estimated field failure rate in number of failures per billion power-on device hours; 1000 FITS equals 0.1 percent fail per 1000 device hours.

Operating lifetest Device dynamically exercised at a high ambient temperature (usually 125°C) to simulate field usuage that would

	expose the device to a much lower ambient temperature (such as 55°C). Using a derived high temperature, a 55°C ambient failure rate can be calculated.
High-temperature storage	Device exposed to 150°C unbiased condition. Bond integrity is stressed in this environment.
Biased humidity	Moisture and bias used to accelerate corrosion-type failures in plastic packages. Conditions include 85°C ambient temperature with 85-percent relative humidity (RH). Typical bias voltage is +5 V and ground on alternating pins.
Autoclave (pressure cooker)	Plastic-packaged devices exposed to moisture at 121°C using a pressure of one atmosphere above normal pressure. The pressure forces moisture permeation of the package and accelerates corrosion mechanisms (if present) on the device. External package contaminates can also be activated and caused to generate inter-pin current leakage paths.
Temperature cycle	Device exposed to severe temperature extremes in an alternating fashion (-65°C for 15 minutes and 150°C for 15 minutes per cycle) for at least 1000 cycles. Package strength, bond quality, and consistency of assembly process are stressed in this environment.
Thermal shock	Test similar to the temperature cycle test, but involving a liquid-to-liquid transfer, per MIL-STD-883C, Method 1011.
PIND	Particle Impact Noise Detection test. A non-destructive test to detect loose particles inside a device cavity.
Mechanical Sequence:	
Fine and gross leak	Per MIL-STD-883C, Method 1014.5
Mechanical shock	Per MIL-STD-883C, Method 2002.3, 1500 g, 0.5 ms, Condition B
PIND (optional)	Per MIL-STD-883C, Method 2020.4
Vibration, variable frequency	Per MIL-STD-883C, Method 2007.1, 20 g, Condition A
Constant acceleration	Per MIL-STD-883C, Method 2001.2, 20 kg, Condition D, Y1 Plane min
Fine and gross leak	Per MIL-STD-883C, Method 1014.5

Electrical test	To data sheet limits
Thermal Sequence:	
Fine and gross leak	Per MIL-STD-883C, Method 1014.5
Solder heat (optional)	Per MIL-STD-750C, Method 1014.5
Temperature cycle (10 cycles minimum)	Per MIL-STD-883C, Method 1010.5, -65 to +150°C, Condition C
Thermal shock (10 cycles minimum)	Per MIL-STD-883C, Method 1011.4, -55 to +125°C, Condition B
Moisture resistance	Per MIL-STD-883C, Method 1004.4
Fine and gross leak	Per MIL-STD-883C, Method 1014.5
Electrical test	To data sheet limits
Thermal/Mechanical Sequence:	
Fine and gross leak	Per MIL-STD-883C, Method 1014.5
Temperature cycle (10 cycles minimum)	Per MIL-STD-883C, Method 1010.5, -65 to +150°C, Condition C
Constant acceleration	Per MIL-STD-883C, Method 2001.2, 30 kg, Y1 Plane
Fine and gross leak	Per MIL-STD-883C, Method 1014.5
Electrical test	To data sheet limits
Electrostatic discharge	Per MIL-STD-883C, Method 3015
Solderability	Per MIL-STD-883C, Method 2003.3
Solder heat	Per MIL-STD-750C, Method 2031, 10 sec
Salt atmosphere	Per MIL-STD-883C, Method 1009.4, Condition A, 24 hrs min
Lead pull	Per MIL-STD-883C, Method 2004.4, Condition A
Lead integrity	Per MIL-STD-883C, Method 2004.4, Condition B1
Electromigration	Accelerated stress testing of conductor patterns to ensure acceptable lifetime of power-on operation
Resistance to solvents	Per MIL-STD-883C, Method 2015.4

Table E-1. Microprocessor and Microcontroller Tests

TEST	DURATION	SAMPLE SIZE	
		PLASTIC	CERAMIC
Operating life, 125°C, 5.0 V	1000 hrs	129	129
Storage life, 150°C	1000 hrs	77	77
Biased 85°C/85 percent RH, 5.0 V	1000 hrs	129	-
Autoclave, 121°C, 1 ATM	240 hrs	77	-
Temperature cycle, -65 to 150°C	1000 cyc†	129	129
Thermal shock, -65 to 150°C	200 cyc	77	77
Electrostatic discharge, ±2 kV		15	15
Latch-up (CMOS devices only)		5	5
Mechanical sequence		-	38
Thermal sequence		-	38
Thermal/mechanical sequence		-	38
PIND		-	45
Internal water vapor		-	3
Solderability		22	22
Solder heat		22	22
Resistance to solvents		15	15
Lead integrity		15	15
Lead pull		22	-
Lead finish adhesion		15	15
Salt atmosphere		15	15
Flammability (UL94-V0)		3	-
Thermal impedance		5	5

† For severe environments; reduced cycles for office environments

TI Qualification test updates are available upon request at no charge. TI will consider performing any additional reliability test(s), if requested. For more information on TI quality and reliability programs, contact the nearest TI Field Sales Office.

Note:

Texas Instruments reserves the right to make changes in MOS Semiconductor test limits, procedures, or processing without notice. Unless prior arrangements for notification have been made, TI advises all customers to reverify current test and manufacturing conditions prior to relying on published data.

Appendix F

TMS320 EPROM Programming

The EPROM versions of the TMS320 family include a 4K-word x 16-bit EPROM implemented using an industry-standard EPROM cell. These devices can be used for prototyping, early field testing, and low volume production. The CMOS counterparts of the TMS320 family with a 4K-word masked ROM offer a migration path for cost-effective higher volume production. EPROM adapter sockets are available that provide 40-pin to 28-pin conversion for programming the TMS320E15/E17. Adapter sockets are also available to provide the 68-pin to 28-pin conversion required for programming the TMS320E14/E25. Refer to Table A-3 of Appendix A for part number information.

Key features of the EPROM cell include standard programming and verification. The EPROM cell also includes a code protection feature that allows code to be protected against copyright violations. The protection feature can be used to protect reading the EPROM contents. This appendix describes erasure, programming, and verification, plus EPROM protection and verification.

F.1 Programming and Verification

The TMS320 EPROM cell is programmed using the same family and service codes as the TMS27C64 8K x 8-bit EPROM. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable read-only memories. They are fabricated using HVCMOS technology. The TMS27C64 is pin-compatible with existing 28-pin ROMs and EPROMs. The TMS320 EPROM family, like the TMS27C64, operates from a single 5-V supply in the read mode. In the programming mode, an additional 12.5-V supply is required. All programming signals are TTL level. For programming outside the resident system, many of the commercial EPROM programmers can be used. Memory locations can be programmed singly, in blocks, or at random.

F.1.1 Block Programming

When block programming, the data is loaded into the TMS320 EPROM one byte at a time. From a programmer's point of view, data for each memory location is loaded high byte first, low byte second.

Caution:

The EPROM versions of the TMS320 family do not support the signature mode available with some EPROM programmers. The signature mode on these programmers places a high voltage (12.5-VDC) on address pin A9. The TMS320 EPROM cell is not designed for this feature and will be damaged if subjected to this voltage. A 3.9 kOhm resistor is standard on the TI programmer socket between address pin A9 and the programmer. This protects the device from the unintentional use of the signature mode.

F.2 Erasure

Before programming, the TMS320 EPROM device is erased by exposing the chip (through the transparent lid) to high-intensity ultraviolet-light (wavelength 2537 angstroms). For information on the recommended exposure time and lamp location for a particular TMS320 EPROM device, consult the appropriate TMS320 User's Guide. After erasure, all bits are in the high state. Note that normal ambient light contains ultraviolet. Therefore, when using a TMS320 EPROM, the transparent window of the device should be covered with an opaque tape or label after erasure. This will prevent the degradation and/or erasure of the programmed data.

F.3 Fast and SNAP! Pulse Programming

Two programming algorithms are available for use with the TMS320 EPROM devices. Fast programming is normally used to program the entire EPROM contents, although individual locations may be programmed separately. Fast programming is supported on the TMS320E15/E17, TMS320E14, and TMS320E25. TI SNAP! Pulse Programming can reduce programming time to a nominal of one second. (Actual programming time will vary as a function of the programmer used). SNAP! Pulse Programming is supported on the TMS320E14 and TMS320E25. For more information on these two programming algorithms, consult the appropriate TMS320 user's guide.

F.4 Program Verify

Information verification of the EPROM versions of the TMS320 family is contained in the appropriate TMS320 user's guide.

F.5 EPROM Protection and Verification

The EPROM protection facility is used to completely disable reading of the EPROM contents to guarantee security of proprietary algorithms. This facility is implemented through a unique EPROM cell called the RBIT (ROM Protect bit) cell. Once the contents to be protected are programmed into the EPROM, the RBIT is programmed, disabling access to the EPROM contents and disabling the microprocessor mode on the device. Once programmed, the RBIT can only be cleared by erasing the entire EPROM array with ultraviolet light, thus maintaining security of the proprietary algorithm. Information on programming and verification of the RBIT can be found in the appropriate TMS320 user's guide.

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