TMS320C6x Interface to External Asynchronous SRAM

APPLICATION REPORT: PRELIMINARY

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TMS320C6x Interface to External Asynchronous SRAM

Abstract

Interfacing external ASRAM to the TMS320C62xx is simple when compared to previous generations of TI DSPs due to the advanced External Memory Interface (EMIF), which provides a glueless interface to a variety of external memory devices.

This document will describe the:

- ❏ EMIF’s control registers and ASRAM signals
- ❏ ASRAM functionality and performance considerations
- ❏ Full example using Toshiba’s TC55V1664FT-12 (64k x 16, 12 ns)
- ❏ Full example using IDT’s IDT71L016L70 (64k x 16, 70 ns)

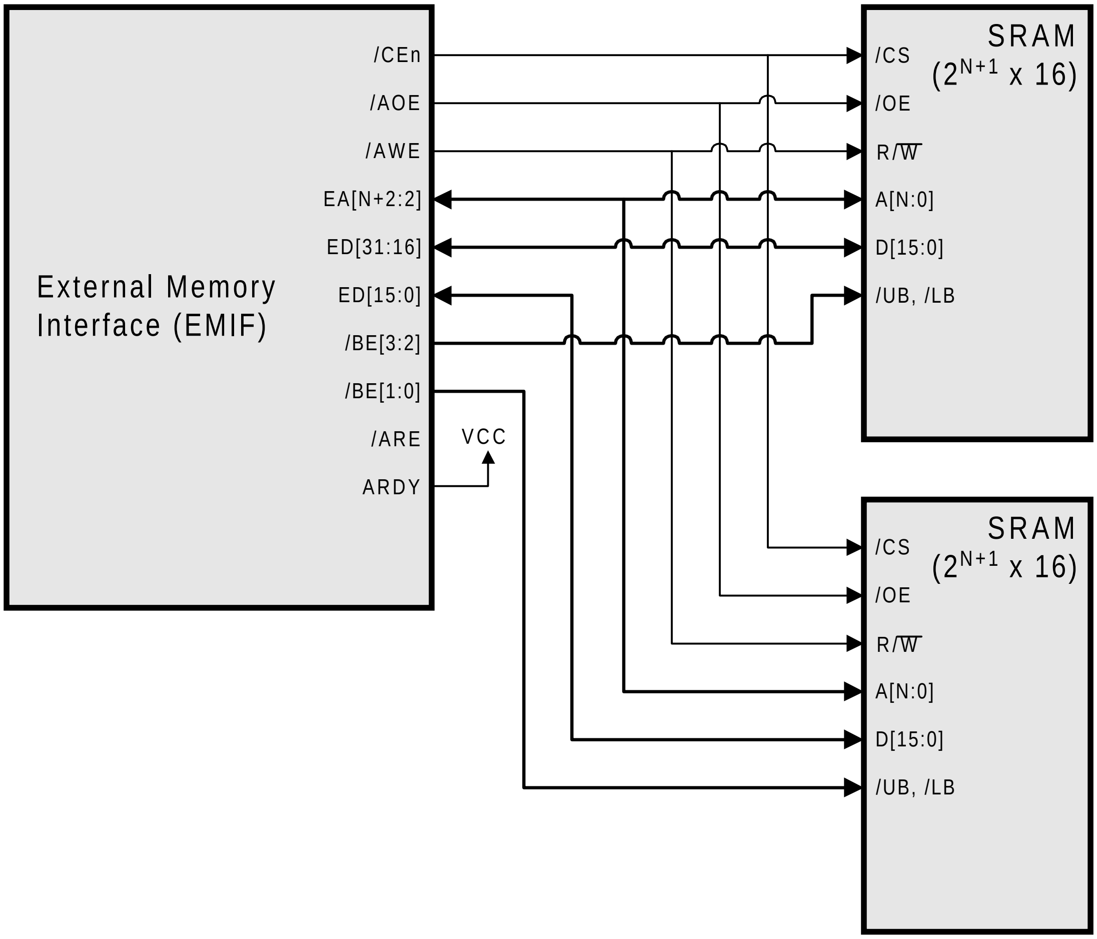
Asynchronous SRAM Interface

The asynchronous interface of the EMIF offers users configurable memory cycles, and can be used to interface to a variety of memory and peripheral types; including SRAM, EPROM, FLASH, as well as FPGA and ASIC designs. This document will focus on the interface between the EMIF and Asynchronous SRAM (ASRAM).

Figure 1 shows an interface to 16 bit wide standard SRAM. Since the ASRAM for this example is 16 bits wide, 2 devices must be used in parallel to produce a 32 bit word. Similarly, if 8 bit wide ASRAM were used, 4 devices would be required.

Notice that in the diagram there is no clock interface, as is indicated by the term asynchronous. The EMIF still uses the internal clock to coordinate the timing of its signals, however, the SRAM responds to the signals at its inputs irrespective of any clock.

Figure 1. EMIF-SRAM Interface



Overview of EMIF

EMIF Signal Descriptions

Figure 2 shows a block diagram of the EMIF. As the figure shows, the EMIF is the interface between external memory and the other internal units of the ‘C6x. The interface with the processor is provided via the DMA controller, Program Memory Controller, and the Data Memory Controller. The signals described in Table 1, however, focus on the ASRAM interface and the shared interface signals.

Figure 2. Block Diagram of EMIF

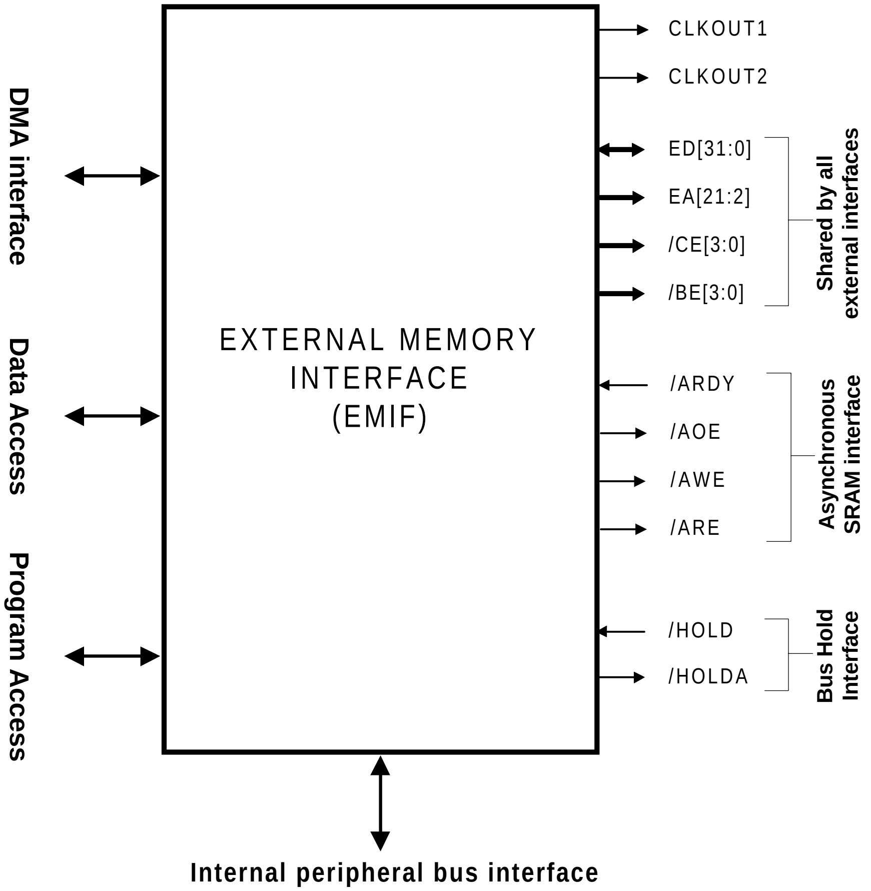


Table 1. EMIF Signal Descriptions : Shared Signals and ASRAM Signals

EMIF Pin	ASRAM Signal	Description
CLKOUT1	N/A	Clock. Clock output - the CPU clock rate.
ED[31:0]	DQ	Data I/O. 32-bit data input/output from external memories and peripherals.
EA[21:2]	A	External Address output. Drives bits 21-2 of the byte address.
/Cen	CS	External /CE0 Chip Select. Active low chip select for CE space 0.
/BE[3:0]	_UB/ _LB	Byte Enables. Active low byte strobes. Individual bytes and halfwords can be selected for both read and write cycles. Decoded from 2 LSBs of the byte address.
/AOE	/OE	Output Enable - active low during the entire period of a read access.
/AWE	/WE	Write Enable - active low during a write transfer strobe period.
/ARE	N/A	Read Enable - active low during a read transfer strobe period. Although not used for standard ASRAM interface, still used logically to determine when the data is read by the EMIF.
ARDY	N/A	Ready input used to insert wait states into the memory cycle. Not used for standard ASRAM interface.

EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory mapped registers within the EMIF. The memory mapped registers are shown in Table 2.

Table 2. EMIF Memory Mapped Registers

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	Reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control

CE Space Control Registers

The four CE Space Control Registers (Figure 3) correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or 32 bit Asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. Table 3 contains a more detailed description of the asynchronous configuration fields.

Figure 3. EMIF CE(0/1/2/3) Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
RW, +1111	RW, +111111	RW, +11	RW, +1111

15 14	13 8	7	6 4	3 2	1 0
Reserved	READ STROBE	rsv	MTYPE	reserved	READ HOLD
R, +11	RW, +111111	R, +0	RW, +010	R, +0	RW, +11

Table 3. EMIF CE(0/1/2/3) Space Control Registers Bitfield Description

Field	**Description**
READ SETUP WRITE SETUP	Setup width. Number of CLKOUT1 cycles of setup for address (EA) and byte enables (/BE(0-3)) before read strobe (/ARE) or write strobe (/AWE) falling. On the first access to a CE space this is also the setup after /CE falling.
READ STROBE WRITE STROBE	Strobe width. The width of read strobe (/ARE) and write strobe (/AWE) in CLKOUT1 cycles.
READ HOLD WRITE HOLD	Hold width. Number of CLKOUT1 cycles that address (EA) and byte strobes (/BE(0-3)) are held after read strobe (/ARE) or write strobe (/AWE) rising.

MTYPE	Memory Type.
	MTYPE=000b, 8-bit wide ROM
	MTYPE=001b, 16-bit wide ROM
	MTYPE=010b, 32-bit wide Asynchronous Interface
	MTYPE=011b, 32-bit wide SDRAM
	MTYPE=100b, 32-bit wide SBSRAM
	MTYPE=other, reserved

Programmable ASRAM Parameters

The EMIF allows a high degree of programmability for shaping asynchronous accesses. The programmable parameters that allow this are:

- ❑ **Setup:** The time between the beginning of a memory cycle (/CE low, address valid) and the activation of the read or write strobe
- ❑ **Strobe:** The time between the activation and deactivation of the read (/ARE) or write strobe (/AWE)
- ❑ **Hold:** The time between the deactivation of the read or write strobe and the end of the cycle (which may be either an address change or the deactivation of the /CE signal)

These parameters are programmable in terms of CPU clock cycles via fields in the EMIF CE Space Control Registers. Separate setup, strobe, and hold parameters are available for read and write accesses. The SETUP, HOLD, and STROBE fields represent actual cycle counts, in contrast to the SDRAM parameters which are the cycle counts - 1.

The SETUP and STROBE fields have minimum count of 1, and because of this a value of 0 in these fields will still be interpreted as a 1 by the C6x. For the first access in a set of consecutive accesses or a single access, the setup period will have a minimum of 2. HOLD has a minimum of 0.

The following sections explain these parameters and the guidelines that should be used when setting the SETUP, HOLD, and STROBE parameters. Table 5 through Table 8 define constraints that will be used in the following discussion.

Margin Considerations

Notice that the output signals from the C6x are output a time t_d after the rising edge of CLKOUT1. The data sheet for the C6x gives both a maximum delay time and a minimum delay time. Therefore, over a range of operating temperatures and supply voltage levels, the actual value of t_d can range between these two extremes. However, for a given set of operating conditions, the delay time will more or less be the same for both the transition from inactive to active and again for the transition from active to inactive. Therefore the effect of t_d on output signals cancels itself out.

For example, (refer to Figure 5) assume that a write pulse (t_{wp}) of 5 ns is required by the memory, the CPU is operating at a frequency of 200 Mhz (5 ns CLKOUT1), and the delay time, t_d, is 3 ns. Assuming that STROBE is set to 1, then the transition of AWE from inactive to active occurs ~3 ns after the rising edge of CLKOUT1, and the transition from active to inactive occurs ~3 ns after the next rising edge of CLKOUT1, leaving a write strobe length of 5 ns, as desired. This example assumes no margin is included.

Therefore, for the calculations below, the delay time will not be included for output signal requirements. A time t_{margin}, however, will be calculated for each of the measurements in the examples below, in order to account for any skew time, clock jitter, or slight differences in delay time. As a general constraint, the examples will require the output margin to be within 1 ns. If the necessary margin is not met, then the corresponding parameter can be increased by a cycle. This time is only a rough guideline, and for any system, the necessary margin should be determined.

For the read cycles, there are two situations that arise that require different amounts of margin. First, for the parameters that affect the input setup to the C6x, extra timing margin (~2ns) is recommended to account for the propagation of the output control/address signals from the C6x to the memory and the propagation of the data back to the C6x from the memory. For these calculations, the maximum output delay of the C6x will also be included to create a worst case calculation, since there is no canceling effect of the delay times for this situation. For the input hold time requirement of the C6x, no additional margin is required, due to the two propagation delays previously mentioned, which guarantee that hold timings are met without any additional margin added in.

It is important to realize that the recommended margins described here are only a guideline, which may apply to a well designed board with relatively short board traces. The timing margin required for any design should be verified. With the asynchronous interface, additional margin can always be created by adding additional cycles in the appropriate field.

Table 4. Recommended Timing Margin

Timing Parameter	**Recommended Margin**
Output Parameters	~1 ns
Input Setup	~2 ns
Input Hold	~0 ns

Table 5. EMIF – Input Timing Requirements (Input Data)

Timing Parameter	Definition
t_{su}	Data Setup time, read D before CLKOUT1 high
t_h	Data Hold time, read D after CLKOUT1 high

Table 6. EMIF – Output Timing Characteristics (Data, Address, Control)

Timing Parameter	Definition
t_d	Output delay time, CLKOUT1 high to output signal valid

Table 7. ASRAM –Input Timing Requirement

Timing Parameter	Definition
$t_{xw(m)}$	Time from Control/Data Signals Active to /AWE inactive
$t_{wp(m)}$	Write Pulse Width
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either Write Recovery Time or Data Hold Time
$t_{rc(m)}$	Length of the read cycle
$t_{wc(m)}$	Length of the write cycle

Table 8. ASRAM – Output Timing Characteristics

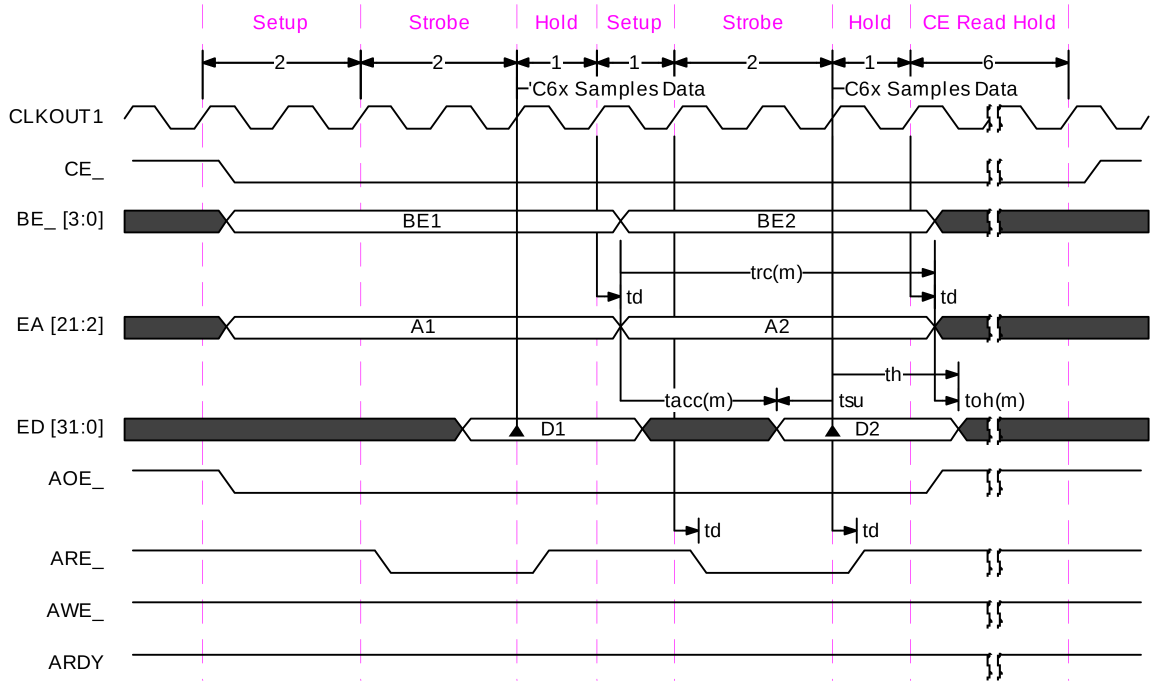
Timing Parameter	Definition
$t_{acc(m)}$	Access Time, from EA, /BE, /AOE, /CE active to ED Valid
$t_{oh(m)}$	Output Hold Time

Asynchronous Reads

Figure 4 illustrates an asynchronous read cycle with a setup/strobe/hold timing of 1/2/1. An asynchronous read proceeds as follows:

- At the beginning of the setup period
  - /CE becomes active low.
  - /AOE becomes active low.
  - /BE[3:0] becomes valid.
  - EA becomes valid.
  - For first access, setup has a minimum value of 2, after the first access setup has a minimum value of 1.
- At the beginning of a strobe period
  - /ARE is becomes active low.
- At the beginning of a hold period
  - /ARE is pulled inactive high
  - Data is sampled on the CLKOUT1 rising edge concurrent with the beginning of the hold period (end of the strobe period), just prior to the /ARE low-to-high transition.
- At the end of the hold period.
  - /AOE becomes inactive as long as another read access to the same /CE space is not scheduled for the next cycle.
- After the last access (burst transfer or single access) CE will stay active for seven minus the value of Read Hold cycles. For example, if READ HOLD = 1, then CE stays active for six more cycles. This does not affect performance but merely reflects the EMIF’s overhead.

Figure 4. Asynchronous Read Timing Example



ASYNCHRONOUS MEMORY READ TIMING (1/2/1 Timing)

Setting the Read Parameters for a Specific Asynchronous SRAM

Notice in Figure 4 that the actual timing that the C6x uses to determine when read data is valid is based on the /ARE signal. In other words, data is actually read on the rising clock edge corresponding to the cycle prior to which /ARE goes high, which is the end of the STROBE period. However, Figure 1 shows that /ARE is not connected to Asynchronous SRAM. This is being pointed out to stress the significance of the SETUP, STROBE, and HOLD times for the C6x and compare them to the significant timing parameters of actual ASRAM.

ASRAM is not synchronized to any clock, however it does have a maximum access time (t_{acc}) which relates when the output data is valid after receiving the required inputs. Thus, the data should be sampled at a time t_{acc} plus t_{su} after the inputs are valid, which, as mentioned, should correspond to the end of the strobe period.

Therefore, when defining the parameters for the C6x for SETUP, STROBE, and HOLD, the following constraints apply:

(1) $\text{SETUP} + \text{STROBE} \geq (t_{acc(m)} + t_{su} + t_{dmax})/P$

(2) $\text{SETUP} + \text{STROBE} + \text{HOLD} \geq (t_{rc(m)})/P$

(3) $\text{HOLD} \geq (t_h - t_{oh(m)})/P$

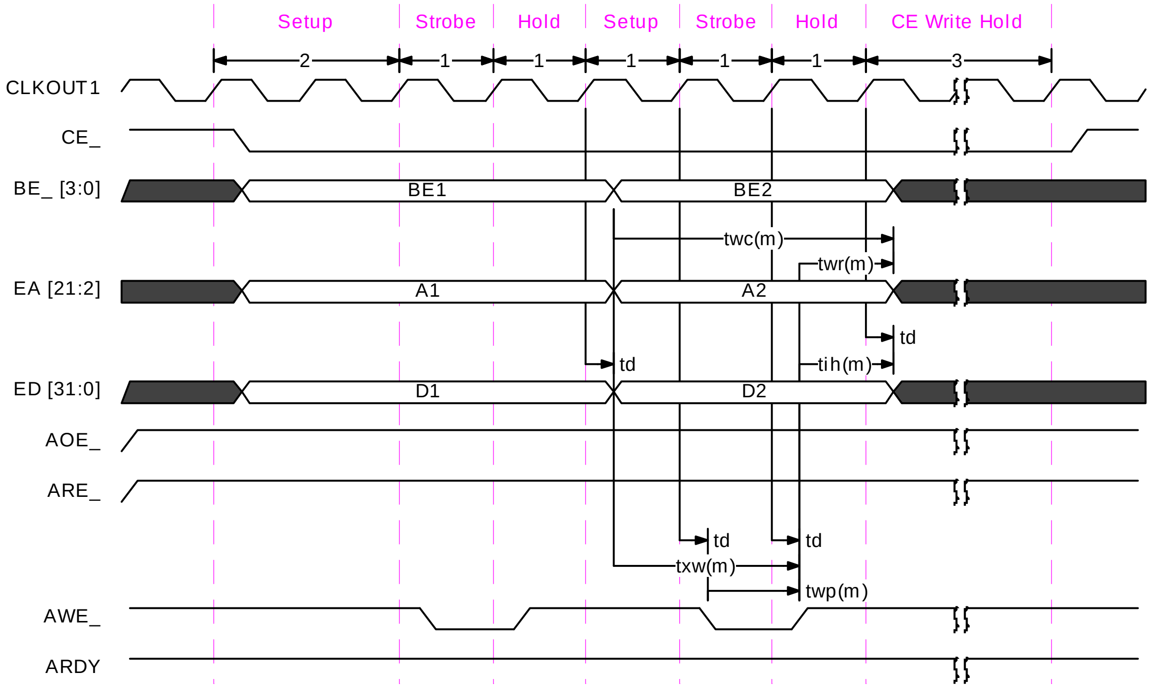
Normally, SETUP can be set to 1 cycle, then STROBE can be solved for using constraint (1). Then, HOLD can be solved for using constraint (2). Of course, the smallest value possible should be used for all three parameters to satisfy the constraints while giving the necessary timing margin, since normally speed is an important consideration when accessing memory.

Asynchronous Writes

Figure 5 illustrates back to back asynchronous write with a setup/strobe/hold of 1/1/1. An asynchronous write proceeds as follows.

- At the beginning of the setup period
  - /CE becomes active low.
  - /BE[3:0] becomes valid.
  - EA becomes valid.
  - ED becomes valid.
  - For the first access, setup has a minimum value of 2, after the first access setup has a minimum value of 1
- At the beginning of a strobe period
  - /AWE becomes active low.
- At the beginning of a hold period
  - /AWE becomes inactive high
- At the end of the hold period.
  - ED goes into the high-impedance state only if another write to the same /CE space is not scheduled for the next cycle.
  - If no write accesses are scheduled for the next cycle and write HOLD is set to 1 or greater, then CE will stay active for 3 cycles after the programmed HOLD period. If write HOLD is set to 0, then /CE will stay active for 4 more cycles. This does not affect performance, but merely reflects the EMIF’s overhead.

Figure 5. *Asynchronous Write Timing Example*



ASYNCHRONOUS MEMORY WRITE TIMING (1/1/1 Timing)

Setting the Write Parameters for a Specific Asynchronous SRAM

For an ASRAM write, the SETUP, STROBE, and HOLD parameters should be set according to the following constraints:

(3) $\text{STROBE} \geq t_{wp(m)}/P$

(4) $\text{SETUP} + \text{STROBE} \geq t_{xw(m)}\ /P$

(5) $\text{HOLD} \geq (\max(t_{ih(m)},\ t_{wr(m)}))/P$

(6) $\text{SETUP} + \text{STROBE} + \text{HOLD} \geq t_{wc(m)}/P$

Full Examples

This section will walk through the configuration steps required to implement Toshiba's TC55V1664FT-12 ASRAM and IDT's IDT71L016L70 ASRAM, which are both 64k x 16 devices, with access times of 12 ns and 70 ns respectively.

For both implementations, the following assumptions will be made :

- ☐ ASRAM will be used in address space CE0.
- ☐ CPU Clock Speed of 200 MHz, therefore P is 5 ns.
- ☐ The wiring of both parts is the same as shown in Figure 1.

Table 9. EMIF – Input Requirements

		MIN	MAX	UNIT
t_{su}	Setup time, read ED before CLKOUT1 high	5		ns
t_h	Data Hold time, read D after CLKOUT1 high	0		

Table 10. EMIF – Output Timing Characteristics

		MIN	MAX	UNIT
t_d	Output delay time, CLKOUT1 high to output signal valid	–1	5	ns

Register Configuration for Toshiba's TC55V1664FT-12

Table 11 and Table 12 summarize the timing characteristics of the TC55V1664FT-12, which will be used to calculate the values for the CE0 Space Configuration Register. This data was taken from the C6x Data Sheet and the TC55V1664FT-12 Data Sheet.

Table 11. ASRAM Input Requirements from EMIF for TC55V1664FT-12

		MIN	MAX	UNIT
$t_{xw(m)}$	Time from Control/Data Signals Active to /AWE inactive	10		ns
$t_{wp(m)}$	Write Pulse Width	8		ns
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either Write Recovery Time or Data Hold Time	0		ns
$t_{rc(m)}$	Length of the read cycle	12		ns
$t_{wc(m)}$	Length of the write cycle	12		ns

Table 12. ASRAM – Output Timing Characteristics for TC55V1664FT-12

		MIN	MAX	UNIT
$t_{acc(m)}$	Access Time, from EA, /BE, /AOE, /CE active to ED Valid		12	ns
$t_{oh(m)}$	Output Hold Time	3		

Read Calculations

- **SETUP = 1**, based on the suggestion stated in the section, Setting the Read Parameters for a Specific Asynchronous SRAM.

- $\text{SETUP} + \text{STROBE} \geq (t_{acc(m)} + t_{su} + t_{dmax})/P$

  Therefore,

  $\text{STROBE} \geq (t_{acc(m)} + t_{su} + t_{dmax})/P - \text{SETUP}$

  $\geq (12\text{ ns} + 5\text{ ns} + 5\text{ ns})/\ 5\text{ ns} -1$

  ≥ 4.4 cycles - 1 cycle = 3.4 cycles

  STROBE = 4 cycles; $t_{margin} = 3$ ns

- $\text{SETUP} + \text{STROBE} + \text{HOLD} \geq (t_{rc(m)})/P$

  Therefore,

  $\text{HOLD} \geq (t_{rc(m)})/P - \text{SETUP} - \text{STROBE}$

  $\geq (12\text{ns})/5\text{ns} - 1 - 4 = -2.6$ cycles

  HOLD = 0 cycles, since it cannot be negative;t_{margin}=13 ns

- $\text{HOLD} \geq (t_h - t_{oh(m)})/P$

  Therefore,

  $\text{HOLD} \geq (t_h - t_{oh(m)})/P$

  $\geq (0 - 3\text{ ns})/\ 5\text{ns} = -0.6$ cycles

  The previously calculated hold value satisfies this condition with $t_{margin} = 3$ ns.

With the settings specified in bold, the margin recommended is met.

Write Calculations

- STROBE $\geq (t_{wp(m)})/P$

  $\geq$ (8ns)/ 5ns = 1.6 cycles

  STROBE = 2 cycles; t_{margin} = 2 ns

- SETUP + STROBE $\geq (t_{xw(m)})/P$

  Therefore,

  SETUP $\geq (t_{xw(m)})/P$ - STROBE

  = (10ns)/5ns – 2 cycles

  = 0.0 cycles.

  SETUP = 1 cycle, minimum value;t_{margin}=5ns

- HOLD $\geq (\max(t_{ih(m)}, t_{wr(m)}))/P$

  $\geq$ (0 +)/5 ns = 0 cycles

  HOLD = 1 cycles; t_{margin} = 5 ns. The value of HOLD is extended to 1 cycle in order to provide additional timing margin.

- SETUP + HOLD + STROBE $\geq t_{wc}$

  This requirement is satisfied. The sum of the three parameters is 4 cycles, which is greater than 12 ns (2.4 cycles). t_{margin}=8 ns

Using the above calculations, the CE Space Control Register can now be properly configured. Figure 6 shows the CE0 Space Control Register with the properly assigned values for each field. MTYPE = 010 identifies the memory in this address space as 32 bit wide asynchronous memory, while the other fields are used as calculated above.

Figure 6. EMIF CE0 Space Control Register Diagram for TC55V1664FT-12

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
0001	000010	01	0001

15 14	13 8	7	6 4	3 2	1 0
Reserved	READ STROBE	rsv	MTYPE	Reserved	READ HOLD
11	000100	0	010	00	00

Sample Code

The following code segment will set up the EMIF as described above, using the TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.     /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Configure CE0 as ASRAM  */
LOAD_FIELD(&ce0_ctrl, MTYPE_32ASYNC, MTYPE       , MTYPE_SZ       );
LOAD_FIELD(&ce0_ctrl, 1            , READ_SETUP  , READ_SETUP_SZ  );
LOAD_FIELD(&ce0_ctrl, 4            , READ_STROBE , READ_STROBE_SZ );
LOAD_FIELD(&ce0_ctrl, 0            , READ_HOLD   , READ_HOLD_SZ   );
LOAD_FIELD(&ce0_ctrl, 1            , WRITE_SETUP , WRITE_SETUP_SZ );
LOAD_FIELD(&ce0_ctrl, 2            , WRITE_STROBE, WRITE_STROBE_SZ);
LOAD_FIELD(&ce0_ctrl, 1            , WRITE_HOLD  , WRITE_HOLD_SZ  );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                 sdram_ctrl, sdram_ref);
.
.     /*OTHER USER CODE*/
.
```

Register Configuration for IDT's IDT71L016L70

Table 13 and Table 14 summarize the timing characteristics of the IDT71L016L70, which will be used to calculate the values for the CE0 Space Configuration Register. This data was taken from the C6x Data Sheet and the IDT71L016 Data Sheet.

Table 13. ASRAM Input Requirements from EMIF for IDT71L016L70

		MIN	MAX	UNIT
$t_{xw(m)}$	Time from Control/Data Signals Active to /AWE inactive	65		Ns
$t_{wp(m)}$	Write Pulse Width	55		Ns
$t_{ih(m)}$, $t_{wr(m)}$	Maximum of either Write Recovery Time or Data Hold Time	0		Ns
$t_{rc(m)}$	Length of the read cycle	70		ns
$t_{wc(m)}$	Length of the write cycle	70		ns

Table 14. ASRAM – Output Timing Characteristics for IDT71L016L70

		MIN	MAX	UNIT
$t_{acc(m)}$	Access Time, from EA, /BE, /AOE, /CE active to ED Valid		70	ns
$t_{oh(m)}$	Output Hold Time	10		

Read Calculations

- ❑ **SETUP = 1**, based on the suggestion stated in the section, Setting the Read Parameters for a Specific Asynchronous SRAM.

- ❑ SETUP + STROBE $\geq (t_{acc(m)} + t_{su} + t_{dmax})/P$

  Therefore,

  $$\text{STROBE} \geq (t_{acc(m)} + t_{su} + t_{dmax})/P - \text{SETUP}$$

  $$\geq (70\text{ ns} + 5\text{ ns} + 5\text{ ns})/\ 5\text{ ns} - 1$$

  $$\geq 16\text{ cycles} - 1\text{ cycle} = 15\text{ cycles}$$

  STROBE = 16 cycles; t_{margin} = 5 ns. The value of STROBE is extended by one cycle to give the desired timing margin.

- ❑ SETUP + STROBE + HOLD $\geq (t_{rc(m)})/P$

  Therefore,

  $$\text{HOLD} \geq (t_{rc(m)})/P - \text{SETUP} - \text{STROBE}$$

  $$\geq (70\text{ns})/5\text{ns} - 1 - 16 = -3\text{ cycles}$$

  HOLD = 0 cycles, since it cannot be negative;t_{margin}=15 ns

- ❑ HOLD $\geq (t_h - t_{oh(m)})/P$

  Therefore,

  $$\text{HOLD} \geq (t_h - t_{oh(m)})/P$$

  $$\geq (0 - 10\text{ ns})/\ 5\text{ns} = -2\text{ cycles}$$

  The previously calculated hold value satisfies this condition with t_{margin} = 10 ns.

With the settings specified in bold, the margin recommended is met.

Write Calculations

❏ STROBE ≥ ($t_{wp(m)}$)/P

≥ (55ns)/ 5ns = 11 cycles

STROBE = 12 cycles; t_{margin} = 2 ns. The STROBE value is extended by one cycle to give the desired timing margin.

❏ SETUP + STROBE ≥ ($t_{xw(m)}$)/P

Therefore,

SETUP ≥ ($t_{xw(m)}$)/P - STROBE

= (65ns)/5ns – 12 cycles

= 1 cycle.

SETUP = 2 cycle;t_{margin}=5ns. The SETUP value is extended by one cycle to give the desired timing margin.

❏ HOLD ≥ (max($t_{ih(m)}$, $t_{wr(m)}$))/P

≥ (0 +)/5 ns = 0 cycles

HOLD = 1 cycles; t_{margin} = 5 ns. The value of HOLD is extended to 1 cycle in order to provide additional timing margin.

❏ SETUP + HOLD + STROBE ≥ t_{wc}

This requirement is satisfied. The sum of the three parameters is 15 cycles, which is greater than 70 ns (14 cycles). t_{margin}=5 ns

Using the above calculations, the CE Space Control Register can now be properly configured. Figure 6 shows the CE0 Space Control Register with the properly assigned values for each field. MTYPE = 010 identifies the memory in this address space as 32 bit wide asynchronous memory, while the other fields are used as calculated above.

Figure 7. EMIF CE0 Space Control Register Diagram for IDT71L016L70

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
0010	001100	01	0001

15 14	13 8	7	6 4	3 2	1 0
Reserved	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	010000	0	010	00	00

Sample Code

The following code segment will set up the EMIF as described above, using the TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.     /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Configure CE0 as ASRAM, w/ calculated timings */
LOAD_FIELD(&ce0_ctrl, MTYPE_32ASYNC, MTYPE       , MTYPE_SZ       );
LOAD_FIELD(&ce0_ctrl,  1           , READ_SETUP  , READ_SETUP_SZ  );
LOAD_FIELD(&ce0_ctrl, 16           , READ_STROBE , READ_STROBE_SZ );
LOAD_FIELD(&ce0_ctrl,  0           , READ_HOLD   , READ_HOLD_SZ   );
LOAD_FIELD(&ce0_ctrl,  2           , WRITE_SETUP , WRITE_SETUP_SZ );
LOAD_FIELD(&ce0_ctrl, 12           , WRITE_STROBE, WRITE_STROBE_SZ);
LOAD_FIELD(&ce0_ctrl,  1           , WRITE_HOLD  , WRITE_HOLD_SZ  );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                 sdram_ctrl, sdram_ref);
.
.     /*OTHER USER CODE*/
.
```

References

TMS320C6201 Digital Signal Processor Data Sheet, Texas Instruments, March 1998, Literature Number SPRS051C

TMS320C62x Peripherals Reference Guide, Texas Instruments, October 1997, Literature number SPRU190

TMS320C6x Peripheral Support Library Programmers Reference, Texas Instruments, March 1998, Literature number SPRU273

TC55V1664FT Data Sheet, Toshiba, June 1997.

IDT71L016 Data Sheet, Integrated Device Technology, July 1997.