TMS320C6201/C6701 PERIPHERAL REFERENCE GUIDE (SPRU190B) ERRATA

Internal Program Access

Page 2-6 DMA Controller Access to Program Memory

Please remove the NOTE and add the following as normal text in its place.

During HPI boot-load, the program memory controller allows both read and writes to the program memory. This allows the HPI to read back the boot code for verification, if required.

Internal Data Access

Page 3-13 Data Endianness

Please add the following after the 2nd sentence after the two bullets:

This input is latched only once when the device /RESET pin is de-asserted. Hence, the LENDIAN pin is static after device reset.

DMA Controller

Page 4-12 Initiating Block Transfer

Please modify 4th sentence under 'Pause Operation' as follows:

Once paused, STATUS = 10b only after the DMA channel has completed pending write transfers.

Please add the following as the 2nd sentence under 'Stop Operation':

In this case, STATUS = 00b after the DMA channel has completed all pending write transfers.

Page 4-20 Address Adjustment with the DMA Channel Index Registers

Section 4.7.2: Description under Element Index: 3rd line should read …

… DMA channel source or the destination address …

Page 4-34 Emulation

Last sentence in paragraph has typos: simulates, channels, multiple.

Host Port Interface

Page 5-8 Section 5.2.7

7th line from bottom:
Remove /HBE[1:0] from the third bullet.

EMIF

Page 6-7 Figure 6-3: EMIF Global Control Register Diagram

Reserved bit-fields 12, 13 should be designated as R, +0.

Page 6-8 Table 6-3: EMIF Global Control Register Description

Modify description for MAP as follows:

MAP=0; external memory is used at address 0

MAP=1; internal memory is used at address 0

Page 6-9 EMIF CE Space Control Registers

Section 6.3.2. Add after first paragraph

The MTYPE field in the CE space control register can only be set once, and should be done during system initialization. The only exception is that if CE1 is used for a ROM boot-mode, then that CE space can be configured to another asynchronous memory type.

Figure 6-4: Reserved bit-fields 14, 15 should be designated as R, +00.

Page 6-34 Hold Interface

Add a bullet with sub-bullets as follows:

❑ The HOLD/HOLDA acknowledge functionality can be controlled by the NOHOLD bit in the EMIF Global Control Register and affects the operation as follows:

❑ If NOHOLD is not set and a HOLD request comes in, the C6x will flush all current accesses, perform an urgent refresh if SDRAM is in the system, give up the I/O bus, and assert HOLDA. When HOLD is then de-asserted by the external requestor, HOLDA will be de-asserted, the C6x will regain the bus and will immediately perform an urgent refresh if SDRAM is in the system before continuing with normal operation.

❑ If NOHOLD is set and a HOLD request is detected, the C6x will ignore the HOLD request. If while the Hold request is still asserted, the NOHOLD bit is then de-asserted, the HOLD will be acknowledged as above.

❑ If NOHOLD is not set and a hold request comes in and after granting the external device the bus as above, and software then sets the NOHOLD bit, then the NOHOLD bit is ignored until the current HOLD request is removed by the external requestor.

Boot Configuration

Page 7-6 Boot Processes

Please remove the NOTE and add the following under HPI boot process:

During HPI boot-load, the program memory controller allows both read and writes to the program memory. This allows the HPI to read back the boot code for verification, if required.

McBSP

Page 8-50 Figure 8-37: Sample Rate Generator

The output of the mux should be called CLKSRG. This drives the CLKGDV divider stage.

Page 8-52 Table 8-13

Replace the last sentence under Function for CLKGDV as follows:

Valid value: 0 to 255.

Power Down Logic

Page 11-2 Overview

Fig. 11-1: Power-Down Mode Logic

All OR gates associated with PD1, PD2, and PD3 should be replaced with AND gates.

PD output via NOR gate should be replaced with OR gate.