TMS320C54x, TMS320LC54x Datasheet Addendum

(Timing Information for '548/'549)

This addendum is to provide preliminary 80 and 100 MIPS timing data to the existing LC54x datasheet (SPRS039A). The page number references are only valid to the data sheet revised in April 1997.

Timing
Operating conditions

Recommended operating conditions

	'54x-80		'54x-100		Unit
	Min Max	Typ	Min Max	Typ	
Vdd	3.0 3.6	3.3	3.0 3.6	3.3	**V**
Vcc	3.0 3.6	3.3	2.38 2.62	2.5	**V**

Internal divide by two with external crystal (page 65)

recommended operating conditions

	'54x-80		'54x-100		Unit
	Min Max	Nom	Min Max	Nom	
fx Input clock frequency	0	160	0	200	MHz
C1,C2		10		10	pF

External divide-by-two clock option (Page 66)

The divide by two option at over 50 MIPS should be avoided.

External multiply by N clock option (Page 67)

Switching characteristics over recommended operating conditions

			'54x-80			'54x-100			Unit
			Min	Typ	Max	Min	Typ	Max	
$t_{c(CO)}$	Cycle time, CLKOUT		125	$2t_{c(CI)/N}$		10	$t_{c(CI)/N}$		ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN low to CLKOUT high	N= 1, 2, 3, 4, 5, 9	*	*	*	*	*	*	ns
$t_{d(CIH-CO)}$	Delay time, X2/CLKIN low to CLKOUT high	N= 1.5, 2.5, 4.5	*	*	*	*	*	*	ns
$t_{f(CO)}$	Fall time, CLKOUT			2			2		ns
$t_{r(CO)}$	Rise time, CLKOUT			2			2		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low		H-3	H-1	H	H-2	H-1	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high		H-3	H-1	H	H-2	H-1	H	ns
t_p	PLL lock-up time				50			50	ns

- **will be defined after characterization**

Timing requirements over recommended operating conditions

	'54x-80	'54x-100	

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			Min	Max	Min	Max	Unit
$t_{c(CI)}$	Cycle time, X2/CLKIN	N=1, 2, 3, 4, 5, 9	10N	200N	10N	200N	ns
		N=1.5, 2.5, 4.5	10N	200N	10N	200N	
$t_{f(CI)}$	Fall time, X2/CLKIN			2		2	ns
$t_{r (CI)}$	Rise time, X2/CLKIN			2		2	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low		3		2		ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high		3		2		ns

Memory read timings (Page 69)

Switching characteristics over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	0	4	0	3	ns
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high (transition)	0	4	0	3	ns
$t_{d (CLKL-MSL)}$	Delay time, MSTRB low from CLKOUT low	0	4	0	3	ns
$t_{d (CLKL-MSH)}$	Delay time, MSTRB high from CLKOUT low	-2	2	-2	2	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low	0	4	0	3	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high	0	4	0	3	ns

Timing requirements over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{a(A)M}$	Access time, read data access from address valid		2H-7.5		2H-5	ns
$t_{a(MSTRBL)}$	Access time, read data access from MSTRB low		2H-7.5		2H-5	ns
$t_{su (D)R}$	Setup time, read data before CLKOUT low	2		2		ns
$t_{h(D)R}$	Hold time, read data after CLKOUT low	0		0		ns
$t_{h(A-D)R}$	Hold time, read data after address invalid	0		0		ns
$t_{h(D)MSTRBH}$	Hold time, read data after MSTRB high	0		0		ns

Memory write timings (Page 71)

Switching characteristics over recommended operating conditions

		'54x-100		'54x-100		Unit
		Min	Max	Min	Max	
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high	0	4	0	3	ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low (transition)	0	4	0	3	ns
$t_{d (CLKL-MSL)}$	Delay time, MSTRB low from CLKOUT low	0	4	0	3	ns
$t_{d(CLKL-D)W}$	Delay time, data valid from CLKOUT low		5		3	
$t_{d (CLKL-MSH)}$	Delay time, MSTRB high from CLKOUT low	-2	2	-2	2	ns
$t_{d(CLKH-RWL)}$	Delay time, R/W low from CLKOUT high	0	4	0	3	ns
$t_{d(CLKH-RWH)}$	Delay time, R/W high from CLKOUT high	-2	2	-2	2	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high	0	3	0	3	ns

Timing requirements over recommended operating conditions

		'54x-80	'54x-100	

		Min	Max	Min	Max	Unit
$t_{h(D)MSH}$	Hold time, write data valid after MSTRB high	H-5	H+5	H-2	H+2	ns
$t_{w(SL)MS}$	Pulse duration MSTRB low	2H-5		2H-3		ns
$t_{su(A)W}$	Setup time, address valid before MSTRB low	2H-5		2H-3		ns
$t_{su(D)MSH}$	Setup time, write data valid before MSTRB high	2H-7	2H+7	2H-5	2H+5	ns

I/O read timings (Page 73)

Switching characteristics over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	0	4	0	3	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, IOSTRB low from CLKOUT high	0	4	0	3	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, IOSTRB high from CLKOUT high	-2	2	-2	2	ns
$t_{h(A)IOR}$	Hold tiem, address after CLKOUT low	0	4	0	3	ns

Timing requirements over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{a(A)IO}$	Access time, read data access from address valid		3H-5		3H-3	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from IOSTRB low		3H-5		3H-3	ns
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	4		4		ns
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	0		0		ns
$t_{h(ISTRBH-D)R}$	Hold time, read data after IOSTRB high	0		0		ns

I/O write timings (Page 75)

Switching characteristics over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	0	4	0	3	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, IOSTRB low from CLKOUT high	0	4	0	3	ns
$t_{d(CLKH-D)IOW}$	Delay time, write data valid from CLKOUT high	H-5	H+5	H-5	H+3	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, IOSTRB high from CLKOUT high	-2	2	-2	2	ns
$t_{d(CLKL-RWL)}$	Delay time, R/W low from CLKOUT low	0	4	0	3	ns
$t_{d(CLKL-RWH)}$	Delay time, R/W high from CLKOUT low	-2	2	-2	2	ns
$t_{h(A)IOW}$	Hold time, address valid from CLKOUT low	0	4	0	3	ns

Timing requirements over recommended operating conditions

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{h(D)IOW}$	Access time, read data access from address valid	H-4	H+4	H-3	H+3	ns
$t_{su(D)IOSTRBH}$	Access time, read data access from IOSTRB low	2H-7	2H+7	2H-3		ns
$t_{su(D)IOSTRBL}$	Setup time, read data before CLKOUT high	2H-5		2H-3		ns

READY timing for externally generated wait states (Page 79)

Timing requirements over recommended operating conditions

		'54x-80		'54x-100		Unit

PRELIMINARY

		Min	Max	Min	Max	
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	6		5		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after MSTRB low		4H-12		4H-8	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after MSTRB low	4H		4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after IOSTRB low		5H-12		5H-8	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after IOSTRB low	5H		5H		ns
$t_{v(MSCL)}$	Valid time, MSC low after CLKOUT low	0	4	0	3	ns
$t_{v(MSCH)}$	Valid time, MSC high after CLKOUT low	-2	2	-2	2	ns

HOLD and HOLDA timings (Page 83)

No change from -66. But, need to be reconsidered the of tsu(hold) min after characterization.

RESET,BIO, interrupt, and MP/MC timings.

		'54x-80		'54x-100		Unit
		Min	Max	Min	Max	
$t_{h(RS)}$	Hold time, RS after CLKOUT low	0		0		ns
$t_{h(BIO)}$	Hold time, BIO after CLKOUT low	0		0		ns
$t_{h(INT)}$	Hold time, INTn, NMI, after CLKOUT low	0		0		ns
$t_{h(MPMC)}$	Hold time, MP/MC after CLKOUT low	0		0		ns
$t_{w(RSL)}$	Pulse duration, RS low	4H+7		4H+5		ns
$t_{w(BIO)S}$	Pulse duration, BIO low, synchronous	2H+7*		2H+5*		ns
$t_{w(BIO)A}$	Pulse duration, BIO low, asynchronous	4H		4H		ns
$t_{w(INTH)S}$	Pulse duration, INTn, NMI high (synchronous)	2H+7		2H+7		ns
$t_{w(INTH)A}$	Pulse duration, INTn, NMI high (asynchronous)	4H		4H		ns
$t_{w(INTL)S}$	Pulse duration, INTn, NMI low (synchronous)	2H+7*		2H+7*		ns
$t_{w(INTL)A}$	Pulse duration, INTn, NMI low (asynchronous)	4H		4H		ns
$t_{w(INTL)WKP}$	Pulse duration, INTn, NMI low for IDLE2/IDLE3 wakeup	10		8		ns
$t_{su(RS)}$	Setup time, RS before X2/CLKIN low	5		5		ns
$t_{su(BIO)}$	Setup time, BIO before CLKOUT low	10*		8*		ns
$t_{su(INT)}$	Setup time, INTn, NMI, RS before CLKOUT low	10*		8*		ns
$t_{su(MPMC)}$	Setup time, MP/MC before CLKOUT low	10*		8*		ns

* Need to be re-considered after characterization

BSP timings (Page 92-98)

No change from "-66's". But, need to redefine the value of all BSP timings after characterization

HPI timings (Page 99-104)

No change from "-66's". But, need to redefine the value of all HPI timings after characterization

PRELIMINARY