TMS320C6201 Power Consumption Summary

APPLICATION REPORT: PRELIMINARY

Kyle Castille
June 26, 1998

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

Contents

Tables

TMS320C6201 Power Consumption Summary

Abstract

This document discusses the power consumption of the TMS320C6201 (Revision 2.1) for typical applications and presents an estimate for the power consumption of the TMS320C6201B[1] (Revision 3.0.)

[1] For more information on the differences between the TMS320C6201 and the TMS320C6201B, refer to “TMS320C6201 (revision 2.x) to TMS320C6201B (revision 3.x) Migration Document”

Activity Level Models

'C6201 power consumption can be modeled with two levels of activity – High DSP Activity and Low DSP Activity. Based on weighted averages of the two, a fairly accurate representation of an application's power consumption can be predicted.

Table 1. Definition of Activity Levels

	CPU Activity Level	Program Memory Access Rate	Data Memory Access Rate	I/O 100MHz Ext. Mem 30pf load
High DSP Activity	8 instr.	100%	75%	100% Access
75% High, 25% Low				
50% High, 50% Low				
Low DSP Activity	2 instr.	25%	25%	0% Access

Table 1 shows the characteristics associated with high DSP activity and low DSP activity. High DSP activity represents a FIR, FFT, or other fully optimized algorithm. Low DSP activity represents the time spent setting up registers or executing other less optimized code segments.

The actual code used to model the activity levels is described in detail in Table 2.

Table 2. Activity Level Model Representation

Module	High DSP Activity	Low DSP Activity
CPU	8 instructions/cycle, with 2 LDH instructions	2 instructions/cycle, with 1 LDH instruction
Program Memory	100% = 1 Fetch Packet/ Cycle	25 % = 1 Fetch Packet / 4 Cycles
DMA/EMIF	50/50 transfer to/from 1/2x SBSRAM	Fully servicing McBSP
Data Memory	75 % = 32 bits/cycle via CPU LDH instructions, 32 bits/2 cycle via DMA transactions	25% = 16 bits/cycle via CPU LDH instruction
I/O	32 bits/cycle @ 100 MHz	None
McBSP	2 channels @ E1 Rate	2 channels @ E1 Rate
Timers	2 timers @ Max Rate (1/8 CPU Clock)	2 timers @ Max Rate (1/8 CPU Clock)

Real world applications typically spend between fifty and seventy-five percent of their time performing high DSP activity and the remainder of their time performing low DSP activity. The 75% High/25% Low and 50% High/50% Low categories are representative of these applications. Depending on the particular application, an estimate of the ratio of high/low activity must be made in order to predict power consumption.

Power Measurement/Estimate Results

The following tables show the actual measured power consumption for the Revision 2.1 device and the estimated power consumption for the 'C6201B device. The measurements reveal that the power consumption of the 'C6201 is linear versus frequency. Therefore, the tables report the results as Current/Frequency. The corresponding power consumption can be found by simply multiplying the Current/Frequency by the desired frequency of operation and by the nominal operating voltage.

The Revision 2.1 device is a 0.25 micron device, operating with a core voltage of 2.5 V. The 'C6201B device is a 0.18-micron device with a core voltage of 1.8 V. The 'C6201B will operate with substantially lower power consumption. This is based on several factors, but the most significant reasons for the dramatic power reduction are:

1) Reduced core voltage

2) Improved Low Power RAM cell.

Table 3. Current Consumption by C6201 Modules

		High DSP Activity				Low DSP Activity			
		Revision 2.1		'C6201B		Revision 2.1		'C6201B	
		mA/MHz	% of Supply	mA/MHz	% of Supply	mA/MHz	% of Supply	mA/MHz	% of Supply
VDD2 Current Consumption									
CPU	CPU	2.16	13.5%	1.47	31.9%	1.06	12.4%	0.72	27.5%
CPU	CPU Memory Access	7.70	48.1%	0.76	16.4%	3.22	37.6%	0.30	11.4%
CPU	Clocking	4.10	25.6%	1.47	31.9%	4.10	47.8%	1.47	56.2%
CPU Total		13.96	87.3%	3.70	80.3%	8.38	97.8%	2.49	95.1%
Peripherals	DMA/EMIF	0.40	2.5%	0.47	10.2%	0.15	1.8%	0.10	3.9%
Peripherals	DMA Memory Access	1.60	10.0%	0.10	2.2%	0.00	0.0%	0.00	0.0%
Peripherals	Other	0.04	0.3%	0.33	7.2%	0.04	0.5%	0.03	1.0%
Peripherals Total		2.04	12.8%	0.91	19.7%	0.19	2.2%	0.13	4.9%
Core Current Total		16.00	100.0%	4.61	100.0%	8.57	100.0%	2.62	100.0%
VDD3 Current Consumption									
I/O Current Total		0.89	100.0%	0.89	100.0%	0.45	100.0%	0.45	100.0%

Table 4. Power Consumption for Typical DSP Activity

	50% High/50% Low		75% High/25% Low		units
	Rev 2.1	C6201B	Rev 2.1	C6201B	
CPU w/ Memory Access	11.17	3.10	12.57	3.40	ma/MHz
Peripherals	1.12	0.52	1.58	0.71	ma/MHz
I/O	0.67	0.67	0.78	0.78	ma/MHz

Table 3 and Table 4 detail the power consumption of each of the major blocks of the ‘C6201, both at High DSP Activity and Low DSP Activity. The Revision 2.1 numbers are actual measured numbers, and the ‘C6201B numbers are estimates based on simulation data. These tables illustrate the superior power characteristics of the TMS320C6201B device.

I/O provides an additional power saving opportunity. If most code and data can be stored in internal memory, thus reducing the required I/O, then the ‘C6201B power consumption can be further reduced. In addition, all test measurements were based on a worst case load (30 pF). With less load, the I/O power consumption would reduce accordingly.

The numbers reported above in Table 3 and Table 4 can be used directly to estimate the power consumption for either the Revision 2.1 device or the C6201B. For example, in order to compute power consumption of the C6201B at 50% High DSP Activity and 50% Low DSP Activity, the current/MHz rating must be multiplied by the supply voltage and by the desired operating frequency. Therefore,

*Power = ((CPU Current/Freq + Peripheral Current/Freq) * Core Supply Voltage + IO Current/Freq * IO Supply Voltage) * Operating Frequency*

= ((3.1mA/MHz + 0.52mA/MHz) 1.8V + 0.67mA/MHz * 3.3V) * 200MHz*

= ~ 1.75 Watts

Another common point for comparison in the DSP industry is the power consumption due to CPU and internal memory accesses. For the C6201B, this can be found at 50% High DSP Activity and 50% Low DSP Activity as:

*CPU Power = CPU Current/Freq * Core Supply Voltage * Operating Frequency*
*= 3.1 mA/MHz * 1.8 V * 200 MHz*
= ~ 1.1 W

The calculation for the Revision 2.1 device is identical. The only thing to note is that the core voltage between the two devices is different. For Revision 2.1, a core voltage of 2.5 V should be used, and for C6201B, 1.8 V should be used.

Table 5. Low Power Modes

	Rev 2.1	'C6201B	units
Idle	11.75	5.9	mW/MHz
PD1	8.75	5.15	mW/MHz
PD2	< 0.5	< 0.4	mW/MHz
PD3	< 0.5	< 0.4	mW/MHz

Table 5 reports the power consumption of the C6201 for several special operating conditions. IDLE is an instruction which is comparable to executing continuous NOPs. The advantage with the IDLE instruction is that Program Fetches do not occur until an interrupt occurs. The other power down modes (PD1, PD2, PD3) enable and disable the clock at different portions of the 'C6201. These low power modes are the optimal way of saving power during pauses in an application.

Conclusion

The TMS320C6201 is a high performance DSP that offers a superior price to performance ratio. The TMS320C6201B is poised to improve this price to performance ratio as well as giving a significantly superior performance to power ratio.