TMS320C6201/6701 Host Port Interfaces to Popular Hosts and PCI Bridge Chips

APPLICATION REPORT: PRELIMINARY

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TEXAS INSTRUMENTS

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TRADEMARKS

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TMS320C6201/6701 Host Port Interfaces to Popular Hosts and PCI Bridge Chips.

Abstract

The Host Port Interface is a 16-bit parallel port used to interface a host processor to a 'C6201/6701 DSP. The host device functions as a master to the interface, which increases its ease of access.

This document will describe the:

❑ HPI signals and registers

❑ Interface between various host processors (TI 'C6201/6701 Motorola MC68302, Motorola MC68360, PowerPC MPC750, Motorola MPC860, Intel 80960Rx, Intel 80960Jx), PCI bridge chips (PLX PCI9050) and HPI of a 'C6201/6701 device. This includes a schematic showing connections between the two devices and verification that timing requirements are met for each device (tables and timing diagrams).

Overview of Host Port Interface

The host-port interface (HPI) is a 16 bit wide parallel port through which a host processor can directly access the CPU's memory space. Connectivity to the CPU's memory space is provided through the DMA controller. Dedicated address and data registers not accessible to the CPU connect the HPI to the DMA auxiliary channel that connects the HPI to the CPU's memory space.

Figure 1 shows a simplified diagram of host interface to the HPI.

Figure 1.   HPI Block Diagram
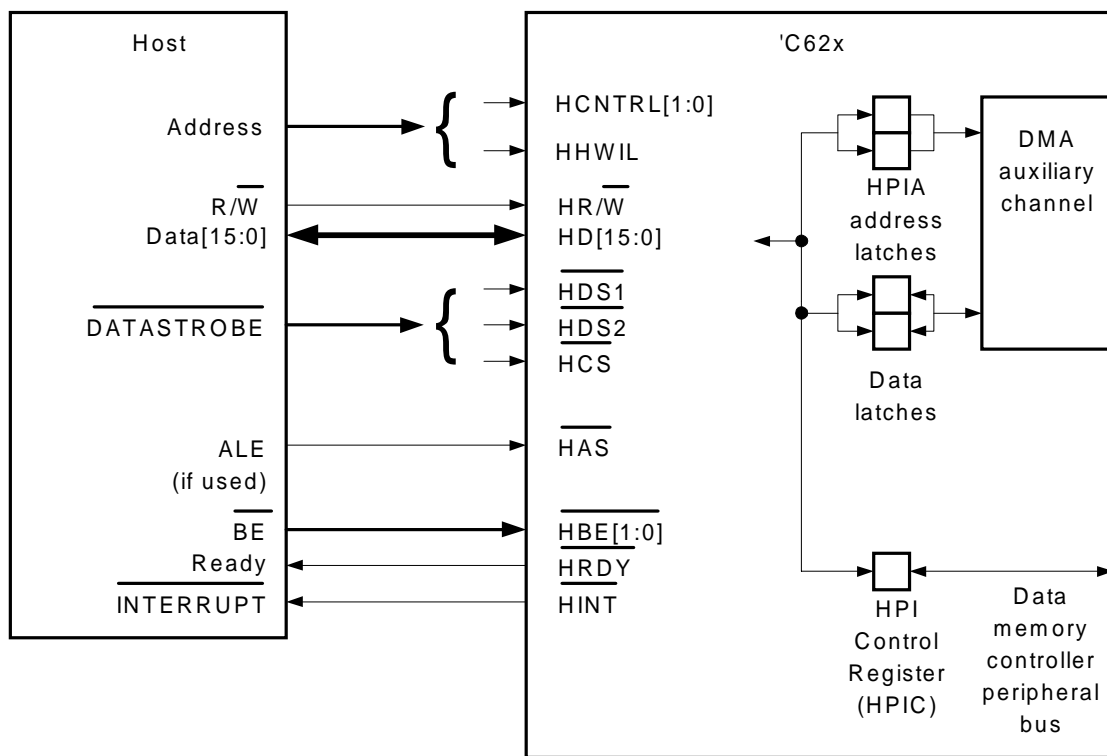
The HPI provides 32-bit data to the CPU with an economical 16-bit external interface by automatically combining successive 16-bit transfers.

The external HPI interface consists of the HPI data bus and control signals that configure and control the interface. The interface can connect to a variety of host devices with little or no additional logic.

HPI Signal Description

The external HPI interface signals implement a flexible interface to a variety of host devices. Table 1 lists the HPI pins and their functions.

Table 1.   External Interface Signals

Signal Name	Signal Type (I/O/Hi-Z)	Signal Count	Host Connection	Signal Function
HD[15:0]	I/O/Hi-Z	16	Data Bus.	
HCNTL[1:0]	I	2	Address or control lines.	Controls HPI access type.
HHWIL	I	1	Address or control lines.	Half-word identification input.
HAS-	I	1	Address Latch Enable (ALE) or address strobe or unused (tied high).	Differentiates address versus data values on multiplexed address/data host.
HBE[1:0]-	I	2	Byte enables.	Data write byte enables for TMS320C6201/6701.
HR/W-	I	1	Read/write strobe, address line, or multiplexed address/data.	Read/Write select.
HCS-	I	1	Address or control lines.	Data strobe inputs.
HDS1- HDS2-	I I	2	Read strobe and write strobe or data strobe.	Data strobe inputs.
HRDY-	O	1	Asynchronous ready.	Ready status of current HPI access.
HINT-	O	1	Interrupt input.	Interrupt signal to host.

The 16-bit data bus (HD0-HD15) exchanges information with the host. Because of the 32-bit word structure of the chip architecture, all transfers with a host consist of two consecutive 16-bit half-words. On host data (HPID) write accesses, the HBE[1:0]- byte enables select which bytes in a 32-bit accesses should be written.

HCNTL[1:0] indicate which internal HPI register is being accessed. The states of these two pins select access to the HPI address (HPIA), HPI data (HPID), or HPI control (HPIC) registers. Additionally, the HPID register can be accessed with an optional automatic address increment.

HPIA, HPIC, and HPID read accesses are performed as 32-bit accesses, and the byte enables are not used. The dedicated HHWIL pin indicates whether the first or second half-word is being transferred. An internal control register bit determines whether the first or second half-word is placed into the most significant half-word of a word.

The two data strobes (HDS1- and HDS2-), the read/write select (HR/W-), and the address strobe (HAS-) enable the HPI to interface to a variety of industry standard host devices with little or no additional logic. The HPI can easily interface to hosts with a multiplexed or dedicated address/data bus, data strobe and a read/write strobe, or two separate strobes for read and write.

Regardless of HDS connections, the HR/W- is still required to determine direction of transfer.

Used together, HCS-, HDS1- and HDS2- generate an active-low internal HSTRB- signal.

HSTRB- is used for three purposes:

1) On a read, the failing edge of HSTRB- initiates HPI read accesses for all access types.

2) On a write, its rising edge initiates HPI write accesses for all access types.

3) Falling edges latch HPI control inputs including: HHWIL, HR/W-, and HCNTL[1:0].

Additionally, HCS- gates HRDY- output.

HAS- allows HCNTL[1:0]- to be removed earlier in an access cycle, which allows more time to switch bus states from address to data information. This feature facilitates interface to multiplexed address and data type buses. In this type of system, an ALE signal is often provided and would normally be the signal connected to HAS.

The HPI ready pin (HRDY-) allows insertion of host-wait states. Wait-states may be necessary depending on latency to the point in the memory map accessed via the HPI as well as on the rate of host access. When low, HRDY- indicates that the HPI is ready for a transfer to be performed. Signal HRDY- is enabled by the HCS- (HRDY- is always low when HCS- is high). When HCS- becomes valid, on the first half-word transfer, HRDY- may indicate that HPI is busy completing the internal portion of a previous HPI request. Previous requests include a read from HPID with auto-increment or a write to HPID. When host performs a read access from HPID without auto-increment, the HPI sends the read request to the DMA auxiliary channel, and HRDY- becomes high. This event occurs with the first falling edge of HSTRB-. HRDY- remains high until the DMA auxiliary channel loads the requested data into HPID. At the beginning of the second read access the data is already present in HPID (DMA auxiliary channel performs word reads). Thus, the second half-word HPID read will never encounter a not ready condition and HRDY- will remain low. In case of HPID read access with auto-increment, the data pointed to by the next address is fetched immediately after the completion of the current read. Therefore, after the second half-word transfer of the current read (with the second rising edge of HSTRB-), HRDY- will become high again indicating that HPI is busy pre-fetching data. During a HPID write access two half-word portions of the HPID are transferred from the host. At the end of this write access HRDY- will become high (with the second rising edge of HSTRB-), and HPID is transferred as a 32-bit word to the address specified by HPIA. Reading or writing to HPIC or HPIA does not affect HRDY- signal.

The host and the CPU can interrupt each other using bits in the HPIC register. The CPU can send an active low interrupt condition on HINT- signal by writing to the HINT bit in the HPIC (DSP to Host interrupt). The HINT bit is inverted and tied directly to the HINT- pin. The CPU can set HINT- active low by writing HINT=1. The host can clear the HINT- to inactive-high bit by writing DSPINT=1. This bit is driven inactive-high when the chip is being reset.

HPI Registers

Table 2 summarizes the three registers that the HPI utilizes for communication between the host device and the CPU.

Table 2.   HPI Input Control Signals Function Selection Descriptions

HCNTL1	HCNTL0	Description
0	0	Host can read or write the HPI control register, HPIC.
0	1	Host can read or write the address register, HPIA.
1	0	Host can read or write HPID. HPIA is post-incremented by a word address (4 bytes).
1	1	Host can read or write HPID. HPIA is not affected.

The HPI and CPU can access the HPI control register (HPIC). The host can access the host address register (HPIA) and host data register (HPID) as well as the HPIC using external data and interface control signals.

Table 3 summarizes the three registers that the HPI utilizes for communication between the host device and the CPU. The HPIC is normally the first register accessed when setting configuration bits and initializing the interface. HPID contains the data that was read from the HPI memory if the current access is a read, or the data that will be written to HPI memory if the current access is a write. HPIA contains the address in the HPI memory at which the current access occurs. As this address is a 30-bit word address, the bottom two bits are unaffected by HPIA writes and are always read as 0.

Table 3.   HPI Register Description

Register Acronym	Register Name	Host Read/Write	CPU Read/Write	CPU Read/Write (Hex Byte Address)
HPID	HPI Data	RW	-	-
HPIA	HPI Address	RW	-	-
HPIC	HPI control	RW	RW	0188 0000h

HPI Bus Access

Figure 2 and Figure 3 show HPI access timing for the cases when HAS is and is not used.

Figure 2.   HPI Timing Diagram Using HAS

HPI Read Timing HAS Used

HPI Write Timing HAS Used
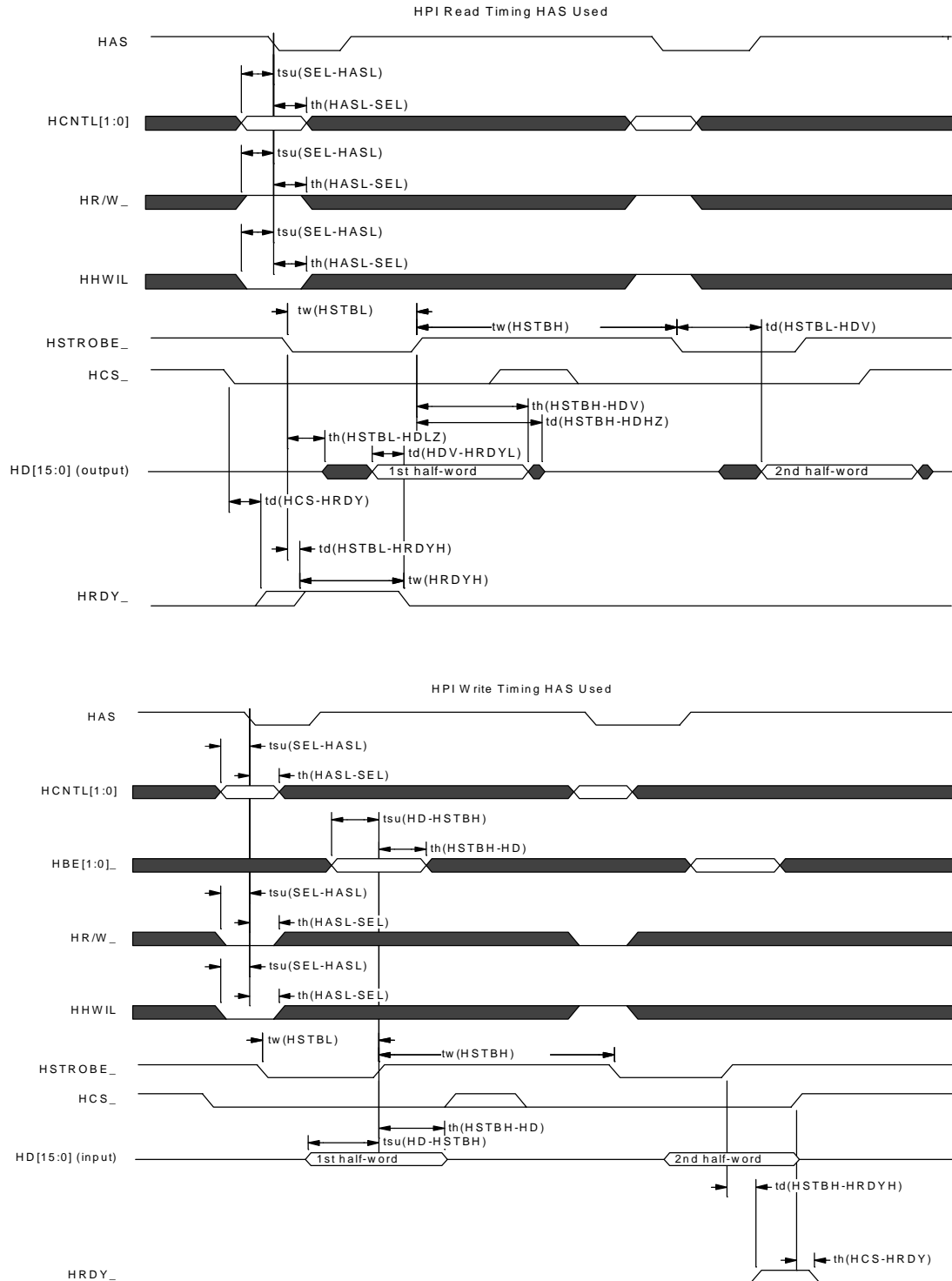
Figure 3. HPI Timing Diagram Not Using HAS
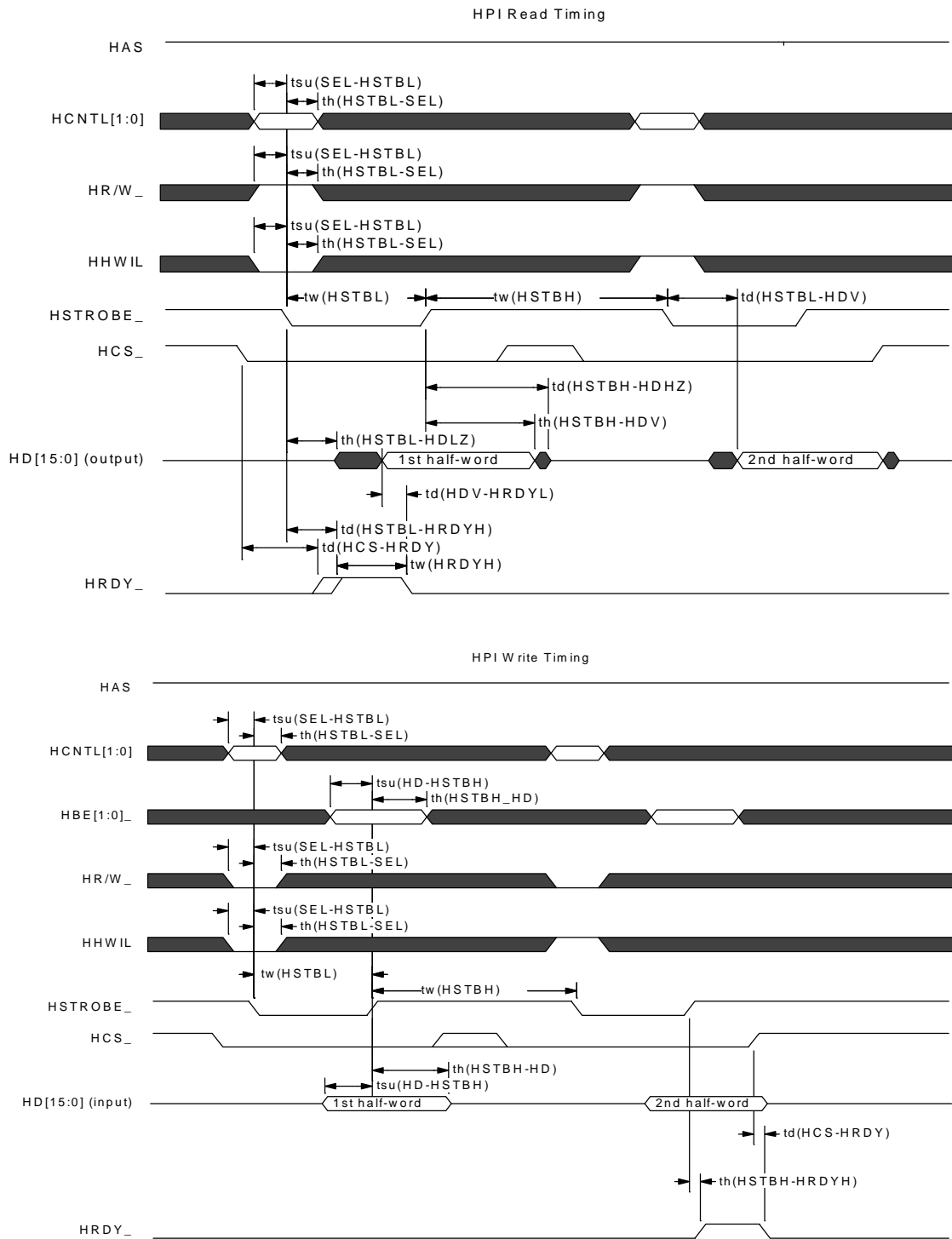
In Figures 2 and 3 timing parameters are named in the same way as in the TMS320C6201/6701's data-sheet.

Example Interfaces

The following summarize various host/HPI interfaces. Please refer to the host microprocessor's documentation for the host configuration explanation.

TMS320C6201 Processor

TMS320C6201/6701 Interface

Figure 4 shows diagram of the host (TMS320C6201/6701) interface to the HPI.

Figure 4.   TMS320C6201/6701 to HPI Interface Block Diagram
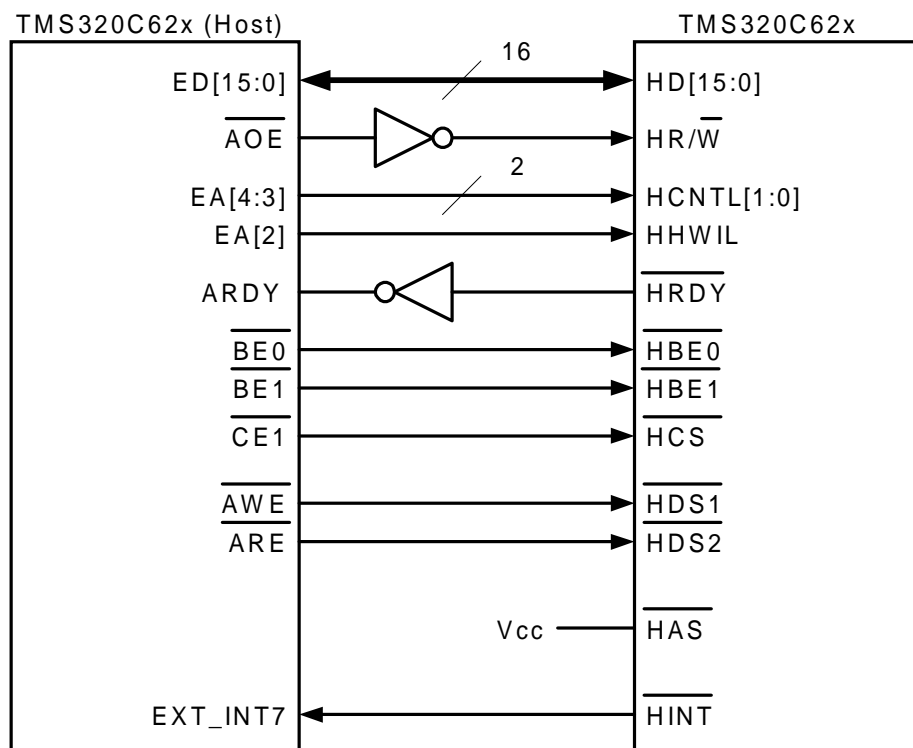
Table 4.   *TMS320C6201/6701 to HPI Pin Connections*

HPI Pin	TMS320C6201/6701 Pin	Comments
HCNTL[1:0]	EA[4:3]	EA[4:3] Control HPI access type.
HHWIL	EA2	EA2 identifies the first or second half-word of transfer.
HR/W-	Externally inverted AOE-	Output-enable (AOE-) line is inverted and connected to HR/W- to decode reads and writes.
HD[15:0]	ED[15:0]	16 LSBs of data.
HDS1-	AWE-	Since the EMIF asynchronous interface has separate read and write strobes that are by nature mutually exclusive, these are tied to HDS1-, and HDS2-.
HDS2-	ARE-	See above.
HAS-	Vcc	Unused.
HCS-	CE1-	Although any CE space can be used CE1 is chosen since it has the additional ability to perform 16-bit wide reads to asynchronous memory.
HBE0-	BE1-	C6201/C6701 HPI uses this value on writes only.
HBE1-	BE2-	C6201/C6701 HPI uses this value on writes only.
HRDY-	ARDY	Asynchronous ready input.
HINT-	INT7-	Any external interrupt INT7:4 can be chosen. INT7 is used as an example.

Externally inverted the AOE- pin is connected to HR/W- in order to selects between read and write. EA[4:3] select the type of access with HCNTL[1:0]. The Host 'C6201/6701 performs word writes, to the EMIF (Only ED[15:0] are connected to the HPI). For writes, EA5 is equivalent to logical addresses A5, and EA[4:3] correspond to A[4:3], as expected.

For reads, EMIF CE1 space of the host can be configured to 16-bit or 32-bit wide ROM.

If the host's CE1 memory space is configured to perform 16-bit wide read access then before being presented on the EA pins the logical address is shifted up by 1. The EMIF always reads the lower addresses first and packs these into the LSBytes and pack subsequent accesses into the higher order bytes. Thus, the expected packing format in ROM is always little endian, regardless of the value of the LENDIAN bit.

Table 5 shows the EMIF memory mapping in case when CE1 memory space of the host is configured as 16 bit wide ROM. AOE is used as the read/write select.

Table 5. *TMS320C6201/6701 to HPI Interface Host Memory Mapping (CE1 memory space of the host is configured to perform 16 bit wide reads).*

Host Address (Map 0)	EA4 (HCNTL1)	EA3 (HCNTL0)	EA2 (HHWIL)	HPI Action
	TMS320C6201/6701 Host Address **Little Endian**			
1000 0000	0	0	0	HPIC Read 1st half-word.
1000 0002	0	0	1	HPIC Read 2nd half-word.
1000 0004	0	1	0	HPIA Read 1st half-word.
1000 0006	0	1	1	HPIA Read 2nd half-word.
1000 0008	1	0	0	HPID Read 1st half-word with Auto-increment.
1000 0010	1	0	1	HPID Read 2nd half-word with Auto-increment.
1000 000C	1	1	0	HPID Read 1st half-word without Auto-increment.
1000 000E	1	1	1	HPID Read 2nd half-word without Auto-increment.
1000 0000	0	0	0	HPIC Write 1st half-word.
1000 0004	0	0	1	HPIC Write 2nd half-word.
1000 0008	0	1	0	HPIA Write 1st half-word.
1000 000C	0	1	1	HPIA Write 2nd half-word.
1000 0010	1	0	0	HPID Write 1st half-word with Auto-increment.
1000 0014	1	0	1	HPID Write 2nd half-word with Auto-increment.
1000 0018	1	1	0	HPID Write 1st half-word without Auto-increment.
1000 001C	1	1	1	HPID Write 2nd half-word without Auto-increment.

If the host's CE1 memory space is configured to perform 32-bit wide reads then upper 16 bits of each read has to be discarded (only ED[15:0] are connected to the HPI).

Configuration

The HPI is mapped into the CE1 memory space of the host. Configuration of CE1 space control register of the host, is shown in Table 6.

Table 6.   EMIF CE1 Space Control Register

Write setup				Write strobe						Write hold		Read setup			
31			28	27					22	21	20	19			16
0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	1

rsv		Read Strobe						rsv	MTYPE			rsv		Read hold	
15	14	13					8	7	6		4	3	2	1	0
X	X	0	0	0	1	0	1	X	0	0	1	X	X	0	1

The CE1 memory space of the Host is configured to 16-bit wide ROM (MTYPE=1) (another option would be to use MTYPE=2, to configure CE1 to 32-bit wide ROM). The data transfer speed directly depends on the HRDY- signal timing. The host is sampling the HRDY- signal with an internal delay of two cycles. Therefore, to ensure that the correct HRDY- value is sampled during a write the WRITE STROBE and WRITE SETUP are set to 3. During a read, in order to guarantee that the data is valid before the rising edge of CLCKOUT1 the READ STROBE is set to 5 (to meet data setup time tsu(ED-CK1H) requirement).

The external interrupt polarity register allows you to change the polarity of the four external interrupts (EXT_INT4-EXT_INT7). By setting the related XIP bit in this register to 1, the CPU recognizes a high-to-low transition as signaling an interrupt.

TMS320C6201/6701 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a TMS320C6201/6701 write to HPI and 2) a TMS320C6201/6701 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 5. *Host TMS320C6201/6701 Reads Internal Memory of TMS320C6201/6701 Using the HPI (read w/o auto-increment)*
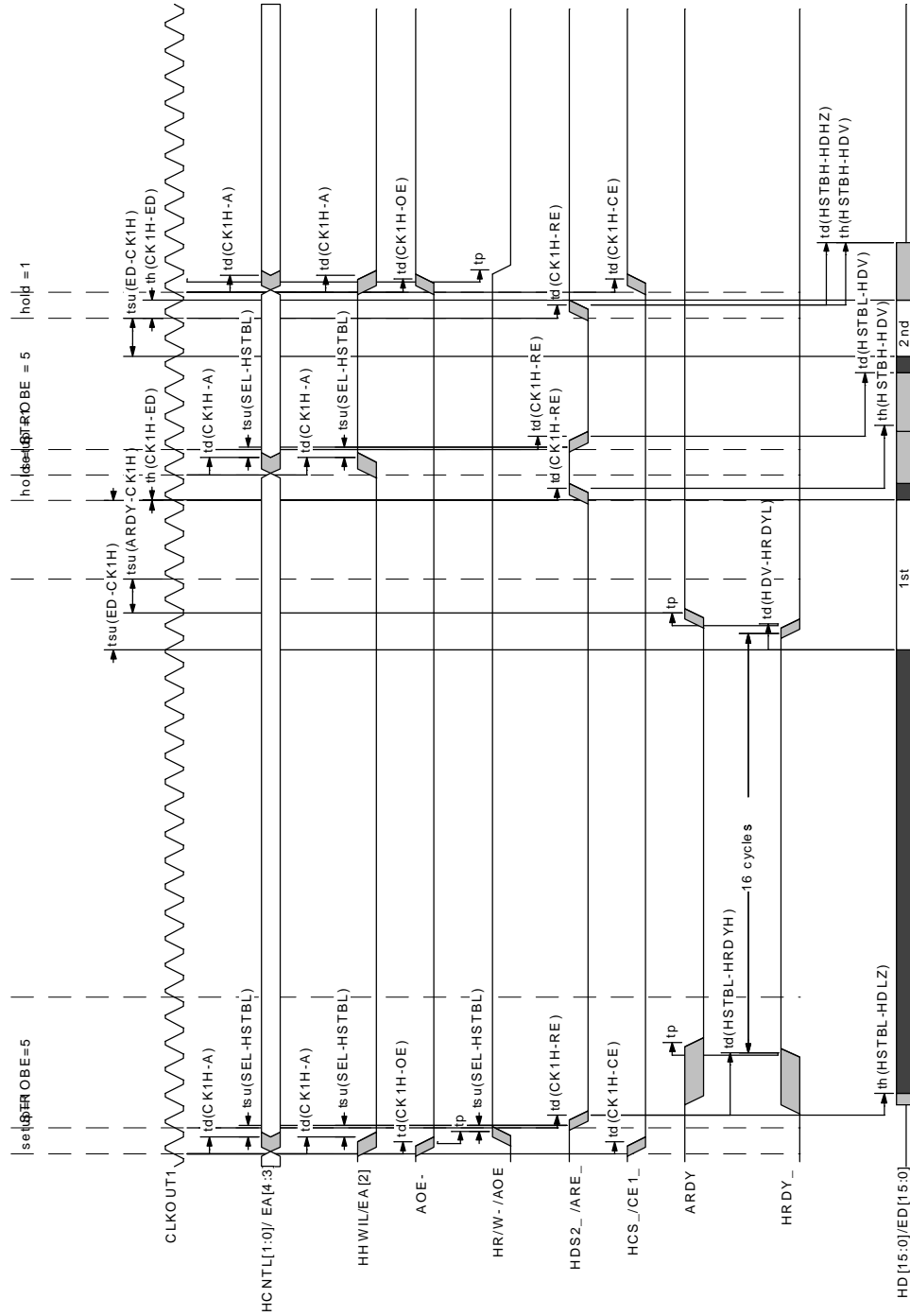
Figure 6. TMS320C6201/6701 Write to HPI
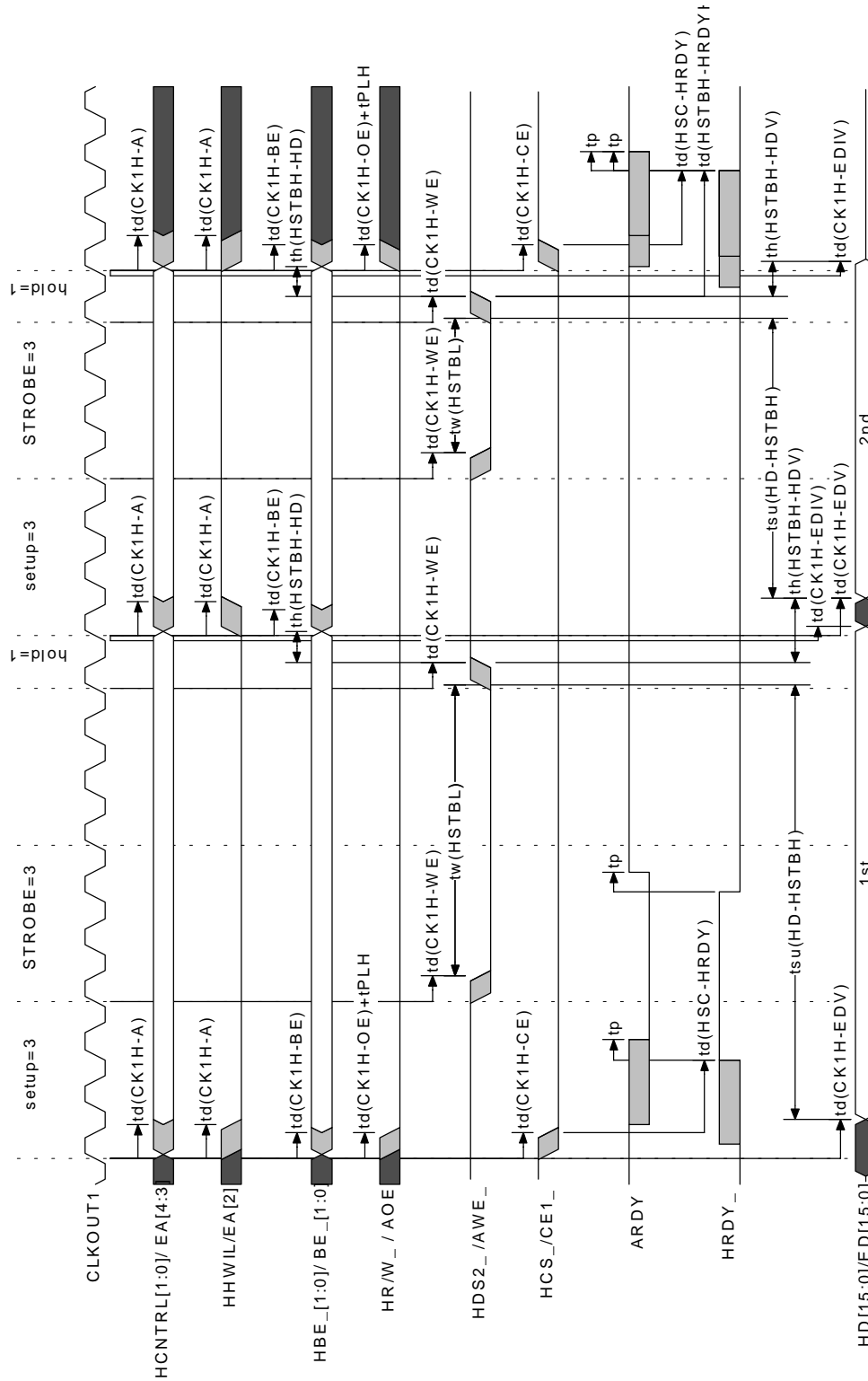
In Figures 5 and 6 timing parameters are named in the same way as those in the TMS320C6201/6701's data-sheet. Actual timing parameter values are listed in the Appendix.

Table 7.   Timing Requirements for HPI

HPI Symbol	TMS320C6201/6701 Symbol	Parameter	Min HPI [ns]	Min TMS320C6201/ C6701 [ns]
tw(HSTBL)	(STRB)*tcyc$^@$	Pulse width of HSTROBE low (STROBE=3)	2tcyc	3tcyc
tsu(SEL-HSTBL)	tcyc$^@$ - td(CK1H-OE)- tP+ td(CK1H-RE)	Setup time, Select Signals valid before HSTROBE low	1	1
th(HSTBL-SEL)	(STRB+1)*tcyc$^@$- td(CK1H-WE) + td(CK1H-EA)	Hold time, Select signals valid after HSTROBE low (STROBE=3).	2	20.8
tsu(HD-HSTBH)	(STRB+SETUP)*tcyc$^@$ - td(CK1H-EDV) + td(CK1H-WE)	Setup time, Host Data valid before HSTROBE high. (WRITE SETUP TIME) SETUP=3, STROBE=3	1	26.7
th(HSTBH-HD)	tcyc$^@$+ td(CK1H-EDIV) - th(CK1H-WE)	Hold time, Host Data valid after HSTROBE high.	1	3.4

Table 8.   Timing Requirements for TMS320C6201/6701 (Host)

HPI Symbol	TMS320C6201/6701 Symbol	Parameter	Min HPI [ns]	Min TMS320C6201 /C6701 [ns]
(STROBE)*tcyc$^@$- td(CK1H-RE)- td(HSTBL-HDV)	tsu(ED-CK1H)	Setup time, Data ready before CLKOUT1 high (READ SETUP TIME) STROBE=5	10.5	5
td(CK1H-RE)+ th(HSTBH-HDV)	th(CK1H-ED)	Hold time, Data valid after CLKOUT1 high.	3.4	0

@ tcyc denotes one clock cycle time of the host TMS320C6201. At 200 MHz operating frequency, tcyc= 5 ns. Time required for an edge to propagate through an inverter is represented as tP.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of TMS320C6201/6701 and HPI.

Note that when, on a first half-word write, CS- becomes valid HRDY- indicates that HPI is busy completing the internal portion of a previous HPI request.

M68300 Family of Integrated Microprocessors

Motorola's 68300 family of integrated microprocessors and micro-controllers combines the 32-bit performance of Motorola's 68K processor cores with a variety of on-chip peripheral configurations, to provide a versatile family of integrated solutions. Today there are dozens of 68300 family choices.

MC68302 Processor

The MC68302 integrated multiprotocol processor (IMP) is the first device to offer the benefits of a closely coupled, industry-standard M68000 microprocessor core and a flexible communications architecture. The device is especially suitable to applications in the communications industry.

MC68302 Interface

Figure 7 shows diagram of the host (MC68302) interface to the HPI.

Figure 7.   MC68302 to HPI Interface Block Diagram
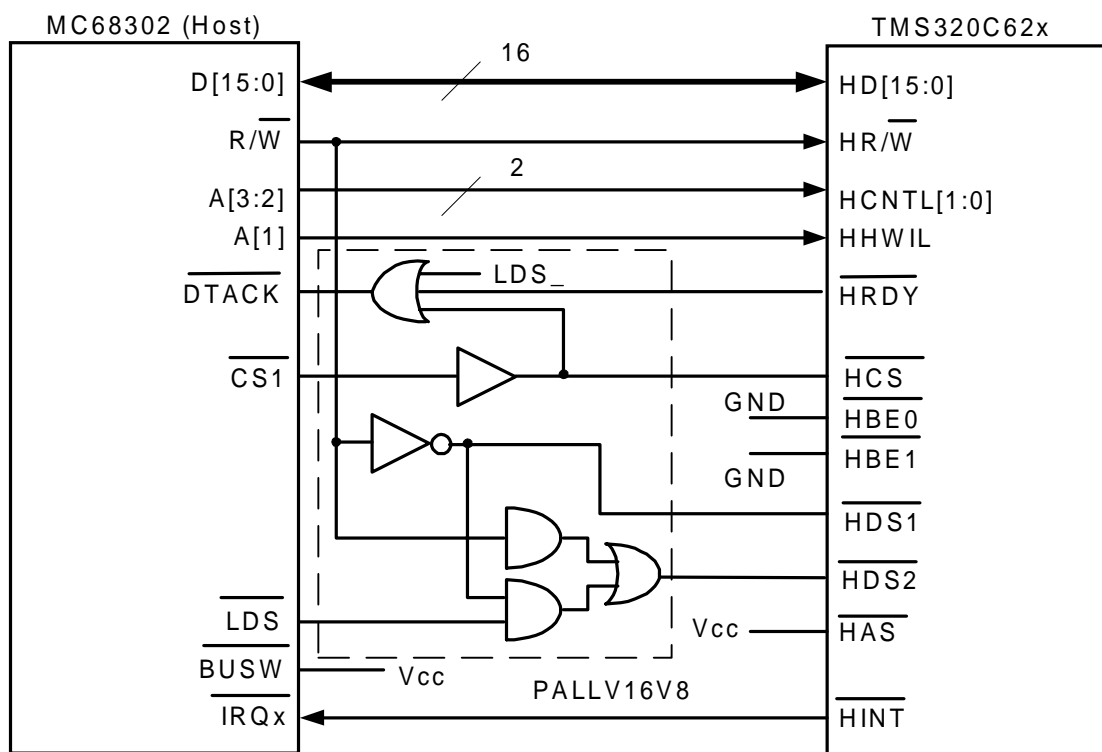
Table 9.   MC68302 to HPI Pin Connections

HPI Pin	MC68302 Pin	Comments
HCNTL[1:0]	A[3:2]	Address bits of MC68302 are used as control signals
HHWIL	A[1]	See above.
HR/W-	R/W-	Indicates a read or write access.
HD[15:0]	D[15:0]	16 LSBs of data.
HDS1-	Inverted R/W-	During a read transfer HDS1- is low (HDS2- is high), which enables HCS- to serve as both the chip select signal and the data strobe signal.
HDS2-	This signal is generated using PALLV16V8.	During a write cycle LDS- is used to generate HDS2- signal.

HAS-	Vcc	Unused
HCS-	Delayed CS1-	During a read CS1- serves as both the chip select signal and the data strobe signal.
HBE0-	GND	Unused.
HBE1-	GND	Unused
HRDY-	DTACK-	The MC68302 Option Registers need to be set to indicate that DTACK- is generated externally by HPI instead of internally by MC68302. Refer for MC68302 User's Manual for details.
HINT-	IRQx-	Refer to MC68302 User's manual for the desired level of interrupt (IRQ1-, IRQ6-, or IRQ7).
Vcc	BUSW-	Data bus is 16 bit wide.

UDS- and LDS- of MC68302 are data strobes. They cannot be used as control byte enable signals due to timing conflicts. Therefore the byte write enable control signals HBE1- and HBE0- are not used in this interface.

During a read transfer, the MC68302 requires the input data to stay valid tIDHCL after S6 low (hold time). The User's Manual does not specify the minimum time during which LDS- stays valid after S6 low. Therefore, it is not reliable to use LDS- as a HSTROBE during a read (since it could become inactive even before S6 low). During HPI read, CS- of the MC68302 is used to generate HSTROBE signal of the HPI. The timing requirement is met if CS- (output of the MC68302) is delayed for at least tIDHCL and then tied to HCS of the HPI. The delay is generated using PALLV16V8. During write CS- can not be used to generate HSTROBE since R/W- signal (HPI control signal) of the MC68302 could become valid after CS-. Therefore, during a write LDS- is used to generate HSTROBE.

Refer to MC68302 User's Manual for signal pull-up information. All bi-directional control signals need to be pulled-up high so that they are inactive when MC68302 is not driving them.

Configuration

The MC68302 provides a set of four programmable chip-select signals. This simplifies the interfacing to the HPI.

Each of the four chip-select units has two registers that define its specific operation. These registers are 16-bit base register (BR) and a 16-bit option register (OE) (e.g., BR0 and OR0). For each chip-select, the user programs the block size by choosing the starting address in the base register and the length in the option register. The staring address must be on a block boundary.

Chip select 0 has the special property of being enabled upon system reset to address range from 0 to 8K bytes.

DTACK field in the Option Registers is set to '111' to specify that signal DTACK- is generated externally from HPI.

The BR should normally be programmed after the OR since the BR contains the chip-select enable bit.

Table 10 and 11 illustrate configuration of the BR and OR registers.

Table 10.   Base Register (BR) Relevant Bits

Bit-field	Description	Value
BA23-BA13	Base Address. These bits are used to set the starting address of a particular address space.	
RW	Read/Write 0 = The chip-select line is asserted for read operations only. 1 = The chip-select line is asserted for write operations only.	Masked by MRW bit in the OR.
EN	Enable. After system reset, only CS0- is enabled. The chip-select line used by HPI has to be enabled by setting this bit to one.	EN=1

Table 11.   Option Register (OR) Relevant Bits

Bit-field	Description	Value
DTACK	These bits are used to determine whether DATCK- is generated internally or externally by the peripheral.	$\overline{DTACK}$ = '111'
M23-M13	Base Address Mask. These bits are used to set the block size of a particular chip-select line. 0 = The address bit in the corresponding BR is masked. 1 = The address bit in the corresponding BR is not masked.	
MRW	Mask Read/Write. 0 = The RW bit in the BR is masked. The chip-select is asserted for both read and write operations. 1 = The RW bit in the BR is not masked.	MRW=0

The user of MC68302 device communicates with the interrupt controller using four registers. The global interrupt mode register (GIMR) defines the interrupt controller's operational mode. The interrupt pending register (IPR) indicates which INRQ interrupt sources require interrupt service. The interrupt mask register (IMR) allows the user to prevent any of the INRQ interrupt sources from generating an interrupt request. The interrupt in-service register (ISR) provides a capability for nesting INRQ interrupt requests. With exception of level 7, which is always treated as edge sensitive, each of the interrupt lines of the MC68302 can be programmed to be either level sensitive or edge sensitive. For more detailed description on interrupts please refer to the MC68302 User's Manual.

MC68302 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a MC68302 write to HPI and 2) a MC68302 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 8. *MC68302 reads from internal memory of the TMS320C6201/6701 using the HPI (read without auto-increment)*

Figure 9.   MC68302 Write to HPI
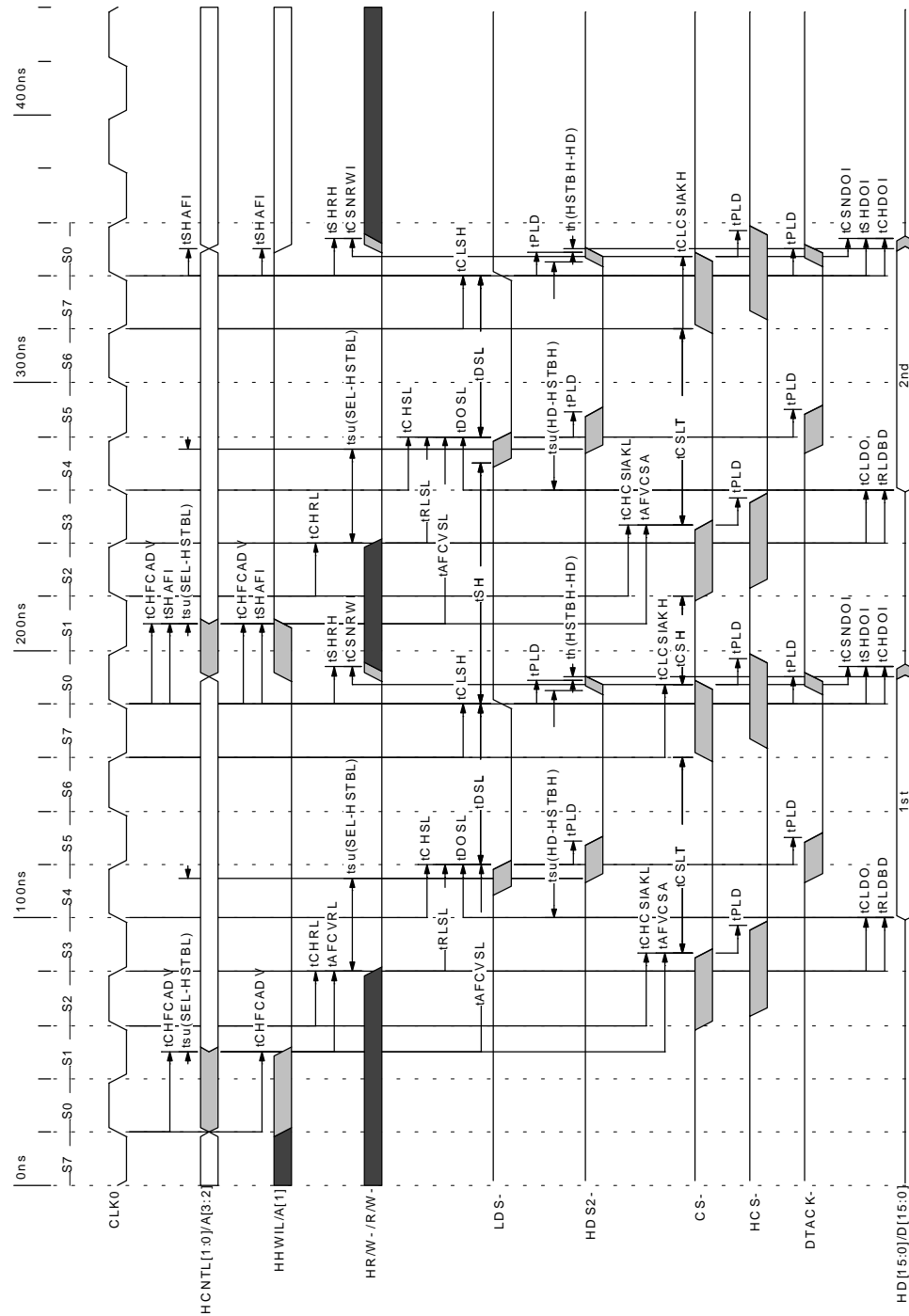
In Figures 8 and 9 timing parameters are named in the same way as those in the TMS320C6201/6701's and MC68302's data-sheets. Actual timing parameter values are listed in the Appendix.

Table 12.   Timing Requirements for HPI

HPI Symbol	MC68302 Symbol	Parameter	Min HPI [ns]	Min MC68302 [ns]
tw(HSTBL)	tDSL	Pulse width of HSTB- low.	10	40
tsu(SEL-HSTBL)	tAFVCSA+ tPLD	Setup time, Select Signals valid before HSTB- low.	1	22.5
th(HSTBL-SEL)	tDSL	Hold time, Select Signals valid after HSTB- low.	2	40
tsu(HD-HSTBH)	2tcyc$^@$- tCLDO+ tCLSH+tPLD	Setup time, Host Data valid before HSTB- high (WRITE SETUP TIME).	1	87.5
th(HSTBH-HD)	tSHDOI-tPLD	Hold time, Host Data valid after HSTB- high.	1	2.5

Table 13.   Timing Requirements for MC68302

HPI Symbol	MC68302 Symbol	Parameter	Min HPI [ns]	Min MC68302 [ns]
tPLD+ th((HSTBH-HDV))	tIDHCL	Input data hold time from clock low	10.5	5
3 Htcyc$^{@@}$- tCHCSIAKL- tPLD - td(HSTBL-HDV) + tcyc$^@$	tDICL	Data-in valid to clock low (READ SETUP TIME).	53.5	5
tCLCSIAKH + tPLD + td(HSTBH-HDV) - tCLSH	tSHDII	AS-,DS- Negated to Data In invalid (Hold time on read)	1	0

@ tcyc denotes one clock cycle time of MC68302. At 25MHz operating frequency, tcyc=40ns.

@@Htcyc denotes half clock time of MC68302. At 25 MHz operating frequency, Htcyc=20ns.

tPLD denotes PAL propagation.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of MC68302 and HPI. This interface is based on an MC68302-25 MHz device and a TMS320C6201 device at any frequency ranging from 100-200 MHz or C6701 device at any frequency up to167MHz.

MC68360 Processor

The MC68360 Quad Integrated Communication Controller (QUICC) is 32-bit controller that is an extension of other members of the Motorola M68300 family.

The MC68360 Quad Integrated Communication Controller (QUICC) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities.

MC68360 Interface

Figure 10 shows diagram of the host (MC68360) interface to the HPI.

Figure 10. MC68360 to HPI Interface Block Diagram
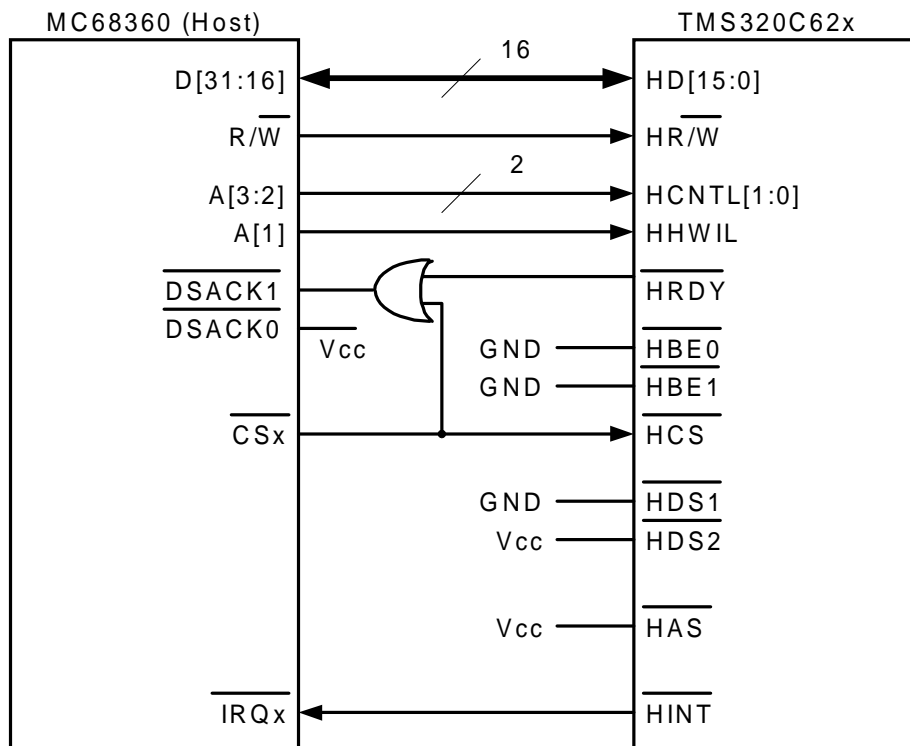
Table 14.   MC68360 to HPI Pin Connections

HPI Pin	MC68360 Pin	Comments
HCNTL[1:0]	A[3:2]	Address bits of MC68360 are used as control signals.
HHWIL	A[1]	A[1] identifies the first or second half-word of transfer.
HR/W-	R/W-	This indicates a read or write access.
HD[15:0]	D[31:16]	MC68360 uses D[31:16] for 16-bit port interface.
HDS1-	GND	HDS1- and HDS2- are internally exclusively-NORed. HDS1- and HDS2- are tied logic low and high, respectively, to enable data strobe at all time.
HDS2-	Vcc	See above.
HAS-	Vcc	Since host device MC68360 has separate address and data bus, HAS- does not need to be used. HAS- is tied inactive high.
HCS-	CSx-	Any one of chip-select of MC68360 can be connected to HCS- as the chip select signal. This also serves as the data strobe signal in this case (since DS- of MC68360 is not used as data strobe).
HBE0-	GND	MC68360 does not have byte write enable signals that have the same timing as other control signals. Therefore HBE1- and HBE0- of HPI are tied low to enable host access to both lower and upper bytes of the half-word during a write.
HBE1-	GND	See above.
HRDY-	DSACK1-	The SPS bits in the MC68360 Option Registers need to be set to indicate that DSACK1- is generated externally by HPI. Refer to the User's Manual for details.
HINT-	IRQx-	User can select interrupt level (IRQ1- to IRQ7-). Priority level 7 interrupt is a special case. Level 7 interrupts are non-maskable interrupts (NMI). IRQ7- is a level sensitive input and must remain low until the second instruction processing module (CPU32+) returns an interrupt acknowledge cycle for interrupt 7. Refer to the MC68360 User's Manual for the detailed description.

DS- (Data Strobe) of MC68360 is not used in this interface because MC68360 asserts DS- only after it latches a DSACK-low. However, HPI of 'C6201/6701 does not assert HRDY-(DSACK1-) until after DS- is asserted. Due to this timing conflict, HDS1- and HDS2- of 'C6x are tied logic low and high, respectively, to enable data strobe at all time.

The 'C6201/6701 must keep DSACKx- asserted until it detects the negation of AS-, DS- (whichever it detects first). The 'C6201/6701 must negate DSACKx- within approximately of one clock period after sampling negation of AS- or DS-. DSACKx-signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle. This is avoided by using OR combination of the HRDY- and CSx- signals.

HBE1- and HBE2- of 'C6201/6701 are tied low to enable host access to both lower and upper bytes of the half-word during a write. Although MC68360 has byte write enable signals WE1- and WE0, they are not used in this interface due to timing conflict. HPI expects control signals, including HBE1- and HBE0-, to be ready before data strobe (which is HCS- in this case) is asserted. However, MC68360 asserts chip select and write enable signals at the same time. Therefore, WE1- and WE0- cannot be used.

Configuration

The QUICC is comprised of three modules: the CPU32+ core, the System Integration Module (SIM60), and Communication Processor Module (CPM).

The memory controller is a sub-block of the SIM60 that is responsible for up to eight general-purpose chip-select lines. The general-purpose chip selects are available on lines CS0-CS7. CS0 also functions as the global (boot) chip select for accessing the boot EPROM. The SIM60 supports a glue-less interface to HPI.

The MC68360's general-purpose chip selects are controlled by the global memory register (GMR) and the memory controller status register (MSTAT). There is one GMR and MSTAT in the memory controller. Additionally, each SRAM bank has a base register (BR) and an option register (OR). MC68360 has eight identical sets of two registers, the BR and OR.

The 32-bit read-write GMR contains selections that are common to the entire memory controller. The GMR is used to control global parameters for memory banks.

The MSTAT reports write protect violations and parity errors for all banks.

Configuration of the BR and OR registers is shown in Tables 15 and 16.

Table 15.   Base Register (BR) Relevant Bits

Bit-field	Description	Value
CSNTQ	CS Negate Timing. This bit is used to determine when CS is negated during an internal QUICC or external QUICC/MC68030 –type bus master write cycle.	It should be set to 0 (CS negated normally).
TRLXQ	Timing Relax. This bit delays the beginning of the internal QUICC or external QUICC/MC68030-type bus master cycle to relax the timing constraints on the user.	It should be set to 0 (do not relax timing).
BA31-BA11	Base Address. The base address field, the upper 21 bits of each BR, and the function field are compared to the address on the address bus to determine if a DRAM/SRAM region is being accessed by an internal QUICC master.	

The option register is 32-bit read-write register that may be accessed at any time.

Table 16.   Option Register (OR) Relevant Bits

Bit-field	Description	Value
DSSEL	Dynamic RAM Select. This bit determines if the bank is	For HPI this bit should be set to 0.

	SRAM or DRAM.	
SPS1-SPS0	SRAM Port Size.	SPS0=1
	Since external DSACKx is used SPS[1:0]=11	SPS1=1
AM27-AM11	Address Mask.	
	Mask any of the corresponding bits in the associated BR. By masking the address bits independently, external devices of different address range sizes can be used.	
TCYC3-TCYC0	Cycle Length in Clocks	Since external DSACKx is selected with SPS, TCYC should not be set to zero.

MC68360 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a MC68360 write to HPI and 2) a MC68360 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 11.   MC68360 reads internal memory of the TMS320C6201/6701 using the HPI (read without auto-increment).
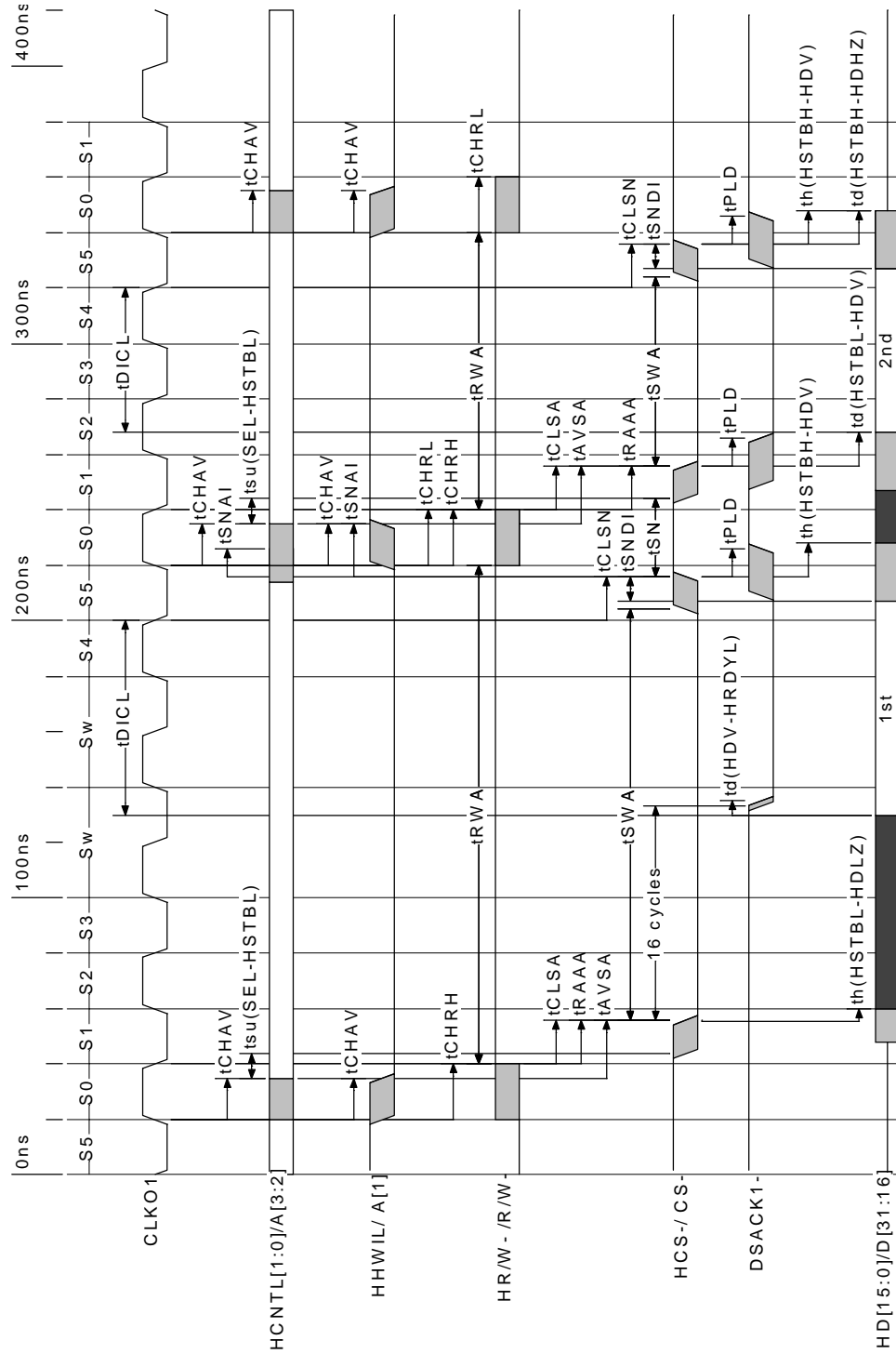
Figure 12. MC68360 Write to HPI
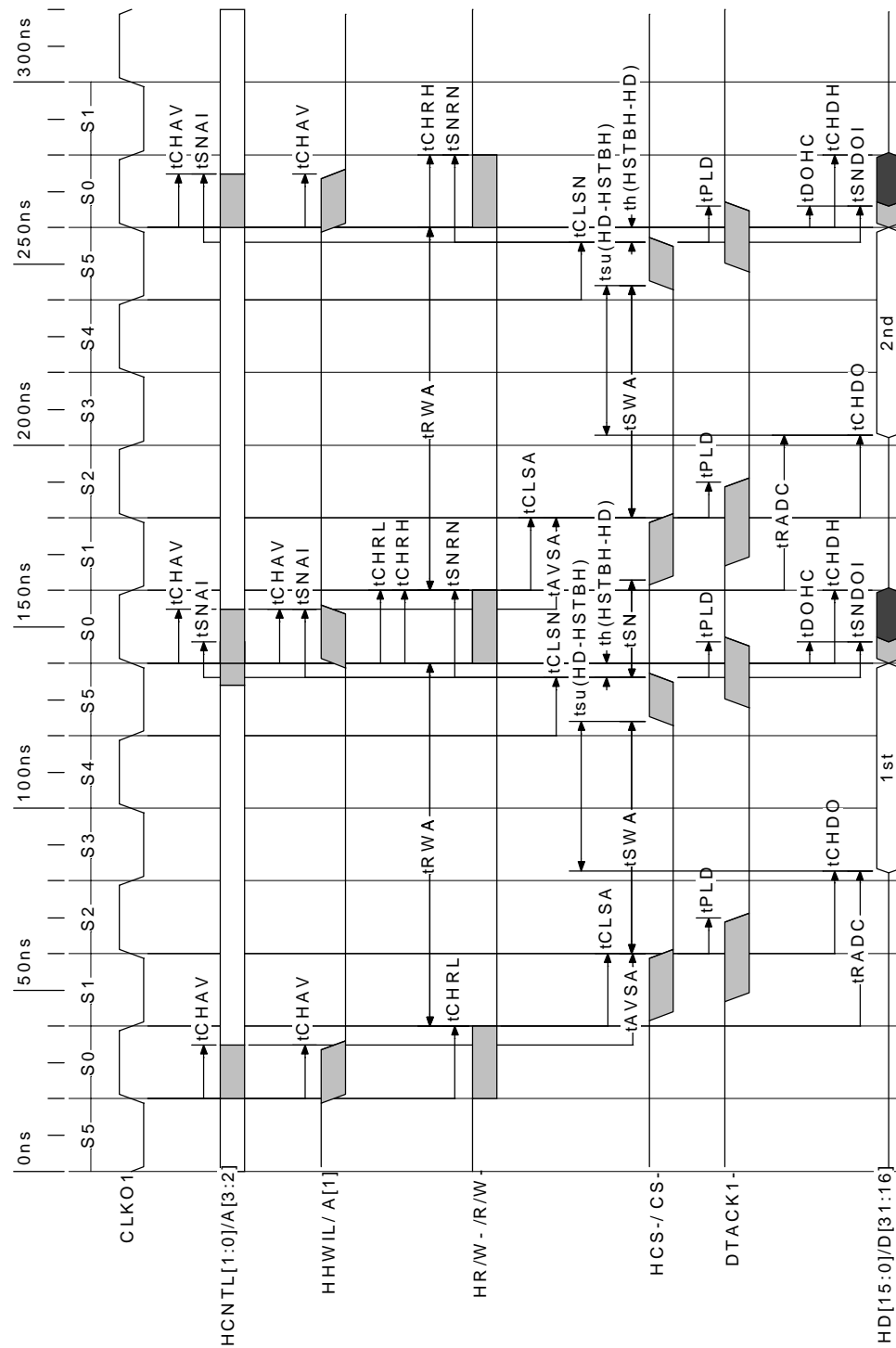
Table 17.   Timing Requirements for HPI

HPI Symbol	MC68360 Symbol	Parameter	Min HPI [ns]	Min MC68360 [ns]
tw(HSTBL)	tSWA	Pulse width of HCS- low	10	75
tsu(SEL-HSTBL)	tAVSA	Setup time, Select Signals valid before HDS- (HCS-) low	1	10
th(HSTBL-SEL)	tSNAI+tSWA	Hold time, Select signals valid after HDS-, (HCS-) low.	2	85
tsu(HD-HSTBH)	1.5*tcyc$^{@}$ - tCHDO+tCLSN	Setup time, Host Data valid before HDS-, (HCS-) high. (WRITE SETUP TIME)	1	41
th(HSTBH-HD)	tSNDOI	Hold time, Host Data valid after HDS-, (HCS-) high.	1	10

Table 18.   Timing Requirements for MC68360

HPI Symbol	MC68360 Symbol	Parameter	Min HPI [ns]	Min MC68360 [ns]
th(HSTBH-HDV)	tSNDI	Input data hold time from CS- negated	3	0
2tcyc$^{@}$-tCLSA-td(HSTBL-HDV)	tDICL	Data-in valid to clock low (READ SETUP TIME)	52	1

@ tcyc denotes one clock cycle time of MC68360. At 25MHz operating frequency, tcyc=40ns.

In Figures 11 and 12 timing parameters are named in the same way as those in the TMS320C6201/6701's and MC68360's datasheets. Actual timing parameter values are listed in the Appendix.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of MC68360 and HPI. This interface is based on a MC68360-25 MHz device and a TMS320C6201 device at any frequency ranging from 100-200 MHz or C6701 device at any frequency up to 167MHz.

PowerPC Microprocessors

The PowerPC family of microprocessors, which is being jointly developed by IBM, Motorola and Apple, is the foundation for an established and rapidly expanding market for RISC-based hardware and software. The three companies agreed to create a hardware reference platform (HRP) specification. A prime objective of the HRP specification and its initial hardware implementation is to create an environment that lets other chip and system vendors build components and HRP systems rapidly and inexpensively. The specification emphasizes the programming model of a compliant system. As an architecture, it is precise enough to assure software compatibility for several operating environments (Mac OS, AIX, OS/2, Windows NT, Solaris and Netware), broad enough to cover a range of systems from portables through servers, and flexible enough to evolve with technology and market demands.

MPC750 Processor

The PowerPC 750 microprocessor is a 32 bit implementation of the PowerPC family of Reduced Instruction Set Computer (RISC) microprocessors. The PowerPC 750 microprocessor is especially suitable for the notebook, mobile and power conscious desktop computing segments. Enhancements to this generation of the PowerPC 750 microprocessor family include:

1. Higher clock frequencies delivering higher levels of performance.

2. Dedicated L2 bus independent of the system bus.

3. 3x to 8x bus divider ratios, with half step increments, making the PowerPC 750 microprocessor easier to design in.

4. A performance enhancing feature supporting misalign little endian accesses for certain operating system environments

MPC750 Interface

The PowerPC 60x, PowerPC 740 and PowerPC 750 are all members of the PowerPC family. Although not identical, the system interfaces of these devices are very similar. The Power PC 750 to HPI interface described below is designed for single processor, non-pipelined system, in which the processor is parked on the bus and it's data bus grant line is tied low.

Figure 13 shows diagram of the host (MPC750) interface to the HPI.

Figure 13. MPC750 to HPI Interface Block Diagram

MPC750 (Host)   TMS320C62x

DH[0:15]   ←—— 16 ——→   HD[15:0]
A[29:28]   ——— 2 ——→   HCNTL[1:0]
A[30]   ————→   HHWIL
DBB   ————→   HDS1   HAS — Vcc
                                  HBE0 — GND
TT[0:4]   GENERATE   PALLV20V10 HBE1 — GND
           R/W-   HR/W   HDS2 — Vcc

A[3:0]   ADDRESS
           DECODE

TS   D Q   HCS
ABB   Q
AACK   HRDY
TA
GND — DBG
GND — BG

                D Q   D Q
                  Q   Q
SYSCLK ←

                HRDYS HRDYSD
INT ←   HINT

                SYSCLK
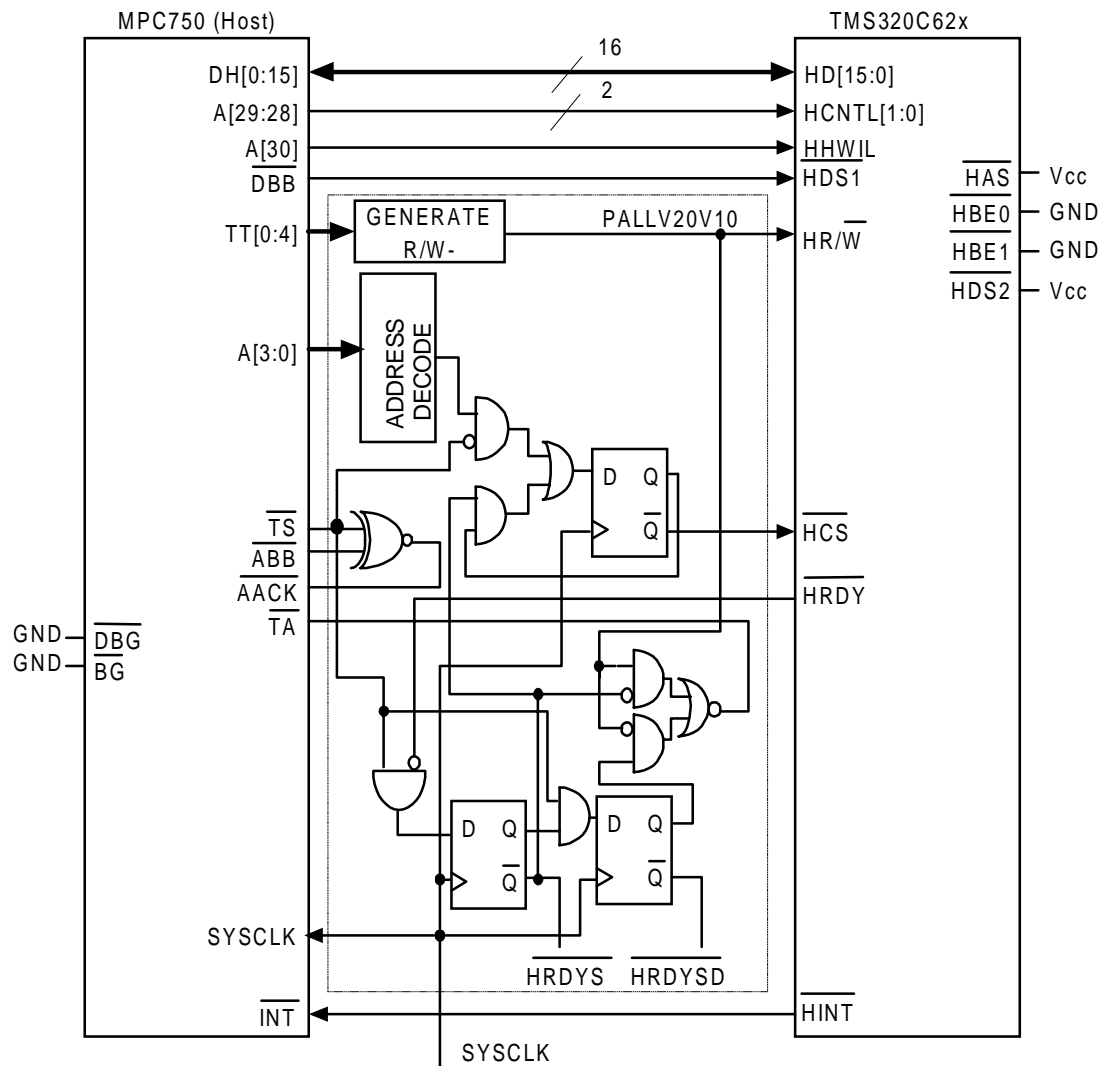
Table 19. MPC750 to HPI Pin Connections

HPI Pin	MPC750 Pin	Comments
HCNTL[1:0]	A[29:28]	Address bits of MPC750 are used as control signals. A31 is the LSB of the MPC750 address bus.
HHWIL	A[30]	See above.
HR/W-	TT[0:4]	The transactions on the PowerPC bus are identified

		by the TT[0:4] signals. The HR/W- is decoded from TT[0:4]
HD[15:0]	DH[0:15]	MPC750 uses DH[0:15] for 16-bit port interface. DH0 is the MSB of the MPC750 data bus, while HD15 is the MSB of HPI.
HDS1-	DBB-	The HPI data strobe (HDS1-) can be tied to DBB- signal of the MPC750.
HDS2-	Vcc	Unused. Tied to Vcc
HAS-	Vcc	Since host device MPC750 has separate address and data bus, HAS- does not need to be used. HAS- is tied inactive high.
HCS-	PAL is used to generate this signal.	Address decoder, TS- and synchronized HRDY are used to generate CS- signal (PALLV20V10-7).
HBE0-	GND	MPC750 does not have byte write enable signals that have the same timing as other control signals. Therefore HBE1- and HBE0- of HPI are tied low to enable host access to both lower and upper bytes of the half-word during a write.
HBE1-	GND	See above.
HRDY-	TA-	When asserted TA- indicates that a data transfer completed successfully. TA- is synchronous input and HRDY- has to be synchronized.
HINT-	INT-	Interrupt pin of HPI is tied to INT- of MPC750.
GND	BG-	Bus Grant (BG-) is asserted indicating that the host is the only bus master in the system.
GND	DBG-	The only device in this system that can be the data bus master is the host, therefore Data Bus Grant (DBG-) is tied low.
-	AACK-	When asserted AACK- indicates that the address phase of a transaction is complete. The address bus goes to high-impedance state on the next bus clock cycle.
-	ABB-	If asserted ABB- Indicates that the device is the address bus master. ABB- and TS- are used to generate AACK-.
-	TS-	Asserted TS- indicates that the master has begun a memory bus transaction and the address bus and transfer attribute signals are valid. ABB- and TS- are used to generate AACK-.

The simple interface described here (see Figure 13) uses a single PLLV22V10-7.

PowerPC60x microprocessors use Big Endian nomenclature, where the most significant position is labeled 'bit zero'. Therefore, MPC750 data bus DH[0:15] is connected to HPI data bus HD[15:0] in reverse order.

The transfer type signals TT[0:4] indicate whether it is a read or write, whether it is a burst or a single beat transfer etc. The encoding has been chosen to simplify decoding. For example, TT1 is generally zero for writes and one for reads. The transfer type signals are decoded using a PALLV20V10-7, which generates HR/W- required by the HPI.

To guarantee that timing requirement th(HSTBH-HDV) is met during an HPI write the internal HSTROBE is generated differently for a read and write cycles. During a read transfer, HSTROBE is asserted on rising edge of SYSCLK when address is matched and ADS- is low. HSTROBE is negated when synchronized HRDY indicates ready status. During a write transfer synchronized HRDY is used to de-assert HSTROBE while synchronized HRDY delayed for one clock is used to generate ready signal for MPC750. This way MPC750 holds the data on the bus, and ends the transfer one clock after HSTROBE is negated. This is done in order to meet data hold-timing requirement of the HPI.

MPC750 requires single system clock input, SYSCLK, which represents the bus interface frequency. Internally, the processor uses a phase-locked loop (PLL) circuit to generate a master core clock that is frequency-multiplied and phase locked to the SYSCLK input. This core frequency is used to operate the internal circuitry. The PLL is configured by the PLL_CFG[0-3] signals, which select the multiplier that the PLL uses to multiply the SYSCLK frequency up to the internal core frequency. For information about supported clock frequencies, see the MPC750 hardware specifications.

The operational (SYSCLK) frequency of the design shown in Figure 13 is 50 MHZ.

Configuration

The PowerPC architecture defines an external interrupt exception, which in the MPC750 processor is signaled to the processor by assertion of the external interrupt signal, INT-.

The MPC750 processor recognizes the interrupt condition (INT-asserted) only if Machine State Register bit MSR[EE] is set. To guarantee that the external interrupt is taken, INT- must remain asserted until the processor takes the interrupt; otherwise, the processor is not guaranteed to take an external interrupt.

The MSR[LE] bit enables little-endian mode. If MSR[LE] is one MPC750 runs in little-endian mode otherwise it runs in big-endian mode.

MPC750 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a MPC750 write to HPI and 2) a MPC750 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

*Figure 14. MPC750 reads from internal memory of TMS320C6201/6701 using the HPI (read without auto-increment).*
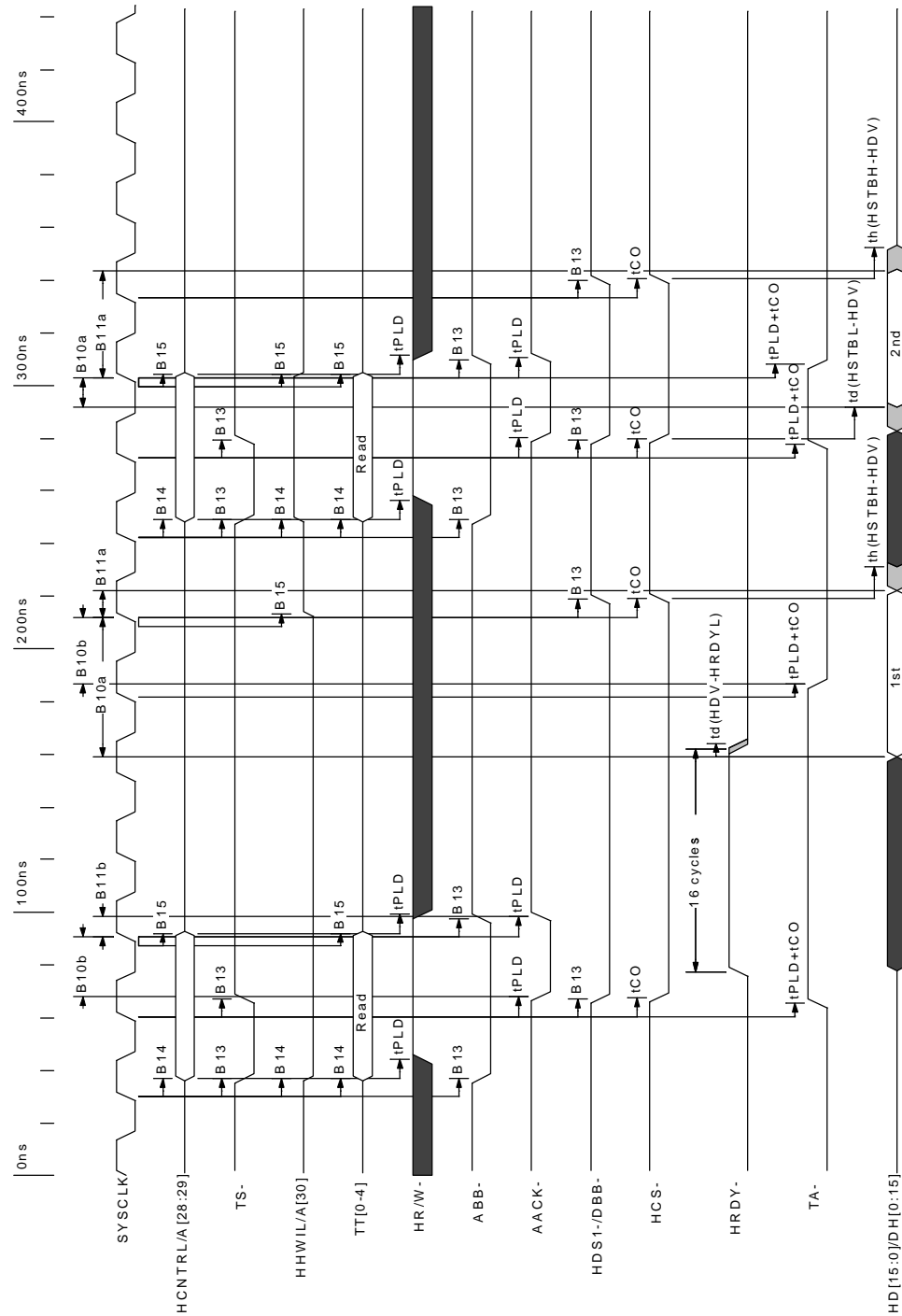
Figure 15.   MPC750 Write to HPI
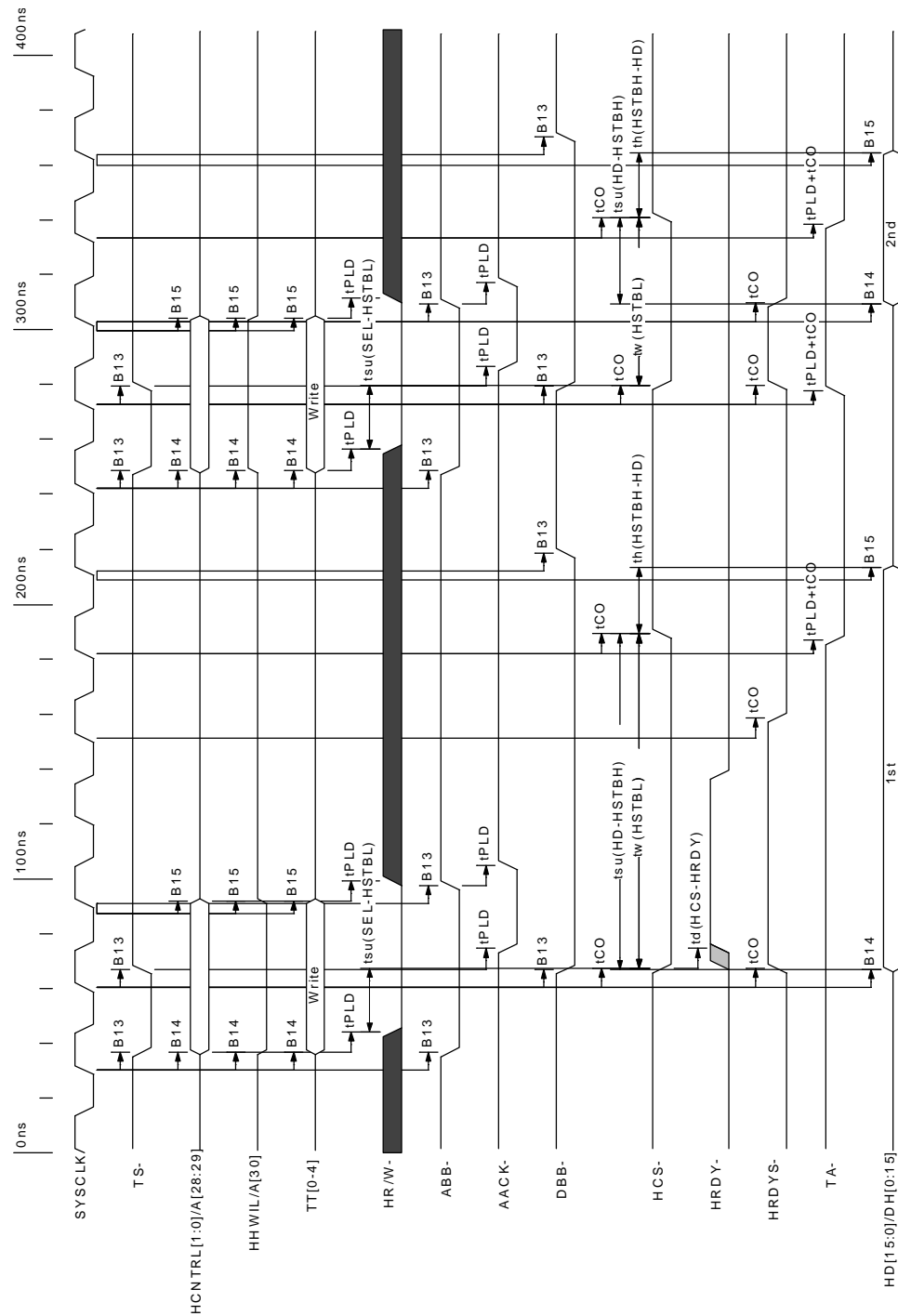
Table 20.   Timing Requirements for HPI

HPI Symbol	MPC750 Symbol	Parameter	Min HPI [ns]	Min MPC750 [ns]
tw(HSTBL)	2tcyc$^{@}$	Pulse width of HCS-low.	10	60
tsu(SEL-HSTBL)	tcyc$^{@}$-B14-tPLD+B13	Setup time, Select Signals valid before HCS-low.	1	25
th(HSTBL-SEL)	tcyc$^{@}$	Hold time, Select Signals valid after HCS-low.	2	30
tsu(HD-HSTBH)	tcyc$^{@}$-B14+tCO	Setup time, Host Data valid before HCS-high. (WRITE SETUP TIME)	1	28.5
th(HSTBH-HD)	tcyc$^{@}$-tCO+B15	Hold time, Host Data valid after HCS-high.	1	26

Table 21.   Timing Requirements for MPC750

HPI Symbol	MPC750 Symbol	Parameter	Min HPI [ns]	Min MPC750 [ns]
tCO+ th(HSTBH-HDV)	B11a	Input data hold time from SYSCLK rising edge.	17	1
>tcyc$^{@}$	B10a	Data in valid to clock high. (READ SETUP TIME)	>30	2.5
tcyc$^{@}$-tCO-tPLD	B10b	TA-Setup time	25	3
>tcyc$^{@}$	B11b	TA-Hold Time	>30	1

@ tcyc denotes one clock cycle time of MPC750. At 33 MHz bus operating frequency, tcyc=30ns.

@@ Htcyc denotes half of one clock cycle time of MPC750. At 30 MHz bus operating frequency, Htcyc=15ns.

In Figures and Tables above tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output respectively for PALLV20V10-7.

In Figures 14 and 15 timing parameters are named in the same way as those in the TMS320C6201/6701's and MPC750's datasheets. Actual timing parameter values are listed in the Appendix.

Note that when, on a first half-word write, CS- becomes valid HRDY- indicates that HPI is busy completing the internal portion of a previous HPI request.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of MPC750 and HPI. This interface is based on a MPC750 device with bus operating at 33 MHz and a TMS320C6201 device at any frequency ranging from 100-200 MHz or C6701 device at any frequency up to 167MHz.

MPC860 Processor

The MPC860 is the first embedded PowerPC family to address the needs of the inter-networking and data communication markets.   The MPC860 PowerQUICC (Quad Integrated Communication Controller) is a versatile, single-chip integrated microprocessor family that continues the heritage of its well-known predecessors, the 32-bit 68360 (360) QUICC and 68302 (302) families. The PowerQUICC family incorporates much of the 360's unique communications-oriented peripheral set and integrates additional enhancements, making it the highest-integration family of embedded PowerPC devices available from Motorola today.   The family is integrating a 32-bit embedded PowerPC core central processing unit (CPU); a memory controller; a second powerful RISC-based communication processor module (CPM); and system functions on a single chip.

MPC860 Interface

Figure 16 shows diagram of the host (MPC860) interface to the HPI.

Figure 16.   MPC860 to HPI Interface Block Diagram
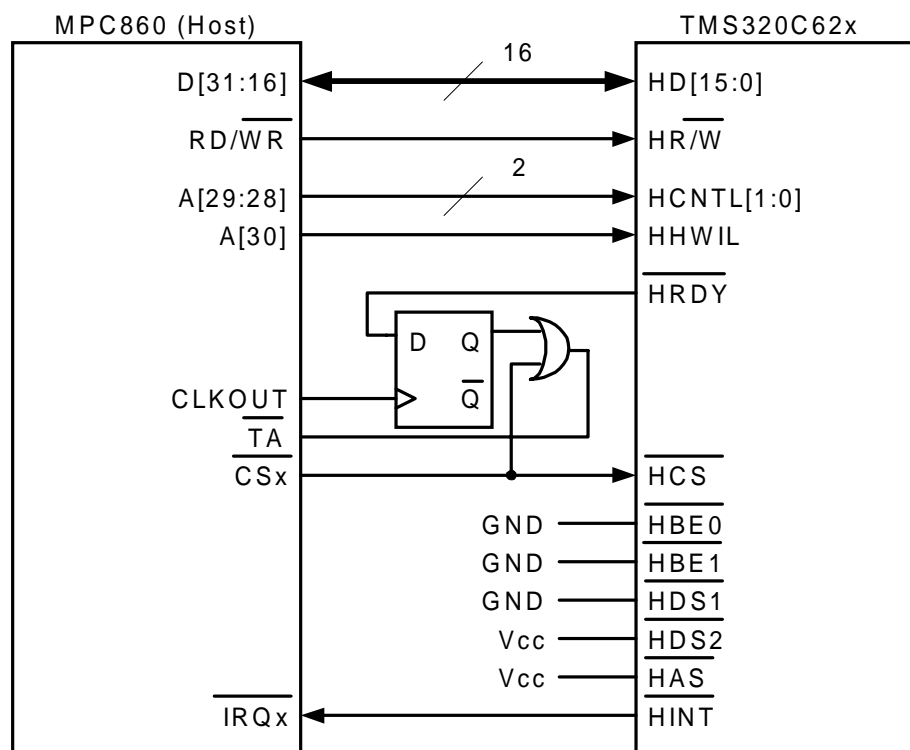

Table 22.   MPC860 to HPI Pin Connections

HPI Pin	MPC860 Pin	Comments
HCNTL[1:0]	A[28:29]	Address bits of MPC860 are used as control signals. A31 is the LSB of the MPC860 address bus.
HHWIL	A[30]	See above.
HR/W-	RD/WR-	Indicates a read or write access.
HD[15:0]	D[0:15]	MPC860 uses D[0:15] for 16-bit port interface. D0 is the MSB of the MPC860 data bus, while HD15 is the MSB of HPI.
HDS1-	GND	HDS1- and HDS2- are internally exclusively-NORed. HDS1- and HDS2- are tied logic low and high, respectively, to enable data strobe at all time.
HDS2-	Vcc	See above.

HAS-	Vcc	Since host device MPC860 has separate address and data bus, HAS- does not need to be used. HAS- is tied inactive high.
HCS-	CSx-	Any one of CS1- to CS5- of MPC860 can be connected to HCS- as the chip select signal. This also serves as the data strobe signal in this case (since no separate MPC860 data strobe signal is used).
HBE0-	GND	MPC860 does not have byte write enable signals that have the same timing as other control signals. Therefore HBE1- and HBE0- of HPI are tied low to enable host access to both lower and upper bytes of the half-word during a write.
HBE1-	GND	See above.
HRDY-	TA-	SETA bit in the MPC860 Option register is set to 1 to indicate that TA- is generated externally by HPI. HRDY~ is synchronized using bus clock and connected to TA~.
HINT-	IRQx-	Refer to the MPC860 User's Manual for the desired interrupt level (IRQ0- to IRQ7-).

MPC860 data bus D[0:15] is connected to HPI data bus HD[15:0] in reverse order, i.e., D0 is connected to HD15, D1 is connected to HD14, D2 is connected to HD13, etc. This is because the most significant bit of the MPC860 data bus is D0, while the most significant bit of the HPI data bus is HD15.

The Transfer Acknowledge (TA) signal of the MPC860 chip is synchronous signal, therefore the HRDY signal of the HPI must be synchronized in order for interface to function properly.

HBE1- and HBE0- of 'C6201/6701 are tied low to enable host access to both lower and upper bytes of the half-word during a write. Although MPC860 has byte write enable signals WE1- and WE0-, they are not used in this interface due to timing conflicts. HPI expects control signals, including HBE1- and HBE0-, to be ready before data strobe (which is HCS- in this case) is asserted. However, MPC860 does not assert write enable signals until after chip select signal is asserted. Therefore WE1- and WE0- cannot be used.

Configuration

The MPC860's memory controller is responsible for the control of up to eight memory banks, and it provides a set of eight programmable chip-select signals. A Chip Select of the MPC860 is tied to the HCS of the HPI. This greatly simplifies the interfacing to the HPI.

Status bits for each one of the memory banks are in the memory controller status register (MSTAT) and there is only one MSTAT for the entire memory controller. Each memory bank has a base register (BR) and an option register (OR). The MSTAT reports write-protect violations that have occurred and parity errors for every bank. The BRx and the ORx registers are specific memory to bank x. The BR contains a valid (V) bit that indicates that the register information for that chip-select is valid.

Each one of the OR registers define the attributes for the general-purpose-chip select machine when accessing the corresponding bank.

The General-Purpose Chip-Select Machine (GPCM) allows a glue-less and flexible interface between the MPC860 and HPI. If the MS bits in the BRx of the selected bank (Bank x) select the GPCM machine, the attributes for the memory cycle initiated are taken from the ORx register. These attributes include the CSNT, ACS(0:1), SCY(0:3), TRLX, EHTR, and SETA fields.

Configuration of the BR and OR is shown in Tables 23 and 24.

Table 23.   Base Register (BR) Relevant Bits

Bit-field	Description	Value
BA[0:16]	Base Address. The base address field, the upper 17 bits of each base address register, and the address type code field are compared to the address on the address bus to determine if a memory bank controlled by the memory controller is being accessed by an internal bus master. These bits are used in conjunction with the AM[0:16] bits in the OR.	
PS[0:1]	Port Size.	10 = 16 bits port size.

	This field specifies the port size of this memory region.	
WP	Write Protect. This bit can restrict write accesses within the address range of a base register.	0 = Both read and write accesses are allowed.
MS[0:1]	Machine Select. This field specifies the machine selected for the memory operations handling.	00 = G.P.C.M.
V	Valid Bit. This bit indicates that the contents of the base register and the option register pair are valid. The CS- signal does not assert until the V-bit is set.	1 = This bank is valid.

Table 24.   Option Register (OR) Relevant Bits

Bit-field	Description	Value
AM[0:16]	Address Mask. The address mask provides masking on any corresponding bits in the associated base register. By masking the address bits independently, external devices of different size address ranges can be used.	
ATM[0:2]	Address Type Mask. This field can be used to mask certain address type bits, allowing more than one address space type to be assigned to a chip-select.	
CSNT	Chip Select Negation Time. This attribute is used to determine when CS-/WE- are negated during an external memory write access handled by the GPCM.	0 = CS-/WE- are negated normally.
ACS[0:1]	Address to Chip-Select Setup. It allows the CS- assertion to be	11 = CS- is output half a clock later than the address lines.

	delayed relative to the address change.	
BI-	Burst Inhibit. This attribute determines whether or not this memory bank supports burst accesses.	1 = This bank does not support burst accesses.
SCY[0:3]	Cycle Length in Clocks.	Since an external TA- response is selected, SCY bits are not used.
SETA	External Transfer Acknowledge.	1 = TA- is generated by external logic.
TRLX	Timing Relaxed. This bit, when asserted, modifies the timing of the signals that control the memory devices when the GPCM is selected to handle the memory access initiated to this memory region.	0 = Normal timing is generated by GPCM.
EHTR	Extended Hold Time on Read Access. This bit, when asserted inserts an idle clock cycle after a read access from the current bank and any MPC860	0 = Normal timing is generated by the memory controller.

MPC860 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a MPC860 write to HPI and 2) a MPC860 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 17. *MPC860 reads internal memory of the TMS320C6201/6701 using the HPI (read without auto-increment).*
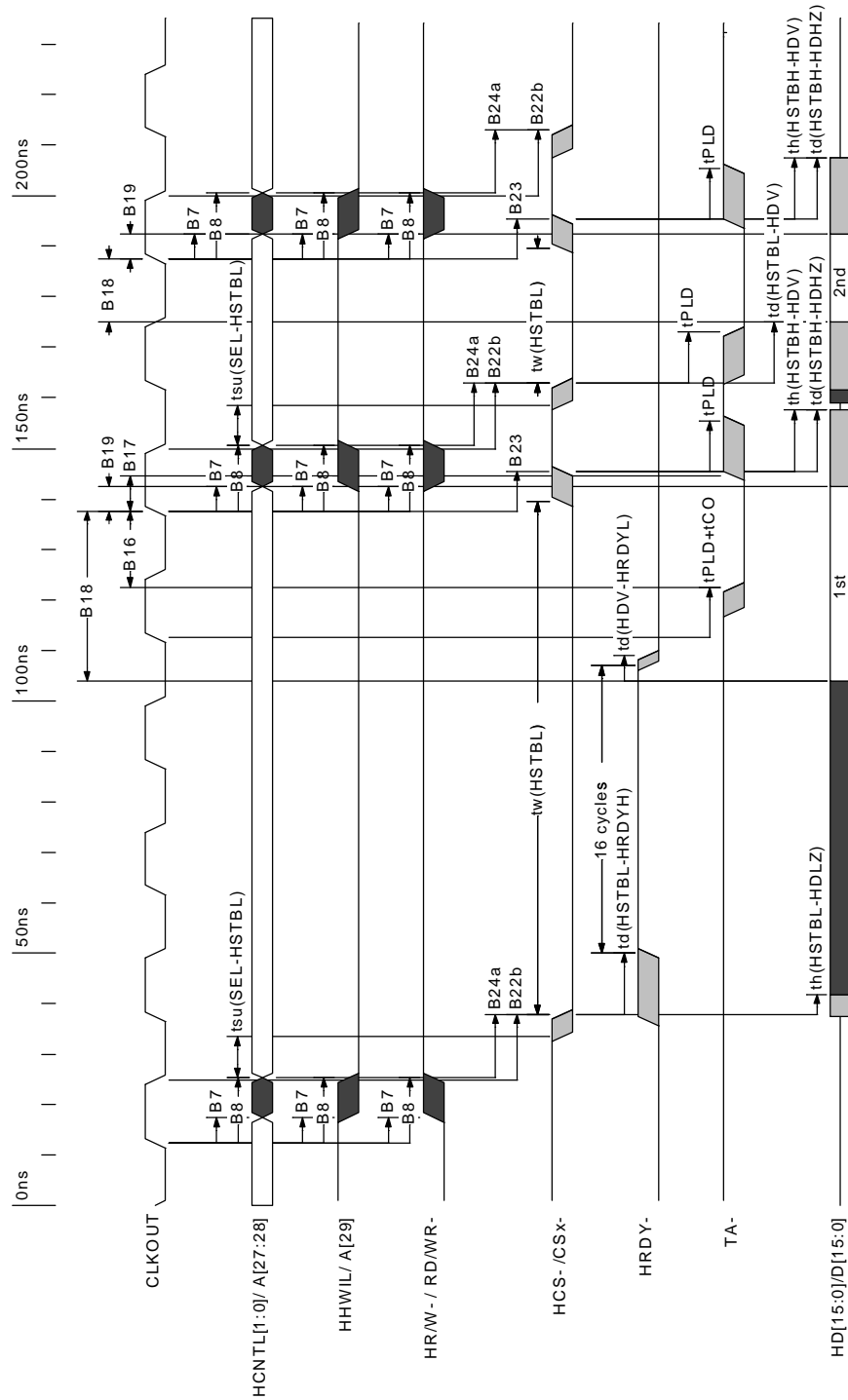
Figure 18.   MPC860 Write to HPI
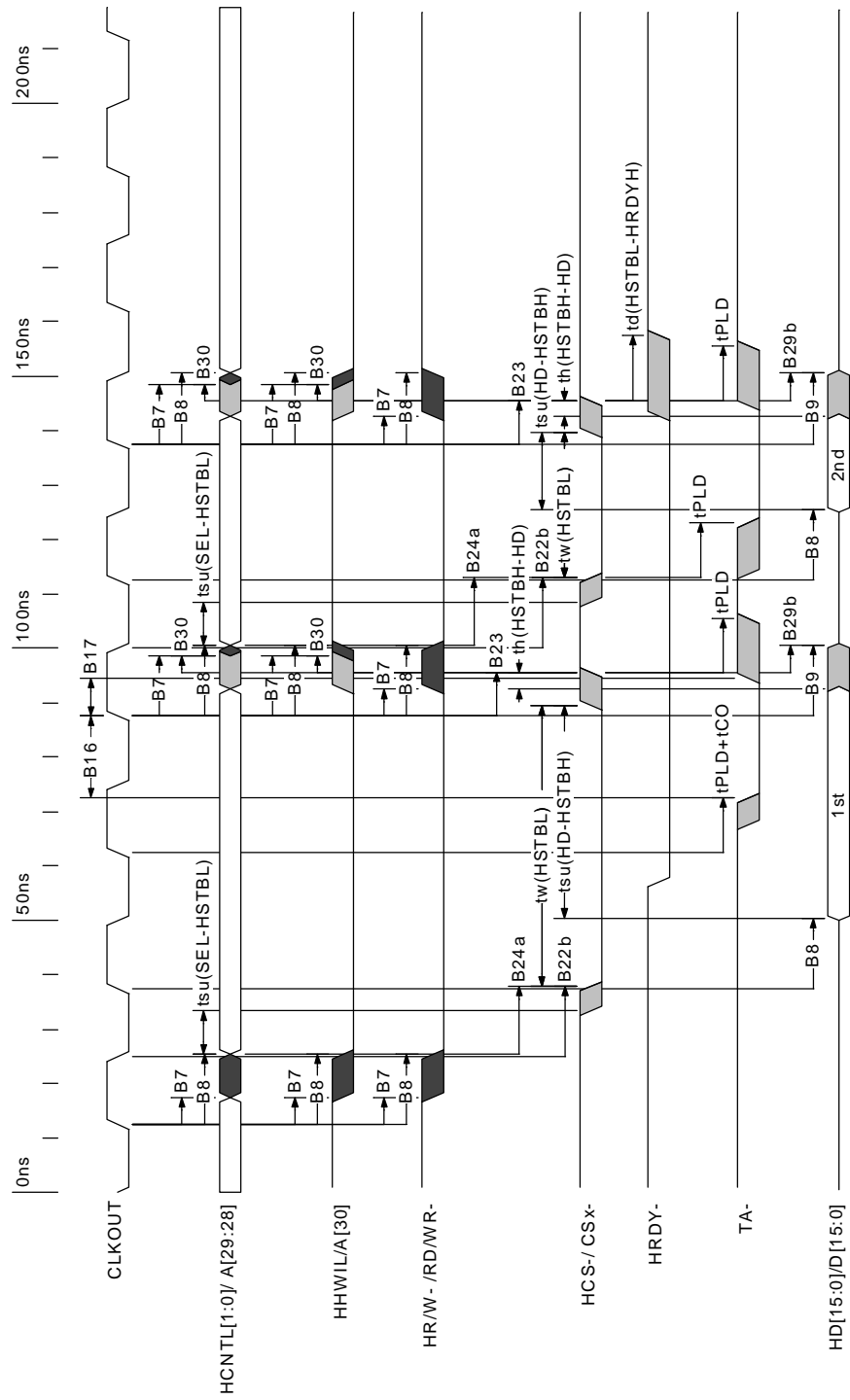
Table 25. Timing Requirements for HPI

HPI Symbol	MPC860 Symbol	Parameter	Min HPI [ns]	Min MPC860 [ns]
tw(HSTBL)	3*Htcyc$^{@@}$- B22b+B23	Pulse width of HSTROBE low.	10	26.5
tsu(SEL-HSTBL)	B24a	Setup time, Select Signals valid before HSTROBE low.	1	8
th(HSTBL-SEL)	3* Htcyc$^{@@}$- B22b+B7	Hold time, Select Signals valid after HSTROBE low.	2	29.5
tsu(HD-HSTBH)	tcyc$^{@}$-B8+B23	Setup time, Host Data valid before HSTROBE high. (WRITE SETUP TIME)	1	14
th(HSTBH-HD)	B29b	Hold time, Host Data valid after HSTROBE high.	1	3

Table 26. Timing Requirements for MPC860

HPI Symbol	MPC860 Symbol	Parameter	Min HPI [ns]	Min MPC860 [ns]
B23+ th(HSTBH-HDV)	B19	Input data hold time from CLKOUT rising edge.	5	1
3*Htcyc$^{@@}$- B22b- td(HSTBL-HDV)	B18	Data in valid to clock high. (READ SETUP TIME)	14.5	6
tcyc$^{@}$- tPLD-tCO	B16	TA- valid to CLKOUT (setup time)	25	7
B23+tPLD	B17	CLKOUT to TA- valid (hold time)	7	2

@ tcyc denotes one clock cycle time of MPC860. At 40MHz operating frequency, tcyc=25ns.

@ @ Htcyc denotes half of one clock cycle time of MPC860. At 40MHz operating frequency, Htcyc=12.5ns.

In Figures and Tables above tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output respectively for PALLV16V8.

Note that when, on a first half-word write, CS- becomes valid HRDY- indicates that HPI is busy completing the internal portion of a previous HPI request.

In Figures 17 and 18 timing parameters are named in the same way as those in the TMS320C6201/6701's and MPC860's datasheets. Actual timing parameter values are listed in the Appendix.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of MPC860 and HPI. This interface is based on a MPC860-40 MHz device and a TMS320C6201 device at any frequency ranging from 100-200 MHz or C6701 device at any frequency up to 167MHz.

Intel 80960 Microprocessor Family

The i960 is a high performance 32-bit RISC embedded processor family, with performance range of 7 MIPS to 150 MIPS. The i960 is targeted for applications that execute large amounts of code (usually over 1 MByte), move large amounts of data rapidly, and/or require very fast response times. Specifically, the i960 processors are a good fit for:

1) Local and wide area networking - bridges, routers, hubs, ATM, FDDI.

2) Intelligent PC I/O controllers - SCSI, RAID.

3) Imaging - printers, scanners, x-terminals, medical imaging.

Intel 80960Jx and 80960Rx Processors

The series of i960 Microprocessor Jx Family (JA, JF, JD) members are differentiated by frequency, core speed, operation voltage and cache size.

The first proliferation, the 80960JF, utilizes 4-Kbyte, 2-way set associative instruction cache, 2-Kbyte direct mapped data cache at 5V and 3V.

The 80960JA has 2-Kbyte instruction cache and 1-Kbyte data cache at 5V and 3V.

The highest proliferation, the 80960JD, contains 4-Kbyte-instruction cache, 2-Kbyte data cache plus an internal clock doubler.

Intel's family of I/O processors, the 80960RP and RD, build on the established performance of Intel's 80960 RISC architecture and also encompass industry initiatives, including PCI and I2O, to effectively off-load host CPUs of I/O processing tasks. These highly integrated processors offer a cost-effective approach to implementing PCI-based intelligent I/O subsystems.

The i960 RP/RD I/O processor is a highly integrated device incorporating the JF/JD RISC processor core, a PCI-PCI bridge, an I2C interface for system management features, memory controller, two DMA controllers as well as several other peripherals required to meet server performance requirements.

The memory Controller allows direct control of external memory systems, including DRAM, SRAM, ROM and Flash memory. It provides a direct connect interface to memory that typically does not require external logic.

80960Jx/80960Rx Interface

Figure 19 shows diagram of the host (Intel 80960Jx/Rx) interface to the HPI.

*Figure 19.   80960Jx (80960Rx) to HPI Interface Block Diagram*
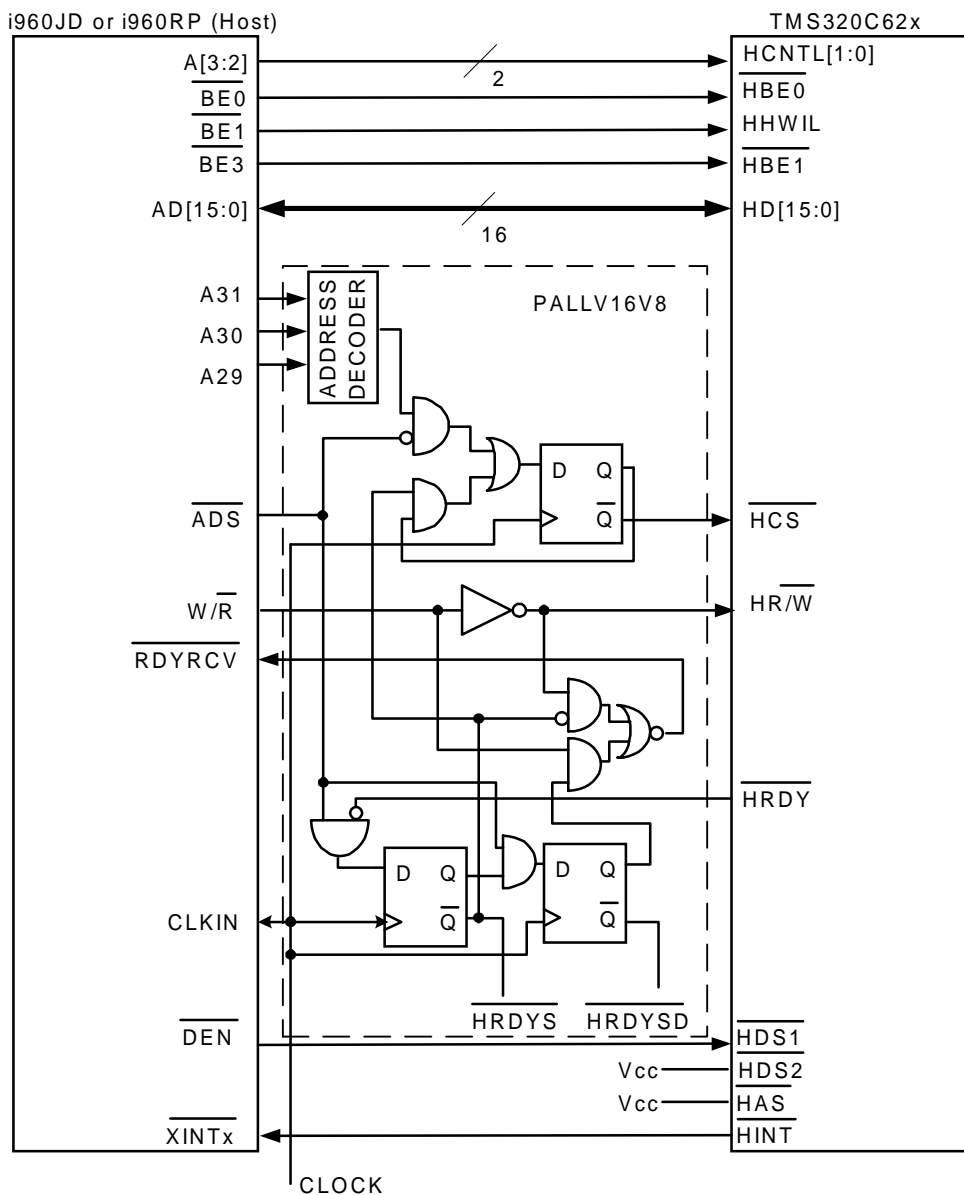
Table 27.   80960Jx to HPI Pin Connections

HPI Pin	80960Jx Pin	Comments
HCNTL[1:0]	A[3:2]	Address bits of i960JD/RP are used as control signals.
HHWIL	BE1-	BE1- identifies the first or second half-word of transfer.

HR/W-	Inverted W/R-	Indicates a read or write access. Since the C6201/6701 HPI port has a read-write (HR/W~) line which has the opposite polarity of i960JD/RP's read-write pin, an inverter is used to connect these two lines.
HD[15:0]	AD[15:0]	16 LSBs of data.
HDS1-	GND	HDS1- and HDS2- are internally exclusively-NORed. HDS2~ is tied logic high. HDS1~ is tied to GND. HCS~ is used to generate HSTROBE~.
HDS2-	Vcc	See above
HAS-	Vcc	Address Latch Enable is not used in this interface.
HCS-	Address lines A[31:29] are decoded and synchronized using ALE-.	Since the i960JD/RP does not have a chip select line, it is necessary to use some decode logic as an input to HCS-.
HBE0-	BE0-	HPI uses this value on writes only.
HBE1-	BE3-	HPI uses this value on writes only.
HRDY-	RDYRCV-	Asynchronous ready output is synchronized and connected to the RDYRCV~.
HINT-	XINTx-	Any external interrupt can be chosen.

The HPI is mapped using A[31:29] into one of the memory 8 regions. The selected memory region has to be configured as 16-bit wide.

The interface shown in Figure 19 is not using address latch enable to latch control signals. If ALE is used to latch the HPI control signals (ALE tied to HAS~) there is no enough time to generate and latch HCS~ signal, since the HCS~ has to be asserted prior to the falling edge of HAS~.

In this interface HAS~ is tied to the Vcc, and internal HSTROBE~ signal is generated by asserting the HCS~ or HDS1~ whichever come first (HDS1~ is tied to DEN~).

The HCS~ signal is asserted and latched on the rising edge of the CLKIN if i960 initiates address phase of a data transfer (ADS~ is asserted), and output from the Address Decoder is high.

To guarantee that timing requirement th(HSTBH-HDV) is met during an HPI write the internal HSTROBE is generated differently for a read and write cycles. During a read transfer, HSTROBE is asserted on rising edge of SYSCLK when address is matched and ADS- is low. HSTROBE is negated when synchronized HRDY indicates ready status. During a write transfer synchronized HRDY is used to de-assert HSTROBE while synchronized HRDY delayed for one clock is used to generate ready signal for i960. This way i960 holds the data on the bus, and ends the transfer one clock after HSTROBE is negated. This is done in order to meet data hold-timing requirement of the HPI.

The 80960 local bus is a synchronous interface for burst transactions. However, the 80960 host can perform only non-burst HPI transactions (HPI is asynchronous interface).

Configuration

The only programmable physical memory attribute for the i960Jx microprocessor is the bus width, which can be 8-, 16- or 32-bits wide.

For the purposes of assigning memory attributes, the physical address space is partitioned into 8, fixed 512 MByte regions determined by the upper three address bits. The physical memory attributes for each region are programmable through the PMCON registers. The PMCON registers are loaded from the Control Table. The i960 Jx microprocessor provides one PMCON register for each region.

The bus width for a region is controlled by the BW[1:0] bits in the PMCON register. The BW1=0 and BW0= 1 for 16-bit HPI interface.

All eight PMCON registers are loaded automatically during system auto-initialization. Immediately after a hardware reset, the PMCON register contents are marked invalid in the Bus Control (BCON) register. The initial PMCON register values are stored in the Control Table in the Initialization Boot Record. After hardware reset the processor first loads all PMCON registers from the Control Table. The processor then loads BCON from the Control Table. The BCON.ctv bit in BCON has to be set in order to use the programmed PMCON values for each memory region.

The Default Logical Memory Configuration register (DLMCON) provides default logical memory control for those accesses which do not fall within a region defined by the logical memory control register pairs. On the 80960Jx, the byte order programmed in the DLMCON register controls byte ordering for the entire 32-bit memory space.

The interrupt controller register of the 80960 Jx processors controls basic functionality such as interrupt mode, signal detection, global enable/disable, mask operation, interrupt vector caching, and sampling mode (for more detailed information on interrupt configuration please see the I960 Jx User's Manual).

80960JD to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) an 80960JD write to HPI and 2) an 80960JD read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 20.   80960JD reads internal memory of the TMS320C6201/6701 using the HPI (read without auto-increment).

Figure 21. 80960JD Write to HPI
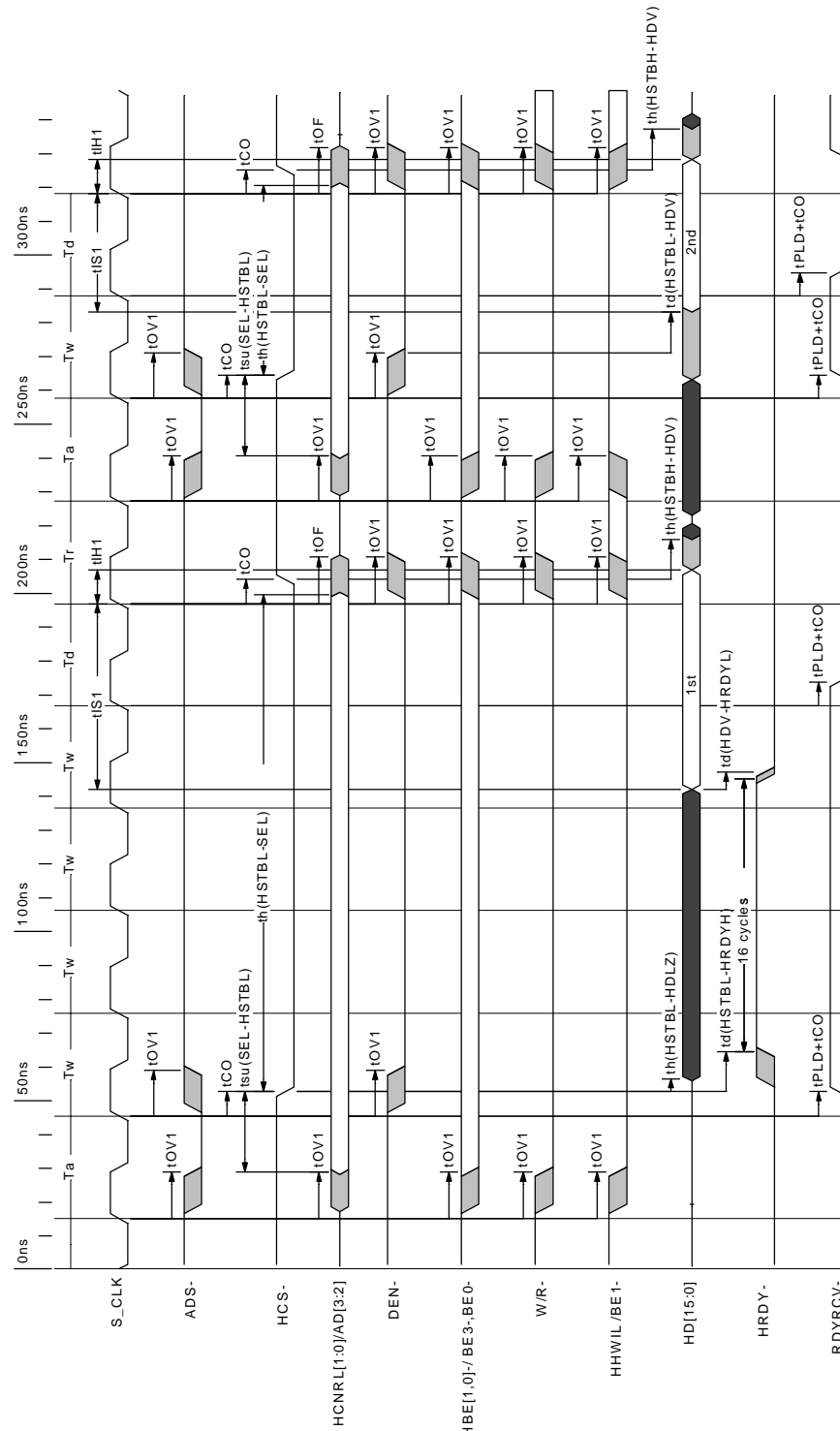
Table 28.   Timing Requirements for HPI

HPI Symbol	80960JD Symbol	Parameter	Min HPI [ns]	Min 80960JD [ns]
tw(HSTBL)	$2tcyc^@$	Pulse width of HDS-low.	10	60
tsu(SEL-HSTBL)	$tcyc^@$	Setup time, Select Signals valid before HSTROBE-low.	1	19
th(HSTBL-SEL)	$2tcyc^@$	Hold time, Select Signals valid after HSTROBE-low.	2	60
tsu(HD-HSTBH)	$2tcyc^@ - tOV1+tCO$	Setup time, Host Data valid before HDS-high.	1	53.5
th(HSTBH-HD)	$tcyc^@ - tCO+tOF$	Hold time, Host Data valid after HDS-high.	1	36.5

Table 29.   Timing Requirements for 80960JD

HPI Symbol	80960JD Symbol	Parameter	Min HPI [ns]	Min 80960JD [ns]
$>tcyc^@$	tIS1	Input Setup to CLKIN - AD[31:0]	30	6
tOV1+th(HSTBH-HDV)	tIH1	Input hold from CLKIN - AD[31:0]	5.5	1.5
$tcyc^@ - tCO-tPLD$	tIS2	Input Setup to CLKIN – RDYRCV	23	6.5
$tcyc^@$	tIH2	Input hold from CLKIN – RDYRCV	30	1

@ tcyc denotes one clock cycle time of 80960JD. At 33 MHz operating frequency, tcyc=30 ns. tCO denotes PLD propagation.

In Figures and Tables above tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output respectively for PALLV16V8.

In Figures 20 and 21 timing parameters are named in the same way as those in the TMS320C6201/C6701's and i960JD's datasheets. Actual timing parameter values are listed in the Appendix.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of Intel 80960JD and HPI. This interface is based on an Intel 80960JD-30 MHz device and a TMS320C6201 device at any frequency ranging from 100-200 MHz or C6701 device at any frequency up to 167MHz.

80960RP to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) an 80960RP write to HPI and 2) an 80960RP read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables (timing diagrams look similar to the ones shown in Figure 20 and Figure 21).

Table 30.   Timing Requirements for HPI

HPI Symbol	80960RP Symbol	Parameter	Min HPI [ns]	Min 80960RP [ns]
tw(HSTBL)	$2tcyc^@$	Pulse width of HDS- low.	10	60
tsu(SEL-HSTBL)	$tcyc^@$	Setup time, Select Signals valid before HSTROBE- low.	1	19
th(HSTBL-SEL)	$2tcyc^@$	Hold time, Select Signals valid after HSTROBE- low.	2	60
tsu(HD-HSTBH)	$2tcyc^@$ - tOV1+tCO	Setup time, Host Data valid before HDS- high.	1	53.5
th(HSTBH-HD)	$tcyc^@$ - tCO+tOF	Hold time, Host Data valid after HDS- high.	1	36.5

Table 31.   Timing Requirements for 80960RP

HPI Symbol	80960RP Symbol	Parameter	Min HPI [ns]	Min 80960RP [ns]
$>tcyc^@$	tIS1	Input Setup to S_CLK - AD[31:0]	30	5
tOV1+th(HSTBH-HDV)	tIH1	Input hold from S_CLK - AD[31:0]	5.5	2
$tcyc^@$ - tCO-tPLD	tIS2	Input Setup to CLKIN – RDYRCV	23	10
$tcyc^@$	tIH2	Input hold from CLKIN – RDYRCV	30	2

@ tcyc denotes one clock cycle time of 80960RP. At 33 MHz operating frequency, tcyc=30 ns.

In Figures 23 and 24 timing parameters are named in the same way as those in the TMS320C6201/6701's and i960RP's data-sheets. Actual timing parameter values are listed in the Appendix.

In Tables above tPLD and tCO represent the propagation time from input to combinatorial output, and propagation time from the clock to output respectively for PALLV16V8.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of Intel 80960RP and HPI. This interface is based on an Intel 80960RP-30 MHz device and a TMS320C6201 device at any frequency ranging from 100-200 MHz or TMS320C6701 at any frequency up to 167MHz.

Host Port Interfaces to the PCI Bus

This section will describe interface between TMS320C6201/6701 Host Port and the most popular PCI interface chips. This includes a schematic showing connections between the two devices and verification that timing requirements are met for each device.

PLX PCI9050

The PCI 9050-1 provides a compact high performance PCI bus target (slave) interface for adapter boards. The PCI 9050-1 is designed to connect a wide variety of local bus designs to the PCI bus. The PCI 9050-1 can be programmed to connect directly to the multiplexed or non-multiplexed 8, 16, or 32 bit local bus. The 8- and 16-bit modes enable easy conversion of ISA designs to PCI. The PCI 9050-1 contains a bidirectional FIFO to speed match the 32-bit wide, 33 MHz PCI bus to a local bus, which may be narrower or slower. Up to five local address spaces and up to four chip selects are supported.

PCI9050 Interface

Voltage conversion is required between PCI9050 and TMS320C6201/6701 since PCI9050 requires a 5V to operate, and TMS320C6201/6701 is a 3V device. Voltage conversion can be accomplished by SN74CBTD3384 bus switch. The SN74CBTD3384 is a 10-bit straight through switch with inputs on one side and outputs on the opposite side of the package. The basic bus switch is a NMOS device with the substrate connected to ground thus allowing bi-directional data flow through the channel. To make this device into a voltage translator the 5V Vcc is lowered to 4.3V through an internal diode. The 3.3V bus is established because the NMOS bus switch requires a gate-to-source voltage of 1V to conduct.

Figure 22 is a diagram of the HPI to PCI9050 connections. The PCI9050 local bus is programmed to be non-multiplexed (MODE pin is low).

Figure 22.   PCI9050 to HPI Interface Block Diagram
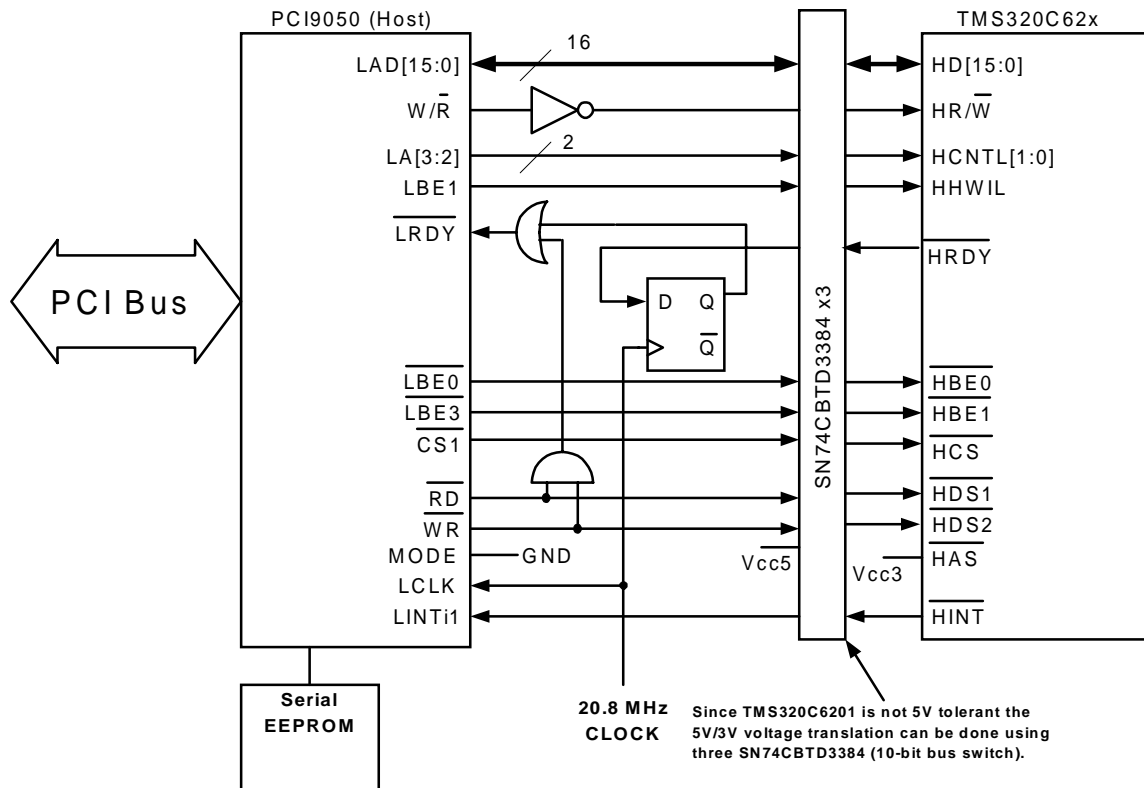
Table 32. PCI9050 to HPI Pin Connections

HPI Pin	PCI9050 Pin	Comments
HCNTL[1:0]	LA[3:2]	Address bits of PCI9050 are used as control signals.
HHWIL	LBE1	LBE1 identifies the first or second half-word of transfer.
HR/W-	Inverted W/R-	Indicates a read or write access. Since the C6201/6701 HPI port has a read-write (HR/W~) line which has the opposite polarity of PCI9050's read-write pin, an inverter is used to connect these two lines.
HD[15:0]	LAD[15:0]	16 LSBs of data.
HDS1-	RD-	HDS1- is connected to the RD-
HDS2-	WR-	HDS2- is connected to the WR-
HAS-	Vcc	Address Latch Enable is not used in this interface.
HCS-	CS1-	HCS- can be connected to any of CS- output lines of the PCI9050.
HBE0-	LBE0-	HPI uses this value on writes only.
HBE1-	LBE3-	HPI uses this value on writes only.
HRDY-	LRDY-	Asynchronous HPI ready output is synchronized and connected to the LRDY~.
HINT-	XINTx-	Any external interrupt can be chosen.

The PCI9050 has no Direct Master capability on the PCI bus. The internal registers are accessible from the Host CPU on the PCI bus or from the serial EEPROM.

Configuration shown does not support the PCI9050 burst mode.

Configuration

During power up, the PCI RST_ signal resets the default values of the PCI9050 internal registers. In return, the PCI9050 outputs the local reset signal (LRESET_) and checks for existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word is not FFFF, the PCI9050 loads the internal registers for the serial EEPROM. Otherwise, default values are used. The PCI9050 configuration registers can be written only by the optional serial EEPROM or the PCI host processor.

Five local address spaces (local spaces 0-3 and expansion ROM) are accessible from the PCI bus. In this example local space 1 is used. A set of four registers defines each space, defining the local bus characteristics:

- PCI Base Address

- Local Range

- Local Base Address (Remap)

- Local Bus Region Descriptor.

Local bus address space 1 region descriptor (LAS1BRD register) has to be set to:

- Disable Burst (LAS1BRD [0] = 0)

- Enable READY input (LAS1BRD [1] = 1).

- Disable BTERM input (LAS1BRD [2] = 0).

- Enable 16 bit bus width (LAS1BRD [23:22] = 01).

- Little Endian (LAS1BRD [24] = 0).

- The 9050-1 provides a write cycle hold parameter that should be used to extend the cycle for one clock after write strobe is de-asserted (LAS1BRD [31:30] =01, in order to extend a write cycle for one clock). This is done to meet data hold time requirement of the TMS320C6201/6701.

The wait states for READ strobe should be set to zero.

PCI9050 to HPI Timing Verification

To verify proper operation, two functions have been examined: 1) a PCI9050 write to HPI and 2) a PCI9050 read from HPI. In each instance, timing requirements were compared for each of the devices and the results are shown in the following tables and timing diagrams.

Figure 23.   PCI9050 Reads from TMS320C6201/6701's Internal Memory using the HPI.
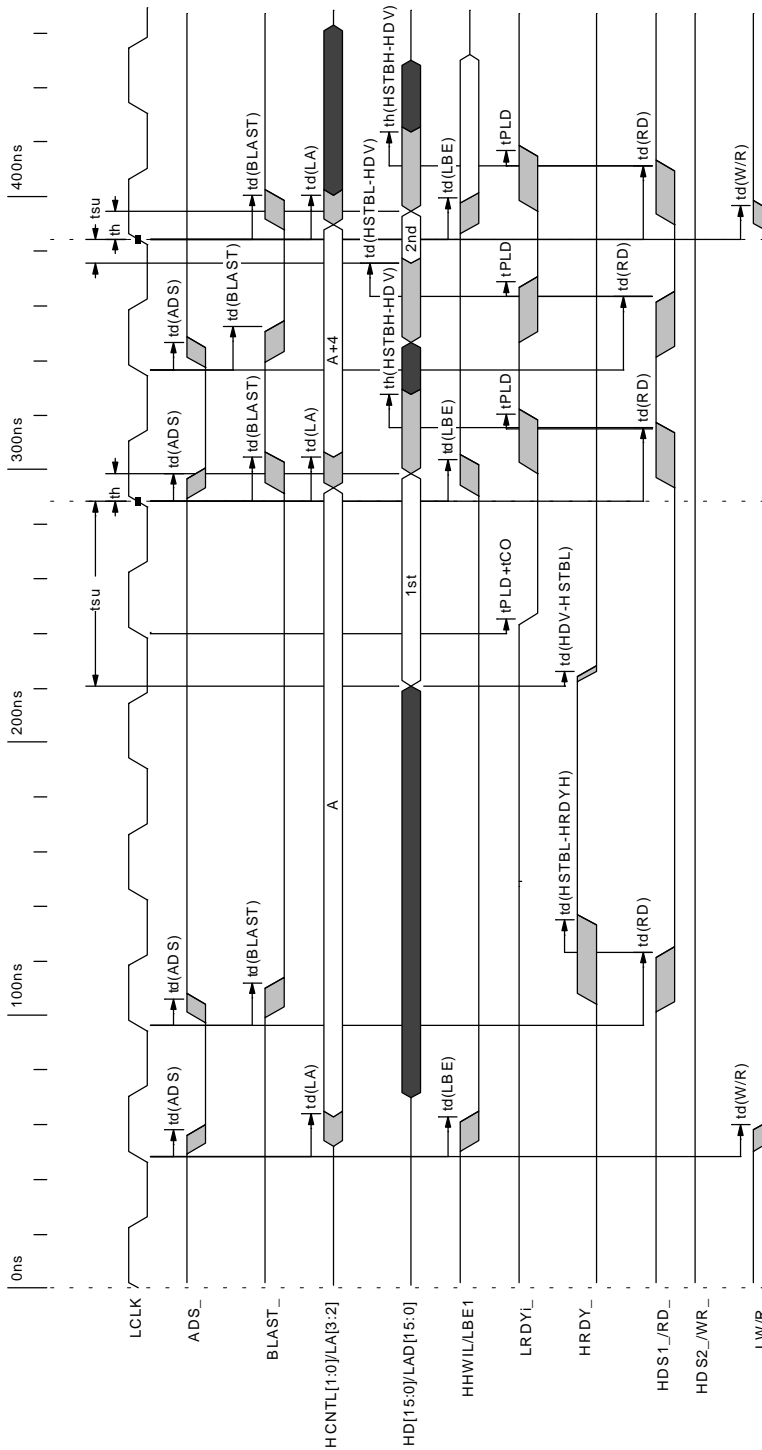
Figure 24. PCI9050 Writes to TMS320C6201/6701 using the HPI
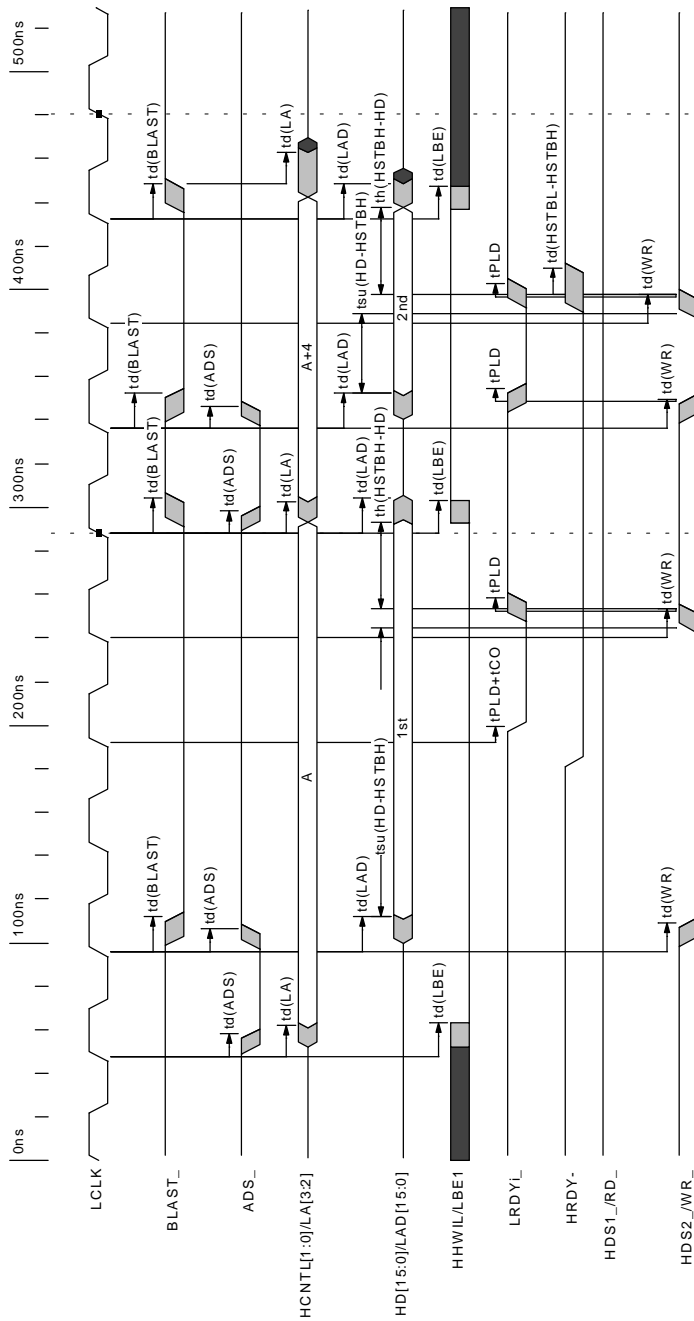
Estimated maximum transfer speed to the PCI bus is 9 Mbytes/s for writes and 11 Mbytes/s for reads. The speed limiting factor in the interface is the timing requirement td(RD) of the PCI9050-1.

Table 33. Timing Requirements for HPI

HPI Symbol	PCI9050 Symbol	Parameter	Min HPI [ns]	Min PCI9050 [ns]
tw(HSTBL)	tcyc$^@$	Pulse width of HDS- low.	10	48
tsu(SEL-HSTBL)	tyc$^@$ - td(LBE)+td(WR)	Setup time, Select Signals valid before HDS-.	1	37
th(HSTBL-SEL)	tyc$^@$ - td(RD)+td(LBE)	Hold time, Select Signals valid after HDS- low.	1	25
tsu(HD-HSTBH)	tyc$^@$ - td(LAD)+td(WR)	Setup time, Host Data valid before HDS- high. (WRITE SETUP TIME)	2	37
th(HSTBH-HD)	tyc$^@$ +td(LAD)- td(WR)	Hold time, Host Data valid after HDS- high.	1	40

Table 34. Timing Requirements for PCI9050

HPI Symbol	PCI9050 Symbol	Parameter	Min HPI [ns]	Min PCI9050 [ns]
tcyc$^@$-td(RD) – td(HSTBL-HDV)	Tsu	(READ SETUP TIME) Input Setup LAD[15:0] - LCLK	9	8
td(RD)+th(HSTBH-HDV)	Th	Input hold from LCLK - LAD[15:0]	10	2
tcyc@ - tCO-tPLD	Tsu	LRDYi valid to LCLK high –READY setup time.	43	8
td(RD)+tPLD	Th	LCLK high to LRDYi invalid –READY hold time	12	2

@ tcyc denotes one clock cycle time of PCI9050 Local Bus. At 20.8 MHz operating frequency, tcyc=48 ns.

The tables and timing diagrams above show that the timing parameters for both devices are met in the interface of PLX PCI9050 and HPI. The PCI9050 local bus, in this example operates at 20.8 MHz while a TMS320C6201 device operates at any frequency ranging from 100-200 MHz (C6701 device can operate at frequencies up to 167MHz).

APPENDIX A   TMS320C6201 Timing Requirements

Table 35.   TMS320C6201 Host Port Timing Requirements

Characteristic	Symbol	Min [ns]	Max [ns]
Pulse width of HSTROBE_ high between consecutive accesses.	tw(HSTBH)	2 Tcyc[f]	
Hold time, HSTROBE_ low after HRDY_ low.	th(HRDY-HSTBL)	1	
Pulse width of strobe low.	tw(HSTBL)	2 Tcyc[f]	
Delay Time, HCS_ to HRDY_.	td(HCS-HRDY)	1	7
Setup time, Select signals valid before HSTROBE_ low.	tsu(SEL-HSTBL)	1	
Hold time, Select signals valid after HSTROBE_ low.	th(HSTBL-SEL)	2	
Setup time, Select signals valid before HAS_ low.	tsu(SEL-HASL)	1	
Hold Time, Select signals valid after HDS_ low.	th(HASL-SEL)	2	
Setup time, Host data valid before HSTROBE_ high.	tsu(HD-HSTBH)	1	
Hold Time, Host Data valid after strobe HSTROBE_ high (write).	th(HSTBH-HD)	1	
Hold time, Host data valid after HSTROBE_ high (HPI read).	th(HSTBH-HDV)	3	12
Hold time, Host data low impedance after HSTROBE_ low.	th(HSTBL-HDLZ)	4	
Delay time, HSTROBE_ high to Host Data not driven.	td(HSTBH-HDHZ)	3	12
Delay time, HSTROBE_ low to HRDY_ high.	td(HSTBL-HRDYH)	3	12
Delay time, Host Data valid to HRDY_ low.	td(HDV-HRDYL)	Tcyc[f] −2	Tcyc[f]
Delay Time, Data valid after HSTROBE_ low	td(HSTBL-HDV)	3	12
Delay time, HSTROBE_ high to HRDY_ high.	td(HSTBH-HRDYH)	3	12

[f] Tcyc = (1/ clock frequency) [ns]

Table 36.   Timing Requirements for Asynchronous Memory Cycles (TMS320C6201)

Characteristic	Symbol	Min [ns]	Max [ns]
Delay Time, CLKOUT1 high to CE_ valid.	td(CK1H-CE)	0.4	2.5
Delay time, CLKOUT1 high to BE_ valid.	td(CK1H-BE)	0.4	2.5
Delay time, CLKOUT1 high to EA valid.	td(CK1H-EA)	0.4	3.3
Delay time, CLKOUT1 high to ED low impedance.	td(CK1H-EDLZ)	1.6	
Delay time, CLKOUT1 high to ED valid.	td(CK1H-EDV)		3.7
Hold time, CLKOUT1 high to ED invalid.	th(CK1H-EDIV)	0.9	
Delay time, CLKOUT1 high to ED high impedance.	td(CK1H-EDHZ)		6.5
Delay time, CLKOUT1 high to AOE_ valid.	td(CK1H-OE)	0.4	2.5
Delay time, CLKOUT1 high to ARE_ valid.	td(CK1H-ARE)	0.4	2.5
Delay time, CLKOUT1 high to AWE_ valid.	td(CK1H-AWE)	0.4	2.5
Setup time, read D before CLKOUT1 high.	tsu(ED-CK1H)	5	
Hold time, read D valid after CLKOUT1 high.	th(CK1H-ED)	0	
Setup time, ARDY before CLKOUT1 high.	tsu(ARDY-CK1H)	5	

Hold time, ARDY valid after CLKOUT1 high.	th(CK1H-ARDY)	0

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the TMS320C6201 Data Sheet.

APPENDIX B   MC68302 Timing Requirements

Table 37.   Motorola MC68302 Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
Clock High to FC, Address Valid [6]	tCHFCADV	0	30
Clock High to Address, Data Bus High Z [7]	tCHADZ		33
Clock High to Address [8]	tCHAFI	0	
Clock High to AS-,DS- asserted [9]	tCHSL	3	20
Address, FC valid to AS-, DS- asserted [11]	tAFCVSL	10	
Clock low to AS-,DS- negated [12]	tCLSH		20
AS-,DS- negated to Address [13]	tSHAFI	10	
AS-, DS- width negated [14]	tSL	80	
DS- width asserted [14A]	tDSL	40	
AS-, DS- width negated [15]	tSH	40	
AS-, DS- negated to R/W- invalid [17]	tSHRH	10	
Clock high to R/W- high [18]	tCHRH		20
Clock high to R/W- low [20]	tCHRL		20
AS- asserted to R/W- Low (Write) [20A]	tASRV		7
Address FC Valid to R/W- Low (Write) [21]	tAFCVRL	10	
R/W- Low to DS- Asserted (Write) [22]	tRLSL	20	
Clock Low to Data Out Valid [23]	tCLDO		20
AS-, DS-, negated to Data Out Invalid (Write) [25]	tSHDOI	10	
Data Out Valid to DS- asserted (write) [26]	tDOSL	10	
Data In Valid to Clock Low [27]	tDICL	5	
AS-,DS- negated to DTACK- negated (Async .hold) [28]	tSHDAH	0	75
AS-,DS- Negated to Data In invalid (Hold time on read) [29]	tSHDII	0	
DTACK- asserted to Data In valid (Setup time) [31]	tDALDI		33
Async.Setup Time [47]	tASI	7	
Data Out hold from clock high [53]	tCHDOI	0	
R/W- Asserted to Data Bus Impedance change [55]	tRLDBD	0	
Clock High to CS-, IACK- Low [150]	tCHCSIAKL	0	27
Clock Low to CS-, IACK- High [151]	tCLCSIAKH	0	27
CS- Width negated [152]	tCSH	40	
Clock high to DTACK- Low (0 Wait State) [153]	tCHDTKL		30
Clock Low to DTACK- low (1-6 Wait States) [154]	tCLDTKL		20
Clock Low to DTACK- high [155]	tCLDTKH		27
Input Data Hold Tome From S6 Low [171]	tIDHCL	5	
CS- Negated to Data Out Invalid (write) [172]	tCSNDOI	7	
Address, FC valid to CS- Asserted [173]	tAFVCSA	15	
CS- negated to Address, FC Invalid [174]	tCSNAFI	12	
CS- Low Time [175]	tCSLT	80	

CS- Negated to R/W- Invalid [176]	tCSNRWI	7	
CS- Asserted to R/W- Low (write) [177]	tCSARWL		8
CS- Negated to Data-In Invalid (Hold Time on Read) [178]	tCSNDII	0	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the MC68302 User's Manual.

APPENDIX C   MC68360 Timing Requirements

Table 38.   Motorola MC68360 Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
CLKO1 High to Address, FC valid [6]	tCHAV	0	15
CLKO1 High to Address, FC Invalid [8]	tCHAZn	0	
CLKO1 Low to CS- Asserted [9]	tCLSA	4	16
AS to DS or CS- Asserted [9A]	tSTSA	-6	6
AS to CS- Asserted [9C]	tSTCA	14	26
Address valid to AS,CS-,OE Asserted [11]	tAVSA	10	
CLKO1 Low to CS- Negated [12]	tCLSN	4	16
AS,DS,CS-,OE,WE Negated to Address, FC Invalid (Address Hold) [13]	tSNAI	10	
AS,CS-,OE and DS (read) width asserted [14]	tSWA	75	
AS,DS,CS-,OE width negated [15]	tSN	35	
CLKO1 High to AS,DS,R/W- High Impedance [16]	tCHSZ		40
AS,DS,CS-,WE negated to R/W High [17]	tSNRN	10	
CLKO1 High to R/W High [18]	tCHRH	0	20
CLKO1 High to R/W Low [20]	tCHRL	0	20
R/W High to AS,CS-, OE Asserted [21]	tRAAA	10	
R/W- Low to DS- Asserted (Write) [22]	tRASA	47	
CLKO1 High to Data-Out Valid [23]	tCHDO		23
DS,CS-,WE Negated to Data-Out Invalid (Data Out hold) [25]	tSNDOI	10	
Data Out valid to DS Asserted (write) [26]	tDVSA	10	
Data In to CLKO1 Low (Data setup) [27]	tDICL	1	
AS,DS, negated to DSACK- Negated [28]	tSNDN	0	50
DS,CS-,OE Negated to Data In invalid (Data In hold) [29]	tSNDI	0	
DS,CS-,OE negated to DAta In high Z [29A]	tSHDI		40
DSACK- Asserted to DSACK- valid (Skew) [31A]	tDADV		10
R/W- width asserted (write or read) [46]	tRWA	100	
Async Input Setup Time [47A]	tAIST	5	
Async Input Hold Time [47B]	tAIHT	10	
Data Out from CLKO1 High [53]	tDOHC	0	
CLKO1 High to Data-Out high Z [54]	tCHDH		20
R/W Asserted to Data Bus Impedance Change [55]	tRADC	25	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the MC68360 User's Manual.

APPENDIX D MPC750 Timing Requirements

Table 39. PowerPC MPC750 Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup)	B10a	2.5	
All other inputs valid to SYSCLK (Input Setup).	B10b	3	
SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold).	B11a	1	
SYSCLK to all other inputs Invalid (Input Hold).	B11b	1	
SYSCLK to Output Driven (Output Enable Time)	B12	0.5	
SYSCLK to Output Invalid (Output Hold)	B15	1	
SYSCLK to Output High Impedance.	B16		6
SYSCLK to all other Outputs valid	B14		6.5
SYSCLK to Output Valid (TS-, ABB-,DBB-)	B13		6.5

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the MPC750 User's Manual.

APPENDIX E   MPC860 Timing Requirements

Table 40.   Motorola MPC860 Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
CLKOUT to A[0:31], RD/WR-,D invalid	B7	5	
CLKOUT to A(0:31), RD/WR-,D(0:31),DP(0:3) Valid	B8		13
CLKOUT to A(0:31),RD/WR-,D(0:31) High-Z	B9	5	13
CLKOUT to TS-,BB- Assertion	B11	5	13
CLKOUT to TS-,BB- negation	B12	5	13
Data, DP valid to CLKOUT Rising Edge (Setup Time)	B18	6	
CLKOUT Rising edge to Data, DP Valid (Hold time)	B19	1	
CLKOUT Falling Edge to CS- Asserted (GPCM ACS=11,TRLX=0)	B22B	5	13
CLKOUT Rising Edge to CS- Negated –GPCM-Read Access	B23	2	8
A(0:23) to CS- Asserted -GPCM- ACS=11,TRLX=0	B24A	8	
CLKOUT Rising Edge to OE-,WE-(0:3) Asserted	B25		9
CLKOUT Rising Edge to OE- Negated	B26	2	9
CLKOUT Rising edge to WE(0:3)- Negated -GPCM- write Access, CSNT=0	B28		9
CS- negated to Data Hi-Z (write access) CSNT=0	B29B	3	
WE(0:3)- Negated to D Hi-Z -GPCM-Write Access, CSNT=0	B29	3	
CS-,WE(0:3)- Negated to A(0:31) Invalid -GPCM- Write Access	B30	3	
CLKOUT to TA-,BI- Assertion	B11A		10
CLKOUT to TA-,BI- Negation	B12A		11
CLKOUT to TA- BI- Hi-Z	B13A		15
TA- valid to CLKOUT (setup time)	B16	7	
CLKOUT to TA- (hold time)	B17	2	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the MPC860 User's Manual.

APPENDIX F   I960JD Timing Requirements

Table 41.   Intel 80960JD Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
Output valid delay, except ALE inactive and DT/R- for 3.3V input signals	tOV1	2.5	13.5
Output float delay	tOF	2.5	13.5
input setup to CLKIN- AD[31:0]	tIS1	6	
Input Hold from CLKIN AD[31:0]	tIH1	1.5	
Input setup to CLKIN RDYRCV-	tIS2	6.5	
Input hold from CLKIN RDYRCV-	tIH2	1	
Address valid to ALE Inactive	tLX	10	
ALE width	tLXL	8	
Address hold from ALE inactive	tLXA	8	
DT/R- valid to DEN- active	tDXD	8	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the I960JD User's Manual.

APPENDIX G   I960RP Timing Requirements

Table 42.   Intel 80960RP Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
Output valid delay, except ALE inactive and DT/R- for 3.3V input signals	tOV1	3	15.5
Output float delay	tOF	3	13
input setup to CLKIN- AD[31:0]	tIS1	5	
Input Hold from CLKIN AD[31:0]	tIH1	2	
Input setup to CLKIN RDYRCV-	tIS2	10	
Input hold from CLKIN RDYRCV-	tIH2	2	
ALE width	tLXL	4.5	
Address hold from ALE inactive	tLXA	4.5	
DT/R- valid to DEN- active	tDXD	4.5	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the I960RP User's Manual.

APPENDIX I   PCI9050 Timing Requirements

Table 43.   PLX PCI9050 Timing Parameters

Characteristic	Symbol	Min [ns]	Max [ns]
Local Bus Address Strobe.	td(ADS)	3	10
Local Bus Burst Last Signal.	td(BLAST)	5	16
Local Bus Address.	td(LA)	5	14
Local Bus Data.	td(LAD)	5	16
Local Bus Byte Enables.	td(LBE)	4	15
Local Bus Write Control Signal	td(WR)	4	13
Local Bus Read Control Signal.	td(RD)	7	27
Local Bus W/R_ Control Signal.	td(W/R)	4	12
Local Bus Input Setup Time.	Tsu		8
Local Bus Input Hold Time.	Th	2	

The timing requirements are given here only for a quick reference. For detailed description, notes and restrictions please refer to the PCI9050 User's Manual.

References

TMS320C62x/C67x Peripherals Reference Guide

TMS320C6201 DSP Data Sheet

TMS320C6701 DSP Data Sheet

MC68302 Integrated Multiprotocol Processor User's Manual

MC68360 Quad Integrated Communications Controller User's Manual

MPC860 User's Manual

PowerPC Microprocessor Family: The Bus Interface for 32-bit Microprocessors

MPC750 User's Manual

Intel 80960JD User's Manual

Intel 80960RP User's Manual

PLX PCI9050 Data-Sheet.