TMS320 DSP
Number 0.01
DESIGNER'S NOTEBOOK
PRELIMINARY

TMS320C6x Interface to External SBSRAM

Contributed by Kyle Castille

Design Problem

Configuring the TMS320C62xx and external SBSRAM for proper operation

Solution

Interfacing external SBSRAM to the TMS320C62xx is simple when compared to previous generations of TI DSPs due to the advanced External Memory Interface (EMIF), which provides a glueless interface to a variety of external memory devices.

This document will describe the:

- EMIF's control registers and SBSRAM signals
- SBSRAM functionality and performance considerations
- Full example using ISSI's IS61SP12836 SBSRAM (128k x 36) with full speed SSCLK
- Full example using Micron's MT58LC64K32G1 SBSRAM (32k x 32) with half speed SSCLK

Overview of EMIF

EMIF Signal Descriptions

Figure 1 shows a block diagram of the EMIF, the interface between external memory and the other internal units of the 'C6x. The interface with the processor is provided via the DMA controller, Program Memory Controller (PMC), and the Data Memory Controller (DMC)[1]. The signals described in Table 1 describe the SBSRAM interface and the shared interface signals.

[1] For a more detailed description of the interface between the EMIF and the other internal units of the C6x, see the TMS320C62xx Peripherals Reference Guide.

Figure 1. Block Diagram of EMIF SBSRAM Interface

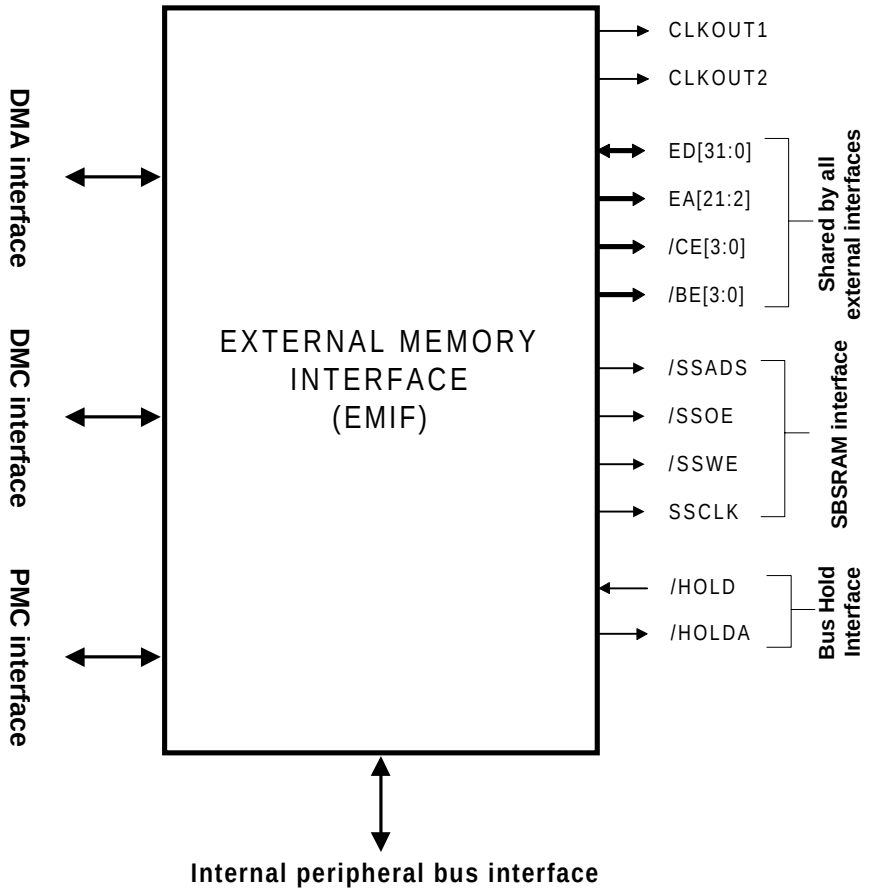


Table 1. EMIF Signal Descriptions : Shared Signals and SBSRAM Signals

Pin	(I/O/Z)	Description
CLKOUT1	O	Clock. Clock output - the CPU clock rate.
CLKOUT2	O	Clock. Clock output - ½ the CPU clock rate.
ED[31:0]	I/O/Z	Data I/O. 32-bit data input/output from external memories and peripherals.
EA[21:2]	O/Z	External Address output. Drives bits 21-2 of the byte address.
/CE0	O/Z	External /CE0 Chip Select. Active low chip select for CE space 0.
/CE1	O/Z	External /CE1 Chip Select. Active low chip select for CE space 1.
/CE2	O/Z	External /CE2 Chip Select. Active low chip select for CE space 2.
/CE3	O/Z	External /CE3 Chip Select. Active low chip select for CE space 3.
/BE[3:0]	O/Z	Byte Enables. Active low byte strobes. Individual bytes and halfwords can be selected for both read and write cycles. Decoded from bits 1:0 of the byte address.
/SSADS	O/Z	Active-low address strobe/enable for SBSRAM interface.
/SSOE	O/Z	Output buffer enable for SBSRAM interface.
/SSWE	O/Z	Active-low write enable for SBSRAM interface.
SSCLK	O/Z	SBSRAM interface clock. Equivalent to CLKOUT1 or CLKOUT2 as selected by the user.
/HOLD	I	Active-low external bus hold (3-state) request.
/HOLDA	O	Active-low external bus hold acknowledge.

EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory mapped registers within the EMIF. A write to any EMIF register will not complete until all pending EMIF accesses which use that register have completed. The memory mapped registers are shown in Table 2.

Table 2. EMIF Memory Mapped Registers for SBSRAM

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control

EMIF Global Control Register

The EMIF Global Control Register (Figure 2) configures parameters common to all the CE spaces. Table 3 only lists those parameters that are relevant for use with SBSRAM.[2]

Figure 2. EMIF Global Control Register Diagram

31 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	SDCINV	CLK2INV	rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
R, +0	RW, +1	RW, +1	R, +0	R, +x	R, +x	R, +0	RW, +0	RW, +1	RW, +1	RW, +1	RW, +1	RW, +0	RW, +0	R, +x

[2] For a description of all of the parameters of the EMIF Global Control Register, see the TMS320C62xx Peripherals Reference Guide.

Table 3. EMIF Global Control Register Bit Field Description for SBSRAM

Field	Description
SSCEN	SSCLK enable
	SSCEN=0, SSCLK held high
	SSCEN=1, SSCLK enabled to clock
SSCRT	SBSRAM clock rate select
	SSCRT=0, SSCLK ½x CPU clock rate
	SSCRT=1, SSCLK 1x CPU clock rate

CE Space Control Registers

The four CE Space Control Registers (Figure 3) correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or Asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. The only field of interest for SBSRAM is the MTYPE field, which should be set to 100b to indicate 32 bit wide SBSRAM in the corresponding CE space. Modification of a CE Space Control Register does not occur until that CE space is inactive.

Figure 3. EMIF CE(0/1/2/3) Space Control Register Diagram

31–28	27–22	21–20	19–16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
RW, +1111	RW, +111111	RW, +11	RW, +1111

15–14	13–8	7	6–4	3–2	1–0
TA	READ STROBE	rsv	MTYPE	reserved	READ HOLD
RW, +11	RW, +111111	R, +0	RW, +010	R, +0	RW, +11

SBSRAM Interface

As shown in Figure 4, the EMIF interfaces directly to 32 bit wide industry standard synchronous burst SRAMs. This memory interface allows a high speed memory interface without some of the limitations of SDRAM. Most notably, since SBSRAMs are SRAM devices, random accesses in the same direction may occur in a single cycle. The SBSRAM interface may run at either the CPU clock speed or at ½ of this rate. The selection is made based on the setting of the SSCRT bit in the EMIF Global Control Register.

The four SBSRAM control pins are latched by the SBSRAM on the rising SSCLK edge to determine the current operation. These signals are only valid if the chip select line for the SBSRAM is low. The /ADV signal is used to allow the SBSRAM device to generate addresses internally for interfacing to controllers which cannot provide addresses quickly enough, but the EMIF does not need to use this signal because it generates the addresses at the required rate.

Figure 4. EMIF-SBSRAM Interface

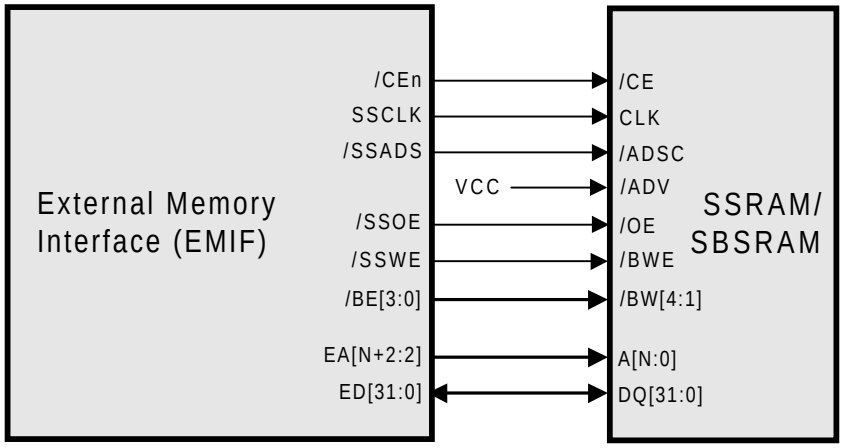


Table 4. EMIF SBSRAM Pins

EMIF Signal	SBSRAM Signal	SBSRAM Function
/CEn	/CE	Chip Enable. /CE must be active (low) for a command to be clocked into the SBSRAM.
SSCLK	CLK	SBSRAM Clock. Runs at either 1x or 1/2x the CPU rate.
SSADS	/ADSC	Synchronous Address Status Controller: Causes a new external address to be registered. If /CE is active, then a READ or WRITE is performed.
/SSOE	/OE	Output Enable. Enables the data I/O drivers.
/SSWE	/BWE	Write Enable. Permits write operations.
/BE[3:0]	/BW[4:1]	Byte Write Enables. Allow individual bytes to be written when /BWE is active. A Byte Write Enable is LOW for a WRITE and HIGH for a READ cycle. /BW1 controls Byte 1, /BW2 controls Byte 2, /BW3 controls Byte 3, and /BW4 controls Byte 4.
EA[N+2:2]	A[N:0]	Address Inputs. Registered on rising edge of CLK.
ED[31:0]	DQ[32:1]	Data I/O. Byte 1 is DQ[8:1], Byte 2 is DQ[16:9], Byte 3 is DQ[24:17], and Byte 4 is DQ[32:25].

As mentioned, the SSCRT (SBSRAM Clock Rate Select) bit in the EMIF Global Control Register can configure SSCLK to operate at either full speed (SSCLK = CLKOUT1) or half speed (SSCLK = CLKOUT2 = ½ CLKOUT1). However, different advantages and disadvantages are associated with each configuration.

The biggest disadvantage for the Full Speed Interface is that the CPU runs at the same clock rate as the SBSRAM. Since, SBSRAMs are common at speeds up to 133 MHz and are emerging in the 166 MHz range, the CPU will not be able to operate at its peak rate, which is 200 MHz. Therefore, if the improvement in the memory access time is worth the sacrifice in CPU speed, then a full speed interface should be used.

However, if a half rate interface is used, then the CPU clock rate can be operated at the peak speed of 200 MHz, giving a slightly slower SSCLK rate of 100 MHz.

When either full speed or half speed interfaces are used, it is important to verify that the timing parameters of the SBSRAM meet the requirements of the ‘C6x.

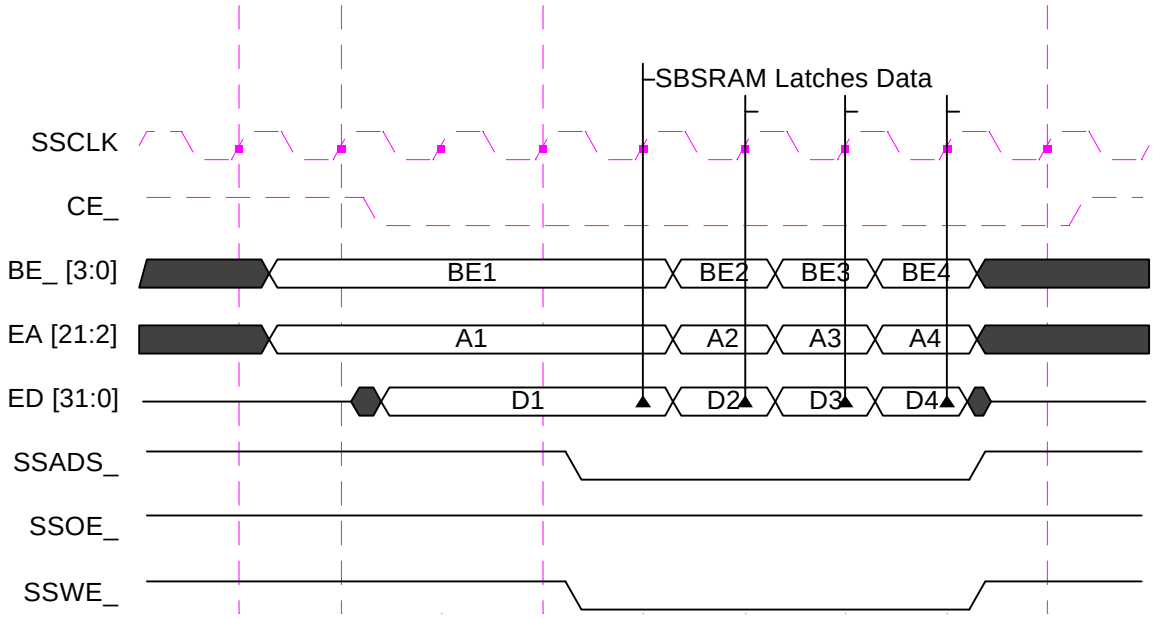
Full Speed

SBSRAM Write

Figure 5 shows a 4 word write of an SBSRAM with SSCLK = CLKOUT1. Every access strobes a new address into the SBSRAM. The first access requires an initial startup penalty of 3 cycles; thereafter all access can occur in a single SSCLK cycle. This startup penalty is to ensure that there is no contention over the data bus due to a previous read.

For an SBSRAM write at full speed, notice that the outputs from the ‘C6x (control, address, and data signals) are triggered after the rising edge of SSCLK. Since the SBSRAM latches the inputs on the rising edge of SSCLK, this gives almost a full cycle of setup time for the inputs to the SBSRAM.

Figure 5. SBSRAM Write - Full Speed



SBSRAM WRITE TIMING

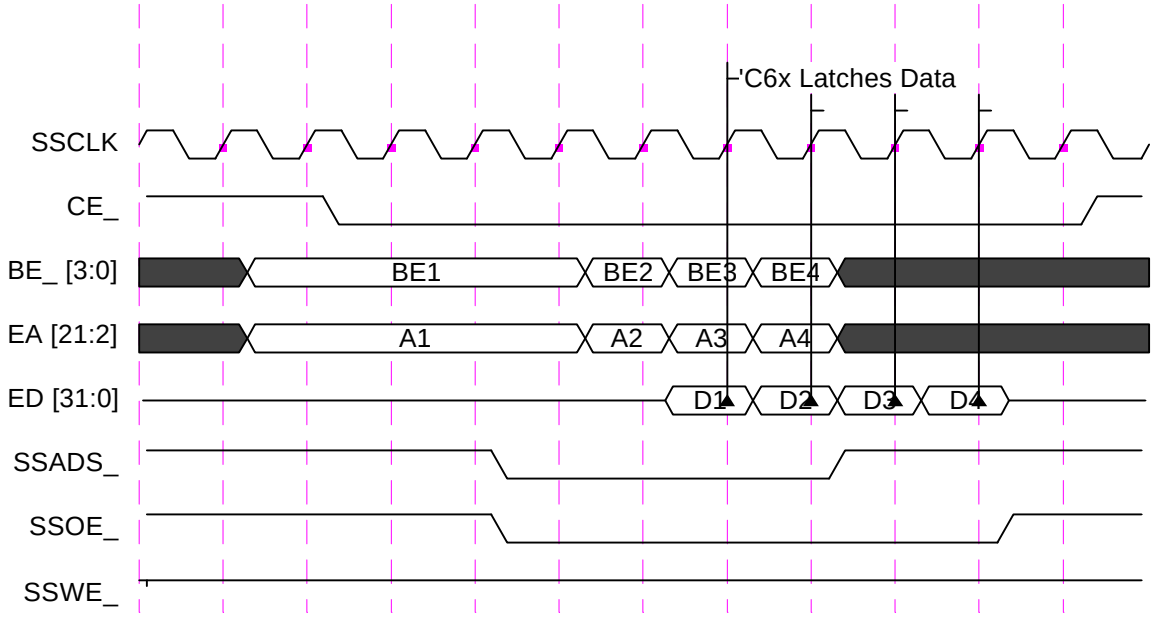
SBSRAM Read

Figure 6 shows a 4 word read of an SBSRAM at full speed (SSCLK = CLKOUT1). Every access strobes a new address into the SBSRAM, indicated by the /SSADS strobe low. The first access requires a delay of 2 cycles before the data is present on the bus; thereafter single cycle throughput is achieved.

The control and address signals for a full speed read are triggered off of the rising edge, and have the same timing constraints as for a full speed write.

The read data being output from the SBSRAM is also triggered by the rising edge of the SSCLK. Since the 'C6x latches the data on the rising edge of SSCLK, this gives almost a full cycle of setup time for the inputs to the C6x (less the access time of the SBSRAM).

Figure 6. SBSRAM Read - Full Speed



SBSRAM READ TIMING

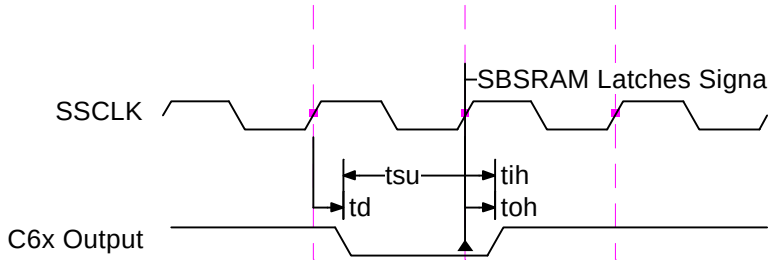
Timing Constraints

This section will discuss the timing constraints used to determine if an SBSRAM can operate with the C6x for full speed timing.

Figure 7 shows the outputs from the C6x, including output data, control signals, and address signals. For full speed timing, each of these outputs is triggered after the rising edge of SSCLK, and is valid after a time t_d. Since the SBSRAM will not latch the signal until the next rising edge, there is a relatively long setup period t_{su} provided to the SBSRAM. As long as the setup time required by the SBSRAM is shorter than that provided by the C6x, this constraint is met.

Similarly, the output signals become invalid a time t_{oh} after a rising edge of SSCLK. As long as the signal is valid for a time longer than the input hold time (t_{ih}) required by the SBSRAM, this constraint is satisfied.

Figure 7. Outputs from C6x (Write Data (ED), Control, and Address Signals)

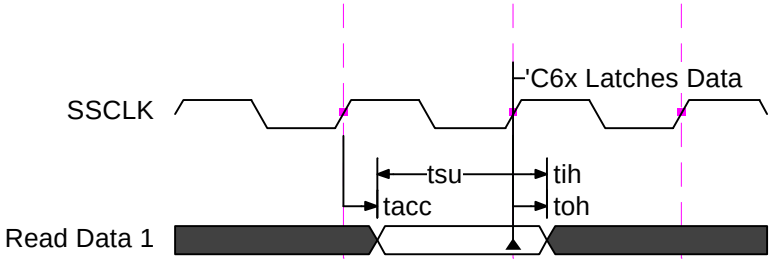


Both of these constraints are expressed as follows:

- $t_{su} < t_{period} - t_d$
- $t_{ih} < t_{oh}$

Figure 8 shows the output data from the SBSRAM, as occurs during a read cycle. The situation is similar to the outputs from the C6x, except the SBSRAM must provide an ample setup and input hold to the C6x.

Figure 8. Output Data from SBSRAM



The constraints can be expressed as follows:

- $t_{su} < t_{period} - t_{acc}$
- $t_{ih} < t_{oh}$

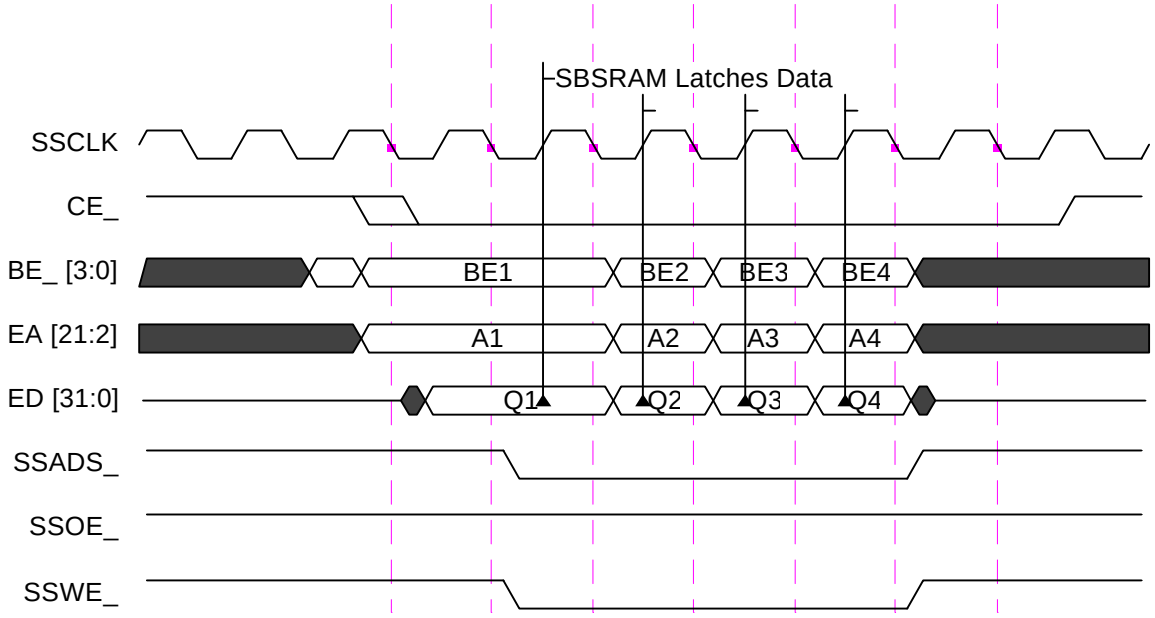
Half Speed

SBSRAM Write

Figure 9 shows a 4 word write to SBSRAM, with SSCLK = ½ CLKOUT1. Every access strobes a new address into the SBSRAM. The first access requires an initial startup penalty; thereafter all access can occur in a single SSCLK cycle. This startup penalty is to ensure that there is no contention over the data bus due to a previous read.

Although the initial transition of /CE and /BE are flexible, and transition off of either rising or falling edges of the half speed SSCLK, this has no effect on the operation of the SBSRAM. The data, address, and control signals for a half speed write are all triggered off of the falling edge of SSCLK. Since for a half speed write, the data, control, and address lines are triggered off of the falling edge, less than a half of a cycle of setup time is provided to the SBSRAM.

Figure 9. SBSRAM Write - Half Speed



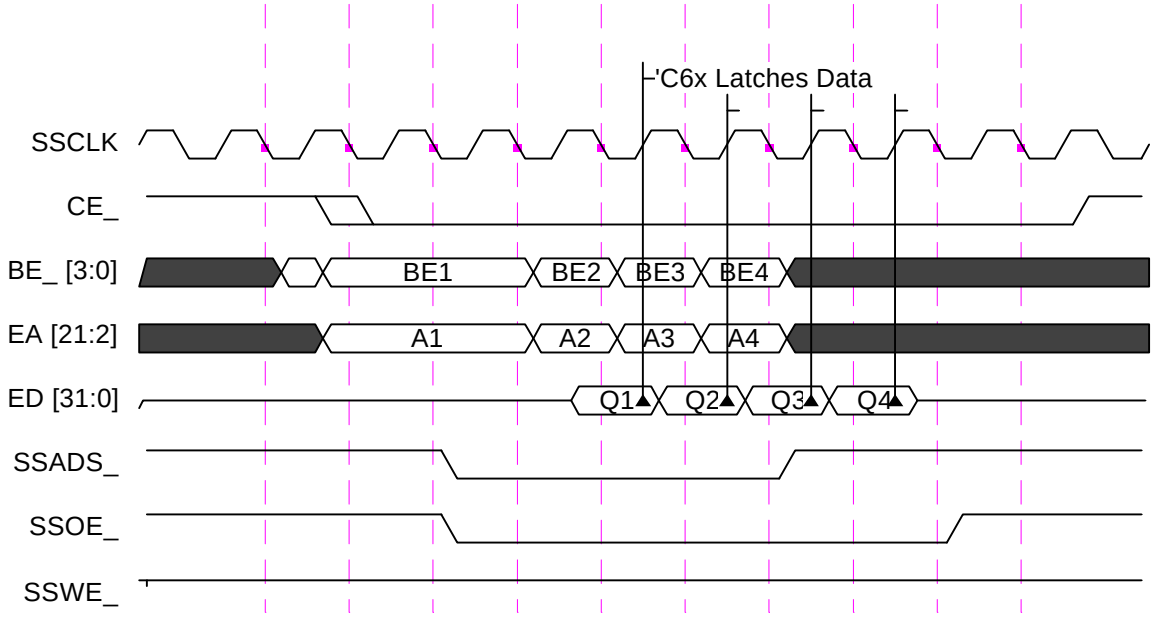
SBSRAM Read

Figure 10 shows a 4 word read of an SBSRAM at half speed (SSCLK = CLKOUT2 = ½ CLKOUT1). Every access strobes a new address into the SBSRAM, indicated by the /SSADS strobe low. The first access requires an initial read latency of 2 cycles; thereafter all accesses have single cycle throughput.

For an SBSRAM read at half speed, notice that the control signals and address signals (after the first access) are triggered by the falling edge of SSCLK, just as for the half speed write cycle, providing less than a half cycle of setup time for the SBSRAM.

Timing for the data output from the SBSRAM during a read has the same constraints as those for a full speed read, since the SBSRAM is triggering the output data off of the rising edge of SSCLK, and the 'C6x is latching the data on the following rising edge.

Figure 10. SBSRAM Read - Half Speed



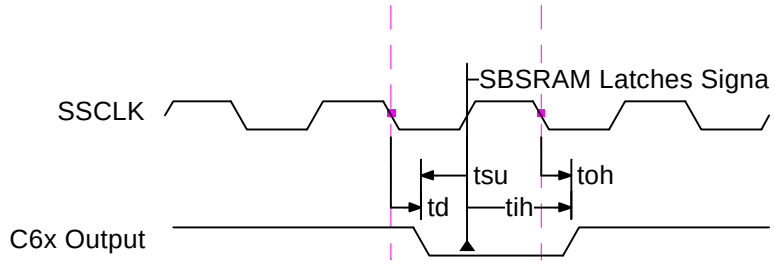
Timing Constraints

This section will discuss the timing constraints used to determine if an SBSRAM can operate with the C6x for half speed timing.

Figure 11 shows the outputs from the C6x, including output data, control signals, and address signals for half speed timing. Each of these outputs is triggered off of the falling edge of SSCLK, and is valid after a time t_d. Since the SBSRAM latches the signal on the next rising edge, there is a relatively short setup time t_{su} provided to the SBSRAM, compared to the full speed cycle. As long as the setup time required by the SBSRAM is shorter than that provided by the C6x, this constraint is met.

Similarly, the output signals become invalid a time t_{oh} after a rising edge of SSCLK. As long as the signal is valid for a time longer than the input hold time (t_{ih}) required by the SBSRAM, this constraint is satisfied.

Figure 11. Outputs from C6x (Write Data (ED), Control, and Address Signals)

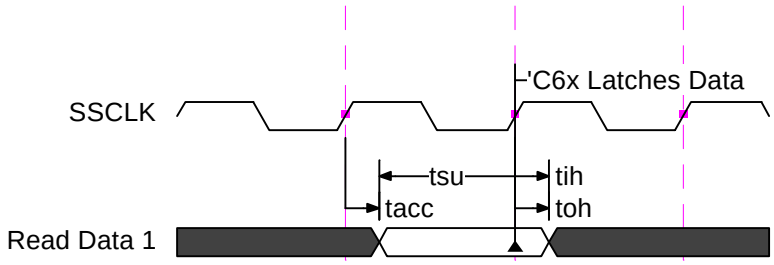


The constraints can be summarized as follows:

- $t_{su} < ½\ t_{period} - t_d$
- $t_{ih} < ½\ t_{period} + t_{oh}$

Figure 12 shows the output data from the SBSRAM, as occurs during a read cycle. The situation is identical to the one for a full speed cycle.

Figure 12. Output Data from SBSRAM



The constraints are:

- $t_{su} < t_{period} - t_{acc}$
- $t_{ih} < t_{oh}$

Optimizing SBSRAM Accesses

SBSRAMs are latent by their architecture, meaning that read data follows address and control information. Consequently, the EMIF inserts cycles between read and write commands to ensure that no conflict exists on the ED[31:0] bus. The EMIF keeps this turn-around penalty to a minimum. The initial 3-cycle penalty is present when changing directions on the bus. In general, the rule is this; the first access of a burst sequence will incur a 3 cycle startup penalty.

Complete Example Using the IS61SP12836

This section will walk through the complete register configuration for interfacing the C6x with ISSI's IS61SP12836-3.5, which is a 128k x 36 SBSRAM capable of operating at 166 MHz. The block diagram for the interface schematic is identical to Figure 4, shown above.

This section will present the necessary timing analysis to ensure that this device meets the timing requirements of the TMS320C6x. In addition, other interface considerations will be presented, such as register configurations and the proper termination of unused pins on the SBSRAM.

Assumptions:

- CLKOUT1 Frequency of 166 MHz
- SBSRAM to be operated at 166 MHz. Therefore, the period is 6 ns.
- SBSRAM to be located at CE2 (logical address 0x02000000)

Timing Analysis of C6x and IS61SP12836-3.5

Figure 13 and Figure 14 compare the timing parameters of the ISSI SBSRAM and the 'C6x. The data shown is from the device's data sheet. And the Conditions listed are from those derived above for a full speed SSCLK.

Figure 13. Outputs from C6x (Write ED, EA, /CE, /SDWE, SDA10, /SDRAS, /SDCAS)

		Condition	**Satisfied ?**
SDRAM Setup Time	t_{su} = 1.5 ns	$t_{su} < t_{period} - t_d$	✔
C6x Delay Time	t_d = 1.1 ns	1.5 ns < 6 ns - 1.1 ns	
SDRAM Input Hold Time	t_{ih} = 0.5 ns	$t_{ih} < t_{oh}$	✔
C6x Output Hold Time	t_{oh} = 1.1 ns	0.5 ns < 1.1 ns	

Figure 14. Inputs to C6x (Read ED)

		Condition	**Satisfied ?**
C6x Setup Time	t_{su} = 1.8 ns	$t_{su} < t_{period} - t_{acc}$	✔
SDRAM Access Time	t_{acc} = 3.5 ns	1.8 ns < 6 ns - 3.5 ns	
C6x Input Hold Time	t_{ih} = 1 ns	$t_{ih} < t_{oh}$	✔
SDRAM Output Hold Time	t_{oh} = 1.5 ns	1 ns < 1.5 ns	

Register Configuration

Table 5. SBSRAM Registers

Register Name	Fields Required
EMIF Global Control	SSCEN, SSCRT
EMIF CE2 Space Control	MTYPE

Figure 15. EMIF Global Control Register Diagram

31 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	SDCINV	CLK2INV	rsv	ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
reserved	x	x	rsv	0	1	1	1	0	1	0	0	1	0	1
R, +0	RW, +1	RW, +1	R, +0	R, +x	R, +x	R, +0	RW, +0	RW, +1	RW, +1	RW, +1	RW, +1	RW, +0	RW, +0	R, +x

SSCEN = 1 indicates that SSCLK is enabled to clock.

SSCRT = 1 indicates that SSCLK is equal to the CPU clock rate, since this was one of the assumptions previously made.

Figure 16. EMIF CE(0/1/2/3) Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
x	x	x	x
RW, +1111	RW, +111111	RW, +11	RW, +1111

15 14	13 8	7	6 4	3 2	1 0
TA	READ STROBE	rsv	MTYPE	reserved	READ HOLD
x	x	rsv	100	reserved	x
RW, +11	RW, +111111	R, +0	RW, +010	R, +0	RW, +11

MTYPE = 100 indicates that 32 bit wide SBSRAM is located in the CE2 address space. Since SBSRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

Termination of Unused Pins

Table 9 summarizes the connections that should be made to the ISSI SBSRAM for unused pins in order to guarantee desired operation.

Table 6. Termination of Unused Pins

Terminate to:	**Pin Description**
GND	/CE2
GND	MODE
GND	ZZ
GND	VSS
3.3V	VCC
3.3 V	CE2
3.3 V	/ADV
3.3 V	/ADSP
3.3 V	/GW
1kΩ to GND	Parity Data

Complete Example Using MT58LC32K32G1-10

This section will walk through the complete register configuration for interfacing the C6x with Micron's MT58LC32K32G1-10, which is a 32k x 32 SBSRAM capable of operating at 100 MHz. The block diagram for the interface schematic is identical to Figure 4, shown above.

This section will present the necessary timing analysis to ensure that this device meets the timing requirements of the TMS320C6x. In addition, other interface considerations will be presented, such as register configurations and the proper termination of unused pins on the SBSRAM.

Assumptions:

- CLKOUT1 Frequency of 200 MHz
- SBSRAM to be operated at 100 MHz. Therefore, the period is 10 ns.
- SBSRAM to be located at CE2 (logical address 0x02000000)

Timing Analysis of C6x and MT58LC32K32G1-10

Figure 13 and Figure 14 compare the timing parameters of the Micron SBSRAM and the 'C6x. The data shown is from the device's data sheet and the Conditions listed are from those derived above for a half speed SSCLK.

Figure 17. Outputs from C6x (Write ED, EA, /CE, /SDWE, SDA10, /SDRAS, /SDCAS)

		Condition	**Satisfied ?**
SDRAM Setup Time	t_{su} = 2 ns	$t_{su} < ½\ t_{period} - t_d$	✔
C6x Delay Time	t_d = 1.1 ns	2 ns < ½ (10 ns) - 1.1 ns	
SDRAM Input Hold Time	t_{ih} = 0.5 ns	$t_{ih} < ½\ t_{period} + t_{oh}$	✔
C6x Output Hold Time	t_{oh} = 1.1 ns	0.5 ns < ½ (10 ns) + 1.1 ns	

- tsu < tperiod - tacc
- tih < toh

Figure 18. Inputs to C6x (Read ED)

		Condition	**Satisfied ?**
C6x Setup Time	t_{su} = 1.8 ns	$t_{su} < t_{period} - t_{acc}$	✔
SDRAM Access Time	t_{acc} = 5.5 ns	1.8 ns < 10 ns - 5.5 ns	
C6x Input Hold Time	t_{ih} = 1 ns	$t_{ih} < t_{oh}$	✔
SDRAM Output Hold Time	t_{oh} = 1.5 ns	1 ns < 1.5 ns	

Register Configuration

Table 7. SBSRAM Registers

Register Name	Fields Required
EMIF Global Control	SSCEN, SSCRT
EMIF CE2 Space Control	MTYPE

Figure 19. EMIF Global Control Register Diagram

31 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	SDCINV	CLK2INV	rsv	ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
reserved	x	x	rsv	0	1	1	1	0	1	0	0	1	0	1
R, +0	RW, +1	RW, +1	R, +0	R, +x	R, +x	R, +0	RW, +0	RW, +1	RW, +1	RW, +1	RW, +1	RW, +0	RW, +0	R, +x

SSCEN = 1 indicates that SSCLK is enabled to clock.

SSCRT = 0 indicates that SSCLK is equal to the ½ of the CPU clock rate, since this was one of the assumptions previously made.

Figure 20. EMIF CE(0/1/2/3) Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
x	x	x	x
RW, +1111	RW, +111111	RW, +11	RW, +1111

15 14	13 8	7	6 4	3 2	1 0
TA	READ STROBE	rsv	MTYPE	reserved	READ HOLD
x	x	rsv	100	reserved	x
RW, +11	RW, +111111	R, +0	RW, +010	R, +0	RW, +11

MTYPE = 100 indicates that 32 bit wide SBSRAM is located in the CE2 address space. Since SBSRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

Termination of Unused Pins

Table 9 summarizes the connections that should be made to the Micron SBSRAM for unused pins in order to guarantee desired operation.

Table 8. Termination of Unused Pins

Terminate to:	Pin Description
GND	/CE2
GND	MODE
GND	ZZ
GND	VSS
3.3V	VCC
3.3 V	CE2
3.3 V	/ADV
3.3 V	/ADSP
3.3 V	/GW

References

"TMS320C6201 Data Sheet, Revision 2," Texas Instruments, October 1997.

"TMS320C62xx Peripherals Reference Guide," Texas Instruments, October 1997.

"MT58LC32K32G1 Data Sheet," Micron Technology, Inc., January 1997.

"IS61SP12836 Data Sheet," Integrated Silicon Solution, Inc., June 1997.