TMS320C6201 DIGITAL SIGNAL PROCESSOR DATA SHEET (SPRS051C) ERRATA

Changes to SPRS051C are indicated in gray.

Page 27 electrical characteristics over recommended operating ranges

For Ii, Input Current, the following pins not included due to internal pullups: TMS, TDI ; and the following pins not included due to internal pulldowns: TRST

Page 33 switching characteristics for synchronous SRAM cycles (full-rate SSCLK)

9	tsu(ADSV-SSCLKH)	Setup time, /SSADS valid before SSCLK high	P-3		ns
10	toh(SSCLKH- ADSV)	Setup time, /SSADS valid after SSCLK high	0		ns
17	tsu(WEV-SSCLKH)	Setup time, /SSWE valid before SSCLK high	P-3		ns
18	toh(SSCLKH- WEV)	Setup time, /SSWE valid after SSCLK high	0		ns

Page 41 timing requirements for the hold/hold acknowledge cycles

2	th(CKO1H-HOLDL)	Hold time, /HOLD low after CLKOUT1 high	2		ns

Page 48 timing requirements for McBSP

3	tw(CKRX)	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P-1	ns

Page 49 switching characteristics for McBSP

9	td(CKXH-FXV)	Delay time, CLKX high to internal FSX valid	CLKX int	0	4	ns
12	tdis(CKXH-DXHZ)	Disable time, DX high impedance following last data bit from CLKX high	CLKX int	0	4	ns
13	td(CKXH-DXV)	Delay time, CLKX high to DX valid.	CLKX int	0	4	ns

Page 52 timing requirements for McBSP as SPI master or slave: CLKSTP=10b, CLKXP=0

5	th(CKXL-DRV)	Hold time, DR valid after CLKX low	4	5 + 6P	ns

Page 52 switching characteristics for McBSP as SPI master or slave: CLKSTP=10b, CLKXP=0

1	th(CKXL-FXL)	Hold time, FSX low after CLKX low	T – 2	T + 3			Ns
2	td(FXL-CKXH)	Delay time, FSX low to CLKX high	L – 2	L + 3			Ns
3	td(CKXH-DXV)	Delay time, CLKX high to DX valid	-2	4	3P + 4	5P + 17	Ns
6	tdis(CKXL-DXHZ)	Disable time, DX high impedance following last data bit from CLKX low	L – 2	L + 3			Ns

Page 54 timing requirements for McBSP as SPI master or slave: CLKSTP=11b, CLKXP=0

5	th(CKXH-DRV)	Hold time, DR valid after CLKX high	4	5 + 6P			Ns

Page 54 switching characteristics for McBSP as SPI master or slave: CLKSTP=11b, CLKXP=0

1	th(CKXL –FXL)	Hold time, FSX low after CLKX low	L – 2	L + 3			ns
2	td(FXL-CKXH)	Delay time, FSX low to CLKX high	T – 2	T + 3			ns
3	td(CKXL-DXV)	Delay time, CLKX low to DX valid	-2	4	3P + 4	5P + 17	ns
6	tdis(CKXL-DXHZ)	Disable time, DX high impedance following last data bit from CLKX low	-2	4	3P + 4	5P + 17	ns
7	td(FXL-DXV)	Delay time, DX valid after FSX valid low	H – 2	H + 4	2P + 4	4P + 17	ns

Page 55 timing requirements for McBSP as SPI master or slave: CLKSTP=10b, CLKXP=1

5	th(CKXH-DRV)	Hold time, DR valid after CLKX high	4	5 + 6P			ns

Page 55 switching characteristics for McBSP as SPI master or slave: CLKSTP=10b, CLKXP=1

1	th (CKXH –FXL)	Hold time, FSX low after CLKX high	T – 2	T + 3			ns
2	td(FXL-CKXL)	Delay time, FSX low to CLKX low	H – 2	H + 3			ns
3	td(CKXL-DXV)	Delay time, CLKX low to DX valid	-2	4	3P + 4	5P + 17	ns
6	tdis (CKXH-DXHZ)	Disable time, DX high impedance following last data bit from CLKX high	H – 2	H + 3			ns

Page 57 timing requirements for McBSP as SPI master or slave: CLKSTP=11b, CLKXP=1

5	th(CKXL-DRV)	Hold time, DR valid after CLKX low	4	5 + 6P			ns

Page 57 switching characteristics for McBSP as SPI master or slave: CLKSTP=11b, CLKXP=1

1	th(CKXH –FXL)	Hold time, FSX low after CLKX high	H – 2	H + 3			ns
2	td(FXL-CKXL)	Delay time, FSX low to CLKX low	T – 2	T + 1			ns
3	td(CKXH-DXV)	Delay time, CLKX high to DX valid	-2	4	3P + 4	5P + 17	ns
6	tdis(CKXH-DXHZ)	Disable time, DX high impedance following last data bit from CLKX high	-2	4	3P + 4	5P + 17	ns
7	td(FXL-DXV)	Delay time, FSX low to DX valid	L - 2	L + 4	2P + 4	4P + 17	ns

Page 58 switching characteristics for DMAC outputs

1	td(CKO1H-DMACV)	Delay Time, CLKOUT1 high to DMAC valid.	2	7	ns