TEXAS INSTRUMENTS

Application Report

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Using Boundary Scan on the TMS320VC5441

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ABSTRACT

The TMS320VC5441 DSP (hereafter referred to as VC5441) is a quad-core processor implementing standard IEEE 1149.1 boundary scan capability. This application report contains a description of the VC5441 boundary scan implementation and information about how to use it with other boundary scan tools and devices.

The material covered in this application report assumes the reader is familiar with the boundary scan concepts defined by IEEE Standard 1149.1. An overview of these concepts is presented in the IEEE Std 1149.1 (JTAG) Testability Primer (literature number SSYA002). For detailed information on the operation and requirements for boundary scan, refer to the IEEE standard itself. Copies of the standard are available from IEEE at 1-800-678-IEEE.

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1 VC5441 Boundary Scan Implementation

1.1 VC5441 Silicon Revision Requirements

The VC5441 boundary scan implementation described in this document applies to all silicon revisions.

1.2 Full Observe and Control Capability

VC5441 implements standard observe and control capability with respect to the IEEE Standard 1149.1. This means all pins with input functions (input or I/O pins) have observe capability and all pins with output functions (outputs and I/O pins) have control capability.

1.3 VC5441 Hardware Requirements for Boundary Scan Test

Boundary scan test requires control of the five test access port signals (TMS, TCK, TDI, TDO and TRST) as described in IEEE standard 1149.1. Two additional signals, EMU0 and EMU1/OFF, are used by TI DSPs to provide emulation debug capability through the JTAG test access port. TI also uses these signals for scan-based factory tests.

During boundary scan tests, EMU0 and EMU1/OFF must be held high while TRST is transitioned from low to high. This operation sets the correct internal test mode for boundary scan test to be performed. EMU0 and EMU1/OFF should be pulled high through 4.7k ohm pull-up resistors on each pin. The pull-up resistors are connected to the DVdd power supply for the VC5441.

Boundary scan ATPG tools should be configured to cycle TRST/ prior to beginning boundary scan tests to ensure that the device is in the proper test mode.

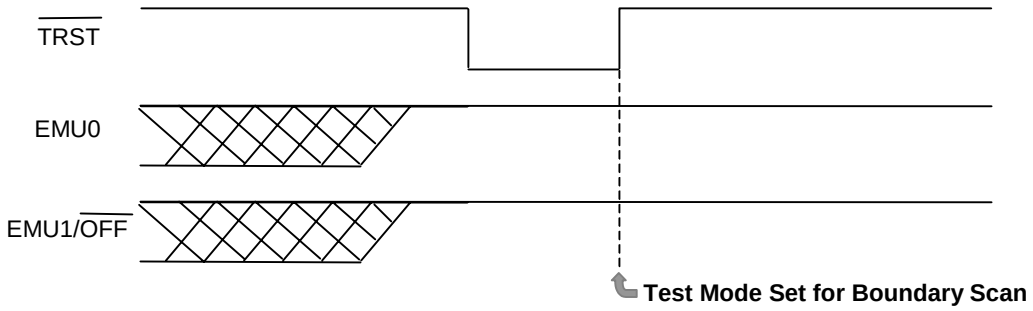

Figure 1. Initialization for Boundary Scan Test Mode using TRST, EMU0 and EMU1/OFF

1.4 VC5441 Boundary Scan Pin Coverage

All digital pins (112 pins) on the VC5441 have boundary scan cells for test with the following exceptions. The device pins not testable through boundary scan are shown below in Table 1.

Table 1. Device Pins Not Testable Through Boundary Scan

Pin	Pin Function
DVdd, CVdd, Vss, AVdd, Vssa	Power supply pins
TEST	Factory test pins
TMS, TCK, TDI, TDO, TRST~	JTAG test access pins
EMU0, EMU1/OFF~	Emulation test pins

1.5 VC5441 Boundary Scan Description Language (BSDL) Implementation

A representation of the internal structure of the VC5441 with respect to boundary scan is shown in Figure 2. The VC5441 is composed of four internal processors called subsystems. Each subsystem has its own independent TAP controller to provide boundary scan test and emulation capability. The device signals TMS, TCK and TRST are connected to each subsystem in parallel.

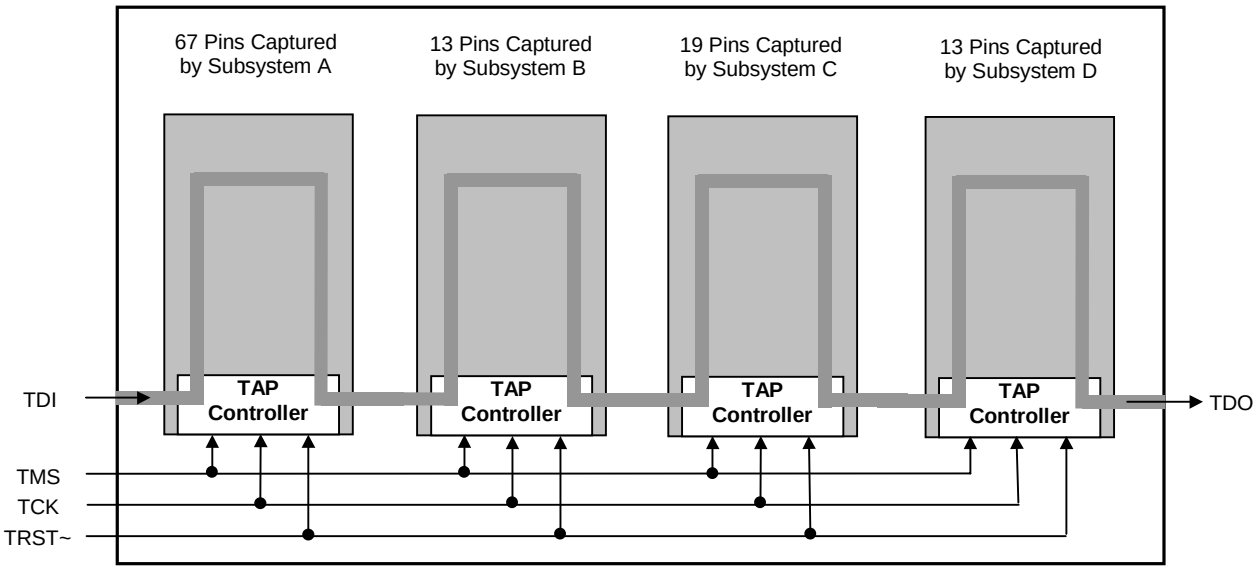

Figure 2. Boundary Scan Structure of the VC5441

The device TDI is connected to subsystem A.
The internal equivalent of TDO for subsystem A is connected to the internal TDI for subsystem B.
The output of the chain from subsystem B is connected to the internal TDI for subsystem C.
The output of the chain from subsystem C is connected to the internal TDI for subsystem D.
The output of the chain from subsystem D is connected to the device TDO.

To a boundary scan test system, this structure is equivalent to treating the subsystems as independent devices.

The four subsystems have the ability to capture unique groups of pins on the device. Subsystem A captures 67 pins which include the pins associated uniquely with subsystem A and the device pins that are common to four subsystems. Subsystem B captures only the 13 device pins associated with subsystem B. Subsystem C captures 19 pins that include the pins associated uniquely with subsystem C and the device pins that are common to four subsystems. Subsystem D captures only the 13 device pins associated with subsystem D. The pins captured by each subsystem are listed in Table 2.

Table 2. Pins Captured by each VC5441 Subsystem During Boundary Scan Test

Subsystem	Pins	Description
A	HA[0:18]	HPI Address Bus
	HD[0:15]	HPI Data Bus
	HCS~ HAS~ HMODE HDS1~ HDS2~ HR/W~ HRDY HPI_SEL1 HPI_SEL2	HPI-16 Signals
	RESET	Device Reset Signal
	CLKMD CLKIN CLKOUT	Clock Signals
	BDR2 BCLKR2 BCLKX2 BFSR2 BFSX2 BDX2	McBSP2 Signals
	A_BDR0 A_BCLKR0 A_BCLKX0 A_BFSR0 A_BFSX0 A_BDX0	A_McBSP0 Signals
	A_GPIO[0:3]	A General Purpose I/O Signals
	A_RS~ A_NMI~ A_INT~	A Reset Interrupt Signals
B	B_BDR0 B_BCLKR0 B_BCLKX0 B_BFSR0 B_BFSX0 B_BDX0	B_McBSP0 Signals
	B_GPIO[0:3]	B General Purpose I/O Signals
	B_RS~ B_NMI~ B_INT~	B Reset Interrupt Signals
C	BDR1 BCLKR1 BCLKX1 BFSR1 BFSX1 BDX1	McBSP1 Signals
	C_BDR0 C_BCLKR0 C_BCLKX0 C_BFSR0 C_BFSX0 C_BDX0	C_McBSP0 Signals
	C_GPIO[0:3]	C General Purpose I/O Signals
	C_RS~ C_NMI~ C_INT~	C Reset Interrupt Signals
D	D_BDR0 D_BCLKR0 D_BCLKX0 D_BFSR0 D_BFSX0 D_BDX0	D_McBSP0 Signals
	D_GPIO[0:3]	D General Purpose I/O Signals
	D_RS~ D_NMI~ D_INT~	D Reset Interrupt Signals

Although ATPG tools vary in how they describe system level structure, all tools provide a method to describe the order of the devices in the scan chain. The BSDL description of the VC5441 is implemented as 4 BSDL files, one for each subsystem. These four boundary scan objects must always be grouped and described to the ATPG tools in the proper order. Subsystem D must be described as the subsystem closer to TDO, then is subsystem C, and subsystem B follows, the last is subsystem A. If the order is reversed, tests generated by the ATPG tools will be incorrect.

Since the connection between the scan chains of the four subsystems is internal to the device, some ATPG tools may issue a warning or error indicating that the TDO-TDI connection between the two subsystem objects is not present. In this case, the device can be modeled as a multi-chip module using the hierarchical capabilities of the ATPG tool. Many boundary scan systems have

hierarchical scan chain descriptions where, for example, a plug-in module may be described as a sub-chain to the main boundary scan chain. The model for the sub-chain is generated separately, and then referenced in the description of the main boundary scan chain. The same approach can be used to model the VC5441 as a single object if necessary. The device can be modeled as a sub-chain composed of subsystem A, subsystem B, subsystem C, and subsystem D, shown in Figure 3. Then, the VC5441 can be referenced in the main description of the scan chain as a single device "module". Since the methods to describe hierarchical and modular systems are tool dependent, a single method cannot be described here. It will be necessary to contact the ATPG tool vendor regarding how this procedure is done on their tool. Given the BSDL files for each subsystem and the information in this document, a model can be generated.

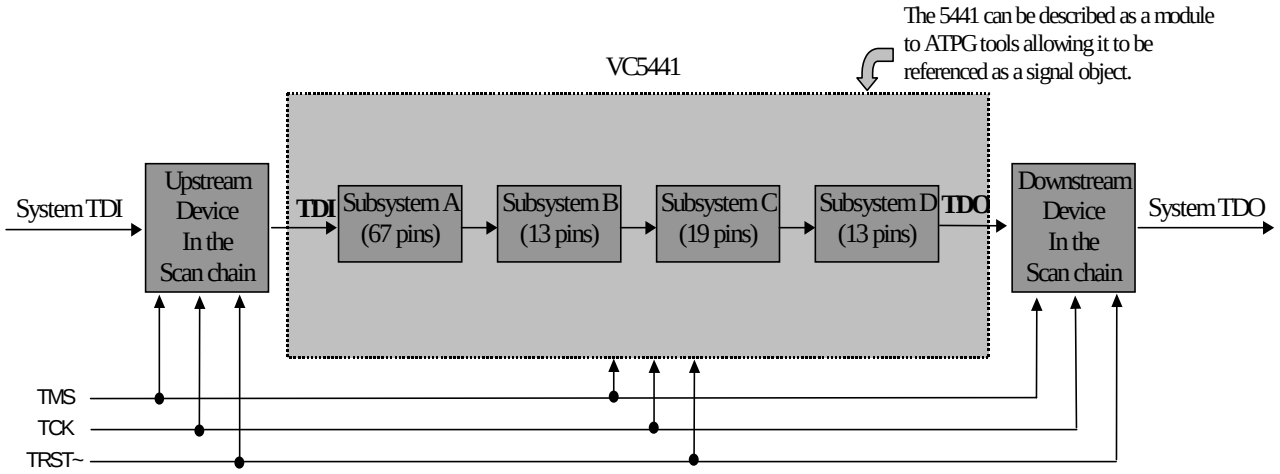

Figure 3. The VC5441 Subsystems Modeled as a "Module" in the Scan Chain

Separate BSDL files are provided for subsystem A, B, C, and D. Current VC5441 BSDL files and information are available on the web at:

http://www.ti.com/sc/docs/tools/dsp/ftp/c54x.htm

1.6 VC5441 Boundary Scan Instruction Implementation

The VC5441 implements the following instructions for boundary scan:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- HIGHZ

IEEE standard 1149.1 specifies that the SAMPLE/PRELOAD instruction samples inputs and preloads but does not drive outputs. During the SAMPLE/PRELOAD instruction, the device pins maintain their normal functional behavior. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the EXTEST instruction samples inputs, and loads and drives outputs. During the EXTEST instruction, all device pins function as boundary scan inputs. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the BYPASS instruction maps a one-bit bypass register between TDI and TDO (to minimize the chain length when a device is not being tested) and the device pins operate in their normal functional (non-test) mode. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard. Note that the VC5441 has one bypass bit for each subsystem (since there is a TAP controller for each subsystem) for a total of four bits between the device TDI and TDO. This behavior is accounted for (and maintains compliance with IEEE standard 1149.1) through the use of separate BSDL files for each subsystem.

IEEE standard 1149.1 specifies that the HIGHZ instruction places the bypass register in the scan chain and causes all output pins (either dedicated outputs or I/O pins) to enter a high-impedance state. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

None of the other boundary scan instructions specified as optional in IEEE standard 1149.1 are implemented on the VC5441.

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