TMX320F206 Flash Serial Loader Rev 2.0

This document contains the software specifications and functional description of the TMX320F206 serial loader for programming the on-chip flash. **The data is preliminary and subject to change at any time**.

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A. TMX320F206 Flash Serial loader features

The Serial loader for TMX320F206 devices facilitates initial programming of flash arrays. Sections in this document describes the functional aspects of the serial loader and should give a quick start on flash programming.

A.1 Rev 2.0 software features

- Rev 2.0 serial loader provides flash control utilities to communicate with PC/host and program 32k words of on_chip flash. Clear, Erase functions will operate on the entire 16k of flash 0 or flash1 array.
- Flash function algorithms Clear, Erase and Program are available only as object modules. The source code for these algorithms will be available along with future revisions of this software.
- Rev 2.0 flash algorithms require the F206 device to run at 20Mhz CLKOUT1 only. For any speeds less than 20Mhz the flash algorithms have to be modified. Refer to section D.7 for details.
- Rev 2.0 PC/host serial communication utility is for Windows'95 only.

A.2 F206 memory map for serial loader

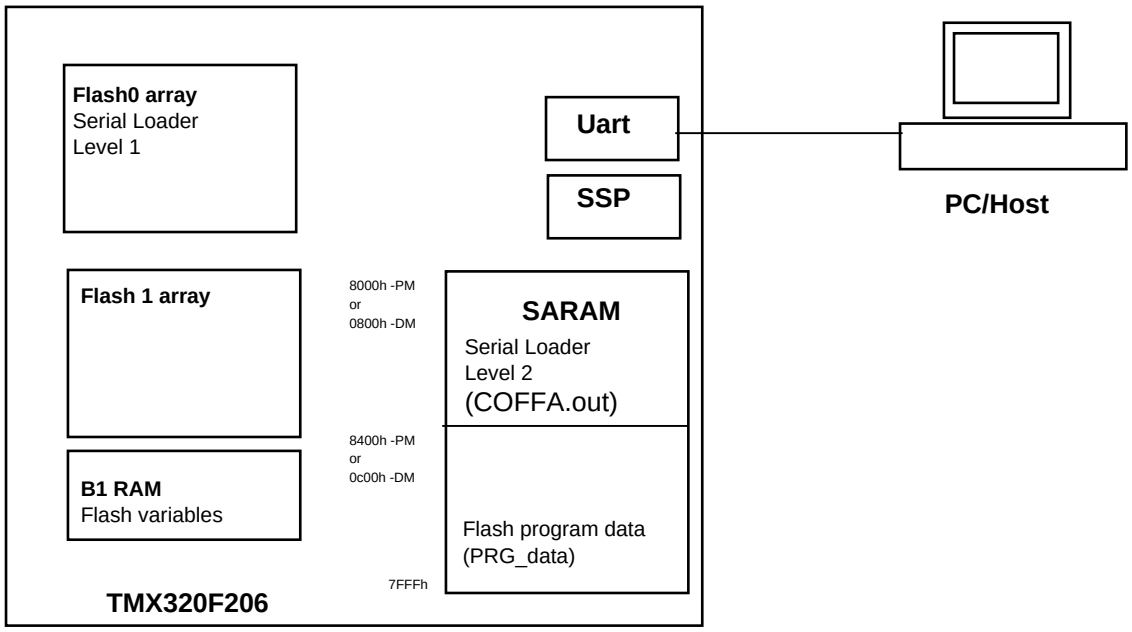


Figure 1 F206 memory map and serial port connections

A.3 Functional description

Software modules:

The flash serial loader utility is intended for programming the on-chip flash (32k) of TMX320F206 devices. The flash serial loader utility has three software modules. The first module is the serial loader Level 1, Which should reside in the on-chip flash (flash 0 array at 0x0000h). All the F206 devices rev 2.0 and above shipped from Texas Instruments will have this code pre-programmed in Flash 0. The Level 1 module has a serial communication code that will communicate through the on-chip UART to a host computer to load any application code on to its internal memory. The second module is the host serial communication utility (F206sldr.exe). This is a Windows'95 program for IBM/PC compatibles which uses the PC's COM ports to communicate with the F206 devices. The host utility will communicate with Level 1 code on the F206 device to download flash algorithms and flash data to be programmed. The third module is the serial loader Level 2, which contains the flash control and flash algorithms. The Level 2 code will be loaded into the internal memory using the Level 1 code and the host utility.

Operation:

Figure 1 explains a typical set up between the F206 device and a host system. At power on reset the Level 1 software resident in the on-chip flash of the F206 device will initialize the UART or SSP based on the BIO pin. If the BIO pin is high the UART loader will be enabled. The UART loader will enable auto-baud detect logic and wait for characters through the UART port. Flowchart 1 explains the software logic in detail. The host PC will send ascii character 'a' as the first character through the serial link to the F206. On receipt of valid 'a' the F206 software logic locks to incoming data rate and updates its baud rate register and echoes character 'a' back to the host. The host, after receiving a valid echo from the DSP, sends the Level 2 algorithm code to the F206. Once the Level2 code is successfully loaded into the target's internal RAM, the Level 2 code will take control of the DSP core. The Level 2 code will further handshake with the host to receive flash data for flash programming.

Loading status and modes:

The host utility communicates with Level2 code until the programming is done and updates the communication status window (both successful completion and error code, if any). The host activates its communication status through the DTR and RTS signals on its serial port as well as on the host monitor. The DTR signal will go active low when it receives a valid echo of character 'a' from the F206 device, indicating the loading is in progress. Once the loading is done the DTR signal will go inactive high, indicating the loading is complete. If during the loading process any error occurs, the RTS signal will go active low, and remain low, indicating there was an error in the current loading process. If LEDs (light emitting devices) are added to these signals, they will provide visual indication of loading status at the remote end (at the F206 device side).

The host software can run in continuous mode or single device mode. In the single device mode, the host program will halt after loading. In the continuous mode the host software will resend character 'a' and wait for a valid echo to proceed with a loading process. This logic will run continuously until the program is aborted. The continuous mode enables multiple device programming without manual interaction on the host terminal.

B. Flash serial loader program modules

B.1 F206 serial Loader Level 1

Resides in Flash0 from 0x0000-0x00ff. This program should be in the flash0 array for the serial loader to function.

Source files - usload_2.asm, usload_2.out .
Level 1 loader (usload_2.out) is a beta version.
Shipped in all F206 silicon rev 2.0 and above.

Function - After reset, the DSP is initialized, B0 RAM will be in program space and either UART or SSP loader will be enabled.

SSP loader:
If BIO pin is low at reset, the serial loader will enable SSP interrupt only and will accept data through the synchronous serial port (SSP). This feature is for future use and application specific loaders.

UART loader:
If BIO pin is high at reset the uart loader will enable uart interrupt and initialize the auto baud detect feature of the uart.

This document/program uses only the uart loader features to do flash functions!!

The uart will wait for 'a'/ 'A' as the first character from the host.
On a valid character 'a'/ 'A' receive the DSP will update its baud register with host baud rate and will be ready to receive application data.

After the baud detect stage the incoming serial application data should be in the following format.

Header
Destination/Run address high byte
Destination/Run address low byte
Length of data that follows - high byte
Length of data that follows - low byte
Data
High byte
Low byte

The serial loader will move the incoming data to the destination address, disable all interrupts and will jump to execute the code from destination/run address.

Refer to Level 1 flow chart (section F.1)- for more details.

B.2 F206 serial loader Level 2

Resides in destination/run address, Default 0x8000h in SARAM.
Level 2 code is loaded by Level 1 part of the serial loaders. Once Level 2 is loaded Level 1 code is no longer required.

Source file - COFFA.out

Function - Level 2 of the serial loader has the flash control code that selects flash functions, Clear, Erase and Program on the appropriate flash array. It also manages the host handshaking and additional uart based COFF file loading. The flash control code selects the required flash functions. These functions are selected by two flag/command registers.
SFLAG - for selection of flash array functions, (Serial loader command word)
HFLAG - for host status indication. (Host command word)
Refer to section E for more details.

Level 2 of the code communicates with the host and moves the application code to program data buffer (PRG_data) at 0x8400 -PM/ 0x0c00 -DM in SARAM.(SARAM is mapped in both program (PM) and data memory (DM)).

B.3 Flash function modules

The flash function modules are loaded into the SARAM along with Level 2 code. The flash functions use all the CPU resources while execution. If these flash function are to be customized in any applications refer to the following sections for more details.

B.3.1 Flash function calling conventions

Rev 2.0 serial loader utilities are shipped with flash function modules for CLEAR, ERASE and PROGRAM of flash arrays. These are object modules used in the serial loader and can be used in any application. The calling conventions are listed below for reference and customizing applications. It is suggested that while calling these functions, all the CPU resources should be saved and recovered after return. Currently these flash functions are under optimization. Future versions of this utility will provide detail documentation of the CPU resources used by these functions. Texas Instruments reserves the right to change these functions in future versions.

B.3.1.1 Flash register utilities

This has three functions that are used to access flash registers and create variable delay loops.

Function name	: DELAY
Function	: Delay loop in micro and milliseconds. Useful in generating
	: CLEAR,ERASE pulses for the flash array.
Include file	: svar20.h
Object file	: sutils20.obj

Function name : REGS
Function : Modifies the flash array access control register F_access0/1, and
: enable register mode
Include file : svar20.h
Object file : sutils20.obj

Function name : ARRAY
Function : Modifies the flash array access control register F_access0/1,
: and disables register mode
Include file : svar20.h
Object file : sutils20.obj

B.3.1.2 Flash function, CLEAR

Function name : GCLR
Function : Clears the selected flash segments in the specfiedflash array
Include file : svar20.h
Object file : sclr20.obj

B.3.1.3 Flash function, ERASE

Function name : GERS
Function : Erase the selected flash segments in the specified flash array
Include file : svar20.h
Object file : sera20.obj

B.3.1.4 Flash function, PROGRAM

Function name : GPGM
Function : Program the selected flash segments in the specified flash array
Include file : svar20.h
Object file : spgm20.obj

B.4 Reserved memory map and variables for flash programming

The on_chip RAM, B1, B2 and SARAM are reserved for loading programming algorithms. Figures 2 and 3 explain the reserved space and variables. If flash algorithms need to be customized for specific applications refer to these Figures for more details.

Figure 3 explains the function of the variables while executing Clear, Erase and Programming algorithms. The current serial loader application is written based on these variables and these variables are also common to the JTAG based flash utilities. Refer to the assembler source files to understand the software logic.

Figure 2 Reserved memory map and variables

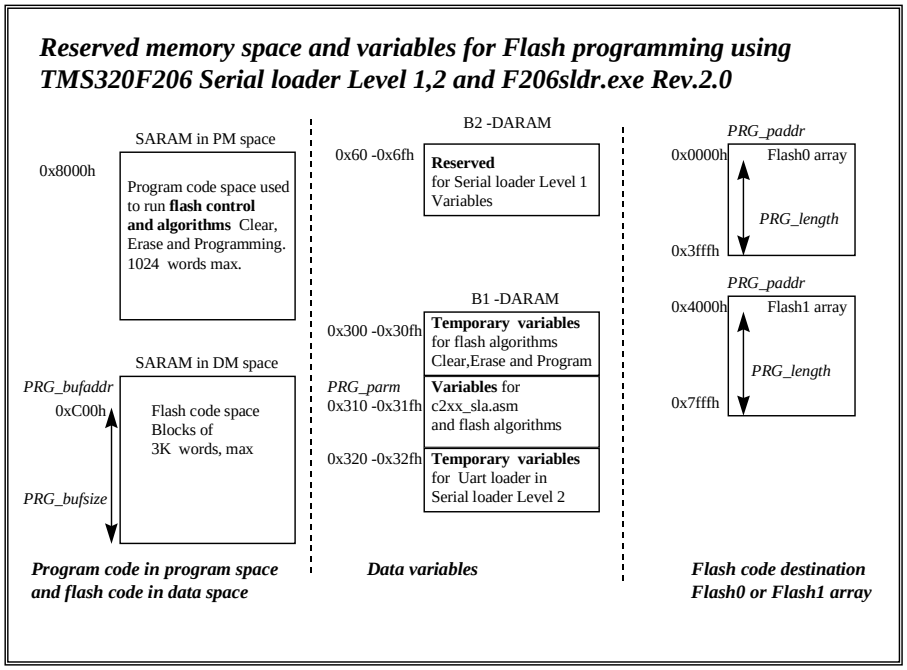
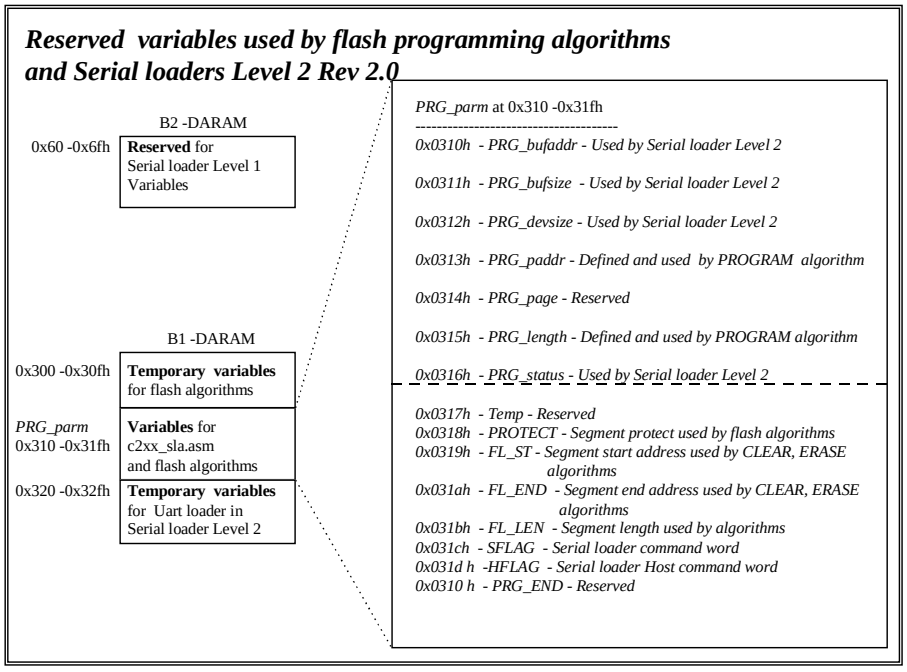


Figure 3 Reserved variables and their functions



B.5 PC host software Rev 2.0

Application - F206sldr.exe
Windows'95 program for serial communication between PC/host and F206 DSP devices

Function - Windows'95 program to transfer Level 2 algorithm COFF file and application code to be programmed as COFF file through PC serial ports COM1,COM2,COM3 or COM4 Host baud can be selected from 110 baud to 57600 baud. Higher speeds are possible if PC serial ports are designed for higher speeds.

Facilitates serial transfer of F206 Level 2 source code (COFFA.out) while Level 1 is running in F206 and downloads flash code in blocks.

UART transmit files

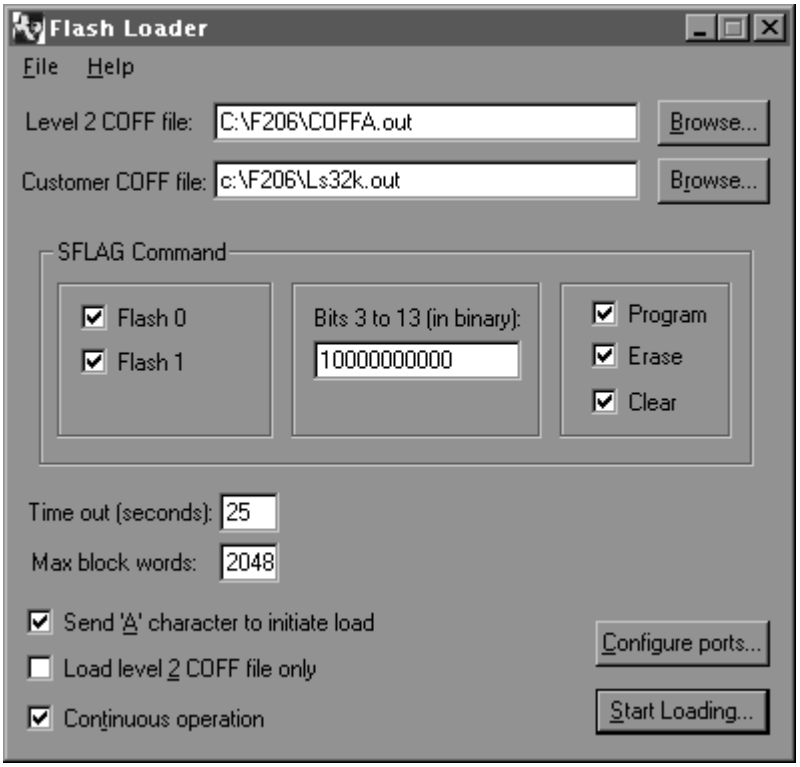
COFFA.out

This is a COFF file with only one .text section. Refer to the COFFA.out source files for details of building this file. The host serial loader program will not accept algorithm COFF files with multiple sections.

Customer COFF file

This is the actual COFF file to be programmed into the 32k of flash memory. The COFF file can be as large as 32k words (max). The COFF file can have multiple program sections or a single section under boot_sec directive. The serial loader may not accept all types of COFF files. Refer to the code examples in section C.2.

B.5.1 Flash loader main screen



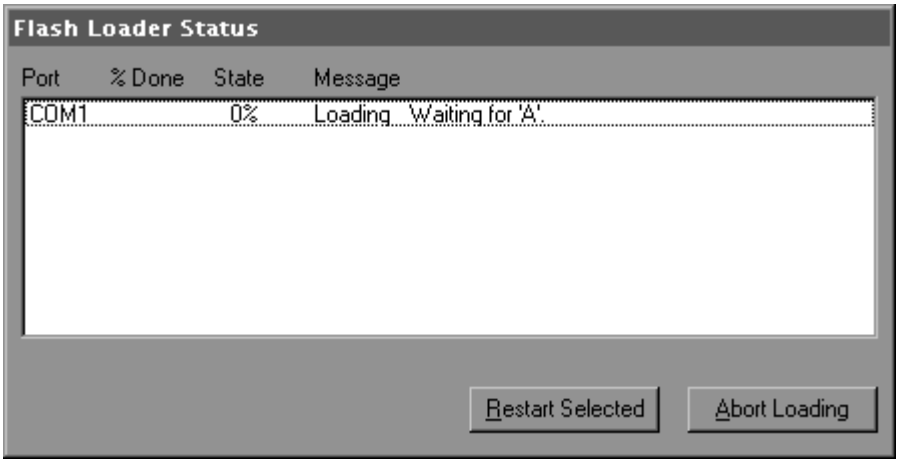
An example for menu selections in F206sldr.exe:

a. Enter the directory path for the Level 2 algorithm code COFFA.out file to be loaded
b. Enter the directory path for the customer flash code COFF file to be programmed
c. Define the SFLAG bits to enable flash array and flash functions. SFLAG is a 16 bit number, each of these bits will select the required flash functions in the serial loader Level 2.
(Select SFLAG bits to be 0xe007 for fast programming of Flash 0 and 1 array on new F206 devices. This selection will Clear, Erase flash 0 array and program Flash0 and Flash 1 arrays. Flash 1 array comes in erased state, ready for programming. Flash 0 is cleared and erased to remove the Level 1 loader code shipped with the device).
Refer to section E for SFLAG command details.

d. Select the host time out limit to 25 seconds if 32k words of flash are to be programmed
e. Define flash code buffer size in SARAM to be 2048.
f. Select 'Send A character to initiate load'. This will make the host send a character 'a' before loading
g. Select 'Level 2 COFF file only' if the serial loader is to load only Level 2 code to do CLEAR and ERASE. Enabling will make the utility ignore customer COFF file selection.
h. Select 'Continuous operation' if the serial loader is to run in the background continuously. This is a useful feature for programming multiple F206 boards without any menu selection on the host terminal.

After selecting the above options, the selections can be saved in a configuration file for future use. The File menu provides all the standard file operations.

B.5.2 Flash loader communication status window



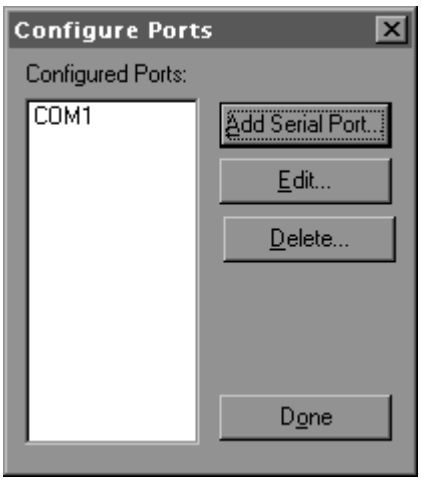
The host serial loader software will update a communication status window while the loading is in progress. The status window will display the selected COM port, percentage of loading done, and error message with (error code).

a. Loading Done (1)
b. Communication error (2)
c. Algorithm error in CLEAR (3)
d. Algorithm error in ERASE (4)
e. Algorithm error in PROGRAM (5)

B.5.3 Flash serial loader 'Configure ports' menu

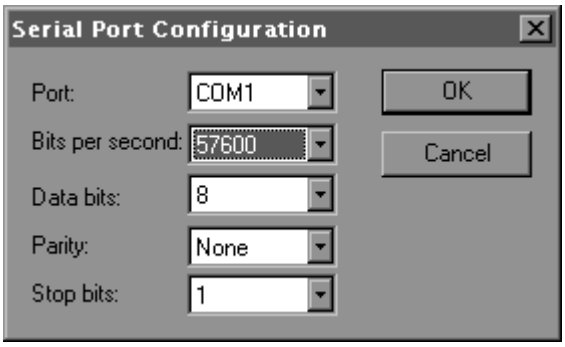
Serial port options:

Select 'Configure ports' menu to define the serial ports (COM1,COM2,COM3 or COM4)



B.5.4 Flash loader serial port selections

Select the baud rate as desired and 8 bits data, no parity and 1 stop bit



C. List of source files that are necessary to build the flash programming files.

C.1 Control code

```
Assembler/hex  source files
        c2xx_sla.asm            ; Flash control and algorithms
 Include files
        sldrv20. h              ; Variable declarations
        cmds20.h                ; SFLAG, HFLAG and host commands declarations
Linker command files            ; To generate COFF files using TI tools
        c2xx_sla.cmd
Level 2 COFF file               ; Flash Algorithm COFF file
        COFFA.out
```

C.2 Flash algorithms

```
 Object modules
        sclr20.obj              ; Clear algorithm
        sera20.obj              ; Erase algorithm
        spgm20.obj              ; Program and Verify algorithm
        sutils20.obj            ; Flash register utility
```

C.3 User code to be programmed in flash array 0/1 using serial loader Rev 2.0

Ls32k.asm is a sample code to explain serial flash programming flow. In actual application the relevant application file should be used. The Ls32k.out COFF file is a test file to test the 32k flash programming on the F206 devices. The COFF file has Level1 code plus a dummy code (alternate 0xaaaa, 0x5555) to make up the rest of the 32k words of memory. If the programming is successful, the Level 1 code will be restored for future use of the serial loader.

```
 Lf32k.asm          ; This is a sample application code with 32k words of  hex
                    ; numbers(0xaaaa, 0x5555).
 Ls32k.cmd          ; Linker command file to load user/application COFF file
                     ; to arrays 0 and 1.
 Ls32k.out          ; The user application code COFF file
                    ( Level1 code + Lf32k code)
```

C.4. Level 1 serial loader rev 2.0

```
 usload_2.asm       ; Assembler source code
 finit.h            ; Include file
 usload_2.out       ; COFF file
```

C.5 PC host serial communication program Rev2.0 for Windows'95 only!

F206sldr.exe

Note:
Refer to TMS320Cx/c2x/c2xx/c5xTI's Assembly language tools User's guide - SPRU018D for details on file extension names and their function.

D. Quick learn procedure for flash programming using serial loader Rev 2.0

This procedure assumes that the F206 is already programmed with serial loader Level 1 in flash array 0. Level 1 loader (usload_2.out) is a beta version. This code will be shipped in all TMX320F206 silicon release rev 2.0 and above.

Refer to JTAG programming utilities rev 2.0 documentation for on-chip flash programming basics.

D.1 User application code formatting.

D.1.1. Select the required application code to be programmed in Flash 0/1 array. This code could be 32k words in length (max). The COFF file could be a single section code under boot_sec directive for grouping multiple program sections or program codes with multiple COFF sections.

Note: Use the Ls32k.out shipped with Rev 2.0 s/w utilities to get familiar with programming steps.

D.2 Choosing the flash functions

The F206sldr.exe is a windows program with menus to define the programming and serial port options. Select the configurations as outlined below and save the current selections in any desired configuration file (xxxx.cfg) for future use. See section B.2 for details.

D.3 Procedure to generate COFFA.out file

D.3.1 If the F206 target runs at speeds other than 20Mhz, the flash algorithms have to be modified. Go to step D.7 and update the algorithm file, before moving on to step D.3.2.
(*The flash algorithm Level 2 code (COFFA.out) for the serial programming is linked to run at the SARAM address 0x8000h. Location 0x8400(PM) and 0C00(DM) are reserved for flash algorithms and flash code buffer respectively)*

D.4 Setting up F206- host link

D.4.1. Connect the serial cable between PC/host (COM1/COM2 /COM3/COM4 port) and F206 target board asynchronous serial port.

D.4.2. Reset the target F206 board and invoke the F206sldr.exe on the PC side.
Select the configuration file with options as explained in step D.2.

D.4.3. Select continuous mode or non continuous mode. If non continuous mode is selected the host utility will update the communication status window with error code and display loading Done!. If continuous mode is selected, the host program after loading, will start sending character ‘a’ again and wait for valid echo from F206 to start another loading sequence. This is intended to initiate continuous loading without any menu selection on the host terminal. While this mode is selected new F206 circuit boards could be plugged after every loading complete indication. Refer to D.6 for loading status and error indications

D.5 Invoking the serial loaders

D.5.1. Invoke “Start loading” menu for the serial loader to communicate with the F206 device

D.5.2 Once the Level 2 program is transferred to F206, the XF bit will be cleared and the XF pins will go low. At this point the flash function will get initiated. After the flash function is complete (that is clearing erasing, or programming based on SFLAG value) the XF bit will toggle forever. Which would indicate the flash function is complete else there is an error in the communication or flash function.

D.6 Programming and communication status

D.6.1 Communication status window on the host terminal

The host serial loader software will update a communication status window during the loading process. Refer to section B.2.2 for details.

D.6.2 Communication status using RS232 signals

The DTR and RTS signals are bit outputs issued from the host RS232 serial port. These bits are used to indicate the status of loading and error conditions. If LEDs or RS232 line monitor are used on the DTR and RTS lines, then these bits will provide visual status of the serial loading process.

a. DTR - Bit output - Active low. Indicates the host received a valid echo from F206 device and loading is in progress.
   - High initially, and after successful loading.
b. RTS - bit output - Active low. Indicates there is an error while loading. Could be due to algorithms or communication. Will remain low until the F206 board is reset or a new board is plugged and the serial loader receives a valid character ‘a’ as echo. Refer to section B.2.2 for details.

Note: If XF bit is tied to an LED (as in some C2xx EVM’s) then the LED would flash indicating the status of the flash loader. This function can be modified to suit customer specific indicators. Refer to c2xx_sla.asm source code for application specific changes.

D.7. Procedure to rebuild flash algorithms for variable CLKOUT1 speeds.

D.7.1. This version of the serial loader utility is not intended for variable CLKOUT1 clock on the F206 devices. It is recommended that the flash utilities be used at 20Mhz CLKOUT1.

The flash algorithms are being optimized for variable speeds and programming time. Future revisions of this software utility will illustrate this feature.

D.7.1 Go to step D.3.2

E. F206 serial loader command tables

E.1 SFLAG command definitions for flash programming

Refer to JTAG programming utilities rev 2.0 documentation for on-chip flash programming basics.

SFLAG is a memory variable used to select flash functions CLEAR,ERASE and PROGRAM on Flash 0 or Flash 1 array. SFLAG can be defined in program or updated using application programs, before calling the required flash functions. In the Rev 2.0 flash programmer SFLAG variable is defined in the software screen and could be saved in a configuration file for future use.

Figure 4 SFLAG memory variable bit definitions

15	14	13	12 - 3	2	1	0
Select Flash array 1	Select Flash array 0	Select Flash0 and 1 Program	Reserved	PROGRAM	ERASE	CLEAR
R/W	R/W	R/W		R/W	R/W	R/W

Table 1 SFLAG bit commands used to select flash functions

Bit	Name	Function Bit =1 is select and Bit = 0 is deselect
0	C	Clear the selected flash array (selected by bits 14 or 15)
1	E	Erase the selected flash array (selected by bits 14 or 15)
2	P	Program the selected flash array (selected by bits 14 or 15)
3		Reserved
...		Reserved
...		Reserved
12		Reserved
13	F01	Bit to select special function in rev 2.0 s.w Selecting this bit along with F0,F1 and CEP bits, will enable the flash algorithms 2.0 to prepare the new F206 device for programming Flash 0 and Flash 1 array with 32k words of flash data. This primarily skips Flash 1 array clear and erase as it comes in erased state.
14	F0	Select Flash 0 array for any of the flash functions Clear, Erase, Program
15	F1	Select Flash 1 array for any of the flash functions Clear, Erase, Program

Note:
Select SFLAG bits to be 0xe007 for fast programming of Flash 0 and 1 array on new F206 devices. This selection will Clear, Erase flash 0 array and program Flash0 and Flash 1 arrays. Flash 1 array comes in erased state, ready for programming. Flash 0 is cleared and erased to remove the Level 1 loader code shipped with the device.

Table 2 SFLAG command table

	SFLAG command (Used in COFFA.out)	SFLAG value in Hex	Flash utility function	Host function
		0000	Nop	-----
1	F0_CLR	4001	Clear Flash 0	-----
2	F0_ERS	4002	Erase Flash 0	-----
3		4003	Clear & Erase Flash 0	-----
4	F0_PGM	4004	Program Flash 0	-----
5	F0_FN1	4005	Reserved	-----
6	F0_FN2	4008	Reserved	-----
7	F0_FN3	6000	Program Flash 0 or 1*	-----
8	F0_FN4	6003	Clear, Erase and Program *	
9		0000	Nop	-----
10	F1_CLR	8001	Clear Flash 1	-----
11	F1_ERS	8002	Erase Flash 1	-----
12		8003	Clear & Erase Flash 1	-----
13	F1_PGM	8004	Program Flash 1	-----
14	F1_FN1	8005	Reserved	-----
15	F1_FN2	8008	Reserved	-----
16	F1_FN3	a000	Program Flash 0 or 1 *	-----
17	F1_FN4	a003	Clear, Erase and Program *	-----
18	F1_FN11	2000	Selects special mode for rev 2.0	-----

Note : * Indicates that the program module in rev 2.0 can handle 32k words of flash code, the array selection is based on the COFF sections in the COFF file.

E.2 HFLAG flag command definitions for flash programming

HFLAG - 16 bit memory variable used by Level 2 of the serial loader in F206 to decide on host status, while transferring COFF files. More useful in future versions of the serial loaders.

Figure 5 HFLAG memory variable bit definitions

15 - 8	7	6-0
Reserved	More_data	Reserved
R/W	R/W	R/W

Table 3 HFLAG bit command description

Bit	Name	Function Bit =1 is select and Bit = 0 is deselect
0	--	Reserved
.....	---	Reserved
6	--	Reserved
7	More_data	1= Host has more COFF data to send. 0 = Last COFF section
8-15	---	Reserved

Table 4 HFLAG command table

	HFLAG commands	HFLAG value hex		Host actions
1	No_More_data	0000 0001	-----	Host sends last flash data
2	More_data	1000 0001	-----	Host will send more flash data
3		1000 xxxx	-----	

E.3 H_CMDS flag command definitions for flash programming

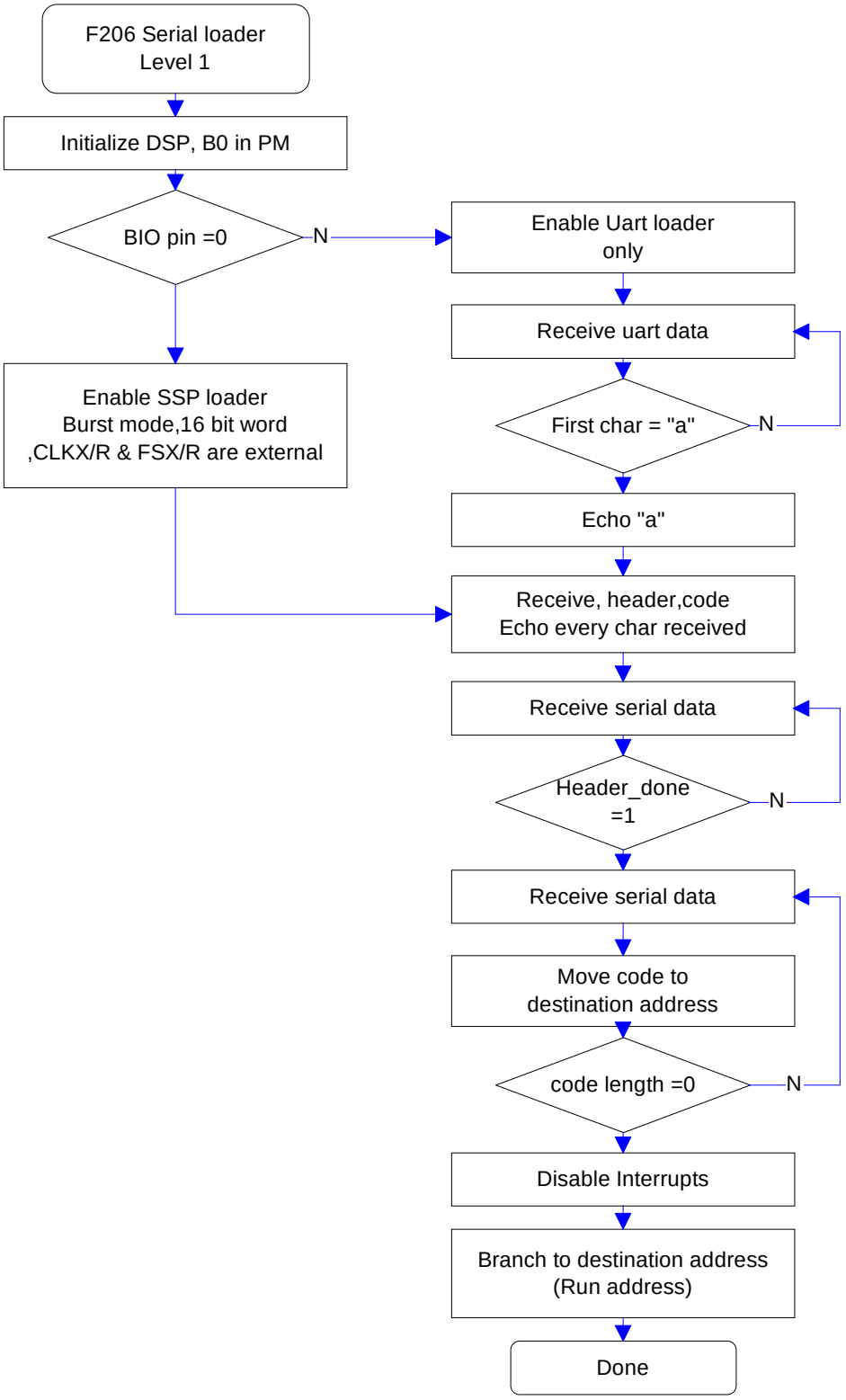
H_CMD - 8 bit commands issued by Level 2 of the serial loader to indicate F206 status to the PC/Host. Refer to the serial loader Level 2 source code for more details.

Table 5 H_CMDS command table

	H_CMDS commands (Used in COFFA.out)	H_CMDS in hex		Host requests
1	H_sflag_req	0001 0000	-----	Request for new SFLAG
2	H_coffc_req	0010 0000	-----	Request COFFC
3	H_alg_err	0011 0000	-----	Algorithm error
4	H_com_err	0100 0000	-----	Communication Error
5	H_done	0101 0000	-----	Done
6	H_rung	0110 0000	-----	Algorithm running
7	H_CMD1	0111 0000	-----	Reserved
8	H_CMD2	1000 0000	-----	Reserved

F. Serial loader flow charts and tools

F.1 TMX320F206 Flash Serial loader - F206 Level 1



F.2 Suggested tools for external indication of the serial loading process.

The host serial loader utility enables the host RS232 serial port lines DTR and RTS to indicate the status of the flash programming and error. These lines could be monitored by external circuits to provide visual indication of the flash loading process. Two inexpensive and useful methods are explained below.

F.2.1 RS232 line monitor

Use a standard inexpensive RS232 line monitor in series with the RS232 cable at the F206 device end. These monitors have LED's on the RS232 line signals, and provide visual indication of the line activity. DTR and RTS LED's will provide Loading status and error conditions. While using long RS232 cables to connect to the F206 circuit boards, the line monitors, would indicate the programming status at the remote end. Refer to section D.6 for DTR, RTS signal status.

RS 232 Line Monitor

Loading (DTR) - O

Error (RTS) - O

F.2.2 Dedicated RS232 line monitor

If the F206 applications do not use the on-chip UART , then adding RS232 line buffers to the serial port may not be cost effective and useful, except for initial programming. For such applications the circuit below could be a useful tool along with the serial loader.

A simple RS232 line monitor could be designed with RS232 line driver (such as MAX 232 line driver) to to convert the host RS232 signals into TTL signals. DTR and RTS signals could be connected to LED's to provide line indication. The F206 board should provide the power to the RS232 line driver. Basically the line driver board should have four lines connected to the F206 board as shown.