TMS320C6x EMIF to External SBSRAM Interface

APPLICATION REPORT:

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Texas Instruments

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Contents

Abstract **7**
Interface of EMIF with SBSRAM **8**
Termination of Unused Pins 10
Overview of EMIF **11**
EMIF Signal Descriptions 11
EMIF Registers 13
EMIF Global Control Register 13
CE Space Control Registers 14
SBSRAM Operations **15**
Half Speed Write 16
Half Speed Read 17
Full Speed Write 18
Full Speed Read 19
Optimizing SBSRAM Accesses 20
Timing Constraints **21**
Half Speed 22
C6x Outputs(ED, EA, CE, BE, SSADS, SSOE, SSWE) 22
C6x Inputs (Output Data from the SBSRAM, read ED) 23
Full Speed 24
C6x Outputs(ED, EA, CE, BE, SSADS, SSOE, SSWE) 24
C6x Inputs (Output Data from the SBSRAM, read ED) 25
Timing Comparisons for Three SBSRAMs 26
Complete Example – Half Speed **29**
Register Configuration 30
EMIF Global Control Registers 30
EMIF CE2 Space Control Register 31
Code Segment 32
Complete Example – Full Speed **33**
Register Configuration 34
EMIF Global Control Registers 34
EMIF CE2 Space Control Register 34
Code Segment 36

Figures

Figure 1. EMIF – x36 SBSRAM Interface 8
Figure 2. EMIF – x18 SBSRAM Interface 9
Figure 3. Block Diagram of EMIF SBSRAM Interface 11
Figure 4. EMIF Global Control Register Diagram 13
Figure 5. EMIF CE(0/1/2/3) Space Control Register Diagram 14
Figure 6. SBSRAM Write - Half Speed 16
Figure 7. SBSRAM Read - Half Speed 17
Figure 8. SBSRAM Write - Full Speed 18
Figure 9. SBSRAM Read - Full Speed 19

Figure 10. Outputs from C6x (Write Data (ED), Control, and Address Signals) 22
Figure 11. Output Data from SBSRAM 23
Figure 12. Outputs from C6x (Write Data (ED), Control, and Address Signals) 24
Figure 13. Output Data from SBSRAM 25
Figure 14. EMIF Global Control Register Diagram 30
Figure 15. EMIF CE2 Space Control Register Diagram 31
Figure 16. EMIF Global Control Register Diagram 34
Figure 17. EMIF CE2 Space Control Register Diagram 34

Tables

Table 1. Termination of Unused Pins 10
Table 2. EMIF SBSRAM Pins 12
Table 3. EMIF Memory Mapped Registers for SBSRAM 13
Table 4. EMIF Global Control Register Bit Field Description for SBSRAM 14
Table 5. Timing Comparisons for SBSRAM at Half Speed 27
Table 6. Timing Comparisons for SBSRAM at Full Speed 28
Table 7. SDRAM Registers 30
Table 8. SDRAM Registers 34

TMS320C6x EMIF to External SBSRAM Interface

Abstract

Interfacing external SBSRAM to the TMS320C62xx is simple when compared to previous generations of TI DSPs due to the advanced External Memory Interface (EMIF), which provides a glueless interface to a variety of external memory devices.

This document will describe the:

- EMIF's control registers and SBSRAM signals
- Interface schematic of x32/36 and x18 SBSRAM devices
- SBSRAM functionality and performance considerations,
- Timing analysis of Micron's MT58LC32K32D80-10 SBSRAM (32k x 32) with Half Speed interface
- Timing analysis of Samsung's KM736V689/L-7 SBSRAM (64k x 36) with Half Speed interface
- Timing analysis of Samsung's KM736V789/L-6 SBSRAM (128k x 36) with Full Speed interface
- Complete software example of both Half Speed and Full Speed interface

Interface of EMIF with SBSRAM

As shown in Figure 1, the EMIF interfaces directly to 32 bit wide industry standard synchronous burst SRAMs. SBSRAMs are available in both Flow Through and Pipeline, however, the ‘C6x interfaces only to Pipeline SBSRAM, which has the capability to operate at higher frequencies with sustained throughput.

The SBSRAM interface allows a high speed memory interface without some of the limitations of SDRAM. Most notably, since SBSRAMs are SRAM devices, random accesses in the same direction may occur in a single cycle. The SBSRAM interface may run at either the CPU clock speed or at ½ of this rate, based on the setting of the SSCRT bit in the EMIF Global Control Register.

Figure 1 shows the connections used to interface to a 36 bit wide SBSRAM. For this interface, the 4 parity bits of the SBSRAM should be tied to ground through a resistor, since the ‘C6x data bus is only 32 bits wide and can not take advantage of the parity bits. This interface is almost identical to the interface to a 32 bit wide SBSRAM, except that a 32 bit wide SBSRAM will have No Connects instead of parity bits.

Figure 1. EMIF – x36 SBSRAM Interface

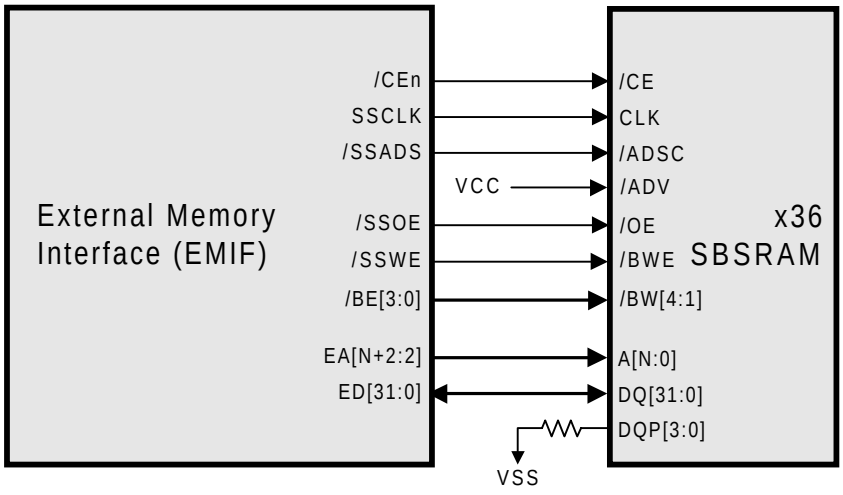
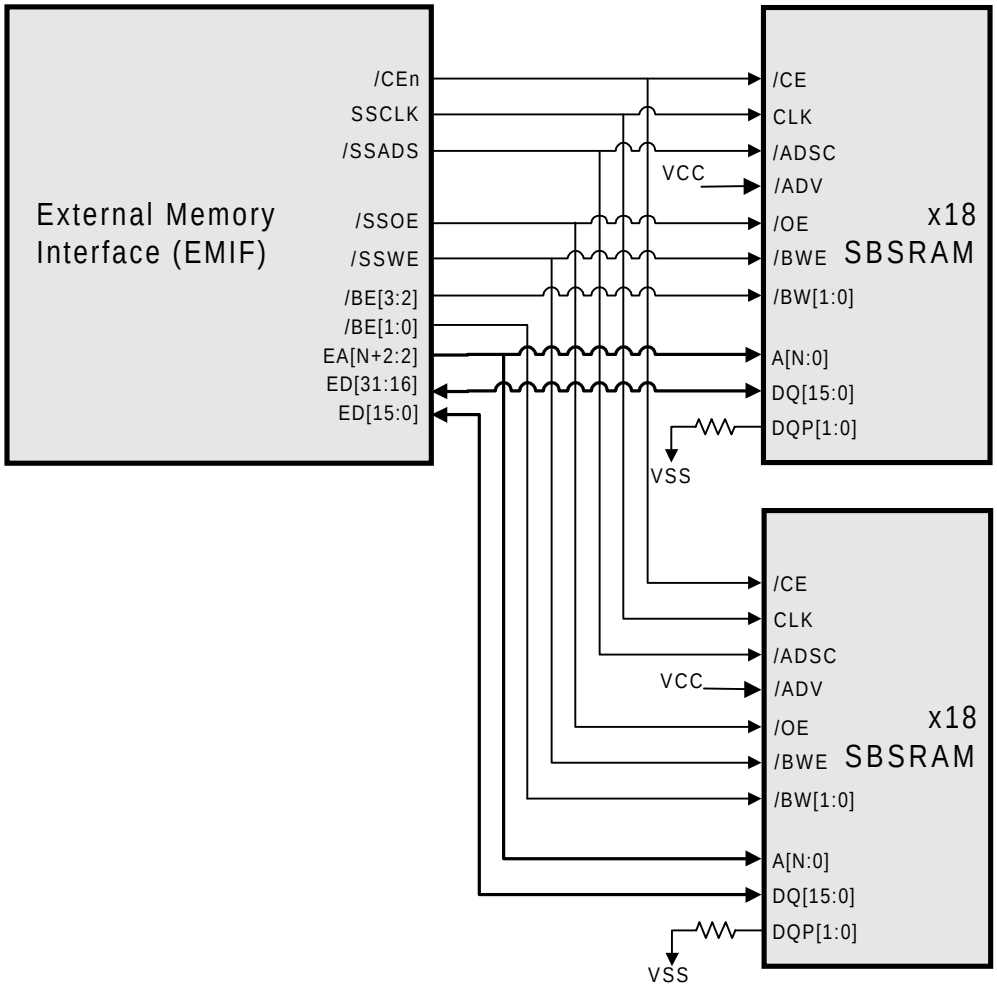


Figure 2 shows the connections used to interface to two 18 bit wide SBSRAMs. For this example, two SBSRAMs must be used in parallel to interface to the 32 bit wide data bus of the ‘C6x. The parity bits of the SBSRAMs are tied to ground through a pull down resister.

Figure 2. EMIF – x18 SBSRAM Interface



The four SBSRAM control signals are latched by the SBSRAM on the rising SSCLK edge to determine the current operation. These signals are only valid if the chip select line for the SBSRAM is low. The /ADV signal is used to allow the SBSRAM device to generate addresses internally for interfacing to controllers which cannot provide addresses quickly enough, but the EMIF does not need to use this signal because it generates the addresses at the required rate.

As mentioned, the SSCRT (SBSRAM Clock Rate Select) bit in the EMIF Global Control Register can configure SSCLK to operate at either full speed (SSCLK = CLKOUT1) or half speed (SSCLK = CLKOUT2 = ½ CLKOUT1). However, advantages and disadvantages are associated with each configuration.

The biggest disadvantage for the Full Speed Interface is that the CPU runs at the same clock rate as the SBSRAM. Since, SBSRAMs are common at speeds up to 133 MHz and are emerging in the 166 MHz range, the CPU will not be able to operate at its peak rate, which is 200 MHz. Therefore, if the improvement in throughput for memory accesses is worth the sacrifice in CPU speed, then a full speed interface should be used.

If a half rate interface is used, then the CPU clock rate can be operated at the peak speed of 200 MHz, giving a slightly slower SSCLK rate of 100 MHz.

Whether a full speed or half speed interfaces is selected, it is important to verify that the timing parameters of the SBSRAM meet the requirements of the ‘C6x.

Termination of Unused Pins

Table 1 summarizes the connections that should be made to the SBSRAM for unused pins in order to guarantee desired operation.

Table 1. Termination of Unused Pins

Terminate to:	Pin Description
GND	/CE2
GND	MODE
GND	ZZ
GND	VSS
3.3V	VCC
3.3 V	CE2
3.3 V	/ADV
3.3 V	/ADSP
3.3 V	/GW
1kΩ to GND	Parity Data

Overview of EMIF

EMIF Signal Descriptions

Figure 3 shows a block diagram of the EMIF, the interface between external memory and the other internal units of the ‘C6x. The interface with the processor is provided via the DMA controller, Program Memory Controller, and the Data Memory Controller. The signals described in Table 2 describe the SBSRAM interface and the shared interface signals.

Figure 3. Block Diagram of EMIF SBSRAM Interface

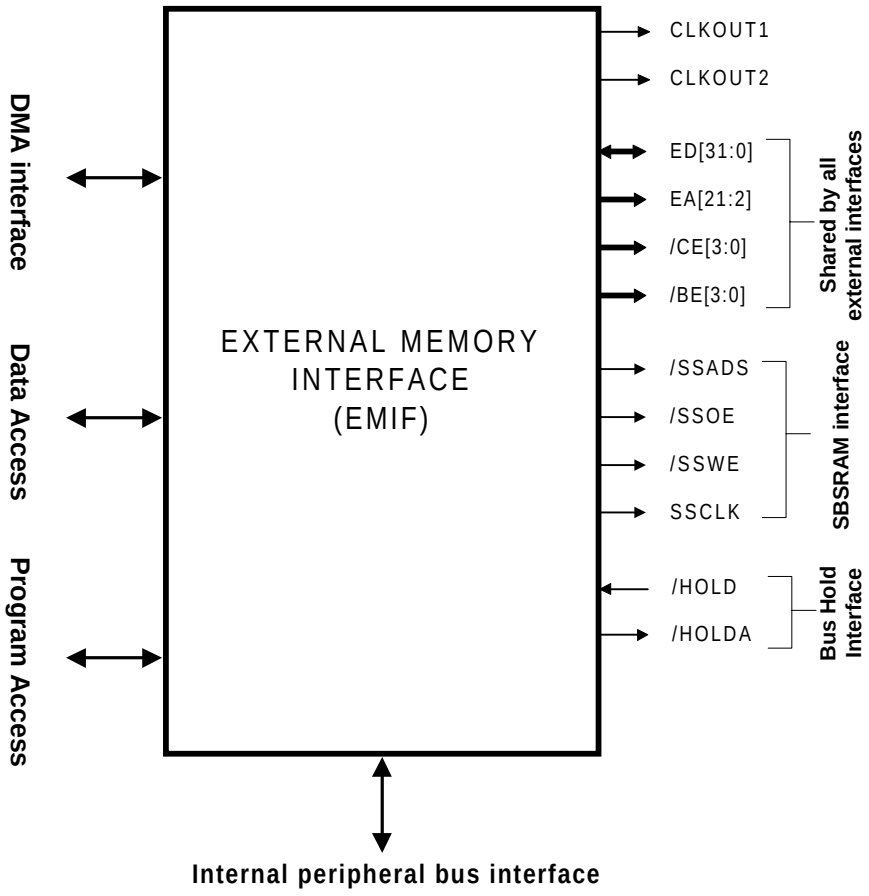


Table 2. EMIF SBSRAM Pins

EMIF Signal	SBSRAM Signal	SBSRAM Function
/CEn	/CE	Chip Enable. /CE must be active (low) for a command to be clocked into the SBSRAM.
SSCLK	CLK	SBSRAM Clock. Runs at either 1x or 1/2x the CPU rate.
SSADS	/ADSC	Synchronous Address Strobe: Causes a new external address to be registered. If /CE is active, then a READ or WRITE is performed.
/SSOE	/OE	Output Enable. Enables the data I/O drivers.
/SSWE	/BWE	Write Enable. Permits write operations.
/BE[3:0]	/BW[4:1]	Byte Write Enables. Allow individual bytes to be written when /BWE is active. A Byte Write Enable is LOW for a WRITE and DON'T CARE for a READ cycle. /BW1 controls Byte 1, /BW2 controls Byte 2, /BW3 controls Byte 3, and /BW4 controls Byte 4.
EA[N+2:2]	A[N:0]	Address Inputs. Registered on rising edge of SSCLK.
ED[31:0]	DQ[32:1]	Data I/O. Byte 1 is DQ[8:1], Byte 2 is DQ[16:9], Byte 3 is DQ[24:17], and Byte 4 is DQ[32:25].

EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory mapped registers within the EMIF. A write to any EMIF register will not complete until all pending EMIF accesses which use that register have completed. The memory mapped registers are shown in Table 3.

Table 3. EMIF Memory Mapped Registers for SBSRAM

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control

EMIF Global Control Register

The EMIF Global Control Register (Figure 4) configures parameters common to all the CE spaces. Table 4 only lists those parameters that are relevant for use with SBSRAM.[1]

Figure 4. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
reserved	Reserved	rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
R, +0	R, +1	R, +0	R, +x	R, +x	R, +0	RW, +0	RW, +1	RW, +1	RW, +1	RW, +1	RW, +0	RW, +0	R, +x

[1] For a description of all of the parameters of the EMIF Global Control Register, see the TMS320C62xx Peripherals Reference Guide.

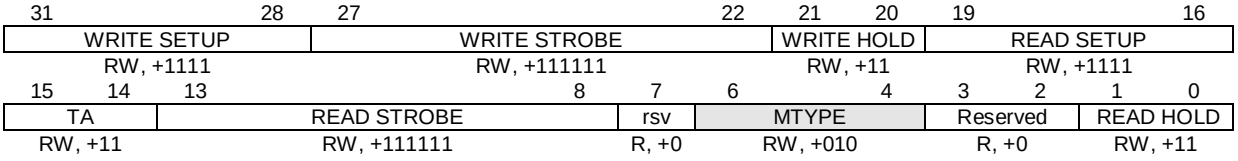
Table 4. EMIF Global Control Register Bit Field Description for SBSRAM

Field	Description
SSCEN	SSCLK enable
	SSCEN=0, SSCLK held high
	SSCEN=1, SSCLK enabled to clock
SSCRT	SBSRAM clock rate select
	SSCRT=0, SSCLK ½x CPU clock rate
	SSCRT=1, SSCLK 1x CPU clock rate

CE Space Control Registers

The four CE Space Control Registers (Figure 5) correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or Asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. The only field of interest for SBSRAM is the MTYPE field, which should be set to 100b to indicate 32 bit wide SBSRAM in the corresponding CE space. Modification of a CE Space Control Register does not occur until that CE space is inactive.

Figure 5. EMIF CE(0/1/2/3) Space Control Register Diagram



SBSRAM Operations

The SBSRAM interface is capable of operating at either the CPU clock speed or at ½ of the CPU clock speed.

For the full speed SBSRAM interface, the output signals are triggered off of a rising edge of SSCLK, in order to give as much setup time as possible to the SBSRAM device. For the half speed SBSRAM interface, the output signals are triggered off of a falling edge of SSCLK since the timing is not as critical, leaving almost a half cycle of setup to the SBSRAM.

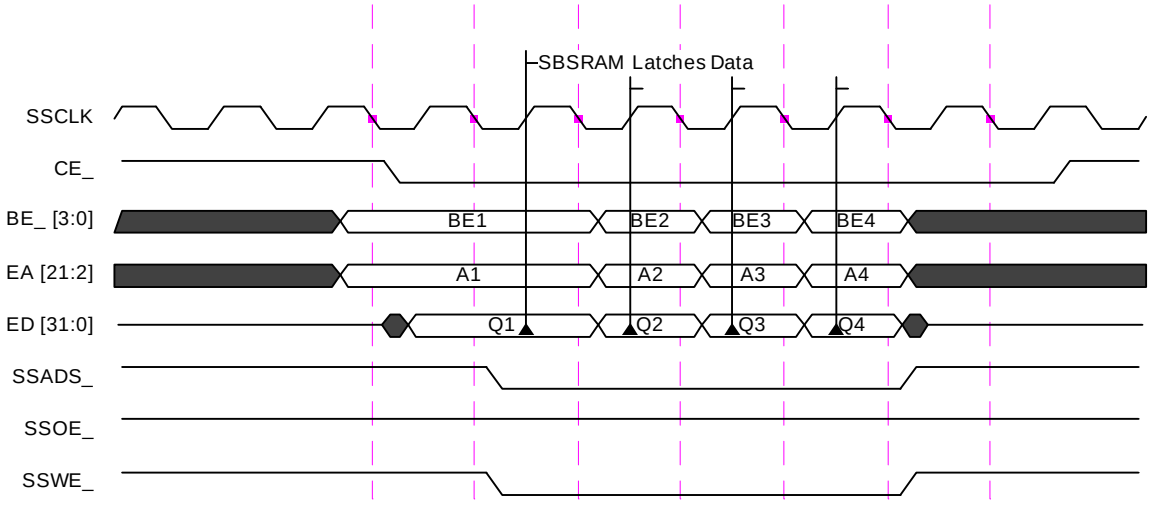
The following sections illustrate the differences between the two modes of operation.

Half Speed Write

Figure 6 shows a 4 word write to SBSRAM, with SSCLK = ½ CLKOUT1. Every access strobes a new address into the SBSRAM. The first access requires an initial startup penalty of at least 3 SSCLK cycles; thereafter all access can occur in a single SSCLK cycle. This startup penalty is to ensure that there is no contention over the data bus due to a previous read.

The data, address, and control signals for a half speed write are all triggered off of the falling edge of SSCLK. Since for a half speed write, the data, control, and address lines are triggered off of the falling edge, less than a half of a cycle of setup time is provided to the SBSRAM.

Figure 6. SBSRAM Write - Half Speed

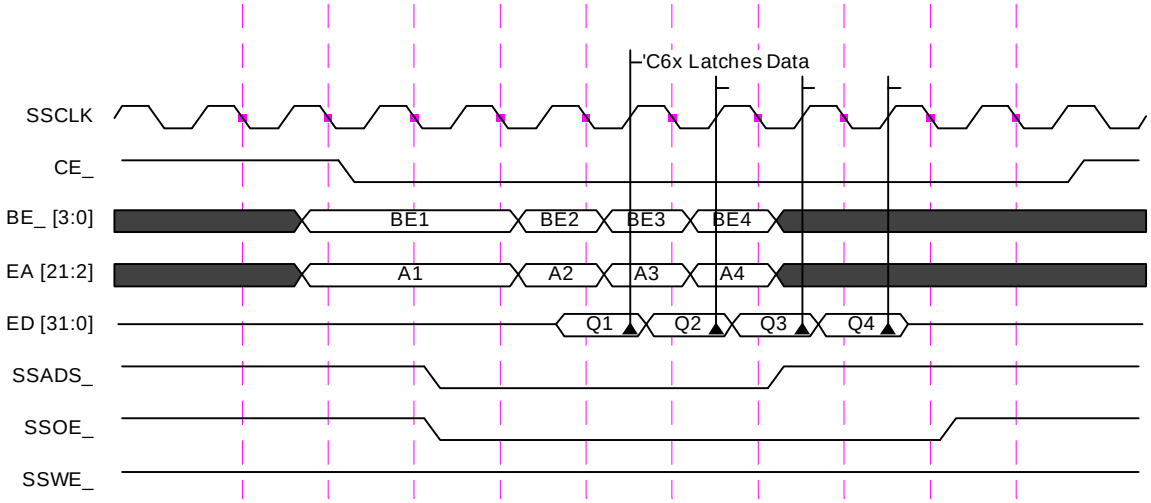


Half Speed Read

Figure 7 shows a 4 word read of an SBSRAM at half speed (SSCLK = CLKOUT2 = ½ CLKOUT1). Every access strobes a new address into the SBSRAM, indicated by the /SSADS strobe low. The first access requires an initial read latency of 2 cycles; thereafter all accesses have single cycle throughput.

For an SBSRAM read at half speed, notice that the control signals and address signals (after the first access) are triggered by the falling edge of SSCLK, just as for the half speed write cycle, providing less than a half cycle of setup time for the SBSRAM.

Figure 7. SBSRAM Read - Half Speed

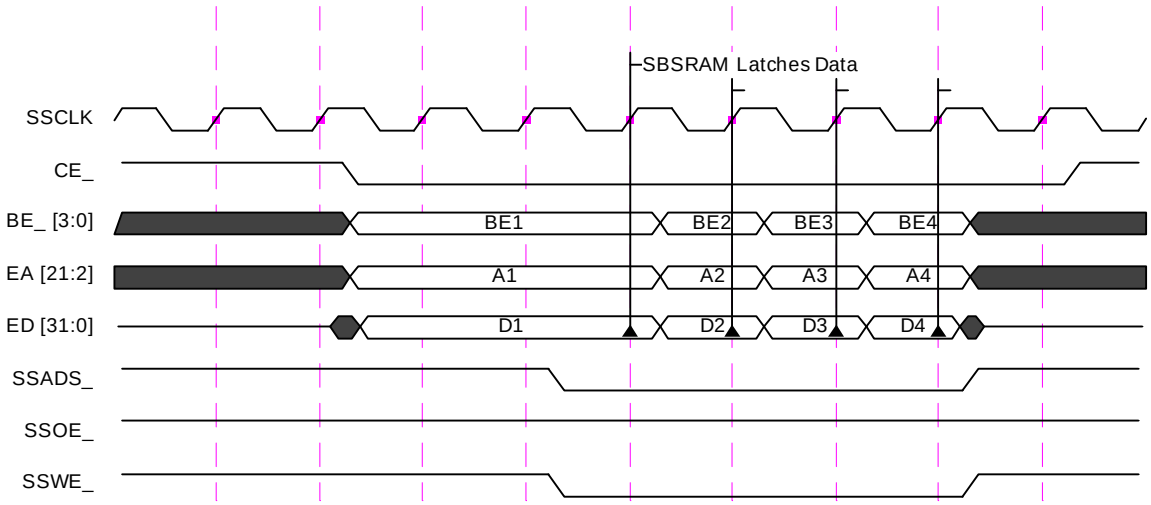


Full Speed Write

Figure 8 shows a 4 word write of an SBSRAM with SSCLK programmed to operate at the CPU clock speed. Every access strobes a new address into the SBSRAM. The first access requires an initial startup penalty of at least 3 cycles; thereafter all access can occur in a single SSCLK cycle. This startup penalty is to ensure that there is no contention over the data bus due to a previous read.

For an SBSRAM write at full speed, notice that the outputs from the 'C6x (control, address, and data signals) are triggered after the rising edge of SSCLK. Since the SBSRAM latches the inputs on the rising edge of SSCLK, this gives almost a full cycle of setup time for the inputs to the SBSRAM.

Figure 8. SBSRAM Write - Full Speed



SBSRAM WRITE TIMING

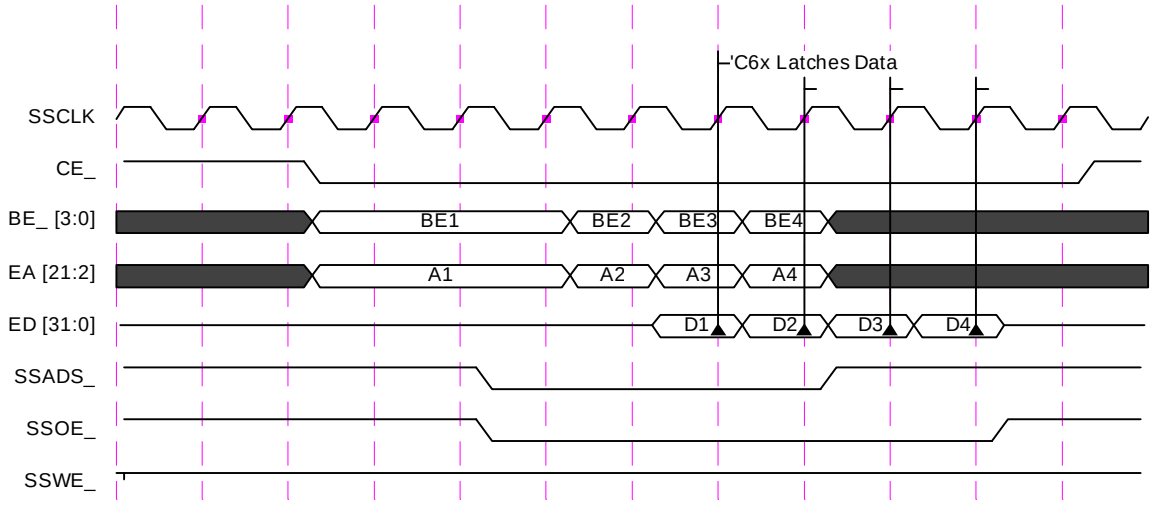
Full Speed Read

Figure 9 shows a 4 word read of an SBSRAM at full speed (SSCLK = CPU Clock Speed). Every access strobes a new address into the SBSRAM, indicated by the /SSADS strobe low. Pipeline SBSRAM has a read latency of two cycles. Once the data is strobed into the SBSRAM on the first rising SSCLK edge after /SSADS goes active, then data is latched by the C6x two cycles later. Although the first access requires a delay of 2 cycles before the data is present on the bus; each subsequent read has single cycle throughput.

The control and address signals for a full speed read are triggered off of the rising edge, and have the same timing constraints as for a full speed write.

The read data being output from the SBSRAM is also triggered by the rising edge of the SSCLK. Since the 'C6x latches the data on the rising edge of SSCLK, this gives almost a full cycle of setup time for the inputs to the C6x (less the access time of the SBSRAM).

Figure 9. SBSRAM Read - Full Speed



SBSRAM READ TIMING

Optimizing SBSRAM Accesses

SBSRAMs are latent by their architecture, meaning that read data follows address and control information. Consequently, the EMIF inserts cycles between read and write commands to ensure that no conflict exists on the ED[31:0] bus. The EMIF keeps this turn-around penalty to a minimum. The initial 3-cycle penalty is present when changing directions on the bus. In general, the rule is this; the first access of a burst sequence will incur at least a 3 cycle startup penalty. Therefore, to maximize throughput, an attempt should be made to keep direction changes on the data bus to a minimum when accessing SBSRAM.

Timing Constraints

This section will discuss the timing constraints used to determine if an SBSRAM can operate with the C6x at either full or half speed.

For the following constraint calculations, a time t_{margin} will be calculated, which represents the margin in the system after taking into account the worst case numbers from the data sheets of the memory and the 'C6x.

After calculating the time t_{margin}, it is a system level issue to determine if the proper amount of margin has been met. The required timing margin is extremely system dependent, depending primarily on trace length and loading, but other factors can come into play. Therefore, this parameter should be determined for the particular system in question.

In general, the timing margin required will not be the same for the different parameters of the read/write cycles. For output signals, the timing margin required will be minimal, since the output clock and the output control/data signals will both be propagating from the C6x to the SBSRAM. Therefore, the timing margin needs to account for the possible skew between the two signals (SSCLK vs Control/Data) caused by loading effects or differences in route length. For a well designed board, with relatively short board routes, the necessary margin can be estimated as approximately 0.5 ns for both output setup and output hold.

For reads, however, the timing margin required is more complicated. The issue with reads is that the memory is outputting data relative to a clock that has undergone a propegation delay when traveling from the C6x to the SBSRAM. The memory outputs the data a time t_{acc} from this delayed clock, and the output data from the memory undergoes a delay itself before arriving at the C6x. Therefore, the timing margin for read setup must account for these two propegation delays. The read hold time is improved because of this and the margin required can be considered negligible. For a well designed board, with relatively short leads, the input setup margin can be estimated as approximately 1.0 ns and the input hold margin can be estimated as 0 ns.

These numbers are guidelines and the actual margin required for any system may be different from these guidelines.

In the discussion below, an 'm' will be used to denote the memory specifications and no additional designators will be used to to denote the 'C6x timing specifications.

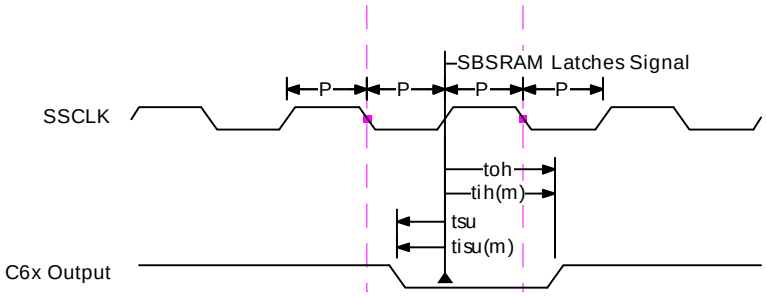
Half Speed

C6x Outputs(ED, EA, CE, BE, SSADS, SSOE, SSWE)

When operating at half speed, the C6x begins the output of address, data, and control signals on the falling edge of SSCLK, whereas the SBSRAM will latch these signals on the next rising edge of SSCLK. For simplicity, the TMS320C6x Data Sheet specifies the outputs as a setup time (tsu) to the next rising edge and a hold time (toh) from the previous rising edge so that the comparison between C6x specifications and memory specifications is extremely straightforward. The following equations, which are derived from Figure 10, should be used to calculate the timing margin between the C6x and the desired SBSRAM when using a half speed interface.

- Setup Time: Output setup time (t_{su}) from inactive to active must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the margin available is:
- $t_{margin} = t_{su} - t_{isu(m)}$
- Hold Time: Output hold time (t_{oh}) from active to inactive must be greater than the Hold Time required by the input ($t_{ih(m)}$). As seen in Figure 10, since the transition occurs t_{oh} after the rising edge of SSCLK and the input is read by the SBSRAM on the rising edge, this means that the hold time required by the input ($t_{ih(m)}$) must be less than the output hold time. The margin is then:
- $t_{margin} = t_{oh} - t_{ih(m)}$

Figure 10. Outputs from C6x (Write Data (ED), Control, and Address Signals)



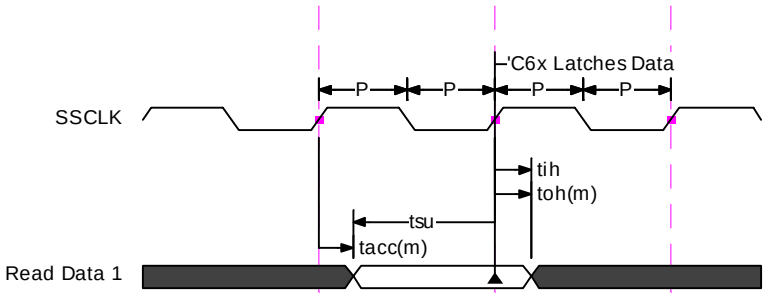
C6x Inputs (Output Data from the SBSRAM, read ED)

Figure 11shows the output data from the SBSRAM, as occurs during a read cycle. The situation is similar to the outputs from the C6x, except the SBSRAM must provide an ample setup and input hold to the C6x.

The constraints can be expressed as follows:

- Setup Times: The access time ($t_{acc(m)}$) of the SBSRAM must provide a large enough input setup time (t_{su}) for the input to the C6x. The P used here refers to the period of the CPU clock, which is equal to half the period of half speed SSCLK.
- $t_{margin} = 2P – (t_{acc(m)} + t_{su})$
- Hold Times: the output hold time ($t_{oh(m)}$) for data output from the SBSRAM, must provide a hold time greater than the hold time required by the input (t_h) of the C6x.
- $t_{margin} = t_{oh(m)} - t_h$

Figure 11. Output Data from SBSRAM



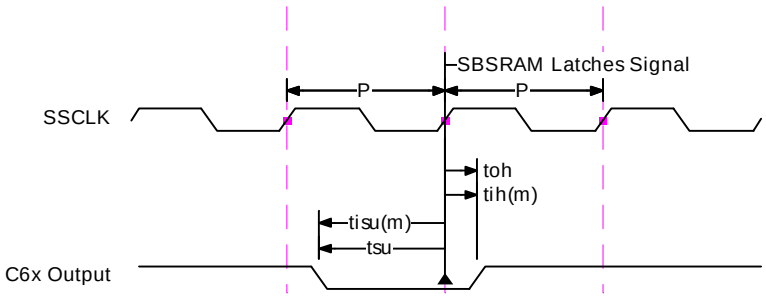
Full Speed

C6x Outputs(ED, EA, CE, BE, SSADS, SSOE, SSWE)

When operating at full speed, the C6x begins the output of address, data, and control signals on the rising edge of SSCLK, whereas the SBSRAM will latch these signals on the next rising edge of SSCLK. For simplicity, the TMS320C6x Data Sheet specifies the outputs as a setup time (tsu) to the next rising edge and a hold time (toh) from a rising edge so that the comparison between C6x specifications and memory specifications is extremely straightforward. The following equations, which are derived from Figure 12, should be used to calculate the timing margin between the C6x and the desired SBSRAM when using a full speed interface.

- Setup Time: Output setup time (t_{su}) from inactive to active must provide an ample setup time ($t_{isu(m)}$) for the input. Therefore, the timing margin is:
- $t_{margin} = t_{su} - t_{isu(m)}$
- Hold Time: Output hold time (t_{oh}) from active to inactive must be greater than the Hold Time required by the input ($t_{ih(m)}$). As seen in Figure 12, since the transition occurs t_{oh} after the rising edge of SSCLK and the input is read by the SBSRAM on the rising edge, this means that the hold time required by the input ($t_{ih(m)}$) must be less than the output hold time. The margin is:
- $t_{margin} = t_{oh} - t_{ih(m)}$

Figure 12. Outputs from C6x (Write Data (ED), Control, and Address Signals)



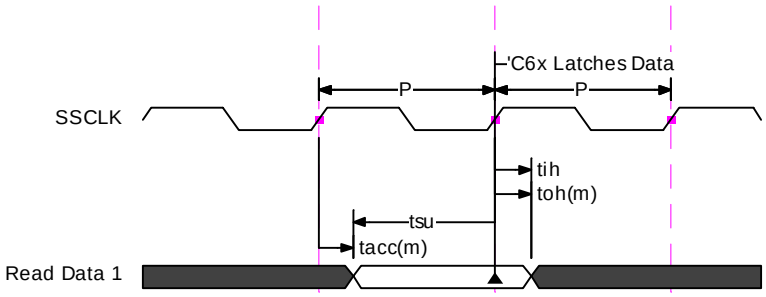
C6x Inputs (Output Data from the SBSRAM, read ED)

Figure 13 shows the output data from the SBSRAM, as occurs during a read cycle. The situation is similar to the outputs from the C6x, except the SBSRAM must provide an ample setup and input hold to the C6x.

The constraints can be expressed as follows:

- Setup Times: The access time (tacc(m)) of the SBSRAM must provide a large enough input setup time (tsu) for the input to the C6x. The P used here refers to the period of CLKOUT1, which is equal to the period of full speed SSCLK.
- $t_{margin} = P – (t_{acc(m)} + t_{su})$
- Hold Times: the output hold time (toh(m)) for data output from the SBSRAM, must provide a hold time greater than the hold time required by the input (th) of the C6x. The margin is:
- $t_{margin} = t_{oh(m)} - t_h$

Figure 13. Output Data from SBSRAM



Timing Comparisons for Three SBSRAMs

This section summarizes the comparisons listed above for two different SBSRAMs using a half speed interface and one SBSRAM using a full speed interface.

For the half speed interface, the example shown in Table 5 uses a CPU clock speed of 200 MHz, which gives a half speed SBSRAM interface at 100 MHz. The Micron part listed (-10) is a 100 MHz device, and as seen in Table 5, give slightly less margin than the Samsung (-7) 133MHz device when operating with a 100 MHz SSCLK. Both speed grades are shown here to illustrate that additional timing margin is attainable by using faster SBSRAMs. Several vendors have SBSRAM devices available at 100 MHz or faster, and since new data sheets are constantly becoming available, the newest data sheets should be compared to the 'C6x Data Sheet in order to guarantee operation with the desired margins.

- Micron's MT58LC32K32D8-10 is 32k x 32 bits
- Samsung's KM736V689/L-7 is 64k x 36 bits

For the full speed interface, the example shown uses a CPU clock speed and a SSCLK speed of 166 MHz. This is because no SBSRAM parts currently exist which offer a clock speed of faster than 166 MHz. Therefore, in order to use the full speed SBSRAM interface, the CPU clock speed must be sacrificed. For applications which require very high speed memory access, this tradeoff may be worthwhile.

- Samsung's KM736V789/L-6

Table 5. Timing Comparisons for SBSRAM at Half Speed

Given : P = 5 ns			**Margin**	**Satisfied ?**
C6x Output Setup Time		t_{su} = P – 2.3 ns	$t_{margin} = t_{su} - t_{isu(m)}$	
SBSRAM Input Setup Time	Micron's MT58LC32K32D8-10	$t_{su(m)}$ = 2.2 ns	t_{margin} = 0.5 ns	✔
	Samsung's KM736V689/L-7	$T_{su(m)}$ = 2.0	t_{margin} = 0.7	✔
C6x Output Hold Time		t_{oh} = P – 4 ns	$t_{margin} = t_{oh} - t_{ih(m)}$	
SBSRAM Input Hold Time	Micron's MT58LC32K32D8-10	$t_{ih(m)}$ = 0.5 ns	t_{margin} = 0.5 ns	✔
	Samsung KM736V689/L-7	$t_{ih(m)}$ = 0.5 ns	t_{margin} = 0.5 ns	✔
C6x Input Setup Time		t_{su} = 3.6 ns	$t_{margin} = 2P - (t_{acc} + t_{su})$	
SBSRAM Output Access Time	Micron's MT58LC32K32D8-10	$t_{acc(m)}$ = 5.0 ns	t_{margin} = 1.4 ns	✔
	Samsung KM736V689/L-7	$t_{acc(m)}$ = 4.5 ns	t_{margin} = 1.9 ns	✔
C6x Input Hold Time		t_h = 1.2 ns	$t_{margin} = t_{oh(m)} - t_h$	
SBSRAM Output Hold Time	Micron's MT58LC32K32D8-10	$t_{oh(m)}$ = 1.5 ns	t_{margin} = 0.3 ns	✔
	Samsung KM736V689/L-7	$t_{oh(m)}$ = 1.5 ns	t_{margin} = 0.3 ns	✔

Table 6. Timing Comparisons for SBSRAM at Full Speed

Given : P = 6 ns			**Margin**	**Satisfied ?**
C6x Output Setup Time		t_{su} = P – 4 ns	$t_{margin} = t_{su} - t_{isu(m)}$	
SBSRAM Input Setup Time	Samsung's KM736V789/L-6	$t_{su(m)}$ = 1.5 ns	t_{margin} = 0.5 ns	✔
C6x Output Hold Time		t_{oh} = 1 ns	$t_{margin} = t_{oh} - t_{ih(m)}$	
SBSRAM Input Hold Time	Samsung's KM736V789/L-6	$t_{ih(m)}$ = 0.5 ns	t_{margin} = 0.5 ns	✔
C6x Input Setup Time		t_{su} = 1.5 ns	$t_{margin} = P - (t_{acc} + t_{su})$	
SBSRAM Output Access Time	Samsung's KM736V789/L-6	$t_{acc(m)}$ = 3.5 ns	t_{margin} = 1 ns	✔
C6x Input Hold Time		t_h = 1.2 ns	$t_{margin} = t_{oh(m)} - t_h$	
SBSRAM Output Hold Time	Samsung's KM736V789/L-6	$t_{oh(m)}$ = 1.5 ns	t_{margin} = 0.3 ns	✔

Complete Example – Half Speed

This section walks through the register configuration for interfacing the C6x with SBSRAM at half speed. Since there are no SBSRAM parameters that directly tie the EMIF settings to a specific SBSRAM, this software example is generic to any SBSRAM device.

If a single 32 or 36 bit wide SBSRAM is used, then the block diagram for the interface schematic is identical to that shown in Figure 1. If two 18 bit wide devices are used in parallel, then the schematic is identical to Figure 2.

Assumptions:

- CLKOUT1 frequency of 200 MHz
- 100 MHz SBSRAM clock frequency.
  (SSCLK = ½ x CLKOUT1 frequency)
- SBSRAM to be located at CE2 (logical address 0x02000000)
- Assume CLKOUT1 not in use in the system
- Assume SDCLK, CLKOUT2 is being used in the system

Register Configuration

Table 7. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, SSCEN, CLK1EN, CLK2EN, SSCRT
EMIF CE2 Space Control	MTYPE

EMIF Global Control Registers

Since the SBSRAM will be driven by SSCLK, we must then set the following:

Figure 14. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	1	1	0	1	0	0	1

SDCEN = 1 indicates that SDCLK is enabled to clock, since we assume it is in use by the system

SSCEN = 1 Indicates that SSCLK is enabled, since it is driving the SBSRAM interface.

CLK1EN = 0 Indicates that CLKOUT1 is disabled, since we assume it is NOT in use by the system

CLK2EN = 1 Indicates that CLKOUT2 is enabled, assuming that it is in use by the system.

SSCRT = 0 Specifies a **half rate** SBSRAM Interface

Thus, a valid setting for the EMIF Global Control Register is 0x00003369.

For additional information on the remainder of the fields, see the *TMS320C6x Peripherals Reference Guide*.

EMIF CE2 Space Control Register

Figure 15. EMIF CE2 Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
Rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	100	00	11

MTYPE = 100 indicates that 32 bit wide SBSRAM is located in the CE2 address space. Since SBSRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF43.

Code Segment

The following code segment will set up the EMIF as described above, using The TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Enable CLKOUT2,SDCLK, and SSCLK*/
/*                    - Disable CLKOUT1 */
/*                    - Set for ½x SBSRAM interface */
RESET_BIT(&g_ctrl, SSCRT);
SET_BIT(&g_ctrl, CLK2EN);
RESET_BIT(&g_ctrl, CLK1EN);
SET_BIT(&g_ctrl, SSCEN);
SET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SBSRAM  */
LOAD_FIELD(&ce2_ctrl  ,MTYPE_32SBSRAM, MTYPE , MTYPE_SZ       );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

Complete Example – Full Speed

This section walks through the register configuration for interfacing the C6x with SBSRAM at full speed. Since there are no SBSRAM parameters that directly tie the EMIF settings to a specific SBSRAM, this software example is generic to any SBSRAM device.

If a single 32 or 36 bit wide SBSRAM is used, then the block diagram for the interface schematic is identical to that shown in Figure 1. If two 18 bit wide devices are used in parallel, then the schematic is identical to Figure 2.

Assumptions:

- CLKOUT1 frequency of 166 MHz
- 166 MHz SBSRAM clock frequency.
  (SSCLK = 1x CLKOUT1 frequency)
- SBSRAM to be located at CE2 (logical address 0x02000000)
- Assume CLKOUT1 is in use in the system
- Assume SDCLK, CLKOUT2 is NOT being used in the system

Register Configuration

Table 8. SDRAM Registers

Register Name	Fields Required
EMIF Global Control	SDCEN, SSCEN, CLK1EN, CLK2EN, SSCRT
EMIF CE2 Space Control	MTYPE

EMIF Global Control Registers

Since the SBSRAM will be driven by SDCLK, we must then set the following:

Figure 16. EMIF Global Control Register Diagram

31 14	13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Reserved	Rsv	/ARDY	/HOLD	/HOLDA	NOHOLD	SDCEN	SSCEN	CLK1EN	CLK2EN	SSCRT	RBTR8	MAP
0	1 1	0	0	1	1	0	0	1	1	0	1	0	1

SDCEN = 0 Indicates that SDCLK is disabled to clock, since we assume it is NOT in use by the system

SSCEN = 1 Indicates that SSCLK is enabled, since it is driving the SBSRAM interface.

CLK1EN = 1 Indicates that CLKOUT1 is enabled, since we assume it is in use by the system

CLK2EN = 0 Indicates that CLKOUT2 is disabled, since we assume it is NOT in use by the system

SSCRT = 1 Specifies a **full rate** SBSRAM Interface

Thus, a valid setting for the EMIF Global Control Register is 0x00003335.

For additional information on the remainder of the fields, see the *TMS320C6x Peripherals Reference Guide*.

EMIF CE2 Space Control Register

Figure 17. EMIF CE2 Space Control Register Diagram

31 28	27 22	21 20	19 16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
1111	111111	11	1111

15 14	13 8	7	6 4	3 2	1 0
Rsv	READ STROBE	Rsv	MTYPE	Reserved	READ HOLD
11	111111	0	100	00	11

MTYPE = 100 indicates that 32 bit wide SBSRAM is located in the CE2 address space. Since SBSRAM is configured for this space, the rest of the fields are irrelevant, since they refer to Asynchronous memory.

A valid setting for EMIF CE2 Space Control is 0xFFFFFF43.

Code Segment

The following code segment will set up the EMIF as described above, using The TMS320C6x Peripheral Runtime Support Control Library.

```
#include <emif.h>
.
.   /*OTHER USER CODE*/
.
/* Get default values for all EMIF registers */
unsigned int g_ctrl     = GET_REG(EMIF_GCTRL);
unsigned int ce0_ctrl   = GET_REG(EMIF_CE0_CTRL);
unsigned int ce1_ctrl   = GET_REG(EMIF_CE1_CTRL);
unsigned int ce2_ctrl   = GET_REG(EMIF_CE2_CTRL);
unsigned int ce3_ctrl   = GET_REG(EMIF_CE3_CTRL);
unsigned int sdram_ctrl = GET_REG(EMIF_SDRAM_CTRL);
unsigned int sdram_ref  = GET_REG(EMIF_SDRAM_REF);

/* Set Global Control - Disable CLKOUT2,SDCLK */
/*                    - Enable CLKOUT1 and SSCLK*/
/*                    - Set for 1x SBSRAM interface */
SET_BIT(&g_ctrl, SSCRT);
RESET_BIT(&g_ctrl, CLK2EN);
SET_BIT(&g_ctrl, CLK1EN);
SET_BIT(&g_ctrl, SSCEN);
RESET_BIT(&g_ctrl, SDCEN);

/* Configure CE2 as SBSRAM  */
LOAD_FIELD(&ce2_ctrl  ,MTYPE_32SBSRAM, MTYPE , MTYPE_SZ       );

/* Store EMIF Control Registers */
emif_init(g_ctrl, ce0_ctrl, ce1_ctrl, ce2_ctrl, ce3_ctrl,
                sdram_ctrl, sdram_ref);
.
.   /*OTHER USER CODE*/
.
```

References

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