TMS320C6x Interface to External Logic FIFOs

APPLICATION REPORT: PRELIMINARY

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TMS320C6x Interface to External Logic FIFOs

Abstract

Interfacing high speed external First In First Out Memories (FIFO) to the C62x is possible via the C62x's External Memory Interface (EMIF). The EMIF is designed for a flexible interface to a wide variety of external memory devices, however, since it will be necessary to use the Asynchronous Interface of the EMIF for the FIFO interface, glue logic will be necessary in order to implement the interface.

This document will describe the:

- EMIF's control registers and asynchronous interface signals
- FIFO types and characteristics,
- General example for each type of FIFO
- Full example for Strobed FIFO

Overview of EMIF

EMIF Signal Descriptions

Figure 1 shows a block diagram of the EMIF. As the figure shows, the EMIF is the interface between external memory and the other internal units of the C62x. The interface with the processor is provided via the DMA controller, Program Memory Controller (PMC), and the Data Memory Controller (DMC)[1]. The signals described in Table 1, however, focus on the asynchronous interface and the shared interface signals.

[1] For a more detailed description of the interface between the EMIF and the other internal units of the C62x, see the TMS320C62x Peripherals Reference Guide.

Figure 1. Block Diagram of EMIF

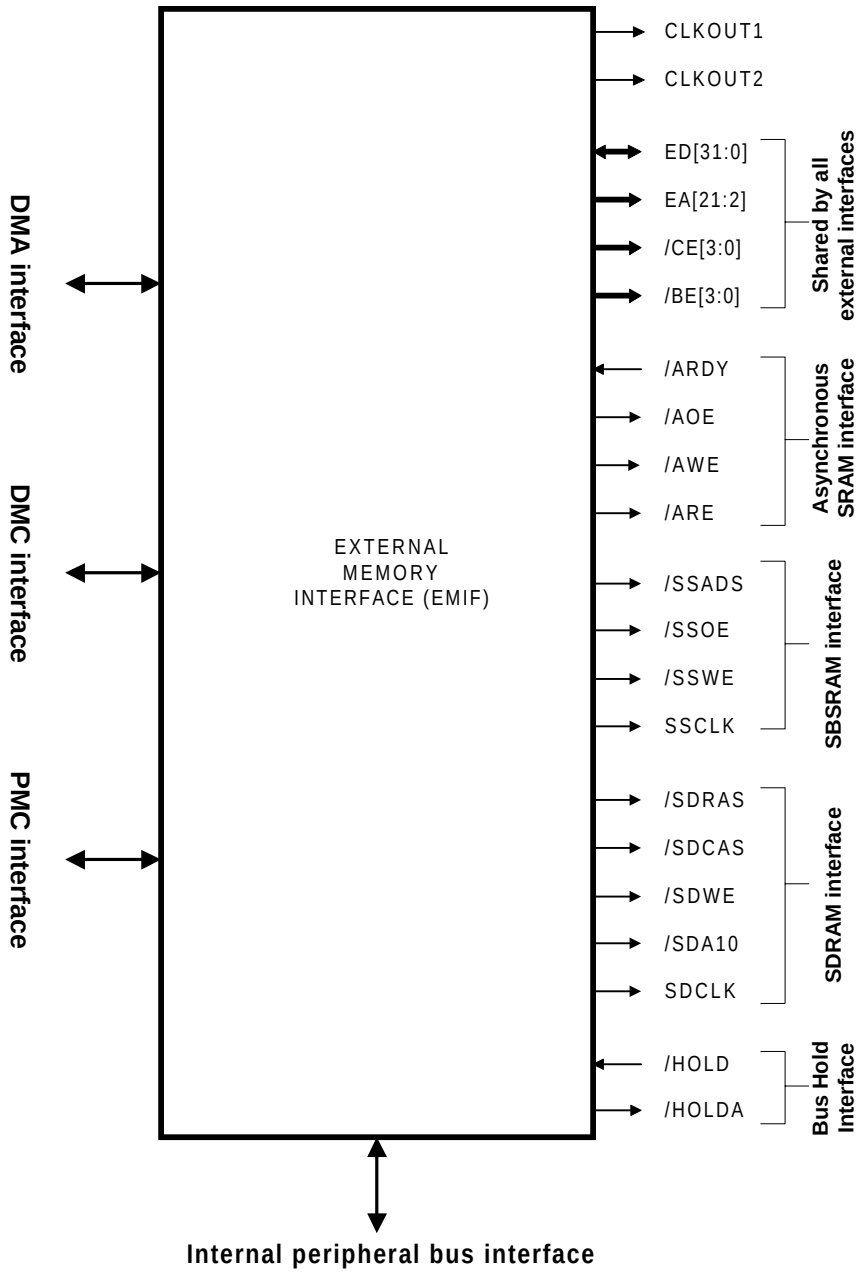


Table 1. Signals Used in FIFO Interface : Shared Signals and Asynchronous Signals

Pin	(I/O/Z)	Description
CLKOUT1	O	Clock. Clock output - the CPU clock rate.
ED(31:0)	I/O/Z	Data I/O. 32-bit data input/output from external memories and peripherals.
/CE0	O/Z	External /CE0 Chip Select. Active low chip select for CE space 0.
/CE1	O/Z	External /CE1 Chip Select. Active low chip select for CE space 1.
/CE2	O/Z	External /CE2 Chip Select. Active low chip select for CE space 2.
/CE3	O/Z	External /CE3 Chip Select. Active low chip select for CE space 3.
ARDY	I	Ready. Asynchronous ready input used to insert wait states for slow memories and peripherals.
/AOE	O/Z	Output Enable. Active low output enable for asynchronous memory interface.
/AWE	O/Z	Write Strobe. Active low write strobe for asynchronous memory interface.
/ARE	O/Z	Read Strobe. Active low read strobe for asynchronous memory interface.

EMIF Registers

Control of the EMIF and the memory interfaces it supports is maintained through a set of memory mapped registers within the EMIF. A write to any EMIF register will not complete until all pending EMIF accesses which use that register have completed. The memory mapped registers are shown in Table 2.

Table 2. EMIF Memory Mapped Registers

Byte Address	Name
0x01800000	EMIF Global Control
0x01800004	EMIF CE1 Space Control
0x01800008	EMIF CE0 Space Control
0x0180000C	reserved
0x01800010	EMIF CE2 Space Control
0x01800014	EMIF CE3 Space Control
0x01800018	EMIF SDRAM Control
0x0180001C	EMIF SDRAM Refresh Period

CE Space Control Registers

The four CE Space Control Registers (Figure 2) correspond to the four CE spaces supported by the EMIF. The MTYPE field identifies the memory type for the corresponding CE space. If MTYPE selects SDRAM or SBSRAM, the remaining fields in the register do not apply. If an asynchronous type is selected (ROM or Asynchronous), the remaining fields specify the shaping of the address and control signals for access to that space. Table 3 contains a more detailed description of the asynchronous configuration fields, which will be used in the FIFO interface. Modification of a CE Space Control Register does not occur until that CE space is inactive.

Figure 2. EMIF CE(0/1/2/3) Space Control Register Diagram

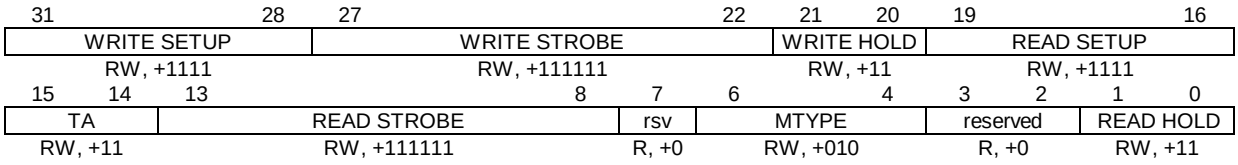


Table 3. EMIF CE(0/1/2/3) Space Control Registers Bitfield Description

Field	Description
READ SETUP WRITE SETUP	Setup width. Number of CLKOUT1 cycles from the beginning of the memory access (/CE high to low for first access in sequence) until /ARE or /AWE goes low for the beginning of the Strobe cycles. Range : 1 to 15 cycles
READ STROBE WRITE STROBE	Strobe width. The width of read strobe (/ARE) and write strobe (/AWE) in CLKOUT1 cycles. Range : 1 to 63 cycles
READ HOLD WRITE HOLD	Hold width. Number of CLKOUT1 cycles from end of Strobe cycles until the end of the current memory access. Range : 0 to 3 cycles
MTYPE	Memory Type. MTYPE=000b, 8-bit wide ROM MTYPE=001b, 16-bit wide ROM MTYPE=010b, 32-bit wide Asynchronous Interface MTYPE=011b, 32-bit wide SDRAM MTYPE=100b, 32-bit wide SBSRAM MTYPE=other, reserved

FIFO Interface

The asynchronous interface, which will be used with FIFO memories, offers users configurable memory cycle types, used to interface to a variety of memory and peripheral types; including SRAM, EPROM, FLASH, as well as FPGA and ASIC designs. This section, however, will focus on the interface between the EMIF and FIFO Memory.

In most situations when interfacing the C62x with an external FIFO, the FIFO will be used in one direction only. That is, the C62x will either write to the FIFO, expecting some other device, which could be another C62x, to read from the FIFO. Or the C62x will read from the FIFO, expecting some other device to write to the FIFO. Therefore for all of the examples given below, the diagrams will be illustrated separately for the read interface and for the write interface to a given FIFO.

There are four basic types of FIFO memory, which will be summarized in the following sections.[2] The timing notations used in all of the examples are summarized in Table 4 and Table 5. In the following examples, all of the signals going to the FIFOs are being used in conjunction with the /CE signal. This is done to prevent any undesired behavior which would occur if some other CE space also used asynchronous memory, and thus also used the asynchronous interface pins. By ORing the asynchronous signals from the EMIF with the CE signal corresponding to the CE space where the FIFO resides, the FIFO will only be accessed at the desired times.

As Table 3 describes, the Setup, Strobe, and Hold fields for both Read and Write cycles are fully programmable via the EMIF CE Space Control Registers. These fields must be set appropriately to ensure proper operation with the FIFOs in the examples in the following sections. In all of the timing diagrams illustrated, the Setup/Strobe/Hold timing is 1/2/1 cycles. However, this will not be the case depending on the speed of the FIFO or asynchronous memory being used. The general constraints used to set these parameters will be explained in the following sections.

[2] These summaries are not complete and are only intended to point out the major differences between FIFO types. For complete details, see an appropriate data sheet.

Table 4. EMIF Input Timing Requirement Definitions

Timing Parameter	Definition
t_{su}	Data Setup time required by the EMIF for reads, read D before CLKOUT1 high

Table 5. ASRAM Input Timing Requirement Definitions

Timing Parameter	Definition
t_{acc}	Access Time, time from active edge until output data from the FIFO is valid
t_{rp}	Minimum Required Read Pulse Width
t_{wp}	Minimum Required Write Pulse Width
t_{su}	Data Setup time required by the FIFO for writes, write D before /W High
t_{oe}	Output enable time, /OE low to output valid
t_{ens}	Enable setup time, time required from /OE, /REN, /WEN low to UNC high
t_{rc}	Length of the read cycle
t_{wc}	Length of the write cycle

Common Features

All FIFOs have features to let the user know what state it is in. Although the number and complexity of these features range from device to device and manufacturer to manufacturer, there are several that are common to most of them. These include the Empty Flag (/EF), which is set when no valid data remains, the Full Flag (/FF), which indicates that the FIFO is full, and the Half Full flag (/HF), which indicates that half +1 of the memory locations are in use.[3]

Also, many FIFOs have the capability of being operated in depth expansion mode, which effectively increases the number of words of the device by using multiple devices serially. Width expansion allows the word width to be expanded by using devices in parallel.

[3] Some devices use a different flag scheme. A common scheme uses Input Ready Flag (IR), Output Ready Flag (OR) and Half Full Flag (HF). In addition, it is quite common, but not universal, to have a programmable Almost Full and Almost Empty Flag.

Asynchronous FIFO

For Asynchronous FIFOs, data reads and writes are not edge triggered. Instead, data writes are initiated by a low level on write enable (/W) when the full flag is not asserted. The data is actually written on the rising edge. Data reads are initiated by low level on read enable (/R) when the empty flag is not asserted. For this type of FIFO, it is actually the /R signal which takes the output data bus (Q[x:0]) out of high impedance state immediately before the data becomes valid, as shown in Figure 4. Figure 3 and Figure 5 show the interface between the EMIF and two 18 bit wide Asynchronous FIFOs. The EMIF will directly interface to the lower 16 bits of each FIFO, logically combining them to appear as a single 32 bit wide FIFO. This is referred to as width expansion, and is covered in detail in most FIFO data sheets. The additional two bits can be used for parity if desired.

The External Logic Block shown in Figure 3 and Figure 5 is required to glue the EMIF to the FIFO. Of primary concern in this example is that the /R and /W signal on the FIFO is only activated when this memory space is activated (by the /CE signal). This can be done by ORing the appropriate strobe signal with the /CE signal :

- /R = /CE + /ARE
- /W = /CE + /AWE

Figure 4 shows the timing diagram illustrating both the outputs from the EMIF and the inputs to the Asynchronous FIFO for a read cycle. Figure 6 shows the write cycle. Although the state flags (/EF,/HF, /FF) are not shown, there should be an interrupt routine set up to prevent reading from an empty FIFO or writing to a full FIFO.

Figure 3. Asynchronous FIFO Interface for Read Transmission

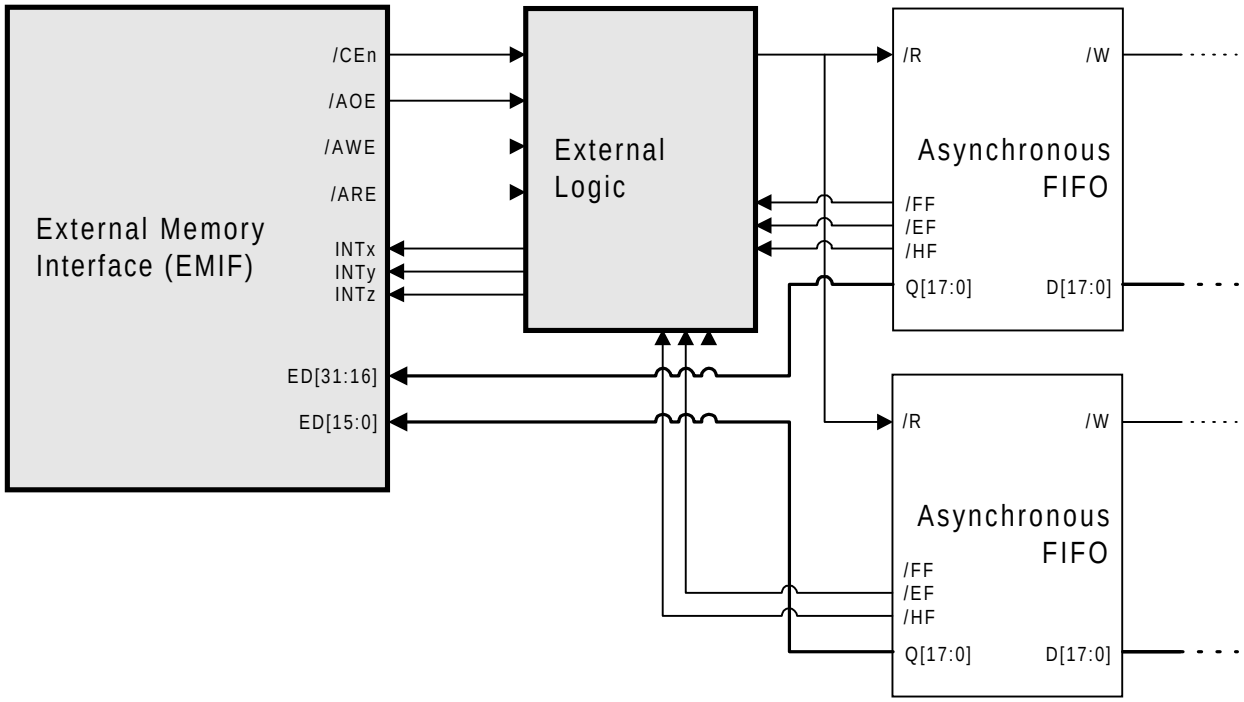
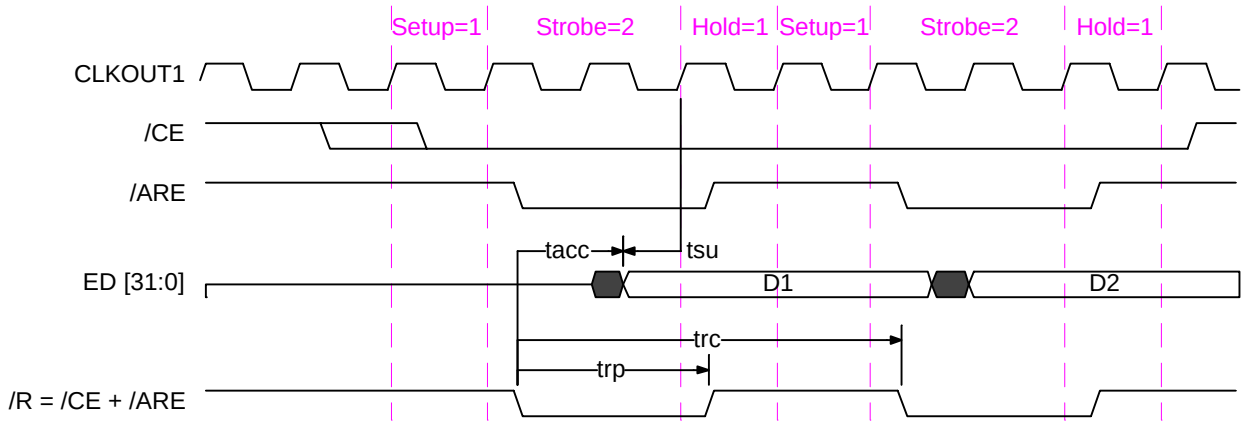


Figure 4. Asynchronous FIFO Read



Timing Constraints for Read Interface

- Setup ≥ 1 (minimum allowed by C62x)
- Strobe ≥ $t_{acc} + t_{su}$
- Strobe ≥ t_{rp}
- Setup + Strobe + Hold ≥ t_{rc}

Figure 5. Asynchronous FIFO Interface for Write Transmission

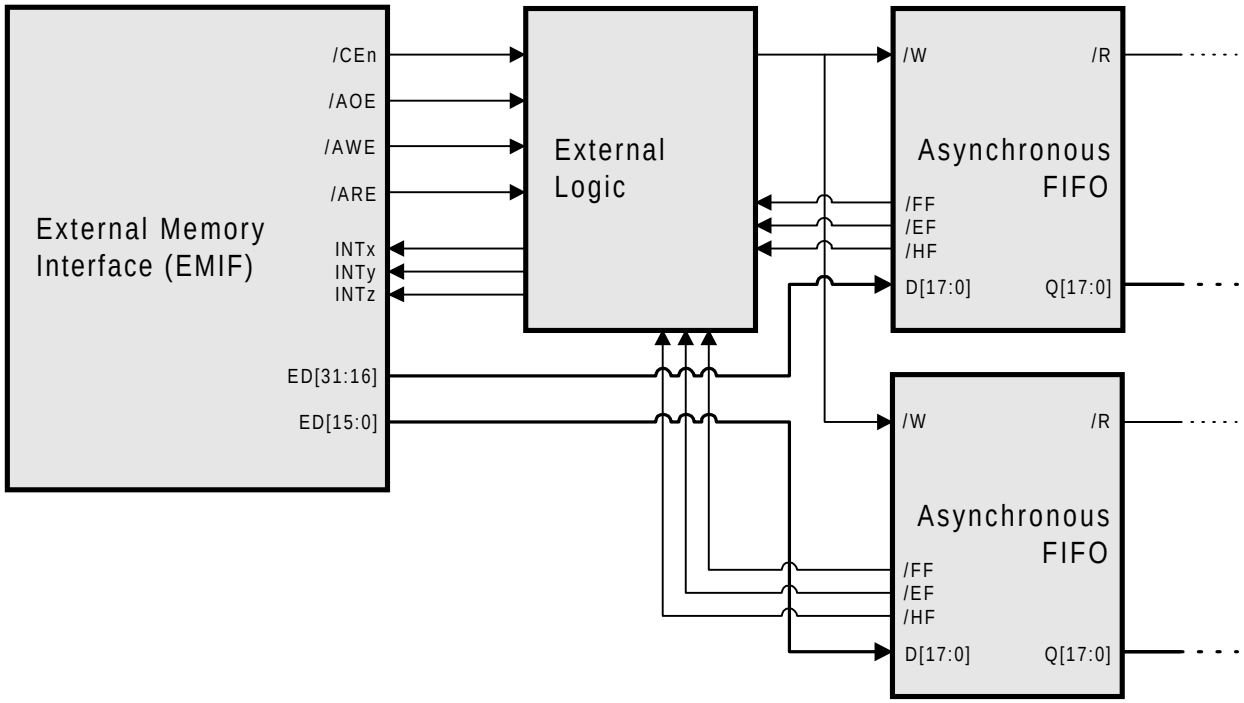
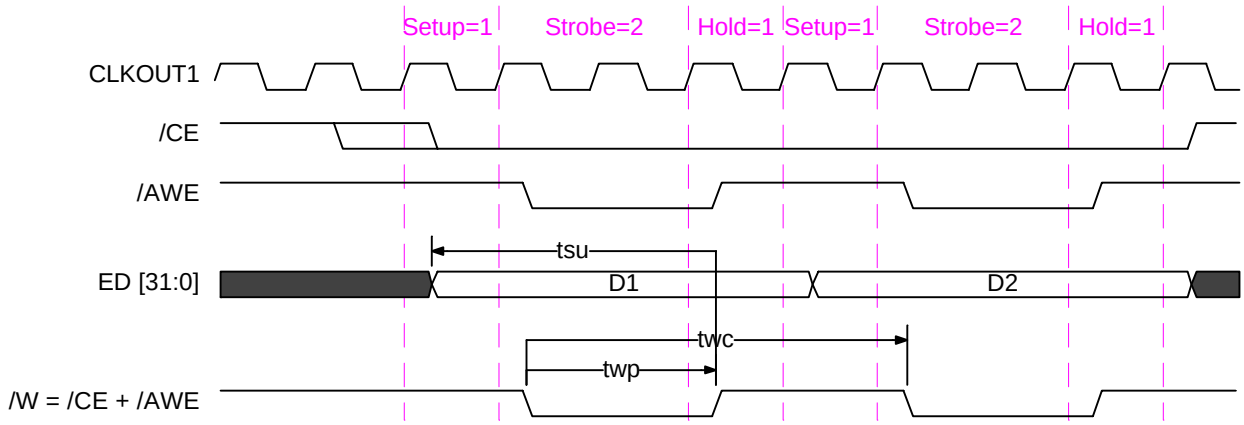


Figure 6. Asynchronous FIFO Write



Timing Constraints for Write Interface

- Setup ≥1
- Strobe ≥twp
- Setup + Strobe ≥ tsu
- Setup + Strobe + Hold ≥ twc

Strobed FIFO

The strobed FIFO is very similar to the Asynchronous FIFO. The addition of an output enable signal (/OE) signal, which is responsible for tri-stating the output data bus, allows the FIFO to use the read enable signal (UNCK) as an edge trigger. The write cycle is identical to the Asynchronous FIFO write cycle.

Figure 7 and Figure 9 show the interface between the EMIF and two 18 bit wide Strobed FIFOs. The EMIF will directly interface to the lower 16 bits of each FIFO, logically combining them to appear as a single 32 bit wide FIFO. This is referred to as width expansion, and is covered in detail in most FIFO data sheets. The additional two bits can be used for parity if desired.

The External Logic Block shown in Figure 7 and Figure 9 is required to glue the EMIF to the FIFO. The UNCK, LDCK, and /OE signals can be created by logically ORing the Asynchronous control signals from the EMIF as follows:

- UNCK = /CE + /ARE
- LDCK = /CE + /AWE
- /OE = /CE + /AOE

Figure 7 shows the timing diagram illustrating both the outputs from the EMIF and the inputs to the Strobed FIFO for a read cycle. The write cycle is not shown since it is identical to the cycle shown above for Asynchronous FIFO. These timing diagrams illustrate the creation of the FIFO signals with the above logic. Although the state flags (/EF,/HF, /FF) are not shown, there should be an interrupt routine set up to prevent reading from an empty FIFO or writing to a full FIFO.

Figure 7. Strobed FIFO Interface for Read Transmission

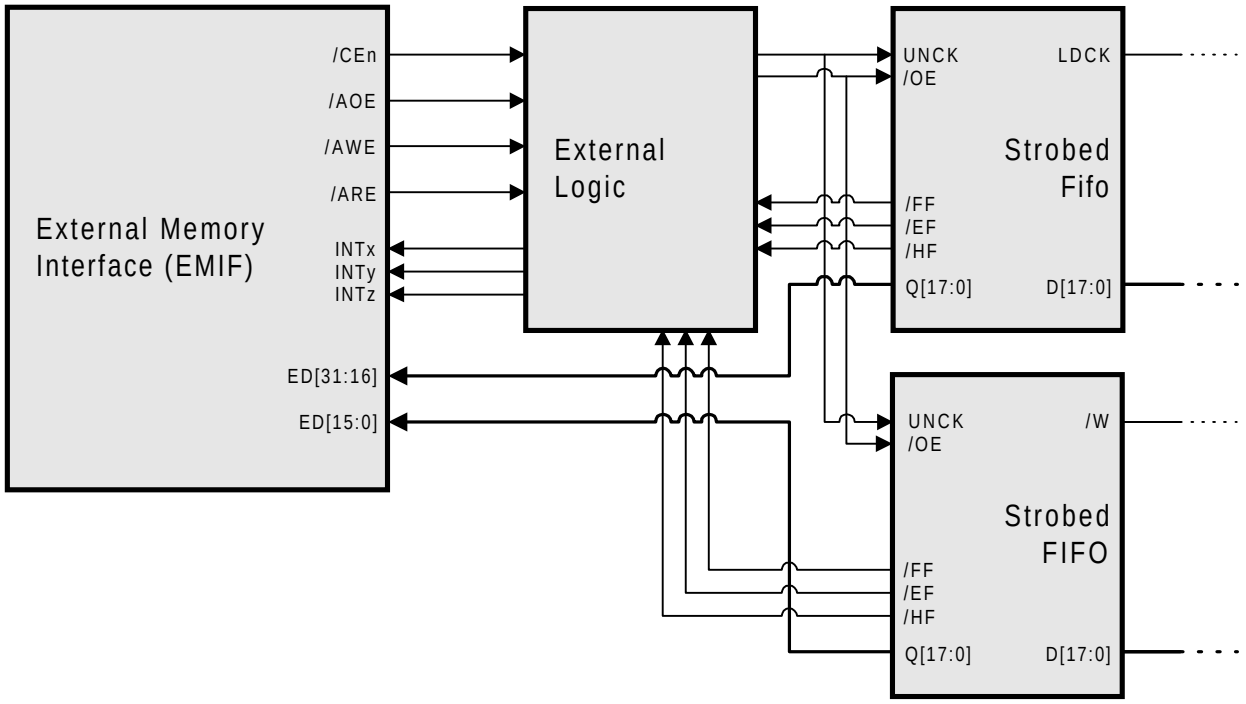
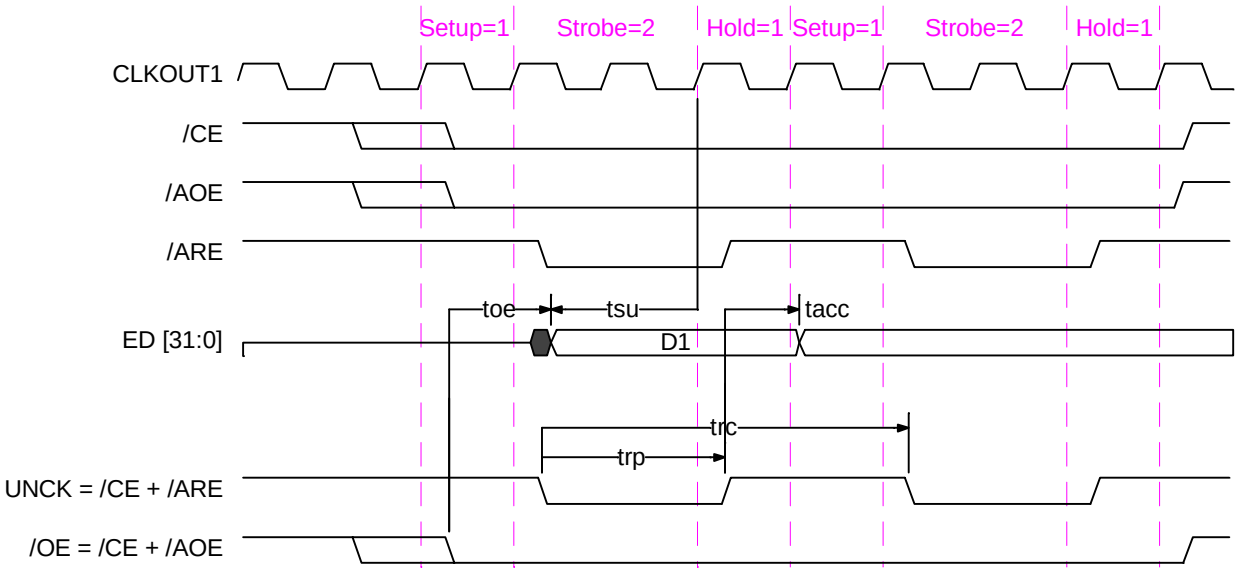


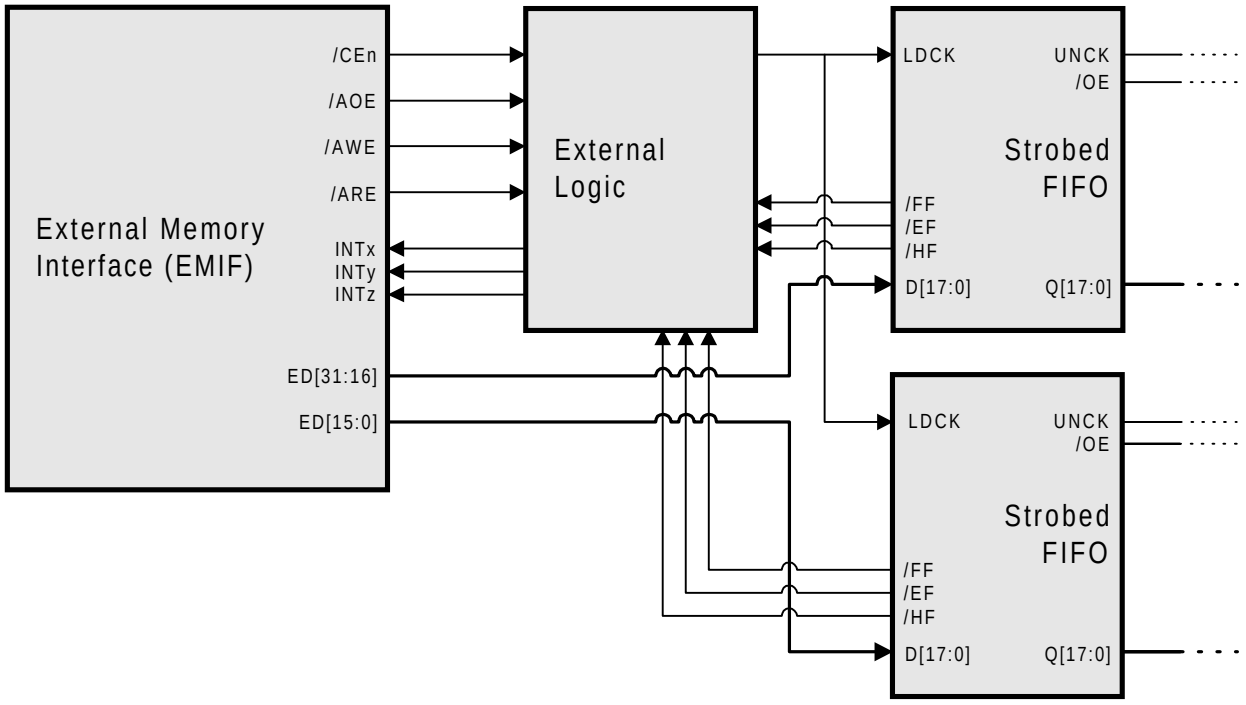
Figure 8. Strobed FIFO Read



Timing Constraints for Read Interface

- Setup ≥ 1
- Setup + Strobe ≥ toe + tsu
- Setup + Strobe ≥ tens
- Strobe ≥ trp
- Setup + Strobe + Hold ≥ trc

Figure 9. Strobed FIFO Interface for Write Transmission



Timing Constraints for Write Interface

Same as for asynchronous.

Synchronous FIFO

The synchronous FIFO employs both a read clock (RCLK) and a write clock (WCLK) along with read enable (/REN), write enable (/WEN), and output enable (/OE) signals. Data is written on a rising edge of the WCLK if the /WEN pin is asserted. The read operation is started on a rising edge of the RCLK if the /REN and /OE pins are asserted.

There are two types of synchronous FIFOs which often go by different names. The biggest difference between the two types is what occurs on the first write cycle.

Standard Timing

Standard Timing FIFOs are often referred to simply as Synchronous FIFOs.

With Standard Timing, the first data written to the FIFO after reset remains in a memory cell and the output buffer is empty. Then, for the first read access, the read is started when /REN is active at the rising edge of RCLK, and thus brings the data to the output buffer a time t_{acc} after RCLK goes high. This therefore invalidates the first read, since the EMIF is latching in the data at the end of the STROBE period, which corresponds to the point at which the RCLK goes high. This is illustrated in Figure 11.

Then for the second read, this data is in the output buffer and is output to the EMIF when the /OE signal goes low, and is then read at the rising edge of RCLK by the EMIF, which is valid. In addition, the rising RCLK with an active /REN causes the next data to be read into the output buffer, thus preparing the FIFO for the next read cycle. This is illustrated in Figure 12.

Therefore, it is important that for a standard synchronous FIFO, a dummy read be executed before actual data is able to be read.

First Word Fall Through (FWFT) Timing

First Word Fall Through FIFOs are often referred to as Clocked FIFOs, but some manufacturers use Clocked and Synchronous synonymously.

FWFT is very similar to the standard timing FIFO. The major difference is in what occurs at the first write cycle after reset. When the first write is performed, the data is automatically fed through to the output buffer, instead of residing in a memory cell. Thus, when a read is performed, the /OE signal actually causes the data to appear on the bus, and the /REN signal pulls the next valid memory location to the output buffer, so that it is ready for the next read. Thus for FWFT, the first read is valid, and is identical to Figure 12.

Figure 10 and

Figure 13 show the interface between the EMIF and two 18 bit wide synchronous FIFOs. The EMIF will directly interface to the lower 16 bits of each FIFO, logically combining them to appear as a single 32 bit wide FIFO. This is referred to as width expansion, and is covered in detail in most FIFO data sheets. The additional two bits can be used for parity if desired.

External Logic

The External Logic Block shown in Figure 10 and

Figure 13 is required to glue the EMIF to the FIFO. The RCLK, WCLK, /REN, /WEN, and /OE signals are created by logically ORing the Asynchronous control signals from the EMIF as follows:

- RCLK = /CE + /ARE
- WCLK = /CE + /AWE
- /REN = /CE + /AOE
- /WEN = /CE + /AWE
- /OE = /CE + /AOE

Figure 11 and Figure 12 show the timing diagram illustrating both the outputs from the EMIF and the inputs to the synchronous FIFO for a read cycle. The write cycle is shown in

Figure 13. These timing diagrams illustrate the creation of the FIFO signals with the above logic. Although the state flags (/EF,/HF, /FF) are not shown, there should be an interrupt routine set up to prevent reading from an empty FIFO or writing to a full FIFO.

Figure 10. Synchronous FIFO Interface for Read Transmission

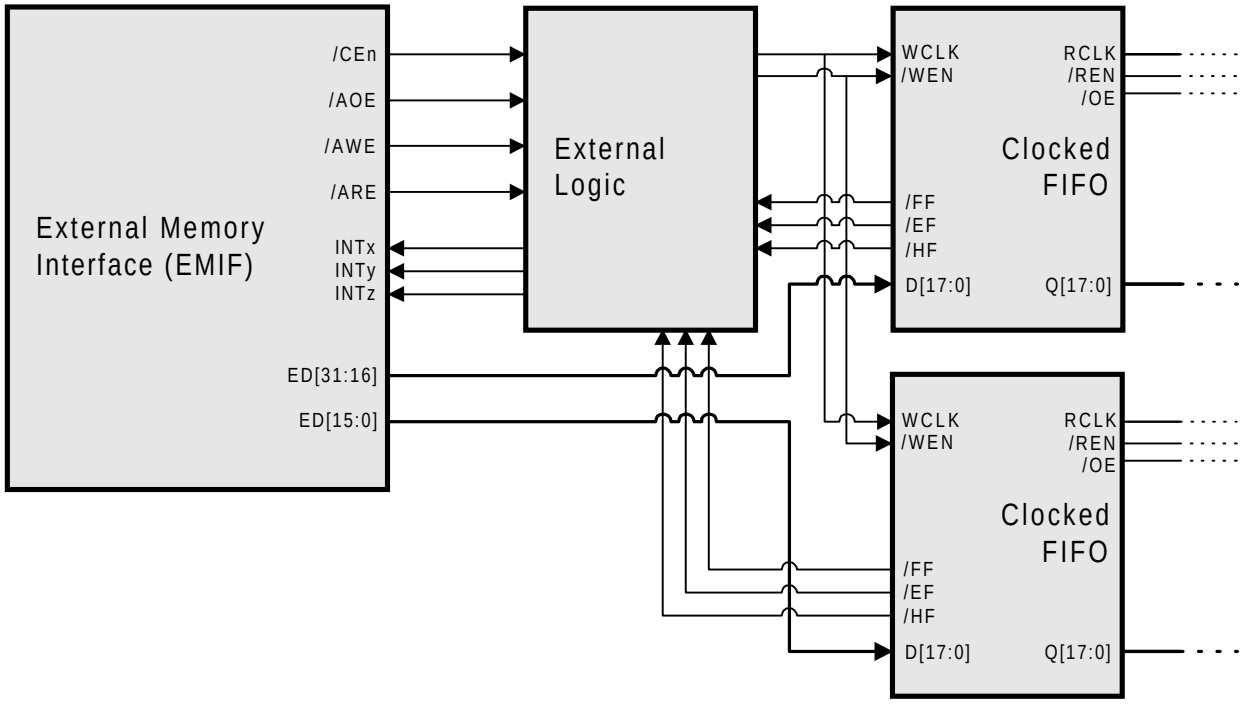


Figure 11. Synchronous FIFO Read Timing - First Read w/ Standard Timing

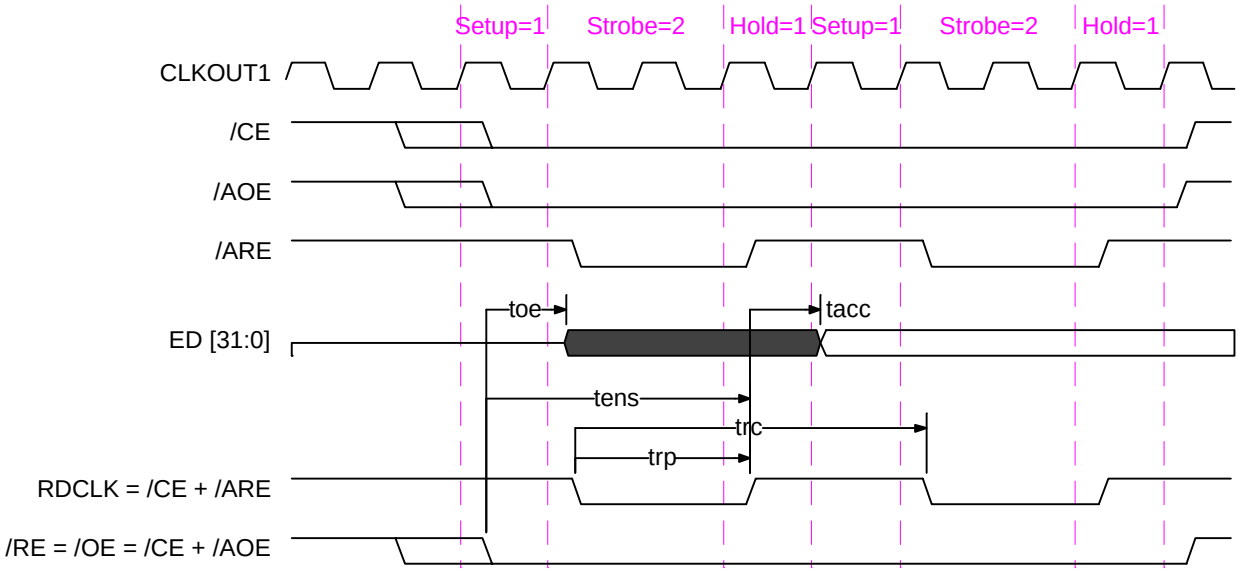
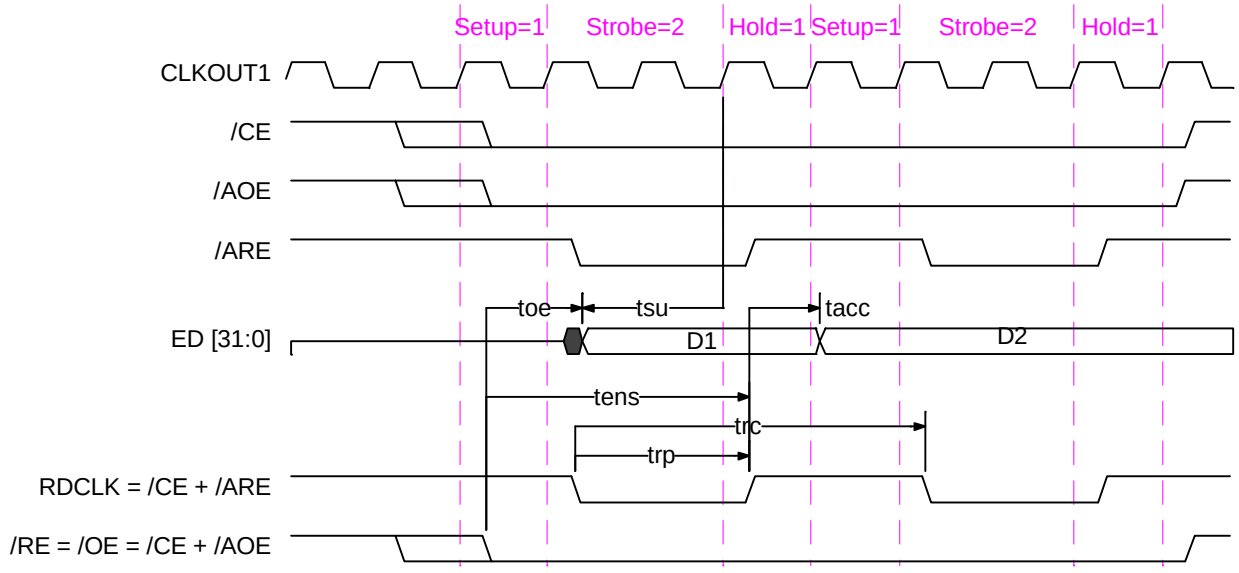


Figure 12. Synchronous FIFO Read Timing-After First Read w/Standard Timing - Any Read w/ FWFT



Timing Constraints for Read Interface

- Setup ≥ 1
- Setup +Strobe ≥ toe + tsu
- Setup + Strobe ≥ tens
- Strobe ≥ trp
- Setup + Strobe + Hold ≥ trc

Figure 13. Synchronous FIFO Interface for Write Transmission

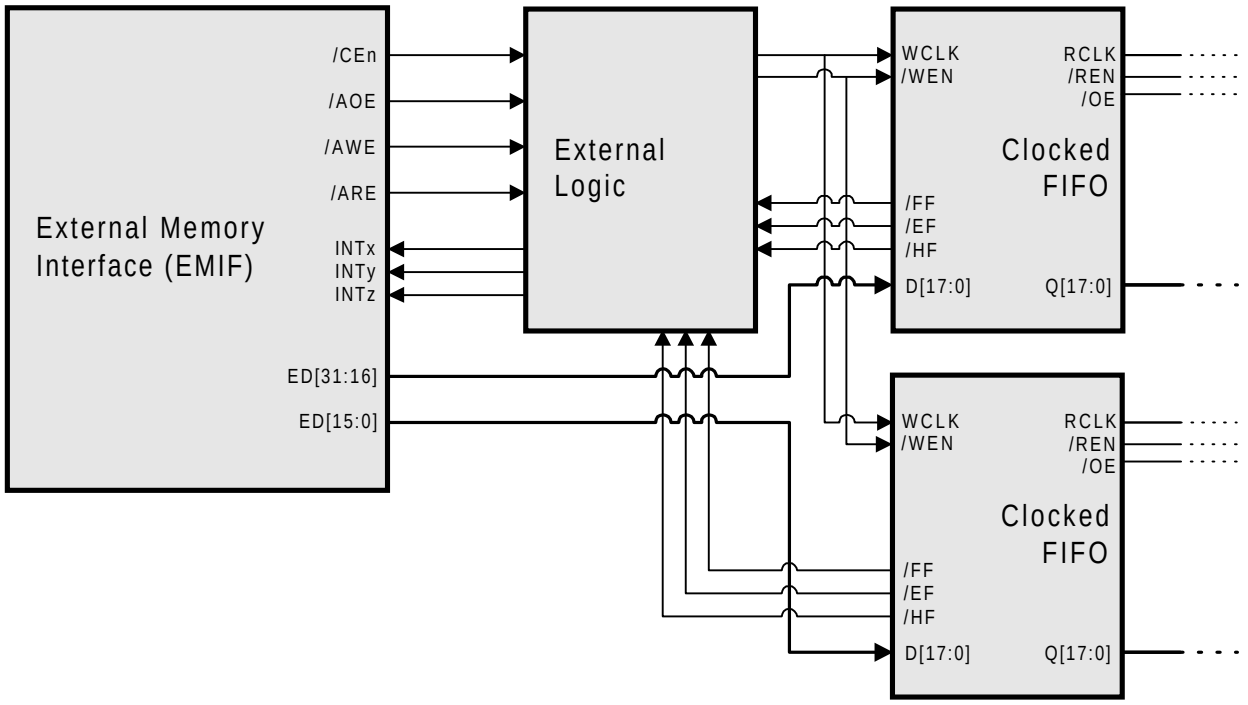
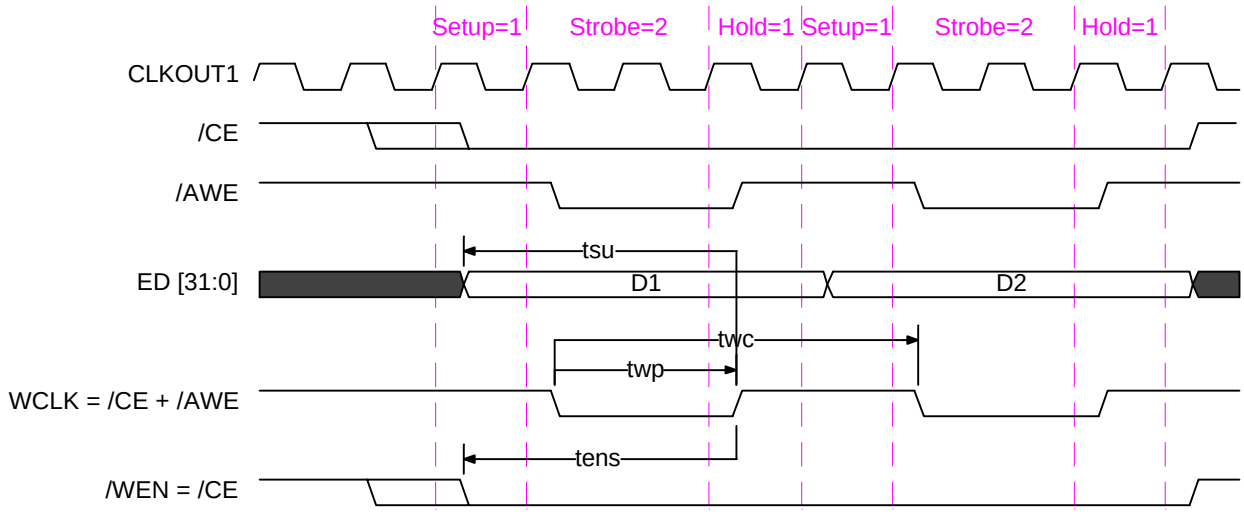


Figure 14. Synchronous FIFO Write Timing



Timing Constraints for Write Interface

- Setup ≥ 1
- Setup + Strobe ≥ tsu
- Setup + Strobe ≥ tens
- Strobe ≥ twp
- Setup + Strobe + Hold ≥ twc

Special Considerations

The following list contains peculiarities associated with certain FIFOs. This list is far from complete, but is included to assist the user from making avoidable design errors. Therefore, the user should be sure that the chosen FIFO for a given design meets the timing requirements of the C62x and that both the C62x's operation and the FIFO's operation is fully understood.

- Some Synchronous FIFO's have special reset requirements which require a given number of RCLK and WCLK cycles to occur while the reset signal is active low. This is a problem with the interface discussed since the solution provided uses the /ARE and /AWE to create a clock, and thus does not have a free running clock

provided to the FIFO.

- Synchronous FIFO's often have flags which are synchronized to only one of the clocks. For example, the /EF is only updated on a rising edge of /RCLK. Thus, with the solution provided above, dummy reads would need to be executed to cause the transition of the /EF, in order for the FIFO to allow a real read to occur.

- Above all, do not assume that a FIFO will behave exactly as this document describes, due to the many variations which are in existence.

Full Example

This section will walk through the configuration steps required to implement TI's SN74ALVC7806 Strobed FIFO, which is a 256 x 18 device with an access time of 18 ns and a maximum frequency of 40 MHz.

The following assumptions will be made :

- The FIFO will be used in address space CE0.
- CLKOUT1 = 200 MHz, therefore t_{period} is 5 ns.
- The FIFO will be used as a block buffer for transferring 128 words between two points.

Read Interface

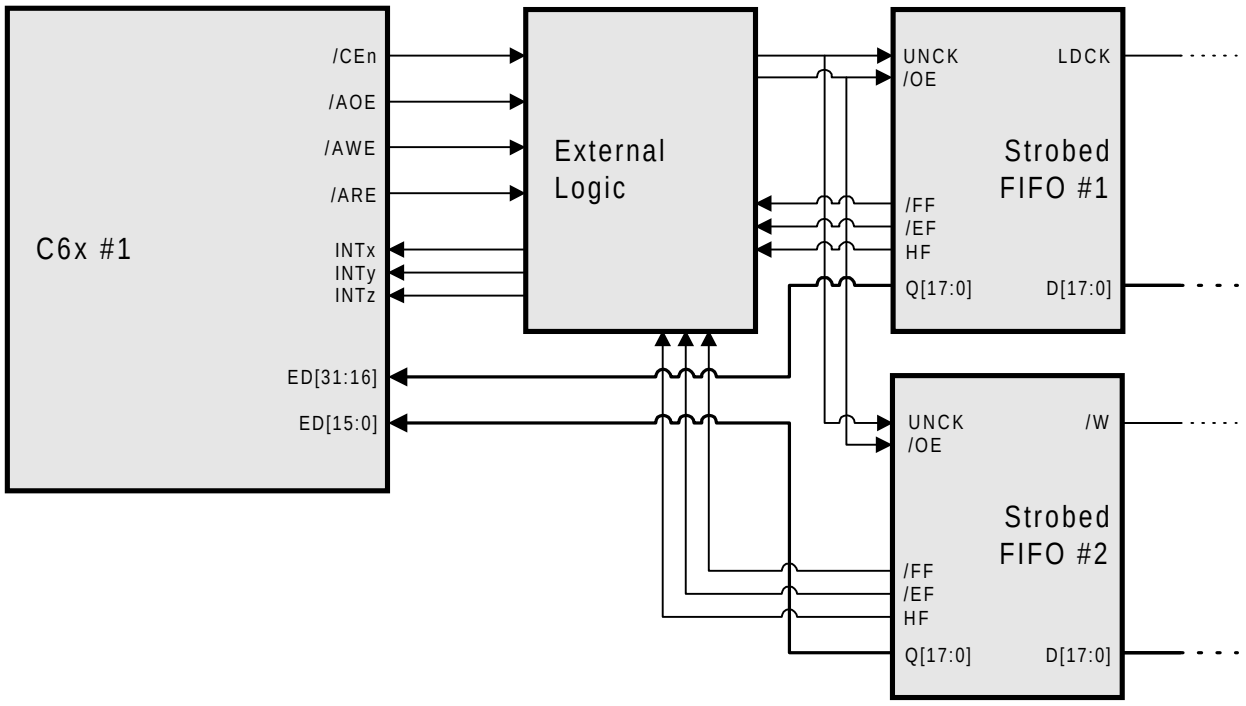
Figure 15 shows the interface between the EMIF and TI's SN74ALVC7806. The only difference between this diagram and the generic diagram for strobed FIFOs is that TI's device uses an active high HF flag.

Since in this example we wish to transfer 128 words, we wish to have the FIFO signal the CPU when this has occurred via an interrupt. Since interrupts for the C62x are edge triggered, we will need to also have the FIFO signal when it is less than half full by using the inverse of the signal. The logic for this example is as follows:

- UNCK = /CE + /ARE
- /OE = /CE + /AOE
- INTx = HF1
- INTy = !HF1

Thus, INTx will be set on a low to high transition of HF1, which implies that it will be set when the buffer becomes half full. INTy will be set on a high to low transition of HF1, which implies that it will be set when the buffer is less than half full.

Figure 15. Read Interface for SN74ALVC7806



Register Configuration

Table 6 and Table 7 summarize the timing characteristics of the C62x and the '7806 FIFO, which will be used to calculate the values for the CE0 Space Configuration Register. This data was taken from the C62x Data Sheet and the 7806 Data Sheet.

Table 6. C62x EMIF Input Requirements from FIFO

NO			MIN	MAX	UNIT
1	t_{su}	Setup time, read D before CLKOUT1 high	5		ns

Table 7. ASRAM Input Requirements from C62x EMIF

NO			MIN	MAX	UNIT
	t_{acc}	Access Time, time from active edge of UNCK until next data is in the output buffer.		22	
	t_{rp}	Minimum Required Read Pulse Width	8		
3	t_{oe}	Output enable time, /OE low to output valid		10	ns
5	t_{rc}	Length of the read cycle	25		ns

† Values specified by design and not tested

Read Calculations

- Setup ≥ 1

  SETUP = 1 cycle

- Setup + Strobe ≥ toe + tsu

  Therefore,

  STROBE ≥ (toe + tsu)/tperiod - SETUP = (10ns + 5ns)/5ns - 1 cycle

  ≥ 2 cycles

  STROBE = 2 cycles

- Strobe ≥ trp

  STROBE ≥ 8 ns / 5 ns = 1.6 cycles, which is satisfied with previously calculated value of 2 cycles.

- Setup + Strobe + Hold ≥ trc

  Therefore,

  HOLD ≥ trc/tperiod - SETUP - STROBE = 25ns/5ns - 2 cycles - 1 cycle

  ≥ 2 cycles

  HOLD = 2 cycles

Using the above calculations, the CE Space Control Register can now be properly configured. Figure 16 shows the CE0 Space Control Register with the properly assigned values for each field. MTYPE = 010 identifies the memory in this address space as 32 bit wide asynchronous memory, while the other fields are used as calculated above. Notice, that since this example is for a read interface, the write parameters are all don't cares.

Figure 16. EMIF CE0 Space Control Register Diagram for '7806

31–28	27–22	21–20	19–16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
Xxxx	xxxxxx	xx	0001
RW, +1111	RW, +111111	RW, +11	RW, +1111

15	14	13–8	7	6–4	3–2	1–0
TA		READ STROBE	rsv	MTYPE	reserved	READ HOLD
xx		000010	rsv	010	reserved	10
RW, +11		RW, +111111	R, +0	RW, +010	R, +0	RW, +11

Write Interface

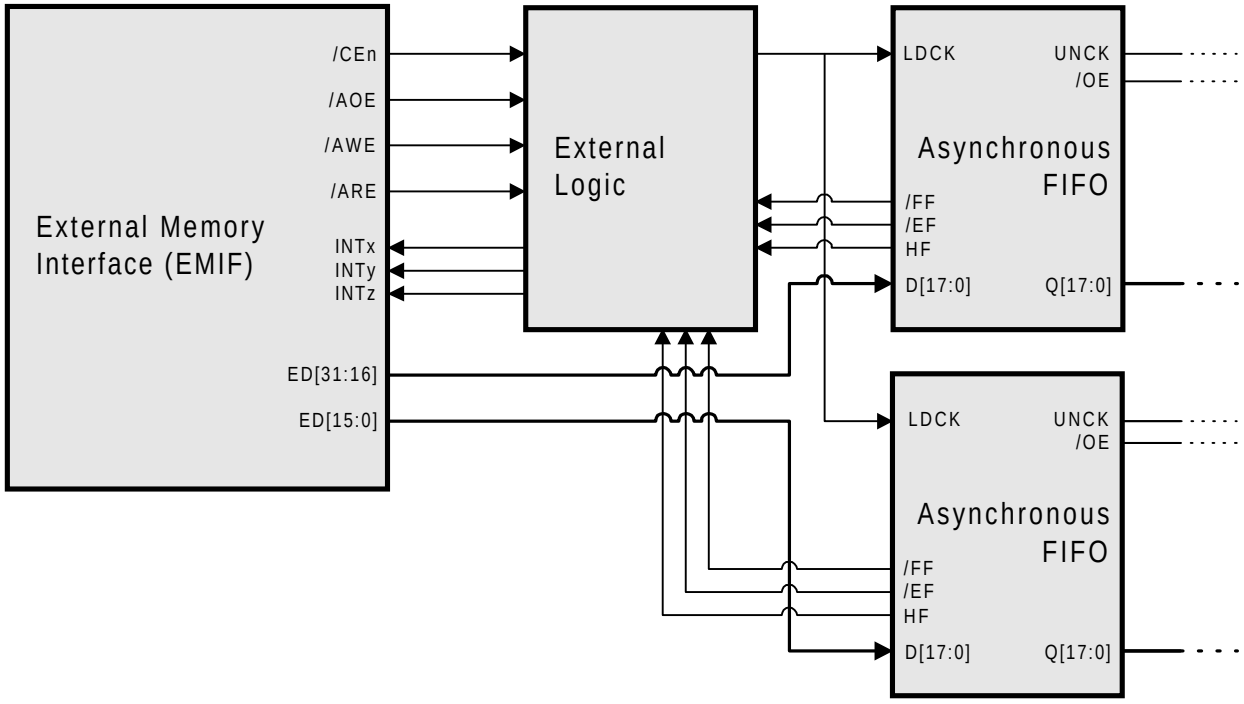
Figure 15 shows the interface between the EMIF and TI's SN74ALVC7806. The only difference between this diagram and the generic diagram for strobed FIFOs is that TI's device uses an active high HF flag.

Since in this example we wish to transfer 128 words, we wish to have the FIFO signal the CPU when this has occurred via an interrupt. Since interrupts for the C62x are edge triggered, we will need to also have the FIFO signal when it is less than half full by using the inverse of the signal. The logic for this example is as follows:

- UNCK = /CE + /ARE
- /OE = /CE + /AOE
- INTx = HF1
- INTy = !HF1

Thus, INTx will be set on a low to high transition of HF1, which implies that it will be set when the buffer becomes half full. INTy will be set on a high to low transition of HF1, which implies that it will be set when the buffer is less than half full.

Figure 17. Write Interface for SN74ALVC7806



Register Configuration

Table 8 summarizes the timing characteristics of the '7806 FIFO for write cycles, which will be used to calculate the values for the CE0 Space Configuration Register. This data was taken from the 7806 Data Sheet.

Table 8. ASRAM Input Requirements from C62x EMIF

		MIN	MAX	UNIT
t_{su}	Setup time, time from Data valid until rising edge of LDCK.	5		ns
t_{wp}	Minimum Required Write Pulse Width	8		ns
t_{rc}	Length of the read cycle	25		ns

Write Calculations

- Setup ≥1

  SETUP = 1 cycle

- Strobe ≥ twp

  STROBE ≥ twp/tperiod = 8ns/5ns = 1.6

  ≥ 1.6 cycles

  STROBE = 2 cycles

- Setup + Strobe ≥ tsu

  SETUP + STROBE ≥ tsu/tperiod = 5 ns / 5ns = 1 cycle, therefore this constraint is satisfied.

- Setup + Strobe + Hold ≥ twc

  Therefore,

  HOLD ≥ twc/tperiod - SETUP - STROBE = 25ns/5ns - 2 cycles - 1cycle

  ≥ 2 cycles

  HOLD = 2 cycles

Using the above calculations, the CE Space Control Register can now be properly configured. Figure 18 shows the CE0 Space Control Register with the properly assigned values for each field. MTYPE = 010 identifies the memory in this address space as 32 bit wide asynchronous memory, while the other fields are used as calculated above. Notice, that since this example is for a write interface, the read parameters are all don't cares.

Figure 18. EMIF CE0 Space Control Register Diagram for '7806

31–28	27–22	21–20	19–16
WRITE SETUP	WRITE STROBE	WRITE HOLD	READ SETUP
0001	000010	10	xxxx
RW, +1111	RW, +111111	RW, +11	RW, +1111

15	14	13–8	7	6–4	3–2	1–0
TA		READ STROBE	rsv	MTYPE	reserved	READ HOLD
xx		xxxxxx	rsv	010	reserved	xx
RW, +11		RW, +111111	R, +0	RW, +010	R, +0	RW, +11

References

"TMS320C6201 Data Sheet, Revision 2," Texas Instruments, October 1997.

"TMS320C62xx Peripherals Reference Guide," Texas Instruments, October 1997.

"SN74ALVC7806 Data Sheet," Texas Instruments, October 1997.