EDI's x32 MCM-L SRAM Family: Integrated Memory Solution for TMS320C3x DSPs

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Abstract

Memory modules have long been a system designer’s trump card. Modules, in addition to the traditional space savings, allow ease of implementation, known operating performance, flexible density options, and the ability to move across technology boundaries (i.e. CMOS to BiCMOS) without changing their system board design. As technology innovations continue, both at the chip and assembly levels, modules are no longer saddled by performance penalties associated with system board interfaces. Today’s modules achieve equivalent or, in some cases, improved performance over traditional monolithic approaches. This performance improvement is linked to reductions in capacitance and inductance as well as improved power planes and signal line impedance versus a monolithic solution. This application report will show how these benefits can be taken advantage of in a system design using Texas Instrument’s TMS320C3x DSPs.

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Introduction

How often during a design cycle do your system requirements change? Have you ever been at the end of your design cycle and had the memory requirements increased two to four times the density the initial design required? As competition and cost pressures increase, the need for multi-function and multi-application designs has become a requirement as opposed to a benefit. In many cases, changing the density, access time, or technology of the memory array provides the required flexibility for multi-application designs. For example, a DSP board design with a high density BiCMOS memory array will meet the high-end performance market, while changing the memory to lower density CMOS or Flash array will allow the design to meet the requirements of the cost sensitive consumer market. Designing in this type of flexibility can lead to complex board designs and excessive board costs. What if all these options came in a single package with a compatible footprint? How many problems would it solve?

EDI has developed a family of x32 SRAM and Flash products that are packaged in a JEDEC standard 68 pin PLCC. The SRAM products are available in densities from 64Kx32 through 512Kx32 in both BiCMOS and CMOS technologies. The Flash products are available in densities from 128Kx32 through 512Kx32.

This application report will describe the SRAM products, detail proper interfacing to the TI TMS320C3x family of DSPs, and provide the technical information required to take full advantage of these benefits. The 5V only Flash products, though not described in this report, are pin for pin compatible and provide additional options for cost sensitive applications.

x32 MCM-L Family Architecture

EDI's x32 MCM-L family is a series of high performance SRAM arrays packaged in a JEDEC standard 68 pin PLCC. The x32 MCM-L family of devices currently range in density from 64Kx32 to 512Kx32.

The basic components of the architecture include: a single address bus, a single databus, a single write enable pin, a single output enable pin, and four enable pins. The enable pins control individual bytes (8 bits) of the 32 bit databus.

The differences within the family lie in the address bus, which requires additional address lines for increased density and the addition of two enable pins for the 64Kx32 and the 256Kx32 densities. As the following block diagrams will show, the 64Kx32 and the 256Kx32 are based on x16 SRAMs, which provide two byte enable pins as well as a chip enable pin. The additional chip enable pin is required to place the device in low power, standby mode. The address bus and the enable configuration need to be considered when designing a system which can take advantage of the multiple density options provided by the x32 MCM-L family.

8L3265C and 8L32256C (64K/256Kx32 SRAM) Architecture

The EDI8L3265C (64Kx32) and 8L32256C (256Kx32) are comprised of two x16 CMOS SRAMs, 64Kx16 and 256Kx16, respectively. The address buses, write enables, and output enables of the two x16 SRAMs are internally connected between the two SRAM die providing a single address bus, write enable and output enable pin to the package pins. This provides a 50% reduction in signal connections required at the system board

Since the 8L3265C and the 8L32256C are designed using x16 SRAMs the enable configuration contains a chip enable (E\) and two byte selects (BS0 and BS1) per SRAM die. For the x32 array this leads to two chip enables (E0\ and E1\) as well as four byte selects (BS0-BS3). The byte selects provide the ability to perform byte (8 bit) wide operations while the chip enable pins allow word (16 bit) operations and are **required** to place the device in low power standby mode. Table 1 below provides a truth table description on the Enable configuration.

Table 1. Truth Table for EDI8L3265C and EDI8L32256C Enable Configuration

Enable Pins						Databus	Function	Power
E1\	E0\	BS3\	BS2\	BS1\	BS0\	Status		
H	H	X	X	X	X	High Z	standby	standby
L	L	L	L	L	L	Data Out (W\ = H)	x32 Read	active
						Data In (W\ = L)	X32 Write	active
L	L	H	H	H	H	High Z	output disable	active
H	L	X	X	L	L	DQ31-DQ16 High Z DQ15-DQ0 Active	word operation (dependent on W\ status) (See Note)	X16 active
H	L	X	X	H	L	DQ31-DQ8 High Z DQ7-DQ0 Active	byte operation (dependent on W\ status) (See Note)	X8 active

Note: This is only an example. Operations on other bytes/words are achieved by enabling the desired byte/word. Please refer to datasheet or block diagram for reference.

8L32128C and 8L32512C (128K/512Kx32) Architecture

The EDI8L32128C (128Kx32) and EDI8L32512C (512Kx32) are comprised of four x8 CMOS SRAMs, 128Kx8, and 512Kx8, respectively. The address buses, write enables, and output enables of the four x8 SRAMs are internally connected between the four SRAM die, providing a single address bus, write enable, and output enable pin to the package pins. This provides a 50% reduction in signal connections required at the system board.

Since the 8L32128C and 8L32512C are designed using x8 SRAMs the enable configuration contains a chip enable (E\) per SRAM die. For the x32 array this leads to four chip enables (E0\ - E3\). In this case the chip enables provide the ability to perform byte (8 bit) wide operations as well as place the device in low power standby mode. Chip Enables (E0\ - E3\) occupy the same pins as the byte selects (BS0 - BS3) on the EDI8L3265C and EDI8L32256C, which are based on x16 SRAM devices. Table 2 below provides a truth table description on the Enable configuration.

Table 2. Truth Table for EDI8L32128C and EDI8L32512C Enable Configuration

Enable Pins				Databus	Function	Power
E3\	E2\	E1\	E0\	Status		
X	X	X	X	High Z	standby	standby
L	L	L	L	Data Out (W\ = H)	x32 Read	active
				Data In *W\ = L)	x32 Write	active
H	H	L	L	DQ31-Dq16 High Z DQ15-DQ0 Active	word operation (dependent on W\ status) (See Note)	x16 active
H	H	H	L	DQ31-DQ8 High Z DQ7-DQ0 Active	byte operation (dependent on W\ status) (See Note)	x8 active

Note: This is only an example. Operations on other bytes/words are achieved by enabling the desired byte/word. Please refer to datasheet or block diagram for reference.

Block Diagrams

Figure 1 shows a block diagram of the EDI8L3265C and EDI8L32256C. Figure 2 show a block diagram of the EDI8L32128C and EDI8L32512C. Shaded area in each diagram indicates the boundary of the PLCC package. All signal connections within the shaded area indicate connections internal to the PLCC package.

Figure 1. EDI8L3265C and EDI8L32256C Block Diagram

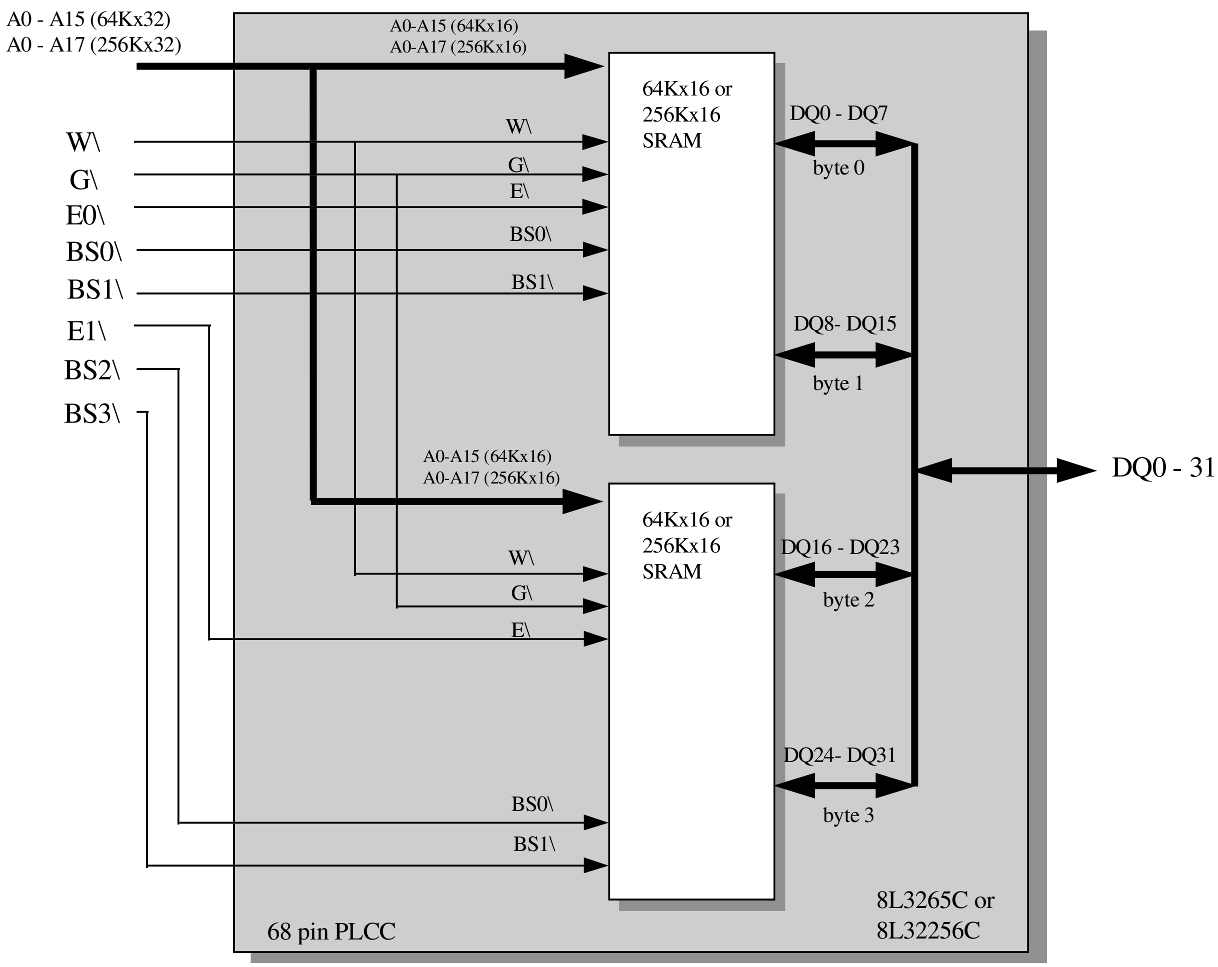
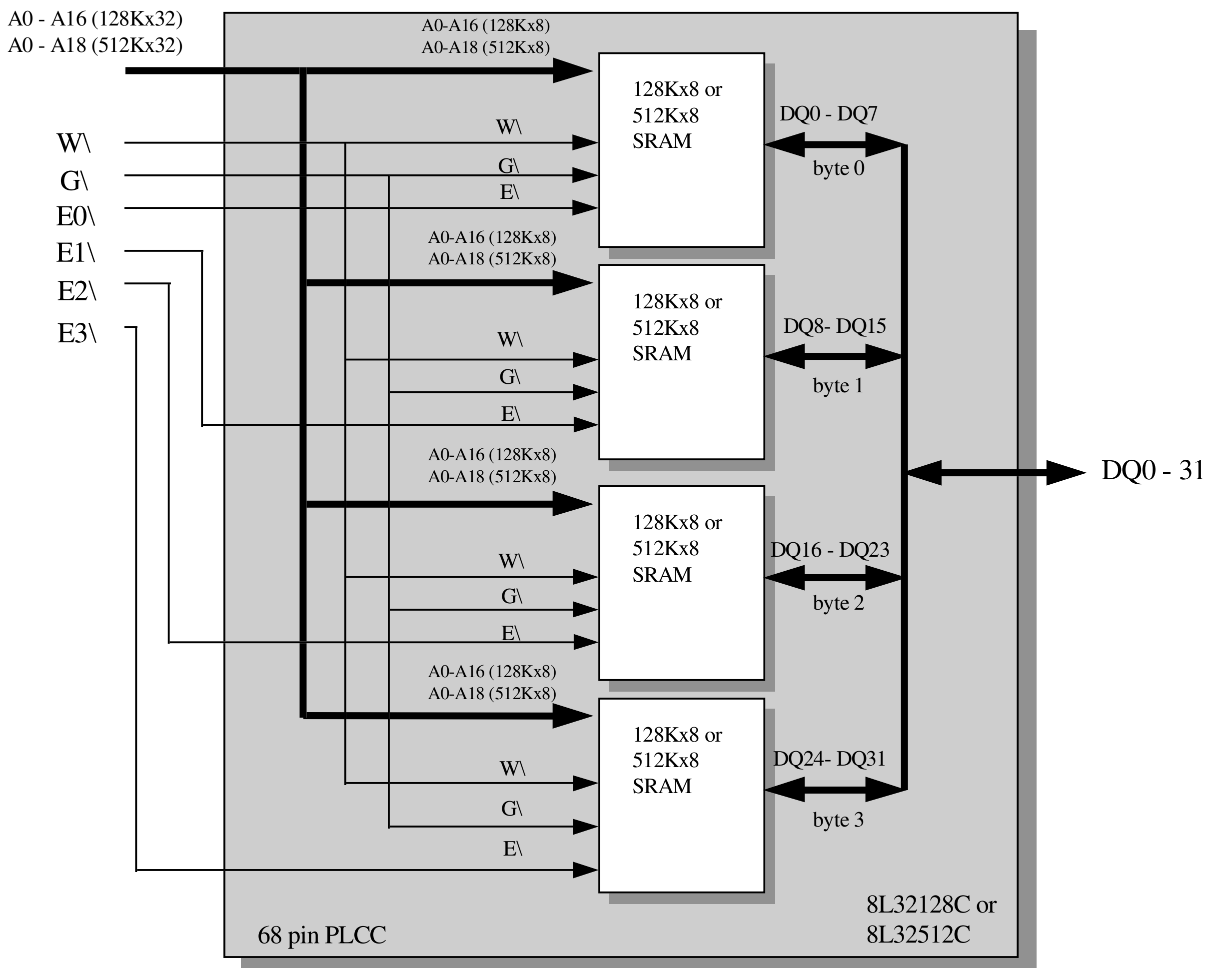


Figure 2. EDI8L32128C and EDI8L32512C Block Diagram



x32 MCM-L Family Features and Benefits

Table 3 shows the features and benefits of the x32 MCM-L family. Table 4 compares the benefits of EDI8L32128C to the benefits of other common approaches for 128Kx32 memory array.

Table 3. x32 MCM-L Family Features and Benefits

Feature	Benefit
Single component x32 SRAM Array	Improved system performance, inventory reduction
Fast Access Times : BI-CMOS 8nS to 12nS CMOS 15nS to 45nS	Wide availability of speed ranges to fit each application. CMOS and BI-CMOS in same footprint
Individual byte enables	User configurable array size, x32, x16, or x8
Master write control and output enable	Provides glueless interface
68 lead PLCC (JEDEC MO-47AE)	Manufacturing: - pick and place operations - socket availability
Multiple VCC and VSS pins	Improved noise immunity (ground bounce)
Reduced inductance and capacitance	Improved signal integrity and noise immunity
Fully asynchronous	No clock circuitry required
Upgrade path available	Upgrade to 64Kx32 through 512Kx32 without redesigning system board

Table 4. Comparison of Benefits

Memory Solution	Component package	Components required	Number of connections at system board	Board space required	Upgrade Path
EDI8L32128C	68 PLCC	1	63	0.990 sq. in.	yes (through 512Kx32)
128Kx8 Monolithic	32pin 300mil PSOJ	4	120	1.689 sq. in.	no (512Kx8 in 36 pin)
128Kx8 Monolithic	32pin 400mil PSOJ	4	120	2.020 sq. in.	no (512Kx8 in 36 pin)

Interfacing to the TI TMS320C30/31 DSP

The Texas Instruments TMS320C30 and TMS320C31 are 32 bit floating point general purpose digital signal processors. The C30 and C31 are used in a wide variety of applications including : networking, digital audio, 3-D graphics, video conferencing, and industrial automation.

The TMS320C30 has two Program/Data buses: The Primary bus, which is comprised of a 24 bit address bus and a 32 bits data bus, and an expansion bus, which is comprised of a 13 bit address bus and a 32 bit data bus. Due to the smaller address bus (13 bits = 8K depth) of the expansion bus, only the Primary bus will be considered when discussing interfacing to the EDI x32 MCM-L family. The TMS320C31 has only a Primary bus, which is identical to that of the C30. All further discussions in this section will refer to the Primary bus only and both the C30 and C31.

The primary bus interface for the C30 and C31 consists of the address and data buses, an external access strobe (STRB\), a read/write signal (R/W\), and a ready signal (RDY\). Interfacing to the EDI x32 MCM-L family is straight forward. The databus of the EDI x32 MCM-L, DQ0 - DQ31 is connected directly to the Primary databus, D0-D31, of the C30/C31. The connections may be one to one (D0 to DQ0, D1 to DQ1, etc.) or mixed in any combination (D0 to DQ12, D1 to DQ23, etc.). Since all operations are 32 bit, the order is irrelevant.

NOTE:

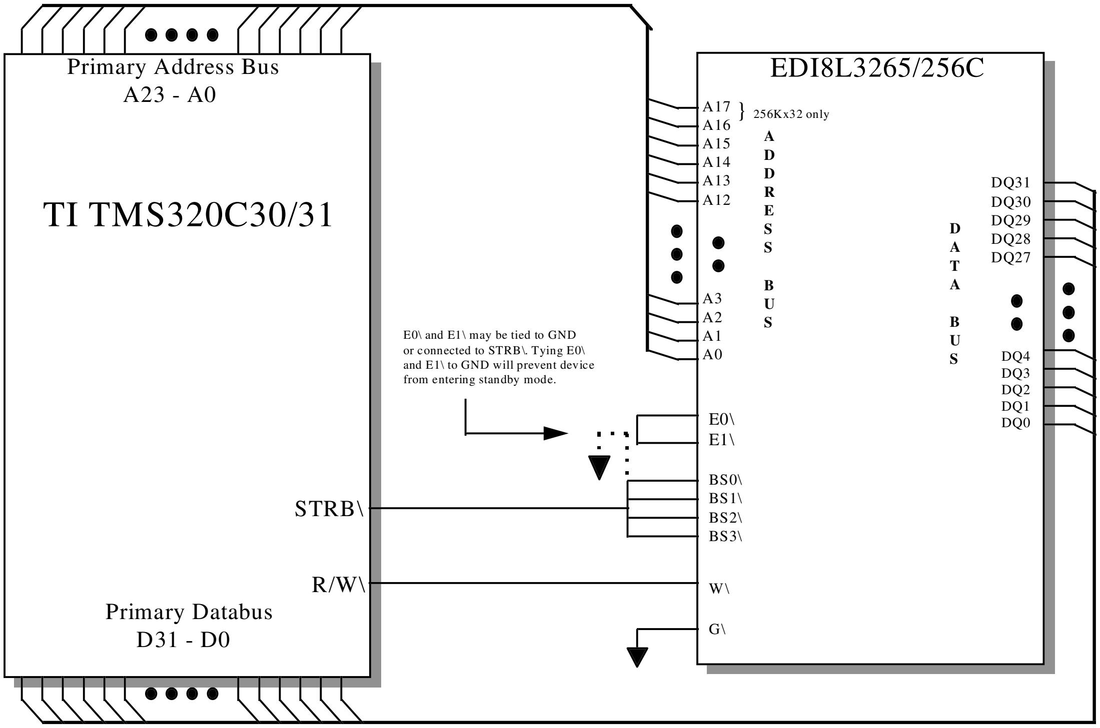
If the design also incorporates EDI’s 68-pin Flash products in the same socket, databuses must be connected one-to-one due to commands required for Flash product.

The memory control requires only two pins, the external strobe pin (STRB\) and the read/write pin (R/W\). The strobe pin acts an enable pin and is connected to the chip enable pins of the x32 MCM-L product. As described earlier in the device architecture section, the Enable configuration differs slightly between the 64K/256Kx32 and the 128K/512Kx32 products. This difference needs to be accounted and is described in the following text. The read/write pin connects directly to the write enable pin on the x32 MCM-L products and controls write and read functionality.

The outputs are switched to the high impedance state via STRB\ going high (memory disable) or via R/W\ pin going low (memory enters write mode). Therefore, the output enable functionality is not required via the output enable (G\) pin, and it may be tied to ground.

Figure 3 shows the interface to the EDI8L3265C or EDI8L32256C.

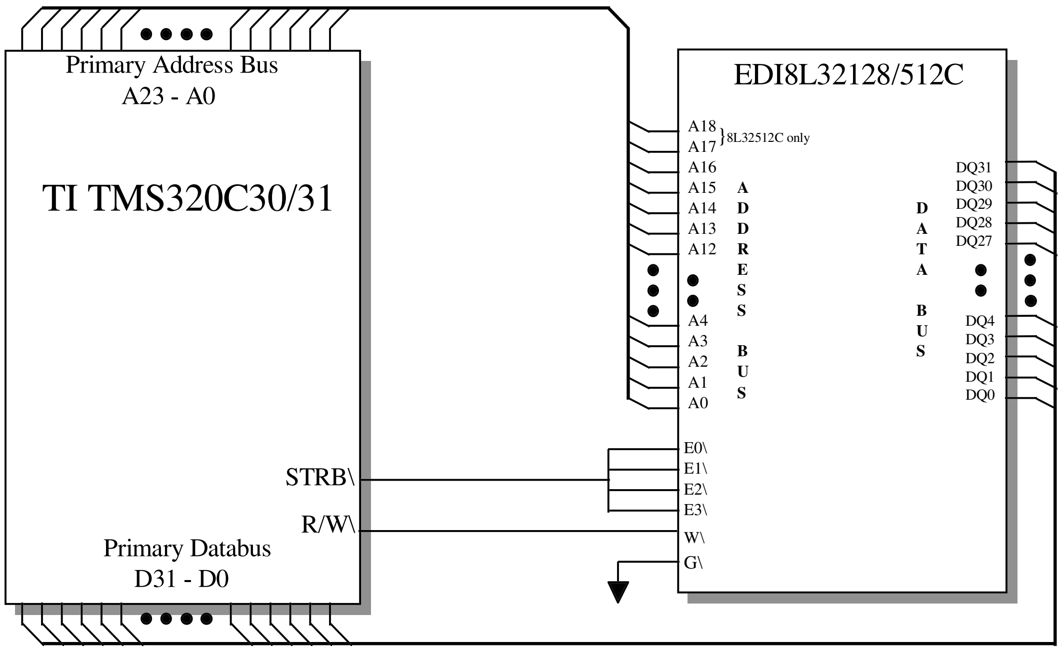
Figure 3. Interfacing the C30/C31 to the EDI8L3265C or EDI8L32256C



Of particular interest is the connection of the external strobe of the C30/C31 to the Enable pins of the EDI8L3265C or the EDI8L32256C. The byte select pins, BS0\ -BS3\, are connected directly to the strobe pin of the C30/C31, STRB\. The Chip Enable pins, E0\ - E1\, may be connected in one of two ways: E0\ and E1\ may be tied to ground or also connected to the STRB\ pin. If E0\ and E1\ are tied to ground the device will not be able to enter low power standby mode. If connected to STRB\, the memory will enter low power standby mode when STRB\ pin is active high. The decision on which implementation is best should be based on system power requirements. Databus pins D31 - D0 of the TMS320C30/31 are connected to the corresponding DQ31 - DQ0 of the 8L3265C or 8L32256C.

Figure 4 shows interfacing to either the EDI8L32128C or EDI8L32512C.

Figure 4. Interfacing the C30/C31 to the EDI8L32128C or EDI8L32512C



In this case, the strobe pin of the C30 and C31 is connected to the four chip enable pins, E0\ - E3\, of the memory array. The device enters low power standby mode whenever STRB\ of the C30/C31 is active high. E0\ - E3\ of the 128Kx32 and 512Kx32 are located on the same device pins as the BS0\ - BS3\ pins on the 64Kx32 and 256Kx32. Therefore, when considering upgrade paths the decisions required are the connection of E0\ and E1\ on the 64Kx32 and the 256Kx32 and supplying the extra address signals required for the additional density. Databus pins D31 - D0 of the TMS320C30/31 are connected to the corresponding DQ31 - DQ0 of the 8L32128C/512C.

Interfacing to the TI TMS320C32

The TMS320C32 is the newest member of the C3X family. The major change from the C30/C31 DSPs is the enhanced memory interface.

The enhanced memory interface supports 8/16/32 bit wide data access from external RAM and 16/32 bit wide program execution from external RAM. The configurable external memory interface allows system designers to reduce system costs by minimizing external memory chip count. The memory interface consists of a 24 bit address bus, a 32 bit databus, a read/write signal (R/W\), a program memory width select pin (PRGW), a ready signal (RDY\), and three independent multi-function strobes. The IOSTRB\ signal is a single pin strobe that allows only 32 bit accesses. STRB0\ and STRB1\ are a group of four pins each, B0 - B3, which provides the ability to use 8 bit or 16 bit memory arrays, as well as 32 bit memory arrays.

Since the C32 uses a 32 bit internal bus, there is no need to configure EDI's 32 bit wide products as 8 bit or 16 bit wide arrays. This section will only discuss 32 bit interfacing to the STRB0 and STRB1 interfaces of the TMS320C32. The interface to the IOSTRB\ signal is identical to the C30/C31 interface. More detailed information on the operation of the C32 memory interface for 8 bit or 16 bit memory may be found in the TMS320C32 datasheet or in the TI application report, Interfacing Memory to the TMS320C32, which can be downloaded from the TI web page (www.ti.com).

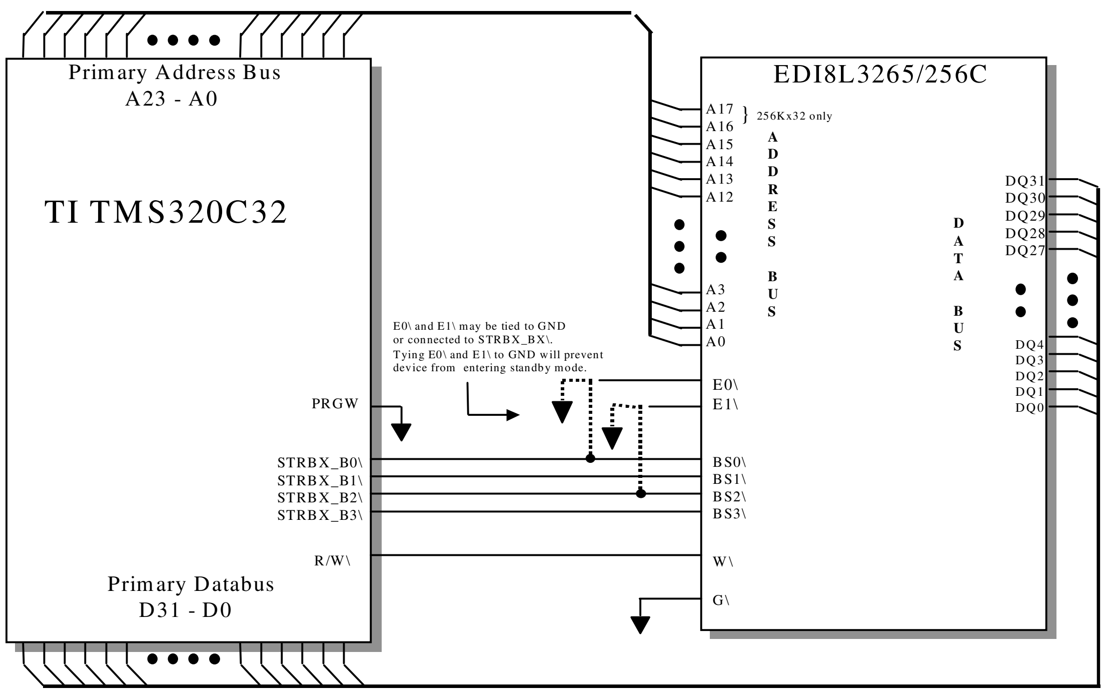
STRB0 and STRB1 function identically and will be referred to as STRBX in the following text. The multi-function strobes consist of 4 control lines, STRBX_B0 through STRBX_B3. The control lines have identical timing and control each byte of a 32 bit memory array. This is ideal when interfacing to the EDI x32 MCM-L SRAM (or Flash) products due to the four enables associated with the memory array. Interfacing the C32 to the EDI8L3265C and EDI8L32256C products is demonstrated in Figure 5. Interfacing to the EDI8L32128C and EDI8L32512C is shown in Figure 6. The interface is identical to that of the C30 and C31 except for the addition of the PRGW pin on the C32 and the STRBX interface. PRGW (the program memory width select) pin is tied low for 32 bit operations. As shown in the figures, the four strobe lines STRBX_B0 through STRBX_B3 are connected to the enable pins, E0\ - E3\ on the EDI8L32128C and EDI8L32512C and B0\ - B3\ on the EDI8L3265C and EDI8L32256C. The read/write pin connects directly to the write enable pin on the x32 MCM-L products and controls write and read functionality.

The outputs are switched to the high impedance state via STRBX_B0\ - B3\ going high, (memory disable), or via R/W\ pin going low (memory enters write mode). Therefore the output enable functionality is not required via the output enable (G\) pin and it may be tied to ground.

Of primary interest is the connection of the external strobe of the C32 to the Enable pins of the EDI8L3265C or the 8L32256C. The byte select pins, BS0\ -BS3\, are connected directly to the strobe pin of the C32, STRBX_B0\ - B3\. The Chip Enable pins, E0\ - E1\, may be connected in one of two ways. E0\ and E1\ may be tied to ground or connected to the STRBX pins. If E0\ and E1\ are tied to ground the device will not be able to enter low power standby mode. If connected to STRBX\ pins the memory will enter low power standby mode when STRBX\ pins are active high. Decision on best implementation should be based on system power requirements.

Figure 5 shows one option of connecting E0\ and E1\ to the STRBX\ pins.

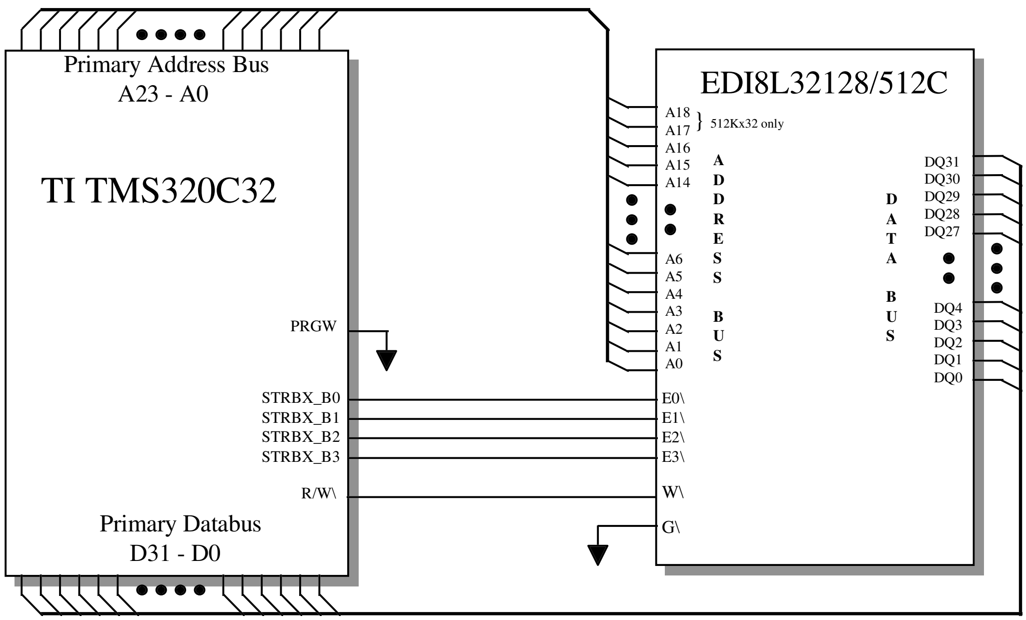
Figure 5. Interfacing the C32 to the EDI8L3265C or EDI8L32256C Using STRBX 32 bit Interface



Here E0\ is connected to STRBX_B0\ (shown as an option in dashed line) and E1\ is connected to STRBX_B2. This connection is a matter of convention only. Since E0\ controls the lower word of the 32 bit SRAM array and E1\ controls the upper word they are connected to the STRBX byte control signal, which controls the lowest order byte in each word. In reality, since all operations are 32 bit, E0\ and E1\ may be connected to any of the STRBX pins. The strobe pins (STRBX_B0\ through B3\) of the TMS320C32 are connected directly to the four byte enables (BS0\ - BS3\) of the EDI8L3265C. The Chip Enable pins of the 8L3265C or 8L32256C (E0\ and E1\) may be connected to STRBX or tied to ground. In this example E0\ is tied to STRBX_B0\ and E1\ is tied to STRBX_B2\ for convention purposes only. E0\ controls the two bytes associated with STRBX_B0\ and B1\ and E1\ controls the two bytes associated with STRBX_B2\ and B3\. For 32 bit operations, E0\ and E1\, may be tied to any STRBX pin. Databus pins D31 - D0 of the TMS320C32 are connected to the corresponding DQ31 - DQ0 of the 8L3265C or 8L32256C.

Figure 6 shows an example of 32 bit memory interfacing using STRBX.

Figure 6. Interfacing the C32 to the EDI8L32128C or EDI8L32512C Using STRBX 32 Bit Interface



The four strobe pins (STRBX_B0 - STRBX_B3) of the TMS320C32 are connected directly to the four chip enables (E0\ - E3\) of the EDI8L32128C/512C. Databus pins D31 - D0 of the TMS320C32 are connected to the corresponding DQ31 - DQ0 of the 8L32128C/512C.

Matching Memory Access to DSP Bus Frequency

Table 5 compares the various DSP speed options available in the TMS320C3x family and presents the memory access required for zero wait state operation. The table also presents the EDI x32 MCM-L SRAM device part number required for zero wait state operation.

Table 5. Memory Access Time versus DSP Bus Frequency

DSP	External Bus Cycle Time	Memory Access Required (2)	EDI Part Number (1)	Memory Access
TMS320C32-60	33nS	16nS	EDI8L32XXXC15AC	15nS
TMS320C3x-50	40nS	21nS	EDI8L32XXXC20AC	20nS
TMS320C3x-40	50nS	25nS	EDI8L32XXXC25AC	25nS
TMS320C3x-33	60nS	30nS	EDI8L32XXXC25AC	25nS
TMS320C3x-27	74nS	40nS	EDI8L32XXXC25AC	25nS

Notes: 1) XXX in EDI part number refers to device density and is substituted as follows:
65=64Kx32
128=128Kx32
256=256Kx32
512=512Kx32

2) Requirements may differ depending on system board design, capacitive loading, signal line lengths, etc. For example, the 16nS memory requirement for the TMS320C32-60 should be met with the 15nS EDI device. However, under non-ideal conditions (heavy loading, etc.), the 1nS guardband may not be sufficient and may require the next fastest access memory component. In this example, the EDI8L32XXXB12, with a 12 nS, access may be required.

Summary

EDI' s x32 MCM-L SRAM product family provides an ideal memory solution for the TMS320C3x family of DSPs. In addition to the space savings typically associated with module approaches, EDI's x32 SRAM family also provides a wide variety of density and speed performance options within the same 68 pin PLCC package. Densities are available from 64Kx32 through 512Kx32 and access speeds from 8nS through 25nS. This wide range of options allows system designers to provide a system design with multiple options and the ability to use single designs across multiple applications.

The single address bus , data bus and write enable pin provides an easy interface to the TMS320C3x family of DSPs that requires no additional logic.

References

TMS320C3x User's Guide

TMS320C32 Datasheet

EDI8L3265C Datasheet

EDI8L32128C Datasheet

EDI8L32256C Datasheet

EDI8L32512C Datasheet

TMS320C32 datasheet available on-line at: www.ti.com. EDI datasheets available on-line at: www.electronic-designs.com.