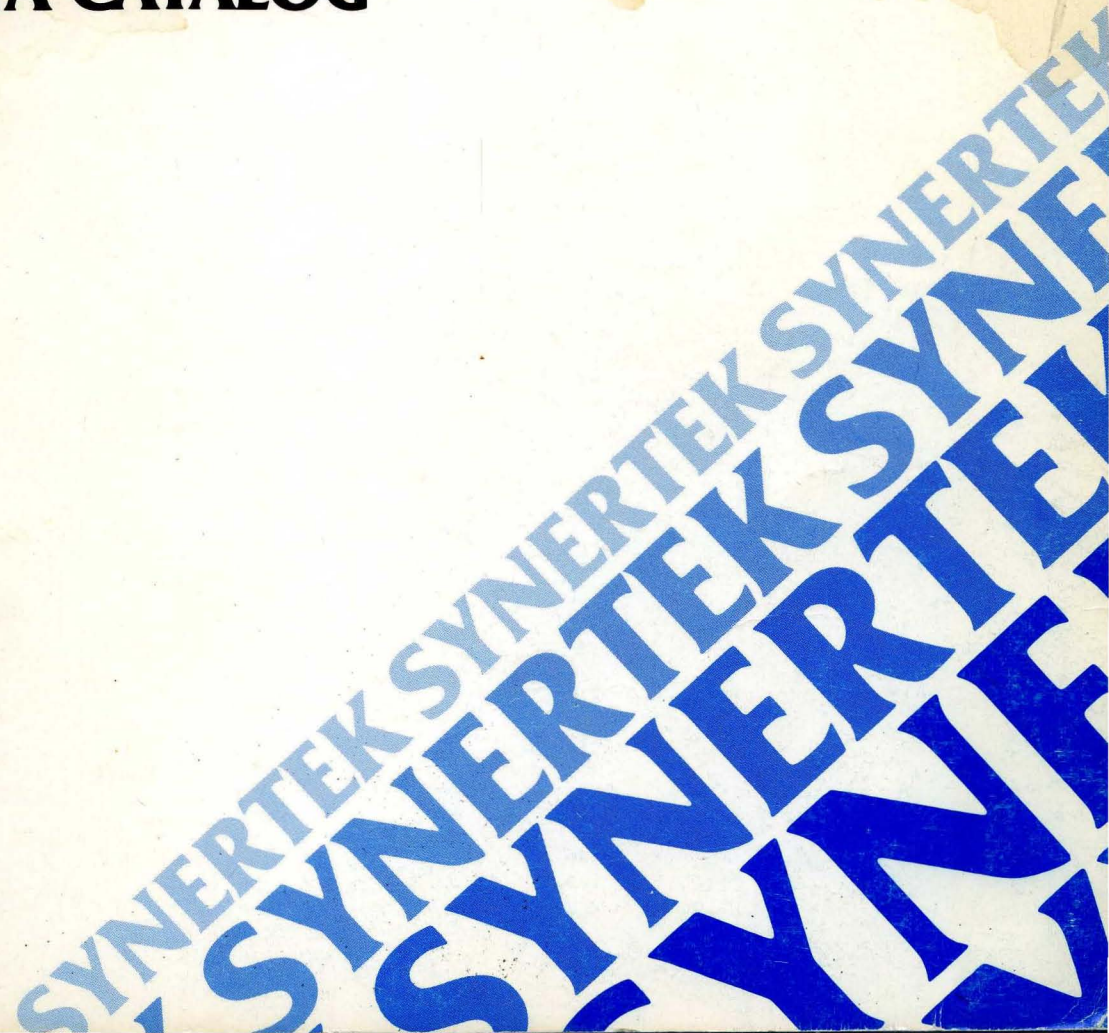
$5.00

SYNERTEK 1981-1982 DATA CATALOG



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SYNERTEK
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Random Access Memories

SAMPLE

RAM Selector Guide

Commercial: $T_A = 0°C$ to $+70°C$

Part No.	Organization	No. of Pins	Access Time (ns) Max.	Maximum Current (mA) Operating	Maximum Current (mA) Standby	Power Supply (Volts)	Page
SY2101-1	256 x 4	22	500	70	—	+5	1-3
SY2101A	256 x 4	22	350	55	—	+5	1-3
SY2101A-2	256 x 4	22	250	55	—	+5	1-3
SY2101A-4	256 x 4	22	450	55	—	+5	1-3
SY2111-1	256 x 4	18	500	70	—	+5	1-7
SY2111A	256 x 4	18	350	55	—	+5	1-7
SY2111A-2	256 x 4	18	250	55	—	+5	1-7
SY2111A-4	256 x 4	18	450	55	—	+5	1-7
SY2112-1	256 x 4	16	500	70	—	+5	1-11
SY2112A	256 x 4	16	350	55	—	+5	1-11
SY2112A-2	256 x 4	16	250	55	—	+5	1-11
SY2112A-4	256 x 4	16	450	55	—	+5	1-11
SY2114	1024 x 4	18	450	100	—	+5	1-17
SY2114-1	1024 x 4	18	150	100	—	+5	1-17
SY2114-2	1024 x 4	18	200	100	—	+5	1-17
SY2114-3	1024 x 4	18	300	100	—	+5	1-17
SY2114L	1024 x 4	18	450	70	—	+5	1-17
SY2114L-1	1024 x 4	18	150	70	—	+5	1-17
SY2114L-2	1024 x 4	18	200	70	—	+5	1-17
SY2114L-3	1024 x 4	18	300	70	—	+5	1-17
SY2114LV	1024 x 4	18	450	70	—	+5[1]	1-21
SY2114LV-2	1024 x 4	18	200	70	—	+5[1]	1-21
SY2114LV-3	1024 x 4	18	300	70	—	+5[1]	1-21
SY2142	1024 x 4	20	450	100	—	+5	1-26
SY2142-2	1024 x 4	20	200	100	—	+5	1-26
SY2142-3	1024 x 4	20	300	100	—	+5	1-26
SY2142L	1024 x 4	20	450	70	—	+5	1-26
SY2142L-2	1024 x 4	20	200	70	—	+5	1-26
SY2142L-3	1024 x 4	20	300	70	—	+5	1-26
SY2142LV	1024 x 4	20	450	70	—	+5[1]	1-30
SY2142LV-2	1024 x 4	20	200	70	—	+5[1]	1-30
SY2142LV-3	1024 x 4	20	300	70	—	+5[1]	1-30
SY2148H	1024 x 4	18	70	150	30	+5	1-40
SY2148H-2	1024 x 4	18	45	150	30	+5	1-40
SY2148H-3	1024 x 4	18	55	150	30	+5	1-40
SY2148HL	1024 x 4	18	70	125	20	+5	1-40
SY2148HL-3	1024 x 4	18	55	125	20	+5	1-40
SY2149H	1024 x 4	18	70	150	—	+5	1-45
SY2149H-2	1024 x 4	18	45	150	—	+5	1-45
SY2149H-3	1024 x 4	18	55	150	—	+5	1-45
SY2149HL	1024 x 4	18	70	125	—	+5	1-45
SY2149HL-3	1024 x 4	18	55	125	—	+5	1-45
SY2147	4096 x 1	18	70	160	20	+5	1-34
SY2147-3	4096 x 1	18	55	180	30	+5	1-34
SY2147-6	4096 x 1	18	85	160	20	+5	1-34
SY2147L	4096 x 1	18	70	140	10	+5	1-34
SY2147H[2]	4096 x 1	18	35-70	180	30	+5	1-38
SY2128[2]	2048 x 8	24	120-200	100	30	+5	1-25

Military: $T_A = -55°C$ to $+125°C$

SYM2148[2]	1024 x 4	18	70	150	30	+5	1-44
SYM2148-6[2]	1024 x 4	18	85	150	30	+5	1-44
SYM2149H[2]	1024 x 4	18	70	150	—	+5	1-49
SYM2149H-3[2]	1024 x 4	18	55	150	—	+5	1-49
SYM2147[2]	4096 x 1	18	70	180	30	+5	1-39
SYM2147-6[2]	4096 x 1	18	85	180	30	+5	1-39

1. +2.5V Data Retention
2. To Be Announced.

256 x 4 Static Random Access Memory

SY2101

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

RAMs

- 256x4 Organization to Meet Needs For Small System Memories
- Access Time – 250/350/450/500/ns
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Two Chip Enable Inputs
- Inputs Protected – All Inputs Have Protection Against Static Charge
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Three-State Output – OR-Tie Capability
- Output Disable Provided For Ease of Use in Common Data Bus Systems

The SY2101 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

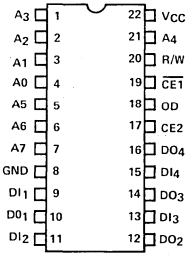
The SY2101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two Chip Enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

The SY2101 is fabricated with N-channel ion implanted silicon gate technology. This technology allows the design and production of high-performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

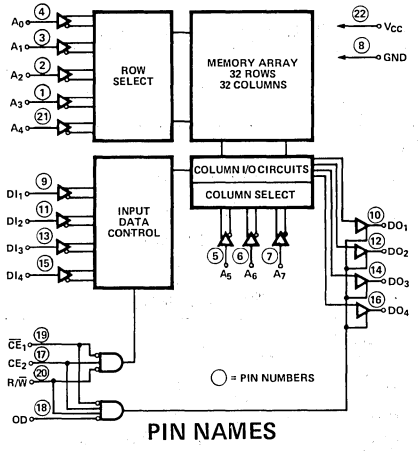
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2101-1	Plastic DIP	500 ns	0°C to 70°C
SYC2101-1	Ceramic DIP	500 ns	0°C to 70°C
SYP2101A-2	Plastic DIP	250 ns	0°C to 70°C
SYC2101A-2	Ceramic DIP	250 ns	0°C to 70°C
SYP2101A	Plastic DIP	350 ns	0°C to 70°C
SYC2101A	Ceramic DIP	350 ns	0°C to 70°C
SYP2101A-4	Plastic DIP	450 ns	0°C to 70°C
SYC2101A-4	Ceramic DIP	450 ns	0°C to 70°C

BLOCK DIAGRAM



PIN NAMES

DIN	DATA INPUT	OD	OUTPUT DISABLE
A0–A7	ADDRESS INPUTS	DOUT	DATA OUTPUT
R/W	READ/WRITE INPUT	VCC	POWER (+5V)
CE1, CE2	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2101-1 Min.	2101-1 Typ.(1)	2101-1 Max.	2101A-2 2101A, 2101A-4 Min.	2101A-2 2101A, 2101A-4 Typ.(1)	2101A-2 2101A, 2101A-4 Max.	Unit	Test Conditions
I_{LI}	Input Current			10			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current(2)			15			10	µA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current(2)			-50			-10	µA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60		30	50	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70			55	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			+0.45			+0.4	V	I_{OL} = 3.2mA (I_{OL} = 2.0mA 2101-1)
V_{OH}	Output High Voltage	2.2			2.4			V	I_{OH} = -150µA

NOTE: 1. Typical Values are for T_A = 25°C and nominal supply voltage. 2. Input and Output tied together.

CAPACITANCE T_A = 25°C, f = 1MHz

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12	pF

A.C. CHARACTERISTICS — SY2101-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	500		ns
t_A	Access Time		500	ns
t_{CO}	Chip Enable To Output		350	ns
t_{OD}	Output Disable To Output		300	ns
t_{DF}[1]	Data Output to High Z State	0	150	ns
t_{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	500		ns
t_{AW}	Write Delay	100		ns
t_{CW}	Chip Enable To Write	400		ns
t_{DW}	Data Setup	280		ns
t_{DH}	Data Hold	100		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	50		ns

A.C. CHARACTERISTICS – SY2101A-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable To Output		180	ns
t_{OD}	Output Disable To Output		130	ns
t_{DF}[1]	Data Output to High Z State	0	180	ns
t_{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	250		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	150		ns
t_{DW}	Data Setup	150		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	150		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

A.C. CHARACTERISTICS – SY2101A

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable To Output		240	ns
t_{OD}	Output Disable To Output		180	ns
t_{DF}[1]	Data Output to High Z State	0	150	ns
t_{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	350		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	200		ns
t_{DW}	Data Setup	200		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	200		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

NOTE: 1 t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.

A.C. CHARACTERISTICS – SY2101A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

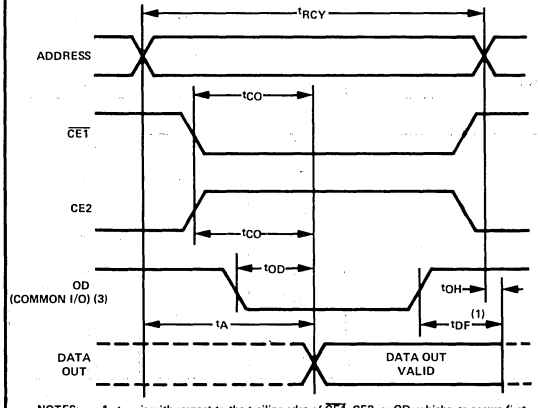
Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable To Output		310	ns
t_{OD}	Output Disable To Output		250	ns
t_{DF}[1]	Data Output to High Z State	0	200	ns
t_{OH}	Previous Data Read Valid after change of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	450		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	250		ns
t_{DW}	Data Setup	250		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	250		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

A.C. CONDITIONS OF TEST

	2101A-2 2101A 2101A-4	2101-1
Input Pulse Levels	+0.8V to 2.0V	+0.65V to 2.2V
Input Pulse Rise & Fall Times	10ns	10ns
Timing Measurement Reference Level: Inputs	1.5V	1.5V
Outputs	0.8V & 2.0V	0.8V & 2.0V
Output Load	1 TTL Gate & C_L = 100pF	1 TTL Gate & C_L = 100pF

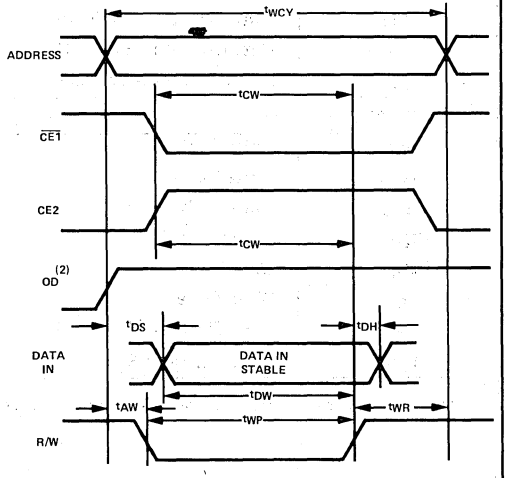
TIMING DIAGRAMS

READ CYCLE



NOTES:
1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
2. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
3. OD should be tied low for separate I/O operation.

WRITE CYCLE



256 x 4 Static Random Access Memory

SY2111

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

RAMs

- Organization 256 Words By 4 Bits
- Common Data Input And Output
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 250/350/450/500ns
- Simple Memory Expansion — 2 Chip Enable Inputs
- Fully Decoded — On-Chip Address Decode
- Inputs Protected — All Inputs have Protection Against Static Charge
- Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration
- Low Power — Typically 150mW
- Three - State Output — OR - Tie Capability

The SY2111 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

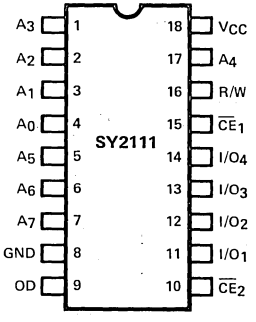
The SY2111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate Chip Enable leads allow easy selection of an individual package when outputs are OR-tied.

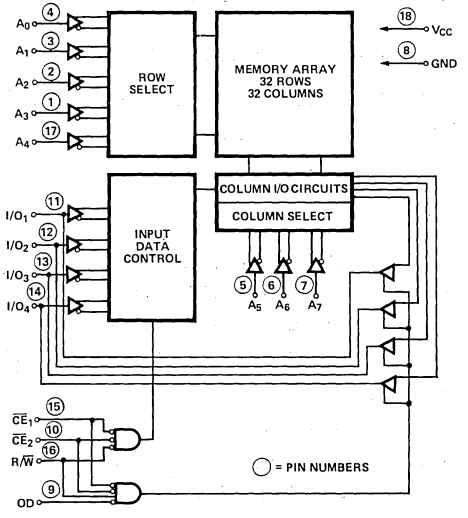
The SY2111 is fabricated with N-channel ion-implanted silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2111-1	Plastic DIP	500 ns	0°C to 70°C
SYD2111-1	Cerdip	500 ns	0°C to 70°C
SYP2111A-2	Plastic DIP	250 ns	0°C to 70°C
SYD2111A-2	Cerdip	250 ns	0°C to 70°C
SYP2111A	Plastic DIP	350 ns	0°C to 70°C
SYD2111A	Cerdip	350 ns	0°C to 70°C
SYP2111A-4	Plastic DIP	450 ns	0°C to 70°C
SYD2111A-4	Cerdip	450 ns	0°C to 70°C

PIN NAMES

A0-A7	ADDRESS INPUTS	$\overline{CE}_1$	CHIP ENABLE 1
OD	OUTPUT DISABLE	$\overline{CE}_2$	CHIP ENABLE 2
R/W	READ/WRITE INPUT	I/O1-I/O4	DATA INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

		2111-1			2111A 2111A-2, 2111A-4				
Symbol	Parameter	Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15			10	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50			-10	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60		30	50	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70			55	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45			0.4	V	I_{OL} = 3.2mA (I_{OL} = 2.0mA - 2111-1)
V_{OH}	Output High Voltage	2.2			2.4			V	I_{OH} = -150µA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS – SY2111-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	500		ns
t_A	Access Time		500	ns
t_{CO}	Chip Enable To Output		350	ns
t_{OD}	Output Disable To Output		300	ns
t_{DF}[1]	Data Output To High Z State	0	150	ns
t_{OH}	Previous Data Read Valid After Change Of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	500		ns
t_{AW}	Write Delay	100		ns
t_{CW}	Chip Enable To Write	400		ns
t_{DW}	Data Setup	280		ns
t_{DH}	Data Hold	100		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	50		ns
t_{DS}	Output Disable Setup	20		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of CE1, CE2, or OD, whichever comes first.

A.C. CHARACTERISTICS – SY2111A-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable To Output		180	ns
t_{OD}	Output Disable To Output		130	ns
t_{DF}[1]	Data Output To High Z State	0	180	ns
t_{OH}	Previous Data Read Valid After Change Of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	250		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	150		ns
t_{DW}	Data Setup	150		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	150		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

A.C. CHARACTERISTICS – SY2111A

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable To Output		240	ns
t_{OD}	Output Disable To Output		180	ns
t_{DF}[1]	Data Output To High Z State	0	150	ns
t_{OH}	Previous Data Read Valid After Change Of Address	40		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	350		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	200		ns
t_{DW}	Data Setup	200		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	200		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever comes first.

A.C. CHARACTERISTICS – SY2111A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable To Output		310	ns
t_{OD}	Output Disable To Output		250	ns
t_{DF} [1]	Data Output To High Z State	0	200	ns
t_{OH}	Previous Data Read Valid After Change Of Address	40		
WRITE CYCLE				
t_{WCY}	Write Cycle	450		ns
t_{AW}	Write Delay	20		ns
t_{CW}	Chip Enable To Write	250		ns
t_{DW}	Data Setup	250		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	250		ns
t_{WR}	Write Recovery	0		ns
t_{DS}	Output Disable Setup	20		ns

A.C. CONDITIONS OF TEST

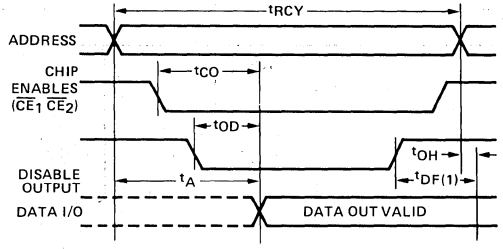
	2111A, 2111A-2, 2111A-4	2111-1
Input Pulse Levels	+0.8V to 2.0V	+0.65V to 2.2V
Input Pulse Rise & Fall Times:	10ns	10ns
Timing Measuremnt Reference Level Inputs:	1.5V	1.5V
Outputs:	0.8V & 2.0V	0.8V & 2.0V
Output Load:	1 TTL Gate & C_L = 100pF	1 TTL Gate & C_L = 100pF

CAPACITANCE T_A = 25°C, f = 1 MHz

Symbol	Test	Typ.	Max	Unit
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15	pF

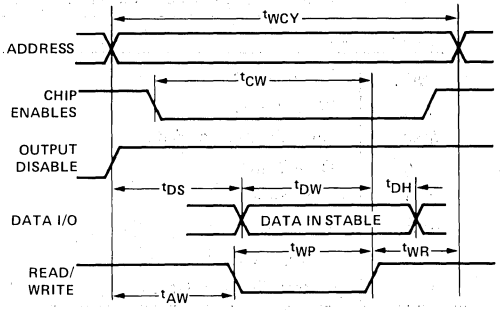
TIMING DIAGRAMS

READ CYCLE



NOTE: 1. t_{DF} is with respect to the trailing edge of CE1, CE2 or OD, whichever comes first.

WRITE CYCLE



256 x 4 Static Random Access Memory

SY2112

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

RAMs

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Static MOS - No Clocks or Refreshing Required
- Access Time - 250/350/450/500 ns
- Simple Memory Expansion - Chip Enable Input
- Fully Decoded - On-Chip Address Decode
- Inputs Protected - All Inputs Have Protection Against Static Charge
- Low Cost Packaging - 16 Pin Plastic Dual-In-Line Configuration
- Low Power - Typically 150 mW
- Three-State Output - OR-tie Capability

The SY2112 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

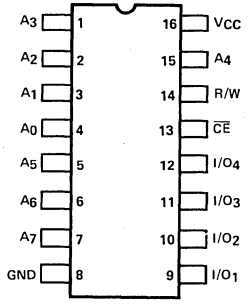
The SY2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Enable lead allows easy selection of an individual package when outputs are OR-tied.

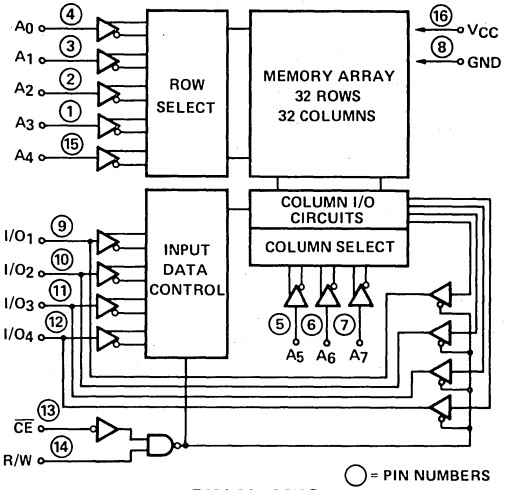
The SY2112 is fabricated with ion implanted N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2112A-2	Plastic DIP	250nsec	0°C to 70°C
SYD2112A-2	Cerdip	250nsec	0°C to 70°C
SYP2112A	Plastic DIP	350nsec	0°C to 70°C
SYD2112A	Cerdip	350nsec	0°C to 70°C
SYP2112A-4	Plastic Dip	450nsec	0°C to 70°C
SYD2112A-4	Cerdip	450nsec	0°C to 70°C
SYP2112-1	Plastic DIP	500nsec	0°C to 70°C
SYD2112-1	Cerdip	500nsec	0°C to 70°C

PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS – SY2112A, SY2112A-2, SY2112A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			10	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-10	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	50	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	I_{OL} = 3.2mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -150μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

D. C. AND OPERATING CHARACTERISTICS – SY2112-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. CHARACTERISTICS – SY2112A-2

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable to Output Time		180	ns
t_{CD}	Chip Enable to Output Disable Time	0	120	ns
t_{OH}	Previous Read Data Valid After Change of Address	40		ns

WRITE CYCLE NO. 1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	250		ns
t_{AW1}	Address to Write Setup Time	20		ns
t_{DW1}	Write Setup Time	180		ns
t_{WP1}	Write Pulse Width	180		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	180		ns

WRITE CYCLE NO. 2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	250		ns
t_{AW2}	Address to Write Setup Time	20		ns
t_{DW2}	Write Setup Time	180		ns
t_{WD2}	Write To Output Disable Time	120	100	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable to Output Time		240	ns
t_{CD}	Chip Enable to Output Disable Time	0	200	ns
t_{OH}	Previous Read Data Valid After Change of Address	40		ns

A. C. CHARACTERISTICS – SY2112A (Cont.)

WRITE CYCLE NO. 1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	350		ns
t_{AW1}	Address to Write Setup Time	20		ns
t_{DW1}	Write Setup Time	250		ns
t_{WP1}	Write Pulse Width	250		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	250		ns

WRITE CYCLE NO. 2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	350		ns
t_{AW2}	Address to Write Setup Time	20		ns
t_{DW2}	Write Setup Time	250		ns
t_{WD2}	Write To Output Disable Time	200	130	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A-4

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable to Output Time		200	ns
t_{CD}	Chip Enable to Output Disable Time	0	260	ns
t_{OH}	Previous Read Data Valid After Change of Address	40		ns

WRITE CYCLE NO. 1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	450		ns
t_{AW1}	Address to Write Setup Time	20		ns
t_{DW1}	Write Setup Time	300		ns
t_{WP1}	Write Pulse Width	300		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	300		ns

A. C. CHARACTERISTICS – SY2112A-4 (Cont.)

WRITE CYCLE NO. 2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	450		ns
t_{AW2}	Address to Write Setup Time	20		ns
t_{DW2}	Write Setup Time	300		ns
t_{WD2}	Write To Output Disable Time	260	150	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112-1

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	500		ns	t_r, $t_f \leqslant$20ns
t_A	Access Time		500	ns	0.65V $\geqslant V_{IN} \geqslant$ 2.2V
t_{CO}	Chip Enable To Output Time		350	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0	150	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	0		ns	C_L = 100pF

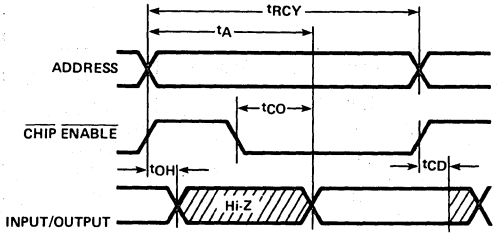
WRITE CYCLE NO. 1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WCY1}	Write Cycle	500		ns	t_r, $t_f \leqslant$20ns
t_{AW1}	Address To Write Setup Time	100		ns	0.65V $\geqslant V_{IN} \geqslant$ 2.2V
t_{DW1}	Write Setup Time	200		ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300		ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0	100	ns	C_L = 100pF
t_{CH1}	Chip Enable Hold Time	0		ns	
t_{WR1}	Write Recovery Time	50		ns	
t_{DH1}	Data Hold Time	100		ns	
t_{CW1}	Chip Enable to Write Setup Time	200		ns	

WRITE CYCLE NO. 2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WCY2}	Write Cycle	500		ns	t_r, $t_f \leqslant$20ns
t_{AW2}	Address To Write Setup Time	100		ns	0.65V $\geqslant V_{IN} \geqslant$ 2.2V
t_{DW2}	Write Setup Time	200		ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	100		ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0		ns	C_L = 100pF
t_{CH2}	Chip Enable Hold Time	0		ns	
t_{WR2}	Write Recovery Time	50		ns	
t_{DH2}	Data Hold Time	100		ns	

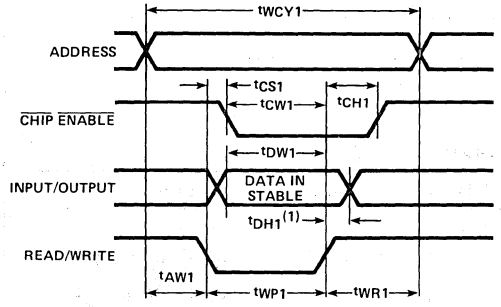
READ CYCLE WAVEFORMS



CAPACITANCE

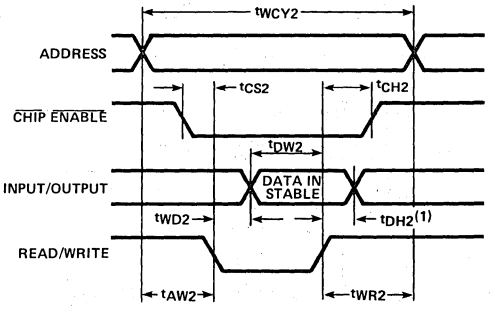
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	18

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V±5%



NOTE 1. Data Hold Time. (T_{DH}) is reference to the trailing edge of CHIP ENABLE (CE)or READ/WRITE (R/W) whichever comes first.

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V±5%

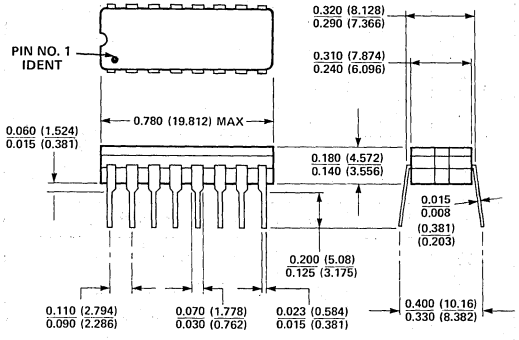


A.C. CONDITIONS OF TEST

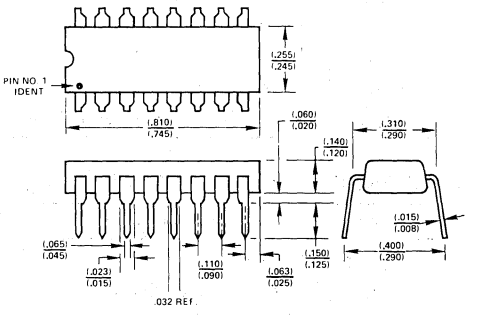
Input Pulse Leads ..... 0.8 to 2.0 Volt
Input Pulse Rise and Fall Times ..... 10 nsec
Timing Measurement Reference Level: Input ..... 1.5 Volt
Output ..... 0.8 and 2.0 Volt
Output Load ..... 1 TTL Gate and C_L = 100 pF

PACKAGE DIAGRAM

CERDIP PACKAGE



PLASTIC PACKAGE



1024 x 4 Static Random Access Memory

SY2114

SYNERTEK
A SUBSIDIARY OF HONEYWELL

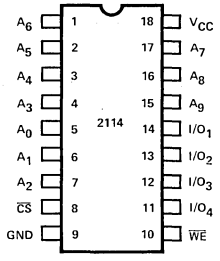
MEMORY PRODUCTS

RAMs

- 150 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

PIN CONFIGURATION



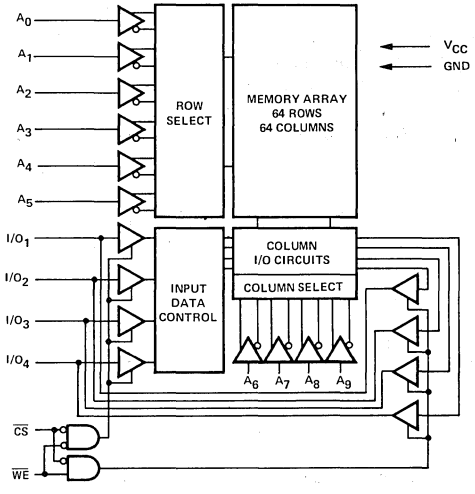
ORDERING INFORMATION

Order Number	Access Time	Supply Current	Package Type	Temperature Range
SYD2114-1	150nsec	100mA	Cerdip	0°C to 70°C
SYP2114-1	150nsec	100mA	Plastic	0°C to 70°C
SYD2114-2	200nsec	100mA	Cerdip	0°C to 70°C
SYP2114-2	200nsec	100mA	Plastic	0°C to 70°C
SYD2114-3	300nsec	100mA	Cerdip	0°C to 70°C
SYP2114-3	300nsec	100mA	Plastic	0°C to 70°C
SYD2114	450nsec	100mA	Cerdip	0°C to 70°C
SYP2114	450nsec	100mA	Plastic	0°C to 70°C
SYD2114L-1	150nsec	70mA	Cerdip	0°C to 70°C
SYP2114L-1	150nsec	70mA	Plastic	0°C to 70°C
SYD2114L-2	200nsec	70mA	Cerdip	0°C to 70°C
SYP2114L-2	200nsec	70mA	Plastic	0°C to 70°C
SYD2114L-3	300nsec	70mA	Cerdip	0°C to 70°C
SYP2114L-3	300nsec	70mA	Plastic	0°C to 70°C
SYD2114L	450nsec	70mA	Cerdip	0°C to 70°C
SYP2114L	450nsec	70mA	Plastic	0°C to 70°C

The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as improved protection against contamination.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	2114-1,-2 2114-3,2114 Min	2114-1,-2 2114-3,2114 Max	2114L-1,-2 2114L,2114L-3 Min	2114L-1,-2 2114L,2114L-3 Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	μA	V_{IN} = 0 to 5.25V
I_{LO}	I/O Leakage Current		10		10	μA	$\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		95		65	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		100		70	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

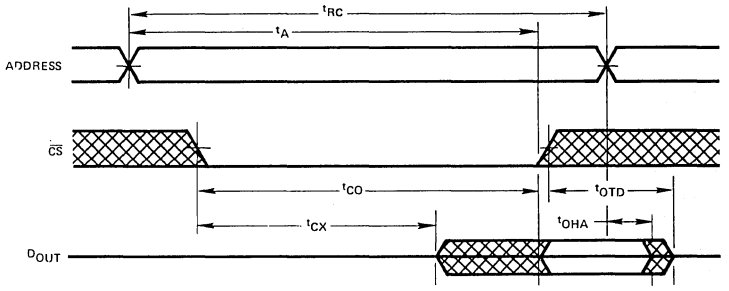
Symbol	Parameter	2114-1,2114L-1 Min.	2114-1,2114L-1 Max.	2114-2, 2114L-2 Min.	2114-2, 2114L-2 Max.	2114-3, 2114L-3 Min.	2114-3, 2114L-3 Max.	2114, 2114L Min.	2114, 2114L Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	150		200		300		450		nsec
t_A	Access Time		150		200		300		450	nsec
t_{CO}	Chip Select to Output Valid		70		70		100		120	nsec
t_{CX}	Chip Select to Output Enabled	20		20		20		20		nsec
t_{OTD}	Chip Deselect to Output Off	0	60	0	60	0	80	0	100	nsec
t_{OHA}	Output Hold From Address Change	50		50		50		50		nsec
Write Cycle										
t_{WC}	Write Cycle Time	150		200		300		450		nsec
t_{AW}	Address to Write Setup Time	0		0		0		0		nsec
t_W	Write Pulse Width	120		120		150		200		nsec
t_{WR}	Write Release Time	0		0		0		0		nsec
t_{OTW}	Write to Output Off	0	60	0	60	0	80	0	100	nsec
t_{DW}	Data to Write Overlap	120		120		150		200		nsec
t_{DH}	Data Hold	0		0		0		0		nsec

A.C. Test Conditions

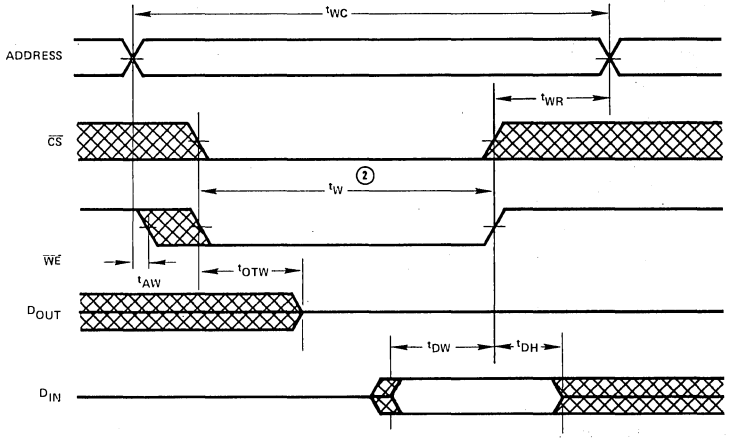
Input Pulse Levels . . . . . 0.8V to 2.0V
Input Rise and Fall Time . . . . . 10 n sec
Timing Measurement Levels: Input 1.5V
Output . . . . . 0.8 and 2.0V
Output Load . . . . . 1TTL Gate and 50pF

TIMING DIAGRAMS

Read Cycle ①



Write Cycle



NOTES:

① $\overline{WE}$ is high for a Read Cycle
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

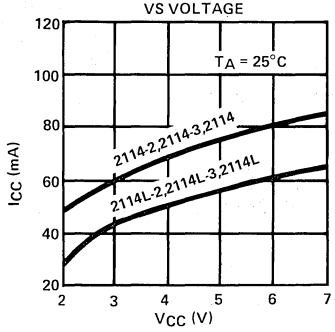
Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

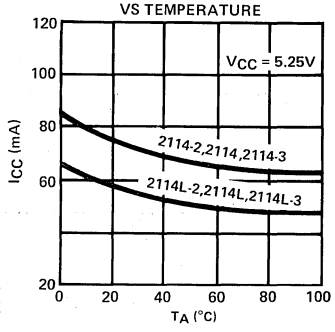
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

TYPICAL CHARACTERISTICS

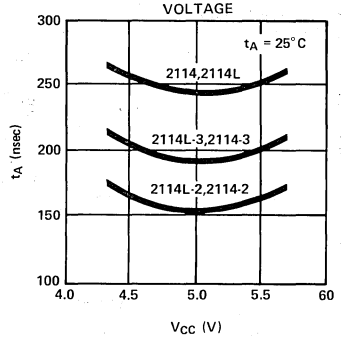
SUPPLY CURRENT VS VOLTAGE



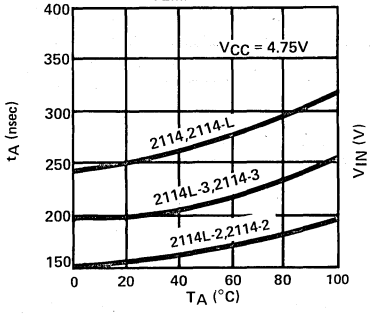
SUPPLY CURRENT VS TEMPERATURE



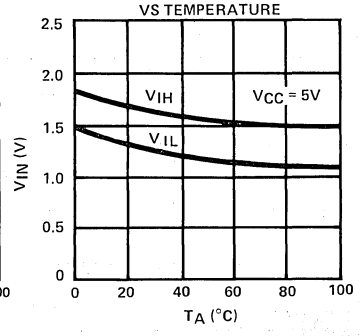
ACCESS TIME VS VOLTAGE



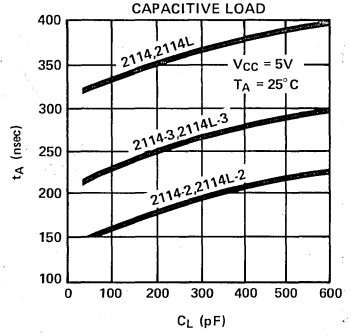
ACCESS TIME VS TEMPERATURE



INPUT VOLTAGE LIMITS VS TEMPERATURE

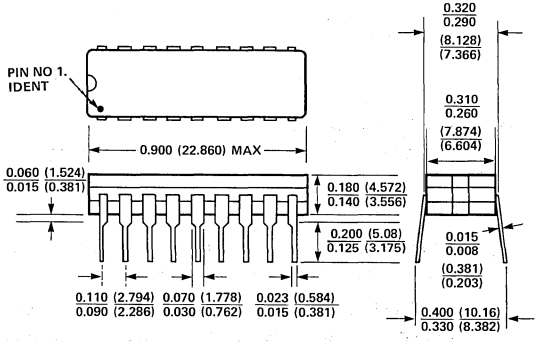


ACCESS TIME VS CAPACITIVE LOAD

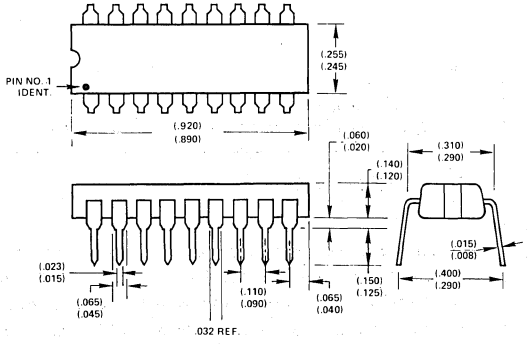


PACKAGE DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



1024 x 4 Static Random Access Memory Low Power Standby

SY2114LV

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

RAMs

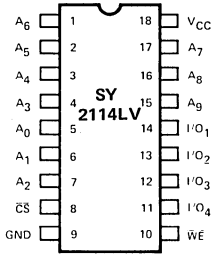
- 200 ns Maximum Access
- Low Power: 0.1 mW/Bit Operating
  .03 mW/Bit Standby
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single Supply: +5V Operating
  +2.5V Standby
- Totally TTL Compatible:
  All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114LV is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. These advanced processing techniques allow the SY2114LV to maintain memory with V_{CC} reduced to 2.5V. This reduces standby power by 60% and simplifies the design of battery back-up systems. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

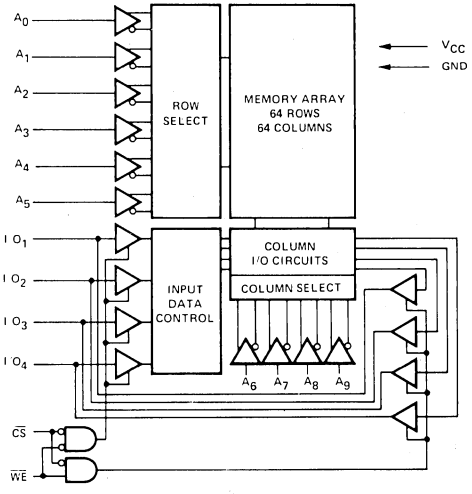
The SY2114LV is designed for memory applications where high performance, low power, large bit storage and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114LV is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as improved protection against contamination.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYD2114LV	Cerdip	450nsec	70mA	0° C to +70° C
SYP2114LV	Molded	450nsec	70mA	0° C to +70° C
SYD2114LV-3	Cerdip	300nsec	70mA	0° C to +70° C
SYP2114LV-3	Molded	300nsec	70mA	0° C to +70° C
SYD2114LV-2	Cerdip	200nsec	70mA	0° C to +70° C
SYP2114LV-2	Molded	200nsec	70mA	0° C to +70° C

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	2114LV-2, 2114LV-3, 2114LV Min	Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{IN} = 0 to 5.25V
I_{LO}	I/O Leakage Current		10	μA	$\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		65	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		70	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage	2.4	0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage		V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

Symbol	Parameter	2114LV-2 Min.	2114LV-2 Max.	2114LV-3 Min.	2114LV-3 Max.	2114LV Min.	2114LV Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	200		300		450		nsec
t_A	Access Time		200		300		450	nsec
t_{CO}	Chip Select to Output Valid		70		100		120	nsec
t_{CX}	Chip Select to Output Enabled	20		20		20		nsec
t_{OTD}	Chip Deselect to Output Off	0	60	0	80	0	100	nsec
t_{OHA}	Output Hold From Address Change	50		50		50		nsec
Write Cycle								
t_{WC}	Write Cycle Time	200		300		450		nsec
t_{AW}	Address to Write Setup Time	0		0		0		nsec
t_W	Write Pulse Width	120		150		200		nsec
t_{WR}	Write Release Time	0		0		0		nsec
t_{OTW}	Write to Output Off	0	60	0	80	0	100	nsec
t_{DW}	Data to Write Overlap	120		150		200		nsec
t_{DH}	Data Hold	0		0		0		nsec

A.C. Test Conditions

Input Pulse Levels . . . . . 0.8V to 2.0V
Input Rise and Fall Time . . . . . 10 n sec
Timing Measurement Levels: Input 1.5V
Output . . . . . 0.8 and 2.0V
Output Load . . . . . 1TTL Gate and 100pF

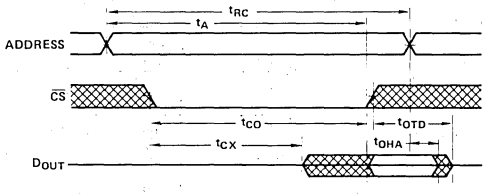
STANDBY CHARACTERISTICS

$T_A = 0°C$ to $70°C$

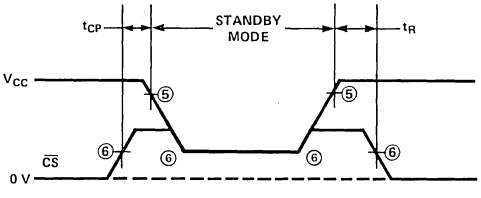
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	2.5		V	
V_{CSS}(2)	$\overline{CS}$ Bias in Standby	2.5		V	$2.5V \leqslant V_{PD} \leqslant V_{CC}$ Max.
I_{PD}	Standby Current Drain		50	mA	All Inputs = V_{PD} = 2.5V
t_{CP}	Chip Deselect to Standby Time	0		ns	
t_R	Standby Recovery Time	500		ns	

TIMING DIAGRAMS

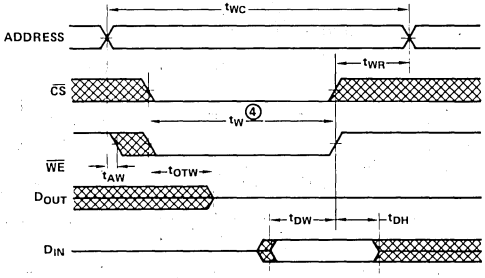
Read Cycle(3)



Standby Operation



Write Cycle



NOTES

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.5V, then $\overline{CS}$ must be held at 2.5V Min.
3. $\overline{WE}$ is high for a Read Cycle.
4. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
5. 4.75 Volts
6. 2.5 Volts

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

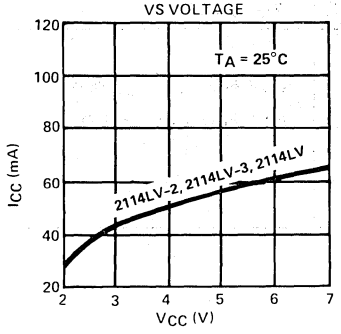
Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

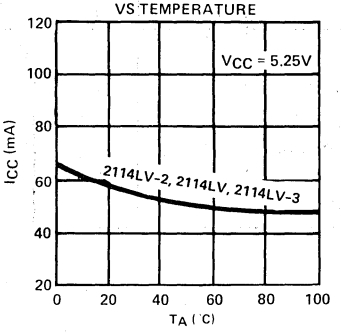
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

TYPICAL CHARACTERISTICS

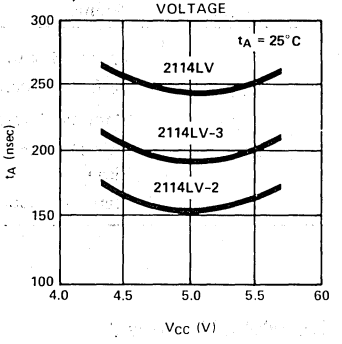
SUPPLY CURRENT VS VOLTAGE



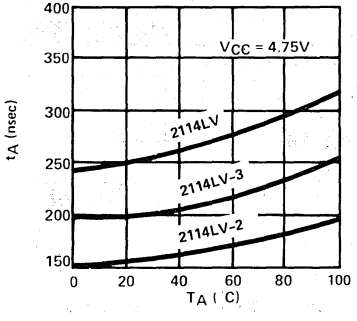
SUPPLY CURRENT VS TEMPERATURE



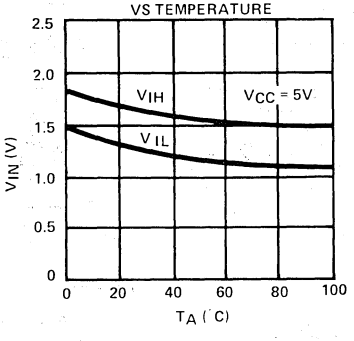
ACCESS TIME VS VOLTAGE



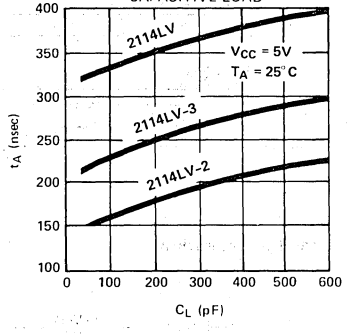
ACCESS TIME VS TEMPERATURE



INPUT VOLTAGE LIMITS VS TEMPERATURE

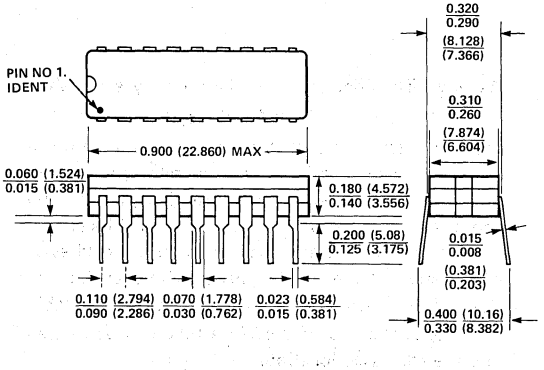


ACCESS TIME VS CAPACITIVE LOAD

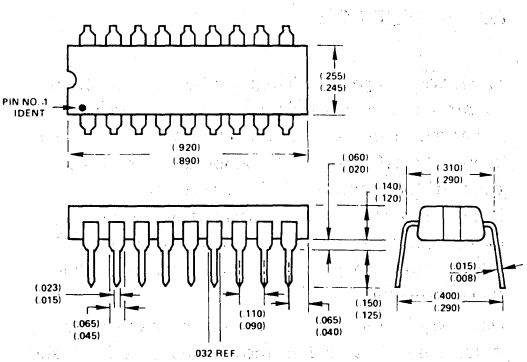


PACKAGE DIAGRAM

CERDIP PACKAGE



MOLDED PACKAGE



2048 x 8 Static Random Access Memory

SY2128

MEMORY PRODUCTS

PRELIMINARY

RAMs

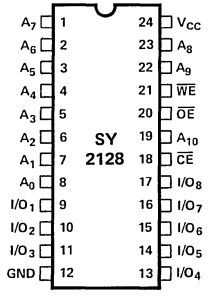
- 120nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (± 10%)
- Pin Compatible with 2716 16K EPROM
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- JEDEC Approved Pinout

The Synertek SY2128 is a 16,384 bit static Random Access Memory organized 2048 words by eight bits and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus.

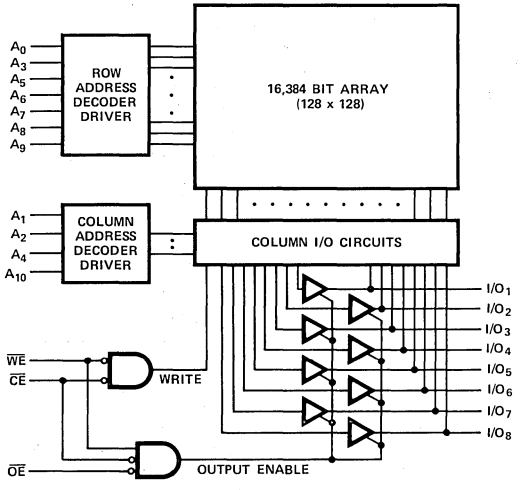
The SY2128 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings.

The SY2128 is configured in the JEDEC approved pinout for 24 pin byte organized memories and is pin compatible with 16K ROMs, EPROMs and EEPROMs. This offers the user the flexibility of being able to switch between RAM, ROM, EPROM, or EEPROM as his needs dictate with a minimum of board changes.

PIN CONFIGURATION



BLOCK DIAGRAM



1024 x 4 Static Random Access Memory

SY2142

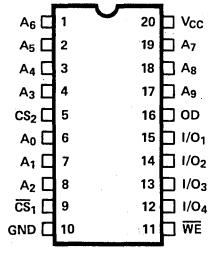
MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- 200ns Maximum Access
- Low Operating Power Dissipation 0.1mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400mv Noise Immunity
- High Density 20 Pin Package
- Two Chip Selects and Output Disable Functions Simplify Memory Expansion

The 2142 is a 4096-bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of bus oriented systems, and the outputs can drive 2 TTL loads.

PIN CONFIGURATION



ORDERING INFORMATION

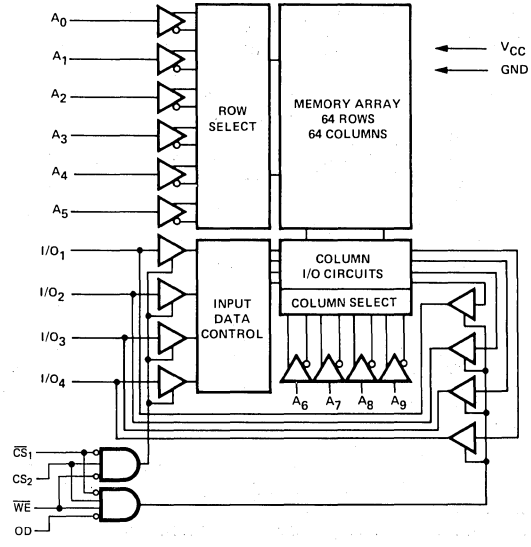
Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYD2142	Cerdip	450nsec	100mAmp	0°C to 70°C
SYP2142	Plastic	450nsec	100mAmp	0°C to 70°C
SYD2142-3	Cerdip	300nsec	100mAmp	0°C to 70°C
SYP2142-3	Plastic	300nsec	100mAmp	0°C to 70°C
SYD2142L	Cerdip	450nsec	70mAmp	0°C to 70°C
SYP2142L	Plastic	450nsec	70mAmp	0°C to 70°C
SYD2142L-3	Cerdip	300nsec	70mAmp	0°C to 70°C
SYP2142L-3	Plastic	300nsec	70mAmp	0°C to 70°C
SYD2142-2	Cerdip	200nsec	100mAmp	0°C to 70°C
SYP2142-2	Plastic	200nsec	100mAmp	0°C to 70°C
SYD2142L-2	Cerdip	200nsec	70mAmp	0°C to 70°C
SYP2142L-2	Plastic	200nsec	70mAmp	0°C to 70°C

The SY2142 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply.

Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided to simplify systems where memory expansion is implemented by OR-tying several 2142's. Also an Output Disable directly controls the output stages.

The SY2142 is packaged in a 20-pin DIP and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin with
Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	2142, 2142-2 2142-3 Min	2142, 2142-2 2142-3 Max	2142L,2142L-2 2142L-3 Min	2142L,2142L-2 2142L-3 Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	μA	$V_{IN} = 0$ to 5.25V
I_{LO}	I/O Leakage Current		10		10	μA	$\overline{CS} = 2.0V$, $V_{I/O} = 0.4V$ to V_{CC}
I_{CC1}	Power Supply Current		95		65	mA	$V_{CC} = 5.25V$, $I_{I/O} = 0$ mA, $T_A = 25°C$
I_{CC2}	Power Supply Current		100		70	mA	$V_{CC} = 5.25V$, $I_{I/O} = 0$ mA, $T_A = 0°C$
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	$I_{OL} = 3.2$ mA
V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	V	$I_{OH} = -1.0$ mA

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Unless Otherwise Specified)

Symbol	Parameter	2142-2,2142L-2 Min.	2142-2,2142L-2 Max.	2142-3,2142L-3 Min.	2142-3,2142L-3 Max.	2142,2142L Min.	2142,2142L Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{OD}	Output Enable to Output Valid		70		100		120	ns
t_{ODX}	Output Enable to Output Active	20		20		20		ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Disable	0	60	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	200		300		450		ns
t_{AW}	Address to Write Setup Time	0		0		0		ns
t_W	Write Pulse Width	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTD}	Output 3-state from Disable	0	60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns

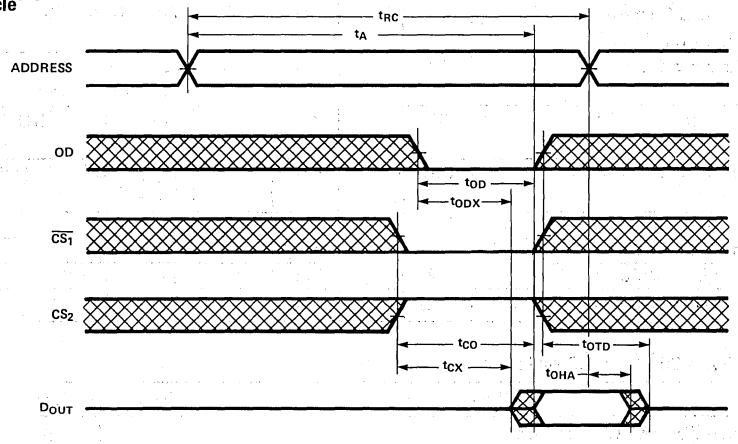
See following page for A.C. Test Conditions

A.C. Test Conditions

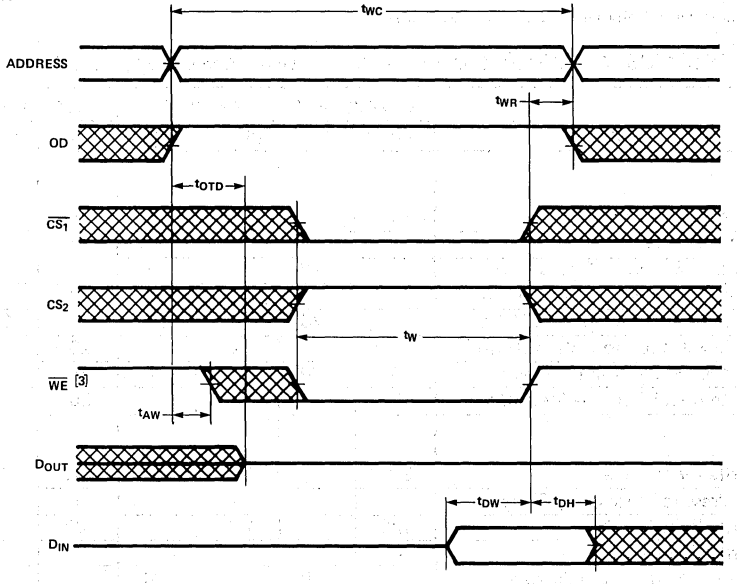
Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Time	10nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	1TTL Gate and 100pF

TIMING DIAGRAMS

Read Cycle[1]



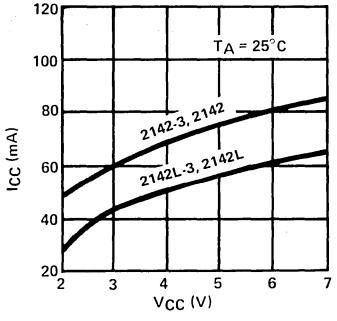
Write Cycle[2]



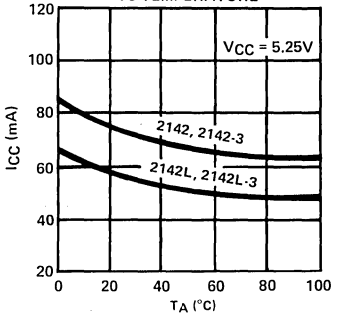
NOTES:
1. A Read occurs during the overlap of a low $\overline{CS_1}$, high CS_2 and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS_1}$, high CS_2 and a low $\overline{WE}$.
3. $\overline{WE}$ must be high during all address transitions.

TYPICAL CHARACTERISTICS

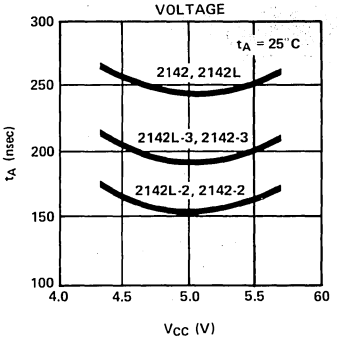
SUPPLY CURRENT VS VOLTAGE



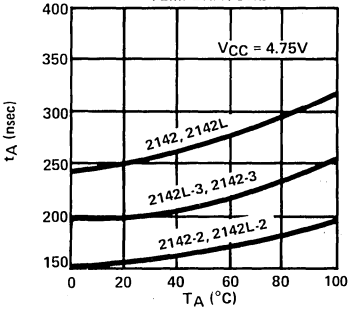
SUPPLY CURRENT VS TEMPERATURE



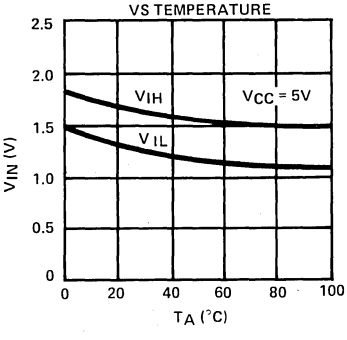
ACCESS TIME VS VOLTAGE



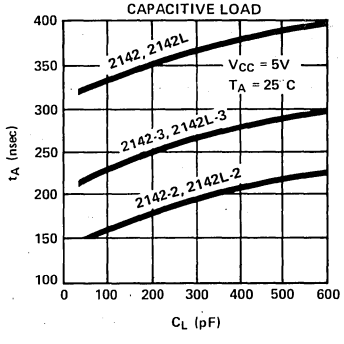
ACCESS TIME VS TEMPERATURE



INPUT VOLTAGE LIMITS VS TEMPERATURE

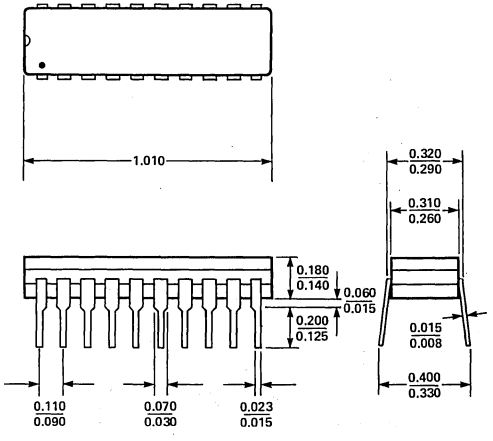


ACCESS TIME VS CAPACITIVE LOAD

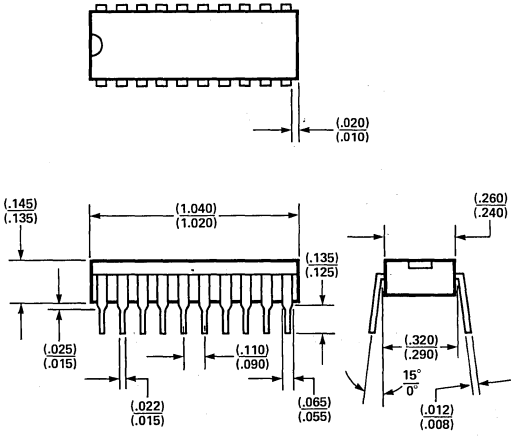


PACKAGE DIAGRAMS

20 PIN CERDIP



20 PIN PLASTIC



1024 x 4 Static Random Access Memory Low Power Standby

SY2142LV

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- 200 ns Maximum Access
- Low Power: 0.1 mW/Bit Operating
  .03 mW/Bit Standby
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single Supply: +5V Operating
  +2.5V Standby
- Totally TTL Compatible:
  All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package
- Two Chip Selects and Output Disable Functions Simplify Memory Expansion

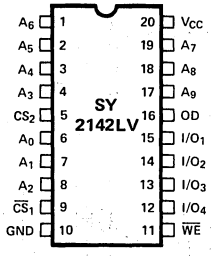
The SY2142LV is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. These advanced processing techniques allow the SY2142LV to maintain memory with V_{CC} reduced to 2.5V. This reduces standby power by 60% and simplifies the design of battery back-up systems. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

The SY2142LV is designed for memory applications where high performance, low power, large bit storage and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply.

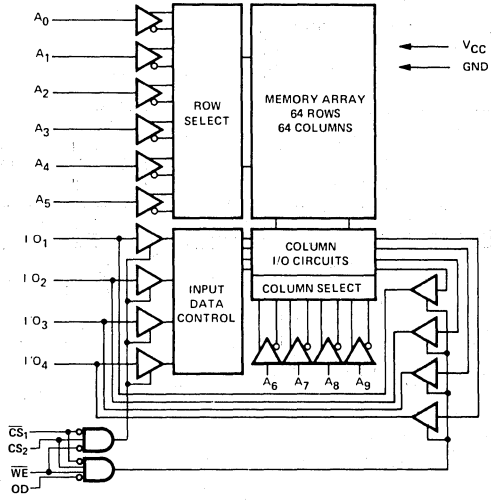
Two Chip Selects ($\overline{CS}_1$ and CS_2) are provided to simplify systems where memory expansion is implemented by OR-tying several 2142LVs. Also an Output Disable directly controls the output stages.

The SY2142LV is packaged in a 20-pin DIP and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology — a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYP2142LV	Plastic	450nsec	70mA	0°C to +70°C
SYP2142LV-3	Plastic	300nsec	70mA	0°C to +70°C
SYP2142LV-2	Plastic	200nsec	70mA	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7 V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ± 5% (Unless otherwise specified)

Symbol	Parameter	2142LV-2 2142LV-3, 2142LV Min	Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10	μA	V_{IN} = 0 to 5.25V
I_{LO}	I/O Leakage Current		10	μA	$\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		65	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		70	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage	2.4	0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage		V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

Symbol	Parameter	2142LV-2 Min.	Max.	2142LV-3 Min.	Max.	2142LV Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	200		300		450		nsec
t_A	Access Time		200		300		450	nsec
t_{OD}	Output Enable to Output Valid		70		100		120	nsec
t_{ODX}	Output Enable to Output Active	20		20		20		nsec
t_{CO}	Chip Select to Output Valid		70		100		120	nsec
t_{CX}	Chip Select to Output Enabled	20		20		20		nsec
t_{OTD}	Chip Deselect to Output Off	0	60	0	80	0	100	nsec
t_{OHA}	Output Hold From Address Change	50		50		50		nsec
Write Cycle								
t_{WC}	Write Cycle Time	200		300		450		nsec
t_{AW}	Address to Write Setup Time	0		0		0		nsec
t_W	Write Pulse Width	120		150		200		nsec
t_{WR}	Write Release Time	0		0		0		nsec
t_{OTW}	Write to Output Off	0	60	0	80	0	100	nsec
t_{DW}	Data to Write Overlap	120		150		200		nsec
t_{DH}	Data Hold	0		0		0		nsec

A.C. Test Conditions

Input Pulse Levels . . . . . 0.8V to 2.0V
Input Rise and Fall Time . . . . . 10 n sec

Timing Measurement Levels: Input 1.5V
Output . . . 0.8 and 2.0V
Output Load . . . . . 1TTL Gate and 100pF

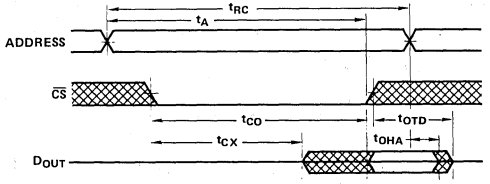
STANDBY CHARACTERISTICS

T_A = 0°C to 70°C

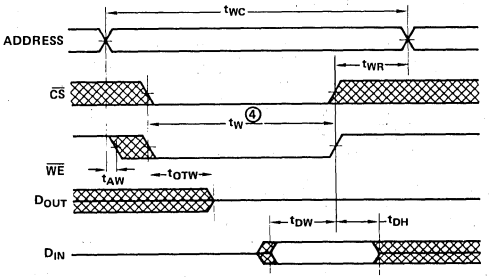
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	2.5		V	
V_{CSS}(2)	$\overline{CS}$ Bias in Standby	2.5		V	$2.5V \leqslant V_{PD} \leqslant V_{CC}$ Max.
I_{PD}	Standby Current Drain		50	mA	All Inputs = V_{PD} = 2.5V
t_{CP}	Chip Deselect to Standby Time	0		ns	
t_R	Standby Recovery Time	500		ns	

TIMING DIAGRAMS

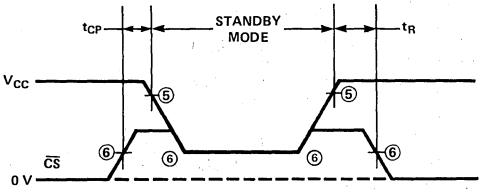
Read Cycle (3)



Write Cycle



Standby Operation



NOTES

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.5V, then $\overline{CS}$ must be held at 2.5V Min.
3. $\overline{WE}$ is high for a Read Cycle.
4. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
5. 4.75 Volts
6. 2.5 Volts

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

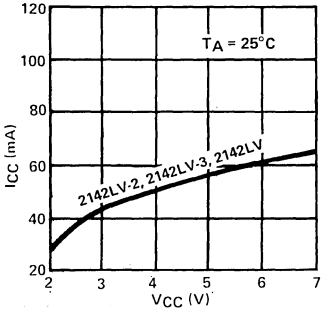
Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

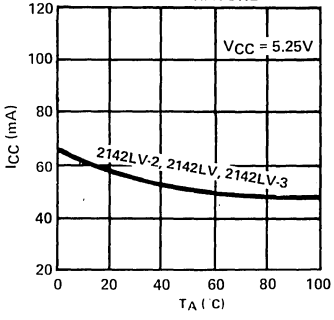
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

TYPICAL CHARACTERISTICS

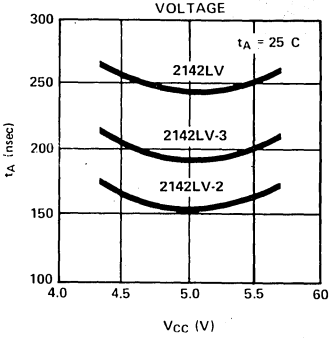
SUPPLY CURRENT VS VOLTAGE



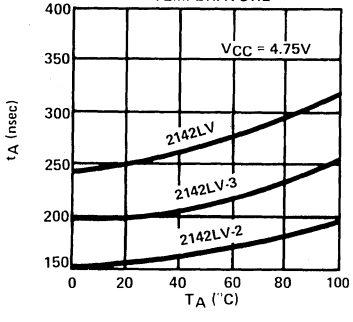
SUPPLY CURRENT VS TEMPERATURE



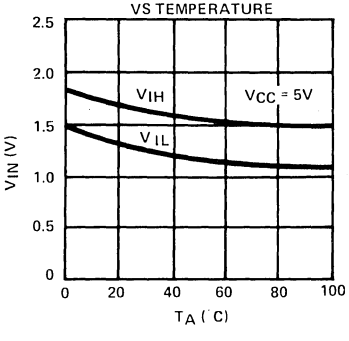
ACCESS TIME VS VOLTAGE



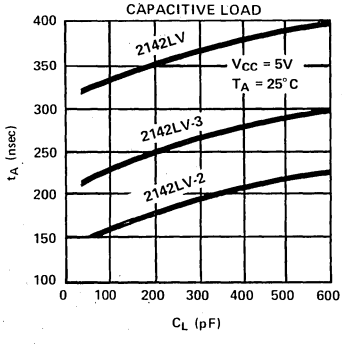
ACCESS TIME VS TEMPERATURE



INPUT VOLTAGE LIMITS VS TEMPERATURE

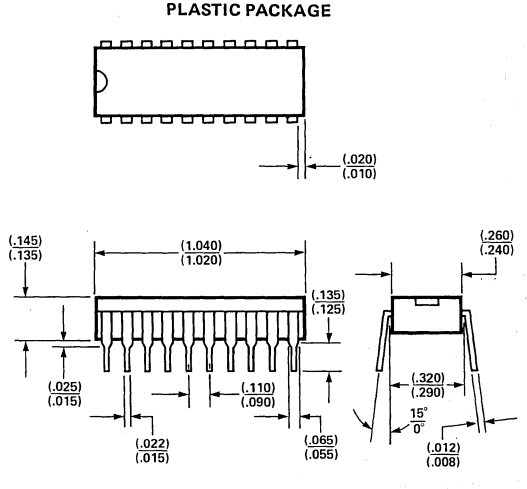


ACCESS TIME VS CAPACITIVE LOAD



PACKAGE DIAGRAM

PLASTIC PACKAGE



4096 x 1 Static Random Access Memory

SY2147

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

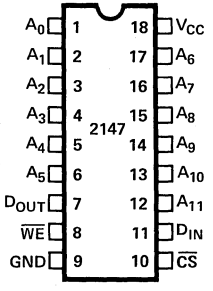
- 55 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CS}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SY2147 is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

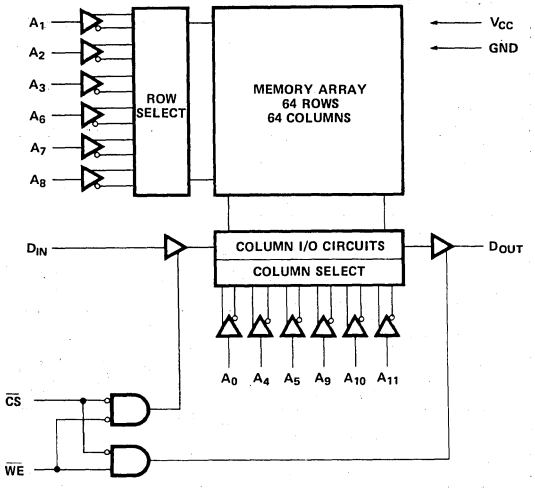
The SY2147 offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select ($\overline{CS}$) goes high, thus de-selecting the SY2147, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remain high. This unique feature provides system level power savings as much as 80%.

The SY2147 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYC2147-3	55ns	180mA	30mA	Ceramic
SYD2147-3	55ns	180mA	30mA	Cerdip
SYC2147	70ns	160mA	20mA	Ceramic
SYD2147	70ns	160mA	20mA	Cerdip
SYC2147L	70ns	140mA	10mA	Ceramic
SYD2147L	70ns	140mA	10mA	Cerdip
SYC2147-6	85ns	160mA	20mA	Ceramic
SYD2147-6	85ns	160mA	20mA	Cerdip

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature . . . . . -65°C to 150°C
Voltage on Any Pin with
Respect to Ground . . . . . -3.5V to +7V
Power Dissipation 1.2W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 8)

Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147, 2147-6 Min.	2147, 2147-6 Max.	2147L Min.	2147L Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		50		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		170		150		135	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}
			180		160		140	mA	T_A = 0°C; Outputs Open
I_{SB}	Standby Current		30		20		10	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
I_{PO}	Peak Power-on Current (Note 9)		70		50		30	mA	V_{CC} = Gnd to V_{CC} Min $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		2.4		2.4		V	I_{OH} = -4.0mA
I_{OS}	Output Short Circuit Current (Note 10)	-120	120	-120	120	-120	120	mA	V_{OUT} = GND to V_{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		6	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 8)

READ CYCLE

Symbol	Parameter	2147-3 Min.	2147-3 Max.	2147, 2147L Min.	2147, 2147L Max.	2147-6 Min.	2147-6 Max.	Unit	Conditions
t_{RC}	Read Cycle Time	55		70		85		ns	
t_{AA}	Address Access Time		55		70		85	ns	
t_{ACS1}	Chip Select Access Time		55		70		85	ns	Note 1
t_{ACS2}	Chip Select Access Time		65		80		85	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	10		10		10		ns	Note 7
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	40	0	40	ns	Note 7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

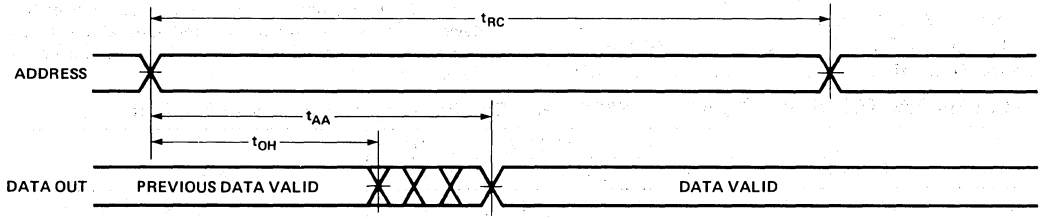
WRITE CYCLE

t_{WC}	Write Cycle Time	55		70		85		ns	
t_{CW}	Chip Selection to End of Write	45		55		65		ns	
t_{AW}	Address Valid to End of Write	45		55		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		45		ns	
t_{WR}	Write Recovery Time	10		15		20		ns	
t_{DW}	Data Valid to End of Write	25		30		30		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	30	0	35	0	40	ns	Note 7
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 7

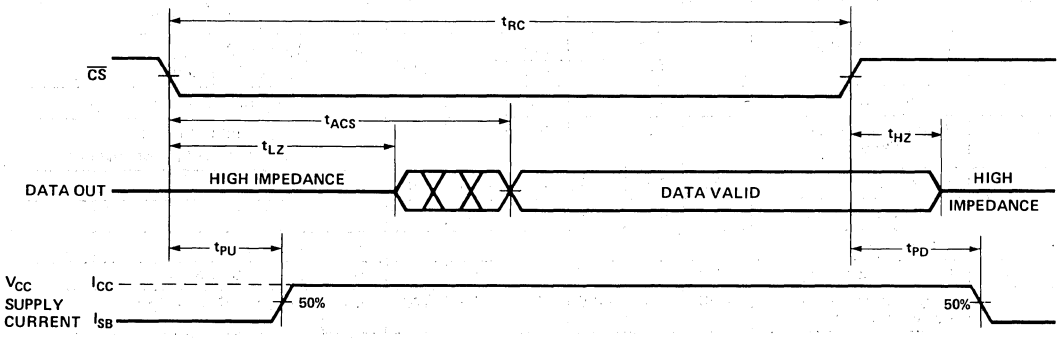
(See following page for notes)

TIMING DIAGRAMS

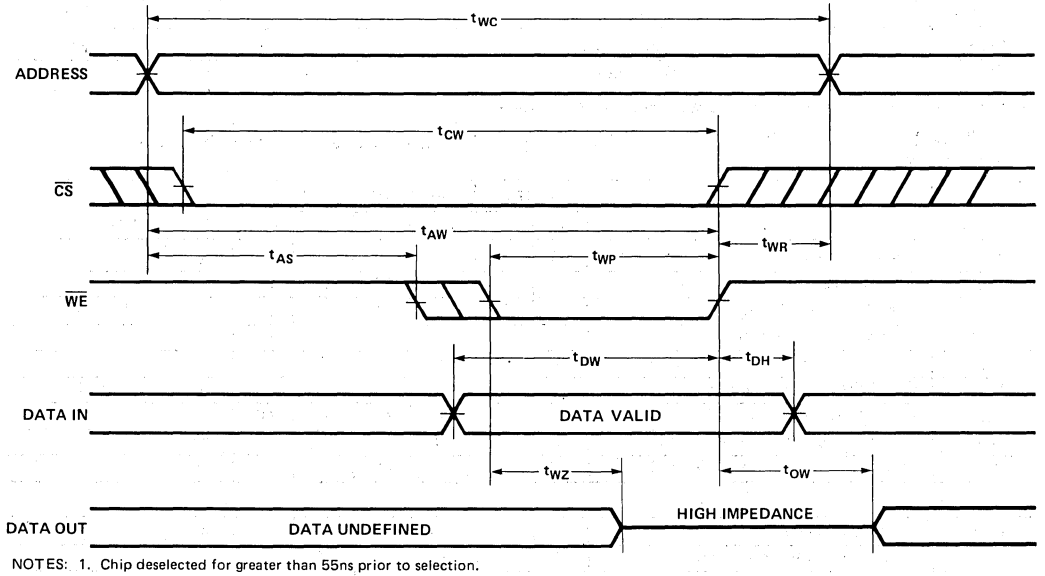
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)

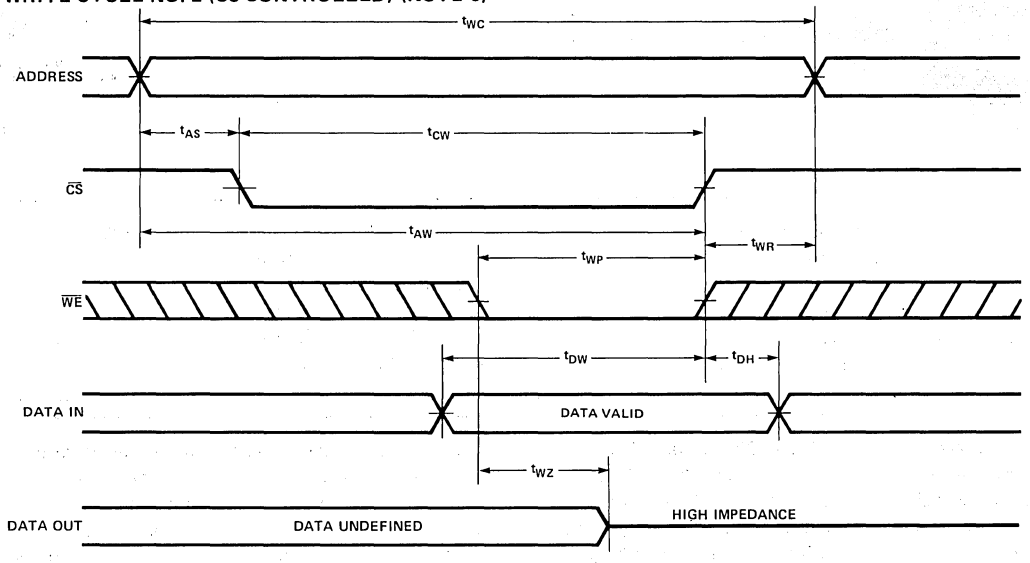


WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



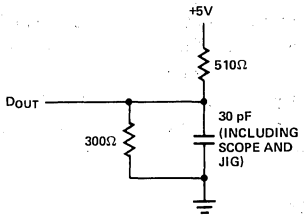
NOTES:
1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
6. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
7. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.
10. Duration not to exceed one minute.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (NOTE 6)

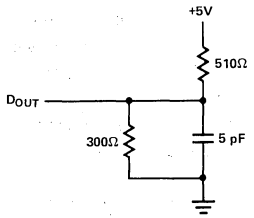


A.C. TEST CONDITIONS

INPUT PULSE LEVELS	GND TO 3.5 VOLTS
INPUT RISE AND FALL TIMES	10 nsec
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1.5 VOLTS
OUTPUT LOAD	SEE LOAD A.



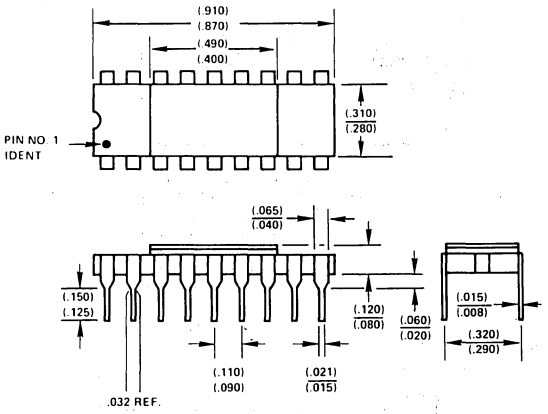
LOAD A.



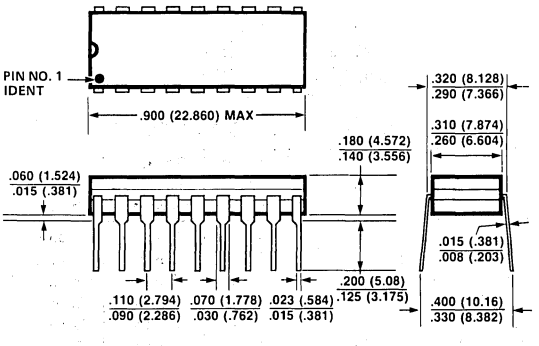
LOAD B.

PACKAGE DIAGRAMS

CERAMIC PACKAGE



CERDIP PACKAGE



4096 x 1 Static Random Access Memory

SY2147H

MEMORY PRODUCTS

PRELIMINARY

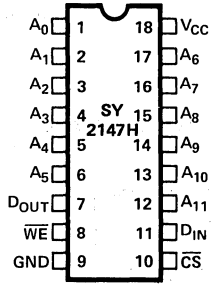
- 35–70 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CS}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2147
- Direct Performance Upgrade For SY2147
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SY2147H is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

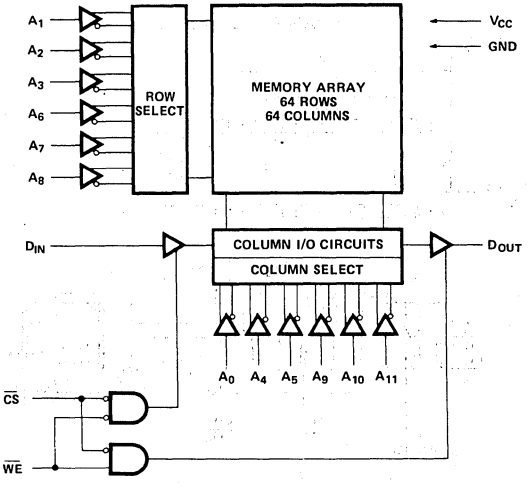
The SY2147H offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select ($\overline{CS}$) goes high, thus deselecting the SY2147H, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remain high. This unique feature provides system level power savings as much as 80%.

The SY2147H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Operating Current (Max)	Standby Package (Max)	Type
SYC2147H-1	35ns	180mA	30mA	Ceramic
SYD2147H-1	35ns	180mA	30mA	Cerdip
SYC2147H-2	45ns	180mA	30mA	Ceramic
SYD2147H-2	45ns	180mA	30mA	Cerdip
SYC2147H-3	55ns	180mA	30mA	Ceramic
SYD2147H-3	55ns	180mA	30mA	Cerdip
SYC2147HL-3	55ns	125mA	15mA	Ceramic
SYD2147HL-3	55ns	125mA	15mA	Cerdip
SYC2147H	70ns	160mA	20mA	Ceramic
SYD2147H	70ns	160mA	20mA	Cerdip
SYC2147HL	70ns	140mA	10mA	Ceramic
SYD2147HL	70ns	140mA	10mA	Cerdip

Military 4096 x 1 Static Random Access Memory

Extended Temperature Range (-55° C to +125° C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYM2147

MEMORY PRODUCTS

PRELIMINARY

RAMs

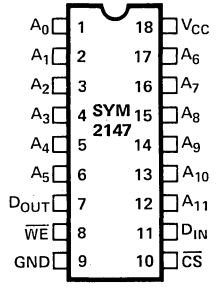
- 70 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CS}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SYM2147 is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

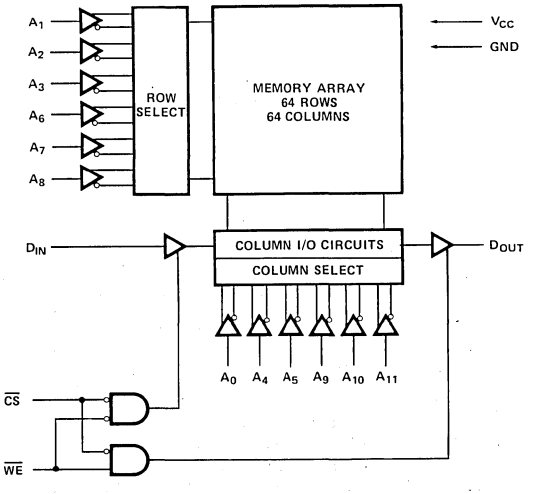
The SYM2147 offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select ($\overline{CS}$) goes high, thus de-selecting the SYM2147, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remains high. This unique feature provides system level power savings as much as 80%.

The SYM2147 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYMC2147	70ns	180mA	30mA	Ceramic
SYMD2147	70ns	180mA	30mA	Cerdip
SYMF2147	70ns	180mA	30mA	Flatpak
SYMC2147-6	85ns	180mA	30mA	Ceramic
SYMD2147-6	85ns	180mA	30mA	Cerdip
SYMF2147-6	85ns	180mA	30mA	Flatpak

1024 x 4 Static Random Access Memory

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SY2148H

MEMORY PRODUCTS

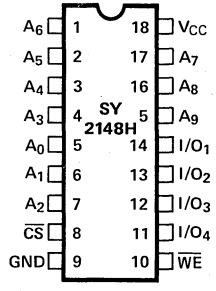
- 35-70 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CS}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2148
- Performance Upgrade for SY2148
- Industry Standard 2114 Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SY2148H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

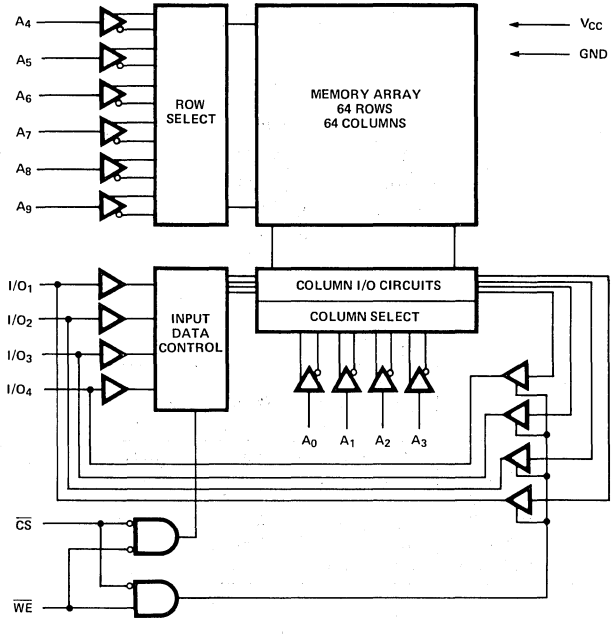
The SY2148H offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select ($\overline{CS}$) goes high, thus de-selecting the SY2148H, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remains high. This unique feature provides system level power savings as much as 85%.

The SY2148H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYC2148H	70ns	150mA	30mA	Ceramic
SYD2148H	70ns	150mA	30mA	Cerdip
SYC2148H-2	45ns	150mA	30mA	Ceramic
SYD2148H-2	45ns	150mA	30mA	Cerdip
SYC2148H-3	55ns	150mA	30mA	Ceramic
SYD2148H-3	55ns	150mA	30mA	Cerdip
SYC2148HL	70ns	125mA	20mA	Ceramic
SYD2148HL	70ns	125mA	20mA	Cerdip
SYC2148HL-3	55ns	125mA	20mA	Ceramic
SYD2148HL-3	55ns	125mA	20mA	Cerdip

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature . . . . . -65°C to 150°C
Voltage on Any Pin with
Respect to Ground . . . . . -3.5V to +7V
Power Dissipation 1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (note 8)

Symbol	Parameter	2148H/H-2/H-3 Min.	2148H/H-2/H-3 Max.	2148HL/HL-3 Min.	2148HL/HL-3 Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		140		115	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
			150		125	mA	T_A = 0°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		30		20	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
I_{PO}	Peak Power-on Current Note 9		50		30	mA	V_{CC} = Gnd to V_{CC} Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.1	6.0	2.1	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = -4mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (note 8)

READ CYCLE

Symbol	Parameter	2148H-2 Min.	2148H-2 Max.	2148H-3/HL-3 Min.	2148H-3/HL-3 Max.	2148H/HL Min.	2148H/HL Max.	Unit	Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS1}	Chip Select Access Time		45		55		70	ns	Note 1
t_{ACS2}	Chip Select Access Time		55		60		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	20		20		20		ns	Note 7
t_{HZ}	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns	Note 7
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		30		30		30	ns	

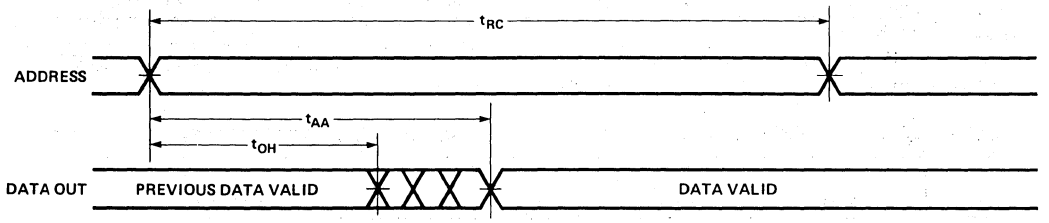
WRITE CYCLE

t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 7
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 7

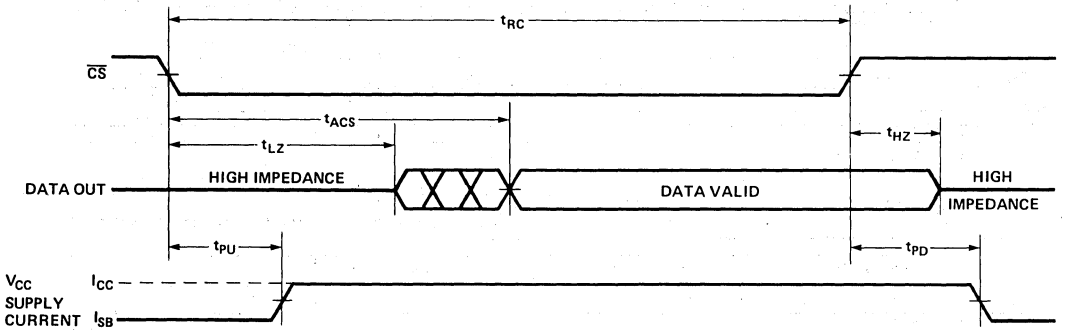
(See following page for notes)

TIMING DIAGRAMS

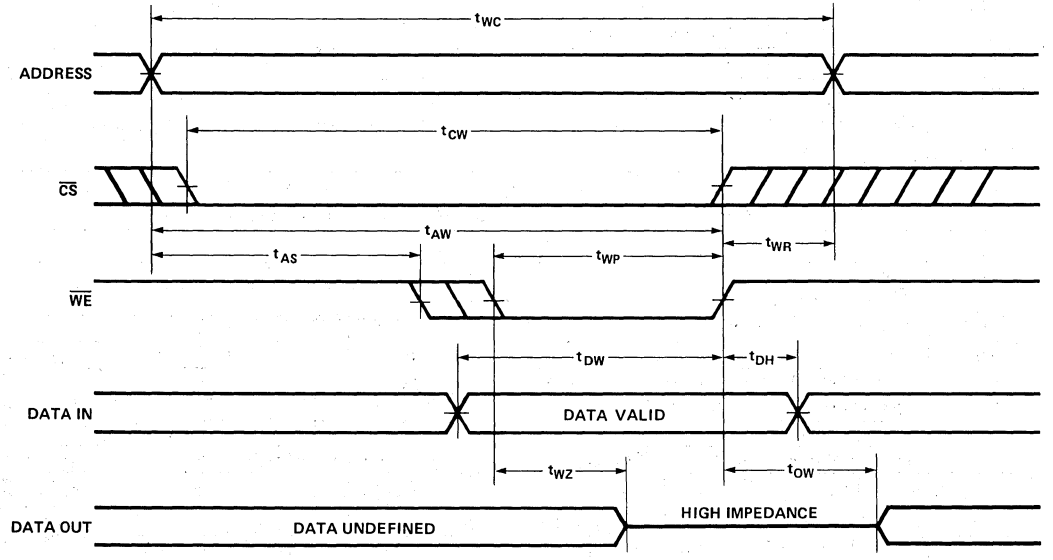
READ CYCLE NO. 1 (NOTES 3 AND 4)



READ CYCLE NO. 2 (NOTES 3 AND 5)

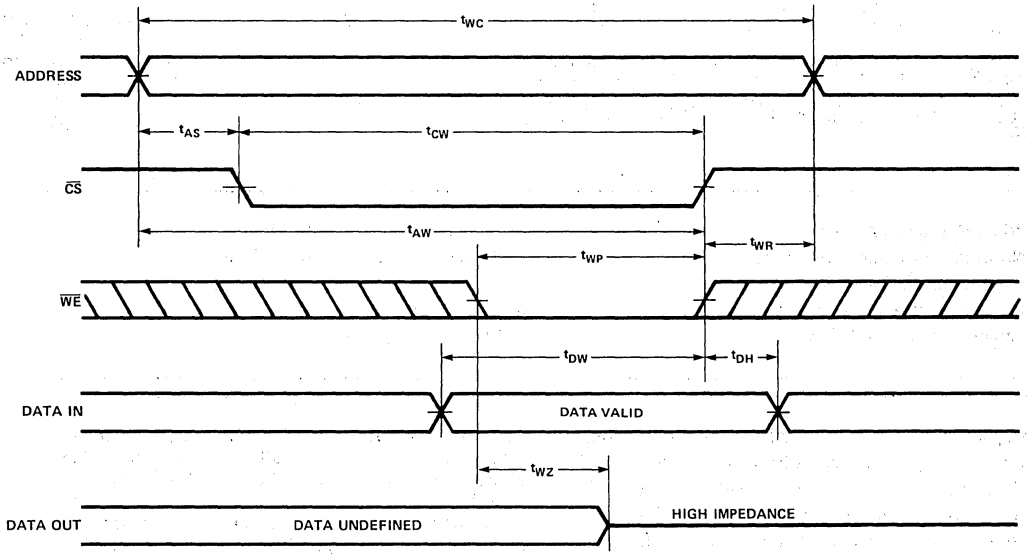


WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (NOTE 6)



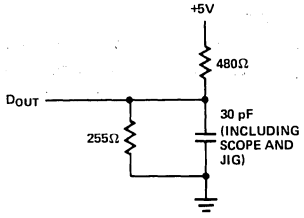
NOTES:
1. Chip deselected for greater than 55ns prior to selection.
2. Chip deselected for a finite time that is less than 55ns prior to selection. (If the deselect time is 0ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
6. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
7. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
8. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
9. A pullup resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected: otherwise, power-on current approaches I_{CC} active.

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (NOTE 6)

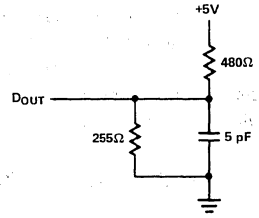


A.C. TEST CONDITIONS

INPUT PULSE LEVELS	GND TO 3.0 VOLTS
INPUT RISE AND FALL TIMES	10 nsec
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1.5 VOLTS
OUTPUT LOAD	SEE LOAD A.



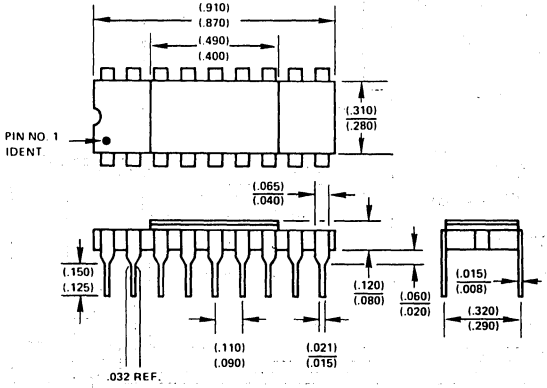
LOAD A.



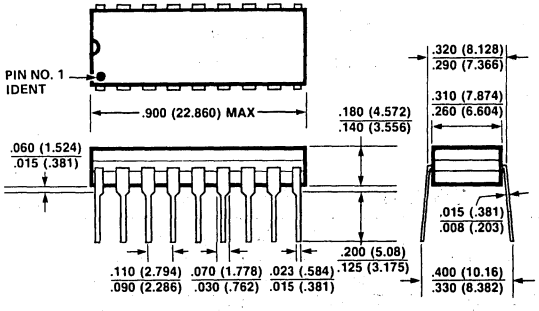
LOAD B.

PACKAGE DIAGRAMS

CERAMIC PACKAGE



CERDIP PACKAGE



Military 1024 x 4 Static Random Access Memory

Extended Temperature Range (-55°C to +125°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYM2148

MEMORY PRODUCTS

PRELIMINARY

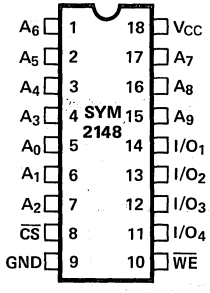
- 70 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CS}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Industry Standard 2114 Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

The Synertek SYM2148 is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

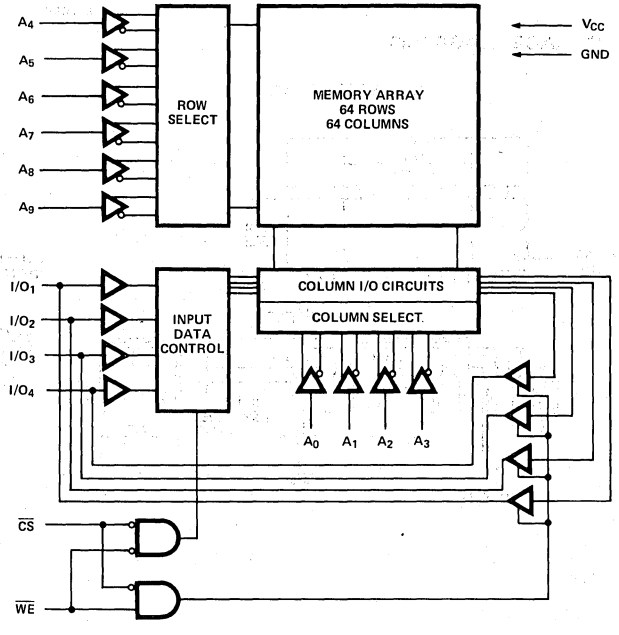
The SYM2148 offers an automatic power down feature. Power down is controlled by the Chip Select input. When Chip Select ($\overline{CS}$) goes high, thus deselecting the SYM2148, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remains high. This unique feature provides system level power savings as much as 85%.

The SYM2148 is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)	Package Type
SYMC2148	70ns	150mA	30mA	Ceramic
SYMD2148	70ns	150mA	30mA	Cerdip
SYMF2148	70ns	150mA	30mA	Flatpak
SYMC2148-6	85ns	150mA	30mA	Ceramic
SYMD2148-6	85ns	150mA	30mA	Cerdip
SYMF2148-6	85ns	150mA	30mA	Flatpak

1024 x 4 Static Random Access Memory

SY2149H

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

RAMs

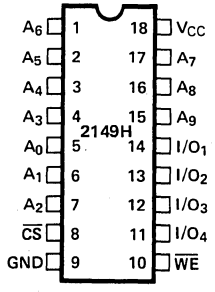
- 45 ns Maximum Address Access
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access Time: 20ns Max.
- Identical Cycle and Access Times
- Single +5V Supply
- Industry Standard 2114 Pinout
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Outputs
- High Density 18-Pin Package
- Three-State Output

The Synertek SY2149H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

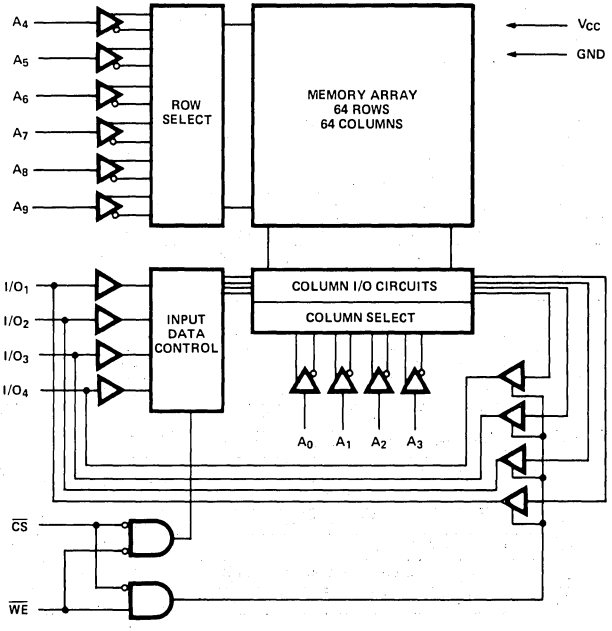
The SY2149H offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The SY2149H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Supply Current (Max)	Package Type
SYC2149H-2	45nsec	150mA	Ceramic
SYD2149H-2	45nsec	150mA	Cerdip
SYC2149H-3	55nsec	150mA	Ceramic
SYD2149H-3	55nsec	150mA	Cerdip
SYC2149HL-3	55nsec	125mA	Ceramic
SYD2149HL-3	55nsec	125mA	Cerdip
SYC2149H	70nsec	150mA	Ceramic
SYD2149H	70nsec	150mA	Cerdip
SYC2149HL	70nsec	125mA	Ceramic
SYD2149HL	70nsec	125mA	Cerdip

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . -10°C to 85°C
Storage Temperature . . . . . -65°C to 150°C
Voltage on Any Pin with
Respect to Ground . . . . . -3.5V to +7V
Power Dissipation 1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6)

Symbol	Parameter	2149HL-3, 2149HL Min.	2149HL-3, 2149HL Max.	2149H-2, 2149H-3, 2149H Min.	2149H-2, 2149H-3, 2149H Max.	Unit	Conditions
I_{LI}	Input Load Current (All input pins).		10		10	µA	V_{CC} = Max, V_{IN} = Gnd to V_{CC}
I_{LO}	Output Leakage Current		50		50	µA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = Gnd to 4.5V
I_{CC}	Power Supply Current		115		140	mA	T_A = 25°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
			125		150	mA	T_A = 0°C; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
V_{IL}	Input Low Voltage	-3.0	0.8	-3.0	0.8	V	
V_{IH}	Input High Voltage	2.0	6.0	2.0	6.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = -4.0 mA
I_{OS}	Output Short Circuit Current		±200		±200	mA	V_{OUT} = GND to V_{CC}

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ.	Max.	Unit
C_{OUT}	Output Capacitance		7	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Unless otherwise specified) (Note 6)

READ CYCLE

Symbol	Parameter	2149H-2 Min.	2149H-2 Max.	2149HL-3 2149H-3 Min.	2149HL-3 2149H-3 Max.	2149HL 2149H Min.	2149HL 2149H Max.	Unit	Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	
t_{AA}	Address Access Time		45		55		70	ns	
t_{ACS}	Chip Select Access Time		20		25		30	ns	
t_{OH}	Output Hold from Address Change	5		5		5		ns	
t_{LZ}	Chip Selection to Output in Low Z	5		5		5		ns	Note 5
t_{HZ}	Chip Deselectio to Output in High Z	0	15	0	15	0	15	ns	Note 5

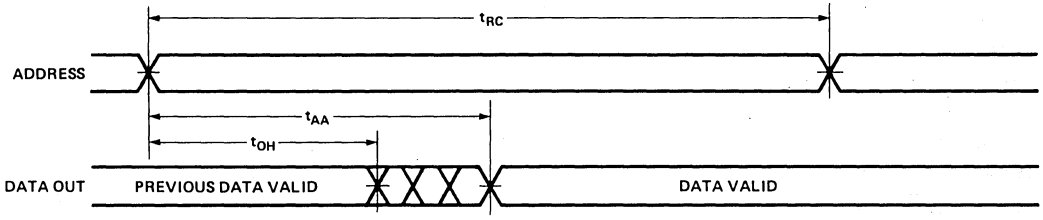
WRITE CYCLE

t_{WC}	Write Cycle Time	45		55		70		ns	
t_{CW}	Chip Selection to End of Write	40		50		65		ns	
t_{AW}	Address Valid to End of Write	40		50		65		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{WP}	Write Pulse Width	35		40		50		ns	
t_{WR}	Write Recovery Time	5		5		5		ns	
t_{DW}	Data Valid to End of Write	20		20		25		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	15	0	20	0	25	ns	Note 5
t_{OW}	Output Active from End of Write	0		0		0		ns	Note 5

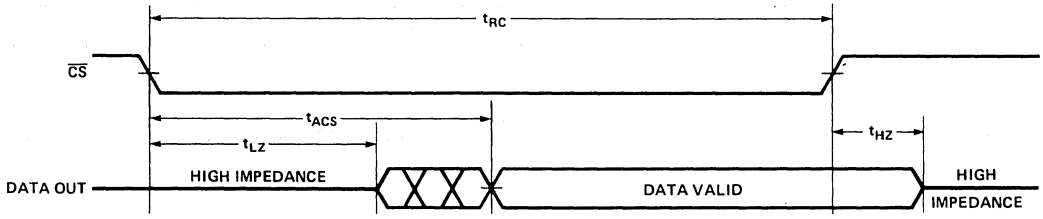
(See following page for notes)

TIMING DIAGRAMS

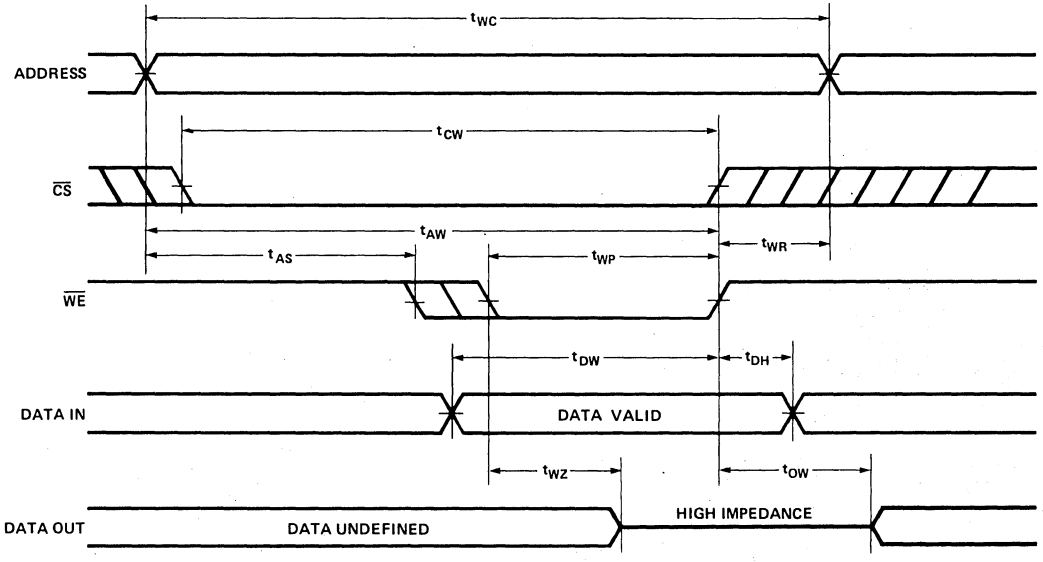
READ CYCLE NO. 1 (Notes 1 and 2)



READ CYCLE NO. 2 (Notes 1 and 3)

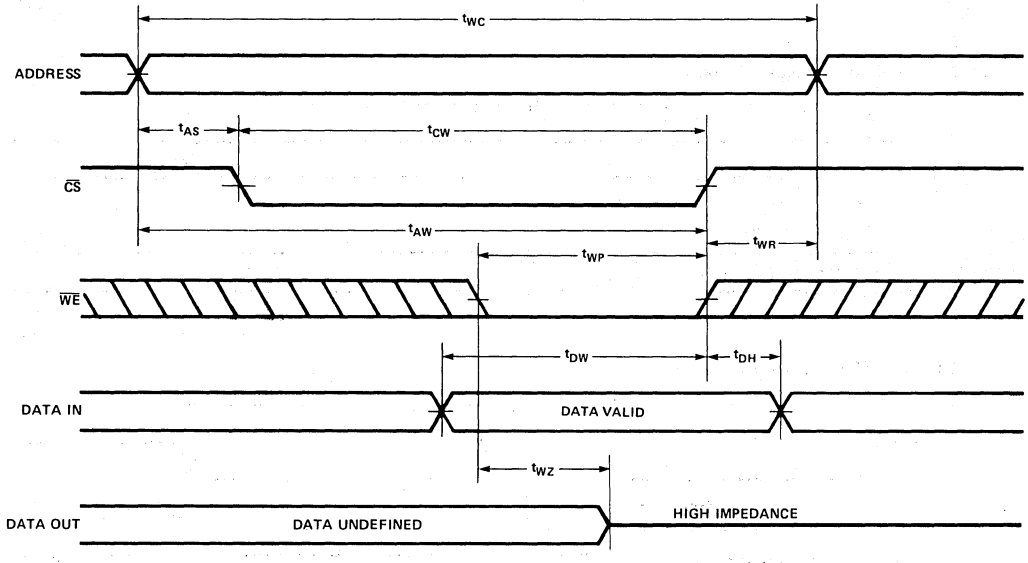


WRITE CYCLE NO. 1 ($\overline{WE}$ controlled) (Note 4)



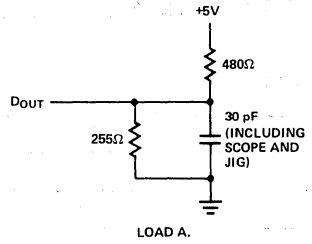
NOTES:
1. $\overline{WE}$ is high for Read Cycles.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Addresses valid.
4. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
5. Transition is measured ±500mV from low or high impedance voltage with load B. This parameter is sampled and not 100% tested.
6. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

WRITE CYCLE NO. 2 ($\overline{CS}$ controlled) (Note 4)

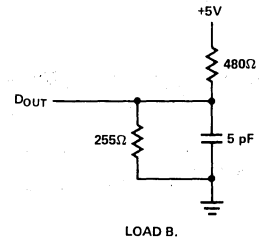


A.C. TEST CONDITIONS

INPUT PULSE LEVELS	GND TO 3.0 VOLTS
INPUT RISE AND FALL TIMES	5 nsec
INPUT AND OUTPUT TIMING REFERENCE LEVELS	1.5 VOLTS
OUTPUT LOAD	SEE LOAD A.



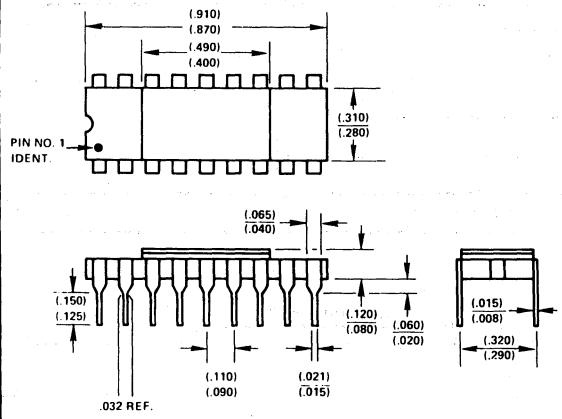
LOAD A.



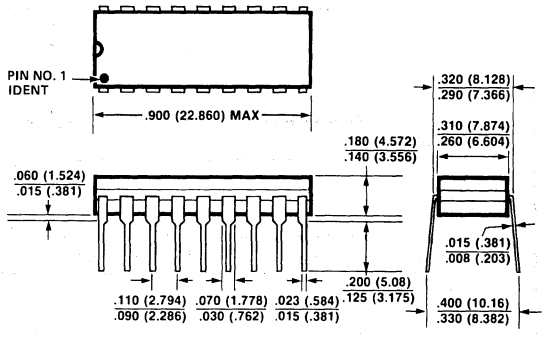
LOAD B.

PACKAGE DIAGRAMS

CERAMIC PACKAGE



CERDIP PACKAGE



Military 1024 x 4 Static Random Access Memory

Extended Temperature Range (-55°C to +125°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYM2149H

MEMORY PRODUCTS

PRELIMINARY

RAMs

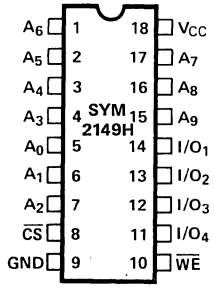
- 55 ns Maximum Address Access
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access Time: 25 ns Max.
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Industry Standard 2114 Pinout
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Outputs
- High Density 18-Pin Package
- Three-State Output

The Synertek SYM2149H is a 4096-Bit Static Random Access Memory organized 1024 words by 4 bits and is fabricated using Synertek's new N-Channel Silicon-Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

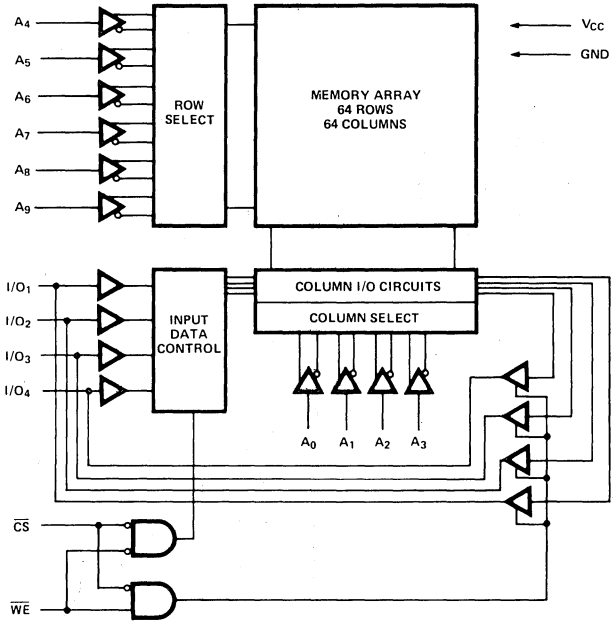
The SYM2149H offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The SYM2149H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time (Max)	Supply Current (Max)	Package Type
SYMC2149H-3	55 nsec	150mA	Ceramic
SYMD2149H-3	55 nsec	150mA	Cerdip
SYMC2149H	70 nsec	150mA	Ceramic
SYMD2149H	70 nsec	150mA	Cerdip

Read Only Memories

ROM Selector Guide

Commercial: T_A = 0°C to +70°C

Part No.	Organization	Access Time Max. (ns)	Supply Current Max. (mA)		Power Supply (Volts)	No. of Pins	Pin Compatible EPROM/PROM	Page
			Operating	Standby				
SY3308	1024 x 8	70	120	—	+5	24	82S181	2-32
SY2316A	2048 x 8	550	98	—	+5	24	—	2-3
SY2316B	2048 x 8	450	98	—	+5	24	2716	2-3
SY2316B-2	2048 x 8	200	98	—	+5	24	2716	2-7
SY2316B-3	2048 x 8	300	98	—	+5	24	2716	2-11
SY3316	2048 x 8	80	120	—	+5	24	82S191	2-36
SY3316A	2048 x 8	80	120	20	+5	24	82S191	2-36
SY2332	4096 x 8	450	100	—	+5	24	TMS2532	2-15
SY2332-3	4096 x 8	300	100	—	+5	24	TMS2532	2-19
SY2333	4096 x 8	450	100	—	+5	24	2732/A	2-15
SY2333-3	4096 x 8	300	100	—	+5	24	2732/A	2-19
SY2364	8192 x 8	450	100	—	+5	24	TMS2564	2-23
SY2364-2	8192 x 8	200	100	—	+5	24	TMS2564	2-23
SY2364-3	8192 x 8	300	100	—	+5	24	TMS2564	2-23
SY2364A	8192 x 8	450	100	12	+5	24	TMS2564	2-23
SY2364A-2	8192 x 8	200	100	12	+5	24	TMS2564	2-23
SY2364A-3	8192 x 8	300	100	12	+5	24	TMS2564	2-23
SY2365	8192 x 8	450	100	—	+5	28	2764	2-27
SY2365-2	8192 x 8	200	100	—	+5	28	2764	2-27
SY2365-3	8192 x 8	300	100	—	+5	28	2764	2-27
SY2365A	8192 x 8	450	100	12	+5	28	2764	2-27
SY2365A-2	8192 x 8	200	100	12	+5	28	2764	2-27
SY2365A-3	8192 x 8	300	100	12	+5	28	2764	2-27
SY23128[1]	16,384 x 8	200	100	10	+5	28	—	2-31

Military: -55°C to +125°C

SYM3316[1]	2048 x 8	100	150	—	+5	24	82S191	2-40
SYM3316A[1]	2048 x 8	100	150	30	+5	24	82S191	2-40

Note 1. To Be Announced.

2048 x 8 Static Read Only Memory

SY2316A/B

SYNERTEK
A SUBSIDIARY OF HONEYWELL

MEMORY PRODUCTS

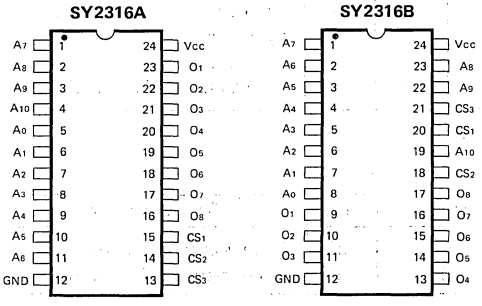
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time–550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A – Replacement for Intel 2316A
- SY2316B – Pin Compatible with 2716 EPROM
  – Replacement for Two 2708s

The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

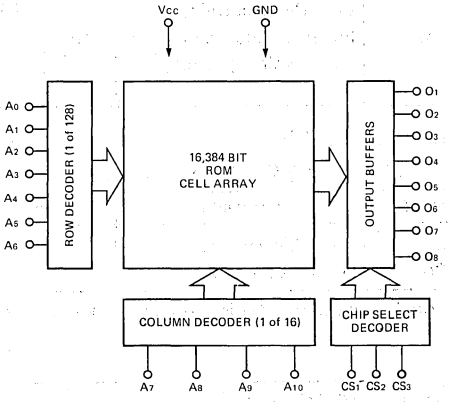
The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316A	Cerdip	550ns	0°C to +70°C
SYP2316A	Plastic	550ns	0°C to +70°C
SYD2316B	Cerdip	450ns	0°C to +70°C
SYP2316B	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY2316B		SY2316A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		550	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		120		300	ns	and 100 pf
t_{DF}	Chip Deselect Delay		100		150	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	10		20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.2V

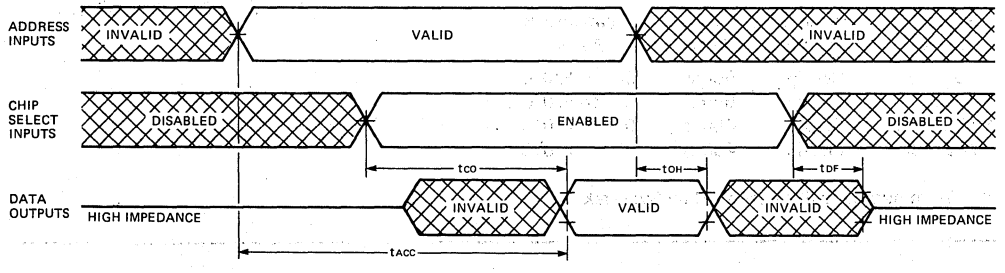
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316A" or "2316B")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

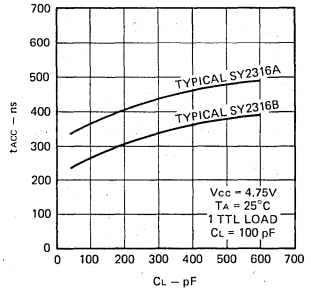
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

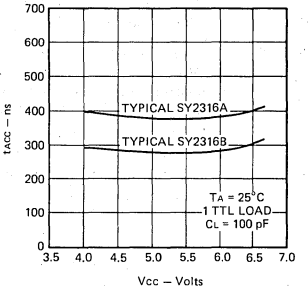
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

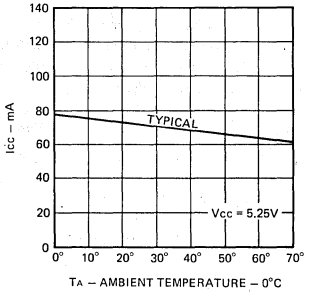
ACCESS TIME VS. CAPACITIVE LOAD



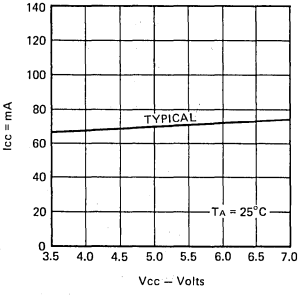
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

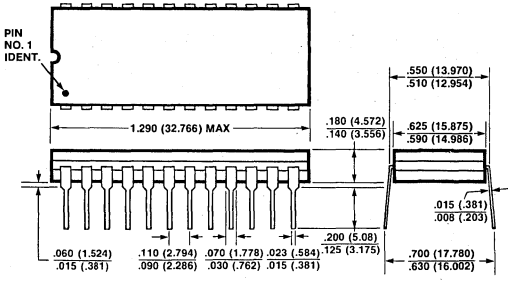


SUPPLY CURRENT VS. SUPPLY VOLTAGE

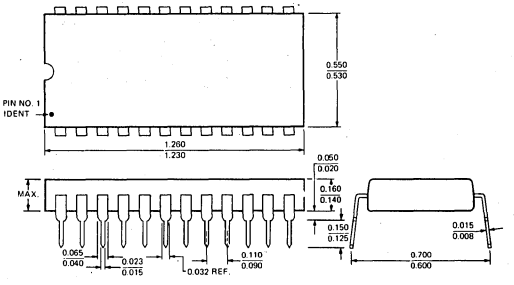


PACKAGE DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



2048x8 Static Read Only Memory

SY2316B-2

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

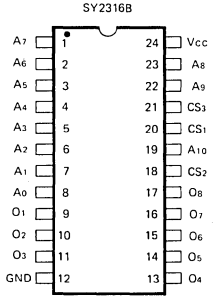
- Access Time—200ns (max.)
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- Metal Mask Programming
  —Two Week Prototype Turnaround
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316B — Pin Compatible with 2716 EPROM
  — Replacement for Two 2708s

The SY2316B-2 high performance Read Only Memory is organized 2048 words by 8 bits with an access time of less than 200ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

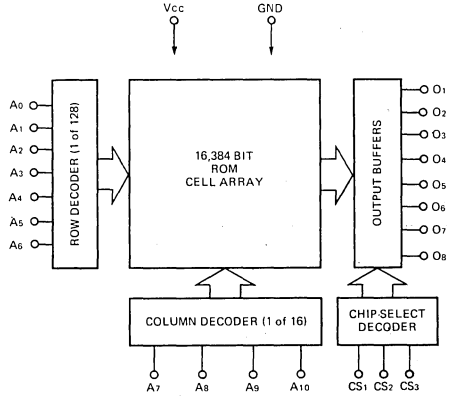
The SY2316B-2 operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B-2 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316B-2	Cerdip	200ns	0°C to +70°C
SYP2316B-2	Plastic	200ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10° to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ Vin ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
Icc	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, Vin = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		200	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		100	ns	and 100 pF
t_{DF}	Chip Deselect Delay		100	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	10		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

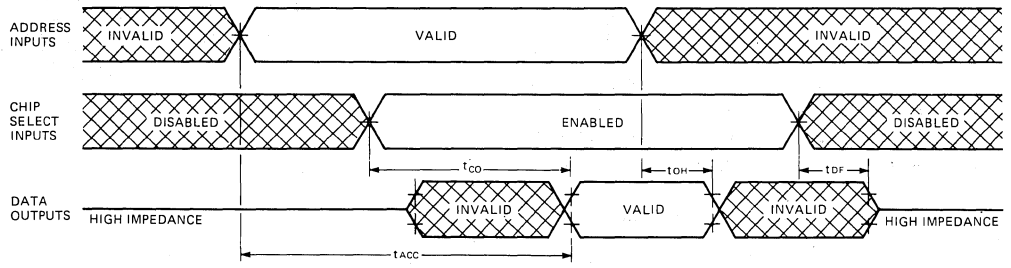
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316B-2")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

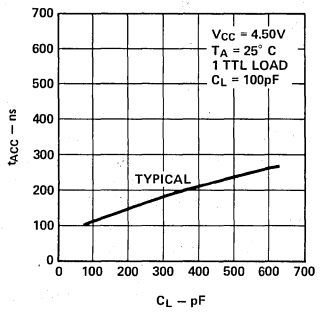
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

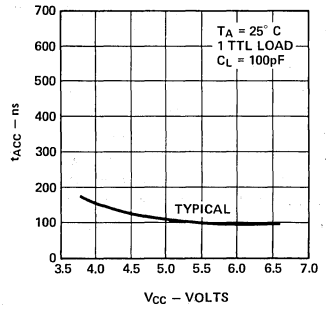
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

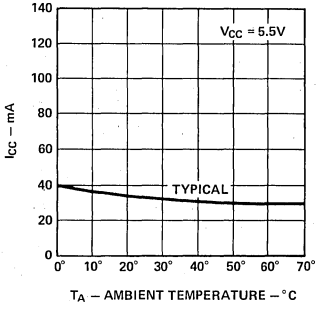
ACCESS TIME vs. CAPACITIVE LOAD



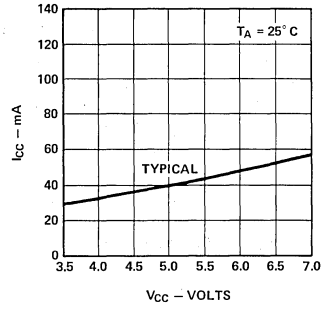
ACCESS TIME vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. AMBIENT TEMPERATURE

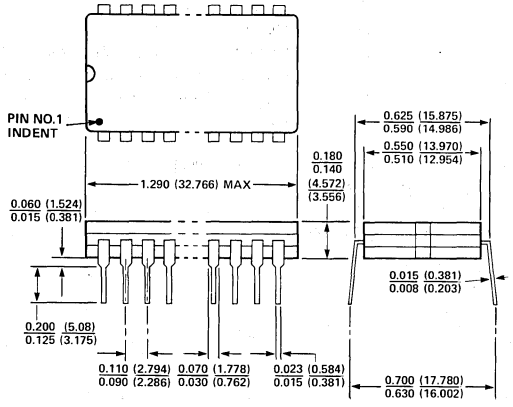


SUPPLY CURRENT vs. SUPPLY VOLTAGE

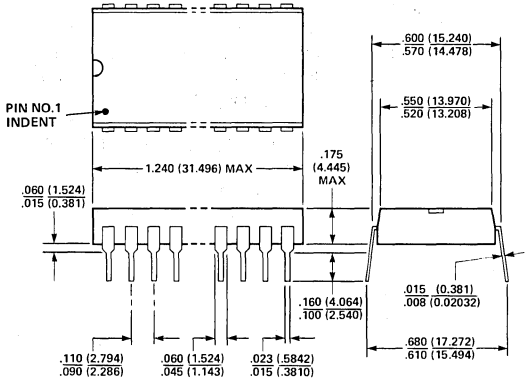


PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



2048 x 8 Static Read Only Memory

SY2316B-3

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Access Time—300ns (max.)
- 2048x8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316B — Pin Compatible with 2716 EPROM
  — Replacement for Two 2708s

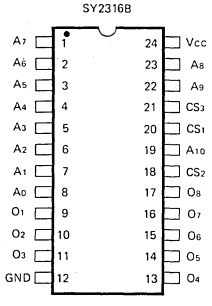
ROMs

The SY2316B-3 high performance Read Only Memory is organized 2048 words by 8 bits with an access time of less than 300 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

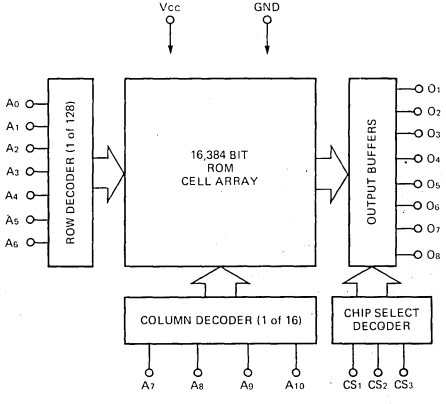
The SY2316B-3 operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace the 2716 16K EPROM, the SY2316B-3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2316B-3	Cerdip	300ns	0°C to +70°C
SYP2316B-3	Plastic	300ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10° to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		300	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		130	ns	and 100 pF
t_{DF}	Chip Deselect Delay		130	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

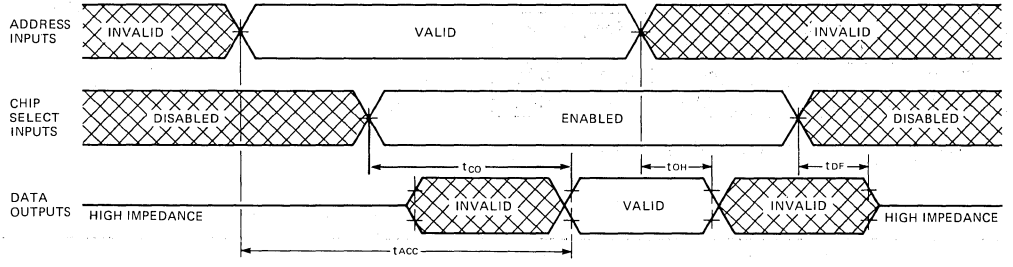
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316B-3")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

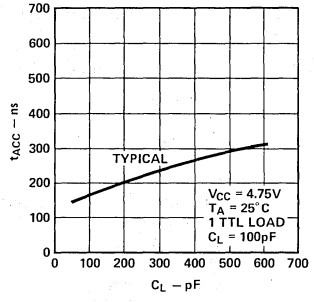
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

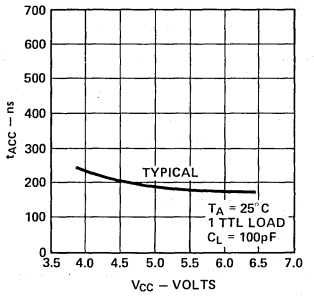
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

TYPICAL CHARACTERISTICS

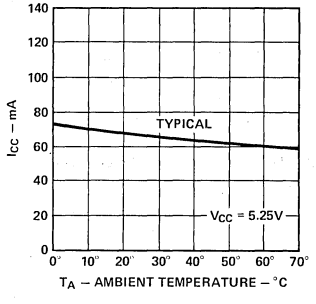
ACCESS TIME VS. CAPACITIVE LOAD



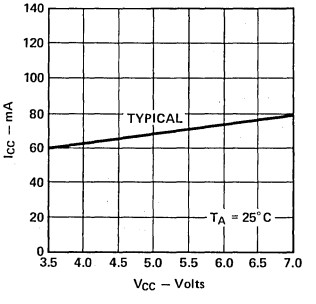
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

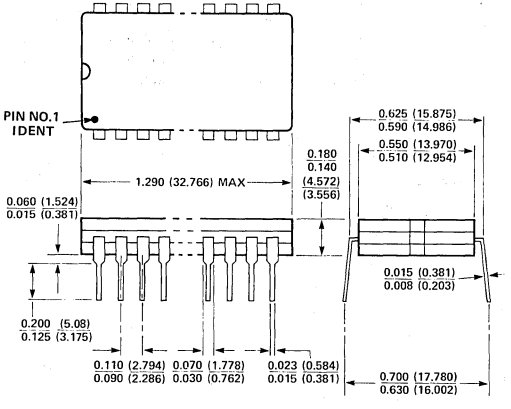


SUPPLY CURRENT VS. SUPPLY VOLTAGE

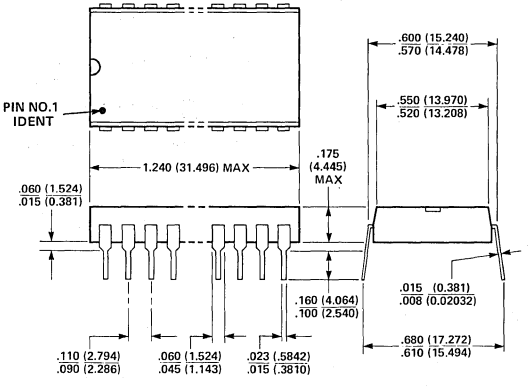


PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



4096 x 8 Static Read Only Memory

SY2332/33

SYNERTEK
A SUBSIDIARY OF HONEYWELL

MEMORY PRODUCTS

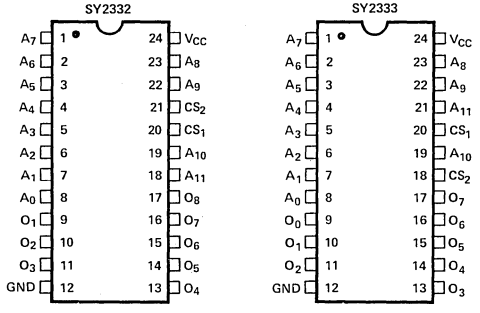
- SY2333-2732 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time—450ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2332-2532 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- 2708/2716/2532/2732 EPROMs Accepted as Program Data Inputs

The SY2332/3 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

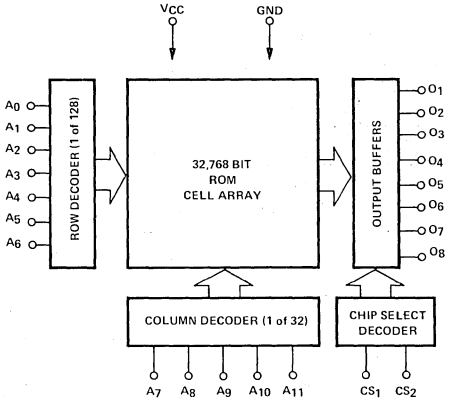
The SY2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace either the 2732 or 2532 32K EPROMs, the SY2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYD2333	Cerdip	450ns	0°C to +70°C
SYP2333	Plastic	450ns	0°C to +70°C
SYD2332	Cerdip	450ns	0°C to +70°C
SYP2332	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.75V, I_{OH} = -200μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.25V, 0V ≤ V_{IN} ≤ 5.25V
I_{LO}	Output Leakage Current		10	μA	Chip Deselected· V_{OUT} = +0.4 V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled V_{CC} = 5.25V, V_{IN} = V_{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	SY2332/33		Units	Test Conditions
		Min.	Max.		
t_{ACC}	Address Access Time		450	ns	Output load: 1 TTL load and 100pF
t_{CO}	Chip Select Delay		150	ns	Input Pulse Levels: 0.8 to 2.4V
t_{DF}	Chip Deselect Delay		150	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

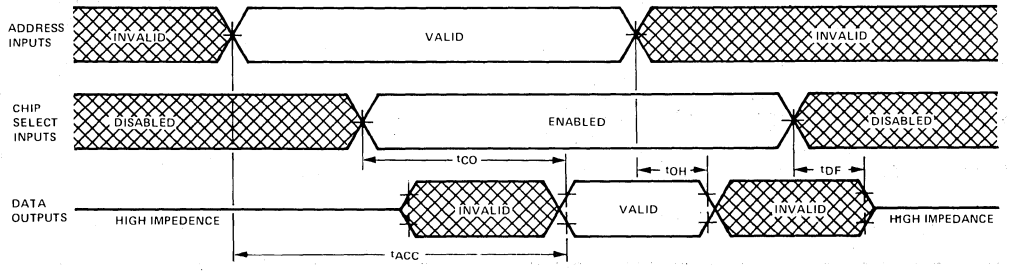
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2333 or 2332)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	30	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
	31	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8 or O_7) is the MSB and Output 1 (O_1 or O_0) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the inital input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

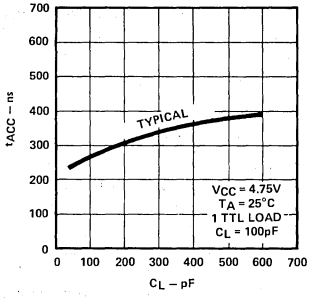
:0300010053F8ECC5

Send bit pattern data to the following special address:

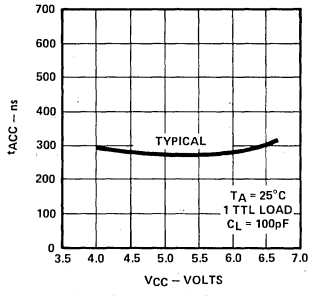
Synertek — ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

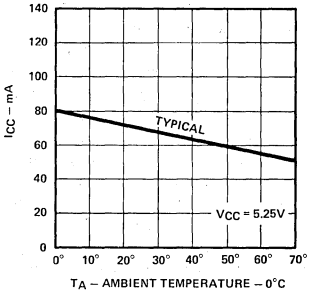
ACCESS TIME VS. CAPACITIVE LOAD



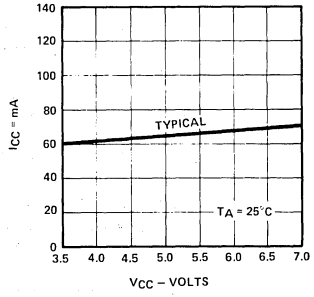
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

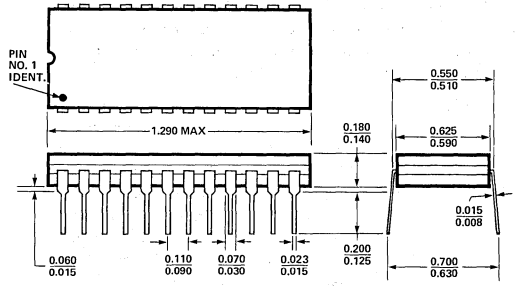


SUPPLY CURRENT VS. SUPPLY VOLTAGE

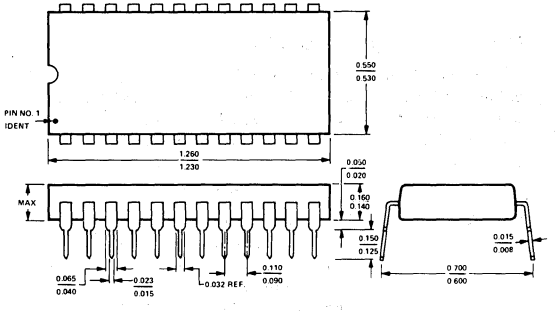


PACKAGING DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



4096 x 8 Static Read Only Memory

SY2332-3
SY2333-3

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- SY2333-2732 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply (±10%)
- Access Time—300ns (max)
- Totally Static Operation
- Completely TTL Compatible
- SY2332-2716 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- 2708/2716/2732 EPROMs Accepted as Program Data Inputs

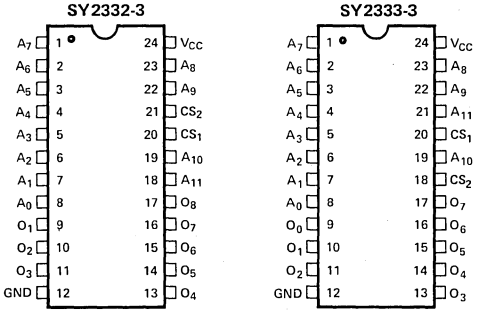
ROMs

The SY2332-3 and SY2333-3 high performance read only memories are organized 4096 words by 8 bits with access times of less than 300 ns. They are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

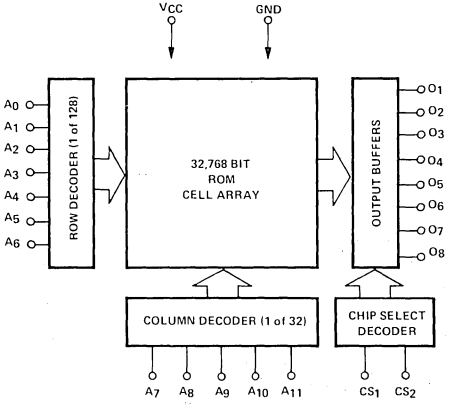
The SY2332-3 and SY2333-3 operate totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace 2716 or 2732 32K EPROMs, the SY2332-3 and SY2333-3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2333-3	Ceramic	300ns	0°C to +70°C
SYP2333-3	Plastic	300ns	0°C to +70°C
SYC2332-3	Ceramic	300ns	0°C to +70°C
SYP2332-3	Plastic	300ns	0°C to +70°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.5V, I_{OH} = -400μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.5V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current		10	μA	Chip Deselected
					V_{OUT} = +0.4 V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled
					V_{CC} = 5.5V, V_{IN} = V_{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±10% (unless otherwise specified)

Symbol	Parameter	SY2332-3 and SY2333-3		Units	Test Conditions
		Min.	Max.		
t_{ACC}	Address Access Time		300	ns	Output load: 1 TTL load
t_{CO}	Chip Select Delay		100	ns	and 100pF
t_{DF}	Chip Deselect Delay		100	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After	20		ns	Timing reference levels:
	Address Change Delay				Input: 1.5V
					Output: 0.8V and 2.0V

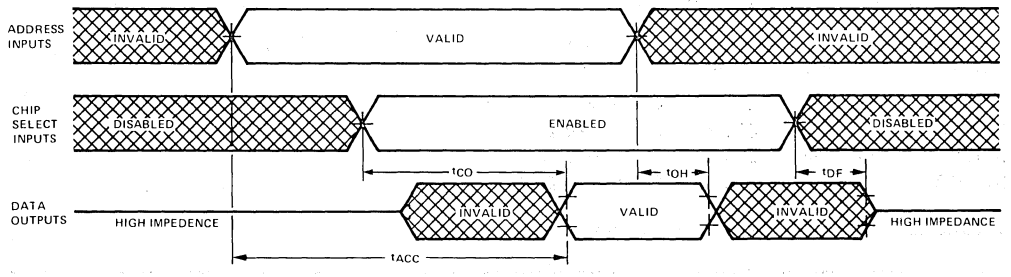
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under
C_O	Output Capacitance		10	pF	test tied to AC ground

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch 2333 or 2332)
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
	31	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8 or O_7) is the MSB and Output 1 (O_1 or O_0) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the inital input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

Frames 7, 8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

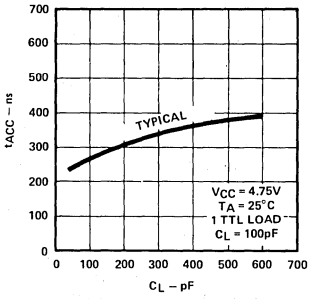
:0300010053F8ECC5

Send bit pattern data to the following special address:

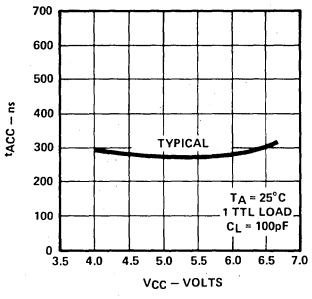
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

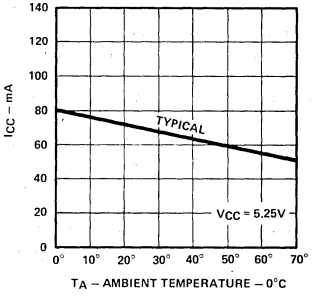
ACCESS TIME VS. CAPACITIVE LOAD



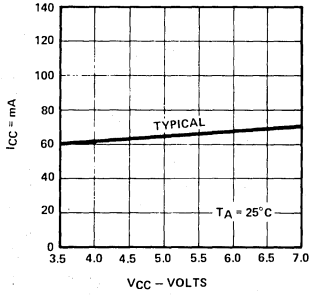
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

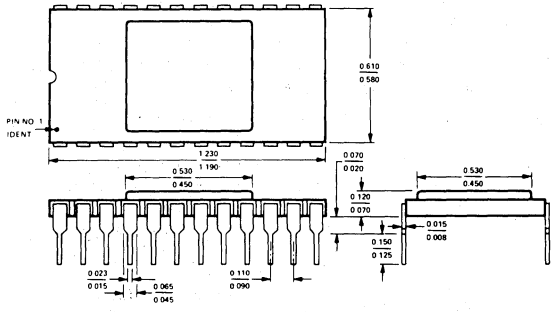


SUPPLY CURRENT VS. SUPPLY VOLTAGE

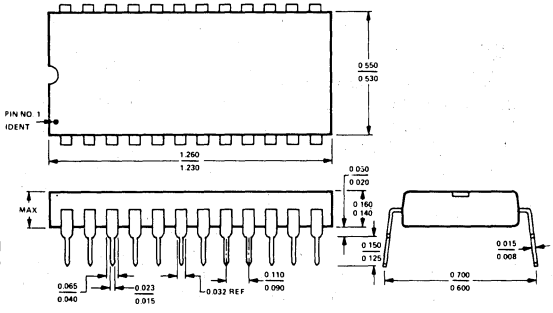


PACKAGE DIAGRAMS

CERAMIC PACKAGE



PLASTIC PACKAGE



8192 x 8 Static Read Only Memory

SY2364/SY2364A

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- 2564 EPROM Pin Compatible
- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 24 Pin JEDEC Approved Pinout
- SY2364A — Automatic Power Down ($\overline{CE}$)
- SY2364 — Non Power Down Version
  — Programmable Chip Select
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

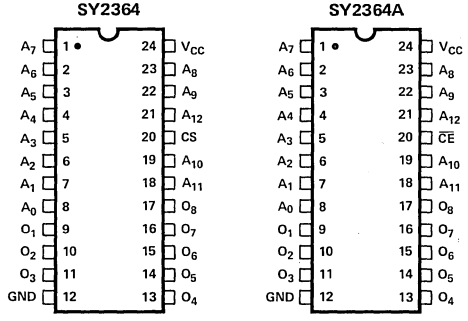
The SY2364 and SY2364A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 24 pin 64K ROMs.

The SY2364 offers the simplest operation (no power down.) Its programmable chip select allows two 64K ROMs to be OR-tied without external decoding.

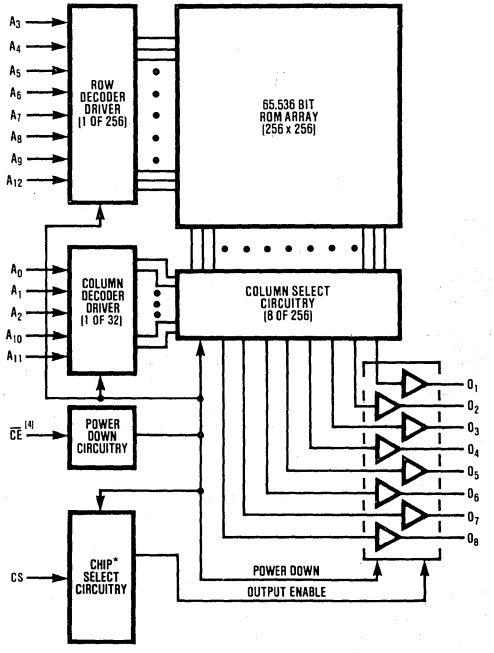
The SY2364A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%.

Both the SY2364 and SY2364A are pin compatible with the 2564 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE LOW ACTIVE OR HIGH ACTIVE

ORDERING INFORMATION

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYD2364	450 ns	100 mA	N.A.*	Cerdip
SYP2364	450 ns	100 mA	N.A.	Plastic
SYD2364-3	300 ns	100 mA	N.A.	Cerdip
SYP2364-3	300 ns	100 mA	N.A.	Plastic
SYD2364-2	200 ns	100 mA	N.A.	Cerdip
SYP2364-2	200 ns	100 mA	N.A.	Plastic
SYD2364A	450 ns	100 mA	12 mA	Cerdip
SYP2364A	450 ns	100 mA	12 mA	Plastic
SYD2364A-3	300 ns	100 mA	12 mA	Cerdip
SYP2364A-3	300 ns	100 mA	12 mA	Plastic
SYD2364A-2	200 ns	100 mA	12 mA	Cerdip
SYP2364A-2	200 ns	100 mA	12 mA	Plastic

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0° C to +70° C, V_{CC} = +5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	-0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			90	mA	Note 3

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Note: This parameter is periodically sampled and is not 100% tested.

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

A.C. CHARACTERISTICS

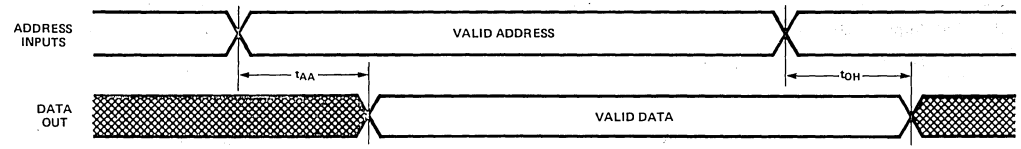
T_A = 0° C to +70° C, V_{CC} = +5V ± 10%

Symbol	Parameter	2364-2 2364A-2		2364-3 2364A-3		2364 2364A		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

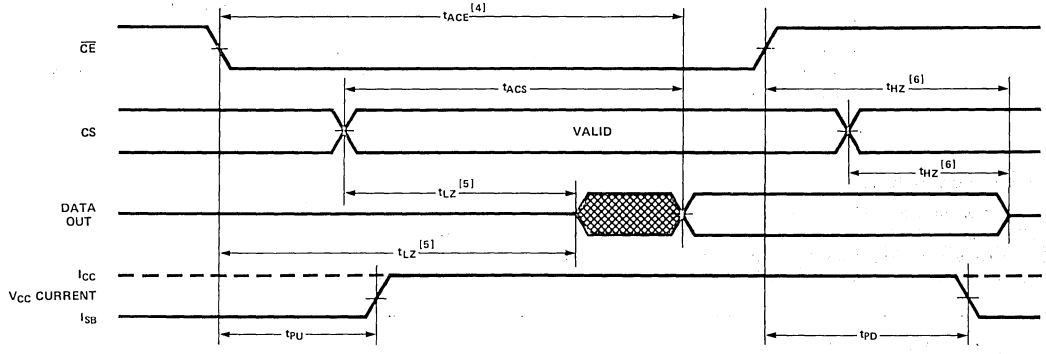
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed 30 seconds.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ going low or CS going active.
6. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ going high or CS going inactive.

TIMING DIAGRAMS

Propagation Delay from Address ($\overline{CE}$ LOW or CS = Active)



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



A.C. TEST CONDITIONS

Input Pulse Levels	2.0V to 2.2V
Input Rise and Fall Times	10 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	See Figure 1

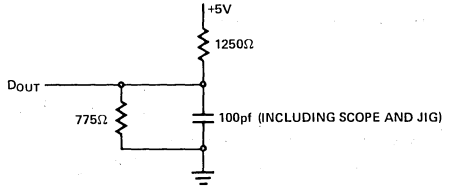


Figure 1.

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2364" or "2364A")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	32	CS chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"). If 2364A, leave blank.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

INTEL DATA CARD FORMAT

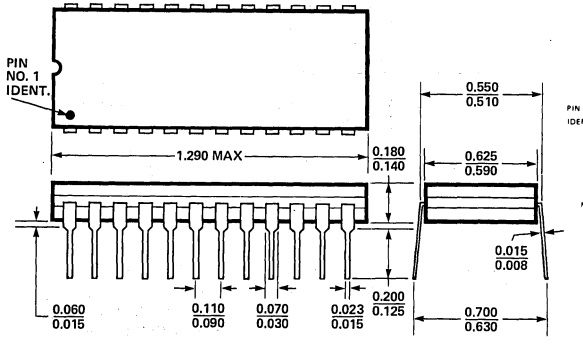
Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

Send bit pattern data to the following special address:

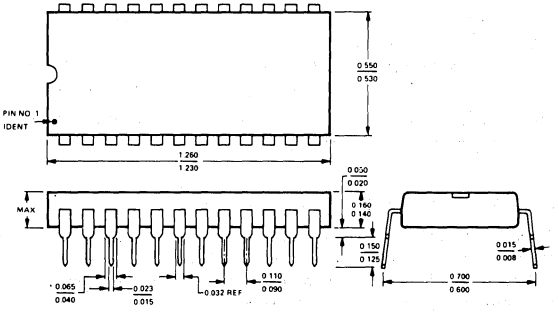
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

PACKAGE DIAGRAMS

CERDIP PACKAGE



PLASTIC PACKAGE



8192 x 8 Static Read Only Memory

SY2365/SY2365A

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- 2764 EPROM Pin Compatible
- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY2365A — Automatic Power Down ($\overline{CE}$)
  — Output Enable Function ($\overline{OE}$)
  — Two Programmable Chip Selects
- SY2365 — Non Power Down Version
  — Four Programmable Chip Selects
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

ROMs

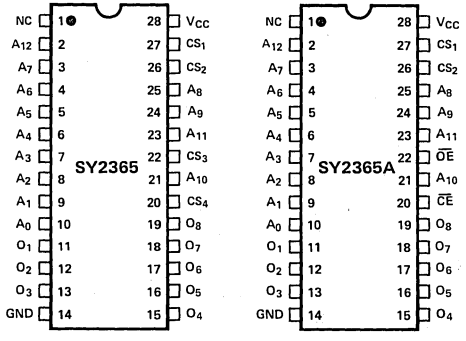
The SY2365 and SY2365A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 64K ROMs.

The SY2365 offers the simplest operation (no power down.) Its four programmable chip selects allow up to sixteen 64K ROMs to be OR-tied without external decoding.

The SY2365A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY2365A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The two programmable chip selects allow up to four 64K ROMs to be OR-tied without external decoding.

Both the SY2365 and SY2365A are pin compatible with the 2764 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

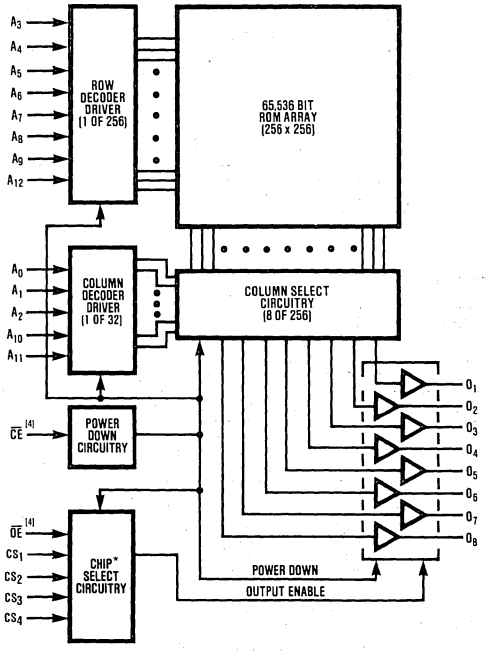
PIN CONFIGURATIONS



ORDERING INFORMATION

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYD2365	450ns	100 mA	N.A.*	Cerdip
SYP2365	450 ns	100 mA	N.A.	Plastic
SYD2365-3	300 ns	100 mA	N.A.	Cerdip
SYP2365-3	300 ns	100 mA	N.A.	Plastic
SYD2365-2	200 ns	100 mA	N.A.	Cerdip
SYP2365-2	200 ns	100 mA	N.A.	Plastic
SYD2365A	450 ns	100 mA	12 mA	Cerdip
SYP2365A	450 ns	100 mA	12 mA	Plastic
SYD2365A-3	300 ns	100 mA	12 mA	Cerdip
SYP2365A-3	300 ns	100 mA	12 mA	Plastic
SYD2365A-2	200 ns	100 mA	12 mA	Cerdip
SYP2365A-2	200 ns	100 mA	12 mA	Plastic

BLOCK DIAGRAM



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output HIGH Level	2.4		V_{CC}	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW Level			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Level	2.0		V_{CC}	V	
V_{IL}	Input LOW Level	-0.5		0.8	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			12	mA	Note 2
I_{OS}	Output Short Circuit Current			70	mA	Note 3

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

Note: This parameter is periodically sampled and is not 100% tested.

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_I	Input Capacitance		5	pf	V_{IN} = 0V
C_O	Output Capacitance		5	pf	V_{OUT} = 0V

A.C. CHARACTERISTICS

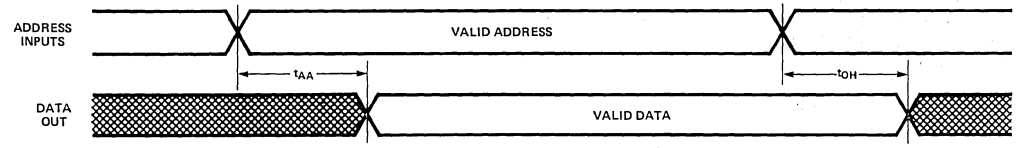
T_A = 0°C to +70°C, V_{CC} = +5V ± 10%

Symbol	Parameter	2365-2 2365A-2		2365-3 2365A-3		2365 2365A		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	Note 4
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	Note 4
t_{LZ}	Ouput LOW Z Delay	10		10		10		ns	Note 5
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 6
t_{PU}	Power Up Time	0		0		0		ns	Note 4
t_{PD}	Power Down Time		85		100		150	ns	Note 4

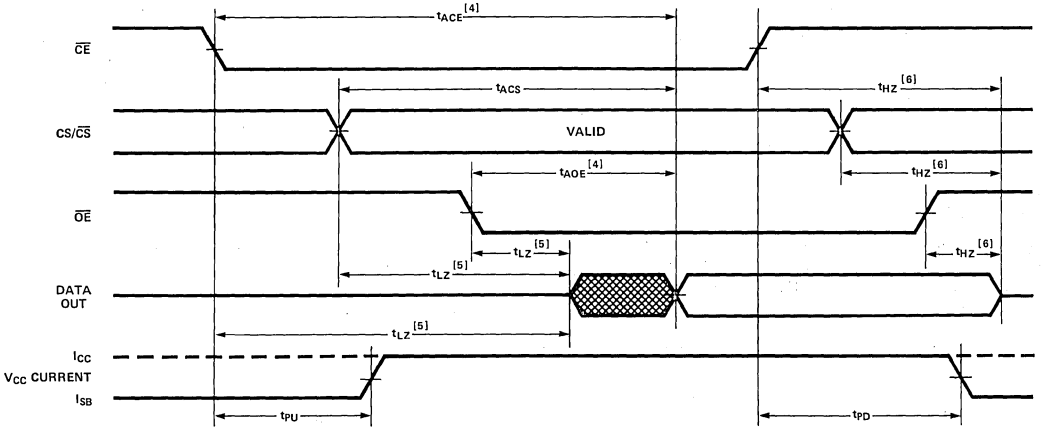
Notes:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE}$ = 2.0V.
3. For a duration not to exceed 30 seconds.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
6. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.

TIMING DIAGRAMS

Propagation Delay from Address ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active)



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



A.C. TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	See Figure 1

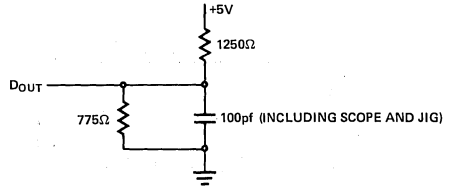


Figure 1.

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2365" or "2365A")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	29	CS_4 chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"). If 2365A, leave blank.
	30	CS_3 chip select logic level. If 2365A, leave blank.
	31	CS_2 chip select logic level.
	32	CS_1 chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

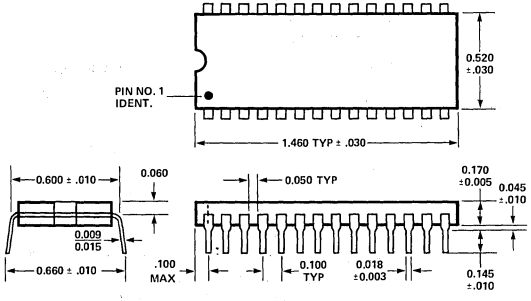
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

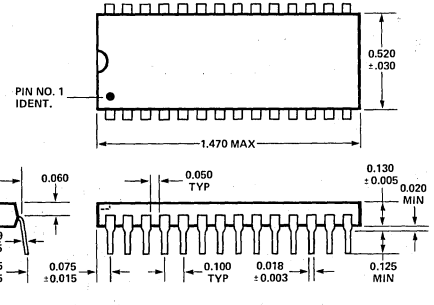
Synertek — ROM
P.O. Box 552
Santa Clara, CA 95052

PACKAGE DIAGRAMS

CerDIP Dual In-Line
28 Leads



Plastic Dual In-Line
28 Leads



16,384 x 8 Static Read Only Memory

SY23128

MEMORY PRODUCTS

PRELIMINARY

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- 2764 EPROM Pin Compatible
- 16,384 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- Automatic Power Down ($\overline{CE}$)
- Output Enable Function ($\overline{OE}$)
- Programmable Chip Select
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

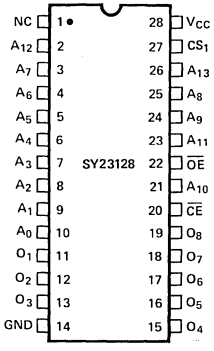
ROMs

The SY23128 high performance Read Only Memory is organized 16,384 words by 8 bits with an access time of 200ns. The ROM is designed to be compatible with all microprocessor and similar applications where high performance large bit storage and simple interfacing are important design considerations. It conforms to the JEDEC approved pinout for 28 pin 128K ROMs.

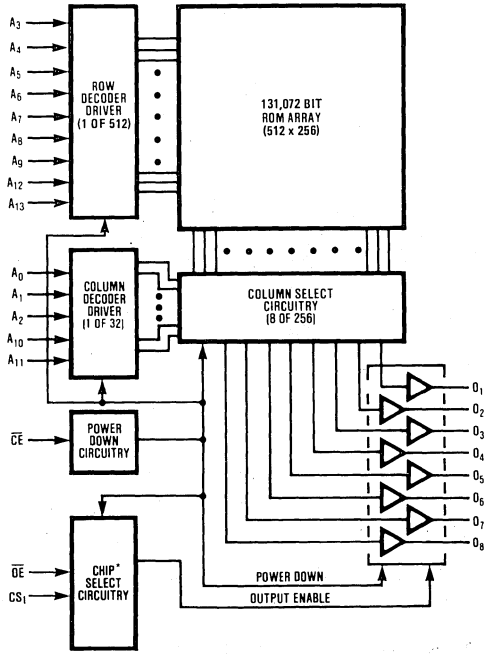
The SY23128 offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY23128 is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The programmable chip select allows up to two 128K ROMs to be OR-tied without external decoding.

The SY23128 is pin compatible with the 2764 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATION



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE LOW ACTIVE OR HIGH ACTIVE

1024 x 8 High Speed Read Only Memory

SY3308

MEMORY PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

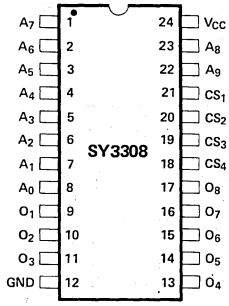
- Access Time — 70 ns (max)
- Single +5 Volt Supply
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- Pin Compatible with 8K Bipolar PROMs — Replaces 7681 or 82S181
- Three-State Outputs for Wire-OR Expansion
- Four Programmable Chip Selects
- 8K Bipolar PROMs Accepted as Program Data Inputs

The Synertek SY3308 is a high speed 8192-bit static mask programmable Read Only Memory organized 1024 words by 8 bits. Designed to be compatible with industry standard 8K bipolar PROMs, it eliminates the need to redesign printed circuit boards for volume production after prototyping with PROM's. The device offers full TTL compatibility on all inputs and outputs and operates on a single +5V power supply. The three-state output buffers facilitate system expansion by allowing outputs to be wire-ORed together. These features, combined with a maximum access time of 70 nsec, make the SY3308 suitable for application where high performance, large bit storage and simple interface are important design considerations.

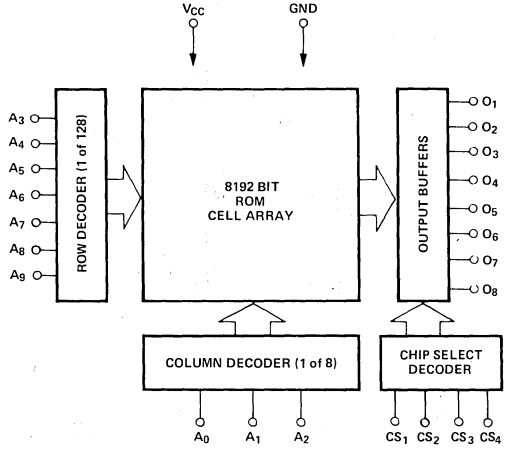
The SY3308 utilizes fully static circuitry and operates asynchronously so no clocks are required. The four chip select buffers are mask programmable to be any combination of high active, low active or don't care that is desired. This allows up to sixteen ROM's to be OR-tied without external decoding.

The SY3308 is fabricated using Synertek's scaled, high performance N-channel MOS technology, This, combined with innovative design techniques, provides the high performance and ease-of-use features associated with non-clocked static memories.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC3308	Ceramic	70 ns	0°C to +75°C
SYD3308	Cerdip	70 ns	0°C to +75°C

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-1.5V to +7.0V
Applied Output Voltage	-1.5V to +7.0V
Applied Input Voltage	-1.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = 5.0V ± 10% (unless otherwise specified) (Note 1)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		Vcc	Volts	V_{CC} = 4.5V, I_{OH} = -2.4mA
V_{OL}	Output LOW Voltage			0.45	Volts	V_{CC} = 4.5V, I_{OL} = 10mA
V_{IH}	Input HIGH Voltage	2.0		Vcc	Volts	
V_{IL}	Input LOW Voltage	-1.0		0.8	Volts	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ V_{CC}
I_{LO}	Output Leakage Current	-10		10	μA	Chip Deselected, V_{out} = 0V to V_{CC}
I_{SC}	Output Short Circuit Current	-80			mA	Duration not to exceed 30 sec.
I_{CC}	Power Supply Current			120	mA	Output Unloaded, V_{CC} = 5.5V, V_{in} = V_{CC}

A.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = 5.0V ± 10% (unless otherwise specified) (Note 1)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time		70	ns	
t_{CO}	Chip Select Delay		40	ns	
t_{DF}	Chip Deselect Delay	0	40	ns	See A.C. Test Conditions
t_{OH}	Previous Data Valid After Address Change Delay	5		ns	

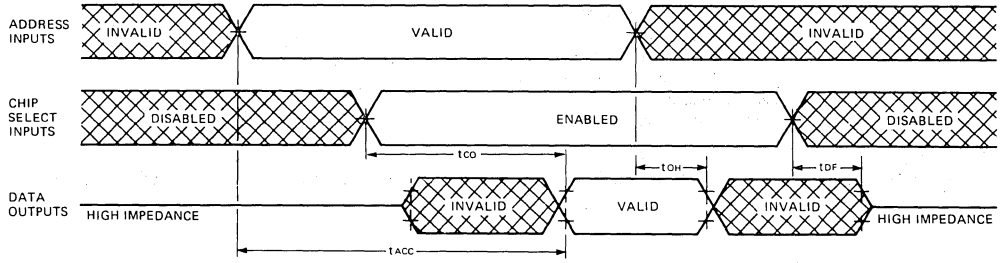
CAPACITANCE

t_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		5	pF	V_{in} = 0V
C_O	Output Capacitance		8	pF	V_{out} = 0V

NOTE: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



(See following page for notes.)

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0 Volts
Input Rise and Fall Times	5 nsec
Input and Output Timing Reference Levels	1.5 Volts
Output Load	See Figure 1

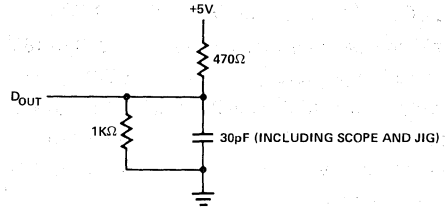


Figure 1.

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "3308")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	29	CS_4 chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2").
	30	CS_3 chip select logic level.
	31	CS_2 chip select logic level.
	32	CS_1 chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

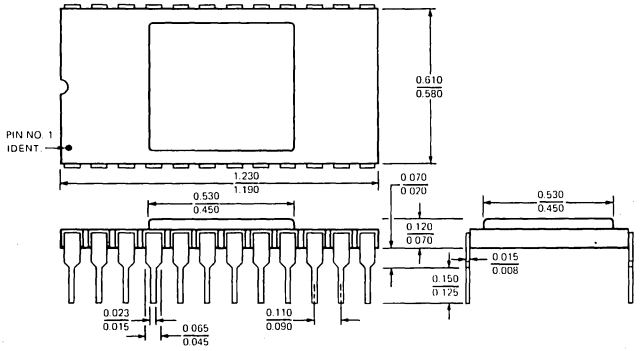
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

NOTES:

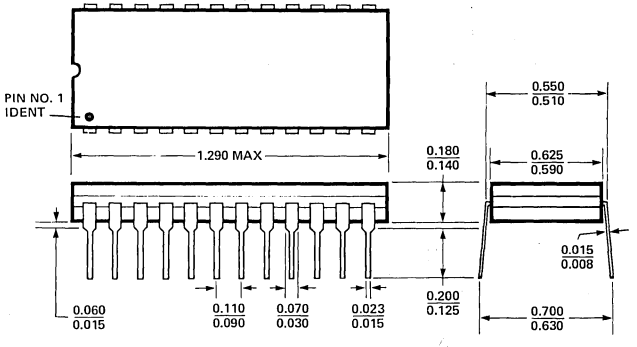
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

PACKAGING DIAGRAM

CERAMIC PACKAGE



CERDIP PACKAGE



ROMs

2048 x 8 High Speed Read Only Memory

SY3316/SY3316A

MEMORY PRODUCTS

SYNERTEK®
A SUBSIDIARY OF HONEYWELL

- Access Time — 80ns (max)
- Single +5 Volt Supply (± 10%)
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- SY3316A — Automatic Power Down ($\overline{CE}$)
- Pin Compatible with 16K Bipolar PROMs — Replaces 3636 or 82S191
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects (two on SY3316A)
- 16K Bipolar PROMs Accepted as Program Data Inputs

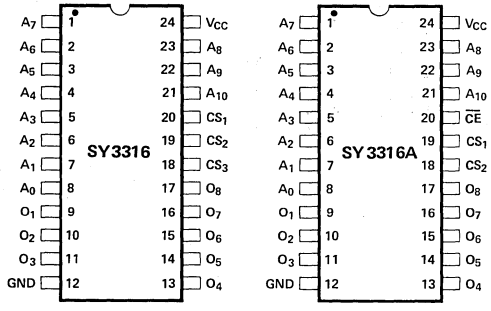
The SY3316 and SY3316A are high speed 16,384 bit static mask programmable Read Only Memories organized 2048 words by 8 bits. Designed to be pin compatible with 16K bipolar PROMs, they eliminate the need to redesign printed circuit boards for volume production after prototyping with PROMs.

The SY3316A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings of as much as 80%. The two programmable chip selects (CS) allow as many as four ROMs to be OR-tied without external decoding.

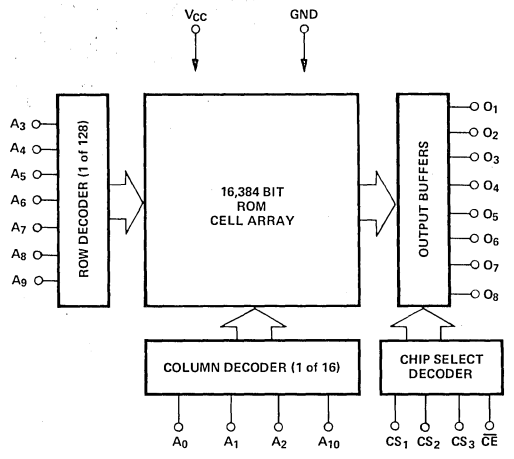
The SY3316 offers somewhat simpler operation than the SY3316A. It's three programmable chip selects allow up to eight ROMs to be OR-tied without external decoding.

Both devices are fabricated using Synertek's scaled high performance N-channel MOS technology. This, combined with innovative design techniques, provides the high performance and ease-of-use features associated with static memories.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYC3316	80 ns	120 mA	N.A.	Ceramic
SYD3316	80 ns	120 mA	N.A.	Cerdip
SYC3316A	80 ns	120 mA	20 mA	Ceramic
SYD3316A	80 ns	120 mA	20 mA	Cerdip

A custom number will be assigned by Synertek.

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	-10°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-1.5V to +7.0V
Applied Output Voltage	-1.5V to +7.0V
Applied Input Voltage	-1.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = 5.0V ± 10% (Note 1)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		Vcc	Volts	V_{CC} = 4.5V, I_{OH} = -2.4mA
V_{OL}	Output LOW Voltage			0.45	Volts	V_{CC} = 4.5V, I_{OL} = 10mA
V_{IH}	Input HIGH Voltage	2.0		Vcc	Volts	
V_{IL}	Input LOW Voltage	-1.0		0.8	Volts	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{in} ≤ V_{CC}
I_{LO}	Output Leakage Current	-10		10	μA	Chip Deselected, V_{out} = 0V to V_{CC}
I_{SC}	Output Short Circuit Current	-100			mA	Note 5
I_{CC}	Power Supply Current			120	mA	Note 2
I_{SB}	Standby Supply Current			20	mA	Note 3

A.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = +5V ± 10% (Note 1)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{ACC}	Address Access Time			80	ns	
t_{ACE}	Chip Enable Access Time			80	ns	Note 4
t_{ACS}	Chip Select Access Time			40	ns	
t_{OFF}	Chip Deselect Time	0		40	ns	
t_{OH}	Output Hold Time	5			ns	
t_{PU}	Power Up Time	0			ns	Note 4
t_{PD}	Power Down Time			40	ns	Note 4

CAPACITANCE

t_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		5	pF	V_{in} = 0V
C_O	Output Capacitance		8	pF	V_{out} = 0V

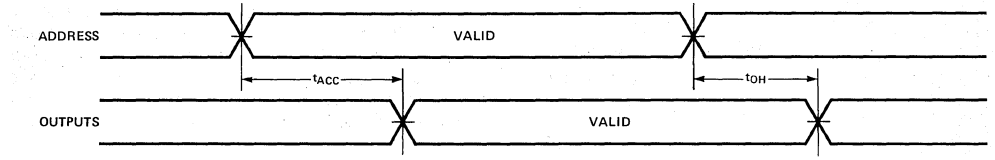
NOTE: This parameter is periodically sampled and is not 100% tested.

NOTES:

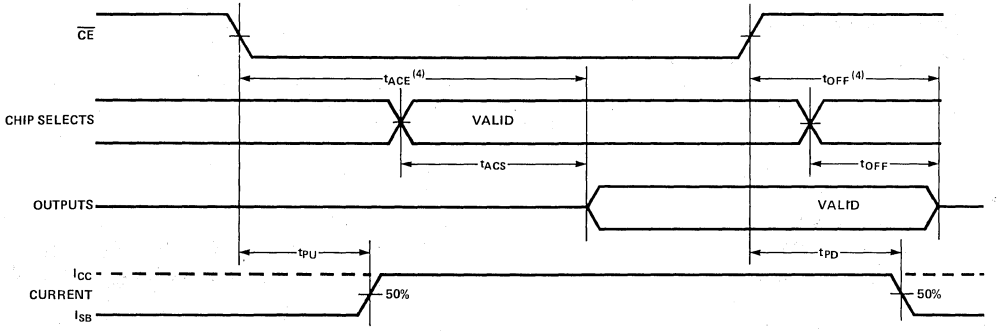
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Device selected with outputs unloaded.
3. Applies to SY3316A only with CE = 2.0V.
4. Applies to SY3316A only.
5. Output short circuit current is measured with V_{OUT} = 0V, one output at a time with a maximum duration of 30 seconds.

TIMING DIAGRAMS

Address to Output Delay (CS Active and $\overline{CE}$ Low)



Chip Enable/Chip Select to Output Delay (Address Valid)



A.C. TEST CONDITIONS

Input Pulse Levels		0.4V to 2.4V
Input Rise and Fall Times		5 nsec
Timing Reference Levels:	Input	1.5V
	Output	0.8V and 2.0V
Output Load		See Figure 1

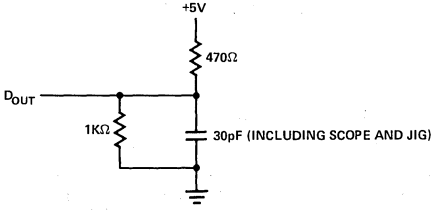


Figure 1.

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "3316" or "3316A")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

INTEL DATA CARD FORMAT

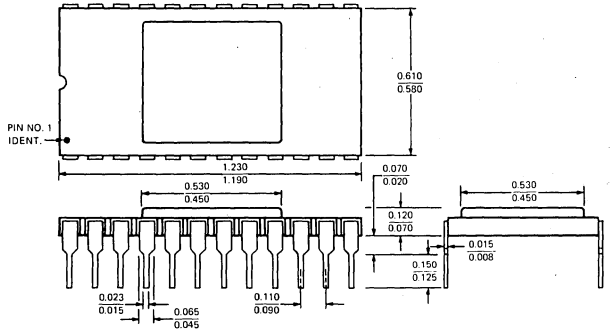
Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

Send bit pattern data to the following special address:

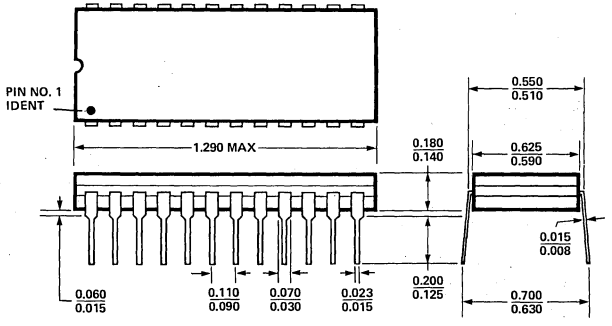
Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

PACKAGE DIAGRAMS

Ceramic Package



Cerdip Package



2048 x 8 High Speed Read Only Memory

Extended Temperature Range (-55°C to +125°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYM3316/ SYM3316A

MEMORY PRODUCTS

PRELIMINARY

ROMs

- Access Time — 100ns (max.)
- Single +5 Volt Supply (± 10%)
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- SYM3316A — Automatic Power Down ($\overline{CE}$)
- Pin Compatible with 16K Bipolar PROMs — Replaces 3636 or 82S191
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects (two on SYM3316A)
- 16K Bipolar PROMs Accepted as Program Data Inputs

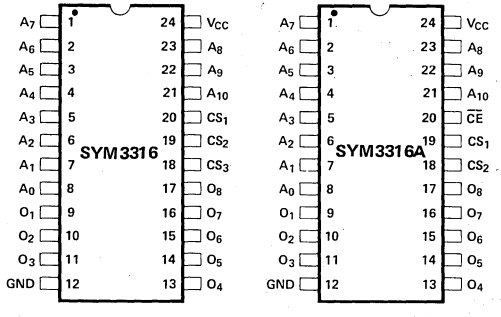
The SYM3316 and SYM3316A are high speed 16,384 bit static mask programmable Read Only Memories organized 2048 words by 8 bits. Designed to be pin compatible with 16K bipolar PROMs, they eliminate the need to redesign printed circuit boards for volume production after prototyping with PROMs.

The SYM3316A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings of as much as 80%. The two programmable chip selects (CS) allow as many as four ROMs to be OR-tied without external decoding.

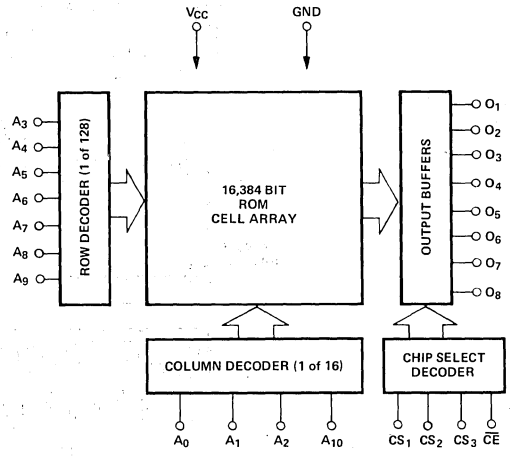
The SYM3316 offers somewhat simpler operation than the SYM3316A. It's three programmable chip selects allow up to eight ROMs to be OR-tied without external decoding.

Both devices are fabricated using Synertek's scaled high performance N-channel MOS technology. This, combined with innovative design techniques, provides the high performance and ease-of-use features associated with static memories.

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time	Operating Current	Standby Current	Package Type
SYMC3316	100 ns	120 mA	N.A.	Ceramic
SYMD3316	100 ns	120 mA	N.A.	Cerdip
SYMC3316A	100 ns	120 mA	20 mA	Ceramic
SYMD3316A	100 ns	120 mA	20 mA	Cerdip

A custom number will be assigned by Synertek.

Microprocessors

CONFIDENTIAL

Microprocessors

		Page
Microcomputers		
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Microprocessors and Peripherals		
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SY2661	Enhanced Programmable Communications Interface	3-39
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SY6520/6520A; SY6820/68B20	Peripheral Interface Adapter (PIA)	3-67
SYE6520/6820; SYE6520A/68B20	Peripheral Interface Adapter (Extended Temperature)	3-79
SY6521/6821; SY6521A/68B21	Peripheral Interface Adapter (PIA)	3-81
SYE6521/6821; SYE6521A/68B21	Peripheral Interface Adapter (Extended Temperature)	3-93
SY6522/6522A	Versatile Interface Adapter	3-95
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SY6591/6591A	Floppy Disk Controller (FDC)	3-179
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SY68045	CRT Controller (CRTC)	3-185

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Single-Chip Microcomputer

Z8™

PRODUCT SPECIFICATION

PRELIMINARY

Description

The Z8 microcomputer introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcomputers, the Z8 offers faster execution; more efficient use of memory; more sophisticated interrupt, input/output and bit-manipulation capabilities; and easier system expansion.

Under program control, the Z8 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2K of internal ROM, a traditional microprocessor that manages up to 124K of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-Bus. In all configurations, a large number of pins remain available for I/O.

Features

- □ Complete microcomputer with on-chip RAM, ROM and I/O
  - ○ 128 bytes of on-chip RAM
  - ○ 2K bytes of on-chip ROM
  - ○ 32 I/O lines
- □ Two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler
- □ Full-duplex UART clocked by an internal timer
- □ 144-byte register file includes:
  - ○ 124 general-purpose registers, each of which can be used as an accumulator, index register, storage element, address register or part of the internal stack
  - ○ Four I/O port registers
  - ○ Sixteen status and control registers for programming and polling the Z8 Microcomputer
- □ Register pointer permits shorter, faster instructions to access one of nine working-register groups
- □ Vectored, prioritized interrupts for I/O, counter/timers and UART
- □ Expandable bus interfaces up to 62K bytes each of external program memory and external data memory
- □ On-chip oscillator can be driven by a crystal, RC, LC or external clock source
- □ High-speed instruction execution

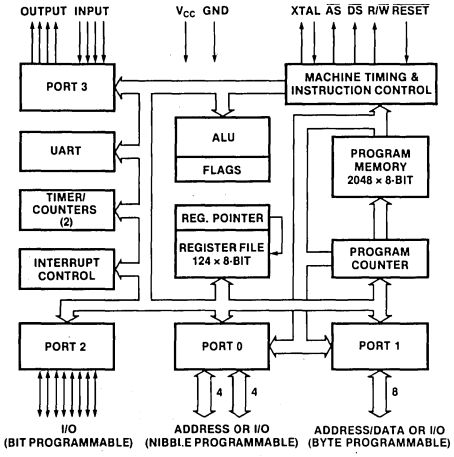

Figure 1. Z8 Block Diagram

- ○ Working-register operations = 1.5 μs
- ○ Average instruction execution = 2.2 μs
- ○ Longest instruction = 5 μs
- □ Low-power standby mode retains contents of general-purpose registers
- □ Single +5 V supply
- □ All pins TTL compatible

Pin Description

$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$. *I/O Port Lines* (Input/Outputs, TTL compatible). These 32 lines are divided into four 8-bit I/O ports that can be configured under program control for I/O or external memory interface.

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Pin Description (Cont.)

$\overline{AS}$. *Address Strobe* (output, active Low), Address Strobe is pulsed once at the beginning of each machine cycle. Addresses are output via Ports 0 and 1 for internal and external program fetches and external data memory transfers. The addresses for all external program or data memory transfers are valid at the trailing edge of $\overline{AS}$. Under program control, $\overline{AS}$ can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe and Read/Write.

$\overline{DS}$. *Data Strobe* (output, active Low). Data Strobe is activated once for each external memory transfer.

R/$\overline{W}$. *Read/Write* (output). R/W is Low when the Z8 is writing to external program or data memory.

XTAL1, XTAL2. *Crystal 1, Crystal 2* (time-base input and output). These pins connect a series-resonant crystal (8 MHz maximum), LC network, RC network or an external single-phase clock (8 MHz maximum) to the on-chip clock oscillator and buffer.

$\overline{RESET}$. *Reset* (input, active Low). $\overline{RESET}$ initializes the Z8. When $\overline{RESET}$ is deactivated, the Z8 begins program execution from internal program location $000C_H$.

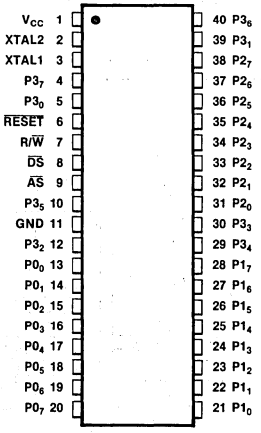


Figure 2. Pin Assignments

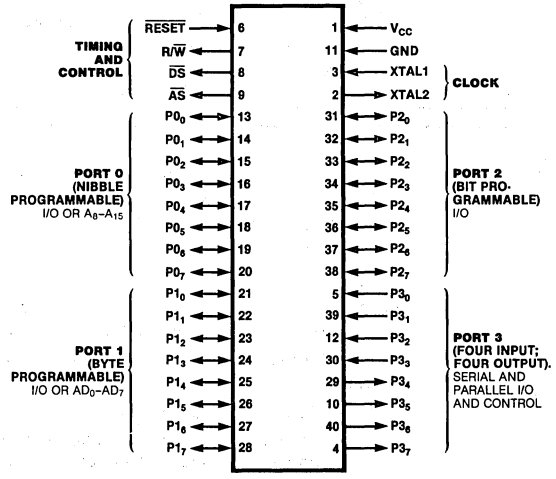


Figure 3. Pin Functions

Architecture

Z8 architecture is characterized by a flexible I/O scheme, an efficient register and address space structure and a number of ancillary features that are helpful in many applications.

Microcomputer applications demand powerful I/O capabilities. The Z8 fulfills this with 32 pins dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

Because the multiplexed address/data bus is merged with the I/O-oriented ports, the Z8 can assume many different memory and I/O configurations. These configurations range from a self-contained microcomputer to a microprocessor that can address 124K of external memory.

The Z8 offers three basic address spaces to support this wide range of configurations: program memory (internal and external), data memory (external) and the register file (internal). The 144-byte random-access register file is composed of 124 general-purpose registers, 4 I/O port registers, and 16 control and status registers.

To unburden the program from coping with real-time problems such as serial data communication and counting/timing, the Z8 offers an on-chip asynchronous receiver/transmitter (UART), and two counter/timers with a large number of user-selectable modes. Hardware support for the UART is minimized because one of the on-chip timers supplies the bit rate.

Address Spaces

Program Memory. The 16-bit program counter addresses 64K bytes of program memory space. Program memory can be located in two areas: one internal and the other external (Figure 4). The first 2048 bytes consist of on-chip mask-programmed ROM. At addresses 2048 and greater, the Z8 executes external program memory fetches.

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts.

Address Spaces (Cont.)

Data Memory. The Z8 can address 62K bytes of external data memory beginning at locations 2048 (Figure 5). External data memory may be included with or separated from the external program memory space. $\overline{DM}$, an optional I/O function that can be programmed to appear on pin $P3_4$, is used to distinguish between data and program memory space.

Register File. The 144-byte register file includes four I/O port registers (R0–R3), 124 general-purpose registers (R4–R127) and sixteen control and status registers (R240–R255). These registers are assigned the address locations shown in Figure 6.

Z8 instructions can access registers directly or indirectly with an 8-bit address field. The Z8 also allows short 4-bit register addressing using the register pointer (one of the control registers). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying sixteen contiguous locations (Figure 7). The register pointer addresses the starting location of the active working-register group.

Stacks. Either the internal register file or the external data memory can be used for the stack. A 16-bit stack pointer (R254 and R255) is used for the external stack, which can reside anywhere in data memory between locations 2048 and 65535. An 8-bit stack pointer (R255) is used for the internal stack which resides within the 124 general-purpose registers (R4–R127).

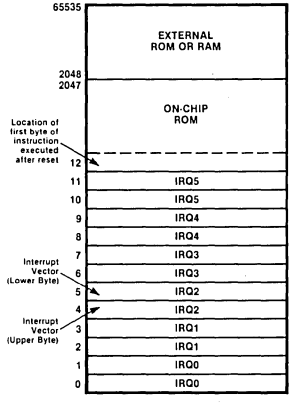


Figure 4. Program Memory Map

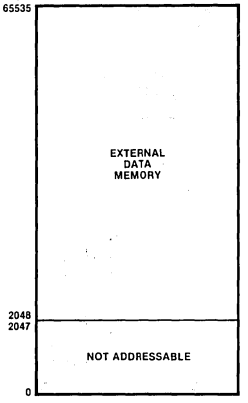


Figure 5. Data Memory Map

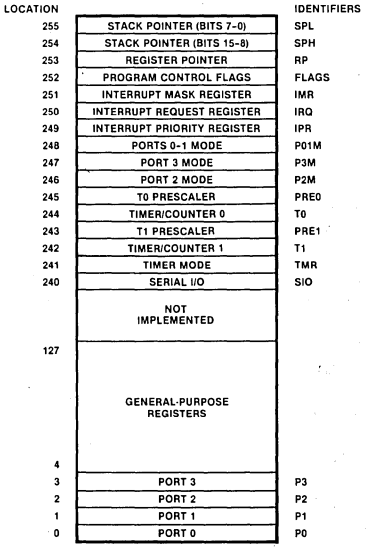


Figure 6. The Register File

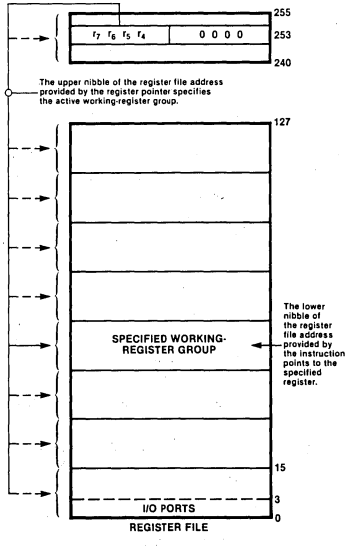


Figure 7. The Register Pointer

I/O Ports

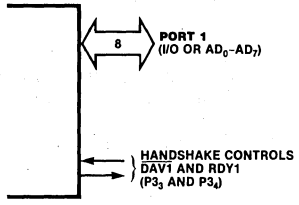
The Z8 has 32 lines dedicated to input and output. These lines are grouped into four ports of eight lines each and are configurable as input, output or address/data. Under software control, the ports can be programmed to provide address outputs, timing, status signals, serial I/O, and parallel I/O with or without handshake. All ports have active pull-ups and pull-downs compatible with TTL loads.

Port 1

Port 1 can be programmed as a byte I/O port or as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 lines $P3_3$ and $P3_4$ are used as the handshake controls RDY1 and $\overline{DAV1}$ (Ready and Data Available).

Memory locations greater than 2048 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed address/data mode (AD_0–AD_7). If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$, allowing the Z8 to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning $P3_3$ as a Bus Acknowledge input, and $P3_4$ as a Bus Request output.

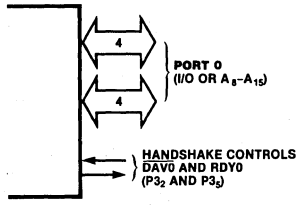


Port 1

Port 0

Port 0 can be programmed as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3 lines P32 and P35 are used as the handshake controls $\overline{DAV0}$ and RDY0.

For external memory references, Port 0 can provide address bits A_8–A_{11} (lower nibble) or A_8–A_{15} (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. When Port 0 nibbles are defined as address bits, they can be set to the high-impedance state along with Port 1 and the control signals $\overline{AS}$, $\overline{DS}$ and R/$\overline{W}$.

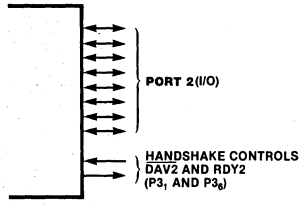


Port 0

Port 2

Each bit of Port 2 can be programmed independently as an input or an output, and is always available for I/O operations. In addition, Port 2 can be configured to provide open-drain outputs.

Like Ports 0 and 1, Port 2 may also be placed under handshake control. In this configuration, Port 3 lines $P3_1$ and $P3_6$ are used as the handshake controls lines $\overline{DAV2}$ and RDY2. The handshake signal assignment for Port 3 lines $P3_1$ and $P3_6$ is dictated by the direction (input or output) assigned to bit 7 of Port 2.

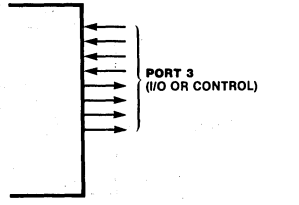


Port 2

Port 3

Port 3 lines can be configured as I/O or control lines: In either case, the direction of the eight lines is fixed as four input ($P3_0$–$P3_3$) and four output ($P3_4$–$P3_7$). For serial I/O, lines $P3_0$ and $P3_7$ are programmed as serial in and serial out respectively.

Port 3 can also provide the following control functions: handshake for Ports 0, 1 and 2 ($\overline{DAV}$ and RDY); four external interrupt request signals (IRQ0–IRQ3); timer input and output signals (T_{IN} and T_{OUT}) and Data Memory Select ($\overline{DM}$).



Port 3

Serial Input/ Output

Port 3 lines $P3_0$ and $P3_7$ can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by counter/timer 0, with a maximum rate of 62.5 kilobits per second.

The Z8 automatically adds a start bit and two stop bits to transmitted data (Figure 8). The Z8 can also provide odd parity. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

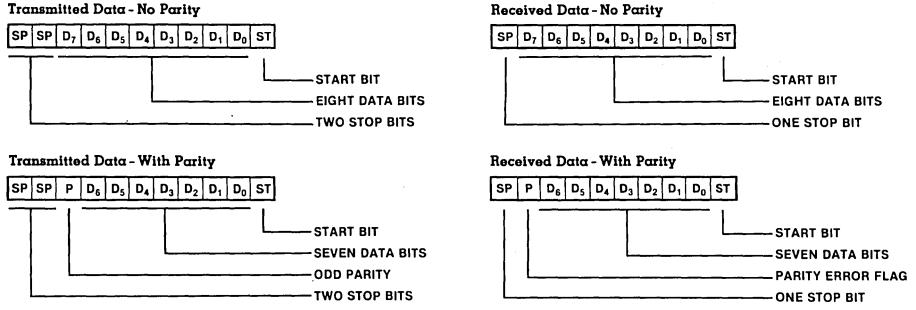


Figure 8. Serial Data Formats

Counter/ Timers

The Z8 contains two 8-bit programmable counter/timers (T_0 and T_1), each driven by its own 6-bit programmable prescaler. The T_1 prescaler can be driven by internal or external clock sources; however, the T_0 prescaler is driven by the internal clock only.

The 6-bit prescalers can divide the input frequency of the clock source by any number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request—IRQ4 (T_0) or IRQ5 (T_1)—is generated.

The counters can be started, stopped, restarted to continue, or restarted from the initial value. The counters can also be programmed to stop upon reaching zero (single-pass mode), or to automatically reload the initial value and continue counting (modulo-n continuous mode). The counters, but not the prescalers, can be read any time without disturbing their value or count mode.

The clock source for T_1 is user-definable and can be the internal microprocessor clock (4 MHz maximum) divided by four, or an external signal input via Port 3. The Timer Mode register configures the external timer input as an external clock (1 MHz maximum), a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the T_0 output to the input of T_1. Port 3 line $P3_6$ also serves as a timer output (T_{OUT}) through which T_0, T_1 or the internal clock can be output.

Interrupts

The Z8 allows six different interrupts from eight sources: the four Port 3 lines $P3_0$-$P3_3$, Serial In, Serial Out, and the two counter/timers. These interrupts are both maskable and prioritized. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority Register.

All Z8 interrupts are vectored. When an interrupt request is granted, the Z8 enters an interrupt machine cycle that disables all subsequent interrupts, saves the program counter and status flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

The Z8 also supports polled systems. To accommodate a polled structure, any or all of the interrupt inputs can be masked and the Interrupt Request Register polled to determine which of the interrupt requests needs service.

Clock

The on-chip oscillator has a high-gain, series-resonant amplifier for connection to a crystal or to any suitable external clock source (XTAL1 = Input, XTAL2 = Output).

The crystal source is connected across XTAL1 and XTAL2, using the recommended capacitors (C_1 = 15 pF) from each pin to ground. The specifications for the crystal are as follows:

- AT cut, series resonant
- Fundamental type, 8 MHz maximum
- Series resistance, $R_S \leq 100\ \Omega$

Power Down Standby Option

The low-power standby mode allows power to be removed without losing the contents of the 124 general-purpose registers. This mode is available to the user as a bonding option whereby pin 2 (normally XTAL2) is replaced by the V_{MM} (standby) power supply input. This necessitates the use of an external clock generator (input = XTAL1) rather than a crystal source.

The removal of power, whether intended or due to power failure, must be preceded by a software routine that stores the appropriate status into the register file. Figure 9 shows the recommended circuit for a battery back-up supply system.

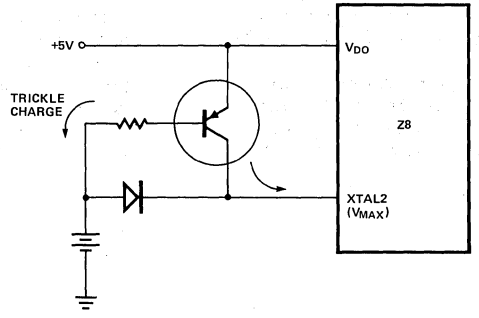


Figure 9. Recommended Driver Circuit for Power Down Operation

Z8-02 Development Device

The 64-pin development version of the 40-pin mask-programmed Z8 allows the user to prototype the system in hardware with an actual Z8 device, and develop the code that is eventually mask-programmed into the on-chip ROM of the Z8-01.

The Z8-02 is identical to the Z8-01 with the following exceptions:

- The internal ROM has been removed
- The ROM address lines and data lines are buffered and brought out to external pins
- Control lines for the new memory have been added

Z8-02 Pin Description

The functions of the Z8-02 I/O lines, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, XTAL1, XTAL2 and $\overline{RESET}$ are identical to those of their Z8-01 counterparts. The functions of the remaining 24 pins are as follows:

A_0-A_{11}. *Program Memory Address* (outputs). A_0-A_{11} access the first 2K bytes of program memory. A_{11} is a reserved pin.

D_0-D_7. *Program Data* (inputs). Program data from the first 2K bytes of program memory is input through pins D_0-D_7.

$\overline{MDS}$. *Program Memory Data Strobe* (output, active Low). $\overline{MDS}$ is Low during an instruction fetch cycle when the first 2K bytes of program memory are being accessed. $\overline{MDS}$ remains High during other program memory read cycles.

$\overline{SYNC}$. *Instruction Sync* (output, active Low). This strobe output is forced Low during the internal clock period preceding the beginning of an opcode fetch.

SCLK. *System Clock* (output). SCLK is the internal clock output through a buffer. The clock rate is equal to one-half the crystal frequency.

IACK. *Interrupt Acknowledge* (output, active High). IACK is driven High in response to an interrupt during the interrupt machine cycle.

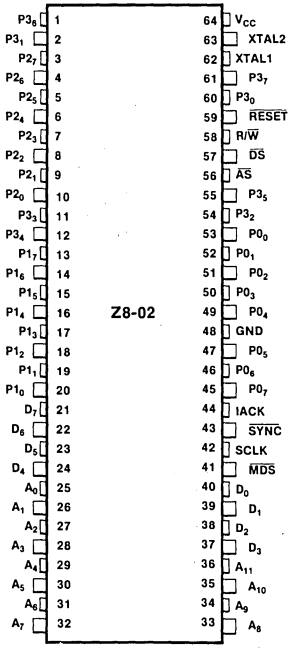


Figure 10. Z8-02 Pin Assignments

Addressing Modes

The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols

dst	Destination location or contents
src	Source location or contents
cc	Condition code (see list)
@	Indirect address prefix
SP	Stack pointer (control registers 254-255)
PC	Program counter
FLAGS	Flag register (control register 252)
RP	Register pointer (control register 253)
IMR	Interrupt mask register (control register 251)

Assignment of a value is indicated by the symbol "←". For example,

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr(n)" is used to refer to bit "n" of a given location. For example,

dst (7)

refers to bit 7 of the destination operand.

Flags

Control Register R252 contains the following six flags:

C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

0	Cleared to zero
1	Set to one
*	Set or cleared according to operation
–	Unaffected
X	Undefined

Condition Codes

Condition Codes			
Value	**Mnemonic**	**Meaning**	**Flags Set**
1000		Always true	---
0111	C	Carry	C = 1
1111	NC	No carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	[Z OR (S XOR V)] = 0
0010	LE	Less than or equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned greater than or equal	C = 0
0111	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1
0000		Never true	---

Instruction Formats

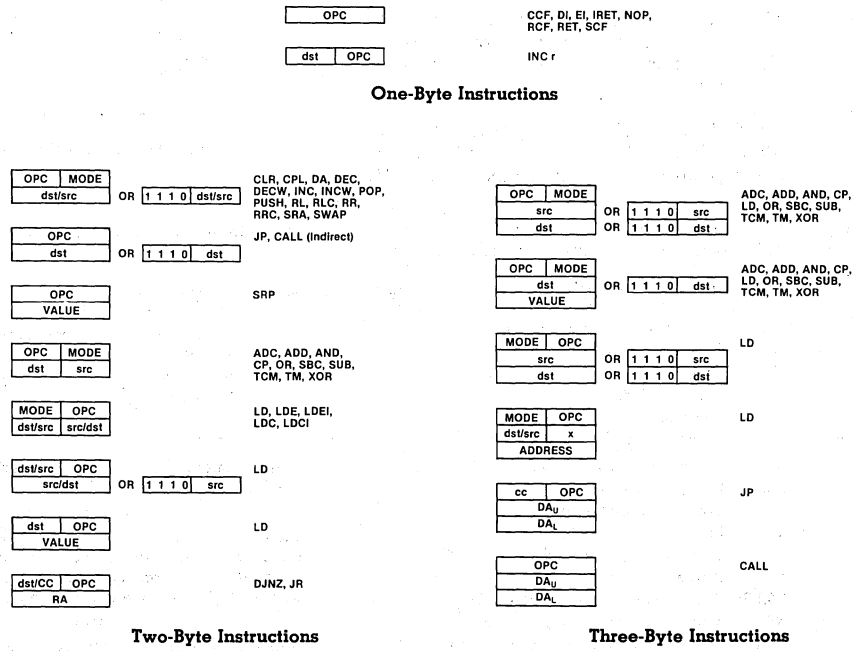
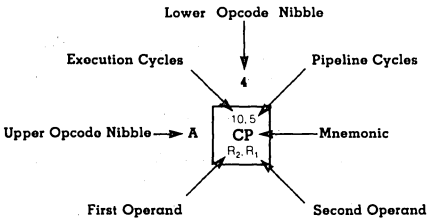


Figure 11. Instruction Formats

Z8 Opcode Map

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6,5 **DEC** R1	6,5 **DEC** IR1	6,5 **ADD** r1,r2	6,5 **ADD** r1,Ir2	10,5 **ADD** R2,R1	10,5 **ADD** IR2,R1	10,5 **ADD** R1,IM	10,5 **ADD** IR1,IM	6,5 **LD** r1,R2	6,5 **LD** r2,R1	12/10,5 **DJNZ** r1,RA	12/10,0 **JR** cc,RA	6,5 **LD** r1,IM	12/10,0 **JP** cc,DA	6,5 **INC** r1	
1	6,5 **RLC** R1	6,5 **RLC** IR1	6,5 **ADC** r1,r2	6,5 **ADC** r1,Ir2	10,5 **ADC** R2,R1	10,5 **ADC** IR2,R1	10,5 **ADC** R1,IM	10,5 **ADC** IR1,IM								
2	6,5 **INC** R1	6,5 **INC** IR1	6,5 **SUB** r1,r2	6,5 **SUB** r1,Ir2	10,5 **SUB** R2,R1	10,5 **SUB** IR2,R1	10,5 **SUB** R1,IM	10,5 **SUB** IR1,IM								
3	8,0 **JP** IRR1	6,1 **SRP** IM	6,5 **SBC** r1,r2	6,5 **SBC** r1,Ir2	10,5 **SBC** R2,R1	10,5 **SBC** IR2,R1	10,5 **SBC** R1,IM	10,5 **SBC** IR1,IM								
4	8,5 **DA** R1	8,5 **DA** IR1	6,5 **OR** r1,r2	6,5 **OR** r1,Ir2	10,5 **OR** R2,R1	10,5 **OR** IR2,R1	10,5 **OR** R1,IM	10,5 **OR** IR1,IM								
5	10,5 **POP** R1	10,5 **POP** IR1	6,5 **AND** r1,r2	6,5 **AND** r1,Ir2	10,5 **AND** R2,R1	10,5 **AND** IR2,R1	10,5 **AND** R1,IM	10,5 **AND** IR1,IM								
6	6,5 **COM** R1	6,5 **COM** IR1	6,5 **TCM** r1,r2	6,5 **TCM** r1,Ir2	10,5 **TCM** R2,R1	10,5 **TCM** IR2,R1	10,5 **TCM** R1,IM	10,5 **TCM** IR1,IM								
7	10/12,1 **PUSH** R2	12/14,1 **PUSH** IR2	6,5 **TM** r1,r2	6,5 **TM** r1,Ir2	10,5 **TM** R2,R1	10,5 **TM** IR2,R1	10,5 **TM** R1,IM	10,5 **TM** IR1,IM								
8	10,5 **DECW** RR1	10,5 **DECW** IR1	12,0 **LDE** r1,Irr2	18,0 **LDEI** Ir1,Irr2												6,1 **DI**
9	6,5 **RL** R1	6,5 **RL** IR1	12,0 **LDE** r2,Irr1	18,0 **LDEI** Ir2,Irr1												6,1 **EI**
A	10,5 **INCW** RR1	10,5 **INCW** IR1	6,5 **CP** r1,r2	6,5 **CP** r1,Ir2	10,5 **CP** R2,R1	10,5 **CP** IR2,R1	10,5 **CP** R1,IM	10,5 **CP** IR1,IM								14,0 **RET**
B	6,5 **CLR** R1	6,5 **CLR** IR1	6,5 **XOR** r1,r2	6,5 **XOR** r1,Ir2	10,5 **XOR** R2,R1	10,5 **XOR** IR2,R1	10,5 **XOR** R1,IM	10,5 **XOR** IR1,IM								16,0 **IRET**
C	6,5 **RRC** R1	6,5 **RRC** IR1	12,0 **LDC** r1,Irr2	18,0 **LDCI** Ir1,Irr2				10,5 **LD** r1,x,R2								6,5 **RCF**
D	6,5 **SRA** R1	6,5 **SRA** IR1	12,0 **LDC** r2,Irr1	18,0 **LDCI** Ir2,Irr1	20,0 **CALL*** IRR1		20,0 **CALL** DA	10,5 **LD** r2,x,R1								6,5 **SCF**
E	6,5 **RR** R1	6,5 **RR** IR1		6,5 **LD** r1,Ir2	10,5 **LD** R2,R1	10,5 **LD** IR2,R1	10,5 **LD** R1,IM	10,5 **LD** IR1,IM								6,5 **CCF**
F	6,7 **SWAP** R1	6,7 **SWAP** IR1		6,5 **LD** Ir1,r2		10,5 **LD** R2,IR1										6,0 **NOP**
Bytes Per Instruction	2				3				2					3	1	



Legend:
R = 8-Bit Address
r = 4-Bit Address
R_1 or r_1 = Dst Address
R_2 or r_2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank areas are reserved instructions.

*2-byte instruction; fetch cycle appears as a 3-byte instruction.

Instruction Summary

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
ADC dst,src dst ← dst + src + C	(Note 1)		1□	* * * * 0 *
ADD dst,src dst ← dst + src	(Note 1)		0□	* * * * 0 *
AND dst,src dst ← dst AND src	(Note 1)		5□	- * * 0 - -
CALL dst SP ← SP - 2 @SP ← PC; PC ← dst	DA IRR		D6 D4	- - - - - -
CCF C ← NOT C			EF	* - - - - -
CLR dst dst ← 0	R IR		B0 B1	- - - - - -
COM dst dst ← NOT dst	R IR		60 61	- * * 0 - -
CP dst,src dst - src	(Note 1)		A□	* * * * - -
DA dst dst ← DA dst	R IR		40 41	* * * X - -
DEC dst dst ← dst - 1	R IR		00 01	- * * * - -
DECW dst dst ← dst - 1	RR IR		80 81	- * * * - -
DI IMR (7) ← 0			8F	- - - - - -
DJNZ r,dst r ← r - 1 if r ≠ 0 PC ← PC + dst Range: +127, -128	RA		rA r=0-F	- - - - - -
EI IMR (7) ← 1			9F	- - - - - -
INC dst dst ← dst + 1	r R IR		rE r=0-F 20 21	- * * * - -
INCW dst dst ← dst + 1	RR IR		A0 A1	- * * * - -
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR (7) ← 1			BF	* * * * * *
JP cc,dst if cc is true PC ← dst	DA IRR		cD c=0-F 30	- - - - - -
JR cc,dst if cc is true, PC ← PC + dst Range: +127, -128	RA		cB c=0-F	- - - - - -
LD dst,src dst ← src	r r R r X r Ir R R R IR IR	IM R r X r Ir r R IR IM IM R	rC r8 r9 r=0-F C7 D7 E3 F3 E4 E5 E6 E7 F5	- - - - - -
LDC dst,src dst ← src	r Irr	Irr r	C2 D2	- - - - - -
LDCI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	C3 D3	- - - - - -
LDE dst,src dst ← src	r Irr	Irr r	82 92	- - - - - -

Instruction and Operation	Addr Mode dst	Addr Mode src	Opcode Byte (Hex)	Flags Affected C Z S V D H
LDEI dst,src dst ← src r ← r + 1; rr ← rr + 1	Ir Irr	Irr Ir	83 93	- - - - - -
NOP			FF	- - - - - -
OR dst,src dst ← dst OR src	(Note 1)		4□	- * * 0 - -
POP dst dst ← @SP SP ← SP + 1	R IR		50 51	- - - - - -
PUSH src SP ← SP - 1; @SP ← src		R IR	70 71	- - - - - -
RCF C ← 0			CF	0 - - - - -
RET PC ← @SP; SP ← SP + 2			AF	- - - - - -
RL dst	R IR		90 91	* * * * - -
RLC dst	R IR		10 11	* * * * - -
RR dst	R IR		E0 E1	* * * * - -
RRC dst	R IR		C0 C1	* * * * - -
SBC dst,src dst ← dst - src - C	(Note 1)		3□	* * * * 1 *
SCF C ← 1			DF	1 - - - - -
SRA dst	R IR		D0 D1	* * * 0 - -
SRP src RP ← src		IM	31	- - - - - -
SUB dst,src dst ← dst - src	(Note 1)		2□	* * * * 1 *
SWAP dst	R IR		F0 F1	X * * X - -
TCM dst,src (NOT dst) AND src	(Note 1)		6□	- * * 0 - -
TM dst,src dst AND src	(Note 1)		7□	- * * 0 - -
XOR dst,src dst ← dst XOR src	(Note 1)		B□	- * * 0 - -

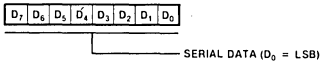
Note 1

These instructions have an identical set of addressing modes, which are encoded for brevity in this table. The higher opcode nibble is found in the instruction set table above. The lower nibble is expressed symbolically by a □ in the table above, and its value is found in the following table to the right of the applicable addressing mode pair.

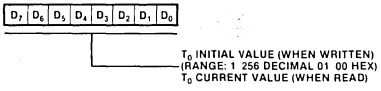
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Addr Mode dst	Addr Mode src	Lower Opcode Nibble
r	r	2
r	Ir	3
R	R	4
R	IR	5
R	IM	6
IR	IM	7

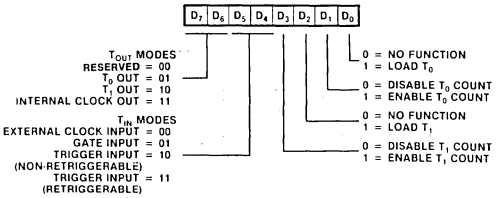
R240 SIO
Serial I/O Register
($F0_H$; Read/Write)



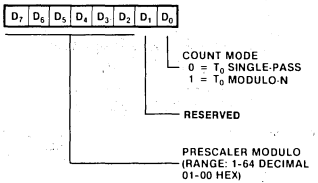
R244 T0
Counter/Timer 0 Register
($F4_H$; Read/Write)



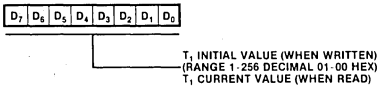
R241 TMR
Timer Mode Register
($F1_H$; Read/Write)



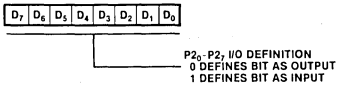
R245 PRE0
Prescaler 0 Register
($F5_H$; Write Only)



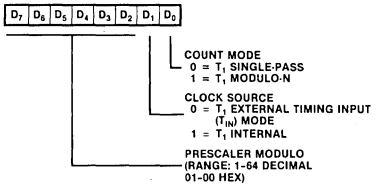
R242 T1
Counter Timer 1 Register
($F2_H$; Read/Write)



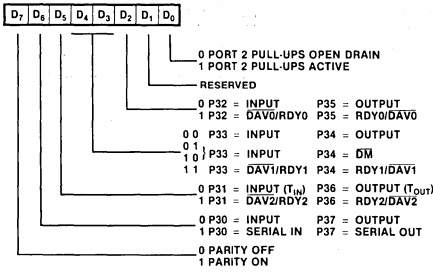
R246 P2M
Port 2 Mode Register
($F6_H$; Write Only)



R243 PRE1
Prescaler 1 Register
($F3_H$; Write Only)

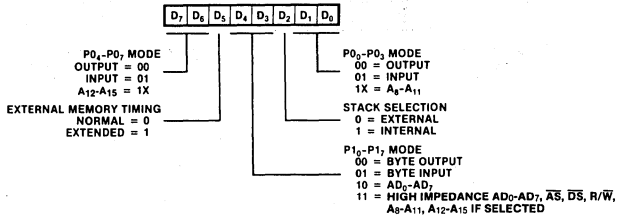


R247 P3M
Port 3 Mode Register
($F7_H$; Write Only)

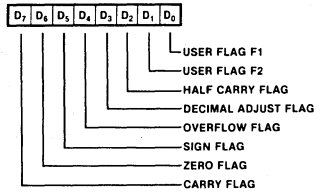


Z8 Control Registers

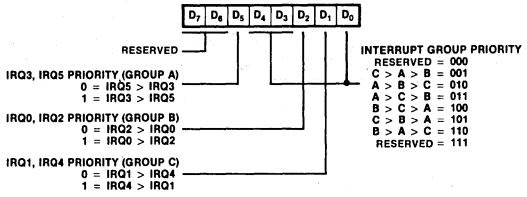
R248 P01M
Port 0 and 1 Mode Register
($F8_H$; Write Only)



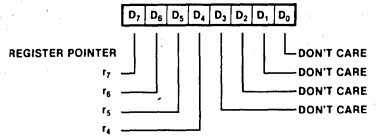
R252 FLAGS
Flag Register
(FC_H; Read/Write)



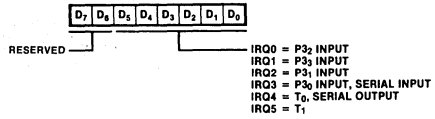
R249 IPR
Interrupt Priority Register
($F9_H$; Write Only)



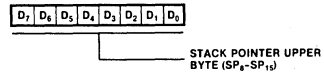
R253 RP
Register Pointer
(FD_H; Read/Write)



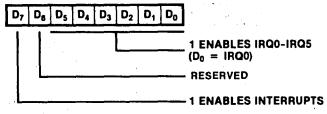
R250 IRQ
Interrupt Request Register
(FA_H; Read/Write)



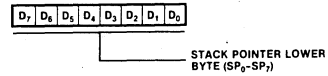
R254 SPH
Stack Pointer
(FE_H; Read/Write)



R251 IMR
Interrupt Mask Register
(FB_H; Read/Write)



R255 SPL
Stack Pointer
(FF_H; Read/Write)



Z8 Control Registers

Absolute Maximum Ratings

Voltages on all inputs and outputs with respect to GND . . . . . -0.3 V to +7.0 V
Operating Ambient Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

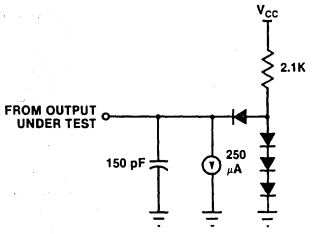
- □ +4.75 V ≤ V_{CC} ≤ +5.25 V
- □ GND = 0 V
- □ 0°C ≤ T_A ≤ +70°C

DC Characteristics

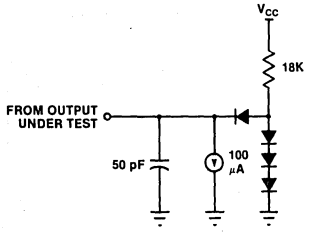
Symbol	Parameter	Min	Max	Unit	Condition	Notes
V_{CH}	Clock Input High Voltage	3.8	V_{CC}	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	-0.3	0.8	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0	V_{CC}	V		
V_{IL}	Input Low Voltage	-0.3	0.8	V		
V_{RH}	Reset Input High Voltage	3.8	V_{CC}	V		
V_{RL}	Reset Input Low Voltage	-0.3	0.8	V		
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA	1
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = +2.0 mA	1
I_{IL}	Input Leakage		±10	μA	$0V \le V_{IN} \le +5.25V$	
I_{OL}	Output Leakage		±10	μA	$0V \le V_{IN} \le +5.25V$	
I_{IR}	Reset Input Current		-50	μA	V_{CC} = +5.25 V, V_{RL} = 0 V	
I_{CC}	V_{CC} Supply Current		180	mA	V_{CC} = 5.25V	
I_{MM}	V_{MM} Supply Current		10	mA	Power Down Mode	
V_{MM}	Backup Supply Voltage	3.0	V_{CC}	V	Power Down Mode	

1. For A_0-A_{11}, $\overline{MDS}$, $\overline{SYNC}$, SCLK and IACK on the Z8-02 version, I_{OH} = -100 μA and I_{OL} = 1.0 mA.

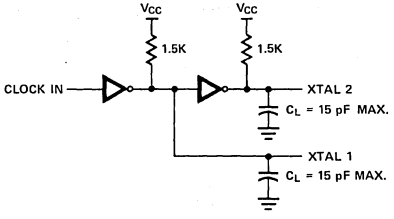
Test Load Circuits



Test Load 1



Test Load 2



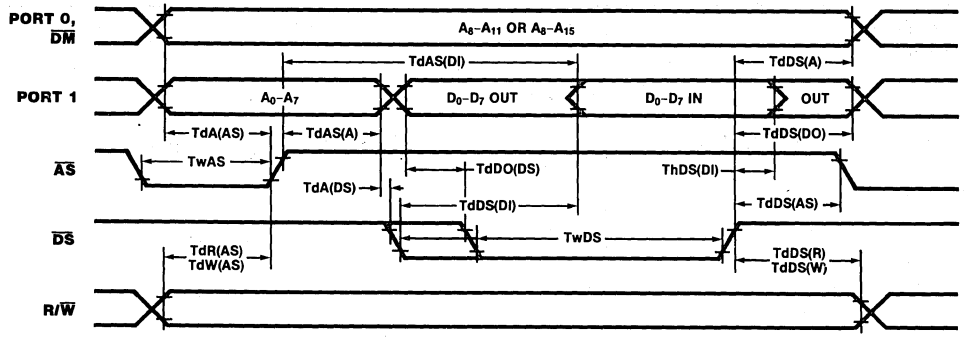
External Clock Interface Circuit

MICRO PROCESSORS

External I/O or Memory Read and Write Cycle

Symbol	Parameter	Min	Max	Unit	Condition	Notes
TdA(AS)	Address Valid to Address Strobe Delay	50		ns	Test Load 1	1
TdAS(A)	Address Strobe to Address Float Delay	60		ns	Test Load 1	1
TdAS(DI)	Address Strobe to Data In Valid Delay		320	ns	Test Load 1	3
TwAS	Address Strobe Width	80		ns	Test Load 1	1
TdA(DS)	Address Float to Data Strobe Delay	0		ns	Test Load 1	
TwDS	Data Strobe Width (Read) (Write)	250 160		ns	Test Load 1	2
TdDS(DI)	Data Strobe to Data In Valid Delay		200	ns	Test Load 1	3
ThDS(DI)	Data In Hold Time	0		ns		
TdDS(A)	Data Strobe to Address Change Delay	80		ns	Test Load 1	1
TdDS(AS)	Data Strobe to Address Strobe Delay	70		ns	Test Load 1	1
TdR(AS)	Read Valid to Address Strobe Delay	50		ns	Test Load 1	1
TdDS(R)	Data Strobe to Read Change Delay	60		ns	Test Load 1	1
TdDO(DS)	Data Out Valid to Data Strobe Delay	50		ns	Test Load 1	1
TdDS(DO)	Data Strobe to Data Out Change Delay	80		ns	Test Load 1	1
TdW(AS)	Write Valid to Address Strobe Delay	50		ns	Test Load 1	1
TdDS(W)	Data Strobe to Write Change Delay	60		ns	Test Load 1	1

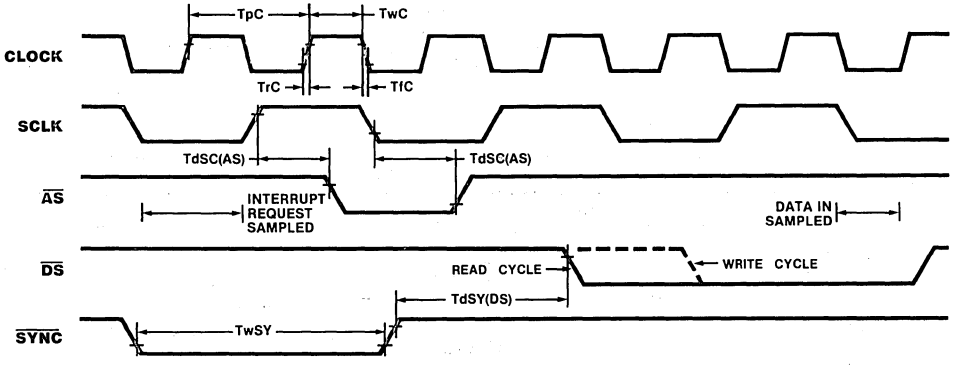
1. Delay times are specified for an input clock frequency of 8 MHz. When operating at a lower frequency, the increase in input clock period must be added to the specified delay time.
2. Data Strobe Width is specified for an input clock frequency of 8 MHz. When operating at a lower frequency, the increase in *three* input clock periods must be added to the specified width. Data Strobe Width varies according to the instruction being executed.
3. Address Strobe and Data Strobe to Data In Valid delay times represent memory system access times and are given for an 8 MHz crystal input frequency. For lower frequencies; the change in four clock periods must be added to TdAS(DI) and the change in three clock periods added to TdDS(DI).
4. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0."



Additional Timing

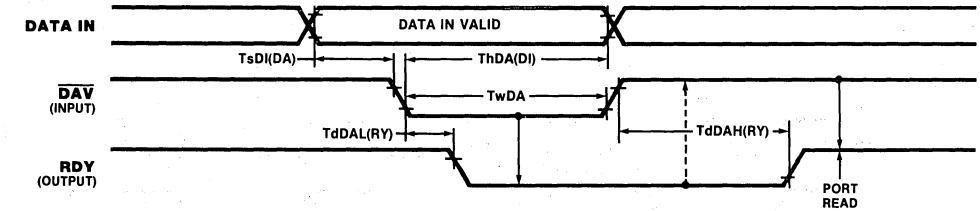
Symbol	Parameter	Min	Max	Unit	Condition	Notes
TpC	Input Clock Period	125	1000	ns		
TrC, TfC	Input Clock Rise and Fall Times		25	ns	From External Clock Generator	
TwC	Input Clock Width	37		ns	From External Clock Generator	
TdSC(AS)	System Clock Out to Address Strobe Delay Time			ns		1
TdSY(DS)	Instruction Sync Out to Data Strobe Delay Time	200		ns		1, 2
TwSY	Instruction Sync Out Width	160		ns		1, 2
TwI	Width of Interrupt Request via Port 3 Input	100		ns		

1. Test Conditions use Test Load 1 for SCLK when output through Port 3 and Test Load 2 on the SCLK and $\overline{SYNC}$ direct outputs on the Z8-02.
2. Times given assume an 8 MHz crystal input frequency. For lower frequencies, the change in two clock periods must be added.
3. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0."

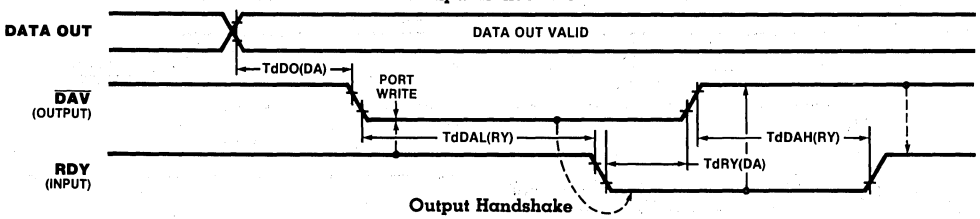


Handshake Timing

Symbol	Parameter	Min	Max	Unit	Condition
TsDI(DA)	Data In Setup Time	0		ns	
ThDA(DI)	Data In Hold Time	230		ns	
TwDA	Data Available Width	175		ns	Input Handshake Test Load 1
TdDAL(RY)	Data Available Low to Ready Delay Time	20	175	ns	Input Handshake Test Load 1
		0		ns	Output Handshake Test Load 1
TdDAH(RY)	Data Available High to Ready Delay Time		150	ns	Input Handshake Test Load 1
		0		ns	Output Handshake Test Load 1
TdDO(DA)	Data Out to Data Available Delay Time	50		ns	Test Load 1
TdRY(DA)	Ready to Data Available Delay Time	0	205	ns	Test Load 1



Input Handshake

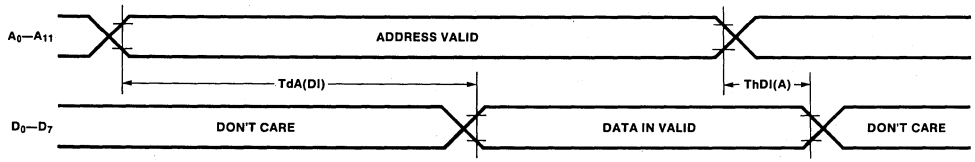


Output Handshake

Z8-02, -03 Memory Port Timing

Symbol	Parameter	Min	Max	Unit	Condition
TdA(DI)	Address Valid to Data In Valid Delay Time		460	ns	Test Load 2
ThDI(A)	Data In Hold Time	0		ns	

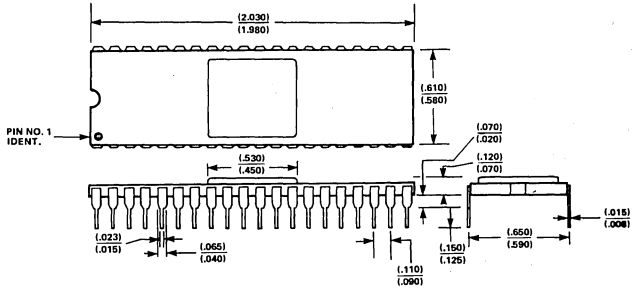
1. Delay times are specified for an input clock frequency of 8 MHz.
2. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0."



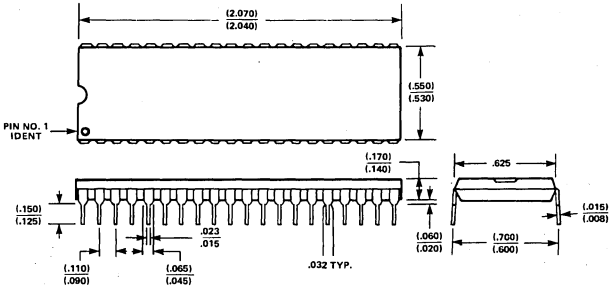
Ordering Information

Part Number	Temperature Range	Number of Pins	Package	Description
Z8-01 PS	0°C to +70°C	40	Plastic	8-Bit Single-Chip Microcomputer Circuit
Z8-01 CS	0°C to +70°C	40	Ceramic	8-Bit Single-Chip Microcomputer Circuit
Z8-02 QS	0°C to +70°C	64	Ceramic	8-Bit Microcomputer Development Device
Z8-03 RS	0°C to +70°C	40	Ceramic	8-Bit Microcomputer Protopack Emulator

Package Information



40-Pin Ceramic Package Dimensions (CS Package)



40-Pin Plastic Package Dimensions (PS Package)

Notice: Z8 and Z-bus are trademarks of Zilog, Inc.

Microcomputer Protopack™-Emulator

Z8™-03

PRODUCT SPECIFICATION

PRELIMINARY

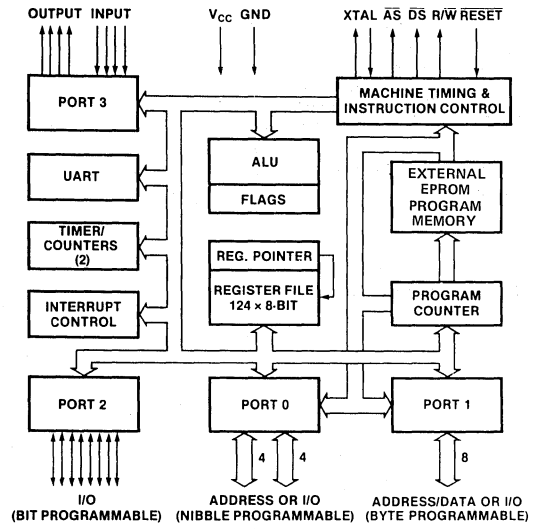
SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Prototyping version of Synertek Z8.
- Piggyback 2716 EPROM program memory.
- Pin-compatible with Z8-01 masked-ROM for hardware debugging or low-volume production.
- Complete microcomputer on-chip
  - 128 bytes of on-chip data RAM
  - 32 I/O lines
  - Socket for 2716 2Kx8 EPROM
- Two 14-bit counter/timers.
- Duplex UART and baud-rate generator.
- Vectored priority interrupt system.
- Up to 62K of external data memory.
- Up to 62K of external program memory.
- On-chip crystal, RC, or LC oscillator.
- High-speed instruction execution.
  - Working-register operations = 1.5μs
  - Average instruction = 2.2μs
- Single +5V supply voltage.
- All inputs/outputs TTL compatible.

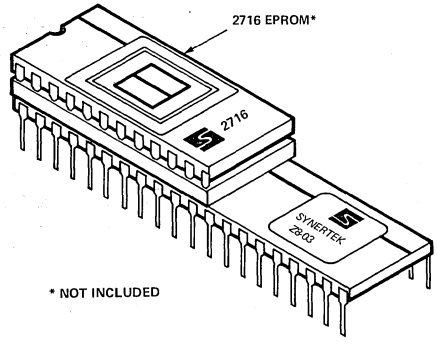
MICRO-PROCESSORS

The Synertek Z8-03 Microcomputer Protopack Emulator is a ROM-less version of the Synertek Z8 single-chip microcomputer. A removable 2716 EPROM plugged into the 24-pin "piggy-back" socket atop the Z8-03 allows pin-compatible emulation of the Z8-01 masked-ROM version.

BLOCK DIAGRAM



PACKAGE DRAWING



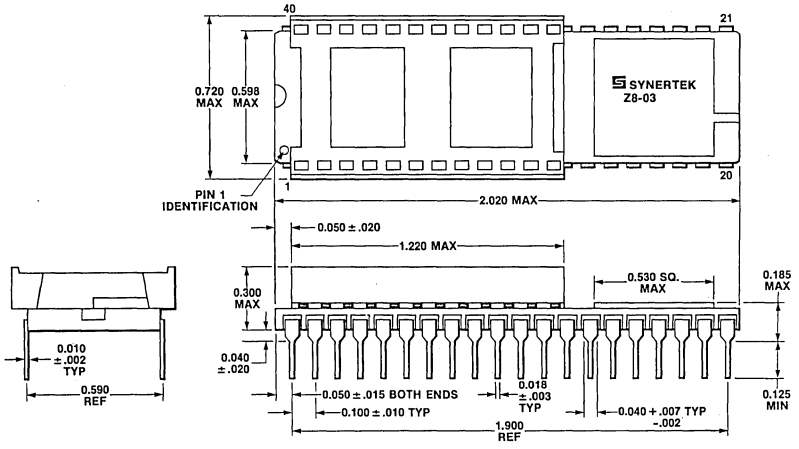
* NOT INCLUDED

Z8 and Protopack are trademarks of Zilog, Inc.

Ordering Information

Part Number	Temperature Range	Number of Pins	Package	Description
Z8-03 RS	0°C to +70°C	40	Ceramic	8-Bit Microcomputer Protopack Emulator

Package Information



MICRO-PROCESSORS

Floppy Disk Controller (FDC)

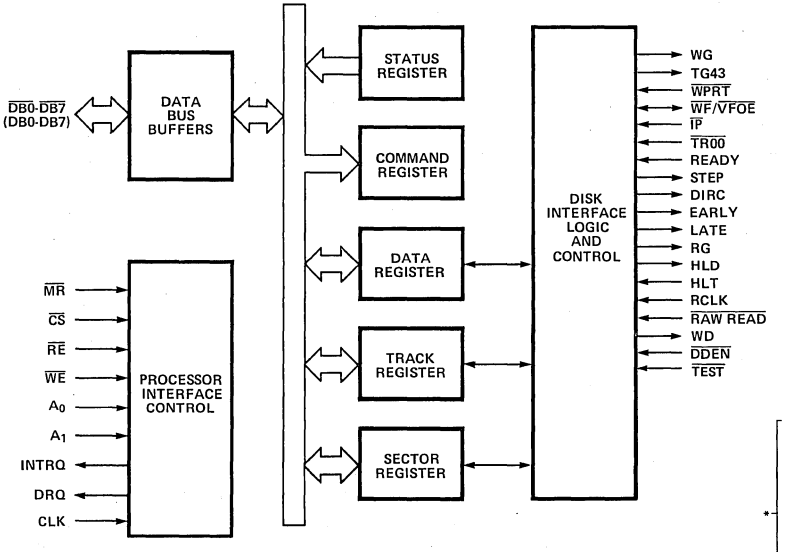
SY1791-02/SY1793-02

MICROPROCESSOR PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Pin and function compatible with Western-Digital FD1791-02 and FD1793-02
- Single 5-volt power supply
- Accommodates both Single Density (FM) and Double Density (MFM) formats
- IBM format compatibility:
  IBM 3740 Single-Density
  IBM System-34 Double-Density
- Numerous automatic control functions

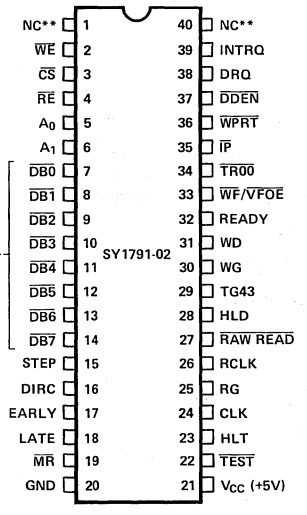
The SY1791-02/SY1793-02 Floppy Disk Controller is a fully programmable device intended for microprocessor based systems. Autonomous operation permits complete control of floppy disk functions with minimum CPU intervention required. Programmability is provided to allow either single-density (FM) or double-density (MFM) formats compatible with IBM standards, or formats uniquely defined by the user. The SY1791-02 uses negative-true data bus logic; the SY1793-02 uses positive-true.



( ) DENOTES SY1793-02 SIGNALS

Figure 1. SY1791-02/SY1793-02 Block Diagram

PIN ASSIGNMENTS



*1793-02 HAS POSITIVE-TRUE DATA BUS LOGIC.

**NC PINS ARE INTERNALLY OPEN CIRCUITED. VOLTAGES APPLIED TO THESE PINS HAVE NO AFFECT.

ORDERING INFORMATION

PART NUMBER	PACKAGE	DATA BUS LOGIC
SYC1791-02	CERAMIC	NEGATIVE-TRUE
SYD1791-02	CERDIP	NEGATIVE-TRUE
SYP1791-02	PLASTIC	NEGATIVE-TRUE
SYC1793-02	CERAMIC	POSITIVE-TRUE
SYD1793-02	CERDIP	POSITIVE-TRUE
SYP1793-02	PLASTIC	POSITIVE-TRUE

DETAILED LIST OF FEATURES

- Replaces Western-Digital FD1791-02 and FD1793-02
- Single 5-volt power supply
- 40-pin DIP package
- Automatic track seek with verification
- Accommodates single-density (FM) and double-density (MFM) formats
- Soft-sector format compatibility
- IBM 3740 (single-density) and System 34 (double-density) compatible
- Single or multiple record read with automatic sector search or entire track read
- Selectable record length (128, 256, 512, 1024 bytes)
- Single or multiple record write with automatic sector search
- Entire track write for initialization
- Programmable Controls
  - Selectable track-to-track stepping time
  - Selectable head settling and engage times
  - Head position verification
  - Side verification
- Double-buffered read and write data flow
- DMA or programmed data transfers
- TTL-compatible inputs and outputs
- Write precompensation (FM and MFM)
- Comprehensive Status Register

1.0 GENERAL DESCRIPTION

1.1 Functional Blocks in the SY1791-02/SY1793-02

The SY1791-02/SY1793-02 Floppy Disk Controller (FDC) consists of several functional sections, as shown in Figure 1. Detailed operation of each section is described below.

- DATA REGISTER (DR) — This 8-bit read/write register is used as a holding register during Disk Read and Write operations. During Disk Read operations, serial data is assembled in the Data Shift Register then transferred in parallel to the DR, where it is made available to the data bus. In a Disk Write operation, parallel data is transferred from the data bus to the DR to await transfer to the Data Shift Register. The DR is also used, while executing a Seek command, to hold the Track address.
- TRACK REGISTER (TR) — This 8-bit read/write register holds the track number of the current Read/Write head position. It can be incremented (decremented) by one each time the head is stepped in (out), toward track 76 (00). The TR's contents are compared with the track number (recorded in the disk's ID field) during Read, Write, or Verify operations. This register should not be loaded when the device is busy.
- SECTOR REGISTER (SR) — This 8-bit read/write register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. This register should not be loaded when the device is busy.
- COMMAND REGISTER (CR) — This 8-bit write only register holds the command which is being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This is accomplished with the Interrupt command.
- STATUS REGISTER (STR) — This 8-bit read only register holds device status information. The meaning of the STR bits is a function of the contents of the Command Register.
- DATA SHIFT REGISTER (DSR) — As part of the Disk Interface Logic and Control, this 8-bit register assembles serial data from $\overline{\text{RAW READ}}$ input during READ operations, prior to transfer to the DR. During WRITE operations it accepts parallel data from the DR and serially transfers it to the Write Data output.
- CRC LOGIC — This logic, part of Disk Interface Logic and Control, does the checking or the generating of the 16-bit Cyclic Redundancy Check (CRC). The polynominal is: $G(X) = X^{16} + X^{12} + X^5 + 1$. The CRC logic checks all information, starting with the address mark, up to the CRC characters. The CRC register is preset to ones before data is shifted through the circuit.
- ARITHMETIC/LOGIC UNIT (ALU) — A part of Disk Interface Logic and Control, the ALU does serial comparisons, increments, and decrements. It is used for register modification and comparisons with the ID field recorded on the disk.
- TIMING AND CONTROL — All Processor and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external clock.
- AM DETECTOR — The Address Mark Detector, part of Disk Interface Logic and Control, detects ID, Data and Index Address Marks during read and write operations.

1.2 MPU Interface Pin Functions

- MASTER RESET ($\overline{\text{MR}}$) — A low on this input resets the device and loads hex 03 into the command register. The Not Ready status bit (status bit 7) is reset during $\overline{\text{MR}}$ low. When $\overline{\text{MR}}$ is driven high, a Restore command is executed regardless of the state of the Ready signal, and hex 01 is loaded into the Sector Register.
- CHIP SELECT ($\overline{\text{CS}}$) — A low level on this input selects the FDC and enables processor communications with the FDC.
- DATA BUS LINES ($\overline{\text{DB0}}$-$\overline{\text{DB7}}$ on SY1791-02 and DB0-DB7 on SY1793-02) — Bi-directional data bus used for transfer of data between the system MPU and the FDC (negative-true for the SY1791-02, positive-true for the SY1793-02).

- REGISTER ADDRESS LINES (A0-A1) — These inputs address the internal registers for access by the Data Bus lines under $\overline{RE}$ and $\overline{WE}$ control.

REGISTER ADDRESS CODES

A1	A0	READ	WRITE
0	0	STATUS	COMMAND
0	1	TRACK	
1	0	SECTOR	
1	1	DATA	

- READ ENABLE ($\overline{RE}$) — If $\overline{CS}$ is low, a low on this input enables the addressed internal register to output data onto the data bus.
- WRITE ENABLE ($\overline{WE}$) — If $\overline{CS}$ is low, then a low on this input gates data from the data bus into the addressed register.
- INTERRUPT REQUEST (INTRQ) — This open drain output is set high at the completion or termination of any operation and is reset when a new command is loaded into the Command Register or when the Status Register is read. Use 10KΩ pull-up resistor to V_{CC}.
- DATA REQUEST (DRQ) — DRQ is an open drain output. DRQ high during read operations indicates that the Data Register (DR) contains data. When high during write operations, DRQ indicates that the DR is empty and ready to be loaded. DRQ is reset by reading or loading the DR during read or write operations, respectively. Use 10K pull-up resistor to V_{CC}.
- CLOCK (CLK) — This input requires a square wave clock for internal timing reference (2 MHz for 8-inch drives, 1 MHz for 5-inch drives).

1.3 Floppy Disk Interface Pin Functions

- READ GATE (RG) — A high on this output indicates that a field of zeroes (zeroes or ones) has been detected in FM (MFM) encoded information. This can be used to indicate to a data separator that a sync field has been found.
- WRITE DATA (WD) — This output to the disk drive electronics supplies one pulse per required flux transition.
- READ CLOCK (RCLK) — The RCLK input is a nominal square-wave clock signal derived from the data stream. Phasing (RCLK relative to $\overline{RAW\ READ}$) is important, but polarity (RCLK high or low) is not.
- RAW READ ($\overline{RAW\ READ}$) — This is the data input to the FDC from the drive. This input must be a negative pulse for each recorded flux transition.
- HEAD LOAD (HLD) — The HLD output notifies the drive to engage the Read/Write head against the medium.
- HEAD LOAD TIMING (HLT) — The HLT input, which is generated by external logic, indicates that a sufficient time has elapsed for the head to have engaged.
- STEP — The step output provides a pulse to the disk drive electronics to cause each incremental head movement.
- DIRECTION (DIRC) — The DIRC output defines the direction of the step. It is high for stepping the head in towards track 76, and low for stepping the head out towards track 0.
- EARLY — A high EARLY output indicates to external circuitry that the WD pulse should be shifted early for write precompensation.
- LATE — A high LATE output indicates to external circuitry that the WD pulse should be shifted late for write precompensation.
- TRACK GREATER THAN 43 (TG43) — This output informs the drive that the Read/Write head is positioned between tracks 44-255 inclusive. This output is valid during Read and Write commands.
- WRITE GATE (WG) — The WG output is set high when writing to the disk if all the Write prerequisites have been met. WG is used to enable the drive's write circuitry.
- READY — This input indicates disk readiness to perform any Read or Write command. READY must he high for a Read or Write command to be accepted. If READY is low and the FDC receives any such command, the command is not executed and an interrupt is generated if the Not-Ready status bit is set.
- WRITE FAULT ($\overline{WF}$)/VFO ENABLE ($\overline{VFOE}$) — This pin is used as both an input and output. During Write operations after WG is high, this pin acts as an input to sense a negative transition indicating a Write Fault. If a Write Fault is detected, the Write command is terminated, the Write Fault status bit is set, and INTRQ goes high.

  During Read operations, $\overline{WE/VFOE}$ is an output used to synchronously control external RCLK circuitry. $\overline{VFOE}$ will go true (low) when the following are all true:
  1. HLD and HLT are true;
  2. settling time, if programmed, has expired;
  3. the SY1791-02/SY1793-02 is inspecting data from the disk.
- TRACK 00 ($\overline{TR00}$) — This input, when low, indicates to the FDC that the Read/Write head is positioned over track Ø.
- INDEX PULSE ($\overline{IP}$) — This input is generated by the drive electronics to indicate the start of a track.
- WRITE PROTECT ($\overline{WPRT}$) — This input is sampled whenever a Write command is received. A low terminates the command and sets the Write Protect status bit.
- DOUBLE DENSITY ($\overline{DDEN}$) — This input selects either single or double density operation. When $\overline{DDEN}$ is low, double density is selected. When $\overline{DDEN}$ is high, single density is selected.
- TEST ($\overline{TEST}$) — This input is used for testing purposes and should be tied to +5V, or left open, by the user unless interfacing to voice coil motors. When low, the motor stepping rate is increased (see Figure 3b).

2.0 FUNCTIONAL OPERATION

2.1 Single/Double Density Selection

The SY1791-02/SY1793-02 has two selectable data densities, determined by input $\overline{DDEN}$.

2.2 Clock Selection

In addition to $\overline{DDEN}$, the CLK input determines overall circuit timings, and must be properly selected. A 1MHz CLK input is normally used for 5" mini-diskette drives and 2MHz for standard 8" drives.

2.3 DRQ Operation

The DRQ output indicates that a data transfer operation is required. For disk read operations, DRQ signifies that the Data Register needs to be read so that the next data byte can be received. For disk write operations, DRQ signifies that a data byte has been transmitted and another must be entered. DRQ may be used as a "handshake" control signal in a DMA based system.

2.4 DMA Sequences

In disk read operations, DRQ goes high when a serial data byte is assembled in the Data Register. DRQ is reset when the byte is read by the DMA controller (or system processor). If a newly assembled byte is transferred into the DR (from the DSR) before the DR has been read, then the overwritten byte in the DR is lost. Furthermore, the Lost Data status bit in the Status Register is set, to indicate this condition. Read operations continue until the end of sector is encountered.

Disk write operations are similar. DRQ is activated when the data byte is transferred from the Data Register to the Data Shift Register, indicating that the DR is ready to be loaded with another byte. It is cleared when the new byte is loaded by the DMA controller (or system processor). However, if the new byte is not loaded by the time the prior byte is shifted out, then a byte of all zeroes is written on the diskette and the Lost Data status bit in the Status Register is set.

2.5 Disk Read Operations

For disk read operations, the FDC requires $\overline{\text{RAW READ}}$ and RCLK inputs. $\overline{\text{RAW READ}}$ is a low going pulse for each flux transition. The FDC detects the rising and falling edges of RCLK and uses these edges to frame $\overline{\text{RAW READ}}$ data/clock inputs. RCLK is provided by some drives, but if not it must be provided externally (phase-lock-loops, one-shots, counters, etc.) To assist in generating RCLK, the FDC has a RG (Read Gate) output, which may be used to acquire synchronization. Whenever two bytes of zeroes are detected in read operations (in single-density mode), RG is activated (high) and the FDC must find a valid AM (Address Mark) within the next 10 bytes. If the AM is not found, RG is deactivated (low) and the search for two bytes of zeroes is re-started. If the AM is found, RG remains active as long as the FDC is deriving data from the diskette. For double-density mode, RG is activated when 4 bytes of hex ØØ or hex FF are detected and the FDC must find the AM within 16 bytes.

2.6 Disk Write Operations

The fundamental signals in write operations are: WD (Write Data) output, WG (Write Gate) output, $\overline{\text{WPRT}}$ (Write Protect) input, and $\overline{\text{WF}}$ (Write Fault) input. When writing to the diskette, WG goes high enabling the disk drive write electronics. However, WG will not be activated until the first data byte has been loaded in the Data Register. This ensures that false writing will not occur. Writing is inhibited when $\overline{\text{WPRT}}$ is low. This sets the Write Protect status bit and an interrupt (INTRQ) is generated.

The $\overline{\text{WF}}$ input signifies a fault condition at the disk drive. When low, it causes the current command to terminate, sets the Write Fault bit in the Status Register, and generates the INTRQ interrupt.

2.7 Write Precompensation

EARLY and LATE are two additional signals which are generated by the SY1791-02/SY1793-02 during write operations. They are used for write precompensation functions. Both signals are active-high. The EARLY signal is active when the WD pulse is to be written early; the LATE signal is active when WD is to be written late. If neither signal is active, then WD is to be written at its normal time. EARLY and LATE are valid for both single and double density modes.

3.0 COMMAND WORDS

The FDC accepts eleven commands. Command words should be loaded in the Command Register only when the Busy status bit (status bit Ø) is low. The sole exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Figure 2.

		BIT							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	RESTORE	0	0	0	0	h	V	r_1	r_0
	SEEK	0	0	0	1	h	V	r_1	r_0
	STEP	0	0	1	u	h	V	r_1	r_0
	STEP IN	0	1	0	u	h	V	r_1	r_0
	STEP OUT	0	1	1	u	h	V	r_1	r_0
II	READ SECTOR	1	0	0	m	S	E	C	0
	WRITE SECTOR	1	0	1	m	S	E	C	a_0
III	READ ADDRESS	1	1	0	0	0	E	0	0
	READ TRACK	1	1	1	0	0	E	0	0
	WRITE TRACK	1	1	1	1	0	E	0	0
IV	FORCE INTERRUPT	1	1	0	1	I_3	I_2	I_1	I_0

1 = HIGH LEVEL 0 = LOW LEVEL

Figure 2. Command Summary

3.1 Type I Commands

The Type I commands are Restore, Seek, Step, Step-In, and Step-Out.

- RESTORE — The RESTORE command is used to position the Read/Write head to track Ø of the diskette. Upon the receipt of this command, the $\overline{\text{TR00}}$ input is sampled. If $\overline{\text{TR00}}$ is low, indicating the Read/Write head is positioned over track Ø, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not low, step pulses at a rate specified by the r_1r_0 field are issued until the $\overline{\text{TR00}}$ input is asserted. At this time, the TR is loaded with zeroes and an interrupt is generated. If the $\overline{\text{TR00}}$ input does not go low after 255 stepping pulses, the FDC terminates operation, interrupts and sets the Seek Error status bit. A verification operation takes place if the V bit is set. The h bit allows the head to be loaded at the start of the command. Note that the Restore command is executed when $\overline{\text{MR}}$ goes from low (true) to high (false).

- SEEK — This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The FDC will update the Track Register and issue stepping pulses until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V bit is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP — Upon receipt of this command, the FDC issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V bit is on. If the u bit is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP-IN — Upon receipt of this command, the FDC sets DIRC high and issues one stepping pulse. If the u bit is on, the Track Register is incremented. After a delay determined by the r_1r_0 field, a verification takes place if the V bit is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.
- STEP-OUT — This command is identical to the Step-In command, except that DIRC is set low and the Track Register is decremented for each step pulse if the u bit is high.

3.1.1 Type I Command Option Bits

The operation of the option determining bits for Type I commands is summarized in Figures 3a and 3b.

The detailed descriptions of the Type I option bits follow.

- r_1r_0 (Step Rate) — These bits select the rate at which step pulses are issued. Note that the stepping rates are independent of $\overline{DDEN}$ select. Both single and double-density modes step at the same rate.
- V (VERIFY) — This bit is used to select track verification at the end of the stepping sequence. During verification, the head is loaded and after an internal 15*ms delay, the HLT input is sampled. Note: If $\overline{TEST}$=0, the internal delay to HLT sampling is <= 300μs. When HLT is true, the first encountered ID field is read from the disk. The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match, but there is a valid ID CRC, an interrupt is generated, the Seek Error status bit (status bit 4) is set, and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC Error status bit (status bit 3) is set, and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC terminates the operation and generates an interrupt.
- h (Head Load) — This bit determines if the head is to be loaded at the beginning of the command. If so, the HLD output goes high (active) and remains in this state until the FDC receives a command to disengage the head. If the FDC is idle (not Busy) for 15 disk revolutions, then the head is automatically disengaged (HLD goes low). If track verification is selected (V = "1"), then the head loading is affected, as follows:
  - h = 0, V = 1
    HLD is activated near the end of the sequence, an internal 15* msec delay occurs, and the FDC waits for the HLT input to go active (high) before verifying track identification.
  - h = 1, V = 1
    HLD is activated at the start of the sequence. Then an internal 15* msec delay occurs and the FDC waits for HLT to go active before verification.
- u (Update) — With Update selected (u = "1"), the Track Register is updated at each step pulse. The update operation increments the Track Register for stepping in toward track 76 and decrements it for stepping out toward track 0.

*30 msec delay for 1 MHz CLK.

BIT								
7	6	5	4	3	2	1	0	COMMAND
0	0	0	0	h	V	r_1	r_0	RESTORE
0	0	0	1	h	V	r_1	r_0	SEEK
0	0	1	u	h	V	r_1	r_0	STEP
0	1	0	u	h	V	r_1	r_0	STEP-IN
0	1	1	u	h	V	r_1	r_0	STEP-OUT

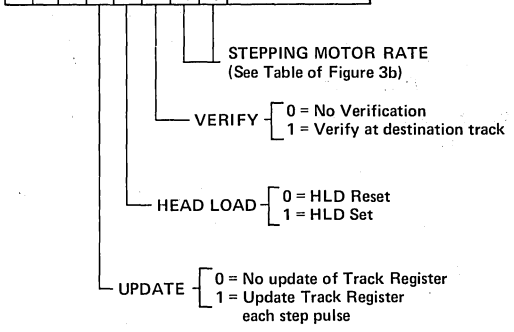


Figure 3a. Type I Command Option Bit

$\overline{TEST}$	r_1	r_0	STEPPING RATE	
			CLK = 1MHz	CLK = 2MHz
H	0	0	6 ms	3 ms
H	0	1	12 ms	6 ms
H	1	0	20 ms	10 ms
H	1	1	30 ms	15 ms
L	—	—	~400μs	~200μs

Figure 3b. Stepping Motor Rates

3.2.1 Type I Command Signals

Type I commands control the operation of the STEP and DIRC (Direction) output signals of the FDC.

- STEP — A 2 μs (MFM) or 4 μs (FM) positive-true output pulse is generated at a rate determined by the r_1r_0 field of the command (see Figure 3b). Each step pulse moves the Read/Write head one track location in a direction controlled by the DIRC output.
- DIRC — The DIRC output determines the direction of the track stepping. A high level indicates step direction IN towards track 76, a low level indicating direction OUT towards track Ø.

In addition, the Type I commands use the following signals:

- HLD (Head Load) — This output is used to control movement of the Read/Write head against the recording medium. HLD is set at the beginning of a Type I command if h = "1", near the end of a Type I command if V = "1" and h = "0", or immediately when a TYPE II or TYPE III command is executed. Once HLD is set it remains high until a subsequent Type I command with h = "0" and V = "0" is loaded, or until the FDC goes into its non-busy state after 15 index pulses.
- HLT (Head Load Timing) — The low to high transition of this input indicates that a sufficient time has elapsed for the drive's head to become engaged. It typically follows HLD going high, by a time delay which is dependent on the particular drive's characteristics. If not available from the drive electronics, this input must be generated by the user (typically by means of one-shot timers). Figure 4 illustrates an example of HLD and HLT timing.

  The logical AND of HLD and HLT is status bit 5 for Type I commands, and it controls the operation of the disk read and write functions.

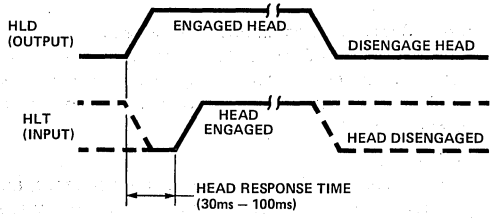


Figure 4. HLD/HLT Timing Example

3.2 Type II Commands

The Type II commands, Read Sector and Write Sector, permit actual data to be read from or written onto the diskette. Before the command is entered, it is necessary for the processor to have loaded the Sector Register with the number of the desired sector. Figure 5 is useful for understanding the operation of Type II commands.

3.2.1 Type II Command Basic Operation Sequence

The basic operation of Type II commands is outlined as the following sequence:

— The ID field is located by the detection of the ID AM (ID Address Mark).

— The Track Number in the ID field is compared to the contents of the Track Register. If it does not match, then the ID AM search begins again.

— As a selectable option, the Side Number is checked for a match. If selected, a failure to match again causes the ID AM search to re-start.

— The Sector Number is compared to the contents of the Sector Register. If there is not a match, the ID AM search is again begun.

— The Sector Length field is entered into the FDC and stored internally for use in Read or Write operations. The value of the Sector Length byte is determined when the diskette is formatted (initialized) and must have one of the values in the table of Figure 6.

— The ID field CRC1 and CRC2 bytes are checked with internally generated CRC. If they match, then the command (Read or Write) is permitted; if not, the CRC Error status bit is set and the search for the ID AM is begun again.

If the Track Number, Side Number, Sector Number, and CRC all check properly within 4 disk revolutions (5 index pulses), then the command continues; otherwise the Record-Not-Found status bit is set and the command is terminated with an interrupt (INTRQ).

SECTOR LENGTH FIELD (hex)	NUMBER OF BYTES IN SECTOR
00	128
01	256
02	512
03	1024

Figure 6. Sector Length Field Codes

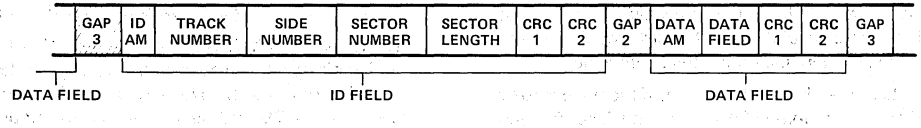


Figure 5. General Track Format

BIT								
7	6	5	4	3	2	1	0	COMMAND
1	0	0	m	S	E	C	0	READ SECTOR
1	0	1	m	S	E	C	a_0	WRITE SECTOR

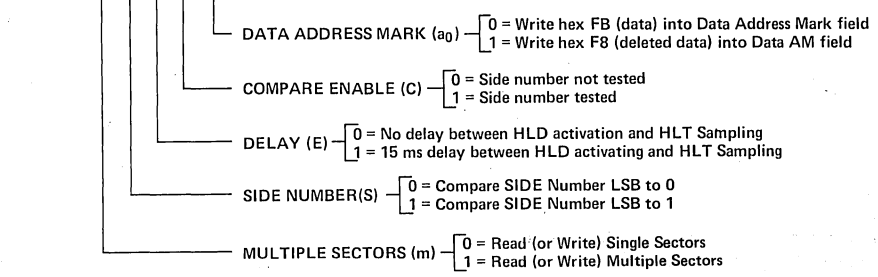


Figure 7. Type II Command Option Bits

3.2.2 Type II Command Option Bits

Several bits in the Type II command words are used to select various options. Figure 7 summarizes the special control bits which are outlined, as follows:

- a_0 (Data AM) — The a_0 bit is used to select which of two Data Address Mark bytes is to be stored in the Data AM field for Write Sector operations. A "1" in a_0 causes hex F8 to be stored, indicating that the data field is actually deleted data. A "0" in a_0 causes hex FB to be stored, indicating undeleted data.
- S (Side) — The S bit is compared with the LSB of the Side Number (in the ID field), if the side number compare option has been enabled by the C bit.
- C (Compare) — This bit enables the comparison of the Side Number (in the ID field) with the S bit of the Type II command.
- E (Delay) — The E bit causes a 15 msec delay to be inserted between the time the HLD (Head Load) output is activated and the time the HLT (Head Load Timing) input is strobed and checked.
- m (multiple Records) — This bit is used to select whether one sector (m = "0") or more than one sector (m = "1") is to be read or written. For single sector operation, the interrupt is generated and the command is terminated immediately after the sector operation is complete. Multiple sector operation, however, is somewhat different. After the first sector operation is complete, the FDC Sector Register is incremented and the sequence is re-started. In this way, the next sequential sector number is read or written. Likewise, after it is complete, the Sector Register is again updated and the sequence re-started. This continues until the Sector Register has incremented to a number higher than any sector on the current track. At this point, the sequence terminates.

3.2.3 Type II Command Operation

The specific operation of the Read Sector and Write Sector commands, once the ID field is properly encountered, is outlined below:

- READ SECTOR — When the correct Track Number, Side Number (if selected), Sector Number, and CRC have been identified, the Data Field check commences. The Data AM must be found within 30 bytes for single-density (or 43 bytes for double-density) from the time the last CRC byte for the ID field was encountered. If not, the Record-Not-Found bit in the Status Register is set and the command is terminated. After the Data AM is found, the data bytes are entered through the internal Data Shift Register and transferred to the Data Register. Each byte transferred results in a DRQ. The Data Register must be unloaded (read) by the MPU or DMA controller before the next byte is fully received. If not, then the new byte is written over the previous byte in the Data Register, the previous byte is lost, and the Lost Data status bit is set. At the end of the Data Field, the CRC bytes are compared to the internal CRC generated by the FDC. If they do not match, the CRC Error status bit is set and the command is terminated, even if it is a multiple-record command (m = "1"). At the end of the sequence, the Data AM encountered in the Data Field determines bit 5 of the Status Register. If the Data AM was hex FB (undeleted), then bit 5 is set to "0"; hex F8 (deleted data) causes bit 5 to be set to "1".
- WRITE SECTOR — The Write Sector command operates in a fashion very similar to Read Sector. When the correct Track Number, Side Number (if selected), Sector Number, and CRC have been identified, a DRQ is generated, requesting the first data byte which is to be written on the diskette. The FDC then counts 11 bytes for single-density (or 22 bytes for double-density) to account for part of the gap between the ID

and DATA fields (Gap 2 in Figure 5). At this point, if the DRQ has been serviced and a data byte stored in the Data Register, the WG output goes true (high) and 6 bytes of zeroes for single-density (12 bytes for double-density) are written on the diskette. This accounts for the remainder of Gap 2. (If the DRQ had not been serviced, the Lost Data status bit would have been set and the command terminated). Following Gap 2, the Data AM is written. This byte is either hex FB (undeleted data) or hex F8 (deleted data) and is determined by the state of the a_0 bit in the command byte, (see Figure 7). Finally, the data is written on the diskette, starting with the byte already loaded in the Data Register. As each byte is transferred from the Data Register to the Data Shift Register to be stored on the diskette, a DRQ is generated to the MPU or DMA control unit requesting the next data. If any DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeroes is stored on the diskette, but the command is not terminated. After the last data byte is stored on the diskette, the two-byte CRC (generated in the FDC) is then stored on the diskette. Finally, after the CRC bytes, the FDC stores one more byte (hex FF), the WG output goes low (false), and the command is terminated.

3.3 Type III Commands

There are three Type III Commands:

- READ ADDRESS — Read the next ID field (6 bytes) into the FDC.
- READ TRACK — Read all bytes of the entire track, including gaps.
- WRITE TRACK — Write all bytes to the entire track, including gaps.

3.3.1 Type III Command Option Bit

There is one option bit for Type III commands.

- E (DELAY) — This option bit acts the same for Type III commands as it does for Type II commands. See section 3.2.2 for further information.

3.3.2 Type III Command Operation

- READ ADDRESS — When this command is issued, the head is loaded (HLD high) and the Busy status bit is set. The next ID field encountered on the diskette is then read a byte at a time, using DRQ initiated data transfers to the MPU or DMA controller. Six bytes are entered, comprising the entire ID field. They are: Track Number (1 byte); Side Number (1 byte); Sector Number (1 byte); Sector Length (1 byte); and CRC (2 bytes). Although the CRC bytes are passed unaltered, the FDC checks their validity and sets the CRC Error status bit accordingly. Part of the operation of this command causes the Track Number to be stored in the Sector Register of the FDC. The command ends with the generation of an interrupt (INTRQ) and the clearing of the Busy status bit.
- READ TRACK — The initiation of this command causes the head to be loaded (HLD active) and the Busy status bit to be set. Reading of the track starts with the next encountered Index pulse and continues until the following Index Pulse. Each byte is assembled and transferred to the Data Register. As in any normal read operation, a DRQ output is generated with each byte, signalling to the MPU or DMA control unit that the byte is ready. CRC and Gap bytes are treated as any other byte. No CRC checking is performed. When all bytes are transferred, the Busy status bit is cleared, and INTRQ goes high.
- WRITE TRACK — The start of this command causes the head to be loaded (HLD active) and the Busy status bit to be set. Data is written onto the track when the first Index pulse is encountered, and terminated at the subsequent Index Pulse. DRQ is activated immediately after the command is issued to permit adequate time for the first byte to be made available before the Index is found. If this time is not enough and the Index Pulse occurs before the Data Register is loaded, then the command is terminated. Once the data transfers begin, the DRQ is generated for each byte as needed. Any byte which is not transferred into the FDC in time causes a byte of all zeroes to be stored on the diskette instead. Address Marks and CRC bytes are generated by the FDC in response to format control bytes supplied by the system MPU or DMA control unit. When all bytes are transferred, the command is terminated, the Busy status bit is cleared, and INTRQ is set high.

3.4 Type IV Command

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 8 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for $I_3 = 1$ (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all 0.

3.5 Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated

BIT								
7	6	5	4	3	2	1	0	COMMAND
1	1	0	1	I_3	I_2	I_1	I_0	FORCE INTERRUPT

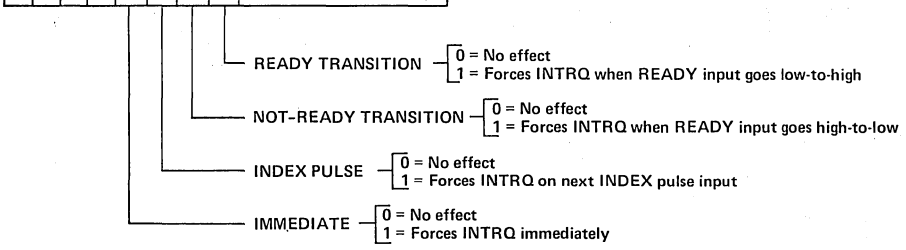


Figure 8. Force Interrupt Command Flags

COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 9. Status Register Summary

when there is not another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 9 illustrates the meaning of the status bits for each command.

Detailed descriptions of each status bit function follow:

- NOT READY
  0 = Drive is Ready
  1 = Drive is Not Ready
- WRITE PROTECT
  0 = $\overline{\text{WPRT}}$ input is high (unprotected)
  1 = $\overline{\text{WPRT}}$ input is low (protected)
- HEAD LOADED
  0 = Head is not currently loaded
  1 = Head is loaded and engaged (both HLD and HLT are active)
- SEEK ERROR
  0 = Desired track was found. Updating clears this bit
  1 = Desired track was not found
- TRACK 0
  0 = $\overline{\text{TR00}}$ input is high
  1 = $\overline{\text{TR00}}$ input is low (Read/Write head is on Track Ø)
- INDEX
  0 = $\overline{\text{IP}}$ input is high (no index mark)
  1 = $\overline{\text{IP}}$ input is low (index mark)
- BUSY
  0 = Not Busy
  1 = Busy (Command sequence in progress)
- RECORD TYPE
  0 = Non-deleted data mark
  1 = Deleted data mark
- WRITE FAULT
  0 = No write fault
  1 = Write fault has occurred
- RECORD NOT FOUND
  0 = Desired track and sector properly found. Updating clears this bit
  1 = Desired track and sector not found
- CRC ERROR
  0 = No CRC error. Updating clears this bit
  1 = CRC check error encountered
- LOST DATA
  0 = No data lost. Updating clears this bit
  1 = MPU did not respond to DRQ. Data was lost
- DATA REQUEST (DRQ)
  0 = DRQ not in progress. Updating clears this bit.
  1 = DRQ currently in progress

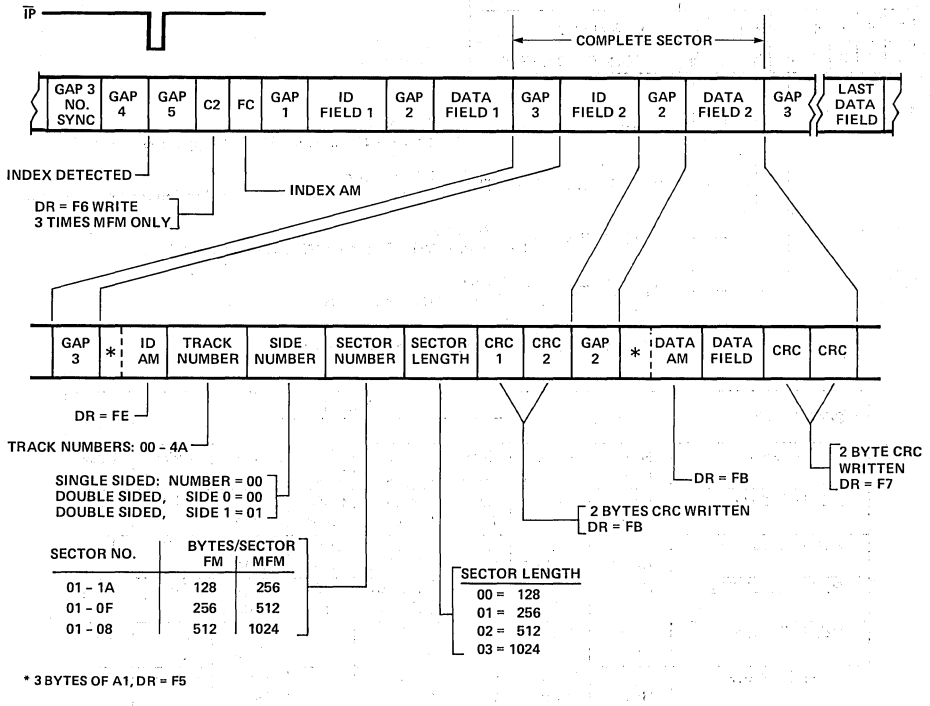


Figure 10. IBM Compatible Sector/Track Format

4.0 DISK FORMATTING

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 10 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as Data AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

4.1 IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 11.

4.2 IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 12.

4.3 Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 13.

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	FF	40	Gap 5 (Post Index)
	00	6	
	FC	1	Index AM
	FF	26	Gap 1
	00	6	
	FE	1	ID AM
	XX	1	Track Number (00-4A)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	00	1	Sector Length (128 bytes)
ONE SECTOR (1)	F7	1	Causes 2-Byte CRC to be Written
	FF	11	Gap 2 (ID Gap)
	00	6	
	FB	1	Data AM
	E5	128	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	FF	27	Part of Gap 3 (Data Gap)
	FF	247 (2)	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

Figure 11. Byte Sequence for IBM 3740 Formatting

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	4E	80	Gap 5 (Post Index)
	00	12	
	F6	3	Writes C2
	FC	1	Index AM
	4E	50	
	00	12	Gap 1
	F5	3	Writes ID AM Sync Bytes
	FE	1	ID AM
	XX	1	Track Number (00-4C)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	01	1	Sector Length (256 Bytes)
ONE SECTOR (1)	F7	1	Causes 2-Byte CRC to be Written
	4E	22	Gap 2 (ID Gap)
	00	12	
	F5	3	Writes ID AM Sync Bytes
	FB	1	Data AM
	40	256	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	4E	54	Part of Gap 3 (Data Gap)
	4E	598 (2)	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

Figure 12. Byte Sequence for IBM System-34 Formatting

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

Figure 13. Gap Size Limitations

MICRO-PROCESSORS

5.0 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temp.	T_{OP}	0°C to 70°C
Storage Temp.	T_{STG}	-55°C to 150°C

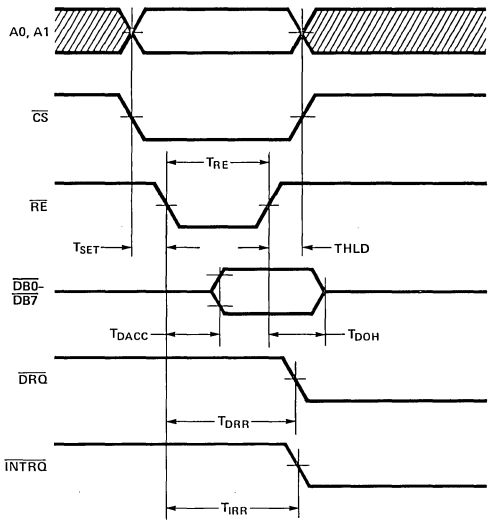
All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

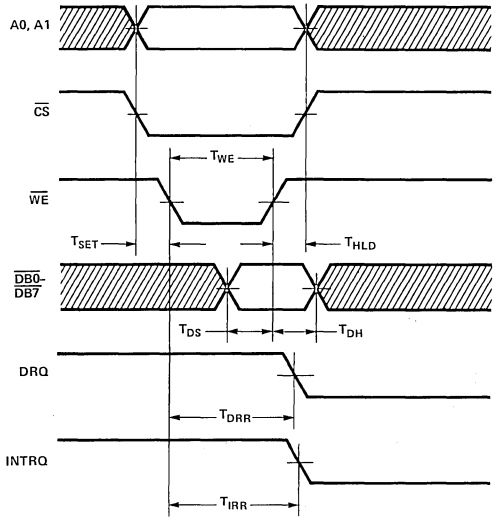
D.C. CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0-70°C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.6	–	V
Input Low Voltage	V_{IL}	–	0.8	V
Input Leakage Current, V_{IN} = 0V to V_{CC}	I_{IL}	–	±10	μA
Output High Voltage, I_{LOAD} = -100 μA	V_{OH}	2.8	–	V
Output Low Voltage, I_{LOAD} = 1.6 mA	V_{OL}	–	0.45	V
Output Leakage Current, V_{OUT} = V_{CC}	I_{OL}	–	10	μA
Power Dissipation (V_{CC} = 5.25V)	P_D	–	525	mW
Input Capacitance	C_{IN}	–	15	pF

MPU READ CYCLE TIMING



MPU WRITE CYCLE TIMING



MPU READ CYCLE REQUIREMENTS (V_{CC} = 5V ± 5%, T_A = 0−70°C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT	NOTE
Address and $\overline{CS}$ Setup Time	T_{SET}	50	–	ns	
$\overline{RE}$ Pulse Width	T_{RE}	400	–	ns	
Address and $\overline{CS}$ Hold Time	T_{HLD}	10	–	ns	
Data Access Time	T_{DACC}	–	300	ns	C_L = 50pF
Data Hold Time	T_{DOH}	50	150	ns	C_L = 50pF
DRQ Reset Delay	T_{DRR}	–	500	ns	
INTRQ Reset Delay	T_{IRR}	–	3000	ns	1

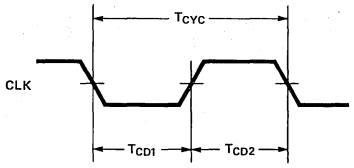
1. Timing shown is for 2MHz CLK frequency. For 1 MHz, this parameter is doubled.

MPU WRITE CYCLE CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0−70°C)

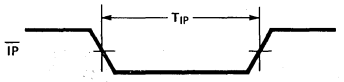
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT	NOTE
Address and $\overline{CS}$ Setup Time	T_{SET}	50	–	ns	
$\overline{WE}$ Pulse Width	T_{WE}	350	–	ns	
Address and $\overline{CS}$ Hold Time	T_{HLD}	10	–	ns	
Data Setup Time	T_{DS}	250	–	ns	
Data Hold Time	T_{DH}	20	–	ns	
DRQ Reset Delay	T_{DRR}	–	500	ns	
INTRQ Rest Delay	T_{IRR}	–	3000	ns	1

1. Timing shown is for 2MHz CLK frequency. For 1MHz, this parameter is doubled.

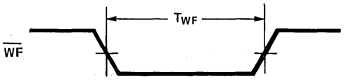
SYSTEM CLOCK REFERENCE



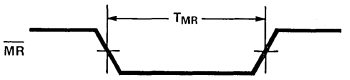
INDEX PULSE INPUT



WRITE FAULT INPUT



MASTER RESET INPUT

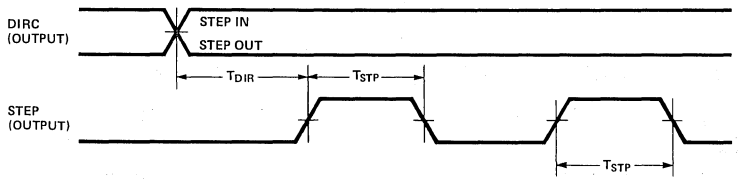


MISCELLANEOUS TIMINGS (V_{CC} = 5V ± 5%, T_A = 0 – 70°C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT	NOTE
Clock Low Time	T_{CD1}	230	20000	ns	2
Clock High Time	T_{CD2}	200	20000	ns	2
DIRC Setup Time	T_{DIR}	12	–	μs	2
STEP Pulse Width	T_{STP}	2, 4 or 8	–	μs	1
Index Pulse Width	T_{IP}	10	–	μs	2
Write Fault Pulse Width	T_{WF}	10	–	μs	2
Master Reset Pulse Width	T_{MR}	50	–	μs	2

1. Depends upon FM/MFM mode and CLK frequency. See timing figure below.
2. Timing shown is for 2 MHz clock: Minimum time doubles for 1 MHz clock.

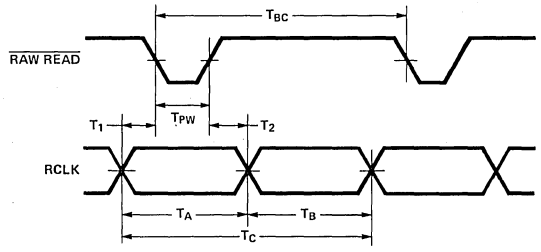
STEP AND DIRECTION MOTOR CONTROL TIMING



T_{STP} PULSE WIDTH

CLK FREQ.	MODE	
	MFM	FM
1MHz	4μs	8μs
2MHz	2μs	4μs

INPUT DATA TIMING CHARACTERISTICS



SYMBOL	DESCRIPTION	COMMENTS
T_C	T_C, RCLK's period, must be greater than 1.5 μsec.	
T_A T_B	T_A and T_B must each be greater than 800 nsec.	

CLK FREQ.	MODE	NOMINAL RCLK TIMES T_A	T_B	T_C	UNIT
1MHz	MFM	2	2	4	μs
	FM	4	4	8	μs
2MHz	MFM	1	1	2	μs
	FM	2	2	4	μs

SYMBOL	DESCRIPTION	COMMENTS
T_{PW}	RAW READ Pulse Width. Normally is 100-300 ns. May be any width providing it is entirely within RCLK stable time. If it extends beyond RCLK transition, then it must be constrained by the values in the table.	

CLK FREQ.	MODE MFM	FM
1MHz	⩽600ns	⩽1200ns
2MHz	⩽300ns	⩽600ns

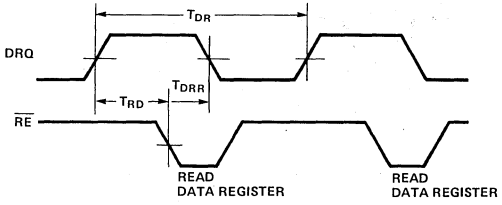
SYMBOL	DESCRIPTION	COMMENTS
T_{BC}	RAW READ Pulse Period 1.6 μs min. at 2 MHz 3.2 μs min. at 1 MHz	

CLK FREQ.	MODE MFM	FM
1MHz	4, 6 or 8μs	4 or 8μs
2MHz	2, 3 or 4μs	2 or 4μs

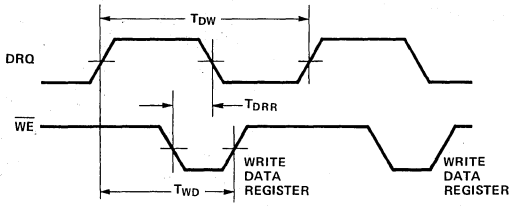
SYMBOL	DESCRIPTION	COMMENTS
T_1, T_2	T_1 and T_2 must each be greater than 40 ns.	

DISKETTE DATA TIMING CHARACTERISTICS

READ ENABLE TIMING

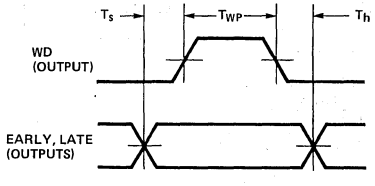


WRITE ENABLE TIMING

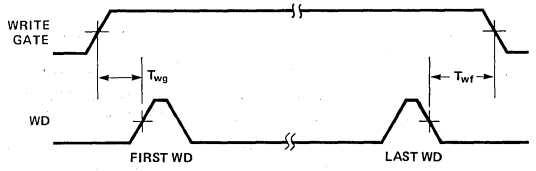


CLK FREQ.	MODE	T_{DR} nom.	T_{RD} max.	T_{DW} nom.	T_{WD} max.	UNIT
1MHz	MFM	32	27.0	32	23.0	μs
	FM	64	55.0	64	47.0	μs
2MHz	MFM	16	13.5	16	11.5	μs
	FM	32	27.5	32	23.5	μs

WRITE DATA TIMING



WRITE GATE TIMING



CLK FREQ	MODE	T_{wp} min.	T_{wp} max.	T_s min.	T_h min.	T_{wg} nom.	T_{wf} nom.	UNIT
1 MHz	MFM	300	500	250	250	2000	2000	nsec
	FM	900	1100	—	—	4000	4000	nsec
2 MHz	MFM	150	250	125	125	1000	1000	nsec
	FM	450	550	—	—	2000	2000	nsec

Enhanced Programmable Communications Interface

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SY2661

MICROPROCESSOR PRODUCTS

PRELIMINARY

SYNCHRONOUS OPERATION

- 5 to 8-bit characters plus parity
- Single or double SYN operation
- Internal or external character synchronization
- Transparent or non-transparent mode
- Transparent mode DLE stuffing (Tx) and detection (Rx)
- Automatic SYN or DLE-SYN insertion
- SYN, DLE and DLE-SYN stripping
- Odd, even, or no parity
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)

ASYNCHRONOUS OPERATION

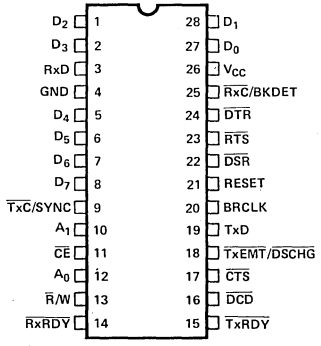
- 5 to 8-bit characters plus parity
- 1, 1½ or 2 stop bits transmitted
- Odd, even, or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loop back mode
- Baud rate: dc to 1M bps (1X clock)
  - — dc to 62.5K bps (16X clock)
  - — dc to 15.625K bps (64X clock)

OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets (2661-1, -2, -3)
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- 3 open drain MOS outputs can be wire-ORed
- Single 5V power supply
- No system clock required
- 28-pin dual-in-line package

MICRO-PROCESSORS

PIN CONFIGURATION



ORDERING INFORMATION

Part No.	Package
SYP2661-X	Plastic
SYD2661-X	Cerdip
SYC2661-X	Ceramic

X = 1, 2 or 3
(See Table 1)

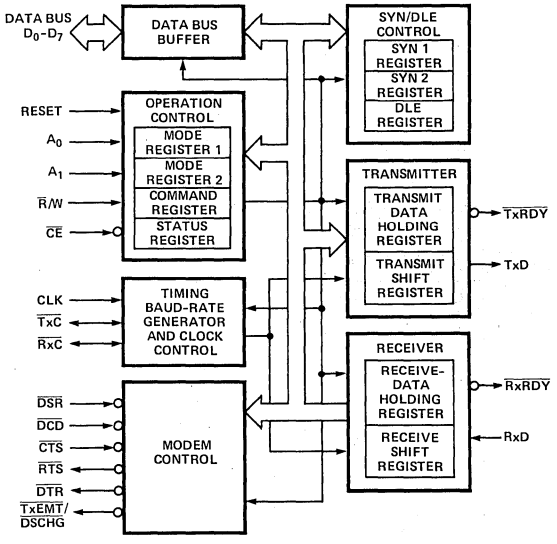


Figure 1. Block Diagram

Table 1 Baud Rate Generator Characteristics

2661-1 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6144
0	0	0	1	75	1.2	—	4096
0	0	1	0	110	1.7598	-0.01	2793
0	0	1	1	134.5	2.152	—	2284
0	1	0	0	150	2.4	—	2048
0	1	0	1	200	3.2	—	1536
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9.6	—	512
1	0	0	0	1050	16.8329	0.196	292
1	0	0	1	1200	19.2	—	256
1	0	1	0	1800	28.7438	-0.19	171
1	0	1	1	2000	31.9168	-0.26	154
1	1	0	0	2400	38.4	—	128
1	1	0	1	4800	76.8	—	64
1	1	1	0	9600	153.6	—	32
1	1	1	1	19200	307.2	—	16

2661-2 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45.5	0.7279	0.005	6752
0	0	0	1	50	0.8	—	6144
0	0	1	0	75	1.2	—	4096
0	0	1	1	110	1.7598	-0.01	2793
0	1	0	0	134.5	2.152	—	2284
0	1	0	1	150	2.4	—	2048
0	1	1	0	300	4.8	—	1024
0	1	1	1	600	9.6	—	512
1	0	0	0	1200	19.2	—	256
1	0	0	1	1800	28.7438	-0.19	171
1	0	1	0	2000	31.9168	-0.26	154
1	0	1	1	2400	38.4	—	128
1	1	0	0	4800	76.8	—	64
1	1	0	1	9600	153.6	—	32
1	1	1	0	19200	307.2	—	16
1	1	1	1	38400	614.4	—	8

2661-3 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	—	6336
0	0	0	1	75	1.2	—	4224
0	0	1	0	110	1.76	—	2880
0	0	1	1	134.5	2.1523	0.016	2355
0	1	0	0	150	2.4	—	2112
0	1	0	1	300	4.8	—	1056
0	1	1	0	600	9.6	—	528
0	1	1	1	1200	19.2	—	264
1	0	0	0	1800	28.8	—	176
1	0	0	1	2000	32.081	0.253	158
1	0	1	0	2400	38.4	—	132
1	0	1	1	3600	57.6	—	88
1	1	0	0	4800	76.8	—	66
1	1	0	1	7200	115.2	—	44
1	1	1	0	9600	153.6	—	33
1	1	1	1	19200	316.8	3.125	16

Note: 16X CLK is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

SIGNAL DESCRIPTIONS

CPU INTERFACE

RESET (Reset)

A high on this input performs a master reset on the SY2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

A_0, A_1 (Address 0, 1)

Address lines used to select the internal registers.

$\overline{R}/W$ (Read/Write)

The direction of data transfers between the EPCI and the CPU is controlled by the $\overline{R}/W$ input. When $\overline{CE}$ and $\overline{R}/W$ are both low the contents of the selected registers will be transferred to the data bus. With $\overline{CE}$ low and $\overline{R}/W$ high a write to the selected register is performed.

$\overline{CE}$ (Chip Enable)

When low, the selected register will be accessed. When high the D_0-D_7 lines will be placed in the high impedance state.

DB_0-DB_7 (Data Bus)

An 8-bit three-state positive true data bus used to transfer commands, data and status between the EPCI and the CPU.

$\overline{TxRDY}$ (Transmitter Ready)

This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt.

$\overline{RxRDY}$ (Receiver Ready)

This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RxHR) has a character ready for input to the CPU. It goes high when the RxHR is read by the CPU and also when the receiver is disabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt line.

$\overline{TxEMT}/\overline{DSCHG}$

This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU if the TxEMT condition does not exist. Otherwise, the TxHR must be loaded by the CPU for this line to go high. It is an open drain output which can be "wire OR-ed" to the CPU interrupt line.

TRANSMITTER/RECEIVER SIGNALS

BRCLK (Baud Rate Clock)

Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET (Receiver Clock, Break Detect)

When the EPCI is programmed for External Receiver Clock, this pin will act as an input and control the rate at which a character is received. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data are sampled on the rising edge. If internal Receiver Clock is programmed this pin will provide an output, either a 1X/16X clock or Break Detect signal determined by programming Mode Register 2.

$\overline{TxC}$/XSYNC (Transmitter Clock/External SYNC)

When the EPCI is programmed for External Transmitter clock, this pin will act as an input and control the rate at which the character is transmitted. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data changes on the falling edge of this clock. If the UPCI is programmed for Internal Transmitter clock, this pin can be either an output providing a 1X/16X clock or an input for External Synchronization determined by Mode Register 2 programming.

RxD (Receive Data)

RxD is the serial data input to the receiver.

TxD (Transmit Data)

TxD is the serial data output from the transmitter. When the transmitter is disabled the output will be in the high, "Mark", state.

$\overline{DSR}$ (Data Set Ready)

$\overline{DSR}$ is an input that can be used to indicate to the UPCI Data Set Ready or Ring Indicator. Its complement appears in the Status Register as bit SR7. A change of state on $\overline{DSR}$ will cause $\overline{TxEMT}/\overline{DSCHG}$ to go low if either CR0 or CR2 = 1.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input must be low for the receiver to operate. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited. The complement of $\overline{DCD}$ appears in the Status Register as bit SR6. A change of state in $\overline{DCD}$ will cause $\overline{TxEMT}/\overline{DSCHG}$ to go low if either CR0 or CR2 = 1.

$\overline{CTS}$ (Clear To Send)

The $\overline{CTS}$ input must be low for the transmitter to operate. If $\overline{CTS}$ goes high while transmitting, the character currently in the Transmit Shift Register will be transmitted before termination TxD will then go to the high level (Mark).

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output is the complement of CR1. It is normally used to indicate Data Terminal Ready.

$\overline{RTS}$ (Request To Send)

The $\overline{RTS}$ output is the complement of CR5. If the Transmit Shift Register is not empty when CR5 is reset, $\overline{RTS}$ will not go high until one TxC after the last serial bit is transmitted.

FUNCTIONAL DESCRIPTION

The internal organization of the EPCI consists of six major blocks, (see Fig. 1). These are the Transmitter, Receiver, Clock Control, Operation Control, Modem Control and SYN-/DLE Control. These blocks internally communicate over common data and control buses. The data bus is also linked to the CPU via a bi-directional three-state interface.

Briefly, these blocks perform the following functions:

Transmitter

The Transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting Start, Stop, and Parity bits, as selected by the user, and outputs a composite serial data stream.

Receiver

The Receiver accepts serial data from the sending device, converts it to a parallel format checking for appropriate Start, Stop and Parity bits and Control Characters, as selected by the user, and sends the assembled character to the CPU.

Timing Control

The Timing Control block contains a programmable Baud Rate Generator (BRG) which is able to accept external Transmit ($\overline{TxC}$) or Receive ($\overline{RxC}$) clocks or to divide external clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

Operating Control

The Operation Control block contains four registers; Mode Registers 1 and 2, (MR1, MR2) the Command Register (CR) and Status Register (SR). These registers are used to store configuration and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE character provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

OPERATION

The EPCI's operation is determined by programming the Mode and Command Registers. Baud rate, asynchronous or synchronous communication, and SYN characters are determined before enabling the transmitter or receiver.

Asynchronous Receiver Operation

After the Mode Registers are configured the receiver is enabled when the RxEN bit in the Command Register (CR2) is set to a 1 and $\overline{DCD}$ is low. The EPCI then monitors the RxD input waiting for a high to low transition. If a transition is detected, the RxD input is again sampled one-half bit time later. If RxD is now high, a search for a valid start bit is begun again. If RxD is still low a valid start bit is assumed and the receiver continues to sample the RxD input at one bit time intervals until the correct number of data bits, parity bit and one stop bit have been assembled. The character is then transferred to the Receive Data Holding Register (RxHR); RxRDY in the status Register is set (SR1); the $\overline{RxRDY}$ output goes low. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundry. See Figure 6 and 8.

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins. See Figure 9.

Pin 25 can be programmed as a Break Detect (BKDET) output by setting both bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go high. If RxD returns high for at least one RxD time, BKDET will return low.

Synchronous Receiver Operation

When the EPCI is programmed for synchronous operation the receiver will remain idle until the receiver enable bit (CR2) is set. At this time the EPCI enters the hunt mode. Data are shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). See Figure 6.

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note: the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

By setting MR24 (MR2 bit 4) and MR27 = 1 pin 9 ($\overline{RxC}$/XSYNC) will be programmed as an external jam synchronization input. When XSYNC is selected internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC must be lowered prior to the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

ASYNCHRONOUS TRANSMITTER OPERATION

When the EPCI is programmed to transmit the transmitter will remain idle until $\overline{CTS}$ is low and the TxEN bit (CR0) is set. The EPCI will respond by setting status register (SR) bit 0 and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register (TxHR), SR0 is reset and $\overline{TxRDY}$ returns high. The character is then transferred to the transmit shift register (TxSR) when it is idle or has completed transmission of the previous character. SR0 is again set, and $\overline{TxRDY}$ goes low. See Figure 7.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting CR3.

SYNCHRONOUS TRANSMITTER OPERATION

When the EPCI is initially programmed for synchronous transmission it will remain in the idle state (RxD high) until TxEN is set. At this point TxD remains high, $\overline{\text{TxRDY}}$ will go low and both will stay in this state until the first character (usually a SYN character) is written into the TxHR. This starts transmission, with $\overline{\text{TxRDY}}$ going low each time a character is shifted from the TxHR to the TxSR. If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output will go low and the EPCI will automatically fill the pending gap with SYN1, SYN1, SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR6 and MR17. Transmission will be continuous until TxEN is reset to 0. See Figure 7.

If the send DLE bit (CR3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR. Since this is a one time command, CR3 does not have to be reset.

EPCI PROGRAMMING

Before data communications can be started the EPCI must be programmed by writing to its mode and command registers. Additionally, if synchronous communication has been selected the appropriate SYN1, SYN2 and DLE registers must be loaded. Reference the Register Addressing Table and Initialization Flow Chart for address requirements and programming procedure.

The Register Addressing table shows MR1 and MR2 at the same address. The EPCI has an internal pointer that initially directs the first read or write to MR1, then on the next access at that same address the pointer directs the operation to MR2. A similar sequence occurs for the SYN and DLE registers; first SYN1 then SYN2 then DLE. If more than the required number of accesses are made the internal pointer resets to the first register. The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register, but unaffected by any other read or write operation.

REGISTER FORMATS

The register formats are summarized in Figures 2 through 5. MR1 and MR2 define the general operating characteristics. The Command Register controls the basic operation defined by MR1 and MR2. The Status Register indicates the EPCI operating status and the condition of external inputs. These registers are cleared by a RESET input (SR6 and SR7 excepted).

MODE REGISTER 1 (MR1)

MR11 and MR10 select the communication mode and baud rate multiplier. Note: the multiplier in asynchronous mode applies only if the external input option is selected by MR24 and MR25.

MR13 and MR12 select Character length. Character length does not include the parity bit, when selected, and does not include the start and stop bits in asynchronous operation.

MR14, when set, selects parity. A parity bit will be transmitted with each character, and a parity check will be performed on each character received.

MR15 selects either odd or even parity.

In the asynchronous mode MR16 and MR17 select the number of stop bits; 1, 1.5 or 2. If 1X baud rate is programmed 1.5 stop bits defaults to 1 on transmit.

In the synchronous mode MR17 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are 0.

MR16 controls selection of the transparent mode. When MR16 is set (transparent selected) DLE-SYN1 is used for character fill and SYN detect (SR 5), but the normal synchronization sequence is used to establish character sync. When transmitting in the synchronous transparent mode, a DLE character in the TxHR will cause a second DLE character to be transmitted. Note: if the send DLE command (CR3) is active when a DLE character is in the TxHR only one additional DLE will be transmitted.

The bits in the mode register affecting character assembly and disassembly (MR12-MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12-15 must be changed within n bit times of the active going state of $\overline{\text{RxRDY}}$/$\overline{\text{TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = smaller of the new and old character lengths.)

MODE REGISTER 2 (MR2)

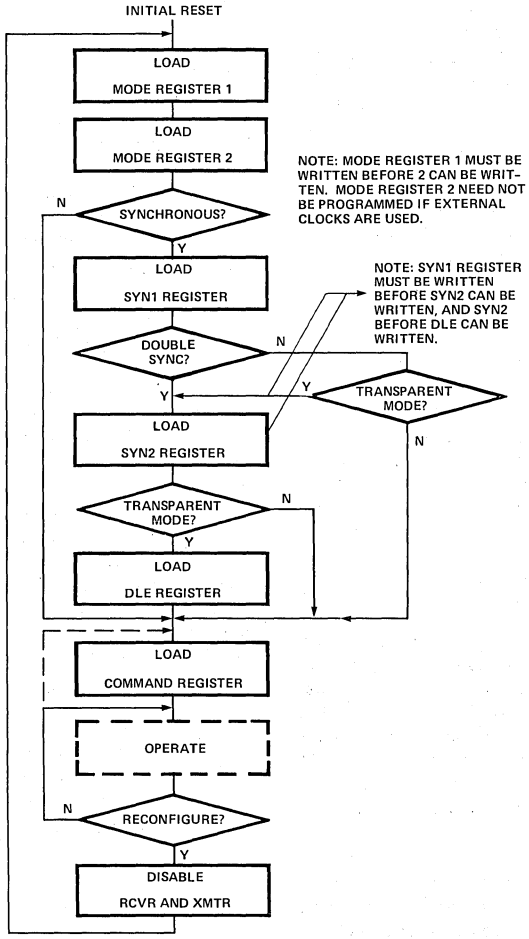
MR20 through MR23 select the internal Baud Rate Generator (BRG). There are sixteen selectable rates for each version as outlined in Table 1.

MR24 through MR27 define the receive and transmit clock source and the function of pins 9 and 25. Reference Figure 3.

Table 2 SY2661 Register Addressing

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	Function
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

EPCI Initialization Flow Chart



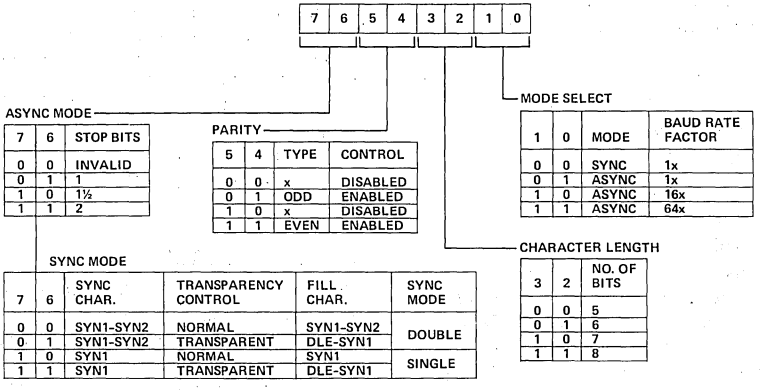


Figure 2. Mode Register 1

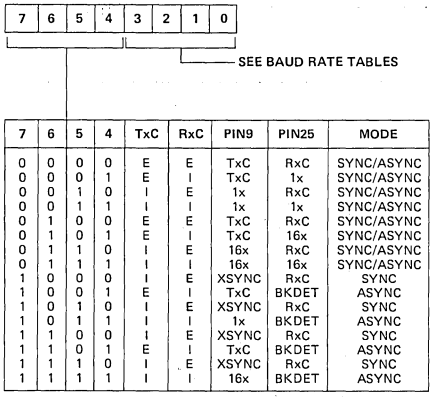


Figure 3. Mode Register 2

COMMAND REGISTER (CR)

CR0 (TxEN) will enable or disable the transmitter. When TxEN = 0, TxD, $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are all high, the transmitter is disabled. When TxEN goes active, $\overline{\text{TxRDY}}$ will go low requesting the first character to be written to the TxHR, and the TxD output will be enabled to transmit. When TxEN goes inactive, the UPCI will complete transmission of any character still in the TxSR. TxD will then go to the marking state and $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high. Refer to Transmit timing diagram.

CR1 controls the $\overline{\text{DTR}}$ output. The $\overline{\text{DTR}}$ output is a logical complement of CR1.

CR2 (RxEN) will enable or disable the receiver. When RxEN = 0, the receiver is in an idle mode with $\overline{\text{RxRDY}}$ high. A 0 to 1 transition of RxEN will initiate a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission. A 1 to 0 transition of RxEN immediately terminates receiver operation.

In the asynchronous mode setting CR3 will force the TxD output low (break condition) at the end of the current transmitted character. TxD will then remain low until CR3 is cleared; at that time TxD will go high for a minimum 1 bit time before resuming normal transmission.

In the synchronous mode setting CR3 will force the transmission of the DLE character prior to sending the character in the TxHR. Because this is a one-time command, bit 3 will automatically reset.

CR5 controls the state of the $\overline{\text{RTS}}$ output. When CR5 = 1, $\overline{\text{RTS}}$ will go low and the transmit logic will be enabled. A 1 to 0 transition of CR5 will cause $\overline{\text{RTS}}$ to go high one TxC time after the last serial bit is transmitted, (if the TxSR was not already empty).

CR7 and CR6 provide four alternate modes of operation in both synchronous and asynchronous operation. When both bits are 0 normal operation is selected.

In the asynchronous mode, when only CR6 is set automatic echo mode is selected. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled

(CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{\text{TxRDY}}$ output = 1.
4. The $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In the synchronous mode, when only CR6 is set automatic SYN/DLE stripping is performed. The state of MR17 and MR16 controls which characters are stripped. Reference Figure 6 for a detailed example of the characters stripped. Note: automatic stripping does not affect setting of the SYN and DLE detect status bits.

Two diagnostic modes are achievable in both synchronous and asynchronous operation; local loop back with CR7 = 1 and CR6 = 0, and remote loopback with both bits = 1.

Local Loop Back

1. The transmitter output is connected to the receiver input.
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$ and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ and $\overline{\text{TxD}}$ outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and RxD inputs are ignored.

Note: CR bits 0, 1 and 5 must be set, CR2 is a don't care.

Remote Loop Back

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

STATUS REGISTER

SR0 is the transmitter ready (TxRDY) status, it is the logical complement of the $\overline{\text{TxRDY}}$ output. This bit indicates the state of the TxHR when the transmitter is enabled (TxEN = 1). A 0 indicates TxHR is full, a 1 indicates TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN = 0). Note: SR0 is not set in either the auto echo or remote loop back modes.

SR1 is the receiver ready (RxRDY) status, it is the logical complement of the $\overline{\text{RxRDY}}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN = 1). A 0 indicates the RxHR is empty, a 1 indicates the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver. (RxEN = 0).

SR2 indicates a change of state of either $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ or that the TxSR is empty. This bit is the logical complement of the $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ output. A read of the status register will clear bit 2 if a state change on $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ has occurred. If a

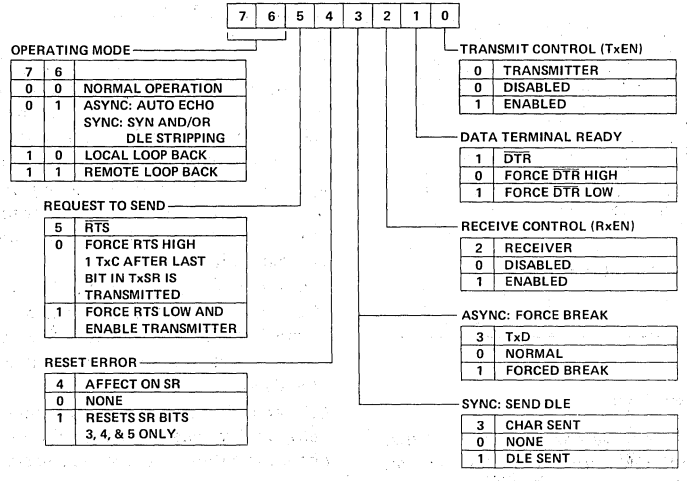


Figure 4. Command Register

second successive read of the status register indicates bit 2 = 0, then $\overline{DCD}$ or $\overline{DSR}$ changed. If bit 2 is still set, then the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status will not be reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note: $\overline{TxEMT}$ status will be set in synchronous mode even though "fill" characters are being transmitted.

SR3 when set reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes. In the synchronous transparent mode, (MR16 = 1) and the parity enable bit (MR14) is 0, SR3 will then indicate DLE detect when set. This indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

SR4 indicates an overrun error when set. An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) SR4 is cleared by the reset error command and when the receiver is disabled.

In the asynchronous mode SR5 indicates that the received character was not framed by a stop bit. If the RxHR is all 0's when bit 5 is set, a break condition was present. In synchronous non-transparent mode, it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. Their state is the logical complement of their respective inputs.

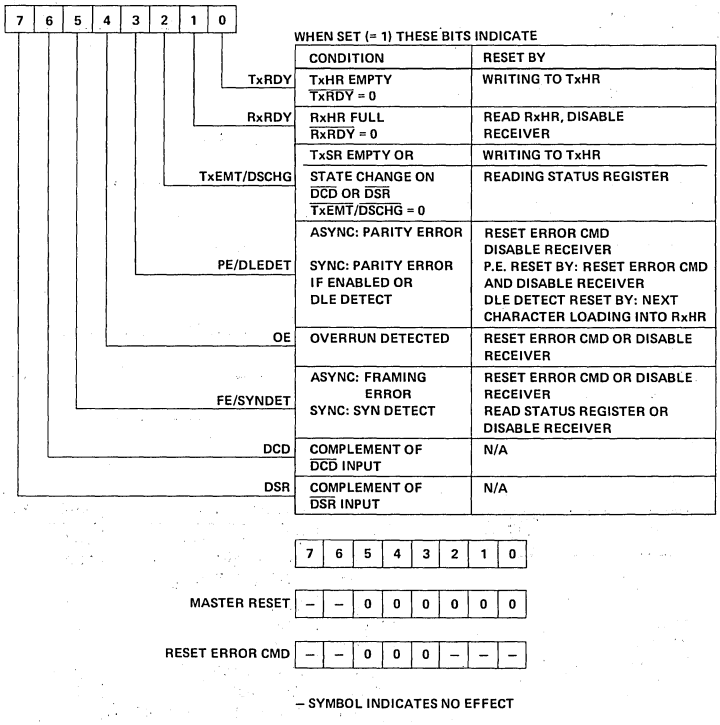


Figure 5. Status Register

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	−0.3°V to +7.0V
Input/Output Voltage	V_{IN}	−0.3°V to +7.0V
Operating Temperature	T_{OP}	0°C to 70°C
Storage Temperature	T_{STG}	−55°C to 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

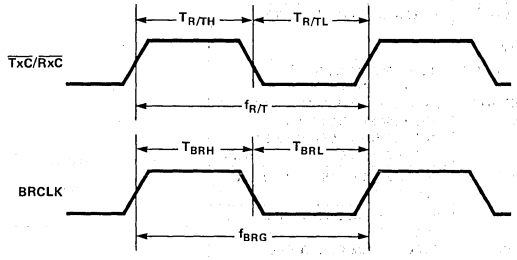
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted

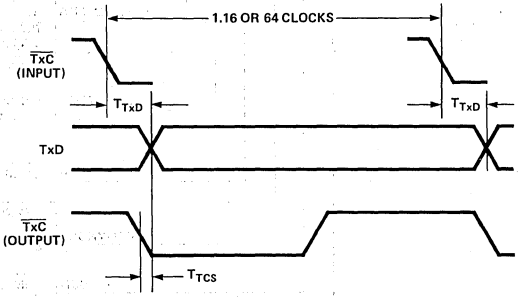
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current V_{IN} = 0 to 5.5V	I_{IN}			10	μA
Input Leakage Current for High Impedance State	I_{TSI}			10	μA
Output High Voltage: I_{LOAD} = −400 μA	V_{OH}	2.4			V
Output Low Voltage: I_{LOAD} = 2.2 mA	V_{OL}			0.4	V
Input Capacitance: f_C = 1 MHz	C_{IN}			20	pF
Output Capacitance	C_{OUT}			20	pF
Power Dissipation (V_{CC} = 5.25V)	P_D			800	mW

RECEIVER/TRANSMITTER SIGNAL TIMING

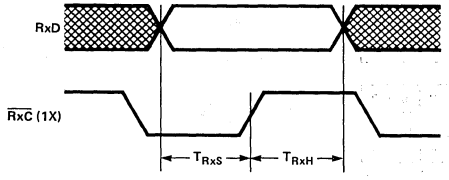
CLOCKS



TRANSMIT TIMING



RECEIVE TIMING

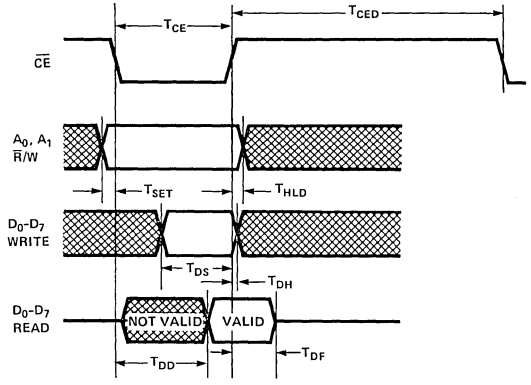


Symbol	Characteristic	MIN	TYP	MAX	UNIT
T_R/TH	$\overline{TxC}$ or $\overline{RxC}$ HIGH	500			ns
T_R/TL	$\overline{TxC}$ or $\overline{RxC}$ LOW	500		1.0	ns
f R/T	$\overline{TxC}$ or $\overline{RxC}$ freq.	DC		1.0	MHz
T_{BRH}	BRCLK HIGH	70			ns
T_{BRL}	BRCLK LOW	70			ns
f BRG	BRCLK freq. [1]		4,9152		MHz
T_{RxS}	RxD SETUP	300			ns
T_{RxH}	RxD HOLD	350			ns
T_{TxD}	TxD DELAY FROM $\overline{TxC}$ C_L = 150 pF			650	ns
T_{TCS}	SKEW TxD vs $\overline{TxC}$ C_L = 150 pF		0		ns

Note:
1. F_{BRG} = 4.9152 applicable for -1 and -2, F_{BRG} = 5.0688 for -3.

READ/WRITE TIMING CHARACTERISTICS

V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted



Symbol	Characteristic	MIN	MAX	UNIT
T_{CE}	$\overline{CE}$ Pulse Width	250		ns
T_{CED}	$\overline{CE}$ to $\overline{CE}$ Delay	600		ns
T_{SET}	Address and R/$\overline{W}$ Set Up	10		ns
T_{HLD}	Address and R/$\overline{W}$ Hold	10		ns
T_{DS}	Write Data Set Up	150		ns
T_{DH}	Write Data Hold	0		ns
T_{DD}	Read Data Delay C_L = 150 pF		200	ns
T_{DF}	READ DATA HOLD C_L = 150 pF		100	ns

Table 3 Effect of MR17 and MR16 on Character Fill and Character Stripping (Synchronous Mode)

MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7 = 0, CR6 = 1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2[1]
1	0	Single SYN Normal	SYN1	SYN1	SYN1[1]
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1[1] SYN1-SYN2[1] (Only Initial Synchronizing Sequence) DLE (also Sets SR3 if Parity Disabled and it is not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1[1] SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

Note:

1. Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of a DLE-SYN1 pair.

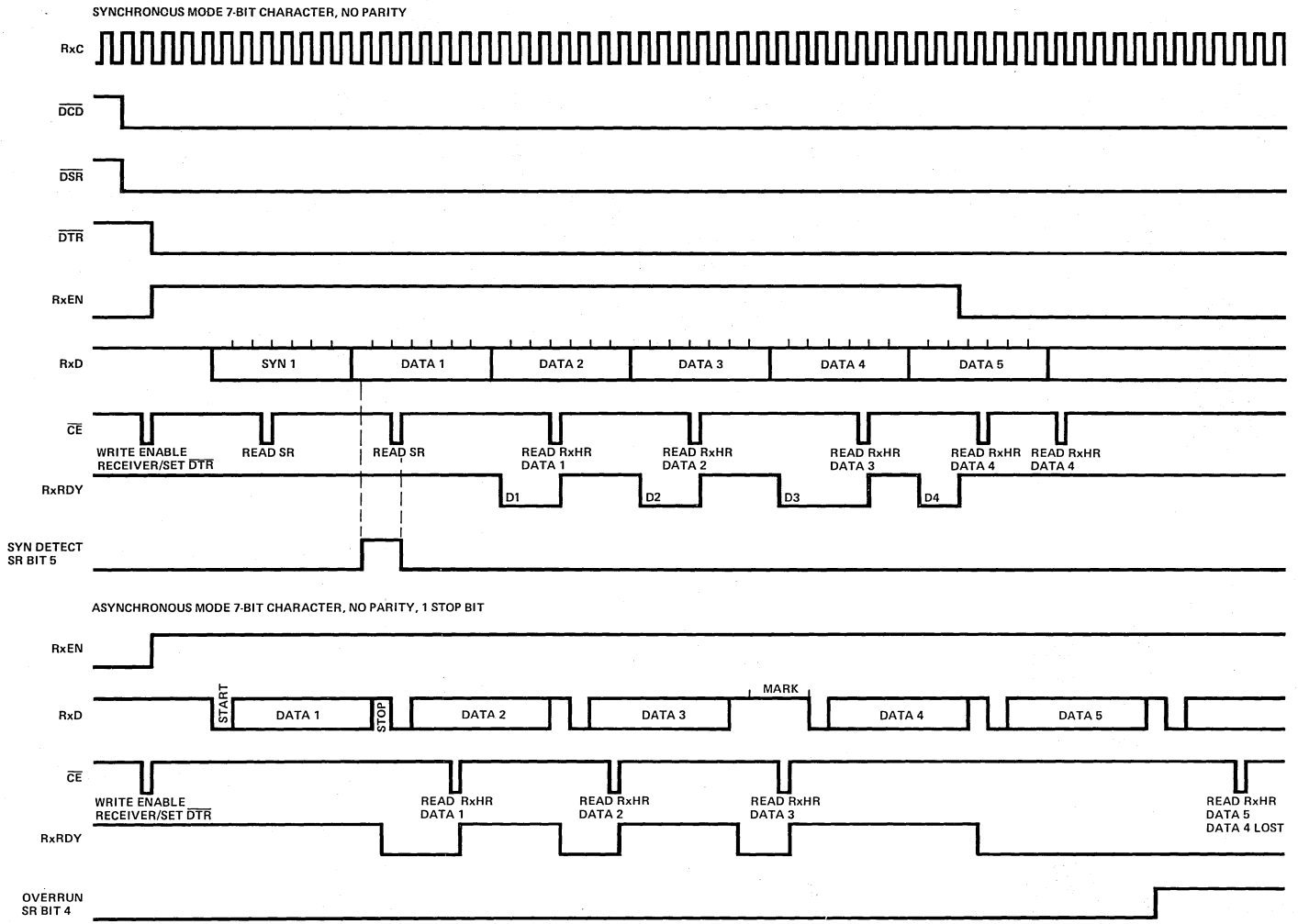


Figure 6. Receiver Operation Timing Diagram

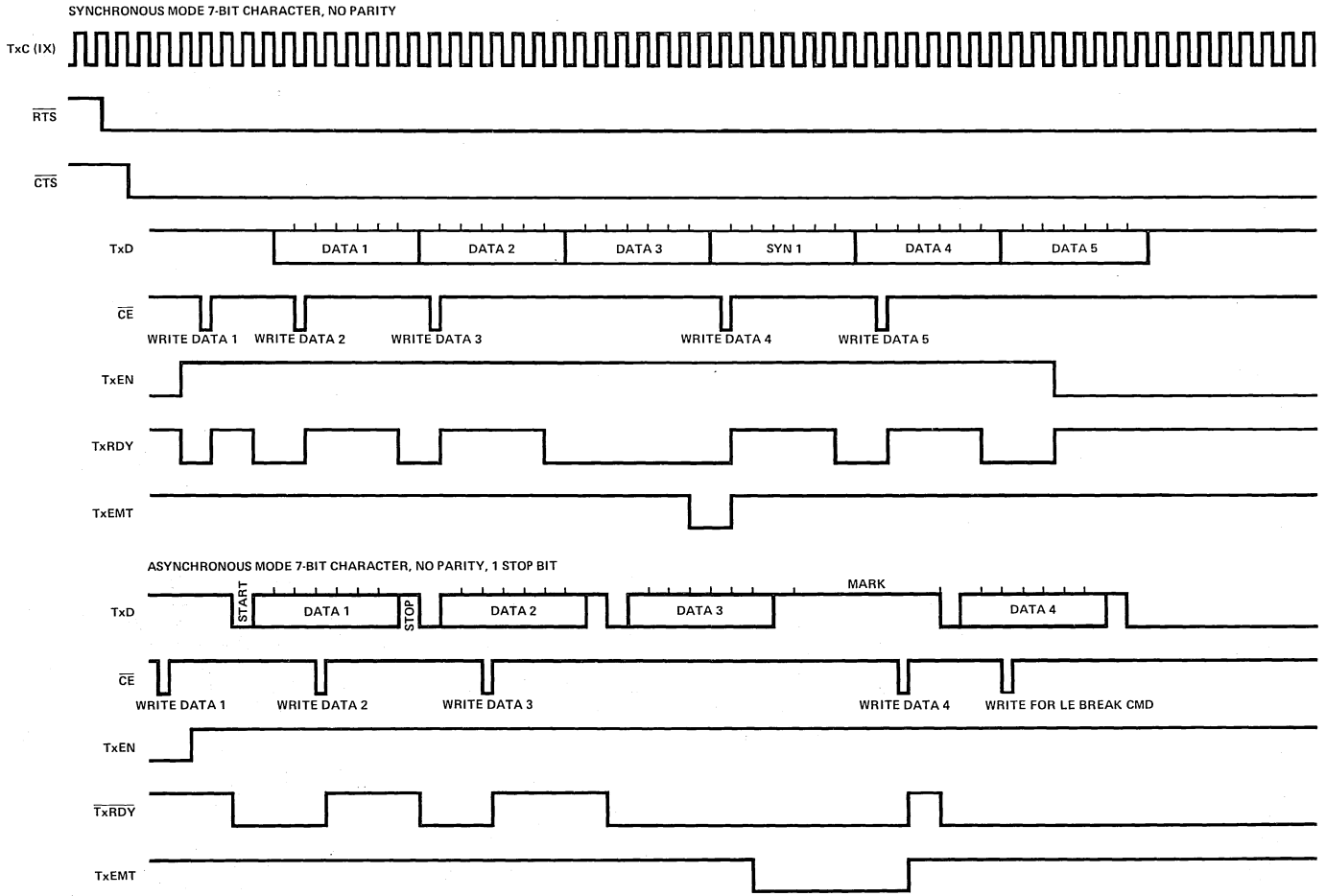


Figure 7. Transmitter Operation Timing Diagram

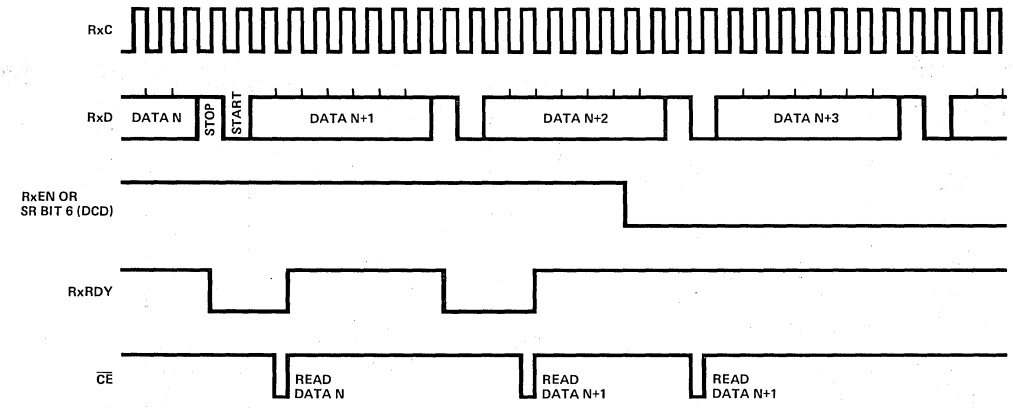


Figure 8. Asynchronous Receiver Operation with Loss of $\overline{DCD}$ or Disabling RxEN

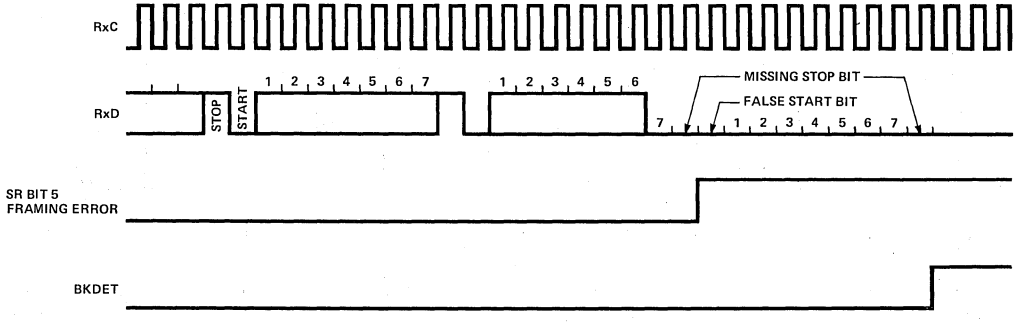
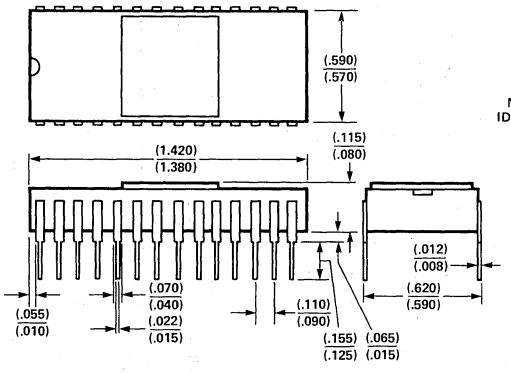


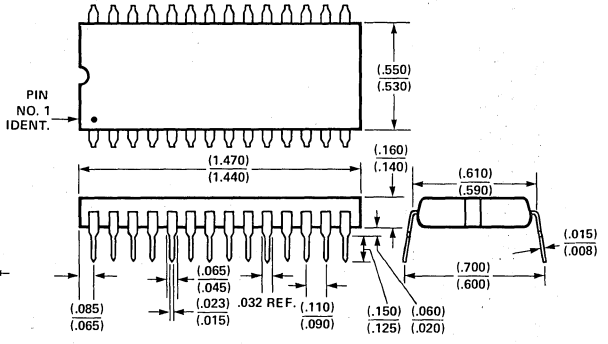
Figure 9. Framing Error and Break Detection Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



8-Bit Microprocessor Family

SY6500

MICROPROCESSOR PRODUCTS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Single 5 V ±5% power supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus
- Instruction decoding and control
- Addressable memory range of up to 65 K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, 3 MHz and 4 MHz operation
- On-chip clock options
  * External single clock input
  * Crystal time base input
- 40 and 28 pin package versions
- Pipeline architecture

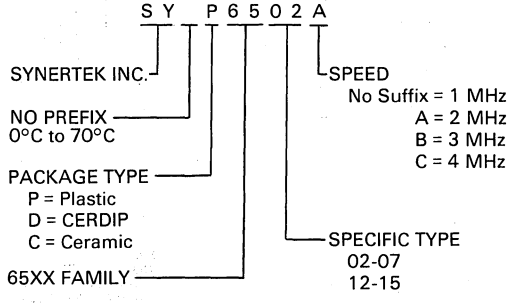
The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SY6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz, 3 MHz and 4 MHz maximum operating frequencies.

MEMBERS OF THE FAMILY

PART NUMBERS	CLOCKS	PINS	$\overline{IRQ}$	$\overline{NMI}$	RYD	ADDRESSING
SY6502	On-Chip	40	√	√	√	64 K
SY6503	"	28	√	√		4 K
SY6504	"	28	√			8 K
SY6505	"	28	√		√	4 K
SY6506	"	28	√			4 K
SY6507	"	28			√	8 K
SY6512	External	40	√	√	√	64 K
SY6513	"	28	√	√		4 K
SY6514	"	28	√			8 K
SY6515	"	28	√		√	4 K

ORDERING INFORMATION

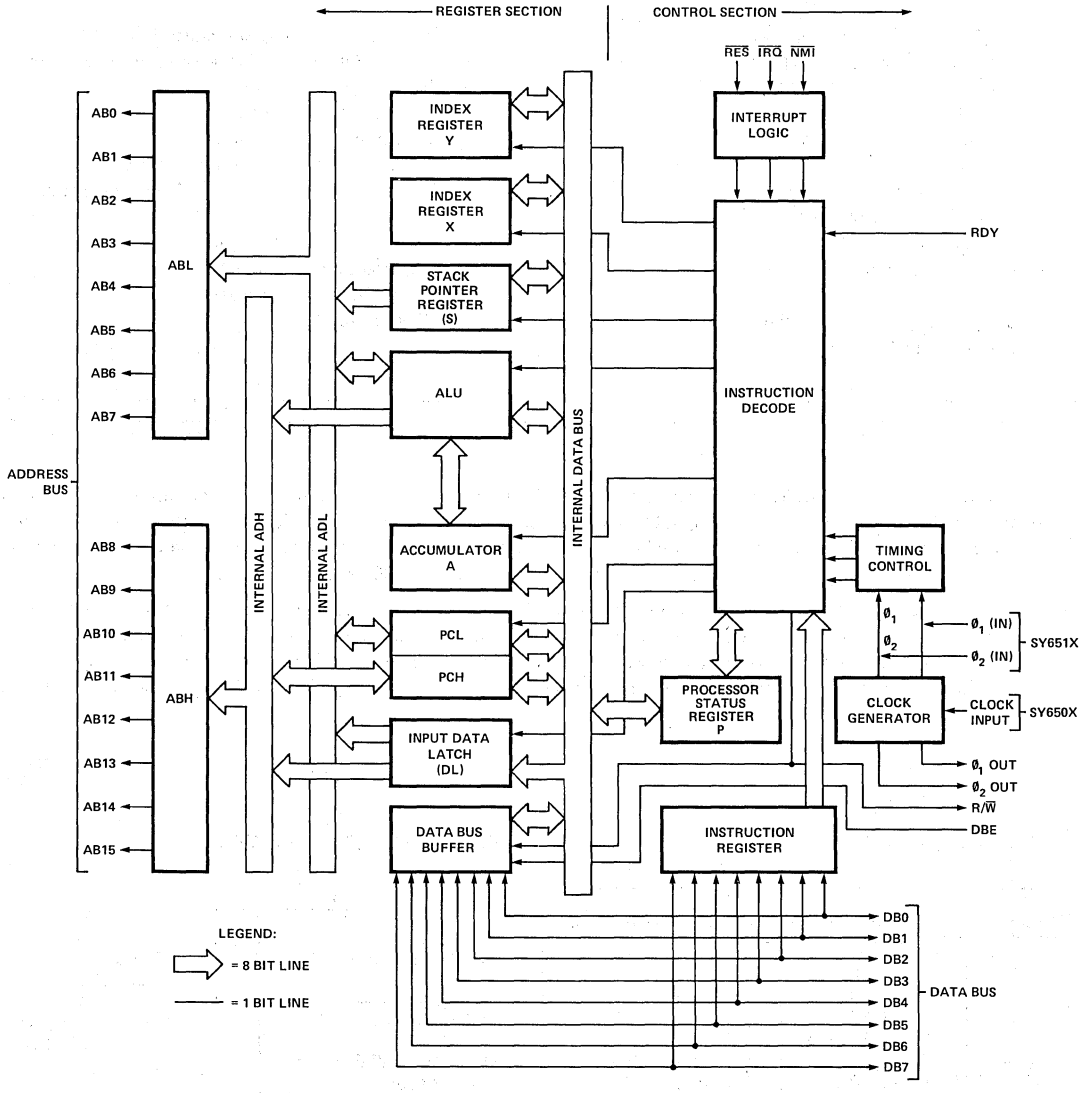


Only 6502 and 6512 are available in 3 and 4 MHz

COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics" – those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

SY6500 INTERNAL ARCHITECTURE



NOTE:
1. CLOCK GENERATOR IS NOT INCLUDED ON SY651X.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE SY6500 PRODUCTS.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

COMMENT

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ±5%, T_A = 0-70°C)

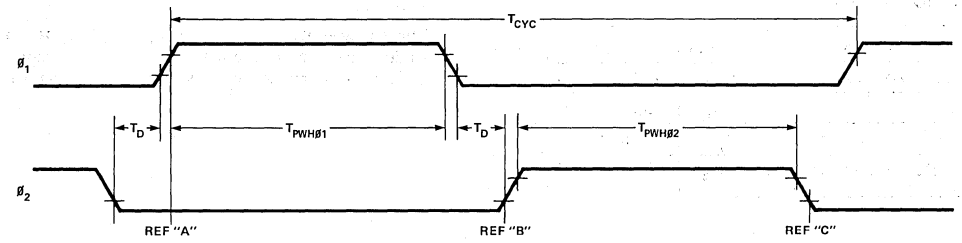
($\emptyset_1$, $\emptyset_2$ applies to SY651X, $\emptyset_{o\,(in)}$ applies to SY650X)

Symbol	Characteristic		Min.	Max.	Unit
V_{IH}	Input High Voltage				
	Logic and $\emptyset_o$ (in) for all 650X devices	1,2,3 MHz	+2.4	V_{CC}	V
		4 MHz	+3.3	V_{CC}	V
	$\emptyset_1$ and $\emptyset_2$ only for all 651X devices. Logic as 650X	All Speeds	V_{CC} −0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage				
	Logic, $\emptyset_{o\,(in)}$	(650X)	−0.3	+0.4	
	$\emptyset_1$, $\emptyset_2$	(651X)	−0.3	+0.2	V
I_{IL}	Input Loading (V_{in} = 0 V, V_{CC} = 5.25 V) RDY, S.O.		−10	−300	μA
I_{in}	Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0)				
	Logic (Excl. RDY, S.O.)		–	2.5	μA
	$\emptyset_1$, $\emptyset_2$	(651X)	–	100	μA
	$\emptyset_{o\,(in)}$	(650X)	–	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V) DB0-DB7		–	±10	μA
V_{OH}	Output High Voltage				
	(I_{LOAD} = −100μAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1,2,3 MHz	2.4	–	V
		4 MHz	2.0	–	V
V_{OL}	Output Low Voltage				
	(I_{LOAD} = 1.6mAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1,2,3 MHz	–	0.4	V
		4 MHz	–	0.8	V
P_D	Power Dissipation (V_{CC} = 5.25V)	1 MHz and 2 MHz	–	700	mW
		3 MHz	–	800	mW
		4 MHz	–	900	mW
C	Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)				
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE		–	10	pF
	DB0-DB7		–	15	
C_{out}	A0-A15, R/$\overline{W}$, SYNC		–	12	
$C_{\emptyset o(in)}$	$\emptyset_{o\,(in)}$	(650X)	–	15	
$C_{\emptyset 1}$	$\emptyset_1$	(651X)	–	50	
$C_{\emptyset 2}$	$\emptyset_2$	(651X)	–	80	

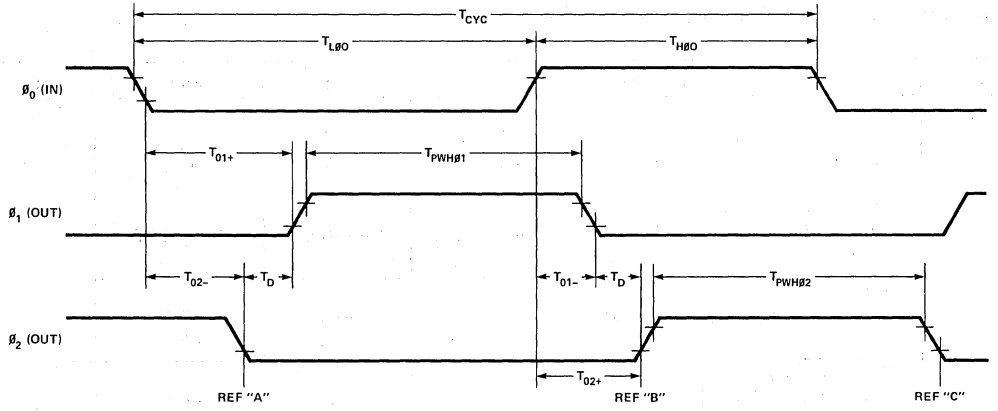
MICRO-PROCESSORS

TIMING DEFINITIONS, COMPOSITE TIMING DIAGRAM (See note at bottom of page 5)

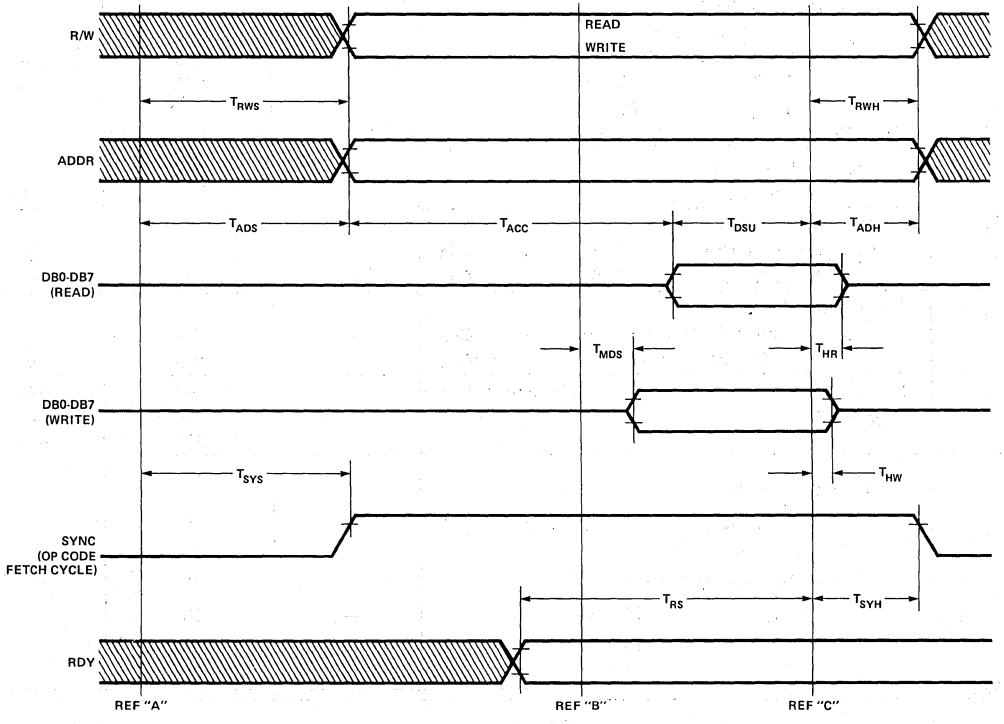
SY651X INPUT CLOCK TIMING



SY650X INPUT CLOCK TIMING



SY65XX TIMING (See note at bottom of page 5)



DYNAMIC OPERATING CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, T_A = 0° to 70°C)

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
651X										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
$Ø_1$ Pulse Width	$T_{PWHØ_1}$	430	—	215	—	150	—			ns
$Ø_2$ Pulse Width	$T_{PWHØ_2}$	470	—	235	—	160	—			ns
Delay Between $Ø_1$ and $Ø_2$	T_D	0	—	0	—	0	—			ns
$Ø_1$ and $Ø_2$ Rise and Fall Times[1]	T_R, T_F	0	25	0	20	0	15			ns
650X										
Cycle Time	T_{CYC}	1.00	40	0.50	40	0.33	40	0.25	40	μs
$Ø_{o(IN)}$ Low Time[2]	$T_{LØ_o}$	480	—	240	—	160	—	110	—	ns
$Ø_{o(IN)}$ High Time[2]	$T_{HØ_o}$	460	—	240	—	160	—	115	—	ns
$Ø_o$ Neg to $Ø_1$ Pos Delay[5]	T_{O1+}	10	70	10	70	10	70	10	70	ns
$Ø_o$ Neg to $Ø_2$ Neg Delay[5]	T_{O2-}	5	65	5	65	5	65	5	65	ns
$Ø_o$ Pos to $Ø_1$ Neg Delay[5]	T_{O1-}	5	65	5	65	5	65	5	65	ns
$Ø_o$ Pos to $Ø_2$ Pos Delay[5]	T_{O2+}	15	75	15	75	15	75	15	75	ns
$Ø_{o(IN)}$ Rise and Fall Time[1]	T_{RO}, T_{FO}	0	30	0	20	0	15	0	10	ns
$Ø_{1(OUT)}$ Pulse Width	$T_{PWHØ_1}$	$T_{LØ_o}$-20	$T_{LØ_o}$	$T_{LØ_o}$-20	$T_{LØ_o}$	$T_{LØ_o}$-20	$T_{LØ_o}$	$T_{LØ_o}$-20	$T_{LØ_o}$	ns
$Ø_{2(OUT)}$ Pulse Width	$T_{PWHØ_2}$	$T_{LØ_o}$-40	$T_{LØ_o}$-10	$T_{LØ_o}$-40	$T_{LØ_o}$-10	$T_{LØ_o}$-40	$T_{LØ_o}$-10	$T_{LØ_o}$-40	$T_{LØ_o}$-10	ns
Delay Between $Ø_1$ and $Ø_2$	T_D	5	—	5	—	5	—	5	—	ns
$Ø_1$ and $Ø_2$ Rise and Fall Times[1,3]	T_R, T_F	—	25	—	25	—	15	—	15	ns
650X, 651X										
R/$\overline{W}$ Setup Time	T_{RWS}	—	225	—	140	—	110	—	90	ns
R/$\overline{W}$ Hold Time	T_{RWH}	30	—	30	—	15	—	10	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	—	90	ns
Address Hold Time	T_{ADH}	30	—	30	—	15	—	10	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	—	110	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	20	175	20	100	20	75	—	70	ns
Write Data Hold Time	T_{HW}	60	150	60	150	30	130	20	—	ns
Sync Setup Time	T_{SYS}	—	350	—	175	—	100	—	90	ns
Sync Hold Time	T_{SYH}	30	—	30	—	15	—	15	—	ns
RDY Setup Time[4]	T_{RS}	200	—	200	—	150	—	120	—	ns

NOTES:

1. Measured between 10% and 90% points on waveform.
2. Measured at 50% points.
3. Load = 1 TTL load +30 pF.
4. RDY must never switch states within T_{RS} to end of $Ø_2$.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by a "B" suffix.
8. The 4 MHz devices are identified by a "C" suffix.

TIMING DIAGRAM NOTE:

Because the clock generation for the SY650X and SY651X is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters are referred to these lines and scale variations in the diagrams are of no consequence.

PIN FUNCTIONS

Clocks ($\emptyset_1$, $\emptyset_2$)

The SY651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The SY650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

Address Bus (A_0-A_{15}) (See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (DB_0-DB_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\emptyset_2$) clock, thus allowing data output from microprocessor only during $\emptyset_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the SY6512, only.

Ready (RDY)

This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\emptyset_1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\emptyset_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during $\emptyset_2$ time.

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vestor address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ resistor to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during $\emptyset_2$ (phase 2) and will begin the appropriate interrupt routine on the $\emptyset_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\emptyset_1$.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\emptyset_1$ of an OP. CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\emptyset_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset ($\overline{RES}$)

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/$\overline{W}$ and SYNC signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Read/Write (R/$\overline{W}$)

This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/$\overline{W}$ signifies data into the processor; a low is for data transfer out of the processor.

PROGRAMMING CHARACTERISTICS

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry	DEC	Decrement Memory by One	PHA	Push Accumulator on Stack
AND	"AND" Memory with Accumulator	DEX	Decrement Index X by One	PHP	Push Processor Status on Stack
ASL	Shift left One Bit (Memory or Accumulator)	DEY	Decrement Index Y by One	PLA	Pull Accumulator from Stack
				PLP	Pull Processor Status from Stack
BCC	Branch on Carry Clear	EOR	"Exclusive-or" Memory with Accumulator		
BCS	Branch on Carry Set			ROL	Rotate One Bit Left (Memory or Accumulator)
BEQ	Branch on Result Zero	INC	Increment Memory by One	ROR	Rotate One Bit Right (Memory or Accumulator)
BIT	Test Bits in Memory with Accumulator	INX	Increment Index X by One	RTI	Return from Interrupt
BMI	Branch on Result Minus	INY	Increment Index Y by One	RTS	Return from Subroutine
BNE	Branch on Result not Zero				
BPL	Branch on Result Plus	JMP	Jump to New Location	SBC	Subtract Memory from Accumulator with Borrow
BRK	Force Break	JSR	Jump to New Location Saving Return Address	SEC	Set Carry Flag
BVC	Branch on Overflow Clear			SED	Set Decimal Mode
BVS	Branch on Overflow Set	LDA	Load Accumulator with Memory	SEI	Set Interupt Disable Status
		LDX	Load Index X with Memory	STA	Store Accumulator in Memory
CLC	Clear Carry Flag	LDY	Load Index Y with Memory	STX	Store Index X in Memory
CLD	Clear Decimal Mode	LSR	Shift One Bit Right (Memory or Accumulator)	STY	Store Index Y in Memory
CLI	Clear Interrupt Disable Bit				
CLV	Clear Overflow Flag	NOP	No Operation	TAX	Transfer Accumulator to Index X
CMP	Compare Memory and Accumulator			TAY	Transfer Accumulator to Index Y
CPX	Compare Memory and Index X	ORA	"OR" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
CPY	Compare Memory and Index Y			TXA	Transfer Index X to Accumulator
				TXS	Transfer Index X to Stack Pointer
				TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

Accumulator Addressing

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

Absolute Addressing

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

Zero Page Addressing

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

Indexed Zero Page Addressing – (X, Y indexing)

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calcuated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

Indexed Absolute Addressing – (X, Y indexing)

This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Relative Addressing

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is –128 to +127 bytes from the next instruction.

Indexed Indirect Addressing

In indexed indirect addressing (referred to as (Indirect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Indirect Indexed Addressing

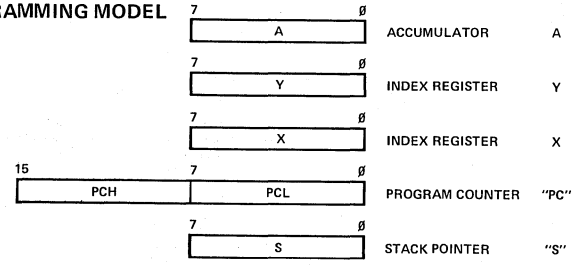
In indirect indexed addressing (referred to as (Indirect),Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

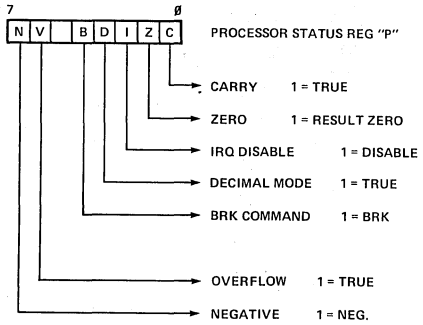
Absolute Indirect

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

PROGRAMMING CHARACTERISTICS

PROGRAMMING MODEL





INSTRUCTION SET – OP CODES, EXECUTION TIME, MEMORY REQUIREMENTS

MNEMONIC	OPERATION	IMMEDIATE OP	N	#	ABSOLUTE OP	N	#	ZERO PAGE OP	N	#	ACCUM OP	N	#	IMPLIED OP	N	#	(IND, X) OP	N	#	(IND), Y OP	N	#	Z, PAGE X OP	N	#	ABS, X OP	N	#	ABS, Y OP	N	#	RELATIVE OP	N	#	INDIRECT OP	N	#	Z, PAGE Y OP	N	#	CONDITION CODES N	Z	C	I	D	V
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3									✓	✓	✓	–	–	✓
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3									✓	✓	–	–	–	–
ASL	C ← 7 0 ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3												✓	✓	✓	–	–	–
BCC	BRANCH ON C=0 (2)																															90	2	2							–	–	–	–	–	–
BCS	BRANCH ON C=1 (2)																															B0	2	2							–	–	–	–	–	–
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							–	–	–	–	–	–
BIT	A ∧ M				2C	4	3	24	3	2																															M_7	✓	–	–	–	M_6
BMI	BRANCH ON N=1 (2)																															30	2	2							–	–	–	–	–	–
BNE	BRANCH ON Z=0 (2)																															D0	2	2							–	–	–	–	–	–
BPL	BRANCH ON N=0 (2)																															10	2	2							–	–	–	–	–	–
BRK	(See Fig. 1)													00	7	1																									–	–	–	✓	–	–
BVC	BRANCH ON V=0 (2)																															50	2	2							–	–	–	–	–	–
BVS	BRANCH ON V=1 (2)																															70	2	2							–	–	–	–	–	–
CLC	0 → C													18	2	1																									–	–	0	–	–	–
CLD	0 → D													D8	2	1																									–	–	–	–	0	–
CLI	0 → I													58	2	1																									–	–	–	0	–	–
CLV	0 → V													B8	2	1																									–	–	–	–	–	0
CMP	A-M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3									✓	✓	✓	–	–	–
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	–	–	–
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	–	–	–
DEC	M-1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3												✓	✓	–	–	–	–
DEX	X-1 → X													CA	2	1																									✓	✓	–	–	–	–
DEY	Y-1 → Y													88	2	1																									✓	✓	–	–	–	–
EOR	A ∀ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3									✓	✓	–	–	–	–
INC	M+1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3												✓	✓	–	–	–	–
INX	X+1 → X													E8	2	1																									✓	✓	–	–	–	–
INY	Y+1 → Y													C8	2	1																									✓	✓	–	–	–	–
JMP	JUMP TO NEW LOC				4C	3	3																													6C	5	3				–	–	–	–	–	–
JSR	(See Fig. 2) JUMP SUB				20	6	3																																		–	–	–	–	–	–
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3									✓	✓	–	–	–	–

MNEMONIC	OPERATION	IMMEDIATE OP	N	#	ABSOLUTE OP	N	#	ZERO PAGE OP	N	#	ACCUM OP	N	#	IMPLIED OP	N	#	(IND, X) OP	N	#	(IND), Y OP	N	#	Z, PAGE X OP	N	#	ABS, X OP	N	#	ABS, Y OP	N	#	RELATIVE OP	N	#	INDIRECT OP	N	#	Z, PAGE, Y OP	N	#	CONDITION CODES N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	✓	✓	–	–	–	–
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3												✓	✓	–	–	–	–
LSR	0 → 7 0 → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3												0	✓	✓	–	–	–
NOP	NO OPERATION													EA	2	1																									–	–	–	–	–	–
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3									✓	✓	–	–	–	–
PHA	A → Ms S-1 → S													48	3	1																									–	–	–	–	–	–
PHP	P → Ms S-1 → S													08	3	1																									–	–	–	–	–	–
PLA	S+1 → S Ms → A													68	4	1																									✓	✓	–	–	–	–
PLP	S+1 → S Ms → P													28	4	1																									(RESTORED)					
ROL	7 0 ← C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3												✓	✓	✓	–	–	–
ROR	C → 7 0				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3												✓	✓	✓	–	–	–
RTI	(See Fig. 1) RTRN INT.													40	6	1																									(RESTORED)					
RTS	(See Fig. 2) RTRN SUB													60	6	1																									–	–	–	–	–	–
SBC	A-M-$\bar{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3									✓	✓	(3)	–	–	✓
SEC	1 → C													38	2	1																									–	–	1	–	–	–
SED	1 → D													F8	2	1																									–	–	–	–	1	–
SEI	1 → I													78	2	1																									–	–	–	1	–	–
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3									–	–	–	–	–	–
STX	X → M				8E	4	3	86	3	2																															96	4	2	–	–	–	–	–	–
STY	Y → M				8C	4	3	84	3	2													94	4	2																	–	–	–	–	–	–
TAX	A → X													AA	2	1																									✓	✓	–	–	–	–
TAY	A → Y													A8	2	1																									✓	✓	–	–	–	–
TSX	S → X													BA	2	1																									✓	✓	–	–	–	–
TXA	X → A													8A	2	1																									✓	✓	–	–	–	–
TXS	X → S													9A	2	1																									–	–	–	–	–	–
TYA	Y → A													98	2	1																									✓	✓	–	–	–	–

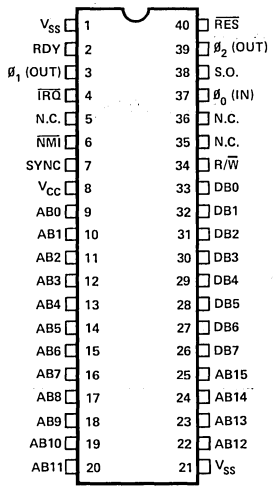
(1) ADD 1 TO "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BELOW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
-- SUBTRACT
∧ AND
∨ OR
∀ EXCLUSIVE OR
✓ MODIFIED

– NOT MODIFIED
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
N NO. CYCLES
NO. BYTES

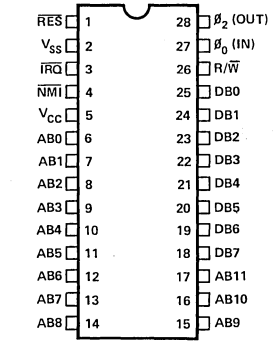
SY6502 – 40 Pin Package



Features

- 65K Addressable Bytes of Memory
- IRQ Interrupt
- NMI Interrupt
- On-the-chip Clock
  - √ TTL Level Single Phase Input
  - √ Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used for single cycle execution)
- Two Phase Output Clock for Timing of Support Chips

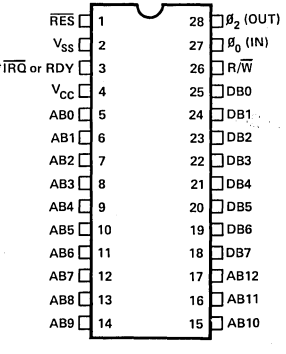
SY6503 – 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bi-Directional Data Bus

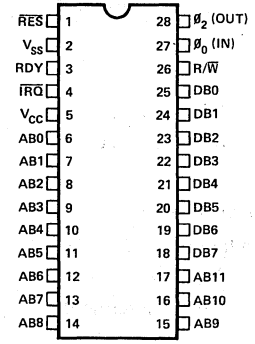
SY6504 & SY6507 – 28 Pin Package



Features

- IRQ Interrupt (6504 only)
- RDY Signal (6507 only)
- 8K Addressable Bytes of Memory (AB00-AB12)
- On-the-chip Clock
- 8 Bit Bi-Directional Data Bus

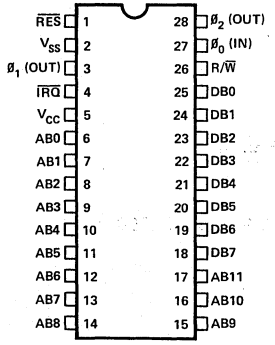
SY6505 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus

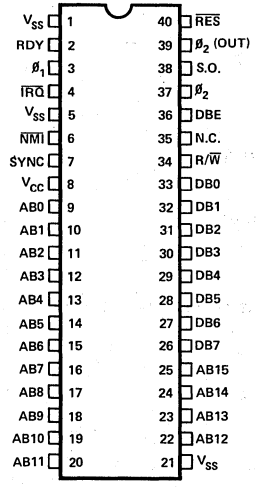
SY6506 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phases off
- 8 Bit Bi-Directional Data Bus

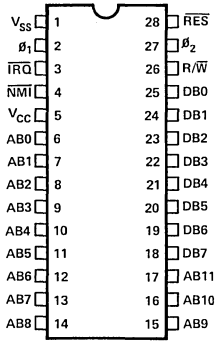
SY6512 — 40 Pin Package



Features

- 65K Addressable Bytes of Memory
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bi-Directional Data Bus
- SYNC Signal
- Two phase input
- Data Bus Enable

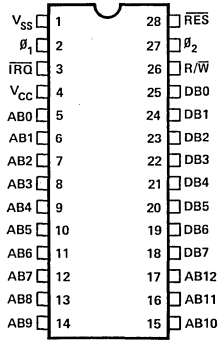
SY6513 — 28 Pin Package



Features

- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bi-Directional Data Bus

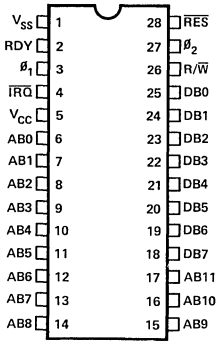
SY6514 — 28 Pin Package



Features

- 8K Addressable Bytes of Memory (AB00-AB12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bi-Directional Data Bus

SY6515 — 28 Pin Package

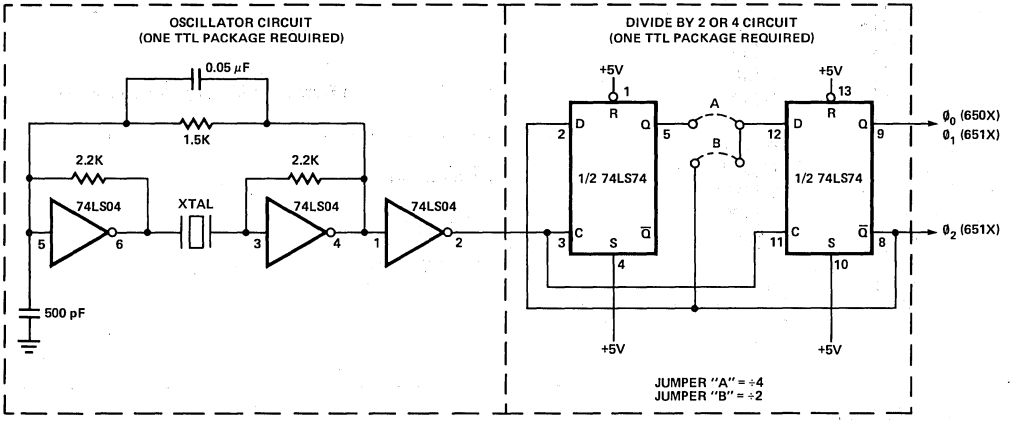


Features

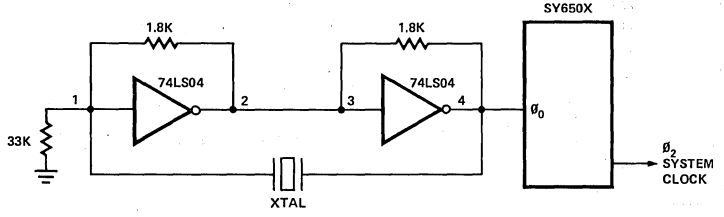
- 4K Addressable Bytes of Memory (AB00-AB11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bi-Directional Data Bus

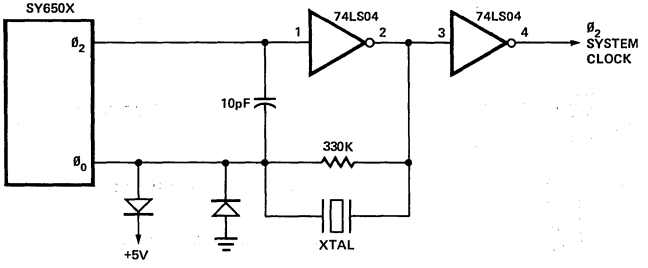
CLOCK GENERATION CIRCUITS*

*For further details refer to Synertek SY6500 Applications Information Note AN2. Crystals used are CTS Knight MP Series or equivalents. (Series Mode)



CRYSTAL FREQUENCY	OUTPUT FREQUENCY	
	÷2	÷4
3.579545 MHz	1.7897 MHz	0.894886 MHz
4.194304 MHz	2.097152 MHz	1.048576 MHz





SYNERTEK
A SUBSIDIARY OF HONEYWELL

8-Bit Microprocessor Family

Extended Temperature (-40° C to +85° C)

SYE6500
SYE6500A
MICROPROCESSOR PRODUCTS

- Single 5 V ±5% power supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus
- Instruction decoding and control
- Addressable memory range of up to 65 K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1 MHz and 2 MHz operation
- On-chip clock options
  * External single clock input
  * Crystal time base input
- 40 and 28 pin package versions
- Pipeline architecture
- Operation over wide temperature range (-40°C to +85°C)

The SYE6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SYE6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz and 2 MHz maximum operating frequencies.

MEMBERS OF THE FAMILY

PART NUMBERS			CLOCKS	PINS	$\overline{IRQ}$	$\overline{NMI}$	RDY	ADDRESSING
Plastic	Cerdip	Ceramic						
SYEP6502	SYED6502	SYEC6502	On-Chip	40	√	√	√	16 (64 K)
SYEP6503	SYED6503	SYEC6503	"	28	√	√		12 (4 K)
SYEP6504	SYED6504	SYEC6504	"	28	√			13 (8 K)
SYEP6505	SYED6505	SYEC6505	"	28	√		√	12 (4 K)
SYEP6506	SYED6506	SYEC6506	"	28	√			12 (4 K)
SYEP6507	SYED6507	SYEC6507	"	28			√	13 (8 K)
SYEP6512	SYED6512	SYEC6512	External	40	√	√	√	16 (64 K)
SYEP6513	SYED6513	SYEC6513	"	28	√	√		12 (4 K)
SYEP6514	SYED6514	SYEC6514	"	28	√			13 (8 K)
SYEP6515	SYED6515	SYEC6515	"	28	√		√	12 (4 K)

D.C. CHARACTERISTICS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

COMMENT

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = -40°C to +85°C)

(ϕ_1, ϕ_2 applies to SYE651X, $\phi_{0\,(in)}$ applies to SYE650X)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage			
	Logic, $\phi_{o\,(in)}$ (650X)	+2.4	V_{CC}	
	ϕ_1, ϕ_2 (651X)	V_{CC} - 0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage			
	Logic, $\phi_{o\,(in)}$ (650X)	-0.3	+0.4	
	ϕ_1, ϕ_2 (651X)	-0.3	+0.2	V
I_{IL}	Input Loading (V_{in} = 0 V, V_{CC} = 5.25 V) RDY, S.O.	-10	-300	μA
I_{in}	Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0)			
	Logic (Excl. RDY, S.O.)	–	2.5	μA
	ϕ_1, ϕ_2 (651X)	–	100	μA
	$\phi_{o\,(in)}$ (650X)	–	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V) DB0-DB7	–	10	μA
V_{OH}	Output High Voltage (I_{LOAD} = -100μAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/W	2.4	–	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/W	–	0.4	V
P_D	Power Dissipation V_{CC} = 5.25V			
	1 MHz and 2 MHz	–	700	mW
		–		
C	Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)			
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE	–	10	
	DB0-DB7	–	15	
C_{out}	A0-A15, R/W, SYNC	–	12	pF
$C_{\phi o(in)}$	$\phi_{o\,(in)}$ (650X)	–	15	
$C_{\phi 1}$	ϕ_1 (651X)	–	50	
$C_{\phi 2}$	ϕ_2 (651X)	–	80	

Note: $\overline{IRQ}$ and $\overline{NMI}$ require 3 K pull-up resistors.

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Peripheral Interface Adapter (PIA)

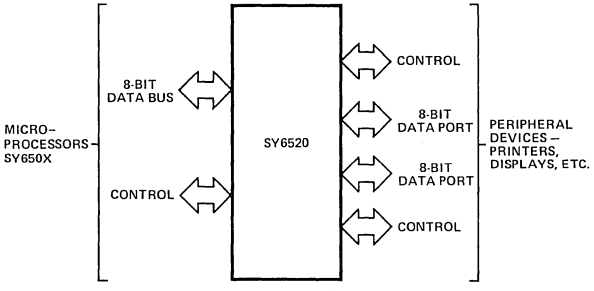
SY6520/6520A SY6820/68B20

MICROPROCESSOR PRODUCTS

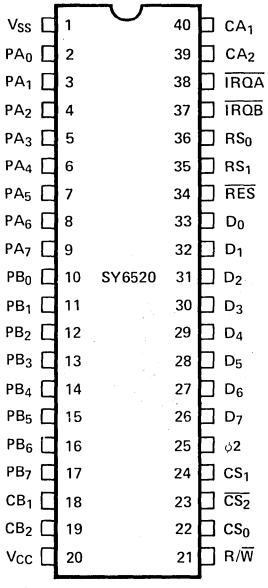
- Direct Replacement for MC6820
- Single +5V Power Supply
- Two 8-bit Bi-directional I/O Ports with Individual Data Direction Control
- CMOS-Compatible Peripheral Port A Lines
- Automatic "Handshake" Control of Data Transfers
- Programmable Interrupt Capability
- Automatic Initialization on Power Up
- 1 and 2 MHz Versions

The SY6520 Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

BASIC SY6520 INTERFACE DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	Speed
SYC6520/6820	Ceramic	1MHz
SYD6520/6820	Cerdip	1MHz
SYP6520/6820	Plastic	1MHz
SYC6520A/68B20	Ceramic	2MHz
SYD6520A/68B20	Cerdip	2MHz
SYP6520A/68B20	Plastic	2MHz

MICRO-PROCESSORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0-70°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	+2.0	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Input Leakage Current V_{IN} = 0 to 5.0 V R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	I_{IN}	–	±2.5	μA
Three-State (Off State Input Current) (V_{IN} = 0.4 to 2.4 V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	I_{TSI}	–	±10	μA
Input High Current (V_{IH} = 2.4 V), PA_0-PA_7, CA_2	I_{IH}	-100	–	μA
Input Low Current (V_{IL} = 0.4 V), PA_0-PA_7, CA_2	I_{IL}	–	1.6	mA
Output High Voltage (V_{CC} = min, I_{OH} = -100 μA)	V_{OH}	2.4	–	V
Output Low Voltage (V_{CC} = min, I_{OL} = 1.6mA)	V_{OL}	–	+0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V) (V_O = 1.5 V, the current for driving other than TTL, e.g., Darlington Base), PB_0-PB_7, CB_2	I_{OH}	-100 -1.0	– -10	μA mA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	1.6	–	mA
Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	–	10	μA
Power Dissipation (V_{CC} = 5.25 V)	P_D	–	500	mW
Input Capacitance (V_{IN} – 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, CS_2, CA_1, CB_1, ϕ_2	C_{IN}	– – –	10 7.0 20	pF
Output Capacitance (V_{IN} – 0, T_A = 25°C, f = 1.0 MHz)	C_{OUT}	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

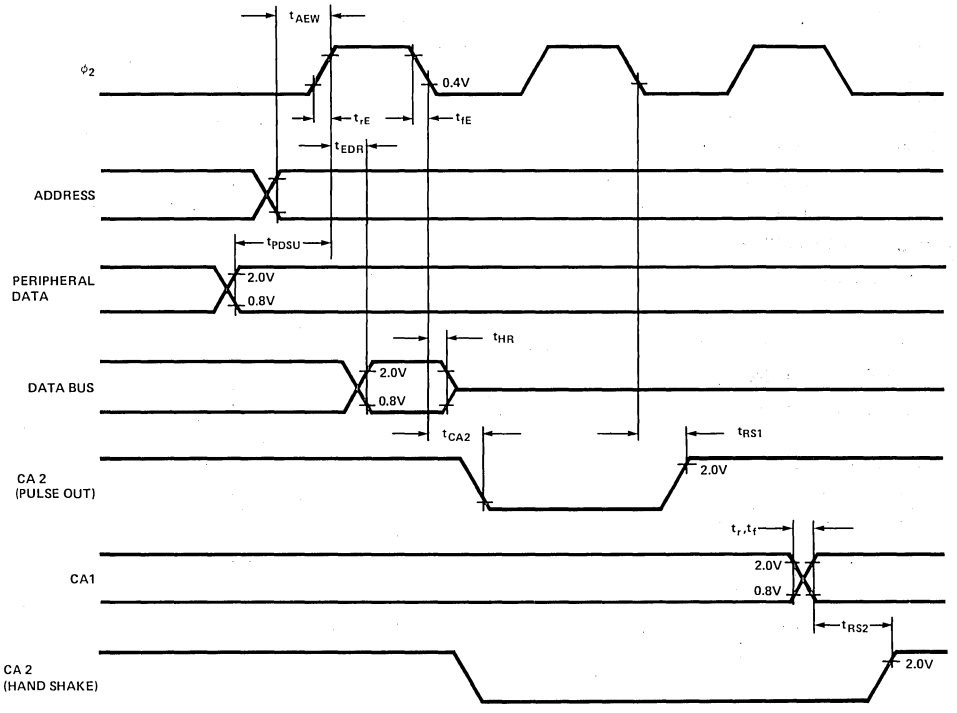


Figure 1. Read Timing Characteristics

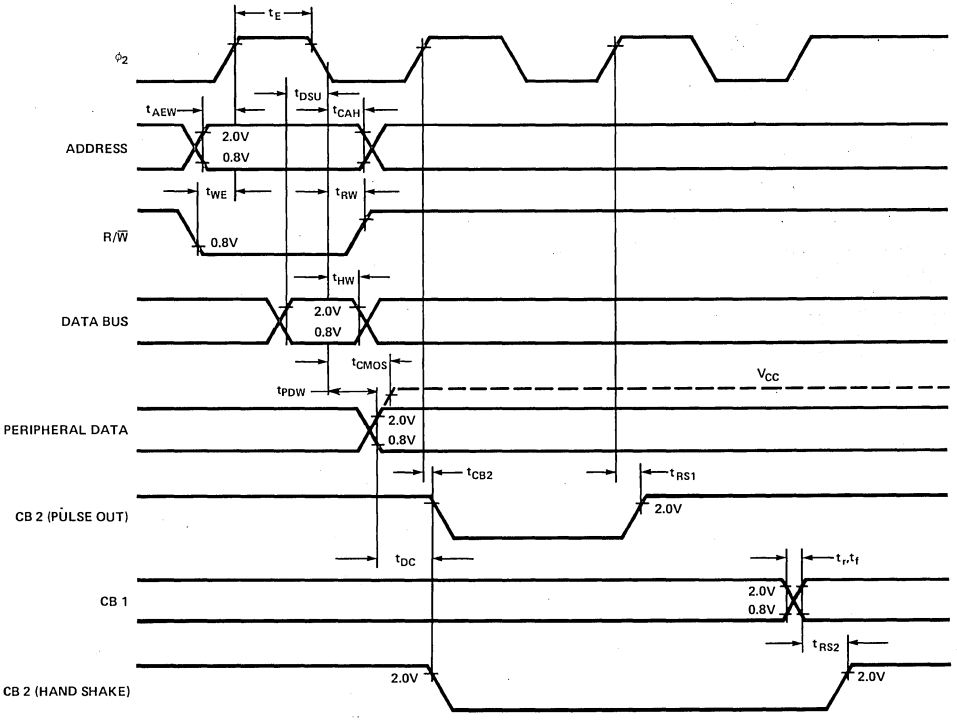
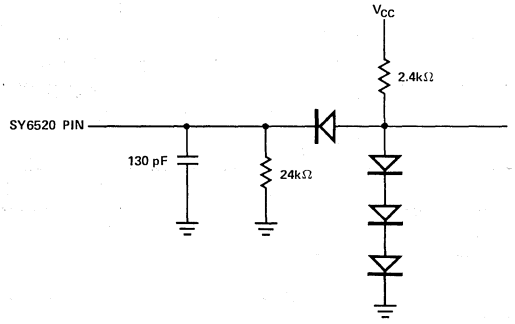


Figure 2. Write Timing Characteristics

SWITCHING CHARACTERISTICS (V_{CC} = +5V ± 5%, T_A = 0–70°C, unless otherwise noted)

Characteristic	Symbol	SY6520 (1 MHz) Min.	SY6520 (1 MHz) Max.	SY6520A (2 MHz) Min.	SY6520A (2 MHz) Max.	Unit
READ TIMING CHARACTERISTICS						
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	–	90	–	ns
Delay Time, ϕ_2 Positive Transition to Data Valid on Bus	T_{EDR}	–	395	–	190	ns
Peripheral Data Setup Time	T_{PDSU}	300	–	150	–	ns
Data Bus Hold Time	T_{HR}	10	–	10	–	ns
Delay Time, ϕ_2 Negative Transition to CA2 Negative Transition	T_{CA2}	–	1.0	–	0.5	μs
Delay Time, ϕ_2 Negative Transition to CA2 Positive Transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	–	0.5	μs
Delay Time from CA1 Active Transition to CA2 Positive Transition	T_{RS2}	–	2.0	–	1.0	μs
Rise and Fall Time for ϕ_2 Input	t_{rE}, t_{fE}	–	25	–	25	ns
WRITE TIMING CHARACTERISTICS						
ϕ_2 Pulse Width	T_E	0.440	–	0.200	–	μs
Delay Time, Address Valid to ϕ_2 Positive Transition	T_{AEW}	180	–	90	–	ns
Delay Time, Data Valid to ϕ_2 Negative Transition	T_{DSU}	300	–	150	–	ns
Delay Time, Read/Write Negative Transition to ϕ_2 Positive Transition	T_{WE}	130	–	65	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid	T_{PDW}	–	1.0	–	0.5	μs
Delay Time, ϕ_2 Negative Transition to Peripheral Data Valid CMOS (V_{CC} - 30%) PA0–PA7, CA2	T_{CMOS}	–	2.0	–	1.0	μs
Delay Time, ϕ_2 Positive Transition to CB2 Negative Transition	T_{CB2}	–	1.0	–	0.5	μs
Delay Time, Peripheral Data Valid to CB2 Negative Transition	T_{DC}	0	1.5	0	0.75	μs
Delay Time, ϕ_2 Positive Transition CB2 Positive Transition	T_{RS1}	–	1.0	–	0.5	μs
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	–	0.5	μs
Delay Time, CB1 Active Transition to CB2 Positive Transition	T_{RS2}	–	2.0	–	1.0	μs
Delay Time, ϕ_2 Negative Transition to Read/Write Positive Transition	T_{RW}	50	–	25	–	ns

TEST LOAD



INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

This signal is used to initialize the PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

ϕ_2 (Input Clock)

This input is the system ϕ_2 clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/$\overline{W}$ (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ signal permits the processor to read data supplied by the PIA; a low on the R/$\overline{W}$ signal permits the processor to Write into the PIA.

$\overline{IRQA}$, $\overline{IRQB}$ (Interrupt Requests)

$\overline{IRQA}$ and $\overline{IRQB}$ are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRQ signal input.

D_0-D_7 (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally high-impedance except when selected for a read operation.

CS0, CS1, $\overline{CS2}$ (Chip Selects)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

INTERNAL ARCHITECTURE

The SY6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 3 is a block diagram of the SY6520.

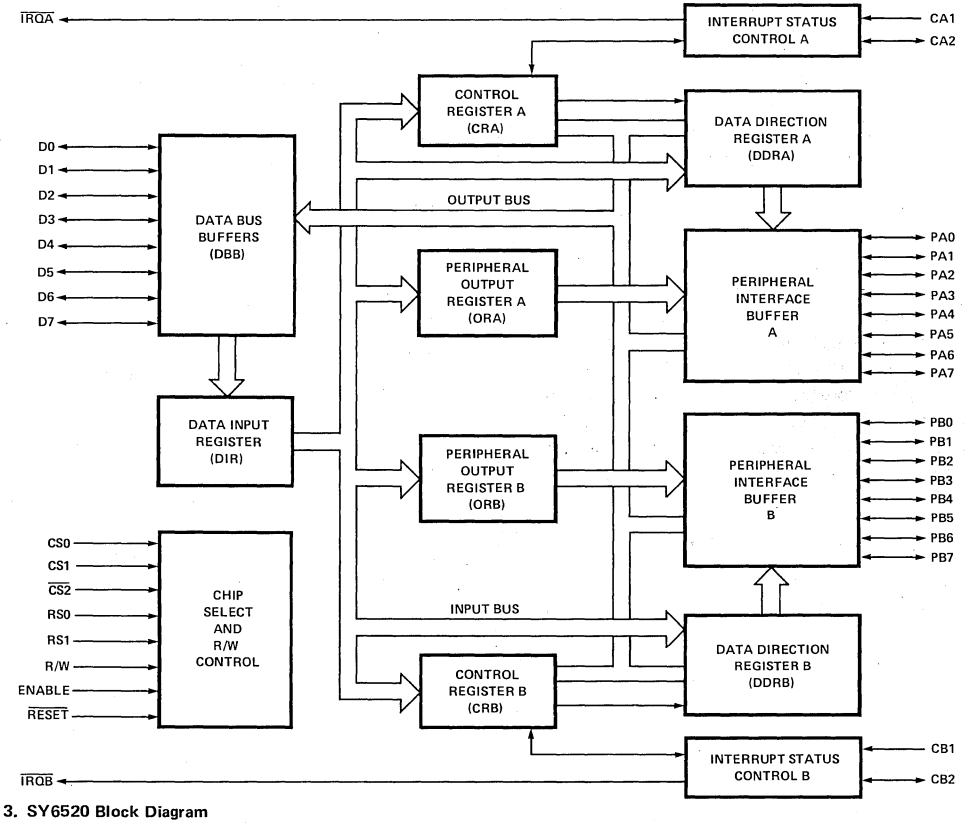


Figure 3. SY6520 Block Diagram

	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 4. Control Registers

Data Input Register

When the microprocessor writes data into the SY6520, the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the SY6520 after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($< 0.4V$) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.

FUNCTIONAL DESCRIPTION

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Figure 5.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the SY6520. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output.

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for

Register Select Pin		Data Direction Register Access Control Bit		
RS1	RS0	CRA-2	CRB-2	Register Selected
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 5. Register Addressing

those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:
$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between SY6520 and Peripheral Devices

The SY6520 provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 6. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 6 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an out-

put has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 7. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to 1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

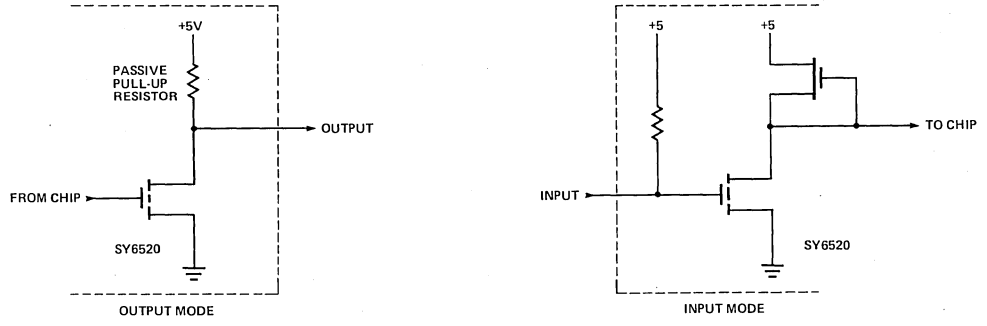


Figure 6. Port A Buffer Circuit (PA_0-PA_7)

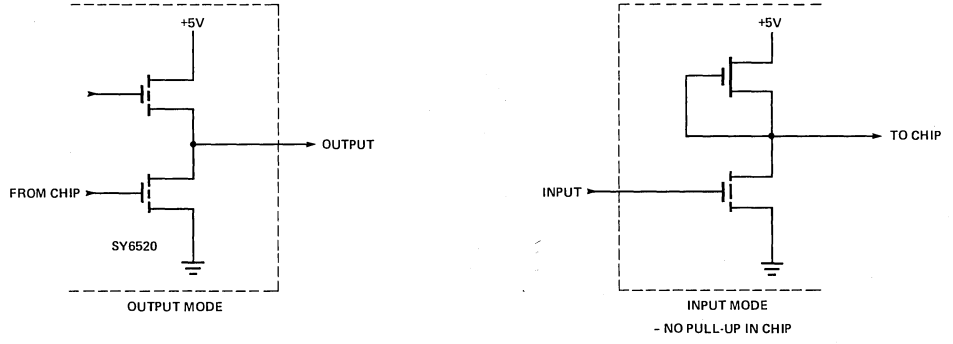


Figure 7. Port B Buffer Circuit (PB_0-PB_7)

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 8 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through $\overline{IRQA}$ if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	Negative	Disable — remain high
0	1	Negative	Enable — goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable — remain high
1	1	Positive	Enable — as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	0	Negative	Disable — remains high
0	0	1	Negative	Enable — goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable — remains high
0	1	1	Positive	Enable — as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

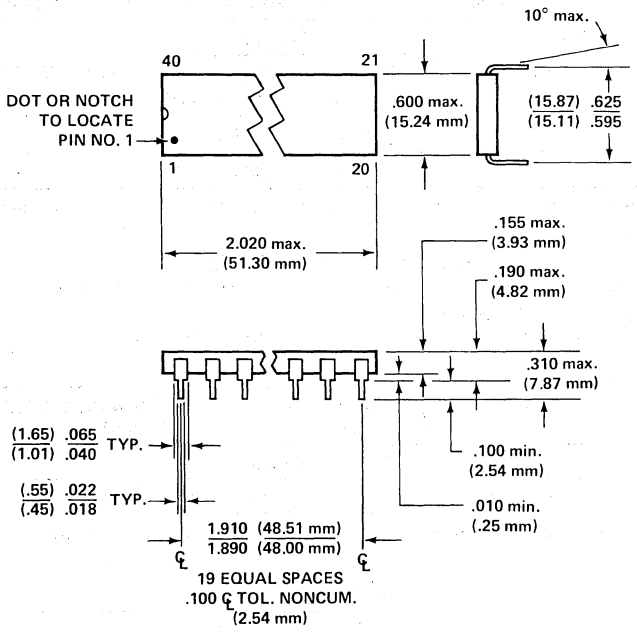
CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 8. Summary of Operation of Control Lines

PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

MICRO-PROCESSORS

Peripheral Interface Adapter (PIA)

Extended Temperature (-40°C to +85°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

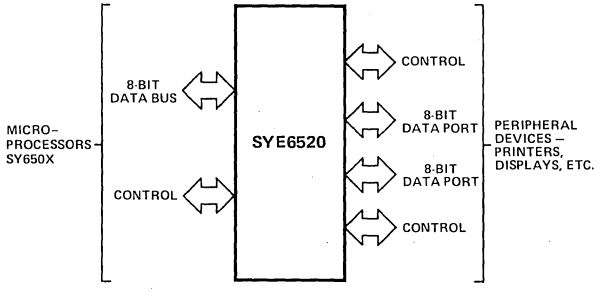
SYE6520/SYE6820
SYE6520A/SYE68B20

MICROPROCESSOR PRODUCTS

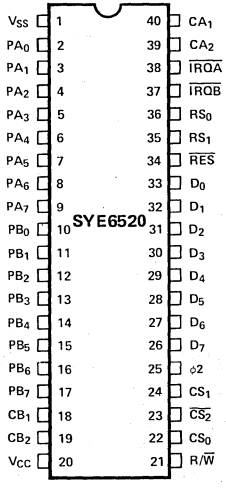
- Direct Replacement for MC6820
- Single +5V Power Supply
- Two 8-bit Bi-directional I/O Ports with Individual Data Direction Control
- CMOS-Compatible Peripheral Port A Lines
- Automatic "Handshake" Control of Data Transfers
- Programmable Interrupt Capability
- Automatic Initialization on Power Up
- 1 and 2 MHz Versions
- Operation over wide temperature range (-40°C to +85°C)

The SYE6520 Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

BASIC SY6520 INTERFACE DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	Clock Frequency
SYEC6520	Ceramic	1 MHz
SYED6520	Cerdip	1 MHz
SYEP6520	Plastic	1 MHz
SYEC6520A	Ceramic	2 MHz
SYED6520A	Cerdip	2 MHz
SYEP6520A	Plastic	2 MHz
SYEC6820	Ceramic	1 MHz
SYED6820	Cerdip	1 MHz
SYEP6820	Plastic	1 MHz
SYEC68B20	Ceramic	2 MHz
SYED68B20	Cerdip	2 MHz
SYEP68B20	Plastic	2 MHz

MICRO PROCESSORS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{in}	-0.3 to +7.0	V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = -40°C to +85°C unless otherwise noted)

Characteristic	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.4	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	0.4	V
Input Leakage Current V_{IN} = 0 to 5.0 V R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	I_{IN}	–	±2.5	μA
Three-State (Off State Input Current) (V_{IN} = 0.4 to 2.4 V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	I_{TSI}	–	±10	μA
Input High Current (V_{IH} = 2.4 V), PA_0-PA_7, CA_2	I_{IH}	–100	–	μA
Input Low Current (V_{IL} = 0.4 V), PA_0-PA_7, CA_2	I_{IL}	–	1.6	mA
Output High Voltage (V_{CC} = min, I_{OH} = -100 μA)	V_{OH}	2.4	–	V
Output Low Voltage (V_{CC} = min, I_{OL} = 1.6mA)	V_{OL}	–	+0.4	V
Output High Current (Sourcing) (V_{OH} = 2.4 V) (V_O = 1.5 V, the current for driving other than TTL, e.g., Darlington Base), PB_0-PB_7, CB_2	I_{OH}	-100 -1.0	– -10	μA mA
Output Low Current (Sinking) (V_{OL} = 0.4 V)	I_{OL}	1.6	–	mA
Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	I_{OFF}	–	10	μA
Power Dissipation V_{CC} = 5.25V	P_D	–	500	mW
Input Capacitance (V_{IN} – 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, CS_2, CA_1, CB_1, ϕ_2	C_{IN}	 – – –	 10 7.0 20	pF
Output Capacitance (V_{IN} – 0, T_A = 25°C, f = 1.0 MHz)	C_{OUT}	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Peripheral Interface Adapter (PIA)

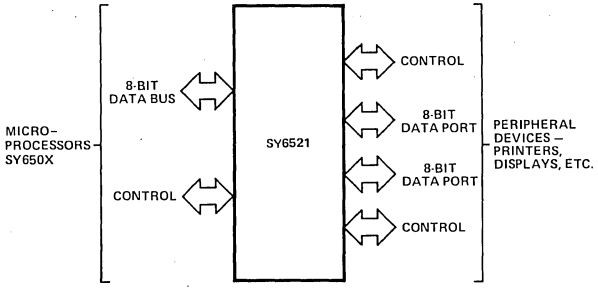
SY6521/SY6821
SY6521A/SY68B21

MICROPROCESSOR PRODUCTS

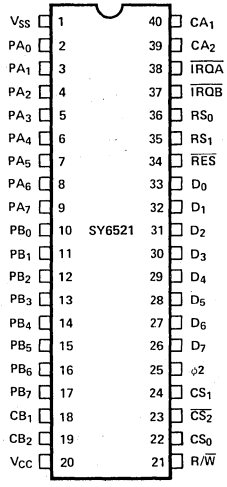
- Extended Performance Version of SY6520
- Single +5V Power Supply
- Two 8-bit Bi-directional I/O Ports with Individual Data Direction Control
- CMOS-Compatible Peripheral Port A lines
- Automatic "Handshake" Control of Data Transfers
- Programmable Interrupt Capability
- Automatic Initialization on Power Up
- 1 and 2 MHz Versions
- Direct Replacement for MC6821

The SY6521 Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. It is functionally compatible with the SY6520, but with more drive capability and improved performance. Control of peripheral devices is accomplished through two 8-bit bi-directional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

BASIC SY6521 INTERFACE DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	Speed
SYC6521	Ceramic	1 MHz
SYD6521	Cerdip	1 MHz
SYP6521	Plastic	1 MHz
SYC6521A	Ceramic	2 MHz
SYD6521A	Cerdip	2 MHz
SYP6521A	Plastic	2 MHz
SYC6821	Ceramic	1 MHz
SYD6821	Cerdip	1 MHz
SYP6821	Pastic	1 MHz
SYC68B21	Ceramic	2 MHz
SYD68B21	Cerdip	2 MHz
SYP68B21	Plastic	2 MHz

MICRO-PROCESSORS

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +7.0	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	+2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	+0.8	V
I_{IN}	Input Leakage Current V_{IN} = 0 to 5.0V R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	 –	 ±2.5	 μA
I_{TSI}	Three-State (Off-State Input Current) (V_{IN} = 0.4 to 2.4V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	–	±10	μA
I_{IH}	Input High Current (V_{IH} = 2.4V), PA_0-PA_7, CA_2	-200	–	μA
I_{IL}	Input Low Current (V_{IL} = 0.4V), PA_0-PA_7, CA_2	–	2.4	mA
V_{OL}	Output Low Voltage (I_L = 3.2 mA), $\overline{IRQA}$, $\overline{IRQB}$	–	0.4	V
V_{OH}	Output High Voltage (I_L =-205 μA), D_0-D_7	2.4	–	V
V_{OL}	Output Low Voltage (I_L = 3.2mA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	–	0.4	V
V_{OH}	Output High Voltage (I_H = -200μA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	2.4	–	V
I_{OH}	Output High Current (Direct Transistor Drive Outputs) (V_{OUT} = 1.5V), PB_0-PB_7, CB_2	-1.0	-10.0	mA
I_{OFF}	Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	–	10	μA
P_D	Power Dissipation (V_{CC} = 5.25V)	–	500	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	 – – –	 10 7.0 20	 pF pF pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

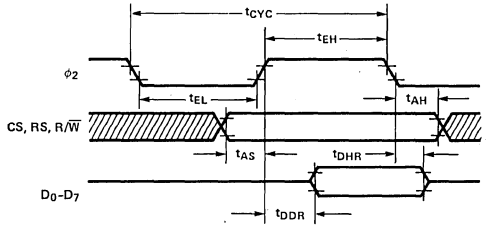


Figure 1. Read Timing Characteristics

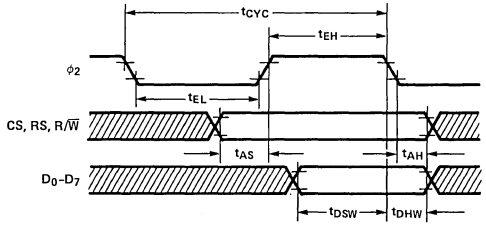


Figure 2. Write Timing Characteristics

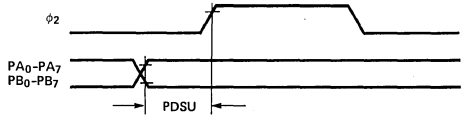


Figure 3. Peripheral Data Setup Time

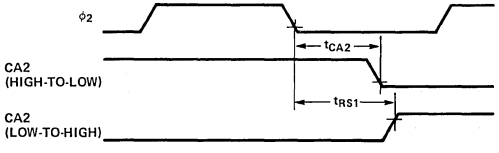


Figure 4. CA_2 Timing

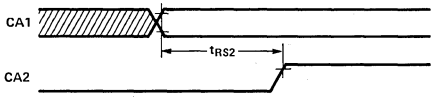


Figure 5. CA_1/CA_2 Timing

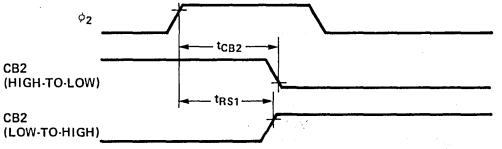


Figure 6. CB_2 Timing

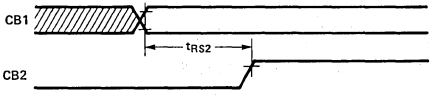


Figure 7. CB_1/CB_2 Handshake Timing

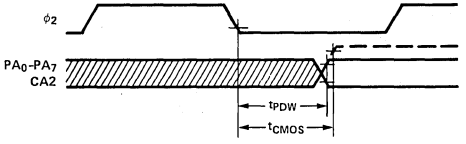


Figure 8. PA Port Delay Time

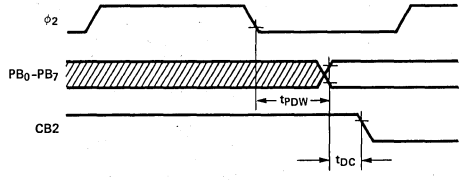


Figure 9. PB Port Delay Time

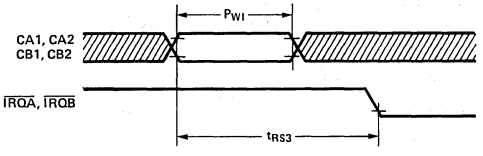


Figure 10. Interrupt Timing

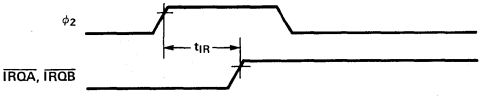


Figure 11. Interrupt Clear Timing

MICRO-PROCESSORS

PROCESSOR INTERFACE TIMING (V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Parameter	SY6521		SY6521A		Unit
		Min.	Max.	Min.	Max.	
t_{CY}	Cycle Time	1000	–	500	–	ns
t_{EH}	ϕ_2 Pulse Width	440	–	200	–	ns
t_{EL}	ϕ_2 Pulse Delay	430	–	210	–	ns
t_{AS}	CS, RS, R/$\overline{W}$ Setup Time	160	–	70	–	ns
t_{AH}	CS, RS, R/$\overline{W}$ Hold Time	10	–	10	–	ns
t_{DDR}	Data Delay Time, Read Cycle	–	320	–	180	ns
t_{DHR}	Data Hold Time, Read Cycle	10	–	10	–	ns
t_{DSW}	Data Setup Time, Write Cycle	195	–	60	–	ns
t_{DHW}	Data Hold Time, Write Cycle	10	–	10	–	ns

PERIPHERAL INTERFACE TIMING (V_{CC} = 5V ± 5%, T_A = 0°C to 70°C unless otherwise noted)

Symbol	Parameter	SY6521		SY6521A		Unit
		Min.	Max.	Min.	Max.	
t_{PDSU}	Peripheral Data Setup Time	200	–	100	–	ns
t_{CA2}	CA_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CA_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CA_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{CB2}	CB_2 Delay Time, High-to-Low	–	1.0	–	0.5	μs
t_{RS1}	CB_2 Delay Time, Low-to-High	–	1.0	–	0.5	μs
t_{RS2}	CB_2 Delay Time, Handshake Mode	–	2.0	–	1.0	μs
t_{PDW}	Peripheral Port Delay Time	–	1.0	–	0.5	μs
t_{CMOS}	Peripheral Port Delay Time (CMOS)	–	2.0	–	1.0	μs
t_{DC}	CB_2 Delay Time from Data Valid	20	–	20	–	ns
P_{WI}	Interrupt Input Pulse Width	500	–	500	–	ns
t_{RS3}	Interrupt Response Time	–	1.0	–	1.0	μs
t_{IR}	Interrupt Clear Delay	–	1.6	–	0.85	μs
t_R, t_F	Rise and Fall Times – CA_1, CA_2, CB_1, CB_2	–	1.0	–	1.0	μs

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

This signal is used to initialize the PIA. A low signal on the $\overline{RES}$ input causes all internal registers to be cleared.

ϕ_2 (Input Clock)

This input is the system ϕ_2 clock and is used to trigger all data transfers between the microprocessor and the PIA.

R/$\overline{W}$ (Read/Write)

This signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ signal permits the processor to read data supplied by the PIA; a low on the R/$\overline{W}$ signal permits the processor to Write into the PIA.

$\overline{IRQA}$, $\overline{IRQB}$ (Interrupt Requests)

$\overline{IRQA}$ and $\overline{IRQB}$ are interrupt lines generated by the PIA for ports A and B respectively. These signals are active low signals and have open-drain outputs, thus allowing multiple IRQ signals from multiple PIA's to be wire-ORed together before connecting to the processor IRQ signal input.

D_0-D_7 (Data Bus)

These eight data bus lines are used to transfer data information between the processor and the PIA. These signals are bi-directional and are normally high-impedance except when selected for a read operation.

CS0, CS1, $\overline{CS2}$ (Chip Selects)

The PIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. These three chip select lines are normally connected to the processor address lines either directly or through external decoder circuits.

RS0, RS1 (Register Selects)

These two signals are used to select the various registers inside the PIA.

INTERNAL ARCHITECTURE

The SY6520 is organized into two independent sections referred to as the "A Side" and the "B Side." Each section consists of a Control Register (CRA, CRB), Data Direction Register (DDRA, DDRB), Output Register (ORA, ORB), Interrupt Status Control and the buffers necessary to drive the Peripheral Interface buses. Figure 12 is a block diagram of the SY6521.

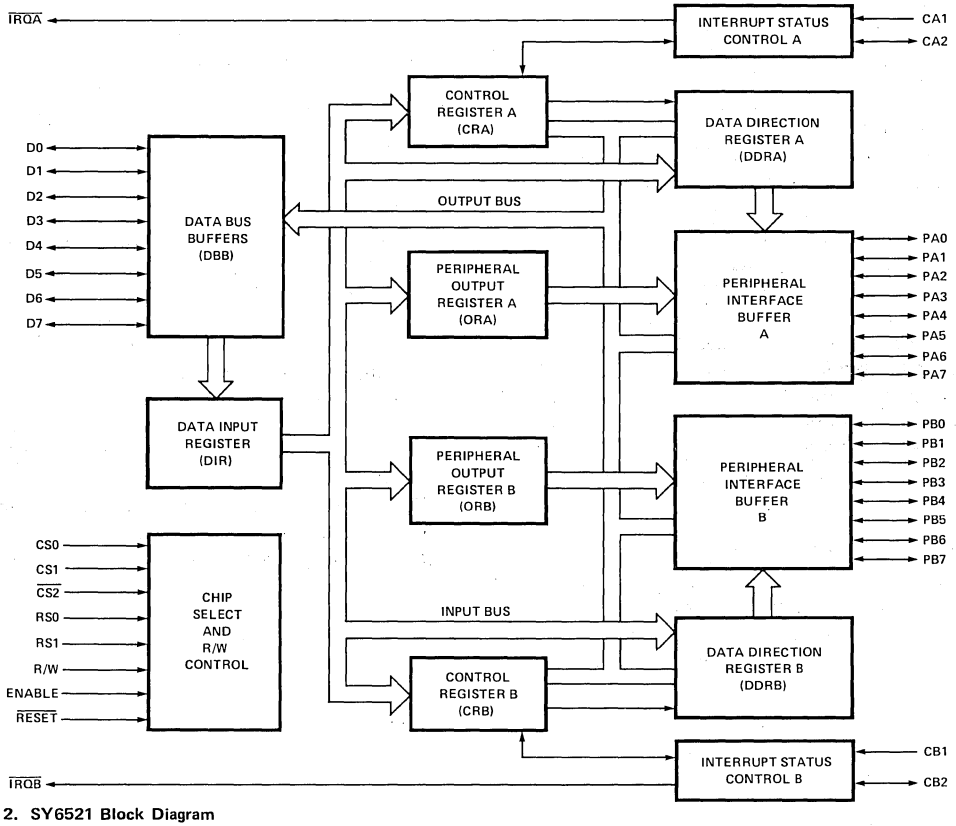


Figure 12. SY6521 Block Diagram

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
	7	6	5	4	3	2	1	0
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Figure 13. Control Registers

Data Input Register

When the microprocessor writes data into the SY6521 the data which appears on the data bus during the Phase Two clock pulse is latched into the Data Input Register. It is then transferred into one of six internal registers of the SY6521 after the trailing edge of Phase Two. This assures that the data on the peripheral output lines will make smooth transitions from high to low or from low to high and the voltage will remain stable except when it is going to the opposite polarity.

Control Registers (CRA and CRB)

Figure 4 illustrates the bit designation and functions in the Control Registers. The Control Registers allow the microprocessor to control the operation of the Interrupt Control inputs (CA1, CA2, CB1, CB2), and Peripheral Control outputs (CA2, CB2). Bit 2 in each register controls the addressing of the Data Direction Registers (DDRA, DDRB) and the Output Registers (ORA, ORB). In addition, two bits (bit 6 and 7) are provided in each control register to indicate the status of the interrupt input lines (CA1, CA2, CB1, CB2). These interrupt status bits (IRQA1, IRQB1) are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These are the interrupt lines which drive the interrupt input ($\overline{IRQ}$, $\overline{NMI}$) of the microprocessor.

Data Direction Registers (DDRA, DDRB)

The Data Direction Registers allow the processor to program each line in the 8-bit Peripheral I/O port to be either an input or an output. Each bit in DDRA controls the corresponding line in the Peripheral A port and each bit in DDRB controls the corresponding line in the Peripheral B port. Placing a "0" in a bit position in the Data Direction Register causes the corresponding Peripheral I/O line to act as an input; a "1" causes it to act as an output.

Peripheral Output Registers (ORA, ORB)

The Peripheral Output Registers store the output data which appears on the Peripheral I/O port. Writing a "0" into a bit in ORA causes the corresponding line on the Peripheral A port to go low ($< 0.4V$) if that line is programmed to act as an output. A "1" causes the corresponding output to go high. The lines of the Peripheral B port are controlled by ORB in the same manner.

Interrupt Status Control

The four interrupt/peripheral control lines (CA1, CA2, CB1, CB2) are controlled by the Interrupt Status Control logic (A, B). This logic interprets the contents of the corresponding Control Register, detects active transitions on the interrupt inputs and performs those operations necessary to assure proper operation of these four peripheral interface lines.

Peripheral Interface Buffers (A, B) and Data Bus Buffers (DBB)

These Buffers provide the necessary current and voltage drive on the peripheral I/O ports and data bus to assure proper system operation and to meet the device specifications.

FUNCTIONAL DESCRIPTION

Bit 2 (DDR) in each Control Register (CRA and CRB) controls the accessing to the Data Direction Register or the Peripheral interface. If bit 2 is a "1", a Peripheral Output register (ORA, ORB) is selected, and if bit 2 is a "0", a Data Direction Register (DDRA, DDRB) is selected. The Data Direction Register Access Control bit, together with the Register Select lines (RS0, RS1) selects the various internal registers as shown in Figure 14.

In order to write data into DDRA, ORA, DDRB, or ORB registers, bit 2 in the proper Control Register must first be set. The desired register may then be accessed with the address determined by the address interconnect technique used.

Register Select Lines (RS0), (RS1)

These two register select lines are used to select the various registers inside the SY6521. These input lines are used in conjunction with internal control registers to select a particular register that is to be accessed by the microprocessor. These lines are normally connected to microprocessor address output lines. These lines operate in conjunction with the chip-select inputs to allow the microprocessor to address a single 8-bit register within the microprocessor address space. This register may be an internal register (CRA, ORA, etc.) or it may be a Peripheral I/O port.

The processor may write directly into the Control Registers (CRA, CRB), the Data Direction Registers (DDRA, DDRB) and the Peripheral Output Registers (ORA, ORB). In addition, the processor may directly read the contents of the Control Registers and the Data Direction Registers. Accessing the Peripheral Output Register for the purpose of reading data back into the processor operates differently on the ORA and the ORB registers and therefore are discussed separately below.

Reading the Peripheral A I/O Port

The Peripheral A I/O port consists of 8 lines which can be programmed to act as inputs or outputs. When programmed to act as outputs, each line reflects the contents of the corresponding bit in the Peripheral Output Register. When programmed to act as inputs, these lines will go high or low depending on the input data. The Peripheral Output Register (ORA) has no effect on those lines programmed to act as inputs. The eight lines of the Peripheral A I/O port therefore contain either input or output data depending on whether the line is programmed to act as an input or an output.

Performing a Read operation with RS1 = 0, RS0 = 0 and the Data Direction Register Access Control bit (CRA-2) = 1, directly transfers the data on the Peripheral A I/O lines into the processor (via the data bus). This will contain both the input and output data. The processor must be programmed to recognize and interpret only those bits which are important to the particular peripheral operation being performed.

Since the processor always reads the Peripheral A I/O port pins instead of the actual Peripheral Output Register (ORA), it is possible for the data read into the processor to differ from the contents of the Peripheral Output Register for an output line. This is true when the I/O pin is not allowed to go to a full +2.4V DC when the Peripheral Output register contains a logic 1. In this case, the processor will read a 0 from the Peripheral A pin, even though the corresponding bit in the Peripheral Output register is a 1.

Reading the Peripheral B I/O Port

Reading the Peripheral B I/O port yields a combination of input and output data in a manner similar to the Peripheral A port. However, data is read directly from the Peripheral B Output Register (ORB) for

Register Select Pin		Data Direction Register Access Control Bit		
RS1	RS0	CRA-2	CRB-2	Register Selected
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 14. Register Addressing

those lines programmed to act as outputs. It is therefore possible to load down the Peripheral B Output lines without causing incorrect data to be transferred back into the processor on a Read operation.

Interrupt Request Lines ($\overline{IRQA}$, $\overline{IRQB}$)

The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the microprocessor either directly or through external interrupt priority circuitry. These lines are "open drain" and are capable of sinking 1.6 milliamps from an external source. This permits all interrupt request lines to be tied together in a "wired-OR" configuration. The "A" and "B" in the titles of these lines correspond to the "A" peripheral port and the "B" peripheral port. Hence each interrupt request line services one peripheral data port.

Each Interrupt Request line has two interrupt flag bits which can cause the Interrupt Request line to go low. These flags are bits 6 and 7 in the two Control Registers. These flags act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the processor to enable or disable the interrupt from each of the four interrupt inputs (CA1, CA2, CB1, CB2).

The four interrupt flags are set by active transitions of the signal on the interrupt input (CA1, CA2, CB1, CB2).

Control of $\overline{IRQA}$

Control Register A bit 7 is always set by an active transition of the CA1 interrupt input signal. Interrupting from this flag can be disabled by setting bit 0 in the Control Register A (CRA) to a logic 0. Likewise, Control Register A bit 6 can be set by an active transition of the CA2 interrupt input signal. Interrupting from this flag can be disabled by setting bit 3 in the Control Register to a logic 0.

Both bit 6 and bit 7 in CRA are reset by a "Read Peripheral Output Register A" operation. This is defined as an operation in which the proper chip-select and register-select signals are provided to allow the processor to read the Peripheral A I/O port.

Control of $\overline{IRQB}$

Control of $\overline{IRQB}$ is performed in exactly the same manner as that described above for $\overline{IRQA}$. Bit 7 in CRB is set by an active transition on CB1; interrupting from this flag is controlled by CRB bit 0. Likewise, bit 6 in CRB is set by an active transition on CB2; interrupting from this flag is controlled by CRB bit 3.

Also, both bit 6 and bit 7 are reset by a "Read Peripheral B Output Register" operation.

SUMMARY:
$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

It should be stressed at this point that the flags act as the link between the peripheral interrupt signals and the processor interrupt inputs. The interrupt disable bits allow the processor to control the interrupt function.

Interface Between SY6521 and Peripheral Devices

The SY6521 provides two 8-bit bi-directional ports and 4 interrupt/control lines for interfacing to peripheral devices. These ports and the associated interrupt/control lines are referred to as the "A" side and the "B" side. Each side has its own unique characteristics and will therefore be discussed separately below.

Peripheral I/O Ports

The Peripheral A and Peripheral B I/O ports allow the microprocessor to interface to the input lines on the peripheral device by loading data into the Peripheral Output Register. They also allow the processor to interface with the peripheral device output lines by reading the data on the Peripheral Port input lines directly onto the data bus and into the internal registers of the processor.

Peripheral A I/O Port (PA0-PA7)

Each of the Peripheral I/O lines can be programmed to act as an input or an output. This is accomplished by setting a "1" in the corresponding bit in the Data Direction Register for those lines which are to act as outputs. A "0" in a bit of the Data Direction Register causes the corresponding Peripheral I/O lines to act as an input.

The buffers which drive the Peripheral A I/O lines contain "passive" pull-ups as shown in Figure 15. These pull-up devices are resistive in nature and therefore allow the output voltage to go to V_{CC} for a logic 1. The switches can sink a full 1.6mA, making these buffers capable of driving one standard TTL load.

In the input mode, the pull-up devices shown in Figure 15 are still connected to the I/O pin and still supply current to this pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral B I/O Port (PB0-PB7)

The Peripheral B I/O port duplicates many of the functions of the Peripheral A port. The process of programming these lines to act as an input or an out-

put has been discussed previously. Likewise, the effect of reading or writing this port has been discussed. However, there are several characteristics of the buffers driving these lines which affect their use in peripheral interfacing.

The Peripheral B I/O port buffers are push-pull devices as shown in Figure 16. The pull-up devices are switched "OFF" in the "0" state and "ON" for a logic 1. Since these pull-ups are active devices, the logic "1" voltage is not guaranteed to go higher than +2.4V. They are TTL compatible but are not CMOS compatible.

However, the active pull-up devices can source up to 1mA at 1.5V. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows very simple control of relays, lamps, etc.

Because these outputs are designed to drive transistors directly, the output data is read directly from the Peripheral Output Register for those lines programmed to act as inputs.

The final characteristic which is a function of the Peripheral B push-pull buffers is the high-impedance input state. When the Peripheral B I/O lines are programmed to act as inputs, the output buffer enters the high impedance state.

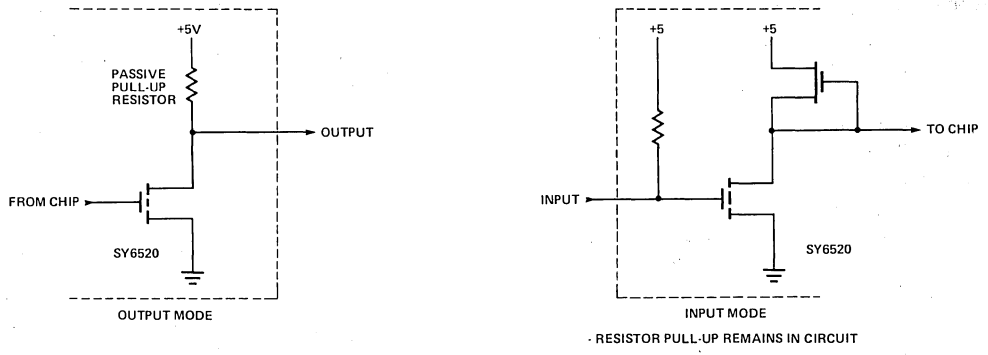


Figure 15. Port A Buffer Circuit (PA_0-PA_7)

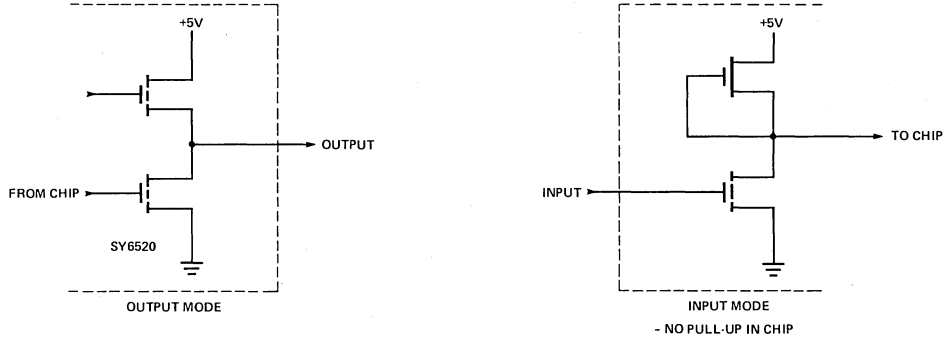


Figure 16. Port B Buffer Circuit (PB_0-PB_7)

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1, CB2)

The four interrupt input/peripheral control lines provide a number of special peripheral control functions. These lines greatly enhance the power of the two general purpose interface ports (PA0-PA7, PB0-PB7). Figure 17 summarizes the operation of these control lines.

Peripheral A Interrupt Input/Peripheral Control Lines (CA1, CA2)

CA1 is an interrupt input only. An active transition of the signal on this input will set bit 7 of the Control Register A to a logic 1. The active transition can be programmed by setting a "0" in bit 1 of the CRA if the interrupt flag (bit 7 of CRA) is to be set on a negative transition of the CA1 signal or a "1" if it is to be set on a positive transition.

NOTE: A negative transition is defined as a transition from a high to a low, and a positive transition is defined as a transition from a low to a high voltage.

Setting the interrupt flag will interrupt the processor through $\overline{IRQA}$ if bit 0 of CRA is a 1 as described previously.

CA2 can act as a totally independent interrupt input or as a peripheral control output. As an input (CRA, bit 5 = 0) it acts to set the interrupt flag, bit 6 of CRA, to a logic 1 on the active transition selected by bit 4 of CRA.

These control register bits and interrupt inputs serve the same basic function as that described above for CA1. The input signal sets the interrupt flag which serves as the link between the peripheral device and the processor interrupt structure. The interrupt disable bit allows the processor to exercise control over the system interrupts.

In the Output mode (CRA, bit 5 = 1), CA2 can operate independently to generate a simple pulse each time the microprocessor reads the data on the Peripheral A I/O port. This mode is selected by setting CRA, bit 4 to a "0" and CRA, bit 3 to a "1". This pulse output can be used to control the counters, shift registers, etc. which make sequential data available on the Peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the processor and the peripheral device. On the A side, this technique allows positive control of data transfers from the peripheral device into the microprocessor. The CA1 input signals the processor that data is available by interrupting the processor. The processor reads the data and sets CA2 low. This signals the peripheral device that it can make new data available.

The final output mode can be selected by setting bit 4 of CRA to a 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of CRA to a 1 or a 0 respectively.

Peripheral B Interrupt Input/Peripheral Control Lines (CB1, CB2)

CB1 operates as an interrupt input only in the same manner as CA1. Bit 7 of CRB is set by the active transition selected by bit 0 of CRB. Likewise, the CB2 input mode operates exactly the same as the CA2 input modes. The CB2 output modes, CRB bit 5 = 1, differ somewhat from those of CA2. The pulse output occurs when the processor writes data into the Peripheral B Output Register. Also, the "handshaking" operates on data transfers from the processor into the peripheral device.

CA1/CB1 CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	Negative	Disable — remain high
0	1	Negative	Enable — goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable — remain high
1	1	Positive	Enable — as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	0	Negative	Disable — remains high
0	0	1	Negative	Enable — goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable — remains high
0	1	1	Positive	Enable — as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

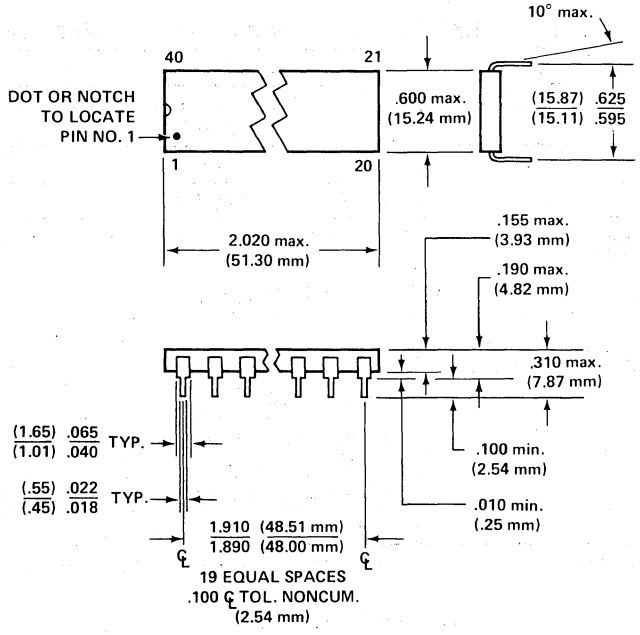
CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 17. Summary of Operation of Control Lines

PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

Peripheral Interface Adapter (PIA)

Extended Temperature (-40°C to +85°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYE6521/SYE6821
SYE6521A/SYE68B21

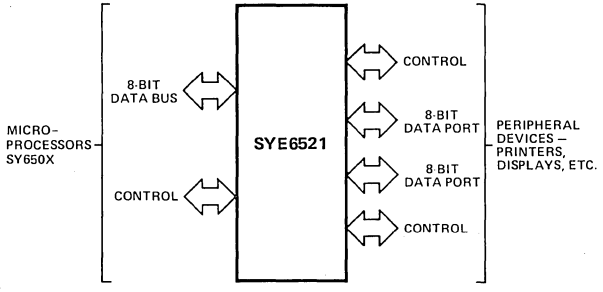
MICROPROCESSOR PRODUCTS

- Extended Performance Version of SY6520
- Single +5V Power Supply
- Two 8-bit Bi-directional I/O Ports with Individual Data Direction Control
- CMOS-Compatible Peripheral Port A lines
- Automatic "Handshake" Control of Data Transfers
- Programmable Interrupt Capability
- Automatic Initialization on Power Up
- 1 and 2 MHz Versions
- Direct Replacement for MC6821
- Operation over wide temperature range (-40°C to +85°C)

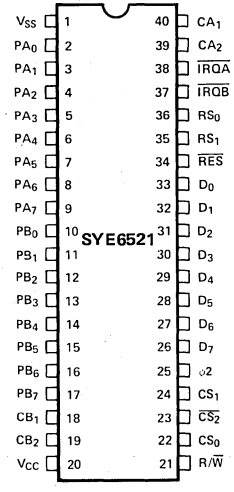
The SYE6521 Peripheral Interface Adapter (PIA) is designed to provide a broad range of peripheral control to microcomputer systems. It is functionally compatible with the SYE6520, but with more drive capability and improved performance. Control of peripheral devices is accomplished through two 8-bit bidirectional I/O ports. Each I/O line may be programmed to be either an input or an output. In addition, four peripheral control lines are provided to perform "handshaking" during data transfers.

MICRO-PROCESSORS

BASIC SY6521 INTERFACE DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	Clock Frequency
SYEC6521	Ceramic	1 MHz
SYED6521	Cerdip	1 MHz
SYEP6521	Plastic	1 MHz
SYEC6521A	Ceramic	2 MHz
SYED6521A	Cerdip	2 MHz
SYEP6521A	Plastic	2 MHz
SYEC6821	Ceramic	1 MHz
SYED6821	Cerdip	1 MHz
SYEP6821	Plastic	1 MHz
SYEC68B21	Ceramic	2 MHz
SYED68B21	Cerdip	2 MHz
SYEP68B21	Plastic	2 MHz

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = -40°C to +85°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	+2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	+0.8	V
I_{IN}	Input Leakage Current V_{IN} = 0 to 5.0V R/$\overline{W}$, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	 –	 ±2.5	 μA
I_{TSI}	Three-State (Off-State Input Current) (V_{IN} = 0.4 to 2.4V, V_{CC} = max), D_0-D_7, PB_0-PB_7, CB_2	–	±10	μA
I_{IH}	Input High Current (V_{IH} = 2.4V), PA_0-PA_7, CA_2	-200	–	μA
I_{IL}	Input Low Current (V_{IL} = 0.4V), PA_0-PA_7, CA_2	–	2.4	mA
V_{OL}	Output Low Voltage (I_L = 3.2 mA), $\overline{IRQA}$, $\overline{IRQB}$	–	0.4	V
V_{OH}	Output High Voltage (I_L - 205 μA), D_0-D_7	2.4	–	V
V_{OL}	Output Low Voltage (I_L = 3.2mA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	–	0.4	V
V_{OH}	Output High Voltage (I_H = -200μA), PA_0-PA_7, PB_0-PB_7, CA_2, CB_2	2.4	–	V
I_{OH}	Output High Current (Direct Transistor Drive Outputs) (V_{OUT} = 1.5V), PB_0-PB_7, CB_2	-1.0	-10.0	mA
I_{OFF}	Output Leakage Current (Off-State), $\overline{IRQA}$, $\overline{IRQB}$	–	10	μA
P_D	Power Dissipation (V_{CC} = 5.25V)	–	500	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz) D_0-D_7, PA_0-PA_7, PB_0-PB_7, CA_2, CB_2 R/W, $\overline{Reset}$, RS_0, RS_1, CS_0, CS_1, $\overline{CS_2}$, CA_1, CB_1, ϕ_2	 – – –	 10 7.0 20	 pF pF pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	–	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

Versatile Interface Adapter (VIA)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SY6522
SY6522A

MICROPROCESSOR PRODUCTS

- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Port A lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz and 2 MHz Operation

The SY6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

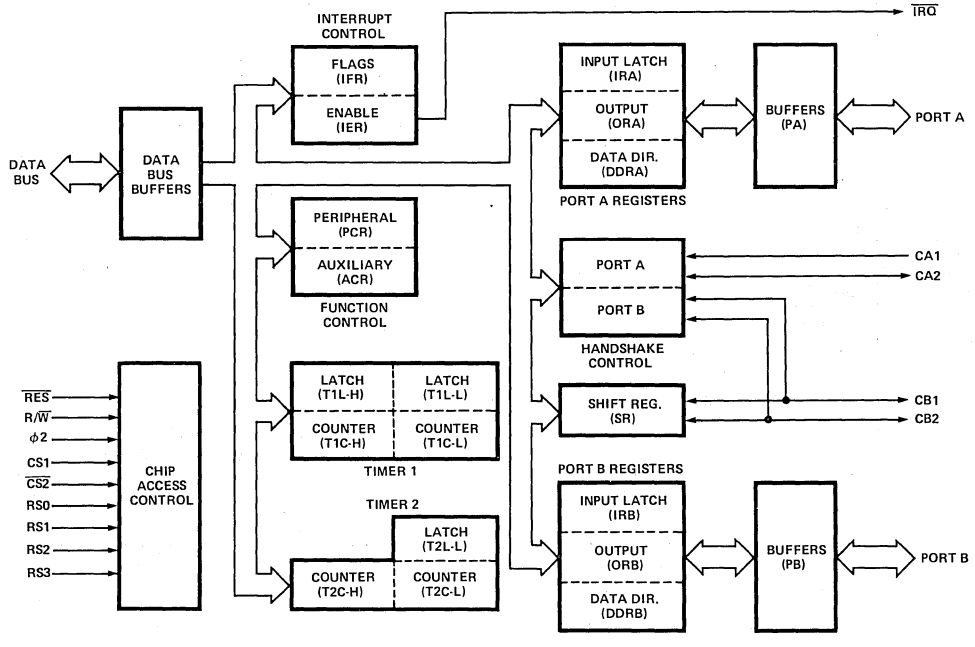


Figure 1. SY6522 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage Current — V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\Phi 2$	—	±2.5	μA
I_{TSI}	Off-state Input Current — V_{IN} = .4 to 2.4V V_{CC} = Max, D0 to D7	—	±10	μA
I_{IH}	Input High Current — V_{IH} = 2.4V PA0-PA7, CA2, PB0-PB7, CB1, CB2	-100	—	μA
I_{IL}	Input Low Current — V_{IL} = 0.4 Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	—	-1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = -100 μAdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	—	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	—	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0-PB7)	 -100 -1.0	 — —	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	—	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	—	10	μA
C_{IN}	Input Capacitance — T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\Phi 2$ Input)	 — — —	 7.0 10 20	 pF pF pF
C_{OUT}	Output Capacitance — T_A = 25°C, f = 1 MHz	—	10	pF
P_D	Power Dissipation (V_{CC} = 5.25V)	—	700	mW

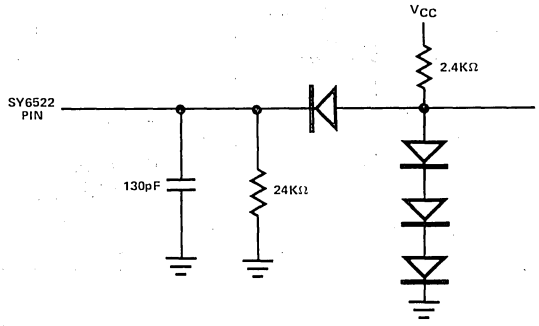


Figure 2. Test Load (for all Dynamic Parameters)

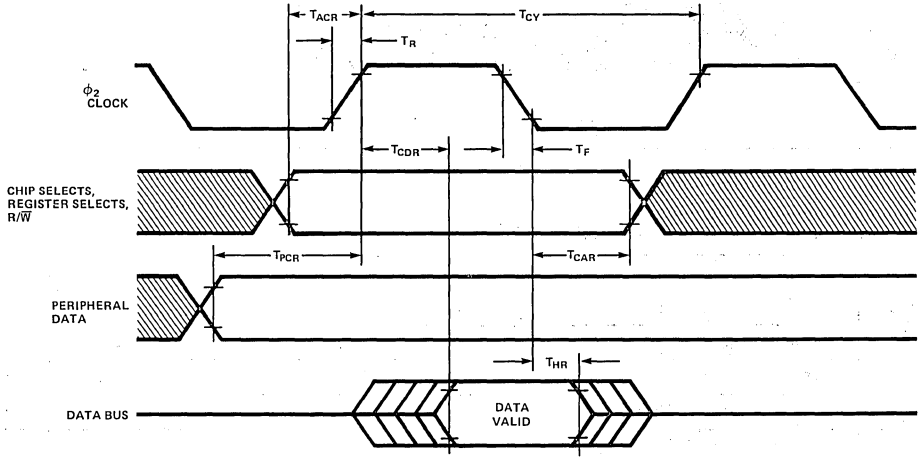


Figure 3. Read Timing Characteristics

READ TIMING CHARACTERISTICS (FIGURE 3)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

NOTE: tr, tf = 10 to 30ns.

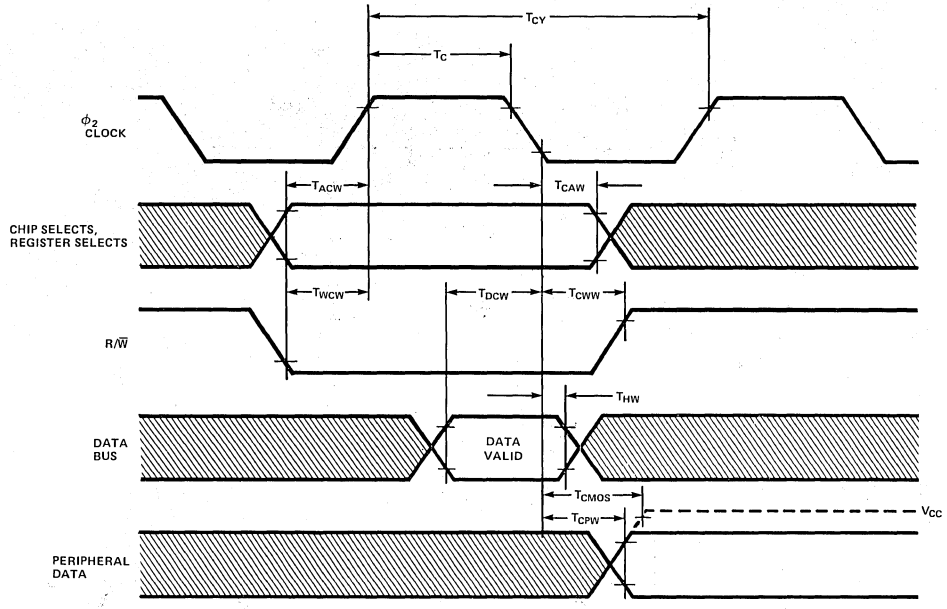


Figure 4. Write Timing Characteristics

WRITE TIMING CHARACTERISTICS (FIGURE 4)

Symbol	Parameter	SY6522		SY6522A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	ϕ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	300	–	200	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

NOTE: tr, tf = 10 to 30ns.

PERIPHERAL INTERFACE CHARACTERISTICS

Symbol	Characteristic	Min.	Max.	Unit	Figure
t_r, t_f	Rise and Fall Time for CA1, CB1, CA2, and CB2 Input Signals	–	1.0	μs	–
T_{CA2}	Delay Time, Clock Negative Transition to CA2 Negative Transition (read handshake or pulse mode)	–	1.0	μs	5a, 5b
T_{RS1}	Delay Time, Clock Negative Transition to CA2 Positive Transition (pulse mode)	–	1.0	μs	5a
T_{RS2}	Delay Time, CA1 Active Transition to CA2 Positive Transition (handshake mode)	–	2.0	μs	5b
T_{WHS}	Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (write handshake)	0.05	1.0	μs	5c, 5d
T_{DS}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	0.20	1.5	μs	5c, 5d
T_{RS3}	Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (pulse mode)	–	1.0	μs	5c
T_{RS4}	Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (handshake mode)	–	2.0	μs	5d
T_{21}	Delay Time Required from CA2 Output to CA1 Active Transition (handshake mode)	400	–	ns	5d
T_{IL}	Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (input latching)	300	–	ns	5e
T_{SR1}	Shift-Out Delay Time – Time from ϕ_2 Falling Edge to CB2 Data Out	–	300	ns	5f
T_{SR2}	Shift-In Setup Time – Time from CB2 Data In to ϕ_2 Rising Edge	300	–	ns	5g
T_{SR3}	External Shift Clock (CB1) Setup Time Relative To ϕ_2 Trailing Edge	100	T_{CY}	ns	5g
T_{IPW}	Pulse Width – PB6 Input Pulse	$2 \times T_{CY}$	–		5i
T_{ICW}	Pulse Width – CB1 Input Clock	$2 \times T_{CY}$	–		5h
T_{IPS}	Pulse Spacing – PB6 Input Pulse	$2 \times T_{CY}$	–		5i
T_{ICS}	Pulse Spacing – CB1 Input Pulse	$2 \times T_{CY}$	–		5h
T_{AL}	CA1, CB1 Set Up Prior to Transition to Arm Latch	300	–	ns	5e
T_{PDH}	Peripheral Data Hold After CA1, CB1 Transition	150	–	ns	5e

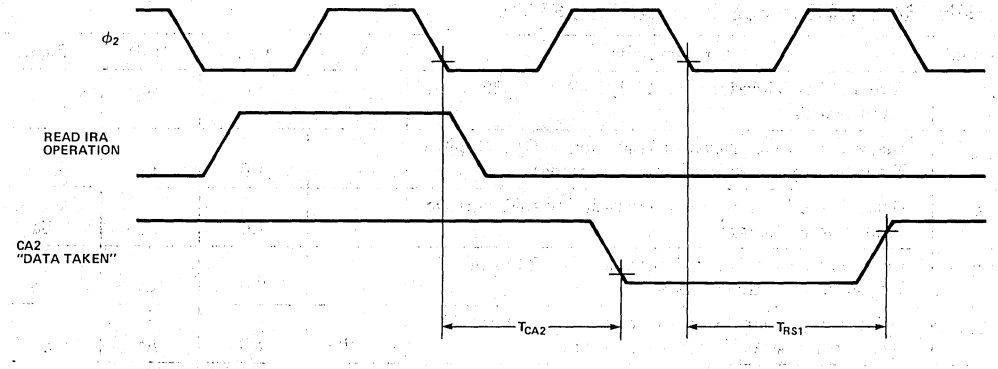


Figure 5a. CA2 Timing for Read Handshake, Pulse Mode

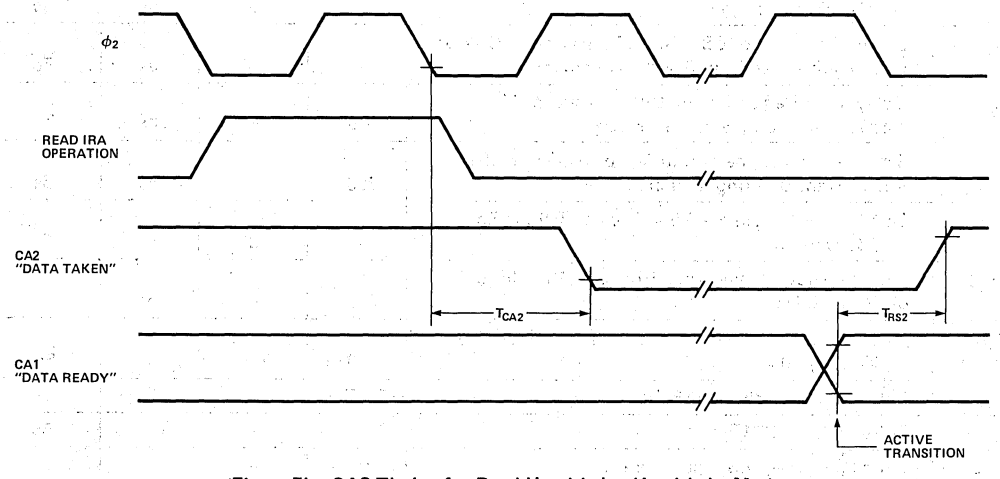


Figure 5b. CA2 Timing for Read Handshake, Handshake Mode

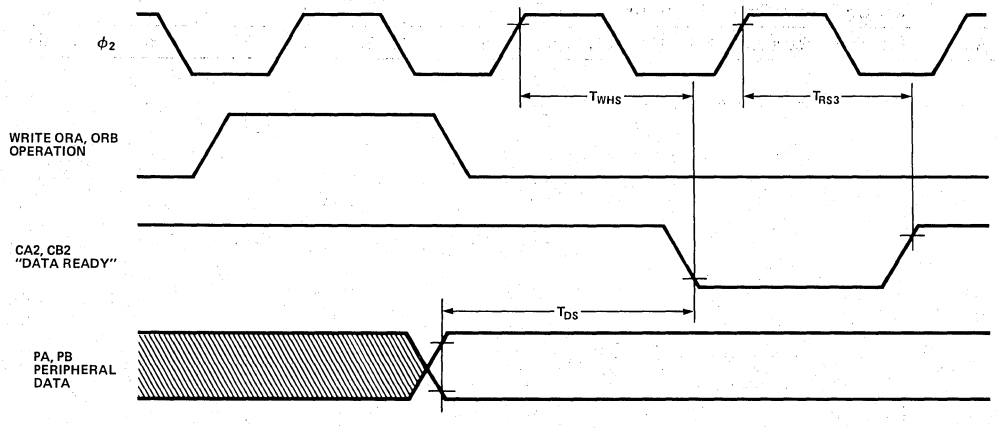


Figure 5c. CA2, CB2 Timing for Write Handshake, Pulse Mode

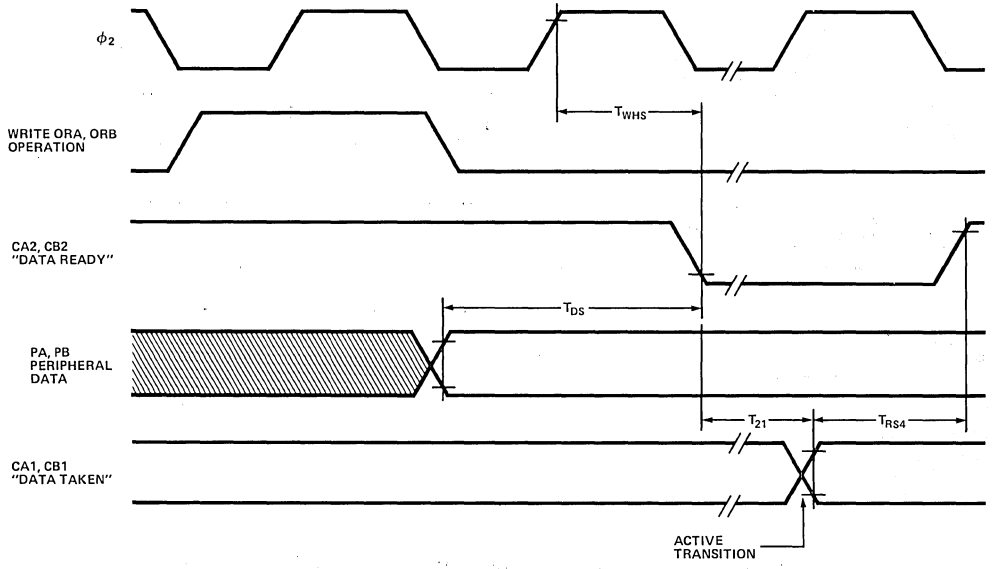


Figure 5d. CA2, CB2 Timing for Write Handshake, Handshake Mode

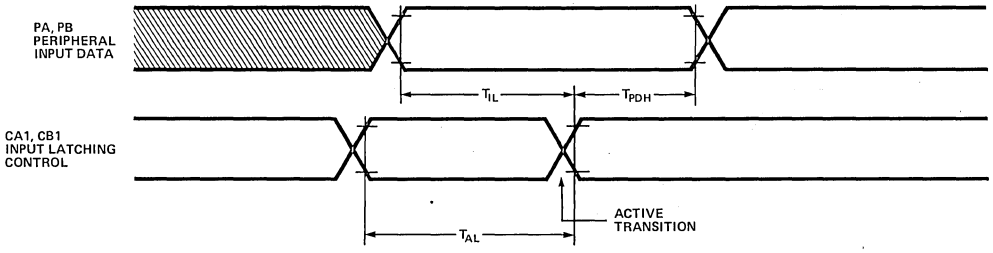


Figure 5e. Peripheral Data Input Latching Timing

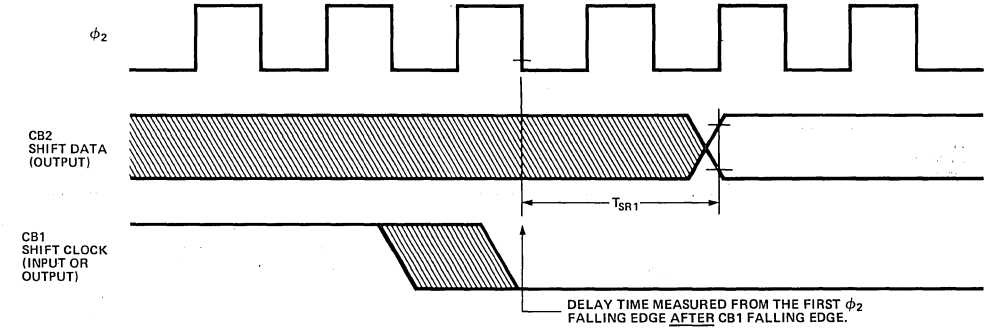


Figure 5f. Timing for Shift Out with Internal or External Shift Clocking

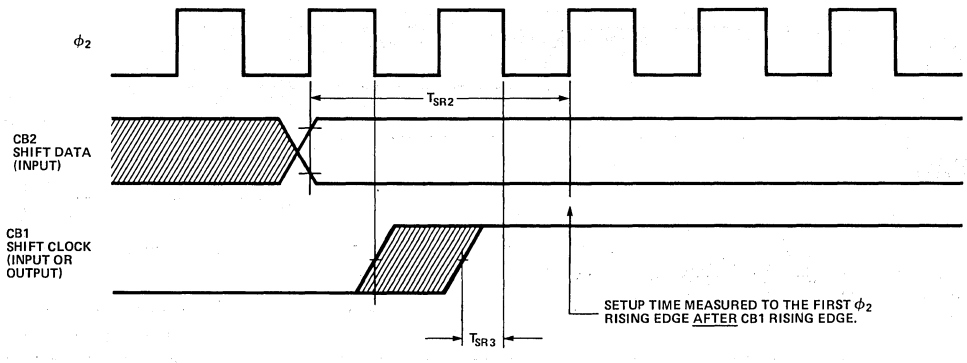


Figure 5g. Timing for Shift In with Internal or External Shift Clocking

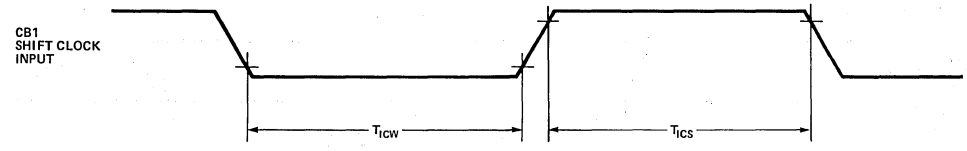


Figure 5h. External Shift Clock Timing

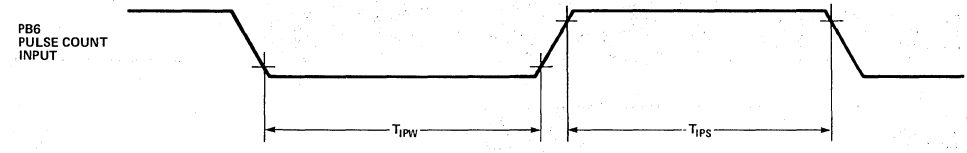


Figure 5i. Pulse Count Input Timing

PIN DESCRIPTIONS

$\overline{RES}$ (Reset)

The reset input clears all internal registers to logic 0 (except T1 and T2 latches and counters and the Shift Register). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system processor and the SY6522.

R/$\overline{W}$ (Read/Write)

The direction of the data transfers between the SY6522 and the system processor is controlled by the R/$\overline{W}$ line. If R/$\overline{W}$ is low, data will be transferred out of the processor into the selected SY6522 register (write operation). If R/$\overline{W}$ is high and the chip is selected, data will be transferred out of the SY6522 (read operation).

DB0–DB7 (Data Bus)

The eight bi-directional data bus lines are used to transfer data between the SY6522 and the system processor, During read cycles, the contents of the selected SY6522 register are placed on the data bus lines and transferred into the processor. During write cycles, these lines are high-impedance inputs and data is transferred from the processor into the selected register. When the SY6522 is unselected, the data bus lines are high-impedance.

CS1, $\overline{CS2}$ (Chip Selects)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected SY6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

RS0–RS3 (Register Selects)

The four Register Select inputs permit the system processor to select one of the 16 internal registers of the SY6522, as shown in Figure 6.

Register Number	RS Coding				Register Desig.	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same as Reg 1 Except No "Handshake"	

Figure 6. SY6522 Internal Register Summary

IRQ (Interrupt Request)

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PA0-PA7 (Peripheral A Port)

The Peripheral A port consists of 8 lines which can be individually programmed to act as inputs or outputs under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data may be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Figure 7 illustrates the output circuit.

CA1, CA2 (Peripheral A Control Lines)

The two Peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A port input lines. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

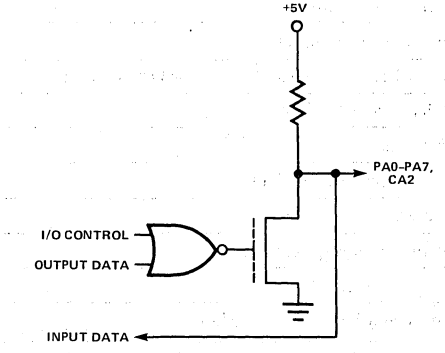


Figure 7. Peripheral A Port Output Circuit

PB0-PB7 (Peripheral B Port)

The Peripheral B port consists of eight bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. Peripheral B lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 1.0mA at 1.5VDC in the output mode to allow the outputs to directly drive Darlington transistor circuits. Figure 8 is the circuit schematic.

CB1, CB2 (Peripheral B Control Lines)

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. Unlike PB0-PB7, CB1 and CB2 cannot drive Darlington transistor circuits.

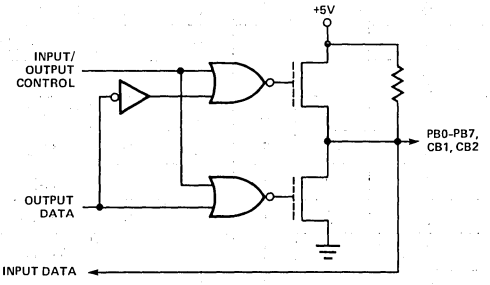


Figure 8. Peripheral B Port Output Circuit

FUNCTIONAL DESCRIPTION

Port A and Port B Operation

Each 8-bit peripheral port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

When programmed as an output each peripheral pin is also controlled by a corresponding bit in the Output Register (ORA, ORB). A 1 in the Output Register causes the output to go high, and a "0" causes the output to go low. Data may be written into Output Register bits corresponding to pins which are pro-

grammed as inputs. In this case, however, the output signal is unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferred onto the Data Bus. With input latching disabled, IRA will always reflect the levels on the PA pins. With input latching enabled and the selected active transition on CA1 having occurred, IRA will contain the data present on the PA lines at the time of the transition. Once IRA is read, however, it will appear transparent, reflecting the current state of the PA lines until the next "latching" transition.

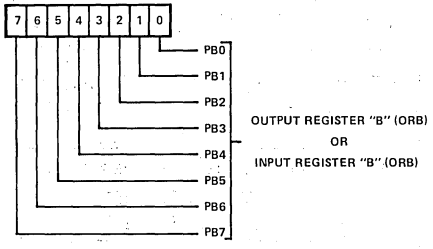
The IRB register operates similar to the IRA register. However, for pins programmed as outputs there is a difference. When reading IRA, the level on the pin determines whether a 0 or a 1 is sensed. When reading IRB, however, the bit stored in the output register, ORB, is the bit sensed. Thus, for outputs which have large loading effects and which pull an output "1" down or which pull an output "0" up, reading IRA may result in reading a "0" when a "1" was actually programmed, and reading a "1" when a "0" was programmed. Reading IRB, on the other hand, will read the "1" or "0" level actually programmed, no matter what the loading on the pin.

Figures 9, 10, and 11 illustrate the formats of the port registers. In addition, the input latching modes are selected by the Auxiliary Control Register (Figure 16.)

Handshake Control of Data Transfers

The SY6522 allows positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

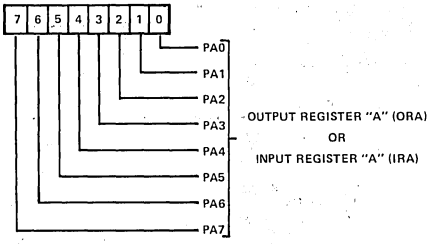
REG 0 – ORB/IRB



Pin Data Direction Selection	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no affect.
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 9. Output Register B (ORB), Input Register B (IRB)

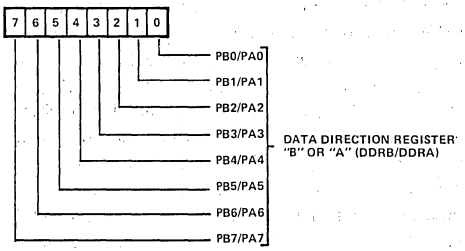
REG 1 – ORA/IRA



Pin Data Direction Selection	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA).	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 10. Output Register A (ORA), Input Register A (IRA)

REG 2 (DDRB) AND REG 3 (DDRA)



"0" ASSOCIATED PB/PA PIN IS AN INPUT (HIGH-IMPEDANCE)

"1" ASSOCIATED PB/PA PIN IS AN OUTPUT, WHOSE LEVEL IS DETERMINED BY ORB/ORA REGISTER BIT.

Figure 11. Data Direction Registers (DDRB, DDRA)

Read Handshake

Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using Read Handshaking. In this case, the peripheral device must generate the equivalent of a "Data Ready" signal to the processor signifying that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

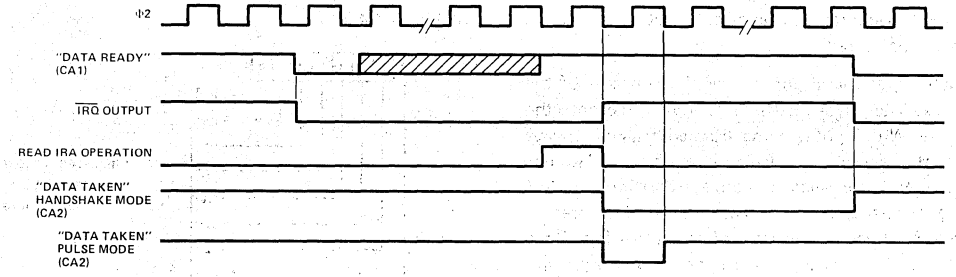


Figure 12. Read Handshake Timing (Port A, Only)

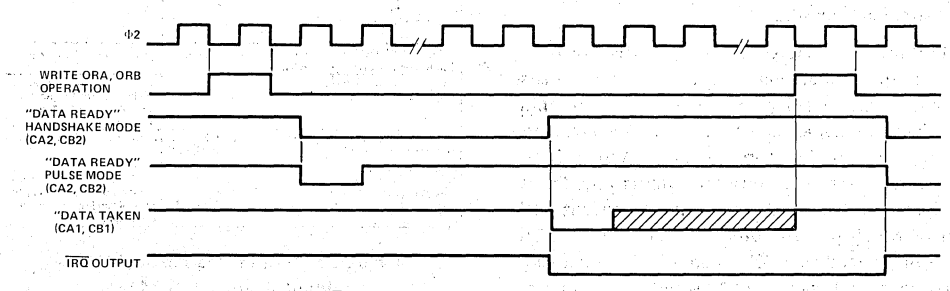


Figure 13. Write Handshake Timing

In the SY6522, automatic "Read" Handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The "Data Ready" signal will set an internal flag which may interrupt the processor or which may be polled under program control. The "Data Taken" signal can either be a pulse or a level which is set low by the system processor and is cleared by the "Data Ready" signal. These options are shown in Figure 12 which illustrates the normal Read Handshaking sequence.

Write Handshake

The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described for Read Handshaking. However, for Write Handshaking, the SY6522 generates the "Data Ready" signal and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the SY6522. CA2 or CB2 act as a "Data Ready" output in either the handshake mode or pulse mode and CA1 or CB1 accept the "Data Taken" signal from the peripheral device, setting the interrupt flag and cleaning the "Data Ready" output. This sequence is shown in Figure 13.

Selection of operating modes for CA1, CA2, CB1, and CB2 is accomplished by the Peripheral Control Register (Figure 14).

Timer Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at $\phi 2$ clock rate. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low if the interrupt is enabled. The timer will then disable any further interrupts, or (when programmed to) will automatically transfer the contents of the latches into the counter and begin to decrement again. In addition, the timer may be programmed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is discussed separately below.

The T1 counter is depicted in Figure 15 and the latches in Figure 16.

REG 12 – PERIPHERAL CONTROL REGISTER

7	6	5	4	3	2	1	0

CB2 CONTROL

7	6	5	OPERATION
0	0	0	INPUT-NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT-NEG EDGE *
0	1	0	INPUT-POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

CB1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA1 INTERRUPT CONTROL

0 = NEGATIVE ACTIVE EDGE
1 = POSITIVE ACTIVE EDGE

CA2 CONTROL

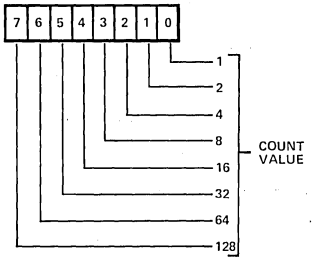
3	2	1	OPERATION
0	0	0	INPUT-NEGATIVE ACTIVE EDGE
0	0	1	INDEPENDENT INTERRUPT INPUT-NEG EDGE *
0	1	0	INPUT-POSITIVE ACTIVE EDGE
0	1	1	INDEPENDENT INTERRUPT INPUT-POS EDGE *
1	0	0	HANDSHAKE OUTPUT
1	0	1	PULSE OUTPUT
1	1	0	LOW OUTPUT
1	1	1	HIGH OUTPUT

*SEE NOTE ACCOMPANYING FIGURE 25.

Figure 14. CA1, CA2, CB1, CB2 Control

Two bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of the T1 operating modes. The four possible modes are depicted in Figure 17.

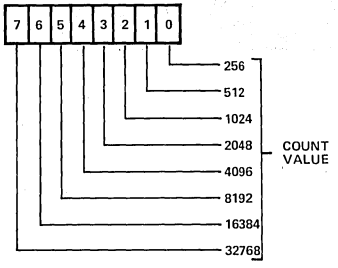
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. LATCH CONTENTS ARE TRANSFERRED INTO LOW-ORDER COUNTER AT THE TIME THE HIGH-ORDER COUNTER IS LOADED (REG 5).

READ – 8 BITS FROM T1 LOW-ORDER COUNTER TRANSFERRED TO MPU. IN ADDITION, T1 INTERRUPT FLAG IS RESET (BIT 6 IN INTERRUPT FLAG REGISTER).

REG 5 – TIMER 1 HIGH-ORDER COUNTER

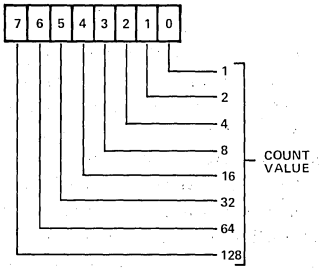


WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. ALSO, AT THIS TIME BOTH HIGH AND LOW-ORDER LATCHES TRANSFERRED INTO T1 COUNTER, AND INITIATES COUNTDOWN. T1 INTERRUPT FLAG ALSO IS RESET.

READ – 8 BITS FROM T1 HIGH-ORDER COUNTER TRANSFERRED TO MPU.

Figure 15. T1 Counter Registers

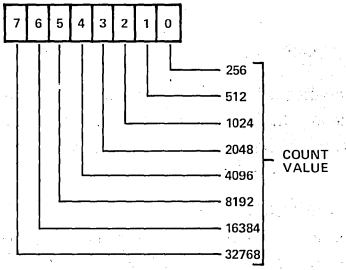
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 LOW-ORDER LATCHES. THIS OPERATION IS NO DIFFERENT THAT A WRITE INTO REG 4.

READ – 8 BITS FROM T1 LOW-ORDER LATCHES TRANSFERRED TO MPU. UNLIKE REG 4 OPERATION, THIS DOES NOT CAUSE RESET OF T1 INTERRUPT FLAG.

REG 7 – TIMER 1 HIGH-ORDER LATCHES



WRITE – 8 BITS LOADED INTO T1 HIGH-ORDER LATCHES. UNLIKE REG 4 OPERATION NO LATCH-TO-COUNTER TRANSFERS TAKE PLACE.

READ – 8 BITS FROM T1 HIGH-ORDER LATCHES TRANSFERRED TO MPU.

Figure 16. T1 Latch Registers

REG 11 – AUXILIARY CONTROL REGISTER

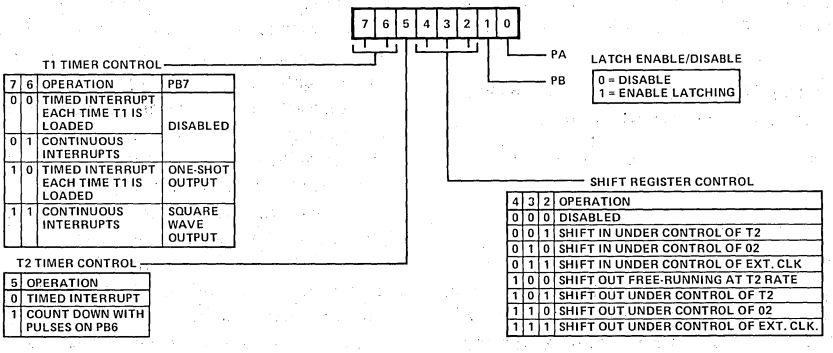


Figure 17. Auxiliary Control Register

Note: The processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

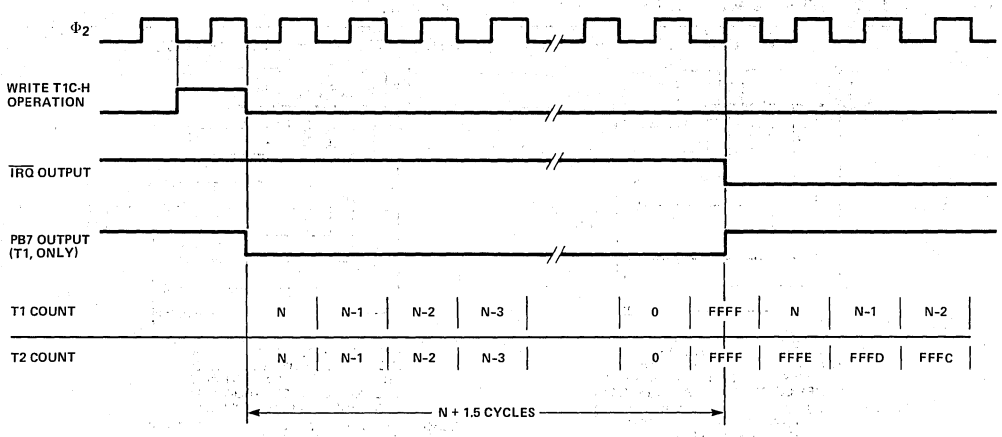


Figure 18. Timer 1 and Timer 2 One-Shot Mode Timing

Timer 1 One-Shot Mode

The interval timer one-shot mode allows generation of a single interrupt for each Timer load operation. In addition, Timer 1 can be programmed to produce a single negative pulse on PB7.

To generate a single interrupt ACR bits 6 and 7 must be 0 then either TIL-L or TIC-L must be written with the low-order count value. (A write to TIC-L is effectively a Write to TIL-L). Next the high-order count value is written to TIC-H, (the value is simultaneously written into TIL-H), and TIL-L is transferred to TIC-L. Countdown begins on the ϕ_2 following the write TIC-H and decrements at the ϕ_2 rate. T1 interrupt occurs when the counters reach 0. Generation of a negative pulse on PB7 is done in the same manner except ACR bit 7 must be a one. PB7 will go low after a Write TIC-H and go high again when the counters reach 0.

The T1 interrupt flag is reset by either writing TIC-H (starting a new count) or by reading TIC-L.

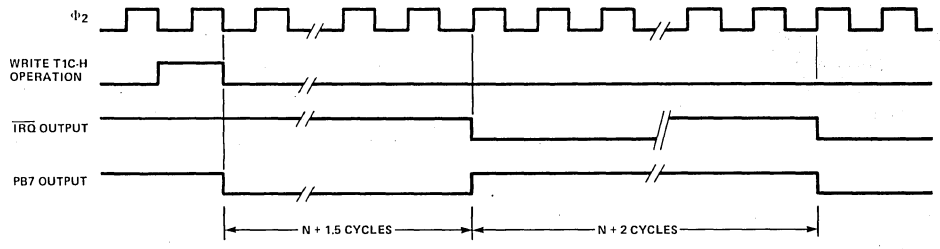
Timing for the one-shot mode is illustrated in Figure 18.

Timer 1 Free-Run Mode

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode, the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. It is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out. The interrupt flag can be cleared by reading TIC-L, by writing directly into the flag as described later, or if a new count value is desired by a write to TIC-H.

All interval timers in the SY6522 are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 19.



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 19. Timer 1 Free-Run Mode Timing

Timer 2 Operation

Timer 2 operates as an interval timer (in the "one-slot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate. Figure 20 illustrates the T2 Counter Registers.

Timer 2 One-Shot Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, (reading 0) the counters "roll-over" to all 1's ($FFFF_{16}$) and continue decrementing, allowing the user to read them and determine how long T2 interrupt has been set. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 18.

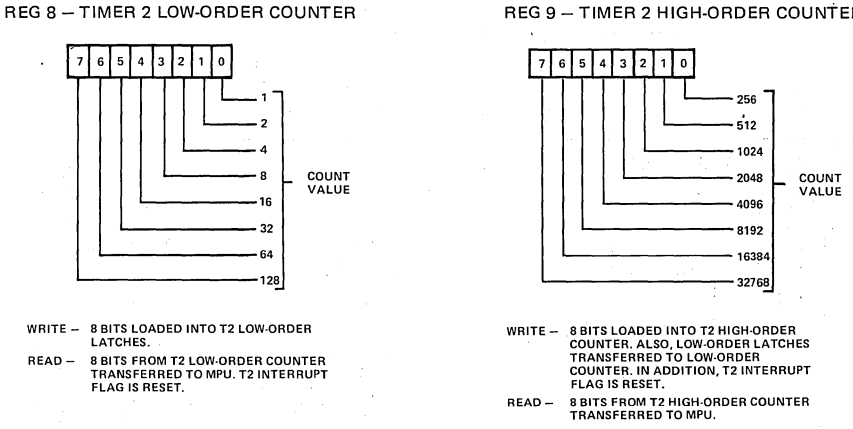


Figure 20. T2 Counter Registers

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 21. The pulse must be low on the leading edge of $\Phi 2$.

Shift Register Operation

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. Figure 22 illustrates the configuration of the SR data bits and the SR control bits of the ACR.

Figures 23 and 24 illustrate the operation of the various shift register modes.

Interrupt Operation

Controlling interrupts within the SY6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signaling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

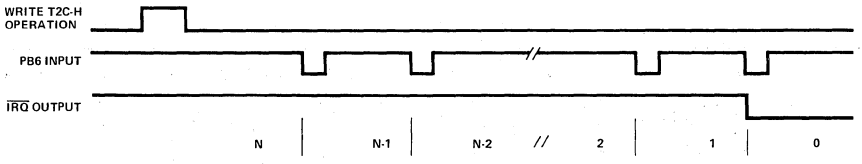
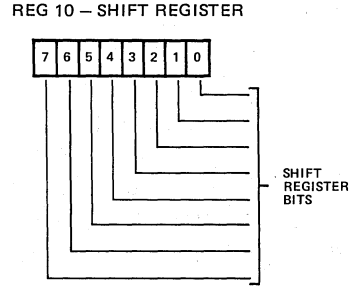
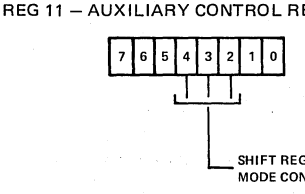


Figure 21. Timer 2 Pulse Counting Mode



NOTES:
1. WHEN SHIFTING OUT, BIT 7 IS THE FIRST BIT OUT AND SIMULTANEOUSLY IS ROTATED BACK INTO BIT 0.
2. WHEN SHIFTING IN, BITS INITIALLY ENTER BIT 0 AND ARE SHIFTED TOWARDS BIT 7.



4	3	2	OPERATION
0	0	0	DISABLED
0	0	1	SHIFT IN UNDER CONTROL OF T2
0	1	0	SHIFT IN UNDER CONTROL OF Φ_2
0	1	1	SHIFT IN UNDER CONTROL OF EXT CLK
1	0	0	SHIFT OUT FREE-RUNNING AT T2 RATE
1	0	1	SHIFT OUT UNDER CONTROL OF T2
1	1	0	SHIFT OUT UNDER CONTROL OF Φ_2
1	1	1	SHIFT OUT UNDER CONTROL OF EXT CLK

Figure 22. SR and ACR Control Bits

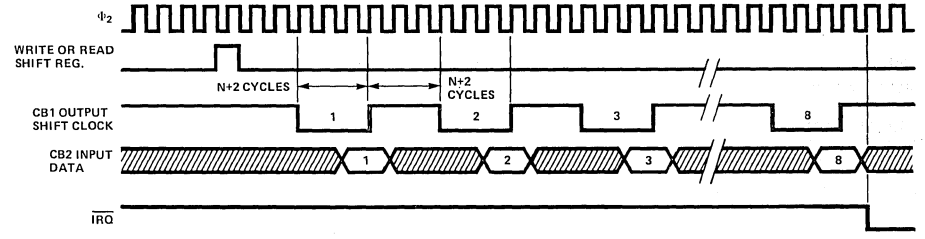
SR Disabled (000)

The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Shift in Under Control of T2 (001)

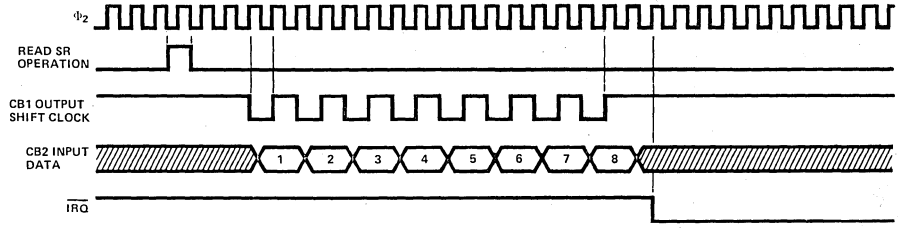
In the 001 mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch (N).

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit of the shift register on the negative-going edge of each clock pulse. The input data should change before the positive-going edge of the CB1 clock pulse. This data is shifted into the shift register during the ϕ_2 clock cycle following the positive-going edge of the CB1 clock pulse. After 8 CB1 clock pulses, the shift register interrupt flag will be set and $\overline{IRQ}$ will go low.



Shift in Under Control of ϕ_2 (010)

In mode 010 the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each ϕ_2 clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.



Shift in Under Control of External CB1 Clock (011)

In mode 011 CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high.

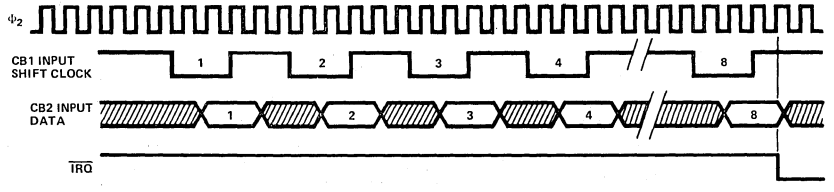
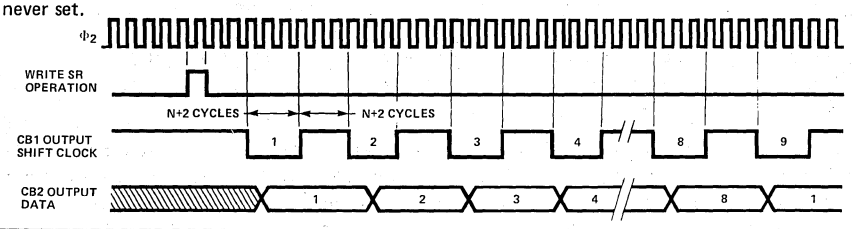


Figure 23. Shift Register Input Modes

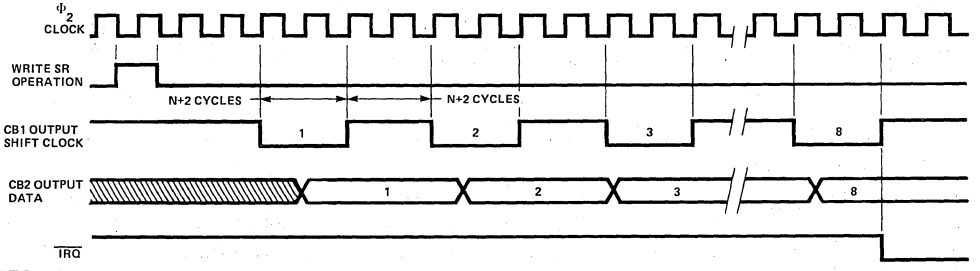
Shift Out Free-Running at T2 Rate (100)

Mode 100 is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CR2 repetitively. In this mode the shift register counter is disabled, and $\overline{IRQ}$ is never set.



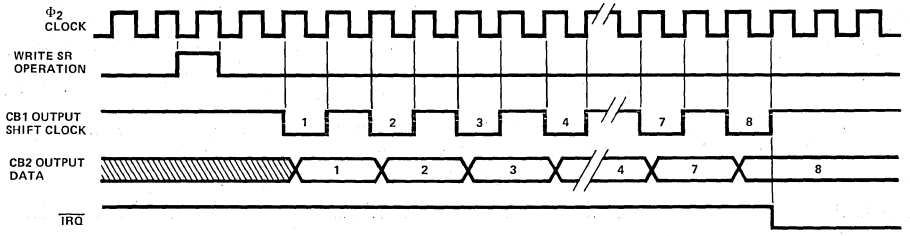
Shift Out Under Control of T2 (101)

In mode 101 the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in external devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 remains at the last data level.



Shift Out Under Control of ϕ_2 (110)

In mode 110, the shift rate is controlled by the ϕ_2 system clock.



Shift Out Under Control of External CB1 Clock (111)

In mode 111 shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

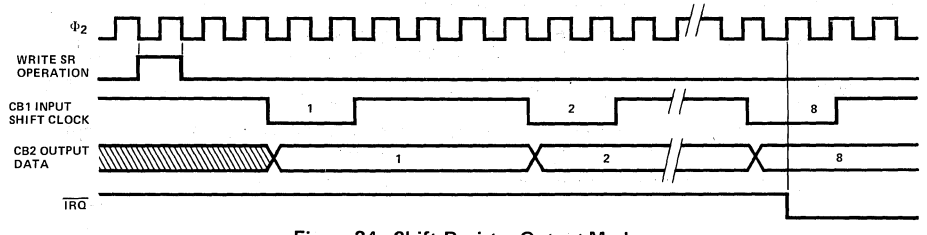


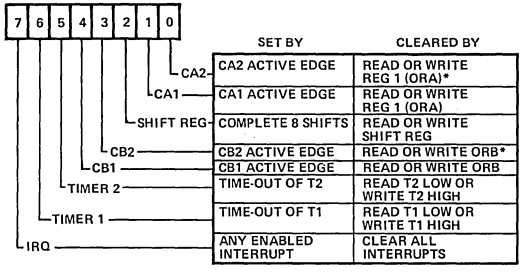
Figure 24. Shift Register Output Modes

The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) are depicted in Figures 25 and 26, respectively.

The IFR may be read directly by the processor. In addition, individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the IRQ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

REG 13 — INTERRUPT FLAG REGISTER



	SET BY	CLEARED BY
CA2	CA2 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)*
CA1	CA1 ACTIVE EDGE	READ OR WRITE REG 1 (ORA)
SHIFT REG	COMPLETE 8 SHIFTS	READ OR WRITE SHIFT REG
CB2	CB2 ACTIVE EDGE	READ OR WRITE ORB*
CB1	CB1 ACTIVE EDGE	READ OR WRITE ORB
TIMER 2	TIME-OUT OF T2	READ T2 LOW OR WRITE T2 HIGH
TIMER 1	TIME-OUT OF T1	READ T1 LOW OR WRITE T1 HIGH
IRQ	ANY ENABLED INTERRUPT	CLEAR ALL INTERRUPTS

* IF THE CA2/CB2 CONTROL IN THE PCR IS SELECTED AS "INDEPENDENT" INTERRUPT INPUT, THEN READING OR WRITING THE OUTPUT REGISTER ORA/ORB WILL NOT CLEAR THE FLAG BIT. INSTEAD, THE BIT MUST BE CLEARED BY WRITING INTO THE IFR, AS DESCRIBED PREVIOUSLY.

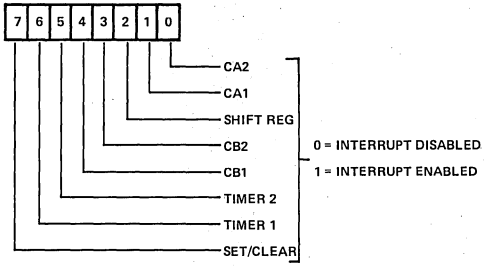
Figure 25. Interrupt Flag Register (IFR)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a logic 1.

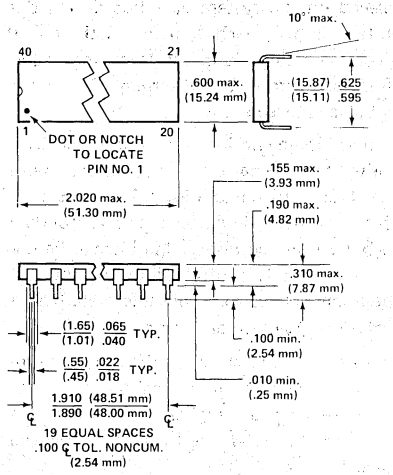
REG 14 — INTERRUPT ENABLE REGISTER



NOTES:
1. IF BIT 7 IS A "0", THEN EACH "1" IN BITS 0 - 6 DISABLES THE CORRESPONDING INTERRUPT.
2. IF BIT 7 IS A "1", THEN EACH "1" IN BITS 0 - 6 ENABLES THE CORRESPONDING INTERRUPT.
3. IF A READ OF THIS REGISTER IS DONE, BIT 7 WILL BE "1" AND ALL OTHER BITS WILL REFLECT THEIR ENABLE/DISABLE STATE.

Figure 26. Interrupt Enable Register (IER)

PACKAGE OUTLINE

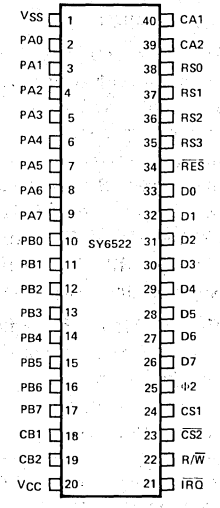


NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

ORDERING INFORMATION

Order Number	Package Type	Frequency Option
SYP 6522	Plastic	1 MHz
SYP 6522A	Plastic	2 MHz
SYC 6522	Ceramic	1 MHz
SYC 6522A	Ceramic	2 MHz

PIN CONFIGURATION



MICRO-PROCESSORS

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Versatile Interface Adapter (VIA)

Extended Temperature (-40°C to +85°C)

SYE6522/ SYE6522A

MICROPROCESSOR PRODUCTS

- Two 8-Bit Bidirectional I/O Ports
- Two 16-Bit Programmable Timer/Counters
- Serial Data Port
- Single +5V Power Supply
- TTL Compatible
- CMOS Compatible Peripheral Port A Lines
- Expanded "Handshake" Capability Allows Positive Control of Data Transfers Between Processor and Peripheral Devices
- Latched Output and Input Registers
- 1 MHz Operation
- Operation over wide temperature range (-40°C to +85°C)

The SYE6522 Versatile Interface Adapter (VIA) is a very flexible I/O control device. In addition, this device contains a pair of very powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each line can be programmed as either an input or an output. Several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves or for counting externally generated pulses. To facilitate control of the many powerful features of this chip, an interrupt flag register, an interrupt enable register and a pair of function control registers are provided.

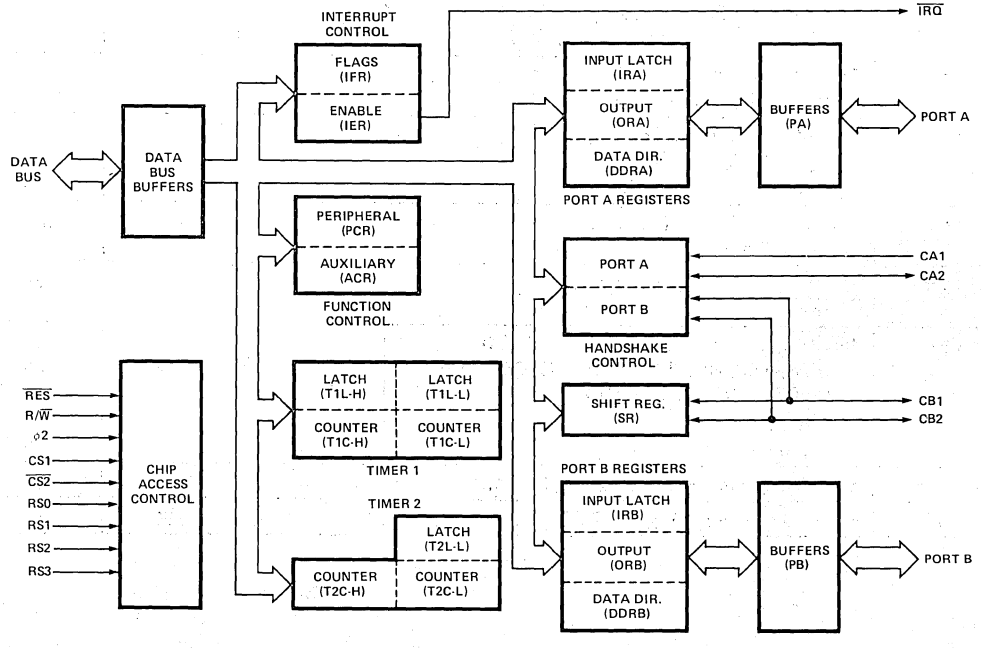


Figure 1. SYE6522 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to +7.0	V
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

ORDERING INFORMATION

Part Number	Package	Clock Frequency
SYEC6522	Ceramic	1 MHz
SYED6522	Cerdip	1 MHz
SYEP6522	Plastic	1 MHz

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = -40°C to +85°C unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage (all except $\phi 2$)	2.4	V_{CC}	V
V_{CH}	Clock High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage Current — V_{IN} = 0 to 5 Vdc R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, $\Phi 2$	—	±2.5	μA
I_{TSI}	Off-state Input Current — V_{IN} = .4 to 2.4V V_{CC} = Max, D0 to D7	—	±10	μA
I_{IH}	Input High Current — V_{IH} = 2.4V PA0-PA7, CA2, PB0-PB7, CB1, CB2	-100	—	μA
I_{IL}	Input Low Current — V_{IL} = 0.4 Vdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	—	-1.6	mA
V_{OH}	Output High Voltage V_{CC} = min, I_{load} = -100 μAdc PA0-PA7, CA2, PB0-PB7, CB1, CB2	2.4	—	V
V_{OL}	Output Low Voltage V_{CC} = min, I_{load} = 1.6 mAdc	—	0.4	V
I_{OH}	Output High Current (Sourcing) V_{OH} = 2.4V V_{OH} = 1.5V (PB0-PB7)	 -100 -1.0	 — —	 μA mA
I_{OL}	Output Low Current (Sinking) V_{OL} = 0.4 Vdc	1.6	—	mA
I_{OFF}	Output Leakage Current (Off state) $\overline{IRQ}$	—	10	μA
C_{IN}	Input Capacitance — T_A = 25°C, f = 1 MHz (R/$\overline{W}$, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, D0-D7, PA0-PA7, CA1, CA2, PB0-PB7) (CB1, CB2) ($\Phi 2$ Input)	 — — —	 7.0 10 20	 pF pF pF
C_{OUT}	Output Capacitance — T_A = 25°C, f = 1 MHz	—	10	pF
P_D	Power Dissipation V_{CC} = 5.25V	—	750	mW

Memory, I/O, Timer Array

SYNERTEK
A SUBSIDIARY OF HONEYWELL

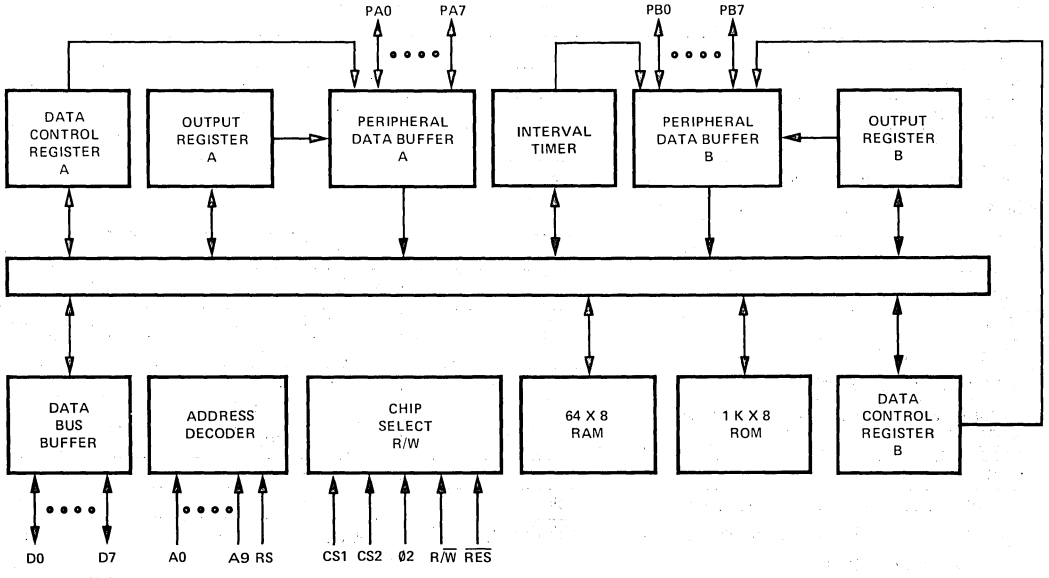
SY6530

MICROPROCESSOR PRODUCTS

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

The SY6530 is designed to operate in conjunction with the SY6500 microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in intervals from 1 to 262,144 clock periods.

FIGURE 1. SY6530 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) . . . . . -.3 to +7.0V
Input/Output Voltage (V_{IN}) . . . . . -.3 to +7.0V
Operating Temperature (T_{OP}) . . . . . 0 to 70°C
Storage Temperature Range (T_{STG}) . . . . . -55 to +150°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C)

	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	-0.3		0.4	V
Input Leakage Current; V_{IN} = V_{SS} +5V AØ-A9, RS, R/$\overline{W}$, $\overline{RES}$, Ø2, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedence State (Three State); V_{IN} = .4V to 2.4V; DØ-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300.		μA
Low Input Current; V_{IN} = .4V PAØ-PA7, PBØ-PB7	I_{IL}		1.0	1.6	mA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leqslant$ -100μA (PAØ-PA7, PBØ-PB7, DØ-D7) $I_{LOAD} \leqslant$ -3mA (PAØ, PBØ)	V_{OH}	 2.4 1.5			V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leqslant$ 1.6mA	V_{OL}			0.4	V
Output High Current (Sourcing); $V_{OH} \geqslant$ 2.4V (PAØ-PA7, PBØ-PB7, DØ-D7) $\geqslant$ 1.5V Available for other than TTL (Darlingtons) (PAØ, PBØ)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA mA
Output Low Current (Sinking); $V_{OL} \leqslant$ .4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CLK}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation (V_{CC}= 5.25V)	P_D			700	mW

*When Programmed as address pins All values are D.C. readings

WRITE TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Period	T_{CYC}	1		10	μs
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/$\overline{W}$ valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μs
Peripheral data valid after negative transition of clock driving CMOS (Level = V_{CC} -30%)	T_{CMOS}			2	μs
R/$\overline{W}$ hold time after negative clock transition	T_{CWW}	0			ns
Address hold time	T_{CAH}	0			ns

READ TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
R/$\overline{W}$ valid before positive transition of clock	T_{WCR}	180			ns
Address valid before positive transition of clock	T_{ACR}	180			ns
Peripheral data valid before positive transition of clock	T_{PCR}	300			ns
Data bus valid after positive transition of clock	T_{CDR}			395	ns
Data Bus Hold Time	T_{HR}	10			ns
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200			ns
R/$\overline{W}$ hold time after negative clock transition	T_{CWR}	0			ns
Address hold time	T_{CAH}	0			ns

Loading = 30 pF + 1 TTL load for PAØ-PA7, PBØ-PB7
= 130 pF + 1 TTL load for DØ-D7

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)
During system initialization a low ($\leqslant$0.4V) on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs, protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock (ϕ 2)
The input clock is a system Phase Two clock.

Read/Write (R/$\overline{W}$)
R/$\overline{W}$ is supplied by the microprocessor and is used to control the transfer of data to and from the SY6530. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the SY6530. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the SY6530.

Interrupt Request ($\overline{IRQ}$)
The $\overline{IRQ}$ output is derived from the interval timer. The same line, if not used as an interrupt, can be used as a peripheral I/O (PB7). When used as an interrupt, the pin should be set to an input in the data direction register. As $\overline{IRQ}$ the output will be normally high with a low indicating an interrupt from the SY6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pull-up may be omitted with a mask option.

Data Bus (D0-D7)
The SY6530 has eight bi-directional data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)
The SY6530 has two 8-bit peripheral I/O ports, Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually software programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed as an input. Likewise, by writing "1" to any bit position in the DDR will cause the corresponding line to act as an output.

When the Ports are programmed as inputs and their output registers (ORA and ORB) are read by the MPU, the level on the port lines will be transferred to the Data Bus. When the ports are programmed as outputs the lines will reflect the data written by the MPU into the output registers.

PA0 and PB0 are capable of direct transistor drive (source 3mA at 1.5V).

Address and Select Lines (A0-A9, RS, PB5 and PB6)
A0-A9 and ROM SELECT (RS) are always used as addressing lines. There are 2 additional lines which are mask programmable and can be used either individually or together as CHIP SELECTS. They are PB5 and PB6. When used as peripheral data lines they cannot be used as chip selects.

FIGURE 2. WRITE TIMING CHARACTERISTICS

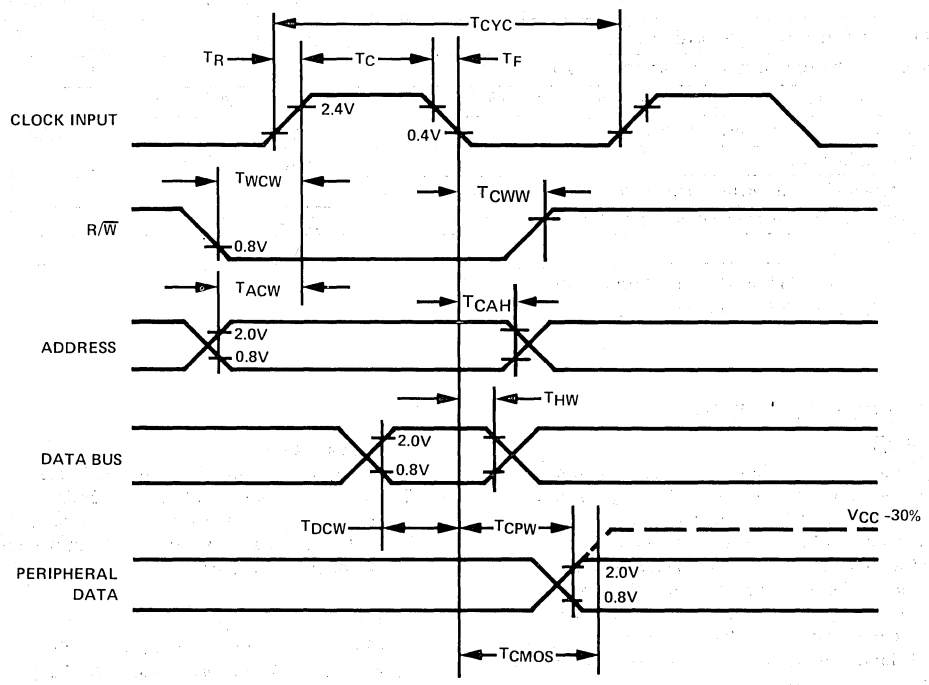
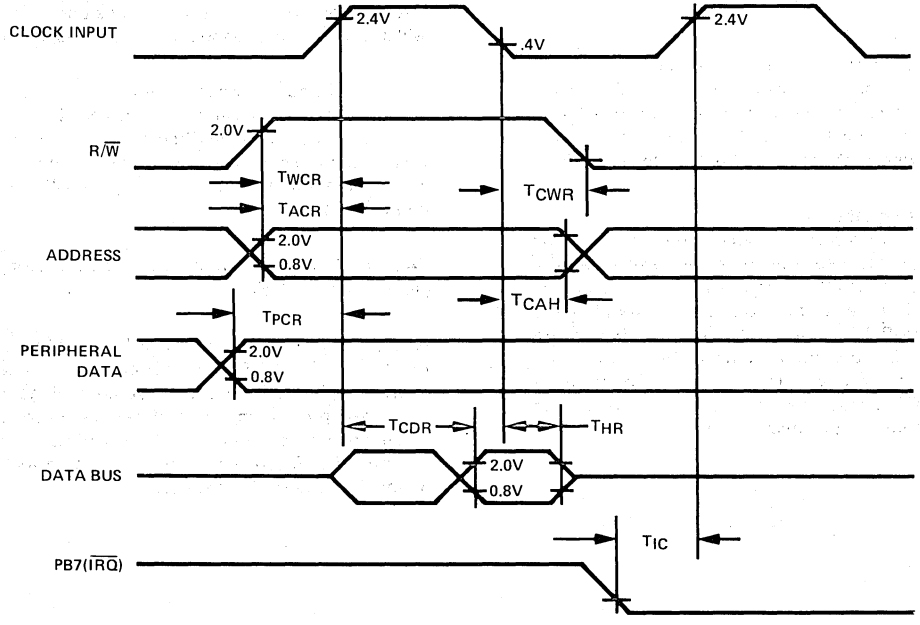


FIGURE 3. READ TIMING CHARACTERISTICS



INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1 K Byte (8 K Bits)
The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS are needed to address the entire ROM. With the addition of CS1 and CS2, seven SY6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM-64 Bytes (512 Bits)
A 64 x 8 static RAM is contained on the SY6530. It is addressed by A0-A5 (Byte Select), RS, A6, A7, A8, A9, and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers
There are four 8-bit internal registers, two data direction registers (DDRA and DDRB) and two peripheral I/O data registers (ORA and ORB). The two data direction registers control the direction of the data into and out of the peripheral line. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer line as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction A, position 3, sets up peripheral line PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a read operation by the microprocessor the SY6530 transfers the TTL level on the peripheral data lines to the data bus. For the peripheral data lines which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral lines.

Interval Timer
The Timer section of the SY6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock continues counting down at a 1T rate to a maximum of -255T. This allows the user to read the counter and then determine how long the interrupt has been set.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 00110100 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written into the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., $A_3 = 1$ enables $\overline{IRQ}$ on PB7, $A_3 = 0$ disables $\overline{IRQ}$ on PB7. When PB7 is used as $\overline{IRQ}$ with the Interval Timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to 00000000 an interrupt will occur on the next count and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of 1 1 1 0 0 1 1 1 is read, the time since interrupt is 28T. The value read is in two's complement.

Value Read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus, to arrive at the total elapsed time, merely do a two's complement and add to the original time written into the Timer. Again, assume time written as 00110100 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After an interrupt, whenever the Timer is written or read the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 5 illustrates an example of interrupt.

FIGURE 4. BASIC ELEMENTS OF INTERVAL TIMER

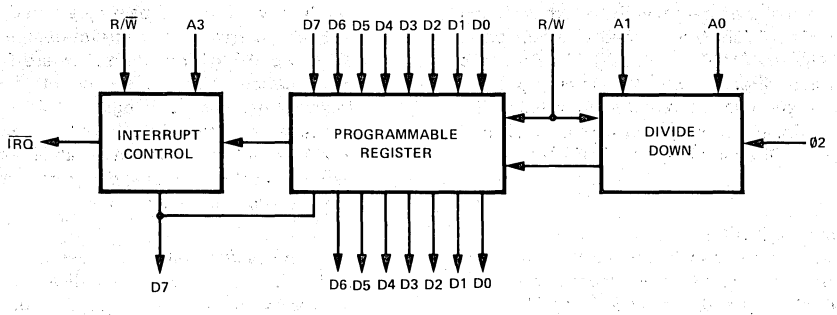
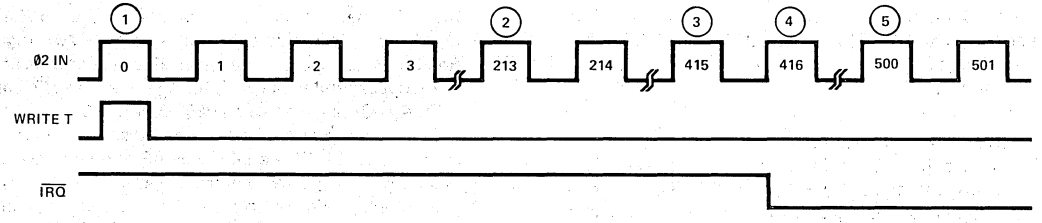


FIGURE 5. TIMER INTERRUPT TIMING



1. Data written into Interval Timer is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval Timer is 0 0 0 1 1 0 0 1 = 25_{10}

$$52 - \frac{213}{8} - 1 = 52-26-1 = 25$$

3. Data in Interval Timer is 0 0 0 0 0 0 0 0 = 0_{10}

$$52 - \frac{415}{8} - 1 = 52-51-1 = 0$$

4. Interrupt has occured at ϕ_2 pulse #416
   Data in Interval Timer = 1 1 1 1 1 1 1 1
5. Data in Interval Timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ output. This is done so as to avoid future interrupts until another Write timer operation.

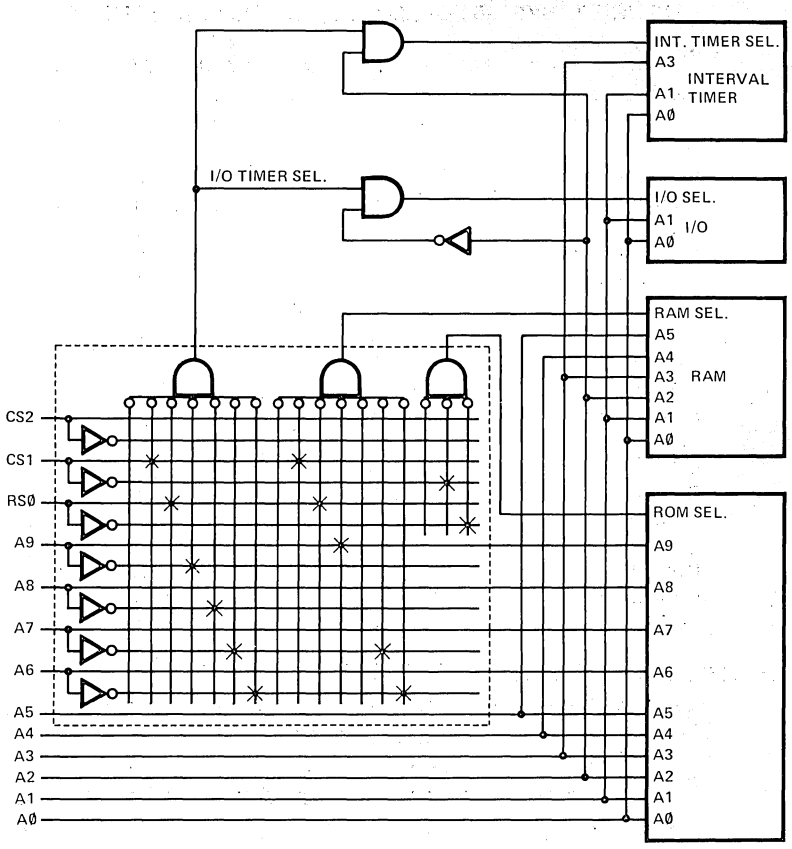
ADDRESSING

Because the address decode matrix is maskable the SY6530 offers many variations to the user. RAM, ROM and the I/O — Interval Timer block may be enabled individually by any combination of A6-A9 plus RS, CS1 and CS2 (refer to Figure 6 for a typical configuration). Because CS1 and CS2 are mask options and act independently neither, either, or both may be masked as Chip Selects or Port B lines.

One-Chip Addressing

Figure 6 illustrates a 1-chip system for the SY6530, and Figure 8 details address decoding.

FIGURE 6. SY6530 ONE CHIP ADDRESS ENCODING SCHEME



A. X indicates mask programming
i.e. ROM select = CS1•RSO
RAM select = $\overline{CS1}$•$\overline{RSO}$•$\overline{A9}$•A7•A6
I/O TIMER SELECT = $\overline{CS1}$•$\overline{RSO}$•A9•A8•A7•A6

B. Notice that A8 is a don't care for RAM select

C. The CS2/PB5 pin functions as PB5 in this example.

Seven Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14, and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 lines designated as chip-select or I/O would be mask programmed as chip select. RS would be connected to address line A10. CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

I/O Register — Timer Addressing

The previous two examples have illustrated how to address the ROM, RAM and the general I/O Register — Timer Block. A0 thru A3 specify which of the four I/O registers are selected and select the modes of operation for the Timer. Figure 8 illustrates the internal decoding of these address bits and their function.

Address line A2 selects I/O or Timer. If I/O-Timer Select is enabled and A2 is low the I/O registers are selected and bits A0 and A1 are decoded to select the individual register.

During a write when I/O-Timer Select is enabled and A2 is high the Timer is selected. Bits A0 and A1 select the ÷ by rate (the data lines should at this time have the count value to be written), and A3 determines if PB7 is to act as an $\overline{IRQ}$ output.

The addressing of the ROM select, RAM select and I/O timer select lines would be as follows:

FIGURE 7. SY6530 SEVEN CHIP ADDRESSING SCHEME

		CS2 A12	CS1 A11	RS A10	A9	A8	A7	A6
SY6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
SY6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
SY6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
SY6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
SY6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
SY6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
SY6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

* RAM select for SY6530 #5 would read = $\overline{A12} \bullet \overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$

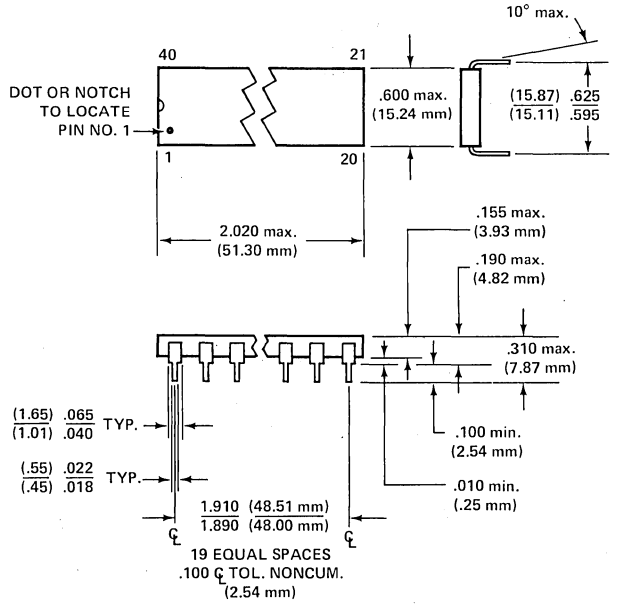
FIGURE 8. ADDRESSING DECODE FOR I/O REGISTER AND TIMER

ADDRESSING DECODE								
	ROM SELECT	RAM SELECT	I/O-TIMER SELECT	R/$\overline{W}$	A3	A2	A1	A0
READ ROM	1	0	0	1	X	X	X	X
WRITE RAM	0	1	0	0	X	X	X	X
READ RAM	0	1	0	1	X	X	X	X
WRITE DDRA	0	0	1	0	X	0	0	1
READ DDRA	0	0	1	1	X	0	0	1
WRITE DDRB	0	0	1	0	X	0	1	1
READ DDRB	0	0	1	1	X	0	1	1
WRITE ORA	0	0	1	0	X	0	0	0
WRITE ORA	0	0	1	1	X	0	0	0
WRITE ORB	0	0	1	0	X	0	1	0
WRITE ORB	0	0	1	1	X	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	*	1	0	0
÷ 8T	0	0	1	0	*	1	0	1
÷ 64T	0	0	1	0	*	1	1	0
÷ 1024T	0	0	1	0	*	1	1	1
READ TIMER	0	0	1	1	*	1	X	0
READ INTERRUPT FLAG	0	0	1	1	X	1	X	1

X = Don't care condition

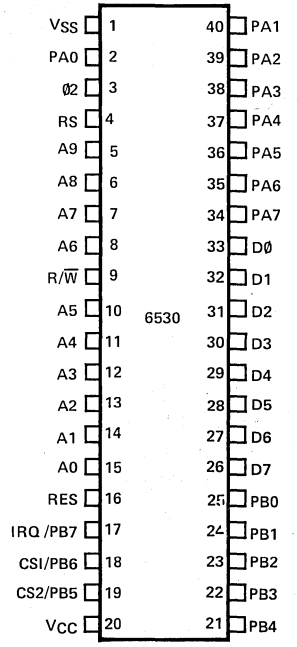
* A_3 = 1 Enables IRQ to PB7

A_3 = 0 Disables IRQ to PB7



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PACKAGE OUTLINE



PIN DESIGNATION

PROGRAMMING INSTRUCTIONS

The SY6530 utilizes computer aided techniques to manufacture and test custom ROM patterns. The pattern and address coding is supplied to Synertek in any of several formats.

1) 2708-type EPROMs.
2) Synertek data card formats.
3) Other input formats, providing they can be translated into one of the above.

Synertek Data Card Format

A. The format for the first and all succeeding records, except for the last record in a file is as follows:

$;N_1N_0 \quad A_3A_2A_1A_0 \quad (D_1D_0)_1 \quad (D_1D_0)_2 \quad X_3X_2X_1X_0$

where:

1. All characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal digit.
2. ; is a record mark indicating the start of a record.
3. N_1N_0 = the number of bytes of data in this record (in hexadecimal). Each pair of hexadecimal characters (D_1D_0) represents a single byte in the record.
4. $A_3A_2A_1A_0$ = the hexadecimal starting address for the record. A_3 represents address bits 15 through 12, etc. The 8-bit byte represented by $(D_1D_0)_1$ is stored in address $A_3A_2A_1A_0$; $(D_1D_0)_2$ is stored in $(A_3A_2A_1A_0) + 1$, etc.
5. (D_1D_0) = two hexadecimal digits representing an 8-bit byte of data. (D_1 = high order 4 binary bits and D_0 = low-order 4 bits). A maximum of 18 (Hex) or 24 (decimal) bytes of data per record is permitted.
6. $X_3X_2X_1X_0$ = record check sum. This is the hexadecimal sum of all characters in the record, including N_1N_0 and $A_3A_2A_1A_0$ but excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hexadecimal digits) and is then represented in the record as four ASCII characters ($X_3X_2X_1X_0$).

B. The format for the last record in a file is as follows:

; 00 $C_3C_2C_1C_0$ $X_3X_2X_1X_0$

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.
2. $C_3C_2C_1C_0$ = the total number of records (in hexadecimal) in this file, including the last record.
3. $X_3X_2X_1X_0$ = check sum for this record.

C. Example

The following example illustrates the exact format of the hex interface file in both listing and punched paper tape form.

```
;18F000CA86004C00F0FDF9212D21FF292DBF2161F5F7FF657D677D0D40
;18F018E564672DFD7575E50000CF4112F800925198D200539192F20C98
;18F03008DB02880810DE12D894189AC2830E9800FBB6232F087F650AA5
;18F048036E20EF2FA58D4465E8FDF93DE775EF257FB520ED64657C0DEB
;18F0607F11D05A1EDF0250B0DAFE009252909912DB108A0298DE080C0D
;18F078D95058DF82D2D79A00ED65E68724EE05212764A5F5BDA9050E2C
;18F090EC20FF6525252469332 13F20FF31293B7E18D65042DE40500A92
;18F0A81E5E5B02534A53DE4A9B189259969F589E5E92DF52DE9E9A0CA2
;18F0C000B3268D2400EF6765E7A0B5606725217D20AF35EDF5202F0C08
;18F0D8692525342B35256CDF12F2785FFF547FD2E2D6525BDF5A720D26
;10F0F012DB020F1A1ABF86D2DA9ADAC8DECA1B0A12
;00000B000B
```

ADDITIONAL PATTERN INFORMATION

In addition to the ROM data patterns, it is necessary to provide the information outlined below.

CUSTOMER NAME
CUSTOMER PART NO.
CUSTOMER CONTACT (NAME)
CUSTOMER TELEPHONE NO.
CS1/PB6 (ENTER "CS1" OR "PB6")
CS2/PB5 (ENTER "CS2" OR "PB5")
PULL-UP RESISTOR ON PB7 ("YES" OR "NO")
LOGIC FORMAT ("POS" OR "NEG")

DEVICE ADDRESSING (Enter "H" for High, "L" for Low, or "N" for don't care)

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT							
RAM SELECT							
I/O TIMER SELECT							

Send Information To:

Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

SY6530 CUSTOMER SPECIFICATION FORM

1. Date.

2. Customer name.

3. Customer part no.
   (maximum 10 digits)

4. Synertek "C" number.

5. Customer Contact.

6. Customer phone number

7. Chip Select Code
   (Check one square in each block)

CS1	
PB6	

CS2	
PB5	

PULL UP	YES	
ON PB7	NO	

8. ROM/RAM/I-O SELECTS (Specify H or L or N (don't care) in each box.

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT				N	N	N	N
RAM SELECT							
I/O SELECT							

9. Customer's Input

   Punched Cards ☐
   Punched Tape ☐

10. Data Format

    MOS Technology ☐
    Intel Hex ☐
    Intel BPNF ☐
    Binary ☐

11. Logic Format

    Positive ☐
    Negative ☐

12. Verification Status

    Hold ☐
    Not Required ☐

RAM, I/O, Timer Array

SY6532

MICROPROCESSOR PRODUCTS

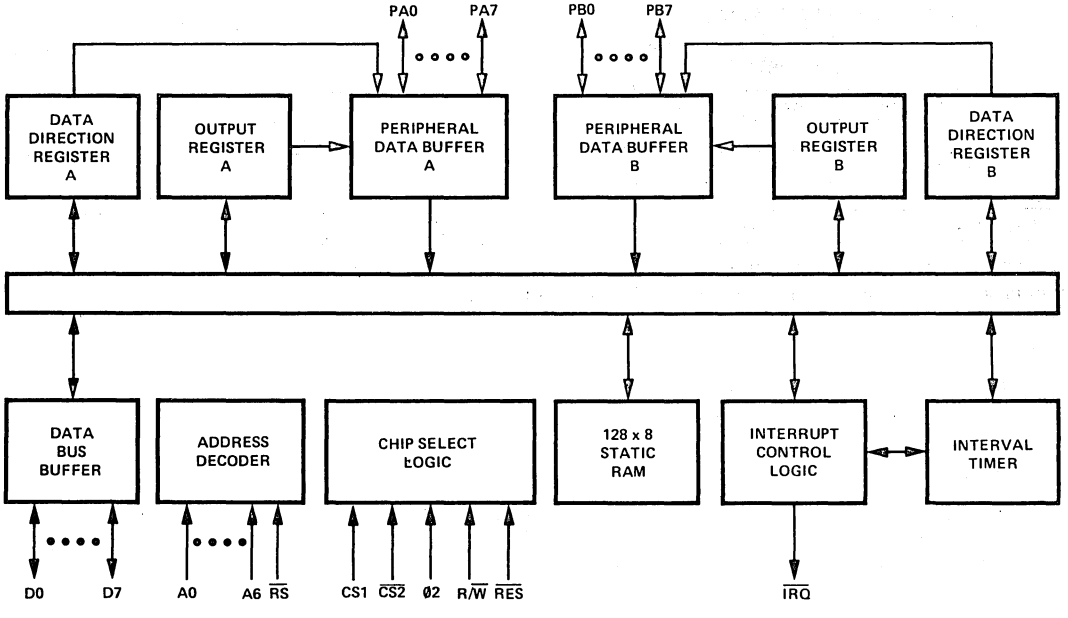
SYNERTEK
A SUBSIDIARY OF HONEYWELL

The SY6532 is designed to operate in conjunction with the SY6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins

MICRO-PROCESSORS

Figure 1. 6532 BLOCK DIAGRAM



MAXIMUM RATINGS

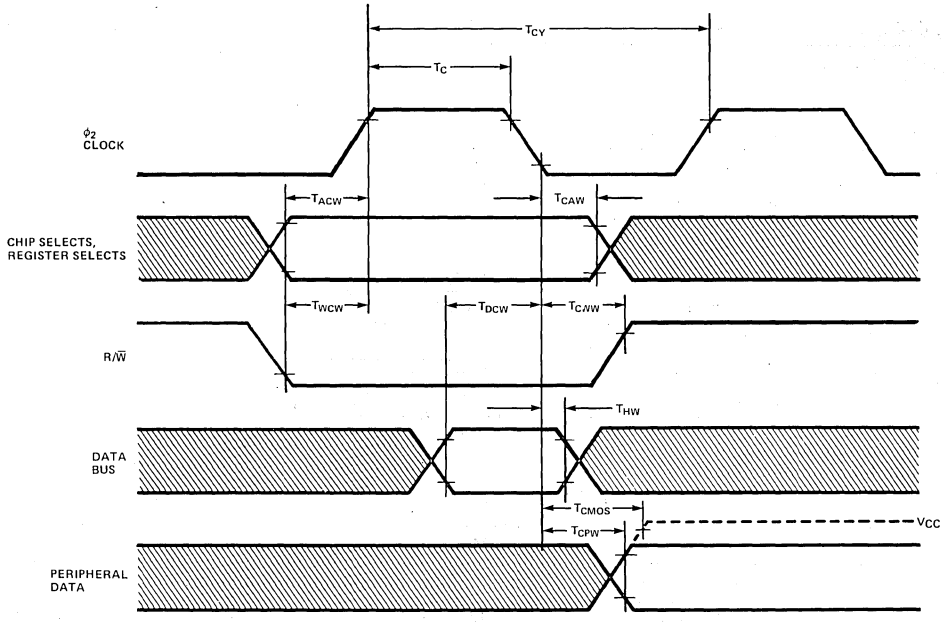
RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V_{CC}	-.3 to +7.0	V
Input/Output Voltage	V_{IN}	-.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0 - 70°C)

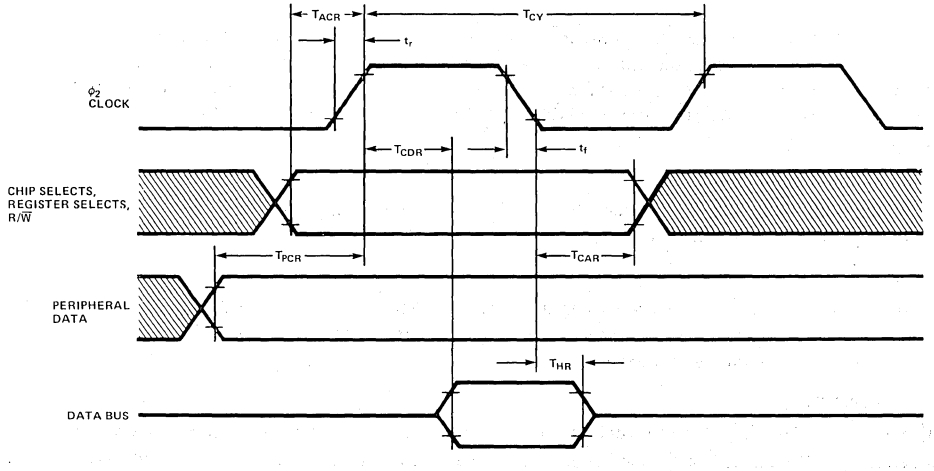
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	.3		.4	V
Input Leakage Current; V_{IN} = V_{SS} + 5V AØ-A6, $\overline{RS}$, R/W, $\overline{RES}$, Ø2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = .4V to 2.4V; DØ-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300.		μA
Input Low Current; V_{IN} = .4V PAØ-PA7, PBØ-PB7	I_{IL}		1.0	1.6	mA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leq$ -100μA (PAØ-PA7, PBØ-PB7, DØ-D7) $I_{LOAD} \leq$ 3 MA (PBØ-PB7)	V_{OH}				V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leq$ 1.6MA	V_{OL}			.4	V
Output High Current (Sourcing); $V_{OH} \geq$ 2.4V (PAØ-PA7, PBØ-PB7, DØ-D7) $\geq$ 1.5V Available for direct transistor drive (PBØ-PB7)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA mA
Output Low Current (Sinking); $V_{OL} \leq$ .4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{Clk}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation (V_{CC} = 5.25V)	P_D			660	mW

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

WRITE TIMING CHARACTERISTICS



READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS

Symbol	Parameter	SY6532		SY6532A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.50	50	μs
T_C	φ2 Pulse Width	0.44	25	0.22	25	μs
T_{ACW}	Address Set-Up Time	180	–	90	–	ns
T_{CAW}	Address Hold Time	0	–	0	–	ns
T_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
T_{CWW}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
T_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
T_{HW}	Data Bus Hold Time	10	–	10	–	ns
T_{CPW}	Peripheral Data Delay Time	–	1.0	–	1.0	μs
T_{CMOS}	Peripheral Data Delay Time to CMOS Levels	–	2.0	–	2.0	μs

NOTE: tr, tf = 10 to 30ns.

READ TIMING CHARACTERISTICS

Symbol	Parameter	SY6532		SY6532A		Unit
		Min.	Max.	Min.	Max.	
T_{CY}	Cycle Time	1	50	0.5	50	μs
T_{ACR}	Address Set-Up Time	180	–	90	–	ns
T_{CAR}	Address Hold Time	0	–	0	–	ns
T_{PCR}	Peripheral Data Set-Up Time	300	–	300	–	ns
T_{CDR}	Data Bus Delay Time	–	340	–	200	ns
T_{HR}	Data Bus Hold Time	10	–	10	–	ns

NOTE: tr, tf = 10 to 30ns.

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc \pm^{.3}_{.2}$).

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the SY6532. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the SY6532. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the SY6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output is derived from the interrupt control logic. It will normally be high with a low indicating an interrupt from the SY6532. $\overline{IRQ}$ is an open-drain output, permitting several units to be wire-or'ed to the common $\overline{IRQ}$ microprocessor input pin. The $\overline{IRQ}$ output may be activated by a transition on PA7 or timeout of the Interval Timer.

Data Bus (D0-D7)

The SY6532 has eight bi-directional data lines (D0-D7). These lines connect to the system's data bus and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0-PA7, PB0-PB7)

The SY6532 has two 8-bit peripheral I/O Ports, Port A (lines PA0-PA7) and Port B (lines PB0-PB7). Each line is individually programmable as either an input or an output. By writing a "0" to any bit position of the Data Direction Register (DDRA or DDRB) the corresponding line will be programmed as an input. Likewise, by writing a "1" to any bit position in DDRA or DDRB will cause the corresponding line to act as an output.

When a Port line is programmed as an input and its ouput register (ORA or ORB) is read by the MPU, the TTL level on the Port line will be transferred to the data bus. When the Port lines are programmed as outputs, the lines will reflect the data written by the MPU into the output registers. See Edge Sense Interrupt Section for an additional use of PA7.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

A0-A6 and $\overline{RS}$ are used to address the RAM, I/O registers, Timer and Flag register. CS1 and $\overline{CS2}$ are used to select (enable access to) the SY6532.

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the SY6532. It is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral I/O. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding line of the I/O port to act as an input. A logic one causes the corresponding line to act as an output. The voltage on any line programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA lines during a peripheral read operation. For a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the line is allowed to be $\geqslant 2.4$ volts for a logic one and $\leqslant 0.4$ volts for a zero. If the loading on the line does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB lines are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB lines.

Interval Timer

The Timer section of the SY6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 2.

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T, or 1024T increments, where T is the system clock period. When a full count is reached, the interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock continues counting down, but at a 1T rate to a maximum of -255T. This allows the user to read the counter and then determine how long the interrupt has been set.

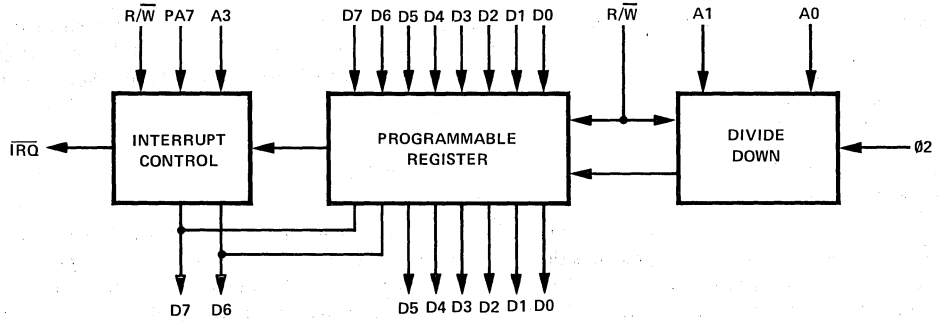
The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., $A_3 = 1$ enables $\overline{IRQ}$, $A_3 = 0$ disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs $\overline{IRQ}$ will go low. When the Timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the Timer has counted down to 0 0 0 0 0 0 0 0 an interrupt will occur on the next count time and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the Timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read	= 1 1 1 0 0 1 0 0
Complement	= 0 0 0 1 1 0 1 1
Add 1	= 0 0 0 1 1 1 0 0 = 28.

Figure 2. BASIC ELEMENTS OF INTERVAL TIMER

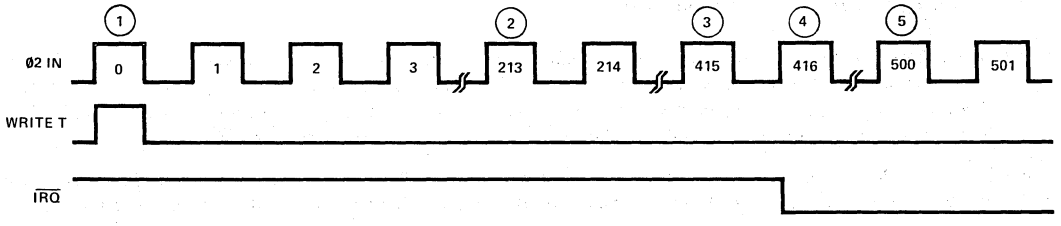


Thus, to arrive at the total elapsed time, merely do a two's complement and add to the original time written into the Timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After an interrupt, whenever the Timer is written or read the interrupt is reset. However, the reading of the Timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 3 illustrates an example of interrupt.

Figure 3. TIMER INTERRUPT TIMING



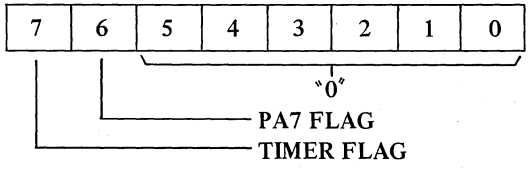
1. Data written into Interval Timers is $0\,0\,1\,1\,0\,1\,0\,0 = 52_{10}$
2. Data in Interval timer is $0\,0\,0\,1\,1\,0\,0\,1 = 25_{10}$
   $52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$
3. Data in Interval Timer is $0\,0\,0\,0\,0\,0\,0\,0 = 0_{10}$
   $52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$
4. Interrupt has occurred at Ø2 pulse #416
   Data in Interval Timer = 1 1 1 1 1 1 1 1
5. Data in Interval Timer is 1 0 1 0 1 1 0 0
   two's complement is $0\,1\,0\,1\,0\,1\,0\,0 = 84_{10}$
   $84 + (52 \times 8) = 500_{10}$

When reading the Timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.

Figure 4. INTERRUPT FLAG REGISTER



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

ADDRESSING

Addressing of the SY6532 is accomplished by the 7 address inputs, the $\overline{RS}$ input and the two chip select inputs CS1 and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval Timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O-Timer Section the $\overline{RS}$ input is used. When this input is low the RAM is addressed, when high the I/O Interval Timer section is addressed. To distinguish between Timer and I/O, address line A2 is utilized. When A2 is high the Interval Timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Table 1.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register.

I/O Register - Timer Addressing

Table 1 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinguishes I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1 ADDRESSING DECODE

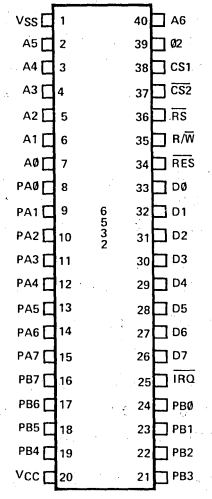
FUNCTION	$\overline{RS}$	A6	A5	A4	A3	A2	A1	A0	WR	RD
RAM	L	X	X	X	X	X	X	X	√	√
ORA	H	—	—	—	—	L	L	L	√	√
DDRA	H	—	—	—	—	L	L	H	√	√
ORB	H	—	—	—	—	L	H	L	√	√
DDRB	H	—	—	—	—	L	H	H	√	√
Timer, ÷1, IRQ ON	H	—	—	H	L	H	L	L	√	
Timer, ÷8, IRQ ON	H	—	—	H	L	H	L	H	√	
Timer, ÷64, IRQ ON	H	—	—	H	L	H	H	L	√	
Timer, ÷1024, IRQ ON	H	—	—	H	L	H	H	H	√	
Timer, ÷1, IRQ OFF	H	—	—	H	H	H	L	L	√	
Timer, ÷8, IRQ OFF	H	—	—	H	H	H	L	H	√	
Timer, ÷64, IRQ OFF	H	—	—	H	H	H	H	L	√	
Timer, ÷1024, IRQ OFF	H	—	—	H	H	H	H	H	√	
Read Timer, IRQ ON	H	—	—	—	L	H	—	L		√
Read Timer, IRQ OFF	H	—	—	—	H	H	—	L		√
Read Interrupt Flags	H	—	—	—	—	H	—	H		√
PA7 IRQ OFF, NEG EDGE	H	—	—	L	—	H	L	L	*	
PA7 IRQ OFF, POS EDGE	H	—	—	L	—	H	L	H	*	
PA7 IRQ ON, NEG EDGE	H	—	—	L	—	H	H	L	*	
PA7 IRQ ON, POS EDGE	H	—	—	L	—	H	H	H	*	

NOTES: X = ADDRESS - = ADDRESS BITS DON'T CARE * = DATA BITS ARE "DON'T CARE"

ORDERING INFORMATION

Part Number	Package	Speed
SYC6532	Ceramic	1 MHz
SYD6532	Cerdip	1 MHz
SYP6532	Plastic	1 MHz
SYC6532A	Ceramic	2 MHz
SYD6532A	Cerdip	2 MHz
SYP6532A	Plastic	2 MHz

PIN DESIGNATION



RAM, I/O, Timer Array

Extended Temperature
(-40°C to +85°C)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SYE6532
SYE6532A

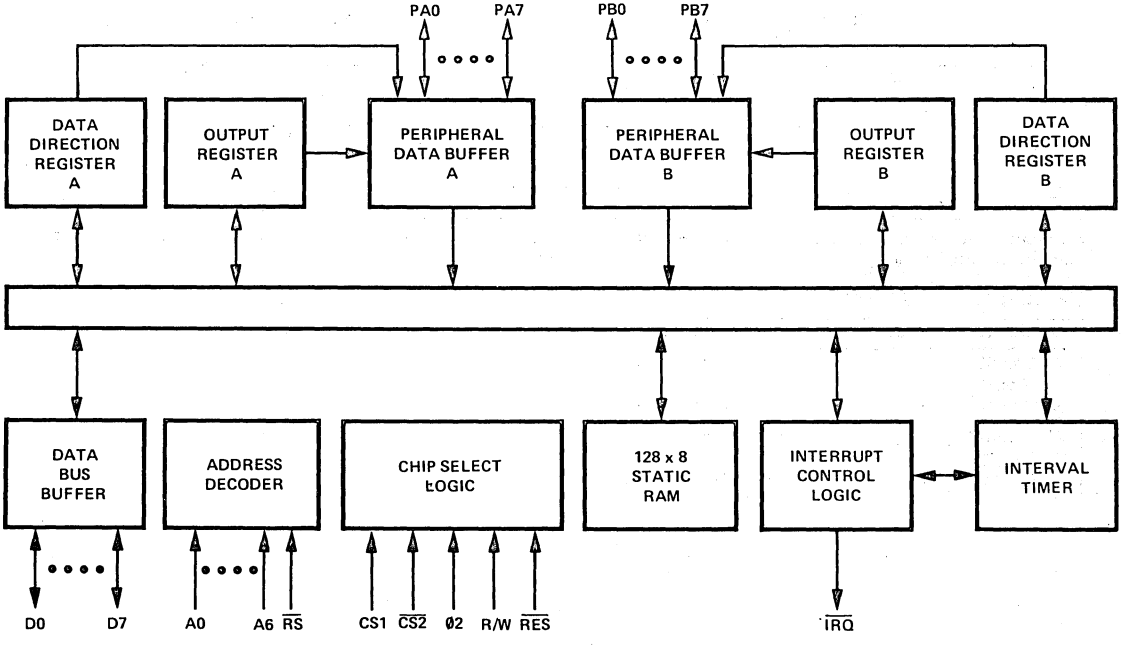
MICROPROCESSOR PRODUCTS

The SYE6532 is designed to operate in conjunction with the SYE6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Operation over wide temperature range (-40°C to +85°C)

MICRO-PROCESSORS

Figure 1. 6532 BLOCK DIAGRAM



MAXIMUM RATINGS

RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V_{CC}	-.3 to +7.0	V
Input/Output Voltage	V_{IN}	-.3 to +7.0	V
Operating Temperature Range	T_{OP}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

D. C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, T_A = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4		V_{CC}	V
Input Low Voltage	V_{IL}	-0.3		0.4	V
Input Leakage Current; V_{IN} = V_{SS} + 5V AØ-A6, $\overline{RS}$, R/W, $\overline{RES}$, Ø2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = .4V to 2.4V; DØ-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300.		μA
Input Low Current; V_{IN} = .4V PAØ-PA7, PBØ-PB7	I_{IL}		1.0	1.6	mA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leq$ -100μA (PAØ-PA7, PBØ-PB7, DØ-D7) $I_{LOAD} \leq$ 3 MA (PBØ-PB7)	V_{OH}	 V_{SS} + 2.4 V_{SS} + 1.5			V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leq$ 1.6MA	V_{OL}			0.4	V
Output High Current (Sourcing); $V_{OH} \geq$ 2.4V (PAØ-PA7, PBØ-PB7, DØ-D7) $\geq$ 1.5V Available for direct transistor drive (PBØ-PB7)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA mA
Output Low Current (Sinking); $V_{OL} \leq$ .4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{Clk}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation V_{CC} = 5.25V	P_D			735	mW

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

ORDERING INFORMATION

Part Number	Package	Clock Frequency
SYEC6532	Ceramic	1 MHz
SYED6532	Cerdip	1 MHz
SYEP6532	Plastic	1 MHz
SYEC6532A	Ceramic	2 MHz
SYED6532A	Cerdip	2 MHz
SYEP6532A	Plastic	2 MHz

CRT Controller

SY6545

SYNERTEK
A SUBSIDIARY OF HONEYWELL

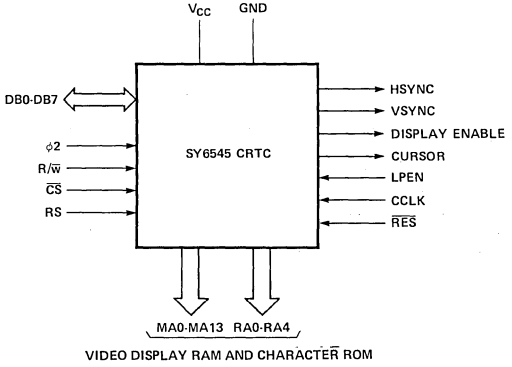
MICROPROCESSOR PRODUCTS

PRELIMINARY

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Interlaced or non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for Video Display RAM.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6545.
- Internal status register.

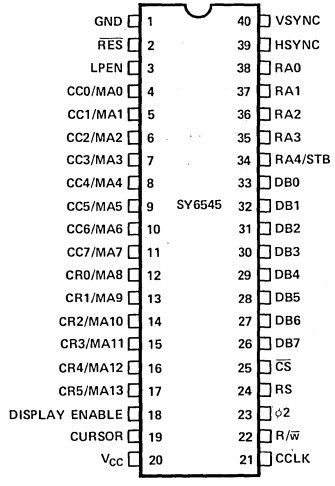
The SY6545 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

INTERFACE DIAGRAM



VIDEO DISPLAY RAM AND CHARACTER ROM

PIN DESIGNATION



ORDERING INFORMATION

Part Number	Package	Clock Rate
SYC6545	Ceramic	1 MHz
SYD6545	Cerdip	1 MHz
SYP6545	Plastic	1 MHz
SYC6545A	Ceramic	2 MHz
SYD6545A	Cerdip	2 MHz
SYP6545A	Plastic	2 MHz

MICRO-PROCESSORS

MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

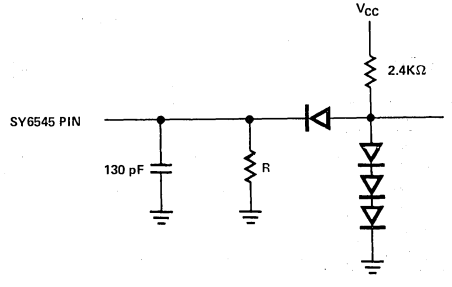
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70° C, unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.0	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–	2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	–	±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = 205μA (DB0-DB7) I_{LOAD} = 100μA (all others)	2.4	–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–	0.4	V
P_D	Power Dissipation (V_{CC} = 5.25V)	–	800	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	 – –	 10.0 12.5	 pF pF
C_{OUT}	Output Capacitance	–	10.0	pF

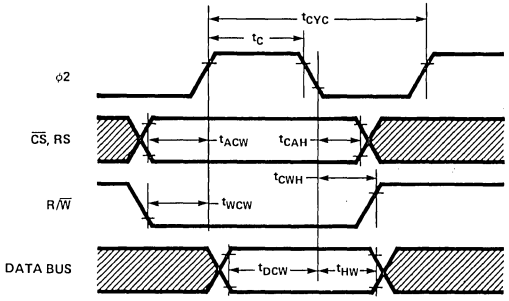
TEST LOAD



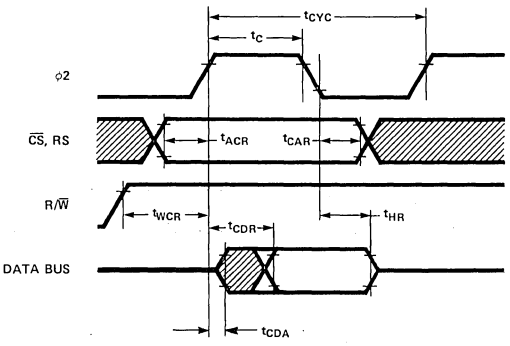
R = 11KΩ FOR DB_0-DB_7
= 24KΩ FOR ALL OTHER OUTPUTS

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACW}	Address Set-Up Time	180	–	90	–	ns
t_{CAH}	Address Hold Time	0	–	0	–	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
t_{DCW}	Data Bus Set-Up Time	300	–	150	–	ns
t_{HW}	Data Bus Hold Time	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

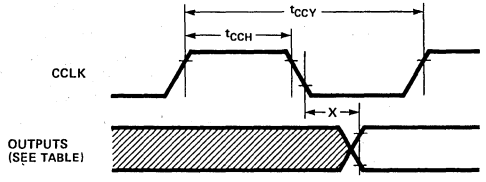
Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	φ2 Pulse Width	470	–	235	–	ns
t_{ACR}	Address Set-Up Time	180	–	90	–	ns
t_{CAR}	Address Hold Time	0	–	0	–	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CDR}	Read Access Time (Valid Data)	–	395	–	200	ns
t_{HR}	Read Hold Time	10	–	10	–	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

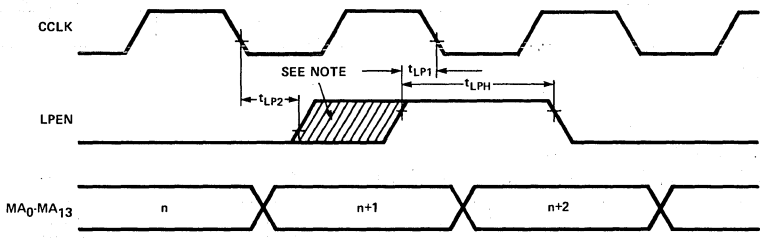
SYSTEM TIMING



Output X	Parameter
MA0-MA13	t_{MAD}
RA0-RA4	t_{RAD}
DISPLAY-ENABLE	t_{DTD}
HSYNC	t_{HSD}
VSYNC	t_{VSD}
CURSOR	t_{CDD}

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	μs
t_{CCH}	Character Clock Pulse Width	200	–	200	–	ns
t_{MAD}	MA0-MA13 Propagation Delay	–	160	–	160	ns
t_{RAD}	RA0-RA4 Propagation Delay	–	160	–	160	ns
t_{DTD}	DISPLAY ENABLE Propagation Delay	–	300	–	300	ns
t_{HSD}	HSYNC Propagation Delay	–	300	–	300	ns
t_{VSD}	VSYNC Propagation Delay	–	300	–	300	ns
t_{CDD}	CURSOR Propagation Delay	–	300	–	300	ns

LIGHT PEN STROBE TIMING



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6545 Min.	SY6545 Max.	SY6545A Min.	SY6545A Max.	Unit
t_{LPH}	LPEN Strobe Width	100	–	100	–	ns
t_{LP1}	LPEN to CCLK Delay	120	–	120	–	ns
t_{LP2}	CCLK to LPEN Delay	0	–	0	–	ns

t_r, t_f = 20 ns (max)

MPU INTERFACE SIGNAL DESCRIPTION

$\phi 2$ (Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6545. Since there is no maximum limit to the allowable $\phi 2$ cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6545 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6545; a low on the R/$\overline{W}$ pin allows a write to the SY6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6545 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6545. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6545 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6545 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6545 with only a small amount of external circuitry.

DESCRIPTION OF INTERNAL REGISTERS

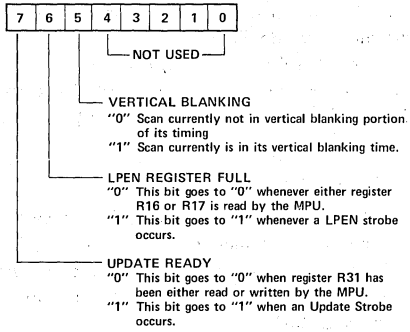
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6545 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6545 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line.

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

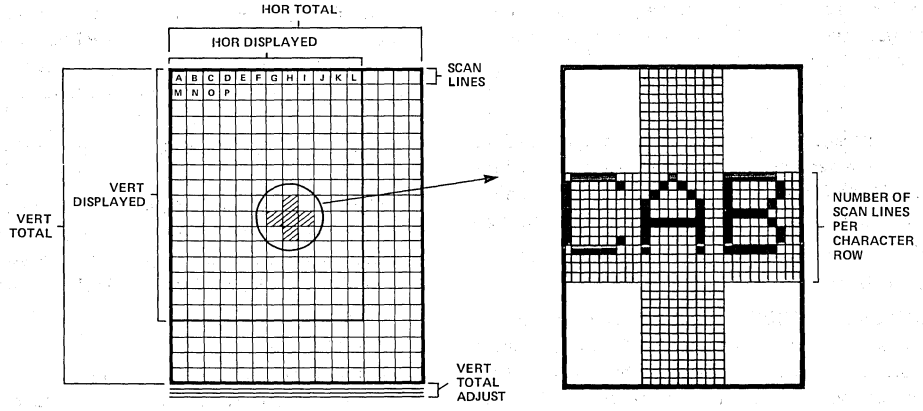


Figure 1. Video Display Format

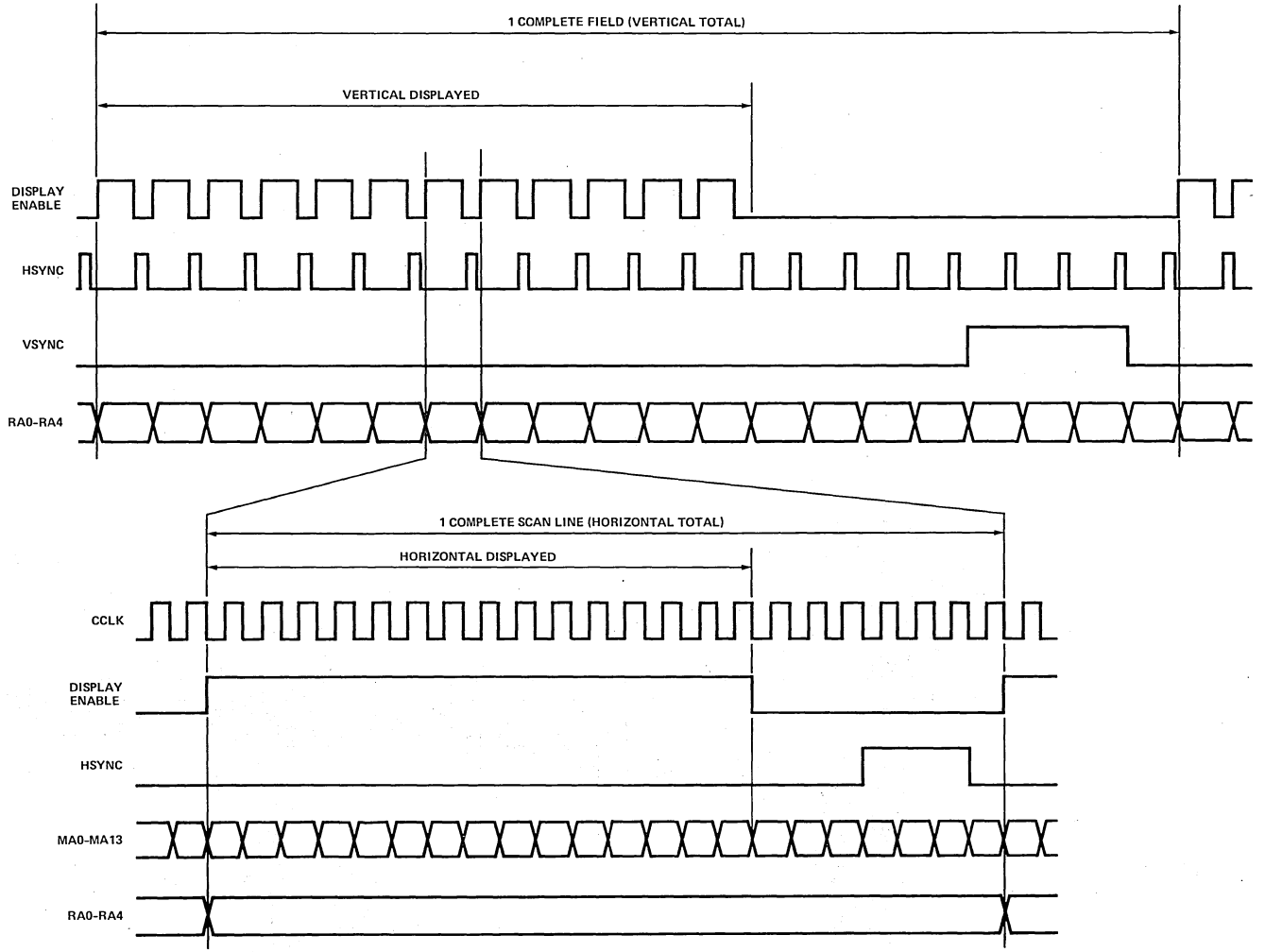
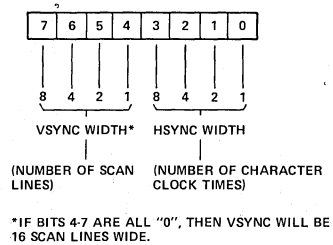


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6545 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1		–	–	–	–	–	–												
0		0	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0		0	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total	# Charac. –1		√	●	●	●	●	●	●	●	●
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		√	●	●	●	●	●	●	●	●
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total	# Charac. Row –1		√		●	●	●	●	●	●	●
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		√				●	●	●	●	●
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac. Rows		√		●	●	●	●	●	●	●
0	1	0	1	0	0	0	R8	Mode Control			√	U_1	U_0	C	D	T	RC	I_1	I_0
0	1	0	1	0	0	1	R9	Scan Line	# Scan Lines –1		√				●	●	●	●	●
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√		B_1	B_0	●	●	●	●	●
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				●	●	●	●	●
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				●	●	●	●	●
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	●	●	●	●	●	●	●	●
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				●	●	●	●	●
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	●	●	●	●	●	●	●	●
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					●	●	●	●	●
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		●	●	●	●	●	●	●	●
0	1	1	0	0	1	0	R18	Update Location (H)			√				●	●	●	●	●
0	1	1	0	0	1	1	R19	Update Location (L)			√	●	●	●	●	●	●	●	●
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: ● Designates binary bit

▨ Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for $\overline{CS}$ = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

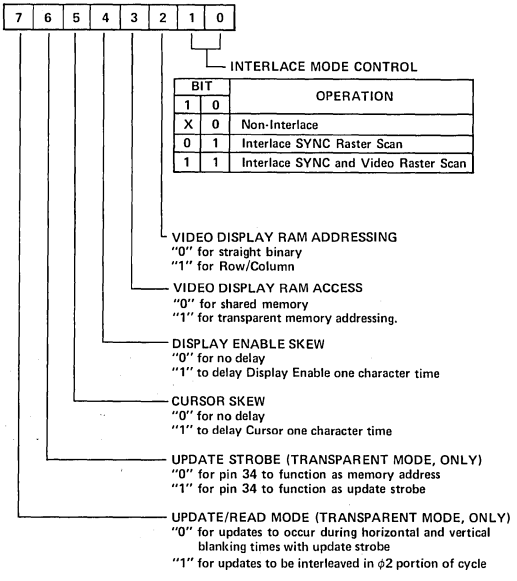
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6545 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing minus one.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

TOTAL = 90 / DISPLAY = 80 / TOTAL = 34 / DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90 / DISPLAY = 80 / COLUMN ADDRESS (MA0-MA7) / TOTAL = 34 / DISPLAY = 24 / ROW ADDRESS (MA8-MA13)

	0	1	2			77	78	79	80	81		89
0	0	1	2	---	---	77	78	79	80	81	---	89
1	256	257	258	---	---	333	334	335	336	337	---	345
2	512	513	514	---	---	589	590	591	592	593	---	601
⋮								⋮				⋮
21												
22	5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
23	5888	5889	5890	---	---	5965	5966	5967	5968	5969	---	5977
24	6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
25	6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
⋮								⋮				⋮
33	8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6545 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6545 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6545. All MPU accesses are made via the SY6545 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

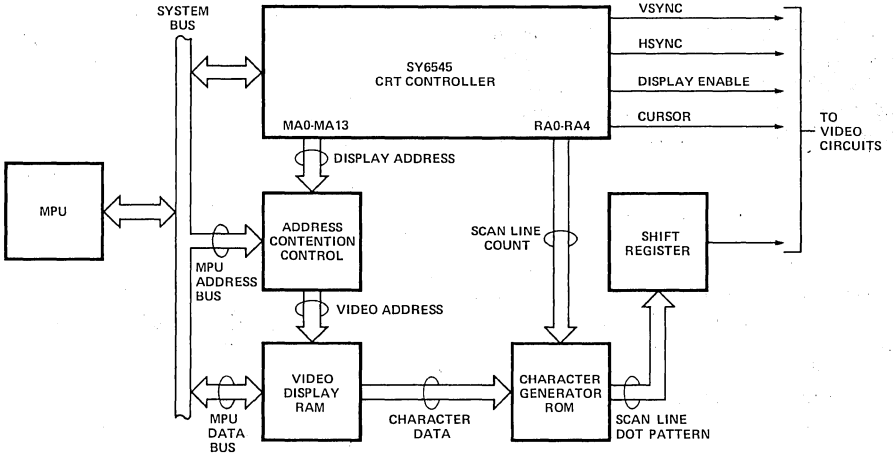


Figure 5. Shared Memory System Configuration

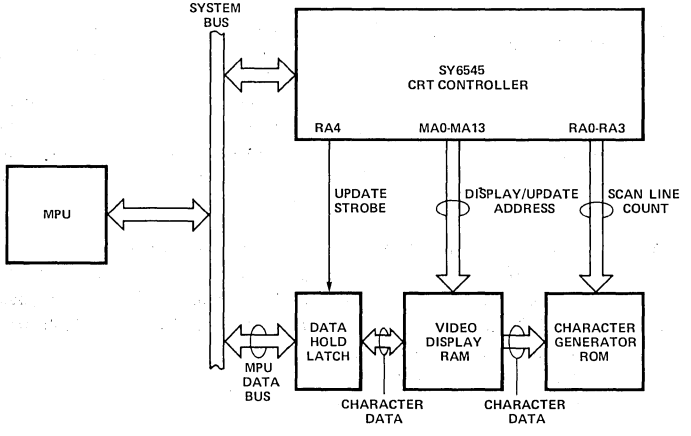


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 4, it is clear that both the SY6545 and the system MPU must be capable of addressing the video display memory. The SY6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6545 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6545 and the MPU has immediate access.

- $\phi1/\phi2$ Memory Interleaving

  This method permits both the SY6545 and the MPU access to the video display memory by time-sharing via the system $\phi1$ and $\phi2$ clocks. During the $\phi1$ portion of each cycle (the time when $\phi2$ is low), the SY6545 address outputs are gated to the video display memory. In the $\phi2$ time, the MPU address lines are switched in. In this way, both the SY6545 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

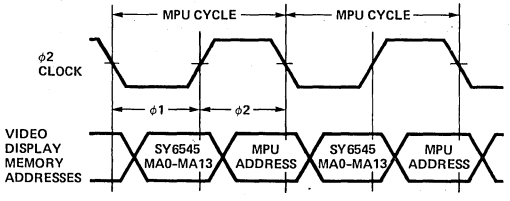


Figure 7. $\phi1/\phi2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6545. In effect, the contention is handled by the SY6545. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi1/\phi2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6545. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi2$. Figure 8 shows the timing.

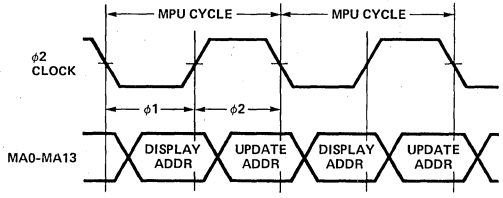


Figure 8. $\phi1/\phi2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in a related Technical Note available from Synertek.

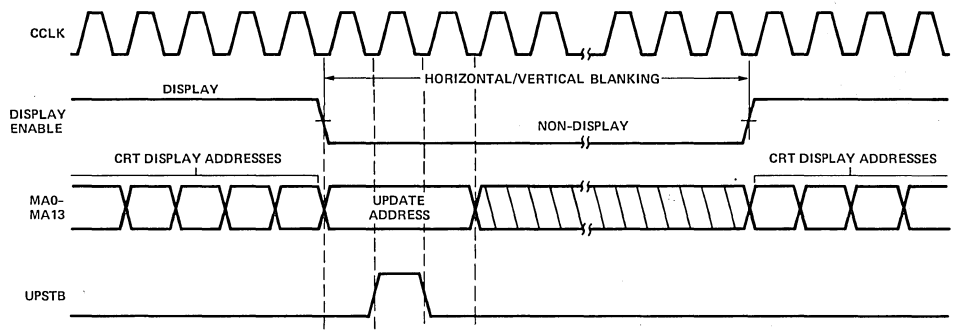


Figure 9. Retrace Update Timings

Interlace Modes

There are three raster-scan display modes (see Figure 10).

a) Non-Interlaced Mode. In this mode each scan line is refreshed at the vertical field rate (50 or 60 Hz).

In the interlaced scan modes, even and odd fields alternate to generate frames. The horizontal and vertical timing relationship causes the scan lines in the odd fields to be displaced from those in the even fields. The two additional raster-scan display modes pertain to interlaced scans.

b) Interlace-Sync Mode. This mode is used when the same information is to be displayed in both odd and even fields. Enhanced readability results because the spaces between adjacent rows are filled and a higher quality character is displayed. This is achieved with only a slight alteration in the device operation: in alternate fields, the position of the VSYNC signal is delayed by ½ of a scan line time. This is illustrated in Figure 11 and is the only difference in the SY6545 operation in this mode.

c) Interlaced Sync and Video Mode. This mode is used to double the character density on the screen by displaying the even lines in even fields and the odd lines in odd fields. As in the Interlace-Sync mode, the VSYNC position is delayed in alternate display fields. In addition, the address generation is altered. Figure 12 illustrates the timing.

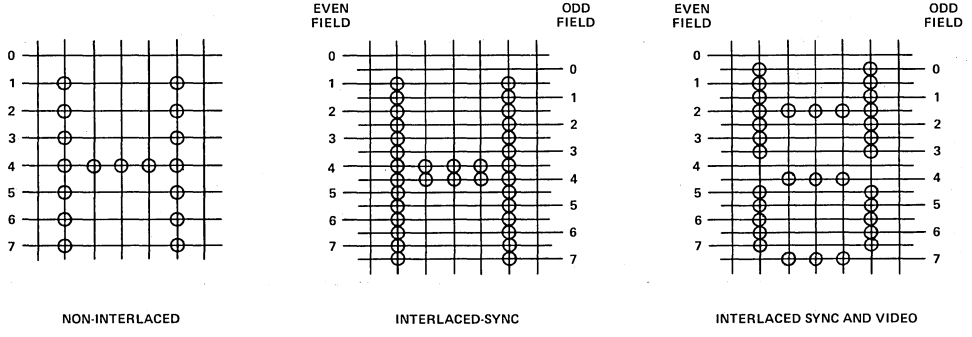


Figure 10. Comparison of Display Modes.

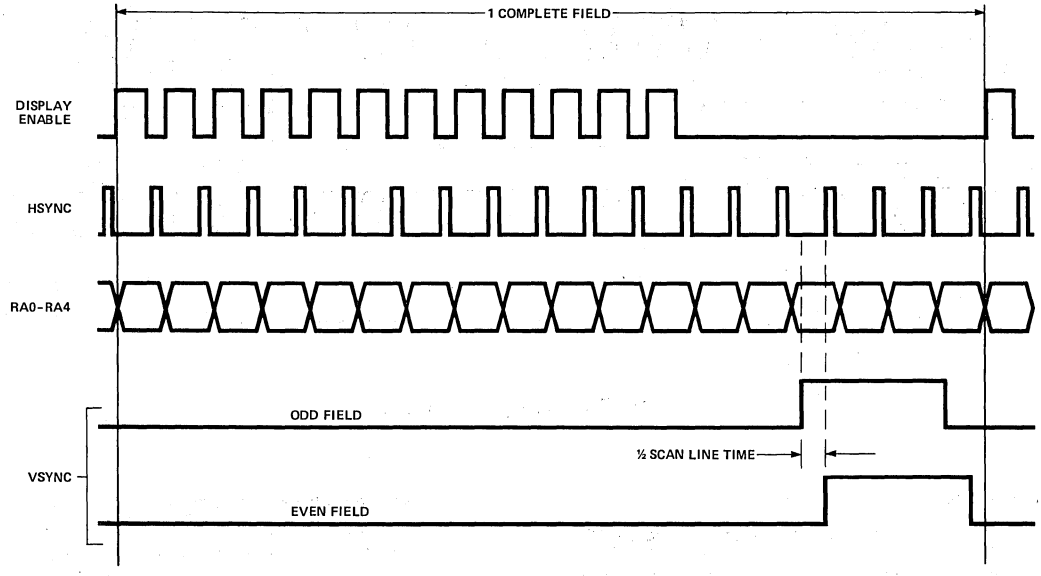


Figure 11. Interlace-Sync Mode Timing

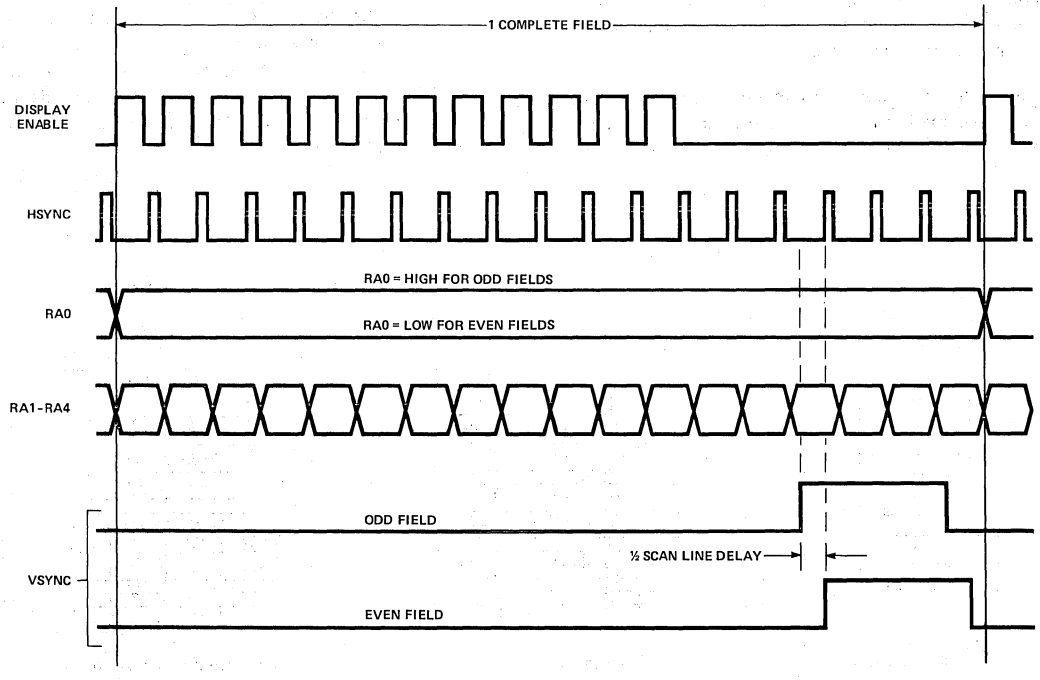


Figure 12. Interlace-Sync-and-Video Mode Timing

Some restrictions on interlace modes of operation are:

a) The Horizontal Total Character count (register R0) must be odd, in order to represent an even number of character times.

b) For Interlaced Sync and Video mode, only, the following registers must be programmed in a non-standard fashion:
   - R4 (Vertical Total) must be programmed to one-half the actual number desired, minus one. For example, for a total of 24 characters high, R4 must contain 11 (decimal).
   - R6 (Vertical Displayed) must be programmed to one-half the actual number desired. For example, for 16 displayed characters high, R6 must contain 8 (decimal).
   - R7 (Vertical Sync Position) must be programmed to one-half the actual number desired.
   - R9 # of scan lines per character row must be odd (i.e.) even number of scan lines)

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 13 illustrates the effect of the delays.

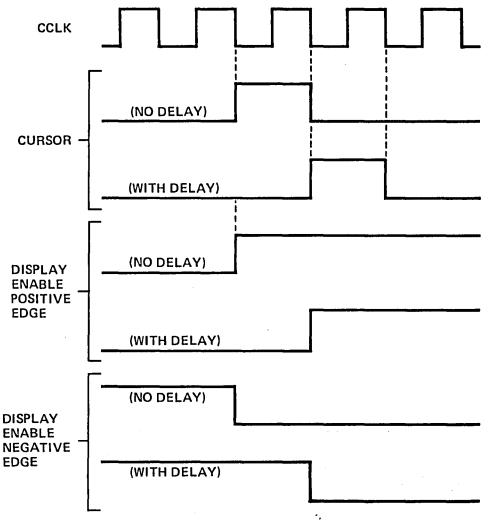


Figure 13. Cursor and Display Enable Skew

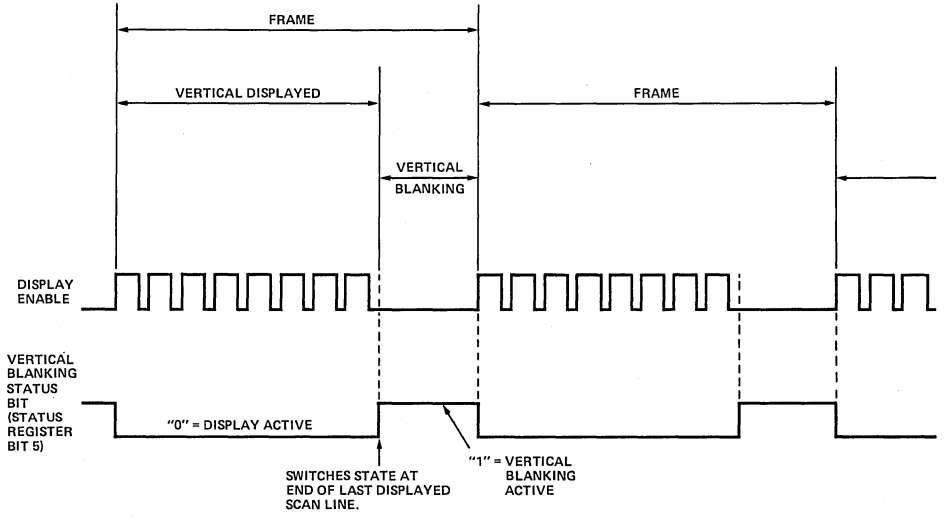


Figure 14. Operation of Vertical Blanking Status Bit

CRT Controller

SY6545-1

MICROPROCESSOR PRODUCTS

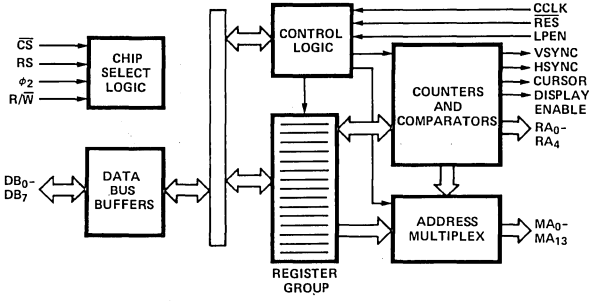
SYNERTEK
A SUBSIDIARY OF HONEYWELL

- Single +5 volt (±5%) power supply.
- Alphanumeric and limited graphics capabilities.
- Fully programmable display (rows, columns, blanking, etc.).
- Non-interlaced scan.
- 50/60 Hz operation.
- Fully programmable cursor.
- External light pen capability.
- Capable of addressing up to 16K character Video Display RAM.
- No DMA required.
- Pin-compatible with MC6845.
- Row/Column or straight-binary addressing for Video Display RAM.
- Internal status register.
- Video Display RAM may be configured as part of microprocessor memory field or independently slaved to 6545 (Transparent Addressing).

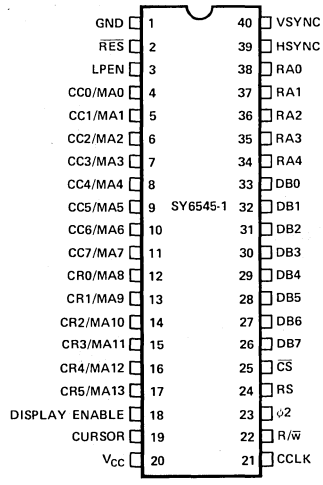
MICRO-PROCESSORS

The SY6545-1 is a CRT Controller intended to provide capability for interfacing the 6500/6800 microprocessor families to CRT or TV-type raster scan displays. A unique feature is the inclusion of several modes of operation, so that the system designer can configure the system with a wide assortment of techniques.

INTERFACE DIAGRAM



PIN DESIGNATION



ORDERING INFORMATION

Part Number	Package	
SYP6545-1	Plastic	1 MHz
SYC6545-1	Ceramic	1 MHz
SYD6545-1	Cerdip	1 MHz
SYP6545A-1	Plastic	2 MHz
SYC6545A-1	Ceramic	2 MHz
SYD6545A-1	Cerdip	2 MHz

MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.3V to +7.0V
Input/Output Voltage, V_{IN}	-0.3V to +7.0V
Operating Temperature, T_{OP}	0°C to 70°C
Storage Temperature, T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

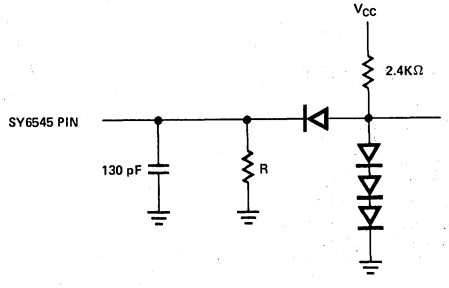
COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, GND = 0V, T_A = 0 - 70°C, unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Unit
V_{IH}	Input High Voltage	2.4	V_{CC}	V
V_{IL}	Input Low Voltage	-0.3	0.4	V
I_{IN}	Input Leakage (ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	–	2.5	μA
I_{TSI}	Three-State Input Leakage (DB0-DB7) V_{IN} = 0.4 to 2.4V	–	±10.0	μA
V_{OH}	Output High Voltage I_{LOAD} = -205μA (DB0-DB7) I_{LOAD} = -100μA (all others)	2.4	–	V
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mA	–	0.4	V
P_D	Power Dissipation (T_A = 25°C), V_{CC} = 5.25V	–	900	mW
C_{IN}	Input Capacitance ϕ2, R/$\overline{w}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK DB0-DB7	– –	10.0 12.5	pF pF
C_{OUT}	Output Capacitance	–	10.0	pF

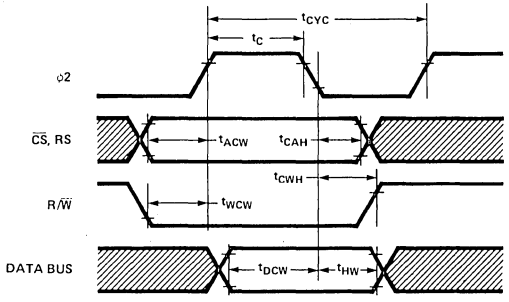
TEST LOAD



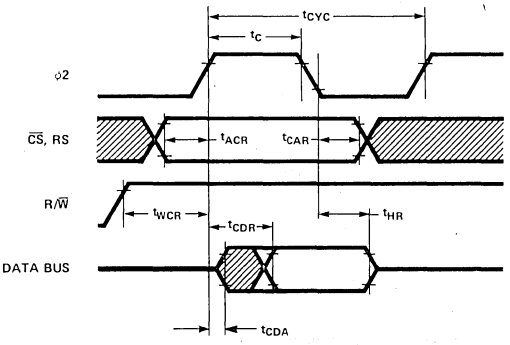
R = 11KΩ FOR DB_0-DB_7
= 24KΩ FOR ALL OTHER OUTPUTS

MPU BUS INTERFACE CHARACTERISTICS

WRITE CYCLE



READ CYCLE



WRITE TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

Symbol	Characteristic	SY6545-1		SY6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	ϕ2 Pulse Width	440	–	200	–	ns
t_{ACW}	Address Set-Up Time	180	–	90	–	ns
t_{CAH}	Address Hold Time	0	–	0	–	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	–	0	–	ns
t_{DCW}	Data Bus Set-Up Time	265	–	100	–	ns
t_{HW}	Data Bus Hold Time	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0–70°C, unless otherwise noted)

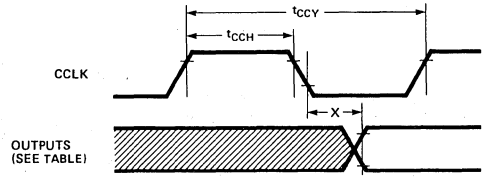
Symbol	Characteristic	SY6545-1		SY6545A-1		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	–	0.5	–	μs
t_C	ϕ2 Pulse Width	440	–	200	–	ns
t_{ACR}	Address Set-Up Time	180	–	90	–	ns
t_{CAR}	Address Hold Time	0	–	0	–	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	180	–	90	–	ns
t_{CDR}	Read Access Time (Valid Data)	–	340	–	150	ns
t_{HR}	Read Hold Time	10	–	10	–	ns
t_{CDA}	Data Bus Active Time (Invalid Data)	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

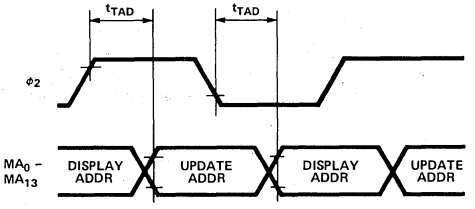
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

SYSTEM TIMING

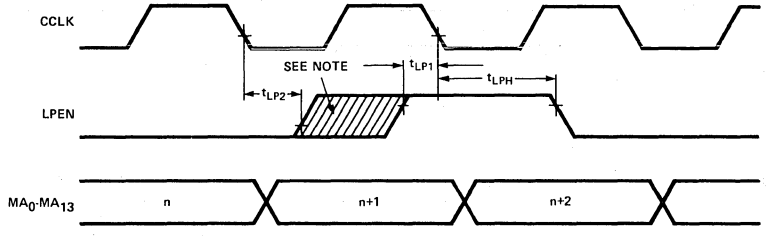


TRANSPARENT ADDRESSING (ϕ_1/ϕ_2 INTERLEAVING)



Symbol	Characteristic	SY6545-1 Min.	SY6545-1 Max.	SY6545A-1 Min.	SY6545A-1 Max.	Unit
t_{CCY}	Character Clock Cycle Time	0.40	40	0.40	40	μs
t_{CCH}	Character Clock Pulse Width	200	–	200	–	ns
(X)t_{MAD}	MA0-MA13 Propagation Delay	–	300	–	300	ns
(X)t_{RAD}	RA0-RA4 Propagation Delay	–	300	–	300	ns
(X)t_{DTD}	DISPLAY ENABLE Propagation Delay	–	450	–	450	ns
(X)t_{HSD}	HSYNC Propagation Delay	–	450	–	450	ns
(X)t_{VSD}	VSYNC Propagation Delay	–	450	–	450	ns
(X)t_{CDD}	CURSOR Propagation Delay	–	450	–	450	ns
t_{TAD}	MA0-MA13 Switching Delay	–	200	–	200	ns

LIGHT PEN STROBE TIMING



NOTE: "Safe" time position for LPEN positive edge to cause address n+2 to load into Light Pen Register. t_{LP2} and t_{LP1} are time positions causing uncertain results.

Symbol	Characteristic	SY6545-1 Min.	SY6545-1 Max.	SY6545A-1 Min.	SY6545A-1 Max.	Unit
t_{LPH}	LPEN Hold Time	150	–	150	–	ns
t_{LP1}	LPEN Setup Time	20	–	20	–	ns
t_{LP2}	CCLK to LPEN Delay	0	–	0	–	ns

t_r, t_f = 20 ns (max)

MPU INTERFACE SIGNAL DESCRIPTION

$\phi 2$ (Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6545. Since there is no maximum limit to the allowable $\phi 2$ cycle time, it is not necessary for it to be a continuous clock. This capability permits the SY6545 to be easily interfaced to non-6500-compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6545; a low on the R/$\overline{W}$ pin allows a write to the SY6545.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The SY6545 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes into the Address Register and reads from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

DB_0-DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6545. These lines are bi-directional and are normally high-impedance except during read cycles when the chip is selected.

VIDEO INTERFACE SIGNAL DESCRIPTION

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active-high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC position and width are both fully programmable.

DISPLAY ENABLE

The DISPLAY ENABLE signal is an active-high output and is used to indicate when the SY6545 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed characters are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE may be delayed by one character time by setting bit 4 of R8 to a "1".

CURSOR

The CURSOR signal is an active-high output and is used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The CURSOR position may be delayed by one character time by setting bit 5 of R8 to a "1".

LPEN

The LPEN signal is an edge-sensitive input and is used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency.

MEMORY ADDRESS SIGNAL DESCRIPTION

MA0-MA13 (Video Display RAM Address Lines)

These signals are active-high outputs and are used to address the Video Display RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

- Binary
  Characters are stored in successive memory locations. Thus, the software must be developed so that row and column co-ordinates are translated to sequentially-numbered addresses for video display memory operations.
- Row/Column
  In this mode, MA0-MA7 function as column addresses CC0-CC7, and MA8-MA13, as row addresses CR0-CR5. In this case, the software may handle addresses in terms of row and column locations, but additional

address compression circuits are needed to convert CC0-CC7 and CR0-CR5 into a memory-efficient binary scheme.

RA0-RA4 (Raster Address Lines)

These signals are active-high outputs and are used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

The high-order line, RA4, is unique in that it can also function as a strobe output pin when the SY6545 is programmed to operate in the "Transparent Address Mode". In this case the strobe is an active-high output and is true at the time the Video Display RAM update address is gated on to the address lines, MA0-MA13. In this way, updates and readouts of the Video Display RAM can be made under control of the SY6545 with only a small amount of external circuitry.

DESCRIPTION OF INTERNAL REGISTERS

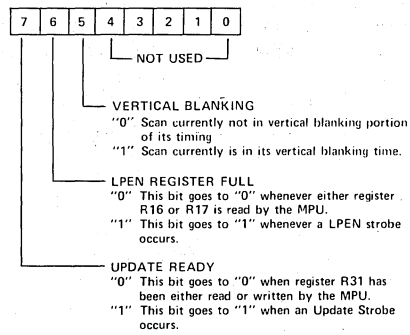
Figure 1 illustrates the format of a typical video display and is necessary to understand the functions of the various SY6545 internal registers. Figure 2 illustrates vertical and horizontal timing. Figure 3 summarizes the internal registers and indicates their address selection and read/write capabilities.

Address Register

This is a 5-bit register which is used as a "pointer" to direct SY6545 data transfers to and from the system MPU. Its contents is the number of the desired register (0-31). When RS is low, then this register may be loaded; when RS is high, then the register selected is the one whose identity is stored in this register.

Status Register

This 3-bit register is used to monitor the status of the CRTC, as follows:



Horizontal Total (R0)

This 8-bit register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

Horizontal Displayed (R1)

This 8-bit register contains the number of displayed characters per horizontal line .

Horizontal Sync Position (R2)

This 8-bit register contains the position of the HSYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left-to-right location of the displayed text on the video screen. In this way, the side margins are adjusted.

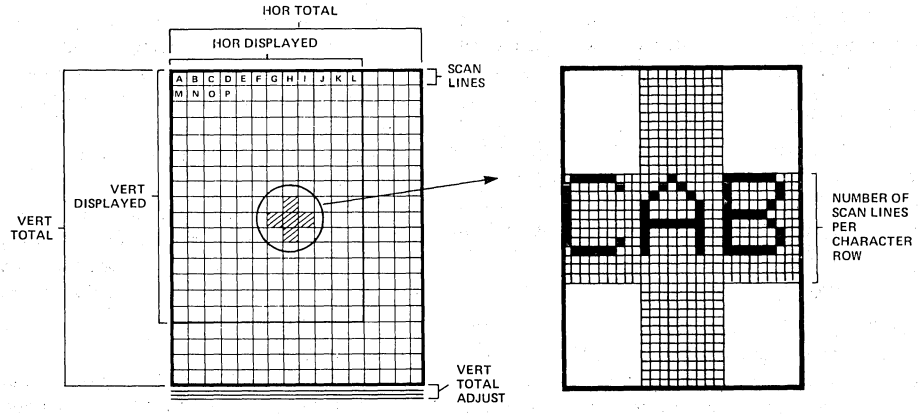


Figure 1. Video Display Format

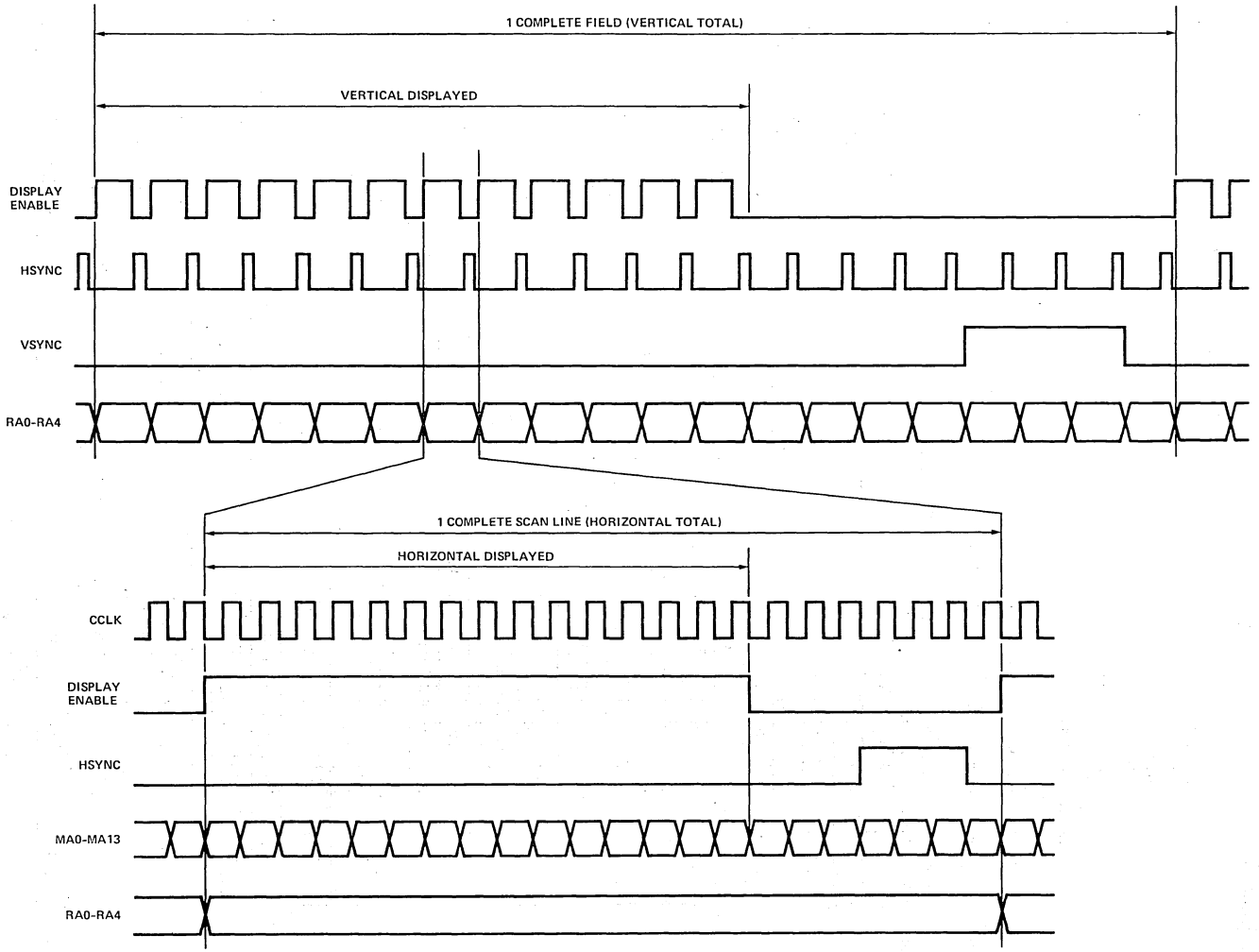
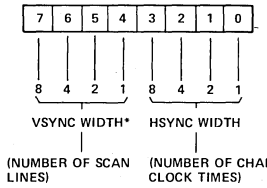


Figure 2. Vertical and Horizontal Timing

Horizontal and Vertical SYNC Widths (R3)

This 8-bit register contains the widths of both HSYNC and VSYNC, as follows:



*IF BITS 4-7 ARE ALL "0", THEN VSYNC WILL BE 16 SCAN LINES WIDE.

Control of these parameters allows the SY6545 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one-shot timing.

Vertical Total (R4)

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

$\overline{CS}$	RS	Address Reg. 4	3	2	1	0	Reg. No.	Register Name	Stored Info.	RD	WR	Register Bit 7	6	5	4	3	2	1	0
1	–	–	–	–	–	–	–												
0	0	–	–	–	–	–	–	Address Reg.	Reg. No.		√				A_4	A_3	A_2	A_1	A_0
0	0	–	–	–	–	–	–	Status Reg.		√		U	L	V					
0	1	0	0	0	0	0	R0	Horiz. Total - 1	# Charac.		√	o	o	o	o	o	o	o	o
0	1	0	0	0	0	1	R1	Horiz. Displayed	# Charac.		√	o	o	o	o	o	o	o	o
0	1	0	0	0	1	0	R2	Horiz. Sync Position	# Charac.		√	o	o	o	o	o	o	o	o
0	1	0	0	0	1	1	R3	VSYNC, HSYNC Widths	# Scan Lines and # Char. Times		√	V_3	V_2	V_1	V_0	H_3	H_2	H_1	H_0
0	1	0	0	1	0	0	R4	Vert. Total - 1	# Charac. Row		√		o	o	o	o	o	o	o
0	1	0	0	1	0	1	R5	Vert. Total Adjust	# Scan Lines		√				o	o	o	o	o
0	1	0	0	1	1	0	R6	Vert. Displayed	# Charac. Rows		√		o	o	o	o	o	o	o
0	1	0	0	1	1	1	R7	Vert. Sync Position	# Charac.Rows		√		o	o	o	o	o	o	o
0	1	0	1	0	0	0	R8	Mode Control			√	o	o	o	o	o	o	o	o
0	1	0	1	0	0	1	R9	Scan Lines - 1	# Scan Lines		√				o	o	o	o	o
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line No.		√			B_1	B_0	o	o	o	o
0	1	0	1	0	1	1	R11	Cursor End	Scan Line No.		√				e	e	e	e	e
0	1	0	1	1	0	0	R12	Display Start Addr (H)			√				o	o	o	o	o
0	1	0	1	1	0	1	R13	Display Start Addr (L)			√	o	o	o	o	o	o	o	o
0	1	0	1	1	1	0	R14	Cursor Position (H)		√	√				o	o	o	o	o
0	1	0	1	1	1	1	R15	Cursor Position (L)		√	√	o	o	o	o	o	o	o	o
0	1	1	0	0	0	0	R16	Light Pen Reg (H)		√					o	o	o	o	o
0	1	1	0	0	0	1	R17	Light Pen Reg (L)		√		o	o	o	o	o	o	o	o
0	1	1	0	0	1	0	R18	Update Address Reg (H)			√				o	o	o	o	o
0	1	1	0	0	1	1	R19	Update Address Reg (L)			√	o	o	o	o	o	o	o	o
0	1	1	1	1	1	1	R31	Dummy Location											

Notes: o Designates binary bit

Designates unused bit. Reading this bit is always "0", except for R31, which does not drive the data bus at all, and for CS = "1" which operates likewise.

Figure 3. Internal Register Summary

Vertical Total Adjust (R5)

The Vertical Total Adjust Register is a 5-bit write only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

Vertical Displayed (R6)

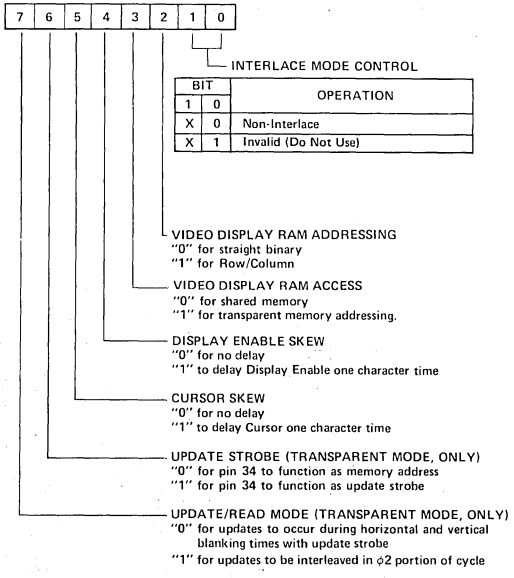
This 7-bit register contains the number of displayed character rows in each frame. In this way, the vertical size of the displayed text is determined.

Vertical Sync Position (R7)

This 7-bit register is used to select the character row time at which the VSYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

Mode Control (R8)

This register is used to select the operating modes of the SY6545 and is outlined as follows:



Scan Line (R9)

This 5-bit register contains the number of scan lines per character row, including spacing, minus 1.

Cursor Start (R10) and Cursor End (R11)

These 5-bit registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor mode, as follows:

BIT		CURSOR MODE
6	5	
0	0	No Blinking
0	1	No Cursor
1	0	Blink at 1/16 field rate
1	1	Blink at 1/32 field rate

Note that the ability to program both the start and end scan line for the cursor enables either block cursor or underline to be accommodated. Registers R14 and R15 are used to control the character position of the cursor over the entire 16K address field.

Display Start Address High (R12) and Low (R13)

These registers together comprise a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the SY6545 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

Cursor Position High (R14) and Low (R15)

These registers together comprise a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

LPEN High (R16) and Low (R17)

These registers together comprise a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

Update Address High (R18) and Low (R19)

These registers together comprise a 14-bit register whose contents is the memory address at which the next read or update will occur (for transparent address mode, only). Whenever a read/update occurs, the update location automatically increments to allow for fast updates or readouts of consecutive character locations. This is described elsewhere in this document.

Dummy Location (R31)

This register does not store any data, but is required to detect when transparent addressing updates occur. This is necessary to increment the Update Address Register and to set the Update Ready bit in the status register.

DETAILED DESCRIPTION OF OPERATION

Register Formats

Register pairs R12/R13, R14/R15, R16/R17, and R18/R19 are formatted in one of two ways:

1. Straight binary if register R8, bit 2 is a "0".
2. Row/Column if register R8, bit 2 is a "1". In this case the low byte is the Character Column and the high byte is the Character Row.

Figure 4 illustrates the address sequence for the video display control for each mode.

Note from Figure 4 that the straight-binary mode has the advantage that all display memory addresses are stored in a continuous memory block, starting with address 0 and ending at 1919. The disadvantage with this method is that, if it is desired to change a displayed character location, the row and column identity of the location must be converted to its binary address before the memory may be written. The row/column mode, on the other hand, does not need to undergo this conversion. However, memory is not used as efficiently, since the memory addresses are not continuous, but gaps exist. This requires that the system be equipped with more memory than is actually used and this extra memory is wasted. Alternatively, address compression logic may be employed to translate the row/column format into a continuous address block.

In this way, the user may select whichever mode is best for the given application. The trade-offs between the modes are software versus hardware. Straight-binary mode minimizes hardware requirements and row/column requires minimum software.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	---	---	77	78	79	80	81	---	89
80	81	82	---	---	157	158	159	160	161	---	169
160	161	162	---	---	237	238	239	240	241	---	249
⋮							⋮				⋮
⋮							⋮				⋮
⋮							⋮				⋮
1760	1761	1762	---	---	1837	1838	1839	1840	1841	---	1849
1840	1841	1842	---	---	1917	1918	1919	1920	1921	---	1929
1920	1921	1922	---	---	1997	1998	1999	2000	2001	---	2009
2000	2001	2002	---	---	2077	2078	2079	2080	2081	---	2089
⋮							⋮				⋮
2640	2641	2642	---	---	2717	2718	2719	2720	2721	---	2729

STRAIGHT BINARY ADDRESSING SEQUENCE

TOTAL = 90

DISPLAY = 80

COLUMN ADDRESS (MA0-MA7)

TOTAL = 34

DISPLAY = 24

ROW ADDRESS (MA8-MA13)

	0	1	2	---	---	77	78	79	80	81	---	89
0	0	1	2	---	---	77	78	79	80	81	---	89
1	256	257	258	---	---	333	334	335	336	337	---	345
2	512	513	514	---	---	589	590	591	592	593	---	601
⋮	⋮							⋮				⋮
⋮	⋮							⋮				⋮
21	⋮							⋮				⋮
22	5632	5633	5634	---	---	5709	5710	5711	5712	5713	---	5721
23	5888	5889	5890	---	---	5965	5966	5967	5968	5969	---	5977
24	6144	6145	6146	---	---	6221	6222	6223	6224	6225	---	6233
25	6400	6401	6402	---	---	6477	6478	6479	6480	6481	---	6489
⋮								⋮				⋮
33	8448	8449	8450	---	---	8525	8526	8527	8528	8529	---	8537

ROW/COLUMN ADDRESSING SEQUENCE

Figure 4. Display Address Sequences (with Start Address = 0) for 80 x 24 Example

Video Display RAM Addressing

There are two modes of addressing for the video display memory:

1. Shared Memory
   In this mode the memory is shared between the MPU address bus and the SY6545 address bus. For this case, memory contention must be resolved by means of external timing and control circuits. Both the MPU and the SY6545 must have access to the video display RAM and the contention circuits must resolve this multiple access requirement. Figure 5 illustrates the system configuration.
2. Transparent Memory Addressing
   For this mode, the display RAM is not directly accessible by the MPU, but is controlled entirely by the SY6545. All MPU accesses are made via the SY6545 and a small amount of external circuits. Figure 6 shows the system configuration for this approach.

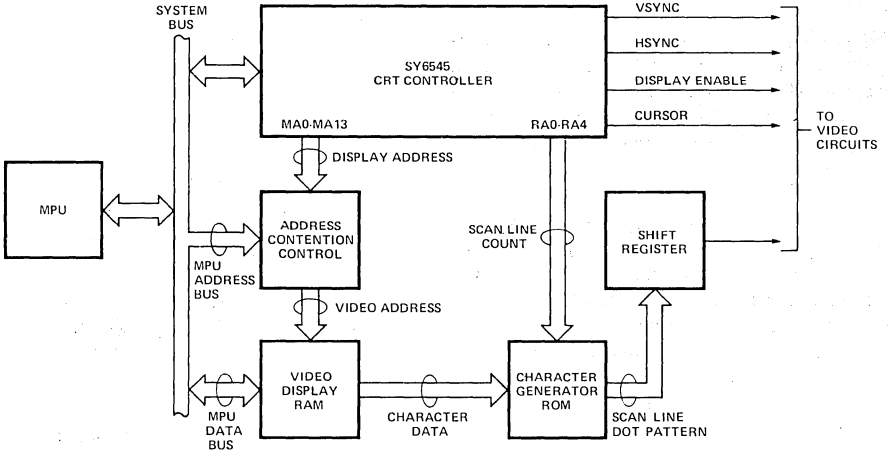


Figure 5. Shared Memory System Configuration

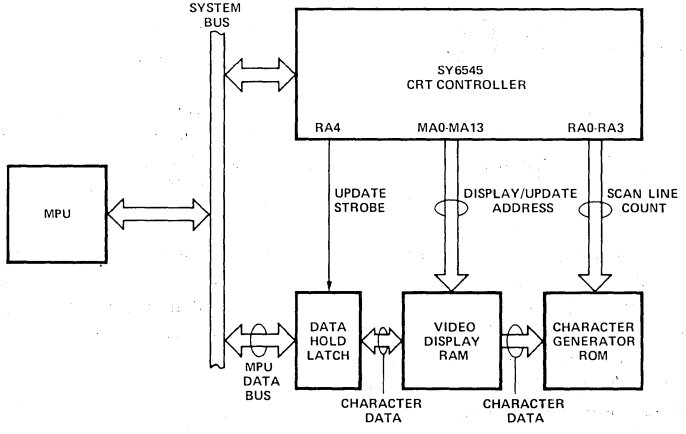


Figure 6. Transparent Memory Addressing System Configuration (Data Hold Latch needed for Horizontal/Vertical Blanking updates, only).

Memory Contention Schemes for Shared Memory Addressing

From the diagram of Figure 5, it is clear that both the SY6545 and the system MPU must be capable of addressing the video display memory. The SY6545 repetitively fetches character information to generate the video signals in order to keep the screen display active. The MPU occasionally accesses the memory to change the displayed information or to read out current data characters. Three ways of resolving this dual-contention requirement are apparent:

- MPU Priority

  In this technique, the address lines to the video display memory are normally driven by the SY6545 unless the MPU needs access, in which case the MPU addresses immediately override those from the SY6545 and the MPU has immediate access.

- $\phi 1/\phi 2$ Memory Interleaving

  This method permits both the SY6545 and the MPU access to the video display memory by time-sharing via the system $\phi 1$ and $\phi 2$ clocks. During the $\phi 1$ portion of each cycle (the time when $\phi 2$ is low), the SY6545 address outputs are gated to the video display memory. In the $\phi 2$ time, the MPU address lines are switched in. In this way, both the SY6545 and the MPU have unimpeded access to the memory. Figure 7 illustrates the timings.

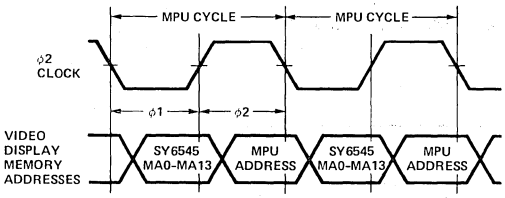


Figure 7. $\phi 1/\phi 2$ Interleaving

- Vertical Blanking

  With this approach, the address circuitry is identical to the case for MPU Priority updates. The only difference is that the Vertical Retrace status bit (bit 5 of the Status Register) is used by the MPU so that access to the video display memory is only made during vertical blanking time (when bit 5 is a "1"). In this way, no visible screen perturbations result.

Transparent Memory Addressing

In this mode of operation, the video display memory address lines are not switched by contention circuits, but are generated by the SY6545. In effect, the contention is handled by the SY6545. As a result, the schemes for accomplishing MPU memory access are different:

- $\phi 1/\phi 2$ Interleaving

  This mode is similar to the Interleave mode used with shared memory. In this case, however, the $\phi 2$ address is generated from the Update Address Register (Registers R18 and R19) in the SY6545. Thus, the MPU must first load the address to be accessed into R18/R19 and then this address is always gated onto the MA lines during $\phi 2$. Figure 8 shows the timing.

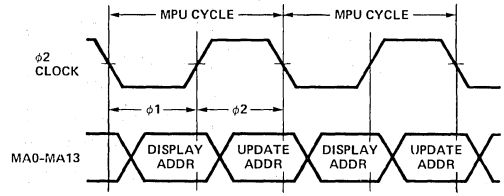


Figure 8. $\phi 1/\phi 2$ Transparent Interleaving

- Horizontal/Vertical Blanking

  In this mode, the Update Address is loaded by the MPU, but is only gated onto the MA lines during horizontal or vertical blank times, so memory accesses do not interfere with the display appearance. To signal when the update address is on the MA lines, an update strobe (STB) is provided as an alternate function of pin 34. Data hold latches are necessary to temporarily retain the character to be stored until the retrace time occurs. In this way, the system MPU is not halted waiting for the blanking time to arrive. Figure 9 illustrates the address and strobe timing for this mode.

Transparent address modes are quite complex and offer significant advantages in system implementation. The details of their application are covered thoroughly in related Technical Notes available from Synertek.

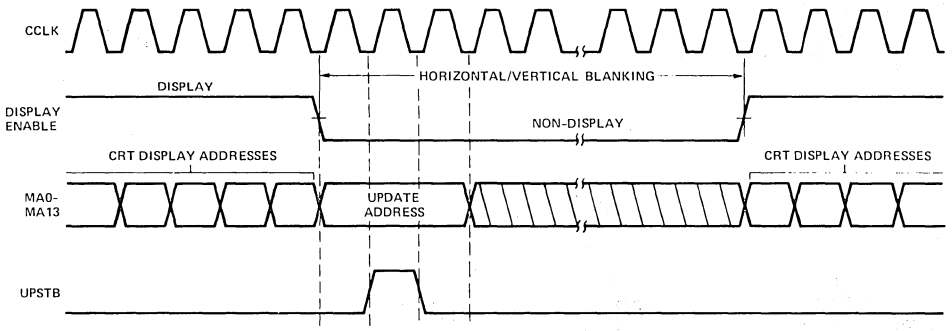


Figure 9. Retrace Update Timings

Cursor and Display Enable Skew Control

Bits 4 and 5 of the Mode Control register (R8) are used to delay the Display Enable and Cursor outputs, respectively. Figure 10 illustrates the effect of the delays.

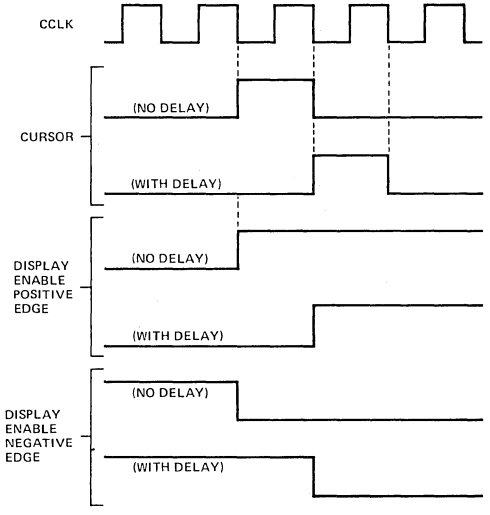


Figure 10. Cursor and Display Enable Skew

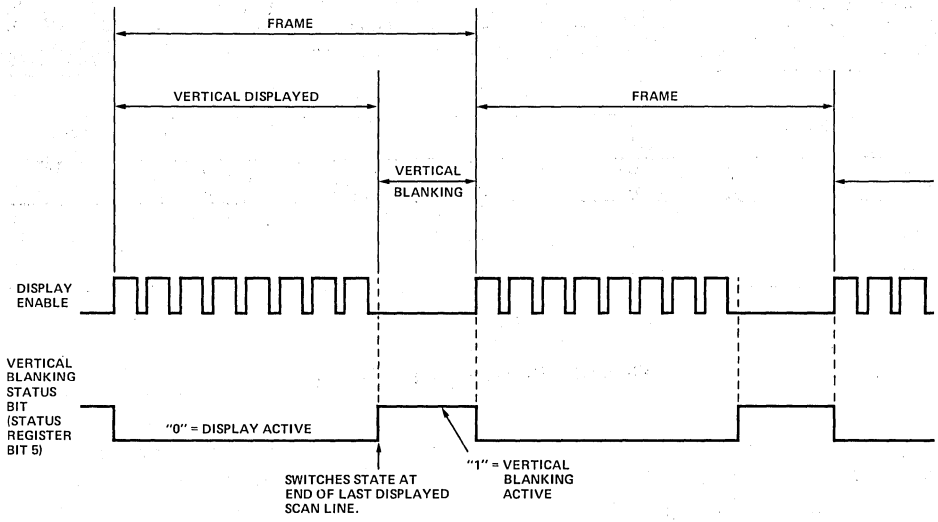


Figure 11. Operation of Vertical Blanking Status Bit

Asynchronous Communication Interface Adapter

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SY6551

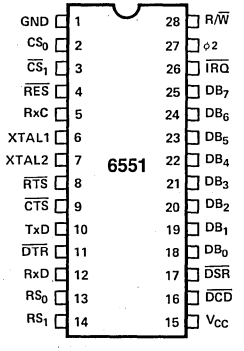
MICROPROCESSOR PRODUCTS

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

The SY6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

MICRO-PROCESSORS

PIN CONFIGURATION



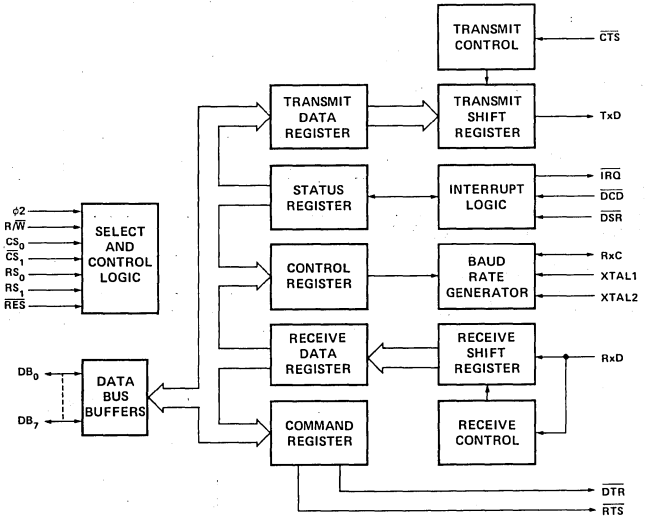


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Package	Clock Rate
SYC6551	Ceramic	1 MHz
SYD6551	Cerdip	1 MHz
SYP6551	Plastic	1 MHz
SYC6551A	Ceramic	2 MHz
SYD6551A	Ceramic	2 MHz
SYP6551A	Plastic	2 MHz

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temperature	T_{OP}	0°C to 70°C
Storage Temperature	T_{STG}	-55°C to 150°C

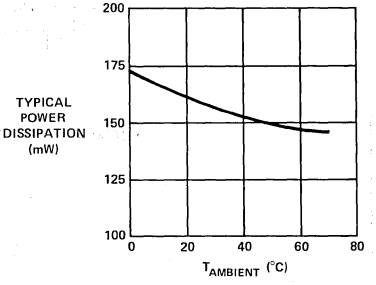
All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V ($\phi 2$, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = -100μA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance ($\phi 2$)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	170	300	mW

POWER DISSIPATION vs TEMPERATURE



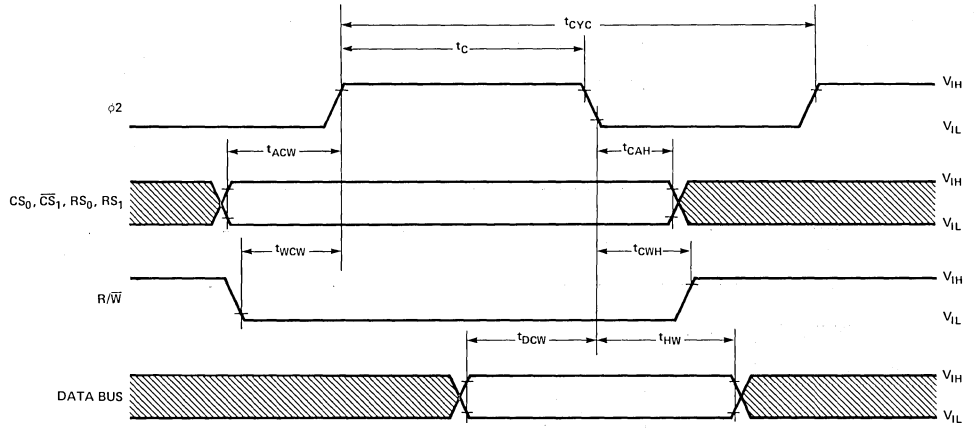


Figure 2. Write Timing Characteristics

WRITE CYCLE (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
$\phi 2$ Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

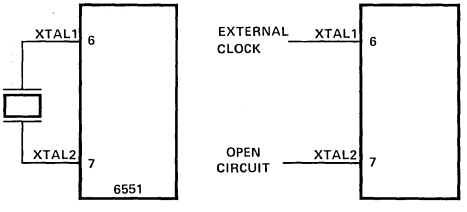
(t_r and t_f = 10 to 30 ns)

CRYSTAL SPECIFICATION

1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   - a. Frequency (MHz) 1.8432
   - b. Frequency tolerance (±%) 0.02
   - c. Resonance mode Series
   - d. Equivalent resistance (ohm) 400 max.
   - e. Drive level mW 2
   - f. Shunt capacitance pF 7 max.
   - g. Oscillation mode Fundamental

No other external components should be in the crystal circuit

CLOCK GENERATION



INTERNAL CLOCK EXTERNAL CLOCK

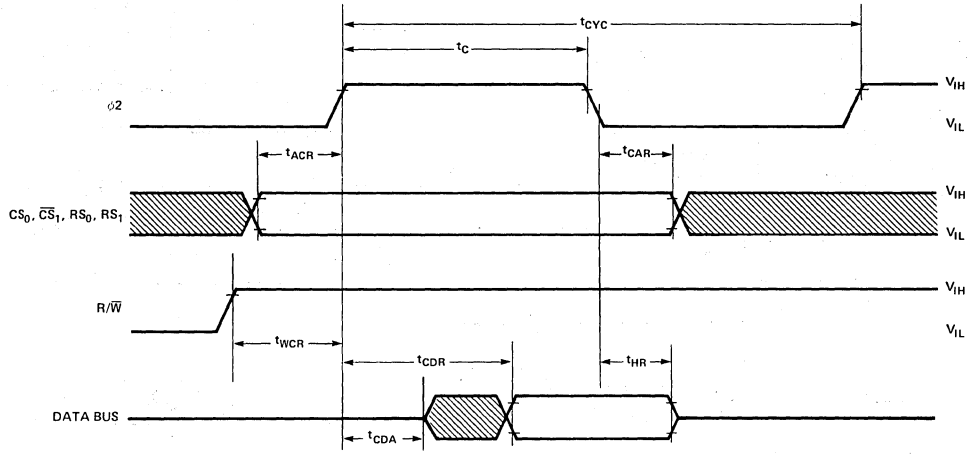
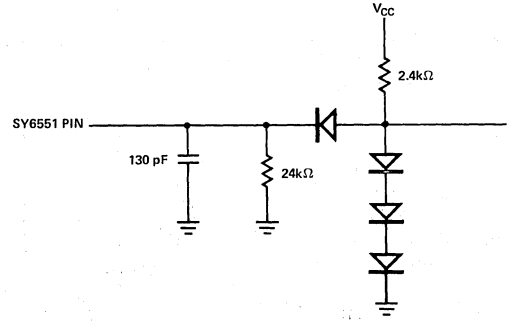


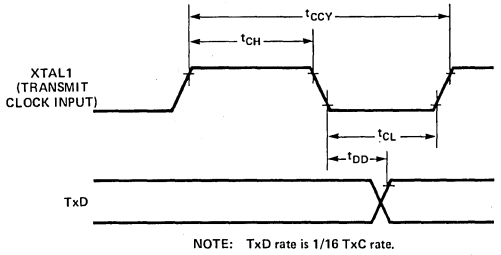
Figure 3. Read Timing Characteristics

READ CYCLE (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (ϕ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns



TEST LOAD FOR DATA BUS (DB_0 – DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS OUTPUTS



NOTE: TxD rate is 1/16 TxC rate.

Figure 4a. Transmit Timing with External Clock

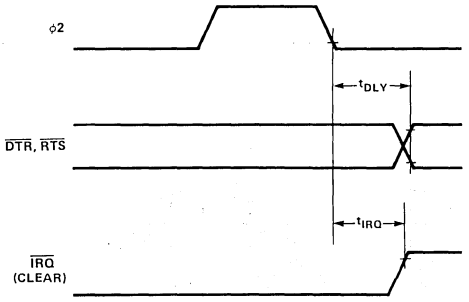
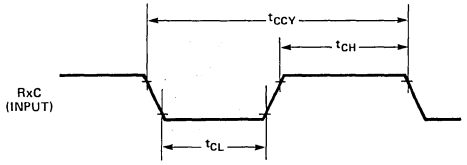


Figure 4b. Interrupt and Output Timing



NOTE: RxD rate is 1/16 RxC rate.

Figure 4c. Receive External Clock Timing

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	—	400*	—	ns
Transmit/Receive Clock High Time	t_{CH}	175	—	175	—	ns
Transmit/Receive Clock Low Time	t_{CL}	175	—	175	—	ns
XTAL1 to TxD Propagation Delay	t_{DD}	—	500	—	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	—	500	—	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	—	500	—	500	ns

(t_r, t_f = 10 to 30 nsec)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6551. A low on the R/$\overline{W}$ pin allows a write to the SY6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0 - DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS_1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The SY6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_ϕ, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various SY6551 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the SY6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/MODEM INTERFACE SIGNAL DESCRIPTION

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the SY6551 to the modem. A low on $\overline{DTR}$ indicates the SY6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the SY6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the SY6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

INTERNAL ORGANIZATION

The Transmitter/Receiver sections of the SY6551 are depicted by the block diagram in Figure 5.

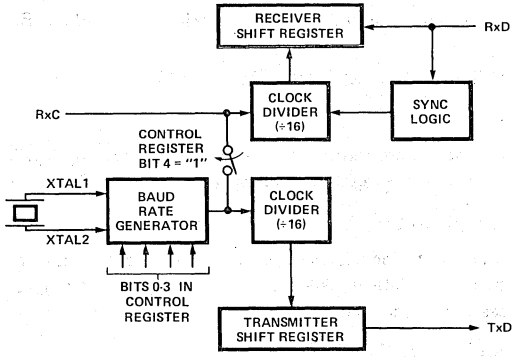


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the SY6551.

CONTROL REGISTER

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

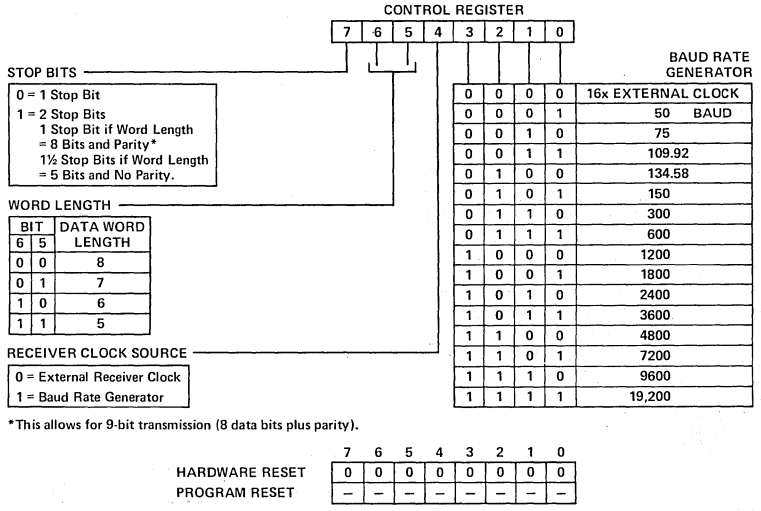


Figure 6. Control Register Format

COMMAND REGISTER

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.

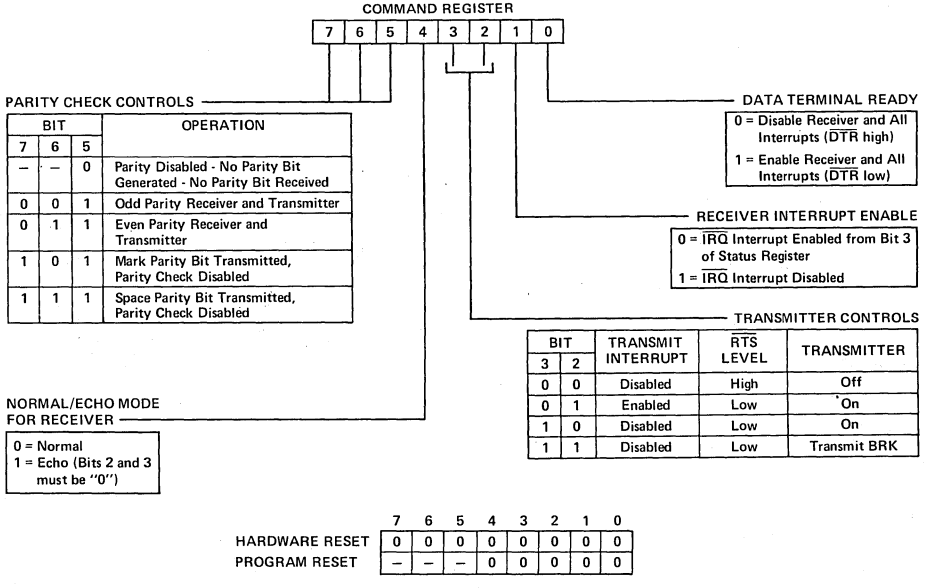
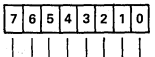


Figure 7. Command Register Format

STATUS REGISTER

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.



STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

TRANSMIT AND RECEIVE DATA REGISTERS

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

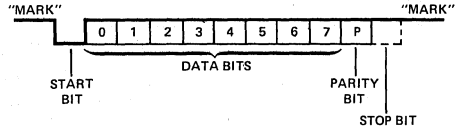
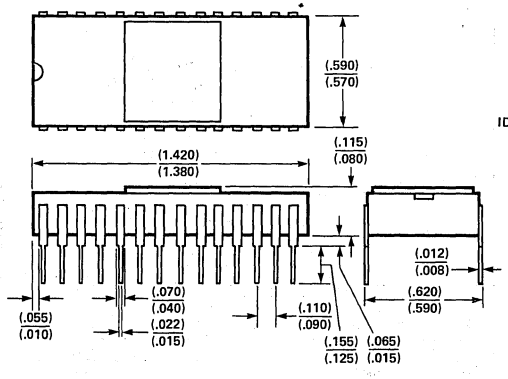


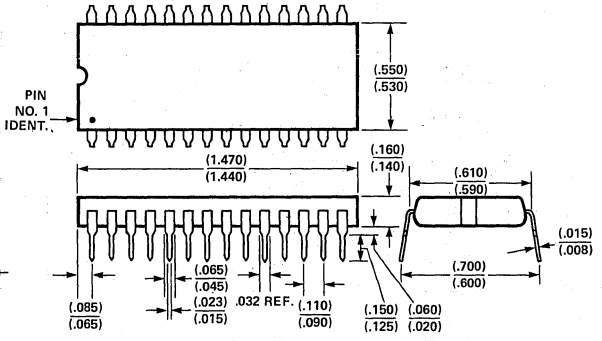
Figure 9. Serial Data Stream Example

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



Asynchronous Communication Interface Adapter

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Extended Temperature
(-40°C to +85°C)

SYE6551
SYE6551A

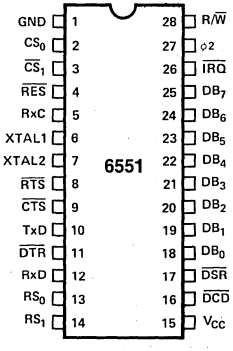
MICROPROCESSOR PRODUCTS

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.
- Operation over wide temperature range (-40°C to +85°C)

The SYE6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

MICRO PROCESSORS

PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Package	Clock Frequency
SYEC6551	Ceramic	1 MHz
SYED6551	Cerdip	1 MHz
SYEP6551	Plastic	1 MHz
SYEC6551A	Ceramic	2 MHz
SYED6551A	Cerdip	2 MHz
SYEP6551A	Plastic	2 MHz

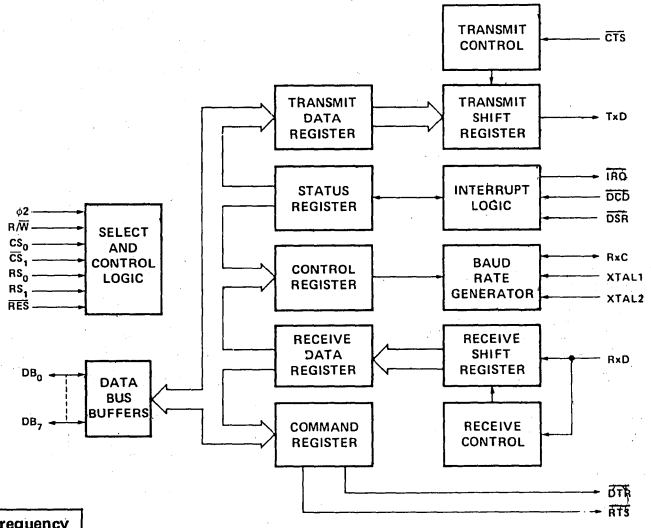


Figure 1. Block Diagram

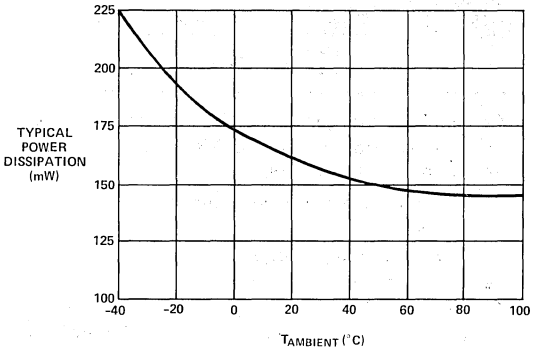
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Allowable Range
Supply Voltage	V_{CC}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to +7.0V
Operating Temperature	T_{OP}	-40°C to +85°C
Storage Temperature	T_{STG}	-55°C to 150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

POWER DISSIPATION vs TEMPERATURE



D.C. CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = -40°C to +85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	-0.3	–	0.8	V
Input Leakage Current: V_{IN} = 0 to 5V (ϕ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS}_1$, RS_0, RS_1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$)	I_{IN}	–	±1.0	±2.5	μA
Input Leakage Current for High Impedance State (Three State)	I_{TSI}	–	±2.0	±10.0	μA
Output High Voltage: I_{LOAD} = -100μA (DB_0 – DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	V_{OH}	2.4	–	–	V
Output Low Voltage: I_{LOAD} = 1.6mA (DB_0 - DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	V_{OL}	–	–	0.4	V
Output High Current (Sourcing): V_{OH} = 2.4V (DB_0 – DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$)	I_{OH}	-100	–	–	μA
Output Low Current (Sinking): V_{OL} = 0.4V (DB_0 – DB_7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	I_{OL}	1.6	–	–	mA
Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	I_{OFF}	–	1.0	10.0	μA
Clock Capacitance (ϕ2)	C_{CLK}	–	–	20	pF
Input Capacitance (Except XTAL1 and XTAL2)	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	10	pF
Power Dissipation (See Graph) (T_A = 0°C) V_{CC} = 5.25V	P_D	–	220	350	mW

SYNERTEK
A SUBSIDIARY OF HONEYWELL

Floppy Disk Controller (FDC)

SY6591/SY6591A

MICROPROCESSOR PRODUCTS

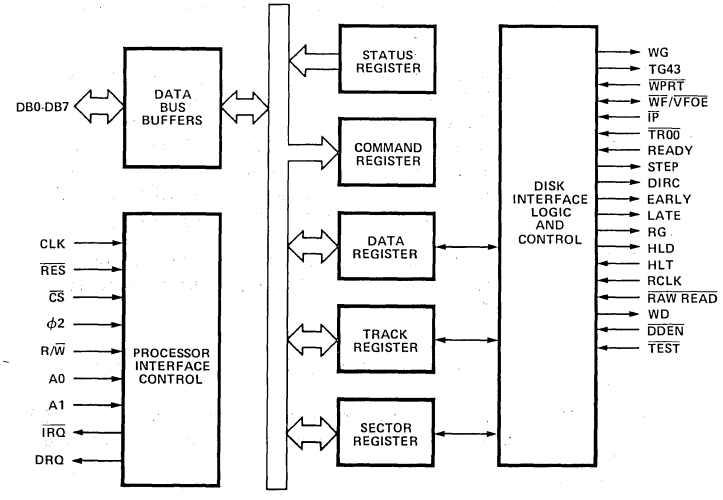
PRELIMINARY

- Functionally compatible with SY1791-02/SY1793-02
- MPU bus interface directly compatible with SY6500 and MC6800 microprocessors.
- Single 5 volt power supply
- Accommodates both single-density (FM) and double-density (MFM) formats
- IBM format compatibility:
  - IBM 3740 Single-Density
  - IBM System-34 Double-Density

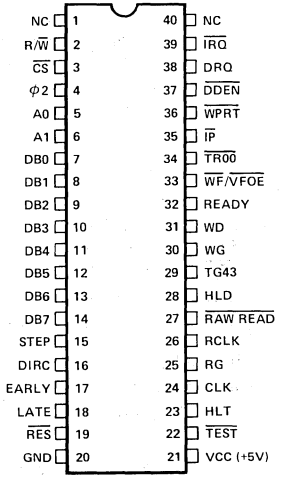
The SY6591 Floppy Disk Controller is a fully programmable device intended for SY6500 or MC6800 microprocessor-based systems. Floppy disk control functions are fully autonomous and are thoroughly described in the SY1791-02/SY1793-02 data sheet. The SY6591 version is different only in the MPU bus interface characteristics.

MICRO-PROCESSORS

BLOCK DIAGRAM



PIN ASSIGNMENTS



ORDERING INFORMATION

Part Number	Package	MPU Clock Rate
SYC6591	Ceramic	1MHz
SYD6591	Cerdip	1MHz
SYP6591	Plastic	1MHz
SYC6591A	Ceramic	2MHz
SYD6591A	Cerdip	2MHz
SYP6591A	Plastic	2MHz

DETAILED LIST OF FEATURES

- Single 5 volt (±5%) power supply
- 40-pin package
- Automatic track seek with verification
- Accommodates single-density (FM) and double-density (MFM) formats
- Soft-sector format compatibility
- IBM 3740 (single-density) and System-34 (double-density) compatible
- Single or multiple record read with automatic sector search or entire track read
- Selectable record length (128, 256, 512 or 1024 bytes)
- Single or multiple record write with automatic sector search
- Entire track write for initialization
- Programmable controls:
  - Selectable track-to-track stepping time
  - Selectable head settling and engage times
  - Head position verification
  - Side verification
- Double-buffered read and write data flow
- DMA or programmed data transfers
- TTL-compatible inputs and outputs
- Write precompensation (FM and MFM)
- Comprehensive status register

PROCESSOR INTERFACE SIGNALS

- $\phi 2$ ($\phi 2$) — The $\phi 2$ signal is combined with $\overline{CS}$ to gate the processor interface signals A0, A1 and R/$\overline{W}$ into the floppy disk controller (FDC).
- DATA BUS (DB0-DB7) — This 8-bit non-inverting bidirectional data bus is used for transferring data, control, and status words. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.
- READ/WRITE (R/$\overline{W}$) — This input signal is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read data supplied by the FDC. A low on the R/$\overline{W}$ pin allows data to be written to the FDC.
- INTERRUPT REQUEST ($\overline{IRQ}$) — The $\overline{IRQ}$ is an open drain output. This signal goes low at the completion or termination of any operation and is reset when a new command is loaded into the command register or when the status register is read. An external pull-up resistor to V_{CC} is required when using the SY6591 with a SY6500 or a MC6800 MPU.
- RESET ($\overline{RES}$) — This signal is identical to $\overline{MR}$ on the SY1791-02/SY1793-02. A low on this input resets the device and loads hex 03 into the command register. The Not Ready status bit (status bit 7) is reset during $\overline{RES}$ low. When $\overline{RES}$ is driven high, a Restore command is executed regardless of the state of the Ready signal, and hex 01 is loaded into the Sector Register.
- REGISTER ADDRESS LINES (A0-A1) — These inputs address the internal registers for access by the Data Bus lines under R/$\overline{W}$ and $\phi 2$ control.

REGISTER ADDRESS CODES

A1	A0	READ	WRITE
0	0	STATUS	COMMAND
0	1	TRACK	
1	0	SECTOR	
1	1	DATA	

- READ/WRITE (R/$\overline{W}$) — If $\overline{CS}$ is low, a high on this input enables the addressed internal register to output data onto the data bus when $\phi 2$ is high. If $\overline{CS}$ is low, then a low on this input gates data from the data bus into the addressed register when $\phi 2$ is high.
- CHIP SELECT ($\overline{CS}$) — A low level on this input selects the FDC and enables processor communications with the FDC.
- DATA REQUEST (DRQ) — DRQ is an open drain output. DRQ high during read operations indicates that the Data Register (DR) contains data. When high during write operations, DRQ indicates that the DR is empty and ready to be loaded. DRQ is reset by reading or loading the DR during read or write operations, respectively. Use 10K pull-up resistor to V_{CC}.
- CLOCK (CLK) — This input requires a square wave clock for internal timing reference (2 MHz for 8-inch drives, 1 MHz for 5-inch drives).

FLOPPY DISK CONTROL FUNCTIONS

These functions are identical to those of the SY1791-02/SY1793-02, and are fully described in the corresponding data sheet.

D.C. CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0-70°C) PRELIMINARY

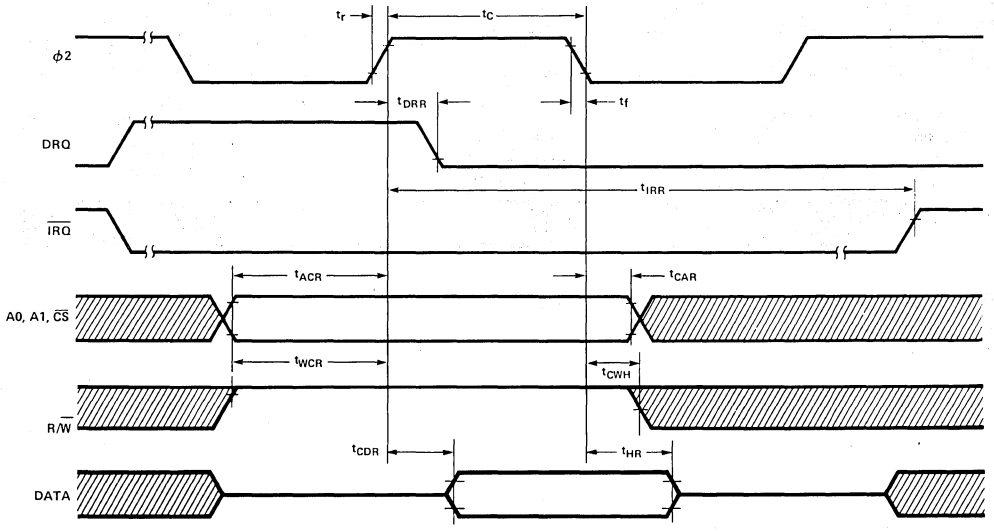
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.0	–	V
Input Low Voltage	V_{IL}	–	0.8	V
Input Leakage Current, V_{IN} = 0V to V_{CC}	I_{IL}	–	± 10	μA
Output High Voltage, I_{LOAD} = -100 μA	V_{OH}	2.4	–	V
Output Low Voltage, I_{LOAD} = 1.6 mA	V_{OL}	–	0.4	V
Output Leakage Current, V_{OUT} = V_{CC}	I_{OL}	–	10	μA
Power Dissipation (V_{CC} = 5.25 V)	P_D	–	525	mW
Input Capacitance	C_{IN}	–	15	pF

READ CYCLE (V_{CC} = 5.0V ±5%, T_A = 0 to70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	μs
Address Setup Time	t_{ACR}	180	–	90	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCR}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Access Time	t_{CDR}	–	395	–	200	ns
Data Bus Hold Time	t_{HR}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

READ TIMING

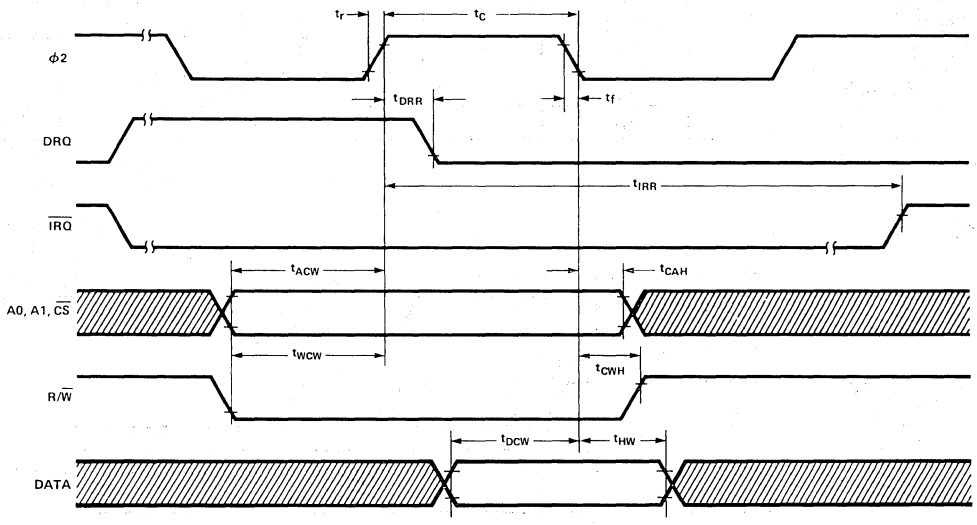


WRITE CYCLE (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	6591		6591A		Units
		Min.	Max.	Min.	Max.	
$\phi 2$ Pulse Width	t_C	470	–	235	–	ns
DRQ Reset From $\phi 2$	t_{DRR}	–	500	–	500	ns
$\overline{IRQ}$ Reset From $\phi 2$	t_{IRR}	–	3	–	3	μs
Address Setup Time	t_{ACW}	180	–	90	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Setup Time	t_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Setup Time	t_{DCW}	300	–	150	–	ns
Data Bus Hold Time	t_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE TIMING



ANSI Rigid Disk Controller (ARDC™)

SYNERTEK
A SUBSIDIARY OF HONEYWELL

SY6691/2

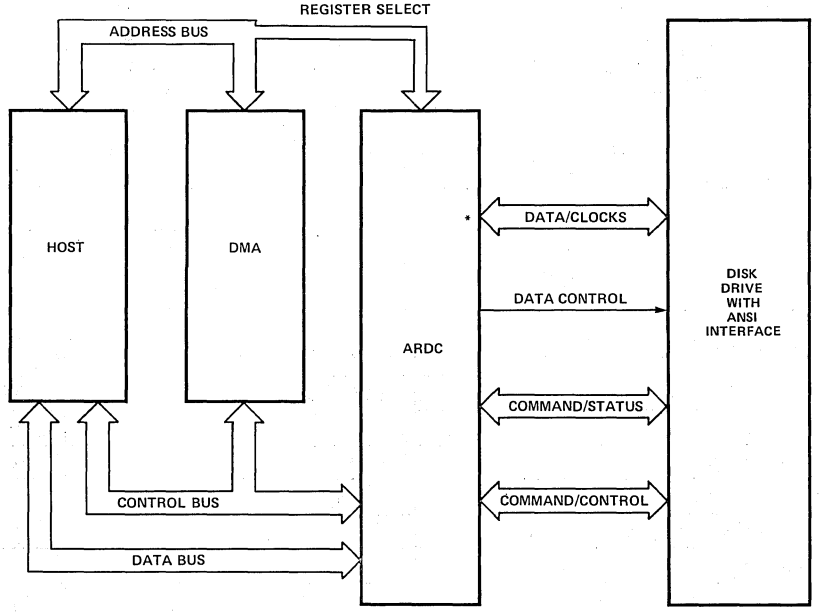
MICROPROCESSOR PRODUCTS

ADVANCED INFORMATION

- Meets proposed ANSI Interface Standard*
- Built-in self-check capability
- Single +5 volt supply
- Works with all ANSI commands
- High level (Macro) commands
- Internal CRC generation and checking
- 8-bit or 16-bit data bus
- Handles up to 8 drives

The Synertek SY6691/2 ANSI Rigid Disk Controller (ARDC) is fully programmable by a host system. The ARDC is intended for the control of ANSI interface Winchester-type disk drives in microprocessor based systems. The use of high-level commands minimizes CPU intervention. The SY6691 has an 8-bit data bus, the SY6692 a 16-bit data bus.

BLOCK DIAGRAM



*External line drivers/receivers

MICRO-PROCESSORS

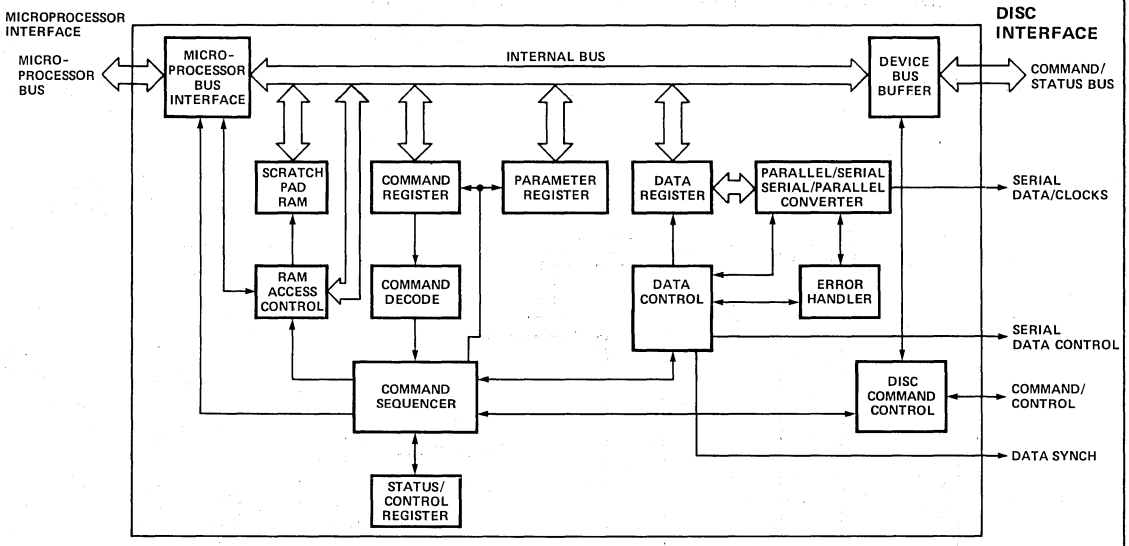
FEATURES

- Meets proposed ANSI interface standard
- Built-in self-check capability
- Single +5 volt supply
- Designed in high-density NMOS
- Host uses high-level commands
- Host may issue primitive commands
- CRC is generated by the ARDC
- CRC checked on all data read
- ARDC holds an image of the drive parameters
- Up to 8 drives may be controlled
- Communication with host memory is via DMA
- Available with 8-bit or 16-bit data bus
- Data rate up to 10 Megabits/sec
- Data synch signal for ECC

High Level Commands Include:

- Initialize All Drives
- Initialize Drive N
- Ready Drive N
- Read, Write, and Verify with implied Seek
- Read N sectors
- Diagnostic Read
- Write N sectors
- Verify Disk, Track, or Sector
- Implied Retry with offset
- Abort
- Erase Address Mark
- Format Disk, Track, or Sector

LOGICAL BLOCK DIAGRAM (ARDC)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0-70° C)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Input High Voltage	V_{IH}	2.0		V
Input Low Voltage	V_{IL}		0.8	V
Input Leakage Current, V_{IN} = V_{CC}	I_{IL}		10	μA
Output High Voltage, I_{LOAD} = -100 μA	V_{OH}	2.4		V
Output Low Voltage, I_{LOAD} = 1.6 mA	V_{OL}		0.45	V
Output Leakage Current, V_{OUT} = V_{CC}	I_{OL}		10	μA

CRT Controller (CRTC)

SY68045

SYNERTEK
A SUBSIDIARY OF HONEYWELL

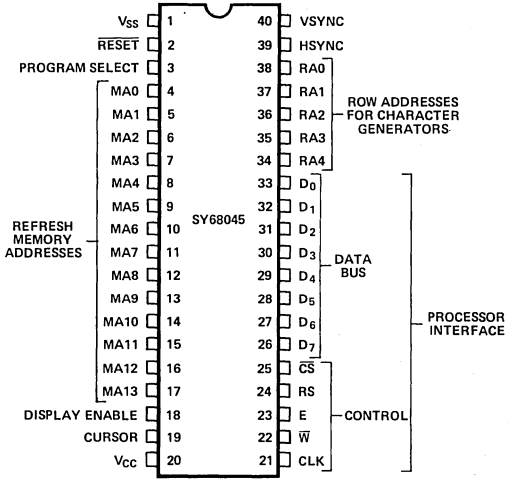
PRELIMINARY

FEATURES

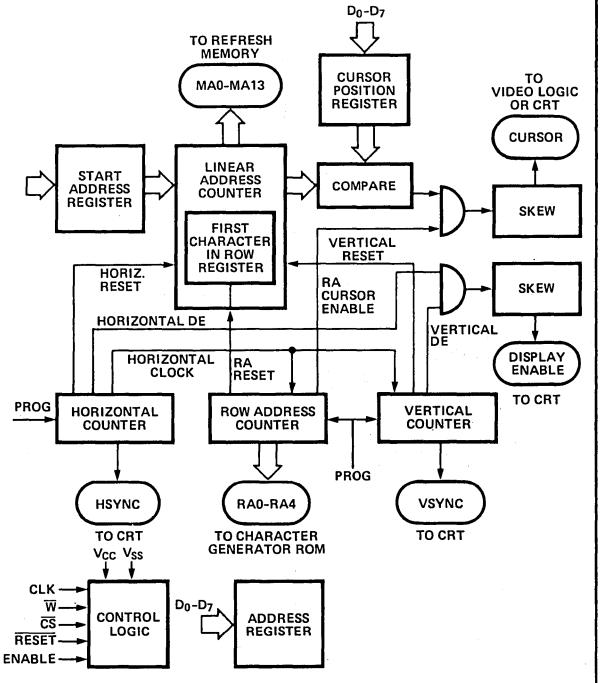
- Generates refresh addresses and row selects
- Generates video monitor inputs: horizontal and vertical sync and display enable
- Low cost; MC6845/SY6545 pin compatible
- Text can be scrolled on a character, line or page basis
- Addresses 16K bytes of memory
- Screen can be up to 128 characters tall by 256 wide
- Character font can be 32 lines high with any width
- Two complete ROM programs
- Cursor and/or display can be delayed 0, 1 or 2 clock cycles
- Four cursor modes:
  - Non-blink
  - Slow blink
  - Fast blink
  - Reverse video with addition of a single TTL gate
- Three interface modes
  - Normal sync
  - Interlace sync
  - Interlace sync and video
- Full hardware scrolling
- NMOS silicon gate technology
- TTL-compatible, single +5 volt supply

MICRO-PROCESSORS

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Clock Rate
SYC68045	Ceramic	1 MHz
SYD68045	Cerdip	1 MHz
SYP68045	Plastic	1 MHz

Logic Capabilities

Siemens Confidential

Why Go Custom And Why Use Synertek?

Your decision to use a Custom circuit rests basically on the requirements of your system. You'll want to consider the alternatives available to you:

- **Standard circuits** are off-the-shelf products designed for general product applications. If your yearly system volume will be less than 10,000, SSI (small scale integration) and MSI (medium scale integration) circuits may be your best solution.
- **Microprocessors** may fill your need if your application requires great flexibility and cost is not an overriding factor. They are most practical when total circuit volume does not exceed 50,000.

Advantages of Custom Circuits
A Custom circuit is an exclusive proprietary design built specifically to meet your product requirements. Its advantages are:

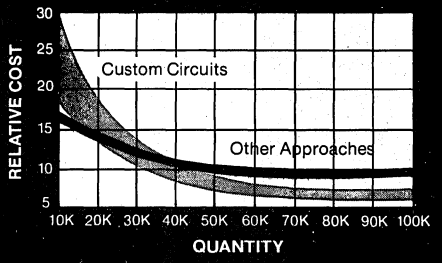
- **Reduced system cost**—Through circuit integration the total number of discrete and integrated components can be cut by 75-90%. This dramatically reduces component inventory, PC board assembly, and power supply costs.
- **Increased reliability**—As circuit device count and total system size is reduced, system reliability increases. For you, the more reliable a system you sell to your customers, the less you will have to expend on warranty costs.
- **Features**—Special features not available in standard circuits or microprocessors can be cost-effectively designed into a Custom circuit.
- **Market leadership**—CUSTOM MOS/LSI technology can revolutionize a product. It enables new features to be built which would otherwise be unavailable or too expensive to implement. When your product is manufactured with a proprietary design, competitors have a more difficult time copying it. As a result, you can enjoy longer periods of market leadership and penetration.

Why Use Synertek?
You don't want just anyone to develop your Custom design. You want a company with experience, skill and an understanding of how important your design is to you. As a major supplier of Custom circuits, we fulfill those requirements and offer competitive design and process solutions.

Our ability to develop sophisticated technologies insures our market leadership position in custom integrated circuits. We currently offer silicon gate HMOS, NMOS, and HCMOS technologies. Our advanced computer-aided design facilities, projection alignment equipment, 4-inch wafer fabrication lines, and VLSI testing equipment further demonstrate Synertek's commitment to state-of-the-art technology. Your choice depends on your need.

- **Classic Custom circuit design**—We will design your circuit from concept. You may initially provide us with a written explanation of the function you want, or with a logic diagram of the circuit, or with just a specification. We will create your work-of-art from beginning to full production.
- **C.O.T.™**—Synertek will become the manufacturing arm of your in-house design group or your consulting design house. By providing you with process design rules, parameters, computer simulation programs and, most of all, our total cooperation, we can assure you the manufacturing capability you want.
- **Cooperative design, training, and production**—You may want to set up your own CUSTOM LSI design group for reasons of design control and flexibility. We can help you achieve this on a joint-development basis. Your engineers would come to Synertek and work with our engineers through a complete design cycle. This training method shortens your learning curve and enables you to develop a technical and manufacturing partnership with a major Custom vendor.

We advocate a firm policy of partnership in all three of these circuit production services. Your success is directly related to ours, and a close working relationship promotes understanding and efficiency between us. It also insures that the Custom circuit is produced exactly to your specifications. This spirit of cooperation and teamwork will heighten your feeling of ownership for your proprietary Custom circuit.

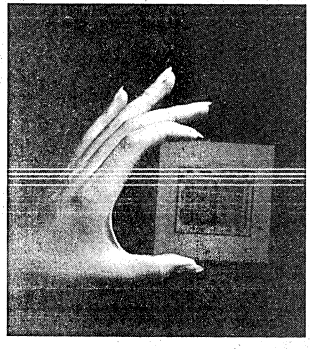


Custom costs vs. other alternatives

Evolution Of A Masterpiece

A masterpiece is never developed overnight. An artist needs time to think, plan, and create. At Synertek, the average length of time needed to bring a circuit from the concept stage to prototype production is 6-9 months. Depending on the complexity of the device, this may be longer or shorter. Simple circuits can be completed within 3-4 months. All circuits, however, are subjected to the same stringent testing, quality control, and verification checks.

Keeping with our philosophy of partnership, our engineers will confer with you often throughout the design and development phases.

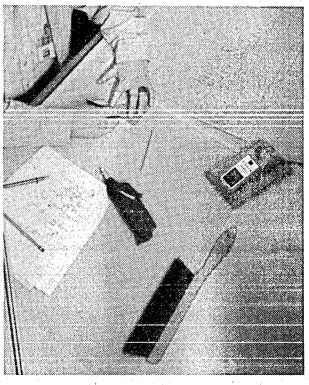


Reticles are used for mask production and are made from database tapes. One reticle represents one layer of the circuit. Some circuits have up to ten layers.

The Design and Development Process

- **System definition—** Synertek and the customer establish block diagrams, flow charts, and mechanical and electrical specifications. A program milestone schedule is confirmed.
- **Logic design and computer simulation—**Our design engineers convert system functions to MOS logic. Computer simulations of critical logic design characteristics are done in our DA (design automation) center. SCEPT™ (Synertek Circuit Emulation Program and Test) is a conventionally designed breadboard which duplicates MOS logic. We consider SCEPT™ an indispensable tool for verifying the functionality of the design. It also gives you your first opportunity for hands-on verification of the actual logic functions. Once approved by you, SCEPT™ is used to write and debug a test program. From this point, SCEPT™ is the functional reference for the remaining design steps.

1-10 wks.



Synertek engineers perform the initial logic design. In the case of C.O.T.™, a customer may provide Synertek with his circuit design on a database tape, a pattern generator tape, or a working plate.

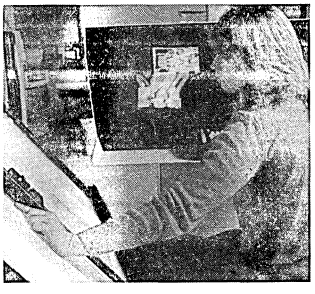
- **Circuit design and analysis**— Individual transistors are laid out to implement the SCEPT™ logic. Particular attention is paid to critical speed paths. Additional computer-aided circuit simulation information is analyzed and incorporated into the actual circuit design.

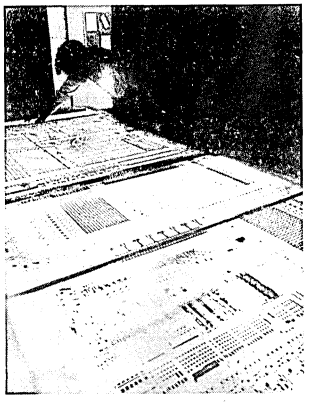
1-4 wks.

- **Composite layout design**— A layout of the circuit design, called a composite, is hand drawn to minimize final chip size. Composites are drawn at 500 to 2000 times the size of the finished chip.
- **Digitizing**—The composite drawing is converted in our CAD (Computer Aided Design) center to a database tape using a Calma interactive graphic system. This digitized information is used to generate plots of each circuit layer. The plots are compared to the original composite and editing changes are made. Editing and checking continues until the database tape is approved for the entire composite. Design rule checks (DRCs) and electrical rule checks (ERCs) are accomplished by our CAD system using the database tape.

4-14 wks.

A technician digitizes a composite through the use of GDS-II. Such equipment is part of Synertek's sophisticated Computer Aided Design capability.





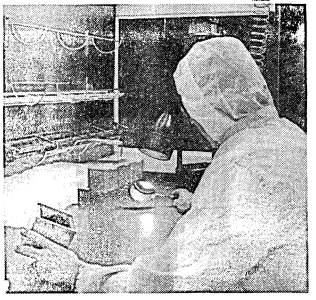
With the help of a "light table" each mask layer is verified against the original circuit plot to assure absolute accuracy.

- **Mask generation**—Once the database tape is approved, a PG (pattern generation) tape is produced. This tape is used to create each mask level.
  We use three methods in mask making—photolithography, E-beam and a combination of both.
  In the photolithographic process the 10X reticles are created on a pattern generator. These reticles are photo reduced to the actual 1X mask size and reproduced by a step-and-repeat camera.
  With E-beam technology, the PG tape is converted to E-beam format. The full array is then written directly at the 1X mask size.
  In the combination method, 10X reticles are generated from the E-beam-formatted tape. As in the photolithographic process, these reticles are then photo reduced to the actual 1X mask size and reproduced by a step-and-repeat camera.
  Which method should be used is determined by device complexity, die size, and the process chosen for wafer fabrication.

4-9 wks.

- **Prototype wafer fabrication**—During prototype fabrication, numerous quality and electrical inspections are performed to assure that every wafer lot meets our specifications.
- **First samples**—These are untested devices commonly referred to as "Cut & Go's." They are placed in ceramic packages, assembled, and sent to you for initial evaluation.

2-3 wks.



All wafer fabrication and quality inspections are performed in a clean room environment. Room temperature is controlled to within + or -1° C. All employees wear clean room attire to keep air impurities to a minimum.

- **Test generation**—The Cut & Go's play an essential role in the completion of the test program, which was initiated during the circuit design stage. The test program must be verified with the Cut & Go's before it is finalized.
- **Prototype production**— After fully tested samples are approved, prototype production begins.
- **Full production**— Scheduled delivery commences after prototype qualification and test verification are completed.

C.O.T.™ & MOS Processes

Perhaps you have your own MOS design group, or have chosen to have your circuit designed by a consulting firm. Or maybe another MOS supplier designed the chip and you want to tool-up a second-source supplier. Whatever your design source, we can produce your circuit on a customer owned tooling (C.O.T.™) basis.

Because of our extensive experience with MOS/LSI technology, we understand your reasons for going C.O.T.™. You want to minimize design cost and production time while maximizing proprietary design control. We guarantee that your Custom circuit will receive the same confidential, proprietary treatment as our own in-house designed circuits.

You may enter the production cycle at a number of various stages. We'll accept your design on a database tape, a pattern generator tape, or working plate. You'll be given an initial documentation package that includes an overview of design rules and parameters for our MOS processes.

Again, we will meet with you as early in the program as possible to establish a close working relationship. If you wish to design your own proprietary circuit, our engineering staff is available for design workshops and general program guidance, on a consulting basis. We take measures to enhance a smooth product flow. Our program managers monitor your circuit from our CAD center through production. We also have a back-log control system that continually updates you on product schedules and shipments.

As a C.O.T.™ customer, you not only will have access to our extensive manufacturing and assembly facilities, but our overall company technologies as well.

SILICON GATE NMOS

PROCESS	FLDI²	ENHI²	DEPI²	V_{SB}	V_{TEO}	V_{TDO}
				VOLTS		
NSJ2	YES	YES	YES	0	+0.7	-4.0
NPJ4	YES	NO	YES	-2.5	0.45	-3.3
NDK4	YES	YES	YES	0	+0.2	-3.0
NPK4	YES	YES	YES	0	0.45	-3.3
NTK4	YES	YES	YES	-3.0	+0.8 VTI +0.3V	-3.5
NPM5	YES	YES	YES	0	+0.5 -0.2	-3.0 -1.3

BURIED CONTACT OPTION AVAILABLE

* SHRINKABLE BY 16% FOR LOW VOLTAGE APPLICATIONS

V_{TFO}	BVDSS	BETA	GAMMA	C_{DA}	ρN	ρP	Xj	CHANNEL	TOPOLOGICAL PITCH			COMMENTS
		A/V²	V½	F/cm²x10⁻⁸	Ω/□	Ω/□	μ	LENGTH μ	POLY WIDTH/ SPACE μ	DIFF. WIDTH/ SPACE μ	Al-Al WIDTH/ SPACE μ	
VOLTS												
10	10	12	0.95	1.5	20	45	1.1	6	6/7	6/7	7/7	*
15	20	12	0.65	1.6	15	45	1.2	6	6/6	6/6	7/7	* Planox
16	10	11	0.25	0.7	15	60	1.5	6	6/6	6/6	6/6	Planox. 2 poly process, switch capacitor techniques for analog circuits.
15	20	12	0.65	1.6	15	45	1.2	6	6/6	6/6	7/7	* Planox
15	10	15	0.30	1.5	12	45	1.1	5	5/5	5/5	5/5	Has an intrinsic transistor mask option. High speed applications.
15	7	19	0.26	0.7	27	30	0.45	3 (E&D) 4 (I)	4/5	5/5	5/5	Dual implants for each ENH and DEP transistor. (optional)

SILICON GATE CMOS

PROCESS	CHANNEL	V_{TFO}	V_{TO}	BETA UA/V²	BVDSS	GAMMA	ρN or ρP Ω/□	ρPOLY Ω/□	CHANNEL LENGTH	TOPOLOGICAL PITCH				COMMENTS
										POLY WIDTH/ SPACE	P WELL WIDTH/ SPACE	DIFF. WIDTH/ SPACE	AL-AL WIDTH/ SPACE	
CSI 3	P-Channel	-16	-1.5	-2.5	-20	0.8	50	80	8μ	8/7μ				—
	N-Channel	+10	+0.9	+3.3	+20	2.6	20	70	6μ	6/7μ	8/20μ	6/9μ	7/7μ	
CSI 5	P-Channel	-4.0	-0.4	-2.1	-20	0.8	50	80	8μ	8/7μ				—
	N-Channel	+5.0	+0.6	+6.0	+20	1.2	20	70	6μ	6/7μ	8/20μ	6/9μ	7/7μ	
CSI 7	P-Channel	-8.0	-0.7	-2.1	-20	0.8	50	80	8μ	8/7μ				—
	N-Channel	+8.0	+0.75	+7.0	+20	1.3	20	70	6μ	6/7μ	8/20μ	6/9μ	7/7μ	
ICMOS 1	P-Channel	-25.0	-0.60	-9.0	-20	—	25	15	5μ					N-Well
	N-Channel	+25.0	+0.65	+22.0	+20	—	10	15	5μ	5/5μ	5/22μ	5/5μ	5/6μ	Dble Poly
HCMOS 1	P-Channel	-10.0	-0.80	-6.0	-18	0.3	60	40	3μ				3.5	—
	N-Channel	+10.0	+0.65	+19.0	+19	0.5	35	40	3μ	3/3μ	3/13μ	3/4.5μ	4.5μ	

A Process for Every Masterpiece
Selecting the right process for your Custom circuit is one of your most important decisions in the design cycle.

Synertek's offering of fully proven manufacturing processes has the right answer for you. It includes state-of-the-art HMOS and HCMOS in addition to the industry standard NMOS silicon gate technology.

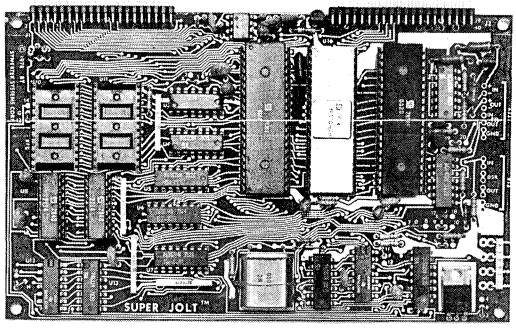
The chart on these pages contains conservative data on Process Characteristics and Topology. This data is provided only as a guideline to help you determine the general "fit" to new circuits and those already in production. Detailed Electrical and Topological Design Rules are available under a non-disclosure agreement.

You may find that the process requirements for your circuit differ from what is shown on our chart. If so, be assured that our process engineers will work with you to determine any needed variations for your circuit.

Systems

SNEAK PREVIEW

CP110 SUPER JOLT



- SY6502 NMOS 8-Bit Microprocessor
- 1K Bytes of Static RAM Memory
- 64 Bytes of Interrupt Vector RAM
- 28 Bi-Directional Programmable I/O Lines
- 1 MHz Crystal Controlled Clock
- Interval Timer
- Four Interrupts, Including a Timer Interrupt and a Non-Maskable Interrupt
- Three Serial Interfaces — 20 mA Current Loop, RS-232-C and TTL
- Buffered Address and Data Lines
- 1,024 Bytes of Resident ROM Program Memory Containing DEMON Debug Monitor Program
- Dimensions 4.25 in. x 7.00 in.

The CP110 SUPER JOLT CPU board is the most versatile microcomputer on a single PC board. Connected to a terminal, the CP110 provides everything necessary to begin writing, debugging, assembling and executing microcomputer programs. Stand-alone, the CP110 is a single board OEM microcomputer suited to a wide range of dedicated applications.

AS200 UNIVERSAL CARD

- Ideal for Experimental/Prototype Circuits
- Accepts 14-Pin to 40-Pin Wirewrap Sockets
- Power and Ground Busses Provided for Each Row of Holes
- Accepts up to 50 14-Pin Sockets
- Dimensions: 4.25 in. x 7.00 in. Card Compatible with SUPER JOLT

Universal Card is ideal for constructing experimental and prototype circuits. Holes are provided for mounting connectors for mating cables to interconnect the AS200 to other boards in the SUPER JOLT family.

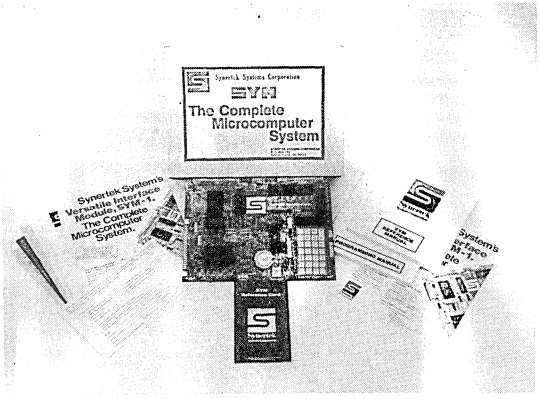
SYSTEMS

EPS-1 SYM-1 DIAGNOSTIC PROGRAM

- Diagnostic/Test Program for SYM-1
- Supplied as a Pre-Programmed 2716 EPROM
- Function Test for On-Board RAM, ROM, Display LEDs, Keyboard, I/O Chips, TTY/CRT I/O, Cassette I/O, and Scope Output
- Modular Tests with Separate Error Messages
- Version Available for SUPERMON V1.0 or SUPERMON V1.1
- Useful for Receiving Inspection, Field Service, or Self-Test by User
- Complete with Manual Containing Instructions, Error Codes, Flow Charts, Trouble Shooting Aids and a Complete Test Program Listing

The EPS-1 Diagnostic Program for SYM provides a valuable self-test capability to aid in any phase of test, trouble shooting or repair. Essentially all components of the SYM are functionally tested assuring a fully working unit.

SYM-1 SINGLE BOARD COMPUTER



- Assembled, Tested and Ready to Use
- Full Documentation — Two Manuals
- SY6502 NMOS 8-Bit Microprocessor
- 51 I/O Lines, Expandable to 71
- Five On-Board Programmable Interval Timers
- 28 Key Keypad
- Six Digit Display
- 4K Byte ROM SUPERMON Resident Monitor, User Expandable
- 1K Bytes of Static RAM provided, expandable to 4K Bytes On-Board with Sockets Provided
- User PROM/ROM for up to 28K Bytes of User Program
- Application Port — 15 Bi-directional TTL Lines, with Expansion Capability
- Expansion Port for Add-On Modules
- Requires Single +5V Supply
- Standard Interfaces:
  - Audio Cassette Recorder with Remote Control
  - Full Duplex 20mA TTY
  - System Expansion Bus
  - RS-232-C Compatible Interface
  - Four Strappable Relay Drivers or Input Buffers
- Applications In
  - Training
  - Engineering
  - Prototyping
  - Instrumentation
  - Testing
  - Experimentation
- Dimensions 8.25 in. x 10.72 in.

SYM-1 Versatile Interface Module is designed for future growth and expansion.

You can store your programs in the 1K Static RAM and debug by simply using the single-step feature of the monitor. User static RAM is easily expandable to 4K bytes on-board the basic unit. The 51 I/O lines which are available to control your custom applications can be expanded to a total of 71 I/O lines via an additional socket provided for Synertek's Versatile Interface Adapter — SY6522. Connect the SYM-1 to our KTM-3 Keyboard Terminal Module and your home TV (using an RF adapter) or monitor and you have a complete computer system with keyboard entry and video display.

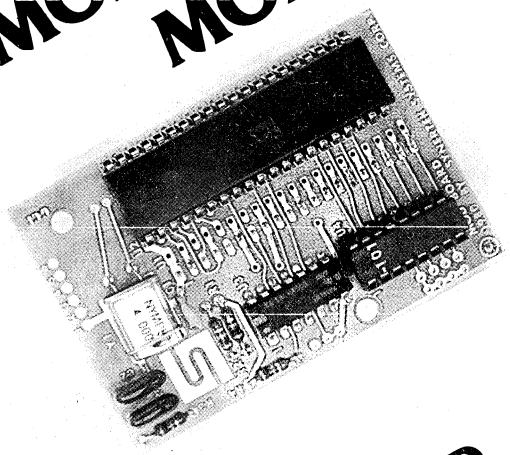
SYM-1/68 SYM-1/69 SINGLE BOARD COMPUTERS

- Features Popular 6802 8-bit NMOS Microprocessor (SYM-1/68) or New Powerful 6809 8-bit NMOS Microprocessor (SYM-1/69)
- Incorporates the Same Features and Capabilities as the Original SYM-1
- Includes New 4K Byte SUPERMON Monitors for Each New Microprocessor

Now the highly popular SYM-1 Microcomputer is available with a choice of microprocessors; the 6802 or the 6809 as well as the original SY6502. New SUPERMON Monitors give the SYM-1/68 and SYM-1/69 all the commands and operating features of the original SYM-1. A newly written SYM-1 Reference Manual is supplied which includes special sections describing use of the SYM-1 using the new microprocessors.

Also available are adaptor boards which allow existing SYM-1 microcomputers to use one of the new microprocessors. Refer to MOD-68 and MOD-69 on the next page.

MOD-68 MOD-69



- **Adapter Boards for SYM-1 Allow Use of Popular 6802 or Powerful New 6809 8-bit NMOS Microprocessors**
- **New Microprocessor and Circuitry Included on Small 2"×3" Circuit Board**
- **Includes New SUPERMON Monitor Firmware**
- **Full Instructions Supplied for Making the Simple Conversion**

The MOD-68 and MOD-69 provide a low-cost means of converting existing SYM-1 microcomputers to use either the 6802 or 6809 microprocessor. The simple conversion requires the removal of the old microprocessor and SUPERMON chips, and insertion of one of the new adaptor boards.

Complete installation instructions are supplied as well as a newly written SYM-1 Reference Manual with special sections on the use of the SYM-1 with the new microprocessors.

PEX-1 PORT EXPANSION AND CONNECTOR KIT

- **Includes SY6522 Versatile Interface Adaptor**
- **Edge Connectors for Applications and Expansion Ports**
- **EIA Connector for RS-232-C Interface**
- **Phono Connectors for Cassette Interface**

The PEX-1 provides a SY6522 VIA which expands the SYM-1 I/O by an additional 20 lines. The SY6522 is plugged into socket U28 on the SYM-1 board.

Also provided are connectors to allow building a variety of interfacing cables. Included in the PEX-1 kit is a diagram for a suggested cable assembly which will provide complete connection to an EIA (RS-232-C) terminal, an audio cassette recorder, and a TTY.

SRM-1, SRM-3 STATIC RAM MEMORY KIT

- **Expand SYM-1 Memory to 2K Bytes (SRM-1) or to 4K Bytes (SRM-3)**
- **Uses Synertek SY2114L Low Power Static RAMs**

The static RAM memory kits provide for expansion of the on-board memory in the SYM-1 to 2K bytes or 4K bytes. The SY2114L low power RAM devices are plugged into existing on-board sockets per the following table.

RAM Address	Sockets	Comments
0000-03FF	U12, U13*	Lowest 1K bytes
0400-07FF	U14, U15	2nd 1K bytes
0800-0BFF	U16, U17	3rd 1K bytes
0C00-0FFF	U18, U19	4th 1K bytes

*The SYM-1 microcomputer is shipped with 1K bytes of RAM inserted in sockets U12 and U13.

SM100 OEM VERSION OF SYM-1

- **Same Power, Features, and Performance as the SYM-1 Module at lower cost.**
- **Additional Economies for O.E.M. Applications Achieved by Supplying Board without the Keyboard, Display, Speaker and Associated Electronics**

The SM100 is designed especially for OEM controller or other applications where the microcomputer board is an integral part of a user's system. All the power and flexibility of the SYM-1 is retained but without the overhead of on-board keyboard and display.

BAS-1 BASIC

- **Resides in ROM, Always Available**
- **I/O Supported by SUPERMON on SYM-1 or SM100**
- **Full Floating-Point 9-Digit, Extended BASIC**
- **Standard Dartmouth BASIC Statements**

  LET READ PRINT DATA IF
  THEN FOR NEXT DIM END
  GOTO
- **Extended BASIC Statements**

  RESTORE REM STEP GOSUB DEF
  RETURN STOP INPUT FN
  ON...GOTO ON...GOSUB
- **Scientific Functions**

  SGN INT ABS SQR RND
  LOG EXP
- **Logical Operators**

  AND OR NOT
- **Operation Commands**

  RUN NEW CLR LIST CONT FRE
- **Formatting Functions (TAB, POS, SPC)**
- **Peek, Poke, JSR to Machine Code Subroutines**
- **String Functions**
- **Cassette SAVE and LOAD Statements**
- **Decimal, Hexadecimal and String Constants**
- **Real, Integer and String Variables**

BAS-1 is a full function BASIC developed for Synertek Systems by Microsoft Corporation. BASIC provides higher level language capabilities, always instantly available from ROM.

RAE-1 RESIDENT ASSEMBLER/ EDITOR/LOADER

- **Compatible with SYM-1 or SM100**
- **Resides in ROM, always available**
- **I/O Supported by SUPERMON**

Assembler

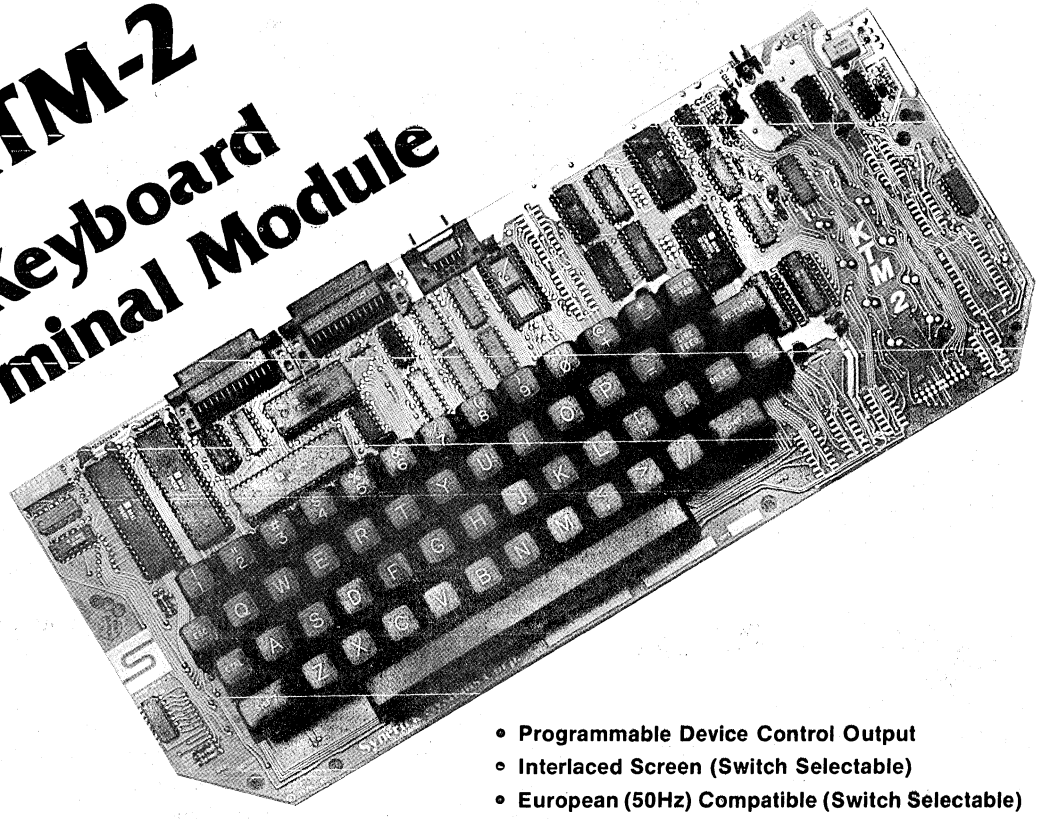
- **Macro Capability**
- **Conditional Assembly**
- **Source Input from RAM or Tape**
- **Produces Relocatable Object Code**
- **Relocating Loader**
- **Assemble with Source Listing or Errors-Only Listing**
- **Hex, Binary, Decimal or Mixed Data Types**
- **16 Assembler Pseudo-Ops**
- **23 Error Codes**
- **Storage of Hex or ASCII Bytes**

Text Editor

- **Edits Line Numbered Text**
- **Upper and Lower Case**
- **Character String Search with Optional Replace, Display or Show Number of Occurrences**
- **Line Edit**
- **Block Insert**
- **Delete Line(s)**
- **Delete File**
- **Renumber Text File**
- **Tabbing**
- **Free Format Command Input**
- **Output to Hard Copy Device With or Without Line Numbers**
- **Load and Record in High Speed Format; Entire File or Range of Lines**
- **Automatic Cassette Motor Control or Manual Control through ON and OFF Commands**

RAE-1 is a full features Resident Assembler/ Editor. Many powerful text editing functions are available with error messages giving error type and location. The user has complete control over all editor and assembler functions as well as editor controlled entry to SYM BASIC or SYM SUPERMON. The user also has control over cassette recorders for file I/O, or control may be left to software. The relocating loader may store executable code in memory during assembly or may store object code offset from its proper execution address.

KTM-2 Keyboard Terminal Module



- Choice of Character Screen Sizes:
  - 24×80 Character Screen Size (KTM-2/80)
  - 24×40 Character Screen Size (KTM-2/40)
- Full ASCII Upper and Lower Alphanumeric Character Set with Descenders
- Control and Special Characters
- 128 Graphics Characters
- Reverse Video
- Scrolling
- Cursor Blanking
- Full Cursor Control
- Absolute and Relative Cursor Addressing
- Auto CR at End of Line (Switch Selectable)
- 110 to 9600 Baud
- Even, Odd, or No Parity
- Complete RS-232-C Handshaking
- Auxiliary RS-232-C I/O Port
- Typewriter Style Keyboard 54 Keys
- Automatic Character Repeat
- Alpha Lock
- Erase — Partial Line, Partial Screen, Full Screen
- Programmable Bell Output
- Programmable Device Control Output
- Interlaced Screen (Switch Selectable)
- European (50Hz) Compatible (Switch Selectable)
- Requires Single +5V Supply

The KTM-2 provides a keyboard and all the logic circuitry for a full keyboard terminal. The display interface provides composite video for user provided monitor or for a standard TV set equipped with an RF modulator.

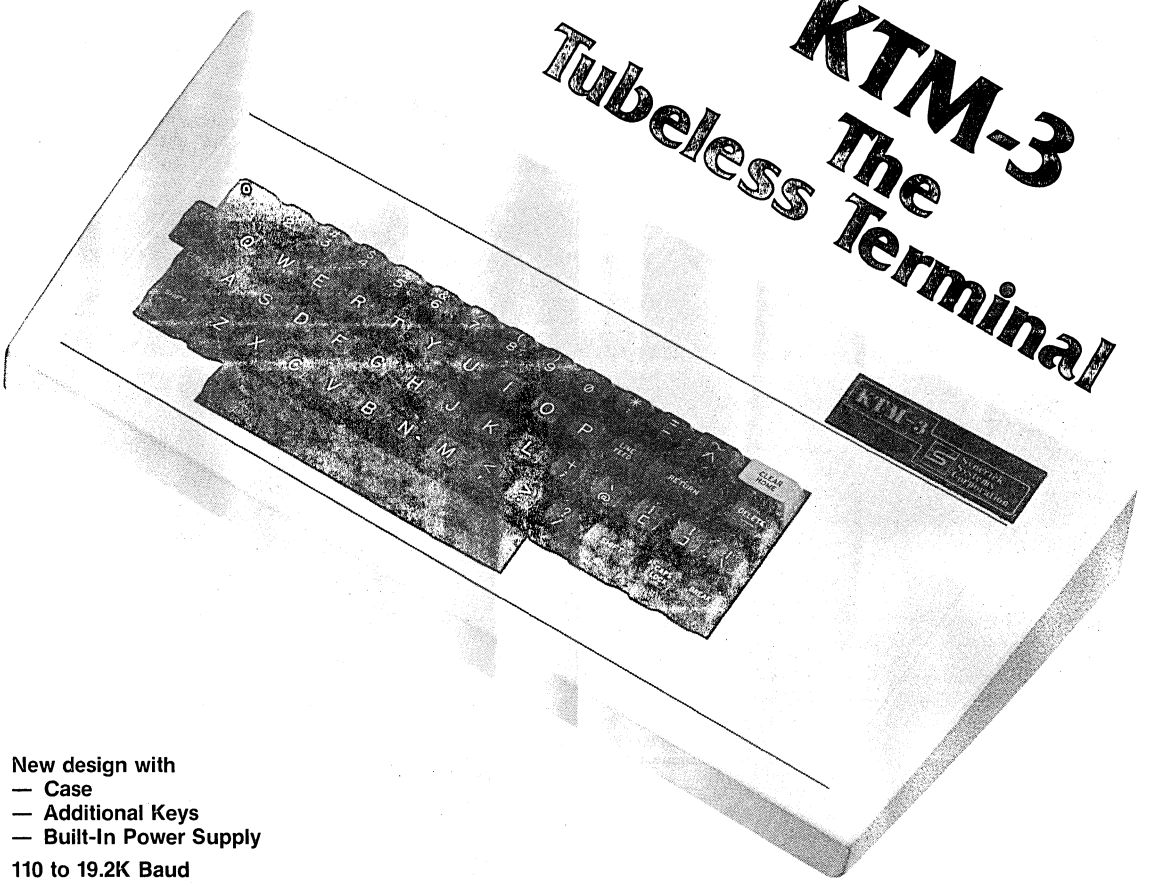
The design of the KTM-2 incorporates 8 MOS-LSI integrated circuit chips, including two dedicated microprocessors. Twenty TTL devices are used, resulting in a total chip count of 28 devices.

The use of standard LSI devices results in a highly cost effective design with great flexibility allowing modifications for custom OEM applications. More features are available at lower cost than if a CRT controller chip or other approach had been used.

CUSTOM

For large volume requirements, Synertek Systems has the capability to customize the keyboard terminal modules to meet OEM terminal subsystem requirements, offering flexibility over screen size, character size, scan rate, character set, and keyboard function and definition.

KTM-3
The Tubeless Terminal

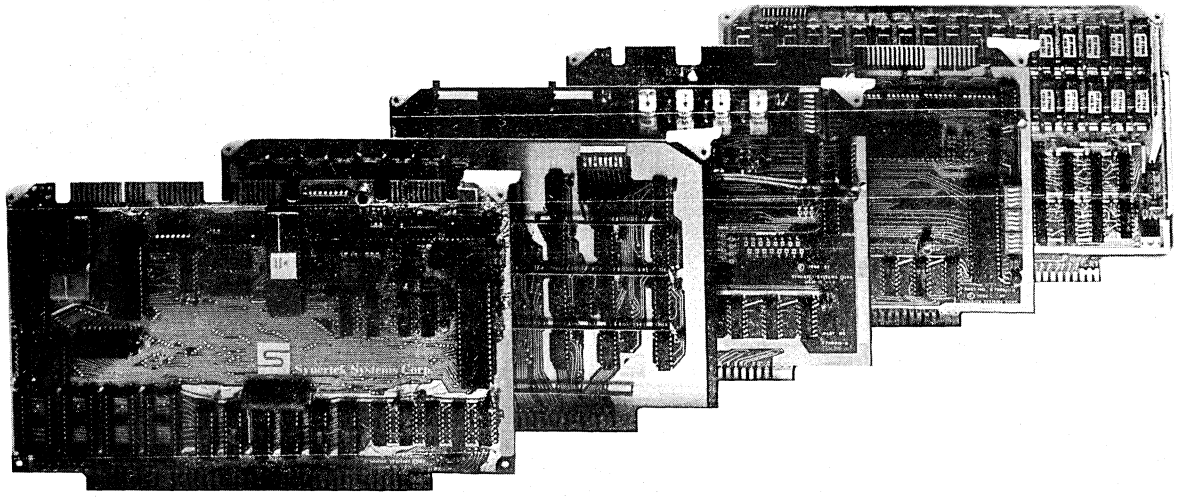


- New design with
  - — Case
  - — Additional Keys
  - — Built-In Power Supply
- 110 to 19.2K Baud
- Choice of Character Screen Sizes:
  24 × 80 Character Screen Size (KTM-3/80)
  24 × 40 Character Screen Size (KTM-3/40)
- 7 × 9 Character Matrix in 8 × 10 Field
- Typewriter Style Keyboard—58 Keys
- CAPS LOCK Key
- Upper and Lower Case Alphanumeric Character Set with Descenders
- Generates and Displays 128 ASCII Characters
- Full and Half Duplex with Modem Controls
- Built-In Power Includes On/Off Switch
- Scrolling
- Full Cursor Control
- Absolute and Relative Cursor Positioning
- Clear to End-of-Screen, End-of-Line
- Even, Odd, or No Parity
- One or Two Stop Bits
- Framing and Parity Errors Displayed
- Auto Key Repeat
- Debug Mode (Displays Control Characters)
- Cables Included
- Built-In Diagnostics
- KTM-3/40 Will Attach to Standard TV Set Using RF Modulator
- 50/60 Hz Operation
- 220 Volt Version Available

Newly designed to incorporate the best features of the popular KTM-2 series, the KTM-3 uses the latest LSI technology with two microprocessors to provide a highly reliable, ready-to-use terminal minus the CRT monitor. The dual microprocessor design is highly cost-effective with great flexibility, providing more features at lower cost than other approaches used today. For volume usage, Synertek Systems can customize the KTM-3 to your O.E.M. specifications.

The display interface provides composite video output and complete video control including scrolling, full cursor control, and absolute and relative cursor positioning. A choice of screen sizes is offered—either 24 × 40 characters, or 24 × 80 characters.

The unit is now in stock and available from your local distributor.



Synertek Systems' Micromodules

SYSTEMS

A whole new world of support from Synertek Systems

From single board computers to single-purpose special usage boards, Synertek Systems offers a growing line of Micromodules that are Motorola EXORcisor™ and Micromodule bus compatible. These boards provide high quality yet are low in cost for maximum utility in any microprocessor application.

Three types of boards are available: CPU and Single Board Computers, Memory Boards, and Peripheral Boards.

Synertek Systems' Development Stations can be utilized for prototyping, product development, and learning. The MDT series is designed for ease of use and easy expansion with our Micromodules. Both a low-cost cassette-based system and a floppy-disk-based system are available.

MBC010 CPU Board
MBC020 CPU/Video Board

DESCRIPTION

The MBC010 and MBC020 CPU Boards provide complete computers on a single board. Both are fully compatible with the Motorola EXORcisor™/Micromodule bus and support RAM, I/O, and analog boards in those families. Both offer a choice of microprocessors — either SY6512 or MC6800 — for use in a full range of systems or development applications.

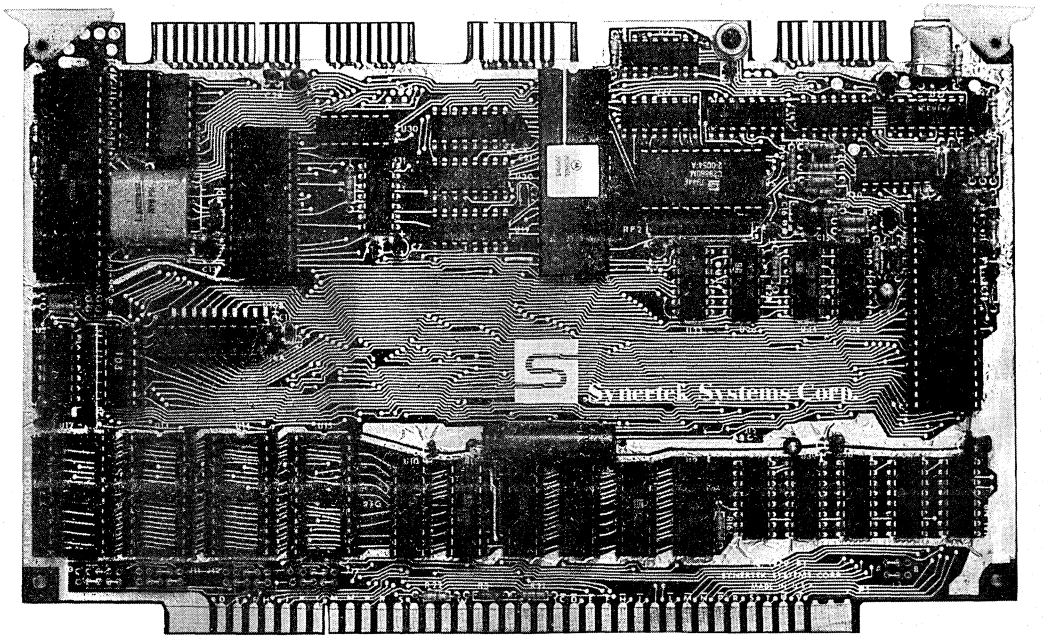
The MBC020 may be used as a cost-effective alternative single board computer, or, with the video circuitry, it can replace two or more boards and operate as the heart of a complete system.

FEATURES

- Choice of Microprocessors — SY6512 (MBC010-65; MBC020-65) or MC6800 (MBC010-68; MBC020-68)
- Fully Buffered Data and Address lines
- 1024 bytes of User RAM
- SY6551 ACIA for RS-232-C Serial Interface with Crystal-Controlled, Programmable Baud Rate
- SY6522 VIA Provides 20 I/O Lines (with 7 lines optionally buffered), and 2 16-Bit Counter/Timers
- Full 65K Programmable Memory Map in 2K Increments, using 32 x 8 Bipolar PROM
- Direct Memory Access (DMA) Controls
- Dynamic Memory Refresh Controls
- Power-on Reset
- MBC020 Includes Complete Video Interface Circuitry for Direct Attachment to a CRT Monitor
- 1 or 2 MHz Versions

Video Features for MBC020

- Dual Intensity Video Levels
- SY6545 Programmable CRT Controller for User Definable Screen Formats
- Light Pen Input
- Composite or Separated Video Outputs



SYSTEMS

SPECIFICATIONS

Power Requirements
+5 VDC @ 1.5 A (max) MBC010
+5 VDC @ 1.75 A (max) MBC020
+12 VDC @ 50 mA (max)
−12 VDC @ 50 mA (max)

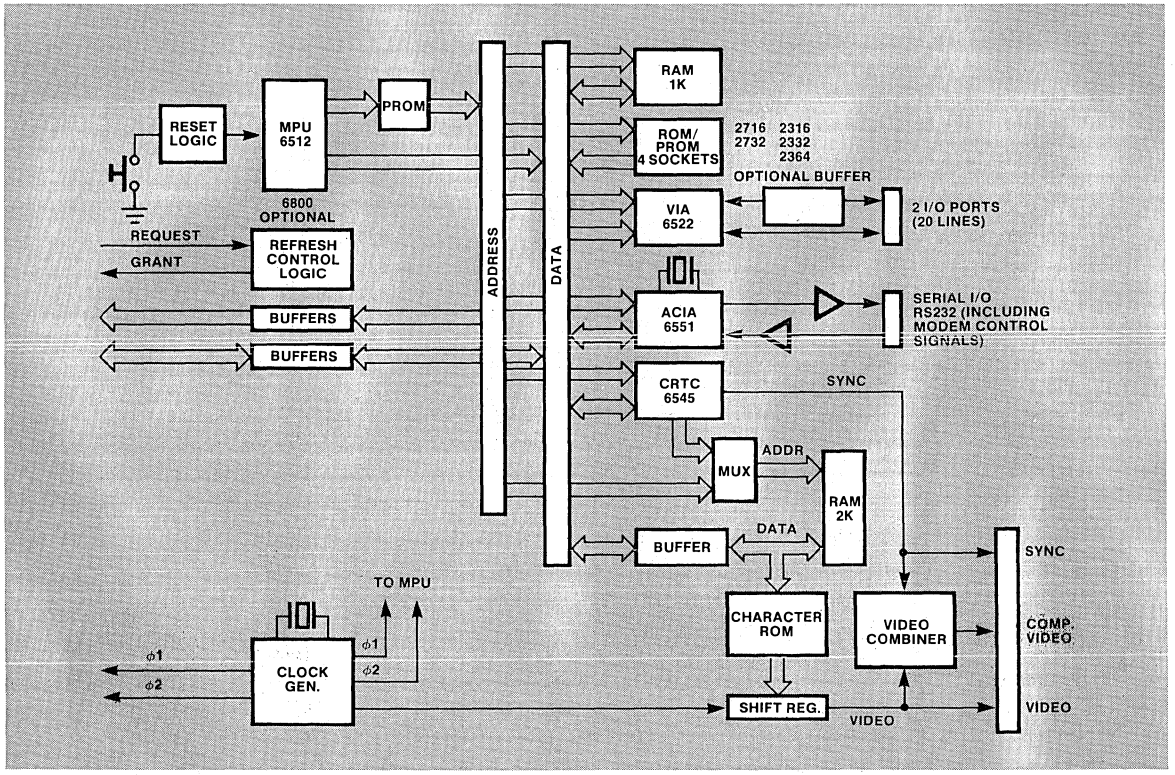
Bus Signals
ADDRESS BUS: Three-state TTL-compatible buffered outputs
DATA BUS: TTL-compatible buffered inputs/outputs
CONTROL BUS:
R/W, VMA, VUA: Three-state TTL-compatible buffered outputs
BA, REF GRANT, MEMCLK, SYNC, Baud Rate: TTL-compatible buffered outputs
$\overline{IRQ}$, $\overline{NMI}$, $\overline{RESET}$, HALT, $\overline{REF\ REQ}$, $\overline{RDY}$, $\overline{DMA}$: TTL-compatible buffered inputs with 3.3K ohm pull-up resistors

Operating Temperature
0°C to 70°C

Physical Characteristics
Width: 9.75 in.
Height: 6.00 in.
Board Thickness: .0625 in.

Connectors
86 pins:
Stanford Applied Engineering SAC-43 D/1-2
50 pins: 3M type 3415-0001
20 pins: 3M type 3461-0001

MBC020 DIAGRAM



MBC01A2 MBC01A2-1 Single Board Computer
Motorola Micromodule Replacement

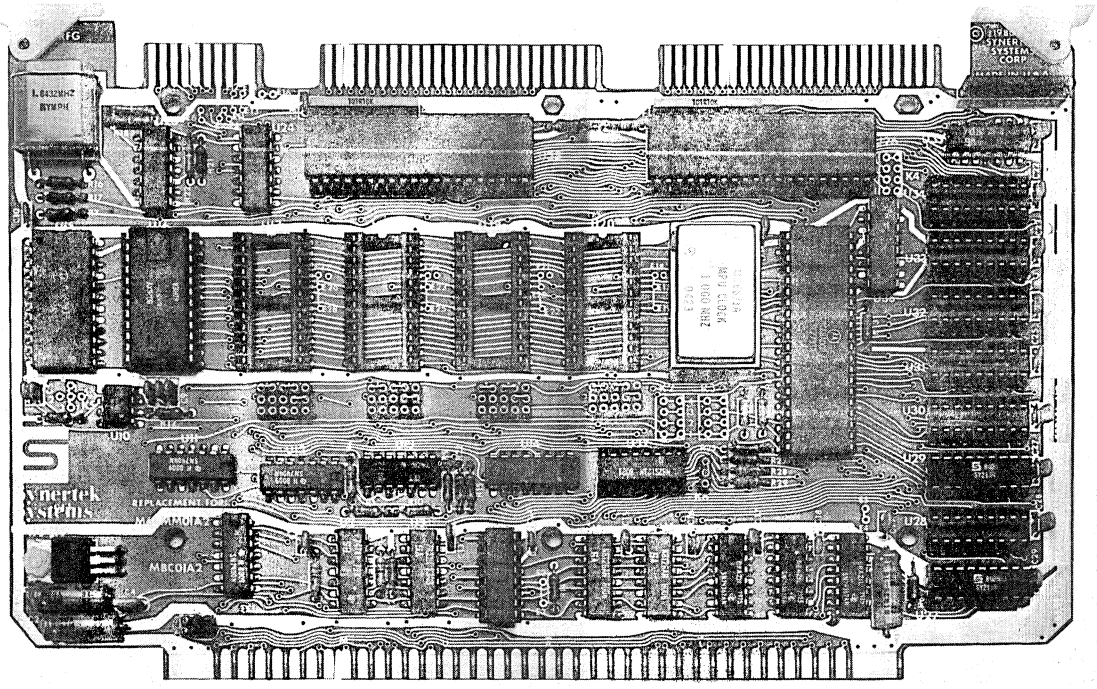
DESCRIPTION

The MBC01A2 board is a direct replacement for Motorola's M68MM01A2 Micromodule. Additional ROM and RAM capacity has been added for increased system requirements. Up to 4096 bytes of static RAM and 32K bytes of ROM can be utilized on the MBC01A2 Micromodule.

The MBC01A2 Micromodule includes a serial communications interface using the MC6850 and two MC6821 PIA's for parallel interfacing.

FEATURES

- Exact Replacement for Motorola M68MM01A2 Micromodule with additional RAM and ROM capacity
- EXORcisor™/Micromodule Bus Compatible
- Serial Communication Port using MC6850 ACIA with RS-232-C interface
- Four Parallel Ports using MC6821 PIA s
- 1 MHz operation (2 MHz available on special order)
- 1024 Bytes of Static RAM with Sockets for up to 4096 Bytes total
- Four ROM/EPROM/RAM Sockets for interfacing with 1K-8K ROM's; 1K-4K EPROMs; or compatible 1K and 2K RAM's
- Power-On Reset Circuitry
- Dynamic Memory Refresh Circuitry
- Four mating connectors supplied with MBC01A2-1



SYSTEMS

MBC01A2 MBC01A2-1 Single Board Computer
Motorola Micromodule Replacement

SPECIFICATIONS

Power Requirements with 1K of RAM and no EPROMs
+5 VDC @ 1.1 A (max)
+12 VDC @ 25 mA (max)
−12 VDC @ 25 mA (max)

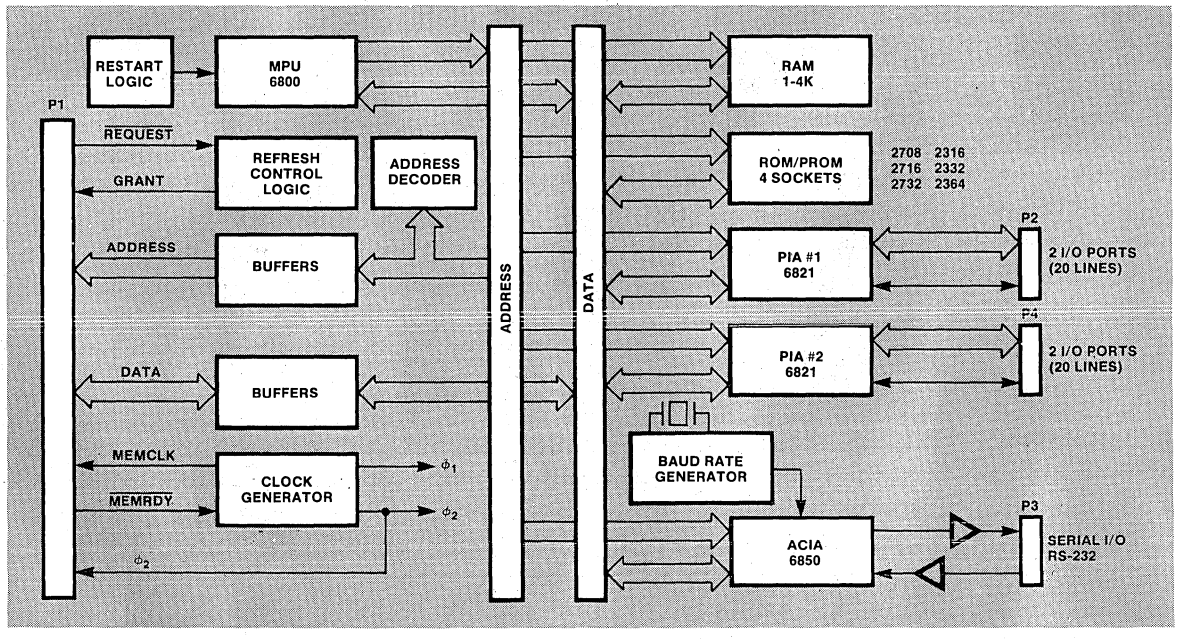
Bus Signals
ADDRESS BUS: Three-state TTL compatible buffered outputs
DATA BUS: TTL-compatible buffered inputs/outputs
CONTROL BUS:
R/W, VMA, VUA: Three-state TTL-compatible buffered outputs
OTHERS:
TTL compatible

Operating Temperature
0°C to 70°C

Physical Characteristics
Width: 9.75 in.
Height: 6.00 in.
Board Thickness: .0625 in.

Connectors
(supplied with MBC01A2-1 only)
86 pins:
Stanford Applied Engineering SAC-43 D/1-2
50 pins: 3M type 3415-0001
20 pins: 3M type 3461-0001

MBC01A2 DIAGRAM



SYSTEMS

MBC008 Static RAM
MBC016 Static RAM

DESCRIPTION

The MBC008/MBC016 Static RAM Modules are directly compatible with Motorola EXORcisor™/ Micromodule bus. The modules include address decoding, write protection, and data buffering circuitry. The MBC008 contains 8K bytes of read/write memory, implemented with 16 SY2114 1024 x 4 static RAM memory devices, while the MBC016 contains 16K bytes of memory, implemented with 32 SY2114 devices. Address select switches allow each 8K memory section to be independently placed in any 8K address range. On the MBC016, each 8K section can be independently write-protected through the write-protect lines.

FEATURES

- Two Speed Versions — 500ns access and 300ns access
- Two Power Versions — 3.5A max. and 2.5A max.
- MBC016 has 16K bytes of Random Access Memory address in 8K sections
- Separate Write-Protect of Each 8K Section of Memory
- Static — No Clocks or Refresh Required
- Single +5V Power Supply Required

SPECIFICATIONS

Power Requirements
+5 VDC @ 3.5A (max.)

Low Power Version:
+5 VDC @ 2.5A (max.)

Operating Temperature
0°C to 70°C

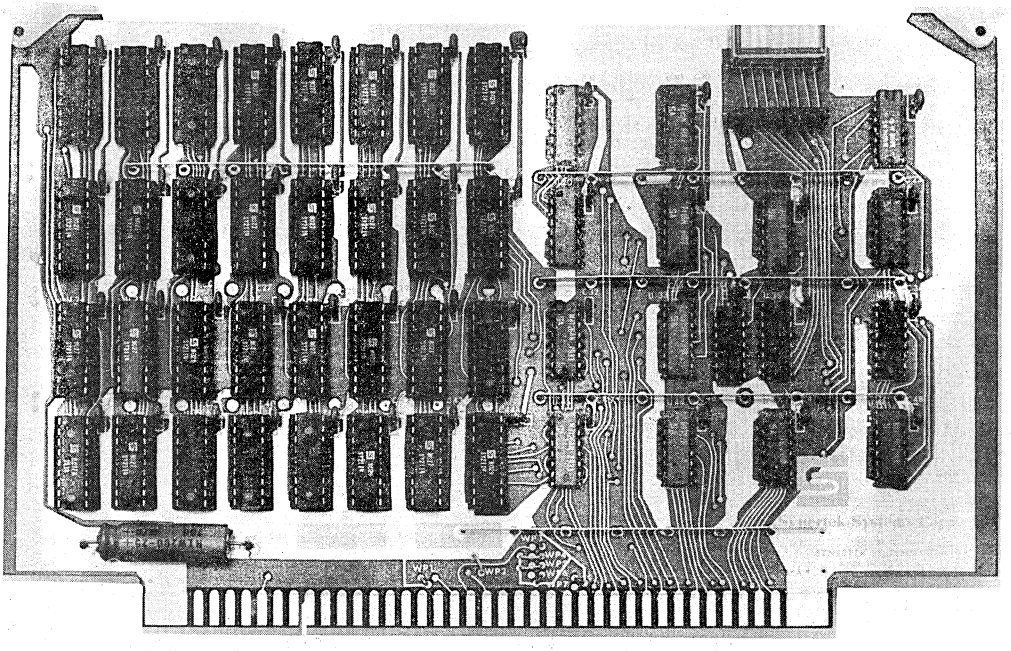
Physical Characteristics

Width:	9.75 in.
Height:	6.00 in.
Thickness:	.0625 in.

Connectors
86 pin — Stanford Applied Engineering SAC-43D/1-2

PART NUMBERS

Power Consumption	Speed-nsec	
	500	300
2.5 Amps (Typ.)	MBC008 MBC016	MBC008-3 MBC016-3
1.75 Amps (Typ.)	MBC008L MBC016L	MBC008L-3 MBC016L-3



SYSTEMS

Dynamic RAM MBC016D Dynamic RAM MBC048D
Dynamic RAM MBC032D Dynamic RAM MBC064D

DESCRIPTION

The Dynamic RAM Boards with hidden refresh are available in 16K, 32K, 48K, and 64K memory arrays in either 1 or 2 MHz versions. Memory refresh is performed on-board during $\phi 1$ when the processor is not accessing memory. On-board circuitry generates and detects even parity through the use of an additional memory bit. Whenever a parity error is detected, a signal is output to the system which is jumper selectable as a parity error or non-maskable interrupt. The memory array can be deselected in 4096 byte blocks to meet any system requirements. As with all SSC Micromodules, the Dynamic RAM Boards are directly compatible with Motorola EXORcisor™/Micromodule bus.

FEATURES

- Available in 16K, 32K, 48K, or 64K Memory Arrays
- 1 or 2 MHz Versions
- Hidden Refresh (without processor interruption)
- Fully Buffered Address, Data, and Control Lines
- Any 4K Block Memory can be Deselected by Jumpers
- 20 Pin Header for Implementation of Priority Interrupts, Multi-Paged Memory, and I/O Systems
- Even Parity Error Checking with Jumper Selectable Output
- Power saving selective refresh during $\phi 1$ of every fourth processor cycle

SPECIFICATIONS

Power Requirements (64K of RAM)
+5 VDC @ 0.7 A (max)
+12 VDC @ .12 A (max.)
−12 VDC @ 8 mA (max)

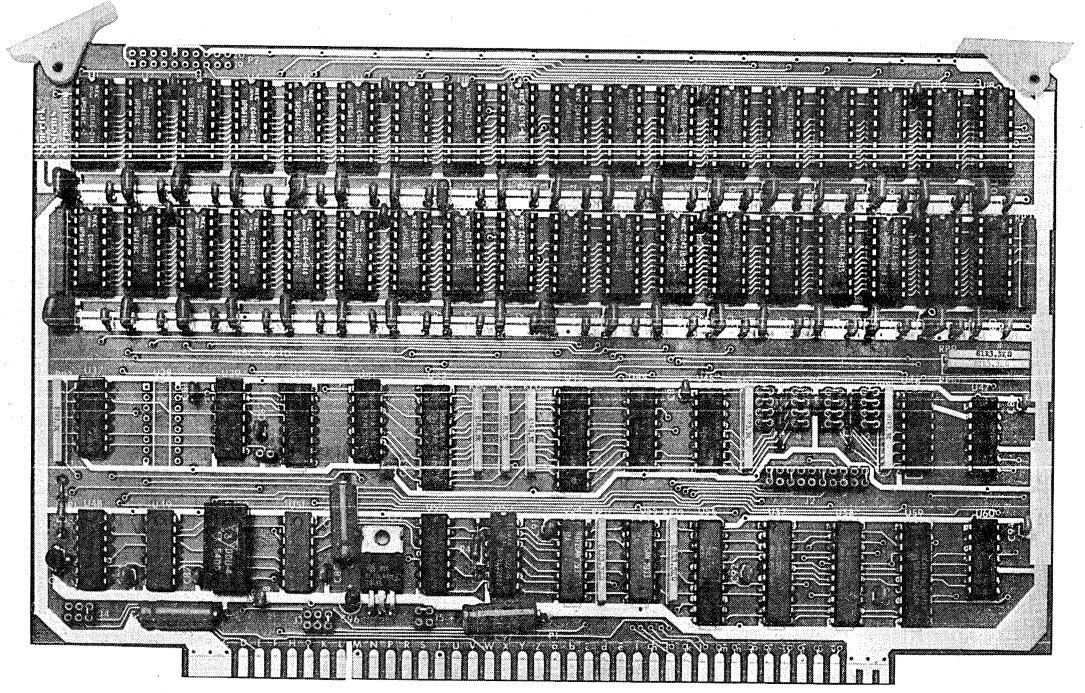
Operating Temperature
0°C to +70°C

Physical Characteristics
Width: 9.75 in.
Height: 6.00 in.
Board Thickness: .0625 in.

Connectors
86 pin:
Stanford Applied Engineering SAC-43D/1-2 or equivalent

Read Access Time
2 MHz operation —
210 ns after leading edge of $\phi 2$
1 MHz operation —
350 ns after leading edge of $\phi 2$

Write Data Available
2 MHz operation —
110 ns after leading edge of $\phi 2$
1 MHz operation —
220 ns after leading edge of $\phi 2$



MBC081 EPROM Programmer MBC092 Extender
MBC091 Prototyping MBC093 Extender

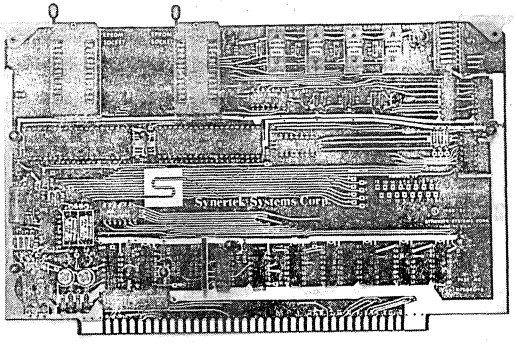
MBC081, MBC081-1
DESCRIPTION

The MBC081 EPROM PROGRAMMER provides two EPROM sockets for copying one EPROM to another, verifying contents of one EPROM against another, or simultaneous programming of two EPROMs.

Programs 2716, 2532, or 2732 EPROMs.

FEATURES

- Two EPROM Sockets, Each Capable of Programming 2716, 2532, and 2732 EPROMs
- On-Board DC to DC Converter Provides +25V Regulated Supply Voltage with Short Circuit Protection
- Address Switch Selectable in 256 Byte Blocks
- MBC081-1 includes special cable for installing board in MDT2000 Micro. Development System



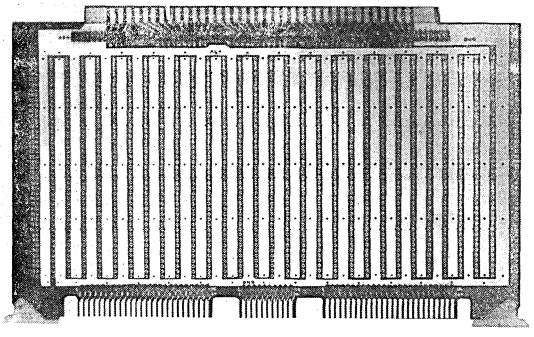
MBC081

MBC091
DESCRIPTION

The MBC091 PROTOTYPING BOARD plugs directly into the standard Micromodule bus and provides space for prototyping user developed circuits. To aid prototyping, ground and power buses are provided with locations for decoupling capacitors.

FEATURES

- Provides Space for Developing Experimental or Custom Circuits
- Standard Spacing for Wirewrap IC Sockets
- One 20-Pin and Two 50-Pin Edge Finger Connectors are Provided at Top of Board
- All Wirewrapping Hardware for Edge Finger Connectors is Provided



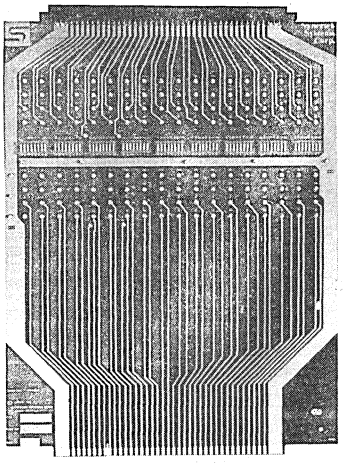
MBC091

MBC092, MBC093
DESCRIPTION

EXTENDER BOARDS are available in two versions. The MBC092 is an extender only, allowing the user access to all points on the circuit board under test. The MBC093, in addition to its role as an extender, also has switches in each line to allow opening selected lines between the board in test and the backplane bus. Labeled test points are also provided between the board in test and the backplane bus for monitoring system signals.

FEATURES

- Useful for Troubleshooting and Testing
- Allows Access to All Points on Circuit Board
- Built-In Test Points and In-Line Switches
- Interfaces with All MBC Boards and Micromodules



MBC093

SYSTEMS

MBC210 Floppy Disk Controller
MBC510 Combo I/O Board

MBC210
DESCRIPTION

The MBC210 FLOPPY DISK CONTROLLER/FORMATTER is an intelligent interface between the Micromodule bus and up to seven floppy drives — four 8" drives and three 5" mini floppies. Sixteen RAM locations provide a control/status block for simplified processor independent interfacing to the MBC210.

FEATURES

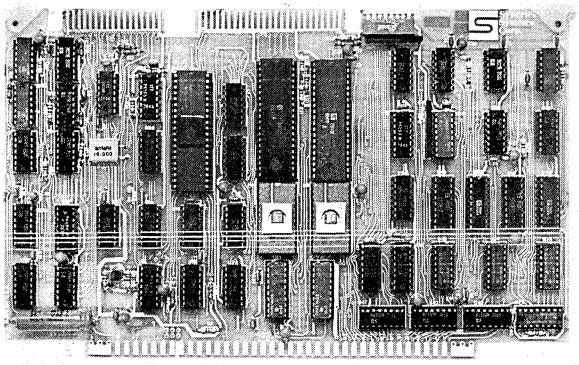
- Handles up to Four 8" Drives and Three 5" Mini Floppies
- Single or Double Sided
- Single or Double Density
- On-Board Processor Controller
- IBM Format Compatible
- On-Board Diagnostics
- Extensive Error/Status Reporting
- Self-Contained On-Board Disk Formatting Software
- Data Transfers, Control and Status Information Communicated through On-Board RAM Buffer/Status Block Providing Processor Independent Interface
- Interrupt and/or Status Bit Buffer Handshaking
- Address Space Switch Selectable on 2K Boundaries
- Simple "Daisy Chain" Drive Connection

MBC510
DESCRIPTION

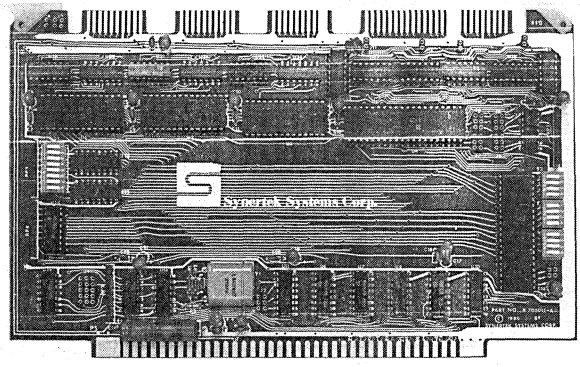
The MBC510 COMBO I/O BOARD provides three serial ports using SY6551 ACIA s with complete RS-232-C compatibility and two parallel ports with buffers and sockets for resistor terminators. The MBC510 also contains four 16-bit counter/timers to provide several operating modes.

FEATURES

- Address Switch Selectable in 256 Byte Blocks
- Two 8-Bit Parallel I/O Ports with Handshake using SY6522 VIA s
- Nibble Programmable with Buffer Option
- Expanded Handshake Capability for Positive and Negative Data Transfer Control
- Sockets for Terminators Provided
- Three Serial Ports using Crystal-Controlled SY6551 ACIA s
- 16 Programmable Baud Rates from 50 to 19.2K Baud
- Full RS-232-C Compatibility



MBC210



MBC510

MDT 2000 Micro Development System for Z8 and SY6500 Processors

DESCRIPTION

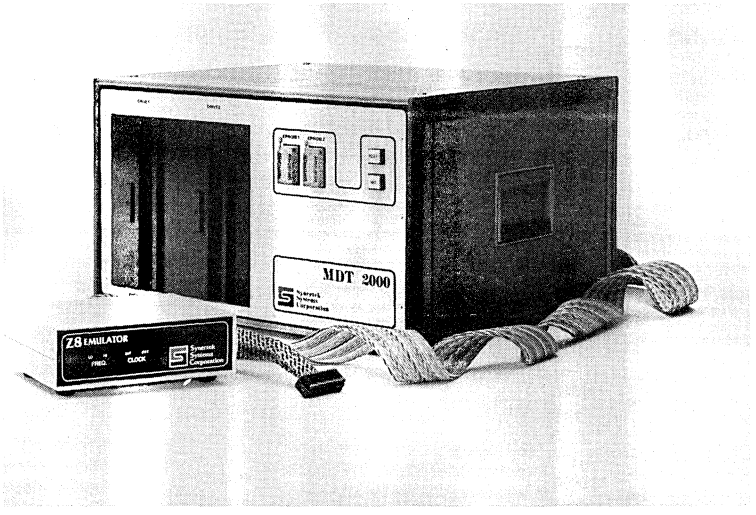
THE MDT 2000 MICRO DEVELOPMENT SYSTEM provides the user with a flexible, powerful, development and emulation system for SYZ8 and SY6500 series microprocessors. Debugging is facilitated with in-circuit emulation which provides a separate and non-conflicting execution environment. Optional Debug (Breakpoint/Trace) boards permit an execution halt, or real-time trace events to be qualified by complex breakpoint conditions. These events can include user-system status.

Emulation control is achieved with a screen-oriented Supervisor which provides various prompting background displays and parameter toggle fields.

Assembly language source and object program generation is supported with a PASCAL-Based Operating System (PBOS). PBOS provides a powerful screen-oriented editor and floppy disk file manager with user-controlled operations on file name families (i.e., wildcards). User-adaptable CRT terminal and printer configuration utilities are available to tailor the system to various terminal and printer characteristics.

A versatile ROM Bootstrap provides power-up access to RAM and/or disk diagnostics, user-controlled booting of PBOS, and an elementary RAM-oriented debugger for pre-disk boot utilization. Remote Communications software (optional) provides access to other systems for terminal interaction or file transfer (binary/ASCII) with error detection and recovery capability.

The intelligent floppy disk controller maintains a log of soft (recoverable) disk errors for user request via a PBOS utility. Self-test of ROM and RAM is automatically performed at power-up and system reset time, and the results are reported.



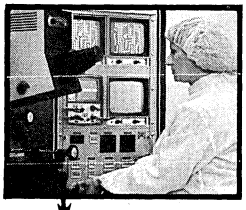
FEATURES

- Supports both SY6500 and SYZ8 Microprocessors
- Supports Up to Three Debug Cards, Providing Four Breakpoint Registers and Trace
- Intelligent Floppy Disk Controller with Two 8" Drives
- Three Serial and One Parallel Interfaces
- PASCAL Disk-Based Operating System with Command Prompting
- Powerful CRT Screen-Oriented Editor
- Versatile Disk File Operations with "Ignore Character" Selection
- Opfional PASCAL Compiler
- Optional Remote Communications Software
- ROM-Based RAM/Disk Diagnostics and Mini-Debugger
- Supports Disk Booting of User-Generated Operating Systems
- Supports Single or Double Density 8" Data Disks
- User Configuration of CRT Terminal/Printer Attributes
- PASCAL Access to Serial or Parallel Printer (mutually exclusive)
- Disk File Hexadecimal Patch Utility
- 230 Volt Option Available
- 2K User RAM (Expandable to 4K) for SYZ8 Internal ROM Emulation Option
- 64K User Dynamic RAM for SY6500 Emulation Option
- Screen Graphics Control of Emulation
- Optional EPROM Programmer Board
- Two Sockets for Programming 2716, 2732, 2532 EPROMs
- Optional Assemblers for 6800, 6809, Z80, 8080, 9900, and LSI-11

Quality Assurance

SAMPLE

STANDARD PRODUCT FLOW



Receiving Inspection

Wafer Fabrication

Electrical Wafer Sort

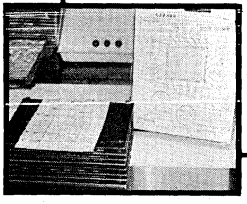
1st Optical Inspection for Sort/Fab Defects Q.A. Gate

Optical Inspection

Saw & Break

2nd Optical Inspection 2nd Optical QA Gate

Die Attach QA Die Attach Monitor



Lead Bond QA Lead Bond Monitor

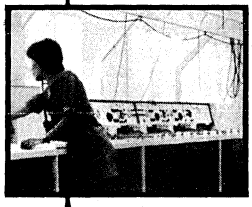
Seal

Hermetic

Stabilization Bake

Temp Cycle

Centrifuge



Tin Plate

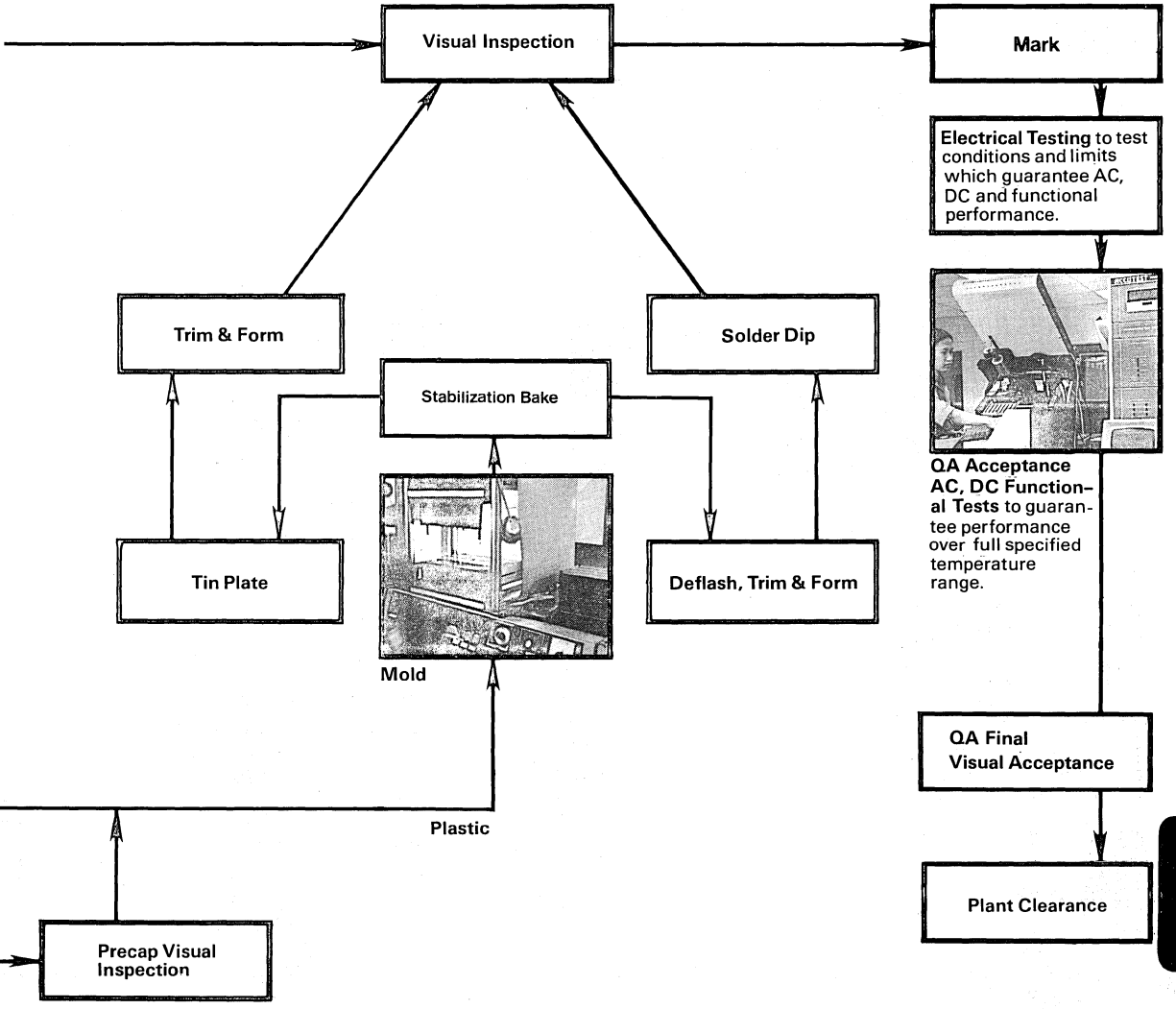
Hermeticity Testing

Lead Trim

QUALITY ASSURANCE

For detailed information on Synertek's Quality Program, contact your local Synertek Representative.

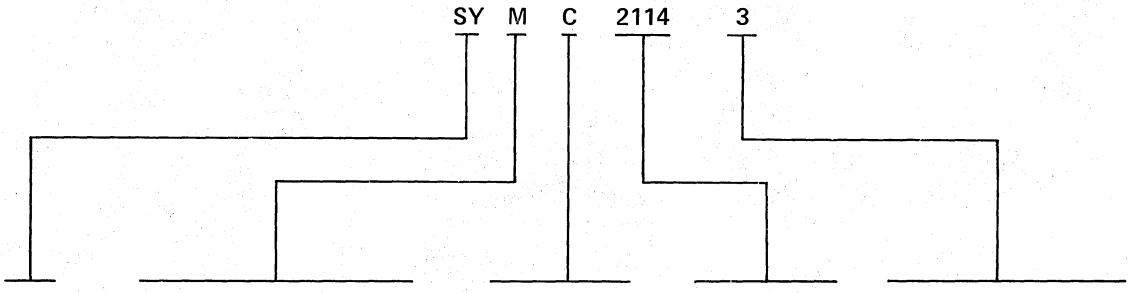
SYNERTEK
A SUBSIDIARY OF HONEYWELL



General Information

SYNERGIE SYNERGIE SYNERGIE

Ordering Information



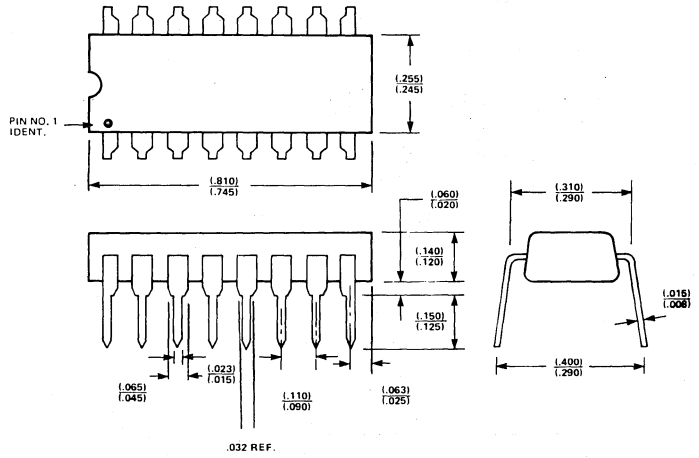
Prefix	Temperature Range	Package Type	4 Digit Device Code	3 Digit Performance or Processing Designator
	No Designator — 0°C to 70°C M — -55°C to +125°C X — Special E — -40°C to +85°C	C - Ceramic P - Molded D - Cerdip X - Dice F - Flat Pac T - TO Can		

For specially programmed devices (ROM's, 6530 Combo, etc.) Synertek will assign a special custom number. This number must be used when ordering these devices.

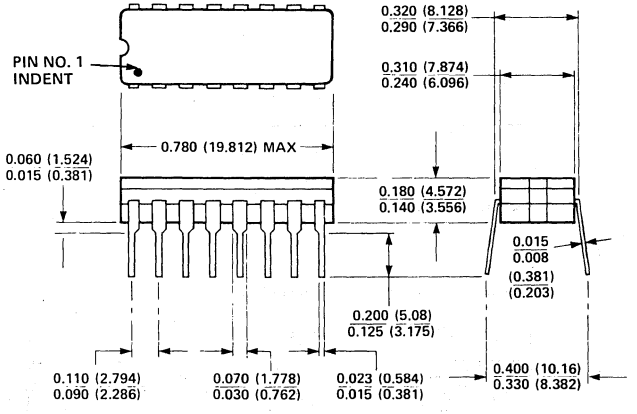
EXAMPLE: SYP 2316B, C28000: 2048 x 8 Read Only Memory, plastic 24 pin Dip, 0°C to +70°C, bit pattern as defined by C28000.

Packaging Information

Plastic Dual In-Line—
16 Leads

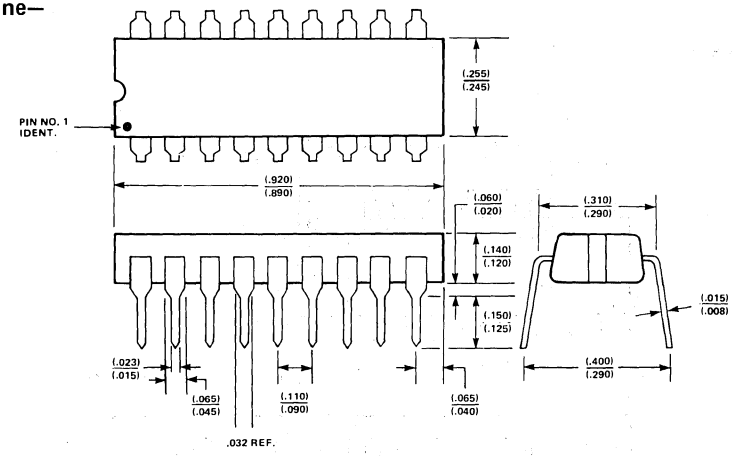


CerDIP—
16 Leads

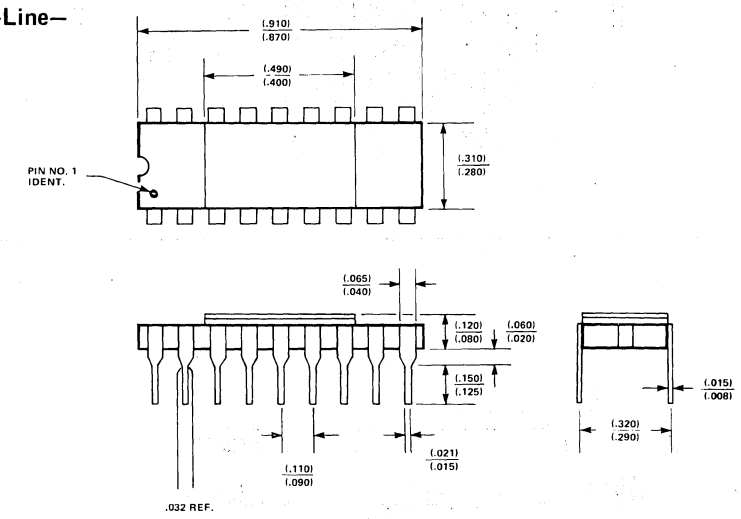


Packaging Information

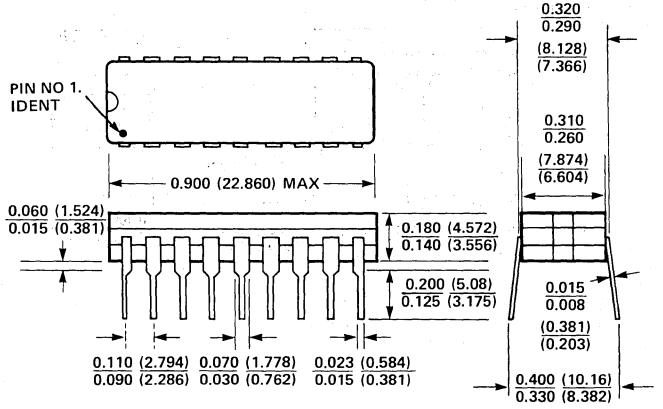
Plastic Dual In-Line— 18 Leads



Ceramic Dual In-Line— 18 Leads



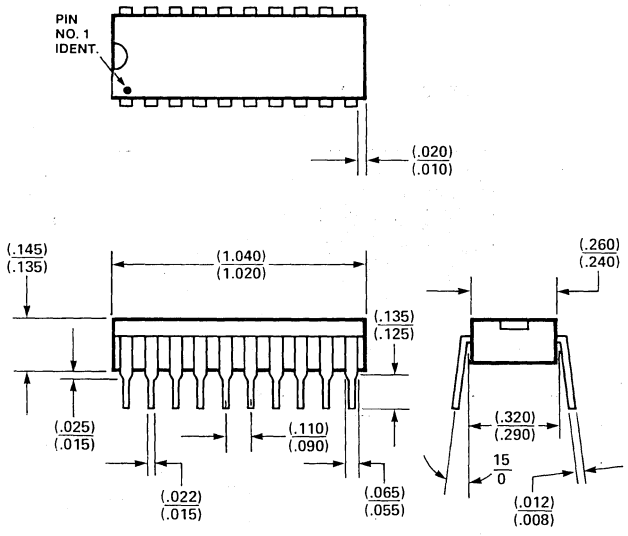
CerDIP— 18 Leads



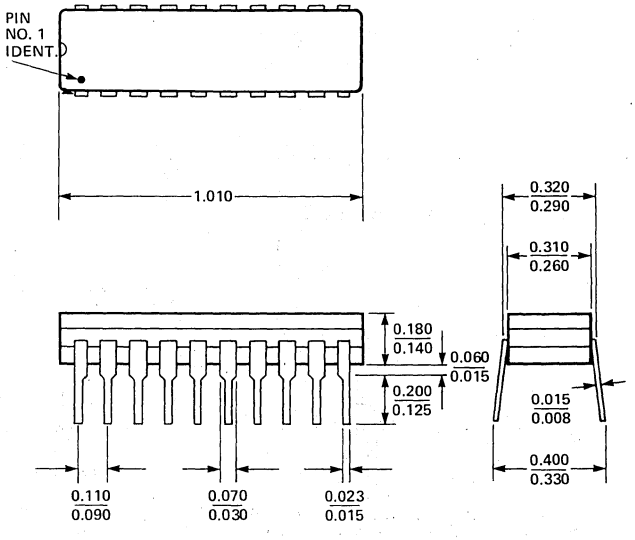
GENERAL

Packaging Information

Plastic Dual In-Line—
20 Leads



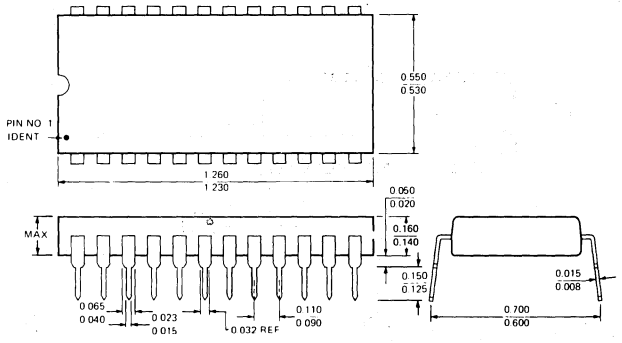
CerDIP—
20 Leads



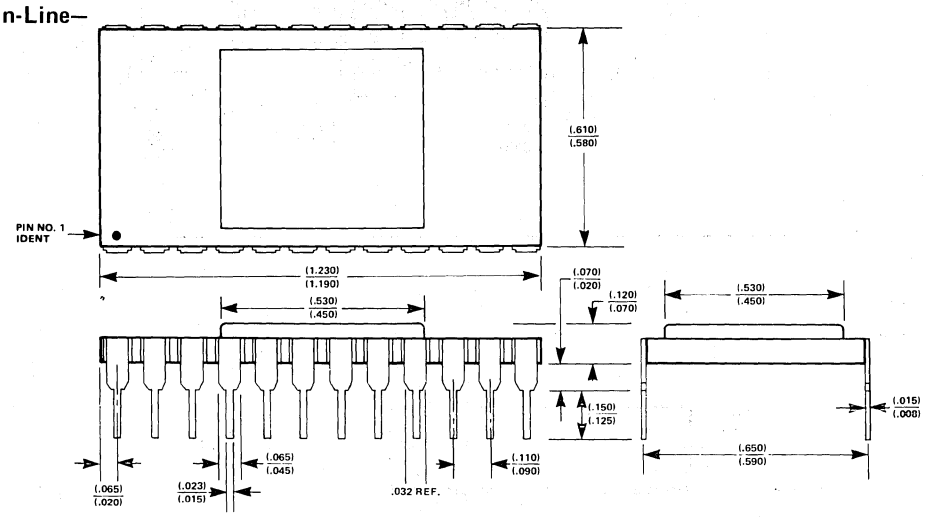
GENERAL

Packaging Information

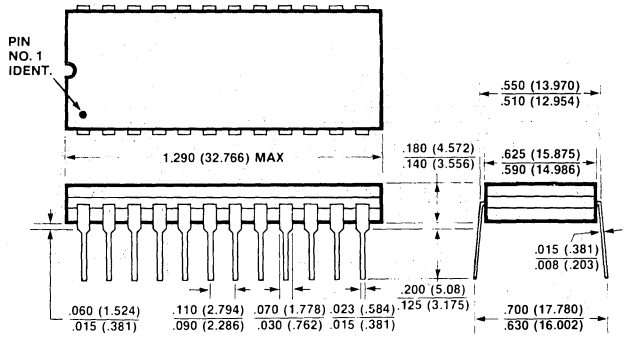
Plastic Dual In-Line—
24 Leads



Ceramic Dual In-Line—
24 Leads



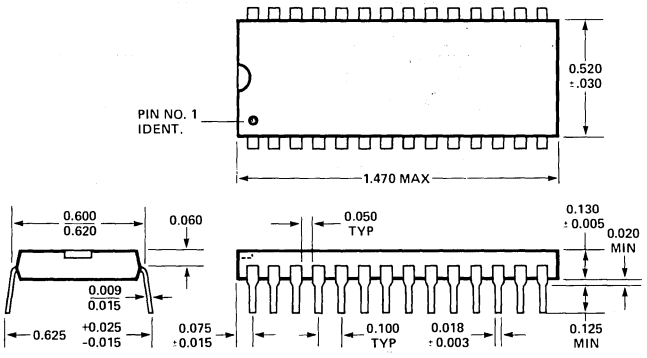
CerDIP—
24 Leads



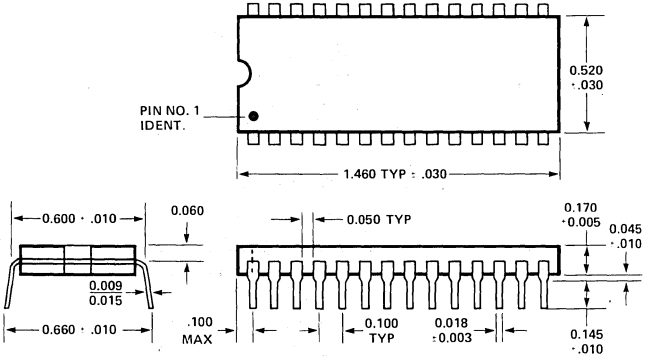
GENERAL

Packaging Information

Plastic Dual In-Line—
28 Leads



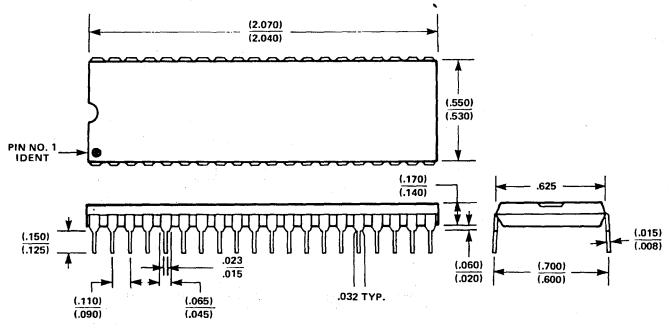
CerDIP—
28 Leads



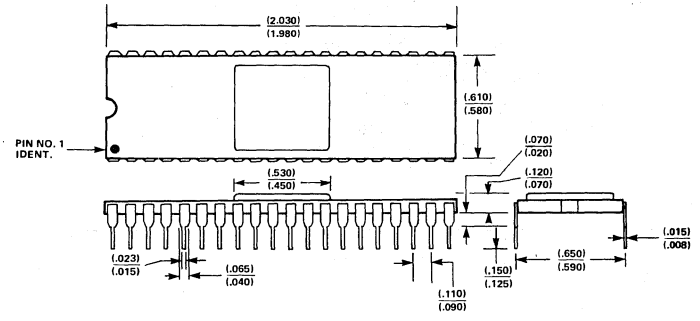
GENERAL

Packaging Information

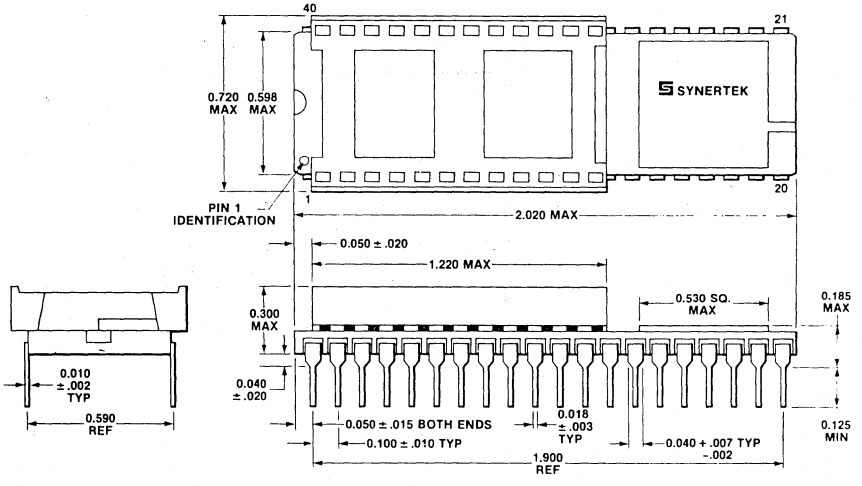
Plastic Dual In-Line—
40 Leads



Ceramic Dual In-Line—
40 Leads



Protopack™ —
40 Leads

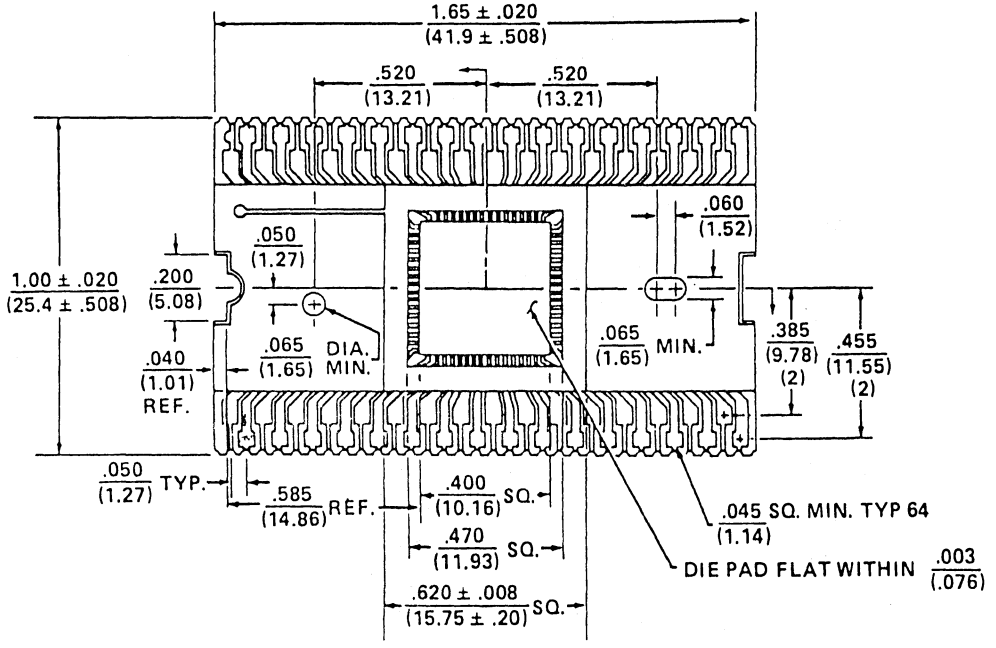


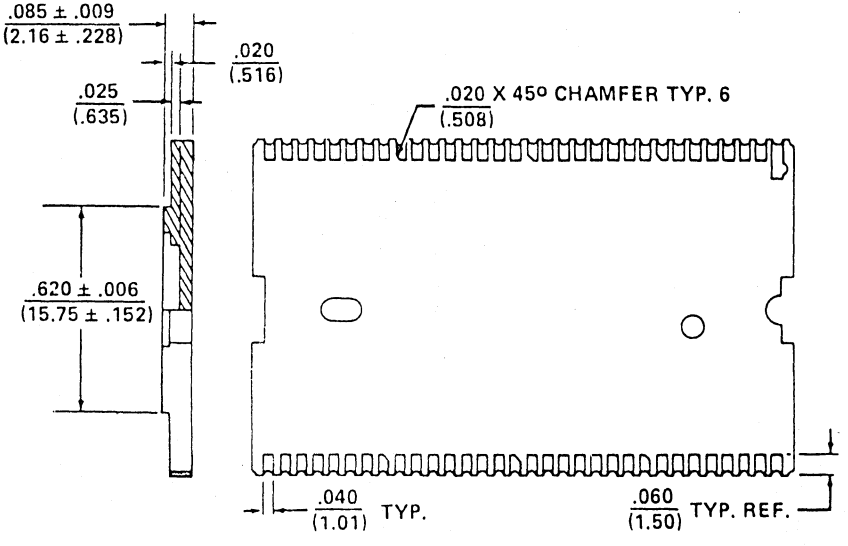
Protopack is a trademark of Zilog, Inc.

GENERAL

Packaging Information

Quad In-Line Package (QWIP)—
64 Leads





Printed in U.S.A. — TMP - 50K - 6/81