# TABLE OF CONTENTS

# PART NUMBER INDEX

# FUNCTIONAL INDEX

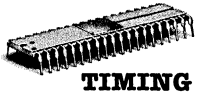
## Data Communication Products

| Part Number | Name | Description | Max Baud Rate | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|
| COM 1553A | MIL-STD-1553A Controller | MIL-STD-1553A Manchester Interface Controller | 1 MB | +5 | 40 DIP/ 44SMT | 35-50 |
| COM 1553B | MIL-STD-1553B Controller | MIL-STD-1553B Manchester Interface Bus Controller/Remote Terminal | 1 MB | +5, −5, +12 | 40 DIP/ 44SMT | 51-66 |
| COM 1671 | ASTRO | Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock | 1 MB | +5, −5, +12 | 40 DIP | 67-82 |
| COM 1863 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin | 62.5 KB | +5 | 40 DIP | 83-90 |
| COM 2017 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (use 8017 for new designs) | 25 KB | +5, −12 | 40 DIP | 91-98 |
| COM 2502 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (use 8502 for new designs) | 25 KB | +5, −12 | 40 DIP | 91-98 |
| COM 2601 | USRT | Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible | 250 KB | +5, −12 | 40 DIP | 99-106 |
| COM 2651 | USART/PCI | Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock | 1 MB | +5 | 28 DIP/ 28 SMT | 107-118 |
| COM 2661-1 -2 -3 | USART/EPCI | Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock | 1 MB | +5 | 28 DIP/ 28 SMT | 119-130 |
| COM 5025 | Multi-Protocol USYNRT | SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection | 1.5 MB | +5, +12 | 40 DIP | 131-142 |
| COM 52C50 | TWINAX | Interface Controller for IBM System/ 34, 36, 38 designated TWINAX or 5250 environment, CMOS | 1 MB | +5 | 28 DIP/ 28 SMT | 143-144 |
| COM 7210 | GPIB Interface | Intelligent Interface Controller for GPIB (IEEE-488-1978) | 8 MHz | +5 | 40 DIP | 145-156 |
| COM 78808 | OCTAL UART | 8 UART's, 8 Baud Rate Generators plus control logic and modem signals all on a single chip | 19.2 KB | +5 | 68 CERDIP LCC | 157-172 |
| COM 8004 | 32 Bit CRC Generator/ Checker | Companion device to COM 5025 Dual 32 bit CRC Generator/Checker | 2.0 MB | +5 | 20 DIP | 173-178 |
| COM 8017 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (compatible with COM 2017) | 40 KB | +5 | 40 DIP | 179-186 |
| COM 8018 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion, margin | 62.5 KB | +5 | 40 DIP | 83-90 |
| COM 81C17 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex with built-in Baud Rate Generator, CMOS | 19.5 KB | +5 | 20 DIP/ 28 SMT | 187-188 |
| COM 8251A | USART | Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit | 64 KB (sync) 9.6 KB (async) | +5 | 28 DIP | 189-204 |
| COM 8502 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (compatible with COM 2502) | 40 KB | +5 | 40 DIP | 179-186 |
| COM 9004 | IBM 3270 Receiver/ Transmitter | IBM 3274 Compatible Receiver/ Transmitter for COAX type "A" protocol (use COM 9064 for new designs) | 2.36 MB | +5, ±12 | 40 DIP/ 44 SMT | 205-212 |

# Data Communication Products CONT.

| Part Number | Name | Description | Max Baud Rate | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|
| COM 9026 | LANC | Local Area Network Controller for token pass systems | 2.5 MB | +5 | 40 DIP/ 44 SMT | 213-228 |
| COM 9032 | LANT | Local Area Network Transceiver | 2.5 MB | +5 | 16 DIP | 229-234 |
| COM 9046 | SSBSS | Single Side Band Speech Scrambler, Low Power, Full Duplex, uses 3.58 MHz TV burst crystal | NA | ±2.6 | 14 DIP | 235-238 |
| COM 90C56[2] | ELANC | CMOS Enhanced Local Area Network Controller, with high throughput, network management and network diagnostic | 5 MBps | +5 | 48 PLCC | 239-240 |
| COM 90C57[2] | NBMU | CMOS Network Buffer Management Unit, to simplify interface of ELANC with dynamic RAM's | 5 Mps | +5 | 24 DIP/ 28 SMT | 241-242 |
| COM 9064 | IBM 3270 | IBM 3270 COAX type "A" controller +5V only version of COM 9004 | 2.36 MB | +5 | 40 DIP/ 44 SMT | 243-250 |
| HYC 9058 | HIT 1 | High Impedance Transceiver for Local Area Networks allows BUS topology with multi drop nodes | 2.5 MBps | +5 | 20 SIP | 251-256 |
| HYC 9068 | LAND | Local Area Network Driver with (93 Ω) line matching impedance for ARCNET networks | 2.5 MBps | +5 | 20 SIP | 257-260 |
| HYC 9078[2] | HIT 2 | High Impedance Transceiver for Local Area Networks for operation at 5MHz | 5 MBps | +5 | 20 SIP | 261-262 |

[2]For future release



# CRT Display

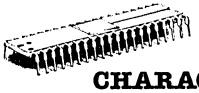
## TIMING CONTROLLERS

| Part Number | Description | Features | Display Format | Max Clock | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 5027 | Provides all of the timing and control for interlaced and non-interlaced CRT display | | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 5037 | | Balanced beam interlace | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 5047 | | Fixed format | 80 column 24 row | 4MHZ | +5, +12 | 40 DIP | 301-302 |
| CRT 5057 | | Line-lock | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 7220A, −1, −2 | Graphics Display Controller | Intelligent graphics display controller | 1024 x 1024 Pixel | 6, 7, 8 MHz | +5 | 40 DIP | 309-332 |
| CRT 9007A, B, C | CRT video processor and controller | Sequential or row-table driven memory programmable DMA | Programmable | A-3.7 MHz B-3.33 MHz C-2.5 MHz | +5 | 40 DIP | 369-388 |
| CRT 97C11[2] | 3rd generation CRT controller which allows manipulation of independent window areas on screen | Control of window size and position, window attributes, prog cursor, max of 127 windows, DRAM refresh | Up to 16K pixels vertical and 1KxN (N = display memory width) in horizontal pixels | TBD | +5 | 68 PLCC | 455-456 |

## VIDEO TERMINAL LOGIC CONTROLLERS

| Part Number | Description | Features | Display Format | Attributes | Max Clock | Power Supply | Package | Page |
|---|---|---|---|---|---|---|---|---|
| CRT 9028/ 9128[1] | Complete CRT video processor and controller. Display and attribute control for alphanumeric and graphics display. Two types of processor interface signals differentiate the two parts. | Separate display memory eliminates contention, smooth scroll, status row, on-board clock, and video shift register. | Mask programmable, 5x8 character font, 8x12 character cell. | Tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics. | 14MHz | +5 | 40 DIP | 401-416 |
| CRT 9053/ 9153[1] | | | Mask programmable, 7x11 character font, 9x13 character cell. | Embedded or tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics. | 18.7MHz | | | 433-448 |

[1]May be custom mask programmed [2]For future release



# CRT Display CONT.

## CHARACTER GENERATORS

| Part Number | Description | Max Frequency | Power Supply | Package | Page |
|---|---|---|---|---|---|
| CRT 7004A[1,4] | 7 x 11 x 128 character generator, latches, video shift register | 20 MHz | +5 | 24 DIP | 303-308 |
| CRT 7004B[1,4] | | 15 MHz | | | |
| CRT 7004C[1,4] | | 10 MHz | | | |

## ROW BUFFER

| Part Number | Description | Max Row Length | Power Supply | Package | Page |
|---|---|---|---|---|---|
| CRT 9006-83 | 8 bit wide serial cascadable single row buffer memory for CRT or printer | 83 characters | +5 | 24 DIP | 363-368 |
| CRT 9006-135 | | 135 characters | | | |
| CRT 9212 | 8 bit wide serial cascadable double row buffer memory for CRT or printer | 135 characters | +5 | 28 DIP | 449-454 |

## VDAC™ DISPLAY CONTROLLERS

| Part Number | Description | Display | Attributes | Max Clock | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 8002H | Provides complete display and attributes control for alphanumeric and graphic display. Consists of 7 x 11 x 128 character generator, video shift register latches, graphics and attributes circuits. | 7x11 dot matrix, wide graphics, thin graphics, on-chip cursor | Reverse video blank blink underline strike-thru | 25 MHz | +5 | 28 DIP | 347-354 |
| CRT 8002A[1,3] | | | | 20 MHz | | | 333-346 |
| CRT 8002B[1,3] | | | | 15 MHz | | | 333-346 |
| CRT 8002C[1,3] | | | | 10 MHz | | | 333-346 |

## VIDEO ATTRIBUTES CONTROLLERS

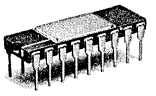
| Part Number | Description | Display | Attributes | Max Clock | Power Supply | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 8021 | Provides attributes and graphics control for CRT video displays | Alphanumeric, wide graphics, thin graphics, on-chip cursor | Reverse video, blank, blink underline, strike-thru | 20 MHz | +5 | 28 DIP | 355-362 |
| CRT 9021B | Provides attributes and graphics control for CRT video displays | Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width | Reverse video, blank, blink underline, intensity | 28.5 MHz | +5 | 28 DIP | 389-400 |
| CRT 9041A, B, C | Provides attributes and graphics control for CRT video displays. Full VT100® and VT220® compatible | Alphanumeric, wide and thin graphics, 4 cursor modes, double height/width, 12 bit shift register | Reverse video, blink, blank, underline, 4 intensity levels | A-33 MHz B-30 MHz C-28.5 MHz | +5 | 40 DIP | 417-432 |

[1]May be custom mask programmed [3]Also available as CRT8002A, B, C-001 Katakana CRT8002A, B, C-003, -018 5 x 7 dot matrix [4]Also available as CRT7004A, B, C -003 5 x 7 dot matrix

VT100 and VT220 are registered trademarks of Digital Equipment Corp.

# Microprocessor Products

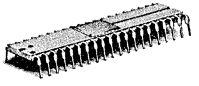
| Part Number | Description | Size | Process | Speed | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| MPU800 | Microprocessor | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 691-714 |
| MPU800-1 | Microprocessor | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 691-714 |
| MPU800-4 | Microprocessor | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 691-714 |
| MPU810A | RAM-I/O-Timer | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 715-726 |
| MPU810A-1 | RAM-I/O-Timer | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 715-726 |
| MPU810A-4 | RAM-I/O-Timer | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 715-726 |
| MPU830 | ROM-I/O | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 727-734 |
| MPU830-1 | ROM-I/O | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 727-734 |
| MPU830-4 | ROM-I/O | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 727-734 |
| MPU831 | I/O | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 727-734 |
| MPU831 | I/O | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 727-734 |
| MPU831-4 | I/O | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 727-734 |



# Baud Rate Generator

| Part Number | Description | Features | Power Supplies | Package | Page |
|---|---|---|---|---|---|
| COM 5016 | Dual Baud Rate Generator | On-chip oscillator or external frequency input (use 8116 for new designs) | +5, +12 | 18 DIP | 265-266 |
| COM 5016T[1] | Dual Baud Rate Generator | External frequency input | +5, +12 | 18 DIP | 265-266 |
| COM 5026 | Single Baud Rate Generator | On-chip oscillator or external frequency input (use 8126 for new designs) | +5, +12 | 14 DIP | 267-272 |
| COM 5026T[1] | Single Baud Rate Generator | External frequency input | +5, +12 | 14 DIP | 267-272 |
| COM 5036 | Dual Baud Rate Generator | COM 5016 with additional output of input frequency ÷ 4 (use 8136 or 81C36 for new designs) | +5, +12 | 18 DIP | 265-266 |
| COM 5036T[1] | Dual Baud Rate Generator | COM 5016T with additional output of input frequency ÷ 4 | +5, +12 | 18 DIP | 265-266 |
| COM 5046 | Single Baud Rate Generator | COM 5026 with additional output of input frequency ÷ 4 (use 8146 for new designs) | +5, +12 | 14 DIP | 267-272 |
| COM 5046T[1] | Single Baud Rate Generator | COM 5026T with additional output of input frequency ÷ 4 | +5, +12 | 14 DIP | 267-272 |
| COM 8046 | Single Baud Rate Generator | 32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply | +5 | 16 DIP | 273-274 |
| COM 8046T[1] | Single Baud Rate Generator | COM 8046 with external frequency input only | +5 | 16 DIP | 273-274 |
| COM 8116 | Dual Baud Rate Generator | Single +5 volt version of COM 5016 | +5 | 18 DIP | 275-276 |
| COM 8116T[1] | Dual Baud Rate Generator | Single +5 volt version of COM 5016T | +5 | 18 DIP | 275-276 |
| COM 8126 | Single Baud Rate Generator | Single +5 volt version of COM 5026 | +5 | 14 DIP | 277-284 |
| COM 8126T[1] | Single Baud Rate Generator | Single +5 volt version of COM 5026T | +5 | 14 DIP | 277-284 |
| COM 8136 | Dual Baud Rate Generator | Single +5 volt version of COM 5036 | +5 | 18 DIP | 275-276 |
| COM 8136T[1] | Dual Baud Rate Generator | Single +5 volt version of COM 5036T | +5 | 18 DIP | 275-276 |
| COM 8146 | Single Baud Rate Generator | Single +5 volt version of COM 5046 | +5 | 14 DIP | 277-284 |
| COM 8146T[1] | Single Baud Rate Generator | Single +5 volt version of COM 5046T | +5 | 14 DIP | 277-284 |
| COM 8156 | Dual Baud Rate Generator | High-frequency clock input version of COM 8116 with additional outputs of input frequency ÷ 2 and ÷ 8 | +5 | 18 DIP | 285-288 |
| COM 8156T[1] | Dual Baud Rate Generator | External clock input version of COM 8156 | +5 | 18 DIP | 285-288 |
| COM 81C66[2] | Timer/Clock Generator | CMOS User Programmable Clock and Timer | +5 | 16 DIP | 289-290 |
| COM 81C66T[2] | Timer/Clock Generator | External Frequency Input version of COM 8166T | +5 | 16 DIP | 289-290 |

[1]May be custom mask programmed [2]For future release



# Keyboard Encoder

| Part Number | No. of Keys | Modes | Features | Standard Fonts Suffix | Standard Fonts Description | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|---|
| KR-9600 XX[1] | 90 | 4 | 2 or N Key Rollover | -PRO<br>-STD | Binary Sequential ASCII | +5 | 40 DIP/ 44 SMT | 665-678 |
| KR-9601 XX[1] | 90 | 4 | 2 or N Key Rollover, caps-lock, -012[1] auto-repeat | -STD<br>-012[2] | Binary Sequential ASCII | +5 | 40 DIP/ 44 SMT | 665-678 |
| KR-9602 XX[1] | 90 | 4 | 2 or N Key Rollover, caps-lock, auto-repeat, serial output | -STD<br>-005[2] | Binary Sequential ASCII | +5 | 28 DIP/ 28 SMT | 665-678 |

[1]May be custom mask programmed [2]For future release

# Floppy Disk/Hard Disk

| Part Number | Description | Sector/ Format | Density | Data Bus | Side/Head Select Output | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|---|
| FDC765A/765-2 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 459-474 |
| FDC7265 | Micro Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 459-474 |
| FDC72C65 | CMOS Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 475-476 |
| FDC72C66 | CMOS Micro Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 475-476 |
| FDC9266 | Floppy Disk Controller/Formatter with data separator, and write precompensation generator | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 523-538 |
| FDC9267 | Floppy Disk Controller/Formatter with high performance analog data separator and write pre-compensation generator | Soft | Double Quad | True | Yes | +5 | 40 DIP/ 44 PLCC | 539-554 |
| FDC9268 | Enhanced Floppy Disk Controller/ Formatter with Data Separator and Write Precompensation Generator | Soft | Double Quad | True | Yes | +5 | 40 DIP/ 44 PLCC | 555-556 |
| FDC9216/B | Floppy Disk Data Separator | Soft/Hard | Double | NA | NA | +5 | 8 DIP | 493-496 |
| FDC9229T/BT | Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double | NA | NA | +5 | 20 DIP/ 28 PLCC | 497-504 |
| FDC92C36/B | Enhanced CMOS Floppy Disk Data Separator | Soft/Hard | Double Quad | NA | NA | +5 | 8 DIP | 505-508 |
| FDC9238/B/BT/T | Enhanced CMOS Floppy Disk Data Separator and Clock Generator | Soft/Hard | Double Quad | NA | NA | +5 | 14 DIP | 509-512 |
| FDC9239B/BT/T | Enhanced CMOS Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double Quad | NA | NA | +5 | 20 DIP/ 28 PLCC | 513-520 |
| FDC92C49 | Analog CMOS Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double Quad | NA | NA | +5 | 24 DIP/ 28 PLCC | 521-522 |
| FDC1791 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | No | +5, +12 | 40 DIP | 477-492 |
| FDC1793 | Floppy Disk Controller/Formatter | Soft | Double | True | No | +5, +12 | 40 DIP | 477-492 |
| FDC1795 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | Yes | +5, +12 | 40 DIP | 477-492 |
| FDC1797 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5, +12 | 40 DIP | 477-492 |
| FDC9791 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | No | +5 | 40 DIP | 557-572 |
| FDC9793 | Floppy Disk Controller/Formatter | Soft | Double | True | No | +5 | 40 DIP | 557-572 |
| FDC9795 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | Yes | +5 | 40 DIP | 557-572 |
| FDC9797 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 557-572 |
| HDC1100-XX | Hard Disk Controller | Soft | Double | True | NA | +5 | 20 DIP | 573-592 |
| HDC7261 | Hard Disk Controller (ST506/SMD) | Soft/Hard | Double | True | Yes | +5 | 40 DIP | 593-594 |
| HDC9223 | Analog Data Separator Support Circuit | Soft | Double | NA | NA | +12 | 14 DIP | 595-598 |
| HDC9224 | Hard/Floppy Disk Controller Up to 4 drives with tape back-up | Soft (ST-506) | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 599-634 |
| HDC9225 | Disk Buffer Management Unit | ST-506 | Double | True | NA | +5 | 48 DIP | 635-646 |
| HDC9226 | Hard Disk Data Separator | ST-506 | Double | NA | NA | +5 | 24 DIP/ 28 PLCC | 647-654 |
| HDC9227 | High Performance Hard Disk And Floppy Disk Data Separators | Soft (ST-506) | Double Quad | NA | NA | +5 | 28 DIP | 655-662 |

# Shift Register

| Part Number | Description | Feature | Max Clock Freq. | Power Supply | Package | Page |
|---|---|---|---|---|---|---|
| SR 5015-80, 81, 133 | Quad Static Shift Register Mask Programmable Length | Load, Recirculate, Shift Controls | 1 MHz | +5 | 16 DIP | 681-684 |
| SR 5017 | Quad 133 Bit | Shift Left/Shift Right, Recirculate Controls | 1 MHz | +5 | 16 DIP | 685-688 |
| SR 5018 | Quad 81 Bit | | | | | |

# SMC CROSS

| Description | SMC Part # | AMI | AMD | Fairchild | General Instrument | Harris | Intel |
|---|---|---|---|---|---|---|---|
| UART (1½ SB)** | COM2017 | S1883* | — | — | AY 5-1013A | — | — |
| UART (1, 2 SB)** | COM2502 | — | — | — | AY 5-1013 | — | — |
| UART (n-Channel)** | COM8017 | S6850* | — | F6850* | AY 3-1015 | HM6402* | — |
| UART (n-Channel)** | COM8502 | — | — | — | AY 3-1015 | HM6403* | — |
| UART (n-Channel)* | COM1863 | S1602* | — | — | — | — | — |
| USRT | COM2601 | S2350* | — | — | — | — | — |
| ASTRO | COM1671 | — | — | — | — | — | — |
| PCI | COM2651 | — | — | — | — | — | — |
| EPCI | COM2661 | — | — | — | AY2661 | — | — |
| USART | COM8251A | — | 8251 | — | — | — | 8251A |
| Multi-Protocc USYNRT | COM5025 | S6852* | — | F3846* F3856* | — | — | — |
| IEEE-488 | COM7210 | — | — | F68488* 96LS488* | — | — | 8291/92* |
| COAX I/F Circuit | COM9004/ COM9064 | — | — | — | — | — | — |
| LAN Controller | COM9026 | — | — | — | — | — | — |
| Dual Baud Rate Gen. | COM5016/36/ COM8116/36 | — | — | — | AY5-8116/36 | — | — |
| Single Baud Rate Gen. | COM5026/46/ COM8126/46 | — | — | F4702* | — | HD4702* HD6405* | — |
| 90 Key KB Encoder | KR9600/01/02 | — | — | — | AY 5-3600* | — | — |
| CRT Controller | CRT5037 | — | — | — | — | — | 8275 |
| Character Generator | CRT7004 | S8564* | — | — | — | — | — |
| Character Generator/ Display Controller | CRT8002 | — | — | — | — | — | — |
| Graphics Controller | CRT7220/ CRT7220A | — — | — — | — — | — — | — — | 82720 — |
| Video Processor and Controller | CRT9007 | — | — | — | — | — | — |
| Video Attributes Controller | CRT9041 | — | — | — | — | — | — |
| Video Terminal Logic Controller | CRT9028/9128 CRT9053/9153 | — | — | — | — | — | — |
| Shift Register | SR5015 | S2182/3/5 | — | — | — | — | — |
| CMOS Microprocessor | MPU800 | — | — | — | — | — | — |
| CMOS RAM-I/O-Timer | MPU810A | — | — | — | — | — | — |
| CMOS ROM-I/O | MPU830 | — | — | — | — | — | — |
| CMOS Input/Output | MPU831 | — | — | — | — | — | — |
| Octal UART | COM78808 | — | — | — | — | — | — |

*Functional equivalent.
**Most UART'S are interchangeable; consult the factory for detailed information on interchangeability.

# REFERENCE GUIDE

| Motorola | National | NEC | Signetics | Solid State Scientific | DEC | Texas Instruments | Western Digital |
|---|---|---|---|---|---|---|---|
| — | MM5303* | — | — | — | — | TMS6011 | TR1602 |
| — | — | — | 2536* | — | — | — | TR1402 |
| MC6850* | NSC858* | — | — | SCR1854* | — | — | — |
| — | — | — | — | — | — | — | TR1983* |
| — | — | — | — | — | — | — | TR1863 |
| — | — | — | — | — | — | — | — |
| — | INS1671 | — | — | — | — | — | UC1671 |
| — | INS2651 | — | 2651 | — | — | — | — |
| MC2661* | — | — | 2661 | — | — | — | — |
| — | INS8251 | μPD8251A | — | — | — | — | TR1983* |
| 2652* | 6852* | — | 2652 | SND5025 | — | — | SD1933* |
| MC6BB488* | — | μPD7210 | — | — | — | TMS9914* | WD9914* |
| — | DP8340/41* | — | — | — | — | — | — |
| — | — | — | — | — | — | — | WD2840* |
| — | — | — | — | — | — | — | BR1941<br>BR1943/4 |
| MC14411* | MM307* | — | — | — | — | — | — |
| — | MM5740* | — | — | — | — | TMS5001 | — |
| MC6845* | DP8350* | — | — | SND5027<br>SND5037 | — | TMS9927 | — |
| MCM66700*<br>MC6570 | DM8678* | — | 2609 | — | — | — | — |
| — | — | — | — | SND8002 | — | — | — |
| —<br>— | —<br>— | μPD7220<br>μPD7220A | —<br>— | —<br>— | —<br>— | —<br>— | —<br>— |
| — | — | — | SCN2674* | — | — | — | — |
| — | — | — | SCN2675* | — | — | — | — |
| — | NS455* | — | — | — | — | — | — |
| — | 5024* | — | 2532* | — | — | TMS3113*<br>TMS3114* | — |
| — | NSC800 | — | — | — | — | — | — |
| — | NSC810A | — | — | — | — | — | — |
| — | NSC830 | — | — | — | — | — | — |
| — | NSC831 | — | — | — | — | — | — |
| — | — | — | — | — | 78808 | — | — |

# FLOPPY DISK/HARD DISK

| Description | SMC Part # | Fujitsu | NEC | Western Digital | Intel | Siemens | Rockwell |
|---|---|---|---|---|---|---|---|
| Floppy Disk Controller | FDC1791-02 | MB8876 | — | FD1791-02 | — | SAB-1791 | — |
| Floppy Disk Controller | FDC1792-02 | — | — | FD1792-02 | — | — | — |
| Floppy Disk Controller | FDC1793-02 | M8877 | — | FD1793-02 | — | SAB-1793 | — |
| Floppy Disk Controller | FDC1794-02 | — | — | FD1794-02 | — | — | — |
| Floppy Disk Controller | FDC1795-02 | — | — | FD1795-02 | — | SAB-1795 | — |
| Floppy Disk Controller | FDC1797-02 | — | — | FD1797-02 | — | SAB-1797 | — |
| Floppy Disk Controller | FDC9791 | MB8876* | — | FD1791-02* | — | SAB-1791* | — |
| Floppy Disk Controller | FDC9793 | M8877* | — | FD1793-02* | — | SAB-1793* | — |
| Floppy Disk Controller | FDC9795 | — | — | FD1795-02* | — | SAB-1795* | — |
| Floppy Disk Controller | FDC9797 | — | — | FD1797-02* | — | SAB-1797* | — |
| Floppy Disk Controller | FDC765A | — | μPD765A | — | 8272A | — | 765A |
| Microfloppy Disk Controller | FDC7265 | — | μPD7265 | — | — | — | — |
| Floppy Disk Controller | FDC765A-2 | — | μPD765A-2 | — | — | — | — |
| Floppy Disk Controller | FDC72C65 | — | μPD72065C | — | — | — | — |
| Microfloppy Disk Controller | FDC72C66 | — | μPD72066C | — | — | — | — |
| Floppy Disk Data Separator | FDC9216 | — | — | FD9216 | — | — | — |
| Floppy Disk Data Separator | FDC92C36 | — | — | FD92C32 | — | — | — |
| Hard Disk Controller | FDC7261A | — | μPD7261A | — | — | — | — |
| Hard Disk Controller | HDC1100-XX | — | — | WD1100-X | — | — | — |
| Universal Disk Controller | HDC9224 | — | μPD7260** | — | — | — | — |

*SMC part will replace cited device with no changes required.
**Functional Equivalent.

# Innovation in Microelectronic Technology is the Key to Growth at Standard Microsystems.



Since its inception, Standard Microsystems has been a leader in creating new technology for metal oxide semiconductor large scale integrated (MOS/LSI) and very large scale integrated (MOS/VLSI) circuits.

Standard Microsystems' COPLAMOS® silicon gate n-channel process, licensed to over 15 prominent semiconductor companies, is the defacto standard for high speed, high density integrated circuits.

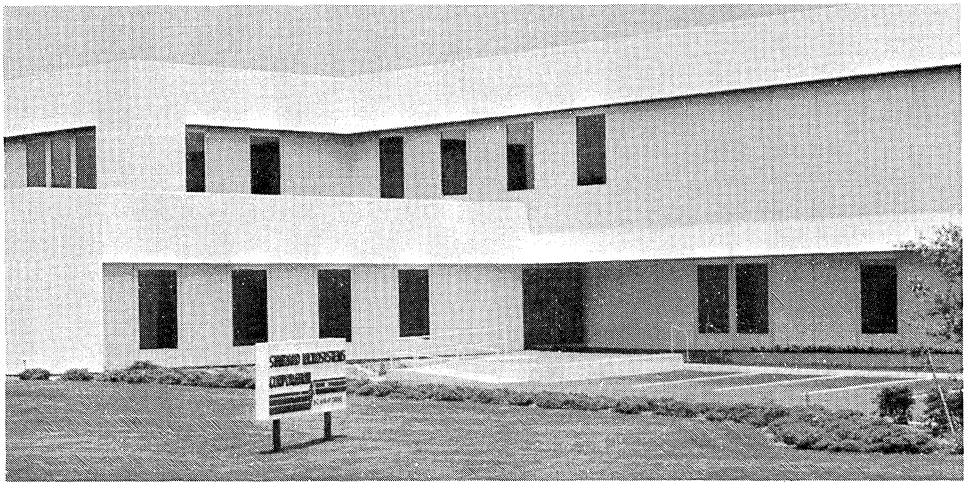
COPLAMOS® utilizes a self-aligned, field-doped, locally oxidized structure to eliminate parasitic currents and shunt capacitance, allowing the tight packing of circuitry essential for VLSI, yet with performance rivaling that of bipolar technologies.

In addition, on-chip generation of substrate bias, also pioneered by Standard Microsystems, when added to the COPLAMOS® technology, results in the ability to design dense, high-speed, low-power n-channel MOS integrated circuits through the use of one external power supply voltage.

Another Standard Microsystems' innovation is the CLASP® process. CLASP® provides a fast turnaround, easily programmable semi-custom LSI technology through the use of ion implantation to define either an active or passive device in the matrix of a memory or logic array. This step is accomplished after all wafer manufacturing steps are performed including metalization and final passivation layer formation. Thus, the wafer can be tested and stored until customer needs dictate the application, a huge saving in turnaround time and inventory costs.

These innovations in both process and circuit technology have received widespread industry recognition. In fact, many of the world's most prominent semiconductor companies have been granted patent and patent/technology licenses covering various aspects of these technologies. The companies include Texas Instruments, IBM, General Motors, ITT, Western Electric, Mostek, Hitachi, Fujitsu, National Semiconductor, Mitsubishi, NEC, AT&T, Data General, and Oki Electric, among others.

Over the past few years, scientists and engineers at Standard Microsystems have been developing a technology to significantly reduce the sheet resistivity of the gate material used in MOS, dramatically decreasing internal time constants in MOS devices.



This technology replaces the polycrystalline silicon normally used in n-channel MOS devices with an alternate material, titanium disilicide. This has enabled Standard Microsystems to become the first semiconductor manufacturer to market and sell MOS/VLSI circuits which employ a metal silicide to replace the conventional doped polycrystalline silicon layer.

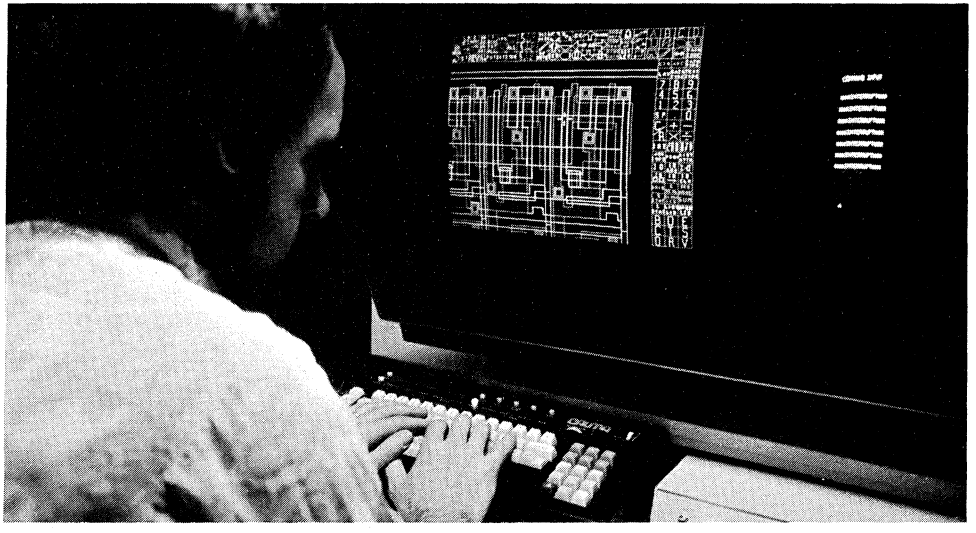
Standard Microsystems is continuing its technological leadership with the introduction of new products utilizing advanced low power n-well and p-well CMOS processes.

# We've Established a Position as the Industry Leader in Microprocessor Peripheral Products with a Steady String of Industry "Firsts".

Innovation at Standard Microsystems extends far beyond new processes. Standard Microsystems has established a position as the industry leader in microprocessor peripheral products with a steady string of industry "firsts".

Standard Microsystems has continually recognized the need for communication controllers to handle the latest data communication protocols. As a result, Standard Microsystems has introduced many new products in the area of data communications. Among these are the COM2601, the first synchronous receiver/transmitter for bi-sync protocols, and the COM5025, the first multiprotocol receiver/transmitter for all standard bit and byte oriented synchronous protocols, including SDLC, HDLC, ADCCP, bi-sync, and DDCMP.

Recognizing the office automation requirement for distributed processing via local area networks, SMC was the first to sell a monolithic VLSI circuit for Local Area Network Control, the industry standard COM9026, a complete controller for token-passing LAN systems. Other areas pioneered by SMC, with the introduction of unique monolithic controllers, include two important IBM families of computers with large installed bases and very high growth rate. The COM9064 is the first single controller for the IBM 3270 Coax Type "A" protocol, while the COM52C50 is the



first and only single chip controller for the IBM System/3x that is commercially available in the market.

SMC also has a first in the area of military standards with the COM1553B controller. This device integrates all the functions necessary to implement the MIL-STD-1553B communication protocol adopted as a standard by the three branches of the military in the U.S.

These data communications firsts offer designers cost effective solutions to the problems of connecting small computers to each other and to Mainframes.

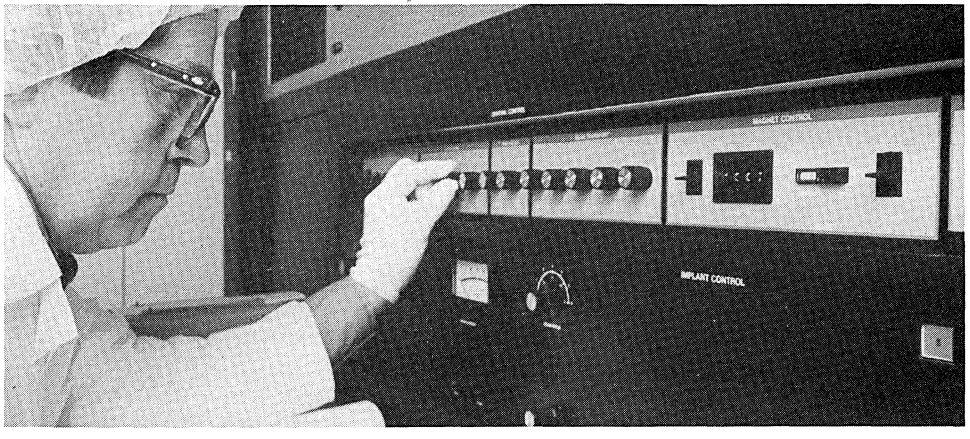
In another area, CRT display systems have traditionally required a great deal of support circuitry for the complex timing, refresh and control functions.

This need led the engineers at Standard Microsystems to develop the CRT5027 Video Timer and Controller (VTAC®), the first CRT controller to provide all of these functions on a single chip. The display, graphics and attributes control functions were then all combined for the first time in the CRT8002 Video Display Attributes Controller (VDAC®).

Another major achievement has been the development of the "next generation" Video Processor And Controller (VPAC®), the CRT9007. Besides replacing up to 80 SSI and MSI TTL devices, the VPAC® is the first CRT controller to provide a hardware solution to many of the software problems of CRT Video Controller design. The CRT9007 is the basis of a complete high performance, low cost, CRT control family, which includes single and double row buffers, and a variety of Video Attribute Controllers utilizing the COPLAMOS® technology to run from 20 MHz to 33 MHz. The various elements of the VPAC® family can be selected to provide the optimal video control solution from low to high end systems.

Most recently, the CRT9028 VTLC and CRT9053 EVTLC have integrated the entire video and attribute control functions, as well as the character generator, all on one VLSI circuit. A complete terminal can be built using these devices with just the inclusion of a RAM and microprocessor.

Standard Microsystems has spearheaded many developments in the rotating memory area as well. Extracting the actual stored data and clock signals from the distorted and jittery signal provided by a floppy disk drive has historically required not only a large number of analog components, but finicky production line adjustments. Both of these problems are solved by SMC products. The FDC9216 Floppy Disk Data Separator provides a revolutionary single chip solution to the data separation problem in a single 8 pin mini-dip package. Utilizing both long-term and short-term timing correctors, the FDC9216 requires absolutely no external components or adjustments. The FDC9229 Floppy Disk Interface Circuit provides, in addition to the digital data separator, a clock generator, precom-



pensation generator, and head load timer. The new FDC9236 and FDC9239 provide even higher resolution data acquisition with the additional benefit of low power CMOS technology. The FDC9236 and FDC9239 are pin for pin replacements for the FDC9216 and FDC9229. SMC's FDC9238 offers high resolution, CMOS technology, and FDC765 compatibility, all in a 14 pin package.

Along with these data separators, Standard Microsystems offers a broad line of floppy disk controllers, including the FDC9266, FDC9267, and FDC9268, which combine the industry standard FDC765A Floppy Disk Controller with a choice of SMC Data Separator/Precompensation Generators, all on one chip. The FDC9266, FDC9267, and FDC9268 provide the highest level of integration in floppy disk control circuits.

The HDC9224 Universal Disk Controller is the first IC to control not only hard disks, but also floppy disks and the tape drives used to back up the disks, as well. In addition, it offers user transparent error detection and correction for up to four 16 head drives.

Hard disk drives suffer from the same signal distortion and jitter as floppy disk drives. SMC provides a choice of Hard Disk Data Separators to solve this problem. The HDC9226 enhances the HDC9224 by providing hard disk data separation with a soft error rate as low or lower than that of the drive itself. The HDC9227 Dual Data Separator includes both a Hard Disk Data Separator and a high resolution Floppy Disk Data Separator on a single chip. Designed for use with either the HDC9226 or HDC9227, the HDC9223 Analog Data Separator Support chip includes all the active analog circuit components needed to form a phase locked loop for performing hard disk data separation.

The HDC9225, when used with the HDC9224, greatly reduces the total number of IC's required by a hard disk control system, while permitting low cost RAMs to be used in a dual-ported configuration to improve system performance.

Achievements like these help keep Standard Microsystems' custom and standard products in the forefront of technology, with increased speeds and densities and a lower cost per function.

# Improvements in Processing and Manufacturing Keep Pace with Advances in Semiconductors.

With the phenomenal growth of the electronics industry, innovation is, of course, highly desirable. But, if the products are to perform as designed, they also have to be reliable.

That's why at Standard Microsystems we take every means to insure the utmost quality and dependability. Consequently, "state-of-the-art" applies not only to our products, but to the way we manufacture them.

In wafer fabrication, the latest equipment and techniques are employed. In addition to conventional processing equipment, we use ion implantation technology extensively. We also use plasma reactors for much of our etching and stripping operations to maintain tight tolerances on process parameters. Perkin Elmer scanning projection printers and TRE mask steppers assure that the critical photolithographic requirements of the latest small geometry processes are met.

Standard Microsystems' commitment to excellence is further demonstrated in the use of the latest Fairchild, Megatest and Genrad testers. Our full service capability lets us make full use of the technologies we develop. We can produce any quantity of semiconductors customers may require. What's more, we can provide our customers with the fast delivery times that they require in today's increasingly competitive environment.

# Standard Microsystems' Custom Capability.



## Custom MOS. A Small Revolution with a Large Impact.

Remarkable advances in semiconductor technology, combined with the availability of quality, low-cost electronics, continue to open new markets for products incorporating micro-electronic components.

Today, metal-oxide semiconductor/large scale integrated (MOS/LSI) circuits are integral components in computers and computer peripherals, automobiles, televisions, electrical appliances, data communications, bank terminals, telephones and a host of other significant applications.

With further applications for large scale integrated and very large scale integrated (VLSI) circuits being discovered every day, one thing is certain. They will have a profound effect on our lifestyle.

## Custom Commitment.

Custom Products has its own management, marketing, and engineering team that is fully dedicated to developing and producing standard cell semicustom and full custom products.

Custom MOS/LSI is a major portion of our business. A sizable portion of all our revenue is a direct result of our custom MOS/LSI projects.

Over the years, Standard Microsystems has developed custom circuits for a wide variety of applications: Computers and computer peripherals, telecommunications and data communications, garage door openers and burglar alarms, electronic toys and games, musical instruments and more. Both over-the-air and cable T.V. systems have made use of our custom circuits. One company's line of word processing equipment makes almost exclusive use of our custom LSI.

As a company committed to serve the custom marketplace, Standard Microsystems has developed the resources and established procedures for MOS/LSI and MOS/VLSI circuit development that enables the company to respond rapidly to growing customer needs.

## The Custom Option.

Standard Microsystems offers two custom design alternatives: fully crafted custom design and cell library based designs. Where reduction of chip size for lowest production pricing in high volume is the dominant factor, the fully crafted design method will provide the best solution. However, development costs and development time will be greatest. Where quick turnaround and reduction of engineering costs are dominant factors then use of our cell library design approach will be the better alternative.

Regardless of the design approach, a custom circuit will provide—

### Lowest Overall Cost.

The overall cost savings realized with custom MOS/VLSI circuitry can be substantial, especially when high-volume production is encountered.

Savings are effected in several ways. Because custom designed circuits contain only necessary components, the cost of unused circuitry on standard microprocessors or integrated circuits is eliminated. Costs for troubleshooting, repair and warranty claims are reduced. In addition, custom MOS can be more economical over SSI and MSI when purchase, inventory and assembly costs are considered. Also, when a system contains a large amount of SSI and MSI, its custom counterpart can significantly reduce power consumption.

### Lowest Parts Count.

There are many applications where a single-package custom LSI or VLSI circuit can outperform a microprocessor and its ROM and RAM circuits while reducing costs. A custom LSI unit can rapidly execute repetitive functions using high speed logic. A microprocessor needs time-consuming algorithms to do the same thing.

### Highest Reliability.

Higher reliability is achieved, especially when replacing circuits that contain significant amounts of SSI and MSI. Fewer parts and solder points reduce the failure rate and raise the reliability. This means low MTTR (mean time to repair), which translates into lower maintenance costs and higher customer satisfaction.

### Minimum Size, Weight, Power Dissipation.

The size and complexity of printed circuit boards are greatly reduced when using a custom circuit. The custom circuit results in a most compact package, specifically designed to perform only the necessary tasks utilizing minimum power and space.

### Unique Proprietary Features.

Proprietary design is another major benefit. It protects your design from would-be copiers because it makes testing and support difficult. This, coupled with the complexity of custom semiconductor fabrication, makes duplicating your custom circuit far less probable.

## A Complete Cell Library Design System for Semicustom LSI/VLSI.

### An idea whose time has come.

To prosper, if not survive, in today's fast-paced electronics industry, you must differentiate your products from the competition.

This means designing in more features, higher reliability and lower power consumption, while reducing size to a minimum. Of course, your next-generation products should also cost less than their predecessors.

Full custom CMOS LSI/VLSI is one way to achieve these goals, but that approach has definite limitations. For example, long development times can upset scheduled product introductions and high development costs can significantly erode profit margins.

Fortunately, the availability of powerful workstations and a new generation of CAD software tools has created a viable alternative: Semicustom LSI/VLSI.

Now, Standard Microsystems Corporation is offering you a complete semicustom design system that combines the advantages of full custom CMOS with rapid turnaround, low cost and virtually guaranteed first-time success.

We call our new system Customation™. It is a "standard cell" design approach that uses a database of proven building blocks and a family of state-of-the-art software tools which enable the engineer to both perform the design and verify it with the utmost speed and precision.

A typical Customation™ design sequence involves the use of a progression of software design tools, with the output of one serving as the input for the next.

Although the designer is constantly monitoring this process, he is not actually "in line". Therefore, problems due to human error are virtually eliminated and you're assured that first silicon is working silicon.

The result? You get the semicustom ICs you need quickly and your development and production costs are reduced.

## Bringing Process, Software and Hardware Together.

### Process technology you can count on.

For over a decade, Standard Microsystems has been at the leading edge of n-channel, silicon-gate process technology. Our patented COPLAMOS® process is used throughout the world and is one of the most widely licensed processes in the semiconductor industry.

Now we've channeled our expertise into a production-proven 3-micron, silicon-gate CMOS process that's compatible with the design rules of several other major semiconductor manufacturers, including NCR Corporation, our contractual alternate source. It's the cornerstone of our Customation™ design system.

### A large, proven cell library.

The Customation™ cell library includes more than 180 cells. Most emulate 74LS logic functions, so your design engineers are already familiar with them. The design system stores the cell layouts, logical models and performance characteristics of each cell in its database. You can feel confident about the performance of these cells, too. They are thoroughly characterized and have been used successfully in numerous applications.

Standard Microsystems is dedicated to incorporating more complex macrocells and supercells into the library. These currently encompass such functions as ROMs, RAMs, and core microprocessors and, in the future, will include data communications functions as well as computer peripheral controllers developed at SMC.

### Industry-standard software.

Customation™ gives you a complete and integrated set of software tools for design, simulation, modeling, checking, and verification test pattern generation.

CUSTOMATION™ is a trademark of Standard Microsystems Corporation

COPLAMOS® is a registered trademark of Standard Microsystems Corporation.

Whenever possible, we've utilized "industry-standard" software that provides a well-proven package of design aids which many of your engineers may already be comfortable using. It can also be licensed through Standard Microsystems.

**A turnkey workstation.**

Standard Microsystems offers a complete turnkey workstation design system that you can use at your own facility. This system, along with SMC's utility software, is optimally configured for semicustom design, combining high performance and ease of operation. We are also constantly enhancing our software to support other workstations and mainframes. Workstations can be acquired directly from the manufacturer or through special arrangement with SMC.

Much of our software already runs on VAX computers. We are currently porting our cell library and software onto several other popular workstations. Please check with us on the status support for your preferred workstation.

## A Design Partnership.

**Comprehensive training.**

Even if you've never had IC design experience, Standard Microsystems can quickly teach you to create cell-based ICs using Customation™.

At our plant on Long Island, we conduct classes for all skill levels, tailoring our instruction to your particular needs and experience level. We cover all phases of design, and you'll work on an actual Customation™ workstation to get hands-on experience and sharpen your design technique. You'll complete the training session ready to produce usable designs utilizing Customation™.

**Do your design work at your place or ours.**

A major benefit of Customation™ is the control it gives you over your design. You work at your own pace—at your own facility, if you wish—verifying the logic through simulation at each step of the way.

We provide everything you need to perform the design from schematic capture through logic simulation and timing analysis.

Once you're satisfied with your design, we'll perform automatic placement and routing from your netlist. We then carry the process through masks, wafers and prototypes.

You also have the option of doing your design work on a workstation located at one of our convenient design centers or having SMC engineers perform the entire design.

**Technical support.**

We offer continuing technical support for our Customation™ users. Our application engineers are experts in the use of the Customation™ design system and can provide prompt assistance from our home office and our regional sales offices. An applications engineer assigned to your program will be available to assist you with any problems that may arise during the course of the development.

Standard Microsystems has developed a particularly strong applications expertise in data communications, video displays, disk controllers, and small computer peripherals and can provide very extensive support in these areas.

**A typical design sequence.**

If needed, you obtain a powerful CAD workstation either from us or directly from the workstation manufacturer.

We teach your design engineers all they need to know about "front-end" design using the Customation™ design system.

You design and verify logic on workstations at your own facility or at our design centers, performing the logic simulations and generating the input and output test vectors.

You submit the resulting netlist to us for layout and post-layout timing parameter extraction.

We perform the chip layout with our cell place-and-route program and return actual layout timing parameters for designer review. You sign off the design only after you are totally satisfied with the final simulations using actual parameters.

We fabricate prototype circuits.

SMC's design engineers can also perform the full design or assume responsibility at any step in the design process.

## Fast Turnaround, Low Cost, Guaranteed Results.

**Working silicon within 8 weeks.**

Fast turnaround is another important benefit of Customation™. We can supply working prototypes within eight weeks of receipt of your signed-off netlist.

Design time and logic simulation is dependent on you, the customer. With an

experienced designer using our Customation™ design system, frontend design should take approximately 4 weeks.*

### Cost-effective chips.

Unit cost depends on a variety of factors: gate count, complexity of interconnect, package cost and performance requirements. A Customation™ design, however, almost always results in a smaller die size than a comparable gate array design. This means lower prices when you get into volume production. Your system will have fewer ICs compared to MSI, gate array, or microprocessor-based designs, resulting in lower assembly and test costs, lower power consumption and enhanced reliability.

SMC will calculate and commit to a production price for your Customation™ chip based on your design specifications. This means that you will know your exact production costs before you undertake the design.

### Second source security.

Standard Microsystems has signed a worldwide, comprehensive agreement with NCR Corporation, providing for the mutual second sourcing and joint development of our CMOS standard cell libraries.

Not only does this agreement assure compatibility at both the process and netlist level, it merges together two of the most innovative and well-respected cell libraries in the semiconductor industry. The common library will be supported on the four leading workstations: Daisy, Mentor, Valid Logic and Metheus/CV.

The agreement also calls for ongoing technical cooperation. Both companies are committed to the enrichment of the cell library through the addition of MSI cells and supercells. Our joint effort will continue with the development of next-generation, fine-line geometry process technologies.

### Guaranteed results.

With Customation™, you're virtually guaranteed first time success. We've designed our system for outstanding accuracy with a number of strategic checkpoints to find and eliminate problems before the circuit is fabricated.

In fact, we guarantee you'll get the results you want by making the following commitment: "Standard Microsystems will bear the cost of any design iteration that is required as a result of an error in cells, utilities and design tools making up the Customation™ system."

## The Full Design Custom Program.

Typically in a custom program where Standard Microsystems performs all of the operations—from design through to finished product—the following sequence applies:

### Evaluation.

The customer's system characteristics are carefully evaluated from the information provided to determine the feasibility of the custom approach, considering such factors as system partitioning, functional performance, operational environment, operating speed, power requirements, process selection, packaging and testing.

After concluding this evaluation, Standard Microsystems will quickly provide a Quotation to the potential customer, which will include—

- a firm development schedule
- the non-recurring engineering charge (NRE)
- a production price schedule

### System Definition.

Once the design is authorized, a thorough specification review takes place between Standard Microsystems' engineers and the customer's engineers. In this critical phase, Standard Microsystems' years of successful design experience are applied as an extension of the customer's design resource in a close working relationship.

### Circuit Design.

Required functions are converted to detailed MOS logic. The logic is verified via advanced logic simulation routines, utilizing our in-house computers, VAX 11/785 and/or breadboard emulators. Circuit simulation is done using SPICE, MOSAID, and Standard Microsystems proprietary software.

### Artwork Generation.

At Standard Microsystems, device layout is a blend of custom "hand-crafting" and sophisticated CAD, using our Calma GDS I and GDS II color graphics systems, to achieve the optimum composite drawing in terms of size and schedule. Check plots are obtained on our Xynetics and Versatec plotters, and advanced design rule checks (DRC) and electrical rule checks (ERC) provide comprehensive artwork verification.

*These design and prototype development cycles are based on a 1600 gate equivalent chip design.

### Mask Fabrication.

Production tooling is obtained from qualified mask vendors to Standard Microsystems' exacting, above-industry standards. Colored overlays of each mask layer are typically used as a final check point.

### Wafer Fabrication.

Standard Microsystems offers a variety of processes, including a CMOS silicon-gate process, and a range of n-channel silicon-gate processes. We will determine the appropriate process to satisfy each customer's cost/performance requirements.

All wafer processing is done in our facilities, utilizing state-of-the art equipment. Standard Microsystems has made substantial investments in projection alignment equipment, direct-step-on-wafer equipment, and advanced ion-implantation, sputtering, deposition and plasma etch equipment.

### Assembly.

Standard Microsystems can provide a wide variety of industry-standard packages, including ceramic, plastic and CERDIP dual-in-line types, flat-packs and chip carriers. The latest in automated equipment, such as our automatic wire bonders, insure high quality and high volume throughout.



SMC PROCESS CHARACTERISTICS

| PROCESS | TYPE | CHANNEL LENGTH | TYPICAL SUPPLY VOLTAGES | MAX. FREQ. | FEATURES/ COMMENTS |
|---|---|---|---|---|---|
| 9000 | n-MOS | 4μ | +5, +12 optional −5, (optional) | 30 MHz | n-channel, si-gate process, moderate to high performance. |
| 10000 | n-MOS | 3μ | +5 | 45MHz | very high performance n-channel process. |
| 20000 | CMOS | 2μ | +5 | 60MHZ | advanced si-gate CMOS process. |
| 30000 | CMOS | 3μ | +3 to +6 | 45MHz | si-gate CMOS process. |

## Customer Owned Tooling.

An area of continuing interest to Standard Microsystems is that of Customer Owned Tooling (COT) or Customer Supplied Tooling (CST). In contrast to a full custom design program where Standard Microsystems is responsible for the MOS design, a COT/CST program is one in which the design function will be completed by the customer or an outside design house.

Many customers find it desirable to develop an in-house LSI design capability, for their internal circuit requirements. Standard Microsystems can provide valuable assistance in achieving this goal.

The customer then provides Standard Microsystems with either a completed composite drawing, a data base tape (in suitable format), or an actual processing mask set.

Whatever the entry level, Standard Microsystems is prepared to carry the program through to completion.

If the design is in the formative stages, the requirements will be studied and the most suitable set of design rules will be provided.

If the design is already completed, Standard Microsystems will examine the design rules used and recommend which of our processes is most compatible. If small variations to our "standard" processing are required, they can usually be accommodated at little or no expense.

Standard Microsystems has developed comprehensive test sites that are incorporated into our masks for the purpose of parametric and quality assurance measurements. Automated equipment collects and stores

measurements from these test sites. If a customer purchases wafers from us, these measurements are provided with the wafers. If a customer chooses to have masks fabricated himself, our test site can be provided for incorporation into the masks.

Standard Microsystems is also prepared to work with customers in establishing a suitable test interface which will enable us to provide the wafer probe and final test operations. Of course, packaging and burn-in are also available.

Whichever approach is taken, Standard Microsystems wants to participate in a partnership that makes best use of our respective areas of expertise. We'll work together to bring the project to completion; on time and on budget.

## Customer Interface.

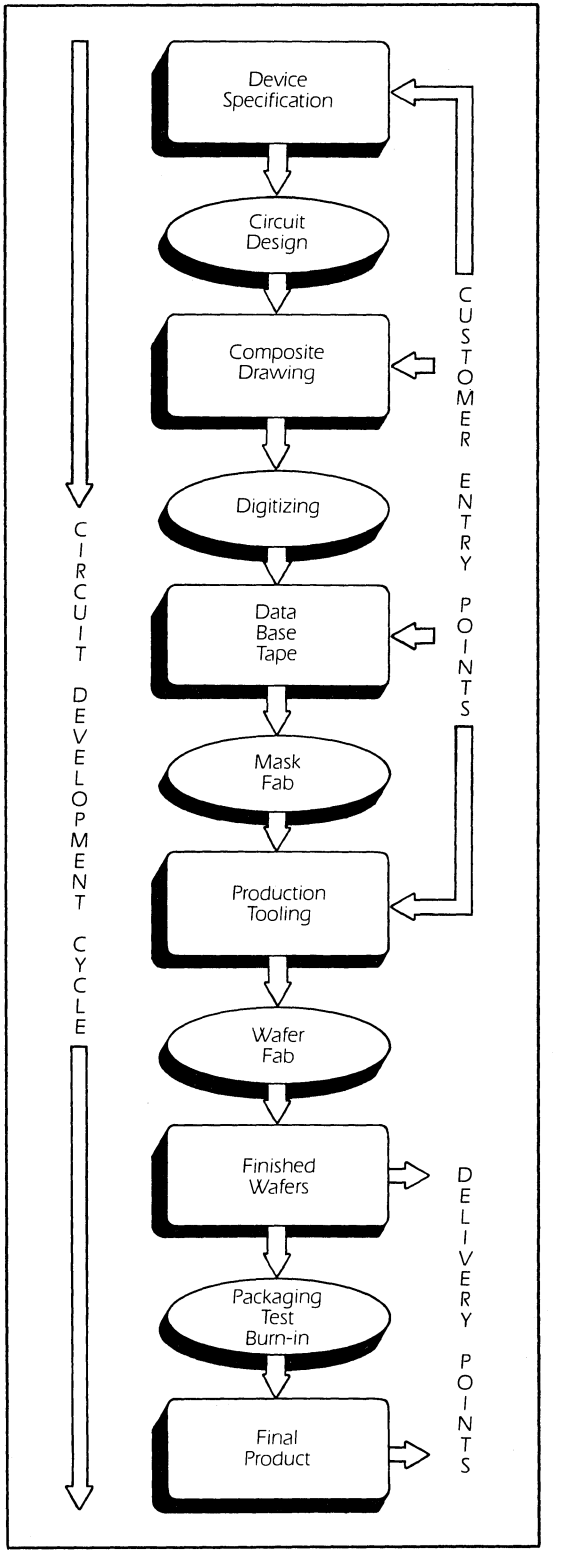
Standard Microsystems is a "full capability" company. We have the resources—an experienced staff and state-of-the-art equipment—to design, process, package and test our Custom MOS circuits.

Our customers are becoming increasingly aware of the benefits of custom circuits in their product lines. They know their products and markets best. Some have developed the technical expertise to perform or participate in the early design phases of a custom program. For this reason, Standard Microsystems offers a variety of customer interface possibilities to serve the broadest possible market.

## Communications: The Key to Custom Development.

On every Custom program, we establish communications with our customers that last throughout the development and production phases.

Our engineers work in an environment that stimulates creativity while encouraging adherence to pragmatic objectives. The status of each program is closely monitored. Strict scheduling, thorough program management and frequent customer contact have become the hallmark of a Standard Microsystems Custom program. Numerous testimonials from satisfied customers give evidence of our ability to perform—to specification and on time.



# STANDARD MICROSYSTEMS CORPORATION

## STANDARD CELL LIBRARY



| Cell Name | Description |
|---|---|
| **Logic Gate Cells** | |
| LS00 | 2-Input NAND Gate |
| LS02 | 2-Input NOR Gate |
| LS04 | Inverter |
| LS08 | 2-Input AND Gate |
| LS10 | 3-Input NAND Gate |
| LS11 | 3-Input AND Gate |
| LS20 | 4-Input NAND Gate |
| LS21 | 4-Input AND Gate |
| LS25 | 4-Input NOR Gate with Strobe |
| LS27 | 3-Input NOR Gate |
| LS28 | 2-Input NOR Gate with Buffer |
| LS30 | 8-Input NAND Gate |
| LS32 | 2-Input OR Gate |
| LS37 | 2-Input NAND Gate with Buffer |
| LS40 | 4-Input NAND Gate with Buffer |
| LS51a | 2-Wide, 2-Input AND-OR-Invert Gate |
| LS51b | 2-Wide, 3-Input AND-OR-Invert Gate |
| LS54 | 4-Wide, 2-Input & 3-Input AND-OR-Invert Gate |
| LS55 | 2-Wide, 4-Input AND-OR-Invert Gate |
| LS64 | 4-2-3-2 Input AND-OR-Invert Gate |
| LS86 | 2-Input Exclusive OR (XOR) Gate |
| LS133 | 13-Input NAND Gate |
| LS134 | 12-Input NAND Gate with Tri-State Output |
| LS260 | 5-Input NOR Gate |
| LS266 | 2-Input Exclusive NOR (XNOR) Gate |
| **Buffer Cells** | |
| LS125 | Non-Inverting Tri-State Buffer |
| LS126 | Non-Inverting Tri-State Buffer |
| LS240 | Inverting Tri-State Buffer |
| LS242 | Inverting Transceiver |
| LS243 | Non-Inverting Transceiver |
| LS244 | Non-Inverting Tri-State Buffer |
| LS245 | Octal Non-Inverting Transceiver |
| LS265a | 1-Input, Dual Complimentary Output Gate |
| LS265b | 2-Input AND Gate w/Complimentary Dual Output |
| LS365 | Hex Non-Inverting Tri-State Buffer |
| LS366 | Hex Inverting Tri-State Buffer |
| LS367 | Quad Non-Inverting Tri-State Buffer |
| LS368 | Quad Inverting Tri-State Buffer |
| **Shift Register Cells** | |
| LS95 | 4-Bit Parallel I/O, Serial Input Left/Right SR |
| LS164 | 8-Bit Parallel Output, Serial Input SR w/Clear |
| LS166 | 8-Bit Parallel/Serial Input, Serial Output SR w/Clear |
| LS178 | 4-Bit Universal Shift Register |
| LS179 | 4-Bit Universal SR with Async. Clear |
| LS194 | 4-Bit Bidirectional Universal SR w/Clear |
| LS195 | 4-Bit Parallel Input/Output SR w/Clear |
| LS198 | 8-Bit Bidirectional Universal SR w/Clear |
| S295 | 4-Bit Universal Shift Register |
| S395 | 4-Bit Universal SR w/Async. Clear, Tri-State Outputs |

| Cell Name | Description |
|---|---|
| **Flip-Flop Cells** | |
| LS73 | J-K Flip-Flop with Clear |
| LS74 | D Flip-Flop with Preset & Clear |
| LS174 | Hex D Flip-Flop with Direct Clear |
| LS175 | Quad D Flip-Flop with Direct Clear |
| LS374 | Octal D Flip-Flop with Tri-State Output |
| LS377 | Octal D Flip-Flop |
| **Latch Cells** | |
| LS75 | Dual Transparent Latch |
| LS77 | Dual Transparent Latch |
| LS100 | Quad Transparent Latch |
| LS116 | Quad Transparent Latch with Clear |
| LS375 | Dual Transparent Latch |
| **Multiplexer/ Selector Cells** | |
| LS151 | 8:1 Multiplexer with Strobe |
| LS152 | 8:1 Multiplexer, Inverting |
| LS153 | 4:1 Multiplexer |
| LS157 | Quad 2:1 Multiplexer |
| LS158 | Quad 2:1 Multiplexer, Inverting |
| LS253 | 4:1 Multiplexer, Tri-State Output |
| LS352 | 4:1 Multiplexer, Inverting |
| LS353 | 4:1 Multiplexer, Tri-State, Inverting |
| **Counter Cells** | |
| LS163a | 4-Bit Syncronous Binary Counter |
| LS169a | 4-Bit Syncronous Binary Up/Down Counter |
| **Decoder/ Encoder Cells** | |
| LS138 | 3:8 Decoder with Enable |
| LS139 | 2:4 Decoder with Enable |
| LS148 | 8:3 Priority Encoder |
| **Comparator Cell** | |
| LS85 | 4-Bit Magnitude Comparator |
| **Arithmetic Operator Cell** | |
| LS83 | 4-Bit Full Adder |
| LS283 | 4-Bit Full Adder |
| LS183 | Full Adder |
| **Parity Generator Cell** | |
| LS180 | 9-Bit Odd/Even Parity Checker |
| **Input/Output Pads– (Individual Gates)** | |
| LS04IP | Inverting Input Pad Buffer |
| LS07IP | Non-Inverting Input Pad Buffer |
| LS74IP | D Flip-Flop Input Pad Buffer (D input only) |
| LS14IP | Schmitt Trigger Input Pad Buffer |
| LS04OP | Inverting Output Pad Buffer |
| LS05OP | Open Drain,Inverting Output Pad Buffer |
| LS07OP | Non-Inverting Output Pad Buffer |
| LS74OP | D Flip-Flop Output Pad Buffer (Q output only) |
| LSBI | Bi-Directional Pad Buffer |

STANDARD MICROSYSTEMS CORPORATION

# STANDARD MICROSYSTEMS CORPORATION

## STANDARD CELL LIBRARY

| Cell Name | Description |
|---|---|
| **Gate Cells** | |
| AND8 | 8 Input AND Gate |
| AOI211 | 2-1-1 AND-OR-Invert |
| AOI22 | 2-2 AND-OR-Invert |
| AOI31 | 3-1 AND-OR-Invert |
| EXNOR | Exclusive NOR Gate |
| EXOR | Exclusive OR Gate |
| HBUF | High Drive Buffer |
| MBUF | Medium Drive Buffer |
| INBUF | Input Buffer |
| INV | Inverter |
| INV3/OUTINV | High Drive INV/Output Buffer |
| IOBUF | Input/Output Buffer |
| DLYCEL | Delay Cell |
| LS125 | Non-Inverting Tri-State Buffer |
| LS240 | Inverting Tri-State Buffer |
| LS242 | Inverting Transceiver |
| NAN2 | 2 Input NAND Gate |
| NAN3 | 3 Input NAND Gate |
| NAN4 | 4 Input NAND Gate |
| NAN5 | 5 Input NAND Gate |
| NOR2 | 2 Input NOR Gate |
| NOR3 | 3 Input NOR Gate |
| NOR4 | 4 Input NOR Gate |
| OR8 | 8 Input OR Gate |
| OAI31 | 3-1 OR-AND-Invert |
| INVT | Inverting Tri-State Driver |
| TBUF | Non-Inverting Tri-State Driver |
| **Latch & Flip-Flop Cells** | |
| CCND | Cross Coupled NAND Latch |
| CCNR | Cross Coupled NOR Latch |
| DFF | D Flip Flop |
| DFFR | D Flip Flop with Reset |
| DFFRS | D Flip Flop w/Set & Reset |
| JKFF | J-K Flip Flop |
| LAT | Transparent Latch |
| LATBUF | Tri-Statable Transparent Latch |
| LATR | Transparent Latch with Reset |
| LS74A | D Flip Flop with Set & Reset |
| LS76A | J-K Flip Flop |
| LS100 | Quad Transparent Latch |
| LS116 | Quad Transparent Latch w/Clear |
| LS175 | Quad D Flip-Flop w/Direct Clear |
| LS164 | 8-Bit Parallel Output, Serial Input SR w/Clear |
| LS194 | 4-Bit Bidirectional Universal SR w/Clear |
| SRBN | Shift Register |
| UDC | Up/Down Counter |
| PCL2 | Two Phase Clock |
| **Multiplexer Cells** | |
| MUX2 | Multiplexer Cell |
| LS151 | 8:1 Multiplexer with Strobe |
| LS153 | 4:1 Multiplexer |
| **Decoder/ Encoder Cells** | |
| LS138 | 3:8 Decoder with Enable |
| LS139 | 2:4 Decoder with Enable |

| Cell Name | Description |
|---|---|
| **Counter Cells** | |
| LS163A | 4-Bit Syncronous Binary Counter |
| LS169A | 4-Bit Syncronous Binary Up/Down Counter |
| **Arithmetic Operator** | |
| LS83 | 4-Bit Full Adder |
| LS85 | 4-Bit Magnitude Comparator |
| **Analog Cells** | |
| ANSW | Analog Switch |
| DS1218 | Schmitt Trigger (1.2-1.8V) |
| DS1238 | Schmitt Trigger (1.2-3.8V) |
| DS1323 | Schmitt Trigger (1.3-2.3V) |
| DS1527 | Schmitt Trigger (1.5-2.7V) |
| DS1728 | Schmitt Trigger (1.7-2.8V) |
| DS2028 | Schmitt Trigger (2.0-2.8V) |
| DS2232 | Schmitt Trigger (2.2-3.2V) |
| OSCP | General Purpose Oscillator |
| POR | Power On Reset |
| VCM1 | Voltage Reference (50uA) |
| VCM2 | Voltage Reference (100uA) |
| VCM3 | Vottage Reference (200uA) |
| OPAMP | General Purpose Operational Amplifier |
| COMP05 | High Speed Low Power Comparator |
| COMPG | General Purpose Comparator |
| **Pad Cells** | |
| INPD | Input PAD |
| IOPD2S | 2mA Split P-Channel I/O PAD |
| IOPD4 | 4mA Input/Output PAD |
| IOPD4S | 4mA Split P-Channel I/O PAD |
| IOPD8 | 8mA Input/Output PAD |
| IPPD4 | Input PAD with 400uA Pullup |
| IPPD8 | Input PAD with 800uA Pullup |
| ODPD4 | 4mA 5V Open-Drain Output PAD |
| ODPD8 | 8mA 5V Open-Drain Output PAD |
| ONPD4 | 4mA 7V Open-Drain Output PAD |
| ONPD8 | 8mA 7V Open-Drain Output PAD |
| OPD4 | 4mA Output PAD |
| OPD8 | 8mA Output PAD |
| OPPD4 | 4mA Tri-State Output PAD |
| OPPD8 | 8mA Tri-State Output PAD |
| PU30 | P-Channel Pullup |
| PD30 | N-Channel Pulldown |
| **Supercells** | |
| ROM Supercell | Modular ROM (512 bits) |
| RAM Supercell | Modular RAM (512 bits) |
| TIMER I Supercell | 16-Bit Counter/Timer |
| 65CX02 Supercell | 8-Bit Core Microprocessor |
| ATOD Supercell | 8-Bit Analog to Digital Converter |
| SCC Supercell | Serial Communication |
| BRG Supercell | Baud Rate Generator |
| VCO Supercell | Voltage Controlled Oscillator |

STANDARD MICROSYSTEMS CORPORATION

STANDARD MICROSYSTEMS CORPORATION



# Quality Assurance and Quality Control

Volume manufacturing of quality products requires a rigorous commitment on behalf of STANDARD MICROSYSTEMS and all of its employees. Each phase of the operation from design to shipping must adhere stringently to documented procedures which have produced a product of proven reliability.

The design of a reliable product is assured by adherence to tested and proven design rules. Any change in design rules must be evaluated using a design-rule test vehicle. Each new product is evaluated first by prototype wafer runs and thorough preliminary production and device characterization.

Manufacturing flow is monitored by Quality Control to insure that parameters meet specifications on incoming material, within the line and at outgoing inspection. Clean room standards, calibration and work methods are also monitored.

The Quality Assurance Department is the customer representative with the primary responsibility of evaluating product to current industry standards and related responsibilities of evaluating developmental processes, product and the standards themselves.

The following is a more detailed description of the types of screening performed and how SMC is organized to produce quality products.

## 1.0 Scope

The measures taken by SMC to produce reliable integrated circuits and the assembly/screening options available to the customer are given in this section.

## 2.0 Approach

Factors relating to quality and reliability are discussed in the following order: package options, screening, process control, test and characterization, quality conformance/reliability testing, and failure analysis.

## 3.0 Applicable Documentation

SMC internal specifications define every phase of production and must be approved by the designated representatives of Engineering, Manufacturing, Processing, Quality Control and Quality Assurance departments.

### 3.1 Design Rules (DR-XX)

3.1.1 Geometric design rules define layout considerations, alignment structures, critical-dimension targets, and input-protection networks.

3.1.2 Electrical design rules define performance criteria, measurement methods, device parameters, and process parameters.

### 3.2 Purchase Specifications (PS-XX)

All critical material is purchased to SMC specifications from qualified vendors.

### 3.3 Process Specifications (WX-XX, AX-XX)

3.3.1 The procedures used for wafer processing and assembly of microcircuits are fully documented.

### 3.4 Quality Control Procedures (QC-XX)

QC procedures define the sampling techniques, accept/reject criteria and test methods used in quality audits.

### 3.5 Quality Assurance Procedures (QA-XX)

QA procedures define methods for product/process qualification, reliability testing and failure analysis.

### 3.6 Military Standards and Specifications

| | |
|---|---|
| MIL-C-45662 | Calibration System Requirements |
| MIL-I-45208 | Inspection System Requirements |
| MIL-M-38510 | General Specification for Microcircuits |
| MIL-M-55565 | Packaging of Microcircuits |
| MIL-STD-105 | Sampling Procedures and Tables for Inspection by Attributes |
| MIL-STD-883 | Test Methods and Procedures for Microelectronics |
| MIL-STD-1331 | Microelectronics Terms and Definitions |

## 4.0 Package Options, Features

### 4.1 Ceramic (no suffix)

Gold plating on external leads and die cavity, gold eutectic die attach.

### 4.2 Cerdip (Suffix "CD")

Meets MIL-STD-883 internal moisture content requirements of Method 5005. Substrate connections are made through jumper chips, gold eutectic die attach.

### 4.3 Plastic (Suffix "P")

The plastic used is a B-type epoxy or an approved advanced type having a better resistance to a humid environment.

## 5.0 Screening Options

### 5.1 High-Reliability Screening

The routing is as defined in MIL-STD-883 Method 5004 for Class B product. Periodic Quality Conformance data (para. 9.2) is taken on generically similar parts. A sample flow chart for ceramic product is given on page 30.

5.1.1 Internal Visual

Both Die and Preseal Visual inspections are to the criteria of Method 2010, Condition B of MIL-STD-883. An AQL audit is performed on each lot by Quality Control.

5.1.2 Stabilization Bake

All parts are given the stabilization bake according to Method 1008, Condition C of MIL-STD-883.

5.1.3 Temperature Cycling

All parts are subjected to 10 cycles of −65°C to + 150°C per Method 1010, Condition C of MIL-STD-883.

5.1.4 Constant Acceleration

All parts are subjected to a 30,000 g force in the Y1 orientation per Method 2001, Condition E.

5.1.5 Seal

Hermeticity testing is performed to conditions A and C of MIL-STD-883 Method 1014.

5.1.6 Pre burn-in Electrical Test.

Ordinarily this is the same as final electrical test.

5.1.7 Burn-in

Condition A and Condition D of MIL-STD-883 Method 1015 are available. The stress is applied for 160 hours at 125°C or at other temperatures according to the time-temperature regression.

5.1.8 Final Electrical Test

Verifies functional and parametric performance to the device specifications.

5.1.9 Final Visual Inspection

All parts are inspected to Method 2009 of MIL-STD-883.

### 5.2 Standard Screening

Standard Screening is designed for the industrial-commercial customer and is available in all package types. For hermetic packages, temperature cycling, centrifuge and hermeticity are specified as well as die, preseal, and final visual inspection.

5.2.1 Standard Die and Preseal Visual Inspections (AC-04, AC-08, AD-04, AD-09, AP-98, AP-92, QC-32, QC-33)

These inspections were developed from Method 2010 of MIL-STD-883. The inspection criteria are specific to SMC's PMOS, NMOS COPLAMOS® and CMOS technologies.

5.2.2 Temperature Cycling (AC-15, AD-13)

Temperature cycling is performed to the MIL-STD-883, equivalent of Method 1010 Condition C, −65°C/ +150°C, ten cycles.

5.2.3 Constant Acceleration (centrifuge)(AC-16, AD-14)

Constant Acceleration is performed to the MIL-STD-883, equivalent of Method 2001, Condition E, 30,000 g in the Y1 orientation.

5.2.4 Hermeticity (AC-11, AD-15)

Includes fine and gross leak testing to SMC equivalent of MIL-STD-883 Method 1014 Conditions A and C.

5.2.5 Final Electrical Test

Verifies functional and parametric performance to the device specifications.

### 5.3 Custom Screening

Certain applications require special screening which can be arranged upon request.

## 6.0 Electrical Test

### 6.1 Probe and Final Test

SMC test programs are developed by Test Engineering and verified by device characterization. An approval procedure is required for the transfer of a new test program or a revised test program from engineering to production.

### 6.2 Characterization/correlation

Characterization of parts and correlation of test results with customer incoming testing performed on SMC test equipment, including Megatest and Sentry™, and Gen Rad test systems.

### 6.3 Product Engineering

SMC product engineers characterize parts to improve processing target parameters and test correlation with customers.

## 7.0 Purchased Material

Manufacturing materials are purchased from qualified vendors to SMC procurement specification.

## 8.0 Quality Control

The Quality Control Department reports to the Vice President of Quality Assurance. QC is responsible for incoming inspection, in-process audits, out-going inspection, document control, processing returned material and certification of compliance to specification.

### 8.1 Incoming Inspection

Inspectors verify critical parameters on all material used in manufacturing. The department maintains an approved vendor list and interfaces directly with vendor QC departments.

### 8.2 In-process Audits

QC performs an on-going monitoring of wafer processing, test and assembly functions.

### 8.3 Outgoing Audit

QC inspectors verify proper documentation and perform an external mechanical/visual inspection prior to shipment.

### 8.4 Document Control

All procedures for design, wafer processing, assembly, quality control and quality assurance are maintained by document control.

### 8.5 Returned Material Processing

Returned material, whether for device performance or clerical reasons, is processed through visual and electrical testing.

### 8.6 Certificates of Compliance

Certificates of Compliance are available for specified screening and/or for products ordered under a customer part number/specification.

## 9.0 Quality Assurance

The Quality Assurance Department is the customer's

representative and is independent of the product line and manufacturing organizations. Quality Assurance is responsible for reliability assessment of new and existing processes, material analysis, failure analysis, calibration and development of evaluation methods.

### 9.1 Process Qualification

All new processes and process revisions must equal or exceed the reliability of existing processes on applicable sections of the SMC Quality Conformance Test.

### 9.2 Quality Conformance Test

Samples of finished product are tested periodically to the criteria of QA-01 (see table 1). This test sequence provides historical data which is also used for qualification of new products and processes. The various subgroups contain tests referenced in Method 5005 of MIL-STD-883 as well as tests designed around industry requirements not yet incorporated in military standards.

### 9.3 Analysis

9.3.1 The analytical facilities include a scanning electron microscope equipped with energy dispersive X-ray (EDX), an infrared microscope, optical microscopes, a laser cutter, metallurgical equipment, an X-ray unit and electronic test instruments.

9.3.2 Scanning electronic microscopy is used in the periodic evaluation of workmanship in wafer processing and assembly, to support engineering efforts at process development and improvement, and in failure analysis.

9.3.3 Failure Analysis is performed upon request by sales, marketing or manufacturing organizations and is also performed on reliability test failures. The failure analysis procedures support the development of new product, process improvements, and the evaluation of screening methods.

9.3.4 Material analysis is performed on layers of the integrated circuit and on packaging to support the engineering development. This characterization is performed on in-house facilities. Independent outside analytical laboratories are used to supplement SMC facilities if and when required.

### 9.4 Calibration

The Quality Assurance Calibration Laboratory specifies calibration intervals, performs calibration and maintains calibration records. The laboratory is traceable to the National Bureau of Standards.

## 10.0 Lot Traceability

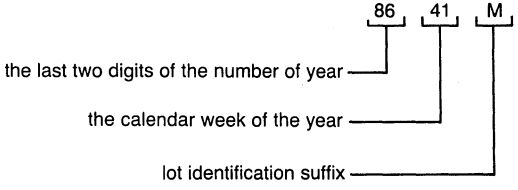
SMC maintains traceability on all product types in all packaging options (including plastic). The information available includes:

### 10.1 Wafer Processing Records

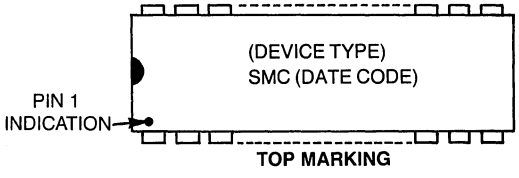
Sign-off and date on all operations, critical measurements and inspection records.



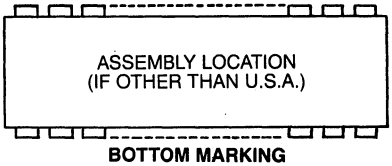
## DATE CODE INTERPRETATION




BI = BURN-IN (WHEN APPROPRIATE)




TOP MARKING




BOTTOM MARKING

### 10.2 Wafer Lot Acceptance (Mapping)

Device parameters are recorded using a high-speed Accutest™ 3600 system. Further evaluation is performed using an HP 4145A semiconductor parametric analyzer.

### 10.3 Wafer Probe and Final Test Data

These are correlated with mapping results to develop optimized process targets and yield improvement.

### 10.4 Assembly Records

Inspection results and screening throughput are recorded with date and sign-off for each lot.

## TABLE 1—QA-01 QUALITY CONFORMANCE

**GROUP B TESTS**

| Test | SMC Test Method | Mil Std 883 Method | Condition | Quantity/ accept no. or LTPD | Frequency Package Type |
|---|---|---|---|---|---|
| Subgroup 1<br>Physical dimensions | | 2016 | | 2 devices<br>(no failures) | every package lot |
| Subgroup 2<br>Resistance to solvents | QC-21 | 2015 | Marking Permanence | 4 devices<br>(no failures) | every shipment |
| Subgroup 3<br>Solderability | QC-15 | 2003 | Soldering temperature of 245 ± 5°C | 15 | periodic conformance |
| Subgroup 4<br>Internal visual and mechanical | QC-33 | 2014 | Failure criteria from design and construction requirements of applicable procurement document | 1 device<br>(no failures) | periodically |
| Subgroup 5<br>Bond strength<br>(1) Thermosonic<br>(2) Ultrasonic or wedge<br>Die shear strength | <br><br>QC-31<br><br>QC-35 | 2011<br><br><br><br>2019 | <br><br>(1) Test condition C or D<br>(2) Test condition C or D | 15 | periodic conformance all hermetic |
| Subgroup 6<br>Internal water-vapor content | | 1018 | 5,000 ppm maximum water content at 100°C | 3 devices<br>(no failures) or<br>5 devices<br>(1 failure) | periodic conformance all hermetic |
| Subgroup 7<br>Seal<br>(a) Fine<br>(b) Gross | AC-11 | 1014 | As applicable | 5 | periodic conformance all hermetic |
| Subgroup 8<br>Electrical parameters<br>Electrostatic discharge sensitivity<br>Electrical parameters | <br>QA-11 | <br>3015 | Group A, subgroup 1<br>Test condition A or B<br><br>Group A, subgroup 1 | 15 | new device types |

**GROUP C TESTS—DIE RELATED**

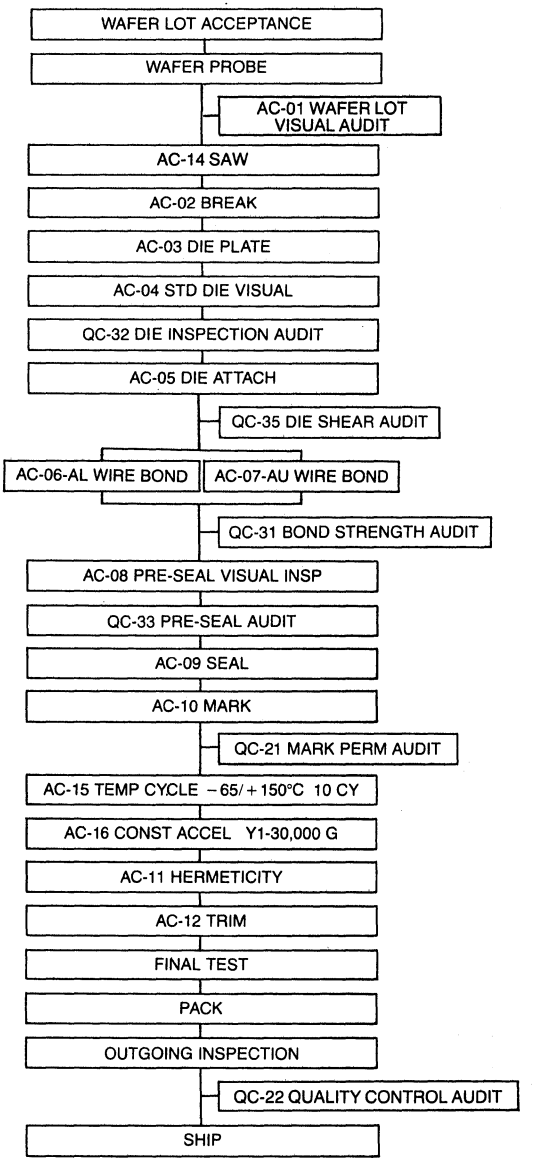
| Test | SMC Test Method | Mil Std 883 Method | Condition | Quantity/ accept no. or LTPD | Package Type |
|---|---|---|---|---|---|
| Subgroup 1<br>Steady state life test<br><br>End-point electrical parameters | <br>QA-02<br><br>Final test | <br>1005 | <br>Test condition to be specified (typically 1,000 hours at 125°C)<br>As specified in the applicable device specification | 5 | all |
| Subgroup 2<br>Temperature cycling<br>Constant acceleration<br><br>Seal<br>(a) Fine<br>(b) Gross<br>Visual examination<br>End-point electrical parameters | <br>AC-15<br>AC-16<br><br><br>AC-11<br><br>QC-22<br>Final test | <br>1010<br>2001<br><br>1014 | <br>Test condition C, 10 cycles<br>Test condition E min.<br>Y, orientation only<br>As applicable<br><br><br><br>As specified in the applicable device specification | 15 | all hermetic |

**GROUP D—PACKAGE RELATED**

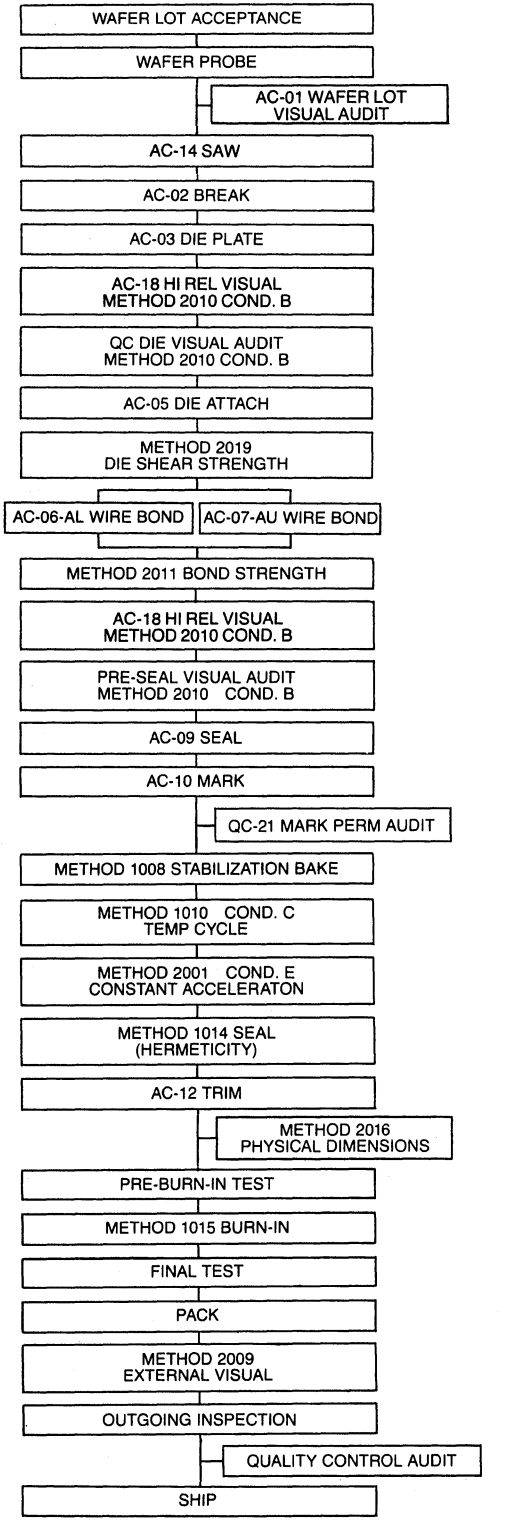
| Test | SMC Test Method | Mil Std 883 Method | Condition | Quantity/ accept no. or LTPD | Package Type |
|---|---|---|---|---|---|
| Subgroup 1 | | | | | |
| Physical dimensions | | 2016 | | 15 | all |
| Subgroup 2 | | | | | |
| Lead integrity | QC-19 | 2004 | Test condition B2 (lead fatigue | 15 | all |
| Seal | AC-11 | 1014 | As applicable | | all |
| (a) Fine | | | | | hermetic |
| (b) Gross | | | | | |
| Lid torque | | 2024 | As applicable | | cerdip only |
| Subgroup 3 | | | | | |
| Thermal shock | | 1011 | Test condition B, 15 cycles | 15 | all |
| Temperature cycling | AC-15 | 1010 | Test condition C, 100 cycles | | hermetic* |
| Moisture resistance | | 1004 | | | |
| Seal | AC-11 | 1014 | As applicable | | |
| (a) Fine | | | | | |
| (b) Gross | | | | | |
| Visual examination | | | Per visual criteria of Method 1004 and 1010 | | |
| End-point electrical parameters | | | As specified in the applicable device specification | | |
| Subgroup 4 | | | | | |
| Mechanical shock | | 2002 | Test condition B minimum | 15 | all |
| Vibration, variable frequency | | 2007 | Test condition A minimum | | hermetic |
| Constant acceleration | AC-16 | 2001 | Test condition E minimum, Y, orientation | | |
| Seal | AC-11 | 1014 | As applicable | | |
| (a) Fine | | | | | |
| (b) Gross | | | | | |
| Visual examination | | | | | |
| End-point electrical parameters | | | As specified in the applicable device specification | | |
| Subgroup 5 | | | | | |
| Salt atmosphere | | 1009 | Test condition A minimum | 15 | all |
| Seal | AC-11 | 1014 | As applicable | | hermetic* |
| (a) Fine | | | | | |
| (b) Gross | | | | | |
| Visual examination | | | Per visual criteria of Method 1009 | | |
| Subgroup 6 | | | | | |
| Internal water-vapor content | | 1018 | 5,000 ppm maximum water content at 100°C | 3 devices (no failures) or 5 devices (1 failure) | all hermetic |
| Subgroup 7 | | | | | |
| Adhesion of lead finish | | 2025 | | 15 | all |
| Subgroup 8 | | | | | |
| Humid Environment | QA-04 | | 1000 hours 85°C/85% Relative Humidity | 15 | plastic |
| End-point electrical parameters | Final test | | | | |
| Subgroup 9 | | | | | |
| Autoclave (Pressure Cooker) | QA-05 | | 48 hours at 2 atm 121°C | 15 | plastic |
| End-point electrical parameters | Final test | | | | |

* packages having gold plating thicknesses of 200 microinches or less are not required to pass subgroups 3 and 5.

## CERAMIC

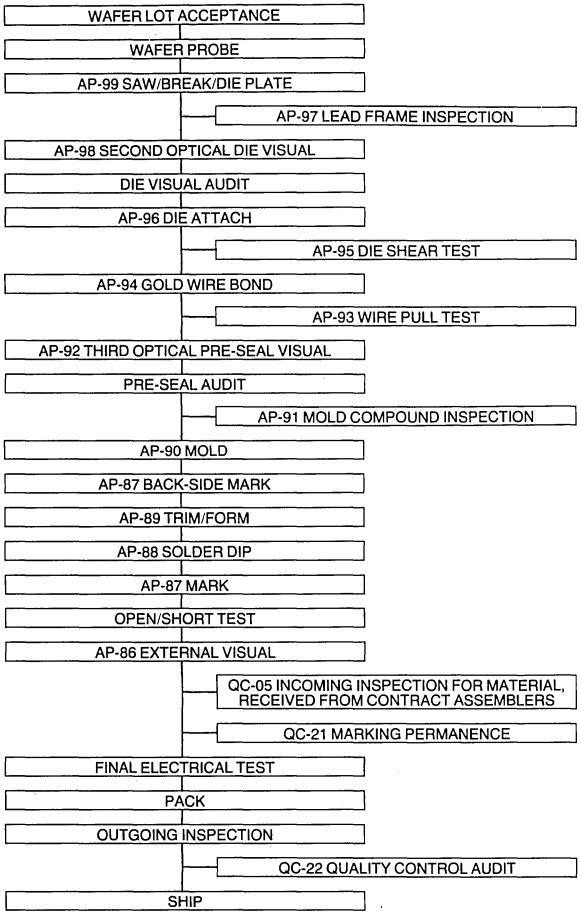



## HI REL AVAILABLE ON ALL HERMETIC PACKAGES*



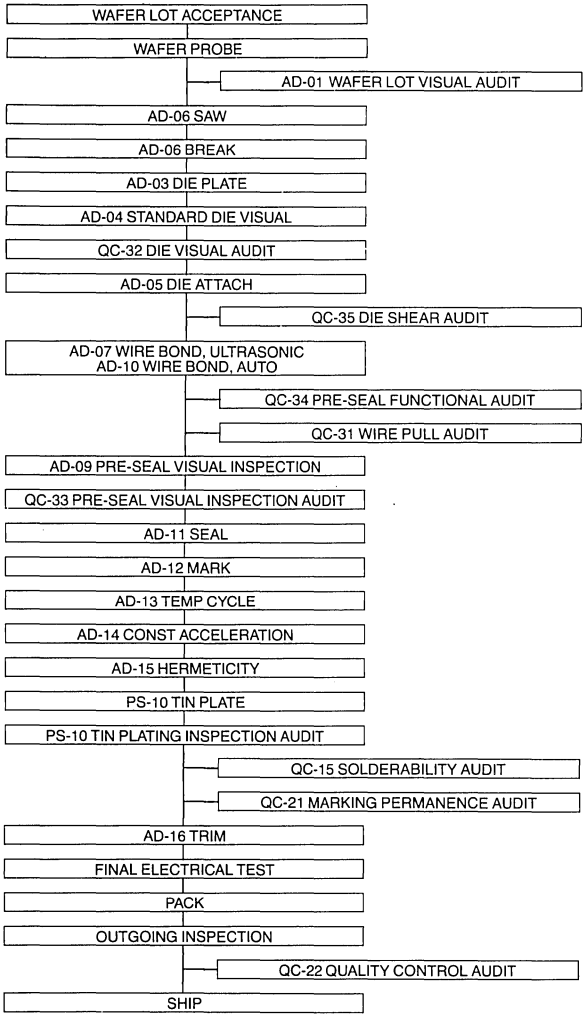

The Quality Control Department reports at the same level as the manufacturing, test and process engineering departments. QC is responsible for incoming inspection, in-process audits, out-going inspection, document control, processing returned material and certification of compliance to specification.

## PLASTIC (NOTE 1)




Note 1—Plastic assembly is sub-contracted. Assembly operations are controlled by SMC approved sub-contractor specifications.

## CERDIP



# Data Communication Products



| Part Number | Name | Description | Max Baud Rate | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|
| COM 1553A | MIL-STD-1553A Controller | MIL-STD-1553A Manchester Interface Controller | 1 MB | +5 | 40 DIP/ 44SMT | 35-50 |
| COM 1553B | MIL-STD-1553B Controller | MIL-STD-1553B Manchester Interface Bus Controller/Remote Terminal | 1 MB | +5, −5, +12 | 40 DIP/ 44SMT | 51-66 |
| COM 1671 | ASTRO | Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock | 1 MB | +5, −5, +12 | 40 DIP | 67-82 |
| COM 1863 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin | 62.5 KB | +5 | 40 DIP | 83-90 |
| COM 2017 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (use 8017 for new designs) | 25 KB | +5, −12 | 40 DIP | 91-98 |
| COM 2502 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (use 8502 for new designs) | 25 KB | +5, −12 | 40 DIP | 91-98 |
| COM 2601 | USRT | Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible | 250 KB | +5, −12 | 40 DIP | 99-106 |
| COM 2651 | USART/PCI | Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock | 1 MB | +5 | 28 DIP/ 28 SMT | 107-118 |
| COM 2661-1 -2 -3 | USART/EPCI | Universal Synchronous/Asynchronous Receiver/Transmitter, Programmable Communication Interface, Internal Baud Rate Generator, 1X, 16X, 64X clock | 1 MB | +5 | 28 DIP/ 28 SMT | 119-130 |
| COM 5025 | Multi-Protocol USYNRT | SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection | 1.5 MB | +5, +12 | 40 DIP | 131-142 |
| COM 52C50 | TWINAX | Interface Controller for IBM System/ 34, 36, 38 designated TWINAX or 5250 environment. CMOS | 1 MB | +5 | 28 DIP/ 28 SMT | 143-144 |
| COM 7210 | GPIB Interface | Intelligent Interface Controller for GPIB (IEEE-488-1978) | 8 MHz | +5 | 40 DIP | 145-156 |
| COM 78808 | OCTAL UART | 8 UART's, 8 Baud Rate Generators plus control logic and modem signals all on a single chip | 19.2 KB | +5 | 68 CERDIP LCC | 157-172 |
| COM 8004 | 32 Bit CRC Generator/ Checker | Companion device to COM 5025 Dual 32 bit CRC Generator/Checker | 2.0 MB | +5 | 20 DIP | 173-178 |
| COM 8017 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit (compatible with COM 2017) | 40 KB | +5 | 40 DIP | 179-186 |
| COM 8018 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion, margin | 62.5 KB | +5 | 40 DIP | 83-90 |
| COM 81C17 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex with built-in Baud Rate Generator, CMOS | 19.5 KB | +5 | 20 DIP/ 28 SMT | 187-188 |

# Data Communication Products CONT.

| Part Number | Name | Description | Max Baud Rate | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|
| COM 8251A | USART | Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit | 64 KB (sync) 9.6 KB (async) | +5 | 28 DIP | 189-204 |
| COM 8502 | UART | Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit (compatible with COM 2502) | 40 KB | +5 | 40 DIP | 179-186 |
| COM 9004 | IBM 3270 Receiver/ Transmitter | IBM 3274 Compatible Receiver/ Transmitter for COAX type "A" protocol (use COM 9064 for new designs) | 2.36 MB | +5, ±12 | 40 DIP/ 44 SMT | 205-212 |
| COM 9026 | LANC | Local Area Network Controller for token pass systems | 2.5 MB | +5 | 40 DIP/ 44 SMT | 213-228 |
| COM 9032 | LANT | Local Area Network Transceiver | 2.5 MB | +5 | 16 DIP | 229-234 |
| COM 9046 | SSBSS | Single Side Band Speech Scrambler, Low Power, Full Duplex, uses 3.58 MHz TV burst crystal | NA | ±2.6 | 14 DIP | 235-238 |
| COM 90C56[2] | ELANC | CMOS Enhanced Local Area Network Controller, with high throughput, network management and network diagnostic | 5 MBps | +5 | 48 PLCC | 239-240 |
| COM 90C57[2] | NBMU | CMOS Network Buffer Management Unit, to simplify interface of ELANC with dynamic RAM's | 5 Mps | +5 | 24 DIP/ 28 SMT | 241-242 |
| COM 9064 | IBM 3270 | IBM 3270 COAX type "A" controller +5V only version of COM 9004 | 2.36 MB | +5 | 40 DIP/ 44 SMT | 243-250 |
| HYC 9058 | HIT 1 | High Impedance Transceiver for Local Area Networks allows BUS topology with multi drop nodes | 2.5 MBps | +5 | 20 SIP | 251-256 |
| HYC 9068 | LAND | Local Area Network Driver with (93 Ω) line matching impedance for ARCNET networks | 2.5 MBps | +5 | 20 SIP | 257-260 |
| HYC 9078[2] | HIT 2 | High Impedance Transceiver for Local Area Networks for operation at 5MHz | 5 MBps | +5 | 20 SIP | 261-262 |

[2]For future release

STANDARD MICROSYSTEMS CORPORATION

# COM 1553A
## μPC FAMILY

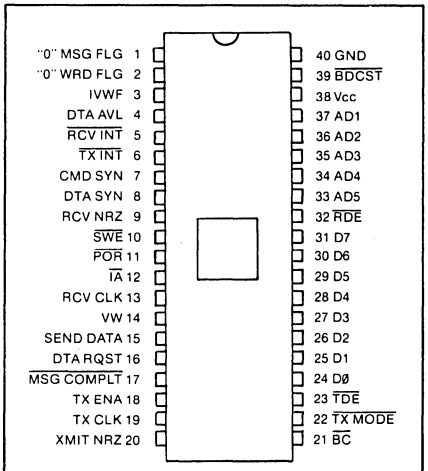


# MIL-STD-1553A "SMART®"

### FEATURES

- ☐ Support of MIL-STD-1553A
- ☐ Operates as a: Remote Terminal Responding
  Bus Controller Initiating
- ☐ Performs Parallel to Serial Conversion when Transmitting
- ☐ Performs Serial to Parallel Conversion when Receiving
- ☐ Compatible with HD-15531 Manchester Encoder/Decoder
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N Channel MOS Technology
- ☐ Available in PC Board Form from Grumman Aerospace Corporation

### PIN CONFIGURATION




PACKAGE: 40-pin D.I.P.

### GENERAL DESCRIPTION

The COM 1553A SMART® (Synchronous Mode Avionics Receiver/Transmitter) is a special purpose COPLAMOS N-Channel MOS/LSI device designed to provide the interface between a parallel 8-bit bus and a MIL-STD-1553A serial bit stream.

The COM 1553A is a double buffered serial/parallel and parallel/serial converter providing all of the "hand shaking" required between a Manchester decoder/encoder and a microprocessor as well as the protocol handling for both a MIL-STD-1553 bus controller and remote terminal.

The COM 1553A performs the following functions in response to a 16 bit Command Word. It provides address detection for the first five bits of the serial data input. If all 1's appear in the address field, a broadcast signal is generated. The sixth bit is decoded as mode: transmit or receive. The next five bits are decoded for zero message flag and special flags in the subaddress/mode field. The last five bits (word-count field) are decoded determining the number of words to be received or transmitted.

When receiving data sync the COM 1553A performs a serial to parallel conversion, buffers the 16 bit message word, and formats it into two parallel (8 bit) bytes for presentation to the I/O bus under processor or hard wired logic control.

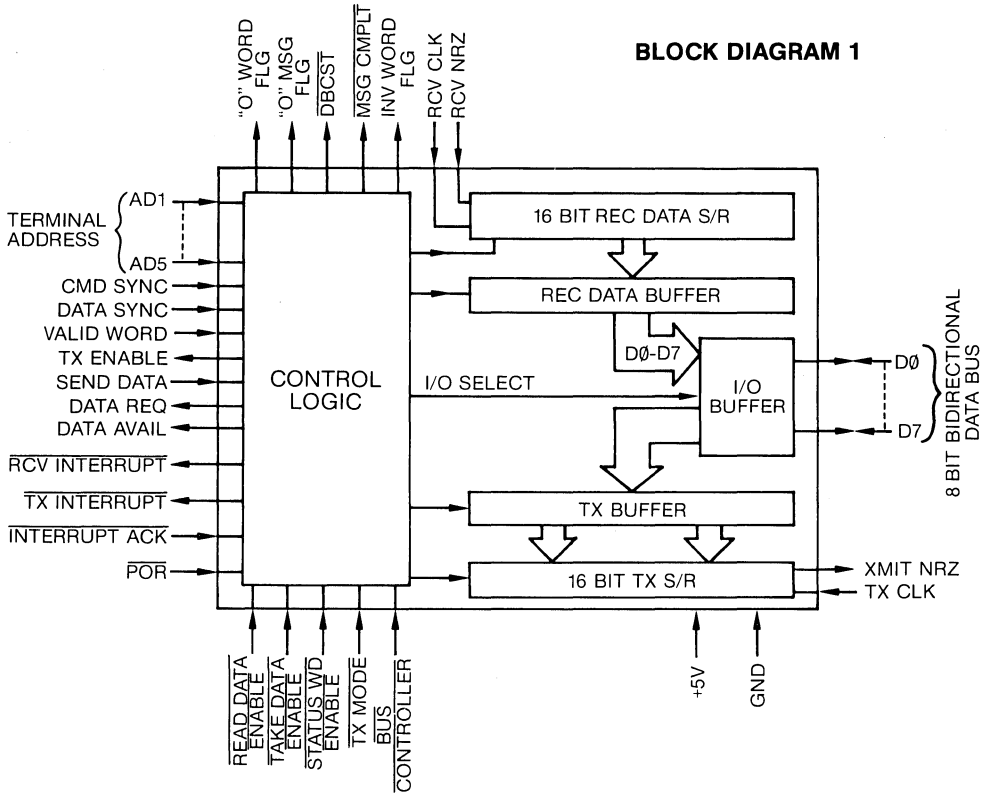
In the transmit mode the COM 1553A takes two parallel 8 bit data words from the I/O bus and serially transmits the resultant 16 bit word to the Manchester encoder. This is done under the control of Send Data. To facilitate data transfer the COM 1553A provides all necessary buffering and storage for transmitted and received data. It also provides all necessary hand shaking, control flags and interrupts to a processor or hard wired logic terminal. See block diagram 1.

The COM 1553A can be set up as either a remote terminal or a bus controller interface.

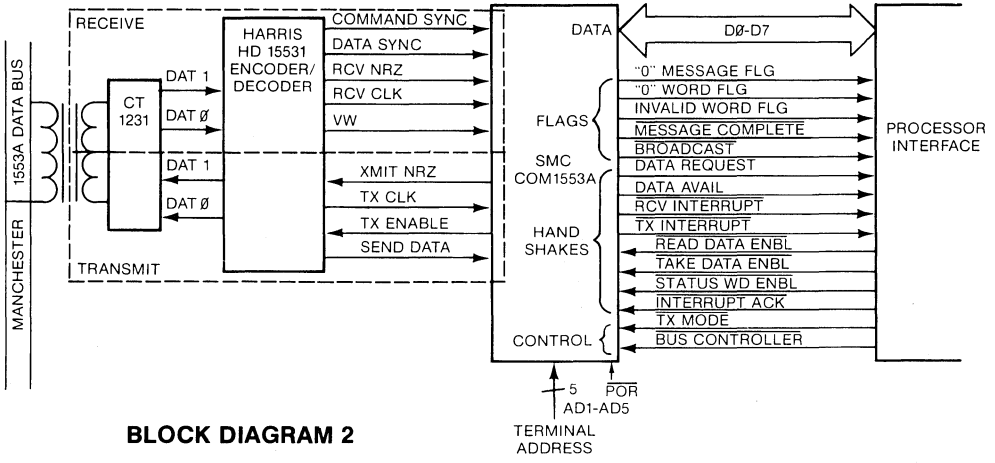
The COM 1553A is compatible with Harris' HD-15531 CMOS Manchester Encoder-Decoder chip and interfaces directly with it. A 3 device kit consisting of: SMC's COM 1553A, Harris' HD-15531 and Circuit Technology's CT1231 forms a complete system interface for the message structure of MIL-STD-1553A. See block diagram 2.

Note: All terminology utilized in this data sheet is consistent with MIL-STD-1553.

## BLOCK DIAGRAM 1




## BLOCK DIAGRAM 2



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | "Ø" MESSAGE FLAG | ØMF | The ZERO MESSAGE FLAG output is set when the 7th through 11th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØMF is an open drain output. |
| 2 | "Ø" WORD FLAG | ØWF | The ZERO WORD FLAG output is set when the 12th through 16th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØWF is an open drain output. |
| 3 | INVALID WORD FLAG | IVWF | The INVALID WORD FLAG output is set when the word just received has an invalid parity bit or invalid format. IVWF is an open drain output. |
| 4 | DATA AVAILABLE | DTA AVL | DATA AVAILABLE is set when a word received is ready to be read. When the COM 1553A is the bus controller, DTA AVL occurs on command, status or data words. When the COM 1553A is a remote terminal, DTA AVL is set only on data words. DTA AVL is an open drain output. |
| 5 | $\overline{\text{RECEIVE INTERRUPT}}$ | $\overline{\text{RCV INT}}$ | $\overline{\text{RECEIVE INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{RCV INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$, or if the line is not active for 32 receive clocks. |
| 6 | $\overline{\text{TRANSMIT INTERRUPT}}$ | $\overline{\text{TX INT}}$ | $\overline{\text{TRANSMIT INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a one, and the first 5 bits match AD1-AD5. $\overline{\text{TXINT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$. |
| 7 | COMMAND SYNC | CMD SYN | COMMAND SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a command word. |
| 8 | DATA SYNC | DTA SYN | DATA SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a data word. |
| 9 | RECEIVER NRZ | RCV NRZ | Receiver serial input from Manchester decoder. Data must be stable during the rising edge of the receive clock. |
| 10 | $\overline{\text{STATUS WORD ENABLE}}$ | $\overline{\text{SWE}}$ | $\overline{\text{SWE}}$ is the output enable for the following open drain outputs:<br>ØMF<br>ØWF<br>IVWF<br>DTA AVL<br>$\overline{\text{DTA RQ}}$<br>$\overline{\text{MSG CPLT}}$ |
| 11 | $\overline{\text{POWER ON RESET}}$ | $\overline{\text{POR}}$ | $\overline{\text{POWER ON RESET}}$. Active low for reset. |
| 12 | $\overline{\text{INTERRUPT ACKNOWLEDGE}}$ | $\overline{\text{IA}}$ | $\overline{\text{IA}}$ resets $\overline{\text{TX INT}}$, $\overline{\text{REC INT}}$, ØMF, ØWF and $\overline{\text{BRD CST}}$. $\overline{\text{IA}}$ may occur between the trailing edges of receive clocks 6 and 10, or between the leading edge of receive clock 12 and the falling edge of receive clock 15, or after the falling edge of clock 17. |
| 13 | RECEIVE CLOCK | RCV CLK | The RECEIVE CLOCK is synchronous with the Receiver NRZ input during the command sync or data sync envelopes. |
| 14 | VALID WORD | VW | This input is driven by the VALID WORD output of the Manchester Decoder. VW should occur immediately after the rise of the first RCV CLK following the fall DATA SYNC or COMMAND SYNC. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 15 | SEND DATA | SD | SEND DATA is a "handshake" signal received from the Manchester encoder indicating that the encoder is ready for the COM 1553A to transmit data. SD will bracket 16 transmit data clocks. The contents of the transmitter buffer will be transferred into the transmit register when SD is low. |
| 16 | DATA REQUEST | DTA RQST | DATA REQUEST is an open drain output which is set high when the transmitter holding register is ready to accept more data. |
| 17 | $\overline{\text{MESSAGE COMPLETE}}$ | $\overline{\text{MSG CMPLT}}$ | In the receive mode the $\overline{\text{MESSAGE COMPLETE}}$ output is set low when the appropriate number of data words have been received. In the transmit mode, $\overline{\text{MSG CMPLT}}$ indicates that the appropriate number of command, status or data words have been transmitted. When the COM 1553A is a bus controller, $\overline{\text{MSG CMPLT}}$ will be asserted low when 33 command status or data words have been transmitted. $\overline{\text{MSG CMPLT}}$ is an open drain output. |
| 18 | TRANSMIT ENABLE | TXENA | A TRANSMIT ENABLE signal will be sent to the Manchester Encoder to initiate transmission of a word. TXENA is generated under the following conditions:<br>1) COM 1553A is a bus controller: A $\overline{\text{TXMODE}}$ pulse will set TXENA. A second $\overline{\text{TXMODE}}$ pulse will reset TXENA.<br>2) COM 1553A is a remote terminal. A Transmit Command from the Controller will cause a TRANSMIT INTERRUPT (see pin 6). When this is acknowledged by a TXMODE pulse from the system, TXENA will be set.<br>TXENA will then be reset by either<br>A) Send Data Command associated with the last data word.<br>B) a second $\overline{\text{TXMODE}}$ pulse.<br>3) COM 1553A is a remote terminal. The falling edge of a DATA SYNC associated with the last data word of a message while in the receive mode. TXENA will be reset during the next SEND DATA envelope. |
| 19 | TRANSMIT CLOCK | TXCLK | Transmitter shift clock. |
| 20 | TRANSMIT NRZ | XMIT NRZ | Serial data output to the Manchester Encoder. |
| 21 | $\overline{\text{BUS CONTROLLER}}$ | $\overline{\text{BC}}$ | $\overline{\text{BC}}$ determines whether the COM 1553A is acting as bus controller ($\overline{\text{BC}} = 0$) or as a remote terminal ($\overline{\text{BC}} = 1$). |
| 22 | $\overline{\text{TRANSMIT MODE}}$ | $\overline{\text{TXMODE}}$ | $\overline{\text{TXMODE}}$ is a system input controlling transmission. See TXENA (pin 18). |
| 23 | $\overline{\text{TAKE DATA ENABLE}}$ | $\overline{\text{TDE}}$ | $\overline{\text{TDE}}$ is an input from the system initiating transmission. Two $\overline{\text{TDE}}$ pulses are required for each 16 bit data word, one for each 8 data bits placed on DØ-D7. |
| 24-31 | DATA BUS | DØ-D7 | Bidirectional 8 bit Data Bus to the system. DØ is the LSB. DØ-D7 present open drain outputs. |
| 32 | $\overline{\text{READ DATA ENABLE}}$ | $\overline{\text{RDE}}$ | $\overline{\text{RDE}}$ is an input from the system instructing the COM 1553A to place the received data onto DØ-D7. Two $\overline{\text{RDE}}$ pulses are required per 16 bit data word, one for each 8 bits. |
| 33-37 | ADDRESS | AD5-AD1 | AD1-AD5 provide addressing to the COM 1553A. Each input has a pull-up resister allowing simple switching to ground to select the user address. |
| 38 | POWER SUPPLY | VCC | +5 Volt supply. |
| 39 | $\overline{\text{BROADCAST}}$ | $\overline{\text{BDCST}}$ | $\overline{\text{BDCST}}$ is set low when a "broadcast" command word (the address bits all set to "one") is being received. $\overline{\text{BDCST}}$ is reset by IA. |
| 40 | GROUND | GND | Ground |

## OPERATION...RECEIVE MODE

The COM 1553A is considered in the receive mode when TXENA = 0. The most significant bit of both command and data words is received first.

Message reception is initiated when CMD SYN goes high. The next 16 receive clocks are used to shift serial data into RCV NRZ.

The first 5 bits of a command word designate a remote terminal address. These 5 bits are compared with AD1-5. Should the address bits compare, the sixth bit is examined. If it is a zero, a $\overline{\text{RECEIVE INTERRUPT}}$ is generated. If it is a one, a $\overline{\text{TRANSMIT INTERRUPT}}$ is generated.

Bit fields 7-11 and 12-16 are examined for all zeros. All zeros in bit field 7-11 denotes a "ZERO MESSAGE" and all zeros in bit field 12-16 denotes a "ZERO WORD."

Receipt of a data word is indicated when DTA SYN goes high.

When DTA SYN or CMD SYN goes low, the contents of the 16 bit receive register are loaded into the receive buffer. The buffer is organized into two groups of 8 bits each. The most significant 8 bits (byte 1) will be enabled onto the 8 bit data bus on receipt of the first $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE1}}$). The second byte will be enabled on receipt of the second $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE2}}$).

A DATA AVAILABLE is generated for data words only. However, data will be available on DØ-D7 for both command and data words.

If 32 clocks are received after the rising edge of CMD SYN or DTA SYN an "Idle Line Reset" condition exists. This implies that a new CMD SYN or DTA SYN has not yet been received within 16 clocks of the fall of the previous sync signal. The "Idle Line Reset" will reset the following signals:

| | |
|---|---|
| $\overline{\text{REC INT}}$ | "0" MSG FLG |
| $\overline{\text{TX INT}}$ | "0" WRD FLG |
| $\overline{\text{BRD CST}}$ | |

When the commanded number of data words have been received, a $\overline{\text{MESSAGE COMPLETE}}$ signal is generated.

As the transmitter and receiver registers operate independently, the COM 1553A will receive its own transmission. The following signals are inhibited during transmission:

| $\overline{\text{BC}} = 0$ | $\overline{\text{BC}} = 1$ |
|---|---|
| $\overline{\text{REC INT}}$ | DAT AVL |
| $\overline{\text{XMT INT}}$ | IVWF |
| $\overline{\text{BRD CST}}$ | $\overline{\text{REC INT}}$ |
| ØWF | $\overline{\text{XMT INT}}$ |
| ØMF | ØMG |
| JAM MESSAGE ERROR* | ØWF |
| | $\overline{\text{BRD CST}}$ |
| | JAM MESSAGE ERROR* |

*JAM MESSAGE ERROR is an internal signal. See OPERATION...TRANSMIT MODE.

## OPERATION...TRANSMIT MODE

The COM 1553A is considered in the transmit mode when TXENA = 1. This is caused by a $\overline{\text{TXMODE}}$ pulse (see description of pin functions, pin 18). The $\overline{\text{TXMODE}}$ pulse in turn is a system response to a transmit command from the receiver.

When the Manchester Encoder receives TXENA = 1, it will respond with SEND DATA = 1. The COM 1553A will then send the system a DATA REQUEST.

Data is loaded into the transmitter data buffer from the 8 bit data bus by pulsing $\overline{\text{TDE}}$. The 8 most significant bits are loaded in by the first $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE1}}$), the 8 least significant bits by the second $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE2}}$).

When SEND DATA (pin 15) is low, the transmitter shift register inputs will follow either the transmit buffer output, JAM ADDRESS or JAM MESSAGE ERROR signals. When SEND DATA is high, the shift register parallel inputs are disabled and the shift register contents are shifted out in NRZ form using the 16 negative edges in the send data envelope.

To facilitate transmission of the status word from a remote terminal, the COM 1553A will "jam" the first (most significant) 6 bits of the status word into the transmit register when $\overline{\text{BC}}$ is high. These bits will automatically be sent at the first SEND DATA pulse. In general for MIL-STD-1553A the remaining 10 bits will normally be all zeros and will automatically be sent out as such. If it is desired to send additional status information (for MIL-STD-1553B), a $\overline{\text{TDE1}}$ pulse will load the least significant 2 bits of the first 8 bit byte, and a $\overline{\text{TDE2}}$ will load all 8 bits of the second byte. Note that these TDE pulses must be sent (and data presented) before the first SD = 1 response from the Manchester Encoder.

A JAM ADDRESS occurs when 1) a transmit command is addressed to the COM 1553A 2) A $\overline{\text{TXMODE}}$ pulse is received and 3) a valid word signal is received. Upon a JAM ADDRESS the COM 1553A will load its address into the first 5 bits of the transmit register.

Alternatively, a JAM ADDRESS will also occur at the fall of the last data sync after valid receive command has been detected.

The JAM ADDRESS function will be inhibited if a "0" word and "0" message condition exists in the command word. The JAM ADDRESS will be reset by the leading edge of SEND DATA.

The JAM MESSAGE ERROR function occurs when, in the receive mode, a data word is not followed by a VALID WORD signal. JAM MESSAGE ERROR consists of loading a one in the sixth bit location of the transmit shift register (the message error location).

JAM MESSAGE ERROR is inhibited when the transmit command word contains "0" Message and "0" Word fields.

When the commanded number of data words has been transmitted a $\overline{\text{MESSAGE COMPLETE}}$ signal will be generated.

## GENERAL OPERATION NOTES

1. BUS CONTROLLER. When $\overline{BC} = 0$, signifying that the COM 1553A is the bus controller the following is true:
   A. DTA AVL is generated on the rising edge of the 17th receive clock following a Command Sync or Data Sync. This allows the bus controller to receive command, status or data words regardless of their address.
   B. TXENA is contingent only on $\overline{TXMODE}$. A bus controller can therefore transmit whenever it desires.
   C. The jam functions are inhibited.

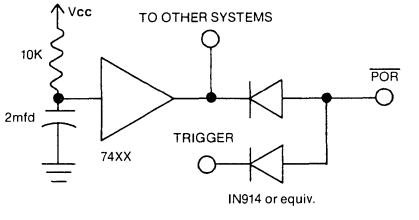
2. INVALID WORD FLAG. When $\overline{BC} = 0$, IVWF will be set if the Valid Word input (from the Manchester decorder) does not go high following receipt of all words. This includes words received from the same device's transmitter. (This provides a validity test of the controller transmission).
   When $\overline{BC} = 1$, IVWF will be set if Valid Word does not go high following receipt of all command and address words addressed to the terminal.
   IVWF will be set for the following conditions:

| *Message type* | *Word* | *Terminal is* | *IVWF generated* |
|---|---|---|---|
| Transit Group | Transmit command | receiving | yes |
| | Status word | transmitting | no |
| | Data word | transmitting | no |
| Receive Group | Receive command | receiving | yes |
| | Data word | receiving | yes |
| | Status word | transmitting | no |
| Receive/Transmit Group (this terminal addressed to receive) | Receive command | receiving | yes |
| | Transmit command | receiving | no |
| | Status word | receiving | no |
| | Data word | receiving | yes |
| | Status word | transmitting | no |
| Receive/Transmit group (this terminal addressed to transmit) | Receive command | receiving | no |
| | Transmit command | receiving | yes |
| | Status word | transmitting | no |
| | Data word | transmitting | no |
| | Status word | receiving | no |

3. POWER ON RESET. During power-up, $\overline{POR}$ is a low to high exponential with a minimum low time, after the supply is within specified limits, of 10 microseconds. $\overline{POR}$ may also occur asynchronously anytime after power has stabilized.
   $\overline{POR}$ initializes the following outputs:

| | | |
|---|---|---|
| ØMG | $\overline{REC\ INT}$ | $\overline{TDE}$ |
| ØWF | $\overline{MSG\ CMPLT}$ | DTA AVL |
| $\overline{BRD\ CST}$ | IVW | TXENA |
| $\overline{XMT\ INT}$ | $\overline{RDE}$ | DTA RQ |

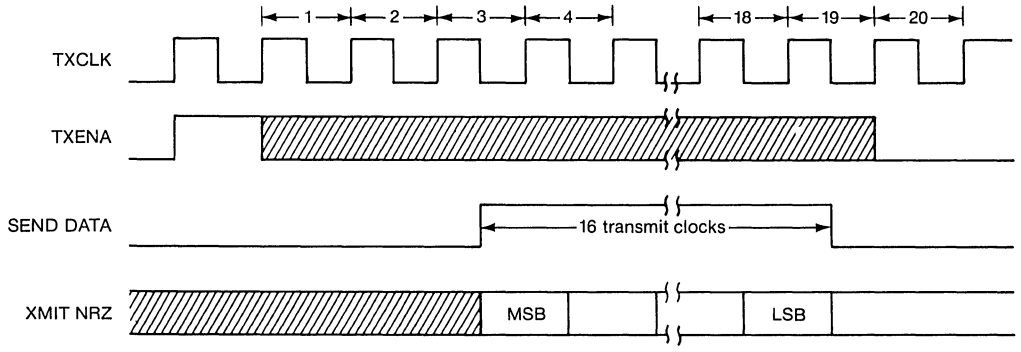
   The following circuit may be used to implement $\overline{POR}$.




4. WORD COUNT: Word count is decoded as follows:

| *D1* | *D2* | *D3* | *D4* | *D5* | *Word Count* |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| 1 | 1 | 1 | 1 | 1 | 31 |
| 0 | 0 | 0 | 0 | 0 | 32 |

## TRANSMIT TIMING FIGURE 1




**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

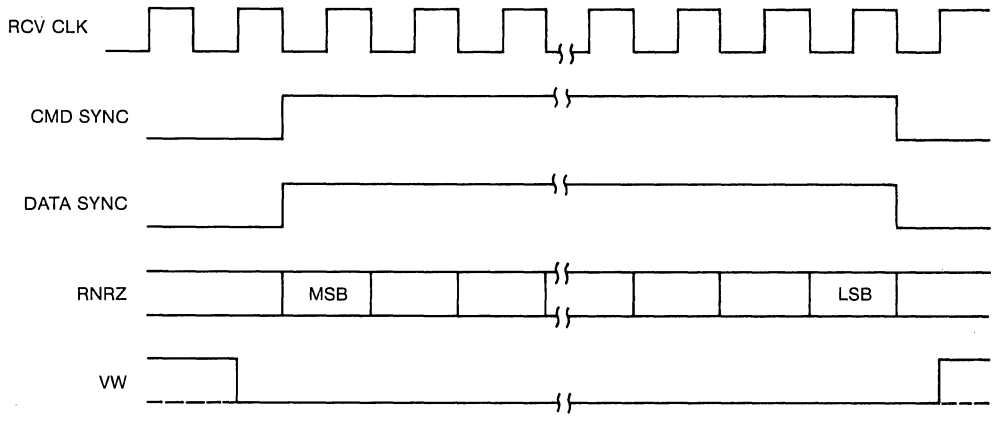
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = -55°C to 125°C, $V_{CC}$ = +5 ±5%, unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| Input Voltage Levels | | | | | |
| Low Level, $V_{IL}$ | | | 0.8 | V | |
| High Level, $V_{IH}$ | 3.0 | | | V | |
| Output Voltage Levels | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = -1.6 mA, except open drain |
| High Level $V_{OH}$ | 3.0 | 4.0 | | V | $I_{OH}$ = 100 μA, except open drain |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = -1.6 mA, open drain output |
| Output Leakage, $I_{LO}$ | | | 10 | μA | |
| Input Current, AD1-AD5 | | 60 | | μA | $V_{IN}$ = 0V |
| Output Capacitance | | 5 | 10 | pf | |
| Input Capacitance | | 10 | 25 | pf | |
| Power Dissipation | | | 500 | mW | |

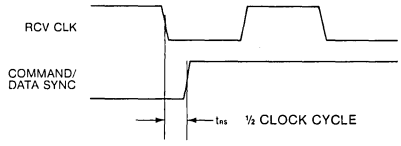
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| Clock Frequency | $f_T$, $f_R$ | 980 | 1000 | 1020 | KHz | |
| Clock Duty Cycle | | 45 | 50 | 55 | % | |
| Rise and fall times, $\overline{IA}$, $\overline{TDE}$ $\overline{TX\ MODE}$, $\overline{SWE}$, $\overline{RDE}$ | $t_r$, $t_f$ | | | 20 | ns | |
| rise and fall times, all other inputs | $t_r$, $t_f$ | | | 50 | ns | |
| receiver clock-NRZ | $t_{RN}$ | | | 65 | ns | figure 3B |
| receiver clock-sync delay | $t_{SR}$ | | | 85 | ns | figure 3B |
| receiver clock-VW delay | $t_{RV}$ | | | 100 | ns | figure 3B |
| VW reset delay | $t_{VS}$ | | | 500 | ns | figure 3C |
| transmit clock-TX ENA delay | $t_{TX}$ | 25 | | | ns | figure 4A |
| TX ENA pulse width | $t_{XW}$ | 60 | | | ns | figure 4A |
| transmit clock-send data set-up | $t_{TS}$ | | | 40 | ns | figure 4B |
| transmit clock-send data hold time | $t_{ST}$ | | | 140 | ns | figure 4C |
| transmit clock fall to NRZ | $t_{TN}$ | 0 | | | ns | figure 4B |
| transmit clock rise to NRZ | $t_{NT}$ | 95 | | | ns | figure 4B |
| $\overline{TX\ MODE}$ pulse width | $t_{MW}$ | 150 | | | ns | figure 5A |
| $\overline{TX\ MODE}$ to TX ENA delay | $t_{MX}$ | | | 750 | ns | figure 5B |
| VALID word to TX ENA delay | $t_{VX}$ | | | 750 | ns | figure 5B |
| Data sync to TX ENA delay | $t_{DX}$ | | | 750 | ns | figure 5C |
| TX ENA reset delay | $t_{SX}$ | | | 750 | ns | figure 5C |
| DATA SET-up time | $t_{D1}$ | 100 | | | ns | figure 6A |
| $\overline{TDE}$ pulse width | $t_{D2}$ | 150 | | | ns | figure 6A |
| Data Hold time | $t_{D3}$ | 100 | | | ns | figure 6A |
| Cycle time | $t_{D4}$ | 450 | | 16000 | ns | figure 6A |
| DTA RQST Delay | $t_{D5}$ | 450 | | | ns | figure 6A |
| Output Enable time | $t_{D6}$ | 100 | | | ns | figure 6B |
| $\overline{RDE}$ Pulse width | $t_{D7}$ | 150 | | | ns | figure 6B |
| receive cycle time | $t_{D8}$ | 450 | | 17000 | ns | figure 6B |
| Flag delay time | $t_{D9}$ | 450 | | | ns | figure 6B |
| Output disable time | $t_{D10}$ | 100 | | | ns | figure 6B |
| SEND DATA delay | $t_{D11}$ | 2.5 | | 3.5 | $\mu$s | figure 6C |
| TDE off delay | $t_{D12}$ | 1.5 | | | $\mu$s | figure 6C |
| $\overline{TDE1}$ delay | $t_{D13}$ | 500 | | | ns | figure 6C |
| SYN to $\overline{RDE}$ | $t_{D14}$ | 500 | | | ns | figure 6D |
| RDE to SYN | $t_{D15}$ | | | 2.5 | $\mu$s | figure 6D |
| Status word Enable | $t_{SE}$ | | | 100 | ns | figure 8A |
| Status word Disable | $t_{SD}$ | | | 100 | ns | figure 8A |
| Flag delay time | $t_{CF}$ | | | 1 | $\mu$s | figure 8B |
| VW delay time | $t_{CV}$ | | | 90 | ns | figure 8B |
| IVWF delay time | $t_{CI}$ | | | 450 | ns | figure 8B |
| DTA AVL delay time | $t_{CD}$ | | | 500 | ns | figure 8B |
| DTA RQST delay time | $t_{SR}$ | | | 450 | ns | figure 8C |
| $\overline{BRD\ CST}$ delay time | $t_{RB}$ | | | 2 | $\mu$s | figure 8C |
| $\overline{BRD\ CST}$ pulse width | $t_{BW}$ | 1 | | | $\mu$s | figure 8D |
| flag reset delay | $t_{IB}$ | | | 750 | ns | figure 8D, 8E |
| Interrupt delay | $t_{RI}$ | | | 1.5 | $\mu$s | figure 8D |
| IA pulse width | $t_{IA}$ | 150 | | | ns | figure 8D |
| Interrupt pulse width | $t_{IW}$ | 1 | | | $\mu$s | figure 8D |
| Flag reset time | $t_{FR}$ | | | 450 | ns | figure 8F |
| DTA AVL reset delay | $t_{RD}$ | | | 750 | ns | figure 8F |
| IVWF reset delay | $t_{RV}$ | | | 750 | ns | figure 8F |
| $\overline{MSG\ CMPLT}$ turn-on delay | $t_{MR}$ | | | 1.5 | $\mu$s | figure 9A, 9B |
| $\overline{MSG\ CMPLT}$ turn-on delay | $t_{MF}$ | | | 1.5 | $\mu$s | figure 9A, 9C |

## RECEIVE TIMING FIGURE 2

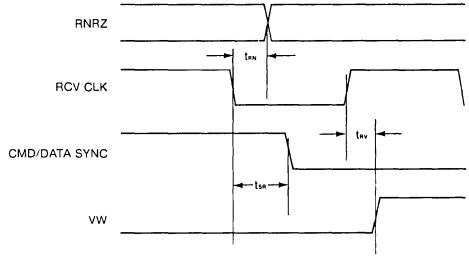



## RECEIVER INPUT TIMING FIGURE 3

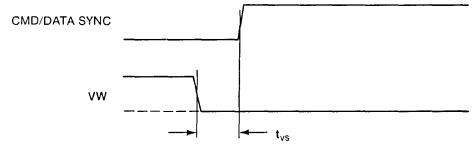
### 3A




### 3B

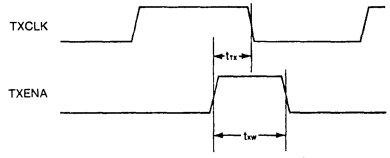



### 3C

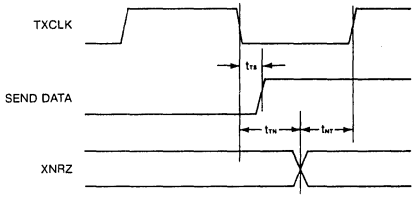



## TRANSMITTER TIMING FIGURE 4

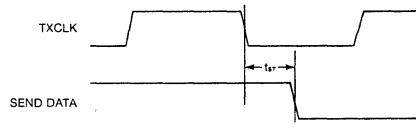
### 4A




### 4B

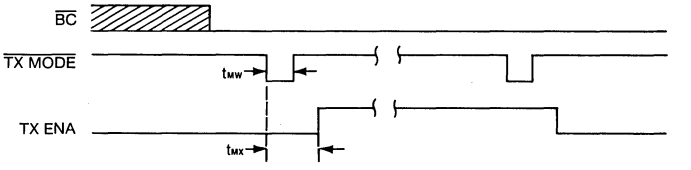



### 4C

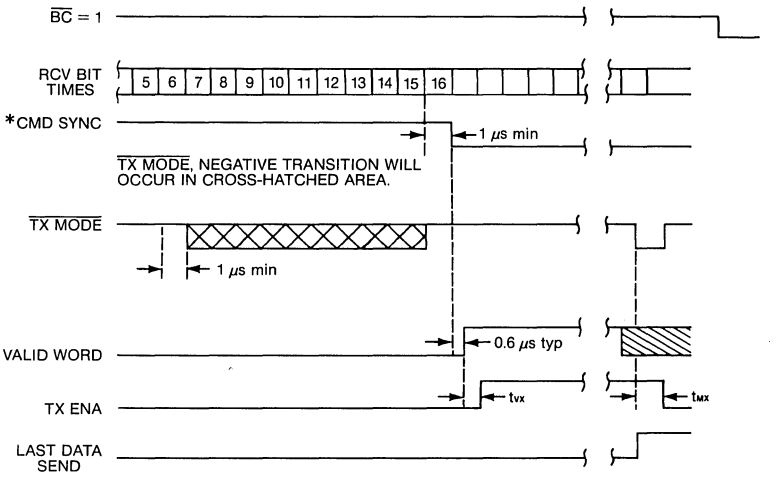


## TRANSMIT ENABLE (TX ENA) TIMING FIGURE 5

### 5A

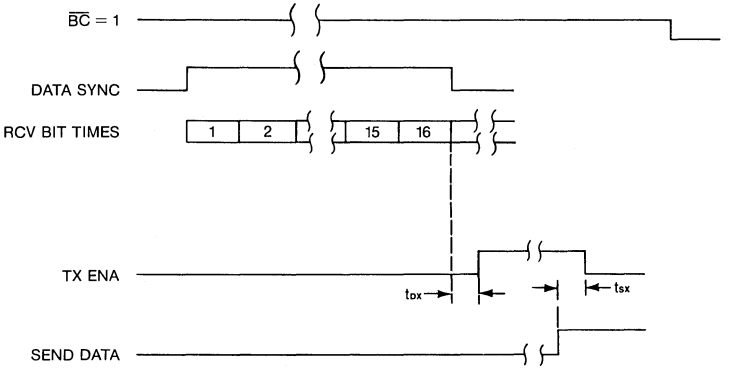



### 5B*




*THIS IS A CMD WORD BEING RECEIVED, IT IS ADDRESSED TO THIS BUFFER AND THE T/R BIT = 1. TX ENA IS RESET BY 2ND TX MODE NEGATIVE TRANSITION OR BY LAST SEND DATA (MESSAGE COMPLETE FUNCTION).

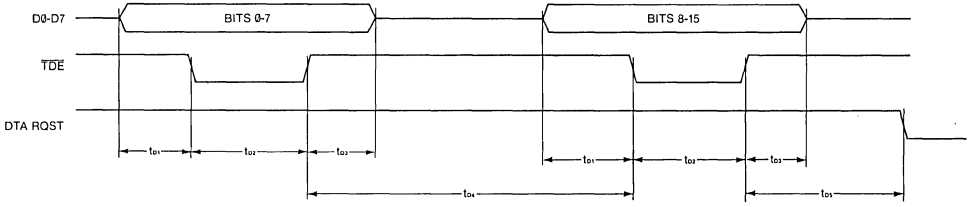
### 5C**



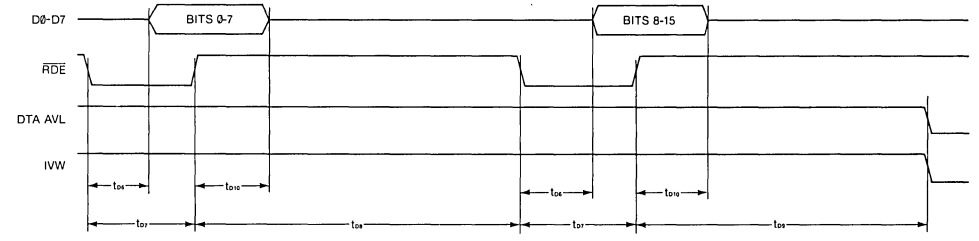

**THIS IS THE LAST DATA WORD BRING RECEIVED. THIS TERMINAL PREVIOUSLY HAD RECEIVED A REC CMD WORD WITH OUR ADDRESS AND A REC/XMIT BIT = 0 DURING THIS MESSAGE SEQUENCE. TX ENABLE IS SET BY MSG CMPLT FUNCTION AND RESET BY RECEIPT OF SEND DATA.

## DATA BUS TIMING FIGURE 6

### 6A

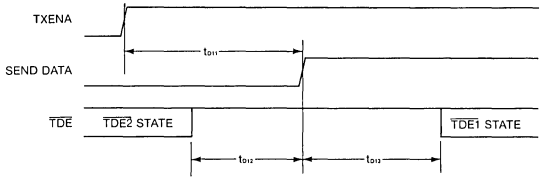



### 6B



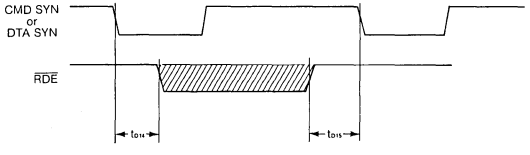

## DATA BUS TIMING FIGURE 6

### 6C

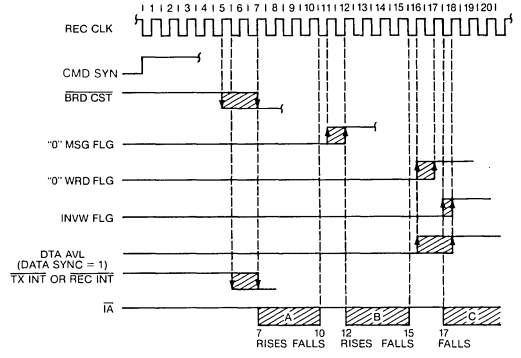



NOTE: SEND DATA RISING EDGE INITIALIZES $\overline{TDE}$ TO $\overline{TDE1}$ STATE

### 6D




## $\overline{IA}$ RESETS FIGURE 7



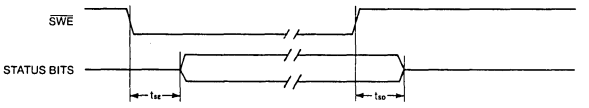

$\overline{IA}$ OCCURRING DURING ZONE A RESETS: BRD CST. TX INT. REC INT.

$\overline{IA}$ OCCURRING DURING ZONE B RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG.

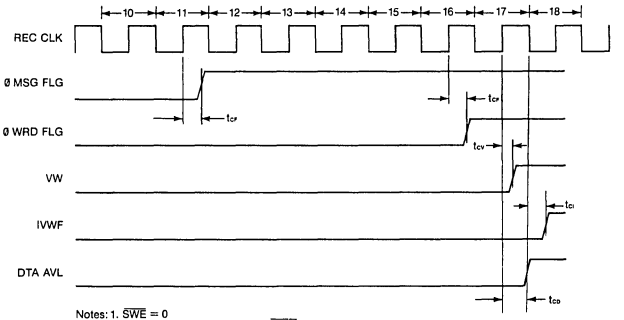
$\overline{IA}$ OCCURRING DURING ZONE C RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG. "0" WRD FLG.

## STATUS FLAGS FIGURE 8

**8A**

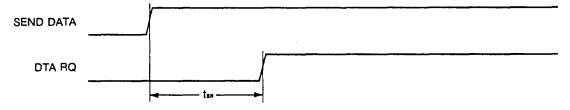



**8B**

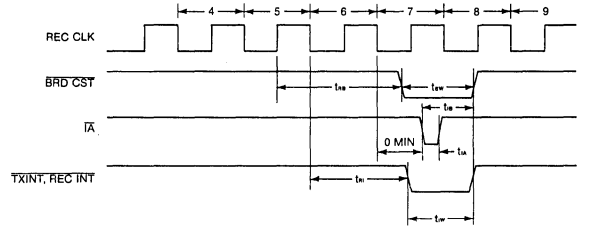



Notes: 1. $\overline{SWE} = 0$
2. IVWF and DTA AVL reset by $\overline{RDE2}$ or REC CLK 14 of the next word

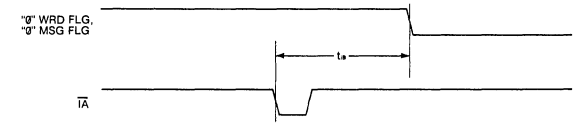
**8C**



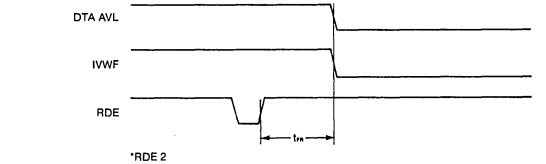

**8D**




**8E**

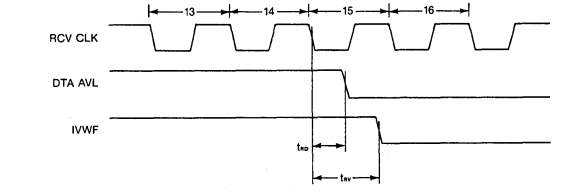



**8F**




*RDE 2

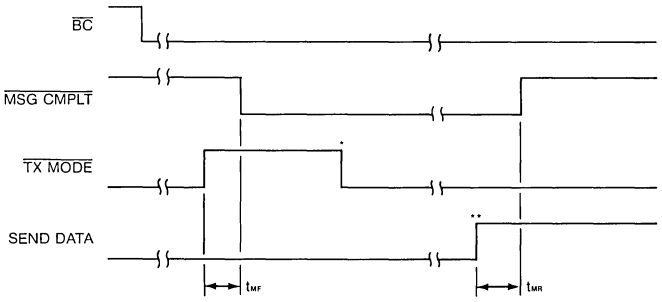
If RDE is not used to reset IVWF and RDE, then they are reset by RCV CLK 14 as shown below.



## MESSAGE COMPLETE FIGURE 9

### BUS CONTROLLER MODE

9A

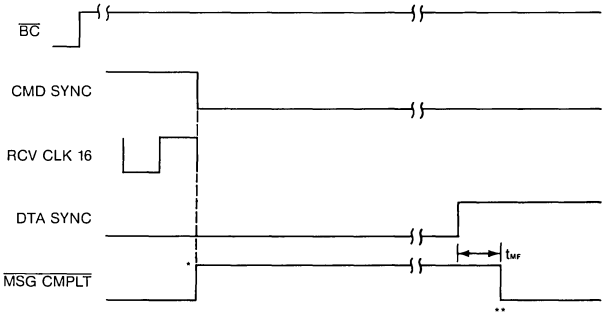



*WORD COUNTER IS PRESET TO 33

**$\overline{\text{MSG CMPLT}}$ SET $t_{MR}$ MAX AFTER RISE OF 33RD SEND DATA PULSE

### REMOTE TERMINAL, RECEIVE COMMAND RECEIVED

9B

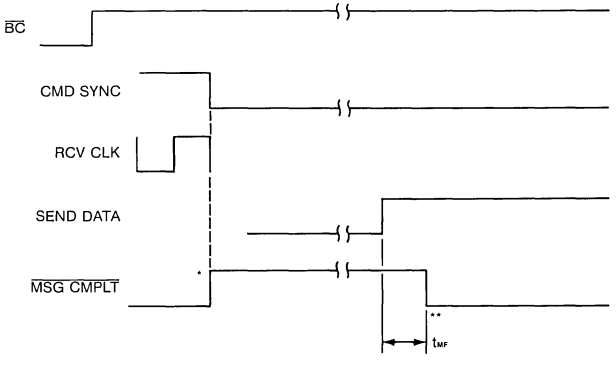



*WORD COUNTER PRESET TO COUNT IN COMMAND WORD

**$\overline{\text{MSG CMPLT}}$ GENERATED BY LAST DATA SYNC OF THE MESSAGE GROUP

### REMOTE TERMINAL, TRANSMIT COMMAND RECEIVED

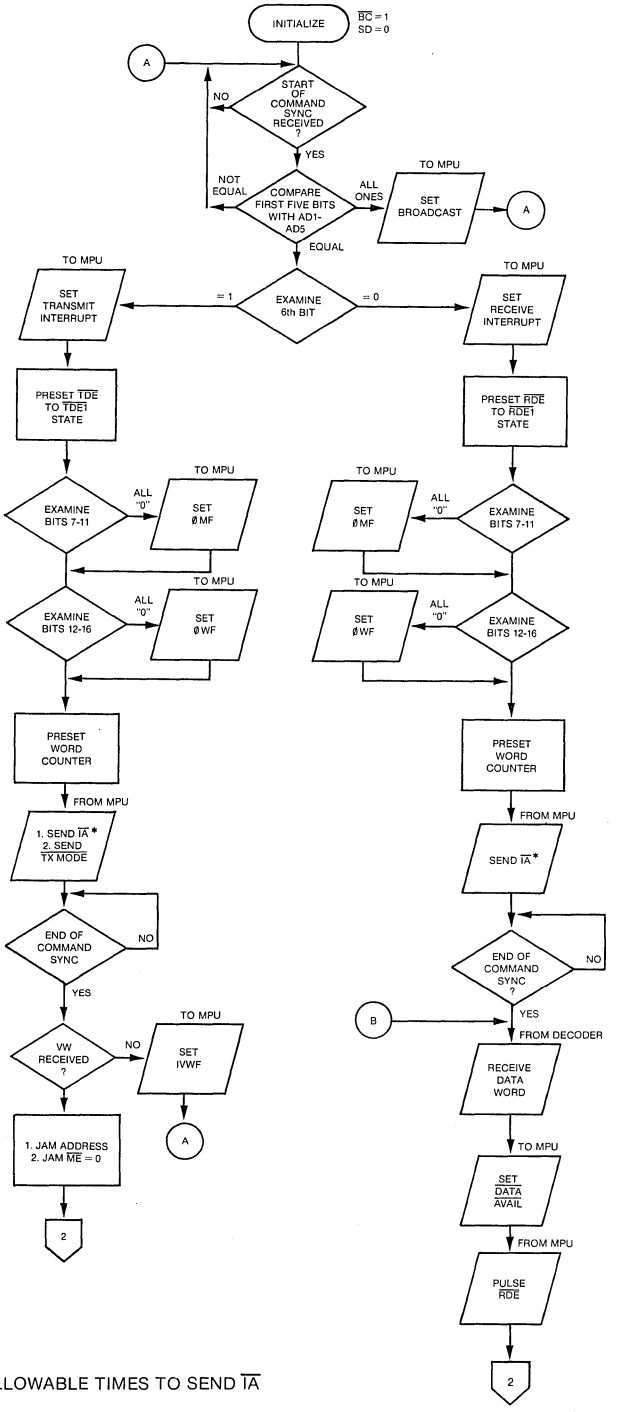
9C



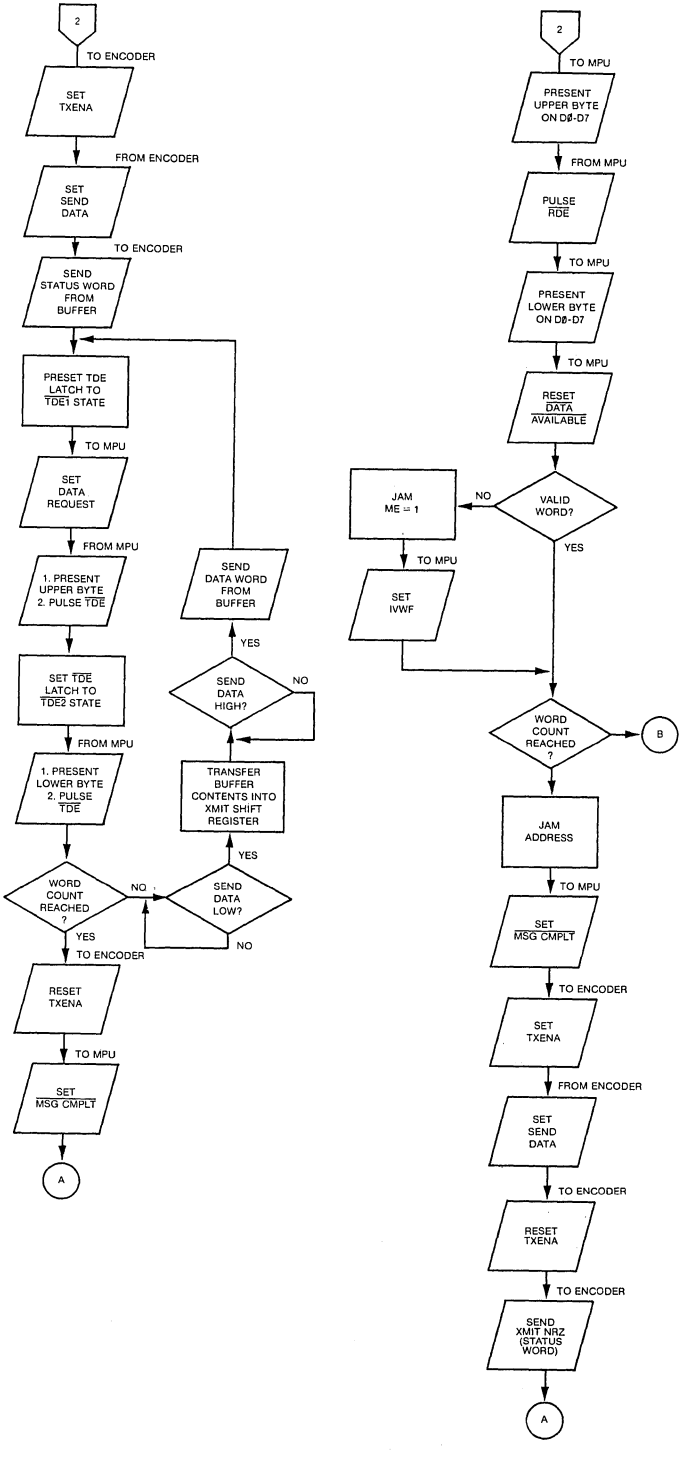

*WORD COUNTER PRESET TO TRANSMIT COMMAND WORD FIELD PLUS 1. THIS ALLOWS FOR THE STATUS WORD.

**$\overline{\text{MSG CMPLT}}$ GENERATED BY THE LAST SEND DATA OF THE TRANSMIT MESSAGE GROUP.

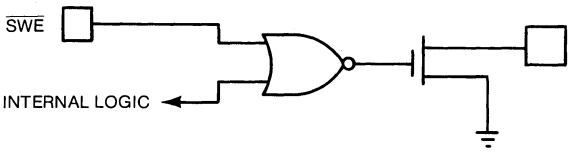
## TYPICAL SYSTEM OPERATION



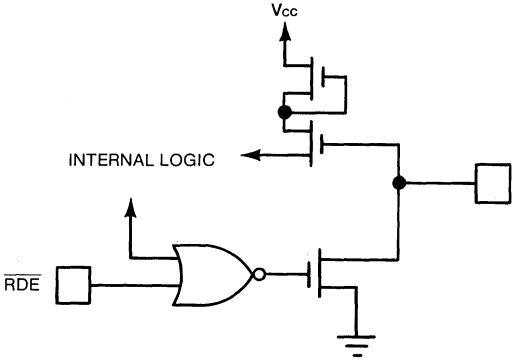

*SEE FIGURE 7 FOR ALLOWABLE TIMES TO SEND $\overline{IA}$


2
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
SEND STATUS WORD FROM BUFFER
PRESET TDE LATCH TO TDE1 STATE
TO MPU
SET DATA REQUEST
FROM MPU
1. PRESENT UPPER BYTE 2. PULSE TDE
SET TDE LATCH TO TDE2 STATE
FROM MPU
1. PRESENT LOWER BYTE 2. PULSE TDE
WORD COUNT REACHED ?
NO
YES
SEND DATA LOW?
YES
NO
TRANSFER BUFFER CONTENTS INTO XMIT SHIFT REGISTER
SEND DATA HIGH?
NO
YES
SEND DATA WORD FROM BUFFER
TO ENCODER
RESET TXENA
TO MPU
SET MSG CMPLT
A
2
TO MPU
PRESENT UPPER BYTE ON DØ-D7
FROM MPU
PULSE RDE
TO MPU
PRESENT LOWER BYTE ON DØ-D7
TO MPU
RESET DATA AVAILABLE
VALID WORD?
NO
YES
JAM ME = 1
TO MPU
SET IVWF
WORD COUNT REACHED ?
B
JAM ADDRESS
TO MPU
SET MSG CMPLT
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
RESET TXENA
TO ENCODER
SEND XMIT NRZ (STATUS WORD)
A

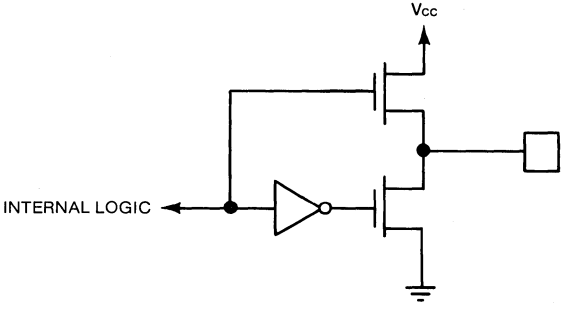
**OPEN DRAIN OUTPUT**
**FIGURE 10**




**DØ-D7 INPUT/OUTPUT**
**FIGURE 11**




**OTHER OUTPUTS**
**FIGURE 12**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX: 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

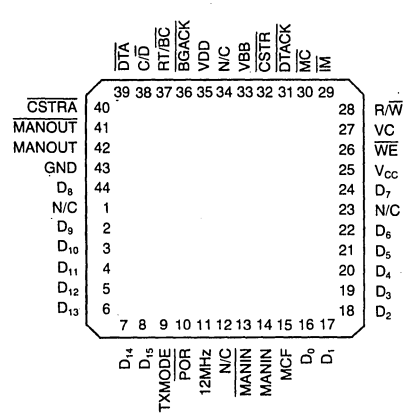
# MIL-STD-1553B "SMART®"



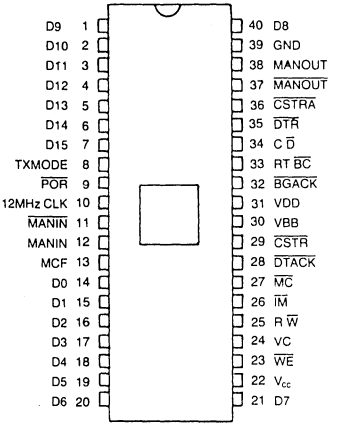
## FEATURES

- ☐ Support of MIL-STD-1553B
- ☐ Operates as both Remote Terminal and Bus Controller
- ☐ Manchester II Serial Biphase Input/Output
- ☐ 16 bit Microprocessor compatible
- ☐ Command/Data Sync Detection/Identification
- ☐ Automatic Command Response Generation
- ☐ On-Chip Address Recognition
- ☐ Error Detection For:
  - Sync Errors
  - Parity Errors
  - Word Count Errors
  - Bit Count Errors
  - Invalid Manchester Code
  - Incorrect Address
  - Incorrect Bus Response Time
- ☐ TTL Compatible
- ☐ Recognizes Mode Codes and Broadcast Commands
- ☐ Provides DMA handshaking signals
- ☐ COPLAMOS® n-Channel MOS Technology

## PIN CONFIGURATION




PACKAGE: 44-pin LCC




PACKAGE: 40-pin D.I.P.

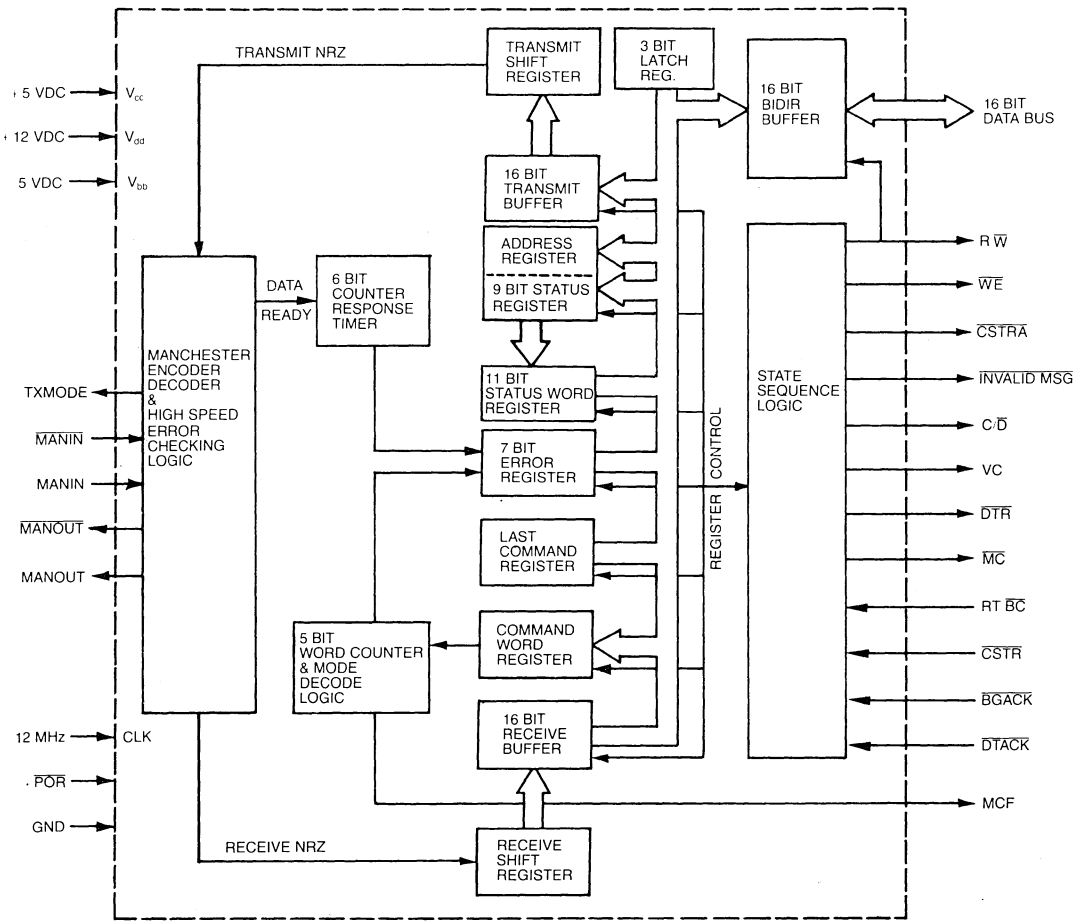
## GENERAL DESCRIPTION

The COM1553B SMART® (Synchronous Mode Avionic Receiver-Transmitter) is a 40-pin COPLAMOS® n-Channel MOS/VLSI circuit designed to simplify the interface of a microprocessor or buffer to the serial MIL-STD-1553B data bus.

The COM1553B is a double buffered serial to parallel, parallel to serial converter. It receives serial Manchester II biphase encoded data from a 1553B bus receiver and converts it to 16 bit parallel data. When receiving Manchester II data, the COM1553B detects and identifies sync polarity, reconstructs the clock, detects zero crossing, checks for the proper number of bits and performs a parity check on the incoming data. In addition to parity check, the COM1553B also checks for sync errors, invalid Manchester code, improper word count, incorrect address and incorrect bus response time. The transmitter in turn, accepts 16 bits parallel data and serially transmits it as Manchester II data, appending the appropriate sync and parity.

The COM1553B recognizes protocol commands, and automatically generates the proper response, thereby offloading what otherwise would be microprocessor tasks. This feature eliminates critical software timing requirements.

The COM1553B is designed to work both as a Bus Controller and Remote Terminal, making it universal within the MIL-STD-1553B environment. The COM1553B automatically loads and recognizes its own address. It determines the type of transfer required in both the Bus Controller and Remote-Terminal modes and generates the proper control signals to complete the transfer. It automatically transmits the status word and detects message errors and mode commands. Furthermore, it generates the control signals for DMA operation, therefore eliminating processor intervention.




**FUNCTIONAL BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1-7, 14-21, 40 | 16-bit Data Bus | D0-D15 | Three-state bidirectional data lines used to transfer Command, Data, Error and Status Words between the COM1553B and external memory. |
| 8 | Transmit Mode | TXMODE | This output signal when high indicates that the COM1553B is transmitting information on the 1553B bus. |
| 9 | Power On Reset | $\overline{POR}$ | Input signal used to initialize or reset the Error registers. The RT address must be reloaded after POR is issued. |
| 10 | 12 MHz Clock | 12 MHz CLK | 12 MHz clock input. |
| 11 | Complementary Manchester In | $\overline{MANIN}$ | This input is low when there is no data on the bus. A high level indicates that the data is in its negative state (Refer to receive waveform, figure 3). |
| 12 | Manchester In | MANIN | This input is low when there is no data on the bus. A high level indicates that the data is in its positive state (Refer to receive waveform, figure 3). |
| 13 | Mode Code Flag | MCF | Output signal that is active high when a mode command (all 1's or all 0's in subaddress) has been detected. |
| 22 | Power Supply | VCC | +5 volts DC supply. |
| 23 | Write Enable | $\overline{WE}$ | Output signal. When low, $\overline{WE}$ indicates that the data on the 16 bit data bus is stable and can be written into the external memory. |
| 24 | Valid Command | VC | Output signal that is pulsed high to signify the reception of a valid command. |
| 25 | Read/Write | R/$\overline{W}$ | Output signal that indicates whether a DMA transaction is a COM1553B read (when high) or a write (when low) operation. |
| 26 | Invalid Message | $\overline{IM}$ | Output signal which is pulsed low at the same time as MC to indicate that a message error has occurred.<br>$\overline{IM}$ is also pulsed low while MC remains high if there are errors in the Command word with matching address. |
| 27 | Message Complete | $\overline{MC}$ | Output signal used as either an interrupt or flag to the processor whenever a COM1553B transaction has been completed. |
| 28 | Data Transfer Acknowledge | $\overline{DTACK}$ | This input signal when low indicates that the Data Transfer Request ($\overline{DTR}$) and $\overline{BGACK}$ has been acknowledged and data is on the data bus. |
| 29 | Command Strobe | $\overline{CSTR}$ | This input signal when low is used to inform the COM1553B that a Command Control Code is available in external memory. When the COM1553B is ready, it issues a Command Strobe Acknowledge and initiates a memory read cycle to load the Command Control Code bits CB2-CB0. |
| 30 | Power Supply | VBB | −5 volts DC supply voltage. |
| 31 | Power Supply | VDD | +12 volts DC supply. |
| 32 | Bus Grant Acknowledge | $\overline{BGACK}$ | This input signal, when low, indicates that the processor has acknowledged $\overline{DTR}$ and relinquished the data bus. |
| 33 | Remote Terminal/Bus Controller | RT/$\overline{BC}$ | When this input is high the COM1553B operates as a Remote Terminal.<br>When RT/$\overline{BC}$ is low, the COM1553B operates as a Bus Controller. |
| 34 | Command/Data | C/$\overline{D}$ | This output signal during memory write operations indicates either a Command or Data Word transfer. A low level indicates that the COM1553B is writing a Data Word, Status Word, the contents of the Error Register, or the contents of the Last Command Register into external memory.<br>A high level indicates that the transferred word is a Command Word. During memory read operations this output is low. It goes high to indicate that data has been latched internally and the read operation is completed. |
| 35 | Data Transfer Request | $\overline{DTR}$ | Output signal that initiates a DMA transfer with the processor. |
| 36 | Command Strobe Acknowledge | $\overline{CSTRA}$ | This output pulse acknowledges the receipt of the command strobe and initiates the Command Control Code (CB2-CB0) transfer. |
| 37 | Complementary Manchester Output | $\overline{MANOUT}$ | This output signal is high when the COM1553B is not transmitting.<br>A low level indicates that output data is in a positive state (refer to driver waveform, figure 4). |
| 38 | Manchester | MANOUT | This output signal is high when the COM1553B is not transmitting.<br>A low level indicates that output data is in a negative state (refer to driver waveform, figure 4). |
| 39 | Ground | GND | Ground |

## FUNCTIONAL DESCRIPTION

The COM1553B is organized into the following five sections:

### Manchester Encoder/Decoder

This section performs the manchester encoder and decoder functions and code error check. The receiver continuously monitors the MANIN and the $\overline{\text{MANIN}}$ input lines for a valid sync. After the reception of the 3 bit sync, the receiver is in full synchronization. It then checks for transition errors and correct (odd) parity. If an error is detected in the Command Word the receiver resets itself, pulses IM and waits for another valid sync. If any errors are detected in Data and Status Words, the appropriate error bits in the Status and Error register are set.

The transmitter section encodes the NRZ data from the data bus into Manchester II and appends, depending on word type, the proper sync and parity.

### State Sequencer Logic

The State Sequencer section generates the appropriate signals to various internal sections to control the overall device operation.

Inputs to the State Sequencer which establish its operational modes are as follows:

**Remote Terminal/Bus Controller (RT/$\overline{\text{BC}}$)**

Determines whether the data terminal is operating as a Remote Terminal or as a Bus Controller. As a result of Dynamic Bus Allocation, any terminal shall be capable of performing either function at different times.

**Command Control Code bits D2-D0 (CB2-CB0)**

These Command Control Code bits determine the type of memory operation the COM1553B will execute. Transfer of these commands to the COM1553B are initiated by asserting Strobe Command ($\overline{\text{CSTR}}$) low. This informs the COM1553B that a command is available in external memory. When the COM1553B acknowledges the $\overline{\text{CSTR}}$ signal, it sets the $\overline{\text{CSTRA}}$ output low. The $\overline{\text{CSTR}}$ must be reset within 1.5 μs after $\overline{\text{CSTRA}}$. The COM1553B then initiates a memory read cycle by setting R/$\overline{\text{W}}$ high, C/$\overline{\text{D}}$ low, and DATA TRANSFER REQUEST ($\overline{\text{DTR}}$) low. When the Command Control Code bits are valid on the bidirectional data bus (D2-D0), $\overline{\text{DTACK}}$ and $\overline{\text{BGACK}}$ are generated by the processor and these bits are loaded into the COM1553B 3-bit latch decode register. The command is then decoded in accordance with Table A. Timing associated with loading these control bits into the COM1553B is shown in Figure 1.

**Transmit Last Command**

Allows the State Sequencer to bypass a memory read cycle to external memory and transmit the Last Command from the TRLC register following the Status Word transmission.

**Broadcast**

When the address field of the Command Word is all ones (11111), the State Sequencer is informed that a Bus Controller or a Remote Terminal is transmitting a Broadcast Command.

**Word Count Zero**

Input from the 5-bit counter and count decode logic informing the State Sequencer that all Data Word memory cycles are complete.

**Sync Input**

Indicates the type of sync word just strobed into the receive register.

**Address Compare**

When programmed as a Remote Terminal, the COM1553B compares the contents of the address register with the address field of the received Command Word. If the addresses compare, the State Sequencer will respond to the received command.

**Any Error**

This input to the State Sequencer indicates that one of the seven possible errors have been set in the error register at the end of a message (Refer to Error register).

**Contiguous Word**

Set if there is a transition 2 μs. after the parity transition of the last word, this signifies that a contiguous word follows the word presently in the receive register (Refer to figure 5).

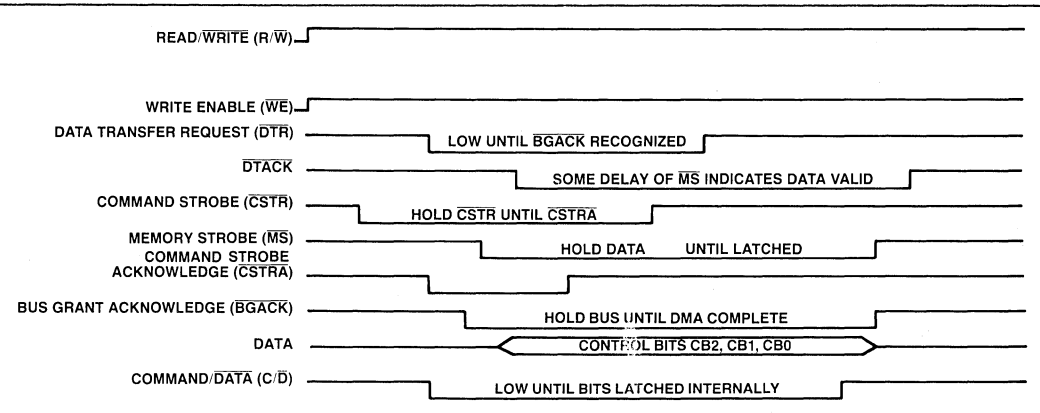



**FIGURE 1:**
**BUS CONTROLLER TIMING SEQUENCE**

Loading the Command Control Code Bits into the COM1553B prior to transmitting a Command or initiating a Diagnostic Sequence.

## Error Detection Logic

The error detection logic of the COM1553B detects the following errors:

**Improper Sync**

One or more words have been received with incorrect sync polarity (For example a Status Word with Data Sync).

**Invalid Manchester II Code**

One or more words have been received with a missing transition during the 17 μs. data and parity bit time.

**Information Field Greater Than 16 Bits**

The decoder has detected a transition within one bit time (1 μs.) following the parity bit in one or more words.

**Odd Parity Error**

One or more words have been received with a parity error.

**Improper Word Count**

An improper word count error occurs when the number of Data Words received is not equal to the number of words indicated in the word count field of the Command Word. In the case of a Mode Code without data, no Data Words should follow the Mode command. Mode Codes with data should consist of only one Data Word. If the contents of the word counter are not zero, and there is no contiguous Data Word, then the receive message is considered incomplete (e.g., fewer words were received than indicated by the word count in the Command word). If the contents of the word counter are zero and there is a transition detected 2 μs. after the parity transition of the last Data Word, then this also will cause an improper word count. In either case, the Message Error bit of the Status Word is set and not transmitted and the invalid message ($\overline{IM}$) output pin pulsed at the same time as the message complete ($\overline{MC}$) signal output.

**Response Time**

The amount of time between the end of transmission of a Command or Data Word and the Status Word reply by a Remote Terminal should be less than 14 μs. If the response is greater than 14 μs. the response error bit is set in the error register.

**Address Mismatch**

An address mismatch occurs when a Bus Controller detects a mismatch between the address of the Status Word reply from a Remote Terminal and the Remote Terminal address of the Command.

## Internal Register Description

**Remote Terminal Address And Status Code Register**

This register is loaded when the processor issues a load Remote Terminal Address (RTA) command. The word that is loaded in this register consists of 9 bits of status information (D0-D8) and the 5-bit address (D11-D15). The Remote Terminal Address may be checked any time by reading out the Error register. The RTA and Status Code register must be loaded before the COM1553B may respond as a Remote Terminal.

Table 1 defines the data bus bits which correspond to the Remote Terminal Address and Status Code register and Status Word that transmitted. Bits D0, D2, D3 and D8 are double buffered to allow the RT to retain this information after the Status Code register is updated. For all legal commands, other than Transmit Last Status and Transmit Last Command Mode command, the Status Word register is updated with these four bits, Any Error and the Broadcast flag. The Dynamic Bus Control and Terminal Flag bits are modified by the appropriate Mode Code commands whereas, the Broadcast Flag and Any Error bits are set by the COM1553B internal logic. The Reserved Bits and the RT address bits are transferred directly into the Status Word register during the RTA and Status Code command.

Bits D0, D2, D3, and D5-D9 are cleared after transmission for all commands except Transmit Last Status and Transmit Last Command Mode Code.



**TABLE A:**
**COMMAND CONTROL CODE BIT DEFINITION**

| | DATA BITS | | | | | | | | | | | | | CONTROL BITS CB2-CB0 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RT/$\overline{BC}$ | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | FUNCTION |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | 1 | X | READ DATA REGISTER |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | 0 | X | LOAD RT ADDRESS REGISTER AND STATUS CODE REGISTER |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | READ LAST CMD |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 0 | 1 | READ ERROR AND REMOTE TERMINAL ADDRESS REGISTERS |
| 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 0 | BUS CONTROLLER TRANSMISSION |
| 0 | X | X | X | X | X | X | X | X | X | X | X | X | X | 0 | 1 | 1 | BUS CONTROLLER RT TO RT TRANSFER |

X—DON'T CARE

## TABLE 1

| Data Bus Bit | RTA and Status Code Reg. Bits | Internal Logic Signals | Status Word Transmitted |
|---|---|---|---|
| D15 (MSB) | RTA Bit 4 (MSB) | — | RTA Bit 4 (MSB) |
| D14 | RTA Bit 3 | — | RTA Bit 3 |
| D13 | RTA Bit 2 | — | RTA Bit 2 |
| D12 | RTA Bit 1 | — | RTA Bit 1 |
| D11 | RTA Bit 0 (LSB) | — | RTA Bit 0 (LSB) |
| D10 | Not used | Any Error | Message Error |
| D9 | Instrumentation Bit | — | Instrumentation |
| D8 | Service Request Bit | — | Service Request |
| D7 | Reserved | — | Reserved |
| D6 | Reserved | — | Reserved |
| D5 | Reserved | — | Reserved |
| D4 | Not Used | Broadcast Flag | Broadcast Flag |
| D3 | Busy | — | Busy |
| D2 | Subsystem Flag Bit | — | Subsystem Flag |
| D1 | Dynamic Bus Control Acceptance Enable Bit (See Note) | Dynamic Bus Mode Code command | Dynamic Bus Control Bit |
| D0 (LSB) | Terminal Flag Enable Bit (See Note) | Inhibit Terminal Flag (set) or Override Terminal Flag (reset) Mode Code command | Terminal Flag |

**Note:** When the Dynamic Bus Control Acceptance Enable bit is set, the RT will accept a Dynamic Bus Mode code request. If this bit is reset the RT will reject a Dynamic Bus Mode Code command request. The Terminal Flag Bit (if enabled) is only set high if no Inhibit Terminal Mode Code command has been received, or if an Override Inhibit Terminal bit command is received.

**Last Command Word Register**

The last valid Command Word received by a Remote Terminal is stored in an internal 16 bit Last Command Register. This makes it readily available for transmission onto the data bus whenever the Remote Terminal receives a Mode Command to transmit the last Command Word. The Last Command Register contents are automatically written into external memory following a receive or a transmit message.

As a bus controller (BC), the Last Command Register is used to hold the command transmitted before the present command. In RT-RT transfers this register of the BC holds the receive command while the transmit command is being transmitted.

The processor has the option of reading the Last Command Register of either a bus controller or remote terminal, by issuing a Read Last Command Register command code.

**Error Register And RTA Register (Error Register)**

A 7-bit error register is provided in the COM1553B to hold any errors associated with the previous message. If one or more of the 7 error types exists, the COM1553B asserts the Invalid Message output pin ($\overline{IM}$) at the same time that Message Complete ($\overline{MC}$) is asserted, cueing either a Remote Terminal or a Bus Controller that an error occurred in the previous message. If desired, the processor may read out the 16-bit error word by issuing a read error register command code. When operating as a Remote Terminal, the COM1553B will write the Receive register, Error register and Last Command register automatically into external memory at the end of each command message because these registers may change before the processor has determined the necessity of reading them. The Error register may be read anytime during a message except during message transfers.

## TABLE 2

The 16-bit error word is defined as follows:

| DATA BUS LINE | ERROR BIT DEFINITION |
|---|---|
| D15 | RT Address Bit 4 |
| D14 | RT Address Bit 3 |
| D13 | RT Address Bit 2 |
| D12 | RT Address Bit 1 |
| D11 | RT Address Bit 0 |
| D10 | Unused |
| D9 | Improper Sync |
| D8 | Address Mismatch Error |
| D7 | Improper Word Count |
| D6 | Response Time Error |
| D5 | Information Field > 16 Bits |
| D4 | Unused |
| D3 | Invalid Manchester II |
| D2 | Parity Error |
| D1 | Unused |
| D0 | Unused |

*Unused bits are set high.

## Mode Detection Logic

Both receive and transmit Command Words for a Remote Terminal and Bus Controller are decoded by the Mode Detection Logic. The Mode Detection Logic examines the following Command Word field to establish the correct operating mode for the COM1553B (Refer to TABLE B).

**Subaddress/Mode Code Field (D5-D9) and Data Word Count/Mode Code (D0-D4)**

This field Determines if the command is a normal command or a Mode command. A subaddress field of 00000 or 11111 implies a Mode command. All other codes are interpreted as a subaddress. Once a Mode Command is detected the most significant bit of the Data Word Count/ Mode Code field is decoded. A most significant bit of "zero" implies no associated data with the Code Command. A "one" in this position implies that a Data Word will follow.

The COM1553B recognizes five Mode Code commands (Refer to TABLE B). Transmit Last Command or Transmit Last Status word Mode Code commands, when received by the COM1553B, will automatically transfer the contents of the Transmit Last Command or Transmit Last Status register onto the 1553B serial bus.

The Override/Inhibit Terminal Flag and Dynamic Bus Control Mode Code commands, when received by the COM1553B, may change the state of the Terminal Flag and Dynamic Bus Control bits of the Status Word register. The Inhibit Terminal Flag Bit Mode Code command resets the Terminal Flag bit.

The Override Inhibit Terminal Flag Mode Code command enables the Terminal Flag bit if it was previously disabled. Finally, Dynamic Bus Control Mode Code command sets the Dynamic Bus Control bit in the Status Word if the Dynamic Bus Control Enable bit is high. If the enable bit is low, the Dynamic Bus Control bit in the Status Word remains low when a Dynamic Bus Control Mode Code command is received.

**Broadcast Mode Code**

Broadcast Mode Code Commands are acknowledged if the T/$\overline{R}$ bit is low. If the T/$\overline{R}$ bit is high all Broadcast Mode Code commands without associated Data words are acknowledged except Dynamic Bus Control and Transmit Last Status Word.

Illegal Broadcast Commands are not acknowledged; the IM output pin is, however, pulsed low.



### TABLE B
### MODE CODE DEFINITION

| FUNCTION | DETECT CONDITION | DETECTED BY | SPECIAL CONDITIONS | COMMENTS |
|---|---|---|---|---|
| Broadcast | All ones in RT address field of CMD WD | Broadcast Decode Logic | Status word is written into Memory but not transmitted | Address compare must recognize all ones as Broadcast |
| Mode Codes | All zeros or ones in sub-address field of CMD WD | Mode Code Decode Logic | MSB of Word Count<br>0 = No data Word<br>1 = With Data Word | Word Count is Decoded as mode code |
| (1) Dynamic Bus Control | | | Word Count Field = 00000 | Dynamic Bus Accept Bit of Status word enabled for transmission |
| (2) Transmit Last Status Word | | | Word Count Field = 00010 | Status Word remains unchanged |
| (3) Inhibit Terminal Flag Bit | | | Word Count Field = 00110 | Terminal Flag Bit of Status word inhibited until overriden |
| (4) Override Inhibit Terminal Flag Bit | | | Word Count Field = 00111 | Removes Inhibit from Terminal Flag Bit of Status Word |
| (5) Transmit Last Command | | | Word Count Field = 10010 | Status Word Transmitted followed by Last Command Register. Status Word remains unchanged. |

## OPERATION

When operating as either a Bus Controller or Remote Terminal, the COM1553B decodes the Command Word and determines the type of message transfer. Having determined the type of message transfer, the COM1553B generates the proper control and timing signals to complete the transfer (refer to Figure 2). The types of messages are listed below:

1) Bus Controller to Remote Terminal
2) Remote Terminal to Bus Controller
3) Remote Terminal to Remote Terminal
4) Mode Code without Data Word
5) Mode Code with Data Word (transmit)
6) Mode Code with Data Word (receive)
7) Broadcast Bus Controller to Remote Terminal
8) Broadcast Remote Terminal to Remote Terminal
9) Broadcast Mode Code without data
10) Broadcast Mode Code with data

## Bus Controller Transaction (RT/$\overline{BC}$ of the COM1553B set low)

The following section describes each 1553B information transfer format from the Bus Controller viewpoint. A table showing external memory operation is also provided for each message format.

Note that all MIL-STD-1553B serial bus activity is initiated by the Bus Controller.

**Bus Controller-to-Remote Terminal Transfer (BC to RT)**

This message format covers transactions where the Bus Controller transmits a receive Command and Data Words to a Remote Terminal. Initializing the COM1553B is accomplished by the processor loading an external memory address counter with the starting address of the COM1553B memory control block (address where the Command Control Code CB2-CB0 resides). The Bus Controller processor next issues a Command Strobe ($\overline{CSTR}$) and holds it low until the COM1553B issues a Command Strobe Acknowledge ($\overline{CSTRA}$). The COM1553B then responds with a Data Transfer Request ($\overline{DTR}$) which initiates a normal memory cycle.

Refer to figure 1 for timing associated with loading the Command Control Codes (CB2-CB0) into the COM1553B prior to transmitting the Command Word.

The first memory cycle loads the Command Control Code bits CB2-CB0 from external memory into the COM1553B functioning as Bus Controller (BC). The BC decodes this command to determine the type of memory transaction to perform (refer to TABLE A). The next read cycle loads the Command Word into the BC command register and then transmits it onto the 1553B bus. This Command Word, while in the command register, determines the BC mode of operation. The BC then completes this BC to RT transaction by issuing a predetermined number of read cycles (determined by the value in the word count field of the Command Word) and transmitting the data onto the 1553B bus. After transmission of the last Data word, the BC initializes its response timer, expecting a Status Word from the remote terminal within 14 μs.

After the reception of the Status Word, the BC initiates a memory write cycle which writes the Status Word into the external memory. If the BC doesn't receive the Status Word within the allowed response time the message error bit is set.

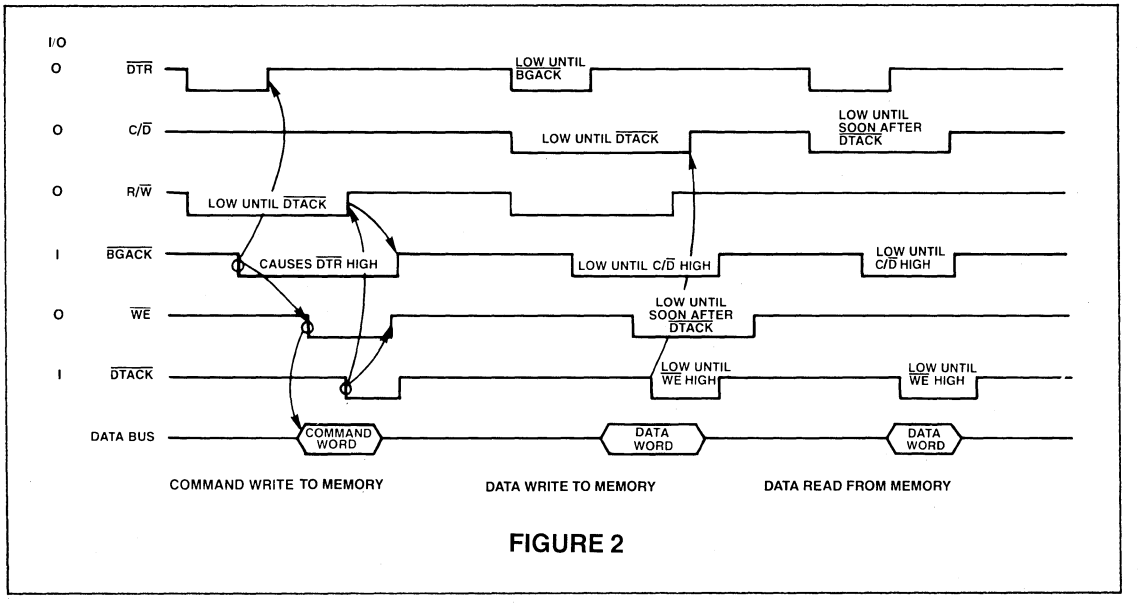



**FIGURE 2**

## TABLE 3
## BC to RT (The BC transmits a receive command to the RT)

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | RECEIVE COMMAND | READ |
| 3 | DATA | READ |
| • | DATA | READ |
| • | DATA | READ |
| 34 | DATA | READ |
| | ** | |
| 35 | STATUS | WRITE |

*reads command control code bits CB2-CB0
** response time
X = don't care

**Remote Terminal Transfer to Bus Controller**

This message format covers transactions where the Bus Controller sends a transmit command to a Remote Terminal and requests data from it. Initialization of the BC for normal memory cycles is the same as the previous transfer. The difference between this transfer and the previous transfer is that after the Command Word is transmitted, the BC waits 14 μs for the Status Word and the requested number of Data Words. The Status and Data Words are written into external memory via write cycles as they are received by the BC.

## TABLE 4
## BC to RT (The BC transmits a Transmit Command to an RT)

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | TRANSMIT COMMAND | READ |
| | ** | |
| 3 | STATUS | WRITE |
| 4 | DATA | WRITE |
| • | DATA | WRITE |
| • | DATA | WRITE |
| 35 | DATA | WRITE |

*reads command control code bits CB2-CB0
** response time
X = don't care

**RT-to-RT Transfer**

In this message format, the Bus Controller first issues a receive Command Word to the receiving Remote Terminal, followed by a transmit Command Word to the transmitting terminal. Next, the transmitting RT responds with a Status Word and the requested number of Data Words to both the receiving RT and BC. The receiving RT at the end of the message sends a Status Word to the BC. As Status and Data Words are received by the BC they are written into external memory.

## TABLE 5
## RT to RT

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX3_H$ | READ* |
| 2 | RECEIVE COMMAND | READ |
| 3 | TRANSMIT COMMAND | READ |
| 4 | STATUS (transmitting RT) | WRITE |
| 5 | DATA | WRITE |
| • | DATA | WRITE |
| • | DATA | WRITE |
| 36 | DATA | WRITE |
| | ** | |
| 37 | STATUS (receiving RT) | WRITE |

*reads command control code bits CB2-CB0
** response time
X = don't care

**Mode Code Command without Data**

The Bus Controller transmits a specific Mode Command and expects a Status Word back from the addressed Remote Terminal.

## TABLE 6

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | COMMAND | READ |
| | ** | |
| 3 | STATUS | WRITE |

*reads command control code bits CB2-CB0
** response time
X = don't care

**Mode Command with Data (BC receives a single word)**

In this mode the Bus Controller issues a transmit Mode Command to an RT. The addressed Terminal responds to the Bus Controller with a Status Word and a single Data Word.

## TABLE 7

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | COMMAND | READ |
| | ** | |
| 3 | STATUS | WRITE |
| 4 | DATA | WRITE |

*reads command control code bits CB2-CB0
** response time
X = don't care

**Mode Command with Data (BC transmits a single word)**

The Bus Controller issues a receive Mode Command and one Data Word to a Remote Terminal. A Status Word is returned by the Remote Terminal to the Bus Controller.

**TABLE 8**

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | COMMAND | READ |
| 3 | DATA | READ |
| | ** | |
| 4 | STATUS | WRITE |

*reads command control code bits CB2-CB0
**response time
X = don't care

**Bus Controller (Broadcast) to Remote Terminal Transfer**

In this mode the Bus Controller issues a Broadcast Command followed by a number of Data Words. In all Broadcast Command transfers a BC will not expect to receive a Status Word back.

**TABLE 9**

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX2_H$ | READ* |
| 2 | RECEIVE COMMAND | READ |
| 3 | DATA | READ |
| • | DATA | READ |
| • | DATA | READ |
| 34 | DATA | READ |

*reads command control code bits CB2-CB0
**response time
X = don't care

**RT to RT Transfer (Broadcast)**

This transfer is similar to the normal RT to RT transfer with the exception that the Status Word is not returned by the receiving RT.

**TABLE 10**

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | $XXX3_H$ | READ* |
| 2 | RECEIVE COMMAND | READ |
| 3 | TRANSMIT COMMAND | READ |
| | ** | |
| 4 | STATUS | WRITE |
| 5 | DATA | WRITE |
| • | DATA | WRITE |
| • | DATA | WRITE |
| 36 | DATA | WRITE |

*reads command control code bits CB2-CB0
**response time
X = don't care

**THE FOLLOWING NOTE APPLIES TO THE CURRENT VERSION OF THE COM 1553B:**

When operating as a Bus Controller in a RT (Remote Terminal) to RT transfer, the COM1553B may incorrectly set the Invalid Sync Bit in the Error Register if the status word response from the receiving RT occurs between 4 and 7 microseconds.

The Bus Controller (BC) may confirm that an error free message transmission occurred by requesting that the receiving RT transmit the last status word. If this status word matches the previous status word, then an error-free transmission occurred.

## Remote Terminal Transaction (RT/$\overline{BC}$ input of the COM1553B set high)

The following section addresses each COM1553B information transfer format from the Remote Terminal viewpoint.

**Bus Controller to Remote Terminal Transfer (BC to RT, where RT receives data)**

In this transfer the COM1553B designated as the RT receives a command to receive data. As the Command Word is completely shifted into the receive shift register, the RT compares the Command Word address field with the preloaded Remote Terminal address. This determines if the message is addressed to the receiving RT. If the Command Word is valid, the RT issues a Data Transfer Request ($\overline{DTR}$) to initiate a memory cycle. Once the processor relinquishes control of the data bus, during the Bus Acknowledge ($\overline{BGACK}$) time, the Command Word is placed on the data bus.

The Subaddress field is thereafter decoded by external logic and the Command word is written into external memory. The RT then receives a predetermined number of Data Words (specified by the word count field). As each Data Word is received it is written into external memory. After the reception of the last Data Word the RT transmits the Status Word, the Message Error, Broadcast Flag, Terminal Flag, Subsystem Flag, Busy, and Service Request bits are updated for all commands except for the Transmit Status Word and Transmit Last Command Code commands. While transmitting the Status, the RT writes it into memory. The RT also writes the Last Command Register, Error Register and Receive Register into memory and then asserts Message complete.

Note that the receive register of the RT will contain the transmitted Status Word.

## TABLE 11
## BC TO RT (RT receives data from BC)

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND | WRITE |
| 2 | DATA | WRITE |
| 3 | DATA | WRITE |
| • | • | WRITE |
| • | • | WRITE |
| 34 | DATA ** | WRITE |
| 35 | STATUS | WRITE |
| 36 | LAST COMMAND | WRITE |
| 37 | ERROR REGISTER | WRITE |
| 38 | RECEIVE REGISTER | WRITE |

**Remote Terminal-to-Bus Controller Transfer (RT transmits data to BC)**

The Remote Terminal receives a Transmit Command Word from the Bus Controller. The RT will then proceed to decode the Command Word, as in the previous case and within the response time transmits the Status Word.

While the Status Word is being transmitted the RT issues a write memory cycle to write the Status Word into external memory. Thereafter, the Data words are read from memory and transmitted. After the last word is transmitted the RT writes the contents of the Last Command Register, Error Register and the Receive Register into memory.

## TABLE 12
## Remote Terminal to Bus Controller (RT Transmits Data to BC)

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND ** | WRITE |
| 2 | STATUS | WRITE |
| 3 | DATA | READ |
| • | DATA | READ |
| • | DATA | READ |
| 34 | DATA | READ |
| 35 | LAST COMMAND | WRITE |
| 36 | ERROR REGISTER | WRITE |
| 37 | RECEIVE REGISTER | WRITE |

**response time

**Remote Terminal-to-Remote Terminal Transfers**

From the Remote Terminal viewpoint, RT-to-RT transfers are similar to the RT to BC receive or transmit data transfers. The only exception is that the receiving terminal waits for the first Data Word from the transmitting terminal. This satisfies the protocol requirement that the transmitting terminal first send its status to the controller before it transmits the data to the receiving terminal.

**Mode Command with Data (RT receives a Mode Code Command to transmit)**

In this transfer, after the Transmit Mode Command is received, the RT transmits the Status and one Data Word.



## TABLE 13

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND ** | WRITE |
| 2 | STATUS | WRITE |
| 3 | DATA | READ* |
| 4 | LAST COMMAND | WRITE |
| 5 | ERROR REGISTER | WRITE |
| 6 | RECEIVE REGISTER | WRITE |

*For a Transmit Last command Mode Code, Data is not read from memory but transmitted from the internal Last Command register.

** response time

**Mode Code Command with Data (RT receives a Mode Command to receive)**

This transfer is similar to a Receive Command having only one Data Word.

## TABLE 14

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND | WRITE |
| 2 | DATA ** | WRITE |
| 3 | STATUS | WRITE |
| 4 | LAST COMMAND | WRITE |
| 5 | ERROR REGISTER | WRITE |
| 6 | RECEIVE REGISTER | WRITE |

** response time

**Bus Controller Broadcast Transfer to RT**

The RT receives a Broadcast Command to receive data. If data received during a broadcast message is invalid, the COM1553B will set the message error bit.

## TABLE 15
## RT RECEIVE

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND | WRITE |
| 2 | DATA | WRITE |
| • | DATA | WRITE |
| • | DATA | WRITE |
| 32 | DATA | WRITE |
| 33 | STATUS | WRITE* |
| 34 | LAST COMMAND | WRITE |
| 35 | ERROR REGISTER | WRITE |

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

**Broadcast Mode Code Command with Data**

This Broadcast Mode Code command is detected if the MSB of the word count field is a logical high.

Transmission of the Status Word is suppressed as in the previous case but is loaded into external memory.

## TABLE 16
## RT RECEIVE

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND | WRITE |
| 2 | DATA | WRITE |
| 3 | STATUS | WRITE* |
| 4 | LAST COMMAND | WRITE |
| 5 | ERROR REGISTER | WRITE |

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

**Broadcast Mode Code Command Without Data**

This Mode Code command is detected if the MSB of the word count field is zero. This transaction is the same as the previous transfer except that there is no Data Word transfer.

## TABLE 17

| MEMORY ADDRESS | MEMORY CONTENTS | COM1553B MEMORY OPERATION |
|---|---|---|
| 1 | COMMAND | WRITE |
| 2 | STATUS | WRITE* |
| 3 | LAST COMMAND | WRITE |
| 4 | ERROR REGISTER | WRITE |

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

**Broadcast RT to RT Transfer**

For this message transfer a Broadcast Command to receive is issued by the Bus Controller. This is followed by a normal Transmit Command to the transmitting Remote Terminal. The Remote Terminal responds with a normal transmit message format of Status Word and Data Word(s). The receiving terminals do not transmit a Status Word after receiving the data. However, they do go through a memory cycle to load the Status Word into their respective memories.

For the Remote Terminal receive transfer refer to Table 15. The only difference in this transfer is that there is a gap time between the Command and Data word.

For the Remote Terminal transmit transfer refer to Table 12. The only difference in this transfer is that the Receive Register is not written into memory.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −55 to +125°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... +15V
Negative Voltage on any pin except VBB, with respect to ground ..... −.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.



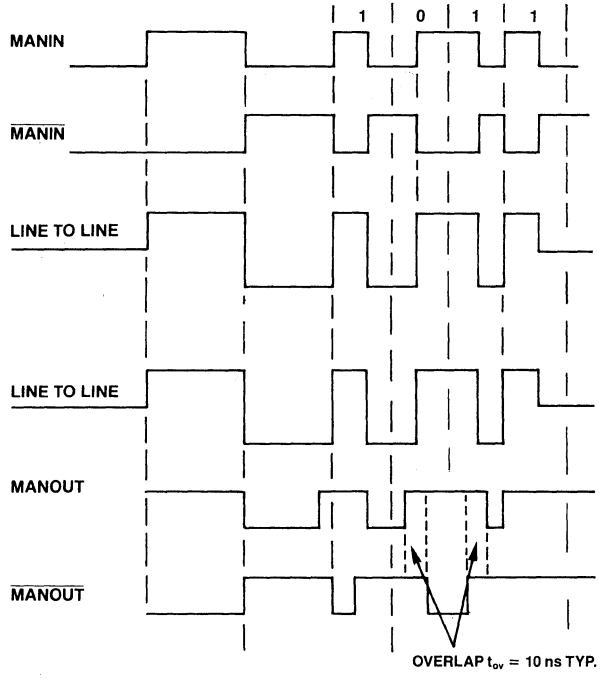
## DC ELECTRICAL CHARACTERISTICS $T_A = -55$ to 125°C, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.3 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 3 | | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL} = -3.2$ mA |
| $V_{OH}$ | Output High Voltage | 2.4 | 4 | 5 | V | $I_{OH} = .8$ mA |
| $I_L$ | Input Leakage Current | | | 10 | µA | |
| $C_{IN}$ | Input Capacitance | | 10 | 25 | pf | |
| $C_o$ | Output Capacitance | | 10 | 15 | pf | |
| $C_L$ | Load Capacitance | | 100 | 150 | pf | |
| $P_W$ | Power Dissipation | | 0.8 | | W | $T_A = 25°C$ |
| $I_{DD}$ | | | | 40 | mA | |
| $I_{CC}$ | | | | 100 | mA | |
| $I_{BB}$ | | | | 5 | mA | |

## AC ELECTRICAL CHARACTERISTICS

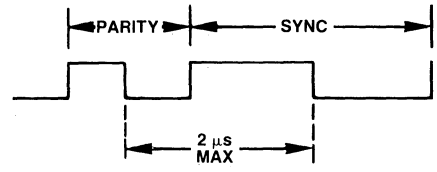
| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| clk | clock frequency | | 12 | | MHz | 50% duty cycle |
| $t_r$ | Clk, rise time | | 6 | | ns | |
| $t_f$ | Clk, fall time | | 6 | | ns | |
| $t_1$ | $\overline{DTR}$ and $\overline{WE}$ | 0.5 | 0.6 | 1 | µs | |
| $t_2$ | $\overline{BGACK}$ to $\overline{DTR}$ | 0.8 | 1.3 | 2 | µs | |
| $t_3$ | $\overline{WE}$ to DATA | 50 | 100 | | ns | |
| $t_4$ | $\overline{DTACK}$ to $\overline{WE}$ | | 1.5 | 2 | µs | |
| $t_5$ | $\overline{DTACK}$ to R/$\overline{W}$ | | 1 | 1.5 | µs | |
| $t_6$ | $\overline{DTACK}$ to C/$\overline{D}$ | | 1.5 | 2.5 | µs | |
| $t_7$ | $\overline{CSTR}$ to $\overline{CSTRA}$ | | | 673 | µs | |
| $t_8$ | $\overline{CSTRA}$ to $\overline{CSTR}$ | | | 1.5 | µs | |
| $t_9$ | $\overline{CSTRA}$ width | | 500 | | ns | |
| $t_{10}$ | C/$\overline{D}$ to DATA | 0 | | | | |
| $t_{11}$ | CMD to $\overline{IM}$ | | | 3.25 | µs | |
| $t_{12}$ | $\overline{IM}$ width | | | 500 | ns | |
| $t_{13}$ | VC width | | | 1 | µs | |
| $t_{14}$ | VC to $\overline{IM}$ | | | 1.75 | µs | |
| $t_{15}$ | C/$\overline{D}$ to MC | | | 700 | ns | |
| $t_{16}$ | C/$\overline{D}$ to $\overline{IM}$ | | | 2.25 | µs | |
| $t_{17}$ | C/$\overline{D}$ to MC | | | 750 | ns | |
| $t_{18}$ | C/$\overline{D}$ to MC | | | 1.25 | µs | |
| $t_{19}$ | CMD to MCF reset | | | 3.75 | µs | |
| $t_{20}$ | CMD to MCF set | | | 4.75 | µs | |
| $t_{21}$ | CMD to VC | | | 2.75 | µs | |
| $t_{22}$ | C/$\overline{D}$ to MCF reset | | | 1.5 | µs | |
| $t_{23}$ | C/$\overline{D}$ to MCF set | | | 1 | µs | |
| $t_{24}$ | POR width | 2.5 | | | µs | |
| $t_{25}$ | Receive CMD to $\overline{DTR}$ | | | 4.25 | µs | |
| $t_{26}$ | Transmit CMD to $\overline{DTR}$ | | | 5.75 | µs | |

## FIGURE 3:
## RECEIVER LOGIC WAVEFORMS

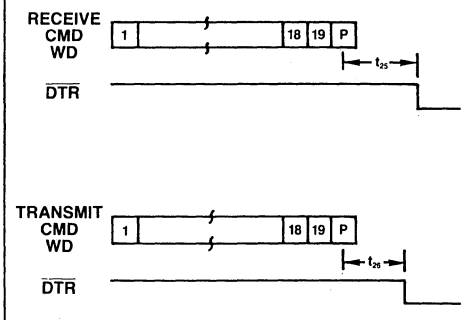



## FIGURE 4:
## DRIVER LOGIC WAVEFORMS

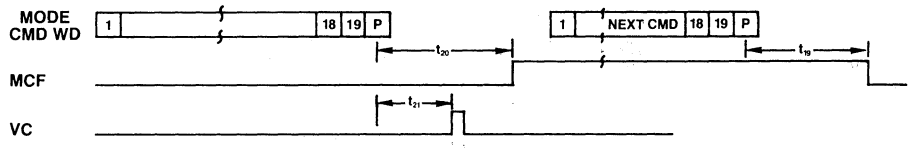
## FIGURE 5:
## CONTIGUOUS WORD



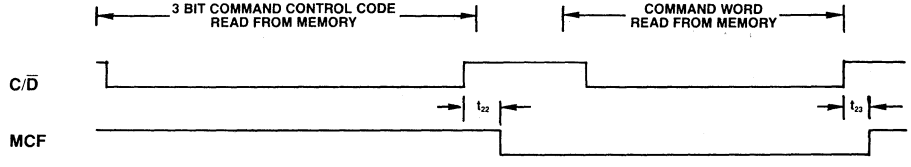

## DTR VS COMMAND WORD



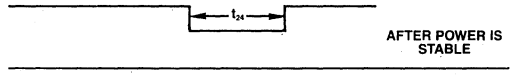

## MODE CODE FLAG (MCF) AS A RT



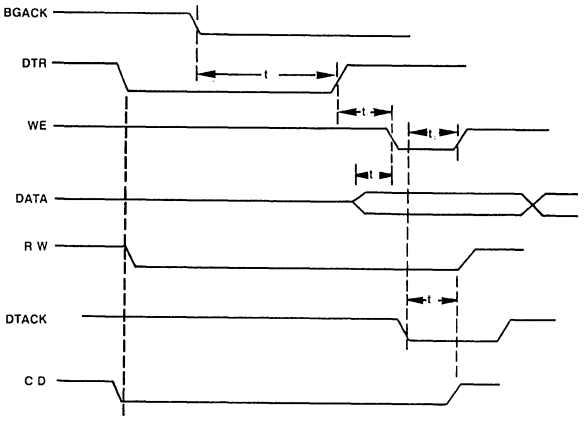

## AS A BC



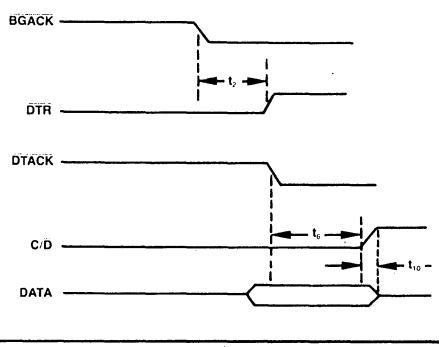

## POR

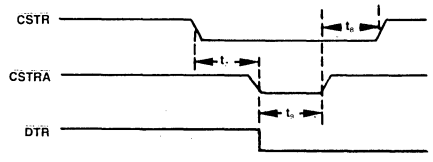


## AC CHARACTERISTICS

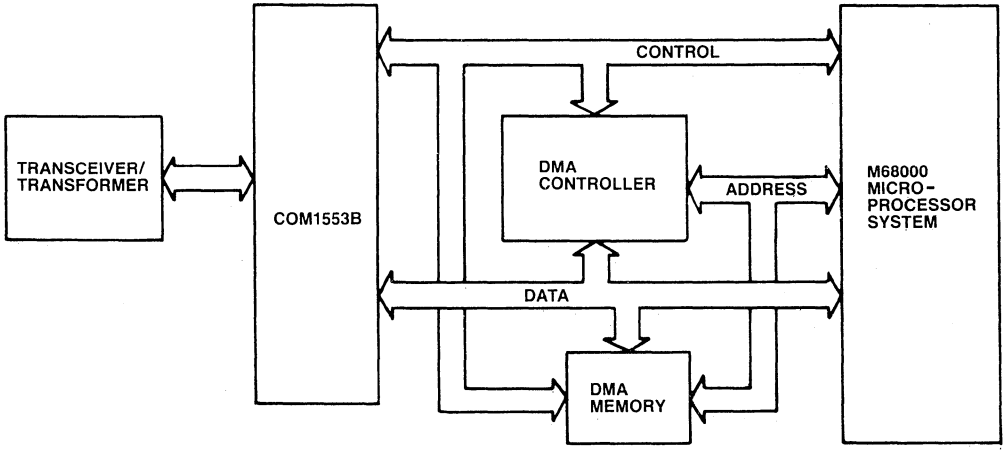



WRITE CYCLE



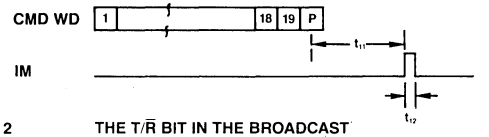

READ CYCLE



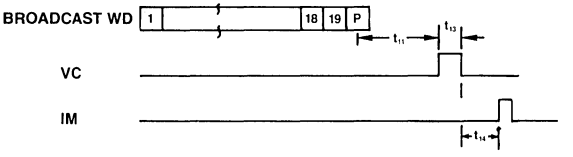

TYPICAL SYSTEM IMPLEMENTATION

## INVALID MESSAGE (IM) AS A RT

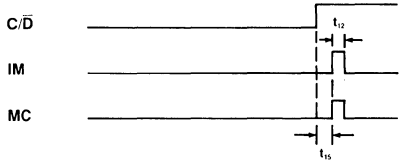
CASE 1



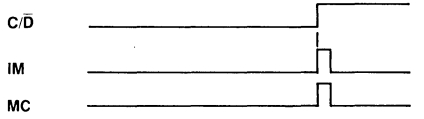

CASE 2 THE T/$\overline{R}$ BIT IN THE BROADCAST CMD IS SET HIGH.




CASE 3 AN ERROR OCCURRED DURING A BROADCAST CMD

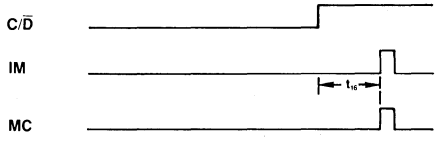



CASE 4 NON BROADCAST CMD



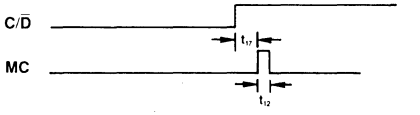

### AS A BC

CASE 5 A TRANSMIT OR RECEIVE BC TRANSFER

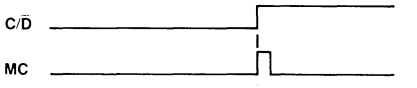



## MESSAGE COMPLETE (MC) AS A RT

CASE 1 AT THE COMPLETION OF AN ERROR FREE BROADCAST COMMAND TRANSACTION AFTER THE ERROR REGISTER IS WRITTEN INTO MEMORY.

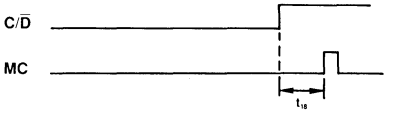



CASE 2 AT THE COMPLETION OF A TRANSMIT OR RECEIVE COMMAND TRANSACTION AFTER THE DATA REGISTER IS WRITTEN INTO MEMORY.



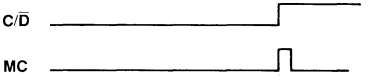

### AS A BC

CASE 3 WHEN THE BC ISSUES A RECEIVE COMMAND, THE MC SIGNAL OCCURS AFTER THE STATUS WORD IS WRITTEN INTO MEMORY.
OR
WHEN THE BC ISSUES A TRANSMIT COMMAND, THE MC SIGNAL OCCURS AFTER THE LAST DATA WORD IS WRITTEN INTO MEMORY.

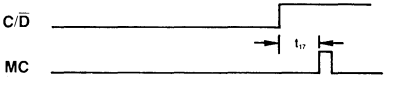



### AS A BC OR RT

CASE 4 AT THE COMPLETION OF LOADING THE RT ADDRESS REGISTER OR READING THE DATA REGISTER.




CASE 5 AFTER READING THE ERROR REGISTER.




**NOTE:** Message complete and invalid message outputs of the COM 1553B are negative pulses i.e. $\overline{MC}$ and $\overline{IM}$.


STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898



Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Asynchronous/Synchronous Transmitter-Receiver

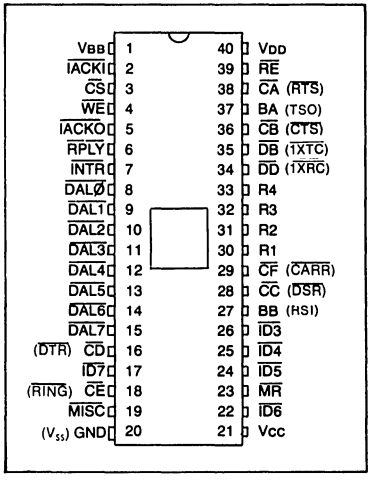
# ASTRO



## FEATURES

- ☐ SYNCHRONOUS AND ASYNCHRONOUS
  - Full Duplex Operations
- ☐ SYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Two Successive SYN Characters Sets Synchronization
  - Programmable SYN and DLE Character Stripping
  - Programmable SYN and DLE-SYN Fill
- ☐ ASYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Selection
  - Start Bit Verification
  - Automatic Serial Echo Mode
- ☐ BAUD RATE—DC TO 1M BAUD
- ☐ 8 SELECTABLE CLOCK RATES
  - Accepts 1X Clock and Up To 4 Different 32X Baud Rate Clock Inputs
  - Up to 47% Distortion Allowance With 32X Clock
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data
  - 8-Bit Bi-Directional Bus For Data, Status, and Control Words
  - All Inputs and Outputs TTL Compatible
  - Up To 32 ASTROS Can Be Addressed On Bus
  - On-Line Diagnostic Capability
- ☐ ERROR DETECTION
  - Parity, Overrun and Framing

## PIN CONFIGURATION




- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Pin for Pin replacement for Western Digital UC1671 and National INS 1671
- ☐ Baud Rate Clocks Generated by COM5036 @ 1X and COM5016-6 @ 32X

## APPLICATIONS

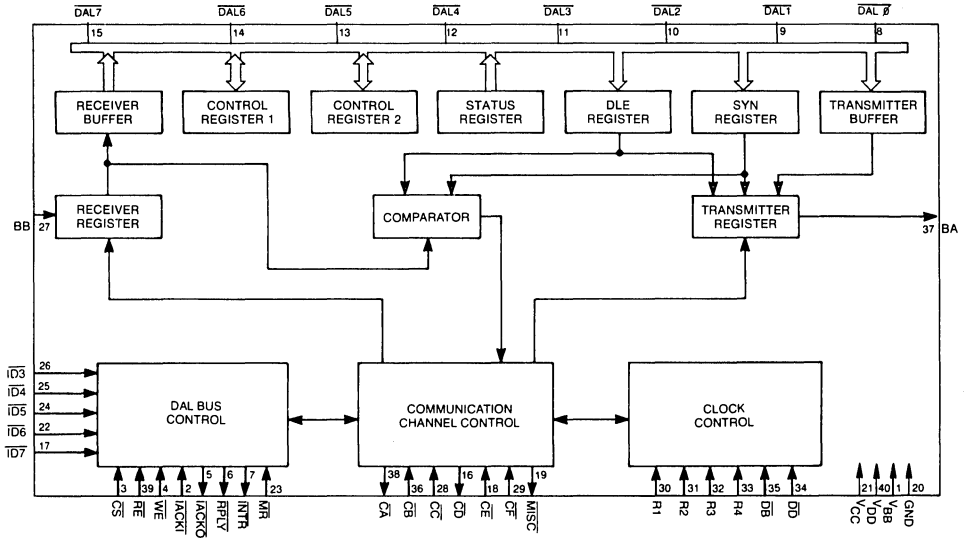
Synchronous Communications
Asynchronous Communications
Serial/Parallel Communications

## General Description

The COM1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO contains several "handshaking" signals to insure easy interfacing with modems or other peripheral devices such as display terminals. In addition, a programmable diagnostic mode allows the selection of an internal looping feature which allows the device to be internally connected for processor testing.

The COM1671 provides the system communication designer with a software responsive device capable of handling complex communication formats in a variety of system applications.




## Organization

**Data Access Lines** — The DAL bus is an 8-bit bi-directional port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL bus also transfers information related to addressing of the device, reading and writing requests, and interrupting information.

**Receiver Buffer** — This 8-bit parallel register presents assembled received characters to the DAL bus when requested through a Read operation.

**Receiver Register** — This 8-bit shift register inputs the received data at a clock rate determined by Control Register 2. The incoming data is assembled to the selected character length and then transferred to the Receiver Buffer with logic zeroes filling out any unused high-order bit positions.

**Syn Register** — This 8-bit register is loaded from the DAL bus by a Write operation and holds the synchronization code used for receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Buffer during transmission. This register cannot be read onto the DAL bus. It must be loaded with logic zeroes in all unused high-order bits.

**Comparator** — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or the DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Buffer. A bit in the Status Register is set when stripping is effected. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

**DLE Register** — This 8-bit register is loaded from the DAL bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

**Status Register** — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL bus by a Read operation.

**Control Registers** — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL bus by a Write operation or read onto the DAL bus by a Read operation. The registers are cleared by a Master Reset.

**Transmitter Buffer** — This 8-bit parallel register holds data transferred from the DAL bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

**Transmitter Register** — This 8-bit shift register is loaded from the Transmitter Buffer, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the serial data output.

# Astro Operation

## Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic 0) at the beginning of a character and a Stop bit(s) (logic 1) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit(s). The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit(s) after reception of the last character bit (including the parity bit, if selected). If the Stop bit(s) is a logic 1, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit(s) is a logic 0, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic 0 when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit(s) location, the first sampled logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Buffer is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (including the parity bit, if selected), then the insertion of a 1, 1.5, or 2 bit length Stop condition. If the Transmitter Buffer is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic 1) condition is continually transmitted until the Transmitter Buffer is loaded.

## Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two contiguous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Buffer, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Buffer is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

## Astro Operation

### Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit with +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Check by 1/32nd of a bit period. The Sampling clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is transferred to the Receiver Buffer; the unused, higher order bits are filled with logic zero's. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Registers. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is transferred to the Receiver Buffer. This error flag indicates that a character has been lost; new data is lost while the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the content of the SYN or the DLE register are not loaded into the Receiver Buffer, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23) or Bit 4 of Control Register 1 (CR14) are set respectively, and SYN Detect and DLE Detect are set with the next non SYN or non DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

### Transmitter

Information is transferred to the Transmitter Buffer by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data occurs only when the Request to Send bit is set to a logic 1 in Control Register 1 and the $\overline{\text{Clear To Send}}$ input is logic 0. Information is normally transferred from the Transmitter Buffer to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Buffer if the Force DLE signal condition is enabled (Bits 5 and 6 of Control Register 1 set to a logic 1). The control bit CR15 must be set prior to loading of a new character in the Transmitter Buffer to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Buffer Empty Flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Buffer, when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Buffer is empty. If the Transmitter Buffer is empty, when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic 1 will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (CR16 = 1), the idle state will be filled by DLE-SYN character transmission in that order. When entering the Transparent mode DLE must precede the contents of the Transmitter Buffer. This is accomplished by setting of Bit 5 of Control Register 1.

If the transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the $\overline{\text{Clear To Send}}$ goes high the transmitted data output will go high.

When the Transmitter parity is enabled, the selected Odd or Even parity bit is inserted into the last data bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

## Input/Output Operations

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular ASTRO, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or input takes data from the ASTRO and places it on the DAL bus, while a Write or Output places data from the DAL bus into the ASTRO.

A Read or Write operation is initiated by the placement of an eight-bit address on the DAL bus by the Controller. When the Chip Select signal goes to a logic 0 state, the ASTRO compares Bits 7-3 of the DAL bus with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its RPLY line low to acknowledge its readiness to transfer data. Bit 0 must be a logic O in Read or Write operation. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations.

### Read

Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

| Bits 2-0 | Selected Register |
|---|---|
| 000 | Control Register 1 |
| 010 | Control Register 2 |
| 100 | Status Register |
| 110 | Receiver Buffer |

When the Read Enable (RE) line is set to a logic 0 condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL bus. The Read operation terminates, and the device becomes unselected, when both the Chip Select and Read Enable return to a logic 1 condition. Reading of the Receiver Buffer clears the Data Received Status bit. The data is removed from the DAL bus when the RE signal returns to the logic high state.

### Write

Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

| Bits 2-0 | Selected Register |
|---|---|
| 000 | Control Register 1 |
| 010 | Control Register 2 |
| 100 | SYN and DLE Register |
| 110 | Transmitter Buffer |

When the Write Enable (WE) line is set to a logic 0 condition by the Controller the ASTRO gates the data from the DAL bus into the addressed register. If data is written into the Transmitter Buffer, the TBMT Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses or other ASTROs resets this condition such that the next 100 will address the SYN register.

### Interrupts

The following conditions generate interrupts:

**Data Received (DR)**
Indicates transfer of a new character to the Receiver Buffer while the Receiver is enabled.

**Transmitter Buffer Empty (TBMT)**
Indicates that the Transmitter Buffer is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty Transmitter Buffer, or after the character is transferred to the Transmitter Register making the Transmitter Buffer empty.

**Carrier On**
Indicates Carrier Detector input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

**Carrier Off**
Indicates Carrier Detector input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

**Data Set Ready On**
Indicates the Data Set Ready input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

**Data Set Ready Off**
Indicates the Data Set Ready input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

**Ring On**
Indicates the Ring Indicator input goes low and the Data Terminal Ready (DTR) bit (CR10) is low.

Each time an interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a low state. On this transition all non-interrupting devices receiving the IACKI signal set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the interrupt request. The highest priority device that is interrupting will then set its RPLY line low. This device will place its ID code on Bit Positions 7-3 of the DAL bus when a low RE signal is received. The data is removed from the DAL bus when the Read Enable (RE) signal returns to the logic one state. To reset the Interrupt condition (INTR) Chip Select (CS) and IACKI must be received by the ASTRO.

## Description of Pin Functions

| Pin No. | Symbol | Pin Name | I/O | Function |
|---|---|---|---|---|
| 1 | $V_{BB}$ | POWER SUPPLY | PS | − 5 Volts |
| 21 | $V_{CC}$ | POWER SUPPLY | PS | + 5 Volts |
| 40 | $V_{DD}$ | POWER SUPPLY | PS | + 12 Volts |
| 20 | $V_{SS}$ | GROUND | GND | Ground |
| 23 | $\overline{MR}$ | $\overline{MASTER\ RESET}$ | I | The Control and Status Registers and other controls are cleared when this input is low. |
| 8-15 | $\overline{DAL0}$-$\overline{DAL7}$ | $\overline{DATA\ ACCESS\ LINES}$ | I/O | Eight-bit bi-directional bus used for transfer of data, control status, and address information. |
| 17 | $\overline{ID7}$ | $\overline{SELECT\ CODE}$ | I | Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts. |
| 22 | $\overline{ID6}$ | | I | |
| 24 | $\overline{ID5}$ | | I | |
| 25 | $\overline{ID4}$ | | I | |
| 26 | $\overline{ID3}$ | | I | |
| 3 | $\overline{CS}$ | $\overline{CHIP\ SELECT}$ | I | The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations. |
| 39 | $\overline{RE}$ | $\overline{READ\ ENABLE}$ | I | This input, when low, gates the contents of the addressed register from a selected ASTRO onto the DAL bus. |
| 4 | $\overline{WE}$ | $\overline{WRITE\ ENABLE}$ | I | This input, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO. |
| 7 | $\overline{INTR}$ | $\overline{INTERRUPT}$ | O | This open drain output, to facilitate WIRE-ORing, goes low when any interrupt conditions occur. |
| 2 | $\overline{IACKI}$ | $\overline{INTERRUPT\ ACKNOWLEDGE\ IN}$ | I | When the Controller (determining the interrupting ASTRO) makes this input low, the ASTRO places its ID code on the DAL bus and sets reply low if it is interrupting, otherwise it makes $\overline{IACKO}$ a low. |
| 5 | $\overline{IACKO}$ | $\overline{INTERRUPT\ ACKNOWLEDGE\ OUT}$ | O | This output goes low in response to a low $\overline{IACKI}$ if the ASTRO is not the interrupting device. |
| 6 | $\overline{RPLY}$ | $\overline{REPLY}$ | O | This open drain output, to facilitate WIRE-ORing, goes low when the ASTRO is responding to being selected by an address on the DAL bus or in affirming that it is the interrupting source. |

## Description of Pin Functions

| Pin No. | Symbol | Pin Name | I/O | Function |
|---|---|---|---|---|
| 30<br>31<br>32<br>33 | R1<br>R2<br>R3<br>R4 | CLOCK RATES | I<br>I<br>I<br>I | These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by bits 0-2 of Control Register 2. |
| 37 | BA | TRANSMITTED DATA | O | This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled. |
| 27 | BB | RECEIVED DATA | I | This input receives serial data into the ASTRO. |
| 38 | $\overline{CA}$ | $\overline{\text{REQUEST TO SEND}}$ | O | This output is enabled by bit 1 of Control Register 1 and remains in a low state during transmitted data from the ASTRO. |
| 36 | $\overline{CB}$ | $\overline{\text{CLEAR TO SEND}}$ | I | This input, when low, enables the transmitter section of the ASTRO. |
| 28 | $\overline{CC}$ | $\overline{\text{DATA SET READY}}$ | I | This input generates an interrupt when going ON or OFF while the Data Terminal Ready signal is ON. It appears as bit 6 in the Status Register. |
| 16 | $\overline{CD}$ | $\overline{\text{DATA TERMINAL READY}}$ | O | This output is generated by bit 0 in Control Register 1 and indicates Controller readiness. |
| 18 | $\overline{CE}$ | $\overline{\text{RING INDICATOR}}$ | I | This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the OFF condition. |
| 29 | $\overline{CF}$ | $\overline{\text{CARRIER DETECTOR}}$ | I | This input from the Data Set generates an interrupt when going ON or OFF if Data Terminal Ready is ON. It appears as bit 5 in the Status Register. |
| 35 | $\overline{DB}$ | $\overline{\text{TRANSMITTER TIMING}}$ | I | This input is the Transmitter 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The transmitted data changes on the negative transition of this signal. |
| 34 | $\overline{DD}$ | $\overline{\text{RECEIVER TIMING}}$ | I | This input is the Receiver 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The Received Data is sampled by the ASTRO on the positive transition of this signal. |
| 19 | $\overline{MISC}$ | $\overline{\text{MISCELLANEOUS}}$ | O | This output is controlled by bits 4 and 5 of Control Register 1 and is used as an extra programmable signal. |

## Device Programming

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip.

## Control Register 1

| BIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SYNC/ASYNC<br>0 – LOOP MODE<br>1 – NORMAL MODE | ASYNC<br>0 – NONBREAK MODE<br>1 – BREAK MODE TX<br>SYNC<br>0 – TRANSMITTER NON TRANSPARENT MODE<br>1 – TRANSMITTER TRANSPARENT MODE | ASYNC (TRANS. ENABLED)<br>0 – 1½ or 2 STOP BIT SELECTION<br>1 – SINGLE STOP BIT SELECTION<br>ASYNC (TRANS. DISABLED)<br>0 – $\overline{\text{MISC}}$ OUT = 1<br>1 – $\overline{\text{MISC}}$ OUT = 0<br>SYNC (CR16 = 0)<br>0 – NO PARITY GENERATED<br>1 – TRANSMIT PARITY ENABLED<br>SYNC (CR16 = 1)<br>0 – NO FORCE DLE<br>1 – FORCE DLE | ASYNC<br>0 – NON ECHO MODE<br>1 – AUTO ECHO MODE<br>SYNC (CR12 = 1)<br>0 – DLE STRIPPING NOT ENABLED<br>1 – DLE STRIPPING ENABLED<br>SYNC (CR12 = 0)<br>0 – $\overline{\text{MISC}}$ OUT = 1<br>1 – $\overline{\text{MISC}}$ OUT = 0 | ASYNC<br>0 – NO PARITY ENABLED<br>1 – PARITY CHECK ENABLED ON RECEIVER AND PARITY GENERATION ENABLED ON TRANSMITTER<br>SYNC<br>0 – RECEIVER PARITY CHECK IS DISABLED<br>1 – RECEIVER PARITY CHECK IS ENABLED | SYNC/ASYNC<br>0 – RECEIVER DISABLED<br>1 – RECEIVER ENABLED | SYNC/ASYNC<br>0 – SETS $\overline{\text{RTS}}$ OUT = 1<br>1 – SETS $\overline{\text{RTS}}$ OUT = 0 | SYNC/ASYNC<br>0 – SETS $\overline{\text{DTR}}$ OUT = 1<br>1 – SETS $\overline{\text{DTR}}$ OUT = 0 |

### Bit 0

Controls the Data Terminal Ready output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

### Bit 1

Controls the Request to Send output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic Clear to Send input enables the Transmitter and allows TBMT interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request to Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request to Send output may be used for other functions such as Make Busy on 103 Data Sets.

### Bit 2

A logic 1 enables the ASTRO to receive data into the Receiver Buffer, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

### Bit 3

**Asynchronous Mode**

A logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

**Synchronous Mode**

A logic 1 bit enables check of parity on received characters only. Note: Transmitter parity enable is controlled by CR15.

**Bit 4**

**Asynchronous Mode**

A logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmitter Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

**Synchronous Mode**

A logic 1, with the Receiver enabled does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Buffer; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver, a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

**Bit 5**

**Asynchronous Mode**

A logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes transmission of 2 stop bits for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

**Synchronous Mode**

A logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR16=1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Buffer as part of the Transmitter Transparent mode.

**Bit 6**

**Asynchronous Mode**

A logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Buffer.

**Synchronous Mode**

A logic 1 conditions the Transmitter to a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE character can be forced ahead of any character in the Transmitter Buffer (Bit 5 above). When forcing DLE transmission, Bit 5 should be set to a logic 1 prior to loading the Transmitter Buffer, otherwise the character in the latter register may be transferred to the Transmitter Register prior to sending the DLE character.

**Bit 7**

A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the BA pin held in a Mark condition and the input to the BB pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the $\overline{\text{Data Set Ready}}$ ($\overline{\text{DSR}}$) input, with the $\overline{\text{Data Terminal Ready}}$ ($\overline{\text{DSR}}$) output pin held in an OFF condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) and $\overline{\text{Carrier Detector}}$ ($\overline{\text{CF}}$) inputs, with the $\overline{\text{Request To Send}}$ ($\overline{\text{RTS}}$) output pin held in an OFF condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

e. The $\overline{\text{Miscellaneous}}$ pin is held in an OFF (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

## Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

| BIT 7 6 | 5 | 4 | 3 | 2 1 0 |
|---|---|---|---|---|
| SYNC/ASYNC<br>CHARACTER LENGTH SELECT<br>00 = 8 BITS<br>01 = 7 BITS<br>10 = 6 BITS<br>11 = 5 BITS | MODE SELECT<br>0 – ASYNCHRONOUS MODE<br>1 – SYNCHRONOUS MODE | SYNC/ASYNC<br>0 – EVEN PARITY SELECT<br>1 – ODD PARITY SELECT | ASYNC<br>0 – RECEIVER CLK = RATE 1<br>1 – RECEIVER CLOCK DETERMINED BY BITS 2-0<br>SYNC (CR16 = 0)<br>0 – NO SYN STRIP<br>1 – SYN STRIP<br>SYNC (CR16 = 1)<br>0 – NO DLE-SYN STRIP<br>1 – DLE-SYN STRIP | SYNC/ASYNC<br>CLOCK SELECT<br>000 – 1X CLOCK<br>001 – RATE 1 CLOCK<br>010 – RATE 2 CLOCK<br>011 – RATE 3 CLOCK<br>100 – RATE 4 CLOCK<br>101 – RATE 4 CLOCK ÷ 2<br>110 – RATE 4 CLOCK ÷ 4<br>111 – RATE 4 CLOCK ÷ 8 |

**Bits 0-2**
These bits select the Transmit and Receive clocks.

| Bits | Clock Source | |
|---|---|---|
| 2 1 0 | Tx | Rx |
| 0 0 0 | 1X Clock (Pin 35) | 1X Clock (Pin 34) |
| 0 0 1 | Rate 1 32X clock (Pin 30) | |
| 0 1 0 | Rate 2 32X clock (Pin 31) * | |
| 0 1 1 | Rate 3 32X clock (Pin 32) * | |
| 1 0 0 | Rate 4 32X clock (Pin 33) * | |
| 1 0 1 | Rate 4 32X clock (Pin 33) (÷ 2) *† | |
| 1 1 0 | Rate 4 32X clock (Pin 33) (÷ 4) *† | |
| 1 1 1 | Rate 4 32X clock (Pin 33) (÷ 8) *† | |

**NOTES:**
*Rx clock is modified by bit 3 in the asynchronous mode.
†Rate 4 is internally dividable so that the required 32X clock may be derived from an applied 64X, 128X, or 256X clock which may be available.

**Bits 3**

**Asynchronous Mode**

A logic 0 selects the Rate 1 32X clock input (Pin 30) as the Receiver clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

**Synchronous Mode**

A logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip (CR14) is a logic 1, or all SYN characters in the Non-transparent mode to be stripped out and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as is transferred to the Receiver Buffer.

**Bit 4**
A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

**Bit 5**
A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

**Bits 6-7**
These bits select the full character length (including parity, if selected) as shown above. When parity is enabled it must be considered as a bit when making character length selection (5 bits plus parity = 6 bits).

## Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| • Data Set Change | • Data Set Ready (DSR) | • Carrier Detector | • Framing Error<br>• Syn Detect | • DLE Detect<br>• Parity Error | • Overrun Error | • Data Received (DR) | • Transmitter Buffer Empty (TBMT) |



**Bit 0**
A logic 1 indicates that the Transmitter Buffer may be loaded with new data. It is set to a logic 1 when the contents of the Transmitter Buffer is transferred to the Transmitter Register. It is cleared when the Transmitter Buffer is loaded from the DAL bus, or when the Transmitter is disabled.

**Bit 1**
A logic 1 indicates that an entire character has been received and transferred into the Receiver Buffer. It is cleared when the Receiver Buffer is read onto the DAL bus, or the Receiver is disabled.

**Bit 2**
A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Buffer has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Buffer. This bit is cleared when no Overrun condition is detected (the next character transfer time) or when the Receiver is disabled.

**Bit 3**
When the DLE Strip is enabled (CR14) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (CR13) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in both modes when the Receiver is disabled.

**Bit 4**

**Asynchronous Mode**

A logic 1 indicates that the received data did not have a valid stop bit, while the Receiver was enabled, which indicates a Framing error. This bit is set to a logic 0 if the stop bit (logic 1) was detected.

**Synchronous Mode**

A logic 1 indicates that the contents of the Receiver Register matches the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character.

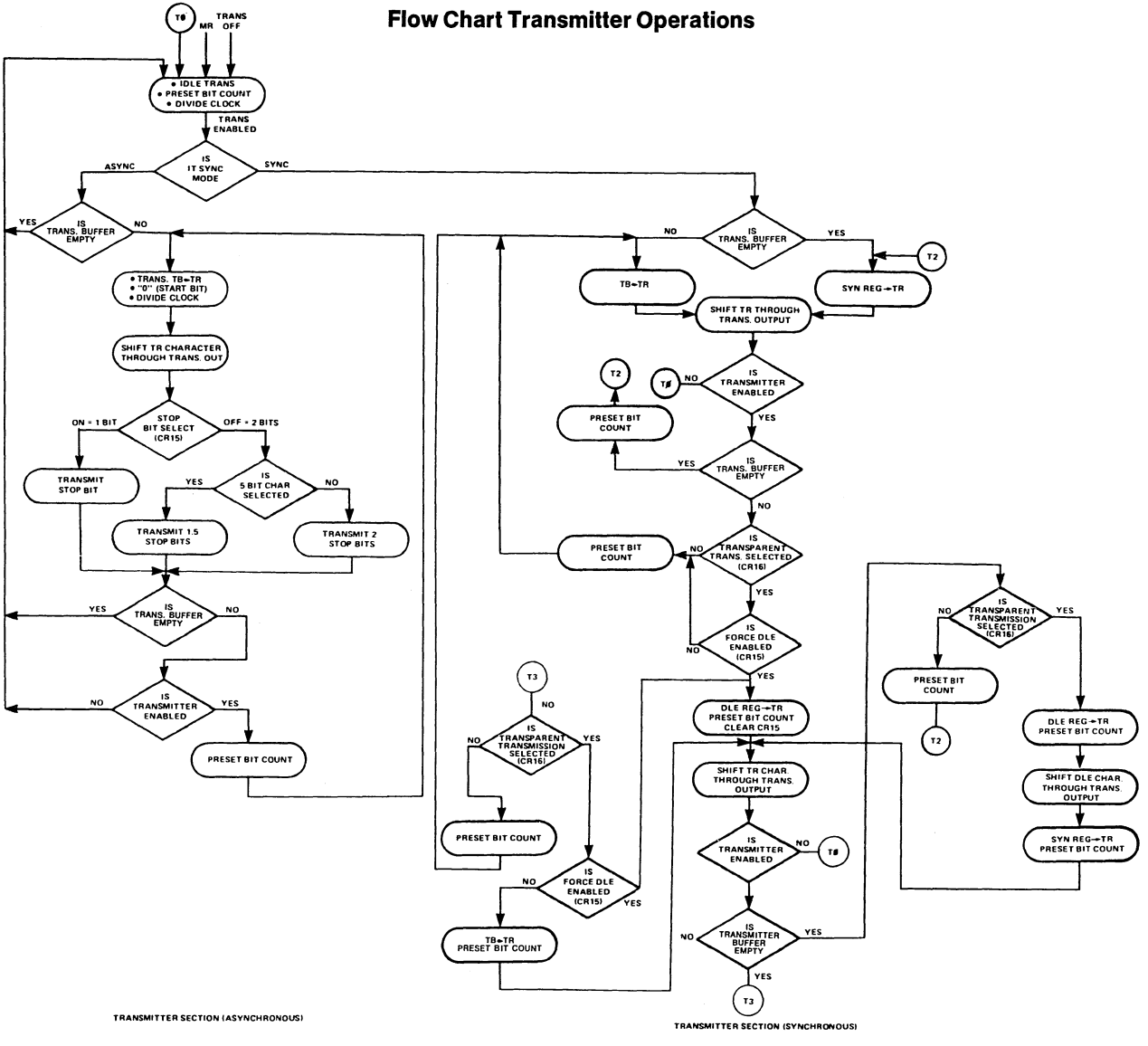
In both modes the bit is cleared when the Receiver is disabled.

**Bit 5**
This bit is the logic complement of the $\overline{\text{Carrier Detector}}$ input on Pin 29.

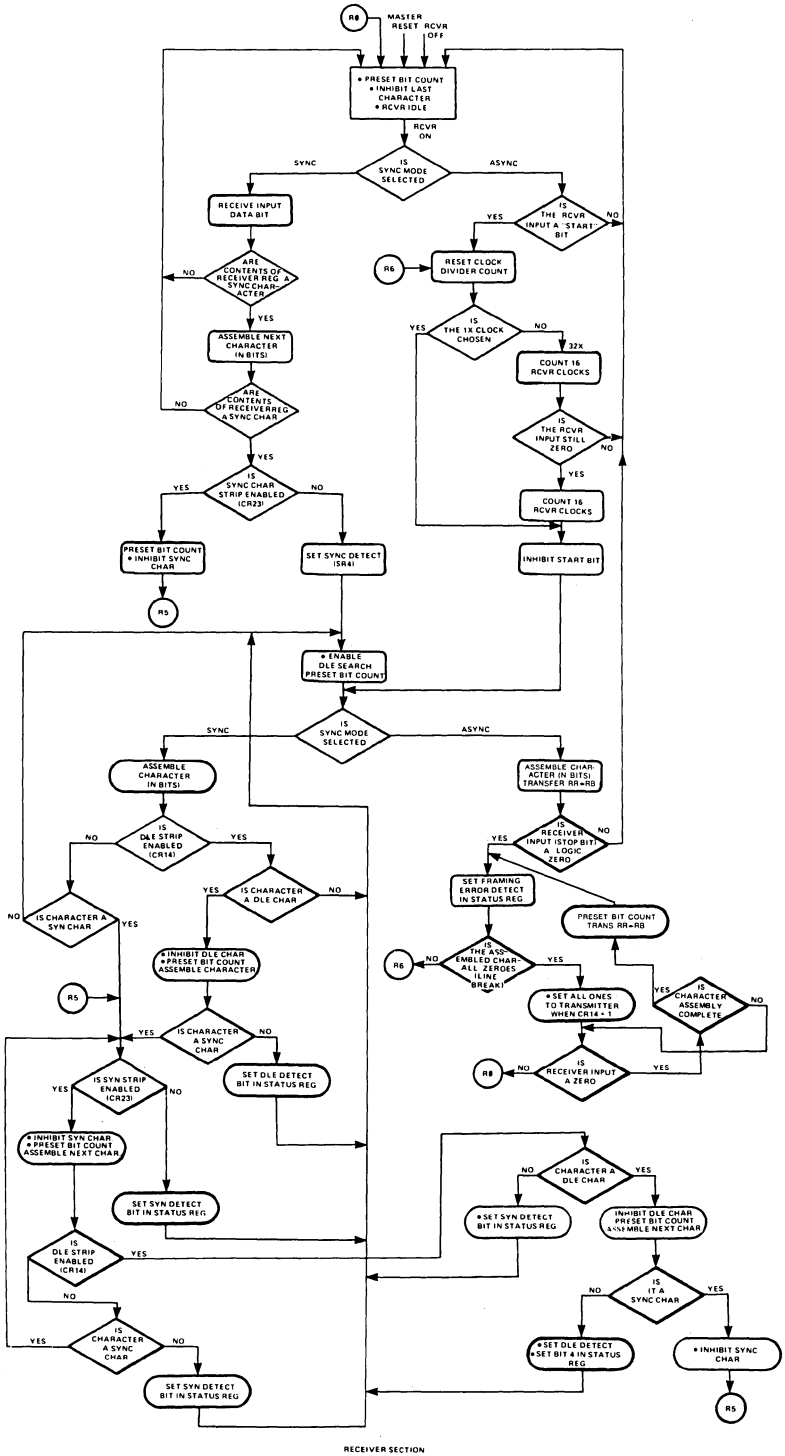
**Bit 6**
This bit is the logic complement of the $\overline{\text{Data Set Ready}}$ input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

**Bit 7**
This bit is set to a logic 1 whenever there is a change in state of the $\overline{\text{Data Set Ready}}$ or $\overline{\text{Carrier Detector}}$ inputs while Data Terminal Ready (CR10) is a logic 1 or the $\overline{\text{Ring Indicator}}$ is turned ON, with DTR a logic 0. This bit is cleared when the Status Register is read onto the DAL bus.

# Flow Chart Transmitter Operations

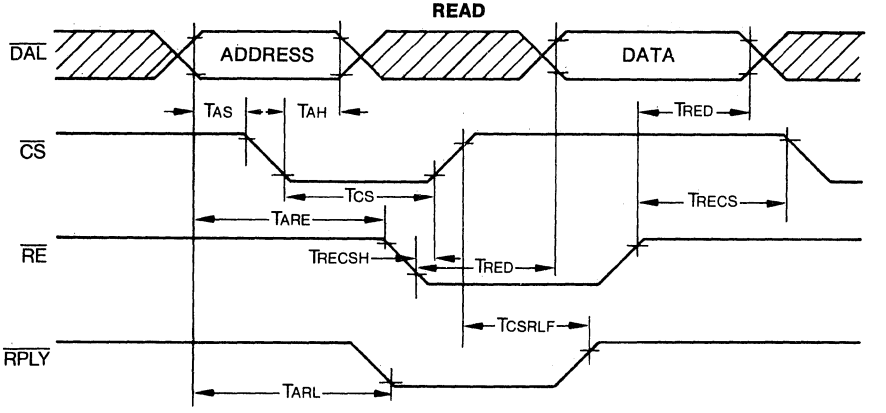


# Flow Chart Receiver Operations

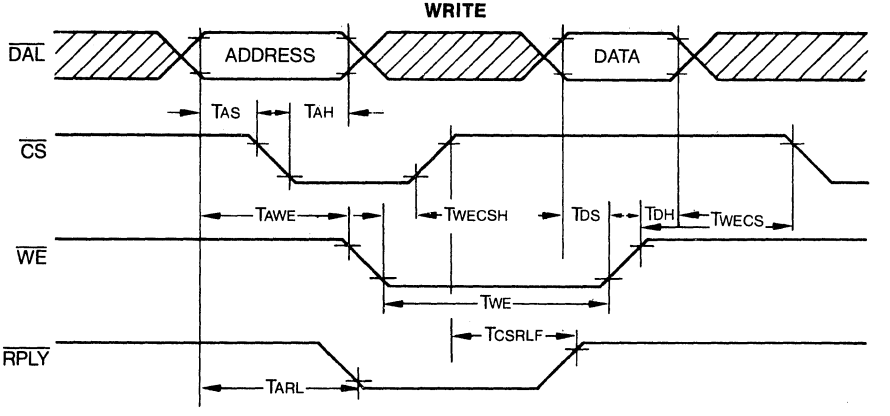



RECEIVER SECTION

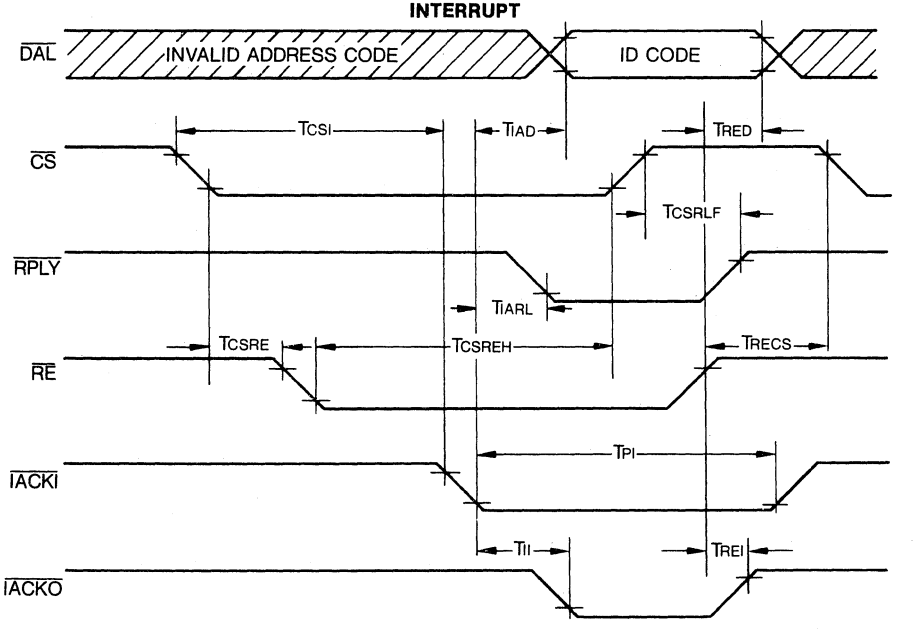
**READ**




**WRITE**




**INTERRUPT**



**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

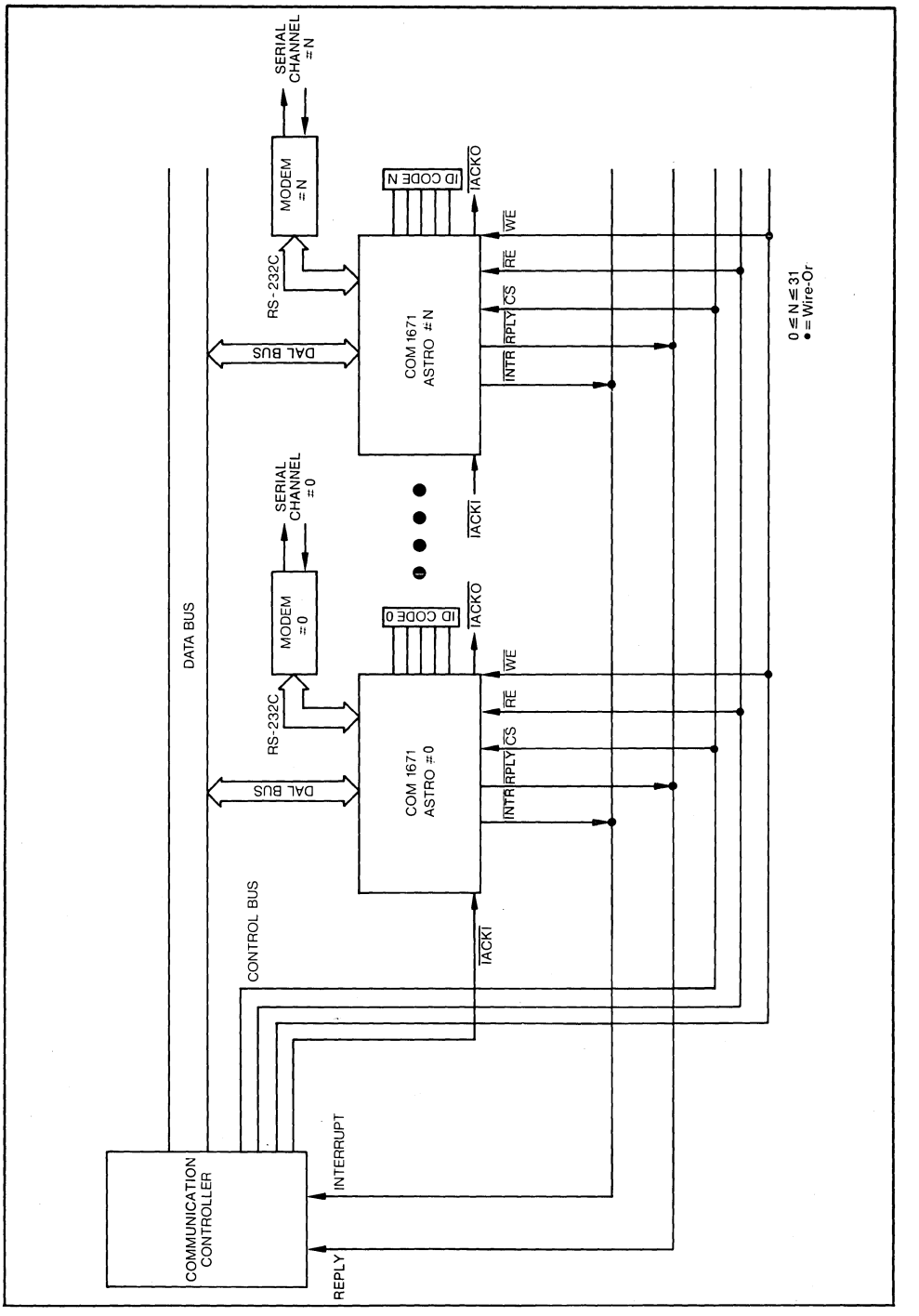
**ELECTRICAL CHARACTERISTICS**

($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%, $V_{DD}$ = +12V ±5%, $V_{BB}$ = −5V ±5%, $V_{SS}$ = 0V, unless otherwise noted)

| Parameter | | Min | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|---|
| **D.C. Characteristics** | | | | | | |
| INPUT VOLTAGE LEVELS | | | | | | |
| Low Level, $V_{IL}$ | | | | 0.8 | V | |
| High Level, $V_{IH}$ | | 2.4 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | | |
| Low Level, $V_{OL}$ | | | 0.4 | | V | $I_{OL}$ = 1.6ma |
| High Level, $V_{OH}$ | | 2.4 | | | | $I_{OH}$ = 100 μa |
| INPUT LEAKAGE | | | | | | |
| Data Bus | | | 5.0 | 10.0 | μa | 0 ≤ $V_{IN}$ ≤ 5 v |
| All others | | | 5.0 | 10.0 | μa | $V_{IN}$ = +12v |
| POWER SUPPLY CURRENT | | | | | | |
| $I_{CC}$ | | | | 80.0 | ma | |
| $I_{DD}$ | | | | 10.0 | ma | |
| $I_{BB}$ | | | | 1.0 | ma | |
| **A.C. Characteristics** | | | | | | $T_A$ = 25°C |
| CLOCK-RCP, TCP | | | | | | |
| frequency | | | 1.0 | | MHz | |
| **DAL Bus** | | | | | | |
| $T_{AS}$ | Address Set-Up Time | 0 | | | ns | |
| $T_{AH}$ | Address Hold Time | 150 | | | ns | |
| $T_{ARL}$ | Address to $\overline{RPLY}$ Delay | | | 400 | ns | |
| $T_{CS}$ | $\overline{CS}$ Width | 250 | | | ns | |
| $T_{CSRLF}$ | $\overline{CS}$ to Reply OFF Relay | 0 | | 250 | ns | $R_L$ = 2.7 KΩ |
| **Read** | | | | | | |
| $T_{ARE}$ | Address and $\overline{RE}$ Spacing | 250 | | | ns | |
| $T_{RECSH}$ | $\overline{RE}$ and $\overline{CS}$ Overlap | 20 | | | ns | |
| $T_{RECS}$ | $\overline{RE}$ to $\overline{CS}$ Spacing | 250 | | | ns | |
| $T_{RED}$ | $\overline{RE}$ to Data Out Delay | | | 180 | ns | $C_L$ = 20 pf |
| **Write** | | | | | | |
| $T_{AWE}$ | Address to $\overline{WE}$ Spacing | 250 | | | ns | |
| $T_{WECSH}$ | $\overline{WE}$ and $\overline{CS}$ Overlap | 20 | | | ns | |
| $T_{WE}$ | $\overline{WE}$ Width | 200 | | 1000 | ns | |
| $T_{DS}$ | Data Set-Up Time | 150 | | | ns | |
| $T_{DH}$ | Data Hold Time | 100 | | | ns | |
| $T_{WECS}$ | $\overline{WE}$ to $\overline{CS}$ Spacing | 250 | | | ns | |
| **Interrupt** | | | | | | |
| $T_{CSI}$ | $\overline{CS}$ to $\overline{IACKI}$ Delay | 0 | | | ns | |
| $T_{CSRE}$ | $\overline{CS}$ to $\overline{RE}$ Delay | 250 | | | ns | |
| $T_{CSREH}$ | $\overline{CS}$ and $\overline{RE}$ Overlap | 20 | | | ns | |
| $T_{RECS}$ | $\overline{RE}$ to $\overline{CS}$ Spacing | 250 | | | ns | |
| $T_{PI}$ | $\overline{IACKI}$ Pulse Width | 200 | | | ns | |
| $T_{IAD}$ | $\overline{IACKI}$ to Valid ID Code Delay | | | 250 | ns | See Note 1. |
| $T_{RED}$ | $\overline{RE}$ OFF to $\overline{DAL}$ Open Delay | | | 180 | ns | |
| $T_{IARL}$ | $\overline{IACKI}$ to $\overline{RPLY}$ Delay | | | 250 | ns | See Note 1. |
| $T_{CSRLF}$ | $\overline{CS}$ to $\overline{RPLY}$ OFF Delay | 0 | | 250 | ns | $R_L$ = 2.7 KΩ |
| $T_{II}$ | $\overline{IACKI}$ to $\overline{IACKO}$ Delay | | | 200 | ns | |
| $T_{REI}$ | $\overline{RE}$ OFF to $\overline{IACKO}$ OFF Delay | | | 250 | ns | |

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

## Multiple ASTRO System in Daisy-Chain Configuration




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights.of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

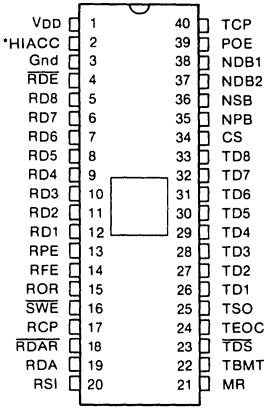
# Universal Asynchronous Receiver/Transmitter UART



## FEATURES

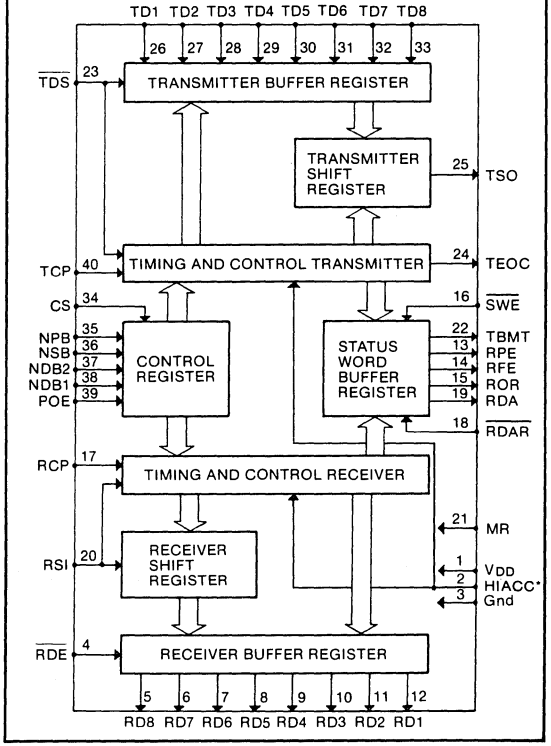
- ☐ Compatible with TR1863 timing
- ☐ High accuracy 32X clock mode: 48.4375% Receiver Distortion Immunity and improved RDA/ROR operation (COM 8018 only)
- ☐ High Speed Operation—62.5K baud, 200ns strobes
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Input pull-up options: COM 8018 has low current pull-up resistors; COM 1863 has no pull up resistors
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Improved Start Bit Verification—decreases error rate
- ☐ 46.875% Receiver Distortion Immunity
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ Master Reset—Resets all status outputs and Receiver Buffer Register
- ☐ Three State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic DIP Package—easy board insertion
- ☐ Baud Rates available from SMC's COM 8046, COM 8116, COM 8126, COM 8136, COM 8146 baud rate generators

## PIN CONFIGURATION




PACKAGE: 40-Pin D.I.P.

## FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1 or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

*If pin 2 is taken to a logic 1 the COM 8018 will operate in a high accuracy mode. If pin 2 is connected to − 12V, GND, a valid logic zero, or left unconnected, the high accuracy feature is disabled, and the UART will operate in a 16X clock mode. Pin 2 is not connected on the COM 1863.

## DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied, and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

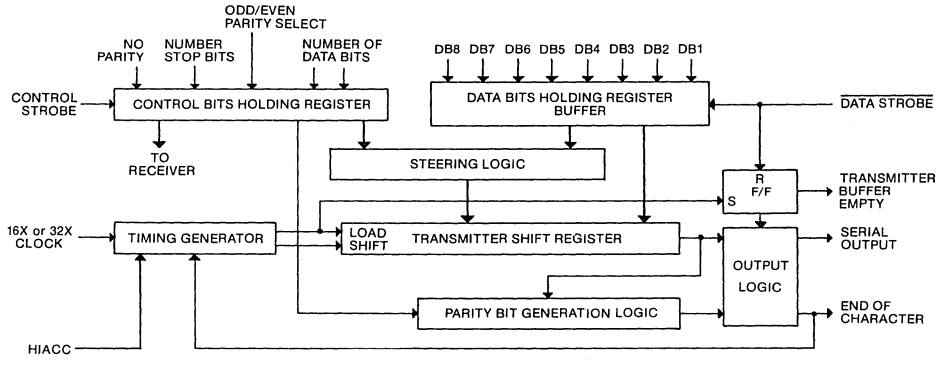
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the data strobe ($\overline{TDS}$) has been pulsed, the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the $\overline{TBMT}$ signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TEOC goes low, TSO goes low (the start bit), and TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

### TRANSMITTER BLOCK DIAGRAM




## DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions for mark (high) to space (low). If the RSI line remains spacing for 15/32 to 17/32 bit times (in the 16X mode, HIACC = 0) or 31/64 to 33/64 bit times (in the 32X mode, HIACC = 1), a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

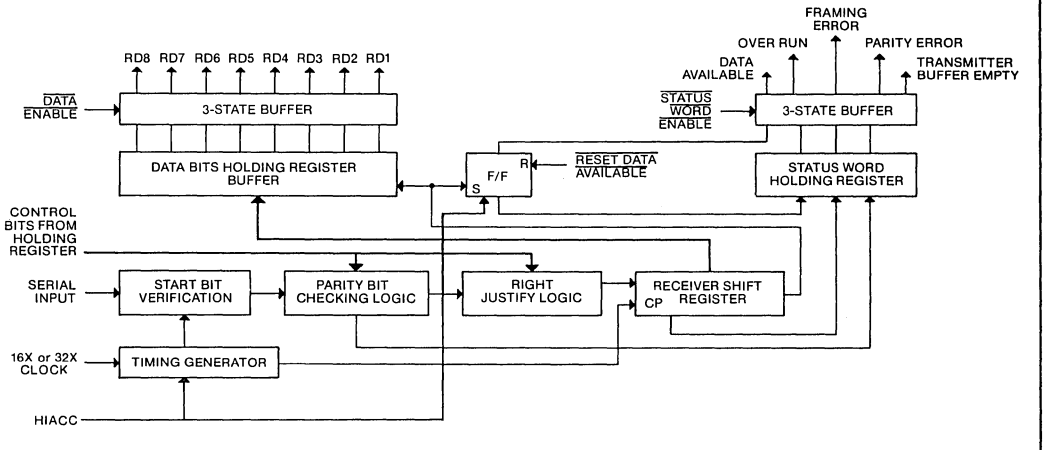
If the received parity bit is incorrect, the parity error flip-flop of the status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, the framing error flip-flop is set high, indicating a framing error.

On the negative RCP edge preceding the stop-bit center sample, internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high, or the $\overline{RDAR}$ signal is low, the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

Subsequently the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.



## RECEIVER BLOCK DIAGRAM




## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $V_{DD}$ | Power Supply | +5 volt Supply |
| 2 | HIACC | High Accuracy Mode | Enables 32X clock and improved RDA/ROR operation. See NOTE on high accuracy mode. |
| 3 | GND | Ground | Ground |
| 4 | $\overline{RDE}$ | Received Data Enable | A low-level input enables the outputs (RD8-RD1) of the receiver buffer register. |
| 5-12 | RD8-RD1 | Receiver Data Outputs | These are the eight 3-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output. |
| 13 | RPE | Receiver Parity Error | This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity. |
| 14 | RFE | Receiver Framing Error | This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit. |

## DESCRIPTION OF PIN FUNCTIONS

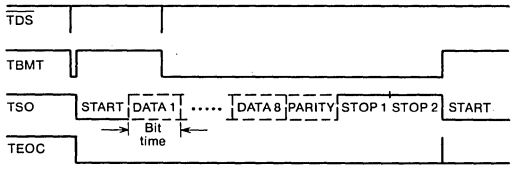
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 15 | ROR | Receiver Over Run | This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output reset not completed) before the present character is transferred into the receiver buffer register. |
| 16 | $\overline{SWE}$ | Status Word Enable | A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register. |
| 17 | RCP | Receiver Clock | This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired receiver baud rate. |
| 18 | $\overline{RDAR}$ | Receiver Data Available Reset | A low-level input resets the RDA output to a low-level. $\overline{RDAR}$ must have gone low and come high again before ROR is sampled to avoid overrun indication. |
| 19 | RDA | Receiver Data Available | This 3-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register. |
| 20 | RSI | Receiver Serial Input | This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception. |
| 21 | MR | Master Reset | This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE, ROR and RD1-RD8 to a low-level. |
| 22 | TBMT | Transmitter Buffer Empty | This 3-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data. |
| 23 | $\overline{TDS}$ | Transmitter Data Strobe | A low-level input strobe enters the data bits into the transmitter buffer register. |
| 24 | TEOC | Transmitter End of Character | This output appears as a high-level during the last half clock cycle of the last stop bit. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission. |
| 25 | TSO | Transmitter Serial Output | This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted. |
| 26-33 | TD1-TD8 | Transmitter Data Inputs | There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1. |
| 34 | CS | Control Strobe | A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level. |
| 35 | NPB | No Parity Bit | A high-level input eliminates the parity bit from being transmitted: the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE. |

## DESCRIPTION OF PIN FUNCTION

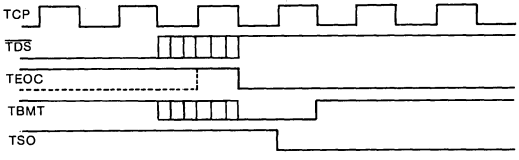
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 36 | NSB | Number of Stop Bits | This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of two stop bits when programming a 5 data bit word generates 1.5 stop bits. |
| 37-38 | NDB2, NDB1 | Number of Data Bits/Character | These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:<br>NDB2 NDB1 data bits/character<br>L L 5<br>L H 6<br>H L 7<br>H H 8 |
| 39 | POE | Odd/Even Parity Select | The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table:<br>NPB POE MODE<br>L L odd parity<br>L H even parity<br>H X no parity<br>X = don't care |
| 40 | TCP | Transmitter Clock | This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired transmitter baud rate. |



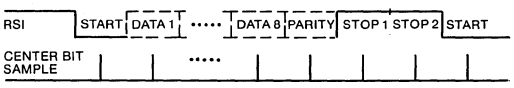
### TRANSMITTER TIMING— 8 BIT, PARITY, 2 STOP BITS



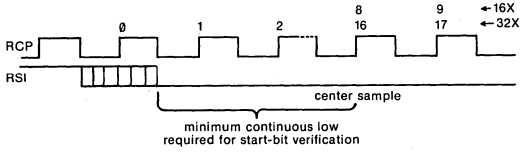

### TRANSMITTER START-UP



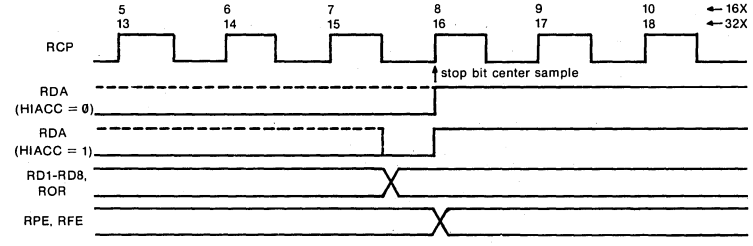

### RECEIVER TIMING— 8 BIT, PARITY, 2 STOP BITS




### START BIT DETECT AND VERIFY




### RECEIVER TIMING DETAIL



**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin (except Pin 2), with respect to ground ..... −0.3V
Negative Voltage on Pin 2, with respect to ground ..... −13.2V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A = 0°C$ to $70°C$, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 2.0 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL} = 1.6mA$ |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH} = -100\mu A$ |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | 300 | $\mu A$ | $V_{IN}$ = GND, COM 8018 only |
| INPUT LEAKAGE | | | ±10 | $\mu A$ | COM 1863 only |
| OUTPUT CURRENT | | | | | |
| Leakage, $I_{LO}$ | | | ±10 | $\mu A$ | $\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$ |
| Short circuit, Ios** | | | 40 | mA | $V_{OUT} = 0V$ |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pf | |
| OUTPUT CAPACITANCE | | | | | |
| All outputs, $C_{OUT}$ | | 10 | 20 | pf | $\overline{SWE} = \overline{RDE} = V_{IH}$ |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 25 | mA | All outputs = $V_{OH}$, All inputs = $V_{DD}$ |
| **A.C. CHARACTERISTICS** | | | | | $T_A = +25°C$, See Timing Diagrams |
| CLOCK FREQUENCY | DC | | 1.0 | MHz | RCP, TCP |
| PULSE WIDTH | | | | | |
| Clock | 0.45 | | | $\mu s$ | RCP, TCP |
| Master reset | 500 | | | ns | MR |
| Control strobe | 200 | | | ns | CS |
| Transmitter data strobe | 200 | | | ns | $\overline{TDS}$ |
| Receiver data available reset | 200 | | | ns | $\overline{RDAR}$ |
| INPUT SET-UP TIME | | | | | |
| Data bits | 0 | | | ns | TD1-TD8 |
| Control bits | 0 | | | ns | NPB, NSB, NDB2, NDB1, POE |
| INPUT HOLD TIME | | | | | |
| Data bits | 0 | | | ns | TD1-TD8 |
| Control bits | 0 | | | ns | NPB, NSB, NDB2, NDB1, POE |
| ENABLE TO OUTPUT DELAY | | | | | Load = 20pf +1 TTL input |
| Receive data enable | | | 250 | ns | $\overline{RDE}$: $T_{PD1}$, $T_{PD0}$ |
| Status word enable | | | 250 | ns | $\overline{SWE}$: $T_{PD1}$, $T_{PD0}$ |
| OUTPUT DISABLE DELAY | | | 250 | ns | $\overline{RDE}$, $\overline{SWE}$ |

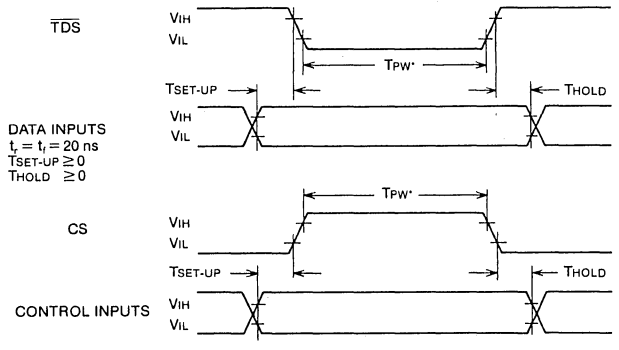
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within 1½ clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one RCP clock period, guaranteeing a maximum start bit slippage of ±1/32 or ±1/64 of a bit time.

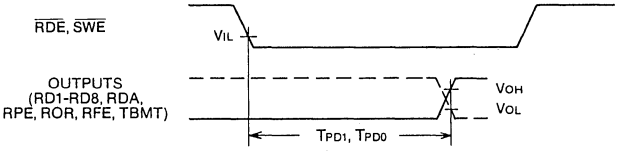
3. The 3-state output has 3 states: 1) low impedance to $V_{DD}$ 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

## DATA/CONTROL TIMING DIAGRAM



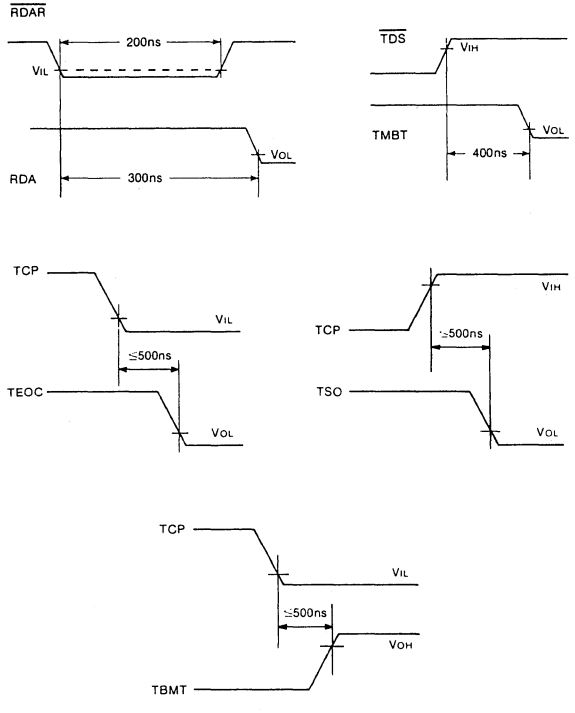

*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

## OUTPUT TIMING DIAGRAM




NOTE: Waveform drawings not to scale for clarity.

## ADDITIONAL TIMING INFORMATION




## NOTES ON COM 8018 AND COM 1863 HIGH-ACCURACY AND IMPROVED RDA/ROR MODE

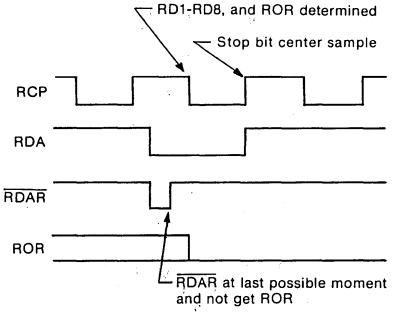
The HIACC mode is enabled by applying a logic "one" to pin 2. If this pin is left unconnected, or connected to GND, −12V, or a logic "zero," the HIACC mode is disabled. The HIACC input has an internal pull-down resistor.

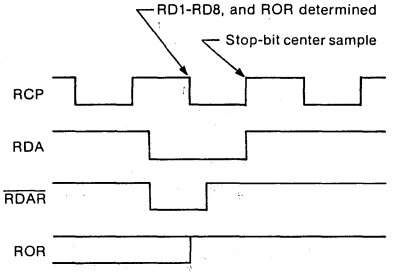
When the HIACC mode is selected, the TX and RX halves both operate on 32X instead of 16X clocks. Also, RDA is notched during the one half receiver clock cycle preceding the stop bit center sample when RD1-RD8 and ROR are changing.

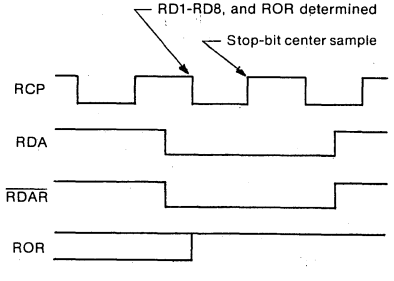
Whether or not the HIACC mode is selected, RDA must be low and RDAR must have returned high to avoid setting ROR. If RDAR is held low past the stop-bit center sample, RDA will go high after RDAR returns high.

The maximum current HIACC will supply if connected to −13.2V is 3.5mA.

## IMPROVED RDA/ROR OPERATION TIMING DIAGRAMS

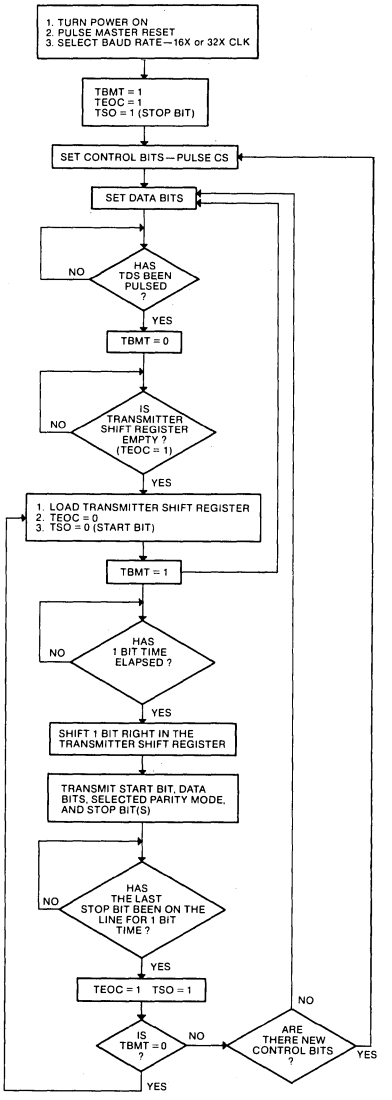


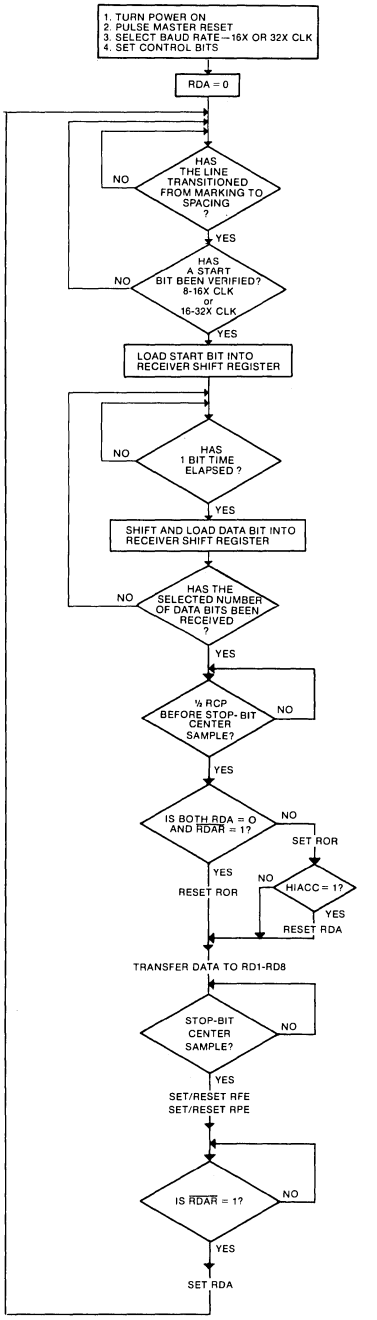




Protection against missing the ROR flag

## FLOW CHART—TRANSMITTER




## FLOW CHART—RECEIVER




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

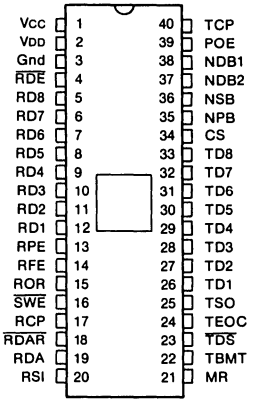
STANDARD MICROSYSTEMS CORPORATION

# COM2502
# COM2017

# Universal Asynchronous Receiver/Transmitter
# UART



**Pin Configuration**

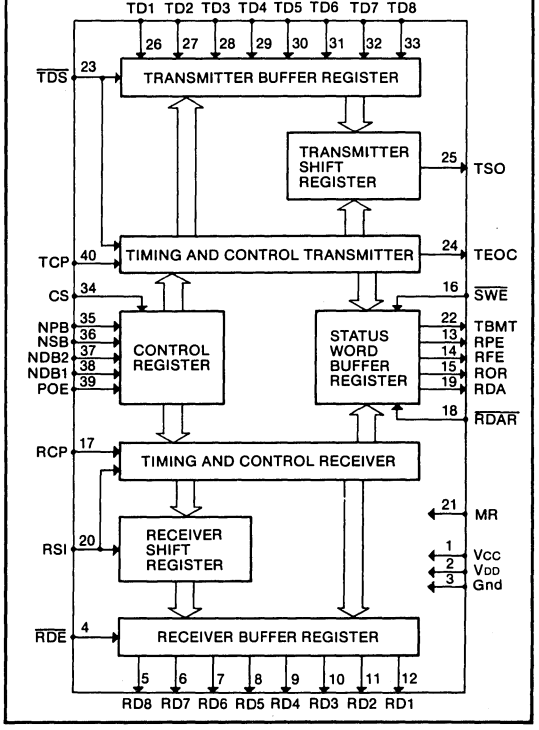



PACKAGE: 40-Pin D.I.P.

## FEATURES

- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Start Bit Verification—decreases error rate
- ☐ Fully Programmable—data word length, parity mode, number of stop bits; one, one and one-half, or two
- ☐ High Speed Operation—40K baud, 200ns strobes
- ☐ Master Reset—Resets all status outputs
- ☐ Tri-State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic Dip Package—easy board insertion

**Functional Block Diagram**




## GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolothic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code from the COM 2017.

The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

## DESCRIPTION OF OPERATION — TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

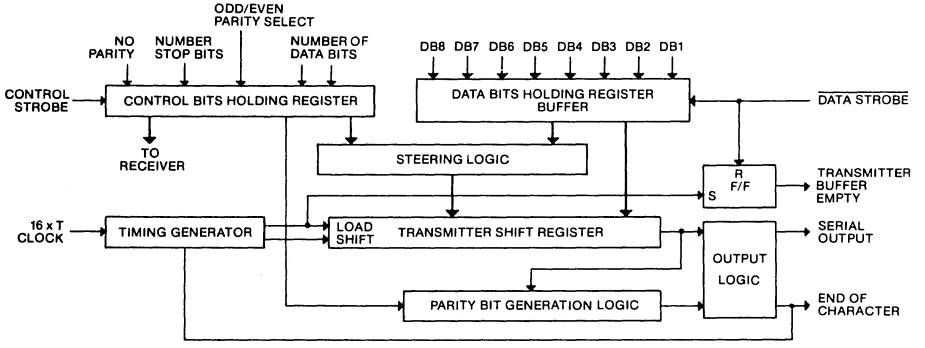
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

### TRANSMITTER BLOCK DIAGRAM




## DESCRIPTION OF OPERATION — RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

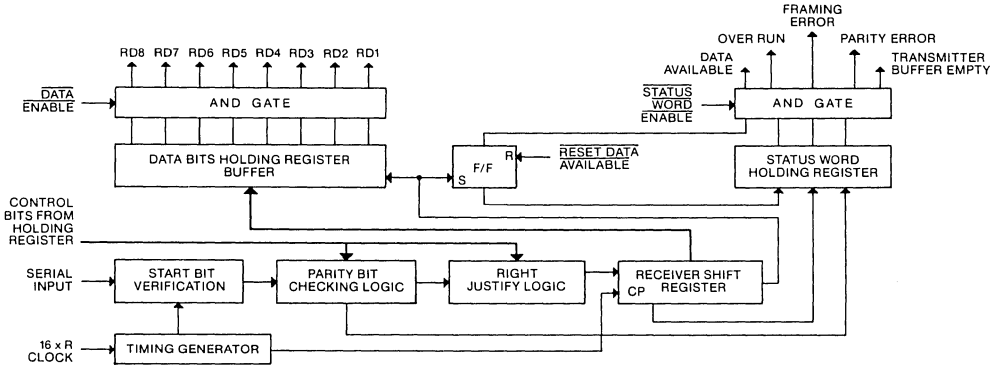
status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.



**RECEIVER BLOCK DIAGRAM**




**DESCRIPTION OF PIN FUNCTIONS**

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | +5 volt Supply |
| 2 | NC | No Connection | −12 volt Supply |
| 3 | GND | Ground | Ground |
| 4 | $\overline{RDE}$ | Received Data Enable | A low-level input enables the outputs (RD8-RD1) of the receiver buffer register. |
| 5-12 | RD8-RD1 | Receiver Data Outputs | These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output. |
| 13 | RPE | Receiver Parity Error | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity. |
| 14 | RFE | Receiver Framing Error | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit. |

## DESCRIPTION OF PIN FUNCTIONS

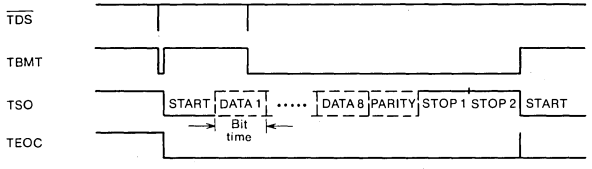
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 15 | ROR | Receiver Over Run | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register. |
| 16 | $\overline{SWE}$ | Status Word Enable | A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register. |
| 17 | RCP | Receiver Clock | This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate. |
| 18 | $\overline{RDAR}$ | Receiver Data Available Reset | A low-level input resets the RDA output to a low-level. |
| 19 | RDA | Receiver Data Available | This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register. |
| 20 | RSI | Receiver Serial Input | This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception. |
| 21 | MR | Master Reset | This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level. |
| 22 | TBMT | Transmitter Buffer Empty | This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data. |
| 23 | $\overline{TDS}$ | Transmitter Data Strobe | A low-level input strobe enters the data bits into the transmitter buffer register. |
| 24 | TEOC | Transmitter End of Character | This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission. |
| 25 | TSO | Transmitter Serial Output | This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted. |
| 26-33 | TD1-TD8 | Transmitter Data Inputs | There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1. |
| 34 | CS | Control Strobe | A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level. |
| 35 | NPB | No Parity Bit | A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE. |

## DESCRIPTION OF PIN FUNCTION

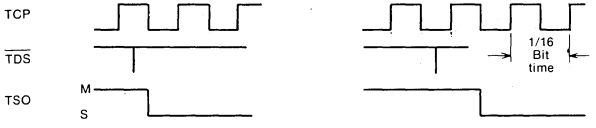
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 36 | NSB | Number of Stop Bits | This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 2017. |
| 37-38 | NDB2, NDB1 | Number of Data Bits/Character | These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:<br>NDB2 NDB1 data bits/character<br>L L 5<br>L H 6<br>H L 7<br>H H 8 |
| 39 | POE | Odd/Even Parity Select | The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table:<br>NPB POE MODE<br>L L odd parity<br>L H even parity<br>H X no parity<br>X = don't care |
| 40 | TCP | Transmitter Clock | This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate. |



### TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

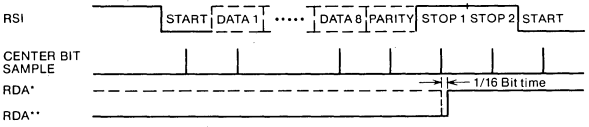



### TRANSMITTER START-UP



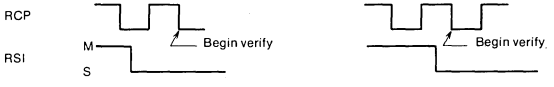

Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of TDS.

### RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS




*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

### START BIT DETECT/VERIFY




If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, $V_{CC}$ ..... +0.3V
Negative Voltage on any Pin, $V_{CC}$ ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

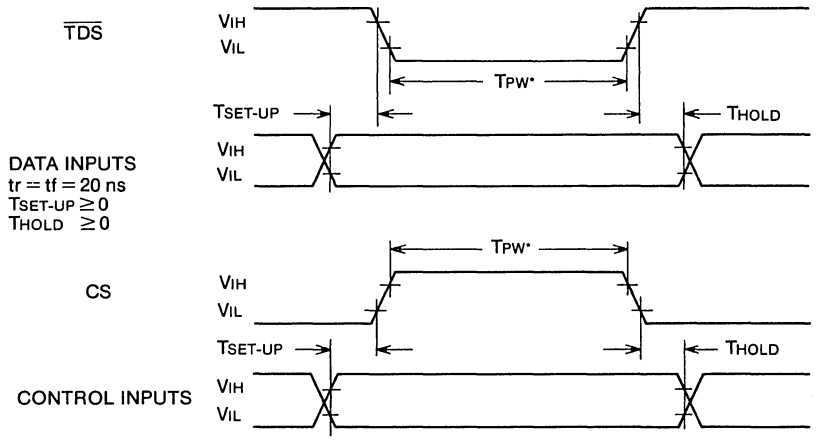
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0° C to 70° C $V_{CC}$ = +5V ±5%, $V_{DD}$ = −12V ±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | $V_{DD}$ | | 0.8 | V | |
| High-level, $V_{IH}$ | $V_{CC}$-1.5 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 1.6mA |
| High-level, $V_{OH}$ | 2.4 | 4.0 | | V | $I_{OH}$ = 100$\mu$A |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | 1.6 | mA | see note 4 |
| OUTPUT CURRENT | | | | | |
| Leakage, $I_{LO}$ | | | −1 | $\mu$A | $\overline{SWE}$ = $\overline{RDE}$ = $V_{IH}$, 0 ≤ $V_{OUT}$ ≤ +5V |
| Short circuit, $I_{OS}$** | | | 10 | mA | $V_{OUT}$ = 0V |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pf | $V_{IN}$ = $V_{CC}$, f = 1MHz |
| OUTPUT CAPACITANCE | | | | | |
| All outputs, $C_{OUT}$ | | 10 | 20 | pf | $\overline{SWE}$ = $\overline{RDE}$ = $V_{IH}$, f = 1MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 28 | mA | All outputs = $V_{OH}$, All inputs = $V_{CC}$ |
| $I_{DD}$ | | | 28 | mA | |
| **A.C. CHARACTERISTICS** | | | | | $T_A$ = +25° C |
| CLOCK FREQUENCY | | | | | |
| (COM2502, COM2017) | DC | | 400 | KHz | RCP, TCP |
| PULSE WIDTH | | | | | |
| Clock | 1 | | | $\mu$s | RCP, TCP |
| Master reset | 500 | | | ns | MR |
| Control strobe | 200 | | | ns | $\overline{CS}$ |
| Transmitter data strobe | 200 | | | ns | $\overline{TDS}$ |
| Receiver data available reset | 200 | | | ns | $\overline{RDAR}$ |
| INPUT SET-UP TIME | | | | | |
| Data bits | ≥0 | | | ns | TD1-TD8 |
| Control bits | ≥0 | | | ns | NPB, NSB, NDB2, NDB1, POE |
| INPUT HOLD TIME | | | | | |
| Data bits | ≥0 | | | ns | TD1-TD8 |
| Control bits | ≥0 | | | ns | NPB, NSB, NDB2, NDB1, POE |
| STROBE TO OUTPUT DELAY | | | | | Load = 20pf +1 TTL input |
| Receive data enable | | | 350 | ns | $\overline{RDE}$: $T_{PD1}$, $T_{PD0}$ |
| Status word enable | | | 350 | ns | $\overline{SWE}$: $T_{PD1}$, $T_{PD0}$ |
| OUTPUT DISABLE DELAY | | | 350 | ns | $\overline{RDE}$, $\overline{SWE}$ |

**Not more than one output should be shorted at a time.

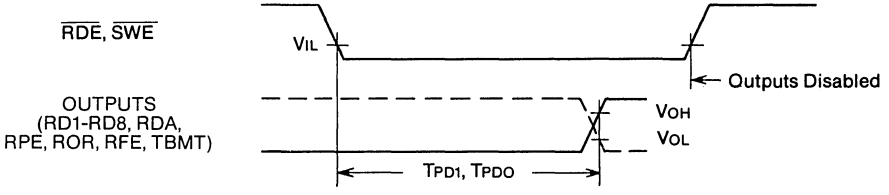
NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.
2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.
3. The tri-state output has 3 states: 1) low impedance to Vcc 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms. The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.
4. Under steady state conditions no current flows for TTL or MOS interfacing. (COM 2502)

## DATA/CONTROL TIMING DIAGRAM

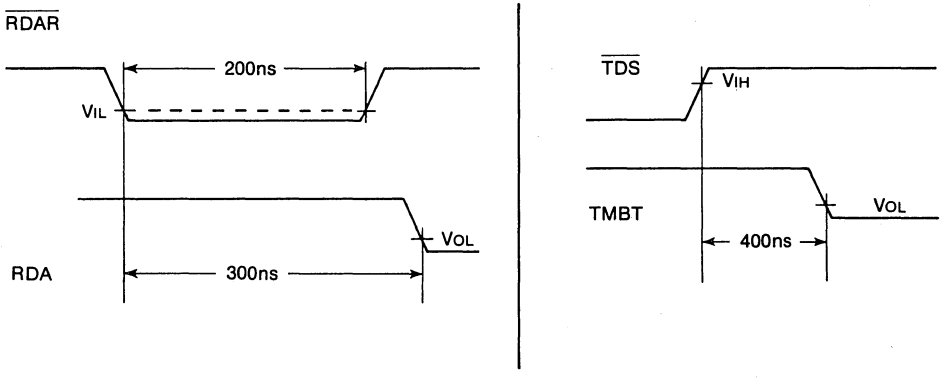



*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

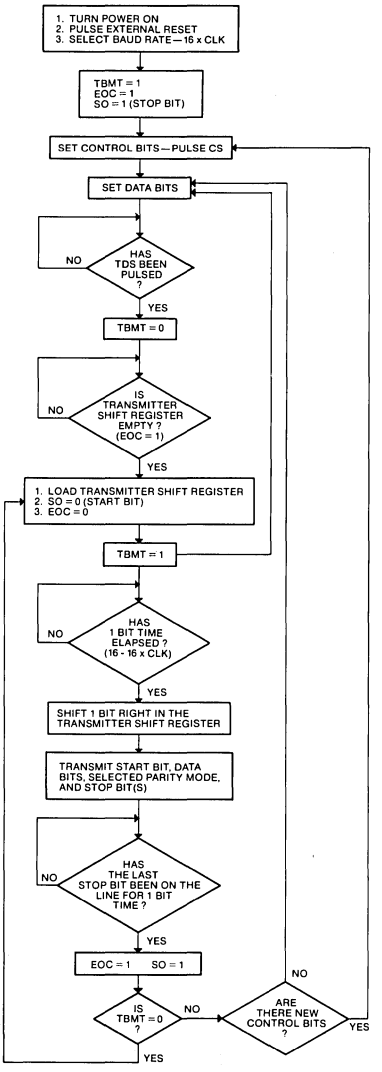
## OUTPUT TIMING DIAGRAM



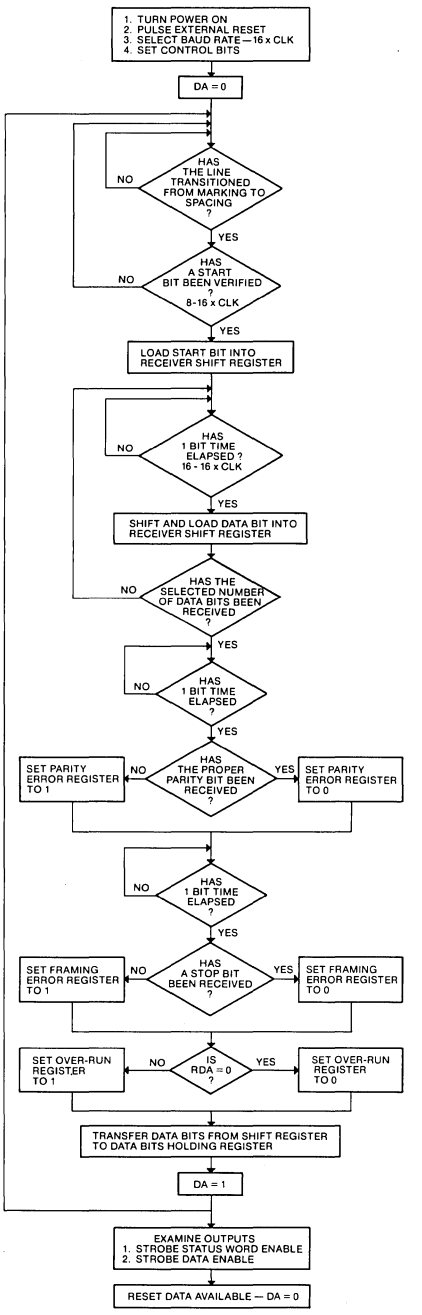

NOTE: Waveform drawings not to scale for clarity.



## FLOW CHART—TRANSMITTER




## FLOW CHART—RECEIVER





STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898



Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM2601

# Universal Synchronous Receiver/Transmitter USRT



## FEATURES

- ☐ STR, BSC — Bi-sync and interleaved bi-sync modes of operation
- ☐ Fully Programmable — data word length, parity mode, receiver sync character, transmitter sync character
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Directly TTL Compatible — no interface components required
- ☐ Tri-State Data Outputs — bus structure oriented
- ☐ IBM Compatible — internally generated SCR and SCT signals
- ☐ High Speed Operation — 250K baud, 200ns strobes
- ☐ Low Power — 300mW
- ☐ Input Protected — eliminates handling problems
- ☐ Dip Package — easy board insertion

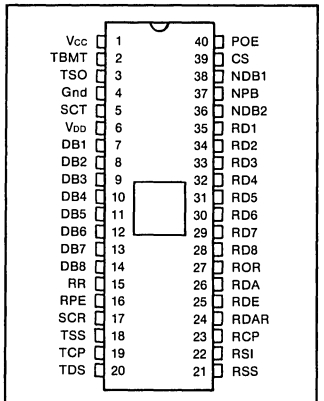
## APPLICATIONS

- ☐ Bi-Sync Communications
- ☐ Cassette I/O
- ☐ Floppy Disk I/O

## GENERAL DESCRIPTION

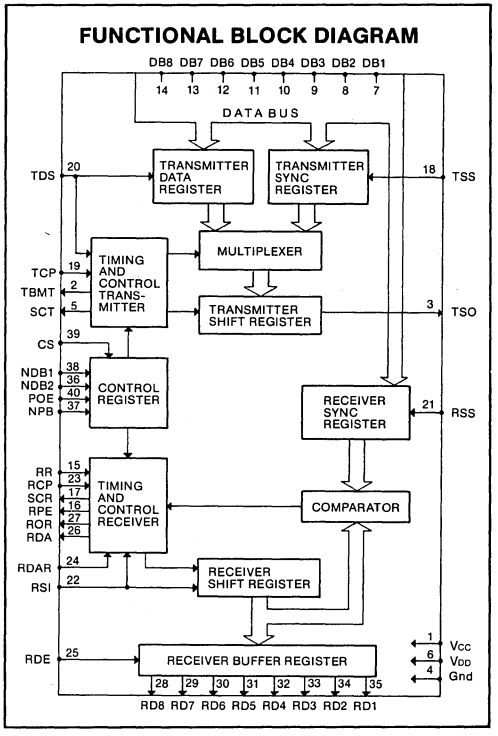
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

## PIN CONFIGURATION




PACKAGE: 40-Pin D.I.P.

## FUNCTIONAL BLOCK DIAGRAM



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $V_{CC}$ | Power Supply | +5 volt Supply |
| 2 | TBMT | Transmitter Buffer Empty | This output is at a high-level when the transmitter data buffer register may be loaded with new data. |
| 3 | TSO | Transmitter Serial Output | This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register. |
| 4 | GND | Ground | Ground |
| 5 | SCT | Sync Character Transmitted | This output is set high when the character loaded into the transmitter shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed. |
| 6 | $V_{DD}$ | Power Supply | −12 volt Supply |
| 7-14 | DB1-DB8 | Data Bus Inputs | This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs may be in either logic state. The LSB should always be placed on DB1. |
| 15 | RR | Receiver Reset | This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. |
| 16 | RPE | Receiver Parity Error | This output is a high-level if the received character parity bit does not agree with the selected parity. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 17 | SCR | Sync Character Received | This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character. |
| 18 | TSS | Transmitter Sync Strobe | A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register. |
| 19 | TCP | Transmitter Clock | The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency. |
| 20 | TDS | Transmitter Data Buffer Strobe | A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register. |
| 21 | RSS | Receiver Sync Strobe | A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register. |
| 22 | RSI | Receiver Serial Input | This input accepts the serial bit input stream. |
| 23 | RCP | Receiver Clock | The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency. |
| 24 | RDAR | Receiver Data Available Reset | A high-level input resets the RDA output to a low-level. |
| 25 | RDE | Received Data Enable | A high-level input enables the outputs (RD8-RD1) of the receiver buffer register |
| 26 | RDA | Receiver Data Available | This output is at a high-level when an entire character has been received and transferred into the receiver buffer register. |
| 27 | ROR | Receiver Over-Run | This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register. |
| 28-35 | RD8-RD1 | Receiver Data Output | These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output. |
| 36, 38 | NDB2, NDB1 | Number of Data Bits | These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: |

| NDB2 | NDB1 | data bits/character |
|---|---|---|
| L | L | 5 |
| L | H | 6 |
| H | L | 7 |
| H | H | 8 |

## DESCRIPTION OF PIN FUNCTIONS

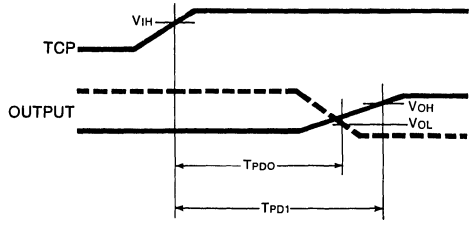
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 37 | NPB | No Parity Bit | A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE. |
| 39 | CS | Control Strobe | A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level. |
| 40 | POE | Odd/Even Parity Select | The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the reciever and transmitter, as per the following table: |

| NPB | POE | MODE |
|---|---|---|
| L | L | odd parity |
| L | H | even parity |
| H | X | no parity |

X = don't care

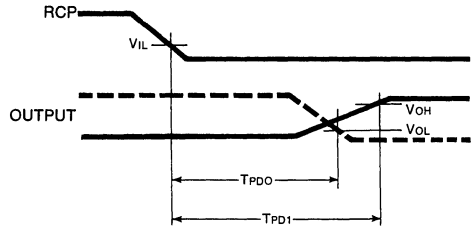
## ADDITIONAL TIMING INFORMATION
### (Typical Propagation Delays)

**Transmitter**

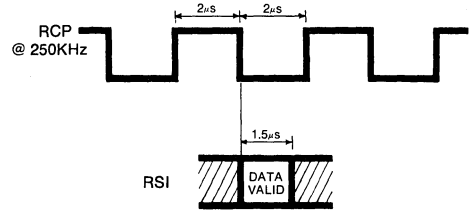



| OUTPUT | TPDO | TPD1 | UNITS |
|---|---|---|---|
| TBMT | NA | 2.0 | μs |
| SCT | 1.0 | 1.5 | μs |
| TSO | 1.0 | 1.0 | μs |

**Receiver**




| OUTPUT | TPDO | TPD1 | UNITS |
|---|---|---|---|
| RDA | NA | 1.0 | μs |
| ROR | 2.0 | 2.5 | μs |
| RPE | 2.0 | 2.5 | μs |
| SCR | 2.0 | 2.5 | μs |
| RD1-RD8 | 2.5 | 2.5 | μs |



**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, $V_{CC}$ ..... +0.3V
Negative Voltage on any Pin, $V_{CC}$ ..... −25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0° C to 70° C, $V_{CC}$ = +5V ±5%, $V_{DD}$ = −12V ±5%, unless otherwise noted)

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | $V_{DD}$ | | 0.8 | V | |
| High-level, $V_{IH}$ | $V_{CC}$-1.5 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | 0.2 | 0.4 | V | $I_{OL}$ = 1.6mA |
| High-level, $V_{OH}$ | 2.4 | 4.0 | | V | $I_{OH}$ = −100μA |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | 1.6 | mA | see note 1 |
| OUTPUT CURRENT | | | | | |
| Leakage, $I_{LO}$ | | | −1 | μA | RDE = $V_{IL}$, O ≤ $V_{OUT}$ ≤ +5V |
| Short circuit, $I_{OS}$** | | | 10 | mA | $V_{OUT}$ = 0V |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pf | $V_{IN}$ = $V_{CC}$, f = 1MHz |
| OUTPUT CAPACITANCE | | | | | |
| All outputs, $C_{OUT}$ | | 10 | 20 | pf | $R_{DE}$ = $V_{IL}$, f = 1MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 28 | mA | All outputs = $V_{OH}$ |
| $I_{DD}$ | | | 28 | mA | All outputs = $V_{OH}$ |
| **A.C. CHARACTERISTICS** | | | | | $T_A$ = +25° C |
| CLOCK FREQUENCY | DC | | 250 | KHz | RCP, TCP |
| PULSE WIDTH | | | | | |
| Clock | 1 | | | μs | RCP, TCP |
| Receiver reset | 1 | | | μs | RR |
| Control strobe | 200 | | | ns | CS |
| Transmitter data strobe | 200 | | | ns | TDS |
| Transmitter sync strobe | 200 | | | ns | TSS |
| Receiver sync strobe | 200 | | | ns | RSS |
| Receiver data available reset | 200 | | | ns | RDAR |
| INPUT SET-UP TIME | | | | | |
| Data bits | >0 | | | ns | DB1-DB8 |
| Control bits | >0 | | | ns | NPB, NDB2, NDB1, POE |
| INPUT HOLD TIME | | | | | |
| Data bits | >0 | | | ns | DB1-DB8 |
| Control bits | >0 | | | ns | NPB, NDB2, NDB1, POE |
| STROBE TO OUTPUT DELAY | | | | | Load = 20pf +1 TTL input |
| Receive data enable | | 180 | 250 | ns | RDE: $T_{PD1}$, $T_{PD0}$ |
| OUTPUT DISABLE DELAY | | 100 | 250 | ns | RDE |

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6 mA maximum flows during a transition of the input.
2. The three-state output has 3 states:
   1) low impedance to $V_{CC}$
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

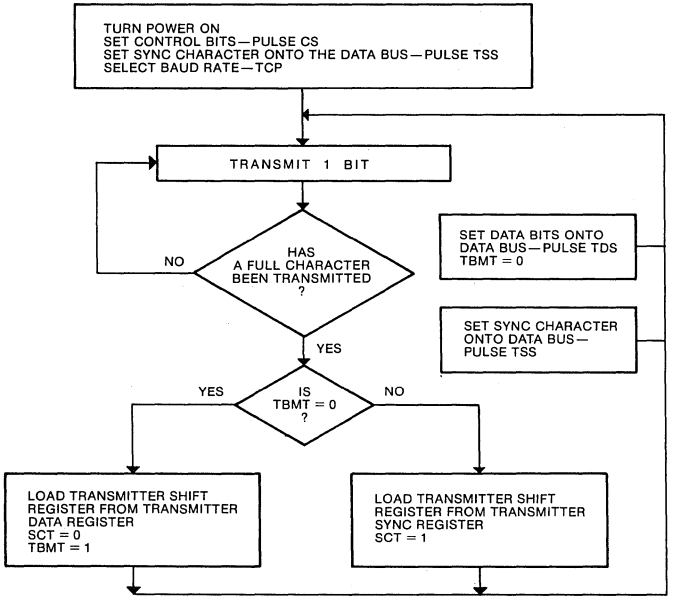
## DESCRIPTION OF OPERATION—RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

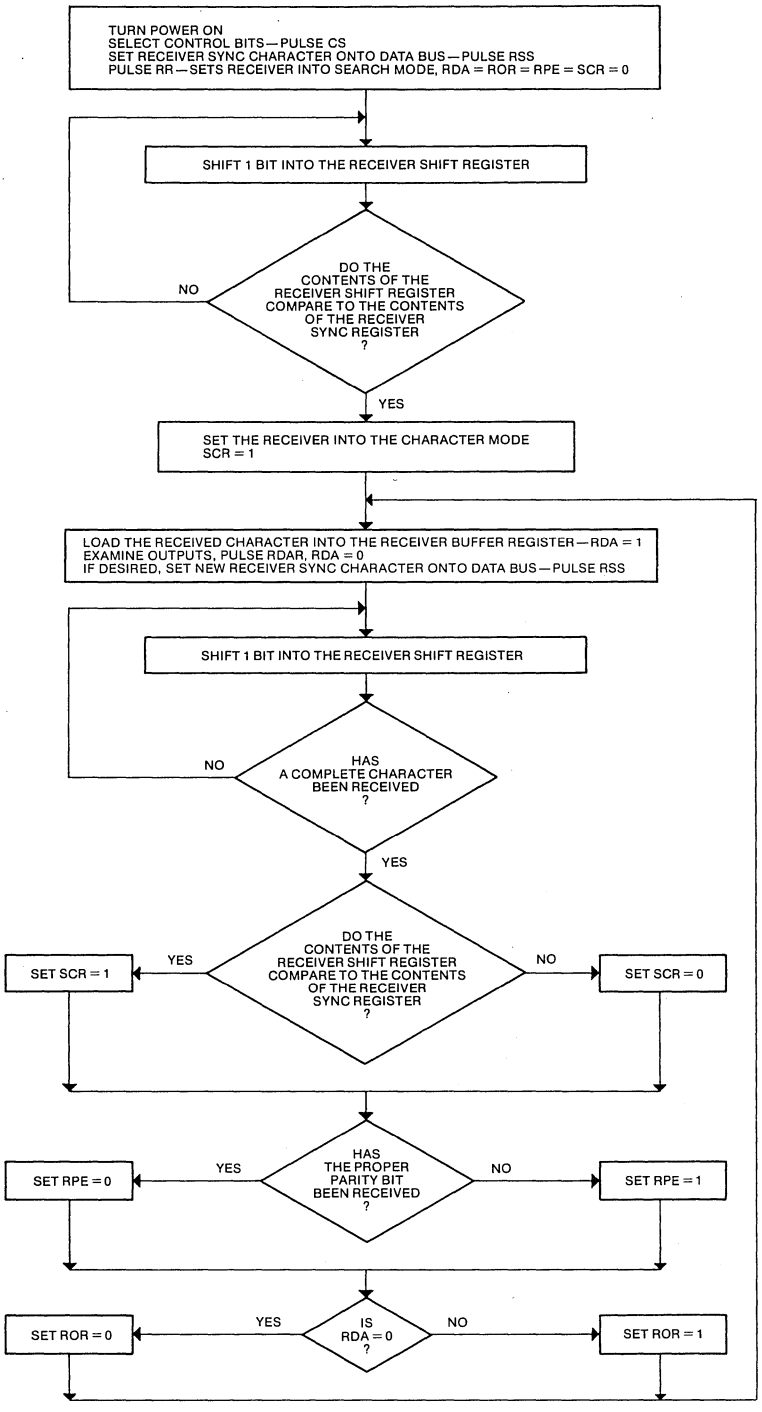
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data output levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

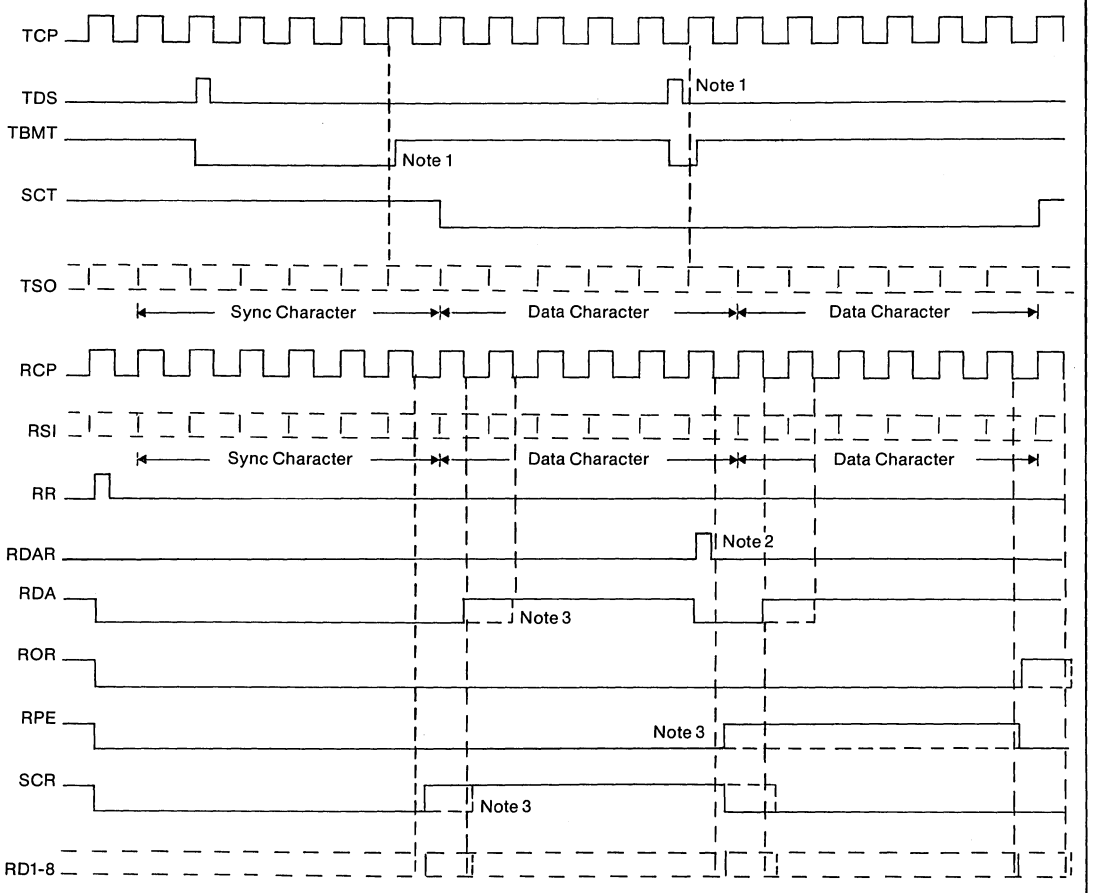
## FLOW CHART—TRANSMITTER



## FLOW CHART—RECEIVER



## USRT TIMING DIAGRAM




**NOTE 1**
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

**NOTE 2**
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

**NOTE 3**
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

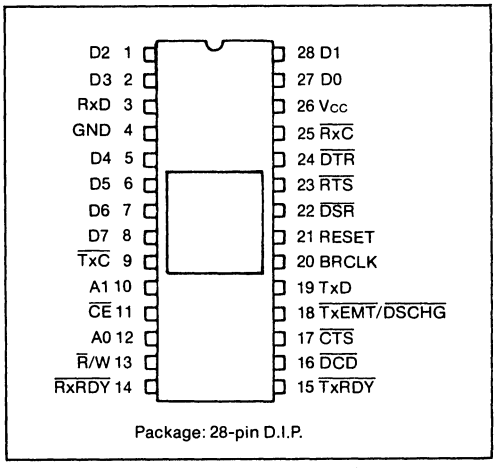
# Programmable Communication Interface PCI



## FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC or DLE Stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)
- ☐ Double Buffering of Data

## PIN CONFIGURATION



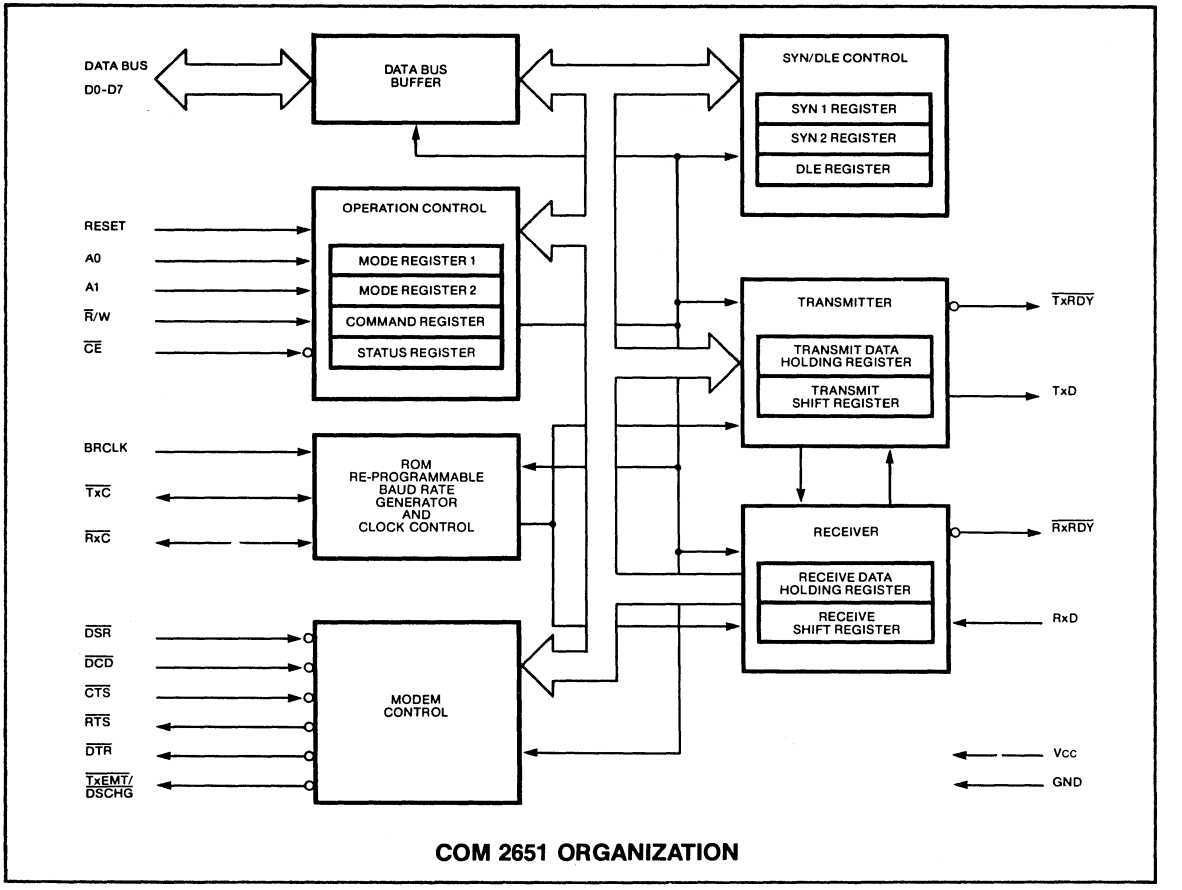

Package: 28-pin D.I.P.

- ☐ Internal or External Baud Rate Clock
  - —16 Internal Rates:50 to 19,200 Baud
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with 2651, INS2651

## GENERAL DESCRIPTION

The COM 2651 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. The on-chip baud rate generator can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2651 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.




**COM 2651 ORGANIZATION**

The COM 2651 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2651.

### Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the COM 2651 programming section of this specification.

### Timing

The COM 2651 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Table 6 illustrates all available baud rates.

### Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

### Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

### Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2651 and a modem.

### SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

### Interface Signals

The COM 2651 interface signals can be grouped into two types: the processor-related signals (shown in Table 2) which interface the COM 2651 to the processor, and the device-related signals (shown in Table 3), which are used to interface to the communications equipment.

**TABLE 2—PROCESSOR RELATED SIGNALS**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1,2,5,6, 7,8,27,28 | Data | D7-DØ | Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2651 and a processor. DØ is the least significant bit; D7 is the most significant bit. |
| 10,12 | Address | A1, AØ | Input; Address lines used to select COM 2651 registers. |
| 11 | Chip Enable | $\overline{CE}$ | Input; when this signal is low, the operation specified by the $\overline{R}$/W, A1 and AØ will be performed. When this input is high, D7-Ø are in the high impedance state. |
| 13 | Read/Write | $\overline{R}$/W | Input; Processor read/write direction control. This signal defines the direction of the data bus D7-Ø when the COM 2651 is selected. D7-Ø drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the chip enable input is active. |
| 14 | Receiver Ready | $\overline{RxRDY}$ | Output; This signal is the complement of Status Register bit 1 (SR1). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor. |
| 15 | Transmitter Ready | $\overline{TxRDY}$ | Output; This signal is the complement of Status Register bit 0 (SR0). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor. |
| 18 | Transmitter empty/data set change | $\overline{TxEMT}$/ $\overline{DSCHG}$ | Output; This signal is the complement of Status Register bit 2 (SR2). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor. |
| 21 | Reset | Reset | Input; A high on this input performs a master reset on the COM 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words. |
| 26 | Supply Voltage | $V_{CC}$ | +5 volts supply. |
| 4 | Ground | GND | Ground. |

**TABLE 3—DEVICE RELATED SIGNALS**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 3 | Receive Data | RxD | Input; Serial data to the receiver. "Mark" is high "space" is low. |
| 9 | Transmitter Clock | $\overline{TxC}$ | Input or Output; If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X, the Baud rate as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin becomes an output at 1X the programmed Baud rate. |
| 16 | Data Carrier Detect | $\overline{DCD}$ | Input; This signal must be low in order for the receiver to function. The complement appears in the Status Register bit 6 (SR6). When this input changes state a low output on $\overline{TxEMT/DSCHG}$ occurs. |
| 17 | Clear to Send | $\overline{CTS}$ | Input; This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination. |
| 19 | Transmit Data | TxD | Output; Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled. |
| 20 | Baud Rate Clock | BRCLK | Input; The standard device requires a 5.0688MHz clock to the internal Baud rate generator allowing for Baud rate shown in Table 6. The reprogrammable ROM on chip allows for user specificed Baud rates and input frequency. Consult the factory for details. This input is not required if external receive and transmit clocks are used. |
| 22 | Data Set Ready | $\overline{DSR}$ | Input; This general purpose signal can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit 7 (SR7). When this input changes state, a low output on $\overline{TxEMT/DSCHG}$ occurs. |
| 23 | Request to Send | $\overline{RTS}$ | Output; This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. |

**TABLE 3—DEVICE RELATED SIGNALS**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 24 | Data Terminal | $\overline{DTR}$ | Output; This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Data Terminal Ready. |
| 25 | Receive Clock | $\overline{RxC}$ | Input or Output; If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate, as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed Baud rate. |

## COM 2651 OPERATION

The functional operation of the COM 2651 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2651 Programming section of this data sheet.

After programming, the COM 2651 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specificed by the control words.

### Receiver

The COM 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition on the RxD input line indicating the start bit. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit[s]), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the COM 2651 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Reciver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2651 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2651 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the $\overline{RxRDY}$ output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

### Transmitter

The COM 2651 is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The COM 2651 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the $\overline{TxRDY}$ output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2651 unless the processor fails to send a new character to the COM 2651 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2651

asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

## COM 2651 PROGRAMMING

Prior to initiating data communications, the COM 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2651 can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if the change is made 1½ $\overline{RxC}$ periods after RxRDY goes active it will affect the next character assembly. A flowchart of the initialization process appears in Figure 1.

The internal registers of the COM 2651 are accessed by applying specific signals to the $\overline{CE}$, R/$\overline{W}$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and R/$\overline{W}$=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the COM 2651, while the Command Register controls the operation within this basic framework. The COM 2651 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

**COM 2651 INITIALIZATION FLOW CHART**

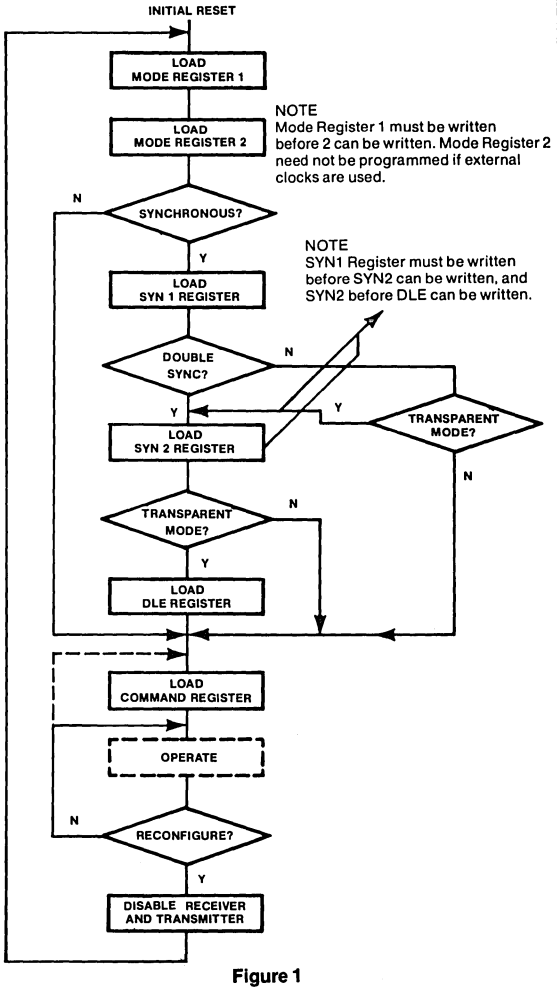



**Figure 1**

| $\overline{CE}$ | A1 | A0 | R/$\overline{W}$ | FUNCTION |
|---|---|---|---|---|
| 1 | X | X | X | Tri-state data bus |
| 0 | 0 | 0 | 0 | Read receive holding register |
| 0 | 0 | 0 | 1 | Write transmit holding register |
| 0 | 0 | 1 | 0 | Read status register |
| 0 | 0 | 1 | 1 | Write SYN1/SYN2/DLE registers |
| 0 | 1 | 0 | 0 | Read mode registers 1 and 2 |
| 0 | 1 | 0 | 1 | Write mode registers 1 and 2 |
| 0 | 1 | 1 | 0 | Read command register |
| 0 | 1 | 1 | 1 | Write command register |

NOTE
See AC Characteristics section for timing requirements.

**Table 4—COM 2651 REGISTER ADDRESSING**

## MODE REGISTER 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

| MR17 | MR16 | MR15 | MR14 | MR13 | MR12 | MR11 | MR10 |
|---|---|---|---|---|---|---|---|
| Sync/Async | | Parity Type | Parity Control | Character Length | | Mode and Baud Rate Factor | |
| ASYNCH: STOP BIT LENGTH<br>00=INVALID<br>01=1 STOP BIT<br>10=1½ STOP BITS<br>11=2 STOP BITS | | 0=ODD<br>1=EVEN | 0=DISABLED<br>1=ENABLED | 00=5 BITS<br>01=6 BITS<br>10=7 BITS<br>11=8 BITS | | 00=SYNCHRONOUS 1X RATE<br>01=ASYNCHRONOUS 1X RATE<br>10=ASYNCHRONOUS 16X RATE<br>11=ASYNCHRONOUS 64X RATE | |
| SYNCH: NUMBER OF SYN CHAR<br>0=DOUBLE SYN<br>1=SINGLE SYN | SYNCH: TRANSPARENCY CONTROL<br>0=NORMAL<br>1=TRANSPARENT | | | | | | |

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

**TABLE 5—MODE REGISTER 1 (MR1)**

## MODE REGISTER 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal Baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 Baud, which have errors of +0.016% +0.253%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the Baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the Baud rate. Custom Baud rates other than the ones provided by the standard part are available. Contact the factory for details.

| MR27 | MR26 | MR25 | MR24 | MR23-MR20 | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Transmitter Clock | Receiver Clock | Code | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Divisor |
| NOT USED | | 0=EXTERNAL<br>1=INTERNAL | 0=EXTERNAL<br>1=INTERNAL | 0000 | 50 | 0.8 KHz | 0.8 KHz | — | 6336 |
| | | | | 0001 | 75 | 1.2 | 1.2 | — | 4224 |
| | | | | 0010 | 110 | 1.76 | 1.76 | — | 2880 |
| | | | | 0011 | 134.5 | 2.152 | 2.1523 | 0.016 | 2355 |
| | | | | 0100 | 150 | 2.4 | 2,4 | — | 2112 |
| | | | | 0101 | 300 | 4.8 | 4.8 | — | 1056 |
| | | | | 0110 | 600 | 9.6 | 9.6 | — | 528 |
| | | | | 0111 | 1200 | 19.2 | 19.2 | — | 264 |
| | | | | 1000 | 1800 | 28.8 | 28.8 | — | 176 |
| | | | | 1001 | 2000 | 32.0 | 32.081 | 0.253 | 158 |
| | | | | 1010 | 2400 | 38.4 | 38.4 | — | 132 |
| | | | | 1011 | 3600 | 57.6 | 57.6 | — | 88 |
| | | | | 1100 | 4800 | 76.8 | 76.8 | — | 66 |
| | | | | 1101 | 7200 | 115.2 | 115.2 | — | 44 |
| | | | | 1110 | 9600 | 153.6 | 153.6 | — | 33 |
| | | | | 1111 | 19200* | 307.2 | 316.8 | 3.125 | 16 |

NOTE *Error at 19200 can be reduced to zero by using crystal frequency 4.9152MHz
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.
Baud rates are valid for crystal frequency = 5.0688MHz

**TABLE 6—MODE REGISTER 2 (MR2)**

## COMMAND REGISTER (CR)

Table 7 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while the $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5 ) to be cleared. This is a one time command. There is no internal latch for this bit.

The COM 2651 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2651 in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continues normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output=1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2651 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching, SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR. However, only the first SYN1 of an SYN1-SYN1 pair is stripped.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the COM 2651.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|---|---|---|---|---|---|---|---|
| Operating Mode | | Request to Send | Reset Error | Sync/Async | Receive Control (RxEN) | Data Terminal Ready | Transmit Control (TxEN) |
| 00=NORMAL OPERATION<br>01=ASYNCH: AUTOMATIC ECHO MODE<br>SYNCH: SYN AND/OR DLE STRIPPING MODE<br>10=LOCAL LOOP BACK<br>11=REMOTE LOOP BACK | | 0=FORCE $\overline{RTS}$ OUTPUT HIGH<br>1=FORCE $\overline{RTS}$ OUTPUT LOW | 0=NORMAL<br>1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT) | **ASYNCH: FORCE BREAK**<br>0=NORMAL<br>1=FORCE BREAK<br>**SYNCH: SEND DLE**<br>0=NORMAL<br>1=SEND DLE | 0=DISABLE<br>1=ENABLE | 0=FORCE $\overline{DTR}$ OUTPUT HIGH<br>1=FORCE $\overline{DTR}$ OUTPUT LOW | 0=DISABLE<br>1=ENABLE |

**TABLE 7—COMMAND REGISTER (CR)**

## STATUS REGISTER (SR)

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero. there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. It is cleared when the Status Register is read by the processor. When SR2 is set, the TxEMT/DSCHG output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

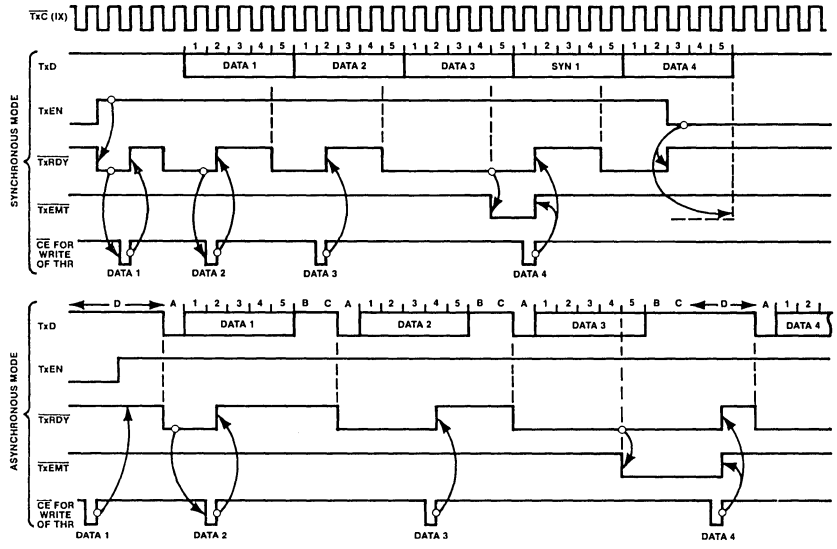
In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (if 1.5 stop bits are programmed, only the first stop bit is checked.) If the RHR contains all 0's when SR5=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when the Status Register is read by the processor in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| **Data Set Ready** | **Data Carrier Detect** | **FE/SYN Detect** | **Overrun** | **PE/DLE Detect** | **TxEMT/DSCHG** | **RxRDY** | **TxRDY** |
| 0=$\overline{\text{DSR}}$ INPUT IS HIGH<br>1=$\overline{\text{DSR}}$ INPUT IS LOW | 0=$\overline{\text{DCD}}$ INPUT IS HIGH<br>1=$\overline{\text{DCD}}$ INPUT IS LOW | **ASYNCH:**<br>0=NORMAL<br>1=FRAMING ERROR<br>**SYNCH:**<br>0=NORMAL<br>1=SYN CHAR DETECTED | 0=NORMAL<br>1=OVERRUN ERROR | **ASYNCH:**<br>0=NORMAL<br>1=PARITY ERROR<br>**SYNCH:**<br>0=NORMAL<br>1=PARITY ERROR OR DLE CHAR RECEIVED | 0=NORMAL<br>1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY | 0=RECEIVE HOLDING REG EMPTY<br>1=RECEIVE HOLDING REG HAS DATA | 0=TRANSMIT HOLDING REG BUSY<br>1=TRANSMIT HOLDING REG EMPTY |

**TABLE 8—STATUS REGISTER (SR)**

**TxRDY, TxEMT** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

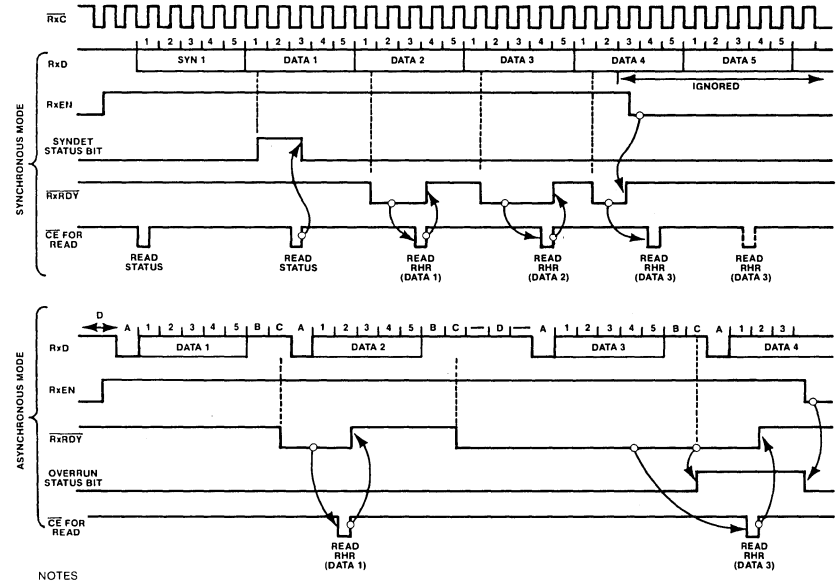



NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

**RxRDY** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

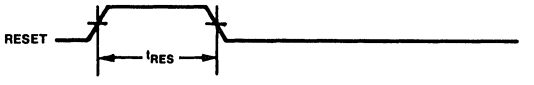



NOTES

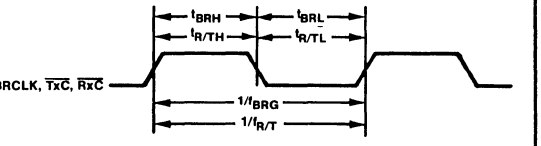
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

# TIMING DIAGRAMS (Cont'd)

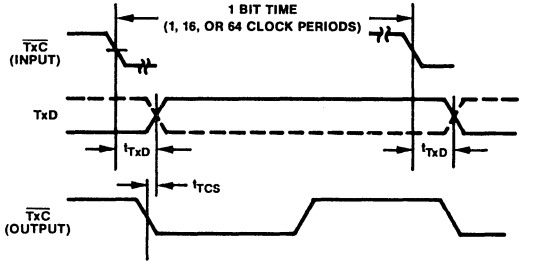
## RESET



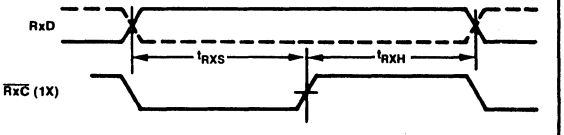

## CLOCK



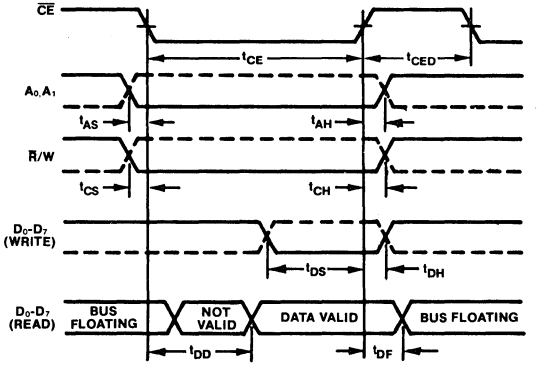

## TRANSMIT




## RECEIVE




## READ AND WRITE



**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it it important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.



**DC ELECTRICAL CHARACTERISTICS** $T_A$=0°C to +70°C, $V_{CC}$=5.0V ±5%

| | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | Input voltage | | | | | |
| $V_{IL}$ | Low | | | 0.8 | V | |
| $V_{IH}$ | High | 2.0 | | | | |
| | Output voltage | | | | | |
| $V_{OL}$ | Low | | | 0.4 | V | $I_{OL}$=1.6mA |
| $V_{OH}$ | High | 2.4 | | | | $I_{OH}$=−100μA |
| $I_{IL}$ | Input leakage current | | | 10 | μA | $V_{IN}$=0 to 5.25V |
| | Output leakage current | | | | | |
| $I_{LH}$ | Data bus high | | | 10 | μA | $V_O$=4.0V |
| $I_{LL}$ | Data bus low | | | 10 | μA | $V_O$=0.45V |
| $I_{CC}$ | Power supply current | | | 150 | mA | |
| | Capacitance | | | | | |
| $C_{IN}$ | Input | | | 20 | pF | fc=1MHz |
| $C_{OUT}$ | Output | | | 20 | pF | Unmeasured pins tied to ground |
| $C_{I/O}$ | Input/Output | | | 20 | pF | |

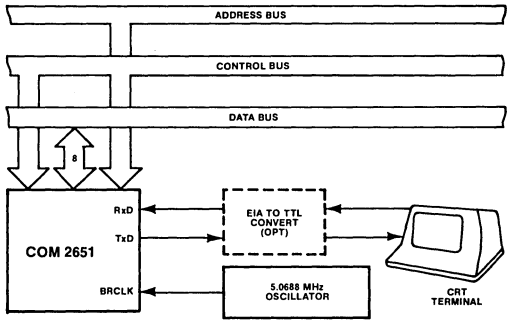
**AC ELECTRICAL CHARACTERISTICS** $T_A$=0°C to +70°C, $V_{CC}$=5.0V ±5%

| | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | Pulse width | | | | | |
| $t_{RES}$ | Reset | 1000 | | | ns | |
| $t_{CE}$ | Chip enable | 300 | | | ns | |
| | Setup and hold time | | | | | |
| $t_{AS}$ | Address setup | 20 | | | ns | |
| $t_{AH}$ | Address hold | 20 | | | ns | |
| $t_{CS}$ | R/$\overline{W}$ control setup | 20 | | | ns | |
| $t_{CH}$ | R/$\overline{W}$ control hold | 20 | | | ns | |
| $t_{DS}$ | Data setup for write | 225 | | | ns | |
| $t_{DH}$ | Data hold for write | 0 | | | ns | |
| $t_{RXS}$ | Rx data setup | 300 | | | ns | |
| $t_{RXH}$ | Rx data hold | 350 | | | ns | |
| $t_{DD}$ | Data delay time for read | | | 250 | ns | $C_L$=100pF |
| $t_{DF}$ | Data bus floating time for read | | | 150 | ns | $C_L$=100pF |
| $t_{CED}$ | $\overline{CE}$ to $\overline{CE}$ delay | 700 | | | ns | |
| | Input clock frequency | | | | | |
| $f_{BRG}$ | Baud rate generator | 1.0 | 5.0688 | 5.0738 | MHz | |
| $f_{R/T}$[1] | $\overline{TxC}$ or $\overline{RxC}$ | dc | | 1.0 | MHz | |
| | Clock width | | | | | |
| $t_{BRH}$ | Baud rate high | 70 | | | ns | $f_{BRG}$=5.0688MHz |
| $t_{BRL}$ | Baud rate low | 70 | | | ns | $f_{BRG}$=5.0688MHz |
| $t_{R/TH}$[1] | $\overline{TxC}$ or $\overline{RxC}$ high | 500 | | | ns | |
| $t_{R/TL}$[1] | $\overline{TxC}$ or $\overline{RxC}$ low | 500 | | | ns | |
| $t_{TXD}$ | TxD delay from falling edge of $\overline{TxC}$ | | | 650 | ns | $C_L$=100pF |
| $t_{TCS}$ | Skew between TxD changing and falling edge of $\overline{TxC}$ output | | 0 | | ns | $C_L$=100pF |

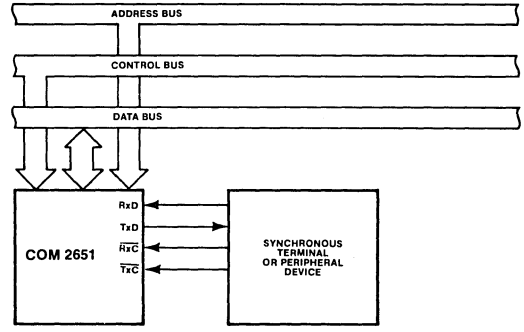
NOTE:
1. $f_{R/T}$ and $t_{R/TL}$ shown for all modes except Local Loopback. For Local Loopback mode $f_{R/T}$=0.7 MHz and $t_{R/TL}$=700ns min.

# TYPICAL APPLICATIONS

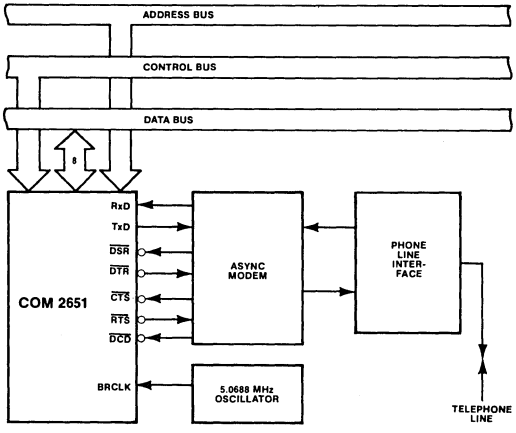
## ASYNCHRONOUS INTERFACE TO CRT TERMINAL



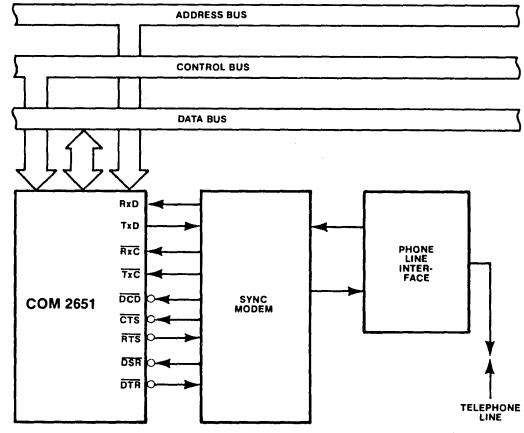

## SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE




## ASYNCHRONOUS INTERFACE TO TELEPHONE LINES




## SYNCHRONOUS INTERFACE TO TELEPHONE LINES




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM 2661-1
# COM 2661-2
# COM 2661-3
## μPC FAMILY

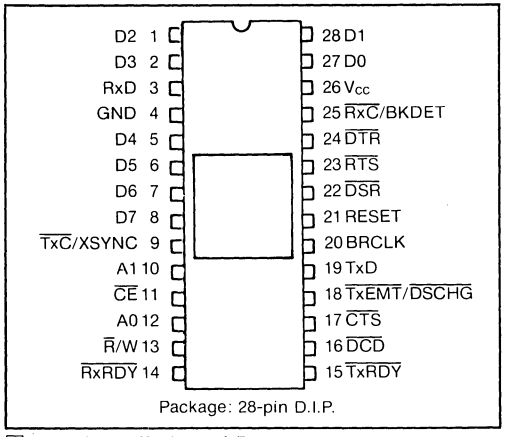
# Enhanced Programmable Communication Interface EPCI



## FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal or External Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Transparent mode DLE stuffing (Tx) and detection (Rx)
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC, DLE and DLE-SYNC stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters plus parity
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)

## PIN CONFIGURATION



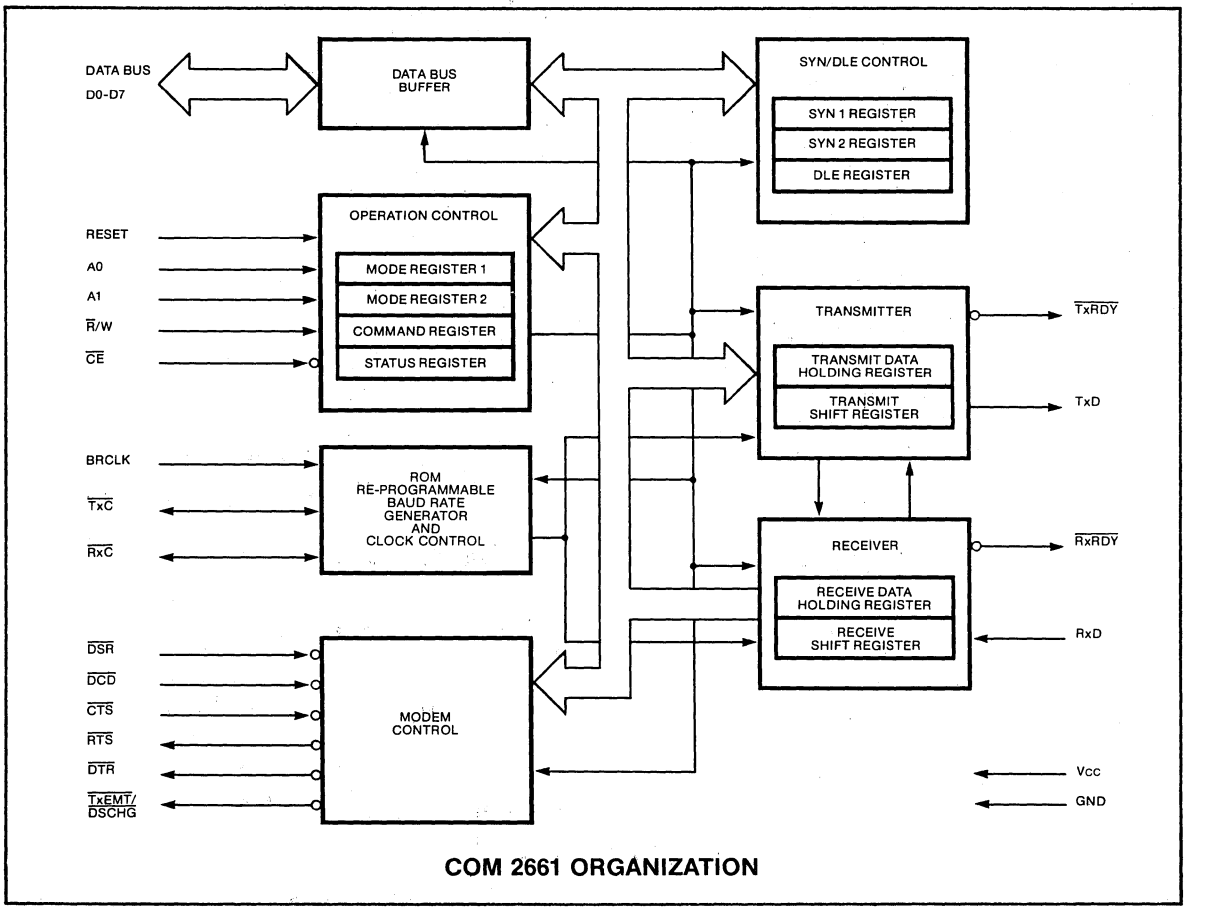

Package: 28-pin D.I.P.

- ☐ Double Buffering of Data
- ☐ RxC and TxC pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2661-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with EPCI 2661

## GENERAL DESCRIPTION

The COM 2661 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is an enhanced pin and register compatible version of the COM 2651 that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2661 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2661 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.




**COM 2661 ORGANIZATION**

The COM 2661 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2661. The differences between the COM 2661 and COM 2651 are outlined in table 1.

## Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the COM 2661 programming section of this specification.

## Timing

The COM 2661 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Tables 2a, b, and c illustrate all available baud rates.

## Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

## Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

## Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2661 and a modem.

## SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

## Interface Signals

The COM 2661 interface signals can be grouped into two types: the processor-related signals (shown in Table 3) which interface the COM 2661 to the processor, and the device-related signals (shown in Table 4), which are used to interface to the communications equipment.

**TABLE 3—PROCESSOR RELATED SIGNALS**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1,2,5,6, 7,8,27,28 | Data | D7-DØ | Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2661 and a processor. DØ is the least significant bit; D7 is the most significant bit. |
| 10, 12 | Address | A1, AØ | Input; Address lines used to select COM 2661 registers. |
| 11 | Chip Enable | $\overline{CE}$ | Input; when this signal is low, the operation specified by the $\overline{R}$/W, A1 and AØ will be performed. When this input is high, D7-Ø are in the high impedance state. |
| 13 | Read/Write | $\overline{R}$/W | Input; Processor read/write direction control. This signal defines the direction of the data bus D7-0 when the COM 2661 is selected. D7-Ø drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the $\overline{CE}$ input is active. |
| 14 | Receiver Ready | $\overline{RxRDY}$ | Output; This signal is the complement of Status Register bit 1 (SR1). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor. |
| 15 | Transmitter Ready | $\overline{TxRDY}$ | Output; This signal is the complement of Status Register bit 0 (SR0). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor. |
| 18 | Transmitter empty/data set change | $\overline{TxEMT}$/ $\overline{DSCHG}$ | Output; This signal is the complement of Status Register bit 2 (SR2). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor. |
| 21 | Reset | Reset | Input; A high on this input performs a master reset on the COM 2661. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words. |
| 26 | Supply Voltage | $V_{CC}$ | +5 volts supply. |
| 4 | Ground | GND | Ground. |

**TABLE 4—DEVICE RELATED SIGNALS**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 3 | Receive Date | RxD | Input; Serial data to the receiver. "Mark" is high "space" is low. |
| 9 | Transmitter Clock/External Sync | $\overline{TxC}$/ XSYNC | Input or Output; If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X, the Baud rate as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input. |
| 16 | Data Carrier Detect | $\overline{DCD}$ | Input; This signal must be low in order for the receiver to function. The complement appears in the Status Register bit 6 (SR6). $\overline{DCD}$ causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited. |
| 17 | Clear to Send | $\overline{CTS}$ | Input; This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination. |
| 19 | Transmit Data | TxD | Output; Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled. |
| 20 | Baud Rate Clock | BRCLK | Input; Clock input to the internal baud rate generator (See Tables 2a, b and c); not required if the external receiver and transmitter clocks are used. |
| 22 | Data Set Ready | $\overline{DSR}$ | Input; This general purpose signal can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit 7 (SR7). $\overline{DSR}$ causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1. |
| 23 | Request to Send | $\overline{RTS}$ | Output; This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. If the Transmit Shift Register is not empty when CR5 is reset (1 to 0), then $\overline{RTS}$ will go high on TxC time after the last serial bit is transmitted. |
| 24 | Data Terminal Ready | $\overline{DTR}$ | Output; This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Data Terminal Ready. |
| 25 | Receive Clock/ Break Detect | $\overline{RxC}$/ BKDET | Input or Output; If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate, as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output. |

**Table 1 COM 2661 vs. COM 2651**

| FEATURE | EPCI | PCI |
|---|---|---|
| 1. MR2 Bit 6, 7 | Control pin 9, 25 | Not used |
| 2. DLE detect-SR3 | SR3=0 for DLE-DLE, DLE-SYNC1 | SR3=1 for DLE-DLE, DLE-SYNC1 |
| 3. Reset of SR3, DLE detect | Second character after DLE; or receiver disable, or CR4=1 | Receiver disable, or CR4=1 |
| 4. Send DLE-CR3 | One time command | Reset via CR3 on next TxRDY |
| 5. DLE stuffing in transparent mode | Automatic DLE stuffing when DLE is loaded except if CR3=1 | None |
| 6. SYNC1 stripping in double sync non-transparent mode | All SYNC1 | First SYNC1 of pair |
| 7. Baud rate versions | Three | One |
| 8. Terminate ASYNC transmission (drop RTS) | Reset CR5 in response to TxRDY changing from 0 to 1 | Reset CR0 when TxEMT goes from 1 to 0. Then reset CR5 when TxEMT goes from 0 to 1 |
| 9. Break detect | Pin 25[1] | FE and null character |
| 10. Stop bit searched | One | Two |
| 11. External jam sync | Pin 9[2] | No |
| 12. Data bus timing | Improved over 2651 | — |
| 13. Data bus drivers | Sink 2.2mA Source 400μA | Sink 1.6mA Source 100μA |

NOTES
1. Internal BRG used for RxC.
2. Internal BRG used for TxC.

**Table 2a BAUD RATE GENERATOR CHARACTERISTICS 2661-1 (BRCLK=4.9152MHz)**

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 50 | 0.8kHz | — | 6144 |
| 0001 | 75 | 1.2 | — | 4096 |
| 0010 | 110 | 1.7598 | −0.01 | 2793 |
| 0011 | 134.5 | 2.152 | — | 2284 |
| 0100 | 150 | 2.4 | — | 2048 |
| 0101 | 200 | 3.2 | — | 1536 |
| 0110 | 300 | 4.8 | — | 1024 |
| 0111 | 600 | 9.6 | — | 512 |
| 1000 | 1050 | 16.8329 | 0.196 | 292 |
| 1001 | 1200 | 19.2 | — | 256 |
| 1010 | 1800 | 28.7438 | −0.19 | 171 |
| 1011 | 2000 | 31.9168 | −0.26 | 154 |
| 1100 | 2400 | 38.4 | — | 128 |
| 1101 | 4800 | 76.8 | — | 64 |
| 1110 | 9600 | 153.6 | — | 32 |
| 1111 | 19200 | 307.2 | — | 16 |

**Table 2b BAUD RATE GENERATOR CHARACTERISTICS 2661-2 (BRCLK=4.9152MHz)**

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 45.5 | 0.7279kHz | 0.005 | 6752 |
| 0001 | 50 | 0.8 | — | 6144 |
| 0010 | 75 | 1.2 | — | 4096 |
| 0011 | 110 | 1.7598 | −0.01 | 2793 |
| 0100 | 134.5 | 2.152 | — | 2284 |
| 0101 | 150 | 2.4 | — | 2048 |
| 0110 | 300 | 4.8 | — | 1024 |
| 0111 | 600 | 9.6 | — | 512 |
| 1000 | 1200 | 19.2 | — | 256 |
| 1001 | 1800 | 28.7438 | −0.19 | 171 |
| 1010 | 2000 | 31.9168 | −0.26 | 154 |
| 1011 | 2400 | 38.4 | — | 128 |
| 1100 | 4800 | 76.8 | — | 64 |
| 1101 | 9600 | 153.6 | — | 32 |
| 1110 | 19200 | 307.2 | — | 16 |
| 1111 | 38400 | 614.4 | — | 8 |

**Table 2c BAUD RATE CHARACTERISTICS 2661-3 (BRCLK=5.0688MHz)**

| MR23-20 | BAUD RATE | ACTUAL FREQUENCY 16X CLOCK | PERCENT ERROR | DIVISOR |
|---|---|---|---|---|
| 0000 | 50 | 0.8kHz | — | 6336 |
| 0001 | 75 | 1.2 | — | 4224 |
| 0010 | 110 | 1.76 | — | 2880 |
| 0011 | 134.5 | 2.1523 | 0.016 | 2355 |
| 0100 | 150 | 2.4 | — | 2112 |
| 0101 | 300 | 4.8 | — | 1056 |
| 0110 | 600 | 9.6 | — | 528 |
| 0111 | 1200 | 19.2 | — | 264 |
| 1000 | 1800 | 28.8 | — | 176 |
| 1001 | 2000 | 32.081 | 0.253 | 158 |
| 1010 | 2400 | 38.4 | — | 132 |
| 1011 | 3600 | 57.6 | — | 88 |
| 1100 | 4800 | 76.8 | — | 66 |
| 1101 | 7200 | 115.2 | — | 44 |
| 1110 | 9600 | 153.6 | — | 33 |
| 1111 | 19200 | 316.8 | 3.125 | 16 |

NOTE:
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

# COM 2661 OPERATION

The functional operation of the COM 2661 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2661 Programming section of this data sheet.

After programming, the COM 2661 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specified by the control words.

## Receiver

The COM 2661 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the COM 2661 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2661 returns to the hunt mode. (Note that the sequence SYN1-SYN1-

SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2661 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the RxRDY output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

### Transmitter

The COM 2661 is conditioned to transmit data when the CTS input is low and the TxEN command register bit is set. The COM 2661 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the TxRDY output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2661 unless the processor fails to send a new character to the COM 2661 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2661 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

## COM 2661 PROGRAMMING

Prior to initiating data communications, the COM 2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2661 can be reconfigured at any time during program execution. A flow chart of the initialization process appears in Figure 1.

The internal registers of the COM 2661 are accessed by applying specific signals to the CE, R/W, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 5.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and R/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more



**COM 2661 INITIAL FLOW CHART**

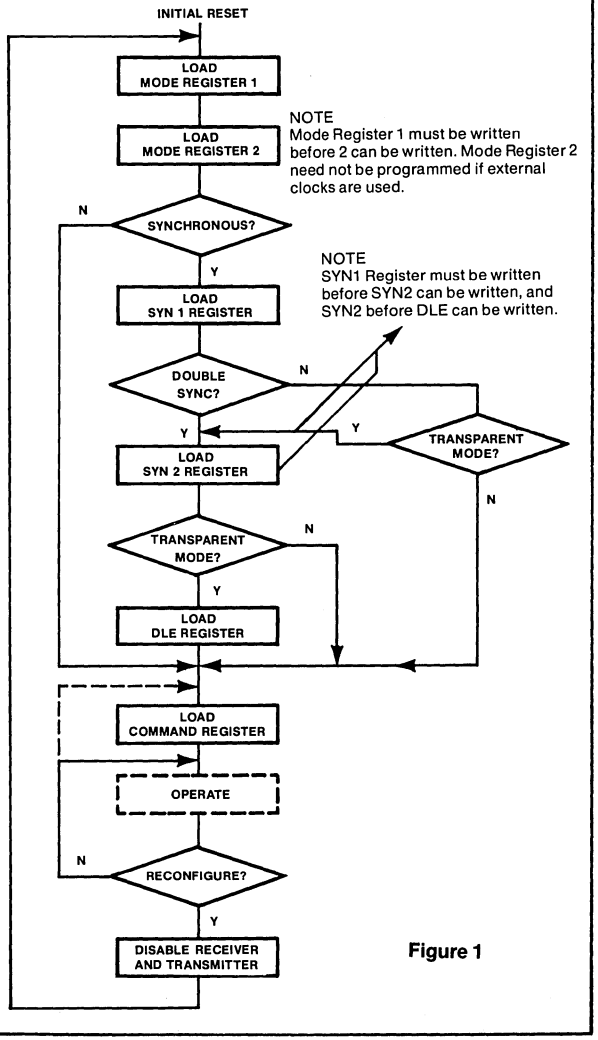



**Figure 1**

than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2661 register formats are summarized in Tables 6, 7, 8 and 9. Mode Registers 1 and 2 define the general operational characteristics of the COM 2661, while the Command Register controls the operation within this basic framework. The COM 2661 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

| $\overline{CE}$ | A1 | A0 | $\overline{R}$/W | FUNCTION |
|---|---|---|---|---|
| 1 | X | X | X | Tri-state data bus |
| 0 | 0 | 0 | 0 | Read receive holding register |
| 0 | 0 | 0 | 1 | Write transmit holding register |
| 0 | 0 | 1 | 0 | Read status register |
| 0 | 0 | 1 | 1 | Write SYN1/SYN2/DLE registers |
| 0 | 1 | 0 | 0 | Read mode registers 1 and 2 |
| 0 | 1 | 0 | 1 | Write mode registers 1 and 2 |
| 0 | 1 | 1 | 0 | Read command register |
| 0 | 1 | 1 | 1 | Write command register |

NOTE
See AC Characteristics section for timing requirements.

**Table 5—COM 2661 REGISTER ADDRESSING**

## MODE REGISTER 1 (MR1)

Table 6 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

| MR17 | MR16 | MR15 | MR14 | MR13 | MR12 | MR11 | MR10 |
|---|---|---|---|---|---|---|---|
| Sync/Async | | Parity Type | Parity Control | Character Length | | Mode and Baud Rate Factor | |
| ASYNCH: STOP BIT LENGTH<br>00=INVALID<br>01=1 STOP BIT<br>10=1½ STOP BITS<br>11=2 STOP BITS | | 0=ODD<br>1=EVEN | 0=DISABLED<br>1=ENABLED | 00=5 BITS<br>01=6 BITS<br>10=7 BITS<br>11=8 BITS | | 00=SYNCHRONOUS 1X RATE<br>01=ASYNCHRONOUS 1X RATE<br>10=ASYNCHRONOUS 16X RATE<br>11=ASYNCHRONOUS 64X RATE | |
| SYNCH: NUMBER OF SYN CHAR<br>0=DOUBLE SYN<br>1=SINGLE SYN | SYNCH: TRANSPARENCY CONTROL<br>0=NORMAL<br>1=TRANSPARENT | | | | | | |

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

**TABLE 6—MODE REGISTER 1 (MR1)**

## MODE REGISTER 2 (MR2)

Table 7 illustrates mode register 2 (MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each COM 2661 version (-1, -2, -3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the COM 2651. MR23-20 are don't cares if external clocks are selected (MR25-24=0). The individual rates are given in table 2a, b and c.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 7.

| MR-27-MR24 | | | | | | | | | | | MR23-MR20 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | TxC | RxC | Pin 9 | Pin 25 | | TxC | RxC | Pin 9 | Pin 25 | Mode | Baud Rate Selection |
| 0000 | E | E | TxC | RxC | 1000 | E | E | XSYNC[1] | RxC/TxC | sync | |
| 0001 | E | I | TxC | 1X | 1001 | E | I | TxC | BKDET | async | |
| 0010 | I | E | 1X | RxC | 1010 | I | E | XSYNC[1] | RxC | sync | |
| 0011 | I | I | 1X | 1X | 1011 | I | I | 1X | BKDET | async | See baud rates in table 2 |
| 0100 | E | E | TxC | RxC | 1100 | E | E | XSYNC[1] | RxC/TxC | sync | |
| 0101 | E | I | TxC | 16X | 1101 | E | I | TxC | BKDET | async | |
| 0110 | I | E | 16X | RxC | 1110 | I | E | XSYNC[1] | RxC | sync | |
| 0111 | I | I | 16X | 16X | 1111 | I | I | 16X | BKDET | async | |

NOTES
1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E=External clock I=Internal clock (BRG)
1X and 16X are clock outputs

**TABLE 7—MODE REGISTER 2 (MR2)**

## COMMAND REGISTER (CR)

Table 8 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second RxC rising edge. Disabling the receiver causes RxRDY to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high while the TxRDY and TxEMT will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. Bits CR1 (DTR) and CR5 (RTS) control the DTR and RTS outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit. When CR5 (RTS) is set, the RTS pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause RTS to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The COM 2661 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic Echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continue normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. TxRDY output=1.
4. The TxEMT/DSCHG pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. DTR is connected to DCD and RTS is connected to CTS.
3. The receiver is clocked by the transmit clock.
4. The DTR, RTS and TxD outputs are held high.
5. The CTS, DCD, DSR and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the COM 2661.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The RxRDY, TxRDY, and TxEMT/DSCHG outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
|---|---|---|---|---|---|---|---|
| Operating Mode | | Request to Send | Reset Error | Sync/Async | Receive Control (RxEN) | Data Terminal Ready | Transmit Control (TxEN) |
| 00=NORMAL OPERATION<br>01=ASYNCH: AUTOMATIC ECHO MODE<br>SYNCH: SYN AND/OR DLE STRIPPING MODE<br>10=LOCAL LOOP BACK<br>11=REMOTE LOOP BACK | | 0 FORCE RTS OUTPUT HIGH ONE CLOCK TIME AFTER TxSR SERIALIZATION<br>1 FORCE RTS OUTPUT LOW | 0=NORMAL<br>1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT) | ASYNCH: FORCE BREAK<br>0=NORMAL<br>1=FORCE BREAK<br>SYNCH: SEND DLE<br>0=NORMAL<br>1=SEND DLE | 0=DISABLE<br>1=ENABLE | 0=FORCE DTR OUTPUT HIGH<br>1=FORCE DTR OUTPUT LOW | 0=DISABLE<br>1=ENABLE |

**TABLE 8—COMMAND REGISTER (CR)**

## STATUS REGISTER (SR)

The data contained in the Status Register (as shown in Table 9) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set,it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0=1) or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1. It is cleared when the status register is read by the processor. If the status register is read twice and SR2=1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received, and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the Receive Data Holding Register, when the receiver is disabled, or by a reset error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If the RHR contains all 0's when SR5=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when the Status Register is read by the processor in the synchronous mode.

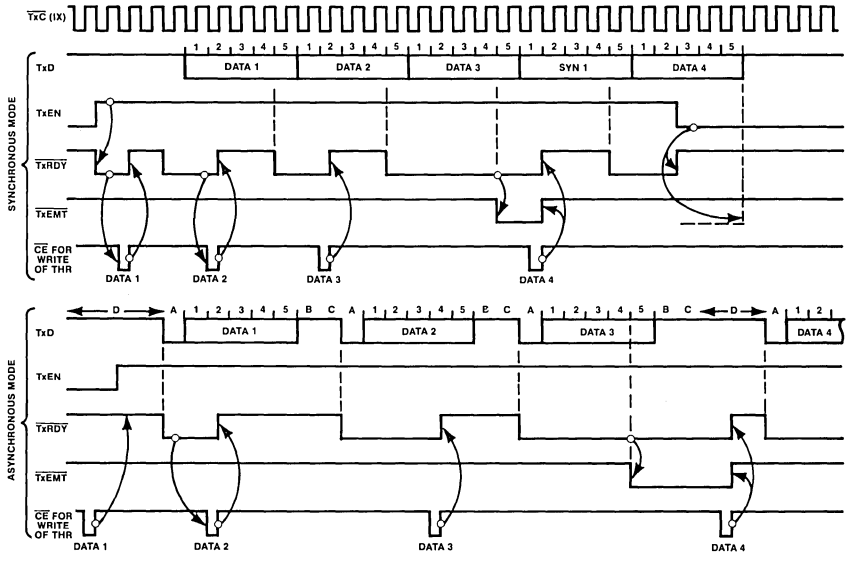
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
|---|---|---|---|---|---|---|---|
| **Data Set Ready** | **Data Carrier Detect** | **FE/SYN Detect** | **Overrun** | **PE/DLE Detect** | **TxEMT/DSCHG** | **RxRDY** | **TxRDY** |
| 0=$\overline{\text{DSR}}$ INPUT IS HIGH<br>1=$\overline{\text{DSR}}$ INPUT IS LOW | 0=$\overline{\text{DCD}}$ INPUT IS HIGH<br>1=$\overline{\text{DCD}}$ INPUT IS LOW | **ASYNCH:**<br>0=NORMAL<br>1=FRAMING ERROR<br>**SYNCH:**<br>0=NORMAL<br>1=SYN CHAR DETECTED | 0=NORMAL<br>1=OVERRUN ERROR | **ASYNCH:**<br>0=NORMAL<br>1=PARITY ERROR<br>**SYNCH:**<br>0=NORMAL<br>1=PARITY ERROR OR DLE CHAR RECEIVED | 0=NORMAL<br>1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY | 0=RECEIVE HOLDING REG EMPTY<br>1=RECEIVE HOLDING REG HAS DATA | 0=TRANSMIT HOLDING REG BUSY<br>1=TRANSMIT HOLDING REG EMPTY |

**TABLE 9—STATUS REGISTER (SR)**

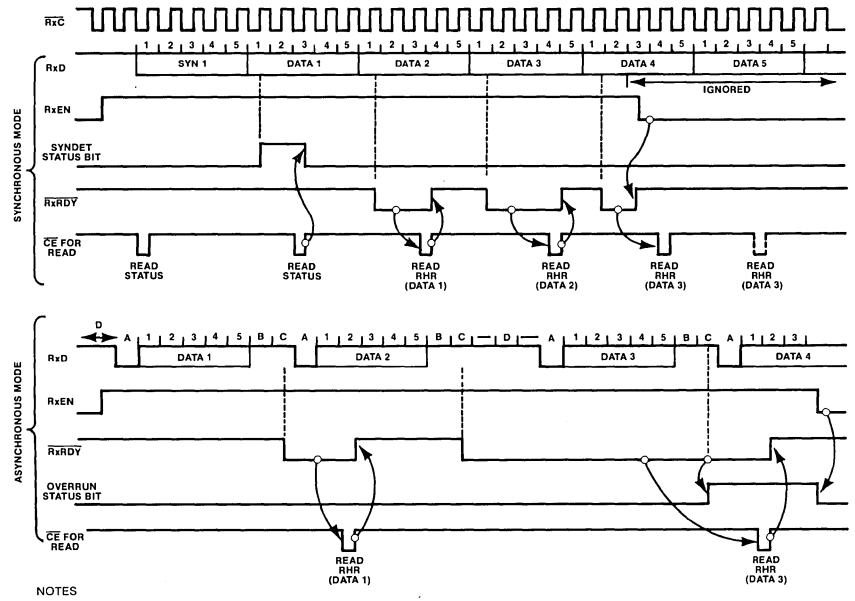
# TIMING DIAGRAMS

**TxRDY, TxEMT** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])




NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

**RxRDY** (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

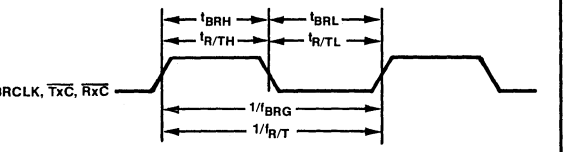



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

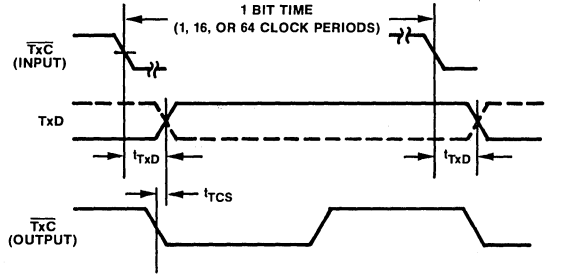
# TIMING DIAGRAMS (Cont'd)

## RESET

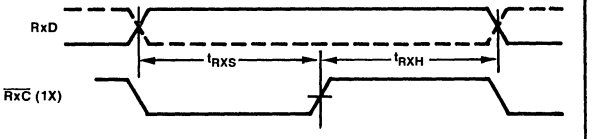

## CLOCK



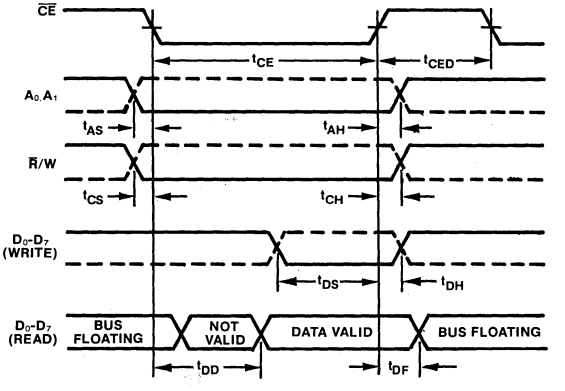

## TRANSMIT



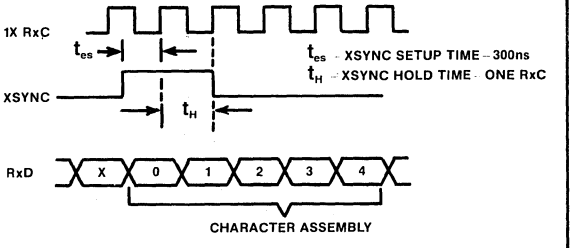

## RECEIVE



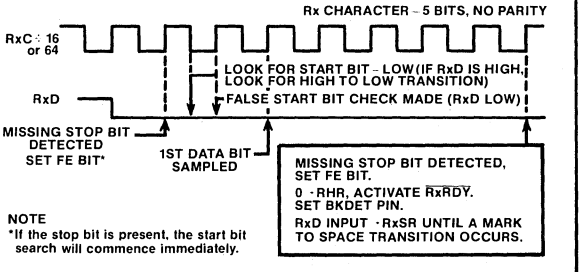

## READ AND WRITE




## EXTERNAL SYNCHRONIZATION WITH XSYNC




## BREAK DETECTION TIMING




NOTE
*If the stop bit is present, the start bit search will commence immediately.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it it important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.



## DC ELECTRICAL CHARACTERISTICS $T_A$=0°C to +70°C, $V_{CC}$=5.0V±5%

| | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | Input voltage | | | | | |
| $V_{IL}$ | Low | | | 0.8 | V | |
| $V_{IH}$ | High | 2.0 | | | | |
| | Output voltage | | | | | |
| $V_{OL}$ | Low | | | 0.4 | V | $I_{OL}$=2.2mA |
| $V_{OH}$ | High | 2.4 | | | | $I_{OH}$=−400μA |
| $I_{IL}$ | Input leakage current | | | 10 | μA | $V_{IN}$=0 to 5.5V |
| | Output leakage current | | | | | |
| $I_{LH}$ | Data bus high | | | 10 | μA | $V_O$=4.0V |
| $I_{LL}$ | Data bus low | | | 10 | μA | $V_O$=0.45V |
| $I_{CC}$ | Power supply current | | | 150 | mA | |
| | Capacitance | | | | | |
| $C_{IN}$ | Input | | | 20 | pF | fc=1MHz |
| $C_{OUT}$ | Output | | | 20 | pF | Unmeasured pins tied |
| $C_{I/O}$ | Input/Output | | | 20 | pF | to ground |

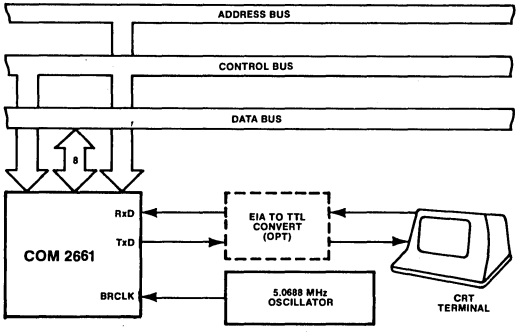
## AC ELECTRICAL CHARACTERISTICS $T_A$=0°C to +70°C, $V_{CC}$=5.0V±5%

| | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | Pulse width | | | | | |
| $t_{RES}$ | Reset | 1000 | | | ns | |
| $t_{CE}$ | Chip enable | 250 | | | ns | |
| | Setup and hold time | | | | | |
| $t_{AS}$ | Address setup | 10 | | | ns | |
| $t_{AH}$ | Address hold | 10 | | | ns | |
| $t_{CS}$ | R/W control setup | 10 | | | ns | |
| $t_{CH}$ | R/W control hold | 10 | | | ns | |
| $t_{DS}$ | Data setup for write | 150 | | | ns | |
| $t_{DH}$ | Data hold for write | 0 | | | ns | |
| $t_{RXS}$ | Rx data setup | 300 | | | ns | |
| $t_{RXH}$ | Rx data hold | 350 | | | ns | |
| $t_{DD}$ | Data delay time for read | | | 200 | ns | $C_L$=150pF |
| $t_{DF}$ | Data bus floating time for read | | | 100 | ns | $C_L$=150pF |
| $t_{CED}$ | $\overline{CE}$ to $\overline{CE}$ delay | 600 | | | ns | |
| | Input clock frequency | | | | | |
| $f_{BRG}$ | Baud rate generator (2661-1, -2) | 1.0 | 4.9152 | 4.9202 | MHz | |
| $f_{BRG}$ | Baud rate generator (2661-3) | 1.0 | 5.0688 | 5.0738 | MHz | |
| $f_{RT}$[1] | $\overline{TxC}$ or $\overline{RxC}$ | dc | | 1.0 | MHz | |
| | Clock width | | | | | |
| $t_{BRH}$ | Baud rate high (2661-1, -2) | 75 | | | ns | $f_{BRG}$=4.915MHz; measured at $V_{IH}$ |
| $t_{BRH}$ | Baud rate high (2661-3) | 70 | | | ns | $f_{BRG}$=5.0688MHz; measured at $V_{IH}$ |
| $t_{BRL}$ | Baud rate low (2661-1, -2) | 75 | | | ns | $f_{BRG}$=4.915MHz; measured at $V_{IL}$ |
| $t_{BRL}$ | Baud rate low (2661-3) | 70 | | | ns | $f_{BRG}$=5.0688MHz; measured at $V_{IL}$ |
| $t_{RTH1}$ | $\overline{TxC}$ or $\overline{RxC}$ high | 480 | | | ns | |
| $t_{RTL}$ | $\overline{TxC}$ or $\overline{RxC}$ low | 480 | | | ns | |
| $t_{TXD}$ | TxD delay from falling edge of $\overline{TxC}$ | | | 650 | ns | $C_L$=150pF |
| $t_{TCS}$ | Skew between TxD changing and falling edge of $\overline{TxC}$ output | | 0 | | ns | $C_L$=150pF |

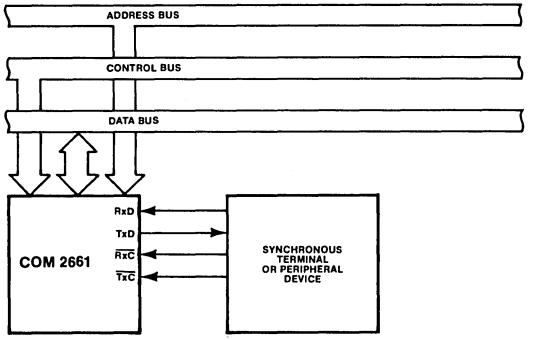
NOTE:
1. $f_{RT}$ and $t_{RTL}$ shown all modes except Local Loopback. For Local Loopback mode $f_{RT}$=0.7MHz and $t_{RTL}$=700ns min.

# TYPICAL APPLICATIONS

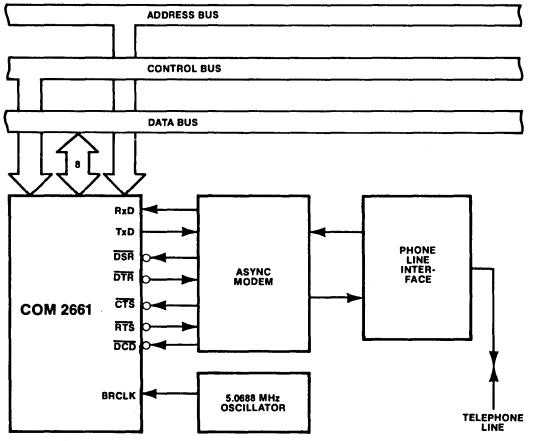
## ASYNCHRONOUS INTERFACE TO CRT TERMINAL



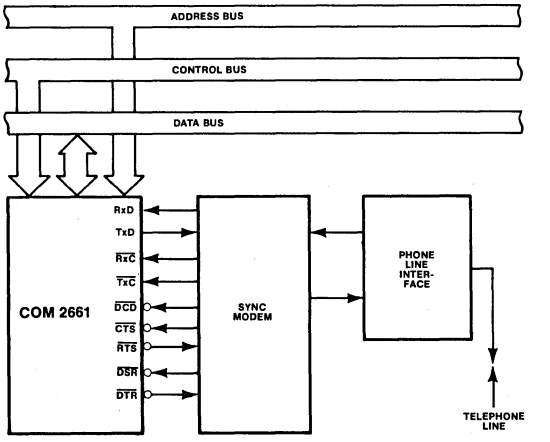

## SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE




## ASYNCHRONOUS INTERFACE TO TELEPHONE LINES




## SYNCHRONOUS INTERFACE TO TELEPHONE LINES




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**COM 5025**
**μPC FAMILY**

# Multi-Protocol Universal Synchronous Receiver/Transmitter

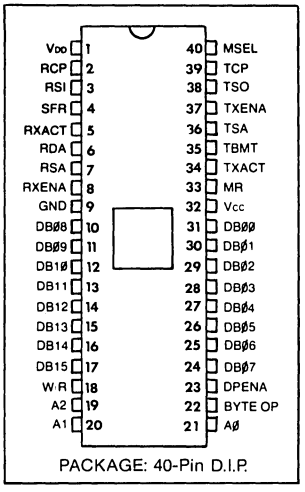
**USYNR/T**



## FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Three-state Input/Output BUS
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—1.5 M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

## PIN CONFIGURATION




PACKAGE: 40-Pin D.I.P.

**BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP**

- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

**SELECTABLE OPTIONS:**

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

**BYTE ORIENTED PROTOCOLS—BiSync, DDCMP**

- ☐ Automatic detection and generation of SYNC characters

**SELECTABLE OPTIONS:**

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

## APPLICATIONS

- ☐ Intelligent Terminals
- ☐ Line Controllers
- ☐ Network Processors
- ☐ Front End Communications
- ☐ Remote Data Concentractors
- ☐ Communication Test Equipment
- ☐ Computer to Computer Links
- ☐ Hard Disk Data Handler

## General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

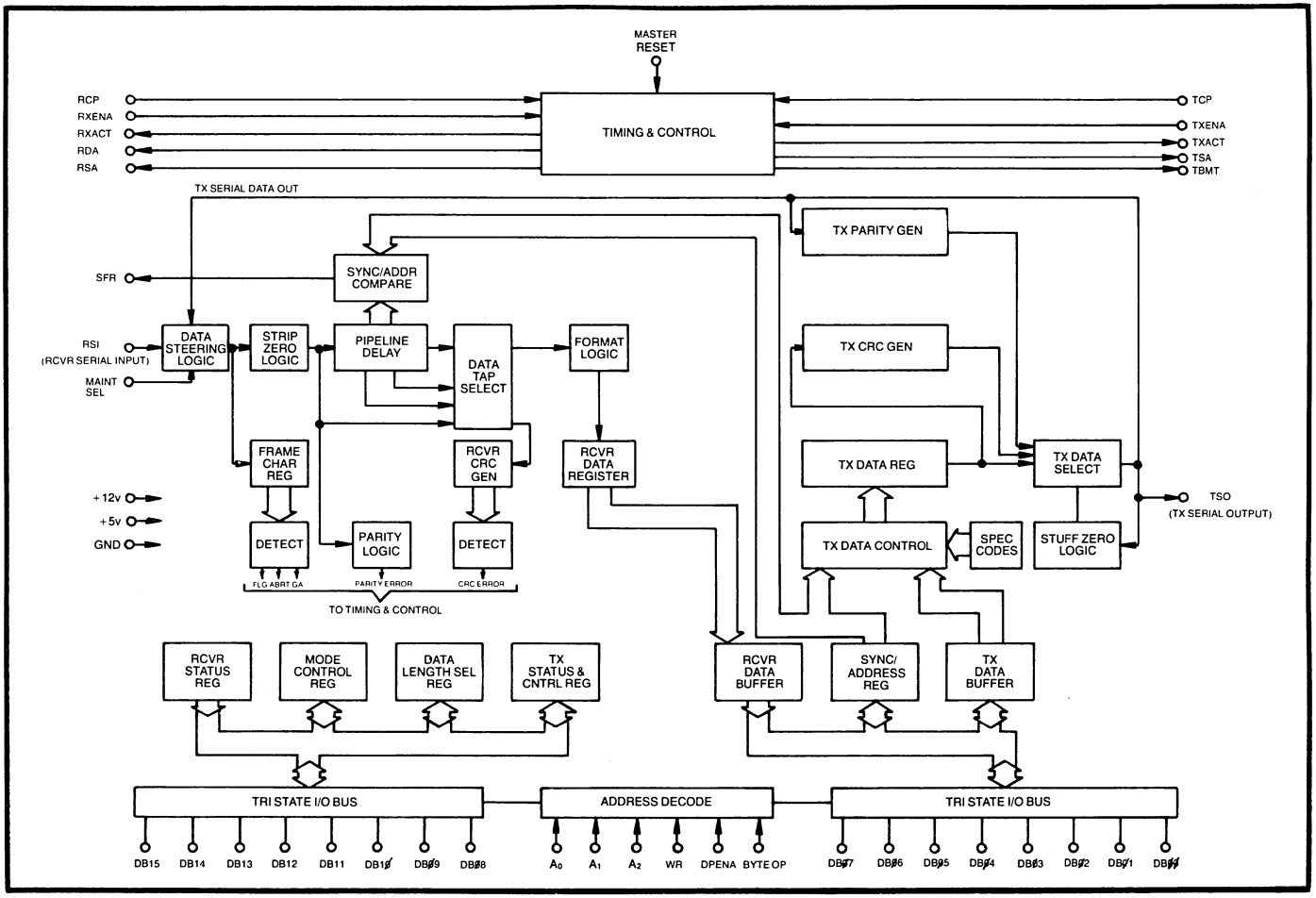
## References:


1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044


# Terminology

| Term | Definition | Term | Definition |
|---|---|---|---|
| BOP | Bit Oriented Protocols: SDLC, HDLC, ADCCP | GA | 01111111 (0 (LSB) followed by 7-1's) |
| CCP | Control Character Protocols: BiSync, DDCMP | LSB | First transmitted bit, First received bit |
| TDB | Transmitter Data Buffer | MSB | Last transmitted bit, Last received bit |
| RDB | Receiver Data Buffer | RDP | Receiver Data Path |
| TDSR | Transmitter Data Shift Register | TDP | Transmitter Data Path |
| FLAG | 01111110 | LM | Loop Mode |
| ABORT | 11111111 (7 or more contiguous 1's) | | |

## BLOCK DIAGRAM



# Description of Pin Functions

| Pin No. | Symbol | Name | I/O | Function |
|---|---|---|---|---|
| 1 | $V_{DD}$ | Power Supply | PS | +12 volt Power Supply. |
| 2 | RCP | Receiver Clock | I | The positive-going edge of this clock shifts data into the receiver shift register. |
| 3 | RSI | Receiver Serial Input | I | This input accepts the serial bit input stream. |
| 4 | SFR | Sync/Flag Received | O | This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received. |
| 5 | RXACT | Receiver Active | O | This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA. |
| 6 | RDA | Receiver Data Available | O | This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB. |
| 7 | RSA | Receiver Status Available | O | This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA. |
| 8 | RXENA | Receiver Enable | I | A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT. |
| 9 | GND | Ground | GND | Ground |
| 10 | DBØ8 | Data Bus | I/O | Bidirectional Data Bus. |
| 11 | DBØ9 | Data Bus | I/O | Bidirectional Data Bus. |
| 12 | DB1Ø | Data Bus | I/O | Bidirectional Data Bus. |
| 13 | DB11 | Data Bus | I/O | Bidirectional Data Bus. |
| 14 | DB12 | Data Bus | I/O | Bidirectional Data Bus. |
| 15 | DB13 | Data Bus | I/O | Bidirectional Data Bus. |
| 16 | DB14 | Data Bus | I/O | Bidirectional Data Bus. |
| 17 | DB15 | Data Bus | I/O | Bidirectional Data Bus. |
| | | | | Wire "OR" with DBØØ-DBØ7 For 8 bit data bus |
| 18 | W/R | Write/Read | I | Controls direction of data port. W/R=1, Write. W/R=0, Read. |
| 19 | A2 | Address 2 | I | Address input—MSB. |
| 20 | A1 | Address 1 | I | Address input. |
| 21 | AØ | Address 0 | I | Address input—LSB. |
| 22 | BYTE OP | Byte Operation | I | If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide. |
| 23 | DPENA | Data Port Enable | I | Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT. |
| 24 | DBØ7 | Data Bus | I/O | Bidirectional Data Bus—MSB. |
| 25 | DBØ6 | Data Bus | I/O | Bidirectional Data Bus. |
| 26 | DBØ5 | Data Bus | I/O | Bidirectional Data Bus. |
| 27 | DBØ4 | Data Bus | I/O | Bidirectional Data Bus. |
| 28 | DBØ3 | Data Bus | I/O | Bidirectional Data Bus. |
| 29 | DBØ2 | Data Bus | I/O | Bidirectional Data Bus. |
| 30 | DBØ1 | Data Bus | I/O | Bidirectional Data Bus. |
| 31 | DBØØ | Data Bus | I/O | Bidirectional Data Bus—LSB. |
| 32 | $V_{CC}$ | Power Supply | PS | +5 volt Power Supply. |
| 33 | MR | Master Reset | I | This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's. |
| 34 | TXACT | Transmitter Active | O | This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped. |
| 35 | TBMT | Transmitter Buffer Empty | O | This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded. |
| 36 | TSA | Transmitter Status Available | O | TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM. |
| 37 | TXENA | Transmitter Enable | I | A high level input allows the processing of transmitter data. |
| 38 | TSO | Transmitter Serial Output | O | This output is the transmitted character. |
| 39 | TCP | Transmitter Clock | I | The positive going edge of this clock shifts data out of the transmitter shift register. |
| 40 | MSEL | Maintenance Select | I | Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO=1. |

# Definition of Terms
## Register Bit Assignment Chart 1 and 2



| Data Bu | Term | Definition | |
|---|---|---|---|
| DBØ8 | RSOM | Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB. | Receiver Status Register |
| DBØ9 | REOM | Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA. | |
| DB1Ø | RAB/GA | Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA. | |
| DB11 | ROR | Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA. | |
| DB12-14 | A, B, C | Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified). | |
| DB15 | ERR CHK | Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message. | |
| DB8 | TSOM | Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG. | Transmitter Status and Control Register |
| DB9 | TEOM | Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line. | |
| DB1Ø | TXAB | Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG. | |
| DB11 | TXGA | Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character. | |
| DB15 | TERR | Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM. | |
| DB8-1Ø | X, Y, Z | Z Y X —W/R bits. These are the error control bits.<br>0 0 0 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "1"<br>0 0 1 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "0"<br>0 1 0 Not used<br>0 1 1 $X^{16}+X^{15}+X^2+1$—CRC16<br>1 0 0 Odd Parity—CCP Only<br>1 0 1 Even Parity—CCP Only<br>1 1 0 Not Used<br>1 1 1 Inhibit all error detection and transmission<br>Note: Do not modify XYZ until both data paths are idle | Mode Control Register |
| DB11 | IDLE | IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register. | |
| DB12 | SEC ADD | Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1. | |
| DB13 | STRIP SYNC/LOOP | Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. | |
| DB14 | PROTOCOL | PROTOCOL—W/R bit. BOP=0, CCP=1 | |
| DB15 | *APA | All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. | |
| DB13-15 | TXDL | Transmitter Data Length—W/R bits.<br>TXDL3 TXDL2 TXDL1 LENGTH<br>0 0 0 Eight bits per character<br>1 1 1 Seven bits per character<br>1 1 0 Six bits per character<br>1 0 1 Five bits per character<br>1 0 0 Four bits per character*<br>0 1 1 Three bits per character*<br>0 1 0 Two bits per character*<br>0 0 1 One bit per character*<br>*For data length only, not to be used for SYNC character (CCP mode). | Data Length Select Register |
| DB8-1Ø | RXDL | Receiver Data Length—W/R bits.<br>RXDL3 RXDL2 RXDL1 LENGTH<br>0 0 0 Eight bits per character<br>1 1 1 Seven bits per character<br>1 1 0 Six bits per character<br>1 0 1 Five bits per character<br>1 0 0 Four bits per character<br>0 1 1 Three bits per character<br>0 1 0 Two bits per character<br>0 0 1 One bit per character | |
| DB11 | EXCON | Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1. | |
| DB12 | EXADD | Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1. | |

*Note: Product manufactured before 1Q79 may not have this feature.

# Register Bit Assignment Chart 1

| REGISTER | DPØ7 | DPØ6 | DPØ5 | DPØ4 | DPØ3 | DPØ2 | DPØ1 | DPØØ |
|---|---|---|---|---|---|---|---|---|
| Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0) | RD7 MSB | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RDØ LSB |
| Transmitter Data Register (Read/Write- Unused Inputs=X) | TD7 MSB | TD6 | TD5 | TD4 | TD3 | TD2 | TD1 | TDØ LSB |
| Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X) | SSA7 MSB | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSAØ LSB |

# Register Bit Assignment Chart 2

| REGISTER | DP15 | DP14 | DP13 | DP12 | DP11 | DP1Ø | DPØ9 | DPØ8 |
|---|---|---|---|---|---|---|---|---|
| Receiver Status (Read Only) | ERR CHK | C | B | A | ROR | RAB/GA | REOM | RSOM |
| TX Status and Control (Read/Write) | TERR (Read Only) | 0 | 0 | 0 | TXGA | TXAB | TEOM | TSOM |
| Mode Control (Read/Write) | *APA | PROTOCOL | STRIP SYNC/ LOOP | SEC ADD | IDLE | Z | Y | X |
| Data Length Select (Read/Write) | TXDL3 | TXDL2 | TXDL1 | EXADD | EXCON | RXDL3 | RXDL2 | RXDL1 |

* Note: Product manufactured before 1Q79 may not have this feature.

# Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

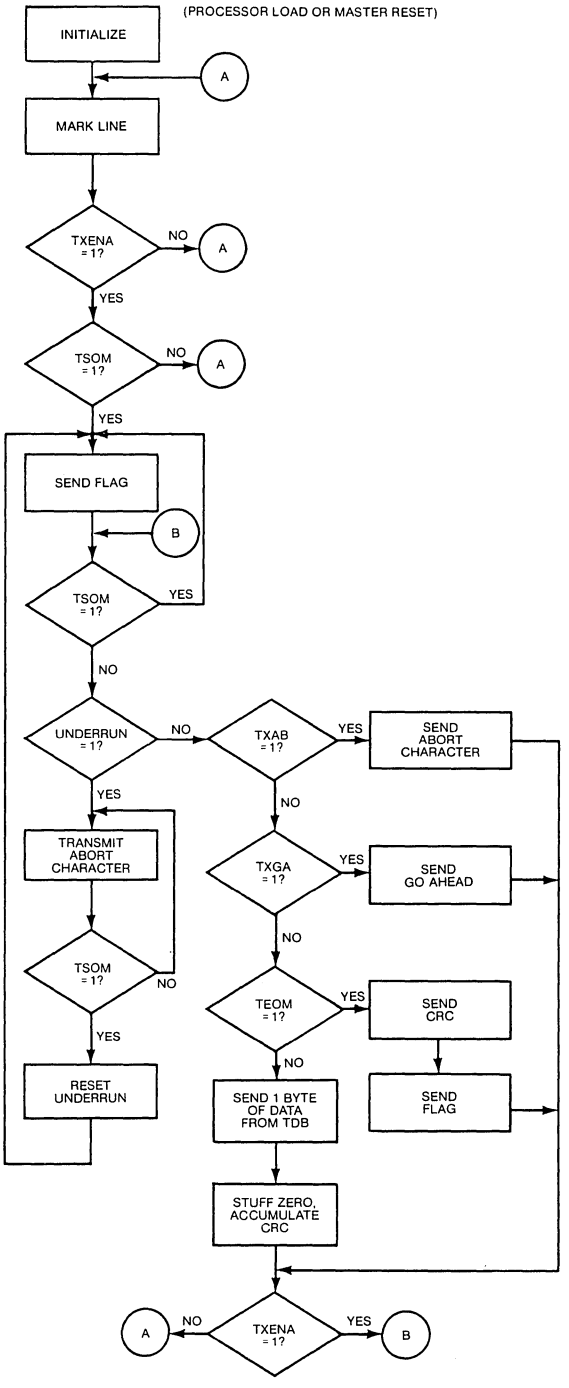
| A2 | A1 | AØ | Register |
|---|---|---|---|
| 0 | 0 | X | Receiver Status Register and Receiver Data Buffer |
| 0 | 1 | X | Transmitter Status and Control Register and Transmitter Data Buffer |
| 1 | 0 | X | Mode Control Register and SYNC/Address Register |
| 1 | 1 | X | Data Length Select Register |

X = don't care

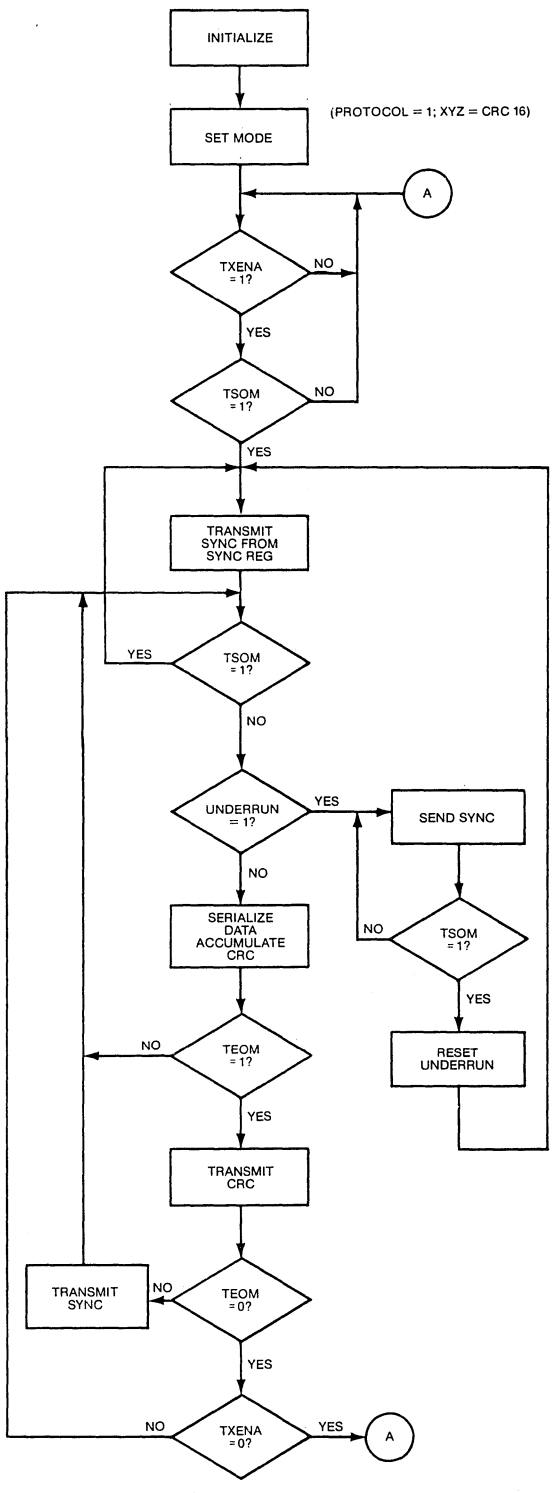
2) BYTE OP = 1, data port 8 bits wide

| A2 | A1 | AØ | Register |
|---|---|---|---|
| 0 | 0 | 0 | Receiver Data Buffer |
| 0 | 0 | 1 | Receiver Status Register |
| 0 | 1 | 0 | Transmitter Data Buffer |
| 0 | 1 | 1 | Transmitter Status and Control Register |
| 1 | 0 | 0 | SYNC/Address Register |
| 1 | 0 | 1 | Mode Control Register |
| 1 | 1 | 0 | ——— |
| 1 | 1 | 1 | Data Length Select Register |

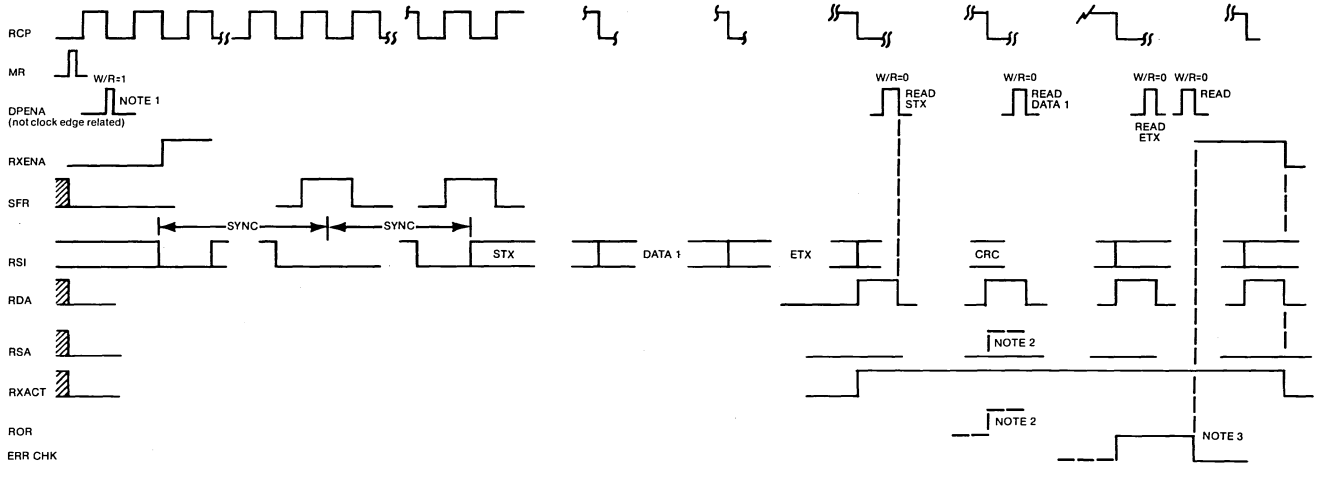
## BOP TRANSMITTER OPERATION




## CCP TRANSMITTER OPERATION

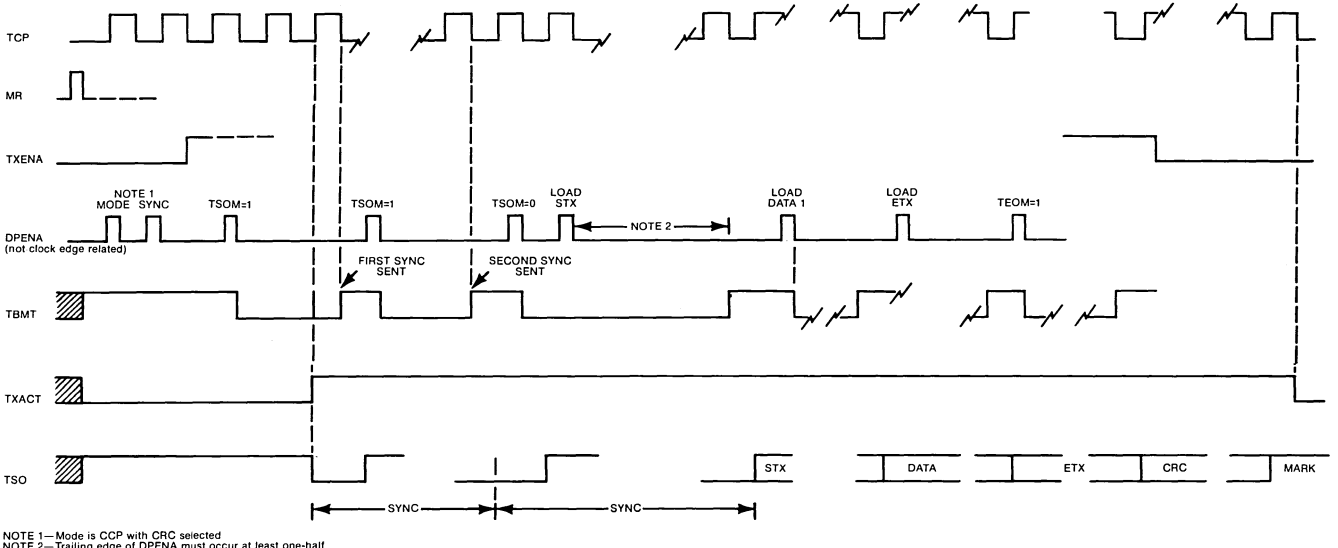


## CCP RECEIVER TIMING



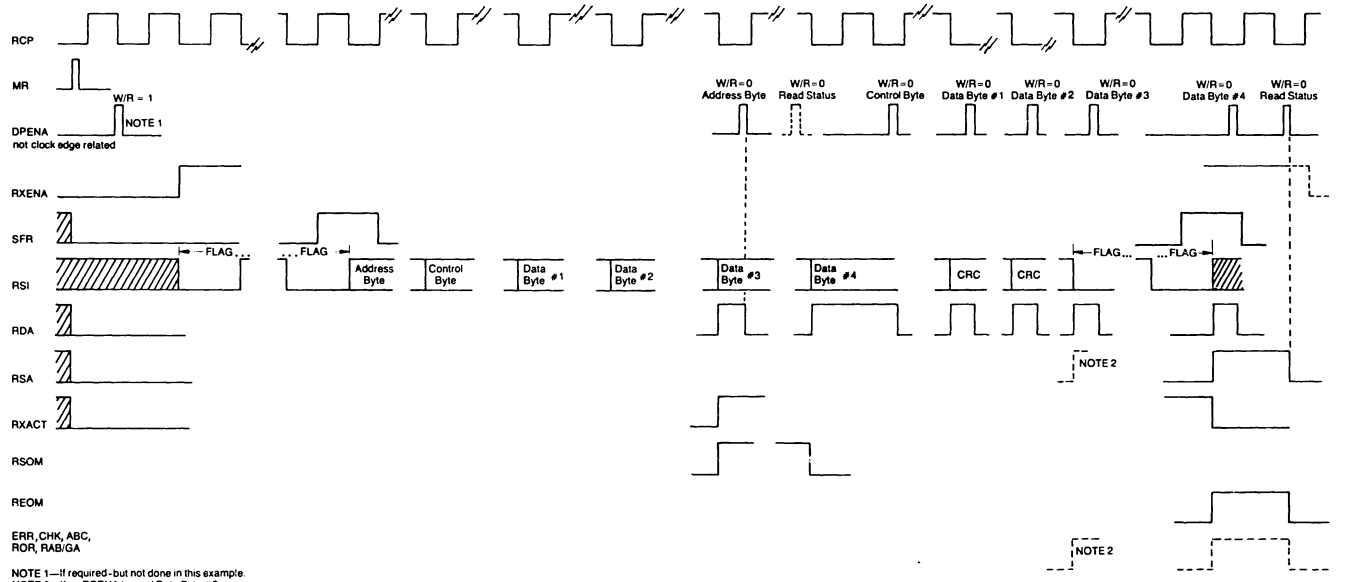

NOTE 1—Mode set for CCP with CRC selected
NOTE 2—If overrun had occured—no READ STX
NOTE 3—ERR CHK must be sampled before next byte or before RXENA brought low

## CCP TRANSMITTER OPERATION



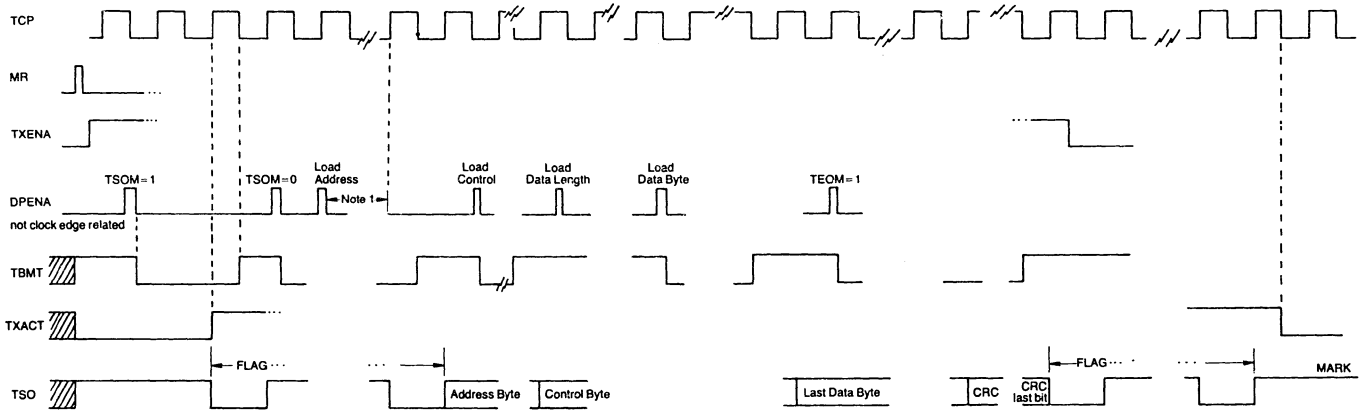

NOTE 1—Mode is CCP with CRC selected
NOTE 2—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1 to avoid underrun

## BOP RECEIVER TIMING



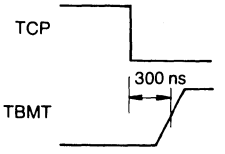

NOTE 1—If required - but not done in this example.
NOTE 2—If no DPENA to read Data Byte #2.

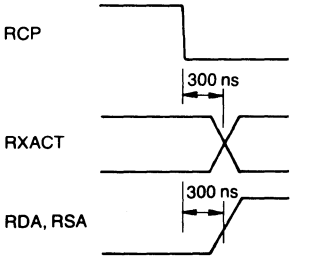
## BOP TRANSMITTER OPERATION

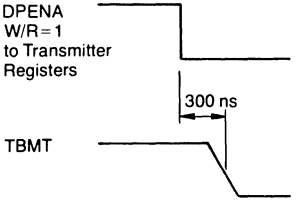


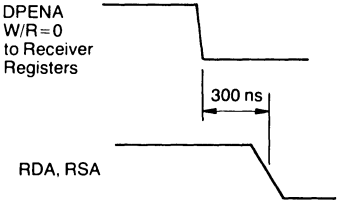

Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT = 1. To avoid underrun.

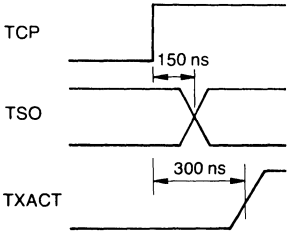
# AC TIMING DIAGRAMS

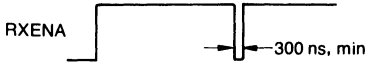


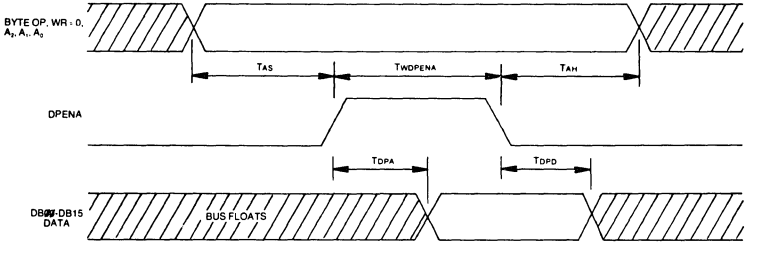



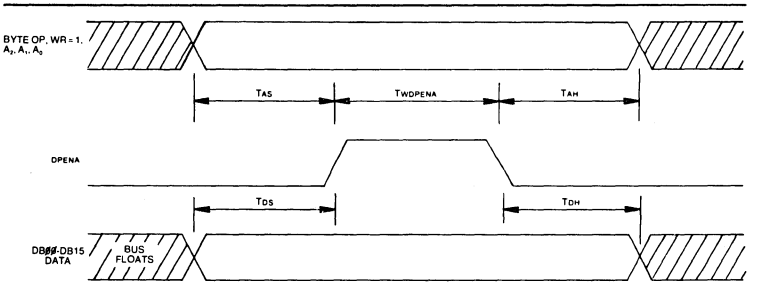

Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

Note: Unless otherwise specified all times are maximum.

## Data Port Timing




**READ FROM USYNR/T**




**WRITE TO USYNR/T**

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

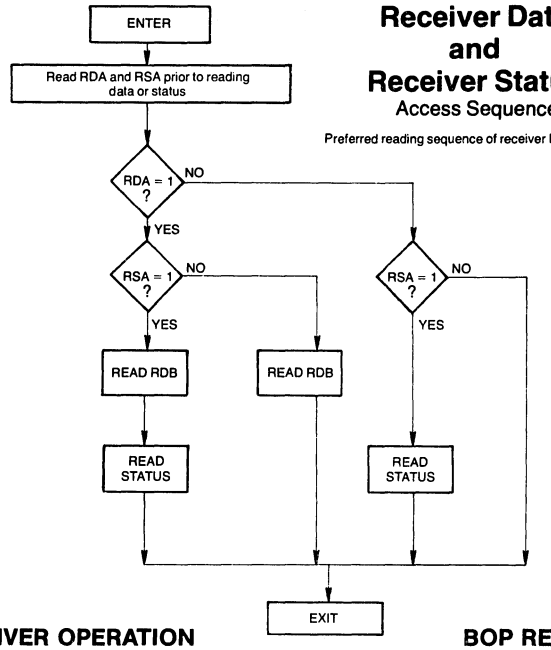


**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, $V_{DD}$=+12V±5%, unless otherwise noted)

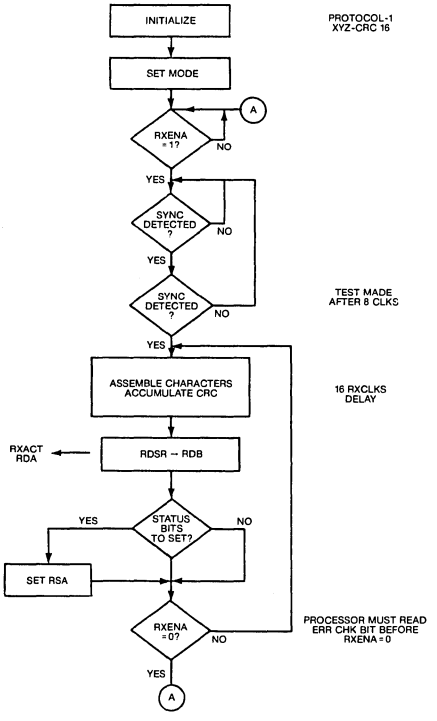
| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. Characteristics** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{IL}$ | | | 0.8 | V | |
| High Level, $V_{IH}$ | 2.0 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=1.6ma |
| High Level, $V_{OH}$ | 2.4 | | | | $I_{OH}$=40μa |
| INPUT LEAKAGE | | | | | |
| Data Bus | | 5.0 | 50.0 | μa | 0≤$V_{IN}$≤5v, DPENA=0 or W/R=I |
| All others | | | | μa | $V_{IN}$=+5v |
| INPUT CAPACITANCE | | | | | |
| Data Bus, $C_{IN}$ | | | | pf | |
| Address Bus, $C_{IN}$ | | | | pf | |
| Clock, $C_{IN}$ | | | | pf | |
| All other, $C_{IN}$ | | | | pf | |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 70 | ma | |
| $I_{DD}$ | | | 90 | ma | |
| **A.C. Characteristics** | | | | | $T_A$=25°C |
| CLOCK-RCP, TCP | | | | | |
| frequency | DC | | 1.5 | MHz | |
| $PW_H$ | 325 | | | ns | |
| $PW_L$ | 325 | | | ns | |
| $t_r$, $t_f$ | | 10 | | ns | |
| DPENA, $T_{WDPENA}$ | 250 | | 50 μs | ns | |
| Set-up Time, $T_{AS}$ | 0 | | | ns | |
| Byte Op, W/R | | | | | |
| $A_2$, $A_1$, $A_0$ | | | | | |
| Hold Time, $T_{AH}$ | 0 | | | ns | |
| Byte Op, WIR, | | | | | |
| $A_2$, $A_1$, $A_0$ | | | | | |
| DATA BUS ACCESS, $T_{DPA}$ | | | 150 | ns | |
| DATA BUS DISABLE DELAY, $T_{DPD}$ | | | 100 | ns | |
| DATA BUS SET-UP TIME, $T_{DBS}$ | 0 | | | ns | |
| DATA BUS HOLD TIME, $T_{DBH}$ | 100 | | | ns | |
| MASTER RESET, MR | 350 | | | ns | |

# Receiver Data and Receiver Status Access Sequence

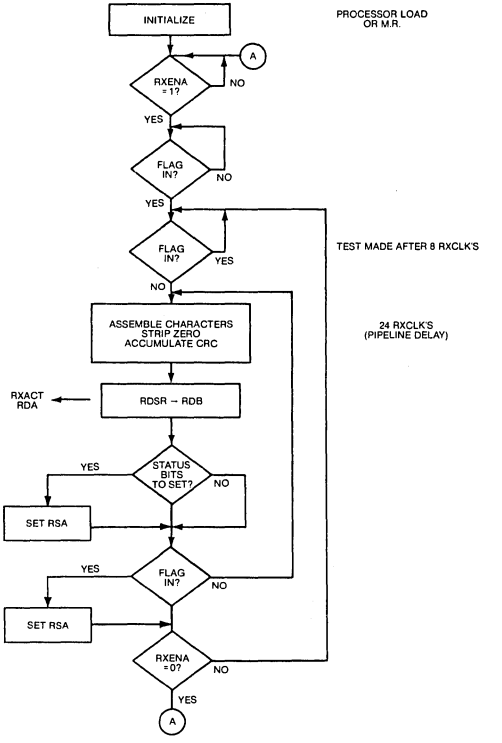
Preferred reading sequence of receiver RDA and RSA.




## CCP RECEIVER OPERATION




## BOP RECEIVER OPERATION




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM52C50

**PRELIMINARY**

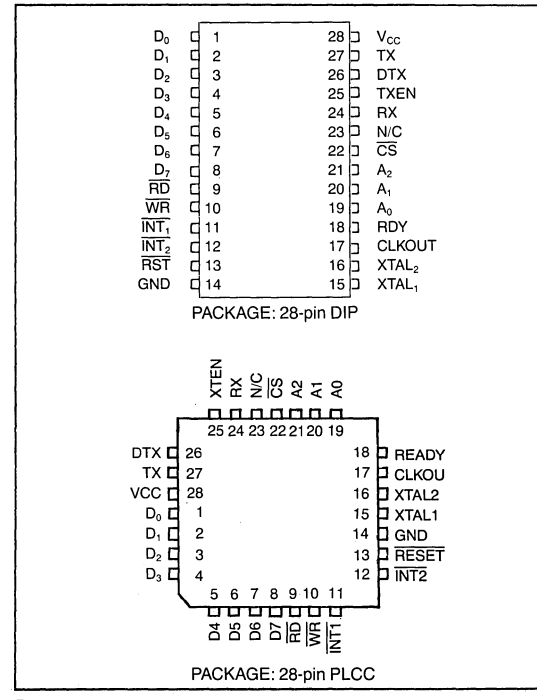
# Twinax Interface Circuit (TIC)

SECTION III

## FEATURES

- ☐ Conforms to IBM 5250 System Standard
- ☐ Operates at 1Mbps Data Rate
- ☐ Transmits and Receives Manchester II Encoded Data
- ☐ On Chip Parity Generation and Checking
- ☐ Programmable Interframe Zero Bit Insertion
- ☐ Handles Multi Byte and Single Byte Transfers
- ☐ Multiple Address Select Register Allows for Up to 7 Mode Address Emulation
- ☐ Master Mode Permits Message Initiation
- ☐ Internal/External Loopback Capability for Self Test Diagnostics
- ☐ Low Power Cmos
- ☐ 28 Pin Plastic Dual In Line and Chip Carrier Packages
- ☐ Open Drain Output on Interrupt Pins
- ☐ On Board Predistortion Circuitry
- ☐ On Board Crystal Oscillator (8MHz) Simplifies Clock Generation
- ☐ TTL Compatible Inputs and Output
- ☐ Single +5v Supply

## PIN CONFIGURATION



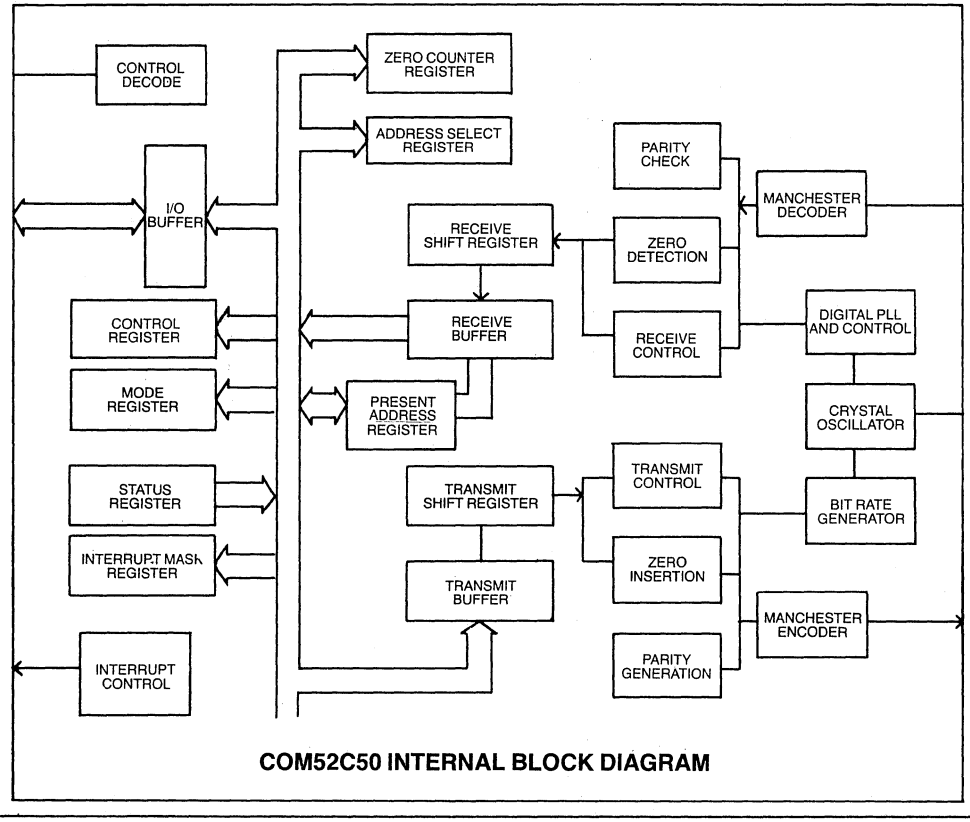

PACKAGE: 28-pin DIP

PACKAGE: 28-pin PLCC

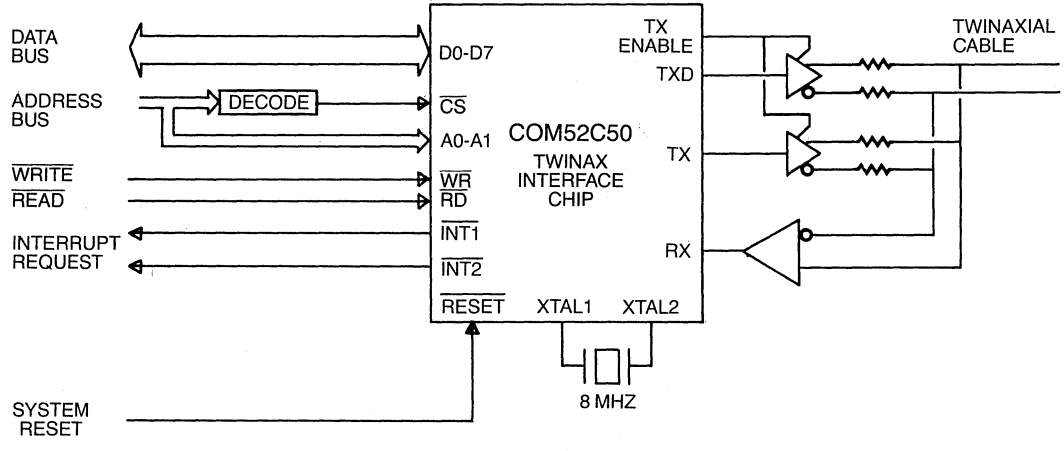
Pin configuration subject to change, contact factory for details.

## GENERAL DESCRIPTION

The COM52C50 is a CMOS device that performs the communications interface to the IBM 5250 TWINAXIAL bus. It interfaces to a general purpose microprocessor on one side and to the IBM 5250 TWINAXIAL bus on the other side. The COM52C50 handles the parallel to serial and serial to parallel conversion of data to and from the TWINAXIAL bus and the encoding and decoding of data in Manchester II format. The COM52C50 consists of a RECEIVE BLOCK, a TRANSMIT BLOCK, and CONTROL circuitry. The receive and transmit sections of the COM52C50 are separate and may be used independent of one another. The COM52C50 generates and detects the bit sync, parity, and the fill zero bit patterns according to the IBM 5250 standard.




**COM52C50 INTERNAL BLOCK DIAGRAM**




**TYPICAL COM52C50 INTERFACE**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 · TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

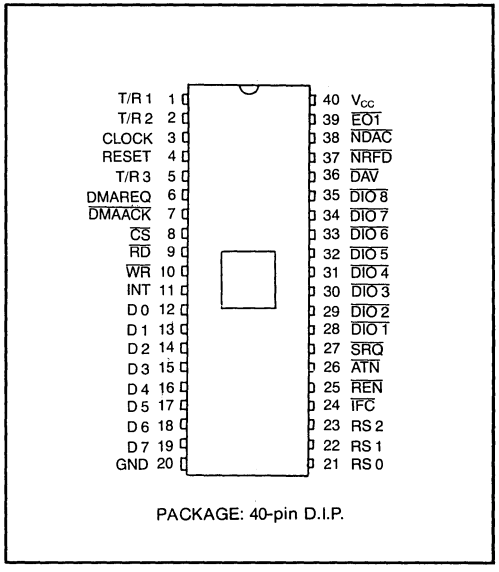
# Intelligent GPIB Interface Controller



## FEATURES

- ☐ All Functional Interface Capability Meeting IEEE Standard 488-1978
  - —SH1 (Source Handshake)
  - —AH1 (Acceptor Handshake)
  - —T5 or TE5 (Talker or Extended Talker)
  - —L3 or LE3 (Listener or Extended Listener)
  - —SR1 (Service Request)
  - —RL1 (Remote Local)
  - —PP1 or PP2 (Parallel Poll) (Remote or Local Configuration)
  - —DC1 (Device Clear)
  - —DT1 (Device Trigger)
  - —C1-5 ((Controller) (All Functions))
- ☐ Programmable Data Transfer Rate
- ☐ 16 MPU Accessible Registers—8 Read/8 Write
- ☐ 2 Address Registers
  - —Detection of MTA, MLA, MSA (My Talk/Listen/ Secondary Address)
  - —2 Device Addresses
- ☐ EOS Message Automatic Detection
- ☐ Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- ☐ DMA Capability
- ☐ Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- ☐ 1 to 8 MHz Clock Range
- ☐ TTL Compatible

## PIN CONFIGURATION

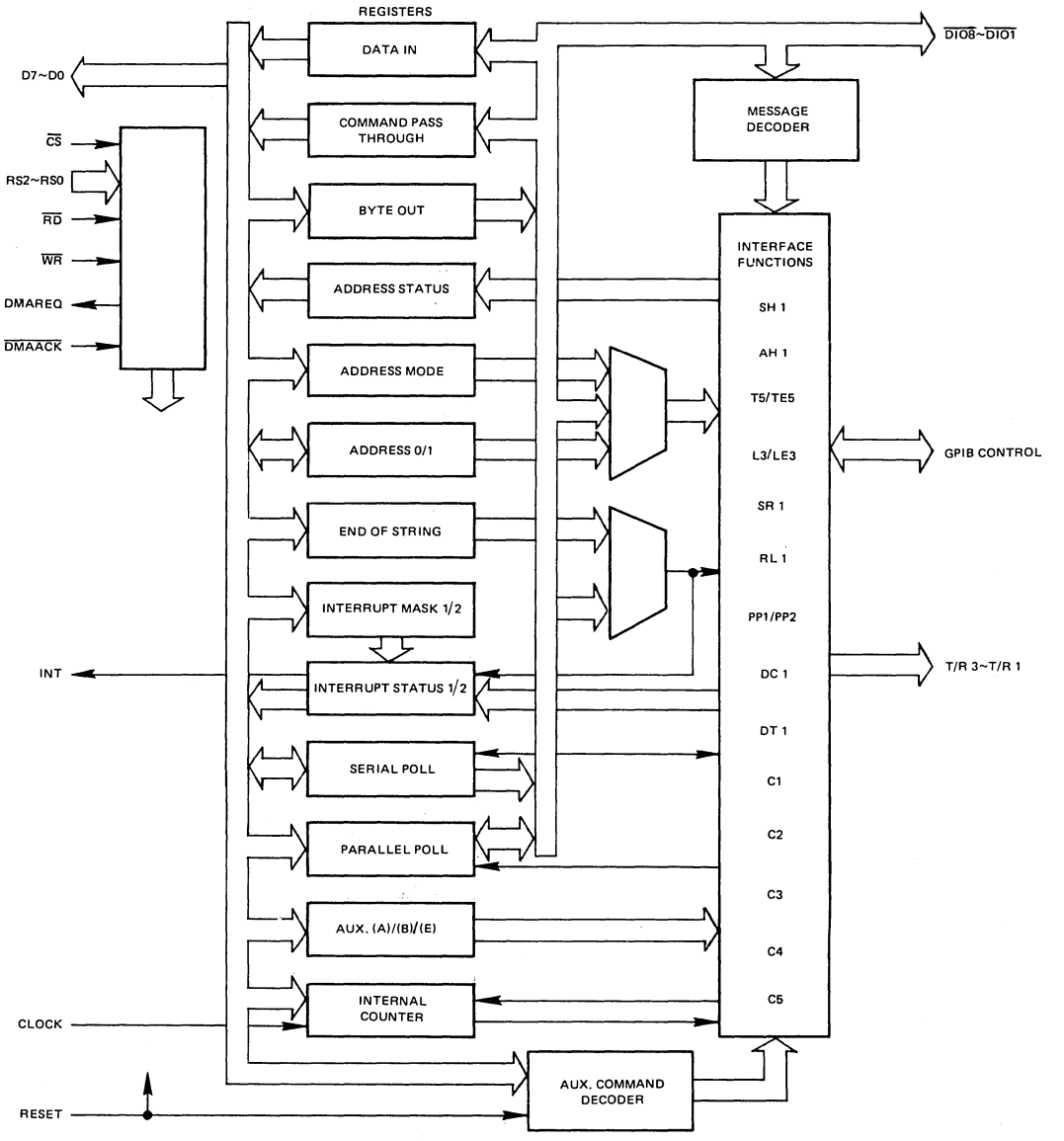



PACKAGE: 40-pin D.I.P.

- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ +5V Single Power Supply
- ☐ 40-Pin DIP
- ☐ 8080/85/86 Compatible

## GENERAL DESCRIPTION

The COM7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.




**BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | T/R1 | O | Transmit/Receive Control—Input/Output Control Signal for the GPIB Bus Transceivers. |
| 2 | T/R2 | O | Transmit/Receive Control—The functions of T/R2, T/R3 are determined by the values of TRM1, TRM0 of the address mode register. |
| 3 | CLK | I | Clock—(1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978. |
| 4 | RST | I | Reset—Resets 7210 to an idle state when high (active high). |
| 5 | T/R3 | O | Transmit/Receive Control—Function determined by TRM1 and TRM0 of address mode register (See T/R2). |
| 6 | DMAREQ | O | DMA Request—7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal DACK. |
| 7 | $\overline{DMAACK}$ | I | DMA Acknowledge—(Active Low) Signal connects the computer system data bus to the data register of the 7210. |
| 8 | $\overline{CS}$ | I | Chip Select—(Active Low) Enables access to the register selected by RS0-2 (read or write operation). |
| 9 | $\overline{RD}$ | I | Read—(Active Low) Places contents of read register specified by RS0-2—on D0-7 (Computer Bus). |
| 10 | $\overline{WR}$ | I | Write—(Active Low) writes data on D0-7 into the write register specified by RS0-2. |
| 11 | INT / $\overline{INT}$ | O | Interrupt Request—(Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset. |
| 12-19 | D0-7 | I/O | Data Bus—8-bit bidirectional data bus, for interface to computer system. |
| 20 | GND | | Ground. |
| 21-23 | RS0-2 | I | Register Select—These lines select one of eight read (write) registers during a read (write) operation. |
| 24 | $\overline{IFC}$ | I/O | Interface Clear—Control line used for clearing the interface functions. |
| 25 | $\overline{REN}$ | I/O | Remote Enable—Control line used to select remote or local control of the devices. |
| 26 | $\overline{ATN}$ | I/O | Attention—Control line which indicates whether data on DIO lines is an interface message or device dependent message. |
| 27 | $\overline{SRQ}$ | I/O | Service Request—Control line used to request the controller for service. |
| 28-35 | $\overline{DIO1\text{-}8}$ | I/O | Data Input/Output—8-bit bidirectional bus for transfer of message on the GPIB. |
| 36 | $\overline{DAV}$ | I/O | Data Valid—Handshake line indicating that data on DIO lines is valid. |
| 37 | $\overline{NRFD}$ | I/O | Ready for Data—Handshake line indicating that device is ready for data. |
| 38 | $\overline{NDAC}$ | I/O | Data Accepted—Handshake line indicating completion of message reception. |
| 39 | $\overline{EOI}$ | I/O | End or Identify—Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN. |
| 40 | $V_{CC}$ | | +5V DC |

## FUNCTIONAL DESCRIPTION

### Introduction

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The COM7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101-D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The COM7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

The COM7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor

overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

## Internal Registers

The TLC has 16 registers, 8 of which are read and 8 write.

| REGISTER NAME | ADDRESSING | | | | | | SPECIFICATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS2 | RS1 | RS0 | $\overline{WR}$ | $\overline{RD}$ | $\overline{CS}$ | | | | | | | | |
| Data In (0R) | 0 | 0 | 0 | 1 | 0 | 0 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 |
| Interrupt Status 1 (1R) | 0 | 0 | 1 | 1 | 0 | 0 | CPT | APT | DET | END | DEC | ERR | D0 | D1 |
| Interrupt Status 2 (2R) | 0 | 1 | 0 | 1 | 0 | 0 | INT | SRQ1 | LOK | REM | CO | LOKC | REMC | ADSC |
| Serial Poll Status (3R) | 0 | 1 | 1 | 1 | 0 | 0 | S8 | PEND | S6 | S5 | S4 | S3 | S2 | S1 |
| Address Status (4R) | 1 | 0 | 0 | 1 | 0 | 0 | CIC | $\overline{ATN}$ | SPMS | LPAS | TPAS | LA | TA | MJMN |
| Command Pass Through (5R) | 1 | 0 | 1 | 1 | 0 | 0 | CPT7 | CPT6 | CPT5 | CPT4 | CPT3 | CPT2 | CPT1 | CPT0 |
| Address 0 (6R) | 1 | 1 | 0 | 1 | 0 | 0 | X | DT0 | DL0 | AD5-0 | AD4-0 | AD3-0 | AD2-0 | AD1-0 |
| Address 1 (7R) | 1 | 1 | 1 | 1 | 0 | 0 | EO1 | DT1 | DL1 | AD5-1 | AD4-1 | AD3-1 | AD2-1 | AD1-1 |
| Byte Out (0W) | 0 | 0 | 0 | 0 | 1 | 0 | BO7 | BO6 | BO5 | BO4 | BO3 | BO2 | BO1 | BO0 |
| Interrupt Mask 1 (1W) | 0 | 0 | 1 | 0 | 1 | 0 | CPT | APT | DET | END | DEC | ERR | DO | DI |
| Interrupt Mask 2 (2W) | 0 | 1 | 0 | 0 | 1 | 0 | 0 | SRQI | DMAO | DMAI | CO | LOKC | REMC | ADSC |
| Serial Poll Mode (3W) | 0 | 1 | 1 | 0 | 1 | 0 | S8 | rsv | S6 | S5 | S4 | S3 | S2 | S1 |
| Address Mode (4W) | 1 | 0 | 0 | 0 | 1 | 0 | ton | lon | TRM1 | TRM0 | 0 | 0 | ADM1 | ADM0 |
| Auxiliary Mode (5W) | 1 | 0 | 1 | 0 | 1 | 0 | CNT2 | CNT1 | CNT0 | COM4 | COM3 | COM2 | COM1 | COM0 |
| Address 0/1 (6W) | 1 | 1 | 0 | 0 | 1 | 0 | ARS | DT | DL | AD5 | AD4 | AD3 | AD2 | AD1 |
| End of String (7W) | 1 | 1 | 1 | 0 | 1 | 0 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |

## Data Registers

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

| DATA IN (0R) | DI7 | DI6 | DI5 | DI4 | DI3 | DI2 | DI1 | DI0 |
|---|---|---|---|---|---|---|---|---|

Holds data sent from the GPIB to the computer

| BYTE OUT (0W) | BO7 | BO6 | BO5 | BO4 | BO3 | BO2 | BO1 | BO0 |
|---|---|---|---|---|---|---|---|---|

Holds information written into it for transfer to the GPIB

## Interrupt Registers

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related bits.

**READ**

| INTERRUPT STATUS 1 (1R). | CPT | APT | DET | END | DEC | ERR | DO | DI |
|---|---|---|---|---|---|---|---|---|
| INTERRUPT STATUS 2 (2R) | INT | SRQI | LOK | REM | CO | LOKC | REMC | ADSC |

**WRITE**

| INTERRUPT MASK 1 (1W) | CPT | APT | DET | END | DEC | ERR | DO | DI |
|---|---|---|---|---|---|---|---|---|
| INTERRUPT MASK 2 (2W) | 0 | SRQI | DMAO | DMAI | CO | LOKC | REMC | ADSC |

**Interrupt Status Bits**

| | |
|---|---|
| INT | OR of All Unmasked Interrupt Status Bits |
| CPT | Command Pass Through |
| APT | Address Pass Through |
| DET | Device Trigger |
| END | End (END or EOS Message Received) |
| DEC | Device Clear |
| ERR | Error |
| DO | Data Out |
| DI | Data In |
| SRQI | Service Request Input |
| LOKC | Lockout Change |
| REMC | Remote Change |
| ADSC | Address Status Change |
| CO | Command Output |

There are thirteen factors which can generate an interrupt from the COM7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

**Noninterrupt Related Bits**

| | |
|---|---|
| LOK | Lockout |
| REM | Remote/Local |
| DMAO | Enable/Disable DMA Out |
| DMAI | Enable/Disable DMA In |



## Serial Poll Registers

**READ**

SERIAL POLL STATUS (3R).

| S8 | PEND | S6 | S5 | S4 | S3 | S1 | S0 |
|---|---|---|---|---|---|---|---|

**WRITE**

SERIAL POLL MODE (3W)

| S8 | rsv | S6 | S5 | S4 | S3 | S2 | S1 |
|---|---|---|---|---|---|---|---|

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

## Address Mode/Status Registers

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS STATUS (4R) | CIC | $\overline{ATN}$ | SPMS | LPAS | TPAS | LA | TA | MJMN |
| ADDRESS MODE (4W) | ton | lon | TRM1 | TRM0 | 0 | 0 | ADM1 | ADM0 |

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The functions of T/R2, T/R3 terminals (2 and 5) are determined as below by the TRM1, TRM0 values of the address mode register.

| T/R2 | T/R3 | TRM1 | TRM0 |
|---|---|---|---|
| EOIOE | TRIG | 0 | 0 |
| CIC | TRIG | 0 | 1 |
| CIC | EOIOE | 1 | 0 |
| CIC | PE | 1 | 1 |

EOIOE = TACS + SPAS + CIC • $\overline{CSBS}$

This denotes the input/output of $\overline{EOI}$ terminal.

When "1": Output
When "0": Input

CIC = $\overline{CIDS + CADS}$

This denotes if the controller interface function is active or not.

When "1": $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When "0": $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + $\overline{PPAS}$

This indicates the type of bus driver connected to DI08 to DI01 and DAV lines.

When "1": 3 state type
When "0": Open collector type

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon RESET, TRM0 and TRM1 become "0" (TRM0 = TRM1 = 0) and local message port is provided, so that T/R2 and T/R3 both become "LOW."

## Address Modes

| ton | lon | ADM1 | ADM0 | ADDRESS MODE | CONTENTS OF ADDRESS (0) REGISTER | CONTENTS OF ADDRESS (1) REGISTER |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Talk only mode | Address Identification Not Necessary (No controller on the GPIB) Not Used | |
| 0 | 1 | 0 | 0 | Listen only mode | | |
| 0 | 0 | 0 | 1 | Address mode 1 (A1) | Major talk address or Major listen address | Minor talk address or Minor listen address |
| 0 | 0 | 1 | 0 | Address mode 2 (A2) | Primary address (talk or listen) | Secondary address (talk or listen) |
| 0 | 0 | 1 | 1 | Address mode 3 (A3) | Primary address (major talk or major listen) | Primary address (minor talk or minor listen) |
| Combinations other than above indicated Prohibited. | | | | | | |

**Notes:** (A1) —Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

(A2) —Address register 0 = primary, Address register 1 = secondary, interface function TE or LE.

(A3) —CPU must read secondary address via Command Pass Through Register interface function (TE or LE).

## Address Status Bits

| | |
|---|---|
| $\overline{ATN}$ | Data Transfer Cycle (device in CSBS) |
| LPAS | Listener Primary Addressed State |
| TPAS | Talker Primary Addressed State |
| CIC | Controller Active |
| LA | Listener Addressed |
| TA | Talker Addressed |
| MJMN | Sets minor T/L address Reset = Major T/L address |
| SPMS | Serial Poll Mode State |

## Address Registers

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS 0 (6R) | X | DT0 | DL0 | AD5-0 | AD4-0 | AD3-0 | AD2-0 | AD1-0 |
| ADDRESS 1 (7R) | EOI | DT1 | DL1 | AD5-1 | AD4-1 | AD3-1 | AD2-1 | AD1-1 |
| ADDRESS 0/1 (6W) | ARS | DT | DL | AD5 | AD4 | AD3 | AD2 | AD1 |

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

## Address 0/1 Register Bit Selections

ARS —Selects which address register, 0 or 1

DT —Permits or Prohibits address to be detected as Talk

DL —Permits or Prohibits address to be detected as Listen

AD5-AD1 —Device address value

EOI —Holds the value of EOI line when data is received

## Command Pass Through Register

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| COMMAND PASS THROUGH (5R) | CPT7 | CPT6 | CPT5 | CPT4 | CPT3 | CPT2 | CP1 | CPT0 |

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

## End of String Register

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| END OF STRING (7W) | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block.

Aux Mode Register A controls the specific use of this register.

## Auxiliary Mode Register

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| AUXILIARY MODE (5W) | CNT2 | CNT1 | CNT0 | COM4 | COM3 | COM2 | COM1 | COM0 |

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

| CNT 2 1 0 | COM 4 3 2 1 0 | OPERATION |
|---|---|---|
| 0 0 0 | $C_4$ $C_3$ $C_2$ $C_1$ $C_0$ | Issues an auxiliary command specified by $C_4$ to $C_0$. |
| 0 0 1 | 0 $F_3$ $F_2$ $F_1$ $F_0$ | The reference clock frequency is specified and $T_1$, $T_6$, $T_7$, $T_9$ are determined as a result. |
| 0 1 1 | U S $P_3$ $P_2$ $P_1$ | Makes write operation to the parallel poll register. |
| 1 0 0 | $A_4$ $A_3$ $A_2$ $A_1$ $A_0$ | Makes write operation to the aux. (A) register. |
| 1 0 1 | $B_4$ $B_3$ $B_2$ $B_1$ $B_0$ | Makes write operation to the aux. (B) register. |
| 1 1 0 | 0 0 0 $E_1$ $E_0$ | Makes write operation to the aux. (E) register. |

## Auxiliary Commands 0 0 0 $C_4$ $C_3$ $C_2$ $C_1$ $C_0$

COM 43210

| | | |
|---|---|---|
| 00000 | iepon | — Immediate Execute pon—Generate local pon Message |
| 00010 | crst | — Chip Reset—Same as External Reset |
| 00011 | rrfd | — Release RFD |
| 00100 | trig | — Trigger |
| 00101 | rtl | — Return to Local Message Generation |
| 00110 | seoi | — Send EOI Message |
| 00111 | nvid | — Non Valid (OSA reception)—Release DAC Holdoff |
| 01111 | vid | — Valid (MSA reception, CPT, DEC, DET)—Release DAC Holdoff |
| 0X001 | sppf | — Set/Reset Parallel Poll Flag |
| 10000 | gts | — Go To Standby |
| 10001 | tca | — Take Control Asynchronously |
| 10010 | tcs | — Take Control Synchronously |
| 11010 | tcse | — Take Control Synchronously on End |
| 10011 | ltn | — Listen |
| 11011 | ltnc | — Listen with Continuous Mode |
| 11100 | lun | — Local Unlisten |
| 11101 | epp | — Execute Parallel Poll |
| 1X110 | sifc | — Set/Reset IFC |
| 1X111 | sren | — Set/Reset REN |
| 10100 | dsc | — Disable System Control |

## Internal Counter 0 0 1 0 $F_3$ $F_2$ $F_1$ $F_0$

The internal counter generates the state change prohibit times ($T_1$, $T_6$, $T_7$, $T_9$) specified in the IEEE std 488-1978 with reference to the clock frequency.

## Auxiliary A Register 1 0 0 $A_4$ $A_3$ $A_2$ $A_1$ $A_0$

Of the 5 bits that may be specified as part of its access word, 2 bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

| $A_1$ | $A_0$ | DATA RECEIVING MODE |
|---|---|---|
| 0 | 0 | Normal Handshake Mode |
| 0 | 1 | RFD Holdoff on all Data Modes |
| 1 | 0 | RFD Holdoff on End Mode |
| 1 | 1 | Continuous Mode |

| BIT NAME | | | FUNCTION |
|---|---|---|---|
| $A_2$ | 0 | Prohibit | Permits (prohibits) the setting of the END bit by reception of the EOS message. |
| | 1 | Permit | |
| $A_3$ | 0 | Prohibit | Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS. |
| | 1 | Permit | |
| $A_4$ | 0 | 7 bit EOS | Makes the 8 bits/7 bits of EOS register the valid EOS message. |
| | 1 | 8 bit EOS | |

## Auxiliary B Register 1 0 1 $B_4$ $B_3$ $B_2$ $B_1$ $B_0$

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

| BIT NAME | | | FUNCTION |
|---|---|---|---|
| $B_0$ | 1 | Permit | Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command. |
| | 0 | Prohibit | |
| $B_1$ | 1 | Permit | Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS). |
| | 0 | Prohibit | |
| $B_2$ | 1 | $T_1$ (high-speed) | $T_1$ (high speed) as $T_1$ of handshake after transmission of 2nd byte following data transmission. |
| | 0 | $T_1$ (low-speed) | |
| $B_3$ | 1 | $\overline{INT}$ | Specifies the active level of $\overline{INT}$ pin. |
| | 0 | INT | |
| $B_4$ | 1 | ist = SRQS | SRQS indicates the value of ist level local message (the value of the parallel poll flag is ignored). SRQS = 1...ist = 1. SRQS = 0...ist = 0. |
| | 0 | ist = Parallel Poll Flag | The value of the parallel poll flag is taken as the ist local message. |

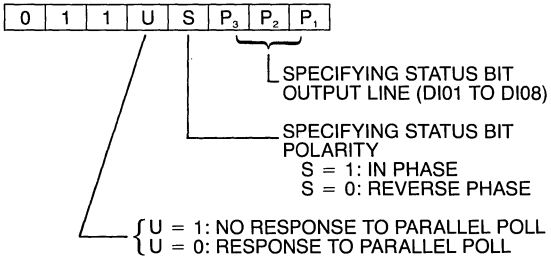
## Auxiliary E Register 1 1 0 0 0 0 $E_1$ $E_0$

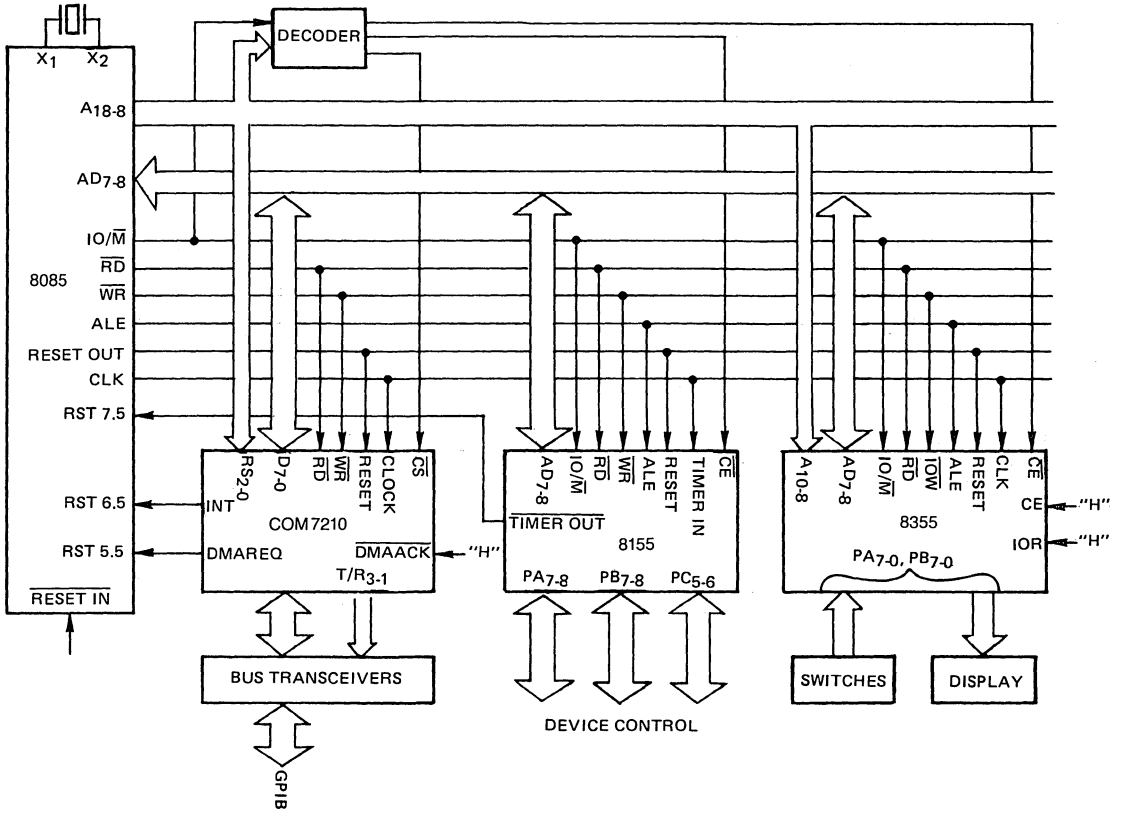
This register controls the Data Acceptance Modes of the TLC.

| BIT | | | FUNCTION |
|---|---|---|---|
| $E_0$ | 1 | Enable | DAC Holdoff by initiation of DCAS |
| | 0 | Disable | |
| $E_1$ | 1 | Enable | DAC Holdoff by initiation of DTAS |
| | 0 | Disable | |

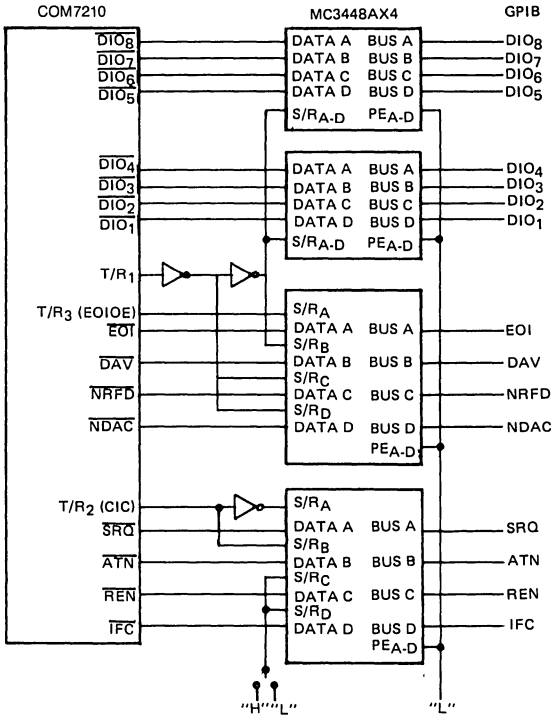
## Parallel Poll Register

The Parallel Poll Register defines the parallel poll response of the COM7210.

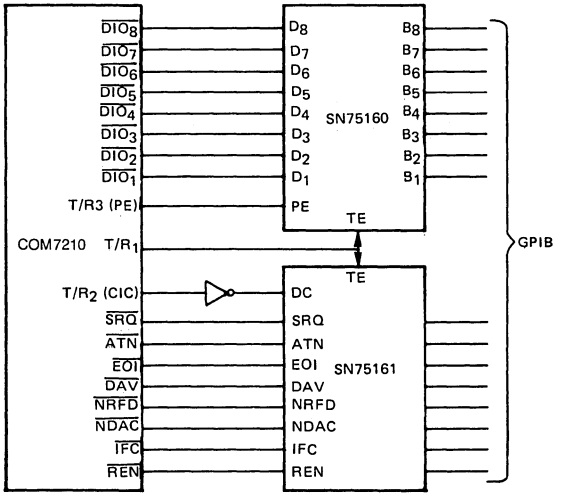





**MINIMUM 8085 SYSTEM WITH COM7210**




**Note:** In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).




**Note:** In the case of low-speed data transfer ($B_2 = 0$), the $T/R_3$ pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0."

## MINIMUM 8085 SYSTEM WITH COM7210 (CONT.)

## ELECTRICAL CHARACTERISTICS

**MAXIMUM GUARANTEED RATINGS** ($T_a$ = 25°C)

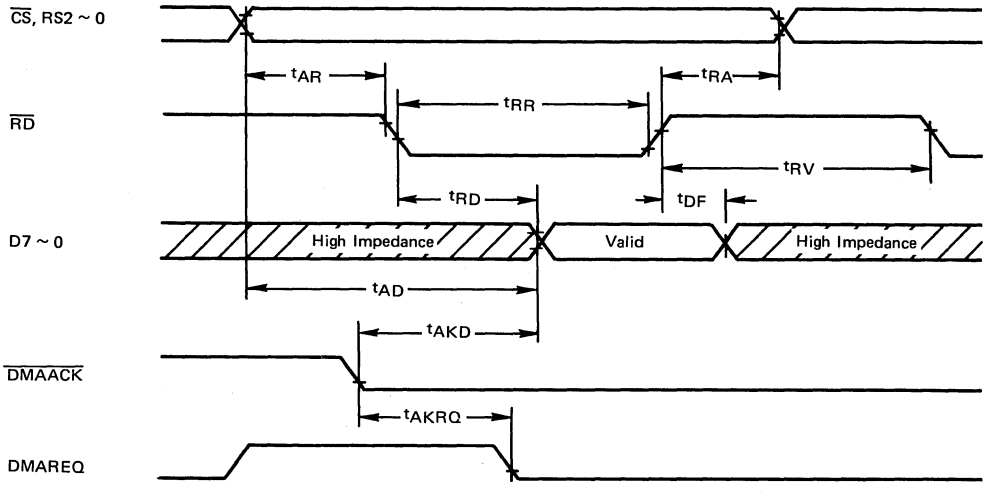
| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.5 ~ +7.0 | V |
| Input Voltage | $V_I$ | −0.5 ~ +7.0 | V |
| Output Voltage | $V_O$ | −0.5 ~ +7.0 | V |
| Operating Temperature | $T_{opt}$ | 0 ~ +70 | °C |
| Storage Temperature | $T_{stg}$ | −65 ~ +125 | °C |

**DC CHARACTERISTICS** ($T_a$ = 0 to +70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | −0.5 | | +0.8 | V | |
| Input High Voltage | $V_{IH}$ | +2.0 | | $V_{CC}$ + 0.5 | V | |
| Low Level Output Voltage | $V_{OL}$ | | | +0.45 | V | $I_{OL}$ = 2 mA (4 mA: T/R1 Pin) |
| High Level Output Voltage | $V_{OH1}$ | +2.4 | | | V | $I_{OH}$ = −400 μA (Except INT) |
| High Level Output Voltage (INT Pin) | $V_{OH2}$ | +2.4<br>+3.5 | | | V | $I_{OH}$ = −400 μA<br>$I_{OH}$ = −50 μA |
| Input Leakage Current | $I_{IL}$ | −10 | | +10 | μA | $V_{IN}$ = 0V ~ $V_{CC}$ |
| Output Leakage Current | $I_{OL}$ | −10 | | +10 | μA | $V_{OUT}$ = 0.45V ~ $V_{CC}$ |
| Supply Current | $I_{CC}$ | | | +180 | mA | |

**CAPACITANCE** ($T_a$ = 25°C, $V_{CC}$ = GND = 0V)

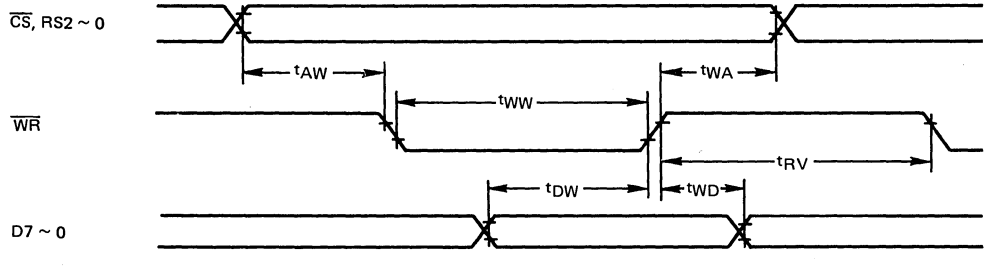
| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 10 | pF | f = 1 MHz |
| Output Capacitance | $C_{OUT}$ | | | 15 | pF | All Pins Except Pin Under Test Tied to AC Ground |
| I/O Capacitance | $C_{I/O}$ | | | 20 | pF | |




**TIMING DIAGRAM**

**AC CHARACTERISTICS,** ($T_a$ = 0 to 70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| $\overline{EOI}$ ↓ → $\overline{DIO}$ | $t_{EODI}$ | | 250 | ns | PPSS → PPAS, ATN = True |
| $\overline{EOI}$ ↓ → T/R1 ↑ | $t_{EOT11}$ | | 155 | ns | PPSS → PPAS, ATN = True |
| $\overline{EOI}$ ↑ → T/RI↓ | $t_{EOT12}$ | | 200 | ns | PPAS → PPSS, ATN = False |
| $\overline{ATN}$ ↓ → $\overline{NDAC}$ ↓ | $t_{ATND}$ | | 155 | ns | AIDS → ANRS, LIDS |
| $\overline{ATN}$↓ → T/R1 ↓ | $t_{ATT1}$ | | 155 | ns | TACS + SPAS → TADS, CIDS |
| $\overline{ATN}$ ↓ → T/R2 ↓ | $t_{ATT2}$ | | 200 | ns | TACS + SPAS → TADS, CIDS |
| $\overline{DAV}$ ↓ → DMAREQ | $t_{DVRQ}$ | | 600 | ns | ACRS → ACDS, LACS |
| $\overline{DAV}$ ↓ → $\overline{NFRD}$ ↓ | $t_{DVNR1}$ | | 350 | ns | ACRS → ACDS |
| $\overline{DAV}$ ↓ → $\overline{NDAC}$ ↑ | $t_{DVND1}$ | | 650 | ns | ACRS → ACDS → AWNS |
| $\overline{DAV}$ ↑ → $\overline{NDAC}$ ↓ | $t_{DVND2}$ | | 350 | ns | AWNS → ANRS |
| $\overline{DAV}$ ↑ → $\overline{DRFD}$ ↑ | $t_{DVNR2}$ | | 350 | ns | AWNS → ANRS → ACRS |
| $\overline{RD}$ ↓ → $\overline{NRFD}$ ↑ | $t_{RNR}$ | | 500 | ns | ANRS → ACRS<br>LACS, DI reg. selected |
| $\overline{NDAC}$ ↑ → DMAREQ ↑ | $t_{NDRQ}$ | | 400 | ns | STRS → SWNS → SGNS, TACS |
| $\overline{NDAC}$ ↑ → $\overline{DAV}$ ↑ | $t_{NDDV}$ | | 350 | ns | STRS → SWNS → SGNS |
| $\overline{WR}$ ↑ → $\overline{DIO}$ | $t_{WDI}$ | | 250 | ns | SGNS → SDYS, BO reg. selected |
| $\overline{NRFD}$ ↑ → $\overline{DAV}$ ↓ | $t_{NRDV}$ | | 350 | ns | SDYS → STRS, $T_1$ = True |
| $\overline{WR}$ ↑ → $\overline{DAV}$ ↓ | $t_{WDV}$ | | 830 + $t_{SYNC}$ | ns | SGNS → SDYS → STRS<br>BO reg. selected, RFD = True<br>$N_F$ = fc = 8 MHz,<br>$T_1$ (High Speed) |
| TRIG Pulse Width | $t_{TRIG}$ | 50 | | ns | |
| Address Setup to $\overline{RD}$ | $t_{AR}$ | 85 | | ns | RS0 ~ RS2 |
| | | 0 | | ns | $\overline{CS}$ |
| Address Hold from $\overline{RD}$ | $t_{RA}$ | 0 | | ns | |
| $\overline{RD}$ Pulse Width | $t_{RR}$ | 170 | | ns | |
| Data Delay from Address | $t_{AD}$ | | 250 | ns | |
| Data Delay from $\overline{RD}$ ↓ | $t_{RD}$ | | 150 | ns | |
| Output Float Delay from $\overline{RD}$ ↑ | $t_{DF}$ | 0 | 80 | ns | |
| $\overline{RD}$ Recovery Time | $t_{RV}$ | 250 | | ns | |
| Address Setup to $\overline{WR}$ | $t_{AW}$ | 0 | | ns | |
| Address Hold from $\overline{WR}$ | $t_{WA}$ | 0 | | ns | |
| $\overline{WR}$ Pulse Width | $t_{WW}$ | 170 | | ns | |
| Data Setup to $\overline{WR}$ | $t_{DW}$ | 150 | | ns | |
| Data Hold from $\overline{WR}$ | $t_{WD}$ | 0 | | ns | |
| $\overline{WR}$ Recovery Time | $t_{RV}$ | 250 | | ns | |
| DMAREQ ↓ Delay from $\overline{DMAACK}$ | $t_{AKRQ}$ | | 130 | ns | |
| Data Delay from $\overline{DMAACK}$ | $t_{AKD}$ | | 200 | ns | |




**TIMING DIAGRAM**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**COM78808**
**PRELIMINARY**

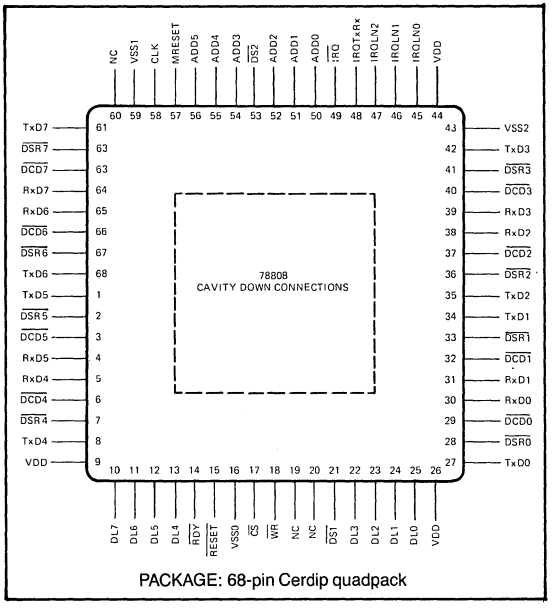


# Eight-channel Universal Asynchronous Receiver/Transmitter Octal UART

## FEATURES

- ☐ Eight independent full duplex serial data lines
- ☐ Programmable baud rates individually selectable for each line's transmitter/receiver (50 to 19,200 baud)
- ☐ Summary registers that allow a single read to detect a data set change or to determine the cause of an interrupt on any line
- ☐ Triple buffers for each receiver
- ☐ Device scanner mechanism that reports interrupt request due transmitter/receiver interrupts
- ☐ Independently programmable lines for interrupt-driven operation
- ☐ Modem status change detection for Data Set Ready (DSR) and Data Carrier Detect (DCD) signals
- ☐ Programmable interrupts for modem status changes
- ☐ Synchronizes critical read-only registers

## PIN CONFIGURATION




PACKAGE: 68-pin Cerdip quadpack

## GENERAL DESCRIPTION

The COM78808 Eight-channel Asynchronous Receiver/Transmitter (Octal UART) is a VLSI device for new generations of asynchronous serial communication designs and for microcomputer systems. This 68-pin device performs the basic operations necessary for simultaneous reception and transmission of asynchronous messages on eight independent lines. Figure 1 is a functional block diagram of the COM78808 Octal UART.

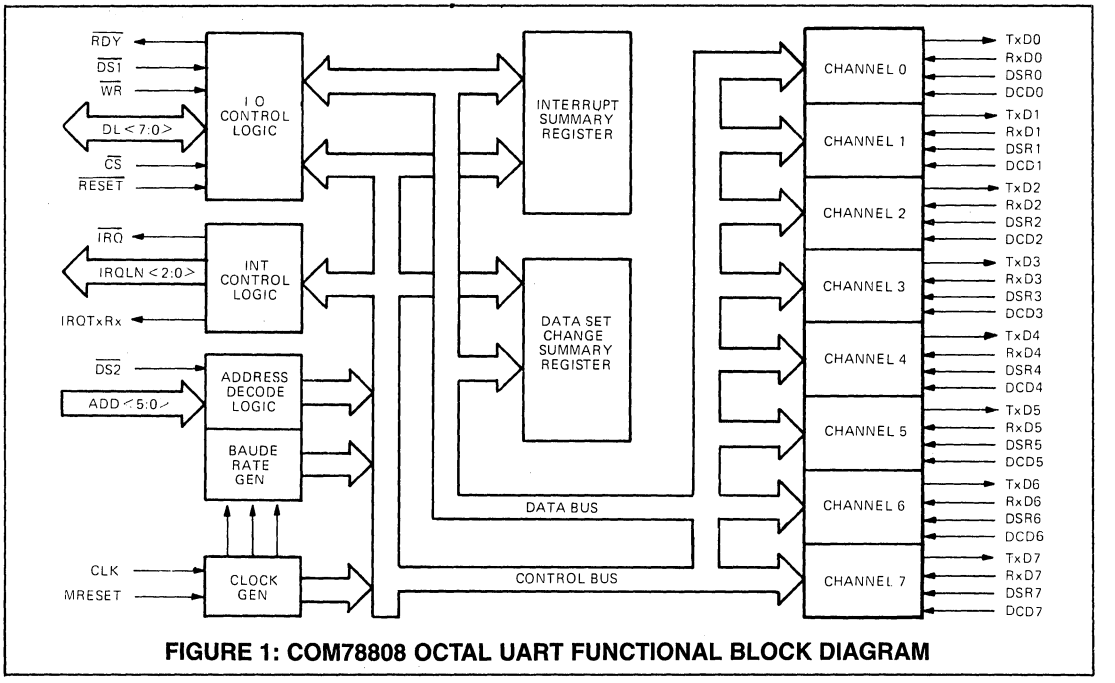



**FIGURE 1: COM78808 OCTAL UART FUNCTIONAL BLOCK DIAGRAM**

## TABLE 1–COM78808 PIN AND SIGNAL SUMMARY

| Pin | Signal | Input/Output | Definition/Function |
|---|---|---|---|
| 10-13,22-25 | DL<7:0> | input/output | Data lines <7:0>–Receives and transmits the parallel data. |
| 50-52,54-56 | ADD<5:0> | input | Address<5:0>–Selects the internal registers in the Octal UART. |
| 17 | $\overline{CS}$ | input | Chip select–Activates the Octal UART to receive and transmit data over the DL<7:0> lines. |
| 21,53 | $\overline{DS1}$,$\overline{DS2}$ | input | Data strobe 1 and 2–Receives timing information for data transfers. The $\overline{DS1}$ and $\overline{DS2}$ inputs must be connected together. |
| 18 | $\overline{WR}$ | input | Write–Specifies direction of data transfer on the DL<7:0> lines. |
| 14 | $\overline{RDY}$ | output | Ready–Indicates when the Octal UART is ready to participate in data transfer cycles. |
| 15 | $\overline{RESET}$ | input | Reset–Initializes the internal logic. |
| 57 | MRESET | input | Manufacturing reset–For manufacturing use. |
| 58 | CLK | input | Clock–Clock input for timing. |
| 62,67,2,7, 41,36,33,28 | $\overline{DSR}$<7:0> | inputs | Data set ready–Monitor data set ready (DSR) signals from modems. |
| 63,66,3,6, 40,37,32,29 | $\overline{DCD}$<7:0> | inputs | Data set carrier detect–Monitor data set carrier detect (DCD) signals from modems. |
| 49 | $\overline{IRQ}$ | output | Interrupt request–Requests a processor interrupt. |
| 45-47 | IRQLN<2:0> | output | Interrupt request line number–Indicates the line number of originating interrupt request. |
| 48 | IRQTxRx | output | Interrupt request transmit/receive–Indicates whether an interrupt request is for transmitting or receiving data. |
| 61,68,1,8, 42,35,34,27 | TxD<7:0> | outputs | Transmit data–Provides asynchronous bit-serial data output streams. |
| 64,65,4,5, 39,38,31,30 | RxD<7:0> | outputs | Receive data–Accepts asynchronous bit-serial data input streams. |
| 44,26,9 | $V_{DD}$ | input | Voltage–Power supply voltage +5 Vdc. |
| 16,59,43 | $V_{SS}$ | input | Ground–Ground reference |

## DATA AND ADDRESS

**Data lines (DL<7:0>)**–These lines are used for the parallel transmission and reception of data between the CPU and the Octal UART. The receivers are active when the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is asserted. The output drivers are active only when the chip select ($\overline{CS}$) signal is asserted, the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is asserted, and the write ($\overline{WR}$) signal is deasserted. The drivers will become inactive (high-impedance) within 50 nanoseconds when one or more of the following occurs: the chip select ($\overline{CS}$) signal is deasserted, the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal is deasserted, or the write ($\overline{WR}$) signal is asserted.

**Address (ADD<5:0>)**–These lines select which Octal UART internal register is accessible through the data I/O lines (DL<7:0>) when the data strobe ($\overline{DS1}$, $\overline{DS2}$) and chip select ($\overline{CS}$) signals are asserted. Table 2 lists the addresses corresponding to each register. The receiver buffer and transmitter holding register for each line have the same address. When the ($\overline{WR}$) signal is deasserted, the address accesses the receiver buffer register and when asserted, it accesses the transmitter holding register.



**TABLE 2–COM78808 REGISTERS ADDRESS SELECTION**

| ADD Line* <5> | <4> | <3> | <2> | <1> | <0> | Read/Write | Register |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Read | Line 0 Receiver Buffer |
| 0 | 0 | 0 | 0 | 0 | 0 | Write | Line 0 Transmitter Holding |
| 0 | 0 | 0 | 0 | 0 | 1 | Read | Line 0 Status |
| 0 | 0 | 0 | 0 | 1 | 0 | Read/Write | Line 0 Mode Registers 1,2 |
| 0 | 0 | 0 | 0 | 1 | 1 | Read/Write | Line 0 Command |
| 0 | 0 | 1 | 0 | 0 | 0 | Read | Line 1 Receiver Buffer |
| 0 | 0 | 1 | 0 | 0 | 0 | Write | Line 1 Transmitter Holding |
| 0 | 0 | 1 | 0 | 0 | 1 | Read | Line 1 Status |
| 0 | 0 | 1 | 0 | 1 | 0 | Read/Write | Line 1 Mode Register 1,2 |
| 0 | 0 | 1 | 0 | 1 | 1 | Read/Write | LIne 1 Command |
| 0 | 1 | 0 | 0 | 0 | 0 | Read | Line 2 Receiver Buffer |
| 0 | 1 | 0 | 0 | 0 | 0 | Write | Line 2 Transmitter Holding |
| 0 | 1 | 0 | 0 | 0 | 1 | Read | Line 2 Status |
| 0 | 1 | 0 | 0 | 1 | 0 | Read/Write | Line 2 Mode Register 1,2 |
| 0 | 1 | 0 | 0 | 1 | 1 | Read/Write | Line 2 Command |
| 0 | 1 | 1 | 0 | 0 | 0 | Read | Line 3 Receiver Buffer |
| 0 | 1 | 1 | 0 | 0 | 0 | Write | Line 3 Transmitter Holding |
| 0 | 1 | 1 | 0 | 0 | 1 | Read | Line 3 Status |
| 0 | 1 | 1 | 0 | 1 | 0 | Read/Write | Line 3 Mode Register 1,2 |
| 0 | 1 | 1 | 0 | 1 | 1 | Read/Write | Line 3 Command |
| 1 | 0 | 0 | 0 | 0 | 0 | Read | Line 4 Receiver Buffer |
| 1 | 0 | 0 | 0 | 0 | 0 | Write | Line 4 Transmitter Holding |
| 1 | 0 | 0 | 0 | 0 | 1 | Read | Line 4 Status |
| 1 | 0 | 0 | 0 | 1 | 0 | Read/Write | Line 4 Mode Register 1,2 |
| 1 | 0 | 0 | 0 | 1 | 1 | Read/Write | Line 4 Command |
| 1 | 0 | 1 | 0 | 0 | 0 | Read | Line 5 Receiver Buffer |
| 1 | 0 | 1 | 0 | 0 | 0 | Write | Line 5 Transmitter Holding |
| 1 | 0 | 1 | 0 | 0 | 1 | Read | Line 5 Status |
| 1 | 0 | 1 | 0 | 1 | 0 | Read/Write | Line 5 Mode Register 1,2 |
| 1 | 0 | 1 | 0 | 1 | 1 | Read/Write | Line 5 Command |
| 1 | 1 | 0 | 0 | 0 | 0 | Read | Line 6 Receiver Buffer |
| 1 | 1 | 0 | 0 | 0 | 0 | Write | Line 6 Transmitter Holding |
| 1 | 1 | 0 | 0 | 0 | 1 | Read | Line 6 Status |
| 1 | 1 | 0 | 0 | 1 | 0 | Read | Line 6 Mode Register 1,2 |
| 1 | 1 | 0 | 0 | 1 | 1 | Read/Write | Line 6 Command |
| 1 | 1 | 1 | 0 | 0 | 0 | Read | Line 7 Receiver Buffer |
| 1 | 1 | 1 | 0 | 0 | 0 | Write | Line 7 Transmitter Holding |
| 1 | 1 | 1 | 0 | 0 | 1 | Read | Line 7 Status |
| 1 | 1 | 1 | 0 | 1 | 0 | Read/Write | Line 7 Mode Register 1,2 |
| 1 | 1 | 1 | 0 | 1 | 1 | Read/Write | Line 7 Command |
| X | X | X | 1 | 0 | 0 | Read | Interrupt Summary |
| X | X | X | 1 | 0 | 1 | Read | Data Set Change Summary |

*X = Either 0 or 1.

## BUS TRANSACTION CONTROL

**Chip select ($\overline{CS}$)**–This signal is asserted to permit data transfers through the DL<7:0> lines to or from the internal registers. Data transfer is controlled by the data strobe ($\overline{DS1}$, $\overline{DS2}$) signal and write ($\overline{WR}$) signal.

**Data strobe ($\overline{DS1}$, $\overline{DS2}$)**– The data strobe inputs ($\overline{DS1}$ and $\overline{DS2}$) must be connected together. This input receives timing information for data transfers. During a write cycle, the CPU asserts the data strobe signal when valid output data is available and deasserts the data strobe signal before the data is removed. During a read cycle, the CPU asserts the data strobe signal and the Octal UART transfers the valid data. When the data strobe signal is deasserted, the DL<7:0> lines become a high impedance.

**Write ($\overline{WR}$)**–The write ($\overline{WR}$) signal specifies the direction of data transfer on the DL<7:0> pins by controlling the direction of their transceivers. If the $\overline{WR}$ signal is asserted during a data transfer (the $\overline{CS}$, $\overline{DS1}$, and $\overline{DS2}$ signals asserted), the Octal UART is receiving data from DL<7:0>. If the $\overline{WR}$ signal is deasserted during a write data transfer, the Octal UART is driving data onto the DL<7:0> lines.

### INTERRUPT REQUEST

**Interrupt request $\overline{IRQ}$**–The $\overline{IRQ}$ pin is an open drain output. The integral interrupt scanner asserts the IRQ signal when it has detected an interrupt condition on one of the eight serial data lines.

**Interrupt Request transmit/receive (IRQTxRx)**—This signal indicates when the interrupt scanner in the Octal UART stops and asserts $\overline{IRQ}$ because of a transmitter interrupt condition (the IRQTxRx signal is asserted) or because of a receiver interrupt condition (the IRQTxRx signal is deasserted). The signal is valid only while $\overline{IRQ}$ is asserted. The state of IRQTxRx signal also appears as bit 0 of the interrupt summary register.

**Interrupt request line number (IRQLN<2:0>)**–These lines indicate the line number at which the Octal UART interrupt scanner stopped and asserted the interrupt request ($\overline{IRQ}$) signal. The number on these lines is valid only while the $\overline{IRQ}$ signal is asserted. Line IRQLN<2> is the high-order bit and the IRQLN<0> line is the low-order bit. The state of these signals also appears as bits in the interrupt summary register: IRQLN<2> as bit 3, IRQLN<1> as bit 2, and IRQLN<0> as bit 1. Table 3 shows the line numbers corresponding to settings of IRQLN<2:0>.

**TABLE 3–COM78808 INTERRUPT REQUEST LINE ASSIGNMENTS**

| IRQ Line <2> | <1> | <0> | Line |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

## SERIAL DATA

**Transmit data (TxD<7:0>)**–These outputs transmit the asynchronous bit-serial data streams. They remain at a high level when no data is being transmitted and a low level when the TxBRK bit in the associated line's command register is set.

**Receive data (RxD<7:0>)**–These lines accept asynchronous bit-serial data streams. The input signals must remain in the high state for at least one-half bit time before a high-to-low transition is recognized. ( A high-to-low transition is required to signal the beginning of a "start" bit and initiate data reception).

## MODEM SIGNALS

**Data set ready ($\overline{DSR}$<7:0>)**–These eight input pins, one for each serial data line on the COM78808, are typically connected via intervening level converters to the data set ready outputs of modems. A TTL low at a $\overline{DSR}$ pin causes the DSR bit (bit 7) in the corresponding line's status register to be asserted. A TTL high at a $\overline{DSR}$ pin causes the DSR bit in the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit that corresponds to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

**Carrier detect (DCD<7:0>)**–These eight input pins, one for each serial data line of the Octal UART, are typically connected through intervening level converters to the received line signal detect (also called carrier detect) outputs of modems. A TTL low at a $\overline{DCD}$ pin causes the DCD bit of the corresponding line's status register to be deasserted. A change of this input from high-to-low, or low-to-high, causes the assertion of the data set change (DSCHNG) bit corresponding to this line in the data set change summary register. Changes from one state to the other and back again that occur within one microsecond may not be detected.

## GENERAL CONTROL SIGNALS

**Ready ($\overline{RDY}$)**–The $\overline{RDY}$ pin is an open drain output. Upon detecting a negative transition of chip select ($\overline{CS}$), the Octal UART asserts the $\overline{RDY}$ signal to indicate readiness to take part in data transfer cycles. The $\overline{RDY}$ signal deasserts after the trailing edge of $\overline{CS}$.

**Reset ($\overline{RESET}$)**–When the $\overline{RESET}$ input is asserted, the TxD<7:0> lines are asserted and all internal status bits listed in the "Architecture Summary" discussion are cleared.

**Manufacturing reset (MRESET)**–This signal is for manufacturing use only and the input should be connected to ground for normal operation.

## MISCELLANEOUS SIGNALS

**Clock in (CLK)**–All baud rates and internal clocks are derived from this input. Normal operating frequency is 4.9152 MHz ±0.1 percent and duty cycle is 50 percent ±5 percent.

## POWER AND GROUND

**Voltage ($V_{DD}$)**–Power supply 5 Vdc

**Ground ($V_{SS}$)**–Ground reference

## ARCHITECTURE SUMMARY

The Octal UART functions as a serial-to-parallel, parallel-to-serial converter/controller. It can be programmed by a microprocessor to provide different characteristics for each of its eight serial data lines (stop bits, parity, character length, split baud rates, etc.)

Each serial line functions the same as a one-line UART-type device thereby reducing the number of chips and conserving space on communication devices that require multiple communications lines.

An integral interrupt scanner checks for device interrupt conditions on the eight lines. Its scanning algorithm gives priority to receivers over transmitters. The scanner can also check for interrupts resulting from changes in modem control signals $\overline{DSR}$ and $\overline{DCD}$.

### Line-specific Registers

Each of the eight serial data lines in the Octal UART has a set of registers for buffering data into and out of the line and for external control of the line's characteristics. These registers are selected for access by setting the appropriate address on lines ADD<5:0>. Lines ADD<5:3> select one of the eight data lines. Lines ADD<2:0> select the specific register for that line. Refer to Table 2 for the register address assignments.

**Receiver buffer register**–Each line's receiver consists of a character assembly register and a two-entry FIFO that is the receiver buffer register. When the RxEN bit in a line's command register is set, received characters are moved automatically into the line's receiver buffer as soon as they have been deserialized from the associated communications line. When there are characters in this FIFO, the RxRDY bit is set in the status register for the line.

The assertion of the RxRDY signal for a line that already has the RxIE bit of its command register set causes the interrupt scanner logic to stop and generate an interrupt condition (the $\overline{IRQ}$ signal is asserted). When the receiver buffer is read, the interrupt condition is cleared (the $\overline{IRQ}$ signal is deasserted) and the interrupt scanner resumes operation.

If there is another entry in a line's FIFO, the RxRDY bit remains asserted. When the interrupt scanner reaches this line again, the assertion of RxRDY causes the scanner to halt and assert the $\overline{IRQ}$ again.

Asserting the $\overline{RESET}$ signal or clearing the RxEN bit initializes the receiver logic of Octal UART. The RxRDY flag is cleared and the receiver buffer register outputs become undefined. Any data in the FIFO at that time is lost.

**Transmitter holding register**–Each line has a writable transmitter holding register. When the TxEN bit in the line's command register is set, characters are moved automatically from the output of this register into the transmitter serialization logic whenever the serialization logic becomes idle.

When this register is empty, the TxRDY bit in the line's status register is set. If the transmitter interrupt enable (TxIE) bit in the line's command register is also set, the interrupt scanner logic halts and generates an interrupt condition. If a character is then loaded into the register, the interrupt is cleared and the scanner resumes operation.

Assertion of the $\overline{RESET}$ signal initializes the transmitter logic of the Octal UART. The TxRDY flag is cleared and the transmitter holding register's contents are lost. The transmitter enable (TxEN) bit in the line's command register is also cleared by $\overline{RESET}$. If at the end of the reset process, the TxEN is reasserted and TxRDY bit is reasserted. Software clearing of TxEN alone produces results different from the full $\overline{RESET}$ in that the transmitter holding register's contents are not lost; they are transmitted when TxEN is set again.

**Status register**–Each line has a read-only status register that provides information about the current state of the given line. This register indicates a line's readiness for transmission or reception of data and flags error conditions in its bit fields. Figure 3 shows the format of the status register. Table 3 lists the flag bits in each status register.

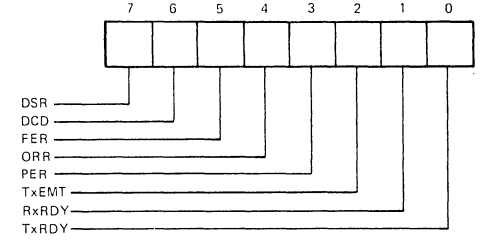



**FIGURE 3: COM78808 STATUS REGISTERS (LINE 0-6) FORMAT**

## TABLE 4–COM78808 STATUS REGISTERS (LINES 0-7) DESCRIPTION

| Bit | Description |
|---|---|
| 7 | DSR (Data set ready)–This bit is the inverted state of the $\overline{DSR}$ line. |
| 6 | DCD (Data set carrier detect)–This bit is the inverted state of the $\overline{DCD}$ line. |
| 5 | FER (Frame error)–Set when the received character currently displayed in the receiver buffer register was not framed by a stop bit. Only the first stop bit is checked to determine that a framing error exists. Subsequent reading of the receiver buffer register that indicates all zeros (including the parity bit, if any) can be interpreted as a Break condition. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, or by setting the reset error RERR (bit 4) of the command register. |
| 4 | ORR (Overrun error)–Set when the character in the receiver buffer register was not read before another character was received. Cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, or by setting reset error RERR (bit 4) of the command register. |
| 3 | PER (Parity error)–If parity is enabled and this bit is set, the received character in the receiver buffer register has an incorrect parity bit. This bit is cleared by clearing RxEN (bit 2) of the command register, by asserting the $\overline{RESET}$ input, by setting reset error RERR (bit 2) of the command register, or by reading the current character in the receiver buffer register. |
| 2 | TxEMT (Transmitter empty)–Set when the transmitter serialization logic for the associated line has completed transmission of a character, and no new character has been loaded into the transmitter holding register. Cleared by loading the transmitter holding register, by clearing TxEN (0) of the command register, or by asserting the $\overline{RESET}$ input. |
| 1 | RxRDY (Receiver buffer ready)–When set, a character has been loaded into the FIFO buffer from the deserialization logic. Cleared by reading the receiver buffer register, by clearing RxEN (bit 2) in the command register, or by asserting the $\overline{RESET}$ input. |
| 0 | TxRDY (Transmitter holding register ready)—When set, this bit indicates that the transmitter holding register is empty. Cleared when the program has loaded a character into the transmitter holding register, when the transmitter for this line is disabled by clearing TxEN (bit 0) in the command register, or by asserting the $\overline{RESET}$ input. This bit is initially set when the transmitter logic is enabled by the setting of TxEN (bit 0) and the transmitter holding register is empty. This bit is not set when the automatic echo or remote loopback modes are programmed. Data can be overwritten if a consecutive write is performed while TxRDY is cleared. |

**Mode registers 1 and 2**—These read/write registers control the attributes (including parity, character length, and line speed) of the communications line.

Each of the eight communications lines has two of these registers, both accessed by the same address on ADD<5:0>. Successive access operations (either read or write, in any combination) alternate between the two registers at that address by use of an internal pointer. The first operation addresses mode register 1, the next address mode register 2, and another after that would recycle the pointer to mode register 1. The pointer is reset to point to mode register 1 by $\overline{\text{RESET}}$ or by a read of the command register for this line. These registers should not be accessed by bit-oriented instructions that do read/modify/write cycles such as the PDP-11 BIS, BIC, and BIT instructions.

Figure 4 shows the format of mode registers 1 and Table 5 describes the function of the register information.

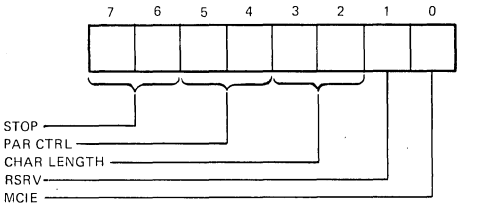



**FIGURE 4–COM78808 MODE REGISTERS 1 (LINE 0-6) FORMAT**

**TABLE 5–COM78808 MODE REGISTERS 1 (LINES 0-6) DESCRIPTION**

| Bit | Description |
|---|---|
| 7,6 | STOP–These bits determine the number of stop bits that are appended to the transmitted characters as follows. These bits are cleared by asserting the $\overline{\text{RESET}}$ input.<br>**Bits 7 6** — **Stop Bits**<br>0 0 — Invalid<br>0 1 — 1.0<br>1 0 — 1.5<br>1 1 — 2.0 |
| 5,4 | PAR CTRL (Parity control)–These bits determine parity as follows and are cleared by asserting the $\overline{\text{RESET}}$ input. X = either 1 or 0.<br>**Bits 5 4** — **Parity Type**<br>1 1 — Even<br>0 1 — Odd<br>X 0 — Disabled |
| 3,2 | CHAR LENGTH (Character length)–These bits determine the length (excluding start bit, parity, and stop bits) of the characters received and sent. Received characters of less than 8 bits are "right aligned" in the receiver buffer with unused high-order bits equal to zero. Parity bits are not shown in the receiver buffer. The character length bits are cleared by asserting the $\overline{\text{RESET}}$ input. The character length bits are defined as follows:<br>**Bit 3 2** — **Bit Length**<br>0 0 — 5<br>0 1 — 6<br>1 0 — 7<br>1 1 — 8 |
| 1 | RSRV (Reserved and cleared by asserting the $\overline{\text{RESET}}$ input.) |
| 0 | MCIE (Modem control interrupt enable)–When set and RxIE (bit 5) of the command register is set, the modem control interrupts are enabled. Refer to the Interrupt Scanner and Interrupt Handling information. Cleared by asserting the $\overline{\text{RESET}}$ input. |

Figure 5 shows the format of mode registers 2 and Table 6 indicates the baud rate selections of the register. Bits 7 through 4 of the mode register 2 control the transmitter baud rate and bits 3 through 0 control the receiver baud rate. These registers are cleared by asserting $\overline{\text{RESET}}$ input.

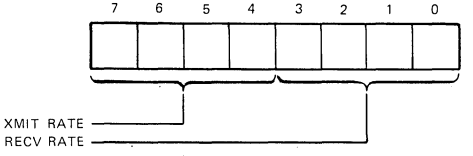



**FIGURE 5–COM78808 MODE REGISTERS 2 (LINE 0-6) FORMAT**

**Command register**–These read/write registers control various functions on the selected line. Figure 6 shows the format of the command registers and Table 6 describes the function of the register information.

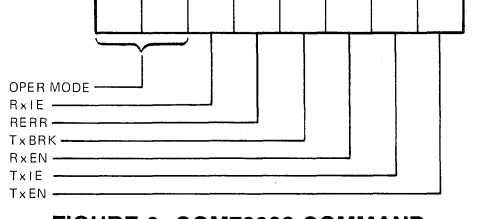



**FIGURE 6–COM78808 COMMAND REGISTERS (LINE 0-6) FORMAT**

## TABLE 6–COM78808 MODE REGISTERS 2 (LINES 0-6) DESCRIPTION

| Bit | Description |
|---|---|
| 7:0 | XMIT RATE/RECV RATE (Transmitter/Receiver Rate)–Selects the baud rate of the transmitter (bits 7:4) and receiver (bits 3:0) as follows: |

| Transmitter Bits | | | | Receiver Bits | | | | Nominal | Actual | Error* |
|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Rate | Rate | (percent) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 50 | same | — |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 75 | same | — |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 110 | 109.09 | 0.826 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 134.5 | 133.33 | 0.867 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 150 | same | — |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 300 | same | — |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 600 | same | — |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1200 | same | — |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1800 | 1745.45 | 3.03 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 2000 | 2021.05 | 1.05 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2400 | same | — |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3600 | 3490.91 | 3.03 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4800 | same | — |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 7200 | 6981.81 | 3.03 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 9600 | same | — |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 19200 | same | — |

*The frequency of the clock input (CLK) is 4.9152 MHz. The clock input may vary by 0.1 percent. This variance results in an error that must be added to the error listed.

## TABLE 7–COM78808 COMMAND REGISTERS (LINES 0-7) DESCRIPTION

| Bit | Description |
|---|---|
| 7,6 | OPER MODE (Operating mode)–These bits control the operating mode of the channel as follows. These bits are cleared by asserting the RESET input. |

| Bit | | Operating Mode |
|---|---|---|
| 7 | 6 | |
| 0 | 0 | Normal operation |
| 0 | 1 | Automatic echo |
| 1 | 0 | Local loopback |
| 1 | 1 | Remote loopback |

| | |
|---|---|
| 5 | RxIE (Receiver interrupt enable)–When set, the RxRDY flag (bit 1) of the status register for this line will generate an interrupt. |
| 4 | RERR (Reset error)–When set, this bit clears the framing error, overrun error, and parity error of the status register associated with this line. This bit is cleared by asserting the RESET input (not self-clearing). |
| 3 | TxBRK (Transmit break)–When set, this bit forces the appropriate TxD<7:0> line to the spacing state at the conclusion of the character presently being transmitted. When the program clears this bit, normal operation is restored, and any character pending in the transmitter holding register is moved into the serialization logic and transmitted. The minimum break length obtainable is twice the character length plus 1 bit time. The maximum break length depends on the amount of time between the program setting and clearing this bit, but is an integral number of bit times. This bit is cleared by asserting the RESET input. |
| 2 | RxEN (Receiver enable)–When set, this bit enables the receiver logic. When cleared, it stops the assembling of the received character, clears all receiver error bits and the RxRDY (bit 1) of the status register, clears any receiver interrupt conditions associated with this line, and initializes all receiver logic. This bit is cleared by asserting the RESET input. |
| 1 | TxIE (Transmit interrupt enable)–When set, the state of the associated TxRDY flag (bit 0) of the status register is made available to the interrupt scanner logic. When the interrupt scanner logic scans this line, it determines if the TxRDY flag is asserted and generates an interrupt by asserting the IRQ signal. |
| 0 | TxEN (Transmitter enable)–When set, this bit enables the transmitter logic. When cleared, it inhibits the serialization of the characters that follow but the serialization of the current character is completed. It also clears the TxRDY flag (bit 0) of the status register, clears any transmitter interrupt conditions associated with this line, and initializes all transmitter logic except that associated with the transmitter holding register. The character in the transmitter holding register is retained so that XON/XOFF situations can be properly processed. This bit is cleared by asserting the RESET input. |

Bits 5 through 0 enable the line's receiver and transmitter, enable handling of interrupts, initiate the transmission of break characters, and reset error bits for the line. Refer to "Interrupt Scanner" and "Interrupt Handling" paragraphs for detailed interrupt information. Bits 7 and 6 control the operating mode of the line. The four modes that can be set are:

- Normal operation–The serial data received is assembled in the receiver logic and transferred in parallel to the receiver buffer register. (The RxEN bit must be set.) Data to be transmitted is loaded in parallel into the transmitter holding register, then automatically transferred into the transmitter logic and serialized for transmission. (The TxEN bit must be set.)

- ☐ Automatic echo–The serial data received is assembled into parallel in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register. Arriving serial data is also routed to the line's TxD<n> pin for serial output. TxEN is ignored and the transmitter logic is disabled. TxRDY flags and TxEMT indications are cleared. No transmitter interrupts are generated.
- ☐ Local loopback–The serial data from the RxD<n> input is ignored and the receiver serial input receives data from the transmitter serial output. The data is assembled into parallel form in the receiver logic (the RxEN bit must be set) and transferred to the receiver buffer register where it can be read by the program. Data to be transmitted to the receiver is loaded in parallel form into the transmitter holding register from which it is automatically moved into the transmitter logic and serialized for transmission. (The TxEN bit must be set.) The transmission goes only to the receiver serial input; the TxD<n> output is held high. As in normal operation, transmission and reception baud rates are controlled by the transmitter speed and receiver speed entries in mode register 2.
- ☐ Remote loopback–The serial data received on the RxD<n> line is returned to the TxD<n> line without further action. No data is received or transmitted. The RxRDY, TxRDY, and TxEMT flags are disabled. The TxEN and RxEN bits of the command register are held cleared, causing the transmitter and receiver logic to be disabled.

**SUMMARY REGISTERS**

The Octal UART contains two registers that summarize the current status of all eight serial data lines, making it possible to determine that a line's status has changed with a single read operation. These registers are selected for access by setting the appropriate address on pins ADD <2:0>. Because the registers are shared by eight serial lines, the line-selection bits (ADD <5:3>) are ignored when these registers are accessed. Refer to "Interrupt Scanner and Interrupt Handling" for detailed interrupt information.

**Interrupt summary register**–This read-only register indicates that a transmitter or receiver interrupt condition has occured, and indicates the line number that generated the interrupt. Figure 7 shows the format of the interrupt summary register and Table 8 describes register information.

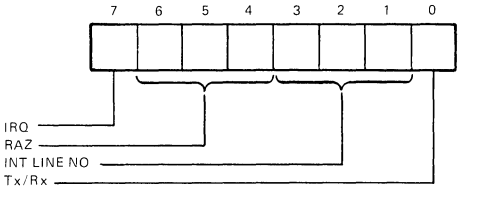



**FIGURE 7–COM78808 INTERRUPT SUMMARY REGISTER FORMAT**

**TABLE 8–COM78808 INTERRUPT SUMMARY REGISTER DESCRIPTION**

| Bit | Description |
|---|---|
| 7 | IRQ (Interrupt request)–When set, this bit indicates that the interrupt scanner has found an interrupting condition among the eight serial lines of the Octal UART. These conditions also result in the Octal UART asserting the $\overline{IRQ}$ signal. |
| 6:4 | RAZ (Read as zero)–Not used |
| 3:1* | INT LINE NO (Interrupting line number)–These bits indicate the line number upon which an interrupting condition was found. These bits correspond to the IRQLN <2:0> signals–(bit 3 = IRQLN<2>, bit 2 = IRQLN<1>, and bit 1 = IRQLN<0>. Refer to Table 3. |
| 0* | Tx/$\overline{Rx}$ (Transmit/receive)–This bit indicates whether the interrupting condition was caused by a transmitter (Tx/$\overline{Rx}$ equals 1) or a receiver (Tx/$\overline{Rx}$ equals 0). This bit corresponds to the IRQTxRx signal of the Octal UART and is set when IRQTxRx is asserted. |

*Bits 3-0 above represent the outputs of a free-running counter and are valid only when bit 7 is set.

**Data set change summary register**–When the $\overline{DSR}$ or $\overline{DCD}$ inputs that are associated with a line change state, the bit corresponding to that line in this read-only register is set. The current state of the $\overline{DSR}$ and $\overline{DCD}$ inputs can then be obtained from that line's status register. If the state of a line changes twice within one microsecond, the change in state may not be detected. Figure 8 shows the format of the data set change summary register.

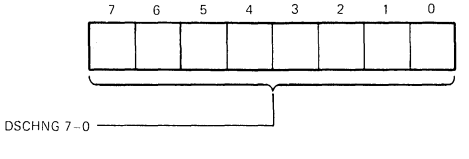



**FIGURE 8–COM78808 DATA SET CHANGE SUMMARY REGISTER FORMAT**

When the MCIE bit in a line's mode register 1 is set and RxIE is also set, the modem control interrupts are enabled for that line. If DSCHNG for that line is then set, the interrupt scanner will halt and assert the $\overline{IRQ}$ signal. The data set change summary register bits are cleared by writing a 1 into the bit position. A program that uses this register should read and save a copy of its contents. The copy can then be written back to the register to clear the bits that were set. The system interrupts should be disabled and writeback should directly follow the read operation.

Assertion of the $\overline{RESET}$ signal disables and initializes the data set change logic. When the $\overline{RESET}$ signal is deasserted, future changes in $\overline{DSR}$ and $\overline{DCD}$ are reported as they occur.

## INTERRUPT SCANNER AND INTERRUPT HANDLING

The interrupt scanner is a four-bit counter that sequentially checks lines 0 through 7 for a receiver interrupt (counter positions (0-7) and then checks the lines in the same order for a transmitter interrupt (counter positions 8-15). If the scanner detects an interrupt condition, it stops and the $\overline{IRQ}$ signal is asserted. An interrupt must be serviced by software or no other interrupt request can be posted.

The scanner determines that a line has a receiver interrupt if the line's receiver buffer is ready and receiver interrupts are enabled for that line (RxRDY and RxIE = 1) or either of the line's modem status signals has changed state and both receiver and modem control interrupts are enabled for that line (DSCHNG and RxIE and MCIE = 1).

The scanner determines that a line has a transmitter interrupt if the line's transmitter holding the register is empty and transmitter interrupts are enabled for that line (TxRDY and TxIE = 1).

When the scanner detects an interrupt, it reports the line number on the IRQ<2:0> lines. The IRQTxRx signal is asserted for a transmitter interrupt and deasserted for a receiver interrupt. The appropriate bits are also updated in the interrupt summary register. The $\overline{IRQ}$ line is deasserted and the scanner is restarted for each of the following three types of interrupt conditions.

- ☐ Reading the receiver buffer or resetting the RxIE bit of the interrupting line for the first type of receiver interrupt previously described.
- ☐ Resetting the MCIE, RxIE, or DSCHNG bit of the interrupting line for the second type of receiver interrupt previously described.
- ☐ Loading the transmitter holding register or resetting the TxIE bit of the interrupting line for transmitter interrupts.

If the scanner was originally stopped by a receiver interrupt condition, the scanner resumes sequential operation from where it stopped, thus providing receivers with equal priority. If the scanner was stopped by a transmitter condition, the scanner restarts from position 0 (line 0's receiver), thus giving receivers priority over transmitters.

## EDGE-TRIGGERED AND LEVEL-TRIGGERED INTERRUPT SYTSTEMS

If the interrupt system of the Octal UART is used only for generating interrupts for the RxRDY and/or TxRDY flags, the $\overline{IRQ}$ line can be connected to a processor having either edge-triggered or level-triggered interrupt capability. If the modem control interrupts are being used (MCIE in mode register 1 = 1), the $\overline{IRQ}$ line can be connected only to a processor that uses level-triggered interrupts.

## MODEM HANDLING

The TxEMT (transmitter empty) bit of the status register is typically used to indicate when a program can disable the transmission medium, as when deasserting the request-to-send line of a modem. A typical program will load the last character for transmission and then monitor the TxEMT bit of the status register.

The assertion of the TxEMT bit to indicate that transmission is complete may occur a substantial time after the loading of the last character. After the last character is loaded, one character is in the transmitter holding register and one character is in the serialization logic. Therefore, it will be two character times before the transmission process is completed. Waiting for the TxRDY signal to assert before monitoring the TxEMT status shortens this by one character time because the TxRDY status bit indicates that there are no characters in the transmitter holding register. The times involved are calculated by taking the reciprocal of the baud rate being used, multiplying by the number of bits per character (a starter bit–5,6,7, or 8 data bits; plus parity bit if enabled; and 1,1.5, or 2 stop bits), and multiplying by either two characters or one, depending on when TxEMT monitoring begins.

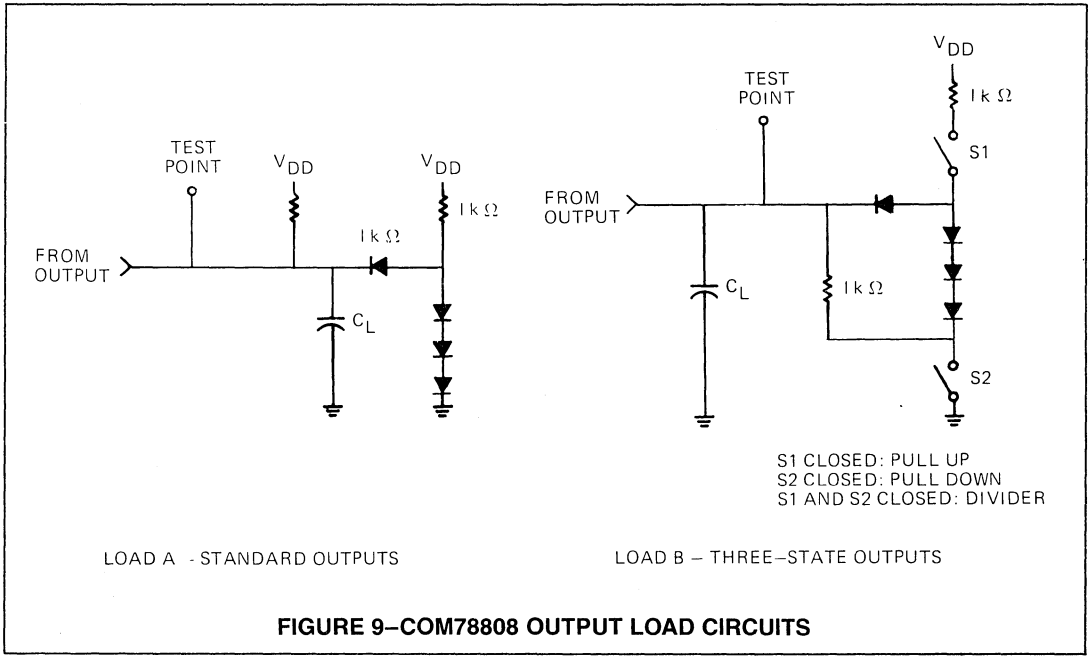



**FIGURE 9–COM78808 OUTPUT LOAD CIRCUITS**

**MAXIMUM GUARANTEED RATINGS***

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −55° to +125°C |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Positive Voltage on any I/O Pin, with respect to ground | +7V |
| Negative Voltage on any I/O Pin, with respect to ground | −0.3V |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

## TABLE 9–COM78808

### DC ELECTRICAL CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{DD}$ = +5V ±5%

| Symbol | Parameter | Test Condition | Requirements Min. | Requirements Max. | Units |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $V_{DD}$ = Min.<br>$I_{OH}$ = 3.5 mA for DL<7:0><br>$I_{OH}$ = 2.0 mA for all remaining output except $\overline{IRQ}$ and $\overline{RDY}$ | 2.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{DD}$ = Min.<br>$I_{OL}$ = 5.5 mA for DL<7:0><br>$I_{OL}$ = 3.5 mA for all remaining outputs | | 0.4 | V |
| $I_{IH}$ | Input current at maximum input voltage | $V_{DD}$ = Max.<br>$V_I$ = $V_{DD}$(Max.) | | 10 | µA |
| $I_{IL}$ | Input current at miminum input voltage | $V_{DD}$ = Max.<br>$V_I$ = 0.0V | | −10 | µA |
| $I_{OS}$[1] | Short-circuit output current for DL<7:0> all remaining outputs except $\overline{IRQ}$ and $\overline{RDY}$ | $V_{DD}$ = Max. | −50<br>−30 | −180<br>−110 | mA<br>mA |
| $I_{OZL}$[2] | Three-state output current | $V_{DD}$ = Max.<br>$V_O$ = 0.4V | | 10 | µA |
| $I_{OZH}$[2] | Three-state output current | $V_{DD}$ = Max.<br>$V_O$ = 2.4V | | 10 | A |
| $I_{DD}$ | Supply current | $V_{DD}$ = Max.<br>$T_A$ = 0° | | 240 | mA |
| $C_{in.}$ | Input capacitance | | | 4 | pF |
| $C_{IO}$[3] | Input/output capacitance | | | 5 | pF |

[1]No more than one ouput should be short circuited at a time, and the duration of the short should not exceed 1 second.
[2]All three-state output drivers are wired in an I/O configuration. The parameters include the driver and input receiver leakage currents.
[3]The parameters include the capacitive loads of the output driver and the input receiver.

## TIMING PARAMETERS

Figure 10 shows the signal timing for a read cycle to transfer information from the Octal UART to the processor. Figure 11 shows the signal timing for a write cycle to transfer information from the processor to the Octal UART. Table 11 lists the timing parameters for the read and write cycles.

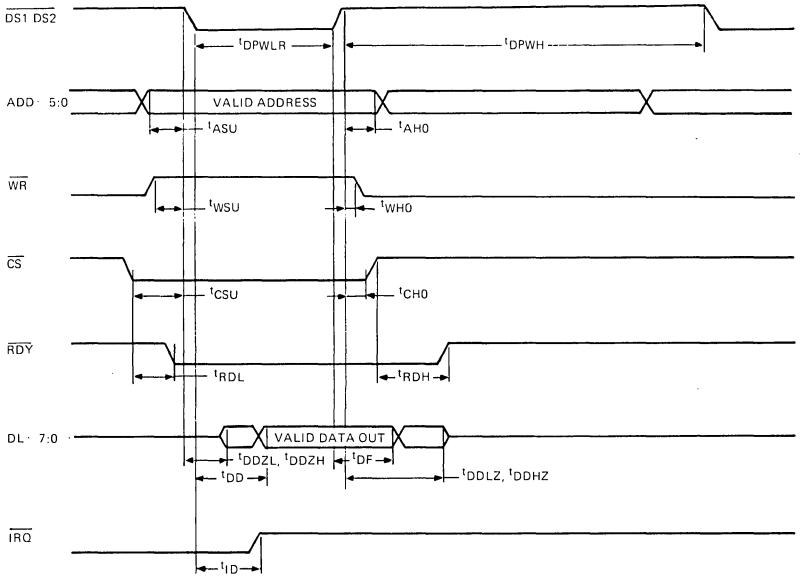



**FIGURE 10–COM78808 BUS READ CYCLE TIMING**

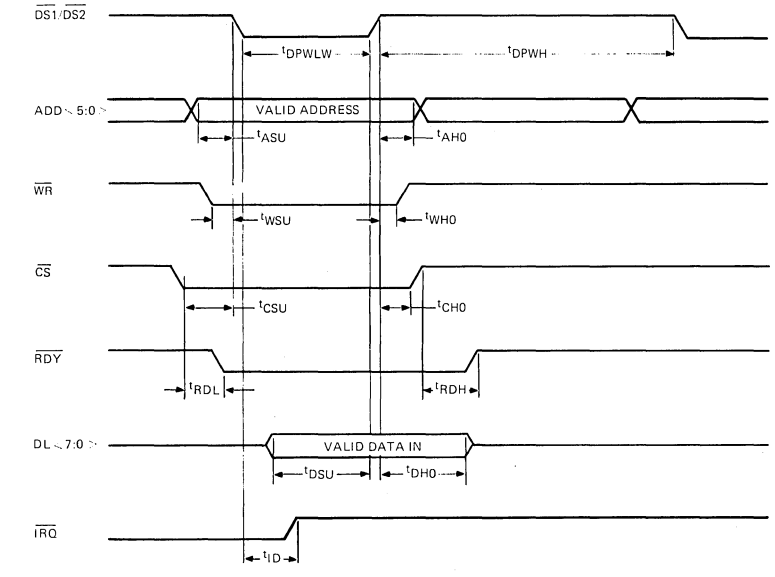



**FIGURE 11–COM78808 BUS WRITE CYCLE TIMING**

## TABLE 10–COM78808 BUS READ AND WRITE TIMING PARAMETERS

| Symbol | Definition | Requirements (ns) Min. | Max. | Load Circuit[1] |
|---|---|---|---|---|
| $t_{AHO}$ | Hold time of a valid ADD <5:0> to a valid high level of $\overline{DS1}$ and $\overline{DS2}$. | 10 | | |
| $t_{ASU}$ | Setup time of a valid ADD <5:0> to the falling edge of $\overline{DS1}$ and $\overline{DS2}$. | 30 | | |
| $t_{CHO}$ | Hold time of a valid low level of $\overline{CS}$ to a valid high level of $\overline{DS1}$ and $\overline{DS2}$. | 10 | | |
| $t_{CSU}$ | Setup time of a valid low level of $\overline{CS}$ to the falling edge of $\overline{DS1}$ and $\overline{DS2}$. | 30 | | |
| $t_{DD}$ | Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to valid high or low data on DL <7:0>. | 165 | | $C_L = 150$ pF |
| $t_{DDLZ}$[2]<br>$t_{DDHZ}$ | Propagation delay of a valid high level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output drivers disabled. | | | |
| | $t_{DDLZ}$ | | 50 | $C_L = 50$pF |
| | $t_{DDHZ}$ | | 50 | $C_L = 50$pF |
| | $t_{DDLZ}$ | | 60 | $C_L = 100$pF |
| | $t_{DDHZ}$ | | 60 | $C_L = 100$pF |
| | $t_{DDLZ}$ | | 65 | $C_L = 150$pF |
| | $t_{DDHZ}$ | | 65 | $C_L = 150$pF |
| $t_{DDZL}$ | Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low and $\overline{WR}$ is high) to DL <7:0> output driver enabled. | | | |
| | $t_{DDZL}$ | 0 | 165 | $C_L = 150$pF |
| | $t_{DDZH}$ | 0 | 165 | $C_L = 150$pF |
| $t_{DF}$ | Hold time provided during a read cycle by Octal UART of valid high or low data on DL <7:0> after the rising edge of $\overline{DS1}$ and $\overline{DS2}$. | 0 | | |
| $t_{DHO}$ | Hold time of a valid DL <7:0> to a valid high level of $\overline{DS1}$ or $\overline{DS2}$. | 30 | | |
| $t_{DPWH}$ | Pulse width high of $\overline{DS1}$ and $\overline{DS2}$. | 450 | | |
| $t_{DPWLR}$ | Pulse width low of $\overline{DS1}$ and $\overline{DS2}$ when $\overline{WR}$ is high (read operation). Refer to timing parameter $t_{DPWLW}$ also. | 180 | 10,000 | |
| $t_{DPWLW}$ | Pulse width low of $\overline{DS1}$ and $\overline{DS2}$ when $\overline{WR}$ is low (write operation). Refer to timing parameter $t_{DPWLR}$ also. | 130 | 10,000 | |
| $t_{DSU}$ | Setup time of a valid DL <7:0> to the falling edge of $\overline{DS1}$ and $\overline{DS2}$. | 0 | | |
| $t_{ID}$[3] | Propagation delay of a valid low level on $\overline{DS1}$ and $\overline{DS2}$ (if $\overline{CS}$ is low) to a high level on IRQ. | | 635 | $C_L = 50$pF |
| $t_{RDH}$[4] | Propagation delay of a valid high level of $\overline{CS}$ to a valid high level on $\overline{RDY}$. | | 210 | $C_L = 50$pF |
| $t_{RDL}$ | Propagation delay of a valid low level on $\overline{CS}$ to a valid low level on $\overline{RDY}$. | | 90 | $C_L = 50$pF |
| $t_{WHO}$ | Hold time of a valid high or low level of $\overline{WR}$ to a valid high level of $\overline{DS1}$ and $\overline{DS2}$. | 10 | | |
| $t_{WSU}$ | Setup time of a valid high or low level of $\overline{WR}$ to the falling edge of $\overline{DS1}$ or $\overline{DS2}$. | 30 | | |

[1]Refer to Figure 9 for the load circuits used with these measurements.
[2]The $t_{DDLZ}$ and $t_{DDHZ}$ parameters are measured with $C_L = 150$ pF. The values of $t_{DDLZ}$ and $t_{DDHZ}$ for $C_L = 50$pF and $C_L = 100$ pF have been derived for user convenience.
[3]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The $t_{ID}$ parameter can be calculated by the following: $t_{ID} = 500 + RC_L$ where R = value of the resistor that connects to capacitor $C_L$ in load A, Figure 9.
[4]Total rise time depends on internal delay plus the pullup delay introduced by the external resistor being used. The $t_{RDH}$ parameter can be calculated by the following: $t_{RDH} = 75 + RC_L$ where R = value of the resistor that connects to capacitor $C_L$ in load A, Figure 9.

Figure 12 shows the signal timing for the clock input, interrupt timing, effect of the $\overline{RESET}$ input on data strobe, data set carrier detect (DCD) and data set ready (DSR) input timing, and the transmit data output timing. Table 11 lists the timing parameters for Figure 12.

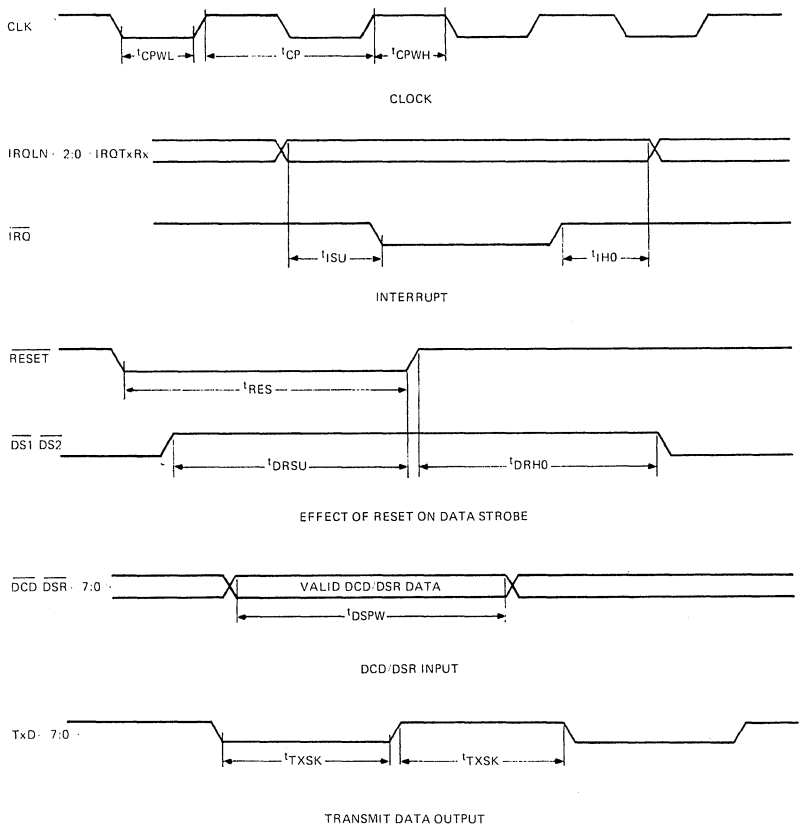



**FIGURE 12–COM78808 MISCELLANEOUS SIGNAL TIMING**

## TABLE 11–MISCELLANEOUS WRITE TIMING PARAMETERS

| Symbol | Definition | Requirements (ns) Min. | Load Circuit[1] |
|---|---|---|---|
| $t_{CP}$ | Period of CLK. | 203.45 (4.9152 MHz) | |
| $t_{CPWH}$ | Pulse width high of CLK. | 95 | |
| $t_{CPWL}$ | Pulse width low of CLK. | 95 | |
| $t_{DRHO}$ | Hold time of a valid high level of $\overline{DS1}$ and $\overline{DS2}$ to a valid high level of $\overline{RESET}$. | 1,000 | |
| $t_{DRSU}$ | Setup time of a valid high level of $\overline{DS1}$ and $\overline{DS2}$ to the rising edge of $\overline{RESET}$. | 900 | |
| $t_{DSPW}$ | Pulse width high or low of DCD <7:0> and DSR <7:0> | 1,000 | |
| $t_{IHO}$ | Hold time provided by Octal UART from a valid IRQLN <2:0> and IRQTxRx to a valid high level of IRQ. | 100 | $C_L = 50pF$ |
| $t_{ISU}$ | Setup time provided by Octal UART from a valid IRQLN <2:0> and IRQTxRx to a valid low level of $\overline{IRQ}$. | 100 | $C_L = 50pF$ |
| $t_{RES}$ | Pulse width low of $\overline{RESET}$. | 1,000 | |
| $t_{TXSK}$ | Pulse width high or low provided by Octal UART on the TxD <7:0> lines. At each baud rate, the actual pulse widths provided vary by $t_{TXSK}$. This timing parameter should be used to determine cumulative reception/transmission errors. | 250 | $C_L = 50pF$ |

*Refer to Figure 9 for the load circuits used with these measurements.

Figure 13 shows the input and output voltage waveforms for the propagation delay and setup and hold measurements. Figure 14 shows the waveforms for the three-state outputs measurement.

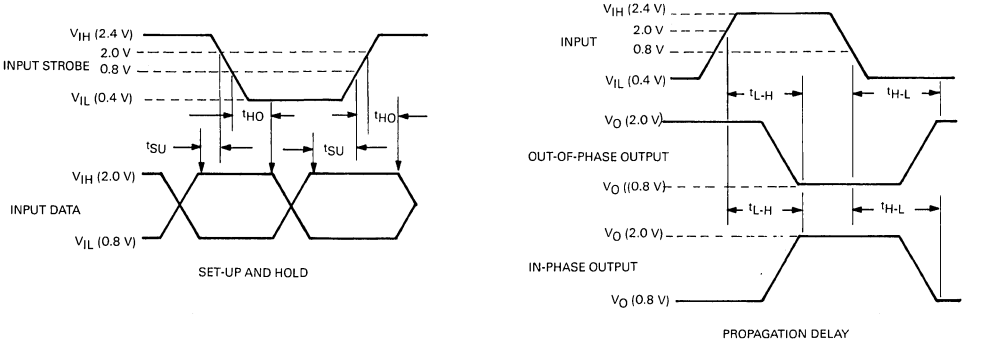
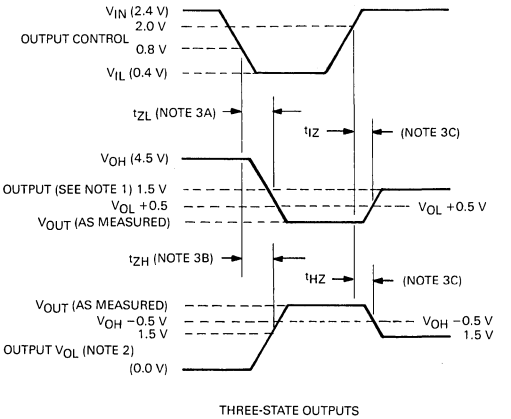



**FIGURE 13–COM78808 PROPAGATION DELAY AND SETUP AND HOLD VOLTAGE WAVEFORMS**

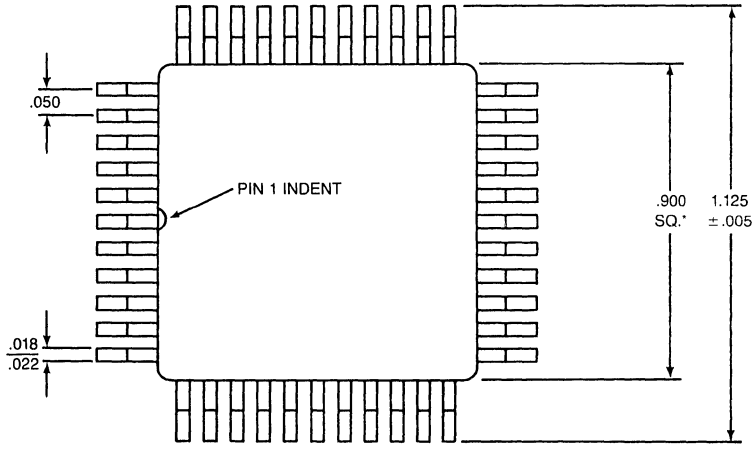



NOTES:
1. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
2. INTERNAL CONDITIONS ARE SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.
3. REFER TO FIGURE 9. A = S1 CLOSED, B = S2 CLOSED, C = S1 AND S2 CLOSED.

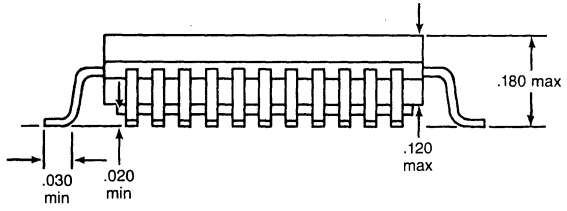
**FIGURE 14–COM78808 THREE-STATE OUTPUT VOLTAGE WAVEFORMS**

# APPENDIX E

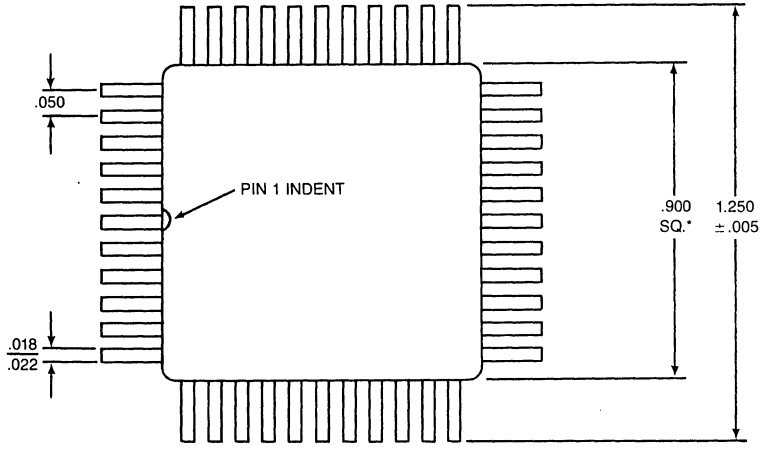
68 LEADED CERQUAD GULLWING VERSION (GA)



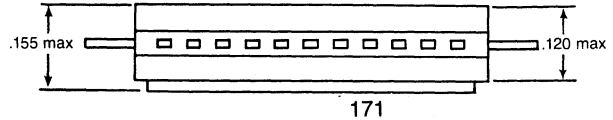

*DEFINES MINIMUM CLEAR LEADFRAME ZONE –zone consists of package body, including ceramic and glass.




68 LEADED CERQUAD FLAT LEAD VERSION (FA)




*DEFINES MINIMUM CLEAR LEADFRAME ZONE –zone consists of package body, including ceramic and glass.



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

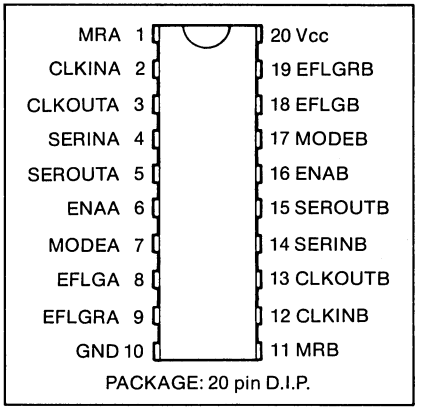
# Dual 32 Bit CRC SDLC Generator/Checker CRC-32



## FEATURES

- ☐ SDLC 32 bit CRC
- ☐ COM 5025 USYNRT Companion
- ☐ Data Rate—2MHz typical
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N-Channel MOS Technology

## PIN CONFIGURATION




PACKAGE: 20 pin D.I.P.

## GENERAL DESCRIPTION

SMC's COM 8004 is a dual 32-bit CRC Generator/Checker for use with SDLC protocols. It is a companion device to SMC's COM 5025 USYNRT. It operates at bit rates from DC to 2.0 MHz from a single +5v supply and is housed in a 20 lead x 0.3 inch DIP. All inputs and outputs are TTL compatible with full noise immunity.

The COM 8004 is comprised of two independent halves, and each half may be operated in the check or generate mode. The polynominal used in computations is:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.

The CRC register is initialized to all ones and the result is inverted before being appended to the message. The expected remainder is:
$X^{31} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^4 + X^3 + X + 1$.

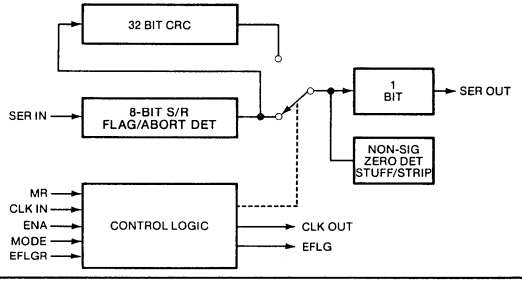
Each half has a nine-bit serial data shift register. Data moves on the positive edge of the clock, and all clocked inputs are designed for zero-hold-time (e.g. 7474). A "clock out" pin provides gated clocks to the accompanying USYNRT (COM 5025).

In the generate mode, computation is initiated upon detection of a flag character in the serial bit stream. CRC computation proceeds upon the serial data until a second flag is detected. CLK OUT to the SDLC transmitter is then halted, and the 32-bit CRC is passed out; CLK OUT is then resumed, and the flag character is passed out. Nonsignificant zeros are automatically stripped and stuffed, and shared flags are supported. If the data between flags is less than two full bytes, the CRC is discarded and the serial data stream remains unaltered.

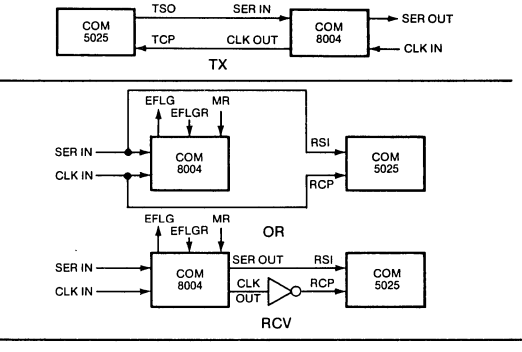
In the check mode, computation is similarly initiated upon detection of a flag. Detection of a second flag causes the conditional setting of the error flag. A separate reset pin is provided for the error flag. No error is flagged on messages of less than two full bytes between flags. Detection of an abort character (7 consecutive ones) in either mode causes computation to be reset and a search for an opening flag resumed.

## BLOCK DIAGRAM

FOR ONE-HALF OF THE COM 8004




## TYPICAL SYSTEM



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | MASTER RESET-A | MRA | MRA presets the CRC calculation in Section A of the COM 8004 to all ones and forces the "pipeline" (8 shift register bits and the output flip-flop) to a logic "1" (Mark). The COM 8004 will only exit the reset state when MRA has been released and all 8 bits of a FLAG (01111110) have been received. |
| 2 | CLOCK INPUT-A | CLKINA | Baud Rate Clock for Section A. |
| 3 | CLOCK OUTPUT-A | CKLOUTA | Clock output from Section A. This is used to provide the clock for the USYNRT. CLKOUTA will normally track CLKINA. In the generate mode, when the last flag bit has been shifted into the shift register of the COM 8004, CLKOUTA will be held high until the CRC check character has been sent out. After the last bit of the CRC character is transmitted, CLKOUTA will resume tracking CLKINA. |
| 4 | SERIAL INPUT-A | SERINA | Serial input to the COM 8004 Section A. For transmission, SERINA is connected to the transmitter serial output of the USYNRT. For receiving, SERINA is connected to the received data output of the modem. |
| 5 | SERIAL OUTPUT-A | SEROUTA | Serial output from Section A of the COM 8004. For transmission, SEROUTA is connected to the transmit data input of the modem. For receiving, SEROUTA may be connected to the serial data input of the USYNRT. |
| 6 | ENABLE-A | ENAA | When ENAA is low, section A of the COM 8004 will pass data from SERINA to SEROUTA after a nine bit delay without alteration and without checking or generating CRC. If ENAA is high, CRC generation or checking will be enabled. ENAA is gated into the COM 8004 by the rising edge of CLKINA. |
| 7 | MODE SELECT-A | MODEA | MODEA determines whether Section A of the COM 8004 is in the receive (CRC check) Mode or transmit (CRC generate) Mode. Logic "1" selects CRC check. Logic "0" selects CRC generate. |
| 8 | ERROR FLAG-A | EFLGA | EFLGA will go high if, when in the CRC check mode, section A of the COM 8004 has detected an error. EFLGA can only be reset by a MASTER RESET (MRA) or by ERROR FLAG RESET (EFLGRA). |
| 9 | ERROR FLAG RESET-A | EFLGRA | A logic "1" on EFLGRA will reset EFLGA. If EFLGRA is kept at a logic "1," it will inhibit the setting of EFLGA. |
| 10 | GROUND | GND | Ground. |
| 11 | MASTER RESET-B | MRB | Master reset for Section B. See MRA for description. |
| 12 | CLOCK IN-B | CLKINB | Clock input for Section B. See CLKINA for description. |
| 13 | CLOCK OUT-B | CLKOUTB | Clock output for Section B. See CLKOUTA for description. |
| 14 | SERIAL INPUT-B | SERINB | Serial input for Section B. See SERINA for description. |
| 15 | SERIAL OUTPUT-B | SEROUTB | Serial output for Section B. See SEROUTA for description. |
| 16 | ENABLE-B | ENAB | CRC enable for Section B. See ENAA for description. |
| 17 | MODE SELECT-B | MODEB | Mode select for Section B. See MODEA for description. |
| 18 | ERROR FLAG-B | EFLGB | Error Flag for Section B. See EFLGA for description. |
| 19 | ERROR FLAG RESET-B | EFLGRB | Error flag reset for Section B. See EFLGRA for description. |
| 20 | POWER SUPPLY | $V_{CC}$ | +5 volt power supply input. |

## OPERATION

The COM 8004 has 3 modes of operation, as selected by the ENABLE and MODE SELECT inputs. They are:

| ENABLE | MODE SELECT | |
|---|---|---|
| 0 | 0 | CRC Disabled. Data is shifted from SERIN to SEROUT with no computation performed. Serial delay is 9 bit times. |
| 0 | 1 | Same as above. |
| 1 | 0 | CRC generation mode. |
| 1 | 1 | CRC check mode. |

In the CRC generation and check modes, calculations begin upon receipt of the first data character after an opening FLAG. "Stuffed zeroes" are stripped for the purpose of the CRC calculation. CRC calculation will continue until either a MASTER RESET occurs, ENABLE is brought to logic zero, an ABORT character is received, or a closing FLAG is received.

### CRC Generation

Upon detection of a closing FLAG character, CLKOUT is left high (stopping USYNRT activity), and the CRC accumulation is shifted out by CLKIN. CLKOUT then resumes clocking, and the FLAG (which has been stored in the shift register) is shifted out. The CRC check data is inverted before this data is transmitted. Zero-stuffing is performed on the inverted CRC check data.

During the time CKLOUT is forced high and CRC check data is being shifted out, data on SERIN will be ignored.

If an ABORT character is received, CRC calculation will cease after the last "1" bit of the ABORT character is shifted into the shift register. Data will pass through the COM 8004 without effect until a FLAG is received.

### CRC Check (Reception)

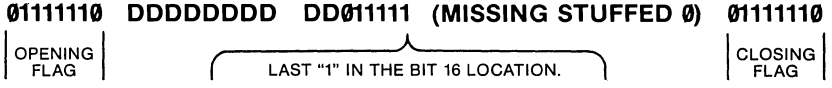
When the last bit of a closing flag enters the shift register, ERRCHK will go high on the following positive CLKIN transition if a CRC error is detected.

SECTION III

### Operation Notes

**Note 1:** The minimum message size is sixteen significant bits following an opening flag. A stuffed zero is not considered a significant bit. If the message is less than 16 bits, the data will pass through the COM 8004 without being affected.

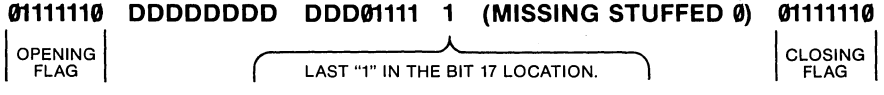
If the sixteenth received bit is the fifth consecutive one, but is not followed by a stuffed zero before a FLAG, the COM 8004 will detect the FLAG but the minimum message will not have occurred. CRC calculation will begin anew after this FLAG is detected.




**Note 2:** If the seventeenth bit of a message followed by a FLAG is the fifth consecutive one, but the stuffed zero is missing, the following will occur:

A) CRC Generate Mode: The last "one" bit, bit 17, will not be calculated into the CRC, but will appear at the serial output. The first bit of the CRC character will be forced to a zero, therefore looking like a stuffed zero.

B) CRC Check Mode: The last "one" bit, bit 17, will not be calculated into the CRC.




**Note 3:** If a stuffed zero is missing in the middle or end of a message, the reaction will depend on the next bit. If it is a one, a FLAG or ABORT may be detected. If an ABORT is detected, the message and the CRC checking is aborted. If a FLAG is detected, a CRC error will be detected.

If the missing zero is followed by a zero, the CRC computation will continue, but the zero bit will be stripped, causing a CRC error.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**PRELIMINARY**
Notice: This is not a final specification.
Some parametric limits are subject to change.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5 Volts ±5%, unless otherwise noted)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| Input Voltage Levels | | | | | | |
| Low Level | $V_{IL}$ | | | 0.8 | V | |
| High Level | $V_{IH}$ | 2.0 | | | V | |
| Output Voltage Levels | | | | | | |
| Low Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| High Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -100 μA |
| Input Capacitance | $C_{IN}$ | | 10 | 25 | pf | |
| Power Supply Current | $I_{CC}$ | | | 100 | mA | |
| **AC CHARACTERISTICS** | | | | | | $T_A$ = 25°C |
| Clock Frequency | $f_{IN}$ | | | 2 | MHz | |
| Clock Pulse Width—High | $t_{CLKH}$ | 350 | | | ns | Figure 1 |
| Input Set-Up Time | $t_{DC}$ | 100 | | | ns | Figure 1 |
| Input Hold Time | $t_{CD}$ | 0 | | | ns | Figure 1 |
| Master Reset Pulse Width | $t_{PW}$ | 250 | | | ns | Figure 2 |
| Reset Delay | $t_{MR}$ | | | 250 | ns | Figure 2 |
| Error Flag Delay | $t_{FD}$ | | | 300 | ns | Figure 3 |
| Error Flag Reset Delay | $t_{FR}$ | | | 100 | ns | Figure 4 |
| ERRST Pulse Width | $t_{EW}$ | 100 | | | ns | Figure 4 |
| Clock Propagation Delay | $t_{PD}$ | | | 150 | ns | Figure 5 |
| SEROUT Propagation Delay | $t_{SD}$ | | | 150 | ns | Figure 5 |

**Figure 1**

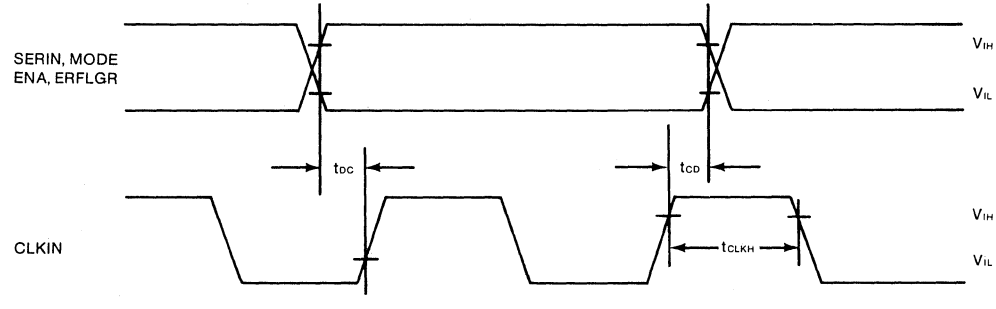


**Figure 2**

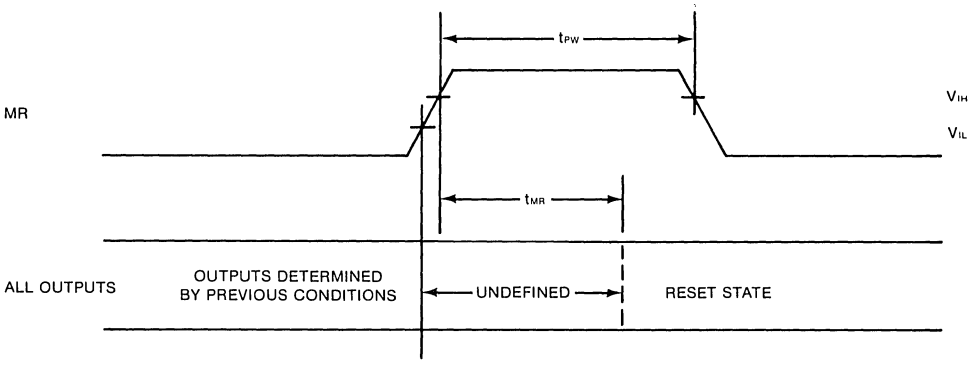



**Figure 3**

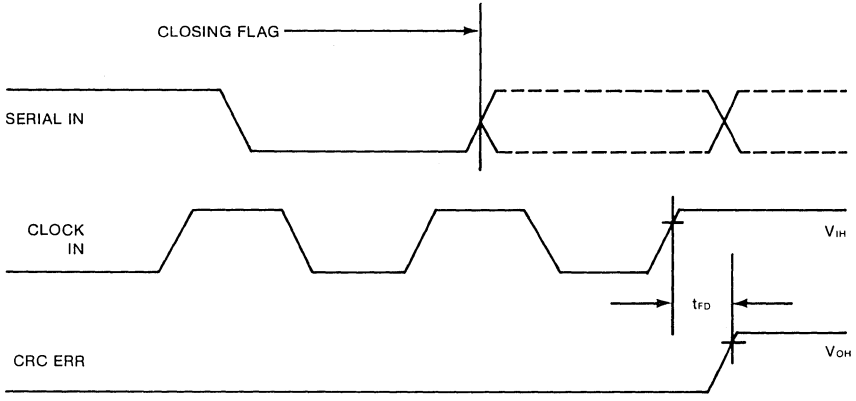



**Figure 4**

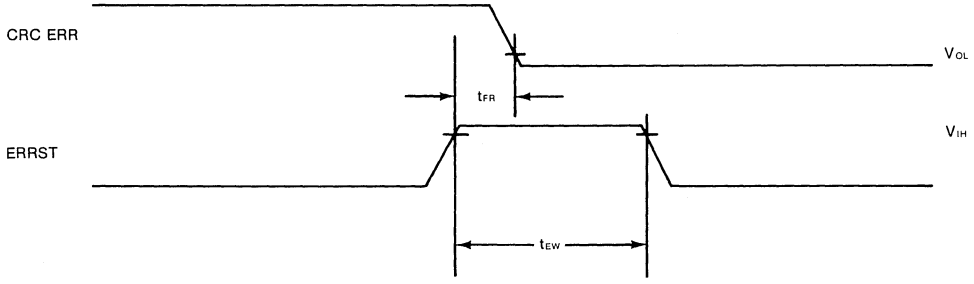
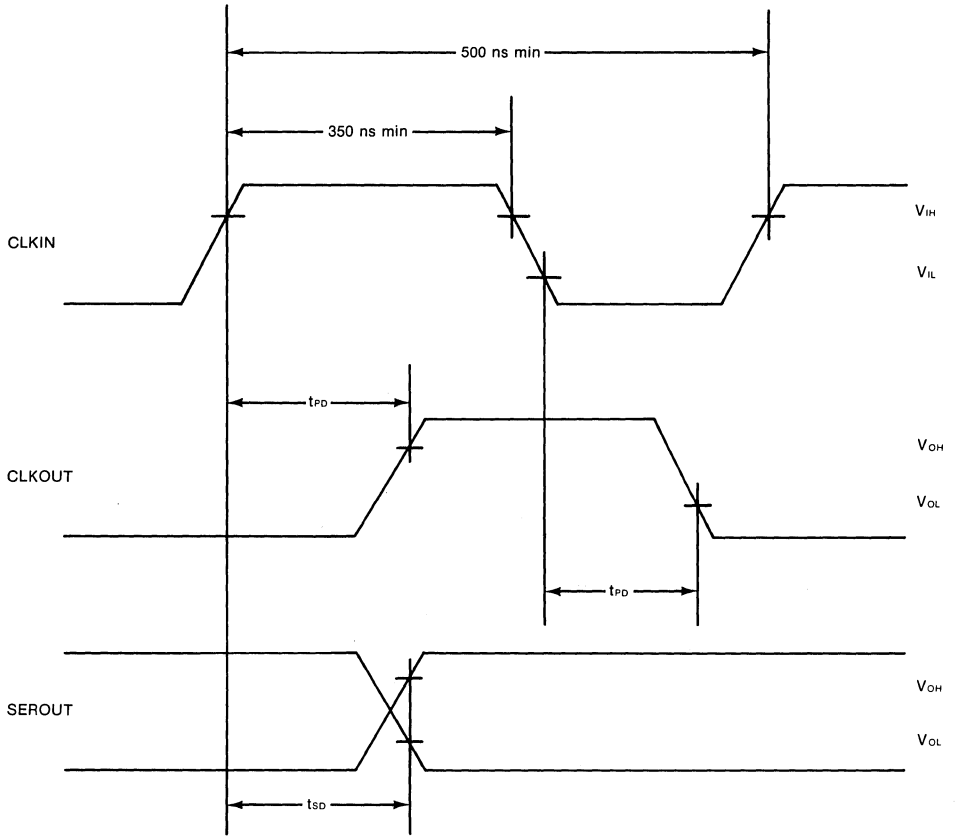


**Figure 5**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

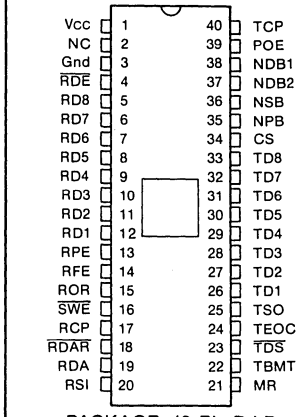
STANDARD MICROSYSTEMS CORPORATION

# COM 8017
# COM 8502

# Universal Asynchronous Receiver/Transmitter
# UART



**Pin Configuration**

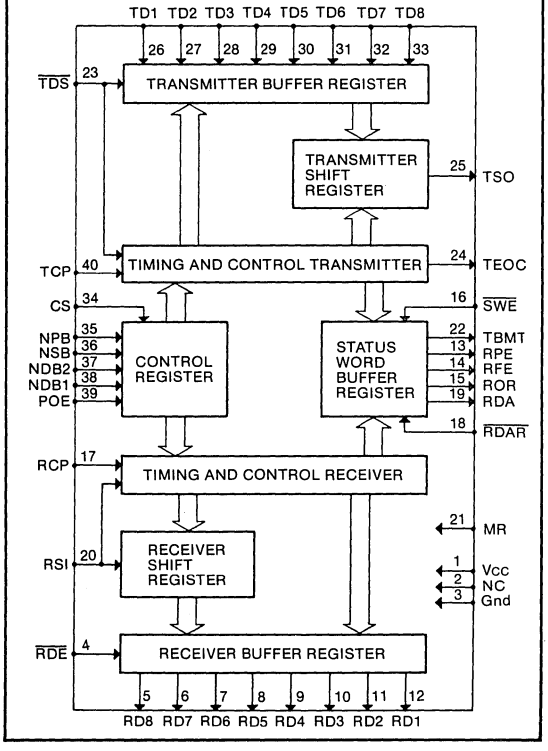



PACKAGE: 40-Pin D.I.P.

## FEATURES

- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Start Bit Verification—decreases error rate
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ High Speed Operation—40K baud, 200ns strobes
- ☐ Master Reset—Resets all status outputs
- ☐ Tri-State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic Dip Package—easy board insertion
- ☐ Compatible with COM 2017, COM 2502
- ☐ Compatible with COM 8116, COM 8126, COM 8136, COM 8146, COM 8046 Baud Rate Generators

**Functional Block Diagram**




## GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits. In addition the COM 8017 will provide 1.5 stop bits when programmed for 5 data bits and 2 stop bits. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

## DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

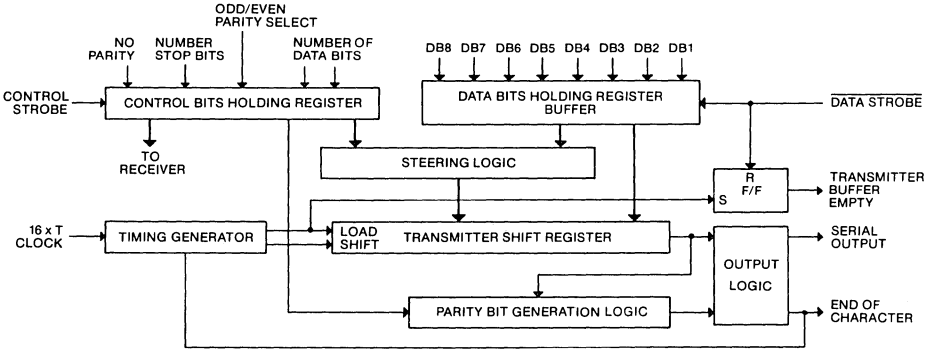
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

### TRANSMITTER BLOCK DIAGRAM




## DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

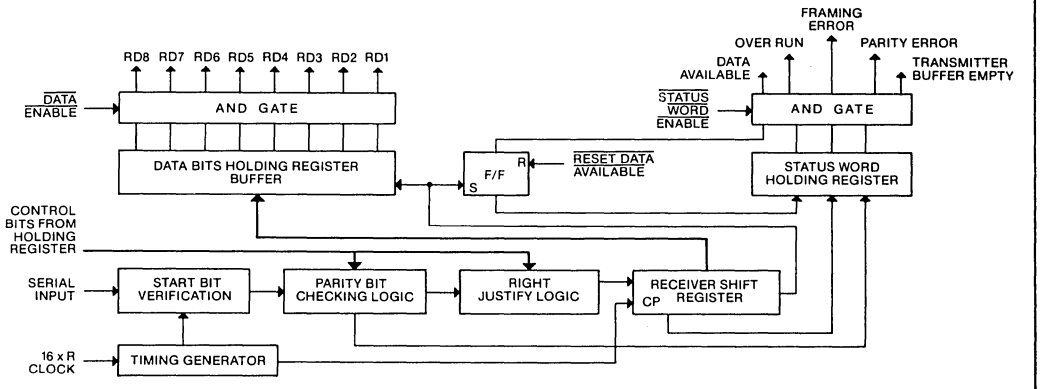
status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.



**RECEIVER BLOCK DIAGRAM**




**DESCRIPTION OF PIN FUNCTIONS**

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | Vcc | Power Supply | +5 volt Supply |
| 2 | NC | No Connection | No Connection |
| 3 | GND | Ground | Ground |
| 4 | $\overline{RDE}$ | Received Data Enable | A low-level input enables the outputs (RD8-RD1) of the receiver buffer register. |
| 5-12 | RD8-RD1 | Receiver Data Outputs | These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output. |
| 13 | RPE | Receiver Parity Error | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity. |
| 14 | RFE | Receiver Framing Error | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit. |

## DESCRIPTION OF PIN FUNCTIONS

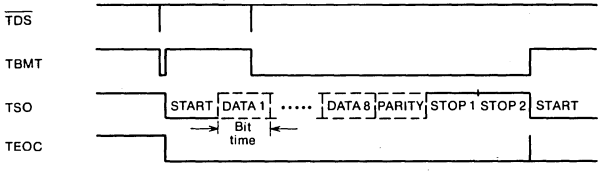
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 15 | ROR | Receiver Over Run | This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register. |
| 16 | $\overline{SWE}$ | Status Word Enable | A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register. |
| 17 | RCP | Receiver Clock | This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate. |
| 18 | $\overline{RDAR}$ | Receiver Data Available Reset | A low-level input resets the RDA output to a low-level. |
| 19 | RDA | Receiver Data Available | This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register. |
| 20 | RSI | Receiver Serial Input | This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception. |
| 21 | MR | Master Reset | This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level. |
| 22 | TBMT | Transmitter Buffer Empty | This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data. |
| 23 | $\overline{TDS}$ | Transmitter Data Strobe | A low-level input strobe enters the data bits into the transmitter buffer register. |
| 24 | TEOC | Transmitter End of Character | This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission. |
| 25 | TSO | Transmitter Serial Output | This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted. |
| 26-33 | TD1-TD8 | Transmitter Data Inputs | There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1. |
| 34 | CS | Control Strobe | A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level. |
| 35 | NPB | No Parity Bit | A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE. |

## DESCRIPTION OF PIN FUNCTION

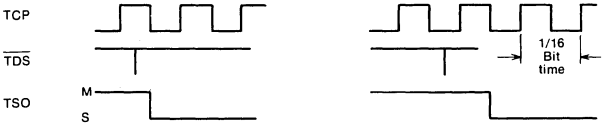
| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 36 | NSB | Number of Stop Bits | This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 8017 or COM 8017/H. |
| 37-38 | NDB2, NDB1 | Number of Data Bits/Character | These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table:<br>NDB2 NDB1 data bits/character<br>L L 5<br>L H 6<br>H L 7<br>H H 8 |
| 39 | POE | Odd/Even Parity Select | The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table:<br>NPB POE MODE<br>L L odd parity<br>L H even parity<br>H X no parity<br>X = don't care |
| 40 | TCP | Transmitter Clock | This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate. |



### TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

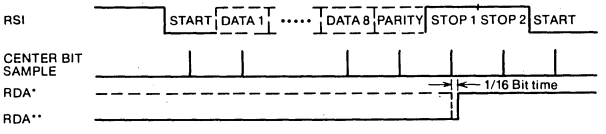



### TRANSMITTER START-UP




Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of $\overline{TDS}$.

### RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS




*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

### START BIT DETECT/VERIFY


If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin. with respect to ground ..... −0.3V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | 0 | | 0.8 | V | |
| High-level, $V_{IH}$ | 2.0 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL} = 1.6mA$ |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH} = -100\mu A$ |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | 300 | $\mu A$ | $V_{IN} = GND$ |
| OUTPUT CURRENT | | | | | |
| Leakage, $I_{LO}$ | | | $\pm 10$ | $\mu A$ | $\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$ |
| Short circuit, $I_{OS}$** | | | 30 | mA | $V_{OUT} = 0V$ |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pf | |
| OUTPUT CAPACITANCE | | | | | |
| All outputs, $C_{OUT}$ | | 10 | 20 | pf | $\overline{SWE} = \overline{RDE} = V_{IH}$ |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 25 | mA | All outputs = $V_{OH}$, All inputs = $V_{CC}$ |
| **A.C. CHARACTERISTICS** | | | | | $T_A = +25°C$ |
| CLOCK FREQUENCY | | | | | |
| COM8502, COM 8017 | DC | | 640 | KHz | RCP, TCP |
| PULSE WIDTH | | | | | |
| Clock | 0.7 | | | $\mu s$ | RCP, TCP |
| Master reset | 500 | | | ns | MR |
| Control strobe | 200 | | | ns | CS |
| Transmitter data strobe | 200 | | | ns | $\overline{TDS}$ |
| Receiver data available reset | 200 | | | ns | $\overline{RDAR}$ |
| INPUT SET-UP TIME | | | | | |
| Data bits | $\geq 0$ | | | ns | TD1-TD8 |
| Control bits | $\geq 0$ | | | ns | NPB, NSB, NDB2, NDB1, POE |
| INPUT HOLD TIME | | | | | |
| Data bits | $\geq 0$ | | | ns | TD1-TD8 |
| Control bits | $\geq 0$ | | | ns | NPB, NSB, NDB2, NDB1, POE |
| STROBE TO OUTPUT DELAY | | | | | Load = 20pf +1 TTL input |
| Receive data enable | | | 350 | ns | $\overline{RDE}$: $T_{PD1}$, $T_{PD0}$ |
| Status word enable | | | 350 | ns | $\overline{SWE}$: $T_{PD1}$, $T_{PD0}$ |
| OUTPUT DISABLE DELAY | | | 350 | ns | $\overline{RDE}$, $\overline{SWE}$ |

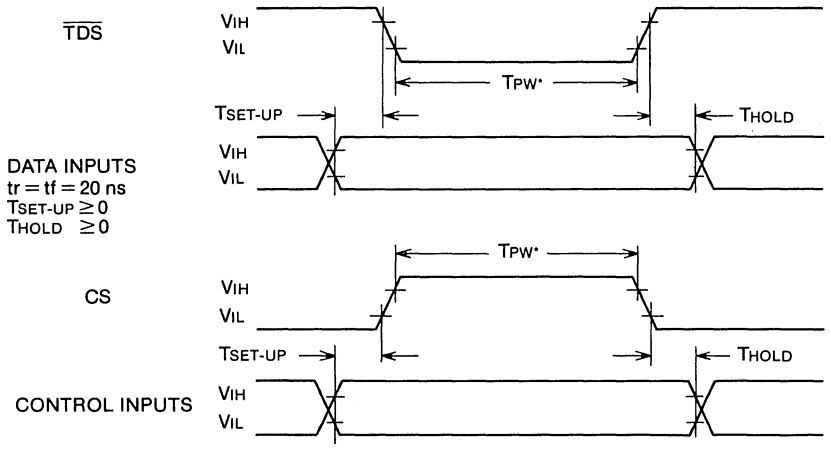
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

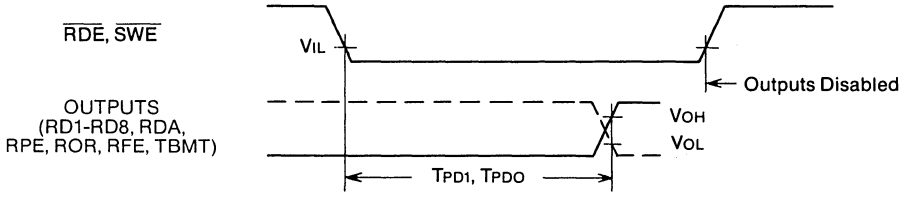
3. The tri-state output has 3 states: 1) low impedance to $V_{CC}$ 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

## DATA/CONTROL TIMING DIAGRAM

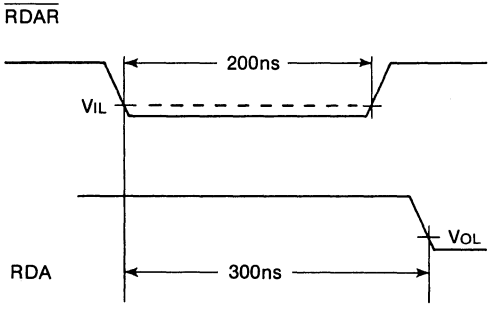


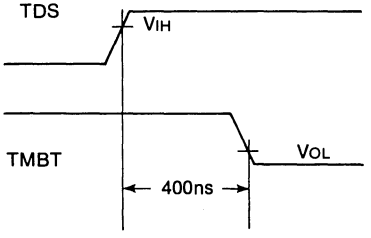

*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

## OUTPUT TIMING DIAGRAM

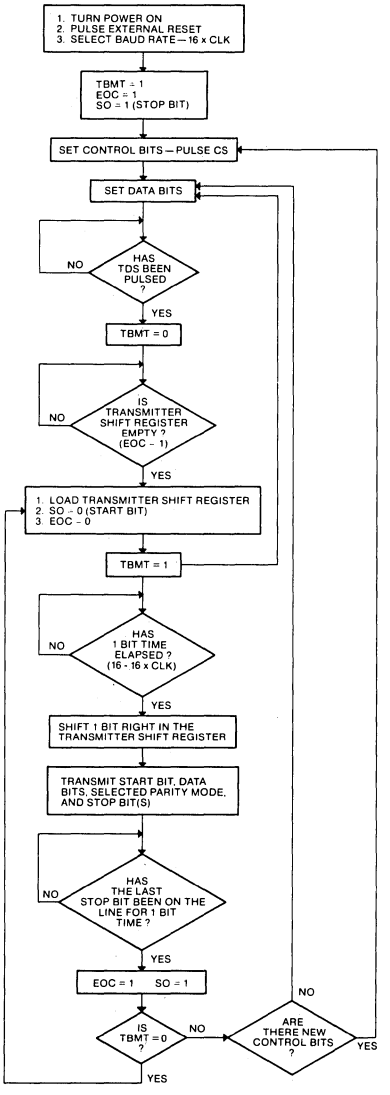



NOTE: Waveform drawings not to scale for clarity.

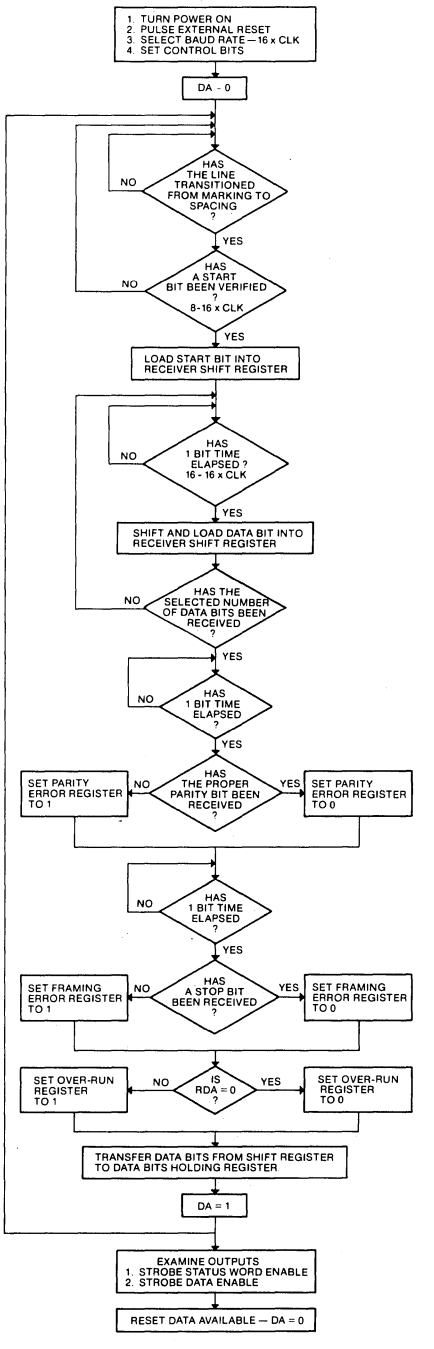


## FLOW CHART—TRANSMITTER




## FLOW CHART—RECEIVER




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**COM81C17**
**PRELIMINARY**

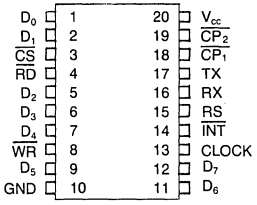
# Universal Asynchronous Receiver Transmitter UART



## FEATURES

- ☐ Single chip UART with Baud Rate Generator
- ☐ Choice of 16 Baud Rates
- ☐ Low power CMOS
- ☐ Available in 20-pin Dual-In-Line package
- ☐ Full or half duplex operation
- ☐ Fully double buffered
- ☐ Programmable interrupt generation
- ☐ Programmable modem/terminal handshake signals
- ☐ Single +5 Volt power supply

## PIN CONFIGURATION*



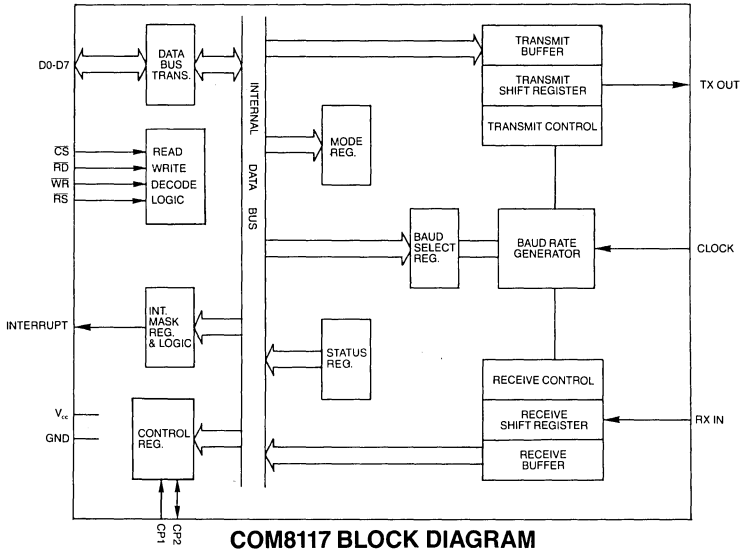

PACKAGE: 20-pin D.I.P.

*PLCC PACKAGE AVAILABLE.

## GENERAL DESCRIPTION

The TPUART is an asynchronous only receiver transmitter with a built-in programmable baud rate generator housed in a twenty pin package. The TPUART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the TPUART will also accept data characters from the processor in parallel format and convert them into serial format along with start, stop and optional parity bits.

The TPUART will signal the processor via interrupt when it has completely transmitted or received a character and requires service. Complete status information is available to the processor through the status register. The TPUART features two general purpose control pins that can be individually programmed to perform as terminal or modem control handshake signals.




COM8117 BLOCK DIAGRAM

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications: consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM 8251A
## μPC FAMILY

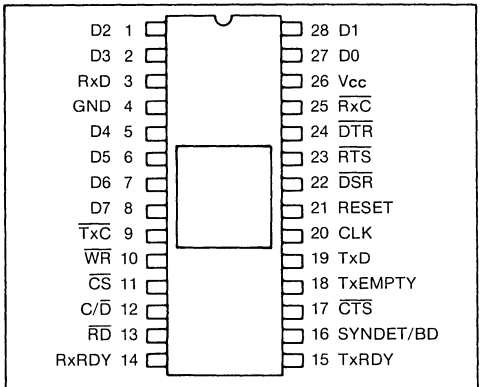
SECTION III

# Universal Synchronous/Asynchronous Receiver/Transmitter USART

## FEATURES

- ☐ Asynchronous or Synchronous Operation
  - —Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate—1, 16 or 64 X Baud Rate
    - Break Character Generation
    - 1, 1½ or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
  - —Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
    - Programmable Sync Character(s)
- ☐ Baud Rate—Synchronous—DC to 64K Baud
  —Asynchronous—DC to 19.2K Baud
- ☐ Baud Rates available from SMC's COM 8116, COM 8126, COM 8136, COM 8146, and COM 8046
- ☐ Full Duplex, Double Buffered Transmitter and Receiver
- ☐ Odd parity, even parity or no parity bit
- ☐ Parity, Overrun and Framing Error Flags
- ☐ Modem Interface Controlled by Processor
- ☐ All Inputs and Outputs are TTL Compatible

## PIN CONFIGURATION




PACKAGE: 28-pin D.I.P.

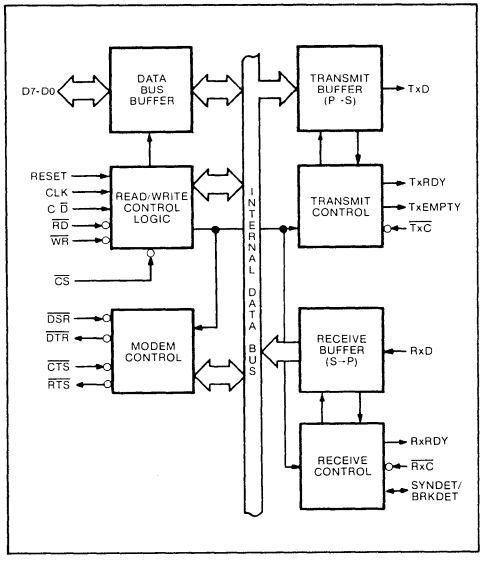
- ☐ Compatable with Intel 8251A, NEC μPD8251A
- ☐ Single +5 Volt Supply
- ☐ Separate Receive and Transmit TTL Clocks
- ☐ Enhanced version of 8251
- ☐ 28 Pin Plastic or Ceramic DIP Package
- ☐ COPLAMOS® N-Channel MOS Technology

## GENERAL DESCRIPTION

The COM 8251A is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 8251A is an enhanced version of the 8251.

The COM 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asychronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status, including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

## BLOCK DIAGRAM



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 1, 2, 27, 28, 5-8 | D2, D3, D0, D1, D4-D7 | DATA BUS | I/O | An 8-bit, 3-state bi-directional DATA BUS used to interface the COM 8251A to the processor data bus. Data is transmitted or received by the bus in response to input/output or Read/Write instructions from the processor. The DATA BUS also transfers Control words, Command words, and Status. |
| 3 | RxD | RECEIVER DATA | I | This input receives serial data into the USART. |
| 4 | GND | GROUND | GND | Ground |
| 9 | $\overline{TxC}$ | $\overline{TRANSMITTER\ CLOCK}$ | I | The $\overline{TRANSMITTER\ CLOCK}$ controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1X, 16X, or 64X the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate.<br>Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$. |
| 10 | $\overline{WR}$ | $\overline{WRITE\ DATA}$ | I | A "zero" on this input instructs the COM 8251A to accept the data or control word which the processor is writing out to the USART via the DATA BUS. |
| 11 | $\overline{CS}$ | $\overline{CHIP\ SELECT}$ | I | A "zero" on this input enables the USART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip. |
| 12 | C/$\overline{D}$ | CONTROL/$\overline{DATA}$ | I | The Control/$\overline{Data}$ input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the DATA BUS. 0 = Data; 1 = Control/Status |
| 13 | $\overline{RD}$ | $\overline{READ\ DATA}$ | I | A "zero" on this input instructs the COM 8251A to place the data or status information onto the DATA BUS for the processor to read. |
| 14 | RxRDY | RECEIVER READY | O | The RECEIVER READY output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY. |
| 15 | TxRDY | TRANSMITTER READY | O | TRANSMITTER READY signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information polled operaton. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the processor. |
| 16 | SYNDET/ BRKDET | SYNC DETECT/ BREAK DETECT | I/O | The SYNDET feature is only used in the Synchronous mode. The USART may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal SYNC mode, the SYNDET output will go to a "one" when the COM 8251A has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second contiguously detected SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input is sampled during the negative half cycle of $\overline{RxC}$ and will cause the COM 8251A to start assembling data character on the next rising edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the COM 8251A is in SYNC. When external SYNC DETECT is programmed, the internal SYNC DETECT is disabled. |

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 16 (cont.) | | | | The SYNDET/BRKDET pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the BREAK DETECT output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx Data returns to a logic one state or upon chip RESET. The state of BREAK DETECT can also be read as a status bit. |
| 17 | $\overline{CTS}$ | $\overline{CLEAR\ TO\ SEND}$ | I | A "zero" on the $\overline{CLEAR\ TO\ SEND}$ input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).<br>If either a TxEN off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART written prior to the Tx Disable command before shutting down. |
| 18 | TxE | TRANSMITTER EMPTY | O | The TRANSMITTER EMPTY output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around". The TxEN bit in the command instruction does not effect TxE.<br>In the Synchronous mode, a "one" on this output indicates that a SYNC character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded; an underflow condition. If the USART is operating in the two SYNC character mode, both SYNC characters will be transmitted before the message can resume. TxE does not go low when the SYNC characters are being shifted out. TxE goes low upon the processor writing a character to the USART. |
| 19 | TxD | TRANSMITTER DATA | O | This output is the transmitted serial data from the USART. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed. |
| 20 | CLK | CLOCK PULSE | I | The CLK input provides for internal device timing. External inputs and outputs are not referenced to CLK, but the CLK frequency must be greater than 30 times the RECEIVER or TRANSMITTER CLOCKS in the 1X mode and greater than 4.5 times for the 16X and 64X modes. |
| 21 | RESET | RESET | I | A "one" on this input forces the USART into the "idle" mode where it will remain until reinitialized with a new set of control words. RESET causes: $\overline{RxRDY}$ = TxRDY = TxEmpty = SYNDET/ BRKDET = 0; TxD = $\overline{DTR}$ = $\overline{RST}$ = 1. Minimum RESET pulse width is 6 $t_{CY}$, CLK must be running during RESET. |
| 22 | $\overline{DSR}$ | $\overline{DATA\ SET\ READY}$ | I | The $\overline{DATA\ SET\ READY}$ input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition. |
| 23 | $\overline{RTS}$ | $\overline{REQUEST\ TO\ SEND}$ | O | The $\overline{REQUEST\ TO\ SEND}$ output is controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line. |
| 24 | $\overline{DTR}$ | $\overline{DATA\ TERMINAL\ READY}$ | O | The $\overline{DATA\ TERMINAL\ READY}$ output is controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines. |
| 25 | $\overline{RxC}$ | $\overline{RECEIVER\ CLOCK}$ | I | The $\overline{RECEIVER\ CLOCK}$ is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1X, 16X or 64X or Synchronous operation at 1X the Baud Rate.<br>Data is sampled into the USART on the rising edge of $\overline{RxC}$. |
| 26 | $V_{CC}$ | $V_{CC}$ SUPPLY VOLTAGE | PS | +5 volt supply |

## DESCRIPTION OF OPERATION—ASYNCHRONOUS

**Transmission—**

When a data character is written into the USART, it automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at a transmission rate of $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

**Receive—**

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge (high to low transition) at RxD signals the possible beginning of a START bit and a new character. The receiver is thus prevented from starting in a "BREAK" state. The START bit is verified by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After the STOP bit time, the input character is loaded into the paralled Data Bus Buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

## DESCRIPTION OF OPERATION—SYNCHRONOUS

**Transmission—**

As in Asynchronous transmission, the TxD output remains "high" (marking) until the USART receives the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ at the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Data Protocols require that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the USART Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until the new data characters are available for transmission. If the USART becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

**Receive—**

In Synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, the ENTER HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the contents of the Receive Buffer are compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the (two contiguous) SYNC character(s) programmed have been detected, the USART leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost. Under this condition the Rx register will be cleared to all "ones".

## OPERATION AND PROGRAMMING

The microprocessor program controlling the COM 8251A performs these tasks:

- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which has been received

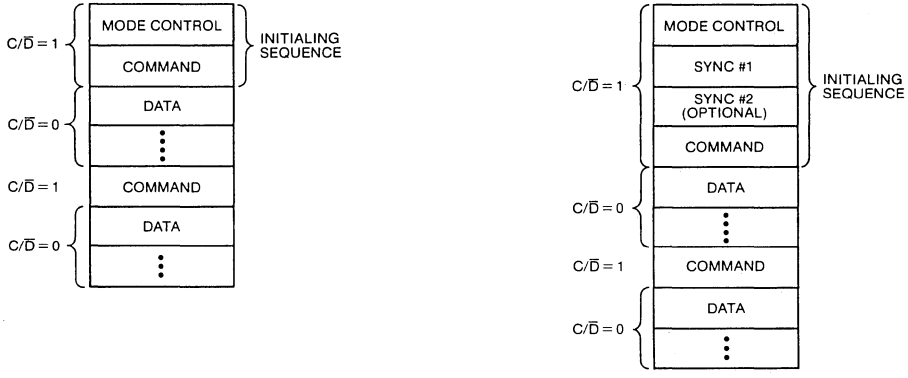
Control codes determine the mode in which the COM 8251A will operate and are used to set or reset control signals output by the COM 8251A.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.



## INITIALIZING THE COM 8251A

**Figure 1. Control Word Sequences for Initialization**




The COM 8251A may be initialized following a system RESET or prior to starting a new seral I/O sequence. The USART must be RESET (external or internal) following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the COM 8251A enters an idle state in which it can neither transmit nor receive data.

The COM 8251A is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the COM 8251A, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a RESET (external or internal), the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following a RESET input or following an internal reset command. A reset operation (internal via IR or external via RESET) will cause the USART to interpret the next "control write", which should immediately follow the reset, as a Mode Instruction.

After receiving the control words the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. Concurrently, the USART is ready to receive serial data.

| C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | USART → Data Bus |
| 0 | 1 | 0 | 0 | Data Bus → USART |
| 1 | 0 | 1 | 0 | Status → Data Bus |
| 1 | 1 | 0 | 0 | Data Bus → Control |
| X | X | X | 1 | Data Bus → 3-State |
| X | 1 | 1 | 0 | |

## MODE CONTROL CODES

The COM 8251A interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse, as programmed. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. In the case of a programmed character length of less than 8 bits, the least significant DATA BUS unused bits are "don't care" when writing data to the USART and will be "zeros" when reading data. Rx data will be right justified onto D0 and the LSB for Tx data is D0.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½ or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16X or 64X baud rate factor. In these two cases, the half stop bit will be equivanlent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

## COMMAND WORDS

Command words are used to initiate specific functions within the COM 8251A such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the processor to the COM 8251A at any time during the execution of a program in which specific functions are to be initialized within the communication circuit.

Figure 4 shows the format for the Command Word.

**Figure 4. COM 8251A Control Command**

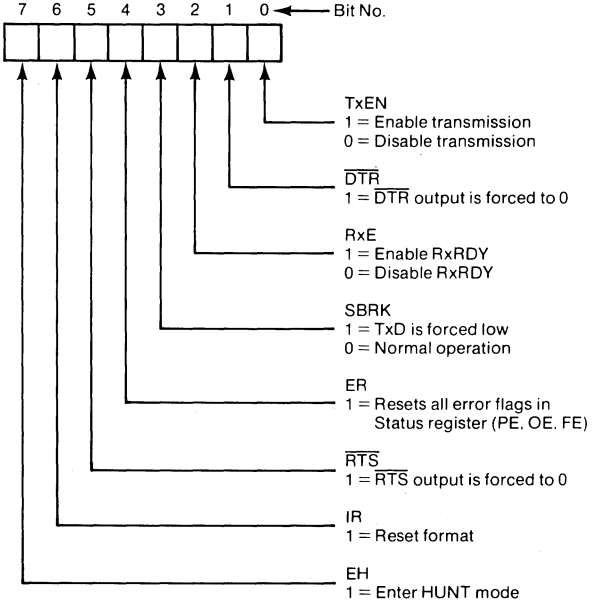


**Figure 2. Synchronous Mode Control Code.**

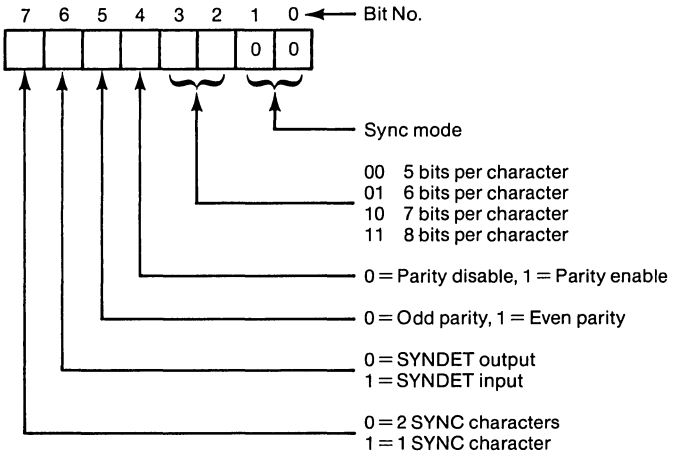
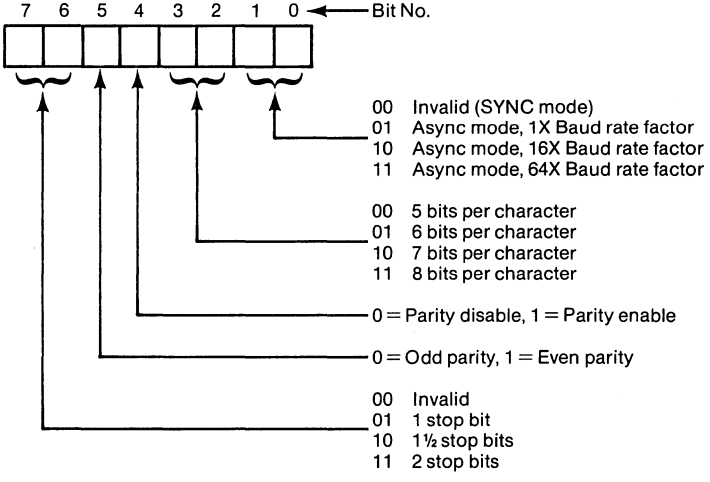



**Figure 3. Asynchronous Mode Control Code.**



Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission for the COM 8251A cannot take place unless TxEN is set (assuming $\overline{CTS} = 0$) in the command register. The TX Disable command is prevented from halting transmission by the Tx Enable logic until all data previously written has been transmitted. Figure 5 defines the way in which TxEN, TxE and TxRDY combines to control transmitter operations.

Bit 1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the $\overline{DTR}$ command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE, when zero, prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

**Figure 5.**
**Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN**

| TxEN | TxE | TxRDY | |
|---|---|---|---|
| 1 | 1 | 1 | Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if COM 8251A is in the asynchronous mode. TxD will send SYNC pattern if COM 8251A is in the Synchronous Mode. Data can be entered into Buffer. |
| 1 | 0 | 1 | Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor. |
| 1 | 1 | 0 | Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition. |
| 1 | 0 | 0 | Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission. |
| 0 | 0/1 | 0/1 | Transmitter is disabled. |

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the COM 8251A to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transferred with the ER bit set, all three error flags (PE, OE, FE) in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the COM 8251A. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit ($\overline{RTS}$), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is created independently of other signals in the COM 8251A. As a result, data transfers may be made by the processor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit 6, the Internal Reset (IR), causes the COM 8251A to return to the Idle mode. All functions within the COM 8251A cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a processor program, the COM 8251A must first be reset. Either the RESET input can be activated, or the Internal Reset Command can be sent to the COM 8251A. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the COM 8251A when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input, clear the Rx register to all "ones", and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the COM 8251A, or when SYNC characters are recognized. Parity is not checked in the EH mode.

## STATUS REGISTER

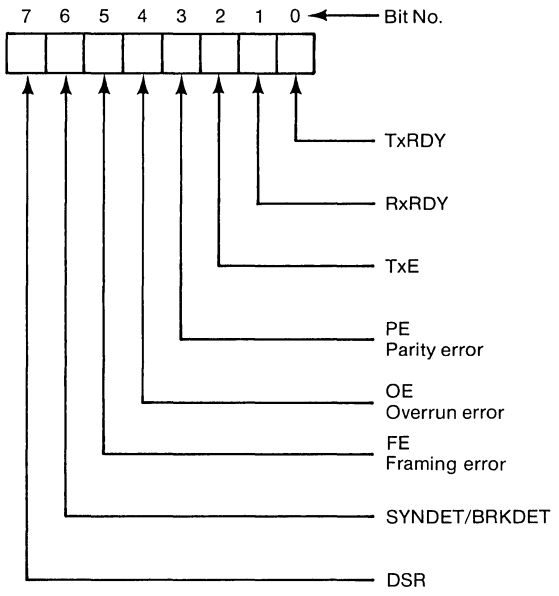
The Status Register maintains information about the current operational status of the COM 8251A. Status can be read at any time, however, the status update will be inhibited during status read. Figure 6 shows the format of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the COM 8251A can accept a new character for transmission. The TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY (status bit) = Tx Character Buffer Empty
TxRDY (pin 15) = Tx Character Buffer Empty • $\overline{CTS}$ • TxEN

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

**Figure 6. The COM 8251A Status Register**




TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. PE does not inhibit USART operation. PE is reset by the ER bit.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor. OE does not inhibit USART operation. OE is reset by the ER bit.

FE (Async only) is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect bit format ("0" stop bit), as specified by the current mode. FE does not inhibit USART operaton. FE is reset by the ER bit.

SYNDET is the synchronous mode status bit associated with internal or external sync detection.

DSR is the status bit set by the external $\overline{\text{Data Set Ready}}$ signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset by the error reset command or the internal reset command or the RESET input. OE, FE, or PE being set does not inhibit USART operation.

Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both Polled and Interrupt driven environments. Status update can have a maximum delay of 16 $t_{CY}$ periods.

**Note:**

1. While operating the receiver it is important to realize that the RxE bit of the Command Instruction only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. As the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. This read should be done immediately following the setting of the RxE bit in the asynchronous mode, and following the setting of EH in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.
2. ER should be performed whenever RxE of EH are programmed. ER resets all error flags, even if RxE = 0.
3. The USART may provide faulty RxRDY for the first read after power-on or for the first read after the receiver is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. This is not the case for the first read after hardware or software reset after the device opration has been established.
4. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through an internal flip-flop which clears itself, assuming the External Sync Detect assertion has removed, upon a status read. As long as External Sync Detect is asserted, External Sync Detect Status will remain high.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that as clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|
| **D.C. Characteristics** | | | | | |
| $V_{IL}$ | Input Low Voltage | −0.3 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 | V | $I_{OL} = 2.2$ mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH} = -400\ \mu A$ |
| $I_{OFL}$ | Output Float Leakage | | ±10 | $\mu A$ | $V_{OUT} = V_{CC}$ TO 0.45V |
| $I_{IL}$ | Input Leakage | | ±10 | $\mu A$ | $V_{IN} = V_{CC}$ TO 0.45V |
| $I_{CC}$ | Power Supply Current | | 100 | mA | All Outputs = High |
| **Capacitance** | | | | | $T_A = 25°C$, $V_{CC}$ = GND |
| $C_{IN}$ | Input Capacitance | | 10 | pF | fc = 1MHz |
| $C_{I/O}$ | I/O Capacitance | | 20 | pF | Unmeasured pins returned to GND |
| **A.C. Characteristics** | | | | | |
| **Bus Parameters** (Note 1) | | | | | |
| **Read Cycle:** | | | | | |
| $t_{AR}$ | Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$) | 0 | | ns | Note 2 |
| $t_{RA}$ | Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$) | 0 | | ns | Note 2 |
| $t_{RR}$ | $\overline{READ}$ Pulse Width | 250 | | ns | |
| $t_{RD}$ | Data Delay from $\overline{READ}$ | | 200 | ns | Note 3, $C_L = 150$ pF |
| $t_{DF}$ | $\overline{READ}$ to Data Floating | 10 | 100 | ns | |
| **Write Cycle:** | | | | | |
| $t_{AW}$ | Address Stable Before $\overline{WRITE}$ | 0 | | ns | |
| $t_{WA}$ | Address Hold Time for $\overline{WRITE}$ | 0 | | ns | |
| $t_{WW}$ | $\overline{WRITE}$ Pulse Width | 250 | | ns | |
| $t_{DW}$ | Data Set Up Time for $\overline{WRITE}$ | 150 | | ns | |
| $t_{WD}$ | Data Hold Time for $\overline{WRITE}$ | 0 | | ns | |
| $t_{RV}$ | Recovery Time Between WRITES | 6 | | $t_{CY}$ | Note 4 |
| **Other Timings:** | | | | | |
| $t_{CY}$ | Clock Period | .320 | 1.35 | $\mu s$ | Notes 5, 6 |
| $t_{\phi}$ | Clock High Pulse Width | 120 | $t_{CY}-90$ | ns | |
| $t_{\bar{\phi}}$ | Clock Low Pulse Width | 90 | | ns | |

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|
| $t_R$, $t_F$ | Clock Rise and Fall Time | 5 | 20 | ns | |
| $t_{DTx}$ | TxD Delay from Falling Edge of $\overline{TxC}$ | | 1 | $\mu$s | |
| $t_{SRx}$ | Rx Data Set-Up Time to Sampling Pulse | 2 | | $\mu$s | |
| $t_{HRx}$ | Rx Data Hold Time to Sampling Pulse | 2 | | $\mu$s | |
| $f_{Tx}$ | Transmitter Input Clock Frequency | | | | |
| | 1X Baud Rate | DC | 64 | kHz | |
| | 16X Baud Rate | DC | 310 | kHz | |
| | 64X Baud Rate | DC | 615 | kHz | |
| $t_{TPW}$ | Transmitter Input Clock Width | | | | |
| | 1X Baud Rate | 12 | | $t_{CY}$ | |
| | 16X and 64X Baud Rate | 1 | | $t_{CY}$ | |
| $t_{TPD}$ | Transmitter Input Clock Pulse Delay | | | | |
| | 1X Baud Rate | 15 | | $t_{CY}$ | |
| | 16X and 64X Baud Rate | 3 | | $t_{CY}$ | |
| $f_{Rx}$ | Receiver Input Clock Frequency | | | | |
| | 1X Baud Rate | DC | 64 | kHz | |
| | 16X Baud Rate | DC | 310 | kHz | |
| | 64X Baud Rate | DC | 615 | kHz | |
| $t_{RPW}$ | Receiver Input Clock Pulse Width | | | | |
| | 1X Baud Rate | 12 | | $t_{CY}$ | |
| | 16X and 64X Baud Rate | 1 | | $t_{CY}$ | |
| $t_{RPD}$ | Receiver Input Clock Pulse Delay | | | | |
| | 1X Baud Rate | 15 | | $t_{CY}$ | |
| | 16X and 64X Baud Rate | 3 | | $t_{CY}$ | |
| $t_{TxRDY}$ | TxRDY Pin Delay from Center of last Bit | | 8 | $t_{CY}$ | Note 7 |
| $t_{TxRDY\ CLEAR}$ | TxRDY ↓ from Leading Edge of $\overline{WR}$ | | 150 | ns | Note 7 |
| $t_{RxRDY}$ | RxRDY Pin Delay from Center of last Bit | | 24 | $t_{CY}$ | Note 7 |
| $t_{RxRDY\ CLEAR}$ | RxRDY ↓ from Leading Edge of $\overline{RD}$ | | 150 | ns | Note 7 |
| $t_{IS}$ | Internal SYNDET Delay from Rising Edge of $\overline{RxC}$ | | 24 | $t_{CY}$ | Note 7 |
| $t_{ES}$ | External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$ | | 16 | $t_{CY}$ | Note 7 |
| $t_{TxEMPTY}$ | TxEMPTY Delay from Center of Data Bit | | 20 | $t_{CY}$ | Note 7 |
| $t_{WC}$ | Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$) | | 8 | $t_{CY}$ | Note 7 |
| $t_{CR}$ | Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$) | | 20 | $t_{CY}$ | Note 7 |

**NOTES:**
1. AC timings measured $V_{OH} = 2.0$, $V_{OL} = 0.8$, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/$\overline{Data}$ ($C/\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $R_{DI}$.
4. This recovery time is for RESET and Mode Initialization. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 $t_{CY}$ and for Synchronous Mode is 16 $t_{CY}$.
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1X Baud Rate, $f_{Tx}$ or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16X and 64X Baud Rate, $f_{Tx}$ or $f_{Rx} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 $t_{CY}$ minimum; System Clock must be running during RESET.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

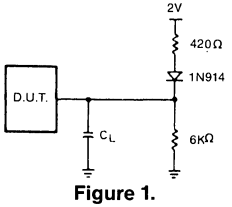
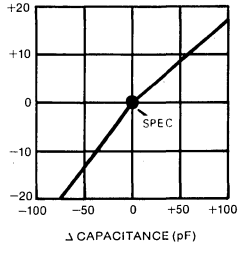



**Figure 1.**

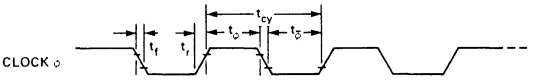
**TEST LOAD CIRCUIT**

**Typical Δ Output Delay Versus Δ Capacitance (pF)**

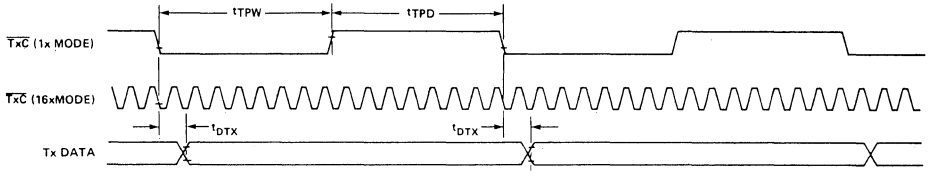


# WAVEFORMS

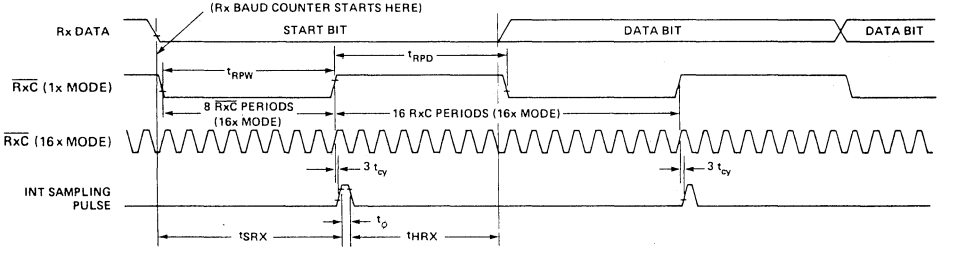
## System Clock Input



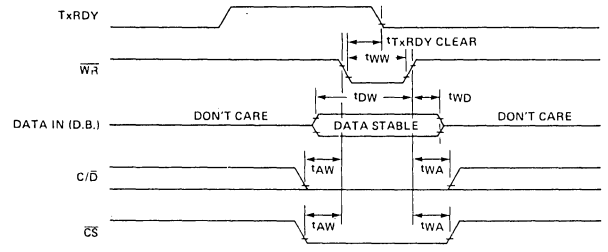

## Transmitter Clock & Data



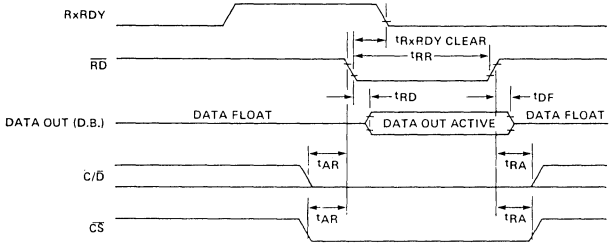

## Receiver Clock & Data



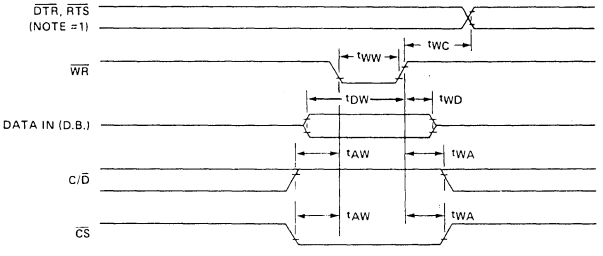
## Write Data Cycle (CPU → USART)




## Read Data Cycle (CPU ← USART)

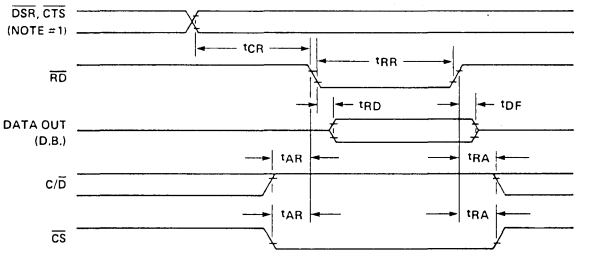



## Write Control or Output Port Cycle (CPU → USART)



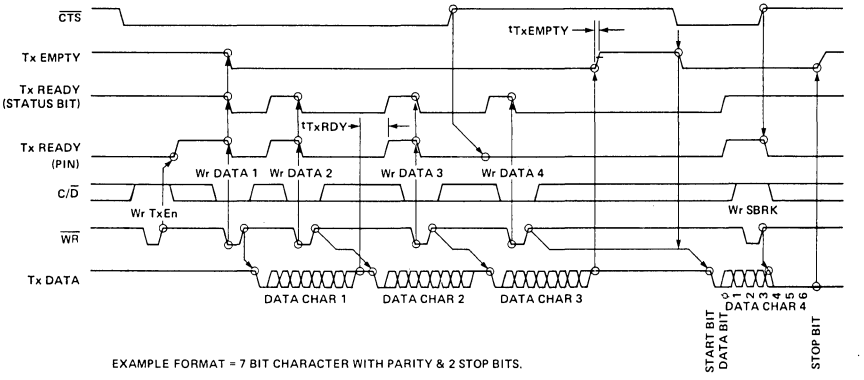

NOTE =1: $T_{WC}$ INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.

## Read Control or Input Port (CPU ← USART)



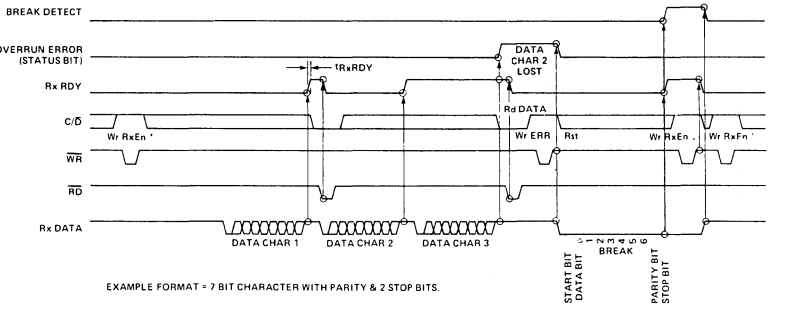

NOTE =1: $T_{CR}$ INCLUDES THE EFFECT OF $\overline{CTS}$ ON THE TxENBL CIRCUITRY.

## Transmitter Control & Flag Timing (ASYNC Mode)



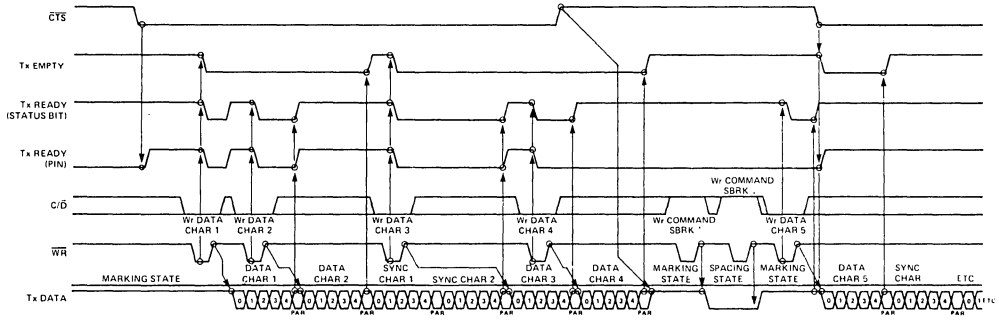

EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

## Receiver Control & Flag Timing (ASYNC Mode)



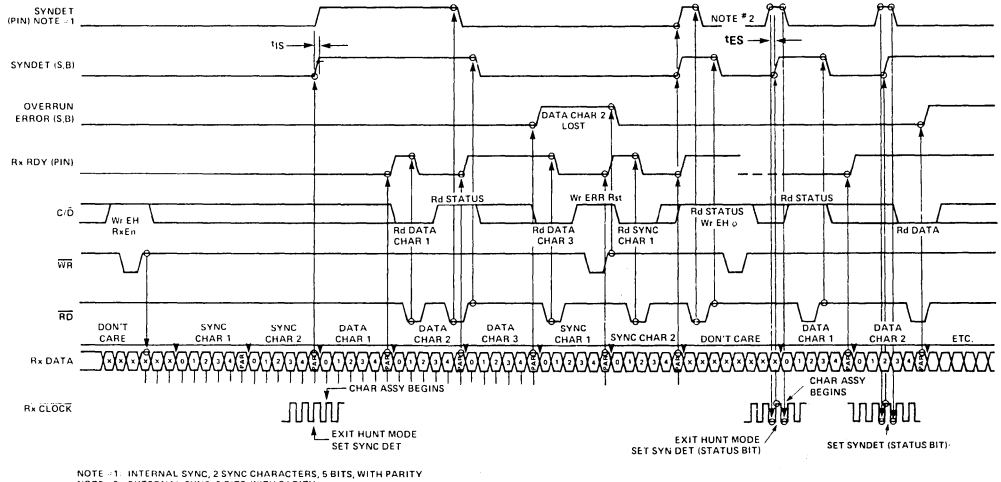

EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

## Transmitter Control & Flag Timing (SYNC Mode)




EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

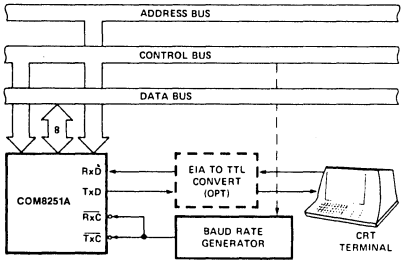
## Receiver Control & Flag Timing (SYNC Mode)



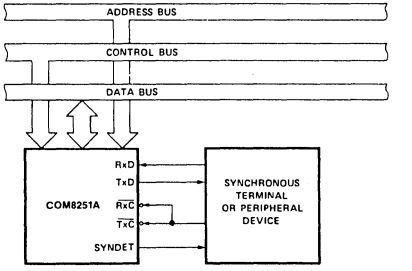

NOTE #1 INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2 EXTERNAL SYNC, 5 BITS, WITH PARITY

# APPLICATION OF THE COM8251A

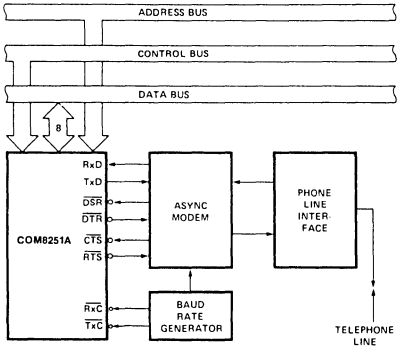
### Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



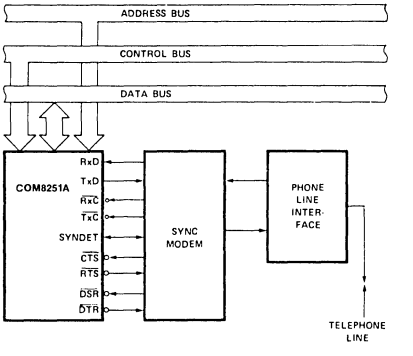

### Synchronous Interface to Terminal or Peripheral Device



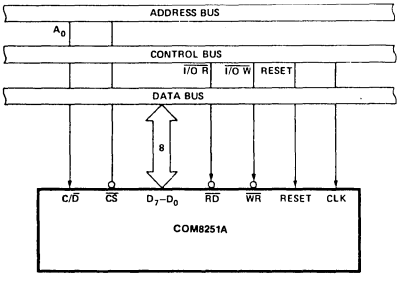

### Asynchronous Interface to Telephone Lines




### Synchronous Interface to Telephone Lines




### COM8251A Interface to $\mu$P Standard System Bus





STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM 9004

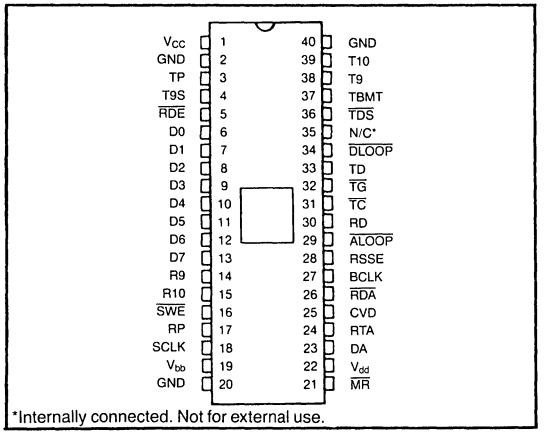
# IBM 3274/3276 Compatible COAX Receiver/Transmitter



## FEATURES

- ☐ Conforms to the IBM 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

## PIN CONFIGURATION



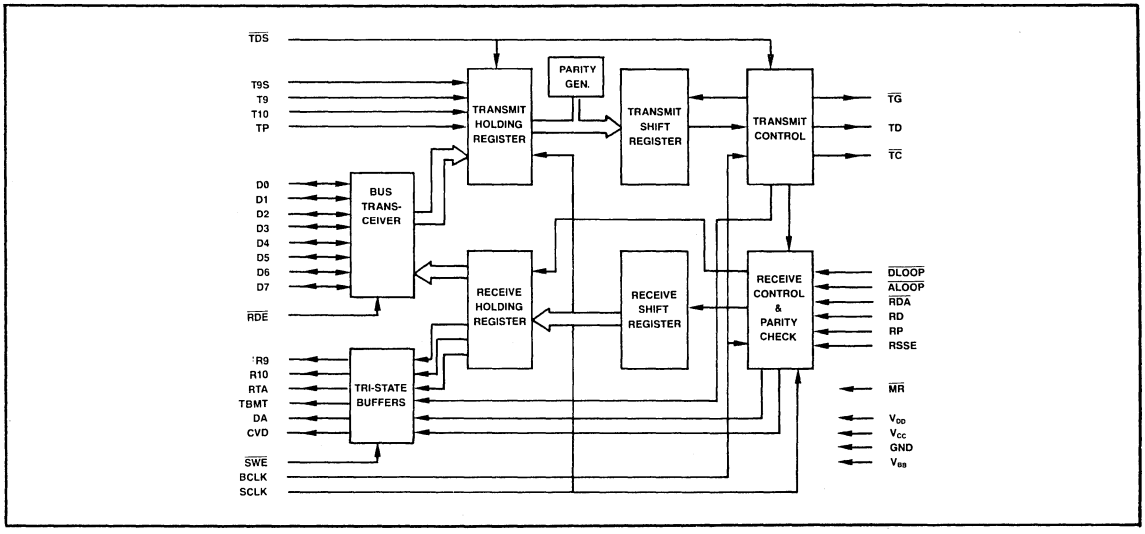

*Internally connected. Not for external use.

## GENERAL DESCRIPTION

The COM 9004 is an MOS/LSI circuit which may be used to facilitate high speed data transmission. The COM 9004 is fabricated using SMC's patented COPLAMOS® technology and may be used to implement an interface between IBM 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. The receiver and transmitter sections of the COM 9004 are separate and may be used independently of each other.

The COM 9004 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit).



## ORGANIZATION

The COM 9004 is organized into 9 major sections. Communication between each section is achieved via internal data and control busses.

### Transmitter Holding Register

The transmit holding register is a 12 bit latch. This latch is loaded with the transmit data and parity generation information from the system bus.

### Tri-State Buffers

These buffers allow gating of the COM 9004's status word onto the system data bus.

### Bus Transceiver

The bus transceiver allows bi-directional data transfer between the system data bus and the transmit and receive holding registers.

### Parity Generator

This logic determines and generates the correct parity for the data in the transmitter holding register.

### Transmitter Control

This logic generates signals required to enable external transmit circuitry. It also generates the Line Quiesce, Code Violation, sync bits and Mini Code Violation patterns.

### Transmitter Shift Register

The transmitter shift register is an 11 bit parallel to serial shift register. It accepts data from the transmitter holding register and the parity generation logic and converts it into serial form for transmission.

### Receive Control/Parity Check

This logic checks the received character for the specified parity and ensures that no Transmit Check conditions occurred. It also handles the self test mode and generates a strobe when the complete data word is received.

### Receiver Shift Register

This logic is a serial to parallel shift register that converts the received information into a 10 bit data word and RTA status bit.

### Receiver Holding Register

This register holds the assembled data word until it is read by the processor.

## DESCRIPTION OF PIN FUNCTIONS
### Processor Related Signals

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 6-13 | Transmit/ Receive Data Bits | D0-D7 | Bidirectional: 8 bit, three state data port used to transfer data between the COM 9004 and the processor. D0 is the first bit transmitted. |
| 4 | Transmit Bit 9 Select | T9S | Input: A low level on this pin enables T9 to be transmitted as bit 9. A high level on this pin causes T9 to determine the type of parity bit generated for bits D0-D7. |
| 38 | Transmit Bit 9 | T9 | Input: If T9S is low, this supplies transmit bit 9. If T9S is high, then T9 low forces odd parity and T9 high forces even parity to be generated for D0-D7. In this case the parity bit generated is transmit bit 9. |
| 39 | Transmit Bit 10 | T10 | Input: This pin supplies transmit bit 10. |
| 3 | Transmit Parity | TP* | Input: This input controls the parity bit for transmit bits 1-10. A low level on this pin causes odd parity and a high level on this pin causes even parity to be generated for bits 1-10. The parity bit generated is transmit bit 11. |
| 18 | System Clock | SCLK | Input: This signal is used to synchronize the COM 9004. The transmitter is loaded and started on the low to high transition of SCLK if TDS is low. DA is reset on the low to high transition of SCLK if RDA is low. |
| 36 | Transmitter Data Strobe | $\overline{TDS}$ | Input: This input and SCLK are used to load the transmitter holding register and start the transmit sequence. Code Violation Detect (CVD) is reset at this time. |
| 26 | Reset Data Available | $\overline{RDA}$ | Input: This input and SCLK are used to reset DA. |
| 16 | Status Word Enable | $\overline{SWE}$ | Input: A low level at this pin enables the status word buffer outputs (DA, CVD, TBMT, R9, R10, and RTA). A high level on $\overline{SWE}$ places the status word buffer outputs in a high impedance state. |
| 23 | Receive Data Available | DA | This three-state output signal is at a high level when an entire word has been received and transferred into the receiver buffer register. It is only set if a Transmit Check Condition did not occur. |
| 25 | Code Violation Detected | CVD | This three-state output signal is at a high level if a valid Code Violation was detected at the receiver since the last time the transmitter was loaded. It is reset when the transmitter is loaded. |
| 37 | Transmit Buffer Empty | TBMT | This three-state output signal is at a high level when the transmit holding register may be loaded with new data. |
| 14 | Receive Bit 9 | R9 | This three-state output signal is receiver data bit 9. |
| 15 | Receive Bit 10 | R10 | This three-state output signal is receiver data bit 10. |
| 24 | Receiver Turn-around | RTA | This three-state output signal is set to a high level when a valid Mini Code Violation is detected. It is only set if a Transmit Check did not occur. It is reset when the transmitter is loaded. |
| 5 | Receive Data Enable | $\overline{RDE}$ | Input: A low level enables the outputs of the receive data register D0-D7. |
| 17 | Receiver Parity | RP* | Input: This input determines whether the entire received word will be checked for even or odd parity. A low at this pin will cause a check for odd parity and a high at this pin will cause a check for even parity. This input has an internal pull-up resistor. |

*The SYNC bit is included in parity checking.

## DESCRIPTION OF PIN FUNCTIONS (cont.)

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 29 | Analog Loopback | $\overline{ALOOP}$ | Input: A low level on this pin disables the receiver except when the transmitter is active. A high level on this pin and $\overline{DLOOP}$ will cause the receiver to be disabled while the transmitter is active. $\overline{ALOOP}$ is used to allow loop-back through the line drivers and receivers. This input has an internal pull-up resistor. |
| 34 | Digital Loopback | $\overline{DLOOP}$ | Input: A low level on this pin disables the receiver except when the transmitter is active. $\overline{TG}$ is forced to a high level to disable the external coax driver. Data input to the receiver is internally wrapped from the transmitter data output. This input has an internal pull-up resistor. |
| 21 | Master Reset | $\overline{MR}$ | Input: This input should be pulsed low after power-on. This signal resets DA to a low level and sets $\overline{TG}$ and TBMT to a high level. This input has an internal pull-up. |
| 1 | Supply Voltage | $V_{cc}$ | +5 volt supply |
| 22 | Supply Voltage | $V_{dd}$ | +12 volt supply |
| 19 | Supply Voltage | $V_{bb}$ | −12 volt supply |
| 2, 20, 40 | Ground | GND | GROUND |

### Device Related Signals

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 27 | Baud Rate Clock | BCLK | This input is a clock whose frequency is 8 times the desired transmitter and receiver baud rate (typically 18.8696 MHz for 3274/3276 operation). This input is not TTL compatible. |
| 33 | Transmit Data | TD | Output: Serial data from the transmitter. This signal is a biphase Manchester II encoded bit stream. This output is high when no data is being transmitted. |
| 31 | Transmit Clock | $\overline{TC}$ | The Transmit Clock output is ½ the frequency of BCLK. It is synchronized with TD and used to provide external pre-distortion timing. |
| 30 | Receive Data | RD | Input: Accepts the serial biphase Manchester II encoded bit stream. |
| 32 | Transmit Gate | $\overline{TG}$ | Output: This signal is low during the time that the transmit data is valid. TG is used to turn on the external transmit circuitry. |
| 28 | Receive Single Shot Enable | RSSE | Input: A high level on this pin enables an internal digital single shot on RD. This limits a high level on RD to 3 clock times. Also when high it will cause the receiver not to detect a valid Code Violation. A low level disables the single shot causing no reshaping of the RD input signal. |

## COM 9004 OPERATION

The COM 9004 consists of a receiver section that converts Manchester II phase encoded serial data to parallel data and a transmitter section that converts parallel data to Manchester II phase encoded serial data.

### Receiver

Message transfers must conform to the IBM 3270 protocol in order for the COM 9004 to acknowledge them.

The received message is checked for the Code Violation sequence (start sequence) bit pattern, preceding the first data word, and Mini Code Violation (end sequence) following the last data word.

The data word consists of 10 data bits, a sync bit and a parity bit. Receiving data in multiple byte format is functional only when even parity is selected.

The data word along with the first bit of the next word or ending zero (bit 13) is shifted into a shift register. Once it is assembled it is transferred and held in the holding register until another data word is assembled. The 13th bit is inverted and presented to the bus or RTA (receiver turn-around). Therefore RTA is set high on the last word of a message and is reset when the transmitter is loaded with the response.

Once the data word is in the holding register and parity is correct the data available (DA) status signal is set high.

The Code Violation Detect signal (CVD) goes active high after a line Quiesce, Code Violation and sync bit have been detected by the receiver. It is reset when the transmitter of the COM 9004 is asserted. By examining this signal, the processor can determine whether a timeout or Transmit Check condition caused a receiver error.

The receive input is sampled at 8 times the data rate. The receiver logic is brought into bit synchronization during the Line Quiesce pattern. Once the Code Violation following the Line Quiesce is detected, the receiver is brought into bit and word synchronization. The internal receiver clock is adjusted after each transition to compensate for jitter and distortion in the received data signal.

### Transmitter

The transmitter section basically consists of a 12-bit holding register, parallel to serial shift register and a parity generator. The firmware initiates a transmit sequence by strobing $\overline{TDS}$ low. The data is loaded into the holding register on the rising edge of SCLK while TDS is low. Nine bits of data (D0-D7 and T10) are transferred without change to the transmit shift register. The logic level of T9S determines whether T9 will be transmitted as parity on the preceding eight bits, or as data.

After the processor loads the transmit holding register with data, status signal TBMT is driven inactive low until the COM 9004 transfers the data from the transmit holding register to the transmit shift register. After the transfer, TBMT is driven

high. The processor should not try to load data into the COM 9004 while TBMT is low. When initiating a data transmission, the COM 9004 automatically transmits a Line Quiesce pattern and a Code Violation. The data is then shifted out of the shift register with a sync bit (1) inserted before the data word, and a parity bit appended after the data word.

If a new word is loaded into the COM 9004 before the parity bit of the previous word has been transmitted, a sync bit (1) followed by the new data bits is transmitted. If not, after the COM 9004 transmits the last data word (no more transmit sequences are started), a sync bit (0) and a Mini Code Violation is appended to the end of the message.

Output $\overline{TG}$ goes active low one-half bit cell time before the first Line Quiesce character is output. It is made inactive (high) during the transmission of the Mini Code Violation.

## Diagnostic Modes

**NORMAL OPERATION ($\overline{ALOOP}$ AND $\overline{DLOOP}$ HIGH)**
Internal read data signal follows the RD input as long as the COM 9004's transmitter is off. The receiver will be disabled while the transmitter is active.

**ANALOG LOOPBACK ($\overline{ALOOP}$ LOW AND $\overline{DLOOP}$ HIGH)**
The internal read data signal follows the RD input as long as the COM 9004's transmitter is active.

**DIGITAL LOOPBACK $\overline{ALOOP}$ HIGH AND $\overline{DLOOP}$ LOW)**
The internal read data signal follows an internally generated and latched valid transmit signal (only when the transmitter is active.) The output $\overline{TG}$ is disabled in digital loopback mode.

**DISABLE RECEIVER ($\overline{ALOOP}$ AND $\overline{DLOOP}$ LOW)**
The internal read data signal is held low and output $\overline{TG}$ is disabled.

## MESSAGE FORMATS

### Single Byte Transmission

| COAX IDLE | LINE QUIESCE | CODE VIOLATION | SYNC BIT | DATA (10 BITS) | PARITY BIT | ENDING SEQUENCE | COAX IDLE |
|---|---|---|---|---|---|---|---|

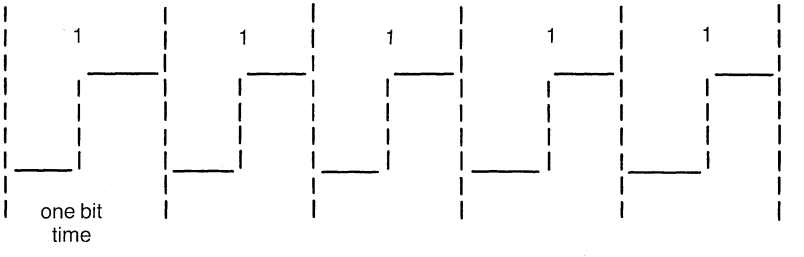
### Multiple Byte Transmission

| COAX IDLE | LINE QUIESCE | CODE VIOLATION | SYNC BIT | DATA 1 (10 BITS) | PARITY BIT | SYNC BIT | DATA 2 (10 BITS) |
|---|---|---|---|---|---|---|---|

| PARITY BIT | ..... | SYNC BIT | DATA N (10 BITS) | PARITY BIT | ENDING SEQUENCE | COAX IDLE |
|---|---|---|---|---|---|---|

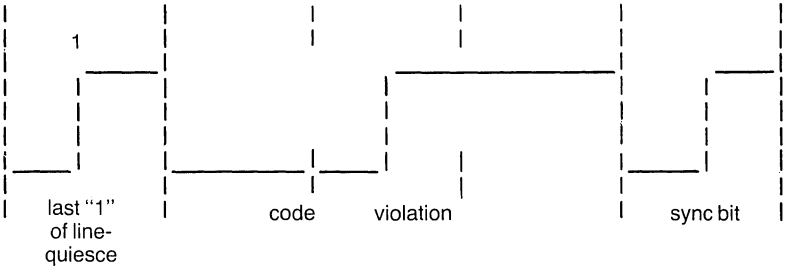
Bits on the coax appear as positive and negative going pulses. A positive pulse to negative pulse transition in the middle of the bit cell is interpreted as a logical '0'. A negative pulse to positive pulse transition in the middle of a bit cell is interpreted as a logical '1'. A predistortion pulse is generated for every pulse transition from an up to down level or a down to up level.

### Line Quiesce Pattern



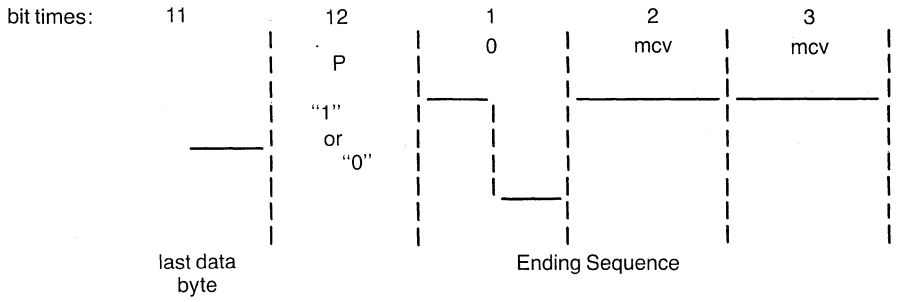

The Line Quiesce pattern consists of five contiguous logical ones. It establishes an equilibrium condition on the coax following line turnaround.

## Code Violation Pattern




The Code Violation pattern is a bit sequence containing no mid-bit time level transition in two of its three bit cells. It is a unique pattern that violates the encoding rules and indicates the start of valid data.

## Mini Code Violation Pattern




The Mini Code Violation (MCV) pattern is a bit sequence containing no mid-bit time level transition in either of its bit cells. It is a unique code that violates the encoding rules and indicates the end of valid transmit data.

## Transmit Check

A Transmit Check is defined as follows:

1) A logical zero sync bit in the ending sequence not followed by a Mini Code Violation.
2) Loss of a level transition at the mid-bit time during other than a normal ending sequence.
3) A transmission parity error.

**MAXIMUM GUARANTEED RATINGS***

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −55° to +150°C |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Positive Voltage on any I/O Pin, with respect to ground | +18.0V |
| Negative Voltage on any I/O Pin, with respect to ground | −0.3V |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

**DC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%, $V_{DD}$ = +12V ±5%, $V_{BB}$ = −12V ±5%)

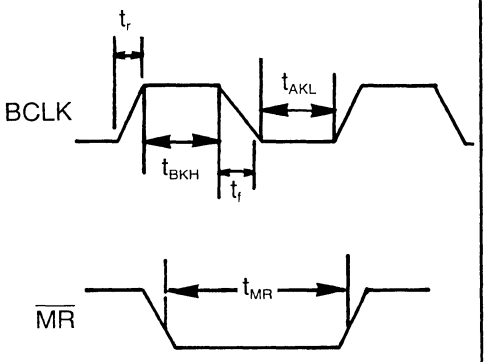
| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| $V_{IL}$ Low | −0.3 | | .8 | V | |
| $V_{IH}$ High | 2.0 | | $V_{CC}$ | V | (Except BCLK, $\overline{MR}$) |
| $V_{IH}$ High | 4.3 | | $V_{CC}$ + .3 | V | (BCLK only) |
| $V_{IH}$ High | 3.0 | | $V_{CC}$ + .3 | V | $\overline{MR}$ only |
| OUTPUT VOLTAGE LEVELS | | | | | |
| $V_{OL}$ Low | | | .4 | | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ High | 2.4 | | | | $I_{OH}$ = −.25 mA |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 70 | | mA | All outputs = $V_{OH}$ |
| $I_{DD}$ | | 16 | | mA | |
| $I_{BB}$ | | 5 | | mA | |
| INPUT LEAKAGE CURRENT | | | | | |
| All input pins | | | .01 | mA | $V_{IN}$ = 0 to $V_{CC}$ |
| CAPACITANCE | | | | | |
| $C_{IN}$ | | | 10 | pf | (Except BCLK) |
| $C_{IN}$ | | | 35 | pf | (BCLK only) |

**AC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%, $V_{DD}$ = +12V ±5%, $V_{BB}$ = −12V ±5%)

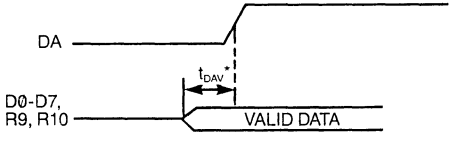
| PARAMETER | | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Frequency | | | | | | |
| $B_{CLK}$ | | 7 | 18.8696 | 18.9 | MHz | |
| $S_{CLK}$ | | DC | 4.7474 | 5 | MHz | |
| Clock Width | | | | | | |
| $t_{SKH}$ | SCLK High | 80 | | | ns | |
| $t_{SKL}$ | SCLK Low | 80 | | | ns | |
| $t_{BKH}$ | BCLK High | 20 | | | ns | |
| $t_{BKH}$ | BCLK Low | 20 | | | ns | |
| $t_r$ | BCLK rise time | | | 6 | ns | |
| $t_F$ | BCLK fall time | | | 6 | ns | |
| $t_{RDD}$ | $\overline{RDE}$ to Data Valid Delay | | | 50 | ns | |
| $t_{SDD}$ | SWE to Data Valid Delay | | | 50 | ns | |
| $t_{DF}$ | Data Read to Bus Float | | | 50 | ns | |
| $t_{DS}$ | Data Setup Time | 100 | | | ns | |
| $t_{DH}$ | Data Hold Time | 10 | | | ns | |
| $t_{DAV}$ | DA to receive data valid delay | −100 | | 100 | ns | |
| $t_{TC}$ | TC clock period | | 106 | | ns | |
| $t_{\overline{TGLD}}$ | TC to TG low delay | −53 | | 30 | ns | |
| $t_{\overline{TGHD}}$ | TC to TG high delay | | | 30 | ns | |
| $t_{TDS}$ | Transmit data to TG setup time | 10 | | | ns | |
| $t_{TDH}$ | Transmit data to TC hold time | 20 | | | ns | |
| $t_D$ | TBMT active to de-active | | 200 | | ns | |
| $t_{DDC}$ | TBMT cycle | | | 3.2 | µs | |
| $t_{DD}$ | $\overline{TBMT}$ de-activated | 1 | | 2 | µs | |
| $t_{DSS}$ | $\overline{TDS}$ set up | 100 | | 200 | ns | |
| $t_{DSH}$ | $\overline{TDS}$ hold | 10 | | 100 | ns | |
| $t_{MR}$ | $\overline{MR}$ pulse width | 300 | | | ns | |

# TIMING DIAGRAMS

## MISC. TIMING

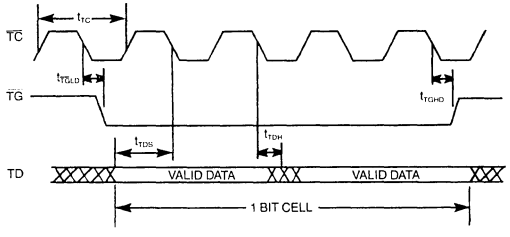



## RECEIVE DATA TIMING

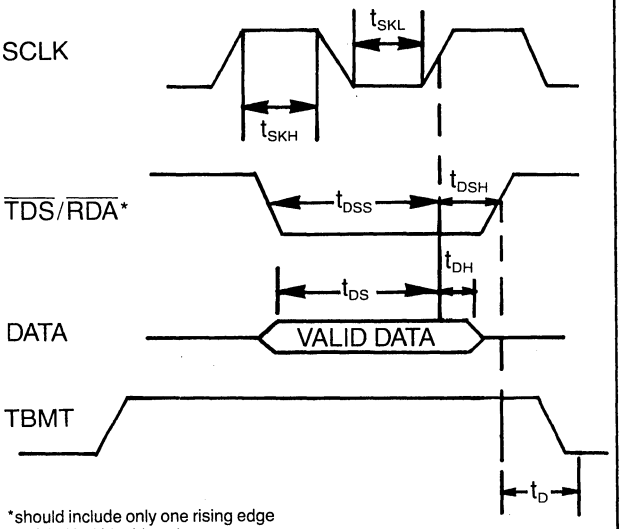



*DA may occur from 100 ns before to 100 ns after data is valid.

## TRANSMITTER TIMING

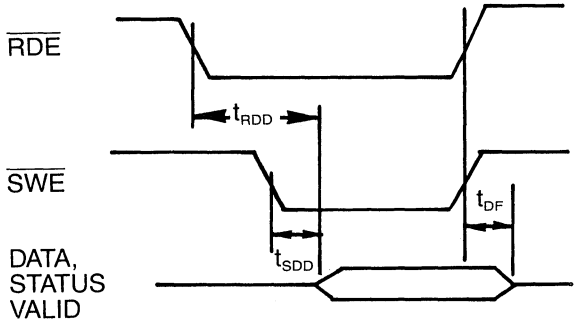



## BUS INPUT TIMING

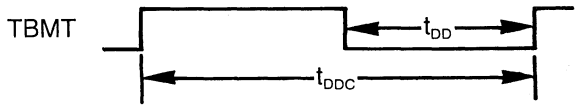


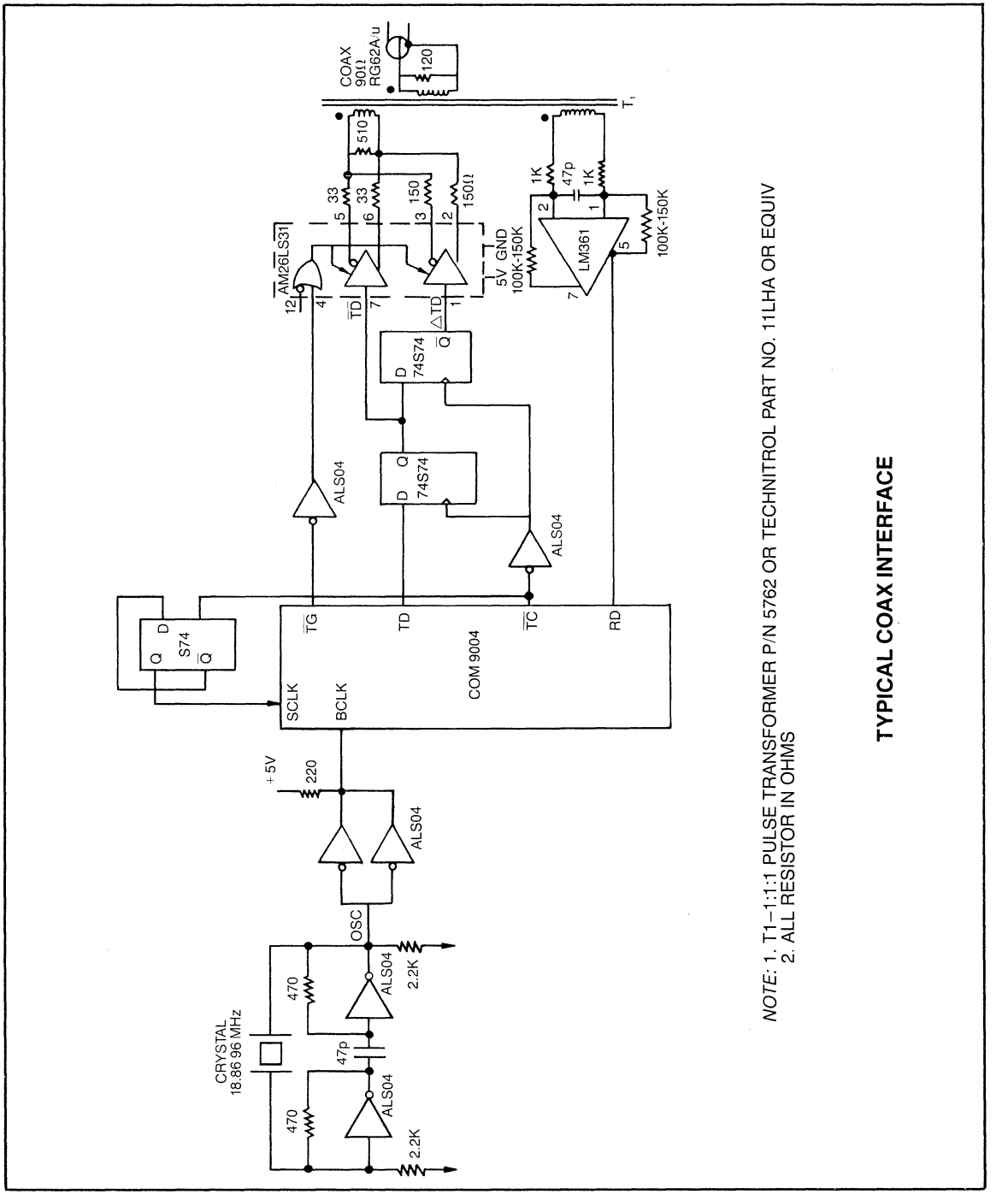

*should include only one rising edge of SCLK within this pulse.

## BUS OUTPUT TIMING




## TBMT CYCLE






**TYPICAL COAX INTERFACE**

*NOTE:* 1. T1–1:1:1 PULSE TRANSFORMER P/N 5762 OR TECHNITROL PART NO. 11LHA OR EQUIV
2. ALL RESISTOR IN OHMS

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge NY 11788
(516) 273-3100 TWX-510 227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM 9026

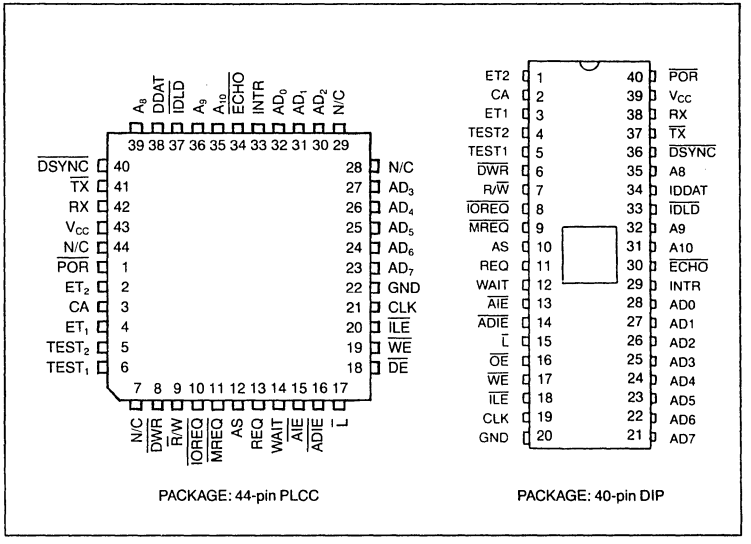
# Local Area Network Controller LANC™



## FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET* local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 9026
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)
- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single +5 volt supply

## PIN CONFIGURATION




PACKAGE: 44-pin PLCC

PACKAGE: 40-pin DIP

## GENERAL DESCRIPTION

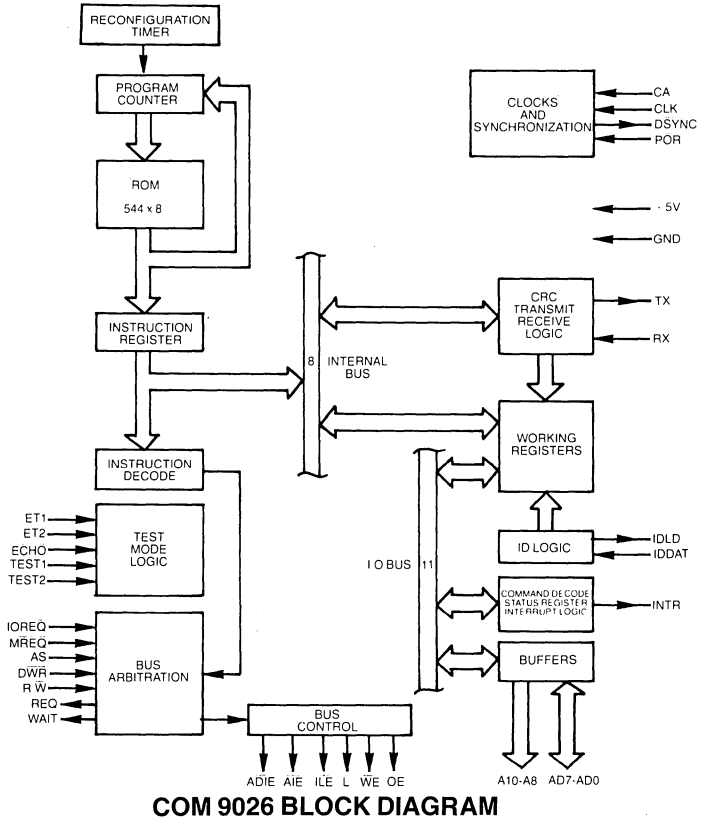
The COM 9026 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The COM 9026 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 9026 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 9026 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 9026 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 9026. The processor can write commands to the COM 9026 and also read COM 9026 status. The COM 9026 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

*ARCNET is a registered trademark of the Datapoint Corporation.




**COM 9026 BLOCK DIAGRAM**

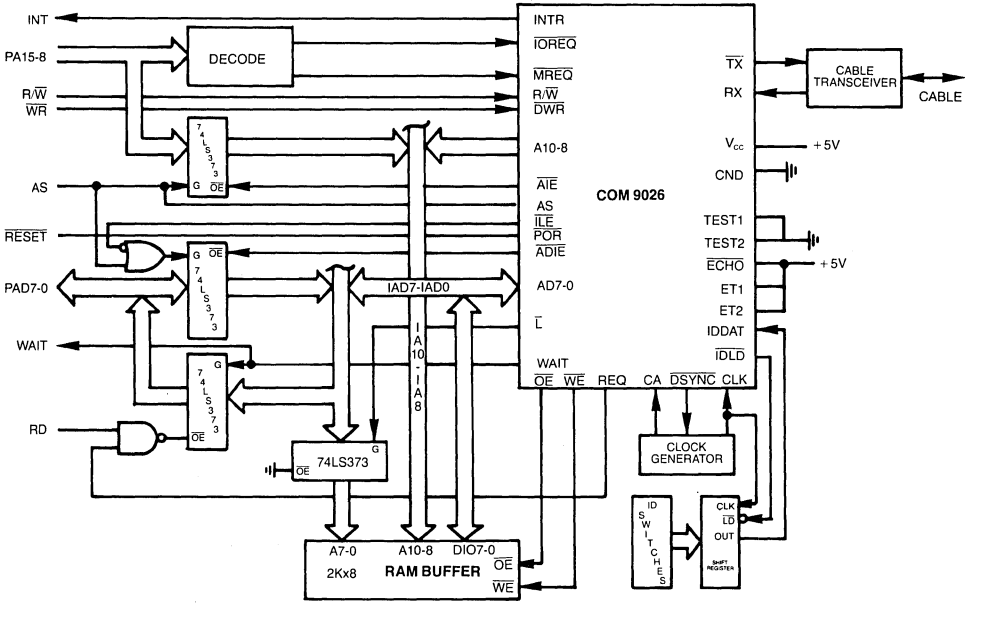



**FIGURE 2—TYPICAL COM 9026 INTERFACE**

## DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

| DIP PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 31, 32, 35 | ADDRESS 10, 9, 8 | A10, A9, A8 | These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 9026 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected. |
| 21, 22, 23, 24, 25, 26, 27, 28 | ADDRESS/ DATA 7-0 | AD7-AD0 | These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 9026. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 9026. |
| 8 | I/O REQUEST | $\overline{\text{IOREQ}}$ | This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 9026. This signal is sampled internally on the falling edge of AS. |
| 9 | MEMORY REQUEST | $\overline{\text{MREQ}}$ | This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS. |
| 7 | READ/$\overline{\text{WRITE}}$ | R/$\overline{\text{W}}$ | A high level on this input signal indicates that the processor's access cycle to the COM 9026 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 9026. The write cycle will not be completed, however, until the $\overline{\text{DWR}}$ input is asserted. This signal is an internal transparent latch gated with AS. |
| 10 | ADDRESS STROBE | AS | This input signal is used by the COM 9026 to sample the state of the $\overline{\text{IOREQ}}$, $\overline{\text{MREQ}}$ and R/$\overline{\text{W}}$ inputs. The COM 9026 bus arbitration is initiated on the falling edge of this signal. |
| 11 | REQUEST | REQ | This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{\text{MREQ}}$ or $\overline{\text{IOREQ}}$ passed through an internal transparent latch gated with AS. |
| 12 | WAIT | WAIT | This output signal is asserted by the COM 9026 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 9026 is ready for the processor to complete its cycle. |
| 6 | DELAYED WRITE | $\overline{\text{DWR}}$ | This input signal informs the COM 9026 that valid data is present on the processor's data bus for write cycles. The COM 9026 will remain in the WAIT state until this signal is asserted. $\overline{\text{DWR}}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded. |
| 29 | INTERRUPT REQUEST | INTR | This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit. |
| 18 | INTERFACE LATCH ENABLE | $\overline{\text{ILE}}$ | This output signal, in conjunction with $\overline{\text{ADIE}}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 9026 operation. |
| 14 | ADDRESS/ DATA INPUT ENABLE | $\overline{\text{ADIE}}$ | This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{\text{ILE}}$ onto the interface address/data bus (IAD7-IAD0). |
| 13 | ADDRESS INPUT ENABLE | $\overline{\text{AIE}}$ | This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8). |
| 15 | LATCH | $\overline{\text{L}}$ | This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles. |
| 17 | WRITE ENABLE | $\overline{\text{WE}}$ | This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{\text{WE}}$. |
| 16 | OUTPUT ENABLE | $\overline{\text{OE}}$ | This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations. |
| 33 | ID LOAD | $\overline{\text{IDLD}}$ | This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 9026. The shift register is clocked with the same signal that feeds the COM 9026 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19. |
| 34 | ID DATA IN | IDDAT | This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1". |
| 1, 3 | EXTENDED TIMEOUT FUNCTION 2, 1 | ET2, ET1 | The levels on these two input pins specify the timeout durations used by the COM 9026 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details. |
| 37 | TRANSMIT DATA | $\overline{\text{TX}}$ | This output signal contains the serial transmit data to the CABLE TRANSCEIVER. |
| 38 | RECEIVE DATA | RX | This input signal contains the serial receive data from the CABLE TRANSCEIVER. |

## DESCRIPTION OF PIN FUNCTIONS (Continued)

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 4, 5 | TEST PIN 2<br>TEST PIN 1 | TEST2<br>TEST1 | These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing. |
| 30 | ECHO DIAGNOSTIC ENABLE | $\overline{ECHO}$ | When this input signal is low, the COM 9026 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing. |
| 19 | CLOCK | CLK | A continuous 5 MHz clock input used for timing of the COM 9026 bus cycles, bus arbitration, serial ID input, and the internal timers. |
| 2 | CA | CA | This input signal is a 5 MHz clock used to control the operation of the COM 9026 microcoded sequencer. This input is periodically halted in the high state by the DSYNC output. |
| 36 | DELAYED SYNC | $\overline{DSYNC}$ | This output signal is asserted by the COM 9026 to cause the external clock generator logic to halt the CA clock. Refer to figure 9. |
| 40 | POWER ON RESET | $\overline{POR}$ | This input signal clears the COM 9026 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network. |
| 39 | +5 VOLT SUPPLY | $V_{CC}$ | Power Supply |
| 20 | GROUND | GND | Ground |

## PROTOCOL DESCRIPTION

### LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

### Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

### Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 85 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

### Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

### Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 86 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

### Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

### NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 9026's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 9026 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet.

If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsuccessful delivery of the packet. An interrupt mask permits the COM 9026 to generate an interrupt to the processor when selected status bits become true. Figure 3 is a flow chart illustrating the internal operation of the COM 9026.

## NETWORK RECONFIGURATION

A significant advantage of the COM 9026 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 9026 is turned on (creating a new active node on the network), or if the COM 9026 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 9026 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 9026 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 9026 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 9026 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 9026 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 9026 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 9026 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 9026 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 9026 on the network will finally have saved a NID value equal to the ID of the COM 9026 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

## BROADCAST MESSAGES

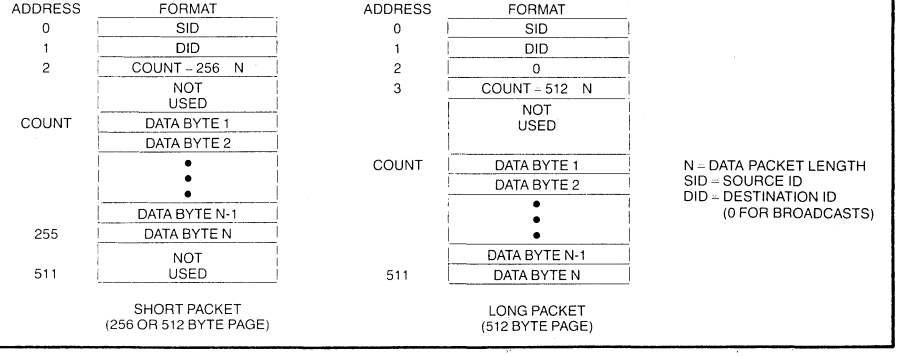
Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 8 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 9026 COMMANDS") to a logic zero.

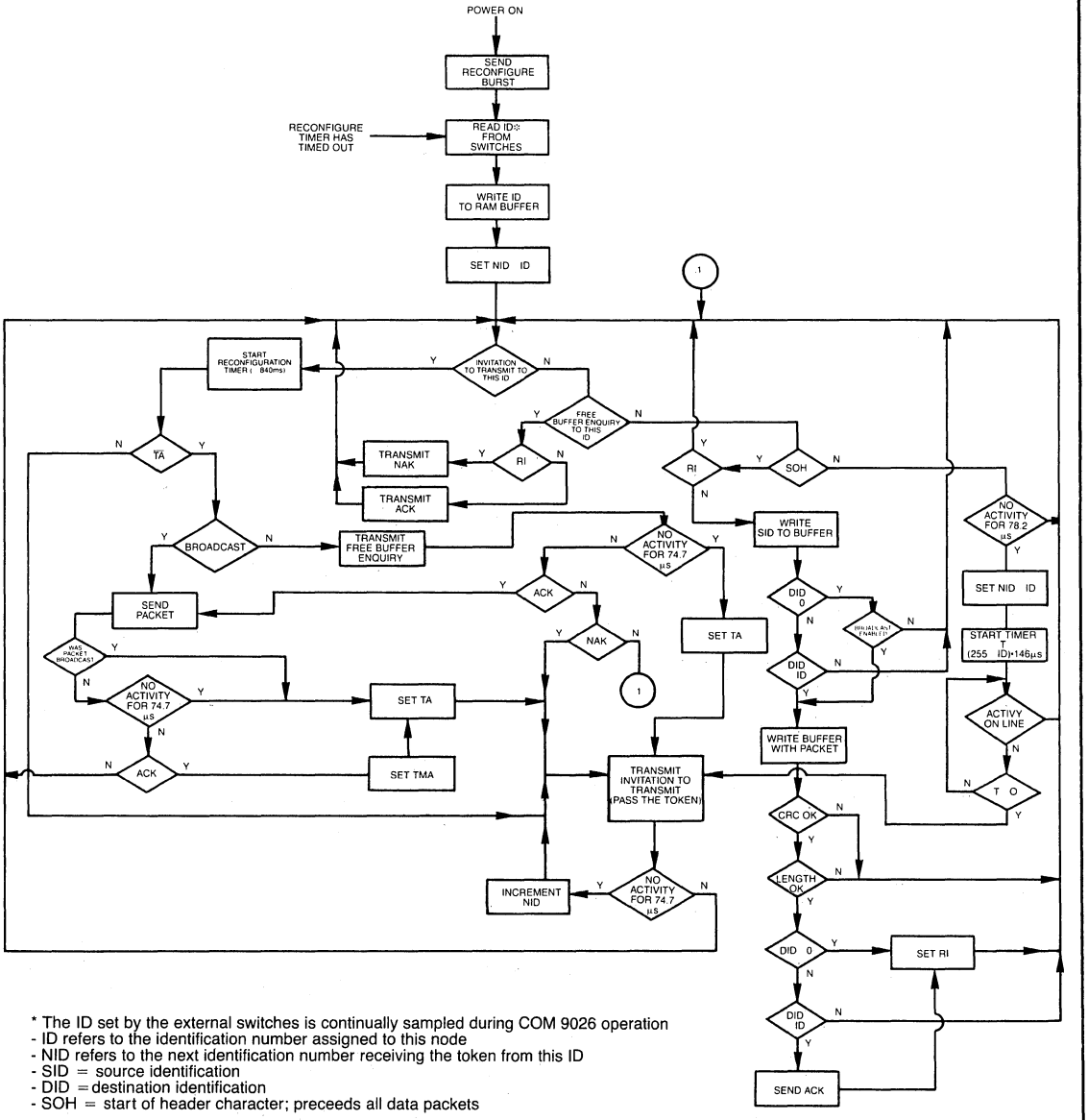
# COM 9026 OPERATION

## BUFFER CONFIGURATION

During a transmit sequence, the COM 9026 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 9026 will interpret the packet as a long or short packet depending on whether the contents of buffer location 02 is zero or non zero. During a receive sequence, the COM 9026 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 9026 receiver or the COM 9026 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512 byte) are shown below.

**FIGURE 8— RAM BUFFER PACKET CONFIGURATION**






* The ID set by the external switches is continually sampled during COM 9026 operation
- ID refers to the identification number assigned to this node
- NID refers to the next identification number receiving the token from this ID
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

**FIGURE 3—9026 OPERATION**

## PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 9026 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 9026, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 9026.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 9026 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multimessage transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 9026, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 9026 or command writes to the COM 9026).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 9026 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 9026.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{\text{IOREQ}}$ or $\overline{\text{MREQ}}$ is asserted. These access cycles run completely asynchronous with respect to the COM 9026. Because of this, upon processor access cycle requests, the COM 9026 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 9026 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 9026, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{\text{AIE}}$ and $\overline{\text{ADIE}}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{\text{L}}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{\text{OE}}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

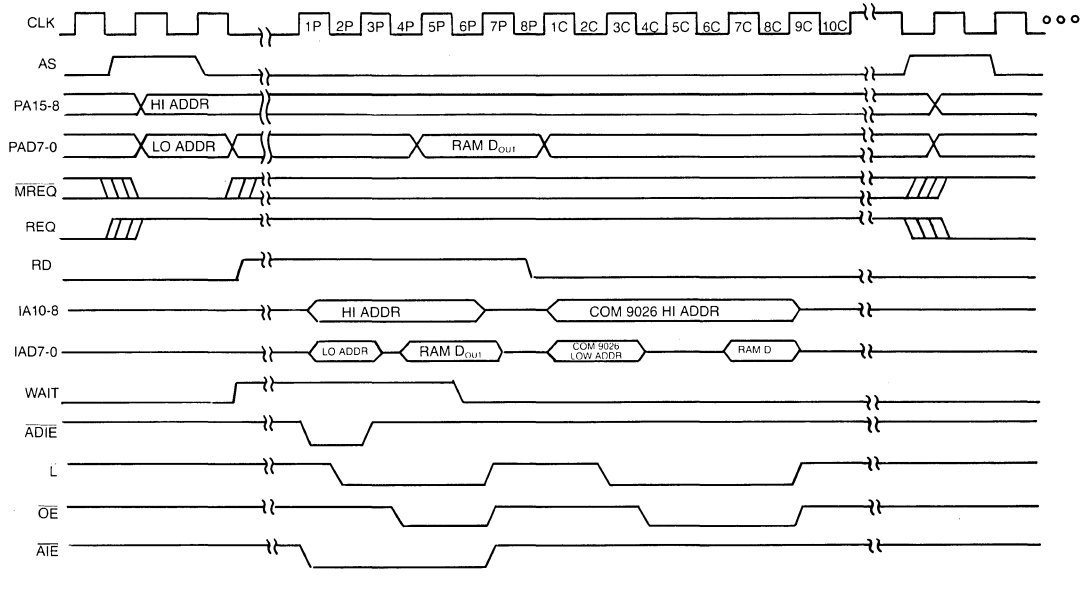



**FIGURE 4—PROCESSOR READ RAM FOLLOWED BY COM 9026 READ RAM**

and driven out via the logic function RD anded with REQ. For processor I/O read cycles from the COM 9026, ADIE and AIE are used to enable the processor address into the COM 9026. Data out of the COM 9026 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 9026 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 9026 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 9026 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 9026 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 9026, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 9026. Delaying the activation of DWR will hold up the COM 9026 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 9026 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 9026 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 9026 cycle will follow immediately after the processor cycle. Figure 4 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 9026 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 4 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 9026 access cycle will take 5 CLK periods to end. Figure 4 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 9026 request has already been granted, the COM 9026 cycle will occur first, as shown in figure 5. Figure 5 illustrates the timing relationship of a COM 9026 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 9026 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 5, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 9026 produces a leading edge on both ADIE and AIE. If the processor request occurs before the end of half

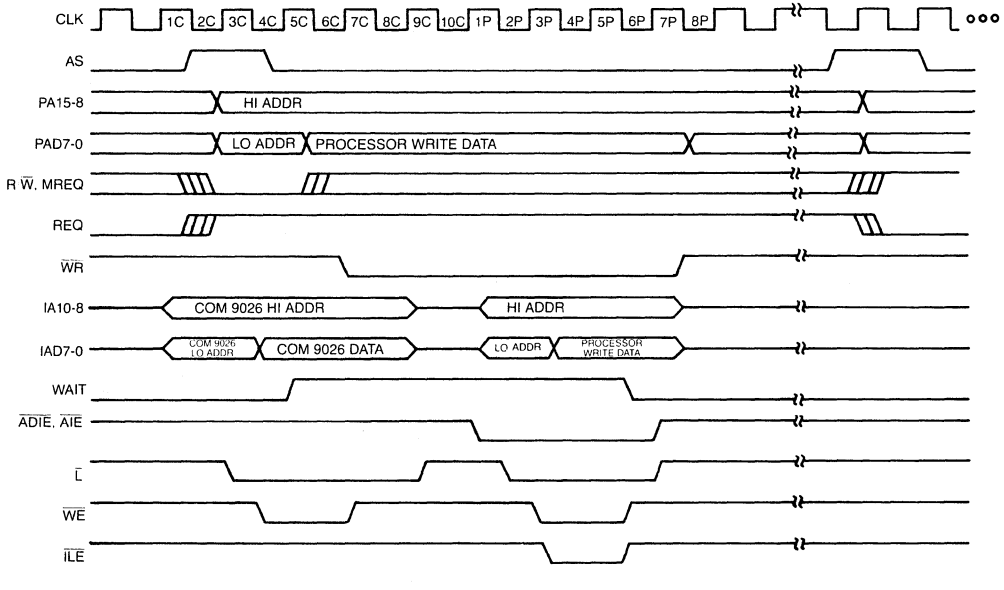



**FIGURE 5—COM 9026 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM**

CLK interval 5C (figure 5 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 9026 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 6 and 7 illustrate timing for Processor Read COM 9026 and Processor Write COM 9026 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 4 and 5 if these processor cycles occur.

## POWER UP AND INITIALIZATION

The COM 9026 has the following power up requirements:

1—The $\overline{\text{POR}}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the $\overline{\text{POR}}$ input is removed.
3—While $\overline{\text{POR}}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{\text{POR}}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{\text{POR}}$ may be released before CA begins running.

During $\overline{\text{POR}}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{\text{DSYNC}}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{\text{POR}}$ signal is removed, the COM 9026 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 9026 will start operation four CA clock cycles after the $\overline{\text{POR}}$ signal is removed. At this time, the COM 9026, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 9026 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

## CLOCK GENERATOR

The COM 9026 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 9026 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{\text{DSYNC}}$ output and the RX input. The $\overline{\text{DSYNC}}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{\text{DSYNC}}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{\text{DSYNC}}$. (See figure 20 for an implementation of this circuit.)

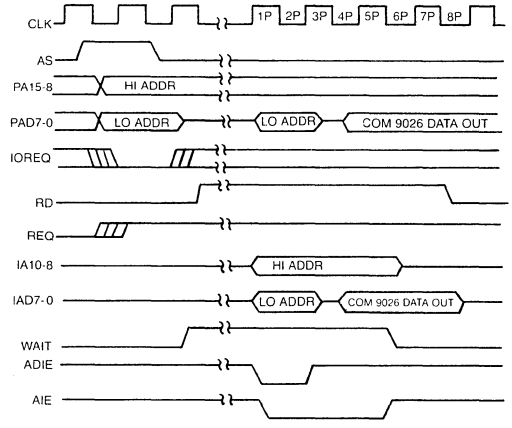



**FIGURE 6—PROCESSOR READ COM 9026**

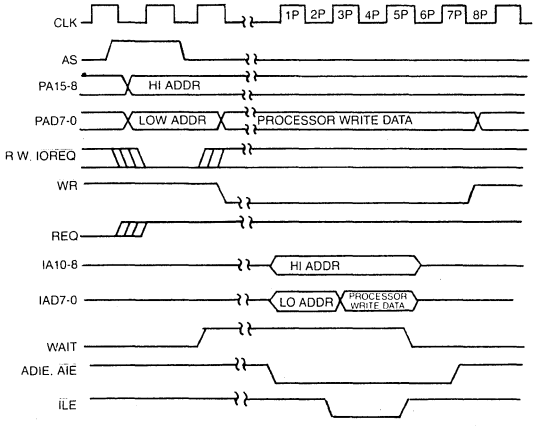



**FIGURE 7—PROCESSOR WRITE COM 9026**

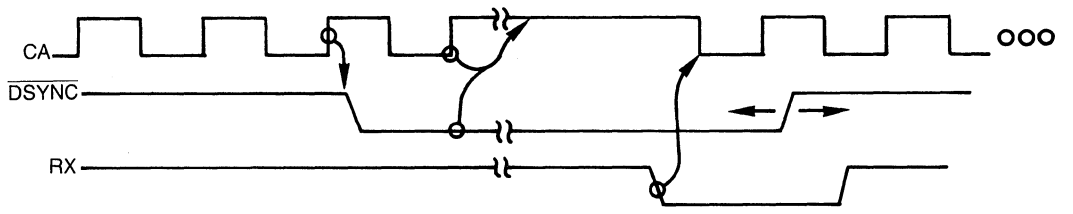



**FIGURE 9—CA CLOCK GENERATOR TIMING**

## EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 9026 operation.

### Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 9026 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 3 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

### Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 3, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 9026 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

### Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 9026 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. It should be noted that for proper network operation, all COM 9026's connected to the same network must have the same response time, idle time and reconfiguration time.

| ET2 | ET1 | RESPONSE TIME (μs) | IDLE TIME (μS) | RECONFIGURATION TIME (ms) |
|---|---|---|---|---|
| 1 | 1 | 78 | 86 | 840 |
| 1 | 0 | 285 | 316 | 1680 |
| 0 | 1 | 563 | 624 | 1680 |
| 0 | 0 | 1130 | 1237 | 1680 |

**TABLE 1**
**COM 9026 INTERNAL PROGRAMMABLE TIMER VALUES**

## I/O COMMANDS

I/O commands are executed by activating the $\overline{\text{IOREQ}}$ input. The COM 9026 will interrogate the AD0 and the R/$\overline{\text{W}}$ inputs at the AS time to execute commands according to the following table:

| $\overline{\text{IOREQ}}$ | AD0 | R/$\overline{\text{W}}$ | FUNCTION |
|---|---|---|---|
| low | low | low | write interrupt mask |
| low | low | high | read status register |
| low | high | low | write COM 9026 command |
| low | high | high | reserved for future use |

## READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 9026 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 9026 has received an active signal on the POR input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

## WRITE INTERRUPT MASK

The COM 9026 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|
| RECEIVE INHIBIT | XXX | XXX | XXX | XXX | RECON TIMER | XXX | TRANSMITTER AVAILABLE |

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

## WRITE COM 9026 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

| WRITTEN DATA | COMMAND |
|---|---|
| 00000000 | reserved for future use |
| 00000001 | DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 9026 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received. |
| 00000010 | DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 9026 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion. |
| 000nn011 | ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 9026 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "0". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 9026 has received an acknowledgement from the destination COM 9026. This acknowledgement is strictly hardware level which is sent by the receiving COM 9026 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits. |
| b00nn100 | ENABLE RECEIVE TO PAGE nn—This command allows the COM 9026 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 9026 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message. |
| 0000c101 | DEFINE CONFIGURATION—If c is a logic "1", the COM 9026 will handle short as well as long packets. If c is a logic "0", the COM 9026 will only handle short packets (less than 254 bytes). |
| 000rp110 | CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "l", the RECON status flag is cleared. |

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... −55 to 150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... +8V
Negative Voltage on any pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**DC ELECTRICAL CHARACTERISTICS** ($T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$)

| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | input low voltage | −0.3 | | 0.8 | V | |
| $V_{IH1}$ | input high voltage 1 | 2.2 | | $V_{CC}$ | V | except CA and CLK |
| $V_{IH2}$ | input high voltage 2 | $V_{CC}-0.5$ | | 6.5 | V | for CA or CLK |
| $V_{OL1}$ | output low voltage 1 | | | 0.4 | V | $I_{OL}$ = 1.6ma |
| $V_{OL2}$ | output low voltage 2 | | | 0.5 | V | $I_{OL}$ = 2.0ma |
| $V_{OH}$ | output high voltage | 2.4 | | | V | except $\overline{Tx}$ and $\overline{DSYNC}$ $I_{OH} = -100\mu A$ |
| $V_{OH}$ | output high voltage | 2.7 | | | V | $\overline{Tx}$ and $\overline{DSYNC}$ only $I_{OH} = -100\mu A$ |
| $I_L$ | input leakage current | | | ±10 | μA | |
| $C_{IN}$ | input capacitance | | | 20 | pf | |
| $C_{DB}$ | data bus capacitance | | | 50 | pf | |
| $C_L$ | all other capacitance | | | 30 | pf | |
| $I_{CC}$ | power supply current | | 180 | 350 | ma | |

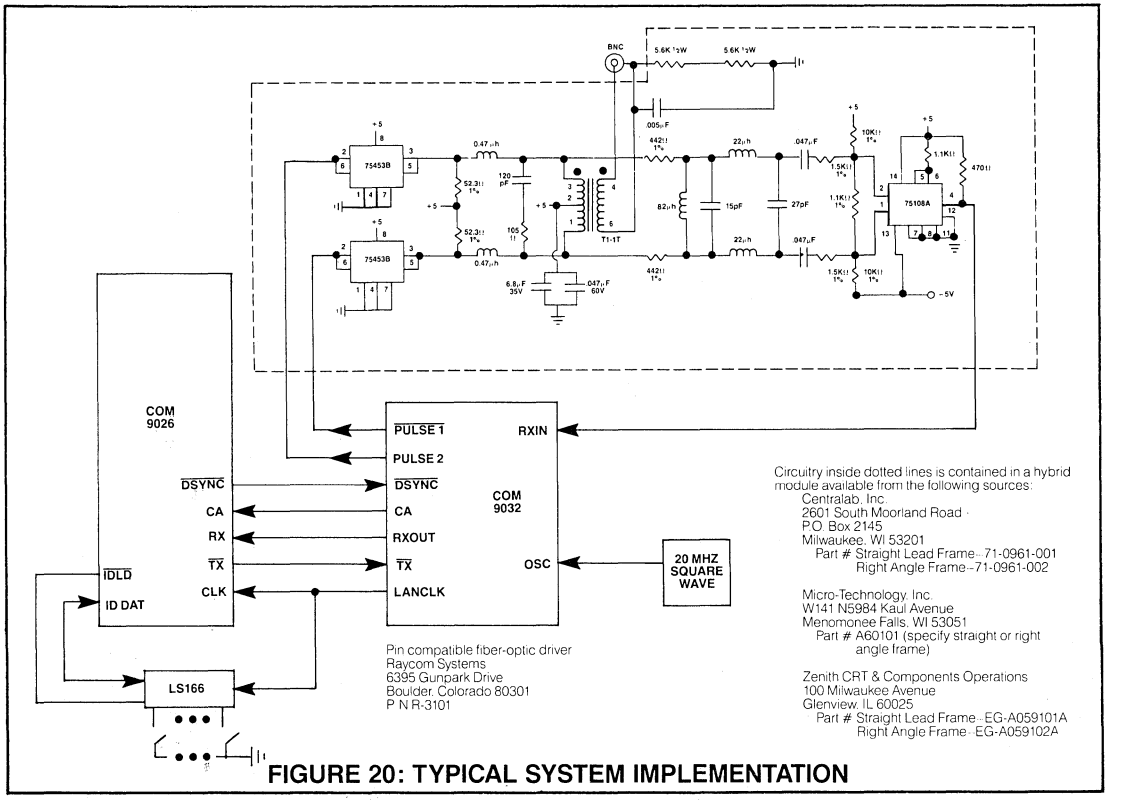


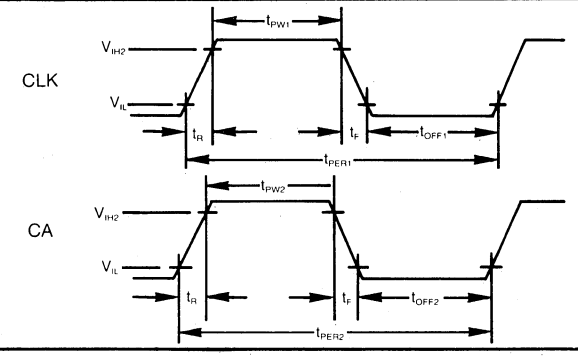

**FIGURE 20: TYPICAL SYSTEM IMPLEMENTATION**

## AC ELECTRICAL CHARACTERISTICS ($T_A = 0°$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$)

| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| $t_{PW1}$ | CLK pulse width | 65 | | | ns | |
| $t_{PER1}$ | CLK period | 190 | 200 | 600 | ns | |
| $t_{OFF1}$ | CLK off time | 65 | | | ns | |
| $t_{PW2}$ | CA pulse width | 60 | | | ns | |
| $t_{PER2}$ | CA period | 190 | | | ns | |
| $t_{OFF2}$ | CA off time | 60 | 100 | 300 | ns | |
| $t_R$ | CLK, CA rise time | | | 20 | ns | |
| $t_F$ | CLK, CA fall time | | | 20 | ns | |
| $t_1$ | width of addr. strobe | 50 | | 400 | ns | |
| $t_2$ | REQ output delay | 0 | | 100 | ns | |
| $t_3$ | WAIT assertion delay | 0 | | 200 | ns | |
| $t_4$ | delay to rising edge of processor cycle | $t_P$ | | $2t_P + 100$ | ns | $t_P = t_{PER1}$ |
| $t_5$ | data hold into COM 9026 | 80 | | | ns | |
| $t_6$ | setup COM 9026 data out | 60 | | | ns | |
| $t_7$ | $\overline{WE}$ delay from CLK | 0 | | 100 | ns | |
| $t_8$ | $\overline{TX}$ on delay from CA falling edge | 10 | | 150 | ns | |
| $t_9$ | $\overline{TX}$ off delay from CA rising edge | 10 | | 150 | ns | |
| $t_{10}$ | AS period | 7/2 $t_P$ | | | ns | $t_P = t_{PER2}$ |
| $t_{11}$ | $\overline{DSYNC}$ delay from CA rising edge | 10 | | 150 | ns | |
| $t_{12}$ | delay to wait off | 20 | | 100 | ns | |
| $t_{13}$ | $\overline{DWR}$ setup time | 50 | | | ns | |
| $t_{14}$ | $\overline{ILE}$ delay from CLK | 10 | | 100 | ns | |
| $t_{15}$ | processor addr. setup from $\overline{ADIE}$, | | | 50 | ns | |
| $t_{16}$ | processor command setup time | 125 | | | ns | |
| $t_{17}$ | addr. enable setup time to $\overline{L}$ | 50 | | | ns | |
| $t_{18}$ | addr. hold time from $\overline{L}$ | 50 | | | ns | |
| $t_{19}$ | strobe and data hold for read | 20 | | | ns | |
| $t_{20}$ | AD bus HI impedance to $\overline{OE}$s | 0 | | | ns | |
| $t_{21}$ | delay of $\overline{IDLD}$ from CLK rising edge | 0 | | 120 | ns | |
| $t_{22}$ | delay of IDDAT from CLK rising edge | 0 | | 50 | ns | |
| $t_{23}$ | off delay from CLK rising edge | 0 | | 100 | ns | |
| $t_{24}$ | addr. to RAM data valid | | | 300 | ns | |
| $t_{25}$ | $\overline{OE}$ setup to WAIT falling edge | 140 | | | ns | |
| $t_{26}$ | strobe & data hold for write | 50 | | | ns | |
| $t_{27}$ | addr. enable setup to WAIT | 300 | | | ns | |
| $t_{28}$ | $\overline{ADIE}$ to $\overline{OE}$ delay | 40 | | | ns | |
| $t_{29}$ | COM 9026 write data hold time | 80 | | | ns | |
| $t_{30}$ | $\overline{OE}$ to RAM data valid | 0 | | 140 | ns | |
| $t_{31}$ | status setup to AS falling edge | 50 | | | ns | |
| $t_{32}$ | status hold from AS falling edge | 50 | | | ns | |
| $t_{33}$ | RX setup to CA rising edge | 80 | | | ns | |
| $t_{34}$ | RX hold time from CA rising edge | 30 | | | ns | |
| $t_{35}$ | $\overline{POR}$ active time | 100 | | | ms | after $V_{CC}$ has been stable for time $t_{35}$, the minimum $\overline{PDR}$ active time is 10 cycles of CLK. |

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

**FIGURE 10— CLK, CA AC CHARACTERISTICS**



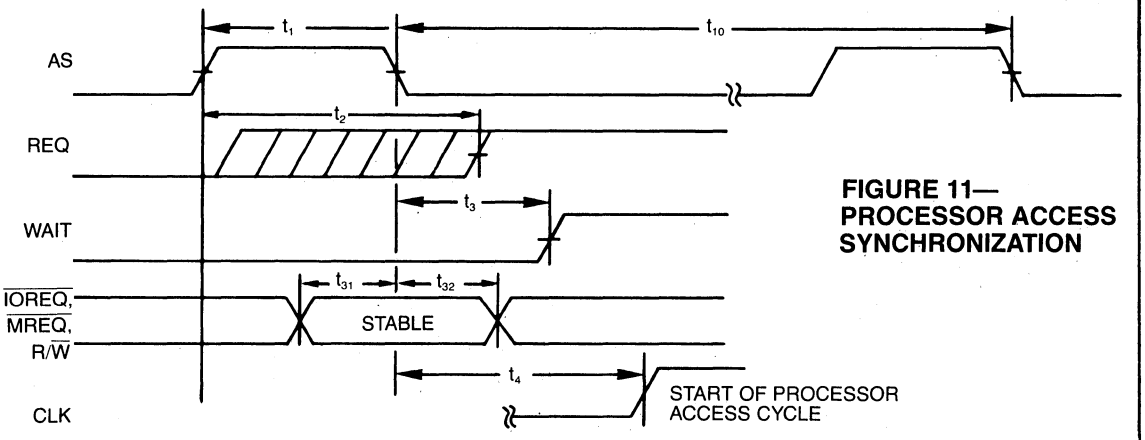



**FIGURE 11—PROCESSOR ACCESS SYNCHRONIZATION**

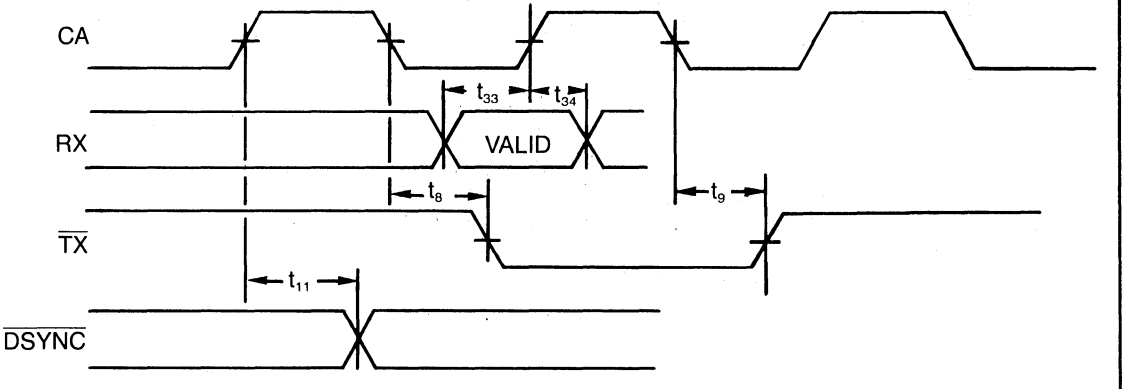



**FIGURE 12—TRANSMIT AND RECEIVE TIMING**

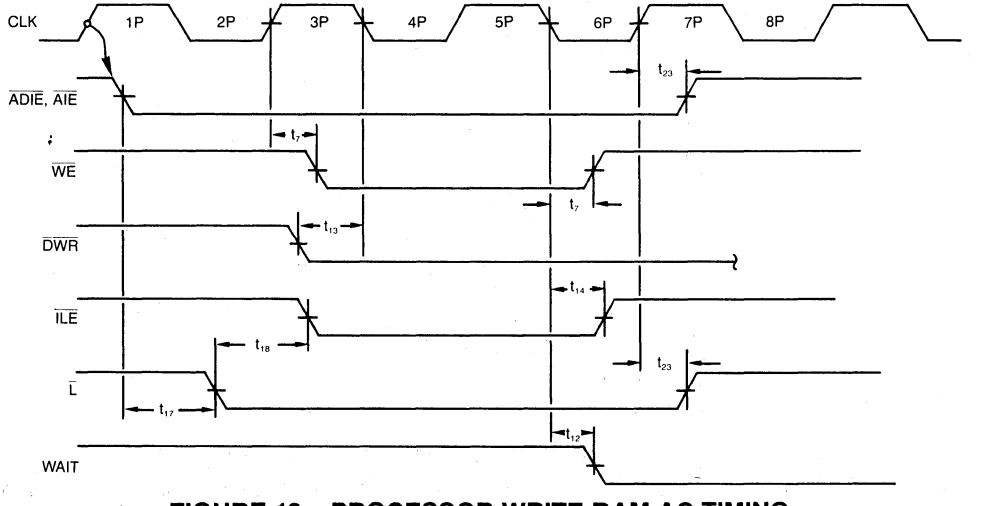



**FIGURE 13—PROCESSOR WRITE RAM AC TIMING**

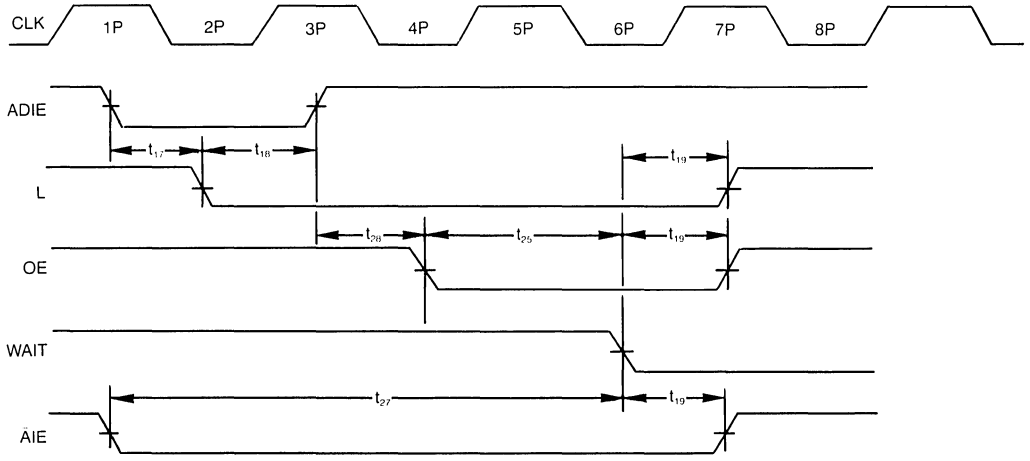



**FIGURE 14—PROCESSOR READ RAM AC TIMING**

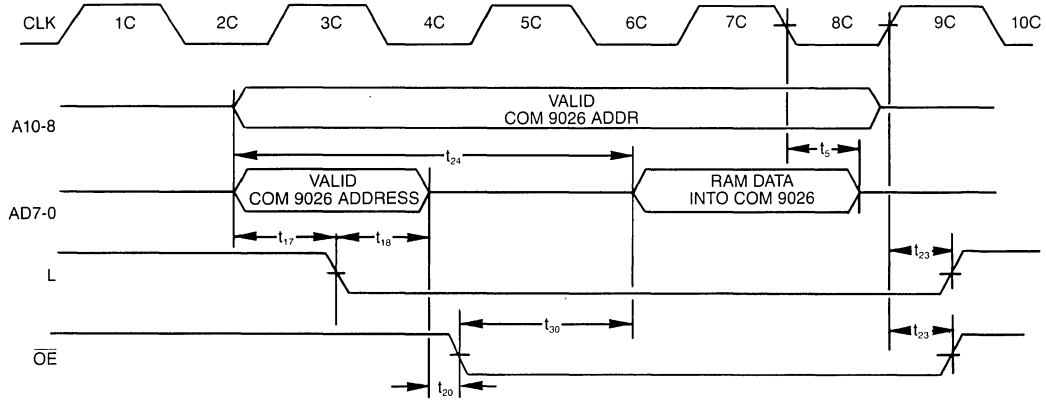



**FIGURE 15—COM 9026 READ RAM AC TIMING**

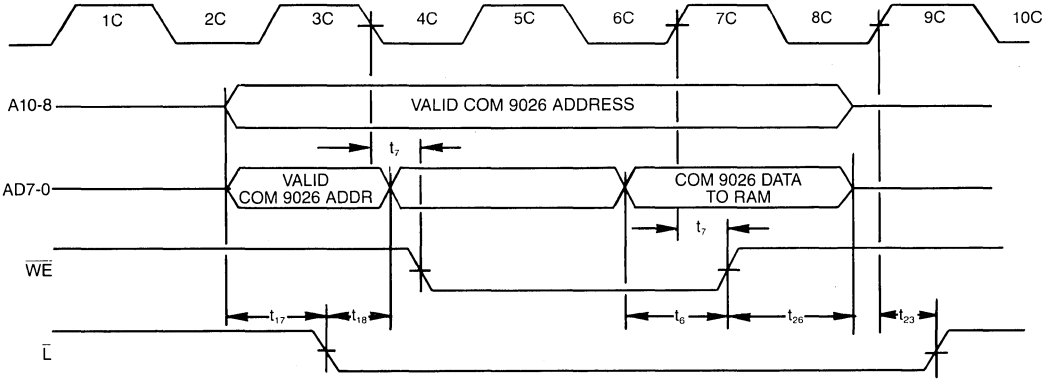



**FIGURE 16—COM 9026 WRITE RAM AC TIMING**

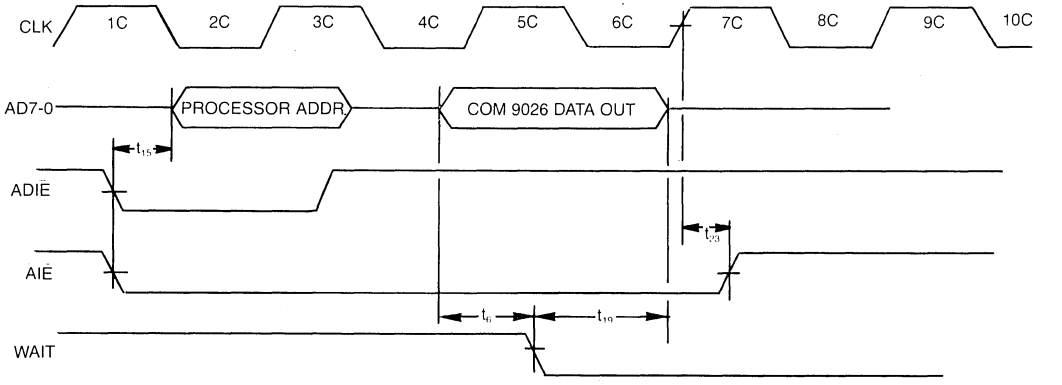



**FIGURE 17—PROCESSOR READ COM 9026 AC TIMING**

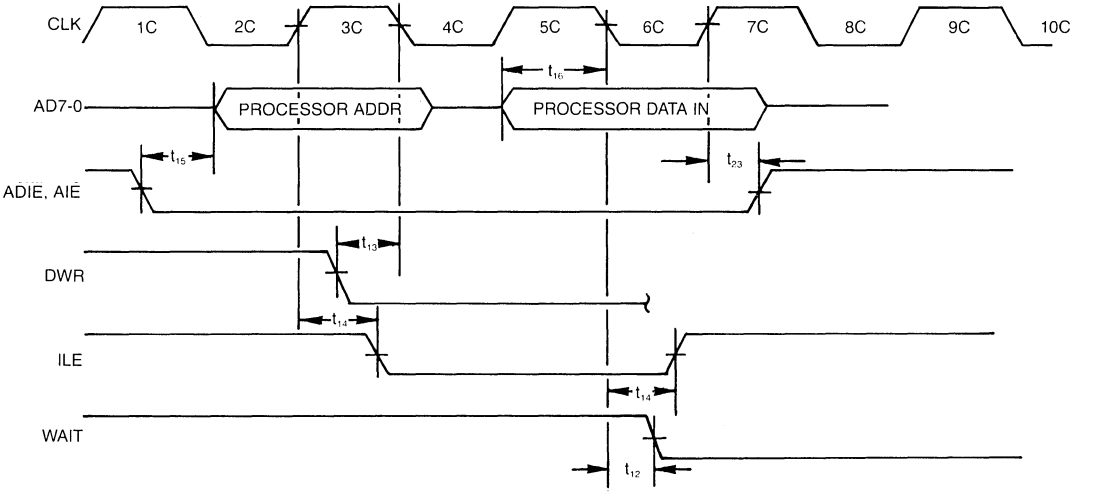



**FIGURE 18—PROCESSOR WRITE COM 9026 AC TIMING**

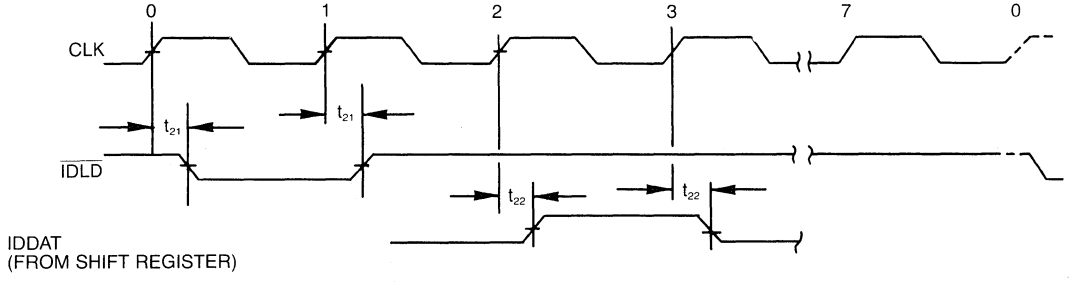



**FIGURE 19—ID INPUT AC TIMING**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

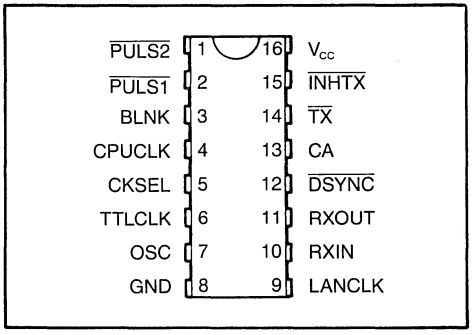
# COM 9032
# Local Area Network Transceiver
# LANT



## FEATURES

- ☐ Reduces chip count for COM 9026 ARCNET* implementations by 6-8 TTL chips
- ☐ Performs all clock generation functions for the COM 9026
- ☐ Compatible with the COM 9026
- ☐ Provides line drive signals for transmission
- ☐ Converts incoming serial receive data to NRZ data format
- ☐ Generates two 4 MHz general purpose clocks

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The COM 9032 local area network transceiver is a companion chip to the COM 9026 Local Area Network Controller (LANC) and will perform the additional functions necessary to allow simple interface to a transmission media for all ARCNET* (or equivalent) local area networks. Using a 20 MHz input clock, the COM 9032 will produce two, 5 MHz clocks for the COM 9026. The first 5 MHz clock is free running and will directly feed the CLK input of the COM 9026 (pin 19). The second 5 MHz clock has start/stop capability which is controlled by the $\overline{\text{DSYNC}}$ output of the COM 9026 (pin 36) and the received data input as required by the COM 9026 (pin 2). Two additional 4 MHz free running clocks are also generated on the COM 9032 to allow operation of other logic, a microprocessor, or an LSI controller.

During data reception, the COM 9032 will convert incoming serial receive data from the transmission media to NRZ form which will directly feed the RX input of the COM 9026 (pin 38). During transmission, the COM 9032 converts the transmit data from the COM 9026 ($\overline{\text{TX}}$, pin 37) into the waveforms necessary to drive opposite ends of the rf transformer used in the ARCNET* cable electronics shown in figure 2.

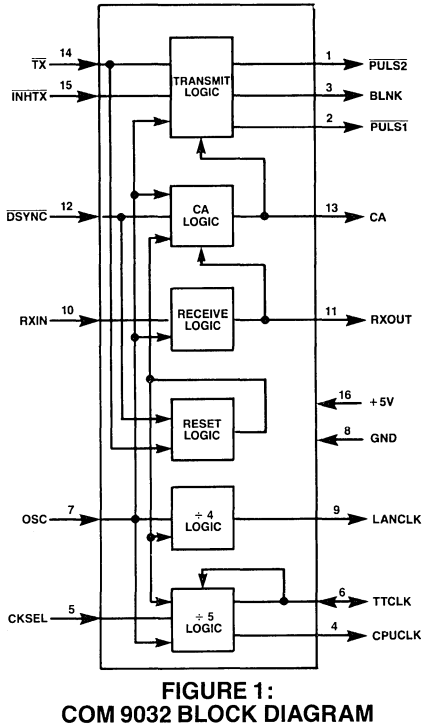
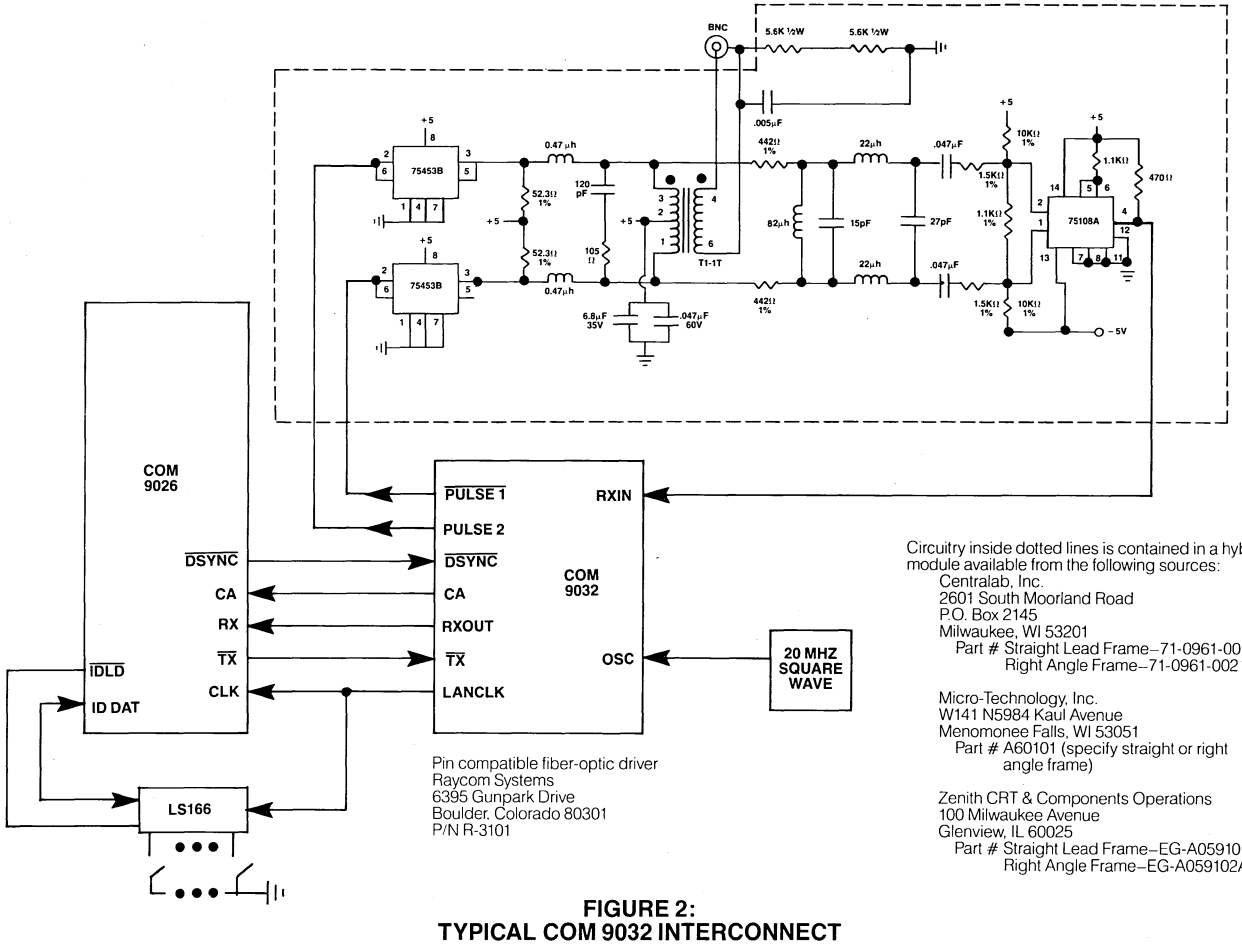



**FIGURE 1:**
**COM 9032 BLOCK DIAGRAM**

*ARCNET is a registered trademark of the Datapoint Corporation.




Pin compatible fiber-optic driver
Raycom Systems
6395 Gunpark Drive
Boulder. Colorado 80301
P/N R-3101

Circuitry inside dotted lines is contained in a hybrid module available from the following sources:

Centralab, Inc.
2601 South Moorland Road
P.O. Box 2145
Milwaukee, WI 53201
Part # Straight Lead Frame–71-0961-001
Right Angle Frame–71-0961-002

Micro-Technology, Inc.
W141 N5984 Kaul Avenue
Menomonee Falls, WI 53051
Part # A60101 (specify straight or right angle frame)

Zenith CRT & Components Operations
100 Milwaukee Avenue
Glenview, IL 60025
Part # Straight Lead Frame–EG-A059101A
Right Angle Frame–EG-A059102A

**FIGURE 2:**
**TYPICAL COM 9032 INTERCONNECT**

## DESCRIPTION OF PIN FUNCTIONS

(Refer to figure 2)

### COM 9026 INTERFACE

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1, 2 | PULSE 2<br>PULSE 1 | $\overline{PULS2}$<br>$\overline{PULS1}$ | $\overline{PULS2}$ and $\overline{PULS1}$ are two nonoverlapping negative pulses which occur every time the $\overline{TX}$ input is pulsed. $\overline{PULS2}$ and $\overline{PULS1}$ are used to feed an external driver as shown in figure 2. |
| 3 | BLANK | BLNK | When used with the circuitry shown in figure 2, this output should be left unconnected. The timing of this signal is shown in figure 4. |
| 10 | RECEIVE IN | RXIN | This input is the recovered receive data from the network. For each dipulse appearing on the network, the comparator shown in figure 2 will produce a positive pulse which directly feeds this input. |
| 11 | RECEIVE OUT | RXOUT | This output is the NRZ data generated as a function of the RXIN pulse waveform which directly feeds the RX input of the COM 9026 (pin 38). |
| 12 | DELAYED SYNC | $\overline{DSYNC}$ | This active low input, which is asserted by the COM 9026, will halt the CA clock output. |
| 13 | CA | CA | This output is a 5 MHz start/stop clock that is halted when $\overline{DSYNC}$ goes active low and restarted by a low signal on the RXOUT output. This clock is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times. |
| 14 | TRANSMIT DATA | $\overline{TX}$ | This input, which is asserted by the COM 9026, is the serial data transmitted by the node. |
| 15 | TRANSMIT INHIBIT | $\overline{INHTX}$ | This active low input inhibits the $\overline{TX}$ signal from initiating transmit signals by forcing $\overline{PULS1}$ and $\overline{PULS2}$ to a high and BLNK to a low. This signal should be asserted during a power on reset condition. |

### SYSTEM CLOCK INTERFACE

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 4 | CPU CLOCK | CPUCLK | This output is a 4 MHz free running clock capable of driving 130 pf with 30 nanosecond rise and fall times. It is identical to the TTLCLK input when CKSEL is high. When CKSEL is low, this output becomes the inversion of the signal that is fed into the TTLCLK input. |
| 5 | CLOCK SELECT | CKSEL | This input selects the clock interface option for the TTLCLK and CPUCLK. When this signal is high, both the TTLCLK and CPUCLK are identical 4 MHz free running clock outputs which are generated from the 20 MHz input clock (OSC) via a divide by 5 frequency divider. When this input is low, the TTLCLK pin becomes an input and the CPUCLK output will produce the inversion of the signal appearing on TTLCLK input. |
| 6 | TTL CLOCK | TTLCLK | This pin can be either an input or an output depending on the state of the CKSEL input. When CKSEL is high, a free running 4 MHz clock is ouput. When CKSEL is low, the pin becomes an input which drives an inverter that feeds the CPUCLK output. |
| 7 | OSCILLATOR | OSC | This input requires a 20 MHz clock. |
| 9 | LOCAL AREA NETWORK CLOCK | LANCLK | This output will supply the free running 5 MHz clock to the COM 9026, pin 19. It is capable of driving 70 pf plus one LS load with 20 nanoseconds rise and fall times. |
| 8 | GROUND | GND | Ground |
| 16 | +5 VOLT SUPPLY | $V_{CC}$ | Power Supply |

## FUNCTIONAL DESCRIPTION

**Transmit logic** (refer to figures 2 and 4)

The COM 9026, when transmitting data on $\overline{TX}$, will produce a negative pulse of 200 nanoseconds in duration to indicate a logic "1" and no pulse to indicate a logic "0". Refering to figure 4, a 200 nanosecond pulse on $\overline{TX}$ is converted to two, 100 nanosecond nonoverlapping pulses shown as $\overline{PULS1}$ and $\overline{PULS2}$. The signals $\overline{PULS1}$ and $\overline{PULS2}$ are used to create a 200 nanosecond wide dipulse by driving opposite ends of the RF transformer shown in figure 2.

**Receive logic** (refer to figures 2 and 5)

As each dipulse appears on the cable, it is coupled through the RF transformer, passes through the matched filter, and feeds the 75108B comparator. The 75108B produces a positive pulse for each dipulse received from the cable. These pulses are captured by the COM 9032 and are converted to NRZ data with the NRZ data bit boundaries being delayed by 5 OSC clock periods as shown in figure 5. As each byte is received by the COM 9026, the CA clock is stopped by the COM 9026 (via $\overline{DSYNC}$) until the first bit of the next byte is received which will automatically restart the CA clock. The COM 9026 uses the CA clock to sample the NRZ data and these sample points are shown in figure 5.

Typically, RXIN pulses occur at multiples of the transmission rate of 2.5 MHz (400 nanoseconds). The COM 9032 can tolerate distortion of plus or minus 100 nanoseconds and still correctly capture and convert the RXIN pulses to NRZ format.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −55° to 150°C
Lead Temperature (soldering, 10 sec.) ..... 325°C
Positive Voltage on any Pin ..... +8V
Negative Voltage on any Pin ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**DC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| INPUT VOLTAGES | | | | | |
| $V_{IH}$ | 2.7 | | | V | |
| $V_{IL}$ | | | 0.8 | V | |
| OUTPUT VOLTAGES | | | | | |
| $V_{OH1}$ | 2.4 | | | V | $I_{OH}$ = −0.4 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs. |
| $V_{OL1}$ | | | 0.4 | V | $I_{OL}$ = 4.0 mA, $\overline{PULS1}$, $\overline{PULS2}$, BLNK, RXOUT and TTLCLK outputs. |
| $V_{OH2}$ | $V_{CC}$-0.5 | | | V | $I_{OH}$ = −0.1 mA, CPUCLK output. |
| $V_{OL2}$ | | | 0.4 | V | $I_{OL}$ = 0.1 mA, CPUCLK output. |
| $V_{OH3}$ | $V_{CC}$-0.5 | | | V | $I_{OH}$ = −0.1 mA, CA and LANCLK outputs. |
| $V_{OL3}$ | | | 0.4 | V | $I_{OL}$ = 0.4 mA, CA and LANCLK outputs. |
| LEAKAGE CURRENT | | | | | |
| $I_{11}$ | | | 50 | µA | TTLCLK input with CKSEL low. |
| $I_{12}$ | | | 10 | µA | all other inputs. |
| INPUT CAPACITANCE | | | | | |
| $C_{IN}$ | | | 20 | pf | |
| SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 20 | mA | at 20 MHz OSC frequency. |

**AC CHARACTERISTICS**

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| OSC Input | | | | | |
| $t_{CY1}$ | | 50 | | ns | |
| $t_{CH1}$ | 20 | | | ns | |
| $t_{CL1}$ | 20 | | | ns | |
| CA, LANCLK | | | | | |
| $t_{CY2}$ | | 200 | | ns | |
| $t_{CH2}$ | 75 | | | ns | |
| $t_{CL2}$ | 75 | | | ns | |
| $t_{F2}$ | | | 20 | ns | |
| $t_{R2}$ | | | 20 | ns | |
| TTLCLK | | | | | |
| $t_{CY3}$ | | 250 | | ns | |
| $t_{CH3}$ | 110 | | | ns | |
| $t_{CL3}$ | 110 | | | ns | |
| CPUCLK (CKSEL is high) | | | | | |
| $t_{CY4}$ | | 250 | | ns | |
| $t_{CH4}$ | 110 | | | ns | |
| $t_{CL4}$ | 110 | | | ns | |
| $t_{F4}$ | | | 30 | ns | |
| $t_{R4}$ | | | 30 | ns | |
| $t_{DCK}$ | | | 45 | ns | for CKSEL low. |
| TRANSMIT TIMING | | | | | |
| $t_{STC}$ | 50 | 30 | | ns | |
| $t_{HTC}$ | 10 | | | ns | |
| $t_{DP}$ | | | 60 | ns | |
| $t_{P1W}$ | | $2t_{CY1}$ | | ns | |
| $t_{WB}$ | | $t_{CY1}$ | | ns | |
| $t_{P2W}$ | | $2t_{CY1}$ | | ns | |
| $t_{RST}$ | | | 40 | ns | |
| RECEIVE TIMING | | | | | |
| $t_{RS}$ | 30 | | | ns | |
| $t_{RW}$ | 10 | | | ns | |
| $t_{DO}$ | | | 70 | ns | |
| $t_{RO}$ | | $5t_{CY1} + t_{DO}$ | | ns | |
| $t_{SSO}$ | 10 | | | ns | |
| $t_{SSC}$ | | 20 | | ns | |
| $t_{ROW}$ | | 400 | | ns | |

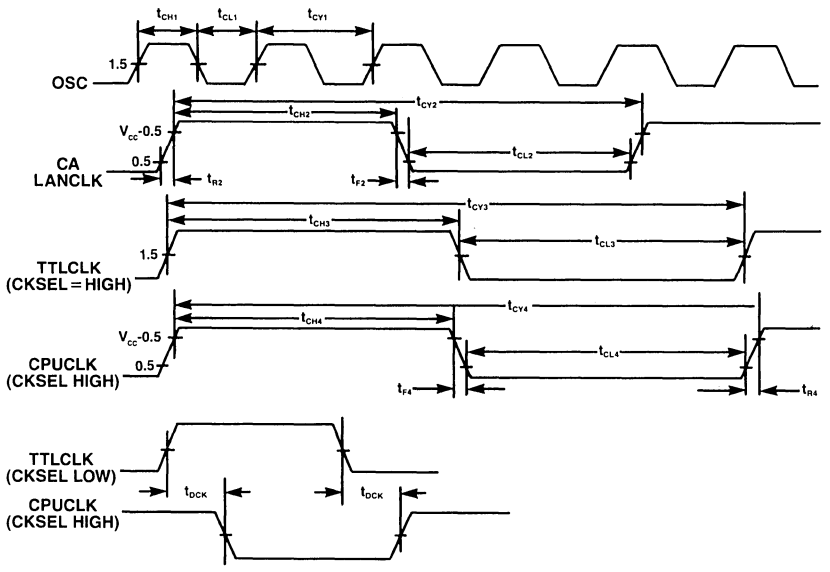



**FIGURE 3: CLOCK TIMING**

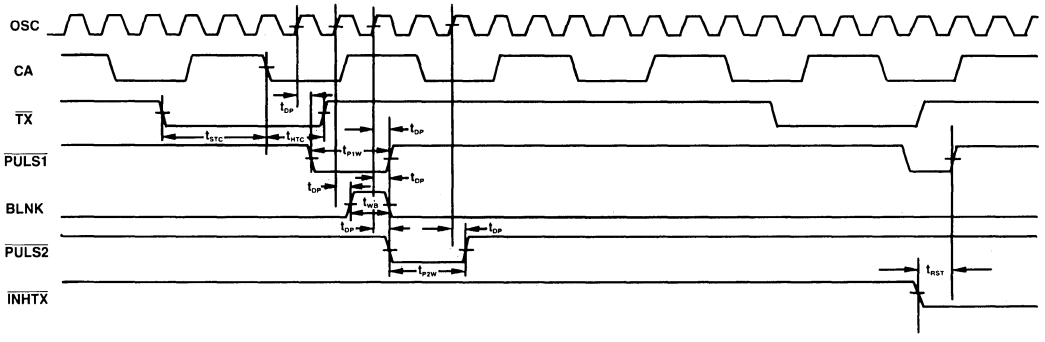



**FIGURE 4: TRANSMIT TIMING PARAMETERS**

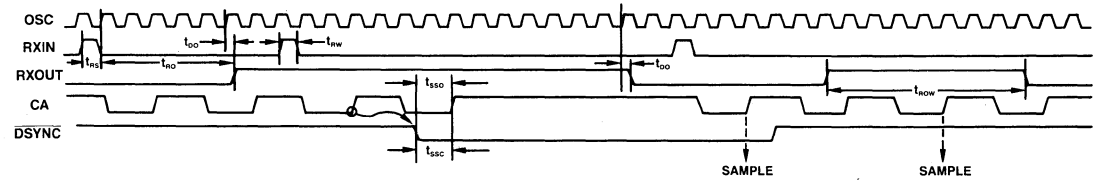



**FIGURE 5: RECEIVE TIMING PARAMETERS**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 · TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM9046

**PRELIMINARY**

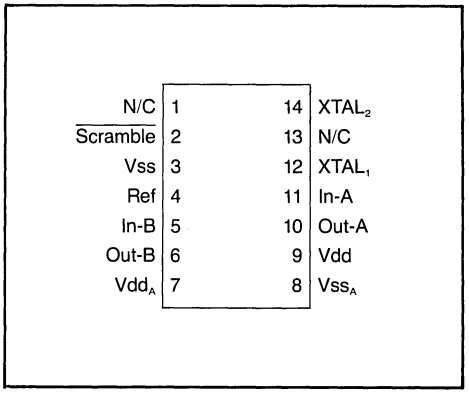


# Single Side Band Speech Scrambler

## FEATURES

- ☐ Speech Scrambling/Descrambling
- ☐ High Dynamic Range
- ☐ Low Voltage Operation
- ☐ Low Power Consumption
- ☐ On Board Crystal Oscillator
- ☐ Uses Common Color Burst Crystal
- ☐ Full Duplex Operation
- ☐ Selectable Scramble Enable/Disable
- ☐ Switched Capacitor Filter
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The COM9046 is a monolithic integrated circuit containing a voice scrambler, a descrambler and a crystal oscillator. It is designed to provide speech communication equipment with a privacy feature. The COM9046 is also designed to operate with power supply voltages as low as ±2Volts. The low voltage operation and low power consumption of the COM9046 make it ideal for use in portable equipment.

Two identical speech channels are contained in the COM9046 for full duplex operation. Either channel is capable of performing the scrambling or descrambling function. These functions can be enabled or disabled via an external pin. The on-board oscillator employs an inexpensive 3.58 MHz TV color-burst crystal. Switched capacitor techniques are used to perform analog signal processing in the COM9046.

Typical applications for the COM9046 are Voice Communications, Cellular Phones, Wireless Phones, PBX's, Dictation Machines, Two-way Radios and Audio Recording Equipment.

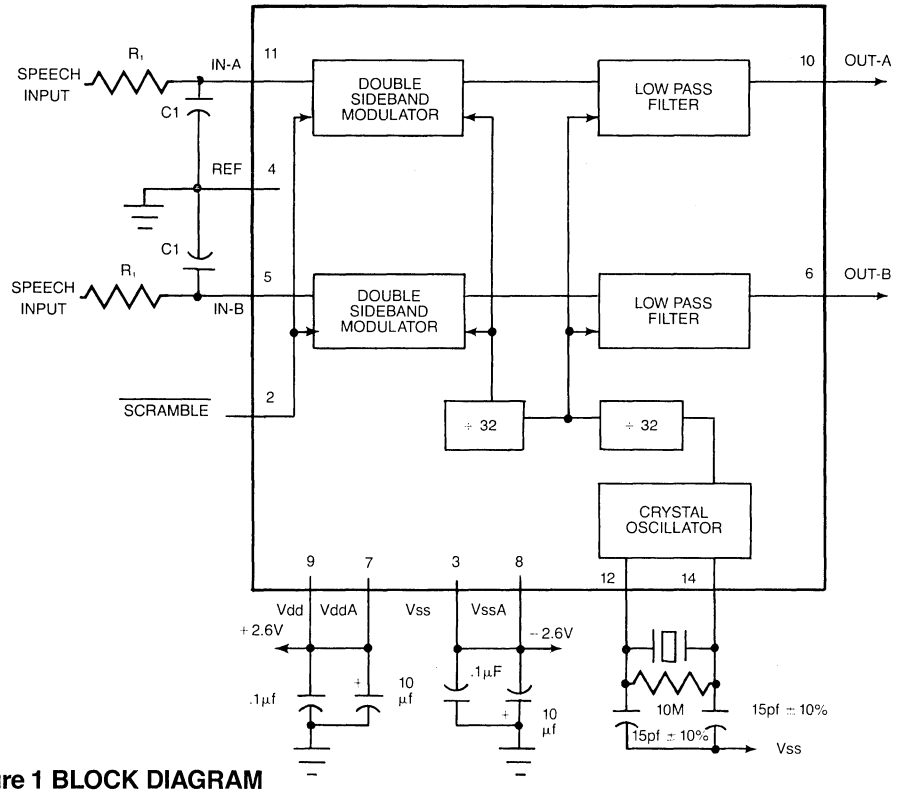



**Figure 1 BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN # | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | N/C | | No Connection |
| 2 | Scramble | — | Vss applied to this pin asserts the scramble; Vdd asserts non-scramble. |
| 3 | Digital Supply | Vss | Negative digital supply. Vss is typically −2.6 volts with respect to pin 4. |
| 4 | Ref Input | Ref | Analog ground or mid-supply voltage. This is the chip 0 volt reference. |
| 5 | Audio Input B | In-B | Channel B audio input. D.C. voltage must be 0V with respect to pin 4. |
| 6 | Audio Output B | Out-B | Channel B audio output. DC voltage is 0V typical with respect to pin 4. |
| 7 | Analog Supply | $Vdd_A$ | Positive analog supply. Vdd is typically +2.6 volts with respect to pin 4. |
| 8 | Analog Supply | $Vss_A$ | Negative analog supply. $Vss_A$ is typically −2.6 volts with respect to pin 4. |
| 9 | Digital Supply | Vdd | Positive digital supply. Vss is typically +2.6 volts with respect to pin 4. |
| 10 | Audio Output A | Out-A | Channel A audio output. DC voltage is 0V typical with respect to pin 4. |
| 11 | Audio Input A | In-A | Channel B audio input. D.C. voltage must be 0V with respect to pin 4. |
| 12 | Crystal input/ Ext Clock | $XTAL_1$ | Crystal Oscillator input or external clock. External clock frequency should be 3.58MHz with an amplitude of 4Vp-p and 0VDC. |
| 13 | N/C | — | No connection |
| 14 | Crystal input | $XTAL_2$ | Crystal Oscillator output. This pin is left floating when external clock is applied to pin 12. |

## OPERATION

Figure 1 shows a block diagram of the chip. Also shown in Figure 1 are the required external components.

Since switched-capacitor filters are used on the chip, the input speech signal must first be filtered by an anti-aliasing one-pole low pass filter before it is applied to the Audio input pin. The filter 3dB break point, which is determined by the product of C1 and R1 plus the output impedance of the audio source, should be less than 20KHz. This filter is required only if high frequency noise is present at the input. To maintain an output signal to noise ratio of 40dB, any unwanted signal higher than 3.5KHz contained in the speech input must be filtered to 40dB below the nominal speech input level, due to the fact that the on-chip modulator is switched at 3.5KHz.

The on-chip double sideband modulator can be turned on or off by asserting the SCRAMBLE input pin. The 3.5KHz switching frequency of the modulator is generated by dividing the output of the oscillator by 1024. The modulator output contains two sidebands centered at the suppressed switching frequency of 3.5KHz. The upper sideband is attenuated by a 4th order Butterworth lowpass filter. The filter, consisting of two biquad switched capacitor filters in cascade, is clocked at 111.9KHz. The inverted input speech spectrum appears at the filter output, and is available at the Audio Output pin. The filter output circuit is designed to drive a maximum capacitive load of 5pf in parallel with a minimum resistance of 15K ohms.

A parallel resonant crystal oscillator is employed in the device. The parallel resonant crystal should have a maximum series resistance of 150 ohms with a shunt capacitance of 5pf. To insure reliable oscillator performance, the components shown connected to XTAL pins 14 and 12 in Figure 1 should be used.



## ELECTRICAL CHARACTERISTICS — COM9046

### MAXIMUM GUARANTEED RATINGS*:

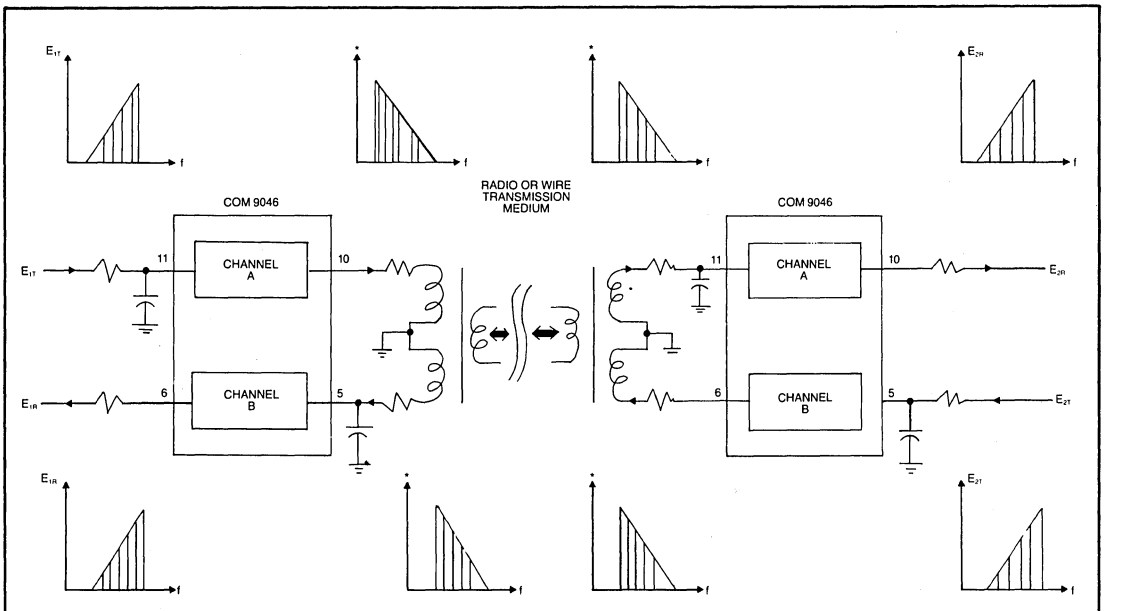
| | |
|---|---|
| Operating Temperature Range | −15°C to +55°C |
| Storage Temperature Range | −55°C to +125°C |
| Lead Temperature (soldering, 10 sec.) | +325°C |
| Positive Voltage on any pin with respect to Vss | +6.5 V |
| Negative Voltage on any pin with respect to Vss | −0.3 V |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

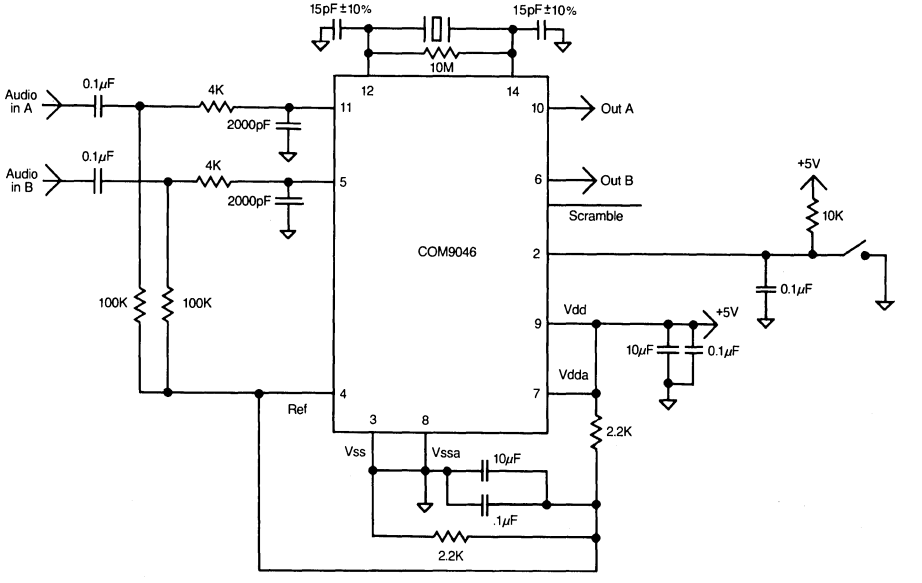
**ELECTRICAL CHARACTERISTICS** (Ta = −10°C to +50°C, Vdd = $Vdd_A$ = +2.6V ±5%, Vss = $Vss_A$ = −2.6V ±5%.)

| Parameter | Min | Typ | Max | Units | Comments |
|---|---|---|---|---|---|
| Supply Current | | 5 | 8 | ma | |
| Insertion Loss | | 0 | 1 | db | |
| Audio Voltage Swing | | 0.8 | 1 | Vp-p | |
| S/N Ratio | 40 | | | db | |
| Modulation Frequency | | 3.5 | | KHz | |
| Bandedge of Sideband Filter | | 3.2 | | KHz | |
| Scramble Input High | Vdd-1.0 | | Vdd | V | |
| Scramble Logic Low | Vss | | Vss+.3 | V | |
| Input Resistance | | 5 | | M Ohm | |
| Dynamic Output Resistance | | 900 | | Ohm | |
| 3.5KHz Feedthrough | | −60 | −50 | db | |




## Figure 2 TYPICAL APPLICATION

*Inverted Frequency Spectrum of the Inspect Signals are Transmitted on the Transmission Medium.




**RECOMMENDED CONNECTION FOR SINGLE +5V SUPPLY OPERATION**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM90C56
**PRELIMINARY**

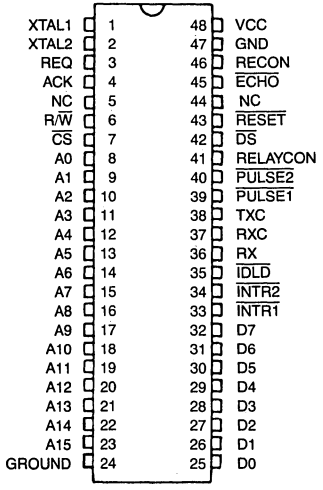
SECTION III

# Enhanced Local Area Network Controller ELANC

## FEATURES

- ☐ 5.0/2.5 M bit data rates
- ☐ 100% compatible with COM9026 (in slow mode) ARCNET local area network controller
- ☐ 64 K byte shared buffer memory
- ☐ Handles variable length data packets (up to 2 K long)
- ☐ Supports up to 255 nodes per network segment
- ☐ Allows 8/16 bit word per sync to enhance line efficiency
- ☐ Allows for nodal priority
- ☐ Supports event scheduling via buffer descriptors
- ☐ On board GP event counters (4) to monitor the network
- ☐ On chip network diagnostics
- ☐ Duplicate ID detection/prevention
- ☐ Node list/Group list requests
- ☐ Provides mail distribution capabilities
- ☐ Supports group broadcast messages
- ☐ Provides the hooks for broadband systems (modem)
- ☐ Internal/external loopback capability for self test
- ☐ Ram buffer test capability
- ☐ On board oscillator
- ☐ Low power CMOS technology
- ☐ 48 pin D.I.P. plastic package or PLCC
- ☐ Single +5v Supply
- ☐ Compatible with HYC9058, HYC9068, HYC9078

## PIN CONFIGURATION*




PACKAGE: 48-pin D.I.P.

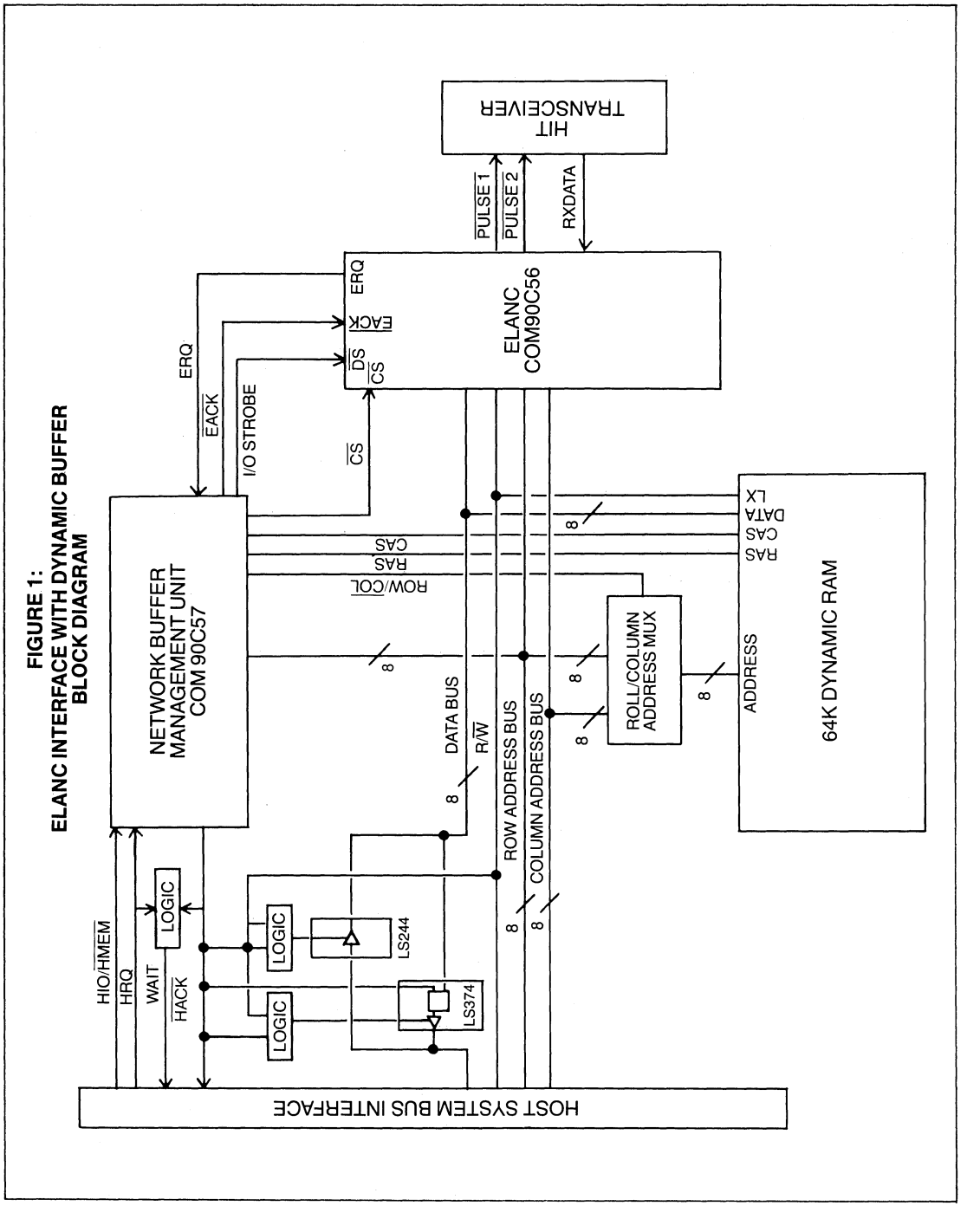
*Available in PLCC

Pin configuration subject to change, contact factory for details.

## GENERAL DESCRIPTION

The ELANC is a general purpose communications adapter designed to provide high speed intercommunication between a number of intelligent electrical machines. Data is carried over a variable media (twisted pair, coax, or fiber optics) in variable size packets up to 2048 bytes long at speeds of up to 5.0 Mbps. The interconnection of several nodes through their associated ELANCs forms an enhanced local area network. Each node has a unique ID number from 1 to 255 to distinguish it from other nodes on the same network.

**FIGURE 1:**
**ELANC INTERFACE WITH DYNAMIC BUFFER BLOCK DIAGRAM**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**COM90C57**
**PRELIMINARY**

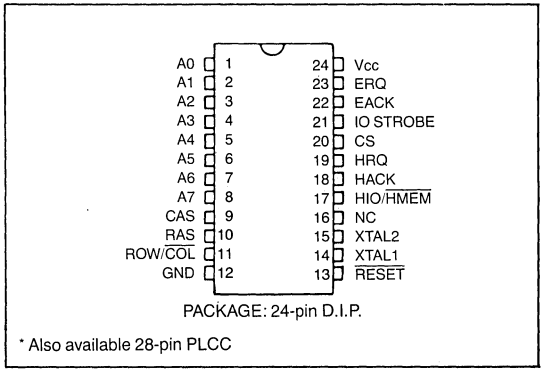


# Network Buffer Management Unit NBMU

## FEATURES

- ☐ Auto refresh cycle generation
- ☐ Refresh 64K DRAM
- ☐ Compatible with SMC's COM90C56 Enhanced Local Area Network Controller (ELANC)
- ☐ Low power CMOS
- ☐ Replaces several MSI/LSI devices
- ☐ Simplifies the interface of COM90C56 to lower cost DRAM
- ☐ Single +5v supply

## PIN CONFIGURATION*




PACKAGE: 24-pin D.I.P.

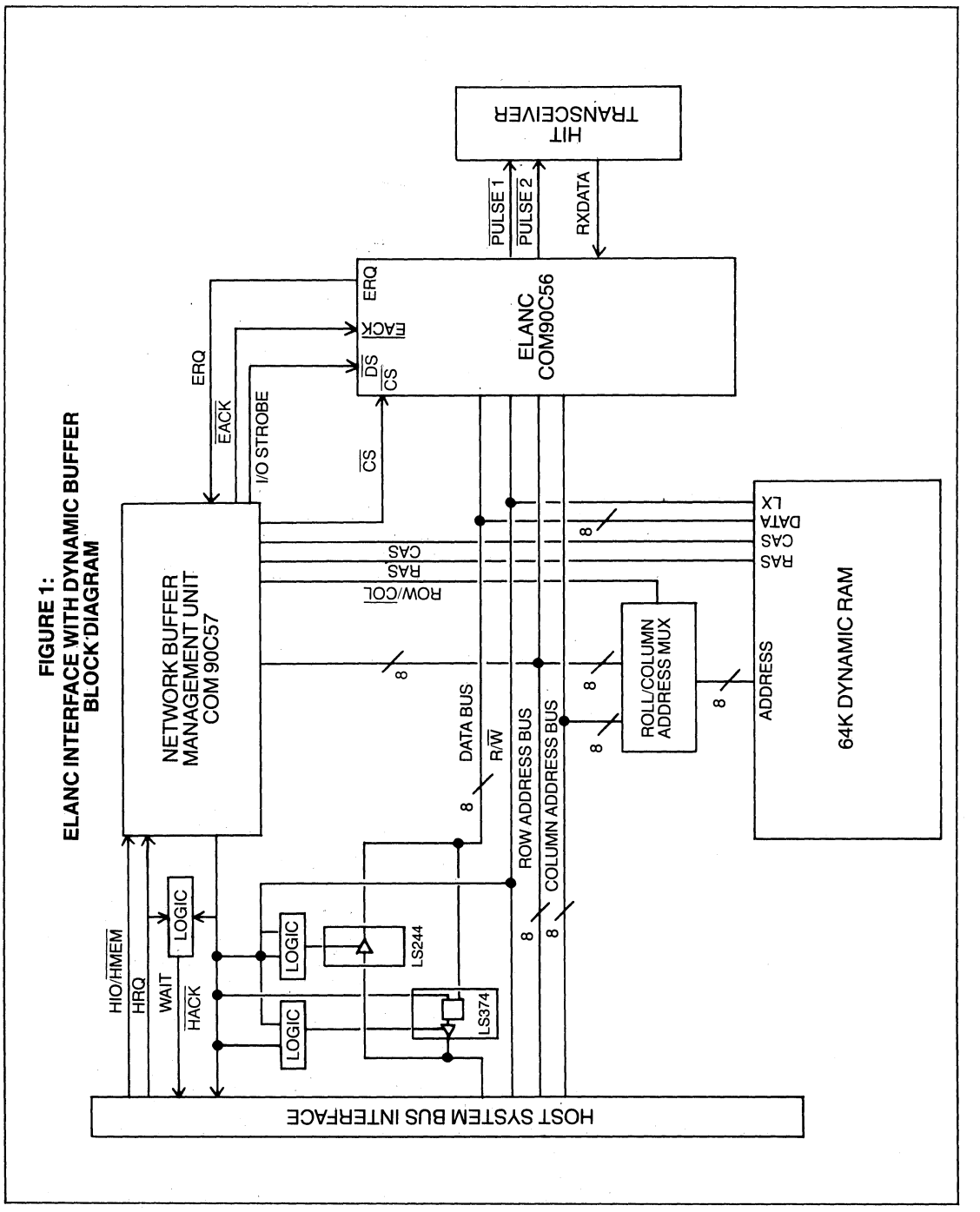
* Also available 28-pin PLCC

Pin configuration subject to change, contact factory for details.

## GENERAL DESCRIPTION

The NBMU provides the arbitration and memory control required to manage a dynamic memory buffer which is shared by the ELANC and a Host processor. Both access arbitration and dynamic memory refresh are taken care of by the NBMU so that minimal additional circuitry is required to construct an efficient shared dynamic memory buffer interface between the ELANC and a Host system. Figure 1 shows how such an interface might be constructed using the NBMU.

**FIGURE 1:**
**ELANC INTERFACE WITH DYNAMIC BUFFER**
**BLOCK DIAGRAM**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**COM 9064**
**PRELIMINARY**

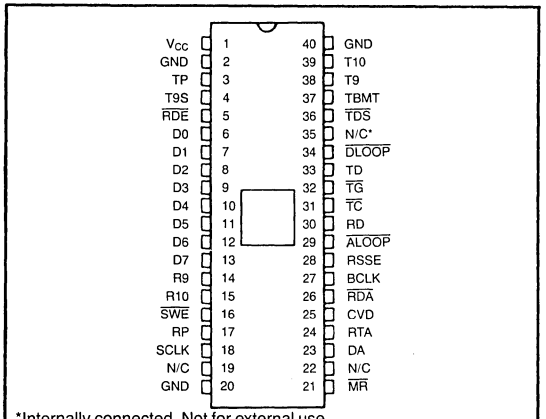
# IBM® 3274/3276 Compatible COAX Receiver/Transmitter



## FEATURES

- ☐ Conforms to the IBM® 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Single +5 Volt power supply

## PIN CONFIGURATION**




*Internally connected. Not for external use.

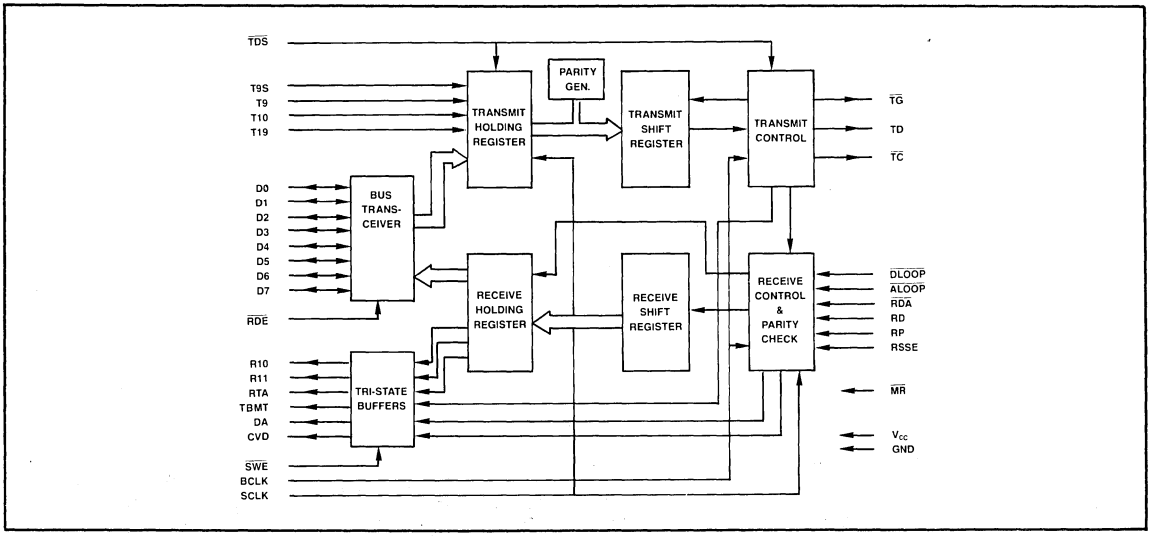
**PLCC (J LEAD QUAD PACK) also available.

## GENERAL DESCRIPTION

The COM 9064 is an MOS/LSI circuit which may be used to facilitate high speed data transmission. The COM 9064 is fabricated using SMC's patented COPLAMOS® technology and may be used to implement an interface between IBM® 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. The receiver and transmitter sections of the COM 9064 are separate and may be used independently of each other.

The COM 9064 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit).




IBM® is a registered trademark of the International Business Machines Corporation

## ORGANIZATION

The COM 9064 is organized into 9 major sections. Communication between each section is achieved via internal data and control busses.

### Transmitter Holding Register

The transmit holding register is a 12 bit latch. This latch is loaded with the transmit data and parity generation information from the system bus.

### Tri-State Buffers

These buffers allow gating of the COM 9064's status word onto the system data bus.

### Bus Transceiver

The bus transceiver allows bi-directional data transfer between the system data bus and the transmit and receive holding registers.

### Parity Generator

This logic determines and generates the correct parity for the data in the transmitter holding register.

### Transmitter Control

This logic generates signals required to enable external transmit circuitry. It also generates the Line Quiesce, Code Violation, sync bits and Mini Code Violation patterns.

### Transmitter Shift Register

The transmitter shift register is an 11 bit parallel to serial shift register. It accepts data from the transmitter holding register and the parity generation logic and converts it into serial form for transmission.

### Receive Control/Parity Check

This logic checks the received character for the specified parity and ensures that no Transmit Check conditions occurred. It also handles the self test mode and generates a strobe when the complete data word is received.

### Receiver Shift Register

This logic is a serial to parallel shift register that converts the received information into a 10 bit data word and RTA status bit.

### Receiver Holding Register

This register holds the assembled data word until it is read by the processor.

## DESCRIPTION OF PIN FUNCTIONS
## Processor Related Signals

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 6-13 | Transmit/ Receive Data Bits | D0-D7 | Bidirectional: 8 bit, three state data port used to transfer data between the COM 9064 and the processor. D0 is the first bit transmitted. |
| 4 | Transmit Bit 9 Select | T9S | Input: A low level on this pin enables T9 to be transmitted as bit 9. A high level on this pin causes T9 to determine the type of parity bit generated for bits D0-D7. |
| 38 | Transmit Bit 9 | T9 | Input: If T9S is low, this supplies transmit bit 9. If T9S is high, then T9 low forces odd parity and T9 high forces even parity to be generated for D0-D7. In this case the parity bit generated is transmit bit 9. |
| 39 | Transmit Bit 10 | T10 | Input: This pin supplies transmit bit 10. |
| 3 | Transmit Parity | TP* | Input: This input controls the parity bit for transmit bits 1-10. A low level on this pin causes odd parity and a high level on this pin causes even parity to be generated for bits 1-10. The parity bit generated is transmit bit 11. |
| 18 | System Clock | SCLK | Input: This signal is used to synchronize the COM 9064. The transmitter is loaded and started on the low to high transition of SCLK if TDS is low. DA is reset on the low to high transition of SCLK if RDA is low. |
| 36 | Transmitter Data Strobe | $\overline{TDS}$ | Input: This input and SCLK are used to load the transmitter holding register and start the transmit sequence. Code Violation Detect (CVD) is reset at this time. |
| 26 | Reset Data Available | $\overline{RDA}$ | Input: This input and SCLK are used to reset DA. |
| 16 | Status Word Enable | $\overline{SWE}$ | Input: A low level at this pin enables the status word buffer outputs (DA, CVD, TBMT, R9, R10, and RTA). A high level on $\overline{SWE}$ places the status word buffer outputs in a high impedance state. |
| 23 | Receive Data Available | DA | This three-state output signal is at a high level when an entire word has been received and transferred into the receiver buffer register. It is only set if a Transmit Check Condition did not occur. |
| 25 | Code Violation Detected | CVD | This three-state output signal is at a high level if a valid Code Violation was detected at the receiver since the last time the transmitter was loaded. It is reset when the transmitter is loaded. |
| 37 | Transmit Buffer Empty | TBMT | This three-state output signal is at a high level when the transmit holding register may be loaded with new data. |
| 14 | Receive Bit 9 | R9 | This three-state output signal is receiver data bit 9. |
| 15 | Receive Bit 10 | R10 | This three-state output signal is receiver data bit 10. |
| 24 | Recever Turn-around | RTA | This three-state output signal is set to a high level when a valid Mini Code Violation is detected. It is only set if a Transmit Check did not occur. It is reset when the transmitter is loaded. |
| 5 | Receive Data Enable | $\overline{RDE}$ | Input: A low level enables the outputs of the receive data register D0-D7. |
| 17 | Receiver Parity | RP* | Input: This input determines whether the entire received word will be checked for even or odd parity. A low at this pin will cause a check for odd parity and a high at this pin will cause a check for even parity. This input has an internal pull-up resistor. |

*The SYNC bit is included in parity checking.

## DESCRIPTION OF PIN FUNCTIONS (cont.)

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 29 | Analog Loopback | $\overline{ALOOP}$ | Input: A low level on this pin disables the receiver except when the transmitter is active. A high level on this pin and $\overline{DLOOP}$ will cause the receiver to be disabled while the transmitter is active. $\overline{ALOOP}$ is used to allow loop-back through the line drivers and receivers. This input has an internal pull-up resistor. |
| 34 | Digital Loopback | $\overline{DLOOP}$ | Input: A low level on this pin disables the receiver except when the transmitter is active. $\overline{TG}$ is forced to a high level to disable the external coax driver. Data input to the receiver is internally wrapped from the transmitter data output. This input has an internal puil-up resistor. |
| 21 | Master Reset | $\overline{MR}$ | Input: This input should be pulsed low after power-on. This signal resets DA to a low level and sets $\overline{TG}$ and TBMT to a high level. This input has an internal pull-up. |
| 1 | Supply Voltage | $V_{cc}$ | +5 volt supply |
| 19, 22, 35 | | N/C | No Connection |
| 2, 20, 40 | Ground | GND | GROUND |

### Device Related Signals

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 27 | Baud Rate Clock | BCLK | This input is a clock whose frequency is 8 times the desired transmitter and receiver baud rate (typically 18.8696 MHz for 3274/3276 operation). This input is not TTL compatible. |
| 33 | Transmit Data | TD | Output: Serial data from the transmitter. This signal is a biphase Manchester II encoded bit stream. This output is low when no data is being transmitted. |
| 31 | Transmit Clock | $\overline{TC}$ | The Transmit Clock output is ½ the frequency of BCLK. It is synchronized with TD and used to provide external pre-distortion timing. |
| 30 | Receive Data | RD | Input: Accepts the serial biphase Manchester II encoded bit stream. |
| 32 | Transmit Gate | $\overline{TG}$ | Output: This signal is low during the time that the transmit data is valid. TG is used to turn on the external transmit circuitry. |
| 28 | Receive Single Shot Enable | RSSE | Input: A high level on this pin enables an internal digital single shot on RD. This limits a high level on RD to 3 clock times. Also when high it will cause the receiver not to detect a valid Code Violation. A low level disables the single shot causing no reshaping of the RD input signal. |

## COM 9064 OPERATION

The COM 9064 consists of a receiver section that converts Manchester II phase encoded serial data to parallel data and a transmitter section that converts parallel data to Manchester II phase encoded serial data.

### Receiver

Message transfers must conform to the IBM 3270 protocol in order for the COM 9064 to acknowledge them.

The received message is checked for the Code Violation sequence (start sequence) bit pattern, preceding the first data word, and Mini Code Violation (end sequence) following the last data word.

The data word consists of 10 data bits, a sync bit and a parity bit. Receiving data in multiple byte format is functional only when even parity is selected.

The data word along with the first bit of the next word or ending zero (bit 13) is shifted into a shift register. Once it is assembled it is transferred and held in the holding register until another data word is assembled. The 13th bit is inverted and presented to the bus or RTA (receiver turn-around). Therefore RTA is set high on the last word of a message and is reset when the transmitter is loaded with the response.

Once the data word is in the holding register and parity is correct the data available (DA) status signal is set high.

The Code Violation Detect signal (CVD) goes active high after a line Quiesce, Code Violation and sync bit have been detected by the receiver. It is reset when the transmitter of the COM 9064 is asserted. By examining this signal, the processor can determine whether a timeout or Transmit Check condition caused a receiver error.

The receive input is sampled at 8 times the data rate. The receiver logic is brought into bit synchronization during the Line Quiesce pattern. Once the Code Violation following the Line Quiesce is detected, the receiver is brought into bit and word synchronization. The internal receiver clock is adjusted after each transition to compensate for jitter and distortion in the received data signal.

### Transmitter

The transmitter section basically consists of a 12-bit holding register, parallel to serial shift register and a parity generator. The firmware initiates a transmit sequence by strobing $\overline{TDS}$ low. The data is loaded into the holding register on the rising edge of SCLK while TDS is low. Nine bits of data (D0-D7 and T10) are transferred without change to the transmit shift register. The logic level of T9S determines whether T9 will be transmitted as parity on the preceding eight bits, or as data.

After the processor loads the transmit holding register with data, status signal TBMT is driven inactive low until the COM 9064 transfers the data from the transmit holding register

to the transmit shift register. After the transfer, TBMT is driven high. The processor should not try to load data into the COM 9064 while TBMT is low. When initiating a data transmission, the COM 9064 automatically transmits a Line Quiesce pattern and a Code Violation. The data is then shifted out of the shift register with a sync bit (1) inserted before the data word, and a parity bit appended after the data word.

If a new word is loaded into the COM 9064 before the parity bit of the previous word has been transmitted, a sync bit (1) followed by the new data bits is transmitted. If not, after the COM 9064 transmits the last data word (no more transmit sequences are started), a sync bit (0) and a Mini Code Violation is appended to the end of the message.

Output $\overline{TG}$ goes active low one-half bit cell time before the first Line Quiesce character is output. It is made inactive (high) during the transmission of the Mini Code Violation.

## Diagnostic Modes

**NORMAL OPERATION ($\overline{ALOOP}$ AND $\overline{DLOOP}$ HIGH)**
Internal read data signal follows the RD input as long as the COM 9064's transmitter is off. The receiver will be disabled while the transmitter is active.

**ANALOG LOOPBACK ($\overline{ALOOP}$ LOW AND $\overline{DLOOP}$ HIGH)**
The internal read data signal follows the RD input as long as the COM 9064's transmitter is active.

**DIGITAL LOOPBACK $\overline{ALOOP}$ HIGH AND $\overline{DLOOP}$ LOW)**
The internal read data signal follows an internally generated and latched valid transmit signal (only when the transmitter is active.) The output $\overline{TG}$ is disabled in digital loopback mode.

**DISABLE RECEIVER ($\overline{ALOOP}$ AND $\overline{DLOOP}$ LOW)**
The internal read data signal is held low and output $\overline{TG}$ is disabled.

## MESSAGE FORMATS

### Single Byte Transmission

| COAX IDLE | LINE QUIESCE | CODE VIOLATION | SYNC BIT | DATA (10 BITS) | PARITY BIT | ENDING SEQUENCE | COAX IDLE |
|---|---|---|---|---|---|---|---|

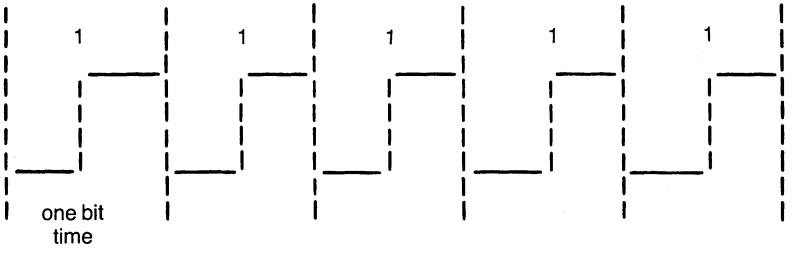
### Multiple Byte Transmission

| COAX IDLE | LINE QUIESCE | CODE VIOLATION | SYNC BIT | DATA 1 (10 BITS) | PARITY BIT | SYNC BIT | DATA 2 (10 BITS) |
|---|---|---|---|---|---|---|---|

| PARITY BIT | ..... | SYNC BIT | DATA N (10 BITS) | PARITY BIT | ENDING SEQUENCE | COAX IDLE |
|---|---|---|---|---|---|---|

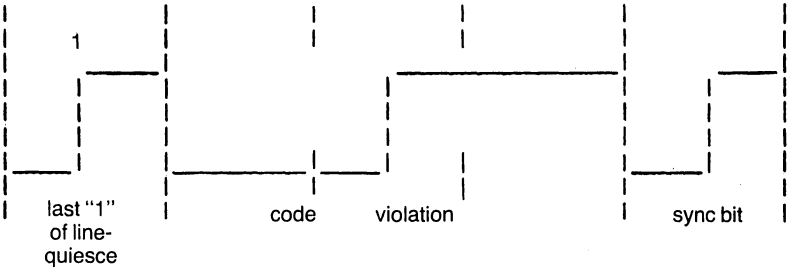
Bits on the coax appear as positive and negative going pulses. A positive pulse to negative pulse transition in the middle of the bit cell is interpreted as a logical '0'. A negative pulse to positive pulse transition in the middle of a bit cell is interpreted as a logical '1'. A predistortion pulse is generated for every pulse transition from an up to down level or a down to up level.

### Line Quiesce Pattern



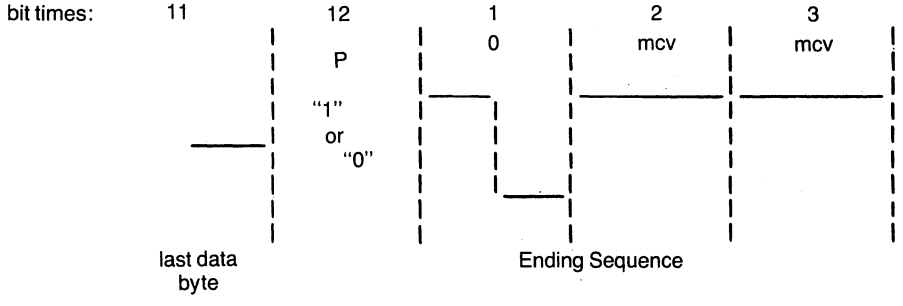

The Line Quiesce pattern consists of five contiguous logical ones. It establishes an equilibrium condition on the coax following line turnaround.

## Code Violation Pattern




The Code Violation pattern is a bit sequence containing no mid-bit time level transition in two of its three bit cells. It is a unique pattern that violates the encoding rules and indicates the start of valid data.

## Mini Code Violation Pattern




The Mini Code Violation (MCV) pattern is a bit sequence containing no mid-bit time level transition in either of its bit cells. It is a unique code that violates the encoding rules and indicates the end of valid transmit data.

## Transmit Check

A Transmit Check is defined as follows:

1) A logical zero sync bit in the ending sequence not followed by a Mini Code Violation.
2) Loss of a level transition at the mid-bit time during other than a normal ending sequence.
3) A transmission parity error.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +8.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +5 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

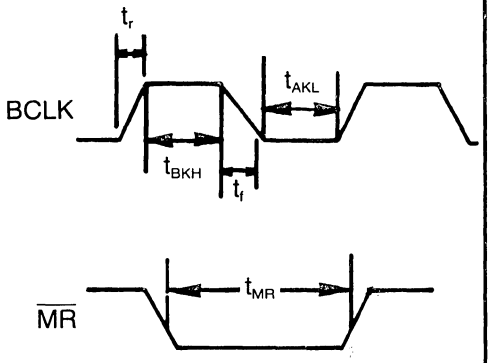
**DC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE | | | | | |
| $V_{IL}$ Low | −0.3 | | .8 | V | |
| $V_{IH}$ High | 2.0 | | $V_{CC}$ | V | (Except BCLK and $\overline{MR}$) |
| $V_{IH}$ High | 4.3 | | $V_{CC}$+.3 | V | (BCLK only) |
| $V_{IH}$ High | 3.5 | | $V_{CC}$+.3 | V | ($\overline{MR}$ only) |
| OUTPUT VOLTAGE | | | | | |
| $V_{OL}$ Low | | | .4 | | $I_{OL}$ = 2.0 mA |
| $V_{OH}$ High | 2.4 | | | | $I_{OH}$ = −.25 mA |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 125 | | mA | All outputs = $V_{OH}$ |
| INPUT LEAKAGE CURRENT | | | | | |
| All input pins | | | .01 | mA | $V_{IN}$ = 0 to $V_{CC}$ |
| CAPACITANCE | | | | | |
| $C_{IN}$ | | | 10 | pf | (Except BCLK) |
| $C_{IN}$ | | | 35 | pf | (BCLK only) |

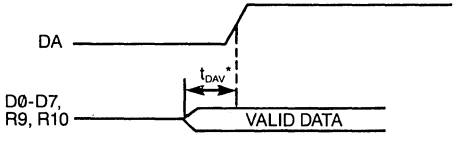
**AC ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| Clock Frequency | | | | | |
| $B_{CLK}$ | 7 | 18.8696 | 18.9 | MHz | |
| $S_{CLK}$ | DC | 4.7474 | 5 | MHz | |
| Clock Width | | | | | |
| $t_{SKH}$ SCLK High | 80 | | | ns | |
| $t_{SKL}$ SCLK Low | 80 | | | ns | |
| $t_{BKH}$ BCLK High | 20 | | | ns | |
| $t_{BKH}$ BCLK Low | 20 | | | ns | |
| $t_r$ BCLK rise time | | | 6 | ns | |
| $t_F$ BCLK fall time | | | 6 | ns | |
| $t_{RDD}$ $\overline{RDE}$ to Data Valid Delay | | | 50 | ns | |
| $t_{SDD}$ $\overline{SWE}$ to Data Valid Delay | | | 50 | ns | |
| $t_{DF}$ Data Read to Bus Float | | | 50 | ns | |
| $t_{DS}$ Data Setup Time | 100 | | | ns | |
| $t_{DH}$ Data Hold Time | 10 | | | ns | |
| $t_{DAV}$ DA to receive data valid delay | −100 | | 100 | ns | |
| $t_{TC}$ TC clock period | | 106 | | ns | |
| $t_{\overline{TGLD}}$ TC to TG low delay | −53 | | 30 | ns | |
| $t_{\overline{TGHD}}$ TC to TG high delay | | | 30 | ns | |
| $t_{TDS}$ Transmit data to TG setup time | 10 | | | ns | |
| $t_{TDH}$ Transmit data to TC hold time | 20 | | | ns | |
| $t_D$ TBMT active to de-active | | 200 | | ns | |
| $t_{TDDC}$ TBMT cycle | | | 3.2 | µs | |
| $t_{DD}$ $\overline{TBMT}$ de-activated | 1 | | 2 | µs | |
| $t_{DSS}$ $\overline{TDS}$ set up | 100 | | 200 | ns | |
| $t_{DSH}$ $\overline{TDS}$ hold | 10 | | 100 | ns | |
| $t_{MR}$ $\overline{MR}$ pulse width | 300 | | | ns | |

## MISC. TIMING

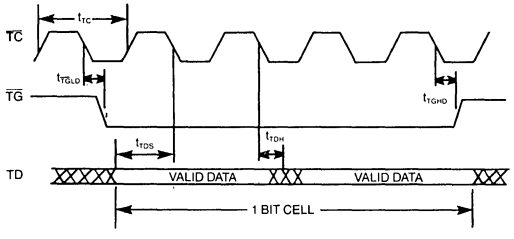



## RECEIVE DATA TIMING

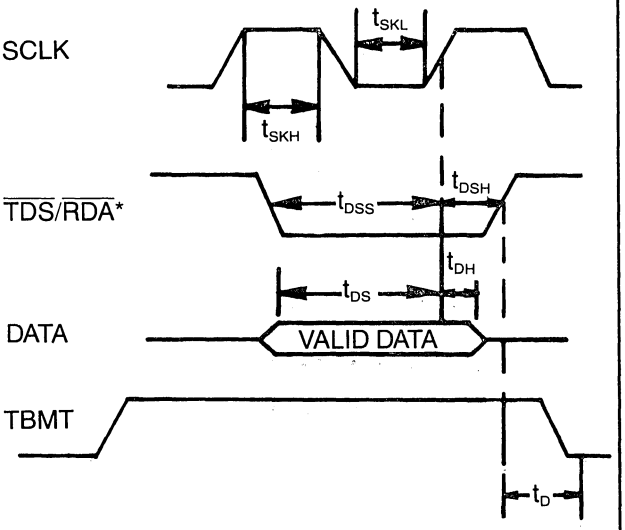



*DA may occur from 100 ns before to 100 ns after data is valid.

## TRANSMITTER TIMING

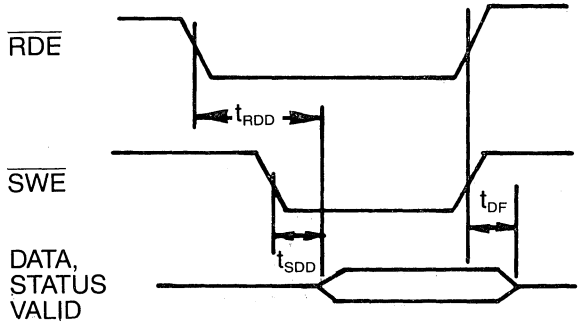



## BUS INPUT TIMING

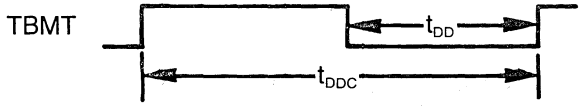


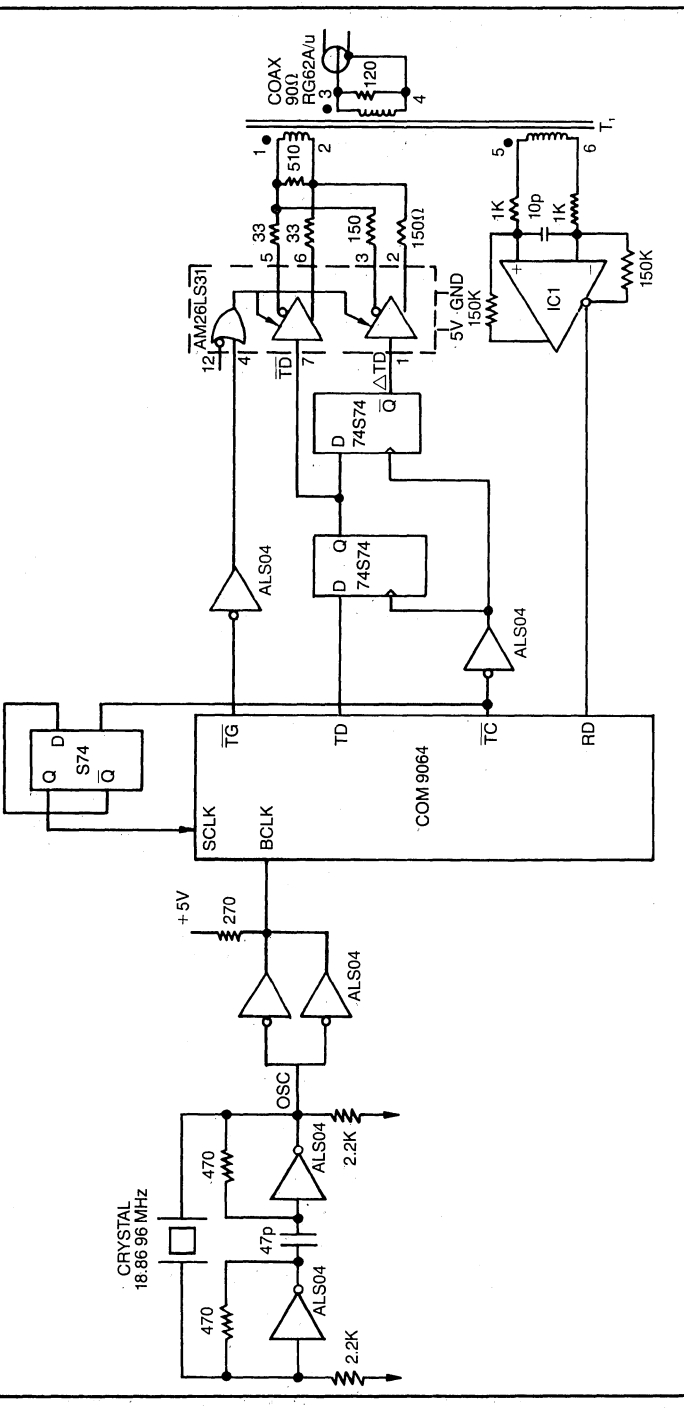

*Only one rising edge of SCLK within this pulse width.

## BUS OUTPUT TIMING




## TBMT CYCLE






NOTE: 1. T1—1:1:1 PULSE TRANSFORMER (TECHNITROL PART NO. 11LHA. PULSE ENGINEERING P N 5762 OR EQUIV.)
2. ALL RESISTOR IN OHMS
3. IC 1 COMPARATOR: FAIRCHILD μA760. SIGNETICS NE529 OR NATIONAL LM361

**TYPICAL COAX INTERFACE**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications: consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# HYC9058

**PRELIMINARY**

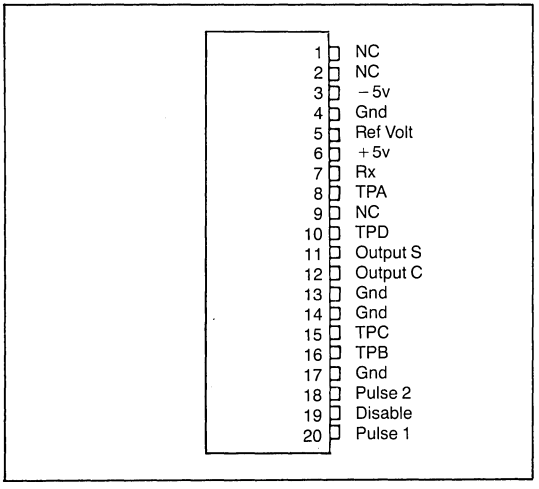


# ARCNET® High Impedance Transceiver HIT™

## FEATURES

- ☐ Compatible with existing ARCNET® installations
- ☐ Compatible with ARCNET® coax drivers
- ☐ Pin Compatible with ARCNET® fiber-optic drivers
- ☐ Enables Bus topology on ARCNET® LAN's
- ☐ Provides network expansion without any additional repeaters or major rewiring
- ☐ Multi-media drive capability
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The High Impedance Transceiver (HIT) provides ARCNET® LAN's designers with a new bus configuration option, while reducing hardware and installation costs. The HIT offers ARCNET® LAN's with the ability to provide the highest node performance/cost ratio available heretofore. The bus topology and the reduced need for HUB's (active repeaters) eliminate the excessive costs usually associated with installing a new LAN or modifying an existing one.

The HIT is compatible with SMC monolithic LAN controller chip set the COM9026 and the COM9032. However it can work with other controllers and its inherent high output impedance enables it to drive several types of media cables.

The HIT is easily incorporated into existing ARCNET® LAN's. The HIT is pin-compatible with other media drivers, like the COAX driver currently used in most ARCNET® baseband applications and the fiber optic driver manufactured by Raycom Systems.

The HIT contains all the necessary filtering to guarantee noise-immunity for interference-free data transfers at 2.5 Mbps.

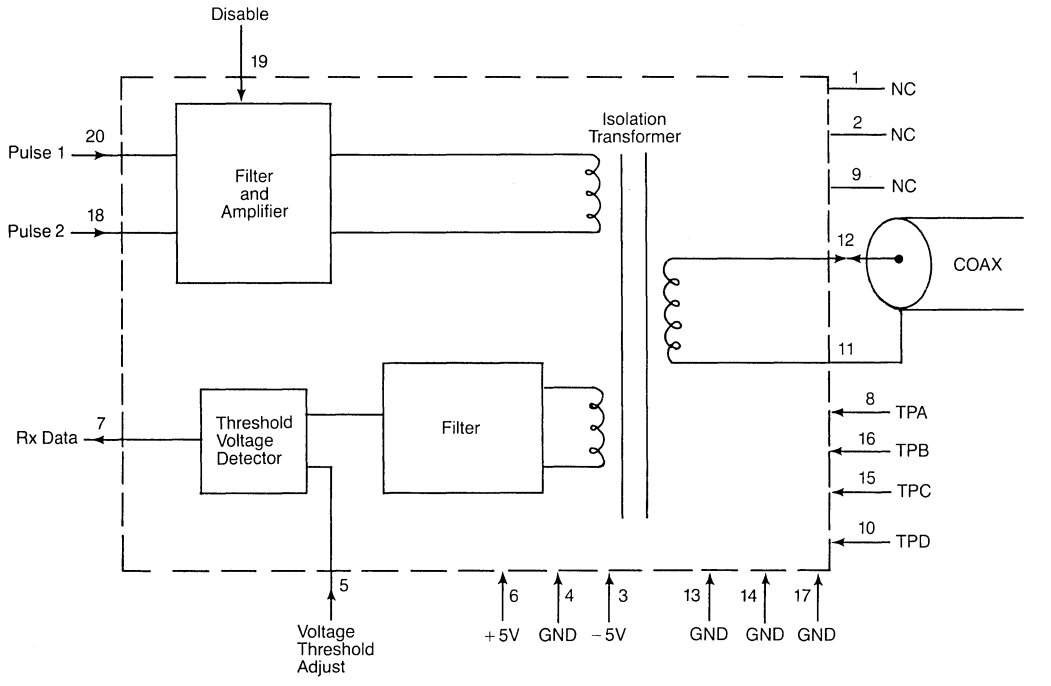



**Figure 1—HIT Block Diagram**

## DESCRIPTION OF PIN FUNCTIONS

| PIN # | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1, 2, 9 | — | NC | Not used. No connection. |
| 3 | Power Supply | VDD | −5 Volts Power Supply. |
| 4, 13, 14, 17 | Ground | GND | Ground |
| 5 | Threshold Voltage | REF V | External Reference Voltage to adjust Internal Voltage Detector Threshold. |
| 6 | Power Supply | VCC | +5 Volt Power Supply. |
| 7 | Received Data Output | RX | Received Data, goes to RXIN of COM9032 (TTL). |
| 8, 10, 15, 16 | Test Points | TPA, TPB TPD, TPC | Test Points. Make no connection to these pins. |
| 11 | COAX I/O | SHLD | Connect to Coax Cable Shield (Outer Conductor). Bypass to GND is recommended. |
| 12 | COAX I/O | CNTR | Connect to Coax Cable Inner Conductor (Center) |
| 18 | Pulse 2 | P2 | TTL Level Input to the Transmitter Section (Active Low). |
| 19 | Disable | DSBL | Normally connected to ground a high disables the transmitting. |
| 20 | Pulse 1 | P1 | TTL Level Input to the Transmitter Section (Active Low). |

## FUNCTIONAL DESCRIPTION

The HIT integrates a host of discrete components onto a hybrid microcircuit to provide the Local Area Network design with space and cost reductions as well as the enhanced reliability of a single component.

**Transmit section:**
Referring to the block diagram of figure 1, Pulse 1 and Pulse 2 signals can be TTL pulses of 100 nsec each with Pulse 2 delayed by 100 nsec. The optimum timing for these signals can be obtained from SMC's COM9032. Amplification and filtering is used to eliminate undesirable frequencies from the signals, while providing them with the necessary drive, before transmitting onto the line through an isolation transformer. The driving circuitry has been designed to present a very high impedance to the line for minimum loading. The transformer typical voltage output is 20 volts peak to peak. In most applications, it is recommended that the shield of the coaxial cable be bypassed to ground by a parallel R-C combination.

**Receive section:**
The received dipulse signal from the line is DC isolated by the transformer. It is filtered to reduce noise, voltage transients and intersymbol interference. It is then recovered by a threshold voltage detector. The minimum signal amplitude necessary for reliable operation is 6 volts peak to peak. The TTL Rx Data output is then sent to the receive input of the COM9032. A voltage threshold pin can be used to vary the threshold voltage for special situations.

In normal operation, the "disable" at pin 19 should be tied to ground. However, in certain cases, this pin can be used to prevent transmission.

## APPLICATION INFORMATION

The hit is designed to eliminate the need for Hubs in small (8 nodes) installations extending up to 1000 feet as shown in figure 2. However the number of nodes is inversely proportional to the bus length.

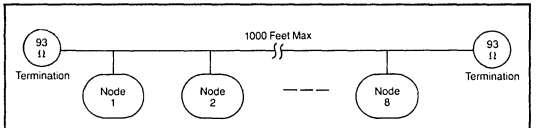



**Figure 2—Typical Small Hubless Network**

Figures 3 and 4 show alternative ARCNET® local area network implementation using the "LAND" and the HIT. As can be easily observed the straight forward approach of the HIT version results in very low per node cost as well as ease of installation.

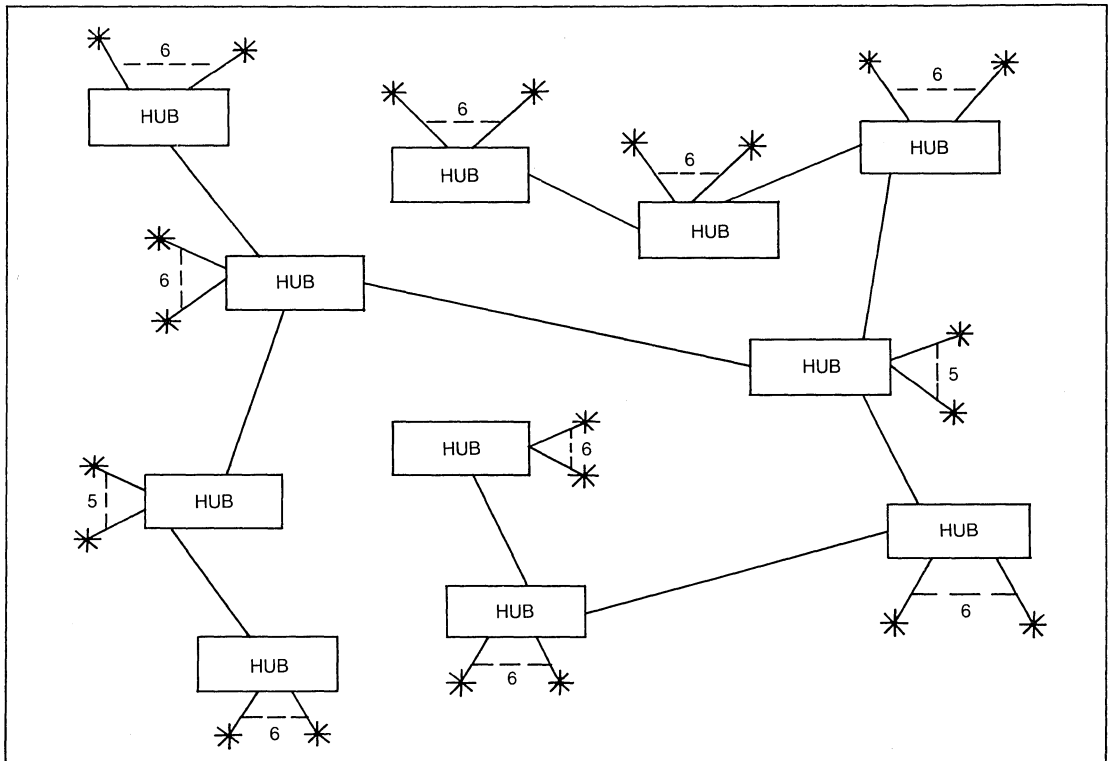



**Figure 3—Typical 64 Node Network Using HUBs and LANDs**

## ELECTRICAL CHARACTERISTICS

### MAXIMUM GUARANTEED RATINGS*:

Operating Temperature Range ..... 0 C to +70 C
Storage Temperature Range ..... −40 C to +125 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any pin with respect to Gnd ..... 8 V
Negative Voltage on any pin except Vdd with respect to Gnd ..... −0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**Electrical Characteristics** Ta = 0 to 70 C, Vcc = +5V ±5%, Vdd = −5V ±5%.

| Parameter | Min. | Typ. | Max | Unit | Comments |
|---|---|---|---|---|---|
| INPUT VOLTAGE LEVELS | | | | | |
| Pulse 1, 2, DSBL inputs | | | | | |
| Low-level, VIL | | | 0.8 | V | Iil = −.8ma |
| High-level, VIH | 2.0 | | | V | Iih = .2ma |
| Received signal amplitude | 6 | | | Vp-p | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Rx Data output | | | | | |
| Low-level, VOL | | | 0.4 | V | One TTL load |
| High-level, VOH | 2.4 | | | V | One TTL load |
| Transformer output | 16 | 20 | | Vp-p | |
| Cable noise amplitude | | | 4 | Vp-p | |
| POWER SUPPLY CURRENT | | | | | |
| Icc | | 190 | 285 | mA | |
| Idd | | 180 | 270 | mA | |
| PULSE WIDTH | | | | | |
| Pulse 1, 2 inputs | | 100 | | nsec | |

Shorting the transformer output can cause permanent damage to the device.

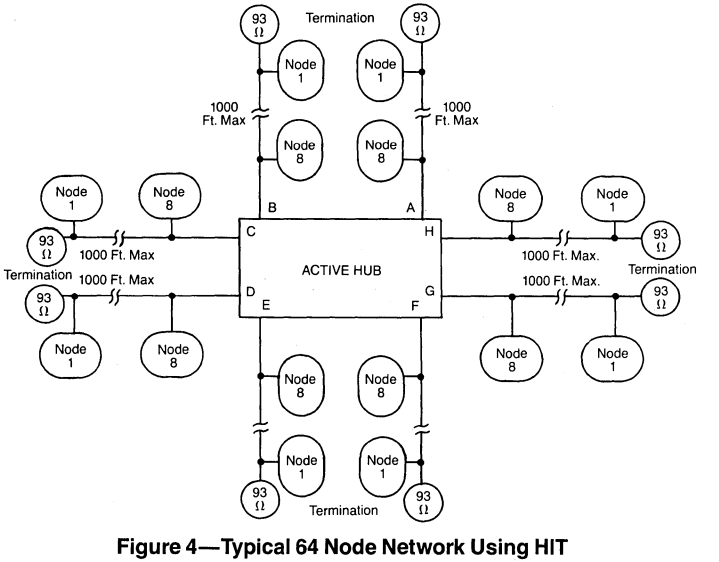



**Figure 4—Typical 64 Node Network Using HIT**

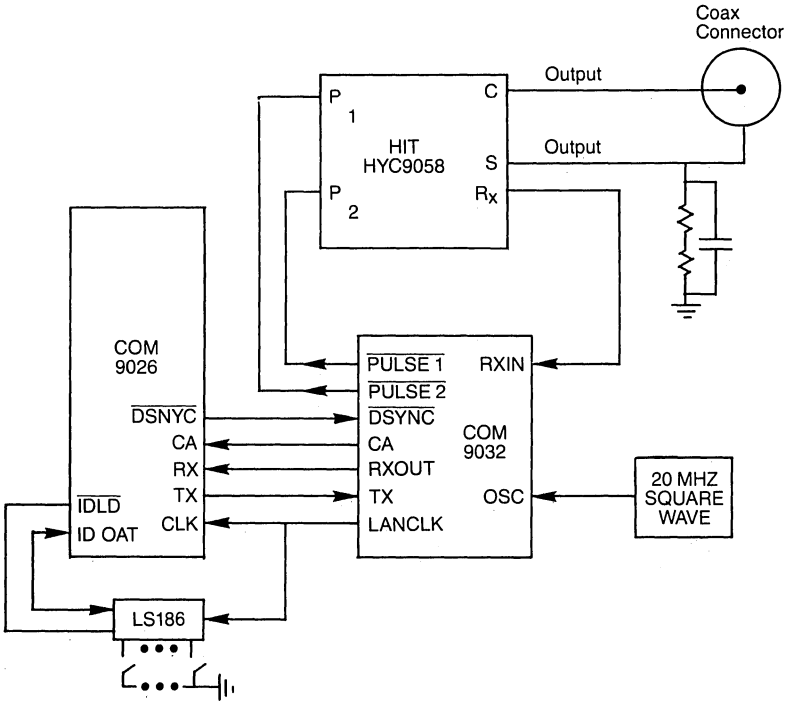
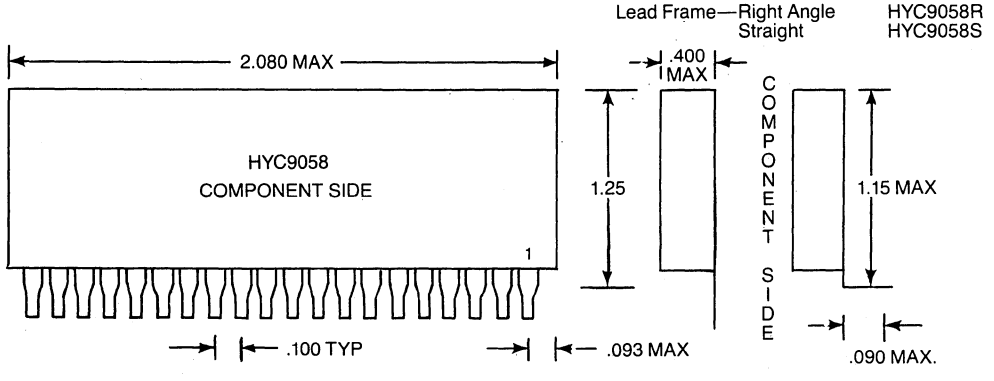



**Figure 5—Typical HYC9058 Interconnect**




**Mechanical Specification**

ARCNET® is a registered trademark of the Datapoint Corporation

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**HYC9068**
**PRELIMINARY**

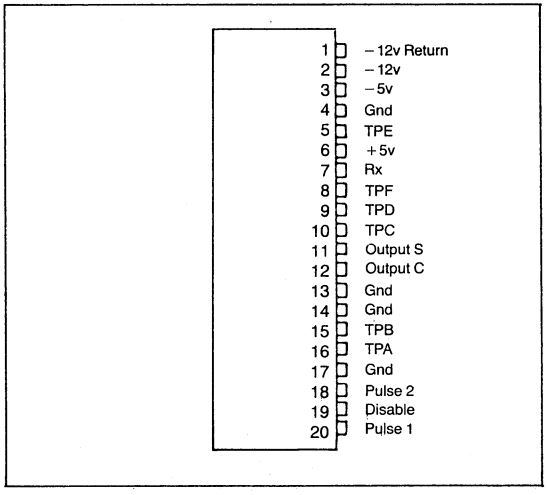


# ARCNET® Local Area Network Driver LAND™

## FEATURES

- ☐ Compatible with existing ARCNET® installations
- ☐ Compatible with ARCNET® coax drivers
- ☐ Pin Compatible with ARCNET® fiber-optic drivers
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity
- ☐ Drives up to 2,000 ft. of Coax
- ☐ Replaces more than 25 discrete components and IC's

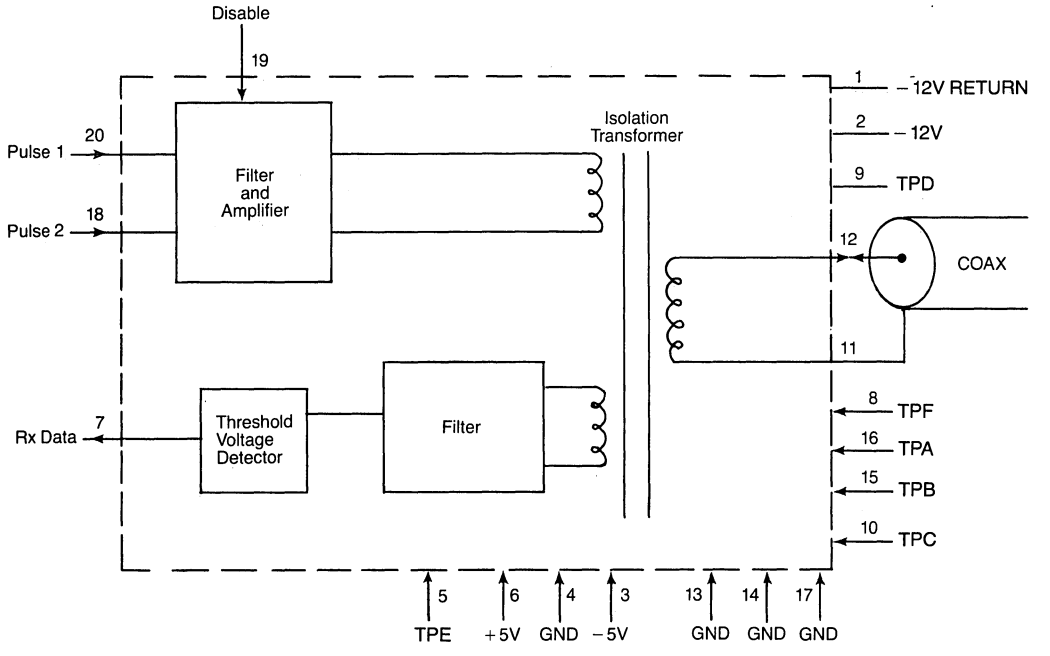
## PIN CONFIGURATION




## GENERAL DESCRIPTION

The HYC9068 is a Coax Driver for ARCNET Local Area Networks. The HYC9068 is compatible with SMC's COM9026 Local Area Network Controller (LANC) and the COM9032 Local Area Network Transceiver (LANT). The HYC9068 simplifies network implementation while providing considerable space and cost savings plus the high reliability of a single component.

The HYC9068 contains both receive and transmit filters to guarantee interference-free data transfer over 2,000 ft. of RG-62 coaxial cable at 2.5 Mbps data rate.




**HYC9068-LAND BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN # | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | -12V Return | GND | -12V Return |
| 2 | Power Supply | Vss | -12V Power Supply |
| 3 | Power Supply | VDD | -5 Volts Power Supply. |
| 4, 13, 14, 17 | Ground | GND | Ground |
| 6 | Power Supply | VCC | +5 Volt Power Supply. |
| 7 | Received Data Output | RX | Received Data, goes to RXIN of COM9032 (TTL). |
| 8, 10, 15, 16, 5, 9 | Test Points | TPA, TPB, TPE TPD, TPC, TPF | Test Points. Make no connection to these pins. |
| 11 | COAX I/O | SHLD | Connect to Coax Cable Shield (Outer Conductor). Bypass to GND is recommended. |
| 12 | COAX I/O | CNTR | Connect to Coax Cable Inner Conductor (Center). |
| 18 | Pulse 2 | P2 | TTL Level Input to the Transmitter Section (Active Low). |
| 19 | Disable | DSBL | Normally connected to ground a high disables the transmitting. |
| 20 | Pulse 1 | P1 | TTL Level Input to the Transmitter Section (Active Low). |

When using the optional −12V supply Pin 3 must not be connected. Pin 1 must be grounded and −12V must be applied to Pin 2.

The easiest way to create the optimum input is to use the SMC COM9032 to provide PULSE 1 ($P_1$) and PULSE 2 ($P_2$). The DISABLE (Pin 19) should be grounded during normal operation.

In order to inhibit surge damage as well as limit spurious radiation, it is suggested that the shield of the COAXIAL CABLE be bypassed to ground by a parallel R-C Network (0.005 μFd/1Kv in parallel with two 5.6K ohm/½W resistors in series) as shown in typical interconnect diagram.

## ELECTRICAL CHARACTERISTICS

### MAXIMUM GUARANTEED RATINGS*:

Operating Temperature Range ..... 0 C to + 70 C
Storage Temperature Range..... − 40 C to + 125 C
Lead Temperature (soldering, 10 sec.) ..... + 325 C
Positive Voltage on any pin with respect to Gnd ..... 8 V
Negative Voltage on any pin except Vdd and Vss with respect to Gnd ..... − 0.3 V

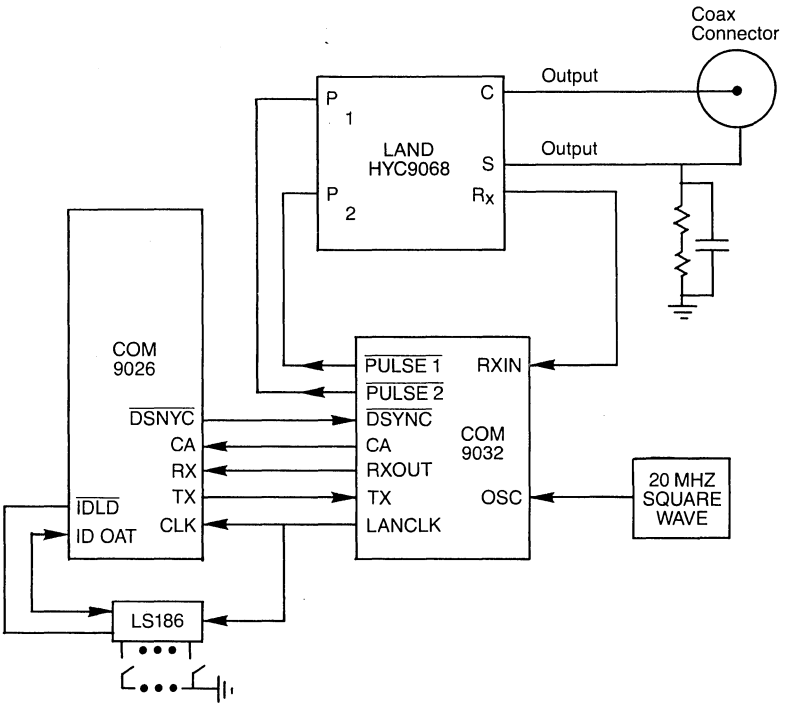
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

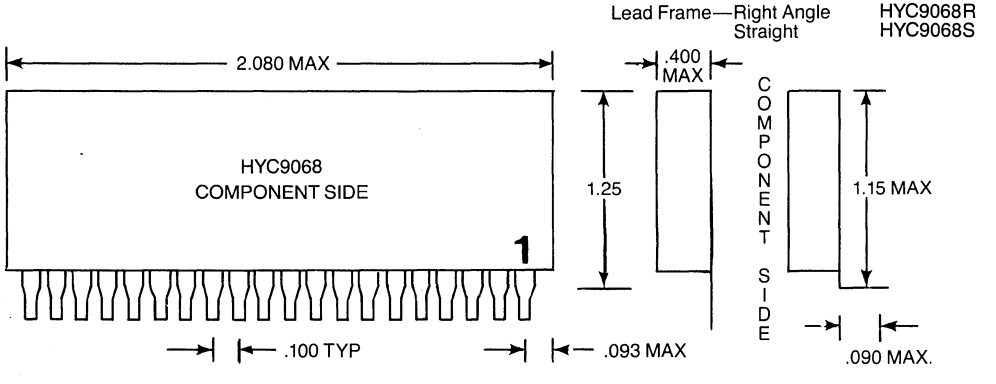
**PRELIMINARY**
Notice: This is not a final specification.
Some parametric limits are subject to change.

**Electrical Characteristics** Ta = 0 to 70 C, Vcc = + 5V ± 5%, Vdd = −5V ± 5%, or Vss = −12V ± 5%

| Parameter | Min. | Typ. | Max | Unit | Comments |
|---|---|---|---|---|---|
| INPUT VOLTAGE LEVELS | | | | | |
| Pulse 1, 2, DSBL inputs | | | | | |
| Low-level, VIL | | | 0.8 | V | Iil = −.8ma |
| High-level, VIH | 2.0 | | | V | Iih = .2ma |
| Received signal amplitude | 6 | | | Vp-p | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Rx Data output | | | | | |
| Low-level, VOL | | | 0.4 | V | One TTL load |
| High-Level, VOH | 2.4 | | | V | One TTL load |
| Transformer output | 15.4 | 20 | | Vp-p | |
| Cable noise amplitude | | | 4 | Vp-p | |
| POWER SUPPLY CURRENT | | | | | |
| Icc | | | 250 | mA | |
| Idd | | | 20 | mA | |
| Iss | | | 50 | mA | |
| PULSE WIDTH | | | | | |
| Pulse 1, 2 inputs | | 100 | | nsec | |
| COAXIAL CABLE | | | | | |
| Type RG-62 (93Ω) | | | 2,000 | ft | |




**TYPICAL HYC9068 INTERCONNECT**




**MECHANICAL SPECIFICATION**

ARCNET® is a registered trademark of the Datapoint Corporation

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

**HYC9078**
**PRELIMINARY**

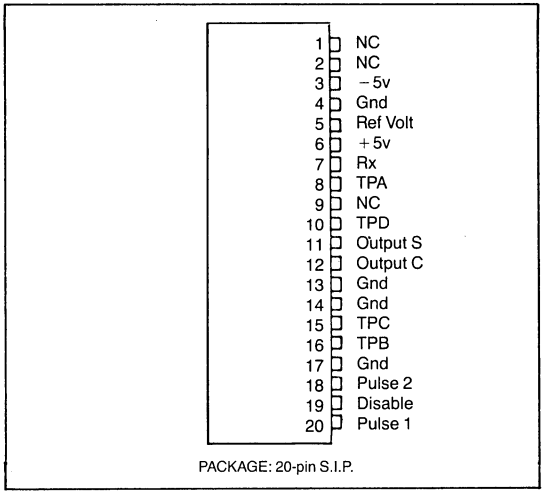


# High Impedance Transceiver HIT™ 2

## FEATURES

- ☐ Compatible with SMC's COM9056 Enhanced Local Area Network Controller (ELANC)
- ☐ 5 MHz operation
- ☐ High impedance
- ☐ Enables Bus topology on LAN's
- ☐ Provides network expansion without any additional repeaters or major rewiring
- ☐ Multi-media drive capability
- ☐ Space saving economy
- ☐ 20 pin single in line package (SIP)
- ☐ Straight or right angle lead frame
- ☐ Built in filters for noise immunity
- ☐ Common mode isolation
- ☐ Wide dynamic range
- ☐ Very low level receiver sensitivity

## PIN CONFIGURATION




PACKAGE: 20-pin S.I.P.

## GENERAL DESCRIPTION

The HIT2 is a new media interface hybrid which works with the ELANC in the new high speed 5Mbps mode of signalling. The HIT2 will be available in a 20pin SIP hybrid package.

The HIT2 has been tuned to operate with the ELANC's high speed mode and includes a specially designed receive circuit to receive data in the manchester signalling scheme without introducing a significant amount of bit jitter. The HIT2 also includes a transmit signal amplifier and high frequency filter so that it generates clean signals that are free from high order harmonics that might cause EMI problems. Both the transmit section and receive circuit are transformer coupled to the output and have both been designed with very high input impedances which allow the HIT2 to be used in bus topologies. Additionally, the large dynamic range of the HIT2 provides very relaxed cabling restrictions.

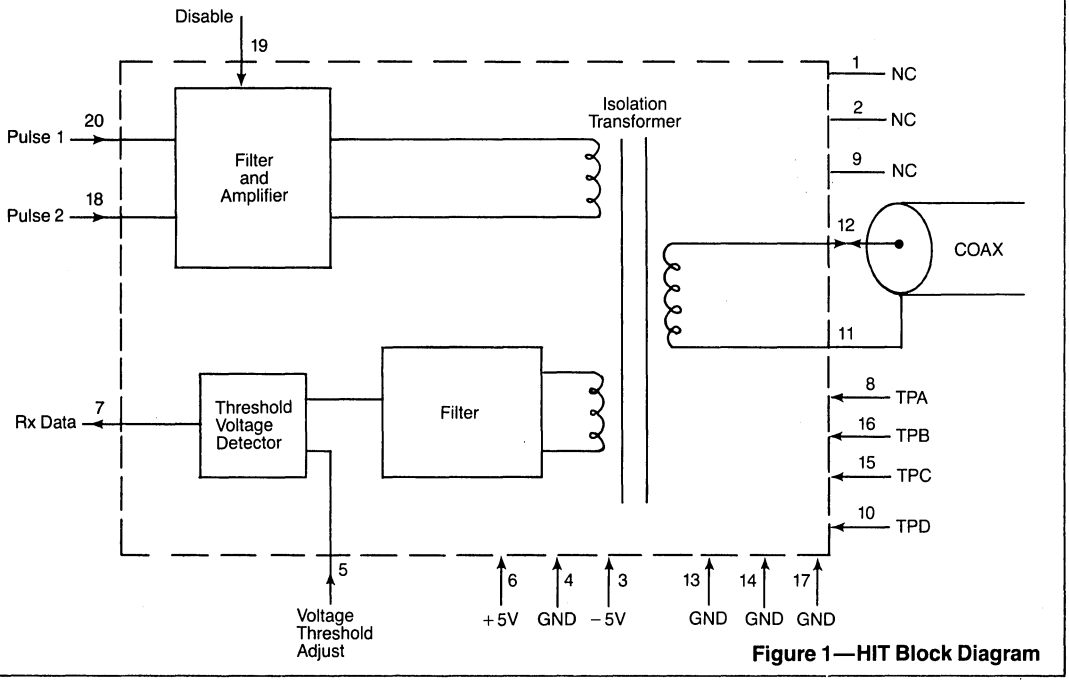
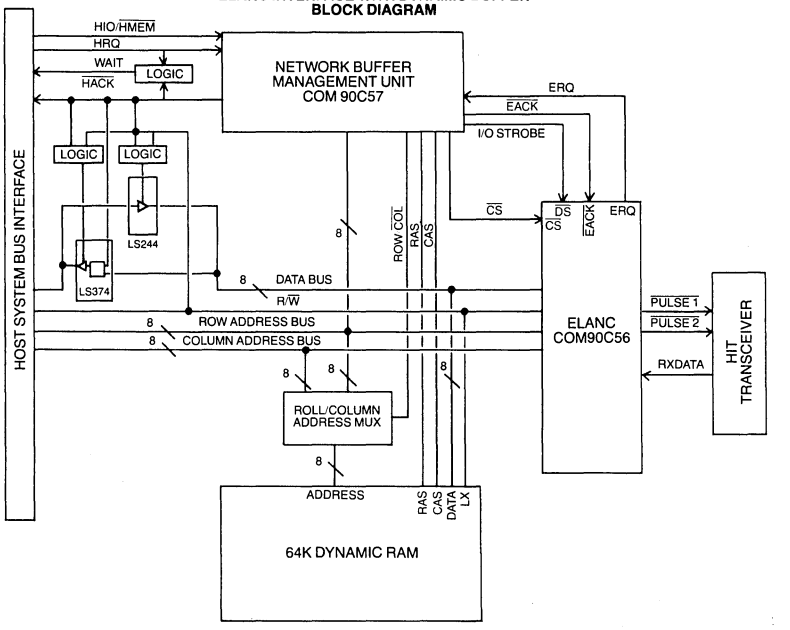


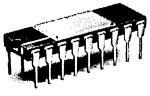

**Figure 1—HIT Block Diagram**

**FIGURE 2:**
**ELANC INTERFACE WITH DYNAMIC BUFFER**
**BLOCK DIAGRAM**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.



# Baud Rate Generator



| Part Number | Description | Features | Power Supplies | Package | Page |
|---|---|---|---|---|---|
| COM 5016 | Dual Baud Rate Generator | On-chip oscillator or external frequency input (use 8116 for new designs) | +5, +12 | 18 DIP | 265-266 |
| COM 5016T[1] | Dual Baud Rate Generator | External frequency input | +5, +12 | 18 DIP | 265-266 |
| COM 5026 | Single Baud Rate Generator | On-chip oscillator or external frequency input (use 8126 for new designs) | +5, +12 | 14 DIP | 267-272 |
| COM 5026T[1] | Single Baud Rate Generator | External frequency input | +5, +12 | 14 DIP | 267-272 |
| COM 5036 | Dual Baud Rate Generator | COM 5016 with additional output of input frequency ÷ 4 (use 8136 or 81C36 for new designs) | +5, +12 | 18 DIP | 265-266 |
| COM 5036T[1] | Dual Baud Rate Generator | COM 5016T with additional output of input frequency ÷ 4 | +5, +12 | 18 DIP | 265-266 |
| COM 5046 | Single Baud Rate Generator | COM 5026 with additional output of input frequency ÷ 4 (use 8146 for new designs) | +5, +12 | 14 DIP | 267-272 |
| COM 5046T[1] | Single Baud Rate Generator | COM 5026T with additional output of input frequency ÷ 4 | +5, +12 | 14 DIP | 267-272 |
| COM 8046 | Single Baud Rate Generator | 32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply | +5 | 16 DIP | 273-274 |
| COM 8046T[1] | Single Baud Rate Generator | COM 8046 with external frequency input only | +5 | 16 DIP | 273-274 |
| COM 8116 | Dual Baud Rate Generator | Single +5 volt version of COM 5016 | +5 | 18 DIP | 275-276 |
| COM 8116T[1] | Dual Baud Rate Generator | Single +5 volt version of COM 5016T | +5 | 18 DIP | 275-276 |
| COM 8126 | Single Baud Rate Generator | Single +5 volt version of COM 5026 | +5 | 14 DIP | 277-284 |
| COM 8126T[1] | Single Baud Rate Generator | Single +5 volt version of COM 5026T | +5 | 14 DIP | 277-284 |
| COM 8136 | Dual Baud Rate Generator | Single +5 volt version of COM 5036 | +5 | 18 DIP | 275-276 |
| COM 8136T[1] | Dual Baud Rate Generator | Single +5 volt version of COM 5036T | +5 | 18 DIP | 275-276 |
| COM 8146 | Single Baud Rate Generator | Single +5 volt version of COM 5046 | +5 | 14 DIP | 277-284 |
| COM 8146T[1] | Single Baud Rate Generator | Single +5 volt version of COM 5046T | +5 | 14 DIP | 277-284 |
| COM 8156 | Dual Baud Rate Generator | High-frequency clock input version of COM 8116 with additional outputs of input frequency ÷ 2 and ÷ 8 | +5 | 18 DIP | 285-288 |
| COM 8156T[1] | Dual Baud Rate Generator | External clock input version of COM 8156 | +5 | 18 DIP | 285-288 |
| COM 81C66[2] | Timer/Clock Generator | CMOS User Programmable Clock and Timer | +5 | 16 DIP | 289-290 |
| COM 81C66T[2] | Timer/Clock Generator | External Frequency Input version of COM 8166T | +5 | 16 DIP | 289-290 |

[1]May be custom mask programmed [2]For future release

STANDARD MICROSYSTEMS CORPORATION

# COM 5016
# COM 5016T
# COM 5036
# COM 5036T

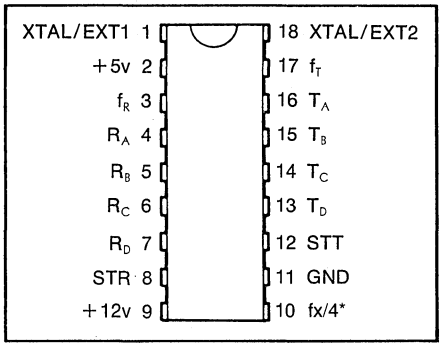
# Dual Baud Rate Generator
## Programmable Divider



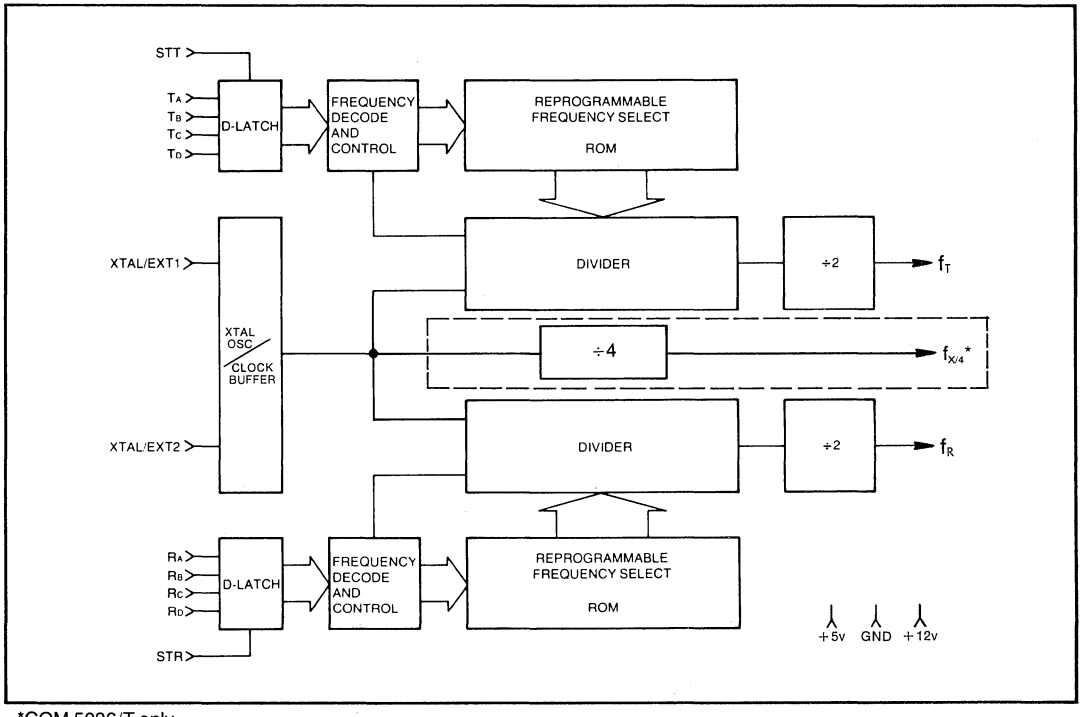
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ DIRECT UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output*
- ☐ TTL, MOS compatibility

### PIN CONFIGURATION




### BLOCK DIAGRAM




*COM 5036/T only

## General Description

The Standard Microsystems COM 5016/COM 5036 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016/COM 5036 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016/COM 5036 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016/COM 5036 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016/COM 5036's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016/COM 5036 can be driven by either an external crystal or TTL logic level inputs; COM 5016T/COM 5036T is driven by TTL logic level inputs only.

The COM 5036 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

## Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | XTAL/EXT1 | Crystal or External Input 1 | This input is either one pin of the crystal package or one polarity of the external input. |
| 2 | $V_{CC}$ | Power Supply | +5 volt supply |
| 3 | $f_R$ | Receiver Output Frequency | This output runs at a frequency selected by the Receiver divisor select data bits. |
| 4-7 | $R_A$, $R_B$, $R_C$, $R_D$ | Receiver-Divisor Select Data Bits | The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, $f_R$. |
| 8 | STR | Strobe-Receiver | A high level input strobe loads the receiver data ($R_A$, $R_B$, $R_C$, $R_D$) into the receiver divisor select register. This input may be strobed or hard-wired to a high level. |
| 9 | $V_{DD}$ | Power Supply | +12 volt supply |
| 10 | $f_X/4$* | $f_X/4$ | ¼ crystal/clock frequency reference output. |
| 11 | GND | Ground | Ground |
| 12 | STT | Strobe-Transmitter | A high level input strobe loads the transmitter data ($T_A$, $T_B$, $T_C$, $T_D$) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level. |
| 13-16 | $T_D$, $T_C$, $T_B$, $T_A$ | Transmitter-Divider Select Data Bits | The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, $f_T$. |
| 17 | $f_T$ | Transmitter Output Frequency | This output runs at a frequency selected by the Transmitter divisor select data bits. |
| 18 | XTAL/EXT2 | Crystal or External Input 2 | This input is either the other pin of the crystal package or the other polarity of the external input. |

*COM 5036/T only

For electrical characteristics, see page 221.

STANDARD MICROSYSTEMS CORPORATION

# COM 5026
# COM 5026T
# COM 5046
# COM 5046T

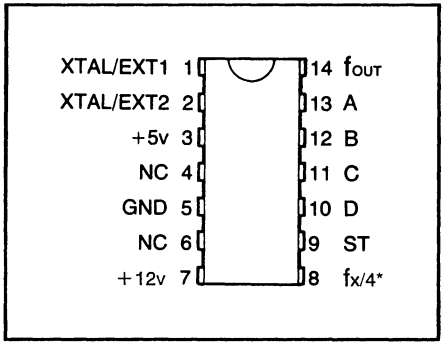
# Baud Rate Generator
## Programmable Divider



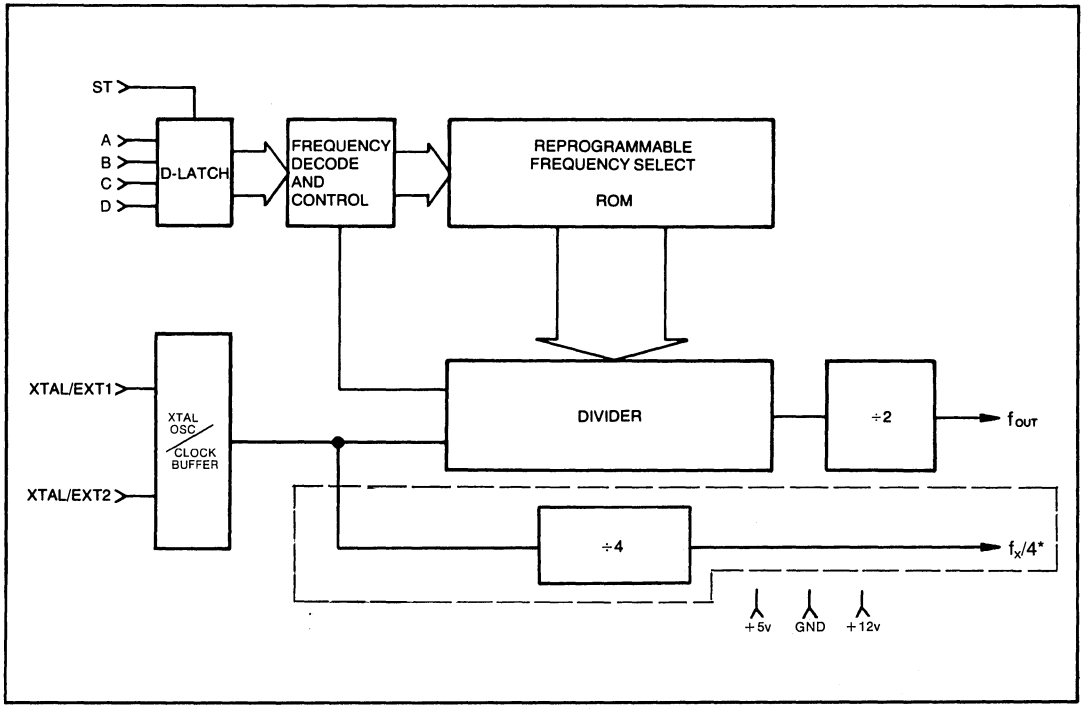
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output*
- ☐ TTL, MOS compatibility

### PIN CONFIGURATION




### BLOCK DIAGRAM




*COM 5046/T only

## GENERAL DESCRIPTION

The Standard Microsystems COM 5026/COM 5046 Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 16 externally selectable frequencies.

The COM 5026/COM 5046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs; as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs may be strobe (150ns) or DC loaded.

The COM 5026/COM 5046 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using the frequency output, it is possible to generate additional divisions of the master clock frequency by cascading COM 5026/COM 5046's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5026/COM 5046 can be driven by either an external crystal or TTL logic level inputs COM 5026T/COM 5046T is driven by TTL logic level inputs only.

THE COM 5046 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

### Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | XTAL/EXT1 | Crystal or External Input 1 | This input is either one pin of the crystal package or one polarity of the external input. |
| 2 | XTAL/EXT2 | Crystal or External Input 2 | This input is either the other pin of the crystal package or the other polarity of the external input. |
| 3 | $V_{CC}$ | Power Supply | +5 volt Supply. |
| 4,6 | NC | No Connection | |
| 5 | GND | Ground | Ground |
| 7 | $V_{DD}$ | Power Supply | +12 volt Supply. |
| 8 | fx/4* | Reference Frequency | High frequency reference output @ (1/4) $f_{IN}$ |
| 9 | ST | Strobe | A high-level strobe loads the Input Address ($A_A$, $A_B$, $A_C$, $A_D$) into the Input Address register. This input may be strobed or hard wired to a high-level, |
| 10-13 | $A_D$, $A_C$, $A_B$, $A_A$ | Input Address | The logic level on these inputs. as shown in Table 1, selects the output frequency. |
| 14 | $f_{OUT}$ | Output Frequency | This output runs at a frequency as selected by the Input Address. |

*COM 5046/T only

## ELECTRICAL CHARACTERISTICS COM5016, COM5016T, COM5026, COM5026T, COM5036, COM5036T, COM5046, COM5046T

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

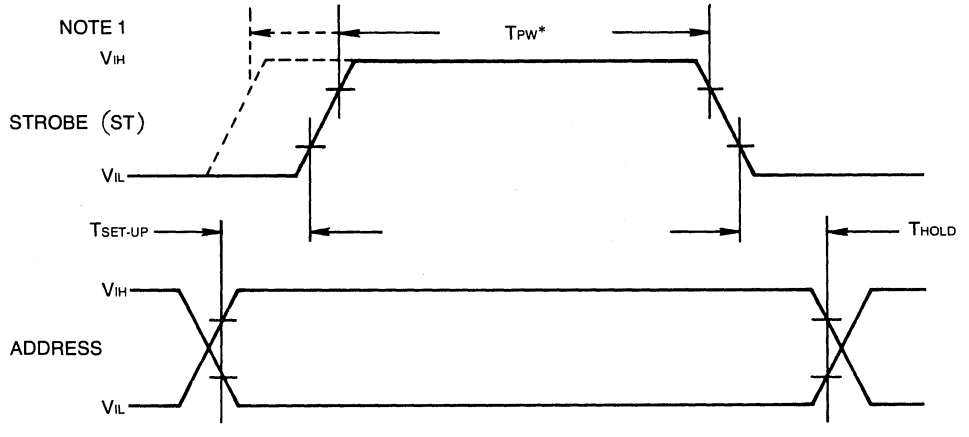
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, $V_{DD}$=+12V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | excluding XTAL inputs |
| High-level, $V_{IH}$ | 2.0 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6ma |
| | | | 0.5 | V | $I_{OL}$ = 3.2ma |
| High-level, $V_{OH}$ | $V_{CC}$−1.5 | 4.0 | | V | $I_{OH}$ = 100μA |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | 0.3 | mA | $V_{IN}$ = GND, excluding XTAL inputs |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pf | $V_{IN}$ = GND, excluding XTAL inputs |
| EXT INPUT LOAD | | 8 | 10 | | Series 7400 unit loads |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 28 | 45 | mA | |
| $I_{DD}$ | | 12 | 22 | mA | |
| **A.C. CHARACTERISTICS** | | | | | $T_A$ = +25°C |
| CLOCK FREQUENCY | | 5.0688 | | MHz | XTAL, EXT |
| PULSE WIDTH | | | | | |
| Clock | | | | | 50% Duty Cycle ±5% |
| Strobe | 150 | | DC | ns | See Note 1. |
| INPUT SET-UP TIME | | | | | |
| Address | 50 | | | ns | See Note 1. |
| INPUT HOLD TIME | | | | | |
| Address | 50 | | | ns | |
| STROBE TO NEW FREQUENCY DELAY | | | 3.5 | μs | $=1/f_{IN}$ (18) |

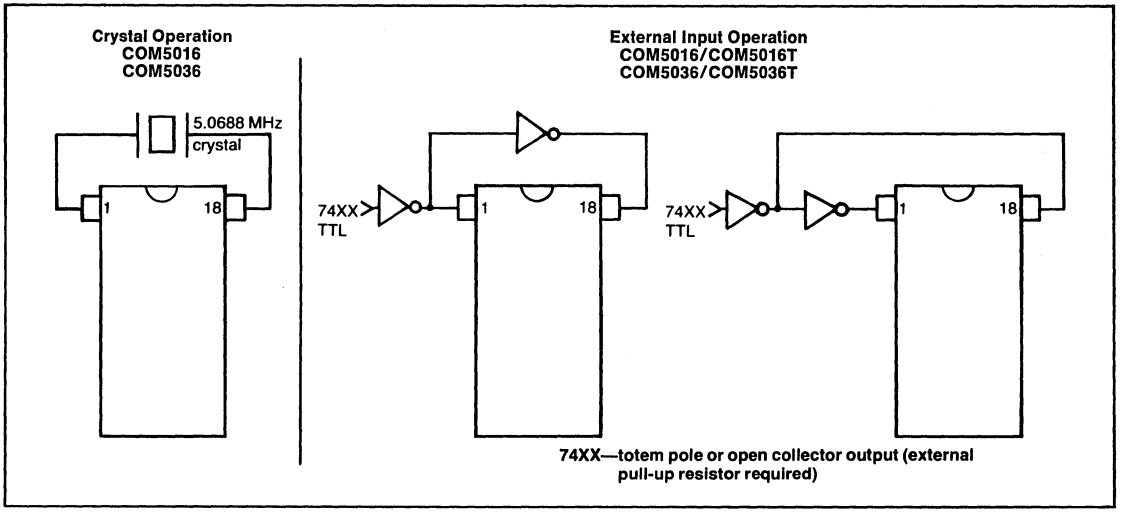
Note 1: Input set-up time can be decreased to ⩾ 0ns by increasing the minimum strobe width by 50ns to a total of 200ns.

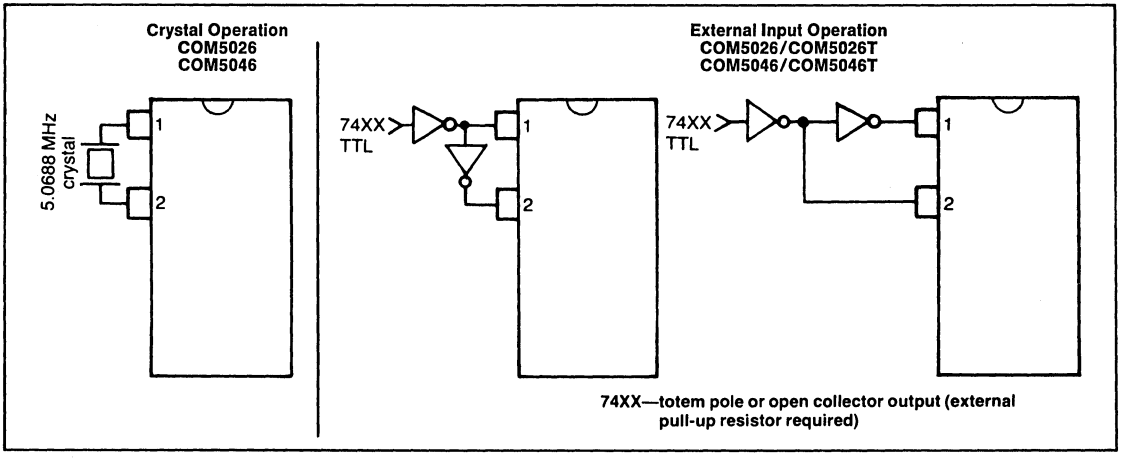
**TIMING DIAGRAM**




*Address need only be valid during the last $T_{PW}$, Min time of the input strobe.

SECTION IV




For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

## Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency — 5.0688 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance $<50\ \Omega$
Series Resonant
Overall tolerance $\pm$ .01%
or as required

## Crystal manufacturers (Partial List)

**Northern Engineering Laboratories**
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

**Bulova Frequency Control Products**
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

**CTS Knights Inc.**
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

**Crystek Crystals Corporation**
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

## APPLICATIONS INFORMATION

Charge pump techniques using the +5 volt power supply can be used to generate the +12 volt power supply required. The +12 volt power supply of figure 1 will supply the 22 milli-amps that is typically required.

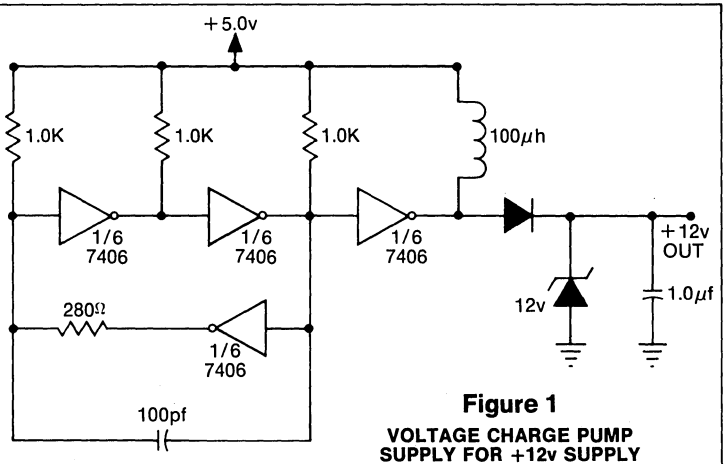



**Figure 1**
**VOLTAGE CHARGE PUMP SUPPLY FOR +12v SUPPLY**

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that the clamp circuit of figure 2 or a Semtech* bi-polarity silicon transient suppressor such as the 1N6110 be used.

*SEMTECH CORPORATION
652 Mitchel Road
Newbury Park, California 91320
213-628-5392

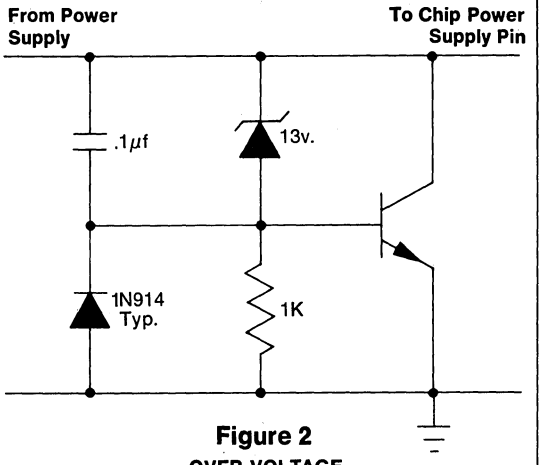



**Figure 2**
**OVER-VOLTAGE PROTECTION CIRCUIT**

# Baud Rate Generator Output Frequency Options

**Table 1.** (16X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6336 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4224 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.76 | — | 50/50 | 2880 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.1523 | 0.016 | 50/50 | 2355 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2112 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1056 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 528 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 264 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.8 | — | 50/50 | 176 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 32.081 | 0.253 | 50/50 | 158 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 132 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.6 | — | 50/50 | 88 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 66 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 115.2 | — | 50/50 | 44 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 48/52 | 33 |
| 1 | 1 | 1 | 1 | 19.200 | 307.2 | 316.8 | 3.125 | 50/50 | 16 |

**Table 2.** (16X clock)

CRYSTAL FREQUENCY = 4.9152 MHz

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6144 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4096 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.7589 | −0.01 | * | 2793 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.152 | — | 50/50 | 2284 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2048 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1024 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 512 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 256 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.7438 | −0.19 | * | 171 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 31.9168 | −0.26 | 50/50 | 154 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 128 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.8258 | 0.39 | * | 85 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 64 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 114.306 | −0.77 | * | 43 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 50/50 | 32 |
| 1 | 1 | 1 | 1 | 19,200 | 307.2 | 307.2 | — | 50/50 | 16 |

**Table 3.** (32X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 32X Clock | Actual Frequency 32X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 1.6 KHz | 1.6 KHz | — | 50/50 | 3168 |
| 0 | 0 | 0 | 1 | 75 | 2.4 | 2.4 | — | 50/50 | 2112 |
| 0 | 0 | 1 | 0 | 110 | 3.52 | 3.52 | — | 50/50 | 1440 |
| 0 | 0 | 1 | 1 | 134.5 | 4.304 | 4.306 | .06 | * | 1177 |
| 0 | 1 | 0 | 0 | 150 | 4.8 | 4.8 | — | 50/50 | 1056 |
| 0 | 1 | 0 | 1 | 200 | 6.4 | 6.4 | — | 50/50 | 792 |
| 0 | 1 | 1 | 0 | 300 | 9.6 | 9.6 | — | 50/50 | 528 |
| 0 | 1 | 1 | 1 | 600 | 19.2 | 19.2 | — | 50/50 | 264 |
| 1 | 0 | 0 | 0 | 1200 | 38.4 | 38.4 | — | 50/50 | 132 |
| 1 | 0 | 0 | 1 | 1800 | 57.6 | 57.6 | — | 50/50 | 88 |
| 1 | 0 | 1 | 0 | 2400 | 76.8 | 76.8 | — | 50/50 | 66 |
| 1 | 0 | 1 | 1 | 3600 | 115.2 | 115.2 | — | 50/50 | 44 |
| 1 | 1 | 0 | 0 | 4800 | 153.6 | 153.6 | — | * | 33 |
| 1 | 1 | 0 | 1 | 7200 | 230.4 | 230.4 | — | 50/50 | 22 |
| 1 | 1 | 1 | 0 | 9600 | 307.2 | 316.8 | 3.125 | 50/50 | 16 |
| 1 | 1 | 1 | 1 | 19,200 | 614.4 | 633.6 | 3.125 | 50/50 | 8 |

**OUTPUT FREQUENCY OPTIONS**

| Part No. | Dash Number | | |
|---|---|---|---|
| | Table 1 | Table 2 | Table 3 |
| 5016/5016T | STD | −5 | −6 |
| 5026/5026T | STD | −5 | −6 |
| 5036/5036T | STD | N/A | N/A |
| 5046/5046T | STD | N/A | N/A |

*When Duty Cycle is not exactly 50%, it is 50% ± 10%.

STANDARD MICROSYSTEMS CORPORATION

# COM 8046
# COM 8046T

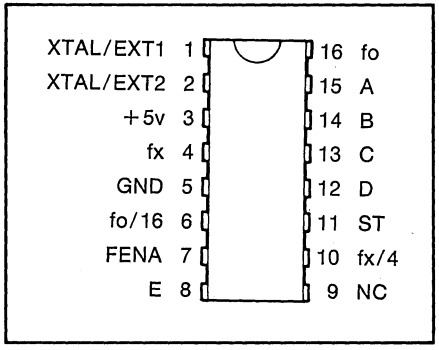
# Baud Rate Generator
## Programmable Divider



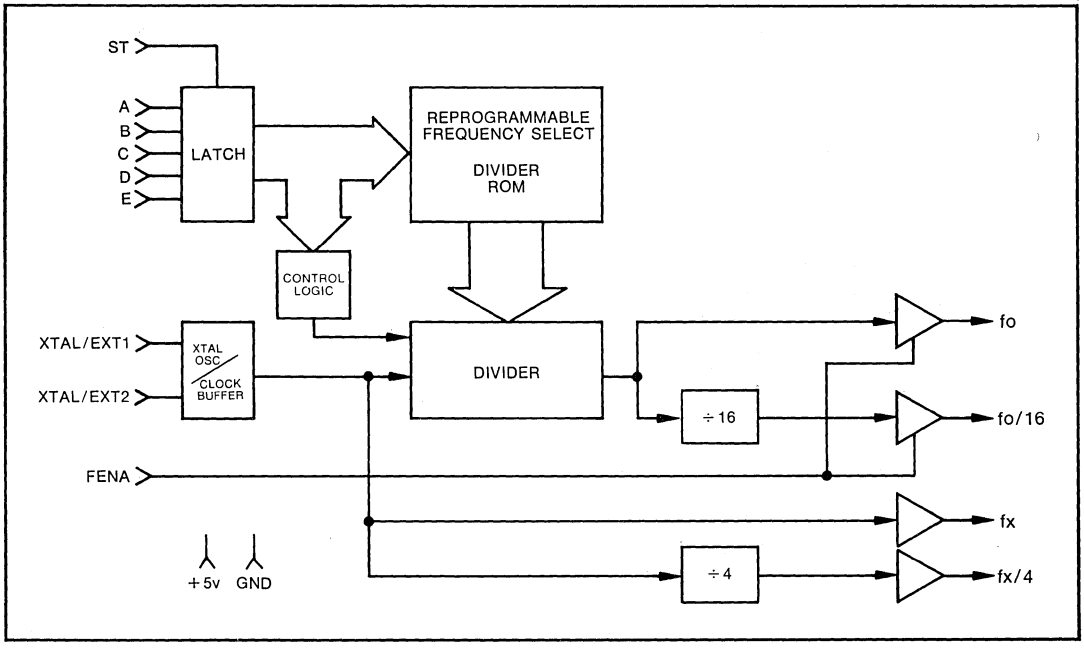
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 32 output frequencies
- ☐ 32 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatible
- ☐ 1X Clock via fo/16 output
- ☐ Crystal frequency output via fx and fx/4 outputs
- ☐ Output disable via FENA

### PIN CONFIGURATION




### BLOCK DIAGRAM



## General Description

The Standard Microsystems COM 8046 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 1X, 16X and 32X UART/USRT/ASTRO/USYNRT devices.

The COM 8046 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8046T. TTL outputs used to drive the COM 8046 or COM 8046T should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The reference frequency (fx) is used to provide two high frequency outputs: one at fx and the other at fx/4. The fx/4 output will drive one standard 7400 load, while the fx output will drive two 74LS loads.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency $f_O$. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period. The output of the divider is also divided internally by 16 and made available at the $f_O/16$ output pin. The $f_O/16$ output will drive one and the $f_O$ output will drive two standard 7400 TTL loads. Both the $f_O$ and $f_O/16$ outputs can be disabled by supplying a low logic level to the FENA input pin. Note that the FENA input has an internal pull-up which will cause the pin to rise to approximately $V_{CC}$ if left unconnected.

The divisor ROM contains 32 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around-time for ROM patterns.

The five divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the five divisor select bits; strobe activity is not required. This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current $f_O$ half-cycle All five data inputs have pull-ups identical to that of the FENA input, while the strobe input has no pull-up.

## Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | XTAL/EXT1 | Crystal or External Input 1 | This input is either one pin of the crystal package or one polarity of the external input. |
| 2 | XTAL/EXT2 | Crystal or External Input 2 | This input is either the other pin of the crystal package or the other polarity of the external input. |
| 3 | $V_{CC}$ | Power Supply | +5 volt supply |
| 4 | $f_X$ | $f_X$ | Crystal/clock frequency reference output |
| 5 | GND | Ground | Ground |
| 6 | $f_O/16$ | $f_O/16$ | 1X clock output |
| 7 | FENA | Enable | A low level at this input causes the $f_O$ and $f_O/16$ outputs to be held high. An open or a high level at the FENA input enables the $f_O$ and $f_O/16$ outputs. |
| 8 | E | E | Most significant divisor select data bit. An open at this input is equivalent to a logic high. |
| 9 | NC | NC | No connection |
| 10 | $f_X/4$ | $f_X/4$ | ¼ crystal/clock frequency reference output. |
| 11 | ST | Strobe | Divisor select data strobe. Data is sampled when this input is high, preserved when this input is low. |
| 12-15 | D,C,B,A | D,C,B,A | Divisor select data bits. A=LSB. An open circuit at these inputs is equivalent to a logic high. |
| 16 | $f_O$ | $f_O$ | 16X clock output |

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

# COM 8116
# COM 8116T
# COM 8136
# COM 8136T

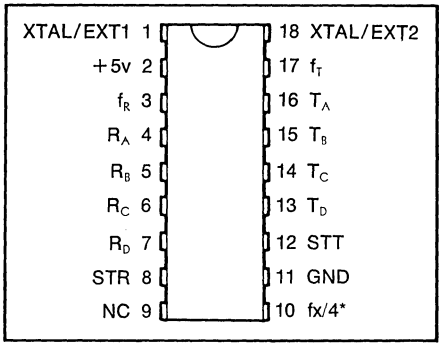
# Dual Baud Rate Generator
## Programmable Divider



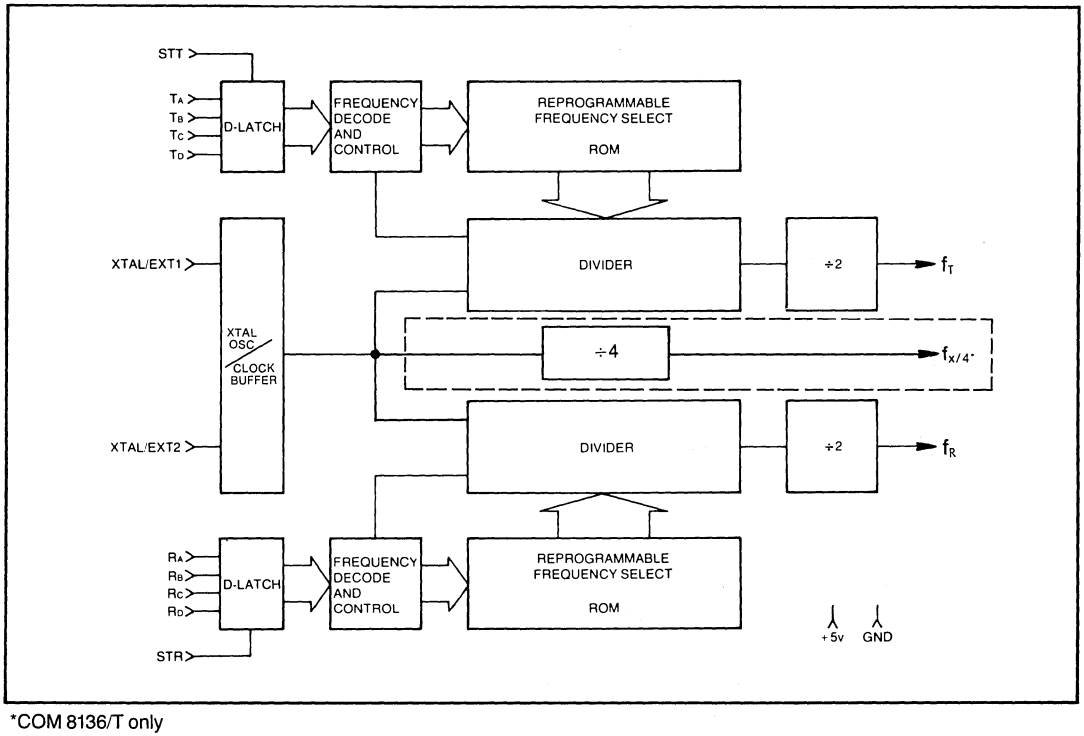
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output*
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016/COM 5036

### PIN CONFIGURATION




### BLOCK DIAGRAM




*COM 8136/T only

## General Description

The Standard Microsystem's COM 8116/COM 8136 is an enhanced version of the COM 5016/COM 5036 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116/COM 8136 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116/COM 8136 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T/COM 8136T. TTL outputs used to drive the COM 8116/COM 8136 or COM 8116T/COM 8136T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies $f_T$, $f_R$. The dividers are capable of dividing by any integer from 6 to $2^{19}$ + 1, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4 on the COM 8136/T.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

## Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | XTAL/EXT1 | Crystal or External Input 1 | This input is either one pin of the crystal package or one polarity of the external input. |
| 2 | $V_{CC}$ | Power Supply | +5 volt supply |
| 3 | $f_R$ | Receiver Output Frequency | This output runs at a frequency selected by the Receiver divisor select data bits. |
| 4-7 | $R_A$, $R_B$, $R_C$, $R_D$ | Receiver-Divisor Select Data Bits | The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, $f_R$. |
| 8 | STR | Strobe-Receiver | A high level input strobe loads the receiver data ($R_A$, $R_B$, $R_C$, $R_D$) into the receiver divisor select register. This input may be strobed or hard-wired to a high level. |
| 9 | NC | No Connection | |
| 10 | $f_X/4$* | $f_X/4$ | ¼ crystal/clock frequency reference output. |
| 11 | GND | Ground | Ground |
| 12 | STT | Strobe-Transmitter | A high level input strobe loads the transmitter data ($T_A$, $T_B$, $T_C$, $T_D$) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level. |
| 13-16 | $T_D$, $T_C$, $T_B$, $T_A$ | Transmitter-Divider Select Data Bits | The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, $f_T$. |
| 17 | $f_T$ | Transmitter Output Frequency | This output runs at a frequency selected by the Transmitter divisor select data bits. |
| 18 | XTAL/EXT2 | Crystal or External Input 2 | This input is either the other pin of the crystal package or the other polarity of the external input. |

*COM 8136/T only

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

# COM 8126
# COM 8126T
# COM 8146
# COM 8146T

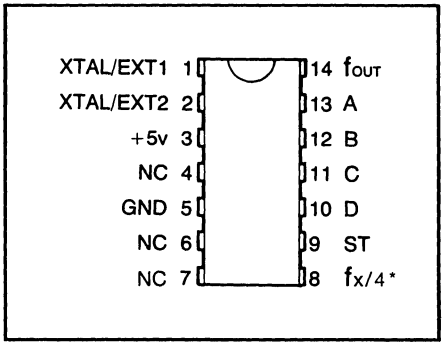
# Baud Rate Generator
## Programmable Divider



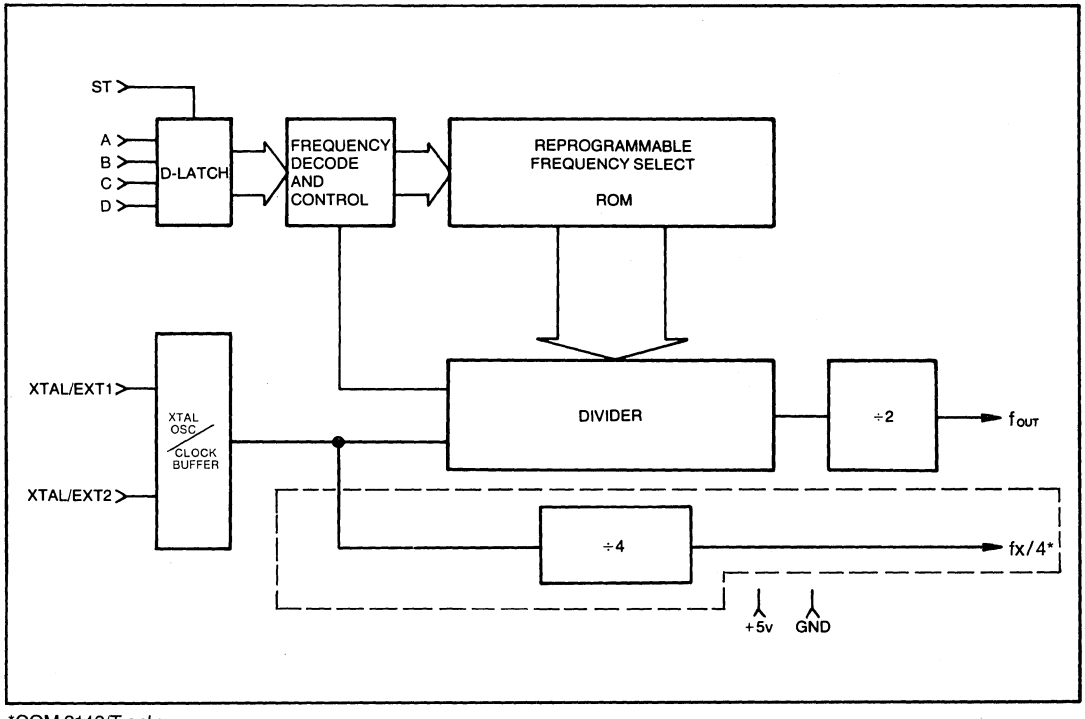
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output*
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5026/COM 5046

### PIN CONFIGURATION




### BLOCK DIAGRAM




*COM 8146/T only

## General Description

The Standard Microsystem's COM 8126/COM 8146 is an enhanced version of the COM 5026/COM 5046 Baud Rate Generator. It is fabricated using SMC's patended COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8126/COM 8146 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8126/COM 8146 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8126T/COM 8146T. TTL outputs used to drive the COM 8126/COM 8146 or COM 8126T/COM 8146T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4 on the COM 8146/T.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turnaround time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is affected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current $f_{OUT}$ half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

## Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | XTAL/EXT1 | Crystal or External Input 1 | This input is either one pin of the crystal package or one polarity of the external input, |
| 2 | XTAL/EXT2 | Crystal or External Input 2 | This input is either the other pin of the crystal package or the other polarity of the external input. |
| 3 | $V_{CC}$ | Power Supply | +5 volt supply |
| 4,6,7 | NC | No Connection | |
| 5 | GND | Ground | Ground |
| 8 | $f_X/4$ * | $f_X/4$ | ¼ crystal/clock frequency reference output. |
| 9 | ST | Strobe | A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level. |
| 10-13 | D,C,B,A | Divisor Select Data Bits | The logic level on these inputs as shown in Table 1, selects the output frequency. |
| 14 | $f_{OUT}$ | Output Frequency | This output runs at a frequency selected by the divisor select data bits. |

*COM 8146/T only

# ELECTRICAL CHARACTERISTICS COM8046, COM8046T, COM8116, COM8116T, COM8126, COM8126T, COM8136, COM8136T, COM8146, COM8146T

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

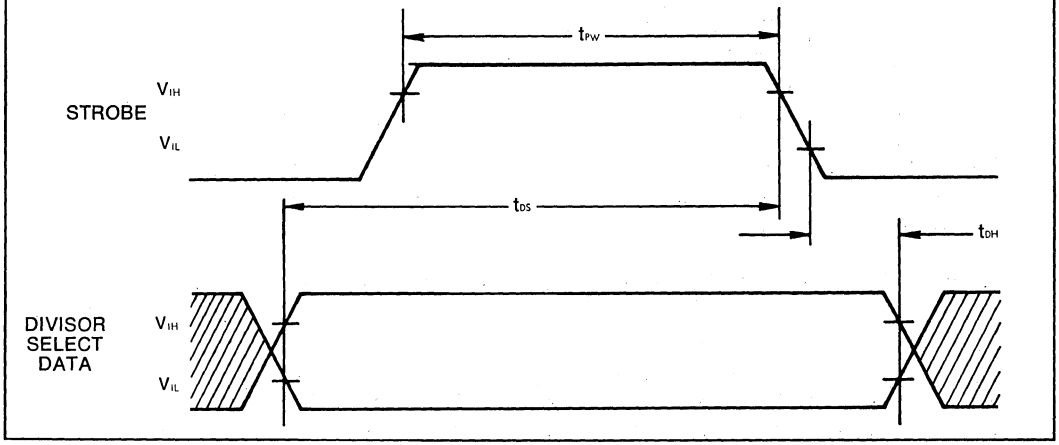
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

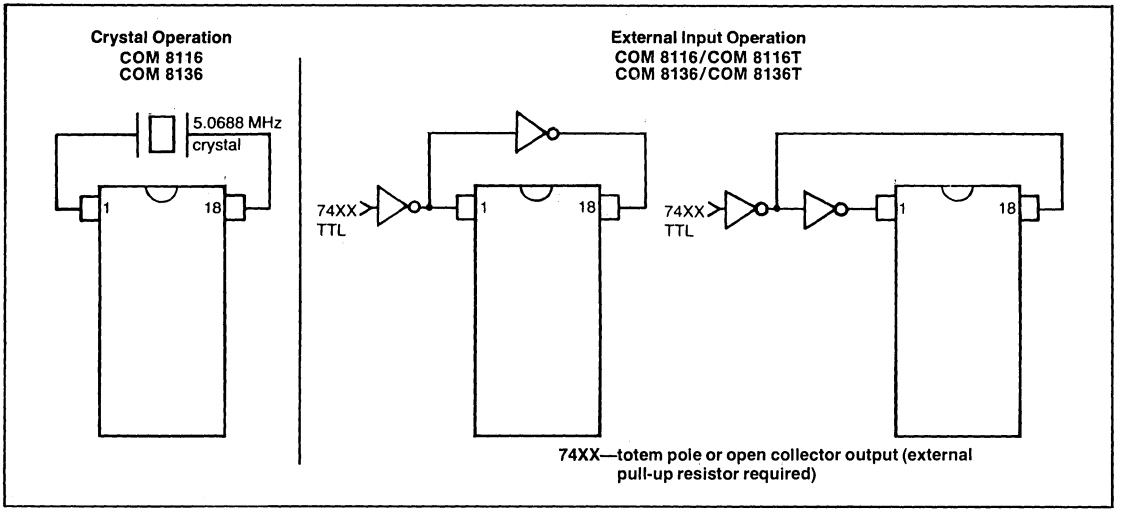
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

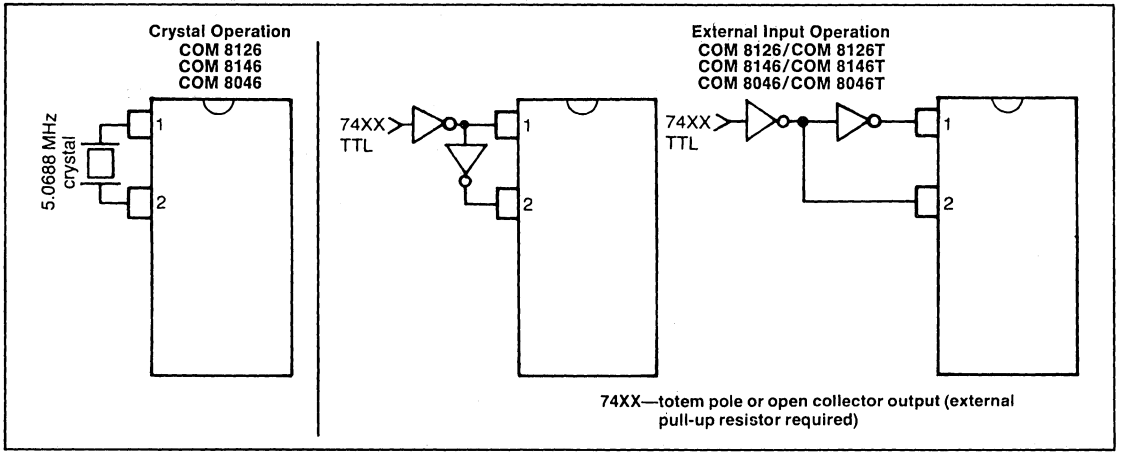
**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 2.0 | | | V | excluding XTAL inputs |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=1.6mA, for $f_X/4$, $f_O/16$ |
| | | | 0.4 | V | $I_{OL}$=3.2mA, for $f_O$, $f_R$, $f_T$ |
| | | | 0.4 | V | $I_{OL}$=0.8mA, for $f_X$ |
| High-level, $V_{OH}$ | 3.5 | | | V | $I_{OH}$=−100μA; for $f_X$, $I_{OH}$=−50μA |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | -0.1 | mA | $V_{IN}$=GND, excluding XTAL inputs |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pF | $V_{IN}$=GND, excluding XTAL inputs |
| EXT INPUT LOAD | | 8 | 10 | | Series 7400 equivalent loads |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 50 | mA | |
| **A.C. CHARACTERISTICS** | | | | | $T_A$= +25°C |
| CLOCK FREQUENCY, $f_{IN}$ | 0.01 | | 7.0 | MHz | XTAL/EXT, 50% Duty Cycle ±5% COM 8046, COM 8126, COM 8146 |
| | 0.01 | | 5.1 | MHz | XTAL/EXT, 50% Duty Cycle ±5% COM 8116, COM 8136 |
| STROBE PULSE WIDTH, $t_{PW}$ | 150 | | DC | ns | |
| INPUT SET-UP TIME | | | | | |
| $t_{DS}$ | 200 | | | ns | |
| INPUT HOLD TIME | | | | | |
| $t_{DH}$ | 50 | | | ns | |
| STROBE TO NEW FREQUENCY DELAY | | | 3.5 | μs | @ $f_X$=5.0 MHz |

**TIMING DIAGRAM**






For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

## Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency — 5.0688 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance <50 Ω
Series Resonant
Overall tolerance ± .01%
or as required

## Crystal manufacturers (Partial List)

**Northern Engineering Laboratories**
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

**Bulova Frequency Control Products**
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

**CTS Knights Inc.**
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

**Crystek Crystals Corporation**
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

# COM 8046
# COM 8046T



**Table 2**

REFERENCE FREQUENCY = 5.068800MHz

| Divisor Select EDCBA | Desired Baud Rate | Clock Factor | Desired Frequency (KHz) | Divisor | Actual Baud Rate | Actual Frequency (KHz) | Deviation |
|---|---|---|---|---|---|---|---|
| 00000 | 50.00 | 32X | 1.60000 | 3168 | 50.00 | 1.600000 | 0.0000% |
| 00001 | 75.00 | 32X | 2.40000 | 2112 | 75.00 | 2.400000 | 0.0000% |
| 00010 | 110.00 | 32X | 3.52000 | 1440 | 110.00 | 3.520000 | 0.0000% |
| 00011 | 134.50 | 32X | 4.30400 | 1177 | 134.58 | 4.306542 | 0.0591% |
| 00100 | 150.00 | 32X | 4.80000 | 1056 | 150.00 | 4.800000 | 0.0000% |
| 00101 | 200.00 | 32X | 6.40000 | 792 | 200.00 | 6.400000 | 0.0000% |
| 00110 | 300.00 | 32X | 9.60000 | 528 | 300.00 | 9.600000 | 0.0000% |
| 00111 | 600.00 | 32X | 19.20000 | 264 | 600.00 | 19.200000 | 0.0000% |
| 01000 | 1200.00 | 32X | 38.40000 | 132 | 1200.00 | 38.400000 | 0.0000% |
| 01001 | 1800.00 | 32X | 57.60000 | 88 | 1800.00 | 57.600000 | 0.0000% |
| 01010 | 2400.00 | 32X | 76.80000 | 66 | 2400.00 | 76.800000 | 0.0000% |
| 01011 | 3600.00 | 32X | 115.20000 | 44 | 3600.00 | 115.200000 | 0.0000% |
| 01100 | 4800.00 | 32X | 153.60000 | 33 | 4800.00 | 153.600000 | 0.0000% |
| 01101 | 7200.00 | 32X | 230.40000 | 22 | 7200.00 | 230.400000 | 0.0000% |
| 01110 | 9600.00 | 32X | 307.20000 | 16 | 9900.00 | 316.800000 | 3.1250% |
| 01111 | 19200.00 | 32X | 614.40000 | 8 | 19800.00 | 633.600000 | 3.1250% |
| 10000 | 50.00 | 16X | 0.80000 | 6336 | 50.00 | 0.800000 | 0.0000% |
| 10001 | 75.00 | 16X | 1.20000 | 4224 | 75.00 | 1.200000 | 0.0000% |
| 10010 | 110.00 | 16X | 1.76000 | 2880 | 110.00 | 1.760000 | 0.0000% |
| 10011 | 134.50 | 16X | 2.15200 | 2355 | 134.52 | 2.152357 | 0.0166% |
| 10100 | 150.00 | 16X | 2.40000 | 2112 | 150.00 | 2.400000 | 0.0000% |
| 10101 | 300.00 | 16X | 4.80000 | 1056 | 300.00 | 4.800000 | 0.0000% |
| 10110 | 600.00 | 16X | 9.60000 | 528 | 600.00 | 9.600000 | 0.0000% |
| 10111 | 1200.00 | 16X | 19.20000 | 264 | 1200.00 | 19.200000 | 0.0000% |
| 11000 | 1800.00 | 16X | 28.80000 | 176 | 1800.00 | 28.800000 | 0.0000% |
| 11001 | 2000.00 | 16X | 32.00000 | 158 | 2005.06 | 32.081013 | 0.2532% |
| 11010 | 2400.00 | 16X | 38.40000 | 132 | 2400.00 | 38.400000 | 0.0000% |
| 11011 | 3600.00 | 16X | 57.60000 | 88 | 3600.00 | 57.600000 | 0.0000% |
| 11100 | 4800.00 | 16X | 76.80000 | 66 | 4800.00 | 76.800000 | 0.0000% |
| 11101 | 7200.00 | 16X | 115.20000 | 44 | 7200.00 | 115.200000 | 0.0000% |
| 11110 | 9600.00 | 16X | 153.60000 | 33 | 9600.00 | 153.600000 | 0.0000% |
| 11111 | 19200.00 | 16X | 307.20000 | 16 | 19800.00 | 316.800000 | 3.1250% |

# Baud Rate Generator Output Frequency Options

**Table 1.** (16X clock)

**CRYSTAL FREQUENCY = 5.0688 MHz**

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6336 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4224 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.76 | — | 50/50 | 2880 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.1523 | 0.016 | 50/50 | 2355 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2112 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1056 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 528 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 264 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.8 | — | 50/50 | 176 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 32.081 | 0.253 | 50/50 | 158 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 132 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.6 | — | 50/50 | 88 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 66 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 115.2 | — | 50/50 | 44 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 48/52 | 33 |
| 1 | 1 | 1 | 1 | 19.200 | 307.2 | 316.8 | 3.125 | 50/50 | 16 |

**Table 2.** (16X clock)

**CRYSTAL FREQUENCY = 4.9152 MHz**

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6144 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4096 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.7589 | −0.01 | * | 2793 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.152 | — | 50/50 | 2284 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2048 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1024 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 512 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 256 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.7438 | −0.19 | * | 171 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 31.9168 | −0.26 | 50/50 | 154 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 128 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.8258 | 0.39 | * | 85 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 64 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 114.306 | −0.77 | * | 43 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 50/50 | 32 |
| 1 | 1 | 1 | 1 | 19,200 | 307.2 | 307.2 | — | 50/50 | 16 |

**Table 3.** (32X clock)

**CRYSTAL FREQUENCY = 5.0688 MHz**

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 32X Clock | Actual Frequency 32X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 1.6 KHz | 1.6 KHz | — | 50/50 | 3168 |
| 0 | 0 | 0 | 1 | 75 | 2.4 | 2.4 | — | 50/50 | 2112 |
| 0 | 0 | 1 | 0 | 110 | 3.52 | 3.52 | — | 50/50 | 1440 |
| 0 | 0 | 1 | 1 | 134.5 | 4.304 | 4.306 | .06 | * | 1177 |
| 0 | 1 | 0 | 0 | 150 | 4.8 | 4.8 | — | 50/50 | 1056 |
| 0 | 1 | 0 | 1 | 200 | 6.4 | 6.4 | — | 50/50 | 792 |
| 0 | 1 | 1 | 0 | 300 | 9.6 | 9.6 | — | 50/50 | 528 |
| 0 | 1 | 1 | 1 | 600 | 19.2 | 19.2 | — | 50/50 | 264 |
| 1 | 0 | 0 | 0 | 1200 | 38.4 | 38.4 | — | 50/50 | 132 |
| 1 | 0 | 0 | 1 | 1800 | 57.6 | 57.6 | — | 50/50 | 88 |
| 1 | 0 | 1 | 0 | 2400 | 76.8 | 76.8 | — | 50/50 | 66 |
| 1 | 0 | 1 | 1 | 3600 | 115.2 | 115.2 | — | 50/50 | 44 |
| 1 | 1 | 0 | 0 | 4800 | 153.6 | 153.6 | — | * | 33 |
| 1 | 1 | 0 | 1 | 7200 | 230.4 | 230.4 | — | 50/50 | 22 |
| 1 | 1 | 1 | 0 | 9600 | 307.2 | 316.8 | 3.125 | 50/50 | 16 |
| 1 | 1 | 1 | 1 | 19,200 | 614.4 | 633.6 | 3.125 | 50/50 | 8 |

**OUTPUT FREQUENCY OPTIONS**

| Dash Number | | |
|---|---|---|
| Table 1 | Table 2 | Table 3 |
| STD | −5 | −6 |
| STD | −5 | −6 |

*When Duty Cycle is not exactly 50%, it is 50% ± 10%.

# Baud Rate Generator Output Frequency Options

## COM 8116T-013

CRYSTAL FREQUENCY = 2.76480 MHz

| Transmit/ Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | 0 | 50/50 | 3456 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | 0 | 50/50 | 2304 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.76 | −.006 | 50/50 | 1571 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.152 | −.019 | 50/50 | 1285 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | 0 | 50/50 | 1152 |
| 0 | 1 | 0 | 1 | 200 | 3.2 | 3.2 | 0 | 50/50 | 864 |
| 0 | 1 | 1 | 0 | 300 | 4.8 | 4.8 | 0 | 50/50 | 576 |
| 0 | 1 | 1 | 1 | 600 | 9.6 | 9.6 | 0 | 50/50 | 288 |
| 1 | 0 | 0 | 0 | 1200 | 19.2 | 19.2 | 0 | 50/50 | 144 |
| 1 | 0 | 0 | 1 | 1800 | 28.8 | 28.8 | 0 | 50/50 | 96 |
| 1 | 0 | 1 | 0 | 2000 | 32.0 | 32.149 | +.465 | 50/50 | 86 |
| 1 | 0 | 1 | 1 | 2400 | 38.4 | 38.4 | 0 | 50/50 | 72 |
| 1 | 1 | 0 | 0 | 3600 | 57.6 | 57.6 | 0 | 50/50 | 48 |
| 1 | 1 | 0 | 1 | 4800 | 76.8 | 76.8 | 0 | 50/50 | 36 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | 0 | 50/50 | 18 |
| 1 | 1 | 1 | 1 | 19,200 | 307.2 | 307.2 | 0 | 44/56 | 9 |

## COM 8116T-003

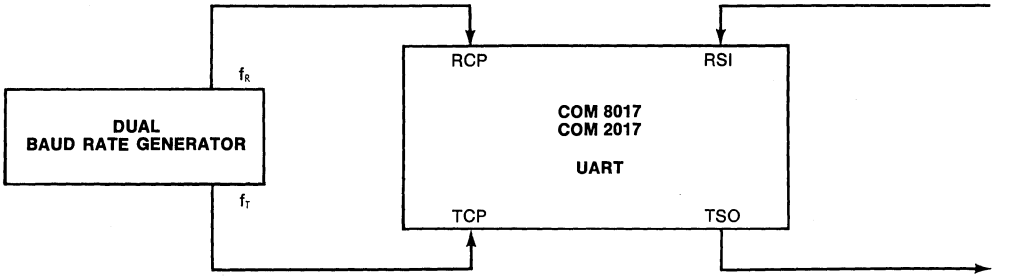
CRYSTAL FREQUENCIES = 6.01835 MHz

| Transmit/ Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 799.9 Hz | 0 | 50/50 | 7523 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1200.0 | 0 | 50/50 | 5015 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1759.7 | 0 | 50/50 | 3420 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2151.7 | 0 | 50/50 | 2797 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2399.6 | 0 | 50/50 | 2508 |
| 0 | 1 | 0 | 1 | 200 | 3.2 | 3199.5 | 0 | 50/50 | 1881 |
| 0 | 1 | 1 | 0 | 300 | 4.8 | 4799.3 | 0 | 50/50 | 1254 |
| 0 | 1 | 1 | 1 | 600 | 9.6 | 9598.6 | 0 | 50/50 | 627 |
| 1 | 0 | 0 | 0 | 1200 | 19.2 | 19227.9 | +0.14 | 50/50 | 313 |
| 1 | 0 | 0 | 1 | 1800 | 28.8 | 28795.9 | 0 | 50/50 | 209 |
| 1 | 0 | 1 | 0 | 2000 | 32.0 | 32012.5 | 0 | 50/50 | 188 |
| 1 | 0 | 1 | 1 | 2400 | 38.4 | 38333.4 | −0.17 | 50/50 | 157 |
| 1 | 1 | 0 | 0 | 3600 | 57.6 | 57868.7 | +0.46 | 50/50 | 104 |
| 1 | 1 | 0 | 1 | 4800 | 76.8 | 77158.3 | +0.46 | 50/50 | 78 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 154316.6 | +0.46 | 50/50 | 39 |
| 1 | 1 | 1 | 1 | 19,200 | 307.2 | 300917.5 | 2.04 | 50/50 | 20 |

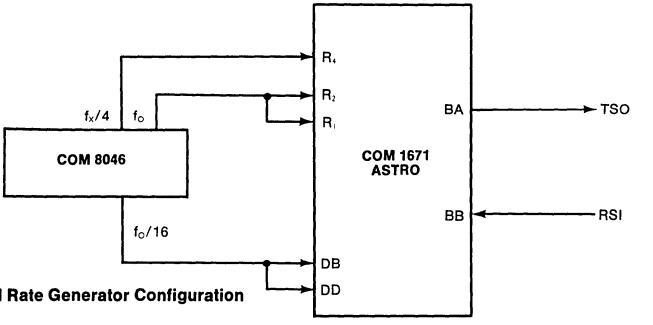
## COM 8116T-013A

CRYSTAL FREQUENCY—5.52960 MHz

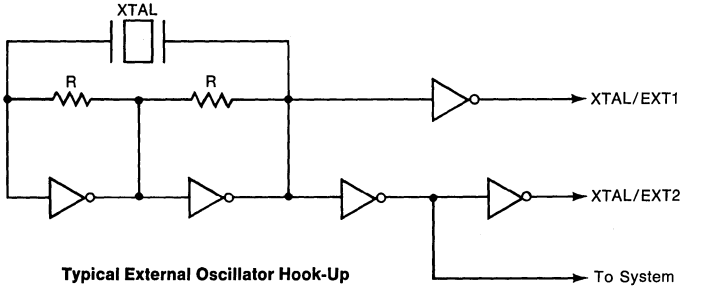
| Transmit/ Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 100 | 1.6 KHz | 1.6 KHz | 0 | 50/50 | 3456 |
| 0 | 0 | 0 | 1 | 150 | 2.4 | 2.4 | 0 | 50/50 | 2304 |
| 0 | 0 | 1 | 0 | 220 | 3.52 | 3.5197 | −.006 | 50/50 | 1571 |
| 0 | 0 | 1 | 1 | 269 | 4.304 | 4.3032 | −.019 | 50/50 | 1285 |
| 0 | 1 | 0 | 0 | 300 | 4.8 | 4.8 | 0 | 50/50 | 1152 |
| 0 | 1 | 0 | 1 | 400 | 6.4 | 6.4 | 0 | 50/50 | 864 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | 0 | 50/50 | 576 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | 0 | 50/50 | 288 |
| 1 | 0 | 0 | 0 | 2400 | 38.4 | 38.4 | 0 | 50/50 | 144 |
| 1 | 0 | 0 | 1 | 3600 | 57.6 | 57.6 | 0 | 50/50 | 96 |
| 1 | 0 | 1 | 0 | 4000 | 64.0 | 64.298 | +.466 | 50/50 | 86 |
| 1 | 0 | 1 | 1 | 4800 | 76.8 | 76.8 | 0 | 50/50 | 72 |
| 1 | 1 | 0 | 0 | 7200 | 115.2 | 115.2 | 0 | 50/50 | 48 |
| 1 | 1 | 0 | 1 | 9600 | 153.6 | 153.6 | 0 | 50/50 | 36 |
| 1 | 1 | 1 | 0 | 19,200 | 307.2 | 307.2 | 0 | 50/50 | 18 |
| 1 | 1 | 1 | 1 | 38,400 | 614.8 | 614.8 | 0 | 44/56 | 9 |



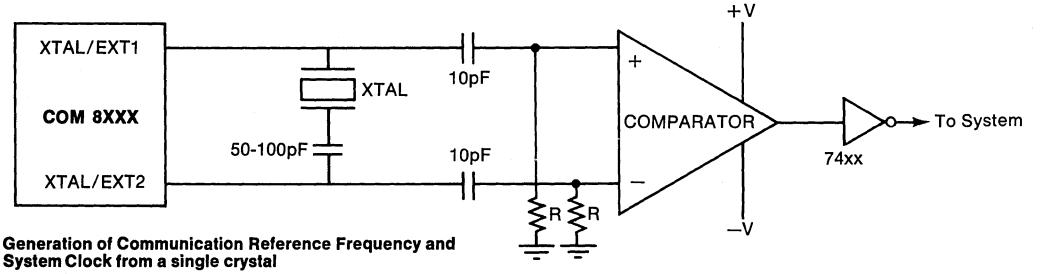

**Typical UART—Dual Baud Rate Generator Configuration**
**Full Duplex—Split Speed**




**Typical ASTRO—Baud Rate Generator Configuration**




**Typical External Oscillator Hook-Up**




**Generation of Communication Reference Frequency and System Clock from a single crystal**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273 3100 TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# COM 8156
# COM 8156T
**PRELIMINARY**

# Dual Baud Rate Generator
## Programmable Divider



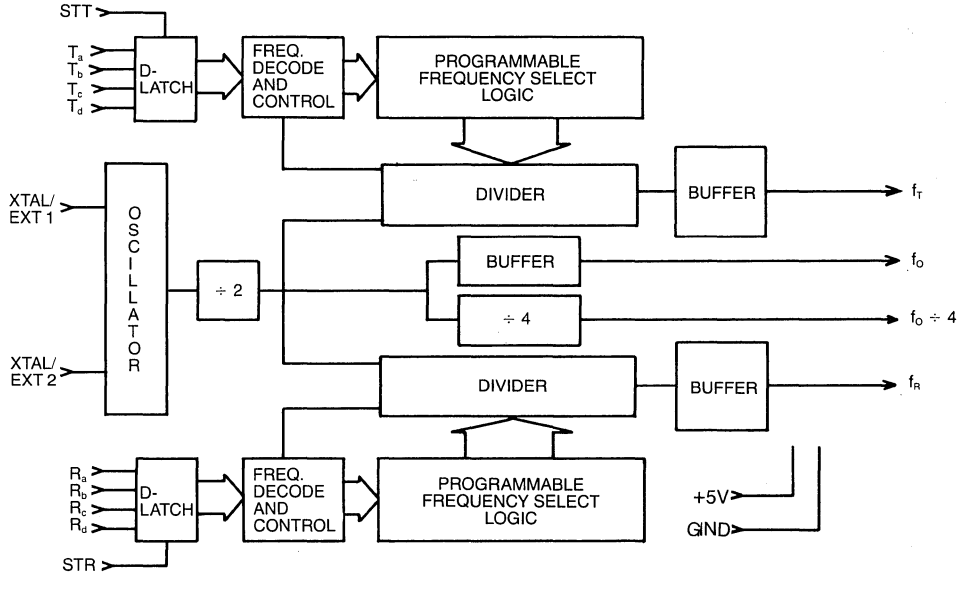
### FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ High crystal/clock frequency operation
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ High frequency reference outputs
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ N-channel silicon gate technology
- ☐ Single $+5_V$ power supply
- ☐ TTL, MOS compatibility
- ☐ Re-programmable ROM technology allows generation of other frequencies

### PIN CONFIGURATION

| | | | |
|---|---|---|---|
| Rb | 1 | 18 | Ra |
| Rc | 2 | 17 | $f_R$ |
| Rd | 3 | 16 | Vcc |
| STR | 4 | 15 | $XTAL_1$ |
| $XTAL_2$ | 5 | 14 | fo |
| fo/4 | 6 | 13 | $f_T$ |
| GND | 7 | 12 | Ta |
| STT | 8 | 11 | Tb |
| Td | 9 | 10 | Tc |

### BLOCK DIAGRAM



## GENERAL DESCRIPTION

The Standard Microsystem's COM8156 is a dual baud rate generator that operates at twice the crystal/clock frequency of the COM8116/36. It is fabricated using SMC's patented COPLAMOS™ technology and employs depletion mode loads allowing operation from a single +5V supply.

The standard COM8156 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM8156 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 9. Parts suitable for use only with an external TTL reference are marked COM 8156T. TTL outputs used to drive the COM8156 or COM8156T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies $f_T$, $f_R$. The dividers are capable of dividing by an integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer that it is low by one $f_O$ clock period.

The crystal frequency is divided by two to give ($f_O$) and again by four to give ($f_{O/4}$). The transmit ($f_T$) and receive ($f_R$) frequencies are obtained by dividing ($f_O$) by N. Up to 32 different divisors can be mask-programmed on custom parts to accommodate different crystal frequencies and divider schemes. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5us of a change in any of the four divisor select bits (strobe activity is not required). The divisor select bits (strobe activity is not required). The divisor select inputs and the strobe inputs have pull-up resistors.

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 15 | XTAL/EXT 1 | Crystal | This input receives one pin of the crystal package. |
| 16 | $V_{CC}$ | Power Supply | +5 Volt Supply. |
| 17 | $f_R$ | Receiver Output | This output runs at a frequency selected by the Receiver Address Inputs. |
| 18<br>1-3 | $R_a$ $R_b$ $R_c$, $R_d$ | Receiver<br>Divisor Select<br>Address | The logic level on these inputs as shown in Table 1, selects the receiver output frequency, $f_R$. |
| 4 | STR | Strobe-Receiver<br>Address | A high-level input strobe loads the receiver address ($R_a$, $R_b$, $R_c$, $R_d$) into the receiver address register. This input may be strobed or hard wired to +5V. |
| 5 | XTAL/EXT 2 | Crystal | This input receives one pin of the crystal package. |
| 6 | $f_{o/4}$ | Oscillator<br>Output | This output runs at a frequency selected by the crystal ÷ 8. |
| 7 | GND | Ground | Ground |
| 8 | STT | Strobe-Transmitter<br>Address | A high-level input strobe loads the transmitter address ($T_a$, $T_b$, $T_c$, $T_d$) into the transmitter address register. This input may be strobed or hard wired to +5V. |
| 9-12 | $T_d$ $T_c$, $T_b$ $T_a$ | Transmitter<br>Divisor Select<br>Address | The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, $f_T$. |
| 13 | $f_T$ | Transmitter<br>Output Frequency | This output runs at a frequency selected by the Transmitter Address inputs. |
| 14 | $f_o$ | Oscillator<br>Output Frequency | This output runs at a frequency selected by the crystal ÷ 2. |

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

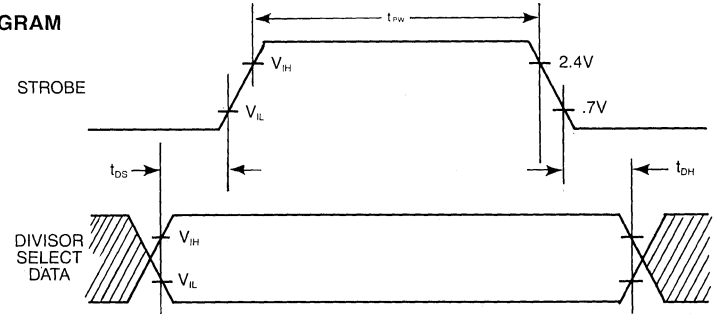
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.



**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%, unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{IL}$ | | | 0.8 | V | |
| High Level $V_{IH}$ | 2.0 | | | V | excluding XTAL inputs |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA, for $f_{o4}$ |
| | | | 0.4 | V | $I_{OL}$ = 3.2 mA, for $f_R$, $f_T$ |
| High Level $V_{OH}$ | | | 0.5 | V | $I_{OL}$ = 3.2 mA, for $f_O$ |
| | 2.4 | | | V | $I_{OH}$ = −100 µA |
| INPUT CURRENT | | | | | |
| Low-level, $I_{IL}$ | | | −0.1 | mA | $V_{IN}$ = GND, excluding XTAL inputs |
| INPUT CAPACITANCE | | | | | |
| All inputs, $C_{IN}$ | | 5 | 10 | pF | $V_{IN}$ = GND, excluding XTAL inputs |
| EXT INPUT LOAD | | 8 | 10 | | Series 7400 equivalent loads |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 60 | mA | |
| **AC CHARACTERISTICS** | | | | | |
| CLOCK FREQUENCY, $f_{IN}$ | 5.0 | | 11.0 | MHz | XTAL/EXT, 50% Duty Cycle ±5% |
| STROBE PULSE WIDTH, $t_{PW}$ | 150 | | DC | ns | |
| INPUT SET-UP TIME | | | | | |
| $t_{DS}$ | 50 | | | ns | |
| INPUT HOLD TIME | | | | | |
| $T_{DH}$ | 50 | | | ns | |
| STROBE TO NEW FREQ. DELAY | | | 3.5 | µs | |
| OUTPUT CLOCKS DUTY CYCLE | | | | | |
| $f_O$ | 40 | | 60 | % | @ 1.5V LEVEL |
| $f_{O4}$ | 45 | | 55 | % | @ 1.5V LEVEL |
| $f_R$, $f_T$ | 48 | | 52 | % | @ 1.5V LEVEL |
| **CRYSTAL CHARACTERISTICS** | | | | | |
| Series Crystal Resistance | | 30 | 70 | | @ Resonance |
| Crystal Shunt Capacitance | 2 | 5 | 10 | pf | |

## TIMING DIAGRAM




## Baud Rate Generator Output Frequency Options

**COM8156/COM8156T (16X clock)**

**CRYSTAL FREQUENCY = 10.1376 MHz**

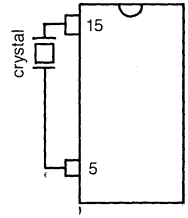
| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6336 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4224 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.76 | — | 50/50 | 2880 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.1523 | 0.016 | 50/50 | 2355 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2112 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1056 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 528 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 264 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.8 | — | 50/50 | 176 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 32.081 | 0.253 | 50/50 | 158 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 132 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.6 | — | 50/50 | 88 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 66 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 115.2 | — | 50/50 | 44 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 48/52 | 33 |
| 1 | 1 | 1 | 1 | 19.200 | 307.2 | 316.8 | 3.125 | 50/50 | 16 |

**COM8156-005/COM8156T-005 (16X clock)**

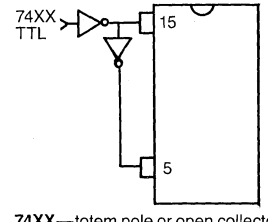
**CRYSTAL FREQUENCY = 9.8304 MHz**

| Tr'mit/Receive Address D | C | B | A | Baud Rate | Theoretical Frequency 16X Clock | Actual Frequency 16X Clock | Percent Error | Duty Cycle % | Divisor |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 50 | 0.8 KHz | 0.8 KHz | — | 50/50 | 6144 |
| 0 | 0 | 0 | 1 | 75 | 1.2 | 1.2 | — | 50/50 | 4096 |
| 0 | 0 | 1 | 0 | 110 | 1.76 | 1.7589 | −0.01 | * | 2793 |
| 0 | 0 | 1 | 1 | 134.5 | 2.152 | 2.152 | — | 50/50 | 2284 |
| 0 | 1 | 0 | 0 | 150 | 2.4 | 2.4 | — | 50/50 | 2048 |
| 0 | 1 | 0 | 1 | 300 | 4.8 | 4.8 | — | 50/50 | 1024 |
| 0 | 1 | 1 | 0 | 600 | 9.6 | 9.6 | — | 50/50 | 512 |
| 0 | 1 | 1 | 1 | 1200 | 19.2 | 19.2 | — | 50/50 | 256 |
| 1 | 0 | 0 | 0 | 1800 | 28.8 | 28.7438 | −0.19 | * | 171 |
| 1 | 0 | 0 | 1 | 2000 | 32.0 | 31.9168 | −0.26 | 50/50 | 154 |
| 1 | 0 | 1 | 0 | 2400 | 38.4 | 38.4 | — | 50/50 | 128 |
| 1 | 0 | 1 | 1 | 3600 | 57.6 | 57.8258 | 0.39 | * | 85 |
| 1 | 1 | 0 | 0 | 4800 | 76.8 | 76.8 | — | 50/50 | 64 |
| 1 | 1 | 0 | 1 | 7200 | 115.2 | 114.306 | −0.77 | * | 43 |
| 1 | 1 | 1 | 0 | 9600 | 153.6 | 153.6 | — | 50/50 | 32 |
| 1 | 1 | 1 | 1 | 19.200 | 307.2 | 307.2 | — | 50/50 | 16 |

### Crystal Operation




### External Input Operation




**74XX**—totem pole or open collector output (external pull-up resistor required)

For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

### Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency: 10.1376 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance <50 Ω
Series Resonant
Overall tolerance ±.01%
or as required

### Crystal manufacturers (Partial List)

**Northern Engineering Laboratories**
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

**Bulova Frequency Control Products**
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

**CTS Knights Inc.**
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

**Crystek Crystals Corporation**
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109


STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898



Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

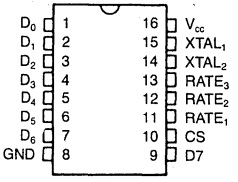
# COM81C66
**PRELIMINARY**

# Universal Rate Generator & Timer

## FEATURES

- ☐ Three independent 32 bit programmable counters
- ☐ Clock input from DC to 16 MHz
- ☐ Low power CMOS
- ☐ 8/16-pin Dual-In-Line package
- ☐ Uses a crystal or a TTL signal as frequency source
- ☐ Single +5 Volt power supply

## PIN CONFIGURATION




PACKAGE: 16-pin D.I.P.

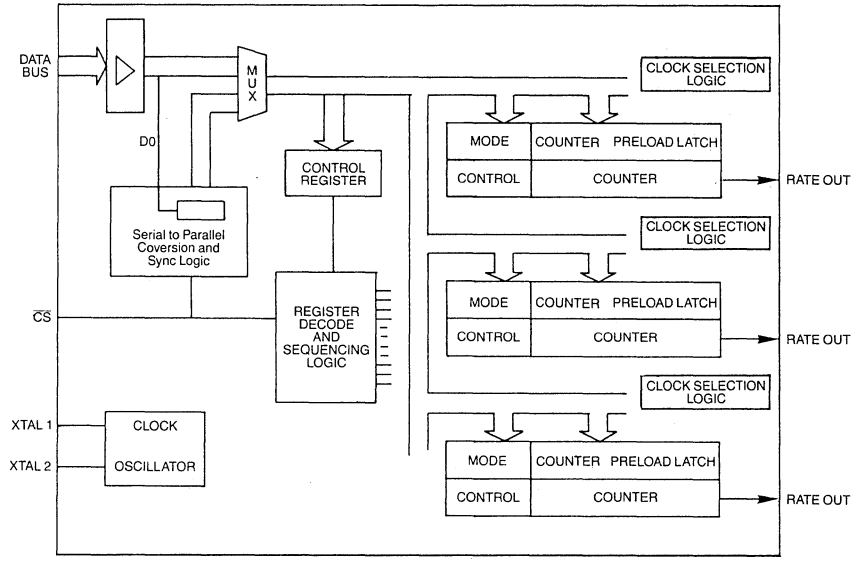
SECTION IV

## GENERAL DESCRIPTION

The TIMER chip is a device designed to provide a convenient and inexpensive solution to applications requiring programmable multiple clock divider sources. The source frequency can be either an integrated crystal controlled oscillator, or an external TTL signal. The TIMER consists of a data input portion, a register addressing block and three counter blocks.

The counter blocks are accessed and programmed independently and they can be configured to operate in various modes simultaneously.

The TIMER chip serves a broad range of applications some of which are: Programmable rate generations, pulse generation, motor control, real time clock, interrupt applications and others.




**COM8166 BLOCK DIAGRAM**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications: consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# CRT Display

## TIMING CONTROLLERS

| Part Number | Description | Features | Display Format | Max Clock | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 5027 | Provides all of the timing and control for interlaced and non-interlaced CRT display | | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 5037 | | Balanced beam interlace | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 5047 | | Fixed format | 80 column 24 row | 4MHZ | +5, +12 | 40 DIP | 301-302 |
| CRT 5057 | | Line-lock | Programmable | 4MHz | +5, +12 | 40 DIP | 293-300 |
| CRT 7220A, -1, -2 | Graphics Display Controller | Intelligent graphics display controller | 1024 x 1024 Pixel | 6, 7, 8 MHz | +5 | 40 DIP | 309-332 |
| CRT 9007A, B, C | CRT video processor and controller | Sequential or row-table driven memory programmable DMA | Programmable | A-3.7 MHz B-3.33 MHz C-2.5 MHz | +5 | 40 DIP | 369-388 |
| CRT 97C11[2] | 3rd generation CRT controller which allows manipulation of independent window areas on screen | Control of window size and position, window attributes, prog cursor, max of 127 windows, DRAM refresh | Up to 16K pixels vertical and 1KxN (N = display memory width) in horizontal pixels | TBD | +5 | 68 PLCC | 455-456 |

## VIDEO TERMINAL LOGIC CONTROLLERS

| Part Number | Description | Features | Display Format | Attributes | Max Clock | Power Supply | Package | Page |
|---|---|---|---|---|---|---|---|---|
| CRT 9028/ 9128[1] | Complete CRT video processor and controller. Display and attribute control for alphanumeric and graphics display. Two types of processor interface signals differentiate the two parts. | Separate display memory eliminates contention, smooth scroll, status row, on-board clock, and video shift register. | Mask programmable, 5x8 character font, 8x12 character cell. | Tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics. | 14MHz | +5 | 40 DIP | 401-416 |
| CRT 9053/ 9153[1] | | | Mask programmable, 7x11 character font, 9x13 character cell. | Embedded or tagged attributes: reverse video, blank, blink, underline, intensity and wide/thin graphics. | 18.7MHz | | | 433-448 |

## CHARACTER GENERATORS

| Part Number | Description | Max Frequency | Power Supply | Package | Page |
|---|---|---|---|---|---|
| CRT 7004A[3,4] | 7 x 11 x 128 character generator, latches, video shift register | 20 MHz | +5 | 24 DIP | 303-308 |
| CRT 7004B[3,4] | | 15 MHz | | | |
| CRT 7004C[3,4] | | 10 MHz | | | |

## ROW BUFFER

| Part Number | Description | Max Row Length | Power Supply | Package | Page |
|---|---|---|---|---|---|
| CRT 9006-83 | 8 bit wide serial cascadable single row buffer memory for CRT or printer | 83 characters | +5 | 24 DIP | 363-368 |
| CRT 9006-135 | | 135 characters | | | |
| CRT 9212 | 8 bit wide serial cascadable double row buffer memory for CRT or printer | 135 characters | +5 | 28 DIP | 449-454 |

[1]May be custom mask programmed [2]For future release [4]Also available as CRT7004A, B, C -003 5 x 7 dot matrix

# CRT Display CONT.

## VDAC™ DISPLAY CONTROLLERS

| Part Number | Description | Display | Attributes | Max Clock | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 8002H | Provides complete display and attributes control for alphanumeric and graphic display. Consists of 7 x 11 x 128 character generator, video shift register latches, graphics and attributes circuits. | 7x11 dot matrix, wide graphics, thin graphics, on-chip cursor | Reverse video blank blink underline strike-thru | 25 MHz | +5 | 28 DIP | 347-354 |
| CRT 8002A[1,3] | | | | 20 MHz | | | 333-346 |
| CRT 8002B[1,3] | | | | 15 MHz | | | 333-346 |
| CRT 8002C[1,3] | | | | 10 MHz | | | 333-346 |

## VIDEO ATTRIBUTES CONTROLLERS

| Part Number | Description | Display | Attributes | Max Clock | Power Supply | Package | Page |
|---|---|---|---|---|---|---|---|
| CRT 8021 | Provides attributes and graphics control for CRT video displays | Alphanumeric, wide graphics, thin graphics, on-chip cursor | Reverse video, blank, blink underline, strike-thru | 20 MHz | +5 | 28 DIP | 355-362 |
| CRT 9021B | Provides attributes and graphics control for CRT video displays | Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width | Reverse video, blank, blink underline, intensity | 28.5 MHz | +5 | 28 DIP | 389-400 |
| CRT 9041A, B, C | Provides attributes and graphics control for CRT video displays. Full VT100® and VT220® compatible | Alphanumeric, wide and thin graphics, 4 cursor modes, double height/width, 12 bit shift register | Reverse video, blink, blank, underline, 4 intensity levels | A-33 MHz B-30 MHz C-28.5 MHz | +5 | 40 DIP | 417-432 |

[1]May be custom mask programmed [3]Also available as CRT8002A, B, C-001 Katakana
CRT8002A, B, C-003, -018 5 x 7 dot matrix

VT100 and VT220 are registered trademarks of Digital Equipment Corp.

STANDARD MICROSYSTEMS CORPORATION

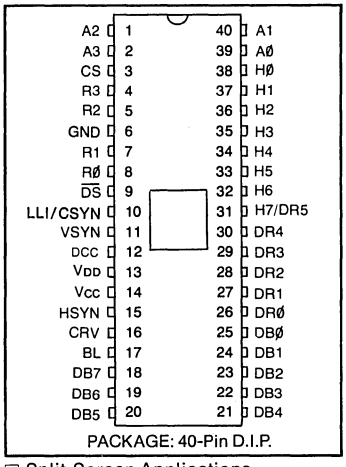
# CRT 5027
# CRT 5037
# CRT 5057
## μPC FAMILY

# CRT Video Timer and Controller
# VTAC®

## FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

## PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

## GENERAL DESCRIPTION

The CRT Video Timer and Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

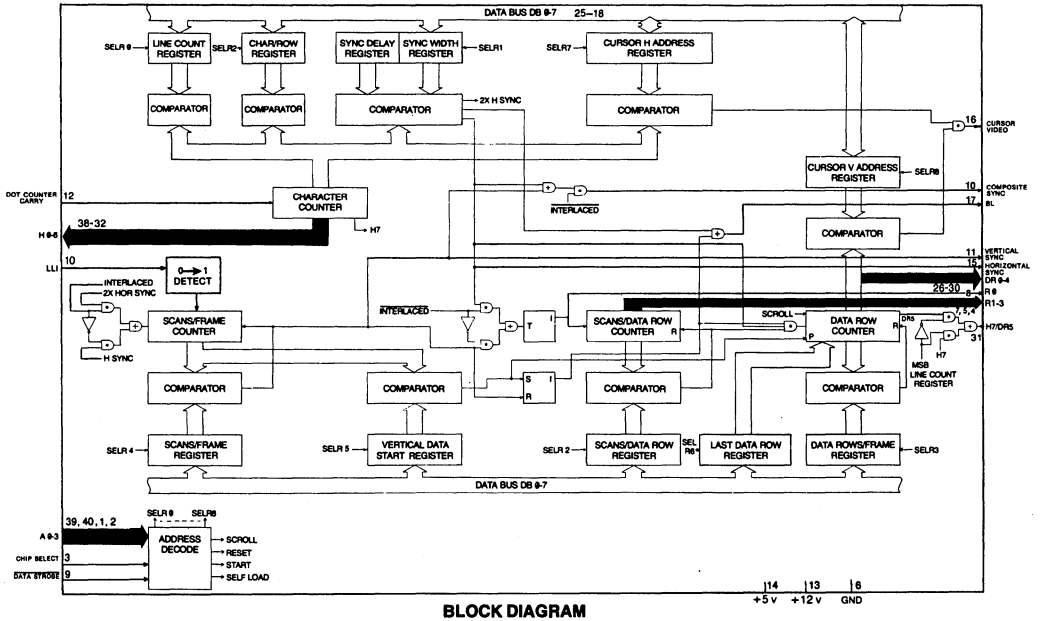
Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

## Description of Pin Functions

| Pin No. | Symbol | Name | Input/ Output | Function |
|---|---|---|---|---|
| 25-18 | DBØ-7 | Data Bus | I/O | Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address. |
| 3 | CS | Chip Select | I | Signals chip that it is being addressed |
| 39,40,1,2 | AØ-3 | Register Address | I | Register address bits for selecting one of seven control registers or either of the cursor address registers |
| 9 | $\overline{DS}$ | Data Strobe | I | Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus |
| 12 | DCC | DOT Counter Carry | I | Carry from off chip dot counter establishing basic character clock rate. Character clock. |
| 38-32 | HØ-6 | Character Counter Outputs | O | Character counter outputs. |
| 7, 5, 4 | R1-3 | Scan Counter Outputs | O | Three most significant bits of the Scan Counter; row select inputs to character generator. |
| 31 | H7/DR5 | H7/DR5 | O | Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≧128; otherwise output is MSB of Data Row Counter. |
| 8 | RØ | Scan Counter LSB | O | Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate. |
| 26-30 | DRØ-4 | Data Row Counter Outputs | O | Data Row counter outputs. |
| 17 | BL | Blank | O | Defines non active portion of horizontal and vertical scans. |
| 15 | HSYN | Horizontal Sync | O | Initiates horizontal retrace. |
| 11 | VSYN | Vertical Sync | O | Initiates vertical retrace. |
| 10 | CSYN/ LLI | Composite Sync Output/ Line Lock Input | O/I | Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin. |
| 16 | CRV | Cursor Video | O | Defines cursor location in data field. |
| 14 | $V_{CC}$ | Power Supply | PS | +5 volt Power Supply |
| 13 | $V_{DD}$ | Power Supply | PS | +12 volt Power Supply |




**BLOCK DIAGRAM**

## Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

| | |
|---|---|
| Characters/Data Row | A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132. |
| Horizontal Sync Delay | 3 bits assigned providing up to 8 character times for generation of "front porch". |
| Horizontal Sync Width | 4 bits assigned providing up to 15 character times for generation of horizontal sync width. |
| Horizontal Line Count | 8 bits assigned providing up to 256 character times for total horizontal formatting. |
| Skew Bits | A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code. |

Vertical Formatting:

| | |
|---|---|
| Interlaced/Non-interlaced | This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode. |
| Scans/Frame | 8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits.<br>1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.<br>Range = 513 to 1023 scans/frame, odd counts only.<br>2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).<br>Range = 256 to 766 scans/frame, even counts only.<br>In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H). |
| Vertical Data Start | 8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page. |
| Data Rows/Frame | 6 bits assigned providing up to 64 data rows per frame. |
| Last Data Row | 6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row. |
| Scans/Data Row | 4 bits assigned providing up to 16 scan lines per data row. |

## Additional Features

*Device Initialization:*

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

## Control Registers Programming Chart

**Horizontal Line Count:** Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

**Characters/Data Row:**

| DB2 | DB1 | DB0 | | |
|---|---|---|---|---|
| 0 | 0 | 0 | = 20 | Active Characters/Data Row |
| 0 | 0 | 1 | = 32 | |
| 0 | 1 | 0 | = 40 | |
| 0 | 1 | 1 | = 64 | |
| 1 | 0 | 0 | = 72 | |
| 1 | 0 | 1 | = 80 | |
| 1 | 1 | 0 | = 96 | |
| 1 | 1 | 1 | = 132 | |

**Horizontal Sync Delay:** = N, from 1 to 7 character times (DB0 = LSB) (N = 0 Disallowed)

**Horizontal Sync Width:** = N, from 1 to 15 character times (DB3 = LSB) (N = 0 Disallowed)

**Skew Bits**

| DB7 | DB6 | Sync/Blank Delay (Character Times) | Cursor Delay |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 2 | 1 |
| 1 | 1 | 2 | 2 |

**Scans/Frame**

8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. (DB0 = LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.

Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).

Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (=3H).

**Vertical Data Start:** N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

**Data Rows/Frame:** Number of data rows = N + 1, N = 0 to 63 (DBO = LSB)

**Last Data Row:** N = Address of last dsplayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

**Mode:** Register, 1, DB7 = 1 establishes Interlace.

**Scans/Data Row:**

Interlace Mode

CRT 5027: Scans per Data Row = N + 1 where N = programmed number of scans/data rows. N = 0 to 15. Scans per data row must be even counts only.

CRT 5037, CRT 5057: Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037, CRT 5057: Scans per Data Row = N + 1, odd or even count. N = 0 to 15.

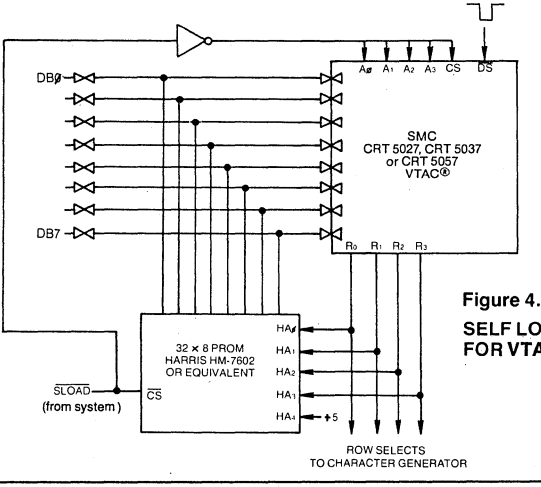



**Figure 4.**

**SELF LOADING SCHEME FOR VTAC® SET-UP**

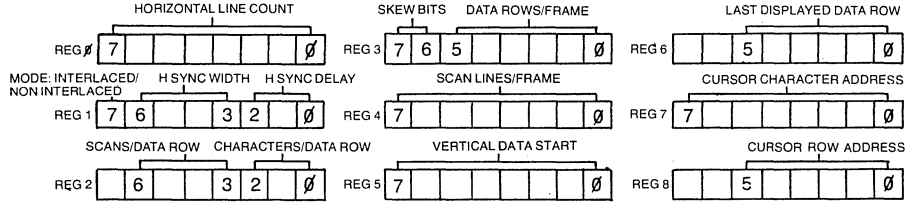
## Register Selects/Command Codes

| A3 | A2 | A1 | AØ | Select/Command | Description |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Load Control Register Ø | See Table 1 |
| 0 | 0 | 0 | 1 | Load Control Register 1 | |
| 0 | 0 | 1 | 0 | Load Control Register 2 | |
| 0 | 0 | 1 | 1 | Load Control Register 3 | |
| 0 | 1 | 0 | 0 | Load Control Register 4 | |
| 0 | 1 | 0 | 1 | Load Control Register 5 | |
| 0 | 1 | 1 | 0 | Load Control Register 6 | |
| 0 | 1 | 1 | 1 | Processor Initiated Self Load | Command from processor instructing VTAC® to enter Self Load Mode (via external PROM) |
| 1 | 0 | 0 | 0 | Read Cursor Line Address | |
| 1 | 0 | 0 | 1 | Read Cursor Character Address | |
| 1 | 0 | 1 | 0 | Reset | Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command. |
| 1 | 0 | 1 | 1 | Up Scroll | Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0. |
| 1 | 1 | 0 | 0 | Load Cursor Character Address* | |
| 1 | 1 | 0 | 1 | Load Cursor Line Address* | |
| 1 | 1 | 1 | 0 | Start Timing Chain | Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command. |
| 1 | 1 | 1 | 1 | Non-Processor Self Load | Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed. |

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

**TABLE 1**

**BIT ASSIGNMENT CHART**



## AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

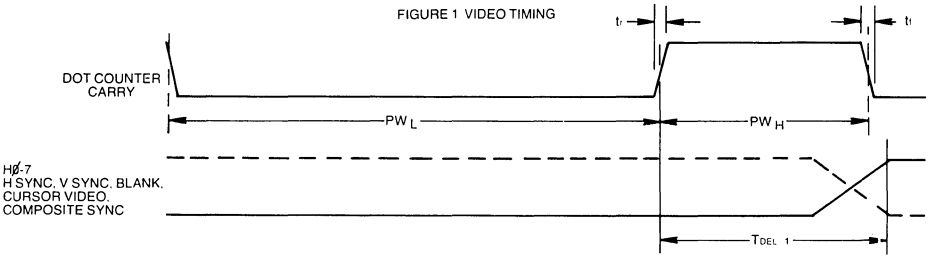



FIGURE 2 LOAD/READ TIMING

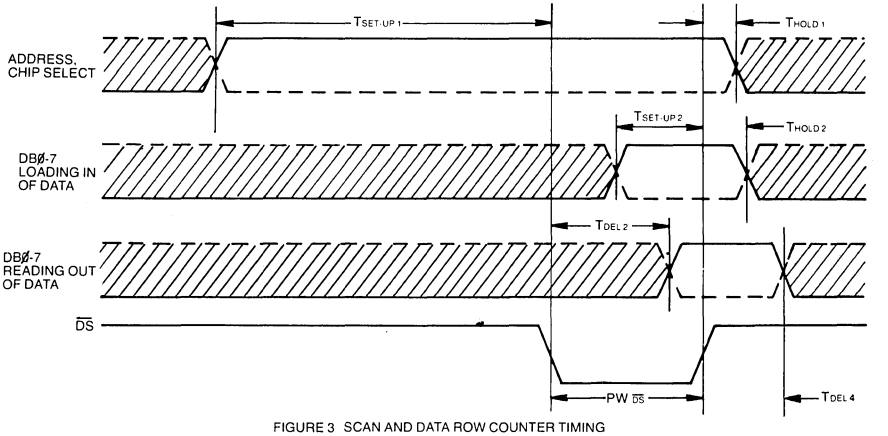
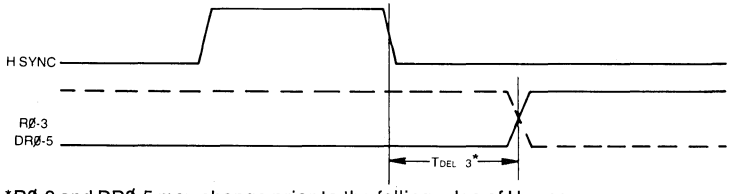
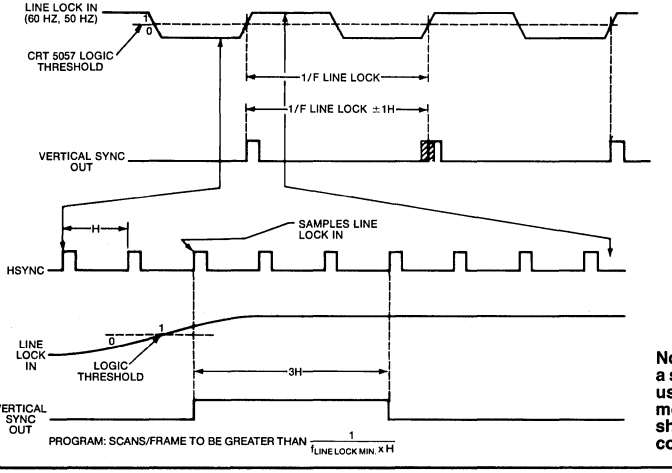



FIGURE 3 SCAN AND DATA ROW COUNTER TIMING




*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

## CRT 5057 LINE LOCK




**Note: To ensure a stable display when using the line lock mode, the CRT 5057 should be used with DC coupled monitors only.**

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, $V_{DD}$=+12V±5%, unless otherwise noted)

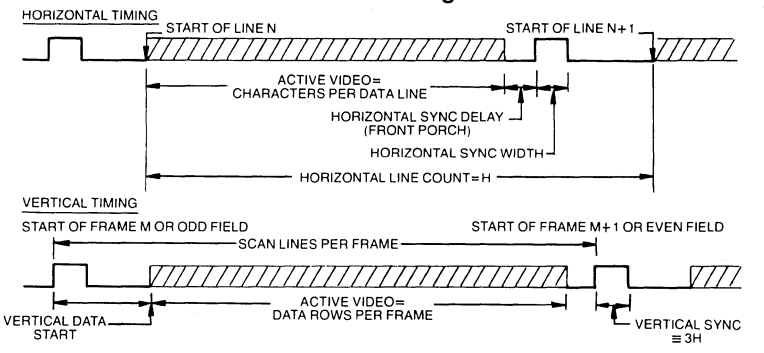
| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{IL}$ | | | 0.8 | V | |
| High Level, $V_{IH}$ | $V_{CC}$−1.5 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level—$V_{OL}$ for RØ-3 | | | 0.4 | V | $I_{OL}$=3.2ma |
| Low Level—$V_{OL}$ all others | | | 0.4 | V | $I_{OL}$=1.6ma |
| High Level—$V_{OH}$ for RØ-3, DBØ-7 | 2.4 | | | | $I_{OH}$=80μa |
| High Level—$V_{OH}$ all others | 2.4 | | | | $I_{OH}$=40μa |
| INPUT CURRENT | | | | | |
| **Low Level, $I_{IL}$ (Address, CS only)** | | | 250 | μA | $V_{IN}$=0.4V |
| **Leakage, $I_{IL}$ (All Inputs except Address, CS)** | | | 10 | μA | O≤$V_{IN}$≤$V_{CC}$ |
| INPUT CAPACITANCE | | | | | |
| Data Bus, $C_{IN}$ | | 10 | 15 | pF | |
| $\overline{DS}$, Clock, $C_{IN}$ | | 25 | 40 | pF | |
| All other, $C_{IN}$ | | 10 | 15 | pF | |
| DATA BUS LEAKAGE in INPUT MODE | | | | | |
| $I_{DB}$ | | | 10 | μA | 0.4V ≤ $V_{IN}$ ≤ 5.25V |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 80 | 100 | mA | |
| $I_{DD}$ | | 40 | 70 | mA | |
| **A.C. CHARACTERISTICS** | | | | | $T_A$ = 25°C |
| DOT COUNTER CARRY | | | | | |
| frequency | 0.5 | | 4.0 | MHz | Figure 1 |
| $PW_H$ | 35 | | | ns | Figure 1 |
| $PW_L$ | 215 | | | ns | Figure 1 |
| $t_r$, $t_f$ | | 10 | 50 | ns | Figure 1 |
| DATA STROBE | | | | | |
| $PW_{\overline{DS}}$ | 150ns | | 10μs | | Figure 2 |
| ADDRESS, CHIP SELECT | | | | | |
| Set-up time | 125 | | | ns | Figure 2 |
| Hold time | 50 | | | ns | Figure 2 |
| DATA BUS—LOADING | | | | | |
| Set-up time | 125 | | | ns | Figure 2 |
| Hold time | 75 | | | ns | Figure 2 |
| DATA BUS—READING | | | | | |
| $T_{DEL2}$ | | | 125 | ns | Figure 2, CL=50pF |
| $T_{DEL4}$ | 5 | | 60 | ns | Figure 2, CL=50pF |
| OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-$T_{DEL1}$ | | | 125 | ns | Figure 1, CL=20pF |
| OUTPUTS: RØ-3, DRØ-5 | | | | | |
| $T_{DEL3}$ | * | | 750 | ns | Figure 3, CL=20pF |

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

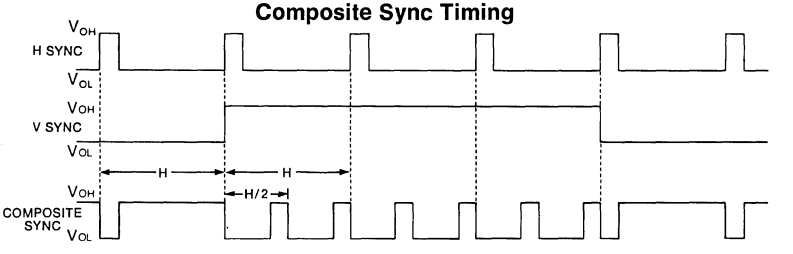
## Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

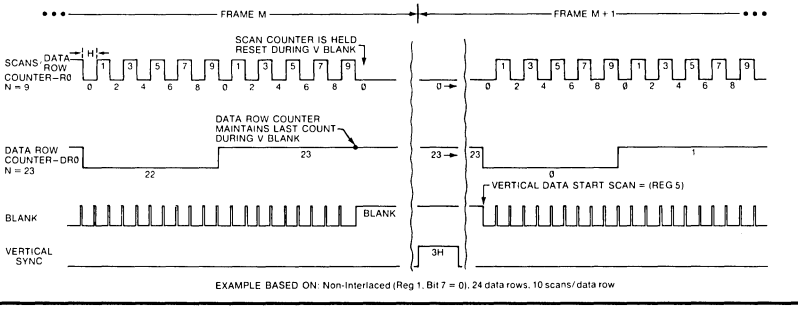
## General Timing




## Composite Sync Timing




## Vertical Sync Timing




EXAMPLE BASED ON: Non-Interlaced (Reg 1, Bit 7 = 0), 24 data rows, 10 scans/data row

## Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

| ADDRESS | | | | COMMAND |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | Start Timing Chain |
| 1 | 0 | 1 | 0 | Reset |
| 0 | 0 | 0 | 0 | Load Register 0 |
| | | • | | • |
| | | • | | • |
| | | • | | • |
| 0 | 1 | 1 | 0 | Load Register 6 |
| 1 | 1 | 1 | 0 | Start Timing Chain |

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037 or CRT 5057.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

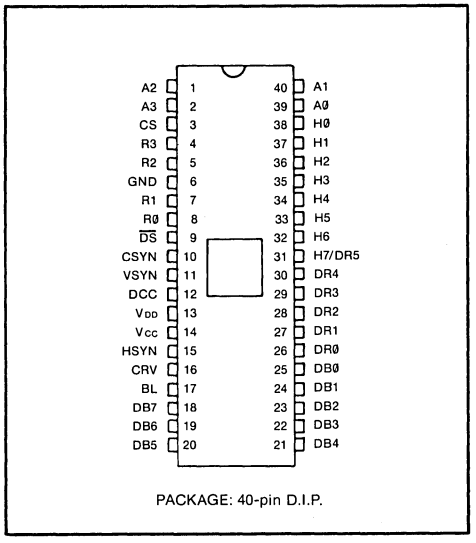
Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Preprogrammed CRT Video Timer and Controller VTAC®

## FEATURES

- ☐ Preprogrammed (Mask-Programmed) Display Format
  - 80 Characters Per Data Row
  - 24 Data Rows Per Frame
  - 9 Scan Lines Per Data Row
- ☐ Preprogrammed Monitor Sync Format
  - 262 Scan Lines Per Frame
  - 6 Character Times for Horizontal Front Porch
  - 8 Character Times for Horizontal Sync Width
  - 6 Character Times for Horizontal Back Porch
  - 16 Scan Lines for Vertical Front Porch
  - 3 Scan Lines for Vertical Sync Width
  - 27 Scan Lines for Vertical Back Porch
  - Non-Interlace
  - 15.720KHz Horizontal Scan Rate
  - 60Hz Frame Refresh Rate
- ☐ Fixed Character Rate
  - 1.572MHz Character Rate (636.13ns/Character)
  - 11.004MHz Dot Rate (90.88ns/Dot) for 7 Dot Wide Character Block
- ☐ Character Format
  - 5 X 7 Character in a 7 X 9 Block
- ☐ Compatible with CRT 8002B-003 VDAC™
- ☐ Compatible with CRT 7004B-003
- ☐ May be mask-programmed with other display formats

## PIN CONFIGURATION




PACKAGE: 40-pin D.I.P.

SECTION V

## GENERAL DESCRIPTION

The two chip combination of SMC's CRT 5047 and CRT 8002B-003 effectively provide all of the video electronics for a CRT terminal. This chip set along with a μC form the basis for a minimum chip count CRT terminal.

The CRT 5047 Video Timer and Controller is a special version of the CRT 5037 VTAC® which has been ROM-programmed with a fixed format. It is especially effective for low-cost CRT terminals using an 80 X 24 display format with a 5 X 7 character matrix. The use of a fixed ROM program in the CRT 5047 eliminates the software overhead normally required to specify the display parameters and simplifies terminal software design.

The Cursor Character Address Register and the Cursor Row Address Register are the only two registers accessible by the processor. The CRT 5047 is easily initialized by the following sequence of commands:

Reset  Load Control Register 6  Start Timing Chain

The parameters of the CRT 5047 have been selected to be compatible with most CRT monitors. The horizontal timing is programmed so that when the two character skew delay of the CRT 8002 VDAC™ is taken into account, the effective timing is: Horizontal Front Porch—four characters, and Horizontal Back Porch—eight characters.

Figure 1 shows the contents of the internal CRT 5047 registers. Other mask-programmed versions of the CRT 5037 are available. Consult SMC for more information.

## VTAC® WORK SHEET

1. H CHARACTER MATRIX (No. of Dots): . 5
2. V CHARACTER MATRIX (No. of Horiz. Scan Lines): ..... 7
3. H CHARACTER BLOCK (Step 1 + Desired Horiz. Spacing = No. in Dots): .. 7
4. V CHARACTER BLOCK (Step 2 + Desired Vertical Spacing = No. in Horiz. Scan Lines): ..... 9
5. VERTICAL FRAME (REFRESH) RATE (Freq. in Hz): ..... 60
6. DESIRED NO. OF DATA ROWS: ..... 24
7. TOTAL NO. OF ACTIVE "VIDEO DISPLAY" SCAN LINES (Step 4 x Step 6 = No. in Horiz. Scan Lines): ..... 216
8. VERT. SYNC DELAY (No. in Horiz. Scan Lines): ..... 16
9. VERT. SYNC (No. in Horiz. Scan Lines; T= 190.8 μs*): ..... 3
10. VERT. SCAN DELAY (No. in Horiz. Scan Lines; T= 1.718 ms*): ..... 27
11. TOTAL VERTICAL FRAME (Add steps 7 thru 10 = No. in Horiz. Scan Lines): ... 262
12. HORIZONTAL SCAN LINE RATE (Step 5 x Step 11 = Freq. in KHz): ..... 15.720
13. DESIRED NO. OF CHARACTERS PER HORIZ. ROW: ..... 80
14. HORIZ. SYNC DELAY (No. in Character Time Units; T = 3.817 μs**): ..... 6
15. HORIZ. SYNC (No. in Character Time Units; T = 5.090 μs**): ..... 8
16. HORIZ. SCAN DELAY (No. in Character Time Units; T = 3.817 μs**): ..... 6
17. TOTAL CHARACTER TIME UNITS IN (1) HORIZ. SCAN LINE (Add Steps 13 thru 16): ..... 100
18. CHARACTER RATE (Step 12 x Step 17 = Freq. in MHz): ..... 1.572
19. CLOCK (DOT) RATE (Step 3 x Step 18 = Freq. in MHz): ..... 11.004

*Vertical Interval **Horizontal Interval

| REG. # | ADDRESS A3 A0 | FUNCTION | BIT ASSIGNMENT | HEX. | DEC. |
|---|---|---|---|---|---|
| 0 | 0000 | HORIZ. LINE COUNT 100 | 0 1 1 0 0 0 1 1 | 63 | 99 |
| 1 | 0001 | INTERLACE 0<br>H SYNC WIDTH 8<br>H SYNC DELAY 6 | 0 1 0 0 0 1 1 0 | 46 | 70 |
| 2 | 0010 | SCANS/DATA ROW 9<br>CHARACTERS/ROW 80 | X 1 0 0 0 1 0 1 | 45 | 69 |
| 3 | 0011 | SKEW CHARACTERS 0,0<br>DATA ROWS 24 | 0 0 0 1 0 1 1 1 | 17 | 23 |
| 4 | 0100 | SCANS/FRAME 262<br>X = 3 | 0 0 0 0 0 0 1 1 | 03 | 03 |
| 5 | 0101 | VERTICAL DATA START = 3 + VERTICAL SCAN DELAY:<br>SCAN DELAY 27<br>DATA START 30 | 0 0 0 1 1 1 1 0 | 1E | 30 |
| 6* | 0110 | LAST DISPLAYED DATA ROW (= DATA ROWS) | X X | – | – |

*Register 6 has an initialization option. It is loaded with the data contained in Register 3 by a "Load Register 6" command. The "Up Scroll" command can be used to effect scrolling operations.

**Figure 1: CRT 5047 Mask Programmed Registers**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 · TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

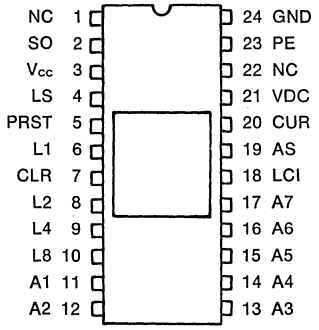
# Dot Matrix Character Generator

**128 Characters of 7 × 11 Bits**

## FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 7004A 20MHz
    - CRT 7004B 15MHz
    - CRT 7004C 10MHz
    - Access time 400ns
- ☐ No descender circuitry required
- ☐ On chip cursor
- ☐ On chip character address buffer
- ☐ On chip line address buffer
- ☐ Single +5 volt power supply
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM
- ☐ Compatible with CRT 5027 VTAC®
- ☐ Enhanced version of CG5004L-1

## PIN CONFIGURATION




PACKAGE: 24-Pin D.I.P.

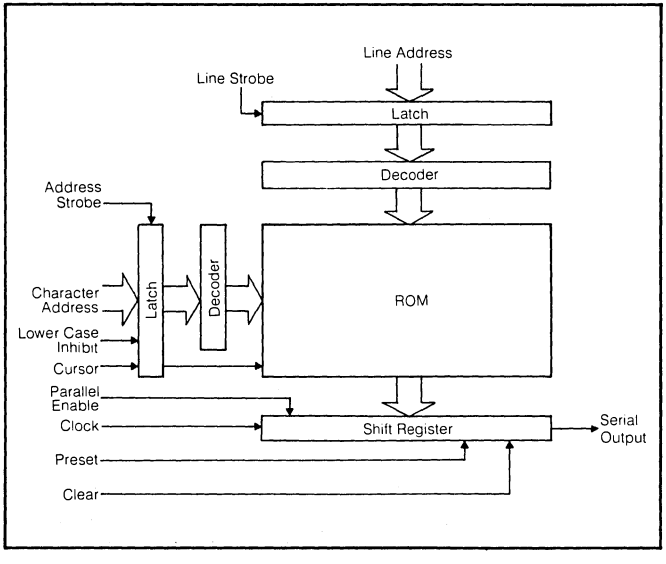
SECTION V

## GENERAL DESCRIPTION

SMC's CRT 7004 is a high speed character generator with a high speed video shift register designed to display 128 characters in a 7 x 11 dot matrix. The CRT 7004 is an enhanced, pin for pin compatible, version of SMC's CG5004L-1. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply. This process permits reduction of turn-around time for ROM patterns.

The CRT 7004 is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

## FUNCTIONAL BLOCK DIAGRAM



**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

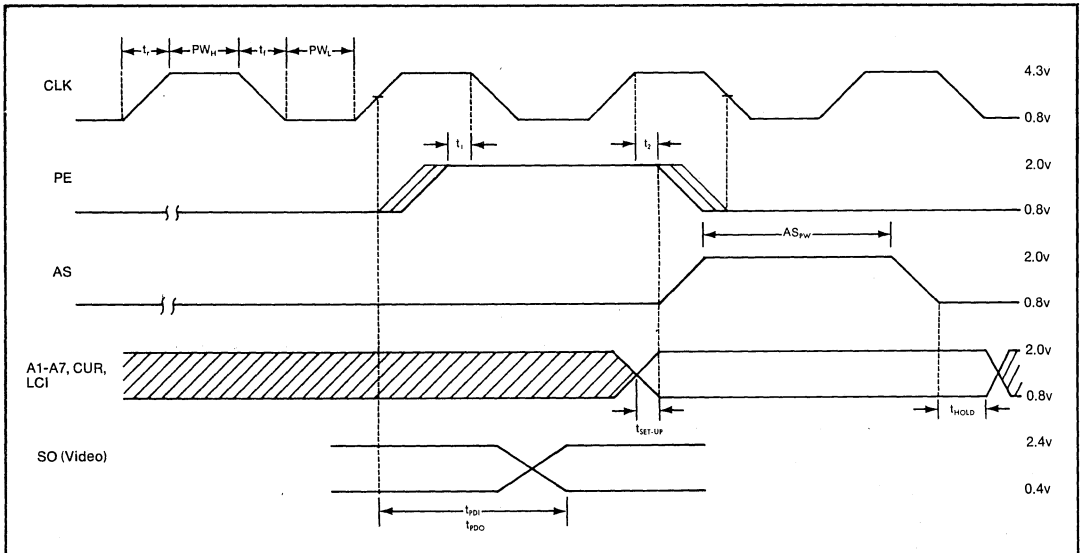
**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | excluding VDC |
| High-level, $V_{IH}$ | 2.0 | | | V | excluding VDC |
| INPUT VOLTAGE LEVELS-CLOCK | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 4.3 | | | V | See AC Timing Diagram |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=0.4 mA, 74LSXX load |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH}$=−20μA |
| INPUT CURRENT | | | | | |
| Leakage, $I_L$ | | | 100 | μA | $V_{IN}$ = O, LS, AS, A1-A7, Cursor LCI |
| | | | 10 | μA | $O \leq V_{IN} \leq V_{CC}$, All others |
| INPUT CAPACITANCE | | | | | |
| Data | | 10 | | pF | @ 1 MHz |
| PE | | 20 | | pF | @ 1 MHz |
| CLOCK | | 25 | | pF | @ 1 MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 100 | | mA | |

| SYMBOL | PARAMETER | CRT 7004A | | CRT 7004B | | CRT 7004C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| VDC | Video Dot Clock Frequency | 1.0 | 20 | 1.0 | 15 | 1.0 | 10 | MHz |
| $PW_H$ | VDC — High Time | 13.5 | | 21 | | 36 | | ns |
| $PW_L$ | VDC — Low Time | 13.5 | | 21 | | 36 | | ns |
| $t_{CY}AS$ | Address strobe to PE high | 400 | | 533 | | 800 | | ns |
| $t_{CY}LS$ | Line strobe to PE high | 1.0 | | 1.0 | | 1.0 | | μs |
| $t_r$, $t_f$ | Rise, fall time | | 10 | | 10 | | 10 | ns |
| $t_1$ | PE set-up time | 5 | | 20 | | 20 | | ns |
| $t_2$ | PE hold time | 15 | | 15 | | 15 | | ns |
| $AS_{PW}$ | Address strobe pulse width | 50 | | 50 | | 50 | | ns |
| $LS_{PW}$ | Line strobe pulse width | 50 | | 50 | | 50 | | ns |
| $t_{SET-UP}$ | Input set-up time | ≥0 | | ≥0 | | ≥0 | | ns |
| $t_{HOLD}$ | Input hold time | 15 | | 15 | | 15 | | ns |
| $t_{Pd1}$, $t_{Pd0}$ | Output propagation delay | | 45 | | 60 | | 90 | ns |

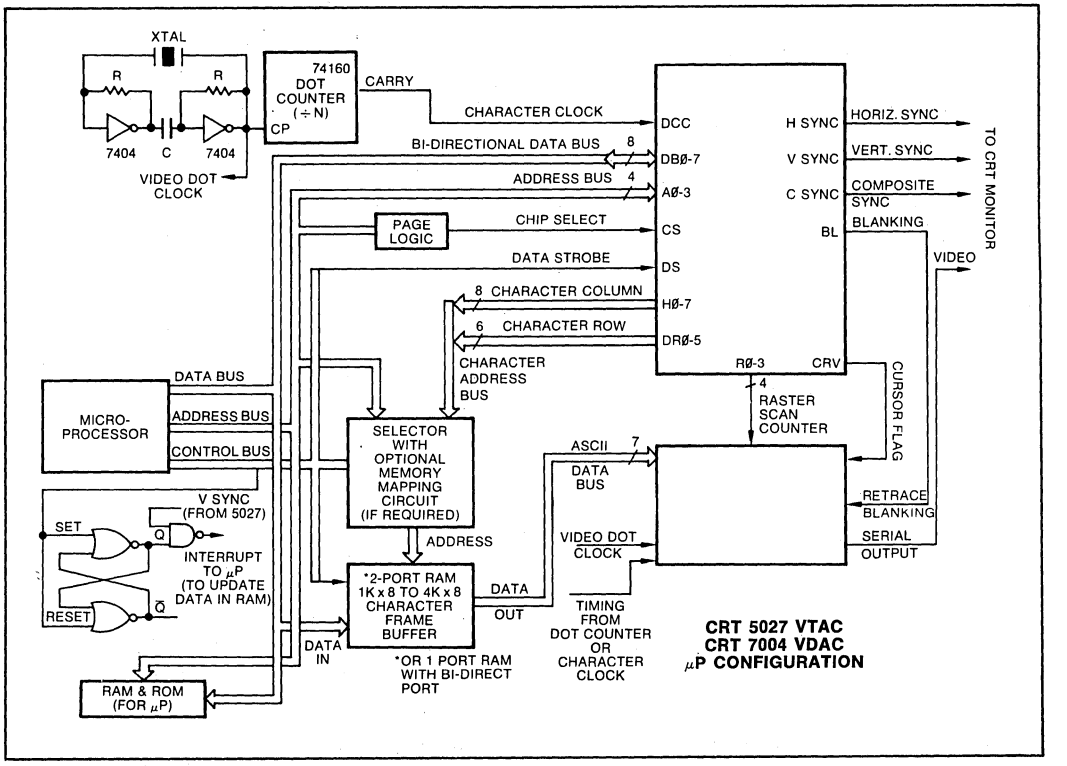
## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | NC | No Connection | |
| 2 | SO | Serial Output | The output of the dynamic shift register is clocked out on this pin. The serial input to this shift register is internally grounded; thus zeros are shifted in while data is shifted out. |
| 3 | $V_{CC}$ | Power Supply | +5 volt supply |
| 4 | LS | Line Strobe | A positive pulse on this input enters data from the L1, L2, L4, L8 lines into the line address holding register. The LS input may be left open, in which case it is pulled up to $V_{CC}$ by an internal resistor. Data on the L1 to L8 inputs is then entered directly into the register without any latching action. |
| 5 | PRST | Preset | A high level on this input forces the last stage of the shift register and the serial output to a logic high. |
| 6,8,9,10 | L1, L2, L4, L8 | Line Address | A binary number N, on these four inputs address the Nth line of the character font for N = 1—11. If lines 0, 12, 13, 14 or 15 are addressed, the parallel inputs to the shift register are all forced low. |
| 7 | CLR | Clear | A high level on this input forces the last stage of the shift register and the serial output to a logic low and will be latched (for a character time) by PE. Clear overrides preset. |
| 11-17 | A1-A7 | Character Address | The seven-bit word on these inputs is decoded internally to address one of the 128 available characters. |
| 18 | LCI | Lower Case Inhibit | A high level on this input transforms the address of a lower case character into that of the equivalent upper case character. This is internally achieved by forcing A6 low whenever A7 and LCI are high. |
| 19 | AS | Address Strobe | A positive pulse on this input enters data from the A1-A7, LCI and CUR inputs into the holding register. The AS input may be left open, in which case it is pulled up to $V_{CC}$ by an internal resistor. The data on the A1-A7, LCI and CUR inputs is then entered directly into the register without any latching action. |
| 20 | CUR | Cursor* | A high level on this input causes the cursor pattern to be superimposed on the pattern of the character addressed, i.e., the two patterns are OR-ed to generate the parallel inputs to the shift register. The standard cursor is presented as a double underscore on rows 10 and 11. |
| 21 | CLK | Clock | Frequency at which video (SO) is shifted. |
| 22 | NC | No Connection | |
| 23 | PE | Parallel Enable | A high level on this input loads the word at the output of the ROM into the shift register. The PE input must then be brought low again to allow the shift register to clock out this word. |
| 24 | GND | Ground | Ground |



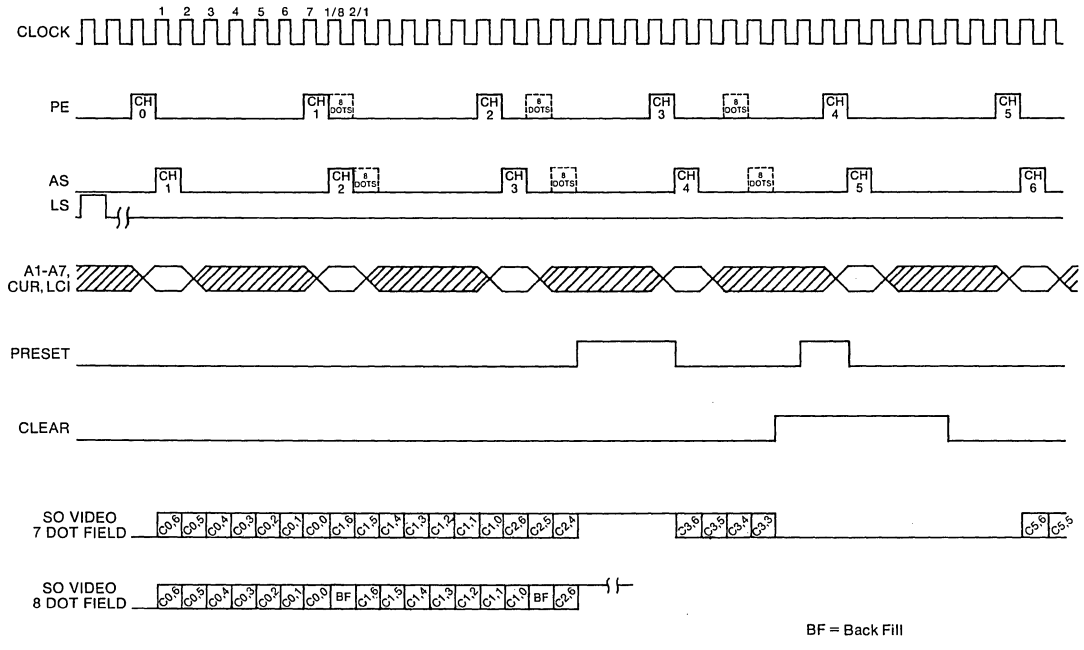

**AC TIMING DIAGRAM**

SECTION V

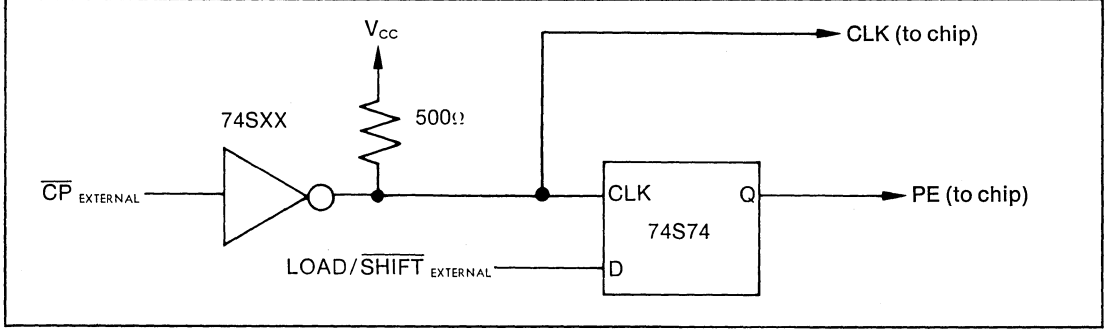



| A4..A1 / A7..A5 | 0000 C6...C0 | 0001 C6...C0 | 0010 C6...C0 | 0011 C6...C0 | 0100 C6...C0 | 0101 C6...C0 | 0110 C6...C0 | 0111 C6...C0 | 1000 C6...C0 | 1001 C6...C0 | 1010 C6...C0 | 1011 C6...C0 | 1100 C6...C0 | 1101 C6...C0 | 1110 C6...C0 | 1111 C6...C0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 R1–R11 | | | | | | | | | | | | | | | | |
| 001 R1–R11 | | | | | | | | | | | | | | | | |
| 010 R1–R11 | | | | | | | | | | | | | | | | |
| 011 R1–R11 | | | | | | | | | | | | | | | | |
| 100 R1–R11 | | | | | | | | | | | | | | | | |
| 101 R1–R11 | | | | | | | | | | | | | | | | |
| 110 R1–R11 | | | | | | | | | | | | | | | | |
| 111 R1–R11 | | | | | | | | | | | | | | | | |

*CONSULT FACTORY FOR CUSTOM FONT AND CURSOR OPTION.




**TYPICAL VIDEO OUTPUT**

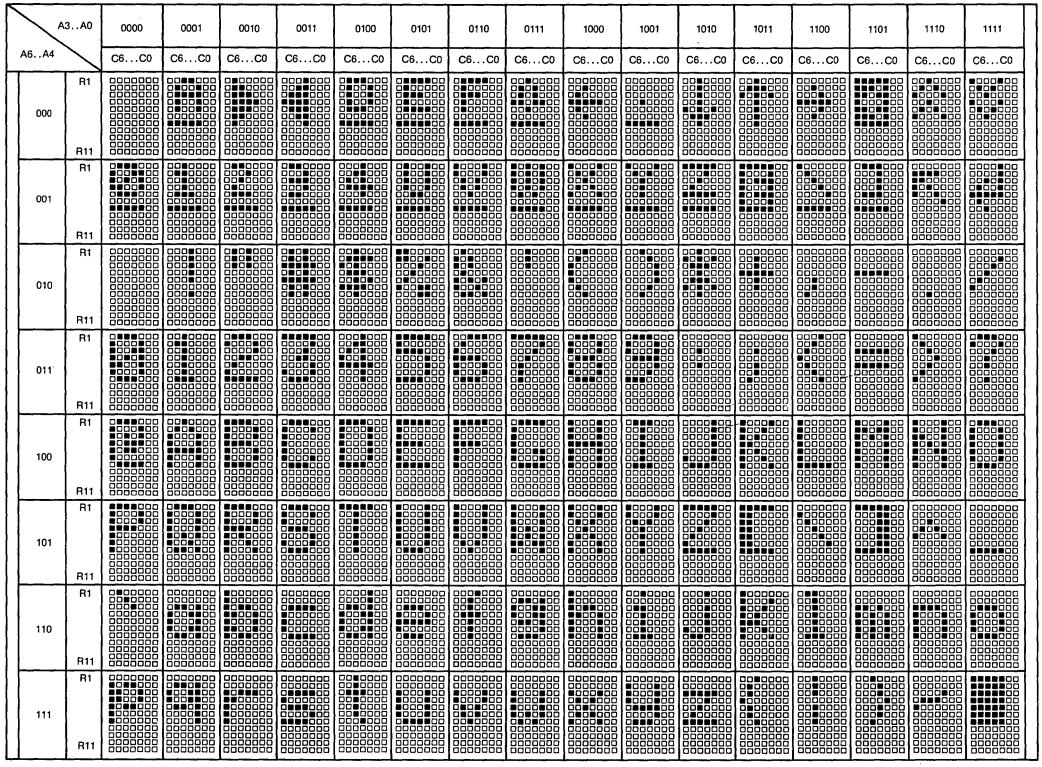



## NOTE

The differences between the CRT 7004 and CG5004L-1 are detailed below:

| CG5004L-1 | CRT 7004 |
|---|---|
| 1. If both the Preset and Clear inputs are brought high simultaneously the Serial Output is disabled and may be wire-ORed. | 1. Clear overrides Preset, no output disable is possible. |
| 2. All Inputs $V_{IH} = V_{CC} - 1.5v$ | 2. All inputs (except CLK) $V_{IH} = 2.0v$, min. CLK $V_{IH} = 4.3v$, min. |
| 3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.2mA$ | 3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.4mA$ 74LSXX load |
| 4. Shift Register is static | 4. Shift Register is dynamic |
| 5. Clear—directly forces the output low; when released, the output is determined by the state of the shift register output. | 5. Clear directly forces the output low and will be latched (for a character time) by PE. |
| 6. General Timing Differences—See Timing Diagram | 6. General Timing Differences—See Timing Diagram |

# Dot Matrix Character Generator




The Cursor for the CRT 7004-003 is presented as a double underscore on Rows 8 and 9.

STANDARD MICROSYSTEMS CORPORATION

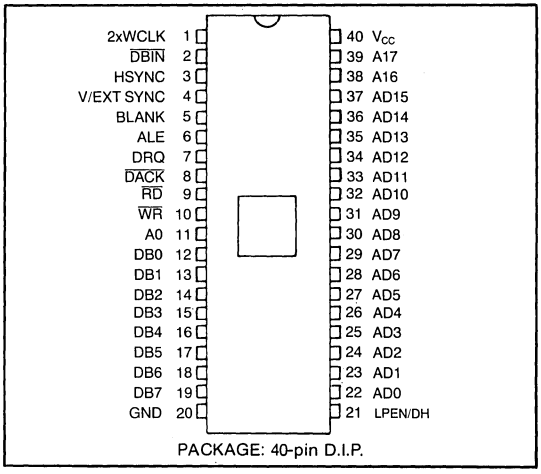
# CRT 7220A
# CRT 7220A-1
# CRT 7220A-2

# High-Performance Graphics Display Controller

## FEATURES

- ☐ Microprocesser Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles as fast as 500ns
  - Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode
  - Four megabit, bit-mapped display memory
- ☐ Character Mode
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Character Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities
  - Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100

## PIN CONFIGURATION




PACKAGE: 40-pin D.I.P.

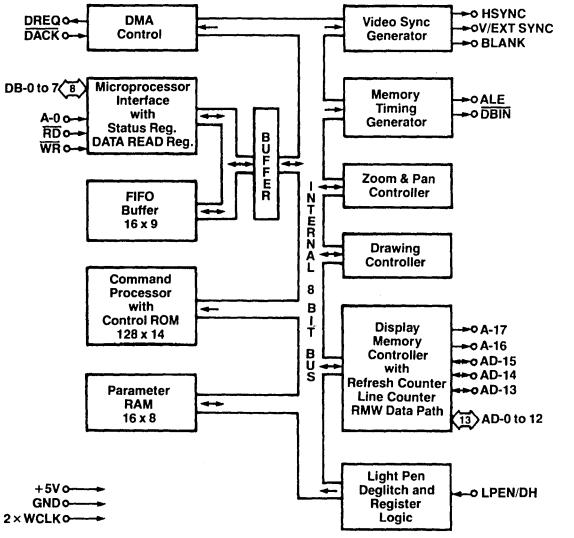
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
- ☐ Single +5 volt Power Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ DMA Capability
  - Bytes or word transfers
  - 4 clock periods per byte transferred

SECTION V

## GENERAL DESCRIPTION

The CRT 7220A High-performance Graphics Display Controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.




## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | IN/OUT | FUNCTION |
|---|---|---|---|
| 1 | 2XWCLK | IN | Clock Input |
| 2 | $\overline{DBIN}$ | OUT | Display Memory Read Input Flag |
| 3 | HSYNC | OUT | Horizontal Video Sync Output |
| 4 | V/EXTSYNC | IN/OUT | Vertical Video Sync Output or External VSYNC Input |
| 5 | BLANK | OUT | CRT Blanking Output |
| 6 | ALE ($\overline{RAS}$) | OUT | Address Latch Enable Output |
| 7 | DRQ | OUT | DMA Request Output |
| 8 | $\overline{DACK}$ | IN | DMA Acknowledge Input |
| 9 | $\overline{RD}$ | IN | Read Strobe Input for Microprocessor Interface |
| 10 | $\overline{WR}$ | IN | Write Strobe Input for Microprocessor Interface |
| 11 | A0 | IN | Address Select Input for Microprocessor Interface |
| 12-19 | DB0-DB7 | IN/OUT | Bidirectional data bus to Host Microprocessor |
| 20 | GND | — | Ground |
| 21 | LPEN/DH | IN | Light Pen Detect Input/Drawing Hold Input |
| 22-34 | AD0-AD12 | IN/OUT | Address and Data Lines to Display Memory |
| 35-37 | AD13-AD15 | IN/OUT | Character Mode: Line Counter Outputs, Bits 0-2<br>Mixed Mode: Address and Data Bits 13-15<br>Graphics Mode: Address and Data Bits 13-15 |
| 38 | A16 | OUT | Character Mode: Line Counter Output, Bit 3<br>Mixed Mode: Attribute Blink and Clear Line Counter Output<br>Graphics Mode: Address Bit 16 Output |
| 39 | A17 | OUT | Character Mode: Cursor Output and Line Counter Bit 4<br>Mixed Mode: Cursor and Bit Map Area Flag Output<br>Graphics Mode: Address Bit 17 Output |
| 40 | VCC | — | +5 Volt Power Supply |

## FUNCTIONAL DESCRIPTION

### Microprocessor Bus Interface

Control of the HGDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal HGDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

### Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the HGDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

### DMA Control

The DMA control circuitry in the HGDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

### Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

### Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple HGDC's.

### Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the HGDC's ALE and DBIN outputs.

### Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

### Drawing Controller

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

### Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

### Light Pen Deglitcher

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address. If this input is held high for a period greater than four 2xWCLK cycles, drawing execution is halted.

## PROGRAMMER'S VIEW OF HGDC

The HGDC occupies two addresses on the system microprocessor bus through which the HGDC's status register and FIFO are accessed. Commands and parameters are written into the HGDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

| A0 | READ | WRITE |
|---|---|---|
| 0 | Status Register | Parameter Into FIFO |
| 1 | FIFO Read | Command Into FIFO |

**HGDC Microprocessor Bus Interface Registers**

Commands to the HGDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate reigsters within the HGDC, and initiates the required operations.

The commands available in the HGDC can be organized into five categories as described in the following section.

## HGDC COMMAND SUMMARY

### Video Control Commands

1. RESET 1 Resets the HGDC to its idle state.
2. RESET 2 Resets the HGDC to its idle state. Does not resynchronize video timing. Blanks the display.
3. RESET 3 Resets the HGDC to its idle state. Does not resynchronize video timing. Does not blank the display.
4. SYNC Specifies the video display format.
5. VSYNC Selects master or slave video synchronization mode.
6. CCHAR Specifies the cursor and character row heights.

### Display Control Commands

1. START — Ends Idle mode and unblanks the display.
2. BLANK 1 — Controls the blanking and unblanking of the display, along with video resynchronization.
3. BLANK 2 — Controls the blanking and unblanking of the display. Does not blank the display.
4. ZOOM — Specifies zoom factors for the display and graphics characters writing.
5. CURS — Sets the position of the cursor in display memory.
6. PRAM — Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
7. PITCH — Specifies the width of the X dimension of display memory.

### Drawing Control Commands

1. WDAT — Writes data words or bytes into display memory.
2. MASK — Sets the mask register contents.
3. FIGS — Specifies the parameters for the drawing controller.
4. FIGD — Draws the figure as specified above.
5. GCHRD — Draws the graphics character into display memory.

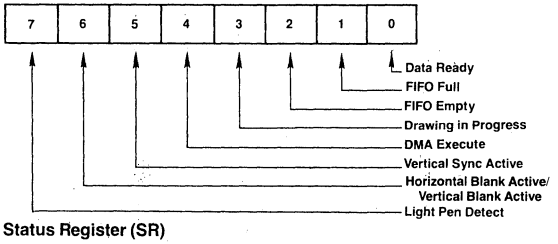
### Data Read Commands

1. RDAT: — Reads data words or bytes from display memory.
2. CURD: — Reads the cursor position.
3. LPRD: — Reads the light pen address.

### DMA Control Commands

1. DMAR — Requests a DMA read transfer.
2. DMAW — Requests a DMA write transfer.

### STATUS REGISTER FLAGS




Status Register (SR)

### SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

### SR-6: Horizontal Blanking Active/Vertical Blank Active

A 1 value for this flag signifies that horizontal retrace blanking or vertical retrace blanking is currently underway dependent on the status of the VH bit in SYNC or the RESETx parameter 6.

### SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

### SR-4: DMA Execute

This bit is a 1 during DMA data transfers.

### SR-3: Drawing in Progress

While the HGDC is drawing a graphics figure, this status bit is a 1.

### SR-2: FIFO Empty

This bit and the FIFO Full flag coordinate system microprocessor accesses with the HGDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the HGDC have been interpreted.

### SF-1: FIFO Full

A 1 at this flag indicates a full FIFO in the HGDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked out before each write into the HGDC.

### SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

## FIFO OPERATION & COMMAND PROTOCOL

The first-in, first-out buffer (FIFO) in the HGDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the HGDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the HGDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the HGDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the HGDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the HGDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the HGDC always put the FIFO into write mode if it wasn't in it already.

If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a HGDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the HGDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

## READ-MODIFY-WRITE CYCLE

Data transfers between the HGDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of

memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the HGDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

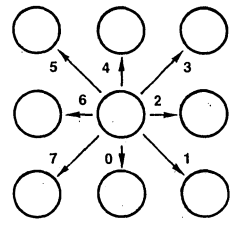
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern Register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

## FIGURE DRAWINGS

The HGDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 8MHz, this is equal to 500ns. During the RMW cycle the HGDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the HGDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the HGDC's internal RMW logic.

During the drawing process, the HGDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The HGDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.




Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

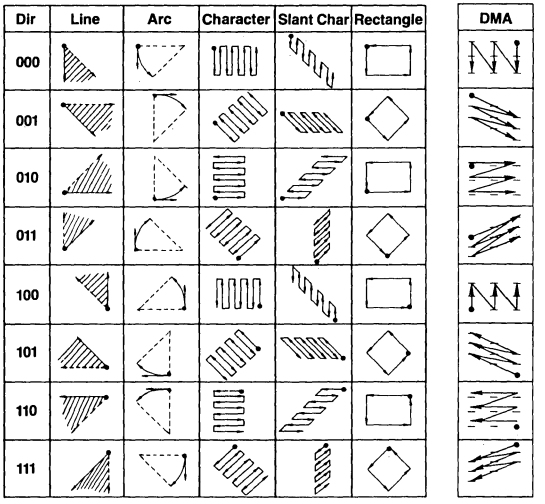
The table below summarizes these operations for each direction.

| Dir | Operations to Address the Next Pixel |
|---|---|
| 000 | EAD − P → EAD |
| 001 | EAD − P → EAD<br>dAD (MSB) = 1:EAD − 1 → EAD dAD → LR |
| 010 | dAD (MSB)1:EAD − 1 → EAD dAD → LR |
| 011 | EAD − P → EAD<br>dAD (MSB) = 1:EAD − 1 → EAD dAD → LR |
| 100 | EAD − P → EAD |
| 101 | EAD − P → EAD<br>dAD (LSB) = 1:EAD − 1 → EAD dAD → RR |
| 110 | dAD (LSB) = 1:EAD − 1 → EAD dAD → RR |
| 111 | EAD − P → EAD<br>dAD (LSB) = 1:EAD − 1 → EAD dAD → RR |

Where P = Pitch, LR = Left Rotate, RR = Right Rotate,
EAD = Execute Word Address, and
dAD = Dot Address stored in the Mask Register.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:




Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the HGDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

## DRAWING PARAMETERS

In preparation for graphics figure drawing, the HGDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the HGDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The HGDC Drawing Controller coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specified details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the HGDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

| Drawing Type | DC | D | D2 | D1 | DM |
|---|---|---|---|---|---|
| Initial Value* | 0 | 8 | 8 | −1 | −1 |
| Line | $\lvert\Delta I\rvert$ | $2\lvert\Delta D\rvert - \lvert\Delta I\rvert$ | $2(\lvert\Delta D\rvert - \lvert\Delta I\rvert)$ | $2\lvert\Delta D\rvert$ | − |
| Arc** | rsin $\phi$ | r−1 | 2(r−1) | −1 | rsin $\theta\downarrow$ |
| Rectangle | 3 | A−1 | B−1 | −1 | A−1 |
| Area Fill | B−1 | A | A | − | − |
| Graphic Character*** | B−1 | A | A | − | − |
| Read + Write Data | W−1 | − | − | − | − |
| DMAW | D−1 | C−1 | − | − | − |
| DMAR | D−1 | C−2 | (C−2)/2† | − | − |

**Notes:** All numbers are shown in base 10 for convenience. The HGDC accepts base 2 numbers (2s complement notation) where appropriate.

*Initial values for the various parameters remain as each drawing process ends.

**Circles are drawn with 8 arcs, each of which span 45°, so that $\sin\phi = 1/\sqrt{2}$ and $\sin\theta = 0$.

***Graphic characters are a special case of bit-map area filling in which B and A ≤ 8. If A = 8 there is no need to load D and D2.

Where:

−1= all ONES value.

−= No parameter bytes sent to GDC for this parameter.

ΔI= The larger at Δx or Δy.

ΔD= The smaller at Δx or Δy.

r= Radius of curvature, in pixels.

$\phi$= Angle from major axis to end of the arc. $\phi \leq 45°$

$\theta$= Angle from major axis to start of the arc. $\theta \leq 45°$

↑ = Round up to the next higher integer.

↓ = Round down to the next lower integer.

A= Number of pixels in the initially specified direction.

B= Number of pixels in the direction at right angles to the initially specified direction.

W= Number of words to be accessed.

C= Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)

D= Number of words to be accessed in the direction at right angles to the initially specified direction.

DC= Drawing count parameter which is one less than the number of RMW cycles to be executed.

DM= Dots masked from drawing during arc drawing.

†= Needed only for word reads.

## GRAPHICS CHARACTER DRAWING

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character display is loaded into the HGDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The HGDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the

drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is narrower than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the HGDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8).

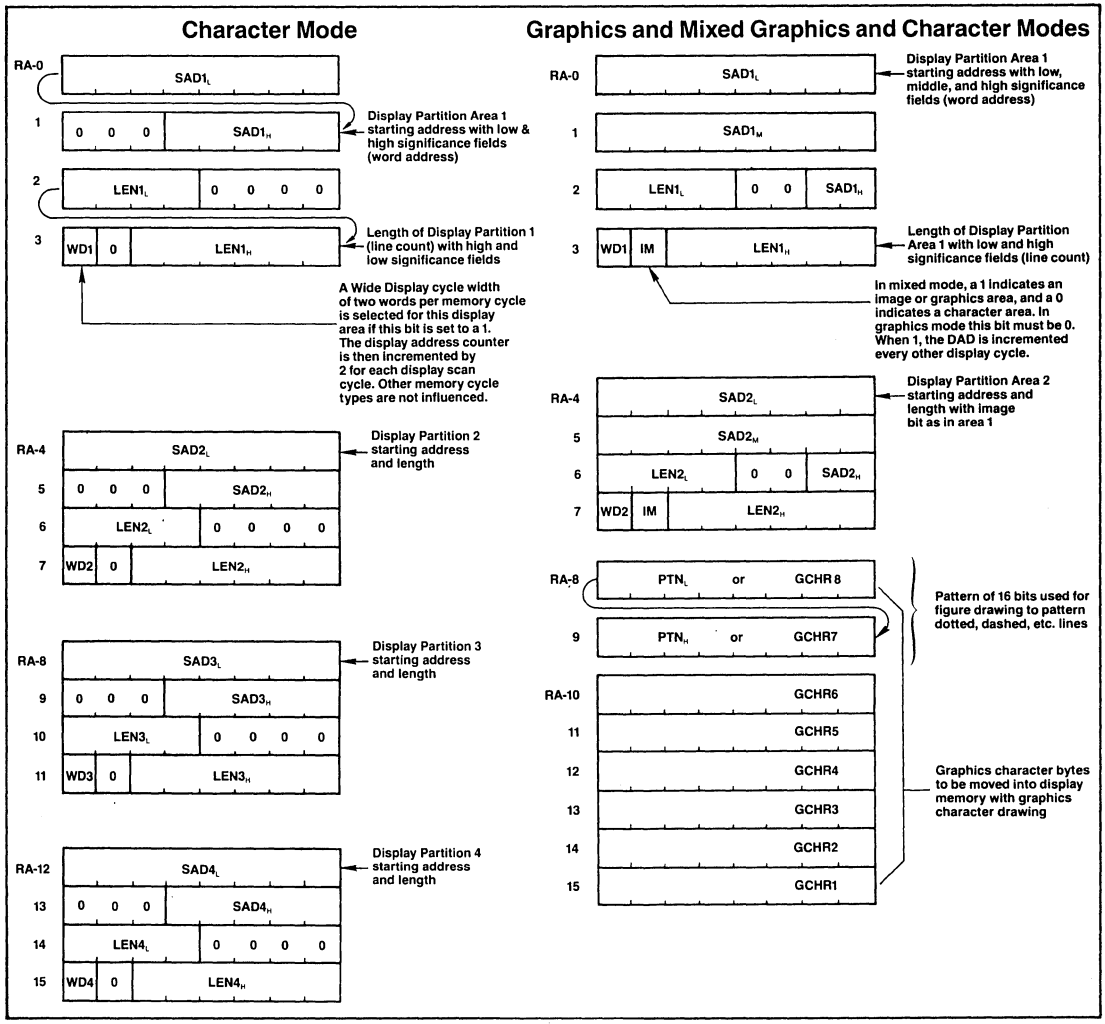
## PARAMETER RAM CONTENTS: RAM ADDRESS RA 0 TO 15

The parameters stored in the parameter RAM, PRAM, are available for the HGDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the HGDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

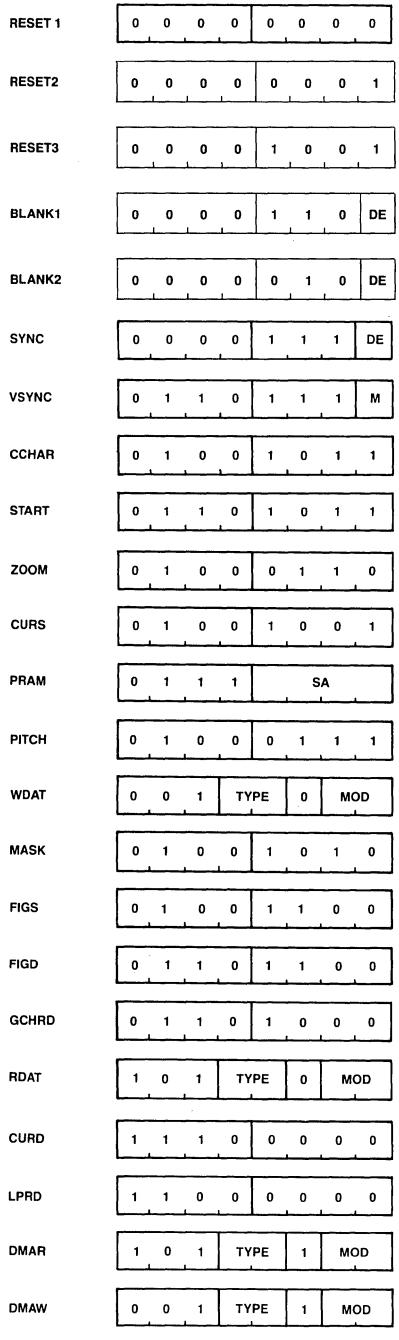
The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the HGDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

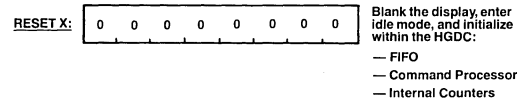


## Command Bytes Summary




## VIDEO CONTROL COMMANDS

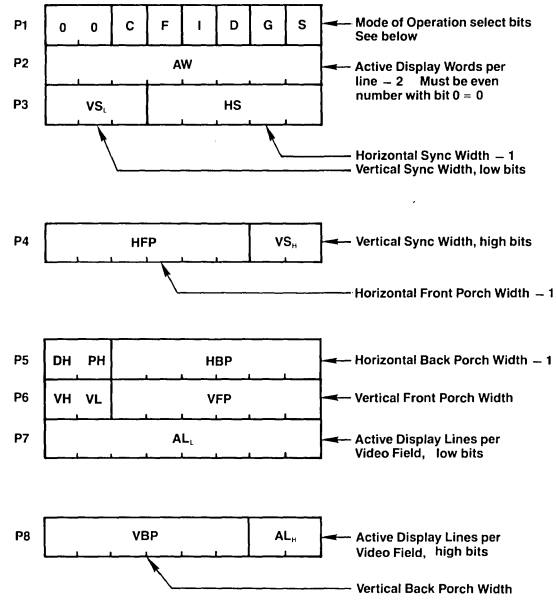
### Reset




This command can be executed at any time and does not modify any of the parameters already loaded into the HGDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.

RESET 1: Resync video timing in slave mode.
RESET 2: Blank the display and do not resync.
RESET 3: Unblank the display and do not resync.




In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to $2^n$ where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical intervals are counted in lines.

If the Drawing Hold (DH) is set to one, pin 21 (LPEN/DH) is used as the drawing hold control pin. When the input to LPEN/DH is held high for over four 2 x WCLK clocks, the drawing address output is temporarily held and the display address is output.

The HGDC allows an even or odd number of lines per frame. Selection is via the VL flag, the seventh bit of the sixth parameter byte following a RESET or SYNC command. When VL is 0, an odd number of display lines is generated.

| VL | Number of lines in interlaced mode |
|---|---|
| 0 | Odd, as in 7220 |
| 1 | Even |

When VH = 0, status operation is as in CRT 7220.

| VH | Blank Status Bit Definition |
|---|---|
| 0 | Status register bit 6 indicates Horizontal Blank |
| 1 | Status register bit 6 indicates Vertical Blank |

PH is the most significant bit (9) of the display pitch parameter. Use the PITCH command to set the lower eight bits.

## SYNC GENERATOR PERIOD CONSTRAINTS

### Horizontal Back Porch Constraints

1. In general:
   HBP≥3 Display Word Cycles (6 clock cycles).
2. If the Image bit or WD modes change within one video field:
   HBP≥5 Display Word Cycles (10 clock cycles).
3. If interlace, mixed mode, or split screen is used:
   HBP≥5 Display Word Cycles (10 clock cycles).

### Horizontal Front Porch Constraints

1. In general:
   HFP≥2 Display Word Cycles (4 clock cycles).
2. If the HGDC is used in the video sync Slave mode:
   HFP≥4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP≥6 Display Word Cycles (12 clock cycles).
4. If interlace mode, DMA, or ZOOM is used:
   HFP≥3 Display Word Cycles (6 clock cycles).

### Horizontal SYNC Constraints

1. If interlaced display mode is used:
   HS≥5 Display Word Cycles (10 clock cycles).
2. If DRAM Refresh is enabled:
   HS≥2 Display Word Cycles (4 clock cycles).

### Modes of Operation Bits

| C | G | Display Mode |
|---|---|---|
| 0 | 0 | Mixed Graphics & Character |
| 0 | 1 | Graphics Mode |
| 1 | 0 | Character Mode |
| 1 | 1 | Invalid |

| I | S | Video Framing |
|---|---|---|
| 0 | 0 | Noninterlaced |
| 0 | 1 | Invalid |
| 1 | 0 | Interlaced Repeat Field for Character Displays |
| 1 | 1 | Interlaced |

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.

Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.

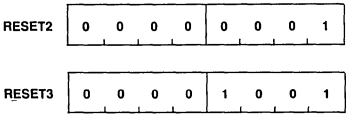
Noninterlaced Framing: 1 field brings all of the information to the screen.

| D | Dynamic RAM Refresh Cycles Enable |
|---|---|
| 0 | No Refresh — STATIC RAM |
| 1 | Refresh — Dynamic RAM |

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

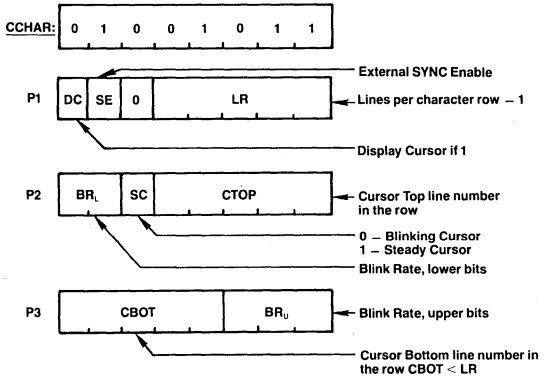
| F | Drawing Time Window |
|---|---|
| 0 | Drawing during active display time and retrace blanking |
| 1 | Drawing only during retrace blanking |

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.




Both commands allow a reset while presenting reinitialization of the internal sync generator by an external sync source (slave mode).

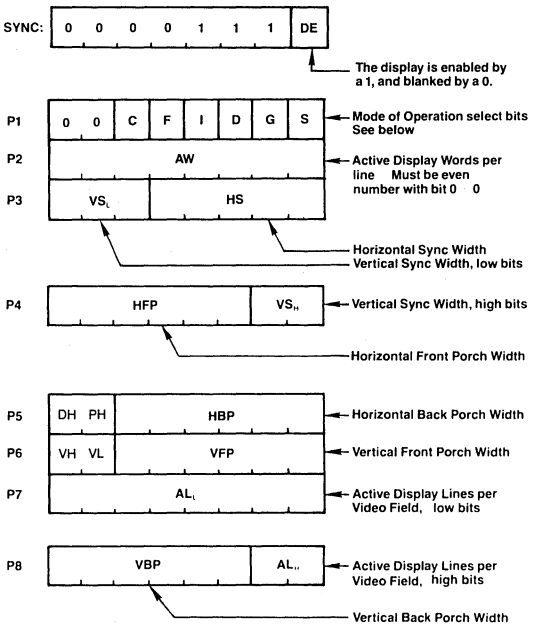
### Cursor & Character Characteristics




In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on -¼ off duty cycle. All three parameter bytes must be output for interlace displays, regardless of mode. For interlace displays in graphics mode, the parameter $BR_L$ = 3.

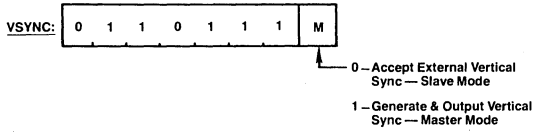
When SE = 0, the HGDC, in slave mode, detects the falling edge of EX. SYNC on the first frame. When SE = 1, the HGDC, in slave mode, detects the falling edge of EX. SYNC on every frame.

## SYNC Format Specify




This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The HGDC is not reset nor does it enter idle mode.

## Vertical Sync Mode



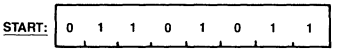

When using two or more HGDCs to contribute to one image, one HGDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all HGDCs are connected together.

A few considerations should be observed when synchronizing two or more HGDCs to generate overlayed video via the V/EXT SYNC pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave HGDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave HGDC to complete the operation before the start of the HSYNC interval.

Once the HGDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master HGDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

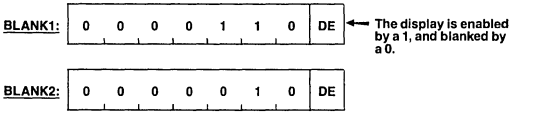
# DISPLAY CONTROL COMMANDS

## Start Display & End Idle Mode



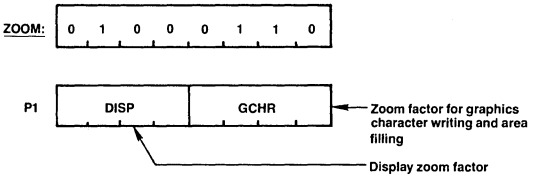

The START command generates the video signals as specified by the RESETX or SYNC command.

## Display Blanking Control



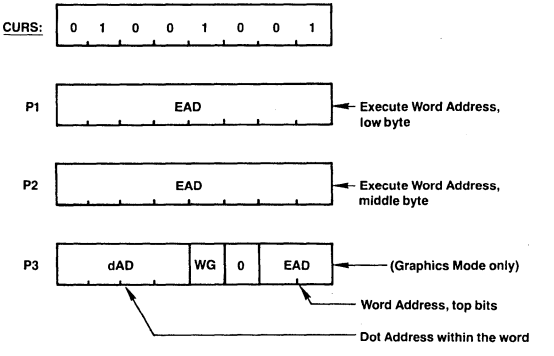

BLANK 2 does not cause the resyncing of an HGDC in slave mode. BLANK 1 does cause the resyncing of an HGDC in slave mode.

## Zoom Factors Specify




Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

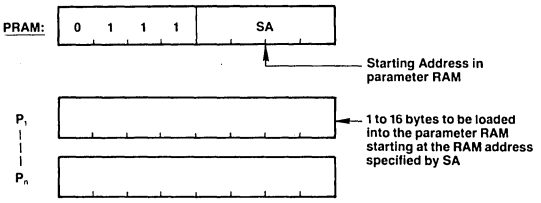
## Cursor Position Specify




In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

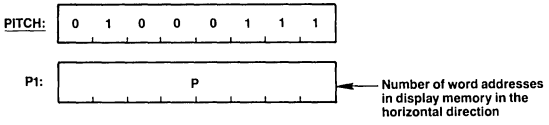
When the WG bit is set to one, any data following the WDAT command is written as is. When the WG bit is set to zero, the 7220A performs as the 7220 does: The pattern written is determined by the least significant bit of each parameter byte following the WDAT command. This bit is expanded into 16 identical bits which form the pattern.

## Parameter RAM Load




From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

## Pitch Specification

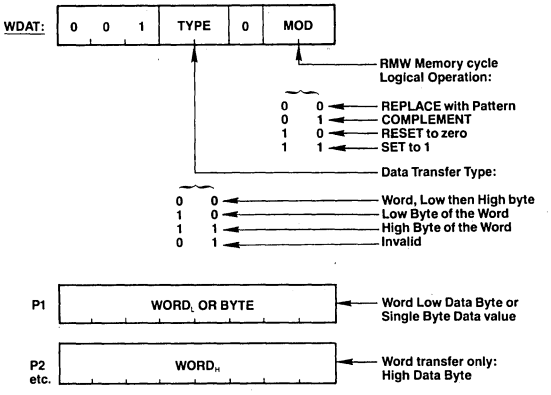



This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.

# DRAWING CONTROL COMMANDS

## Write Data into Display Memory



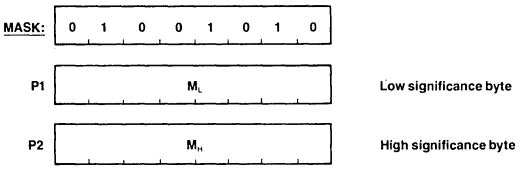

Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. If the WG bit of the third parameter of the CURS command is set to one, any byte following the WDAT command is written as is. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need to be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter + 1 will be the number of RMW cycles done by the HGDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.

## Mask Register Load




This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

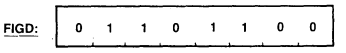
The Mask register is loaded by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 to 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all "ONES" for any "word-at-a-time" operation.

## Valid Figure Type Select Combinations

| SL | R | A | GC | L | Operation |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT |
| 0 | 0 | 0 | 0 | 1 | Straight Line Drawing |
| 0 | 0 | 0 | 1 | 0 | Graphics Character Drawing and Area filling with graphics character pattern |
| 0 | 0 | 1 | 0 | 0 | Arc and Circle Drawing |
| 0 | 1 | 0 | 0 | 0 | Rectangle Drawing |
| 1 | 0 | 0 | 1 | 0 | Slanted Grapnics Character Drawing and Slanted Area Filling |

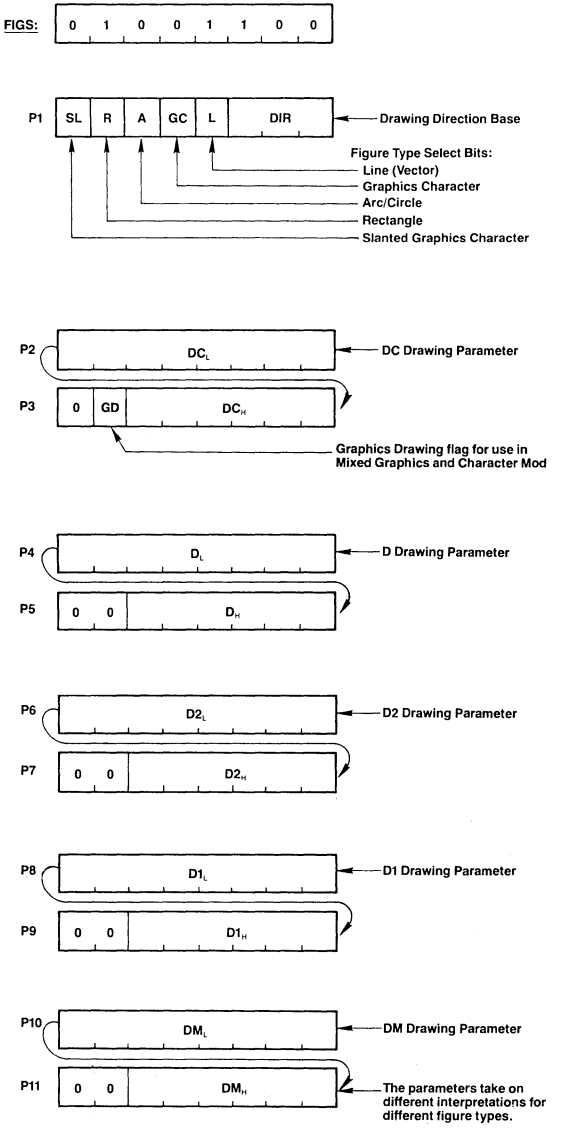
Only these bit combinations assure correct drawing operation.

## Figure Draw Start

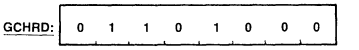



On execution of this instruction, the HGDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

## Figure Drawing Parameters Specify



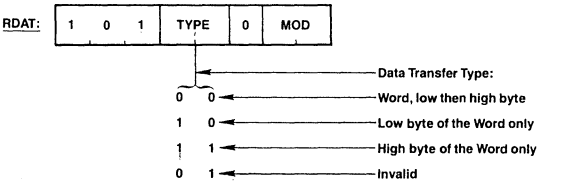

## Graphics Character Draw and Area Filling Start




Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

# DATA READ COMMANDS

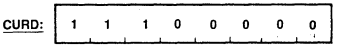
## Read Data from Display Memory



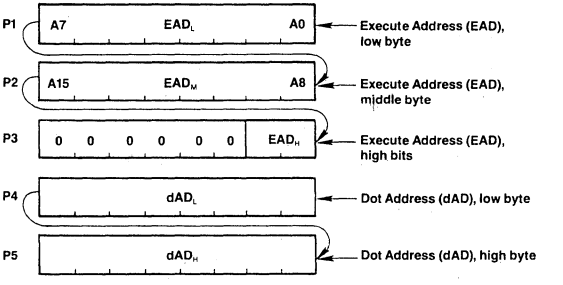

Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the HGDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

## Cursor Address Read



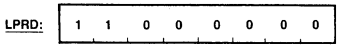

The following bytes are returned by the HGDC through the FIFO:



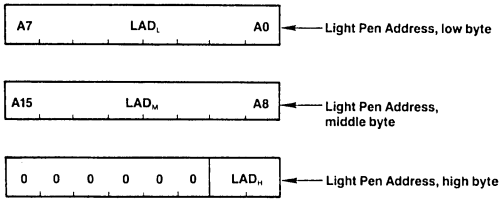

The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

## Light Pen Address Read




The following bytes are returned by the HGDC through the FIFO:

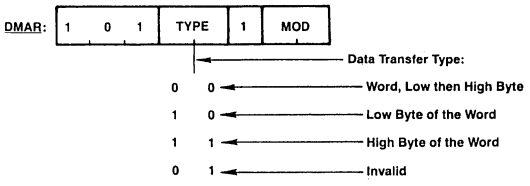



The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

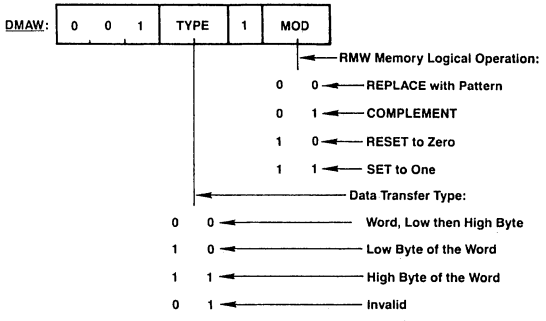
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

# DMA CONTROL COMMANDS

## DMA Read Request




## DMA Write Request



## ELECTRICAL CHARACTERISTICS

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

### ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Ambient Temperature under Bias | 0°C to 70°C |
| Storage Temperature | −65°C to 150°C |
| Voltage on Any Pin with Respect to Ground | −0.5V to +7V |
| Power Dissipation | 1.5 W |

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS $T_a$ = 0°C to 70°C; $V_{CC}$ = 5V ± 10%; GND = 0V

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | −0.5 | | 0.8 | V | ① |
| Input High Voltage | $V_{IH}$ | 2.2 | | $V_{CC}$ + 0.5 | V | ②③ |
| Output Low Voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 2.2 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −400 µA |
| Input Low Leak Current (except VSYNC, $\overline{DACK}$) | $I_{IL}$ | | | −10 | µA | $V_I$ = 0V |
| Input Low Leak Current (VSYNC, $\overline{DACK}$) | $I_{IL}$ | | | −500 | µA | |
| Input High Leak Current (except LPEN/DH) | $I_{IH}$ | | | +10 | µA | $V_I$ = $V_{CC}$ |
| Input High Leak Current (LPEN/DH) | $I_{IH}$ | | | +500 | µA | |
| Output Low Leak Current | $I_{OL}$ | | | −10 | µA | $V_O$ = 0V |
| Output High Leak Current | $I_{OH}$ | | | −10 | µA | $V_O$ = $V_{CC}$ |
| Clock Input Low Voltage | $V_{CL}$ | −0.5 | | 0.6 | V | |
| Clock Input High Voltage | $V_{CH}$ | 3.5 | | $V_{CC}$ − 1.0 | V | |
| $V_{CC}$ Supply Current | $I_{CC}$ | | | 270 | mA | |

### CAPACITANCE $T_a$ = 25°C; $V_{CC}$ = GND = 0V

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 10 | pF | fc = 1 MHz |
| I/O Capacitance | $C_{I/O}$ | | | 20 | pF | $V_I$ (unmeasured) = 0V |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |
| Clock Input Capacitance | Cf | | | 20 | pF | |

**Notes:**
① For 2XWCLK, $V_{IL}$ = −0.5V to +0.6V. ② For 2XWCLK, $V_{IH}$ = +3.9V to $V_{CC}$ + 1.0V. ③ For $\overline{WR}$, $V_{IH}$ = 2.5V to $V_{CC}$ + 0.5V.

### AC Characteristics, $T_a$ = 0°C to 70°C; $V_{CC}$ = 5.0V ± 10%; GND = 0V

**Read Cycle (HGDC↔CPU)**

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Address Setup to $\overline{RD}$ ↓ | $t_{AR}$ | 0 | | 0 | | 0 | | ns | |
| Address Hold from $\overline{RD}$ ↑ | $t_{RA}$ | 0 | | 0 | | 0 | | ns | |
| $\overline{RD}$ Pulse Width | $t_{RR1}$ | $t_{RD1}$ + 20 | $t_{RCY}$-½ $t_{CLK}$ | $t_{RD1}$ + 20 | $t_{RCY}$-½$t_{CLK}$ | $t_{RD1}$ + 20 | $t_{RCY}$-½$t_{CLK}$ | ns | |
| Data Delay from $\overline{RD}$ ↓ | $t_{RD1}$ | | 75 | | 65 | | 55 | ns | $C_L$ = 50 pF |
| Data Floating from $\overline{RD}$ ↑ | $t_{DF}$ | 0 | 75 | 0 | 65 | 0 | 55 | ns | |
| $\overline{RD}$ Pulse Cycle | $t_{RCY}$ | 4 $t_{CLK}$ | | 4 $t_{CLK}$ | | 4 $t_{CLK}$ | | ns | |

**Write Cycle (HGDC↔CPU)**

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Address Setup to $\overline{WR}$ ↓ | $t_{AW}$ | 0 | | 0 | | 0 | | ns | |
| Address Hold from $\overline{WR}$ ↑ | $t_{WA}$ | 10 | | 10 | | 10 | | ns | |
| $\overline{WR}$ Pulse Width | $t_{WW}$ | 80 | $t_{WCY}$ − $t_{CLK}$ | 70 | $t_{WCY}$ − $t_{CLK}$ | 60 | $t_{WCY}$ − $t_{CLK}$ | ns | |
| Data Setup to $\overline{WR}$↑ | $t_{DW}$ | 65 | | 55 | | 45 | | ns | |
| Data Hold from $\overline{WR}$ | $t_{WD}$ | 10 | | 10 | | 10 | | ns | |
| $\overline{WR}$ Pulse Cycle | $t_{WCY}$ | 4 $t_{CLK}$ | | 4 $t_{CLK}$ | | 4 $t_{CLK}$ | | ns | |

## DMA Read Cycle (HGDC↔CPU)

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| DACK Setup to $\overline{RD}$ ↓ | $t_{KR}$ | 0 | | 0 | | 0 | | ns | |
| DACK Hold from $\overline{RD}$ ↑ | $t_{RK}$ | 0 | | 0 | | 0 | | ns | |
| $\overline{RD}$ Pulse Width | $t_{RR2}$ | $t_{RD2}$ + 20 | | $t_{RD2}$ + 20 | | $t_{RD2}$ + 20 | | ns | |
| Data Delay from $\overline{RD}$ ↓ | $t_{RD2}$ | | 1.5 $t_{CLK}$ + 80 | | 1.5 $t_{CLK}$ + 70 | | 1.5 $t_{CLK}$ + 60 | ns | $C_L$ = 50 pF |
| DREQ Delay from 2XWCLK ↑ | $t_{REQ}$ | | 100 | | 85 | | 75 | ns | $C_L$ = 50 pF |
| DREQ Setup to $\overline{DACK}$ ↓ | $t_{QK}$ | 0 | | 0 | | 0 | | ns | |
| $\overline{DACK}$ High Level Width | $t_{DK}$ | $t_{CLK}$ | | $t_{CLK}$ | | $t_{CLK}$ | | ns | |
| $\overline{DACK}$ Pulse Cycle | $t_E$ | 4 $t_{CLK}$* | | 4 $t_{CLK}$* | | 4 $t_{CLK}$* | | ns | |
| DREQ ↓ Delay from $\overline{DACK}$ ↓ | $t_{KQ(R)}$ | | $t_{CLK}$ + 100 | | $t_{CLK}$ + 90 | | $t_{CLK}$ + 80 | ns | $C_L$ = 50 pF |
| $\overline{DACK}$ Low-level Width | $t_{LK}$ | 2$t_{CLK}$ | | 2$t_{CLK}$ | | 2$t_{CLK}$ | | ns | |

*for high byte and low byte transfers: $t_E = 5\ t_{CLK}$

## DMA Write Cycle (GDC↔CPU)

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| DACK Setup to WR ↓ | $t_{KW}$ | 0 | | 0 | | 0 | | ns | |
| DACK Hold from WR ↑ | $t_{WK}$ | 0 | | 0 | | 0 | | ns | |

## R/M/W Cycle (GDC↔Display Memory)

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Address/Data Delay from 2XWCLK ↑ | $t_{AD}$ | 20 | 105 | 20 | 90 | 15 | 80 | ns | $C_L$ = 50 pF |
| Address/Data Floating from 2XWCLK ↑ | $t_{OFF}$ | 20 | 105 | 20 | 90 | 15 | 80 | ns | $C_L$ = 50 pF |
| Input Data Setup to 2XWCLK ↓ | $t_{DIS}$ | 0 | | 0 | | 0 | | ns | |
| Input Data Hold from 2XWCLK ↓ | $t_{DIH}$ | $t_{DE}$ | | $t_{DE}$ | | $t_{DE}$ | | ns | |
| DBIN Delay from 2XWCLK ↓ | $t_{DE}$ | 20 | 80 | 20 | 70 | 15 | 60 | ns | $C_L$ = 50 pF |
| ALE ↑ Delay from 2XWCLK ↑ | $t_{RR}$ | 20 | 80 | 20 | 70 | 15 | 60 | ns | $C_L$ = 50 pF |
| ALE ↓ Delay from 2XWCLK ↓ | $t_{RF}$ | 20 | 65 | 20 | 55 | 15 | 50 | ns | $C_L$ = 50 pF |
| ALE Width | $t_{RW}$ | ⅓ $t_{CLK}$ | | ⅓ $t_{CLK}$ | | ⅓ $t_{CLK}$ | | ns | $C_L$ = 50 pF |
| ALE Low Width | $t_{RL}$ | 1.5$t_{CLK}$ − 30 | | 1.5$t_{CLK}$ − 30 | | 1.5$t_{CLK}$ − 30 | | ns | |
| Address Setup to ALE ↓ | $t_{AA}$ | 30 | | 30 | | 30 | | ns | |

## Display Cycle (GDC↔Display Memory)

| Parameter | Symbol | 7220D Limits Min | 7220D Limits Max | 7220D-1 Limits Min | 7220D-1 Limits Max | 7220D-2 Limits Min | 7220D-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Video Signal Delay from 2XWCLK ↑ | $t_{VD}$ | | 90 | | 80 | | 70 | ns | $C_L$ = 50 pF |

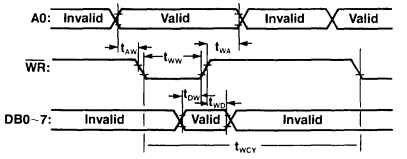
## Input Cycle (GDC↔Display Memory)

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Input Signal Setup to 2XWCLK ↑ | $t_{PS}$ | 10 | | 10 | | 10 | | ns | |
| Input Signal Width | $t_{PW}$ | $t_{CLK}$ | | $t_{CLK}$ | | $t_{CLK}$ | | ns | |

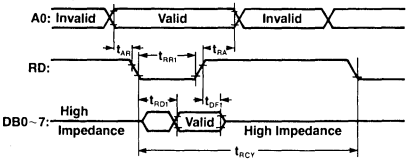
## Clock (2XWCLK)

| Parameter | Symbol | 7220AD Limits Min | 7220AD Limits Max | 7220AD-1 Limits Min | 7220AD-1 Limits Max | 7220AD-2 Limits Min | 7220AD-2 Limits Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Clock Rise Time | $t_{CR}$ | | 15 | | 15 | | 15 | ns | |
| Clock Fall Time | $t_{CF}$ | | 15 | | 15 | | 15 | ns | |
| Clock High Pulse Width | $t_{CH}$ | 70 | | 61 | | 52 | | ns | |
| Clock Low Pulse Width | $t_{CL}$ | 70 | | 61 | | 52 | | ns | |
| Clock Cycle | $t_{CLK}$ | 165 | 10,000 | 145 | 10,000 | 125 | 10,000 | ns | |

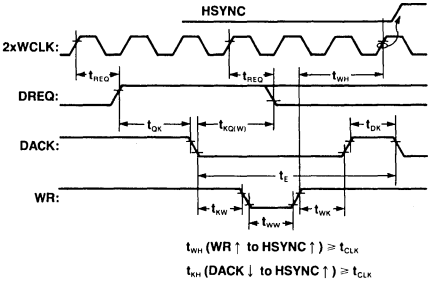
### Microprocessor Interface Write Timing




### Microprocessor Interface Read Timing



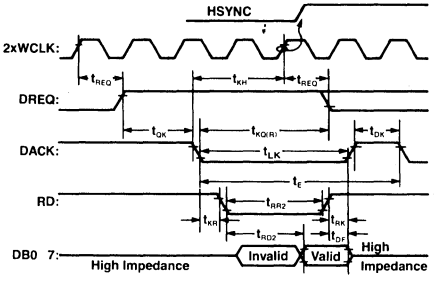

### Microprocessor Interface DMA Write Timing



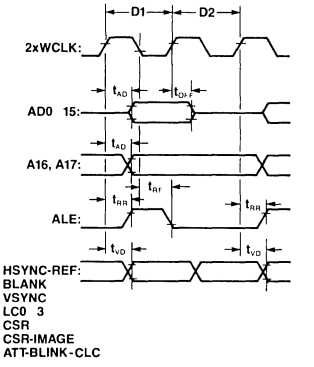

$t_{WH}$ (WR ↑ to HSYNC ↑) ≥ $t_{CLK}$

$t_{KH}$ (DACK ↓ to HSYNC ↑) ≥ $t_{CLK}$

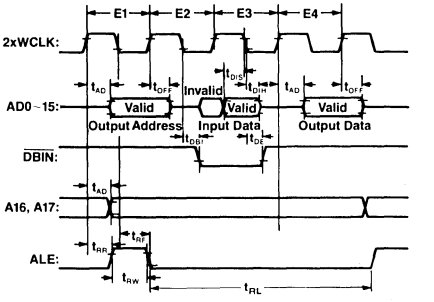
### Microprocessor Interface DMA Read Timing




### Display Memory Display Cycle Timing

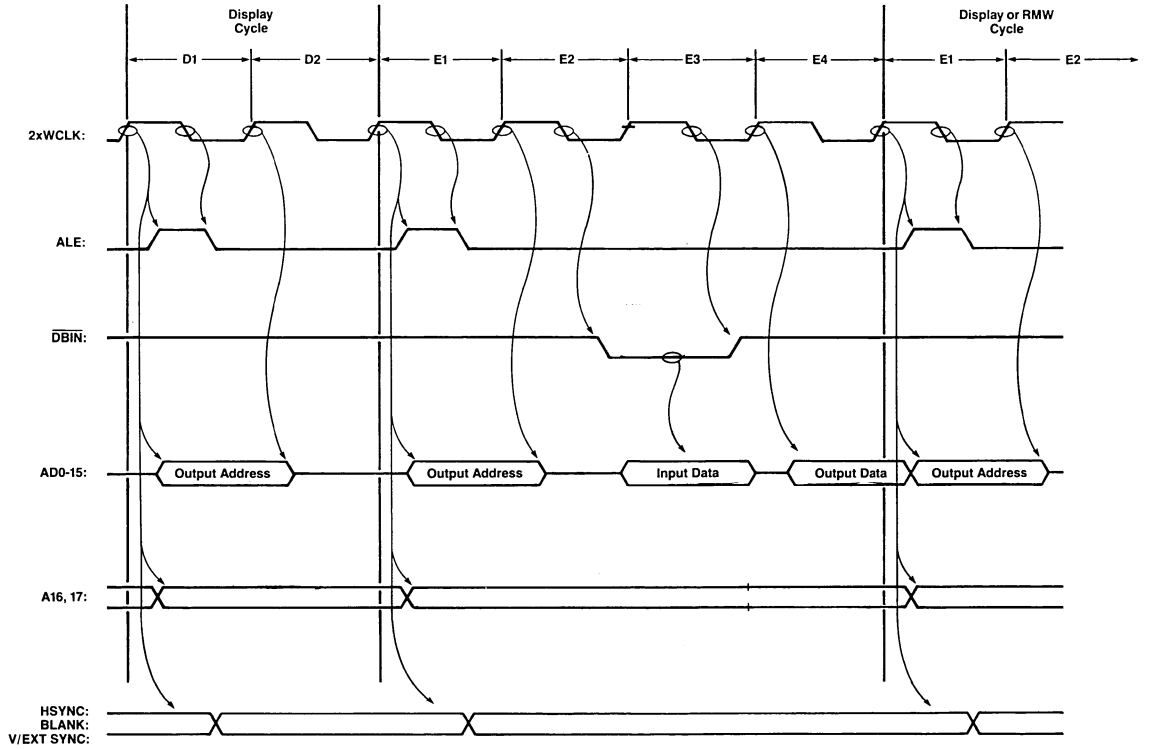



### Display Memory RMW Timing



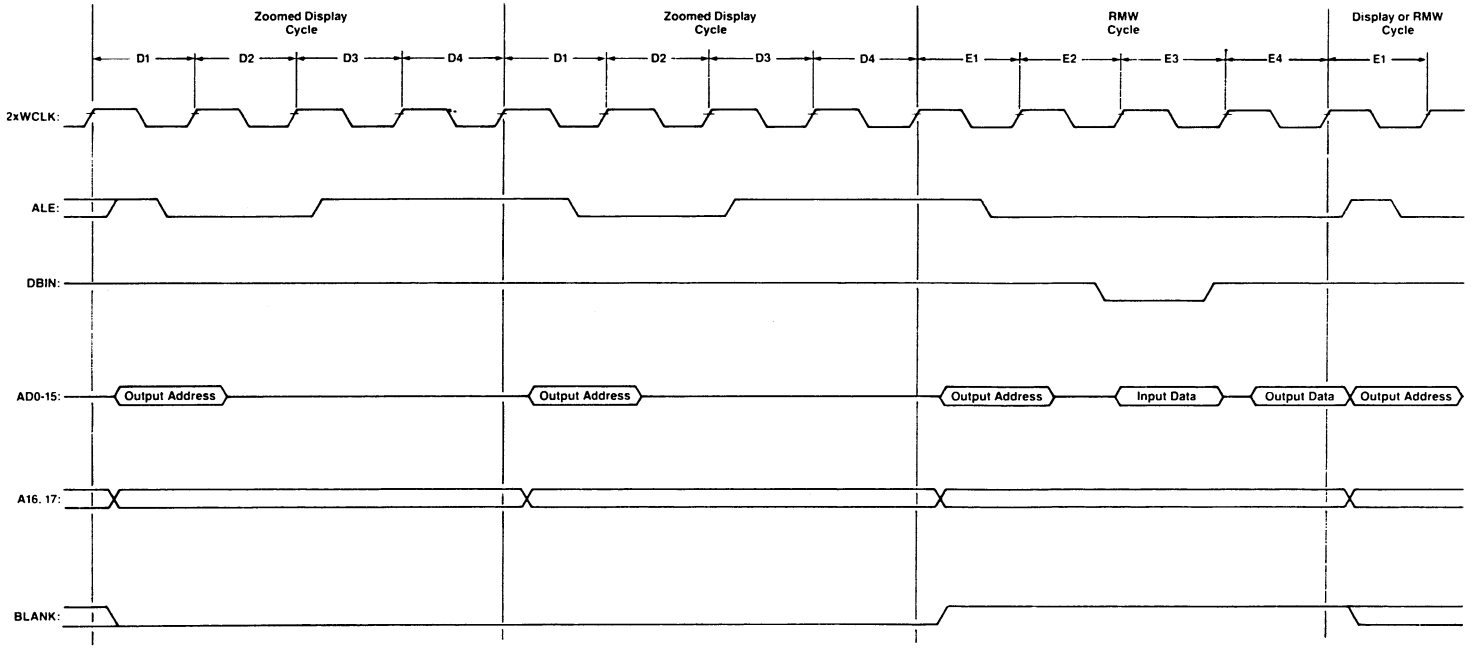

## TIMING WAVEFORMS

## Display and RMW Cycles (1x Zoom)



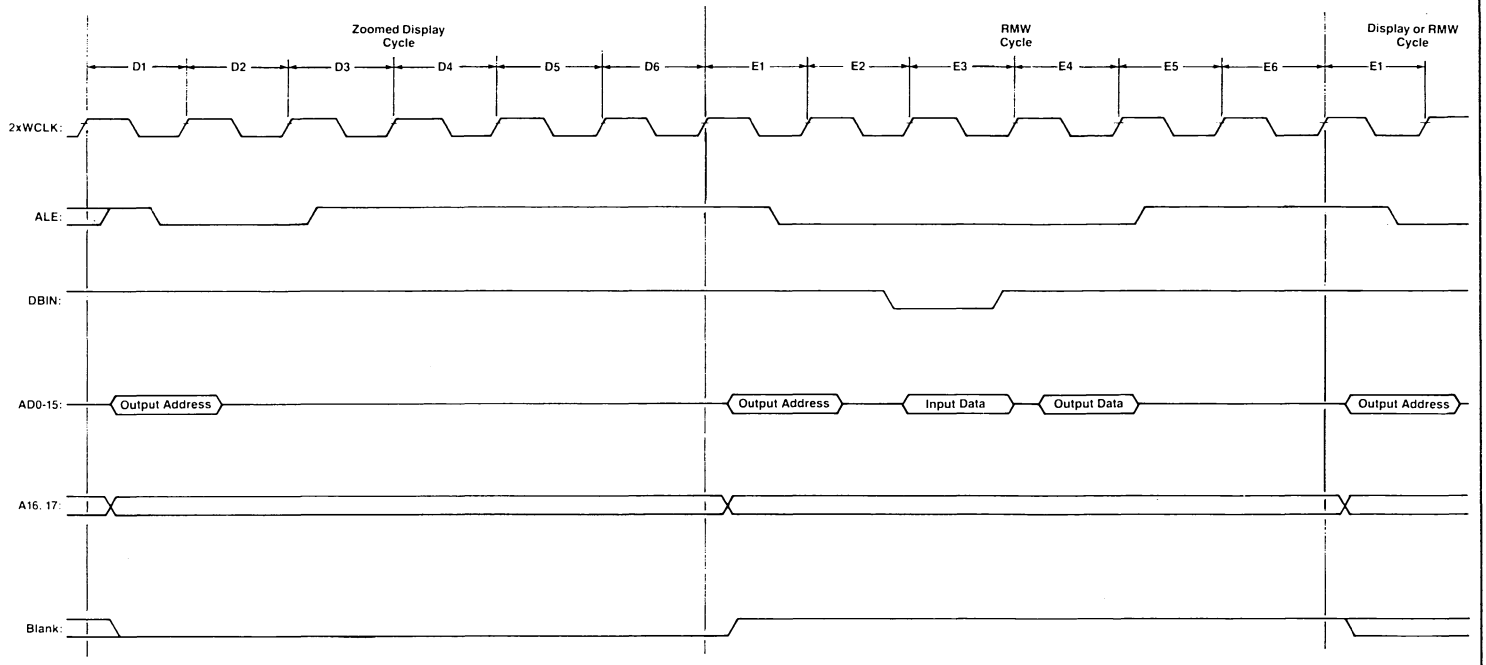

**TIMING WAVEFORMS**

## Display and RMW Cycles (2x Zoom)



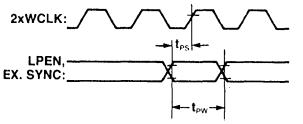

**TIMING WAVEFORMS**

## Zoomed Display Operation with RMW Cycle (3x Zoom)

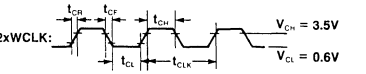



**TIMING WAVEFORMS**

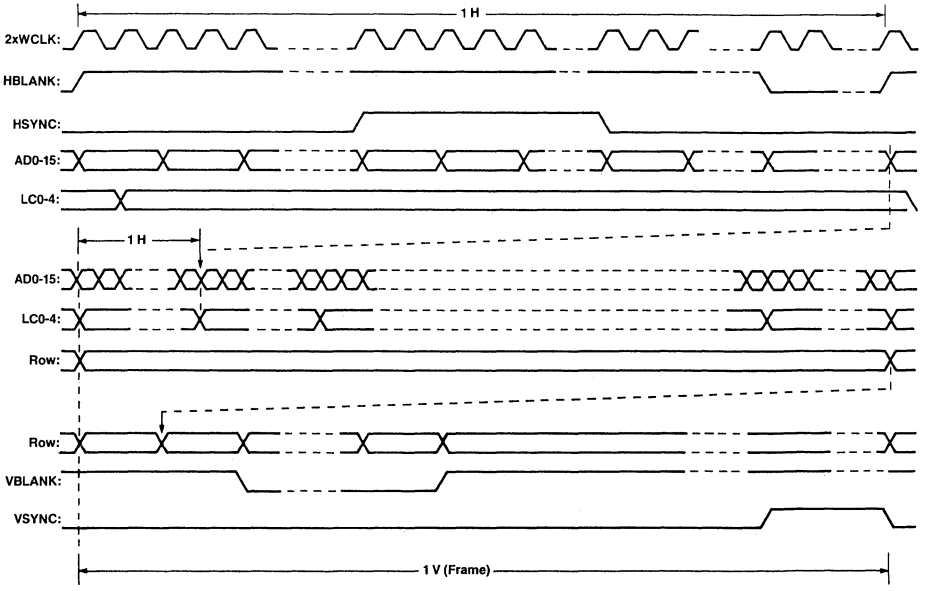
### Light Pen and External Sync Input Timing



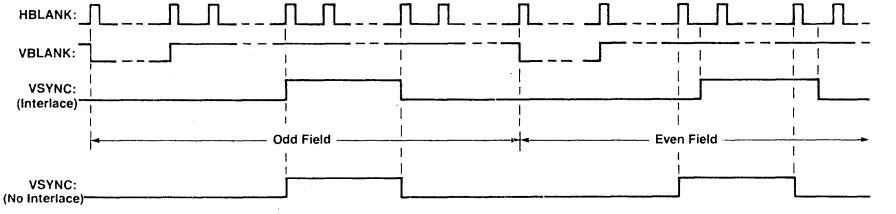

### Clock Timing (2XWCLK)



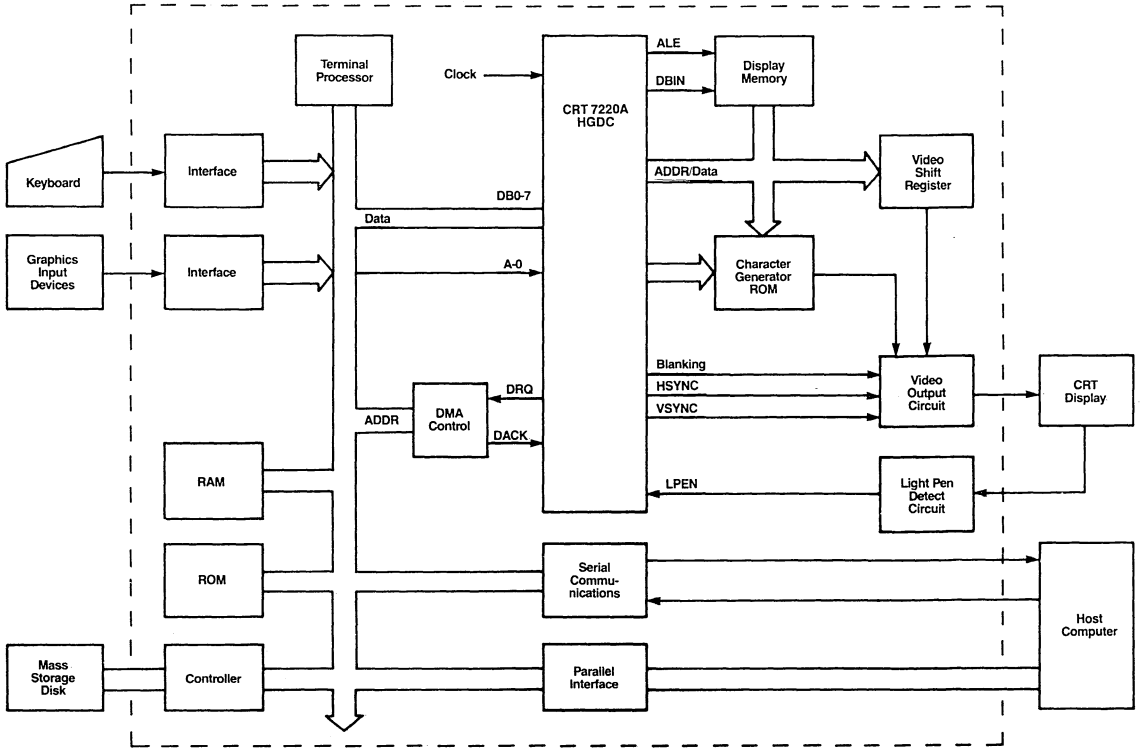

### Video Sync Signals Timing




### Interlaced Video Timing

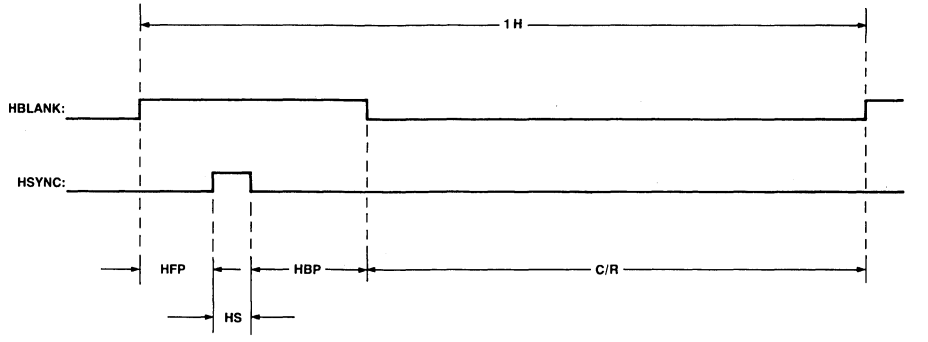



## TIMING WAVEFORMS

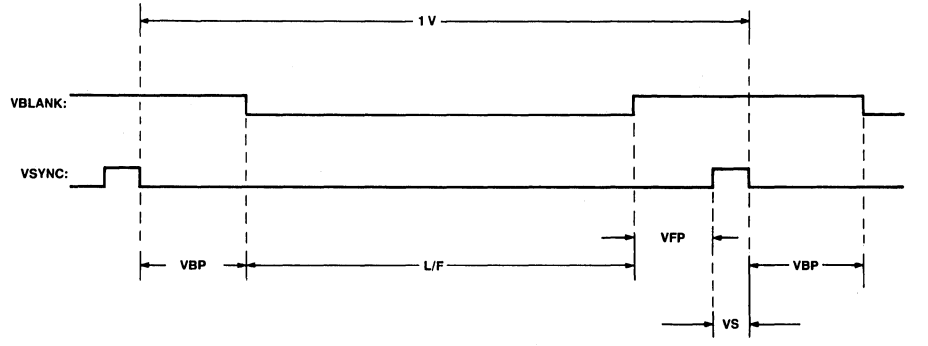



**BLOCK DIAGRAM OF A GRAPHICS TERMINAL**

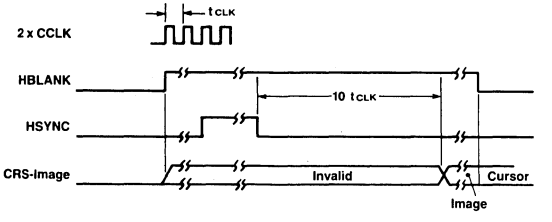
### Video Horizontal Sync Generator Parameters




### Video Vertical Sync Generator Parameters

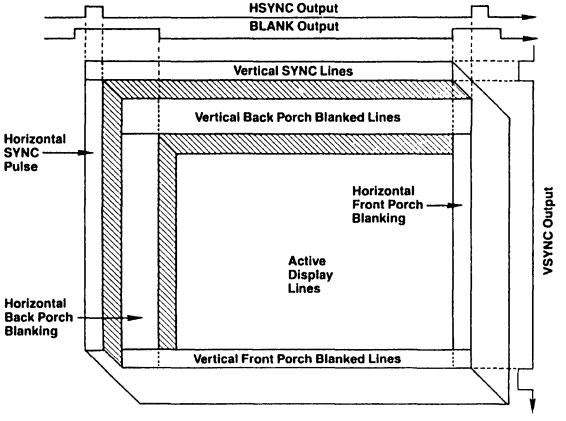



### Cursor—Image Bit Flag

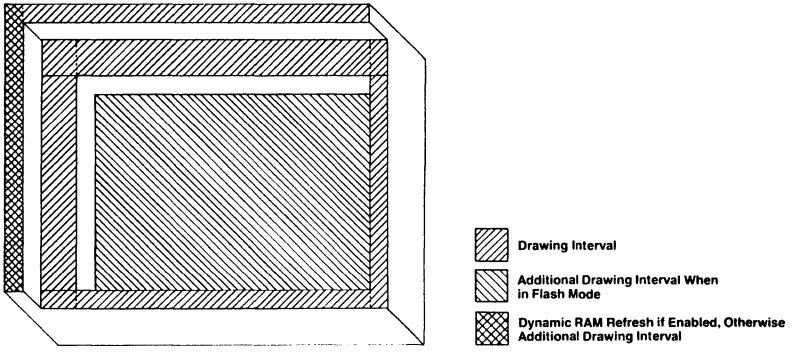



## TIMING WAVEFORMS

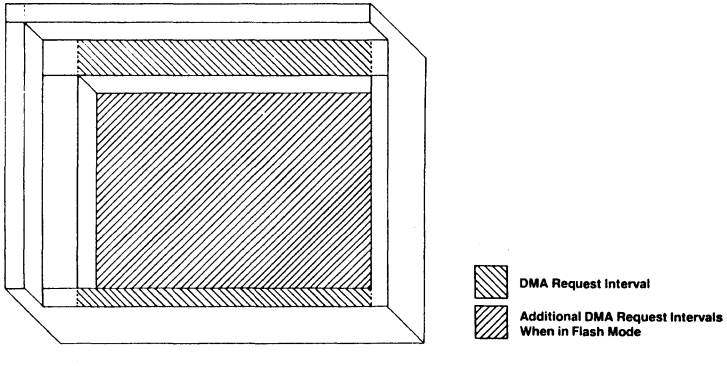
## VIDEO FIELD TIMING

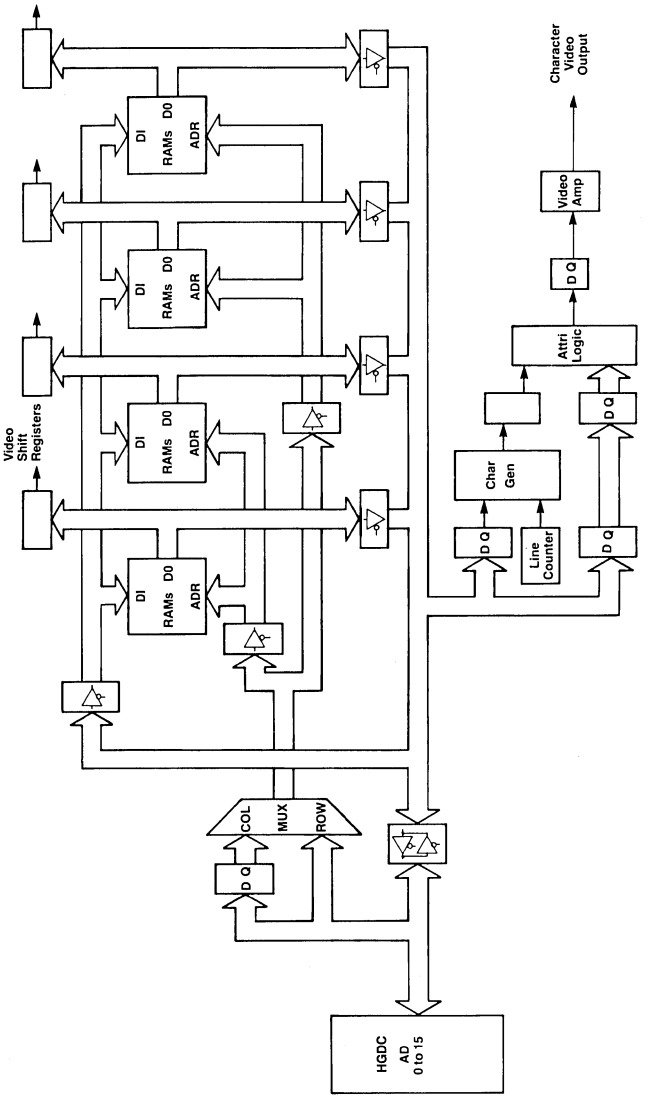



## DRAWING INTERVALS




## DMA REQUEST INTERVALS






MULTIPLANE DISPLAY MEMORY DIAGRAM

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

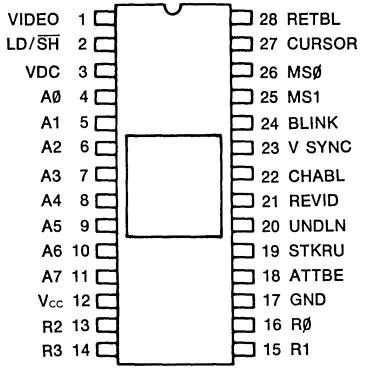
**CRT 8002**
**μPC FAMILY**

# CRT Video Display Attributes Controller Video Generator VDAC™

## FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
    - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

## PIN CONFIGURATION




SECTION V

## General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC™ is a companion chip to SMC's CRT 5027 VTAC. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 15Hz to 1Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5Hz to 0.5Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

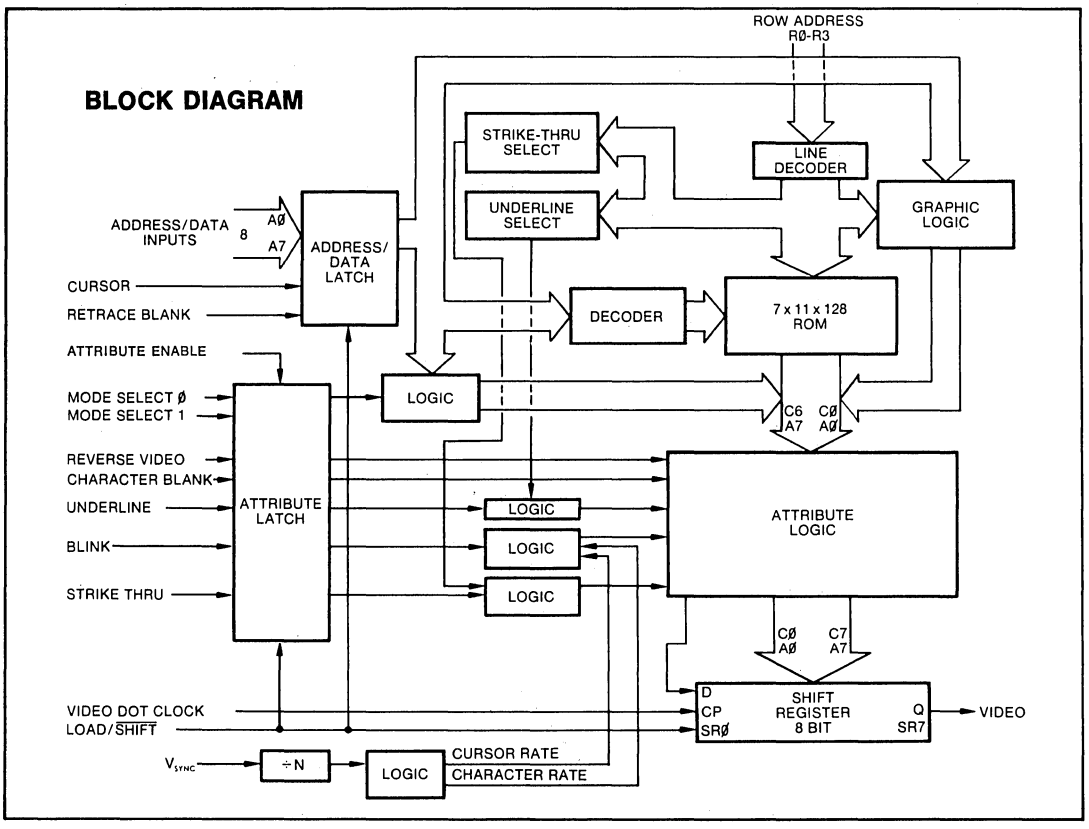
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$= +5V ±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | excluding VDC |
| High-level, $V_{IH}$ | 2.0 | | | V | excluding VDC |
| INPUT VOLTAGE LEVELS-CLOCK | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 4.3 | | | V | See Figure 6 |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=0.4 mA, 74LSXX load |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH}$=−20μA |
| INPUT CURRENT | | | | | |
| Leakage, $I_L$ (Except CLOCK) | | | 10 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| Leakage, $I_L$ (CLOCK Only) | | | 50 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| INPUT CAPACITANCE | | | | | |
| Data | | 10 | | pF | @ 1 MHz |
| LD/$\overline{SH}$ | | 20 | | pF | @ 1 MHz |
| CLOCK | | 25 | | pF | @ 1 MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 100 | | mA | |
| **A.C. CHARACTERISTICS** | | | | | |
| See Figure 6, 7 | | | | | |

| SYMBOL | PARAMETER | CRT 8002A | | CRT 8002B | | CRT 8002C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| VDC | Video Dot Clock Frequency | 1.0 | 20 | 1.0 | 15 | 1.0 | 10 | MHz |
| $PW_H$ | VDC—High Time | 15.0 | | 23 | | 40 | | ns |
| $PW_L$ | VDC—Low Time | 15.0 | | 23 | | 40 | | ns |
| $t_{CY}$ | LD/$\overline{SH}$ cycle time | 400 | | 533 | | 800 | | ns |
| $t_r$, $t_f$ | Rise, fall time | | 10 | | 10 | | 10 | ns |
| $t_{SET-UP}$ | Input set-up time | ≥0 | | ≥0 | | ≥0 | | ns |
| $t_{HOLD}$ | Input hold time | 15 | | 15 | | 15 | | ns |
| $t_{PDI}$, $t_{PDO}$ | Output propagation delay | 15 | 50 | 15 | 65 | 15 | 100 | ns |
| $t_1$ | LD/$\overline{SH}$ set-up time | 10 | | 15 | | 20 | | ns |
| $t_2$ | LD/$\overline{SH}$ hold time | 15 | | 15 | | 15 | | ns |



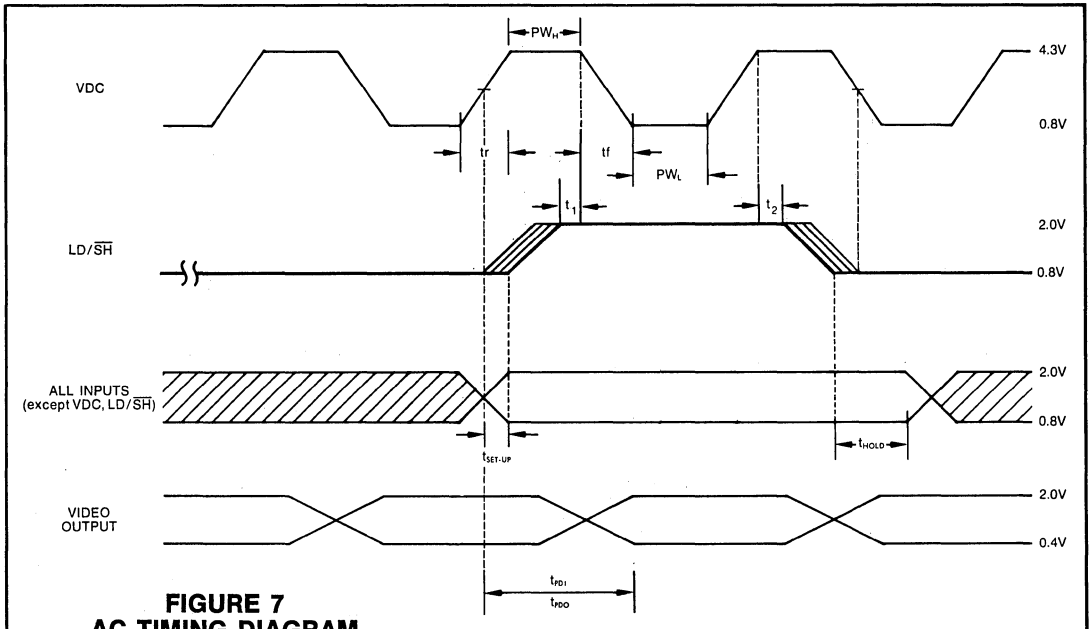




**FIGURE 7**
**AC TIMING DIAGRAM**

SECTION V

# DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 1 | VIDEO | Video Output | 0 | The video output contains the dot stream for the selected row of the alpha-numeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs.<br>In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ.<br>The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4.<br>When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats. |
| 2 | LD/$\overline{\text{SH}}$ | Load/$\overline{\text{Shift}}$ | I | The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7. |
| 3 | VDC | Video Dot Clock | I | Frequency at which video is shifted. |
| 4-11 | AØ-A7 | Address/Data | I | In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments. |
| 12 | $V_{CC}$ | Power Supply | PS | +5 volt power supply |
| 13,14,15,16 | R2,R3,R1,RØ | Row Address | I | These 4 binary inputs define the row address in the current character block. |
| 17 | GND | Ground | GND | Ground |
| 18 | ATTBE | Attribute Enable | I | A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7. |
| 19 | STKRU | Strike-Thru | I | When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6. |
| 20 | UNDLN | Underline | I | When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard under-line will be a single line on R11. |
| 21 | REVID | Reverse Video | I | When this input is low and $\overline{\text{RETBL}}$ = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1. |
| 22 | CHABL | Character Blank | I | When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1. |
| 23 | V SYNC | V SYNC | I | This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character). |
| 24 | BLINK | Blink | I | When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz. |
| 25<br>26 | MS1<br>MSØ | Mode Select 1<br>Mode Select Ø | I<br>I | These 2 inputs define the four modes of operation of the CRT 8002 as follows:<br>Alphanumeric Mode — In this mode addresses AØ-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic.<br>Thin Graphics Mode — In this mode AØ-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row. |

| MS1 | MSØ | MODE |
|---|---|---|
| 1 | 1 | Alphanumeric |
| 1 | 0 | Thin Graphics |
| 0 | 1 | External Mode |
| 0 | 0 | Wide Graphics |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 25<br>26<br>(cont.) | | | | External Mode – In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3.<br>Wide Graphics Mode—In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory.<br>These 4 modes can be intermixed on a per character basis. |
| 27 | CURSOR | Cursor | I | When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are:<br>Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs.<br>Blinking Underline—In this mode the underline blinks at the cursor rate.<br>Reverse Video Block—In this mode the Character Block is set to reverse video.<br>Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video.<br>The cursor functions are listed in table 1. |
| 28 | RETBL | Retrace Blank | I | When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time. |

## TABLE 1

| CURSOR | RETBL | REVID | CHABL | UNDLN* | FUNCTION |
|---|---|---|---|---|---|
| X | 1 | X | X | X | "0" S.R. All |
| 0 | 0 | 0 | 0 | 0 | D (S.R.) All |
| 0 | 0 | 0 | 0 | 1 | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| 0 | 0 | 0 | 1 | X | "0" (S.R.) All |
| 0 | 0 | 1 | 0 | 0 | D (S.R.) All |
| 0 | 0 | 1 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| 0 | 0 | 1 | 1 | X | "1" (S.R.) All |
| Underline* | 0 | 0 | 0 | X | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| Underline* | 0 | 0 | 1 | X | "1" (S.R.)* |
| | | | | | "0" (S.R.) All others |
| Underline* | 0 | 1 | 0 | X | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| Underline* | 0 | 1 | 1 | X | "0" (S.R.)* |
| | | | | | "1" (S.R.) All others |
| Blinking** Underline* | 0 | 0 | 0 | X | "1" (S.R.)* Blinking |
| | | | | | D (S.R.) All others |
| Blinking** Underline* | 0 | 0 | 1 | X | "1" (S.R.)* Blinking |
| | | | | | "0" (S.R.) All others |
| Blinking** Underline* | 0 | 1 | 0 | X | "0" (S.R.)* Blinking |
| | | | | | D (S.R.) All others |
| Blinking** Underline* | 0 | 1 | 1 | X | "0" (S.R.)* Blinking |
| | | | | | "1" (S.R.) All others |
| REVID Block | 0 | 0 | 0 | 0 | D (S.R.) All |
| REVID Block | 0 | 0 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 0 | 1 | X | "1" (S.R.) All |
| REVID Block | 0 | 0 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 1 | 0 | 0 | D (S.R.) All |
| REVID Block | 0 | 1 | 0 | 1 | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 1 | 1 | X | "0" (S.R.) All |
| Blink** REVID Block | 0 | 0 | 0 | 0 | Alternate Normal Video/REVID At Cursor Blink Rate |
| Blink** REVID Block | 0 | 0 | 0 | 1 | |
| Blink** REVID Block | 0 | 0 | 1 | X | |
| Blink** REVID Block | 0 | 1 | 0 | 0 | |
| Blink** REVID Block | 0 | 1 | 0 | 1 | |
| Blink** REVID Block | 0 | 1 | 1 | X | |

*At Selected Row Decode **At Cursor Blink Rate

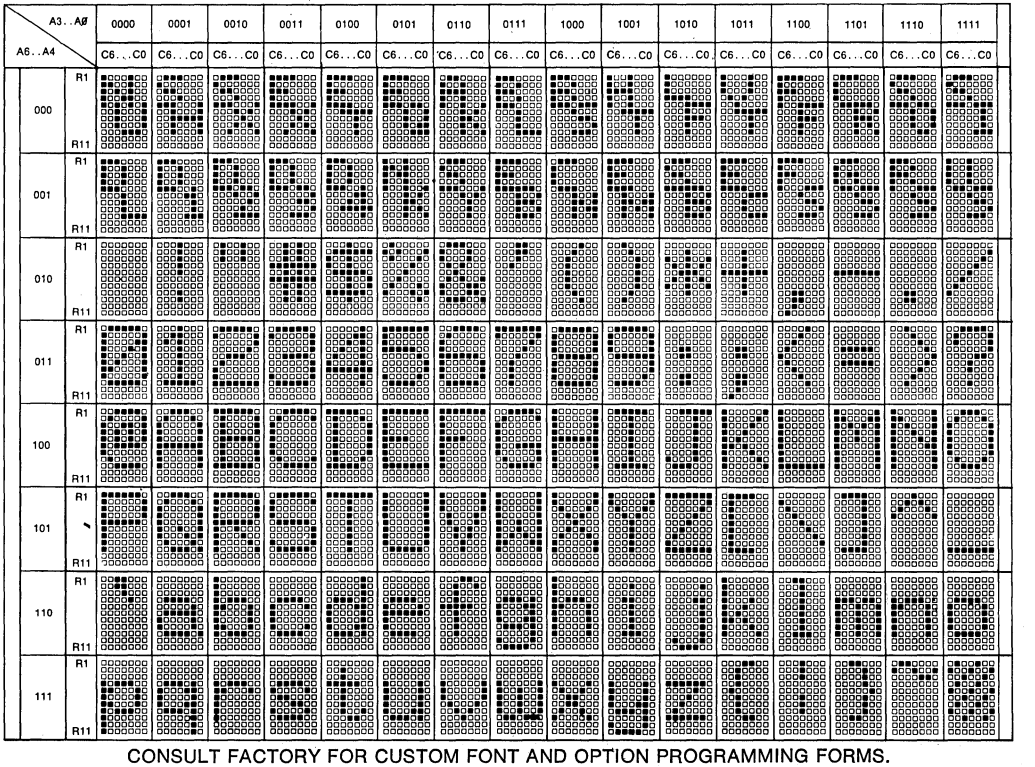
*Note:* If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

## FIGURE 5
## ROM CHARACTER BLOCK FORMAT

| | *C7 | C6 | C5 | C4 | C3 | C2 | C1 | CØ | — | — | ROWS | R3 | R2 | R1 | RØ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (ALL ZEROS) → | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | RØ | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R1 | 0 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R2 | 0 | 0 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R3 | 0 | 0 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R4 | 0 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R5 | 0 | 1 | 0 | 1 |
| 77 BITS (7 x 11 ROM) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R6 | 0 | 1 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R7 | 0 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R8 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R9 | 1 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | RIØ | 1 | 0 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R11 | 1 | 0 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R12 | 1 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R13 | 1 | 1 | 0 | 1 |
| (ALL ZEROS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R14 | 1 | 1 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R15 | 1 | 1 | 1 | 1 |

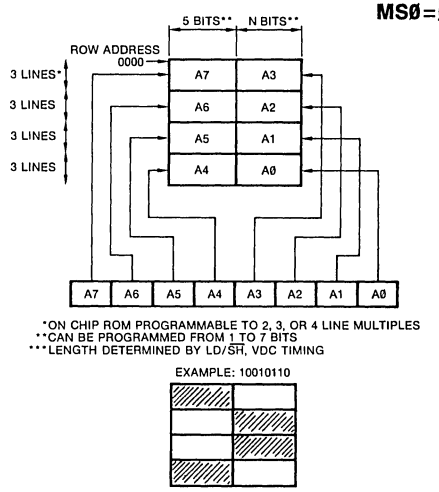
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/$\overline{SH}$, VDC TIMING)

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST




CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

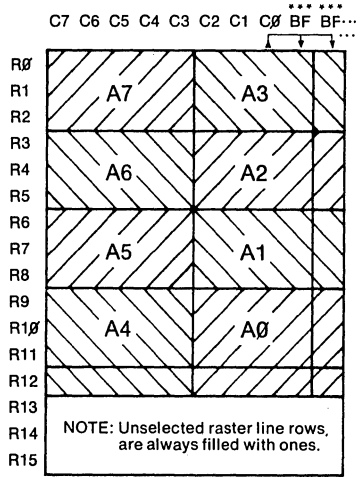
## FIGURE 1
## WIDE GRAPHICS MODE
**MSØ=Ø MS1=Ø**




*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/$\overline{SH}$, VDC TIMING

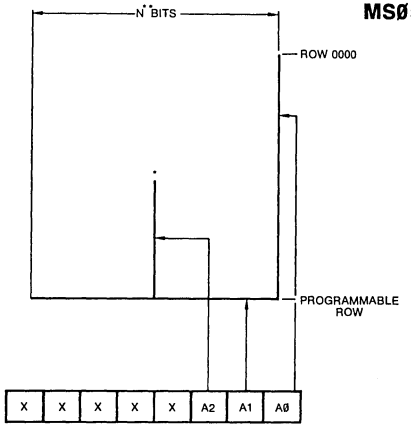
EXAMPLE: 10010110



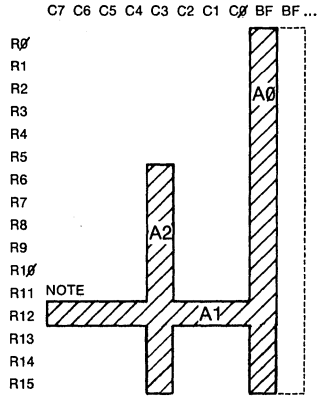



BF = back fill

## FIGURE 2
## THIN GRAPHICS MODE
**MSØ=Ø MS1=1**




X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/$\overline{SH}$, VDC TIMING




NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

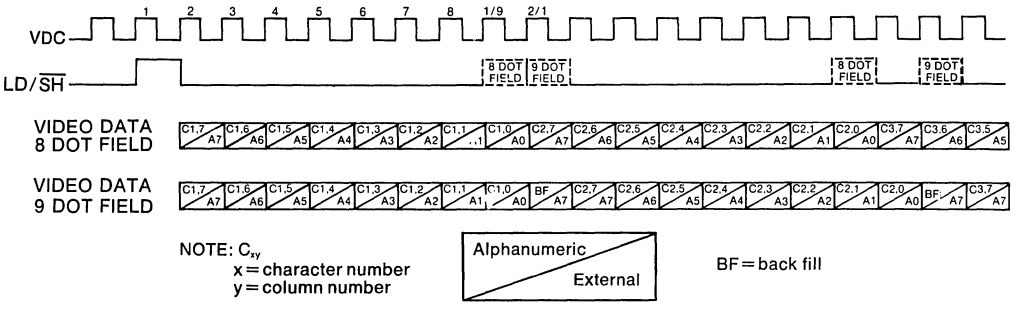
BF = back fill

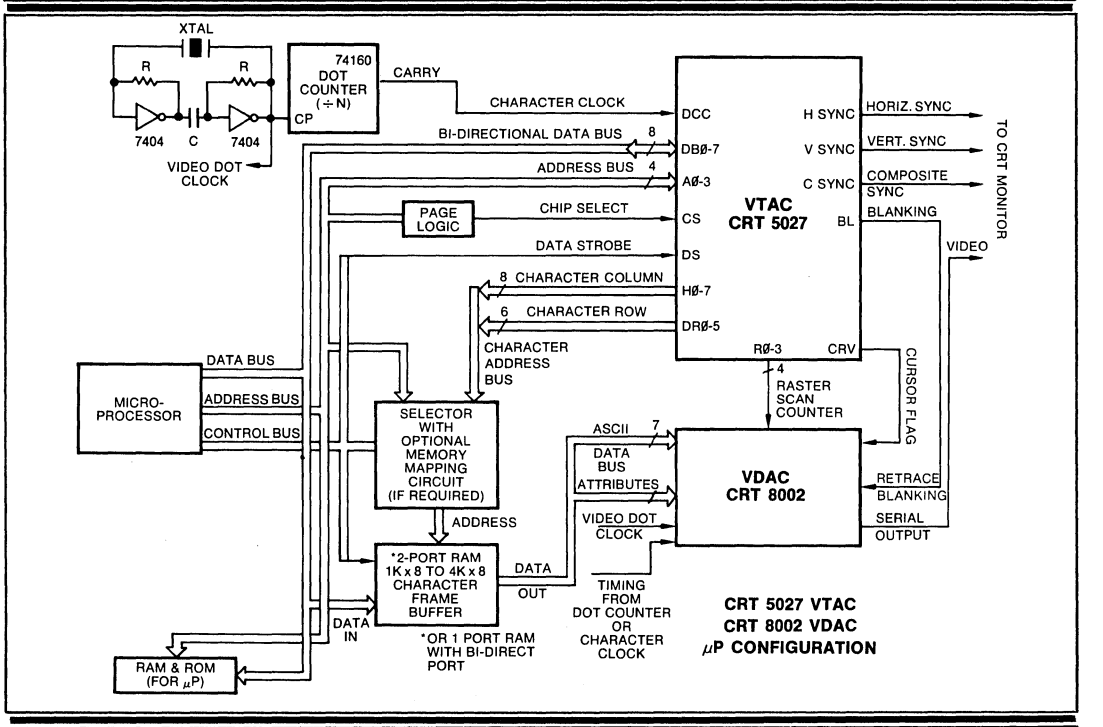
## FIGURE 3
## EXTERNAL MODE
**MSØ=1 MS1=Ø**

| | C7 | C6 | C5 | C4 | C3 | C2 | C1 | CØ | BF | BF | ··· |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RØ – R15 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | AØ | A7 | A7 | ··· |

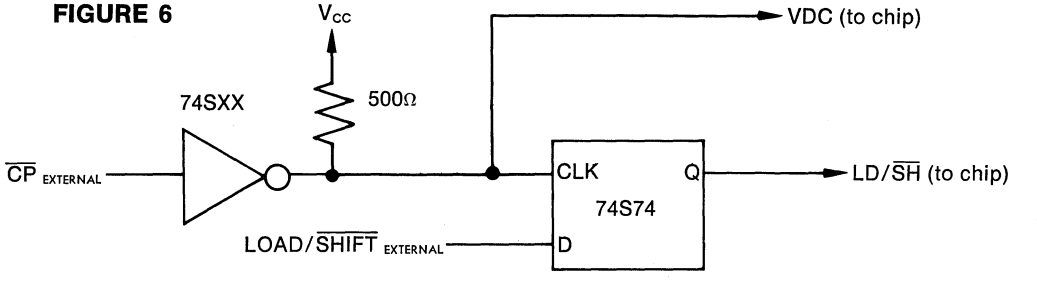
BF = back fill

## FIGURE 4 TYPICAL VIDEO OUTPUT

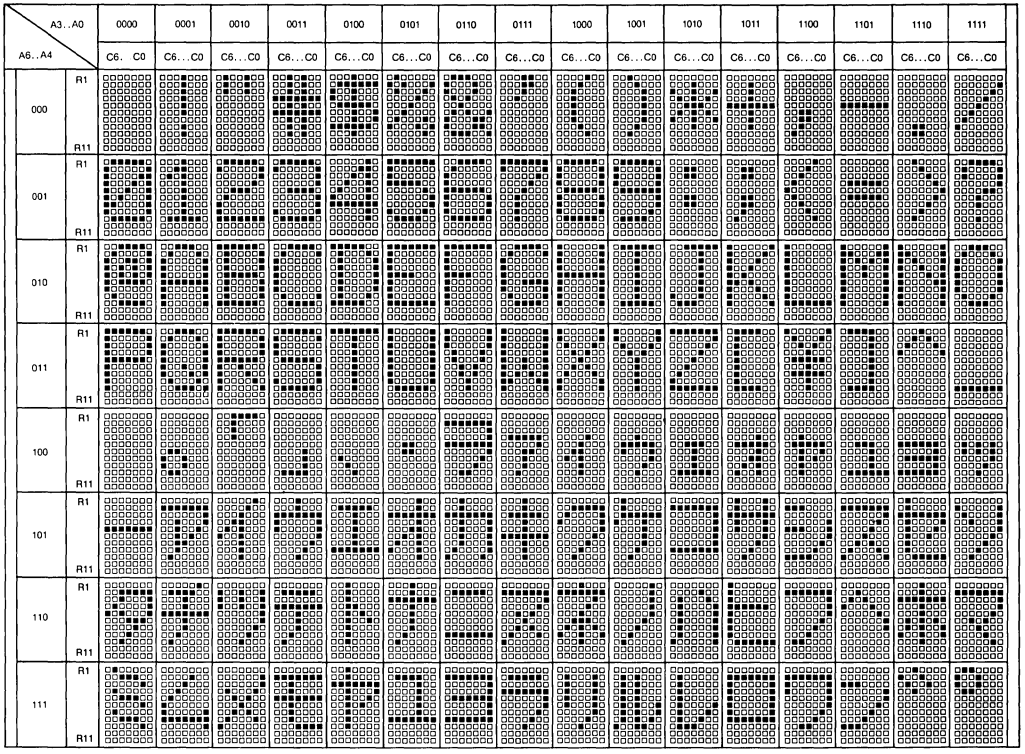


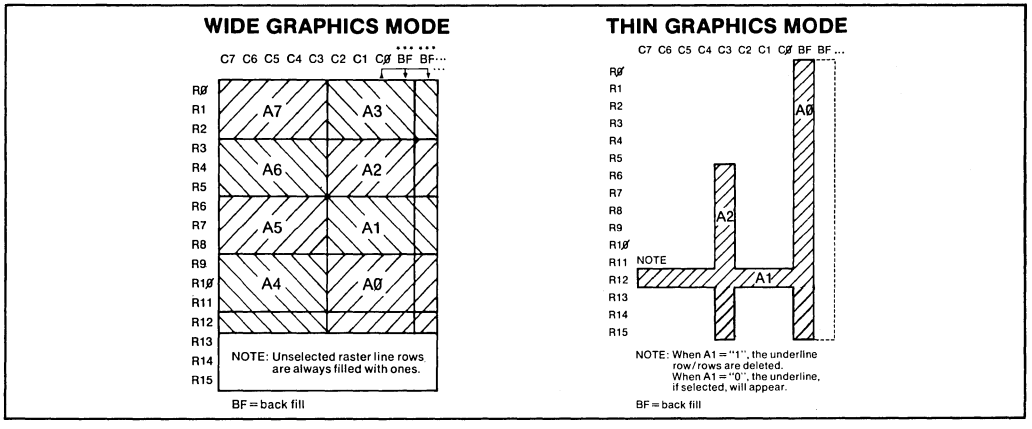




## FIGURE 6



# CRT Video Display-Controller Video Generator VDAC™




## ATTRIBUTES

**Underline**
Underline will be a single horizontal line at row R11

**Cursor**
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

**Blink Rate**
The character blink rate will be 1.875 Hz

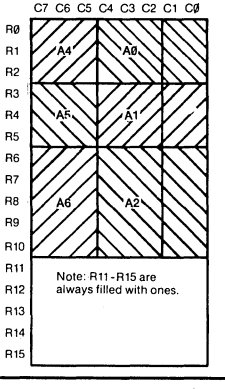
**Strike-Thru**
The strike-thru will be a double line at rows R5 and R6

SECTION V

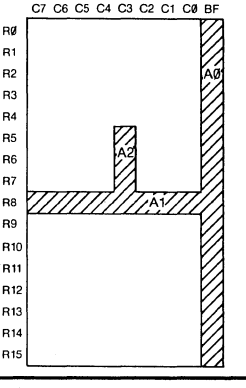
# CRT Video Display-Controller Video Generator VDAC™

| A6..A4 \ A3..A0 | | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 | C6...C0 |
| 000 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 001 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 010 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 011 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 100 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 101 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 110 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |
| 111 | R1 | | | | | | | | | | | | | | | | |
| | R11 | | | | | | | | | | | | | | | | |

## WIDE GRAPHICS MODE




## THIN GRAPHICS MODE




## ATTRIBUTES

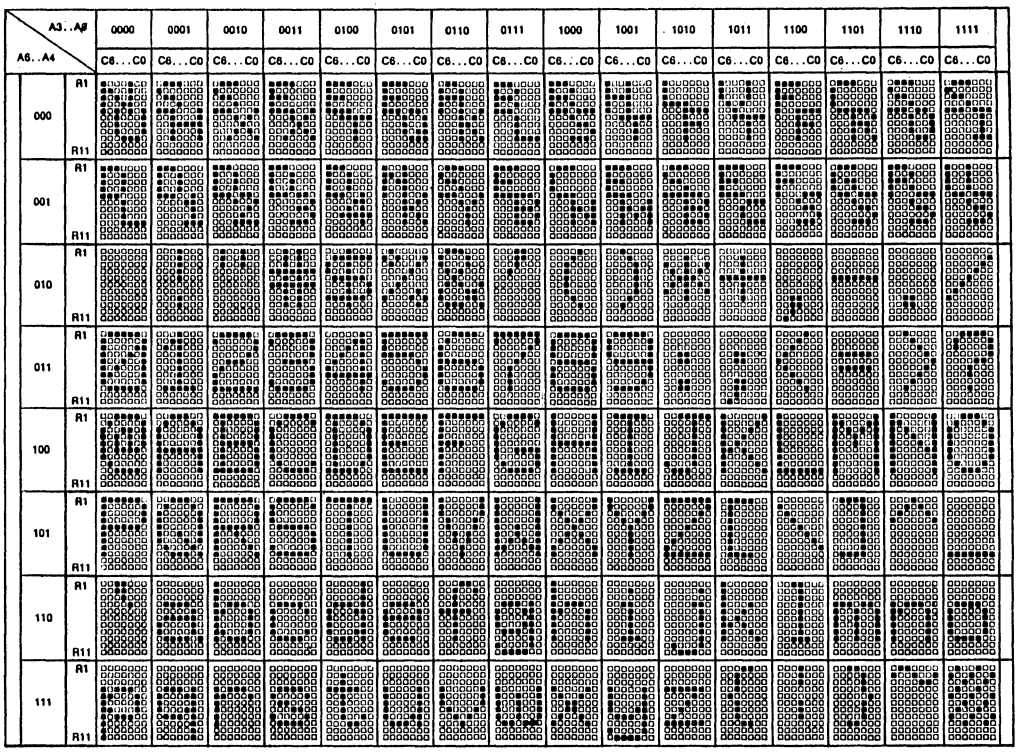
**Underline**
Underline will be a single horizontal line at R8

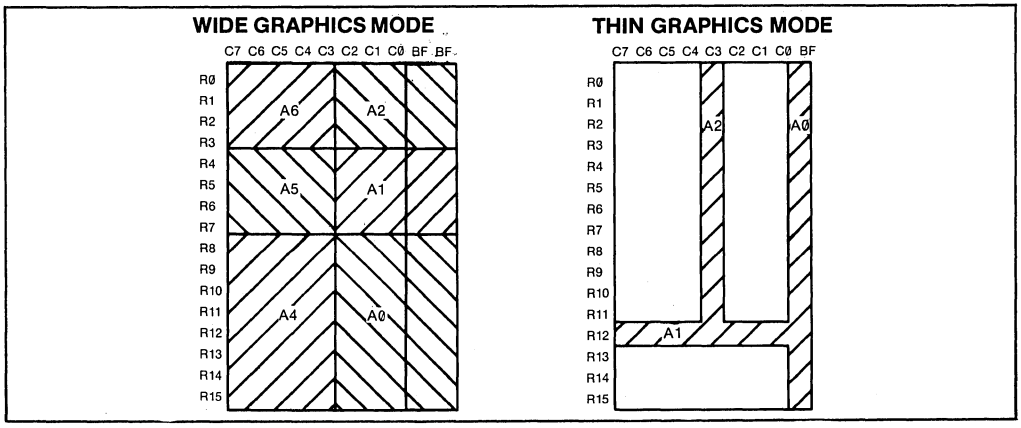
**Cursor**
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

**Blink Rate**
The character blink rate is 1.875 Hz

**Strike-Thru**
The strike-thru will be a single horizontal line at R4

# CRT Video Display-Controller Video Generator VDAC™




## ATTRIBUTES

**Underline**
Underline will be a single horizontal line at R12

**Cursor**
Cursor will be a reverse video block

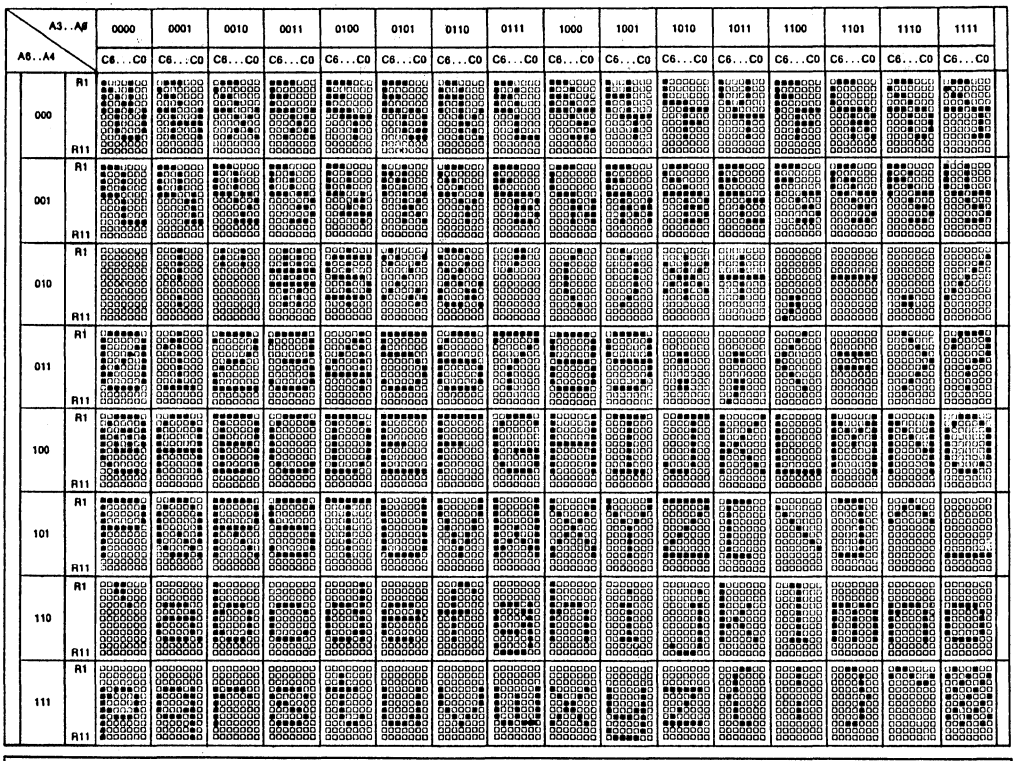
**Blink Rate**
The character blink rate is 1.875 Hz

**Strike-Thru**
The strike-thru will be a double line at rows R5 and R6

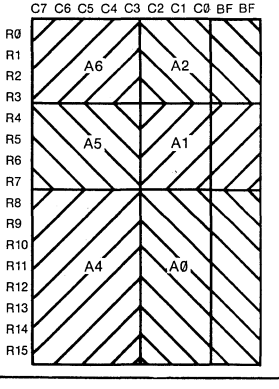
STANDARD MICROSYSTEMS CORPORATION

# CRT 8002-011 (ASCII) CODING INFORMATION

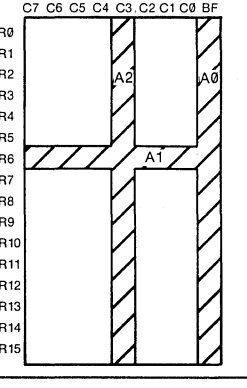
# CRT Video Display-Controller Video Generator VDAC™




## WIDE GRAPHICS MODE




## THIN GRAPHICS MODE




## ATTRIBUTES

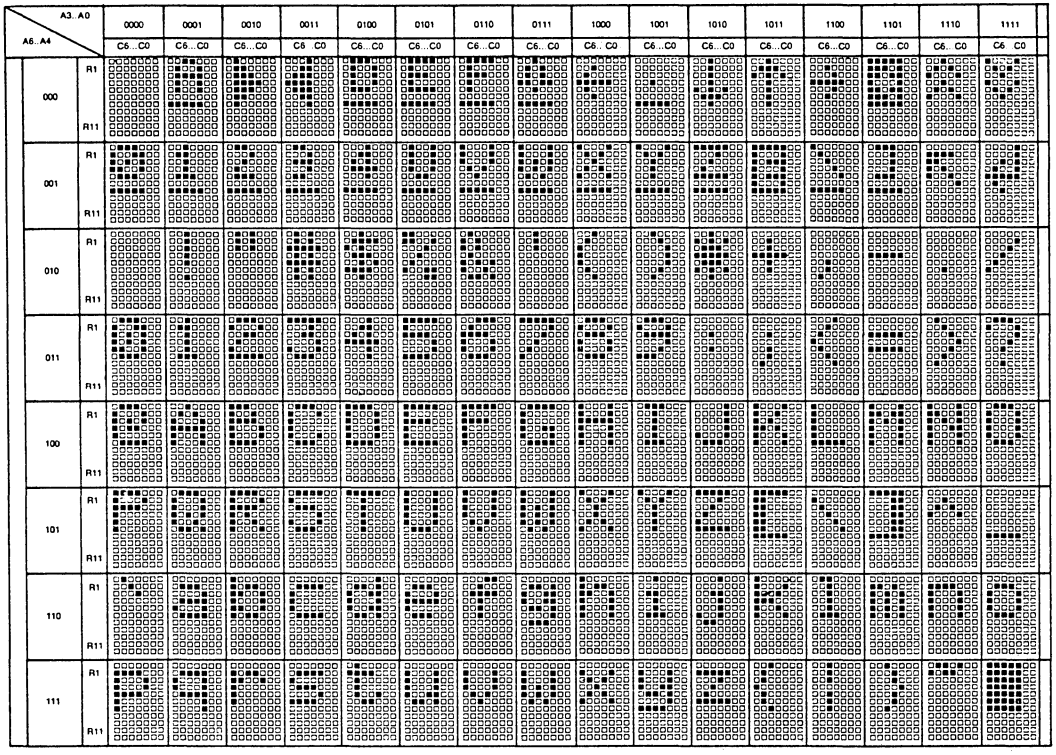
**Underline**
Underline will be a single horizontal line at R11

**Cursor**
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

**Blink Rate**
The character blink rate is 1.875 Hz

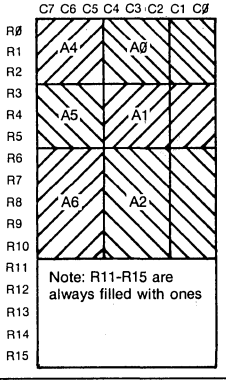
**Strike-Thru**
The strike-thru will be a double line at rows R5 and R6

# CRT Video Display-Controller Video Generator VDAC™

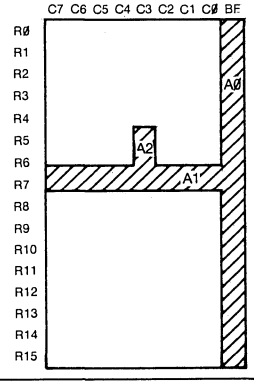





## WIDE GRAPHICS MODE




## THIN GRAPHICS MODE




## ATTRIBUTES

**Underline**
Underline will be a double horizontal line at R7 and R8

**Cursor**
Cursor will be a reverse video block

**Blink Rate**
The character blink rate is 1.875 Hz

**Strike-Thru**
The strike-thru will be a single horizontal line at R4

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

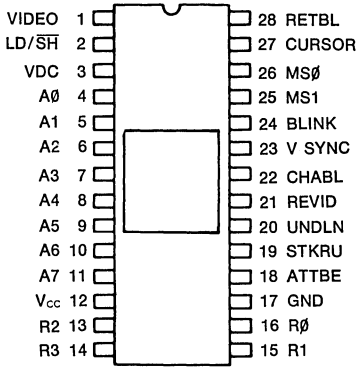
**CRT 8002H**
**μPC FAMILY**

# CRT Video Display Attributes Controller Video Generator VDAC™

## FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency 25 MHz
- ☐ ROM Access time 310 ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ On chip cursor
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM

## PIN CONFIGURATION




- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ N-channel COPLAMOS® Titanium Disilicide Process
- ☐ Compatible with CRT 5027/37 VTAC®

SECTION V

### General Description

The SMC CRT 8002H Video Display Attributes Controller (VDAC) is an n-channel COPLAMOS® MOS/LSI device. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002H VDAC is a companion chip to SMC's CRT 5027/37 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002H video output may be connected directly to a CRT monitor video input. The CRT 5027/37 blanking output can be connected directly to the CRT 8002H retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

The CRT 8002H attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002H produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002H can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

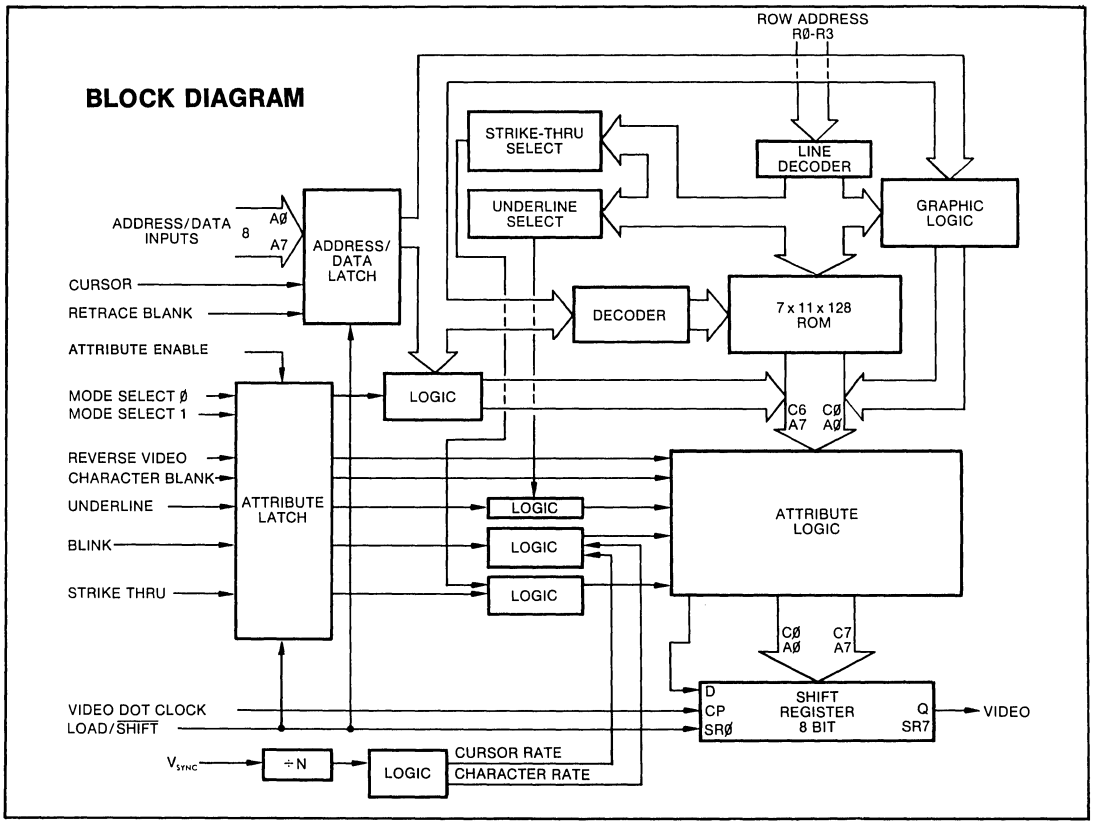
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | excluding VDC |
| High-level, $V_{IH}$ | 2.0 | | | V | excluding VDC |
| INPUT VOLTAGE LEVELS-CLOCK | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 4.3 | | | V | See Figure 6 |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=0.4 mA, 74LSXX load |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH}$=−20μA |
| INPUT CURRENT | | | | | |
| Leakage, $I_L$ (Except CLOCK) | | | 10 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| Leakage, $I_L$ (CLOCK Only) | | | 50 | μA | $0 \leq V_{IN} \leq V_{CC}$ |
| INPUT CAPACITANCE | | | | | |
| Data | | 10 | | pF | @ 1 MHz |
| LD/$\overline{SH}$ | | 20 | | pF | @ 1 MHz |
| CLOCK | | 25 | | pF | @ 1 MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 100 | | mA | |
| **A.C. CHARACTERISTICS** | | | | | |
| See Figure 6, 7 | | | | | |

| SYMBOL | PARAMETER | MIN. | MAX. | UNITS |
|---|---|---|---|---|
| VDC | Video Dot Clock Frequency | 1.0 | 25 | MHz |
| $PW_H$ | VDC—High Time | 11.0 | | ns |
| $PW_L$ | VDC—Low Time | 11.0 | | ns |
| $t_{CY}$ | LD/SH cycle time | 310 | | ns |
| $t_r$, $t_f$ | Rise, fall time | | 9 | ns |
| $t_{SET-UP}$ | Input set-up time | ≥0 | | ns |
| $t_{HOLD}$ | Input hold time | 15 | | ns |
| $t_{PDI}$, $t_{PDO}$ | Output propagation delay | 15 | 27 | ns |
| $t_1$ | LD/SH set-up time | 5 | | ns |
| $t_2$ | LD/SH hold time | 5 | | ns |



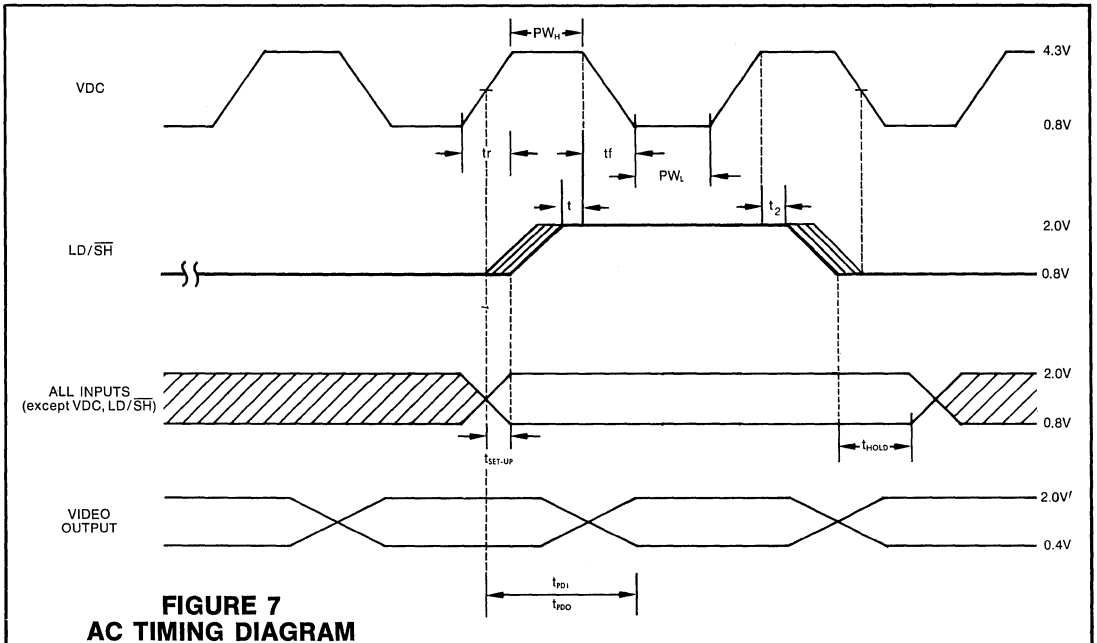




**FIGURE 7**
**AC TIMING DIAGRAM**

SECTION V

# DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 1 | VIDEO | Video Output | 0 | The video output contains the dot stream for the selected row of the alpha-numeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs.<br>In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ.<br>The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4.<br>When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats. |
| 2 | LD/$\overline{\text{SH}}$ | Load/$\overline{\text{Shift}}$ | I | The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7. |
| 3 | VDC | Video Dot Clock | I | Frequency at which video is shifted. |
| 4-11 | AØ-A7 | Address/Data | I | In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7=X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments. |
| 12 | $V_{CC}$ | Power Supply | PS | +5 volt power supply |
| 13,14,15,16 | R2,R3,R1,RØ | Row Address | I | These 4 binary inputs define the row address in the current character block. |
| 17 | GND | Ground | GND | Ground |
| 18 | ATTBE | Attribute Enable | I | A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7. |
| 19 | STKRU | Strike-Thru | I | When this input is high and RETBL=0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6. |
| 20 | UNDLN | Underline | I | When this input is high and RETBL=0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11. |
| 21 | REVID | Reverse Video | I | When this input is low and RETBL=0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1. |
| 22 | CHABL | Character Blank | I | When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1. |
| 23 | V SYNC | V SYNC | I | This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character). |
| 24 | BLINK | Blink | I | When this input is high and RETBL=0 and CHABL=0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875Hz. |
| 25<br>26 | MS1<br>MSØ | Mode Select 1<br>Mode Select Ø | I<br>I | These 2 inputs define the four modes of operation of the CRT 8002 as follows:<br>Alphanumeric Mode — In this mode addresses AØ-A6 (A7=X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic.<br>Thin Graphics Mode — In this mode AØ-A2 (A3-A7=X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row. |

| MS1 | MSØ | MODE |
|---|---|---|
| 1 | 1 | Alphanumeric |
| 1 | 0 | Thin Graphics |
| 0 | 1 | External Mode |
| 0 | 0 | Wide Graphics |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 25<br>26<br>(cont.) | | | | External Mode — In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3.<br>Wide Graphics Mode—In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory.<br>These 4 modes can be intermixed on a per character basis. |
| 27 | CURSOR | Cursor | I | When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are:<br>Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs.<br>Blinking Underline—In this mode the underline blinks at the cursor rate.<br>Reverse Video Block—In this mode the Character Block is set to reverse video.<br>Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video.<br>The cursor functions are listed in table 1. |
| 28 | RETBL | Retrace Blank | I | When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time. |

## TABLE 1

| CURSOR | RETBL | REVID | CHABL | UNDLN* | FUNCTION |
|---|---|---|---|---|---|
| X | 1 | X | X | X | "0" S.R. All |
| 0 | 0 | 0 | 0 | 0 | D (S.R.) All |
| 0 | 0 | 0 | 0 | 1 | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| 0 | 0 | 0 | 1 | X | "0" (S.R.) All |
| 0 | 0 | 1 | 0 | 0 | D (S.R.) All |
| 0 | 0 | 1 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| 0 | 0 | 1 | 1 | X | "1" (S.R.) All |
| Underline* | 0 | 0 | 0 | X | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| Underline* | 0 | 0 | 1 | X | "1" (S.R.)* |
| | | | | | "0" (S.R.) All others |
| Underline* | 0 | 1 | 0 | X | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| Underline* | 0 | 1 | 1 | X | "0" (S.R.)* |
| | | | | | "1" (S.R.) All others |
| Blinking** Underline* | 0 | 0 | 0 | X | "1" (S.R.)* Blinking |
| | | | | | D (S.R.) All others |
| Blinking** Underline* | 0 | 0 | 1 | X | "1" (S.R.)* Blinking |
| | | | | | "0" (S.R.) All others |
| Blinking** Underline* | 0 | 1 | 0 | X | "0" (S.R.)* Blinking |
| | | | | | D (S.R.) All others |
| Blinking** Underline* | 0 | 1 | 1 | X | "0" (S.R.)* Blinking |
| | | | | | "1" (S.R.) All others |
| REVID Block | 0 | 0 | 0 | 0 | D (S.R.) All |
| REVID Block | 0 | 0 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 0 | 1 | X | "1" (S.R.) All |
| REVID Block | 0 | 0 | 0 | 1 | "0" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 1 | 0 | 0 | D (S.R.) All |
| REVID Block | 0 | 1 | 0 | 1 | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| REVID Block | 0 | 1 | 1 | X | "0" (S.R.) All |
| Blink** REVID Block | 0 | 0 | 0 | 0 | Alternate Normal Video/REVID At Cursor Blink Rate |
| Blink** REVID Block | 0 | 0 | 0 | 1 | |
| Blink** REVID Block | 0 | 0 | 1 | X | |
| Blink** REVID Block | 0 | 1 | 0 | 0 | |
| Blink** REVID Block | 0 | 1 | 0 | 1 | |
| Blink** REVID Block | 0 | 1 | 1 | X | |

*At Selected Row Decode **At Cursor Blink Rate

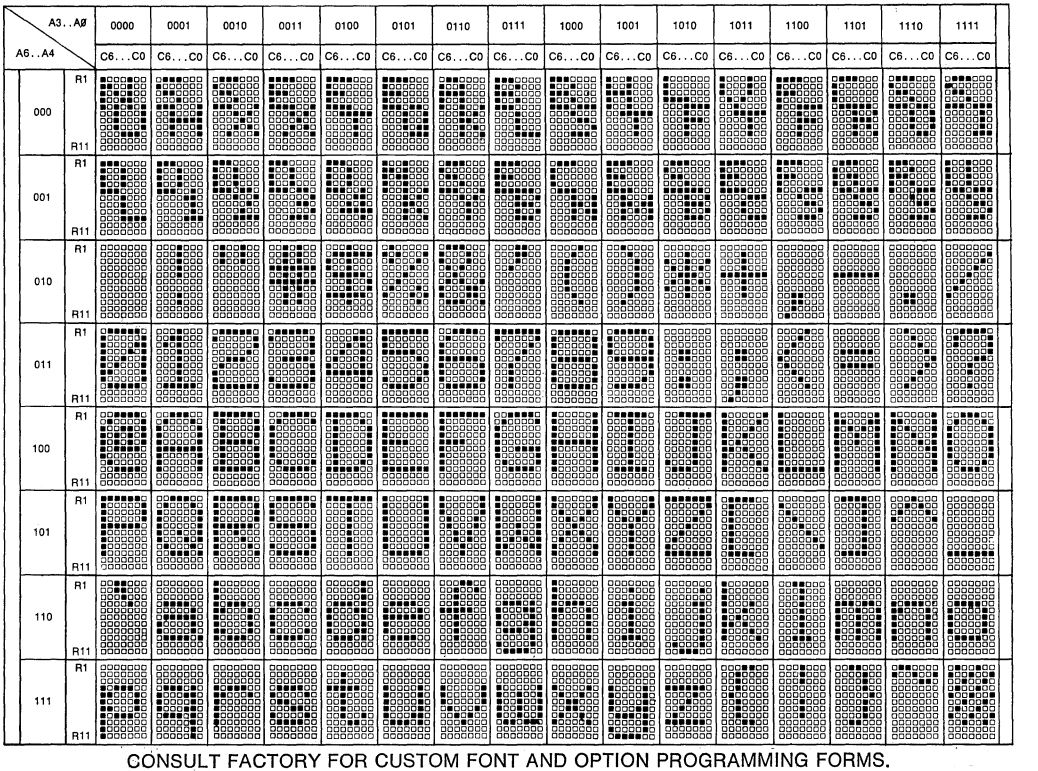
*Note:* If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

## FIGURE 5
## ROM CHARACTER BLOCK FORMAT

| | *C7 | C6 | C5 | C4 | C3 | C2 | C1 | CØ | — | — | ROWS | R3 | R2 | R1 | RØ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (ALL ZEROS) → | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | RØ | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R1 | 0 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R2 | 0 | 0 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R3 | 0 | 0 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R4 | 0 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R5 | 0 | 1 | 0 | 1 |
| 77 BITS (7 x 11 ROM) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R6 | 0 | 1 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R7 | 0 | 1 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R8 | 1 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R9 | 1 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R1Ø | 1 | 0 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R11 | 1 | 0 | 1 | 1 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R12 | 1 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R13 | 1 | 1 | 0 | 1 |
| (ALL ZEROS) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R14 | 1 | 1 | 1 | 0 |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | R15 | 1 | 1 | 1 | 1 |

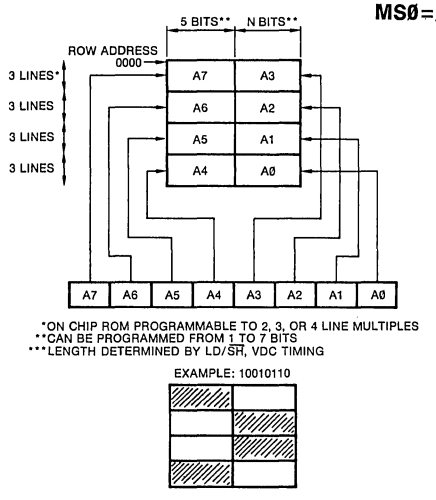
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/$\overline{SH}$, VDC TIMING)

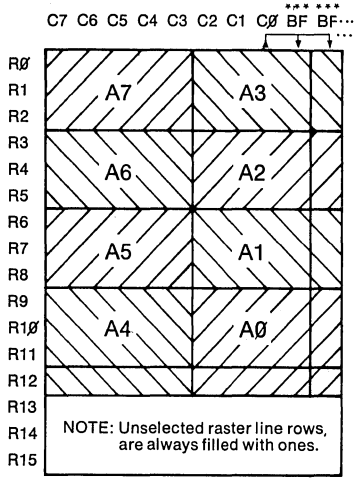
*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST




CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

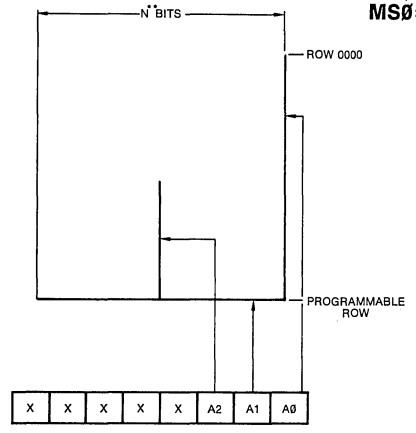
## FIGURE 1
## WIDE GRAPHICS MODE
**MSØ=Ø MS1=Ø**



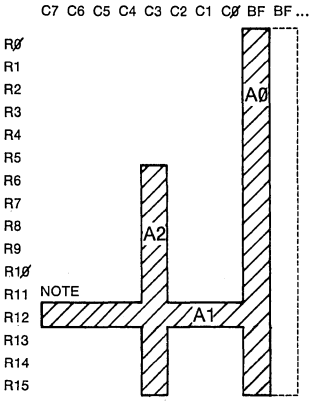




BF = back fill

## FIGURE 2
## THIN GRAPHICS MODE
**MSØ=Ø MS1=1**




X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/SR, VDC TIMING




NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

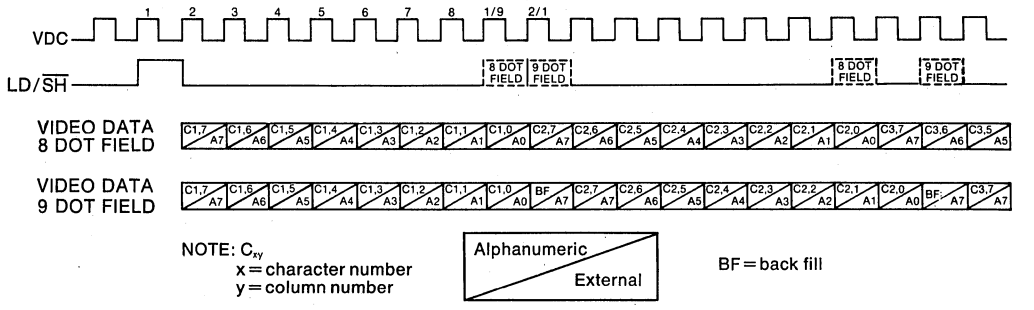
BF = back fill

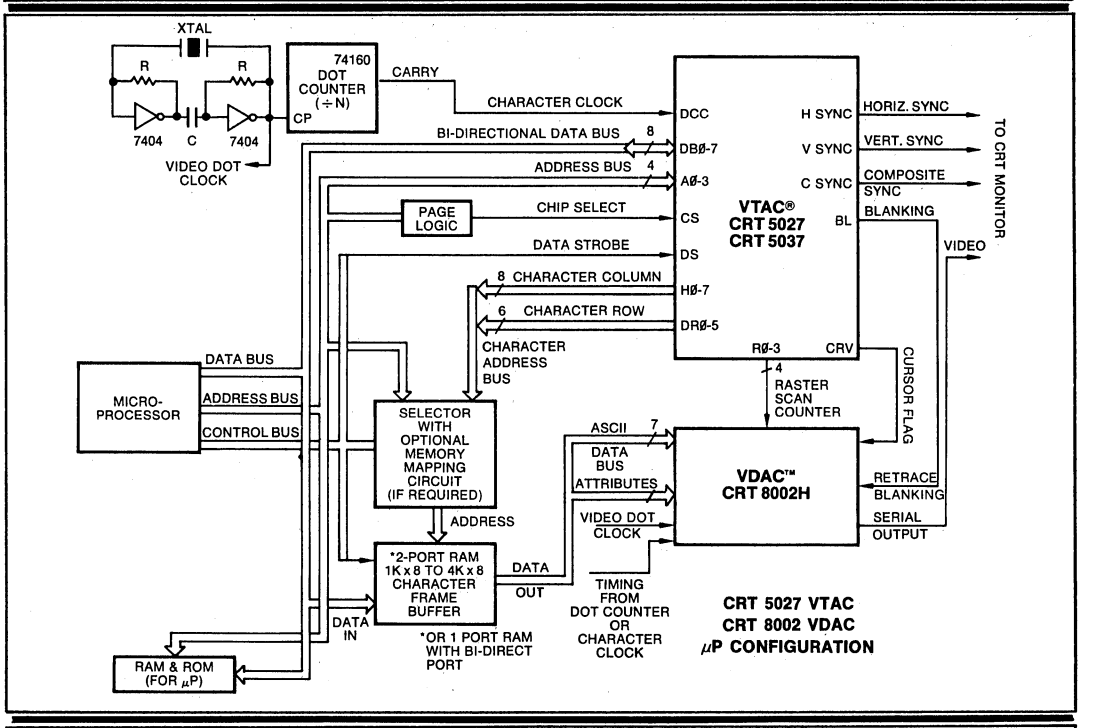
## FIGURE 3
## EXTERNAL MODE
**MSØ=1 MS1=Ø**

| | C7 | C6 | C5 | C4 | C3 | C2 | C1 | CØ | BF | BF | ... |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RØ – R15 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | AØ | A7 | A7 | ... |

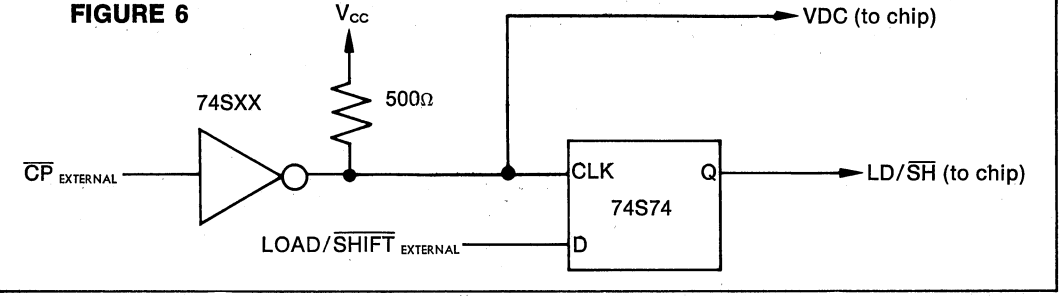
BF = back fill

## FIGURE 4 TYPICAL VIDEO OUTPUT




## FIGURE 6




STANDARD MICROSYSTEMS CORPORATION

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# CRT 8021
# CRT 8021-003
## μPC FAMILY

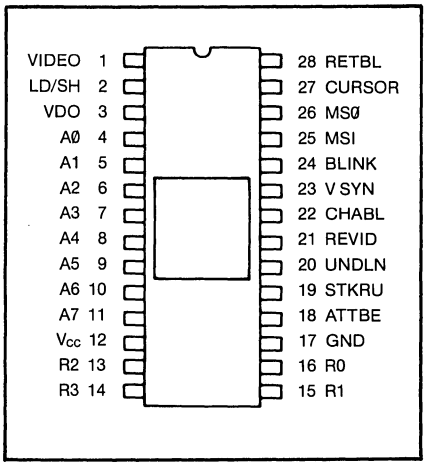
# CRT Video Attributes Controller
# Video Generator
# VAC



### FEATURES

- ☐ ON CHIP VIDEO SHIFT REGISTER
  Maximum shift register frequency—20MHz
  Maximum character clock rate—2.5MHz
- ☐ ON CHIP HORIZONTAL AND VERTICAL RETRACE VIDEO BLANKING
- ☐ ON CHIP GRAPHICS GENERATION
- ☐ ON CHIP ATTRIBUTE LOGIC-CHARACTER, FIELD
  Reverse video
  Character blank
  Character blink
  Underline
  Strike-thru
- ☐ ON CHIP BLINKING CURSOR
- ☐ ON CHIP DATA BUFFER
- ☐ ON CHIP ATTRIBUTE BUFFER
- ☐ +5 VOLT OPERATION
- ☐ TTL COMPATIBLE
- ☐ MOS N-CHANNEL SILICON-GATE COPLAMOS® PROCESS

### PIN CONFIGURATION




- ☐ COMPATIBLE WITH CRT 5027/37 VTAC® AND CRT 9007 VPAC

### GENERAL DESCRIPTION

The SMC CRT 8021 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device. It contains wide and thin graphics logic, attributes logic, a data latch, field and character attribute latch, a blinking cursor, and a high speed video shift register. The CRT 8021 VAC is a companion to SMC's CRT 5027/37 VTAC® or CRT 9007 VPAC. The CRT 8021 and a character ROM combined with either a CRT 5027/37 or a CRT 9007 comprises the major circuitry required for the display portion of a CRT video terminal.

The CRT 8021 video output may be connected directly to a CRT monitor video input. The CRT 5027/37 or CRT 9007 blanking output can be connected directly to the CRT 8021 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

A blinking cursor is available on the CRT 8021. There is a separate cursor blink rate which is twice the character blink rate and has a duty cycle of 50/50.

The CRT 8021 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions. These attributes are available in all modes.

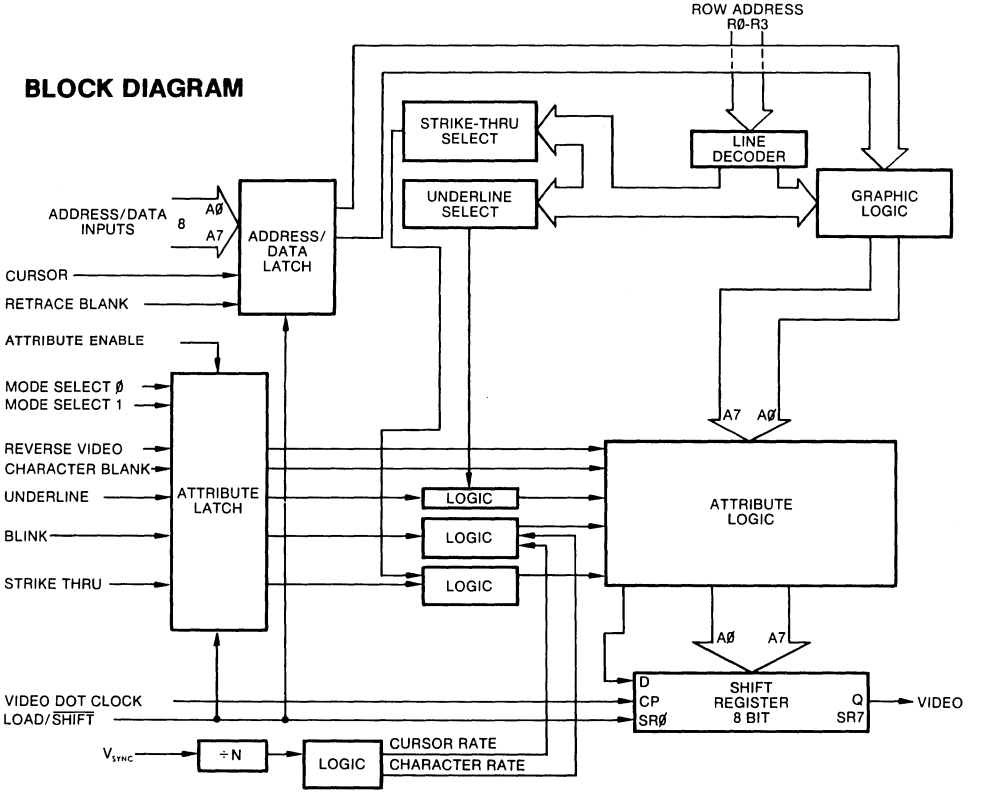
The thin graphic mode enables the user to create single line drawings and forms.

In the wide graphic mode the CRT 8021 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing 256 unique graphic symbols. Thus, the CRT 8021 can produce either alphanumeric symbols or various graphic entities depending on the mode selected. The mode can be changed on a per character basis.

The CRT 8021 is available in two versions. The CRT 8021 provides an eight-part graphic entity which fills the character block. The CRT 8021 is designed for seven dot wide, nine or eleven dot high characters in nine by twelve or ten by twelve character blocks.

The CRT 8021-003 provides a six part graphic entity for five by seven or five by nine characters in character blocks of up to seven by ten dots.

## BLOCK DIAGRAM



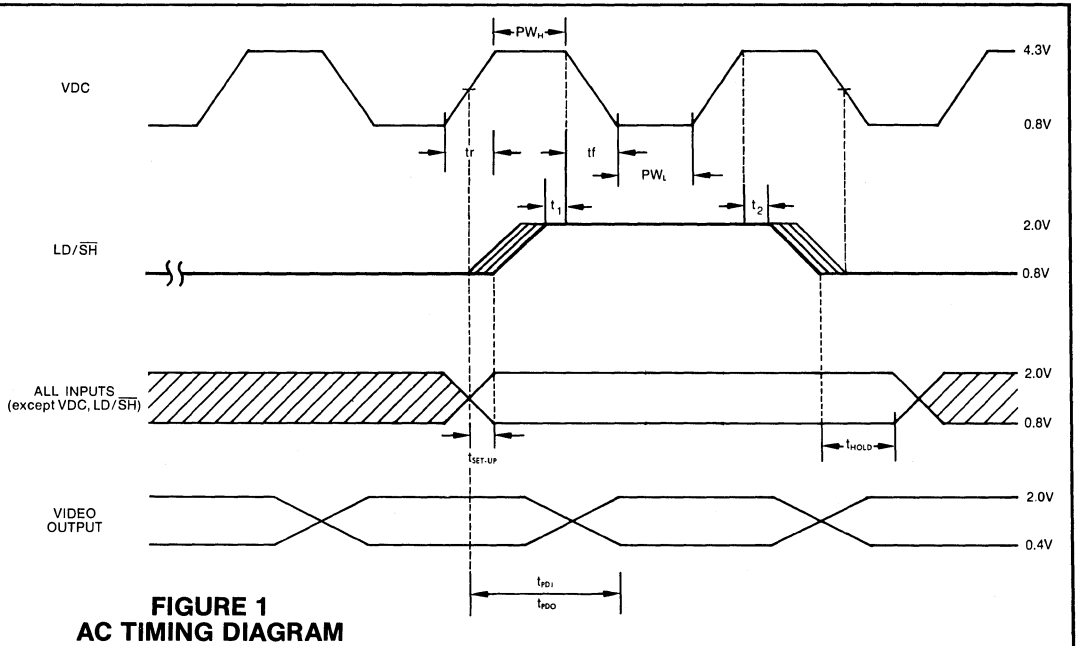




**FIGURE 1**
**AC TIMING DIAGRAM**

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | excluding VDC |
| High-level, $V_{IH}$ | 2.0 | | | V | excluding VDC |
| INPUT VOLTAGE LEVELS-CLOCK | | | | | |
| Low-level, $V_{IL}$ | | | 0.8 | V | |
| High-level, $V_{IH}$ | 4.3 | | | V | See Figure 7 |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, $V_{OL}$ | | | 0.4 | V | $I_{OL} = 0.4$ mA, 74LSXX load |
| High-level, $V_{OH}$ | 2.4 | | | V | $I_{OH} = -20\ \mu A$ |
| INPUT CURRENT | | | | | |
| Leakage, $I_L$ (Except CLOCK) | | | 10 | $\mu A$ | $0 \leq V_{IN} \leq V_{CC}$ |
| Leakage, $I_L$ (CLOCK Only) | | | 50 | $\mu A$ | $0 \leq V_{IN} \leq V_{CC}$ |
| INPUT CAPACITANCE | | | | | |
| Data | | 10 | | pF | @ 1 MHz |
| LD/$\overline{SH}$ | | 20 | | pF | @ 1 MHz |
| CLOCK | | 25 | | pF | @ 1 MHz |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 100 | | mA | |
| **A.C. CHARACTERISTICS** | | | | | |
| See Figure 6, 7 | | | | | |

| SYMBOL | PARAMETER | CRT 8021 | | UNITS |
|---|---|---|---|---|
| | | MIN. | MAX. | |
| VDC | Video Dot Clock Frequency | 1.0 | 20 | MHz |
| $PW_H$ | VDC—High Time | 15.0 | | ns |
| $PW_L$ | VDC—Low Time | 15.0 | | ns |
| $t_{CY}$ | LD/$\overline{SH}$ cycle time | 400 | | ns |
| $t_r$, $t_f$ | Rise, fall time | | 10 | ns |
| $t_{SET-UP}$ | Input set-up time | ≥0 | | ns |
| $t_{HOLD}$ | Input hold time | 15 | | ns |
| $t_{PDI}$, $t_{PDO}$ | Output propagation delay | 15 | 50 | ns |
| $t_1$ | LD/$\overline{SH}$ set-up time | 10 | | ns |
| $t_2$ | LD/$\overline{SH}$ hold time | 5 | | ns |

# DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | NAME | INPUT/ OUTPUT | FUNCTION |
|---|---|---|---|---|
| 1 | VIDEO | Video Output | O | The video output contains the dot stream for the selected row of the wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs.<br>The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4.<br>When the next Load/$\overline{\text{Shift}}$ pulse appears the next character via the attribute logic, is parallel loaded into the shift register and the cycle repeats. |
| 2 | LD/$\overline{\text{SH}}$ | Load/$\overline{\text{Shift}}$ | I | The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 1. |
| 3 | VDC | Video Dot Clock | I | Frequency at which video is shifted. |
| 4-11 | AØ-A7 | Address/Data | I | In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Mode AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments. |
| 12 | $V_{CC}$ | Power Supply | PS | +5 volt power supply. |
| 13, 14, 15, 16 | R2, R3, R1, RØ | Row Address | I | These 4 binary inputs define the row address in the current character block. |
| 17 | GND | Ground | GND | Ground |
| 18 | ATTBE | Attribute Enable | I | A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 1. |
| 19 | STKRU | Strike-Thru | I | When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). The strike-thru is a double line on rows R5 and R6 for the CRT 8021 and a single line on row R4 for the CRT 8021-003. |
| 20 | UNDLN | Underline | I | When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). The underline is a single line of R11 for the CRT 8021 and a single line on R8 for the CRT 8021-003. |
| 21 | REVID | Reverse Video | I | When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1. |
| 22 | CHABL | Character Blank | I | When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1. |
| 23 | V SYNC | V SYNC | I | This input is used as the clock input for the two on-chip blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). |
| 24 | BLINK | Blink | I | When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The character blink rate is 1.875 Hz when V SYNC = 60 Hz. |
| 25<br>26 | MS1<br>MSØ | Mode Select 1<br>Mode Select Ø | I<br>I | These 2 inputs define the three modes of operation of the CRT 8002 as follows:<br>Thin Graphics Mode — In this mode AØ-A2, (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 6.<br>Character Mode — In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3.<br>Wide Graphics Mode — In this mode the inputs AØ-A7 will define a graphic entity as described in figure 5. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory.<br>These 3 modes can be intermixed on a per character basis. |
| 27 | CURSOR | Cursor | I | When this input is enabled the cursor will be activated. The cursor will be a blinking (at 3.75 Hz when V SYNC = 60 Hz) reverse video block. In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. |
| 28 | RETBL | Retrace Blank | I | When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/$\overline{\text{Shift}}$ pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time. |

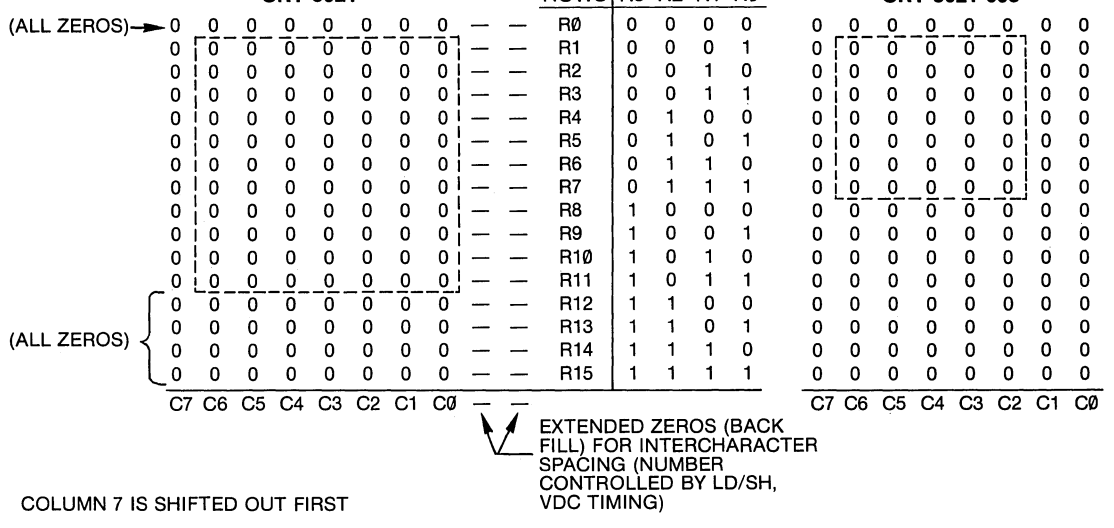
| MS1 | MSØ | MODE |
|---|---|---|
| 1 | 0 | Thin Graphics |
| 0 | 1 | Character Mode |
| 0 | 0 | Wide Graphics |

## TABLE 1

| CURSOR | RETBL | REVID | CHABL | UNDLN* | FUNCTION |
|---|---|---|---|---|---|
| X | 1 | X | X | X | "0" (S.R.) All |
| 0 | 0 | 0 | 0 | 0 | D (S.R.) All |
| 0 | 0 | 0 | 0 | 1 | "1" (S.R.)* |
| | | | | | D (S.R.) All others |
| 0 | 0 | 0 | 1 | X | "0" (S.R.) All |
| 0 | 0 | 1 | 0 | 0 | $\overline{D}$ (S.R.) All |
| 0 | 0 | 1 | 0 | 1 | "0" (S.R.)* |
| | | | | | $\overline{D}$ (S.R.) All others |
| 0 | 0 | 1 | 1 | X | "1" (S.R.) All |
| Blink** REVID Block | 0 | 0 | 0 | 0 | Alternate Normal Video/REVID At Cursor Blink Rate |
| Blink** REVID Block | 0 | 0 | 0 | 1 | |
| Blink** REVID Block | 0 | 0 | 1 | X | |
| Blink** REVID Block | 0 | 1 | 0 | 0 | |
| Blink** REVID Block | 0 | 1 | 0 | 1 | |
| Blink** REVID Block | 0 | 1 | 1 | X | |

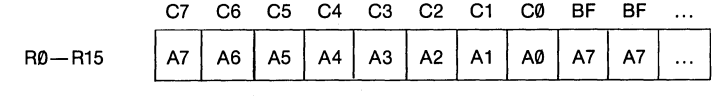
*At Selected Row Decode **At Cursor Blink Rate
*Note:* If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate

## FIGURE 2
## TYPICAL CHARACTER MODE BLOCK FORMATS



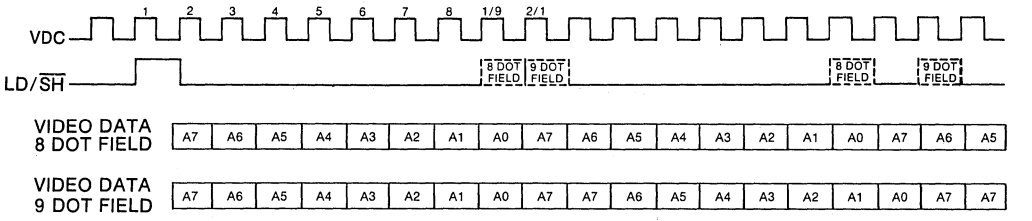

*Note:* Dotted line shows typical character display area.

## FIGURE 3
## CHARACTER MODE
**MSØ = 1 MS1= Ø**

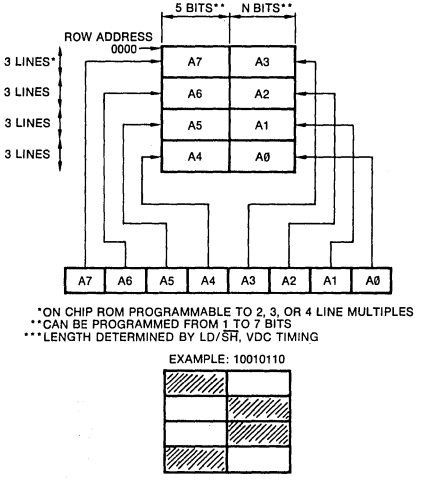



BF = back fill

## FIGURE 4. TYPICAL VIDEO OUTPUT—CHARACTER MODE




## FIGURE 5
## WIDE GRAPHICS MODE
**MSØ = Ø MS1 = Ø**

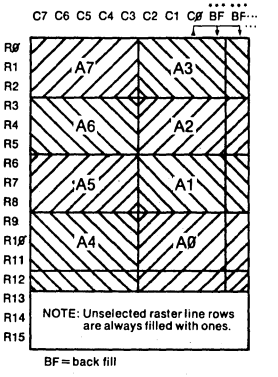



*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/SH, VDC TIMING

EXAMPLE: 10010110

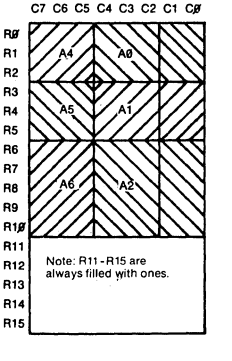


### CRT 8021

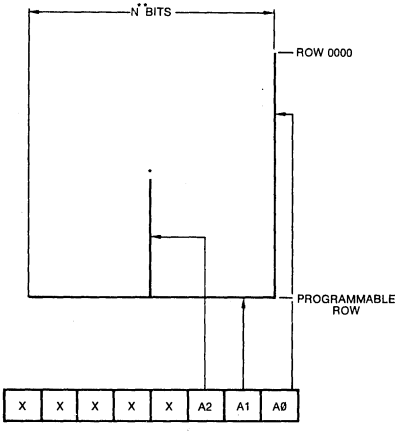



BF = back fill

### CRT 8021-003

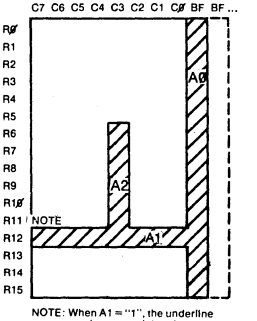



## FIGURE 6
## THIN GRAPHICS MODE
**MSØ = Ø MS1 = 1**




X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/SH, VDC TIMING

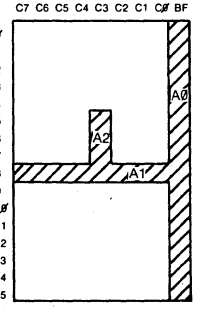
### CRT 8021



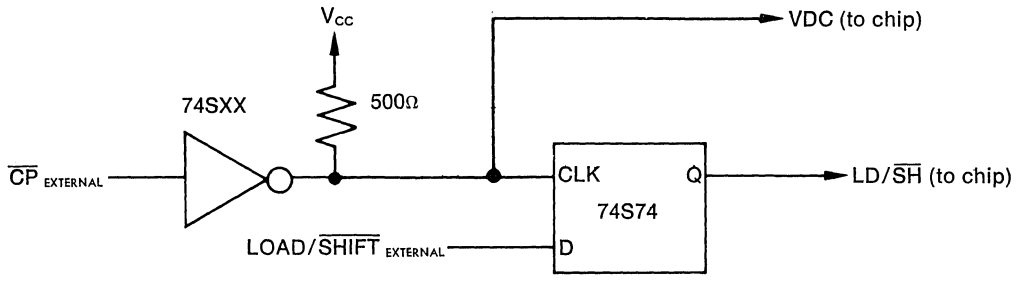

NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

BF = back fill

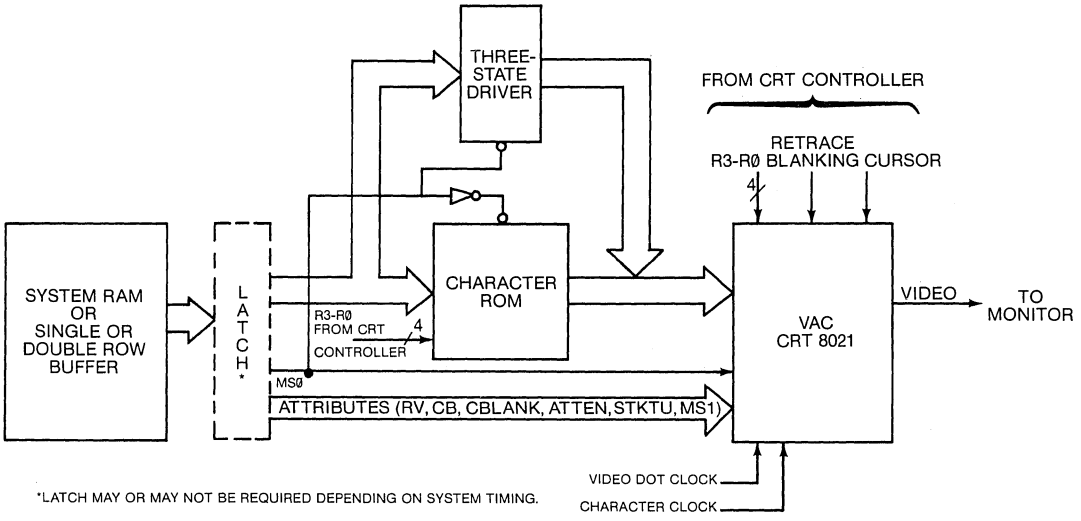
### CRT 8021-003



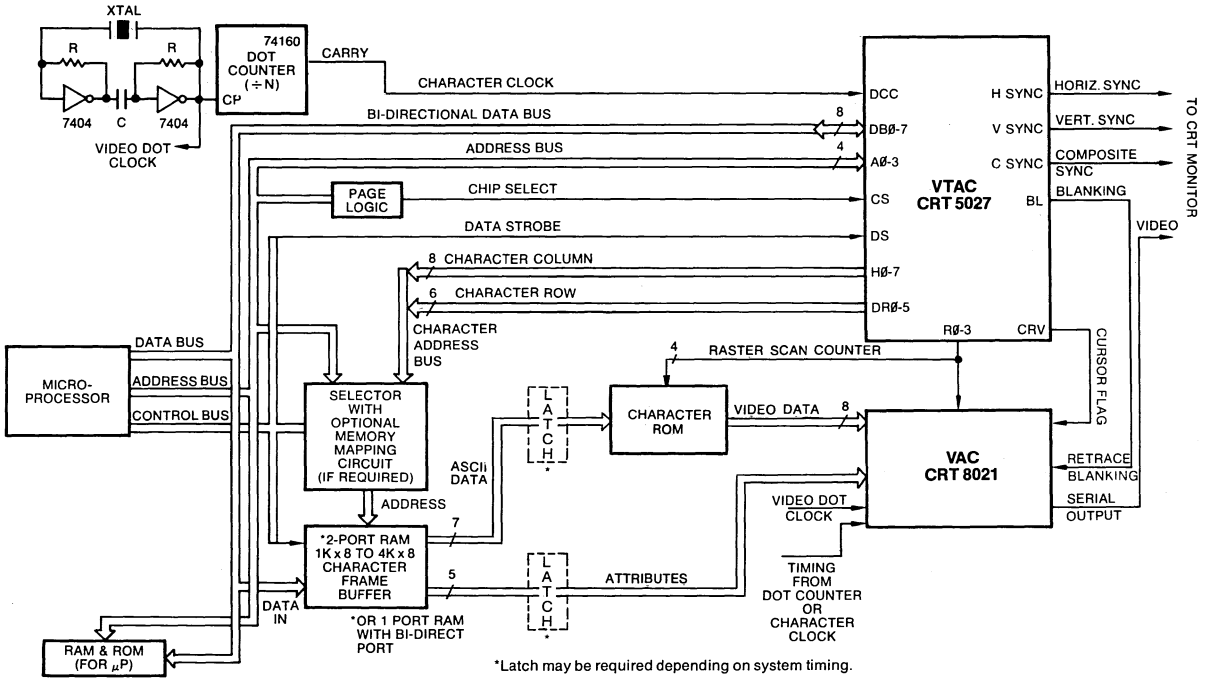
## FIGURE 7




## FIGURE 8
## TYPICAL CRT 8021 CONFIGURATION FOR COMBINED CHARACTER AND GRAPHICS MODES




*LATCH MAY OR MAY NOT BE REQUIRED DEPENDING ON SYSTEM TIMING.




*Latch may be required depending on system timing.

**FIGURE 9. CRT 8021 TYPICAL μP CONFIGURATION (CHARACTER MODE ONLY)**

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

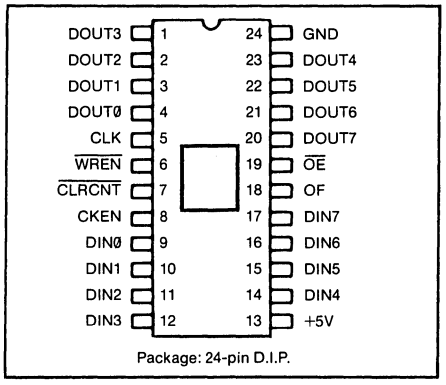
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge NY 11788
(516) 273-3100 TWX 510 227-8898

# Single Row Buffer
# SRB

## FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 3.3MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

## PIN CONFIGURATION




Package: 24-pin D.I.P.

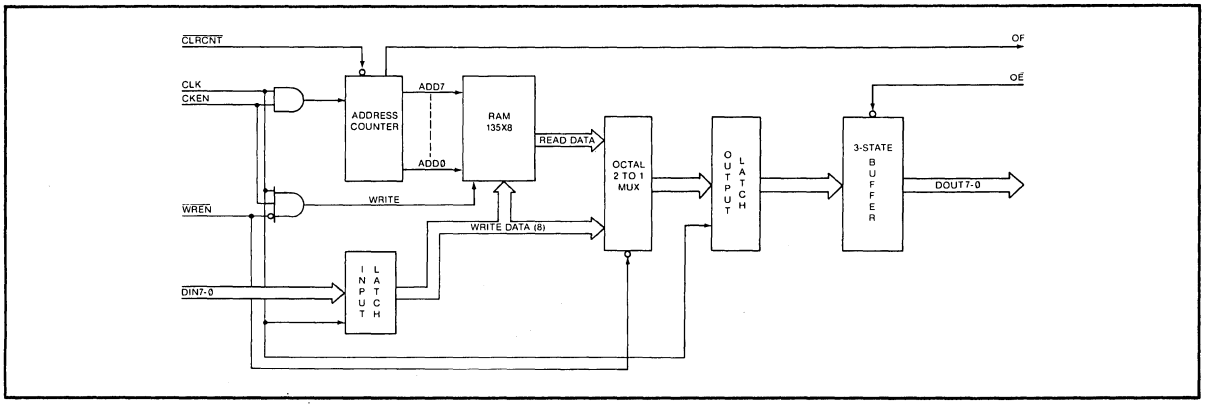
## APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION V

## GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1-4 | DATA OUTPUTS | DOUT3-DOUTØ | Data Outputs from the internal output latch. |
| 5 | CLOCK | CLK | Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter. |
| 6 | WRITE ENABLE | $\overline{\text{WREN}}$ | When $\overline{\text{WREN}}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM. |
| 7 | CLEAR COUNTER | $\overline{\text{CLRCNT}}$ | A negative transition on $\overline{\text{CLRCNT}}$ clears the RAM address counter. $\overline{\text{CLRCNT}}$ is normally asserted low near the beginning of each scan line. |
| 8 | CLOCK ENABLE | CKEN | When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM. |
| 9-12 | DATA INPUTS | DINØ-DIN3 | Data Inputs from system memory. |
| 13 | POWER SUPPLY | $V_{CC}$ | +5 Volt supply. |
| 14-17 | DATA INPUTS | DIN4-DIN7 | Data Inputs from system memory. |
| 18 | OVERFLOW FLAG | OF | This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip. |
| 19 | OUTPUT ENABLE | $\overline{\text{OE}}$ | When $\overline{\text{OE}}$ is low, the data outputs DOUTØ-DOUT7 are enabled. When $\overline{\text{OE}}$ is high, DOUTØ-DOUT7 present a high impedance state. |
| 20-23 | DATA OUTPUTS | DOUT7-DOUT4 | Data Outputs from the internal output latch. |
| 24 | GROUND | GND | Ground. |

## OPERATION

For CRT operation, the Write Enable ($\overline{\text{WREN}}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{\text{CLRCNT}}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{\text{CLRCNT}}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{\text{WREN}}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

## MAXIMUM GUARANTEED RATINGS*

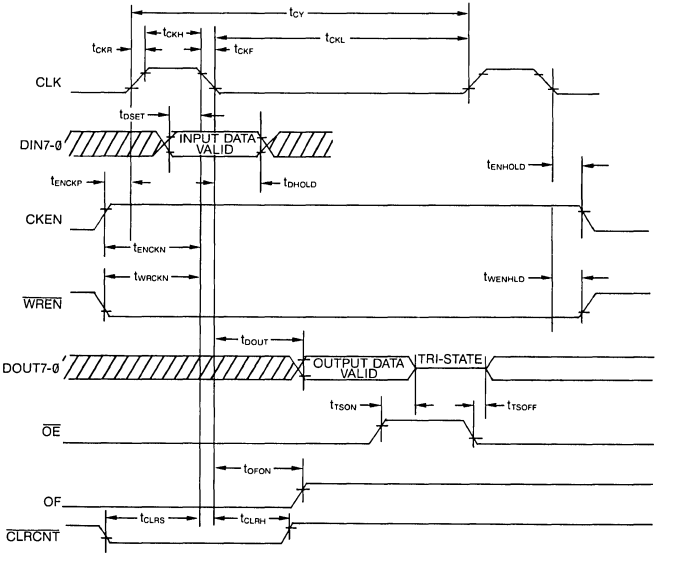
Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... -55° C to + 150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

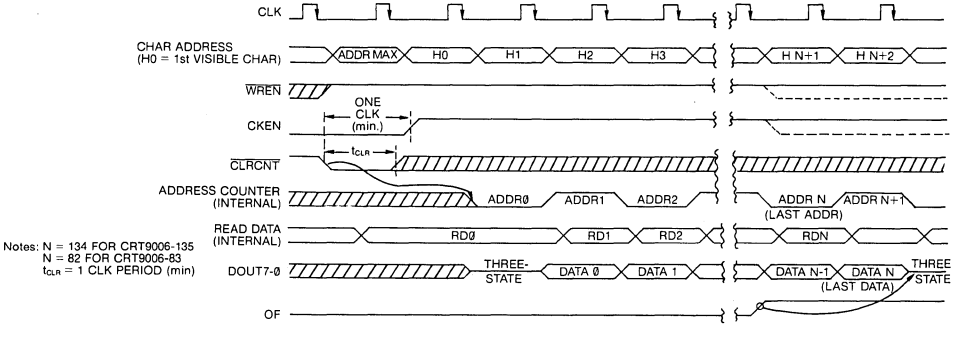
## ELECTRICAL CHARACTERISTICS ($T_A = 0°$ C to 70° C, $V_{CC} = +5 \pm 5\%$, unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| Input Voltage Levels | | | | | |
| Low Level $V_{IL}$ | | | 0.8 | V | |
| High Level $V_{IH}$ | 2.0 | | | V | |
| Output Voltage Levels | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL} = 2mA$ |
| High Level $V_{OH}$ | 2.4 | | | V | $I_{OH} = -100\mu A$ |
| Input Current Leakage, $I_{IL}$ | | | 10 | $\mu A$ | $0 \leq V_{IN} \leq V_{CC}$ |
| Output '1' Leakage | | | 10 | $\mu A$ | |
| Output '0' Leakage (Off State) | | | 10 | $\mu A$ | |
| Input Capacitance | | | | | |
| CLK | | 30 | 45 | pF | |
| All other inputs | | 10 | 15 | pF | |
| Power Supply Current | | | | | |
| $I_{CC}$ (SRB-135) | | | 115 | mA | |
| $I_{CC}$ (SRB-83) | | | 100 | mA | |
| **AC CHARACTERISTICS** | | | | | |
| $t_{cy}$ | | | | | |
| (SRB135) | 300 | 250 | | ns | |
| (SRB83) | 400 | 330 | | ns | |
| $t_{CKL}$ | | | | | |
| (SRB135) | 240 | 190 | DC | ns | |
| (SRB83) | 320 | 250 | DC | ns | |
| $t_{CKH}$ | | | | | |
| (SRB135) | 28 | | 5000 | ns | |
| (SRB83) | 34 | | 5000 | ns | |
| $t_{CKR}$ | | | | | |
| (SRB135) | | | 10 | ns | $t_{CKH} = 28ns$ |
| (SRB83) | | | 10 | ns | $t_{CKH} = 34ns$ |
| $t_{CKF}$ | | | | | |
| (SRB135) | | | 10 | ns | $t_{CKL} = 240ns$ |
| (SRB83) | | | 10 | ns | $t_{CLK} = 320ns$ |
| $t_{DSET}$ | 65 | | | ns | |
| $t_{DHOLD}$ | 5 | | | ns | |
| $t_{ENCKP}$ | 0 | | | ns | |
| $t_{ENCKN}$ | | | | | |
| (SRB135) | 100 | | | ns | |
| (SRB83) | 125 | | | ns | |
| $t_{ENHOLD}$ | 0 | | | ns | |
| $t_{WRCKN}$ | | | | | |
| (SRB135) | 100 | | | ns | |
| (SRB83) | 125 | | | ns | |
| $t_{WENHLD}$ | 0 | | | ns | |
| $t_{DOUT}$ | | | 175 | ns | $C_L = 50pF$ |
| $t_{TSON}$ | | | 175 | ns | |
| $t_{TSOFF}$ | | | 175 | ns | |
| $t_{OFON}$ | | | 175 | ns | $C_L = 30pF$ |
| $t_{CLRS}$ | | | | | |
| (SRB135) | 100 | | | ns | |
| (SRB83) | 125 | | | ns | |
| $t_{CLRH}$ | 0 | | | ns | |

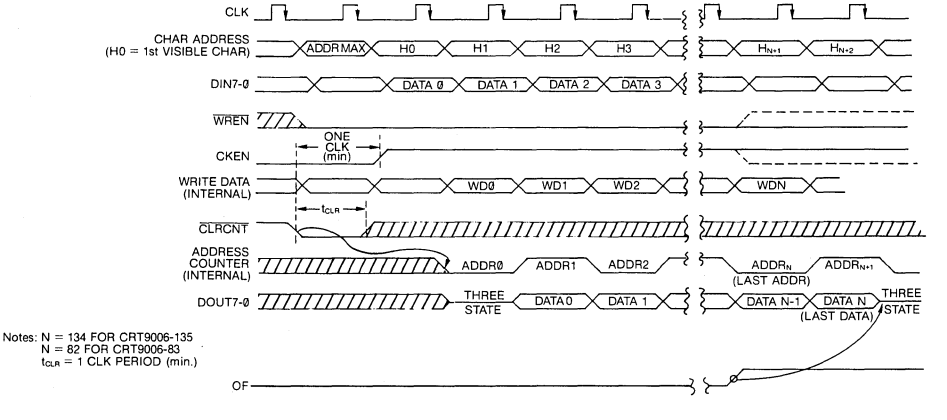
## FIGURE 1: AC CHARACTERISTICS




## FIGURE 2: SINGLE ROW BUFFER READ TIMING




## FIGURE 3: SINGLE ROW BUFFER WRITE TIMING



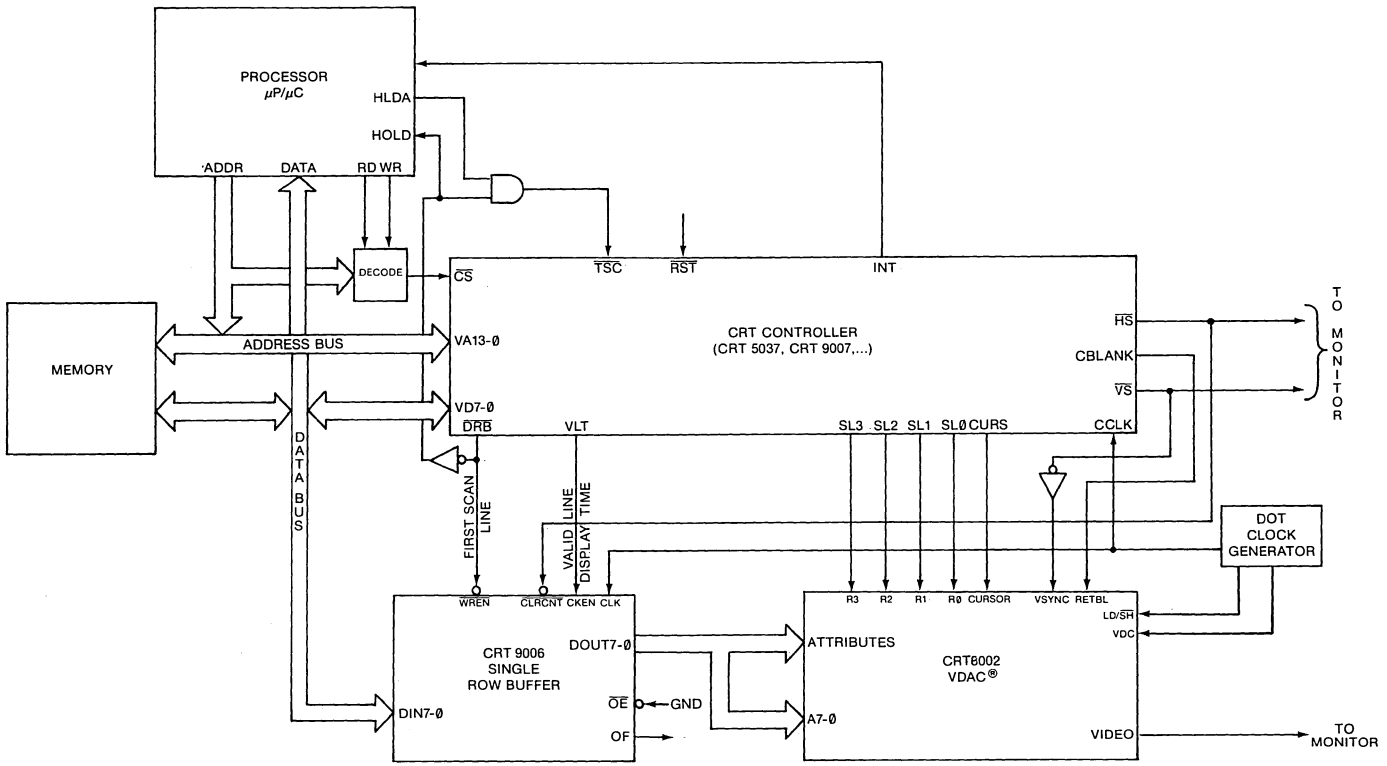
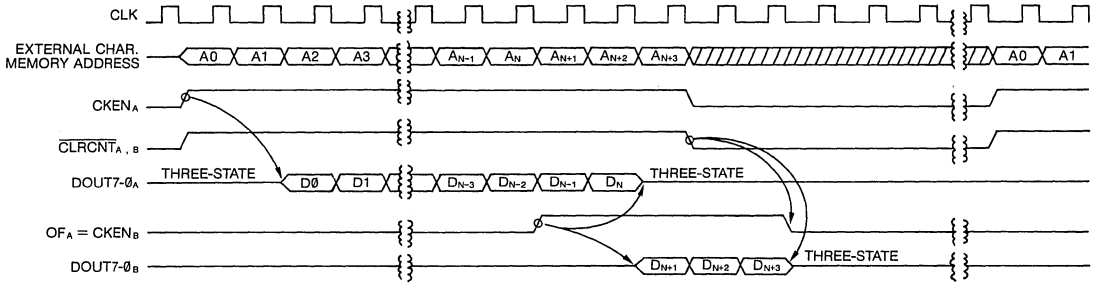


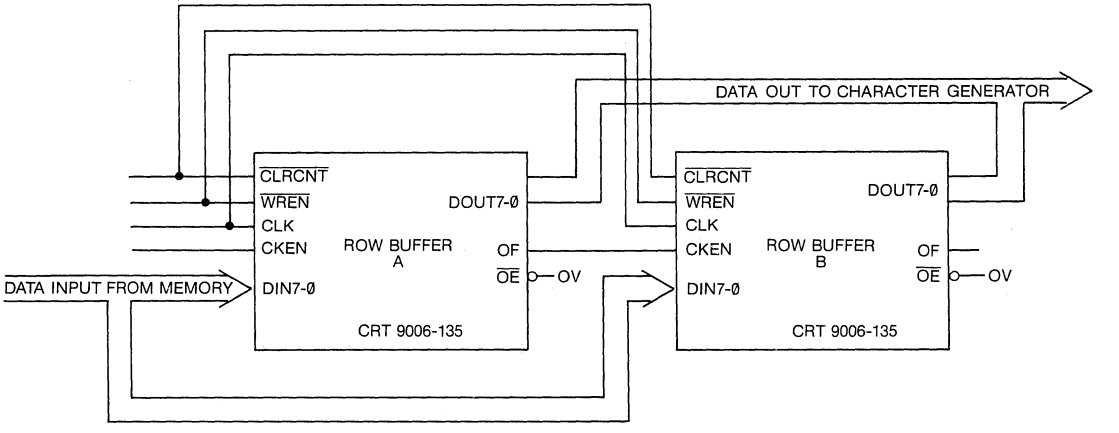

**FIGURE 2: TYPICAL CRT CONTROLLER CONFIGURATION WITH SINGLE ROW BUFFER**

## FIGURE 4:
## TYPICAL READ TIMING FOR SRB CASCADED CONFIGURATION




Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
EXAMPLE IS FOR N+3 CHARACTERS TOTAL
A, B REFER TO DEVICES A&B IN FIGURE 5

## FIGURE 5:
## TYPICAL CASCADE OF SINGLE ROW BUFFERS—270 BYTES TOTAL




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 · TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# CRT 9007A
# CRT 9007B
# CRT 9007C
## μPC FAMILY

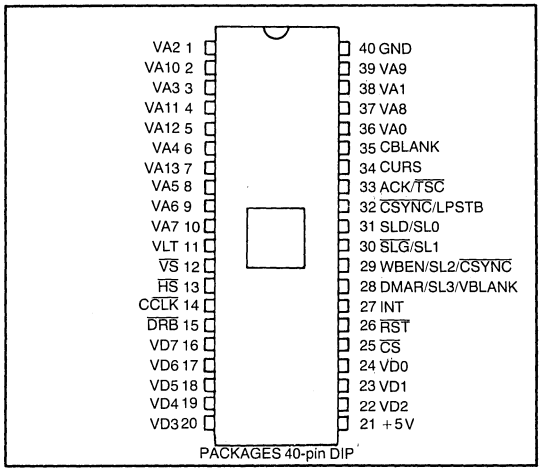
# CRT Video Processor and Controller
# VPAC™



## FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch—Horizontal (Negative or Positive)
  - —Vertical
  - Sync Width—Horizontal (1-128 Character Times)
  - —Vertical (2-256 Scan Lines)
  - Back Porch—Horizontal
  - —Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

## PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

## GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

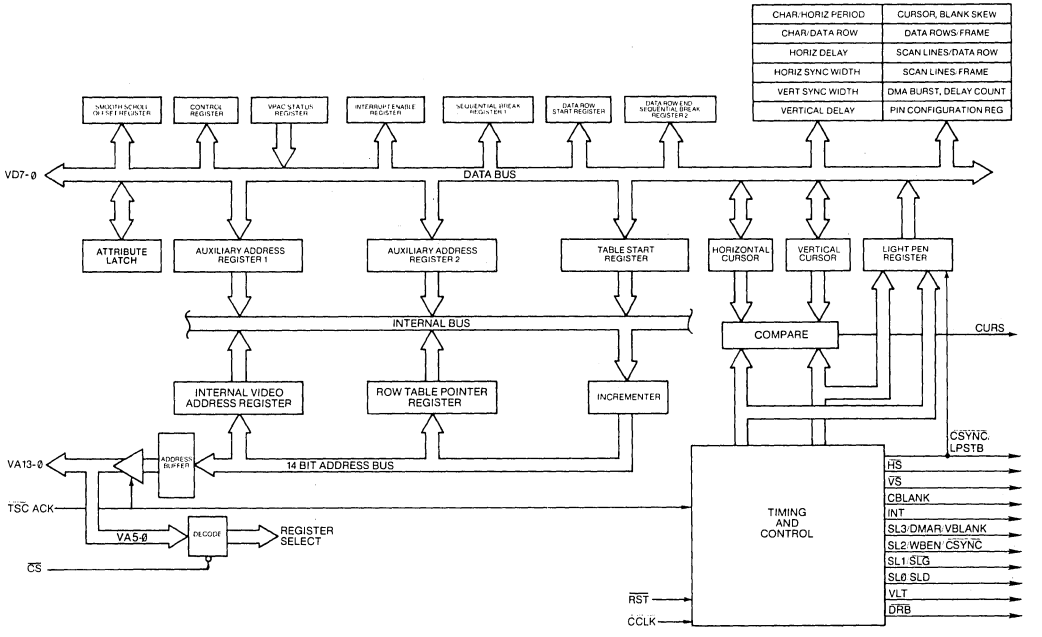



**FIGURE 1: CRT 9007 BLOCK DIAGRAM**

# DESCRIPTION OF PIN FUNCTIONS

**PROCESSOR INTERFACE:**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36 | Video Address 13-0 | VA13-VA0 | These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional.<br>—Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times.<br>—Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times.<br>—Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state.<br>If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register. |
| 16, 17, 18, 19, 20, 22, 23, 24 | Video Data 7-0 | VD7-VD0 | Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode. |
| 25 | Chip strobe | $\overline{CS}$ | Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing. |
| 26 | Reset | $\overline{RST}$ | Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition. |
| 27 | Interrupt | INT | Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read. |

# DESCRIPTION OF PIN FUNCTIONS CONT'D

**CRT INTERFACE:**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 11 | Visible Line Time | VLT | Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer. |
| 12 | Vertical Sync | $\overline{VS}$ | Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$). |
| 13 | Horizontal Sync | $\overline{HS}$ | Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$). |
| 14 | Character Clock | $\overline{CCLK}$ | Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation. |
| 15 | Data Row Boundary | $\overline{DRB}$ | Output: this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra $\overline{DRB}$ signal which will become active during the first scan line of the vertical retrace interval. |
| 34 | Cursor | CURS | Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows.<br>CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details. |
| 35 | Composite Blank | CBLANK | Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT. |

**USER SELECTABLE PINS: (see Tables 4 and 5)**

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 28, 29, 30, 31 | Scan Line 3-Scan Line 0 | SL3-SL0 | Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SL0 are the most and least significant bits respectively. |
| 28 | Direct Memory Access Request | DMAR | Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation. |
| 28 | Vertical Blank | VBLANK | Output; this signal is active high only during the vertical retrace period. |
| 29 | Write Buffer Enable | WBEN | Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration. |
| 29 or 32 | Composite Sync | $\overline{CSYNC}$ | Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats. |
| 30 | Scan Line Gate | $\overline{SLG}$ | Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with SLD (pin 31), allows scan line information to be loaded serially into an external shift register. |
| 31 | Scan Line Data | SLD | Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row.<br>The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing. |
| 32 | Light Pen Strobe | LPSTB | Input; this signal strobes the current row/column position into the light pen register at its positive transition. |
| 33 | Acknowledge | ACK | Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time. |
| 33 | Three State Control | $\overline{TSC}$ | Input; this signal, when active low, places VA13-VA0 in their high impedance state. |

## Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately $[(N-1)/N] \times 100$ where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

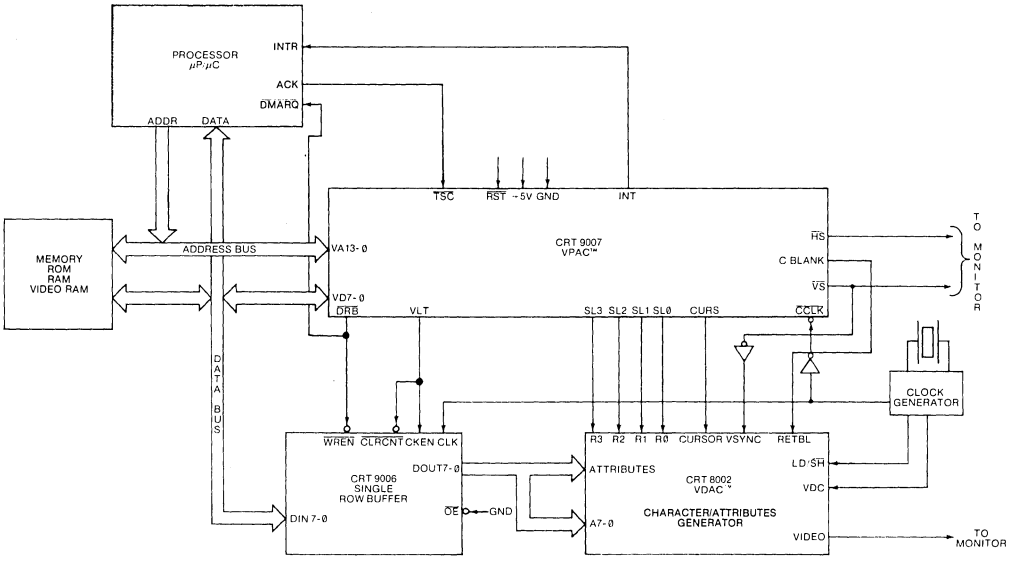



**FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER**

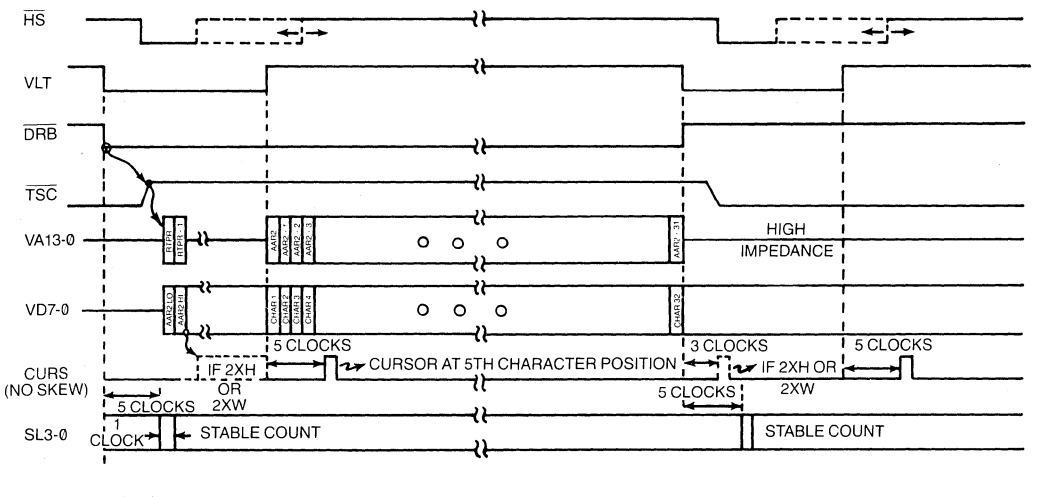



**FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)**

## Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

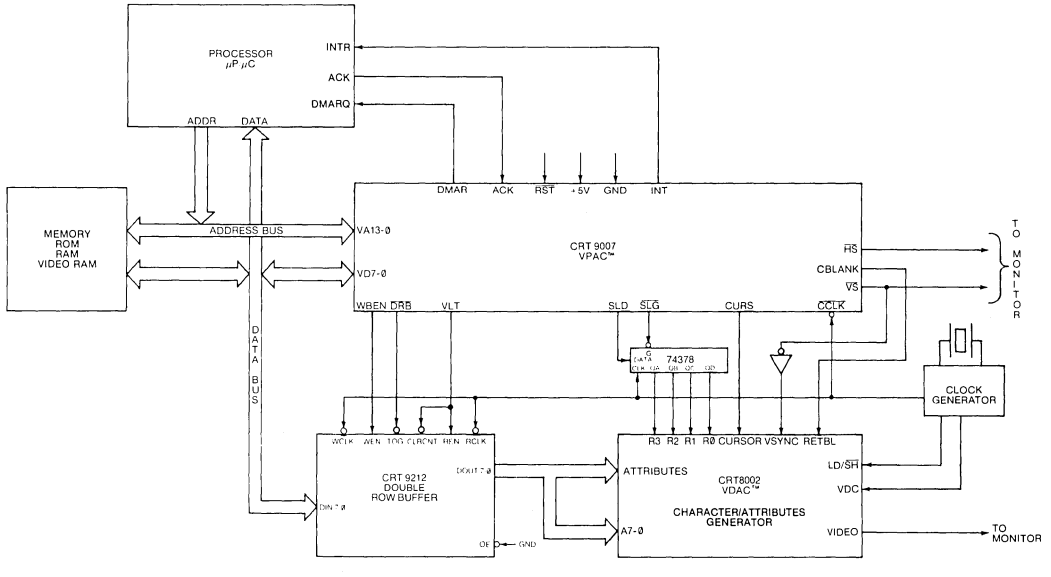



**FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER**

SECTION V

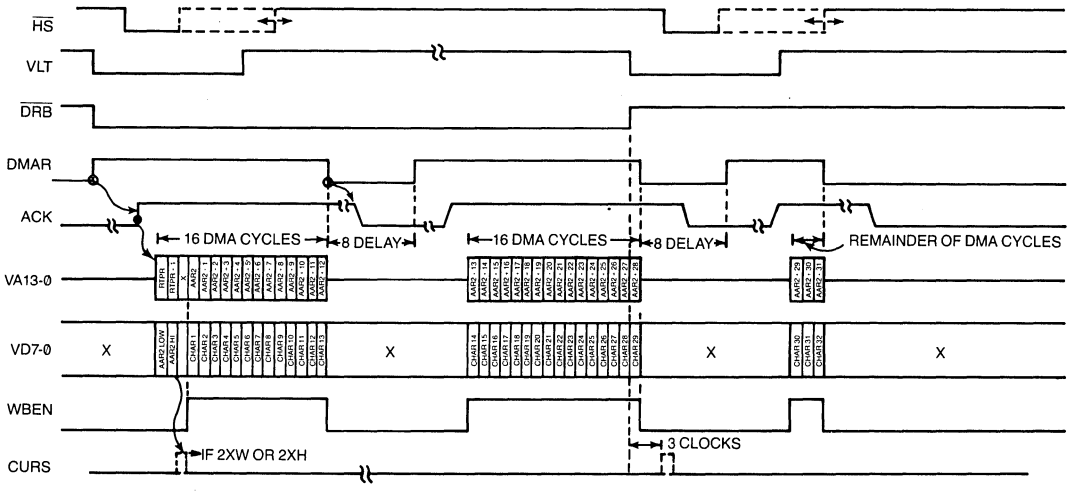



**FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)**

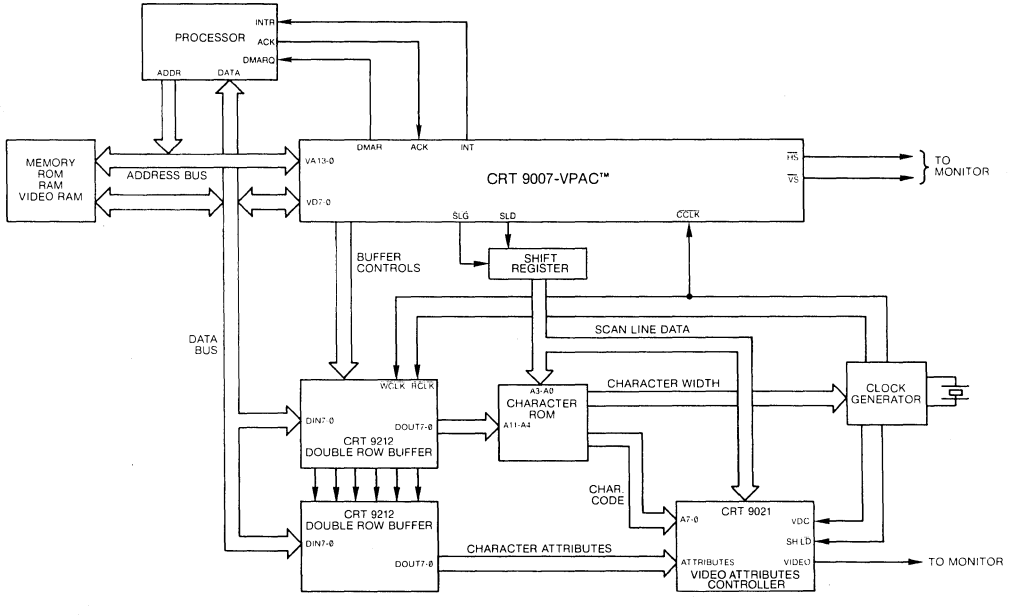



**FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY**

## Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

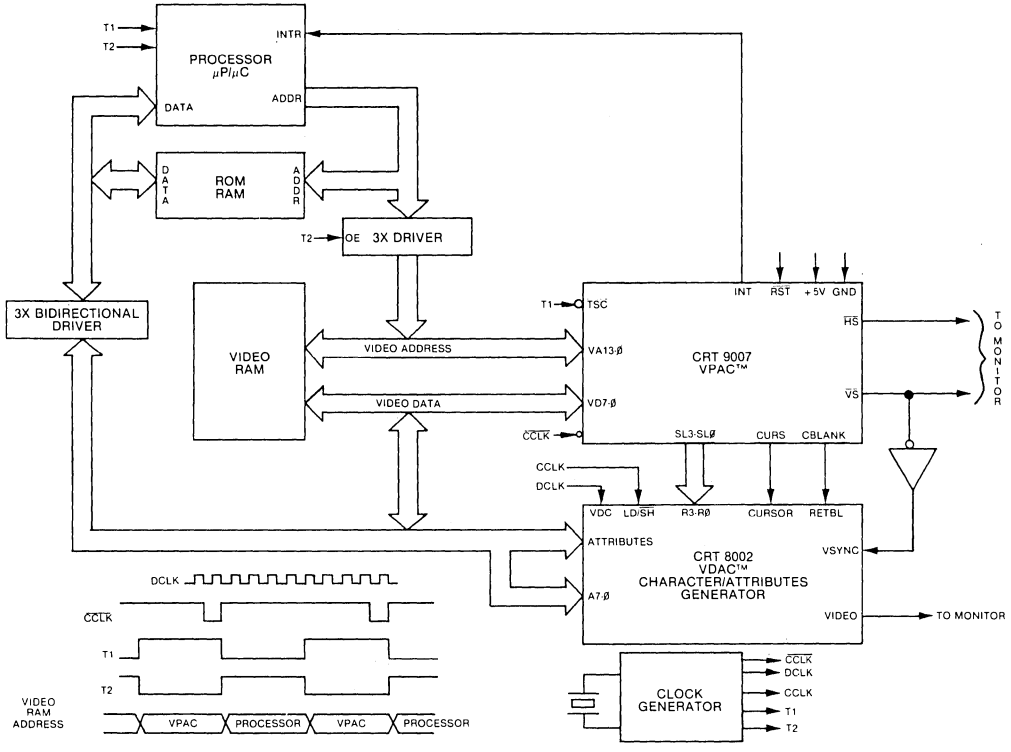



FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

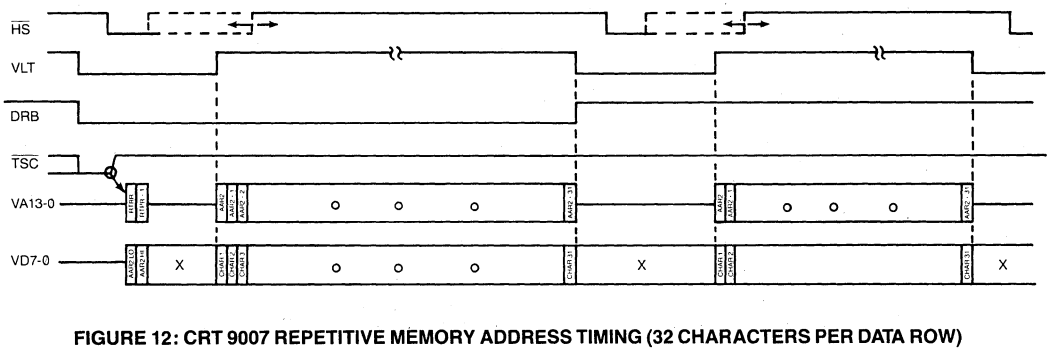



FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

## Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

| Memory Address (typ) | Memory Data (8 bits) |
|---|---|
| 0D00 | Attribute 0 |
| 0D01 | Character 0 |
| 0D02 | Attribute 1 |
| 0D03 | Character 1 |
| 0<br>0<br>0 | 0<br>0<br>0 |
| 2N | Attribute N |
| 2N + 1 | Character N |

**Figure 13: Attribute Assemble Memory Organization**

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

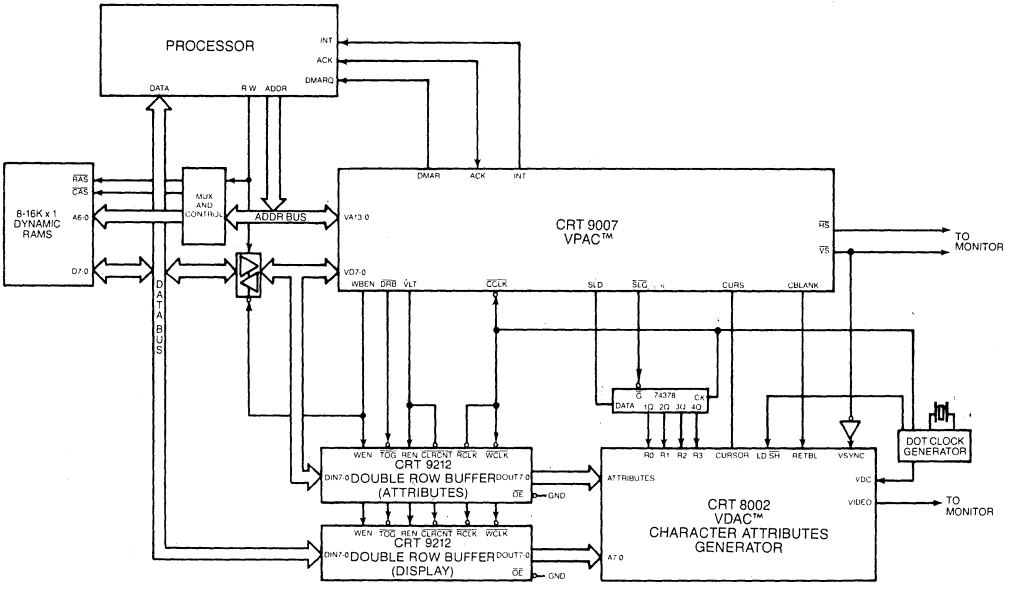
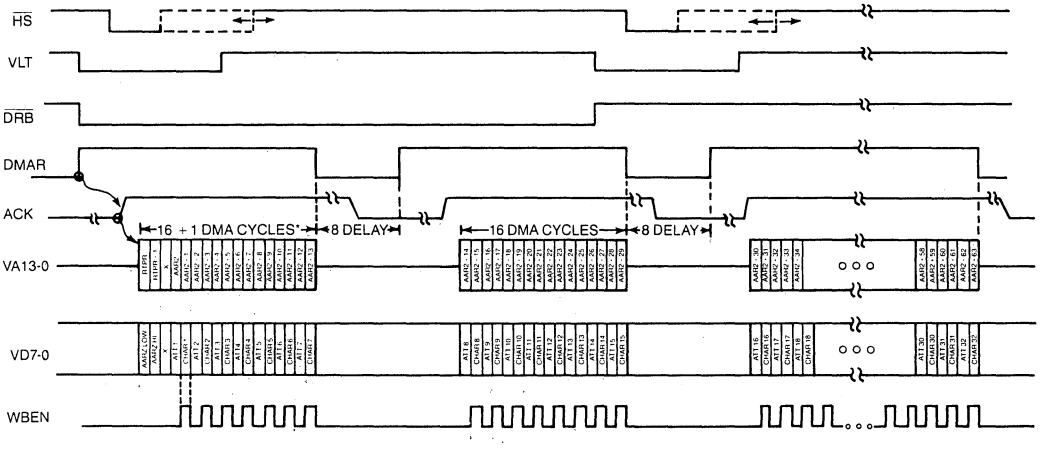



**FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE**

## Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).




*DMA cycles will always end at a character fetch

**FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)**

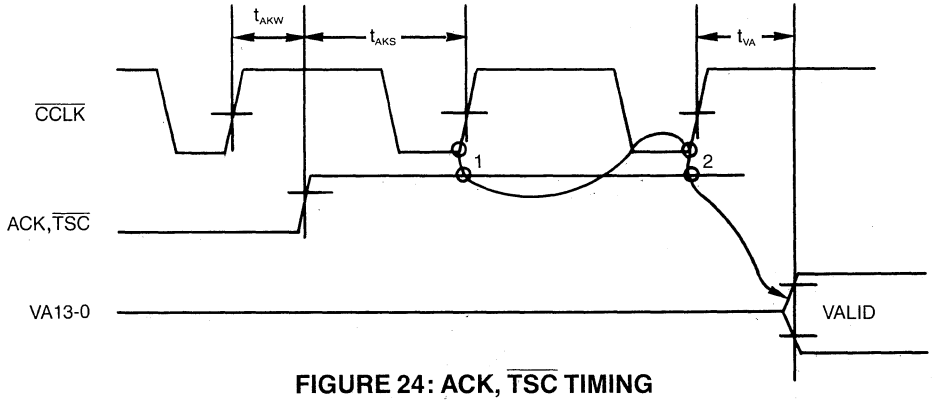



**FIGURE 24: ACK, $\overline{TSC}$ TIMING**

SECTION V

## Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

## Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

## Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

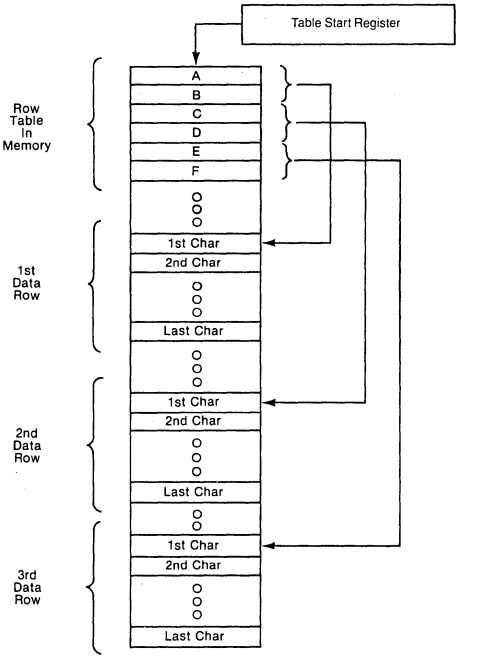



**FIGURE 16: CONTIGUOUS ROW TABLE ADDRESS FORMAT**

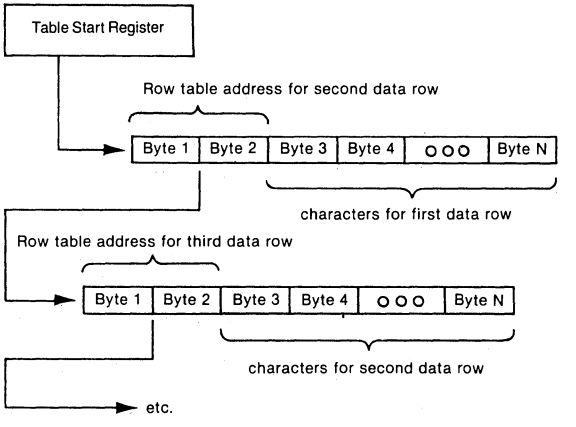



**FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT**

## Sequential Addressing[1]

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

[1]SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

| Data Row | Address range | |
|---|---|---|
| 0 | 1000 to 104 F | |
| 1 | 1050 to 109F | |
| 2 | 10A0 to 10EF | |
| 3 | 2000 to 204F | (Break 1) |
| 4 | 2050 to 209F | |
| 5 | 20A0 to 20EF | |
| 6 | 0800 to 084F | (Break 2) |
| 7 | 0850 to 089F | |
| 8 | 08A0 to 08EF | |
| | O | |
| | O | |
| | O | |

**Figure 18: Sequential Addressing Example With Two Breaks**

## Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or $\overline{SLG}$, $\overline{SLD}$) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 $\overline{CCLK}$'s after VLT trailing edge and stays active for exactly 1 $\overline{CCLK}$ assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 $\overline{CCLK}$'s to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

| OPERATION MODE | ADDRESSING MODE | |
|---|---|---|
| | Row Driven (linked list or contiguous) | Sequential |
| Repetitive Memory Addressing | 1 CCLK after high byte of row table read | 1 CCLK after TSC leading edge |
| Single row buffer | 1 CCLK after high byte of row table read | 1 CCLK after TSC leading edge |
| Double row buffer | 1 CCLK after high byte of row table read | 1 CCLK after ACK leading edge |

**Table 1: Double Height/Width CURS activation for top scan line of new data row.**

| OPERATION MODE | ADDRESSING MODE | |
|---|---|---|
| | Row driven (linked list or contiguous) | Sequential |
| Repetitive Memory Addressing | at the leading edge of VLT | at the leading edge of VLT |
| Single row buffer | at the leading edge of VLT | at the leading edge of VLT |
| Double row buffer | 1 CCLK after leading edge of CURS | 1 CCLK after leading edge of CURS |

**Table 2: Double Height/Width CURS deactivation for top scan line of new data row.**

## PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

### HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

### CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

### CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

### HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

### HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER 0 rounded to the smallest even integer.

## VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

### VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

### VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

### VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

### SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

### SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

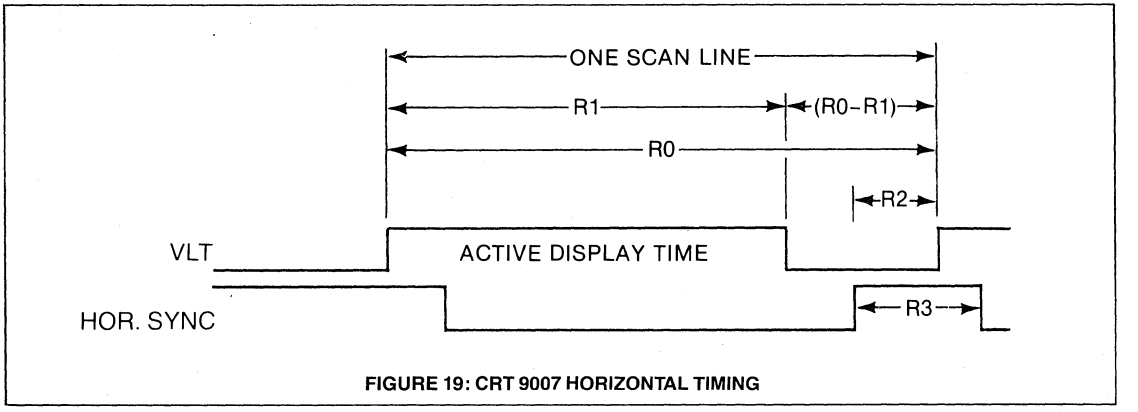



**FIGURE 19: CRT 9007 HORIZONTAL TIMING**

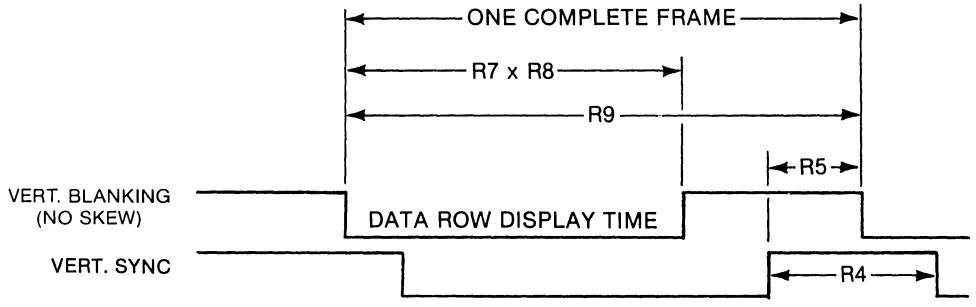



**FIGURE 20: CRT 9007 VERTICAL TIMING**

## PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

| REGISTER R6 BITS | | CRT 9007 PIN NUMBER | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 28 | 29 | 30 | 31 | 32 | 33 |
| 0 | 1 | DMAR | WBEN | $\overline{SLG}$ | SLD | $\overline{CSYNC}$ | ACK |
| 1 | 1 | DMAR | WBEN | $\overline{SLG}$ | SLD | LPSTB | ACK |
| 0 | 0 | NOT PERMITTED | | | | | |
| 1 | 0 | NOT PERMITTED | | | | | |

**Table 4: Pin configuration for double row buffer and attribute assemble modes.**

| REGISTER 6 BITS | | CRT 9007 PIN NUMBER | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 28 | 29 | 30 | 31 | 32 | 33 |
| 0 | 0 | SL3 | SL2 | SL1 | SL0 | $\overline{CSYNC}$ | $\overline{TSC}$ |
| 1 | 0 | SL3 | SL2 | SL1 | SL0 | LPSTB | $\overline{TSC}$ |
| 1 | 1 | VBLANK | $\overline{CSYNC}$ | $\overline{SLG}$ | SLD | LPSTB | $\overline{TSC}$ |
| 0 | 1 | NOT PERMITTED | | | | | |

**Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.**

## DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N+1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

## CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

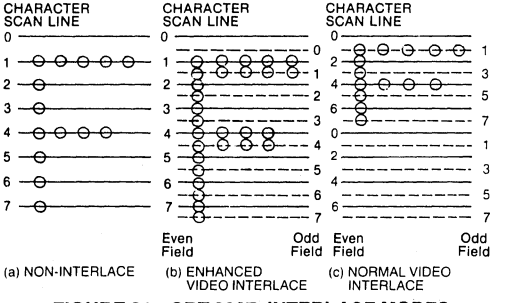



**FIGURE 21: CRT 9007 INTERLACE MODES**

## TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

## AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SECTION V

## SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

## DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

## DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

## AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

## START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

## RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the RST input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

| CRT 9007 outputs | Reset state |
|---|---|
| VA13-0 | High impedance |
| VD7-0 | High impedance |
| HS | High |
| VS | High |
| CBLANK | High |
| CURS | Low |
| VLT | Low |
| DRB | High |
| INT | Low |
| Pin 28 | Low |
| Pin 29 | Low |
| Pin 30 | Low |
| Pin 31 | Low |
| Pin 32 | Low |

## SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

## VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

## HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

## INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

## STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

## VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

## HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

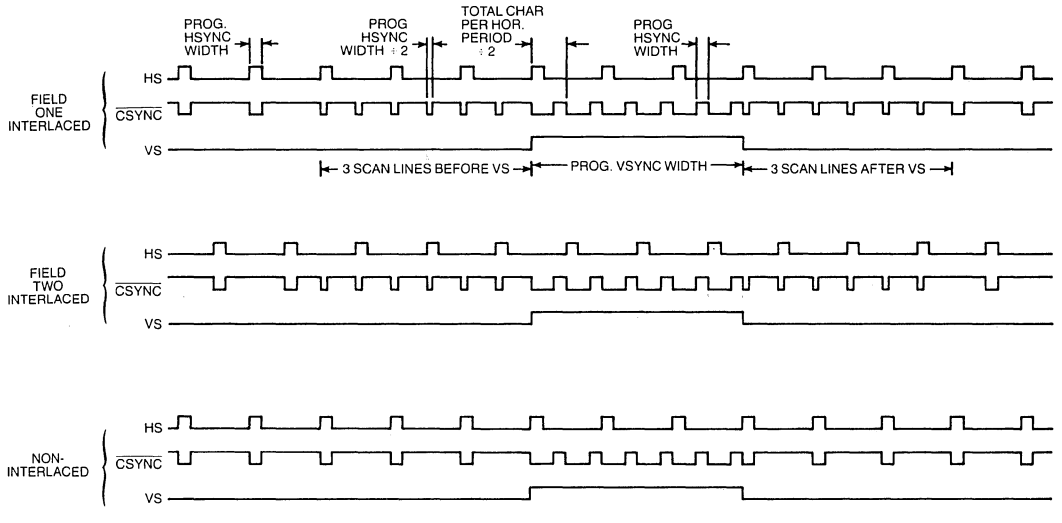



**FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES**

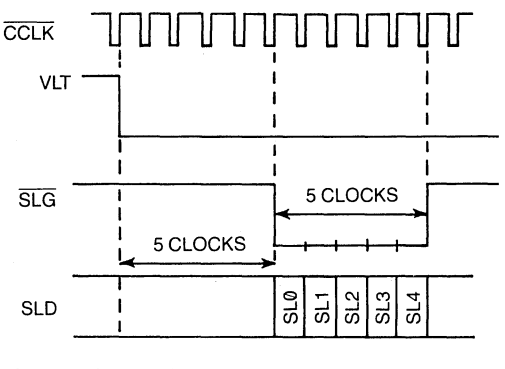



**FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS**

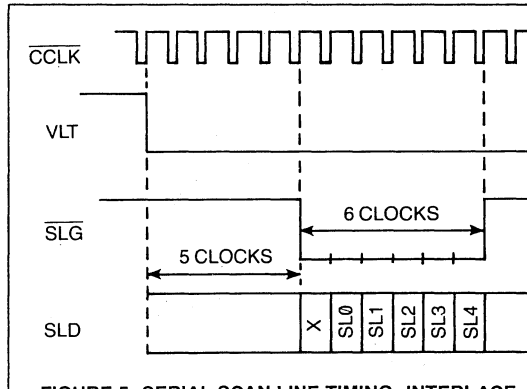



**FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS**

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0° to + 70°C
Storage Temperature Range ..... − 55°C to + 150°C
Lead Temperature (soldering, 10 sec.) ..... + 325°C
Positive Voltage on any Pin, with respect to ground ..... + 8V
Negative Voltage on any Pin, with respect to ground ..... − 0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**DC ELECTRICAL CHARACTERISTICS** $T_A$ = 0°C to + 70°C, $V_{CC}$ = 5.0V ± 5%

| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| | Input voltage | | | | | |
| $V_{IL}$ | Low | | | 0.8 | V | |
| $V_{IH1}$ | High | 2.0 | | | V | all inputs except $\overline{CCLK}$ |
| $V_{IH2}$ | High | 4.3 | | | V | $\overline{CCLK}$ input; see note 4 |
| | Output voltage | | | | | |
| $V_{OL}$ | Low | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| $V_{OH}$ | High | 2.4 | | | V | $I_{OH}$ = 100 μA |
| | Input leakage current | | | | | |
| $I_{L1}$ | | | | 10 | μA | $0 \leq V_{IN} \leq 3.5V$; excluding $\overline{CCLK}$ |
| $I_{L2}$ | | | | 50 | μA | $V_{IN}$ = 5V; for $\overline{CCLK}$ |
| | | | | −300 | μA | $V_{IN}$ = 0V; for $\overline{CCLK}$ |
| | Input capacitance | | | | | |
| $C_{IN1}$ | | | 10 | | pF | all inputs except $\overline{CCLK}$ |
| $C_{IN2}$ | | | 25 | | pF | $\overline{CCLK}$ input |
| | Power supply current | | | | | |
| $I_{CC}$ | | | 100 | 170 | mA | |

**AC ELECTRICAL CHARACTERISTICS**[3]; $T_A$ = 0°C to + 70°C, $V_{CC}$ = 5.0V ± 5%

| | PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|---|
| | Clock | | | | | |
| $t_{CY}$ | Clock period | 290 | | 1200 | ns | CRT9007A } double row buffer |
| | | 330 | | 1200 | ns | CRT9007B } or attribute assemble |
| | | 400 | | 1200 | ns | CRT9007C } |
| | | 270 | | 1200 | ns | CRT9007A } all other operation |
| | | 300 | | 1200 | ns | CRT9007B } modes |
| | | 400 | | 1200 | ns | CRT9007C } |
| $t_{CKL}$ | Clock low | 90 | | | ns | |
| $t_{CKH}$ | Clock high | 150 | | | ns | |
| $t_{CKR}$ | Clock rise time | | | 15 | ns | measured from 0.8V to 3.5V level |
| $t_{CKF}$ | Clock fall time | | | 10 | ns | measured from 90% to 10% points |
| | Output Delay[1]: | | | | | |
| $t_{D1}$ | | | | 150 | ns | CRT9007A/B |
| | | | | 240 | ns | CRT9007C |
| $t_{D2}$ | | | | 150 | ns | CRT9007A/B |
| | | | | 240 | ns | CRT9007C |
| $t_{D3}$ | | | | 150 | ns | CRT9007A/B |
| | | | | 200 | ns | CRT9007C |
| $t_{D4}$ | | | | 150 | ns | CRT9007A/B |
| | | | | 200 | ns | CRT9007C |
| $t_{VA}$ | | 25 | | 100 | ns | CRT9007A } measured to the 2.3V |
| | | 25 | | 115 | ns | CRT9007B } or 0.5V level on |
| | | 25 | | 125 | ns | CRT9007C } VA13-VA0 |
| $t_{DSL}$ | | | | 500 | ns | |
| $t_{D5}$ | | | | 185 | ns | CRT9007A/B |
| | | | | 200 | ns | CRT9007C |
| $t_{D6}$ | | | | 185 | ns | CRT9007A/B |
| | | | | 200 | ns | CRT9007C |
| $t_{DSY}$ | | | | 185 | ns | CRT9007A/B |
| | | | | 240 | ns | CRT9007C |
| $t_{VDS}$ | | 50 | | | ns | CRT9007A } valid for loading auxiliary |
| | | 55 | | | ns | CRT9007B } address register 2 or |
| | | 60 | | | ns | CRT9007C } attribute latch |
| $t_{VDH}$ | | 10 | | | ns | |
| $t_{VDO}$ | | | | 185 | ns | $C_L$ = 50 pF |
| $t_{SLG}$ | | | | 185 | ns | CRT9007A/B |
| | | | | 240 | ns | CRT9007C |
| $t_{SLD}$ | | | | 185 | ns | CRT9007A/B |
| | | | | 240 | ns | CRT9007C |
| $t_{D7}$ | | | | 240 | ns | cursor skew of zero |
| | | | | 185 | ns | CRT9007A/B } cursor skew of one |
| | | | | 240 | ns | CRT9007C } through five |
| $t_{DB}$ | | | | 300 | ns | CRT9007A/B |
| | | | | 310 | ns | CRT9007C |
| | Processor Read/Write[2]: | | | | | |
| $t_{AS}$ | | 100 | | | ns | CRT9007A |
| | | 110 | | | ns | CRT9007B/C |
| $t_{AH}$ | | 0 | | | ns | |
| $t_{PW}$ | | 165 | | | ns | |
| $t_{CSH}$ | | 650 | | | ns | |
| $t_{PDS}$ | | 100 | | | ns | |
| $t_{PDH}$ | | 0 | | | ns | |
| $t_{PDA}$ | | | | 140 | ns | CRT9007A/B |
| | | | | 189 | ns | CRT9007C |
| $t_{PDO}$ | | 10 | | 85 | ns | |
| $t_{IRR}$ | | | | 400 | ns | CRT9007A/B |
| | | | | 410 | ns | CRT9007C |
| | Miscellaneous Timing: | | | | | |
| $t_{ATS}$ | | 25 | | 115 | ns | measured from the 0.4V level of ACK or TSC falling edge |
| $t_{RW}$ | | 4tcy | | | ns | measured from the 0.4V level falling edge to 0.4V level rising edge |
| $t_{AKW}$ | | 50 | | | ns | see figure 24 |
| $t_{AKS}$ | | 50 | | | ns | see figure 24 |

NOTE: 1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the output unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of $\overline{CCLK}$.

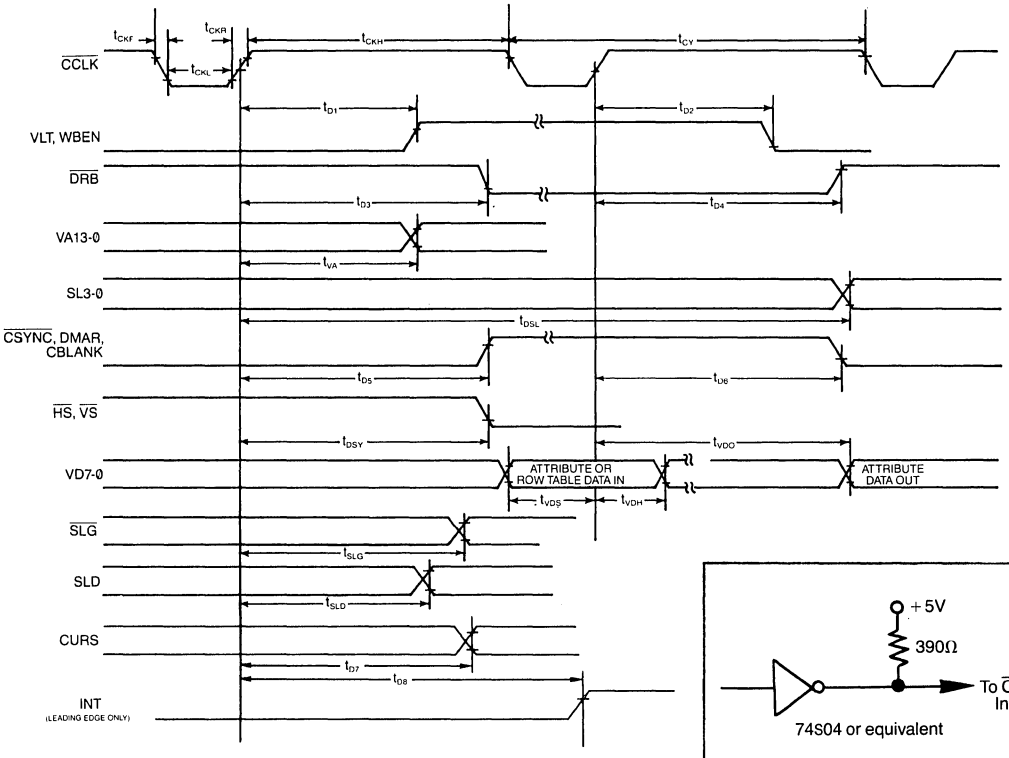



**FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS**




**FIGURE 25: RECOMMENDED CCLK DRIVER CIRCUIT**

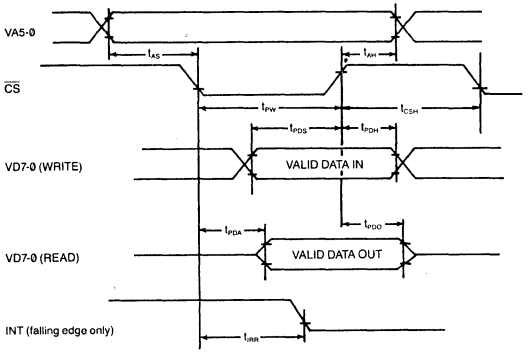
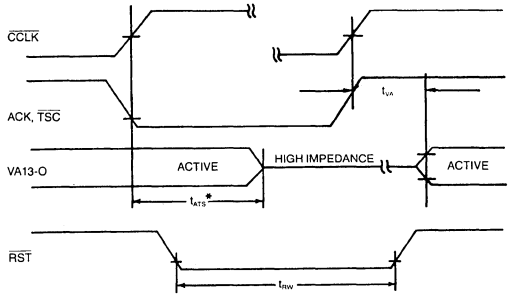



**FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS**




* $t_{ATS}$ is controlled directly from ACK or TSC or from the particular CCLK that ends a DMA burst cycle.

**FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS**

| Register Type | ADDRESS DECODE VA5 | VA4 | VA3 | VA2 | VA1 | VA0 | BIT DEFINITION D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER NUMBER (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRITE | 0 | 0 | 0 | 0 | 0 | 0 | MSB | CHARACTERS PER HORIZONTAL PERIOD | | | | | | LSB | R0 |
| WRITE | 0 | 0 | 0 | 0 | 0 | 1 | MSB | CHARACTERS PER DATA ROW | | | | | | LSB | R1 |
| WRITE | 0 | 0 | 0 | 0 | 1 | 0 | MSB | HORIZONTAL DELAY | | | | | | LSB | R2 |
| WRITE | 0 | 0 | 0 | 0 | 1 | 1 | MSB | HORIZONTAL SYNC WIDTH | | | | | | LSB | R3 |
| WRITE | 0 | 0 | 0 | 1 | 0 | 0 | MSB | VERTICAL SYNC WIDTH | | | | | | LSB | R4 |
| WRITE | 0 | 0 | 0 | 1 | 0 | 1 | MSB | VERTICAL DELAY | | | | | | LSB | R5 |
| WRITE | 0 | 0 | 0 | 1 | 1 | 0 | PIN CONFIG-URATION | CURSOR SKEW MSB | | | LSB | MSB | BLANK SKEW | LSB | R6 |
| WRITE | 0 | 0 | 0 | 1 | 1 | 1 | MSB | VISIBLE DATA ROWS PER FRAME | | | | | | LSB | R7 |
| WRITE | 0 | 0 | 1 | 0 | 0 | 0 | SCAN LINES FRAME (B10)) | (B8) | MSB | SCAN LINES PER DATA ROW | | | | LSB | R8 |
| WRITE | 0 | 0 | 1 | 0 | 0 | 1 | (B7) | SCAN LINES PER FRAME | | | | | | LSB (B0) | R9 |

**Table 3a: CRT 9007 Screen Format Registers**

| Register Type | ADDRESS DECODE VA5 | VA4 | VA3 | VA2 | VA1 | VA0 | BIT DEFINITION D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER NUMBER (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRITE | 0 | 0 | 1 | 0 | 1 | 0 | DMA DIS-ABLE | DMA BURST DELAY MSBA | | LSB | DMA BURST COUNT MSB | | | LSB | RA |
| WRITE | 0 | 0 | 1 | 0 | 1 | 1 | X | PB/$\overline{SS}$ | INTERLACE MODES | | OPERATION MODES | | | 2XC/1XC | RB |
| WRITE | 0 | 0 | 1 | 1 | 0 | 0 | MSB | TABLE START REGISTER (LS BYTE) | | | | | | LSB | RC |
| WRITE | 0 | 0 | 1 | 1 | 0 | 1 | ADDRESS MODE | TABLE STRT REGISTER (MS BYTE) MSB | | | | | | LSB | RD |
| WRITE | 0 | 0 | 1 | 1 | 1 | 0 | MSB | AUXILIARY ADDRESS REGISTER 1 (LS BYTE) | | | | | | LSB | RE |
| WRITE | 0 | 0 | 1 | 1 | 1 | 1 | ROW ATTRIBUTES | AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB | | | | | | LSB | RF |
| WRITE | 0 | 1 | 0 | 0 | 0 | 0 | MSB | SEQUENTIAL BREAK REGISTER 1 | | | | | | LSB | R10 |
| WRITE | 0 | 1 | 0 | 0 | 0 | 1 | MSB | DATA ROW START REGISTER | | | | | | LSB | R11 |
| WRITE | 0 | 1 | 0 | 0 | 1 | 0 | MSB | DATA ROW END/SEQUENTIAL BREAK REGISTER 2 | | | | | | LSB | R12 |
| WRITE | 0 | 1 | 0 | 0 | 1 | 1 | MSB | AUXILIARY ADDRESS REGISTER 2 (LS BYTE) | | | | | | LSB | R13 |
| WRITE | 0 | 1 | 0 | 1 | 0 | 0 | ROW ATTRIBUTES | AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB | | | | | | LSB | R14 |

**Table 3b: Control and Memory Address Registers**

| Register Type | ADDRESS DECODE VA5 | VA4 | VA3 | VA2 | VA1 | VA0 | BIT DEFINITION D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REGISTER NUMBER (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| READ OR WRITE | 0 | 1 | 0 | 1 | 0 | 1 | START COMMAND | | | | | | | | R15 |
| READ OR WRITE | 0 | 1 | 0 | 1 | 1 | 0 | RESET COMMAND | | | | | | | | R16 |
| WRITE | 0 | 1 | 0 | 1 | 1 | 1 | OFFSET OVER-FLOW | OFFSET VALUE MSB | | | | | LSB | 0 | R17 |
| WRITE | 0 | 1 | 1 | 0 | 0 | 0 | MSB | VERTICAL CURSOR REGISTER (ROW COORD.) | | | | | | LSB | R18 or R38 |
| READ | 1 | 1 | 1 | 0 | 0 | 0 | | | | | | | | | |
| WRITE | 0 | 1 | 1 | 0 | 0 | 1 | MSB | HORIZONTAL CURSOR REGISTER (COL. COORD.) | | | | | | LSB | R19 or R39 |
| READ | 1 | 1 | 1 | 0 | 0 | 1 | | | | | | | | | |
| WRITE | 0 | 1 | 1 | 0 | 1 | 0 | X | VER-TICAL RE-TRACE | LIGHT PEN | INTERRUPT ENABLE REGISTER X | X | X | X | FRAME TIMER | R1A |
| READ | 1 | 1 | 1 | 0 | 1 | 0 | INT PEND-ING | VER-TICAL RE-TRACE | LIGHT PEN | STATUS REGISTER | | | ODD/ EVEN | X FRAME TIMER | R3A |
| READ | 1 | 1 | 1 | 0 | 1 | 1 | MSB | VERTICAL LIGHT PEN REGISTER (ROW COORD.) | | | | | | LSB | R3B |
| READ | 1 | 1 | 1 | 1 | 0 | 0 | MSB | HORIZONTAL LIGHT PEN REGISTER (COL. COORD.) | | | | | | LSB | R3C |

**Table 3c: Cursor, Light Pen, Offset, and Status Registers**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

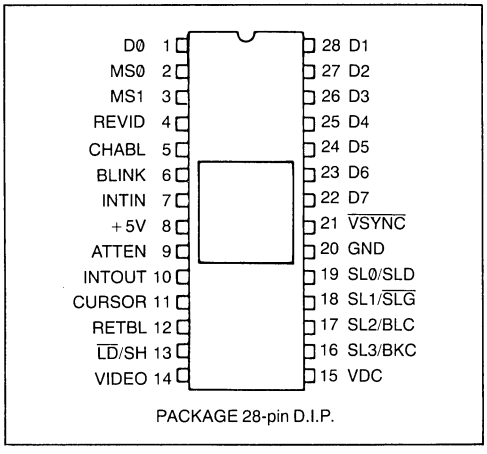
# CRT 9021A
# CRT 9021B
## µPC FAMILY

# CRT Video Attributes Controller VAC

### FEATURES

- ☐ On chip video shift register
  Maximum shift register frequency
  CRT 9021A 30 MHz
  CRT 9021B 28.5 MHz
- ☐ On chip attributes logic
  Reverse video
  Character blank
  Character blink
  Underline
  Full/half intensity
- ☐ Four modes of operation
  Wide graphics
  Thin graphics
  Character mode without underline
  Character mode with underline
- ☐ On Chip logic for double height/double width characters
- ☐ Accepts scan line information in parallel or serial format
- ☐ Four cursor modes dynamically selectable via 2 input pins
  Underline
  Blinking underline
  Reverse video
  Blinking reverse video
- ☐ Programmable character blink rate

### PIN CONFIGURATION




PACKAGE 28-pin D.I.P.

- ☐ Programmable cursor blink rate
- ☐ On chip data and attribute latches
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS n-Channel silicon gate COPLAMOS® process
- ☐ Compatible with CRT 5037 VTAC®; CRT 9007 VPAC™

SECTION V

### GENERAL DESCRIPTION

The SMC CRT 9021 Video Attributes Controller (VAC) is an n-channel COPLAMOS MOS/LSI device containing Graphics logic, attributes logic, data and attributes latches, cursor control, and a high speed video shift register. The CRT 9021, a character generator ROM and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9021 serial video output may be connected directly to a CRT monitor's video input. The maximum video shift register frequency of 28.5 MHz or 30 MHz allows for CRT displays of up to 132 characters per data row.

The CRT 9021 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition, when used in conjunction with the CRT 9007 VPAC,™ the CRT 9021 will provide double height or double width characters.

Four programmable cursor modes are provided on the CRT 9021. They are: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the CRT 9021 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

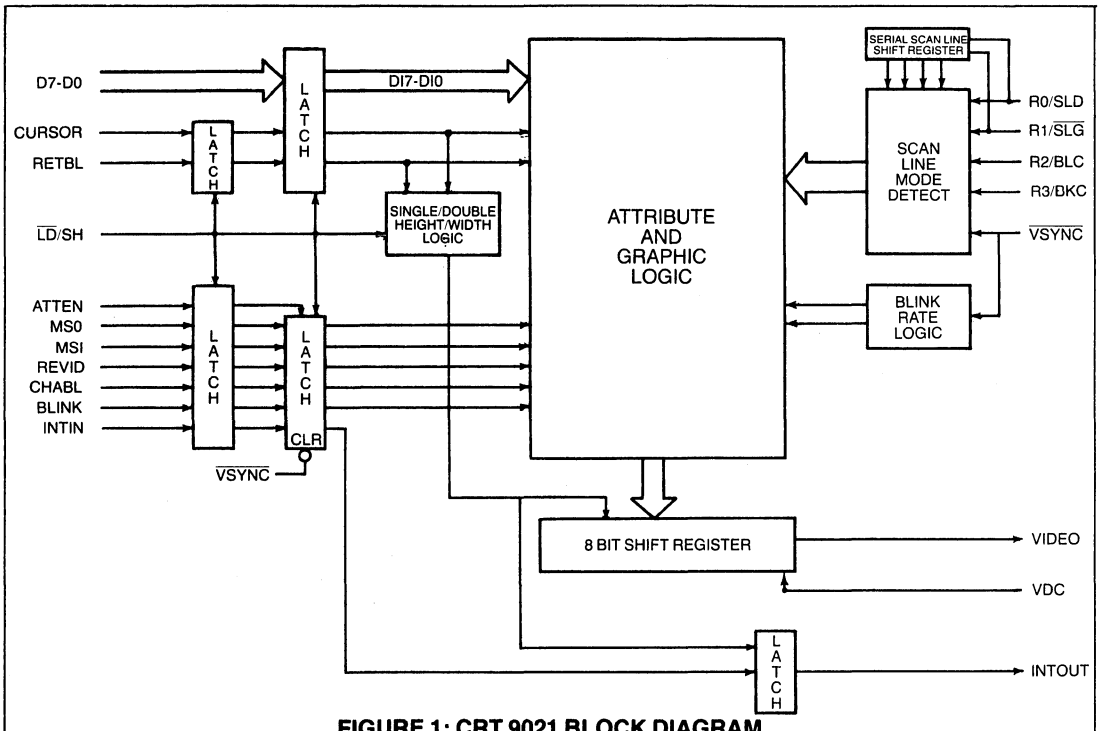



**FIGURE 1: CRT 9021 BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1, 28, 27, 26, 25, 24, 23, 22 | Data | D7-D0 | In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the LD/SH input goes low.<br>In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Figures 2 and 3 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0 |
| 2<br>3 | Mode Select Ø<br>Mode Select 1 | MS0<br>MS1 | These 2 inputs define the four modes of operation of the CRT 9021 as follows:<br>MS1, MS0 = 00; Wide graphics mode<br>= 10; Thin graphics mode<br>= 01; Character mode without underline<br>= 11; Character mode with underline<br>See section entitled Display Modes for details. |
| 4 | Reverse Video | REVID | When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register. |
| 5 | Character blank | CHABL | When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block. |
| 6 | Blink | BLINK | When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75/25 (on/off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink. |
| 7 | Intensity In | INTIN | The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity". |

## DESCRIPTION OF PIN FUNCTIONS CONT'D

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 8 | Supply Voltage | +5V | +5 volt power supply |
| 9 | Attribute Enable | ATTEN | When this input is high, the internal attribute latch is updated at the positive going edge of the LD/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes).. |
| 10 | Intensity Out | INTOUT | This output is used in conjunction with the INTIN input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7). |
| 11 | Cursor | CURSOR | When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9021 enters the double width mode. See section entitled cursor formats for details. |
| 12 | Retrace Blank | RETBL | When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next LD/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time. |
| 13 | Load/Shift | LD/SH | The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of LD/SH. |
| 14 | Video | VIDEO | The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of the LD/SH input will determine the number of backfill dots. See figure 5. |
| 15 | Video Dot Clock | VDC | This input clock controls the rate at which video is shifted out on the VIDEO output. |
| 16 | Scan line 3/Block Cursor | SL3/BKC | This input has two separate functions depending on the way scan line information is presented to the CRT 9021.<br>*Parallel scan line mode*—This input is the most significant bit of the binary scan line row address.<br>*Serial scan line mode*—This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed. |
| 17 | Scan line 2/Blink Cursor | SL2/BLC | This input has two separate functions depending on the way scan line information is presented to the CRT 9021.<br>*Parallel scan line mode*—This input is the second most significant bit of the binary scan line row address.<br>*Serial scan line mode*—This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking. |
| 18 | Scan Line 1/Scan Line Gate | SL1/SLG | This input has two separate functions depending on the way scan line information is presented to the CRT 9021.<br>*Parallel scan line mode*—This input is the next to the least significant bit of the binary scan line row address.<br>*Serial scan line mode*—This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more LD/SH pulses, the CRT 9021 will assume the parallel input scan line row address mode. |
| 19 | Scan line 0/Scan Line data | SL0/SLD | This input has two separate functions depending on the way scan line information is presented to the CRT 9021. Refer to figure 6.<br>*Parallel scan line mode*—This input is the least significant bit of the binary scan line row address.<br>*Serial scan line mode*—This input will present the scan line information in serial form (least significant bit first) to the CRT 9021 and permits the proper scan line information to enter the serial scan line shift register during the LD/SH pulses framed by SLG (pin 18). |
| 20 | Ground | GND | Ground |
| 21 | Vertical Sync | VSYNC | This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The VSYNC input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes". |

## ATTRIBUTES FUNCTION

Retrace Blank —The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video —The REVID input causes inverted data to be loaded into the video shift register.

Character Blank —The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline —MS1, MS0 = 1, 1 forces the video to go to the inverse of the background level for the scan line(s) programmed for underline.

Blink —The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) —The INTiN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the CRT 9021. An external mixer can be used to combine VIDEO and INTOUT to create the desired video level. See figure 8.

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

## TABLE 1: CRT 9021 ATTRIBUTE COMBINATIONS

| CURSOR FORMAT | CRT 9021 INPUTS | | | | | VIDEO SHIFT REGISTER LOADED WITH: | |
|---|---|---|---|---|---|---|---|
| | RETBL | CURSOR | REVID | CHABL | UNDLN | | |
| X | 1 | X | X | X | X | all zero's | |
| | 0 | 0 | 0 | 0 | 0 | data | |
| | 0 | 0 | 0 | 0 | 1 | One's for selected scan line(s); Data for all other scan lines. | |
| | 0 | 0 | 0 | 1 | X | All zero's | |
| | 0 | 0 | 1 | 0 | 0 | $\overline{data}$ | |
| | 0 | 0 | 1 | 0 | 1 | Zero's for selected scan line(s); $\overline{data}$ for all other scan lines. | |
| | 0 | 0 | 1 | 1 | X | One's for all scan lines. | |
| UNDERLINE[2] | 0 | 1 | 0 | 0 | X[1] | One's for selected scan line(s) for cursor; data for all other scan lines. | |
| | 0 | 1 | 0 | 1 | X[1] | One's for selected scan line(s) for cursor; zero's for all other scan lines. | |
| | 0 | 1 | 1 | 0 | X[1] | Zero's for selected scan line(s) for cursor; Data for all other scan lines. | |
| | 0 | 1 | 1 | 1 | X[1] | Zero's for selected scan line(s) for cursor; one's for all other scan lines. | |
| BLINKING[3] UNDERLINE[2] | 0 | 1 | 0 | 0 | X[1] | One's for selected scan line(s) blinking; Data for all other scan lines. | |
| | 0 | 1 | 0 | 1 | X[1] | One's for selected scan line(s) blinking; zero's for all other scan lines. | |
| | 0 | 1 | 1 | 0 | X[1] | Zero's for selected scan line(s) blinking; Data for all other scan lines. | |
| | 0 | 1 | 1 | 1 | X[1] | Zero's for selected scan line(s) blinking; one's for all other scan lines. | |
| REVID BLOCK | 0 | 1 | 0 | 0 | 0 | $\overline{Data}$ for all scan lines. | |
| | 0 | 1 | 0 | 0 | 1 | Zero's for selected scan line(s) for underline; data for all other scan lines. | |
| | 0 | 1 | 0 | 1 | X | One's for all scan lines. | |
| | 0 | 1 | 1 | 0 | 0 | Data for all scan lines | |
| | 0 | 1 | 1 | 0 | 1 | One's for selected scan line(s) for underline; data for all other scan lines. | |
| | 0 | 1 | 1 | 1 | X | Zero's for all scan lines. | |
| BLINKING[3] REVID BLOCK | 0 | 1 | 0 | 0 | 0 | On Data for all scan lines. | Off Data for all scan lines. |
| | 0 | 1 | 0 | 0 | 1 | Zero's for selected scan line(s) for underline; Data for all other scan lines. | One's for selected scan line(s) for underline; Data for all other scan lines. |
| | 0 | 1 | 0 | 1 | X | One's for all scan lines. | Zero's for all scan lines. |
| | 0 | 1 | 1 | 0 | 0 | Data for all scan lines. | $\overline{Data}$ for all scan lines. |
| | 0 | 1 | 1 | 0 | 1 | One's for selected scan line(s); Data for all other scan lines. | Zero's for selected scan line(s); Data for all other scan lines. |
| | 0 | 1 | 1 | 1 | X | Zero's for all scan lines. | One's for all scan lines. |

1 - if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence; otherwise both are displayed.
2 - at programmed scan line(s) for underline
3 - at cursor blink rate
Note—cursor blink rate overrides character blink rate.

## DISPLAY MODES

Inputs MS1 and MSØ select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 8a and 8b illustrate a typical CRT 9021 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 —Wide Graphics Mode. In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 2. Note that individual bits in D7-D0 will illuminate particular portions of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

MS1, MS0 = 10 —Thin Graphics Mode. In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 3. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.

MS1, MS0 = 01 —Character Mode Without Underline. In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 8a and 8b.

MS1, MS0 = 11 —Character Mode With Underline. Same operation as MS1, MSØ = 01 with the underline attribute appearing on the scan line(s) mask programmed.

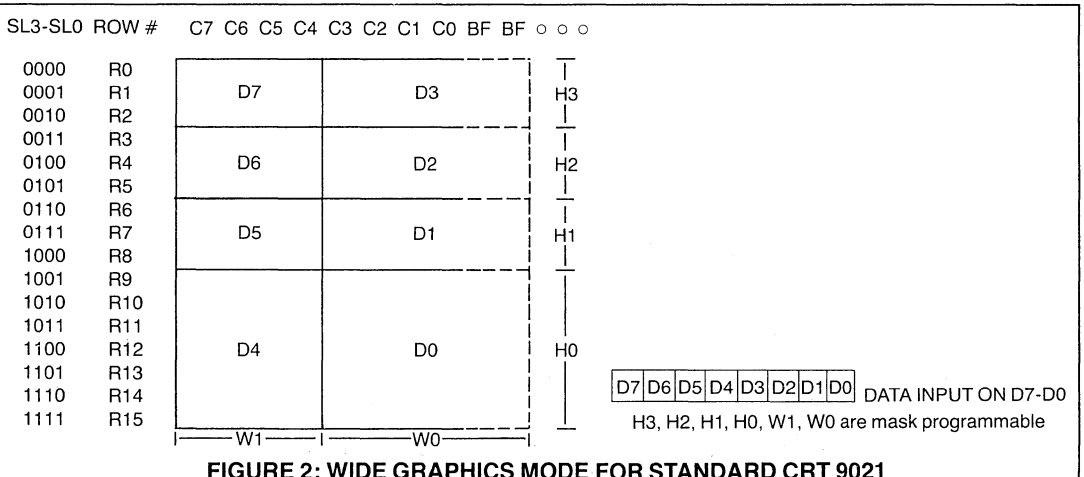



**FIGURE 2: WIDE GRAPHICS MODE FOR STANDARD CRT 9021**

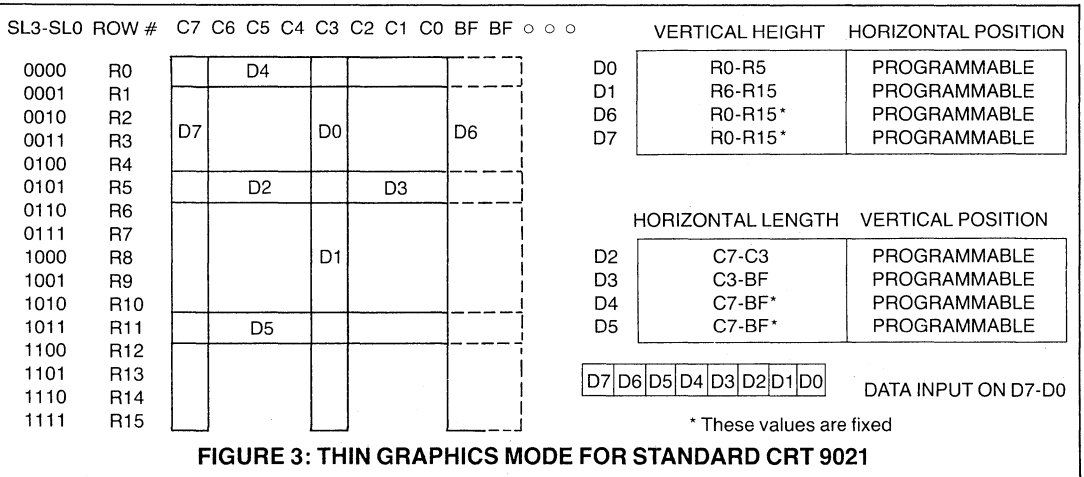



**FIGURE 3: THIN GRAPHICS MODE FOR STANDARD CRT 9021**

## BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyond 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

## CURSOR FORMATS

Four cursor formats are possible with the CRT 9021. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 5. The four cursor modes are as follows:

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse video block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

| Scan Line Input Mode | Pin 17 | Pin 16 | Cursor Function |
|---|---|---|---|
| Serial | 1 | 0 | Underline |
| | 1 | 1 | Reverse Video Block |
| | 0 | 0 | Blinking Underline |
| | 0 | 1 | Blinking Reverse Video Block |
| Parallel | X | X | Mask programmable Only |

**TABLE 5: CURSOR FORMATS**

## DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the CRT 9021, no distinction between double width and double height display is necessary. Figure 4 illustrated timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the CURSOR signal as required by the CRT 9021 with no additional hardware.

## SCAN LINE INPUT MODES

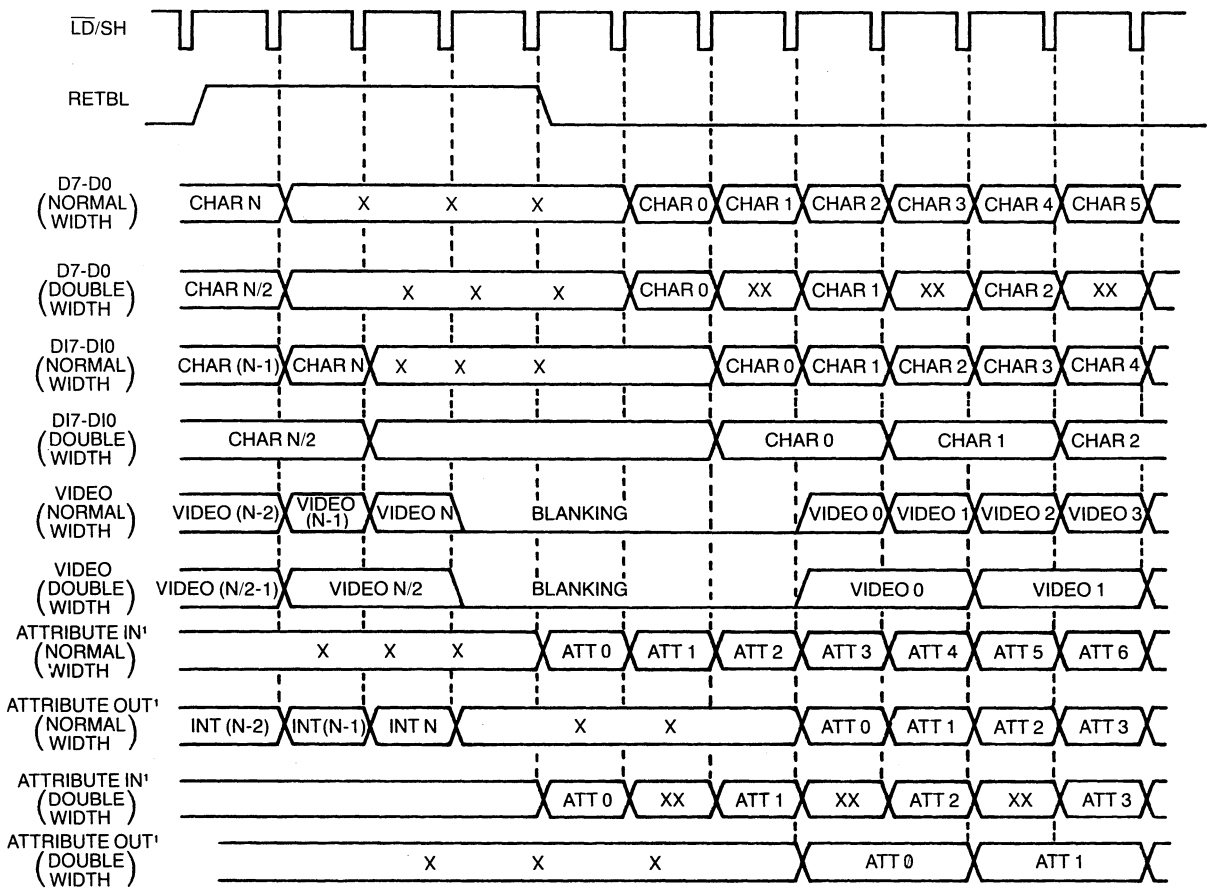
Scan line information can be introduced into the CRT 9021 in parallel format or serial format. Table 6 illustrates the pin definition as a function of the scan line input mode. The CRT 9021 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two conditions occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$/SH periods. Refer to figure 7 for timing details.

| Scan Line Input Mode | CRT 9021 Pin Number | | | |
|---|---|---|---|---|
| | 19 | 18 | 17 | 16 |
| Serial | SLD | $\overline{SLG}$ | BLC | BKC |
| Parallel | SL0 | SL1 | SL2 | SL3 |

**TABLE 6: PIN DEFINITION FOR PARALLEL AND SERIAL SCAN LINE MODES**

## PROGRAM OPTIONS

The CRT 9021 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 4 illustrates the range of the miscellaneous mask programmed options. In addition, Tables 2, 3 and 4 show the mask programmed options for the standard CRT 9021.




1 - Attributes include MS0 , MSI, BLINK, CHABL, INTENSITY, REVID

**FIGURE 4: CRT 9021 FUNCTIONAL I/O TIMING**

**MAXIMUM GUARANTEED RATINGS***

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −55°C to +150°C |
| Lead Temperature (soldering, 10 sec.) | +325°C |
| Positive Voltage on any Pin, with respect to ground | .15V |
| Negative Voltage on any Pin, with respect to ground | −0.3V |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%, unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{IL}$ | | | 0.8 | V | All inputs except VDC, $\overline{LD}$/SH |
| Low Level $V_{IL}$ | | | 0.65 | V | For VDC, $\overline{LD}$/SH inputs |
| High Level $V_{IH1}$ | 2.0 | | | V | All inputs except VDC, $\overline{LD}$/SH |
| High Level $V_{IH2}$ | 4.3 | | | V | For VDC, $\overline{LD}$/SH input |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 0.4 mA |
| High Level $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 100μA |
| INPUT LEAKAGE CURRENT | | | | | |
| Leakage $I_{L1}$ | | | 10 | μA | $0 \leq V_{IN} < V_{CC}$; excluding VDC, $\overline{LD}$/SH |
| Leakage $I_{L2}$ | | | 50 | μA | $0 \leq V_{IN} \leq V_{CC}$; for VDC $\overline{LD}$/SH |
| INPUT CAPACITANCE | | | | | |
| $C_{IN1}$ | | 10 | | pf | Excluding VDC, $\overline{LD}$/SH |
| $C_{IN2}$ | | 20 | | pf | For $\overline{LD}$/SH |
| $C_{IN3}$ | | 25 | | pf | For VDC |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 50 | | mA | |

**AC CHARACTERISTICS**

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| VDC[1] | | | | | |
| $1/t_{CY1}$ VDC frequency | 10.0 | | 30.0 | MHZ | CRT 9021A; see note 1 |
| | 10.0 | | 28.5 | MHZ | CRT 9021B |
| $1_{CKL}$ VDC low | 10 | | | | |
| $t_{CKH}$ VDC high | 10 | | | ns | |
| $t_{CKR}$ VDC rise time | | | 10 | ns | Measured from 10% to 90% points |
| $t_{CKF}$ VDC fall time | | | 10 | ns | Measured from 90% to 10% points |
| $\overline{LD}$/SH | | | | | |
| $t_{CY2}$ | 290 | | | ns | CRT 9021A; see note 1 |
| | 315 | | | ns | CRT 9021B |
| $t_{S1}$ | 7 | | | ns | |
| $t_{H1}$ | 0 | | | ns | |
| INPUT SETUP AND HOLD | | | | | |
| $t_{S2}$ | 35 | | | ns | |
| $t_{H2}$ | 0 | | | ns | |
| MISCELLANEOUS TIMING | | | | | |
| $t_{PD}$ | | | 35 | ns | $C_L$ = 15 pf |
| $t_{DW}$ | $t_{CY2}$ | | | | |

1-These parameters are Preliminary.

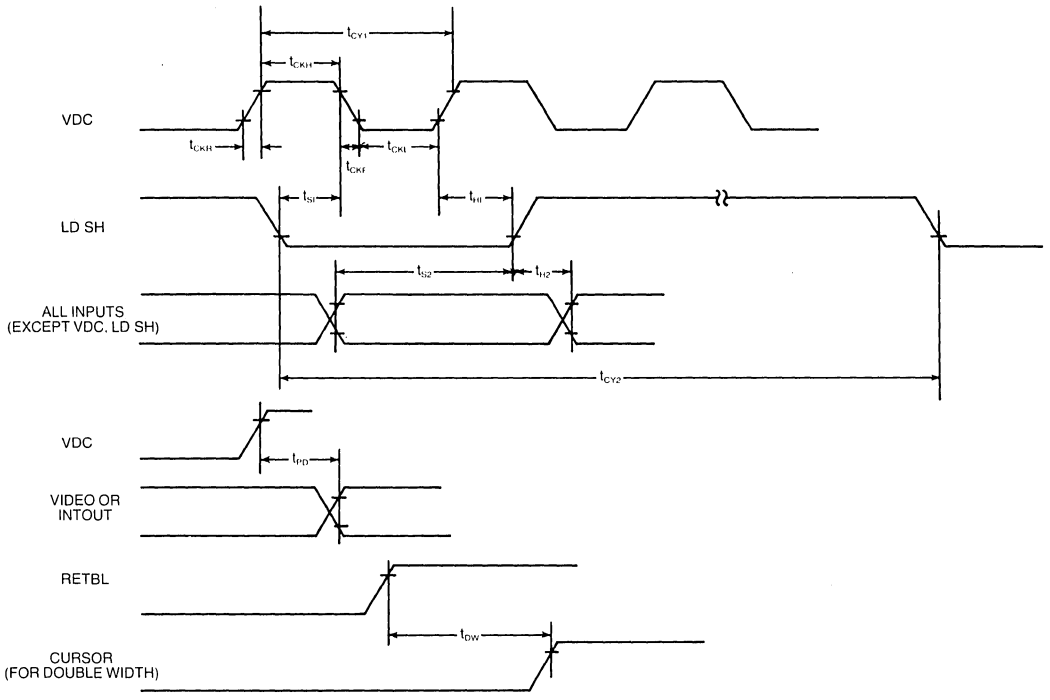



**FIGURE 5: CRT 9021 INPUT/OUTPUT TIMING**

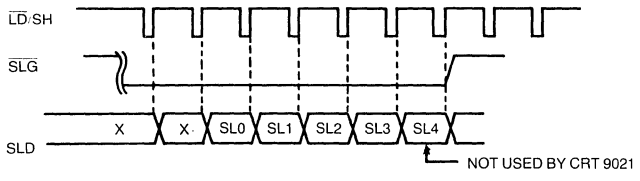



**FIGURE 6: SERIAL SCAN LINE MODE TIMING**

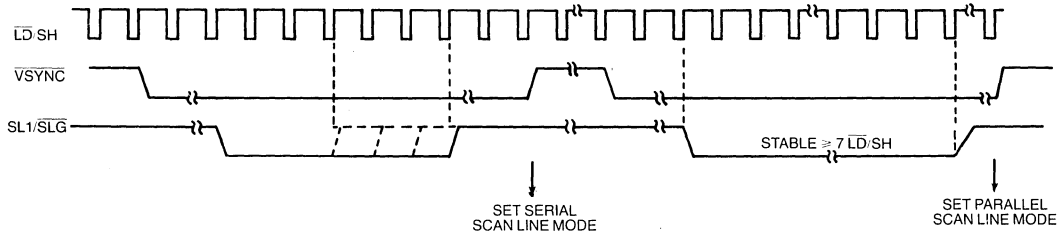



**FIGURE 7: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING**

SECTION V

## TABLE 2
## WIDE GRAPHICS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | STANDARD CRT 9021 |
|---|---|---|
| Height of graphic block* | | |
| D7 and D3 | any scan line(s) | R0, R1, R2 |
| D6 and D2 | any scan line(s) | R3, R4, R5 |
| D5 and D1 | any scan line(s) | R6, R7, R8 |
| D4 and D0 | any scan line(s) | R9, R10, R11, R12, R13, R14, R15 |
| Width of D7, D6, D5, D4** | any number of dots 0 to 8 | C7, C6, C5, C4 |
| Width of D3, D2, D1, D0** | any number of dots 0 to 8 | C3, C2, C1, C0, BF |

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

## TABLE 3
## THIN GRAPHICS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | STANDARD CRT 9021 |
|---|---|---|
| Backfill | C1 or C0 | C0 |
| Horizontal position for | | |
| D2 and D3 | any scan line(s) R0-R15 | R5 |
| D4 | any scan line(s) R0-R15 | R0 |
| D5 | any scan line(s) R0-R15 | R11 |
| Horizontal length for | | |
| D2[2] | any continuous dots C7-C0, BF | C7-C3 |
| D3[2] | all dots not covered by D2 | C3-BF |
| Blanked dots for serrated horizontal lines | | |
| D2 | any dot(s) C7-C0, BF | none |
| D3 | any dot(s) C7-C0, BF | none |
| D4 and D5 | any dot(s) C7-C0, BF | none |
| Vertical position for | | |
| D0 and D1 | any dot(s) C7-C0, BF | C3 |
| D6[1] | any dot(s) C6-C0, BF | BF |
| D7[1] | any dot(s) C7-C0 | C7 |
| Vertical length for | | |
| D0 | any scan line(s) | R0 to R5 |
| D1 | all scan lines not used by D0 | R6 to R15 |
| D6 | no choice; always R0-R15 | R0 to R15 |
| D7 | no choice; always R0-R15 | R0 to R15 |

1-D7 must always come before D6 with no overlap; otherwise D6 is lost.
2-D2 and D3 must always overlap by one and only one dot.

## TABLE 4
## MISCELLANEOUS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | STANDARD CRT 9021 |
|---|---|---|
| Backfill in character mode | C7 or C0 | C7 |
| Character blink rate (division of $\overline{\text{VSYNC}}$ frequency) | 8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1] | 32 (1.875 Hz)[1] |
| Cursor blink rate[2] | Twice the character blink rate | 16 (3.75 Hz)[1] |
| character underline position | any scan line(s) R0-R15 | R11 |
| cursor underline[3] | any scan line(s) R0-R15 | not applicable |
| cursor format[4] | underline<br>Blinking underline<br>Reverse video block<br>Blinking reverse video block | Blinking reverse video block |

1 - Assumes $\overline{\text{VSYNC}}$ input frequency of 60 Hz.
2 - Valid only if the cursor is formatted to blink.
3 - Valid only if the cursor is formatted for underline.
4 - Valid for the parallel scan line mode only.

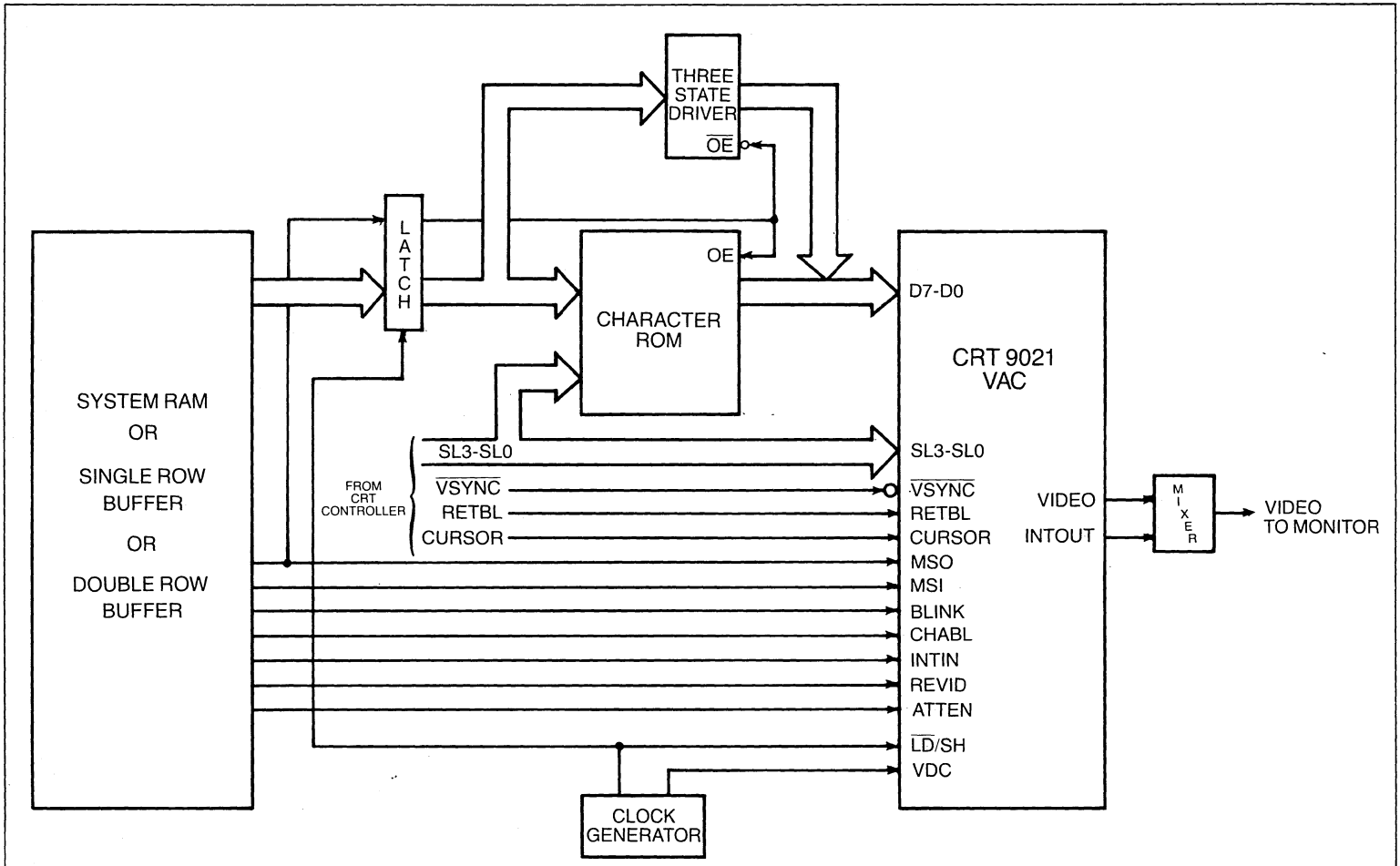



**FIGURE 8a: CRT 9021 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE**

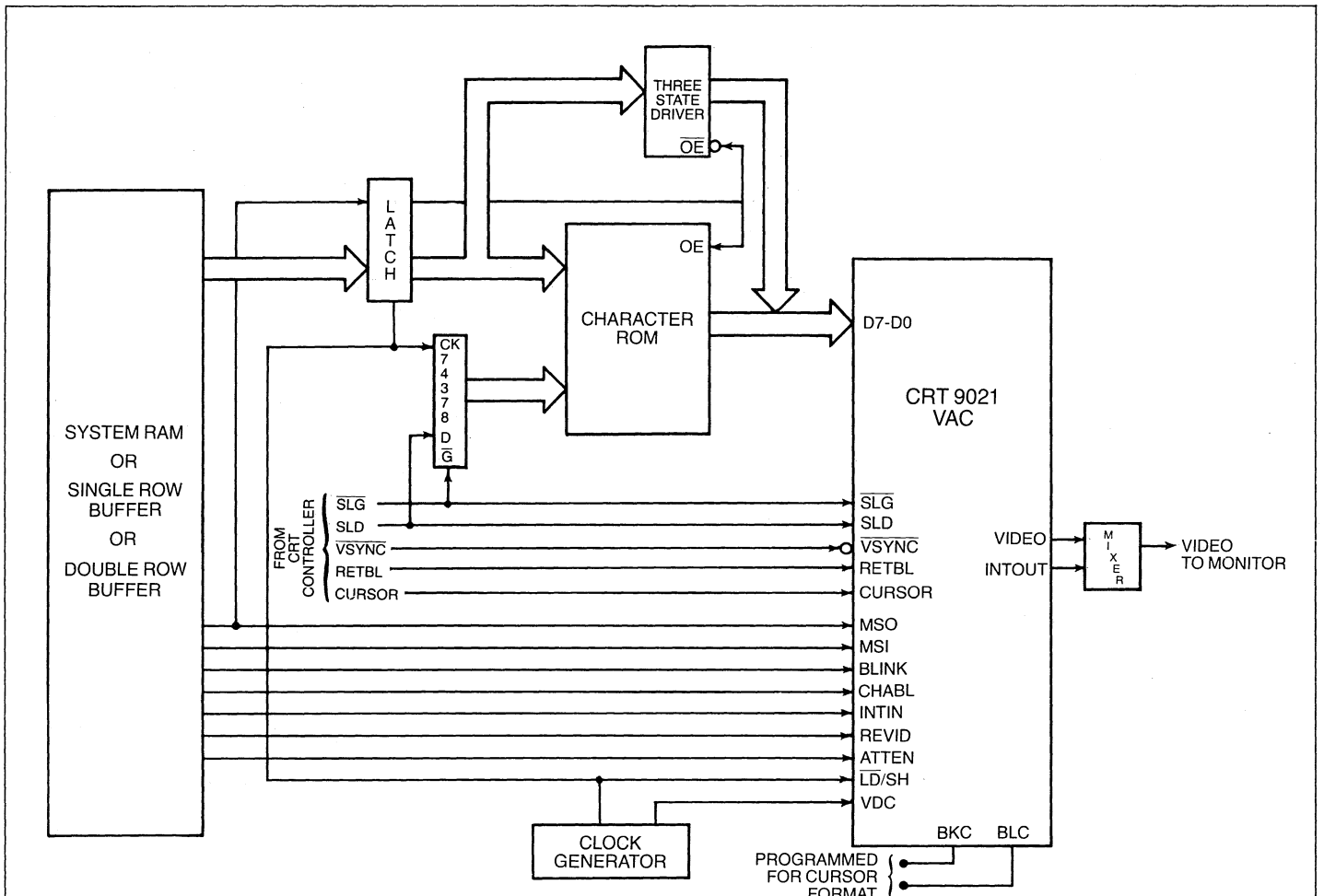



**FIGURE 8b: CRT 9021 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE**

STANDARD MICROSYSTEMS CORPORATION

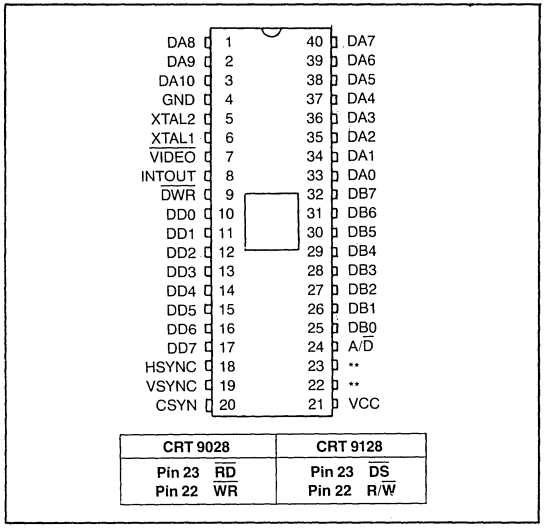
# CRT 9028
# CRT 9128
**PRELIMINARY**

# VTLC
# Video Terminal Logic Controller

## FEATURES

- ☐ Built-in High Frequency (4-14 MHz) Oscillator
- ☐ Built-in Video Shift Register
- ☐ Built-in Character Generator
- ☐ Bi-Directional Smooth Scroll Capability
- ☐ Visual Attributes Include Reverse Video, Intensity Control, Underline and Character Blank
- ☐ Separate HSYNC, VSYNC and VIDEO Outputs
- ☐ Composite Sync (RS170 Compatible) Output
- ☐ Absolute (RAM address) Cursor Addressing
- ☐ MASK Programmable Video Parameters:
  - Dots Per Character Block (6-8)
  - Raster Scans Per Data Row (8-12)
  - Characters Per Data Row (32, 48, 64, 80)
  - Data Rows Per Page (8,10,12,16,20,24 or 25)
  - Horizontal Blanking (8-64 Characters)
  - Horizontal Sync Front Porch (0-7 Characters)
  - Horizontal Sync Duration (1-64 Characters)
  - Horizontal Sync Polarity
  - Two Values of Vertical Blanking
  - Two Values of Vertical Sync Front Porch (0-63 Scan Lines)
  - Two Values of Vertical Sync Duration (1-16 Scan Lines)
  - Vertical Sync Polarity
  - Internal 128 Character 5x8 Dot Font
  - Character/Cursor Underline Position
  - Scan Row and Column for Thin Graphics Entity Segments
  - Scan Rows and Columns for Wide Graphics Entity Elements
- ☐ Software Enabled Non-Scrolling 25th Data Row Available with 25 Data Row/Page Display
- ☐ Non-Interlace Display Format
- ☐ Separate Display Memory Bus Eliminates Contention Problems
- ☐ Fill (Erase) Screen Capability
- ☐ Standard 8-bit Data Bus Microprocessor Interface
- ☐ Wide Graphics with Six Independently Addressable Segments Per Character Space
- ☐ Thin Graphics with Four Independently Addressable Segments Per Character Space
- ☐ Single +5V Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ TTL Compatible

## PIN CONFIGURATION




| CRT 9028 | CRT 9128 |
|---|---|
| Pin 23 RD | Pin 23 DS |
| Pin 22 WR | Pin 22 R/W |

## GENERAL DESCRIPTION

The CRT 9028 VTLC and CRT 9128 VTLC are mask programmable 40 pin COPLAMOS® n-channel MOS/LSI Video Display Controller Chips that combine video timing, video attributes, alphanumeric and graphics generation, smooth scroll and screen buffer interface functions.

The VTLC incorporates many of the features (previously requiring a number of external components) required in building a low cost yet versatile display interface. An internal mask programmable 128 character font provides for a full ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

Two pinout configurations enhance the versatility of the VTLC. The CRT 9028 controls data flow over the processor system data bus through separate read ($\overline{RD}$) and write ($\overline{WR}$) strobes for use with the 8085, 8051, Z80®, 8086, and similar microprocessors or microcomputers. The CRT 9128 regulates the data flow with a data strobe ($\overline{DS}$) and read/write (R/$\overline{W}$) enable signals for use with the 6500, Z8™, 68000 and similar microprocessors or microcomputers.

The VTLC provides two independent data buses; one bus that interfaces to the processor and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the VTLC eliminating contention problems and the need for a separate row buffer.

The VTLC has an internal crystal oscillator requiring only an external crystal to operate. Masked constants for critical video timing simplify programming, operation and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

*Z80 is a registered trademark of Zilog Corporation.
Z8 is a trademark of Zilog Corporation.

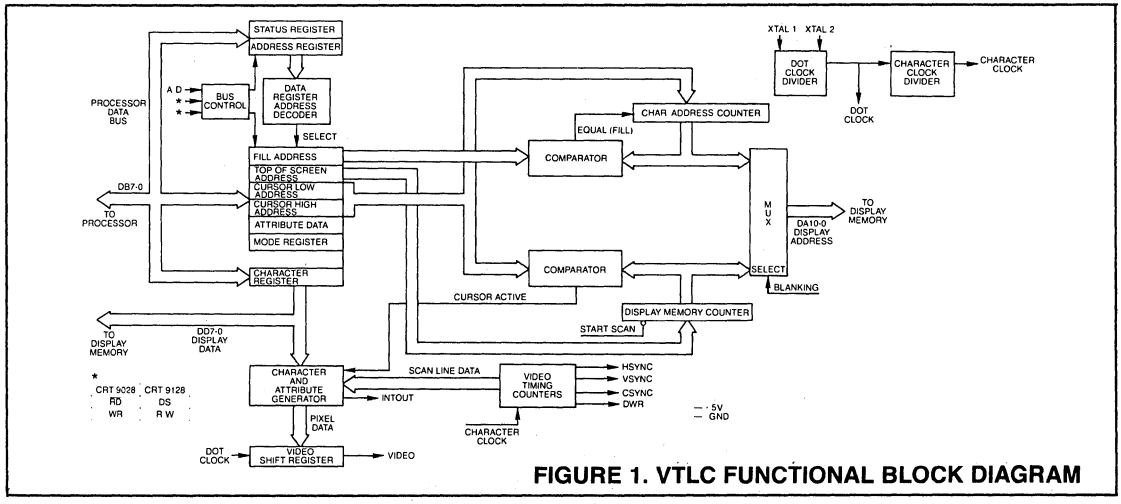



**FIGURE 1. VTLC FUNCTIONAL BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | I/O | NAME | DESCRIPTION |
|---|---|---|---|---|
| 3-1, 40-33 | DA10-0 | O | Display Address | 11 bit address bus to display memory |
| 4 | GND | | Ground | Ground Connection |
| 5,6 | XTAL2,1 | I | Crystal 2,1 | External Crystal<br>An external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating). |
| 7 | $\overline{\text{VIDEO}}$ | O | $\overline{\text{Video Output}}$ | This output is a digital TTL waveform used to develop the VIDEO and composite VIDEO signals to the monitor. The polarity of this signal is: HIGH = BLACK<br>LOW = WHITE |
| 8 | INTOUT | O | Intensity Output | This pin is the intensity level modification attribute bit (synchronized with the video data output). |
| 9 | $\overline{\text{DWR}}$ | O | $\overline{\text{Display Write}}$ | Write strobe to display memory |
| 17-10 | DD7-0 | I/O | Display Data | 8-bit bidirectional data bus to display memory |
| 18 | HSYNC | O | Horizontal Sync | Horizontal sync signal to monitor |
| 19 | VSYNC | O | Vertical Sync | Vertical sync signal to monitor |
| 20 | CSYNC | O | Composite Sync | This output is used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor. |
| 21 | $V_{cc}$ | | Power | 5.0 V power connection |
| | | | **CRT 9028** | |
| 22 | $\overline{\text{WR}}$ | I | $\overline{\text{Write Strobe}}$ | Causes data on the microprocessor data bus to be strobed into the VTLC |
| 23 | $\overline{\text{RD}}$ | I | $\overline{\text{Read Strobe}}$ | Causes data from the VTLC to be strobed onto the microprocessor data bus |
| | | | **CRT 9128** | |
| 22 | R/$\overline{\text{W}}$ | I | Read/$\overline{\text{Write}}$ Select | Determines whether the processor is reading data from or writing data into the VTLC (high for read, low for write) |
| 23 | $\overline{\text{DS}}$ | I | $\overline{\text{Data Strobe}}$ | Causes data to be strobed into or out of the VTLC from the microprocessor data bus depending on the state of the R/W signal |
| 24 | A/$\overline{\text{D}}$ | I | Register Select | The state of this input pin will determine whether the data is being read from, or written to, the address or status register, or a data register. |
| 32-25 | DB7-0 | I/O | Processor Data Bus | 8-bit bi-directional processor data bus |

## DESCRIPTION OF OPERATION*

### THE VTLC INTERNAL REGISTERS

#### CRT 9028

Addressing of the internal VTLC data registers of the CRT 9028 is accomplished through the use of the A/$\overline{D}$ select input qualified by the $\overline{RD}$ and $\overline{WR}$ strobes.

| A/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | REGISTER OPERATION |
|---|---|---|---|
| 0 | 1 | 0 | WRITE TO DATA REGISTER |
| 0 | 0 | 1 | READ DATA REGISTER |
| 1 | 1 | 0 | WRITE TO ADDRESS REGISTER |
| 1 | 0 | 1 | READ STATUS REGISTER |

#### CRT 9128

Addressing of the internal VTLC data registers of the CRT 9128 is accomplished through use of the A/$\overline{D}$ and R/$\overline{W}$ select inputs qualified by the $\overline{DS}$ strobe.

| A/$\overline{D}$ | $\overline{DS}$ | R/$\overline{W}$ | REGISTER OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | WRITE TO DATA REGISTER |
| 0 | 0 | 1 | READ DATA REGISTER |
| 1 | 0 | 0 | WRITE TO ADDRESS REGISTER |
| 1 | 0 | 1 | READ STATUS REGISTER |

The contents of the seven processor programmable registers located in the upper left hand side of the Functional Block Diagram of figure 1 indicate the memory locations from which screen data is to be fetched and displayed as well as the selected modes of display operation. These registers are addressed indirectly via the Address Register.

To access one of the seven eight-bit registers, the processor must first load the Address Register with the three-bit address of the selected data register. The next read or write to a data register will then cause the data register pointed to by the Address Register to be accessed. The Line A/$\overline{D}$ controls whether writing is occurring to the Address Register or to a data register. When a read operation is performed, A/$\overline{D}$ controls access to either the Status Register or to the data register selected by the Address Register.

### REGISTER DESCRIPTION

#### ADDRESS REGISTER

Writing a byte to the ADDRESS register will select the specified register the next time the processor writes to or reads the VTLC data registers. The data register addresses are as follows:

#### STATUS REGISTER

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register. This bit is used to synchronize data transfers between the processor and the VTLC. The VTLC will set the DONE bit to a logic one after completing a byte transfer command or a FILL operation. The DONE bit is set to a logic zero by reading from, or writing to, the CHARACTER register. The processor must wait until the DONE bit is 1 before attempting to change the CURSOR ADDRESS, in order to write a character to, or read a character from, the CHARACTER register.

STATUS REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| DONE | X | X | X | X | X | X | X |

DONE = 1 signifies that external processor is allowed to access cursor ADDRESS and/or CHARACTER registers.

DONE = 0 signifies that external processor must wait until VTLC completes transfer of data between display memory and CHARACTER register.

#### DATA REGISTERS

FILADD (Fill Address) This register contains the RAM address of the character following the last address to be filled. Writing to this register will enable the VTLC "fill" circuitry. The FILL operation will then be triggered by the next processor write to the CHARACTER register. The FILL operation will write the character in the CHARACTER register to every location in display memory starting with the address specified in the CURLO and CURHI registers through the location preceeding the address specified in the FILADD register. The cursor position is not changed after a FILL operation. Note that the address bits DA3-DA0 are internally forced to 0 forcing the FILADD address to be 00, 16, 32, etc. to 1920. The CURLO and CURHI registers will not be changed by this operation. Writing to the CHARACTER register will cause the VTLC to reset DB7 of the STATUS register to "0". Bit 7 will be set to 1 after the VTLC has filled the last memory location specified.

FILADD REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| X | DA10 | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 |

| ADDRESS | | | | | | | | TYPE | REGISTER |
|---|---|---|---|---|---|---|---|---|---|
| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| X | X | X | X | 0 | 1 | 1 | 0 | Write | CHIP RESET |
| X | X | X | X | 1 | 0 | 0 | 0 | Write | TOSADD |
| X | X | X | X | 1 | 0 | 0 | 1 | Write | CURLO |
| X | X | X | X | 1 | 0 | 1 | 0 | Write | CURHI |
| X | X | X | X | 1 | 0 | 1 | 1 | Write | FILADD |
| X | X | X | X | 1 | 1 | 0 | 0 | Write | ATTDAT |
| X | X | X | X | 1 | 1 | 0 | 1 | RD/WR | CHARACTER |
| X | X | X | X | 1 | 1 | 1 | 0 | Write | MODE REGISTER |

(X = don't care)

*NOTE: Chip Reset is required before starting operation.

TOSADD (Top of Screen Address) This register contains the RAM address of the first character displayed at the top of the video monitor screen. In addition, this register controls selection of either of two mask programmable vertical scan rates.

TOSADD REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TIM | DA10 | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 |

Note that address bits DA3-DAO are internally forced to 0 forcing the first address at the beginning of each row to be 00, 16, 32, etc. to 1920.

The most significant bit of this register (TIM) is used to select between the two mask programmed sets of vertical retrace parameters (scan A and scan B). This allows software selection of, for example, 50/60 HZ.

TIM = 0 enable raster scan A (60 Hz)
TIM = 1 enable raster scan B (50 Hz)

CURLO (Cursor Low) This register contains the eight lower order address bits of the RAM cursor address. All FILL screen and character transfer operations begin at the memory location pointed to by this address.

CURLO REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |

CURHI (Cursor High) This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8). All FILL screen and character transfer operations begin at the memory location pointed to by this address. In addition, this register contains the Smooth Scroll Offset Values SS3-SS0 which determine the number of scan lines that the data is shifted on the screen. The MSB of this register (SLE-status line enable) is the enable for the non-scrolling status line (this feature is available only on a part programmed for 25 data rows).

CURHI REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| SLE | SS3 | SS2 | SS1 | SS0 | DA10 | DA9 | DA8 |

SLE = 1 enables non-scrolling 25th status line
SLE = 0 disables and blanks non-scrolling status line

SS3-SS0 Smooth Scroll Offset Value

ATTDAT (Attribute Data) This register specifies the visual attributes of the video data and the cursor presentation. The visual attributes specified in the ATTDAT register (DB3-DB0) are enabled or disabled by a TAG bit that is appended to the ASCII character written to the CHARACTER register. Every character on the screen with its TAG bit set is displayed with the same attribute. Changing the Attribute register will change the attribute of every "tagged" character on the screen. The functions of the remaining bits in the ATTDAT register are not affected by the display character's TAG bit.

There are two display modes, "alphanumerics" and "graphics". In the alphanumeric mode, visual attributes may be selected by the TAG bit. In the graphics mode, a tagged character will be a normal alphanumeric character. This allows a screen to display a mix of graphic and alphanumeric characters or visually attributed alphanumeric characters. The display variations of the alphanumerics and graphics modes are summarized by the following:

ATTDAT REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|

| | | | |
|---|---|---|---|
| DB7 | MODE SELECT | DB7 = 1 | enables graphics mode display (No attributes allowed) |
| | | DB7 = 0 | enables alpha mode display |
| DB6 | CURSOR SUPPRESS | DB6 = 1 | inhibits VIDEO display at cursor time by forcing the VIDEO output to background level during cursor display time |
| | | DB6 = 0 | enables VIDEO display at cursor time<br>Note: a blinking cursor display can be achieved by toggling this bit under processor control. |
| DB5 | CURSOR DISPLAY | DB5 = 1 | enables underline cursor display |
| | | DB5 = 0 | enables block cursor display<br>Note: An underline cursor in an underline character attribute field will be dashed. |
| DB4 | SCREEN | DB4 = 1 | for white screen and black characters |
| | | DB4 = 0 | for black screen and white characters<br>Note: this is a screen attribute (versus character attribute) bit and sets the default Video background level. |

ENABLED OR DISABLED BY TAG BIT

| | | | |
|---|---|---|---|
| DB3 | CHARACTER SUPPRESS | DB3 = 1 | to enable Video suppress |
| | | DB3 = 0 | to inhibit Video suppress<br>This bit allows character blinking and blanking under processor control |
| DB2 | INTENSITY | DB2 = 1 | allows the INTOUT output pin to go high for the character time |
| | | DB2 = 0 | inhibits the INTOUT output pin from going high |
| DB1 | UNDERLINE | DB1 = 1 | will cause the character to be underlined |
| | | DB1 = 0 | will inhibit the underline |
| DB0 | REVERSE VIDEO | DB0 = 1 | will cause the standard foreground and background Video levels (selected with DB4) to be reversed for the character time |
| | | DB0 = 0 | will inhibit reverse video |

MODE

The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the VTLC after every read/write of the CHARACTER register. Note: The visible cursor position is not affected.

MODE REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| AUTO INC | X | X | X | X | X | X | X |

DB7 AUTO INCREMENT

DB7 = 1 to enable automatic character address
The RAM address is incremented after the VTLC completes a display memory access initiated by a processor to RAM or RAM to processor character transfer.

DB7 = 0 to disable automatic increment

CHARACTER

This register allows access to the display memory for both byte transfers and FILL operations. In BYTE Transfer Write Mode, the processor first writes a character to this register. The VTLC takes that character and stores it in the display memory in the location specified by the CURLO and CURHI registers. In Byte Transfer Read Mode, the processor reads this register causing the VTLC to fetch the character whose address is specified in the CURLO and CURHI registers from the display memory and place it in the CHARACTER register. The processor then reads the character and initiates another fetch from memory cycle. In FILL mode, writing a byte to this register will initiate a FILL operation. All VTLC/memory data transfers take place during horizontal and vertical video retrace blank time.

CHARACTER REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TAG BIT + 7 BIT ASCII CHARACTER | | | | | | | |

## CHARACTER SET

Using the DB7-DB0 data bus I/O pins and the MOD SEL bit in the ATTDAT register, the user can address 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity. Included in the 128 mask programmable characters can be the 96 standard ASCII characters and 32 special characters.

A. (MODE SEL = 1) GRAPHICS MODE

This mode allows an intermix of alpha-numeric and graphics characters. No attributes are permitted in this mode. If TAG BIT = 1, the character will be an alpha-numeric. If TAG BIT = 0, the character will be a graphics character.

CHARACTER REGISTER

ALPHANUMERIC: TAG BIT = 1

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TAG = 1 | ⟵ ALPHA-NUMERIC CHARACTER ⟶ | | | | | | |

DB6-DB0 Specify character

CHARACTER REGISTER

GRAPHICS: TAG BIT = 0

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TAG=0 | W/T | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |

DB6 W/T = 1 specifies a wide graphics character
W/T = 0 specifies a thin graphics character

WIDE GRAPHICS ONLY:

DB5-4 SEG6-5 = 1 to turn on graphics entity segment
SEG6-5 = 0 to turn off graphics entity segment

Note that DB5 and DB4 have no meaning in the thin graphics entity.

SECTION V

WIDE AND THIN GRAPHICS:

DB3-0 SEG4-1 if any bit = 1, corresponding graphics entity segment ON

It any bit = 0, corresponding graphics entity segment OFF

B. (MOD SEL = 0) ALPHA-NUMERICS MODE

This mode allows display of alpha-numeric characters with attributes. If DB7 is set to a logical one, the attribute(s) specified in the ATTDAT register will be enabled for that character. If TAG BIT is cleared, attributes will not be enabled for that character.

CHARACTER REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TAG | ⟵ ALPHA-NUMERIC CHARACTER ⟶ | | | | | | |

DB7 = 1 to enable attribute(s) for character.
DB7 = 0 to disable attribute(s) for character.

DB6-DB0 Specify character

| | |
|---|---|
| SEGMENT 6 | SEGMENT 3 |
| SEGMENT 5 | SEGMENT 2 |
| SEGMENT 4 | SEGMENT 1 |

WIDE GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

| | |
|---|---|
| | SEGMENT 3 |
| SEGMENT 4 | SEGMENT 2<br>SEGMENT 1 |

THIN GRAPHICS ENTITY

NOTE: scan line and column of segment locations are mask programmable.

## DESCRIPTION OF SYSTEM OPERATION

The VTLC circuitry provides two control functions. One function interprets and controls data from the system processor interface through the data bus DB7-DB0 as shown in the Processor Timing of figure 3. The other function generates and refreshes the video image on the screen through the DD7-DD0 data bus as shown in the Display Memory Timing of figure 2. Because the system data bus is isolated from the display data bus, the VTLC maintains complete control over access to display memory. All data flow between display RAM and the processor or the VTLC takes place through the VTLC. Refer to the VTLC Display Memory Access Timing of figure 7.

### DISPLAY MEMORY ACCESS

Processor/display memory access is accomplished through the CHARACTER register of the VTLC. All processor transfers to or from the CHARACTER register take place only when the DONE bit is high. The DONE bit is used to synchronize data transfers between the VTLC and the processor as shown in the Typical Processor To Display Memory Transfer of figure 6. When the processor needs to store a byte of data in the display memory, it will write the byte to the CHARACTER register of the VTLC. The VTLC will immediately reset the DONE bit indicating that the transfer hardware is busy. At the next blanked Video time, the VTLC will store the byte in the display memory, increment the character address, (if auto increment is enabled) and set the DONE bit. When the processor needs to read a byte of data from the display memory, it will read the CHARACTER register. The VTLC will fetch the desired byte from the display memory during the next blanked VIDEO time, increment the character address (if enabled), and set the DONE bit. When the processor detects that the DONE bit is set, it will read the CHARACTER register to get the data byte from the VTLC. This read will reset the DONE bit and cause the VTLC to fetch the next byte of data from the memory.

If auto increment is not enabled, the processor must set the cursor address in the CURLO and CURHI register to the address of the memory location being read from, or written into, before every access to the CHARACTER register.

It should be noted that Auto Increment does not affect the visible cursor location. If auto-increment is enabled, the current character location will equal the cursor position only for the first character transfered following an update of the CURLO and CURHI registers. Note that the DONE bit must be high before attempting to update the cursor registers because the loading of the cursor registers will reset the character position counters to the cursor position.

### SMOOTH SCROLL

The VTLC may be programmed to do either "jump" or "smooth" scrolling. Jump scrolling moves the data up or down the monitor screen one data row at a time. Smooth scrolling moves the data up the monitor screen one scan line at a time. The number of scan lines and the rate they move up the screen is under processor control.

Smooth scroll is controlled through manipulation of the SS3-SS0 bits of the CURHI register. These bits represent the binary address of the first scan line of the first data row displayed on the monitor screen (the data row whose beginning address is in the TOSADD register). When the value represented by these bits is incremented, the video data on the monitor screen moves up by the same number of scan lines. After the address of the last scan line of the data row is loaded into the CURHI register and the VIDEO data has moved up the last scan line of the data row, the processor resets the SS3-SS0 address to point to scan line

0 and does a jump scroll. Jump scroll is accomplished by incrementing the RAM address in the TOSADD register by a data row length (so that it points to the address of the first character of the new top data row on the monitor).

When programmed for a data row of 80 characters/data row display (1920 data words), for example, the display RAM contains 25 actual rows of data (2000 RAM locations). If the smooth scroll offset equals zero, the VTLC will display the 1919 RAM locations following the top of screen address when displaying data. The first data row is partially scrolled off the screen and the 25th data row is scrolled onto the screen when the smooth scroll offset is incremented. The VTLC will now display the 1999 RAM locations following the top of screen address (wrapping to 0 after address 1999). After the VTLC does a jump scroll, the processor will program it to erase the line just scrolled off the screen (preparing it to be scrolled onto the screen). This line now becomes the non-displayed 25th data row.

## NON-SCROLLING STATUS LINE

The non-scrolling status line is only functional on a VTLC that has been programmed for 25 data rows. This data row will remain stationary at the bottom of the screen and will not move up the screen when the remainder of the display data is scrolled. Otherwise, VIDEO data on the status line may be manipulated as though it were normal display data. The smooth scroll offset will not function properly when the status line is enabled. The memory address of the characters on the status line are always characters 1920–1999.
NOTE: If the part is programmed for 25 data rows an additional mask option must be specified which makes the 25th data row either fixed (always displayed) or a status row (enabled/disabled by the SLE bit).

## CHIP RESET

The CRT 9028 and CRT 9128 Chip Reset requires two steps. The system processor first writes the reset address to the address register of the VTLC. The system processor then writes a dummy character to the VTLC Data register. Writing to the Data register resets the chip. The only state affected by the reset function is the setting of the DONE bit in the STATUS register.

**ROM CHARACTER BLOCK FORMAT**

| COLUMN DOT -> | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|---|
| SCAN LINE 0 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 1 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 2 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 3 -> | 0 | | | MASK PROGRAMMABLE | | | 0 | 0 |
| SCAN LINE 4 -> | 0 | | | CHARACTER BLOCK (FONT) 5 X 8 | | | 0 | 0 |
| SCAN LINE 5 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 6 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 7 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 8 -> | 0 | | | | | | 0 | 0 |
| SCAN LINE 9 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 10 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 11 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Mask programmable options–The ROM character block format above shows the 5X8 mask programmable character font within the character cell as defined by dots C7 through C0 and scan lines 0 through 11.

Dots/Character: 6 dots/character cell = > C7 - C2 displayed
7 dots/character cell = > C7 - C1 displayed
8 dots/character cell = > C7 - C0 displayed

Column dots C0 and C1 will be the same as column dot C7 when more than 6 dots/character cell are specified when generating alpha-numerics.

NOTE: The maximum dot clock crystal frequency is dependent on the dots/character programmed:

| DOTS/CHARACTER | MAX XTAL FREQ |
|---|---|
| 6 dots | 10.5 MHz max* |
| 7 dots | 12.25 MHz max* |
| 8 dots | 14.0 MHz max* |

*These values are preliminary

Scan Lines per Character: 8 scan lines character = > SL0 - SL7 displayed
9 scan lines character = > SL0 - SL8 displayed
10 scan lines character = > SL0 - SL9 displayed
11 scan lines character = > SL0 - SL10 displayed
12 scan lines character = > SL0 - SL11 displayed

Thin and Wide Graphics: Dots mask programmed for vertical column C2 will be the same as backfill Columns 0 and 1 when generating wide and thin graphics.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** (TA = 0°C to 70°C, $V_{cc}$ = +5V ±5%, unless otherwise noted.)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, Vil | | | 0.8 | V | |
| High-Level, Vih | 2.2 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, Vol | | | 0.4 | V | All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 1.6 mA |
| Low-level, Vol | | | 0.4 | V | $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 0.4 mA |
| High-level, Voh | 2.4 | | | V | All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −40 µA |
| High-level, Voh | 2.4 | | | V | $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −20 µA |
| INPUT LEAKAGE CURRENT | | | | | |
| High-level, Ilh | | | 10 | µA | All inputs; Vin = Vcc |
| Low-level, Iil | | | −10 | µA | All inputs except $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = .04V |
| Low-level, Iil | | | −200 | µA | $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V |
| INPUT CAPACITANCE | | | | | |
| All inputs, Cin | | | 15 | pF | |
| OUTPUT LOAD | | | | | |
| $C_L$ | | | 15 | pF | Except DB7-0 |
| $C_L$ | | | 100 | pF | DB7-0 |
| POWER SUPPLY CURRENT | | | | | |
| Icc | | 125 | | mA | |
| **AC CHARACTERISTICS** | | | | | |
| CLOCK FREQUENCY, fin | 1.0 | | 14.0 | MHz | |
| DISPLAY MEMORY TIMING | | | | | |
| Address Set-up Time | | | | | |
| $t_{AS}$ | 20 | | | ns | |
| Write Strobe Set-up Time | | | | | |
| $t_{WST}$ | 80 | | | ns | |
| Data Set-up Time | | | | | |
| $t_{ST}$ | 80 | | | ns | |
| Data Hold Time | | | | | |
| $t_{DH}$ | 10 | | 25 | ns | |

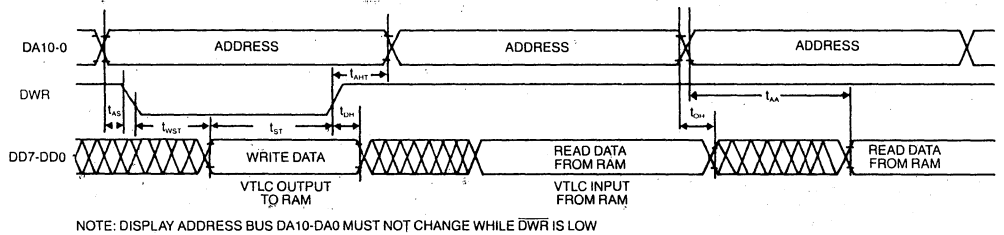
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| Address Hold Time $t_{AHT}$ | 25 | | | ns | |
| Output Hold From Address Change $t_{OH}$ | 15 | | | ns | |
| Address Access Time $t_{AA}$ | | | 250 | ns | |
| PROCESSOR TIMING | | | | | |
| Address Read/Write Set-up $t_{ARWS}$ | 160 | | | ns | |
| Write Pulse Width $t_{WPW}$ | 160 | | | ns | |
| Write Hold Time $t_{WHT}$ | 15 | | | ns | |
| Read Set-up Time $t_{RST}$ | | | 200 | ns | |
| Read Data Valid $T_{RDV}$ | 0 | | | ns | |
| Read Pulse Width $t_{RPW}$ | 250 | | | ns | |
| Data Write Falling Set-up $t_{DWFS}$ | 120 | | | ns | |
| Data Write Rising Set-up $t_{DWRS}$ | 160 | | | ns | |

Crystal specification (Applies for 4-14 MHz):

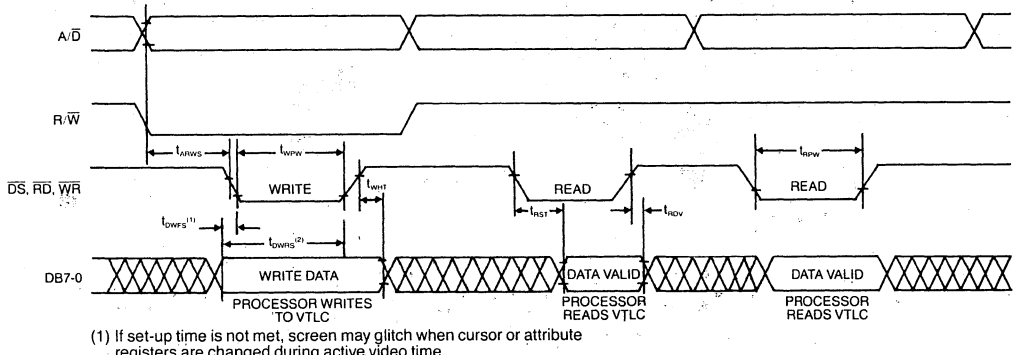
Series Resonant
50 ohms max series resistance
1.5 pf typ parallel capacitance
Operation below 4 MHz requires external crystal oscillator





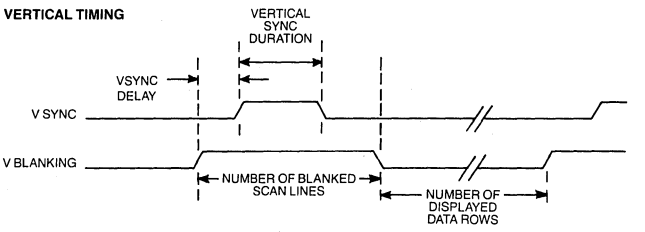

NOTE: DISPLAY ADDRESS BUS DA10-DA0 MUST NOT CHANGE WHILE $\overline{DWR}$ IS LOW

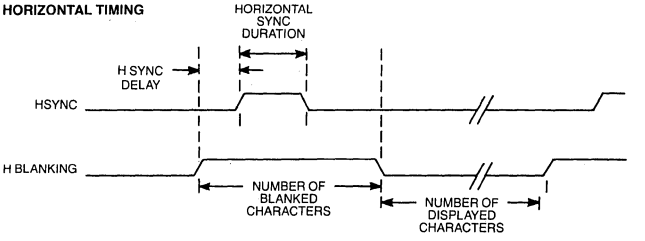
**FIGURE 2. DISPLAY MEMORY TIMING**




(1) If set-up time is not met, screen may glitch when cursor or attribute registers are changed during active video time.
(2) Minimum set-up time to ensure valid data into VTLC internal registers.

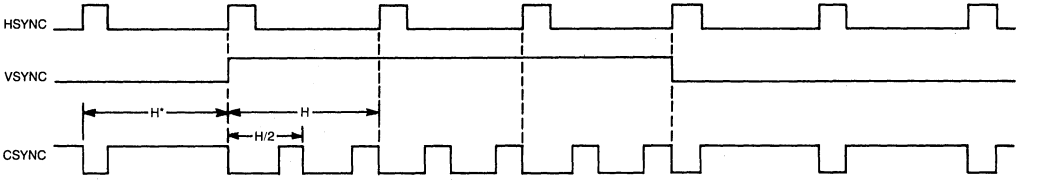
**FIGURE 3. PROCESSOR TIMING**



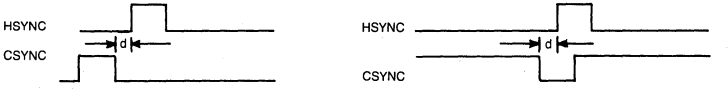




NOTE: Video parameters above are mask programmable

**FIGURE 4. VERTICAL AND HORIZONTAL SYNC TIMING**




NOTE: Delays between pulse edges and pulse width values may vary due to mask programmable features.
*H represents horizontal interval

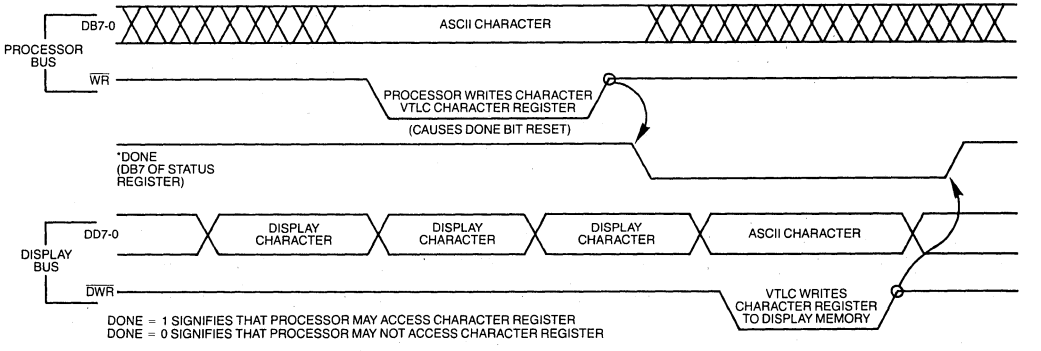



d = HSYN Delay -CSYN Delay

**WITHIN VERTICAL SYNC PULSE TIME**

**OUTSIDE OF VERTICAL SYNC PULSE TIME**

**FIGURE 5. VIDEO SIGNAL TIMING**




DONE = 1 SIGNIFIES THAT PROCESSOR MAY ACCESS CHARACTER REGISTER
DONE = 0 SIGNIFIES THAT PROCESSOR MAY NOT ACCESS CHARACTER REGISTER

**FIGURE 6. TYPICAL PROCESSOR TO DISPLAY MEMORY TRANSFER**

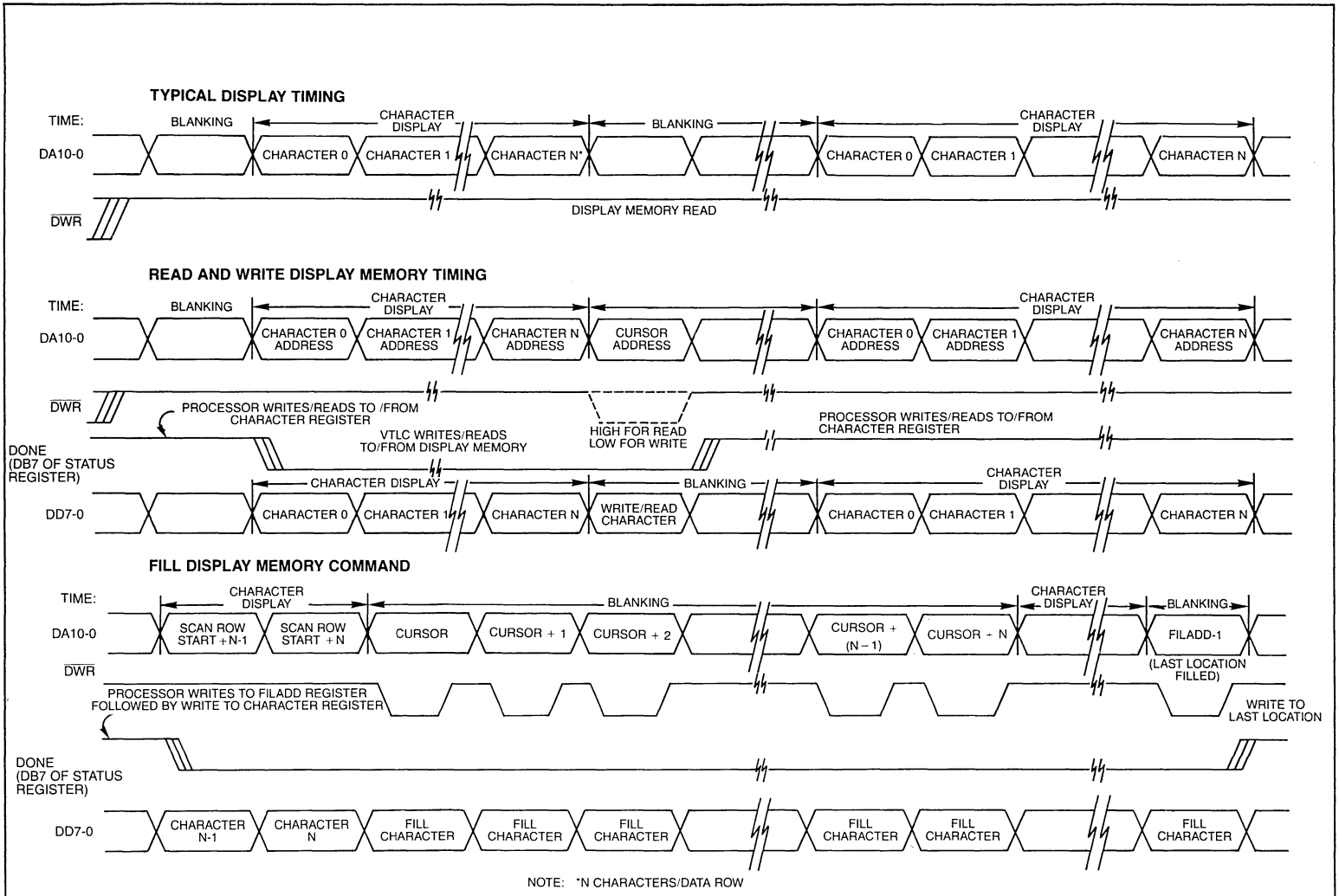



**FIGURE 7. VTLC DISPLAY MEMORY ACCESS TIMING**

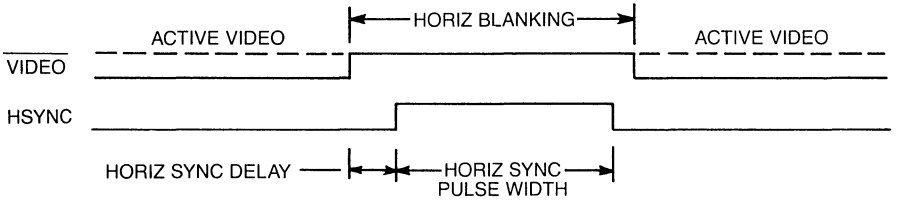
## I. ROM CHARACTER BLOCK FORMAT:

| COLUMN DOT | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
|---|---|---|---|---|---|---|---|
| SCAN LINE 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 1 | 0 | | | | | | 0 |
| SCAN LINE 2 | 0 | | | | | | 0 |
| SCAN LINE 3 | 0 | | CHARACTER BLOCK 5 X 8 CELL | | | | 0 |
| SCAN LINE 4 | 0 | | | | | | 0 |
| SCAN LINE 5 | 0 | | | | | | 0 |
| SCAN LINE 6 | 0 | | | | | | 0 |
| SCAN LINE 7 | 0 | | | | | | 0 |
| SCAN LINE 8 | 0 | | | | | | 0 |
| SCAN LINE 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

DOTS PER CHARACTER: 7
DOT CLOCK XTAL FREQUENCY (MHz): 10.92

## II. HORIZONTAL TIMING (IN CHARACTER TIMES):

CHARACTERS PER DATA ROW: 80
HORIZONTAL BLANKING: 20
HORIZONTAL SYNC DELAY: 4
HORIZONTAL SYNC PULSE WIDTH: 8
HORIZONTAL SYNC POLARITY: NEGATIVE ACTIVE

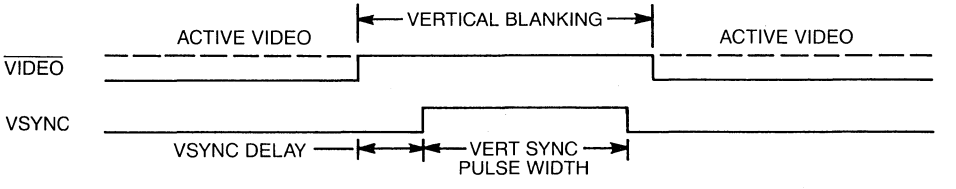



## III. VERTICAL TIMING:

CHARACTER ROWS: 24
SCAN LINES PER CHARACTER: x 10
TOTAL VISIBLE SCAN LINES: 240
VERTICAL SYNC POLARITY: NEGATIVE ACTIVE

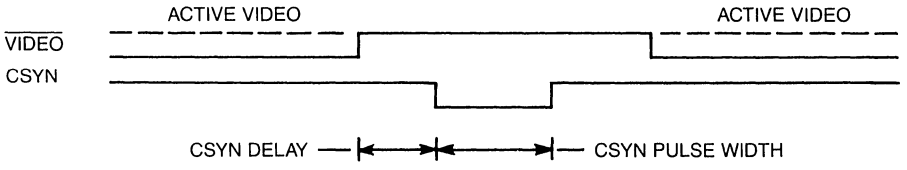
## IV. VERTICAL SYNC TIMING (IN SCAN LINES):

60 Hz VERTICAL BLANKING: 20
60 Hz VERTICAL SYNC DELAY: 4
60 Hz VERTICAL SYNC PULSE WIDTH: 8
ALTERNATE (50 Hz) VERTICAL BLANKING: 72
ALTERNATE (50 Hz) VERTICAL SYNC DELAY: 30
ALTERNATE (50 Hz) VERTICAL SYNC PULSE WIDTH: 10



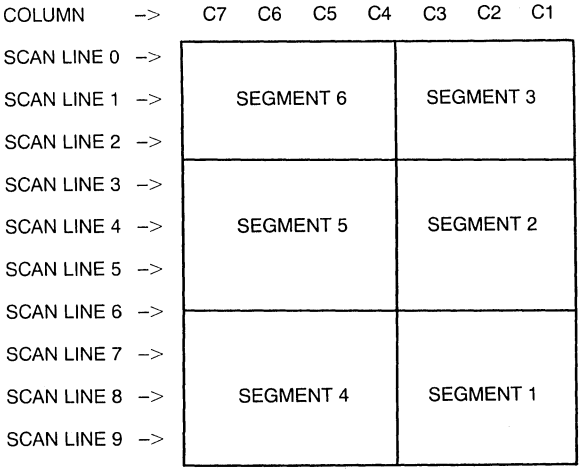
## V. COMPOSITE SYNC OUTPUT (IN CHARACTER TIMES):

COMPOSITE SYNC DELAY: 2
COMPOSITE SYNC PULSE WIDTH: 8

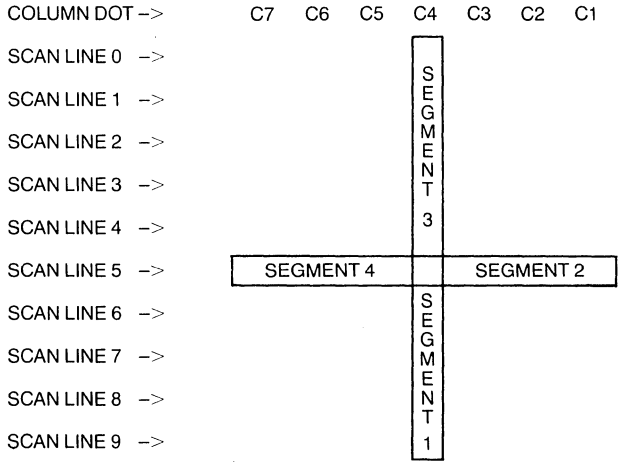



## VI. UNDERLINE ATTRIBUTE AND CURSOR LINE: SCAN LINE 9

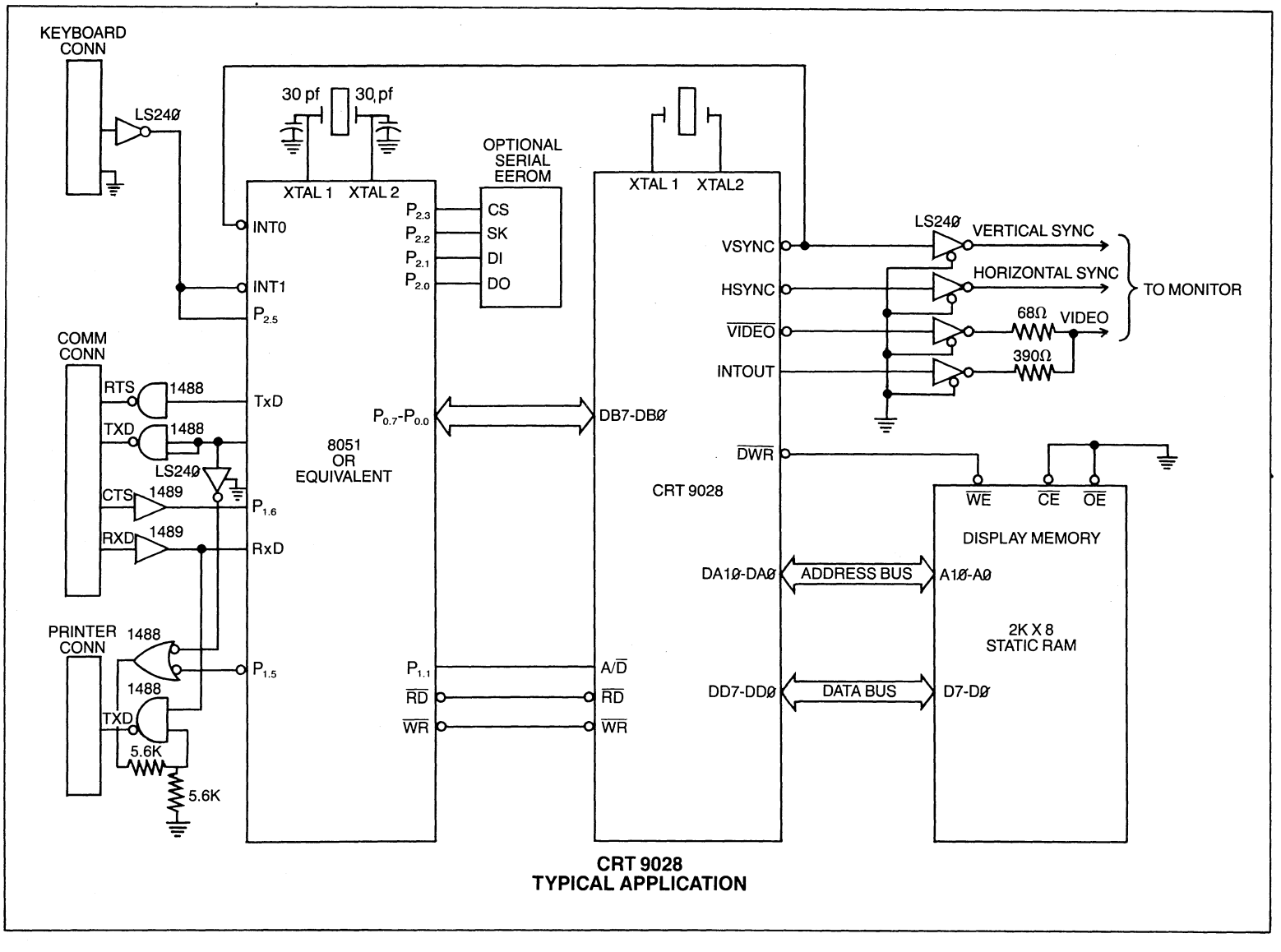
## VII. WIDE GRAPHICS FIGURE DEFINITION:



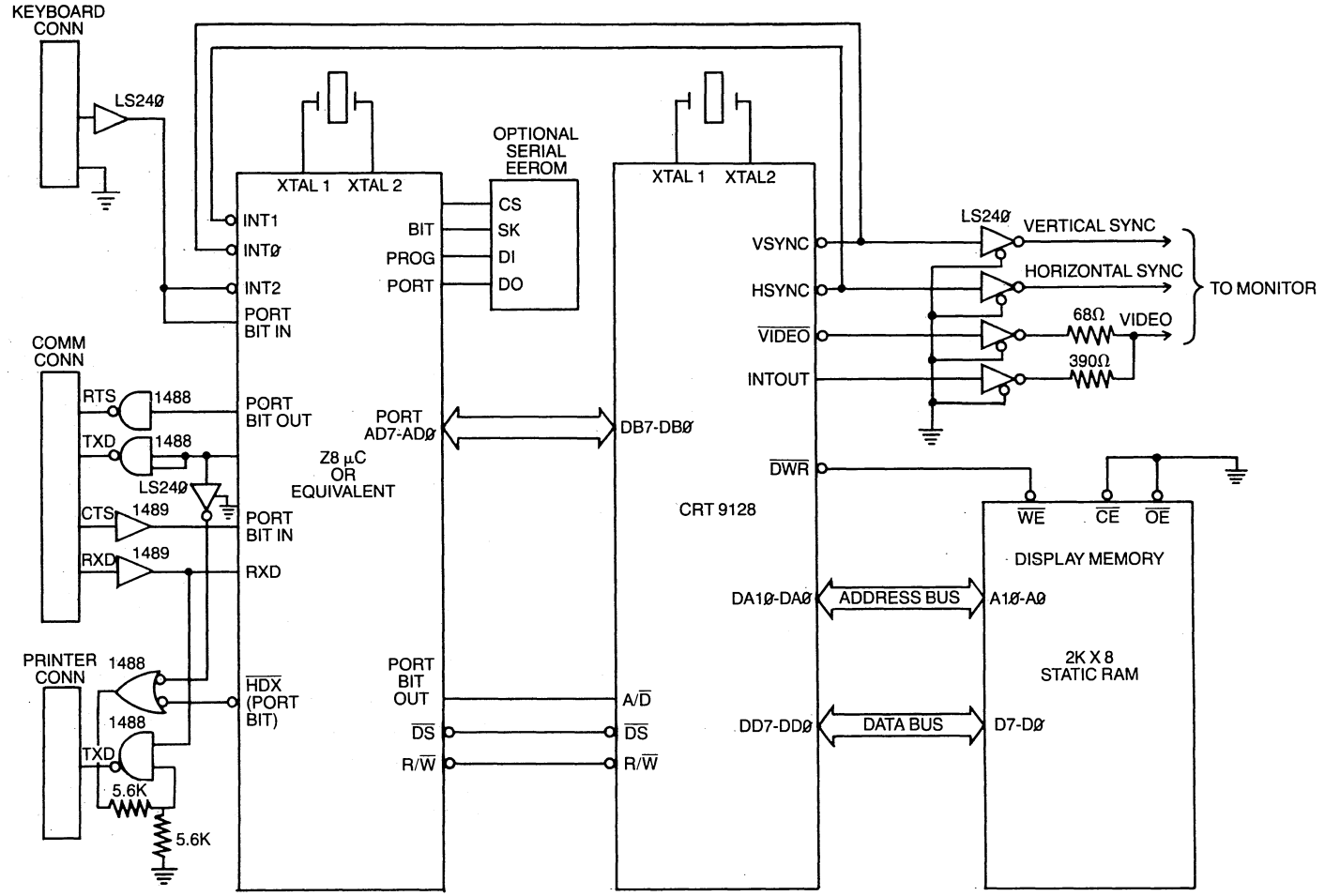

## VIII. THIN GRAPHICS FIGURE DEFINITION:




SEGMENT 4 = SCAN LINE 5; C7, C6, C5, C4
SEGMENT 3 = C4; SCAN LINES 0, 1, 2, 3, 4, 5
SEGMENT 2 = SCAN LINE 5; C4, C3, C2, C1
SEGMENT 1 = C4; SCAN LINES 5, 6, 7, 8, 9




**CRT 9028**
**TYPICAL APPLICATION**




**CRT 9128**
**TYPICAL APPLICATION**

## CRT 9028/9128-000

| DD6...DD4 \ DD3...DD0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 | C6-2 |
| 000 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 001 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 010 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 011 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 100 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 101 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 110 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |
| 111 | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL | SL |

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd, Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# CRT 9041A
# CRT 9041B
# CRT 9041C
**PRELIMINARY**

# CRT Video Attributes Controller VAC

## FEATURES

- ☐ On chip 12 bit shift register
  - 3 speed versions:
    - CRT 9041A -33MHz
    - CRT 9041B -30MHz
    - CRT 9041C -28.5MHz
- ☐ On chip attributes logic
  - Reverse video
  - Character blank
  - Character blink to blank
  - Character blink between any two of four video intensity levels
  - Two independent underline attributes
  - Four video intensity levels
  - Two general purpose attributes
- ☐ Wide graphics mode
- ☐ Thin graphics mode
- ☐ Reverse screen input
- ☐ On chip logic for double height/double width data rows
- ☐ Accepts scan line information in parallel or serial format
- ☐ Supports multiple cursors
- ☐ Four cursor modes dynamically selectable via 2 input pins
  - Underline
  - Blinking underline
  - Reverse video block
  - Blinking reverse video block
- ☐ Mask programmable cursor blink rate and duty cycle

## PIN CONFIGURATION

| | | | |
|---|---|---|---|
| CURS | 1 | 40 | Vcc |
| RETBL | 2 | 39 | GP2O |
| $\overline{LD}$/SH | 3 | 38 | GP1O |
| VDC | 4 | 37 | HINTO |
| VIDEO | 5 | 36 | BOLDO |
| DST | 6 | 35 | ATTEN |
| D11 | 7 | 34 | CHABL |
| D10 | 8 | 33 | UL2/GP2I |
| D9 | 9 | 32 | XCURS/GP1I |
| D8 | 10 | 31 | HINTI |
| D7 | 11 | 30 | BOLDI |
| D6 | 12 | 29 | BLINK |
| D5 | 13 | 28 | RS |
| D4 | 14 | 27 | REVID |
| D3 | 15 | 26 | MS1 |
| D2 | 16 | 25 | MSØ |
| D1 | 17 | 24 | $\overline{VSYNC}$ |
| D0 | 18 | 23 | SL0/SLD |
| SL3/BKC | 19 | 22 | SL1/$\overline{SLG}$ |
| GND | 20 | 21 | SL2/BLC |

- ☐ Mask programmable character blink rate and duty cycle
- ☐ On chip data and attribute latches
- ☐ Externally multiplexible for higher video rates
- ☐ Dot stretch on a character basis
- ☐ + 5 volt operation
- ☐ TTL compatible
- ☐ MOS n-channel silicon gate COPLAMOS® process
- ☐ Compatible with the CRT 5037 and CRT 9007

SECTION V

## GENERAL DESCRIPTION

The SMC CRT 9041 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device containing graphics logic, attributes logic, data and attribute latches, cursor control, and a high speed video shift register. The CRT 9041, a character generator ROM, and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9041 serial video output may be connected directly to a CRT monitor's video input. The CRT 9041 is available in three speed versions: 28.5 MHZ (9041C), 30 MHZ (9041B) and 33 MHZ (9041A).

The CRT 9041 attributes include: reverse video, 2 underlines, character blank, and character blink. Character blink may be to background, or between any 2 of 4 possible video intensity levels. Two output pins define 4 video levels: half, three quarters, full, and bold. When used in conjunction with the CRT 9007 VPAC™, the CRT 9041 will provide double height or double width data row display.

Two cursor input pins allow simultaneous display of two cursors. Each of these cursors can be displayed in one of 4 display formats: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, each cursor may be displayed in any of the 4 cursor display modes as selected via the two input pins. When used in the parallel scan line input mode, each cursor display mode is mask programmable and fixed at the time of manufacture.

The cursor format or the parallel scan line information can be changed on a character by character basis to allow different cursor formats on separate areas of the screen or for superscripted or subscripted characters.

Two graphics modes are provided. In the wide graphics mode, the CRT 9041 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms. In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided through the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal lines.

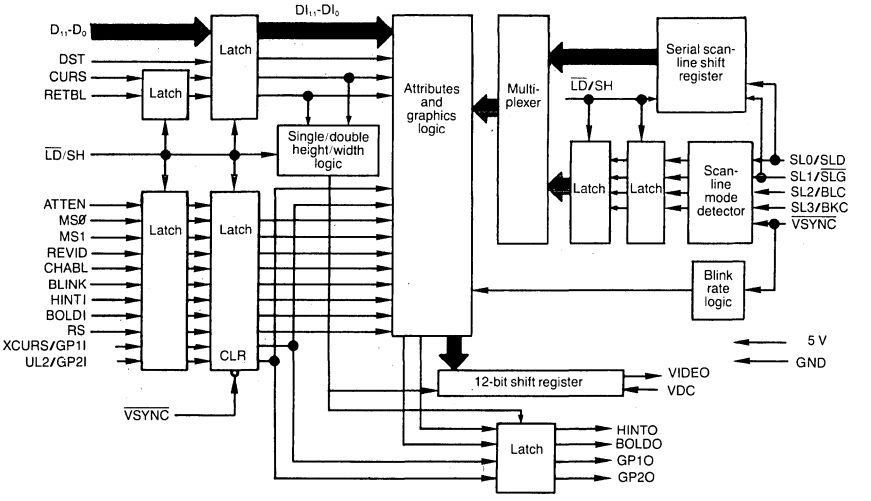



**FIGURE 1: CRT 9041 BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | Cursor | CURS | When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9041 enters the double width mode. See section entitled "Cursor Formats" for details. |
| 2 | Retrace Blank | RETBL | When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next $\overline{LD}$/SH pulse. This forces the Video output to a low voltage level, independent of all attributes for blanking the CRT during horizontal and vertical retrace time. |
| 3 | $\overline{Load}$/Shift | $\overline{LD}$/SH | The 12 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of $\overline{LD}$/SH. If the period of this signal is greater than 12 dots, video information will be supplied in the form of backfill dots as specified in the mask programmed options. |
| 4 | Video Dot Clock | VDC | This input clock controls the rate at which video data is shifted out on the VIDEO output. |
| 5 | Video | VIDEO | The Video output provides the serial dot stream to the CRT. Video data is shifted out on the rising edge of the video dot clock VDC. The timing of the $\overline{LD}$/SH input will determine the number of backfill dots. |
| 6 | Dot Stretch | DST | This input determines if all dots in the video stream will be stretched by one dot. In normal video, all 1's are stretched and in reverse video all 0's are stretched. This input enters the CRT 9041 along with D11-D0 with one $\overline{LD}$/SH delay. Updating can occur each $\overline{LD}$/SH to allow selected dot stretching on a character by character basis. A high voltage will cause the dot stretch and a low voltage will inhibit the dot stretch mechanism. See section entitled "Dot Stretch" for details. |
| 7-18 | Data | D11-D0 | In the character mode, the data on these inputs are passed through the attributes logic into the 12 bit high speed video shift register. The binary information on D11 will be the first bit output after the $\overline{LD}$/SH input goes low. In the thin or wide graphics mode only the D11 through D4 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Tables 5 and 6 illustrate the wide and thin graphics modes respectively and their relationships to D11-D4. |

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 19 | Scan line 3/<br>Block Cursor | SL3/BKC | Information on this input is delayed 2 $\overline{LD}$/SH cycles before entering the Attribute and Graphics Logic. As a result, this input can be changed on a character basis to allow the cursor format to enter the CRT 9041 as an attribute or to allow the parallel scan line information to change on a character basis. This input has two separate functions depending on the way scan line information is presented to the CRT 9041. In the Parallel Scan Line Mode, this input is the most significant bit of the binary scan line row address. In the Serial Scan Line Mode, this input controls the cursor's physical dimensions. If high, the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed. (See Table 4.) |
| 20 | Ground | GND | Ground |
| 21 | Scan line 2/<br>Blink Cursor | SL2/BLC | Information on this input is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic. As a result, this input can be changed on a character basis to allow the cursor format to enter the CRT 9041 as an attribute or to allow the parallel scan line information to change on a character basis. This input has two separate functions depending on the way scan line information is presented to the CRT 9041. (See Table 4.) |
| 22 | $\overline{\text{Scan Line 1/}}$<br>$\overline{\text{Scan Line Gate}}$ | SL1/$\overline{SLG}$ | This input has two separate functions depending on the way scan line information is presented to the CRT 9041. In the Parallel Scan Line Mode this input is the next to the least significant bit of the binary scan line row address. In this mode the information presented is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic to allow the scan line information to be changed on a character basis. In the Serial Scan Line Mode this input will be low for 5 or 6 $\overline{LD}$/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more $\overline{LD}$/SH pulses, the CRT 9041 will assume the parallel input scan line row address mode. |
| 23 | Scan line 0/<br>Scan Line data | SL0/SLD | This input has two separate functions depending on the way scan line information is presented to the CRT 9041. Refer to Table 4. In the Parallel Scan Line Mode this input is the least significant bit of the binary scan line row address. The information presented in this mode is delayed 2 $\overline{LD}$/SH cycles before entering the Attributes and Graphics Logic to allow the scan line information to be changed on a character basis. In the Serial Scan Mode this input will present the scan line information in serial form (least significant bit first) to the CRT 9041 and permits the proper scan line information to enter the serial scan line shift register during the $\overline{LD}$/SH pulses framed by $\overline{SLG}$. |
| 24 | $\overline{\text{Vertical}}$<br>$\overline{\text{Sync}}$ | $\overline{VSYNC}$ | This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the on-chip mask programmable blink rate dividers. The cursor blink rate can be a multiple or submultiple of the character blink which is selectable as a mask program option (see Table 10.) In addition, the internal attributes are reset when this input is low. The $\overline{VSYNC}$ input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes". |
| 25<br>26 | Mode Select 0<br>Mode Select 1 | MS0<br>MS1 | These 2 inputs define the four modes of operation of the CRT 9041 as follows:<br><br>MS1 / MS0 / MODE<br>0 / 0 / Wide graphics mode<br>1 / 0 / Thin graphics mode<br>0 / 1 / Character mode without underline one<br>1 / 1 / Character mode with underline one<br><br>See section entitled Display Modes for details. |
| 27 | Reverse Video | REVID | When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics Logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics Logic will invert the data before presenting it to the video shift register. |
| 28 | Reverse Screen | RS | This input defines the base background level of the screen. A low on this input will cause normal (non-reverse) video to appear white with a black background. A high on this input will cause normal (non-reverse) video to appear black with a white background. |

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 29 | Blink | BLINK | When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. This input allows a character to blink between 2 of 4 levels of video or to the background level according to one of the 3 mask programmable blink tables (Tables 1, 2 and 3). The duty cycle for the character blink is mask programmable at either 75/25 (off/on) or 50/50. |
| 30 | Bold in | BOLDI | The BOLDI input along with the BOLDO output provides a user with a Bold (high intensity) attribute on a character by character basis. Data input on BOLDI will appear at BOLDO with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise the voltage level of the video output to produce the bold attribute. |
| 31 | Half intensity in | HINTI | The HINTI input along with the HINTO output provides a user with a half intensity attribute on a character by character basis. Data input on HINTI will appear at HINTO with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to lower the voltage level of the video output to produce the half intensity attribute. |
| 32 | Extra Cursor/ General Purpose Attribute 1 In | XCURS/ GP1I | This input has a dual function. It can produce a second cursor with either a dynamically selectable format or a masked programmed format. If no scan line(s) are programmed for the XCURS format (or if the programmed scan lines are beyond the range of the actual scan lines), this input will simply be pipelined through the CRT 9041 to produce a user controlled general purpose attribute. Data appearing on this input is pipelined to the GP1O with the same delay as that from any other attribute input and can affect the video as desired. Whether XCURS is used or not, data appearing on this input will be pipelined to the GP1O output. |
| 33 | Underline 2 General Purpose Attribute 2 In | UL2/ GP2I | This input has a dual function. It can produce a second underline (UL2) at the masked programmed scan line(s). If no scan line(s) are programmed for underline 2, this input will simply be pipelined through the CRT 9041 to produce a user controlled general purpose attribute. Data appearing on this input is pipelined to the GP2O with the same delay as that from any other attribute input and can affect the video as desired. Whether UL2 is used or not, data appearing on this input will be pipelined to the GP2O output. Note that underline 1 is selected via the MS0 and MS1 inputs. |
| 34 | Character Blank | CHABL | When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID and RS) thus providing a constant video level for the entire length of the character block. Only the cursor is visible in a character blank field. |
| 35 | Attribute Enable | ATTEN | When this input is high, the internal attribute latch is updated at the positive going edge of the $\overline{LD}$/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK, BOLDI, HINTI, UL2/GP2I, DST RS, and XCURS/GP1I inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tying this input high (thus allowing "invisible" attributes). All attributes are reset by the $\overline{VSYNC}$ input. |
| 36 | Bold out Out | BOLDO | This output is used in conjunction with the BOLDI input to provide a three character pipeline delay when creating a high intensity effect on the video bit stream. In addition, this output is activated independent of the BOLDI signal during certain character and cursor blink operations according to Tables 1, 2 and 3. |
| 37 | Half Intensity Out | HINTO | This output is used in conjunction with the HINTI input to provide a three character pipeline delay when creating a half intensity effect on the video bit stream. In addition, this output is activated independent of the HINTI signal during certain character and cursor blink operations according to Tables 1, 2 and 3. |
| 38 | General Purpose Attribute 1 out | GP1O | This output is used in conjunction with the XCURS/GP1I input and provides a three character pipeline delay to allow for general purpose attributes to be implemented. |
| 39 | General Purpose Attribute 2 out | GP2O | This output is used in conjunction with the UL2/GP2I input and provides a three character pipeline delay to allow for general purpose attributes to be implemented. |
| 40 | Supply Voltage | Vcc | + 5 volt power supply. |

## ATTRIBUTES FUNCTIONS

**Reverse Video** – The REVID input causes inverted data to be loaded into the video shift register.

**Character Blank** – The CHABL input forces the video to go to the current background level as defined by Reverse Video and Reverse screen. This attribute blanks all video with the exception of both cursor displays.

**Underline** – MS1, MS0 = 1,1 or UL2 = 1: either condition forces the video to the inverse of the background level (all 1's or all 0's) for all scan line(s) programmed for underline. The two underlines are independent.

**Half Intensity** – The HINTI input and the HINTO output allow a half intensity attribute to be carried through the pipeline of the CRT 9041. An external mixer can be used to combine VIDEO and HINTO to create a decreased white level in the video.

**Retrace Blank** – The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

**Bold** – The BOLDI input and the BOLDO output allow a bold (high intensity) attribute to be carried through the pipeline of the CRT 9041. An external mixer can be used to combine VIDEO and BOLDO to create an increased white level in the video.

**Blink** – The BLINK input will cause characters to blink in a number of mask programmable ways. Referring to Tables 1, 2 or 3, video can be made to blink between 2 or 4 possible video levels with either a 50/50 on/off or a 75/25 on/off duty cycle. The tables also illustrate that the blink levels can be programmed to be a function of the reverse video input attribute. A blinking cursor overrides the character blink for the scan lines programmed for cursor. The CRT 9041 can implement character blinking in several different mask programmable visual formats as shown in the Tables. The blink function illustrated in Table 2 implements CRT 9021 compatibility blinking.

The CRT 9041 may be mask programmed for one of three combinations of blinking operation. These are illustrated respectively in Tables 1, 2, and 3. Since 4 levels of video are possible, Tables 1 and 3 define the video blinking between 2 video levels and Table 2 defines the video blinking to the background level making this table compatible with the CRT 9021.

The Non-blink Option Table 1A shows the state of the video DATA (DATA = non inverted video, $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 1A result in a non-character blink display as compared to the video DATA shown in the Blink Combinations Option Table 1B.

(1) Reverse video = (REVID) and ($\overline{RS}$) or ($\overline{REVID}$) and (RS)

**TABLE 1A: NON-BLINK COMBINATIONS OPTION TABLE**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| BLINK | REVERSE VIDEO (1) | BOLDI | HINTI | VIDEO | BOLDO | HINTO |
| 0 | 0 | 0 | 0 | DATA | 0 | 0 |
| 0 | 0 | 0 | 1 | DATA | 0 | 1 |
| 0 | 0 | 1 | 0 | DATA | 1 | 0 |
| 0 | 0 | 1 | 1 | DATA | 1 | 1 |
| 0 | 1 | 0 | 0 | $\overline{DATA}$ | 0 | 1 |
| 0 | 1 | 0 | 1 | $\overline{DATA}$ | 0 | 1 |
| 0 | 1 | 1 | 0 | $\overline{DATA}$ | 0 | 0 |
| 0 | 1 | 1 | 1 | $\overline{DATA}$ | 1 | 1 |

**TABLE 1B: BLINK COMBINATIONS OPTION TABLE**

| INPUTS | | | | CHARACTER BLINK WITHOUT CURSOR (2) | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|
| BLINK | REVERSE VIDEO (1) | BOLDI | HINTI | | | BOLDO | | HINTO | |
| | | | | A* | B* | A* | B* | A* | B* |
| 1 | 0 | 0 | 0 | DATA | DATA | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | DATA | DATA | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | DATA | DATA | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | DATA | DATA | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | $\overline{DATA}$ | $\overline{DATA}$ | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | $\overline{DATA}$ | $\overline{DATA}$ | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | $\overline{DATA}$ | $\overline{DATA}$ | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | $\overline{DATA}$ | $\overline{DATA}$ | 0 | 1 | 0 | 1 |

The Blink Combinations Option Table 1B shows the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 1B result in a blinking character display as compared to the non-blinking video DATA shown in the Non-blink Combinations Option Table 1A. Since 4 levels of video are possible, Table 1B defines video blinking between 2 video levels. This is shown in the explanation Table 1C below. It should be noted that the designation NORMAL, ½ INTENSITY, ¾ INTENSITY and BOLD have been used arbitrarily. The actual video levels caused by the BOLDO and HINTO are defined by the external video mixing circuit.

**TABLE 1 C**

| BOLDO | HINTO | INTENSITY LEVEL | BLINK BETWEEN THESE 2 LEVELS (OFF-ON) | |
|---|---|---|---|---|
| | | | NON REVERSE VIDEO | REVERSE VIDEO |
| 0 | 0 | NORMAL (N) | N - ½ | N - ½ |
| 0 | 1 | ½ INTENSITY (½) | ½ - N | N - ½ |
| 1 | 0 | BOLD (B) | B - N | N - B |
| 1 | 1 | ¾ INTENSITY (¾) | ¾ - N | N - ¾ |

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(2) The combinations in Table 1 allow the user to define the cursor and the character blink interaction. A non-blinking cursor adds one more inversion to either a non-blinking character or a blinking character. A blinking cursor overrides a character blink for the scan lines programmed for cursor. A blinking cursor will introduce and then remove one more inversion to either a non-blinking character or a blinking character.

### TABLE 2A: ALTERNATE NON-BLINK COMBINATIONS FOR CRT 9021 COMPATIBILITY

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| BLINK | REVERSE VIDEO | BOLDI | HINTI | VIDEO | BOLDO | HINTO |
| 0 | 0 | 0 | 0 | DATA | 0 | 0 |
| 0 | 0 | 0 | 1 | DATA | 0 | 1 |
| 0 | 0 | 1 | 0 | DATA | 1 | 0 |
| 0 | 0 | 1 | 1 | DATA | 1 | 1 |
| 0 | 1 | 0 | 0 | $\overline{DATA}$ | 0 | 0 |
| 0 | 1 | 0 | 1 | $\overline{DATA}$ | 0 | 1 |
| 0 | 1 | 1 | 0 | $\overline{DATA}$ | 1 | 0 |
| 0 | 1 | 1 | 1 | $\overline{DATA}$ | 1 | 1 |

The Alternate Non-blink Combinations for CRT 9021 Compatibility Table 2A show the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 2A result in a non-character blink display as compared to video DATA shown in Alternate Blink Combinations for CRT 9021 Compatibility Table 2B.

### TABLE: 2B BLINK COMBINATIONS OPTION TABLE

| INPUTS | | | | CHARACTER BLINK WITHOUT CURSOR (1) | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| BLINK | REVERSE VIDEO | BOLDI | HINTI | | BOLDO | | HINTO | |
| | | | | | A* | B* | A* | B* |
| 1 | 0 | 0 | 0 | DATA 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | DATA 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | DATA 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | DATA 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | $\overline{DATA}$ 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | $\overline{DATA}$ 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | $\overline{DATA}$ 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | $\overline{DATA}$ 1 | 1 | 1 | 1 | 1 |

The Alternate Blink Combinations for CRT 9021 Compatability Table 2B show the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 2B result in a blinking character display as compared to the non-blinking video DATA shown in the Alternate Non-Blink Combinations for CRT Compatibility Table 2A. In this table, the BOLDO and HINTO attributes are controlled by the BOLDI and HINTI attributes making them truly general purpose.

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(1) The combinations in Table 2 allow the user to define the cursor and the character blink interaction. A non-blinking cursor adds one more inversion to either a non-blinking character or a blinking character. In both cases the character blinks to the background video level. A blinking cursor overrides a character blink for the scan lines programmed for cursor. A blinking cursor will introduce and then remove one more inversion to either a non-blinking cursor or a blinking character.

### TABLE 3A: NON-BLINK COMBINATIONS FOR THE STANDARD CRT 9041 (CRT 9041-004)

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| BLINK | REVERSE VIDEO | BOLDI | HINTI | VIDEO | BOLDO | HINTO |
| 0 | 0 | 0 | 0 | DATA | 0 | 0 |
| 0 | 0 | 0 | 1 | DATA | 0 | 1 |
| 0 | 0 | 1 | 0 | DATA | 1 | 0 |
| 0 | 0 | 1 | 1 | DATA | 1 | 1 |
| 0 | 1 | 0 | 0 | $\overline{DATA}$ | 0 | 0 |
| 0 | 1 | 0 | 1 | $\overline{DATA}$ | 0 | 1 |
| 0 | 1 | 1 | 0 | $\overline{DATA}$ | 1 | 0 |
| 0 | 1 | 1 | 1 | $\overline{DATA}$ | 1 | 1 |

The Non-blink Combinations for the Standard CRT 9041 of Table 3A shows the state of the video data (DATA = non inverted video; $\overline{DATA}$ = inverted video) and the value of the output attributes (BOLDO, HINTO) that can be applied to the video DATA as a function of the four input attributes. The BLINK = 0 inputs in Table 3A result in a non-character blink display as compared to video DATA shown in the Blink Combinations for the Standard CRT 9041 of Table 3B.

### TABLE 3B: BLINK COMBINATIONS FOR THE STANDARD CRT 9041 (CRT 9041-004)

| INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|
| BLINK | REVERSE | BOLDI | HINTI | NON-CURSOR(2) | BOLDO | | HINTO | |
| | | | | A* B* | A* | B* | A* | B* |
| 1 | 0 | 0 | 0 | DATA $\overline{DATA}$ | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | DATA $\overline{DATA}$ | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | DATA $\overline{DATA}$ | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | DATA $\overline{DATA}$ | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | $\overline{DATA}$ $\overline{DATA}$ | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | $\overline{DATA}$ $\overline{DATA}$ | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | $\overline{DATA}$ $\overline{DATA}$ | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | $\overline{DATA}$ $\overline{DATA}$ | 1 | 0 | 1 | 0 |

The Blink Combinations for the Standard CRT 9041 of Table 3B shows the state of the video DATA (DATA = non inverted video; $\overline{DATA}$ = inverted video) during a character blink cycle (TIME A = OFF, TIME B = ON). The values of the output attributes (BOLDO, HINTO) that can be applied to the video DATA are determined by the state of the four input attributes. The BLINK = 1 inputs in Table 3B result in the blinking character display as compared to the non-blinking video DATA shown in the Non-Blink Combinations for the Standard CRT 9041 Table 3A. Since 4 levels of video are possible, Table 3B defines video blinking between 2 video levels. This is shown by the explanation Table 3C below. It should be noted that the designation NORMAL, ½ INTENSITY, ¾ INTENSITY and BOLD have been used arbitrarily. The actual video level caused by the BOLDO and HINTO are defined by the external video mixing circuit.

### TABLE 3C

| BOLDO | HINTO | INTENSITY LEVEL | BLINK BETWEEN THESE 2 LEVELS (OFF-ON) NON REVERSE VIDEO | REVERSE VIDEO |
|---|---|---|---|---|
| 0 | 0 | NORMAL (N) | N - ½ | N - ½ |
| 0 | 1 | ½ INTENSITY (½) | ½ - ¾ | ½ - ¾ |
| 1 | 0 | BOLD (B) | B - N | B - N |
| 1 | 1 | ¾ INTENSITY (¾) | ¾ - N | ¾ - N |

*The duty cycle for the blink with respect to the video, HINT, BOLD is mask programmable with the following choices:

A = 75% OR 50% B = 25% OR 50% (A + B must equal 100%)

(2)The scan lines programmed for a non-blinking cursor force a non-blinking or blinking character to a normal video level and introduce one more level of inversion. A blinking cursor adds one more level of inversion to the video during the blink time to a non-blinking or blinking character.

## CURSOR FORMATS

Four cursor formats are possible with the CRT 9041. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option for each cursor independently. If the serial scan line input is used, the cursor format is dynamically selectable on a character by character basis via input pins 21 and 19 (SL2/BLC, SL3/BKC). See Table 4. The four cursor formats are as follows:

Underline – The cursor will appear as an underline. The position and width of the cursor underline is mask programmed. An underline cursor will add one more level of inversion to the video on the programmed scan line(s) for underline cursor.

Blinking Underline – The cursor will appear as an underline and introduce and then remove one more level of inversion to the video on the programmed scan line(s) for cursor underline. The cursor blink rate and duty cycle is mask programmable as outlined in Tables 1, 2 or 3.

Reverse Video Block – The cursor will appear as a reverse video block. The block cursor will add one more level of inversion to the video for all scan lines in the character cell.

Blinking Reverse Video – The cursor will appear as a blinking reverse video block. The cursor will introduce and then remove one more level of inversion to the video for all scan lines in the character cell. The cursor blink rate and duty cycle is mask programmable as outlined in Tables 1, 2 or 3.

In the parallel scan line mode it is possible to change the scan line count on a character by character basis. If the scan inputs are stable a time TS2 (figure 2) prior to the next rising edge of the LD/SH input the scan line count will enter the delay latch of the CRT 9041. In the serial scan line mode, it is possible to change the cursor format on a character by character basis with the timing identical to that described in the parallel scan line mode (TS2). This timing is shown in the AC timing diagram, Figure 2.

**TABLE 4: CURSOR FORMATS**

| Scan Line Input Mode | (PIN21) SL2/BLC | (PIN19) SL3/BKG | Cursor Function |
|---|---|---|---|
| Serial | 1 | 0 | Underline |
| | 1 | 1 | Reverse Video Block |
| | 0 | 0 | Blinking Underline |
| | 0 | 1 | Blinking Reverse Video Block |
| Parallel | X | X | Mask programmable only |

## DISPLAY MODES

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 6a and 6b illustrate a typical CRT 9041 configuration which operates in all display modes for the parallel and serial scan line modes respectively.

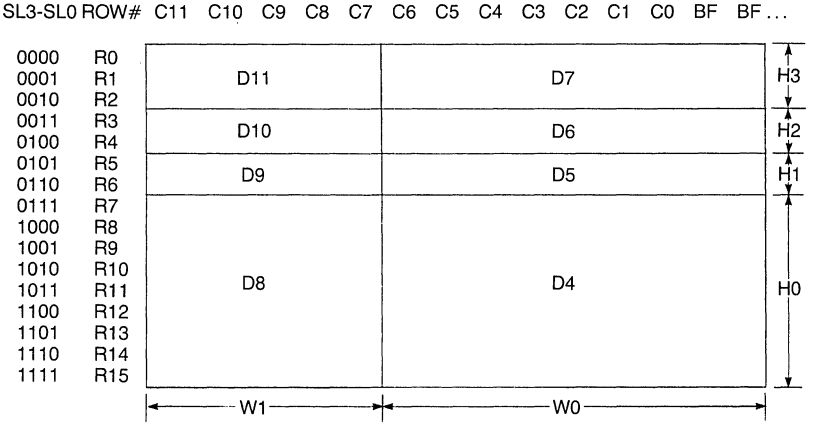
MS1,MS0 = 00–Wide Graphics Mode.
In this display mode, inputs D11-D4 define a graphic entity as illustrated in Table 5. Note that individual bits in D11-D4 will illuminate particular portions of the character block. Table 5 shows all programming ranges possible when defining the wide graphics boundaries. Only underline 2 is possible in this display mode.

MS1,MS0 = 10–Thin Graphics Mode.
In this display mode inputs D11-D4 define a graphic entity as illustrated in Table 6. Note that individual bits in D11-D4 will illuminate particular horizontal or vertical line segments within the character block. Table 6 shows all programming ranges possible when defining the thin graphics boundaries. Only underline 2 is possible in this display mode.

MS1,MS0 = 01–Character Mode without Underline 1.
In this display mode, inputs D11-D4 go directly from the input latch to the video shift register via the Attributes and Graphics Logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixel on the CRT) or a character generator as shown in Figures 6a and 6b. Underline 2 is available in this display mode.

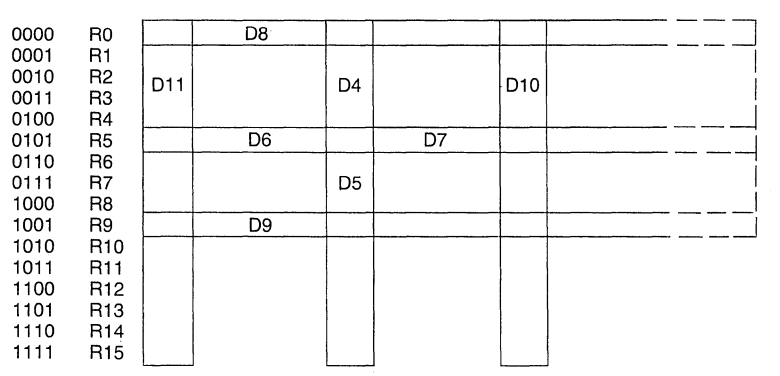
MS1,MS0 = 11–Character Mode with Underline 1.
Same operation as MS1, MS0 = 01 with the underline attribute byte appearing on the scan line(s) mask programmed. Underline 2 is available in this display mode.

## TABLE 5: WIDE GRAPHICS MODE




H0, H1, H2, H3, W0, W1, are mask programmable.
The values shown are for the CRT 9041-004.

## TABLE 6: THIN GRAPHICS MODE




| | VERTICAL HEIGHT | HORIZONTAL POSITION |
|---|---|---|
| D4 | R0-R5 | PROGRAMMABLE |
| D5 | R6-R15 | PROGRAMMABLE |
| D10 | R0-R15* | PROGRAMMABLE |
| D11 | R0-R15* | PROGRAMMABLE |

| | HORIZONTAL LENGTH | VERTICAL POSITION |
|---|---|---|
| D6 | C11-C7 | PROGRAMMABLE |
| D7 | C7-BF | PROGRAMMABLE |
| D8 | C11-BF* | PROGRAMMABLE |
| D9 | C11-BF* | PROGRAMMABLE |

The height of D4 and D5, the length of D6 AND D7, and the position of D4-D11 are mask programmable. The values shown are for the CRT 9041-004.
*These values are fixed

## DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. Figure 5 illustrates timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the cursor signal as required by the CRT 9041 with no additional hardware. It should be noted that the XCURSOR input will not affect the double width logic on the CRT 9041 in any way.

## SCAN LINE INPUT MODES

Scan line information can be introduced into the CRT 9041 in parallel format or serial. Table 7 illustrates the pin definition as a function of the scan line input mode. The CRT 9041 will automatically recognize the scan line mode by observing the activity on pin 22. In parallel mode, this input will be active low for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 22 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next frame. The parallel scan line input mode will be selected for the next frame if the following two conditions occur during the VSYNC low time. First, at least one positive transition must occur on pin 22 and second, pin 22 must be low for seven or more $\overline{LD}$/SH periods. Refer to Figure 4 for timing details. Whenever the CRT 9041 detects a change of scan line modes (from parallel to serial or visa versa), the internal blink counter will be initialized to a known count value. This allows the user to achieve phase synchronization of the blink rates from two or more CRT 9041's. This is useful if one multiplexes alternate dots from two CRT 9041's to double the allowable video dot rate.

**TABLE 7: PIN DEFINITION FOR PARALLEL**

| Scan Line Input Mode | CRT 9041 Pins | | | |
|---|---|---|---|---|
| | 23 | 22 | 21 | 19 |
| Serial | SLD | SLG | BLC | BKC |
| Parallel | SL0 | SL1 | SL2 | SL3 |

## DOT STRETCH

Dot stretch is a mechanism whereby a single illuminated dot will never stand alone in the video stream. This eliminates the intensity variation otherwise found between single and multiple dots by raising the intensity level of single dots up to the level of consecutively displayed dots. To accomplish this, each illuminated dot (represented by a logic "1") will be extended into the next dot position. The following example illustrates the dot stretch mechanism.

| | |
|---|---|
| Input bit pattern (D11-D0) | 1 0 0 1 0 1 1 0 0 1 0 0 |
| Output bit pattern | 1 1 0 1 1 1 1 1 1 0 1 1 0 |

For reverse video, logic "0"'s are stretched (logic "1" represents the background of the reverse video character). The following example illustrates the mechanism in reverse video.

| | |
|---|---|
| Input bit pattern (D11-D0) | 0 1 0 0 1 1 0 0 1 0 0 0 |
| Reverse video pattern | 1 0 1 1 0 0 1 1 0 1 1 1 |
| Output bit pattern | 1 0 0 1 0 0 0 1 0 0 1 1 |

In all cases, the next load of the shift register will always load the D11 bit to the output regardless of the value of the video output prior to the load. This dot stretch mechanism can be enabled on a character by character basis (or scan line by scan line) and is controlled by the DST input which is updated each $\overline{LD}$/SH period. The dot stretch signal enters the CRT 9041 with the D11-D0 inputs. In all cases, backfill (BF) is not affected by the dot stretch input.

## BACKFILL

Backfill is a mechanism that allows a character width of greater than 12 dots and provides dot information (usually blanks) for all dots beyond 12. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the end of the character by two methods which are mask programmable.

Method A– The backfill (BF) dots will be the same as the dot displayed in position C11.

Method B– The backfill (BF) dots will be the same as the dots displayed in position C0.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature in Range ..... 0° C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{cc}$ = +5V ±5%, unless otherwise noted)

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

### DC CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{IL}$ | | | 0.8 | V | All inputs except VDC, $\overline{LD}$/SH |
| Low Level $V_{IL}$ | | | 0.65 | V | For VDC, $\overline{LD}$/SH input |
| High Level $V_{IH1}$ | 2.0 | | | V | All inputs except VDC, $\overline{LD}$/SH |
| High Level $V_{IH2}$ | 4.3 | | | V | For VDC, $\overline{LD}$/SH input |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OH}$ = 0.4 mA |
| High Level $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 100μA |
| INPUT LEAKAGE CURRENT | | | | | |
| Leakage $I_{L1}$ | | | 10 | μA | $0 \leq V_{IN} < V_{cc}$; excluding VDC, $\overline{LD}$/SH |
| Leakage $I_{L2}$ | | | 50 | μA | $0 \leq V_{IN} \leq V_{cc}$; for VDC, $\overline{LD}$/SH |
| INPUT CAPACITANCE | | | | | |
| $C_{IN1}$ | | 10 | | pf | Excluding VDC, $\overline{LD}$/SH |
| $C_{IN2}$ | | 35 | | pf | $\overline{LD}$/SH |
| $C_{IN3}$ | | 35 | | pf | VDC |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 95 | | mA | |

### AC CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| VDC | 1.0 | | 33.0 | MHZ | CRT9041A |
| $1/t_{CY1}$ VDC frequency | 1.0 | | 30.0 | MHZ | CRT9041B |
| | 1.0 | | 28.5 | MHZ | CRT9041C |
| $t_{CKL}$ VDC low | 10 | | | ns | |
| $t_{CKH}$ VDC high | 10 | | | ns | |
| $t_{CKR}$ VDC rise time | | | 10 | ns | Measured from 10% to 90% points |
| $t_{CKF}$ VDC fall time | | | 10 | ns | Measured from 90% to 10% points |
| $\overline{LD}$/SH | | | | | |
| $t_{CY2}$ | 250 | | | ns | CRT9041A (1) |
| | 270 | | | ns | CRT9041B (1) |
| | 300 | | | ns | CRT9041C (1) |
| $t_{S1}$ | 7 | | | ns | |
| $t_{H1}$ | 0 | | | ns | |
| INPUT SETUP AND HOLD | | | | | |
| $t_{S2}$ | 60 | | | ns | CRT9041A } For inputs $\overline{SLG}$, SLD, |
| | 80 | | | ns | CRT9041B } $\overline{VSYNC}$ |
| | 110 | | | ns | CRT9041C } |
| | 35 | | | ns | For all other inputs except VDC, $\overline{LD}$/SH, $\overline{SLG}$, SLD, $\overline{VSYNC}$ |
| $t_{H2}$ | 10 | | | ns | For inputs $\overline{SLG}$, SLD, $\overline{VSYNC}$ |
| | 0 | | | ns | For all inputs except VDC, $\overline{LD}$/SH, $\overline{SLG}$, SLD, $\overline{VSYNC}$ |
| MISCELLANEOUS TIMING | | | | | |
| $t_{PD}$ | | | 30 | ns | CRT9041A |
| | | | 33 | ns | CRT9041B |
| | | | 35 | ns | CRT9041C |
| $t_{DW}$ | $t_{CY2}$ | | | | |

(1) When mask programmed for CRT 9021 compatibility TCY2 will be slower.

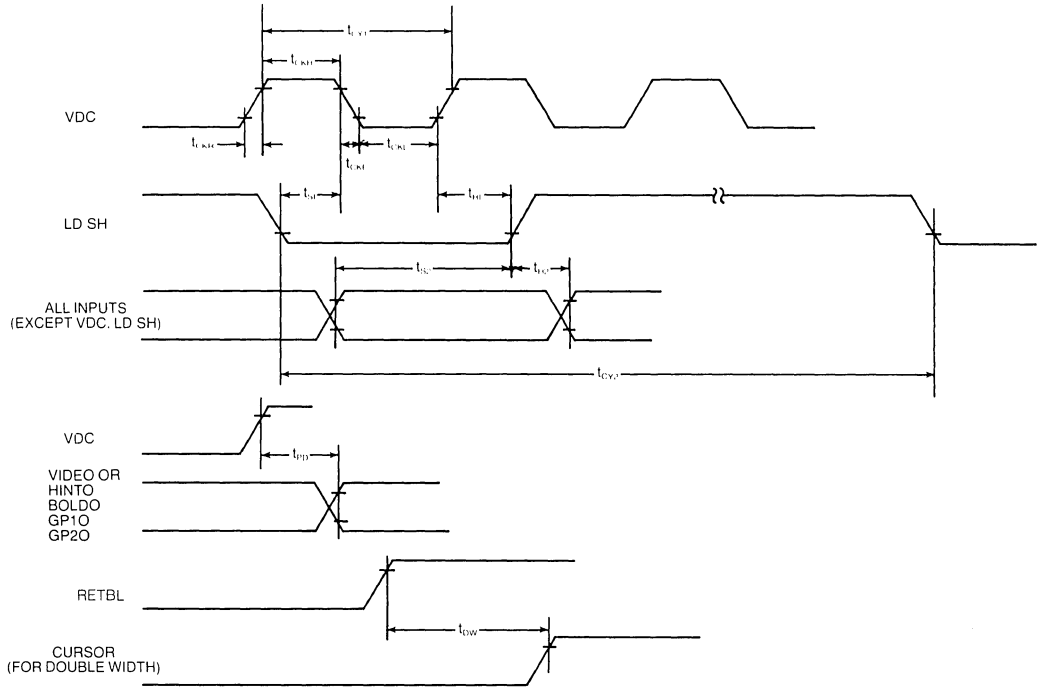



**FIGURE 2: CRT 9041 INPUT/OUTPUT TIMING**

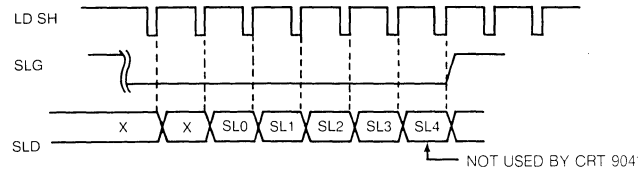



**FIGURE 3: SERIAL SCAN LINE MODE TIMING**

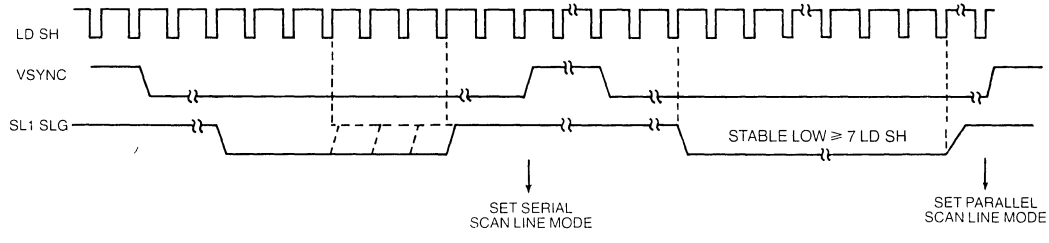
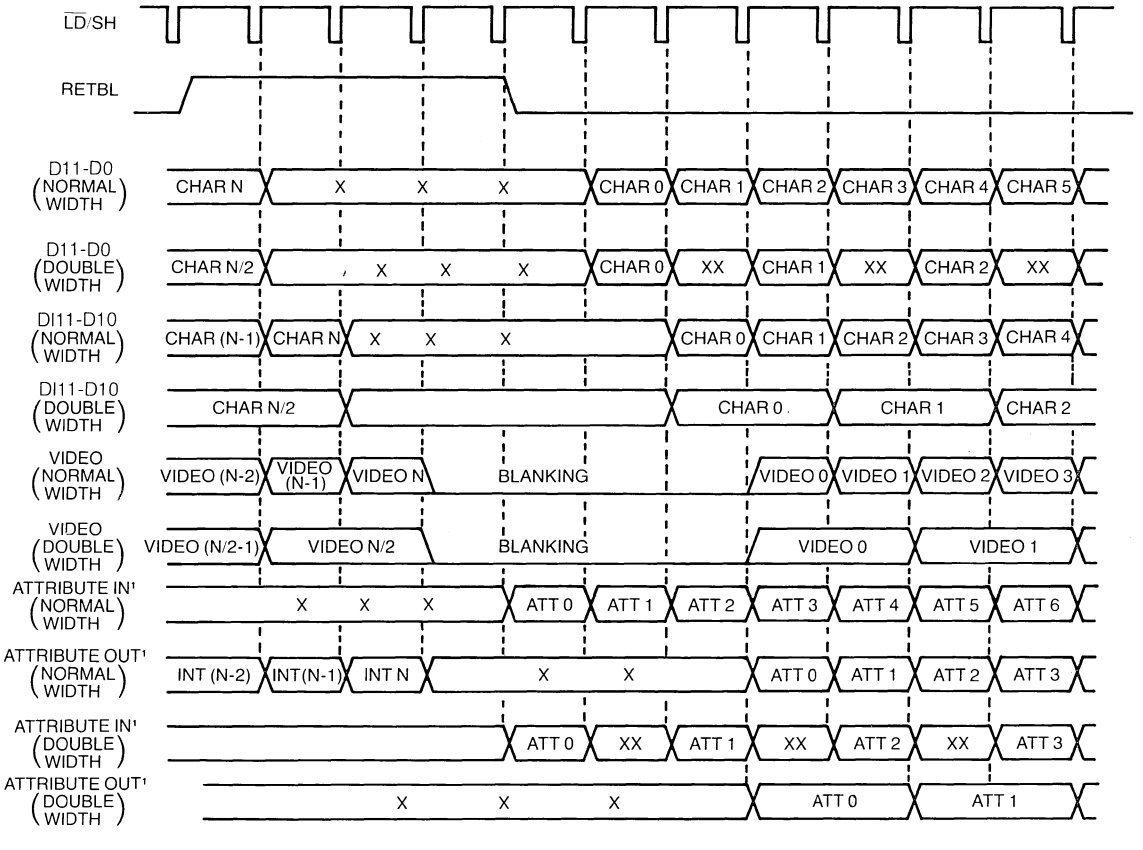



**FIGURE 4: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING**

SECTION V




1-Attributes include MS0, MS1, BLINK, CHABL, HINT, BOLD, REVID and XCURS

**FIGURE 5: CRT 9041 FUNCTIONAL I/O TIMING**

## PROGRAM OPTIONS

The CRT 9041 has a variety of mask programmed options. Tables 8 and 9 illustrate the range of these options for the wide and thin graphics modes respectively. Table 10 illustrates the range of the miscellaneous other mask programmed options. In addition, Tables 8, 9 and 10 show the mask programmed options for the CRT 9041-004.

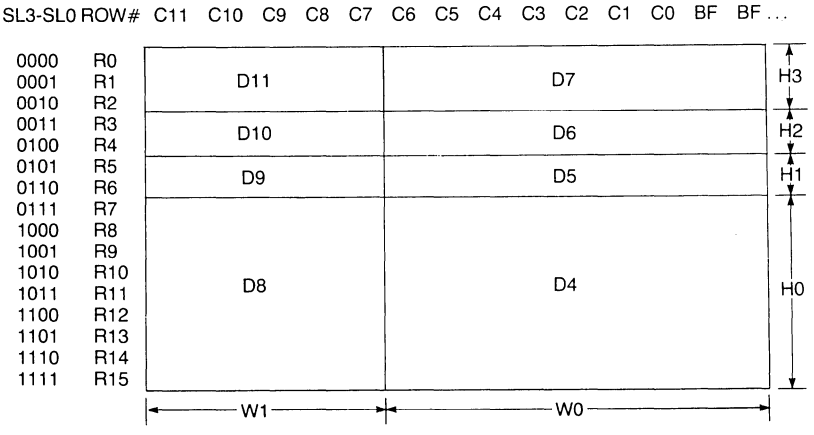
### TABLE 8: WIDE GRAPHICS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | CRT 9041-004 |
|---|---|---|
| Height of Graphic block* | | |
| D11 AND D7 | any scan line(s) | R0,R1,R2 |
| D10 AND D6 | any scan line(s) | R3,R4 |
| D9 AND D5 | any scan line(s) | R5,R6 |
| D8 AND D4 | any scan line(s) | R7 thru R15 |
| Width of graphic block** | any consecutive dots | C11 thru C7 |
| D11,D10,D9,D8 | C11 thru C0 | |
| D7,D6,D5,D4 | all remaining dots not specified above | C6 thru C0 plus BF |

*Any graphic block pair can be removed by programming for zero scan lines.

**Total number of dots for both must be equal to the total dots per character with no overlap. D11,D10,D9 and D8 must always be to the left of D7-D4.

### WIDE GRAPHICS



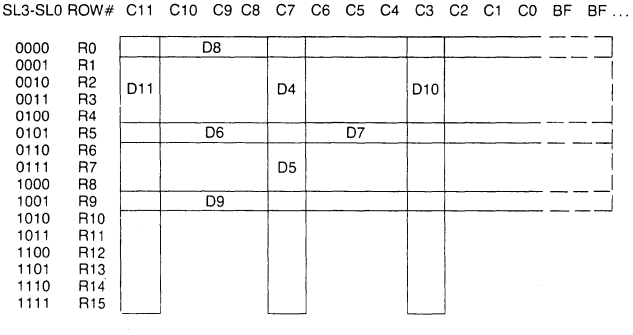

H0, H1, H2, H3, W0, W1, are mask programmable.
The values shown are for the CRT 9041-004.

## TABLE 9: THIN GRAPHICS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | STANDARD CRT 9041-004 |
|---|---|---|
| Backfill | any dot(s) within the programmed D7 range to the right of the programmed column(s) for D11. | C0 |
| Horizontal position for | | |
| D6 and D7 | any scan line(s) R0-R15 | R5 |
| D8 | any scan line(s) R0-R15 | R0 |
| D9 | any scan line(s) R0-R15 | R9 |
| Horizontal length for | | |
| D6 (1) | any consecutive dots | C11 thru C7 |
| D7 (1) | all dots not covered by D6 with one dot overlapping. | C7 thru BF |
| Blanked dots for serrated horizontal lines | | |
| D6 | any dot(s), BF programmed | none |
| D7 | any dot(s), BF programmed | none |
| D8, D9 | any dot(s), BF programmed | none |
| Vertical position for: | | |
| D4 and D5 | any dot(s) C11-C0,BF | C7 |
| D10 (2) | any dot(s) C10-C0,BF | C3 |
| D11 (2) | any dot(s) C11-C0 | C11 |
| Vertical length for: | | |
| D4 | any scan line(s) | R0 thru R5 |
| D5 | any scan lines not in D4 | R6 thru R15 |
| D10 | no choice; always R0 thru R15 | R0 thru R15 |
| D11 | no choice; always R0 thru R15 | R0 thru R15 |

(1) D6 and D7 must always overlap by 1 dot. This overlap may be blanked by specifying the proper column(s) in the serration program line. D7 must always be to the right of D6.
(2) D11 must always come before D10 with no overlap: otherwise D10 is lost.

## THIN GRAPHICS




| | VERTICAL HEIGHT | HORIZONTAL POSITION |
|---|---|---|
| D4 | R0-R5 | PROGRAMMABLE |
| D5 | R6-R15 | PROGRAMMABLE |
| D10 | R0-R15 | PROGRAMMABLE |
| D11 | R0-R15* | PROGRAMMABLE |

| | HORIZONTAL LENGTH | VERTICAL POSITION |
|---|---|---|
| D6 | C11-C7 | PROGRAMMABLE |
| D7 | C7-BF | PROGRAMMABLE |
| D8 | C11-BF* | PROGRAMMABLE |
| D9 | C11-BF* | PROGRAMMABLE |

The height of D4 and D5, the length of D6 AND D7, and the position of D4-D11 are mask programmable. The values shown are for the CRT 9041-004.
*These values are fixed

## TABLE 10: MISCELLANEOUS MASK PROGRAMMING OPTIONS

| OPTION | CHOICES | "STANDARD" CRT 9041-004 |
|---|---|---|
| Backfill in character mode | C11 or C0 | C11 |
| Character blink rate (division of VSYNC frequency) | 7.5 Hz to 0.5 Hz (1) (1) | 1.25Hz (1) |
| Cursor blink rate (2) | same as, half, or twice the character blink rate | 2.50 Hz (1) |
| Character blink duty cycle | 50/50 or 75/25 | 50/50 |
| Cursor blink duty cycle | 50/50 or 75/25 | 50/50 |
| Character underline 1 position | any scan line(s) R0 thru R15 | R8 |
| Character underline 2 position | any scan line(s) R0 thru R15 | R10 |
| Cursor underline position | any scan line(s) R0 thru R15 | R9 |
| Extra cursor underline position | any scan line(s) R0 thru R15 | R11 |
| Cursor format (3) | underline<br>blinking underline<br>reverse video block<br>blinking reverse video block | blinking reverse video block |
| Extra cursor format (3) | underline<br>blinking underline<br>reverse video block<br>blinking reverse video block | blinking underline |
| Blink table | Table 1<br>Table 2<br>Table 3 | Table 3 |
| CURSOR or XCURSOR effect on BOLDO and HINTO | no effect or force to zero at cursor position | force to zero at cursor position. |

(1) Assumes VSYNC input frequency of 60 HZ.
(2) Valid only if the cursor is formatted to blink.
(3) Valid for the parallel scan line mode only.

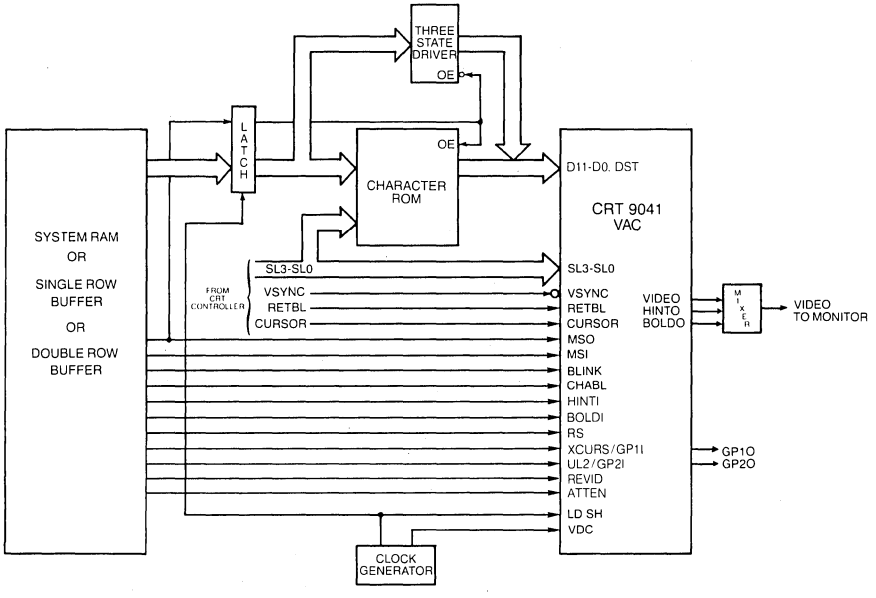



**FIGURE 6a: CRT 9041 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE**

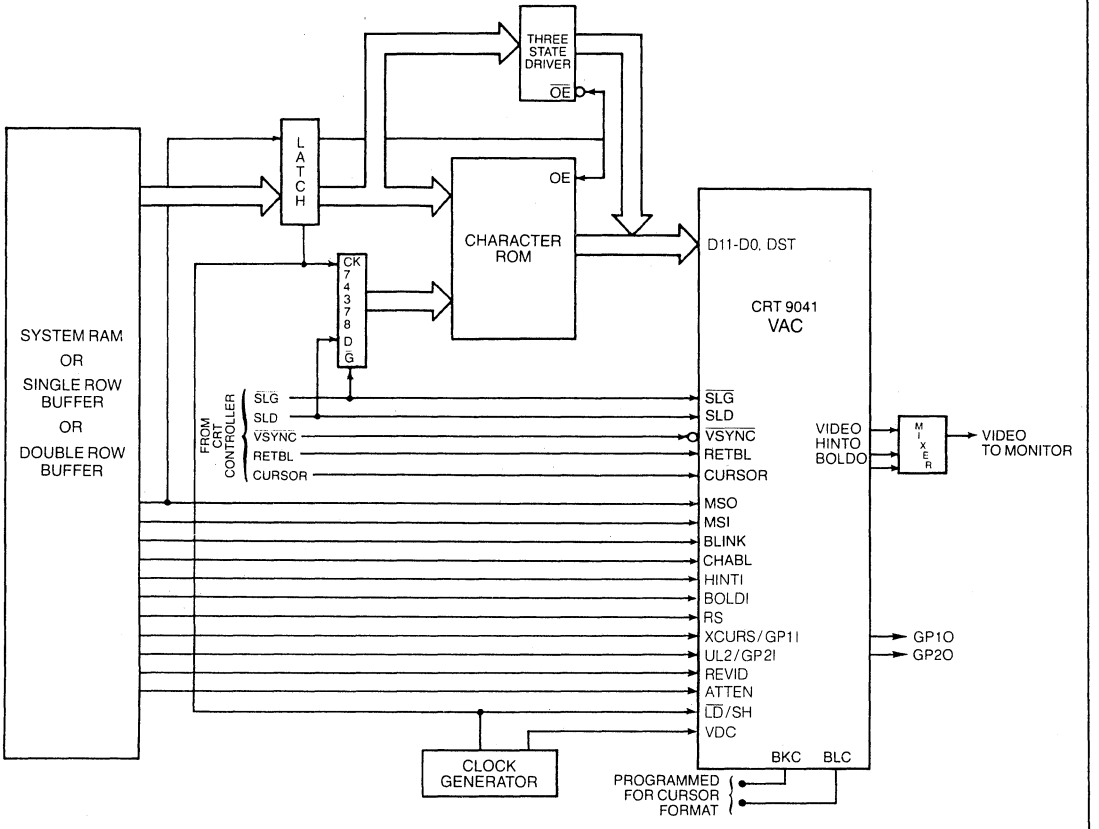



**FIGURE 6b: CRT 9041 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# CRT 9053
# CRT 9153

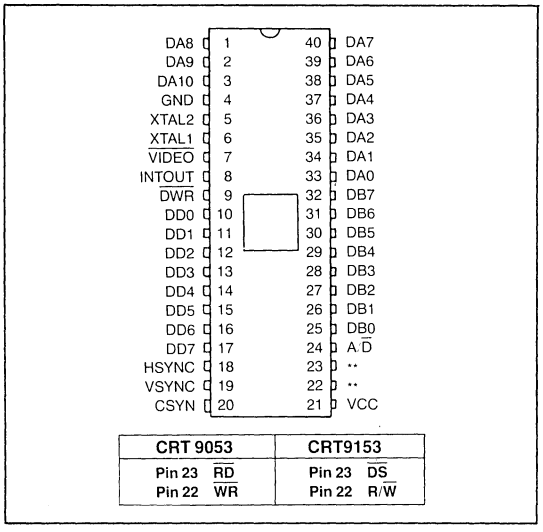
PRELIMINARY

# EVTLC
# Enhanced Video Terminal Logic Controller

## FEATURES

- ☐ Built-in High Frequency (4-18.7 MHz) Oscillator
- ☐ Built-in Video Shift Register
- ☐ Built-in Character Generator (128 Characters, 7x11 Dot Font)
- ☐ Bi-Directional Smooth Scroll Capability
- ☐ Visual Attributes Include Reverse Video, Intensity Control, Underline, and Character Blank and Blink
- ☐ Separate HSYNC, VSYNC and VIDEO Outputs
- ☐ Composite Sync (RS170 Compatible) Output
- ☐ Absolute (RAM address) Cursor Addressing
- ☐ MASK Programmable Video Parameters:
  - Dots Per Character Block (8-9)
  - Raster Scans Per Data Row (11-13)
  - Characters Per Data Row (32, 48,64,80)
  - Data Rows Per Page (8,10,12,16,20,24 or 25)
  - Horizontal Blanking (8-64 Characters)
  - Horizontal Sync Front Porch (0-7 Characters)
  - Horizontal Sync Duration (1-64 Characters)
  - Horizontal Sync Polarity
  - Two Values of Vertical Blanking
  - Two Values of Vertical Sync Front Porch (0-63 Scan Lines)
  - Two Values of Vertical Sync Duration (1-16 Scan Lines)
  - Vertical Sync Polarity
  - Internal 128 Character 7x11 Dot Font
  - Character/Cursor Underline Position
  - Character/Cursor Blink Rate
  - Scan Row and Column for Thin Graphics Entity Segments
  - Scan Rows and Columns for Wide Graphics Entity Elements
- ☐ Software Enabled Non-Scrolling 25th Data Row Available with 25 Data Row/Page Display
- ☐ Non-Interlace Display Format

## PIN CONFIGURATION




| CRT 9053 | CRT9153 |
|---|---|
| Pin 23 $\overline{RD}$ | Pin 23 $\overline{DS}$ |
| Pin 22 $\overline{WR}$ | Pin 22 R/$\overline{W}$ |

- ☐ Embedded Attribute or Tag Bit Attribute Capability
- ☐ Separate Display Memory Bus Eliminates Contention Problems
- ☐ Fill (Erase) Screen Capability
- ☐ Standard 8-bit Data Bus Microprocessor Interface
- ☐ Wide Graphics with Six Independently Addressable Segments Per Character Space
- ☐ Thin Graphics with Four Independently Addressable Segments Per Character Space
- ☐ Single +5V Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ TTL Compatible

## GENERAL DESCRIPTION

The CRT 9053 EVTLC and CRT 9153 EVTLC are mask programmable 40 pin COPLAMOS® n-channel MOS/LSI Video Display Controller Chips that combine video timing, video attributes, alphanumeric and graphics generation, smooth scroll and screen buffer interface functions.

The EVTLC incorporates many of the features (previously requiring a number of external components) required in building a low cost yet versatile display interface. An internal mask programmable 128 character font provides for a full ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

Two pinout configurations enhance the versatility of the EVTLC. The CRT 9053 controls data flow over the processor system data bus through separate read ($\overline{RD}$) and write ($\overline{WR}$) strobes for use with the 8085, 8051, Z80®, 8086, and similar microprocessors or microcomputers. The CRT 9153 regulates the data flow with a data strobe ($\overline{DS}$) and read/write (R/$\overline{W}$) enable signals for use with the 6500, Z8™, 68000 and similar microprocessors or microcomputers.

The EVTLC provides two independent data buses; one bus that interfaces to the processor and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the EVTLC eliminating contention problems and the need for a separate row buffer.

The EVTLC has an internal crystal oscillator requiring only an external crystal to operate. Masked constants for critical video timing simplify programming, operation and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

*Z80 is a registered trademark of Zilog Corporation.
Z8 is a trademark of Zilog Corporation.

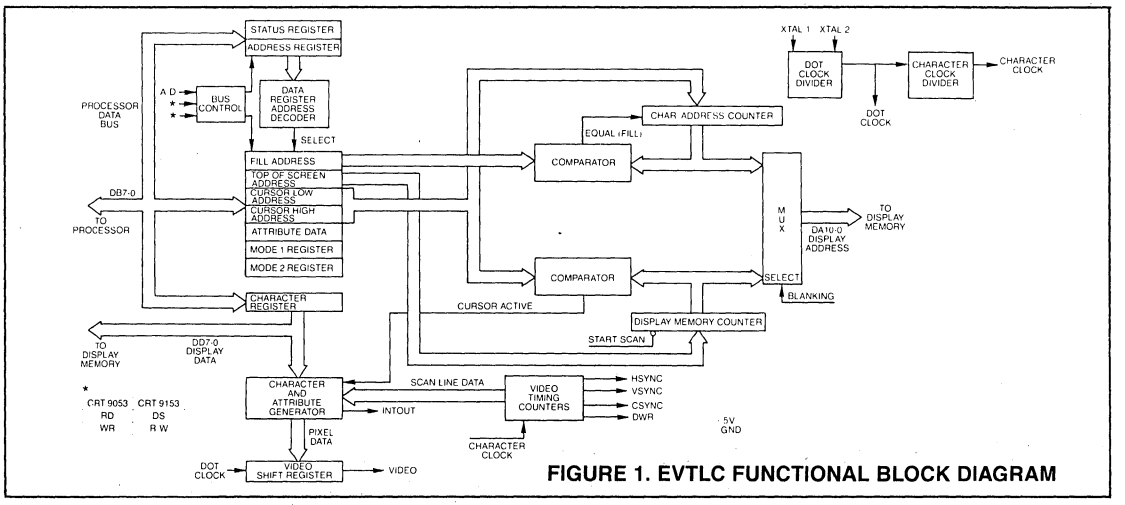



**FIGURE 1. EVTLC FUNCTIONAL BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | I/O | NAME | DESCRIPTION |
|---|---|---|---|---|
| 3-1, 40-33 | DA10-0 | O | Display Address | 11 bit address bus to display memory |
| 4 | GND | | Ground | Ground Connection |
| 5,6 | XTAL2,1 | I | Crystal 2,1 | External Crystal<br>An external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating). |
| 7 | $\overline{\text{VIDEO}}$ | O | $\overline{\text{Video Output}}$ | This output is a digital TTL waveform used to develop the VIDEO and composite VIDEO signals to the monitor. The polarity of this signal is: HIGH = BLACK<br>LOW = WHITE |
| 8 | INTOUT | O | Intensity Output | This pin is the intensity level modification attribute bit (synchronized with the video data output). |
| 9 | $\overline{\text{DWR}}$ | O | $\overline{\text{Display Write}}$ | Write strobe to display memory |
| 17-10 | DD7-0 | I/O | Display Data | 8-bit bidirectional data bus to display memory |
| 18 | HSYNC | O | Horizontal Sync | Horizontal sync signal to monitor |
| 19 | VSYNC | O | Vertical Sync | Vertical sync signal to monitor |
| 20 | CSYNC | O | Composite Sync | This output is used to generate an RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor. |
| 21 | $V_{cc}$ | | Power | 5.0 V power connection |
| | | | **CRT 9053** | |
| 22 | $\overline{\text{WR}}$ | I | $\overline{\text{Write Strobe}}$ | Causes data on the microprocessor data bus to be strobed into the EVTLC |
| 23 | $\overline{\text{RD}}$ | I | $\overline{\text{Read Strobe}}$ | Causes data from the EVTLC to be strobed onto the microprocessor data bus |
| | | | **CRT9153** | |
| 22 | R/$\overline{\text{W}}$ | I | Read/$\overline{\text{Write}}$ Select | Determines whether the processor is reading data from or writing data into the EVTLC (high for read, low for write) |
| 23 | $\overline{\text{DS}}$ | I | $\overline{\text{Data Strobe}}$ | Causes data to be strobed into or out of the EVTLC from the microprocessor data bus depending on the state of the R/W signal |
| 24 | A/$\overline{\text{D}}$ | I | Register Select | The state of this input pin will determine whether the data is being read from, or written to, the address or status register, or a data register. |
| 32-25 | DB7-0 | I/O | Processor Data Bus | 8-bit bi-directional processor data bus |

## THE EVTLC INTERNAL REGISTERS

### CRT 9053

Addressing of the internal EVTLC data registers of the CRT 9053 is accomplished through the use of the A/$\overline{D}$ select input qualified by the $\overline{RD}$ and $\overline{WR}$ strobes.

| A/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | REGISTER OPERATION |
|---|---|---|---|
| 0 | 1 | 0 | WRITE TO DATA REGISTER |
| 0 | 0 | 1 | READ DATA REGISTER |
| 1 | 1 | 0 | WRITE TO ADDRESS REGISTER |
| 1 | 0 | 1 | READ STATUS REGISTER |

### CRT9153

Addressing of the internal EVTLC data registers of the CRT 9153 is accomplished through use of the A/$\overline{D}$ and R/$\overline{W}$ select inputs qualified by the $\overline{DS}$ strobe.

| A/$\overline{D}$ | $\overline{DS}$ | R/$\overline{W}$ | REGISTER OPERATION |
|---|---|---|---|
| 0 | 0 | 0 | WRITE TO DATA REGISTER |
| 0 | 0 | 1 | READ DATA REGISTER |
| 1 | 0 | 0 | WRITE TO ADDRESS REGISTER |
| 1 | 0 | 1 | READ STATUS REGISTER |

The contents of the eight processor programmable registers located in the upper left hand side of the Functional Block Diagram of figure 1 indicate the memory locations from which screen data is to be fetched and displayed as well as the selected modes of display operation. These registers are addressed indirectly via the Address Register.

To access one of the eight eight-bit registers, the processor must first load the Address Register with the three-bit address of the selected data register. The next read or write to a data register will then cause the data register pointed to by the Address Register to be accessed. The Line A/$\overline{D}$ controls whether writing is occurring to the Address Register or to a data register. When a read operation is performed, A/$\overline{D}$ controls access to either the Status Register or to the data register selected by the Address Register.

## REGISTER DESCRIPTION

### ADDRESS REGISTER

Writing a byte to the ADDRESS register will select the specified register for the next time the processor writes to or reads the EVTLC data registers. The data register addresses are as follows:

| ADDRESS | | | | | | | | TYPE | REGISTER |
|---|---|---|---|---|---|---|---|---|---|
| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| X | X | X | X | 0 | 1 | 1 | 0 | Write | CHIP RESET |
| X | X | X | X | 1 | 0 | 0 | 0 | Write | TOSADD |
| X | X | X | X | 1 | 0 | 0 | 1 | Write | CURLO |
| X | X | X | X | 1 | 0 | 1 | 0 | Write | CURHI |
| X | X | X | X | 1 | 0 | 1 | 1 | Write | FILADD |
| X | X | X | X | 1 | 1 | 0 | 0 | Write | ATTDAT |
| X | X | X | X | 1 | 1 | 0 | 1 | RD/WR | CHARACTER |
| X | X | X | X | 1 | 1 | 1 | 0 | Write | MODE1 REGISTER |
| X | X | X | X | 1 | 1 | 1 | 1 | Write | MODE2 REGISTER |

(X = don't care) NOTE: Chip Reset is required before starting operation.

### STATUS REGISTER

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register. This bit is used to synchronize data transfers between the processor and the EVTLC. The EVTLC will set the DONE bit to a logic one after completing a byte transfer command or a FILL operation. The DONE bit is set to a logic zero by reading from, or writing to, the CHARACTER register. The processor must wait until the DONE bit is 1 before attempting to change the CURSOR ADDRESS, in order to write a character to, or read a character from, the CHARACTER register.

STATUS REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| DONE | X | X | X | X | X | X | X |

DONE = 1 signifies that external processor is allowed to access CURSOR ADDRESS and/or CHARACTER registers.

DONE = 0 signifies that external processor must wait until EVTLC completes transfer of data between display memory and CHARACTER register.

### DATA REGISTERS

FILADD (Fill Address) This register contains the RAM address of the character following the last address to be filled. Writing to this register will enable the EVTLC "fill" circuitry. The FILL operation will then be triggered by the next processor write to the CHARACTER register. The FILL operation will write the character in the CHARACTER register to every location in display memory starting with the address specified in the CURLO and CURHI registers through the location preceding the address specified in the FILADD register. The cursor position is not changed after a FILL operation. Note that the address bits DA3-DA0 are internally forced to 0 forcing the FILADD address to be 00, 16, 32, etc. to 1920. The CURLO and CURHI registers will not be changed by this operation. Writing to the CHARACTER register will cause the EVTLC to reset DB7 of the STATUS register to "0". Bit 7 will be set to 1 after the EVTLC has filled the last memory location specified.

FILADD REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| X | DA10 | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 |

TOSADD (Top of Screen Address) This register contains the RAM address of the first character displayed at the top of the video monitor screen. In addition, this register controls selection of either of two mask programmable vertical scan rates.

TOSADD REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| TIM | DA10 | DA9 | DA8 | DA7 | DA6 | DA5 | DA4 |

Note that address bits DA3-DAO are internally forced to 0 forcing the first address at the beginning of each row to be 00, 16, 32, etc. to 1920.

The most significant bit of this register (TIM) is used to select between the two mask programmed sets of vertical retrace parameters (scan A and scan B). This allows software selection of, for example, 50/60 HZ.

TIM = 0 enable raster scan A (60 Hz)

TIM = 1 enable raster scan B (50 Hz)

CURLO (Cursor Low) This register contains the eight lower order address bits of the RAM cursor address. All FILL screen and character transfer operations begin at the memory location pointed to by this address.

CURLO REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| DA7 | DA6 | DA5 | DA4 | DA3 | DA2 | DA1 | DA0 |

CURHI (Cursor High) This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8). All FILL screen and character transfer operations begin at the memory location pointed to by this address. In addition, this register contains the Smooth Scroll Offset Values SS3-SS0 which determine the number of scan lines that the data is shifted on the screen. The MSB of this register (SLE-status line enable) is the enable for the non-scrolling status line.

CURHI REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| SLE | SS3 | SS2 | SS1 | SS0 | DA10 | DA9 | DA8 |

SLE = 1 enables non-scrolling 25th status line
SLE = Ø disables and blanks non-scrolling status line

SS3-SS0 Smooth Scroll Offset Value

ATTDAT (Screen Attribute Data) Two attribute modes are provided. In the "tag bit" attribute mode, the MSB of each character is used to "tag" those characters which are to be enhanced with the attribute specified by the ATTDAT register. This allows individual characters to be attributed, but with the limitation that only one attribute style may be enabled for a specific screen. This is compatible with the CRT9028/9128, and is specified as the 9x28 operation mode. In the "embedded attribute" mode, multiple attributes may be displayed on one screen. This is specified as the 9x53 operation mode. See "MODE 2" register for selection of 9x28 and 9x53 modes.

The ATTDAT register specifies the visual attributes of the video data, in 9x28 operation mode, and the cursor presentation. The visual attributes specified in the ATTDAT register (DB3-DB0) are enabled or disabled by a TAG bit that is appended to the ASCII character written to the CHARACTER register. Every character on the screen with its TAG bit set is displayed with the same attribute. Changing the Attribute register will change the attribute of every "tagged" character on the screen. Character attributes in the 9x53 mode are determined by specific attribute characters embedded in the character data stream as explained below in the section titled CHARACTER SETS. The functions of the remaining bits in the ATTDAT register are not affected by the display character's TAG bit. NOTE: All 8 bits are valid for the 9x28 mode. In the 9x53 mode the only bits that are recognized are DB6, 5 and 4.

ATTDAT REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|

DB7 (1) MODE SELECT
DB7 = 1 enables graphics mode display (No attributes allowed)
DB7 = 0 enables alpha mode display
Note: See CHARACTER SETS for definition of characters available in each mode.

DB6 CURSOR SUPPRESS
DB6 = 1 inhibits VIDEO display at cursor time by forcing the VIDEO output to background level during cursor display time
DB6 = 0 enables VIDEO display at cursor time
Note: A blinking cursor display can be achieved by toggling this bit under processor control.

DB5 CURSOR DISPLAY
DB5 = 1 enables underline cursor display
DB5 = 0 enables block cursor display
Note: An underline cursor in an underline character attribute field will be dashed.

DB4 SCREEN
DB4 = 1 for white screen and black characters
DB4 = 0 for black screen and white characters
Note: This is a screen attribute (versus character attribute) bit and sets the default video background level.

ENABLED OR DISABLED BY TAG BIT (9x28 MODE ONLY)

DB3[1] CHARACTER SUPPRESS
- DB3 = 1 to enable Video suppress
- DB3 = 0 to inhibit Video suppress

Note: This bit allows character blinking and blanking under processor control

DB2[1] INTENSITY
- DB2 = 1 allows the INTOUT output pin to go high for the character time
- DB2 = 0 inhibits the INTOUT output pin from going high

DB1[1] UNDERLINE
- DB1 = 1 will cause the character to be underlined
- DB1 = 0 will inhibit the underline

DB0[1] REVERSE VIDEO
- DB0 = 1 will cause the standard foreground and background Video levels (selected with BIT 4) to be reversed for the character time
- DB0 = 0 will inhibit reverse video

[1] These bits not recognized in 9x53 mode and represent don't care states.

MODE 1 The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the EVTLC after every read/write of the CHARACTER register. Note: The visible cursor position is not affected.

MODE 1 REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| AUTO INC | X | X | X | X | X | X | X |

DB7 AUTO INCREMENT
- DB7 = 1 to enable automatic character address

The RAM address is incremented after the EVTLC completes a display memory access initiated by a processor to RAM or RAM to processor character transfer.

- DB7 = 0 to disable automatic increment.

MODE 2 This register contains two bits which control operational modes of the device. DB0 controls whether the device operates as a 9x53 or emulates the 9x28. In the 9x28 mode the device is fully compatible with the CRT 9028/9128 with the exception of the higher density character set. DB1 enables the cursor blink function where the blink rate is a mask programmable feature (see CRT 9053/9153 coding sheet.) This function is automatically disabled when in 9x28 mode.

MODE 2 REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | CUR BLINK | 9x53 ENBL |

DB1 CURSOR BLINK
- DB1 = 1 will enable blinking cursor.
- DB1 = 0 will disable blinking cursor and state of cursor is controlled by DB6 in ATTDAT register.

DB0 9x53 ENABLE
- DB0 = 1 will enable operation as a 9053/9153.
- DB = 0 will enable operation as 9028/9128.

CHARACTER This register allows access to the display memory for both byte transfers and FILL operations. In BYTE Transfer Write Mode, the processor first writes a character to this register. The EVTLC takes that character and stores it in the display memory in the location specified by the CURLO and CURHI registers. In Byte Transfer Read Mode, the processor reads this register causing the EVTLC to fetch the character whose address is specified in the CURLO and CURHI registers from the display memory and place it in the CHARACTER register. The processor then reads the character and initiates another fetch from memory cycle. In FILL mode, writing a byte to this register will initiate a FILL operation. All EVTLC/memory data transfers take place during horizontal and vertical video retrace blank time.

CHARACTER REGISTER

| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|
| 8 BIT CHARACTER[2] | | | | | | | |

[2] See next section, CHARACTER SETS, for definition of 8 bit characters.

## CHARACTER SETS

The character set consists of 128 characters, a six segment "wide graphics" and a four segment "thin graphics" entity. Included in the 128 mask programmable characters can be the 96 standard ASCII characters and 32 special characters.

### 9x28 OPERATION MODE (MODE 2: DB0 = 0)

A. GRAPHICS MODE - (ATTDAT: DB7 = 1)

This mode allows an intermix of alphanumeric and graphics characters. No attributes are permitted in this mode. If DB7 = 1, the character will be alphanumeric. If DB7 = 0, the character will be a graphics character. DB7 is "tag bit".

| ENTITY | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CHARACTER | 1 | ← CHARACTER DATA → | | | | | | |
| THIN[1] GRAPHICS | 0 | 0 | X | X | SEG4 | SEG3 | SEG2 | SEG1 |
| WIDE[1] GRAPHICS | 0 | 1 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |

B. ALPHANUMERICS MODE-(ATTDAT: DB7 = 0)

This mode allows display of alphanumeric characters with attributes. If DB7 is set to a logical one, the attribute(s) specified in the ATTDAT register will be enabled for that character. If DB7 is cleared, attributes will not be enabled for that character. DB7 is "tag bit".

| ENTITY | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CHARACTER (Attr enabled) | 1 | ← CHARACTER DATA → | | | | | | |
| CHARACTER (No attribute) | 0 | ← CHARACTER DATA → | | | | | | |

### 9x53 OPERATION MODE (MODE 2: DB0 = 1)

This mode allows the use of embedded field attributes where the desired attribute for any given string of one or more consecutive characters is defined by an attribute character which is part of the character data stream and is located immediately in front of the characters to be attributed. A second attribute character should be located immediately following the string of attributed characters to restore the normal display mode. Since the specific attribute characters occupy character positions, they are actually displayed as spaces.

| ENTITY | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CHARACTER | 0 | ← CHARACTER DATA → | | | | | | |
| ATTRIBUTE[2] CHARACTER | 1 | 0 | 0 | BLANK | BLINK | INT | UNDLN | RV |
| THIN[1] GRAPHICS | 1 | 0 | 1 | X | SEG4 | SEG3 | SEG2 | SEG1 |
| WIDE[1] GRAPHICS | 1 | 1 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 |

[1] Graphics segments are turned on when bit is set to a "1".

[2] A specific field attribute is enabled by setting the appropriate bit and disabled by resetting the bit. Attributes can be mixed. The following defines the available attributes indicated in the ATTRIBUTE CHARACTER.

DB4 (BLANK)–Suppresses character video output.
DB3 (BLINK)–Causes character to blink at mask programmed rate.
DB2 (INTENSITY)–Controls INTOUT output pin.
DB1 (UNDERLINE)–Causes character to be underlined.
DB0 (REVERSE VIDEO)–Reverses foreground/background video levels.

### GRAPHICS CHARACTERS[3]

| | |
|---|---|
| SEGMENT 6 | SEGMENT 3 |
| SEGMENT 5 | SEGMENT 2 |
| SEGMENT 4 | SEGMENT 1 |

WIDE GRAPHICS ENTITY

| | |
|---|---|
| | SEGMENT 3 |
| SEGMENT 4 | SEGMENT 2<br>SEGMENT 1 |

THIN GRAPHICS ENTITY

[3] Scan line and column of segment locations are mask programmable.

## DESCRIPTION OF SYSTEM OPERATION

The EVTLC circuitry provides two control functions. One function interprets and controls data from the system processor interface through the data bus DB7-DB0 as shown in the Processor Timing of figure 3. The other function generates and refreshes the video image on the screen through the DD7-DD0 data bus as shown in the Display Memory Timing of figure 2. Because the system data bus is isolated from the display data bus, the EVTLC maintains complete control over access to display memory. All data flow between display RAM and the processor or the EVTLC takes place through the EVTLC. Refer to the EVTLC Display Memory Access Timing of figure 7.

### DISPLAY MEMORY ACCESS

Processor/display memory access is accomplished through the CHARACTER register of the EVTLC. All processor transfers to or from the CHARACTER register take place only when the DONE bit is high. The DONE bit is used to synchronize data transfers between the EVTLC and the processor as shown in the Typical Processor To Display Memory Transfer of figure 6. When the processor needs to store a byte of data in the display memory, it will write the byte to the CHARACTER register of the EVTLC. The EVTLC will immediately reset the DONE bit indicating that the transfer hardware is busy. At the next blanked Video time, the EVTLC will store the byte in the display memory, increment the character address, (if auto increment is enabled) and set the DONE bit. When the processor needs to read a byte of data from the display memory, it will read the CHARACTER register. The EVTLC will fetch the desired byte from the display memory during the next blanked VIDEO time, increment the character address (if enabled), and set the DONE bit. When the processor detects that the DONE bit is set, it will read the CHARACTER register to get the data byte from the EVTLC. This read will reset the DONE bit and

cause the EVTLC to fetch the next byte of data from the memory.

If auto increment is not enabled, the processor must set the cursor address in the CURLO and CURHI register to the address of the memory location being read from, or written into, before every access to the CHARACTER register.

It should be noted that Auto Increment does not affect the visible cursor location. If auto-increment is enabled, the current character location will equal the cursor position only for the first character transfered following an update of the CURLO and CURHI registers. Note that the DONE bit must be high before attempting to update the cursor registers because the loading of the cursor registers will reset the character position counters to the cursor position.

## SMOOTH SCROLL

The EVTLC may be programmed to do either "jump" or "smooth" scrolling. Jump scrolling moves the data up or down the monitor screen one data row at a time. Smooth scrolling moves the data up the monitor screen one scan line at a time. The number of scan lines and the rate they move up the screen is under processor control.

Smooth scroll is controlled through manipulation of the SS3-SS0 bits of the CURHI register. These bits represent the binary address of the first scan line of the first data row displayed on the monitor screen (the data row whose beginning address is in the TOSADD register). When the value represented by these bits is incremented, the video data on the monitor screen moves up by the same number of scan lines. After the address of the last scan line of the data row is loaded into the CURHI register and the VIDEO data has moved up the last scan line of the data row, the processor resets the SS3-SS0 address to point to scan line 0 and does a jump scroll. Jump scroll is accomplished by incrementing the RAM address in the TOSADD register by a data row length (so that it points to the address of the first character of the new top data row on the monitor).

When programmed for a data row of 80 characters/data row display (1920 data words), for example, the display RAM contains 25 actual rows of data (2000 RAM locations). If the smooth scroll offset equals zero, the EVTLC will display the 1919 RAM locations following the top of screen address when displaying data. The first data row is partially scrolled off the screen and the 25th data row is scrolled onto the screen when the smooth scroll offset is incremented. The EVTLC will now display the 1999 RAM locations following the top of screen address (wrapping to 0 after address 1999). After the EVTLC does a jump scroll, the processor will program it to erase the line just scrolled off the screen (preparing it to be scrolled onto the screen). This line now becomes the non-displayed 25th data row.

## NON-SCROLLING STATUS LINE

The non-scrolling status line is only functional on a EVTLC that has been programmed for 25 data rows. This data row will remain stationary at the bottom of the screen and will not move up the screen when the remainder of the display data is scrolled. Otherwise, VIDEO data on the status line may be manipulated as though it were normal display data. The smooth scroll offset will not function properly when the status line is enabled. The memory address of the characters on the status line are always characters 1920–1999.
NOTE: If the part is programmed for 25 data rows an additional mask option must be specified which makes the 25th data row either fixed (always displayed) or a status row (enabled/disabled by the SLE bit).

## CHIP RESET

The CRT 9053 and CRT 9153 Chip Reset requires two steps. The system processor first writes the reset address to the address register of the EVTLC. The system processor then writes a dummy character to the EVTLC Data register. Writing to the Data register resets the chip. See the DONE timing in figure 6. This reset process causes the MODE 2 register to be set to the "00" state which disables the blinking cursor and enables the 9x28 operation mode.

**ROM CHARACTER BLOCK FORMAT**

| COLUMN DOT -> | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|---|---|
| SCAN LINE 0 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 1 -> | 0 | | | | | | | | 0 |
| SCAN LINE 2 -> | 0 | | | | | | | | 0 |
| SCAN LINE 3 -> | 0 | | | | | | | | 0 |
| SCAN LINE 4 -> | 0 | | | | | | | | 0 |
| SCAN LINE 5 -> | 0 | | | | | | | | 0 |
| SCAN LINE 6 -> | 0 | | | MASK PROGRAMMABLE CHARACTER BLOCK (FONT) 7 X 11 | | | | | 0 |
| SCAN LINE 7 -> | 0 | | | | | | | | 0 |
| SCAN LINE 8 -> | 0 | | | | | | | | 0 |
| SCAN LINE 9 -> | 0 | | | | | | | | 0 |
| SCAN LINE 10 -> | 0 | | | | | | | | 0 |
| SCAN LINE 11 -> | 0 | | | | | | | | 0 |
| SCAN LINE 12 -> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Mask programmable options–The ROM character block format above shows the 7X11 mask programmable character font within the character cell as defined by dots C8 through C0 and scan lines 0 through 12.

Dots/Character: 8 dots/character cell => C8 - C1 displayed
9 dots/character cell => C8 - C0 displayed

Column dot C0 will be the same as column dot C8 when more than 8 dots/character cell are specified when generating alpha-numerics.

NOTE: The maximum dot clock crystal frequency is dependent on the dots/character programmed:

| DOTS/CHARACTER | MAX XTAL FREQ |
|---|---|
| 8 dots | 16.62 MHz max* |
| 9 dots | 18.7 MHz max* |

*These values are preliminary

Scan Lines per Character:
11 scan lines/character => SL0-SL10 displayed
12 scan lines/character => SL0-SL11 displayed
13 scan lines/character => SL0-SL12 displayed

Thin and Wide Graphics: Dots mask programmed for vertical column C1 will be the same as backfill Columns 0 when generating wide and thin graphics.

SECTION V

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** (TA = 0°C to 70°C, $V_{cc}$ = +5V ±5%, unless otherwise noted.)

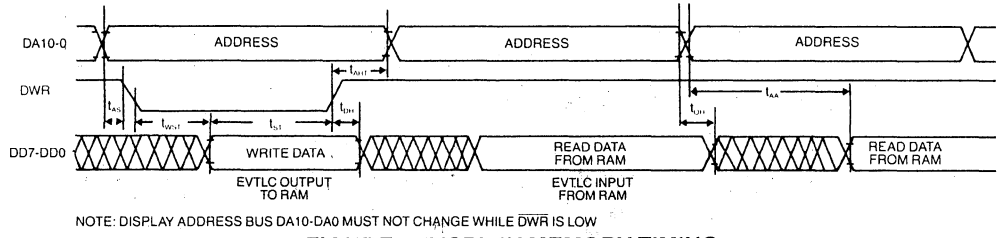
| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low-level, Vil | | | 0.8 | V | |
| High-Level, Vih | 2.2 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low-level, Vol | | | 0.4 | V | All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, $\overline{VSYNC}$; Iol = 1.6 mA |
| Low-level, Vol | | | 0.4 | V | $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Iol = 0.4 mA |
| High-level, Voh | 2.4 | | | V | All outputs except $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −40μa |
| High-level, Voh | 2.4 | | | V | $\overline{VIDEO}$, CSYNC, INTOUT, HSYNC, VSYNC; Ioh = −20μA |
| INPUT LEAKAGE CURRENT | | | | | |
| High-level, Ilh | | | 10 | μA | All inputs; Vin = Vcc |
| Low-level, Ill | | | −10 | μA | All inputs except $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V |
| Low-level, Ill | | | −200 | μA | $\overline{WR}$, $\overline{RD}$, $\overline{DS}$, R/$\overline{W}$; Vin = 0.4V |
| INPUT CAPACITANCE | | | | | |
| All inputs, Cin | | | 15 | pF | |
| OUTPUT LOAD | | | | | |
| $C_L$ | | | 15 | pF | Except DB7-0 |
| $C_L$ | | | 100 | pF | DB7-0 |
| POWER SUPPLY CURRENT | | | | | |
| Icc | | 125 | | mA | |
| **AC CHARACTERISTICS** | | | | | |
| CLOCK FREQUENCY, fin | 1.0 | | 18.7 | MHz | |
| DISPLAY MEMORY TIMING | | | | | |
| Address Set-up Time | | | | | |
| $t_{AS}$ | 20 | | | ns | |
| Write Strobe Set-up Time | | | | | |
| $t_{WST}$ | 100 | | | ns | |
| Data Set-up Time | | | | | |
| $t_{ST}$ | 80 | | | ns | |
| Data Hold Time | | | | | |
| $t_{DH}$ | 10 | | 50 | ns | |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| Address Hold Time $t_{AHT}$ | 50 | | | ns | |
| Output Hold From Address Change $t_{OH}$ | 15 | | | ns | |
| Address Access Time $t_{AA}$ | | | 250 | ns | |
| PROCESSOR TIMING | | | | | |
| Address Read/Write Set-up $t_{ARWS}$ | 160 | | | ns | |
| Write Pulse Width $t_{WPW}$ | 160 | | | ns | |
| Write Hold Time $t_{WHT}$ | 15 | | | ns | |
| Read Set-up Time $t_{RST}$ | | | 200 | ns | |
| Read Data Valid $T_{RDV}$ | 0 | | | ns | |
| Read Pulse Width $t_{RPW}$ | 250 | | | ns | |
| Data Write Falling Set-up $t_{DWFS}$ | 120 | | | ns | |
| Data Write Rising Set-up $t_{DWRS}$ | 160 | | | ns | |

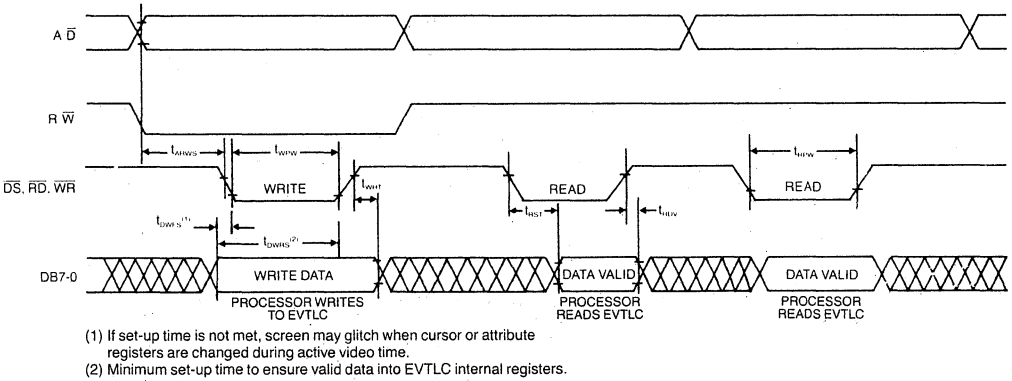
Crystal specification (Applies for 4-18.7 MHz):
- Series Resonant
- 50 ohms max series resistance
- 1.5 pf typ parallel capacitance
- Operation below 4 MHz requires external crystal oscillator





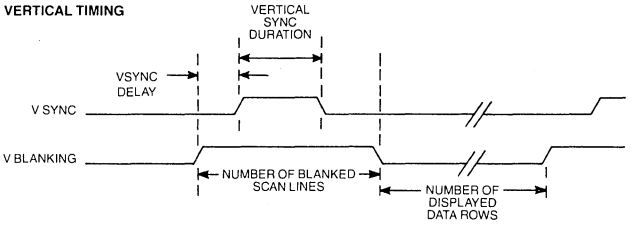

NOTE: DISPLAY ADDRESS BUS DA10-DA0 MUST NOT CHANGE WHILE $\overline{DWR}$ IS LOW

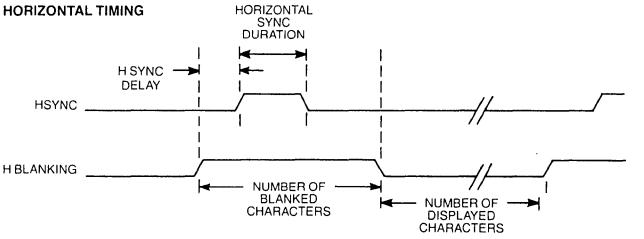
**FIGURE 2. DISPLAY MEMORY TIMING**




(1) If set-up time is not met, screen may glitch when cursor or attribute registers are changed during active video time.
(2) Minimum set-up time to ensure valid data into EVTLC internal registers.

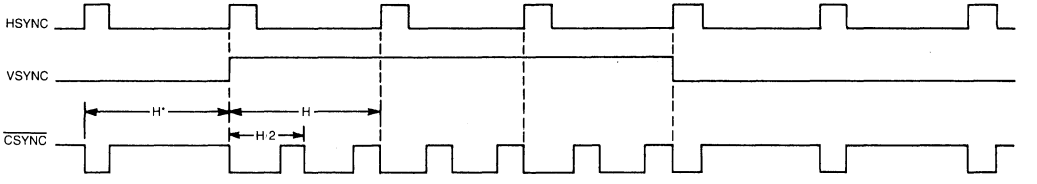
**FIGURE 3. PROCESSOR TIMING**



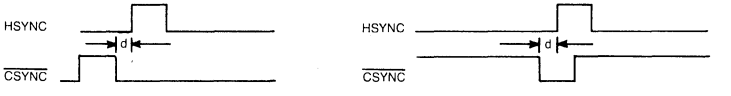




NOTE: Video parameters above are mask programmable

**FIGURE 4. VERTICAL AND HORIZONTAL SYNC TIMING**




NOTE: Delays between pulse edges and pulse width values may vary due to mask programmable features.
*H represents horizontal interval

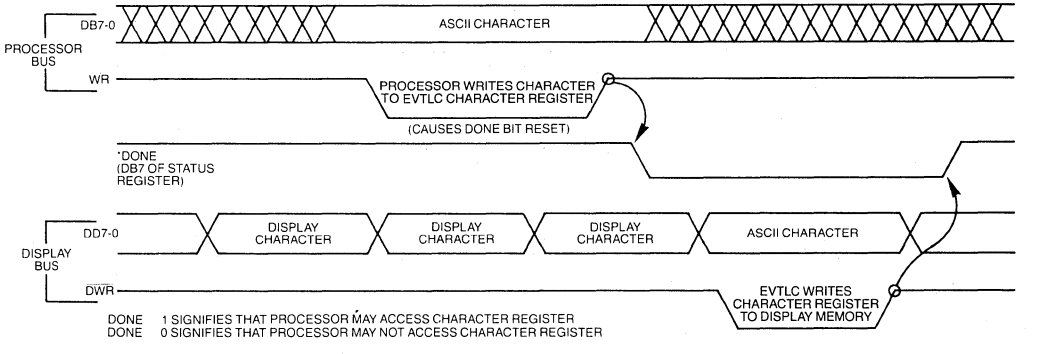



d HSYN Delay -CSYN Delay

**WITHIN VERTICAL SYNC PULSE TIME**

**OUTSIDE OF VERTICAL SYNC PULSE TIME**

**FIGURE 5. VIDEO SIGNAL TIMING**




DONE 1 SIGNIFIES THAT PROCESSOR MAY ACCESS CHARACTER REGISTER
DONE 0 SIGNIFIES THAT PROCESSOR MAY NOT ACCESS CHARACTER REGISTER

**FIGURE 6. TYPICAL PROCESSOR TO DISPLAY MEMORY TRANSFER**

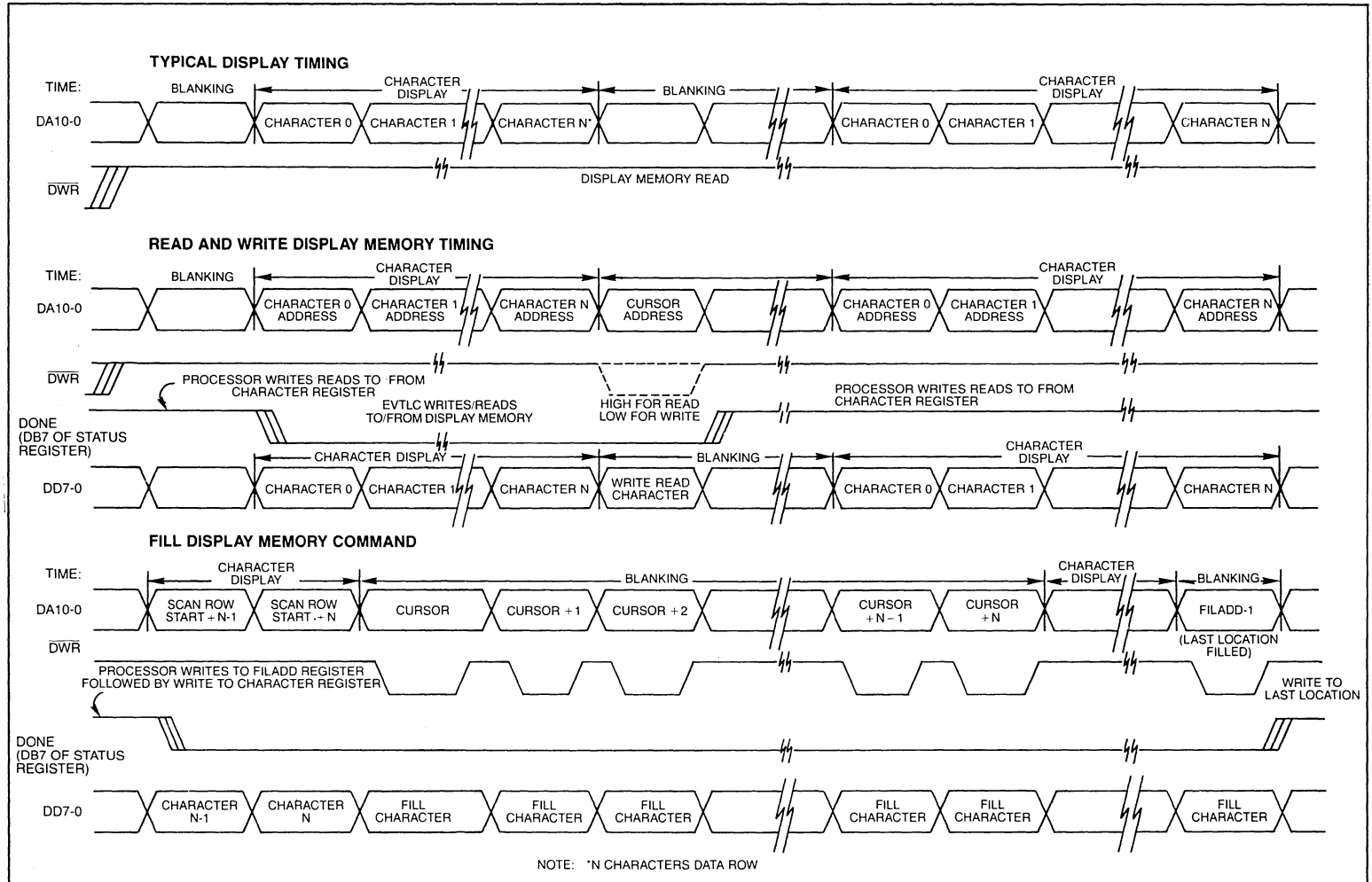



**FIGURE 7. EVTLC DISPLAY MEMORY ACCESS TIMING**

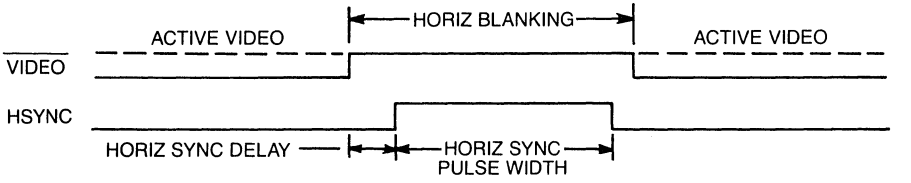
## I. ROM CHARACTER BLOCK FORMAT:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| COLUMN DOT | –> | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| SCAN LINE 0 | –> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SCAN LINE 1 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 2 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 3 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 4 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 5 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 6 | –> | 0 | | | CHARACTER BLOCK 7X11 CELL | | | | | 0 |
| SCAN LINE 7 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 8 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 9 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 10 | –> | 0 | | | | | | | | 0 |
| SCAN LINE 11 | –> | 0 | | | | | | | | 0 |

DOTS PER CHARACTER: 9
DOT CLOCK XTAL FREQUENCY (MHz): 17.1072

## II. HORIZONTAL TIMING (IN CHARACTER TIMES):

CHARACTERS PER DATA ROW: 80
HORIZONTAL BLANKING: 19
HORIZONTAL SYNC DELAY: 4
HORIZONTAL SYNC PULSE WIDTH: 8
HORIZONTAL SYNC POLARITY: NEGATIVE ACTIVE

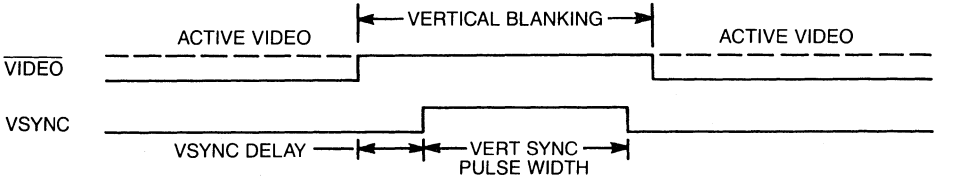



## III. VERTICAL TIMING:

CHARACTER ROWS: 25
SCAN LINES PER CHARACTER: x 12
TOTAL VISIBLE SCAN LINES: 300
VERTICAL SYNC POLARITY: NEGATIVE ACTIVE

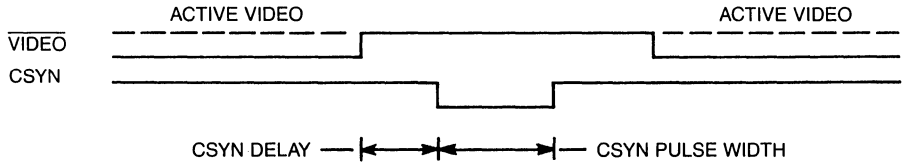
## IV. VERTICAL SYNC TIMING (IN SCAN LINES):

60 Hz VERTICAL BLANKING: 20
60 Hz VERTICAL SYNC DELAY: 4
60 Hz VERTICAL SYNC PULSE WIDTH: 8
ALTERNATE (50 Hz) VERTICAL BLANKING: 84
ALTERNATE (50 Hz) VERTICAL SYNC DELAY: 17
ALTERNATE (50 Hz) VERTICAL SYNC PULSE WIDTH: 34



## V. COMPOSITE SYNC OUTPUT (IN CHARACTER TIMES)

COMPOSITE SYNC DELAY: 2
COMPOSITE SYNC PULSE WIDTH: 8




## VI. BLINK RATES (@ 60 Hz VSYNC):

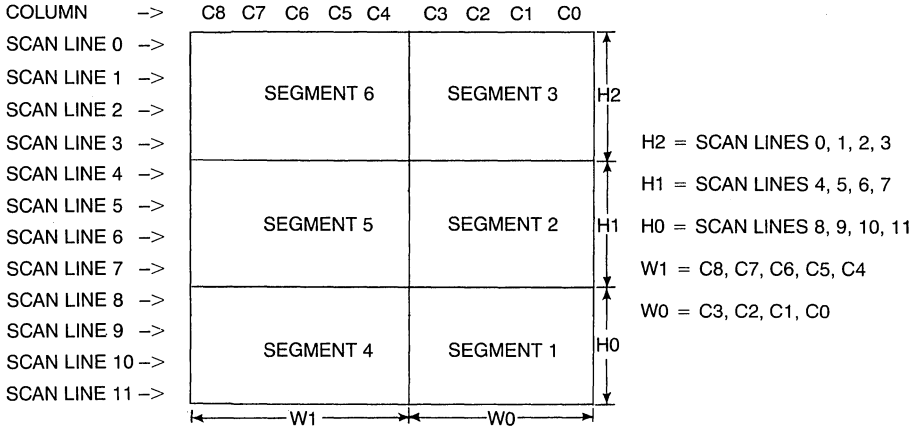
CHARACTER—
- BLINK RATE: 1.25 Hz
- DUTY CYCLE: 75/25

CURSOR—
- BLINK RATE: 2.5 Hz
- DUTY CYCLE: 50/50

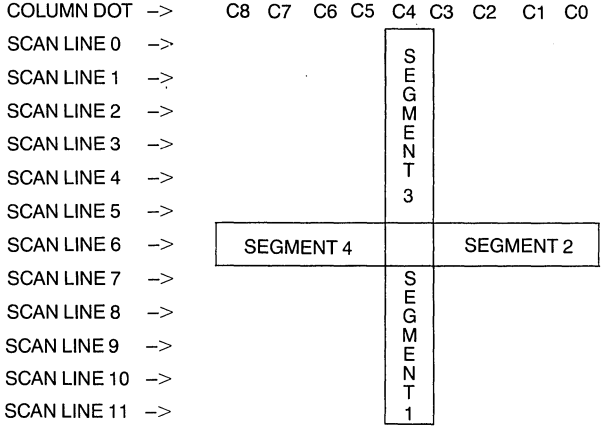
## VII. UNDERLINE ATTRIBUTE:

CHARACTER UNDERLINE: SCAN LINE 11
CURSOR UNDERLINE: SCAN LINE 11

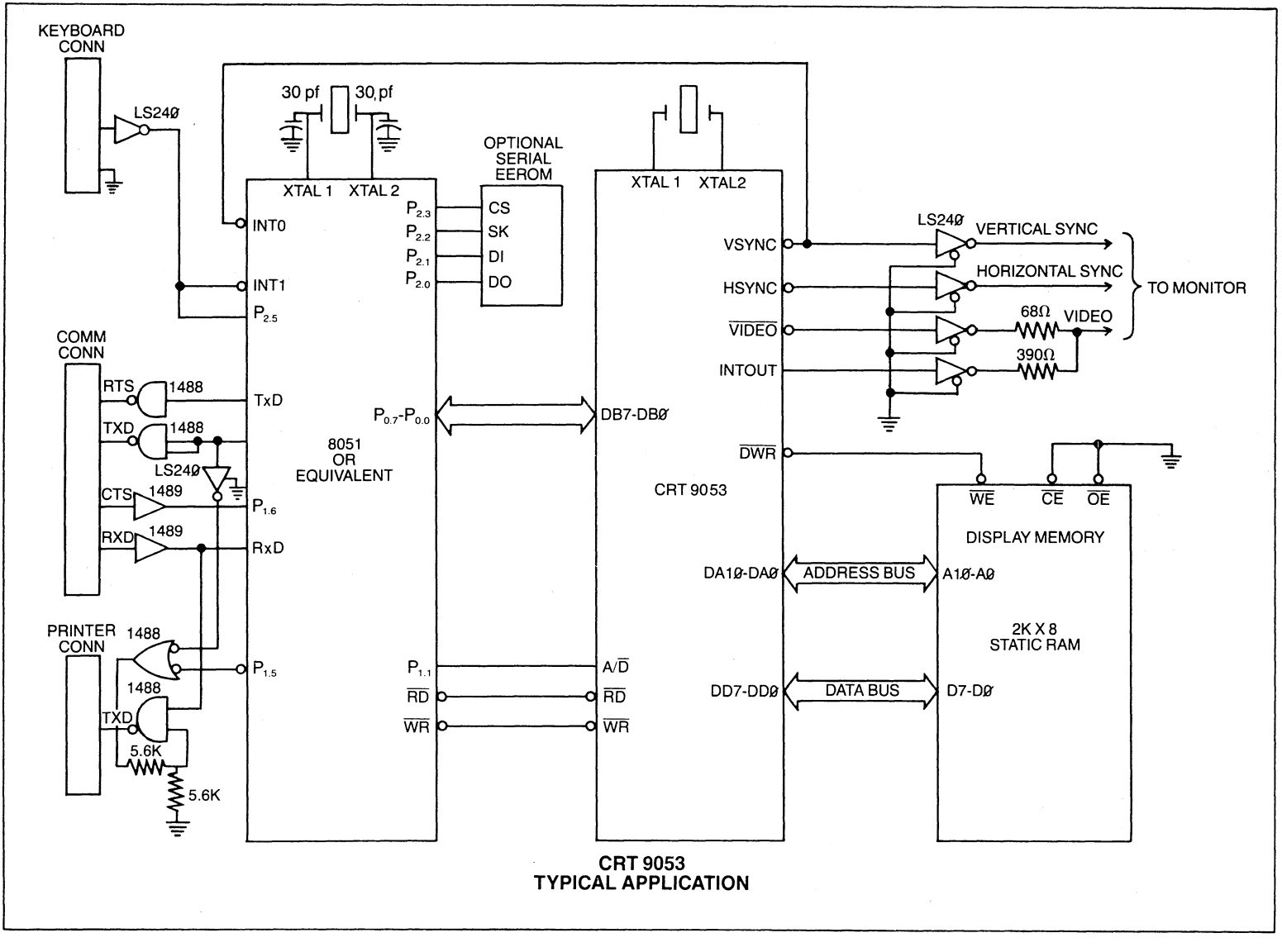
## VIII. WIDE GRAPHICS FIGURE DEFINITION:



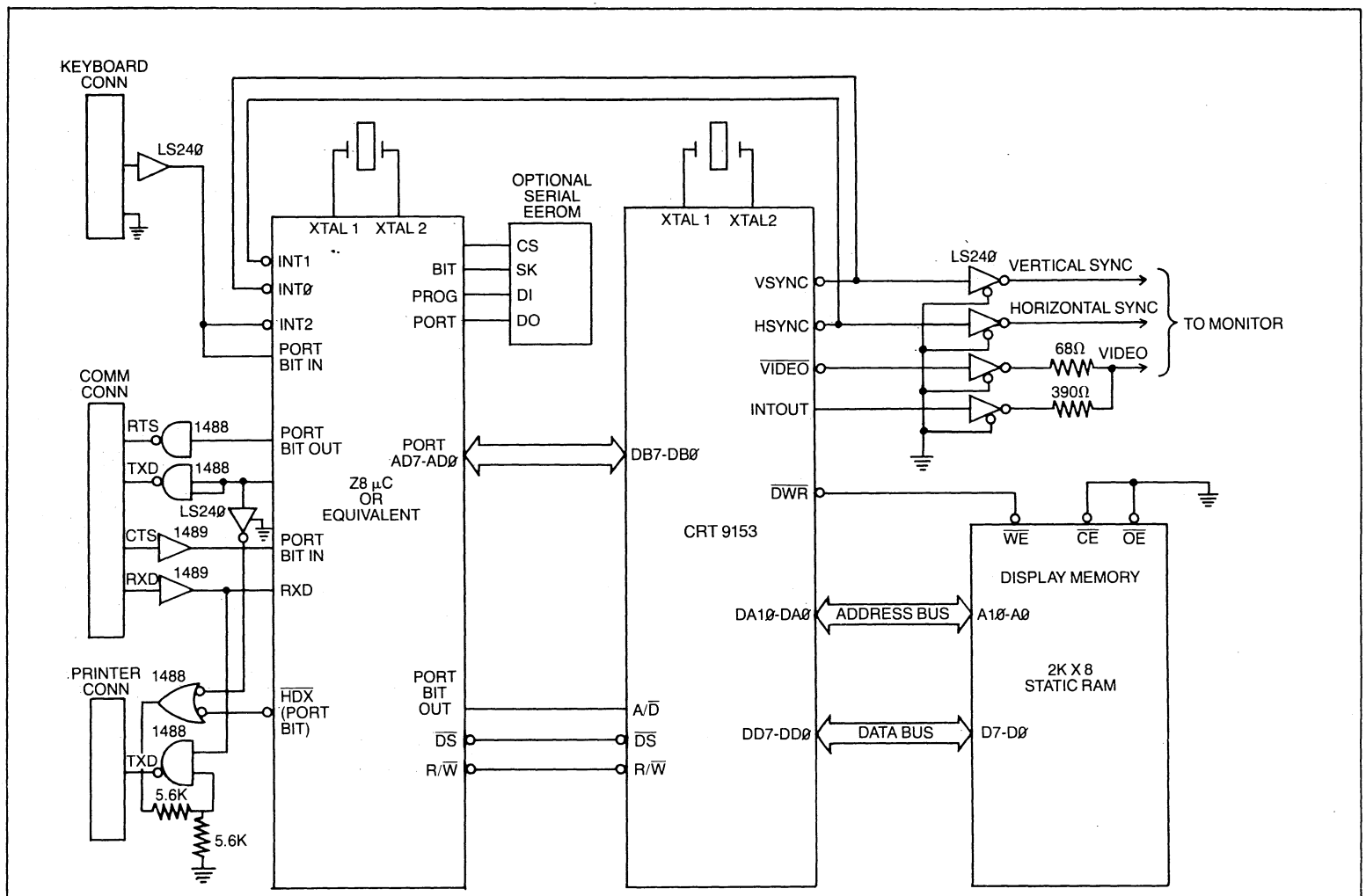

## IX. THIN GRAPHICS FIGURE DEFINITION:




SEGMENT 4 = SCAN LINE 6; C8, C7, C6, C5, C4
SEGMENT 3 = C4; SCAN LINES 0, 1, 2, 3, 4, 5, 6
SEGMENT 2 = SCAN LINE 6; C4, C3, C2, C1, C0
SEGMENT 1 = C4; SCAN LINES 6, 7, 8, 9, 10, 11




**CRT 9053**
**TYPICAL APPLICATION**




**CRT 9153**
**TYPICAL APPLICATION**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510 227-8898

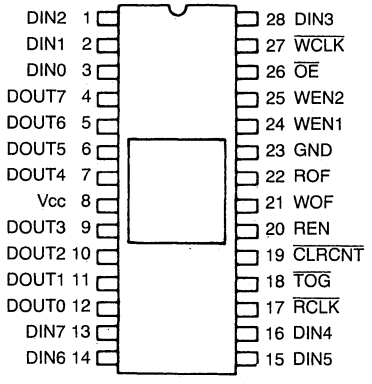
Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Double Row Buffer
# DRB

## FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

**PIN CONFIGURATION**




PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

SECTION V

## GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

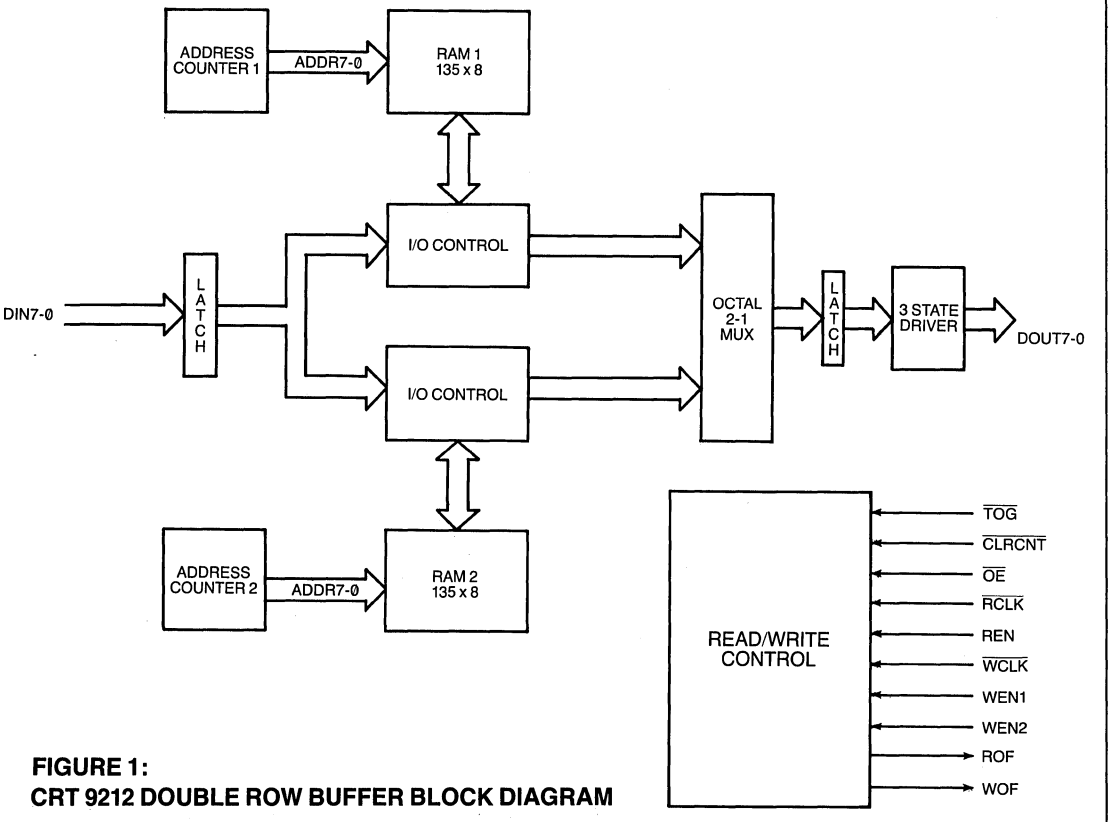



**FIGURE 1:**
**CRT 9212 DOUBLE ROW BUFFER BLOCK DIAGRAM**

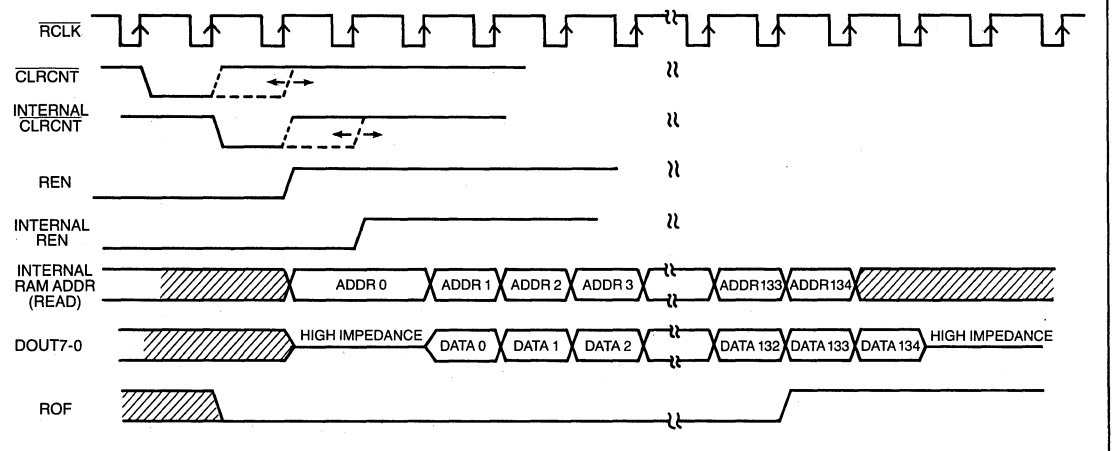



**FIGURE 2: CRT 9212 DOUBLE ROW BUFFER READ TIMING**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 3-0, 28, 16-13 | Data inputs | DIN0-DIN7 | DIN0-DIN7 are the data inputs from the system memory. |
| 12-9, 7-4 | Data outputs | DOUT0-DOUT7 | DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator. |
| 17 | $\overline{\text{Read Clock}}$ | $\overline{RCLK}$ | $\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge. |
| 18 | $\overline{\text{Toggle Signal}}$ | $\overline{TOG}$ | $\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and CLRCNT are low. |
| 19 | $\overline{\text{Clear Counter}}$ | $\overline{CLRCNT}$ | $\overline{\text{Clear Counter}}$ clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active. |
| 20 | Read Enable | REN | REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when $\overline{\text{Read Clock}}$ is active. |
| 21 | Write Overflow | WOF | WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4. |
| 22 | Read Overflow | ROF | The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4. |
| 24, 25 | Write Enable | WEN1, WEN 2 | WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open. |
| 26 | $\overline{\text{Output Enable}}$ | $\overline{OE}$ | When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open. |
| 27 | $\overline{\text{Write Clock}}$ | $\overline{WCLK}$ | $\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high. |
| 8 | Power Supply | $V_{CC}$ | +5 Volt supply |
| 23 | Ground | GND | Ground |



## OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the $\overline{\text{Toggle Signal}}$ ($\overline{TOG}$) will go low. When $\overline{\text{Clear Counter}}$ ($\overline{CLRCNT}$) goes low, the next $\overline{\text{Read Clock}}$ ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a $\overline{\text{Read Clock}}$ ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ± 5%)

| PARAMETER | MIN | TYP | MAX | UNITS | COMMENTS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{IL}$ | | | 0.8 | V | |
| High Level $V_{IH1}$ | 2.0 | | | V | excluding $\overline{RCLK}$; $\overline{WCLK}$ |
| High Level $V_{IH2}$ | 4.2 | | | V | $\overline{RCLK}$, $\overline{WCLK}$ |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | |
| High Level $V_{OH}$ | 2.4 | | | V | |
| INPUT LEAKAGE CURRENT | | | | | |
| High Leakage $I_{LH1}$ | | | 10 | µA | excluding $\overline{OE}$ |
| Low Leakage $I_{LL1}$ | | | 10 | µA | excluding WEN1 |
| High Leakage $I_{LH2}$ | | | 400 | µA | WEN1 |
| Low Leakage $I_{LL2}$ | | | 400 | µA | $\overline{OE}$ |
| INPUT CAPACITANCE | | | | | |
| $C_{IN1}$ | | 10 | | pF | excluding $\overline{RCLK}$, $\overline{WCLK}$ |
| $C_{IN2}$ | | 15 | | pF | $\overline{RCLK}$, $\overline{WCLK}$ |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | 100 | | mA | |

**AC CHARACTERISTICS**[1]

| | | | | | |
|---|---|---|---|---|---|
| $t_{CYW}$ | 300 | | | ns | Write clock period |
| $t_{CYR}$ | 300 | | | ns | Read clock period |
| $t_{CKH}$ | 247 | | DC | ns | |
| $t_{CKL}$ | 33 | | | ns | |
| $t_{CKR}$ | | | 10 | ns | measured from 10% to 90% points |
| $t_{CKF}$ | | | 10 | ns | measured from 90% to 10% points |
| $t_{DS}$ | 50 | | | ns | referenced to $\overline{WCLK}$ |
| $t_{DH}$ | 0 | | | ns | referenced to $\overline{WCLK}$ |
| $t_{EN1}$[2] | 0 | | | ns | |
| $t_{EN2}$[2] | 100 | | | ns | |
| $t_{ENH}$[2] | 0 | | | ns | |
| $t_{DV}$ | | | 175 | ns | $C_L$ = 50 pF; referenced from $\overline{RCLK}$ |
| $t_{DOFF}$ | | | 175 | ns | |
| $t_{DON}$ | | | 175 | ns | |
| $t_{OF}$[3] | | | 175 | ns | $C_L$ = 30 pF |
| $t_{CS}$ | 100 | | | ns | |
| $t_{CH}$ | 0 | | | ns | |
| $t_{WT}$[4] | | $1t_{CYW}$ | | | |

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

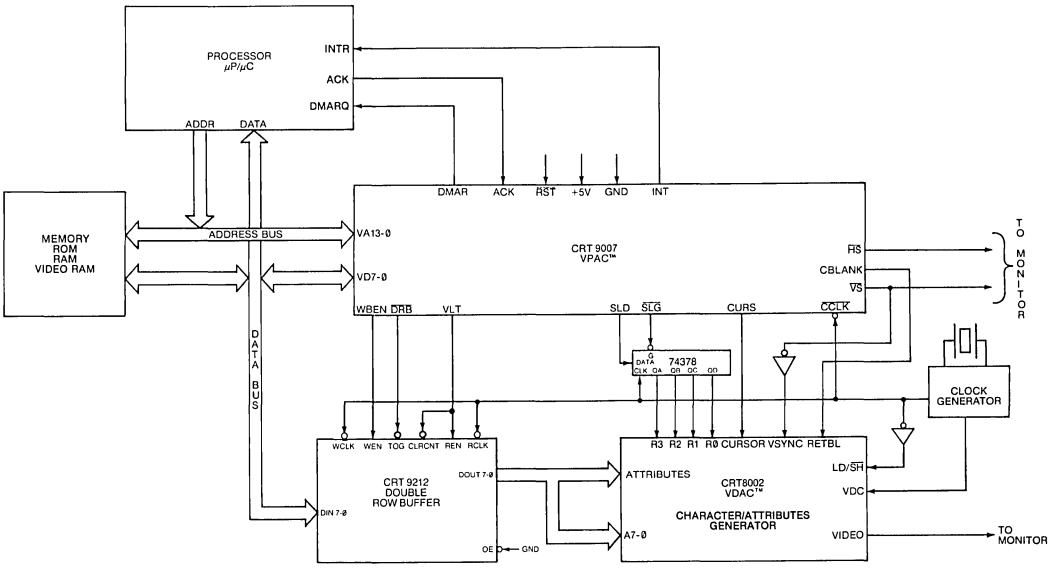



**FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™**

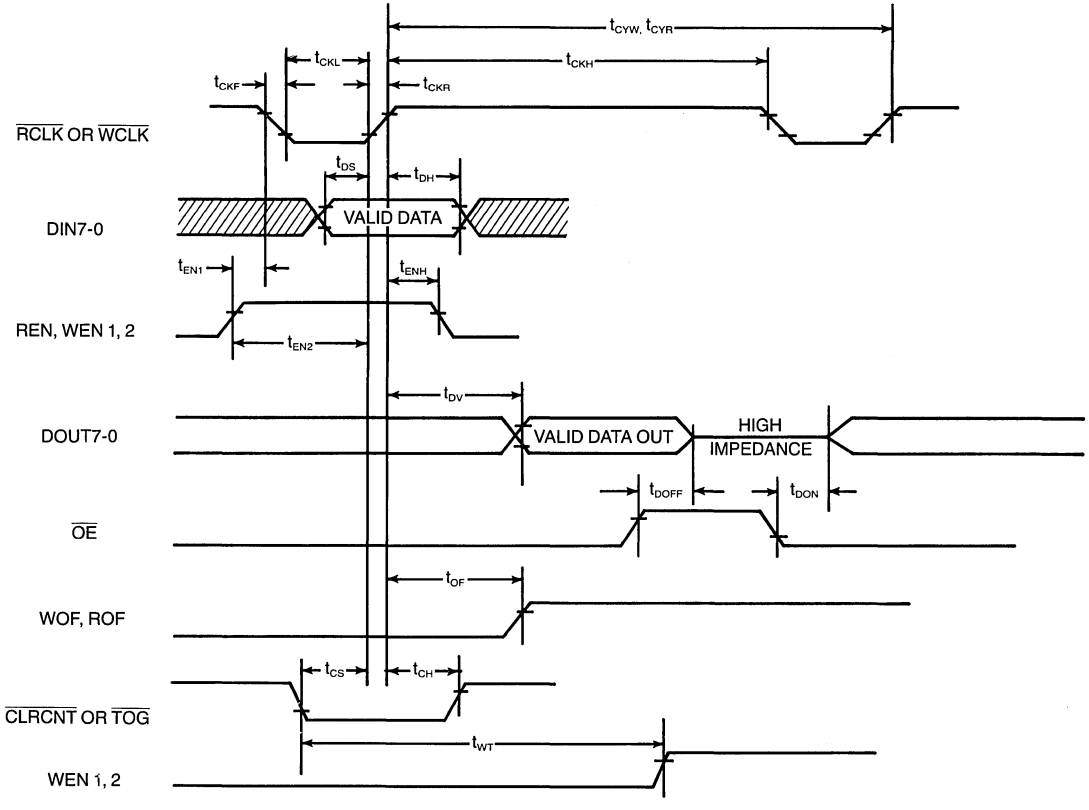
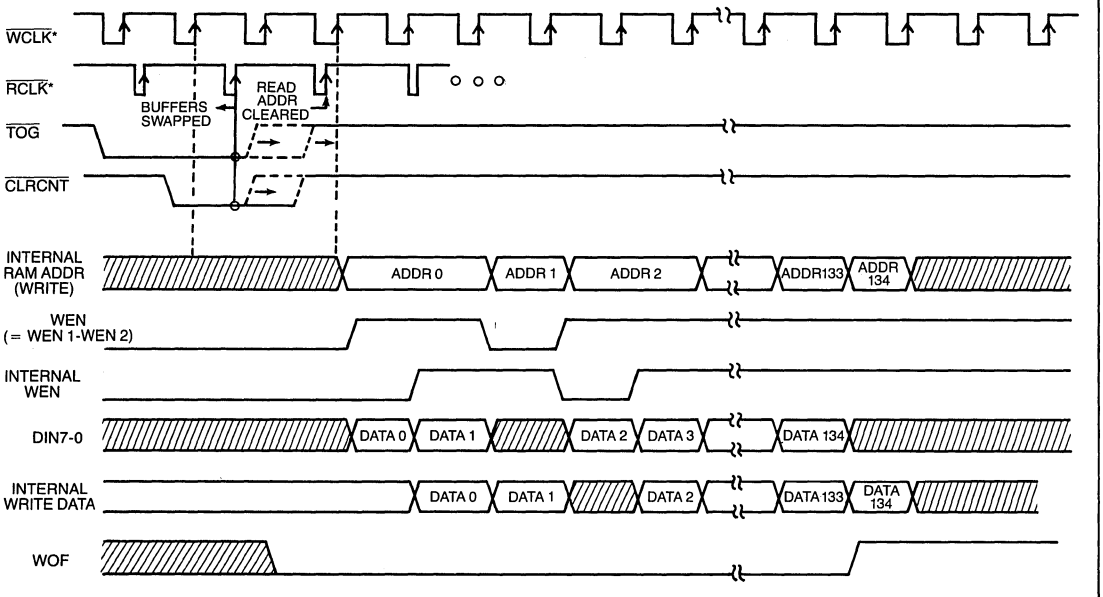



**FIGURE 6: CRT 9212 I/O TIMING**

SECTION V




* in general $\overline{WCLK}$ and $\overline{RCLK}$ can be different

**FIGURE 3: CRT 9212 DOUBLE ROW BUFFER WRITE TIMING**

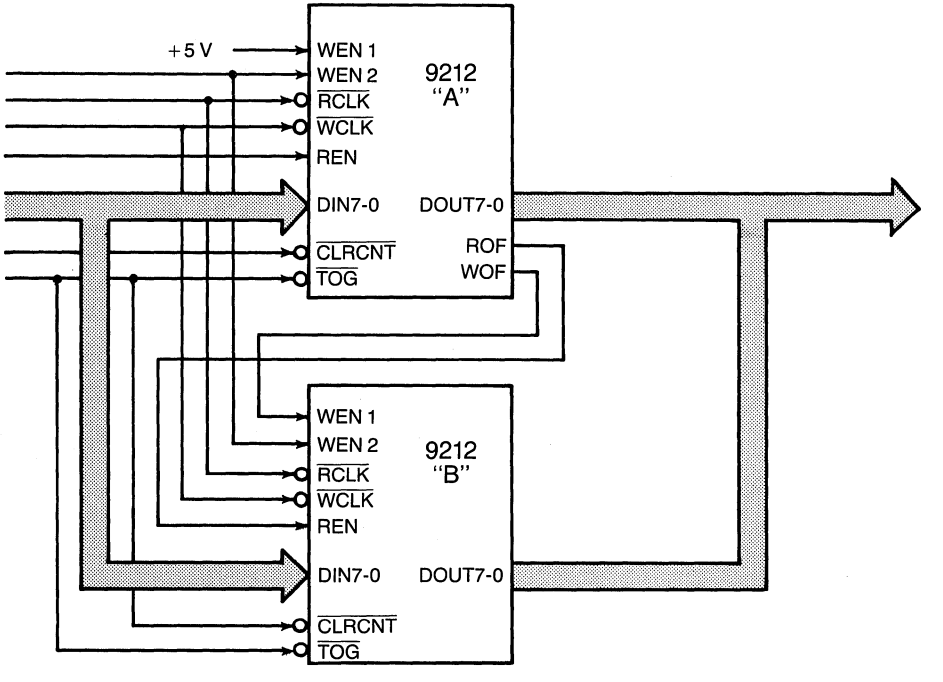



**FIGURE 4: CRT 9212 CASCADED CONFIGURATION FOR DATA ROW LENGTHS UP TO 270 CHARACTERS**

STANDARD MICROSYSTEMS CORPORATION

# CRT 97C11
**PRELIMINARY**

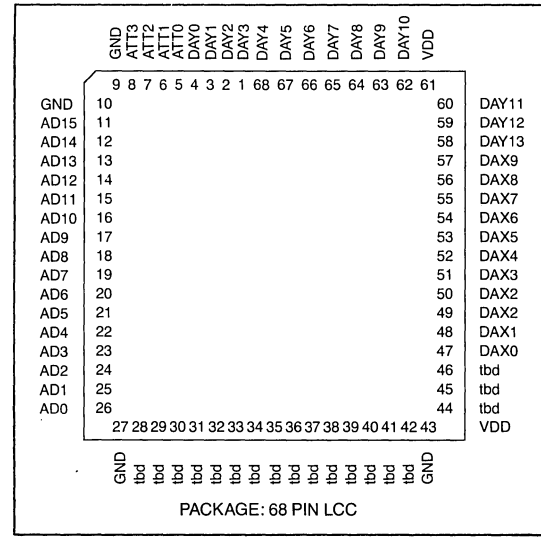
# Video Engine for Windows VIEW



## FEATURES

- ☐ 127 Independent Windows Max per Screen
- ☐ Windows Specified Relative to Screen
  - Window Number
  - X-Y Start Coordinate
  - X-Y End Coordinate
  - Display Memory Address
- ☐ Attributes Can be Specified on a Window Basis
  - Window Priority
  - 8 Parallel Attributes per Window
  - Background Windows
- ☐ 32 Max Visible Horizontal Breaks per Scan Line
- ☐ Three Internal Break Buffers
- ☐ Programmable Cursor Output
- ☐ Fully Programmable Display Format
- ☐ Normal or Interlaced Display
- ☐ External Synchronization of Horizontal and Vertical Drives Available
- ☐ Independent Display and System Buses
  - 24 Bit X-Y Display Memory Address Bus
  - 16 Bit Address/Data Bus to System Memory
- ☐ Separate Clocks for Display and System Buses
- ☐ DMA Master Capability for Interfacing to System Memory

## PIN CONFIGURATION




PACKAGE: 68 PIN LCC

- ☐ Automatic and Transparent Dynamic RAM Refresh for Display Memory

## GENERAL DESCRIPTION

The CRT 97C11 Video Engine for Windows (VIEW) is a third generation CRT controller that is designed to support two-dimensional mapping of video data to a display screen. The VIEW can be used in both bit-map and alphanumeric types of display interfaces. It allows real time manipulation of independent windows on the screen with a minimum of processor intervention.

The system or graphics processor communicates with the VIEW via a window list in system memory. The size and screen location of each window and address pointers to the contents of each window are maintained in this list. The VIEW generates display memory addresses by reconciling the X and Y memory address coordinates at which the windows start and end with the X and Y raster addresses. The VIEW preprocesses and stores this information in three internal break buffers.

As the VIEW generates the display memory addresses for the windows, it automatically resolves priority conflicts that arise when two or more windows overlap. Background windows are output by repetitively addressing a pattern word which significantly optimizes the use display memory. The VIEW can also buffer and output general purpose attribute bits for each window that it displays as it generates that window's addresses. Automatic dynamic RAM refresh addressing during horizontal and vertical retrace intervals is also supported.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge N.Y. 11788
(516) 273-3100 TWX: 510 227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Floppy Disk/Hard Disk

| Part Number | Description | Sector/ Format | Density | Data Bus | Side/Head Select Output | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|---|
| FDC765A/765-2 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 459-474 |
| FDC7265 | Micro Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 459-474 |
| FDC72C65 | CMOS Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 475-476 |
| FDC72C66 | CMOS Micro Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 475-476 |
| FDC9266 | Floppy Disk Controller/Formatter with data separator, and write precompensation generator | Soft | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 523-538 |
| FDC9267 | Floppy Disk Controller/Formatter with high performance analog data separator and write pre-compensation generator | Soft | Double Quad | True | Yes | +5 | 40 DIP/ 44 PLCC | 539-554 |
| FDC9268 | Enhanced Floppy Disk Controller/ Formatter with Data Separator and Write Precompensation Generator | Soft | Double Quad | True | Yes | +5 | 40 DIP/ 44 PLCC | 555-556 |
| FDC9216/B | Floppy Disk Data Separator | Soft/Hard | Double | NA | NA | +5 | 8 DIP | 493-496 |
| FDC9229T/BT | Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double | NA | NA | +5 | 20 DIP/ 28 PLCC | 497-504 |
| FDC92C36/B | Enhanced CMOS Floppy Disk Data Separator | Soft/Hard | Double Quad | NA | NA | +5 | 8 DIP | 505-508 |
| FDC9238/B/BT/T | Enhanced CMOS Floppy Disk Data Separator and Clock Generator | Soft/Hard | Double Quad | NA | NA | +5 | 14 DIP | 509-512 |
| FDC9239B/BT/T | Enhanced CMOS Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double Quad | NA | NA | +5 | 20 DIP/ 28 PLCC | 513-520 |
| FDC92C49 | Analog CMOS Floppy Disk Data Separator, Head Load Timer, Write Precompensation Generator | Soft/Hard | Double Quad | NA | NA | +5 | 24 DIP/ 28 PLCC | 521-522 |
| FDC1791 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | No | +5, +12 | 40 DIP | 477-492 |
| FDC1793 | Floppy Disk Controller/Formatter | Soft | Double | True | No | +5, +12 | 40 DIP | 477-492 |
| FDC1795 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | Yes | +5, +12 | 40 DIP | 477-492 |
| FDC1797 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5, +12 | 40 DIP | 477-492 |
| FDC9791 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | No | +5 | 40 DIP | 557-572 |
| FDC9793 | Floppy Disk Controller/Formatter | Soft | Double | True | No | +5 | 40 DIP | 557-572 |
| FDC9795 | Floppy Disk Controller/Formatter | Soft | Double | Inverted | Yes | +5 | 40 DIP | 557-572 |
| FDC9797 | Floppy Disk Controller/Formatter | Soft | Double | True | Yes | +5 | 40 DIP | 557-572 |
| HDC1100-XX | Hard Disk Controller | Soft | Double | True | NA | +5 | 20 DIP | 573-592 |
| HDC7261 | Hard Disk Controller (ST506/SMD) | Soft/Hard | Double | True | Yes | +5 | 40 DIP | 593-594 |
| HDC9223 | Analog Data Separator Support Circuit | Soft | Double | NA | NA | +12 | 14 DIP | 595-598 |
| HDC9224 | Hard/Floppy Disk Controller Up to 4 drives with tape back-up | Soft (ST-506) | Double | True | Yes | +5 | 40 DIP/ 44 PLCC | 599-634 |
| HDC9225 | Disk Buffer Management Unit | ST-506 | Double | True | NA | +5 | 48 DIP | 635-646 |
| HDC9226 | Hard Disk Data Separator | ST-506 | Double | NA | NA | +5 | 24 DIP/ 28 PLCC | 647-654 |
| HDC9227 | High Performance Hard Disk And Floppy Disk Data Separators | Soft (ST-506) | Double Quad | NA | NA | +5 | 28 DIP | 655-662 |

STANDARD MICROSYSTEMS CORPORATION

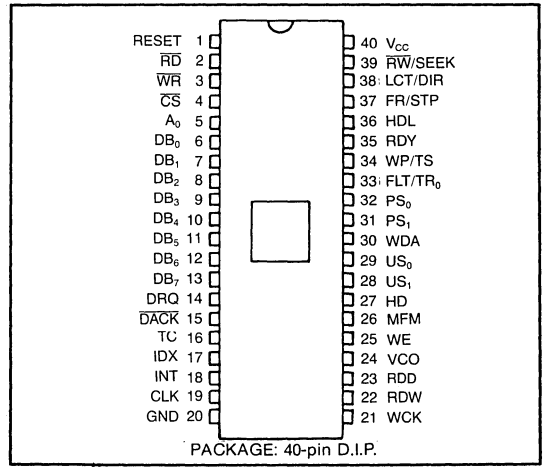
# FDC765A/765A-2
# FDC 7265/7265-2

# Single/Double Density Floppy Disk Controller

## FEATURES

- ☐ IBM Compatible in both Single and Double Density Recording Formats (FDC765A)
- ☐ Sony (EMCA) Compatible Recording Format (FDC7265)
- ☐ Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- ☐ Multi-Sector and Multi-Track Transfer Capability
- ☐ Drive Up to 4 Floppy Disks
- ☐ Data Scan Capability—will scan a Single Sector or an entire cylinder's worth of data fields, comparing on a Byte by Byte Basis, data in the Processor's Memory with data read from the Diskette
- ☐ Data Transfers in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on up to four drives
- ☐ Compatible with Most Microprocessors
- ☐ Single Phase 8 MHz Clock
- ☐ Single + 5 Volt Power Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Available in 40-Pin Dual-in-Line Package

## PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

## GENERAL DESCRIPTION

The FDC765A is an LSI floppy disk controller (FDC) chip, which contains the circuitry and control functions for interfacing a processor to 4 floppy disk drives. It is capable of either IBM 3740 single density format (FM), or IBM System 34 double density format (MFM) including double-sided recording. The FDC765A provides control signals which simplify the design of an external phase-locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy disk interface.

The FDC7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppydisk® drive. The FDC7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The FDC7265 can read a diskette that has been formatted by the FDC765A.

Each of these devices is also available in a -2 version. The -2 versions represent a reduction from 4-micron to 3-micron design rule. Functionally is the same. Minor differences between the two versions are detailed in the AC Characteristics table. The -2 versions are only available in the plastic package at this time.

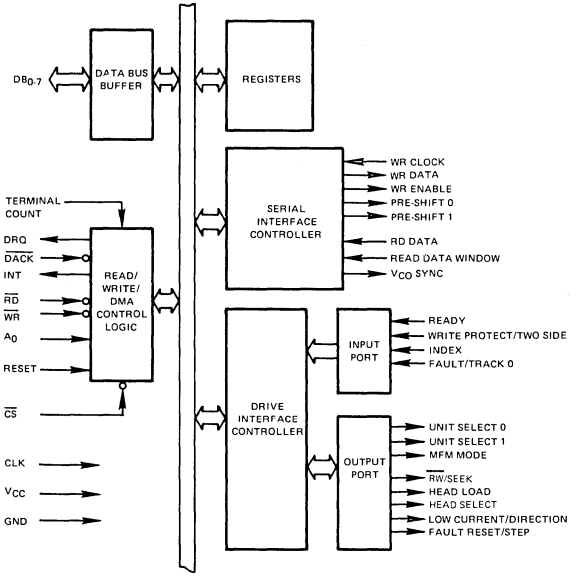
Hand-shaking signals are provided in the FDC765A/FDC7265 which make DMA operation easy to incorporate with the aid of an external DMA controller chip. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 15 commands which the FDC765A/FDC7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

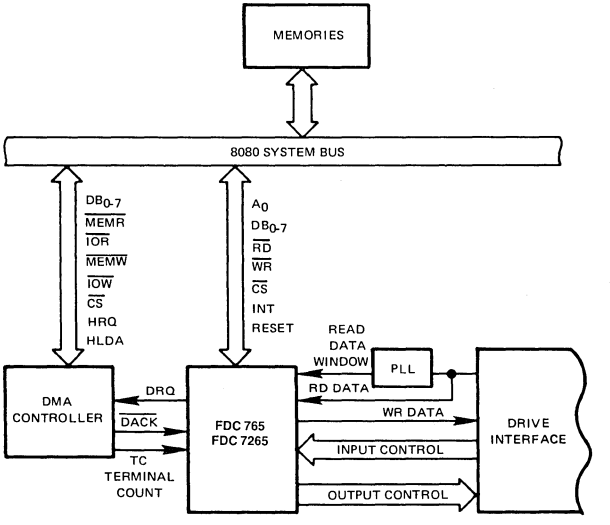
| | |
|---|---|
| Read Data | Read Deleted Data |
| Read ID | Write Data |
| Specify | Format Track |
| Read Track | Write Deleted Data |
| Scan Equal | Seek |
| Scan High or Equal | Recalibrate |
| Scan Low or Equal | Sense Interrupt Status |
| | Sense Drive Status |

Address mark detection circuitry is internal to the FDC which simplifies the phase-locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The FDC765A/FDC7265 offers additional features such as multi-track and multi-side read and write commands and single and double density capabilities.

SECTION VI




**BLOCK DIAGRAM**




**SYSTEM CONFIGURATION**

## DESCRIPTION OF PIN FUNCTIONS

| PIN | | | INPUT/ OUTPUT | CONNECTION TO | FUNCTION |
|---|---|---|---|---|---|
| NO. | SYMBOL | NAME | | | |
| 1 | RST | Reset | Input | Processor | Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command. |
| 2 | $\overline{RD}$ | Read | Input① | Processor | Control signal for transfer of data from FDC to Data Bus, when "0" (low). |
| 3 | $\overline{WR}$ | Write | Input① | Processor | Control signal for transfer of data to FDC via Data Bus, when "0" (low). |
| 4 | $\overline{CS}$ | Chip Select | Input | Processor | IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled. |
| 5 | $A_0$ | Data/Status Reg Select | Input① | Processor | Selects Data Reg ($A_0$ = 1) or Status Reg ($A_0$ = 0) contents of the FDC to be sent to Data Bus. |
| 6-13 | $DB_0$-$DB_7$ | Data Bus | Input① Output | Processor | Bi-Directional 8-Bit Data Bus. |
| 14 | DRQ | Data DMA Request | Output | DMA | DMA Request is being made by FDC when DRW = "1". |
| 15 | $\overline{DACK}$ | DMA Acknowledge | Input | DMA | DMA cycle is active when "0" (low) and Controller is performing DMA transfer. |
| 16 | TC | Terminal Count | Input | DMA | Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode. |
| 17 | IDX | Index | Input | FDD | Indicates the beginning of a disk track. |
| 18 | INT | Interrupt | Output | Processor | Interrupt Request Generated by FDC. |
| 19 | CLK | Clock | Input | | Single Phase 8 MHz Squarewave Clock. |
| 20 | GND | Ground | | | D.C. Power Return. |
| 21 | WCK | Write Clock | Input | | Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM. |
| 22 | RDW | Read Data Window | Input | Phase Lock Loop | Generated by PLL, and used to sample data from FDD. |
| 23 | RDD | Read Data | Input | FDD | Read data from FDD, containing clock and data bits. |
| 24 | VCO | VCO Sync | Output | Phase Lock Loop | Inhibits VCO in PLL when "0" (low), enables VCO when "1." |
| 25 | WE | Write Enable | Output | FDD | Enables write data into FDD. |
| 26 | MFM | MFM Mode | Output | Phase Lock Loop | MFM mode when "1," FM mode when "0." |
| 27 | HD | Head Select | Output | FDD | Head 1 selected when "1" (high). Head 2 selected when "0" (low). |
| 28, 29 | $US_1$, $US_0$ | Unit Select | Output | FDD | FDD Unit Selected. |
| 30 | WDA | Write Data | Output | FDD | Serial clock and data bits to FDD. |
| 31, 32 | $PS_1$, $PS_0$ | Precompensation (pre-shift) | Output | FDD | Write precompensation status during MFM mode. Determines early, late, and normal times. |
| 33 | $FLT/TR_0$ | Fault/Track 0 | Input | FDD | Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode. |
| 34 | WP/TS | Write Protect/ Two-Side | Input | FDD | Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | PIN SYMBOL | PIN NAME | INPUT/ OUTPUT | CONNECTION TO | FUNCTION |
|---|---|---|---|---|---|
| 35 | RDY | Ready | Input | FDD | Indicates FDD is ready to send or receive data. |
| 36 | HDL | Head Load | Output | FDD | Command which causes read/ write head in FDD to contact diskette. |
| 37 | FR/STP | Fit Reset/Stop | Output | FDD | Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode. |
| 38 | LCT/DIR | Low Current/ Direction | Output | FDD | Lowers Write current on inner tracks in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal. |
| 39 | $\overline{RW}$/SEEK | Read Write/SEEK | Output | FDD | When "1" (high) Seek mode selected and when "0" (low) Read/ Write mode selected. |
| 40 | $V_{CC}$ | +5V | | | DC Power. |

Note: ① Disabled when CS = 1.

## DESCRIPTION OF INTERNAL REGISTERS

The FDC765A/7265 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC.

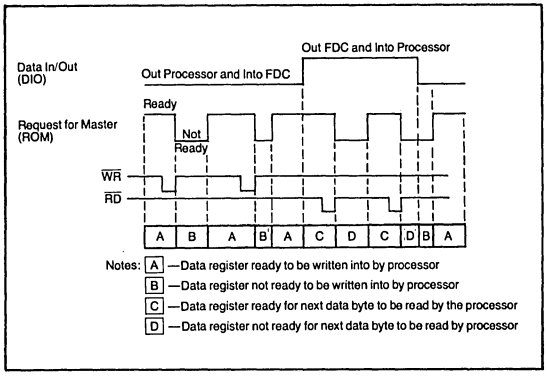
The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and $A_0$ is shown below.

| $A_0$ | $\overline{RD}$ | $\overline{WR}$ | FUNCTION |
|---|---|---|---|
| 0 | 0 | 1 | Read Main Status Register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from Data Register |
| 1 | 1 | 0 | Write into Data Register |

The bits in the Main Status Register are defined as follows:

| BIT NUMBER | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| $DB_0$ | FDD 0 Busy | $D_0B$ | FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_1$ | FDD 1 Busy | $D_1B$ | FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_2$ | FDD 2 Busy | $D_2B$ | FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_3$ | FDD 3 Busy | $D_3B$ | FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_4$ | FDC Busy | CB | A read or write command is in process. FDC will not accept any other command. |
| $DB_5$ | Execution Mode | EXM | This bit is set only during execution phase in non-DMA mode. When $DB_5$ goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation. |
| $DB_6$ | Data Input/Output | DIO | Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register. |
| $DB_7$ | Request for Master | RQM | Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor. |

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when $DB_4$ (FDC Busy) goes low is 12 μs.




## COMMAND SEQUENCE

The FDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

| | |
|---|---|
| Command Phase: | The FDC receives all information required to perform a particular operation from the processor. |
| Execution Phase: | The FDC performs the operation it was instructed to do. |
| Result Phase: | After completion of the operation, status and other housekeeping information are made available to the processor. |

## COMMAND SYMBOL DESCRIPTION

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| $A_0$ | Address Line 0 | $A_0$ controls selection of Main Status Register ($A_0$ = 0) or Data Register ($A_0$ = 1). |
| C | Cylinder Number | C stands for the current/selected Cylinder (track) number 0 through 76 of the medium. |
| D | Data | D stands for the data pattern which is going to be written into a Sector. |
| $D_7$-$D_0$ | Data Bus | 8-bit Data Bus, where $D_7$ stands for a most significant bit, and $D_0$ stands for a least significant bit. |
| DTL | Data Length | When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector. |
| EOT | End of Track | EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT. |
| GPL | Gap Length | GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3. |
| H | Head Address | H stands for head number 0 or 1, as specified in ID field. |
| HD | Head | HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.) |
| HLT | Head Load Time | HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments). |
| HUT | Head Unload Time | HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments). |
| MF | FM or MFM Mode | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT | Multi-Track | If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1. |
| N | Number | N stands for the number of data bytes written in a Sector. |
| NCN | New Cylinder Number | NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head. |
| ND | Non-DMA Mode | ND stands for operation in the Non-DMA Mode. |
| PCN | Present Cylinder Number | PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time. |
| R | Record | R stands for the Sector number, which will be read or written. |
| R/W | Read/Write | R/W stands for either Read (R) or Write (W) signal. |
| SC | Sector | SC indicates the number of Sectors per Cylinder. |
| SK | Skip | SK stands for Skip Deleted Data Address Mark. |
| SRT | Step Rate Time | SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.). |
| ST 0<br>ST 1<br>ST 2<br>ST 3 | Status 0<br>Status 1<br>Status 2<br>Status 3 | ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0$ = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command. |
| STP | | During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared. |
| US0, US1 | Unit Select | US stands for a selected drive number 0 or 1. |

# INSTRUCTION SET ① ②

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 0 | 1 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 1 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 0 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the main-system and FDD |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | SK | 0 | 0 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT. |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ ID** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 0 | 1 | 0 | Commands |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Execution | | | | | | | | | | The first correct ID information on the Cylinder is stored in Data Register |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information read during Execution Phase from Floppy Disk |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **FORMAT A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | N | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | Sectors/Track |
| | W | GPL | | | | | | | | Gap 3 |
| | W | D | | | | | | | | Filler Byte |
| Execution | | | | | | | | | | FDC formats an entire track |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | In this case, the ID information has no meaning |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 0 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

**Note:** ① Symbols used in this table are described at the end of this section.

② $A_0$ should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

## INSTRUCTION SET (CONT.)

| PHASE | R/W | DATA BUS $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | REMARKS |
|---|---|---|---|
| **SCAN LOW OR EQUAL** | | | |
| Command | W | MT MF SK 1 1 0 0 1 | Command Codes |
| | W | X X X X X HD US1 US0 | |
| | W | C | Sector ID information prior Command execution |
| | W | H | |
| | W | R | |
| | W | N | |
| | W | EOT | |
| | W | GPL | |
| | W | STP | |
| Execution | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | Status information after Command execution |
| | R | ST 1 | |
| | R | ST 2 | |
| | R | C | Sector ID information after Command execution |
| | R | H | |
| | R | R | |
| | R | N | |
| **SCAN HIGH OR EQUAL** | | | |
| Command | W | MT MF SK 1 1 1 0 1 | Command Codes |
| | W | X X X X X HD US1 US0 | |
| | W | C | Sector ID information prior Command execution |
| | W | H | |
| | W | R | |
| | W | N | |
| | W | EOT | |
| | W | GPL | |
| | W | STP | |
| Execution | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | Status information after Command execution |
| | R | ST 1 | |
| | R | ST 2 | |
| | R | C | Sector ID information after Command execution |
| | R | H | |
| | R | R | |
| | R | N | |

| PHASE | R/W | DATA BUS $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$ | REMARKS |
|---|---|---|---|
| **RECALIBRATE** | | | |
| Command | W | 0 0 0 0 0 1 1 1 | Command Codes |
| | W | X X X X X 0 US1 US0 | |
| Execution | | | Head retracted to Track 0 |
| **SENSE INTERRUPT STATUS** | | | |
| Command | W | 0 0 0 0 1 0 0 0 | Command Codes |
| Result | R | STO | Status information at the end of seek-operation about the FDC |
| | R | PCN | |
| **SPECIFY** | | | |
| Command | W | 0 0 0 0 0 0 1 1 | Command Codes |
| | W | SRT → ← HUT | |
| | W | HLT → ND | |
| **SENSE DRIVE STATUS** | | | |
| Command | W | 0 0 0 0 0 1 0 0 | Command Codes |
| | W | X X X X X HD US1 US0 | |
| Result | R | ST 3 | Status information about FDD |
| **SEEK** | | | |
| Command | W | 0 0 0 0 1 1 1 1 | Command Codes |
| | W | X X X X X HD US1 US0 | |
| | W | NCN | |
| Execution | | | Head is positioned over proper Cylinder on Diskette |
| **INVALID** | | | |
| Command | W | Invalid Codes | Invalid Command Codes (NoOp – FDC goes into Standby State) |
| Result | R | ST 0 | ST 0 = 80 (16) |

## FUNCTIONAL DESCRIPTION OF COMMANDS

### Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

| Multi-Track MT | MFM/FM MF | Bytes/Sector N | Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors) | Final Sector Read from Diskette |
|---|---|---|---|---|
| 0 | 0 | 00 | (128) (26) = 3,328 | 26 at Side 0 |
| 0 | 1 | 01 | (256) (26) = 6,656 | or 26 at Side 1 |
| 1 | 0 | 00 | (128) (52) = 6,656 | 26 at Side 1 |
| 1 | 1 | 01 | (256) (52) = 13,312 | |
| 0 | 0 | 01 | (256) (15) = 3,840 | 15 at Side 0 |
| 0 | 1 | 02 | (512) (15) = 7,680 | or 15 at Side 1 |
| 1 | 0 | 01 | (256) (30) = 7,680 | 15 at Side 1 |
| 1 | 1 | 02 | (512) (30) = 15,360 | |
| 0 | 0 | 02 | (512) (8) = 4,096 | 8 at Side 0 |
| 0 | 1 | 03 | (1024) (8) = 8,192 | or 8 at Side 1 |
| 1 | 0 | 02 | (512) (16) = 8,192 | 8 at Side 1 |
| 1 | 1 | 03 | (1024) (16) = 16,384 | |

**Table 1. Transfer Capacity**

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

| MT | HD | Final Sector Transferred to Processor | ID Information at Result Phase | | | |
|---|---|---|---|---|---|---|
| | | | C | H | R | N |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | NC | LSB | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | LSB | R = 01 | NC |

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

## Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

## Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

## Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

## Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

| Format | Sector Size | N | SC | GPL① | GPL②③ |
|---|---|---|---|---|---|
| 8″ Standard Floppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 1A | 07 | 1B |
| | 256 | 01 | 0F | 0E | 2A |
| | 512 | 02 | 08 | 1B | 3A |
| | 1024 | 03 | 04 | 47 | 8A |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 1A | 0E | 36 |
| | 512 | 02 | 0F | 1B | 54 |
| | 1024 | 03 | 08 | 35 | 74 |
| | 2048 | 04 | 04 | 99 | FF |
| | 4096 | 05 | 02 | C8 | FF |
| | 8192 | 06 | 01 | C8 | FF |
| 5¼″ Minifloppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 12 | 07 | 09 |
| | 128 | 00 | 10 | 10 | 19 |
| | 256 | 01 | 08 | 18 | 30 |
| | 512 | 02 | 04 | 46 | 87 |
| | 1024 | 03 | 02 | C8 | FF |
| | 2048 | 04 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 12 | 0A | 0C |
| | 256 | 01 | 10 | 20 | 32 |
| | 512 | 02 | 08 | 2A | 50 |
| | 1024 | 03 | 04 | 80 | F0 |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| 3½″ Sony Micro Floppydisk® | | | | | |
| FM Mode | 128 bytes/sector | 0 | 0F | 07 | 1B |
| | 256 | 1 | 09 | 0E | 2A |
| | 512 | 2 | 05 | 1B | 3A |
| MFM Mode ④ | 256 | 1 | 0F | 0E | 36 |
| | 512 | 2 | 09 | 1B | 54 |
| | 1024 | 3 | 05 | 35 | 74 |

***Table 3***

**Notes:** ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

### Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

### Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

### Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$; $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

| COMMAND | STATUS REGISTER 2 | | COMMENTS |
|---|---|---|---|
| | BIT 2 = SN | BIT 3 = SH | |
| Scan Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} \neq D_{PROCESSOR}$ |
| Scan Low or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} < D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| Scan High or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} < D_{PROCESSOR}$ |

**Table 4**

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

## Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $DB_0$-$DB_3$ in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

## Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

## Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

| SEEK END | INTERRUPT CODE | | |
|---|---|---|---|
| BITS 5 | BIT 6 | BIT 7 | CAUSE |
| 0 | 1 | 1 | Ready Line changed state, either polarity |
| 1 | 0 | 0 | Normal Termination of Seek or Recalibrate Command |
| 1 | 1 | 0 | Abnormal Termination of Seek or Recalibrate Command |

**Table 5**

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

### Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms).The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

### Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

### Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC765A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.



## STATUS REGISTER IDENTIFICATION

| BIT | | | |
|---|---|---|---|
| NO. | NAME | SYMBOL | DESCRIPTION |
| $D_7$ $D_6$ | Interrupt Code | IC | $D_7$ = 0 and $D_6$ = 0<br>Normal Termination of Command, (NT). Command was completed and properly executed. |
| | | | $D_7$ = 0 and $D_6$ = 1<br>Abnormal Termination of Command, (AT).<br>Execution of Command was started, but was not successfully completed. |
| | | | $D_7$ = 1 and $D_6$ = 0<br>Invalid Command issue, (IC). Command which was issued was never started. |
| | | | $D_7$ = 1 and $D_6$ = 1<br>Abnormal Termination because during command execution the ready signal from FDD changed state. |
| $D_5$ | Seek End | SE | When the FDC completes the SEEK Command, this flag is set to 1 (high). |
| $D_4$ | Equipment Check | EC | If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set. |
| $D_3$ | Not Ready | NR | When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set. |
| $D_2$ | Head Address | HD | This flag is used to indicate the state of the head at Interrupt. |
| $D_1$ | Unit Select 1 | US 1 | These flags are used to indicate a Drive Unit. Number at Interrupt. |
| $D_0$ | Unit Select 0 | US 0 | |

| BIT NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| | | | **STATUS REGISTER 1(CONT.)** |
| $D_7$ | End of Cylinder | EN | When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set. |
| $D_6$ | | | Not used. This bit is always 0 (low). |
| $D_5$ | Data Errror | DE | When the FDC detects a CRC error in either the ID field or the data field, this flag is set. |
| $D_4$ | Over Run | OR | If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set. |
| $D_3$ | | | Not used. This bit always 0 (low). |
| $D_2$ | No Data | ND | During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set. |
| | | | During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set. |
| | | | During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set. |
| $D_1$ | Not Writable | NW | During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set. |
| $D_0$ | Missing Address Mark | MA | If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. |
| | | | If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set. |
| | | | **STATUS REGISTER 2** |
| $D_7$ | | | Not used. This bit is always 0 (low). |
| $D_6$ | Control Mark | CM | During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set. |
| $D_5$ | Data Error in Data Field | DD | If the FDC detects a CRC error in the data field then this flag is set. |
| $D_4$ | Wrong Cylinder | WC | This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set. |
| $D_3$ | Scan Equal Hit | SH | During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set. |
| $D_2$ | Scan Not Satisfied | SN | During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set. |
| $D_1$ | Bad Cylinder | BC | This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set. |
| $D_0$ | Missing Address Mark in Data Field | MD | When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set. |
| | | | **STATUS REGISTER 3** |
| $D_7$ | Fault | FT | This bit is used to indicate the status of the Fault signal from the FDD. |
| $D_6$ | Write Protected | WP | This bit is used to indicate the status of the Write Protected signal from the FDD. |
| $D_5$ | Ready | RY | This bit is used to indicate the status of the Ready signal from the FDD. |
| $D_4$ | Track 0 | T0 | This bit is used to indicate the status of the Track 0 signal from the FDD. |
| $D_3$ | Two Side | TS | This bit is used to indicate the status of the Two Side signal from the FDD. |
| $D_2$ | Head Address | HD | This bit is used to indicate the status of Side Select signal to the FDD. |
| $D_1$ | Unit Select 1 | US 1 | This bit is used to indicate the status of the Unit Select 1 signal to the FDD. |
| $D_0$ | Unit Select 0 | US 0 | This bit is used to indicate the status of the Unit Select 0 signal to the FDD. |

## PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC is in the NON-DMA Mode, then the receipt of each data byte (if FDC is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The FDC contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

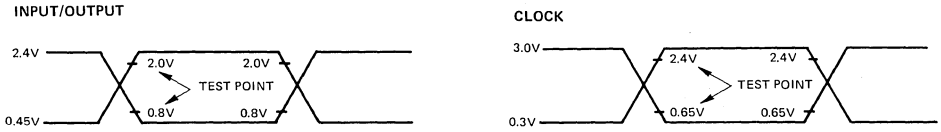
The bytes of data which are sent to the FDC to form the Command Phase, and are read out of the FDC in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC is ready for a new command.

## POLLING FEATURE OF THE FDC765A/7265

After the Specify command has been sent to the FDC, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

SECTION VI

## AC TEST CONDITION



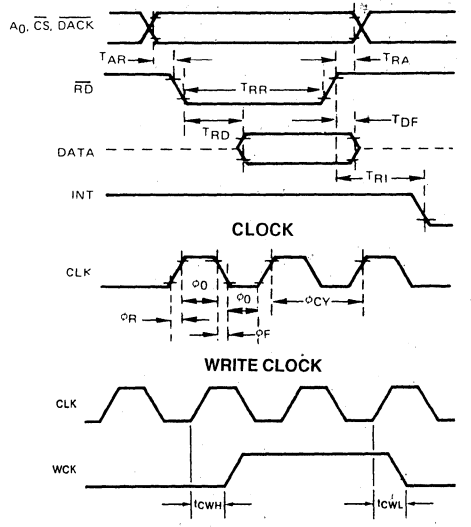

## AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

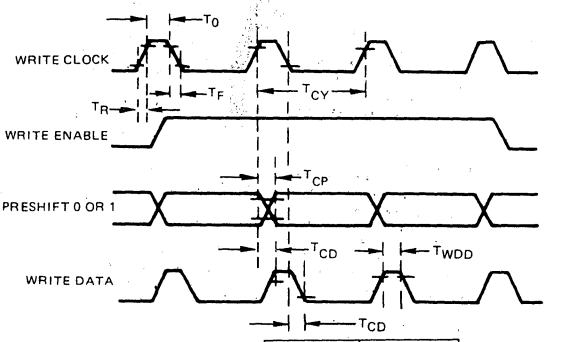
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

## TIMING DIAGRAMS

### PROCESSOR READ OPERATION




### FDD WRITE OPERATION




| | PRESHIFT 0 | PRESHIFT 1 |
|---|---|---|
| NORMAL | 0 | 0 |
| LATE | 0 | 1 |
| EARLY | 1 | 0 |
| INVALID | 1 | 1 |

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −55°c to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage $V_{CC}$ ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS $T_a$ = 0°C to +70°C; $V_{CC}$ = +5V ±5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP① | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | −0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.5 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | $V_{CC}$ | V | $I_{OH}$ = −200 µA |
| Input Low Voltage (CLK + WR Clock) | $V_{IL(\phi)}$ | −0.5 | | 0.65 | V | |
| Input High Voltage (CLK + WR Clock) | $V_{IH(\phi)}$ | 2.4 | | $V_{CC}$ + 0.5 | V | |
| $V_{CC}$ Supply Current | $I_{CC}$ | | | 150 | mA | |
| Input Load Current (All Input Pins) | $I_{LI}$ | | | 10 | µA | $V_{IN}$ = $V_{CC}$ |
| | | | | −10 | µA | $V_{IN}$ = 0V |
| High Level Output Leakage Current | $I_{LOH}$ | | | 10 | µA | $V_{OUT}$ = $V_{CC}$ |
| Low Level Output Leakage Current | $I_{LOL}$ | | | −10 | µA | $V_{OUT}$ = +0.45V |

NOTE: ①Typical values for $T_a$ = 25°C and nominal supply voltage.

### CAPACITANCE $T_a$ = 25°C; $f_c$ = 1 MHz; $V_{CC}$ = 0V

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Input Capacitance | $C_{IN(\phi)}$ | | | 20 | pF | All Pins Except Pin Under Test Tied to AC Ground |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

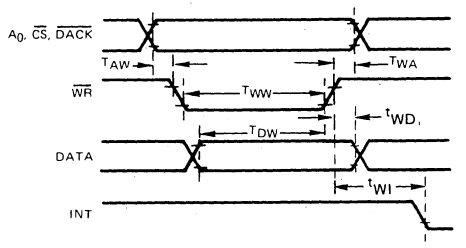
**AC CHARACTERISTICS** $T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| | | 765A, 7265 | | | 765A-2, 7265 | | | | |
| | | MIN | TYP① | MAX | MIN | TYP① | MAX | | |
| Clock Period | $\phi_{CY}$ | 120 | 125 | 500 | 120 | 125 | 500 | ns | |
| Clock Active (High, Low) | $\phi_0$ | 40 | | | 40 | | | ns | |
| Clock Rise Time | $\phi_r$ | | | 20 | | | 20 | ns | |
| Clock Fall Time | $\phi_f$ | | | 20 | | | 20 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓ | $T_{AR}$ | 0 | | | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑ | $T_{RA}$ | 0 | | | 0 | | | ns | |
| $\overline{RD}$ Width | $T_{RR}$ | 250 | | | 200 | | | ns | |
| Data Access Time from $\overline{RD}$ ↓ | $T_{RD}$ | | | 200 | | | 140 | ns | $C_L = 100$ pF |
| DB to Float Delay Time from $\overline{RD}$ ↑ | $T_{DF}$ | 20 | | 100 | 10 | | 85 | ns | $C_L = 100$ pF |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓ | $T_{AW}$ | 0 | | | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑ | $T_{WA}$ | 0 | | | 0 | | | ns | |
| $\overline{WR}$ Width | $T_{WW}$ | 250 | | | 200 | | | ns | |
| Data Set Up Time to $\overline{WR}$ ↑ | $T_{DW}$ | 150 | | | 100 | | | ns | |
| Data Hold Time from $\overline{WR}$ ↑ | $T_{WD}$ | 5 | | | 0 | | | ns | |
| INT Delay Time from $\overline{RD}$ ↑ | $T_{RI}$ | | | 500 | | | 400 | ns | |
| INT Delay Time from $\overline{WR}$ ↑ | $T_{WI}$ | | | 500 | | | 400 | ns | |
| DRQ Cycle Time | $T_{MCY}$ | 13 | | | 13 | | | µs | |
| DRQ Delay Time from $\overline{DACK}$ ↓ | $T_{AM}$ | | | 200 | | | 140 | ns | |
| DRQ ↑ to $\overline{DACK}$ ↓ Delay | $T_{MA}$ | 2 | | | 2 | | | $\phi_{CY}$ | |
| $\overline{DACK}$ width | $T_{AA}$ | 2 | | | 2 | | | $\phi_{CY}$ | |
| TC Width | $T_{TC}$ | 1 | | | 1 | | | $\phi_{CY}$ | |
| Reset Width | $T_{RST}$ | 14 | | | 14 | | | $\phi_{CY}$ | |
| WCK CYCLE TIME | $T_{WCY}$ | | 16<br>8 | | | 16<br>8 | | µs | MFM = 0 5¼"<br>MFM = 1 5¼" |
| | | | 8<br>4 | | | 8<br>4 | | | MFM = 0 8"<br>MFM = 1 8" |
| | | | 8<br>4 | | | 8<br>4 | | | MFM = 0 3½" ⑤<br>MFM = 1 3½" ⑤ |
| | | | 16<br>8 | | | 16<br>8 | | | MFM = 0 3½" ⑥<br>MFM = 1 3½" ⑥ |
| WCK Active Time (High) | $T_0$ | 80 | 250 | 350 | 80 | 250 | 350 | ns | |
| CLK ↑ to WCK ↑ Delay | $T_{CWH}$ | 0 | | 40 | 0 | | 40 | ns | |
| CLK ↑ to WCK ↓ Delay | $T_{CWL}$ | 0 | | 40 | 0 | | 40 | ns | |
| WCK Rise Time | $T_r$ | | | 20 | | | 20 | ns | |
| WCK Fall Time | $T_f$ | | | 20 | | | 20 | ns | |
| Pre-Shift Delay Time from WCK ↑ | $T_{CP}$ | 20 | | 100 | 20 | | 100 | ns | |
| WDA Delay Time from WCK ↑ | $T_{CD}$ | 20 | | 100 | 20 | | 100 | ns | |
| RDD Active Time (High) | $T_{RDD}$ | 40 | | | 40 | | | ns | |
| Window Cycle Time | $T_{WCY}$ | | 2.0<br>1.0 | | | 2.0<br>1.0 | | µs | MFM = 0<br>MFM = 1 |
| Window Hold Time to/from RDD | $T_{RDW}$<br>$T_{WRD}$ | 15 | | | 15 | | | ns | |
| $US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑ | $T_{US}$ | 12 | | | 12 | | | µs | 8 MHz Clock Period |
| SEEK/$\overline{RW}$ Hold Time to LOW CURRENT/DIRECTION ↑ | $T_{SD}$ | 7 | | | 7 | | | µs | |
| LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑ | $T_{DST}$ | 1.0 | | | 1.0 | | | µs | |
| $US_{0,1}$ Hold Time from FAULT RESET/STEP ↑ | $T_{STU}$ | 5.0 | | | 5.0 | | | µs | |
| STEP Active Time (High) | $T_{STP}$ | 6.0 | 7.0 | 8.0 | 6.0 | 7.0 | 8.0 | µs | |
| STEP Cycle Time | $T_{SC}$ | 33 | ③ | ③ | 33 | ③ | ③ | µs | |
| FAULT RESET Active Time (High) | $T_{FR}$ | 8.0 | | 10 | 8.0 | | 10.0 | µs | |
| Write Data Width | $T_{WDD}$ | $T_0$-50 | | | $T_0$-50 | | | ns | |
| $US_{0,1}$ Hold Time After SEEK | $T_{SU}$ | 15 | | | 15 | | | µs | 8 MHz Clock Period |
| Seek Hold Time from DIR | $T_{DS}$ | 30 | | | 30 | | | µs | |
| DIR Hold Time after STEP | $T_{STD}$ | 24 | | | 24 | | | µs | |
| Index Pulse Width | $T_{IDX}$ | 10 | | | 4 | | | $\phi_{CY}$ | |
| $\overline{RD}$ ↓ Delay from DRQ | $T_{MR}$ | 800 | | | 800 | | | ns | 8 MHz Clock Period |
| $\overline{WR}$ ↓ Delay from DRQ | $T_{MW}$ | 250 | | | 250 | | | ns | |
| $\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑ | $T_{MRW}$ | | | 12 | | | 12 | µs | |

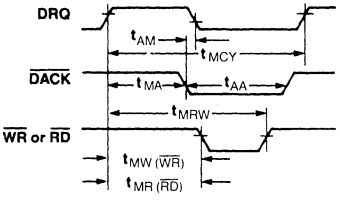
NOTES: ① µ Typical values for $T_a = 25°C$ and nominal supply voltage.
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.
③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.
④ For mini-floppy applications, $\phi_{CY}$ must be 4 mHz.
⑤ Sony microfloppy 3½" drive (8" compatible).
⑥ Sony microfloppy 3½" drive (5¼" compatible).

## TIMING DIAGRAMS

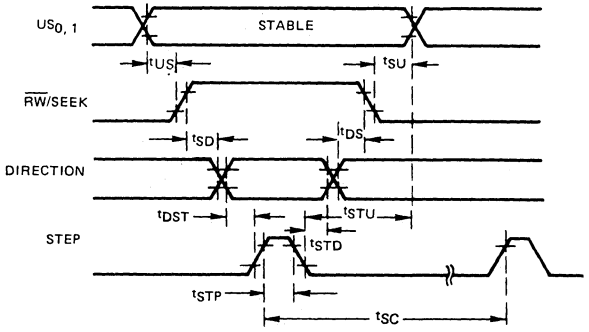
### PROCESSOR WRITE OPERATION




### DMA OPERATION

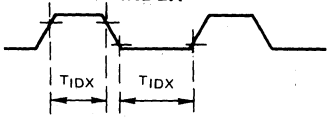



### SEEK OPERATION

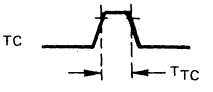



### FLT RESET

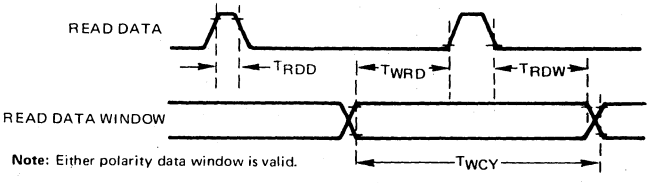

### INDEX




### TERMINAL COUNT

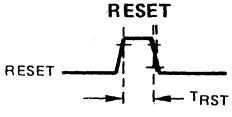



### FDD READ OPERATION




**Note:** Either polarity data window is valid.

### RESET




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge NY 11788
(516) 273-3100 TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

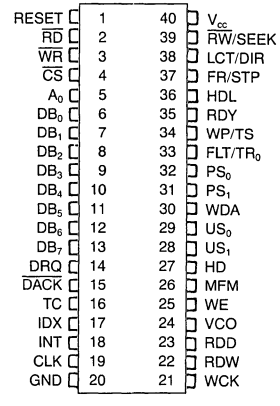
# FDC 72C65
# FDC 72C66
**PRELIMINARY**

# Programmable Floppy Disk Controller

## FEATURES

- ☐ FDC765A compatible
- ☐ IBM Compatible in both Single and Double Density Recording Formats (FDC72C65)
- ☐ Sony (EMCA) Compatible Recording Format (FDC72C66)
- ☐ Selectable Data Recording Lengths: 128, 256, 512 or 1024 Bytes/Sector
- ☐ Multi-Sector and Multi-Track Transfer Capability
- ☐ Sector Read/Write Capability (128 Bytes/Sector only)
- ☐ Drive Up to 4 Floppy Disk Drives
- ☐ CRC Function
- ☐ Programmable Step and Head Load/Unload Time
- ☐ Data Scan Capability
- ☐ Transfer in DMA or Non-DMA Mode
- ☐ Parallel Seek Operation on up to 4 Drives
- ☐ Write Precompensation Signal
- ☐ Software Reset Capability
- ☐ Single Phase Clock
  8 MHz for Standard Floppy Disk
  4 MHz for Mini Floppy Disk
- ☐ CMOS
- ☐ Available in 40-pin DIP or 52-pin Flat Pack

## PIN CONFIGURATION




PACKAGE: 40-pin DIP

## GENERAL DESCRIPTION

The FDC72C65 is an enhanced pin-compatible CMOS version of the industry standard FDC765A. The FDC72C65 contains the circuitry and control functions for interfacing a processor to 4 floppy-disk drives. It is capable of supporting either IBM 3740 Single Density format (FM) or IBM System 34 Double Density format (MFM) including double-sided recording. The FDC72C65 provides control signals which simplify the design of an external phase lock loop and write precompensation circuitry. The FDC72C65 handles most of the burdens associated with implementing a floppy-disk interface.

The FDC72C66 is the CMOS equivalent to the FDC7265, designed specifically for the Sony Micro Floppydisk drive. The FDC72C66 can utilize the Sony recording format.

There are 18 separate commands which the FDC will execute. Three commands are new and provide the system programmer with a software RESET and ON/OFF switches for low power mode (a benefit to battery powered portable computers).

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

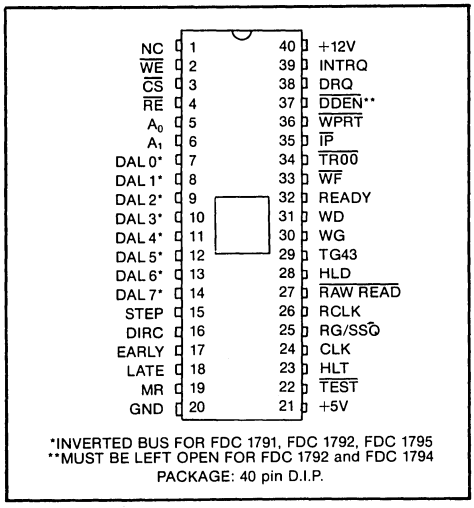
# FDC 1791-02
# FDC 1792-02
# FDC 1793-02
# FDC 1794-02
# FDC 1795-02
# FDC 1797-02
## μPC FAMILY

# Floppy Disk Controller/Formatter FDC

### FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1795, FDC 1797)
- ☐ WINDOW EXTENSION (IN MFM)

### PIN CONFIGURATION




*INVERTED BUS FOR FDC 1791, FDC 1792, FDC 1795
**MUST BE LEFT OPEN FOR FDC 1792 and FDC 1794
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

### GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into six specific parts: FDC 1791, FDC 1792, FDC 1793, FDC 1794, FDC 1795, and the FDC 1797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

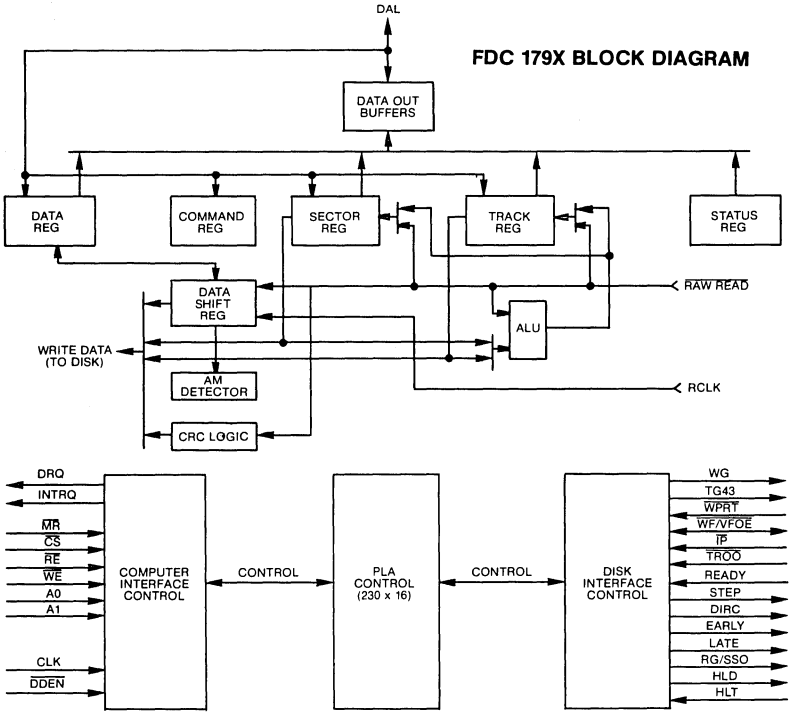
The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

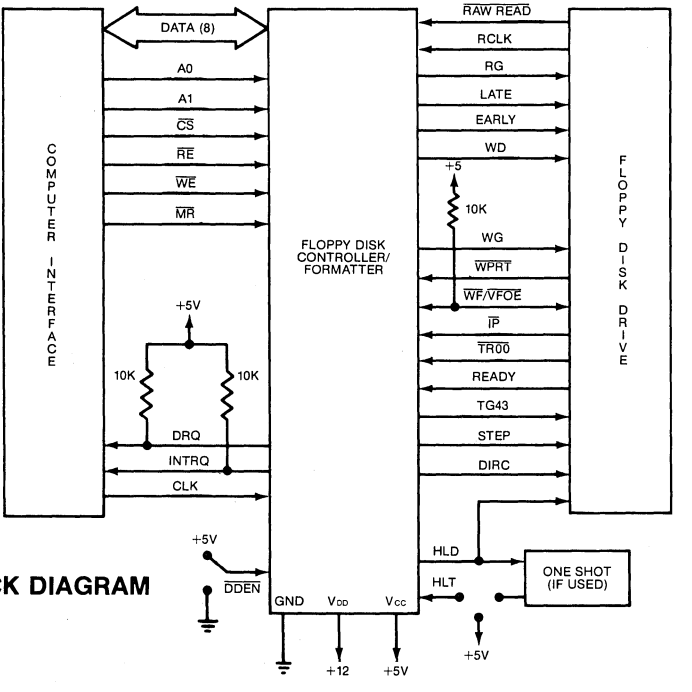
The FDC 1792 operates in the single density mode only. Pin 37 ($\overline{\text{DDEN}}$) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses. The FDC 1795 adds side select logic to the FDC 1791. The FDC 1797 adds the side select logic to the FDC 1793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

## FDC 179X BLOCK DIAGRAM




## SYSTEM BLOCK DIAGRAM



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | NO CONNECTION | NC | This pin is internally connected to the substrate bias generator and must be left open. |
| 20 | GROUND | $V_{SS}$ | Ground |
| 21 | POWER SUPPLY | $V_{CC}$ | +5V |
| 40 | POWER SUPPLY | $V_{DD}$ | +12V |
| 19 | $\overline{\text{MASTER RESET}}$ | $\overline{\text{MR}}$ | A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register. |
| **COMPUTER INTERFACE:** | | | |
| 2 | $\overline{\text{WRITE ENABLE}}$ | $\overline{\text{WE}}$ | A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low. |
| 3 | $\overline{\text{CHIP SELECT}}$ | $\overline{\text{CS}}$ | A logic low on this input selects the chip and the parallel data bus (DAL). |
| 4 | $\overline{\text{READ ENABLE}}$ | $\overline{\text{RE}}$ | A logic low on this input controls the placement of data from a selected register on DALØ-DAL7 when $\overline{\text{CS}}$ is low. |
| 5,6 | REGISTER SELECT LINES | A0, A1 | These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: |
| 7-14 | DATA ACCESS LINES | DAL0-DAL7 | Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{\text{WE}}$ or a transmitter enabled by $\overline{\text{RE}}$. The Data Bus is inverted on the FDC 1791, FDC 1792 and FDC 1795. |
| 24 | CLOCK | CLK | This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for 5¼" drives. |
| 38 | DATA REQUEST | DRQ | This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use a 10K pull-up resistor to +5V. |
| 39 | INTERRUPT REQUEST | INTRQ | This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V. |
| **FLOPPY DISK INTERFACE:** | | | |
| 15 | STEP | STEP | Step and direction motor control. The step output contains a pulse for each step. |
| 16 | DIRECTION | DIRC | Direction Output is active high when stepping in, active low when stepping out. |
| 17 | EARLY | EARLY | Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation. |
| 18 | LATE | LATE | Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation. |
| 22 | $\overline{\text{TEST}}$ | $\overline{\text{TEST}}$ | This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors. |
| 23 | HEAD LOAD TIMING | HLT | When a logic high is found on the HLT input the head is assumed to be engaged. |

| A1 | A0 | $\overline{\text{RE}}$ | $\overline{\text{WE}}$ |
|---|---|---|---|
| 0 | 0 | Status Reg | Command Reg |
| 0 | 1 | Track Reg | Track Reg |
| 1 | 0 | Sector Reg | Sector Reg |
| 1 | 1 | Data Reg | Data Reg |

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 25 | READ GATE (1791/3) | RG | A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization. |
| 25 | SIDE SELECT OUTPUT (1795, 1797) | SSO | The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S=1, SSO is set to a logic 1. When S=0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition. |
| 26 | READ CLOCK | RCLK | A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not. |
| 27 | $\overline{\text{RAW READ}}$ | $\overline{\text{RAW READ}}$ | The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition. |
| 28 | HEAD LOAD | HLD | The HLD output controls the loading of the Read-Write head against the media. |
| 29 | TRACK GREATER THAN 43 | TG43 | This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands. |
| 30 | WRITE GATE | WG | This output is made valid before writing is to be performed on the diskette. |
| 31 | WRITE DATA | WD | A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats. |
| 32 | READY | READY | This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7. |
| 33 | $\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$ | $\overline{\text{WF/VFOE}}$ | This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG=1, Pin 33 functions as a $\overline{\text{WF}}$ input. If $\overline{\text{WF}}$=0, any write command will immediately be terminated. When WG=0, Pin 33 functions as a $\overline{\text{VFOE}}$ output. $\overline{\text{VFOE}}$ will go low during a read operation after the head has loaded and settled (HLT=1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. $\overline{\text{VFOE}}$ will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, $\overline{\text{VFOE}}$ will remain low until the end of the Data Field. |
| 34 | $\overline{\text{TRACK 00}}$ | $\overline{\text{TR00}}$ | This input informs the FDC179X that the Read/Write head is positioned over Track 00. |
| 35 | $\overline{\text{INDEX PULSE}}$ | $\overline{\text{IP}}$ | This input informs the FDC179X when the index hole is encountered on the diskette. |
| 36 | $\overline{\text{WRITE PROTECT}}$ | $\overline{\text{WPRT}}$ | This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit. |
| 37 | $\overline{\text{DOUBLE DENSITY}}$ | $\overline{\text{DDEN}}$ | This pin selects either single or double density operation. When $\overline{\text{DDEN}}$=0, double density is selected. When $\overline{\text{DDEN}}$=1, single density is selected. This line must be left open on the 1792/4. |

## FUNCTIONAL DESCRIPTION

The FDC 179X-02 major functional blocks are as follows:

**Data Shift Register**—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register**—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Sector Register (SR)**—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)**—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)**—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

**CRC Logic**—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x)=x^{16}+x^{12}+x^5+1$.

**Track Register**—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)**—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control**—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

**AM Detector**—The address mark detector detects ID, data and index address marks during ready and write operations.



## OPERATION

FDC 1791, FDC 1793, FDC 1795 and FDC 1797 have two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}}=1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DDEN must be left open for the FDC 1792 and FDC 1794.

### Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FDC179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG=0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF/VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is

transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

**Disk Write Operation**

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution against erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FDC179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FDC179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FDC179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$=1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$=0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FDC179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

## COMMAND WORDS

The FDC179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**Table 1. Command Summary**

| | | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| COMMAND | TYPE | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Restore | I | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| Seek | I | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| Step | I | 0 | 0 | 1 | u | h | V | $r_1$ | $r_0$ |
| Step In | I | 0 | 1 | 0 | u | h | V | $r_1$ | $r_0$ |
| Step Out | I | 0 | 1 | 1 | u | h | V | $r_1$ | $r_0$ |
| Read Sector | II | 1 | 0 | 0 | m | $F_2$ | E | $F_1$ | 0 |
| Write Sector | II | 1 | 0 | 1 | m | $F_2$ | E | $F_1$ | $a_0$ |
| Read Address | III | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 |
| Read Track | III | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 |
| Write Track | III | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 |
| Force Interrupt | IV | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

### Type I Commands

The Type I Commands are Restore, Seek, Step, Step-In, and Step-Out. Each of the Type I Commands contains a rate field ($r_0r_1$), which determines the stepping motor rate as defined in Table 2.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FDC179X receives a command that specifically disengages the head. If the FDC179X is idle (busy=0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field if read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt

is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC179X terminates the operation and sends an interrupt (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

On the FDC 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

**Restore (Seek Track 0)**

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. if $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the $r_1r_0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FDC179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

**Seek**

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FDC179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step**

Upon receipt of this command, the FDC179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step-In**

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step-Out**

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of command. An interrupt is generated at the completion of the command.

**Head Positioning**

The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$=0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

**Step**—A 2 $\mu$s (MFM) or 4 $\mu$s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

**Direction (DIRC)**—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 $\mu$s before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FDC179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

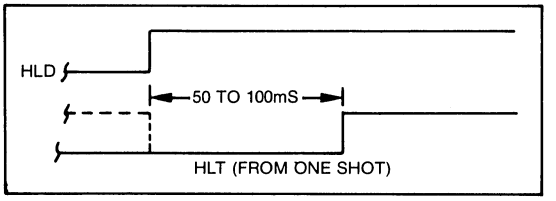
**Table 2. Stepping Rates**

| CLK: | | 2 MHz | 2 MHz | 1 MHz | 1 MHz | 2 MHz | 1 MHz |
|---|---|---|---|---|---|---|---|
| $\overline{DDEN}$: | | 0 | 1 | 0 | 1 | X | X |
| $r_1$ | $r_0$ | $\overline{TEST}$=1 | $\overline{TEST}$=1 | $\overline{TEST}$=1 | $\overline{TEST}$=↑ | $\overline{TEST}$=0 | $\overline{TEST}$=0 |
| 0 | 0 | 3 ms | 3 ms | 6 ms | 6 ms | 184$\mu$s | 368$\mu$s |
| 0 | 1 | 6 ms | 6 ms | 12 ms | 12 ms | 190$\mu$s | 380$\mu$s |
| 1 | 0 | 10 ms | 10 ms | 20 ms | 20 ms | 198$\mu$s | 396$\mu$s |
| 1 | 1 | 15 ms | 15 ms | 30 ms | 30 ms | 208$\mu$s | 416$\mu$s |

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h=1), at the end of the Type I command if the verify flag (V=1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h=0 and V=0); or if the FDC179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FDC179X which is used for the head engage time. When HLT=1, the FDC179X assumes the head is completely engaged.

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC179X.




**Head Load Timing**

When both HLD and HLT are true, the FDC179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

| TYPE I COMMANDS FLAG SUMMARY |
|---|
| h=Head Load Flag (Bit 3) |
| h=1, Load head at beginning<br>h=0, Unload head at beginning |
| V=Verify flag (Bit 2) |
| V=1, Verify on destination track<br>V=0, No verify |
| $r_1r_0$=Stepping motor rate (Bits 1-0) |
| Refer to Table 2 for rate summary |
| u=Update flag (Bit 4) |
| u=1, Update Track register<br>u=0, No update |

## Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag=1 (this is the normal case) HLD is made active and HLT is sampled until true after a 15 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC179X will read or write multiple records starting with the sector presently in the sector register. The FDC179X will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C=0, no side comparison is made. When C=1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The FDC1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

| Sector Length Table (1791/2/3/4 only) | |
|---|---|
| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |

**Field Format**

| GAP III | ID AM | TRACK NUMBER | SIDE NUMBER | SECTOR NUMBER | SECTOR LENGTH | CRC 1 | CRC 2 | GAP II | DATA AM | DATA FIELD | CRC 1 | CRC 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID FIELD | | | | | | | | | | DATA FIELD | | |

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

### Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

| STATUS BIT 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

### Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_0$ field of the command as shown below:

| $a_0$ | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The FDC179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

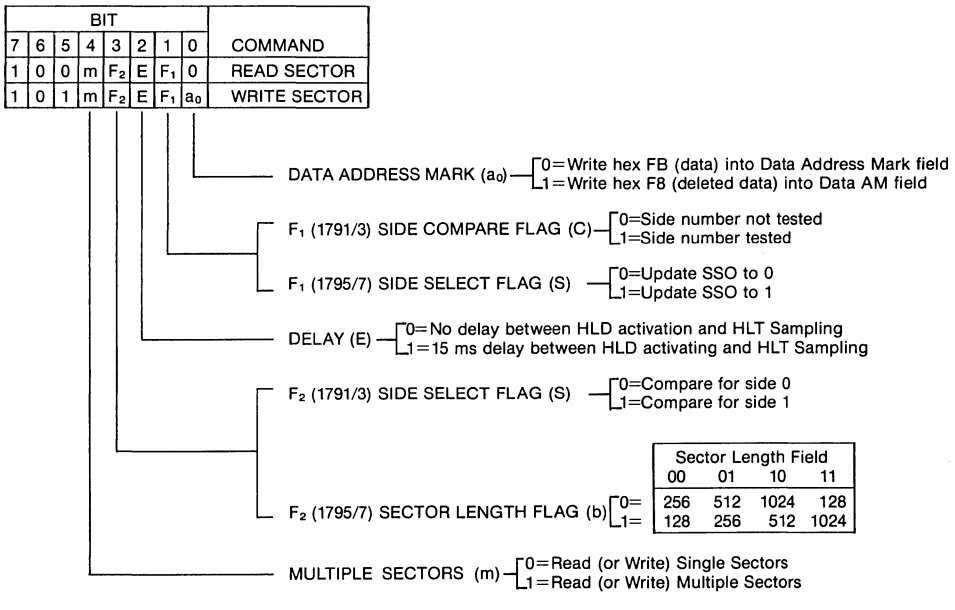



**Figure 1. Type II and III Flag Summary**

## Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

### Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDRESS | SECTOR LENGTH | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transferred to the computer, the FDC179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

### Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

### Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which

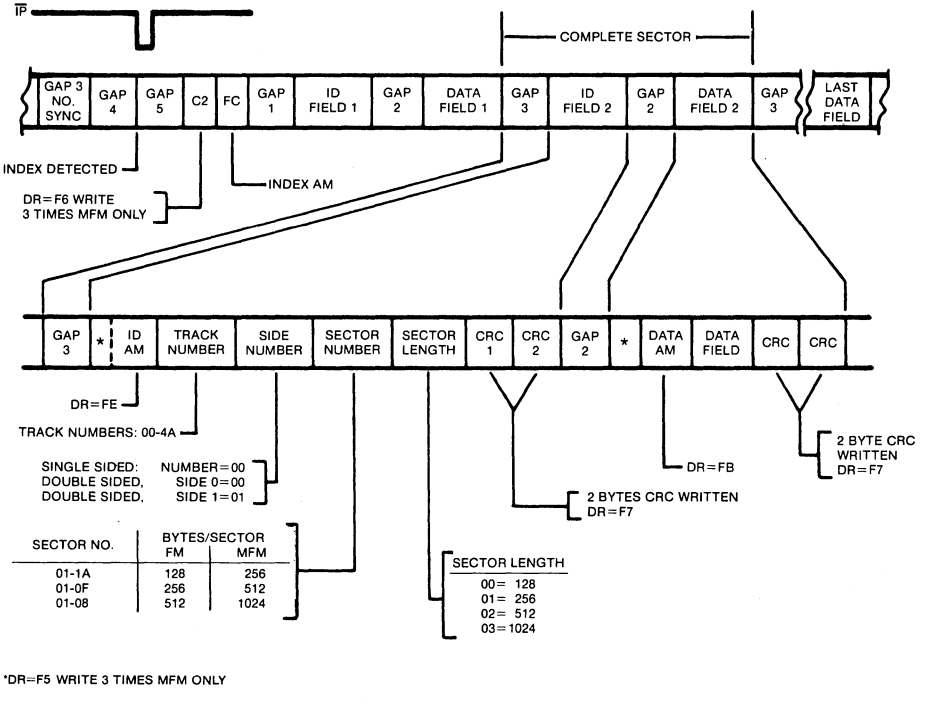



**Figure 2. IBM Compatible Sector/Track Format**

time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

## Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, $I_0$-$I_3$, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If $I_0$-$I_3$ are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for $I_3$=1 (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with $I_0$-$I_3$ all low.

### Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.



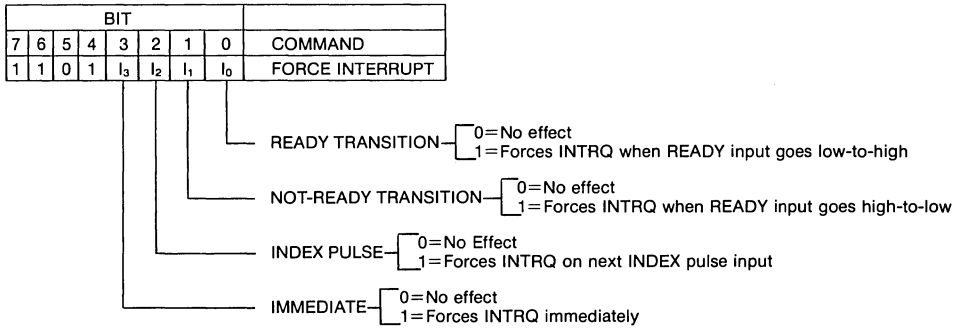



**Figure 3. Force Interrupt Command Flags**

## Figure 4A. Status Register Summary

| COMMAND | STATUS BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ALL TYPE I | Not Ready | Write Protect | Head Loaded | Seek Error | CRC Error | Track 0 | Index | Busy |
| READ SECTOR | Not Ready | 0 | Record Type | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| WRITE SECTOR | Not Ready | Write Protect | Write Fault | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| READ ADDRESS | Not Ready | 0 | 0 | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| READ TRACK | Not Ready | 0 | 0 | 0 | 0 | Lost Data | DRQ | Busy |
| WRITE TRACK | Not Ready | Write Protect | Write Fault | 0 | 0 | Lost Data | DRQ | Busy |

## Figure 4B. Status Description for Type I Commands

| BIT | NAME | MEANING |
|---|---|---|
| S7 | NOT READY | This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR. |
| S6 | PROTECTED | When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input. |
| S5 | HEAD LOADED | When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals. |
| S4 | SEEK ERROR | When set, the desired track was not verified. This bit is reset to 0 when updated. |
| S3 | CRC ERROR | CRC encountered in ID field. |
| S2 | TRACK 00 | When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input. |
| S1 | INDEX | When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input. |
| S0 | BUSY | When set command is in progress. When reset no command is in progress. |

## Figure 4C. Status Description for Type II and III Commands

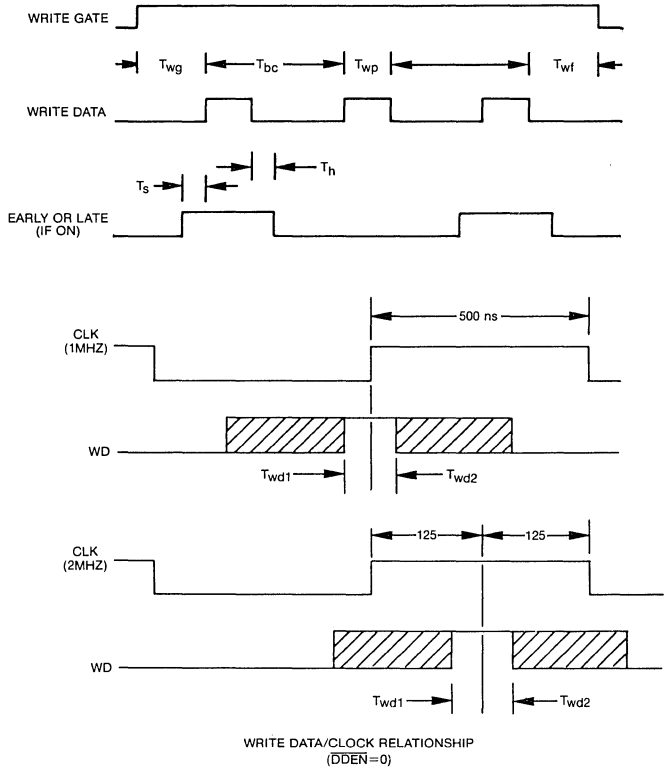
| BIT | NAME | MEANING |
|---|---|---|
| S7 | NOT READY | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready. |
| S6 | WRITE PROTECT | On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated. |
| S5 | RECORD TYPE/ WRITE FAULT | On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated. |
| S4 | RECORD NOT FOUND (RNF) | When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated. |
| S3 | CRC ERROR | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated. |
| S2 | LOST DATA | When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 | DATA REQUEST | This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. |
| S0 | BUSY | When set, command is under execution. When reset, no command is under execution. |

## Write Data Timing:

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| Write Data Pulse Width | $T_{wp}$ | 450 | 500 | 550 | nsec | FM |
| | | 150 | 200 | 250 | nsec | MFM |
| Write Gate to Write Data | $T_{wg}$ | | 2 | | $\mu$sec | FM |
| | | | 1 | | $\mu$sec | MFM |
| Write data cyle Time | $T_{bc}$ | | 2, 3, or 4 | | $\mu$sec | $\pm$CLK Error |
| Early (Late) to Write Data | $T_s$ | 125 | | | nsec | MFM |
| Early (Late) From Write Data | $T_h$ | 125 | | | nsec | MFM |
| Write Gate off from WD | $T_{wf}$ | | 2 | | $\mu$sec | FM |
| | | | 1 | | $\mu$sec | MFM |
| WD Valid to Clk | $T_{wd1}$ | 100 | | | nsec | CLK=1 MHZ |
| | | 50 | | | nsec | CLK=2 MHZ |
| WD Valid after Clk | $T_{wd2}$ | 100 | | | nsec | CLK=1 MHZ |
| | | 30 | | | nsec | CLK=2 MHZ |

These values are doubled when CLK=1 MHz.

### Write Data Timing




WRITE DATA/CLOCK RELATIONSHIP
($\overline{DDEN}$=0)

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, $V_{DD}$=+12V±5% unless otherwise noted)

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| Input Voltage Levels | | | | | | | |
| Low Level, $V_{IL}$ | | | | | 0.8 | V | |
| High Level, $V_{IH}$ | | | 2.6 | | | V | |
| Output Voltage Levels | | | | | | | |
| Low Level $V_{OL}$ | | | | | 0.45 | V | $I_{OL}$=1.6 mA |
| High Level $V_{OH}$ | | | 2.8 | | | V | $I_{OH}$=100 μA |
| Output Leakage, $I_{LO}$ | | | | | 10 | μA | $V_{OUT}=V_{DD}$ |
| Input Leakage, $I_{IL}$ | | | | | 10 | μA | $V_{IN}=V_{DD}$ |
| Output Capacitance | | | | 5 | | pf | |
| Input Capacitance | | | | 10 | | pf | |
| Power Dissipation | | | | | 500 | mW | |
| **AC CHARACTERISTICS** | | | | | | | |
| Processor Read Timing | | | | | | | |
| Address Setup Time | | $t_{SETR}$ | 50 | | | ns | Figure 5 |
| Address Hold Time | | $t_{HLDR}$ | 10 | | | ns | Figure 5 |
| $\overline{RE}$ Pulse Width ($C_L$=50pF) | | $t_{RE}$ | 400 | | | ns | Figure 5 |
| DRQ Reset Time | | $t_{DRR}$ | | | 500 | ns | Figure 5 |
| INTRQ Reset Time | | $t_{IRR}$ | | 500* | 3000* | ns | Figure 5 |
| Data Delay Time ($C_L$=50pF) | | $t_{DACC}$ | | | 350 | ns | Figure 5 |
| Data Hold Time ($C_L$=50pF) | | $t_{DOH}$ | 50 | | 150 | ns | Figure 5 |
| Microprocessor Write Timing | | | | | | | |
| Address Setup Time | | $t_{SETW}$ | 50 | | | ns | Figure 6 |
| Address Hold Time | | $t_{HLDW}$ | 10 | | | ns | Figure 6 |
| WE Pulse Width | | $t_{WE}$ | 350 | | | ns | Figure 6 |
| DRQ Reset Time | | $t_{DRR}$ | | | 500 | ns | Figure 6 |
| INTRQ Reset Time | | $t_{IRR}$ | | 500* | 3000* | ns | Figure 6 |
| Data Setup Time | | $t_{DS}$ | 250 | | | ns | Figure 6 |
| Data Hold Time | | $t_{DH}$ | 70 | | | ns | Figure 6 |
| Disk Input Data Timing | | | | | | | |
| RAWREAD Pulse Width | | $t_{pw}$ | 100* | 200 | | ns | Figure 7, See Note |
| Clock Setup Time | | $t_d$ | 40 | | | ns | Figure 7 See Note |
| Clock Hold Time for MFM | | $t_{cd}$ | 40 | | | ns | Figure 7 |
| Clock Hold Time for FM | | $t_{cs}$ | 40 | | | ns | Figure 7 |
| RAWREAD Cycle Time | | $t_{bc}$ | 1500 | | | ns | 1800 at 70°C, Figure 7 |
| RCLK High Pulse Width | MFM | $t_a$ | 0.8 | 1* | | μs | Figure 7 |
| | FM | | 0.8 | 2* | | μs | Figure 7 |
| RCLK Low Pulse Width | MFM | $t_b$ | 0.8 | 1* | | μs | Figure 7 |
| | FM | | 0.8 | 2* | | μs | Figure 7 |
| RCLK Cycle Time | MFM | $t_c$ | | 2* | | μs | Figure 7 |
| | FM | | | 4* | | μs | Figure 7 |
| Miscellaneous Timing | | | | | | | |
| CLK Low Pulse Width | | $t_{CD1}$ | 230 | 250 | 20000 | ns | Figure 8 |
| CLK High Pulse Width | | $t_{CD2}$ | 200 | 250 | 20000 | ns | Figure 8 |
| STEP Pulse Width | MFM | $t_{STP}$ | 2* | | | μs | Figure 8 |
| | FM | | 4* | | | μs | Figure 8 |
| DIRC Setup Time | | $t_{DIR}$ | | 12 | | μs | Figure 8 |
| MR Pulse Width | | $t_{MR}$ | 50* | | | μs | Figure 8 |
| IP Pulse Width | | $t_{IP}$ | 10* | | | μs | Figure 8 |
| WF Pulse Width | | $t_{WF}$ | 10* | | | μs | Figure 8 |
| CLK Cycle Time | | $t_{CYC}$ | | 0.5* | | μs | Figure 8 |

*: These Values are doubled when CLK=1 MHz.

**Figure 5. Microprocessor Read Timing**

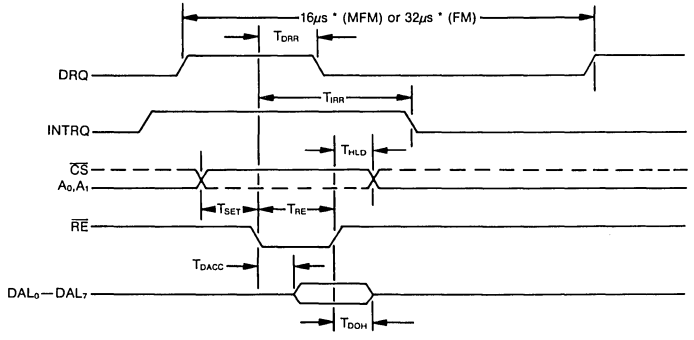



**Figure 6. Microprocessor Write Timing**

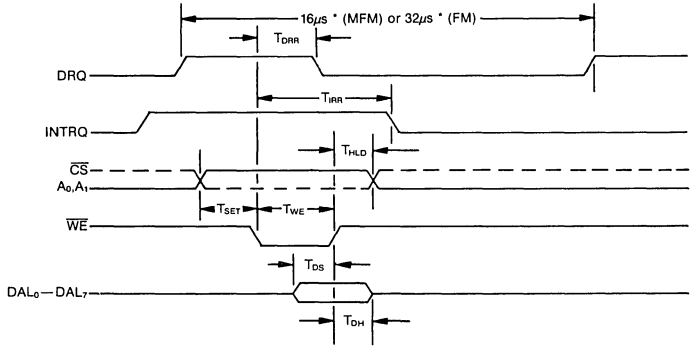
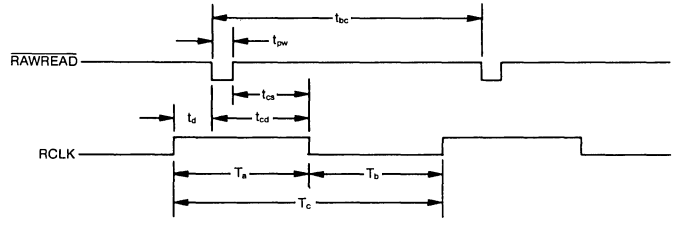
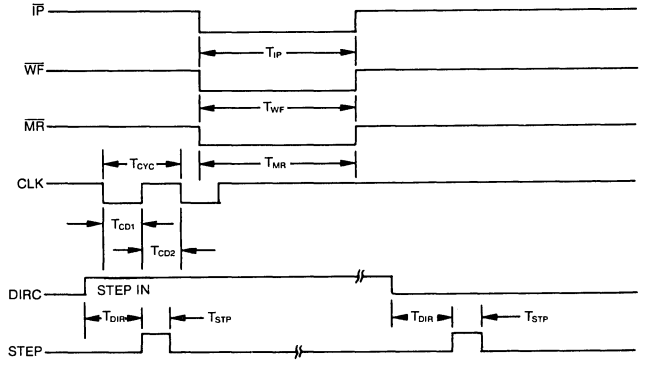



**Figure 7. Disk Input Timing**




Note: Pulse width on RAW READ (Pin 27) is normally 10-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK=2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.

**Figure 8. Miscellaneous Timing**



# DISK FORMATS

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

### IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

### IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

### Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11.

| | DATA BYTE (hex) | NO. OF BYTES | COMMENTS |
|---|---|---|---|
| | FF | 40 | Gap 5 (Post Index) |
| | 00 | 6 | |
| | FC | 1 | Index AM |
| | FF | 26 | Gap 1 |
| | 00 | 6 | |
| ONE SECTOR ① | FE | 1 | ID AM |
| | XX | 1 | Track Number (00-4C) |
| | 0X | 1 | Side Number (00 or 01) |
| | XX | 1 | Sector Number (01-1A) |
| | 00 | 1 | Sector Length (128 bytes) |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | FF | 11 | Gap 2 (ID Gap) |
| | 00 | 6 | |
| | FB | 1 | Data AM |
| | E5 | 128 | Data Field |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | FF | 27 | Part of Gap 3 (Data Gap) |
| | FF | 247 ② | Gap 4 (Pre Index) |

**Figure 9. Byte Sequence for IBM 3740 Formatting**

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

| | DATA BYTE (hex) | NO. OF BYTES | COMMENTS |
|---|---|---|---|
| | 4E | 80 | Gap 5 (Post Index) |
| | 00 | 12 | |
| | F6 | 3 | Writes C2 |
| | FC | 1 | Index AM |
| | 4E | 50 | |
| | 00 | 12 | Gap 1 |
| | F5 | 3 | Writes A1 |
| | FE | 1 | ID AM |
| | XX | 1 | Track Number (00-4C) |
| ONE SECTOR ① | 0X | 1 | Side Number (00 or 01) |
| | XX | 1 | Sector Number (01-1A) |
| | 01 | 1 | Sector Length (256 Bytes) |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | 4E | 22 | Gap 2 (ID Gap) |
| | 00 | 12 | |
| | F5 | 3 | Writes A1 |
| | FB | 1 | Data AM |
| | 40 | 256 | Data Field |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | 4E | 54 | Part of Gap 3 (Data Gap) |
| | 4E | 598 ② | Gap 4 (Pre Index) |

**Figure 10. Byte Sequence for IBM System-34 Formatting**

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

| GAP | SINGLE DENSITY (FM) | DOUBLE DENSITY (MFM) | NOTE |
|---|---|---|---|
| Gap 1 | 16 bytes FF | 16 bytes 4E | 2 |
| Gap 2 | 11 bytes FF<br>6 bytes 00 | 22 bytes 4F<br>12 bytes 00<br>3 bytes A1 | 1 |
| Gap 3 | 10 bytes FF<br>4 bytes 00 | 16 bytes 4E<br>8 bytes 00<br>3 bytes A1 | 2 |
| Gap 4 | 16 bytes FF | 16 bytes 4E | 2 |

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

**Figure 11. Gap Size Limitations**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

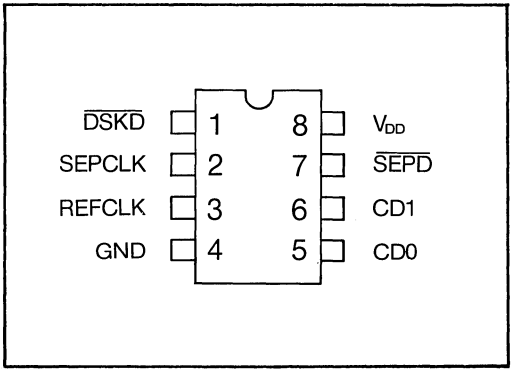
# FDC 9216
# FDC 9216B
## μPC FAMILY

# Floppy Disk Data Separator
# FDDS

### FEATURES

- ☐ PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- ☐ SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ☐ ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- ☐ NO CRITICAL ADJUSTMENTS REQUIRED
- ☐ COMPATIBLE WITH STANDARD MICROSYSTEMS' FDC 1791, FDC 1793 AND OTHER FLOPPY DISK CONTROLLERS
- ☐ SMALL 8-PIN DUAL-IN-LINE PACKAGE
- ☐ +5 VOLT ONLY POWER SUPPLY
- ☐ TTL COMPATIBLE INPUTS AND OUTPUTS

### PIN CONFIGURATION

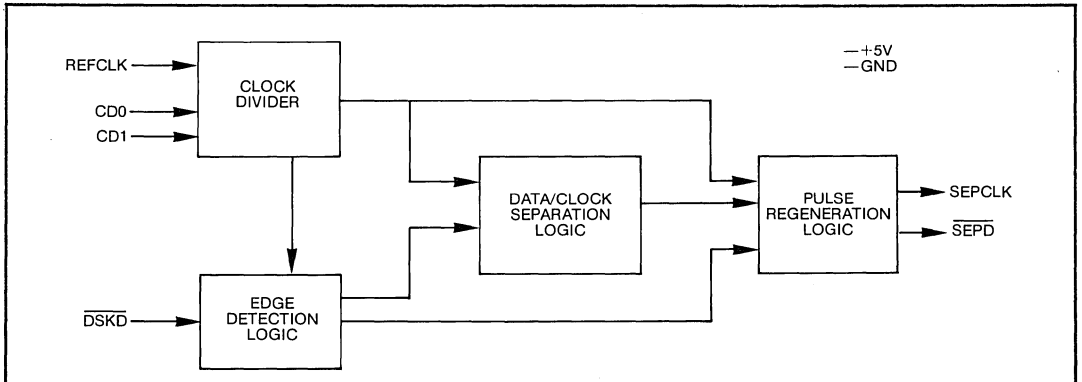



### GENERAL DESCRIPTION

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The FDC 9216 is available in two versions; the FDC 9216, which is intended for 5¼" disks and the FDC 9216B for 5¼" and 8" disks.




FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

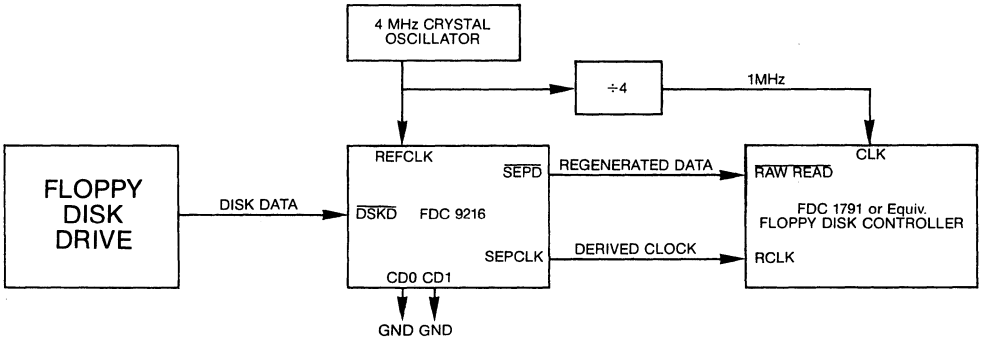
SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | $\overline{\text{Disk Data}}$ | $\overline{\text{DSKD}}$ | Data input signal direct from disk drive. Contains combined clock and data waveform. |
| 2 | Separated Clock | SEPCLK | Clock signal output from the FDDS derived from floppy disk drive serial bit stream. |
| 3 | Reference Clock | REFCLK | Reference clock input |
| 4 | Ground | GND | Ground |
| 5, 6 | Clock Divisor | CD0, CD1 | CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: |
| 7 | $\overline{\text{Separated Data}}$ | $\overline{\text{SEPD}}$ | SEPD is the data output of the FDDS |
| 8 | Power Supply | $V_{DD}$ | +5 volt power supply |

| CD1 | CD0 | Divisor |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 8 |

FIGURE 1
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



## OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

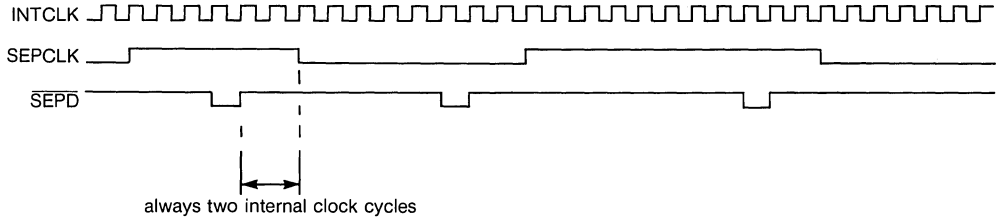
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

**TABLE 1:**
**CLOCK DIVIDER SELECTION TABLE**

| DRIVE (8" or 5¼") | DENSITY (DD or SD) | REFCLK MHz | CD1 | CD0 | REMARKS |
|---|---|---|---|---|---|
| 8 | DD | 8 | 0 | 0 | |
| 8 | SD | 8 | 0 | 1 | Select either one |
| 8 | SD | 4 | 0 | 0 | |
| 5¼ | DD | 8 | 0 | 1 | Select either one |
| 5¼ | DD | 4 | 0 | 0 | |
| 5¼ | SD | 8 | 1 | 0 | |
| 5¼ | SD | 4 | 0 | 1 | Select any one |
| 5¼ | SD | 2 | 0 | 0 | |

FIGURE 2



## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

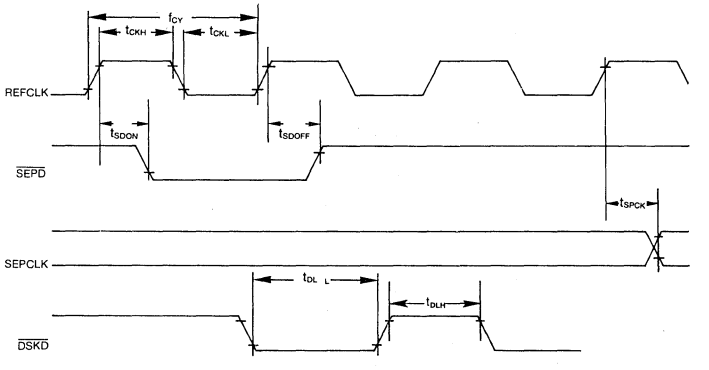
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A$ =0°C to 70°C, $V_{DD}$=+5V±5%, unless otherwise noted)

| Parameter | | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | | |
| INPUT VOLTAGE LEVELS | | | | | | |
| Low Level $V_{IL}$ | | | | 0.8 | V | |
| High Level $V_{IH}$ | | 2.0 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | | |
| Low Level $V_{OL}$ | | | | 0.4 | V | $I_{OL}$=1.6mA |
| High Level $V_{OH}$ | | 2.4 | | | V | $I_{OH}$=−100 μA |
| INPUT CURRENT | | | | | | |
| Leakage $I_{IL}$ | | | | 10 | μA | $0 \le V_{IN} \le V_{DD}$ |
| INPUT CAPACITANCE | | | | | | |
| All Inputs | | | | 10 | pF | |
| POWER SUPPLY CURRENT | | | | | | |
| $I_{DD}$ | | | | 60 | mA | |
| **A.C. CHARACTERISTICS** | | | | | | |
| **Symbol** | | | | | | |
| $f_{cy}$ | REFCLK Frequency | 0.2 | | 4.3 | MHz | FDC 9216 |
| $f_{cy}$ | REFCLK Frequency | 0.2 | | 8.3 | MHz | FDC 9216B |
| $t_{CKH}$ | REFCLK High Time | 50 | | 2500 | ns | |
| $t_{CKL}$ | REFCLK Low Time | 50 | | 2500 | ns | |
| $t_{SDON}$ | REFCLK to $\overline{SEPD}$ "ON" Delay | 25 | 100 | 250 | ns | |
| $t_{SDOFF}$ | REFCLK to $\overline{SEPD}$ "OFF" Delay | 25 | 100 | 250 | ns | |
| $t_{SPCK}$ | REFCLK to SEPCLK Delay | 35 | | | ns | |
| $t_{DLL}$ | DSKD Active Low Time | 0.1 | | 100 | μs | |
| $t_{DLH}$ | DSKD Active High Time | 0.2 | | 100 | μs | |

FIGURE 3: AC CHARACTERISTICS



STANDARD MICROSYSTEMS CORPORATION

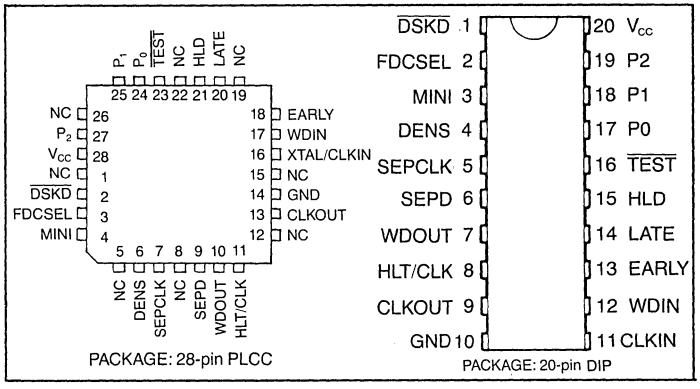
# FDC 9229T
# FDC 9229BT

# FLOPPY DISK INTERFACE CIRCUIT

## FEATURES

- ☐ Digital Data Separator
  Performs complete data separation function for floppy disk drives
  Separates FM and MFM encoded data
  No critical adjustments necessary
  5¼" and 8" compatible
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator Circuit
- ☐ Track-Selectable Write Precompensation
- ☐ Retriggerable Head-Load Timer
- ☐ Compatible with the FDC 179X, 765, and other standard Floppy Disk Controllers
- ☐ COPLAMOS® n-channel MOS Technology
- ☐ Single +5 Volt Supply
- ☐ TTL Compatible

## PIN CONFIGURATION




PACKAGE: 28-pin PLCC

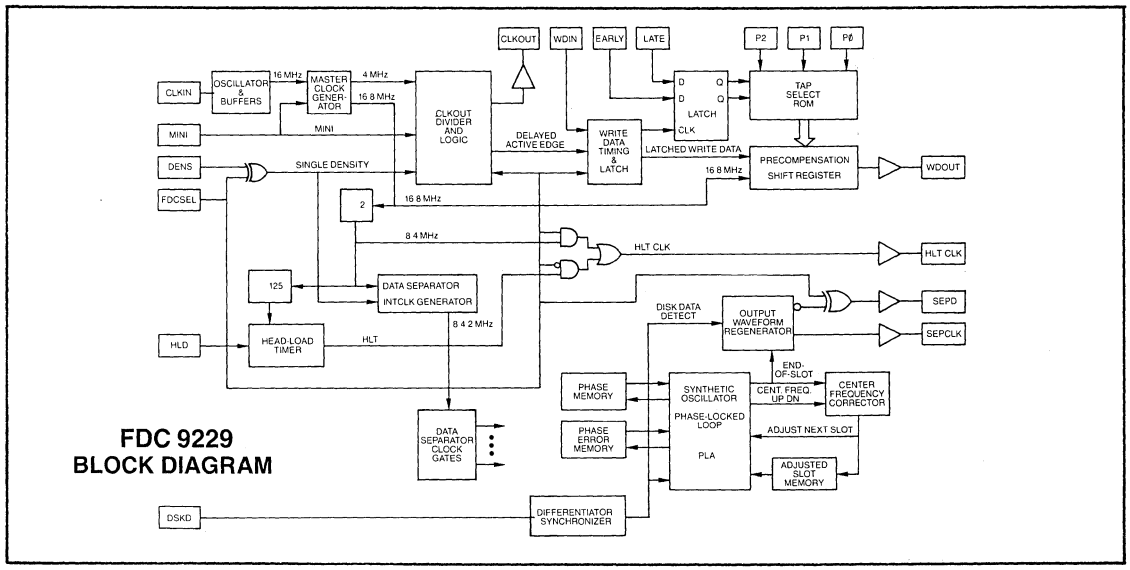
PACKAGE: 20-pin DIP

## FUNCTIONAL DESCRIPTION

The FDC 9229 is an MOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9229 provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9229 operates from a + 5V supply and simply requires that a TTL-level clock be connected to the CLKIN pin. All inputs and outputs are TTL compatible.

The FDC 9229 is available in two versions: The FDC 9229/T are intended for 5¼" drives and the FDC 9229B/T for 5¼" and 8" drives.

SECTION VI




**FDC 9229 BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $\overline{DSKD}$ | I | This input is the raw read data received from the drive. (This input is active low.) |
| 2 | FDCSEL | I | This input signal, when low, programs the FDC 9229 for a 179X type of LSI controller. When FDCSEL is high, the FDC 9229 is programmed for a 765 (8272) type of controller. (See fig. 4.) |
| 3 | MINI | I | The state of this input determines whether the FDC 9229 is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). (See figs. 2, 3, and 4.) |
| 4 | DENS | I | The state of this input determines whether the FDC 9229 is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.) |
| 5 | SEPCLK | O | A square-wave window clock signal output derived from the $\overline{DSKD}$ input. |
| 6 | SEPD | O | This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). This signal may be either active low or active high as determined by FDCSEL (pin 2). |
| 7 | WDOUT | O | The precompensated WRITE DATA stream to the drive. |
| 8 | HLT/CLK | O | When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.) |
| 9 | CLKOUT | O | This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.) |
| 10 | GND | | Ground |
| 11 | CLKIN | I | This input is for direct connection to a 16 MHz or 8 MHz single-phase TTL-level clock. |
| 12 | WDIN | I | The write data stream from the floppy disk controller. |
| 13 | EARLY | I | When this input is high, the current WRITE DATA pulse will be written early to the disk. |
| 14 | LATE | I | When this input is high, the current WRITE DATA pulse will be written late to the disk.<br>When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position. |
| 15 | HLD | I | This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.) |
| 16 | $\overline{TEST}$ | I | This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation. |
| 17 | P0 | I | P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.) |
| 18 | P1 | I | |
| 19 | P2 | I | |
| 20 | $V_{CC}$ | | +5 VOLT SUPPLY |

## Data Separator

The CLKIN input clock is internally divided by the FDC 9229 to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

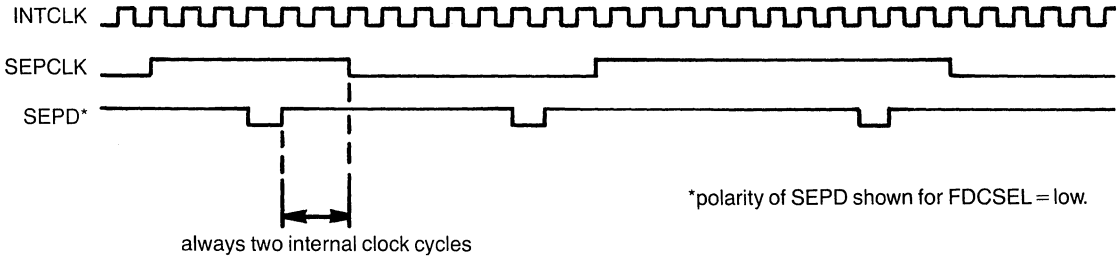
The FDC 9229 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

| INPUTS | | | DIVISOR |
|---|---|---|---|
| FDCSEL | DENS | MINI | f(CLKIN)/f(INTCLK) |
| 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 4 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 8 |
| 1 | 1 | 0 | 2 |
| 1 | 1 | 1 | 4 |

**FIG. 1**




## Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9229 as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

| MINI | P2 | P1 | P0 | PRECOMP VALUE |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 ns |
| 0 | 0 | 0 | 1 | 62.5 ns |
| 0 | 0 | 1 | 0 | 125 ns |
| 0 | 0 | 1 | 1 | 187.5 ns |
| 0 | 1 | 0 | 0 | 250 ns |
| 0 | 1 | 0 | 1 | 250 ns |
| 0 | 1 | 1 | 0 | 312.5 ns |
| 0 | 1 | 1 | 1 | 312.5 ns |
| 1 | 0 | 0 | 0 | 0 ns |
| 1 | 0 | 0 | 1 | 125 ns |
| 1 | 0 | 1 | 0 | 250 ns |
| 1 | 0 | 1 | 1 | 375 ns |
| 1 | 1 | 0 | 0 | 500 ns |
| 1 | 1 | 0 | 1 | 500 ns |
| 1 | 1 | 1 | 0 | 625 ns |
| 1 | 1 | 1 | 1 | 625 ns |

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

**FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION**

### Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9229 goes high before starting a read or write operation.

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| FDCSEL | DENS | MINI | CLKOUT | HLT/CLK |
| 0 | 0 | 0 | 2 MHz | 40 ms* |
| 0 | 0 | 1 | 1 MHz | 80 ms* |
| 0 | 1 | 0 | 2 MHz | 40 ms* |
| 0 | 1 | 1 | 1 MHz | 80 ms* |
| 1 | 0 | 0 | 500 KHz | 8 MHz |
| 1 | 0 | 1 | 250 KHz | 4 MHz |
| 1 | 1 | 0 | 1 MHz | 8 MHz |
| 1 | 1 | 1 | 500 KHz | 4 MHz |

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

*May be mask programmed at factory to any value from 1 to 512 ms in 15.625 μs increments (MINI low) or 1 to 1024 ms in 31.25 μs increments (MINI high).

**FIG. 3 CLOCK AND HEAD LOAD TIME DELAY SELECTION**

| INPUTS | | | FLOPPY DISK DRIVE TYPE | FLOPPY DISK DRIVE DENSITY | FLOPPY DISK CONTROLLER TYPE |
|---|---|---|---|---|---|
| FDCSEL | DENS | MINI | | | |
| 0 | 0 | 0 | 8" DRIVE | DOUBLE | 179X |
| 0 | 0 | 1 | 5¼" DRIVE | DOUBLE | 179X |
| 0 | 1 | 0 | 8" DRIVE | SINGLE | 179X |
| 0 | 1 | 1 | 5¼" DRIVE | SINGLE | 179X |
| 1 | 0 | 0 | 8" DRIVE | SINGLE | 765 (8272) |
| 1 | 0 | 1 | 5¼" DRIVE | SINGLE | 765 (8272) |
| 1 | 1 | 0 | 8" DRIVE | DOUBLE | 765 (8272) |
| 1 | 1 | 1 | 5¼" DRIVE | DOUBLE | 765 (8272) |

**FIG. 4 FLOPPY DISK DRIVE AND CONTROLLER SELECTION**

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +8.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Power Dissipation ..... 0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE | | | | | |
| Low Level $V_{IL}$ | −0.3 | | 0.8 | V | Except CLKIN |
| High Level $V_{IH}$ | 2.0 | | ($V_{CC}$) | V | |
| CLKIN INPUT VOLTAGE | | | | | |
| Low Level | −0.3 | | 0.8 | V | |
| High Level | 2.4 | | ($V_{CC}$) | V | |
| OUTPUT VOLTAGE | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA except HLT/CLK |
| | | | | | $I_{OL}$ = 0.4 mA, HLT/CLK only |
| High Level $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −100 µA except HLT/CLK |
| | | | | | $I_{OH}$ = −400 µA, HLT/CLK only |
| POWER SUPPLY CURRENT | | | | | |
| $I_{cc}$ | | | 100 | mA | |
| INPUT LEAKAGE CURRENT | | | | | |
| $I_{IL}$ | | | 10 | µA | $V_{IN}$ = 0 to $V_{CC}$ |
| INPUT CAPACITANCE | | | 10 | pF | Except CLKIN |
| $C_{IN}$ | | | 25 | pF | CLKIN only |

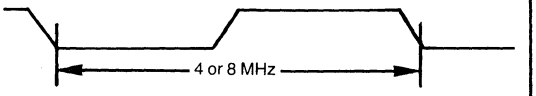
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 5%

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| **AC ELECTRICAL CHARACTERISTICS** | All times assume CLKIN = 16 MHz unless otherwise specified) | | | | |
| CLKIN frequency | 3.95 | 16 | 16.2 | MHz | FDC 9229B |
| | 3.95 | 8 | 8.1 | MHz | FDC 9229 |
| CLKIN DUTY CYCLE | 25 | | 75 | % | |
| $t_{clkoh}$ | 465 | 500 | 515 | ns | FDCSEL = low; MINI = high. |
| | 215 | 250 | 265 | ns | FDCSEL = low; MINI = low. |
| | 90 | 125 | 140 | ns | FDCSEL = high. |
| $t_{wdo}$ | 280 | 312.5 | 350 | ns | Time Doubles with MINI = 1 |
| $t_d$ | 50 | | 400 | ns | |
| $t_{dNEC}$ | 0 | | 400 | ns | |
| $t_{wdE}$ | 500 | 562.5 | 625 | ns | 9 clock times ± 1 clock time |
| $t_{wdN}$ | | precomp value | | | See fig. 2 |
| $t_{wdL}$ | | 2x precomp value | | | See fig. 2 |
| $t_s$ | 1.0 | | | µs | |

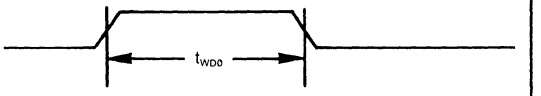
SECTION VI

# AC TIMING CHARACTERISTICS

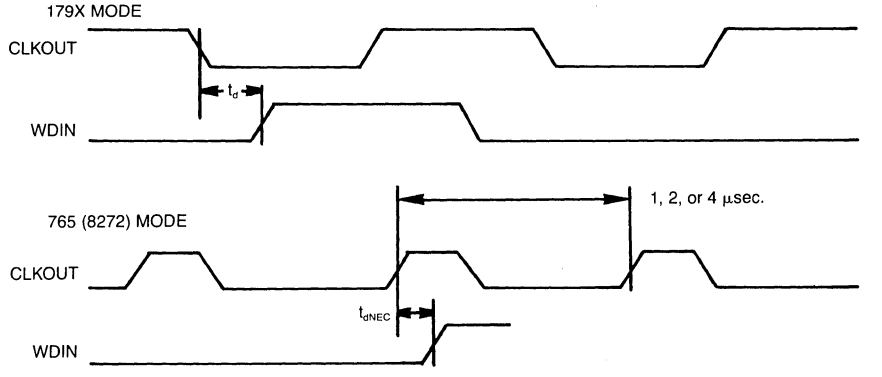
## HLT/CLK (765 MODE)



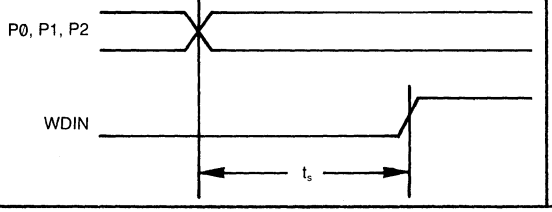

## WDOUT PULSE WIDTH



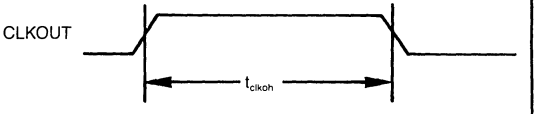

## CLKOUT VS. WDIN TIMING

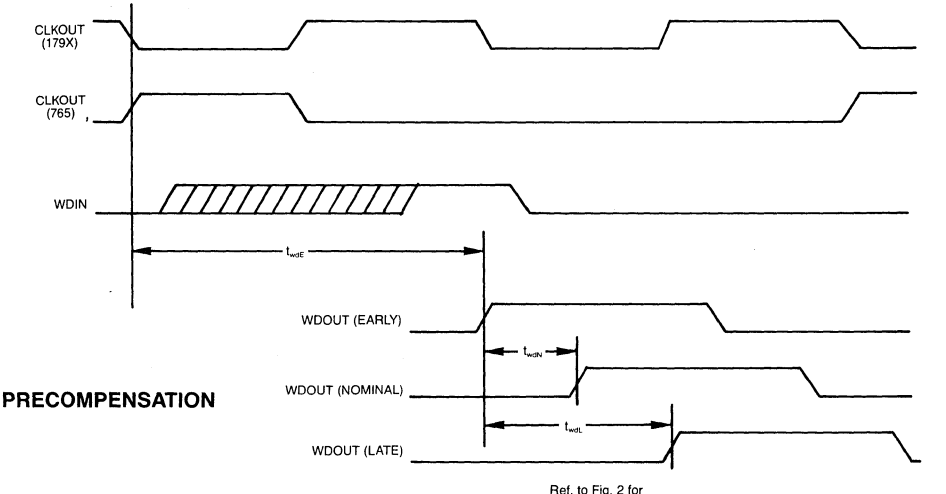



## SET-UP TIME PØ, P1 AND P2 TO WDIN




## CLKOUT

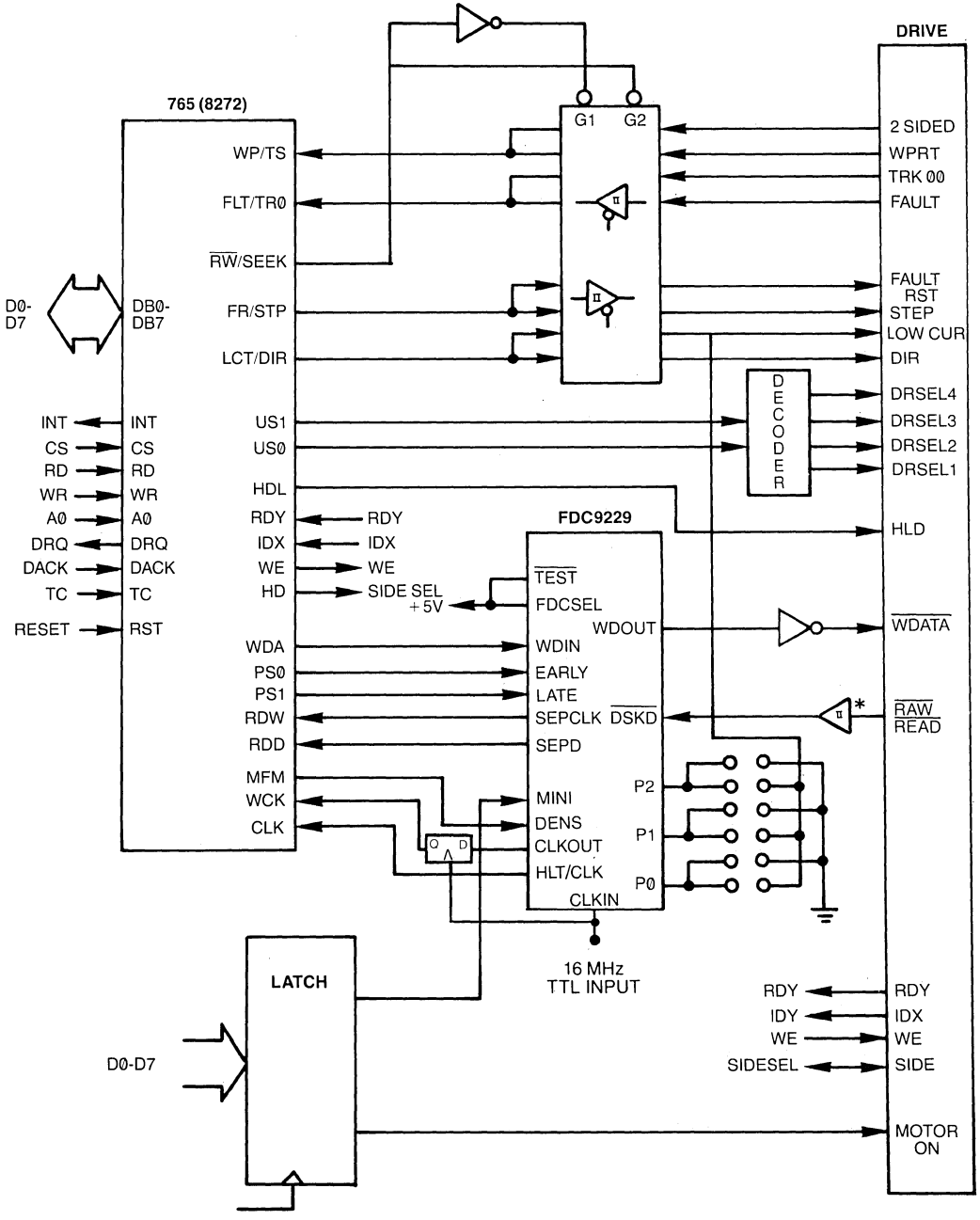



**PRECOMPENSATION**

Ref. to Fig. 2 for $t_p$ (precompensation) value

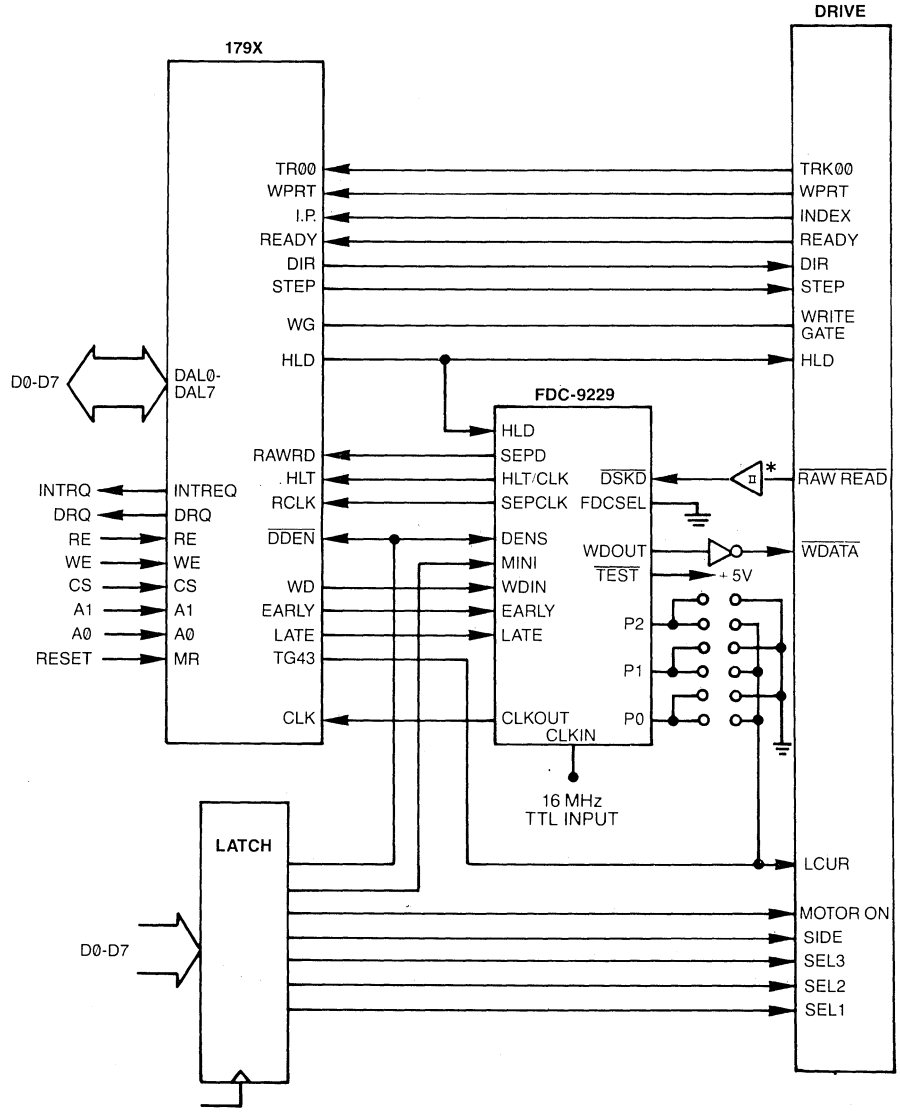
## TYPICAL SYSTEM IMPLEMENTATION—765 (8272) FDC




*The FDC9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

## TYPICAL SYSTEM IMPLEMENTATION—179X FDC




*The FDC9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

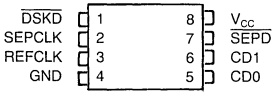
# FDC92C36
PRELIMINARY

# CMOS Floppy Disk Data Separator

## FEATURES

- ☐ High Performance Digital Data Separator
- ☐ Pin Replacement for FDC9216
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Single +5 Volt Supply
- ☐ Fully TTL compatible
- ☐ Fabricated in power saving CMOS
- ☐ Compatible with 3.5″, 5.25″ and 8″ drives and data rates up to 500 KBs
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs

## PIN CONFIGURATION




PACKAGE: 8-pin DIP

SECTION VI

## FUNCTIONAL DESCRIPTION

The FDC 92C36 is a CMOS integrated circuit. It incorporates a high performance, synthetic phase locked loop digital data separator in one 0.3 inch wide 8 pin package.

The use of a high performance synthetic phase locked loop allows the system designer to replace a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC 92C36 is available in two versions: the FDC 92C36 are intended for 5 1/4″ drives using data rates of 250KBs and the FDC 92C36B for 3 1/2″, 5 1/4″, and 8″ drives using data rates of 500KBs.

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | $\overline{\text{Disk Data}}$ | $\overline{\text{DSKD}}$ | Data input signal direct from disk drive. Contains combined clock and data waveform. |
| 2 | Separated Clock | SEPCLK | Clock signal output from the FDDS derived from floppy disk drive serial bit stream. |
| 3 | Reference Clock | REFCLK | Reference clock input |
| 4 | Ground | GND | Ground |
| 5,6 | Clock Divisor | CD0, CD1 | CD0 and CD1 control the internal clock divider circuit. Refer to Table 1. |
| 7 | $\overline{\text{Separated Data}}$ | $\overline{\text{SEPD}}$ | $\overline{\text{SEPD}}$ is the data output of the FDDS |
| 8 | Power Supply | $V_{DD}$ | +5 volt power supply |

## OPERATION

A reference clock (REFCLK) of 8 or 16 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/32 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 16 to a minimum of 12 and a maximum of 21 internal clock cycles.

**TABLE 1**

| CD1 | CD0 | 8MHz REFCLK | 16MHz REFCLK | DIVISOR f(REFCLK)/f(INTCLK) |
|---|---|---|---|---|
| 0 | 0 | not used | 5 1/4" SD | 4 |
| 0 | 1 | 8" SD<br>5 1/4" DD | 8" DD | 1 |
| 1 | 0 | 5 1/4" SD | 8" SD<br>5 1/4" DD | 2 |
| 1 | 1 | Illegal | Illegal | Illegal |

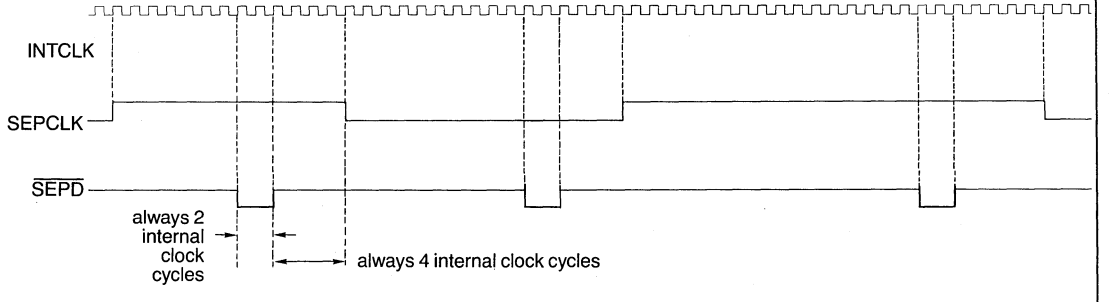



**FIGURE 2**

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.3V
Power Dissipation ..... 0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to 70°C, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

| Parameter | SYMBOL | Min. | Typ. | Max. | Units | Comm... |
|---|---|---|---|---|---|---|
| **D.C. CHARACTERISTICS** | | | | | | |
| INPUT VOLTAGE LEVELS | | | | | | |
| Low Level $V_{IL}$ | | | | 0.8 | V | |
| High Level $V_{IH}$ | | 2.0 | | | V | |
| OUTPUT VOLTAGE LEVELS | | | | | | |
| Low Level $V_{OL}$ | | | | 0.4 | V | $I_{OL} = 1.6mA$ |
| High Level $V_{OH}$ | | 2.4 | | | V | $I_{OH} = -100\ \mu A$ |
| INPUT CURRENT | | | | | | |
| Leakage $I_{IL}$ | | | | 10 | µA | $0 < V_{IN} < V_{DD}$ |
| INPUT CAPACITANCE | | | | | | |
| All Inputs | | | | 10 | pF | |
| POWER SUPPLY CURRENT | | | | | | |
| $I_{DD}$ | | | | TBD | mA | |
| **A.C. CHARACTERISTICS** | | | | | | |
| **Symbol** | | | | | | |
| REFCLK Frequency | $f_{cy}$ | 1.0 | 8.0 | 8.1 | MHz | FDC 92C36 |
| REFCLK Frequency | $f_{cy}$ | 1.0 | 16.0 | 16.2. | MHz | FDC 92C36B |
| $\overline{DSKD}$ Active Low Time | $t_{DLL}$ | 50 | | 100 | ns | |

SECTION VI

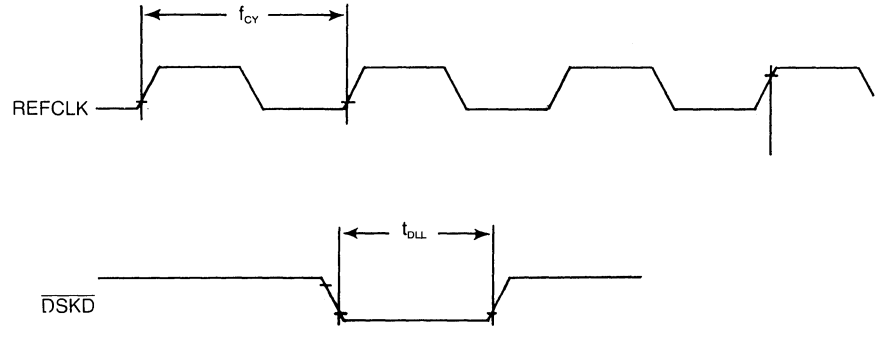
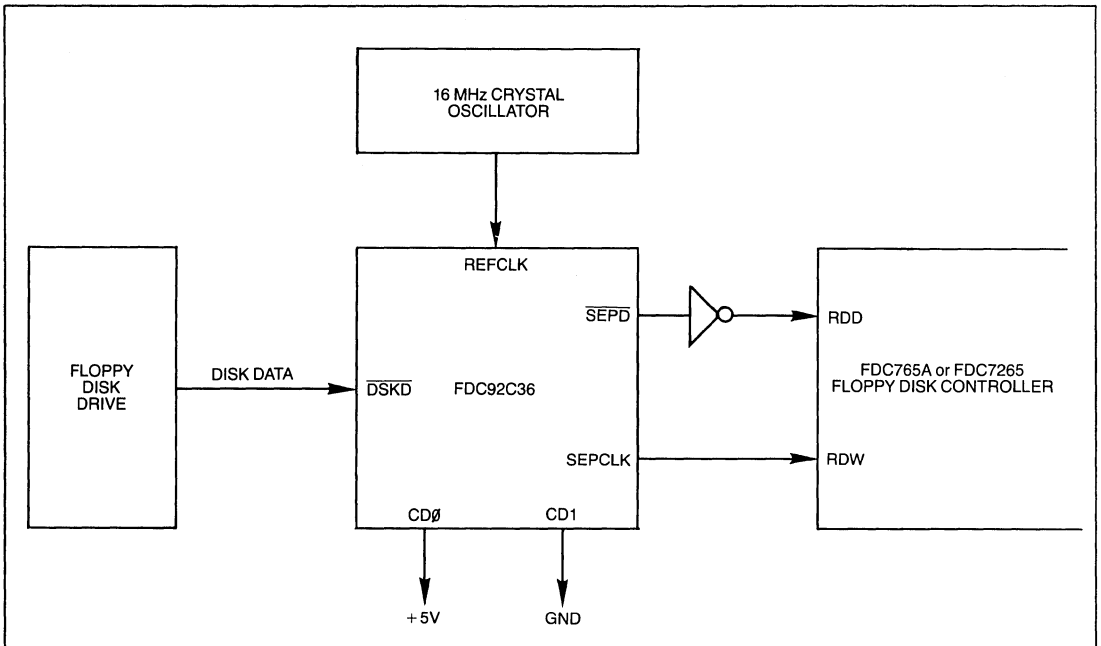



**FIGURE 3: AC CHARACTERISTICS**




**TYPICAL SYSTEM CONFIGURATION**
**(5¼" Drive, Double Density)**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516)273 3100 TWX 510 227 8698

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# FDC 9238/9238B
# FDC 9238T/9238BT

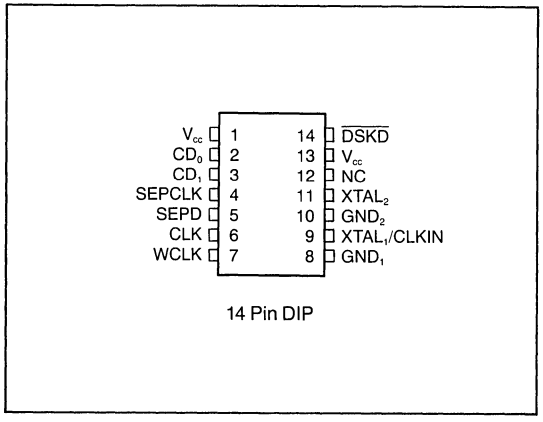
**PRELIMINARY**

# CMOS Floppy Disk Data Separator and Clock Generator

## FEATURES

- ☐ High Performance Digital Data Separator with Synthetic Oscillator and Phase Lock Loop for industry standard FDC 765A and FDC 7265
- ☐ Performs complete data separation function for floppy disk drives
- ☐ Eliminates all adjustments normally associated with high performance data separators
- ☐ Compatible with 3.5", 5.25" and 8" drives and data rates up to 500 KBs
- ☐ Internal Crystal Oscillator Circuit provides all clocks required by FDC 765A and FDC 7265
- ☐ Fabricated in power saving CMOS
- ☐ 16-Bit half Cell Divide Algorithm greatly improves performance over conventional digital designs
- ☐ Single +5 Volt supply
- ☐ Fully TTL compatible

## PIN CONFIGURATION




14 Pin DIP

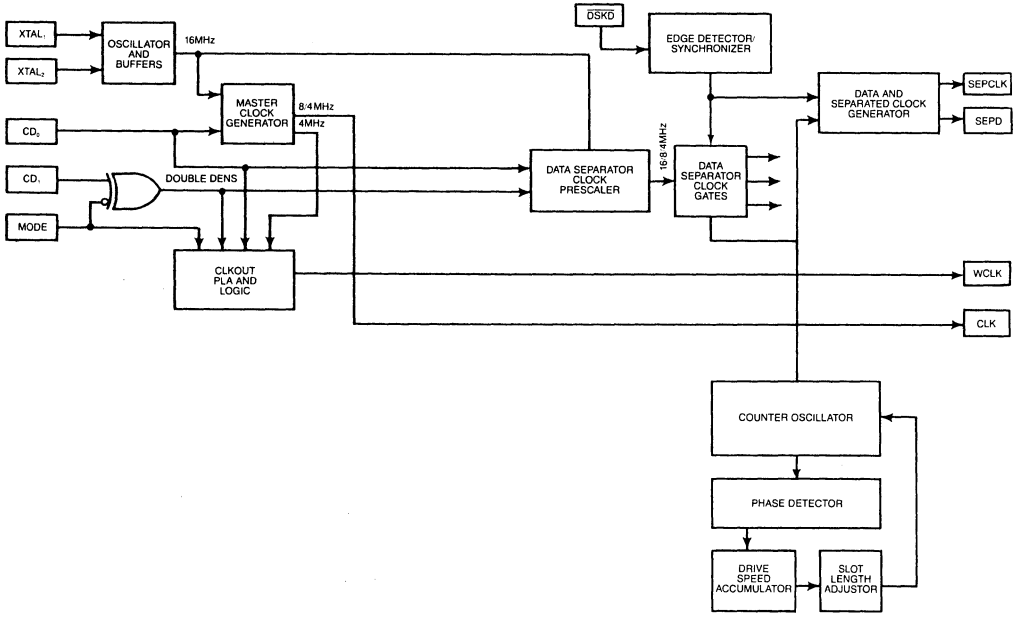
SECTION VI

## FUNCTIONAL DESCRIPTION

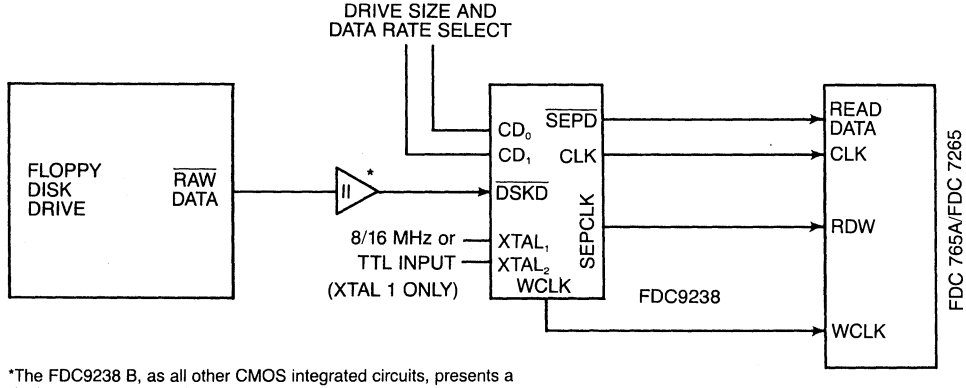
The FDC 9238 is a CMOS integrated circuit designed to complement the FDC 765A (8272A) or the FDC 7265 floppy disk controller. It incorporates a high performance, synthetic phase locked loop digital data separator and clock generator in one 0.3 inch wide 14 pin package.

The use of a high performance synthetic phase locked loop data separator allows the system designer to replace (without sacrificing performance) a costly and board consuming analog data separator (and the tuning normally required with an analog design) with a cost effective, single chip digital circuit.

The FDC 9238 is available in four versions: the FDC 9238/T which is intended for disk transfer rates up to 250 kilobits per second and the FDC 9238B/T is intended for disk transfer rates up to 500 kilobits per second.




**FDC 9238 BLOCK DIAGRAM**




*The FDC9238 B, as all other CMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{DSKD}$ input to the FDC9238 B.

**TYPICAL SYSTEM IMPLEMENTATION**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{cc}$ | I | This pin MUST be tied to $V_{cc}$. |
| 2,3 | $CD_0$,$CD_1$ | I | These inputs select the appropriate internal clock divisor for the data rate of the disk data, the CLK output to the FDC and the WCLK output to the FDC. Refer to Table 1. |
| 4 | SEPCLK | 0 | A Square wave window clock signal output derived from the $\overline{DSKD}$ input. |
| 5 | SEPD | 0 | This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). To insure complete compatibility with the FDC 765A and FDC 7265, this output is positive going. |
| 6 | CLK | 0 | This output provides the clock signal for the FDC 765A or FDC 7265. |
| 7 | WCLK | 0 | This output provides the write clock signal for the FDC 765A or FDC 7265. |
| 8 | $GND_1$ | | Ground |
| 9 | $XTAL_1$/CLKIN | I | This input is for direct connection to an 8 or 16 MHz single-phase TTL level clock, or one lead from an 8 or 16 MHz crystal. |
| 10 | $GND_2$ | I | This pin must be tied to ground. |
| 11 | $XTAL_2$ | I | In the FDC 9238 and FDC 9238B, the second lead from an 8 or 16 MHz crystal is connected to this pin. In the FDC 9238T and FDC 9238BT, this pin should be left floating. |
| 12 | NC | | No connection should be made to this pin. |
| 13 | $V_{cc}$ | I | +5 Volts |
| 14 | $\overline{DSKD}$ | I | This input is the raw read data received from the drive. (This input is active low.) |



## OPERATION

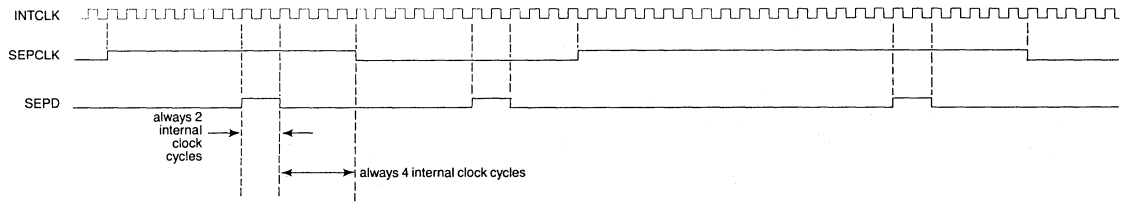
The high performance digital data separator incorporated in the FDC 9238 will accept data from the floppy disk drive at 125 KHz, 250 KHz, or 500 KHz data rates and output the appropriate regenerated clock and data signals.

The heart of the digital floppy disk data separator section is a synthetic oscillator phase locked loop. One half-bit cell of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of 16 phase slices. The circuit, therefore, needs a phase slice clock with a frequency of 16 times the half-bit cell time.

Detection of an input pulse away from the center of its half-bit "slot" causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit slot closer to the pulse.

The end-of-cycle signal from the synthetic oscillator defines the derived clock waveform and the duration of each half-bit slot. If there is a flux transition during the half-bit slot, it is remembered and used to regenerate the data waveform pulses immediately following the end-of-cycle.

A short history of input pulse detections (which induce phase corrections by the FDC 9238) is kept. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency, and helps compensate for drive speed variations. This, along with separate short term and long term correction algorithms, assures accurate floppy disk data separation.



## MAXIMUM GUARANTEED RATINGS

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −55°C to 150°C |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Positive Voltage on any I/O Pin, with respect to ground | +7.0V |
| Negative Voltage on any I/O Pin, with respect to ground | −0.3V |
| Power Dissipation | 0.25W |

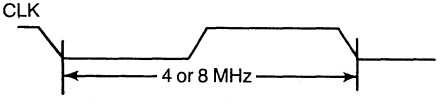
Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

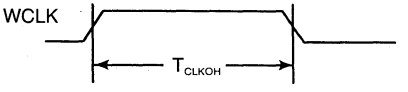
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

**PRELIMINARY**
Notice: This is not a final specification.
Some parametric limits are subject to change.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE | | | | | |
| Low ($V_{IL}$) | −0.3 | | 0.8 | V | Except XTAL/CLKIN |
| High ($V_{IH}$) | 2.0 | | $V_{cc}$ | | |
| XTAL/CLKIN INPUT VOLTAGE | | | | | |
| Low ($V_{IL}$) | −0.3 | | 1.5 | V | |
| High ($V_{IH}$) | 3.2 | | $V_{cc}$ | V | |
| OUTPUT VOLTAGE | | | | | |
| Low ($V_{OL}$) | | | 0.4 | V | $L_{OL}$ = 1.6 ma, except CLK |
| | | | | | $L_{OL}$ = 0.4 ma, CLK only |
| | | | | | $L_{OH}$ = −100µa, except CLK |
| High ($V_{OH}$) | 2.4 | | | | $L_{OH}$ = −400µa, CLK only |
| POWER SUPPLY CURRENT | | | | | |
| $I_{cc}$ | | TBD | | | |
| INPUT LEAKAGE CURRENT | | | | | |
| $I_{IL}$ | | TBD | | | |
| INPUT CAPACITANCE | | | | | |
| $C_{IN}$ | | TBD | | | |
| **AC ELECTRICAL CHARACTERISTICS** | (All times assume XTAL/CLKIN = 16 MHz unless otherwise specified) | | | | |
| CLKIN Frequency | 3.95 | 16 | 16.2 | MHz | FDC 9238B/BT |
| | 3.95 | 8.0 | 8.1 | MHz | FDC 9238/T |
| CLKIN Duty Cycle | 40 | | 60 | % | |
| $T_{CLKOH}$ | 90 | 125 | 140 | ns | |




| XTAL | Inputs $CD_1$ | Inputs $CD_0$ | DISK DATA RATE | CLK | WCLK | ENCODING |
|---|---|---|---|---|---|---|
| 16MHz | 0 | 0 | 250KHz | 8MHz | 500KHz | FM |
| 16MHz | 1 | 0 | 500KHz | 8MHz | 1MHz | MFM |
| 16MHz | 0 | 1 | 125KHz | 4MHz | 250KHz | FM |
| 16MHz | 1 | 1 | 250KHz | 4MHz | 500KHz | MFM |
| 8MHz | 0 | 0 | 125KHz | 4MHz | 250KHz | FM |
| 8MHz | 1 | 0 | 250KHz | 4MHz | 500KHz | MFM |
| 8MHz | 0 | 1 | Not Used | | | |
| 8MHz | 1 | 1 | Not Used | | | |

**TABLE 1**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications: consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# FDC 9239/9239B 9239T/9239BT

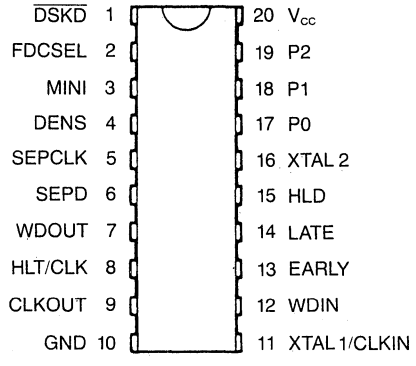
**PRELIMINARY**

# ENHANCED FLOPPY DISK INTERFACE CIRCUIT

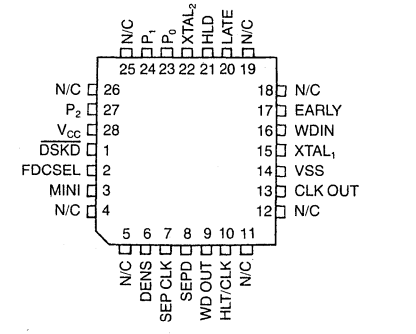
## FEATURES

- ☐ Digital Data Separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 3½", 5¼" and 8" compatible
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator Circuit
- ☐ Track-Selectable Write Precompensation
- ☐ Retriggerable Head-Load Timer
- ☐ Fully compatible with FDC 179X, FDC 765A and FDC 7265
- ☐ 16-Bit Cell Divide Algorithm Improves Performance
- ☐ Fabricated in Low Power CMOS
- ☐ Single +5 Volt Supply
- ☐ TTL Compatible; Fully Compatible with the FDC 9229

## PIN CONFIGURATION




PACKAGE: 20-pin D.I.P.




PACKAGE: 28-pin PLCC

## FUNCTIONAL DESCRIPTION

The FDC 9239 is a CMOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9239 provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9239 operates from a +5V supply.

The FDC 9239 is available in four versions: the FDC 9239/T which is intended for 5¼" drives and the FDC 9239B/T for 3½", 5¼" and 8" drives. (The /T versions require a TTL clock input.)

SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | SYMBOL | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $\overline{DSKD}$ | I | This input is the raw read data received from the drive. (This input is active low.) |
| 2 | FDCSEL | I | This input signal, when low, programs the FDC 9239 for a 179X type of LSI controller. When FDCSEL is high, the FDC 9239 is programmed for a 765 (8272) or 7265 floppy disk controller. (See fig. 4.) |
| 3 | MINI | I | The state of this input determines whether the FDC 9239 is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). See figs. 2, 3, and 4.) |
| 4 | DENS | I | The state of this input determines whether the FDC 9239 is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.) |
| 5 | SEPCLK | O | A square-wave window clock signal output derived from the $\overline{DSKD}$ input. |
| 6 | SEPD | O | This output is the regenerated data pulse derived from the raw data input ($\overline{DSKD}$). This signal may be either active low or active high as determined by FDCSEL (pin 2). |
| 7 | WDOUT | O | The precompensated WRITE DATA stream to the drive. |
| 8 | HLT/CLK | O | When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.) |
| 9 | CLKOUT | O | This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS and FDCSEL input pins. (See fig. 3.) |
| 10 | GND | | Ground |
| 11 | XTAL 1/CLKIN | I | This input is for direct connection to a 16 MHz or 8 MHz single-phase TTL-level clock, or one lead from an 8 MHz or 16 MHz crystal. |
| 12 | WDIN | I | The write data stream from the floppy disk controller. |
| 13 | EARLY | I | When this input is high, the current WRITE DATA pulse will be written early to the disk. |
| 14 | LATE | I | When this input is high, the current WRITE DATA pulse will be written late to the disk.<br>When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position. |
| 15 | HLD | I | This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state MINI output. (See fig. 3.) In 765 mode this pin should be grounded. |
| 16 | XTAL 2 | I | The second lead from an 8 MHz or 16 MHz crystal is connected to this pin. In those applications, using a TTL clock, this pin should be left floating. |
| 17 | P0 | I | P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.) |
| 18 | P1 | I | |
| 19 | P2 | I | |
| 20 | $V_{CC}$ | | +5 VOLT SUPPLY |

## OPERATION

### Data Separator

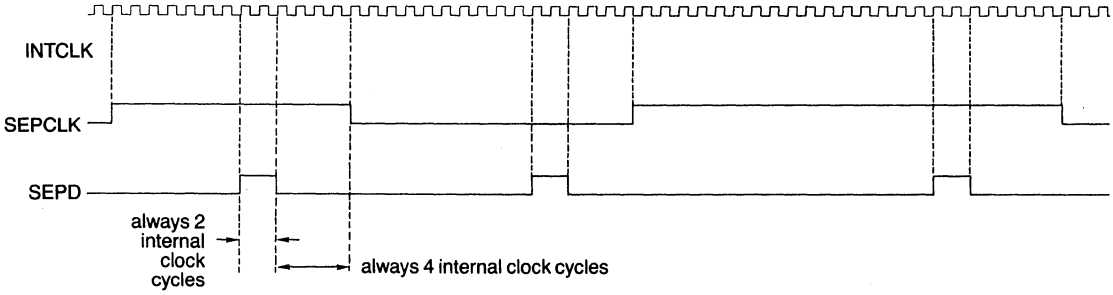
The CLKIN input clock is internally divided by the FDC 9239 to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

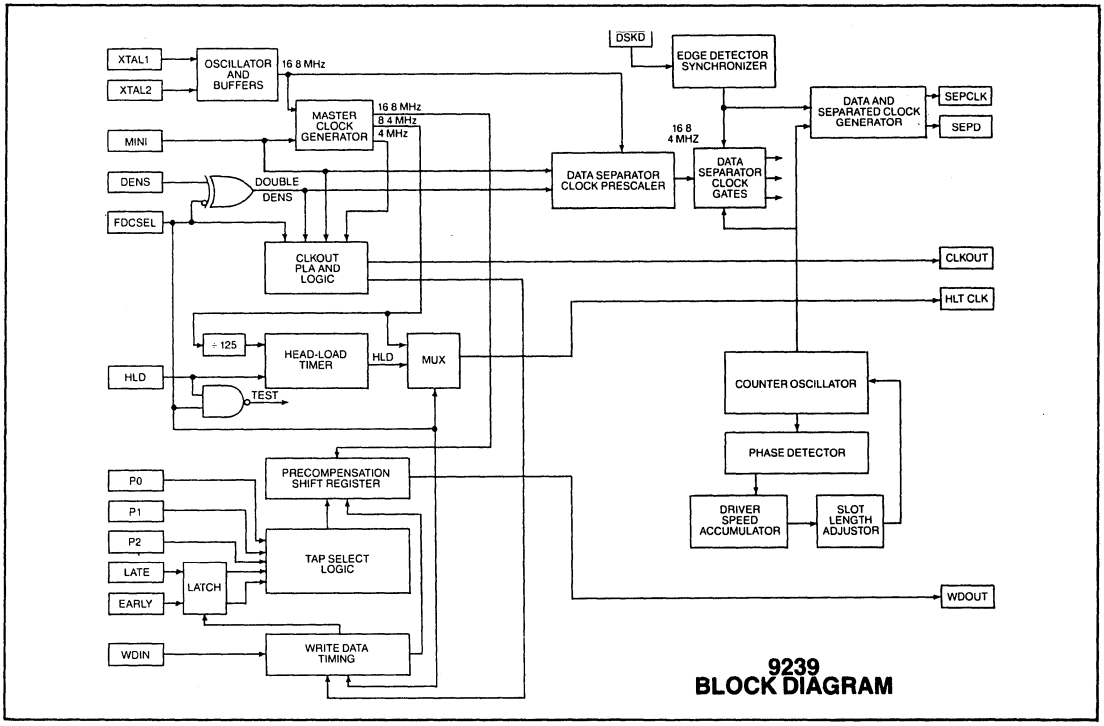
The FDC 9239 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/32 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 16 to a minimum of 12 and a maximum of 21 internal clock cycles.

| INPUTS | | | DIVISOR |
|---|---|---|---|
| FDCSEL | DENS | MINI | f(CLKIN)/f(INTCLK) |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 2 |
| 1 | 0 | 1 | 4 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 2 |




**9239 BLOCK DIAGRAM**

### Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9239 as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

### Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 or 7265 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9239 goes high before starting a read or write operation.

| MINI | P2 | P1 | P0 | PRECOMP VALUE |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 ns |
| 0 | 0 | 0 | 1 | 62.5 ns |
| 0 | 0 | 1 | 0 | 125 ns |
| 0 | 0 | 1 | 1 | 187.5 ns |
| 0 | 1 | 0 | 0 | 250 ns |
| 0 | 1 | 0 | 1 | 250 ns |
| 1 | 0 | 0 | 0 | 0 ns |
| 1 | 0 | 0 | 1 | 125 ns |
| 1 | 0 | 1 | 0 | 250 ns |
| 1 | 0 | 1 | 1 | 375 ns |
| 1 | 1 | 0 | 0 | 500 ns |
| 1 | 1 | 0 | 1 | 500 ns |
| 1 | 1 | 1 | 0 | 625 ns |
| 1 | 1 | 1 | 1 | 625 ns |

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

**FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION**

| INPUTS | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|
| FDCSEL | DENS | MINI | CLKOUT | HLT/CLK | 16 MHZ INPUT CLOCK | 8 MHZ INPUT CLOCK | CONTROLLER |
| 0 | 0 | 0 | 2 MHz | 40 ms* | 8" Double Density | 5¼" Double Density | 179X |
| 0 | 0 | 1 | 1 MHz | 80 ms* | 5¼" Double Density | Not Permitted | 179X |
| 0 | 1 | 0 | 2 MHz | 40 ms* | 8" Single Density | 5¼" Single Density | 179X |
| 0 | 1 | 1 | 1 MHz | 80 ms* | 5¼" Single Density | Not Permitted | 179X |
| 1 | 0 | 0 | 500 KHz | 8 MHz | 8" Single Density | 5¼" Single Density | 765 (8272) |
| 1 | 0 | 1 | 250 KHz | 4 MHz | 5¼" Single Density | Not Permitted | 765 (8272) |
| 1 | 1 | 0 | 1 MHz | 8 MHz | 8" Double Density | 5¼" Double Density | 765 (8272) |
| 1 | 1 | 1 | 500 KHz | 4 MHz | 5¼" Double Density | Not Permitted | 765 (8272) |

NOTE: 3½" drive users should consult drive specifications to determine if drive data rate equals 5.25" or 8" standards.

*NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

**FIG. 3 CLOCK/HEAD LOAD TIME DELAY AND FLOPPY DISK DRIVE/CONTROLLER SELECTION**

**MAXIMUM GUARANTEED RATINGS***

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −55° to +150°C |
| Lead Temperature (soldering, 10 sec.) | +300°C |
| Positive Voltage on any I/O Pin, with respect to ground | +7.0V |
| Negative Voltage on any I/O Pin, with respect to ground | −0.5V |
| Power Dissipation | 0.25W |

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| INPUT VOLTAGE | | | | | |
| Low Level $V_{IL}$ | −0.3 | | 0.8 | V | Except CLKIN |
| High Level $V_{IH}$ | 2.0 | | ($V_{CC}$) | V | |
| XTAL/CLKIN INPUT VOLTAGE | | | | | |
| Low ($V_{IL}$) | −0.3 | | 1.5 | V | |
| High ($V_{IH}$) | 3.2 | | ($V_{CC}$) | V | |
| OUTPUT VOLTAGE | | | | | |
| Low Level $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA except HLT/CLK |
| | | | | | $I_{OL}$ = 0.4 mA, HLT/CLK only |
| High Level $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −100 µA except HLT/CLK |
| | | | | | $I_{OH}$ = −400 µA, HLT/CLK only |
| POWER SUPPLY CURRENT | | | | | |
| $I_{CC}$ | | | 20 | mA | |
| INPUT LEAKAGE CURRENT | | | | | |
| $I_{IL}$ | | | 10 | µA | $V_{IN}$ = 0 to $V_{CC}$ |
| INPUT CAPACITANCE | | | | pF | Except CLKIN |
| $C_{IN}$ | | TBD | | pF | CLKIN only |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

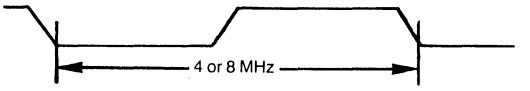
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ±5%)

| PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| **AC ELECTRICAL CHARACTERISTICS** | (All times assume XTAL/CLKIN = 16 MHz unless otherwise specified) | | | | |
| CLKIN frequency | 3.95 | 16 | 16.2 | MHz | FDC 9239B |
| | 3.95 | 8 | 8.1 | MHz | FDC 9239 |
| CLKIN DUTY CYCLE | 40 | | 60 | % | |
| $t_{clkoh}$ | 465 | 500 | 515 | ns | FDCSEL = low; MINI = high |
| | 215 | 250 | 265 | ns | FDCSEL = low; MINI = low |
| | 90 | 125 | 140 | ns | FDCSEL = high |
| $t_{wdo}$ | 150 | 312.5 | 350 | ns | Time Doubles with MINI-1 |
| $t_d$ | 50 | | 400 | ns | |
| $t_{dNEC}$ | 0 | | 400 | ns | |
| $t_{wdE}$ | 500 | 562.5 | | ns | 9 clock times ± 1 clock time |
| $t_{wdN}$ | | precomp value | | | See fig. 2 |
| $t_{wdL}$ | | 2 x precomp value | | | See fig. 2 |
| $t_s$ | 1.0 | | | µs | |

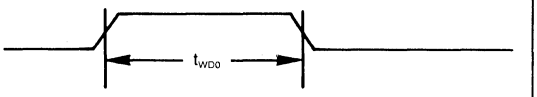
SECTION VI

# AC TIMING CHARACTERISTICS

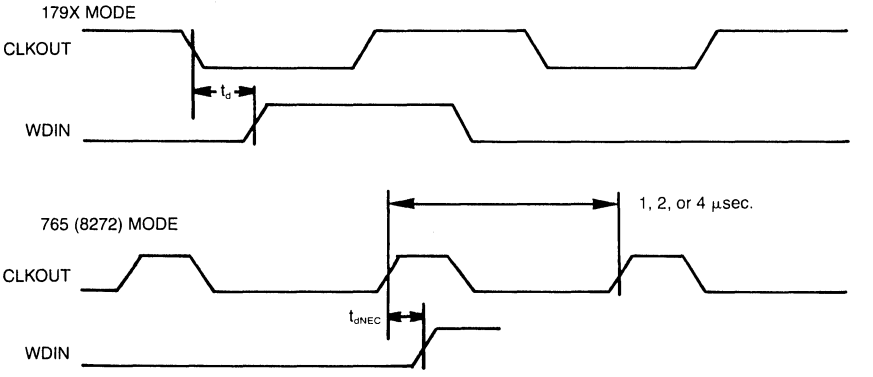
## HLT/CLK (765 MODE)



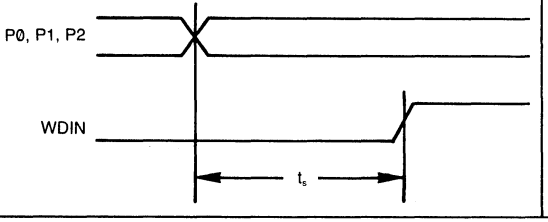

## WDOUT PULSE WIDTH



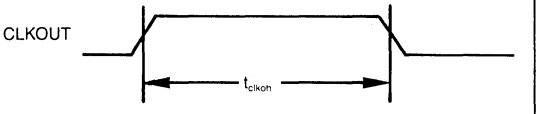

## CLKOUT VS. WDIN TIMING



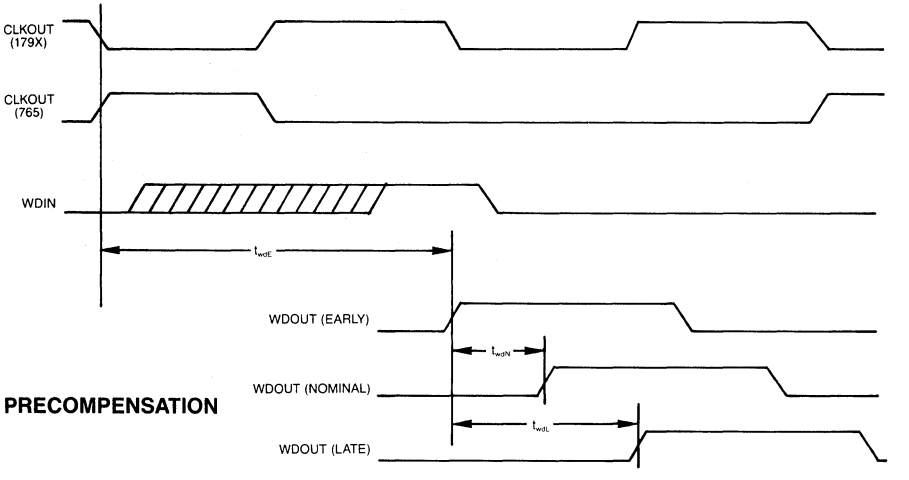

## SET-UP TIME P0, P1 AND P2 TO WDIN




## CLKOUT

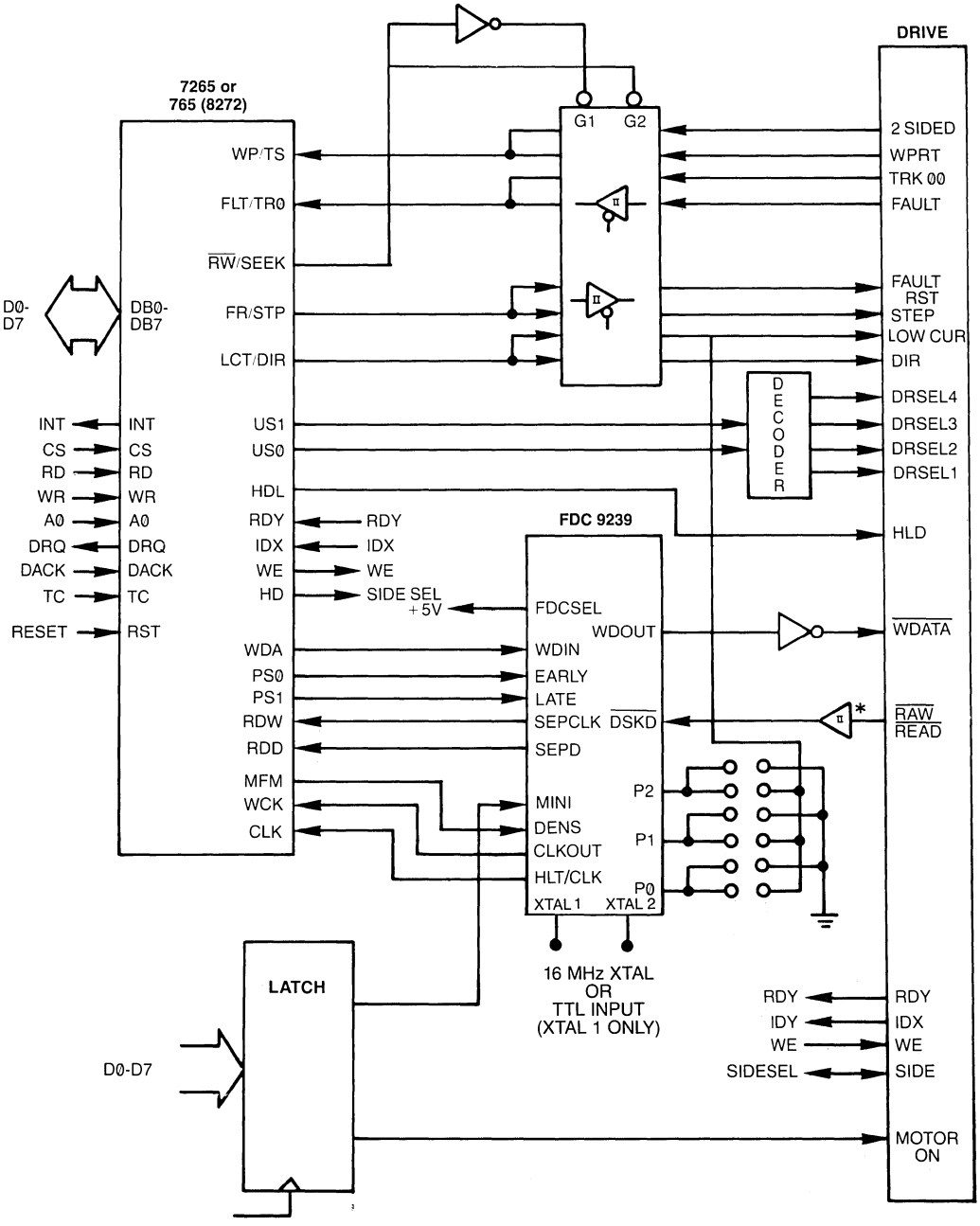



## PRECOMPENSATION




Ref. to Fig. 2 for $t_p$ (precompensation) value

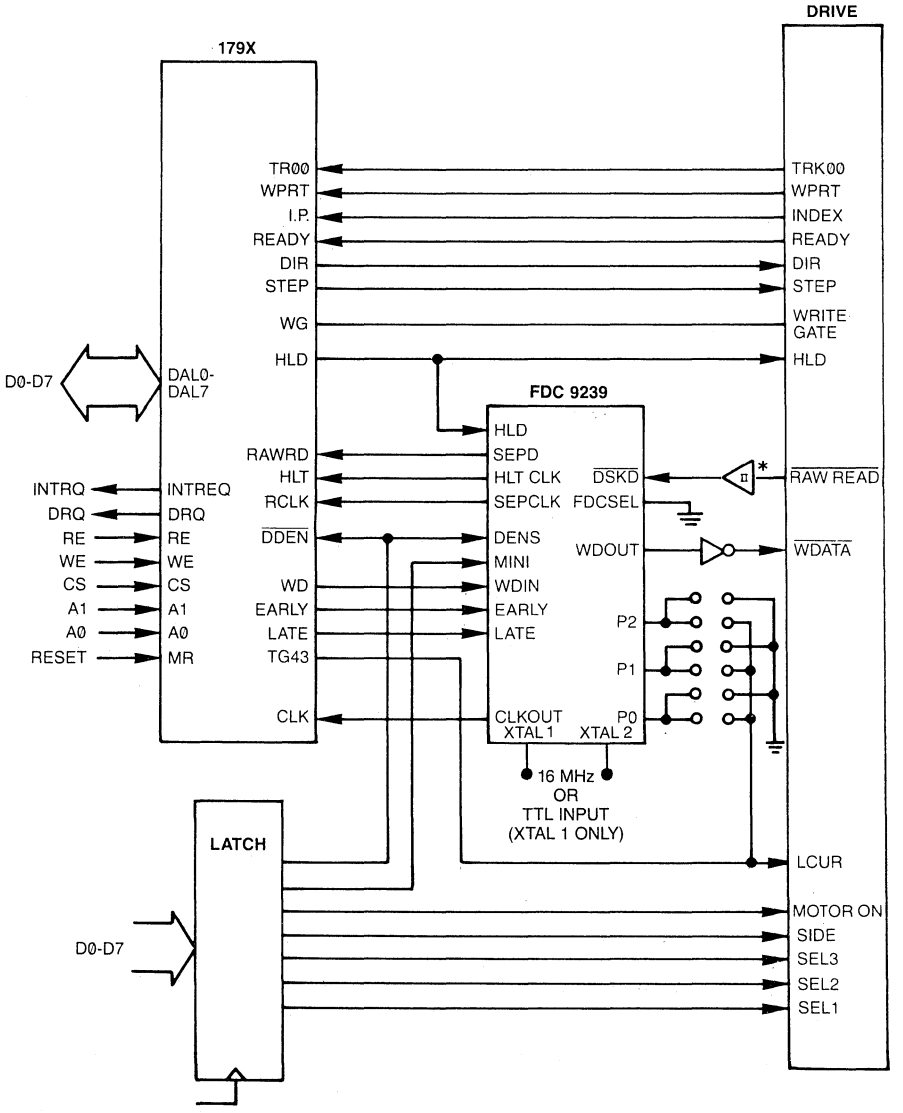
## TYPICAL SYSTEM IMPLEMENTATION—765 (8272) FDC OR 7265 FDC




*The FDC9239/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{\text{DSKD}}$ input to the FDC9239/B.

## TYPICAL SYSTEM IMPLEMENTATION—179X FDC OR 979X FDC




*The FDC9239/B, as all other CMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{DSKD}$ input to the FDC9239/B.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

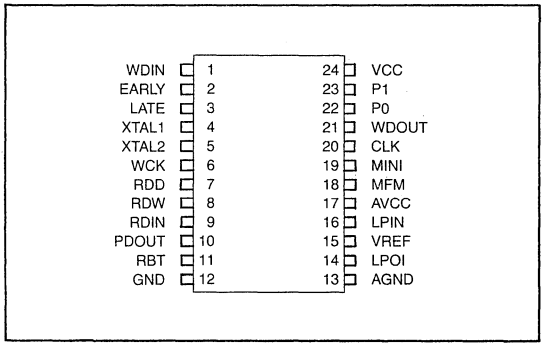
# FDC92C49
**PRELIMINARY**

# Analog Floppy Disk Data Separator (AFDDS)

## FEATURES

- ☐ Analog Data Separator performs complete data separation for floppy disk drives
  Separates FM and MFM encoded data
  3-1/2″, 5-1/4″ and 8″ compatible
- ☐ No critical adjustments necessary
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator
- ☐ Fully compatible with FDC765A
- ☐ High Performance Analog Pase Locked Loop
- ☐ Fabricated in Low Power CMOS
- ☐ TTL Compatible I/O
- ☐ Single +5V Supply

## PRELIMINARY PIN CONFIGURATION




SECTION VI

## GENERAL DESCRIPTION

The FDC92C49 CMOS Analog Floppy Disk Data Separator (AFDDS) performs high performance analog data separation on data from a floppy disk drive. The FDC92C49 is compatible with 3.5″, 5.25″ and 8″ floppy disk drives, and provides all clocks required by the industry standard FDC765A and FDC7265 floppy disk controllers.

The FDC92C49 incorporates all the active components necessary to implement analog floppy disk data separation, eliminating the need for discrete transistors. Only a crystal and a few external resistors and capacitors are required. Using the FDC92C49 and a floppy disk controller chip, a system designer can build a highly reliable, cost efficient double or single density floppy disk data subsystem requiring no tuning adjustments.

Six different user selectable values for write precompensation assure reliable positioning of data when writing to disk.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the products described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

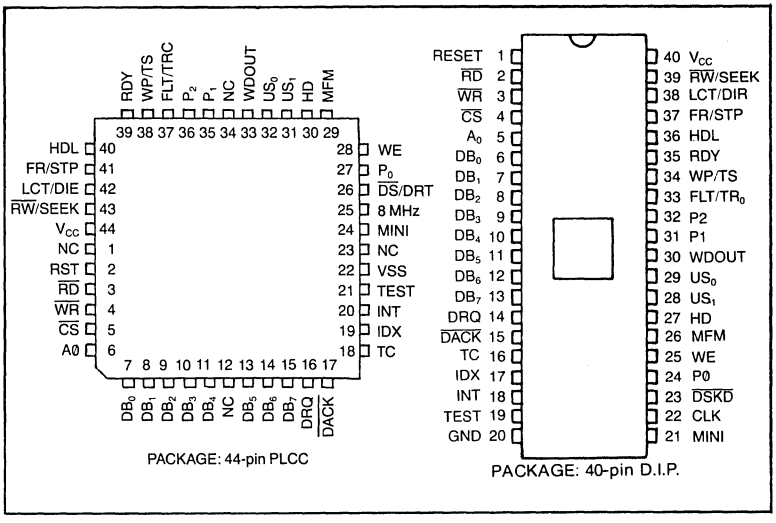
# FDC 9266

# Single/Double Density Enhanced Floppy Disk Controller

## FEATURES

- ☐ Combination Floppy Disk Controller and Floppy Disk Interface
- ☐ Software compatible with industry standard FDC 765A
- ☐ On chip digital data separator eliminates critical analog adjustments
- ☐ On-chip drive control logic reduces component count.
- ☐ IBM compatible in both single and double density recording formats
- ☐ Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- ☐ Multi-sector and multi-track transfer capability
- ☐ Controls up to 4 floppy disk drives
- ☐ Data Scan Capability–will scan a single sector or entire track's worth of data fields, comparing on a byte by byte basis, data in the processor's memory with the data read from the diskette
- ☐ Data transfers in DMA or non-DMA mode
- ☐ Single 8 MHz TTL clock input
- ☐ Single +5 Volt power supply
- ☐ Parallel Seek operations on up to four drives
- ☐ Compatible with most microprocessors
- ☐ COPLAMOS* n-channel silicon gate technology
- ☐ Available in 40-pin Dual-in-Line package and 44-pin PLCC

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The FDC 9266 is a monolithic combination of the industry standard FDC 765A Floppy Disk Controller and the FDC 9229 Floppy Disk Interface Circuit. It preserves all of the processor hardware and software interfaces to the FDC 765A, and contains on-chip circuitry to simplify drive interfacing.

These on-chip enhancements include a digital data separator, compatible with 5.25″ and 8″ drives. The data separator separates both FM (Single Density) and MFM (Double Density) encoded data, and requires no external adjustments.

The FDC 9266 also allows variable write precompensation, which is track selectable.

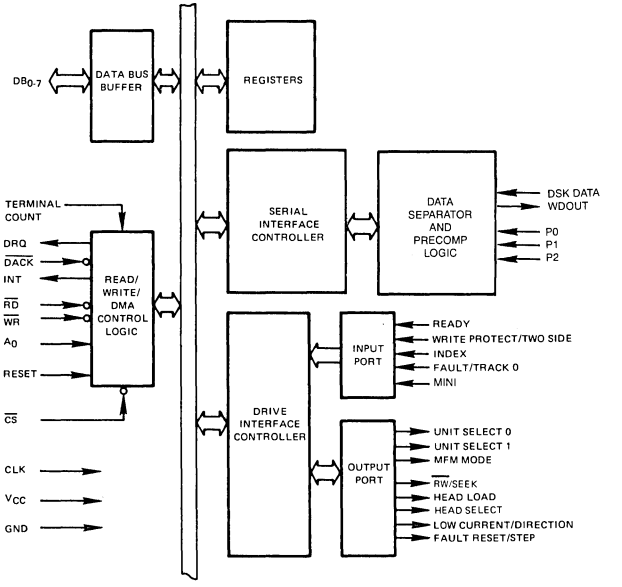
These enhancements greatly reduce the number of components required to interface floppy disks to a microprocessor system.

There are 15 separate commands which the FDC 9266 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

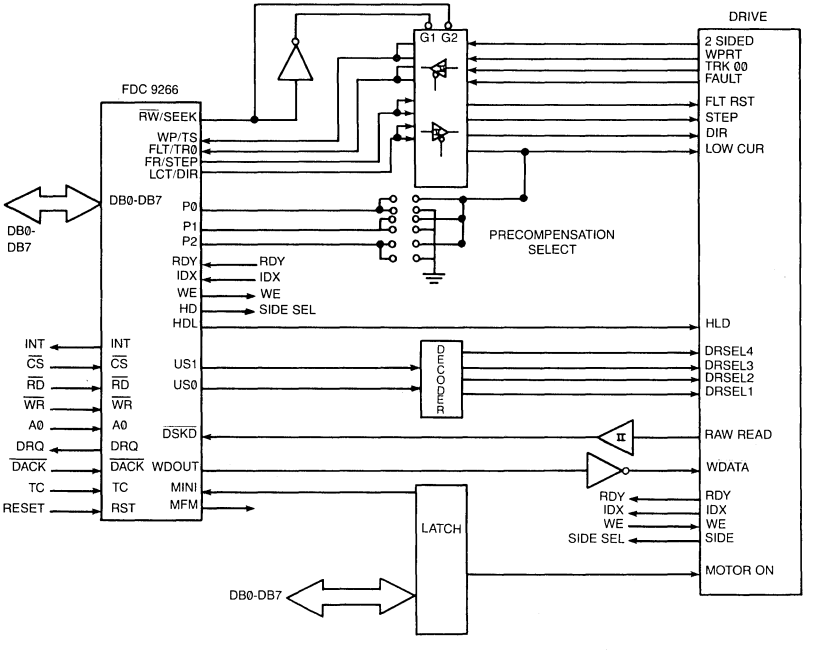
| | |
|---|---|
| Read Data | Write Data |
| Read ID | Format a Track |
| Read Deleted Data | Write Deleted Data |
| Read a Track | Seek |
| Scan Equal | Recalibrate (Restore to Track 0) |
| Scan High or Equal | Sense Interrupt Status |
| Scan Low or Equal | Sense Drive Status |
| Specify | |

Address mark detection circuitry is internal to the FDC which simplifies the read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The FDC 9266 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

SECTION VI




**BLOCK DIAGRAM**




**TYPICAL APPLICATION**

## DESCRIPTION OF PIN FUNCTIONS

| PIN | | | INPUT/ OUTPUT | CONNECTION TO | FUNCTION |
|---|---|---|---|---|---|
| NO. | SYMBOL | NAME | | | |
| 1 | RST | Reset | Input | Processor | Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1.024 ms later. To clear this interrupt use Sense Interrupt Status command. |
| 2 | $\overline{RD}$ | Read | Input① | Processor | Control signal for transfer of data from FDC to Data Bus, when "0" (low). |
| 3 | $\overline{WR}$ | Write | Input① | Processor | Control signal for transfer of data to FDC via Data Bus, when "0" (low). |
| 4 | $\overline{CS}$ | Chip Select | Input | Processor | IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled. |
| 5 | $A_0$ | Data/Status Reg Select | Input① | Processor | Selects Data Reg ($A_0$ = 1) or Status Reg ($A_0$ = 0) contents of the FDC to be sent to Data Bus. |
| 6-13 | $DB_0$-$DB_7$ | Data Bus | Input① Output | Processor | Bi-Directional 8-Bit Data Bus. |
| 14 | DRQ | Data DMA Request | Output | DMA | DMA Request is being made by FDC when DRW = "1". |
| 15 | $\overline{DACK}$ | DMA Acknowledge | Input | DMA | DMA cycle is active when "0" (low) and Controller is performing DMA transfer. |
| 16 | TC | Terminal Count | Input | DMA | Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode. |
| 17 | IDX | Index | Input | FDD | Indicates the beginning of a disk track. |
| 18 | INT | Interrupt | Output | Processor | Interrupt Request Generated by FDC. |
| 19 | TEST | Test | Input | | This pin is for test purposes only. Should be left tied high in normal operation. |
| 20 | GND | Ground | | | D.C. Power Return. |
| 21 | MINI | Mini | Input | Processor | This input, when set to "1" (high), configures the FDC for operation with 5.25" floppies. If reset to "0" (low), then the FDC is configured for 8" drive operation. |
| 22 | CLK | 8 MHz TTL Clock | Input | | Device clock. |
| 23 | $\overline{DSKD}$ | Raw Data | Input | FDD | Raw data from drive. |
| 24,31,32 | P0, P1, P2 | Precompensation Select | Input | Processor | These pins select the amount of precompensation applied to the write data. |
| 25 | $\overline{WE}$ | Write Enable | Output | FDD | Enables write data into FDD. |
| 26 | MFM | MFM Mode | Output | | MFM mode when "1," FM mode when "0." |
| 27 | HD | Head Select | Output | FDD | Head 1 selected when "1" (high). Head 2 selected when "0" (low). |
| 28, 29 | $US_1$, $US_0$ | Unit Select | Output | FDD | FDD Unit Selected. |
| 30 | WD OUT | Write Data Out | Output | FDD | Serial clock and data bits to FDD. |
| 33 | $FLT/TR_0$ | Fault/Track 0 | Input | FDD | Senses FDD fault condition, in Read/Write mode; and Track 0 condition in Seek mode. |
| 34 | WP/TS | Write Protect/ Two-Side | Input | FDD | Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | PIN SYMBOL | PIN NAME | INPUT/ OUTPUT | CONNECTION TO | FUNCTION |
|---|---|---|---|---|---|
| 35 | RDY | Ready | Input | FDD | Indicates FDD is ready to send or receive data. |
| 36 | HDL | Head Load | Output | FDD | Command which causes read/ write head in FDD to contact diskette. |
| 37 | FR/STP | Fit Reset/Stop | Output | FDD | Resets fault F.F. in FDD in Read/ Write mode, contains stop pulses to move head to another cylinder in Seek mode. |
| 38 | LCT/DIR | Low Current/ Direction | Output | FDD | Lowers Write current on inner tracks in Read/Write mode, determines direction head will stop in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal. |
| 39 | $\overline{RW}$/SEEK | Read Write/SEEK | Output | FDD | When "1" (high) Seek mode selected and when "0" (low) Read/ Write mode selected. |
| 40 | $V_{CC}$ | +5V | | | DC Power. |

Note: ① Disabled when CS = 1.

## DESCRIPTION OF INTERNAL REGISTERS

The FDC 9266 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC 9266.

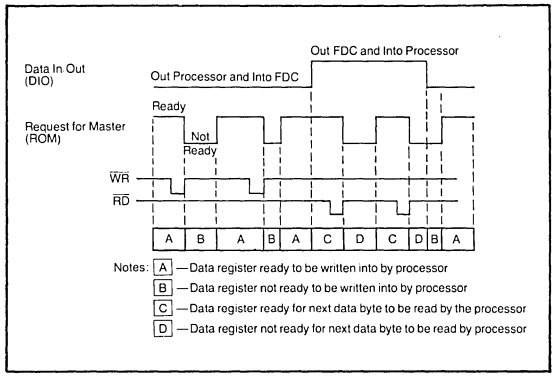
The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and $A_0$ is shown below.

| $A_0$ | $\overline{RD}$ | $\overline{WR}$ | FUNCTION |
|---|---|---|---|
| 0 | 0 | 1 | Read Main Status Register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from Data Register |
| 1 | 1 | 0 | Write into Data Register |

The bits in the Main Status Register are defined as follows:

| BIT NUMBER | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| $DB_0$ | FDD 0 Busy | $D_0B$ | FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_1$ | FDD 1 Busy | $D_1B$ | FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_2$ | FDD 2 Busy | $D_2B$ | FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_3$ | FDD 3 Busy | $D_3B$ | FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command. |
| $DB_4$ | FDC Busy | CB | A read or write command is in process. FDC will not accept any other command. |
| $DB_5$ | Execution Mode | EXM | This bit is set only during execution phase in non-DMA mode. When $DB_5$ goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation. |
| $DB_6$ | Data Input/Output | DIO | Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register. |
| $DB_7$ | Request for Master | RQM | Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor. |

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when $DB_4$ (FDC Busy) goes low is 12 μs.




## COMMAND SEQUENCE

The FDC 9266 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC 9266 and the processor, it is convenient to consider each command as consisting of three phases:

| | |
|---|---|
| Command Phase: | The FDC receives all information required to perform a particular operation from the processor. |
| Execution Phase: | The FDC performs the operation it was instructed to do. |
| Result Phase: | After completion of the operation, status and other housekeeping information are made available to the processor. |

## COMMAND SYMBOL DESCRIPTION

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| $A_0$ | Address Line 0 | $A_0$ controls selection of Main Status Register ($A_0$ = 0) or Data Register ($A_0$ = 1). |
| C | Cylinder Number | C stands for the current/selected Cylinder (track) number 0 through 76 of the medium. |
| D | Data | D stands for the data pattern which is going to be written into a Sector. |
| $D_7$-$D_0$ | Data Bus | 8-bit Data Bus, where $D_7$ stands for a most significant bit, and $D_0$ stands for a least significant bit. |
| DTL | Data Length | When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector. |
| EOT | End of Track | EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT. |
| GPL | Gap Length | GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3. |
| H | Head Address | H stands for head number 0 or 1, as specified in ID field. |
| HD | Head | HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.) |
| HLT | Head Load Time | HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments). |
| HUT | Head Unload Time | HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments). |
| MF | FM or MFM Mode | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT | Multi-Track | If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1. |
| N | Number | N stands for the number of data bytes written in a Sector. |
| NCN | New Cylinder Number | NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head. |
| ND | Non-DMA Mode | ND stands for operation in the Non-DMA Mode. |
| PCN | Present Cylinder Number | PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time. |
| R | Record | R stands for the Sector number, which will be read or written. |
| R/W | Read/Write | R/W stands for either Read (R) or Write (W) signal. |
| SC | Sector | SC indicates the number of Sectors per Cylinder. |
| SK | Skip | SK stands for Skip Deleted Data Address Mark. |
| SRT | Step Rate Time | SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.). |
| ST 0<br>ST 1<br>ST 2<br>ST 3 | Status 0<br>Status 1<br>Status 2<br>Status 3 | ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0$ = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command. |
| STP | | During a Scan operation, if STP = 1, the data in continguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared. |
| US0, US1 | Unit Select | US stands for a selected drive number 0 or 1. |

# INSTRUCTION SET ① ②

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 0 | 1 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 1 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 0 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the main-system and FDD |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | SK | 0 | 0 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT. |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ ID** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 0 | 1 | 0 | Commands |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Execution | | | | | | | | | | The first correct ID information on the Cylinder is stored in Data Register |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information read during Execution Phase from Floppy Disk |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **FORMAT A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | N | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | Sectors/Track |
| | W | GPL | | | | | | | | Gap 3 |
| | W | D | | | | | | | | Filler Byte |
| Execution | | | | | | | | | | FDC formats an entire track |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | In this case, the ID information has no meaning |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 0 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

**Note:** ① Symbols used in this table are described at the end of this section.

② $A_0$ should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

## INSTRUCTION SET (CONT.)

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **SCAN LOW OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | ——— | | | C | | | | ——— | Sector ID information prior |
| | W | ——— | | | H | | | | ——— | Command execution |
| | W | ——— | | | R | | | | ——— | |
| | W | ——— | | | N | | | | ——— | |
| | W | ——— | | | EOT | | | | ——— | |
| | W | ——— | | | GPL | | | | ——— | |
| | W | ——— | | | STP | | | | ——— | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ——— | | | ST 0 | | | | ——— | Status information after |
| | R | ——— | | | ST 1 | | | | ——— | Command execution |
| | R | ——— | | | ST 2 | | | | ——— | |
| | R | ——— | | | C | | | | ——— | Sector ID information after |
| | R | ——— | | | H | | | | ——— | Command execution |
| | R | ——— | | | R | | | | ——— | |
| | R | ——— | | | N | | | | ——— | |
| **SCAN HIGH OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | ——— | | | C | | | | ——— | Sector ID information prior |
| | W | ——— | | | H | | | | ——— | Command execution |
| | W | ——— | | | R | | | | ——— | |
| | W | ——— | | | N | | | | ——— | |
| | W | ——— | | | EOT | | | | ——— | |
| | W | ——— | | | GPL | | | | ——— | |
| | W | ——— | | | STP | | | | ——— | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ——— | | | ST 0 | | | | ——— | Status information after |
| | R | ——— | | | ST 1 | | | | ——— | Command execution |
| | R | ——— | | | ST 2 | | | | ——— | |
| | R | ——— | | | C | | | | ——— | Sector ID information after |
| | R | ——— | | | H | | | | ——— | Command execution |
| | R | ——— | | | R | | | | ——— | |
| | R | ——— | | | N | | | | ——— | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **RECALIBRATE** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | 0 | US1 | US0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 |
| **SENSE INTERRUPT STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command Codes |
| Result | R | ——— | | | STO | | | | ——— | Status information at the end |
| | R | ——— | | | PCN | | | | ——— | of seek-operation about the FDC |
| **SPECIFY** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command Codes |
| | W | ——— | SRT | | ◄ | | | ► | HUT | ——— |
| | W | ——— | HLT | | | | | ► | ND | ——— |
| **SENSE DRIVE STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Result | R | ——— | | | ST 3 | | | | ——— | Status information about FDD |
| **SEEK** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | ——— | | | NCN | | | | ——— | |
| Execution | | | | | | | | | | Head is positioned over proper Cylinder on Diskette |
| **INVALID** | | | | | | | | | | |
| Command | W | ——— | | | Invalid Codes | | | | ——— | Invalid Command Codes (NoOp – FDC goes into Standby State) |
| Result | R | ——— | | | ST 0 | | | | ——— | ST 0 = 80 (16) |

## FUNCTIONAL DESCRIPTION OF COMMANDS

### Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

| Multi-Track MT | MFM/FM MF | Bytes/Sector N | Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors) | Final Sector Read from Diskette |
|---|---|---|---|---|
| 0 | 0 | 00 | (128) (26) = 3,328 | 26 at Side 0 |
| 0 | 1 | 01 | (256) (26) = 6,656 | or 26 at Side 1 |
| 1 | 0 | 00 | (128) (52) = 6,656 | 26 at Side 1 |
| 1 | 1 | 01 | (256) (52) = 13,312 | |
| 0 | 0 | 01 | (256) (15) = 3,840 | 15 at Side 0 |
| 0 | 1 | 02 | (512) (15) = 7,680 | or 15 at Side 1 |
| 1 | 0 | 01 | (256) (30) = 7,680 | 15 at Side 1 |
| 1 | 1 | 02 | (512) (30) = 15,360 | |
| 0 | 0 | 02 | (512) (8) = 4,096 | 8 at Side 0 |
| 0 | 1 | 03 | (1024) (8) = 8,192 | or 8 at Side 1 |
| 1 | 0 | 02 | (512) (16) = 8,192 | 8 at Side 1 |
| 1 | 1 | 03 | (1024) (16) = 16,384 | |

**Table 1. Transfer Capacity**

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

| MT | HD | Final Sector Transferred to Processor | ID Information at Result Phase | | | |
|---|---|---|---|---|---|---|
| | | | C | H | R | N |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | NC | LSB | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | LSB | R = 01 | NC |

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

## Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

## Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

## Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

## Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

| Format | Sector Size | N | SC | GPL① | GPL②③ |
|---|---|---|---|---|---|
| 8" Standard Floppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 1A | 07 | 1B |
| | 256 | 01 | 0F | 0E | 2A |
| | 512 | 02 | 08 | 1B | 3A |
| | 1024 | 03 | 04 | 47 | 8A |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 1A | 0E | 36 |
| | 512 | 02 | 0F | 1B | 54 |
| | 1024 | 03 | 08 | 35 | 74 |
| | 2048 | 04 | 04 | 99 | FF |
| | 4096 | 05 | 02 | C8 | FF |
| | 8192 | 06 | 01 | C8 | FF |
| 5¼" Minifloppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 12 | 07 | 09 |
| | 128 | 00 | 10 | 10 | 19 |
| | 256 | 01 | 08 | 18 | 30 |
| | 512 | 02 | 04 | 46 | 87 |
| | 1024 | 03 | 02 | C8 | FF |
| | 2048 | 04 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 12 | 0A | 0C |
| | 256 | 01 | 10 | 20 | 32 |
| | 512 | 02 | 08 | 2A | 50 |
| | 1024 | 03 | 04 | 80 | F0 |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |

***Table 3***

**Notes:** ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

## Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

## Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC 9266 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes.

## Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

| COMMAND | STATUS REGISTER 2 | | COMMENTS |
|---|---|---|---|
| | BIT 2 = SN | BIT 3 = SH | |
| Scan Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} \neq D_{PROCESSOR}$ |
| Scan Low or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} < D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| Scan High or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} < D_{PROCESSOR}$ |

**Table 4**

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

## Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $DB_0$-$DB_3$ in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

## Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

## Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

| SEEK END | INTERRUPT CODE | | |
|---|---|---|---|
| BITS 5 | BIT 6 | BIT 7 | CAUSE |
| 0 | 1 | 1 | Ready Line changed state, either polarity |
| 1 | 0 | 0 | Normal Termination of Seek or Recalibrate Command |
| 1 | 1 | 0 | Abnormal Termination of Seek or Recalibrate Command |

**Table 5**

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

### Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

### Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

### Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC 9266 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC 9266 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.



## STATUS REGISTER IDENTIFICATION

| BIT | | | |
|---|---|---|---|
| NO. | NAME | SYMBOL | DESCRIPTION |
| $D_7$ $D_6$ | Interrupt Code | IC | $D_7$ = 0 and $D_6$ = 0<br>Normal Termination of Command, (NT). Command was completed and properly executed. |
| | | | $D_7$ = 0 and $D_6$ = 1<br>Abnormal Termination of Command, (AT).<br>Execution of Command was started, but was not successfully completed. |
| | | | $D_7$ = 1 and $D_6$ = 0<br>Invalid Command issue, (IC). Command which was issued was never started. |
| | | | $D_7$ = 1 and $D_6$ = 1<br>Abnormal Termination because during command execution the ready signal from FDD changed state. |
| $D_5$ | Seek End | SE | When the FDC completes the SEEK Command, this flag is set to 1 (high). |
| $D_4$ | Equipment Check | EC | If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set. |
| $D_3$ | Not Ready | NR | When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set. |
| $D_2$ | Head Address | HD | This flag is used to indicate the state of the head at Interrupt. |
| $D_1$ | Unit Select 1 | US 1 | These flags are used to indicate a Drive Unit. Number at Interrupt. |
| $D_0$ | Unit Select 0 | US 0 | |

| BIT NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| | | | **STATUS REGISTER 1(CONT.)** |
| $D_7$ | End of Cylinder | EN | When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set. |
| $D_6$ | | | Not used. This bit is always 0 (low). |
| $D_5$ | Data Errror | DE | When the FDC detects a CRC error in either the ID field or the data field, this flag is set. |
| $D_4$ | Over Run | OR | If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set. |
| $D_3$ | | | Not used. This bit always 0 (low). |
| $D_2$ | No Data | ND | During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set. |
| | | | During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set. |
| | | | During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set. |
| $D_1$ | Not Writable | NW | During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set. |
| $D_0$ | Missing Address Mark | MA | If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. |
| | | | If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set. |
| | | | **STATUS REGISTER 2** |
| $D_7$ | | | Not used. This bit is always 0 (low). |
| $D_6$ | Control Mark | CM | During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set. |
| $D_5$ | Data Error in Data Field | DD | If the FDC detects a CRC error in the data field then this flag is set. |
| $D_4$ | Wrong Cylinder | WC | This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set. |
| $D_3$ | Scan Equal Hit | SH | During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set. |
| $D_2$ | Scan Not Satisfied | SN | During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set. |
| $D_1$ | Bad Cylinder | BC | This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set. |
| $D_0$ | Missing Address Mark in Data Field | MD | When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set. |
| | | | **STATUS REGISTER 3** |
| $D_7$ | Fault | FT | This bit is used to indicate the status of the Fault signal from the FDD. |
| $D_6$ | Write Protected | WP | This bit is used to indicate the status of the Write Protected signal from the FDD. |
| $D_5$ | Ready | RY | This bit is used to indicate the status of the Ready signal from the FDD. |
| $D_4$ | Track 0 | T0 | This bit is used to indicate the status of the Track 0 signal from the FDD. |
| $D_3$ | Two Side | TS | This bit is used to indicate the status of the Two Side signal from the FDD. |
| $D_2$ | Head Address | HD | This bit is used to indicate the status of Side Select signal to the FDD. |
| $D_1$ | Unit Select 1 | US 1 | This bit is used to indicate the status of the Unit Select 1 signal to the FDD. |
| $D_0$ | Unit Select 0 | US 0 | This bit is used to indicate the status of the Unit Select 0 signal to the FDD. |

## PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC 9266. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC 9266. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC 9266 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC 9266 is in the NON-DMA Mode, then the receipt of each data byte (if FDC 9266 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC 9266 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC 9266 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC 9266 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The FDC 9266 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

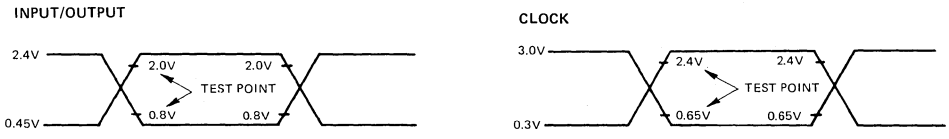
The bytes of data which are sent to the FDC 9266 to form the Command Phase, and are read out of the FDC 9266 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC 9266, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC 9266 is ready for a new command.

## POLLING FEATURE OF THE FDC 9266

After the Specify command has been sent to the FDC 9266, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC 9266 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC 9266 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC 9266 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

SECTION VI

## AC TEST CONDITION




## AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

### PRECOMPENSATION

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive.

| P2 | P1 | P0 | PRECOMP VALUE |
|---|---|---|---|
| 0 | 0 | 0 | 0 NS |
| 0 | 0 | 1 | 125 NS |
| 0 | 1 | 0 | 250 NS |
| 0 | 1 | 1 | 375 NS* |
| 1 | 0 | 0 | 500 NS* |

**WRITE PRECOMPENSATION VALUE SELECTION**

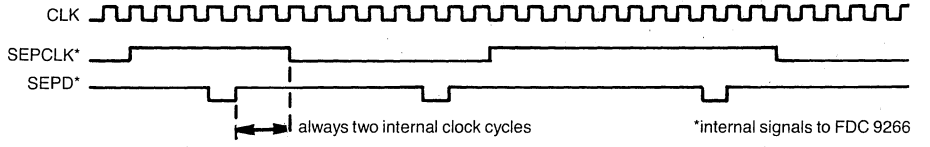
*NOTE: Precomp values of 375 ns and 500 ns are valid only with 5¼" drives.

### DATA SEPARATOR

The FDC 9266 detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the internal SEPCLK signal.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the CLK frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.




## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −55°C to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage $V_{CC}$ ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

$T_a$ = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC CHARACTERISTICS** $T_a$ = −10°C to +70°C; $V_{CC}$ = +5V ±5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP① | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | −0.5 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.5 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | $V_{CC}$ | V | $I_{OH}$ = −200 µA |
| Input Low Voltage (CLK + WR Clock) | $V_{IL(\phi)}$ | −0.5 | | 0.65 | V | |
| Input High Voltage (CLK + WR Clock) | $V_{IH(\phi)}$ | 2.4 | | $V_{CC}$ + 0.5 | V | |
| $V_{CC}$ Supply Current | $I_{CC}$ | | | 200 | mA | |
| Input Load Current (All Input Pins) | $I_{LI}$ | | | 10 | µA | $V_{IN}$ = $V_{CC}$ |
| | | | | −10 | µA | $V_{IN}$ = 0V |
| High Level Output Leakage Current | $I_{LOH}$ | | | 10 | µA | $V_{OUT}$ = $V_{CC}$ |
| Low Level Output Leakage Current | $I_{LOL}$ | | | −10 | µA | $V_{OUT}$ = +0.45V |

NOTE: ①Typical values for $T_a$ = 25°C and nominal supply voltage.

**DC CHARACTERISTICS** $T_a$ = 25°C; $f_c$ = 1 MHz; $V_{CC}$ = 0V

| PARAMETER | SYMBOL | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| Clock Input Capacitance | $C_{IN(\phi)}$ | | | 20 | pF | All Pins Except Pin Under Test Tied to AC Ground |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

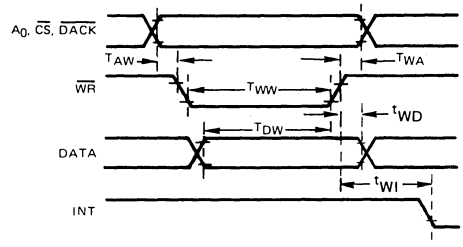
**AC CHARACTERISTICS** $T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP① | MAX | | |
| Clock Period | $\phi_{CY}$ | 120 | 125 | 130 | ns | |
| Clock Active (High, Low) | $\phi_0$ | 40 | | | ns | |
| Clock Rise Time | $\phi_r$ | | | 20 | ns | |
| Clock Fall Time | $\phi_f$ | | | 20 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓ | $T_{AR}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑ | $T_{RA}$ | 0 | | | ns | |
| $\overline{RD}$ Width | $T_{RR}$ | 250 | | | ns | |
| Data Access Time from $\overline{RD}$ ↓ | $T_{RD}$ | | | 200 | ns | $C_L$ = 100 pF |
| DB to Float Delay Time from $\overline{RD}$ ↑ | $T_{DF}$ | 20 | | 100 | ns | $C_L$ = 100 pF |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓ | $T_{AW}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑ | $T_{WA}$ | 0 | | | ns | |
| $\overline{WR}$ Width | $T_{WW}$ | 250 | | | ns | |
| Data Set Up Time to $\overline{WR}$ ↑ | $T_{DW}$ | 150 | | | ns | |
| Data Hold Time from $\overline{WR}$ ↑ | $T_{WD}$ | 5 | | | ns | |
| INT Delay Time from $\overline{RD}$ ↑ | $T_{RI}$ | | | 500 | ns | |
| INT Delay Time from $\overline{WR}$ ↑ | $T_{WI}$ | | | 500 | ns | |
| DRQ Cycle Time | $T_{MCY}$ | 13 | | | µs | |
| DRQ Delay Time from $\overline{DACK}$ ↓ | $T_{AM}$ | | | 200 | ns | |
| TC Width | $T_{TC}$ | 1 | | | $\phi_{CY}$ | |
| Reset Width | $T_{RST}$ | 14 | | | $\phi_{CY}$ | |
| $US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑ | $T_{US}$ | 12 | | | µs | 8 MHz Clock Period |
| SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑ | $T_{SD}$ | 7 | | | µs | |
| LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑ | $T_{DST}$ | 1.0 | | | µs | |
| $US_{0,1}$ Hold Time from FAULT RESET/STEP ↑ | $T_{STU}$ | 5.0 | | | µs | |
| STEP Active Time (High) | $T_{STP}$ | 6.0 | 7.0 | | µs | |
| STEP Cycle Time | $T_{SC}$ | 33 | ② | ② | µs | |
| FAULT RESET Active Time (High) | $T_{FR}$ | 8.0 | | 10 | µs | |
| $US_{0,1}$ Hold Time After SEEK | $T_{SU}$ | 15 | | | µs | 8 MHz Clock Period |
| Seek Hold Time from DIR | $T_{DS}$ | 30 | | | µs | |
| DIR Hold Time after STEP | $T_{STD}$ | 24 | | | µs | |
| Index Pulse Width | $T_{IDX}$ | 10 | | | $\phi_{CY}$ | |
| $\overline{RD}$ ↓ Delay from DRQ | $T_{MR}$ | 800 | | | ns | 8 MHz Clock Period |
| $\overline{WR}$ ↓ Delay from DRQ | $T_{MW}$ | 250 | | | ns | |
| $\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑ | $T_{MRW}$ | | | 12 | µs | |

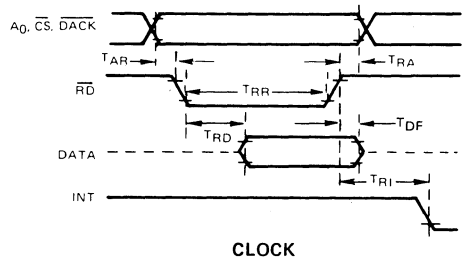
**NOTES:** ① Typical values for $T_a = 25°C$ and nominal supply voltage.
② Under Software Control. The range is from 1 ms to 16 ms for 8" floppies, and 2 to 32 ms for 5¼" floppies.

# TIMING DIAGRAMS

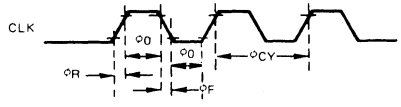
## PROCESSOR WRITE OPERATION



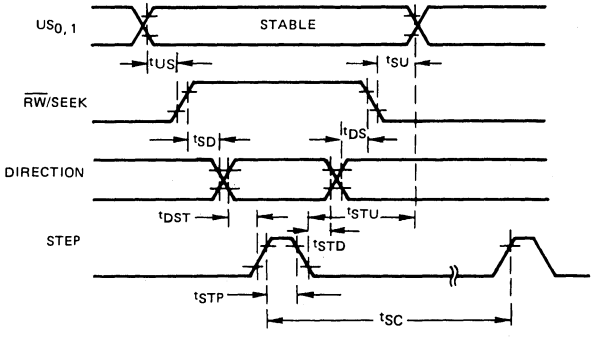

## PROCESSOR READ OPERATION



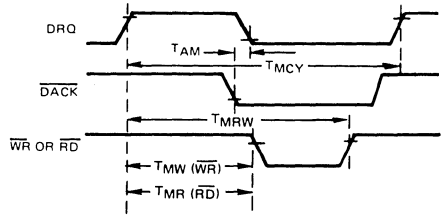

## CLOCK



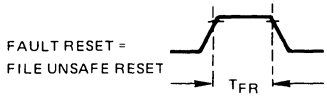

## SEEK OPERATION



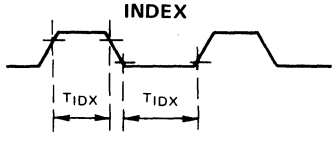

## DMA OPERATION



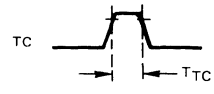

## FLT RESET



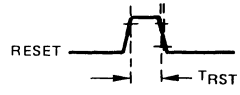

## INDEX




## TERMINAL COUNT




## RESET




For more information, please consult:
Technical Note 6-1 (Digital Data Separation)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# FDC 9267

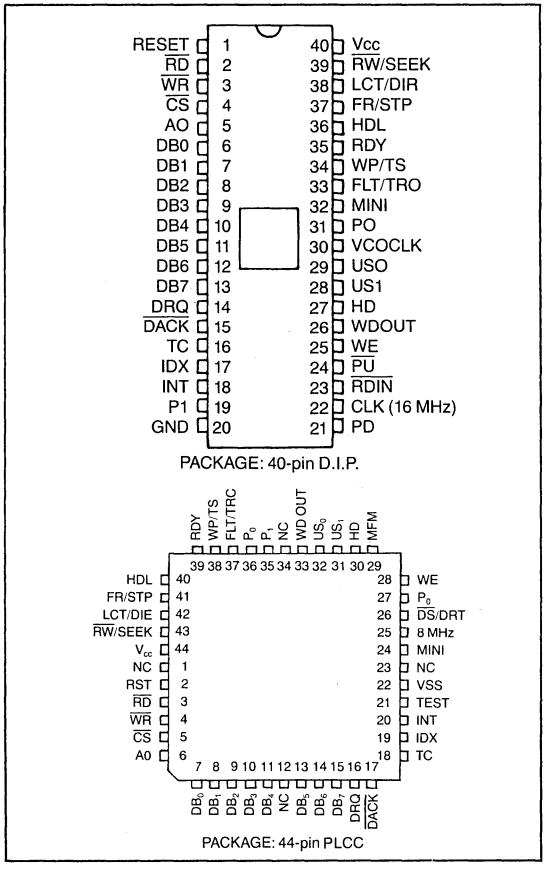
**PRELIMINARY**

# Single/Double Density Floppy Disk Controller With High Performance Analog Data Separator

## FEATURES

- ☐ IBM Compatible in both Single and Double Density Recording Formats
- ☐ High Performance self tuning Analog Data Separator
- ☐ Software compatible with Industry Standard FDC 765A
- ☐ Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- ☐ Multi-Sector and Multi-Track Transfer Capacity
- ☐ Drive Up to 4 Floppy Disks
- ☐ Data Scan Capability - will scan a Single Sector or an entire cylinder's worth of data fields, comparing on a Byte to Byte Basis, data in the Processor's Memory with data read from the Diskette
- ☐ Data Transfer in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on up to four drives
- ☐ Compatible with Most Microprocessors
- ☐ Single Phase 16 MHz Clock
- ☐ Single +5 Volt Power Supply
- ☐ Available in 40-Pin Dual-in-Line Package
- ☐ COPLAMOS®n-Channel Silicon Gate Technology

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The FDC 9267 is an enhanced floppy disk controller that integrates the SMC 765A Floppy Disk Controller with a high performance data separator. The controller portion contains the circuitry for interfacing a micro-processor to four floppy disk drives. The high performance, self tuning analog data separator is capable of recovering data with 2μs, 4μs and 8μs bit cells. This allows the device to be used in systems with 3.5", 5.25" or 8" drives that are single or double sided using FM or MFM encoding.

The FDC 9267 is 100% software compatible with the industry standard SMC FDC 765A. This ensures full diskette and system level compatibility.

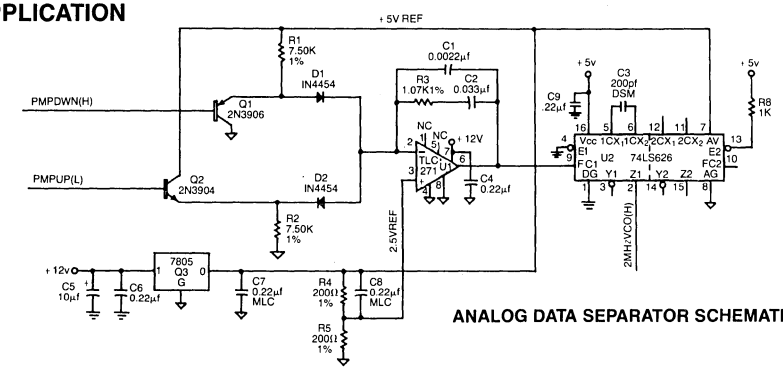
The FDC 9267 provides hand-shaking signals for DMA purposes. It will operate in DMA or non-DMA mode. In non-DMA mode an interrupt is generated each time a byte is available.

There are 15 commands the FDC 9267 is capable of performing. Each command requires multiple byte transfers to specify the operation. The following commands are available:

| | |
|---|---|
| Read Data | Write Data |
| Read ID | Format Track |
| Read Deleted Data | Write Deleted Data |
| Read Track | Seek |
| Scan Equal | Scan High or Equal |
| Scan Low or Equal | Sense Drive Status |
| Specify Sense | Interrupt Status |
| Recalibrate | |

SECTION VI

## TYPICAL APPLICATION




ANALOG DATA SEPARATOR SCHEMATIC

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | RESET | RESET | This input, when high, places the FDC 9267 into an idle state and forces the output signals to the floppy drive low. Reset does not affect SRT, HUT or HLT in Specify command. If the RDY pin is held high during reset, the FDC 9267 will generate an interrupt 1.024ms later. To clear this interrupt use the Sense Interrupt Status Command. |
| 2 | READ | $\overline{RD}$ | This input, when low, allows data to transfer from the FDC 9267 to the data bus. |
| 3 | WRITE | $\overline{WR}$ | This input, when low, allows data to transfer from the data bus to the FDC 9267. |
| 4 | CHIP SELECT | $\overline{CS}$ | This input, when low, selects the FDC 9267 thus enabling RD and WR. |
| 5 | ADDRESS 0 | A0 | This input, when high, allows the data register to be read or written. When low, it allows the status register to be read. |
| 6, 7, 8, 9, 10, 11, 12, 13 | DATA BUS 0-7 | DB0-7 | Bi-directional 8 bit data bus. |
| 14 | DMA REQUEST | DRQ | This output, when high, indicates that the FDC 9267 is requesting a DMA transfer. To allow easier system interfacing, and to insure full compatibility, DRQ is typically active 1µs prior to the data byte being available (during disk read operations). |
| 15 | DMA ACKNOWLEDGE | $\overline{DACK}$ | This input, when low, indicates to the FDC 9267 that a DMA request is being acknowledged. |
| 16 | TERMINAL COUNT | TC | When high, this input indicates the termination of a DMA, polled, or interrupt driven transfer. It terminates data transfer during READ/ WRITE/SCAN command in DMA or interrupt mode. |
| 17 | INDEX | IDX | This input, when high, informs the FDC 9267 of the beginnning of the disk track. |
| 18 | INTERRUPT | INT | This output, when high, indicates the FDC 9267 is requesting an interrupt. |
| 19 | PRECOMP 1 | P1 | Input used to select desired precompensation value. Refer to table 6. |
| 20 | GROUND | GND | |
| 21 | PUMPDOWN | PD | This output, when high, causes the VCO frequency to decrease. |
| 22 | CLOCK | CLK | This input is a 16mhz square wave clock. |
| 23 | RAW DATA IN | $\overline{RDIN}$ | This input is the raw read data from the floppy drive. |
| 24 | PUMP UP | $\overline{PU}$ | This output, when low, causes the VCO frequency to increase. |
| 25 | WRITE ENABLE | WE | This output, when high, enables the floppy disk drive to write data. |
| 26 | WRITE DATA OUT | WDOUT | This output is the precompensated serial data signal to the floppy disk drive. |
| 27 | HEAD SELECT | HD | When high, this outputs selects head 1. When low, head 2 is selected. |
| 28, 29 | UNIT SELECT | US1-0 | These two outputs are the encoded form of unit select 0 thru 3. |
| 30 | VCO CLOCK | VCOCLK | This input is the VCO signal from the VCO. The VCO frequency is nominally 2 mHz. |
| 31 | PRECOMP 0 | P0 | Input used to select desired precompensation value. Refer to table 6. |
| 32 | MINI | MINI | This input, when high, configures the FDC 9267 for operation with floppy disk data rates of 125 Kbs or 250 Kbs. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 33 | FAULT/TRACK 0 | FLT/TR0 | This input senses floppy disk drive fault conditions in read/write mode; and track 0 in seek mode. |
| 34 | WRITE PROTECT TWO SIDED | WP/TS | This input senses write protect status in the read/write mode; and two sided media in the seek mode. |
| 35 | READY | RDY | When high, this input indicates the floppy disk drive is ready for transfers. |
| 36 | HEAD LOAD | HDL | When high, this output causes the floppy disk read/write head to contact the disk. |
| 37 | FAULT RESET/STEP | FR/STP | When high and in the read/write mode this output will reset the fault flip flop. In the seek mode this output is used to step the head. |
| 38 | LOW CURRENT/ DIRECTION | LCT/DIR | In the read/write mode, this output lowers the write current when writing on the inner tracks. In the seek mode, this output determines the direction the head will step. A fault reset pulse is issued at the beginning of each read or write command prior to the occurance of the head load signal. |
| 39 | READ WRITE/SEEK | $\overline{RW}$/SEEK | When this output is high the seek mode is selected. When low, the read/write mode is selected. |
| 40 | POWER | Vcc | |

NOTE: For optimum performance, stray capacitance (on the printed circuit board) must be minimized between the PUMPDOWN and the PUMPUP pins. Printed circuit board traces to these pins should be as short and as symetrical as possible.

## DESCRIPTION OF INTERNAL REGISTERS

The FDC 9267 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and used to facilitate the transfer of data between the processor and FDC.

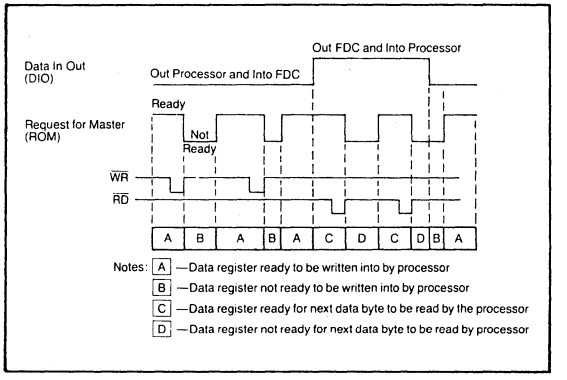
The relationship between the Status Data Registers and the signals $\overline{RD}$, $\overline{WR}$, and $A_0$ is shown below.

| $A_0$ | $\overline{RD}$ | $\overline{WR}$ | FUNCTION |
|---|---|---|---|
| 0 | 0 | 1 | Read Main Status Register |
| 0 | 1 | 0 | Illegal |
| 0 | 0 | 0 | Illegal |
| 1 | 0 | 0 | Illegal |
| 1 | 0 | 1 | Read from Data Register |
| 1 | 1 | 0 | Write into Data Register |

The bits in the Main Status Register are defined as follows:

| BIT NUMBER | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| $DB_0$ | FDD 0 Busy | $D_0B$ | FDD number 0 is in the Seek mode. If any of the bits are set FDC will not accept read or write command. |
| $DB_1$ | FDD 1 Busy | $D_1B$ | FDD number 1 is in the Seek mode. If any of the bits are set FDC will not accept read or write command. |
| $DB_2$ | FDD 2 Busy | $D_2B$ | FDD number 2 is in the Seek mode. If any of the bits are set FDC will not accept read or write command. |
| $DB_3$ | FDD 3 Busy | $D_3B$ | FDD number 3 is in the Seek mode. If any of the bits are set FCC will not accept read or write command. |
| $DB_4$ | FDC Busy | CB | A read or write command is in process. FDC will not accept any other command. |
| $DB_5$ | Execution Mode | EXM | This bit is set only during execution phase in non-DMA mode. When $DB_5$ goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation. |
| $DB_6$ | Data Input/Output | DIO | Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register. |
| $DB_7$ | Request for Master | RQM | Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor. |

DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. When MINI is low, the max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12μs. For this reason, every time Main Status Register is read the CPU should wait 12μs. The max time from the trailing edge of the last $\overline{RD}$ in the phase to when DB4 (FDC Busy) goes low is 12μs. These times must be doubled (to 24μs) when MINI is high.




## COMMAND SEQUENCE

The FDC is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

## COMMAND SYMBOL DESCRIPTION

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| $A_0$ | Address Line 0 | $A_0$ controls selection of Main Status Register ($A_0$ = 0) or Data Register ($A_0$ = 1). |
| C | Cylinder Number | C stands for the current/selected Cylinder (track) number 0 through 76 of the medium. |
| D | Data | D stands for the data pattern which is going to be written into a Sector. |
| $D_7$-$D_0$ | Data Bus | 8-bit Data Bus, where $D_7$ stands for a most significant bit, and $D_0$ stands for a least significant bit. |
| DTL | Data Length | When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector. |
| EOT | End of Track | EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop data transfer after a sector # equal to EOT. |
| GPL | Gap Length | GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3. |
| H | Head Address | H stands for head number 0 or 1, as specified in ID field. |
| HD | Head | HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.) |
| HLT | Head Load Time | HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments). |
| HUT | Head Unload Time | HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments). |
| MF | FM or MFM Mode | If MF is low, FM mode is selected, and if it is high, MFM mode is selected. |
| MT | Multi-Track | If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1. |
| N | Number | N stands for the number of data bytes written in a Sector. |
| NCN | New Cylinder Number | NCN stands for a New Cylinder Number, which is going to be reached as a result of the Seek operation. Desired position of Head. |
| ND | Non-DMA Mode | ND stands for operation in the Non-DMA Mode. |
| PCN | Present Cylinder Number | PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time. |
| R | Record | R stands for the Sector number, which will be read or written. |
| R/W | Read/Write | R/W stands for either Read (R) or Write (W) signal. |
| SC | Sector | SC indicates the number of Sectors per Cylinder. |
| SK | Skip | SK stands for Skip Deleted Data Address Mark. |
| SRT | Step Rate Time | SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.). |
| ST 0<br>ST 1<br>ST 2<br>ST 3 | Status 0<br>Status 1<br>Status 2<br>Status 3 | ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0$ = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command. |
| STP | | During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared. |
| US0, US1 | Unit Select | US stands for a selected drive number 0 or 1. |

## INSTRUCTION SET ① ②

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 0 | 1 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | SK | 0 | 1 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 0 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the main-system and FDD |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **WRITE DELETED DATA** | | | | | | | | | | |
| Command | W | MT | MF | 0 | 0 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk. |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | SK | 0 | 0 | 0 | 1 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | DTL | | | | | | | | |
| Execution | | | | | | | | | | Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT. |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **READ ID** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 0 | 1 | 0 | Commands |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Execution | | | | | | | | | | The first correct ID information on the Cylinder is stored in Data Register |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information read during Execution Phase from Floppy Disk |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **FORMAT A TRACK** | | | | | | | | | | |
| Command | W | 0 | MF | 0 | 0 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | N | | | | | | | | Bytes/Sector |
| | W | SC | | | | | | | | Sectors/Track |
| | W | GPL | | | | | | | | Gap 3 |
| | W | D | | | | | | | | Filler Byte |
| Execution | | | | | | | | | | FDC formats an entire track |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | In this case, the ID information has no meaning |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 0 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior to Command execution |
| | W | H | | | | | | | | |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after Command execution |
| | R | ST 1 | | | | | | | | |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after Command execution |
| | R | H | | | | | | | | |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

**Note:** ① Symbols used in this table are described at the end of this section.

② $A_0$ should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

SECTION VI

## INSTRUCTION SET (CONT.)

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **SCAN LOW OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 0 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior |
| | W | H | | | | | | | | Command execution |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after |
| | R | ST 1 | | | | | | | | Command execution |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after |
| | R | H | | | | | | | | Command execution |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |
| **SCAN HIGH OR EQUAL** | | | | | | | | | | |
| Command | W | MT | MF | SK | 1 | 1 | 1 | 0 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | C | | | | | | | | Sector ID information prior |
| | W | H | | | | | | | | Command execution |
| | W | R | | | | | | | | |
| | W | N | | | | | | | | |
| | W | EOT | | | | | | | | |
| | W | GPL | | | | | | | | |
| | W | STP | | | | | | | | |
| Execution | | | | | | | | | | Data-compared between the FDD and main-system |
| Result | R | ST 0 | | | | | | | | Status information after |
| | R | ST 1 | | | | | | | | Command execution |
| | R | ST 2 | | | | | | | | |
| | R | C | | | | | | | | Sector ID information after |
| | R | H | | | | | | | | Command execution |
| | R | R | | | | | | | | |
| | R | N | | | | | | | | |

| PHASE | R/W | DATA BUS $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | REMARKS |
|---|---|---|---|---|---|---|---|---|---|---|
| **RECALIBRATE** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | 0 | US1 | US0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 |
| **SENSE INTERRUPT STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command Codes |
| Result | R | STO | | | | | | | | Status information at the end |
| | R | PCN | | | | | | | | of seek-operation about the FDC |
| **SPECIFY** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command Codes |
| | W | SRT | | | | | | | HUT | |
| | W | HLT | | | | | | | ND | |
| **SENSE DRIVE STATUS** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| Result | R | ST 3 | | | | | | | | Status information about FDD |
| **SEEK** | | | | | | | | | | |
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command Codes |
| | W | X | X | X | X | X | HD | US1 | US0 | |
| | W | NCN | | | | | | | | |
| Execution | | | | | | | | | | Head is positioned over proper Cylinder on Diskette |
| **INVALID** | | | | | | | | | | |
| Command | W | Invalid Codes | | | | | | | | Invalid Command Codes (NoOp – FDC goes into Standby State) |
| Result | R | ST 0 | | | | | | | | ST 0 = 80 (16) |

## FUNCTIONAL DESCRIPTION OF COMMANDS

### Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

| Multi-Track MT | MFM/FM MF | Bytes/Sector N | Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors) | Final Sector Read from Diskette |
|---|---|---|---|---|
| 0 | 0 | 00 | (128) (26) = 3,328 | 26 at Side 0 |
| 0 | 1 | 01 | (256) (26) = 6,656 | or 26 at Side 1 |
| 1 | 0 | 00 | (128) (52) = 6,656 | 26 at Side 1 |
| 1 | 1 | 01 | (256) (52) = 13,312 | |
| 0 | 0 | 01 | (256) (15) = 3,840 | 15 at Side 0 |
| 0 | 1 | 02 | (512) (15) = 7,680 | or 15 at Side 1 |
| 1 | 0 | 01 | (256) (30) = 7,680 | 15 at Side 1 |
| 1 | 1 | 02 | (512) (30) = 15,360 | |
| 0 | 0 | 02 | (512) (8) = 4,096 | 8 at Side 0 |
| 0 | 1 | 03 | (1024) (8) = 8,192 | or 8 at Side 1 |
| 1 | 0 | 02 | (512) (16) = 8,192 | 8 at Side 1 |
| 1 | 1 | 03 | (1024) (16) = 16,384 | |

**Table 1. Transfer Capacity**

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode*, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the value for C, H, R, and N, when the processor terminates the Command.

| MT | HD | Final Sector Transferred to Processor | ID Information at Result Phase | | | |
|---|---|---|---|---|---|---|
| | | | C | H | R | N |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | NC | R = 01 | NC |
| 0 | 0 | Less than EOT | NC | NC | R + 1 | NC |
| | 0 | Equal to EOT | NC | LSB | R = 01 | NC |
| | 1 | Less than EOT | NC | NC | R + 1 | NC |
| | 1 | Equal to EOT | C + 1 | LSB | R = 01 | NC |

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

SECTION VI

## Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

## Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

## Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

## Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire

*Time refers to 8" mode (MINI = low). When using 5.25" mode, these times are doubled.

| Format | Sector Size | N | SC | GPL① | GPL②③ |
|---|---|---|---|---|---|
| 8″ Standard Floppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 1A | 07 | 1B |
| | 256 | 01 | 0F | 0E | 2A |
| | 512 | 02 | 08 | 1B | 3A |
| | 1024 | 03 | 04 | 47 | 8A |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 1A | 0E | 36 |
| | 512 | 02 | 0F | 1B | 54 |
| | 1024 | 03 | 08 | 35 | 74 |
| | 2048 | 04 | 04 | 99 | FF |
| | 4096 | 05 | 02 | C8 | FF |
| | 8192 | 06 | 01 | C8 | FF |
| 5¼″ Minifloppy | | | | | |
| FM Mode | 128 bytes/sector | 00 | 12 | 07 | 09 |
| | 128 | 00 | 10 | 10 | 19 |
| | 256 | 01 | 08 | 18 | 30 |
| | 512 | 02 | 04 | 46 | 87 |
| | 1024 | 03 | 02 | C8 | FF |
| | 2048 | 04 | 01 | C8 | FF |
| MFM Mode ④ | 256 | 01 | 12 | 0A | 0C |
| | 256 | 01 | 10 | 20 | 32 |
| | 512 | 02 | 08 | 2A | 50 |
| | 1024 | 03 | 04 | 80 | F0 |
| | 2048 | 04 | 02 | C8 | FF |
| | 4096 | 05 | 01 | C8 | FF |
| 3½″ Sony Micro Floppydisk® | | | | | |
| FM Mode | 128 bytes/sector | 0 | 0F | 07 | 1B |
| | 256 | 1 | 09 | 0E | 2A |
| | 512 | 2 | 05 | 1B | 3A |
| MFM Mode ④ | 256 | 1 | 0F | 0E | 36 |
| | 512 | 2 | 09 | 1B | 54 |
| | 1024 | 3 | 05 | 35 | 74 |

*Table 3*

**Notes:** ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
② Suggested values of GPL in format command.
③ All values except sector size and hexidecimal.
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

### Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

### Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

## Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} \leq D_{PROCESSOR}$, or $D_{FDD} \geq D_{PROCESSOR}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

| COMMAND | STATUS REGISTER 2 | | COMMENTS |
|---|---|---|---|
| | BIT 2 = SN | BIT 3 = SH | |
| Scan Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} \neq D_{PROCESSOR}$ |
| Scan Low or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} < D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| Scan High or Equal | 0 | 1 | $D_{FDD} = D_{PROCESSOR}$ |
| | 0 | 0 | $D_{FDD} > D_{PROCESSOR}$ |
| | 1 | 0 | $D_{FDD} < D_{PROCESSOR}$ |

**Table 4**

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode)*. If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

### Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits $DB_0$-$DB_3$ in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

### Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

### Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This com-

*Time refers to 8″ mode (MINI = low). When using 5.25″ mode, these times are doubled.

mand when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

| SEEK END BITS 5 | INTERRUPT CODE BIT 6 | INTERRUPT CODE BIT 7 | CAUSE |
|---|---|---|---|
| 0 | 1 | 1 | Ready Line changed state, either polarity |
| 1 | 0 | 0 | Normal Termination of Seek or Recalibrate Command |
| 1 | 1 | 0 | Abnormal Termination of Seek or Recalibrate Command |

**Table 5**

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

## Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 0 = 32 ms...OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time interval mentioned above is a direct function of the MINI (pin 32). Times indicated above are for MINI set to 0. In a mini floppy application all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

## Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

## Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC 9267 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC 9267 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

## STATUS REGISTER IDENTIFICATION

| BIT NO. | BIT NAME | BIT SYMBOL | DESCRIPTION |
|---|---|---|---|
| $D_7$ $D_6$ | Interrupt Code | IC | $D_7 = 0$ and $D_6 = 0$<br>Normal Termination of Command, (NT). Command was completed and properly executed. |
| | | | $D_7 = 0$ and $D_6 = 1$<br>Abnormal Termination of Command, (AT).<br>Execution of Command was started, but was not successfully completed. |
| | | | $D_7 = 1$ and $D_6 = 0$<br>Invalid Command issue, (IC). Command which was issued was never started. |
| | | | $D_7 = 1$ and $D_6 = 1$<br>Abnormal Termination because during command execution the ready signal from FDD changed state. |
| $D_5$ | Seek End | SE | When the FDC completes the SEEK Command, this flag is set to 1 (high). |
| $D_4$ | Equipment Check | EC | If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set. |
| $D_3$ | Not Ready | NR | When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set. |
| $D_2$ | Head Address | HD | This flag is used to indicate the state of the head at Interrupt. |
| $D_1$ | Unit Select 1 | US 1 | These flags are used to indicate a Drive Unit. Number at Interrupt. |
| $D_0$ | Unit Select 0 | US 0 | |

| BIT NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| | | | **STATUS REGISTER 1 (CONT.)** |
| $D_7$ | End of Cylinder | EN | When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set. |
| $D_6$ | | | Not used. This bit is always 0 (low). |
| $D_5$ | Data Errror | DE | When the FDC detects a CRC error in either the ID field or the data field, this flag is set. |
| $D_4$ | Over Run | OR | If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set. |
| $D_3$ | | | Not used. This bit always 0 (low). |
| $D_2$ | No Data | ND | During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set. |
| | | | During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set. |
| | | | During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set. |
| $D_1$ | Not Writable | NW | During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set. |
| $D_0$ | Missing Address Mark | MA | If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. |
| | | | If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set. |
| | | | **STATUS REGISTER 2** |
| $D_7$ | | | Not used. This bit is always 0 (low). |
| $D_6$ | Control Mark | CM | During executing the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set. |
| $D_5$ | Data Error in Data Field | DD | If the FDC detects a CRC error in the data field then this flag is set. |
| $D_4$ | Wrong Cylinder | WC | This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set. |
| $D_3$ | Scan Equal Hit | SH | During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set. |
| $D_2$ | Scan Not Satisfied | SN | During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set. |
| $D_1$ | Bad Cylinder | BC | This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set. |
| $D_0$ | Missing Address Mark in Data Field | MD | When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set. |
| | | | **STATUS REGISTER 3** |
| $D_7$ | Fault | FT | This bit is used to indicate the status of the Fault signal from the FDD. |
| $D_6$ | Write Protected | WP | This bit is used to indicate the status of the Write Protected signal from the FDD. |
| $D_5$ | Ready | RY | This bit is used to indicate the status of the Ready signal from the FDD. |
| $D_4$ | Track 0 | T0 | This bit is used to indicate the status of the Track 0 signal from the FDD. |
| $D_3$ | Two Side | TS | This bit is used to indicate the status of the Two Side signal from the FDD. |
| $D_2$ | Head Address | HD | This bit is used to indicate the status of Side Select signal to the FDD. |
| $D_1$ | Unit Select 1 | US 1 | This bit is used to indicate the status of the Unit Select 1 signal to the FDD. |
| $D_0$ | Unit Select 0 | US 0 | This bit is used to indicate the status of the Unit Select 0 signal to the FDD. |

## PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written in the FDC 9267. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the FDC 9267. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the FDC 9267 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the FDC 9267 is in the NON-DMA Mode, then the receipt of each data byte (if FDC 9267 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the FDC 9267 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The FDC 9267 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC 9267 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

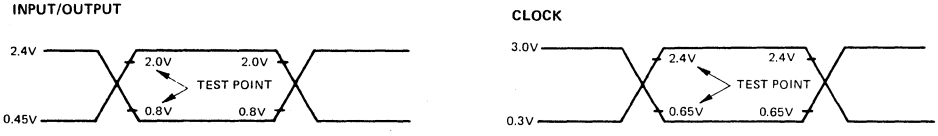
The FDC 9267 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the FDC 9267 to form the Command Phase, and are read out of the FDC 9267 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the FDC 9267, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the FDC 9267 is ready for a new command.

## POLLING FEATURE OF THE FDC9267

After the Specify command has been sent to the FDC 9267, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the FDC 9267 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the FDC 9267 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the FDC 9267 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

## AC TEST CONDITION




## AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

## PRECOMPENSATION

The desired precompensation delay is determined by the state of the MINI, P0 and P1 inputs. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive.

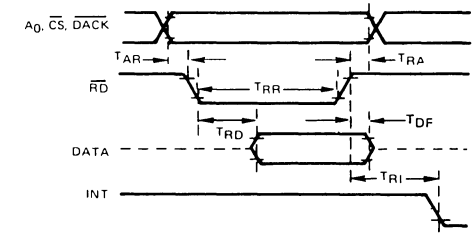
NOTE: The duration of the write pulse from pin 26 (WDOUT) is to be a minimum of 250ns. for all precomp values.

| MINI | P1 | P0 | PRECOMP |
|---|---|---|---|
| 0 | 0 | 0 | 0.0ns |
| 0 | 0 | 1 | 62.5ns |
| 0 | 1 | 0 | 125.0ns |
| 0 | 1 | 1 | 187.5ns |
| 1 | 0 | 0 | 0.0ns |
| 1 | 0 | 1 | 125.0ns |
| 1 | 1 | 0 | 250.0ns |
| 1 | 1 | 1 | 375.0ns |

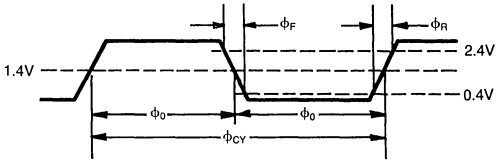
**TABLE 6**
**WRITE PRECOMPENSATION VALUE SELECTION**

## TIMING DIAGRAMS

### PROCESSOR READ OPERATION




### CLOCK



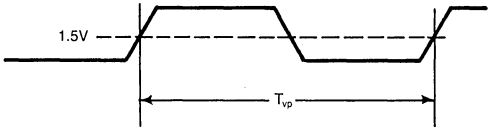




**FIGURE 1: VCOCLK TIMING**

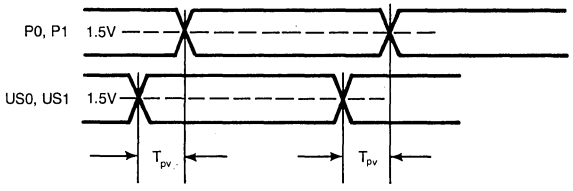



**FIGURE 2: PRECOMP VALUE TIMING**

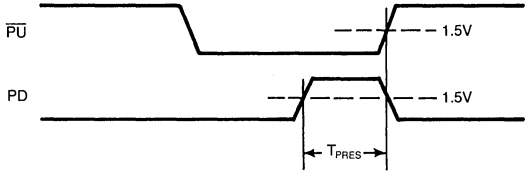



**FIGURE 3: PUMPUP TO PUMPDOWN TIMING**

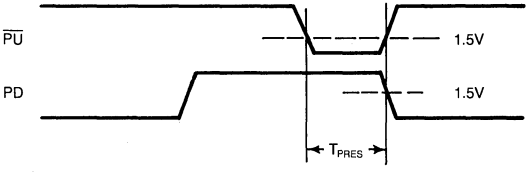



**FIGURE 4: PUMPDOWN TO PUMPUP TIMING**

SECTION VI

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.3 to +7 Volts
Supply Voltage $V_{CC}$ ..... −0.3 to +7 Volts
Power Dissipation ..... 1 Watt
$T_a$ = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC CHARACTERISTICS** $T_a$ = 0°C to +70°C; $V_{CC}$ = +5V ±5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP① | MAX | | |
| Input Low Voltage | $V_{IL}$ | −0.3 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$ + 0.5 | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 2.0 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | $V_{CC}$ | V | $I_{OH}$ = −200 μA |
| Input Low Voltage (CLK) | $V_{IL(\phi)}$ | −0.3 | | 0.65 | V | |
| Input High Voltage (CLK) | $V_{IH(\phi)}$ | 2.4 | | $V_{CC}$ + 0.5 | V | |
| $V_{CC}$ Supply Current | $I_{CC}$ | | | 200 | mA | |
| Input Load Current (All Input Pins) | $I_{LI}$ | | | 10 | μA | $V_{IN}$ = $V_{CC}$ |
| | | | | −10 | μA | $V_{IN}$ = 0V |
| High Level Output Leakage Current | $I_{LOH}$ | | | 10 | μA | $V_{OUT}$ = $V_{CC}$ |
| Low Level Output Leakage Current | $I_{LOL}$ | | | −10 | μA | $V_{OUT}$ = +0.45V |

NOTE: ①Typical values for $T_a$ = 25°C and nominal supply voltage.

**DC CHARACTERISTICS** $T_a$ = 25°C; $f_c$ = 1 MHz; $V_{CC}$ = 0V

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Clock Input Capacitance | $C_{IN(\phi)}$ | | | 20 | pF | All Pins Except Pin Under Test Tied to AC Ground |
| Input Capacitance | $C_{IN}$ | | | 10 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 20 | pF | |

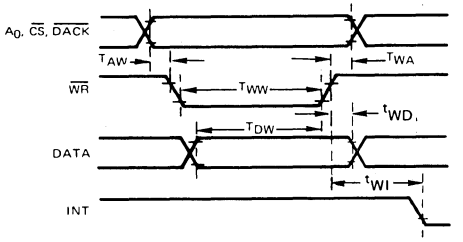
**AC CHARACTERISTICS** $T_a$ = 0°C to +70°C; $V_{cc}$ = +5V ± 5% unless otherwise specified.

| PARAMETER | SYMBOL | LIMITS | | | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP① | MAX | | |
| Clock period<br>Clock Active (High, Low) | $\phi_{CY}$<br>$\phi_0$ | 58<br>40% | 62.5 | 250<br>60% | ns | |
| Clock Rise Time | $\phi_r$ | | | 10 | ns | |
| Clock Fall Time | $\phi_f$ | | | 10 | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓ | $T_{AR}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑ | $T_{RA}$ | 0 | | | ns | |
| $\overline{RD}$ Width | $T_{RR}$ | 250 | | | ns | |
| Data Access Time from $\overline{RD}$ ↓ | $T_{RD}$ | | | 200 | ns | $C_L$ = 100 pF |
| DB to Float Delay Time from $\overline{RD}$ ↑ | $T_{DF}$ | 20 | | 100 | ns | $C_L$ = 100 pF |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Set Up time to $\overline{WR}$↓ | $T_{AW}$ | 0 | | | ns | |
| $A_0$, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑ | $T_{WA}$ | 0 | | | ns | |
| $\overline{WR}$ Width | $T_{WW}$ | 250 | | | ns | |
| Data Set Up Time to $\overline{WR}$ ↑ | $T_{DW}$ | 150 | | | ns | |
| Data Hold Time from $\overline{WR}$ ↑ | $T_{WD}$ | 5 | | | ns | |
| INT Delay Time from $\overline{RD}$ ↑ | $T_{RI}$ | | | 500 | ns | |
| INT Delay Time from $\overline{WR}$ ↑ | $T_{WI}$ | | | 500 | ns | |
| DRQ Cycle Time | $T_{MCY}$ | 13 | | | µs | |
| DRQ Delay Time from $\overline{DACK}$ ↓ | $T_{AM}$ | | | 200 | ns | |
| TC Width | $T_{TC}$ | 2 | | | $\phi_{CY}$ | |
| Reset Width | $T_{RST}$ | 28 | | | $\phi_{CY}$ | |
| RDD Active Time (High) | $T_{RDD}$ | 40 | | | ns | |
| Window Cycle Time | $T_{WCY}$ | | 2.0<br>1.0 | | µs | MFM = 0<br>MFM = 1 |
| Window Hold Time to/from RDD | $T_{RDW}$<br>$T_{WRD}$ | 15 | | | ns | |
| US, Hold Time to $\overline{RW}$/SEEK ↑ | $T_{US}$ | 12 | | | µs | 16 MHz Clock Period<br>MINI pin = 0 |
| SEEK RW Hold Time to LOW CURRENT/DIRECTION ↑ | $T_{SD}$ | 7 | | | µs | |
| LOW CURRENT DIRECTION Hold Time to FAULT RESET/STEP ↑ | $T_{DST}$ | 1.0 | | | µs | |
| US, Hold Time from FAULT RESET/ STEP ↑ | $T_{STU}$ | 5.0 | | | µs | |
| Step Active Time (High) | $T_{STP}$ | 6.0 | 7.0 | | µs | |
| Step Cycle Time | $T_{SC}$ | 33 | | | µs | |
| FAULT RESET Active Time (High) | $T_{FR}$ | 8.0 | | 10 | µs | |
| Write Data Width (WDOUT) | $T_{WDO}$ | 250 | | | ns | |
| US, Hold Time After SEEK | $T_{SU}$ | 15 | | | µs | 16 MHz Clock Period<br>MINI pin = 0 |
| Seek Hold Time from DIR | $T_{DS}$ | 30 | | | µs | |
| DIR Hold Time after STEP | $T_{STD}$ | 24 | | | µs | |
| Index Pulse Width | $T_{IDX}$ | 20 | | | $\phi_{CY}$ | |
| $\overline{WR}$↓, Delay from DRQ | $T_{MW}$ | 250 | | | ns | 16MHz Clock Period<br>MINI pin = 0 |
| $\overline{WE}$ or $\overline{RD}$ Response Time from DRQ↑ | $T_{MRW}$ | | | 12 | µs | |
| VCOCLK Period | $T_{vp}$ | .46 | .5 | .56 | µs | Figure 1 |
| Rise and Fall Times | | | | 10 | ns | Figure 1 |
| Unit Select to Valid PRECOMP Value | $T_{pv}$ | | | 100 | ns | Figure 2 |
| Pump Reset Time | $T_{pres}$ | | | 20 | ns | Figure 3 |
| Rise and Fall Times | | | | 10 | ns | Figure 3 |

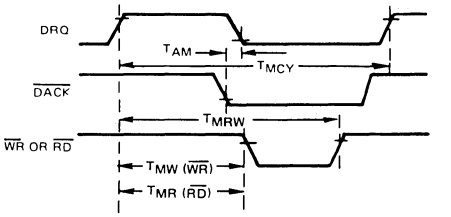
NOTES: ① Typical values for $T_a$ = 25°C and nominal supply voltage
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy
③ Sony microfloppy 3½" drive (8" compatible).
④ Sony microfloppy 3½" drive (5¼" compatible).

## TIMING DIAGRAMS

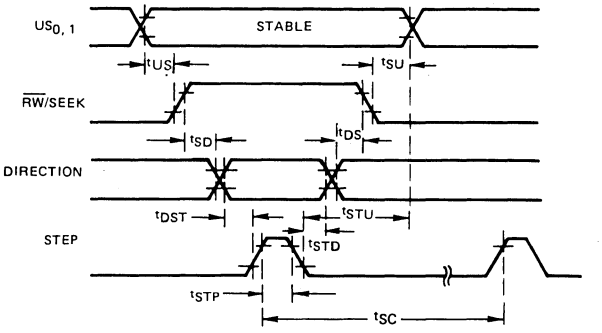
### PROCESSOR WRITE OPERATION



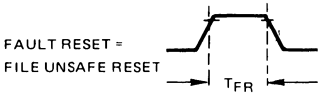

### DMA OPERATION



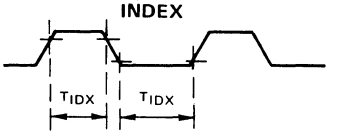

### SEEK OPERATION



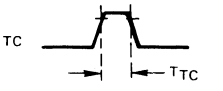

### FLT RESET



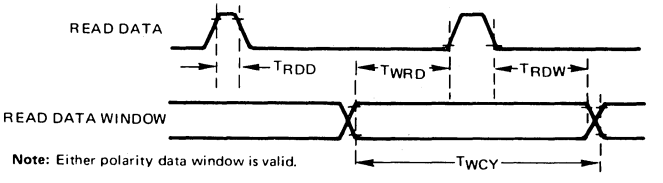

### INDEX




### TERMINAL COUNT




### FDD READ OPERATION




**Note:** Either polarity data window is valid.

### RESET


STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

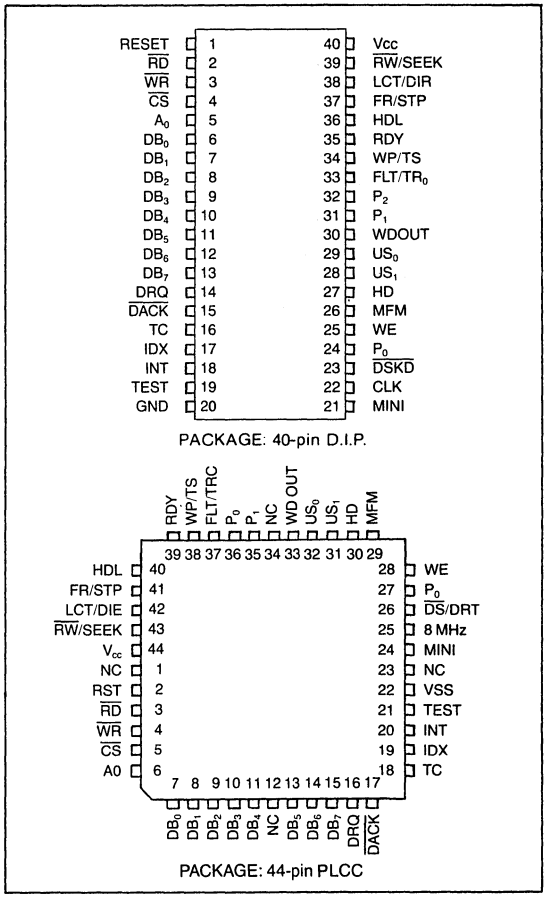
**FDC9268**
**PRELIMINARY**

# Integrated Single/Double Density Floppy Disk Controller

## FEATURES

- ☐ Combination Floppy Disk Controller and Floppy Disk Interface
- ☐ Software compatible with industry standard FDC765A
- ☐ On chip digital data separator eliminates critical analog adjustments
- ☐ IBM compatible in both single and double density recording formats
- ☐ Programmable data record lengths: 128, 256, 512, or 1024 bytes/sector
- ☐ Multi-sector and multi-track transfer capability
- ☐ Controls up to 4 floppy disk drives
- ☐ Data Scan Capability–will scan a single sector or entire track's worth of data fields, comparing on a byte to byte basis, data in the processors memory with the data read from the diskette
- ☐ Data transfer in DMA or non-DMA mode
- ☐ Single 16 MHz TTL clock input
- ☐ Parallel seek operations on up to 4 drives
- ☐ Compatible with most microprocessors
- ☐ COPLAMOS/n-channel silicon gate technology
- ☐ Available in 40-pin Dual-In-Line and 44-pin PLCC packages

## PIN CONFIGURATION




PACKAGE: 40-pin D.I.P.




PACKAGE: 44-pin PLCC

SECTION VI

## GENERAL DESCRIPTION

The FDC9268 is a monolithic combination of the industry standard FDC765A Floppy Disk Controller and the FDC9239 Enhanced Floppy Disk Interface Circuit. It preserves all of the processor hardware and software interfaces to the 765A, and contains on-chip circuitry to simplify drive interfacing.

These on-chip enhancements include a digital data separator, compatible with 3.5", 5.25" and 8" floppy disk drives. The FDC9268 separates both FM (Single Density) and MFM (Double Density) encoded data. The FDC uses a high performance 16-bit cell divide algorithm which produces significant improvements in soft error rates over existing designs. The FDC9268's high performance is achieved without any external adjustments.

The FDC9268 also allows variable write precompensation, which is track selectable.

These enhancements greatly reduce the number of components required to interface floppy disks to a microprocessor system.

There are 15 commands which the FDC9268 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

| | |
|---|---|
| Read Data | Scan High or Equal |
| Format a Track | Sense Drive Status |
| Read a Track | Read ID |
| Recalibrate | Write Deleted Data |
| Scan Low or Equal | Scan Equal |
| Write Data | Sense Interrupt Status |
| Read Deleted Data | Specify |
| Seek | |

Address mark detection circuitry is internal to the FDC which simplifies the read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The FDC9268 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

## FDC9266 COMPATIBILITY

The FDC9268 is software and hardware compatible with the FDC9266 with the following qualifications pertaining to Precomp and clock input.

–A 16 MHz clock is used on the FDC9268.

–The precomp specifications for the FDC9267 and FDC9266 can be used for the FDC9268 with the following qualification. Whenever the precomp select line $P_2$ is active, the FDC9268 uses the maximum precomp available in that mode (i.e. 375 nsec in the 5-1/4″ mode and 187.5 nsec in the 8″ mode).

| MINI | $P_2$ | $P_1$ | $P_0$ | PRECOMP VALUE (nsec) |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 125.0 |
| 1 | 0 | 1 | 0 | 250.0 |
| 1 | 0 | 1 | 1 | 375.0 |
| 1 | 1 | 0 | 0 | 375.0 |
| 1 | 1 | 0 | 1 | 375.0 |
| 1 | 1 | 1 | 0 | 375.0 |
| 1 | 1 | 1 | 1 | 375.0 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 62.5 |
| 0 | 0 | 1 | 0 | 125.0 |
| 0 | 0 | 1 | 1 | 187.5 |
| 0 | 1 | 0 | 0 | 187.5 |
| 0 | 1 | 0 | 1 | 187.5 |
| 0 | 1 | 1 | 0 | 187.5 |
| 0 | 1 | 1 | 1 | 187.5 |

**Write Precompensation Value Selection**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

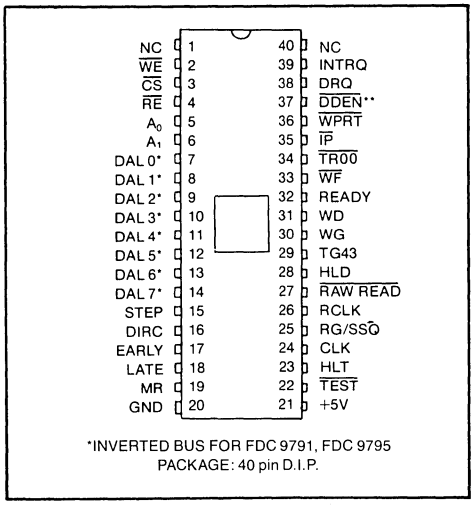
# FDC 9791
# FDC 9793
# FDC 9795
# FDC 9797
μPC FAMILY

# Floppy Disk Controller/Formatter FDC

## FEATURES

- ☐ +5 VOLT ONLY VERSION OF FDC179X-02
- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 9795, FDC 9797)
- ☐ WINDOW EXTENSION (IN MFM)

## PIN CONFIGURATION




*INVERTED BUS FOR FDC 9791, FDC 9795
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FDC 179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

## GENERAL DESCRIPTION

The FDC 979X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 979X chip design has evolved into four specific parts: FDC 9791, FDC 9793, FDC 9795, and the FDC 9797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8″ and 5¼″ (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

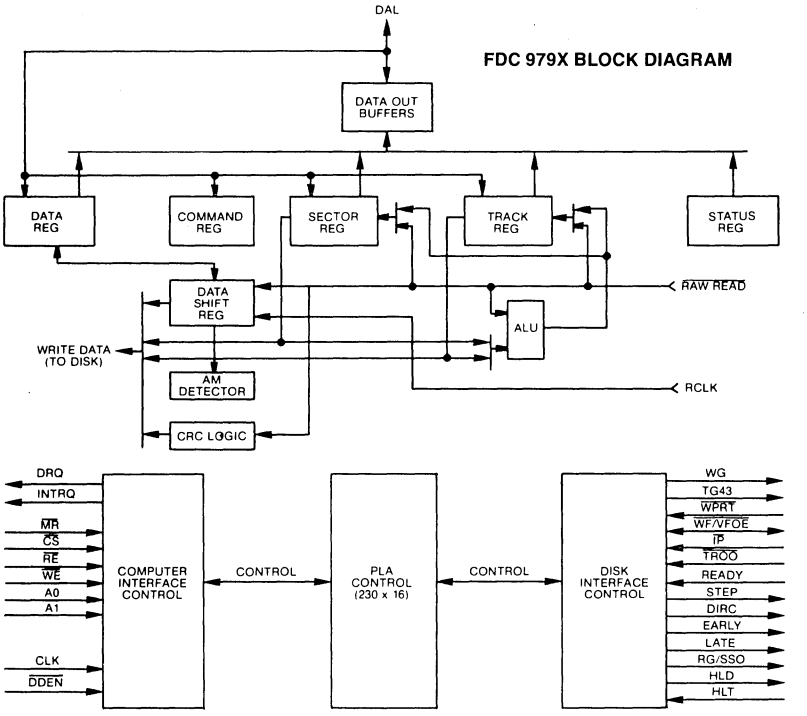
The FDC 9791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 9791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 9793 is identical to the FDC 9791 except the DAL lines are TRUE for systems that utilize true data busses.

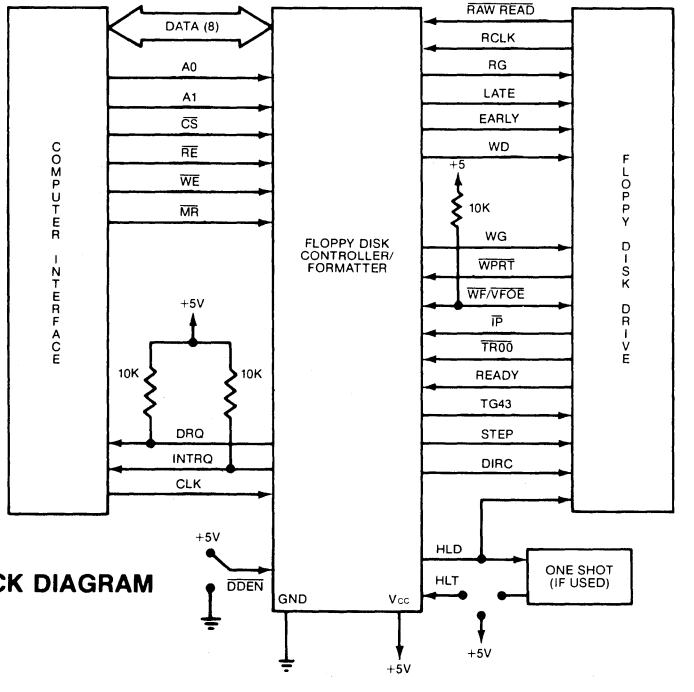
The FDC 9795 adds side select logic to the FDC 9791. The FDC 9797 adds the side select logic to the FDC 9793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

## FDC 979X BLOCK DIAGRAM




## SYSTEM BLOCK DIAGRAM



## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 1 | NO CONNECTION | NC | This pin is internally connected to the substrate bias generator and must be left open. |
| 20 | GROUND | $V_{SS}$ | Ground |
| 21 | POWER SUPPLY | $V_{CC}$ | +5V |
| 40 | NO CONNECTION | NC | This pin is not connected. |
| 19 | $\overline{\text{MASTER RESET}}$ | $\overline{\text{MR}}$ | A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register. |
| **COMPUTER INTERFACE:** | | | |
| 2 | $\overline{\text{WRITE ENABLE}}$ | $\overline{\text{WE}}$ | A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low. |
| 3 | $\overline{\text{CHIP SELECT}}$ | $\overline{\text{CS}}$ | A logic low on this input selects the chip and the parallel data bus (DAL). |
| 4 | $\overline{\text{READ ENABLE}}$ | $\overline{\text{RE}}$ | A logic low on this input controls the placement of data from a selected register on DALØ-DAL7 when $\overline{\text{CS}}$ is low. |
| 5,6 | REGISTER SELECT LINES | A0, A1 | These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control:<br>A1 \| A0 \| $\overline{\text{RE}}$ \| $\overline{\text{WE}}$<br>0 \| 0 \| Status Reg \| Command Reg<br>0 \| 1 \| Track Reg \| Track Reg<br>1 \| 0 \| Sector Reg \| Sector Reg<br>1 \| 1 \| Data Reg \| Data Reg |
| 7-14 | DATA ACCESS LINES | DAL0-DAL7 | Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{\text{WE}}$ or a transmitter enabled by $\overline{\text{RE}}$. The Data Bus is inverted on the FDC 9791, FDC 9792 and FDC 9795. |
| 24 | CLOCK | CLK | This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for 5¼" drives. |
| 38 | DATA REQUEST | DRQ | This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use a 10K pull-up resistor to +5V. |
| 39 | INTERRUPT REQUEST | INTRQ | This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V. |
| **FLOPPY DISK INTERFACE:** | | | |
| 15 | STEP | STEP | Step and direction motor control. The step output contains a pulse for each step. |
| 16 | DIRECTION | DIRC | Direction Output is active high when stepping in, active low when stepping out. |
| 17 | EARLY | EARLY | Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation. |
| 18 | LATE | LATE | Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation. |
| 22 | $\overline{\text{TEST}}$ | $\overline{\text{TEST}}$ | This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors. |
| 23 | HEAD LOAD TIMING | HLT | When a logic high is found on the HLT input the head is assumed to be engaged. |

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 25 | READ GATE (9791/3) | RG | A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization. |
| 25 | SIDE SELECT OUTPUT (9795, 9797) | SSO | The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S=1, SSO is set to a logic 1. When S=0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition. |
| 26 | READ CLOCK | RCLK | A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not. |
| 27 | $\overline{\text{RAW READ}}$ | $\overline{\text{RAW READ}}$ | The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition. |
| 28 | HEAD LOAD | HLD | The HLD output controls the loading of the Read-Write head against the media. |
| 29 | TRACK GREATER THAN 43 | TG43 | This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands. |
| 30 | WRITE GATE | WG | This output is made valid before writing is to be performed on the diskette. |
| 31 | WRITE DATA | WD | A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats. |
| 32 | READY | READY | This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7. |
| 33 | $\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$ | $\overline{\text{WF/VFOE}}$ | This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 9795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 9791/3, VFOE will remain low until the end of the Data Field. |
| 34 | $\overline{\text{TRACK 00}}$ | $\overline{\text{TR00}}$ | This input informs the FDC 979X that the Read/Write head is positioned over Track 00. |
| 35 | $\overline{\text{INDEX PULSE}}$ | $\overline{\text{IP}}$ | This input informs the FDC 979X when the index hole is encountered on the diskette. |
| 36 | $\overline{\text{WRITE PROTECT}}$ | $\overline{\text{WPRT}}$ | This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit. |
| 37 | $\overline{\text{DOUBLE DENSITY}}$ | $\overline{\text{DDEN}}$ | This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. |

## FUNCTIONAL DESCRIPTION

The FDC 979X major functional blocks are as follows:

**Data Shift Register**—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

**Data Register**—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

**Sector Register (SR)**—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

**Command Register (CR)**—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

**Status Register (STR)**—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

**CRC Logic**—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

**Track Register**—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

**Arithmetic/Logic Unit (ALU)**—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

**Timing and Control**—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

**AM Detector**—The address mark detector detects ID, data and index address marks during ready and write operations.



## OPERATION

FDC 9791, FDC 9793, FDC 9795 and FDC 9797 have two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}} = 1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10 and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

### Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1". For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0". Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 979X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC 979X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC 979X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" of "FF" are detected. The FDC 979X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 979X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is

transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

**Disk Write Operation**

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution against erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FDC 979X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FDC 979X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FDC 979X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$=1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$=0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FDC 979X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

## COMMAND WORDS

The FDC 979X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

**Table 1. Command Summary**

| | | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| COMMAND | TYPE | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Restore | I | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| Seek | I | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| Step | I | 0 | 0 | 1 | u | h | V | $r_1$ | $r_0$ |
| Step In | I | 0 | 1 | 0 | u | h | V | $r_1$ | $r_0$ |
| Step Out | I | 0 | 1 | 1 | u | h | V | $r_1$ | $r_0$ |
| Read Sector | II | 1 | 0 | 0 | m | $F_2$ | E | $F_1$ | 0 |
| Write Sector | II | 1 | 0 | 1 | m | $F_2$ | E | $F_1$ | $a_0$ |
| Read Address | III | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 |
| Read Track | III | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 |
| Write Track | III | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 |
| Force Interrupt | IV | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

### Type I Commands

The Type I Commands are Restore, Seek, Step, Step-In, and Step-Out. Each of the Type I Commands contains a rate field ($r_0r_1$), which determines the stepping motor rate as defined in Table 2.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FDC 979X receives a command that specifically disengages the head. If the FDC 979X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field if read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt

is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC 979X terminates the operation and sends an interrupt (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

On the FDC 9795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

**Restore (Seek Track 0)**

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. if $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the $r_1r_0$ field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FDC 979X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

**Seek**

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FDC 979X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step**

Upon receipt of this command, the FDC 979X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step-In**

Upon receipt of this command, the FDC 979X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

**Step-Out**

Upon receipt of this command, the FDC 979X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the $r_1r_0$ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of command. An interrupt is generated at the completion of the command.

**Head Positioning**

The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$=0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

**Step**—A 2 $\mu$s (MFM) or 4 $\mu$s (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

**Direction (DIRC)**—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 $\mu$s before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FDC 979X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

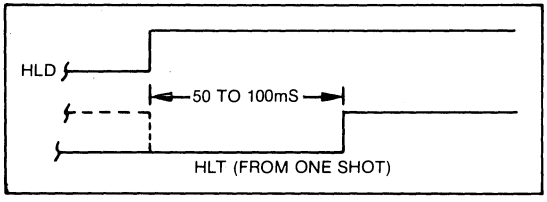
**Table 2. Stepping Rates**

| CLK: | | 2 MHz | 2 MHz | 1 MHz | 1 MHz | 2 MHz | 1 MHz |
|---|---|---|---|---|---|---|---|
| $\overline{DDEN}$: | | 0 | 1 | 0 | 1 | X | X |
| $r_1$ | $r_0$ | $\overline{TEST}$=1 | $\overline{TEST}$=1 | $\overline{TEST}$=1 | $\overline{TEST}$=1 | $\overline{TEST}$=0 | $\overline{TEST}$=0 |
| 0 | 0 | 3 ms | 3 ms | 6 ms | 6 ms | 184$\mu$s | 368$\mu$s |
| 0 | 1 | 6 ms | 6 ms | 12 ms | 12 ms | 190$\mu$s | 380$\mu$s |
| 1 | 0 | 10 ms | 10 ms | 20 ms | 20 ms | 198$\mu$s | 396$\mu$s |
| 1 | 1 | 15 ms | 15 ms | 30 ms | 30 ms | 208$\mu$s | 416$\mu$s |

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h=1), at the end of the Type I command if the verify flag (V=1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h=0 and V=0); or if the FDC 979X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FDC 979X which is used for the head engage time. When HLT = 1, the FDC 979X assumes the head is completely engaged.

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC 979X.




**Head Load Timing**

When both HLD and HLT are true, the FDC 979X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

| TYPE I COMMANDS FLAG SUMMARY |
|---|
| h=Head Load Flag (Bit 3) |
| h=1, Load head at beginning<br>h=0, Unload head at beginning |
| V=Verify flag (Bit 2) |
| V=1, Verify on destination track<br>V=0, No verify |
| $r_1r_0$=Stepping motor rate (Bits 1-0) |
| Refer to Table 2 for rate summary |
| u=Update flag (Bit 4) |
| u=1, Update Track register<br>u=0, No update |

## Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag=1 (this is the normal case) HLD is made active and HLT is sampled until true after a 15 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC979X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC 979X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC 979X will read or write multiple records starting with the sector presently in the sector register. The FDC 979X will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C=0, no side comparison is made. When C=1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 979X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The FDC 9795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

| Sector Length Table (9791/3 only) | |
|---|---|
| Sector Length Field (hex) | Number of Bytes in Sector (decimal) |
| 00 | 128 |
| 01 | 256 |
| 02 | 512 |
| 03 | 1024 |

**Field Format**

| GAP III | ID AM | TRACK NUMBER | SIDE NUMBER | SECTOR NUMBER | SECTOR LENGTH | CRC 1 | CRC 2 | GAP II | DATA AM | DATA FIELD | CRC 1 | CRC 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID FIELD | | | | | | | | | | DATA FIELD | | |

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

### Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

| STATUS BIT 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

### Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC 979X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_0$ field of the command as shown below:

| $a_0$ | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The FDC 979X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

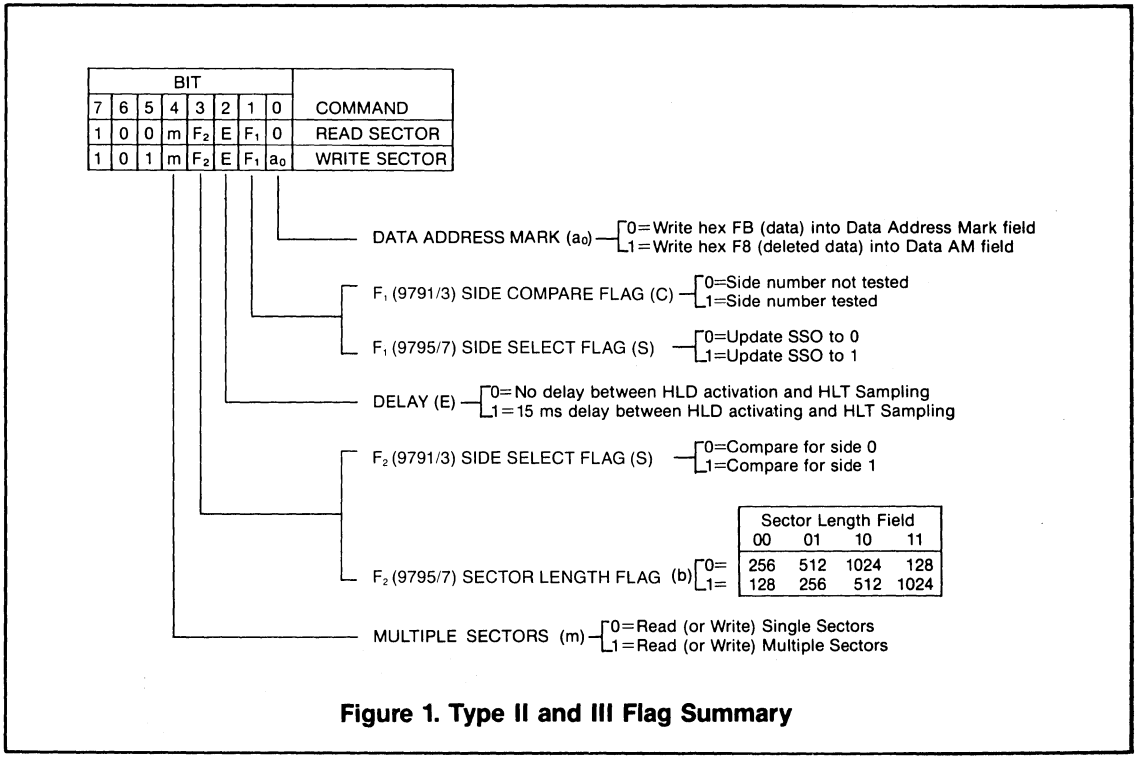



**Figure 1. Type II and III Flag Summary**

## Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

### Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDRESS | SECTOR LENGTH | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transferred to the computer, the FDC979X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

### Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

### Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which

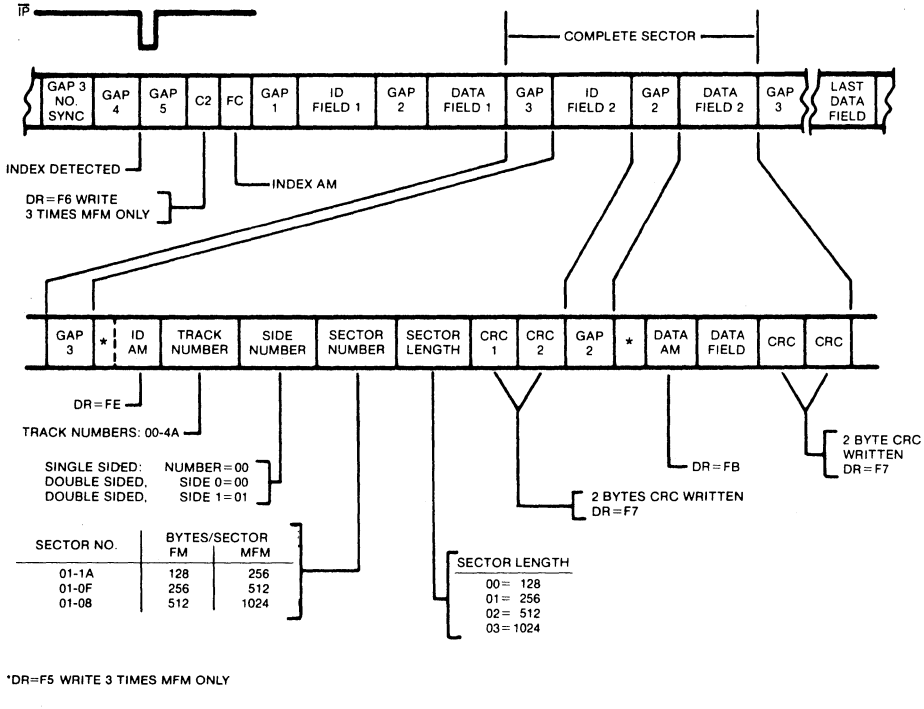



**Figure 2. IBM Compatible Sector/Track Format**

time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

## Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, $I_0$-$I_3$, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If $I_0$-$I_3$ are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for $I_3$=1 (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with $I_0$-$I_3$ all low.

### Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.



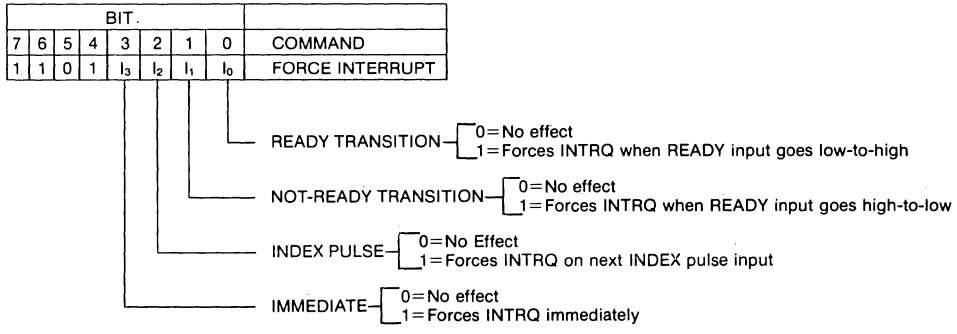



**Figure 3. Force Interrupt Command Flags**

## Figure 4A. Status Register Summary

| COMMAND | STATUS BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ALL TYPE I | Not Ready | Write Protect | Head Loaded | Seek Error | CRC Error | Track 0 | Index | Busy |
| READ SECTOR | Not Ready | 0 | Record Type | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| WRITE SECTOR | Not Ready | Write Protect | Write Fault | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| READ ADDRESS | Not Ready | 0 | 0 | Rec not Found | CRC Error | Lost Data | DRQ | Busy |
| READ TRACK | Not Ready | 0 | 0 | 0 | 0 | Lost Data | DRQ | Busy |
| WRITE TRACK | Not Ready | Write Protect | Write Fault | 0 | 0 | Lost Data | DRQ | Busy |

## Figure 4B. Status Description for Type I Commands

| BIT | NAME | MEANING |
|---|---|---|
| S7 | NOT READY | This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR. |
| S6 | PROTECTED | When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input. |
| S5 | HEAD LOADED | When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals. |
| S4 | SEEK ERROR | When set, the desired track was not verified. This bit is reset to 0 when updated. |
| S3 | CRC ERROR | CRC encountered in ID field. |
| S2 | TRACK 00 | When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input. |
| S1 | INDEX | When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input. |
| S0 | BUSY | When set command is in progress. When reset no command is in progress. |

## Figure 4C. Status Description for Type II and III Commands

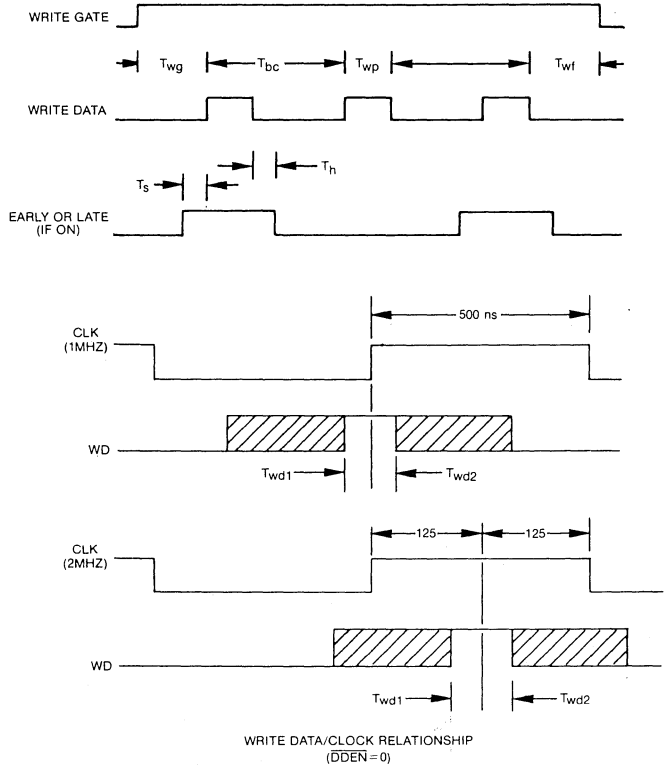
| BIT | NAME | MEANING |
|---|---|---|
| S7 | NOT READY | This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready. |
| S6 | WRITE PROTECT | On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated. |
| S5 | RECORD TYPE/ WRITE FAULT | On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated. |
| S4 | RECORD NOT FOUND (RNF) | When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated. |
| S3 | CRC ERROR | If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated. |
| S2 | LOST DATA | When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 | DATA REQUEST | This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated. |
| S0 | BUSY | When set, command is under execution. When reset, no command is under execution. |

## Write Data Timing:

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| Write Data Pulse Width | $T_{wp}$ | 450 | 500 | 550 | nsec | FM |
| | | 150 | 200 | 250 | nsec | MFM |
| Write Gate to Write Data | $T_{wg}$ | | 2 | | $\mu$sec | FM |
| | | | 1 | | $\mu$sec | MFM |
| Write data cyle Time | $T_{bc}$ | | 2, 3, or 4 | | $\mu$sec | $\pm$CLK Error |
| Early (Late) to Write Data | $T_s$ | 125 | | | nsec | MFM |
| Early (Late) From Write Data | $T_h$ | 125 | | | nsec | MFM |
| Write Gate off from WD | $T_{wf}$ | | 2 | | $\mu$sec | FM |
| | | | 1 | | $\mu$sec | MFM |
| WD Valid to Clk | $T_{wd1}$ | 100 | | | nsec | CLK=1 MHZ |
| | | 50 | | | nsec | CLK=2 MHZ |
| WD Valid after Clk | $T_{wd2}$ | 100 | | | nsec | CLK=1 MHZ |
| | | 30 | | | nsec | CLK=2 MHZ |

These values are doubled when CLK=1 MHz.

### Write Data Timing




WRITE DATA/CLOCK RELATIONSHIP
($\overline{DDEN}$=0)

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on Pin 40, with respect to ground ..... +15V
Positive Voltage on any other Pin, with respect to ground ..... +8V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±5%, unless otherwise noted)

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| Input Voltage Levels | | | | | | | |
| Low Level, $V_{IL}$ | | | | | 0.8 | V | |
| High Level, $V_{IH}$ | | | 2.0 | | | V | |
| Output Voltage Levels | | | | | | | |
| Low Level $V_{OL}$ | | | | | 0.45 | V | $I_{OL}$=1.6 mA |
| High Level $V_{OH}$ | | | 2.4 | | | V | $I_{OH}$=100 μA |
| Output Leakage, $I_{LO}$ | | | | | 10 | μA | 0.4 ≤ 3.5V |
| Input Leakage, $I_{IL}$ | | | | | 10 | μA | 0.4 ≤ 3.5V |
| Output Capacitance | | | | 5 | | pf | |
| Input Capacitance | | | | 10 | | pf | |
| Supply Current | | | | | 160 | mA | |
| **AC CHARACTERISTICS** | | | | | | | |
| Processor Read Timing | | | | | | | |
| Address Setup Time | | $t_{SETR}$ | 50 | | | ns | Figure 5 |
| Address Hold Time | | $t_{HLDR}$ | 10 | | | ns | Figure 5 |
| $\overline{RE}$ Pulse Width ($C_L$=50pF) | | $t_{RE}$ | 400 | | | ns | Figure 5 |
| DRQ Reset Time | | $t_{DRR}$ | | | 500 | ns | Figure 5 |
| INTRQ Reset Time | | $t_{IRR}$ | | 500* | 3000* | ns | Figure 5 |
| Data Delay Time ($C_L$=50pF) | | $t_{DACC}$ | | | 350 | ns | Figure 5 |
| Data Hold Time ($C_L$=50pF) | | $t_{DOH}$ | 50 | | 150 | ns | Figure 5 |
| Microprocessor Write Timing | | | | | | | |
| Address Setup Time | | $t_{SETW}$ | 50 | | | ns | Figure 6 |
| Address Hold Time | | $t_{HLDW}$ | 10 | | | ns | Figure 6 |
| WE Pulse Width | | $t_{WE}$ | 350 | | | ns | Figure 6 |
| DRQ Reset Time | | $t_{DRR}$ | | | 500 | ns | Figure 6 |
| INTRQ Reset Time | | $t_{IRR}$ | | 500* | 3000* | ns | Figure 6 |
| Data Setup Time | | $t_{DS}$ | 250 | | | ns | Figure 6 |
| Data Hold Time | | $t_{DH}$ | 70 | | | ns | Figure 6 |
| Disk Input Data Timing | | | | | | | |
| RAWREAD Pulse Width | | $t_{pw}$ | 100* | 200 | | ns | Figure 7, See Note |
| Clock Setup Time | | $t_d$ | 40 | | | ns | Figure 7 See Note |
| Clock Hold Time for MFM | | $t_{cd}$ | 40 | | | ns | Figure 7 |
| Clock Hold Time for FM | | $t_{cs}$ | 40 | | | ns | Figure 7 |
| RAWREAD Cycle Time | | $t_{bc}$ | 1500 | | | ns | 1800 at 70°C, Figure 7 |
| RCLK High Pulse Width | MFM | $t_a$ | 0.8 | 1* | | μs | Figure 7 |
| | FM | | 0.8 | 2* | | μs | Figure 7 |
| RCLK Low Pulse Width | MFM | $t_b$ | 0.8 | 1* | | μs | Figure 7 |
| | FM | | 0.8 | 2* | | μs | Figure 7 |
| RCLK Cycle Time | MFM | $t_c$ | | 2* | | μs | Figure 7 |
| | FM | | | 4* | | μs | Figure 7 |
| Miscellaneous Timing | | | | | | | |
| CLK Low Pulse Width | | $t_{CD1}$ | 230 | 250 | 20000 | ns | Figure 8 |
| CLK High Pulse Width | | $t_{CD2}$ | 200 | 250 | 20000 | ns | Figure 8 |
| STEP Pulse Width | MFM | $t_{STP}$ | 2* | | | μs | Figure 8 |
| | FM | | 4* | | | μs | Figure 8 |
| DIRC Setup Time | | $t_{DIR}$ | | 12 | | μs | Figure 8 |
| MR Pulse Width | | $t_{MR}$ | 50* | | | μs | Figure 8 |
| IP Pulse Width | | $t_{IP}$ | 10* | | | μs | Figure 8 |
| WF Pulse Width | | $t_{WF}$ | 10* | | | μs | Figure 8 |
| CLK Cycle Time | | $t_{CYC}$ | | 0.5* | | μs | Figure 8 |

* These Values are doubled when CLK=1 MHz.

**Figure 5. Microprocessor Read Timing**

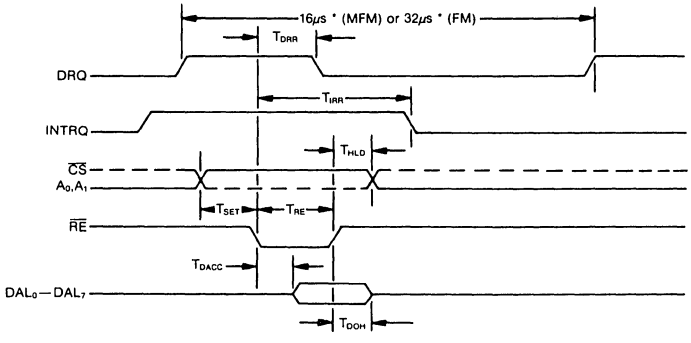



**Figure 6. Microprocessor Write Timing**

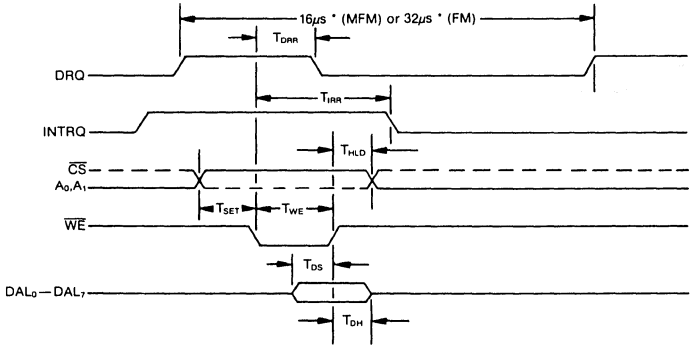
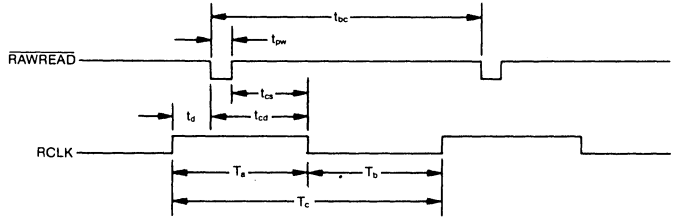
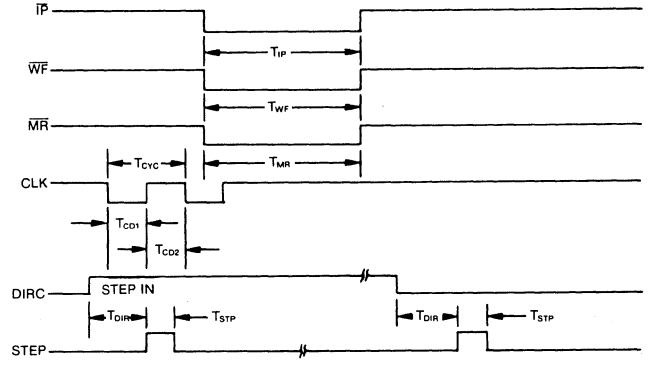



**Figure 7. Disk Input Timing**




Note: Pulse width on RAW READ (Pin 27) is normally 10-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.

**Figure 8. Miscellaneous Timing**




SECTION VI

# DISK FORMATS

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

### IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

### IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

### Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11.

| | DATA BYTE (hex) | NO. OF BYTES | COMMENTS |
|---|---|---|---|
| | FF | 40 | Gap 5 (Post Index) |
| | 00 | 6 | |
| | FC | 1 | Index AM |
| | FF | 26 | Gap 1 |
| | 00 | 6 | |
| | FE | 1 | ID AM |
| | XX | 1 | Track Number (00-4C) |
| | 0X | 1 | Side Number (00 or 01) |
| | XX | 1 | Sector Number (01-1A) |
| | 00 | 1 | Sector Length (128 bytes) |
| ONE SECTOR ① | F7 | 1 | Causes 2-Byte CRC to be Written |
| | FF | 11 | Gap 2 (ID Gap) |
| | 00 | 6 | |
| | FB | 1 | Data AM |
| | E5 | 128 | Data Field |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | FF | 27 | Part of Gap 3 (Data Gap) |
| | FF | 247 ② | Gap 4 (Pre Index) |

**Figure 9. Byte Sequence for IBM 3740 Formatting**

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

| | DATA BYTE (hex) | NO. OF BYTES | COMMENTS |
|---|---|---|---|
| | 4E | 80 | Gap 5 (Post Index) |
| | 00 | 12 | |
| | F6 | 3 | Writes C2 |
| | FC | 1 | Index AM |
| | 4E | 50 | |
| | 00 | 12 | Gap 1 |
| | F5 | 3 | Writes A1 |
| | FE | 1 | ID AM |
| | XX | 1 | Track Number (00-4C) |
| ONE SECTOR ① | 0X | 1 | Side Number (00 or 01) |
| | XX | 1 | Sector Number (01-1A) |
| | 01 | 1 | Sector Length (256 Bytes) |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | 4E | 22 | Gap 2 (ID Gap) |
| | 00 | 12 | |
| | F5 | 3 | Writes A1 |
| | FB | 1 | Data AM |
| | 40 | 256 | Data Field |
| | F7 | 1 | Causes 2-Byte CRC to be Written |
| | 4E | 54 | Part of Gap 3 (Data Gap) |
| | 4E | 598 ② | Gap 4 (Pre Index) |

**Figure 10. Byte Sequence for IBM System-34 Formatting**

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

| GAP | SINGLE DENSITY (FM) | DOUBLE DENSITY (MFM) | NOTE |
|---|---|---|---|
| Gap 1 | 16 bytes FF | 16 bytes 4E | 2 |
| Gap 2 | 11 bytes FF<br>6 bytes 00 | 22 bytes 4F<br>12 bytes 00<br>3 bytes A1 | 1 |
| Gap 3 | 10 bytes FF<br>4 bytes 00 | 16 bytes 4E<br>8 bytes 00<br>3 bytes A1 | 2 |
| Gap 4 | 16 bytes FF | 16 bytes 4E | 2 |

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

**Figure 11. Gap Size Limitations**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

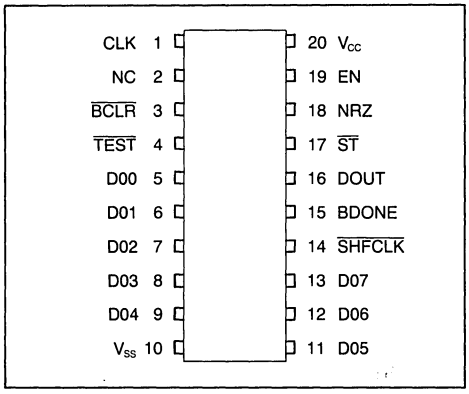
Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Hard Disk Serial to Parallel Converter

## FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 MBit Shift Rate
- ☐ Serial Input/Parallel Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

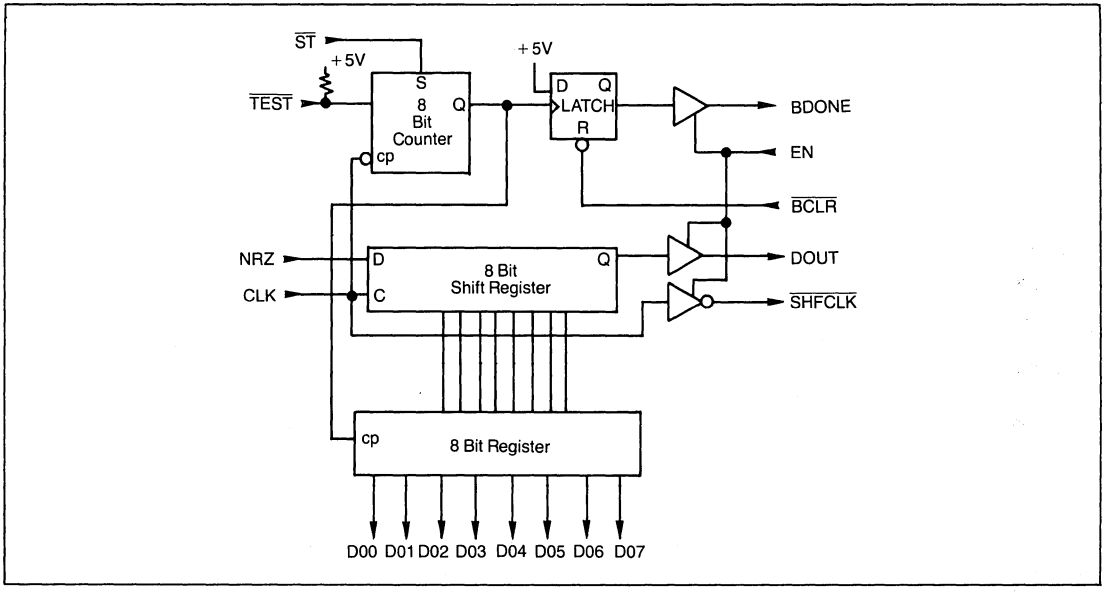
## PIN CONFIGURATION




## GENERAL DESCRIPTION

The HDC 1100-01 converts NRZ data from a Winchester disk drive into eight bit parallel form. Additional inputs are provided to initiate the conversion process, as well as output strobes to indicate the completion.

The HDC 1100-01 contains two sets of 8 bit registers. This allows one register to be read (in parallel) while serial data is being shifted into the other.




SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | CLK | CLOCK | NRZ data is entered into the 8-bit shift register on the low-to-high transition of clock. |
| 2 | NC | NO CONNECTION | No connection. This pin is to be left open by the user. |
| 3 | $\overline{BCLR}$ | $\overline{BYTE\ CLEAR}$ | When this line is at a logic 0, the BDONE (pin 15) line is held reset. |
| 4 | $\overline{TEST}$ | $\overline{TEST\ INPUT}$ | This pin must be left open by the user. |
| 5-9, 11-13 | D00-D07 | DATA0-DATA7 | 8 bit parallel data outputs. |
| 10 | $V_{SS}$ | GROUND | Ground. |
| 14 | $\overline{SHFCLK}$ | $\overline{SHIFT\ CLOCK}$ | Inverted copy of CLOCK (pin 1) which is active when EN (pin 19) is at a logic 1. |
| 15 | BDONE | BYTE DONE | This signal is forced to a logic 1 signifying 8 bits of data have been assembled. BDONE remains in a logic 1 state until reset by a logic 0 on the BCLR (pin 3) line. |
| 16 | DOUT | DATA OUT | Serial Data Output from the 8th stage of the internal shift register. DOUT is in a high impedance state whenever EN (pin 19) is at a logic 0. |
| 17 | $\overline{ST}$ | $\overline{START}$ | This line enables the byte counter and is used for synchronization. It must be held to a logic 1 prior to first data bit on the NRZ (Pin 18) line. |
| 18 | NRZ | NRZ DATA | NRZ serial data is entered on this pin and clocked by the low to high transition of CLK (pin 1). |
| 19 | EN | ENABLE | When this signal is at a logic 0, DOUT, $\overline{SHFCLK}$, and BDONE outputs are in a high impedance state. |
| 20 | $V_{CC}$ | $V_{CC}$ | +5V power supply input. |

## OPERATION

Prior to shifting data through the device, the HDC 1100-01 must be synchronized to the data stream. The ST line (Pin 17 high) is used to hold the internal bit counter in a cleared state until valid data (NRZ) and clocks (CLK) are entered. The $\overline{ST}$ line is a synchronous input and therefore requires one full cycle of the CLK line (Pin 1) to occur in order to accept a $\overline{ST}$ condition. After this happens, the device is ready to perform serial to parallel conversions.

Data is entered on the NRZ line and clocked into the 8-bit shift register on the low-to-high transition of CLK. The $\overline{ST}$ line must be set low during the low time of CLK. Data is accepted on low-to-high transition of the clock while the high-to-low transition of CLK increments the bit counter. After 8 data bits have been entered the final high-to-low transition of CLK sets an internal latch tied to the BDONE line (Pin 15). At the same time, the contents of the shift register are parallel loaded into an 8 bit register making the parallel data available on the D00-D07 outputs. BDONE will remain in a latched state until the $\overline{BCLR}$ is set to a logic 0, clearing off the BDONE signal. $\overline{BCLR}$ is a level triggered input and must be set back to a logic 1 before the next 8 bits are shifted through the register. $\overline{BCLR}$ has no effect on the serial shifting process. When the next 8 bits are received, BDONE will again be set and the operation continues.

When interfacing to a microprocessor, BDONE is used to indicate a parallel byte is ready to be read. As the processor reads the data out of the D00-D07 lines, the $\overline{BCLR}$ line should be strobed to clear off BDONE in anticipation of the next assembled byte. An address decode signal generated at the host may be used for this purpose. During a power-up condition, the state of BDONE is indeterminant. It is recommended that BCLR be strobed low after power-up to insure that BDONE is cleared.

The serial output line from the last stage of the shift register is available on the DOUT pin. An inverted copy of CLK is available on the $\overline{SHFCLK}$ pin. Both DOUT (Pin 16) and $\overline{SHFCLK}$ (Pin 14) can be used to drive another shift register external to the device.

The three signals BDONE, DOUT, and $\overline{SHFCLK}$ can be placed in a high impedance state by setting EN (Pin 19) to a logic 0. Likewise, EN must be at a logic 1 in order for these signals to be active.

The TEST pin is internally OR'ed with the $\overline{ST}$ line to inhibit the bit counter. It is recommended that $\overline{TEST}$ be left open by the user. An internal pull-up resistor is tied to this pin to satisfy the appropriate logic level required internally for proper device operation.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress ... ion of the device at these or at any other condition above those indicated in the operational sections of this ...

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

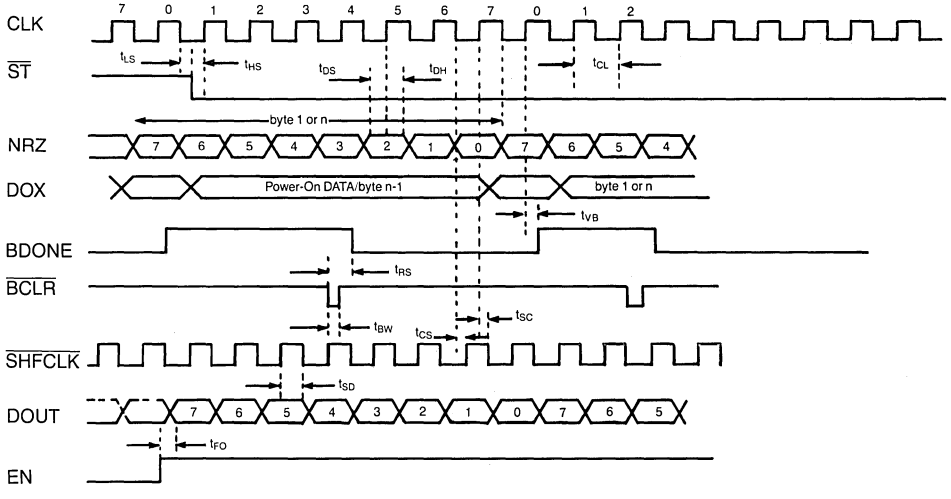
**DC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.2 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.4 | | | V | |
| $V_O$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −200µA |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| $I_{CC}$ | Supply Current | | | 100 | mA | All Outputs Open |

**AC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = 5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{CL}$ | CLK FREQUENCY | 0 | | 5.25 | MHZ | |
| $t_{LS}$ | ↓ CLK to $\overline{ST}$ | 0 | | | nsec | $\overline{ST}$ = 1 (min 200nsec) |
| $t_{HS}$ | ↑ CLK to $\overline{ST}$ | 0 | | | nsec | $\overline{ST}$ = 1 (min 200nsec) |
| $t_{DS}$ | Data set-up to ↑ CLK | 15 | | | nsec | |
| $t_{VB}$ | BDONE valid from ↑ CLK | 65 | | 110 | nsec | EN = 1 |
| $t_{RS}$ | BDONE reset from $\overline{BCLR}$ | | | 110 | nsec | EN = 1 |
| $t_{BW}$ | $\overline{BCLR}$ Pulse Width | 50 | | | nsec | EN = 1 |
| $t_{SC}$ | ↑ CLK to ↓ $\overline{SHFCLK}$ | | | 90 | nsec | EN = 1 |
| $t_{CS}$ | ↓ CLK to ↑ $\overline{SHFCLK}$ | | | 100 | nsec | EN = 1 |
| $t_{SD}$ | Data delay from ↑ $\overline{SHFCLK}$ | | | 55 | nsec | EN = 1 |
| $t_{FO}$ | Enable to DOUT ACTIVE | | | 90 | nsec | |
| $t_{DH}$ | Data Hold w.r.t. ↑ CLK | 25 | | | nsec | |

NOTES: 1. Typical Values are for $T_A$ = 25°C and $V_{CC}$ = +5.0V




SECTION VI

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

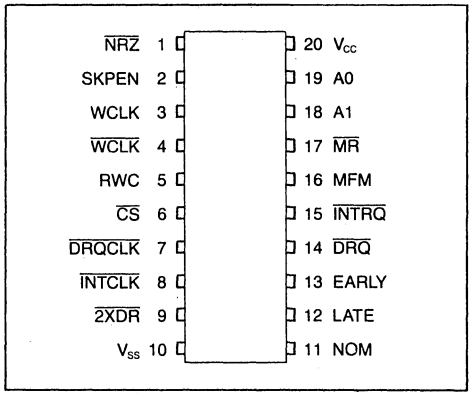
# HDC 1100-12
**PRELIMINARY**

# Hard Disk Improved MFM Generator

## FEATURES

- ☐ Single +5 Volt Power Supply
- ☐ Write Precompensation
- ☐ Address Mark Generation
- ☐ 5 Mbit Data Rate
- ☐ Converts NRZ to MFM
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

## PIN CONFIGURATION

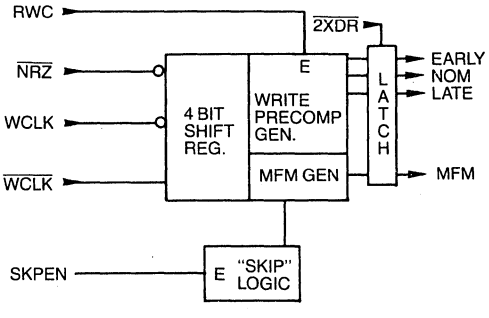



## GENERAL DESCRIPTION

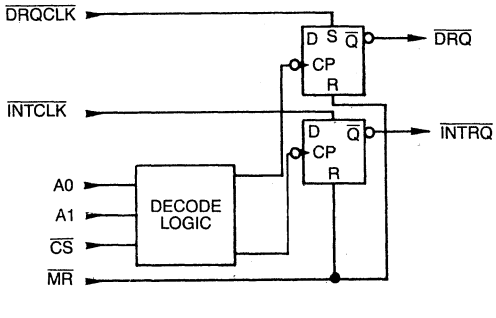
The HDC 1100-12 "improved" MFM Generator converts serial NRZ data into an MFM (Modified Frequency Modulated) data stream. The MFM signal may be used to record information on a Winchester Disk.

In addition, the HDC 1100-12 generates Write Precompensation signals required to compensate for bit shift effects on the recording medium.

The HDC 1100-12 has the ability to delete clock pulses in the outgoing data stream in order to record Address Marks.




MFM GENERATOR




INTERRUPT CONTROLLER

SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $\overline{NRZ}$ | $\overline{NON\text{-}RETURN\text{-}TO\ ZERO}$ | NRZ data input that is strobed into the MFM generator by WCLK (↓). |
| 2 | SKPEN | SKIP ENABLE | This input arms the SKIP logic for recording Address Marks when set to a logic 1. |
| 3 | WCLK | WRITE CLOCK | Complimentary clock inputs. $\overline{NRZ}$ data is clocked into the MFM Generator on the high-to-low transition of WCLK (pin 3). |
| 4 | $\overline{WCLK}$ | $\overline{WRITE\ CLOCK}$ | |
| 5 | RWC | REDUCED WRITE CURRENT | This signal when high, enables EARLY, LATE and NOM outputs. |
| 9 | $\overline{2 \times DR}$ | $\overline{2\ TIMES\ DATA\ RATE}$ | This input is used to latch EARLY, LATE, NOM and MFM outputs. |
| 10 | $V_{SS}$ | $V_{SS}$ | Ground. |
| 11 | NOM | NOMINAL | Output signal from the Write Precompensation Logic used to signify that data is to be written nominal. |
| 12 | LATE | LATE | Output signal from the Write Precompensation Logic used to signify that data is to be shifted LATE before writing. |
| 13 | EARLY | EARLY | Output signal from the Write Precompensation Logic used to signify that data is to be shifted EARLY before writing. |
| 16 | MFM | MFM DATA | This output contains the MFM encoded data derived from the $\overline{NRZ}$ (pin 1) line. |
| 6 | $\overline{CS}$ | $\overline{CHIP\ SELECT}$ | Low input signal used to enable the Address decode logic. |
| 8 | $\overline{INTCLK}$ | $\overline{INTERRUPT\ REQUEST\ CLOCK}$ | A high-to-low transition on this line will latch the INTRQ (pin 15) at a logic 0. |
| 7 | $\overline{DRQCLK}$ | $\overline{DATA\ REQUEST\ CLOCK}$ | A high-to-low transition on this line will latch the DRQ (pin 14) at a logic 0. |
| 15 | $\overline{INTRQ}$ | $\overline{INTERRUPT\ REQUEST}$ | This output is latched at a logic 0 when INTCLK (pin 8) makes a high-to-low transition while the decode logic is disabled. |
| 14 | $\overline{DRQ}$ | $\overline{DATA\ REQUEST}$ | This output is latched at a logic 0 when DRQCLK (pin 7) makes a high-to-low transition while the decode logic is disabled. |
| 17 | $\overline{MR}$ | $\overline{MASTER\ RESET}$ | A low level on this line causes DRQ and INTRQ to set at a logic 1. |
| 18, 19 | $A_0$, $A_1$ | ADDRESS 1, 0 | When CS is low and the address lines are high, INTRQ is cleared; if the address lines are low then DRQ gets cleared. (i.e. set at a logic 1). |
| 20 | $V_{CC}$ | $V_{CC}$ | +5V power supply input. |

## OPERATION

The HDC 1100-12 is divided into two sections: MFM Generator and Interrupt Logic. The MFM Generator converts NRZ data into MFM data and provides Write Precompensation signals. The Interrupt Logic may be used to generate Interrupt signals. The two sections of the device are isolated and have no common input or output signals.

Prior to entering data, the SKPEN line must be set to a logic 0 to enable only clocks in the data stream. Data is entered on the NRZ line and strobed on the high-to-low transition of WCLK. The encoded NRZ data appears on the MFM (pin 16) output lagging by one clock cycle.

Write Precompensation signals EARLY, LATE, and NOM are generated as each data or clock pulse becomes available at the input when RWC is logic 1.

The SKPEN signal is used to record a unique data/clock pattern as an Address Mark, using A1 data with 0A clock. This pattern is used for synchronization prior to data or ID fields that are read from the disk.

When the SKPEN signal is set to a logic 1, the internal skip logic is enabled. As long as zeroes are being shifted into the NRZ line, the device generates normal MFM data. On receipt of the first non-zero bit (typically the MSB of the A1 16) the skip logic begins to count WCLK cycles. When the MFM generator tries to produce a clock between data bits 2 and 3, the skip logic disables the MFM generator during that time. The result for $A1_{16}$ data is a clock pattern of $0A_{16}$ instead of $OE_{16}$. Although other data patterns may be used,

| $\overline{MR}$ | $A_1$ | $A_0$ | $\overline{CS}$ | $\overline{DRQ}$ | $\overline{INTRQ}$ |
|---|---|---|---|---|---|
| 0 | X | X | X | H | H |
| 1 | X | X | 1 | $Q_N$ | $Q_N$ |
| 1 | 0 | 0 | 0 | H | $Q_N$ |
| 1 | 1 | 1 | 0 | $Q_N$ | H |
| 1 | 1 | 0 | 0 | $Q_N$ | $Q_N$ |
| 1 | 0 | 1 | 0 | $Q_N$ | $Q_N$ |

X = Don't care $Q_N$ = remains at previous state

**INTERRUPT REQUEST LOGIC TABLE**

the MSB of the pattern must be a 1 ($80_{16}$ or higher) in order to enable the skip logic at the proper time. After the skip logic has performed, it then disables itself and MFM data is recorded normally starting with the succeeding byte. To re-enable the skip logic again, the SKPEN line must be strobed.

The Interrupt Logic is used to clear Data Requests ($\overline{DRQ}$) and Interrupt Requests (INTRQ) by selecting $\overline{CS}$ (pin 6) in combination with A0 and A1. The $\overline{MR}$ (Master Reset) signal is used to clear both $\overline{DRQ}$ and $\overline{INTRQ}$ simultaneously. $\overline{DRQ}$ and $\overline{INTRQ}$ can be set to a logic 0 only by a low level or $\overline{DRQCLK}$ and $\overline{INTCLK}$ respectively. The signal will remain at a logic 0 until cleared by a $\overline{MR}$ or proper address selection via $\overline{CS}$, A1 and A0.

| LAST DATA SENT | SENDING | TO BE SENT NEXT | EARLY | LATE | NOM |
|---|---|---|---|---|---|
| X 1 | 1 | 0 | H | L | L |
| X 0 | 1 | 1 | L | H | L |
| 0 0 | 0 | 1 | H | L | L |
| 1 0 | 0 | 0 | L | H | L |
| ANY OTHER PATTERN | | | L | L | H |

**WRITE PRECOMPENSATION LOGIC TABLE**

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and fu... device at these or at any other condition above those indicated in the operational sections of this specification is ...

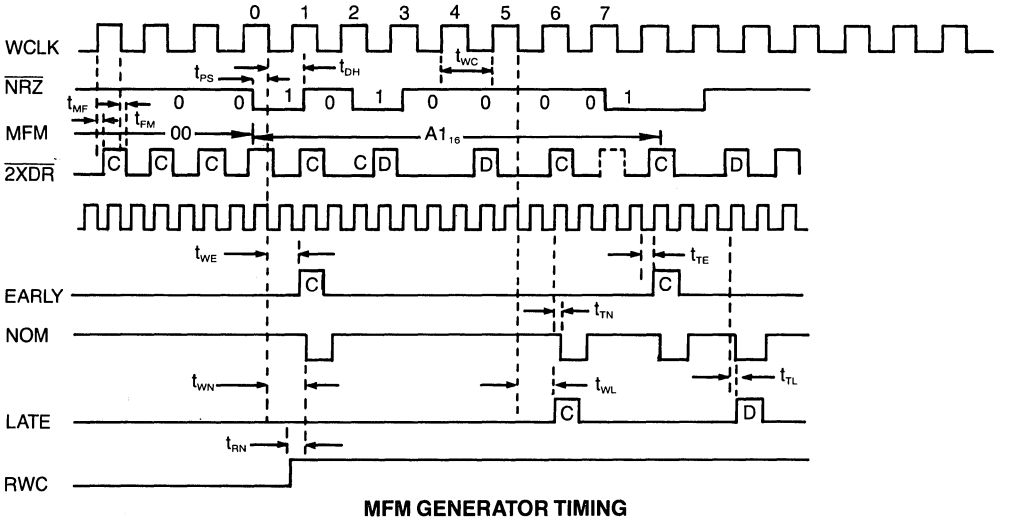
**DC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%; $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.2 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.4 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −200μA |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| $I_{CC}$ | Supply Current | | | 100 | mA | All Outputs Open |

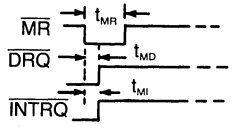
**AC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%; $V_{SS}$ = 0V

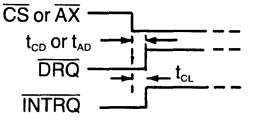
| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{FR}$ | WCLK FREQUENCY | | | 5.25 | MHZ | |
| $t_{DS}$ | Data Setup w.r.t. ↓ WCLK | 10 | | | nsec | |
| $t_{DH}$ | Data hold w.r.t. ↓ WCLK | 25 | | | nsec | |
| $t_{MF}$ | ↑ WCLK to ↑MFM delay | | | 210 | nsec | Pin 1 LOW |
| $t_{FM}$ | ↓ WCLK to ↓ MFM delay | | | 230 | nsec | Pin 1 LOW |
| $t_{WN}$ | Data delay to NOM from ↓ WCLK | | | 240 | nsec | |
| $t_{WE}$ | Data delay to EARLY from ↓ WCLK | | | 230 | nsec | |
| $t_{WL}$ | Data delay to LATE from ↓ WCLK | | | 230 | nsec | |
| $t_{MR}$ | Master reset pulse width | 50 | | | nsec | |
| $t_{MD}$ | ↓ $\overline{MR}$ to ↑ $\overline{DRQ}$ | | | 150 | nsec | |
| $t_{MI}$ | ↓MR to ↑ $\overline{INTRQ}$ | | | 150 | nsec | |
| $t_{DQ}$ | $\overline{DRQCLK}$ pulse width | 50 | | | nsec | |
| $t_{IQ}$ | $\overline{INTCLK}$ pulse width | 50 | | | nsec | |
| $t_{DD}$ | ↓ $\overline{DRQCLK}$ to $\overline{DRQ}$ | | | 120 | nsec | |
| $t_{II}$ | ↓ $\overline{INTCLK}$ to $\overline{INTRQ}$ | | | 120 | nsec | |
| $t_{AD}$ | ↓ AX to ↑ $\overline{DRQ}$ | | | 145 | nsec | |
| $t_{AI}$ | ↑ AX to ↑ $\overline{INTRQ}$ | | | 160 | nsec | |
| $t_{CD}$ | ↓ $\overline{CS}$ to ↑ $\overline{DRQ}$ | | | 145 | nsec | |
| $t_{CI}$ | ↓ $\overline{CS}$ to ↑ $\overline{INTRQ}$ | | | 180 | nsec | |
| $t_{RN}$ | ↑ RWC to ↓ NOM | | | 145 | nsec | |
| $t_{TE}$ | ↓ $\overline{2XDR}$ to ↑ EARLY | | | 75 | nsec | |
| $t_{TN}$ | ↓ $\overline{2XDR}$ to ↑ NOM | | | 75 | nsec | |
| $t_{TL}$ | ↓ $\overline{2XDR}$ to ↑ LATE | | | 75 | nsec | |

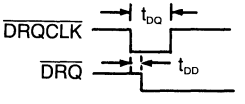
Notes: 1. Typical Values are for $T_A$ = 25°C and $V_{CC}$ = +5.0V.

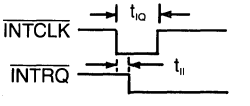



**MFM GENERATOR TIMING**




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

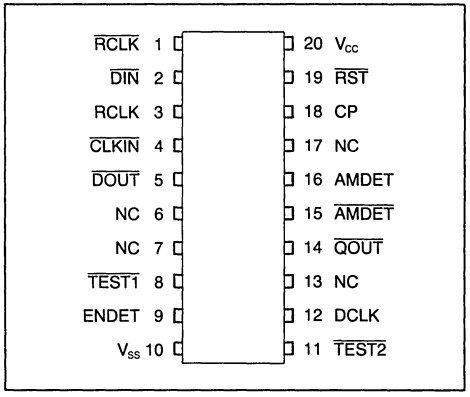
**HDC 1100-03**
**PRELIMINARY**

# Hard Disk Address Mark Detector

## FEATURES

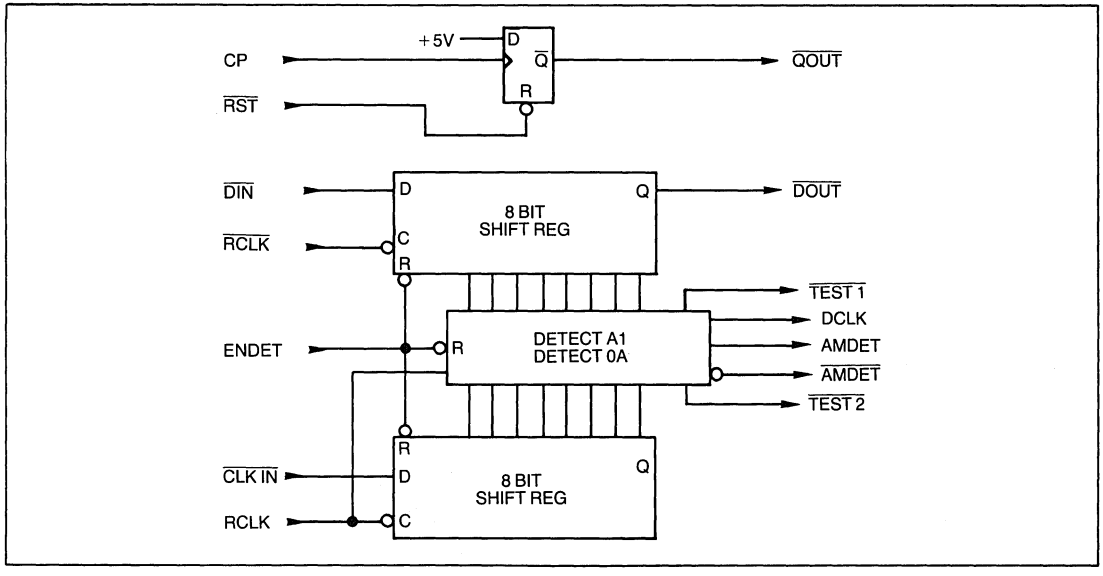
- ☐ Single +5 Volt Power Supply
- ☐ Decodes A1-0A
- ☐ Synchronous Clock/Data Outputs
- ☐ 5 MBit Data Rate
- ☐ Address Mark Detection
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The HDC 1100-03 Address Mark Detector Provides an efficient means of detecting Address Mark Fields in an MFM (NRZ) data stream. MFM clocks and data are fed to the device along with a window clock generated by an external data separator. The HDC 1100-03 searches the data stream for a DATA = A1, CLK = 0A pattern and produces and AM DET signal when the pattern has been found. NRZ data is output from the device for driving a serial/parallel converter. An uncommitted latch is also provided for use by the data separator circuitry if required.




SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $\overline{RCLK}$ | $\overline{READ\ CLOCK}$ | Complimentary clock inputs used to clock DIN and $\overline{CLK\ IN}$ into the AM detector. |
| 3 | RCLK | READ CLOCK | |
| 2 | $\overline{DIN}$ | $\overline{DATA\ INPUT}$ | MFM data pulses from the external Data Separator are connected on this line. |
| 4 | $\overline{CLK\ IN}$ | $\overline{CLOCK\ INPUT}$ | MFM clock pulses from the external Data Separator are connected on this line. |
| 5 | $\overline{DOUT}$ | $\overline{DATA\ OUTPUT}$ | Data Output from the internal Data Shift register, synchronized with DCLK. |
| 6, 7, 13, 17 | NC | No Connection | To be left open by the user. |
| 8<br>11 | $\overline{TEST\ 1}$<br>$\overline{TEST\ 2}$ | $\overline{TEST\ 1}$<br>$\overline{TEST\ 2}$ | To be left open by the user. |
| 9 | ENDET | ENABLE DETECTION | A logic 1 on this line enables the detection logic to search for a data $A1_{16}$ and clock. |
| 10 | $V_{SS}$ | $V_{SS}$ | GROUND. |
| 12 | DCLK | DATA CLOCK | Clock output that is synchronized with $\overline{DATA\ OUT}$ (Pin 5). |
| 14 | $\overline{QOUT}$ | $\overline{LATCH\ OUTPUT}$ | Signal output from the uncommitted latch. |
| 15 | $\overline{AMDET}$ | $\overline{ADDRESS\ MARK\ DETECT}$ | Complimentary Address Mark Detector output. These signals will go active when a Data = $A1_{16}$ Clock = $0A_{16}$ pattern is detected in the data stream. |
| 16 | AMDET | ADDRESS MARK DETECT | |
| 18 | CP | CLOCK PULSE | A low-to-high transition on this line will cause the $\overline{QOUT}$ (Pin 14) to be latched at a logic 0. |
| 19 | $\overline{RST}$ | $\overline{RESET}$ | A logic 0 on this line will cause the QOUT (Pin 14) signal to be set at a logic 1. |
| 20 | $V_{CC}$ | $V_{CC}$ | +5V power supply input. |

## OPERATION

Prior to shifting data through the device, the internal logic must be initialized. While the ENDET (Pin 9) line is at a logic 0, shifting of data will be inhibited and AMDET, $\overline{AMDET}$, DCLK, and $\overline{DATA\ OUT}$ will remain inactive.

When ENDET is at a logic 1, shifting is enabled. NRZ data is entered on the $\overline{DIN}$ line (Pin 2) and shifted on the high-to-low transition of $\overline{RCLK}$ (Pin 1). NRZ clocks are entered on the $\overline{CLK\ IN}$ line, and shifted on the high-to-low transition of RCLK (Pin 3). The $\overline{DOUT}$ line (Pin 5) is tied to the last stage of the Internal Data Shift register and will reflect information clocked into the $\overline{DIN}$ line delayed by 8 bits.

While each bit is being shifted, a 16 bit comparator is continuously checking the parallel contents of the shift registers for the DATA = $A1_{16}$ CLK = $0A_{16}$ pattern. When this pattern is detected, $\overline{AMDET}$ will be set to a logic 0 and AMDET will be set to a logic 1. $\overline{AMDET}$ and AMDET will remain latched until the device is re-initialized by forcing ENDET to a logic 0.

When an AM is detected, DCLK will begin to toggle. Data present on the $\overline{DOUT}$ line may then be clocked into an external serial/parallel converter. DCLK will remain inactive when ENDET is held at a logic 0.

An uncommitted edge-triggered flip/flop has been provided to facilitate the detection of high-frequency by the data separator, but may be used for any purpose. The low-to-high transition of CP (Pin 18) will set the $\overline{QOUT}$ (Pin 14) to a logic 0. $\overline{QOUT}$ may be reset back to a logic 1 by a low level on the RST line (Pin 19).

$\overline{TEST1}$ and $\overline{TEST2}$ are output lines. $\overline{TEST1}$ is an active low pulse when an $A1_{16}$ is detected, and $\overline{TEST2}$ is an active low pulse when a $0A_{16}$ is detected. These signals are used for test points and therefore should be left open by the user if not required.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rat[ing] [only] and operation of the device at these or at any other condition above those indicated in the operational sections of t[his]

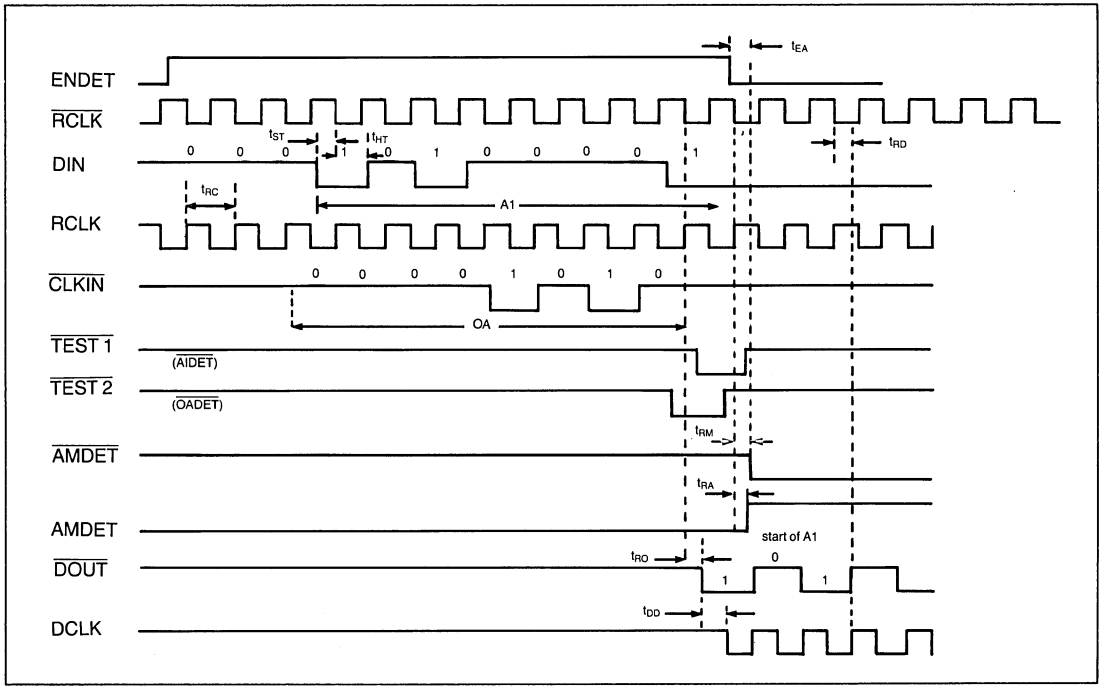
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**DC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.2 | | 0.7 | V | |
| $V_{IH}$ | Input High Voltage | 2.4 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −200μA |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| $I_{CC}$ | Supply Current | | | 100 | mA | All Outputs Open |

**AC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{RC}$ | RCLK Frequency | | | 5.25 | MHZ | |
| $t_{ST}$ | Data Setup time | 40 | | | nsec | |
| $t_{HT}$ | Data Hold time | 10 | | | nsec | |
| $t_{DD}$ | $\overline{DOUT}$ to DCLK DELAY | | | 110 | nsec | |
| $t_{RD}$ | ↓ $\overline{RCLK}$ to ↑ DCLK | | | 120 | nsec | |
| $t_{RA}$ | ↓ $\overline{RCLK}$ to ↑$\overline{AMDET}$ | | | 115 | nsec | |
| $t_{RM}$ | ↓ $\overline{RCLK}$ to ↓ $\overline{AMDET}$ | | | 125 | nsec | |
| $t_{RO}$ | ↓ $\overline{RCLK}$ to $\overline{DOUT}$ | | | 135 | nsec | |
| $t_{EA}$ | ↓ $\overline{ENDET}$ to ↓ AMDET | | | 130 | nsec | |
| $t_{RQ}$ | ↓ $\overline{RST}$ to ↑ $\overline{QOUT}$ | | | 110 | nsec | |
| $t_{RW}$ | Pulse width of $\overline{RST}$ | 50 | | | nsec | |
| $t_{CW}$ | CP Pulse width | 90 | | | nsec | |
| $t_{CQ}$ | ↑ CP to ↓ $\overline{QOUT}$ | | | 106 | nsec | |




SECTION VI

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

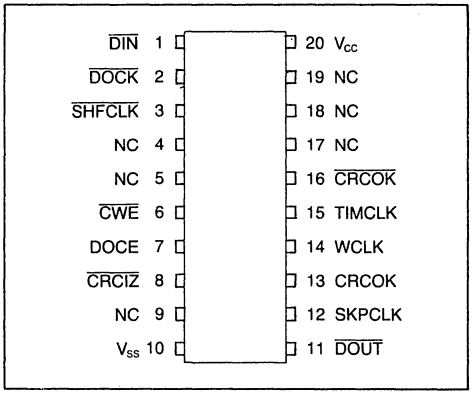
# HDC 1100-04
**PRELIMINARY**

# Hard Disk CRC Checker/Generator

## FEATURES

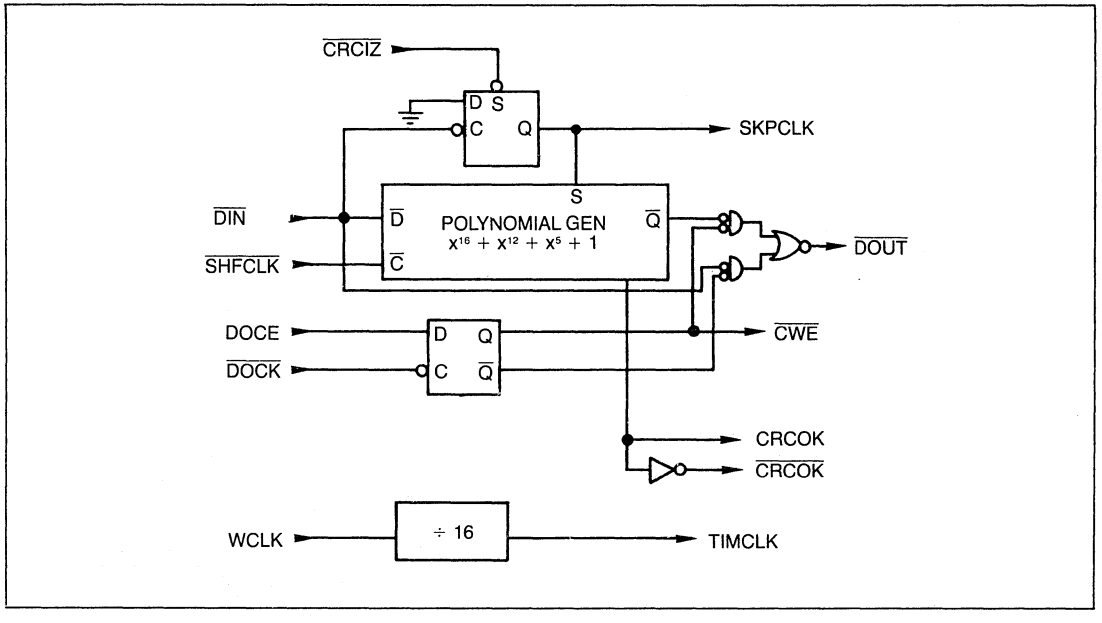
- ☐ Single +5 Volt Power Supply
- ☐ Generates/Checks CRC
- ☐ Latched Error Outputs
- ☐ CCITT-16 CRC
- ☐ Automatic Preset
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The HDC 1100-04 CRC Checker/Generator generates a Cyclic Redundancy Checkword from a serial data stream, and checks for the proper CRC in a received serial data stream. In addition to the transmitted CRC output, complimentary latched "CRCOK" outputs are provided to indicate CRC errors in the check mode.




SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | $\overline{DIN}$ | $\overline{DATA\ INPUT}$ | Active low serial input data stream is used to generate/ check the 2 byte CRC word. |
| 2 | $\overline{DOCK}$ | $\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$ | After a byte of data has been transferred, in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition. |
| 3 | $\overline{SHFCLK}$ | $\overline{SHIFT\ CLOCK}$ | The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to $\overline{DOUT}$ in the write mode (DOCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found. |
| 4, 5 | N.C. | NO CONNECTION | |
| 6 | $\overline{CWE}$ | $\overline{CHECK\ WORD\ ENABLE}$ | This active low output indicates that the CRC checkword is being output on the $\overline{DOUT}$ line. When $\overline{CWE}$ is high, data is being output on $\overline{DOUT}$. |
| 7 | DOCE | DATA OR CRC ENABLE | Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11).<br>DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode. |
| 8 | $\overline{CRCIZ}$ | $\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$ | When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF." |
| 9 | N.C. | NO CONNECTION | NO CONNECTION |
| 10 | $V_{SS}$ | GROUND | GROUND. |
| 11 | $\overline{DOUT}$ | $\overline{DATA\ OUTPUT}$ | In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream. |
| 12 | SKPCLK | SKIP CLOCK | The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word. |
| 13 | CRCOK | CYCLIC REDUNDANCY CHECK OKAY | In the read mode, after the 2 byte CRC word is entered on $\overline{DIN}$ and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as $\overline{DIN}$ is maintained high. |
| 14 | WCLK | WRITE CLOCK | This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry. |
| 15 | TIMCLK | TIMING CLOCK | See above. |
| 16 | $\overline{CRCOK}$ | $\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$ | Complementary output version of CRCOK (pin 13). |
| 17-19 | N.C. | NO CONNECTION | |
| 20 | $V_{CC}$ | $V_{CC}$ | +5V power supply input. |

## OPERATION

Prior to shifting data thru the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the $\overline{CRCIZ}$ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on $\overline{DIN}$ (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The HDC 110-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and $\overline{CRCOK}$ lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and a pseudo DOCK is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flip to gate input data to the output line $\overline{DOUT}$ (pin 11). As shown in the block diagram the $\overline{CWE}$ (pin 6) will be set high. Sometime between the next to the last and the last $\overline{DOCK}$ that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line DOUT (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, $\overline{DOUT}$ will produce a string of zeros (i.e., held high). This portion of the circuitry is dormant in the read mode.

After proper initialization, input data is entered on DIN (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the

complementary output (pin 16) is set low. These output states will be maintained as long as DIN is held high and CRCIZ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a re-try is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rati... of the device at these or at any other condition above those indicated in the operational sections of this spe...

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**DC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

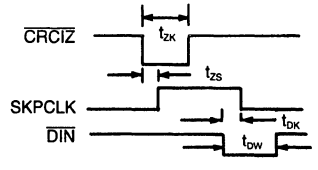
| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.2 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.4 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −200μA |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| $I_{CC}$ | Supply Current | | | 100 | mA | All Outputs Open |

**AC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{WT}$ | ↑ WCLK to ↓ TIMCLK | | | 95 | nsec | |
| $t_{WR}$ | ↑ $\overline{\text{WCLK}}$ to ↑TIMCLK | | | 85 | nsec | |
| $t_{ZS}$ | ↓ $\overline{\text{CRCIZ}}$ to ↑ SKPCLK | | | 120 | nsec | |
| $t_{ZK}$ | $\overline{\text{CRCIZ}}$ pulse width | 90 | | | nsec | |
| $t_{BS}$ | $\overline{\text{DOCE}}$ set up time w.r.t. ↓ $\overline{\text{DOCK}}$ | 20 | | | nsec | |
| $t_{BH}$ | $\overline{\text{DOCE}}$ hold time w.r.t. ↓ $\overline{\text{DOCK}}$ | 40 | | | nsec | |
| $t_{DD}$ | $\overline{\text{DIN}}$ to $\overline{\text{DOUT}}$ delay | | | 105 | nsec | CWE set high |

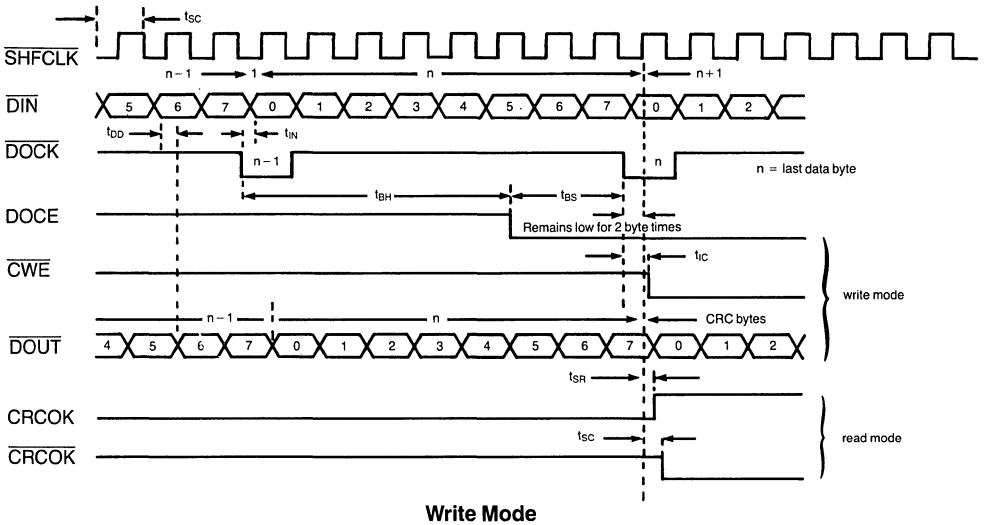
| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{DK}$ | ↓$\overline{\text{DIN}}$ to ↓ SKPCLK | | | 120 | nsec | |
| $t_{DW}$ | $\overline{\text{DIN}}$ P.W. to reset SKPCLK | 50 | | | nsec | |
| $t_{IC}$ | ↓ $\overline{\text{DOCK}}$ to ↓ $\overline{\text{CWE}}$ | | | 120 | nsec | |
| $t_{BC}$ | ↓ $\overline{\text{DOCK}}$ to ↑ $\overline{\text{CWE}}$ | | | 120 | nsec | |
| $t_{SC}$ | $\overline{\text{SHFCLK}}$ frequency | | | 5.25 | MHZ | |
| $t_{SR}$ | ↑ $\overline{\text{SHFCLK}}$ to ↑ CRCOK | | | 85 | nsec | |
| $t_{SC}$ | ↑ $\overline{\text{SHFCLK}}$ to ↓ $\overline{\text{CRCOK}}$ | | | 90 | nsec | |
| $t_{IN}$ | ↓ $\overline{\text{DOCK}}$ to ↓ $\overline{\text{DIN}}$ | | | 90 | nsec | |

Notes: 1. Typical values are for $T_A$ = 25°C and $V_{CC}$ = +5.0V




**Initialize**

SECTION VI




**Write Mode**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

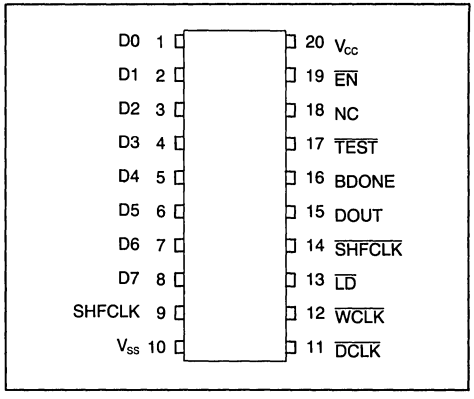
**HDC 1100-05**
**PRELIMINARY**

# Hard Disk Parallel to Serial Converter

## FEATURES

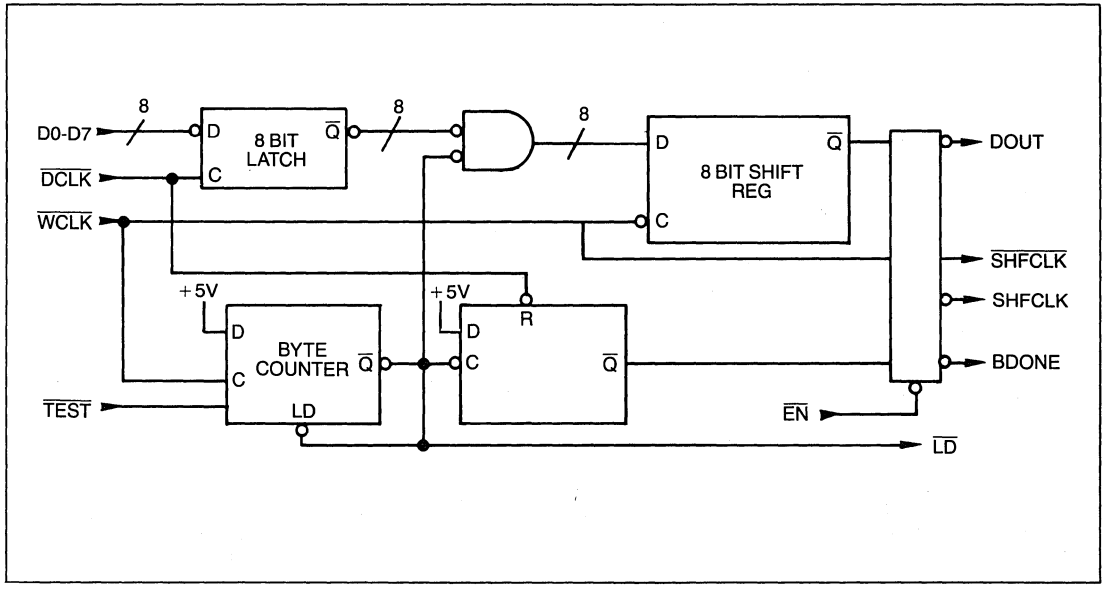
- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 Mbit Data Rate
- ☐ Parallel In/Serial Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

## PIN CONFIGURATION




## GENERAL DESCRIPTION

The HDC 1100-05 converts bytes of parallel data to a serial data stream for writing to disk memories or other serial devices. Parallel data is entered via the D0-D7 lines. A synchronous byte counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.




SECTION VI

## DESCRIPTION OF PIN FUNCTIONS

| PIN NUMBER | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1-8 | D0-D7 | DATA 0-DATA 7 | 8 bit parallel data inputs (bit 7 = MSB). |
| 9 | SHFCLK | SHIFT CLOCK | Inverted copy of $\overline{\text{WCLK}}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0. |
| 10 | $V_{SS}$ | GROUND | GROUND. |
| 11 | $\overline{\text{DCLK}}$ | $\overline{\text{DATA CLOCK}}$ | Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch. |
| 12 | $\overline{\text{WCLK}}$ | $\overline{\text{WRITE CLOCK}}$ | The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (modulo 8). |
| 13 | $\overline{\text{LD}}$ | $\overline{\text{LOAD}}$ | This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user. |
| 14 | $\overline{\text{SHFCLK}}$ | $\overline{\text{SHIFT CLOCK}}$ | Delayed copy of $\overline{\text{WCLK}}$ (pin 12) which is active when EN (pin 19) is at a logic 0. |
| 15 | DOUT | DATA OUT | Serial data output enabled by EN (pin 19). |
| 16 | BDONE | BYTE DONE | This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data. |
| 17 | $\overline{\text{TEST}}$ | $\overline{\text{TEST INPUT}}$ | This pin must be left open by the user. |
| 18 | NC | No Connection | NO CONNECTION |
| 19 | $\overline{\text{EN}}$ | $\overline{\text{ENABLE}}$ | This active low signal enables DOUT, $\overline{\text{SHFCLK}}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state. |
| 20 | $V_{CC}$ | $V_{CC}$ | +5 power supply input. |

## OPERATION

Prior to loading the HDC 1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{\text{EN}}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{\text{DCLK}}$ (pin 11). $\overline{\text{DCLK}}$ also resets BCONE (pin 16). The first BDONE that comes up simply means that the HDC 1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th $\overline{\text{WRITE CLOCK}}$ pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the HDC 1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low transition of the $\overline{\text{WCLK}}$ (pin 12). The low-to-high transition of $\overline{\text{WCLK}}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 WCLK cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, SHFCLK, and $\overline{\text{SHFCLK}}$, can be placed in a high impedance state of setting $\overline{\text{EN}}$ (pin 19) to a logic 1. Likewise, $\overline{\text{EN}}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{\text{TEST}}$ pin is internally OR'd with the counter output to produce the $\overline{\text{LD}}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{\text{TEST}}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

## MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +50°C
Storage Temperature Range ..... −55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any I/O Pin, with respect to ground ..... +7.0V
Negative Voltage on any I/O Pin, with respect to ground ..... −0.2V
Power Dissipation ..... 1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rati... ...tion of the device at these or at any other condition above those indicated in the operational sections of this sp...

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

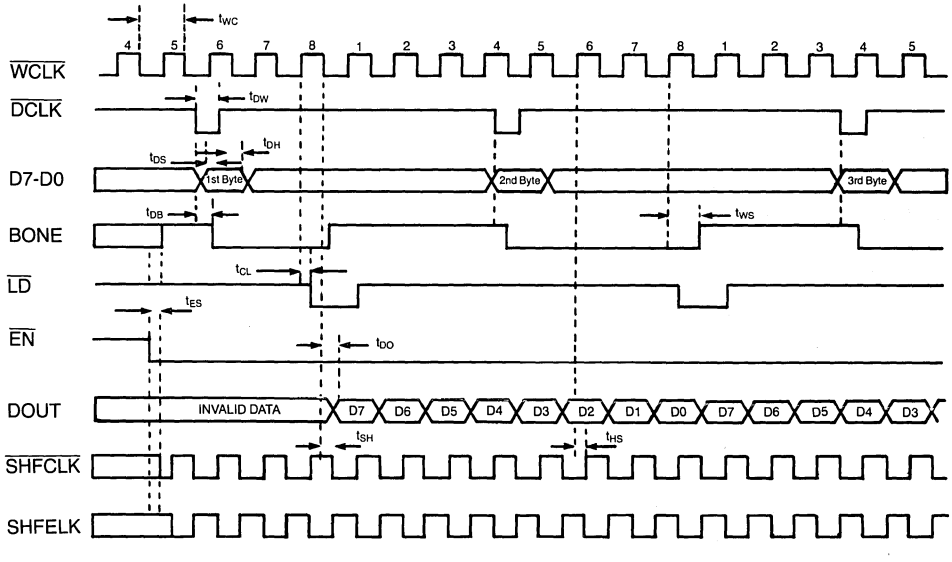
**DC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.2 | | 0.8 | V | |
| $V_{OH}$ | Input High Voltage | 2.4 | | | V | |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = −200μA |
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V | |
| $I_{CC}$ | Supply Current | | | 100 | mA | All Outputs Open |

**AC ELECTRICAL CHARACTERISTICS:** $T_A$ = 0°C to 50°C; $V_{CC}$ = +5V ± 10%, $V_{SS}$ = 0V

| SYMBOL | PARAMETER | MIN | TYP[1] | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $t_{WC}$ | WCLK frequency | | | 5.25 | MHZ | |
| $t_{DW}$ | DCLK pulse width | 50 | | | nsec | |
| $t_{DS}$ | Data set-up w.r.t. ↑ DCLK | 30 | | | nsec | |
| $t_{DH}$ | Data hold time w.r.t. ↑ DCLK | 30 | | | nsec | |
| $t_{DB}$ | ↓ DCLK to ↓ BDONE | | | 130 | nsec | EN = 0 |
| $t_{DO}$ | ↓ WCLK to DOUT | | | 130 | nsec | EN = 0 |
| $t_{SH}$ | ↓ WCLK to ↓ SHFCLK | | | 75 | nsec | EN = 0 |
| $t_{HS}$ | ↓ WCLK to ↑ SHFCLK | | | 70 | nsec | EN = 0 |
| $t_{WB}$ | ↑ $\overline{WCLK}$ to ↑BDONE | 75 | | 180 | nsec | |
| $t_{ES}$ | ↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE | | | 25 | nsec | |
| $t_{CL}$ | ↑ $\overline{WCLK}$ to ↓ $\overline{LD}$ | | | 50 | nsec | |

NOTES: 1. Typical Values are for $T_A$ = 25°C and $V_{CC}$ = +5.0V




SECTION VI

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# HDC 7261D

**PRELIMINARY**

# Hard Disk Controller

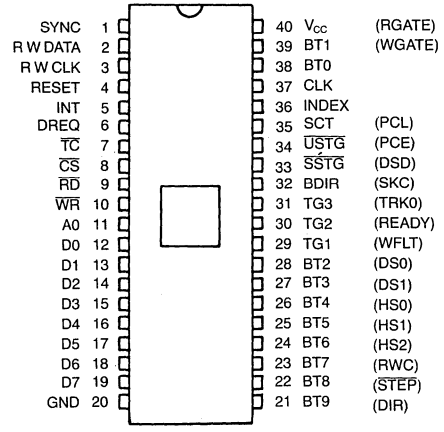
## FEATURES

- ☐ Flexible interface to various types of Hard Disk Drives
- ☐ Programmable Track Format
- ☐ Controls up to 8 Drives
- ☐ Parallel Seek Operation Capability
- ☐ Multi-sector and Multi-track Transfer Capability
- ☐ Data Scan and Data Verify Capability
- ☐ High Level Commands, Including:

| | |
|---|---|
| READ DATA | SEEK (Normal or Buffered) |
| READ ID | RECALIBRATE (Normal or Buffered) |
| WRITE DATA | READ DIAGNOSTIC (SMD Only) |
| WRITE ID | SPECIFY |
| SCAN DATA | SENSE INTERRUPT STATUS |
| VERIFY DATA | SENSE DRIVE STATUS |
| VERIFY ID | DETECT ERROR |
| CHECK | |

- ☐ NRZ, FM, or MFM Data Format
- ☐ Maximum Data Transfer Rate: 12MHz
- ☐ Error Detection and Correction Capability
- ☐ Simple I/O Structure: Compatible with Most Microprocessors
- ☐ All Inputs and Outputs except Clock Pins are TTL-Compatible (Clock Pins Require Pull-up)
- ☐ Single +5V Power Supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

## PIN CONFIGURATION




PACKAGE: 40-pin D.I.P.

**Note:** Signals shown in parentheses are used when the HDC7261 is in the floppy-like mode.

## GENERAL DESCRIPTION

The HDC7261 Hard Disk Controller is an intelligent microprocessor peripheral designed to control a number of different types of disk drives. It is capable of supporting either hard-sector or soft-sector disks and provides all control signals that interface the controller with either SMD disk interfaces or Seagate floppy-like drives. Its sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the HDC7261 and all the data transfers associated with read, write, or format operations are done by the HDC7261 and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The HDC7261 provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

SECTION VI

STANDARD MICROSYSTEMS CORPORATION

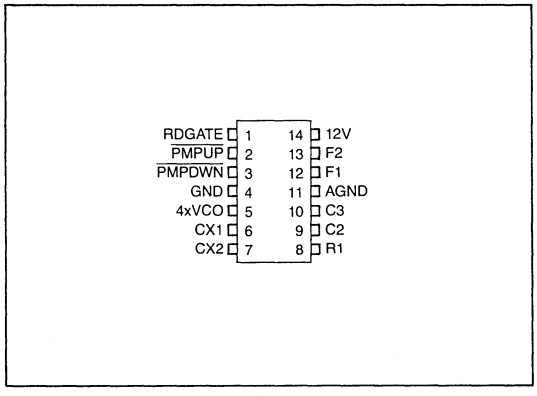
**HDC 9223**
**PRELIMINARY**

# High Performance Analog Data Separator Support Circuit (ADSSC) For Hard Disk

## FEATURES

- ☐ Significantly reduces component count in hard disk systems
- ☐ Completely compatible with the HDC 9226 Hard Disk Data Separator and the HDC 9224 Universal Disk Controller
- ☐ Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- ☐ Eliminates costly critical "tune up" adjustments
- ☐ Space saving 14 pin package
- ☐ Monolithic analog solution reduces critical pc board layout
- ☐ Single + 12V power supply
- ☐ Printed Circuit Board Artwork available to facilitate prototyping and evaluation

## PIN CONFIGURATION




SECTION VI

## GENERAL DESCRIPTION

The HDC 9223 Analog Data Separator Support Circuit (ADSSC) is a 14 pin device, which when used with the HDC 9224 Universal Disk Controller and the HDC 9226 Hard Disk Data Separator significantly simplifies the design of a high performance hard disk data separator.

The HDC 9223, combined with the HDC 9226 and a few resistors and capacitors, forms a phase locked loop which performs phase and frequency locking onto either the MFM or FM data stream output by ST506 or ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9223 and HDC 9226 simplify the task of the designer.

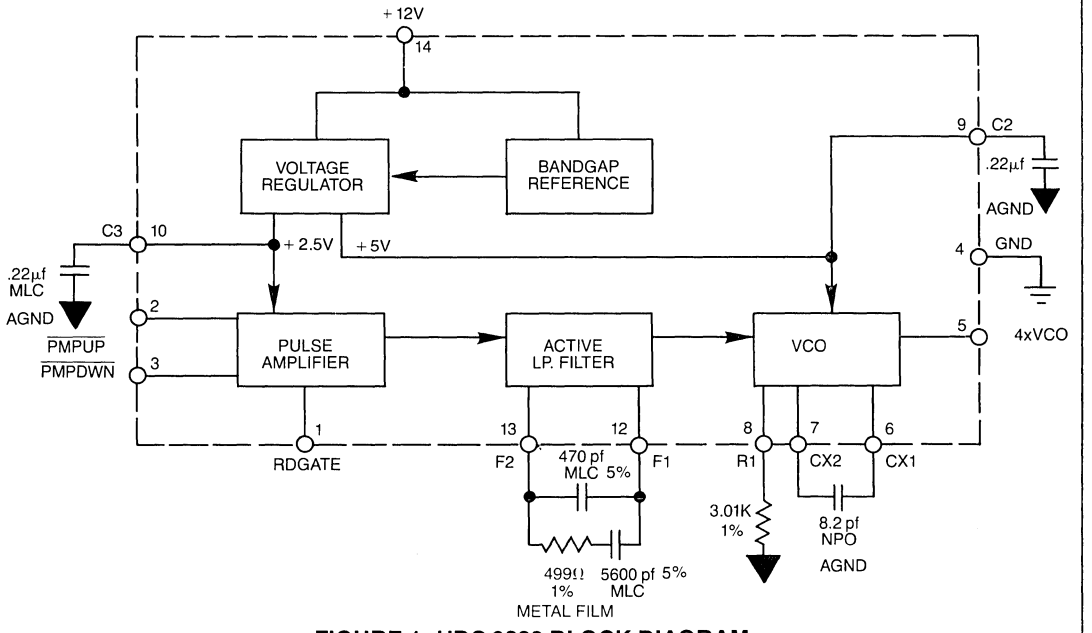



**FIGURE 1: HDC 9223 BLOCK DIAGRAM**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | Read Gate | RDGATE | This active high input controls the gain of the loop. A high level decreases the gain and a low level increases the gain. |
| 2 | $\overline{\text{Pump Up}}$ | $\overline{\text{PMPUP}}$ | This active low input causes the VCO to increase its frequency. |
| 3 | $\overline{\text{Pump Down}}$ | $\overline{\text{PMPDWN}}$ | This active low input causes the VCO to decrease its frequency. |
| 4 | Digital Ground | GND | This is the ground connection for the digital circuitry within the HDC 9223. |
| 5 | Four Times VCO | 4xVCO | This is the VCO output. It will vary from 18 to 22 MHz as a function of the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ input signals. |
| 6 | External Capacitor Connection 1 | CX1 | An 8.2 pf external NPO capacitor is connected across pins 6 and 7. |
| 7 | External Capacitor Connection 2 | CX2 | |
| 8 | External Resistor Connect | R1 | A 3.01K 1% resistor is connected from this pin to Analog Ground. |
| 9 | External Filter Cap Connection 1 | C1 | A .22µf MLC capacitor is connected from this pin to Analog Ground. |
| 10 | External Filter Cap Connection 2 | C2 | A .22µf MLC capacitor is connected from this pin to Analog Ground. |
| 11 | Analog Ground | AGND | This is the ground connection for the analog circuitry within the HDC 9223. |
| 12 | External Filter Connection 1 | F1 | A filter network should be connected to this pin as shown in Figure 4. |
| 13 | External Filter Connection 1 | F2 | A filter network should be connected to this pin as shown in Figure 4. |
| 14 | +12 Volts | 12V | Connect the power supply to this pin. A .22µf bypass capacitor should also be connected from this pin to Analog Ground. |

## DESCRIPTION OF OPERATION

The functional block diagram of the HDC 9223 is shown in Figure 1. The major functional blocks within the HDC 9223 are a voltage controlled oscillator (VCO), an active loop filter, and a pulse amplifier. The gain of the pulse amplifier is controlled by the RDGATE logic input.

The voltage controlled ocsillator generates the 4xVCO output (nominally 20 MHz). The frequency of this output is determined by the signals on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ inputs to the HDC 9223. Since the half bit time for data from the disk is 100ns, the HDC 9226 divides the frequency of the 4xVCO signal in half, and compares the phase and frequency of the resulting 10 MHz signal to that of the incoming data. The HDC 9226 then varies the pulse width on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ lines to adjust the output frequency of the VCO on the HDC 9223, closing the loop.

A voltage regulator and bandgap voltage reference ensure power supply rejection and stable VCO operation.

## MAXIMUM GUARANTEED RATINGS

| | |
|---|---|
| Operating Temperature Range | 0 to 70 C |
| Storage Temperature Range | −55 to +150 C |
| Lead Temperature (soldering, 10 sec) | +300 C |
| Positive Voltage on any Pin, with respect to Ground | $V_{CC}$ +0.5V |
| Negative Voltage on any Pin, with respect to Ground | −0.5V |

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibly exists it is suggested that a clamp circuit be used.

## DC ELECTRICAL SPECIFICATIONS

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

($T_A$ = 0C to 70C, $V_{CC}$ = 12.0V ± 5%)

| Parameter | Min. | Max. | Units | Comments |
|---|---|---|---|---|
| SUPPLY CURRENT | | | | |
| $I_{CC}$ | | 50 | mA | |
| SUPPLY VOLTAGE | | | | |
| $V_{CC}$ | 11.4 | 12.6 | V | 12V ± 5% |
| INPUT VOLTAGE | | | | |
| $V_{IL}$ | | 2.4 | V | $I_{OL}$ = 2.0mA |
| $V_{IH}$ | 3.6 | | V | $I_{OH}$ = −400μA |
| OUTPUT VOLTAGE | | | | |
| $V_{OL}$ | | 1.2 | V | $I_{OL}$ = 2.0mA |
| $V_{OH}$ | 4.1 | | V | $I_{OH}$ = −400μA |
| INPUT CURRENT | | | | |
| $I_{IL}$ | | −10 | μA | $V_{IL}$ = 0.8V |
| $I_{IH}$ | | 40 | μA | $V_{IH}$ = 3.0V |

## AC ELECTRICAL CHARACTERISTICS

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

($T_A$ = 0C to 70C, $V_{CC}$ = 12.0V ± 5%)

| Parameter | Symbol | Min. | Max. | Units | Comments |
|---|---|---|---|---|---|
| $\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ pulse width | $t_{PW}$ | 15 | 125 | ns | Measured at 50% amplitude (Fig. 2) |
| $\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ rise time | $t_{IR}$ | | 10 | ns | Measured between 0.6 and 1.8V (Fig. 2) |
| $\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ fall time | $t_{IF}$ | | 10 | ns | Measured between 0.6 and 1.8V (Fig. 2) |
| Output Frequency (when locked) | | 18 | 22 | MHz | |
| 4xVCO rise time | $t_{OR}$ | | 15 | ns | Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3) |
| 4xVCO fall time | $t_{OF}$ | | 15 | ns | Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3) |
| 4xVCO pulse width high | $t_{OH}$ | 16 | | ns | Fig. 3 Measured at 2.5V |
| 4xVCO pulse width low | $t_{OL}$ | 16 | | ns | Fig. 3 Measured at 2.5V |

SECTION VI

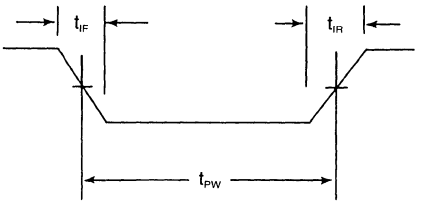



**FIGURE 2:**
**$\overline{\text{PMPUP}}$/$\overline{\text{PMPDWN}}$ TIMING**

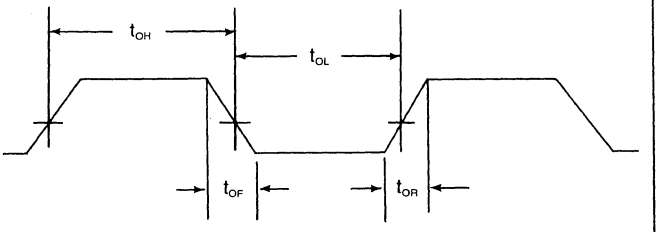



**FIGURE 3: 4xVCO TIMING**

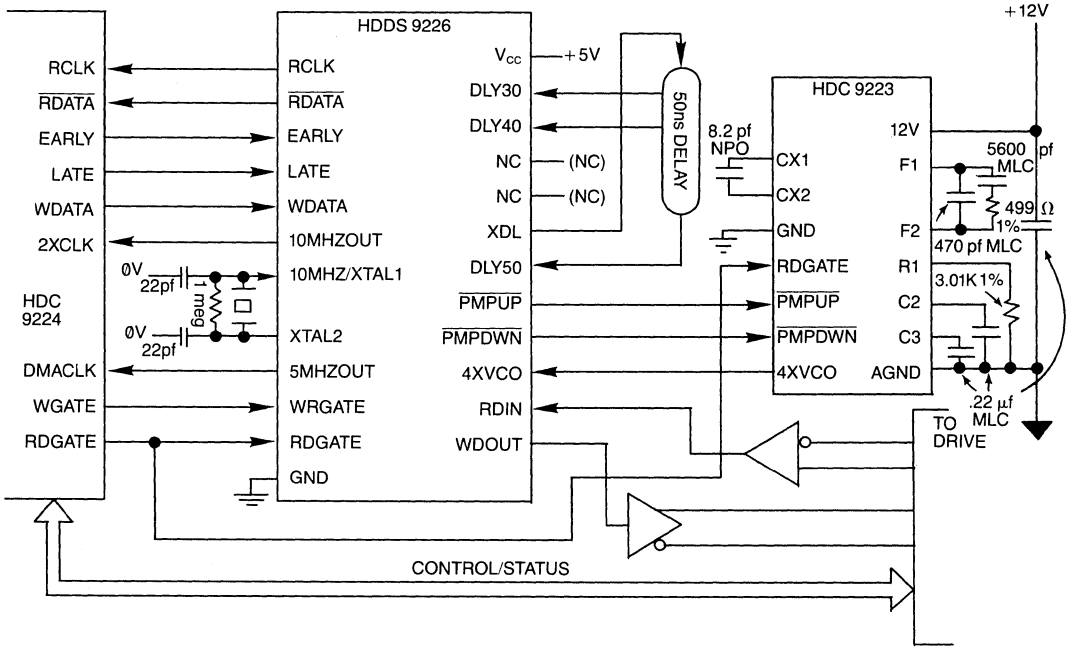



**FIGURE 4: TYPICAL CIRCUIT CONFIGURATION**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273 3100 TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications: consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# HDC 9224

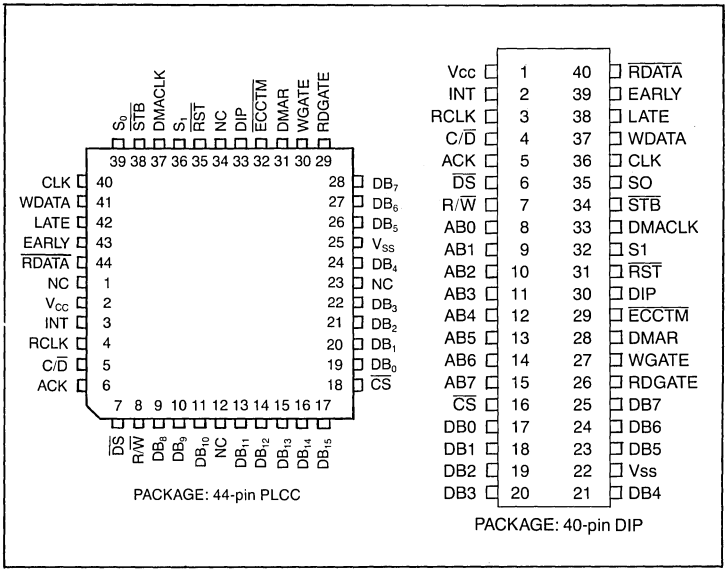
# Universal Disk Controller

## FEATURES

### Programmable Disk Drive Interface and Formats

- ☐ Seagate (ST506) or user definable Hard Disk Formats
- ☐ IBM Compatible Single or Double Density Floppy Disk Formats
- ☐ Controls 8", 5.25", and 3.5" drives
- ☐ Controls tape drives for tape backup of disks
- ☐ Full CRC generation and checking
- ☐ Internal or External Error detection
- ☐ Programmable user-transparent Error correction
- ☐ Programmable automatic retry option
- ☐ Programmable internal write precompensation logic
- ☐ Read/Write commands with automatic seek
- ☐ Multiple sector read/write transfers
- ☐ Sector interleave capability
- ☐ Internal address mark generation and detection
- ☐ Programmable track step rates
- ☐ Supports both buffered and unbuffered seeks
- ☐ Polling command allows overlapping seeks
- ☐ Powerful, high level command set
- ☐ Controls up to 4 drives with
  - ☐ up to 16 heads per drive
  - ☐ up to 2048 cylinders per drive
  - ☐ up to 256 sectors per track

## PIN CONFIGURATION




### Flexible System Interface

- ☐ Built-in DMA controller capable of addressing up to 16 MBytes
- ☐ Supports either private or virtual buffer memory addressing schemes
- ☐ User readable Interrupt, Chip Status, and Drive Status registers
- ☐ Programmable Interrupt Mask
- ☐ TTL compatible
- ☐ Standard 40 pin DIP package
- ☐ Single +5 volt supply

## GENERAL DESCRIPTION

The HDC 9224 Universal Disk Controller (UDC) is a 40 pin, n-channel MOS/LSI device capable of interfacing up to 4 Winchester-type hard disks and/or industry standard floppy disks to a processor. The chip is programmable to support both the Seagate (ST506) and user defined hard disk formats, as well as IBM compatible 8", 5.25" and 3.5" single and double density formats.

A powerful and sophisticated command set reduces the software overhead required to implement a combined hard disk/floppy disk controller. These commands include:

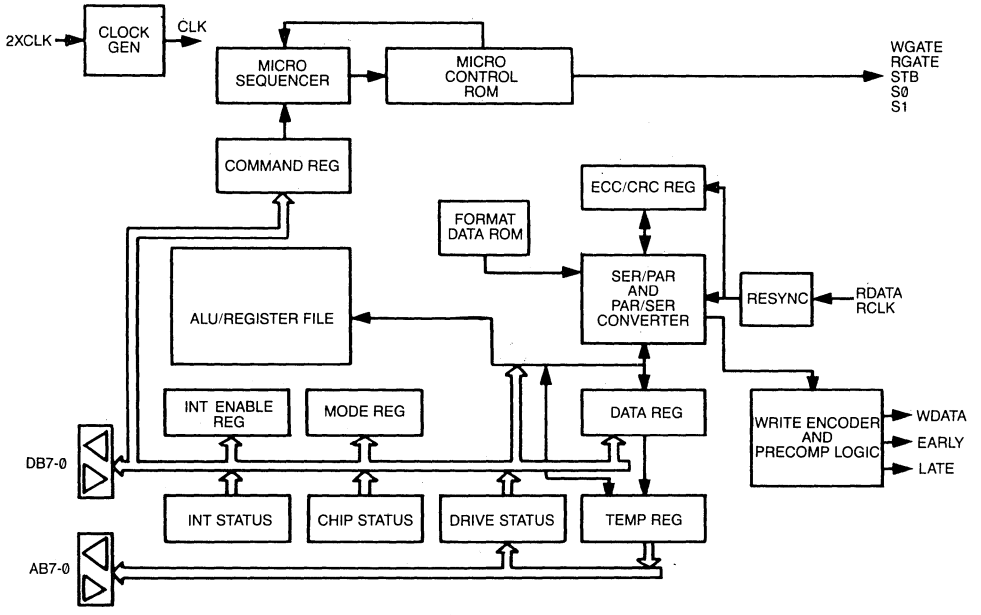
| | |
|---|---|
| Drive Select | Seek to cylinder and read ID |
| Step out 1 cylinder | Step in 1 cylinder |
| Restore Drive | Read Logical Sectors |
| Read Physical Sectors | Read Entire Track |
| Write Logical Sectors | Write Physical Sectors |
| Chip Reset | Deselect Drive |
| Poll Drives for Ready | Set Register Pointer |
| Tape Back-up | Format current track |

The HDC 9224 can use both private memory or shared memory buffers with the chip's internal DMA controller providing up to 24 bit addresses over an 8 bit data bus. This enables the HDC 9224 to address up to 16 megabytes of memory, and allows the hardware designer tremendous flexibility in system design.

Several techniques of error detection and correction are implemented on the HDC 9224. One user selected method allows the chip to detect and transparently correct a read error in the data-stream, without external logic. Another technique allows the designer complete control over the ECC algorithm, by using external logic or system software to detect and correct the error. As a further aid in error handling, the HDC 9224 allows the user to specify the number of read retries to be attempted before an error is reported to the host processor by the HDC 9224.

The HDC 9224 features a versatile track format command which allows formatting with interleaved sectors. The chip needs only 3 or 4 bytes of external memory space per sector (depending on format selected). This feature allows the designer to optimize sector interleaving for optimum throughput.

SECTION VI




**BLOCK DIAGRAM OF DATA PATH IN HDC 9224**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | Power | $V_{CC}$ | +5 volt power supply pin |
| 22 | Ground | $V_{SS}$ | System ground |
| 16 | Chip Select | $\overline{CS}$ | This signal (when active) selects the HDC 9224 for communications with the host processor. This signal is normally derived by decoding the high order address bits. It is active low. |
| 17,18<br>19,20<br>21,23<br>24,25 | Data Bus 7-0 | DB7-0 | All system processor reads and writes, (including status reads, initialization, disk parameters, and commands) are 8 bit transfers which utilize these lines.<br>When the UDC is accessing memory, data is input or output on these lines.<br>Data on these lines is valid only when $\overline{DATA\ STROBE}$ ($\overline{DS}$) is active low. |
| 8-15 | Aux Bus 7-0 | AB7-0 | These 8 pins are used to output drive control signals and DMA Address information.<br>Additionally, these pins are used to input drive status information. |
| 4 | Command/$\overline{Data}$ | C/$\overline{D}$ | During processor to UDC communications, this input is used to indicate whether a command or data transfer will follow.<br>If this pin is low, data may be written to, or read from, the internal data registers.<br>If this pin is high, the processor may write commands or read command results from the UDC. |
| 7 | Read/$\overline{Write}$ | R/$\overline{W}$ | When the processor is communicating to the UDC, a high on this input line indicates a (processor) request for a UDC read operation, and a low indicates a (processor) request for a write operation.<br><br>R/$\overline{W}$ C/$\overline{D}$ Operation<br>0 0 Write to register file<br>0 1 Write to command reg.<br>1 0 Read from register file<br>1 1 Read Interrupt Status Register<br><br>During UDC initiated operations, this pin becomes an output, and is used to indicate a read operation (logic 1) or write operation (logic 0) to external memories. |

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 6 | $\overline{\text{Data Strobe}}$ | $\overline{\text{DS}}$ | This active low pin functions as both an input and output. When the processor is writing to the UDC, the trailing edge of an active (low) signal applied to this pin indicates that the data on DB7-0 is valid, and the data is latched into the appropriate UDC register on the rising edge.<br>When the processor is reading from the UDC, the trailing edge of an active (low) signal applied to this pin is used to clock out the desired UDC register on to DB7-0.<br>During UDC initiated DMA operations, the UDC drives this pin low to either read or write data from memory. On DMA read cycles, data is clocked in on the trailing edge. On DMA write operations, the data on DB7-0 is valid anytime this pin is active (low).<br>When this pin is high (logic 1), DB7-0 return to a high impedance state. |
| 2 | Interrupt | INT | This active high output is used by the UDC whenever it wants to interrupt the processor. The interrupt pin is reset to its inactive (low) state when the UDC interrupt status register is read. |
| 30 | DMA In Progress | DIP | This active high output becomes active whenever the UDC is actually performing a DMA operation. |
| 28 | DMA Request | DMAR | This active high output becomes active whenever the UDC requires the system bus to perform a memory cycle, and ACK is inactive. During hard disk operations, it remains active until the sector transfer is complete.<br>During floppy disk operations, it is active for 1 byte transfer time.<br>The UDC shows that is has released the system bus by resetting this signal to its inactive (low) state. |
| 5 | Acknowledge | ACK | This active high signal from the processor tells the UDC that the processor has released the system bus and the UDC may access system memory. |
| 37 | Write Data | WDATA | This pin is used to output serial data from the UDC to the drive, in either FM or MFM format. In both cases, data is output with the most significant bit first. |
| 38 | Late | LATE | This output (when active high) indicates that the current flux transition appearing on WDATA is to be written late. |
| 39 | Early | EARLY | This output (when active high) indicates that the current flux transition appearing on WDATA is to be written early. |
| 27 | Write Gate | WGATE | This output (when active high) indicates the drive should allow a write operation. |
| 40 | $\overline{\text{Read Data}}$ | $\overline{\text{RDATA}}$ | This input pin contains the serial bit stream read from the drive, in either FM or MFM format. Media flux reversals are indicated by a negative transition. |
| 3 | Read Clock | RCLK | This input is generated by the external data separator. Its frequency should self-adjust to the variations in bit width in the data stream from the drive. This clock supplies a window to indicate half-bit-cell boundaries. |
| 26 | Read Gate | RDGATE | This output pin is used to enable the external data separator, compensate for write to read recovery time of the drive, and filter out the write splice in gaps 2 and 3. The timing of this signal is dependent upon the type of drive (hard or floppy) being used.<br>RDGATE is inactive at all times except when the UDC is actually performing a read operation or an internal ECC operation. |
| 29 | $\overline{\text{ECC Time}}$ | $\overline{\text{ECCTM}}$ | When the UDC is used in external ECC mode, this output pin becomes active (low) during the time the UDC is reading the ECC bytes from memory or external ECC chip, when executing a WRITE command.<br>It is also active during internal ECC correction operations, and for either one (write) or two (read) byte times after DIP (pin 30) becomes inactive following a sector transfer. This shows the system processor when it should service the UDC buffer. |
| 32,35 | Select 1,0 | S1,S0 | These active high outputs are used by external logic to select either the source or destination for data transfers occuring via AB7-0. The following table defines the specific transfer being called for by the UDC. (Note that S1-0 are valid only when $\overline{\text{STB}}$ is active low.) |

| $\overline{\text{STB}}$ | S1 | S0 | AB7-0 Activity |
|---|---|---|---|
| 1 | X | X | S1,S0 Invalid |
| 0 | 0 | 0 | UDC inputs Drive Status Signals |
| 0 | 0 | 1 | UDC outputs DMA address bytes |
| 0 | 1 | 0 | UDC outputs OUTPUT 1 signals |
| 0 | 1 | 1 | UDC outputs OUTPUT 2 signals |

| PIN NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 34 | Strobe | STB | This active low output indicates when the host processor should read or write to AB7-0, as indicated by S1-0.<br>When AB7-0 are used as outputs from the UDC, data is valid anytime this signal is active (low).<br>When AB7-0 are used as inputs to the UDC, data is clocked in on the rising edge of this signal. |
| 36 | DEVICE CLOCK | CLK | This input is the double frequency clock used by the UDC for all internal timing operations.<br>Eight inch hard disk drives (with a nominal bit time of 230 ns) require an input of 8.696 MHz (115 ns period).<br>5.25" hard disks (with a nominal bit time of 200 ns) require a 10 MHz input (100 ns period).<br>Eight inch, 5.25" and 3.5" floppy drives all require a 10 MHz clock, which is internally prescaled by the UDC to the correct frequency, as determined from the Drive Select command and MODE register.<br>This input requires an external pull-up resistor, as it is not TTL-level compatible. See figure 2. |
| 31 | Reset | RST | This active low input will force the UDC into the following known state:<br>INT–Inactive low<br>WDATA–Inactive low<br>ECCTM–Inactive high<br>DMAR–Inactive low<br>EARLY–Inactive low<br>C/D–Input<br>AB7-0–Input<br>LATE–Inactive low<br>R/W–Input<br>DB7-0–Input<br>WGATE–Inactive low<br>DIP–Inactive low<br>RDGATE–Inactive low<br>DS–Input<br>An active low on this pin has the same effect as a RESET Command. |
| 33 | DMA Clock | DMACLK | All UDC DMA operations will be synchronized to this clock input. Three DMACLK periods are required for each DMA byte transfer. |

## OVERVIEW OF UDC REGISTERS

The HDC 9224 has three types of internal, processor addressable registers; Read/Write, Read Only, and Write Only. These registers are addressed by an internal register pointer that is set by the SET REGISTER POINTER command.

All register data is passed to and from the UDC via the data bus (DB7-0).

The internal register pointer is automatically incremented with each register access until it points to the DATA Register. This insures that all subsequent register accesses will address the DATA register.

### PROCESSOR ACESSIBLE REGISTERS

| REGISTER ADDR | WRITE | READ |
|---|---|---|
| 0 | DMA7-0 | DMA7-0 |
| 1 | DMA15-8 | DMA15-8 |
| 2 | DMA23-16 | DMA23-16 |
| 3 | Desired Sector | Desired Sector |
| 4 | Desired Head | Current Head |
| 5 | Desired Cylinder | Current Cylinder |
| 6 | Sector Count | Temporary Storage |
| 7 | Retry Count | Temporary Storage |
| 8 | Mode | Chip Status |
| 9 | Interrupt/Command Terminator | Drive Status |
| A | Data/Delay | Data |
| COMMAND | Current Command | Interrupt Status |

Three internal registers (OUTPUT 1, OUTPUT 2, and INPUT DRIVE STATUS) which are not directly addressable by the processor are accessed by the UDC. The information contained in these registers is used in disk interfacing and is input or output on UDC Pins AB7-0. The following table describes these registers and the signals they output or input on AB7-0.

### UDC ADDRESSABLE REGISTERS

| DRIVE STATUS REGISTER (input) | Select Pins S1 = 0, S0 = 0 |
|---|---|
| AB7—ECC Error | AB6—Index Pulse |
| AB5—Seek Complete | AB4—Track 00 |
| AB3—User Defined | AB2—Write Protect |
| AB1—Drive Ready | AB0—Write Fault |

| OUTPUT 1 (Output) | Select Pins S1 = 1, S0 = 0 |
|---|---|
| AB7—Drive Select 3 | AB6—Drive Select 2 |
| AB5—Drive Select 1 | AB4—Drive Select 0 |
| AB3—Programmable Outputs (see text) | AB2—Programmable Outputs |
| AB1—Programmable Outputs | AB0—Programmable Outputs |

| OUTPUT 2 (Output) | Select Pins S1 = 1, S0 = 1 |
|---|---|
| AB7—Drive Select 3 | AB6—Reduce Write Current |
| AB5—Step Direction | AB4—Step Pulse |
| AB3—Desired Head (Bit 3) | AB2—Desired Head (Bit 2) |
| AB1—Desired Head (Bit 1) | AB0—Desired Head (Bit 0) |

Additionally, several registers (DMA7-0, DMA15-8, DMA23-16, DESIRED SECTOR, DESIRED CYLINDER, SECTOR COUNT, and RETRY COUNT) serve an alternate purpose. These registers are used by the FORMAT TRACK command to hold parameters. This alternate register utilization is described in detail under the FORMAT TRACK command.

## DESCRIPTION OF UDC REGISTERS

**DMA 7-0 (R/W Register; Address 0)**
This 8-bit read/write register is loaded with the low order byte (MSB in bit 7) of the DMA buffer memory starting address.

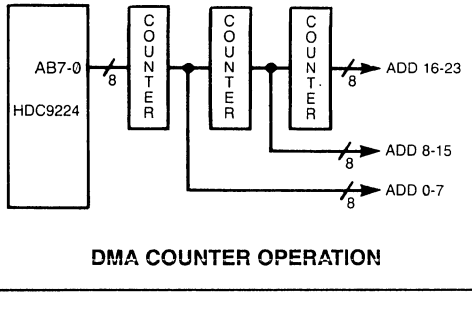
**DMA 15-8 (R/W Register; Address 1)**
This 8-bit read/write register is loaded with the middle order byte (MSB in bit 7) of the DMA buffer memory starting address.

**DMA 23-16 (R/W Register; Address 2)**
This 8 bit read/write register is loaded with the high order byte (MSB in bit 7) of the DMA buffer memory starting address.

Prior to the data transfer portion of a read or write command, the UDC writes the contents of the DMA registers to an external counter. This transfer (from the registers to the external counter) is accomplished by the UDC with 3 separate outputs on AB7-0, with the contents of DMA 24-16 being transfered first. (In memory areas that require less than 24 bit addressing, the higher order bits are overwritten. The external counter must be incremented with the UDC's $\overline{DS}$ signal after each byte transfer.

If, during read operations, an error is detected during the data transfer, a retry will occur (if so programmed), and the three DMA registers will re-initialize the external counter to the original starting address.

During multiple sector read/write operations, the DMA address contained in the DMA registers will be incremented by the size of the sector selected at each sector boundary. This ensures that during read operations the address contained in the DMA registers always corresponds to the proper memory starting address of the sector currently being read.




DMA COUNTER OPERATION

**DESIRED SECTOR REGISTER (R/W Register; Address 3)**
This 8-bit read/write register is loaded with the starting sector number of a multiple sector read/write operation. Except for the last sector of the operation, this register is incremented after each sector is written or read without error.

If the UDC terminates a command because of an error, this register will normally contain the bad sector number, and may be read by the processor.

**DESIRED HEAD REGISTER (Write Register; Address 4)**
This 8-bit write only register is loaded with the 4-bit head number, and the upper 3 bits of the desired cylinder number.

BIT 7 ALWAYS 0
BITS 6-4 MSBs of the Desired Cylinder number
BITS 3-0 Desired Head Number.

The desired head number is output on AB3-0 during OUTPUT 2 times.

**DESIRED CYLINDER REGISTER (Write Register; Address 5)**
This 8-bit write only register is loaded with the 8 low order bits of the desired cylinder (MSB in Bit 7). Combined with the 3 high order bits loaded into the DESIRED HEAD REGISTER, these 11 bits form the desired cylinder number, which is checked by read and write operations during the Check ID portion of the command.

**SECTOR COUNT REGISTER (Write Register; Address 6)**
This 8-bit write only register is loaded with the number of sectors to be operated on by the read or write command. This allows multiple sectors on the same cylinder to be either written or read.

**RETRY COUNT REGISTER (Write Register; Address 7)**
This 8-bit write only register is loaded with the number of times the UDC should retry to read a data field before reporting an error. Additionally, this register is loaded with the user programmable output signals that the UDC outputs on AB0-3 during OUTPUT 1 times.

The retry count is loaded (in 1's complement format) into the 4 most significant bits of this register.

The user programmable output signals are loaded into the 4 least significant bits of the register.

BITS 7-4 Desired Retry Count (in 1's complement format)
BITS 3-0 User Programmable Output Signals

**MODE REGISTER (Write Register; Address 8)**
This 8-bit write only register defines the operating mode of the UDC as follows:

BIT 7 (DRIVE DATA TYPE)
This bit determines how the UDC decodes data from the drive.

BIT 7 = (1): UDC configured for hard disk use. (Level transitions)
BIT 7 = (0): UDC configured for floppy use. (Pulse inputs)

BITS 6,5 (CRC/ECC Enable Code)
These bits determine the error detection/correction code generated and checked by the UDC.

| DB6 | DB5 | CODE GENERATED/CHECKED |
|---|---|---|
| 0 | 0 | CRC |
| 0 | 1 | External ECC |
| 1 | 0 | Internal 32 bit ECC without correction |
| 1 | 1 | Internal 32 bit ECC with correction |

With internal ECC selected the UDC will transfer 4 extra bytes during reads and writes. Normal CRC checking is still done on all ID fields.

With external ECC selected the UDC will flag an ECC error via BIT 7 of the DRIVE STATUS REGISTER. Normal CRC checking is still done on all ID fields.

If neither internal or external ECC is selected, then the UDC will perform CRC checks on both data and ID fields.

**STEP RATES FOR DOUBLE DENSITY (MFM) OPERATION** **(Mode Bit 4 = 0)**

| DRIVE TYPE | | | 5.25" HARD DISK | 8" FLOPPY | 5.25" FLOPPY |
|---|---|---|---|---|---|
| DB2 | DB1 | DB0 | STEP RATE | STEP RATE | STEP RATE |
| 1 | 1 | 1 | 12.8 ms | 128 ms | 256 ms |
| 1 | 1 | 0 | 6.4 ms | 64 ms | 128 ms |
| 1 | 0 | 1 | 3.2 ms | 32 ms | 64 ms |
| 1 | 0 | 0 | 1.6 ms | 16 ms | 32 ms |
| 0 | 1 | 1 | 0.8 ms | 8 ms | 16 ms |
| 0 | 1 | 0 | 0.4 ms | 4 ms | 8 ms |
| 0 | 0 | 1 | 0.2 ms | 2 ms | 4 ms |
| 0 | 0 | 0 | 17.6 us * | 176 us * | 352 us * |
| 0 | 0 | 0 | 21.8 us ** | 218 us ** | 436 us ** |
| Pulse Width: | | | 11.2 us | 112 us | 224 us |

*This rate applies for SEEK commands only
**This rate applies for RESTORE commands only

**(DOUBLE ALL OF THE ABOVE TIMES FOR SINGLE DENSITY (FM) OPERATIONS.)**

BIT 4 (Single or Double Density)
This bit determines whether the UDC will perform its operations in either single or double density.

BIT 4 = (1) Single Density (FM) Format
BIT 4 = (0) Double Density (MFM) Format

BIT 3 (ALWAYS 0)

BITS 2,1,0 (Step Rate Select)
These bits are programmed to select the desired drive step rate. Note that all step rates are determined by the type of drive and density selected, and are scaled from the CLK input.

The UDC can output extremely rapid step rate pulses if these bits are set to 000. This is useful when the UDC is controlling drives which support buffered seeks. For other speeds, please refer to the table above.

**INTERRUPT/COMAND TERMINATION REGISTER (Write Register; Address 9)**

This 8-bit write only register allows the programmer to mask out a number of conditions that would cause termination of a command. (Such termination occurs when the DONE bit in the INTERRUPT STATUS register is set.) One bit in this register also controls the generation of interrupts when either the DONE bit or the READY CHANGE bit in the INTERRUPT STATUS register go active.

BIT 7 (CRC PRESET)
Setting this bit to "1" will cause the CRC register to preset to 1 for CRC generation and checking. Setting this bit to "0" will cause the CRC register to preset to 0 for CRC generation and checking.

ID field CRC and data field CRC or ECC are generated and tested from the first A1 HEX byte in the ID field.

BIT 6 (ALWAYS "0")
This bit should always be set to "0" by the user. Failure to do this may result in unreliable operation.

BIT 5 (INT ON DONE)
If this bit is set (to "1"), an interrupt will occur when the DONE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

BIT 4 (DELETED DATA MARK)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the DELETED DATA MARK bit in the CHIP STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 3 (USER DEFINED)
If this bit is set (to "1"), the DONE bit in the INTERRUPT STATUS register will be set when the USER DEFINED status bit in the DRIVE STATUS register goes active, and the command will terminate when the current sector operation is completed.

BIT 2 (WRITE PROTECT)
If this bit is set to (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE PROTECT bit in the DRIVE STATUS register goes active.

BIT 1 (READY CHANGE)
If this bit is set (to "1"), an interrupt will occur when the READY CHANGE bit in the INTERRUPT STATUS register is set. If this bit is reset (to "0"), no interrupt will be generated for this condition.

The user should note that as a drive is selected or deselected, it is possible for the ready line from the drive to change state, and care should be taken in the design of the interrupt handler.

BIT 0 (WRITE FAULT)
If this bit is set (to "1"), the write or write format command in progress will terminate and the DONE bit in the INTERRUPT STATUS register will be set when the WRITE FAULT status bit in the DRIVE STATUS register is set. The command in progress will terminate when the current sector operation is completed.

**DATA/DELAY REGISTER (R/W Register; Address 0AH)**

This 8-bit read /write register serves a dual purpose. During UDC writes, data is placed in this register for recording to the disk. During UDC reads, recovered data is fetched from this register for storage into memory. All transfers occur via DB7-0, under DMA control.

Additionally, this register is loaded with the HEAD LOAD TIMER COUNT when the Drive Select command is issued. (Note that the actual amount of head load time is this value, times a value predetermined by the UDC, based on the type of drive selected. For more information, please see the Drive Select command description.)

**COMMAND REGISTER (Write Register)**

This 8-bit write only register is used to pass commands to the UDC. Valid commands are given to the UDC by setting C/$\overline{D}$ high and R/$\overline{W}$ active high, while strobing $\overline{DS}$ active (low).

**CURRENT HEAD REGISTER Read Register; Address 4)**

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register contains the actual head number, bad sector flag, and the 3 most significant bits of the cylinder number, as specified during formatting.

BIT 7 = (1) Last sector read had BAD SECTOR bit set
BIT 7 = (0) Last sector read had BAD SECTOR bit reset.

BITS 6-4 Three most significant bits of the current cylinder. (Most significant bit in Bit 6.)

BITS 3-0 Current Head Number (MSB in bit 3).

**CURRENT CYLINDER REGISTER (Read Register; Address 5)**

This 8-bit read only register is updated from the disk when a valid ID field sync mark is found while executing a read ID field command sequence. This register will contain the 8 least significant bits of the cylinder ID number, as specified during formatting. (The 3 most significant bits of the 11 bit cylinder ID number are contained as part of the CURRENT HEAD REGISTER.)

**INTERRUPT STATUS REGISTER (Read Register)**

This 8-bit read only register contains status information associated with interrupt conditions and errors that occur during disk operation. This register is read by setting C/$\overline{D}$ high, and R/$\overline{W}$ high.

When the Interrupt Status register is read, the INT output signal from the UDC will be reset (to an inactive low level).

BIT 7 (INTERRUPT PENDING)
A "1" indicates that either DONE bit or READY CHANGE bit has gone active. The user may disable these interrupts by setting the appropriate bits in the INTERRUPT/COMMAND TERMINATION, REGISTER. This bit is reset (to "0") by reading the Interrupt Status register.

BIT 6 (DMA REQUEST)
A "1" indicates that the UDC requires a data transfer either to or from its data register. This bit is reset (to "0") by the data transfer.

BIT 5 (DONE)
A "1" indicates that the current command is completed. This bit is reset (to "0") when a new command is issued.

BIT 4,3 (COMMAND TERMINATION CODE)
(Valid only when DONE is set)
These two bits indicate the command termination conditions:

| BIT 4 | BIT 3 | CONDITIONS |
|---|---|---|
| 0 | 0 | Successful command termination |
| 0 | 1 | Execution error in READ ID Sequence |
| 1 | 0 | Execution error in SEEK Sequence |
| 1 | 1 | Execution error in DATA field |

More detailed command termination error information is obtained by reading the Chip Status register.

BIT 2 (READY CHANGE)
A "1" indicates that the "ready" signal from the drive has experienced a low-to-high or high-to-low transition. (This shows that the drive has either become ready or become not ready.) This bit is reset (to "0") by reading the Interrupt Status register.

BIT 1 (OVERRUN/UNDERRUN)
A "1" indicates that a overrun or underrun condition has occured during a read or write command. These conditions occur when the UDC does not receive an acknowledge (to a DMA request) by the time a byte is ready for transfer to or from the processor.

This bit can only be reset (to "0") with a RESET command or a high on the RESET pin.

BIT 0 (BAD SECTOR)
A "1" indicates that a bad sector (as indicated from the MSB of the head ID byte in the ID field) has been encountered. This bit is reset when a new command is issued, or a good sector is read.

**CHIP STATUS REGISTER (Read Register; Address 8)**

This 8-bit read only register supplies additional chip status information. The information in this register is only valid between the time that the DONE bit is set in the INTERRUPT STATUS register and the time when the next command is issued to the UDC.

BIT 7 (RETRY REQUIRED)
If a retry was attempted by the UDC during the execution of any read or write command, this bit is set (to "1").

BIT 6 (ECC CORRECTION ATTEMPTED)
If the internal ECC circuitry has attempted to correct a bad sector, this bit is set (to "1").

BIT 5 (CRC/ECC ERROR)
If the UDC detects a CRC error or an ECC error, this bit is set (to "1").

BIT 4 (DELETED DATA MARK)
If the UDC reads a deleted data mark in the ID field, this bit is set (to "1"), otherwise it is reset (to "0").

BIT 3 (SYNC ERROR)
If the UDC does not find a sync mark when it is attempting to read either an ID or data field, then this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 2 (COMPARE ERROR)
If the information contained in the DESIRED HEAD and DESIRED CYLINDER registers does not match that contained in an ID field on the disk, this bit is set (to "1"). The command being executed will terminate when this bit is set.

BIT 1,0 (PRESENT DRIVE SELECTED)
These two binary encoded bits represent the drive currently selected and correspond to the Drive Select bits set in the Output 1 and Output 2 latches.

| BIT 1 | BIT 0 | DRIVE SELECTED |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

## DRIVE STATUS REGISTER (Read Register; Address 9)

This 8-bit read only register contains status information generated by the drives, external ECC Chip (if any), and a user definable input to the UDC from the drive.

To save pins on the UDC, the 8 status lines are input on AB7-0 and are latched in this internal register. The UDC will update this register whenever it is not using AB7-0 to output DMA counter values, OUTPUT 1, or OUTPUT 2 data. When configured as described below, the UDC will input drive status signals and interpret them as follows. In all cases, a logic "1" is considered the active input.

BIT 7 (ECC ERROR)
This bit is set (to "1") when the ECC ERROR signal is generated by an external ECC chip. This signal is input to the UDC on AB7.

BIT 6 (INDEX)
This bit is set (to "1") when the INDEX signal from the selected drive is active. Typically, index pulses from the drives are active for 10us-100us for each disk revolution. This signal is input to the UDC on AB6.

BIT 5 (SEEK COMPLETE)
This bit is set (to "1") when the SEEK COMPLETE signal from the selected drive is active. This bit will go active when the heads of the selected drive have settled over the desired track (at the completion of a seek).

When a drive supplies this signal, reading and writing should not be attempted until SEEK COMPLETE is set (to "1"). This signal is input on AB5.

For floppy disk operation, where the drives normally do not provide this signal, a retriggerable one shot could be used to generate a SEEK COMPLETE signal (if desired).

BIT 4 (TRACK 00)
This bit is set (to "1") when the TRACK 00 signal from the selected drive is active. This indicates that the heads on the selected drive are positioned over track 0. This signal is input on AB4.

BIT 3 (USER DEFINED)
This bit is set (to "1") when the USER DEFINED signal is active. This signal is input on AB3.

BIT 2 (WRITE PROTECT)
This bit is set (to "1") when the WRITE PROTECT signal from the selected drive is active. When set, this bit indicates that the disk in the selected drive is write protected. This signal is input on AB2.

BIT 1 (READY)
This bit is set (to "1") when the READY signal from the selected drive is active. When set, this bit indicates that the drive is ready to execute commands. This signal is input on AB1.

BIT 0 (WRITE FAULT)
This bit is set (to "1") when the WRITE FAULT signal from the selected drive is active. This signal, when active, indicates that a condition exists at the drive that would cause improper writing on the disk. This signal is input to the UDC on AB0.

## TEMPORARY STORAGE REGISTERS

The UDC contains two temporary storage registers, used by the UDC for internal operations. The host processor should not attempt to read or modify these registers, as unpredictable results may occur.

## UDC COMMAND OVERVIEW

The HDC 9224 has 16 high-level commands that provide the user with a high degree of flexibility and control. All of the commands for the UDC can be thought of as falling into one of two basic groups.

The first group handles the "housekeeping" required by the drives and the UDC itself. These commands are:

| | |
|---|---|
| RESET | STEP OUT 1 CYLINDER |
| STEP IN 1 CYLINDER | SET REGISTER POINTER |
| DRIVE SELECT | RESTORE DRIVE |
| DESELECT DRIVES | POLL DRIVES |

The second group comprises the "READ/WRITE" functions required in a magnetic disk subsystem. These commands are:

| | |
|---|---|
| SEEK/READ ID | TAPE BACKUP (READ/ |
| FORMAT TRACK | WRITE) |
| READ TRACK | READ SECTORS LOGICAL |
| READ SECTORS PHYSICAL | |
| WRITE SECTORS LOGICAL | |

An internal status byte, which contains the BAD SECTOR, DELETED DATA and OVER/UNDER RUN bits, along with the current state of the READY, WRITE PROTECT, WRITE FAULT, and USER DEFINED lines, is checked at various times during command execution.

This internal status byte is examined before the execution of all READ/WRITE commands, and is also checked just prior to the completion of all commands (except for RESET, where its values would be meaningless.)

This byte is also checked by the UDC between sector operations during the execution of READ LOGICAL, READ PHYSICAL, WRITE LOGICAL and WRITE PHYSICAL commands.

The UDC makes decisions regarding command termination and interrupt generation based on the contents of this status byte, and the state of the bits in the INTERRUPT/COMMAND TERMINATION register. (Note that "write protect" and "write fault" status may cause command termination only during write and format operations.)

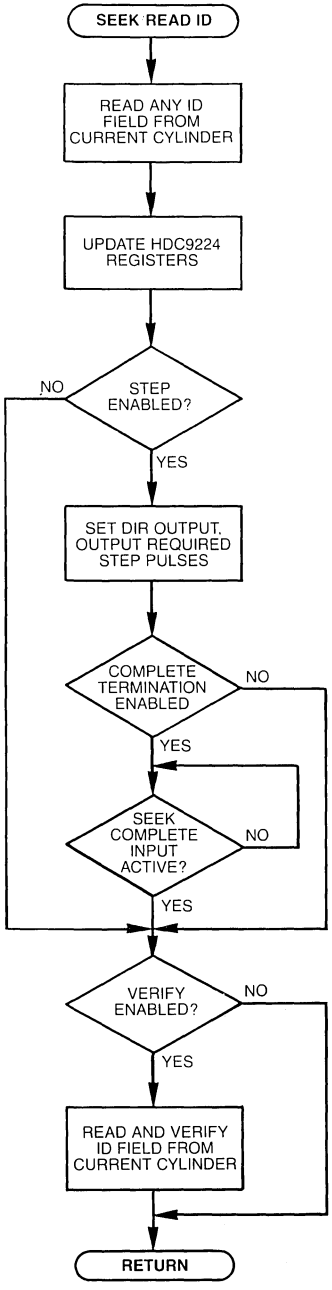
All commands (except RESET) terminate with the DONE bit in the INTERRUPT STATUS register being set. This bit may also be considered to be an inverted "busy" line, as the UDC resets it upon receipt of a valid command.

During all READ/WRITE group commands (except FORMAT TRACK and BACKUP), the UDC utilizes some common command execution sequences. Prior to entering each sequence the UDC sets the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to a known state. If a command fails to execute properly, these bits may then be used to determine where the command aborted.

The sequences common to the READ/WRITE group commands are as follows:

1. READ ID FIELD (Command Termination Code = 0-1)
   First, the UDC attempts to find an ID Field Sync mark. If no sync mark is found within 33,792 byte times (byte time = time to read one byte from the type of drive selected), the SYNC ERROR bit (in the CHIP STATUS register) is set (to "1"), and the command is terminated.

   During this phase, the UDC will raise and drop RDGATE up to 256 times (as it attempts to read each sector on the cylinder).




**SEEK/READ ID OPERATION**

After the ID Field is found, the UDC reads it and updates it CURRENT HEAD and CURRENT CYLINDER registers. This information was written to the disk during formatting.

Next, the UDC checks the CRC of the ID field which was read. If it is incorrect, the UDC sets (to "1") the CRC ERROR status bit (in the CHIP STATUS register) and terminates the command.

If the CRC is correct, the UDC then calculates the direction and number of step pulses required to move the head from the current cylinder to the cylinder specified in the DESIRED HEAD REGISTER. These pulses, and the direction bit are output during the OUTPUT 2 times.

If a command should terminate while in the sequence, the COMMAND TERMINATION bits will be set to 0-1.

2. VERIFY (Command Termination Code = 1-0)

After the UDC has read the ID Field, it attempts to verify that it has found the correct cylinder. To do this, the UDC tries to find an ID Field sync mark on the selected disk. If the UDC is unable to find an ID Field sync mark within 33,792 byte times, the SYNC ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

The UDC, after finding the ID Field sync mark, then reads the ID field and compares the information on the disk to the information contained in the DESIRED CYLINDER, DESIRED HEAD and DESIRED SECTOR registers.

The UDC will hunt for sync marks and read ID fields until the desired sector is found. If the desired sector is not located within 33,792 byte times, then the COMPARE ERROR bit (in the CHIP STATUS register) is set to "1", and the command is terminated.

After the correct sector is found, the UDC checks the CRC for the sector ID Field. If this is found to be incorrect, the UDC sets to "1" the CRC/ECC ERROR bit in the CHIP STATUS register, and the command is terminated.

(When the UDC is executing a READ PHYSICAL or WRITE PHYSICAL command, ID Fields are checked only until the first sector to be transfered is found. No ID Field checking is performed on subsequent sectors, although CRC checking is done.)

If a command should terminate while in this sequence, the COMMAND TERMINATION bits will be set to 1-0.

3. DATA TRANSFER (Command Termination Code = 1-1)

If a READ PHYSICAL or READ LOGICAL command is being executed, the UDC will try to find a data sync mark (FBhex or F8hex) on the disk. If the sync mark found is F8h, then the UDC will set the DELETED DATA MARK bit in the CHIP STATUS register.

After a data sync mark is found, the UDC then updates its CURRENT HEAD and CURRENT CYLINDER registers from the information found on the disk and initiates a DMA request. If the host processor does not respond to the request within 1 byte time, then the UDC will set to "1" the OVER/UNDERRUN status bit in the INTERRUPT STATUS register, and the command will terminate.

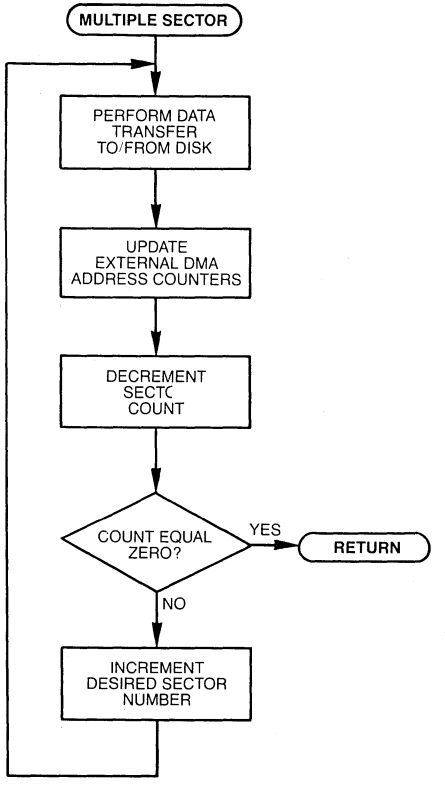
Using DMA, the UDC transfers a sector's worth of data, and then reads the ECC and/or CRC bytes. If a CRC error or uncorrectable ECC error is detected, the UDC will decrement the RETRY REGISTER, set the RETRY REQUIRED status bit (in the CHIP STATUS

register), and return to the VERIFY sequence.

If the UDC cannot read the sector, and the count in the ENTRY COUNT register has expired, then the CRC/ECC Error bit (in the CHIP STATUS register) is set, and the command terminates.

During a multi-sector transfer, the UDC updates the DMA registers after all sector operations, including the last one, and the SECTOR COUNT register is decremented. If the SECTOR COUNT register equals 0, then the command is terminated. If the SECTOR COUNT register is not equal to 0, then the UDC will increment the DESIRED SECTOR register, re-initialize the RETRY COUNT register (to its original value) and return to the VERIFY sequence.

If a command should terminate while in this sequence, the command termination bits will be set to 1-1.




**MULTIPLE SECTOR READ OPERATIONS**

## COMMAND DESCRIPTION

**RESET** **(Hex Value = 00)**

This command causes the UDC to return to a known state. This command allows the system software to reset the chip, and has the same effect as $\overline{RST}$ input becoming active.

**DESELECT DRIVE** **(Hex Value = 01)**

This command causes all of the drive select bits (Drive Select 0-3) in the OUTPUT 1 and OUTPUT 2 registers to become inactive.

**RESTORE DRIVE** **(Hex Values = 02, 03)**

This command will cause the HDC 9224 to output step pulses to the selected drive, so as to move the head back to Track 00. Before each step pulse, the UDC first checks the TRK00 and READY bits in the DRIVE STATUS register. If TRK00 is active (high) or READY is inactive (low), then the UDC will terminate the command.

The UDC will output up to 4096 step pulses. If the drive does not respond with an active (high) TRK00 signal within this period, the UDC will terminate the command with the DONE bit set (to "1") and the COMMAND TERMINATION CODE bits set to 1-0. (These bits are contained in the INTERRUPT STATUS register.)

This command takes two forms:

| COMMAND BYTE | RESULT |
|---|---|
| 02 | The command will terminate, and an interrupt generated after the UDC has issued the step pulses. |
| 03 | The command will terminate, and an interrupt generated after the drive has provided a SEEK COMPLETE signal to the UDC. (This is useful in systems with "buffered seek" drives.) |

This command uses the step rate value loaded into the MODE register.

**STEP IN 1 CYLINDER** **(Hex Values = 04, 05)**

This command will cause the HDC 9224 to issue one step pulse towards the inner most track. This command is generally used during track formatting, and takes two forms:

| COMMAND BYTE | RESULT |
|---|---|
| 04 | The command will terminate, and an interrupt generated after the UDC issues the step pulse. |
| 05 | The command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of SEEK COMPLETE the UDC will generate an interrupt. |

This command uses the step rate value programmed into the MODE register.

**STEP OUT 1 CYLINDER** **(Hex Values = 06, 07)**

This command will cause the HDC 9224 to issue one step pulse towards the outer most track (Track 00). This command is generally used during track formatting, and takes two forms:

| COMMAND BYTE | RESULT |
|---|---|
| 06 | This command will terminate, and an interrupt generated after the UDC issues the step pulse. |
| 07 | This command will not terminate until the UDC recognizes the SEEK COMPLETE signal from the selected drive. Upon recognition of the SEEK COMPLETE, the UDC will generate an interrupt. |

This command uses the step rate value programmed into the MODE Register.

**POLL DRIVES (Hex Values = 10 thru 1F)**

This command polls the drives for a SEEK COMPLETE signal allowing the user to perform simultaneous seeks on up to four drives. Polling is enabled by setting (to 1) the appropriate bit in the command word: bit 0 for drive 0 thru to bit 3 for drive 3.

This command executes as follows:

The UDC will output a drive select for the first drive in the polling sequence and look for a SEEK COMPLETE status input from the polled drive. If the polled drive has not completed a seek, then this line remains low (logic 0), and the UDC selects the next drive in the polling sequence. This continues until the UDC detects a SEEK COMPLETE signal from a drive, which causes the DONE bit in the Interrupt Status register to be set, and the command terminates.

The UDC will continue to select the drive that produced the SEEK COMPLETE signal, allowing the user to read the DRIVE STATUS register to determine which drive caused the command termination.

The POLL DRIVES command must be preceeded by DESELECT.

**DRIVE SELECT (Hex Values = 20 thru 3F)**

This command will cause one of (up to) four drives to be selected for operation. Any previously selected drive is deselected by this command. Bits 0 and 1 in the command word indicate (in binary form) which of the (up to) four drives has been selected.

| COMMAND WORD | | DRIVE SELECTED |
|---|---|---|
| DB1 | DB0 | |
| 0 | 0 | Drive 0 |
| 0 | 1 | Drive 1 |
| 1 | 0 | Drive 2 |
| 1 | 1 | Drive 3 |

Decoded drive select signals are then placed on the data bus (via AB7-AB4) during OUTPUT 1 times and should be latched externally.

Since the HDC 9224 can interface both hard disks and floppy disks to a processor, the Drive Select command needs to also specify the type of drive being selected. Bits 2 and 3 in the command word are used to pass this information to the chip, and take the following form:

| COMMAND WORD | | TYPE OF DRIVE |
|---|---|---|
| DB3 | DB2 | |
| 0 | 0 | Hard disk with ST506 (Seagate) compatible format—256 byte data field and 3 byte ID field per sector. No internal clock prescaling performed. |
| 0 | 1 | Hard disk with user defineable format. This format allows a data field length of 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes with 4 byte ID field per sector. No internal clock pre-scaling is performed. |
| 1 | 0 | 8 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 1 MHz clock to be compatible with standard disk data rates. |
| 1 | 1 | 5.25 inch floppy disk, with standard 4 byte ID field. An internal divider creates a 500 KHz clock to be compatible with standard disk data rates. |

NOTE: Microfloppy system designers should determine whether the drive they have chosen to use in the system is compatible with 8" floppy drives or 5.25" floppy drives, and use the appropriate values from the table above.

Note that eight inch Winchester-type drives require an 8.696 MHz system clock. All other drives require a 10 MHz system clock. It is not possible for the UDC to derive internally the clocks required for floppy disk operation from the 8.696 MHz clock required by 8 inch Winchester drives.

To insure compatibility with various drives, the HDC 9224 features a programmable head load timer. Head load delay may be inhibited by resetting the Delay Bit (Bit 4) in the Drive Select command word to 0. If Bit 4 is set (to 1), then the head load delay timer is configured with the value in the DATA/DELAY register (Register A), multiplied by value shown below:

| DRIVE AND FORMAT SELECTED | HEAD LOAD TIMER INCREMENT (BIT 4 = 1 = Delay Enabled) | |
|---|---|---|
| 5.25" HARD DISK (Double Density) | 200 usec | (The HEAD LOAD TIMER is set to a value equal to this increment times the number in the DATA/DELAY register.) |
| 5.25" HARD DISK (Single Density) | 400 usec | |
| 8" FLOPPY (Double Density) | 2 msec | |
| 8" FLOPPY (Single Density) | 4 msec | |
| 5.25" FLOPPY (Double Density) | 4 msec | |
| 5.25" FLOPPY (Single Density | 8 msec | |

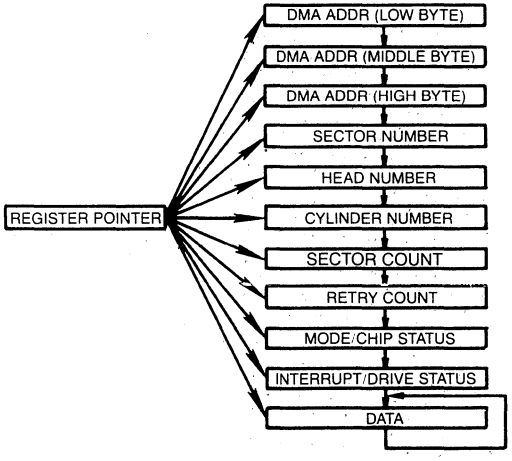
The Drive Select command also optimizes certain characteristics of the HDC 9224 for the type of drive selected.

IF HARD DISK SELECTED:

–DMA mechanism works in burst mode and the bus is held for the entire sector transfer.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.




**SET REGISTER POINTER COMMAND**

SECTION VI

IF FLOPPY DISK SELECTED:

–DMA mechanism transfers an 8-bit byte, and releases the bus.

–The RDGATE and WRGATE output signals follow the timing relationships shown in Figures 12A and 12B.

–The GAP lengths are as shown in Table 1.

–The CLK input clock is prescaled (internally) to create an internal clock compatible with the floppy disk data rates.

**SET REGISTER POINTER (Hex Values = 40 to 4A)**
This command causes the register pointer to point to a register. The desired register number is loaded into the 4 least significant bits of the command word. (MSB in BIT 3).

The register pointer is incremented by the UDC on each register access, until it points to the DATA register. This reduces the number of times the user must set the register pointer during read and write operation.

Care should be taken to ensure that only valid register values are loaded into the command word. (Valid register numbers are 0 thru OAH.)

**SEEK/READ ID (Hex Values = 50 to 57)**
This command will cause the UDC to read the first sector ID field found from the currently selected drive, head, and cylinder. The MODE register should contain the correct value for step rate and density options.

After reading the ID field the UDC will examine the command word and execute the specified options. Bits 2 thru 0 in the command word are used to specify the following options:

BIT 2 = 1 STEP ENABLE. The UDC will execute the step sequence, and position the head on the track specified by the DESIRED CYLINDER register.

BIT 2 = 0 STEP DISABLE. No step pulses will be issued by the UDC.

BIT 1 = 1 WAIT FOR COMPLETE. The UDC will proceed to the verify sequence only after the drive has issued a SEEK COMPLETE signal.

BIT 1 = 0 DO NOT WAIT FOR COMPLETE. The UDC will proceed to the verify sequence after the last step pulse has been issued.

BIT 0 = 1 VERIFY ID. The UDC will execute the VERIFY sequence after operations selected by the previous options have finished.

BIT 0 = 0 DISABLE VERIFY ID. The UDC will not enter the VERIFY sequence. Instead, the command will terminate.

The order in which these options execute is: STEP, COMPLETE, VERIFY ID. Any combination of these option bits may be specified in the command word.

**READ SECTORS PHYSICAL (Hex Values = 58 and 59)**
This command will cause the UDC to read up to a full track from the disk. The user specifies the MODE, DESIRED CYLINDER, DESIRED HEAD, and DESIRED SECTOR along with the SECTOR COUNT. The UDC will find the requested cylinder and sector and set up to begin the data transfer.

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

If a BAD SECTOR bit is read (from the sector ID field) the UDC will set the COMMAND TERMINATION bits (in the INTERRUPT STATUS register) to 1-0, and set the DONE bit (in the INTERRUPT STATUS register) to 1, and terminate the command.

After each sector is successfully read, the SECTOR COUNT register is decremented. If the SECTOR COUNT register is not yet equal to 0 the process is repeated for the next physical sector on the track. This command also will terminate if the Index pulse is received from the drive.

(Note that after the first sector is found, no further comparison is made against sector numbers found on the disk as the DESIRED SECTOR register value may not correspond to the next physical sector on the disk because of sector interleaving.)

This command takes two forms allowing the user to specify the desired transfer option. The options are specified by Bit 0 in the command word, and are:

BIT 0 = 1 TRANSFER ENABLE. The UDC will transfer the data fields to (external) memory, using DMA.

BIT 0 = 0 TRANSFER DISABLE. The UDC will NOT transfer any data to (external) memory, but all error detection circuitry will be enabled and errors reported. This is useful in detecting bad sectors and tracks on the disk.

Before executing this command, the user must set the RETRY COUNT to 0. This is done by loading the high order nybble in the RETRY COUNT register to "1111" (zero in 1's complement format). Failure to do this will result in unpredictable performance because the DESIRED SECTOR register value may not correspond to the next physical sector on the disk.

**READ TRACK (Hex Values = 5A and 5B)**
When this command is issued, the UDC will read the data from the entire track on which the selected drive is currently sitting. The UDC will begin reading when it detects the leading edge of an index mark signal from the drive, and terminate reading when it detects the next leading edge of an index mark signal. Sync detect is performed for the ID field, but no error checking is done on the data field.

This command allows the user to specify a data transfer option, using Bit 0 in the command word. These options are:

BIT 0 = 1 TRANSFER ALL DATA. The UDC will transfer the ID field and data fields to (external) memory.

BIT 0 = 0 TRANSFER ONLY IDs. The UDC will transfer only ID fields to the (external) memory. This is useful during tape backup operations.

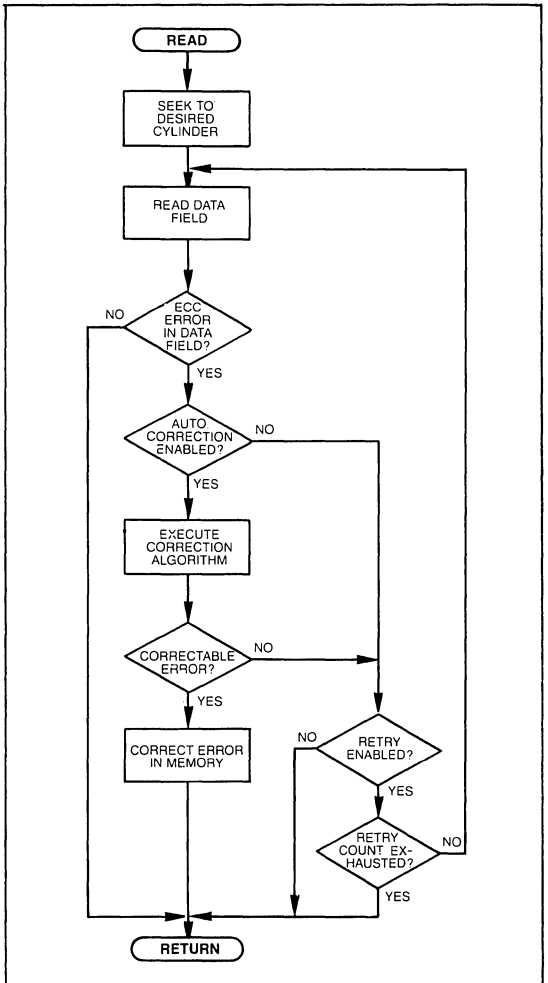
**READ SECTORS LOGICAL (Hex Values = 5C to 5F)**
When this command is issued, the UDC will read up to a full track from the selected drive. Prior to reading the data from the disk, the UDC will use the information in the MODE, DESIRED CYLINDER, DESIRED SECTOR and DESIRED HEAD registers to locate the correct track, sector and drive surface (using the previously described VERIFY sequence).

(If using drives which support buffered seeks, BITS 2-0 in the MODE SELECT register should be set to 0-0-0. This will cause the UDC to wait for a SEEK COMPLETE signal from the drive prior to entering the verify sequence.)

Before the command is issued, the system processor must also load the desired values into the MODE, SECTOR COUNT, RETRY COUNT and the three DMA registers.

When reading multiple sectors, the read command must be configured with ECC correction disabled. If a hard error is detected, the sector count must be set to one, retry count to zero, and ECC correction enabled. The sector can then be read and corrected. After the error has been corrected, ECC correction can be disabled, retry can be re-enabled, and the remainder of the data can be read.

After the desired track and sector is found and verified, the DATA TRANSFER sequence begins. After each successful sector transfer, the UDC increments the DESIRED SECTOR register (except after the last sector is transferred), decrements the SECTOR COUNT register, and re-enters the VERIFY sequence. This process continues until




**READ SECTORS OPERATION**

the SECTOR COUNT register is equal to 0 (or an error occurs).

This command has four options, which are specified by Bit 1 and Bit 0 of the command word. The four options are:

BIT 1 = 1 BAD SECTOR BYPASS. If, during the read, the UDC finds a sector with the BAD SECTOR bit set (from the sector ID field on the disk), the sector be skipped, the sector count will not be decremented, and the sector number will not be changed.

BIT 1 = 0 BAD SECTOR TERMINATE. If, during a read, the UDC finds a sector with the BAD SECTOR bit set, the UDC will set the COMMAND TERMINATION CODE to 1-0, set the BAD SECTOR status bit and the DONE status bit, and terminate the command (with an interrupt, if enabled). All of the above named status bits are contained in the INTERRUPT STATUS register.

BIT 0 = 1 TRANSFER ENABLED. The UDC will transfer data from the disk to the system. The DMA REQUEST status bit (in the INTERRUPT STATUS register) will be set when the UDC requires servicing.

BIT 0 = 0 TRANSFER DISABLED. The UDC will not transfer data read from the disk, but all error checking circuitry will be enabled.

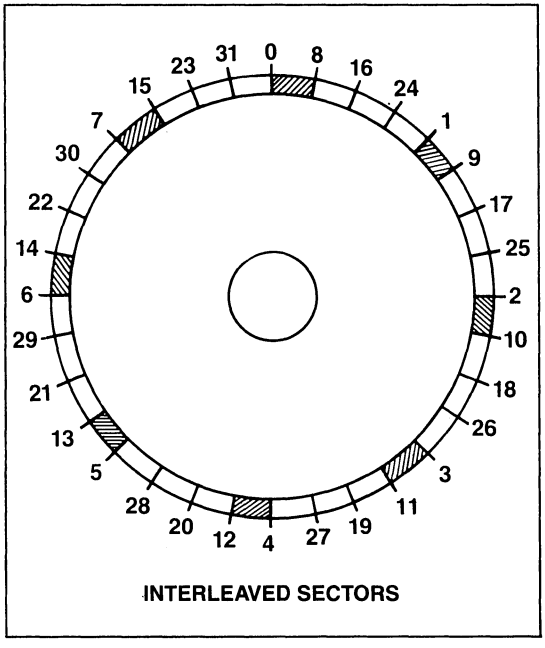
**FORMAT TRACK (Hex Values 60 to 7F)**

This command causes the UDC to format the current cylinder from the leading edge of one index mark to the leading edge of the next index mark. The format chosen is dependent on the Drive Select command.

During execution of the FORMAT TRACK command, the UDC will fetch all required ID field data from external memory, and write it to the disk, along with format constants supplied automatically by the UDC. This reduces the number of bytes required to format a sector to 3 or 4, depending on the format chosen.

Before the FORMAT TRACK command can be given, the system processor must:

1. Generate an ID Field table for the track in UDC memory area. This ID Field Table consists of:
   CYLINDER BYTE
   HEAD BYTE
   SECTOR NUMBER BYTE
   SECTOR SIZE/ECC SIZE BYTE (not required for ST-506 formats) repeated for each sector on the track.




**INTERLEAVED SECTORS**

The UDC can format a track with interleaved sectors by staggering the sector numbers. For example, to format a 32 sector track, with a sector interleave factor of 4, the system processor would set up the ID Field table sector numbers as follows:
0,8,16,24,1,9,17,25,2,10,18,26,3,11,19,
27...7,15,23,31.

(Note that when formatting in ST506 mode, only three bytes are required for each sector, while four bytes are needed for IBM or user defineable formats. Also note that sector numbers start with zero (0) on ST506 compatible format, and start with one (1) on IBM formatted floppy diskettes.)

2. Load the UDC DMA registers with the starting address of the external memory buffer containing the ID Field data just created.

3. Issue the DRIVE SELECT command, which moves the DMA registers to the CURRENT HEAD, CURRENT CYLINDER, and a TEMPORARY REGISTER. (This is necessary because the UDC will now re-use the DMA registers to hold format parameters).

   When formatting multiple cylinders, the system processor does not need to re-issue DRIVE SELECT between cylinders as the STEP IN and STEP OUT commands preserve the DMA addresses and format parameters. It is necessary, however, to update the ID Field table, described in #1, above.

4. Load the DESIRED HEAD register with the proper value.
5. Load the following values (in the format shown) into the registers indicated below:

| PARAMETER | FORMAT | REGISTER |
|---|---|---|
| GAP 0 Size | two's complement format | DMA 7-0 |
| GAP 1 Size | two's complement format | DMA 15-8 |
| GAP 2 Size | two's complement format | DMA 23-16 |
| GAP 3 Size | two's complement format | Desired Sector |
| Sync Size | one's complement format | Desired Cylinder |
| Sector Count | one's complement format | Sector Count |
| Sector Size Mult. | one's complement format | Retry Count |

**FORMAT PARAMETERS TABLE**

When using ST506/PC (fixed length) hard disk format, the values for GAP 0 and GAP 1 must both be set to the same number, and loaded into the appropriate DMA register.

The Sector Size Multiple programs the UDC to format with a sector size that is a multiple of 128 data field bytes. For example, to format a track with a sector data field size of 512 bytes, then the Sector Size Multiple would be set to FD hex, which is "2" in one's complement notation.

In ST506/PC format, the sector size is fixed at 512 bytes. In IBM floppy disk format, the sector sizes allowed are 128, 256, 512, or 1024 bytes. With user defineable hard disk formats, allowed sector sizes are 128, 256, 512, 1024, 2048, 4096, 8192, or 16384 bytes.

6. Load the MODE register to specify the step rate, single or double density option, and CRC/ECC options.
7. Step to the desired track. For the first track, this is normally done by issuing a RESTORE DRIVE command, to return the heads to Cylinder 000, then use the STEP IN 1 or STEP OUT 1 commands to move the head to subsequent cylinders on the disk.
8. Issue the FORMAT TRACK command. All data fields on the disk will be filled with E5 hex. In double density recording (MFM) all gaps will be filled with 4E hex, while in single density (FM) all gaps will be filled with FF hex. This format is compatible for IBM specifications for floppy disks.
9. To Format additional tracks, it is only necessary to update the ID Field table (step 1) and repeat steps 7 and 8. Do NOT modify the DESIRED HEAD register when formatting additional tracks with the same head. If it is necessary to change the DESIRED HEAD register, the system processor must repeat all steps described above.

   The FORMAT TRACK command allows the user to specify several options. These options are specified by setting the appropriate low order bits in the command word. The bit mapping for these options are:

BIT 4 = 1 Write Deleted Data Mark. During the format process, the UDC will write the deleted data mark (F8 hex) for the data address field.

BIT 4 = 0 Write Normal Data Mark. During the format process, the UDC will write the normal data field address mark (FB hex).

BIT 3 = 1 Write with Reduced Current. When this bit is set, the Reduced Write Current Output will go high (active) during the Output 2 time slot.

BIT 3 = 0 Write with Normal Current. When this bit is reset, the Reduced Write Current Output wil remain low (inactive) during the Output 2 time slot.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during the format of disks. The following table specifies these values:

SECTOR SIZE FIELD BITS

| DB2 | DB1 | DB0 | IBM FD FORMAT | HD FORMAT |
|---|---|---|---|---|
| 0 | 0 | 0 | 128 bytes/sector | 128 bytes/sector |
| 0 | 0 | 1 | 256 bytes/sector | 256 bytes/sector |
| 0 | 1 | 0 | 512 bytes/sector | 512 bytes/sector |
| 0 | 1 | 1 | 1024 bytes/sector | 1024 bytes/sector |
| 1 | 0 | 0 | not used | 2048 bytes/sector |
| 1 | 0 | 1 | not used | 4096 bytes/sector |
| 1 | 1 | 0 | not used | 8192 bytes/sector |
| 1 | 1 | 1 | not used | 16,384 bytes/sector |

FORMAT ECC TYPE FIELD

| DB7 | DB6 | DB5 | DB4 | HD FORMAT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 4 ECC bytes generated/checked |
| 1 | 1 | 1 | 1 | 5 ECC bytes generated/checked (1) |
| 1 | 1 | 1 | 0 | 6 ECC bytes generated/checked (1) |
| 1 | 1 | 0 | 1 | 7 ECC bytes generated/checked (1) |

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | track number | | | | | | | |
| HEAD | side number | | | | | | | |
| SECTOR | sector number | | | | | | | |
| SECTOR SIZE | | | | | | | sector size (2 bits) | |

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | cylinder number (8 LSB's) | | | | | | | |
| HEAD | bad sector flag | cyl # bit 10 | cyl # bit 9 | cyl # bit 8 | hd # bit 3 | hd # bit 2 | hd # bit 1 | hd # bit 0 |
| SECTOR | sector number | | | | | | | |

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | cylinder number (8 LSB's) | | | | | | | |
| HEAD | bad sector flag | cyl # bit 10 | cyl # bit 9 | cyl # bit 8 | hd # bit 3 | hd # bit 2 | hd # bit 1 | hd # bit 0 |
| SECTOR | sector number | | | | | | | |
| SECTOR SIZE | ECC type | | | | X | | sector size (3 bits) | |

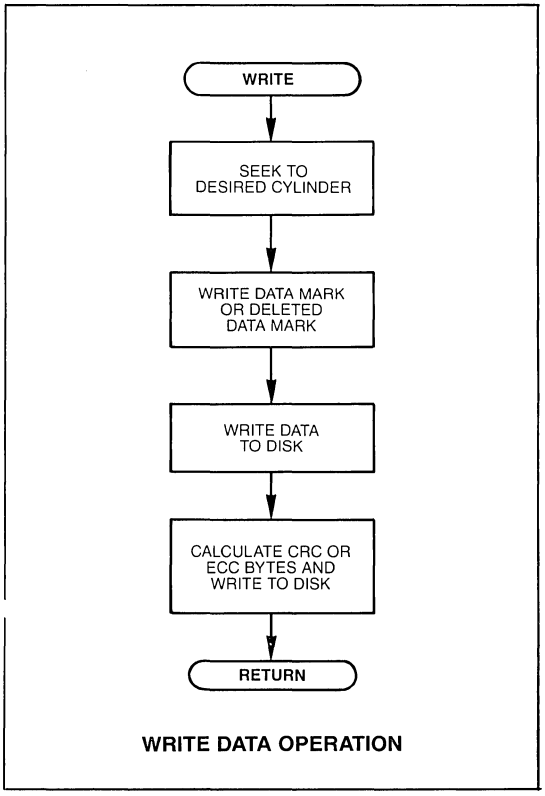
| BIT 2 | BIT 1 | BIT 0 | Precompensation (For Floppy Disks) |
|---|---|---|---|
| 0 | 1 | 0 | None, enable EARLY and LATE Outputs |
| 1 | 0 | 1 | 600 nsec, Minifloppy only |
| 0 | 1 | 1 | 500 nsec, Minifloppy only |
| 1 | 1 | 1 | 400 nsec, Minifloppy only |
| 1 | 1 | 0 | 300 nsec |
| 1 | 0 | 0 | 200 nsec |
| 0 | 0 | 1 | 100 nsec |
| 0 | 0 | 0 | None, suppress EARLY and LATE Outputs |

**WRITE SECTORS LOGICAL (Hex Values A0 thru BF, E0 thru FF)**

This command will cause the UDC to write logically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

| | |
|---|---|
| DESIRED SECTOR | DESIRED CYLINDER |
| DESIRED HEAD | SECTOR COUNT |
| DMA 7-0 | DMA 15-8 |
| DMA 23-16 | MODE |
| RETRY COUNT | |

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).




**WRITE DATA OPERATION**

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register.

Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next logical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flag set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 1 WRITE LOGICAL COMMAND BIT (Always set to "1" for Write logical command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to disks. The table below specifies these values.

| BIT 2 | BIT 1 | BIT 0 | Precompensation (For Floppy Disks) |
|---|---|---|---|
| 0 | 1 | 0 | None, enable EARLY and LATE Outputs |
| 1 | 0 | 1 | 600 nsec, Minifloppy only |
| 0 | 1 | 1 | 500 nsec, Minifloppy only |
| 1 | 1 | 1 | 400 nsec, Minifloppy only |
| 1 | 1 | 0 | 300 nsec |
| 1 | 0 | 0 | 200 nsec |
| 0 | 0 | 1 | 100 nsec |
| 0 | 0 | 0 | None, suppress EARLY and LATE Outputs |

NOTE: For hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

**WRITE SECTORS PHYSICAL (Hex Values 80 thru 9F, C0 thru DF)**

This command will cause the UDC to write physically consecutive sectors on the disk. Before issuing this command, the system processor must load the following UDC registers:

| | |
|---|---|
| DESIRED SECTOR | DESIRED CYLINDER |
| DESIRED HEAD | SECTOR COUNT |
| DMA 7-0 | DMA 15-8 |
| DMA 23-16 | MODE |
| RETRY COUNT | |

Since retries during a write command are not valid, the high order nybble of the RETRY register should be set to 0, in 1's complement format (1111).

Before writing data to the selected disk drive, the UDC will read the current ID field, step to the desired cylinder and

verify that it has located the correct cylinder and sector. (These steps were described previously under "UDC Command Overview").

After the "Verify" sequence is done, the "data transfer" sequence begins. The UDC will first write either a Data Mark (FB hex) or Deleted Data Mark (F8 hex) on the disk, as selected by the user (see below). Then the UDC will transfer a sector's worth of data (using DMA) from the memory area specified by the DMA registers. After writing out the sector, CRC or ECC bytes will be written as specified by the MODE register. Next, the SECTOR COUNT register is decremented, and if not yet equal to 0, the operation continues for the next physical sector.

This command allows the user to specify several options. These options are specified by bits in the command word and are as follows:

BIT 6 = 1 BAD SECTOR BYPASS. The UDC will bypass the sectors with the BAD SECTOR FLAG set in the ID field.

BIT 6 = 0 BAD SECTOR TERMINATION. The UDC will terminate the command when it locates a sector with the BAD SECTOR FLAG flat set in the ID field. In addition, the COMMAND TERMINATION CODE Status bits will be set to 1-0, the BAD SECTOR status bit will be set, the DONE status bit will be set, and if not masked, an interrupt will be generated.

BIT 5 = 0 WRITE PHYSICAL COMMAND BIT (Reset to "0" for Write Physical Command).

BIT 4 = 1 DELETED DATA MARK. Data will be written with a Deleted Data Mark (F8 hex) in the ID field.

BIT 4 = 0 NORMAL DATA MARK. Data will be written with a Normal Data Mark (FB hex) in the ID field.

BIT 3 = 1 REDUCED WRITE CURRENT. Setting this bit will cause the UDC's Reduced Write Current output to go high.

BIT 3 = 0 NORMAL WRITE CURRENT. Resetting this bit will cause the UDC's Reduced Write Current output to go low.

Bits 2, 1, and 0 are used to select the Write Precompensation value to be used during writes to floppy disks. The table below specifies these values.

| BIT 2 | BIT 1 | BIT 0 | Precompensation (For Floppy Disks) |
|---|---|---|---|
| 0 | 1 | 0 | None, enable EARLY and LATE Outputs |
| 1 | 0 | 1 | 600 nsec, Minifloppy only |
| 0 | 1 | 1 | 500 nsec, Minifloppy only |
| 1 | 1 | 1 | 400 nsec, Minifloppy only |
| 1 | 1 | 0 | 300 nsec |
| 1 | 0 | 0 | 200 nsec |
| 0 | 0 | 1 | 100 nsec |
| 0 | 0 | 0 | None, suppress EARLY and LATE Outputs |

NOTE: for hard disks, precompensation is handled with an external delay line, which is connected to the EARLY and LATE Outputs of the UDC. These lines toggle in response to the data pattern being written to the disk.

**TAPE BACK-UP (Hex Values = 08 to 0F)**

The TAPE BACK-UP command set provides the system with the capability of transferring data to and from a tape drive in continuous blocks. TAPE BACK-UP utilizes the UDC's DMA, data conversion, error detection/correction and sector count circuitry.

Because of the mechanical and electronic differences between tape drives and disk drives, some of the register bits described earlier in this data sheet change functions when the UDC is executing the TAPE BACKUP COMMAND. In many cases, the CLK input to the UDC will also need to be changed to compensate for the slower data rate from tape drives.

**TAPE BACKUP REGISTER DESCRIPTION**

The following bits in the UDC's register file assume the functions listed below when executing the BACK-UP command and should be programmed accordingly.

The following tables describe the differences in register usage when the UDC is executing the TAPE BACKUP command. (Complete TAPE BACKUP register bit maps are located in rear of the data sheet.)

MODE REGISTER

Bit 2 = 1 16 byte sync detect delay enable
= 0 16 byte sync detect delay disabled

Bit 1 = 1 TAPE BACKUP Write Enable (writing)
= 0 TAPE BACKUP Write Disable (reading)

Bit 0 = 1 Tape mark enable (short block)
= 0 Tape mark disable (long block)

RETRY COUNT REGISTER

Bits 7-4 Retry should be disabled, by setting these bits to "1". (Retry Disabled)

Bits 3-0 program outputs (user controlled). Bit 3 is typically used for write enable to the tape drive.

Bits 0 and 1 are typically used for tape driven motion control as per drive manufacturer's specification.

DESIRED CYLINDER

Bits 7-4 ECC Type Field:

| DB7 | DB6 | DB5 | DB4 | ECC TYPE |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 4 ECC bytes generated/ checked |
| 1 | 1 | 1 | 1 | 5 ECC bytes generated/ checked |
| 1 | 1 | 1 | 0 | 6 ECC bytes generated/ checked |
| 1 | 1 | 0 | 1 | 7 ECC bytes generated/ checked |

note: 5, 6, 7 byte ECCs are generated and checked by hardware external to the UDC.

DESIRED CYLINDER

Bit 3 Always 1

Bits 2-0 Data Block Size:

| DB2 | DB1 | DBO | DATA BLOCK SIZE |
|---|---|---|---|
| 0 | 0 | 0 | 128 bytes |
| 0 | 0 | 1 | 256 bytes |
| 0 | 1 | 0 | 512 bytes |
| 0 | 1 | 1 | 1024 bytes |
| 1 | 0 | 0 | 2048 bytes |
| 1 | 0 | 1 | 4096 bytes |
| 1 | 1 | 0 | 8192 bytes |
| 1 | 1 | 1 | 16,384 bytes |

Remember that the UDC internal ECC code can correct up to a 4K byte long Data Block, but that the larger the Data Block the greater the probability of a miscorrection.

Also, when executing the TAPE BACKUP command, the DRIVE SELECT command is altered slightly, as illustrated below:

| DRIVE SELECT COMMAND | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Drive Select | 0 | 0 | 1 | Ramp Up/Down delay enable | 1 | CLK divisor | 1 | 1 |

| DB2 | CLOCK DIVISOR FOR TAPE |
|---|---|
| 0 | CLK is divided by 10 (similar to 8" floppy divisor). |
| 1 | CLK is divided by 20 (similar to 5.25" floppy divisor). |

These bits, in conjunction with Bits 4 and 7 of the MODE register, will allow selection of both FM and MFM recording on tape, with a tape format that resembles IBM compatible floppy disk formats.

Setting the Drive Type bits to 1,0 or 1,1 will also cause the UDC to take on the following characteristics:

- –DMA mechanism transfers a byte (8 bits) and relinquishes the bus.
- –The RDGATE and WRGATE output signals have timing characteristics as shown in Figures 12A and 12B of the UDC spec.
- –The gap lengths are as illustrated in Table 1 or the UDC spec.
- –Tape format parameters will be as per Table 1 of the UDC spec.

## COMMAND EXECUTION OVERVIEW

The tape backup command allows the user a convenient method of backing up either floppy or hard disks to tape. The UDC may be interfaced to either cartridge or cassette type tape drives, working in either streaming or start/stop mode.

Read and Write functions of TAPE BACKUP share a common command byte. The three LSB's of the MODE register are also used by the TAPE BACKUP command to specify user options, and to select between tape read or tape write mode.

Two kinds of blocks may be specified when reading or writing dependent on the state of the TAPE MARK ENABLE bit in the MODE register:

1. DATA BLOCK. The length of the data block (also called a long block) is equal to:

   $2^n$* 128 bytes where n is an integer between 0 and 7 inclusive. The desired length of the data block ($2^n$) is programmed into the desired cylinder register.

2. TAPE MARK. The minimum length of the tape mark (also called a short block) is 3 bytes. The maximum length of the tape mark is 257 bytes. The desired length is programmed into the sector count register.

Multiple data block transfers are accomplished by programming the 1's complement of the desired number of data blocks to be transferred into the sector count register.

The three LSB's of the MODE register function as part of the BACK-UP command word. The WRITE ENABLE bit determines whether loading the BACK-UP command into the UDC will initiate execution of a BACK-UP READ or BACK-UP WRITE sequence. The TAPE MARK ENABLE bit determines whether the UDC will write a short or long block of data on the tape and the DELAY ENABLE bit determines whether or not the RDGATE signal is stretched when it coincides with a sync mark when reading the tape. The remaining bits in the command word are as follows:

| COMMAND | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| BACK-UP (READING) | 0 | 0 | 0 | 0 | 1 | 0 | 0 | xfer enable |
| BACK-UP (WRITING) | 0 | 0 | 0 | 0 | 1 | precomp value | | |

## BACK-UP READ

When reading a short block, only CRC is checked. When reading a long block, CRC or ECC will be checked, depending on the CRC/ECC bits in the Mode register.

Bit 0 = 1 Data transfer enabled, error checking enabled
= 0 Data transfer disabled, error checking enabled

## BACK-UP WRITE

When writing, the precompensation value is derived from the CLK frequency as follows:

| Bit 2 | Bit 1 | Bit 0 | Precompensation |
|---|---|---|---|
| 0 | 1 | 0 | None, enable EARLY and LATE |
| 1 | 0 | 1 | 6 CLK cycle periods |
| 0 | 1 | 1 | 5 CLK cycle periods |
| 1 | 1 | 1 | 4 CLK cycle periods |
| 1 | 1 | 0 | 3 CLK cycle periods |
| 1 | 0 | 0 | 2 CLK cycle periods |
| 0 | 0 | 1 | 1 CLK cycle period |
| 0 | 0 | 0 | None, suppress EARLY and LATE |

PRECOMPENSATION SELECT FOR BACK-UP COMMAND

## TAPE BACKUP SYSTEM CONFIGURATION NOTES

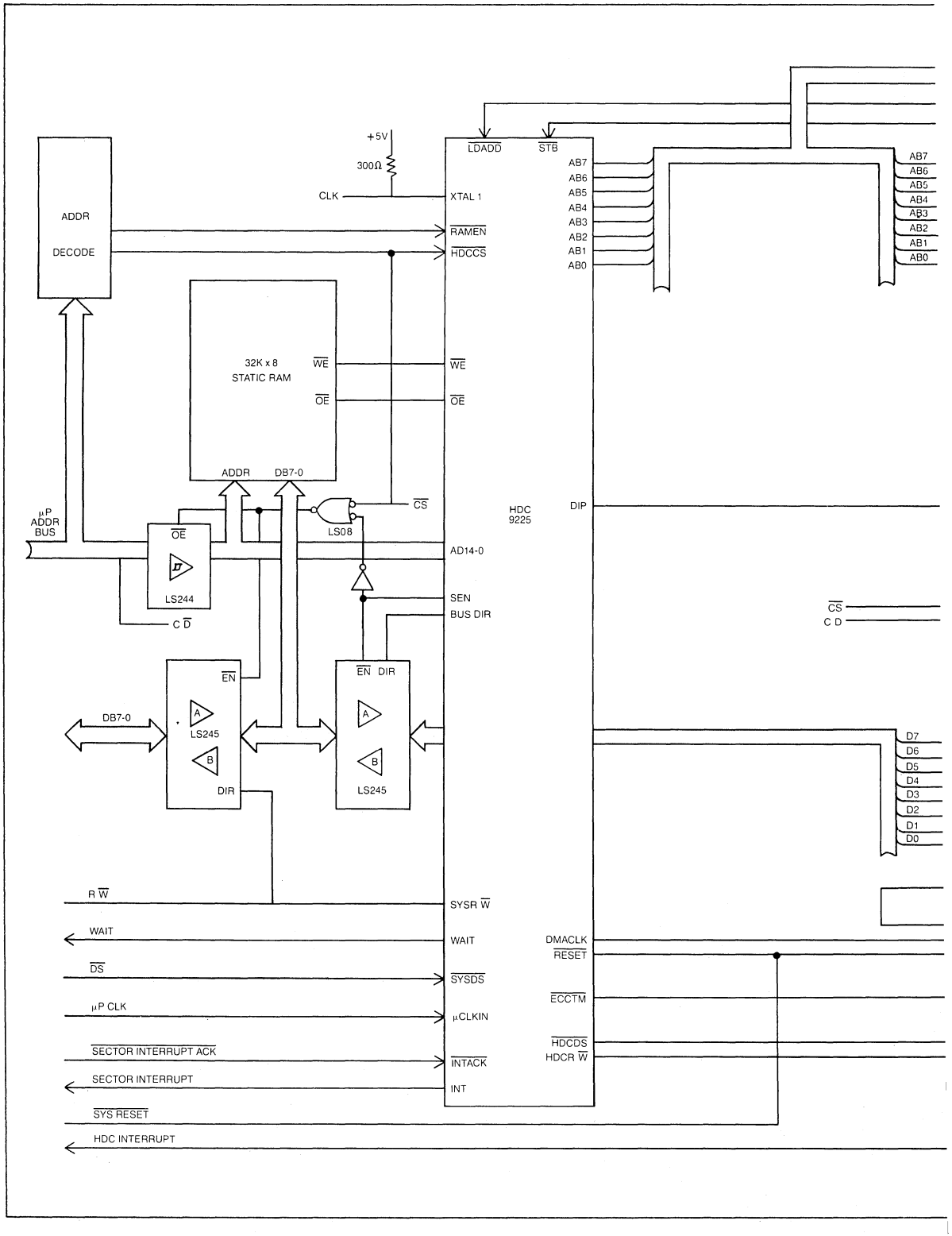
(A schematic showing a typical system implementation using the TAPE BACKUP feature is contained in Schematic Diagram 2.)

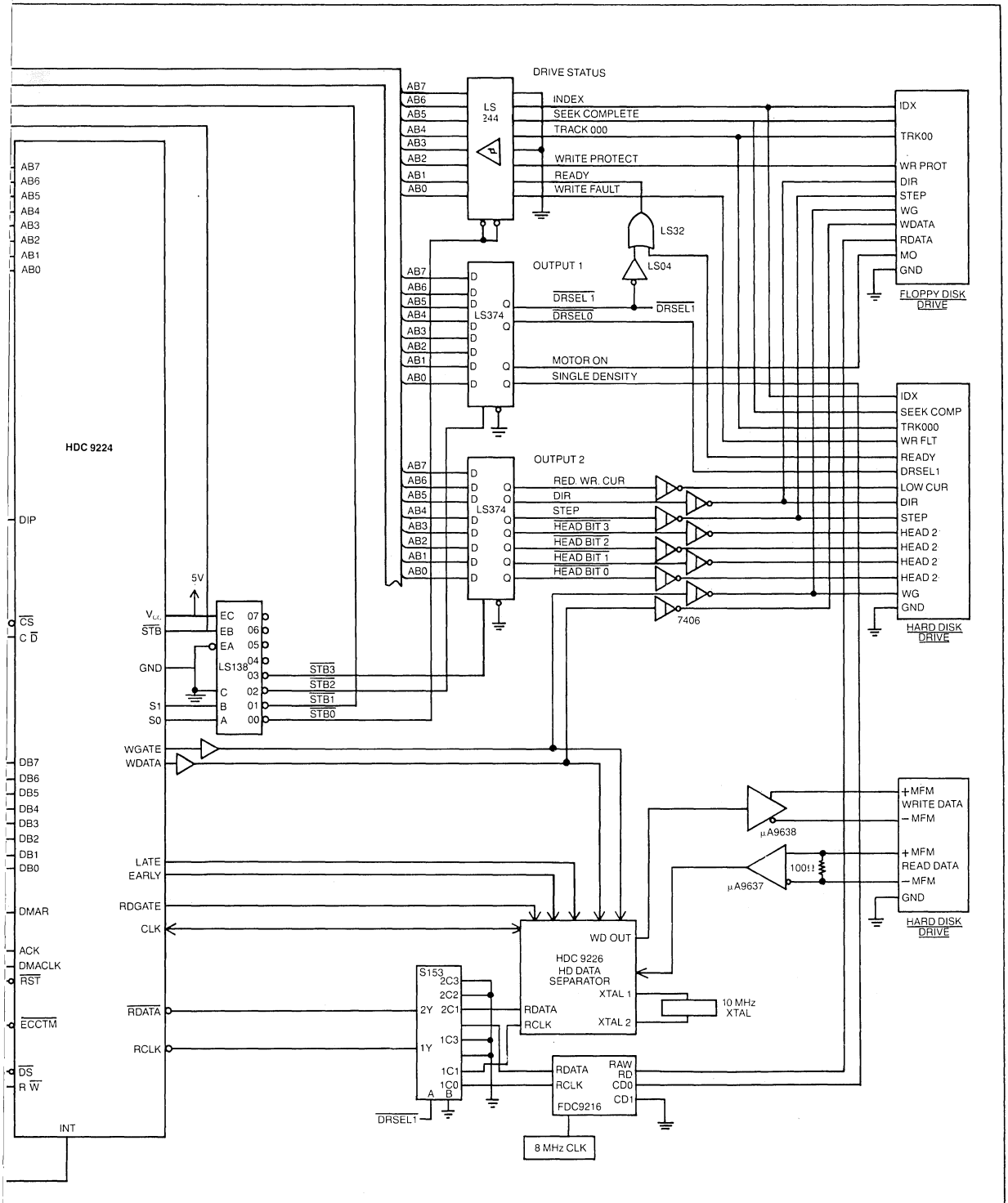
1. Proper operation of the TAPE BACKUP command requires that the tape drive be addressed as DRIVE #3 by the UDC.
2. During the UDC's OUTPUT 2 period external circuitry must enable a separate latch to receive the user defined IO bits and tape track number bits. This latch should use the DRIVE SELECT 3 signal (output during the OUTPUT 2 period) so that the contents of the latch may only be changed when the tape drive is selected.

   Four additional drive control signals may be loaded into the four LSB's of the RETRY COUNT register. These additional outputs are latched externally during OUTPUT 1 times for use by the tape drive. These outputs would normally be used to control tape drive Write Enable logic (bit 3) and tape motion (bits 0 and 1), and tape motor on and off (bit 2).

3. It is important to consider the time required for a tape drive to come up to operating speed when using the TAPE BACKUP command. Also, to insure adequate spacing between tape blocks, a delay is frequently required before stopping tape motion. The UDC has a programmable Ramp Up and Ramp Down timer to allow for easier implementation. The desired delay is programmed into the DATA/DELAY register before issuing the DRIVE SELECT "3" command.

| CLOCK DIVISOR BIT | DENSITY BIT MODE REGISTER BIT 4 | TIME IN SECONDS PER DELAY REGISTER COUNT |
|---|---|---|
| 1 | 1 (Single) | 1 CLK Cycle * 80000 |
| 1 | 0 (Double) | 1 CLK Cycle * 40000 |
| 0 | 1 (Single) | 1 CLK Cycle * 40000 |
| 0 | 0 (Double) | 1 CLK Cycle * 20000 |


+5V
300Ω
CLK
XTAL 1
LDADD
STB
ADDR
DECODE
RAMEN
HDCCS
AB7
AB6
AB5
AB4
AB3
AB2
AB1
AB0
32K x 8
STATIC RAM
WE
OE
ADDR
DB7-0
CS
HDC
9225
DIP
μP
ADDR
BUS
LS08
AD14-0
LS244
C D
SEN
BUS DIR
EN
DIR
DB7-0
A
B
LS245
D7
D6
D5
D4
D3
D2
D1
D0
R W
SYSR W
WAIT
DMACLK
RESET
DS
SYSDS
ECCTM
μP CLK
μCLKIN
HDCDS
HDCR W
SECTOR INTERRUPT ACK
INTACK
SECTOR INTERRUPT
INT
SYS RESET
HDC INTERRUPT


HDC 9224
DRIVE STATUS
LS 244
INDEX
SEEK COMPLETE
TRACK 000
WRITE PROTECT
READY
WRITE FAULT
LS32
LS04
OUTPUT 1
LS374
DRSEL 1
DRSEL0
MOTOR ON
SINGLE DENSITY
OUTPUT 2
RED. WR. CUR
DIR
STEP
HEAD BIT 3
HEAD BIT 2
HEAD BIT 1
HEAD BIT 0
7406
5V
LS138
STB3
STB2
STB1
STB0
WGATE
WDATA
LATE
EARLY
RDGATE
CLK
RDATA
RCLK
ACK
DMACLK
RST
ECCTM
DS
R W
INT
DIP
CS
C D
DMAR
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
S153
2C3
2C2
2C1
1C3
1C1
1C0
2Y
1Y
A
B
DRSEL1
WD OUT
HDC 9226
HD DATA
SEPARATOR
XTAL 1
XTAL 2
10 MHz
XTAL
RDATA
RCLK
RAW RD
CD0
CD1
FDC9216
8 MHz CLK
µA9638
µA9637
100Ω
+MFM WRITE DATA
−MFM
+MFM READ DATA
−MFM
GND
HARD DISK DRIVE
IDX
TRK00
WR PROT
DIR
STEP
WG
WDATA
RDATA
MO
GND
FLOPPY DISK DRIVE
IDX
SEEK COMP
TRK000
WR FLT
READY
DRSEL1
LOW CUR
DIR
STEP
HEAD 2
HEAD 2
HEAD 2
HEAD 2
WG
GND
HARD DISK DRIVE

The UDC will issue a normal interrupt (with the command termination code set to 0-0) when the RAMP UP or RAMP DOWN timer has expired.

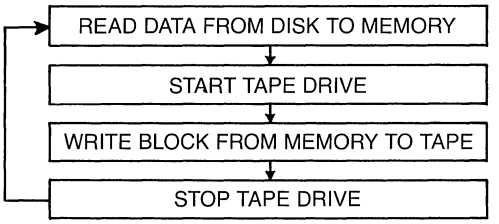
4. BACK-UP WRITE. The user will first request the UDC to perform a disk READ TRACK command, with the TRANSFER ENABLE bit in the command word reset. This will cause the UDC to transfer only the ID field information to memory.

   The TAPE BACKUP command will then be issued causing the UDC to write this ID information to the tape as a tape mark (typically 96 bytes for a drive formatted with a 3 byte/sector ID field or 128 bytes for a drive formatted with a four byte/sector ID field. The data fields should then be transferred to the tape in a similar manner.

   The UDC may be used with either "Streaming" or "Start/Stop" type tape drives. This is illustrated by the following examples:

   A. START/STOP TAPE DRIVE:

   typically transfers ½ or 1 disk track at a time as illustrated by the following flow chart:



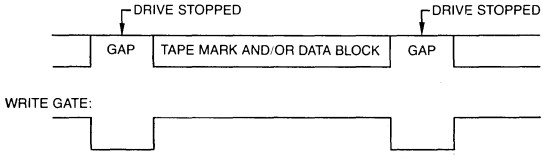

   When controlling a start/stop tape drive, the UDC will write the data "block by block". The system will issue a Drive Select command to the UDC with the Tape Motion, Motor On and Write Enable bits set to start and write data to the tape.

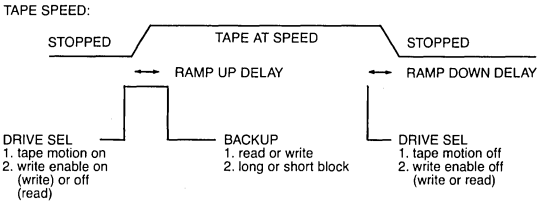
   The UDC will interrupt the system after the completion of the Ramp Up Delay indicating that the tape drive is up to speed. This interrupt is distinguished by the Command Termination Code of 0-0 (normal completion of command).

   The System then outputs the Write command (for a long or short block) and waits for the command termination interrupt. The UDC will write the Sync mark and tape mark or data block on the tape.

   When the System receives the interrupt indicating completion of the Write command, it will issue another drive select command with the Motor On and Write Enable bits set to stop the drive. The UDC will interrupt the system after completion of the Ramp Down Delay indicating that the tape has stopped moving.

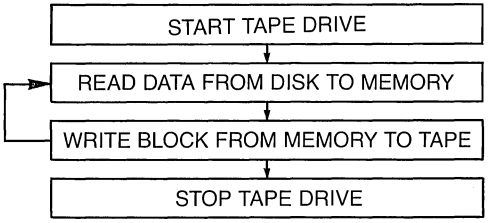
   The UDC will turn the Write Gate signal on when it is writing data and off when it is not, without regard to the tape motion. The Write Gate signal is used to generate "gaps" on the tape between the data blocks. This is done by externally forcing the two Data outputs with the Write Gate signal such that the Data + signal is high and the Data − signal is low when the UDC is not writing data to the tape (Write Gate is off):




   B. STREAMING TAPE DRIVE:

   typically transfers 1 sector at a time as illustrated by the following flow chart:




   Control of a streaming tape drive is similar to that of a start/stop drive. The tape is started at the beginning of the data transfer and stopped after the last block is written to the tape. The tape is not stopped in between blocks. The UDC will however turn the Write Gate signal on when it is writing data and off when it is not so that gaps will be written (with external hardware) on the tape between the data blocks.

5. BACK-UP READ. The data is read from the tape (in either start/stop or streamer mode) and buffered in memory. The disk track is then reconstructed from the data.

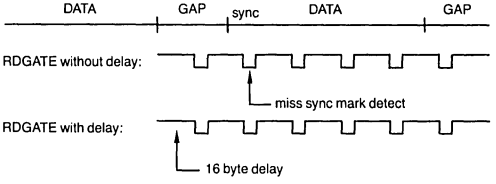
   The start/stop drive typically has a track (or half a track) of disk data stored as a block. It is therefore expedient to read in the data "block by block". When reading data from a streamer drive use can be made of the SECTOR COUNT register and a track's worth of data blocks may be read from the tape before generating the track on the disk.

   Tape motion control is similar to that described above except that the Write Enable Bit is off to inhibit writing to the tape. The UDC reads the tape until it detects a sync mark. After detecting a sync mark the UDC will transfer the data found on the tape to memory.

6. The search count is used when reading the tape. It specifies a maximum number of blocks of 128 bytes between adjacent data blocks. If the search count expires before sync is detected, the command is terminated.

   For example, if a search count of two is specified by loading the Desired Sector register with FD (hex), the UDC will search for 256 byte times before terminating the command. This will prevent the UDC from accidentally skipping a block. The search count is typically about the size of one block length. In the following figure, TM1 and TM2 are two tape marks and DB1, DB2, DB3 etc. are their associated Data Blocks:

7. 16 BYTE DELAY. Provision is made to shift the RDGATE pulse in the event that it coincides with the data block sync mark. If a tape cannot be read (sync is never detected) the tape can be re-read with the 16 byte delay enabled.




8. The DRIVE STATUS bits may be used by the tape drive if they are enabled (on the drive) by DRIVE SELECT 3. The ready change interrupt is especially handy for detecting start of tape (SOT) and end of tape (EOT) as a UDC command can be terminated by a change in state of the READY input.
9. The DATA FORMAT is as follows:

| PRE | TMSYNC | TAPE MARK | POST | GAP | PRE | DBSYNC | DATA BLOCK | POST GAP |
|---|---|---|---|---|---|---|---|---|

The Tape Mark sync mark (TMSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FE (Hex). The Data Block sync mark (DBSYNC) is composed of three bytes of A1 (Hex) followed by one byte of FB (Hex). A1 (Hex) is encoded with the standard missing clock pattern.

The sync mark is preceeded by a "preamble" consisting of bytes of 00 as per figure 2 of the UDC spec (this is required to synchronize the data separator when reading the tape). The Tape Mark and Data Block (including CRC or ECC bytes) are followed by a "postamble" consisting of one byte of 00.

Note that the postamble is not included in the Floppy Disk formats. The GAP sizes are dependent on the type of drive (start/stop or streamer) and the specific mechanical tape drive specifications.

10. Use can be made of the Sector Count register when doing a "file" (versus a "mirror image") backup on a start/stop tape drive. Instead of transferring the entire disk track to the tape in one long block, the data is moved file by file.

    If, for example, it is desired to back up a file consisting of five 256 byte long Hard Disk sectors, a 2048 byte long Data Block would have to be used for an image backup (the Data Block size is specified as $2^n * 128$ restricting blocks to 128, 256, 512 etc.). This would result in a lot of wasted space on the tape.

    If file backup is used and the Sector Count is set to five, 256 byte long Data Blocks can be used. Gaps will be generated on the tape corresponding to the time required to get the data from the disk drive (corresponding to DMA delays and the disk interleave factor).

    The tape will not be stopped until the entire file is transferred. When using sector count, the UDC internal programming will create inter-block gaps of about 30 to 32 bytes on the tape in both single (FM) and double (MFM) density modes.

## SYSTEM CONFIGURATION NOTES

A simplified UDC schematic is shown in Schematic 1. The following notes may be helpful in implementation of the UDC.

1. In systems using a private memory area, it is important to know when the buffer needs servicing from the host processor. A second interrupt signal (INT2) signals the processor that servicing is needed. INT2 is generated by externally ANDING the ECCTM signal with STB1 signal. (The STB1 signal is active when the UDC is outputing the DMA address data, and occurs when STB is active (low), S0 is active (high) and S1 is inactive (low)).

   This "interrupt" occurs only when the UDC needs the system processor to either read from or write to the buffer memory. When reading from the disk, the system processor should empty the memory buffer each time this signal becomes active. (If an ECC error is detected, and error correction is enabled, this signal will not become active until the UDC has attempted to correct the error.)

   When writing data to the disk, the system processor must fill the buffer each time this signal becomes active.
2. The DIP (DMA in Progress) signal is used to isolate the buffer memory from the main system memory. If 74LS244 and 74LS245 address buffers are used in the memory addressing circuits, then this signal should be used to enable or disable the address buffers, as required. This eliminates the possibility of memory contention problems.
3. Write precompensation (for floppy disks) is handled internally by the UDC. For hard disks, the LATE and EARLY signals are connected to a multiplexer which, in turn is connected to a 24 ns delay line. The EARLY and LATE signals will toggle in response to the data pattern being written. This will allow the data being written to the shifted ± 12 ns from the nominal 12 ns delay specified by hard disk manufacturers.
4. The interface to the hard disk drive data inputs and outputs requires RS-422 data tranceivers. Other disk drive interface circuits (including floppy disk data inputs and outputs) may be 74LS series devices.
5. Since the UDC uses its Aux Bus for multiple functions, the system designer must be able to determine which function is occuring on the Aux Bus at any given time. The S0 and S1 signals, when combined with STB signal are decoded (using a 74LS138 or equivalent) to provide STB0-3 signals.

   These generated signals and their respective functions are:

   | | |
   |---|---|
   | STB0 | Drive Status Input Time Slot |
   | STB1 | External DMA Address Counters Time Slot |
   | STB2 | Output 1 Time Slot |
   | STB3 | Output 2 Time Slot |

6. The clocks required by the UDC are not TTL-level compatible. Pullup resistors (typically 390 ohms) should be used with Schottky drivers to insure that the clock signals reach the proper Input (high) level, with acceptable rise and fall times.
7. The UDC features a built-in DMA controller that requires connection to external counters. These counters are configured so that they are incremented after each byte is transferred. (The UDC's internal DMA circuits transfer the starting memory address for each read or write operation.) 74LS161 Counters are typically used in this area.
8. The DMACLK input should be tied to the master system clock, through a bus buffer. It is important to remember that three DMACLK periods are required for each DMA transfer.
9. The system design may be simplified, and costs reduced, by using the FDC 9216B Floppy Disk Data Separator, to separate raw data from the floppy disk drive into RDATA and RCLK.

## ERROR CHECKING AND CORRECTION CIRCUIT (ECC) OPERATING PRINCIPLES

The UDC will automatically detect and correct errors in the data read from the disk. Error checking may be done using industry standard CRC or ECC encoding. Error correction may be done using either internal or external ECC encoding. This section will explain ECC operation, as implemented on the UDC.

The UDC contains two 16-bit registers used by the CRC/ECC circuits. CRC logic uses only one of these registers, while the logic for ECC uses both registers, implementing a full 32-bit algorithm.

These registers may be preset to either one or zero, using the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION register. (This allows compatibility with existing disk controllers and external ECC chips.) Both ECC and CRC are calculated beginning with the sync mark of the address (CRC) or data (ECC) field.

### CRC/ECC GENERATION

The UDC uses the following industry standard polynomials in computing the CRC and ECC check bytes:

CRC: $x^{16} + x^{12} + x^5 + 1$

ECC: $x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$

As the UDC writes data to the disk drive, it first passes this data thru the CRC (and, if enabled, ECC) registers. After all data has been written, the remaining two (CRC) or four (ECC) bytes remaining in these registers are written to the appropriate address or data field.

### CRC/ECC CHECKING

When CRC or ECC checking is initiated, the internal CRC/ECC registers are set to either zero or one, as required by the CRC PRESET bit in the INTERRUPT/COMMAND TERMINATION REGISTER. Data read from the disk is simultaneously shifted thru the CRC/ECC registers, and transferred to external memory.

After the CRC or ECC check bytes have been shifted thru the CRC/ECC registers, the remainder in these registers should be zero, else an error has occurred in the address or data block.

If CRC or ECC (without correction) is enabled, automatic retry (if enabled) or command termination will occur. If internal ECC with automatic correction is enabled, the correction algorithm will be executed. If the internal ECC algorithm is unable to correct the error (in one attempt), then automatic retry (if enabled) or command termination will occur.

### ECC CORRECTION

Error Correction consists of three distinct parts:

1. The CRC/ECC registers are normalized by shifting zeros thru the register. This sets up a data block which is 42,987 bits long, which corresponds to the "natural message length" of the generation polynomial. The actual number of zeros shifted through the registers depends on the difference between the natural message length of the generator polynomial and the actual length of the data block being checked. The longest data block that can be corrected (using the internal ECC algorithm) is 4K bytes.
2. The data input to the CRC/ECC registers is then disabled and the DMA counters are re-initialized to the starting address for this data block. The contents of the CRC/ECC registers are then "ring-shifted" until 21 consecutive zeros are detected. The remaining bits in the CRC/ECC registers compose the error syndrome. As the CRC/ECC registers are shifted, the UDC generates $\overline{DS}$ signals, causing the external DMA counters to be incremented. When the 21 consecutive zeros are detected, the DMA counters are pointing to the corrupt data.

   If the error syndrome is not found within the data block the error is judged to be uncorrectable and the correction algorithm is terminated. (The data block is the length of the data field in the sector and the 4 ECC bytes. A format with a sector size of 256 bytes would have a data block size of 260 bytes.)
3. When the error syndrome is detected, the UDC will enable its $\overline{ECCTM}$ output, read the next byte from memory, exclusive-or it with the first byte of the three byte error syndrome, disable the $\overline{ECCTM}$ output and write the corrected byte back to memory. The correction process is then repeated for the next two bytes in memory.

   When using internal ECC (with correction enabled), the $\overline{ECCTM}$ output is used by the external DMA counters to inhibit the counters from incrementing their addresses when correcting the erroneous bytes. When using external ECC, the $\overline{ECCTM}$ output goes active (low) when the UDC is requesting the ECC Check Bytes from the external ECC chip prior to writing them to the disk.

   After a correction is completed, the UDC will then attempt to read the next sector on the disk (if the SECTOR COUNT register is still greater than zero). Anytime ECC correction has been attempted, (even if unsuccessful), the CORRECTION ATTEMPTED bit in the CHIP STATUS register will be set.

The maximum time required for one ECC Correction Cycle (using the internal algorithm) is:

1) $\frac{\text{(Natural Message Length [Bits])}}{8} + 4 =$ ECC Cycle Time (in Byte times)

2) Maximum ECC Time = ECC Cycle Time + 30 byte times

Since the internal algorithm has a natural message length of 42,987 bits the ECC Cycle time is 5,377 byte times. Since a period of about 30 byte times must be allowed for the read-modify-write operations, the Maximum ECC Time equals 5,407 byte times.

One byte time equals the amount of time required to read one byte for the type of drive selected. For Hard Disks, this is about 1 microsecond. This equates to approximately 1 revolution (maximum) for either 8" floppy disk (running in double density) or 5.25" hard disk.

During the entire operation, the RDGATE signal is kept active.

**MAXIMUM GUARANTEED RATINGS***

Operating Temperature Range ..... 0 to +70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec.) ..... +325 C
Positive Voltage on any Pin, with respect to ground ..... +8 V
Negative Voltage on any Pin, with respect to ground ..... −0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

**DC ELECTRICAL CHARACTERISTICS** Ta = 0 C to +70 C, Vcc = 5.0V ±5%

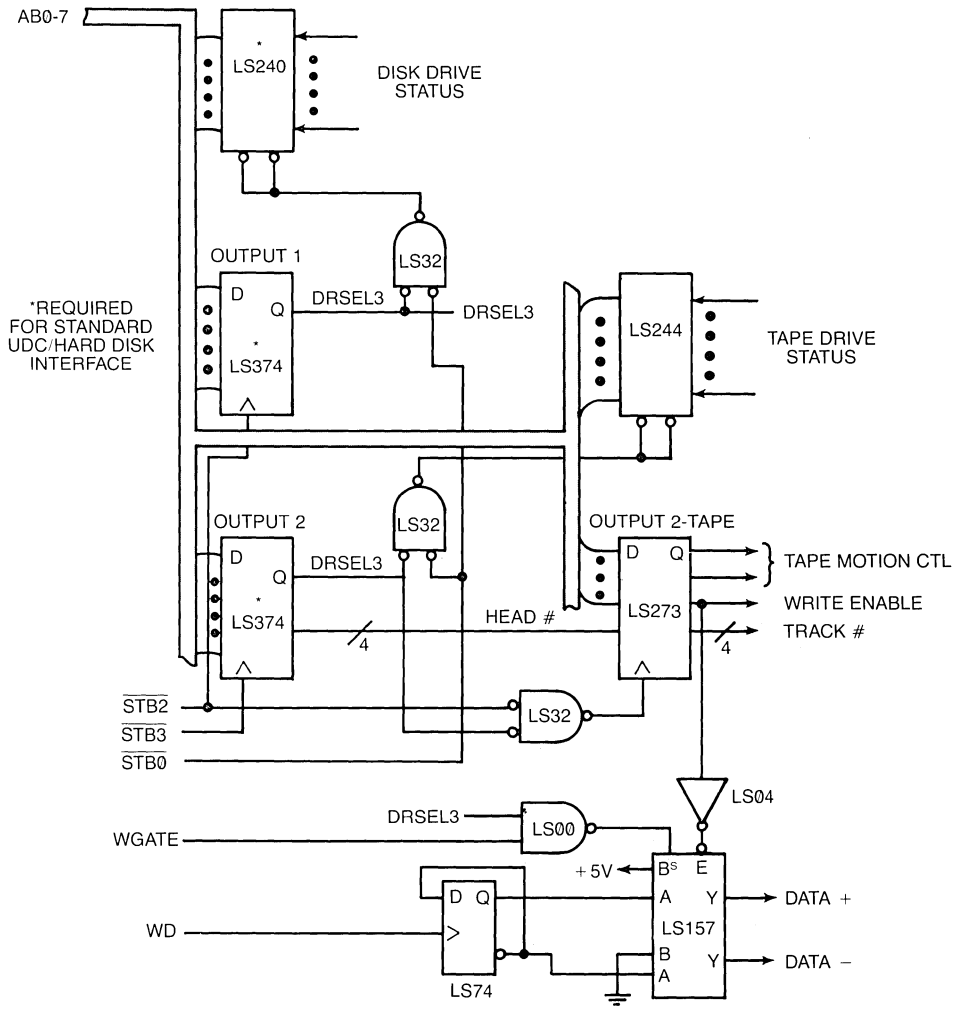
| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS | |
|---|---|---|---|---|---|---|
| Input Voltage | | | | | | |
| $V_{IL}$ Low | | | 0.8 | V | | |
| $V_{IH1}$ High | 2.0 | | | V | all inputs except CLK and DMACLK | |
| $V_{IH2}$ High | 4.2 | | | V | CLK and DMACLK input | |
| Output Voltage | | | | | | |
| $V_{OL1}$ Low | | | 0.4 | V | all outputs except WDATA, | $I_{OL1}$ = 1.6 mA |
| $V_{OH1}$ High | 2.4 | | | V | Early and Late. (Drive 1 TTL load into 50 pf) | $I_{OH1}$ = 40μA |
| $V_{OL2}$ Low | | | 0.5 | V | WDATA, EARLY and LATE | $I_{OL2}$ = 2mA |
| $V_{OH2}$ High | 2.7 | | | V | outputs. (Will drive 1 Schottky load into 15 pf.) | $I_{OH2}$ = 50μA |
| $V_{OL3}$ Low | | | 0.4 | V | DMAR and INT | $I_{OL3}$ = 0.4 mA |
| $V_{OH3}$ High | 2.4 | | | V | DMAR and INT | $I_{OH3}$ = 20μA |
| Input Leakage Current | | | | | 0.4V to 3.5V | |
| $I_L$ | | | ±10 | uA | | |
| $I_{LC}$ (Clock) | | | −600 | μA | 0V | |
| Input Capacitance | | | | | | |
| $C_{IN}$ | | | 25 | pf | | |
| Power Supply Current | | | | | | |
| Icc | | | 200 | ma | | |

**AC ELECTRICAL CHARACTERISTICS** Ta = 0 C to +70 C, Vcc = 5.0V ±5%

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| PROCESSOR WRITE CYCLE | | | | | | |
| C/D, R/W, CS Setup time to DS↓ | $T_{DSB}$ | 110 | | | ns | FIGURE 3 |
| C/D, R/W, CS Hold time to DS↑ | $T_{DSB}$ | 0 | | | ns | |
| DS Pulse Width | $T_{DSL}$ | 150 | | | ns | |
| DS Pulse High Time | $T_{DSH}$ | 850 | | | ns | |
| Data Bus In Setup time to DS↑ | $T_{DIB}$ | 100 | | | ns | |
| Data Bus In Hold time to DS↑ | $T_{DIA}$ | 0 | | | ns | |
| PROCESSOR READ CYCLE | | | | | | |
| Data Access time from DS↓ | $T_{DOB}$ | 75 | | | ns | FIGURE 3 |
| Data Hold time from DS↑ | $T_{DOA}$ | 10 | | | ns | |
| UDC TO MEMORY TIMING (BUS MASTER) (based on 10 Mhz DMACLK Input) | | | | | | |
| Write Setup time to DS↓ | $T_{WB}$ | 110 | | | ns | FIGURE 4 |
| Write Data Strobe Width | $T_{WDS}$ | 180 | | | ns | |
| Write Hold time from DS↑ | $T_{WA}$ | 110 | | | ns | |
| Data Strobe Falling Edge | $T_{DSF}$ | | | 15 | ns | |
| Data Strobe Rising Edge | $T_{DSR}$ | | | 20 | ns | |
| Write Data Valid before DS↑ | $T_{WDB}$ | | | 90 | ns | |
| Write Data Hold time after DS↑ | $T_{WDA}$ | 10 | | | ns | |
| Memory Access Time | $T_W$ | | 200 | | ns | |

SECTION VI

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| Read Setup time to $\overline{DS}\downarrow$ | $T_{RB}$ | 110 | | | ns | FIGURE 4 |
| Read Hold time after $\overline{DS}\uparrow$ | $T_{RA}$ | 110 | | | ns | |
| Read Data Strobe Pulse Width | $T_{RDS}$ | 180 | | | ns | |
| Read Data Setup time to $\overline{DS}\uparrow$ | $T_{RDB}$ | 50 | | | ns | |
| Read Data Hold time from $\overline{DS}\uparrow$ | $T_{RDA}$ | 0 | | | ns | |
| DMACLK$\uparrow$ to $\overline{DS}\downarrow$ | $T_{DDD}$ | | | 100 | ns | |
| DMACLK$\uparrow$ to $\overline{DS}\uparrow$ | $T_{DDA}$ | | | 100 | ns | |
| S0, S1, AND $\overline{STB}$ TIMING | | | | | | |
| $\overline{STB}$ Width | $T_{SW}$ | 800 | | | ns | FIGURE 7 |
| S0, S1 Hold time after $\overline{STB}\uparrow$ | $T_{SD}$ | 100 | | | ns | |
| Data In Setup time to $\overline{STB}\uparrow$ | $T_{DIS}$ | 700 | | | ns | |
| Data In Hold time after $\overline{STB}\uparrow$ | $T_{DIH}$ | 0 | | | ns | |
| S0, S1 Setup time to $\overline{STB}\downarrow$ | $T_{SST1}$ | 100 | | | ns | |
| Aux Bus Setup time to $\overline{STB}\downarrow$ | $T_{SST2}$ | 100 | | | ns | |
| Aux Bus Hold time after $\overline{STB}\uparrow$ | $T_{SST3}$ | | | 100 | ns | |
| INPUT CLOCK TIMING (10 MHz Input) | | | | | | |
| Clock Rise Time | $T_{RT}$ | | | 10 | ns | FIGURE 2 |
| Clock Fall Time | $T_{RF}$ | | | 10 | ns | |
| Clock Cycle High Time | $T_{CH}$ | 40 | | | ns | |
| Clock Cycle Low Time | $T_{CL}$ | 40 | | | ns | |
| Clock Cycle Time | $T_{CYC}$ | 95 | 100 | 105 | ns | |
| PRECOMPENSATION TIMING | | | | | | |
| Early, Late Setup time (Before WDATA$\uparrow$) | $T_{PB}$ | 0 | | | ns | FIGURE 9 |
| Early, Late Hold Time (after WDATA$\downarrow$) | $T_{PB}$ | 50 | | | ns | |
| FLOPPY INPUT DATA TIMING | | | | | | |
| Window Setup time to RDCLK | $T_{FRB}$ | 50 | | | ns | FIGURE 10 |
| Window Hold time from $\overline{RDDATA}\uparrow$ | $T_{FRA}$ | 50 | | | ns | |
| HARD DISK INPUT DATA TIMING | | | | | | |
| Data Setup time to RDCLK$\downarrow$ | $T_{HRB}$ | 60 | | | ns | FIGURE 10 |
| Data Hold time after RDCLK$\downarrow$ | $T_{HRA}$ | 10 | | | ns | |
| Clock Setup time to RDCLK$\uparrow$ | $T_{HCB}$ | 60 | | | ns | |
| Clock Hold time from RCLK$\uparrow$ | $T_{HCA}$ | 10 | | | ns | |
| ECCTIM TIMING | | | | | | |
| $\overline{ECCTM}$ Setup to $\overline{DS}\downarrow$ | $T_{EDS}$ | 50 | | | | FIGURE 10 |
| $\overline{ECCTM}$ Hold after $\overline{DS}\uparrow$ | $T_{EDH}$ | 100 | | | ns | |
| RESET TIMING | | | | | | |
| $\overline{RST}$ Pulse Width | | 1 | | | µs | |




**SCHEMATIC 2: UDC/TAPE DRIVE INTERFACE CIRCUIT**

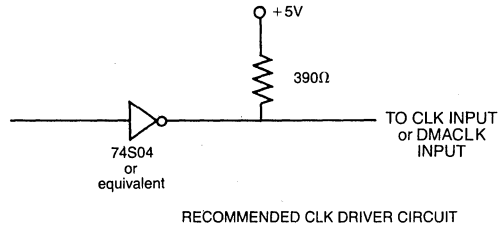



**FIGURE 1: RECOMMENDED CLK/DMACLK INPUT**

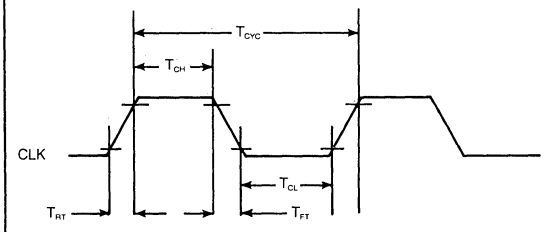



**FIGURE 2: INPUT CLOCK TIMING (10MHz)**

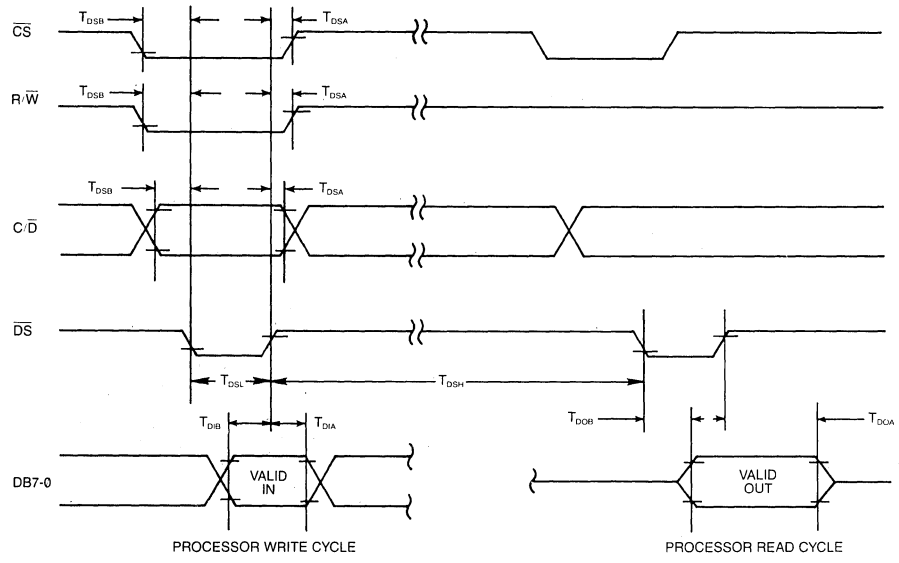



**FIGURE 3: SYSTEM PROCESSOR TO UDC TIMING**

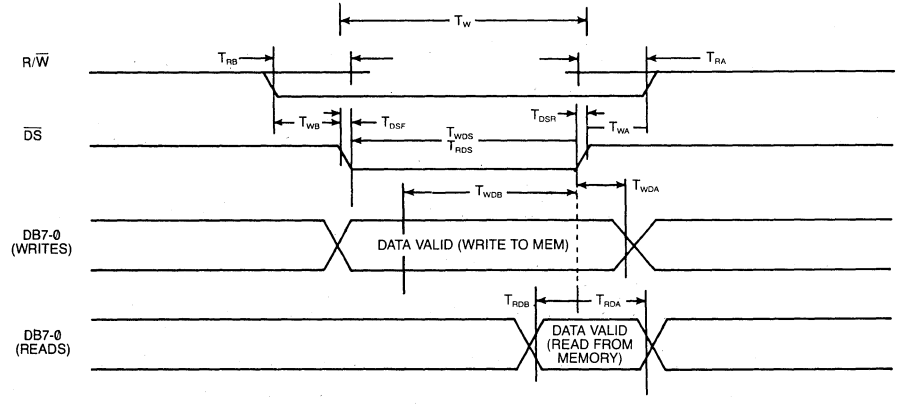



**FIGURE 4: UDC TO MEMORY TIMING (BUS MASTER)**

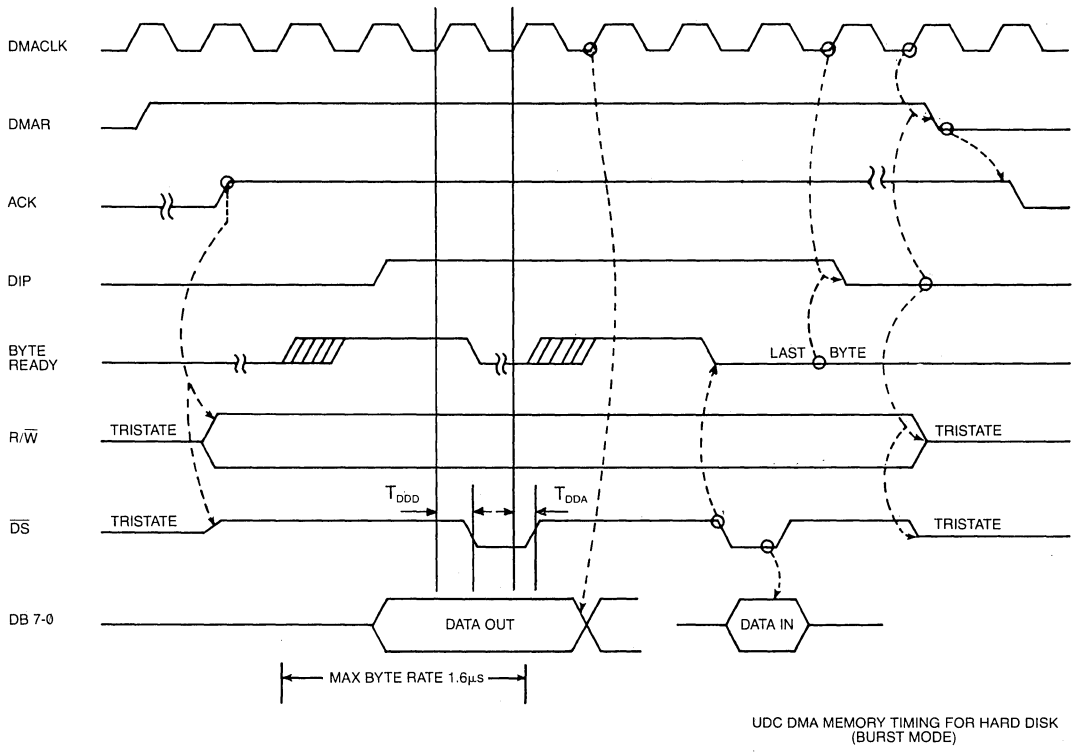



**FIGURE 5: UDC DMA MEMORY TIMING FOR HARD DISK (BURST MODE)**

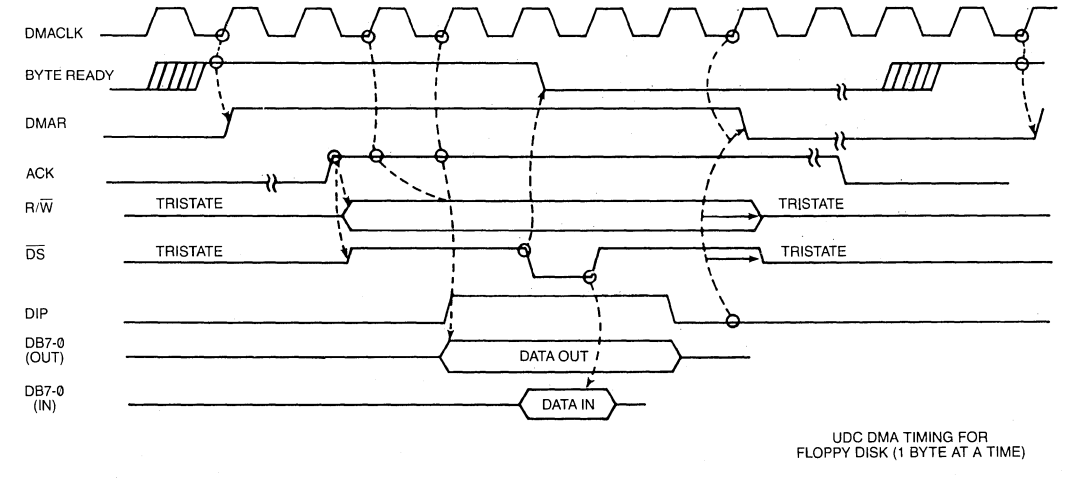



**FIGURE 6: UDC DMA TIMING FOR FLOPPY DISK (1 BYTE AT A TIME)**

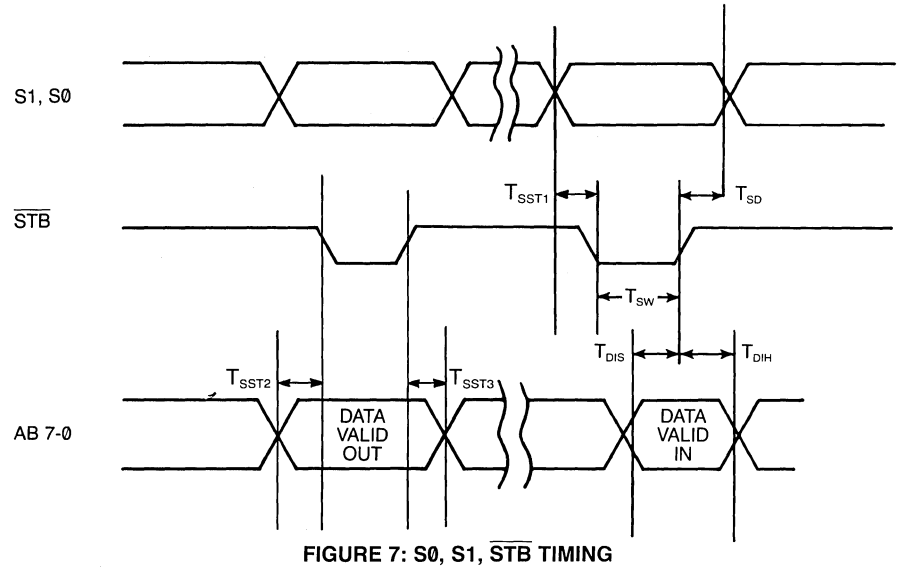



**FIGURE 7: SØ, S1, STB TIMING**

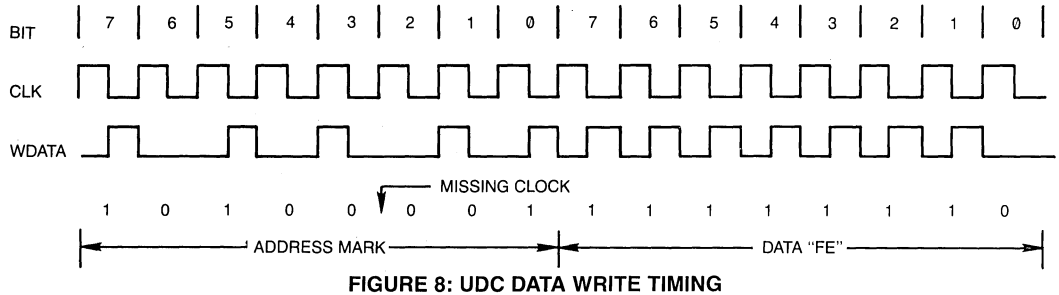
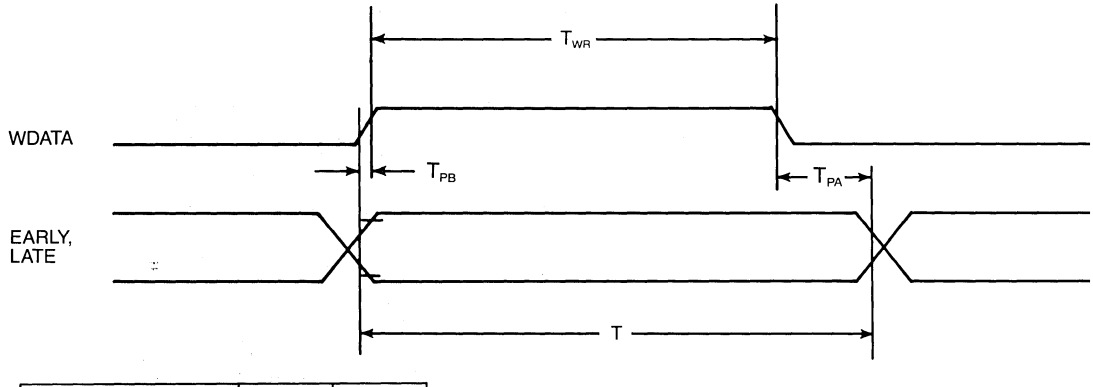
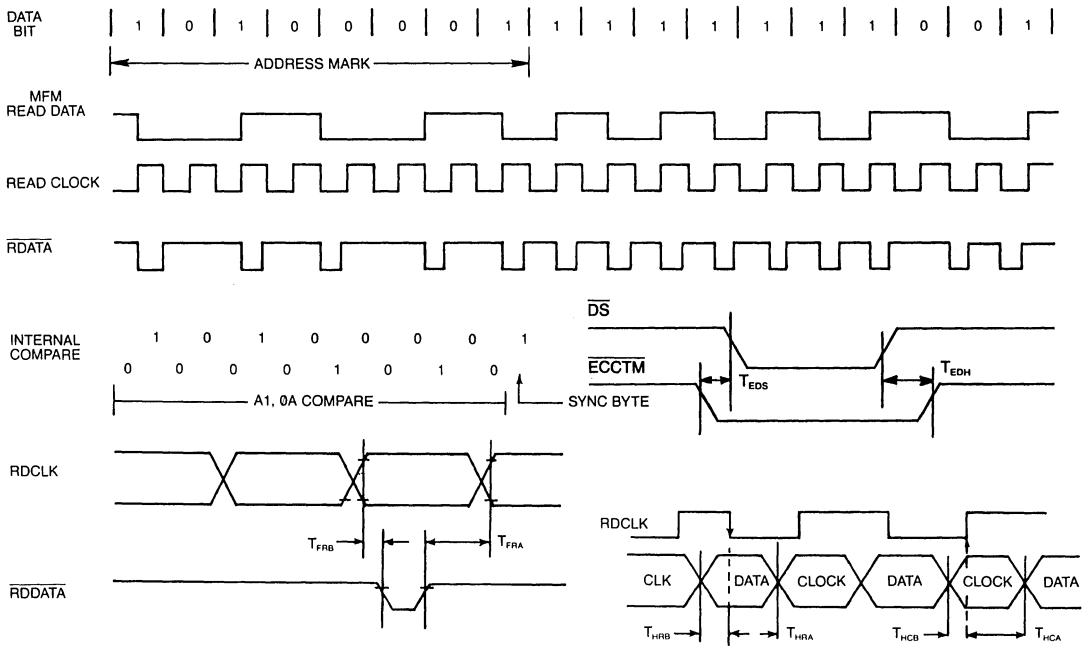



**FIGURE 8: UDC DATA WRITE TIMING**




| DRIVE TYPE | T (typ) | $T_{WR}$ (typ) |
|---|---|---|
| HARD DISK | 200 NS | 100 NS |
| 8" MFM FLOPPY | 2 µs | 300 NS |
| 8" FM FLOPPY | — | 300 NS |
| 5¼" MFM FLOPPY | 4µs | 300 NS |
| 5¼" FM FLOPPY | — | 300 NS |

**FIGURE 9: PRECOMPENSATION TIMING**




**FLOPPY INPUT DATA TIMING (HARD DISK BIT = 0)**

**HARD DISK INPUT DATA TIMING (HARD DISK BIT = 1)**

**FIGURE 10**

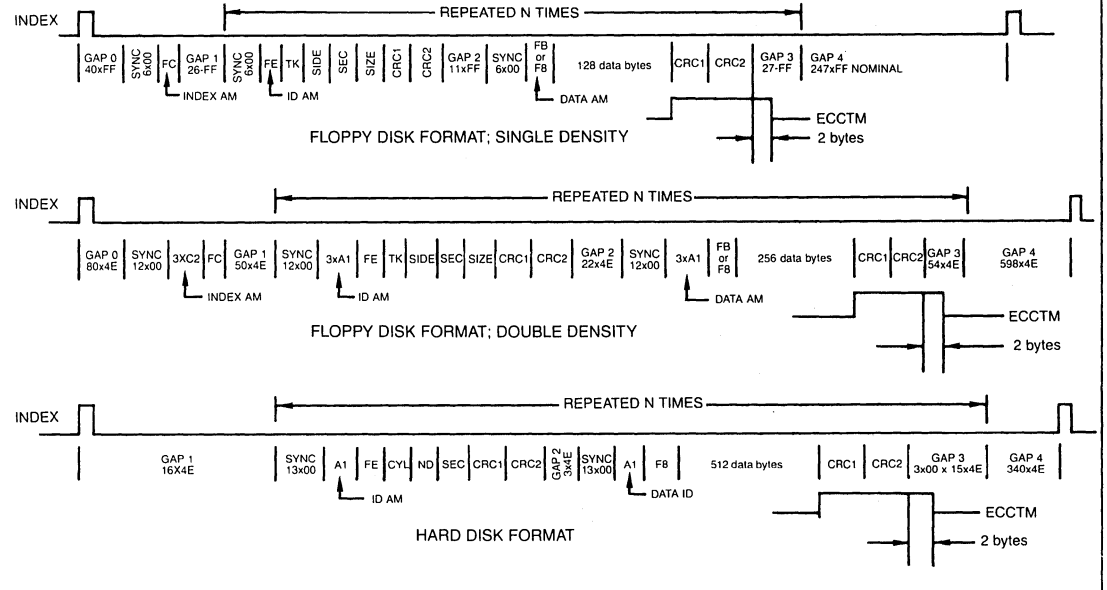



**FIGURE 11: DISK FORMATS**

SECTION VI

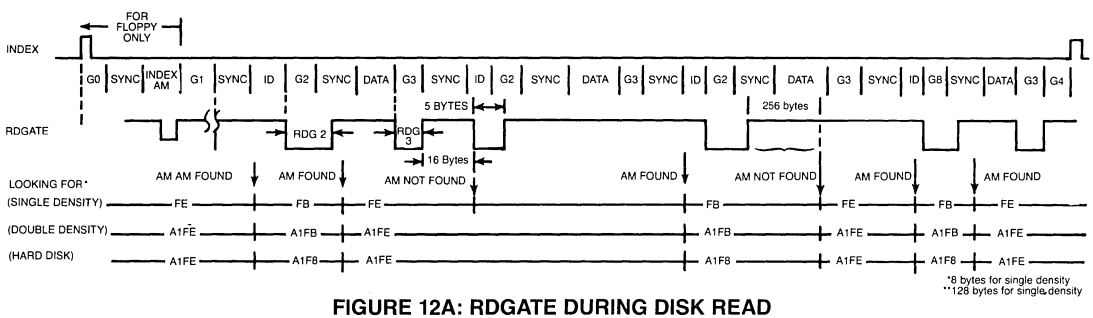



**FIGURE 12A: RDGATE DURING DISK READ**

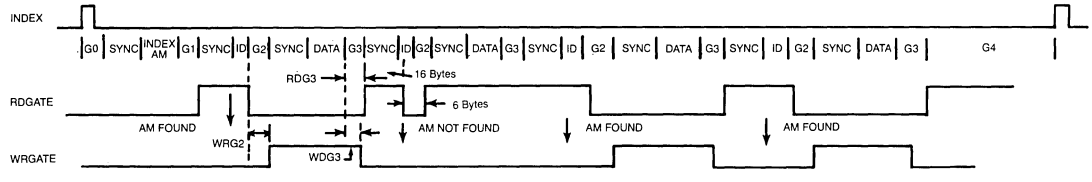



**FIGURE 12B: RDGATE AND WRITE GATE TIMING**

| STANDARD FORMAT PARAMETERS | | | |
|---|---|---|---|
| PARAMETER | HARD DISK | SINGLE DEN. FLOPPY | DOUBLE DEN. FLOPPY |
| GAP 0 * | 0 | 40 | 80 |
| GAP 1 * | 16 | 26 | 50 |
| GAP 2 * | 3 | 11 | 22 |
| GAP 3 * | 18 | 27 | 54 |
| SYNC SIZE * | 13 | 6 | 12 |
| SECTOR COUNT * | user selectable | user selectable | user selectable |
| SECT. SIZE MULT * | user selectable | user selectable | user selectable |
| RDG 1 | 16 | 73 | NA |
| RDG 2 | 6 | 13 | 24 |
| RDG 3 | 25 | 27 | 24 |
| WDG 2 | 5 | 11 | 23 |
| WDG 3 | 3 | 11 | 3 |
| * = PARAMETER USED BY FORMAT COMMAND | | | |

**TABLE 1: STANDARD FORMAT PARAMETERS**

**REGISTER BIT DEFINITIONS**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| DMA 7-0 (REGISTER 0) | (MSB) | | | LOW ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS | | | | (LSB) |
| DMA 15-8 (REGISTER 1) | (MSB) | | | MIDDLE ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS | | | | (LSB) |
| DMA 23-16 (REGISTER 2) | (MSB) | | | HIGH ORDER BYTE OF DMA BUFFER MEMORY STARTING ADDRESS | | | | (LSB) |
| DESIRED SECTOR (REGISTER 3) | (MSB) | | | DESIRED SECTOR NUMBER | | | | (LSB) |
| DESIRED HEAD (REGISTER 4) | ALWAYS 0 | | (MSB) HIGH ORDER BITS OF DESIRED CYLINDER | | (MSB) DESIRED HEAD NUMBER | | | (LSB) |
| DESIRED CYLINDER (REGISTER 5) | (MSB) | | | LOW ORDER BITS OF DESIRED CYLINDER | | | | (LSB) |
| SECTOR COUNT (REGISTER 6) | (MSB) | | | NUMBER OF SECTORS TO BE OPERATED ON BY COMMAND | | | | (LSB) |
| RETRY COUNT (REGISTER 7) | RETRY COUNT (1'S COMPLEMENT) | | | | PROGRAMMABLE OUTPUTS | | | |
| MODE (REGISTER 8) | HARD DISK | CRC/ECC | ENABLE | SINGLE DENSITY | ALWAYS 0 | STEP | RATE | SELECT |
| INTERRUPT/ COMMAND TERM. (REGISTER 9) | CRC PRESET 1 = Set to 1 0 = Set to 0 | ALWAYS 0 | INTERRUPT ON DONE | FLAG DELETED DATA MARK | USER DEFINED FLAG | FLAG WRITE PROTECT | FLAG READY CHANGE | FLAG WRITE FAULT |
| DATA/DELAY (REGISTER A) | (MSB) | | | HEAD LOAD DELAY MULTIPLE IS LOADED INTO THIS REGISTER DATA IS LOADED TO OR READ FROM THIS REGISTER | | | | (LSB) |
| CURRENT HEAD (READ REGISTER 4) | BAD SECTOR FLAG | | (MSB) HIGH ORDER BITS OF CURRENT CYLINDER | | (MSB) CURRENT HEAD NUMBER | | | (LSB) |
| CURRENT CYLINDER (READ REGISTER 5) | (MSB) | | | LOW ORDER BITS OF CURRENT CYLINDER NUMBER | | | | (LSB) |
| CHIP STATUS (READ REGISTER 8) | RETRY REQUIRED | ECC CORRECTION ATTEMPTED | CRC/ECC ERROR | DELETED DATA MARK READ | SYNC ERROR | COMPARE ERROR | PRESENT DRIVE SELECTED | |
| DRIVE STATUS (READ REGISTER 9) | ECC ERROR | INDEX | SEEK COMPLETE | TRACK 00 | USER DEFINED ACTIVE | WRITE PROTECT ACTIVE | DRIVE READY | WRITE FAULT |
| INTERRUPT STATUS (COMMAND READ) | INTERRUPT PENDING | DMA REQUEST | DONE | COMMAND TERMINATION CODE | | READY CHANGE | OVERRUN/ UNDERRUN | BAD SECTOR |

**TABLE 2: REGISTER BIT MAPS**

**UDC WRITE REGISTERS (APPLIES DURING TAPE BACKUP ONLY)**

| REGISTER | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| DMA 7-0 (REGISTER 0) | (MSB) | DMA BEGINNING ADDRESS BUTE (LOW ORDER BITS) | | | | | | (LSB) |
| DMA 15-8 (REGISTER 1) | (MSB) | DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS) | | | | | | (LSB) |
| DMA 23-16 (REGISTER 2) | (MSB) | DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS) | | | | | | (LSB) |
| DESIRED SECTOR (REGISTER 3) | (MSB) | MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT) (1) | | | | | | (LSB) |
| DESIRED HEAD (REGISTER 4) | 0 | 0 | 0 | 0 | TRK # BIT 3 | TRK # BIT 2 | TRK # BIT 1 | TRK # BIT 0 |
| DESIRED CYLINDER (REGISTER 5) | ECC TYPE | | | | ALWAYS 1 | DATA BLOCK SIZE | | |
| SECTOR COUNT (REGISTER 6) | TAPE MARK BLOCK SIZE (IN 2'S COMPLEMENT + 1) (MODULO 256) (2) | | | OR | DATA BLOCK COUNT (IN 1'S COMPLEMENT) (3) | | | |
| RETRY COUNT (REGISTER 7) | 1 | 1 | 1 | 1 | USER DEFINED OUTPUTS | | | |
| MODE (REGISTER 8) | ALWAYS "0" FOR TAPE | CRC/ECC ENABLE CODE | | SINGLE/ DOUBLE DENSITY | ALWAYS 0 | SYNC DELAY ENABLE | WRITE ENABLE | TAPE MARK ENABLE |
| INTERRUPT/ COMMAND TERMINATOR (REGISTER 9) | CRC PRESET | ALWAYS 0 | INTERRUPT ON DONE | ALWAYS 1 | USER DEFINED | FLAG WRITE PROTECT | FLAG READY CHANGE | FLAG WRITE FAULT |

NOTES: (1) The maximum search count is composed of:
130 byte inner loop (RDGATE high 128, 2 byte times)
times the number programmed (maximum of 33,150 byte times
(2) Tape mark operation
(3) Data block operation

**TABLE 3: TAPE BACKUP REGISTER BIT MAPS**

**UDC READ REGISTERS (APPLIES TAPE BACKUP ONLY)**

| REGISTER | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| DMA 7-0 (REGISTER 0) | (MSB) | DMA BEGINNING ADDRESS BYTE (LOW ORDER BITS) | | | | | | (LSB) |
| DMA 15-8 (REGISTER 1) | (MSB) | DMA BEGINNING ADDRESS BYTE (MIDDLE ORDER BITS) | | | | | | (LSB) |
| DMA 23-16 (REGISTER 2) | (MSB) | DMA BEGINNING ADDRESS BYTE (HIGH ORDER BITS) | | | | | | (LSB) |
| DESIRED SECTOR (REGISTER 3) | (MSB) | MAXIMUM SEARCH COUNT (IN 1'S COMPLEMENT) | | | | | | (LSB) |
| CURRENT HEAD (REGISTER 4) | X | X | X | X | X | X | X | X |
| CURRENT CYLINDER (REGISTER 5) | X | X | X | X | X | X | X | X |
| CHIP STATUS (REGISTER 8) | X | ECC CORRECTION ATTEMPTED | CRC/ECC ERROR | X | X | X | PRESENT DRIVE SELECTED | |
| DRIVE STATUS (REGISTER 9) | USER DEFINED | USER DEFINED | SEEK COMP | USER DEFINED | USER DEFINED | WRITE PROTECT | READY | WRITE FAULT |
| DATA (REGISTER A) | READ DATA | | | | | | | |
| INTERRUPT STATUS (COMMAND READ) | INT PENDING | DMA REG | DONE | COMMAND TERMINATION CODE (1) | | READY CHANGE | OVER/ UNDER RUN | X |

NOTES: (1) Command termination bits set to:
11 for data transfer error
10 for sync error
00 for successful termination
X Don't care

**TABLE 4: TAPE BACKUP REGISTER BIT MAPS**

**COMMAND BIT DEFINITIONS**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DESELECT DRIVES | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| RESTORE DRIVE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 = Buffered Seek<br>0 = Normal Seek |
| STEP IN 1 CYLINDER | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 = Buffered Seek<br>0 = Normal Seek |
| STEP OUT 1 CYLINDER | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 = Buffered Seek<br>0 = Normal Seek |
| POLL DRIVES | 0 | 0 | 0 | 1 | 1 = Poll Drive 3<br>0 = Don't Poll | 1 = Poll Drive 2<br>0 = Don't Poll | 1 = Poll Drive 1<br>0 = Don't Poll | 1 = Poll Drive 0<br>0 = Don't Poll |
| SELECT DRIVE | 0 | 0 | 1 | 1 = Head Load Delay Enabled<br>0 = Delay Disabled | TYPE OF DRIVE | | DRIVE UNIT SELECTED | |
| SET REGISTER POINTER | 0 | 1 | 0 | 0 | REGISTER | | NUMBER | |
| SEEK/READ ID | 0 | 1 | 0 | 1 | 0 | Step Enable | Wait For Complete | Verify ID |
| READ SECTORS PHYSICAL | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Enable Transfer |
| READ TRACK | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 = Transfer All<br>0 = Transfer ID |
| READ SECTORS LOGICAL | 0 | 1 | 0 | 1 | 1 | 1 | 1 = Bad Sector Bypass<br>0 = Bad Sector Terminate | Enable Transfer |
| FORMAT TRACK | 0 | 1 | 1 | Write Deleted Data | Write With Reduced Current | PRECOMPENSATION VALUE | | |
| WRITE SECTORS PHYSICAL | 1 | 1 = Bad Sector Bypass<br>0 = Bad Sector Termination | 0 | Write Deleted Data | Write With Reduced Current | PRECOMPENSATION VALUE | | |
| WRITE SECTORS LOGICAL | 1 | 1 = Bad Sector Bypass<br>0 = Bad Sector Terminate | 1 | Write Deleted Data | Write With Reduced Current | PRECOMPENSATION VALUE | | |
| TAPE BACKUP | 0 | 0 | 0 | 0 | 1 | WRITE: | PRECOMPENSATION VALUE | |
| | | | | | | READ: | 0 0 | Transfer Enable |

**TABLE 5: COMMAND WORD BIT MAPS**

SECTOR SIZE FIELD BITS

| DB2 | DB1 | DB0 | IBM FD FORMAT | HD FORMAT |
|---|---|---|---|---|
| 0 | 0 | 0 | 128 bytes/sector | 128 bytes/sector |
| 0 | 0 | 1 | 256 bytes/sector | 256 bytes/sector |
| 0 | 1 | 0 | 512 bytes/sector | 512 bytes/sector |
| 0 | 1 | 1 | 1024 bytes/sector | 1024 bytes/sector |
| 1 | 0 | 0 | not used | 2048 bytes/sector |
| 1 | 0 | 1 | not used | 4096 bytes/sector |
| 1 | 1 | 0 | not used | 8192 bytes/sector |
| 1 | 1 | 1 | not used | 16,384 bytes/sector |

FORMAT ECC TYPE FIELD

| DB7 | DB6 | DB5 | DB4 | HD FORMAT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 4 ECC bytes generated/checked |
| 1 | 1 | 1 | 1 | 5 ECC bytes generated/checked (1) |
| 1 | 1 | 1 | 0 | 6 ECC bytes generated/checked (1) |
| 1 | 1 | 0 | 1 | 7 ECC bytes generated/checked (1) |

note 1: WITH EXTERNAL ECC

IBM FLOPPY DISK FORMAT:

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | | | track number | | | | | |
| HEAD | | | side number | | | | | |
| SECTOR | | | sector number | | | | sector size | |
| SECTOR SIZE | | | | | | | (2 bits) | |

HARD DISK FORMAT: ST506 PC FORMAT (512 BYTES)

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | cylinder number (8 LSB's) | | | | | | | |
| HEAD | bad sector flag | cyl # bit 10 | cyl # bit 9 | hd # bit 8 | hd # bit 3 | hd # bit 2 | hd # bit 1 | hd # bit 0 |
| SECTOR | sector number | | | | | | | |

HARD DISK FORMAT: (USER SELECTABLE SECTOR SIZE)

| ID FIELD | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|
| CYLINDER | cylinder number (8 LSB's) | | | | | | | |
| HEAD | bad sector flag | cyl # bit 10 | cyl # bit 9 | hd # bit 8 | hd # bit 3 | hd # bit 2 | hd # bit 1 | hd # bit 0 |
| SECTOR | sector number | | | | | | | |
| SECTOR SIZE | ECC type | | | | X | sector size (3 bits) | | |

**DISK FORMATS**

**TABLE 6**

For additional information, please consult the following:

- Technical Note 6-2 (9224 Overview)
- Technical Note 6-4 (Using the HDC 9226 HARD DISK DATA SEP.)
- Technical Note 6-5 (Programmer's Reference Manual)
- HDC 9225 Data Sheet
- HDC 9226 Data Sheet
- HDC 9224 Programmer's Quick Reference Card

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

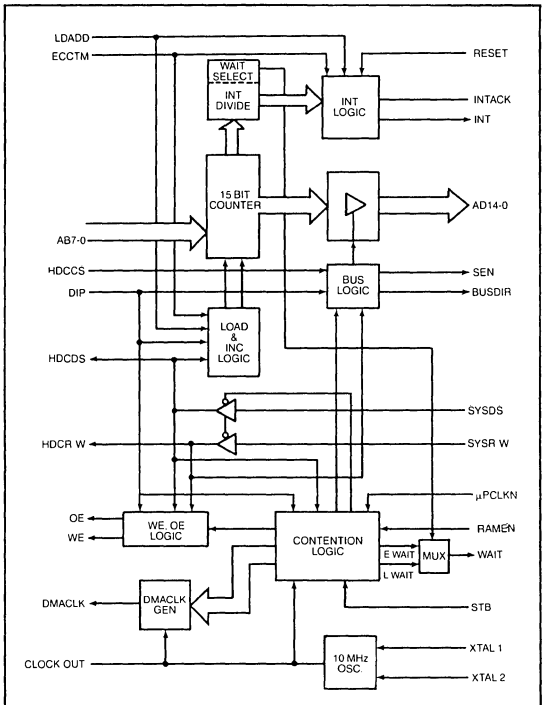
STANDARD MICROSYSTEMS CORPORATION

# HDC 9225

# DISK BUFFER MANAGEMENT UNIT "DBMU"

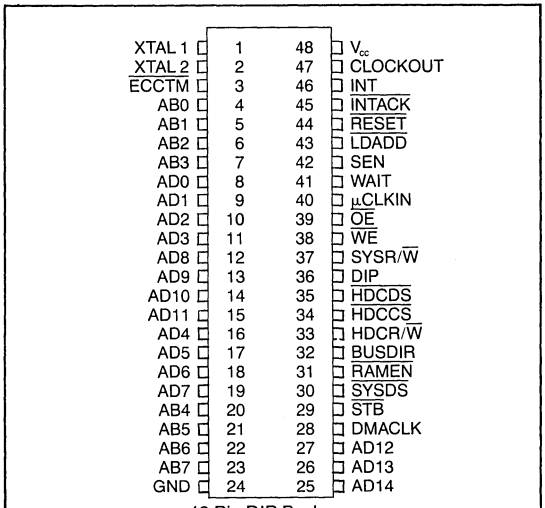
## FEATURES

- ☐ Significantly reduces chip count in hard disc systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Creates a dual-port disk buffer (up to 32K in size) using low cost static ram
- ☐ Programmable sector interrupt counter allows host processor rapid access to data
- ☐ On board 10 MHz oscillator simplifies clock generation
- ☐ Allows disk interleave factor of 1, improving system performance
- ☐ Fabricated in low power CMOS; fully TTL compatible




**BLOCK DIAGRAM**

## PIN CONFIGURATION



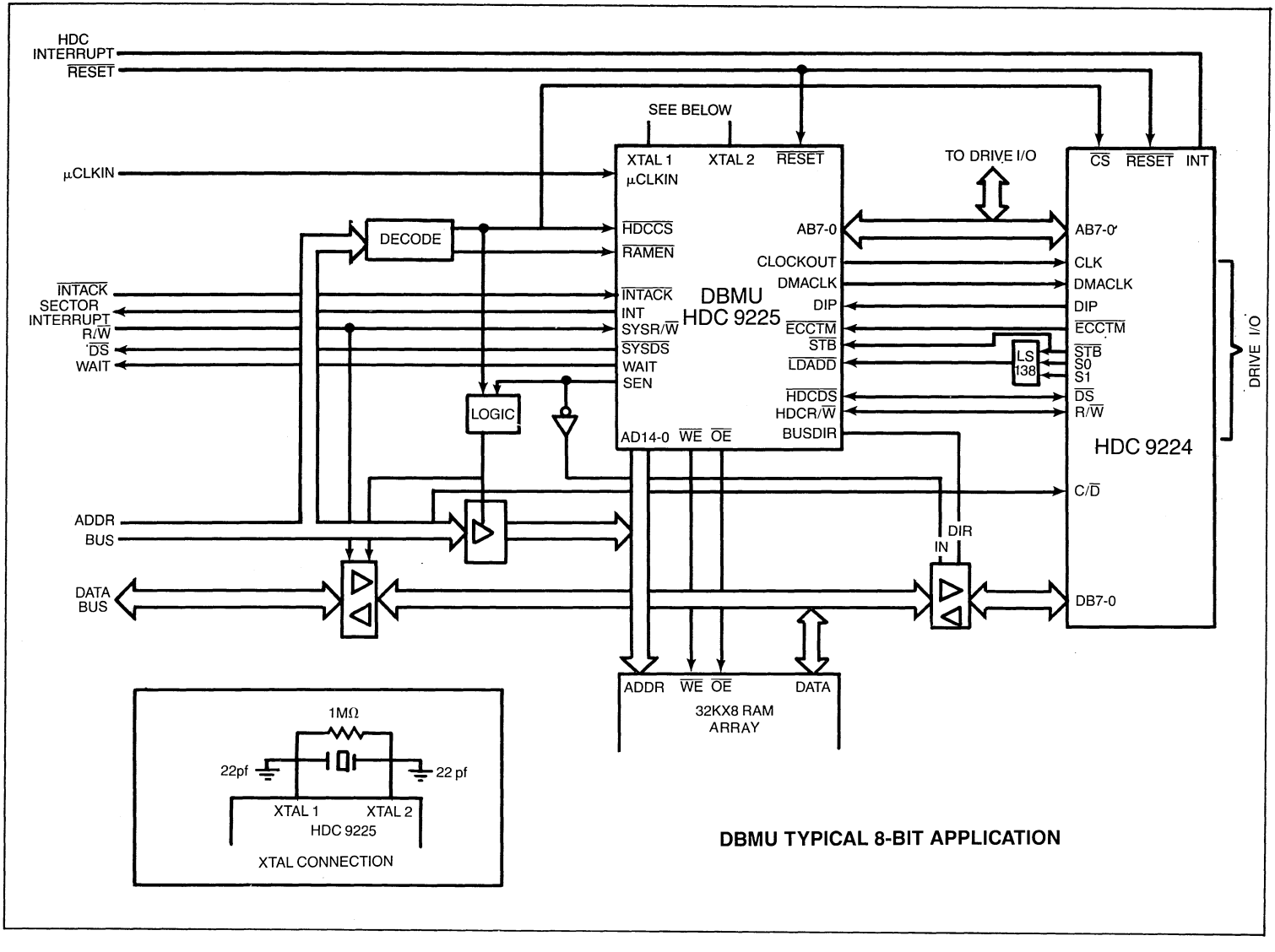

48 Pin DIP Package

## GENERAL DESCRIPTION

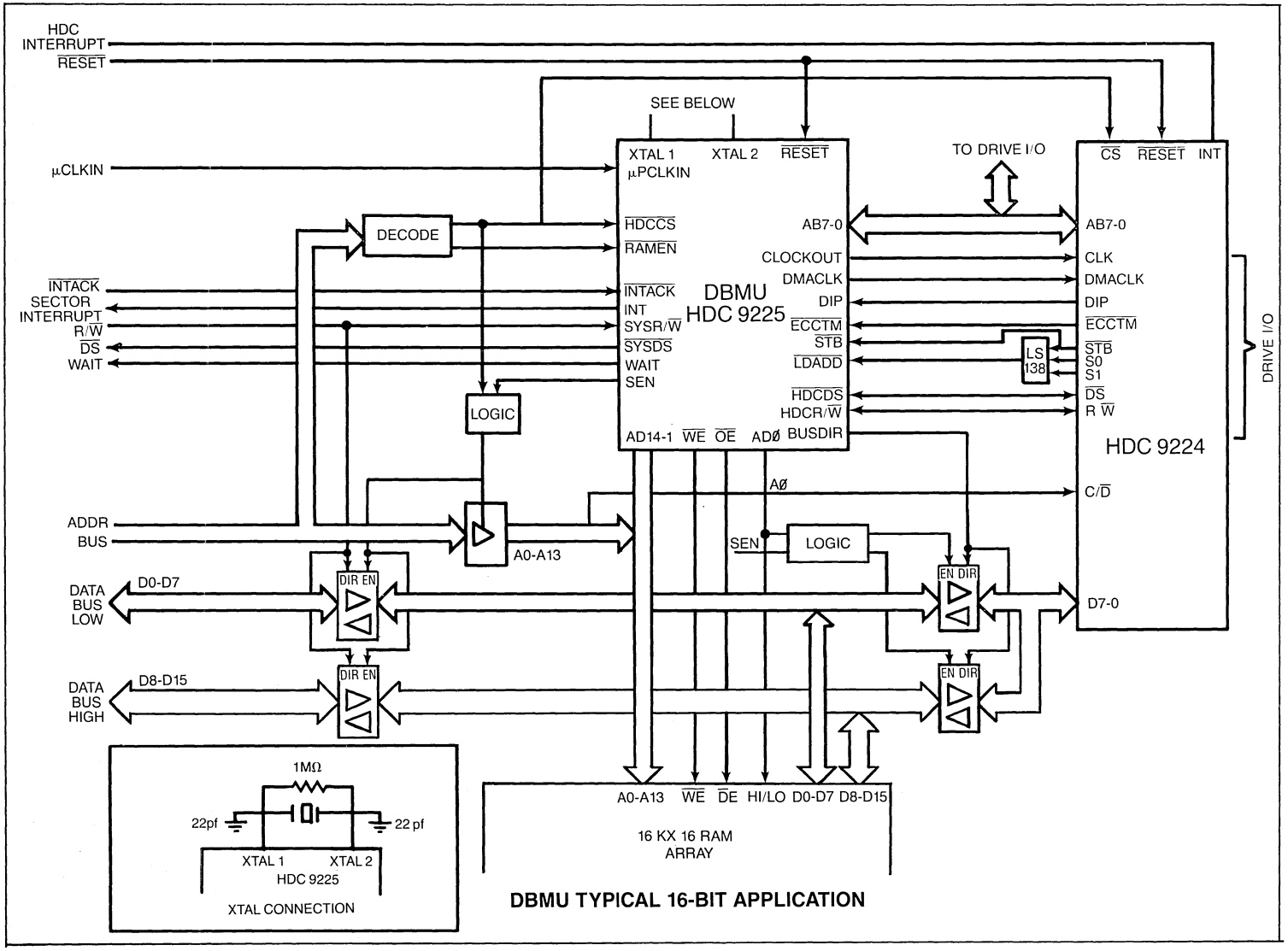
The HDC 9225 Disk Buffer Management Unit (DBMU) is a 48 pin CMOS/LSI device which, when used with the HDC 9224 Universal Disk Controller, significantly reduces the total number of chips required to build a hard and floppy disk controller.

The DBMU allows low cost static rams to be used in a dual-ported configuration. This allows both the system processor and the HDC 9224 Universal Disk Controller to share a common disk buffer local memory area, while eliminating system memory contention problems. This feature greatly improves overall system performance, while simplifying design.

SECTION VI




**DBMU TYPICAL 8-BIT APPLICATION**




**DBMU TYPICAL 16-BIT APPLICATION**

## DESCRIPTION OF PIN FUNCTIONS

| PIN. NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1, 2 | Crystal 1<br>Crystal 2 | XTAL 1<br>XTAL 2 | An external 10 MHz crystal is connected to these two pins. If an external 10 MHz TTL clock is used, it should be connected to XTAL 1 with a 300 ohm pull-up resistor and XTAL 2 left floating. |
| 34 | Processor Select of Hard Disk Controller | $\overline{\text{HDCCS}}$ | This input signal is generated by the host processor and informs the DBMU that the host processor wants to read or write to the HDC 9224. The processor should not access the HDC 9224 while it is executing a previous command. |
| 31 | RAM Enable | $\overline{\text{RAMEN}}$ | This input signal is generated by the host processor to indicate to the DMBU that it wants to access the dual ported ram buffer controlled by the DBMU. If the HDC 9224 is currently using the buffer, the WAIT signal will go active, forcing the host processor into a wait state. |
| 41 | Wait | WAIT | This output signal is used to wait-state the host processor when the HDC 9224 and the host processor attempt to access the disk buffer at the same time. |
| 37 | System Read/Write | SYSR/$\overline{\text{W}}$ | This input signal from the host processor is used for host processor read/write control of the HDC 9224 and the dual ported disk buffer. |
| 33 | HDC Read/Write | HDCR/$\overline{\text{W}}$ | This pin is used as both an input and output. When the host processor is either reading or writing to the HDC 9224, this pin outputs the signal presented on SYSR/$\overline{\text{W}}$. When the HDC 9224 is performing disk I/O, an input to this pin is used to generate the appropriate RAM control signal. |
| 39 | Output Enable | $\overline{\text{OE}}$ | This output is used to control the output enable lines of the memory used in the dual ported RAM disk buffer. |
| 29 | Strobe | $\overline{\text{STB}}$ | This input is connected to the Strobe output on the HDC 9224 and is used to decode the multiplexed Aux Bus. |
| 38 | Write Enable | $\overline{\text{WE}}$ | This output is used to control the write enable lines of the memory used in the dual ported RAM disk buffer. |
| 3 | ECC Time | $\overline{\text{ECCTM}}$ | This input pin serves a dual purpose. When the HDC 9224 is performing error correction, an active (low) input (from the HDC 9224) to this pin inhibits the internal address counters from incrementing. This allows the HDC 9224 to correct the error using read-modify-write cycles.<br>When the HDC 9224 is performing a multiple sector read operation, an active (low) input on this pin, and an active (low) input on the $\overline{\text{LDADD}}$ signal to the DBMU indicates that a good sector transfer has occurred. |
| 30 | System Data Strobe | $\overline{\text{SYSDS}}$ | This input signal is the data strobe generated by the system processor, and is used to synchronize all processor initiated memory cycles. This signal is passed through the DBMU to the HDC 9224 via $\overline{\text{HDCDS}}$ if the processor desires to read or write any of the HDC 9224 internal registers. |
| 35 | HDC Data Strobe | $\overline{\text{HDCDS}}$ | This bidirectional pin performs two functions. When the host processor is accessing the HDC 9224, this output is a "pass through" of the $\overline{\text{SYSDS}}$ input.<br>When the HDC is performing memory cycles this signal becomes an input and uses the $\overline{\text{DS}}$ signal from the HDC 9224 to generate the $\overline{\text{WE}}$ or $\overline{\text{OE}}$ signals to the buffer memory. |
| 24 | Ground | GND | System Ground |
| 4-7,<br>20-23 | Auxiliary Bus 7-0 | AB 7-0 | These 8 inputs are connected directly to the AB7-0 outputs of the HDC 9224. The HDC 9224 will initialize the DBMU's internal 15 bit counter at each disk sector boundary by loading the start address in a byte serial fashion (high order byte first). The information is accepted upon the $\overline{\text{LDADD}}$ signal going active (low). |
| 8-19,<br>25-27 | Address Bus 14-0 | AD 14-0 | During HDC 9224 memory cycles, these output pins point to the memory address for the data passing through the HDC 9224. This address is automatically incremented at the trailing edge of $\overline{\text{HDCDS}}$. This bus is in a high impedance state whenever the system processor is performing memory cycles or working with the internal registers of the HDC 9224. |
| 36 | DMA IN PROGRESS | DIP | This input is generated by the HDC 9224 and informs the DBMU that the HDC 9224 is about to perform a memory cycle. |

## DESCRIPTION OF PIN FUNCTIONS (continued)

| PIN. NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 43 | LOAD ADDRESS | $\overline{LDADD}$ | This input is used to clock the data (appearing on AB7-0) into the internal 15 bit address counter.<br>The HDC 9224 pulls this pin active (low) simultaneous with the $\overline{ECCTM}$ signal when a sector of valid data is in the buffer. The DBMU may be programmed to produce an interrupt on this condition. |
| 40 | CPU CLOCK IN | μCLKIN | This input should be connected to the CPU Clock and must be at least 4 MHz. |
| 48 | +5V | $V_{cc}$ | +5 Volts |
| 46 | Interrupt | INT | This output pin is used to interrupt the system processor. The DBMU may be programmed to produce this interrupt after a (programmed) number of sectors are successfully transferred through the DBMU. |
| 45 | Interrupt Acklowledge | $\overline{INTACK}$ | This input is generated by the processor when acknowledging a DBMU generated interrupt and will reset the INT output to its inactive (low) state. |
| 32 | Bus Direction | BUSDIR | This output signal controls the flow of data through an external bidirectional tristate bus driver. |
| 42 | System Bus Enable | SEN | This output enables the system processor data bus when the DBMU allows the processor access to the RAM buffer memory. |
| 28 | DMA Clock | DMACLK | This output signal normally runs at a frequency of 5 MHz and feeds the HDC 9224 to control the timing of all HDC 9224 memory cycles. When the HDC 9224 is accessing the RAM buffer, the low portion of this signal is stretched to slow down the HDC 9224 memory cycle and allow processor access to the RAM buffer. |
| 47 | Clock Out | CLOCK OUT | This pin provides the 10 MHz clock required by the HDC 9224. This signal conforms to the clock input specifications of the HDC 9224. |
| 44 | Reset | $\overline{RESET}$ | This input pin resets the DBMU into a known state. Additionally, the INT output is reset to logic 0. |

## DESCRIPTION OF OPERATION

### DBMU INTERRUPT GENERATION

The DBMU allows the system to empty the RAM buffer while the HDC 9224 is still filling the buffer. This can significantly improve system throughput. If the processor instructs the HDC 9224 to read multiple sectors (N) from the disk, the DBMU can be programmed to interrupt the processor after N sectors have been successfully transferred to the buffer.

The value (N) is loaded into the 3 least significant bits of the upper most DMA address register in the HDC 9224 (Write Register 2), and transferred to the DBMU when the DMA address is output by the HDC 9224. (This does not cause a conflict as the DBMU only uses the lower most 15 bits of address output by the HDC 9224).

After each successful sector transfer an internal counter (in the DBMU) is incremented, and when coincidence with N is met, the DBMU issues an interrupt to the system processor.

In the case when these 3 bits = "000", an interrupt is generated after each sector is successfully transferred. If these 3 bits = "111" then an interrupt is generated after every 8 sectors are transferred correctly.

### MEMORY CONTENTION

The DBMU serves as an arbitrator between the HDC 9224 and the system processor whenever both request access to the RAM buffer memory. The DBMU input $\overline{RAMEN}$ signals when the system processor needs access to the RAM buffer, while $\overline{HDCDS}$ indicates that the HDC 9224 needs access to the buffer.

During each byte transfer initiated by the HDC 9224, a window is set up which will allow processor cycles to occur. If $\overline{RAMEN}$ becomes active in this window, it will be granted immediate access to the buffer. Otherwise, the DBMU will put the processor in a wait state. This window is open for a certain percentage (described below) of every byte time, and will insure that at least one processor cycle is allowed per byte time.

When the HDC 9224 is not accessing the RAM buffer, the processor window is open 100% of the time. During multiple sector transfers from the HDC 9224, the window is open for 100% of the time between sectors.

During hard disk operations, where one byte time equals 1600 ns, the processor window is open for 500 ns during each byte time, except when the HDC 9224 is loading a new DMA start address to the DBMU. This normally only occurs on sector boundaries, and in these cases, the window is open for 400 ns.

For floppy disk operation, where byte times equal 16 us, 32 us, or 64 us, the window is open for approximately 75% of each byte time. Once again, when the HDC 9224 is loading a new DMA start address to the DBMU, this window time drops to 400 ns.

The window will be open 100% of the time following the successful transfer of a sector.

### WAIT OUTPUT TIMING

Due to the asynchronous nature of the $\overline{\text{RAMEN}}$ input with respect to the internal 10 MHz clock, the generation of WAIT may vary by approximately 50 ns. For this reason, the user has the option of selecting either an "early" WAIT or a "late" WAIT output. If "late" WAIT is selected, the WAIT signal will become active only if a wait state is needed and it will be synchronized to the 10 MHz internal clock.

If "early" WAIT is selected, the WAIT signal will be output for every $\overline{\text{RAMEN}}$ generated and if a wait state is not needed, the signal will be reset on the next rising edge of UPCLK. The selection of "early" or "late" WAIT is programmed via bit 3 of the most significant DMA Address byte (loaded into write register 2 of the HDC 9224.) When this bit is set to a logic 1, the "late" WAIT is selected, while if this bit is reset to a logic 0, an "early" WAIT is selected. (Upon RESET, "early" WAIT is selected.)

Note that when an HDC 9224 memory cycle is being performed, the DMACLK is always stretched—even if no contention exists. The DBMU address bus AD14-0 is put into the high impedance state when the output SEN is active and is incremented at the next rising edge of the $\overline{\text{HDCDS}}$ signal.

### SYSTEM TO HDC ACCESS

When the system processor wants to access the registers in the HDC 9224, it informs the DBMU via the $\overline{\text{HDCCS}}$ input. This input is simply a decode of the system processor address bus lines reserved for the HDC register addresses.

When this signal is active, the BUSDIR signal will be activated to the state which will direct data into or out of the HDC 9224 as of a function of the SYSR/$\overline{\text{W}}$ input. It should be noted that there is no way to produce wait states during system to HDC data transfers. Because of this, it is important to remember that the system must only access the HDC 9224 only after it receives an interrupt from the HDC 9224. This will ensure that all data transfers between the RAM buffer and the HDC have concluded as a result of the DONE bit (in the HDC 9224) being set.

---

### MAXIMUM GUARANTEED RATINGS

| | |
|---|---|
| Operating Temperature Range | 0 to 70 C |
| Storage Temperature Range | −55 C to +150 C |
| Lead Temperature (soldering, 10 sec) | +300 C |
| Positive Voltage on any Pin, with respect to Ground | +7 V |
| Negative Voltage on any Pin, with respect to Ground | −0.3 V |

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

## DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, $V_{CC}$ = 5.0V, ± 5%)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

| Parameter | Min. | Max. | Units | Comments |
|---|---|---|---|---|
| SUPPLY CURRENT | | | | |
| $I_{CC}$ | | 20 | mA | |
| OUTPUT VOLTAGE | | | | |
| $V_{OH}$ (1) | 2.4 | | V | $I_{OH}$ = 400 uA |
| $V_{OH}$ (2) | 4.3 | | V | $I_{OH}$ = 400 uA (DMACLK and CLKOUT only) |
| $V_{OL}$ (1) | | 0.4 | V | $I_{OH}$ = 2 mA for outputs except SEN |
| $V_{OL}$ (2) | | 0.4 | V | $I_{OH}$ = 4 mA for SEN |
| INPUT VOLTAGE | | | | |
| $V_{IH}$ | 2.0 | | V | |
| $V_{IL}$ | | 0.8 | V | |
| INPUT CURRENT | | | | |
| $I_{IH}$ | | 10 | uA | $V_{IH}$ = 2.0V |
| $I_{IL}$ | | 10 | uA | $V_{IL}$ = 0.8V |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## AC ELECTRICAL CHARACTERISTICS (TA = 0 C to +70 C, $V_{CC}$ = 5.0V, ± 5%)

| Symbol | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| $T_{PD1}$ | | | 60 | ns | CL = 15pf; figure 1a |
| $T_{PD2}$ | | | 130 | ns | CL = 15pf; figure 1b |
| $T_{PD3}$ | | | 70 | ns | CL = 15pf; figure 2 |
| $T_{PD4A}$ | | | 60 | ns | CL = 15pf; figure 3 |
| $T_{PD4B}$ | | | 45 | ns | CL = 15pf; figure 3A |
| $T_{PD5A}$ | | | 50 | ns | CL = 15pf; figure 4 |
| $T_{PD5B}$ | | | 40 | ns | CL = 15pf; figure 4A |
| $T_{PD6A}$ | | | 60 | ns | CL = 15pf; figure 4A |
| $T_{PD6B}$ | | | 45 | ns | CL = 15pf; figure 4 |
| $T_{PD7}$ | | | 100 | ns | CL = 30pf; figure 5 |
| $T_{ZX}$ | | 18 | 45 | ns | CL = 30pf; figure 6 |
| $T_{XZ}$ | | 18 | 45 | ns | CL = 30pf; figure 6 |
| $T_{PD8}$ | | | 40 | ns | CL = 15pf; figure 7 |
| $T_{PD9}$ | | | 40 | ns | CL = 25pf; figure 8 |
| $T_{PD10}$ | | | 45 | ns | CL = 25pf; figure 8 |
| $T_{PD11}$ | | | 40 | ns | CL = 15pf; figure 9 |
| $T_{PD12}$ | | | 100 | ns | CL = 15pf; figure 10 |
| $T_{PD13}$ | | | 40 | ns | CL = 15pf; figure 11 |
| $T_{PD14}$ | | | 50 | ns | CL = 15pf; figure 12 |
| $T_{PD15}$ | | | 50 | ns | CL = 15pf; figure 12 |
| $T_{PD16}$ | | | 55 | ns | CL = 15pf; figure 12 |
| $T_{PD17}$ | | | 45 | ns | CL = 15pf; figure 12 |
| $T_{PD18}$ | | 20 | 50 | ns | CL = 10pf; figure 13 |
| $T_{PD19}$ | | 20 | 50 | ns | CL = 10pf; figure 13 |
| $T_{PD20}$ | | 10 | 40 | ns | CL = 30pf; figure 13 |
| $T_{PD21}$ | | 10 | 40 | ns | CL = 30pf; figure 13 |
| $T_{W1}$ | 150 | | | ns | Figure 14 |
| $T_{W2}$ | 300 | | | ns | Figure 14 |
| $T_{W3}$ | 500 | | | ns | Figure 15 |
| $T_{W4}$ | 500 | | | ns | Figure 15 |
| $T_{W5}$ | 650 | | | ns | Figure 16 |
| $T_{W6}$ | 650 | | | ns | Figure 16 |
| $T_{W7}$ | 100 | | | ns | Figure 17 |
| $T_{P}$ | 100 | | | ns | Figure 18 |
| $T_{CH}$ | 50 | | | ns | Figure 18 |
| $T_{CL}$ | 50 | | | ns | Figure 18 |
| $T_{SL}$ | 50 | | | ns | Figure 19 |
| $T_{HL}$ | 50 | | | ns | Figure 19 |
| $T_{S2}$ | 50 | | | ns | Figure 19 |
| $T_{H2}$ | 50 | | | ns | Figure 19 |
| $T_{W8}$ | 200 | | | ns | Figure 20 |
| $T_{W9}$ | | 750 | | ns | Figure 21 |

Note: All propagation delays are measured from the 1.5V level of the input signal to the 1.5V level of the output

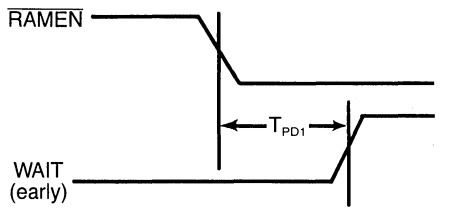



FIGURE 1A

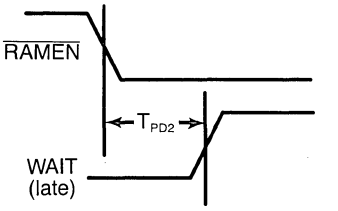



FIGURE 1B

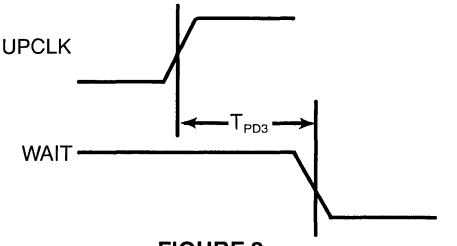



FIGURE 2

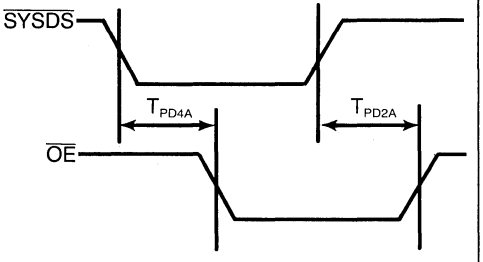



FIGURE 3A

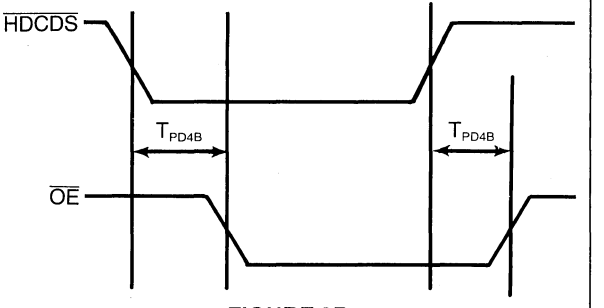



FIGURE 3B

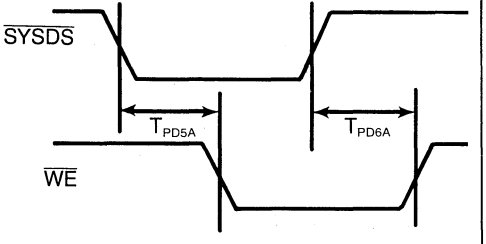



FIGURE 4A

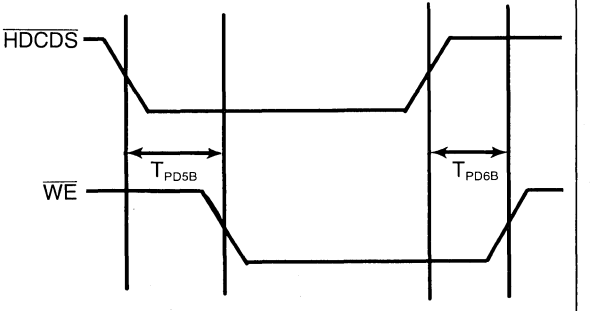



FIGURE 4B

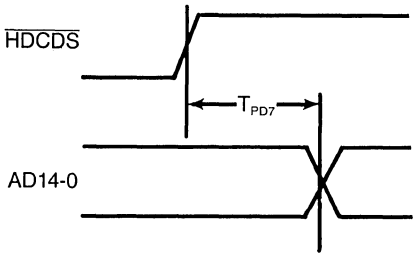



FIGURE 5

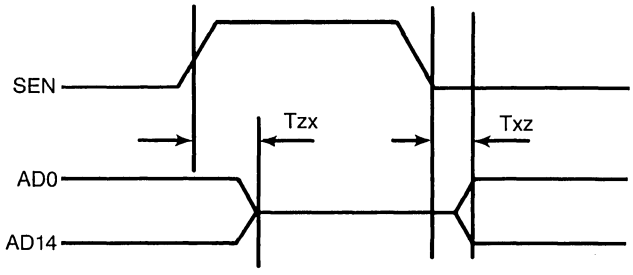



FIGURE 6

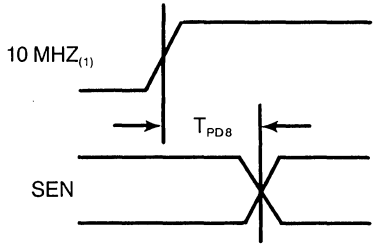



FIGURE 7

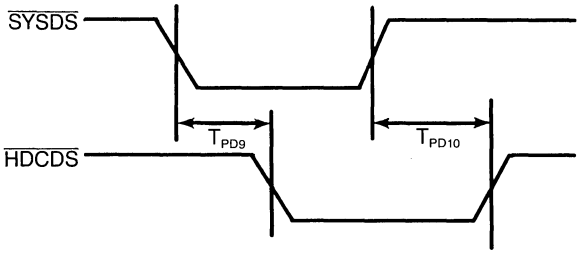



FIGURE 8

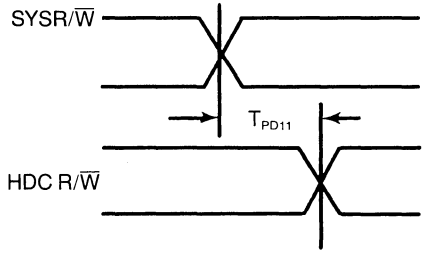



FIGURE 9

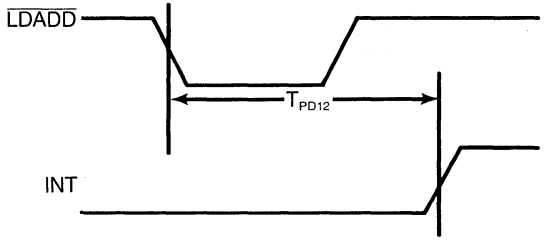



FIGURE 10

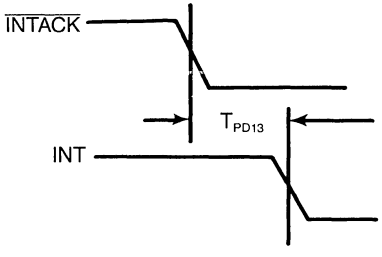



FIGURE 11

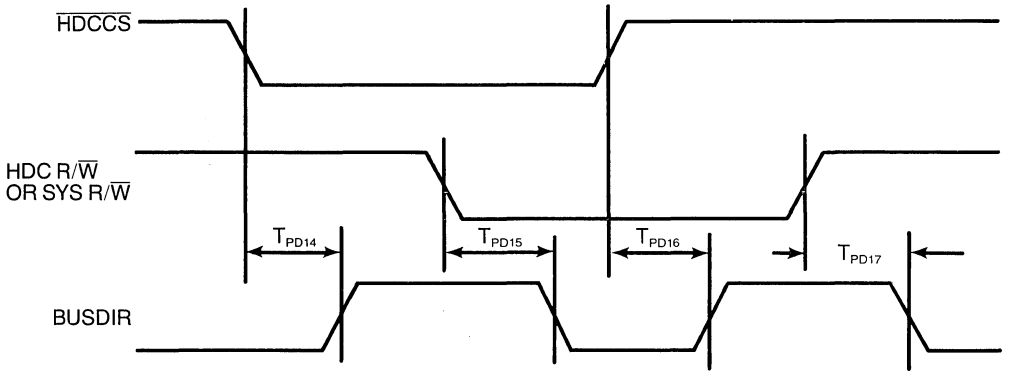



**FIGURE 12**

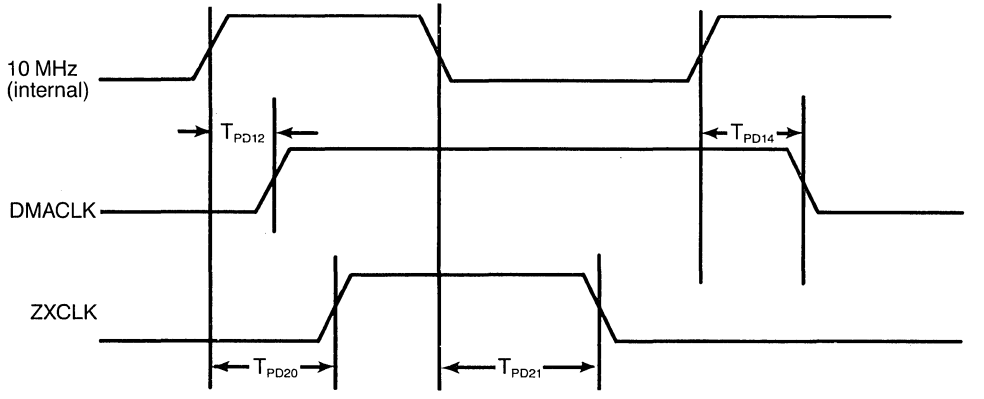



**FIGURE 13**

Note: all measurements referenced to the 1.5V level.

**FIGURE 14**

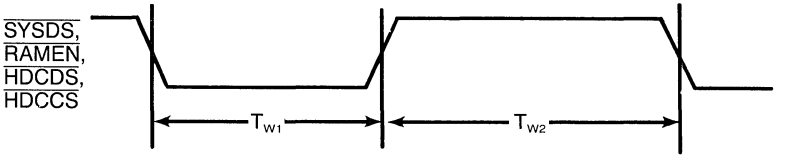



**FIGURE 15**

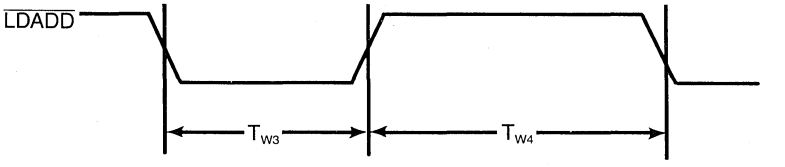
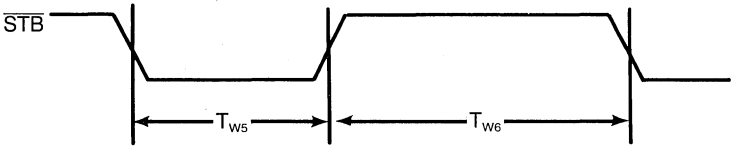



**FIGURE 16**



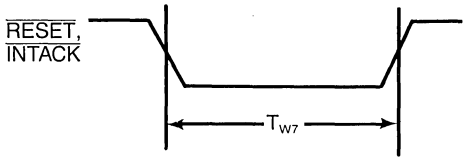



FIGURE 17

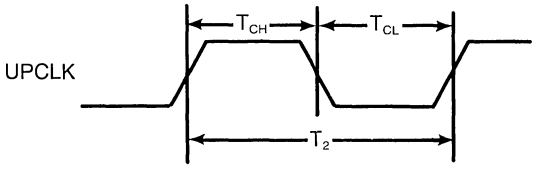



FIGURE 18

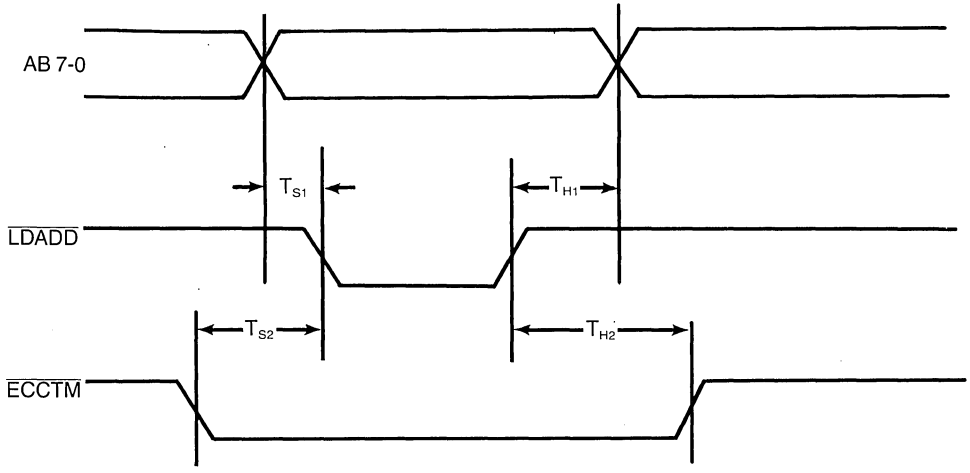



FIGURE 19

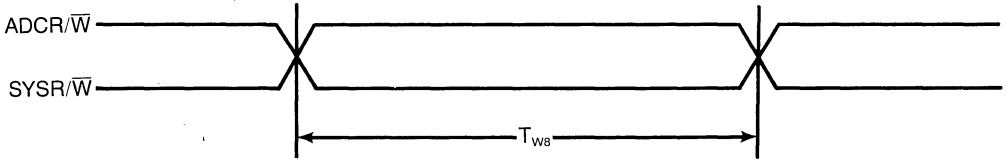



FIGURE 20

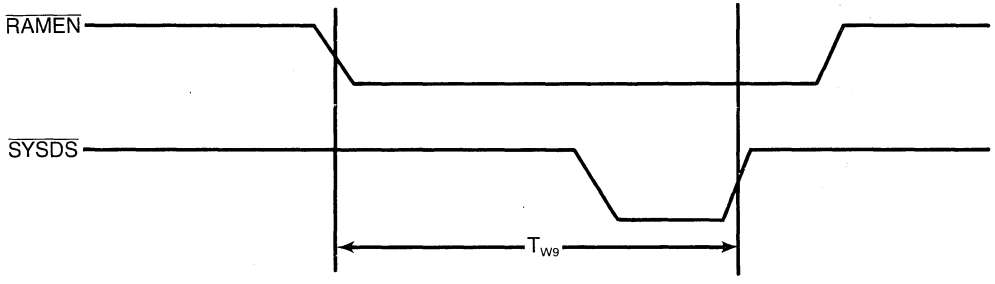



FIGURE 21

SECTION VI

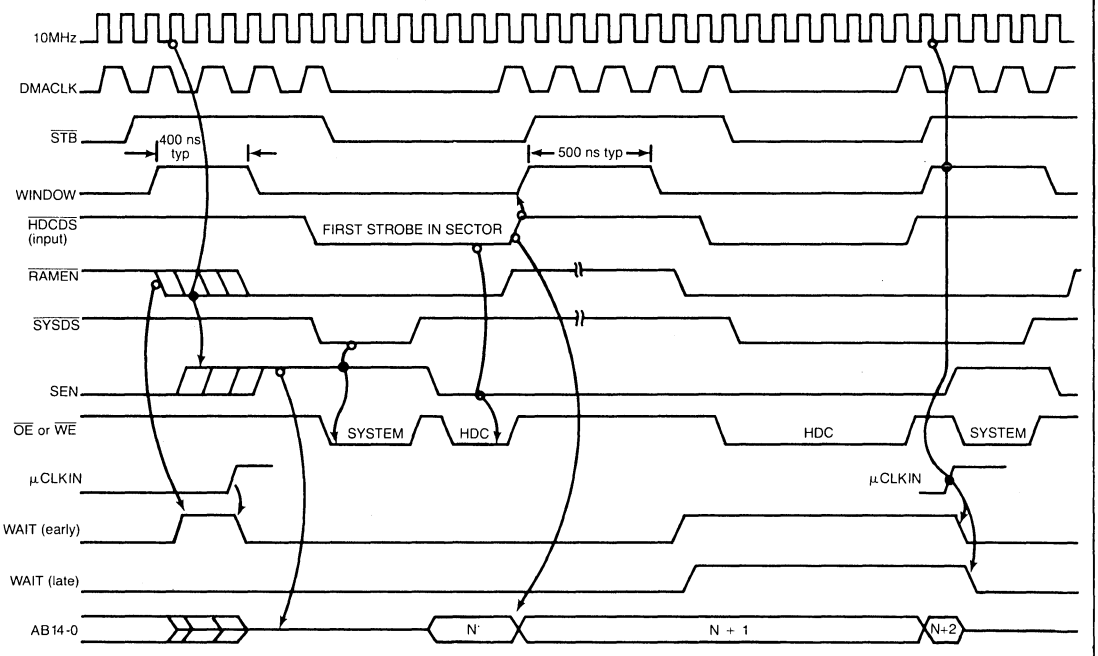



**FIGURE A–PROCESSOR + HDC9224 CONTENTION TIMING FOR HARD DISK**

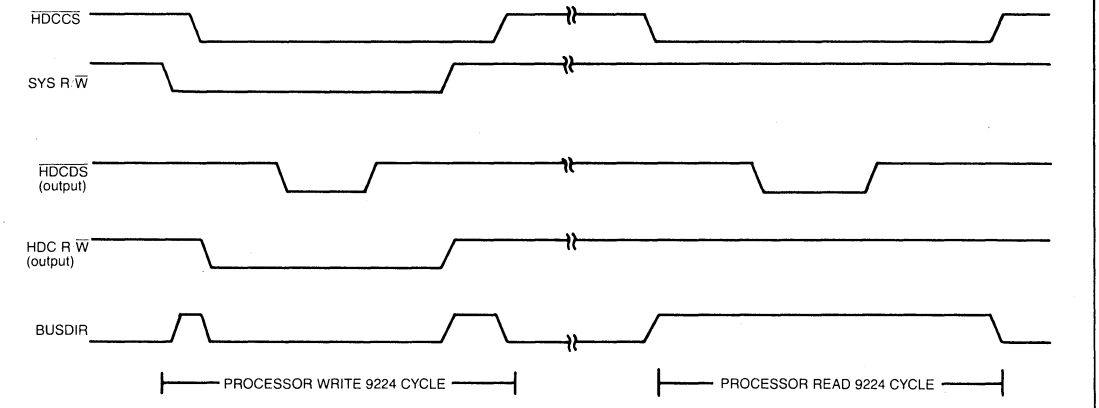



**FIGURE B–PROCESSOR TO 9224 ACCESS CYCLES**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

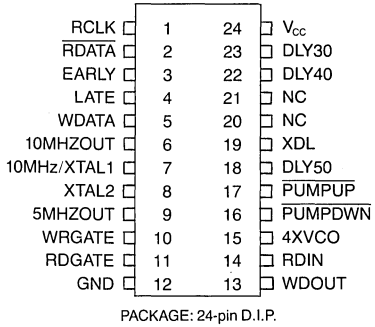
# HDC 9226

# HIGH PERFORMANCE HARD DISK DATA SEPARATOR "HDDS"

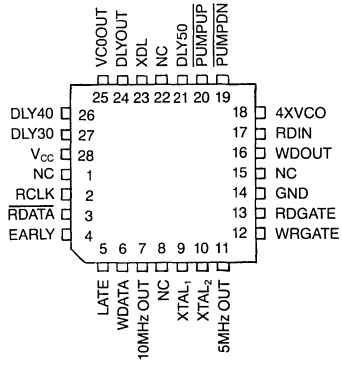
## FEATURES

- ☐ Significantly reduces component count in hard disk systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- ☐ Built-in write precompensation logic
- ☐ Eliminates costly critical "tune up" adjustments
- ☐ Space saving 24 pin package saves board space and reduces critical layout problems.
- ☐ Printed Circuit Board Artwork available to facilitate prototyping and evaluation

## PIN CONFIGURATION




PACKAGE: 24-pin D.I.P.



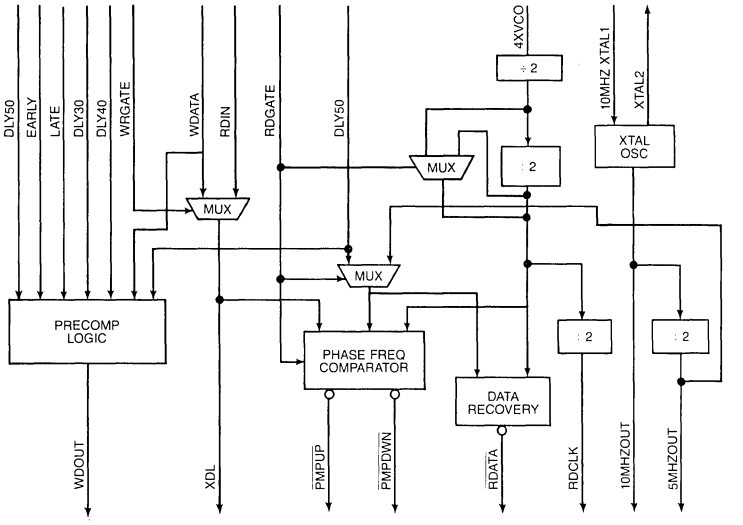

PACKAGE: 28-pin PLCC

## GENERAL DESCRIPTION

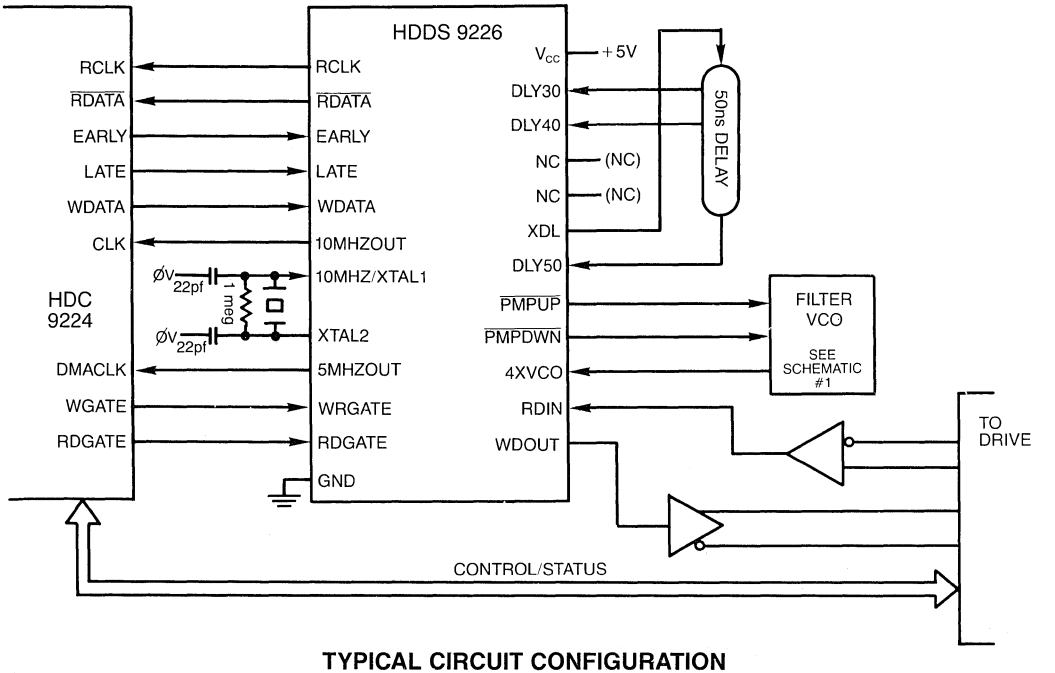
The HDC 9226 Hard Disk Data Separator (HDDS) is a 24 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of a high performance hard disk data separator.

The HDC 9226, combined with a few discrete components, form a phase locked loop which performs phase and frequency locking onto either the FM or MFM data stream output by ST506/ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9226 simplifies the task of the designer.




**HDC 9226**
**BLOCK DIAGRAM**




**TYPICAL CIRCUIT CONFIGURATION**

## DESCRIPTION OF PIN FUNCTIONS

| PIN. NO. | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | Read Clock | RCLK | Read clock output with nominal frequency of 5 MHz which defines the half bit boundaries of the $\overline{\text{RDATA}}$ output. |
| 2 | Read Data | $\overline{\text{RDATA}}$ | This output is the regenerated raw read data from the drive. This signal conforms to all timing requirements of the UDC. |
| 3 | Early | EARLY | This input is connected to the HDC 9224, and causes the HDDS to send out the write data early. |
| 4 | Late | LATE | This input is connected to the HDC 9224, and causes the HDDS to send out the write data late. |
| 5 | Write Data | WDATA | This input is connected to the HDC 9224, and is the MFM encoded write data signal. This signal is passed through the HDDS and is delayed according to the write precompensation inputs EARLY and LATE. |
| 6 | 10 Mhz Out | 10MHZOUT | This output is normally connected to the CLK input on the HDC 9224. |
| 7, 8 | Crystal 1, 2 | XTAL 1,2 | A 10 Mhz crystal may be connected between these two inputs. If a TTL signal is used in place of a crystal, the TTL signal (with pullup) should be connected to the XTAL 1 and the XTAL 2 input should be left open. |
| 9 | 5 Mhz Out | 5MHZOUT | This output is normally tied to the HDC 9224 DMACLK pin in systems that do not use the HDC 9225 Disk Buffer Management Unit. |
| 10 | Write Gate | WRGATE | This input is connected to the WRGATE output of the HDC 9224. When low the RDIN input is selected and is output to the delay line via the XDL pin. When in write mode (WRGATE active), the WDATA input is selected and output to the delay line via the XDL pin for precompensation. |
| 11 | Read Gate | RDGATE | This input signal, when active, allows the external VCO to begin locking on the incoming data from the drive. When this signal is inactive, the VCO will lock on to the 5 MHz output signal. |
| 12 | Ground | GND | This is the ground pin for the device |
| 13 | Write Data Out | WDOUT | This output is the precompensated version of the WDATA input. This output is normally connected to the write data signal of the hard disk drive. |
| 14 | Read Data In | RDIN | This input is normally connected to the Disk Data output of the drive. The leading edge of this input arms the internal phase comparator, and then also asserts the $\overline{\text{PMPUP}}$ output 50 ns later. |
| 15 | 4 Times VCO | 4XVCO | This input is connected to the external VCO and runs at a frequency of 4 times the data rate with RDGATE asserted. This signal is internally divided by 2 and feeds the phase comparator to generate the $\overline{\text{PMPDN}}$ signal. 4XVCO is also divided by four and output as the RCLK signal. |
| 16 | Pump Down | $\overline{\text{PMPDN}}$ | When active (low) this output will decrease the frequency of the VCO. |
| 17 | Pump Up | $\overline{\text{PMPUP}}$ | When active (low) this output will increase the frequency of the VCO. |
| 18 | Delay 50 ns | DLY50 | This is the 50 ns delay of the XDL signal. The 50 ns tap is used to arm the phase detector and create a reclocked version of the raw read data from the drive. |
| 19 | Excite Delay Line | XDL | During write operations, when WRGATE is active, this output is identical to WDATA, and is output to the delay line, creating precise delays which are used to perform write precompensation. When WRGATE is inactive, this output is the image of the raw read data the RDIN input. XDL is output to the delay line and is used to provide proper arming for the phase comparator and clocking for the data recovery circuitry. |
| 20, 21 | No Connect | NC | No connection should be made to these pins. |
| 22<br>23 | Delay 40<br>Delay 30 | DLY40<br>DLY30 | These inputs are delays of 30 and 40 ns of the XDL signal, and come from the external delay line. These signals are used for the nominal, late and early positioning of the databits in the WDOUT data stream. |
| 24 | $V_{CC}$ | $V_{CC}$ | +5V supply connected to this pin. |

## DESCRIPTION OF OPERATION

### DATA SEPARATION

The HDC 9226, in conjunction with an external VCO, tapped delay line and filter, allows the system designer to implement a high performance phase locked loop circuit to perform phase and frequency locking onto either an MFM or FM encoded data stream (from an ST-506 style disk drive.)

In most applications, the data on the hard disk is recorded in double density (MFM). In MFM mode, an input pulse on RDIN indicates not a 1 or 0 but rather a flux transition on the media and (by definition) these flux transitions may be spaced at T, 1.5T or 2T time intervals, where T equals the inverse of the bit data rate. For the standard ST-506 drive, these time intervals are 200 ns, 300 ns, and 400 ns.

Due to the nature of magnetic storage phenomena, the bit spacing found on the hard disk is not constant, but instead will modulate due to magnetic effects and drive rotational speed variations. The HDC 9226 compensates for these shifts in the RDIN signal coming from the drive and regenerates $\overline{\text{RDATA}}$ and RCLK.

The RCLK signal is derived from the VCO which changes its period as a function of the variations in the raw disk data and permits the data from the drive to be correctly clocked into the HDC 9224 Universal Disk Controller, independent of the bit spacing variations found in the raw data coming from the drive.

The VCO nominally runs at 20 Mhz. Since the half bit time (for data from the disk) is 100 ns, the HDC 9226 divides the 4XVCO signal in half and compares the phase and frequency of the VCO with the incoming data. The read data signal is regenerated by the HDC 9266 and is placed correctly within the RCLK window so as to satisfy the input timing requirements of the HDC 9224 Universal Disk Controller.

### WRITE PRECOMPENSATION GENERATOR

The HDC 9226 also performs write precompensation which is needed because of tendency of written data to "re-align" itself on the magnetic media.

Certain bit patterns, when written, and later read back, will cause a phenomena known as "peak" or "bit" shift. Since this shifting is predictable, it is common when writing to magnetic media to intentionally pre-shift when these bits are to be written. This intentional "pre-shifting" minimizes the amount of shifting which occurs when the data is read back, and facilitates proper data recovery.

The HDC 9224 recognizes those patterns which require "pre-shifting" or precompensation, and outputs EARLY and LATE signals to alert the HDC 9226 to the need for precompensation.

Typical ST-506 applications may require "pre-shifting" the data bits by approximately 10 ns (either early or late). Three taps of the delay line (DLY30, DLY40, DLY50) are normally used to implement precompensation. The HDC 9226 then outputs the precompensated data via the WDOUT pin.

### PERFORMANCE SPECIFICATIONS

Complete performance specifications and specification definitions are contained in Technical Note 6-4, which is available from SMC Sales Offices and sales representatives. Technical Note 6-4 also contains full size PC board drawings and a complete bill of materials, useful in the prototyping of designs using the HDC 9226.

**MAXIMUM GUARANTEED RATINGS**

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec) ..... +325 C
Positive Voltage on any Pin, with respect to Ground ..... $V_{CC}$ + 0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5 V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**DC ELECTRICAL SPECIFICATIONS** (TA = 0 C to 70 C, $V_{CC}$ = 5.0V, ± 5%)

| Parameter | Min. | Max. | Units | Comments |
|---|---|---|---|---|
| SUPPLY CURRENT | | | | |
| $I_{CC}$ | | 30 | mA | |
| OUTPUT VOLTAGE | | | | |
| $V_{OH}$ (1) | 2.4 | | V | $I_{OH}$ = 400 uA |
| $V_{OH}$ (2) | 4.3 | | V | $I_{OH}$ = 400 uA |
| $V_{OL}$ | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| INPUT VOLTAGE | | | | |
| $V_{IH}$ (3) | 2.0 | | V | |
| $V_{IL}$ (3) | | 0.8 | V | |
| $V_{IH}$ (4) | 3.5 | | V | |
| $V_{IL}$ (4) | | 1.5 | V | |
| INPUT CURRENT | | | | |
| $I_{IH}$ | | 10 | uA | $V_{IH}$ = 2.0V |
| $I_{IL}$ | | 2.0 | mA | $V_{IL}$ = 0.4V |

Notes:
(1) For all outputs except 10MHzOUT and 5MHzOUT
(2) For 10MHzOUT and 5MHzOUT
(3) For all inputs except XTAL 1 and 4XVCO
(4) For XTAL1 and 4XVCO

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**AC ELECTRICAL CHARACTERISTICS** (TA = 0 C to +70 C, $V_{CC}$ = 5.0V, ± 5%)

| Symbol | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| $T_1$ | | | 70 | ns | figure 1 |
| $T_2$ | | | 80 | ns | figure 1 |
| $T_3$ | | | 65 | ns | figure 2 |
| $T_4$ | | | 70 | ns | figure 2 |
| $T_5$ | | | 100 | ns | figure 3 |
| $T_6$ | | | 100 | ns | figure 3 |
| $T_7$ | | | 35 | ns | figure 4 |
| $T_8$ | | | 35 | ns | figure 4 |
| $T_9$ | | | 60 | ns | figure 4 |
| $T_{10}$ | | | 70 | ns | figure 4 |
| $T_{11}$ | | | 65 | ns | figure 5 |
| $T_{12}$ | | | 65 | ns | figure 5 |
| $T_{13}$ | | | 65 | ns | figure 5 |
| $T_{14}$ | | | 65 | ns | figure 5 |
| $T_{15}$ | | | 45 | ns | figure 6 |
| $T_{16}$ | | | 45 | ns | figure 7 |
| $T_{17}$ | | | 45 | ns | figure 8 |
| $T_{18}$ | 45 | 50 | 55 | ns | figure 9 |
| $T_{19}$ | | 50 | | ns | figure 10 |
| $T_{20}$ | | 50 | | ns | figure 11 |
| $T_{21}$ | 6 | | | ns | figure 12 |
| $T_{22}$ | 50 | | | ns | figure 12 |

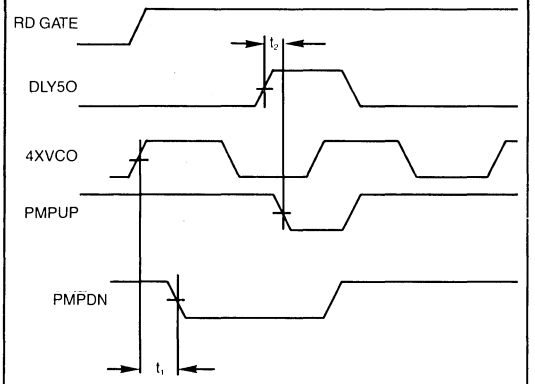



**FIGURE 1**

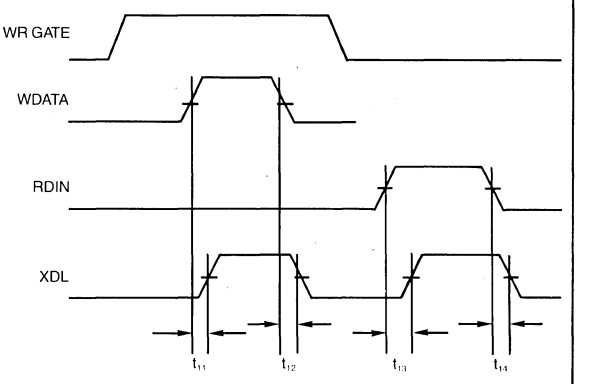



**FIGURE 5**

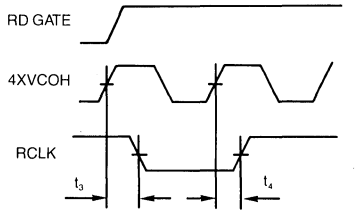



**FIGURE 2**

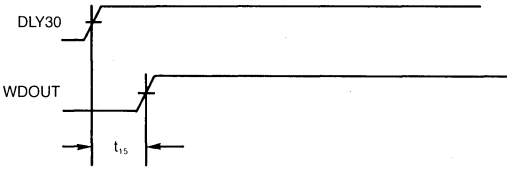



**FIGURE 6**

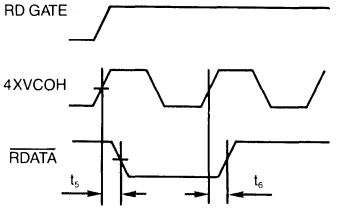



**FIGURE 3**

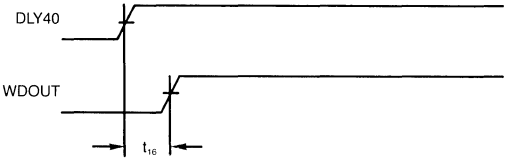



**FIGURE 7**

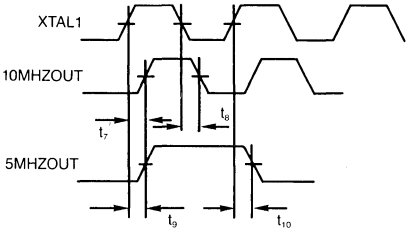



**FIGURE 4**

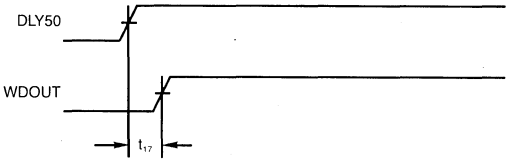



**FIGURE 8**

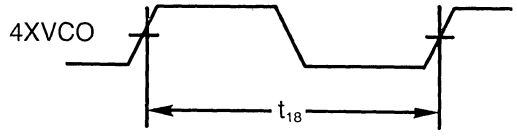



FIGURE 9

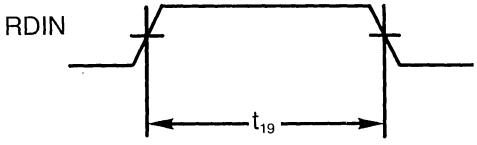



FIGURE 10

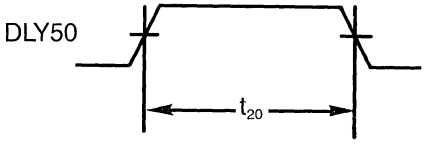



FIGURE 11

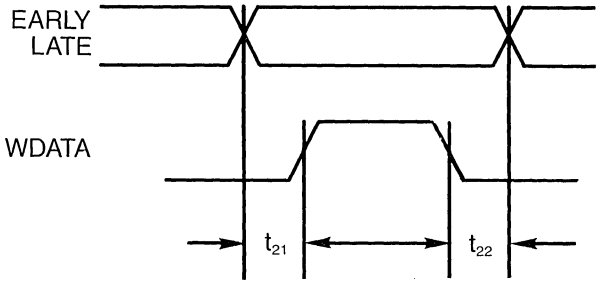
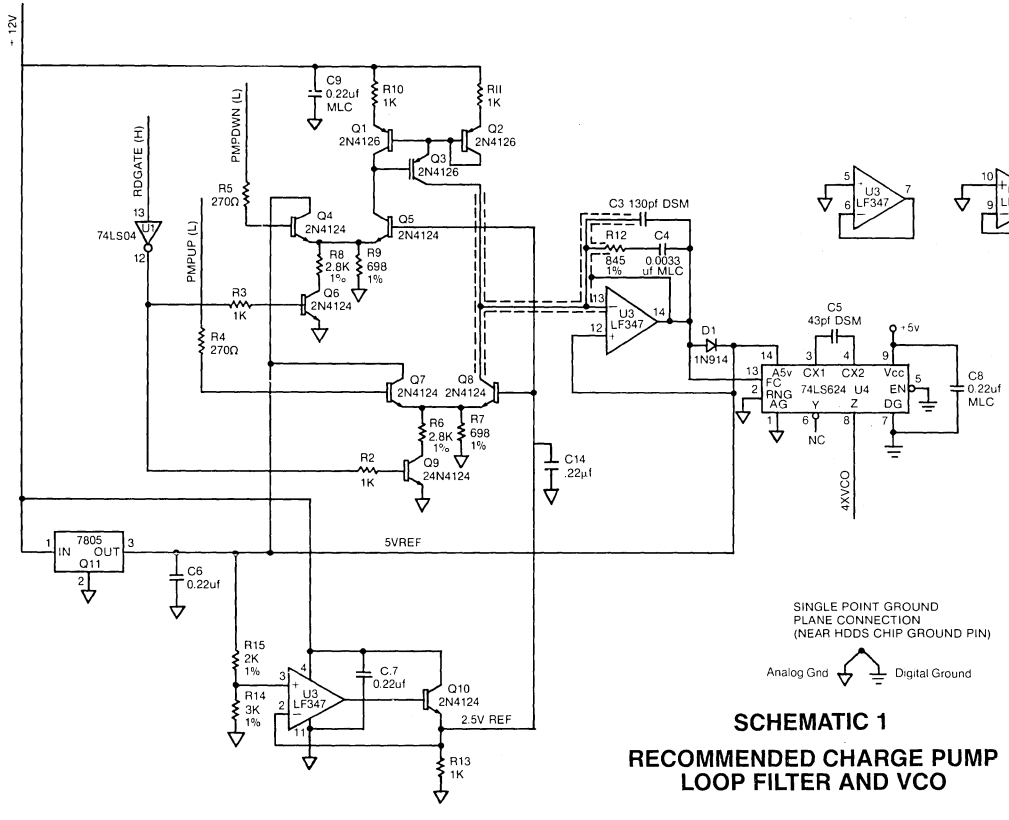



FIGURE 12

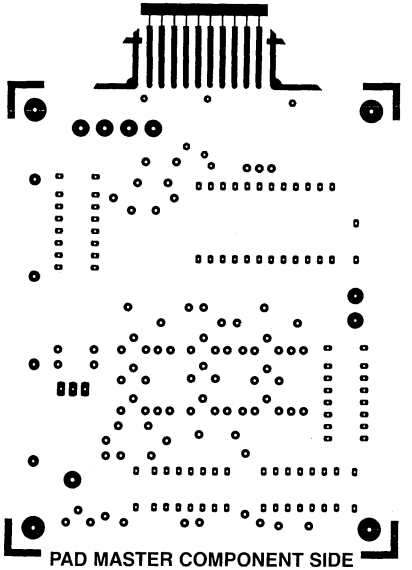



**SCHEMATIC 1**

**RECOMMENDED CHARGE PUMP LOOP FILTER AND VCO**

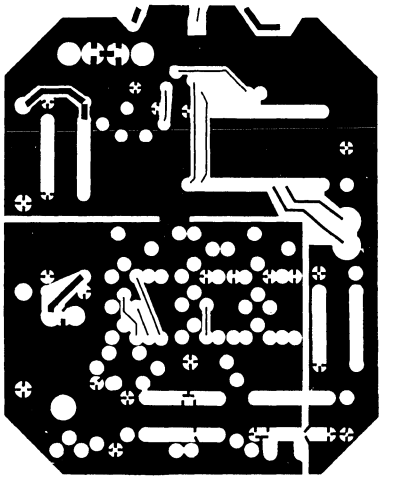
SECTION VI

PC 1



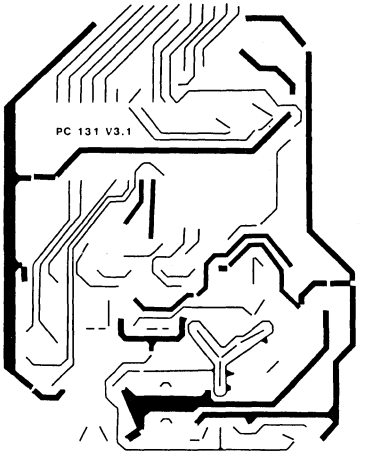
PAD MASTER COMPONENT SIDE

PC 2



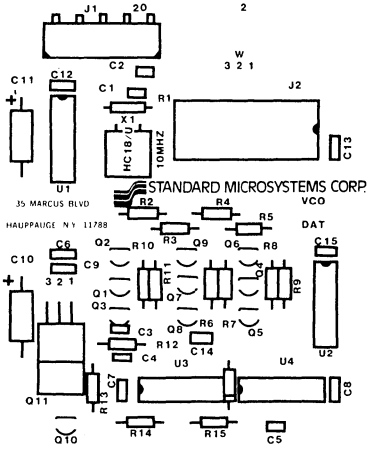
COMPONENT SIDE

PC 3




CIRCUIT SIDE

PC 4




SILK SCREEN

NOTE: The printed circuit board artwork shown above is included for illustration only. Camera ready artwork is available at no charge. Contact your SMC representative or regional sales office, and ask for Technical Note TN 6-4.

Blank PC boards (based on the illustrations above) are also available to facilitate evaluation and design. Contact your SMC representative or regional sales office for more information.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

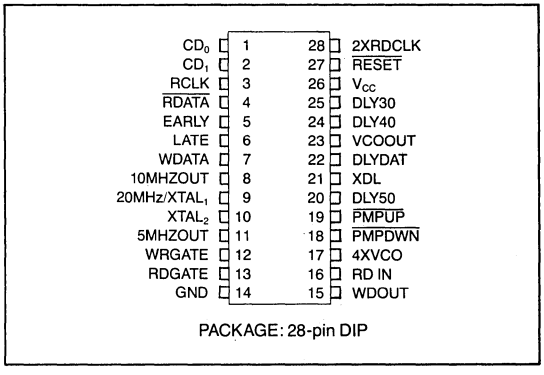
**HDC 9227**
**PRELIMINARY**

# High Performance Dual (Hard/Floppy Disk) Data Separator DDS

## FEATURES

- ☐ Single chip combines high performance analog hard disk data separator and high resolution digital floppy disk data separator
- ☐ Significantly reduces component count in hard disk and floppy systems
- ☐ Completely compatible with the HDC 9224 Universal Disk Controller
- ☐ Eliminates all tuning and tweaking normally required by analog data separators
- ☐ Built-in hard disk write precompensation logic
- ☐ Fabricated in CMOS technology
- ☐ Single +5V supply
- ☐ TTL Compatible

## PIN CONFIGURATION




PACKAGE: 28-pin DIP

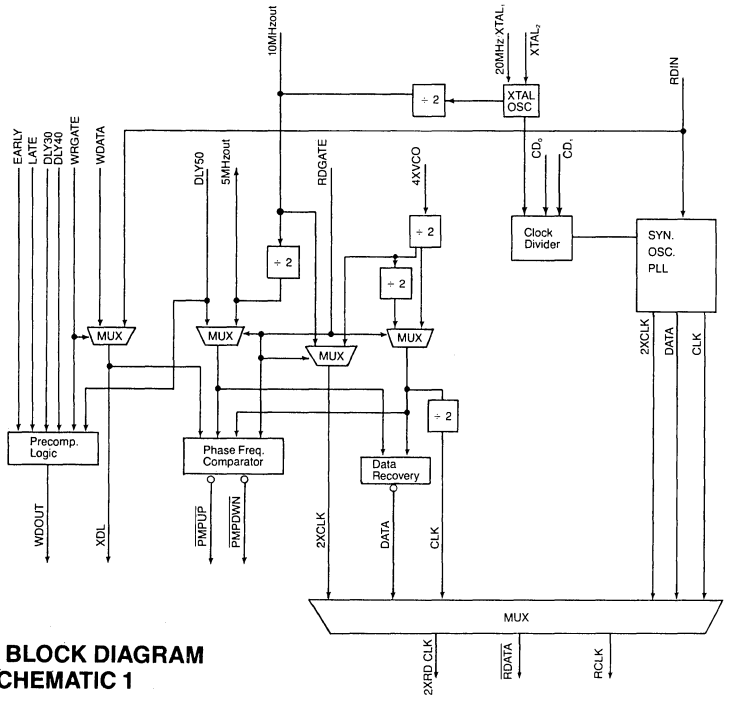
SECTION VI

## GENERAL DESCRIPTION

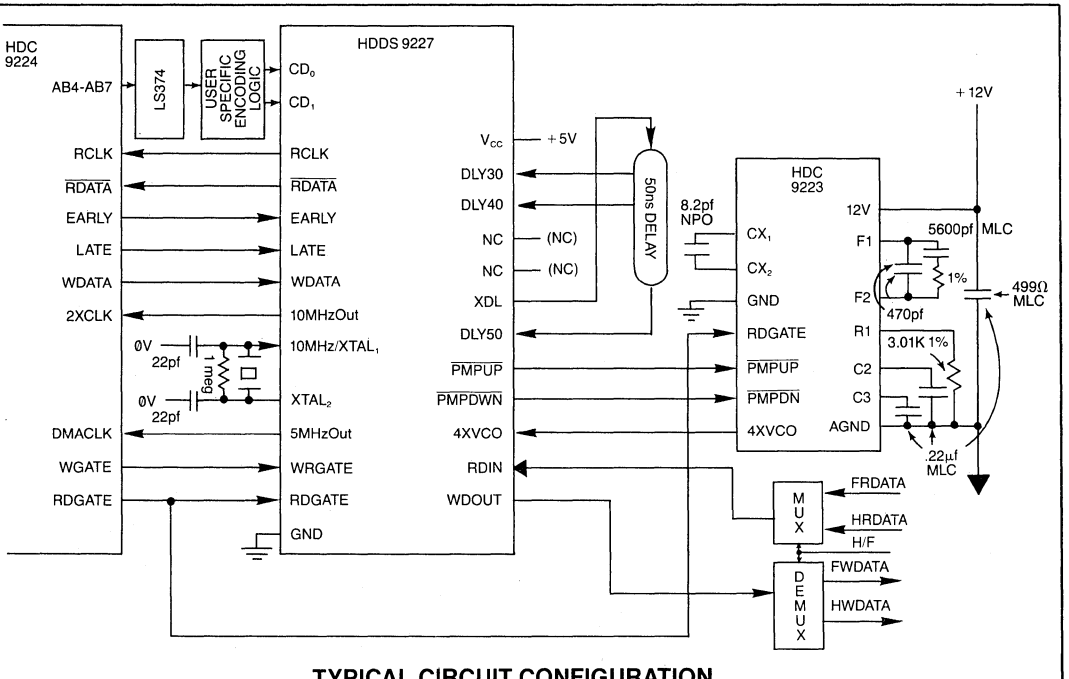
The HDC 9227 Universal Disk Data Separator (UDDS) is a 28 pin CMOS/LSI device, which when used with the HDC 9224 Universal Disk Controller significantly simplifies the design of the hard disk/floppy disk sub-system.

Internally, a precision floppy disk digital data separator is combined with the digital portion of a high performance, self tuning analog hard disk data separator.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9227 simplifies the task of the system designer.




**HDC 9227 BLOCK DIAGRAM**
**SCHEMATIC 1**




**TYPICAL CIRCUIT CONFIGURATION**
**SCHEMATIC 2**

## DESCRIPTION OF PIN FUNCTIONS

| PIN # | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1, 2 | CLOCK DIVISOR 0 AND 1 | $CD_0$, $CD_1$ | $CD_0$ and $CD_1$ control the internal clock divider circuit and hard/floppy mode. See table 1. |
| 3 | READ CLOCK | RCLK | For hard disks this clock has a nominal frequency of 5 MHz and defines the half bit boundaries of the RDATA output. For floppy disks it is the clock derived from the floppy disk drive serial bit stream. |
| 4 | READ DATA | $\overline{RDATA}$ | This output is a regenerated version of the raw read data from the drive, either hard or floppy, which satisfies the timing of the HDC 9224. |
| 5 | EARLY | EARLY | This input is generated by the Hard Disk Controller. In the hard disk mode it causes the data separator to output WDOUT early with respect to WDATA. In the floppy mode this input has no effect, as floppy precompensation is provided by the HDC 9224. |
| 6 | LATE | LATE | This input is generated by the Hard Disk Controller. In the hard disk mode it causes the data separator to output WDOUT late with respect to WDATA. In the floppy mode this input has no effect, as floppy precompensation is provided by the HDC 9224. |
| 7 | WRITE DATA | WDATA | This input is the write waveform generated by the Hard Disk Controller. In the hard disk mode this waveform is passed through the data separator and is delayed according to the write precompensation inputs EARLY and LATE. When in the floppy mode precompensation is handled by the HDC 9224. |
| 8 | 10 MHz OUTPUT | 10MHzOUT | This output is a 10 MHz signal derived from $XTAL_1$ and $XTAL_2$. It is typically used as a 10 MHz clock for the HDC 9224. |
| 9, 10 | CRYSTAL 1, 2 | 20MHz/$XTAL_1$ $XTAL_2$ | A 20 MHz crystal may be connected between these two pins. If a TTL signal is used in place of a crystal, the TTL signal should be connected to the 20 MHz/$XTAL_1$ input and the $XTAL_2$ output should be disconnected. |
| 11 | 5 MHz OUTPUT | 5MHzOUT | This output is the 10 MHz output divided by two. It is normally connected to the HDC 9224 DMACLK input when the HDC 9225 chip is not being used. |
| 12 | WRITE GATE | WRGATE | This is the WRITE GATE input generated by the Hard Disk Controller. When low, the signal at the RDIN input is selected and output to the delay line via the XDL pin. When high (write mode), the signal at the WDATA input is selected and output to the delay line via the XDL pin for precompensation purposes (hard disk mode). |
| 13 | READ GATE | RDGATE | In hard disk mode, this active-high input signal, upon assertion, will permit the VCO to begin locking on the incoming data from the drive. When RDGATE is low, the VCO will lock on to a 5 MHz signal (20 MHz/4). |
| 14 | GROUND | GND | This is the ground pin for the device. |
| 15 | WRITE DATA OUT | WDOUT | This output is the precompensated WDATA signal. This output is the write data signal connected to the hard or floppy drive. |
| 16 | READ DATA IN | RDIN | This input receives data from the drive. |
| 17 | 4XVCO | 4XVCO | This signal is the output of the external VCO and runs at a frequency equal to four times the hard disk data rate. This signal is divided by two and then feeds the phase comparator to generate the PMPUP and PMPDWN signal. It is also divided by four and output as the RCLK signal when in the hard disk mode. |
| 18 | PUMP DOWN | $\overline{PMPDWN}$ | When asserted low, this output will decrease the frequency of the VCO. |
| 19 | PUMP UP | $\overline{PMPUP}$ | When asserted low, this output will increase the frequency of the VCO. |
| 20 | DELAY50 | DLY50 | This input is a 50ns delay of the XDL signal. The 50ns tap is used to arm the phase detector and to create a reclocked version of the raw read data from the hard disk drive. This input is also used (in conjunction with DLY40 and DLY30) to generate the hard disk precompensation delays. |

## DESCRIPTION OF PIN FUNCTIONS

| PIN # | NAME | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 21 | XDL | XDL | During write operations when WGATE is asserted, this output is identical to WDATA. XDL is output to the delay line thus creating precise delays which are used during write precompensation. When WGATE is not asserted, this output is the raw read data on the RDIN input. XDL is output to the delay line and is used to provide proper arming for the phase comparator and clocking for the reclocking circuitry. |
| 22 | TEST OUTPUT | DLYDAT | Leave disconnected. |
| 23 | TEST OUTPUT | VCOOUT | Leave disconnected. |
| 24, 25 | DELAY40<br>DELAY30 | DLY 40,<br>DLY 30 | These inputs are delays of 40 and 30ns of the XDL signal. The 40, 50 and 30ns delays are used respectively for nominal, late and early positioning of the bits respectively in the WDOUT signal when in the hard disk mode. |
| 26 | 5 VOLTS | +5V | This pin is the +5V power pin for the device. |
| 27 | RESET | $\overline{\text{RESET}}$ | For test only. Connect to +5V or leave disconnected. |
| 28 | 2XRDCLK | 2XRDCLK | When in the HARD DISK mode this output is nominally 10 MHz. When in the FLOPPY mode this output is nominally 250KHz, 500KHz or 1 MHz depending on the selected transfer rate.<br>NOTE: This output is undefined when switching between data rates, modes and during "LOCK TIME" associated with the switching of RDGATE. |

## DESCRIPTION OF OPERATION

The HDC 9227 contains a complete, high performance, digital data separator for floppy disk use as well as the digital portion of an analog data separator for hard disk use.

### HARD DISK MODE

(Selected when BOTH $CD_0$ and $CD_1 = 0$ )

When in the hard disk mode, the HDC 9227, in conjunction with the HDC 9223, an external tapped delay line and filter (shown in Schematic 2) allows a system designer to implement a phase locked loop to perform phase and frequency locking onto MFM encoded data from a Winchester hard disk.

In MFM format a pulse on RDIN corresponds not to a 1 or a 0 but to a flux transition on the media. These flux transitions can be spaced at T, 1.5T, or 2T, time intervals where the data transfer bit rate is T = 1/Freq. For the ST 506 drive, Freq. = 5MHz and the flux transitions may be spaced at 200, 300 or 400 nanoseconds.

Due to the phenomena of magnetic storage, the bit spacing is not constant but instead will vary due to magnetic effects and drive rotational speed variation. To compensate for this, the HDC 9227 takes the Read Data from the drive and generates two signals, $\overline{\text{RDATA}}$ and RCLK. The RCLK signal, derived from the VCO, changes period as a function of the variations in the disk data, permitting the data from the drive to be correctly clocked into the HDC 9224 independent of bit spacing variations on the media.

The VCO runs nominally at 20 MHz since the bit spacing can change in 100 ns increments and the oscillator must have the ability to adjust its frequency at this interval. The HDC 9227 divides 4XVCO by 2 and compares the phase of this signal to the incoming data. The positive edge of RDIN arms the phase detector for sampling the phase of the two signals. The positive edge of 4XVCO/2 asserts $\overline{\text{PMPDN}}$. The positive edge of DLY50 asserts $\overline{\text{PMPUP}}$. Sampling is terminated when $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDN}}$ are both asserted. The signal RCLK is generated by dividing 4XVCO by four.

When the HDC 9224 wants to read data from the disk, it asserts RGATE. This signal tells the phase locked loop to acquire bit synchronization. If Read Gate is inactive, the VCO will be locked to a crystal controlled signal of 5 MHz.

The HDC 9227 also performs hard disk write precompensation. Certain bit patterns, when written and then read back, are shifted either late or early depending on the bit pattern. Since this "bit" or "peak shift" is predictable, intentionally writing these bits late or early will compensate for the shift during read back.

The HDC 9224 recognizes these patterns, and in addition to producing the write data waveform, will generate the signals EARLY or LATE to allow the HDC 9227 to write the bits at the appropriate time. Typically, bits are written early or late by 10 ns. The last 3 taps of the delay line allow the HDC 9227 to implement the precompensation as a function of the EARLY and LATE signals. The final output write waveform is presented to the drive on the WDOUT pin.

### FLOPPY DISK MODE

(Selected when either $CD_0$ or $CD_1 = 1$)

When in the floppy mode the high performance digital data separator will accept data from the drive at 125K, 250K, or 500K data rates and output the appropriate regenerated clock and data signals.

The heart of the digital floppy disk data separator section is a synthetic oscillator phase locked loop. One half-bit cell of the incoming data stream corresponds to one cycle of the synthetic oscillator. Each oscillator cycle consists nominally of 20 phase slices. The circuit therefore needs a phase slice clock with a frequency of 20 times the half-bit cell time.

Detection of an input pulse away from the center "slot" of the half-bit cell causes a phase correction to be applied to the synthetic oscillator, bringing the center of the half-bit cell closer to the pulse.

A short history of input pulse detections (which induce phase corrections by the HDC 9227) is kept. This history is used to allow subsequent phase corrections to request upward or downward changes in center frequency, and helps compensate for drive speed variations.

Since the HDC 9227 provides a precompensated WDOUT (write data output) for floppy disks, this signal can be tied directly to the floppy drive and contains the precompensated write data required by the drive.

## MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 C to +150 C
Lead Temperature (soldering, 10 sec) ..... +300 C
Positive Voltage on any Pin, with respect to Ground ..... $V_{CC}$ +0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## DC ELECTRICAL SPECIFICATIONS (TA = 0 C to 70 C, $V_{CC}$ = 5.0V, ±5%)

| Parameter | Min. | Max. | Units | Comments |
|---|---|---|---|---|
| SUPPLY CURRENT | | | | |
| $I_{CC}$ | | | mA | |
| OUTPUT VOLTAGE | | | | |
| $V_{OH}$ | 2.4 | | V | $I_{OH}$ = 400uA (All outputs except 10MHzOUT and 5MHzOUT) |
| $V_{OH}$ | 4.3 | | V | $I_{OH}$ = 400 uA (10MHzOUT and 5MHzOUT) |
| $V_{OL}$ | | 0.4 | V | $I_{OL}$ = 2.0 mA |
| INPUT VOLTAGE | | | | |
| $V_{IH}$ | 2.0 | | V | (For all inputs except $XTAL_1$ and 4XVCO) |
| $V_{IL}$ | | 0.8 | V | (For all inputs except $XTAL_1$ and 4XVCO) |
| $V_{IH}$ | 3.5 | | V | (For $XTAL_1$ and 4XVCO) |
| $V_{IL}$ | | 1.5 | V | (For $XTAL_1$ and 4XVCO) |
| INPUT CURRENT | | | | |
| $I_{IH}$ | | 10 | µA | $V_{IH}$ = 2.0V |
| $I_{IL}$ | | 10 | µA | $V_{IL}$ = 0.4V |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

## AC ELECTRICAL CHARACTERISTICS (TA = 0C to +70C, $V_{CC}$ = 5.0V, ±5%)

| Symbol | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| $T_1$ | | | 70 | ns | figure 1 |
| $T_2$ | | | 80 | ns | figure 1 |
| $T_3$ | | | 65 | ns | figure 3 |
| $T_4$ | | | 70 | ns | figure 3 |
| $T_5$ | | | 100 | ns | figure 5 |
| $T_6$ | | | 100 | ns | figure 5 |
| $T_{11}$ | | | 65 | ns | figure 2 |
| $T_{12}$ | | | 65 | ns | figure 2 |
| $T_{13}$ | | | 65 | ns | figure 2 |
| $T_{14}$ | | | 65 | ns | figure 2 |
| $T_{15}$ | | | 45 | ns | figure 4 |
| $T_{16}$ | | | 45 | ns | figure 6 |
| $T_{17}$ | | | 45 | ns | figure 8 |
| $T_{18}$ | 45 | 50 | 55 | ns | figure 9 |
| $T_{19}$ | 25 | | | ns | figure 10 |
| $T_{20}$ | 25 | | | ns | figure 11 |
| $T_{21}$ | 6 | | | ns | figure 12 |
| $T_{22}$ | 50 | | | ns | figure 12 |
| $T_{23}$ | 25 | | 100 | ns | figure 12 |
| $T_{24}$ | | | | ns | figure 7 |
| $T_{25}$ | | | | ns | figure 7 |
| $T_{26}$ | | | | ns | figure 7 |
| $T_{27}$ | | | | ns | figure 7 |
| $T_{28}$ | | | | ns | figure 7 |
| $T_{29}$ | | | | ns | figure 7 |

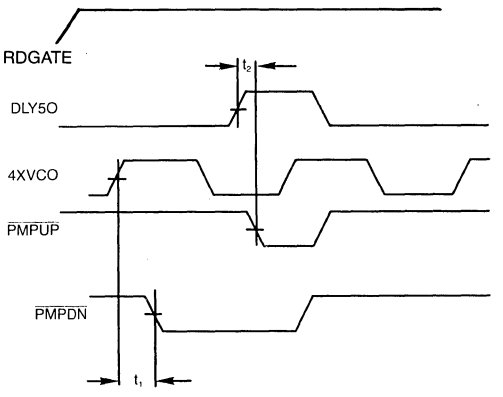



**FIGURE 1**

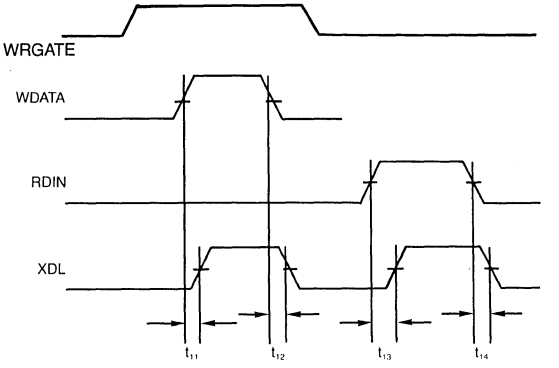



**FIGURE 2**

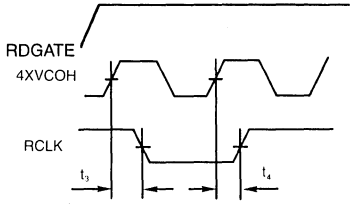



**FIGURE 3**

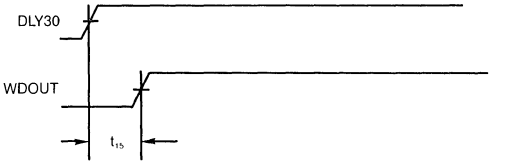



**FIGURE 4**

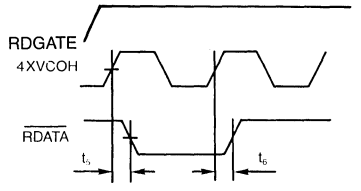



**FIGURE 5**

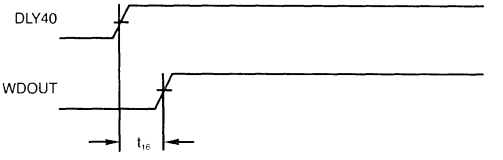



**FIGURE 6**

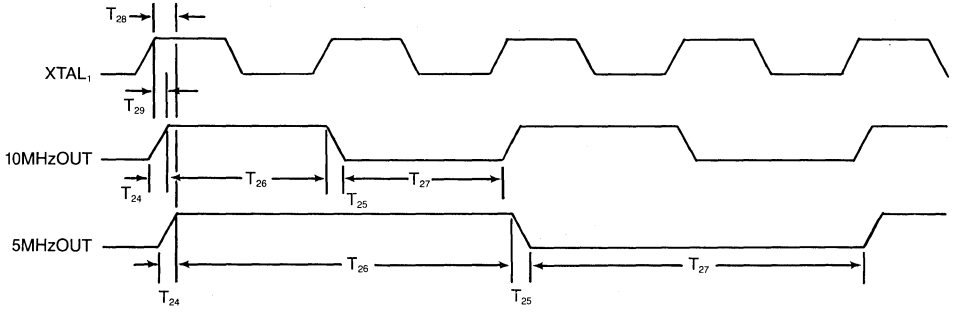



**FIGURE 7**

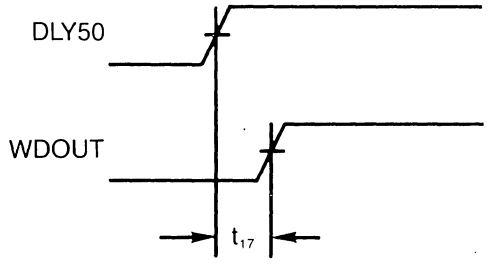



**FIGURE 8**

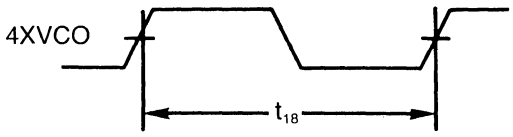



**FIGURE 9**

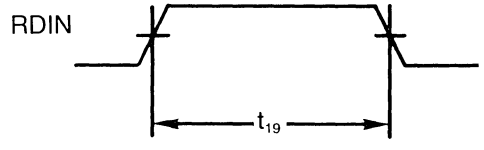



**FIGURE 10**

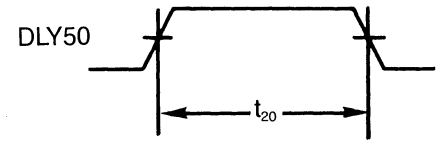



**FIGURE 11**

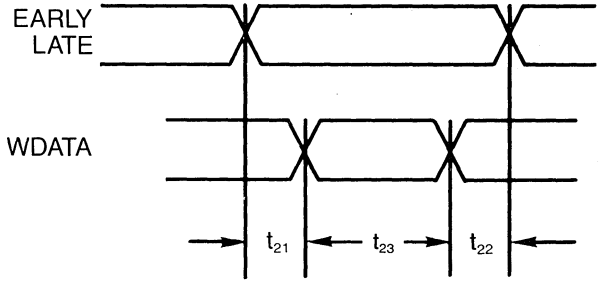


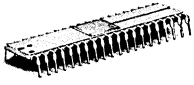

**FIGURE 12**

| $CD_1$ | $CD_0$ | Clock Rate | Data Rate | Drive Type and Mode |
|---|---|---|---|---|
| 0 | 0 | 10 MHz | 5 Mbs | Hard Disk, MFM |
| 0 | 1 | 20 MHz | 500 Kbs | Floppy, MFM |
| 1 | 0 | 10 MHz | 250 Kbs | Floppy, FM or MFM |
| 1 | 1 | 5 MHz | 125 Kbs | Floppy, FM |

**TABLE 1.**

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.



# Keyboard Encoder

| Part Number | No. of Keys | Modes | Features | Standard Fonts Suffix | Standard Fonts Description | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|---|
| KR-9600 XX[1] | 90 | 4 | 2 or N Key Rollover | -PRO<br>-STD | Binary Sequential<br>ASCII | +5 | 40 DIP/<br>44 SMT | 665-678 |
| KR-9601 XX[1] | 90 | 4 | 2 or N Key Rollover, caps-lock, -012[1] auto-repeat | -STD<br>-012[2] | Binary Sequential<br>ASCII | +5 | 40 DIP/<br>44 SMT | 665-678 |
| KR-9602 XX[1] | 90 | 4 | 2 or N Key Rollover, caps-lock, auto-repeat, serial output | -STD<br>-005[2] | Binary Sequential<br>ASCII | +5 | 28 DIP/<br>28 SMT | 665-678 |

[1]May be custom mask programmed [2]For future release

STANDARD MICROSYSTEMS CORPORATION

# KR9600
# KR9601
# KR9602

# Keyboard Encoder Read Only Memory
# KEM

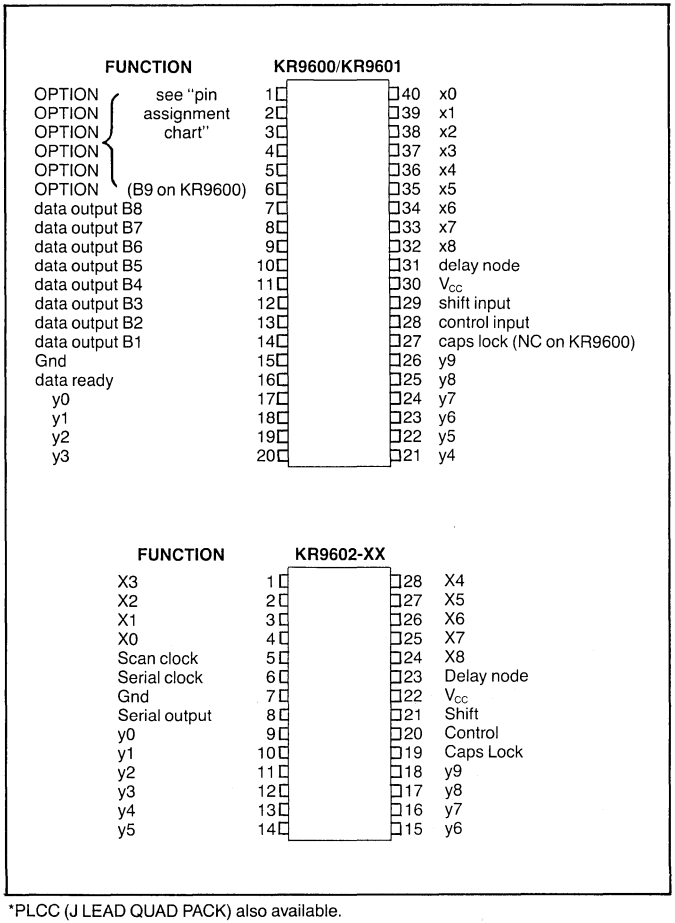
## FEATURES

- ☐ On-chip "caps" lock (KR9601, KR9602)
- ☐ On-chip auto repeat (KR9601, KR9602)
- ☐ Contact bounce protection
- ☐ N Key Rollover or Lockout operation
- ☐ Hysteresis on keyboard matrix inputs
- ☐ Tri-state TTL compatible data outputs
- ☐ Serial output (on KR9602 only)
- ☐ Quad Mode (Normal, shift, control, shift-control)
- ☐ High frequency clock input
- ☐ Pin-compatible with KR3600 (KR9600)
- ☐ Static charge protection on all inputs and outputs
- ☐ +5 volt supply

## EXTERNALLY SELECTABLE OPTIONS ON KR9600 AND KR9601

- ☐ Pulse or level data ready output signal
- ☐ External clock input
- ☐ On chip master/slave oscillator
- ☐ All 10 output bits available
- ☐ Lockout/Rollover external selection
- ☐ Chip enable external selection
- ☐ Data complement control
- ☐ Any Key Down output
- ☐ Selectable Auto-Repeat rate
- ☐ Programmable Auto-Repeat rate

## PIN CONFIGURATION*

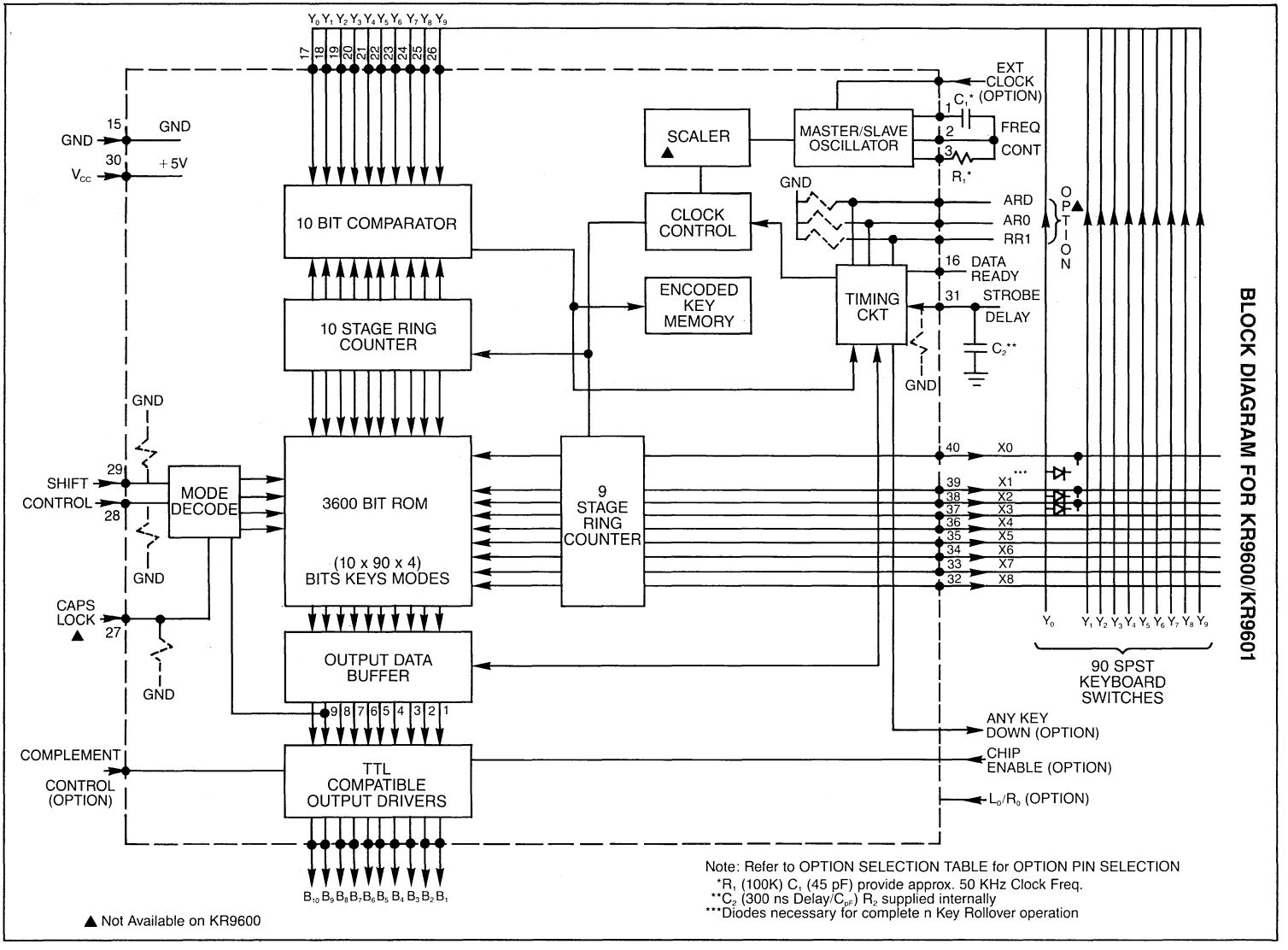



*PLCC (J LEAD QUAD PACK) also available.

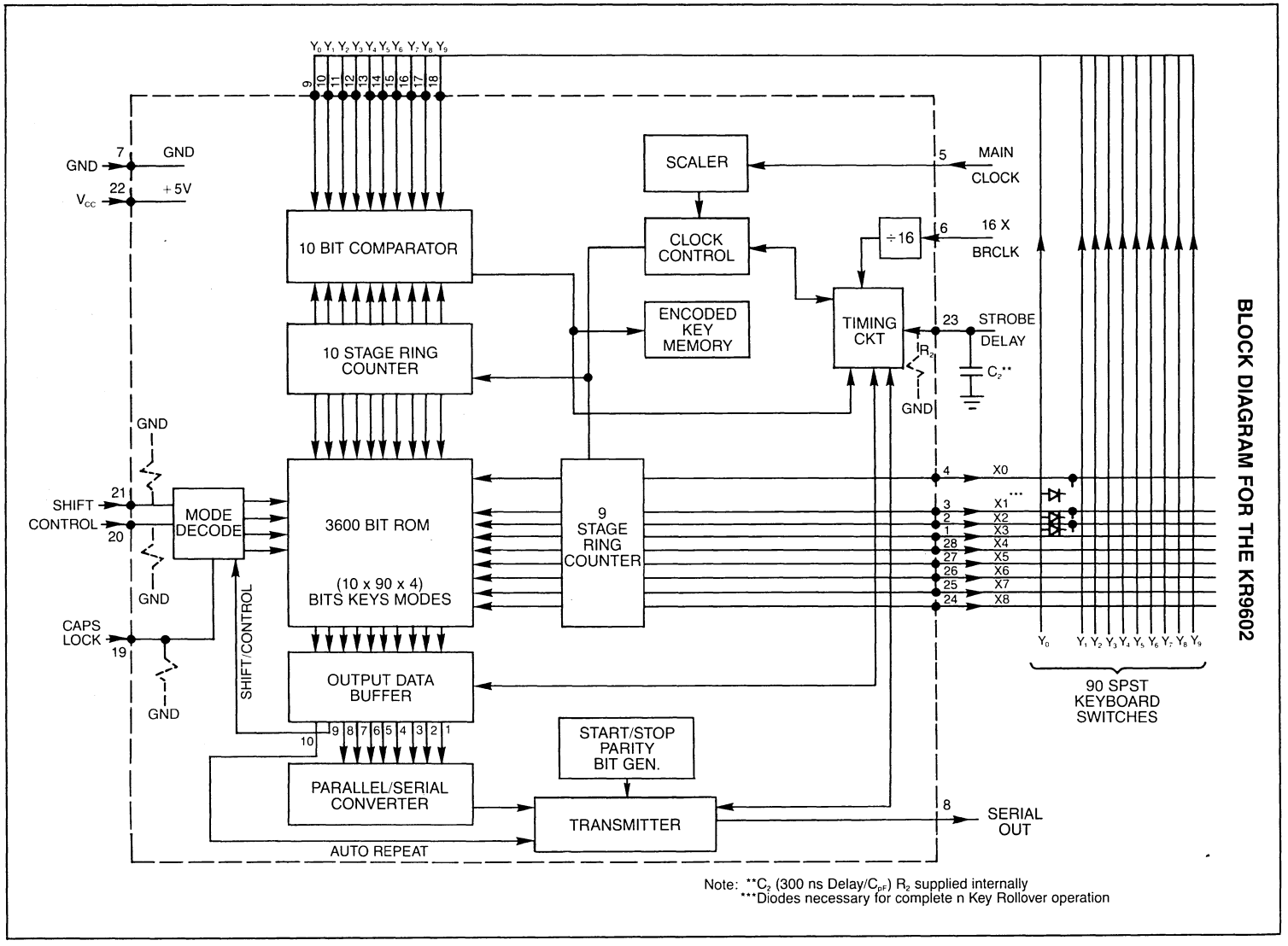
## GENERAL DESCRIPTION

The KR9600/1/2 is a keyboard encoder that contains all the logic necessary to debounce and encode SPST key-switches into a fully decoded data output of up to 10 bits. The KR9600/1/2 contains a 3600 bit ROM, 9 stage and 10 stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for N key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer and TTL compatible output drivers.

The KR9600 and the KR9601 provide a parallel data output in a 40 pin configuration with pin selectable options, while the KR9602 provides a serial asynchronous output in a 28 pin configuration with mask programmable options. (Ref. KR9600/1/2 custom coding information sheet).




BLOCK DIAGRAM FOR KR9600/KR9601




Note: **$C_2$ (300 ns Delay/$C_{pF}$) $R_2$ supplied internally
***Diodes necessary for complete n Key Rollover operation

## BLOCK DIAGRAM FOR THE KR9602

## DESCRIPTION OF PIN FUNCTIONS

| NAME | SYMBOL | KR9600 PIN # | KR9601 PIN # | KR9602 PIN # | FUNCTION |
|---|---|---|---|---|---|
| X OUTPUTS | X0-X8 | 40-32 | 40-32 | 4-1<br>28-24 | External outputs from the 9-stage ring counter to the keyboard to form X-Y matrix with the keyboard switches as the crosspoints. |
| Y INPUTS | Y0-Y9 | 17-26 | 17-26 | 9-18 | External inputs from the keyboard X-Y matrix. |
| EXTERNAL CLOCK (see note) | *** | 1 | 1 | 5 | External clock input. |
| SERIAL CLOCK | *** | *** | *** | 6 | Serial output Baud rate clock, for KR9602. |
| DATA OUTPUTS | B8-B1 | 7-14 | 7-14 | 8 | Data outputs B1-B8. Parallel outputs for the KR9600/9601, serial output for the KR9602. |
| DATA READY | DR | 16 | 16 | N/A | This output, which can be a level or a pulse, signals that a key closure has been detected and that data is available at the output port. |
| DELAY NODE INPUT | DELAY | 31 | 31 | 23 | Externally controllable delay network for eliminating the effect of switch contact bounce. |
| SHIFT INPUT | SHIFT | 29 | 29 | 21 | This input is used to select the shift mode data. |
| CONTROL INPUT | CNTRL | 28 | 28 | 20 | This input is used to select the control mode data. Simultaneous assertion of shift and control inputs will place the encoder into the shift-control mode. |
| CAPS LOCK | CAPS | see note | 27 | 19 | This input "ANDed" with bit B9 of the ROM will cause a mode shift. See "programming options". |
| POWER SUPPLY | $V_{CC}$ | 30 | 30 | 22 | +5V power supply. |
| GROUND | Gnd | 15 | 15 | 7 | Ground. |
| OPTION PINS | | see note | 1-6 | N/A | See option selection table for pin assignment. |

Note: Caps Lock and Auto-Repeat are not available on KR9600.
See option selection table for pin assignment.

## DESCRIPTION OF OPERATION

The main clocks for the KR9600 and KR9601 are derived from either an external clock source or the Internal oscillator. The KR9602 requires an external clock. The external clock is routed to a divider with a mask programmable division rate from 1 to 63 to generate the internal clock.

The keys are scanned in a nine output by ten input matrix, each key having a unique input-output combination connected to it. The inputs all go selectively to a level detector which has logically variable (1's and 0's) levels and hysteresis. The outputs are enabled one at a time from output X0 towards X8, at a rate of 10-100KHz, through a 9 stage ring counter. The 10 inputs are searched one at a time from Y0 to Y9, through a 10 stage ring counter, each time one of the outputs is enabled. The output and input pins all have pullups to $V_{CC}$ and are precharged each clock even if the scan is stopped at one key. When a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10 stage ring counter and the key has not been encoded, the switch bounce delay network is enabled. The key down stroke is examined, without advance to the next key location, until the key has been stable for the length of the DELAY CAP pin to discharge. The code for the depressed key is transferred to the output data buffer and the data ready signal appears.

The scan has two modes as determined by the LOckout/Rollover option. Once a key is determined to be down the scan will not advance if in the LOckout mode. Consequently a new key closure is not detected until the previously depressed key is released. The scan sequence will resume upon key release and the output data buffer stores the code of the last key encoded. In the Rollover mode a "1" is stored in the encoded key memory and the scan sequence is resumed and the code for the last encoded key remains in the data output buffer. Each depressed key is encoded regardless of the state of the previously depressed keys. The internal keyboard ROM is 10 bits wide. Bits 1-8 are output via data outputs B1-B8. Bits 9 and 10 may be output as data and/or utilized respectively for Caps-lock and Auto-repeat select. This allows mask programmable selection of which keys will have caps-lock and auto-repeat. When selected, the auto repeat will commence with a "long" delay after key depression followed by "short" delays. The duration of the delays varying with the clock frequency and the state of the ARD, AR0, and AR1 signals.

A Chip Enable input is available to enable the parallel output buffer. Data Ready can be put in the high-impedance state with Chip Enable (CE) or can be open drain as a mask programmable option to facilitate wire-oring as an interrupt.

In the serial output version of KR9602, when a key is debounced and then called valid, the serial shift register is loaded with the data (8 bits B1-B8) from the ROM, the data from the parity generator, and the data from the start and stop bits generator. Bits B9 and B10 are internally used respectively for Caps-lock and Auto-repeat select. The data register is then allowed to shift data out at the rate of one bit per 16 clocks of the baud rate clock pin, on the negative edge of that clock. If the baud rate clock is too slow with respect to the internal clock, and the keyboard were allowed to continue scanning when the data register is loaded, then new data could be loaded on top of shifting-out data.

To avoid this, if a new key is depressed before the previous data is fully shifted out of the device, including the stop bits, the delay cap will be allowed to decay but the internal logic will delay its effect until the shift out of the previous data is completed. If the new key is released before the end of the extended delay time it will not be encoded.

## OPTION SELECTION TABLE

Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to ten bits can be programmed into the KR9600/KR9601 ROM covering most popular codes such as ASCII, EBCDIC, SELECTRIC etc. as well as many specialized codes.*

### Pin Assignment for KR9600/KR9601

The chip pins from pin #1 thru pin #6 are optionally connected to differing logic functions. Many of the functions are available on more than one pin.

| PIN | FUNCTION (input unless noted) |
|---|---|
| 1 | Ext clock (opt. internal divisor of 1-63)** |
| 1 | Pin 1 of Internal oscillator. |
| 2 | Pin 2 of Internal oscillator. |
| 2 | Lo/Ro CC CE ARD** AR0** AR1** |
| 3 | Pin 3 of Internal oscillator. |
| 3 | Lo/Ro CC CE ARD** AR0** AR1** |
| 4 | AKO output |
| 4 | Lo/Ro CC CE ARD** AR0** AR1** |
| 5 | AKO or B10 output |
| 5 | Lo/Ro CC CE ARD** AR0** AR1** |
| 6 | B9 or AKO** output |

### Options Available for the KR9602:

The following options can be obtained on the KR9602 only with a mask program, and are not pin selectable:

Lo/Ro, CC, AUTO-REPEAT, LONG DELAY, SHORT DELAY, CLOCK DIVISOR 1,2,4,8,16,32,63; PARITY, 1 OR 2 STOP BITS.

### Legend

CC = COMPLEMENT CONTROL
AKO = ANY KEY DOWN
CE = CHIP ENABLE
Lo/Ro = LOCKOUT/ROLLOVER
B10 = B10 (DATA) OUTPUT
B9 = B9 (DATA) OUTPUT
INTERNAL CLOCK = SELF CONTAINED OSCILLATOR (Not available in KR9602)
EXTERNAL CLOCK = EXTERNAL FREQUENCY SOURCE
ARD = INITIAL AUTO-REPEAT DELAY
ARO, AR1 = SECONDARY AUTO-REPEAT DELAY, OR NO AUTO-REPEAT WHEN BOTH ARE FALSE.

*Contact local sales office for custom coding sheet.
**Not available on the KR9600.

## PROGRAMMING OPTIONS

The various options on the KR9600 and KR9601 are user selectable via externally programmable pins, but they are fixed, internally mask programmed, for the KR9602.

### Oscillator:

The main clocks are derived from either an external clock source or from the Internal oscillator. The resultant signal is then routed to a divider with a mask programmable division rate from 2 to 63. If no division is required then the divider is bypassed. The external clock requires one pin (pin #1), while the Internal oscillator needs three pins (pins #1, 2, 3) for frequency selection via an external resistor and capacitor.

### Lockout/Rollover: LO/RO

This option selects the operation of the key scan when a new key is detected. In Lockout the scan stops as long as the key is down. In Rollover the scan stops till the new key is debounced by the DELAY CAP and the key code is output. Then the key position is marked as down and the scan continues until another new key is seen. The option is selected either by an external pin or internally mask programmed, fixed in either state. The external LOckout selection is optionally hi or low active. A pulldown resistor to ground is optional.

### Complement Control: CC

This option inverts the logic true state of the DATA OUTPUTS and can optionally additionally invert the logic true state of the DATA READY pin. The option can be internally fixed as true or false where true will output a high logic level. When externally selected the option can be either input high or low active true. The pulldown to ground is optional.

### Data Ready:

The data ready pin is optionally either a pulse or level upon an output state ready to transfer. This transfer occurs when a new key is encoded or when the current key is repeating via the repeat logic. This output is individually capable of being disabled via CE or inverted via CC. To invert DATA READY is to have the pulse go logic low or the level fall to logic low active when the output is allowed to drive out of the chip.

### Any Key Down: AKO output

The AKO output is an indicator to tell that there is at least one key determined to be depressed. The output is optionally logic high or low true. The CE can be separately used to set the output in the high impedance mode. AKO will reset one full keyboard scan time after the last key is released. AKO cannot be inverted by CC (complement control).

### Chip Enable: $\overline{CE}$

The chip enable option can be internally fixed to true or

can be externally selected. When an external pin is used the true level is only low true. The true state means that the outputs connected to CE will go to the driven state from the high-impedance condition. Output pins B1-B10 are always affected by Chip Enable (CE), optional for Data Ready and Any Key Down. A pulldown to ground is optional.

### Shift Control Lock: S C L

These three pins determine what will be output in response to a new key being detected. The Caps Lock pin is optional on the KR9601 and KR9602 but it is not available on the KR9600. All three pins have optional pulldown resistors to ground. The Lock option is allowed if data bit nine of the ten data bits is programmed as true. In other words the Rom is read with no lock logic allowed, but with the full influence of the Shift and Control pins. This determines the B9 output which is used to see if this key can be shifted (be it a control code or not) by modifying the effect of the Shift upon a second read of the rom. The operation of the allowed Lock follows this table:

| L | B9 | S | C | Result | | |
|---|---|---|---|---|---|---|
| F | F | F | F | N | | |
| F | F | F | T | C | | |
| F | F | T | F | S | L = CAPS LOCK | |
| F | F | T | T | SC | B9 = DATA OUTPUT B9 | |
| | | | | | N = NORMAL | |
| F | T | F | F | N | S = SHIFT | |
| F | T | F | T | C | C = CONTROL | |
| F | T | T | F | S | SC = SHIFT and CONTROL | |
| F | T | T | T | SC | | |
| T | F | F | F | N | | |
| T | F | F | T | C | | |
| T | F | T | F | S | | |
| T | F | T | T | SC | | |
| T | T | F | F | S | Force N–>S | allow shift (ie m–>M) |
| T | T | F | T | SC | Force C–>SC | shift of Control |
| T | T | T | F | *S/N | Opt Force S–>N | allow reverse (ie M–>m) |
| T | T | T | T | *SC/C | Opt Force SC–>C | remove shift in Shift-Control |

*The mask programmable option for the removal of the shift is coded as either ON for all keys or OFF. Note that the B9 DATA output (and all the others) is the code of the second decode. Note that shift only occurs when both the lock is true and the unmodified code gives a B9 ROM output as true.

### Repeat: ARD AR0 AR1

When the Auto-repeat option is selected and a key is pressed, either of two delays can be selected. Typically a long initial delay after the key is pressed, and short delays afterwards if the key is still pressed. These delays consist of a programmable number of scan frequency time clocks varying from 2 to 131071 clock times.

This option is masked programmable and dependent on the programming of the data bit 10 of the ten data outputs to be true for the resultant key code (after lock logic) and upon whether any repeat action should occur at all.

There are three optional pins associated with the auto repeat logic: AR0, AR1, and ARD. Each of these can individually optionally have a pulldown resistor to ground. ARD controls the selection of the initial repeat delay count code, while the combination of AR0 and AR1 controls the selection of the short delays as shown below. If no external pins are desired then those functions can be mask programmed.

TYPICAL INITIAL REPEAT DELAY COUNTS

ARD = hi 80000 clock times
ARD = low 40000 clock times

The repeat delays are selected by a two bit code where one decode is used to disable the repeat operation completely.

TYPICAL SECONDARY REPEAT COUNTS

| AR0 | AR1 | Count |
|---|---|---|
| 0 | 0 | All Auto-Repeat Disabled |
| 0 | 1 | 6250 |
| 1 | 0 | 3125 |
| 1 | 1 | 1250 |

### Typical Example:

One typical approach would be to mask program ARD for only one long delay value and mask AR0 to ground. This way one can save two option pins for ARD and AR0 and still be able to select or disable auto-repeat via AR1 and have the option of having one fixed short delay value.

### ROM Data:

The actual programming data is in 10 bit wide characters with four function codes for each key position. There are 90 key positions organized as 9 "X" outputs with 10 "Y" inputs. The four functions as previously defined are Control, Shift, Normal, and Shift-Control.

The use of the optional Lock requires the programming of the B9 data bit. The use of the optional Auto-Repeat requires the programming of the B10 data bit. If the B9 or B10 outputs are used then these will show the result of the contents of the "corrected" key function data bits. The "corrected" function is the possibly changed Normal to Shift etc. etc. so that the output is that of the 'Shifted key code' NOT that of the initial key code.

---

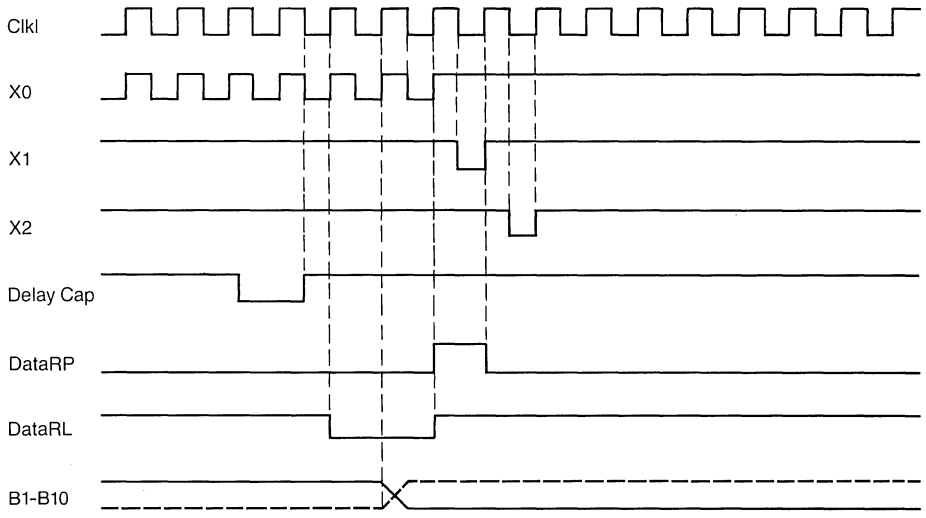
### Minimum Switch Closure:

T = Switch bounce + (90 x 1/f) + Strobe delay + Strobe width

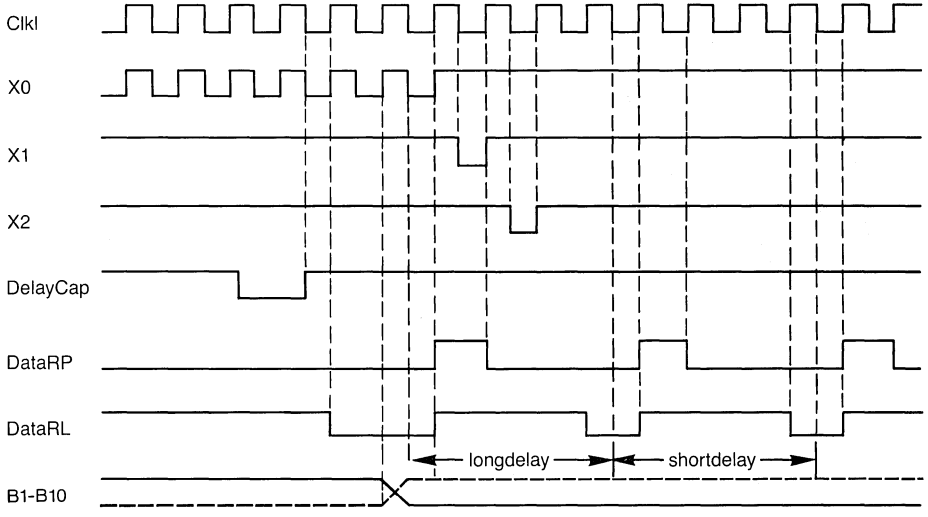
| | | | |
|---|---|---|---|
| maximum expected | determined by frequency of operation | determined by external capacitance | minimum time required by external circuitry |

**CONDITIONS:**

The clock divider is 1 so that Clkl is "same as clock IN".
A key is pressed down at X0Y0 but the delay cap has not timed out.
Data Ready is high true and we have already had another key.
DataRP = Data Ready as a Pulse DataRL = Data Ready as a Level




Condition: Test mode autorepeat at divide by 4 and keep key down



## ELECTRICAL CHARACTERISTICS: KR9600, KR9601, KR9602

### MAXIMUM GUARANTEED RATINGS

Operating Temperature Range** ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

### ELECTRICAL CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ± 5%, unless otherwise noted)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| D.C. CHARACTERISTICS | | | | | | |
| INPUT VOLTAGE LEVELS | | | | | | |
| Low Level | $V_{IL}$ | | | 0.8 | V | All inputs |
| High Level | $V_{IH}$ | 2.0 | | | V | Except Y + 16X CLK |
| | | 2.2 | | | V | 16X CLK only |
| Y INPUTS | | | | | | |
| High Level | $V_{YIH}$ | 2.8 | | | V | Y input |
| Low Level | $V_{YIL}$ | | | 0.8 | V | Y input |
| INPUT CURRENT | | | | | | |
| Leakage | $I_L$ | | | 10.0 | μA | All inputs except Y<br>$V_{IN}$ = 5V |
| Input with Pull-down resistor selected as option | | 75 | | 220 | μA | $V_{IN}$ = 5V |
| Y inputs | $I_{YIL}$ | −100 | −400 | −500 | μA | $V_{YIL}$ = 1 volt<br>Y inputs only |
| OUTPUT VOLTAGE LEVELS | | | | | | |
| Low Level | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| High Level | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = 100 μA<br>Except X outputs |
| X output voltage | $V_{OL}$ | | 0.4 | | V | 600 μA |
| | $V_{OH}$ | 3.4 | 4.0 | | V | clock high<br>$I_{OH}$ = 10 μA |
| TRI-STATE LEAKAGE | | | | 10 | μA | B1-B10 |
| INPUT CAPACITANCE | | | | | | |
| All inputs | $C_{IN}$ | | | 10 | pF | Except Y inputs |
| POWER SUPPLY CURRENT | $I_{CC}$ | | 20 | 40 | mA | KR9600/01 |
| | $I_{CC}$ | | 15 | 35 | mA | KR9602 |
| **A.C. CHARACTERISTICS** | | | | | | |
| CLOCK FREQUENCY* | $F_{IN}$ | 0.01 | | 4 | MHz | KR9601/02 |
| | | 0.01 | | 0.1 | MHz | KR9600 |
| | | DC | | 640 | KHz | KR9602 |
| 16X CLOCK FREQUENCY | | | | | | |
| Chip enable access time | $T_{CE}$ | | | 250 | ns | |
| SWITCH CHARACTERISTICS | | | | | | |
| Min switch closure | | | | | | see timing diagram |
| Contact closure resistance | $Z_{CC}$ | | | 300 | ohms | |
| | $Z_{CC}$ | 1 x $10^7$ | | | | |

NOTE: The KR9600 is a direct replacement for the KR3600. Please note that due to the logic level of the KR9600, when replacing the KR3600 in a N-Key rollover system where diodes are utilized, the polarity of the diodes must be reversed.

* Divisor on KR9601/02 must be selected such that the resulting internal scan frequency is 10 KHz min to 100 KHz max.

** Parts optionally available in extended temperature ranges in hermetic packages. Inquire at factory.

## KR9600-PRO DESCRIPTION

The KR9600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR9600 parts, the KR9600 PRO contains all of the logic to de-bounce and encode key-switch closures, while providing either a 2-key or N-key rollover.

The output of the KR9600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR9600 is shown in Table I. The format is simple: output bits, 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

| Bit 2 | Bit 3 | |
|---|---|---|
| 0 | 0 | Normal |
| 0 | 1 | Shift |
| 1 | 0 | Control |
| 1 | 1 | Shift Control |

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256 x 8 PROM, and Figure 2 a full 90 key, 4 mode application utilizing a 512 x 8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

**FIGURE 1**
**KR9600 PRO TYPICAL APPLICATION**
**64 KEY, 4 MODE**

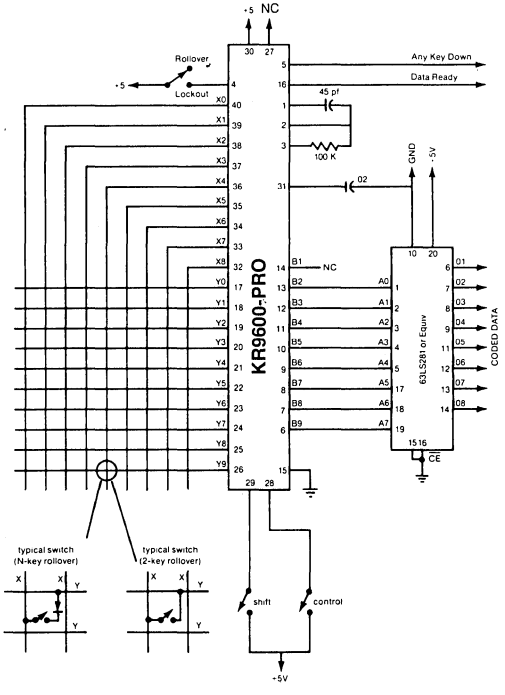
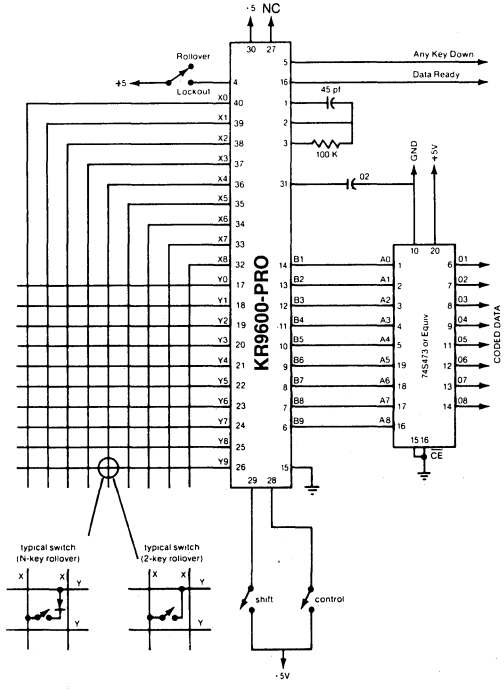



**FIGURE 2**
**KR9600 PRO TYPICAL APPLICATION**
**90 KEY, 4 MODE**




SECTION VII

# TABLE 1
## KR9600-PRO CODING SHEET AND OPTIONS

| XY | Normal B-12345678 910 | Shift B-12345678 910 | Control B-12345678 910 | Shift/Control B-12345678 910 |
|---|---|---|---|---|
| 00 | 000000000 | 001000000 | 010000000 | 011000000 |
| 01 | 000000001 | 001000001 | 010000001 | 011000001 |
| 02 | 000000010 | 001000010 | 010000010 | 011000010 |
| 03 | 000000011 | 001000011 | 010000011 | 011000011 |
| 04 | 000000100 | 001000100 | 010000100 | 011000100 |
| 05 | 000000101 | 001000101 | 010000101 | 011000101 |
| 06 | 000000110 | 001000110 | 010000110 | 011000110 |
| 07 | 000000111 | 001000111 | 010000111 | 011000111 |
| 08 | 000001000 | 001001000 | 010001000 | 011001000 |
| 09 | 000001001 | 001001001 | 010001001 | 011001001 |
| 10 | 000001010 | 001001010 | 010001010 | 011001010 |
| 11 | 000001011 | 001001011 | 010001011 | 011001011 |
| 12 | 000001100 | 001001100 | 010001100 | 011001100 |
| 13 | 000001101 | 001001101 | 010001101 | 011001101 |
| 14 | 000001110 | 001001110 | 010001110 | 011001110 |
| 15 | 000001111 | 001001111 | 010001111 | 011001111 |
| 16 | 000010000 | 001010000 | 010010000 | 011010000 |
| 17 | 000010001 | 001010001 | 010010001 | 011010001 |
| 18 | 000010010 | 001010010 | 010010010 | 011010010 |
| 19 | 000010011 | 001010011 | 010010011 | 011010011 |
| 20 | 000010100 | 001010100 | 010010100 | 011010100 |
| 21 | 000010101 | 001010101 | 010010101 | 011010101 |
| 22 | 000010110 | 001010110 | 010010110 | 011010110 |
| 23 | 000010111 | 001010111 | 010010111 | 011010111 |
| 24 | 000011000 | 001011000 | 010011000 | 011011000 |
| 25 | 000011001 | 001011001 | 010011001 | 011011001 |
| 26 | 000011010 | 001011010 | 010011010 | 011011010 |
| 27 | 000011011 | 001011011 | 010011011 | 011011011 |
| 28 | 000011100 | 001011100 | 010011100 | 011011100 |
| 29 | 000011101 | 001011101 | 010011101 | 011011101 |
| 30 | 000011110 | 001011110 | 010011110 | 011011110 |
| 31 | 000011111 | 001011111 | 010011111 | 011011111 |
| 32 | 000100000 | 001100000 | 010100000 | 011100000 |
| 33 | 000100001 | 001100001 | 010100001 | 011100001 |
| 34 | 000100010 | 001100010 | 010100010 | 011100010 |
| 35 | 000100011 | 001100011 | 010100011 | 011100011 |
| 36 | 000100100 | 001100100 | 010100100 | 011100100 |
| 37 | 000100101 | 001100101 | 010100101 | 011100101 |
| 38 | 000100110 | 001100110 | 010100110 | 011100110 |
| 39 | 000100111 | 001100111 | 010100111 | 011100111 |
| 40 | 000101000 | 001101000 | 010101000 | 011101000 |
| 41 | 000101001 | 001101001 | 010101001 | 011101001 |
| 42 | 000101010 | 001101010 | 010101010 | 011101010 |
| 43 | 000101011 | 001101011 | 010101011 | 011101011 |
| 44 | 000101100 | 001101100 | 010101100 | 011101100 |
| 45 | 000101101 | 001101101 | 010101101 | 011101101 |
| 46 | 000101110 | 001101110 | 010101110 | 011101110 |
| 47 | 000101111 | 001101111 | 010101111 | 011101111 |
| 48 | 000110000 | 001110000 | 010110000 | 011110000 |
| 49 | 000110001 | 001110001 | 010110001 | 011110001 |
| 50 | 000110010 | 001110010 | 010110010 | 011110010 |
| 51 | 000110011 | 001110011 | 010110011 | 011110011 |
| 52 | 000110100 | 001110100 | 010110100 | 011110100 |
| 53 | 000110101 | 001110101 | 010110101 | 011110101 |
| 54 | 000110110 | 001110110 | 010110110 | 011110110 |
| 55 | 000110111 | 001110111 | 010110111 | 011110111 |
| 56 | 000111000 | 001111000 | 010111000 | 011111000 |
| 57 | 000111001 | 001111001 | 010111001 | 011111001 |
| 58 | 000111010 | 001111010 | 010111010 | 011111010 |
| 59 | 000111011 | 001111011 | 010111011 | 011111011 |
| 60 | 000111100 | 001111100 | 010111100 | 011111100 |
| 61 | 000111101 | 001111101 | 010111101 | 011111101 |
| 62 | 000111110 | 001111110 | 010111110 | 011111110 |
| 63 | 000111111 | 001111111 | 010111111 | 011111111 |
| 64 | 100000000 | 101000000 | 110000000 | 111000000 |
| 65 | 100000001 | 101000001 | 110000001 | 111000001 |
| 66 | 100000010 | 101000010 | 110000010 | 111000010 |
| 67 | 100000011 | 101000011 | 110000011 | 111000011 |
| 68 | 100000100 | 101000100 | 110000100 | 111000100 |
| 69 | 100000101 | 101000101 | 110000101 | 111000101 |
| 70 | 100000110 | 101000110 | 110000110 | 111000110 |
| 71 | 100000111 | 101000111 | 110000111 | 111000111 |
| 72 | 100001000 | 101001000 | 110001000 | 111001000 |
| 73 | 100001001 | 101001001 | 110001001 | 111001001 |
| 74 | 100001010 | 101001010 | 110001010 | 111001010 |
| 75 | 100001011 | 101001011 | 110001011 | 111001011 |
| 76 | 100001100 | 101001100 | 110001100 | 111001100 |
| 77 | 100001101 | 101001101 | 110001101 | 111001101 |
| 78 | 100001110 | 101001110 | 110001110 | 111001110 |
| 79 | 100001111 | 101001111 | 110001111 | 111001111 |
| 80 | 100010000 | 101010000 | 110010000 | 111010000 |
| 81 | 100010001 | 101010001 | 110010001 | 111010001 |
| 82 | 100010010 | 101010010 | 110010010 | 111010010 |
| 83 | 100010011 | 101010011 | 110010011 | 111010011 |
| 84 | 100010100 | 101010100 | 110010100 | 111010100 |
| 85 | 100010101 | 101010101 | 110010101 | 111010101 |
| 86 | 100010110 | 101010110 | 110010110 | 111010110 |
| 87 | 100010111 | 101010111 | 110010111 | 111010111 |
| 88 | 100011000 | 101011000 | 110011000 | 111011000 |
| 89 | 100011001 | 101011001 | 110011001 | 111011001 |

**OPTIONS:**

Internal Oscillator (Pins 1, 2, 3)
Lockout/Rollover (Pin 4)
  Internal Resistor to GND
Lockout is Logic 1
Pulse Data Ready
Any Key Down (Pin 5) Positive Output
  Internal Resistor to GND on Shift and Control Pins

# CODING FOR KR9600–STD

| XY | Normal B-12345678910 | Shift B-12345678910 | Control B-12345678910 | Shift Control B-12345678910 |
|---|---|---|---|---|
| 00 | 1 1000111001 | < 0011111001 | 1 1000111011 | SUB 0101100001 |
| 01 | q 1000110101 | Q 1000101101 | q 1000111111 | DLE 0000100001 |
| 02 | a 1000010101 | A 1000000101 | a 1000011111 | @ 0000000101 |
| 03 | z 0101110101 | Z 0101100101 | z 0101111111 | P 0000100101 |
| 04 | HT 1001000001 | HT 1001000001 | HT 1001000001 | I 1001000101 |
| 05 | H 0001000101 | H 0001000101 | H 0001000101 | H 0001000111 |
| 06 | + 1101011001 | + 1101011001 | + 1101011001 | + 1101011011 |
| 07 | SO 0111001001 | > 0111111001 | SO 0111000001 | SO 0111000011 |
| 08 | p 0000110101 | @ 0000000101 | NUL 0000000001 | NUL 0000000001 |
| 09 | 1 1000111001 | ! 1000011001 | SOH 1000000001 | SOH 1000000001 |
| 10 | 2 0100111001 | @ 0000000101 | 2 0100111011 | ETB 1110100001 |
| 11 | w 1110110101 | W 1110100101 | w 1110111111 | 0011100101 |
| 12 | s 1100110101 | S 1100100101 | s 1100111111 | A 1000000101 |
| 13 | x 0001110101 | X 0001100101 | x 0001111111 | Q 1000100101 |
| 14 | RS 0111100001 | RS 0111100001 | RS 0111100001 | FS 0011100001 |
| 15 | % 1010011001 | % 1010011001 | % 1010011001 | % 1010011011 |
| 16 | m 1011010101 | ] 1011100101 | CR 1011000001 | CR 1011000001 |
| 17 | SI 1111000001 | SI 1111000001 | SI 1111000001 | SI 1111000111 |
| 18 | n 0111010101 | 0111100101 | SO 0111000001 | SO 0111000001 |
| 19 | 2 0100111001 | " 0100011001 | STX 0100000001 | STX 0100000001 |
| 20 | 3 1100111001 | # 1100011001 | 3 1100111011 | NAK 1010100001 |
| 21 | e 1010010101 | E 1010000101 | e 1010011111 | DC3 1100100001 |
| 22 | d 0010010101 | D 0010000101 | d 0010011111 | B 0100000101 |
| 23 | c 1100010101 | C 1100000101 | c 1100011111 | R 0100100101 |
| 24 | — 1111100100 | — 1111100100 | — 1111100100 | 0111100100 |
| 25 | $ 0010011001 | $ 0010011001 | $ 0010011001 | $ 0010011011 |
| 26 | L 0011000101 | L 0011000101 | L 0011000101 | L 0011000111 |
| 27 | US 1111100001 | US 1111100001 | US 1111100001 | US 1111100011 |
| 28 | 6 0110111001 | & 0110011001 | ACK 0110000001 | ACK 0110000001 |
| 29 | k 1101010101 | [ 1101100101 | DEL 1111111101 | DEL 1111111101 |
| 30 | 4 0010111001 | $ 0010011001 | 4 0010111011 | DC4 0010100001 |
| 31 | r 0100110101 | R 0100100101 | r 0100111111 | ENQ 1010000001 |
| 32 | f 0110010101 | F 0110000101 | f 0110011111 | C 1100000101 |
| 33 | SP 0000011000 | SP 0000011000 | SP 0000011000 | SP 0000011000 |
| 34 | CAN 0001101000 | ( 0001011000 | CAN 0001100000 | BS 0001000000 |
| 35 | CR 1011000001 | CR 1011000001 | CR 1011000001 | M 1011000101 |
| 36 | l 1101111101 | [ 1101111101 | [ 1101111111 | K 1101000101 |
| 37 | VT 1101000000 | VT 1101000000 | VT 1101000000 | VT 1101000010 |
| 38 | 7 1110111001 | ' 1110011001 | BEL 1110000001 | BEL 1110000001 |
| 39 | " 0100011001 | " 0100011001 | " 0100011001 | " 0100011011 |
| 40 | 5 1010111001 | % 1010011001 | 5 1010111011 | STX 0100000001 |
| 41 | t 0010110101 | T 0010100101 | t 0010111111 | EOT 0010000001 |
| 42 | g 1110010101 | g 1110000101 | G 1110011111 | D 0010000101 |
| 43 | v 0110110101 | V 0110100101 | v 0110111111 | S 1100100101 |
| 44 | ETX 1100000001 | ETX 1100000001 | ETX 1100000001 | ETX 1100000001 |
| 45 | ] 1011111101 | ] 1011111101 | ] 1011111111 | N 0111000101 |
| 46 | ? 1111111001 | ? 1111111001 | ? 1111111011 | [ 1101100101 |
| 47 | — 1011011001 | — 1011111001 | — 1011011001 | — 1011011011 |
| 48 | ) 1001011001 | ) 1001011001 | ) 1001011001 | ) 1001011011 |
| 49 | SP 0000011001 | SP 0000011001 | SP 0000011001 | SP 0000011011 |
| 50 | 6 0110111001 | > 0111111001 | 6 0110111011 | SOH 1000000001 |
| 51 | y 1001110101 | Y 1001100101 | y 1001111111 | DC1 1000100001 |
| 52 | h 0001010101 | H 0001000101 | h 0001011111 | E 1010000101 |
| 53 | b 0100010101 | B 0100000101 | b 0100011111 | T 0010100101 |
| 54 | : 0101111001 | * 0101011001 | : 0101111011 | SYN 0110100001 |
| 55 | > 0111111001 | > 0111111001 | > 0111111011 | Z 0101100101 |
| 56 | ; 1101111001 | + 1101011001 | ; 1101111011 | Y 1001100101 |
| 57 | NUL 0000000001 | NUL 0000000001 | NUL 0000000001 | NUL 0000000001 |
| 58 | * 0101011001 | * 0101011001 | * 0101011001 | * 0101011011 |
| 59 | ! 1000011001 | ! 1000011001 | ! 1000011001 | ! 1000011011 |
| 60 | 7 1110111001 | & 0110011001 | 7 1110111011 | ETX 1100000001 |
| 61 | u 1010110101 | U 1010100101 | u 1010111111 | BEL 1110000001 |
| 62 | j 0101010101 | J 0101000101 | j 0101011111 | F 0110000101 |
| 63 | n 0111010101 | N 0111000101 | n 0111011111 | U 1010100101 |
| 64 | = 1011111000 | = 1011111000 | = 1011111010 | = 0111111100 |
| 65 | < 0011111001 | < 0011111001 | < 0011111011 | W 1110100101 |
| 66 | p 0000110101 | P 0000100101 | p 0000111111 | J 0101000101 |
| 67 | o 0000111001 | ) 0001011001 | o 0000111011 | DC2 0100100001 |
| 68 | & 0110011001 | & 0110011001 | & 0110011001 | & 0110011011 |
| 69 | # 1100011001 | # 1100011001 | # 1100011001 | # 1100011011 |
| 70 | 8 0001111001 | * 0101011001 | 8 0001111011 | ESC 1101100001 |
| 71 | i 1001010101 | I 1001000101 | i 1001011111 | ACK 0110000001 |
| 72 | k 1101010101 | K 1101000101 | k 1101011111 | G 1110000101 |
| 73 | m 1011010101 | M 1011000101 | m 1011011111 | V 0110100101 |
| 74 | / 1111011001 | ? 1111111001 | / 1111011001 | ' 1110011001 |
| 75 | ' 1110011001 | " 0100011001 | ' 1110011001 | " 0100011001 |
| 76 | LF 0101000000 | LF 0101000000 | LF 0101000000 | GS 1011100000 |
| 77 | = 1011111001 | + 1101011001 | = 1011111001 | + 1101011001 |
| 78 | FF 0011001001 | < 0011111001 | FF 0011000001 | FF 0011000011 |
| 79 | ( 0001011001 | ( 0001011001 | ( 0001011001 | ( 0001011011 |
| 80 | 9 1001111001 | ( 0001011001 | 9 1001111011 | EM 1001100001 |
| 81 | o 1111010101 | O 1111000101 | o 1111011111 | ] 1011100101 |
| 82 | l 0011010101 | L 0011000101 | l 0011011111 | X 0001100101 |
| 83 | , 0011011001 | , 0011011001 | , 0011011001 | , 0011011011 |
| 84 | . 0111011001 | . 0111011001 | . 0111011001 | . 0111011011 |
| 85 | ; 1101111001 | : 0101111001 | ; 1101111001 | : 0101111001 |
| 86 | ] 1011100101 | [ 1101100101 | ] 1011100101 | [ 1101100101 |
| 87 | - 1011011001 | — 1111100101 | - 1011011001 | — 1111100101 |
| 88 | 0 0000111001 | 0 0000111001 | 0 0000111001 | 0 0000111001 |
| 89 | 9 1001111001 | ) 1001011001 | HT 1001000001 | HT 1001000001 |

**OPTIONS:**

Internal Oscillator (Pins 1, 2, 3)
Any Key Down (Pin 4) Positive Output
N-Key Rollover only
Pulse Data Ready signal

Internal Resistor to GND on Shift and Control Pins
KR9600-STD outputs provides ASCII bits 1-6 on B1-B6, and bit 7 on B8

# CODING FOR KR9601 AND KR9602 STD

| XY | Normal B-12345678 910 | Shift B-12345678 910 | Control B-12345678 910 | Shift/Control B-12345678 910 |
|---|---|---|---|---|
| 00 | 00000001 00 | 01010101 00 | 10101001 00 | 10101001 00 |
| 01 | 00000010 01 | 01010110 01 | 10101010 01 | 10101010 01 |
| 02 | 00000011 01 | 01010111 01 | 10101011 01 | 10101011 01 |
| 03 | 00000100 01 | 01011000 01 | 10101100 01 | 10101100 01 |
| 04 | 00000101 01 | 01011001 01 | 10101101 01 | 10101101 01 |
| 05 | 00000110 01 | 01011010 01 | 10101110 01 | 10101110 01 |
| 06 | 00000111 01 | 01011011 01 | 10101111 01 | 10101111 01 |
| 07 | 00001000 01 | 01011100 01 | 10110000 01 | 10110000 01 |
| 08 | 00001000 01 | 01011100 01 | 10110000 01 | 10110000 01 |
| 09 | 00001001 01 | 01011101 01 | 10110001 01 | 10110001 01 |
| 10 | 00001010 01 | 01011110 01 | 10110010 01 | 10110010 01 |
| 11 | 00001011 01 | 01011111 01 | 10110011 01 | 10110011 01 |
| 12 | 00001100 01 | 01100000 01 | 10110100 01 | 10110100 01 |
| 13 | 00001100 01 | 01100000 01 | 10110100 01 | 10110100 01 |
| 14 | 00001101 01 | 01100001 01 | 10110101 01 | 10110101 01 |
| 15 | 00001110 01 | 01100010 01 | 10110110 01 | 10110110 01 |
| 16 | 00001111 01 | 01100011 01 | 10110111 01 | 10110111 01 |
| 17 | 00010000 01 | 01100100 01 | 10111000 01 | 10111000 01 |
| 18 | 00010001 01 | 01100101 01 | 10111001 01 | 10111001 01 |
| 19 | 00010010 01 | 01100110 01 | 10111010 01 | 10111010 01 |
| 20 | 00010011 11 | 01100111 11 | 10111011 11 | 10111011 11 |
| 21 | 00010100 11 | 01101000 11 | 10111100 11 | 10111100 11 |
| 22 | 00010101 11 | 01101001 11 | 10111101 11 | 10111101 11 |
| 23 | 00010110 11 | 01101010 11 | 10111110 11 | 10111110 11 |
| 24 | 00010111 11 | 01101011 11 | 10111111 11 | 10111111 11 |
| 25 | 00011000 11 | 01101100 11 | 11000000 11 | 11000000 11 |
| 26 | 00011001 11 | 01101101 11 | 11000001 11 | 11000001 11 |
| 27 | 00011010 11 | 01101110 11 | 11000010 11 | 11000010 11 |
| 28 | 00011011 11 | 01101111 11 | 11000011 11 | 11000011 11 |
| 29 | 00011100 11 | 01110000 11 | 11000100 11 | 11000100 11 |
| 30 | 00011101 01 | 01110001 01 | 11000101 01 | 11000101 01 |
| 31 | 00011110 01 | 01110010 01 | 11000110 01 | 11000110 01 |
| 32 | 00011111 01 | 01110011 01 | 11000111 01 | 11000111 01 |
| 33 | 00011111 01 | 01110011 01 | 11000111 01 | 11000111 01 |
| 34 | 00100000 01 | 01110100 01 | 11001000 01 | 11001000 01 |
| 35 | 00100001 01 | 01110101 01 | 11001001 01 | 11001001 01 |
| 36 | 00100010 01 | 01110110 01 | 11001010 01 | 11001010 01 |
| 37 | 00100011 01 | 01110111 01 | 11001011 01 | 11001011 01 |
| 38 | 00100100 01 | 01111000 01 | 11001100 01 | 11001100 01 |
| 39 | 00100101 01 | 01111001 01 | 11001101 01 | 11001101 01 |
| 40 | 00100110 11 | 01111010 11 | 11001110 11 | 11001110 11 |
| 41 | 00100111 11 | 01111011 11 | 11001111 11 | 11001111 11 |
| 42 | 00101000 11 | 01111100 11 | 11010000 11 | 11010000 11 |
| 43 | 00101001 11 | 01111101 11 | 11010001 11 | 11010001 11 |
| 44 | 00101010 11 | 01111110 11 | 11010010 11 | 11010010 11 |
| 45 | 00101011 11 | 01111111 11 | 11010011 11 | 11010011 11 |
| 46 | 00101100 11 | 10000000 11 | 11010100 11 | 11010100 11 |
| 47 | 00101101 11 | 10000001 11 | 11010101 11 | 11010101 11 |
| 48 | 00101110 11 | 10000010 11 | 11010110 11 | 11010110 11 |
| 49 | 00101110 11 | 10000010 11 | 11010110 11 | 11010110 11 |
| 50 | 00101111 01 | 10000011 01 | 11010111 01 | 11010111 01 |
| 51 | 00110000 01 | 10000100 01 | 11011000 01 | 11011000 01 |
| 52 | 00110001 01 | 10000101 01 | 11011001 01 | 11011001 01 |
| 53 | 00110001 01 | 10000101 01 | 11011001 01 | 11011001 01 |
| 54 | 00110010 01 | 10000110 01 | 11011010 01 | 11011010 01 |
| 55 | 00110011 01 | 10000111 01 | 11011011 01 | 11011011 01 |
| 56 | 00110100 01 | 10001000 01 | 11011100 01 | 11011100 01 |
| 57 | 00110101 00 | 10001001 00 | 11011101 00 | 11011101 00 |
| 58 | 00110110 01 | 10001010 01 | 11011110 01 | 11011110 01 |
| 59 | 00110111 01 | 10001011 01 | 11011111 01 | 11011111 01 |
| 60 | 00111000 11 | 10001100 11 | 11100000 11 | 11100000 11 |
| 61 | 00111001 11 | 10001101 11 | 11100001 11 | 11100001 11 |
| 62 | 00111010 11 | 10001110 11 | 11100010 11 | 11100010 11 |
| 63 | 00111011 11 | 10001111 11 | 11100011 11 | 11100011 11 |
| 64 | 00111100 11 | 10010000 11 | 11100100 11 | 11100100 11 |
| 65 | 00111101 11 | 10010001 11 | 11100101 11 | 11100101 11 |
| 66 | 00111110 11 | 10010010 11 | 11100110 11 | 11100110 11 |
| 67 | 00111111 11 | 10010011 11 | 11100111 11 | 11100111 11 |
| 68 | 00111111 11 | 10010011 11 | 11100111 11 | 11100111 11 |
| 69 | 00111111 11 | 10010011 11 | 11100111 11 | 11100111 11 |
| 70 | 01000000 01 | 10010100 01 | 11101000 01 | 11101000 01 |
| 71 | 01000001 01 | 10010101 01 | 11101001 01 | 11101001 01 |
| 72 | 01000010 01 | 10010110 01 | 11101010 01 | 11101010 01 |
| 73 | 01000011 01 | 10010111 01 | 11101011 01 | 11101011 01 |
| 74 | 01000100 01 | 10011000 01 | 11101100 01 | 11101100 01 |
| 75 | 01000101 01 | 10011001 01 | 11101101 01 | 11101101 01 |
| 76 | 01000110 01 | 10011010 01 | 11101110 01 | 11101110 01 |
| 77 | 01000111 01 | 10011011 01 | 11101111 01 | 11101111 01 |
| 78 | 01001000 01 | 10011100 01 | 11110000 01 | 11110000 01 |
| 79 | 01001001 01 | 10011101 01 | 11110001 01 | 11110001 01 |
| 80 | 01001010 01 | 10011110 01 | 11110010 01 | 11110010 01 |
| 81 | 01001011 01 | 10011111 01 | 11110011 01 | 11110011 01 |
| 82 | 01001100 01 | 10100000 01 | 11110100 01 | 11110100 01 |
| 83 | 01001101 01 | 10100001 01 | 11110101 01 | 11110101 01 |
| 84 | 01001110 01 | 10100010 01 | 11110110 01 | 11110110 01 |
| 85 | 01001111 01 | 10100011 01 | 11110111 01 | 11110111 01 |
| 86 | 01010000 01 | 10100100 01 | 11110000 01 | 11111000 01 |
| 87 | 01010001 01 | 10100101 01 | 11110001 01 | 11111001 01 |
| 88 | 01010010 01 | 10100110 01 | 11111010 01 | 11111010 01 |
| 89 | 01010011 01 | 10100111 01 | 11111011 01 | 11111011 01 |

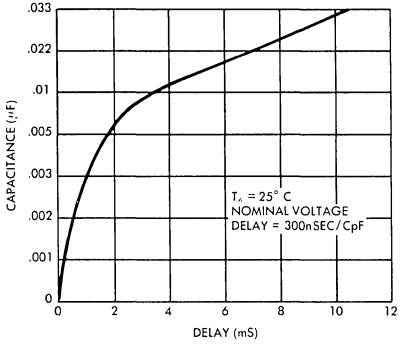
**OPTIONS FOR THE KR9601-STD:**

PINS 1, 2, 3 INTERNAL OSCILLATOR [Input clock divisor = 1]
PIN 4 CE [Active Low]
PIN 5 AR1 [AR0 fixed at Lo = 0]
[FIXED LONG DELAY OF 40000 CLOCK TIMES]
[FIXED SHORT DELAY OF 6250 CLOCK TIMES]
PIN 6 AKO [positive true]
Pulsed DATA READY signal
N-KEY ROLLOVER
Pull-down resistor to ground at the following pins:
_ SHIFT
_ CONTROL
_ CAPS-LOCK
_ ARO

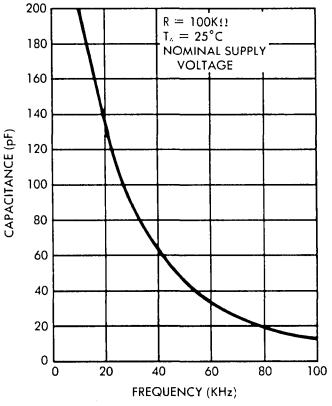
**OPTIONS FOR THE KR9602-STD:**

N-KEY ROLLOVER
AUTO-REPEAT
(FIXED LONG DELAY OF 40000 CLOCK TIMES)
(FIXED SHORT DELAY OF 6250 CLOCK TIMES)
1 STOP bit.
No PARITY bit.
Input clock divisor of 63
Pull-down resistor to ground at the following pins:
—SHIFT
—CONTROL
—CAPS-LOCK

## STROBE DELAY vs C2 FOR KR9600/1/2




## OSCILLATOR FREQUENCY vs C1 FOR KR9600/KR9601




## KEYBOARD LAYOUT FOR KR9601/9602-STD

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X8 Y0 | X7 Y0 | X0 Y0 | X0 Y1 | X0 Y2 | X0 Y3 | X0 Y4 | X0 Y5 | X0 Y6 | X0 Y7 | X1 Y7 | X1 Y8 | X1 Y9 | X1 Y4 | X1 Y5 | X1 Y6 | | X3 Y6 | | X3 Y4 | | | | | |
| X1 Y2 | X1 Y1 | X1 Y0 | X2 Y0 | X2 Y1 | X2 Y2 | X2 Y3 | X2 Y4 | X2 Y5 | X2 Y6 | X2 Y7 | X2 Y8 | X2 Y9 | X3 Y9 | X3 Y8 | | X3 Y7 | X3 Y5 | X5 Y4 | X7 Y1 | | | | | |
| X3 Y2 | X3 Y1 | X3 Y0 | X4 Y0 | X4 Y1 | X4 Y2 | X4 Y3 | X4 Y4 | X4 Y5 | X4 Y6 | X4 Y7 | X4 Y8 | X0 Y9 | X5 Y9 | X5 Y8 | X5 Y7 | X5 Y6 | X5 Y5 | X7 Y2 | | | | | | |
| X5 Y2 | X5 Y1 | X5 Y0 | X6 Y0 | X6 Y1 | X6 Y2 | X6 Y3 | X6 Y4 | X6 Y5 | X6 Y6 | X6 Y7 | X7 Y7 | X7 Y8 | X7 Y9 | X7 Y6 | X7 Y5 | X7 Y4 | X7 Y3 | X8 Y5 | X8 Y4 | | | | | |
| X8 Y3 | X8 Y2 | X8 Y1 | X8 Y6 | | | | | | | | | | X8 Y9 | | X8 Y8 | | X8 Y7 | | | | | | | |

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

# Shift Register

| Part Number | Description | Feature | Max Clock Freq. | Power Supply | Package | Page |
|---|---|---|---|---|---|---|
| SR 5015-80, 81, 133 | Quad Static Shift Register Mask Programmable Length | Load, Recirculate, Shift Controls | 1 MHz | +5 | 16 DIP | 673-676 |
| SR 5017 | Quad 133 Bit | Shift Left/Shift Right, Recirculate Controls | 1 MHz | +5 | 16 DIP | 677-680 |
| SR 5018 | Quad 81 Bit | | | | | |

STANDARD MICROSYSTEMS CORPORATION

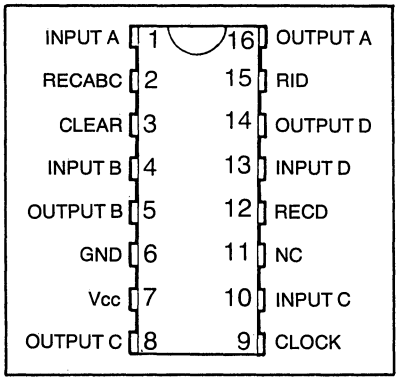
# SR 5015-XXX
## SR 5015-80
## SR 5015-81
## SR 5015-133

# Quad Static Shift Register

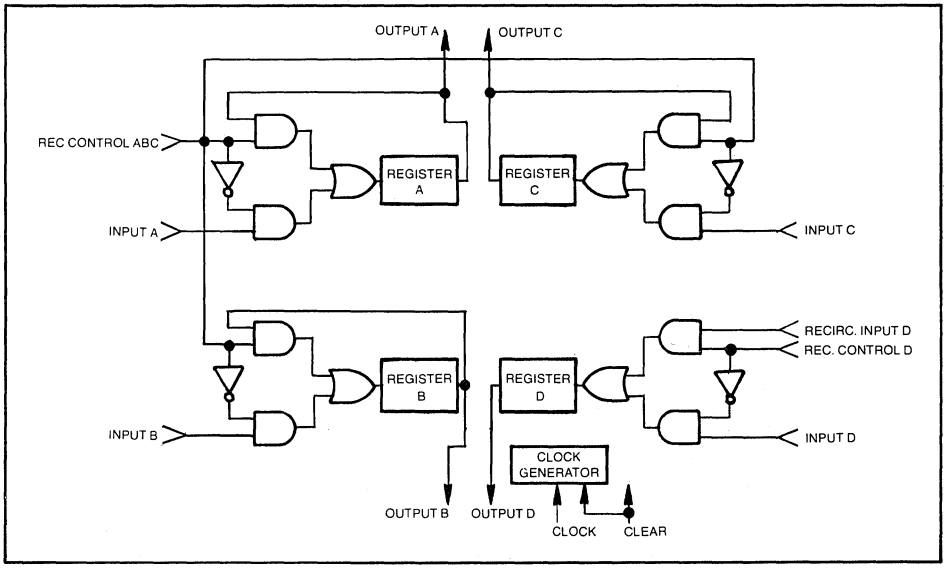
### FEATURES
- ☐ COPLAMOS® N Channel Silicon Gate Technology
- ☐ Variable Length—Single Mask Programmable—1 to 134 bits
- ☐ Directly TTL-compatible on all inputs, outputs, and clock
- ☐ Clear function
- ☐ Operation guaranteed from DC to 1.0 MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ 16 pin ceramic DIP Package
- ☐ Pin for Pin replacement for AMI S2182, 83, 85

### APPLICATIONS
- ☐ Memory Buffering
- ☐ Unique Buffering Lengths
- ☐ Terminals

### PIN CONFIGURATION




### BLOCK DIAGRAM




SECTION VIII

## General Description

The SMC SR 5015-XXX is a quad static shift register family fabricated using SMC's COPLAMOS® N channel silicon gate process which provides a higher functional density and speed on a monolithic chip than conventional MOS technology. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and single +5 volt power supply operation.

These shift registers can be driven by either $T^2L$ circuits or by MOS circuits and provide driving capability to MOS or $T^2L$ circuits. This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information. The SR 5015-80, SR 5015-81, and SR 5015-133 are respectively 80, 81, and 133 bit quad shift registers.

The recirculate control pin is common for registers A, B, and C. Register D has an independent recirculate control pin as well as a recirculate input pin.

A clear pin has been provided that will cause the shift register to be cleared when the pin is at $V_{CC}$. A single $T^2L$ clock is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 and 133 are available for flag storage.

This device has been designed to be used in high speed buffer storage systems and small recirculating memories.

Special custom configurations are achieved via single mask programming in lengths of 1 to 134 bits.

**MAXIMUM GUARANTEED RATINGS***

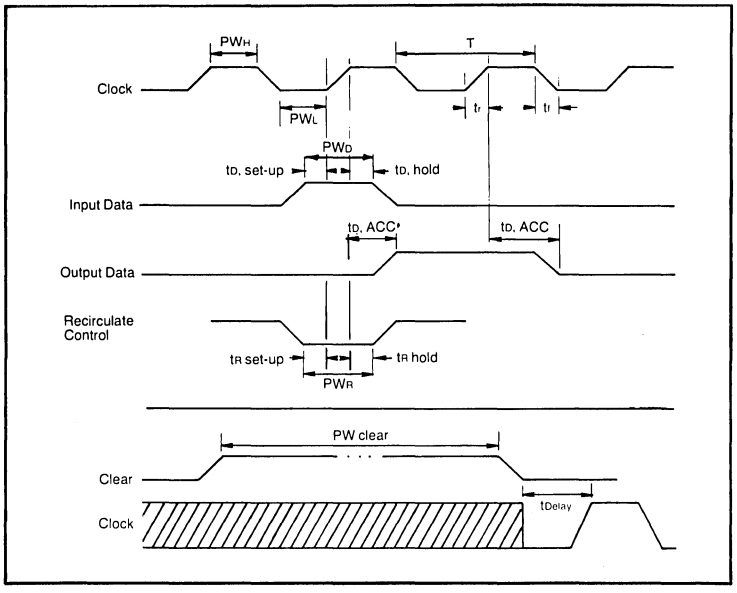
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. Characteristics** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{IL}$ | | | 0.8 | V | |
| High Level, $V_{IH}$ | $V_{CC}$−1.5 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=1.6ma |
| High Level, $V_{OH}$ | $V_{CC}$−1.5 | 4.0 | | V | $I_{OH}$=100μa |
| INPUT LEAKAGE CURRENT | | | 1.0 | μa | $V_{IN}$=$V_{CC}$ |
| CLOCK, CLEAR | | | 25 | pf | |
| All Other | | | 10 | pf | |
| POWER SUPPLY CURRENT | | | 80 | ma | |
| **A.C. Characteristics** | | | | | $T_A$=+25°C |
| CLOCK | | | | | |
| $PW_H$ | 300 | | | ns | |
| $PW_L$ | 600 | | | ns | |
| Transition, $t_r$, $t_f$ | | 0.02 | 1.0 | μs | |
| Repetition Rate, 1/T | 0 | | 1.0 | MHz | |
| $t_{Delay}$ | 300 | | | ns | |
| INPUT DATA | | | | | |
| $t_D$, set-up | 100 | | | ns | |
| $t_D$, hold | 200 | | | ns | |
| $PW_D$ | 300 | | | ns | |
| OUTPUT DATA | | | | | |
| $t_D$, ACC | | 200 | 350 | ns | |
| RECIRCULATE CONTROL | | | | | |
| $t_R$, set-up | 200 | | | ns | |
| $t_R$, hold | 300 | | | ns | |
| $PW_R$ | 500 | | | ns | |
| CLEAR | | | | | |
| $PW_{CLEAR}$ | 20 | | | μs | |

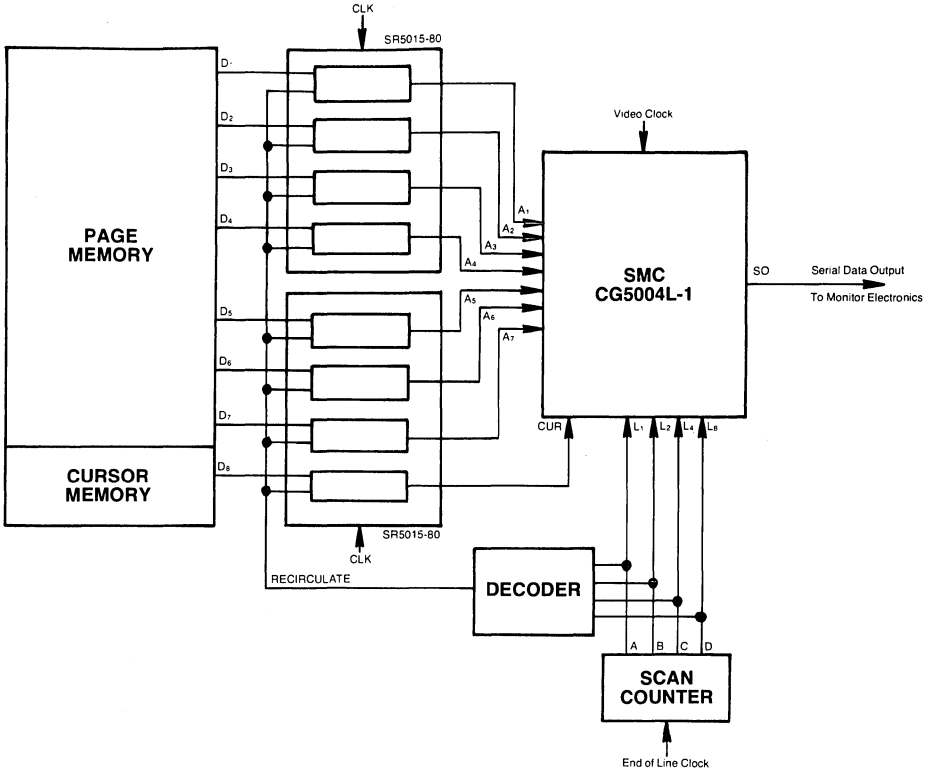
## TIMING DIAGRAMS



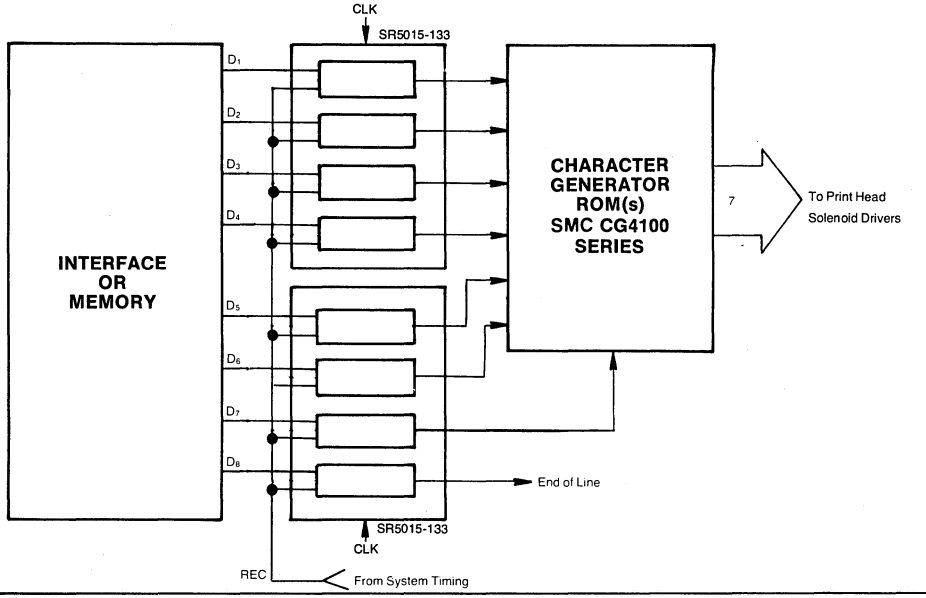

## Description of Pin Functions

| Pin No. | Symbol | Name | Function |
|---|---|---|---|
| 1 | A | Input A | Input signal which is either high or low depending on what word is to be loaded into shift register. |
| 2 | RECABC | Recirculate ABC | Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs. |
| 3 | CLR | Clear | Input signal when high forces outputs to a low state immediately and clears all the registers. |
| 4 | B | Input B | Input signal for B register. |
| 5 | $O_B$ | Output B | Output signal for B register. |
| 6 | GND | GND | Power supply Ground. |
| 7 | $V_{CC}$ | +5 Volt | 5 volt power supply. |
| 8 | $O_C$ | Output C | Output signal for C register. |
| 9 | CLK | Clock Input | Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock. |
| 10 | C | Input C | Input signal for C register. |
| 11 | NC | NC | |
| 12 | RECD | Recirculate Control D | Input signal which is normally low and, when goes high, disconnects Input D to register and connects Recirculate Input D to register. |
| 13 | D | Input D | Input signal for D register. |
| 14 | $O_D$ | Output D | Output signal for D register. |
| 15 | RID | Recirculate Input D | Input signal which is the input to the D register when Recirculate Control D is high: RECD=1. |
| 16 | $O_A$ | Output A | Output signal for A register. |

## Line Buffer for CRT Display . . . 80 Characters per line.




## Line Buffer for Matrix Printer . . . 132 Characters per line.




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# SR 5017
# SR 5018

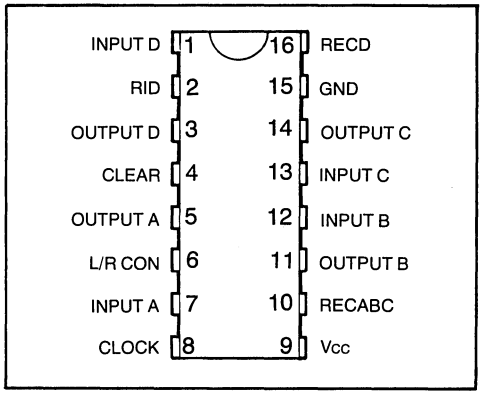
# Quad Static Shift Right/Shift Left Shift Register

## Last In First Out Buffer
## LIFO

### FEATURES

- ☐ COMPLAMOS® N-Channel Silicon Gate Technology.
- ☐ Quad 81 bit or Quad 133 bit
- ☐ Directly Compatible with T²L, MOS
- ☐ Operation Guaranteed from DC to 1.0MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ Single phase clock at T²L levels
- ☐ Clear function
- ☐ 16-pin Ceramic DIP Package

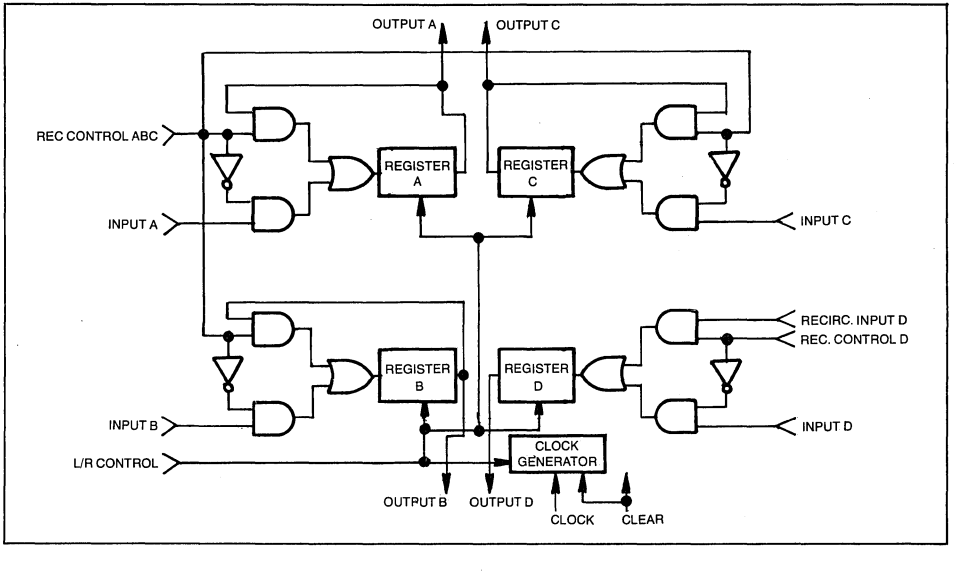
### PIN CONFIGURATION




### APPLICATIONS

- ☐ Bi-Directional Printer
- ☐ Computers—Push Down Stack—LIFO
- ☐ Buffer data storage—memory buffer
- ☐ Delay lines—delay line processing
- ☐ Digital filtering
- ☐ Telemetry Systems
- ☐ Terminals
- ☐ Peripheral Equipment

### BLOCK DIAGRAM




SECTION VIII

## General Description

The SMC SR 5017 and SR 5018 are quad 133 (SR 5017) and quad 81 (SR 5018) bit static shift registers utilizing SMC's COPLAMOS® N channel silicon gate process. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and requires only a single +5 volt power supply.

These shift registers can be driven by either $T^2L$ circuits or by MOS circuits and provide driving capability to MOS to $T^2L$ circuits.

This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information right or left. This shift left/shift right (L/R Control) control input is common to all registers.

The recirculate control input is common for registers A, B, and C. Register D has an independent recirculate control input as well as a Recirculate Input.

A Clear input has been provided that will cause the shift register to be cleared when the input is at $V_{CC}$. A single $T^2L$ clock input is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 or 133 are available for flag storage.

**MAXIMUM GUARANTEED RATINGS***

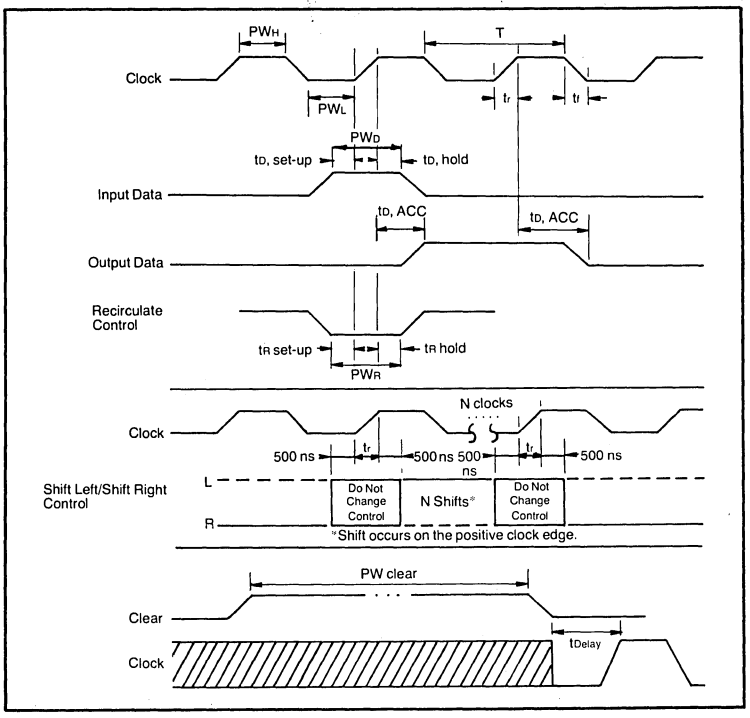
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

**ELECTRICAL CHARACTERISTICS** ($T_A$=0°C to 70°C, $V_{CC}$=+5V±5%, unless otherwise noted)

| Parameter | Min. | Typ. | Max. | Unit | Comments |
|---|---|---|---|---|---|
| **D.C. Characteristics** | | | | | |
| INPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{IL}$ | | | 0.8 | V | |
| High Level, $V_{IH}$ | $V_{CC}$—1.5 | | $V_{CC}$ | V | |
| OUTPUT VOLTAGE LEVELS | | | | | |
| Low Level, $V_{OL}$ | | | 0.4 | V | $I_{OL}$=1.6ma |
| High Level, $V_{OH}$ | $V_{CC}$—1.5 | 4.0 | | V | $I_{OH}$=100μa |
| INPUT LEAKAGE CURRENT | | | 1.0 | μa | $V_{IN}=V_{CC}$ |
| CLOCK, CLEAR | | | 25 | pf | |
| All Other | | | 10 | pf | |
| POWER SUPPLY CURRENT | | | 100 | ma | |
| **A.C. Characteristics** | | | | | $T_A$=+25°C |
| CLOCK | | | | | |
| $PW_H$ | 300 | | | ns | |
| $PW_L$ | 600 | | | ns | |
| Transition, $t_r$, $t_f$ | | 0.02 | 1.0 | μs | |
| Repetition Rate, 1/T | 0 | | 1.0 | MHz | |
| $t$ Delay | 500 | | | ns | |
| INPUT DATA | | | | | |
| $t_D$, set-up | 150 | | | ns | |
| $t_D$, hold | 150 | | | ns | |
| $PW_D$ | 300 | | | ns | |
| OUTPUT DATA | | | | | |
| $t_D$, ACC | | 200 | 350 | ns | |
| RECIRCULATE CONTROL | | | | | |
| $t_R$, set-up | 200 | | | ns | |
| $t_R$, hold | 300 | | | ns | |
| $PW_R$ | 500 | | | ns | |
| CLEAR | | | | | |
| $PW_{CLEAR}$ | 20 | | | μs | |

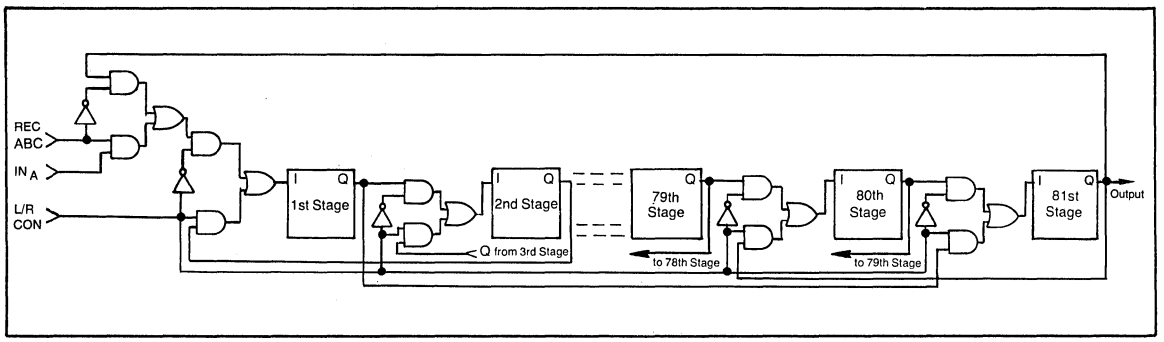
## Timing Diagram




## Description of Pin Functions

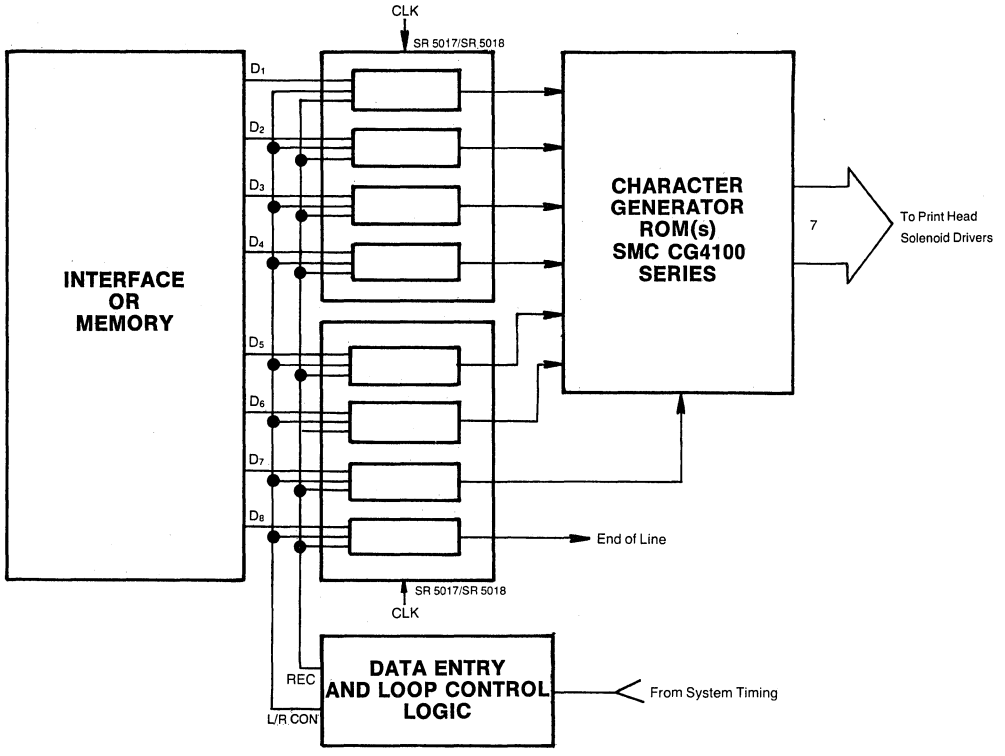
| Symbol | Name | Pin | Function |
|---|---|---|---|
| D | Input D | 1 | Input signal for D register. |
| RID | Recirculate Input D | 2 | Input signal which is the input to the D register when recirculate control D is high: RECD = 1. |
| $O_D$ | Output D | 3 | Output signal for D register. |
| CLR | Clear | 4 | Input signal when high forces outputs to a low state immediately and clears all the registers. |
| $O_A$ | Output A | 5 | Output signal for A register. |
| L/R CON | Shift Left/Shift Right Control | 6 | Input signal which is low for loading data and for shifting right. When L/R CON is high, the register will shift left. |
| A | Input A | 7 | Input signal which is either high or low depending on what word is to be loaded into shift register. |
| CLK | Clock Input | 8 | Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock. |
| $V_{CC}$ | 5 Volt | 9 | 5 volt power supply. |
| RECABC | Recirculate ABC | 10 | Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs. |
| $O_B$ | Output B | 11 | Output signal for B register. |
| B | Input B | 12 | Input signal for B register. |
| C | Input C | 13 | Input signal for C register. |
| $O_C$ | Output C | 14 | Output signal for C register. |
| GND | GND | 15 | Ground. |
| RECD | Recirculate Control D | 16 | Input signal which is normally low and, when goes high, disconnects Input D to register and connects RECIRCULATE INPUT D to register. |

## Logic Diagram



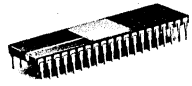

## APPLICATION

**Line Buffer for Bidirectional Matrix Printer . . .** 80/132 characters per line




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.



# Microprocessor Products

| Part Number | Description | Size | Process | Speed | Power Supplies | Package | Page |
|---|---|---|---|---|---|---|---|
| MPU800 | Microprocessor | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 691-714 |
| MPU800-1 | Microprocessor | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 691-714 |
| MPU800-4 | Microprocessor | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 691-714 |
| MPU810A | RAM-I/O-Timer | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 715-726 |
| MPU810A-1 | RAM-I/O-Timer | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 715-726 |
| MPU810A-4 | RAM-I/O-Timer | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 715-726 |
| MPU830 | ROM-I/O | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 727-734 |
| MPU830-1 | ROM-I/O | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 727-734 |
| MPU830-4 | ROM-I/O | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 727-734 |
| MPU831 | I/O | 8 Bit | CMOS | 2.5 MHz | 5V | 40 DIP | 727-734 |
| MPU831 | I/O | 8 Bit | CMOS | 1.0 MHz | 5V | 40 DIP | 727-734 |
| MPU831-4 | I/O | 8 Bit | CMOS | 4.0 MHz | 5V | 40 DIP | 727-734 |

STANDARD MICROSYSTEMS CORPORATION

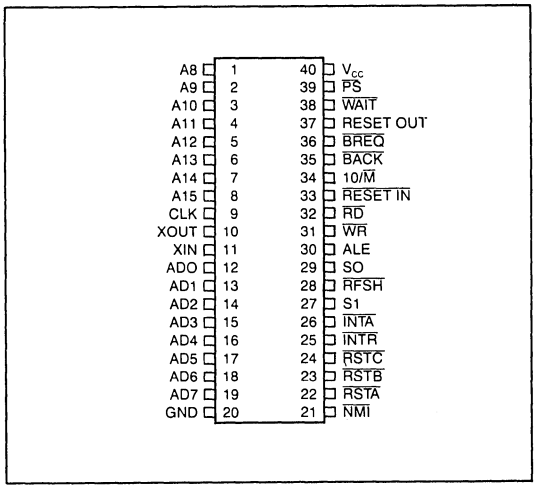
# MPU 800
# MPU 800-1
# MPU 800-4
PRELIMINARY

# High-Performance Low-Power Microprocessor

## FEATURES

- ☐ Variable Power Supply: 2.4V - 6.0V
- ☐ Fully Compatible Wth Z80® Instruction Set
- ☐ Pin-Compatible With NSC800
- ☐ Powerful Set of 158 Instructions
- ☐ 10 Addressing Modes
- ☐ 22 Internal Registers
- ☐ Low Power: 50 mW at 5 V Vcc
- ☐ Multiplexed Bus Structure
- ☐ On Chip Bus Controller and Clock Generator
- ☐ On-Chip 8 bit Dynamic RAM Refresh Circuitry
- ☐ Three Speed Versions:
  - MPU800-4 4 MHz
  - MPU800 2.5 MHz
  - MPU800-1 1 MHz
- ☐ Capable of addressing 64 k bytes of memory, and 256 I/O devices
- ☐ Five interrupt request lines on-chip
- ☐ Schmitt trigger input on reset
- ☐ Power-Save Feature

## PIN CONFIGURATION




## GENERAL DESCRIPTION

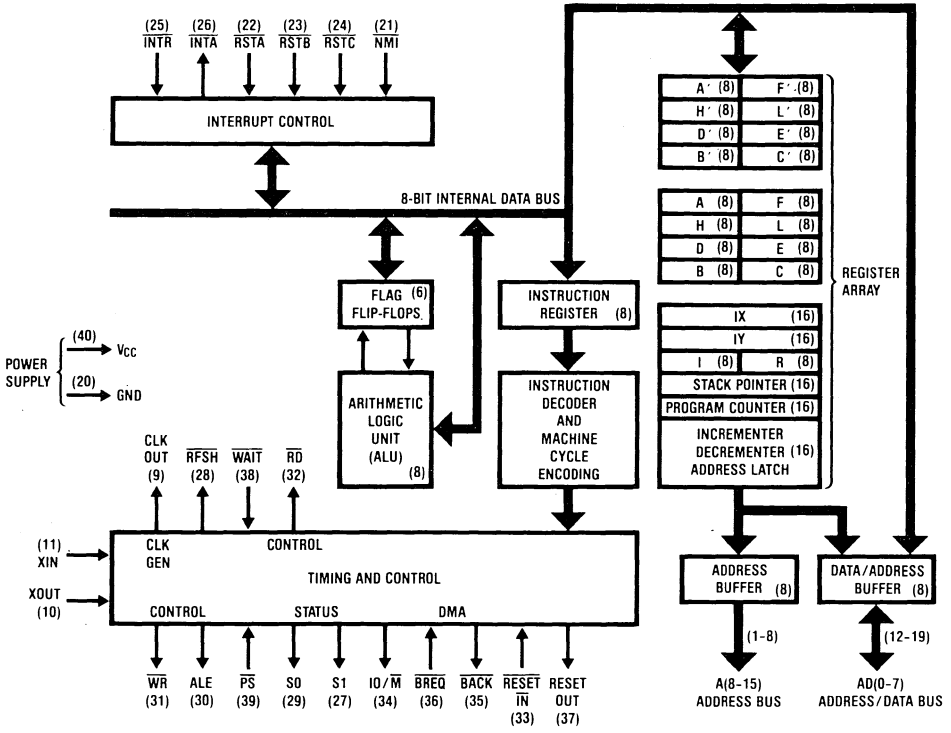
The MPU800 is an 8 bit microprocessor that functions as the central processing unit (CPU) in Standard Microsystems MPU800 microcomputer family. The device is fabricated in double-poly CMOS to combine high performance with the low-power of CMOS.

Many system functions are incorporated on the device including: vectored priority interrupts, refresh control, power save, and interrupt acknowledge.

Dedicated peripherals (MPU810 Ram I/O Timer, MPU830 ROM I/O Timer, and (MPU831 I/O Timer) have on-chip logic for direct interface to the MPU800.

SECTION IX

Z80 is a registered trademark of Zilog Corporation.




**CPU Functional Block Diagram**

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 40 | +5 Volt | Vcc | +5 volt supply |
| 20 | Ground | GND | Ground |
| 10 | Crystal Out | XOUT | Crystal connection |
| 11 | Crystal In | XIN | Crystal connection; XIN may be used as an external clock input |
| Input/Output Signals | | | |
| 12-19 | Address/Data | AD0-AD7 | Multiplexed Address/Data. Active high<br>At $\overline{RD}$ Time: Input data to CPU.<br>At $\overline{WR}$ Time: Output data from CPU.<br>At Falling Edge of ALE Time: Least significant byte of address during memory reference cycle. 8-bit port address during I/O<br>During $\overline{BREQ}$/ $\overline{BACK}$ Cycle: reference cycle.<br>High impedance. |
| Input Signals | | | |
| 33 | Reset In | $\overline{RESET\ IN}$ | Active low. Sets A (8-15) and AD (0-7) to TRI-STATE® (high impedance). Clears the contents of PC, I and R registers, disables interrupts, and causes a reset output to be activated. |
| 36 | Bus Request | $\overline{BREQ}$ | Active low. Used when another device is requesting the system bus. $\overline{BREQ}$ is recognized at the end of the current machine cycle, then A(8-15), AD(0-7), IO/$\overline{M}$, $\overline{RD}$, and $\overline{WR}$ are set to the high impedance mode and the request is acknowledged via the $\overline{BACK}$ output signal. |
| 21 | Non-Maskable Interrupt | $\overline{NMI}$ | Active low. The non-maskable interrupt, generated by the peripheral device(s), is the highest priority interrupt request line. The interrupt is edge sensitive and only a pulse is required to set an internal flip-flop which generates the internal interrupt request. Since the $\overline{NMI}$ flip-flop is monitored on the same clock edge as the other interrupts, it must also meet the minimum set-up time spec for the interrupt to be accepted in the current machine instruction. Once the interrupt is accepted the flip-flop is reset automatically, Its execution is independent of the interrupt enable flip-flop. $\overline{NMI}$ execution involves saving the PC on the stack and automatic branching to restart address X'0066 in memory. |
| 22-4 | Restart Interrupt A,B,C | $\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$ | Active low level sensitive. Restarts generated by the peripherals are recognized at the end of the current instruction if their respective interrupt enable bits and master enable bit are set. Execution is identical to $\overline{NMI}$ except interrupts are enabled for the following restart addresses:<br>**Name** — **Restart Address (X')**<br>$\overline{NMI}$ — 0066<br>$\overline{RSTA}$ — 003C<br>$\overline{RSTB}$ — 0034<br>$\overline{RSTC}$ — 002C<br>$\overline{INTR}$ (Mode 1) — 0038<br>The order of priority is fixed (highest first) as follows:<br>1) $\overline{NMI}$ 2) $\overline{RSTA}$ 3) $\overline{RSTB}$ 4) $\overline{RSTC}$ 5)$\overline{INTR}$ |
| 25 | Interrupt Request | $\overline{INTR}$ | Active low level sensitive. An interrupt request input generated by a peripheral device is recognized at the end of the current instruction provided that the interrupt enable and master interrupt enable bits are set. INTR is the lowest priority interrupt request input. Under program control, INTR can be executed in three distinct modes in conjunction with the INTA output. |
| 38 | Wait | $\overline{WAIT}$ | Active low. When set low during $\overline{RD}$, $\overline{WR}$ or $\overline{INTA}$ machine cycles, the CPU extends its machine cycle in increments of t (wait) states. The wait machine cycle continues until the WAIT input returns high.<br>The wait strobe input will be accepted only during machine cycles that have $\overline{RD}$, $\overline{WR}$ or $\overline{INTA}$ strobes and during the machine cycle immediately after an interrupt has been accepted by the CPU. The later cycle has its RD strobe suppressed but it will still accept the wait. |
| 39 | Power Save | $\overline{PS}$ | Active low. $\overline{PS}$ is sampled at the end of the current instruction cycle. When PS is low, the CPU stops executing at the end of current instruction and keeps itself in the low-power mode. Normal operation resumes when PS is returned high. |

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

| PIN NO | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| Output Signals | | | |
| 35 | Bus Acknowledge | $\overline{BACK}$ | Active low. $\overline{BACK}$ indicates to the bus requesting device that the CPU bus and its control signals are in the TRI-STATE mode. The requesting device may then take control of the bus and its control signals. |
| 1-8 | Address Bits 8-15 | A8-A15 | Active high. These are the most significant 8 bits of the memory address during a memory instruction. During an I/O instruction, the port address on the lower 8 bits of address get duplicated onto these 8 bits. During a $\overline{BREQ}/\overline{BACK}$ cycle, the A (8-15) bus is in the TRI-STATE mode. |
| 37 | Reset Out | RESET OUT | Active high. When RESET OUT is high, it indicates the CPU is being reset. The signal is normally used to reset the peripheral devices. |
| 34 | Input/Output/Memory | IO/$\overline{M}$ | An active high on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to an input/output device. An active low on the IO/$\overline{M}$ output signifies that the current machine cycle is relative to memory. It is TRI-STATE during $\overline{BREQ}/\overline{BACK}$ cycles. |
| 28 | Refresh | $\overline{RFSH}$ | Active low. The refresh output indicates that the dynamic RAM refresh cycle is in progress. $\overline{RFSH}$ goes low during T3 and T4 states of all M1 cycles. During the refresh cycle, AD(0-7) has the refresh address and A(8-15) indicates the interrupt vector register I. |
| 30 | Address Latch Enable | ALE | ALE is active only during the T1 state of any M cycle and also T3 state of M1 cycles. The high to low transition of ALE indicates that a valid memory/I-0/refresh address is available on the AD(0-7) lines. |
| 32 | Read Strobe | $\overline{RD}$ | Active low. On the trailing edge of the $\overline{RD}$ strobe, data is input to the CPU via the AD(0-7) lines. The $\overline{RD}$ line is in the TRI-STATE mode during $\overline{BREQ}/\overline{BACK}$ cycles. |
| 31 | Write Strobe | $\overline{WR}$ | While the $\overline{WR}$ line is low, valid data is output by the CPU on the AD(0-7) lines. The $\overline{WR}$ line is in the TRI-STATE mode during $\overline{BREQ}/\overline{BACK}$ cycles. |
| 9 | Clock | $\overline{CLK}$ | $\overline{CLK}$ is an output provided for use as a system clock. The $\overline{CLK}$ output is a square wave at one half the input frequency. |
| 26 | Interrupt Acknowledge | $\overline{INTA}$ | Active low. The interrupt acknowledge output is activated in the M1 cycle (S) immediately following the t state in which the $\overline{INTR}$ input is recognized. [Output is normally used to gate the interrupt response vector from the peripheral controller onto the AD(0-7) lines.] It is used in two of the three interrupt modes. In mode 0, an instruction is gated onto the AD (0-7) line during $\overline{INTA}$. There will be from 1 to 4 $\overline{INTA}$ strobes issued for each mode 0 interrupt. The amount of $\overline{INTA}$ strobes issued is instruction dependent. In mode 2, a single interrupt response vector is gated onto the data bus. In mode 1, $\overline{INTA}$ is not used. In this mode, $\overline{INTR}$ functions like the restart interrupts. |
| 29, 27 | Status | SO, S1 | Bus status outputs indicate encoded information regarding the ensuing M cycle as follows: |

| Machine Cycle | Status | | | Control | |
|---|---|---|---|---|---|
| | $\overline{SO}$ | $\overline{S1}$ | IO/$\overline{M}$ | $\overline{RD}$ | $\overline{WR}$ |
| Opcode Fetch | 1 | 1 | 0 | 0 | 1 |
| Memory Read | 0 | 1 | 0 | 0 | 1 |
| Memory Write | 1 | 0 | 0 | 1 | 0 |
| I/O Read | 0 | 1 | 1 | 0 | 1 |
| I/0 Write | 1 | 0 | 1 | 1 | 0 |
| Halt* | 0 | 0 | 0 | 0 | 1 |
| Internal Operation* | 0 | 1 | 0 | 1 | 1 |
| Acknowledge of Int** | 1 | 1 | 0 | 1 | 1 |

*ALE is not suppressed in this cycle.

**This is the cycle that occurs immediately after the CPU accepts an interrupt ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, $\overline{INTR}$, $\overline{NMI}$).

**Note 1:** During halt, CPU continues to do dummy opcode fetch from location following the halt instruction with a halt status. This is so CPU can continue to do its dynamic RAM refresh.

**Note 2:** No early status is provided for interrupt or hardware restarts.

## TIMING CONTROL

All necessary timing signals are provided by a single state inverter oscillator contained on the MPU800 chip. The chip operation frequency is equal to one half of the frequency of this oscillator. The oscillator frequency can be controlled by one of the following methods:

1. Leaving the XOUT pin unterminated and driving the XIN pin with an externally generated clock as shown in *Figure 1a*. When driving XIN with a square wave, the minimum duty cycle is 30%-70%, either high or low.

2. Connecting a crystal with the proper biasing network between XIN and XOUT as shown in *Figure 1b*. Recommended crystal is a parallel resonance AT cut crystal.

Resistor capacitor feedback network described in earlier data sheets will not oscillate due to gain of internal inverter circuit. A modification of this circuit by adding two inverters in series between the RC network and XIN will work.

The CPU has a minimum clock frequency input (@ XIN) of 32 kHz, which results in 16 kHz system clock speed. All registers internal to the chip are static, however there is dynamic logic which limits the minimum clock speed. The input clock can be stopped without fear of losing any data or damaging the part. You stop it in the phase of the clock that has XIN low and CLK OUT high. When restarting the CPU, precautions must be taken so that the input clock meets minimum specification. Once started, the CPU will continue operation from the same location at which it was stopped. During DC operation of the CPU, typical current drain will be 2mA. This current drain can be reduced by placing the CPU in a wait state during an opcode fetch cycle then stopping the clock.

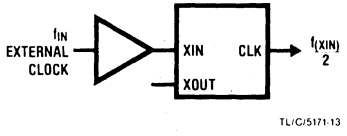
## FUNCTIONAL DESCRIPTION

The MPU800 is an 8-bit general purpose microprocessor designed for stand-alone and DMA (direct memory access) applications. A minimum system can be constructed with an MPU800, and MPU810 (RAMI/O Timer) and an 27C16 (EPROM).

MPU800 uses a multiplexed bus for data and addresses. The 16-bit address bus is divided into a high-order 8-bit address bus that handles bits 8-15 of the address, and a low-order 8-bit mulitplexed address/data bus that handles bits 0-7 of the address and bits 0-7 of the data. Strobe outputs from the MPU800 (ALE, $\overline{RD}$ and $\overline{WR}$) indicate when a valid address or data is present on the bus. IO/$\overline{M}$ indicates whether the ensuing cycle accesses memory or I/O.

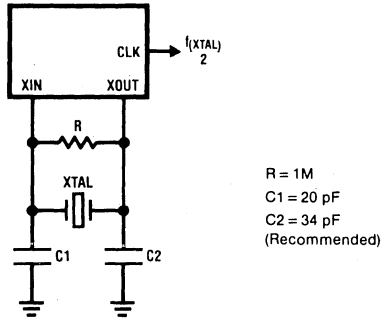
During an input or output instruction, the CPU duplicates the lower half of the address [AD(0-7)] onto the upper half [A(8-15)]. The eight bits of address will stay on A(8-15) for the entire machine cycle.

*Figure 2* illustrates the timing relationship for opcode fetch cycles with and without a wait state. *Figure 3* illustrates the timing relationship for memory read and write cycles with and without a wait state. Input/output cycles with and without wait state are shown in *Figure 4*. One wait state is automatically inserted into each I/O instruction.




TL/C/5171-13

a.




b.

**FIGURE 1. Timing Control Configurations**

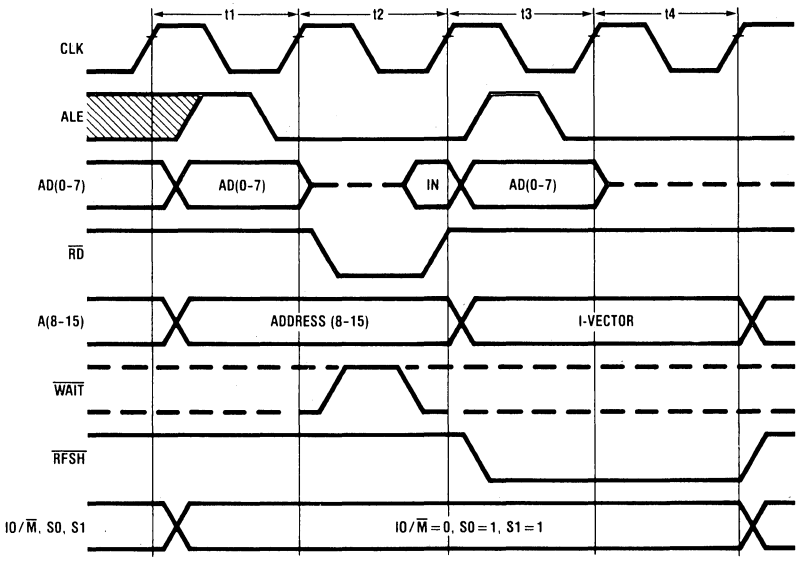



**FIGURE 2a. Opcode Fetch Cycles without WAIT States**

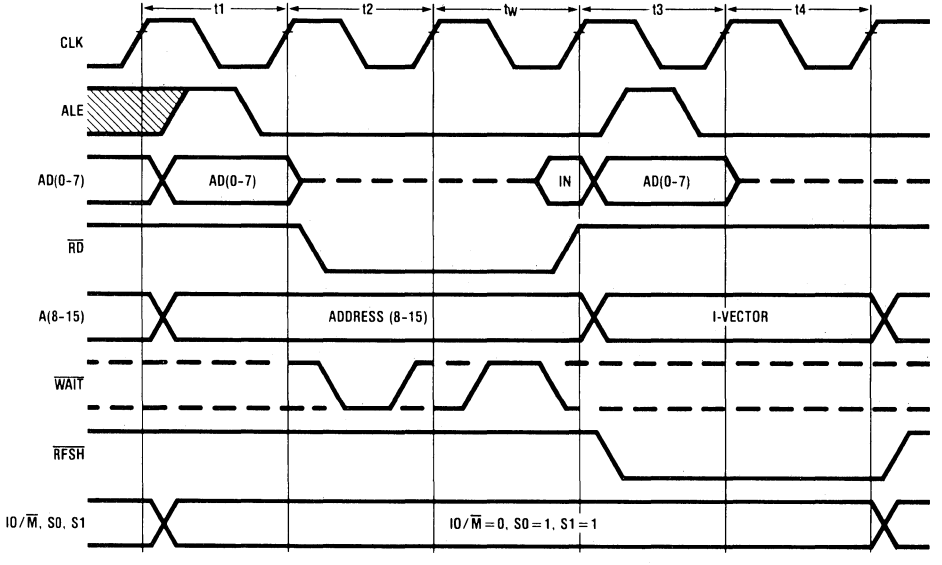



**FIGURE 2b. Opcode Fetch Cycles with WAIT States**

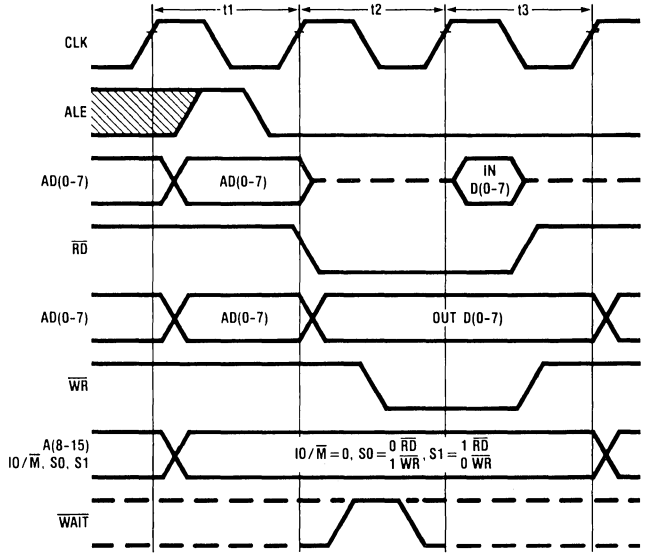



**FIGURE 3a. Memory Read/Write Cycles without WAIT States**

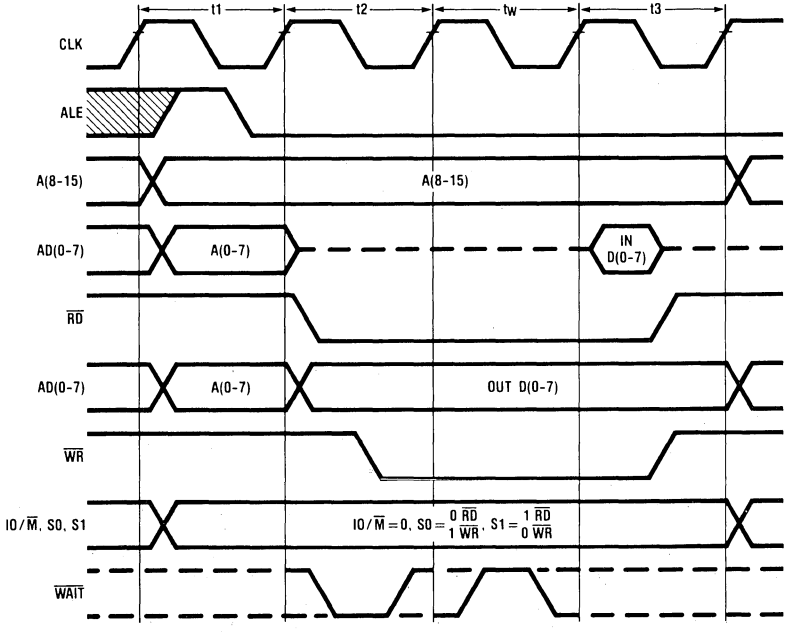



**FIGURE 3b. Memory Read and Write with WAIT States**

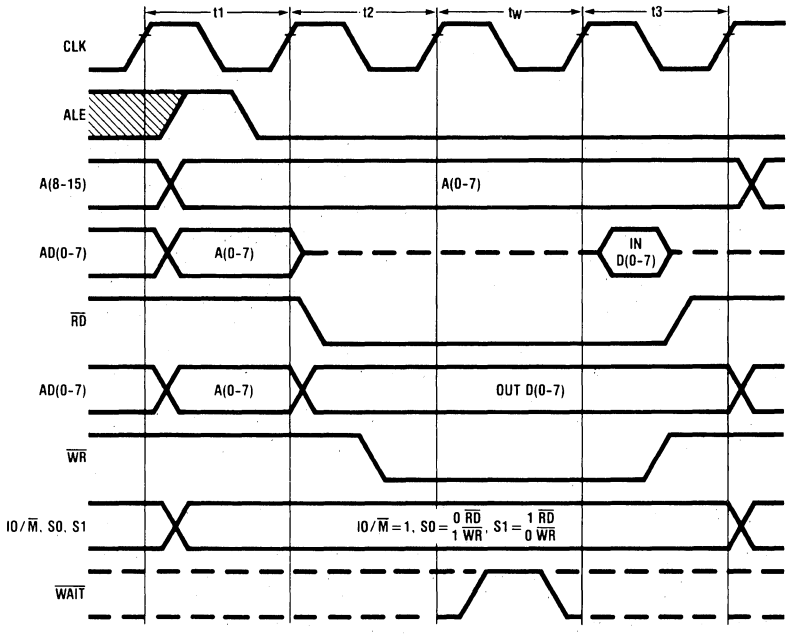
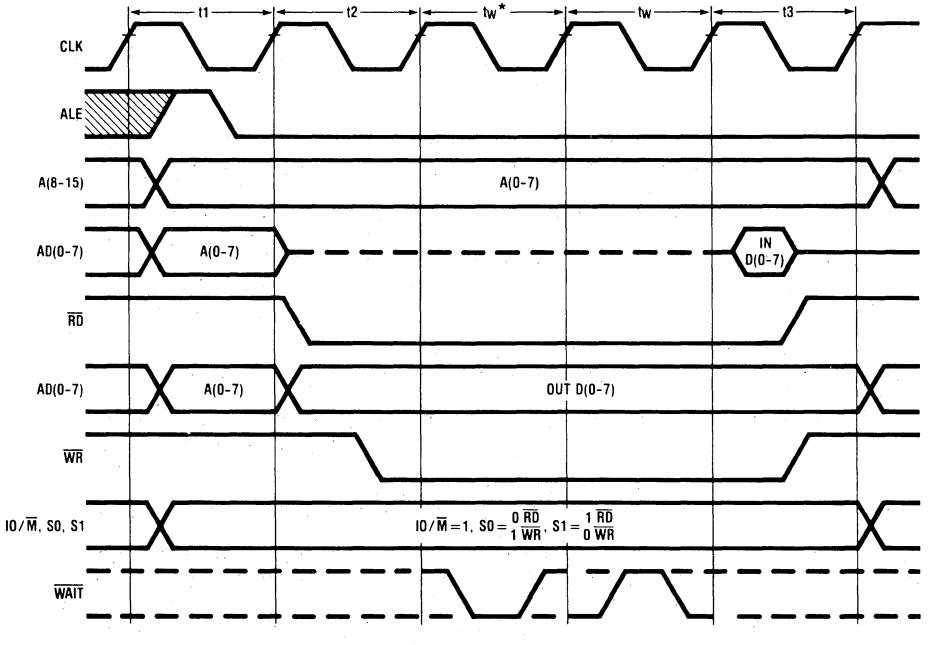



**FIGURE 4a. Input and Output Cycles without WAIT States**




*WAIT state automatically inserted during IO operation.

**FIGURE 4b. Input and Output Cycles with WAIT States**

## INITIALIZATION

The MPU800 and its peripheral components are initialized by $\overline{\text{RESET IN}}$ and RESET OUT. $\overline{\text{RESET IN}}$ input is associated with an on-chip Schmitt trigger that facilitates using an R-C network power-on reset scheme *(Figure 5)*.

To ensure proper power-up conditions for the NSC800, the following power-up and initialization procedure is recommended:

1. Apply power ($V_{CC}$ and GND) and set $\overline{\text{RESET IN}}$ active (low). Allow sufficient time (approximately 100 ms if crystal used) for the oscillator and internal clocks to stabilize. $\overline{\text{RESET IN}}$ must remain low for at least 3t state (CLK) times. RESET OUT, following the clock stabilization period, responds by going high, indicating to the system that the MPU800 is being reset. RESET OUT signal becomes available to reset the peripherals.

2. Set $\overline{\text{RESET IN}}$ high, following which the RESET OUT goes low and the CPU initiates the first opcode fetch cycle.

**NOTE:** The MPU800 initialization includes: Clear PC to X'0000 (the first opcode fetch, therefore, is from memory location X'0000). Clear registers I (Interrupt Vector Base) and R (Refresh Counter) to X'00. Clear interrupt control register bits IEA, IEB and IEC. The interrupt control bit IEI is set to 1 to maintain INS8080A/Z80A compatibility (see INTERRUPTS for more details). Maskable interrupts are disabled and the CPU enters Interrupt Mode 0. While $\overline{\text{RESET IN}}$ is active (low), the A(8-15) and AD(0-7) lines go to high impedance (TRI-STATE) and all CPU strobes go to the inactive state.

## BUS ACCESS CONTROL

*Figure 6* illustrates bus access control in the MPU800. The external device controller produces an active $\overline{\text{BREQ}}$ signal that requests the bus. When the CPU responds with BACK then the bus and related control strobes go to high impedance (TRI-STATE). It should be noted that (1) $\overline{\text{BREQ}}$ is sampled at the last t state of any M machine cycle only. (2) the MPU800 will not acknowledge any interrupt/restart requests, and will not perform any dynamic RAM refresh functions until after $\overline{\text{BREQ}}$ input signal is inactive high. (3) $\overline{\text{BREQ}}$ signal has priority over all interrupt request signals, should $\overline{\text{BREQ}}$ and interrupt request become active simultaneously.

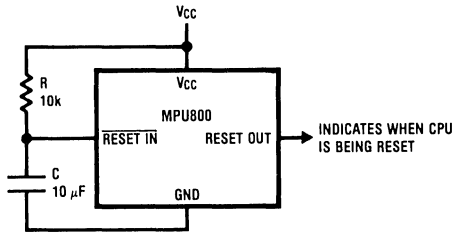
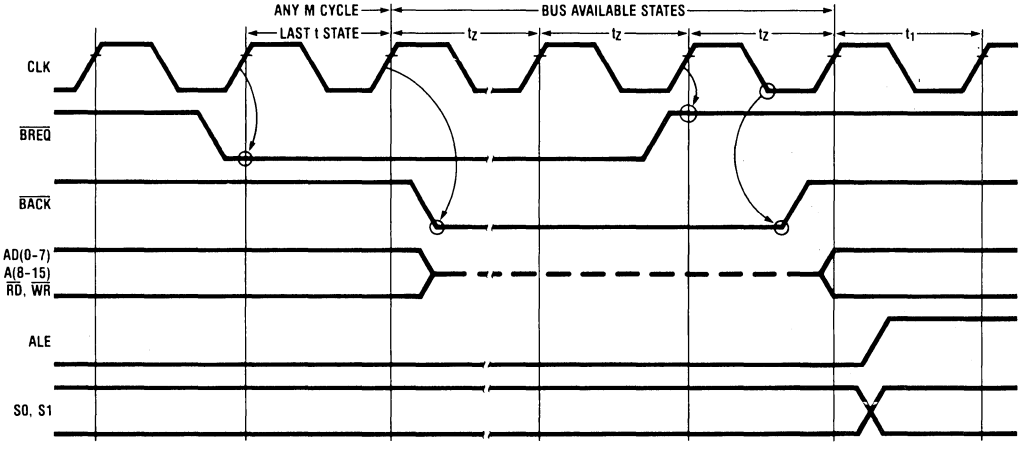



**FIGURE 5. Power-On Reset**




* S0, S1 during $\overline{\text{BREQ}}$ will indicate same machine cycle as during cycle when $\overline{\text{BREQ}}$ was accepted.
$t_Z$ = time states bus and control signals are in high impedance mode.

**FIGURE 6. Bus Acknowledge Cycle**

## REGISTER CONFIGURATION

The MPU800 contains 22 programmable registers as shown in *Figure 7*. The CPU working registers are arranged in two 8-register configurations, each of which includes an 8-bit accumulator, a flag register, and six general purpose 8-bit registers. Only one 8-bit register set may be active at any given moment. However, simple instructions exist that allow the programmer to exchange the active and alternate register sets.

It should also be noted that the six 8-bit general purpose registers (B, C, D, E, H, and L) can be accessed as 16-bit registers (BC, DE, and HL). The functions of these become apparent in the instruction set description.

**CPU Main Working Register Set**

| | | | |
|---|---|---|---|
| Accumulator | (8) | Flags F | (8) |
| Register B | (8) | Register C | (8) |
| Register D | (8) | Register E | (8) |
| Register H | (8) | Register L | (8) |

**CPU Alternate Working Register Set**

| | | | |
|---|---|---|---|
| Accumulator A' | (8) | Flags F' | (8) |
| Register B' | (8) | Register C' | (8) |
| Register D' | (8) | Register E' | (8) |
| Register H' | (8) | Register L' | (8) |

**CPU Dedicated Registers**

| | |
|---|---|
| Index Register IX | (16) |
| Index Register IY | (16) |
| Interrupt Vector Register I | (8) |
| Memory Refresh Register R | (8) |
| Stack Pointer SP | (16) |
| Program Counter PC | (16) |

**FIGURE 7. Register Configuration**

## DEDICATED REGISTERS:

**Program Counter (PC):** The program counter contains the 16-bit address of the current instruction being fetched from memory. The PC is incremented after its contents have been transferred to the address lines. When a program jump occurs, the new address is placed in the PC, overriding the incrementer.

**Stack Pointer (SP):** The stack pointer contains the 16-bit address of the current top of a stack located in external system RAM memory. The external stack memory is organized as a last-in, first-out (LIFO) file. The stack allows simple implementation of multiple level interrupts, virtually unlimited subroutine nesting and simplification of many types of data manipulation.

**Index Registers (IX and IY):** The two 16-bit index registers hold a 16-bit base address used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer.

**Interrupt Page Address Register (I):** The MPU800 CPU can indirectly call any memory location in response to a mode 2 interrupt. The I register is used to store the high-order 8 bits of the address. The low-order 8 bits are supplied by the interrupting peripheral. This feature allows interrupt routines to be dynamically located anywhere in memory with minimal access time to the routine.

**Memory Refresh Register (R):** The MPU800 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. This 8-bit register is automatically incremented after each instruction fetch. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer.

## ACCUMULATORS AND FLAG REGISTERS

The CPU includes two 8-bit accumulators and two associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operation. The flag register indicates specific conditions for 8-bit or 16-bit operations.

### FLAG REGISTERS (F, F')

The two MPU800 flag registers each contain six status bits that are set or reset (cleared) by various CPU operations *(Figure 8)*. Four of these bits (carry, zero, sign, and parity/overflow flags) can be tested by the programmer. The descriptions of the flags follow.

**Carry Flag (C):** This flag is set by the carry from the highest order bit of the accumulator during an add instruction or a borrow generated during a subtraction instruction. Specific shift and rotate instructions also affect this bit.

**Zero Flag (Z):** This flag is set when a zero is loaded into the accumulator as a result of an operation. Otherwise it remains clear.

**Sign Flag (S):** This flag stores the state of bit 7 (the sign bit) in the accumulator after an arithmetic operation. This flag is intended to be used with signed numbers.

**Parity/Overflow Flag (P/V):** During logical operations this flag is set when the parity of the result is even and reset when it is odd. It represents overflow when signed two's complement arithmetic operations are performed. An overflow occurs when the resultant of a two's complement operation (in the accumulator) is out of range.

The two non-testable flag register bits used for BCD arithmetic are:

**Half Carry (H):** The flag indicates a BCD carry or borrow result from the least significant four bits of an operation; when using the DAA (Decimal Adjust Accumulator Instruction), it is used to correct the result of a previously packed decimal add or subtract.

**Add/Subtract Flag (N):** Since the algorithm for correcting BCD operations is different for addition or subtraction, this flag specifies what type of instruction was executed last in order that the DAA operation will be correct for either operation.

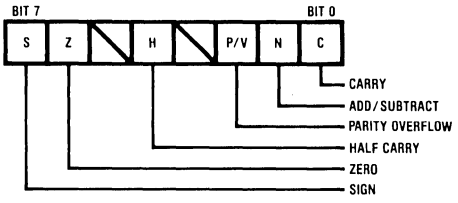



FIGURE 8. Flag Register

## INTERRUPTS

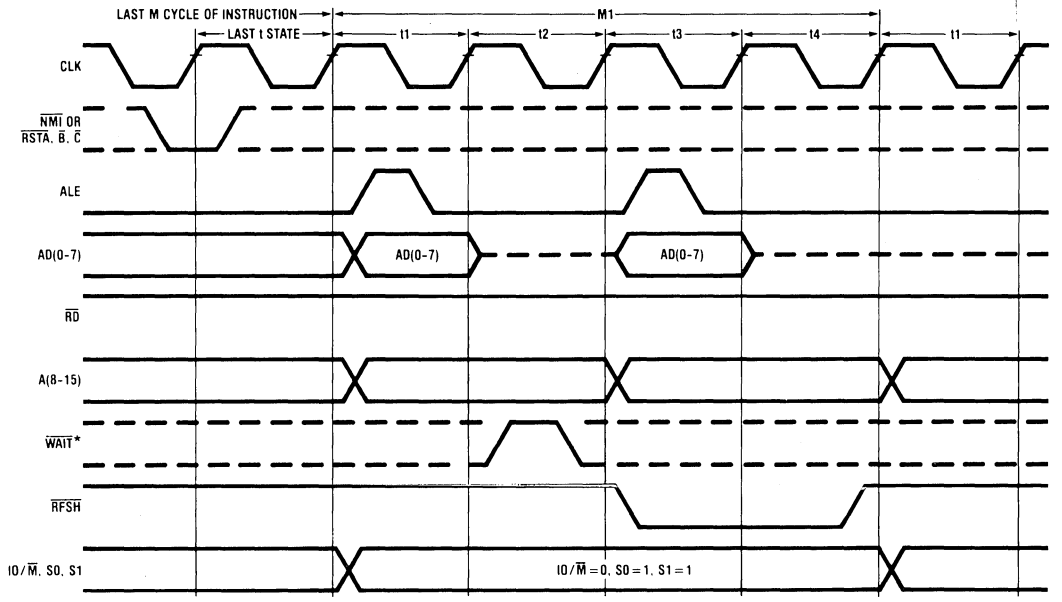
The MPU800 has five interrupt/restart inputs, four are maskable ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and $\overline{INTR}$) and one is non-maskable ($\overline{NMI}$). $\overline{NMI}$, having the highest priority of all interrupts, is always serviced and cannot be disabled by the user. After recognizing an active input on $\overline{NMI}$, the CPU stops before the next instruction, pushes the PC onto the stack, and jumps to address X'0066, where the user's interrupt service routine is located (i.e., restart to memory location X'0066). $\overline{NMI}$ is intended for interrupts requiring immediate attention, such as power-down, control panel, etc. $\overline{RSTA}$, $\overline{RSTB}$ and $\overline{RSTC}$ are restart inputs, which, if enabled, execute a restart to memory location X'003C, X'0034, and X'002C, respectively. Note that the CPU response to the $\overline{NMI}$ and $\overline{RST}$ ($\overline{A}$, $\overline{B}$, $\overline{C}$) request input is basically identical. Unlike $\overline{NMI}$, however, restart request inputs must be enabled.

*Figure 9* illustrates $\overline{NMI}$ and $\overline{RST}$ interrupt machine cycles. M1 cycle will be a dummy opcode fetch cycle followed by M2 and M3 which are stack push operations. The following instruction will then start from the interrupts restart location.

The MPU800 also provides one more general purpose interrupt request input, $\overline{INTR}$. When enabled, the CPU responds to $\overline{INTR}$ in one of the three modes defined by instruction IM0, IM1, and IM2 for modes 0, 1 and 2, respectively. Following reset, the CPU automatically sets itself in mode ).

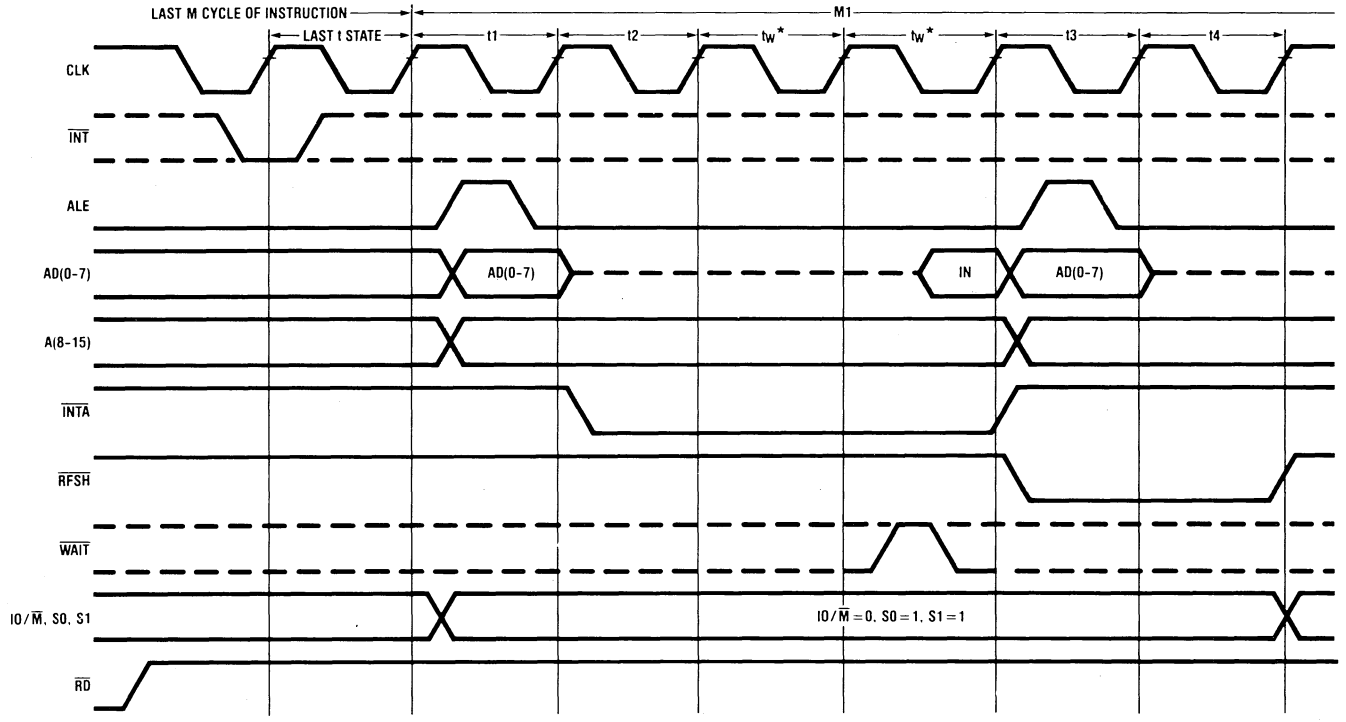
**Interrupt (INTR) Mode 0;** Similar to INS8080A mode. The CPU responds to an interrupt request by providing an $\overline{INTA}$ (interrupt acknowledge) strobe, which can be used to gate an instruction from a peripheral onto the data bus. Two wait states are automatically inserted by the CPU during the first $\overline{INTA}$ cycle to allow the interrupting device (or its controller) ample time to gate the instruction and determine external priorities. *(Figure 10).* This can be any instruction from one to four bytes. The most popular instruction would be a one-byte call (restart instruction) or a three-byte call (CALL NN instruction). If it is a three-byte call, the CPU issues a total of three $\overline{INTA}$ strobes. The last two read NN (which do not include wait states).

**Interrupt ($\overline{INTR}$) Mode 1:** Similar to the restart interrupts except the restart location is X'0038 *(Figure 9).*




* This is the only machine cycle that does not have an $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ strobe but will accept a wait strobe.

FIGURE 9. Non-Maskable and Restart Interrupt Machine Guide




*$t_W$ is the CPU generated WAIT state in response to an interrupt request.

**FIGURE 10. Interrupt Acknowledge Machine Cycle**

**Interrupt ($\overline{INTR}$) Mode 2:** With this mode, the programmer maintains a table that contains the 16-bit starting address of every interrupt service routine. This table may be located anywhere in memory. When the mode 2 interrupt is accepted *(Figure 11)*, a 16-bit pointer must be formed to obtain the desired interrupt service routine starting address from the table. The upper 8 bits of this pointer are from the contents of the I register, which has been previously loaded with the desired value by the programmer. The lower 8 bits of the pointer are supplied by the interrupting device with the low-order bit forced to zero. The pointer is used to get two adjacent bytes from the interrupt service routine starting address table to complete the 16-bit service routine starting address. The first byte of each entry in the table is the least significant (low-order) portion of the address. The programmer must obviously fill this table with the desired addresses before any interrupts are to be accepted.

Note that this table can be changed at any time to allow peripherals to be serviced by different service routines. Once the interrupting device supplies the lower portion of the pointer, the CPU automatically pushes the program counter onto the stack, obtains the starting address from the table and does a jump to this address.

The interrupts have fixed priorities built into the MPU800 as:

| | |
|---|---|
| $\overline{NMI}$ | (Highest Priority) |
| $\overline{RSTA}$ | |
| $\overline{RSTB}$ | |
| $\overline{RSTC}$ | |
| $\overline{INTR}$ | (Lowest Priority) |

## ENABLING INTERRUPTS

$\overline{NMI}$, being a non-maskable interrupt request, is executed as it occurs and can never be disabled.

The maskable interrupt inputs ($\overline{RSTA}$, $\overline{RSTB}$, $\overline{RSTC}$, and INTR) are enabled under program control through the use of the interrupt control register and enable/disable interrupt instruction.

The appropriate interrupt control bits in 4-bit control register (IEA, IEB, IEC, and IEI) must be enabled in conjunction with IFF1 and IFF2, before the maskable $\overline{INTR}$ and $\overline{RST}$ A, B, C can be accepted by the CPU.

The interrupt control register is an on-chip write only output port located at port address X'BB. It can only be written to by either the OUT (C), r or OUT (N), A instructions (for example OUTI instruction will not affect Interrupt Control Register). Its contents are:

| Bit | Name | Function |
|---|---|---|
| 0 | IEI | Interrupt Enable for $\overline{INTR}$ |
| 1 | IEC | " " " $\overline{RSTC}$ |
| 2 | IEB | " " " $\overline{RSTB}$ |
| 3 | IEA | " " " $\overline{RSTA}$ |

For example: In order to enable $\overline{RSTB}$, CPU interrupts must be enabled and IEB must be set.

At reset, IEI bit is set and other mask bits, IEA, IEB, IEC are cleared. This maintains the software compatibility between MPU800 and INS8080A (or Z80A).

Execution of an IO block move instruction will not affect the state of the interrupt control bits. The only two instructions that will modify this write only register are OUT (C), r and OUT (N), A.

## POWER-SAVE FEATURE

The MPU800 provides a unique power-save mode by the means of the $\overline{PS}$ pin. $\overline{PS}$ input is sampled at the last t state of the last M cycle of an instruction. After recognizing an active (low) level on $\overline{PS}$, the MPU800 stops its internal clocks, thereby reducing its power dissipation to one half of operating power, yet maintaining all register values and internal control status. The MPU800 keeps its oscillator running, and makes the CLK signal available to the system. When in power-save the ALE strobe will be stopped high and the address lines [AD(0-7), A(8-15)] will indicate the next machine address. When $\overline{PS}$ is returned high, the opcode fetch (or M1 cycle) of the CPU begins in a normal manner. Note this M1 cycle could also be an interrupt acknowledge cycle if the MPU800 was interrupted simultaneously with $\overline{PS}$. *Figure 12* illustrates the power-save feature.

In the event $\overline{BREQ}$ is asserted (low) at the end of an instruction cycle and $\overline{PS}$ is active simultaneously, the following occurs:

1. The MPU800 will go into $\overline{BACK}$ cycle
2. Upon completion of $\overline{BACK}$ cycle if $\overline{PS}$ is still active the CPU will go into power-save mode.

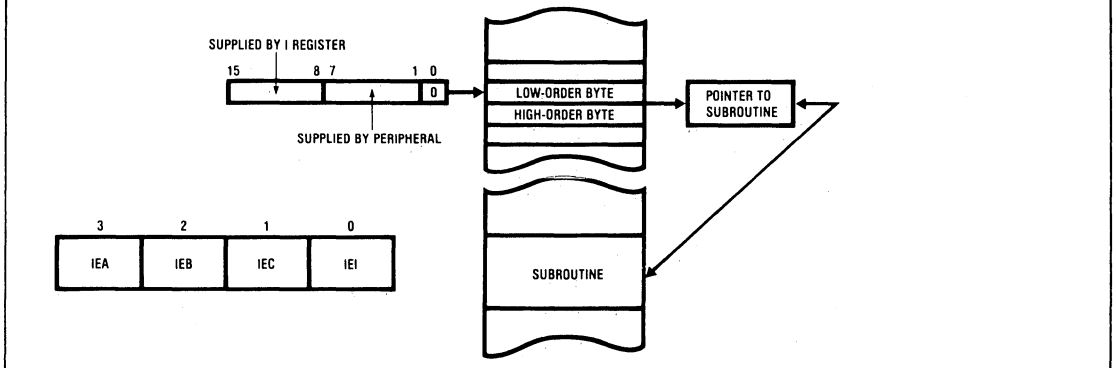



**FIGURE 11. Interrupt Mode 2**

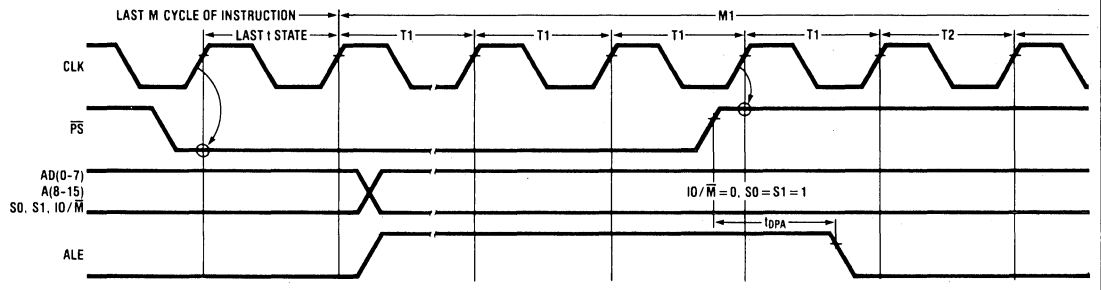



**FIGURE 12. MPU800 Power-Save**

## INSTRUCTION SET

In the following instruction set listing, the notation used is shown below.

b: Used in instructions employing bit mode addressing to designate one bit in a register or memory location.

cc: Designates condition codes used in conditional Jumps, Calls, and Return instructions; may be
NZ = Non Zero (Z Flag = 0)
Z = Zero (Z Flag = 1)
NC = Non Carry (C Flag = 0)
C = Carry (C Flag = 1)

PO = Parity Odd or No Overflow (P/V = 0)
PE = Parity Even or Overflow (P/V = 1)
P = Positive (S = 0)
M = Negative (S = 1)

d: Used in instructions employing relative or indexed modes of addressing to designate 8-bit signed 2's complement displacement.

kk: Subset of cc condition codes used in conjunction with conditional relative jumps; may be NZ, Z, NC or C.

m1: Used in instructions employing register indirect or indexed modes of addressing; may be (HL), (IX + d) or (IY + d).

m2: Used in instructions employing register indirect or direct modes of addressing; may be (BC), (DE), or (nn).

n: Any 8-bit binary number.

nn: Any 16-bit binary number.

pp: Used in 16-bit arithmetic instructions employing register modes of addressing; may be BC, DE, SP, or register designated as destination operand.

qq: Used in instructions employing register modes of addressing; may be BC, DE, HL, AF, IX, or IY.

r: Used in instructions employing register mode of addressing; may be A, B, C, D, E, H, or L.

rr: Used in instructions employing register mode of addressing; may be BC, DE, HL, SP, IX, or IY.

ss: Used in instructions employing register mode of addressing; may be HL, IX, or IY.

T: Used to restart instructions employing modified page zero addressing mode; may take on hex values of 0, 8, 10, 18, 20, 28, 30, or 38.

$X_L$: Subscript L indicates the high order byte of a 16-bit register.

$X_H$: Subscript H indicates the high-order byte of a 16-bit register.

( ): Parentheses indicate the contents are considered a pointer to a memory or I/O location.

## 8-BIT LOADS

### REGISTER TO REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| LD $r_d$, $r_s$ | Load register $r_d$ with $r_s$ | $r_d \leftarrow r_s$ |
| LD A,I | Load ACC with register I | A←I |
| LD I, A | Load register I with ACC | I←A |
| LD A, r | Load ACC with register R | A←r |
| LD r, A | Load register R with ACC | r←A |
| LD r, n | Load register r with immediate data n | r←n |

### REGISTER TO MEMORY

| Mnemonic | Description | Operation |
|---|---|---|
| LD m1, r | Load memory from register r | m1←r |
| LD, m2, A | Load memory from ACC | m2←A |
| LD m1, n | Load memory with immediate data n | m1←n |

### MEMORY TO REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| LD r, m1 | Load register r from memory | r←m1 |
| LD A, m2 | Load ACC from memory | A←m2 |

## 16-BIT LOADS

### REGISTER TO REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| LD rr, nn | Load register rr with immediate data nn | rr←nn |
| LD SP, ss | Load SP register with register ss | SP←ss |

### REGISTER TO MEMORY

| Mnemonic | Description | Operation |
|---|---|---|
| LD (nn), rr | Load memory location nn with 16 bit register rr | $(nn)\leftarrow rr_L$<br>$(nn+1)\leftarrow rr_H$ |
| PUSH qq | Push contents of 16-bit register qq onto memory stack | $(SP-1)\leftarrow qq_H$<br>$(SP-2)\leftarrow qq_L$<br>SP←SP−2 |

### MEMORY TO REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| LD rr, (nn) | Load 16-bit register rr from memory location nn | $rr_L\leftarrow(nn)$<br>$rr_H\leftarrow(nn+1)$ |
| POP qq | Pop contents of stack to register qq | $qq_L\leftarrow(SP)$<br>$qq_H\leftarrow(SP+1)$<br>SP←SP+2 |

## 8-BIT ARITHMETIC

### REGISTER ADDRESSED ARITHMETIC

| Mnemonic | Description | Operation |
|---|---|---|
| ADD A, r | Add contents of register r to ACC | A←A+r |
| ADC, A, r | Add with carry contents of register r to ACC | A←A+r+CY |
| SUB r | Subtract contents of register r from ACC | A←A−r−r |
| SBC A, r | Subtract contents of contents of register r from ACC | A←A−r−CY |
| AND r | Logically AND contents of register r with ACC | A←A ∧ r |
| OR r | Logically AND contents of register r with ACC | A←A ∨ r |
| XOR r | Exclusive OR contents of register r with ACC | A←A⊻r |
| CP r | Compare contents of register r to ACC | A:r<br>Z flag←1<br>if A = r<br>else<br>Z Flagfi0 |
| INC r | Increment contents of register r | r←r+1 |
| DEC r | Decrement contents of register r | r←r−1 |
| DAA | Decimal adjust ACC | (ACC adjust for BCD) |
| CPL | Complement ACC (1's complement) | A←A |
| NEG | Negate ACC (2's complement) | A←0−A |
| CCF | Complement carry flag | CY←CY |
| SCF | Set carry flag | CY←1 |

### IMMEDIATE ADDRESSING MODE ARITHMETIC

| Mnemonic | Description | Operation |
|---|---|---|
| ADD A, n | Add number n to ACC | A←A+n |
| ADC A, n | Add with carry number n to ACC | A←A+n+CY |
| SUB n | Subtract number n from ACC | A←A−n |
| SBC A, n | Subtract with carry number n from ACC | A←A−n−CY |
| AND n | AND number n with ACC | A←A ∧ n |
| OR n | OR number n with ACC | A←A ∨ n |
| XOR n | Exclusive OR number n with ACC | A←A⊻n1 |
| CP n1 | Compare number n to ACC | A: n1<br>Z flag←1<br>if A = n<br>else<br>Z Flag←0 |

### MEMORY ADDRESSED ARITHMETIC

| Mnemonic | Description | Operation |
|---|---|---|
| ADD A, m1 | Add memory to ACC | A←A+m1 |
| ADC A, m1 | Add with carry memory to ACC | A←A+m1+CY |
| SUB m1 | Subtract memory from ACC | A←A−m1 |
| SBC A, m1 | Subtract with carry memory from ACC | A←A−m1−CY |
| AND m1 | AND memory with ACC | A←A∧m1 |
| OR m1 | OR memory with ACC | A←A∨m1 |
| XOR m1 | Exclusive OR memory with ACC | A←A⊻m1 |
| CP m1 | Compare memory with ACC | A: m1<br>Z flag←1<br>if A = r<br>else<br>Z Flag←0 |
| INC m1 | Increment memory | m1←m1+1 |
| DEC m1 | Decrement memory | m1←m1−1 |

## 16-BIT ARITHMETIC

### REGISTER ADDRESSED ARITHMETIC

| Mnemonic | Description | Operation |
|---|---|---|
| ADD ss, pp | Add 16-bit register pp to 16-bit register ss | ss←ss+pp |
| ADC HL, pp | Add with cary 16-bit register pp to HL | HL←HL+pp+CY |
| SBC HL, pp | Subtract with carry 16-bit register pp from HL | HL←HL−pp−CY |
| INC rr | Increment 16-bit register rr | rr←rr+1 |
| DEC rr | Decrement 16-bit register rr | rr←rr−1 |

SECTION IX

## BIT SET, RESET, AND TEST

### REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| SET b, r | Set bit in register r | $r_b \leftarrow 1$ |
| RES b, r | Reset bit in register r | $r_b \leftarrow 0$ |
| BIT b, r | Test bit in register r | $Z \leftarrow r_b$ |

### MEMORY

| Mnemonic | Description | Operation |
|---|---|---|
| Set b, m1 | Set bit in memory location m1 | m1b←1 |
| RES b, m1 | Reset bit b in memory location m1 | m1b←0 |
| BIT b, m1 | Test bit b in memory location m1 | Z←m1b |

## EXCHANGES

### REGISTER/REGISTER

| Mnemonic | Description | Operation |
|---|---|---|
| EX DE, HL | Exchange contents of DE and HL register | DE↔HL |
| EX AF, AF1 | Exchange contents of A and F registers with A1 and F1 registers | AF↔AF′ |
| EXX | Exchange contents of BC, DE and HL registers with corresponding alternate registers | BC↔BC′<br>DE↔DE′<br>HL↔HL′ |

### REGISTER/MEMORY

| Mnemonic | Description | Operation |
|---|---|---|
| EX (SP), ss | Exchange top of stack with 16-bit register ss | $(SP) \leftrightarrow ss_L$<br>$(SP+1) \leftrightarrow ss_H$ |

## MEMORY BLOCK MOVES AND SEARCHES

Block move and search instructions (such as LDIR and INIR) Insert a dummy instruction fetch after each cycle to keep refresh going.

### SINGLE OPERATIONS

| Mnemonic | Description | Operation |
|---|---|---|
| LDI | Move data from memory location (HL) to memory location (DE), increment memory pointers, and decrement byte counter BC. | (DE)←(HL)<br>DE←DE + 1<br>HL←HL + 1<br>BC←BC−1 |
| LDD | Move data from memory location (HL) to memory location (DE), and decrement memory pointer and byte counter BC. | (DE)←(HL)<br>DE←DE−1<br>HL←HL−1<br>BC←HL−1 |
| CPI | Compare data in memory location (HL) to ACC, increment memory pointer and decrement byte counter BC. | A−(HL)<br>HL←HL + 1<br>BC←BC−1 |
| CPD | Compare data in memory location (HL) to ACC and decrement memory pointer and byte counter BC. | A−(HL)<br>HL←HL−1<br>BC←BC−1 |

### REPEAT OPERATIONS

| Mnemonic | Description | Operation |
|---|---|---|
| LDIR | Move data from memory location (HL) to memory location (DE), increment memory pointers, decrement byte counter BC, until BC = 0 | (DE)←(HL)<br>DE←DE + 1<br>HL←HL + 1<br>BC←BC−1<br>Repeat until BC = 0 |
| LDDR | Move data from memory location (HL) to memory location (DE), decrement memory pointers and byte counter BC, repeat until BC = 0 | (DE)←(HL)<br>DE←DE−1<br>HL←HL−1<br>BC←BC−1<br>Repeat until BC = 0 |
| CPIR | Compare data in memory location (HL) to ACC, increment memory pointer, decrement byte counter BC, repeat until BC = 0 or (HL) = A | A−(HL)<br>HL←HL + 1<br>BC←BC−1<br>Repeat until BC = 0 or (HL) = A |
| CPDR | Compare data in memory location (HL) to ACC, decrement memory pointer and byte counter BC, repeat until BC = 0 or (HL) = A | A−(HL)<br>HL←HL−1<br>BC←BC−1<br>Repeat until BC = 0 or (HL) = A |

## INPUT/OUTPUT

Due to the multiplexed bus structure, the MPU800 handles the address bus differently than the Z80 during input and output instructions. The MPU800 duplicates the port address on the upper and lower halves of the address.

| Mnemonic | Description | Operation |
|---|---|---|
| IN A, (n) | Input from I/O device at address n to ACC | A←(n) |
| OUT (n), A | Output to I/O device at address n from ACC | (n)←A |
| IN r, (C) | Input from I/O device at address (C) to register | r←(C) |
| OUT (C), r | Output to I/O device at address (C) from register | (C)←r |
| INI | Input from I/O device at address (C) to memory location (HL), increment pointer, and decrement B counter | (HL)←(C)<br>HL←HL + 1<br>B←B−1 |

| Mnemonic | Description | Operation |
|---|---|---|
| OUTI | Output to I/O at address (C) from memory location (HL), increment pointer, and decrement B counter | (C)←(HL)<br>HL←HL + 1<br>B←B−1 |
| IND | Input from I/O device at address (C) to memory location (HL) and decrement pointer, and B counter | (HL)←(C)<br>HL←HL−1<br>B←B−1 |
| OUTD | Output to I/O device at address (C) from memory location (HL) and decrement pointer B counter | (C)←(HL)<br>HL←HL−1<br>B←B−1 |
| INIR | Output to I/O device at at address (C) to memory location (HL), increment pointer, decrement B counter, and repeat until B = 0 | (HL)←C<br>HL←HL + 1<br>B←B−1<br>Repeat until B = 0 |
| OUTIR | Output to I/O device at address (C) from memory location (HL), increment pointer, decrement B counter, and repeat until B = 0 | (C)←(HL)<br>HL←HL + 1<br>B←B−1<br>Repeat until B = 0 |
| INDR | Input from I/0 device at address (C) to memory location (HL), decrement pointer and B counter, and repeat until B = 0 | (HL)←(C)<br>HL←HL−1<br>B←B−1<br>Repeat until B = 0 |
| OUTDR | Output to I/O device at address (C) from memory location (HL), decrement pointer and B counter, and repeat until B = 0 | (C)←(HL)<br>HL←HL−1<br>B←B−1<br>Repeat until B = 0 |

## CPU CONTROL

| Mnemonic | Description | Operation |
|---|---|---|
| NOP | No operation | |
| HALT* | Halt processor | |
| DI | Disable Interrupts | |
| EI | Enable Interrupts | |
| IM 0 | Set Interrupt Mode 0 | |
| IM 1 | Set Interrupt Mode 1 | |
| IM 2 | Set Interrupt Mode 2 | |

*Halt instruction locks CPU into an endless cycle of instruction fetches until CPU is reset or interrupted. Therefore dynamic memory refresh continues to run.

## PROGRAM CONTROL

### JUMPS

| Mnemonic | Description | Operation |
|---|---|---|
| JP nn | Unconditional jump direct to nn | PC←nn |
| JP (ss) | Unconditional jump indirect via ss register | PC←ss |
| JP cc, nn | Conditionally jump direct to nn if cc is true | If cc true, PC←nn, else continue |
| JR d | Unconditional jump to PC + d | PC←PC + d |
| JR kk, d | Conditionally jump PC + d if kk is true | if kk true, PC←PC + d |
| DJNZ, d | Decrement B register and jump to PC + d if B ≠ 0, otherwise continue | B←B−1<br>if B = 0<br>PC←PC + d |

### CALLS

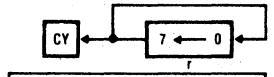
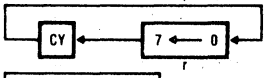
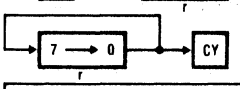
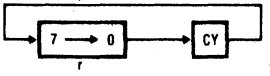
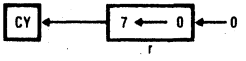
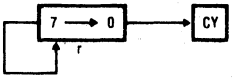
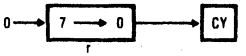
| Mnemonic | Description | Operation |
|---|---|---|
| CALL nn | Unconditional call to subroutine at location nn | $(SP-1)\leftarrow PC_H$<br>$(SP-2)\leftarrow PC_L$<br>PC←nn |
| CALL cc, nn | Conditional call to subroutine at location nn if cc true | if cc true,<br>$(SP-1)\leftarrow PC_H$<br>$(SP-2)\leftarrow PC_L$<br>PC←nn, else continue |

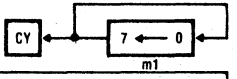
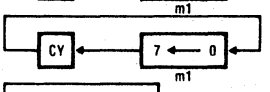
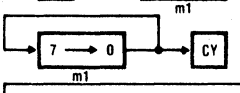
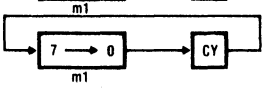
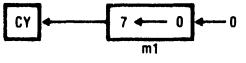
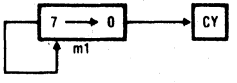
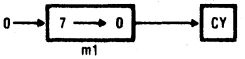
### RETURNS

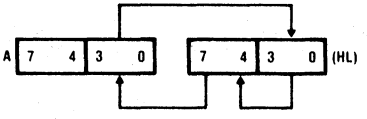
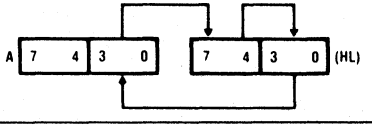
| Mnemonic | Description | Operation |
|---|---|---|
| RET | Unconditional return from subroutine | $PC_L\leftarrow(SP)$<br>$PC_H\leftarrow(SP+1)$ |
| RET cc | Conditional return from subroutine | If cc true:<br>$PC_L\leftarrow(SP)$<br>$PC_H\leftarrow(SP+1)$<br>else continue |
| RETI | Return from interrupt | $PC_L\leftarrow(SP)$<br>$PC_H\leftarrow(SP+1)$ |
| RETN | Return from non-maskable interrupt | $PC_L\leftarrow(SP)$<br>$PC_H\leftarrow(SP+1)$<br>Restore interrupt enable status |

### RESTARTS

| Mnemonic | Description | Operation |
|---|---|---|
| RST T | Interrupt to location T | $(SP-1)\leftarrow PC_H$<br>$(SP-2)\leftarrow PC_L$<br>PC←T |

| REGISTER MNEMONIC | DESCRIPTION | OPERATION |
|---|---|---|
| RLC r | ROTATE REGISTER r LEFT CIRCULAR |  |
| RL r | ROTATE REGISTER r LEFT THROUGH CARRY |  |
| RRC r | ROTATE REGISTER r RIGHT CIRCULAR |  |
| RR r | ROTATE REGISTER r RIGHT THROUGH CARRY |  |
| SLA r | SHIFT REGISTER r LEFT ARITHMETIC |  |
| SRA r | SHIFT REGISTER r RIGHT ARITHMETIC |  |
| SRL r | SHIFT REGISTER r RIGHT LOGICAL |  |

| MEMORY MNEMONIC | DESCRIPTION | OPERATION |
|---|---|---|
| RLC m1 | ROTATE MEMORY LEFT CIRCULAR |  |
| RL m1 | ROTATE MEMORY LEFT THROUGH CARRY |  |
| RRC m1 | ROTATE MEMORY RIGHT CIRCULAR |  |
| RR m1 | ROTATE MEMORY RIGHT THROUGH CIRCULAR |  |
| SLA m1 | SHIFT MEMORY LEFT ARITHMETIC |  |
| SRA m1 | SHIFT MEMORY RIGHT ARITHMETIC |  |
| SRL m1 | SHIFT MEMORY RIGHT LOGICAL |  |

| REGISTER/MEMORY MNENONIC | DESCRIPTION | OPERATION |
|---|---|---|
| RLD | ROTATE DIGIT LEFT AND RIGHT BETWEEN ACC AND MEMORY (HL) |  |
| RRD | ROTATE DIGIT RIGHT AND LEFT BETWEEN ACC AND MEMORY (HL) |  |

## ROTATE AND SHIFT

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -0.3V to $V_{CC}$ + 0.3V
Maximum $V_{CC}$ . . . . . 7V
Power Dissipation . . . . . 1W
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

## DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to +70°C, $V_{CC} = 5V \pm 10\%$, GND = 0V, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logical 1 Input Voltage | | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Logical 0 Input Voltage | | 0 | | 0.2 $V_{CC}$ | V |
| $V_{HY}$ | Hysteresis at RESET IN input | $V_{CC} = 5V$ | 0.25 | 0.5 | | V |
| $V_{OH1}$ | Logical 1 Output Voltage | $I_{OUT} = -1.0$ mA | 2.4 | | | V |
| $V_{OH2}$ | Logical 1 Output Voltage | $I_{OUT} = -10$ µA | $V_{CC}$-.05 | | | V |
| $V_{OL1}$ | Logical 0 Output Voltage | $I_{OL} = 2$ mA | 0 | | 0.4 | V |
| $V_{OL2}$ | Logical 0 Output Voltage | $I_{OUT} = 10$ µA | 0 | | 0.1 | V |
| $I_{IL}$ | Input Leakage Current | $0 \le V_{IN} \le V_{CC}$ | -10.0 | | 10.0 | µA |
| $I_{OL}$ | Output Leakage Current | $0 \le V_{IN} \le V_{CC}$ | -10.0 | | 10.0 | µA |
| $I_{CCA}$ | Active Supply Current | $I_{OUT} = 0$, $f_{(XIN)} = 5$ MHz | | 10 | 15 | mA |
| $I_{CCA}$ | Active Supply Current | $I_{OUT} = 0$, $f_{(XIN)} = 8$ MHz | | 15 | 21 | mA |
| $I_{CCQ}$ | Quiescent Current | $f_{(XIN)} = 0$ MHz | | 2 | 4 | mA |
| $I_{CPS}$ | Power-Save Current | $f_{(XIN)} = 5.0$ MHz | | 5 | | mA |
| $C_{IN}$ | Input Capacitance | | | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | | 8 | 12 | pF |
| $V_{CC}$ | Power Supply Voltage | Note 2 | 2.4 | 5 | 6 | V |

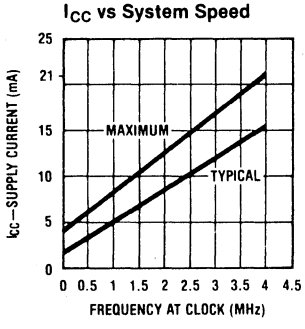
**Note 1:** Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

**Note 2:** CPU operation at lower voltages will reduce the maximum operating speed. DC and AC electrical characteristics at voltages other than 5V ± 10% are forthcoming.

**Preliminary (not tested)**

| Max CPU Speed* | MPU800-1 | MPU800 | MPU800-4 | Units |
|---|---|---|---|---|
| @2.4V | | 500 | 500 | kHz |
| @3.0V | | 1 | 1 | MHz |

*Speed of CPU is expressed in clock speed, not crystal speed.




## AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 10\%$, GND = 0V

| Symbol | Parameter | MPU800-1 | | MPU800 | | MPU800-4 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_x$ | Period at XIN and XOUT Pins | 500 | 31250 | 200 | 31250 | 125 | 31250 | ns |
| T | Period at Clock Output (= 2 $t_x$) | 1000 | 62500 | 400 | 62500 | 250 | 62500 | ns |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

**AC ELECTRICAL CHARACTERISTICS** (Continued) $V_{CC} = 5V \pm 10\%$, GND = 0V

| Symbol | Parameter | MPU800-1 | | MPU800 | | MPU800-4 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_x$ | Period at XIN and XOUT Pins | 500 | 31250 | 200 | 31250 | 125 | 31250 | ns | |
| T | Period at Clock Output ($= 2\ t_x$) | 1000 | 62500 | 400 | 62500 | 250 | 62500 | ns | |
| $t_R$ | Clock Rise Time | | 110 | | 110 | | 75 | ns | Measured from 10%-90% of signal |
| $t_F$ | Clock Fall Time | | 60 | | 60 | | 40 | ns | Measured from 10%-90% of signal |
| $t_L$ | Clock Low Time | 490 | | 190 | | 95 | | ns | 50% duty cycle, square wave input on XIN |
| $t_H$ | Clock High Time | 450 | | 150 | | 80 | | ns | 50% duty cycle, square wave input on XIN |
| $t_{ACC\ (RD)}$ | ALE to Valid Data | | 1375 | | 500 | | 300 | ns | Add t for each $\overline{WAIT}$ STATE<br>Add t/2 for memory read cycles |
| $t_{AFR}$ | $\overline{AD}$(0-7) Float after $\overline{RD}$ Falling | | 0 | | 0 | | 0 | $\overline{ns}$ | |
| $t_{BABE}$ | $\overline{BACK}$ Rising to Bus Enable | | 1000 | | 400 | | 250 | ns | |
| $t_{BABF}$ | $\overline{BACK}$ Falling to Bus Float | | 50 | | 50 | | 50 | ns | |
| $t_{BACL}$ | $\overline{BACK}$ Falling to CLK Falling | 425 | | 125 | | 55 | | ns | |
| $t_{BRH}$ | $\overline{BREQ}$ Hold Time | 0 | | 0 | | 0 | | ns | |
| $t_{BRS}$ | $\overline{BREQ}$ Set-Up Time | 100 | | 50 | | 35 | | ns | |
| $t_{CAF}$ | Clock Falling to ALE Falling | 0 | 30 | 0 | 30 | 0 | 35 | ns | |
| $t_{CAR}$ | Clock Rising to ALE Rising | 0 | 100 | 0 | 100 | 0 | 75 | ns | |
| $t_{DAI}$ | ALE Falling to $\overline{INTA}$ Falling | 530 | | 230 | | 100 | | ns | |
| $t_{DAR}$ | ALE Falling to $\overline{RD}$ Falling | 525 | 575 | 225 | 250 | 125 | 160 | ns | |
| $t_{DAW}$ | ALE Falling to $\overline{WR}$ Falling | 990 | 1010 | 390 | 410 | 220 | 250 | ns | |
| $t_{D(BACK)1}$ | ALE Falling to $\overline{BACK}$ Falling | 2500 | | 1000 | | 600 | | ns | Add t for each $\overline{WAIT}$ state<br>Add t for opcode fetch cycles |
| $t_{D(BACK)2}$ | $\overline{BREQ}$ Rising to $\overline{BACK}$ Rising | 500 | 1600 | 200 | 700 | 125 | 475 | ns | |
| $t_{D(I)}$ | ALE Falling to $\overline{INTR}$, $\overline{NMI}$, $\overline{RSTA\text{-}C}$, $\overline{PS}$, $\overline{BREQ}$ Inputs Valid | | 1375 | | 475 | | 250 | ns | Add t for each $\overline{WAIT}$ state<br>Add t for opcode fetch cycles |
| $t_{DPA}$ | Rising $\overline{PS}$ to Falling ALE | 500 | 1550 | 200 | 650 | 125 | 475 | ns | See *Figure 12* also |
| $t_{D(RFSH)}$ | Falling ALE to Falling $\overline{RFSH}$ | 1500 | | 600 | | 325 | | ns | Add t for each $\overline{WAIT}$ state |
| $t_{D(WAIT)}$ | ALE Falling to $\overline{WAIT}$ input Valid | | 550 | | 250 | | 125 | ns | |
| $t_{H(ADH)1}$ | A(8-15) Holt Time During Opcode Fetch | 0 | | 0 | | 0 | | ns | |
| $t_{H(ADH)2}$ | A(8-15) Hold Time During Memory or IO, $\overline{RD}$ and $\overline{WR}$ | 400 | | 100 | | 60 | | ns | |
| $t_{H(ADL)}$ | AD(0-7) Hold Time | 400 | | 100 | | 50 | | ns | |
| $t_{H(WD)}$ | Write Data Hold Time | 400 | | 100 | | 50 | | ns | |
| $_{INH}$ | Interrupt Hold Time | 0 | | 0 | | 0 | | ns | |
| $t_{INS}$ | Interrupt Set-Up Time | 100 | | 50 | | 35 | | ns | |
| $t_{NMI}$ | Width of NMI Input | 50 | | 30 | | 20 | | ns | |
| $t_{RDH}$ | Data Hold after Read | 0 | | 0 | | 0 | | ns | |
| $t_{RFL}$ | $\overline{RFSH}$ Rising to ALE Rising | | −100 | | −100 | | −70 | ns | Negative number means ALE occurs first |

## AC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = 5V \pm 10\%$, GND = OV

| Symbol | Parameter | MPU800-1 | | MPU800 | | MPU800-4 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{RL(MR)}$ | $\overline{RD}$ Rising to ALE Rising (Memory Read) | 450 | | 150 | | 85 | | ns | |
| $t_{RL(OP)}$ | $\overline{RD}$ Rising to ALE Rising Opcode | | −75 | | −65 | | −55 | ns | |
| $T_{S(AD)}$ | AD(0-7) Set-Up Time | 300 | | 80 | | 40 | | ns | |
| $t_{S(ALE)}$ | A98-15), SO, SI, IO/$\overline{M}$ Set-Up Time | 350 | | 100 | | 50 | | ns | |
| $t_{S(WD)}$ | Write Data Set-Up Time | 385 | | 85 | | 50 | | ns | |
| $t_{W(ALE)}$ | ALE Width | 430 | | 130 | | 75 | | ns | |
| $t_{WH}$ | $\overline{WAIT}$ Hold Time | 0 | | 0 | | 0 | | ns | |
| $t_{W(I)}$ | Width of $\overline{INTR}$, $\overline{RSTA-C}$, $\overline{PS}$, $\overline{BREQ}$ | 500 | | 200 | | 125 | | ns | |
| $t_{W(INTA)}$ | $\overline{INTA}$ Strobe Width | 1000 | | 400 | | 200 | | ns | Add two t states for first $\overline{INTA}$ of each interrupt response string Add t for each $\overline{WAIT}$ state |
| $t_{WL}$ | $\overline{WR}$ Rising to ALE Rising | 450 | | 150 | | 90 | | ns | |
| $t_{W(RD)}$ | Read Strobe Width During Opcode Fetch | 1000 | | 400 | | 225 | | ns | Add t for each $\overline{WAIT}$ State Add t/2 for Memory Read Cycles |
| $t_{W(RFSH)}$ | Refresh Strobe Width | 1925 | | 725 | | 400 | | ns | |
| $t_{WS}$ | $\overline{WAIT}$ Set-Up Time | 100 | | 50 | | 35 | | ns | |
| $t_{W(WAIT)}$ | $\overline{WAIT}$ Input Width | 550 | | 250 | | 175 | | ns | |
| $t_{W(WR)}$ | Write Strobe Width | 1000 | | 400 | | 220 | | ns | Add t for each $\overline{WAIT}$ state |
| $t_{XCF}$ | XIN to Clock Falling | 25 | 55 | 25 | 55 | 25 | 55 | ns | |
| $t_{XCR}$ | XIN to Clock Rising | 45 | 75 | 45 | 75 | 45 | 75 | ns | |

**Note 1:** Test conditions: t = 1000 ns for MPU800-1, 400 ns for MPU800, 250 ns for MPU800-4.

**Note 2:** Output timings are measured with a purely capacitive load of 150 pF. The following correction factor can be used for other loads:
150 pF $< C_L \leq$ 300 pF: + 0.25 ns/pF
50 pF $< C_L \leq$ 150 pF: − 0.15 ns/pF

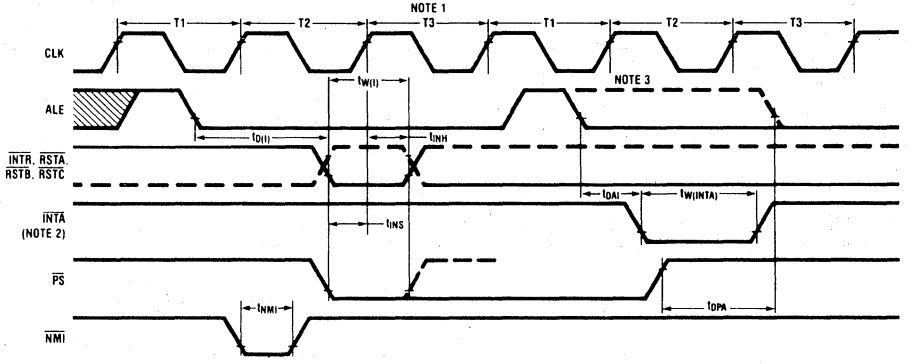
### TABLE 1. BUS TIMING AS T DEPENDENT

| Symbol | 1/T < 2.5 MHz | 2.5 MHz < 1/T < 4.0 MHz | | Symbol | 1/T < 2.5 MHz | 2.5 MHz < 1/T < 4.0 MHz | |
|---|---|---|---|---|---|---|---|
| $t_L$ | (1/2)T−10 | (1/2)T−30 | min | $T_{D(RFSH)}$ | (3/2 + N)T | (3/2 + N)T−50 | Min |
| $t_H$ | (1/2)T−50 | (1/2)T−45 | Min | $t_{D(WAIT)}$ | (1/2)T + 50 | (1/2)T | Max |
| $t_{ACC(RD)}$ | (1 + N)T + 100 | (1 + N)T + 50 | Max | $t_{(ADH)2}$ | (1/2)T−100 | (1/2)T−65 | Min |
| $t_{BABE}$ | T | T | Max | $t_{H(ADH)2}$ | (1/2)T−100 | (1/2)T−6 | Min |
| $t_{BACL}$ | (1/2)T−75 | (1/2)T−70 | Min | $t_{H(ADL)}$ | (1/2)T−100 | (1/2)T−50 | Min |
| $t_{DAI}$ | (1/2)T + 30 | (1/2)T−25 | Min | $t_{RL(MR)}$ | (1/2)T−50 | (1/2)T-40 | Min |
| $t_{DAR}$ | (1/2)T + 25 | (1/2)T | Min | $t_{S(AD)}$ | (1/2)T−120 | (1/2)T−85 | Min |
| $t_{DAR}$ | (1/2)T + 50 | (1/2)T + 35 | Max | $t_{S(ALE)}$ | (1/2)T−100 | (1/2)T−75 | Min |
| $t_{DAW}$ | T−10 | T−30 | Min | $t_{S(WD)}$ | (1/2)T−115 | (1/2)T−75 | Min |
| $t_{DAW}$ | T + 10 | T | Max | $t_{W(ALE)}$ | (1/2)T−70 | (1/2)T−50 | Min |
| $t_{D(BACK)1}$ | (5/2 + N)T | (5/2 + N)T−25 | Min | $t_{W(INTA)}$ | (1 + N)T | (1 + N)T−50 | Min |
| $t_{D(BACK)2}$ | (1/2)T | (1/2)T | Min | $t_{WL}$ | (1/2)T−50 | (1/2)T−35 | Min |
| $t_{D(BACK)2}$ | (3/2)T + 100 | (3/2)T + 100 | Max | $t_{W(RD)}$ | (1 + N)T | (1 + N)T−25 | Min |
| $t_{D(I)}$ | (3/2 + N)T−125 | (3/2 + N)T−125 | Max | $t_{W(RFSH)}$ | 2T−75 | 2T−100 | Min |
| $t_{DPA}$ | (1/2)T | (1/2)T | Min | $t_{W(WR)}$ | (1 + N)T | (1 + N)T−30 | Min |
| $t_{DPA}$ | (3/2)T + 50 | (3/2)T + 100 | Max | | | | |

Note: N is equal to number of WAIT states.

## TIMING REFERENCE

### Interrupt—Power-Save Cycle

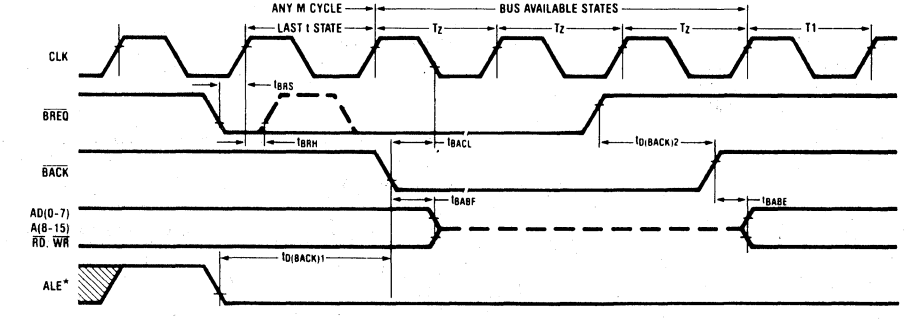



**Note 1:** This t state is the last t state of the last M cycle of any instruction.

**Note 2:** Response to INTR input.

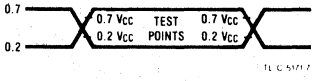
**Note 3:** Response to PS input.

### Bus Acknowledge Cycle

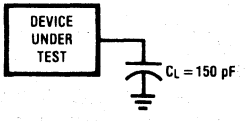



*Waveform not drawn to proportion. Use only for specifying test points.

### AC Testing Input/Output Waveform

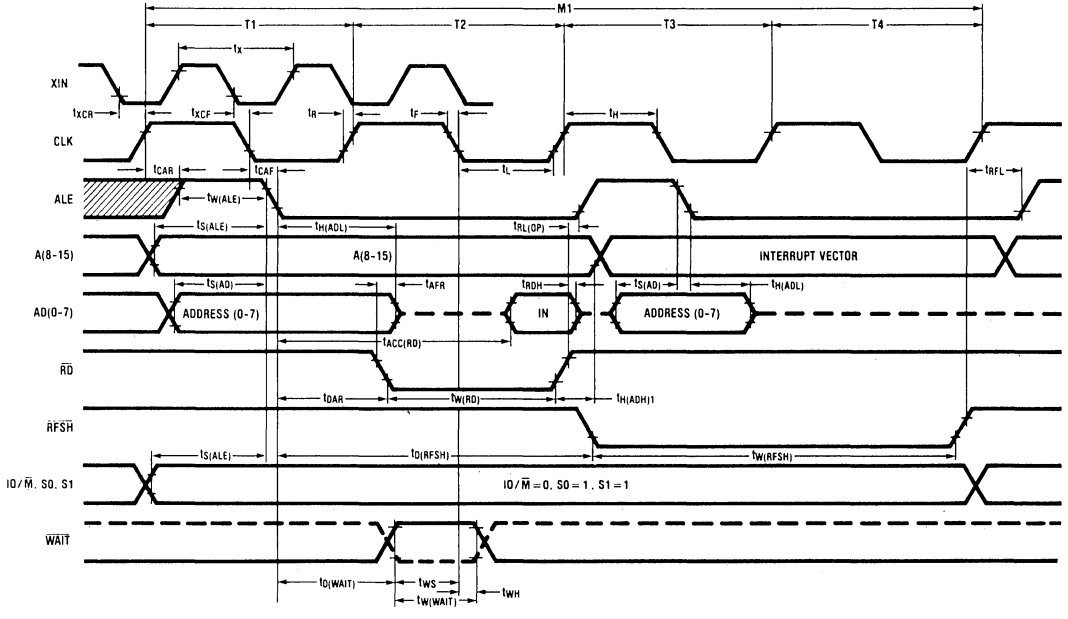



### AC Testing Load Circuit

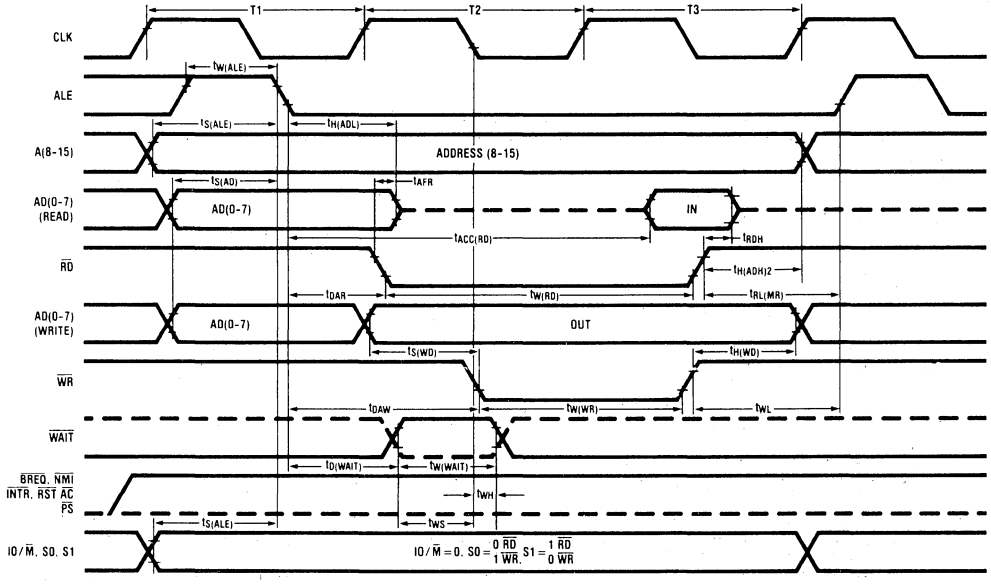


## TIMING WAVEFORMS

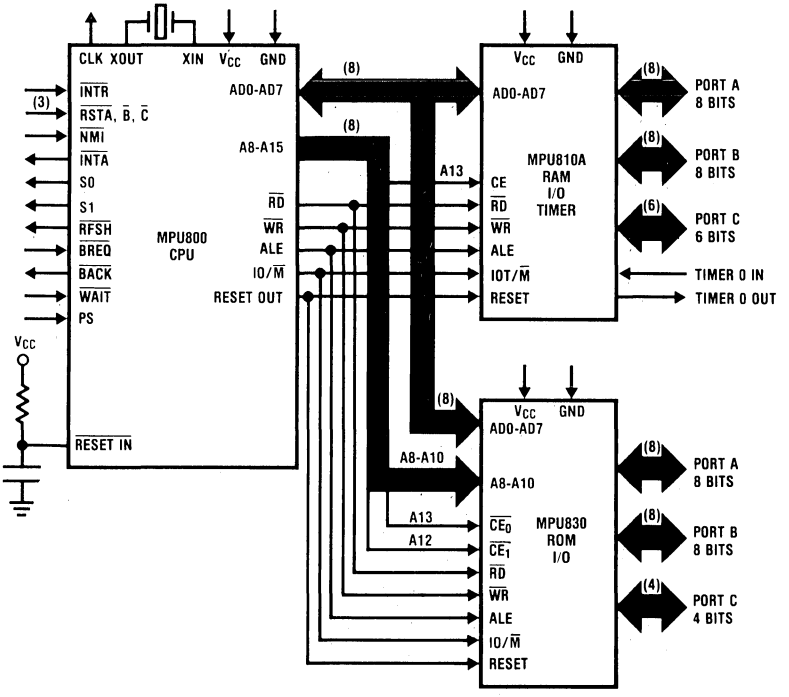
### Opcode Fetch Cycle




### Memory Read and Write Cycle



## MICROCOMPUTER FAMILY BLOCK DIAGRAM




STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N.Y. 11788
(516) 273-3100 TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# MPU 810A
# MPU 810A-1
# MPU 810A-4

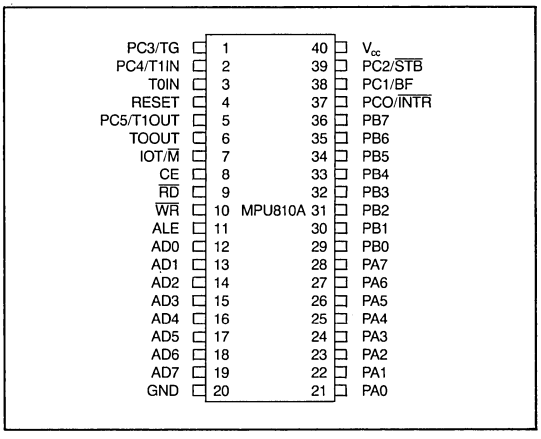
PRELIMINARY

# RAM-I/O-Timer

## FEATURES

- ☐ Variable Power Supply: 2.4V–6.0V
- ☐ Pin-Compatible With NSC810
- ☐ Three Programmable I/O Ports
- ☐ Two 16 Bit Programmable Counter Timers
- ☐ Very Low Power Consumption
- ☐ Fully Static Operation
- ☐ Single Instruction I/O Bit Operations
- ☐ Timer Operation: DC to 5 MHz
- ☐ Bus Compatible with MPU800 Family
- ☐ Three Speed Versions For Full Compatibility with the MPU800:
  MPU810-4–4 MHz
  MPU810 –2.5 MHz
  MPU810-1–1 MHz

## PIN CONFIGURATION




## BLOCK DIAGRAM

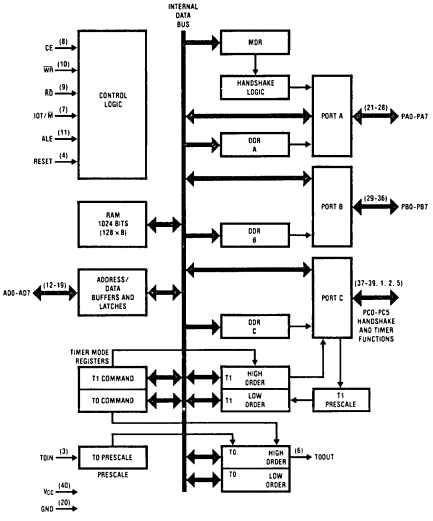



FIGURE 1

## GENERAL DESCRIPTION

The MPU810A functions as a memory, input/output peripheral interface, and a timing device. The memory is comprised of 1024 bits of static RAM organized 128 by 8.

The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A.

The timer portion of the device consists of two programmable 16 bit binary down-counters each capable of operation in any one of 6 modes. Timer counts are extendable by one of the available pre-scale values. The MPU810A comes in three speed versions to match the MPU800.

SECTION IX

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 40 | + 5 Volt | $V_{CC}$ | + 5 volt supply |
| 20 | Ground | GND | Ground |
| **Input Signals** | | | |
| 4 | Reset | RESET | RESET is an active-high input that resets all registers to 0 (low). The RAM contents remain unaltered. |
| 7 | Input/Output Timer/ RAM Select | IOT/$\overline{M}$ | Input/Output Timer or RAM Select (IOT/$\overline{M}$): IOT/$\overline{M}$ is an I/O memory select input line. A logic 1 (high) input selects the I/O-timer portion of the chip; a logic 0 (low) input selects the RAM portion of the chip. IOT/$\overline{M}$ is latched at the falling edge of ALE. |
| 8 | Chip Enable | CE | CE is an active-high input that allows access to the MPU810A. CE is latched at the falling edge of ALE. |
| 9 | Read | $\overline{RD}$ | The $\overline{RD}$ is an active-low input that enables a read operation of the RAM or I/O-timer location. |
| 10 | Write | $\overline{WR}$ | The $\overline{WR}$ is an active-low input that enables a write operation to RAM or I/O-timer locations. |
| 11 | Address Latch Enable | ALE | The falling edge of the ALE input latches AD0-AD7, CE and IOT/$\overline{M}$ inputs to form the address for RAM, I/O or timer. |
| 3 | Timer 0 Input | T0IN | T0IN is the clock input for timer 0. |
| **Output Signals** | | | |
| 6 | Timer 0 Output | T0OUT | T0OUT is the programmable output of timer 0. After reset, T0OUT is set high. |
| **Input/Output Signals** | | | |
| 12-19 | Address/Data Bus | AD0-AD7 | The multiplexed bidirectional address/data bus, AD0-AD7 pins, are in the high impedance state when the MPU810A is not selected. AD0-AD7 will latch address inputs at the falling edge of ALE. The address will designate a location in RAM, I/O or timer. $\overline{WR}$ input enables 8-bit data to be written into the addressed location. $\overline{RD}$ input enables 8-bit data to be read from the addressed location. The $\overline{RD}$ or $\overline{WR}$ inputs occur while ALE is low. |
| 21-28 | Port A, Bits 0-7 | PA0-PA7 | Port A is an 8-bit basic mode input/output port, also capable of strobed mode I/O utilizing three control signals from port C. Strobed mode of operation on port A has three different modes: strobed input, strobed output with active bus, strobed output with TRI-STATE bus. |
| 29-36 | Port B, Bits 0-7 | PB0-PB7 | Port B is an 8-bit basic mode input/output port. |
| 37-39,1,2,5 | Port C, Bits 0-5 | PC0-PC5 | Port C is a 6-bit basic mode I/O port. Each pin has a programmable second function, as follows:<br>**PC0/$\overline{INTR}$:** $\overline{INTR}$ is an active-low strobed mode interrupt request to the Central Processor Unit (CPU).<br>**PC1/BF:** BF is an active-high buffer full output to peripheral devices.<br>**PC2/$\overline{STB}$:** $\overline{STB}$ is an active-low strobe input from peripheral devices.<br>**PC3/TG:** TG is the timer gating signal.<br>**PC4/T1IN:** T1IN is the clock input for timer 1.<br>**PC5/T1OUT:** T1OUT is the programmable output of timer 1. |

## FUNCTIONAL DESCRIPTION

Refer to *Figure 1* for a detailed block diagram of the MPU810A.

### RANDOM ACCESS MEMORY (RAM)

The memory portion of the RAM-I/O-timer is accessed by a 7-bit address input to pins AD0 through AD6. The IOT/$\overline{M}$ input must be low (RAM select) and the CE input must be high at the falling edge of ALE to address the RAM. Address bit AD7 is a "don't care" for RAM addressing. Timing for RAM read and write operations is shown in the timing diagrams.

### INPUT/OUTPUT (I/O)

THE I/O portion of the MPU810A contains three sets of I/O called ports. There are two ports (A and B) which contain eight bits each and one port (port C) which has six bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (6 bits for port C). All ports share common function of Read, Write, Bit-Set and Bit-Clear. Additionally, port A is programmable for strobed (handshake) mode input or output. Port C has programmable second functions for each bit associated with strobed modes and timer functions. Table I defines the address location of the ports, timers and control registers.

### MODE DEFINITION REGISTER (MDR)

The mode definition register (MDR) defines the operating

mode for port A. While ports B and C are always in the basic I/O mode, there are four operating modes for port A:

Mode 0–Basic I/O (Input or Output)
Mode 1–Strobed Mode Input
Mode 2–Strobed Mode Output–Active Peripheral Bus
Mode 3–Strobed Mode Output–TRI-STATE* Peripheral Bus

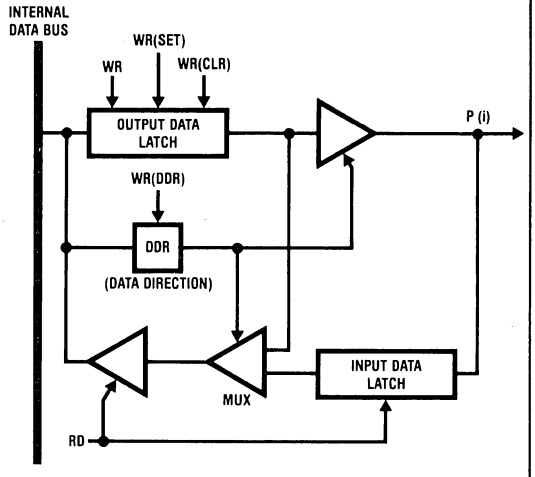
The MDR has the address assignment xxx00111 and is illustrated for the four modes in Table II.

## DATA DIRECTION REGISTERS (DDR)

Each port bit has a data direction register (DDR) that defines the I/O state of the bit. The bit is configured as an input if a "0" is written into its DDR, or as an output if a "1" is written. The DDR bits cannot be individually written to; the entire DDR byte is affected by a write to the DDR address. Thus, all data must be consistent with the direction desired for each port.

Any write or read operations on a port contradicting the DDR will not affect the port output or input. However, a read of a port bit, defined as an output, will cause a read from the output latch, and a write to a port bit, defined as an input, will modify the output latch. Refer to *Figure 2.*

**FIGURE 2. Block Diagram for Port Bit (i)**




## BIT OPERATIONS

The I/O features of the RAM-I/O-timer allow modification of a single bit or several bits of a port with Bit-Set and Bit-Clear command. The address is set up to indicate that a Bit-Set (or Clear) is taking place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing 1s will cause the indicated operation to be performed on the corresponding port bit. All bits of the data mask with 0s cause the corresponding port bits to remain unchanged. Three sample operations are shown in Table III using port B as an example.

*TRI-STATE® is a registered trademark of National Semiconductor Corporation.

**TABLE I. I/O AND TIMER ADDRESS DESIGNATIONS**

| 8-Bit Address Field Bits 7 6 5 4 3 2 1 0 | Designation I/O Port, Timer, etc. | R (Read) W (Write) |
|---|---|---|
| x x x 0 0 0 0 0 | Port A (byte) | R/W |
| x x x 0 0 0 0 1 | Port B (byte) | R/W |
| x x x 0 0 0 1 0 | Port C (byte) | R/W |
| x x x 0 0 0 1 1 | Not Used | ** |
| x x x 0 0 1 0 0 | DDR—Port A | W |
| x x x 0 0 1 0 1 | DDR—Port B | W |
| x x x 0 0 1 1 0 | DDR—Port C | W |
| x x x 0 0 1 1 1 | Mode Definition Reg. | W |
| x x x 0 1 0 0 0 | Port A—Bit-Clear | W |
| x x x 0 1 0 0 1 | Port B—Bit-Clear | W |
| x x x 0 1 0 1 0 | Port C—Bit-Clear | W |
| x x x 0 1 0 1 1 | Not Used | ** |
| x x x 0 1 1 0 0 | Port A—Bit-Set | W |
| x x x 0 1 1 0 1 | Port B—Bit-Set | W |
| x x x 0 1 1 1 0 | Port C—Bit-Set | W |
| x x x 0 1 1 1 1 | Not Used | ** |
| x x x 1 0 0 0 0 | Timer 0 (LB) | * |
| x x x 1 0 0 0 1 | Timer 0 (HB) | * |
| x x x 1 0 0 1 0 | Timer 1 (LB) | * |
| x x x 1 0 0 1 1 | Timer 1 (HB) | * |
| x x x 1 0 1 0 0 | STOP Timer 0 | W |
| x x x 1 0 1 0 1 | START Timer 0 | W |
| x x x 1 0 1 1 0 | STOP Timer 1 | W |
| x x x 1 0 1 1 1 | START Timer 1 | W |
| x x x 1 1 0 0 0 | Timer 0 Mode | R/W |
| x x x 1 1 0 0 1 | Timer 1 Mode | R/W |
| x x x 1 1 0 1 0 | Not Used | ** |
| x x x 1 1 0 1 1 | Not Used | ** |
| x x x 1 1 1 0 0 | Not Used | ** |
| x x x 1 1 1 0 1 | Not Used | ** |
| x x x 1 1 1 1 0 | Not Used | ** |
| x x x 1 1 1 1 1 | Not Used | ** |

x = don't care.
LB = low-order byte
HB = high-order byte
*A write accesses the modulus register, a read the read buffer.
**A read from an unused location reads invalid data, a write does not affect any operation of MPU810A.

**TABLE II. MODE DEFINITION REGISTER BIT ASSIGNMENTS**

| Mode \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | x | x | x | x | 0 |
| 1 | x | x | x | x | x | x | 0 | 1 |
| 2 | x | x | x | x | x | 0 | 1 | 1 |
| 3 | x | x | x | x | x | 1 | 1 | 1 |

x = don't care

SECTION IX

**TABLE III. BIT-SET AND CLEAR EXAMPLES**

| Operation | Set B7 | Clear B2 and B0 | Set B4, B3 and B1 |
|---|---|---|---|
| Address | xxx01101 | xxx01001 | xxx01101 |
| Data | 10000000 | 00000101 | 00011010 |
| Port Pins | | | |
| Prior State | 00001111 | 10001111 | 10001010 |
| Next State | 10001111 | 10001010 | 10011010 |

## PORT FUNCTIONS–BASIC I/O

Basic I/O is the mode of operation of ports B and C and mode 0 of port A (defined by the MDR). Read and write byte operations, and bit operations can be executed in the basic I/O mode. The timing for basic input and basic output modes is shown in the AC Characteristics tables.

When a read occurs, the information is latched from the peripheral (port) bus during the leading (falling) edge of the $\overline{RD}$ strobe. When a write occurs, the port bus is modified after the trailing (rising) edge of the $\overline{WR}$ strobe with data from the AD bus. Port output data remains valid at the output pin from one trailing edge of $\overline{WR}$ strobe to the trailing edge of the next $\overline{WR}$ strobe which then modifies that port.

## PORT A–STROBED (HANDSHAKE) MODE

Port A can be programmed (via the MDR) into one of 3 types of strobed mode for handshake communication with intelligent peripherals. When port A is in mode 1, 2 or 3 (see description of MDR), port C pins 0, 1 and 2 are used as handshake signals between the peripheral and the CPU. These handshake signals are designated $\overline{STB}$, BF, and $\overline{INTR}$. Timing parameters and timing diagrams are detailed under AC Characteristics.

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the I/O to the CPU. In strobed input mode, the CPU reads the valid data at port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing to port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving the ability to control strobed data transfer under software control. It is enabled or disabled respectively, by setting (= 1) or clearing (= 0) the output data latch of bit 2, port C. Port bit PC2 is used as the $\overline{STB}$ input. Since PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signals to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation. Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear instructions. The port C byte write command will not alter the output data latch of PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active-low input from the peripheral device, signaling that data-transfer is about to begin. This strobe is interpreted as an "output request" if port A is in a strobed output mode, or as a "data-valid" signal if port A is in strobed input mode.

BF (Buffer Full) is an output from the I/O to the peripheral signaling that data transfer is complete. In strobed input mode, this strobe indicates that data is received into port A and that no further data should be transmitted by the peripheral device until the port has been read (emptied). In strobed output mode, BF indicates that the request from the peripheral has been processed by the CPU and the valid data now appears in port A.

Note: In either input or output mode BF may be cleared by rewriting mode definition register.

The bits of port C that are used for handshake control of port A (bits C0, C1 and C2) must be direction-defined appropriately in the DDR. Also, the DDR of port A must be consistent with the mode specified in the MDR. Register set-up configurations for the three handshake modes are illustrated in Table IV.

**TABLE IV. MODE DEFINITION REGISTER CONFIGURATIONS**

| Mode | MDR | DDR Port A | DDR Port C | Port C Output Latch |
|---|---|---|---|---|
| Strobed Input | xxxxxx01 | 00000000 | xxx011 | xxx1xx |
| Strobed Output (Active) | xxxxx011 | 11111111 | xxx011 | xxx1xx |
| Strobed Output (TRI-STATE) | xxxxx111 | 11111111 | xxx011 | xxx1xx |

### Strobed Input (Mode 1)

During strobed input operations, an external device can load data into port A with the $\overline{STB}$ signal. Data is input to the PA0-7 input latches on the leading (negative) edge of $\overline{STB}$, causing BF to go high (true). On the trailing (positive) edge of $\overline{STB}$ the data is latched and the interrupt signal, $\overline{INTR}$, becomes valid indicating to the CPU that data is available for reading. $\overline{INTR}$ will become valid only if the interrupt is enabled, that is the output data latch for PC2 is true.

When the CPU reads port A, address X'00, the trailing edge of the $\overline{RD}$ strobe causes BF and $\overline{INTR}$ to become inactive, indicating that the strobed input cycle has been completed.

### Strobed Output (Mode 2)

During strobed output operations, an external device can read data from port A with the $\overline{STB}$ signal. Data is initially loaded into port A by the CPU writing to I/O address X'00. On the trailing edge of $\overline{WR}$, $\overline{INTR}$ is set inactive and BF becomes valid indicating data is available for the external device. When the external device is ready to accept the data in port A it pulses the $\overline{STB}$ signal. $\overline{STB}$ will reset BF with its rising edge and also activates the $\overline{INTR}$ signal.

$\overline{INTR}$ in this mode indicates a condition that requires CPU intervention, which is the output of the next byte of data.

### Strobed Output–TRI-STATE Mode (Mode 3)

The strobed output TRI-STATE mode and the strobed output active (peripheral) bus mode function in a similar manner with one exception. The exception is that the data signals on PA0-7 assume the high impedance state at all times except when accessed by the $\overline{STB}$ signal. Thus, in addition

to its timing function, $\overline{STB}$ activates port A outputs to active logic levels. This mode 3 operation allows other data sources, in addition to the NSC810, to feed a common external device.

## TIMERS

The two timers in the RAM-I/O-timer are 16-bit binary down-counters, each timer having six modes of operation. Full count is reached at "n + 1", where "n" is the value loaded into the modulus register. Read and write commands can occur at any time, asynchronous to timer operation by addressing the timer read buffer or modulus register, respectively. Each timer has a mode register and a write-only start/stop register. Each timer also has a prescaler which divides the incoming clock signal by a programmable value, extending the effective ranges of the timers while maintaining 16-bit precision. Selected timer outputs are ÷ 1 or ÷ 2 for timer 1, and ÷ 1, ÷ 2, or ÷ 64 for timer 0. A diagram representing one timer and associated registers is shown in *Figure 3.*

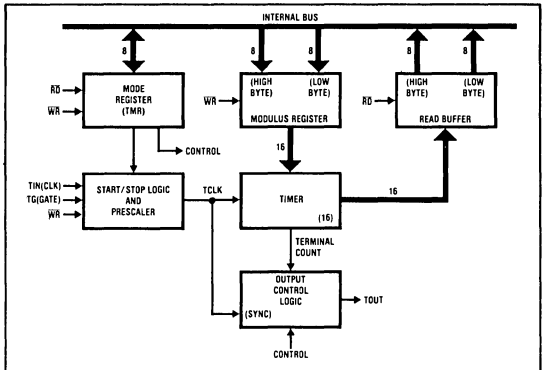



**FIGURE 3. Timer Internal Block Diagram (One of Two)**

## TIN, TOUT, AND TG

Timer 0 has dedicated pins for its clock, TOIN, and its output, TOOUT. Timer 1 must borrow its input and output pins from port C. This is accomplished by writing to the TMR for timer 1. If mode 1,2,3,4,5, or 6 is specified in TMR 1, the pins from port C (PC3, PC4, and PC5) are automatically made available to the timer(s) for gating (TG), T1IN, and T1OUT, respectively. These pins are also taken from port C any time timer 0 is in mode 2, 3, or 4. This is also automatically accomplished by writing TMR 0. In order to reconfigure pins PC3, PC4, PC5 to their original configuration as standard I/O, the timer mode registers must be reset by selecting mode 0 or 7.

TG (PC3), the timer gate, is used to hardware control the starting/stopping (or triggering) of the timers. The timer gate may be used individually by either timer or simultaneously by both timers.

For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If the timer gate makes an active transition prior to a write to the start address, the trailing edge of the WR strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address.

The DDR for port C must be programmed with the correct I/O direction for TG and the input and output of timer 1. See Table V for programming examples.

## TIMER MODES

The low-order three bits (bits 0, 1, 2) of the timer mode registers (TMR) define the mode of operation for the timers. Each TMR may be written to, or read from, at any time. However, to ensure accurate timing, it is important to modify the mode of the timer only when the timer is stopped. Inputs of 000 or 111 will define a NOP (no operation) mode, the timer is stopped and the output is inactive. Inputs of 001 through 110 will select one of six distinct timer functions.

In the explanations that follow, assume that the modulus for the timer is loaded with the appropriate value by writing to the low and high bytes of each timer (I/O addresses X'10 and X'11 for timer T0 and X'12 and X'13 for timer T1). Assume also that the timer is started by writing the I/O address X'15 (T0) or X'17 (T1) and the prescaler is not selected.

### Event Counter (Mode 1, TMR Bits = 001)

In the non-gated mode,the count is decremented for each clock period at the input of the timer (see *Figure 4a*). When the count reaches zero, the output goes valid and remains valid until the timer count is read by the CPU, or the timer is halted.

The timer is reloaded at the terminal count (= 0) with the modulus and continues to decrement even when the output is valid.

**TABLE V. TIMER PROGRAMMMING SECTION EXAMPLE**

| Mode Register Bit 7 6 5 4 3 2 1 0 | Output Sense Active L/H | Timer Gate Polarity Active L/H | Mode Description Single/Double Precision S/D | Prescale Value | Timing Mode | Port C DDR 5 4 3 2 1 0 |
|---|---|---|---|---|---|---|
| **TIMER 0** | | | | | | |
| x x x x x 0 0 0 | x | x | x | x | 0 | x x x x x x |
| 0 x 0 0 0 0 0 1 | L | x | D | ÷ 1 | 1 | x x x x x x |
| 1 x 0 1 1 1 1 0 | H | x | D | ÷ 64 | 6 | x x x x x x |
| 1 0 0 0 1 1 0 0 | H | H | D | ÷ 2 | 4 | 1 0 0 x x x |
| 0 1 1 0 0 0 1 0 | L | L | S | ÷ 1 | 2 | 1 0 0 x x x |
| **TIMER 1** | | | | | | |
| x x x x x 1 1 1 | x | x | x | x | 7 | x x x x x x |
| 0 x 0 x 0 0 0 1 | L | x | D | ÷ 1 | 1 | 1 0 0 x x x |
| 1 0 1 x 1 1 0 1 | H | L | S | ÷ 2 | 5 | 1 0 0 x x x |
| 0 1 0 x 0 0 1 1 | L | H | D | ÷ 1 | 3 | 1 0 0 x x x |

x = don't care

**TABLE VI. MODE SELECTION**

| BIT 2 1 0 | | Timer Function |
|---|---|---|
| 0 0 0 | — | Timer Stopped and Reset |
| 0 0 1 | — | Event Counter |
| 0 1 0 | — | Event Timer (Stopwatch) |
| 0 1 1 | — | Event Timer (Resetting) |
| 1 0 0 | — | One Shot |
| 1 0 1 | — | Square Wave |
| 1 1 0 | — | Pulse Generator |
| 1 1 1 | — | Timer Stopped and Reset |

### Accumulative Timer (Mode 2, TMR Bits = 010)

In this gated mode, the counter will decrement only when the gate input is active (see *Figure 4b*). If the gate becomes inactive, the counter will hold at its present value and continue to decrement when the gate again becomes active. When the counter decrement is zero, the output becomes valid and remains valid until the count is read by the CPU or the timer is halted.

At the terminal count the timer is reloaded and the count continues as long as the gate is active.

### Restartable Timer (Mode 3, TMR Bits = 011)

In this gated mode, the counter will decrement only when the gate input is active. If the gate becomes inactive, the counter will reload the modulus and hold this value until the gate again becomes active (see *Figure 4c*). If the timer is read when the gate is inactive, you will always read the value the timer has counted down to, not the value the timer has been reloaded with. The timer restarts at its modulus value. The prescaler is not reset at this time.

At terminal count the output becomes valid and the timer is reloaded. The timer will continue to run as normal, the only difference is the output is valid. Once the output is valid it remains valid until the count is read by the CPU or the timer is halted.

Note: The gate inactive time must be longer than the high time of the internal clock on the chip. Therefore, with ÷ 64 prescale selected the gate inactive time must be 33 input clocks or greater.

### One Shot (Mode 4, TMR Bits = 100)

In this gated mode, the timer holds the modulus count until the active gate edge (see *Figure 4d*). The output immediately becomes valid and remains valid as the counter decrements. The gating signal may go inactive without affecting the count. If TG (the gate) becomes inactive and returns active prior to the terminal count, the modulus will be reloaded, retriggering the one shot period. When the timer reaches the terminal count, the output becomes inactive. The gate, in this mode, is edge sensitive; the active edge is defined in TMR.

Note: The one shot cannot be retriggered during its last internal count regardless of prescaler selected. Therefore, in divide by 1 prescaler, it cannot be retriggered during the last clock, in divide by 2 prescaler, during the last two clocks and divide by 64 prescaler, during the last 64 clocks.

### Square Wave (Mode 5, TMR Bits = 101)

In this non-gated mode, the output will go active as soon as the timer is started. The counter decrements for each clock period and complements its output when zero is reached (see *Figure 4e*). The modulus is then reloaded and counting continues. Assuming a regular clock input, the output will then be a square wave with a period equal to twice the value loaded into the modulus. Therefore, varying the modulus will vary the duty cycle of the square wave.

Stopping then restarting the timer does not reset the timer. In order to reload the modulus and start from the beginning of the cycle, the timer mode register must be reset by selecting mode 0 and then reprogramming the timer.

### Pulse Generator (Mode 6, TMR Bits = 110)

In this non-gated mode, the counter decrements for each clock period (see *Figure 4f*). When the timer decrements to zero, the output becomes valid for one clock width.

With a prescale of divide by 2 the output will be valid for one full clock and with divide by 64 prescale the output will be valid for 32 clocks. The modulus is then reloaded and the sequence is repeated. Varying the modulus value will vary the frequency of the pulse.

Stopping then restarting the timer does not reset the timer. In order to reload the modulus and start from the beginning of the cycle, the timer mode register must be reset by selecting mode 0 and then reprogramming the timer.

## TIMER MODE REGISTER

The timer mode register (TMR) may be written or read at any time; however, to assure accurate timing it is important to modify the mode when the timer is stopped. The timer mode is selected from one of six modes with TMR bits 0, 1, and 2. Bits 3 and 4 select the prescale value if the prescaler is to be used. Bits 5, 6 and 7 select the read/write mode, gate input polarity, and output sense (active-high or low). The bit functions of the TMR are further illustrated in *Figure 6.*

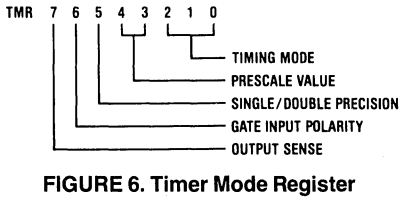



**FIGURE 6. Timer Mode Register**

### Timer Prescaler

There is a prescale function associated with each timer. It serves as an additional divisor to lengthen the counts for each timer circuit. The value of the divisor is fixed and selectable in each TMR.

The timer output is affected by the prescale selection. The output responds to the timer clock, not the incoming clock (TIN); so, TOUT will be prescaled by the same value as the timer. Although the 16-bit prescaled count of the timer may be read, the internal value of the prescaler cannot be read by the user. A "00" for either timer represents ÷ 1 (no prescale). Timer 0 has the two possibilities of ÷ 2 or ÷ 64:

| Timer Bit | 4 3 | Prescale |
|---|---|---|
| | 0 0 | ÷ 1 |
| | 0 1 | ÷ 2 |
| | 1 1 | ÷ 64 |

Timer 1 has only the ÷ 2 prescale available; TMR bit 4 is a "don't care".

| Timer Bit | 4 3 | Prescale |
|---|---|---|
| | x 0 | ÷ 1 |
| | x 1 | ÷ 2 |

### Single/Double Precision

A two-byte word (or a single byte when one byte is a "don't care") may be read from or written to the timers. To program

**Timer Mode Examples** (Modulus register is loaded with 0004 for these examples)

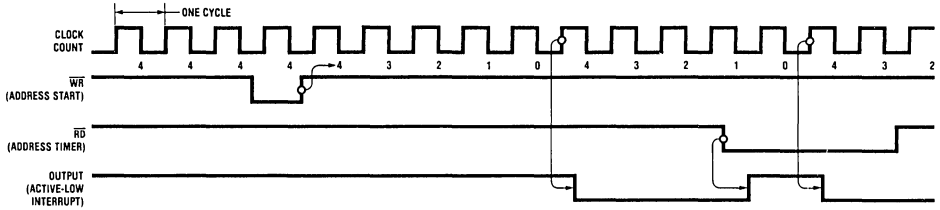



FIGURE 4a. Event Counter Mode (Mode 1)

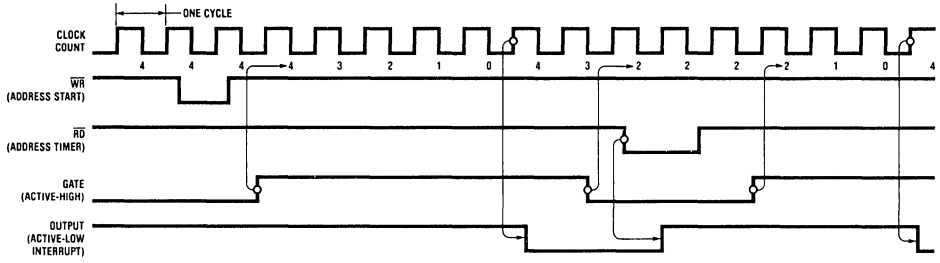



FIGURE 4b. Accumulative Timer (Mode 2)

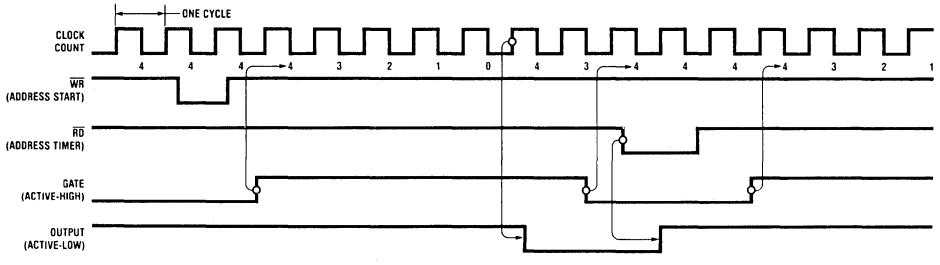



FIGURE 4c. Restartable Timer (Mode 3)

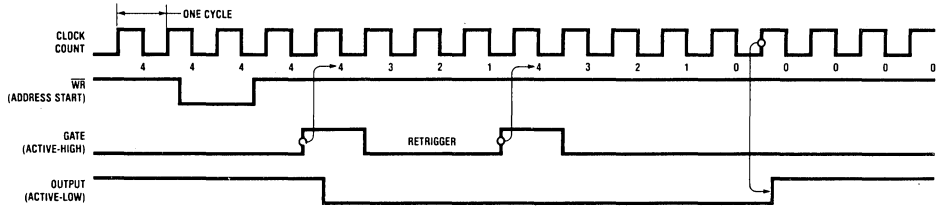



FIGURE 4d. One Shot (Mode 4)

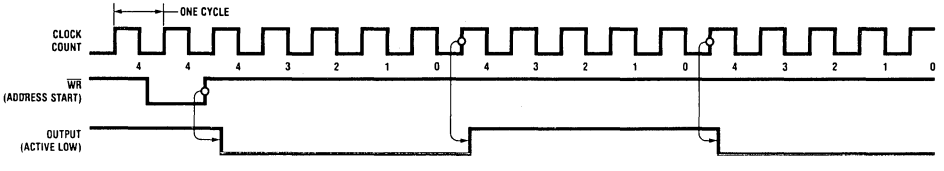



FIGURE 4e. Square Wave (Mode 5)

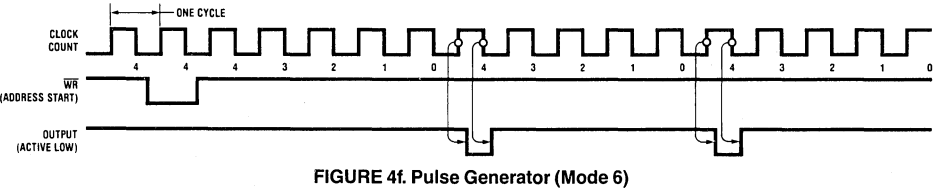
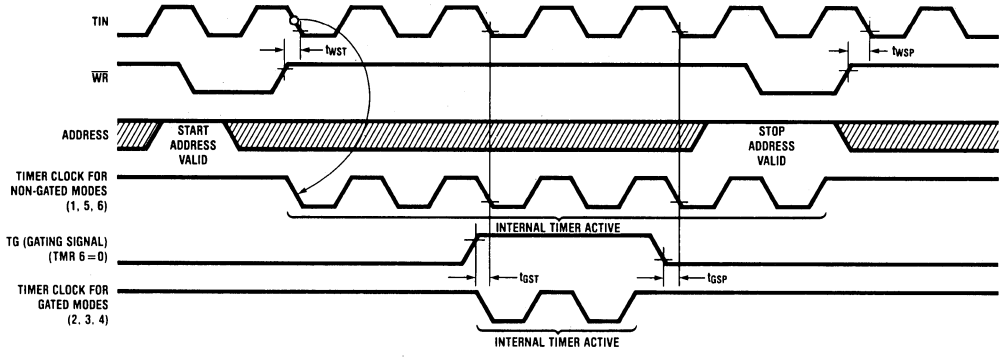



FIGURE 4f. Pulse Generator (Mode 6)




Note: Diagonal lines indicate interval of invalid data.
For mode 4 (one shot), only start-timing applies
$t_{WST}$–$\overline{WR}$ set-up for starting timer 150 ns
$t_{WSP}$–$\overline{WR}$ set-up for stopping timer 150 ns
$t_{GST}$–TG (gate) set-up for starting timer 100 ns
$t_{GSP}$–TG (gate) set-up for stopping timer 100 ns

**FIGURE 5. Start/Stop Timing**

the timer buffers, TMR bit 5 must be set as follows:

0–Double byte read or write low byte first, then high byte. *The order of low byte first, high byte second must be maintained for proper Read/Write communications*

1–Single byte read or write low byte only–high byte "don't care" or high byte only with low byte "don't care."

The difference between these modes is that the double byte mode freezes the read buffer or the modulus register until you have had an opportunity to read or write both bytes. The following example clearly illustrates this point. If the timer had a value of 200 when the low byte was read and then decremented to 1FF before the high byte was read then the double byte mode would have read 00 and 02, respectively. The single precision mode would have read 00 and 01.

Note: In the double precision mode, the high byte should be read immediately after the low byte. Do not access any other registers or unused address location between the reads.

### Gate Input Polarity

The TG input is the hardware control for starting and stopping the timers. For modes 2 and 3, the timer starts on the gate-active transition assuming the start address was previously written. If the timer gate makes an active transition prior to a write to the start address, the trailing edge of the WR strobe starts the timer. However, for mode 4 the timer always waits for an active gate edge following a write to the start address.

The polarity of the gate input may be selected by the contents of bit 6 of the TMR. If bit 6 equals 0, the gate signal will be active-high or positive edge for mode 4; if bit 6 equals 1, the gate polarity will be active-low or negative edge for mode 4.

### Timer Output Polarity

Like the gating function, the polarity of the output signal is also programmable via bit 7 of the TMR. A zero will cause an active-low output; a one will generate an active-high output.

The output for T1 is multiplexed with port C, bit 5. (Similarly T1IN is multiplexed with port C, bit 4.) When any timer mode other than 0 or 7 is specified for T1, or when mode 2, mode 3, or mode 4 is specified to T0, the three port C pins, bit 3, bit 4, and bit 5, become TG, T1IN, and T1OUT, respectively.

### TIMER PROGRAMMING

The proper sequence to program the timer is as follows:

1. Write timer mode register with mode 0 or 7 selected. This stops the timer, resets the prescaler, and sets internal clock high.

2. Write timer mode register again, this time setting it up to your requirements.

3. Write the modulus values, low byte first, high byte second.

4. Start the timers.

The timer output latches are only updated when the internal timer clock gets an active transition. The internal timer clock is defined as the output of the prescaler. Therefore, it is impossible to read back the value just written to the timer unless you have an active transition on the internal clock.

To guarantee the integrity of the data during a read operation, updates to the timer output latches are blocked out. If an update is blocked out due to a read, the output latches will not be updated until the next active transition. If continuous reads were made to the timers and an update was blocked out it would appear as if a count was skipped. For example, if the output latches were FF when a block out occurred, the next update would occur at FD, thereby giving an appearance of the count FE being skipped. In actuality the correct number of clocks has occurred for the timer to read FD.

Writing the modulus value when the timer is running does not update the timer immediately. The new value written will get into the timer when the timer hits its terminal count and reloads its value. If the timer is stopped and a modulus is written the new modulus value will get into the timer only if the internal clock is high for some period before the start command. If it does not go high then the next time the timer hits its terminal count it will load the new modulus. One way to guarantee the data will get into the timer immediately is to follow steps 1-4. Although this procedure guarantees that the data will get into the timer you will not be able to read it back until you get an active transition on the internal clock.

Rewriting modulus does not reset the prescaler. The only way to reset the prescaler is to write the mode register and have internal clock signal be high for some period between the write of the mode register and the start of the timer. Once again steps 1 through 4 will reset the prescaler.

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Range ..... −65°C to + 150°C
Voltage at Any Pin with Respect to Ground ..... −0.3V to $V_{CC}$ + 0.3V
$V_{CC}$ ..... 7V
Power Dissipation ..... 1W
Lead Temperature (Soldering, 10 seconds) ..... 300°C

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

## OPERATING CONDITIONS $V_{CC}$ = 5V ± 10%

## DC ELECTRICAL CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 10%, GND = 0V, unless ot...

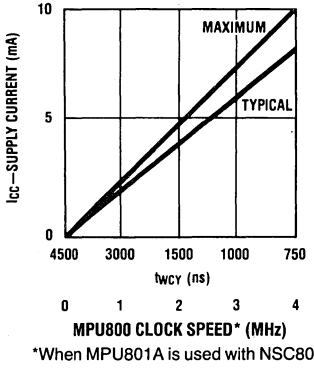
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logical 1 Input Voltage | | 0.7 $V_{cc}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Logical 0 Input Voltage | | 0 | | 0.2 $V_{CC}$ | V |
| $V_{OH}$ | Logical 1 Output Voltage | $I_{OH}$ = −1.0 mA<br>$I_{OUT}$ = −10 μA | 2.4<br>$V_{CC}$ − 0.5 | | | V<br>V |
| $V_{OL}$ | Logical 0 Output Voltage | $I_{OL}$ = 2 mA<br>$I_{OUT}$ = 10 μA | 0<br>0 | | 0.4<br>0.1 | V<br>V |
| $I_{IL}$ | Input Leakage Current | $0 \le V_{IN} \le V_{CC}$ | −10.0 | | 10.0 | μA |
| $I_{OL}$ | Output Leakage Current | $0 \le V_{IN} \le V_{CC}$ | −10.0 | | 10.0 | μA |
| $I_{CC}$ | Active Supply Current | $I_{OUT}$ = 0, Timer = Mode 1, T0IN = T1IN = 2.5 MHz, $t_{WCY}$ = 750 ns | | 8 | 10 | mA |
| $I_Q$ | Quiescent Current | No Input Switching, $T_A$ = 25°C | | 10 | 100 | μA |
| $C_{IN}$ | Input Capacitance | | | 4 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | | 6 | 10 | pF |
| $V_{CC}$ | Power Supply Voltage | | 2.4 | 5 | 6 | V |
| $V_{DRV}$ | Data Retention Voltage | | 1.2 | | | V |

## LOW VOLTAGE OPERATION Preliminary

| Voltage | MPU810A-1 | MPU810A | MPU810A-4 | Units |
|---|---|---|---|---|
| 2.4 | — | 500 | 500 | kHz |
| 3.0 | — | 1 | 1 | MHz |

**Note 1:** Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

**$I_{CC}$ vs Speed**




*When MPU801A is used with NSC800

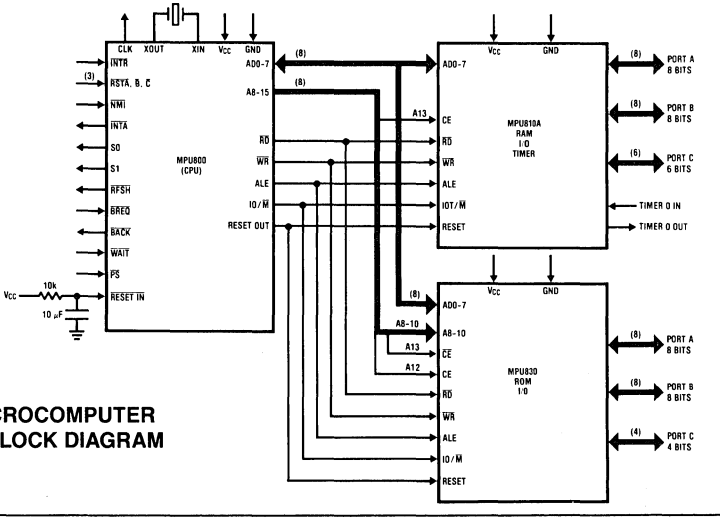
## TIMER AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_C$ | Clock Frequency | | DC | | 2.5 | MHz |
| $F_{CP}$ | Clock Frequency | Prescale Selected | DC | | 5.0 | MHz |
| $t_{CW}$ | Clock Pulse Width | | 150 | | | ns |
| $t_{CWP}$ | Clock Pulse Width | Prescale Selected | 75 | | | ns |
| $t_{GS}$ | Gate Set-Up Time | With Respect to Negative Clock Edge | 100 | | | ns |
| $t_{GH}$ | Gate Hold Time | With Respect to Negative Clock Edge | 250 | | | ns |
| $t_{CO}$ | Clock to Output Delay | $C_L$ = 100 pF | | | 350 | ns |

SECTION IX

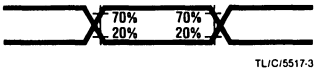
## AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | MPU810A-1 | | MPU810A | | MPU810A-4 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Access Time from ALE | CL = 150pF | | 1000 | | 400 | | 300 | ns |
| $t_{AH}$ | AD0-7, CE, IOT/$\overline{M}$ Hold Time | | 100 | | 60 | | 30 | | ns |
| $t_{ALE}$ | ALE Strobe Width (High) | | 200 | | 125 | | 75 | | ns |
| $t_{ARW}$ | ALE to $\overline{RD}$ or $\overline{WR}$ Strobe | | 150 | | 120 | | 75 | | ns |
| $t_{AS}$ | AD0-7, CE, IOT/$\overline{M}$ Set-Up Time | | 100 | | 75 | | 40 | | ns |
| $t_{DH}$ | Data Hold Time | | 150 | | 90 | | 40 | | ns |
| $t_{DO}$ | Port Data Output Valid | | | 350 | | 310 | | 300 | ns |
| $t_{DS}$ | Data Set-Up Time | | 100 | | 80 | | 50 | | ns |
| $t_{PE}$ | Peripheral Bus Enable | | | 320 | | 200 | | 200 | ns |
| $t_{PH}$ | Peripheral Data Hold Time | | 150 | | 125 | | 100 | | ns |
| $t_{PS}$ | Peripheral Data Set-Up Time | | 100 | | 75 | | 50 | | ns |
| $t_{PZ}$ | Peripheral Bus Disable (TRI-STATE®) | | | 150 | | 150 | | 150 | ns |
| $t_{RB}$ | $\overline{RD}$ to BF Output | | | 300 | | 300 | | 300 | ns |
| $t_{RD}$ | Read Strobe Width | | 400 | | 320 | | 220 | | ns |
| $t_{RDD}$ | Data Bus Disable | | 0 | 100 | 0 | 100 | 0 | 75 | ns |
| $t_{RI}$ | $\overline{RD}$ to $\overline{INTR}$ Output | | | 320 | | 320 | | 300 | ns |
| $t_{RWA}$ | $\overline{RD}$ or $\overline{WR}$ to Next Ale | | 125 | | 100 | | 75 | | ns |
| $t_{SB}$ | $\overline{STB}$ to BF Valid | | | 300 | | 300 | | 300 | ns |
| $t_{SH}$ | Peripheral Data Hold with Respect to $\overline{STB}$ | | 150 | | 125 | | 100 | | ns |
| $t_{SI}$ | $\overline{STB}$ to $\overline{INTR}$ Output | | | 300 | | 300 | | 300 | ns |
| $t_{SS}$ | Peripheral Data Set-Up With Respect to $\overline{STB}$ | | 100 | | 75 | | 50 | | ns |
| $t_{SW}$ | $\overline{STB}$ Width | | 400 | | 320 | | 220 | | ns |
| $t_{WB}$ | $\overline{WR}$ to BF Output | | | 340 | | 340 | | 300 | ns |
| $t_{WI}$ | $\overline{WR}$ to $\overline{INTR}$ Output | | | 320 | | 320 | | 300 | ns |
| $t_{WR}$ | $\overline{WR}$ Strobe Width | | 400 | | 320 | | 220 | | ns |
| $t_{WCY}$ | Width of Machine Cycle | | 3000 | | 1200 | | 750 | | ns |

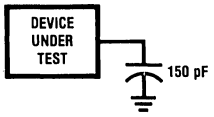



**MPU MICROCOMPUTER FAMILY BLOCK DIAGRAM**

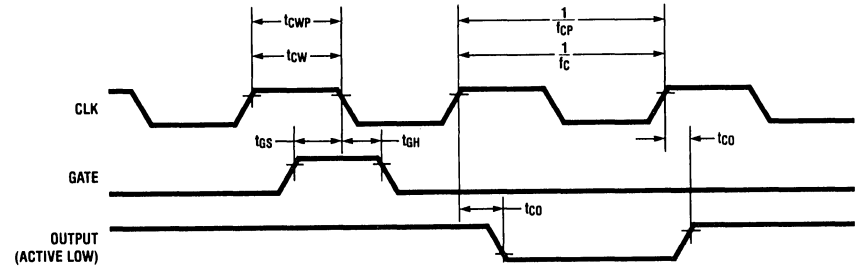
## AC TESTING INPUT/OUTPUT WAVEFORM




## AC TESTING LOAD CIRCUIT

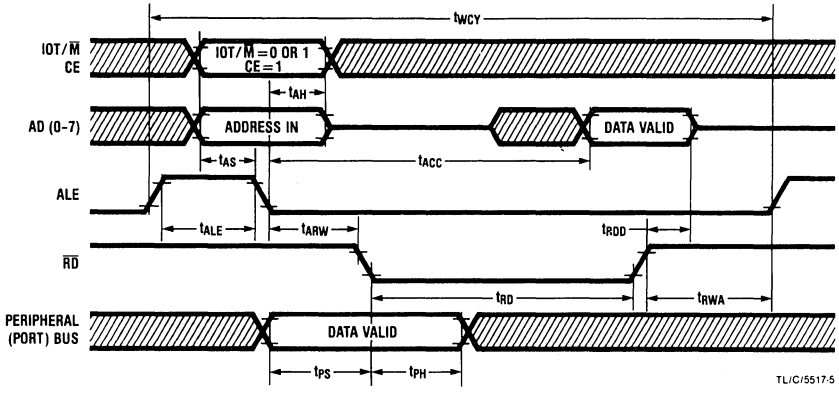



## TIMER WAVEFORMS



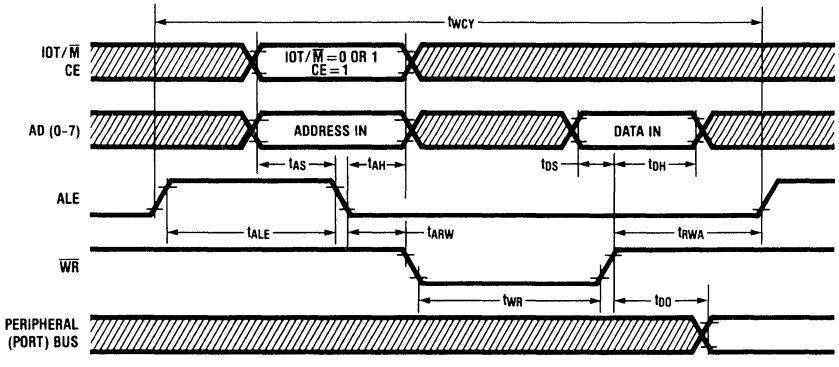

## GENERAL TIMING WAVEFORMS

### Read Cycle (Read from RAM, Port or Timer)




Note: Diagonal lines indicate interval of invalid data.

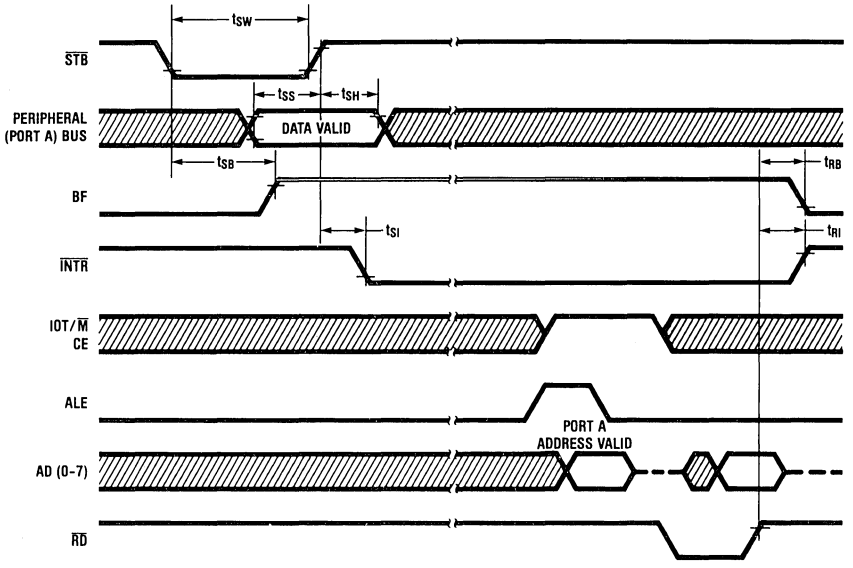
### Write Cycle (Write to RAM, Port or Timer)




Note: Diagonal lines indicate interval of invalid data.

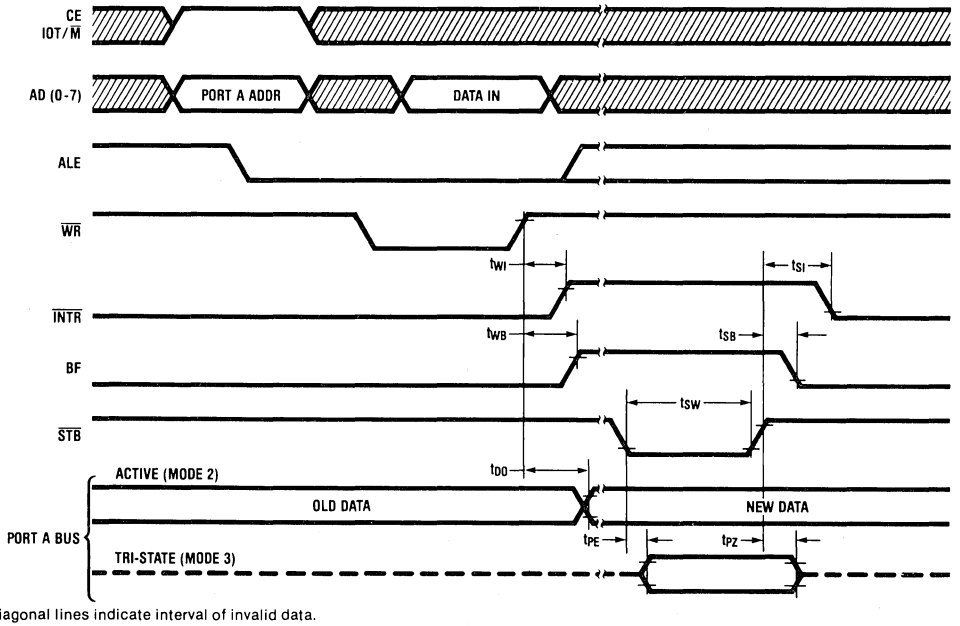
## HANDSHAKE TIMING

### Strobed Mode Input




Note: Diagonal lines indicate interval of invalid data.

### Strobed Mode Output




Note: Diagonal lines indicate interval of invalid data.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX 510 227 8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

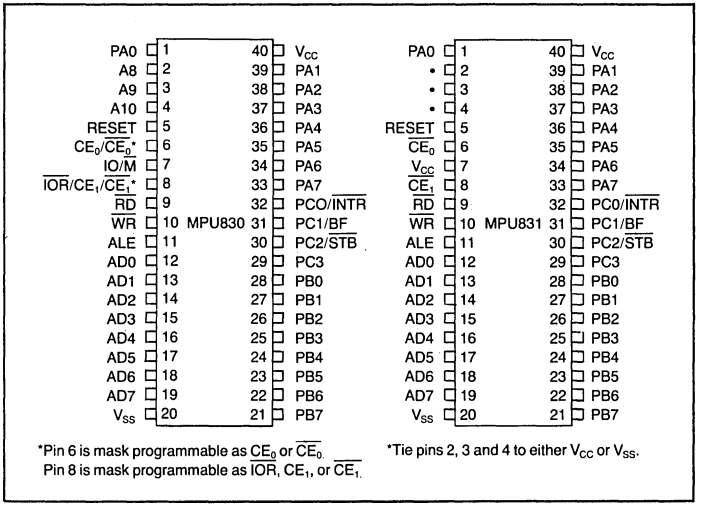
**MPU 830**
**MPU 831**
**PRELIMINARY**

# MPU 830 ROM I/O Device
# MPU 831 I/O Device

## FEATURES

- ☐ Variable Power Supply: 2.4V–6.0V
- ☐ Pin-Compatible With NSC830/NSC831
- ☐ Three Programmable I/O Ports
- ☐ 2K x 8 Read Only Memory (MPU830)
- ☐ Very Low Power Consumption
- ☐ Fully Static Operation
- ☐ Single Instruction I/O Bit Operations
- ☐ Bus Compatible With MPU800 Family
- ☐ Strobed Mode Available on Port A

## PIN CONFIGURATION




*Pin 6 is mask programmable as $\overline{CE_0}$ or $CE_0$.
Pin 8 is mask programmable as $\overline{IOR}$, $CE_1$, or $\overline{CE_1}$.

*Tie pins 2, 3 and 4 to either $V_{CC}$ or $V_{SS}$.

## GENERAL DESCRIPTION

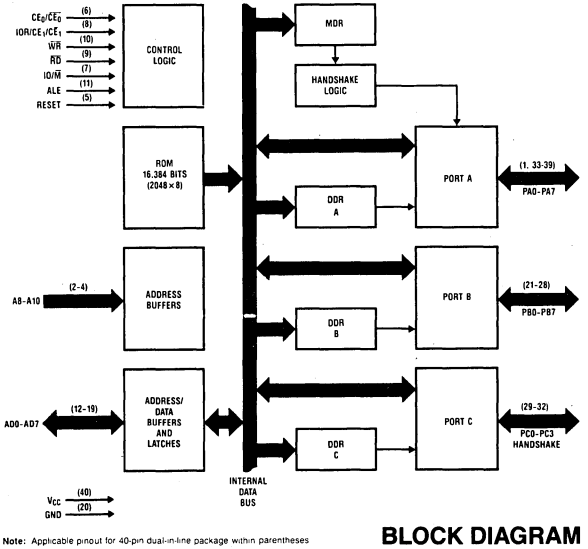
The MPU830 is a combination ROM and I/O peripheral device contained in a standard 40 pin package.

The ROM is comprised of 16,384 bits of Read Only Memory organized as 2048 by 8.

The I/O portion consists of 20 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A.

The MPU831 is similar to the MPU830 except that is contains no ROM. The MPU831 is useful for prototyping work prior to ordering the MPU830, and when on chip ROM is not required.

Figure 1




Note: Applicable pinout for 40-pin dual-in-line package within parentheses

BLOCK DIAGRAM

SECTION IX

## DESCRIPTION OF PIN FUNCTIONS

| PIN NO. | NAME | SYMBOL | FUNCTION |
|---|---|---|---|
| 40 | + 5 Volt | $V_{CC}$ | + 5 volt supply |
| 20 | Ground | GND | Ground |
| **Input Signals** | | | |
| 5 | Master Reset | $\overline{RESET}$ | An active-high input on the RESET pin initializes the chip causing the three I/O ports (A, B and C) to revert to the input mode. The three ports, the three data direction registers and the mode definition register are reset to low (0). |
| 7 | Input/Output/Memory Select | IO/$\overline{M}$ | The IO/$\overline{M}$ pin is a latched, select input line. A high (1) input selects the I/O portion of the chip; a low (0) input selects the ROM portion of the chip. The select input is latched by the trailing edge (high to low transition) of the ALE signal. |
| 6<br>8 | Chip Enable 0<br>Chip Enable 1 | $\overline{CE0}$/$\overline{CE0}$<br>$\overline{IOR}$/CE1/$\overline{CE1}$ | The chip enable inputs are mask programmable at the factory. The CE inputs permit the use of multiple MPU830s in a system without using a chip select decoder. The CE inputs must be active at the falling edge of ALE. At ALE time, the CE inputs are latched to provide access to the MPU830. The $\overline{IOR}$ input performs the same function as the combination of IO/$\overline{M}$ input high and the $\overline{RD}$ input low. |
| 9 | Read | $\overline{RD}$ | When the $\overline{RD}$ (or the $\overline{IOR}$, when mask programmed) input is an active low, data is read from the AD0-AD7 bus. When both $\overline{RD}$ and $\overline{IOR}$ are high, the AD0-AD7 bus is in the high impedance state. |
| 10 | Write | $\overline{WR}$ | When the CE inputs are active, and the IO/$\overline{M}$ input is high, an active low $\overline{WR}$ input causes the selected output port to be written with the data from the AD0-AD7 bus. |
| 11 | Address Latch Enable | ALE | The trailing edge (high to low transition) of the ALE input signal latches the address/data present on the AD0-AD7 bus, A8-A10 bus, plus the input control signals on IO/$\overline{M}$, $CE_0$/$\overline{CE_0}$, and $CE_1$/$\overline{CE_1}$. |
| 2-4 | Address Bus A8-A10 | A8, A9-A10 | The high-order bits of the ROM address are input on this 3-bit bus and are latched by the high-to-low transition of the ALE input. These bits do not affect the I/O operations. |
| **Input/Output Signals** | | | |
| 12-19 | Bidirectional Address/ Data Bus | AD0-AD7 | The lower 8 bits of the ROM or I/O address are applied to these pins, and latched by the trailing edge of ALE. During read operations, 8 bits are present on these pins, and are read when $\overline{RD}$ or $\overline{IOR}$ is low. During an I/O write cycle, Port A, B, or C is written with the data present on this bus at the trailing edge of the $\overline{WR}$ strobe. |
| 1, 39-33<br>28-21<br>32-29 | Port A, Bits 0-7<br>Port B, Bits 0-7<br>Port C, Bits 0-3 | PA0-PA7<br>PB0-PB7<br>PC0-PC3 | These are general purpose I/O pins. Their input/output direction is determined by the contents of the Data Direction Register (DDRs). |

## FUNCTIONAL DESCRIPTION

Refer to *Figure 1* for a detailed block diagram of the MPU830.

**Read Only Memory (ROM):** The memory portion of the ROM-I/O is accessed by an 11-bit address input to pins AD0-AD7 and A8-A10. The IO/$\overline{M}$ input must be low (ROM select) and the chip enable pins in the active programmed state at the falling edge of ALE to address the ROM. Timing for ROM read and write operations is shown in the timing diagrams.

**Input/Output (I/O):** The I/O portion of the MPU830 contains three sets of I/O called Ports. There are two ports (A and B) which contain 8 bits each and one port (Port C) which has 4 bits. Any bit or combination of bits in a port may be addressed with Set or Clear commands. A port can also be addressed as an 8-bit word (4 bits for Port C). When reading Port C, bits 4-7 will be read as ones. All ports share common functions of Read, Write, Bit-Set and Bit-Clear. Additionally, Port A is programmable for strobed (handshake) mode input or output. Port C has a programmable second function for each bit associated with strobed modes. *Table 1* defines the address location of the ports and control registers.

*TRI-STATE® is a registered trademark of National Semiconductor Corporation.

### MODE DEFINITION REGISTER (MDR)

The Mode Definition Register (MDR) defines the operating mode for Port A. While Ports B and C are always in the basic I/O mode, there are four operating modes for Port A:

Mode 0–Basic I/O (Input or Output)

Mode 1–Strobed Mode Input

Mode 2–Strobed Mode Output
- Active Peripheral Bus

Mode 3–Strobed Mode Output
- TRI-STATE® (high impedance) Peripheral Bus

The MDR has the I/O address assignment XXX00111. The bit configuration for the mode selection is illustrated below:

| Mode | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | X | X | X | X | X | X | X | 0 |
| 1 | X | X | X | X | X | X | 0 | 1 |
| 2 | X | X | X | X | X | 0 | 1 | 1 |
| 3 | X | X | X | X | X | 1 | 1 | 1 |

**NOTE:** X = don't care

**Table 1. I/O and Address Designations**

| 8-Bit Address Field Bits | | | | | | | | Designation I/O Port, etc. | R (Read) W (Write) |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| X | X | X | X | 0 | 0 | 0 | 0 | Port A (byte) | R/W |
| X | X | X | X | 0 | 0 | 0 | 1 | Port B (byte) | R/W |
| X | X | X | X | 0 | 0 | 1 | 0 | Port C (byte) | R/W |
| X | X | X | X | 0 | 0 | 1 | 1 | Not Used | — |
| X | X | X | X | 0 | 1 | 0 | 0 | DDR — Port A | W |
| X | X | X | X | 0 | 1 | 0 | 1 | DDR — Port B | W |
| X | X | X | X | 0 | 1 | 1 | 0 | DDR — Port C | W |
| X | X | X | X | 0 | 1 | 1 | 1 | Mode Definition Register | W |
| X | X | X | X | 1 | 0 | 0 | 0 | Port A — Bit Clear | W |
| X | X | X | X | 1 | 0 | 0 | 1 | Port B — Bit Clear | W |
| X | X | X | X | 1 | 0 | 1 | 0 | Port C — Bit Clear | W |
| X | X | X | X | 1 | 0 | 1 | 1 | Not Used | — |
| X | X | X | X | 1 | 1 | 0 | 0 | Port A — Bit Set | W |
| X | X | X | X | 1 | 1 | 0 | 1 | Port B — Bit Set | W |
| X | X | X | X | 1 | 1 | 1 | 0 | Port C — Bit Set | W |
| X | X | X | X | 1 | 1 | 1 | 1 | Not Used | — |

**NOTE:** X = don't care

## DATA DIRECTION REGISTERS (DDR)

Each port bit has a data direction register (DDR) which defines the I/O state of the bit. The bit is configured as an input if a "0" is written into its DDR, or as an output if a "1" is written. The DDR bits cannot be individually written to: the entire DDR byte is affected by a write to the DDR address. Thus all data must be consistent with the direction desired for each port.

Any write or read operations on a port contradicting the DDR will not affect the port output or input. However, a read of a port bit defined as an output will cause a read from the output latch, and a write to a port bit defined as an input will modify the output latch.

## PORT FUNCTIONS—BASIC I/O

Basic I/O is the mode of operation of Ports B and C and mode 0 of Port A (defined by the MDR). Read, write, and bit operations can be executed in the basic I/O mode. The timing for basic input and basic output modes is shown in the AC Characteristics tables.

When a read occurs the information is latched from the peripheral bus on the leading (falling) edge of the $\overline{RD}$ strobe. When a write occurs the port bus is modified after the trailing (rising) edge of the $\overline{WR}$ strobe with data from the AD bus. Port output data remains valid on the output pin from one trailing edge of $\overline{WR}$ strobe to the trailing edge of the next $\overline{WR}$ strobe.

## BIT OPERATIONS

The I/O features of the ROM-I/O allow modification of a single bit or several bits of a port with Bit-Set and Bit-Clear (see *Figure 2*). The address is set up to indicate that a bit set (or clear) is taking place. The incoming data on the address/data bus is latched at the trailing edge of the $\overline{WR}$ strobe and is treated as a mask. All bits containing "1s" will cause the indicated operation to be performed on the corresponding port bit. All bits of the data mask with "0s" cause the corresponding port bits to remain unchanged. Three sample operations are given, using Port B as an example:

| Operation | Set B7 | Bit B2 and B0 | Set B4, B3 and B1 |
|---|---|---|---|
| Address | XXX01101 | XXX01001 | XXX01101 |
| Data | 10000000 | 00000101 | 00011010 |
| Port Pins | | | |
| Prior State | 00001111 | 10001111 | 10001010 |
| Next State | 10001111 | 10001010 | 10011010 |

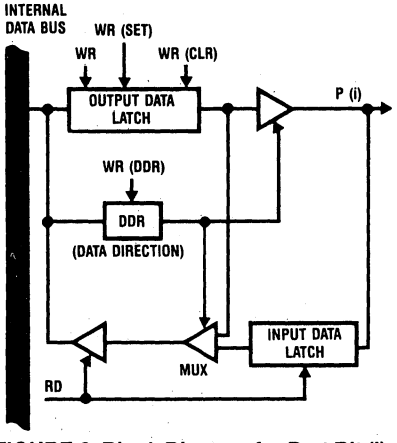



**FIGURE 2. Block Diagram for Port Bit (i)**

## PORT A–STROBED (HANDSHAKE) MODE

Port A can be programmed (via the MDR) into one of 3 types of strobed mode for handshake communication with intelligent peripherals. When Port A is in mode 1, 2, or 3 (see description of MDR), Port C pins 0, 1, and 2 are used as signals to and from the peripheral and to the CPU, controlling handshake operations. These control signals are designated $\overline{STB}$, BF, and $\overline{INTR}$. Timing parameters and timing diagrams are detailed under AC Characteristics.

$\overline{INTR}$ (Strobe Mode Interrupt) is an active-low interrupt from the I/O to the CPU. In strobed input mode, the CPU reads the valid data at Port A to clear the interrupt. In strobed output mode, the CPU clears the interrupt by writing to Port A.

The $\overline{INTR}$ output can be enabled or disabled, thus giving the ability to control strobed data transfer under software control. It is enabled or disabled respectively, by setting (= 1) or clearing (= 0) the output data latch of bit 2, Port C. Port bit PC2 is used as the $\overline{STB}$ input. Since PC2 is always an input during strobed mode of operation, its output data latch is not needed. Therefore, during strobed mode of operation it is internally gated with the interrupt signal to generate the $\overline{INTR}$ output. Reset clears this bit to zero, so it must be set to one to enable the $\overline{INTR}$ pin for strobed operation. Once the strobed mode of operation is programmed, the only way to change the output data latch of PC2 is by using the Bit-Set and Clear instructions. The Port C byte write command will not alter the output data latch of the PC2 during the strobed mode of operation.

$\overline{STB}$ (Strobe) is an active-low input from the peripheral device, signaling that data transfer is about to begin. This strobe is interpreted as an "output request" if Port A is in a strobed output mode, or as a "data valid" signal if Port A is in strobed input mode.

BF (Buffer Full) is an output from the I/O to the peripheral signaling that data transfer is complete. In strobed input mode this strobe indicates that data is received into Port A and that no further data should be transmitted by the peripheral device until the port has been read (emptied). In strobed output mode the BF indicates that the request from the peripheral has been processed by the CPU and the valid data now appears in Port A.

The bits of Port C that are used for handshake control of Port A (bits C0, C1, and C2) must be direction-defined appropriately in the DDR. Also, the DDR of Port A must be consistent with the mode specified in the MDR. Register setup configurations for the three handshake modes are illustrated in Table 2.

**Table 2. Mode Definition Register Configurations**

| Mode | MDR | DDR Port A | DDR Port C | Port C Output Latch |
|---|---|---|---|---|
| Strobed Input | XXXXXX01 | 00000000 | XXX011 | XXX1XX |
| Strobed Output (Active) | XXXXX011 | 11111111 | XXX011 | XXX1XX |
| Strobed Output (TRI-STATE) | XXXXX111 | 11111111 | XXX011 | XXX1XX |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range ..... −65°C to + 150°C
Voltage at Any Pin With Respect to Ground ..... −0.3V to $V_{CC}$ + 0.3V
$V_{CC}$ ..... 7V
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Power Dissipation ..... 1W

**Note:** Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC El[illegible] Characteristics.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

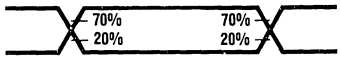
## DC ELECTRICAL CHARACTERISTICS $T_A$ = 0°C to 70°C, $V_{CC}$ = 5V ± 10%, GND =

| Symbol | Parameter | Test Conditions | Min | Typ | Max | |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logical 1 Input Voltage | | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | Logical 0 Input Voltage | | 0 | | 0.2 $V_{CC}$ | V |
| $V_{OH}$ | Logical 1 Output Voltage | $I_{OH}$ = −1.0 mA | 2.4 | | | V |
| | | $I_{OUT}$ = −10 μA | $V_{CC}$ −0.5 | | | V |
| $V_{OL}$ | Logical 0 Output Voltage | $I_{OL}$ = 2 mA | 0 | | 0.4 | V |
| | | $I_{OUT}$ = 10 μA | 0 | | 0.1 | V |
| $I_{IL}$ | Input Leakage Current | $0 \le V_{IN} \le V_{CC}$ | −10.0 | | 10.0 | μA |
| $I_{OL}$ | Output Leakage Current | $0 \le V_{IN} \le V_{CC}$ | −10.0 | | 10.0 | μA |
| $I_{CC}$ | Active Supply Current | $I_{OUT}$ = 0, $t_{WCY}$ = 750 ns | | 8 | 10 | mA |
| $I_Q$ | Quiescent Current | No Input Switching, $T_A$ = 25°C | | 10 | 100 | μA |
| $C_{IN}$ | Input Capacitance | | | 4 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | | 6 | 10 | pF |
| $V_{CC}$ | Power Supply Voltage | | 2.4 | 5 | 6 | V |

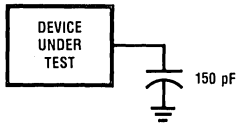
## LOW VOLTAGE OPERATION Preliminary

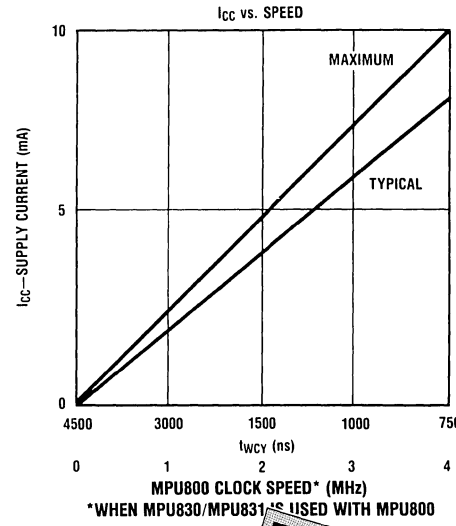
| Voltage | MPU831-1 | MPU831 | MPU831-4 | Units |
|---|---|---|---|---|
| 2.4 | — | 500 | 500 | kHz |
| 3.0 | — | 1 | 1 | MHz |

## AC TESTING INPUT/OUTPUT WAVEFORM




## AC TESTING LOAD CIRCUIT



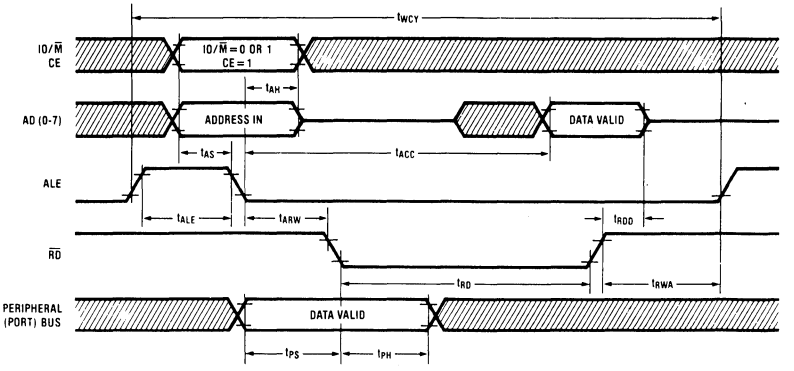

## AC ELECTRICAL CHARACTERISTICS

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

| Symbol | Parameter | Test Conditions | MPU830-1 MPU831-1 | | MPU830 MPU831 | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Access Time from ALE | $C_L$ = 150 pF | | 1000 | | 400 | | 300 | ns |
| $t_{AH}$ | AD0-AD7, CE, IOT/$\overline{M}$ Hold Time | | 100 | | 60 | | 30 | | ns |
| $t_{ALE}$ | ALE Strobe Width (High) | | 200 | | 125 | | 75 | | ns |
| $t_{ARW}$ | ALE to $\overline{RD}$ or $\overline{WR}$ Strobe | | 150 | | 120 | | 75 | | ns |
| $t_{AS}$ | AD0-AD7, CE, IOT/$\overline{M}$ Set-Up Time | | 100 | | 75 | | 40 | | ns |
| $t_{DH}$ | Data Hold Time | | 150 | | 90 | | 40 | | ns |
| $t_{DO}$ | Port Data Output Valid | | | 350 | | 310 | | 300 | ns |
| $t_{DS}$ | Data Set-Up Time | | 100 | | 80 | | 50 | | ns |
| $t_{PE}$ | Peripheral Bus Enable | | | 320 | | 200 | | 200 | ns |
| $t_{PH}$ | Peripheral Data Hold Time | | 150 | | 125 | | 100 | | ns |
| $t_{PS}$ | Peripheral Data Set-Up Time | | 100 | | 75 | | 50 | | ns |
| $t_{PZ}$ | Peripheral Bus Disable (TRI-STATE®) | | | 150 | | 150 | | 150 | ns |
| $t_{RB}$ | $\overline{RD}$ to BF Output | | | 300 | | 300 | | 300 | ns |
| $t_{RD}$ | Read Strobe Width | | 400 | | 320 | | 220 | | ns |
| $t_{RDD}$ | Data Bus Disable | | 0 | 100 | 0 | 100 | 0 | 75 | ns |
| $t_{RI}$ | $\overline{RD}$ to $\overline{INTR}$ Output | | | 320 | | 320 | | 300 | ns |
| $t_{RWA}$ | $\overline{RD}$ to $\overline{WR}$ to Next ALE | | 125 | | 100 | | 75 | | ns |
| $t_{SB}$ | $\overline{STB}$ to BF Valid | | | 300 | | 300 | | 300 | ns |
| $t_{SH}$ | Peripheral Data Hold With Respect to $\overline{STB}$ | | 150 | | 125 | | 100 | | ns |
| $t_{SI}$ | $\overline{STB}$ to INTR Output | | | 300 | | 300 | | 300 | ns |
| $t_{SS}$ | Peripheral Data Set-Up With Respect to $\overline{STB}$ | | 100 | | 75 | | 50 | | ns |
| $t_{SW}$ | $\overline{STB}$ Width | | 400 | | 320 | | 220 | | ns |
| $t_{WB}$ | $\overline{WR}$ to BF Output | | | 340 | | 340 | | 300 | ns |
| $t_{WI}$ | $\overline{WR}$ to $\overline{INTR}$ Output | | | 320 | | 320 | | 300 | ns |
| $t_{WR}$ | $\overline{WR}$ Strobe Width | | 400 | | 320 | | 220 | | ns |
| $t_{WCY}$ | Width of Machine Cycle | | 3000 | | 1200 | | 750 | | ns |

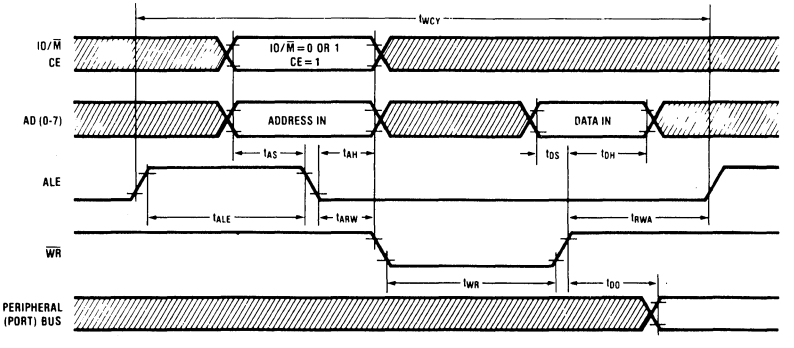
## GENERAL TIMING WAVEFORMS

### Read Cycle (Read from ROM or Port)



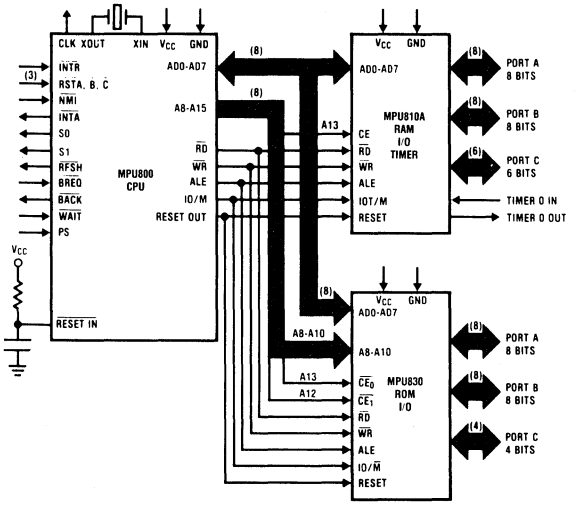

Note: Diagonal lines indicate interval of invalid data.

### Write Cycle (Write to Port)



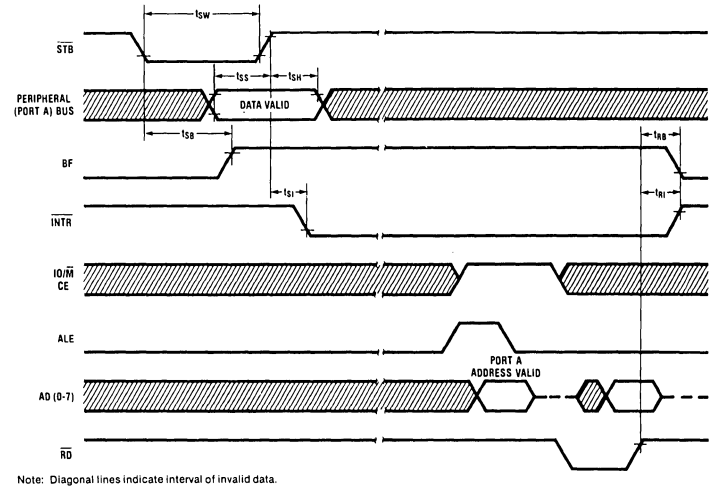

Note: Diagonal lines indicate interval of invalid data.

## MICROCOMPUTER FAMILY BLOCK DIAGRAM



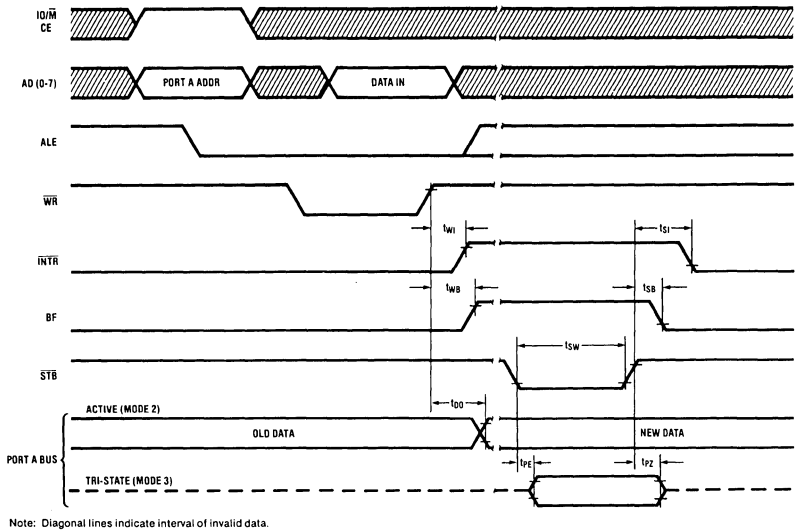
## HANDSHAKE TIMING

**Strobed Mode Output**




Note: Diagonal lines indicate interval of invalid data.

**Strobed Mode Input**




Note: Diagonal lines indicate interval of invalid data.

## APPROVED FORMATS FOR CUSTOM PROGRAMMED PARTS

**Input Medium:**

2716 EPROM
2708 EPROM

### IMPORTANT–EPROM LABELING

Only one customer program may be included in a single order. The following method must be used to identify the EPROMs comprising a program.

a. The EPROMs used for storing a custom program are designated as shown:

| | | |
|---|---|---|
| 2716: | Block A | 0-2047 |
| 2708: | Block A | 0-1023 |
| | Block B | 1024-2047 |

b. All EPROMs must be labeled (stickers, paint, etc.) with this block designation plus a customer assigned print or identification number.

Example:

1. Customer Data
   - Custom Program Length–2K
   - Medium–Two 2708s
   - Customer Print or I.D. No. C123-45
2. EPROM Labels

| | |
|---|---|
| C123-45<br>A<br>0-1023 | C123-45<br>B<br>1024-2047 |

### Verification

You will receive a listing of the options ordered and the input data. If you also wish to receive EPROMs for verification, please send additional blank EPROMs as necessary for this purpose. You can use software (the listing) or hardware (EPROMs) to verify the program.

You will be asked for GO/NO GO response within one week after you receive the listing.

### VERIFICATION LISTING

The verification listing has six sections:

1. A cover sheet with provision for "STOP, DO NOT PROCEED" or "VERIFICATION CERTIFIED" signatures.
2. Description of the options you have chosen.
3. A description of the log designations and assumptions used to process the data.
4. A listing of the data you have submitted.
5. An error summary.
6. A definition of the standard logic definitions for the ROM and the reduced form of the data. This list shows the output word corresponding to each address coded in binary.

---

### ORDERING INFORMATION FOR CUSTOM PROGRAMMED PARTS

The following information must be submitted with each custom ROM program. An order will not be processed unless it is accompanied by this information.

| | |
|---|---|
| Person (Customer, Sales Representative, etc. )to whom Verification Package be sent: | SMC PART NUMBER AND PACKAGE |
| Name | ROM Letter Code (SMC Use Only) |
| Company | Customer Name and Location |
| Address | Customer Print or I.D. Number for this ROM Program |
| City, State, and Zip Code | Purchase Order Number |
| Person (Customer) SMC Can Contact for Technical Questions | Device Marking Instruction (Unless otherwise instructed. SMC will always mark devices with Date Code, SMC Part No., and ROM Code. Any additional marking should be shown below.) |
| Telephone Number | |
| Sales Representative | Customer Service Representative |

**INPUT MEDIUM**

See following page for approved formats. Please check the medium you are using.

☐ 2716 EPROM
☐ 2708 EPROM
____ Total number of EPROMs

**OPTIONS FOR MPU830 ROM–I/O**

Option 1 = ☐
$CE_0$ Select, enter: 0 for $CE_0$
1 for $CE_0$

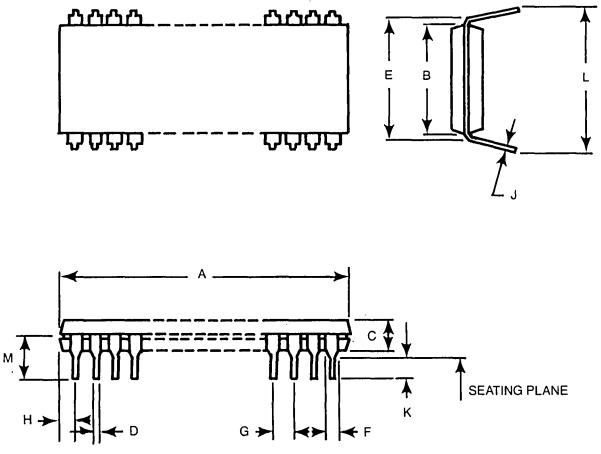
Option 2 = ☐
$CE_1$/IOR Select, enter: 0 for IOR
1 for $CE_1$
2 for $CE_1$

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd Hauppauge N Y 11788
(516) 273-3100 TWX-510-227-8898

Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.

STANDARD MICROSYSTEMS CORPORATION

# Plastic Package Outlines

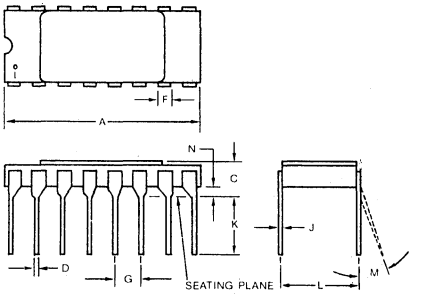



| DIM | 8 LEAD | 14 LEAD | 16 LEAD | 18 LEAD | 20 LEAD | 24 LEAD | 28 LEAD | 40 LEAD |
|---|---|---|---|---|---|---|---|---|
| A | .380-.400 | .750-.770 | .750-.770 | .900-.920 | 1.025-1.050 | 1.245-1.265 | 1.450-1.470 | 2.050-2.070 |
| B | .240-.250 | .240-.250 | .240-.250 | .240-.250 | .240-.260 | .530-.545 | .535-.550 | .535-.550 |
| C | .125-.135 | .125-.135 | .130-.140 | .125-.140 | .125-.140 | .145-.155 | .145-.155 | .145-.155 |
| D | .016-.021 | .016-.021 | .016-.021 | .016-.021 | .016-.021 | .016-.021 | .016-.021 | .016-.021 |
| E | .290-.330 | .290-.330 | .290-.330 | .290-.330 | .290-.330 | .590-.630 | .590-.630 | .590-.630 |
| F | .055-.065 | .060-.070 | .060-.070* | .060-.070 | .060-.070 | .060-.070 | .060-.070 | .050-.060 |
| G | .090-.110 | .090-.110 | .090-.110 | .090-.110 | .090-.110 | .090-.110 | .090-.110 | .090-.110 |
| H | .040-.050 | .075-.085 | .025-.035 | .040-.060 | .065-.075 | .065-.085 | .070-.090 | .070-.090 |
| J | .010-.014 | .010-.014 | .010-.014 | .010-.014 | .010-.014 | .010-.014 | .010-.014 | .010-.014 |
| K | .120-.140 | .120-.140 | .120-.140 | .120-.140 | .120-.140 | .120-.140 | .120-.140 | .120-.140 |
| L | .315-.370 | .315-.365 | .315-.365 | .315-.365 | .315-.365 | .610-.670 | .610-.670 | .610-.670 |
| M | .210-.250 | .210-.250 | .210-.250 | .210-.250 | .210-.250 | .210-.250 | .210-.250 | .210-.250 |

*.045 TYP FOR END LEADS

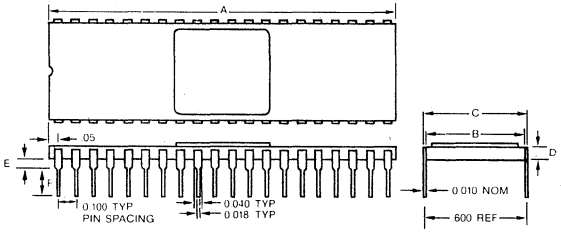
# Ceramic Package Outlines

## 14, 16, 18, 20 PIN HERMETIC PACKAGE




| | 14 LEAD | | 16 LEAD | | 18 LEAD | | 20 LEAD | |
|---|---|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| A | .670 | .760 | .790 | .810 | .885 | .915 | .965 | .995 |
| C | | .175 | | .175 | | .175 | | .175 |
| D | .015 | .021 | .015 | .021 | .015 | .021 | .015 | .021 |
| F | .048 | .060 | .048 | .060 | .048 | .060 | .048 | .060 |
| G | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| J | .008 | .012 | .008 | .012 | .008 | .012 | .008 | .012 |
| K | .130 | .170 | .130 | .170 | .130 | .170 | .130 | .170 |
| L | .295 | .325 | .295 | .325 | .295 | .325 | .295 | .325 |
| M | | 10° | | 10° | | 10° | | 10° |
| N | .025 | .060 | .025 | .060 | .025 | .060 | .025 | .060 |

## 24, 28, 40 LEAD HERMETIC DIP

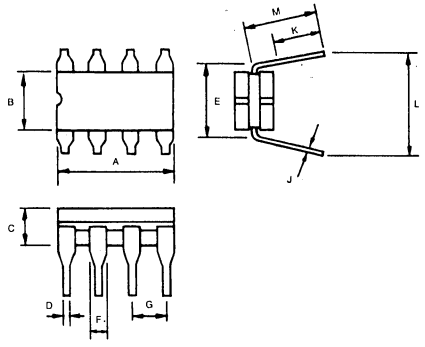



| | 24 LEAD | | 28 LEAD | | 40 LEAD | |
|---|---|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX | MIN | MAX |
| A | 1.188 | 1.212 | 1.386 | 1.414 | 1.980 | 2.020 |
| B | .568 | .598 | .568 | .598 | .568 | .598 |
| C | .590 | .610 | .590 | .610 | .590 | .610 |
| D | .070 | .090 | .070 | .090 | .070 | .090 |
| E | .025 | .060 | .025 | .060 | .025 | .060 |
| F | .130 | .170 | .130 | .170 | .130 | .170 |

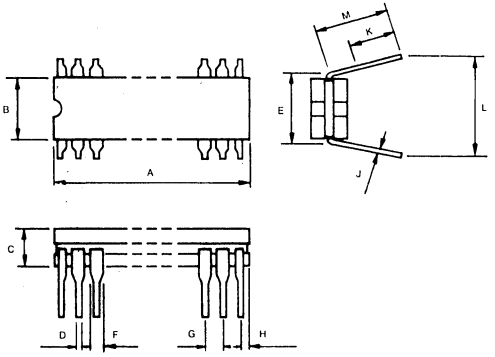
ALL UNITS INCHES UNLESS OTHERWISE SPECIFIED

# Cerdip Package Outlines

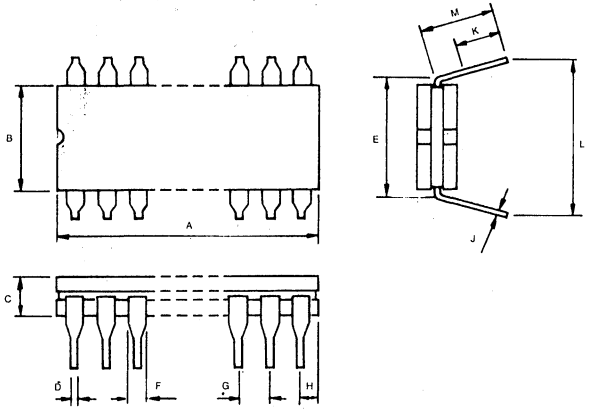
### 8 LEAD CERDIP PACKAGES




### 14, 16, 18, 20 LEAD CERDIP PACKAGES




### 24, 28, 40 LEAD CERDIP PACKAGES

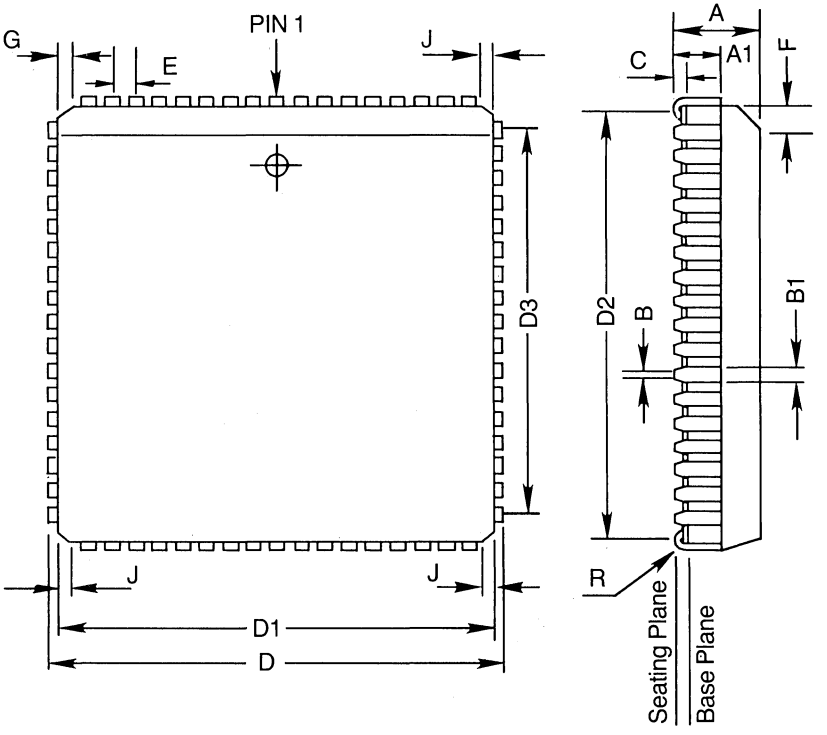



| DIM | 8 LEAD | 14 LEAD | 16 LEAD | 18 LEAD | 20 LEAD | 24 LEAD | 28 LEAD | 40 LEAD |
|---|---|---|---|---|---|---|---|---|
| A | .400 MAX | .785 MAX | .810 MAX | .915 MAX | .970 MAX | 1.280 MAX | 1.460 MAX | 2.070 MAX |
| B | .245-.295 | .244-.295 | .244-.295 | .265-.295 | .265-.295 | .510-.595 | .510-.595 | .510-.595 |
| C | .160 MAX | .160 MAX | .180 MAX | .180 MAX | .180 MAX | .180 MAX | .180 MAX | .180 MAX |
| D | .016-.020 | .016-.020 | .016-.020 | .016-.020 | .016-.020 | .016-.020 | .016-.020 | .016-.020 |
| E | .290-.320 | .290-.320 | .290-.320 | .310-.330 | .310-.330 | .590-.620 | .590-.620 | .590-.620 |
| F | .050-.070 | .050-.070 | .050-.070 | .050-.070 | .050-.070 | .050-.070 | .050- .070 | .050-.070 |
| G | .100 ± .010 | .100 ± .010 | .100 ± .010 | .100 ± .010 | .100 ± .010 | .100 ± .010 | .100 ± .010 | .100-.010 |
| H | — | .065 TYP | .020 TYP | .040 TYP | .020 TYP | .045 TYP | .045 TYP | .045 TYP |
| J | .008-.012 | .008-.012 | .008-.012 | .008-.012 | .008-.012 | .008-.012 | .008-.012 | .008-.012 |
| L | .400 MAX | .400 MAX | .400 MAX | .400 MAX | .400 MAX | .700 MAX | .700 MAX | .700 MAX |
| M | .240-.300 | .240-.300 | .240-.300 | .240-.300 | .240-.300 | .240-.300 | .240-.300 | .240-.300 |
| K | .125 MIN | .125 MIN | .125 MIN | .125 MIN | .125 MIN | .125 MIN | .125 MIN | .125 MIN |

# Plastic Surface Mount Package Outlines
# 28, 44, 68 J-Lead Carrier

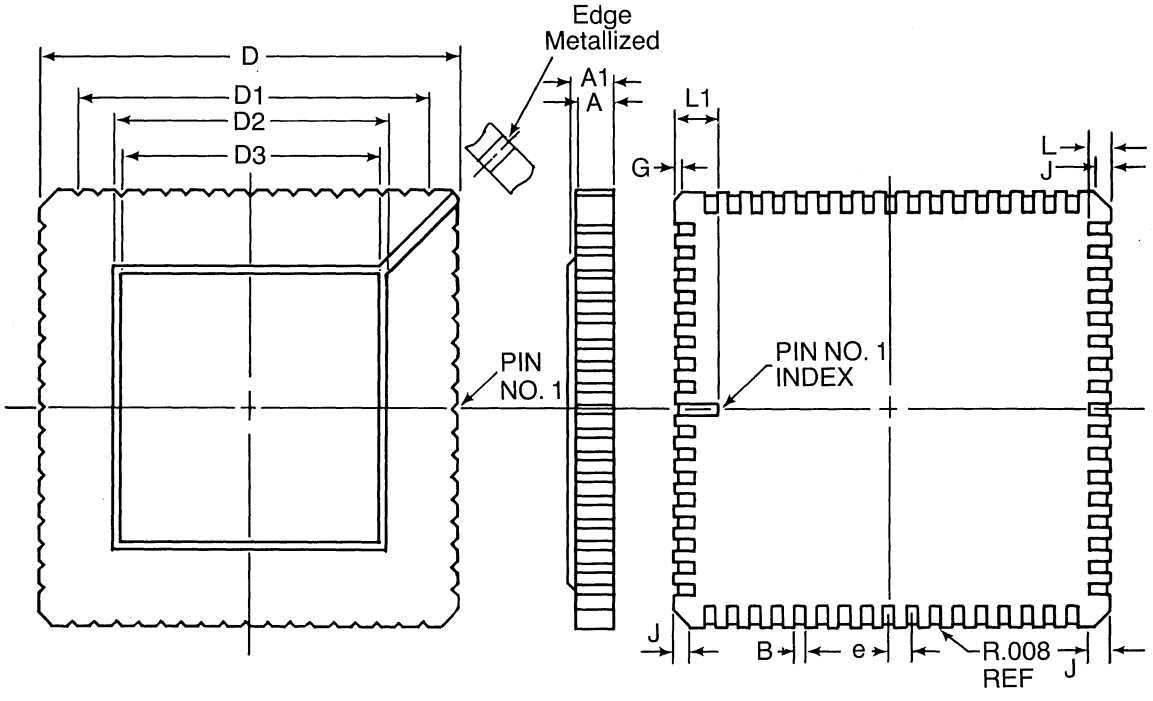
NOTE:

1. All dimensions are in inches.
2. Circle indicating pin 1 can appear on a top surface as shown on the drawing or right above it on a beveled edge.




| DIM | 28L | 44L | 68L |
|---|---|---|---|
| A | .160-.188 | .160-.188 | .160-.190 |
| A1 | .090-.120 | .090-.120 | .090-.130 |
| D | .482-.495 | .682-.695 | .982-.995 |
| D1 | .450-.456 | .650-.656 | .950-.956 |
| D2 | .390-.430 | .590-.630 | .890-.930 |
| F | .042-.056 | .042-.060 | .042-.062 |
| G | .042-.048 | .042-.048 | .042-.048 |
| J | .000-.020 | .000-.028 | .00-.028 |
| E | .047-.053 | .047-.053 | .047-.053 |
| R | .025-.045 | .025-.045 | .025-.045 |
| B | .013-.021 | .013-.021 | .013-.021 |
| B1 | .026-.032 | .026-.032 | .026-.032 |
| C | .020-.045 | .020-.045 | .020-.045 |

# Ceramic Leadless Chip Carrier Outlines




| DIM | 44 LEAD | 68 LEAD |
|---|---|---|
| A | .062 - .078 | .072 - .088 |
| A1 | .071 - .089 | .081 - .099 |
| B | .025TYP | .025TYP |
| D | .640 - .660 | .940 - .965 |
| D1 | .500 | .800 |
| D2 | .355 - .598 | .455 - .820 |
| D3 | .350 - .590 | .450 - .820 |
| e | .050TYP | .050TYP |
| G | .020 x 45° | .020 x 45° |
| J | .040 x 45° | .040 x 45° |
| L | .045 - .055 | .045 - .055 |
| L1 | .075 - .095 | .075 - .095 |

# STANDARD MICROSYSTEMS CORPORATION

# SALES REPRESENTATIVES

**REGIONAL OFFICES**

**EAST COAST SALES/ APPLICATIONS OFFICE**
Standard Microsystems Corporation
35 Marcus Blvd.
Hauppauge, NY 11788
**(516) 273-3100**
**TLX: (510) 227-8898**

**IBM SALES/ APPLICATIONS OFFICE**
Standard Microsystems Corporation
35 Marcus Blvd.
Hauppauge, NY 11788
**(516) 273-3100**
**TLX: (510) 227-8898**

**NORTHEAST SALES/ APPLICATIONS OFFICE**
Standard Microsystems Corporation
1 Tara Blvd., Suite 202
Nashua, NH 03062
**(603) 886-1107**
**TLX: 953027**

**NORTH CENTRAL SALES OFFICE**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive,
Ste. 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**NORTH CENTRAL APPLICATIONS OFFICE**
Standard Microsystems Corporation
250 South Stemmons,
Ste. 334
Lewisville, TX 45067
**(214) 436-4009**

**WESTERN SALES OFFICE**
Standard Micro Sales
4010 Moorpark, Ste. 105
San Jose, CA 95117
**(408) 249-5000**

**WESTERN APPLICATIONS OFFICE**
Turk Enterprises
2172 Dupont Drive
Patio Building
Irvine, California 92715
**(714) 955-1575**
**TLX: (910) 595-2635**

**ALABAMA**
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, AL 35805-0306
**(205) 536-3044**

**ARIZONA**
RELCOM, Inc.
4314 E. Tonto St.
Phoenix, AZ 85044
**(602) 893-1209**
**TLX: (910) 950-0195**

**ARKANSAS**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive
Suite 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**CALIFORNIA**
Cerco
5230 Carroll Canyon Rd.
Ste. 214
San Diego, CA 92121
**(619) 450-1755**
**TLX: (910) 335-1220**

Costar, Inc.
19220 Stevens Creek Blvd.
Cupertino, CA 95014
**(408) 446-9339**
**TLX: (910) 338-0206**

Varigon Associates
137 Eucalyptus Drive
El Segundo, CA 90245
**(213) 634-2116**

Varigon Associates
22932 El Toro Rd. Ste. 5
El Toro, CA 92630
**(714) 855-0233**
**TLX: (910) 997-0225**

**COLORADO**
Elcom, Inc.
2015 South Dayton St.
Suite 100
Denver, CO 80231
**(303) 337-2300**
**Easylink No.: 62927893**

**CONNECTICUT**
Orion Group
27 Meriden Avenue
Southington, CT 06489
**(203) 621-8371**
**TLX: (510) 601-1381**

**DELAWARE**
Tritek Sales, Inc.
21 E. Euclid Avenue
Haddonfield, NJ 08033
**(609) 429-1551**
**TLX: (710) 896-0881**

**FLORIDA**
Semtronic Associates, Inc.
657 Maitland Avenue
Altamonte Springs, FL 32701
**(305) 831-8233**
**TLX: (810) 854-0321**

Semtronic Associates, Inc.
1467 S. Missouri Avenue
Clearwater, FL 33516
**(813) 461-4675**

Semtronic Associates, Inc.
3471 N.W. 55th Street
Fort Lauderdale, FL 33309
**(305) 731-2484**
**TLX: (810) 848-0074**

**GEORGIA**
Electronic Marketing Associates
6695 Peachtree Industrial Blvd.
Suite 109
Atlanta, GA 30360
**(404) 448-1215**

**IDAHO**
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, WA 98008
**(206) 747-9424**
**TLX: (206) 747-9426 (FAX)**

**ILLINOIS**
Sumer, Inc.
1675 Hicks Road
Rolling Meadows, IL 60008
**(312) 991-8500**
**TLX: (910) 693-1477**

**INDIANA**
Wilson Technical Sales, Inc.
4622 W. 72nd Street
Post Office Box 40699
Indianapolis, IN 46268
**(317) 298-3345**
**TLX: (910) 997-8120**

**IOWA**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive
Suite 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**KANSAS**
S. W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, KS 66072
**(913) 898-6552**

**KENTUCKY**
Wilson Technical Sales, Inc.
4622 W. 72nd Street
Post Office Box 40699
Indianapolis, IN 46268
**(317) 298-3345**
**TLX: (910) 997-8120**

**LOUISIANA**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive
Suite 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**MAINE**
Alpha-Omega Sales Corporation
10-G Roessler Road
Woburn, MA 01801
**(617) 933-0237**
**TLX: (910) 997-1119**

**MARYLAND**
Robert Electronic Sales
5525 Twin Knolls Rd.
Ste. 325
Columbia, MD 21045
**(301) 995-1900**

**MASSACHUSETTS**
Alpha-Omega Sales Corporation
10-G Roessler Road
Woburn, MA 01801
**(617) 933-0237**
**TLX: (910) 997-1119**

**MICHIGAN**
A. P. Associates
9903 Weber
Post Office Box 777
Brighton, MI 48116
**(313) 229-6550**
**TLX: 287310 APAIUR**

**MINNESOTA**
Comstrand, Inc.
2852 Anthony Lane So.
Minneapolis, MN 55418
**(612) 788-9234**
**TWX: 910-576-0924**

**MISSISSIPPI**
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, AL 35805-0306
**(205) 536-3044**

**MISSOURI**
Abrams & Associates
67 Ladue Estates
St. Louis, MO 63141
**(314) 569-0447**

**MONTANA**
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, WA 98008
**(206) 747-9424**
**TLX: (206) 747-9426 (FAX)**

**NEBRASKA**
S. W. Wollard Co.
Rural Route 1
Post Office Box 66A
Parker, KS 66072
**(913) 898-6552**

**NEVADA**
RELCOM, Inc.
4314 E. Tonto St.
Phoenix, AZ 85044
**(602) 893-1209**
**TLX: (910) 950-0195**

**NEW JERSEY**
Tritak Sales, Inc.
21 E. Euclid Avenue
Haddonfield, NJ 08033
**(609) 429-1551**
**TLX: (710) 896-0881**

**NEW HAMPSHIRE**
Alpha-Omega Sales Corporation
10-G Roessler Road
Woburn, MA 01801
**(617) 933-0237**
**TLX: (910) 997-1119**

**NEW MEXICO**
RELCOM, Inc.
4314 E. Tonto St.
Phoenix, AZ 85044
**(602) 893-1209**
**TLX: (910) 950-0195**

**NEW YORK**
Standard Microsystems Corporation
35 Marcus Blvd.
Hauppauge, NY 11788
**(516) 273-3100**
**TLX: (510) 227-8898**

T-Squared Elec. Co. Inc.
7353 Victor-Pittsford Rd.
Victor, NY 14564
**(718) 924-9101**
**TWX: (910) 997-8005**
**Faxs Line 62522970**

T-Squared Elec. Co., Inc.
6443 Ridings Road
Syracuse, NY 13206
**(315) 463-8592**

**NORTH CAROLINA**
Electronic Marketing Associates
9225 Honeycutt Creek Road
Raleigh, NC 27609
**(919) 847-8800**
**TLX: (510) 928-0594**

**NORTH DAKOTA**
Comstrand, Inc.
2852 Anthony Lane So.
Minneapolis, MN 55418
**(612) 788-9234**
**TWX: 910-576-0924**

**OHIO**
Thompson & Associates
23715 Mercantile Road
Beachwood, OH 44122
**(216) 831-6277**
**TLX: (810) 427-9453**

Thompson & Associates
309 Regency Ridge
Dayton, OH 45459
**(513) 435-7733**
**TLX: (810) 459-1767**

**OKLAHOMA**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive
Suite 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**OREGON**
Quest Marketing, Inc.
6700 S. W. 105th, Ste. 311D
Beaverton, OR 97005
**(503) 641-7377**

**PENNSYLVANIA**
Thompson & Associates
309 Regency Ridge
Dayton, OH 45459
**(513) 435-7733**
**TLX: (810) 459-1767**

Tritek Sales, Inc.
21 E. Euclid Avenue
Haddonfield, NJ 08033
**(609) 429-1551**
**TLX: (710) 896-0881**

**PUERTO RICO**
Semtronic Associates, Inc.
3471 N.W. 55th Street
Fort Lauderdale, FL 33309
**(305) 731-2484**
**TLX: (810) 848-0074**

**RHODE ISLAND**
Alpha-Omega Sales Corporation
10-G Roessler Road
Woburn, MA 01801
**(617) 933-0237**
**TLX: (910) 997-1119**

**SOUTH CAROLINA**
Electronic Marketing Associates
210 West Stone Avenue
Greenville, SC 29609-5499
**(803) 233-4637/4638**
**TLX: (810) 281-2225**

**SOUTH DAKOTA**
Comstrand, Inc.
2852 Anthony Lane So.
Minneapolis, MN 55418
**(612) 788-9234**
**TWX: 910-576-0924**

**TENNESSEE**
Electronic Marketing Assoc.
1200 Jordan Lane, Ste. 4
Jordan Center
Huntsville, AL 35805-0306
**(205) 536-3044**

**TEXAS**
Standard Microsystems Corporation
Post Office Box 292497
3411 Office Park Drive
Suite 106
Kettering, OH 45429
**(513) 293-5393**
**TLX: (810) 459-1617**

**UTAH**
Elcom, Inc.
2520 South State St.
Suite 116
Salt Lake City, UT 84115
**(801) 486-4233**
**Easylink No.: 62893625**

**VERMONT**
Alpha-Omega Sales Corporation
10-G Roessler Road
Woburn, MA 01801
**(617) 933-0237**
**TLX: (910) 997-1119**

**VIRGINIA**
Robert Electronic Sales
7641 Hull Street Rd., Ste. 101
Richmond, VA 23235
**(804) 276-3979**

**WASHINGTON**
Quest Marketing, Inc.
15921 N.E. 8th St., Ste. 207
Bellevue, WA 98008
**(206) 747-9424**
**TLX: (206) 747-9426 (FAX)**

**WASHINGTON D.C.**
Robert Electronic Sales
5525 Twin Knolls Rd.
Ste. 331
Columbia, MD 21045
**(301) 995-1900**

**WEST VIRGINIA**
Thompson Associates
23715 Marchantile Road.
Beachwood, OH 44122
**(216) 831-6277**
**TLX: (810) 427-9453**

**WISCONSIN**
Eastern
Sumer, Inc.
350 Bishops Way
Brookfield, WI 53005
**(414) 784-6641**
**TLX: (510) 101-1742**

Western
Comstrand, Inc.
2852 Anthony Lane So.
Minneapolis, MN 55418
**(612) 788-9234**
**TWX: 910-576-0924**

# DISTRIBUTORS

**ALABAMA**
Hall-Mark Electronics Corp.
4900 Bradford Drive
Huntsville, AL 35807
**(205) 837-8700**

**ARIZONA**
Cetec Electronics
3617 N. 35th Avenue
Phoenix, AZ 85017
**(602) 272-7951**

Hall-Mark Electronics Corp.
4040 East Raymond
Phoenix, AZ 85040
**(602) 437-1200**

Western Microtechnology, Inc.
7848 East Redfield Drive
Suite 17
Scottsdale, AZ 85260
**(602) 948-4240**

**CALIFORNIA**
Cetec Electronics
5610 E. Imperial Highway
South Gate, CA 90280
**(213) 773-6521**

Cetec Electronics
1692 Browning
Irvine, CA 92714
**(714) 250-4141**

Cetec Electronics
3940 Ruffin Road
San Diego, CA 92123
**(619) 278-5020**

Cetec Electronics
2300 Owen Street
Santa Clara, CA 95051
**(408) 748-8550**

Diplomat Electronics, Inc.
20151 Bahama Street
Chatsworth, CA 91311
**(818) 341-4411**

Diplomat Electronics, Inc.
9787 Aero Drive
San Diego, CA 92123
**(619) 292-5693**

Diplomat Electronics, Inc.
1310 Kifer Road
Sunnyvale, CA 94086
**(408) 737-0204**

Hall-Mark Electronics Corp.
6341 Auburn Blvd.
Suite D
Citrus Heights, CA 95610
**(916) 722-8600**

Hall-Mark Electronics Corp.
8130 Remmet Avenue
Canoga Park, CA 93104
**(818) 716-7300**

Hall-Mark Electronics Corp.
19220 S. Normandie Avenue
Torrance, CA 90502
**(213) 217-8450**

Hall-Mark Electronics Corp.
14831 Franklin Avenue
Tustin, CA 92680
**(714) 669-4700**

Western Microtechnology, Inc.
10040 Bubb Road
Cupertino, CA 95014
**(408) 725-1660**

**COLORADO**
Hall-Mark Electronics Corp.
6950 Tucson Way So.
Suite 206
Englewood, CO 80112
**(303) 790-1662**

# DISTRIBUTORS (con't)

**CONNECTICUT**
Diplomat Electronics, Inc.
52 Federal Road
Danbury, CT 06810
**(203) 797-9674**

Hall-Mark Electronics Corp.
Barnes Industrial Park W.
33 Village Lane,
P.O. Box 5024
Wallingford, CT 06492
**(203) 269-0100**

Milgray Electronics, Inc.
378 Boston Post Road
Orange, CT 06477
**(203) 795-0711**

**FLORIDA**
Diplomat Electronics, Inc.
2120 Calumet Street
Clearwater, FL 33515
**(813) 443-4514**

Diplomat Electronics, Inc.
1300 N.W. 65th Place
Fort Lauderdale, FL 33309
**(305) 974-8700**

Hall-Mark Electronics Corp.
15301 Roosevelt Blvd.
Suite 303
Clearwater, FL 33520
**(813) 530-4543**

Hall-Mark Electronics Corp.
7648 Southland Blvd.
Suite 100
Orlando, FL 32809
**(305) 855-4020**

Hall-Mark Electronics Corp.
3161 S.W. 15th St.
Pompano Beach, FL 33069
**(305) 971-9280**

Milgray Electronics, Inc.
1850 Lee Road, Suite 104
Winter Park, FL 32789
**(305) 647-5747**
**(800) 327-5262**

**GEORGIA**
Hall-Mark Electronics Corp.
6410 Atlantic Blvd.
Suite 115
Norcross, GA 30071
**(404) 447-8000**

Milgray Electronics, Inc.
17 Dunwoody Park, Suite 102
Atlanta, GA 30338
**(404) 393-9666**
**(800) 241-5523**

**IOWA**
Advent Electronics
682 58th Avenue S.W.
Cedar Rapids, IA 52404
**(319) 363-0221**

**ILLINOIS**
Hall-Mark Electronics Corp.
210 Mittel Drive
Wood Dale, IL 60191
**(312) 860-3800**

Mar-Con
4836 Main Street
Skokie, IL 60076
**(312) 675-6450**

**INDIANA**
Advent Electronics
8446 Moller Road
Indianapolis IN 46268
**(317) 872-4910**

Hall-Mark Electronics Corp.
4275 W. 96th Street
Indianapolis, IN 46268
**(317) 872-8875**

**KANSAS**
Hall-Mark Electronics Corp.
10815 Lakeview Drive
Lenexa, KS 66215
**(913) 888-4747**

Milgray Electronics, Inc.
6901 West 63rd Street
Overland Park, KS 66202
**(913) 236-8800**

**MARYLAND**
Diplomat Electronics, Inc.
9150 Rumsey Road
Suite A6
Columbia, MD 21045
**(301) 995-1226**

Hall-Mark Electronics Corp.
10240 Old Columbia Road
Columbia, MD 21046
**(301) 988-9800**

Milgray Electronics, Inc.
9801 Broken Land Pkwy 103
Columbia, MD 21046-1145
**(301) 621-6169**

**MASSACHUSETTS**
Diplomat Electronics, Inc.
28 Cummings Park
Woburn, MA 01801
**(617) 935-6611**

Hall-Mark Electronics Corp.
6 Cook Street
Pinehurst Park
Billerica, MA 01801
**(617) 935-9777**

Milgray Electronics, Inc.
79 Terrace Hall Ave.
Burlington, MA 01803
**(617) 272-6800**

RC Components
222 Andover Street
Wilmington, MA 01887
**(617) 273-1860**

**MICHIGAN**
Advent Electronics
24713 Crestview Court
Farmington Hills, MI 48018
**(313) 477-1650**

**MINNESOTA**
Hall-Mark Electronics Corp.
10300 Valley View Rd.
Suite 10
Eden Prairie, MN 55344
**(612) 941-2600**

**MISSOURI**
Hall-Mark Electronics Corp.
13750 Shoreline Drive
Earth City, MO 63045
**(314) 291-5350**

**NEW JERSEY**
Diplomat Electronics
2091 Springdale Road
Suite 2
Cherry Hill, NJ 08003
**(609) 751-0440**

Diplomat Electronics, Inc.
490 South Riverview Drive
Totowa, NJ 07512
**(201) 785-1830**

Hall-Mark Electronics Corp.
107 Fairfield Road
Suite 18
Fairfield, NJ 07006
**(201) 575-4415**

Hall-Mark Electronics Corp.
1000 Midlantic Drive
Mt. Laurel, NJ 08034
**(609) 235-1900**

Milgray Electronics, Inc.
3002 Greentree
Executive Campus
Marlton, NJ 08053
**(609) 983-5010**
**(800) 257-7808/7111**

**NEW YORK**
ADD Electronics
7 Adler Drive
East Syracuse, New York
13057
**(315) 437-0300**

Current Components
215 Marcus Boulevard
Hauppauge, NY 11788
**(516) 273-2600**

Diplomat Electronics, Inc.
4610 Wetzel Road
Liverpool, NY 13088
**(315) 652-5000**

Diplomat Electronics, Inc.
110 Marcus Drive
Melville, NY 11747
**(516) 454-6334**

Hall-Mark Electronics Corp.
101 Comac Street
Ronkonkoma, NY 11779
**(516) 737-0600**

Milgray Electronics, Inc.
77 Schmitt Blvd.
Farmingdale, NY 11735
**(516) 420-9800**

Milgray Electronics, Inc.
57 Monroe Avenue
Pittsford, NY 14534
**(716) 385-9330**

**NORTH CAROLINA**
Hall-Mark Electronics Corp.
5237 North Blvd. Suite D
Raleigh, NC 27604
**(919) 872-0712**

**OHIO**
Hall-Mark Electronics Corp.
400 E. Wilson Bridge Road
Suite S
Worthington, OH 43085
**(614) 888-3313**

Hall-Mark Electronics Corp.
5821 Harper Road
Solon, OH 44139
**(216) 349-4632**

Milgray Electronics, Inc.
6155 Rockside Road
Cleveland, OH 44131
**(216) 477-1520**
**(800) 321-0006**

**OKLAHOMA**
Quality Components Inc.
9934 E. 21st Street
Tulsa, OK 74129
**(918) 664-8812**

**PENNSYLVANIA**
QED Electronics, Inc.
805 N. Bethlehem Pike
Box 487
Spring House, PA 19477
**(215) 643-9200**
**Easylink No. 6293-1798**

**TEXAS**
Hall-Mark Electronics Corp.
12211 Technology Blvd.
Austin, TX 78727
**(512) 258-8848**

Hall-Mark Electronics Corp.
10375 Brockwood Road
Dallas, TX 75238
**(214) 553-4300**

Hall-Mark Electronics Corp.
8000 Westglen
Houston, TX 77063
**(713) 781-6100**

Quality Components, Inc.
4257 Kellway Circle
P.O. Box 819
Addison, TX 75001
**(214) 733-4300**

Quality Components, Inc.
2120-M Breaker Lane
Austin, TX 78758
**(512) 835-0220**

Quality Components, Inc.
1005 Industrial Blvd.
Sugar Land, TX 77478
**(713) 491-2255**

**UTAH**
Diplomat Electronics, Inc.
3007 S.W. Temple
Salt Lake City, UT 84115
**(801) 486-4134**

Hall-Mark Electronics Corp.
302 West 5400 South
Suite 109
Murray, UT 84107
**(801) 268-3779**

**WASHINGTON**
Western Microtechnology, Inc.
14636 N.E. 95th Street
Redmond, WA 98052
**(206) 881-6737**

**WISCONSIN**
Hall-Mark Electronics Corp.
16255 W. Lincoln Avenue
New Berlin, WI 53153
**414-797-7844**

**CANADA**
Future Electronics, Inc.
Unit 2
3220 5th Ave. N.E.
Calgary, Alberta T2A 5NI
**(403) 235-5325**

Future Elec.
82 St. Regis Crescent No.
Downsview, ON M3J 123
**(416) 638-4771**
**Telex: (610) 491-1470**

Future Elec.
237 Hymus Blvd.
(Pointe Claire)
Montreal, PQ H9R 5C7
**(514) 694-7710**

Future Elec.
Baxter Center
1050 Baxter Road
Ottawa, ON K2C 3P2
**(613) 820-8313**

Future Elec.
3070 Kingsway
Vancouver, B.C. U5R 5J7
**(604) 294-1166**

Prelco Electronics, Ltd.
7611 Bath Road
Mississauga, ON L4T 3T1
**(416) 745-9370**

Prelco Elec.
480 Port Royal St. W.
Montreal, PQ H3L 2R9
**(514) 389-8051**

Prelco Elec.
195 Stafford Road W.
Ottawa, ON K2H 9C1
**(813) 726-1800**

# INTERNATIONAL SALES REPRESENTATIVES AND DISTRIBUTORS

**EUROPEAN SALES OFFICE**
Standard Microsystems Gmbh
Arabellastrasse 5-Buero 131
D-8000 Muenchen 81
West Germany
**49-89-919594**
**TLX: 5214433 SMCG**

**APPLICATIONS CENTER FAR EAST**
Standard Microsystems Corporation
(Asia) Taiwan Branch
7F-1, 665
Tun Hua S. Road
Taipei, Taiwan R.O.C.
**02-700-5457**
**TLX: 21664 SMCTW**

**ARGENTINA**
Electroquimica Delta Ind. Comp. Timoteo Gordillo 72
COD Postal 1408
Buenos Aires-R
**641-3193**
**TLX: 21212 AR EDELTA**

**AUSTRIA**
Othmar Lackner
Elektron Bauelement und Gerate
Landstr Hauptstr 37
A-1031 Vienna
**43-222-75-26-18**

**AUSTRALIA**
Total Electronics
9 Harker Street
Burwood, Victoria 3125
**03-288-4044**
**TLX: AA31261**

**BELGIUM**
Auriema Belgium S.A./N.V.
Rue Brognezstraat 172-A
B-1070 Brussels
**32-2-523-6295**
**TLX: 84621646**

**BRAZIL**
Filcres
Rua Aurora, 165
CEP .01209,
Caixa Postal 18767
Sao Paulo
**011-223-7388**
**TLX: 1131298**

Haltronics, Ltd.
205 9th Ave. S.E.
Suite 300
Calgary, Alberta T2G OP8
**403-264-2121**
**TLX: 038-21519**

Haltronics, Ltd.
1085 North Service Rd. E.
Oakville, Ontario L6H 1A6
**416-844-2121**
**TLX: 610-495-2664**

**DENMARK**
Tage Olsen A/S
Ballerup Byvej 222
DK275D Ballerup
**45-2-658111**
**TLX: 85535293**

**FINLAND**
Instrumentarium Elek.
P.O. Box 64
SF-02631 Espoo 63
**35805284320**
**TLX: 57124426**

**FRANCE**
Tekelec Airtronic
Cite Des Bruyeres
Rue Carle Vernet
BP2 92310 Sevres
**33-14-5347535**
**TLX: 204552F**

**HONG KONG**
Protech Components Ltd.
Flat 3,
10/F Wing Shing Ind Bldg.
26 Ng Fong St.
San Po Kong Kowloon
**3-255106**
**TLX: 38396 PTLD HX**

**INDIA**
Shivam Computers PVT Ltd.
9 National Chambers,
near Dipall Cinema Ashram Road
Ahmedabad
**409161(0) 443488(R)**
**TLX: 121539 TRCE-IN**

**ISRAEL**
RDT Electronics Engr. Ltd.
ATIDIM Advanced Technologies Pk.
Neve Sharat
Tel Aviv
**972-3492187, 188, 191**
**TLX: 371452 or 92233551**

**ITALY**
Dott. Ing. Guiseppe De Mico SPA
Viale Vittorio Veneto 8
20060 Cassina De Pecchi
Milano
**02-95-20-551**
**TLX: 330869**

**JAPAN**
Internix, Inc.
Shinjuku Hamada Bldg. 7-4-7
Nishi-shinjuku, Shinjuku Ku
Tokyo 160
**02-537-5091**
**TLX: 13579MSCG P**

Tomen Electronics Corp.
1-1 Uchisaiwai-Cho
2 Chome, Chiyoda-Ku
Tokyo 100
**506-1670-6**
**TLX: 330869**

**NEDERLAND**
Auriema Nederland BV
Doornakkersweg 26
5642MP Eindhoven
**31-40-816565**
**TLX: 84451992**

**NORWAY**
Henaco A/S
Box 126, Kaldbakken
Trondheimsveien 436
Oslo 9
**47-2-16210**
**TLX: 76716 Hanac N**

**SINGAPORE**
Logic Devices PTE Ltd.
68 Orchard Road
#04-32 Plaza Singapura
Singapore 0923
**3390022**
**TLX: RS3481 INHOME**

**SOUTH AFRICA**
Eagle Electric
31-41 Hout Street
Capetown 8000
Republic of South Africa
**451421**
**TLX: 5-21713**

**SOUTH KOREA**
Kortronics Enterprise
Room 307, B-9
#604-1, Guro-Dong, Guro-gu
Seoul,
**634-5497**
**TLX: MICROS K28484**

**SPAIN**
Amitron S.A.
Avenida de Valladolid, 47A
28008 Madrid
**247-93-13/248-58-63**
**TLX: 45550 AMIT-E**

**SWEDEN**
NAXAB
Box 4115
17104 Solna
**08-98-51-40**
**TLX: 17912**

**SWITZERLAND**
Datacomp AG
Zuercherstrasse 20
CH-8952 Zurich Schileren
**41-1-7302165**
**TLX: 854553533**

**TAIWAN**
Sertek International
3 Fl. No. 135
Chien Kuo N. Road, Sec. 2
Taipei
**02-501-0055**
**TLX: 23756 SERTEK**

**UNITED KINGDOM**
Golden Gate
Manhattan House
Bridge Road
Maidenhead, Berkshire SL6 808
**44-628-75851**
**TLX: 851-847898**

Manhattan Skyline
Manhattan House
Bridge Road
Maidenhead, Berkshire SL6 808
**44-628-75851**
**TLX: 851-847898**

**WEST GERMANY**
Atlantik Elektronik Gmbh
Fraunhoferstr. 11A
D-8033 Martinsried
**49-89-8572086**
**TLX: 5215111 ALEC D**

Beka Electronics Gmbh
Bahnhofstrasse 42
D-2000 Wedel
**TLX: 49-410384061**
**TLX: 2789582**

Tekelec Airtronic Gmbh
Kapauzinerstrasse 9
8000 Munich 2
**49-89-51640**
**TLX: 522241**

STANDARD MICROSYSTEMS CORPORATION

# APPLICATION AND TECHNICAL NOTE DIRECTORY

## DATA COMMUNICATIONS

| NUMBER: | TITLE: | USE WITH PART NUMBERS: |
|---|---|---|
| TN5-1 | Using the COM8004 for High Data Integrity in Bit Oriented Protocols | COM8004<br>COM5025 |
| TN5-2 | Using the COM9026 Local Area Controller and the COM9032 Local Area Network Transceiver | COM9026<br>COM9032 |
| TN5-3 | MIL-STD-1533A and MIL-STD-1553B Overview | COM1553A<br>COM1553B |
| TN5-5 | VLSI Circuit Provides Complete Controller for Token-Pass Systems | COM9026<br>COM9032 |
| TN5-6 | Low Cost High Performance Token Pass LAN | COM9026<br>COM9032 |
| TN5-7 | COM7210 GPIB-488 Talker/ Listener Controller | COM7210 |

## DISPLAY PRODUCTS

| | | |
|---|---|---|
| AN1-7 | Horizontal Scrolling with the CRT5037 VTAC® | CRT5037 |
| AN4-1 | CRT9006 Single Row Buffer Enhances Processor Through-put | CRT9006 |
| AN4-3 | Programming and Interfacing to the CRT9007 | CRT9006<br>CRT9007<br>CRT9021<br>CRT9212 |
| AN4-4 | Next Generation CRT Systems | CRT9006<br>CRT9007<br>CRT9021<br>CRT9212 |
| TN4-2 | CRT9007 VPAC® A Next Generation CRT Controller | CRT8002<br>CRT9006<br>CRT9007<br>CRT9021<br>CRT9212 |
| TN4-5 | CRT9028 VTLC™ A New Video Terminal Logic Controller | CRT9028 |
| TN4-6 | A Flexible Approach to Video Graphic Systems using the CRT9007 VPAC® | CRT9007 |
| TN4-7 | Variable Character Size with the CRT9041 | CRT9007<br>CRT9041 |

## FLOPPY DISK/HARD DISK

| NUMBER: | TITLE: | USE WITH PART NUMBERS: |
|---|---|---|
| TN6-1 | Principles of Digital Floppy Disk Data Separation Using FDC9216, FDC9229 or FDC9266 | FDC9216<br>FDC9229<br>FDC9266 |
| TN6-2 | Improved Functionally Simplifies Disk Controller Design | HDC9224 |
| TN6-3 | FDC765A Circuit Recommendation | FDC765A<br>FDC9229 |
| TN6-4 | Using the HDC9226 Hard Disk Data Separator | HDC9224<br>HDC9226 |
| TN6-5 | Programming the HDC9224 Universal Disk Controller | HDC9224 |
| TN6-6 | Programming the FDC765A, FDC9266 and FDC9267 | FDC765A<br>FDC9266<br>FDC9267 |
| TN6-7 | HDC9224 Programmers Reference Card | HDC9224<br>HDC9225<br>HDC9226 |

# GET OUR 1987 CATALOG HOT OFF THE PRESS!

To make sure you receive Standard Microsystems' 1987 Catalog as soon as it's published, please fill out and return the coupon below.

---

STANDARD MICROSYSTEMS CORPORATION

35 Marcus Blvd., Hauppauge, NY 11788 (516) 273-3100

**ATTENTION: Communications Department**

Please put me on your mailing list for the 1987 Catalog.

Name _____ Title _____

Company _____

Address _____ State _____ Zip _____

Telephone _____ Ext. _____
(Area Code)

My application is _____