Solid State
Micro Technology
for Music

SSM 2110

SSM 2110 AUDIO LEVEL DETECTION SYSTEM

DESCRIPTION

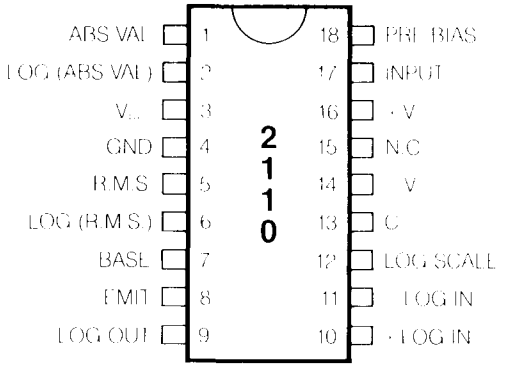
The SSM 2110 is a precision level detection system designed specifically for audio applications. It features both linear and logarithmic (dB) outputs, and unlike previous designs, the dB output can be internally compensated for scale factor changes with temperature.

Two linear outputs, true R.M.S. and absolute value, are available simultaneously and the latter can be alternatively configured to give a peak function. The dB output can provide a log R.M.S., log absolute value or log mean value function. In each case, full on-chip temperature compensation is available.

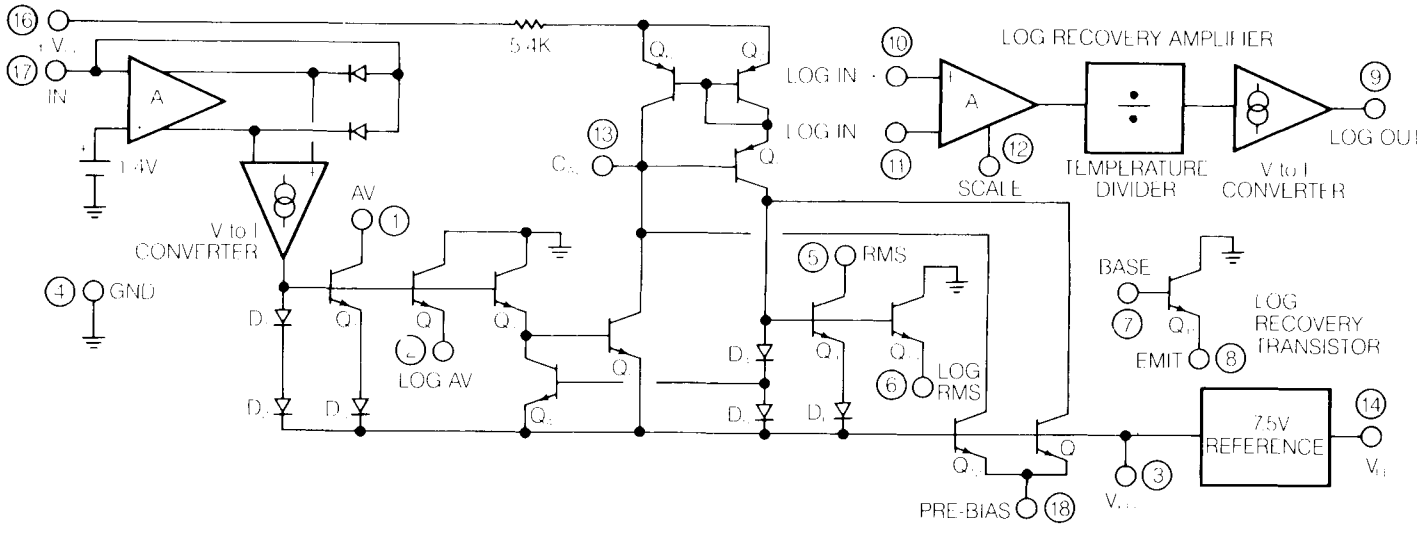
A dynamic range of 100dB is achievable, and a unique pre-bias circuit enables dynamic range to be traded for faster response time at low signal levels.

FEATURES

- Provides all Common Transfer Functions
- Wide Dynamic Range (100dB)
- High Accuracy (0.5%)
- Pre-Bias Option for Fast Response Time at Low Signal Levels
- On-Chip Log Output Amplifier
- Optional Internal Log Output Temperature Compensation
- Low Drift Internal Reference
- High Speed



PIN OUT (TOP VIEW)



BLOCK DIAGRAM

Solid State Micro Technology for Music, Inc., 2076B Walsh Avenue, Santa Clara, CA 95050, USA
(408) 727-0917 Telex **171189**

*PATENTS PENDING

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GENERAL

The SSM2110 is designed to operate off split supplies in the range from ± 12V to ± 18V. Since the level computations of the 2110 are done in terms of currents rather than voltages, the device has an extremely wide dynamic range and bandwidth. The linear outputs, absolute value (pin 1) and RMS (pin 5) are presented as currents while log outputs, log of absolute value and log of RMS, appear as voltages on pins 2 and 6 respectively. The log recovery transistor is an internal level shifting component which may be switched between the two log outputs. This will reference the log output(s) to the internal voltage regulator which is about 7.5 volts above the negative supply. The log recovery amplifier is used to rereference the log output(s) to ground and also to temperature compensate the KT/q term in the log transfer characteristic. This compensation can be defeated for certain applications such as compressor/limiters where the log drift will cancel the thermal gain drift of a VCA dB/volt control port. If the log recovery amp is not used, pins 10 and 11 *MUST* be connected to pin 3 for proper operation of the rest of the circuit.

INPUT (pin 17)

The input (pin 17) is an A.C. virtual ground with about a 1.4V D.C. offset voltage. The useful dynamic range of signal input current the device can process is in excess of 100dB (3 mA to 30nA peak to peak). The input RC network is usually chosen to allow at least 20dB of headroom in order to process high crest factor material and to provide a D.C. block below the audio band. With ± 15 volt supplies, a 10K input resistor will yield the proper maximum input current of ± 1.5mA. If one allows for 20dB of headroom, a nominal signal level would be 300μA pp or 3V pp which is about 0dBV. A very low leakage capacitor must be used as a D.C. block to avoid impairing the dynamic range at low signal levels (many electrolytic types won't work). It is also possible to D.C. couple into the 2110 by using the circuit in Figure 1A. However the low end of the dynamic range will be limited by the resistor matching and the op amp offset.

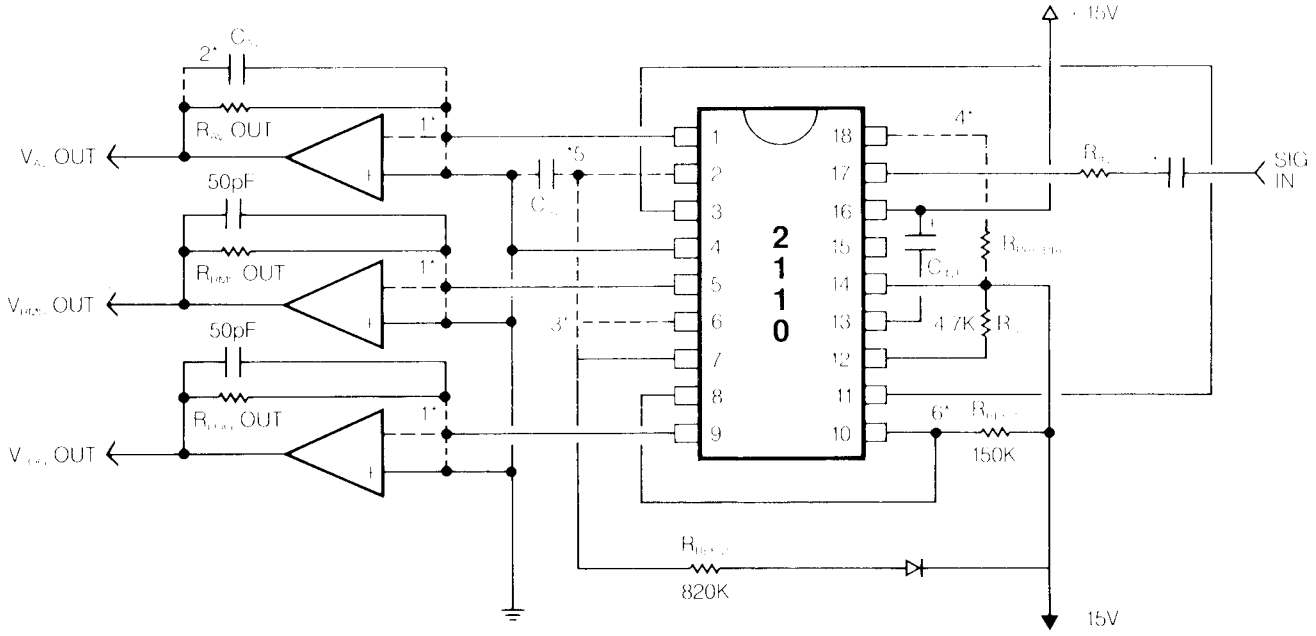


FIGURE 1. 2110 CONNECTION OPTIONS

NOTES:

1). CONNECT OUTPUT PIN(S) TO GROUND IF OUTPUT(S) NOT USED.

2). C_{AV} CAN BE USED TO AVERAGE ABSOLUTE VALUE OUTPUT. A VALUE OF 50pF MINIMUM IS RECOMMENDED TO ENSURE UNCONDITIONAL STABILITY.

3). CONNECT EITHER LOG AV OR LOG RMS TO BASE OF LOG RECOVERY TRANSISTOR.

4). OPTIONAL PRE BIAS CONNECTION.

5). CAP USED FOR AVERAGING LOG OF ABSOLUTE VALUE OUTPUT.

6). PINS 10 AND 11 MUST BE CONNECTED TO PIN 3 IF LOG RECOVERY AMP IS NOT USED.

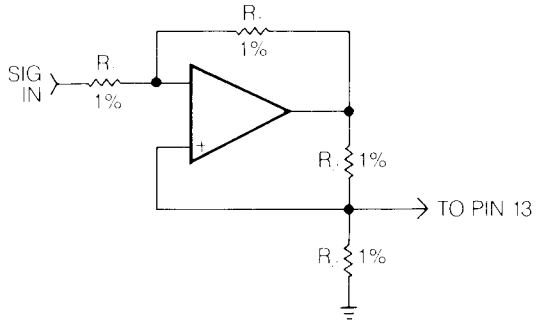


FIGURE 1A

THE RMS COMPUTING LOOP (PIN 13, PIN 5, AND PIN 18)

The RMS section of the SSM2110 consists of an implicit RMS computing loop whose output (pin 5) obeys the equation

$$I_O = I_{IN}^2 / \bar{I}_O \text{ where } \bar{I}_O \text{ is the average of } I_O$$

The time constant for averaging is determined by the value of the averaging cap on pin 13 and an internal resistor whose effective value is 10.8K. Again, a very low leakage cap must be used for C_{INT} to prevent limiting the dynamic range.

The pre bias pin (pin 18), can be used to increase the speed of the RMS computing loop at low signal levels at some expense to the dynamic range. Below a 10μA pp input level the time constant of the RMS loop will increase from its nominal value by a factor of 10 for every 20dB drop in level.

By use of the pre bias pin, one can insure that the loop time constant will not increase above a chosen maximum as the signal level continues to decrease. The equation relating the maximum time constant increase to the resistors value connected between pin 18 and − Vee is given by:

$$\frac{\tau_{MAX}}{\tau_{NOM}} \cong \frac{10\mu A \times R_{PB}}{6.8V} \quad \text{see Fig. 2}$$

LINEAR OUTPUTS (pin 1 and pin 5)

The instantaneous absolute value of the input signal appears as a current into pin 1. The true RMS value of the input signal similarly appears as a current into pin 5. With ± 15 volt supplies the voltage compliance on these outputs is from + 15 to − 6 volts. For simple applications it is possible to convert these currents to output voltage signals by connecting a resistor in series with the pin(s) to ground. For a maximum 3mA pp input signal the resistor(s) value should be 3.6K or less. If one wants an average of absolute value output, a capacitor can be added in parallel with the resistor (fig. 3a).

More commonly a positive going voltage at low inpedance is desired as an output. This can be accomplished by connecting a linear output pin to the virtual ground of an op amp configured as a current to voltage convertor (fig. 3b). The scale factor for the conversion is determined by the value of the feedback resistor. A small capacitor is usually added in parallel with the feedback resistor for stability particularly if a high slew rate FET input op amp is used. This capacitor can be made large to obtain an average of absolute value output. The linear output pins must be kept within their voltage compliance range for proper device operation. An unused linear output should be connected to ground.

A peak output can be implemented by using the circuit in fig. 3c. The output scale factor is determined by Rout. The decay time constant is equal to the product $R_{OUT} C_{HOLD}$.

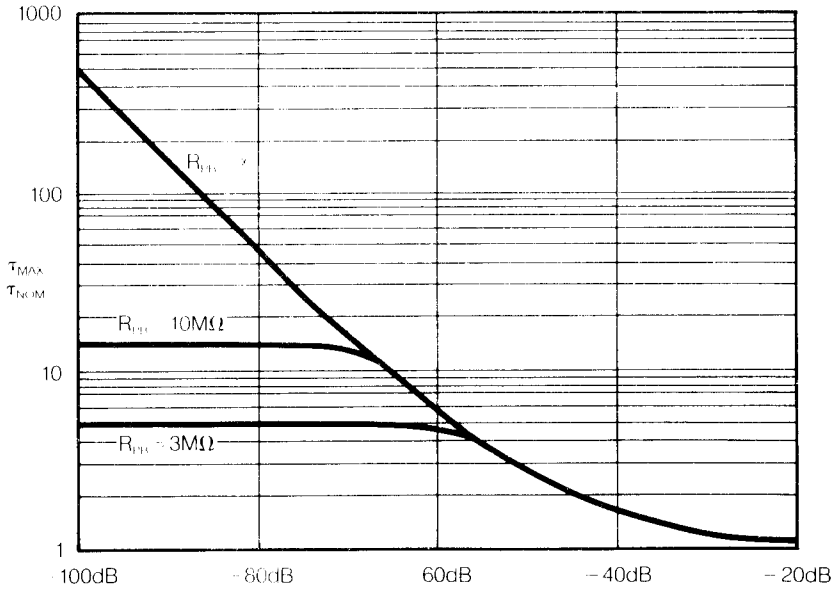


FIGURE 2. NORMALIZED TIME CONSTANT RELATIVE TO 1mA R.M.S.

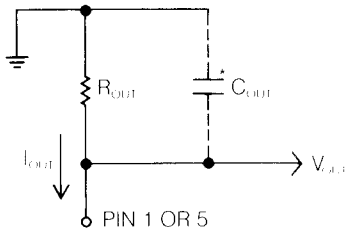


FIGURE 3A.

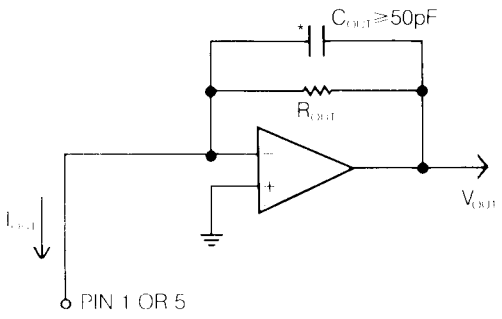


FIGURE 3B.

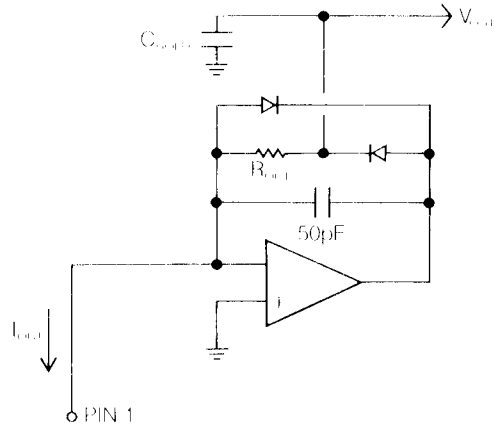


FIGURE 3C.

***CAPACITOR FOR AVERAGING ABSOLUTE VALUE OUTPUT.**

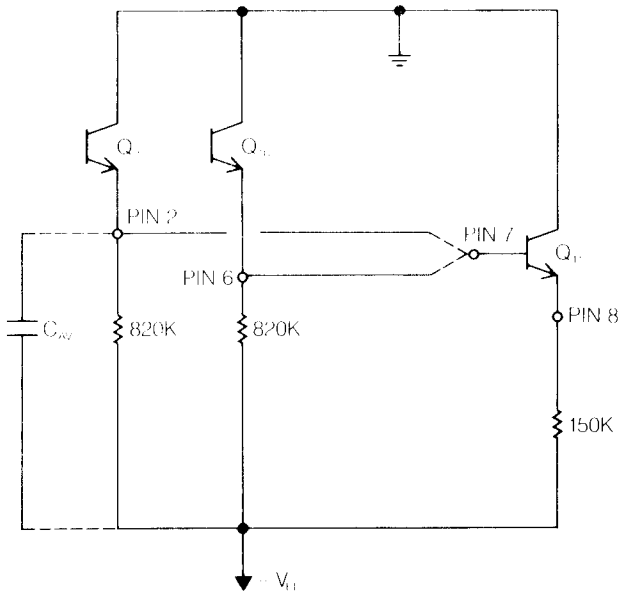


FIGURE 4.

LOG OUTPUTS (pins 2, 6, 7 and 8)

The log of the instantaneous absolute value and the log of true R.M.S. of the input signal appears as voltages on pins 2 and 6 respectively. However, these outputs must be buffered, level shifted and, in many applications, temperature compensated in order to be made useful. Figure 4 shows the recommended connection between the log output transistors Q2 and Q10, and the log recovery transistor Q11. Note that although the log recovery transistor can be switched between the two log outputs, only one log output can be recovered at a time. With the resistor values shown, the output swing at the emitter of Q11 over the dynamic range of the device will be roughly symetrical about the internal negative voltage reference. Also, the output impedance will be low enough to drive the log recovery amp input(s) without introducing significant errors. The output sensitivity at this point is about +60mV for every 10dB of signal level increase at 25°C. This sensitivity has a temperature coefficient of +3300ppm/°C.

The log of absolute value output can be converted to a log of mean value by connecting a capacitor between pin 2 and the negative supply. Since this is an emitter follower output, the response to a large signal level increase will be fast while the time constant of the output following a large signal level decrease will be determined by the product of the averaging capacitor and the resistor from pin 2 to the negative supply.

One might think that connecting a capacitor to the log output would produce the average of the log of the absolute value. However, since the capacitor enforces an ac ground at the emitter of the output transistor, the capacitor charging currents are proportional to the antilog of the signal at the base. Since the base voltage is the log of absolute value, the log and antilog terms cancel, and the capacitor is charged as a linear integrator with a current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging operations. The signal at the output therefore is the log of the average of the absolute value of the input signal.

LOG RECOVERY AMPLIFIER (pins 9, 10, 11, and 12)

The log recovery amplifier is a linearized voltage to current transconductor whose gain can be made proportional to absolute temperature. One input is usually connected to the emitter of the log recovery transistor while the other is connected to the internal voltage reference (pin 3). The output current at pin 9 is given by:

$$I_O \text{ (pin 9)} = \frac{2\,[\,V \text{ (pin 10)} - V \text{ (pin 11)}\,]\,1.25V}{1.8K \times 280\mu A \times \text{Rscale}}$$

This corresponds to about 3.2μA/dB. 1.25 V is the voltage across the Rscale resistor which is connected between pin 12 and the negative supply. A value of 4.7K for this resistor gives best overall linearity and temperature compensation performance which is an improvement of about a factor of 40 over the uncompensated drift. If one connects a 2K resistor in series with a silicon diode from pin 12 to the negative supply, the temperature compensation can be defeated for compressor/limiter applications. The maximum output current for both the compensated and uncompensated examples above is ±260μA. The output current can be converted to a voltage with the circuit in Figure 5. Usually, one would like the output range to be from ground to +5 or +10 volts. This circuit allows for an arbitrary choice of range and scale factor. The offset and scale factor trims can be used to improve unit to unit repeatability.

The SSMT applications staff is available for questions on this or any other SSMT device.

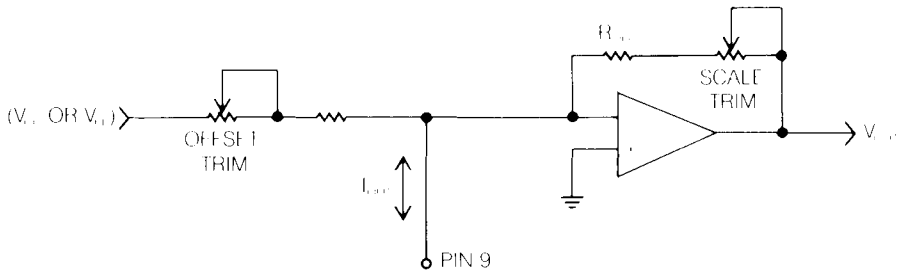


FIGURE 5.

SPECIFICATIONS*

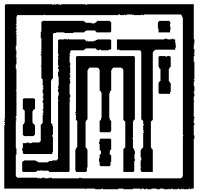
OPERATING TEMPERATURE
−25°C to +75°C

STORAGE TEMPERATURE
−55°C to +125°C

The Following Specifications Apply for $V_s = \pm 15V$, $T_A = 25°C$ and $R_{scale} = 4.7K\Omega$ unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Useful Dynamic Range	100	110		dB	50nA pp ≤ I_{IN}pp ≤ 5mA pp
Linearity Error					
Mean Output 40dB Dynamic Range		.005		dB	
60dB Dynamic Range		.04		dB	
80dB Dynamic Range		0.25		dB	
RMS Output 40dB Dynamic Range		.005		dB	
60dB Dynamic Range		.04		dB	
80dB Dynamic Range		0.25		dB	
Unadjusted Gain (pin 1 or pin 5)	0.475	0.500	0.525		@ I_{IN} = 1mA
Error (Mean or RMS)			±0.5	dB	
Output Offset Current (Mean or RMS		5	20	nA	@ I_{IN} = 0
Shift of I_{OS} with $R_{prebias}$ = 3MΩ (RMS Only)		50	120	nA	@ I_{IN} = 0
Crest Factor @ 1mA RMS					
For 0.1dB Additional Error		2.5			
For 0.5dB Additional Error		5			
For 1.0dB Additional Error		8			
RMS Filter Time Constant (I_{RMS} > 10μ ARMS)		11KΩ x C_{INT}			
Frequency Response (Sine Wave)					
For 0.1dB Additional Error					
I_{IN} = 1mA RMS		400		kHz	
I_{IN} = 10μA RMS		10		kHz	
I_{IN} = 1μA RMS		2		kHz	
For 0.5dB Additional Error					
I_{IN} = 1mA RMS		1000		kHz	
I_{IN} = 10μA RMS		50		kHz	
I_{IN} = 1μA RMS		7.5		kHz	
−3dB Bandwidth					
I_{IN} = 1mA RMS		1500		kHz	
I_{IN} = 10μA RMS		300		kHz	
I_{IN} = 1μA RMS		50		kHz	
Log Amp Output Offset Current (pin 9)		±3.3	±10	μA	
Max Log Amp Output (pin 9)	±250	±265	±280	μA	
Log Scale Factor (pin 2 or pin 6)		±6		mV/dB	@ 25°C
Log Mode Zero Crossing (Mean or RMS) (pin 9)		10		μA	RMS in to get zero out
Log Amp Linearity (pin 9)		0.1	0.25	dB	±240mV −240mV ≤ $V_{PIN10} - V_{PIN11}$
Log Output Tempco (pin 9)		±75	±150	ppm/°C	0°C ≤ T_A ≤ 75°C
V_{REF} (pin 3 to $-V_{EE}$)	7.0	7.5	8.0	V	
Positive Supply Current (Quiescent)	320		500	μA	I_{IN} = 0
Negative Supply Current (Quiescent)	2.1	2.63	3.30	mA	I_{IN} = 0
Supply Voltage Range	±12		±18	V	

*Finial specifications subject to change.

Solid State Micro  **Technology**
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