Signetics

74LS1812
Bit Stream Manager

Serializer/Deserializer
Preliminary Specification

Logic Products

DESCRIPTION

The 74LS1812 Serializer/Deserializer (Figure 1) incorporates speed, flexibility, and proven ISL technology into a general-purpose device that performs many of the functions necessary for the implementation of a disk or communications controller. On-chip serializing/deserializing, programmable ECC and CRC operation, and bit comparison logic (useful for address-mark or header comparisons) make for a truly versatile device. A selectable 8- or 16-bit data bus and associated control lines allow for a DMA interface which requires little external hardware — a minimum system may be easily built with a microcontroller, a DMA controller, a RAM buffer, disk control lines and interface logic.

FEATURES

- **Data rates up to 30MHz**
- **Selectable CRC-16 or CRC-CCITT polynomials**
- **Full Duplex operation with CRC/ECC on receive data**
- **Programmable ECC polynomial register**
- **Programmable control register**
- **On-chip bit comparator**
- **8- or 16-bit selectable data bus**
- **48-pin DIP or 68-pin PLCC**

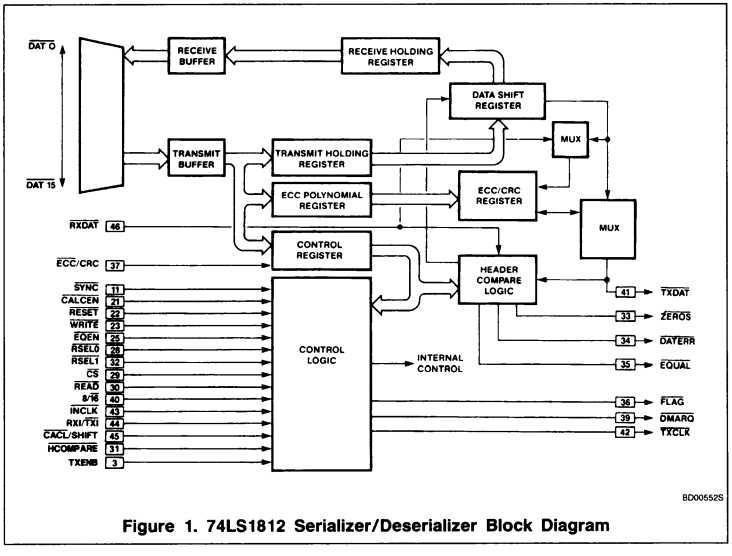
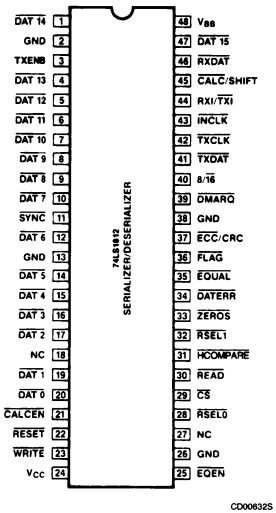
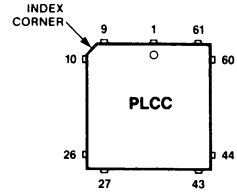


Figure 1. 74LS1812 Serializer/Deserializer Block Diagram

PIN CONFIGURATION





PLCC	FUNCTION	PLCC	FUNCTION	PLCC	FUNCTION
1	VBB	24	DAT 2	47	ZEROS
2	DAT 14	25	NC	48	DATERR
3	GND	26	NC	49	EQUAL
4	NC	27	NC	50	FLAG
5	DAT 13	28	DAT 1	51	ECC/CRC
6	DAT 12	29	DAT 0	52	NC
7	DAT 11	30	CALCEN	53	GND
8	NC	31	NC	54	DMARQ
9	TXENB	32	RESET	55	NC
10	NC	33	NC	56	8/16
11	NC	34	WRITE	57	TXDAT
12	DAT 10	35	VCC	58	TXCLK
13	DAT 9	36	EQEN	59	NC
14	DAT 8	37	GND	60	HCOMPARE
15	NC	38	NC	61	NC
16	DAT 7	39	RSEL0	62	NC
17	SYNC	40	CS	63	INCLK
18	DAT 6	41	READ	64	RXI/TXI
19	GND	42	NC	65	CALC/SHIFT
20	NC	43	NC	66	RXDAT
21	DAT 5	44	NC	67	NC
22	DAT 4	45	NC	68	DAT 15
23	DAT 3	46	RSEL1		

7